Andrea Zuccollo

Spread Spectrum Modulation Techniques for Switch-Mode Power Converters

Tesi di Laurea Magistrale

Università degli studi di Padova

Ottobre 2012

Università degli studi di Padova

Facoltà di Ingegneria

Dipartimento di Ingegneria dell'informazione

Nuovissimo Ordinamento

Corso di Laurea Magistrale

In Ingegneria Elettronica

Tesi di Laurea

Spread Spectrum Modulation Techniques for Switch-Mode Power Converters

Laureando: **Andrea Zuccollo**

Relatore: **Prof. Andrea Neviani**

Anno Accademico: **2011-2012**

Dedication

To my family, my friends and all people I love

Acknowledgements

I would like to warmly thank my advisor Prof. Andrea Neviani and my technical advisors Ing. Cristian Garbossa and Andrea Vecchiato for their guide and support during my thesis work, and for the opportunities given to me to grow up professionally joining Infineon Technologies in Padova. A special thank to all the colleagues in the Standard Team in the Padova Design Center for the nice time we spent together and for all the technical teachings and support. This activity have been entirely sponsored by Infineon Technologies Italia, I would like to thank all the colleagues for the nice experience I had during my ten months stage period in particular for the huge opportunity to grow both professionally and personally. Finally my thanks go to my family, who always supported me in my academic career and always encouraged me to do what I like and I am interested in, as well as to my friends, for being always close to me.

Contents

Chapter

List of Tables

Table

List of Figures

Figure

Abstract

Potential problems related to Electromagnetic emissions Interference (EMI) is a growing concern as more and more systems in automotive environment are being electrified. The problems related to EMI have of course been present for as long as the presence of electrical equipment, but nowadays electrical equipment is squeezed into smaller volumes. Thus, potential problems are imminent if the design of each equipment or component is not properly considered. EMI is a process by which disruptive electromagnetic energy is transmitted from one electronic device to another via a propagation paths. In an automotive electronic system, EMI can adversely affect the performance of an integrated circuit internally, as well as that of other electronic components in close proximity. Identifying the magnitude of different contributions of interference can provide hints of how to approach problems of EMI. This awareness shall give the designer the possibility to deal with possible future problems at an early stage in the design phase. From literature, Spread Spectrum Frequency Modulation seems to be one promising technique to reduce conducted EMI, at the source. The aim of the thesis is to investigate the conducted EMI properties, of switching systems like DC-DC converters by simulations, and to develope a solution which can help to mitigate these emissions, in order to accomplish normative standards. The main purpose of the thesis is then the development of a standalone and configurable clock generator chip solution to apply a Spread Spectrum Modulation to a DC-DC converter, and specifically designed for automotive target.

Chapter 1

Introduction

Potential problems related to Electromagnetic Interference (EMI) is a growing concern as more and more systems in our environment are being electrified. The problems related to EMI have of course been present for as long as the presence of electrical equipment, but nowadays electrical equipment is squeezed into smaller volumes. Thus, potential problems are imminent if the design of each equipment or component is not properly considered. Everyone have probably noticed the annoying interference caused by cellular phones which gets amplified in sound equipment which can be seen as a tolerable disturbance. However if the interference was related to the airbag deployment of a car, life threatening situations can arise which of course is not acceptable.

Identifying the magnitude of different contributions of interference can provide hints of how to approach problems of EMI. This awareness shall give the designer the possibility to deal with possible future problems at an early stage in the design phase.

EMI is a very wide concept covering various types of different phenomenon. During this thesis work the Device Under Test (DUT) is only seen as a source of EMI and not as a victim. EMI emissions can take form of both conducted and radiated and thus can influence its surroundings in different manners. There are many aspects which have to be considered but this thesis only deal with conducted emissions.

The aim of the thesis is to investigate the conducted electromagnetic emission properties, of switching systems like DC-DC converters by simulations, and to develope a solution which can help to mitigate these emissions, in order to accomplish normative standards. The main purpose of the thesis is then the development of a standalone and configurable clock generator chip solution to apply a Spread Spectrum Modulation to a DC-DC converter, and specifically designed for automotive target.

The target application of the circuit is an unfair ambient for a chip because when placed inside vehicles, chips must be able to work correctly even with a widely variable supply voltage range and temperature range; they also must be provided of several protection subsystems that will avoid any failure in all the possible working conditions could happen: ESD and short circuits at the output are just some of the issues that must be kept in mind developing a circuit made specifically for this target application.

This thesis is developed logically in several parts, corresponding to different chapters. A summary of these chapters is presented below.

1.1 Outline of the thesis

This chapter contains a brief introduction to the thesis and the work that is presented. In Chapter 2 the electromagnetic environment within a vehicle is described. The chapter starts with an overview of automotive electronics, showing how this market has become important in the last years, inducing the development of specifically designed electronics. The chapter contains a short historic survey. In order to solve a problem, it is essential to have some knowledge about the background. An introduction to electromagnetic compatibility in vehicles is given for those who have no prior knowledge in this area. Here are the different coupling paths in a vehicle, and also some parts of the electrical system described. Most of the carriers are not a pure sine wave but a set of harmonics, as example, in SMPS, a Pulse Width Modulation (PWM) signal is to be found. The last part of the chapter explains the theory behind pulse width modulation and how to deal with these generic waveforms consisting of infinity of harmonics.

One of the principle causes of EMI in an automobile is coincident with a switching regulator imposing AC currents on the supply harness. These changing currents express themselves as harmonically rich waveforms that radiate and conduct emissions. Chapter 3 focuses on mitigation techniques of the conducted EMI, specifically as generated by a step-down converter, so some mitigation techniques for radiated EMI, aren't discussed. Several techniques to mitigate conducted electromagnetic interference (EMI) in switch-mode power supplies (SMPS) have been reported in literature. To keep the scope the of the chapter limited and focused, the survey only deals with mitigation of conducted EMI in DC-DC power converters. The reduction of the noise can be performed after generation, or at the generation stage itself. These condicted EMI mitigation techniques are

subdivided into different types, and then, detailed reviews on each technique are presented. In particular, the Spread Spectrum Modulation (SSM) techniques are introduced in this chapter.

The simulation software and the model are described in Chapter 4. The chapter introduces a software tool developed during the thesis work. The tool was developed to understand theoretical and real benefits of Spread Spectrum Modulation techniques, and benchmark the reduction of conducted EMI emissions from a generic Switched Mode Power Supply that these techniques can provide. Several Spread Spectrum Modulation techniques are investigated. All these techniques can be found in literature and many articles have shown their respective results obtained by applying different Spread Spectrum modulations. Therefore, with this new software tool a verification of the techniques available in literature can be done. In general conducted EMI analysis and specially Spread Spectrum Modulation techniques are topics quite difficult to understand for beginners, moreover, there are many different standardized test measurement setups. The developed tool is really user friendly and lets the user "to play" with all the SSM techniques and profiles, with all the several modulation parameters, in different test measurement setups. Follows a description of the tool's Graphical User Interface (GUI), and a brief explanation about the Matlab source code and the structure of the algorithm.

Using the simulation Matlab tool it is possible to obtain the theoretical behaviour of the different modulation profiles of interest: sinusoidal, triangular, hershey-kiss, multi-slope triangular, compensated, pseudo-random and chaotic. This way, chapter 5 is intended to completely understand and analyze the theoretical behaviour of these modulation profiles and to quantify the conducted EMI reduction according to several significant measure parameters. Afterwards, a comparison of these modulation profiles is carried out. After all aspects of frequency modulation by means of SSCG methods have been theoretically developed, it is mandatory the verification of the theoretical conclusions. Most practical considerations are here dealt with, like the influence of the Spectrum Analyzer's Resolution Bandwidth (RBW) on the measured EMI, a proposal of a practical method to apply a SSCG technique applied to Switching Power Converters and comparative measurements of conducted EMI within the range of conducted emissions.

Chapter 5 takes profit of the results obtained in Chapter 6, to build a standalone solution for a Spread Spectrum Clock Generator (SSCG) to apply a Spread Spectrum Modulation (SSM) to a SMPC. Initially, there is a dissertation about smart power technology (SPT) that is used for

the project that is going to be developed, in the specific about SPT Infineon technology. Some practical considerations about the architecture of the SSCG solution are here dealt with. The analysis of the standalone concept architecture takes place, where the circuit is first subdivided into the main circuit blocks to study them separately in an easier manner. The main blocks to developed are a master current controlled oscillator, a voltage-to-current converter configurable by external resistors, a modified triangular oscillator as profile generator and finally a frequency divider. After an introduction about the typical oscillators structures, and about the advantages and disadvantages of each different types, the best architecture for both oscillators are selected. The chapter then goes on with a complete description and sizing of the different circuit blocks.

Chapter 6 describes the simulation setups and results that are performed in order to verify the circuit design. A short summary of the results and some reflections are finally presented in Chapter 7.

Several annexes have been included at the end of this document. Some of them are direct references to the thesis and the rest are included because they were considered to be of interest.

In Appendix A a buck converter is used as an example of DC-DC converter because of its wide use and ease of understanding. The basic operation of a buck converter is overviewed in this appendix addressing the most common modes of operation. Power losses in the converter are addressed as well, in order to motivate the choice of the operating mode accordingly to the load condition of the converter.

Therefore, a brief overview of the area of electromagnetic compatibility is given in Appendix B. Definitions, different coupling paths for disturbances, differential and common mode, conducted emissions are described.

In Appendix C and D respectively present measurement instruments, like the spectrum analyzer and the scanning receiver, and automotive standards about conducted emission interferences, like the CISPR 25 and the IEC 61967-4.

A passive component can no longer be regarded as a perfect resistor, inductor or capacitor, as the frequency contents of the signal or current/voltage increases. For example a resistor begin to behave more and more like an inductor. As the frequency is increased, or decreased depending on the reference point, all parts of the circuit begins to suffer from a behavioral change. The PCB itself could start act as a very effective antenna at a certain operating frequency. In Appendix E

these aspects are treated.

In Appendix F, a wide theoretical development of the modulation and related concepts are presented. It is explained generically all aspects related to the frequency modulation. Main parameters of frequency modulation are presented and explained in detail and how practical considerations may affect to the theoretical behaviour of these parameters.

Theoretical basis of the thesis is based on the fundaments of the Fourier Transform and the related computational algorithm is a particular implementation of the Fast Fourier Transform (FFT). The computational algorithm developed and treated in Chapter 4 is intended to obtain the theoretical spectral components resulting from the frequency modulation process. This algorithm was developed for a MATLAB environment, thus, some particularities more must also been taken into account. Therefore in Appendix G a sufficient explanation was thought to include for a right understanding of how to apply FFT correctly to the MATLAB algorithm, using the windowing and interpolation functions.

Finally Appendix H give a brief theoretic basis about the phase noise in oscillators and the relative timing jitter phenomena.

Chapter 2

EMC Automotive Background

Since the introduction of electronics for emission control on engines, the evolution of electronics in automobiles has advanced rapidly. Recently it has been incorporated on new automotive subsystems and it has become standard implementation on many others; such features as antilock braking systems and airbag could only be achieved practically through the use of electronics, now these features are becoming standard features owing to strong pressure in the highly competitive automotive market.

Nowadays electronics are being widely used in automobile and probably will be used even more in the future. Power electronics plays an increasingly important role in improving vehicle performance, fuel economy, emission, safety and comfort; so power semiconductor devices are widely used in automotive power electronic systems, and often dictate the efficiency, cost and size of these systems.

2.1 Historical survey

In 1892, an edict issued by the German parliament and signed by Wilhelm II, Kaiser of Germany and King of Prussia, indicated that in the event electromagnetic disturbances perturb the correct operation of telegraph cables or telegraph equipment, the owners of the appliances that are responsible of causing the disturbances should solve the problem and indemnify the owners of the telegraph cables and telegraph equipment whom he has disturbed. This edict is an important milestone in the history of EMC in the sense that it was the first known regulation to be adopted which attempted to make electrical appliances compatible with each other.

The first consumer product to be subjected to electromagnetic compatibility legislation in the United Kingdom was the car. This was due to broadband impulsive noise from the spark ignition

system, which originally was of sufficient magnitude to cause interference to domestic television reception. In 1952, the Parliament enacted a Statutory Instrument to limit this interference.

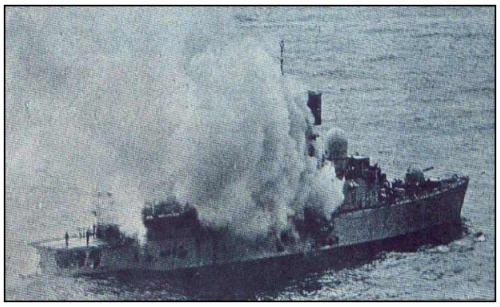
The first EMC problem between two different appliances that has been the subject of intensive studies and scientific investigations, is the radio receiver which is fitted in a car. The primary cause for this generated interference is the motor noise, which is picked up and conducted over long power lines and into sensitive equipment. While the US military encountered interference problems prior to World War I when trying to equip a car with a radio, little is known about the first efforts to minimize or at least find ways to counter or shield this interference. After the First World War, the radio technology which was used and perfected during the conflict, blossomed into civilian broadcasting. As more and more radio transmitters were built, it became necessary to assign different frequencies to various types of radio uses on an international basis in order to avoid interference. Aside from the harmonics generated by neighboring radio transmitters, radio receivers were in turn susceptible to adjacent channel interferences as well as to the unsuppressed impulsive noise generated by electric motors and ignition systems. The radio receiver which fitted into a car was consequently very susceptible to these disturbances, and it is therefore no wonder that its EMC performance has been observed and studied intensively from then on.

The awareness of EMC kept growing throughout the second World War, where new systems like radar emerged, and on-board radio communication became more prevalent in cars, aircraft and ships. The metal superstructure of aircraft provided excellent (yet unpredictable) energy transfer paths between various systems, and the armament and fuel tanks were consequently susceptible to ignition by sparks caused by large radio frequency fields. Additionally, intermodulation products originating from radio transmitters caused by the nonlinear electrical properties of metal joints corroded by seawater, disrupted various radio receivers on ships. Opposed to this, radio and radar jamming which are a form of intentional electromagnetic interference, were extensively developed and used during the second World War as well, e.g. to perturb the reception of the BBC throughout Nazi occupied Europe and to disturb the radio communication of enemy planes.

During the post-war period and through the 1960s, EMC was primarily a concern for the military, for example to control and regulate radar emissions which could (and in some cases did) cause inadvertent weapons releases by interfering with electronic fire mechanisms. The military dominion in EMC related matters changed radically after the massive home computer proliferation

(a) UH-60 Black Hawk. Most of its crashes since 1982 were caused by flying too close to radar and radio transmitters and even citizens band (CB) transmitters, because of the susceptibility of the electronically controlled flight system to these EME

(b) On May 26 1991 the Lauda Air flight 004 crashed into a jungle shortly after taking off from Bangkok. It was supposed, that EMI from a camcorder, a laptop or a mobile phone could have turned on the left engine thrust reverser



(c) On May 30 1986 the UK lost the destroyer HMS Sheffield. Because of interference between the communication radio system with the antimissile detection system, this last one was turned off during communications. Unfortunately this coincided with the enemy missile launch

(d) F-15 destroyed by Human ESD contact caused by an improperly grounded fuel container during maintenance

Figure 2.1: Examples of EMC problems

starting from the 1970s. Indeed, interference problems from computing devices became a significant problem to radio and television broadcasting. In order to limit and control these interferences, various national instances as the FCC in the USA (Federal Communications Commission), or the CISPR (Comité International Spécial des Perturbations Radioélectriques) of the IEC (International Electrotechnical Commission) in Europe, started to compile a set of rules to regulate the amount of emissions, and how the measurements of these electromagnetic emissions were to be performed.

When different circuits and systems are densely integrated in the same appliance, the parasitic electromagnetic coupling between these circuits sharing the same printed circuit board (PCB), power supply and ground lines, is indeed a critical design parameter that can no longer be safely excluded from a product design flow, in fact small PCB tracks and wires pick up the disturbing signals just

as easy as long power supply lines which picked up the motor noise and injected this into sensitive electronic appliances.

2.2 EMC in automotive applications

The automotive industry is particularly interested in increasing the EMC performances of electronic circuits and systems, since the automotive electromagnetic environment can be very severe and (owing to the inherent mobility of automotive applications), most unpredictable. In order to ensure that vehicle accidents are not caused as a result of EMC incompatibilities, vehicle manufacturers as well as electronic sub-assembly (ESA) companies go to enormous lengths (driven by severe product reliability legislation) to ensure that their vehicles do not suffer from EMC problems. It has been claimed that occasional and untested EMI events that could cause a safety incident only once during a 10-year vehicle life, can still expose drivers to safety risks comparable with those of the world's most dangerous occupations[1] . In the next few years, the importance of EMC-proof applications within a vehicle is bound to increase even more. This implies that electromagnetic compatibility is of paramount importance in order to assure the correct functioning of an automobile.

In the 1950s and 1960s, the number of cars with a car radio increased significantly and this required a greater degree of suppression in order to reduce the audio interference to an acceptable level. The extra suppression had to compensate for both the closer vicinity of the receiver antenna to the ignition system and the relatively low level of the desired signal provided by a car antenna. There was an additional EMC phenomenon that was introduced, conducted interference, which also could cause audible interference noticeable on the radio. The conducted interference arose from transients generated by the ignition system or other vehicle electrical devices that were conducted into the radio by the 12 V power supply leads.

The solid-state electronic devices were introduced into the vehicle electrical system in the early 1970s. Initially, discrete semiconductors were used in alternators, radio and ignition system.

[1] *A simple analysis based on reasonable assumptions for a 6-cylinder engine at 2000 rpm with spark-ignition transients lasting 50 ns, shows that in each minute there is a 0.001% likelihood of an overlap of at least 50% with a 100 ns transient that occurs once every minute (on average, for example due to the actuation of an electric motor or solenoid). If the vehicle is driven for 1 hour/day, 5 days/week, 40 weeks/year, the likelihood of such an overlapping pulse event is 12% per year. And if the overlapping pulses caused an electronic sub-assembly (ESA) to malfunction with a 1% chance of death, the driver would have a risk of death of 0.12% per year. This compares with a death rate of about 0.1% per year for very hazardous occupations (e.g. oil industry divers).*

When the semiconductors were used in the vehicle it was important to ensure that that they could withstand the high voltage transients present on the vehicle harness.

In the mid-1970s large-scale integrated circuits and microprocessors began to be used for the control of vehicle functions, which previously had been implemented by purely mechanical means. Over the last two decades, the incorporation of electronics into cars and other vehicles has increased with an exceptional rate and continues to do so. The electrical system in a relatively modern car constitutes at least 20% of the vehicle's total cost. This means that the electrical system of the car costs more than the motor and the transmission together. A modern car today has due to this trend more on board computing power than the Apollo spacecraft of the 1960's.

There are two key reasons for the rapid increase in vehicle's electronic content. Firstly, the price of crude oil rose dramatically in the 1970s, which also caused the cost of petrol to rise. This triggered governments and drivers to demand more fuel efficient cars. At the same time, limits were imposed on the level of exhaust gas pollutants in order to reduce the problems of city smog. To be able to meet these requirements it was necessary to use complex engine management systems to accurately control the spark timing and the air/fuel ratio. Electronic systems were of vital importance to perform this task, which was beyond the capabilities of a purely mechanical system. The availability of the microprocessor enabled the execution of complex calculations atspeed and at a much lower cost than was previously possible. Secondly, customers today are demanding features that only the electronics can provide. Some of these features are for safety purposes, such as traction control and antilock braking systems; some are for instrumentation such as engine speed indicators and trip computers; and some are for convenience such as intermittent wiper and cruise control. There is also a new category of cars, the hybrid cars, where the internal combustion engine is accompanied by one or more electrical motors.

The number of electrically driven loads in a vehicle is increasing, which means that many different systems should be squeezed into an already crowded space. It is usually not possible to keep the power electronic converter, which often is a central unit for different systems, close to the load. The distance between the power electronic converter and the load requires long conductors. In order to keep the cost, weight and assembly work at a minimum; the conductors that are used are often unshielded. It is also common to use the body sheet metal of the vehicle as a current return path, and thereby saving the cost and weight of a current return conductor.

As the electronics systems become more complex, the wiring systems turn out to be a major cost in the manufacturing process. They turn out to be a major failure point also. Placing a large amount of electrical and electronic systems into a very confined space poses the problem of keeping the Electromagnetic Interference (EMI) of these systems from interfering with each other through radiated and conducted emissions. If not properly controlled, the interference can cause each system to malfunction, and even fail. With most systems now fully electronic, the need to contain EMI is more vital than ever. There is the need of containing and suppressing their EMI potential with each other through several solutions.

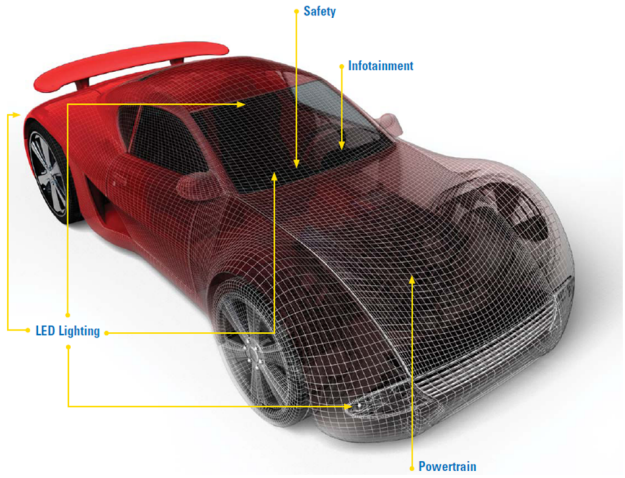
But, what is EMI? EMI is a process by which disruptive electromagnetic energy is transmitted from one electronic device to another via a propagation paths. In an automotive electronic system, EMI can adversely affect the performance of an integrated circuit internally, as well as that of other electronic components in close proximity.

Another EMI issue involves intentional transmitters such as mobile phones, Bluetooth devices, and even commercial broadcast signals. The EMI of these external sources will interfere with the vehicle's electronic system when the vehicle is in close proximity to the transmitting antenna. In short, the new automotive electromagnetic environment is a very complex one involving many internal and external factors.

2.3 EMI Sources and Potential Receptors Internal to the Vehicle

There are two distinct differences between the automotive EMC environment and the commercial EMC environment. First, the mobility of an automobile permits it to travel into many different electromagnetic situations. Obviously, automotive electronics are close to spark ignition systems, both onboard and from neighbouring vehicles. It is expected that the vehicle will remain operational in any-and-all of these environments. The second difference is the safety-critical nature of many of the functions now performed by ECUs on the vehicle. EMI problems can manifest themselves as simple nuisances such as static on the radio. Or they can create a dangerous problem such as loss of control of the vehicle. The term *electronic sub-assembly* (ESA) refers to almost any electrical or electronic device fitted to a vehicle. Special care must be given to *mission critical* systems; especially those that deal with the control and safety of the vehicle. Some of these internal systems include:

- Collision avoidance radar
- Console applications
- Navigation-radio combination
- Power steering module (EPS)
- Infotainment head unit
- Airbag inflator
- ECU and other module connector
- Tire pressure monitoring
- DC motors
- Ignition system
- Engine control module
- Electronic Braking Systems
- Fuel Control Systems
- Adaptive cruise control



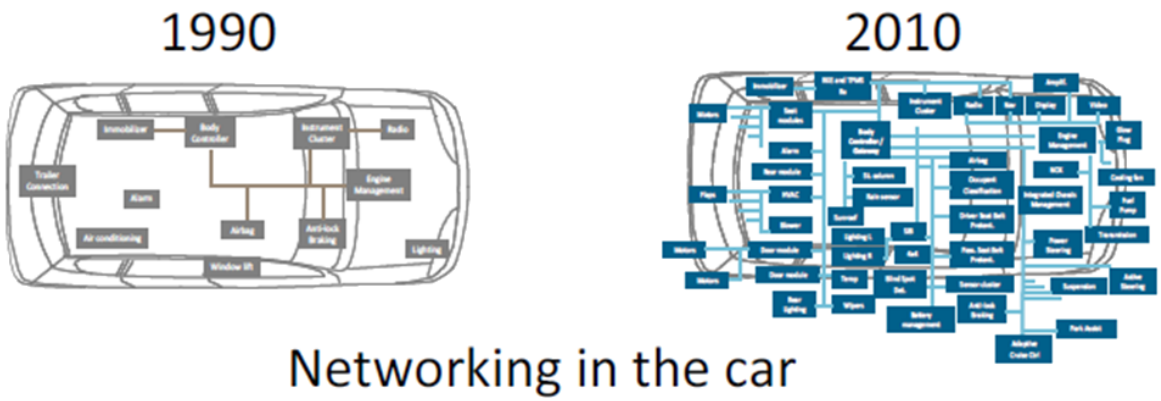
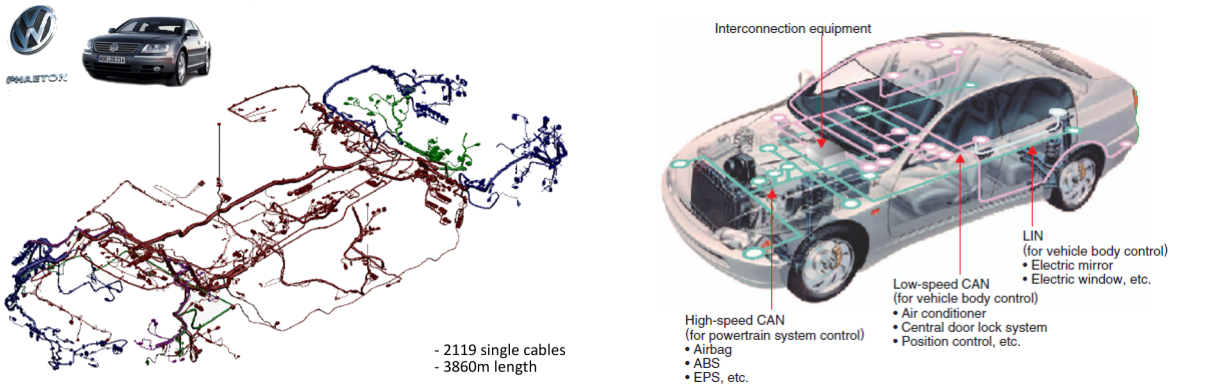


Figure 2.2: Networking evolution in the car

As ever more automotive components are being added, vehicles that employ automotive LAN networks, such as LINs (Local Interconnect Networks) and CANs (Controller Area-Networks), are rapidly increasing, causing the number of ECUs per vehicle to increase year by year. An example of an automotive network employed in a vehicle is illustrated in Figure 2.3(b). Corresponding

to this trend, the demand for automotive electronic components, including EMC countermeasure components, is growing remarkably.



(a) (b)

Figure 2.3: a) Example of cable wiring in VW Phaeton; b) Automotive network in a generic vehicle.

Due to the increase in the number of ECUs in vehicles, noise problems, such as noise interference between ECUs and noise intrusion from power lines, tend to occur more often. In addition, as today's automotive designs use brushless motors rather than conventional brush motors for the EPS and due to the introduction of PWM (Pulse Width Modulation) control for EPSs to meet the need for higher durability and output, the band and level of noise has been growing wider and higher. This also raises the need for a higher level of EMC countermeasures.

2.4 Automotive ground system

Although there is a trend in the automotive industry towards composite or plastic body panels in vehicles, the majority of vehicle bodies still have a significant metal content, with the body and chassis connected to the negative terminal (ground) of the vehicle battery. Even where the body is primarily glass-fibre or other non-metal material, the wiring is usually close to the metal chassis and hence close to the vehicle reference ground. Due to its size, shape and convenient localization (i.e. adjacent to most electrical components), the body sheet metal offers a unique opportunity for current return paths, potential referencing, shielding, and noise reduction. The large surface area and the folded shape of the body sheet metal offer a significant self-capacitance. It has been found that the body sheet metal is an effective sink for low frequency small noise currents. Using the body sheet metal for these purposes increases the risk for common impedance coupling. This is especially

a problem when the current has to pass through body panel joints. An indiscriminate use of the body sheet metal as a universal current return path could furthermore eliminate its beneficial features and create a significant source of radiated emissions. Also, this is not a proper way to ground since the body sheet metal has a high impedance due to the fact that the metal panels often are joined by spot welds or bolts with intervening layers of nonconducting corrosion inhibitor, or with nonconductive paints. The body sheet metal could also be used for low frequency capacitive shielding. For frequencies above a couple of kHz, the body sheet metal creates a modest electromagnetic shielding of the engine compartment as a result of its skin depth. It is also the primary conductor through which the vehicle is shielded from lighting, human generated electrostatic discharges and external sources of radiation. The body sheet metal should also be connected to the battery negative through a robust low-impedance bond. These kinds of connections are seldom present in a body sheet metal. To use a cable for ground return is a good way to protect against unwanted magnetic fields. When a cable is used for return, it is important to place the lead-in and return cable as close to each other as possible. The increased number of electrical loads leads to an increased amount of cables in the vehicle. The cables are routed tightly together, and the chassis is often used as a ground return path. Although there are not very many alternatives for cable routing due to spacing and cost, the alternatives that are present should be taken into account when designing an electrical system.

In a vehicle, the term ground is often used as a description of conductors which function as:

- a current return path,
- an equipotential conducting surface that provides a voltage reference level for analogue sensors and digital logic,
- shielded conductors which are used as a bypass for radio frequency currents,
- a drain for electrostatic charges.

The differences between the automotive and commercial electrical systems give rise to significant differences between the test methods and standards for automotive EMC as compared to commercial testing. The automotive electrical environment is a specialized field in which the more generic EMC tests are simply not applicable.

Solutions to electromagnetic interference problems tend to get more expensive the closer the product is to the market and it is therefore important to try to predict all possible coupling paths

for the disturbances.

2.5 The electromagnetic environment in a vehicle

There are two ways for the electromagnetic fields to be coupled into the vehicle electronics. The first way is coupling into the electronic system via PCB tracks or internal wiring. Both act as antennas and convert the field into a conducted voltage or current. The second way of coupling is when the vehicle wiring harness acts as an antenna and conducts the interference into the electronic system. Since the coupling process is strongly dependent on the frequency of the interference will neither the wiring harness nor the electronic system work as efficient antennas at frequencies at or below 20 MHz. This is due to their length, which is relatively short compared to the wavelength of the interference (a good antenna has a length equal to a quarter of a wavelength). The wiring harness works as a reasonably efficient antenna between 20 and 200 MHz. The vehicle harness attenuates high frequencies above 200 MHz and is therefore no longer a good antenna.

It is not unusual, in a vehicle, for the power electronics and the load to be placed at a distance of about 1-2 m apart. The cables between them are mostly unshielded, and since always are placed near to the body sheet metal, there will always be a parasitic capacitance between the cables and the load. This parasitic capacitance creates a closed current loop for a common mode current, which flows from the power electronics, along the cables and down to ground by the parasitic capacitance. The common mode current together with the cables and the body sheet metal creates a loop antenna, which thereby radiates magnetic emissions. The common mode current through the parasitic capacitance is determined by the size of the parasitic capacitance and the voltage derivatives as in:

$$i = C_{parasitic} \cdot \frac{dV}{dt} \tag{2.1}$$

This implies that when affecting the parasitic capacitance by reducing the distance between the cable and the body sheet metal or by affecting the voltage derivatives, the common mode current can be reduced. In the automotive industry, there is no room, neither financially nor literally, for any extra components (filters, choppers, shields). There are some common noise reduction techniques that often could be used in order to deal with EMI problems. Some of the techniques are essentially free of added cost and should therefore be used whenever applicable, and the other techniques that will be discussed in Chapter 4 are techniques that should be used whenever additional noise

reduction is required.

2.6 Automotive battery

Other significant differences setting automotive EMC apart occur within the power supply. A vehicle is a self-contained system including both generator and storage (battery) and operates at low voltage DC.

When the engine of the vehicle is running the alternator supplies current for most DC-loads but the internal inductance in the alternator is too large to supply rapidly switched currents. The battery therefore supplies these currents. This configuration makes the current return path somewhat ambiguous. One additional complication is the starter motor since it, in order to ensure the function when the weather is cold, should have a current return path with a very low DC-resistance. This implies that the battery negative should be connected to the ground of the starter motor (the engine block), and the placing of the starter motor and battery may cause unfavourable loops for this conductor. The battery is not only an electrical energy storage, but it also performs a number of noise suppression tasks. It has a highly non-linear electrical characteristic, which depends on the frequency, state of charge and load current. At low frequencies the battery has a capacitive reactance that reduces the low-frequency noise components created by the ignition system when the battery is placed in parallel with the alternator. For frequencies in the range of 25 kHz to 250 kHz the capacitance of the battery is roughly constant and in the order of some tens of [nF]. At higher frequencies it is then best described by an LC-circuit, including the lead-inductance. This implies that series resonances are common for frequencies above 1 MHz, and that the battery should not be relied upon to provide a radio frequency suppression in the AM-band and above. The negative battery terminal on a vehicle is not a true ground reference; and in some tests, automobiles are treated as ungrounded (isolated) systems. There are some disadvantages with the present 12 V systems, such as:

- a point-to-point wiring are needed, which makes the wiring harness heavy and complex;
- the system voltage varies from 9 V to 16 V and destructive high voltage transients can occur;
- the system is designed to withstand a load-dump transient; i.e. a voltage spike caused due

to sudden load loss of a fully loaded alternator.

The automotive industry demands that every component (except for the alternator) should be able to withstand a reverse connection of the battery. This demand requires either semiconductor switches at the input of every system in order for it not to be exposed to a voltage of reverse polarity or that components such as RCD snubbers are not used, since they could cause a short circuit if the battery is reversed. One of the constraints, enumerated above, imposed by the conventional system design is that all the loads in the electrical system of a car must survive a transient event known as a *load dump*. A load dump occurs when the battery is disconnected during charging. This causes a sudden drop in the alternator current and a rise in the alternator voltage. The increase in voltage occurs because the decreased alternator current is accompanied by a corresponding decrease in the voltage across the series armature reactance. The time constant of the regulator is typically a fraction of a second, which leads to a delay in the order of 100 ms before the alternator voltage returns to normal. The maximum of this voltage is, for system design purposes, generally assumed to be between 40 V and 80 V, which mean that electronic systems in the car must be design to survive this transient. For practical purposes, semiconductors that are directly connected to the electrical system must be rated for voltages between 50 V and 100 V even though a load dump may never occur during the cars lifetime. This overrating is very costly, especially for power MOSFETs.

DC-DC regulators are used in modern cars to supply electronic systems from the battery voltage. These regulators have the task to stabilize the voltage to a fixed value, normally lower than the battery voltage, and filter the interferences coming from other systems through the battery cable. Indeed, in a car there are many different types of equipment all connected together with the battery.

The challenge for the regulators in automotive systems is to combine the harshest requirements, like:

- wide input voltage range from 5 to 50 V
- wide temperature range from -40°C to +125°C
- very low power consumption in standby mode and without load
- at least a lifetime of 15 years or more
- low cost CMOS technology

- low EMI emission.

The battery voltage in a car changes from 5 V during cranking to 50 V when the battery is temporarily disconnected (load dump) or one inductive load is disconnected. Low power consumption in standby mode is necessary in order to increase the lifetime of the battery when the car is stopped.

DC-DC regulators are systems that can convert a DC voltage to another DC voltage. Compared to linear regulators, DC-DC regulators can achieve better performance in terms of power dissipation, output voltage capability and current capability, but they suffer in terms of output noise, line regulation and load regulation. DC-DC regulators ideally can have an efficiency of 100% and practical designs demonstrate efficiency of about 80-90%. This performance can be achieved forcing the power MOS working as a switch and not as a resistor. Using this trick the power dissipated by the regulator is very low. This means that the efficiency goes up and normally no heatsink is needed thus reducing the system complexity. The linear regulators are very inefficient but compared to DC-DC regulators allow to obtain a better output performance: absence of any ripple and faster response to input and output variations; no electromagnetic interference (EMI) noise is generated.

In particular, designing automotive systems require paying attention in noise reject and in power dissipation. The regulator is one of the most stressed devices in terms of input noise. It is connected directly to the battery and the alternator and, for this reason, it has to withstand at the stress generated by them and by other electronic systems on a car. Furthermore automotive systems have to withstand at very wide ambient temperature range, from -40°C to 125°C.

Electromagnetic interference (EMI) has been a persistent concern in automotive system with multiple electrical subsystems for many years. It is particularly a great concern in newer models of vehicles with dramatic increase in luxury and critical electrical loads. Additionally, conversion of mechanical systems such as pneumatic, hydraulic, and mechanical actuators to electrical systems has been accelerated recently. Current critical and non-critical electrical loads on vehicles include power windows, lights, navigation, DVD systems, satellite radio, airbags, various electric motors, solenoids, relays, switches, miles of magnetic-field-producing wiring, engine management, anti-lock braking, electrical power steering, in-car entertainment, heating controls as well as on-board transmitters and mobile phones.

Parts of the increased electrical loads are performance loads such as electric valve train or electric steering system. The power consumption of these loads is variable and they require tightly regulated input voltage. Multi converter system will be utilized in newer car models, which include various power electronic converters. All of these converters generate and draw ripple current with harmonic frequencies that are in range of EMI frequencies and may interfere with other electrical loads. This disruption could be troublesome if it interferes with a critical system such as anti-lock brake system. To limit the electromagnetic interference in the automotive systems, international agencies such as Society of Automotive Engineers and International Standard Organization and vehicle manufactures established legislations to test the final products.

In all the DC/DC converters, output voltage has a high frequency ripple. Frequency of this ripple voltage is a multiple of switching frequency. In modern DC/DC converters, to decrease the size and cost of inductors and capacitors, higher switching frequencies are utilized. Typically, the frequency of the voltage ripple is more than 150KHz, which is in the range of EMI noises for automotive systems. Load at the output of DC/DC converter draws a current with the same or higher ripple frequency. This ripple is larger in high current and low output voltage converters such as the ones used in automotive systems. Additionally, output capacitor has an Equivalent Series Resistance (ESR) that contributes to the ripple voltage. Ceramic capacitors have lower ESR but are expensive for higher capacitance values. Aluminum electrolytic and tantalum capacitors are relatively inexpensive for higher capacitance values but their ESR is much higher.

The automobile is changing and so, too, are the electronics that make them run. The most radical example is the plug-in electric vehicle (PEV) where a 300-400V Lithium-Ion (Li-Ion) battery replaces the gas tank, and a three-phase propulsion motor replaces the combustion engine. Sophisticated battery pack monitoring, regenerative braking systems, and complex transmission control attempt to optimize battery utilization and life, and extend range between charge cycles. A modern day car, electric or otherwise, has dozens of electronic modules to facilitate performance, safety, convenience and security. It is not uncommon to find mid-range cars with advanced global positioning systems (GPS), integrated DVD players, and high-performance audio systems.

With these advancements comes the need for greater processing speed. As such, today's automobiles incorporate high-performance microprocessors and DSPs requiring core voltages down to 1V, and currents upwards of 5A. Generating these voltages and currents from a car battery

that can vary from 6V to 40V is fraught with challenges, not the least of which is satisfying strict standards for electromagnetic compatibility. The linear regulator, once the primary method for converting the car battery to a regulated source voltage, has run out of steam. Or more accurately, it generates too much steam as output voltages drop and load currents increase. Instead, the switching regulator is seeing increased usage, and with a proliferation of switching regulators, comes an increased concern of electromagnetic interference disturbing radios and safety critical systems.

2.7 EMI in Switched Mode Power Supplies (SMPS)

Switched Mode Power Supplies are usually a part of a complex electronic system. The system operates with electric signals with much lower amplitude and energy compared to those on an SMPS. It means that usually the SMPS is the strongest electrical noise generator in the whole system.

Especially the power switches with their high $\frac{dv}{dt}$ and $\frac{dv}{dt}$ switching slopes are the sources of EMI. The source of differential mode interferences is the current switched by a MOSFET or a diode. High rates of $\frac{dv}{dt}$ and parasitic capacitors to the ground are the reasons for common mode interferences.

Most of the carriers are not a pure sine wave but a set of harmonics, as example, in SMPS, a PWM signal is to be found. The question now is how to deal with these generic waveforms consisting of infinity of harmonics.

Consider the periodic square waveform shown in Figure 2.4, with period T, frequency $f_c = \frac{1}{T}$ or $\left(\omega_c = \frac{2\pi}{T}\right)$, amplitude A and pulse duration of τ. The complete spectral content is to be calculated analytically and displayed graphically onwards.

The complex-exponential expansion coefficients are shown below:

$$c_n = \frac{1}{T}\int_0^T x(t)\cdot e^{-jn\omega_c t}dt = \frac{1}{T}\left[\int_0^\tau A\cdot e^{-jn\omega_c t}dt + \int_\tau^T 0\cdot e^{-jn\omega_c t}dt\right] = \frac{A}{jn\omega_c T}\cdot(1-e^{-jn\omega_c \tau}) \quad (2.2)$$

where n is the harmonic order where "0" represent the DC component. The same coefficients putted into a sine or cosine form:

$$c_n = \frac{A}{jn\omega_c T}\cdot e^{-jn\omega_c \frac{\tau}{2}}\cdot 2j\sin n\omega_c\frac{\tau}{2} = \frac{A\tau}{T}\cdot e^{-jn\omega_c \frac{\tau}{2}}\cdot\frac{\sin n\omega_c\frac{\tau}{2}}{n\omega_c\frac{\tau}{2}} \quad (2.3)$$

From the result above, the following two expressions corresponding to the module and phase of the *n-harmonic* can be derived:

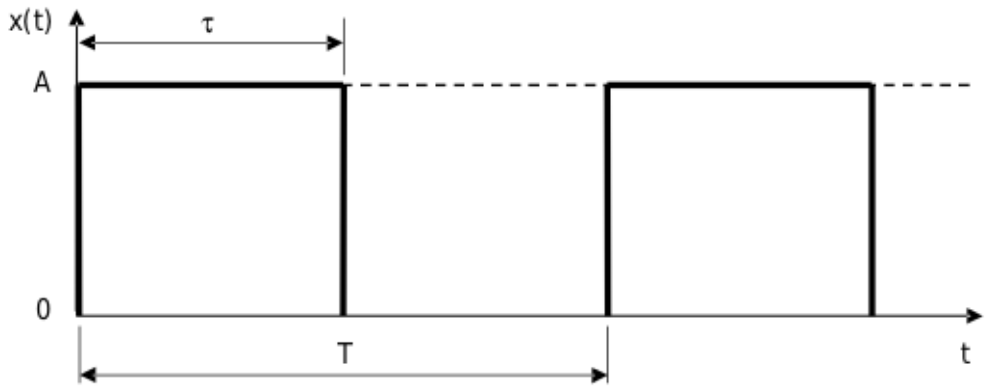


Figure 2.4: A periodic, square waveform

$$|c_n| = \frac{A\tau}{T} \cdot \left| \frac{\sin n\omega_c \frac{\tau}{2}}{n\omega_c \frac{\tau}{2}} \right| = 2 \cdot \frac{A \cdot \tau}{T} \cdot \left| \frac{\sin n\pi f_c \tau}{n\pi f_c \tau} \right| \tag{2.4}$$

$$\angle c_n = \pm n\omega_c \frac{\tau}{2} \tag{2.5}$$

The $\pm$ sign of the angle comes about because the $\sin n\omega_c \frac{\tau}{2}$ term may be positive or negative (an angle of 180°). This is added to the angle of $e^{-jn\omega_c \frac{\tau}{2}}$.

A usual convention is displaying both positive and negative frequency sinusoids for each frequency and halving the amplitude accordingly, as in Figure 2.5(a). A more intuitive convention is related to represent only positive frequency sinusoids, which is achieved by doubling the amplitude of each individual component, as shown in Figure 2.5(c).

Periodical rectangle functions in time domain generate a discrete line spectrum decreasing with 20 dB per decade in the frequency domain. Real waveforms of power switch cycles with turn on (τ_r) and turn off times (τ_f) are trapezoidal.

Instead of using a "perfect square" waveform, which have a significant spectral content at high frequencies, we started to propose finite rising and falling times for the signal flanks in order to obtain a reduction of high-frequency harmonics in the total spectral content of the signal. Figure 2.7 show a trapezoidal waveforms, representing the evolution of the classical square signals just giving values higher than zero for rising τ_R and falling times τ_F. These two values are defined as the time required for the signal to transition from 10% to 90% of the amplitude, and viceversa. The

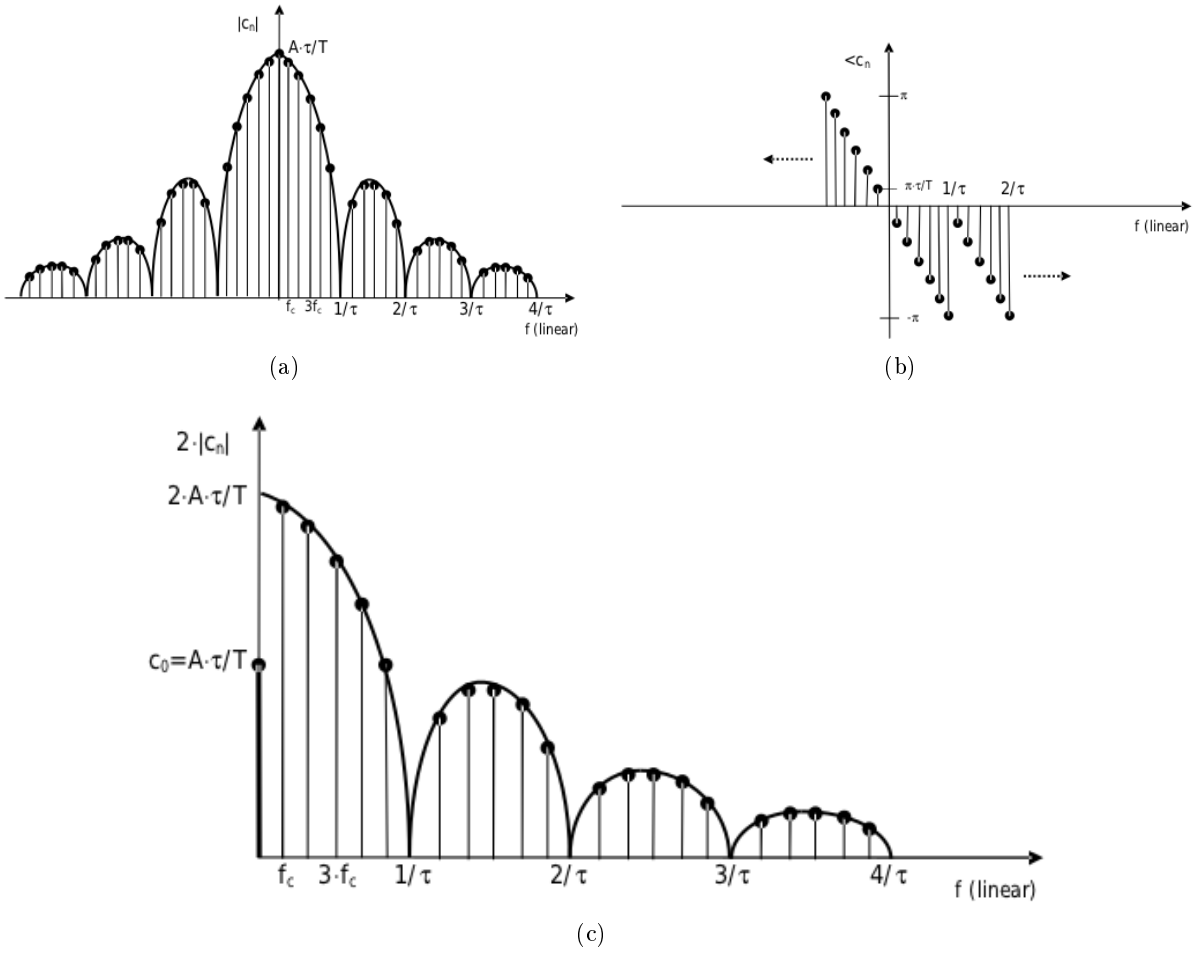


Figure 2.5: Frequency-domain representation of a square wave: (a) the two-sided magnitude spectrum; (b) the phase spectrum; (c) the one-sided magnitude spectrum

spectral contents of both square and trapezoidal waveforms are shown in Figure 2.6 and in Figure 2.8, respectively. A Fourier analysis demonstrates that the spectral content of square waveforms at higher harmonic order is greater than for trapezoidal signals.

From Equation 2.4, we can affirm that the amplitudes of the spectral components lie on an envelope as expressed below:

$$envelope = |c_1| = 2 \cdot \frac{A \cdot \tau}{T} \cdot \left| \frac{\sin \pi f_c \tau}{\pi f_c \tau} \right| \tag{2.6}$$

Expression 2.6 goes to zero when $f_c \cdot \tau = m$ with $m \in \aleph^+$. Moreover, expression 2.6 can be easily represented taking into account that:

$$\left|\frac{\sin x}{x}\right| \leq \begin{cases} 1 & \text{for } x \ll 1 \\ |x|^{-1} & \text{for } x \gg 1 \end{cases} \tag{2.7}$$

This can be drawn in a logarithmic plot (Figure 2.6) as two straight lines, the first one, 0 dB/decade corresponding to small values of x and the second one, representing an asymptote decreasing linearly with x, that is, -20 dB/decade. A similar development applied to the trapezoidal waveform results in the spectral content envelope shown in Figure 2.8.

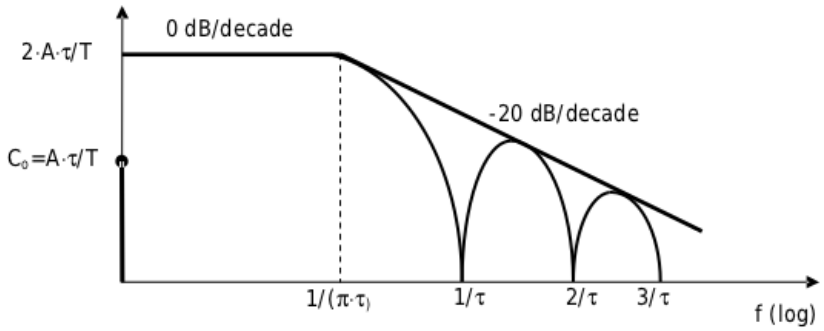


Figure 2.6: Spectral content of a periodic, square signal and the corresponding bounds

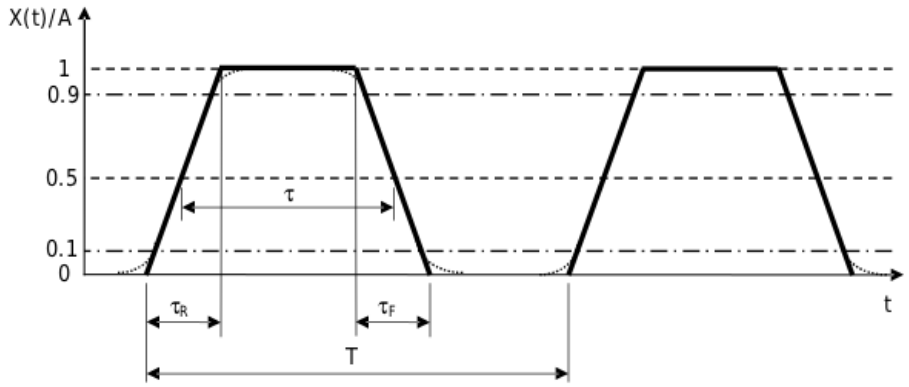


Figure 2.7: A periodic trapezoidal waveform

When viewed in the frequency domain, a trapezoidal waveform with equal rise and fall times is composed of a set of discrete harmonic signals that exist at integer multiples of the periodic signal's fundamental frequency. Notice that the energy in each harmonic falls off at $20dB/dec$ after the first break point at $\frac{1}{p \cdot t}$, where t is the on-time and at $40dB/dec$ after the second located at

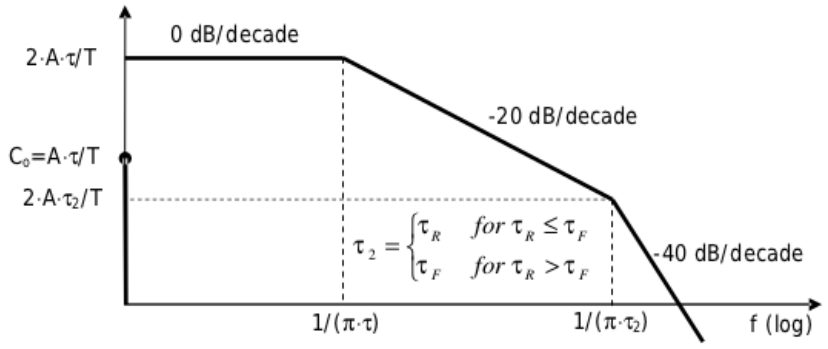


Figure 2.8: Bounds of the spectral content of a periodic, trapezoidal signal

$\frac{1}{p \cdot t_r}$. Consequently, limiting the slew-rate of the switching waveforms can have a profound impact on reducing emissions.

From these spectral bounds it now becomes clear that the high-frequency content of a trapezoidal pulse train is primarily due to the rise/falltime of the pulse. Pulses having small rise/falltimes will have larger high-frequency spectral content than those having larger rise/falltimes. Thus, in order to reduce the high-frequency spectrum and, consequently, the emissions of a product, the rise/falltimes of the clock, data pulses or switching waveform should be increased as much as possible. This kind of signals makes part of a different concept of EMI suppression that consists of limiting the spectral content in the signal itself. When possible, just waveforms with a lower spectral content should be used, this way making easier, simpler and cheaper the use of filters and other suppression means.

Another important consideration is that if the duty cycle is exactly 50 percent, all the energy of the complex trapezoidal switching waveforms is in the odd harmonics (1, 3, 5, 7). Thus, operating at 50 percent duty cycle is typically a worst case condition. At duty cycles above or below 50%, a natural EMI spreading occurs as even harmonics are introduced.

One of the more challenging areas for automobile EMI compliance is associated with the AM band. This band starts at 500 kHz and continues to 2 MHz, pretty much the sweet spot for switching regulators. Since the highest energy component of a trapezoidal waveform is the fundamental (assuming no circuit board resonances) operating below or above the AM band is desirable.

Chapter 3

State of art on conducted EMI reduction techniques

One of the principle causes of EMI in an automobile is coincident with a switching regulator imposing AC currents on the supply harness. These changing currents express themselves as harmonically rich waveforms that radiate and conduct emissions. This brief focuses on the theory and mitigation techniques of the conducted EMI, specifically as generated by a step-down converter, so some mitigation techniques for radiated EMI, like shielding, aren't discussed.

3.1 Overview

Several techniques to mitigate conducted electromagnetic interference (EMI) in switch-mode power supplies (SMPS) have been reported in literature. To keep the scope the of the chapter limited and focused, the main aim of this survey is mitigation of conducted EMI in DC-DC power converters, the chapter does not cover AC-DC converters and DC-AC inverters. The mitigation approaches are classified into two major groups, which are as follows:

(1) reduction of the noise after generation;

(2) reduction of the noise at the generation stage itself.

These are further subdivided into different types of EMI mitigation techniques, and then, detailed reviews on each technique are presented.

Switched Mode Power Supplies (SMPS) generate high frequency electromagnetic interference (EMI) noise due to the fast switching currents and voltages in them. The generated noise currents, called conducted EMI noise, travel along the input power lines and may, in turn, cause interference with other electronic systems, including the SMPS's own auxiliary circuits. Typically, an SMPS

unit sold in a region has to meet the electromagnetic compatibility (EMC) standards imposed by the regulating body of that region.

Minimizing conducted EMI noise to meet the standards often involves trial and error and is often considered an "art". Despite this commonly prevalent view, there are systematic EMI mitigation techniques and design procedures developed over the years. The aim of this chapter is to classify these techniques into different categories and present a detailed survey.

One way to reduce the level of conducted noise is by ensuring that less noise is generated by the noise source itself. On the other hand, the noise can be mitigated along the noise propagation path by filtering and other means. The suggested classification of EMI techniques based on these broad groups is shown in Figure 3.1.

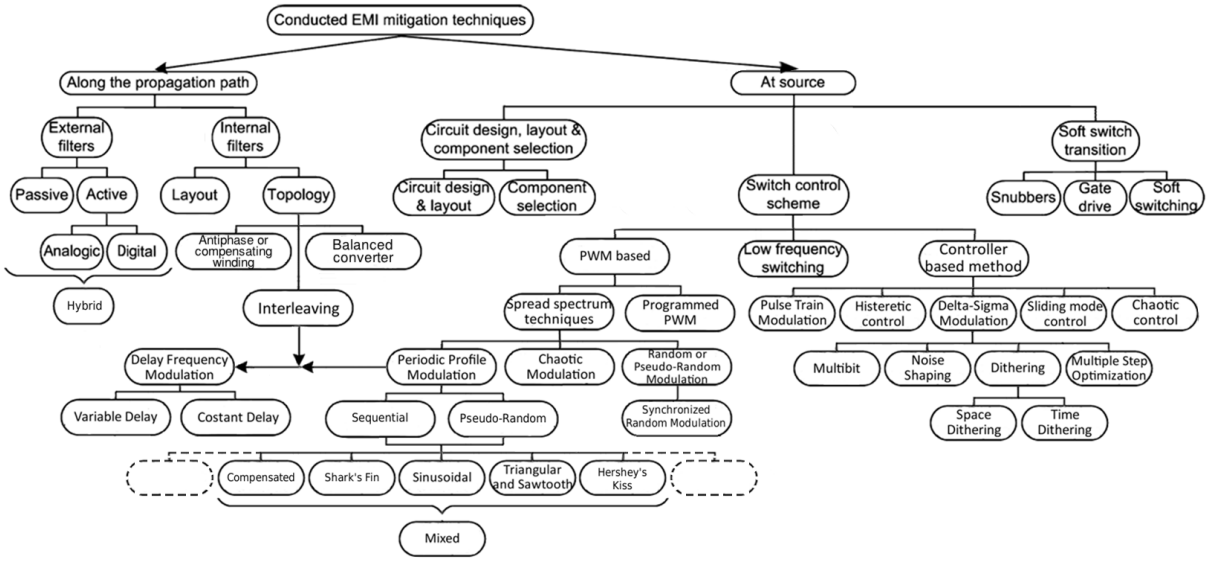


Figure 3.1: Conducted EMI reduction techniques

Filters can be used to modify the characteristics of the noise propagation path so as to reduce the noise at the receiver end. This filter can be a separate unit kept on the front end or it can be integrated into the power converter itself. This leads to a further subdivision into external EMI filters and internal filters.

The external EMI filters can be further divided into passive and active filter types. In the case of internal filters, the noise currents are internally circulated within the converter itself by changes in layout or topology. As mentioned earlier, EMI noise can also be mitigated at the source itself.

This can be achieved by:

(1) selecting/designing appropriate components and/or better physical layout of the circuit;

(2) better switch-control schemes;

(3) soft-switch transition techniques.

The divisions among the subgroups are not rigid and some techniques may be considered to belong to more than one subgroup. Also, it is possible to combine more than one approach to come up with a "hybrid" mitigation approach. For example, the active and passive filter techniques may be combined to develop a hybrid filter technique.

3.2 Condected EMI mitigation along the propagation path level

3.2.1 External EMI Filters

Both passive and active EMI filters (AEFs) have been used along the input power supply lines to mitigate the noise.

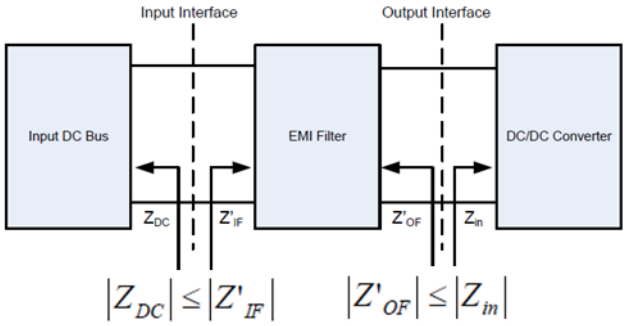


Figure 3.2: External filter.

1) Passive EMI Filters: This is the most common approach for EMI noise mitigation used currently. As the name suggests, these filters use only passive components. The design of such filters for use in power electronics is particularly challenging, since the filters are terminated with varying noise source (SMPS) and load (power line) impedances. Typically, an EMI filter acts as a low-pass filter. It has a negligible effect at the power frequency, while it offers large attenuation to the noise currents in the conducted EMI frequency range.

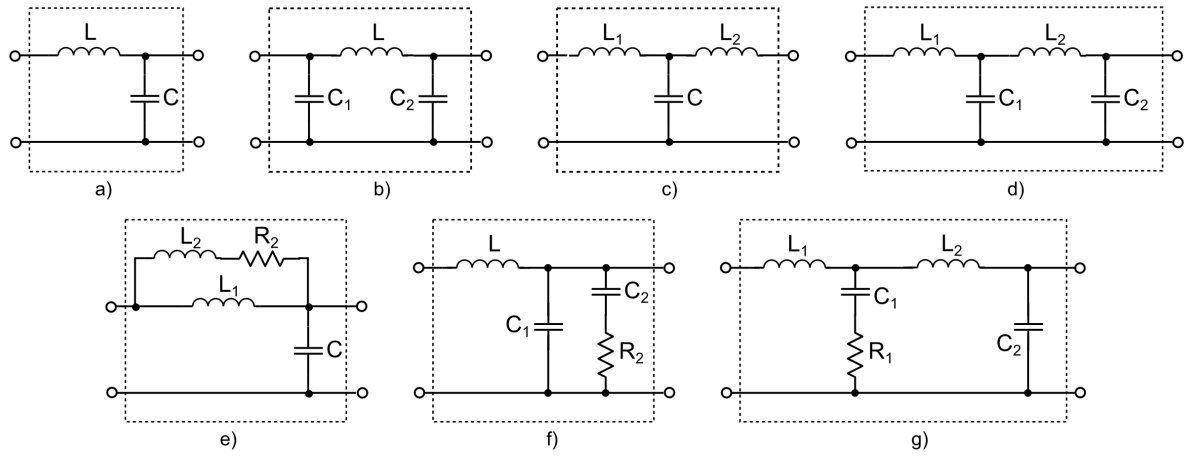


Figure 3.3: Passive external filter tipologies

With a high-order Cauer-Chebyshev filter, it is possible to obtain high attenuation, which is often required in the low-frequency region of the conducted EMI. The performances of the passive filters at high frequency are usually dominated by component parasitics. Neugebauer and Perreault [42] introduced a technique to improve the high frequency performance by cancelling out the effects of the parasitic capacitances of the filter inductors. The technique uses an additional inductor or a small RF transformer and a capacitor.

The input filter, however, if improperly designed, can actually amplify noise and destabilize the control loop. So understanding the concepts of input filter design are important in optimizing filter response and cost.

Whether you are designing a buck or boost supply, the differential mode filter or a bi-directional pi-filter can be your best friend by keeping EMI noise from getting onto the line and radiating, and/or conducting noise. Note that parasitic elements associated with the filter components, including inter-winding terminal capacitance and capacitor ESR, can significantly affect attenuation of harmonic content and should be considered carefully.

A real capacitor includes both an inductor and resistor in the form of leads, traces and even ground planes in series with it. The capacitor behaves ideally up to frequencies of some MHz. Above the resonant frequency the behavior is defined however exclusively by the inductance of the leads. The resonant frequency of the capacitors determines the maximum effective attenuated frequency.

The filters discussed earlier are essentially nondissipative and their performances are depen-

dent on the behaviors of source and load impedances, which, however, can vary over a wide range. Though the load impedance, which in this case is the impedance of ac lines, is stabilized using LISN during conducted EMI measurements, in actual application, it can vary in the absence of the LISN. Discrete passive EMI filters are normally bulky and their performance degrades at higher frequencies due to component parasitics. Integrated EMI filters, using planar electromagnetic integration technology, with distributed inductance and capacitance, have been proposed with the aim of realizing smaller size, better performance, and lower cost.

2) Active EMI Filters: AEFs use active electronic circuits to cancel or suppress the noise and are possible alternatives to bulky passive EMI filters. Based on the method used, an AEF can be of feedforward or feedback type, or a combination of both types. In a feedforward AEF, the noise is reduced by injecting an equal amount of noise of opposite polarity. A feedback AEF, on the other hand, uses a high-gain feedback-control loop to reduce the noise level.

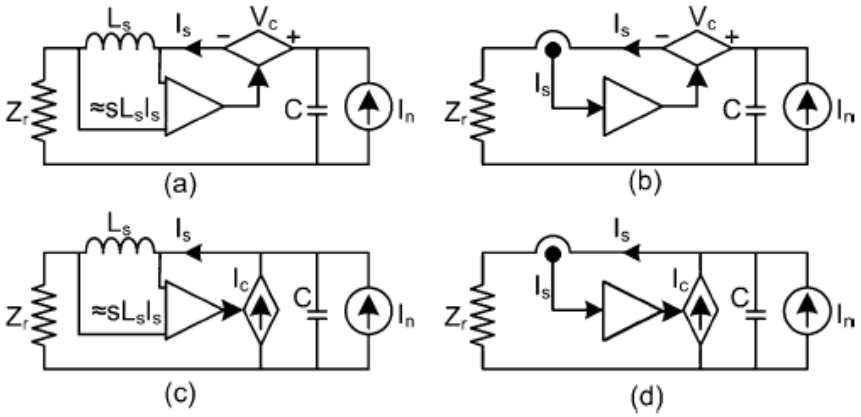


Figure 3.4: Feedback Active External Filter topologies

The AEFs can be configured based on how the noise is sensed and compensated. Figure 3.4 shows four possible topologies for feedback AEF. Either the current in the inductor or the voltage across it can be sensed and the compensation can be through injection of either a series voltage or a shunt current [43], [44]. Series-voltage compensation (see Figure 3.4) increases the effective impedance of the series path, while the shunt-current compensation decreases the effective impedance of the shunt path.

The rejection of components related to power-line frequency and its harmonics, feedback-loop

stability, and realization of high-feedback gain over a large noise frequency bandwidth are the main issues related to AEF design for utility applications [45]. The analysis has shown that there must be sufficiently large difference between the converter's switching frequency and power frequency for good rejection of power frequency and its harmonics, large attenuation of switching noise, and good stability margins of AEF feedback loop. The tradeoff between the stability and achievable noise attenuation and bandwidth is brought out. The stability is largely influenced by the parasitics of the components that are involved in the feedback loop.

Combination of both the feedback and feedforward AEF techniques has been shown a good overall noise reduction, in particular AEFs help to reduce the size of the passive components that are required to achieve desired noise attenuation. Though, in principle, an AEF may help partly to solve the EMI problem, the additional complexity and also issues regarding reliability and large signal behavior will need to be addressed, before it can find wide applications in commercial products.

3) Hybrid EMI Filters: Often AEFs are combined with passive EMI filters to form hybrid EMI filters [46]. The passive filter part helps to bring down the noise to the level that can be handled by the AEFs. A converter with a high switching frequency (say, 1 MHz) requires a large attenuation at the fundamental switching frequency itself. Multistage Hybrid EMI filters are required in such cases to meet the standards. In such an arrangement, the second stage has much smaller ripple currents and ripple voltages than the first, which may allow the second-stage passive filter to be replaced by an AEF to reduce the overall filter volume.

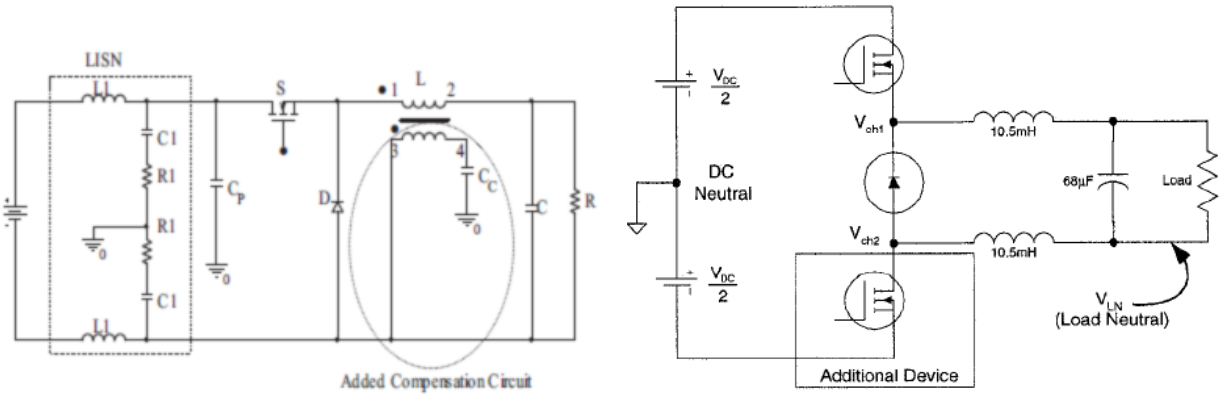
3.2.2 Internal EMI Filters

Internal EMI filter techniques provide noise-current circulation paths within the converter itself. This can be achieved by changing the board layout or topology of the power converter circuit.

1) Layout: The noise currents can be circulated internally by proper design of the circuit layout and can be limited to be within the power converter by ensuring that the EMI generated by the MOSFET switching is absorbed by other parasitic capacitors in the circuit acting as Y-capacitors. A proper design of PCB helps to adjust the values of the filter's Y-capacitors. The relevant circuit nodes have to be identified and the footprints sized appropriately to ensure that the

resulting parasitic capacitors have the requisite values.

2) Topology: The converter topologies that circulate the noise currents internally are discussed in this section. Interleaved converters with phase-displaced switching signals can be used to reduce the EMI noise. The downside of interleaving is the additional cost due to the use of several smaller converters and increased control circuitry.



(a) (b)

Figure 3.5: Feedback Active External Filter topologies

Another possibility is to generate a counterbalancing current to nullify the common mode noise current. This can be achieved by using an anti-phase transformer winding, as shown in Figure 3.5(a), to generate an 180° out of phase voltage waveform through a compensating capacitor that replicates the dv/dt seen across the original parasitic capacitor. Ideally, this results in zero CM current due to the MOSFET's parasitic capacitance. The advantage of this filtering technique is that the filter uses the power converter's magnetic element. The winding carrying the CM cancellation current is rated for noise current only, and thus, the inductor size will not be altered much. The performance of the scheme is affected by the parasitic capacitance between the two windings and also by the leakage inductance of the coupled inductor. *Current ripple steering* technique has been reported in [47] to reduce DM noise. The scheme effectively adds an input-side LC filter. The advantage of the scheme is that the filter uses the magnetics of the converter.

In [48] *balanced switching converters* have been proposed in place of conventional unbalanced circuit topologies to reduce the CM noise. Figure 3.5(b) shows such a modification for the buck converter with the inductor divided equally between the lines. With balanced inductors, the voltages at

both drain and source change complementarily, thus confining the CM current within the converter circuit. Attenuations in the range of $10 - 20 dB\nu V$ in the CM noise have been reported using balanced switching technique. Often this balanced switching feature comes with a more complex gate driver circuitry and an extra power device. In summary, the internal circulation techniques aim to eliminate the external filter or at least reduce its size at the expense of an increase in circuit/control complexity.

3.3 Conducted EMI mitigation at its source

This approach of reducing the EMI noise at the noise source itself has the advantage of preventing interference with converter's own auxiliary circuits. The noise generation can be reduced by proper design of circuit layout and selection of circuit components, better switch-control scheme, and soft-switch transition techniques.

3.3.1 Circuit Design, Layout, and Component Selection

A close attention has to be given to physical layout and component selection during the initial SMPS design stage to minimize the EMI generation.

1) Circuit Design and Layout: The CM noise due to the heat-sink can be reduced by connecting the heat-sink to a constant potential in the circuit. This type of connection may give rise to safety issues, as the heat-sink is not at ground potential. This issue can be resolved by sandwiching a shield between two layers of heat-sink insulators. The shield is tied to a fixed potential in the circuit and the heat-sink is grounded. While this approach can mitigate the CM noise, the effectiveness of the heat-sink will be somewhat diminished due to the additional layers of insulation between the device and the heat-sink. In some cases, rearranging the circuit can eliminate the dv/dt across the parasitic heat-sink capacitor. Moving the output filter inductor to the negative rail makes dv/dt across the cathode of the diode zero. Similarly, relocating MOSFET and putting the drain of MOSFET at constant potential can be helpful. It has been suggested in [49] that the heat sink can be grounded through a resistor, which will reduce the charging/discharging current of the parasitic capacitance leading to reduction in CM noise.

Reduction of the radiated noise from a converter helps to reduce the radiation coupling into

the conductive elements of the circuit. Rossetto et al. [50] evaluated different circuit designs and layouts and their effects on conducted EMI. The critical tracks on the PCB are twisted and inductors are designed with toroidal cores wound in a special way to keep the radiated noise as low as possible.

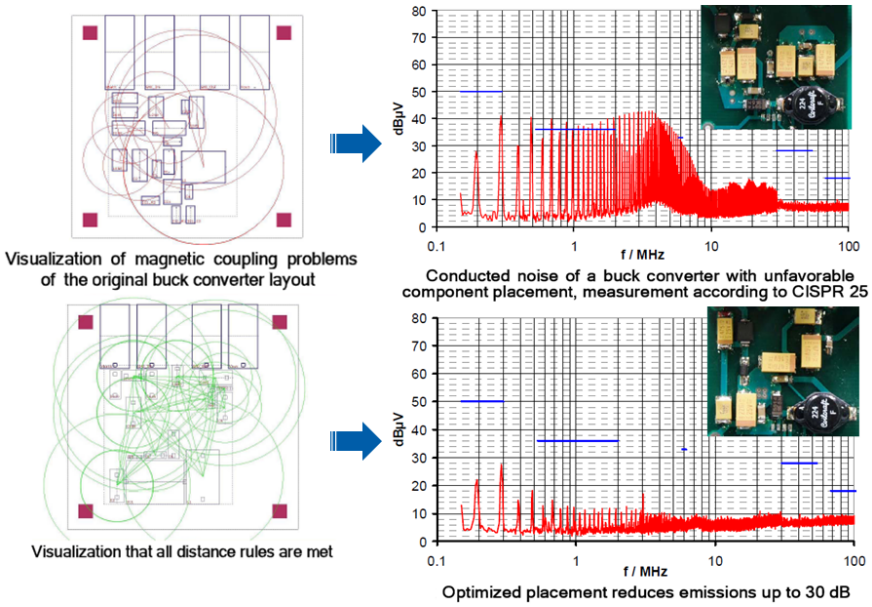


Figure 3.6: Effect of two different layouts of the same DC-DC converter on conducted EMI

Several authors [51] have discussed the circuit design and layout techniques to address the issues related to EMI generation. The most easily controllable and necessary aspect of designing an EMI-compliant switching regulator are circuit trace routing and component placement, in order to minime emissions at the source. The PCB tracks should be as short and wide as possible, in order to make the effective antenna smaller on the one hand and, on the other hand, to reduce the voltage drop. The wider the track the lower is the length-related resistance and inductance and thus also the static and dynamic voltage drop. This is particularly important for the ground track, since it should have as constant as possible potential for the entire system as point of reference.

Fundamental to the proper layout of a power supply is minimizing loop area of high-current caring conductors. In doing this one minimize inductance that can act as an antenna source and radiate energy. One aspect of this is effectively placing the component and selecting the decoupling capacitor. The switched current with its steep slopes generates a magnetic field over the power loops where it flows. The loop inside and surrounding will be penetrated by this magnetic field.

These loops have to cover as small as possible surface, in order to make the surface penetrated by the magnetic field small. If this is not possible, a low-inductance capacitor of some μF, which is connected parallel to the bulk and close to the switch, may help.

The minimization of the parasitic inductances helps to reduce the voltage ringing when the power devices switch and this in turn reduces the generation of high frequency EMI noise. Component layout in PCB also plays a role in operation of the converter and its EMI noise. Moreover, the sensitive circuits, such as control circuits, have to be placed far apart from the noise source such as power switches. Such a practice of partitioning the noise generating modules and noise-susceptive modules prevents the malfunctioning of the converter. The noise voltage generated across the common ground impedance by one circuit may cause interference in another circuit sharing the same common ground connection. It has been suggested to use single-point grounding as far as possible to avoid interaction among the circuit modules. A properly designed PCB can help to achieve the desired noise level with fewer additional filter components.

2) Circuit Components Selection: The parasitic capacitors between the switching devices and the heat sinks are the major contributors of the CM noise. Different heat sink insulators have been compared. Silicon rubber insulators, which are commonly used, have a dielectric constant 6 times that of aluminum oxide insulators. Experimentally, an improvement of $\approx 10\,dB \cdot \nu V$ up to 20 MHz in conducted EMI noise has been achieved when aluminum oxide insulator was used in place of silicon rubber.

At high frequencies, it is noted that a typical inductor has several impedance valleys, which result in much reduced noise attenuation at these frequencies. A redesigned inductor with a lossy core has damped these impedance valleys. This has resulted in lower DM noise. Use of thicker insulation in the inductor's winding help to increase the self-resonant frequency of the inductor, but the resulting increase in the physical size has to be looked into. A shielded inductor helps to reduce stray leakage fields that can radiate and couple into mutual inductances and high-impedance circuits (like the input error amplifier of the PWM controller). A further method, is the parallel connection of capacitors, in order to reduce their effective parasitic series resistance ESR.

Device characteristics also influence the EMI noise spectrum. Devices with larger packaging size will result in larger heat-sink parasitic capacitance. Since diode reverse recovery current has a high frequency current content, using a diode with soft or low-reverse recovery characteristics can

help in reducing conducted noise and minimize high-current spikes.

3.3.2 Soft-Switch Transition Techniques

A way to reduce EMI generation is to slowdown the switching transitions and thereby reduce *di/dt*'s and *dv/dt*'s of the switching device. Such an approach would reduce only the high-frequency spectrum and is unlikely to bring down the envelope of the low frequency conducted EMI. However, with the slowed down switching transitions, the radiated EMI would be reduced, thus resulting in less radiation coupling. Snubbers, gate-drive modifications, and soft-switching techniques all fall under this category.

1) Snubbers: Snubber circuits are placed across switching power devices to soften the switch transitions and to also aid in damping the high frequency waveform oscillations during switching. Thus, snubbers may be viewed as low pass filters reducing the high frequency components, which occur during switching. Use of snubbers will reduce EMI with a slight increase in overall power loss. *Magnetic snubbers* (amorphous core saturable reactor), using linear and saturable inductors, have been reported to have smaller power loss than the normal *dissipative snubbers* (exhibits a very large inductance for an initial *di/dt*, but quickly saturates).

2) Gate-Drive Modification: The well-known way to control the switching speed and therefore the EMI behavior is a variation of the external gate resistance. If the resistance will be increased, the time constant determined by this resistance and the capacitance of the MOSFET will be increased as well. The switching transient will be slowed down and thereby the electrical noise becomes lower. However, this approach, would tend to increase the switching losses.

A method has been suggested to reduce the EMI noise by adjusting the drain voltage and current slopes of the switch independently [52]. With this method, the current slope can be set to the desired low value. In order to keep the switching losses unchanged, the switch voltage slope value has been correspondingly increased. These method has shown improvement in high-frequency region and a small improvement in low-frequency region. The reduction of current slopes may help in reducing high-frequency DM currents drawn by converters, however, increasing the switch voltage slope may result in increase in the high-frequency part of the CM noise. Also, the resulting gate circuit is more complex than normal gate drives.

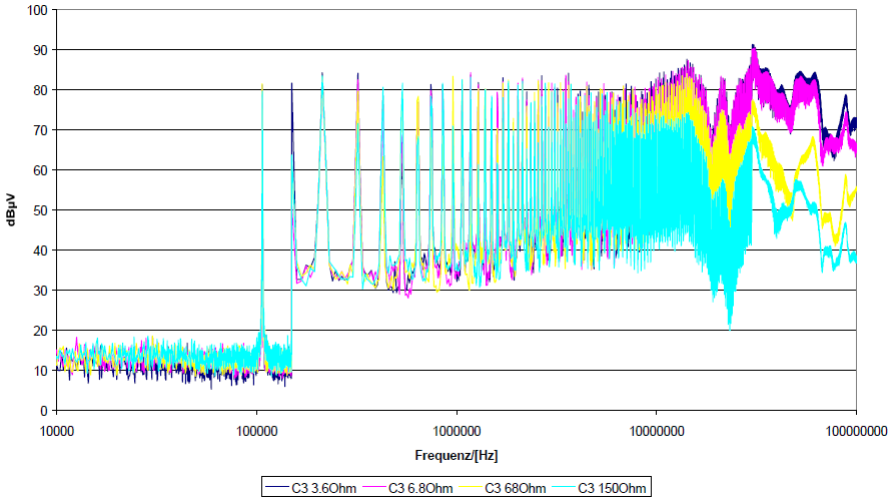


Figure 3.7: Influence of the external gate resistance (discontinuous current mode, Id=6A, measured)

3) Soft-Switching Techniques: Another method of reducing di/dt and dv/dt in order to reduce EMI generation is to use soft-switching techniques. Shaping the waveform coincides somewhat with the strategy mentioned in [53] where a Zero Voltage Transition (ZVT) technique is investigated which in theory promises reduced emissions. As the diode in a ZVT converter is softly turned on and off, both fast voltage transitions across the main switch and fast current change in the diode are avoided and the high frequency harmonics is reduced. In [54] a hard switched converter and a ZVT converter have been compared with the result that the ZVT technique only marginally reduce the emissions. In certain cases, a soft-switched converter may not achieve better conducted EMI noise performance than a hard-switched converter of similar design. This has been attributed to the significant EMI noise generated by the auxiliary switch of the ZVT circuit, which is hard-switched.

3.3.3 Switch-Control Scheme

Though the primary function of switch control is to regulate the power flow, the control can also be changed to influence the noise generated by the power converter.

1) Low-Frequency Switching: The selection of switching frequency plays an important role in minimizing the EMI filter requirements with a reduced switching frequency resulting in lower EMI noise at the expense of large-sized passive components. A common compromise adopted is to

set the switch frequency to be around 70 kHz, so that the first and second harmonic components of the switching current would be below the lower frequency limit (150 kHz) of CISPR conducted EMI standards. This will reduce the size of the passive EMI filter required. However, we may expect the passive elements used in the converter to be larger as a result of the very low switching frequency.

2) Controller based techniques: SMPS are known to be capable of chaotic behavior. Recently chaotic operation of the power converters has been exploited to spread its EMI emission. A design of a power converter PWM control IC based on chaos has been reported in [56]. Other frequency-modulation techniques, Delta-Sigma modulation [**?**], multistep optimal converter (MSOC) [57], frequency hopping technique [58], and bifrequency technique [59], have also been suggested to reduce the conducted EMI. Experimental results with these techniques show typically a 5-10 dBνV reduction in the conducted EMI.

3) PWM based techniques: A technique using preprogrammed turn-ON and turn-OFF times stored in a memory for the PWM waveform to control DC-DC converter has been proposed in [60]. The switching sequence is programmed without disturbing its average duty cycle. The programming of the PWM switching sequence is carried out such that the resulting harmonic spectra fit the desired spectral envelope.

3.4 Spread Spectrum Modulation techniques

3.4.1 Discussion on previous EMI mitigation techniques

An external front-end passive filter is the most-established method to meet the EMI standards and is extensively used at present. The main drawback of a passive filter is its large volume. The layout of the passive filter has to be done carefully to minimize the effect of radiation coupling and often, requires shielding.

AEF appears to be a promising alternative to the passive approach to achieve large attenuation in a small volume. Achieving stability of the active noise compensation circuit can become difficult due to the influence of component parasitics. The capability of the AEFs to achieve sufficient attenuation over a large frequency range is yet to be established. Furthermore, the reliability of active amplifier circuit, and the requirement of clean bias voltages for the amplifier are another

issues of concern.

Conducted EMI mitigation techniques based on layout modifications, component selections and design, use of snubbers, and through gate drive modifications can all result in improvement in the conducted EMI spectrum. However, these techniques will normally have to be combined with others, such as external active or passive filtering, to reduce the SMPS noise below that specified by standards. Also, among these techniques, snubbers, and gate-drive modification are likely to help in reducing noise in the higher frequency range of the EMI spectrum and at the expense of increased power loss.

Lowering the switching frequency will help to reduce the EMI filtering requirements. However, this will increase the size of the passive components in the converter. Other methods reviewed have considered different topologies for reducing the noise generated within the power converter itself. Converters using antiphase windings or balanced switching are promising topologies for internally filtering the generated CM noise. Likewise, interleaved converters can substantially reduce generated DM noise. Topologies using soft switching techniques, on the other hand, have lower di/dt's and dv/dt's, and thus, can result in less EMI noise generation within the converter itself. Such topological approaches to EMI mitigation can tend to increase the complexity of the power converter.

EMI mitigation is a complex issue and different mitigation techniques will normally have to be used simultaneously to reduce the noise below the level required. In general, the reduction of EMI noise at its source is more desirable than reduction along the conduction path, as the former would tend to reduce radiated noise coupling also. Even with the adoption of different EMI mitigation techniques, an external front-end EMI filter will often be required to meet the standards. However, such techniques help to reduce the size of the additional external filter.

Predicting the EMI noise through simulation and analysis will help in the design stage by alerting the designer to the expected amount of noise generation and also suggesting places for improvements.

3.4.2 Spreading the spectrum

Power supplies generally fail EMC tests, not because of excessive total spectral energy, but because of concentrated energy in a narrow frequency band. Fundamentally, the spread spectrum techniques as applied to power converters involves varying the switching frequency from cycle to

cycle, changing the frequency spectrum from a train of large spikes concentrated at the switching frequency and its harmonics to a smoother, more continuous spectrum. Depending on the modulation waveform and the test setup parameters (e.g., RBW of the spectrum analyzer) employed, reduction of the fundamental and harmonics can exceed 15 dB. However, the standards used for EMC measurements and the operation of the EMC equipment must be carefully understood when an effective noise-reduction technique is being qualified. In a spread-spectrummodulated configuration, the fundamental and each harmonic is swept by the modulation signal.

EMI reduction by frequency modulation of a power supply's switching frequency can be explored using classical frequency-modulation (FM) theory. Frequency modulation theoretically will produce an infinite number of sidebands; however, the magnitudes of the spectral components of the higher-order sidebands are typically negligible. Given a periodic signal, the emission power will center at the switching frequency and harmonics associated with the waveform duty cycle. At exactly 50% duty cycle, a square wave's energy is concentrated in the odd harmonics, resulting in a worst-case EMI condition with maximum peak amplitude; but this is generally not the case in a switching power supply. In fact, any deviation from 50% will result in a spreading effect by increasing energy in the even harmonics. Modulating the switching frequency within a limited range creates sidebands (spaced by the modulating frequency) and decreases the spectral density, further lowering the harmonic peaks.

3.4.3 Periodic profile modulation

After modulation, a single harmonic changes into an amount of side-band harmonics with amplitudes smaller than the non-modulated harmonic and separated by a frequency f_m (modulating frequency). Amplitudes of side-band harmonics resulting from modulation show a different aspect or outline depending on the modulation profile. In implementing a frequency modulation technique, it must be ensured that the resulting side bands do not fall into the audible range. Also, overlapping of the side bands of different switching harmonics should be avoided to achieve appreciable spread in spectrum. Such variable switching-frequency techniques are attractive, since they can be realized easily without changes in the topology or power components and with little additional cost, particularly when digital control is used. Many PWM control ICs now have frequency-modulation options.

Figure 3.8 and Figure 3.9 shows the effect of frequency modulation of a periodic waveform in the frequency domain, where f_c is the switching frequency, f_m is the modulating frequency, and Δf_c is the depth of the frequency change. The modulation-index, m_f, is defined as $\Delta f_c / f_m$. The spreading, or extent of distribution, and the resulting fundamental and sideband amplitudes are a function of the modulation index. The larger the m_f, the more distributed the spectrum becomes; however, there are practical limits to the minimum and maximum spreading in a switching-regulator application. On the low end, the modulation must be greater than the resolution bandwidth specified in the EMC standard or no improvement will be realized. In addition, the selection of a modulating index, with spreading artifacts below 20 kHz, could manifest itself as audible noise. On the high end, one has to take care when the modulating switching frequency is greater than the loop-crossover frequency of the feedback-control loop, as this could impact loop stability and output-ripple voltage.

It has been proven mathematically that the technique of frequency modulation in the time domain has the effect of spreading energy in the frequency domain and reducing harmonic-peak amplitude. The next step is to evaluate how to most effectively implement this technique for a given application. The modulation waveform, frequency, and depth of modulation must be selected to achieve the desired scattering effect while also satisfying agency requirements for RBW.

For a continuous-wave modulation, the various modulation waveform shapes exhibit a different spectral spreading effect. Modulation waveforms can be linear and symmetrical or nonlinear and asymmetrical. *Hershey-kiss* modulation offers the benefit of achieving a very flat spectral response, where sideband energy is made to equal the fundamental. This is key to maximizing the attenuation of the fundamental and its harmonics.

Although much easier to analyze and implement, a *sinusoidal* modulation waveform does not provide optimum attenuation of the harmonics. The energy in the spectrum of the modulated waveform will tend to concentrate at those frequencies corresponding to points in the modulation waveform where the time derivative is small. The *triangular* modulation waveform is often used as a good compromise.

A deeper and approfondite analysis on spread spectrum modulation can be found in Appendix F.

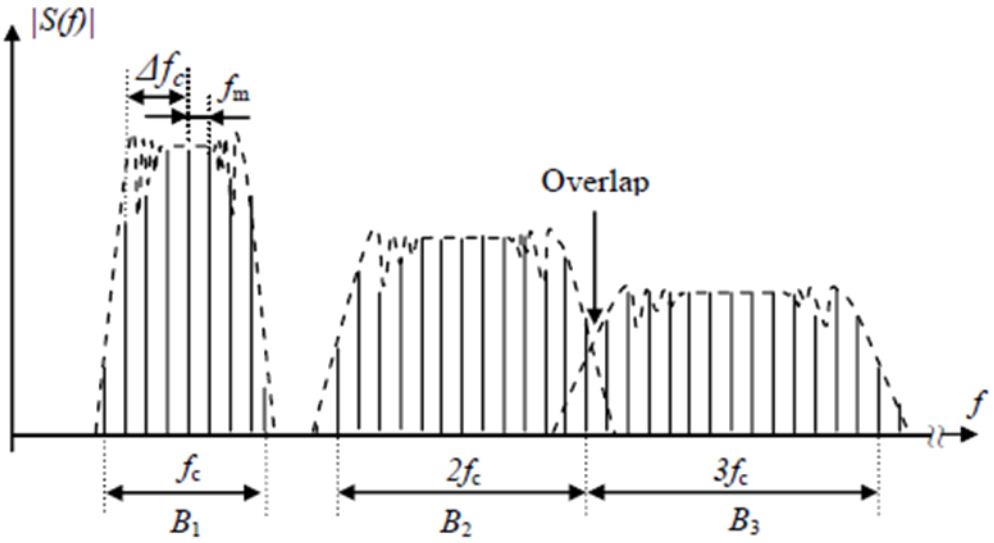
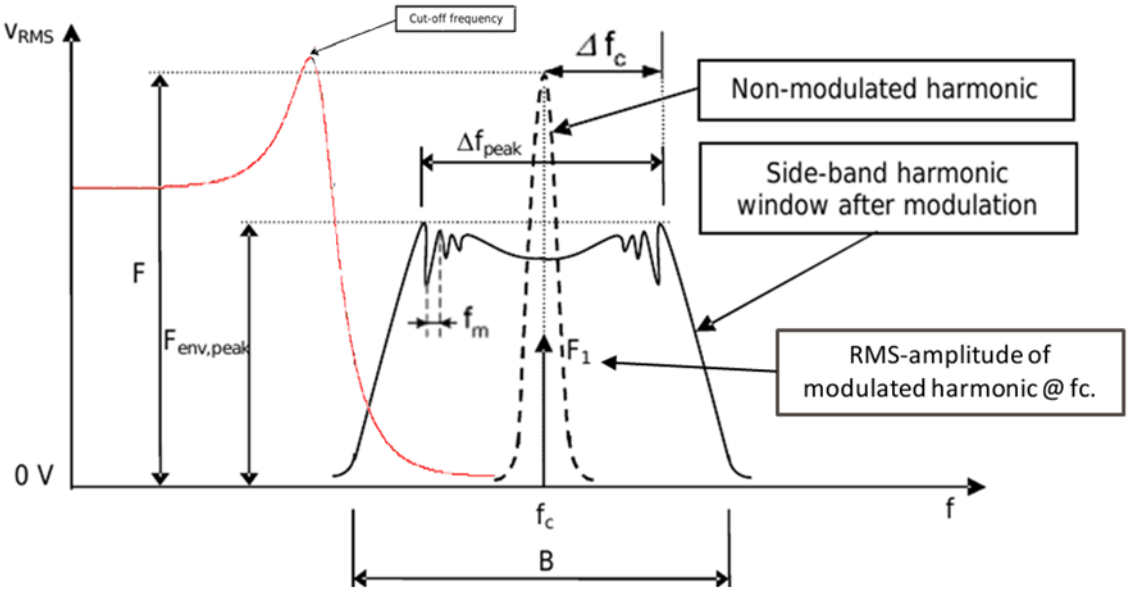


Figure 3.8: Spread Spectrum



$$B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m)$$

Figure 3.9: Spread Spectrum carrier window

3.4.4 Randomic or pseudo-random modulation

Although the periodic frequency modulation is clearly effective in spreading harmonic content, in some cases it may not provide sufficient attenuation of the fundamental. An alternative to periodic

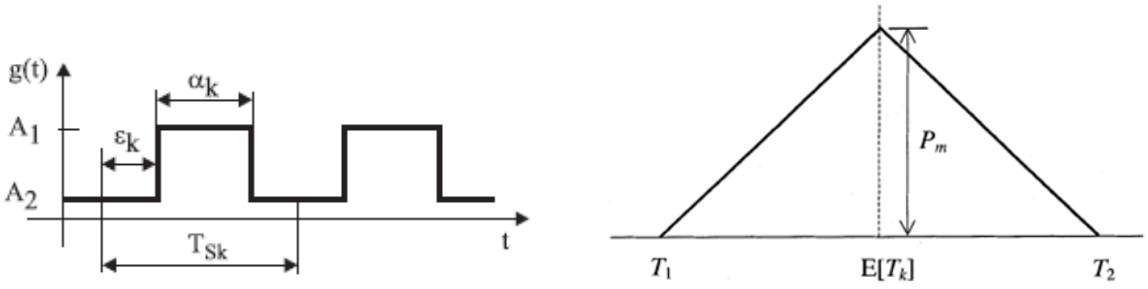
SSFM is random or pseudo-random modulation either of which can actually result in greater spectral spreading of the fundamental.

Recently, random switching technique has been recognized as an emerging technology for power converters. Various random switching schemes, which are originated from statistical communication theory, have been reported for DC-DC power conversion. From several randomized modulation strategies, four of them are more favorable (see Table 3.1): random pulseposition modulation (RPPM), random pulse width modulation (RPWM), and random carrier-frequency modulation with a fixed duty cycle (RCFMFD), or with a variable duty cycle (RCFMVD), as considered in [38]. The characteristics of the switching pulse in each modulation scheme are summarized in Table 3.1, with the aid of Figure 3.10(a). The switching function $g(t)$ has two discrete levels (namely A_1 and A_2), which are applicable for describing the behavior of classical DC-DC converters. T_{S_k} is the duration of the k-th cycle. α_k is the duration of the gate pulse in the k-th cycle and ϵ_k is the delay time of the gate pulse. The duty cycle of the switch d_k in the k-th cycle is equal to α_k/T_{S_k}. RPPM is similar to the classical PWM scheme with constant switching frequency. However, the position of the gate pulse is randomized within each switching period, instead of commencing at the start of each cycle. RPWM allows the pulse width to vary but the average pulse width is equal to the required duty cycle. RCFMFD exhibits a randomized switching period and constant duty cycle, whilest RCFMVD exhibits a randomized switching period and constant pulse width. As the pulse width in RCFMVD is fixed and the switching period is randomized, the resultant duty cycle is also randomized. Nevertheless, the average duty cycle is equal to the desired value.

Modulation	T_{s_k}	α_k	ϵ_k	$d_k = \alpha_k/T_{s_k}$	Randomness level $\Re$
PWM	const	const	0	const	
RPPM	const	const	rand	const	$\Re_{RPPM} = \dfrac{\epsilon_2 - \epsilon_1}{T_S}$
RPWM	const	rand	0	rand	$\Re_{RPWM} = \dfrac{\alpha_2 - \alpha_1}{T_S}$
RCFMFD	rand	rand	0	const	$\Re_{RCFMFD} = \dfrac{T_2 - T_1}{T_S}$
RCFMVD	rand	const	0	rand	$\Re_{RCFMVD} = \dfrac{T_2 - T_1}{T_S}$

Table 3.1: Characteristics of different random switching schemes.

The basic principle of introducing randomness into standard PWM scheme is to spread out the



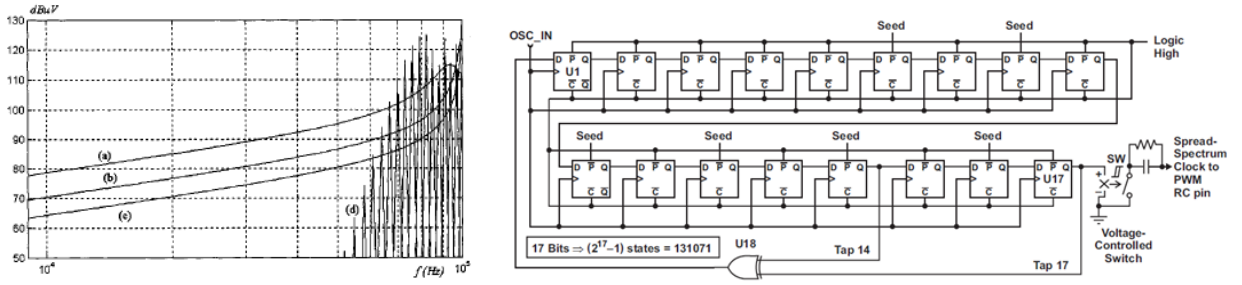
(a) (b)

Figure 3.10: (a) Switching signal in randomized modulation scheme. (b) Probability density function of the switching period.

harmonic power so that no harmonic of significant magnitude exists. As a result, discrete harmonics are significantly reduced and the harmonic power is spread over the spectrum as noise (continuous spectrum). It has been pointed out that the continuous noise spectrum within the pass band of the converter's output low-pass filter could lead to noise-induced low-frequency voltage ripple in the converter's output. This undesirable feature may prohibit the use of random modulation in DC-DC converters, which require tight voltage regulation.

Periodic SSFM requires a periodic modulating signal whilst random SSFM requires either a digital or analog noise generator. A digital-circuit-based pseudorandom signal generator, a microprocessor-based pseudorandom algorithm or a reverse-biased transistor for generating thermal noise in wideband nature can be used to provide the random variable in random SSFM. With a pseudo-random noise generator, the switching frequency varies randomly from cycle to cycle over a range determined by the random-number generator's clock. The technique for implementing a pseudo-random sequence is most easily realized with a linear-feedback shift register, a row of serially connected shift registers where the intermediate values are manipulated in a modulo-2 summation fashion to generate the next state.

Basically, random SSFM gives higher low-frequency harmonics than the periodic SSFM. No harmonics will be generated beyond the sideband of the first-order-switching harmonic in periodic SSFM, see Figure 3.11(a). It can be observed [38] that the random SSFM introduces higher low-frequency variation than the periodic SSFM, thus confirming the theoretical prediction. Although low-frequency harmonics in the random SSFM can be reduced with a smaller $\Re$, the effectiveness of the frequency spreading will be lowered and the harmonic components around the switching



(a) (b)

Figure 3.11: (a) Comparison of the low-frequency characteristics of the diode voltage with RBW = 200 Hz. Random SSFM *(a):* $\Re = 0.5$ *(b):* $\Re = 0.2$ *(c):* $\Re = 0.1$ *(d):* Periodic SSFM. (b) Pseudo-random bit sequencer using a linear-feedback shift register.

frequency will be increased. Nevertheless, with the same frequency deviation, random SSFM gives a more effective way to disperse the harmonics around the switching frequency than the PCFM. Due to different spectral behaviors of the two schemes, they can be applied to applications of different requirements. Periodic SSFM is more suitable for applications that require tight output regulation, like DC-DC converters, since it introduces lower undesirable low-frequency harmonics at the output. On the other hand, random SSFM is more suitable for applications that do not require tight output regulation, like *power-factor correctors* (PFC), since output regulation is usually performed in the second stage and high-frequency harmonic suppression is more effective.

Although good regulation is maintained, irregularities in the output-voltage ripple are evident as a result of momentary changes in duty cycle between states. Increasing the number of states improves spreading and reduces output irregularities.

3.4.5 Chaotic modulation

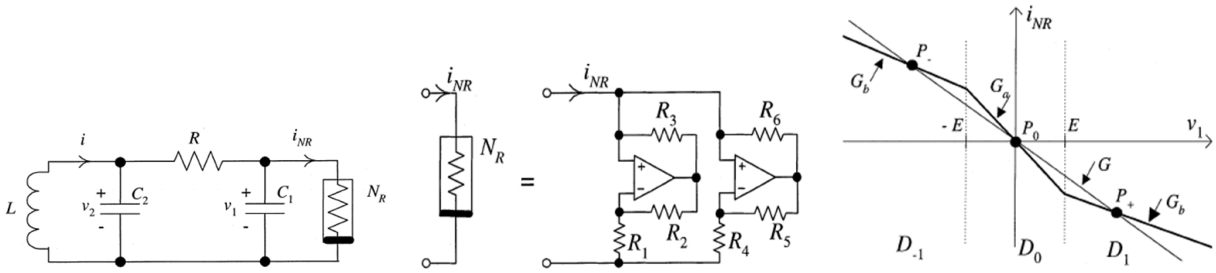
More recently, it has been well accepted that chaos can be used to improve the electromagnetic interference (EMI) for DC-DC converters due to its continuous spectrum feature. The working principal of chaotic frequency modulation technique is same as simple frequency modulation technique, here PWM frequency spread chaotically and energy can be distributed having lower amplitude.

Roughly speaking, there are two kinds of control methodologies to generate chaotic signals in DC-DC converters. One is to make a DC-DC converter itself chaotic by adjusting the system parameters; the other is by chaotic PWM control to make the DC-DC converter chaotic. The

fact that DC-DC converters nonnally work with rated parameters makes the first methodology unrealistic, therefore, the second one is mostly adopted, herein, a chaotic carrier plays a key role. The focus of the chaotic PWM is on designing a chaotic carrier to generate chaotic signals.

Theoretically, a chaotic carrier can be designed in digital or analogue way. The digital chaotic carrier (chaotic or logistic map) is accurate, otherwise the cost is high. On the contrary, the cost of the analogue chaotic carrier is much lower; and the regulable frequency can be much higher by changing the resistance and capacitance of the analogue chaotic carrier circuit, suitable for the function of high frequency DC-DC converters. Furthennore, numerous existing chaotic oscillators can be employed for designing the analogue chaotic carrier.

In recent decades, chaotic oscillators have widely been investigated . Among the existing chaotic oscillators, Chua's, Lorentz's, and Chen's oscillators are well known. In this section, *Chua's oscillator* is adopted due to its simplicity and maturity. Figure 3.12(a) shows Chua's oscillator, in which the value of the voltage-controlled nonlinear resistor N_R or Chua's diode significantly affects the circuit behavior.



(a) (b) (c)

Figure 3.12: (a) Schematic of Chua's circuit. (b) Characteristic of nonlinear resistor N_R. (c) Realization of nonlinear resistor using op-amps.

Characteristics of the nonlinear resistor current i_{NR} are shown in Figure 3.12(b). Depending on the value of v_1, N_R acts as a negative piecewise-linear conductance in three segments. If the absolute value of v_1 is less than a threshold voltage E, N_R equals G_a. Otherwise, N_R equals G_b. Mathematically:

$$i_R = f(v_1) = \begin{cases} G_b v_1 + (G_b - G_a)E & \text{for } v_1 < -E \\ G_a v_1 & \text{for } -E \le v_1 \le E \\ G_b v_1 + (G_a - G_b)E & \text{for } v_1 > E \end{cases} \tag{3.1}$$

where $f(\cdot)$ is the function showing the relationships between i_{NR} and v_1, and $G = 1/R$. The Chua's circuit can be operated in three regions, namely, region "D_{-1}" for $v_1 < -E$, region "D_0" for $-E \leq v_1 \leq E$, and region "D_1" for $v_1 > E$. The eigenvalues in each operating region are determined by solving (3.1). The eigenvalues vary with R. Decreasing the value of R causes the circuit to change from equilibrium to chaos (equilibrium, period-1 limit cycle, period-2 limit cycle, period-4 limit cycle, spiral chaos and double-scroll chaos). The practical circuit of N_R is shown in Figure 3.12(c), having dual operational amplifiers and six resistors. G_a, G_b, and E are defined as follows:

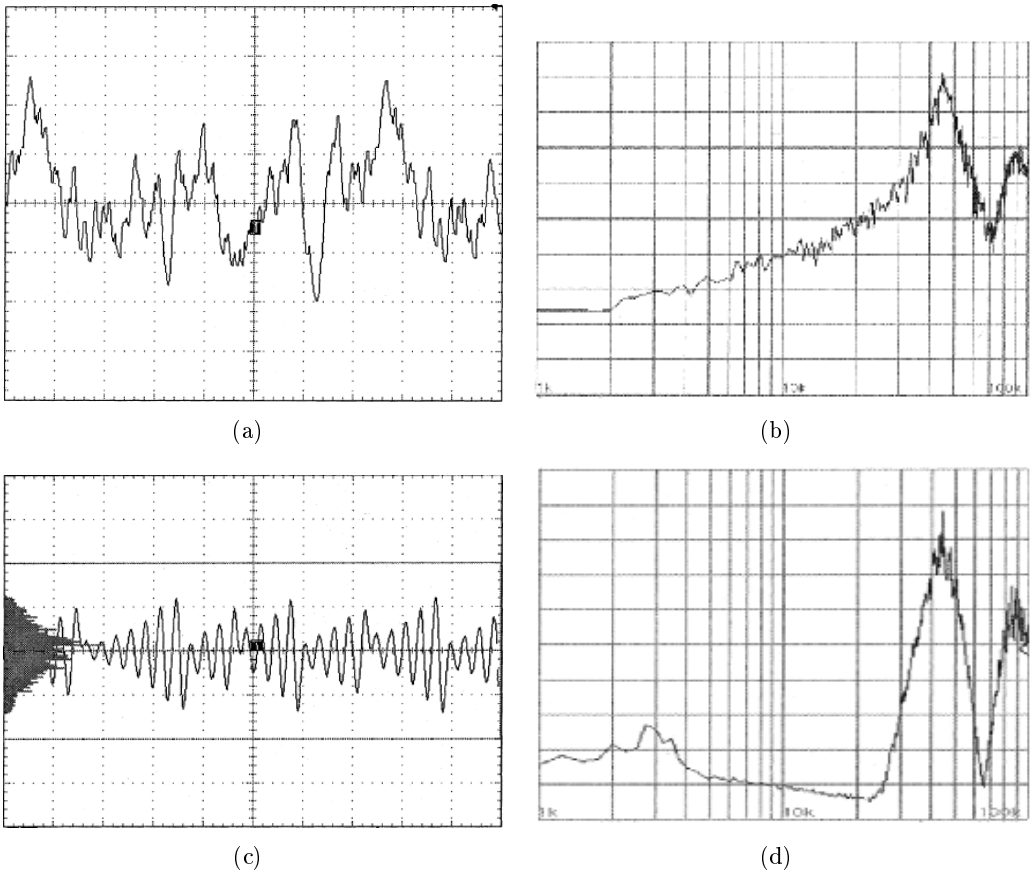
$$G_a = -\frac{R_2}{R_1 R_3} - \frac{R_4}{R_5 R_6} \tag{3.2}$$

$$G_a = \frac{1}{R_3} - \frac{R_4}{R_5 R_6} \tag{3.3}$$

$$E = E_{sat}\frac{R_1}{R_1 + R_2} \tag{3.4}$$

where E_{sat} is the saturation level of the operational amplifiers.

Chaotic operation is deterministic but not predictable. This often misleads some to think that chaotic operation is a random process. Chaos is not a random process, but it usually looks like random. The low-frequency spectral magnitude in the randomic SSFM is higher than that in the chaotic. By comparing Figure 3.13(c) with Figure 3.13(a), the Chua's circuit output signal oscillates alternatively and symmetrically around the origin (even if the amplitude varies). The probability of generating biased and/or lowfrequency harmonic components with chaotic modulation is lower than that of the random modulation. Hence, even if the chaotic and random modulations are stochastic in nature and exhibit the same probability density function, their spectral behaviors are slightly different because the time-domain variation cannot be obtained from the probability density function. Nevertheless, chaotic SSFM has the advantages that it does not introduce significant low-frequency harmonics and that it improves high-frequency characteristics in the conducted EME spectrum. Chaotic SSFM hybridizes the features of periodic and random modulations.



(a) (b)

(c) (d)

Figure 3.13: (a) Random modulation profile. (b) Measured conducted EME in the low frequency range with randomic SSFM. (c) Chaotic modulation profile. (d) Measured conducted EME in the low frequency range with chaotic SSFM.

Chapter 4

MATLAB tool: for understanding and performing Spread Spectrum Modulation

This chapter introduces a software tool developed during this thesis work. The aims and the targets that this tool accomplish are presented in the next section. Follows a description of the tool's Graphical User Interface (GUI), and a brief explanation about the Matlab source code and the structure of the algorithm. Finally are shown the simulation results which will be the basis for the implementation of a Spread Spectrum Clock Generator, described in the next chapter.

4.1 Goals and tasks

At a first step, we need to understand theoretical and real benefits of Spread Spectrum Modulation techniques, and benchmark the reduction of conducted EMI emissions from a generic Switched Mode Power Supply that these techniques can provide. In the previous chapter several Spread Spectrum Modulation techniques and profiles were discussed. All these techniques can be found in literature and many articles have shown their respective results obtained by applying different Spread Spectrum modulations. Therefore, with this new software tool we want to verify the techniques available in literature and match their results, in this way we can made a verification test of the tool's capabilities.

In general conducted EMI analysis and specially Spread Spectrum Modulation techniques are topics quite difficult to understand for beginners, and there are many different standardized test measurement setups. Thus, first of all, we need a user friendly tool that lets us "to play" with all the SSM techniques and profiles, with all the several modulation parameters, in different test measurement setups.

Adopting a monolithic GUI approach, the amount of implemented features, will bring down

to a crowded and confusional GUI with too many setup parameters in little space. Therefore, the idea behind is to implement a multi GUI structure to help us to manage a lot of different test setup and SSM parameters.

The main reason for the birth of this tool, is to provide a very complete suite, not bound to the Cadence framework, for benchmarking the spread spectrum techniques, and to define the best parameter values for applying these techniques. In literature, these analysis were made only by applying a simple Discrete Fourier Transform to a frequency modulated tone. With this method can be proved in a theoric way that when a spread spectrum modulation technique is applied to a tone, the resulting spectrum is spreaded over a range of frequencies and there is a reduction on the maximum value of the power spectrum. But don't yet exist studies and tools that can simulate and evaluate the reduction over the conducted electromagnetic emissions (EME), that carries out from a Switched Mode Power Converter (like a step-down buck), with a standardized test setup, when spread spectrum modulation techniques are applied.

As already explained even if there is a reduction in the conducted EMI emissions, by applying Spread Spectrum Modulation, these enhancement can be faded by normative and by the standardized test measurement setups. In fact, as one can see using this tool, the final reduction on the conductive EME are very dependent by the modulation parameters and by the normative parameters of the measurement instrument, like the resolution bandwith and detector's type in a scanning receiver, as example.

The aim of this tool is not only to apply a spread spectrum modulation to a single sinusoidal carrier, but to all the harmonic content generated by a SMPC, and analyze the conducted EMI that arise from a real test measurement setup, that complies with standard normatives (like the CISPR 25 Artificial Network, and the IEC 61967-4 150Ω methods).

Finally to make this tool more complete as possible, it was added another feature, which allows to post-processing a transient signal previously generated by a simulation in Cadence framework (the user needs to design by himself the entire test setup in Cadence), and to perform a spectrum analysis, emulating a real spectrum analyzer or a scanning receiver.

4.2 Usage instructions and system requirements

The tool is carried out with a `.zip` archive containing several files, and to work properly it requires a `Unix` machine with this softwares installed:

- `matlab/R2009b`: currently the application requires a running Matlab^{TM} 7.9 enviroment in background. To avoid any type of incompatibilities the tool have to run with the Matlab 7.9 (R2009b) version, any other version has not been tested so far.
- `mmsim/7.2.0.isr6`: Cadence plugin that allows the tool to comunicate with the Cadence framework and to import the simulation data results.
- `acroread/(any version)`: to view the program help documentation and tutorial.

In order to start the tool just type in a terminal shell the command `SpreadSpectrumTool` from the directory where you have extracted the `.zip` archive. The `SpreadSpectrumTool` file is a script that needs execution permissions to run.

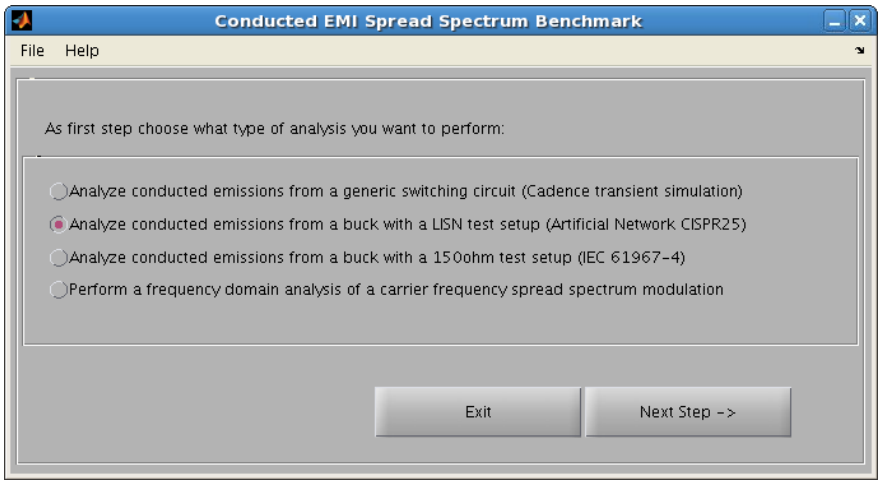


Figure 4.1: Main window

As the program is full loaded a graphic window pop-up, as depicted in Figure 4.1. The graphical user interface (GUI) is waiting for user input. With this first window, the user can choose what type of test setup simulation he wants to perform, like:

- post-process the spectrum of a transient signal previously simulated in Cadence, through a real scanning receiver instrument emulation;

- analyze the conducted EMI from a buck converter through a LISN or a 150 Ω test setup simulated with Simulink/Matlab and with a Spread Spectrum Modulation applied;
- analyze the spectrum of the carrier tone with a Spread Spectrum Modulation applied by the tool, through a real scanning receiver instrument emulation.

Here the user need only to select the right option and then press the `Next Step` push-button, otherwise just close the tool. According to selection different dialog interfaces are shown. Each dialog interface acts for the option selected and try to represent in a graphic way the measurement test setup selected.

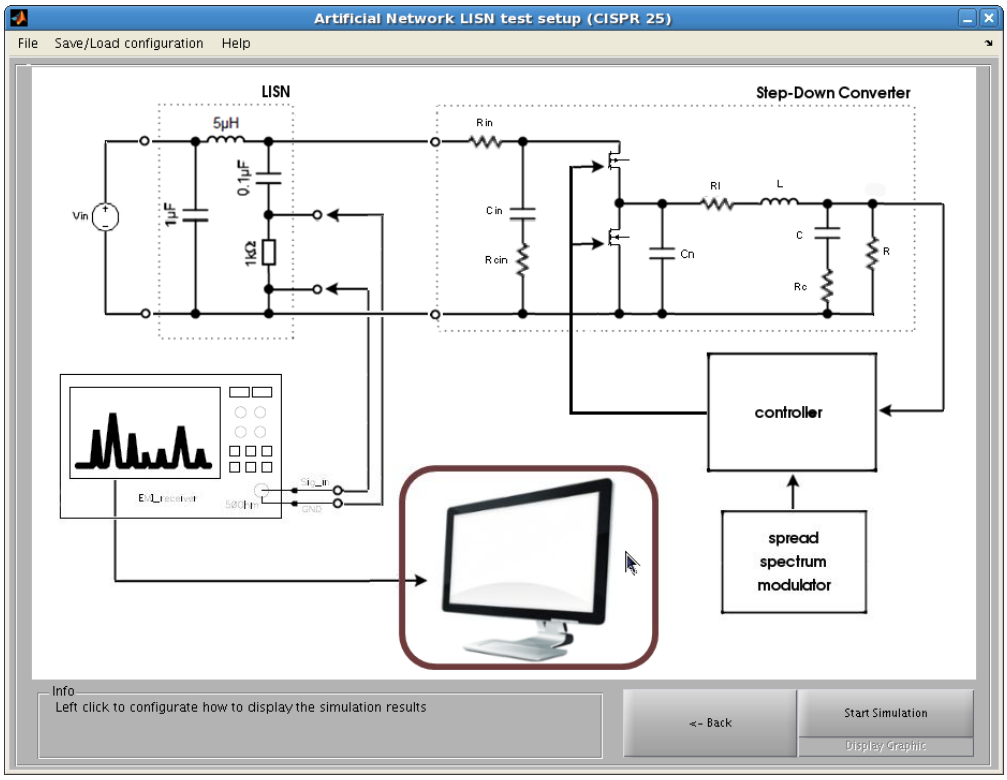


Figure 4.2: Graphical User Interface

The graphic interface of the option selected is composed by a picture and some command to go back at the beginning and to proceed with the simulation and the relative result visualisation. The GUI has menu bar with several sub-menu like the `Help`, the `File` and the `Save/Load configuration`, with these, the user can save several test setups, each with different modulation and measurement parameters, and to recall they in any moment. The tool come with a default

parameter setting. This setting can be changed and the new one can be set as the default.

4.3 Tool structure

As already mentioned, each dialog has a picture that is a graphical representation of the measurement test setup selected, and it is composed by some blocks connected by arrows. The picture isn't a static figure, but as the mouse cursor is moving over the picture's area, the figure dinamically changes and the different blocks that acts for the measurement setup are enlightened (see Figure 4.2). Left clicking the mouse over the enlightened block would open the respective configuration dialog box, where the user can set many parameters. Each block have a different configuration dialog box, and also the setting parameters change.

The user can consider the tool composed by four sub-program grouped all together. Below can be found a brief explanation of the overall usage flow of the application, divided in three parts according to the selection in first application window (the second one and the third one options will be treated together). The four sub-program share same configuration blocks, therefore they are explained only once.

4.3.1 First sub-program

The purpose of the sub-application is to emulate measurement using an EMI receiver. Simulated or measured time domain data is processed to give a EMI receiver result in the frequency domain. Basically measured or simulated data in the time domain is fed by the user as well as the appropriate settings and afterwards the application computes an emulation of the results in the frequency domain. It is able to display the result in a diagram and to export the results into a image file as well as into a PDF document.

The GUI is basically composed by three parts:

- **PSF Input configuration**
- **EMI receiver configuration**
- **Output configuration**

By pressing the "Start Data Processing" button the post processing is issued. Input data is transformed according to the settings made by the user. Depending on system performance this may

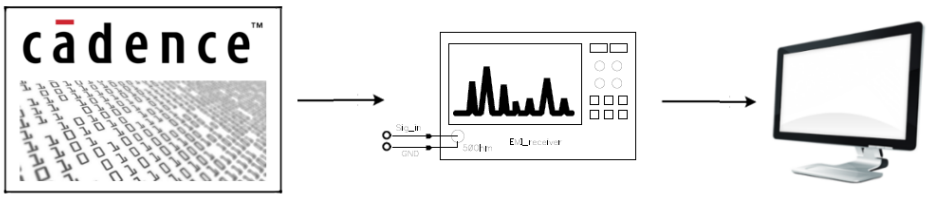


Figure 4.3: Open file setup interface

take some time. After data has been processed the result can be displayed in a Cartesian diagram as shown in Figure []. The final result diagram is created automatically. Appropriate limit curves are shown according the GUI settings. If the user marked the "Export []" checkbox previously the diagram is additionally exported into a picture file format or in an Adobe PDF document.

4.3.2 Second and third sub-programs

The purpose of the sub-application is to emulate measurement using an EMI receiver of the conducted EMI emission produced by a buck converter, and to add a way to reduce this conducted emission using a spread spectrum modulation. According to the selected option the testbench changes. For the second option a CISPR 25 LISN test setup is used, otherwise for the third option an IEC 61967-4 150Ω direct method is used. Also the main picture will change to rappresent the different test setups. In the first case there is rappresented a LISN network between battery and the buck plant, and there is also an input RC filter that can be easily enabled/disabled, here the conducted emissions to battery are analyzed. In the second case, instead, the conducted emissions that come from the output pins are analyzed. Here, the input RC filter disappear, and the artificial network will became a 150Ω network.

The DC-DC step-down converter is simulated through a Simulink model with each block (plant, PID controller and SSCG) realized as a Time Discrete Model. Simulated or measured time domain data is processed to give a EMI receiver result in the frequency domain. Basically measured or simulated data in the time domain is fed by the user as well as the appropriate settings and afterwards the application computes an emulation of the results in the frequency domain. It is able to display the result in a diagram and to export it.

The GUI is basically composed by five parts:

- **Plant configuration**
- **PID Controller configuration**
- **Spread Spectrum Clock Generator configuration**
- **EMI receiver configuration**
- **Output configuration**

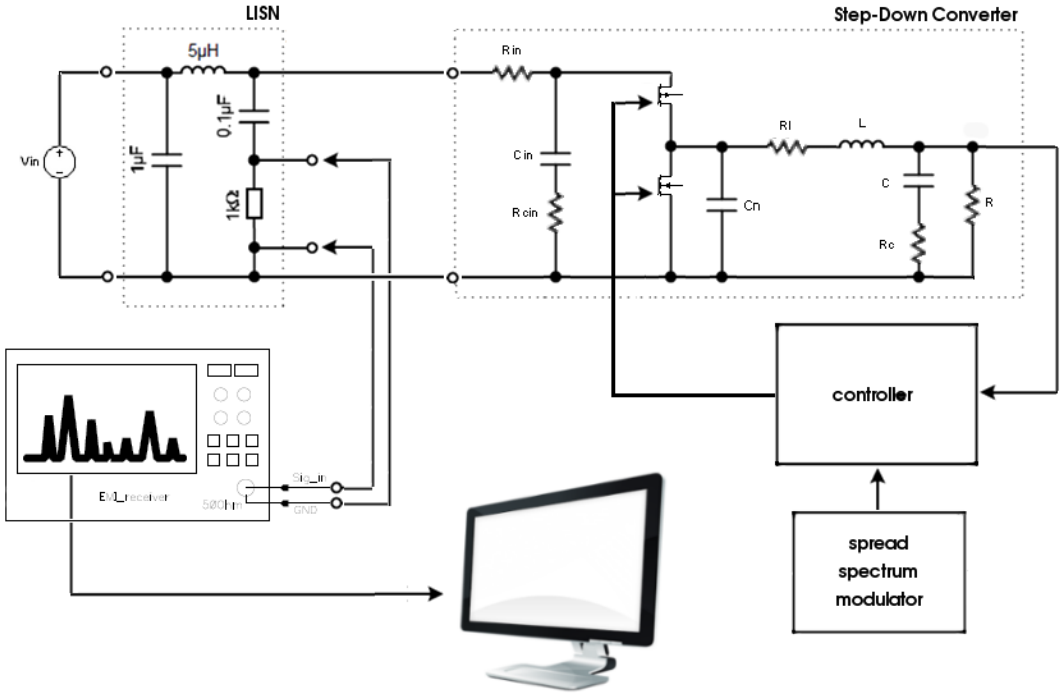


Figure 4.4: Buck LISN setup interface

Buck converter simulation

The DC-DC step-down converter is simulated through a Simulink model with each block like plant, and the PID controller, is realized as a Time Discrete Model. This approach use finite difference equations to give faster simulation times.

Simulink is used only as a GUI for the top level schematic. All functions, such as PLANT, PID CONTROLLER and SPREAD SPECTRUM MODULATOR are implemented as *Embedded*

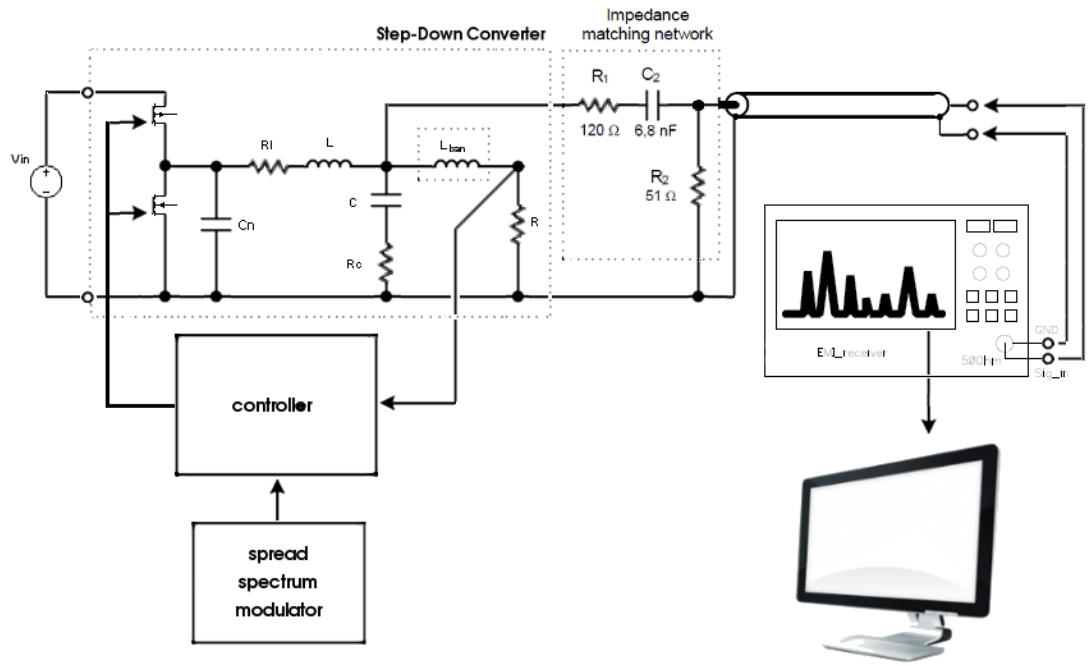


Figure 4.5: Buck 150 Ω setup interface

Matlab functions, as shown in Figure 4.6. Transistors are modeled with variable resistors plus a parasitic capacitor.

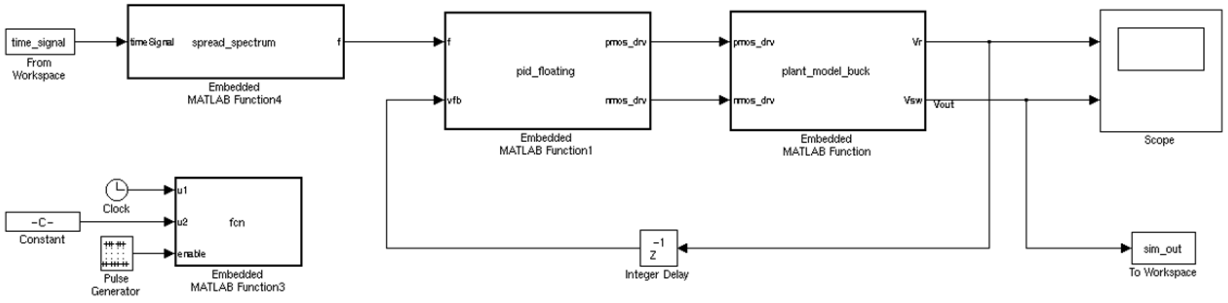


Figure 4.6: Simulink top level schematic.

What about the implementation of a switch-mode power converter in Simulink? In the classical way of using Simulink, the basic elements available in the Simulink libraries are flow connected. This approach has the disadvantage of being not very readable, especially for people not used to Simulink, and modifications require to re-draw the all stuff. Moreover there are no comments and

not a clear flow direction and therefore it is hard to understand the sequence of processing and it is also hard to debug (one needs to put scopes everywhere and to observe internal node you have to bring up in the hierarchies). Lastly all parameters have to be written inside the mask of each small block. Otherwise if Simulink is used only as GUI for the top level schematic and all crucial functions are implemented as Embedded Matlab functions the code isn't embedded directly in the Simulink block but written in a dedicated Matlab function. This approach lets to reuse the same function for different tasks (e.g. the same PID controller for a buck or for a boost converter), and when you want to change a model, one just needs to change the function he is referring to (e.g. you want to try two output caps instead of one). The top level schematic use only very basic blocks of Simulink especially `sources` (stimuli, constants, pattern) and `sinks` (scope, pattern to workspace).

Using Embedded Matlab functions lets to put all the system parameters in a single global variable called `parameters` in the matlab workspace. In this way all the parameters are always available in every function and you need to pass only one single variable.

The PID Controller Embedeed Matlab Function samples the output voltage just before the transition from the low to the high state, of the PWM signal. Then it calculates the new `Toff` phase once per switching period and finally it generates the two driving signals for the NMOS/PMOS switches.

Time discrete modeling of a Buck converter

Simulating using a time discrete model give the advantage of a much shorter simulation time than with a continuous time model. Moreover you can define your model only with equations, therefore there is no need of complicated Simulink schematic.

In order to define a buck converter model only with equations, PMOS and NMOS transistors are modeled with variable resistors (`Rp`, `Rn`) plus a parasitic capacitor `Cn`. With this approach the circuit to solve in the LISN test setup case, will became the one shown in Figure 4.7. To solve this circuit we have to build some finite difference equations. In order to do this, we have to write an equation for each single variable, that are, the currents that flow in each circuit branch, and the voltages over each component.

This will lead for the LISN test setup to a linear system with 30 equations and 30 variables. The plant is composed by seven memory elements, this will lead to seven state update equations. `Vco`, `Ilo`, `Vcno`, `Vcino`, `Vc1lisno`, `Vc2lisno`, `Illisno` are the state variables of the system. The

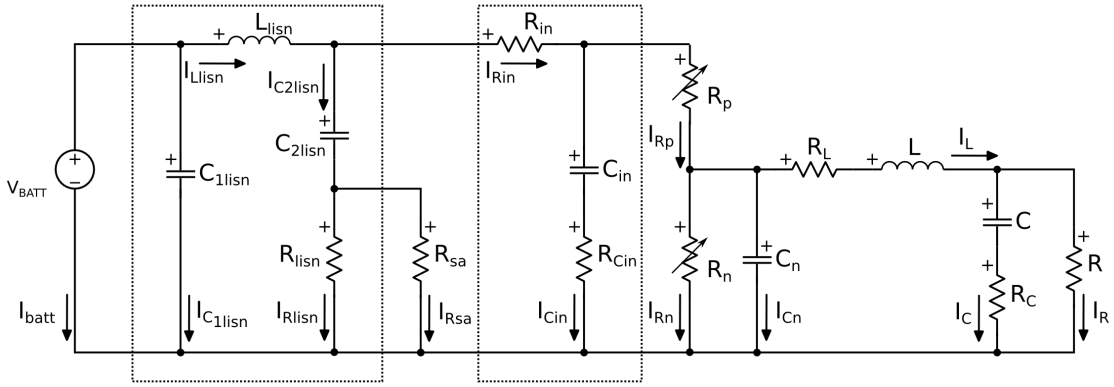


Figure 4.7: Schematic of the circuit resolved in Matlab

circuit plant is composed by 8 mesh or loops, 6 nodes and 16 components, therefore, the 30 equations linear system is composed by 8 Kirchhoff's mesh voltage equations, 6 Kirchhoff's current node equations and 16 generic Ohm's law equations.

```
n1 = Vrin - Rin * Iin == 0
n2 = Vrcin - Icin * Rcin == 0
n3 = Vcin - Vcino - Icin / Cin == 0
n4 = Vrp - Rp * Irp == 0
n5 = Vrn - Rn * Irn == 0
n6 = Vcn - Vcno - Icn / Cn == 0
n7 = Vrl - Rl * Il == 0
n8 = Il - Ilo - Vl / L == 0
n9 = Vc - Vco - Ic/C == 0
n10 = Vrc - Ic * Rc == 0
n11 = Vr - R * Ir == 0
n12 = Vc1lisn - Vc1lisno - Ic1lisn / C1lisn == 0
n13 = Vc2lisn - Vc2lisno - Ic2lisn / C2lisn == 0
n14 = Illisn - Illisno - Vllisn / Llisn == 0
n15 = Vrlisn - Rlisn * Irlisn == 0
n16 = Vrsa - Rsa * Irsa == 0
n17 = Iin - Icin - Irp == 0
n18 = Irp - Irn - Icn - Il == 0
n19 = Il - Ic - Ir == 0
n20 = Ibatt - Ic1lisn - Illisn == 0
n21 = Ic2lisn - Irlisn - Irsa == 0
n22 = Illisn - Iin - Ic2lisn == 0
n23 = Vc2lisn + Vrsa - Vrin - Vcin - Vrcin == 0
n24 = Vcin + Vrcin - Vrp - Vrn == 0
n25 = Vrn - Vcn == 0
n26 = Vcn - Vrl - Vl - Vc - Vrc == 0
n27 = Vc + Vrc - Vr == 0
n28 = Vbatt - Vc1lisn == 0
n29 = Vrlisn - Vrsa == 0
n30 = Vc1lisn - Vrlisn - Vc2lisn - Vllisn == 0
```

In the 150 Ω test setup case the circuit to solve, will became the one shown in Figure 4.8.

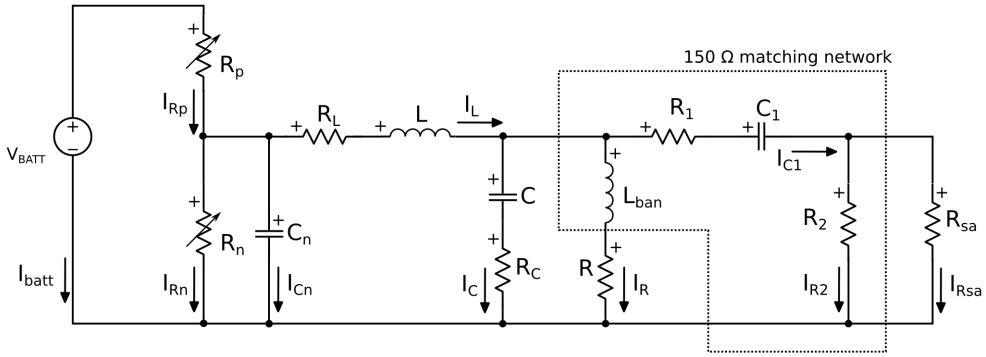


Figure 4.8: Schematic of the circuit resolved in Matlab

This will lead to a linear system with 22 equations and 22 variables. The plant is composed by five memory elements, this will lead to five state update equations. `Vco`, `Ilo`, `Vcno`, `Vc1o`, `Ilbano` are the state variables of the system. The circuit plant is composed by 6 mesh or loops, 3 nodes and 13 components, therefore, the 30 equations linear system is composed by 6 Kirchhoff's mesh voltage equations, 3 Kirchhoff's current node equations and 13 generic Ohm's law equations.

```
n1 = Vrp - Rp * Irp == 0
n2 = Vrn - Rn * Irn == 0
n3 = Vcn - Vcno - Icn / Cn == 0
n4 = Vrl - Rl * Il == 0
n5 = Il - Ilo - Vl / L == 0
n6 = Vc - Vco - Ic/C == 0
n7 = Vrc - Ic * Rc == 0
n8 = Vr - R * Ilban == 0
n9 = Ilban - Ilbano - Vlban / Lban == 0
n10 = Vc1 - Vc1o - Ic1 / C1 == 0
n11 = Vr1 - R1 * Ic1 == 0
n12 = Vr2 - R2 * Ir2 == 0
n13 = Vrsa - Rsa * Irsa == 0
n14 = Irp - Irn - Icn - Il == 0
n15 = Il - Ic - Ilban - Ic1 == 0
n16 = Ic1 - Ir2 - Irsa == 0
n17 = Vr2 - Vrsa == 0
n18 = Vin - Vrp - Vrn == 0
n19 = Vrn - Vcn == 0
n20 = Vcn - Vrl - Vl - Vc - Vrc == 0
n21 = Vc + Vrc - Vr - Vlban == 0
n22 = Vr + Vlban - Vr1 - Vc1 - Vr2 == 0
```

Solving these linear systems with so many equations by hand would be a too long procedure.

Some symbolic calculator softwares, like Matlab MuPAD and Mathematica, can perform this operation very fast. If Mathematica is used the results needs to be converted to Matlab format, moreover the editor is quite unfriendly, and there is no syntax control, so it is hard to debug typing errors. Otherwise using Matlab MuPAD to solve these systems is quite easy, and the result can be rapidly integrated in the Matlab code of the tool.

For both systems the capacitor's C and inductor's L values are normalized by the time step:

```
C = C/T
L = L/T
```

4.3.3 Fourth sub-program

With this last part of the tool, the user can analyze the spectrum of a tone with a Spread Spectrum Modulation applied by the tool, through a real scanning receiver instrument emulation.

The algorithm developed is intended to carry out the main function of generating any frequency modulation of a sinusoidal carrier. These results are also valid for any generic carrier, as square clocks signals in digital devices, PWM signals controlling the switching power converters or trapezoidal signals in digital communication systems. This modulation data are not only valid for the theoretical calculation of the resulting spectra after modulation but also for obtaining a data set to be introduced into the arbitrary function generator. The output resulting spectra can be subsequently post-processed by emulating a measurement using an EMI receiver.

The GUI is basically composed by four parts:

- **Carrier tone configuration**
- **Spread Spectrum Clock Generator configuration**
- **EMI receiver configuration**
- **Output configuration**

The output of the modulation process can be expressed as follows:

$$F(t) = A \cdot \cos[\omega_c \cdot t + \Theta(t)] \qquad \text{where} \qquad \Theta(t) = \int_0^t k_\omega \cdot v_m(t) \cdot dt + \Theta(0) \tag{4.1}$$

where:

- A is a time-dependent amplitude

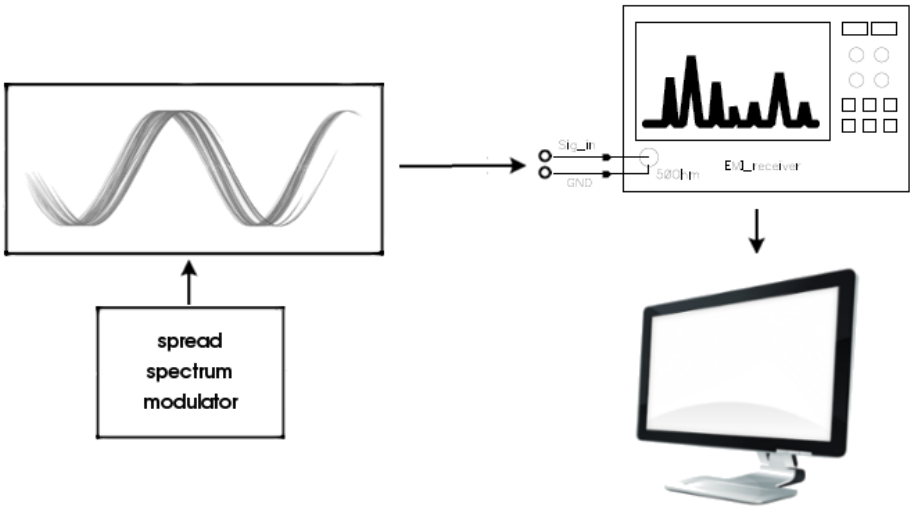


Figure 4.9: Carrier frequency setup interface

- $f_c(\omega_c = 2\pi f_c)$ is the carrier frequency
- $\Theta(t)$ is a time-dependent phase angle
- k_ω is a sensitivity factor of the modulator expressed in rad/sec/V or Hz/V
- $v_m(t)$ is the modulating signal (normally, a periodic wave of frequency f_m)
- $\Theta(0)$ is the initial value of phase and it is commonly taken as zero (this particularity does not subtract any generality to the resulting expression because it would only affect the absolute position of the window generated by the modulation of the original carrier but not to the relative distribution of the side-band harmonics inside this window).

Thus, once the profile or modulating signal equation $v_m(t)$ is selected, its integration, according to expression (4.1), yields a variable angle $\Theta(t)$ which, in summary, produces the variation of the instantaneous carrier frequency.

A working hypotheses is of application in the whole further calculations, defining V_m as the peak value of the modulating signal $v_m(t)$, the product $k_\omega \cdot V_m$ expresses the maximum peak deviation of the pulsation $\omega_c(t)$ respect to the central pulsation ω_c, that is:

$$\Delta\omega_c = 2\pi\Delta f_c = k_\omega \cdot V_m \tag{4.2}$$

Therefore, the frequency modulation can be easily computed with some few lines of code. In Figure 4.10 you can see some examples of the implemented profiles and their time integrals $\Theta(t)$.

4.3.4 Single configuration dialog description

PSF Input configuration

In this dialog GUI the user can specify the input file directory, where is supposed to be the PSF data format results specifying the time domain signal consisting of an advancing time vector and appropriate voltage values. Clicking on the "Browse" button opens a file dialog requesting a PSF directory specification. The directory is supposed to be PSF simulation data directory with files specifying the time domain signal consisting of an advancing time vector and appropriate voltage values. The "Simulation" should be chosen appropriately to the time domain simulation performed previously. Usually this is going to be `tran-tran`. Additionally the user is intended to specify the node name of the voltage signal which is to be processed by the application. After specifying the PSF directory and the simulation data the start and stop times stored in the file are updated automatically in the "T start" and "T stop" editor lines. The user can change these values as required in order to snip a certain part of the time domain voltage vector.

EMI receiver configuration

In this dialog EMI receiver's settings can be specified, like the resolution bandwith and detector, moreover the user can modify the data processing algorithm. The number of samples used to transform data into the time domain should be chosen such that on the one hand sufficient data points are available to achieve a certain maximum frequency in the final results and on the other hand to limit required time and memory consumption. A value of 2^{22} is a reasonable trade-off. The non-editable "F start" and "F stop" text boxes display the minimum and maximum frequencies (in MHz) of the result based on the start and stop time and the number of samples. The noise floor specifies the remaining noise in the result. A value of $-100 dB\mu V/\sqrt{Hz}$ is approximately what is achieved with real measurements in the EMC laboratory. During measurement of emissions using an EMI receiver there is a differentiation between "average", "peak" and "quasi-peak" detectors. Usually "peak" measurements are performed. The user can choose which type of detector should be emulated during data processing. EMI receivers sweep through frequency applying a bandpass

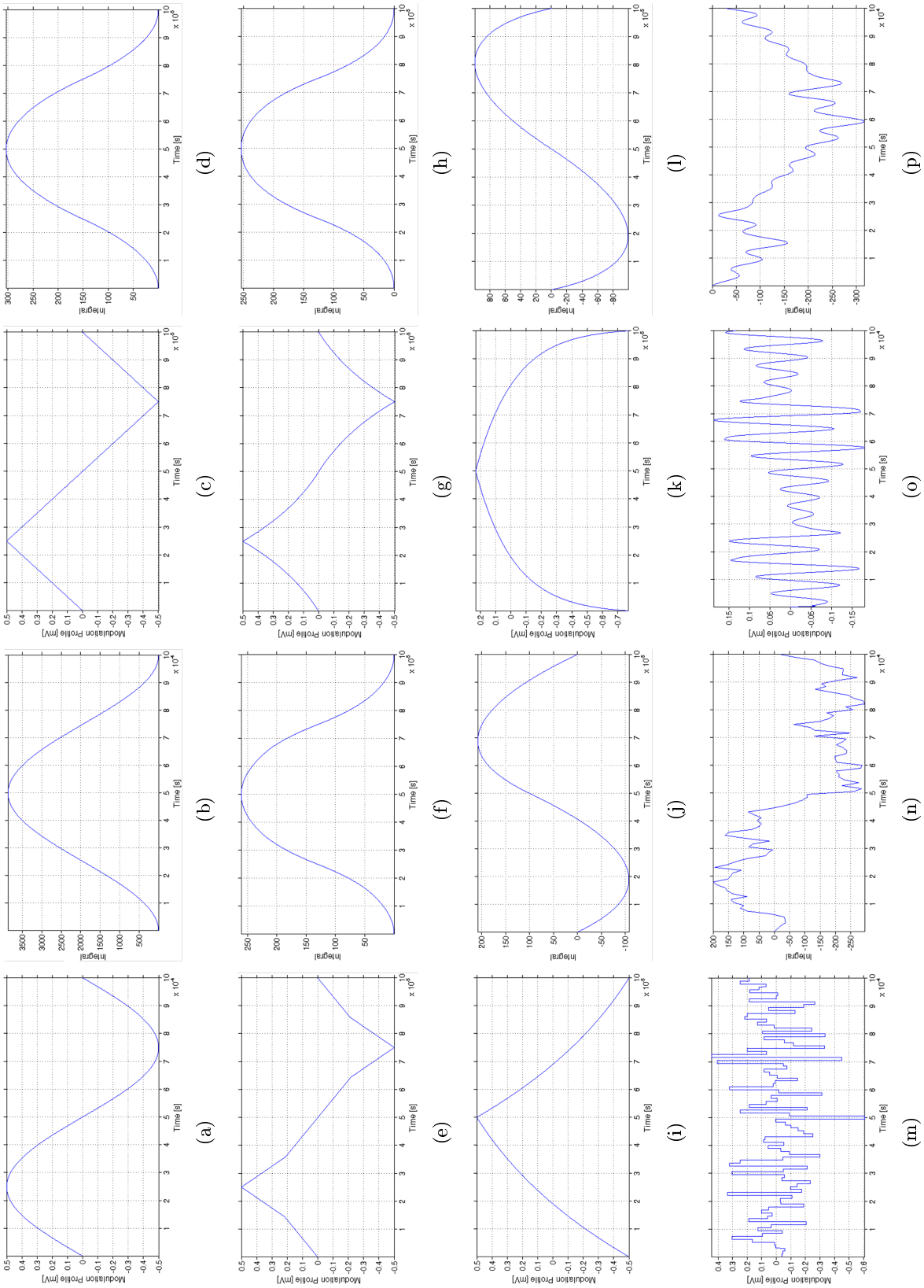


Figure 4.10: Different modulation profiles sinusoidal (a), triangular (c), multi-triangular (e), hershey-kiss (g), sharkfin (i), compensated (k), pseudo-random (m), chaotic (o), and their time integrals $\Theta(t)$ (b), (d), (f), (h), (j), (l), (n), (p)

filter to the signal and measuring the voltage signal. The filter specification made in appropriate international standards can be met with "gaussian" filter type. Before time domain voltage vector is transformed into the frequency domain the time domain samples are interpolated. The user can chose between "linear", "cubic", "spline" and "nearest" type of interpolation. Linear interpolation is fast, but spline interpolation results in the least noisy voltage waveforms. For the resolution bandwith box, predefined values are given such that usually no modification by the user is necessary here.

Output configuration

Within this dialog the output file and data viewer settings are made. The user is meant to specify the output file, can specify output options of the final result diagram and the type of limit curves displayed. By using the "Browse" button the user is asked for an output file name. Depending in the "LISN" or "VDE" choice for the limit curves and depending on the specified detector type different limit curves are drawn into the final result diagram. The limits are according to appropriate international standards and are subject of change.

Plant configuration

In this part the user can specify the values of the passive discrete components RLC that compose a typical step-down buck converter plant. This configuration part doesn't open a configuration dialog GUI, but opens some edit boxes are shown directly over the main picture, therefore the user can change the value of a plant component in a very quick-way. To make these edit boxes to disappear, just left click with the mouse cursor far away.

PID Controller configuration

In this dialog the user can configure a typical PID controller of a SMPC. The settings include the proportional, the integrative and the derivative coefficients, the carrier switching frequency of the SMPC, the output voltage that will also set the duty-cycle and finally, the oversampling ratio that fix the time resolution at which the simulation is performed.

Spread Spectrum Clock Generator configuration

Within this dialog GUI the user can fully customize a SSCG. The most important setting is

the modulation profile, the tool try to be more complete as possible, therefore all the most important profiles are implemented. They are divided in three categories: the chaotic, the random or pseudo-random and the periodic profiles. About the periodic profiles the user can choose between the most famous profiles that can be found in literature: sinusoidal, triangular, hershey-kiss, exponential, compensated and sharkfin. There is also the possibility to create a mixed profile between some of these profiles, in order to create a new profile combining the properties of the two original profiles. Moreover, a new modulation profile, is implemented. This new profile briefly called *multi-triangular* will be discussed in the next chapter.

After choosing the modulation profile, the user have to set other parameters. These settings change according to the profile chosen. If the user selects one of the periodic profiles, the modulation parameters that have to be setted are the modulation frequency f_m, and a parameter at choice between the voltage amplitude of the profile A_m, the amount of frequency spreading Δf_c and the modulation index $m_f = \frac{\Delta f_c}{f_m}$. Otherwise, if the user selects the pseudo-random or the chaotic profiles the setting parameters changes. For the pseudo-random profile they became the randominess index, and the amplitude of the modulating profile, insted for the chaotic one the user has to set the component values of a generic Chua's circuit, that is a non-linear circuit that for certain component values can work in double scroll chaotic mode and produce a chaotic waveform. The "Plot" button plots the time domain profile waveform in a Cartesian diagram according to the settings. Thus the user can verify the settings.

This tool lets the user the possibility to compare different modulation profiles all together. This feature is enabled toggling on this option, and selecting the different profiles. Enabling this feature will freeze the modulation parameters to the previous configurations.

Another feature is the possibility to perform a parametric simulation. To perform it, the user has to select the modulation profile and the parameter to sweep, that will change according to the chosen profile. Moreover, the user has to set the sweep range and the step size. If the user badly set some parameters, the tool will advert the user with some warning and error messages.

Carrier tone configuration

Within this last dialog the user has only to set the frequency and the amplitude of the carrier tone (a sinusoid wave) that will be spread spectrum modulated.

4.4 Structure of the algorithm

In order to make easier the readability of the MATLAB algorithm, an overview of its internal structure was considered to be exposed. Follows the skeleton of this algorithm. First of all, a re-initialization of the environment is mandatory in order to avoid an undesirable influence of previous calculations in the current one. Once the environment is ready, a complete list of definitions and parameters to be used along this algorithm is to be done.

Main parameters hereby described are: switching (carrier) and modulating frequencies (`fc` and `fm`), peak amplitudes of both signals (`ampc` and `ampm`), percentage of modulation (delta), peak deviation of the carrier frequency (`deltafc`), modulation index `mf`, bandwidth of the modulated waveform (bandwidth) from the Carson's rule and a final calculation of the sampling frequency `fsampling`. Other parameters are related to a specific profile, like the sawtooth parameter `s` for triangular modulation, multi slope coefficient `smulti` for multi-triangular modulation, concavity factor `k` for exponential profile, and so on.

A computation of the spectral components related to the modulated signal is carried out by using the MATLAB function `fft(f, N)`. A special mention has to be done now related to `fft`: to obtain the RMS values of the spectral components (`MOD_FFT`, in the algorithm), the following steps must be followed:

```
Y = fft(f, N)
Y = Y(1:1+N/2)
MOD\_FFT = (2/N)*abs(Y/sqrt(2))
```

where `Y(1)` represents the dc component and `Y(1+N/2)` contains the Nyquist component of the modulated waveform. Only the `1+N/2` first points contain the spectra information.

As exposed in Appendix [], the way of working corresponding to the FFT algorithm consists of selecting a truncation window and supposing that the data contained inside this window repeats itself indefinitely in time, thus becoming this window the period of the signal. If this truncation window is not selected in a proper way, for instance, choosing a window a little larger or shorter than the period of the original signal (or an integer value of it), a discontinuity is to be appear between the adjacent periods. This discontinuity in the time domain is also shown in the frequency domain, where fine theoretical spectral lines (representing the true harmonics of the signal) spread over a series of wider lobes. This effect is known in the technical literature as *spectral leakage*. These frequencies or lobes do not exist in the original signal; they are just the result of either an incorrect

application of the analysis methods or the own limitations of these methods. Regarding the Matlab algorithm developed, as the period of the modulated signal is perfectly known and equal to the modulating frequency f_m, a truncation window of $T_0 = 1/f_m$ is to be selected in order to avoid any problems and it is a condition included in the Matlab algorithm.

Afterwards, a graphical representation of the spectral content of the conductive EMI emissions is displayed.

4.5 Results

In this section some simulation results are submitted. All the shown results are displayed in a Cartesian diagram which is a graphical representation of the spectral content of the conductive EMI emissions. Generally, the x-axis of these Cartesian diagrams shows the frequency, while the y-axis shows the power of the EME in a logarithmic scale.

4.5.1 Buck converter's conducted EMI emissions results

In Figures 4.11, 4.12, 4.13 and 4.14 are shown some comparision between the spectral contents of the conducted EMI emissions from the same buck converter to battery, using different modulation profiles. All of these simulations are performed using the LISN test setup as in the CISPR 25 standard. These comparisions help us to detect the best profile to apply subsequently for our SSCG application.

In particular in Figure 4.11 the *triangular* and the *multi-triangular* were compared together also with the conductive EME resulting from a buck without spread spectrum modulation. From these is notable the big improvement that can be achieved with spread spectrum techniques. With the chosen modulation parameters there is about a $\approx 9\,dB$ reduction on the carrier tone window, but even a better gain can be achieved with other settings, in particular increasing the spreading percentage. The carrier tone switching frequency was chosen to be $f_c = 380\,kHz$, and the frequency spreading $\Delta f_c = 76\,kHz$ that with a center spreading give a spreading percentage of $\%_{SPREADING} = 40\%$.

In subsequent diagrams other modulation profiles are compared. In Figure 4.12 the result of a spread spectrum modulation from an *hershey-kiss* and from a *multi-triangular* profiles are shown. From different articles in literature the hershey-kiss profile seems to be the best modulation profile

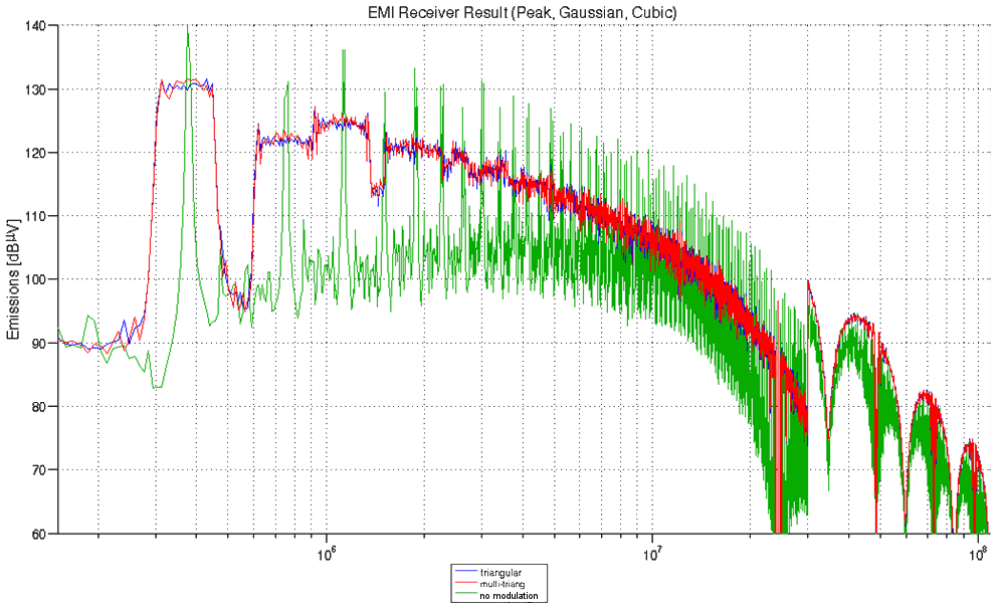


Figure 4.11: Conducted EMI emission simulation results, comparision between the triangular and multi-triangular profiles, against with a no modulation result.

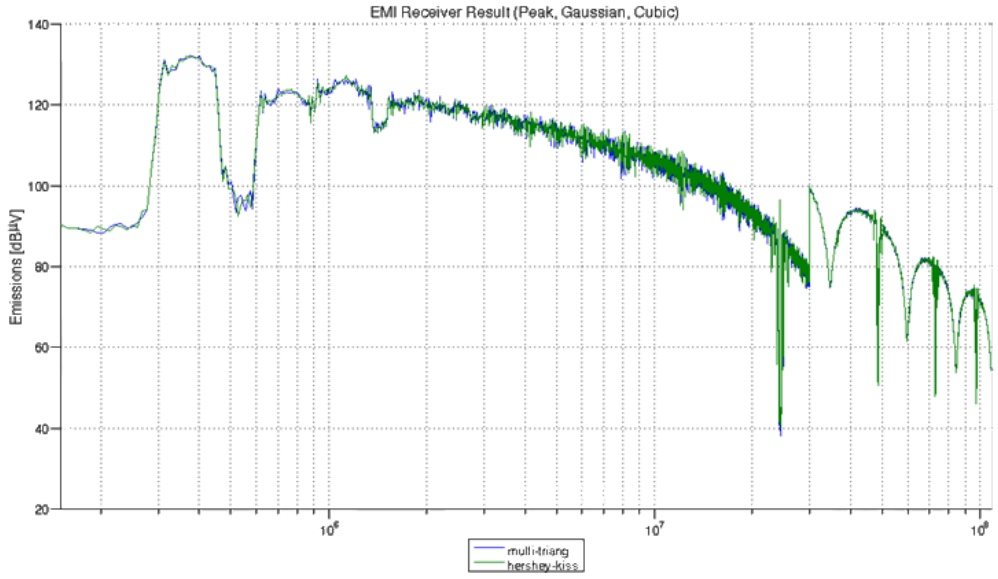


Figure 4.12: Conducted EMI emission simulation results, comparision between the multi-triangular and the hershey-kiss profiles.

to be applied, but it's hard to implement without a digital approach and requires a royalty payment to be used. The multi-triangular, instead is a new profile designed and developed in this thesis work

that try to be the best compromise between implementation feasibility and performances. As one can see from Figure 4.12 there only minimal differences between the two profiles, therefore, using the new multi-triangular profile in a SSCG application seems to be very promising.

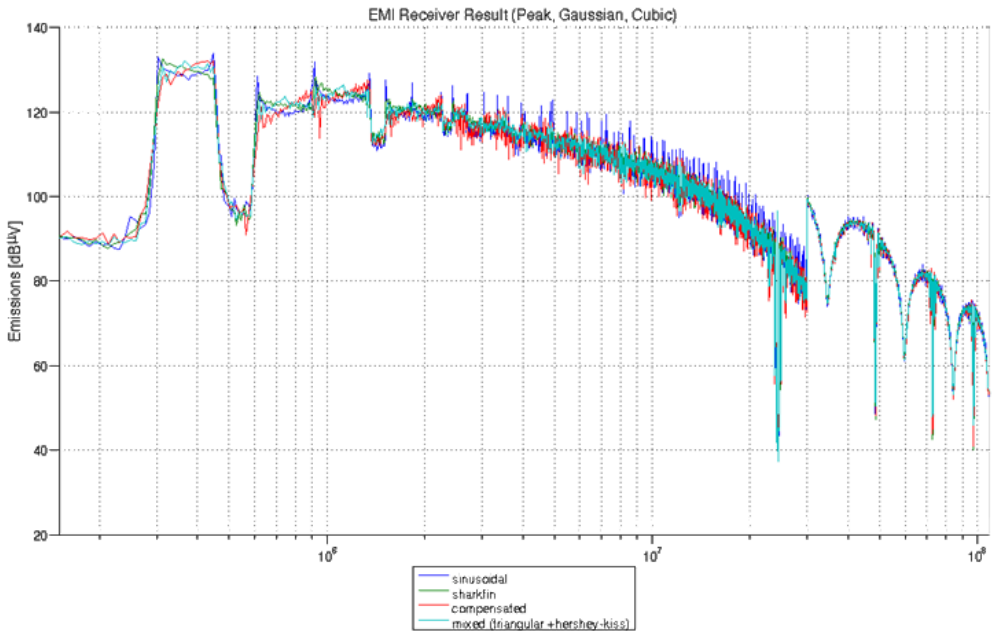


Figure 4.13: Conducted EMI emission simulation results, comparision between the sinusoidal, compensated, sharkfin and mixed profiles.

In Figure 4.13 the result of a spread spectrum modulation from several modulation profiles are shown. As expected from literature the *sinusoidal* profile give a spectral content of the conducted emissions after the modulation with two peaks or horns in corrispondence of both boundaries of the spreading window. The *sharkfin* and the *compensated* profiles, instead present a growing spectral content in corrispondence, respectively, of the lower and the upper boundary of the spreading window. No one of these profiles gives a flat spreading window and thus a good EME reduction. In fact, the sinusoidal profile gives a concave shape, the compensated profile gives a spectral content that rises with the increasing of the frequency and finally the sharkfin profile gives a spectral content that rises with the frequency decreasing. For completeness and to demonstrate the tool's capacities, in Figure 4.13 also a mixed profile is shown. In this example the modulation profile is composed for half by a triangular profile, and for the other half by a hershey-kiss profile.

In Figure 4.14 the result of a spread spectrum modulation from a *pseudo-random* and from a *chaotic* profile are shown. As expected from literature the chaotic profile give a better spectral

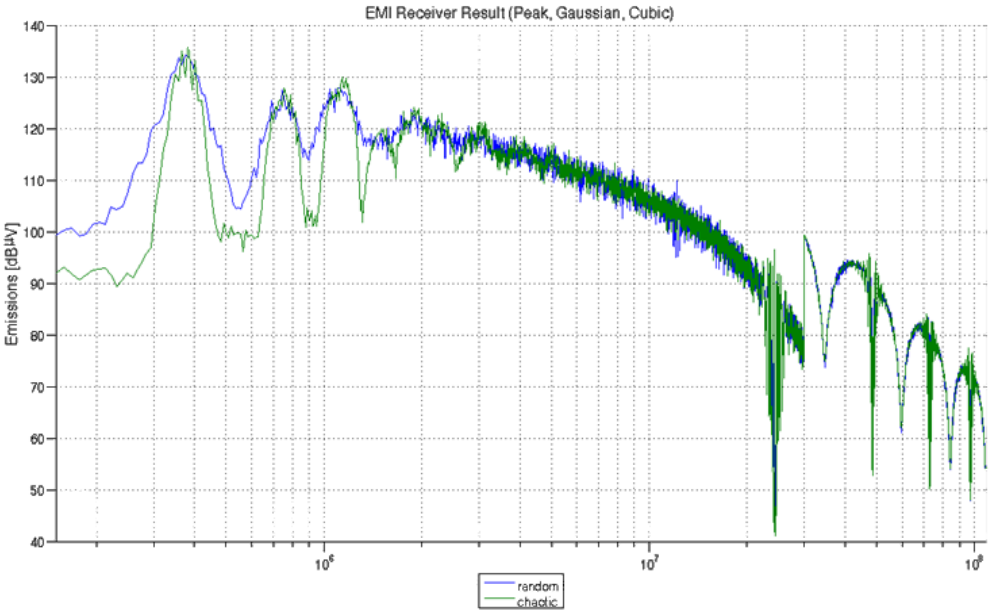


Figure 4.14: Conducted EMI emission simulation results, comparision between the chaotic and the pseudo-random profiles.

content at lower frequencies, compared to the randomic profile, but a lightly worse reduction over the carrier tone, moreover, the high frequency behaviour is practically the same. This result greatly matches with literature articles.

As mentioned above, this tool gives the capability to perform also parametric analysis. To represent the spectral content of conducted EMI emissions in a graphic way, sweeping a parameter, a 3-D plot Cartesian diagram is used. The x-axis of these Cartesian diagrams shows the frequency, the y-axis shows the power of the EME in a logarithmic scale, while the z-axis act for the sweeped parameter. As shown in Figures 4.15, 4.16 and 4.17 in addition to 3-D plot, in the displayed results there are also two 2-D Cartesian diagrams in the left side of the picture. In the first 2-D diagram the peak value of the EME power over the entire frequency range is plotted against the sweeped parameter, in this way the user can have a direct taste of the reduction of the conducted emissions in particular on the carrier tone. The second 2-D diagram is a standard plot of the spectral content of the conducted emission in correspondence of the half range value of the sweeped parameter.

In Figures 4.15 and 4.16 are shown the simulation results of a parametric analysis of the same parameter, that is the amount of frequency spreading. In Figure 4.15 a pseudo-random modulation profile is used, while in Figure 4.16 is employed a triangular profile.

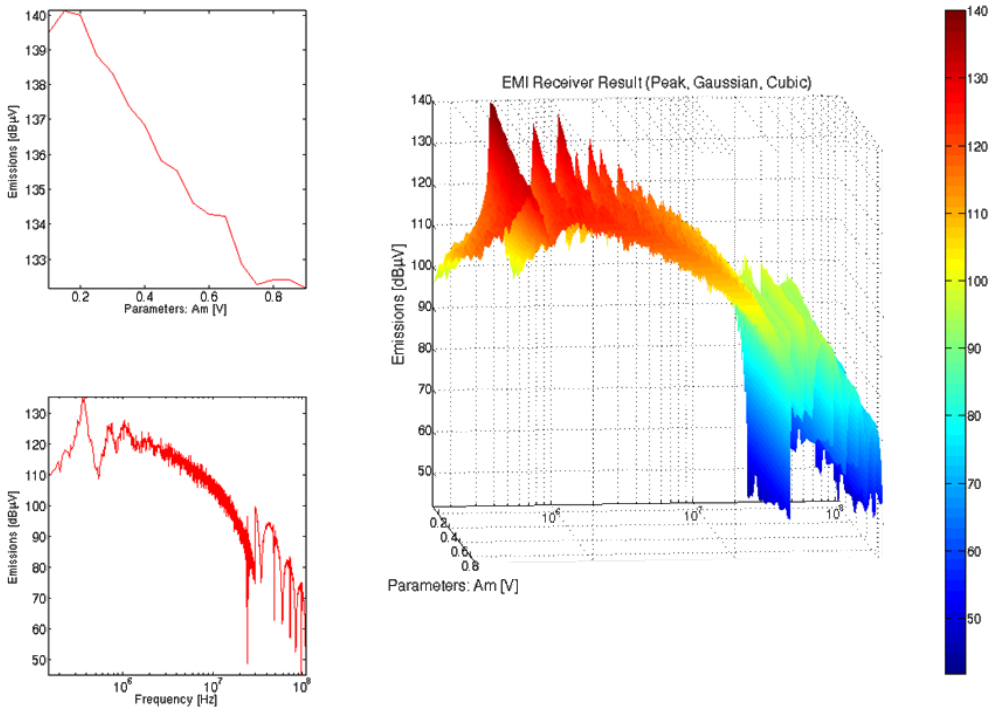


Figure 4.15: Conducted EMI emission parametric simulation results, pseudo-random profile, and the sweeped parameter is the spreading percentage.

The conducted emissions effective reduction is affected by several parameters, but the parameter that seems to have the more important influence is the modulation frequency f_m. This influence is due to the normatives, that impose a standard value for the resolution bandwith RBW of the EMI receiver or of the spectrum analyzer, that is generally $9\,kHz$ or $120\,kHz$. Figure 4.17 shows the results of a parametric analysis where the sweeped parameter is the modulation frequency f_m. As can be enlightned from the top 2-D plot the best value for f_m is precisely $9\,kHz$ that is the value of the standard RBW of measurement instument. This result was expected, also through some theoretical considerations. In particular it is well known that with a fixed spreading percentuage, that decreasing the modulation frequency in a spread spectrum modulation will create an increasing number of sub-harmonics in the spreading window. As the number of sub-harmonics increase as the power of the original tone will be splitted and spreaded, therefore the peak value of the envelope of the spreading window will decrease (see also Figure 4.25). This increase of the number of sub-harmonics would leads to a decrease of the space between the different sub-harmonic tones, in this way also a growing number of sub-harmonics would fall into the measurement RBW,

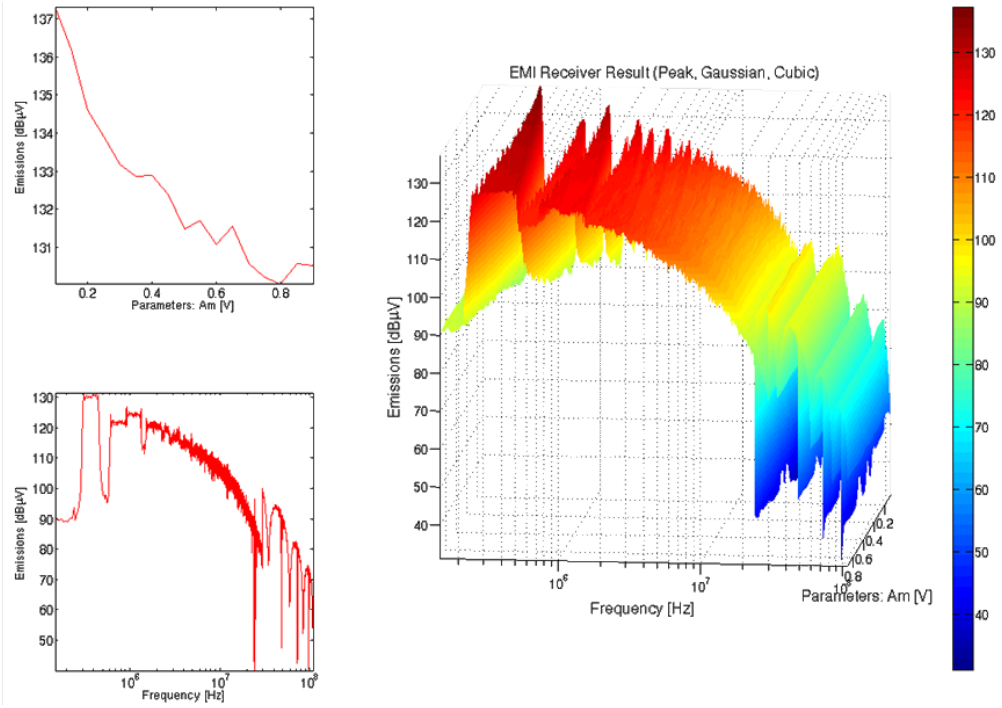


Figure 4.16: Conducted EMI emission parametric simulation results, triangular profile, and the sweeped parameter is the spreading percentage.

and therefore the measured result would fade the real enhancement of the conducted emissions reduction. In conclusion, we expected that the best EME reduction, can be achieved just with the minimum modulation frequency at which only a single tone falls into the measurement instrument's RBW, that is precisely $f_m = RBW = 9\,kHz$.

All the diagrams show above were the results of simulations with a LISN test setup as indicated in the CISPR 25 standard. In Figure 4.18 is shown the comparision of the spectral content of the conducted EMI emissions from the same buck converter to the output, using two different modulation profiles. These simulations are currently performed using the $150\,\Omega$ direct method as in the IEC 61967-4 standard. The compared modulation profiles are the triangular and the compensated. Can be noted that with the previous LISN test setup the triangular profile shown a very flatten spectrum inside the spreading window, instead the compensated profile gives a spectral content that rises with the increasing of the frequency. Therefore, with the LISN test setup the triangular profile shows a better behaviour than compensated profile. Now, applying the $150\,\Omega$ direct method to the output, can be appreciated that is the compensated profile that shows the

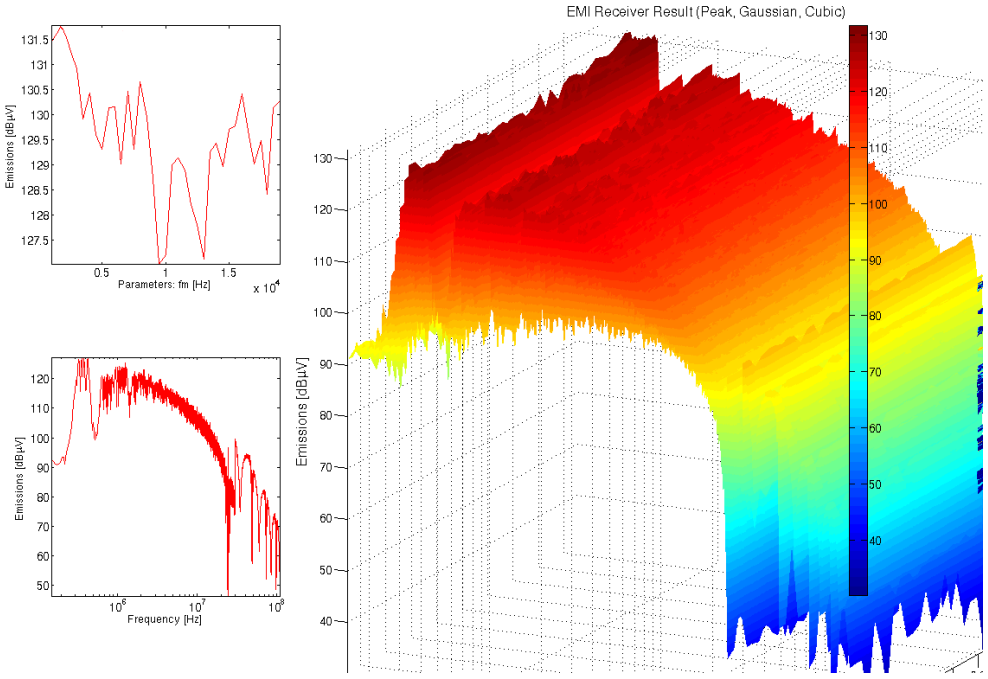


Figure 4.17: Conducted EMI emission parametric simulation results, triangular profile, and the sweeped parameter is the modulation frequency f_m.

flattest spectral content over the spreading window. The triangular profile, instead gives a spectral content that rises with the frequency decreasing, and therefore a worse behaviour, as we expected from literature []. This is the so called *tilt effect*.

4.5.2 Spectral content of a spread spectrum modulated carrier tone

Up to now were presented only simulation results performed using the second or the third sub-programs that compose this Matlab tool. In this subsection are shown, instead, simulation results performed using the fourth sub-program. Simulations performed using this tool part are really fast, also parametric simulations with a low step size are performed in few seconds. The simulation results aren't a conducted EMI emission analysis over the whole spectrum covered by automotive EMC normatives, but only a frequency analysis of the spectral content of a tone after a spread spectrum modulation. Therefore the displayed frequency range is limited only to the frequecies near the carrier tone. Moreover, this methodology, that is performing a spread spectrum modulation by a simple frequency modulation of a single tone and make a direct frequency analysis of the result, is very ideal and don't take into account several non-idealities, so the result doesn't match with a

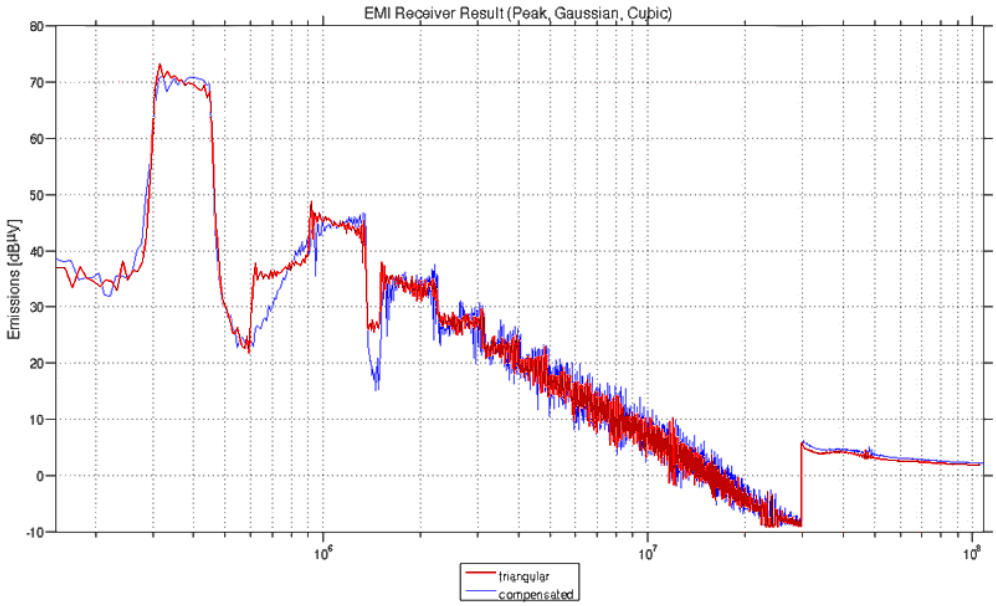


Figure 4.18: Conducted EMI emission simulation results, 150Ω method, comparision between compensated and triangular profile.

practical SSCG system. Despite this, these results are helpful to better understand how a spread spectrum modulation works. In particular toggling off the spectrum analyzer emulation, the user can see the creation of the differents sub-harmonics after the modulation.

In Figures 4.19 and 4.20 are shown some comparision between the spectral contents of a spread spectrum modulated carrier tone, using different modulation profiles, that are sinusoidal, triangular, hershey-kiss. In Figure 4.19 the spectrum analyzer emulation is toggled off, while, in Figure 4.20 it is enabled.

Side-band harmonics resulting from modulation show a different aspect or outline depending on the profile. For a sinusoidal modulation, side-band harmonics tend to concentrate themselves around the two peaks defining the side-band harmonics bandwidth as the modulation index m_f gets higher, which results in a shape of the modulation spectrum envelope showing two peaks at both ends of the bandwidth while the envelope gets a larger concavity between these two peaks. In the case of a triangular modulation profile, envelope of the side-band harmonics corresponds to a nearly flat, straight horizontal line, very opposite to the sinusoidal modulation behaviour, characterised by a concavity between two extreme peaks and to the case of an hershey-kiss modulation profile, where side-band harmonics resulting from the modulation process tend to concentrate around the

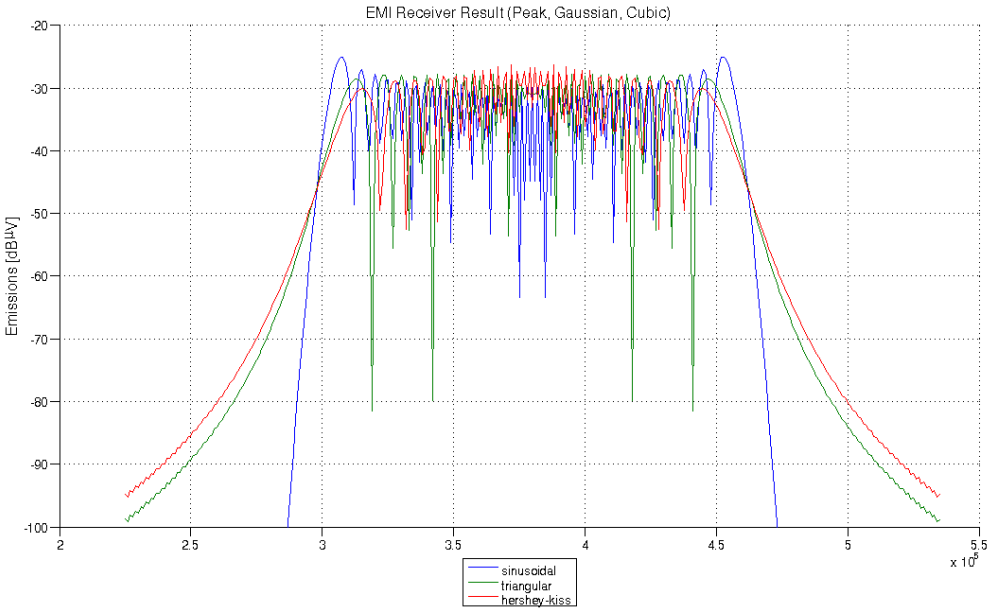


Figure 4.19: Carrier simulation results, comparision between sinusoidal, triangular and hershey-kiss profiles with Spectrum Analyzer emulation toggled off.

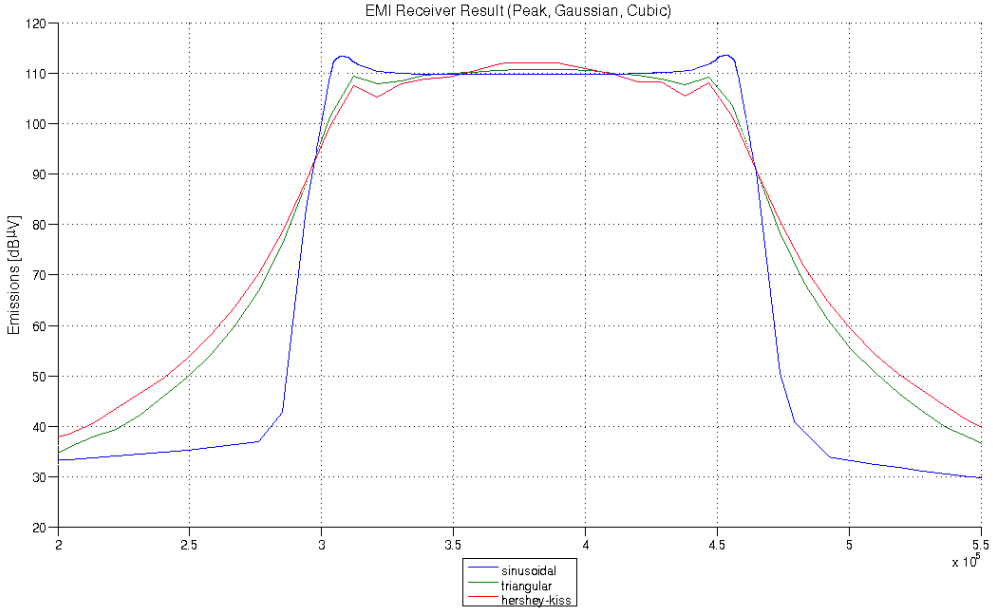


Figure 4.20: Carrier simulation results, comparision between sinusoidal, triangular and hershey-kiss profiles with Spectrum Analyzer emulation toggled on.

carrier frequency, decreasing in amplitude as the side-band harmonic order separates itself from the carrier frequency.

It is concluded then that modulation profiles, or trams of them, which are inscribed inside the triangular base, tend to concentrate the side-band harmonics around the carrier frequency, thus giving a peak aspect to the spectra distribution resulting from the frequency modulation process, as displayed in Figures 4.19 and 4.20. In the same way, any modulation profiles, or trams of them, which stay outside the triangular base tend to concentrate the side-band harmonics not at the carrier frequency but in the opposite sides, that is, a concentration around the two frequencies defining the bandwidth resulting from the modulation process, as shown in Figures 4.19 and 4.20.

Therefore, considering a triangular profile as the reference base, profiles plotted outside the triangular profile limits (e.g., sinusoidal) seems to concentrate harmonics around the two peaks defining the bandwidth; in the same way, profiles plotted inside the reference triangular profile (e.g., hershey-kiss) concentrate harmonics around the carrier frequency.

From the comparison of these three different modulation profiles and considering the global behaviour of the modulation, the most important parameter is peak value of the envelope. It provides a very useful information because of its global characteristic: the maximum amplitude (respect to the non-modulated carrier frequency) along the whole spectrum distribution as a result of a frequency modulation, that is, all harmonic amplitudes will be under this value. Then, a flat harmonic distribution is the most profitable and, therefore, a triangular modulation profile is the most suitable for any application with these characteristics. Sinusoidal profile shows the worst behaviour because of the horns shape of the side-band harmonic distribution.

As just explained, the triangular modulation profile is the most suitable for any application. It seems to be that modulation profiles consisting of straight lines, that is, constant slopes during the modulating period are to produce a flat distribution of the side-band harmonics. Things change as one try to implement a triangular spread spectrum modulation, because the frequency produced by a SSCG isn't able to exactly track the modulation profile, due to the limitated bandwith of the spread spectrum clock generator system. This happens in particular on the vertex of the profile, the resulting behaviour is like a filtering effect, therefore the frequency generated changes more similarly to a sinusoidal shape. This will cause that also in a triangular modulation profile, side-band harmonics will tend to concentrate themselves around the two peaks defining the side-band harmonics bandwidth. Also the hershey-kiss profile is affected by this concentration effect of side-band harmonics around the two peaks, but its particular profile shape compensate it, because

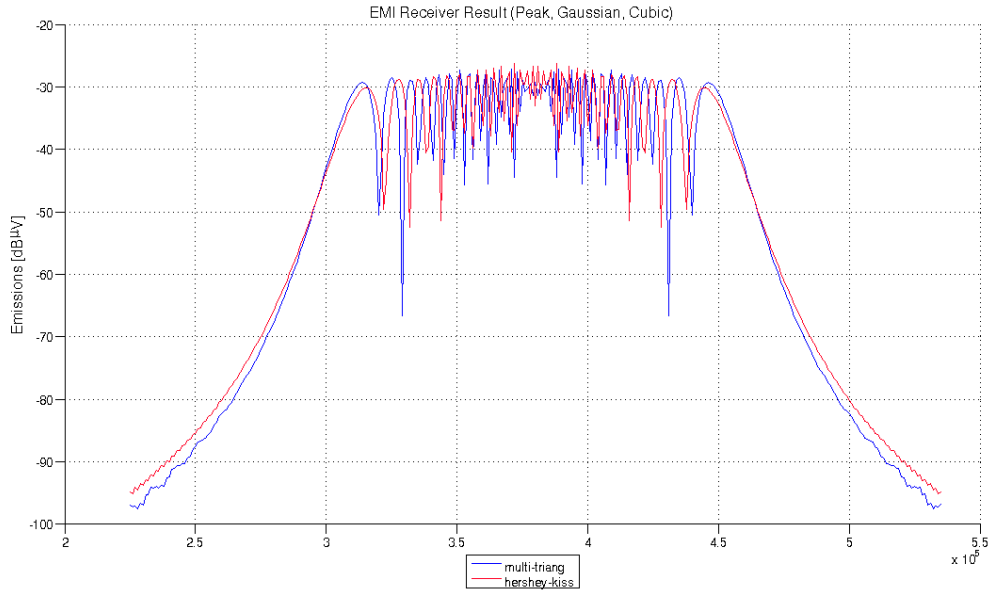


Figure 4.21: Carrier simulation results, comparision between multi-triangular and hershey-kiss profiles with Spectrum Analyzer emulation toggled off.

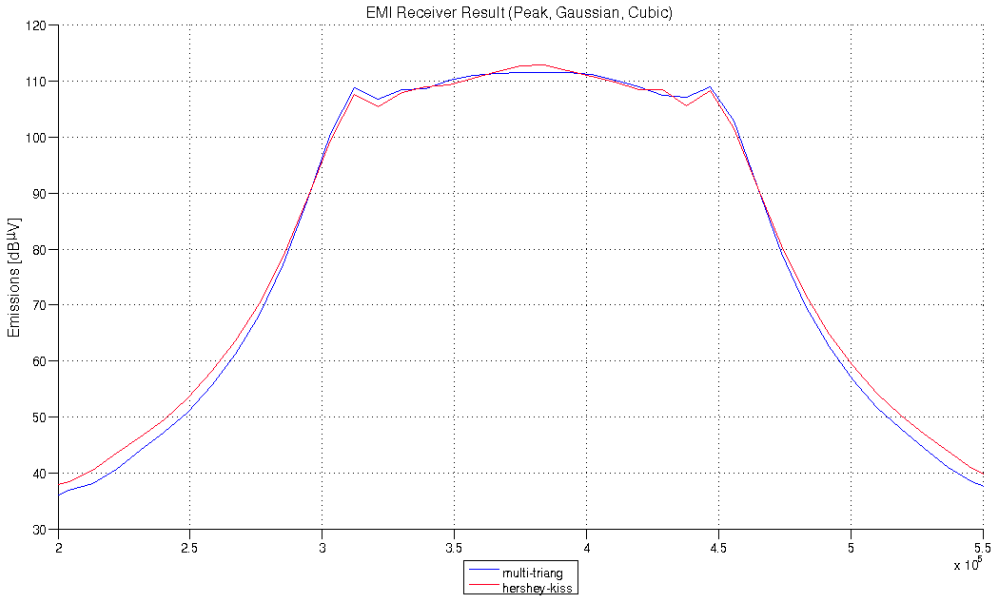


Figure 4.22: Carrier simulation results, comparision between multi-triangular and hershey-kiss profiles with Spectrum Analyzer emulation toggled on.

as already explained intrinsically tends to concentrate its side-band harmonics around the carrier frequency. Therefore the final result is a perfect flat spectrum distribution shape. For these reasons

an hershey-kiss modulation profile is the most suitable for many applications, in particular those in which the bandwith of the SSCG system is quite limitated.

Taking into account the implementation problems of an hershey-kiss modulation profile, we conceptualized the multi-triangular profile. We make a comparision between the two profiles also using this tool sub-program. As one can see from Figure 4.21 and from Figure 4.22 there only minimal differences between the two profiles, therefore, we have the re-proof that using the new multi-triangular profile in a SSCG application seems to be very promising.

In Figure 4.23 and Figure 4.24 are shown the simulation results of a parametric analysis of the same parameter, that is thesawtooth parameter s. In Figure 4.23 the spectrum analyzer emulation is toggled off, while, in Figure 4.24 it is enabled.

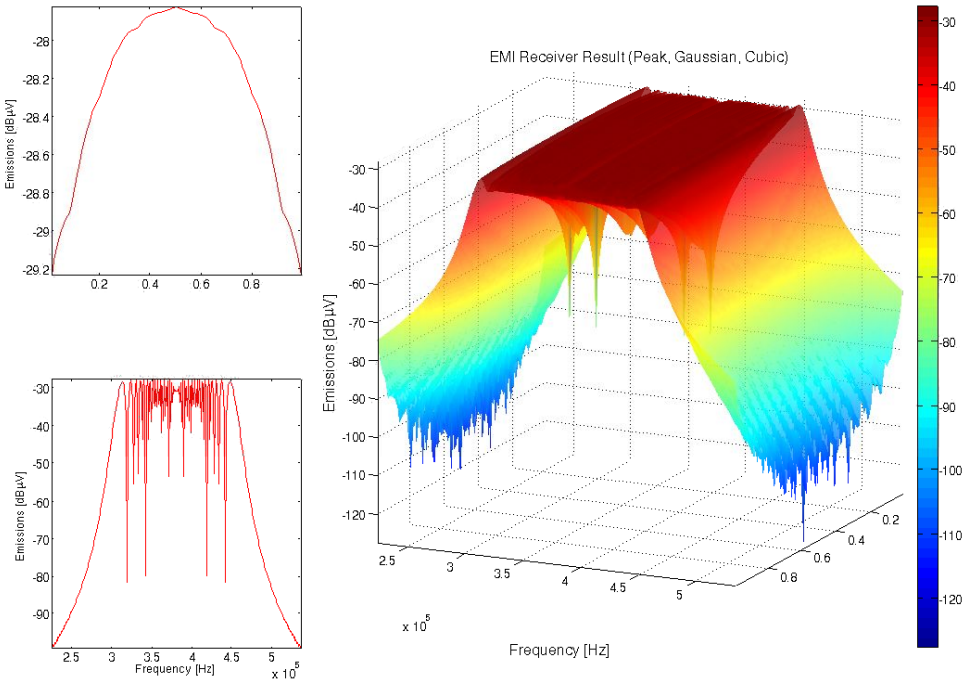


Figure 4.23: Parametric carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled off and sweeped parameter is the sawtooth slope s.

As one can see from Figure 4.23, the triangular modulation profile produces a complete flat spectrum distribution shape, independently on the sawtooth parameter s, but with harmonic amplitudes concentrated in a narrow range of variation for vertex index $s \neq 0.5$. As is evidenced by the top-left 2-D plot, the peak evelope value has its maximum for $s = 0.5$, therefore from this simulation result seems that a sawtooth profile is more suitable than a triangular profile with

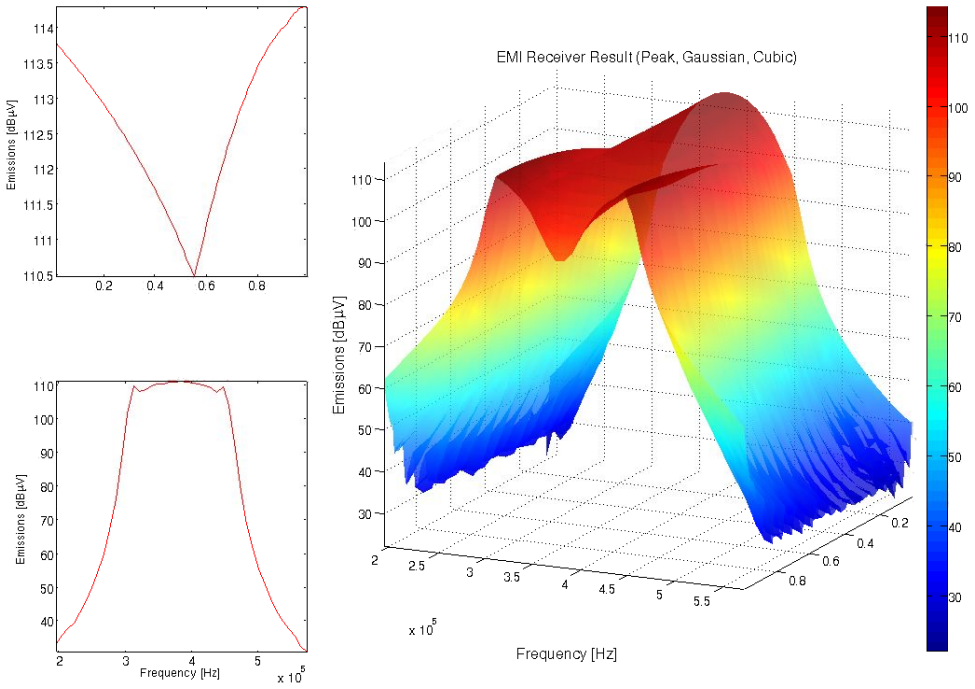


Figure 4.24: Parametric Carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled on and sweeped parameter is the sawtooth slope s.

$s = 0.5$. Indeed performing the same simulation, but toggling on the spectrum analyzer emulation, the result changes drastically. The RBW (Resolution Bandwidth) and measure mode (peak, quasy-peak and average) of spectrum analyzers are responsible for giving different measured values of the same physical fact of modulation. In fact, simulating a spectral content measurement like in the EMC standards, the triangular modulation profile produces a complete flat spectrum distribution shape, only for $s \approx 0.5$, as can be seen from Figure 4.24. As evidenced by Figure 4.24 for values of parameter s that tends to 1 the side-band harmonics will tend to concentrate themselves around the two peaks defining the side-band harmonics bandwidth, conversely as s tends to 0 the side-band harmonics will tend to concentrate themselves around the carrier frequency.

The RBW (Resolution Bandwidth) and measure mode (peak, quasy-peak and average) of spectrum analyzers are responsible for giving different measured values of the same physical fact of modulation; as a general asseveration, the larger the selected RBW, the higher the obtained measure because more side-band harmonics can fall inside this RBW, adding their amplitudes. Figure 4.26 shows the results of a parametric analysis where the sweeped parameter is the modulation frequency f_m. As can be enlightned from the top 2-D plot the best value for f_m is precisely $9\,kHz$ that is the

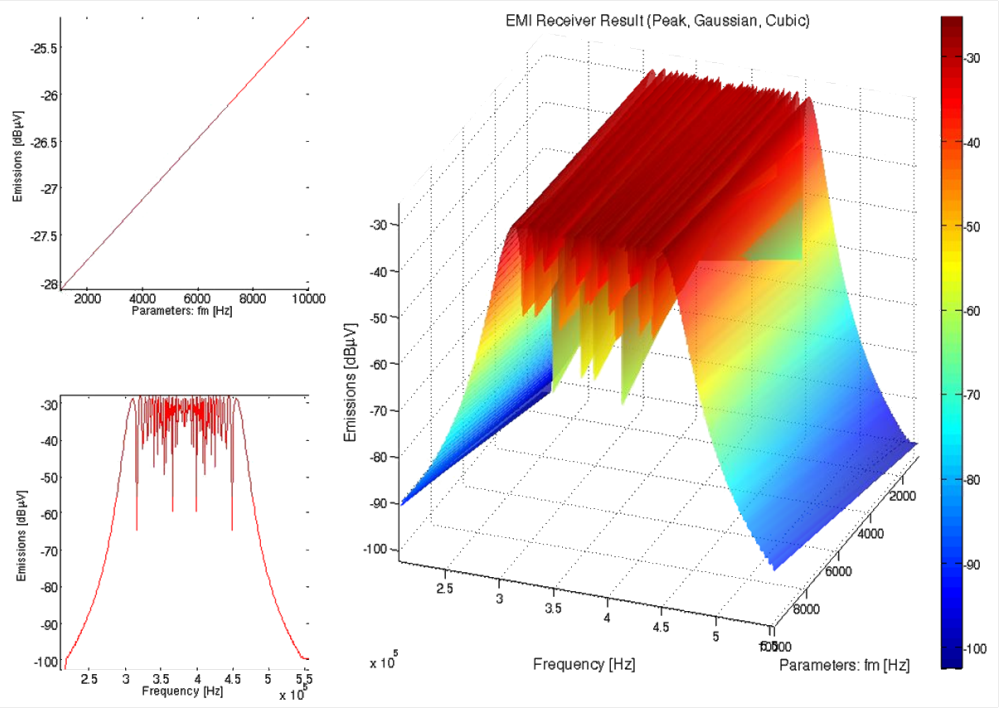


Figure 4.25: Parametric Carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled off and sweeped parameter is the modulation frequency f_m.

value of the standard RBW of measurement instument. This result was expected and confirm the previous result in Figure 4.17. If the spectrum analyzer emulation is toggled off, the peak value of the spectral evelope decreases as do the f_m, as shown in Figure 4.25.

In Figures 4.27 and 4.28 are shown the simulation results of a parametric analysis of the same parameter, that is the amount of frequency spreading, with the spectrum analyzer emulation disabled. In Figure 4.27 a sinusoidal modulation profile is used, while in Figure 4.28 is employed a triangular profile. For every modulation profile, amplitude reduction of the side-band harmonics resulting from the modulation process only depends on the modulation index amount of frequency spreading. The sinuoidal profile gives a better behaviour on the spectral content for frequencies outside the side-band harmonics window, than the triangular profile, but a gives a worse peak envelope value for any amount of frequency spreading. For completeness, in Figure 4.29, is shown the simulation results of a parametric analysis of the same parameter (the amount of frequency spreading), with the spectrum analyzer emulation enabled.

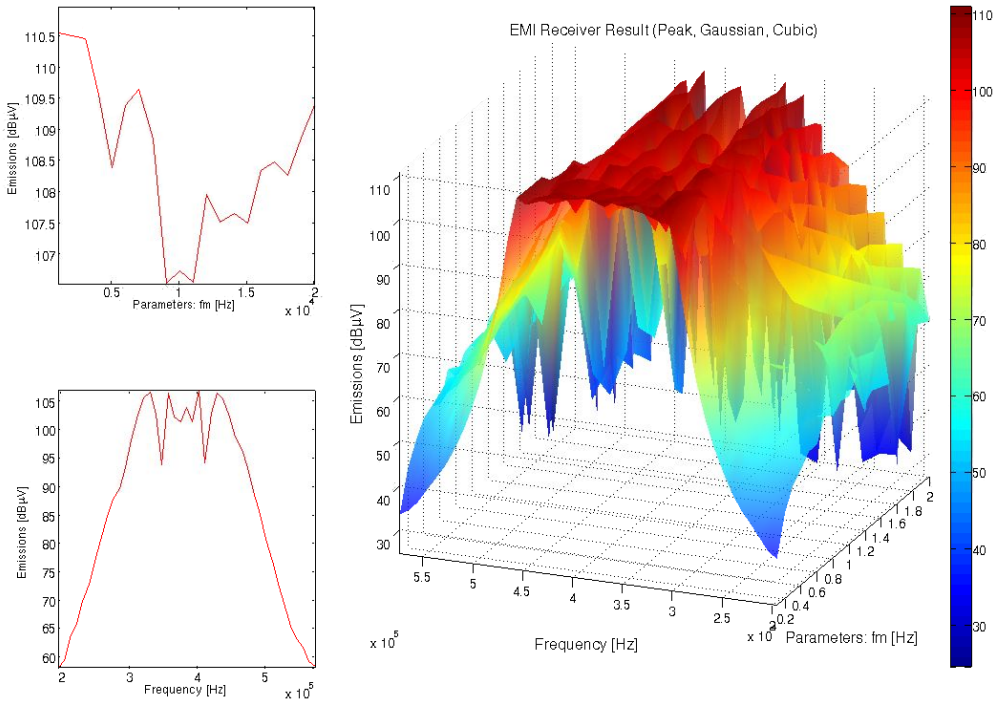


Figure 4.26: Parametric Carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled on and sweeped parameter is the modulation frequency f_m.

4.6 Next steps

The Spread Spectrum Matlab Tool realized during this thesis work, seems to have great possibilities and capabilities, moreover, it can be still improved and above all many new features can be added. Some of these are listed below:

- in order to make more real the final result, add several non idealities to the simulation, such as:
  - modulation profile distortions
  - amplitude noise
  - jitter and phase noise
  - limited bandwith of the SSCG system
  - non-linear voltage-frequency characteristic of the internal VCO
- add other modulation profiles and the multy-cycle modulation;

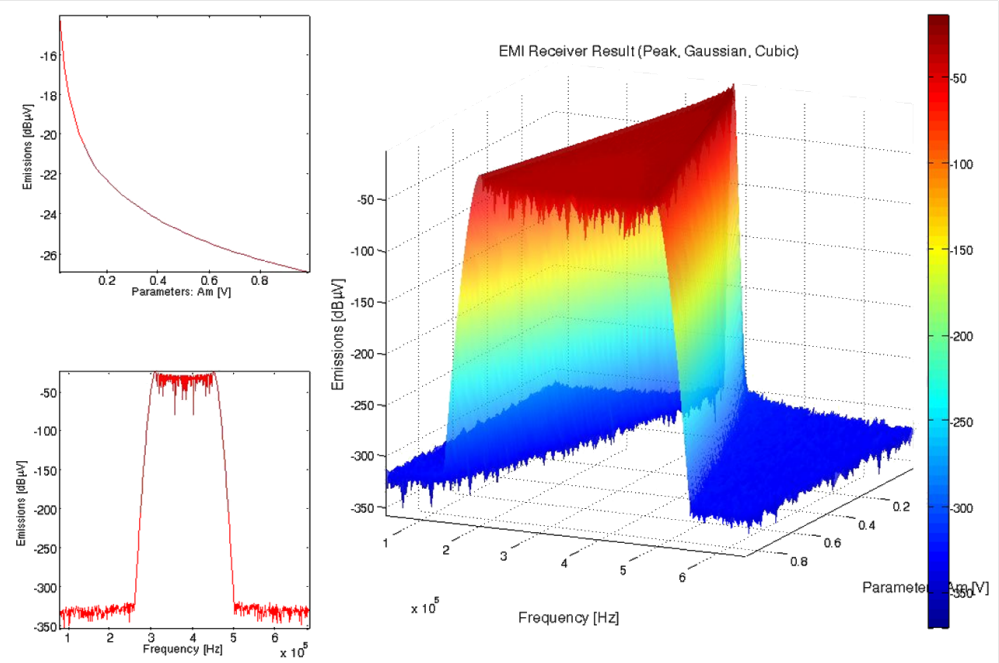


Figure 4.27: Parametric carrier simulation results, sinusoidal profile with Spectrum Analyzer emulation toggled off and sweeped parameter is the spreading percentage.

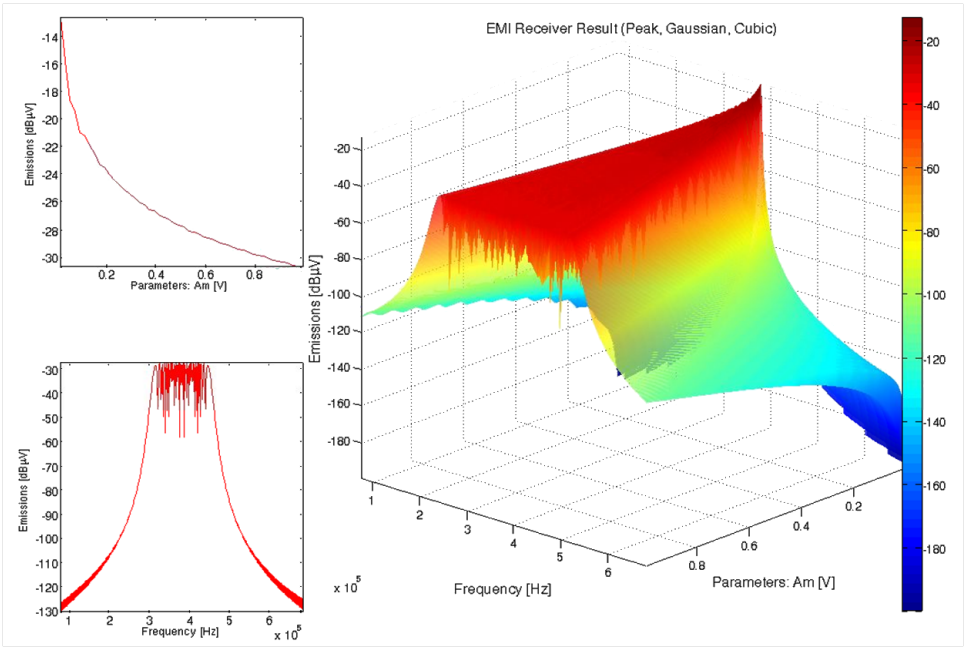


Figure 4.28: Parametric Carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled off and sweeped parameter is the spreading percentage.

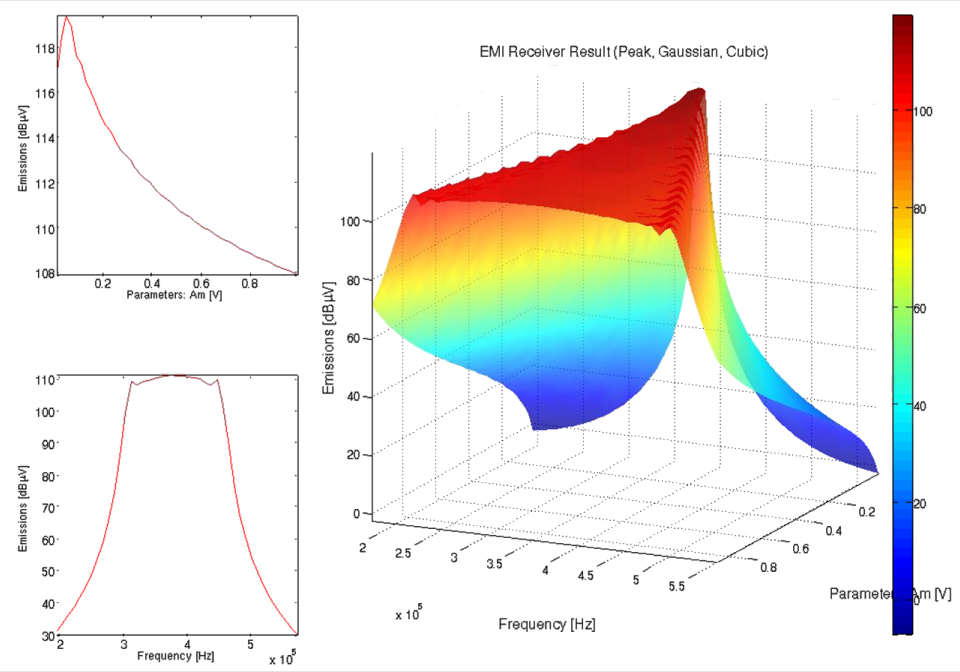


Figure 4.29: Parametric Carrier simulation results, triangular profile with Spectrum Analyzer emulation toggled on and sweeped parameter is the spreading percentage.

- add other tipologies of switching circuit:
  - Switching Mode Power Supplies (Boost, Buck-Boost, etc...)
  - Switched Capacitor Circuits
  - Charge Pumps

4.7 Conclusions

We build a user friendly tool that lets the user "to play" with all the Spread Spectrum Modulation techniques in different test measurements setup. With the help of this tool can be achieved a better understanding of theoretical and real benefits of Spread Spectrum Modulation techniques.

We have verify the techniques available in literature and matched their results. In addition we have benchmarked the reduction of conducted EMI emissions from a generic Switched Mode Power Supply that these techniques can provide, that would be in the $6 \div 16\,dB$ range.

As already explained even if there is a reduction in the conducted EMI emissions, by ap-

plying Spread Spectrum Modulation, these enhancement can be faded by normative and by the standardized test measurement setups. In fact, as one can see using this tool, the final reduction on the conductive EME are very dependent by the modulation parameters and by the normative parameters of the measurement instrument, like the resolution bandwith and detector's type in a scanning receiver.

Chapter 5

Spread Spectrum Clock Generator concept

5.1 Technology considerations

Integrated circuits show a significant growth potential, not only in the traditional segments as information and signal processing but also in the fields of power electronics and sensor systems. The integration of power stages, and analog and digital blocks on a single chip (*Smart Power IC*) offers reliability improvements and reduces electromagnetic interference, the number of components, as well as space and weight. It is therefore an excellent approach for cost savings as increasingly required by today's market. One of the important areas for smart power ICs is the automotive industry, where higher safety standards, tighter environmental legislation and the demand for increasing comfort on board lead to a constantly increasing amount of microelectronic components built into modern cars.

Smart Power Technologies offer the integration of analog and digital circuits combined with the power stages on the same chip. The smart part of the smart power circuits adds diagnostic and protection functions to the power transistors. This increases the robustness and reliability of power drivers for automotive applications. The application range goes from protected low side, high side and bridge driver configurations to complete smart power system ICs. There are many automotive applications which can use these smart power integrated circuits. As an example for automotive applications there exist intelligent power switches for controlling the ABS-braking system, system power chips for airbag control, for engine management of the car, switched mode supplies, intelligent switching of all lights and so on. Additional to normal functionality the smart power circuits must provide highest reliability requirements and robust operation and has to withstand some hostile environment conditions like high voltage spikes, a very extended temperature range, short circuit, overvoltage conditions, EMI pollution, while not being a source of EMI by themselves.

5.1.1 Smart Power Technology (SPT)

At the beginning power ICs were implemented in pure bipolar technologies. As the power needed and available per chip increased and the switching functions became more and more important, DMOS power transistor helped to overcome the bipolar limitations because of its fast switching characteristic and the possibility to control the device by voltage rather than current. As designers wanted to combine power devices with an ever increasing amount of analog and digital processing, smart power or BCD (bipolar-CMOS-DMOS) processes emerged by combining bipolar technologies with CMOS and DMOS power devices. Clearly the combined BCD process gives circuit designers the possibility of choosing the optimal technology for each circuit function: bipolar is the first choice for linear functions where high precision and low offsets are required; CMOS is best for complex analog and digital signal functions because of its high density and power DMOS is ideal for power stages.

Since it was first introduced in 1986, mixed bipolar-CMOS-DMOS smart power technology has evolved rapidly, extending voltage capability and integrating highly complex subsystems on single chips containing thousands of transistors. The introduction of shrunk BCD technologies increases the amount of logic that can be integrated at a reasonable cost. This improvement in microlithography also allows an improvement in current density of the power DMOS transistors.

Several BCD technologies have been generated and updated in order to fulfill the requirements of many specific applications. In the field of applications below $50\,V$, BCD evolution has been driven by the need to integrate on the same chip more and more complex and diversified functions, to the point that today even non-volatile memories are offered. Besides, the density of integration achieved makes it possible to adopt digital design approaches such as integrating microcontrollers, to realize optimal driving solutions to improve performance. In a time of fast technology advancement this approach represents an answer to ever increasing market demand for System on Silicon devices where both the signal processing part and power actuators can be combined.

In parallel to the race towards the minimum lithography reduction to achieve large complexity, other branches with different requirements have developed. For example in the applications up to very high voltages the primary efforts have been addressed to make possible a reliable coexistence on the same chip of low voltage control circuits and high voltage DMOS stages. Other fields, mainly automotive, have required dedicated BCD approaches to satisfy the demand to provide robust

power elements with simplified control sections to guarantee high quality and reliability in harsh application environment at no cost penalty.

5.1.2 SPT classification

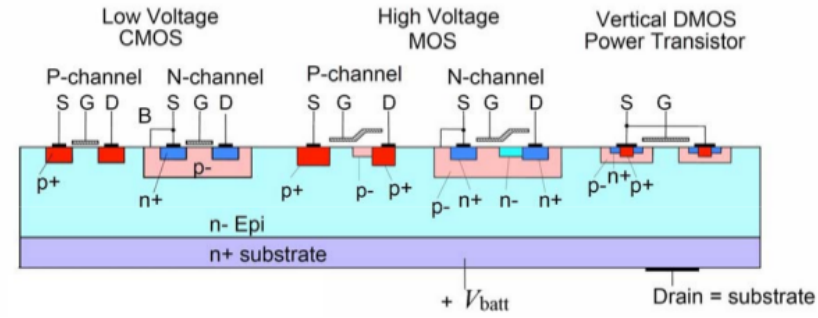
The design of power ICs is not as mechanical as low power ICs. The main difficulty lies in avoiding unwanted interaction between power sections and signal sections. Another non-trivial complication is that there is a difference between designing a circuit which works and designing one that can be produced and tested in large volumes. Often, in fact, the development of testing hardware and software can be more troublesome than the design of the IC itself. Smart power tecnologies can be conveniently classified according to the isolation technique. This because, the different components inside a single chip condivide the same die, and therefore, they should be isolated each other to work properly. Three basic systems are adopted:

- *Self isolation:* the simplest way to obtain isolation, but is not as flexible as the other way of isolation. This technique requires that the components share some pins, and the isolation of neighboring components is only done by applying the right voltages to the components in respect to the substrate or well connection. Furthermore the parasitic effects introduced by using this kind of isolation are not negligible.

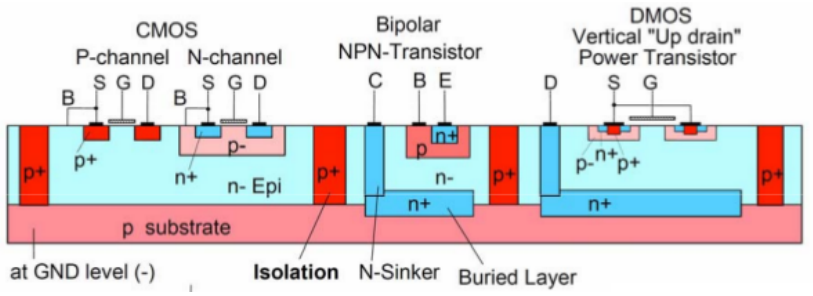
- *Junction isolation:* the most widely used because of its good compromise between low cost and good versatility. A reverse biased PN-junction is used as an insulator between different components. Usually an N-epitaxial layer is grown on a P-substrate, and a P-diffusion can insulate the two different N-silicon islands, realized by diffusing P-regions through the entire depth of the N-type epitaxial layer. Nevertheless, in junction-isolated ICs certain bias conditions can result in minority and majority carrier injection into the substrate.

- *Dielectric isolation:* based on silicon oxide used as an insulator to create separate silicon islands. This allows a very low leakage current, reduction in size of the high voltage components and low parasitic capacitance to substrate. The drawback is the complexity of realization and the poor heat conductivity of the silicon oxide that limits the number of power devices per area unit. To insert a buried oxide layer inside a chip below the active devices requires a more complex and costly manufacturing process. Due to this Silicon

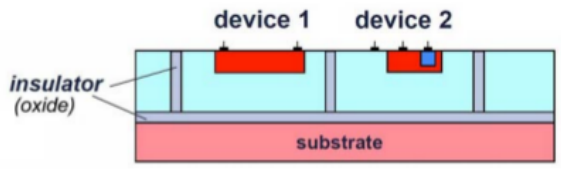
on Insulator (SOI) is an expensive technology and therefore not the mainstream for smart power circuits. A variant of the dielectric isolation is the Deep Trench Isolation (DTI) which uses oxide to separate the components in lateral direction but not against the substrate, see Figure 5.1(d). The advantage here is no limitation in heat transfer for power devices and a chip area reduction for high voltage components, because the oxide filled trenches are significant smaller then the p-diffusion areas used in a junction isolation process. But bulk parasitic problems and leakage currents against substrate are similar as in junction isolation technologies.



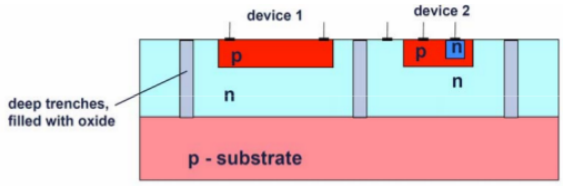
(a)



(b)



(c)



(d)

Figure 5.1: (a) Cross section of a self isolation smart power technology. (b) Cross section of a junction isolated smart power technology (BCD). (c) Dielectric isolation, Silicon on Insulator (SOI). (d) Partial dielectric isolation, Deep Trench Isolation (DTI)

Integrated circuit fabrication technologies that combine bipolar, CMOS and power DMOS structures on the same chip have had a significant impact on *smart power* integrated circuit design. Thanks to the use of the junction and dielectric isolation approachs it is possible to integrate into a single chip any number of DMOS power transistors interconnected in any way. Since the dissipation of power DMOS stages in switch mode operation is very low it is possible to produce ICs capable of delivering substantial power to the load without the usual heatsinks, cooling fans and so on. Unlike bipolar power transistors, power DMOS devices need no driving current in DC conditions and operate very efficiently both in DC operation because of the low on-resistance, and in fast switching operations. Moreover, because it permits the integration of high-density CMOS, that allows signal level circuits of LSI complexity, and multiple DMOS power stages, the traditional constraints on complexity are removed and circuits containing complete subsystems have been produced, so, the technological limit on complexity is beyond the complexity of a wide range of end products. Also, this low dissipation can be exploited to increase the amount of useful power that can be achieved with a given package.

There is a tendency to use digital techniques whenever possible because it allows a greater reduction in area. The possibility of having dense digital circuits on a BCD chip allows designers power IC designers to take advantage of this trend. At present the capabilities of the technology in terms of complexity generally exceed the demands of system designers. Another important consideration is that LSI smart power devices will invariably be full custom and developed for a specific end use.

5.1.3 Tecnology adopted

Depending on the partitioning of the system and the available technologies quite different solutions can be imagined. To use the most advanced, expensive technology may well lead to a technical perfect one chip solution, but eventually will not be the best economic one.

In the preliminary stage of this thesis work, we need to choose the SPT technology among those avaiable to us. In particular the choice was between an "old" but consolidated and robust junction isolation BCD technology with a minimum channel length for digital MOS transistor of $L_{min} = 0.8\mu m$, and a very new trench isolation BCD technology with a minimum channel length of $L_{min} = 130nm$.

In a Spread Spectrum Clock Generation (SSCG) application, the principal aim is to apply the spread spectrum modulation that can achieve the best final conducted EME reduction performances. In this regard, in the previous step we have investigated, by using the *Spread Spectrum Matlab Tool* (just presented in Chapter 4), several modulation parameters and modulation profiles. The investigated modulation profiles go from the simplest and most diffused *triangular* profile, to more complex modulation profiles, like the patented *hershey-kiss*. The effect on the conducted emissions final reduction was evaluated to be about $5-6\,dB\,\mu V$ from the best modulation profile to the worst profile.

However, if the profile to generate is composed by complex and non-linear curves, it is hard to develop the analogic circuit needed to generate the profile. Thus, there is the need of an analogic circuit if the profile is quite simple to generate (like a triangular waveform), otherwise, if a complex profile are adopted a digital approach is prefered. This would lead to a trade-off between the EME reduction and the circuit complexity, and so, also with the chip area and the final cost of the developed solution. In particular the choice between an analog and a digital approach have a big influence also on the most appropriate technology's choice, in fact the realization of a circuit solution with a large digital part would lead to adopt an high shrunk technology, instead of another technology with a larger minimum channel length, to avoid a chip area explosion. Moreover, the use of an high shrunk technology would also imply high production costs, due to the higher number of required process masks.

With these considerations in mind, our choice fell on the implementation of simple modulation profiles like the triangular, and to avoid complex profiles like the hershey-kiss, even if, it would carry better results and performances. Moreover, we choose to implemente a new modulation profile, that claims to be the junction point between triangular and herhey-kiss profiles, and the best trade-off between circuit complexity and performances. This new profile is, the so called, *multi-slope triangular* or *multi-triangular* profile. The implementation of this new profile needs only a simple analogic approach, in this way we can adopte a SPT technology with a minimum channel length of $L_{min} = 0.8\,\mu m$.

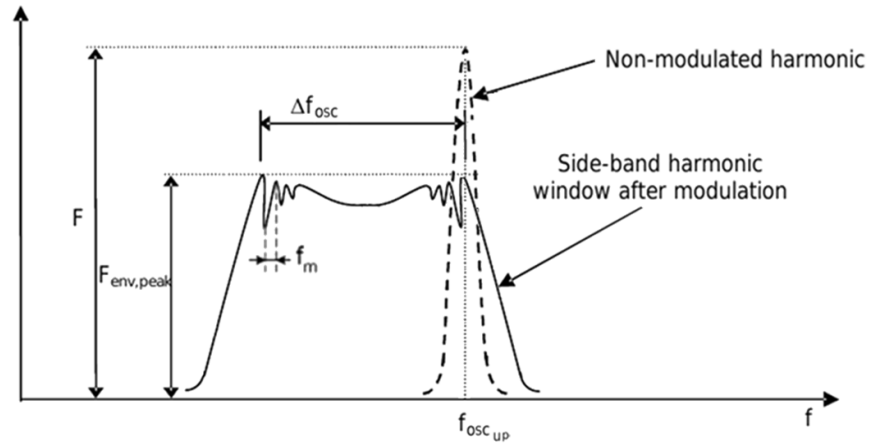


Figure 5.2: Down-spread modulation

5.2 Top concept structure

The aim is to realize an high precision, low power and easy to use oscillator with *spread spectrum frequency modulation* (SSFM) capability that can be activated and fully configurated by some additional external resistors.

The SSFM capability modulates the oscillator's frequency by a configurable periodic signal (whose frequency is set by an external resistor R_{FM}) to spread the oscillator's energy over a wide frequency band. As shown in Figure 5.2 the non-modulated harmonic at frequency $f_{osc_{UP}}$ is spreaded in a side-band harmonic window after the modulation. Each generated harmonics after the spreading have frequencies less than the initial non-modulated harmonic, this type of frequency modulation is called *down-spread modulation*. This spreading decreases the peak conducted electromagnetic emission level and improves electromagnetic compatibility (EMC) performance. The amount of frequency spreading is programmable by a single additional external resistor (R_{MOD}) and is disabled by removing it.

Output provide a rail-to-rail 50% duty cycle reference clock signal. The internal master oscillator frequency $f_{osc_{UP}}$ is set by a single external resistor (R_{SET}) and has a frequency range that can span from $640\,kHz$ to $2.56\,MHz$. In order to accommodate a wider output frequency range (from $40\,kHz$ to $2.56\,MHz$), also a programmable frequency divider (divide by 1, 4 or 16) is included.

5.2.1 Targets and Features

Below the reader can find a brief listate, like a little datasheet, of the main specifications and features we plain to implement in our solution:

- Standalone Spread Spectrum Clock Generator Chip
- Application: Automotive Switching Power Supply Clock Reference
- Operates from a single $2.7\,V$ to $5.5\,V$ supply
- Down Spread Spectrum Frequency Modulation for Improved EMC Performance
- $40\,kHz$ to $2.56\,MHz$ Frequency Range
- One External Resistor Sets the Carrier Frequency
- One External Resistor Sets Percent Frequency Spreading
- One External Resistor Sets the Modulation Frequency
- Configurable Modulation Profile (triangular, multi-triangular, multi-cycle, multi-triangular plus multi-cycle)
- Low Power Consumption ($1.2\,mA$ Max Supply Current)
- Low Timing Jitter $\leq 0.2\%$ Max when Spread Spectrum Frequency Modulation is disabled
- $-40°$ to $150°$ Operating Temperature Range
- 100Ω CMOS Output Driver

5.2.2 Single block concepts and schematics

In Figure 5.3 is shown the top concept structure of the developed application. As you can see, the concept schematic is composed by six main circuit blocks:

- *bandgap reference*
- *internal supply*
- *modulation profile generator*

- *voltage-to-current converter*
- *frequency modulator (Current Controlled Oscillator CCO)*
- *frequency divider*

This thesis work focused on the development of only the four last blocks, of which you can find a complete and depth review on the next sections of this chapter. Conversely the bandgap reference and the internal supply are two re-used blocks, and therefore a review of this parts isn't present in this thesis.

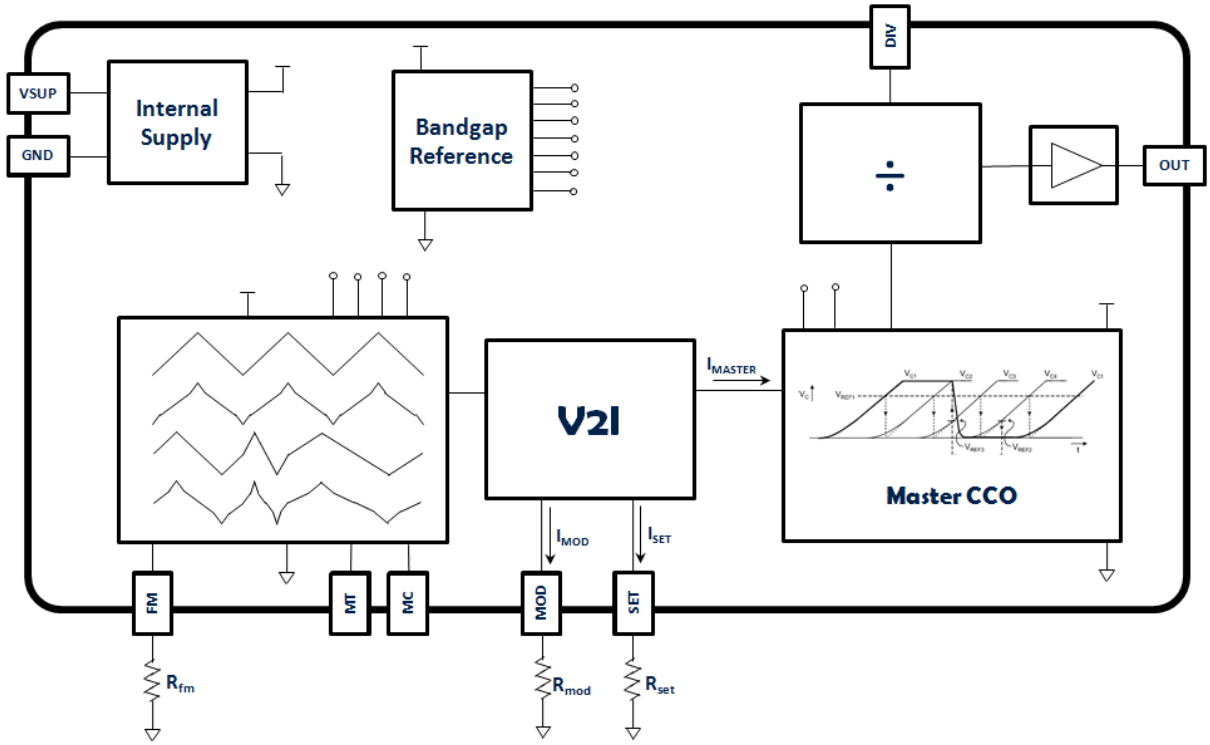


Figure 5.3: Top concept structure of the developed application

5.3 Frequency Modulator: Current Controlled Oscillator (CCO)

The Frequency Modulator oscillator is the real core of the developted application, farther it is the circuital block that most affect the final performances. Therefore at the beginning, a depth architectural study was necessary to investigate how to achieve the specifications performances we

need. Below you can find a brief investigation over different oscillators architectures that can be found in literature, and subsequently the complete review and sizing of the solution chosen.

5.3.1 Oscillators architectures

Several types of oscillators exist with differences in performance concerning stability and controllability of the frequency of oscillation, as well as achievable control linearity. The oscillators can be divided in several types, that are:

- *Resonator based oscillators:* these oscillators apply a tuned network, operating in resonance, to produce a periodic output signal. The tuned network can be for example a quartz crystal or an LC tank. Due to the high quality factor of the resonators applied, these oscillators exhibit excellent frequency stability. As a result, they are often used to realise the local oscillator in RF receivers, where the demands on phase noise are very stringent. In recent years, due to the rapid growth of the mobile communications market, a large research effort is put in realising high quality inductors on chip. The good frequency stability of passive resonator-based oscillators is related on the one hand to the particular frequency dependent behaviour of the impedance of these tuned networks, which shows a large phase variation for only a small frequency variation (high Q) at the resonance frequency, and to their low noise level on the other. Because of the particular phase/frequency behaviour of the resonator's impedance, their frequency controllability is generally poor.

- *Harmonic oscillators:* consisting of a combination of capacitors and transconductance elements (g_m-C). Using g_m-C elements, an element can be synthesised that behaves like an inductor. Due to finite output resistances of the transconductors, the synthesised LC tank can oscillate only when undamped with a negative resistor; the negative resistor can be realised also using transconductors. Because the noise level (due to the active elements) of the synthesised LC-tank is much higher than in a passive LC-tank with high Q, the frequency stability of these oscillators is worse than resonator based oscillators. The frequency of oscillation can be controlled by adapting a transconductance value.

- *Ring oscillators:* these oscillators consist of a ring of identical delay stages. Each delay stage successively produces a voltage ramp at its output node by charging its (parasitic)

capacitance with a current. They exhibit high speed and are easily integrated in standard digital CMOS processes. They are mostly used in clock recovery applications, where phase noise specs are weaker compared to the local oscillator application in RF receivers. Their frequency of oscillation can be tuned over a wide range by changing the current available to charge the load capacitance. Nevertheless, compared to regenerative oscillators, their control linearity is less good. However, the clock recovery application generally does not require a high control linearity. The analysis of their frequency stability has gained more attention in recent years [].

- *Relaxation oscillators:* or *regenerative oscillators* or *multivibrators* are frequently used voltage or current controlled oscillator configurations in monolithic integrated circuit design. They generate a time-varying, periodical signal by alternately charging and discharging a timing capacitor between two threshold levels. In their simplest form, a regenerative circuit exhibiting positive feedback (like for example a Schmitt-trigger) compares the capacitor voltage with two threshold voltages, and reverses the direction of the capacitor current each time the capacitor voltage crosses a threshold level. Due to their excellent suitability for integration, possible high frequency of oscillation and potentially good control linearity, they will be the base of the modulation profile generator circuit of this thesis work. Their oscillator class is the most easily controlled linearly over a wide range. Relaxation oscillators are part of the broader class of *first-order oscillators* []. First-order oscillators are characterised by a single pole that is involved in the generation of the time-varying, periodical signal. Especially first-order oscillators with their pole located in the origin (like the relaxation oscillator) lend themselves admirably for achieving high control linearity, because they show a fundamentally linear relation of the input control signal to frequency. Their practical implementation however, can give rise to trade-offs in performance.

As may become clear from this short survey, each type of oscillator has its own benefits and disadvantages. The oscillator's application determines which (combination of) parameter(s) is of prime importance.

5.3.2 Considerations

In Table 5.1 you can find a graphic comparision between the different oscillator architectures, whose we talked about before, plus a new architecture called *coupled sawtooth oscillator* we will treat below. The oscillator architectures are compared under different aspects like the linearity of their control charactestic, the maximum width of their frequency tuning range, the phase noise and the related timing jitter, the circuit complexity, the power consumption and finally the chip integration concerns and the area occupied. Each of this aspects was weighed and scaled considering its importance for our application, to allow to choose the best architecture for our purposes.

Having an oscillator with a wide frequency tuning range is usually a factor of big importance. But it isn't a fondamental factor, because the frequency tuning range can be easily extended using a configurable frequency divider. Also the area occupation is a concern aspect, because it directly affects the economical cost of the chip, moreover is given greater importance to the power consumption aspect, in particular into field like automotive enviroment. Conversely, design a high complex circuit isn't a concern aspect, even if it would be more difficult to project and to debug.

Jitter and phase noise seems to be not the most critical factors in spread spectrum applications applied to Switched Mode Power Supplies. Therefore in a trade-off with linearity, the timing jitter requirements take second. For this reason, in our application, there is no need of a Phase Locked Loop (PLL) based approach. The use of a PLL is needed only if high timing requirements are required (see Appendix **??**). Anyway phase noise (and jitter) is an important factor that affects the overall EMI reduction, and so, must to be carefully taken into account.

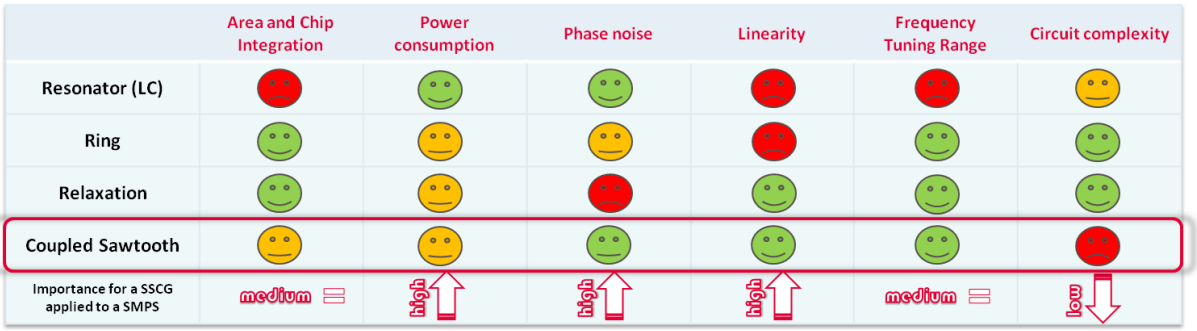


Table 5.1: Comparision of different controlled oscillator architectures. The *coupled sawotooth oscillator* is enlightened because have the best performances and the best trade-off between the different oscillator's figures of merit.

Some applications of VCO's require a good linearity of the frequency control characteristic of the oscillator. For example, in cases where a VCO is used for frequency modulation, linearity of the control characteristic of the VCO is a must, since it directly influences the amount of distortion of the modulated signal. In applications where control linearity is important, relaxation oscillators are often used because of their fundamentally linear relationship between input control signal and frequency of oscillation.

In many first-order oscillator designs, such as relaxation oscillators, the achievable control linearity (and the maximum frequency of oscillation) is ultimately limited by some delay that becomes part of the period of oscillation. This delay is most often introduced by the level detection circuitry that detects the threshold crossings of the capacitor voltage and subsequently reverses the capacitor current. Since this delay is normally non-linearly dependent on the oscillator's frequency control variable, it will degrade the control linearity. Unfortunately, minimising the delay will in turn often degrade the oscillator's frequency stability. Ideally, when the level detection is performed infinitely fast, the frequency of oscillation of a sawtooth oscillators, like the one in Figure 5.4(a), is given by:

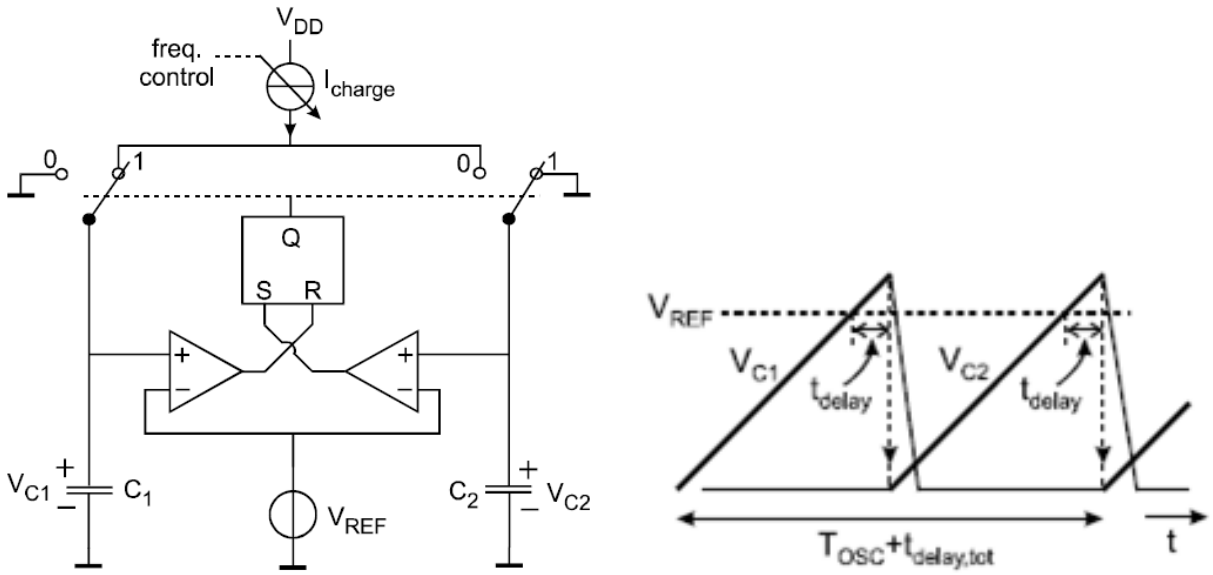
$$f_{osc_0} = \frac{I_{charge}}{2 \cdot C \cdot V_{REF}} \tag{5.1}$$

In practice, the output of the comparator reacts with a certain delay to a crossing of its input signals. This delay becomes noticeable in the capacitor waveforms in the form of overshoot of the reference level V_{REF}. This situation is depicted in Figure 5.4(b).

The delay, that is added to the period of oscillation, originates from the level detection circuitry. In first order, the delay, that is added to the period of oscillation, is independent from the oscillator's control current I_{charge}. In practice, this delay decreases somewhat with increasing frequencies of oscillation, due to the larger slope of the comparator input at higher frequencies of oscillation, resulting in a larger excitation of the comparator. The delay t_{delay}, which is introduced at a V_{REF}-crossing, results in a non-linear relationship between the control current and the frequency of oscillation. Assuming that the delay is independent of I_{charge}, the expression for f_{osc} becomes:

$$f_{osc_0} = \frac{1}{T_{osc_0} + t_{delay_{tot}}} = \frac{1}{\frac{1}{K_0 \cdot I_{charge}} + t_{delay_{tot}}} \quad \text{where:} \quad K_0 = \frac{1}{2 \cdot C \cdot V_{REF}} \tag{5.2}$$

Figure 5.5 gives an illustration of the non-linear dependency between f_{osc} and I_{charge}.



(a) (b)

Figure 5.4: (a) A regenerative sawtooth oscillator. (b) The capacitor voltage waveforms appearing in the regenerative oscillator including the delay introduced by the level detection circuitry.

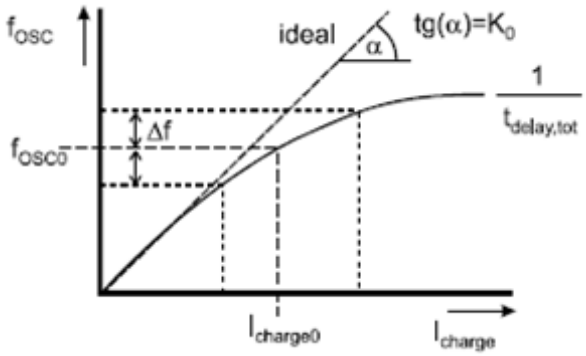


Figure 5.5: The non-linear control characteristic of the oscillator.

Two approaches can be found in literature to improve the control linearity of relaxation oscillators:

- applying negative feedback: a disadvantage of using negative feedback to increase control linearity is that the feedback loop limits the system dynamic. The loop gain at high modulating frequencies is limited. As a result, the accuracy of the frequency control characteristic decreases at this frequencies [];

- applying feedforward compensation to the threshold voltages: successfully applying feedforward techniques requires a thorough analysis of the oscillator. And even then, these techniques often fail because the compensating signal can not be matched well to the switching delay of the level detection circuit [].

For increasing values of I_{charge}, the frequency asymptotically approaches its maximum value $1/t_{delay_{tot}}$. The non-linearity in the control characteristic of the oscillator results in distortion when the oscillator is used in a frequency modulation application. In order to derive expressions for the harmonic distortion, a *Taylor expansion* of (5.2) around $(f_{osc_0}, I_{charge_0})$ must be made.

$$f_{osc}\left(I_{charge_0}+i\right) = f_{osc}\left(I_{charge_0}\right) + a_1 \cdot i + a_2 \cdot i^2 + \Theta\left(i^3\right)$$
$$\xrightarrow{\text{taylor expansion near } I_{charge_0}} \quad \begin{cases} a_1 = \dfrac{K_0}{\left(1+K_0 \cdot I_{charge_0} \cdot t_{delay_{tot}}\right)^2} \\ a_2 = -\dfrac{K_0 \cdot t_{delay_{tot}}}{I_{charge_0} \cdot \left(1+K_0 \cdot I_{charge_0} \cdot t_{delay_{tot}}\right)^2} \end{cases} \tag{5.3}$$

where the Taylor's coefficients can be derived easily using the symbolic calculator MuPad^{TM} of the the Matlab^{TM} suite. When the oscillator is used for frequency modulation, the control non-linearity yields second order distortion:

$$HD_2 = \frac{1}{2}\left|\frac{a_2}{a_1}\right| \cdot \Delta I = \frac{1}{2} \cdot \frac{\Delta I}{I_{charge_0}} \cdot t_{delay_{tot}} \tag{5.4}$$

Notice that the amount of distortion depend linearly on the total delay ($t_{delay_{tot}}$). In order to minimise the distortion, the delay of the level detection circuitry should be minimised. Unfortunately, this increases the noise bandwidth of the equivalent noise at the input of the detection circuit, resulting in an increase of the variance of this noise. As a consequence, the jitter of the oscillator increases.

Most noise sources, appearing in the oscillator circuit, can be represented by an equivalent noise source that is either:

- a current noise source i_n in parallel with the capacitor's charge current I_{charge};
- a voltage noise source v_n in series with the reference voltage V_{REF}.

The jitter of the relaxation oscillator is related to the signal-to-noise ratios of the capacitor's charge current and the threshold levels. These signal-to-noise ratios are in turn related to the power

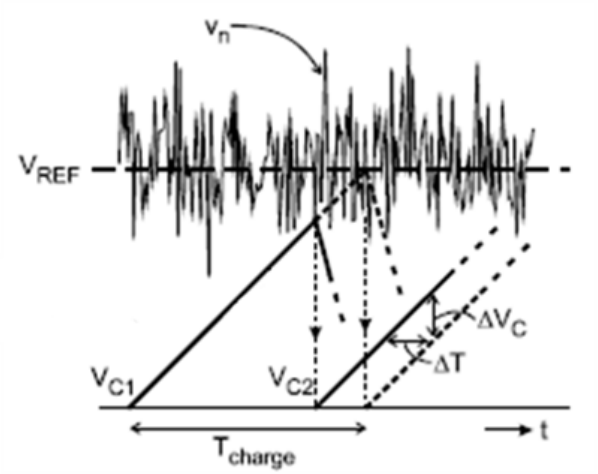


Figure 5.6: Effect on the timing of the capacitor voltage waveform by the noise voltage v_n, that is present on the reference voltage V_{REF}

dissipation. In practical realisations of relaxation oscillators, the jitter is dominantly determined by the signal-to-noise ratio of the threshold levels, like in Figure 5.6. The reason is that the threshold level noise contributes to jitter over a large effective bandwidth, due to the nearly ideal sampling of this noise by the fast circuitry that detects the threshold level crossings. A relationship exists between this effective bandwidth (and thus the jitter) and the control linearity of the relaxation oscillator. This coupling between jitter and control linearity results in a design trade-off in the realisation of relaxation oscillators. This is caused by the relationship between decision delay and noise filtering that exists in the comparators that detect a level crossing of the capacitor voltage. In order to achieve a good control linearity of the regenerative sawtooth oscillator, the decision delay must be made small and thus the bandwidth of the comparators must be chosen large. However, a larger comparator bandwidth gives less filtering of decision level noise, resulting thus in a larger noise voltage variance at the output of the comparator. This in turn increases the jitter of the oscillator.

5.3.3 A new oscillator concept

In this thesis, a new type of relaxation oscillator is implemented, called the *coupled sawtooth oscillator*. In this oscillator, a crossing of the threshold level by the capacitor voltage is detected using a simple differential pair, which is put directly in series with the current path that charges the

oscillator's capacitor (see Figure 5.7). This solution is contrary to the more conventional approaches using a comparator to perform the crossing detection: here, the comparator adds delay-introducing nodes to the timing path of the oscillator, thus deteriorating control linearity.

Conversely, it will be shown that the control linearity of the coupled sawtooth oscillator is ultimately limited only by transistor mismatches. Detecting the threshold level crossing by means of a differential pair thus allows for the achievement of a very high control linearity. More importantly, it will be shown that the application of a differential pair can be exploited to reduce the oscillator's jitter.

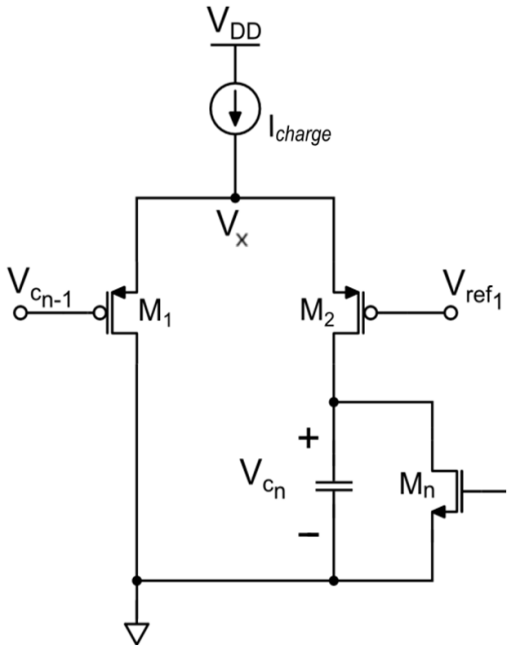


Figure 5.7: Concept schematic of a single cell

By maximising the switching time of the differential pair, the oscillator's capacitor is exploited for an effective filtering of the noise on the threshold levels, thus reducing the effective bandwidth by which this noise contributes to the jitter. This can be achieved without deterioration of the control linearity of the oscillator. As a result, the trade-off between control linearity and jitter disappears.

In the proposed oscillator, only positive ramps of capacitor voltages determine the duration of the period of oscillation. The only requirement for the negative ramps is that the capacitors must be discharged in time to allow the start of a new positive ramp. As shown in Figure 5.8, the capacitor voltages in the coupled sawtooth oscillator are allowed to traverse the decision level V_{REF_1}.

This creates a trajectory around V_{REF_1} that is used to gradually start up a new ramp. The aim of gradually starting up a capacitor voltage ramp in the coupled sawtooth oscillator is to reduce the jitter contribution of the voltage noise in series with V_{REF_1}, that is the dominant cause of jitter in a regenerative oscillator. The level detection circuitry that implements the gradual start-up converts the noise on V_{REF_1} into a current during start-up. This current is then integrated by the oscillator's capacitor. It can be shown that this integration results in an effective bandwidth reduction of the decision level noise, and thus a lower jitter.

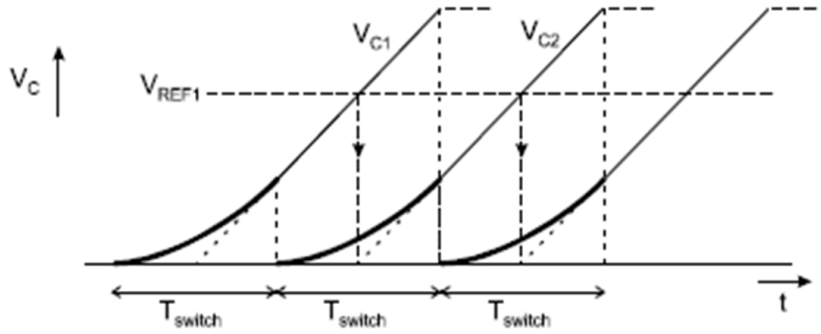


Figure 5.8: The allowable maximum switching time Tswitch of the differential pairs.

A differential pair implements the mechanism by which a new ramp is gradually started in the coupled sawtooth oscillator. Figure 5.7 shows the basic implementation of one stage in the coupled sawtooth oscillator, including a discharge transistor M_n. The differential pair consists of transistors $M_{1,2}$. The gate of transistor M_2 is the reference gate of the differential pair and it is connected to a constant bias voltage V_{REF_1}. The gate of transistor M_1 is the control gate and it is connected to the capacitor in the preceding stage of the oscillator. When this voltage reaches the vicinity of V_{REF_1}, the current though M_2 gradually increases from zero to its maximum value I_{charge}. Figure 5.9 shows the capacitor voltage waveforms of two successive stages V_{C_1} and V_{C_2} during start-up of V_{C_2}. During the time interval T_{switch} that the differential pair switches, the voltage noise v_n, present on V_{REF_1}, is transferred into a current by the differential pair transconductance. Subsequently, this current is integrated by the capacitor, resulting in a capacitor voltage error ΔV_{C_2}. This voltage error with the slope $\frac{I_{charge}}{C}$ determines the time error Δt_{saw} of the ramp starting moment in the next stage.

The magnitude of the voltage error ΔV_{C_2} is among other things dependent on the transconductance of the differential pair and the duration of the switching interval T_{switch}. It will be shown

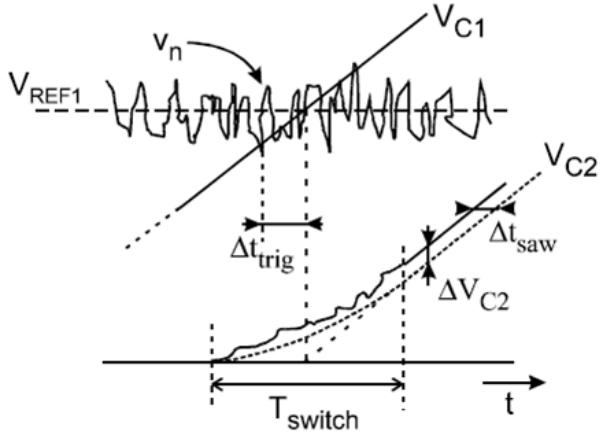


Figure 5.9: The effective filtering of decision level noise results in a smaller time error Δt_{saw} compared to the time error Δt_{trig} that would appear in a regenerative oscillator.

that the variance of ΔV_{C_2} is smaller than the variance of the noise voltage v_n. Figure 5.9 also shows the time error Δt_{trig} that would result if a trigger circuit is used to instantly start a new capacitor voltage ramp. Because the variance of ΔV_{C_2} is smaller than that of the noise voltage v_n, the variance of the time error Δt_{saw} appearing in the coupled sawtooth oscillator is smaller than that of the time error Δt_{trig} appearing in the regenerative sawtooth oscillator.

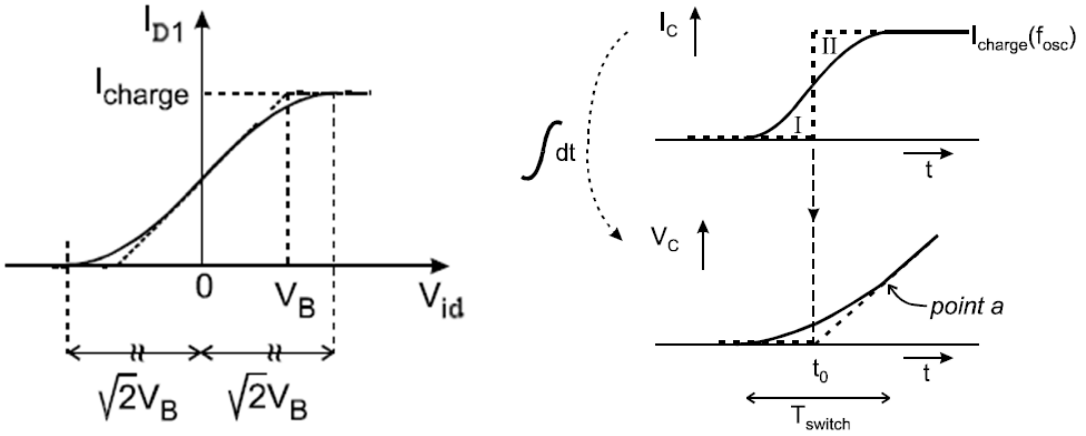
In case n oscillator stages each contribute one positive ramp to the generation of one period of oscillation, then the frequency of oscillation is given by:

$$f_{osc} = \frac{I_{charge}}{n \cdot C \cdot V_{REF_1}} \tag{5.5}$$

5.3.4 Preservation of control linearity

The slow increase of the capacitor current during startup of a ramp does not introduce any deterioration of the oscillator's control-linearity, due to the point-symmetrical transfer function of the differential pair (see Figure 5.10(a)).

During the time interval T_{switch}, the differential pair gradually increases the capacitor current I_C from zero to its maximum value I_{charge}. The solid I_C-curve in Figure 5.10(b) shows the capacitor current as a function of time in one stage of the coupled sawtooth oscillator. In this curve we can recognise the differential pair's transfer function between input differential voltage and output drain



(a) (b)

Figure 5.10: (a) Differential pair's transfer function between input differential voltage and output drain current of M_2. (b) Waveforms in one stage of the coupled sawtooth oscillator during start-up of a ramp, where $t = t_0$ indicates the moment when the gate voltage of transistor M_1 of the differential pair equals V_{REF_1}. The dashed I_C-curve represents the situation in which the differential pair $M_{1,2}$ acts like an instantaneous switch without delay (like in an ideal Schmitt-trigger relaxation oscillator). The lower half shows the resulting V_C-curves achieved by integration of the I_C-curves.

current of M_2, where the input differential voltage have to withstand this relationship:

$$|V_{id}| \leq \sqrt{\frac{I_{charge}}{\beta}} = \sqrt{\frac{2I_{charge}}{\mu C_{ox} \cdot \frac{W}{L}}} = \sqrt{2} \cdot \left(\sqrt{\frac{2I_{D_1}}{\mu C_{ox} \cdot \frac{W}{L}}} \right) \Bigg|_{V_{id}=0} = \sqrt{2} V_{ov} \Big|_{V_{id}=0} = \sqrt{2} V_B \qquad (5.6)$$

The transfer function $V_{id}(I_{D_{M_2}})$ is plotted here as a function of time rather than of the input differential voltage. This is allowed since the gate-voltage of the transistor M_1, which equals the capacitor voltage of the preceding stage, is a linear function of time during the interval T_{switch}. This can be seen in Figure 5.9, where for instance V_{C_1} is a linear function of time at the moment it reaches the proximity of V_{REF_1} and starts the secon ramp V_{C_2}.

Despite the gradual increase of the capacitor current during the start-up of a capacitor voltage ramp, the linearity in the relationship $f_{osc}(I_{charge})$ is guaranteed when the solid V_C-curve overlaps the dashed V_C-curve in their joint linear parts (at point a in Figure 5.10(b)), irrespectively of the value of I_{charge}. This condition is guaranteed if the areas I and II in Figure 5.10(b) are equal for each value of I_{charge}. This is indeed the case because the transfer curve $I_{D_{M_2}}(V_{in})$ of the differential pair is point-symmetrical in the point where the curve crosses the $V_{in} = 0$ axis ($t = t_0$ in Figure 5.10(b)), irrespective of the value of the tail current I_{charge}. *To assure that the input voltage of*

the differential pair is a linear function of time during switching, the start-up intervals T_{switch} of successive stages must not overlap in time. Thus, this give a restriction to the maximum allowable value for the switching time T_{switch}. Figure 5.8 illustrates the allowable maximum T_{switch}. In case n stages each contribute one rising ramp to the generation of one period of oscillation T_{osc}, then the allowable maximum T_{switch} is given by:

$$T_{switch_{MAX}} = \frac{T_{osc}}{n} \tag{5.7}$$

As previously explained, the control linearity is preserved by the differential pair's point-symmetrical relationship between input differential voltage V_in and output drain current $I_{D_{M_2}}$. However, if the position of the point of symmetry in this relationship becomes a function of the differential pair's tail current I_{charge} then non-linearity results in the relationship $f_{osc}(I_{charge})$. Any offset voltage results in a time error ΔT in the time interval T_{charge}. The offset voltage can be due to mismatches between the MOSFET transistors that compose the differential pair. This gives a non-linearity in the control characteristic of the oscillator only if there is a dependency between the time interval T_{charge} and the tail current I_{charge}. Moreover, in order to supply the current I_{charge} to the differential pair, a current mirror is used. Mismatches between the transistors of the mirror may affect the control linearity of the oscillator: whenever the mirror-ratio becomes dependent on the current I_{charge} that is mirrored, a non-linearity in the control characteristic of the oscillator results.

Below you can find a discussion over the different mismatch tipologies (both in the differential pair is in the current mirror), that can affect the control characteristic linearity of the oscillator.

V_{th} mismatch in differential pair

The offset voltage of the differential pair due to a threshold voltage mismatch ΔV_{th} between the differential pair's transistors is given by:

$$V_{offset}(I_{charge}) = \Delta V_{th} \tag{5.8}$$

The offset voltage is independent of the tail current I_{charge}. Hence, threshold voltage mismatch in the differential pair does not result in control non-linearity of the coupled sawtooth oscillator; it will only result in a (constant) shift of the effective reference voltage level V_{REF_1} in the oscillator.

β-factor mismatch in differential pair

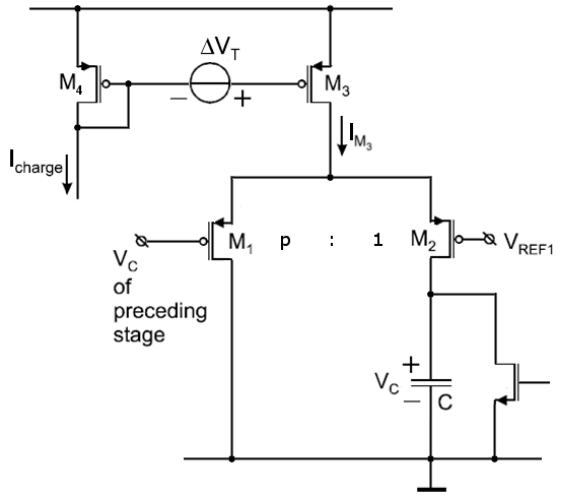


Figure 5.11: Concept schematic of a single cell in case of β-factor mismatch ($p \neq 1$) in the differential pair and/or V_{th} mismatch ($\Delta V_{th} \neq 0$) in the current mirror.

The offset voltage V_{offset} of a differential pair, operating in saturation, as a function of the tail current I_{charge} can be derived as:

$$V_{offset}(I_{charge}) = \eta \cdot \frac{I_{charge}}{g_m} = \frac{\eta}{2}\sqrt{\frac{I_{charge}}{\beta}} \quad \text{with} \quad \beta = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \tag{5.9}$$

in which η represents the relative amount of β-mismatch. The mismatch variance is dependent from the device area:

$$\eta = \frac{\Delta\beta}{\beta} = 6\,\sigma_{\beta\%} \quad \text{with} \quad \sigma_{\beta\%} = \frac{A_{\sigma_{\beta\%}}}{\sqrt{W \cdot L}} \tag{5.10}$$

The offset voltage of the differential pair due to β-mismatch is dependent on the tail current I_{charge} and will therefore result in control non-linearity of the oscillator.

Suppose now that the differential pair in each of the n stages shows the same amount of β-mismatch (worst case). Then the frequency of oscillation is given by (5.5), but with V_{REF_1} replaced

by $V_{REF_1}^{(\text{effective})} = V_{REF_1} + V_{offset}(I_{charge})$. Substituting this expression into (5.5) gives:

$$f_{osc} = \frac{I_{charge}}{n \cdot C \cdot [V_{REF_1} + V_{offset}(I_{charge})]} = \\ = \frac{I_{charge}}{n \cdot C \cdot V_{REF_1} \cdot \left[1 - \left(\frac{V_{offset}(I_{charge})}{V_{REF_1}}\right)^2\right]} \cdot \left[1 - \frac{V_{offset}(I_{charge})}{V_{REF_1}}\right] \cong \\ \cong \frac{I_{charge}}{n \cdot C \cdot V_{REF_1}} \cdot \left[1 - \frac{V_{offset}(I_{charge})}{V_{REF_1}}\right] = \frac{I_{charge}}{n \cdot C \cdot V_{REF_1}} \cdot \left(1 - \frac{\frac{\eta}{2}\sqrt{\frac{I_{charge}}{\beta}}}{V_{REF_1}}\right) \quad (5.11)$$

where the approximation can be made because $V_{offset}(I_{charge}) \ll V_{REF_1}$.

In order to estimate the harmonic distortion that results if the oscillator is used in a frequency modulation application, a Taylor expansion of (5.11) can be made around some I_{charge_0}:

$$f_{osc}\left(I_{charge_0} + i\right) = f_{osc}\left(I_{charge_0}\right) + a_1 \cdot i + a_2 \cdot i^2 + a_3 \cdot i^3 + \Theta\left(i^4\right)$$

$$\xrightarrow{\text{taylor expansion near } I_{charge_0}} \begin{cases} a_1 = \frac{f_{osc_0}}{I_{charge_0}} \cdot \left[1 - \frac{3}{2}\frac{V_{offset}\left(I_{charge_0}\right)}{V_{REF_1}}\right] \approx \frac{f_{osc_0}}{I_{charge_0}} \\ a_2 = -\frac{3}{8}\frac{f_{osc_0}}{{I_{charge_0}}^2}\frac{V_{offset}\left(I_{charge_0}\right)}{V_{REF_1}} \\ a_3 = \frac{1}{16}\frac{f_{osc_0}}{{I_{charge_0}}^3}\frac{V_{offset}\left(I_{charge_0}\right)}{V_{REF_1}} \\ f_{osc_0} = \frac{I_{charge_0}}{n \cdot C \cdot V_{REF_1}} \end{cases} \quad (5.12)$$

where the Taylor's coefficients can be derived easily using the symbolic calculator MuPad^{TM} of the the Matlab^{TM} suite, and where f_{osc_0} is the center-frequency in case of no mismatch.

The second- and third-order distortion can be derived as:

$$HD_2 = \frac{1}{2}\left|\frac{a_2}{a_1}\right| \cdot \Delta I = \frac{1}{8} \cdot \frac{1}{\left(\frac{2}{3}\frac{V_{REF_1}}{V_{offset}\left(I_{charge_0}\right)} - 1\right)} \cdot \frac{\Delta I}{I_{charge_0}} \approx \frac{3}{16}\frac{\frac{\eta}{2}\sqrt{\frac{I_{charge_0}}{\beta}}}{V_{REF_1}} \cdot \frac{\Delta I}{I_{charge_0}} \quad (5.13)$$

$$HD_3 = \frac{1}{4}\left|\frac{a_3}{a_1}\right| \cdot \Delta I^2 = \frac{1}{96} \cdot \frac{1}{\left(\frac{2}{3}\frac{V_{REF_1}}{V_{offset}\left(I_{charge_0}\right)} - 1\right)} \cdot \left(\frac{\Delta I}{I_{charge_0}}\right) \approx \frac{1}{64}\frac{\frac{\eta}{2}\sqrt{\frac{I_{charge_0}}{\beta}}}{V_{REF_1}} \cdot \left(\frac{\Delta I}{I_{charge_0}}\right)^2 \quad (5.14)$$

where ΔI is the amplitude of the sinusoidal current i in (5.12).

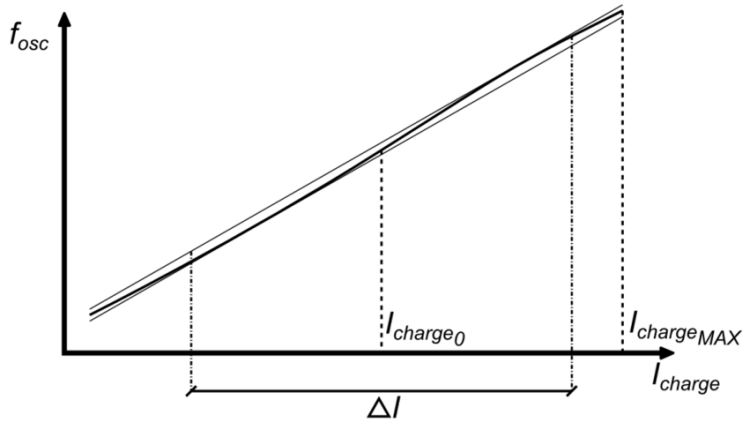


Figure 5.12: The real non-linear $f_{osc}\left(I_{charge_0}+i\right)$ characteristic.

The sizes W and L of the differential pair's transistors M_1 and M_2, can be derived as:

$$\left(\frac{W}{L}\right)_{1,2}=\frac{2}{\mu C_{ox}}\cdot\frac{1}{I_{charge_0}}\cdot\left(\frac{3}{32}\cdot\frac{\eta}{V_{REF_1}}\cdot\frac{\Delta I}{HD_2}\right)^2 \tag{5.15}$$

Substituting (5.10) into (5.15) we can obtain the width W of the differential pair's transistors M_1 and M_2:

$$W_{1,2}=\left[\frac{3}{32}\cdot\frac{6\,A_{\sigma_{\beta_\%}}}{V_{REF_1}}\cdot\frac{\left(\Delta I+8HD_2\cdot I_{charge_0}\right)}{HD_2}\right]\cdot\sqrt{\frac{2}{\mu C_{ox}}\cdot\frac{1}{I_{charge_0}}} \tag{5.16}$$

β-factor mismatch in current mirror

β-factor mismatch between the transistors of the current mirror results in a deviation from the ideal mirror ratio. However, the non-ideal mirror ratio is not dependent on the current that is mirrored. Therefore, β-mismatch in the current mirror does not affect the control linearity of the oscillator.

Threshold voltage V_{th} mismatch in current mirror

Threshold voltage mismatch between the transistors of the current mirror results in a deviation from the ideal mirror ratio that is dependent on the current that is mirrored. The drain current of transistor M_3 (the output current of the mirror) can be written as:

$$I_{D_{M_3}}=\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_3\left[\Delta V_{th}+\left(V_{GS_{M_4}}-V_{th_{M_4}}\right)\right]^2=\beta\cdot\left(\Delta V_{th}+\sqrt{\frac{I_{charge}}{\beta}}\right)^2\neq I_{D_{M_4}}=I_{charge} \tag{5.17}$$

The mismatch variance is dependent from the device area:

$$\Delta V_{th} = 6\,\sigma_{V_{th}} = \frac{A_{\sigma_{V_{th}}}}{\sqrt{W \cdot L}} \tag{5.18}$$

in which I_{charge} is the input current of the mirror. Suppose now that the current mirror in each of the stages of the coupled sawtooth oscillator shows the same threshold voltage mismatch ΔV_{th} (worst case). Then the frequency of oscillation is given by (5.5), but with I_{charge} replaced by $I_{D_{M_3}}$, resulting in:

$$f_{osc} = \frac{I_{D_{M_3}}}{n \cdot C \cdot V_{REF_1}} = \frac{\beta \cdot \left(\Delta V_{th} + \sqrt{\frac{I_{charge}}{\beta}}\right)^2}{n \cdot C \cdot V_{REF_1}} = \frac{\beta \cdot \left[\Delta V_{th} + V_{ov}\left(I_{charge}\right)\right]^2}{n \cdot C \cdot V_{REF_1}} \tag{5.19}$$

In order to estimate the harmonic distortion that results if the oscillator is used in a frequency modulation application, a Taylor expansion of (5.19) can be made around some I_{charge_0}:

$$f_{osc}\left(I_{charge_0} + i\right) = f_{osc}\left(I_{charge_0}\right) + a_1 \cdot i + a_2 \cdot i^2 + a_3 \cdot i^3 + \Theta\left(i^4\right)$$

$$\xrightarrow{\text{taylor expansion near } I_{charge_0}} \begin{cases} a_1 = \dfrac{f_{osc_0}}{I_{charge_0}} \cdot \dfrac{\Delta V_{th} + V_{ov_0}}{V_{ov_0}} \\ a_2 = -\dfrac{1}{4}\dfrac{f_{osc_0}}{{I_{charge_0}}^2} \cdot \dfrac{\Delta V_{th}}{V_{ov_0}} \\ a_3 = \dfrac{1}{8}\dfrac{f_{osc_0}}{{I_{charge_0}}^3} \cdot \dfrac{\Delta V_{th}}{V_{ov_0}} \\ V_{ov_0} = \sqrt{\dfrac{I_{charge_0}}{\beta}} \end{cases} \tag{5.20}$$

where the Taylor's coefficients can be derived easily using the symbolic calculator MuPad^{TM} of the the Matlab^{TM} suite. and where f_{osc_0} and V_{ov_0} are respectively the center-frequency and the overdrive tension in case of no mismatch. The second- and third-order distortion can be derived as:

$$HD_2 = \frac{1}{2}\left|\frac{a_2}{a_1}\right| \cdot \Delta I = \frac{1}{8} \cdot \frac{\Delta V_{th}}{\Delta V_{th} + \sqrt{\frac{I_{charge_0}}{\beta}}} \cdot \frac{\Delta I}{I_{charge_0}} \tag{5.21}$$

$$HD_3 = \frac{1}{4}\left|\frac{a_3}{a_1}\right| \cdot \Delta I^2 = \frac{1}{32} \cdot \frac{\Delta V_{th}}{\Delta V_{th} + \sqrt{\frac{I_{charge_0}}{\beta}}} \cdot \left(\frac{\Delta I}{I_{charge_0}}\right)^2 \tag{5.22}$$

in which ΔI is the amplitude of the sinusoidal current i in (5.20). The sizes W and L of the current mirror's transistors M_3 and M_4, can be derived as:

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_{charge_0}}{\frac{\mu C_{ox}}{2} \cdot \left[\Delta V_{th} \cdot \left(\frac{\Delta I}{8HD_2 \cdot I_{charge_0}} - 1\right)\right]^2} \tag{5.23}$$

Substituting (5.18) into (5.23) we can obtain the length L of the current mirror's transistors M_3 and M_4:

$$L_{3,4} = 6\, A_{\sigma_{\beta\%}} \cdot \left(\frac{\Delta I}{8HD_2 \cdot I_{charge_0}} - 1 \right) \cdot \sqrt{\frac{\mu C_{ox}}{2} \cdot \frac{1}{I_{charge_0}}} \tag{5.24}$$

5.3.5 Sizing

The start-up trajectory in a stage takes place during the time that the capacitor voltage of the preceding stage lies in a range $[-2 \cdot V_B, 2 \cdot V_B]$ symmetrically around V_{REF_1}, where $-2 \cdot V_B$ and $2 \cdot V_B$ bound the input voltage window of the differential pair.

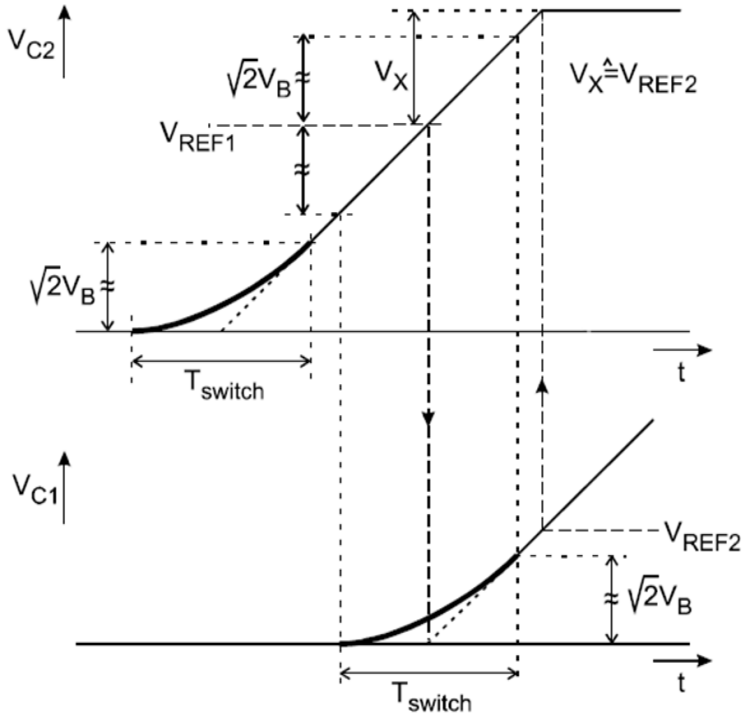


Figure 5.13: The optimum positioning of the reference voltage levels V_{REF_1} and V_{REF_2}.

When the capacitor voltage in the present stage crosses the reference voltage level V_{REF_2}, then the charge-state in the present stage is secured and the capacitor in the preceding stage will be clamped (see Figure 5.13). As the slopes of the capacitor voltage ramps became equal, the voltage V_x, equals V_{REF_2}. As a result, the amplitude of the capacitor voltage equals $V_{REF_1} + V_{REF_2}$. Given the supply voltage and the voltage drop for mantain the MOS of the current mirror in the saturation region, the amplitude $V_{REF_1} + V_{REF_2}$ determines the voltage that can be spent charging

the capacitor. Moreover, in a practical realisation of the circuit the voltage ramp is clamped to an amplitude slightly larger than $V_{REF_1} + V_{REF_2}$ of a quantity $\delta(I_{charge})$ which value is dependent from the current I_{charge}:

$$V_{C_{i_{MAX}}} = V_{REF_1} + V_{REF_2} + \delta(I_{charge}) \tag{5.25}$$

Consider now the stage 1 (take as reference Figure 5.7). Is quite simple to detect the drain-source voltage of transistor M_2 as:

$$V_{DS_2} = V_{C_1} - V_{REF_1} + V_{GS_2} \tag{5.26}$$

For a correct circuit working, and avoid any kind of non-linearities and distortion, transistor M_2 need to work in its saturation region for any capacitor voltages, until this voltage ramp is clamped to its maximum value $V_{C_{1_{MAX}}}$. Therefore, applying the saturation region condition: $V_{DS_2} < V_{GS_2} - V_{th_p}$, and equation (5.25) and (5.26), we finally obtain that:

$$V_{C_{1_{MAX}}} < V_{REF_1} - V_{th_p} \quad \Longrightarrow \quad V_{REF_2} < \delta(I_{charge}) - V_{th_p} \tag{5.27}$$

Others constraints limit the choice of the voltage references V_{REF_1} and V_{REF_2} and can be determined by looking at the capacitor voltage waveforms in Figure 5.13. In order to guarantee the control linearity of the oscillator, the start-up trajectories of successive capacitor voltage ramps are not allowed to overlap. The start-up trajectory of the capacitor voltage in the present stage has to be completed before this voltage crosses the reference voltage level V_{REF_2}. From Figure 5.13 it can be concluded that this gives the following constraints:

$$\begin{cases} V_{REF_1} > 2 \cdot \sqrt{2} V_{ov} \left(I_{D_{M_2}} = I_{charge} \right) = 2 \cdot \sqrt{2} V_B \\ V_{REF_2} > \sqrt{2} V_{ov} \left(I_{D_{M_2}} = I_{charge} \right) = \sqrt{2} V_B \end{cases} \tag{5.28}$$

The voltage V_B, which is related to the transfer function of the differential pair (see Figure 5.10(a)), plays an important role in establishing the right values of the various voltage reference levels. In case of a MOSFET differential pair, V_B is not only dependent on the geometry of the transistors, but also on the tail current I_{charge}. Thus, when I_{charge} is changed in order to change the frequency of oscillation, V_B also changes.

$$V_B\left(I_{charge}\right) = \sqrt{\frac{I_{charge}}{\mu C_{ox} \cdot W/L}} = \sqrt{\frac{I_{charge}}{2 \cdot \beta}} \tag{5.29}$$

As a result, because the voltage reference levels V_{REF_1} and V_{REF_2} are constant, condition (5.28) can only be satisfied as long as the value of I_{charge} remains below a certain maximum value $I_{charge_{MAX}}$. Therefore, a more correct representation of condition (5.28) is given by:

$$\begin{cases} V_{REF_1} > 2 \cdot \sqrt{2} V_B \, (I_{charge} = I_{charge_{MAX}}) \\ V_{REF_2} > \sqrt{2} V_B \, (I_{charge} = I_{charge_{MAX}}) \end{cases} \tag{5.30}$$

As a consequence of the dependency of V_B on I_{charge}, the frequency range over which the oscillator is linearly controllable is limited to a certain maximum frequency of oscillation (related to $I_{charge} = I_{charge_{MAX}}$).

The duration of the start-up interval T_{switch} is determined by the voltage V_B and the slope of the capacitor voltage as:

$$T_{switch} = \frac{2\sqrt{2} \cdot V_B}{\left(\frac{I_{charge}}{C}\right)} = \frac{2\sqrt{2}}{\left(\frac{I_{charge}}{C}\right)} \cdot \sqrt{\frac{I_{charge}}{2 \cdot \beta}} = \frac{2C}{\sqrt{\beta \cdot I_{charge}}} \propto \left(\frac{W}{L}\right)_{1,2}^{-\frac{1}{2}} \tag{5.31}$$

The duration T_{switch} of the start-up trajectories of capacitor voltage ramps should be chosen maximally, in order to establish a maximum effective bandwidth reduction of the noise on V_{REF_1} that contributes to the jitter.

$$Jitter \propto \frac{1}{T_{switch}} \quad \Longrightarrow \quad Jitter \propto \sqrt{\left(\frac{W}{L}\right)_{1,2}} \tag{5.32}$$

As result, to reduce jitter, we need to size the differential pair MOS with a minimum W/L ratio, but as this is in conflict with the very low headroom that we have (the chip have to work at low voltage 2.5 V), so there is a trade-off between jitter and low voltage operation.

5.3.6 Timing

The minimum required number of stages in a coupled sawtooth oscillator is two. But an additional memory is required then to store the information about which capacitor needs to be (dis)charged. Moreover, it is possible to construct ring structures of identical stages that no longer require the use of an additional regenerative memory, and this results in a less complex timing of the necessary discharge intervals. Figure 5.14 shows the complete oscillator circuit.

In a two stage coupled sawtooth oscillator, the maximum possible T_{switch} that can be chosen is rather limited. By implementing the coupled sawtooth oscillator as a ring of several stages, this

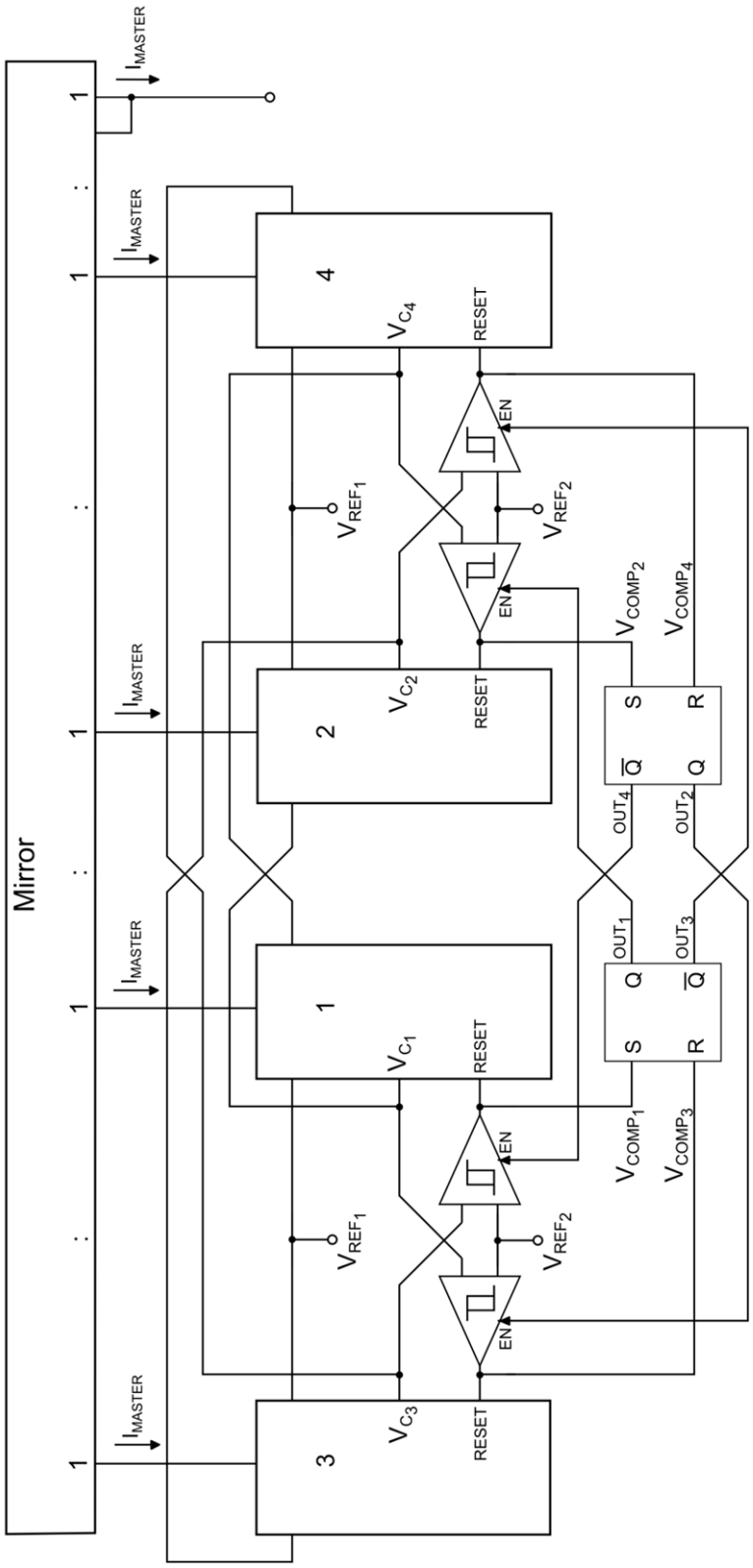


Figure 5.14: Concept schematic of the master curent controlled oscillator

problem can be solved. As there are more than two stages, some other stage (whose capacitor was already discharged earlier) can be given the task to generate the next capacitor voltage ramp. Thus, the start-up of the next ramp does not have to "wait" for the completion of the discharge interval in the preceding stage. As a result, the time between the start-up intervals of successive capacitor voltage ramps can be reduced, resulting in a larger effective coverage of the period of oscillation by a start-up interval. This reduces the contribution of noise on V_{REF_1} to jitter. Another opportunity offered by the ring structure is the possibility to use the capacitor in a stage as the memory securing the charge-state of the capacitor in the next stage. This can be done by simply postponing the discharging of the capacitor in the present stage until the charge-interval of the capacitor in the next stage is completed. The additional circuitry necessary to secure a charge-state is then no longer needed.

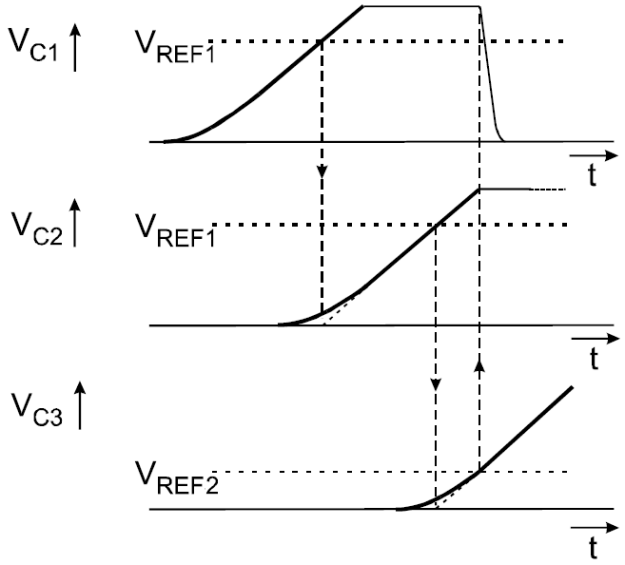


Figure 5.15: By postponing the discharging of C_1, V_{C_2} can safely complete its positive ramp.

Figure 5.15 illustrates this principle. When the capacitor voltage V_{C_1} reaches the vicinity of V_{REF_1}, the differential pair that controls the charge current of C_2 slowly turns on the capacitor current. After the completion of the start-up interval of V_{C_2}, the capacitor C_1 is kept charged (the voltage V_{C_1} remains high), instead of being discharged. As a result, the charge-state of C_2 (equivalent to the positive ramp of V_{C_2}) is safely secured, as the differential pair that controls the charge current of C_2 safely maintains its switched position. The reason that C_1 in Figure 5.15 is not

discharged directly after the start-up of V_{C_2} is that now V_{C_3} instead of V_{C_2} initiates the discharging of C_1. When V_{C_3} reaches V_{REF_2}, the capacitor C_1 is discharged. When this occurs, the differential pair in stage two, controlling the charge current of capacitor C_2, is switched back, such that the current charging C_2 becomes zero. As a result, V_{C_2} no longer increases and remains constant. A similar story holds for the other capacitors in the ring. This also explains the horizontal part in the V_{C_1}-waveform.

The capacitor in stage number n is discharged based on a comparison of the capacitor voltage in stage number $(n+2)$ with V_{REF_2}, so as $V_{C_{n+2}}$ cross the reference level, the discharge will start and will stop as the capacitor voltage cross another reference voltage bigger than V_{REF_2}. Conventionally this is performed using a comparator and a reference voltage, but a simpler method to perform this is to treat the analogic capacitor voltage $V_{C_{n+2}}$ like a digital signal and using a simple `NOT` digital port with an intrisic internal threshold voltage usually at one half of the internal supply voltage. A circuit solution that can perform this function is shown in Figure 5.16.

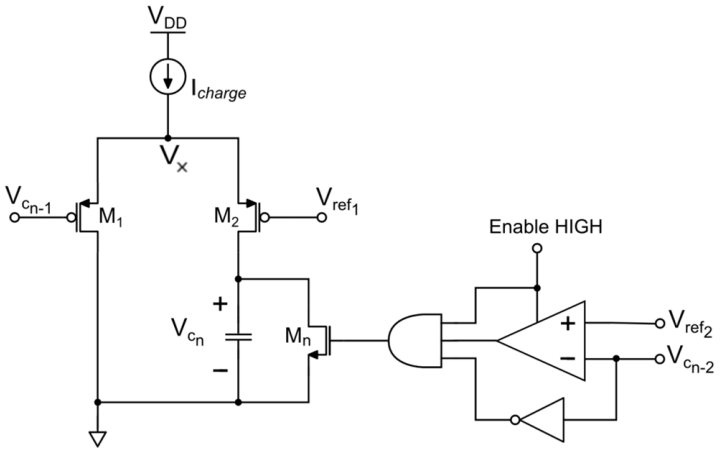


Figure 5.16: Concept schematic of the reset circuit adopted

Simple flip-flops are employed to buffer the capacitor voltages. Buffering is essential because the capacitor voltages can't be employed directly to drive low-impedance loads. This would affect the charge currents of the capacitors and thus possibly the control linearity of the oscillator. The output buffers (flip-flops) that generate the square wave output signals $OUT_{1..4}$ are controlled by the oscillator's comparators. One might wonder whether the equivalent input noise of the comparators or the noise on V_{REF_2} results in additional jitter. Although these noise sources indeed result in

timing errors in the edges of the signals $OUT_{1..4}$, these errors do not accumulate (add up) in time. In other words: they do not result in a growing phase error between the signals $OUT_{1..4}$ and the capacitor voltage waveforms. In 4-phase mode, all outputs have a 50% duty cycle. The outputs are all 90° out of phase. OUT_2 lags OUT_1 by 90°, OUT_3 lags OUT_2 by 90° and OUT_4 lags OUT_3 by 90°.

Figure 5.17 shows the principal signal waveforms related to time of each of the four stage that compose the oscillator implemented, in the top part of the figure are shown the capacitor voltages V_C, in the middle part the digital output phases OUT and in the bottom part the digital reset circuit generated by the circuit in Figure 5.16, and that discharge the capacitor voltages.

5.3.7 Biasing and final sizing

Instead of using just one current mirror with multiple outputs, two separate current mirrors ($M_{1a,2a,1c,2c,3m,4m}$ and $M_{1b,2b,1d,2d,5m,6m}$) are used. Each current mirror supplies the current I_{charge} towards two individual stages. This has the advantage that the gate-bias rails of the transistors in the mirrors that supply the current I_{charge} towards stages 1 and 3 on the one hand and stages 2 and 4 on the other hand are separated. When the capacitor in a certain stage is discharged, the gate of the PMOS transistor of the differential pair in the next stage is pulled to ground abruptly. Due to the parasitic gate-drain capacitance of the output mirror-transistor connected to the differential pair, a spike is generated on the gate-bias rail. For example, if C_1 is discharged, the gate of transistor M_1 in stage 2 is pulled to ground. As a result of the parasitic gate-drain capacitance of the mirror transistor M_{13}, a spike is generated on the gate-bias rail V_{bias2}. However, this has no effect on the positive ramp of V_{C_3} that is generated simultaneously, because the gate of M_9 is connected to the gate-bias rail V_{bias1} of the other mirror.

In order to reduce the systematic error and enhance the common-mode rejection ratio (CMRR), cascode current mirrors are used, such the one shown in Figure 5.19, which is a high-swing CMOS current mirror with two input branches.

Using a cascode transistor enhances the output resistance:

$$R_{out} = r_{o_2} \cdot (1 + g_{m_2} \cdot r_{o_1}) \tag{5.33}$$

If the biasing voltage V_{BIAS} is such that: $V_{DS_1} = V_{BIAS} - V_{GS_2} = V_{ov_1}$ therefore $V_{out_{min}} = V_{ov_1} + V_{ov_2}$. In this way we have an high output swing. If $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$ the

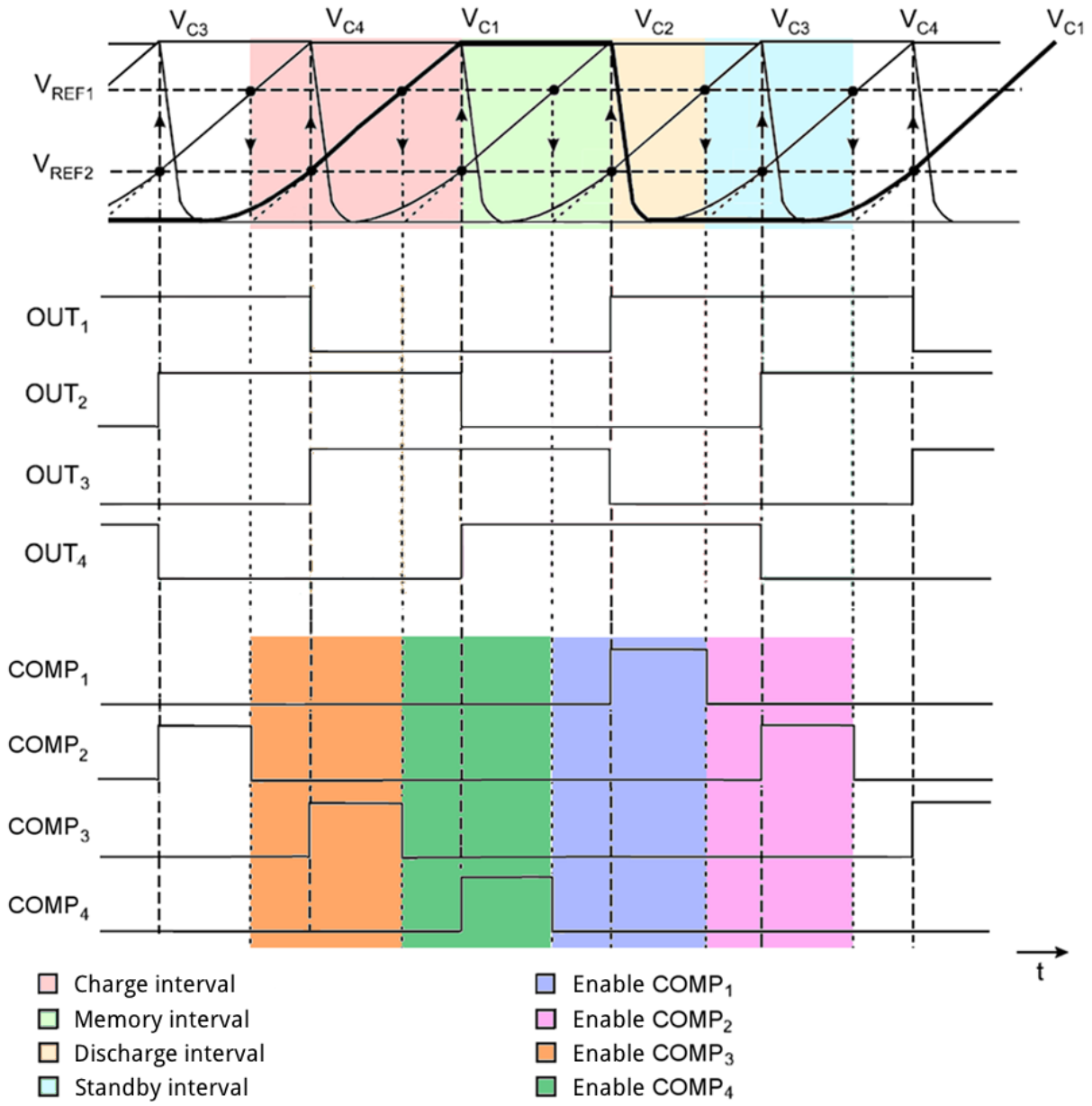


Figure 5.17: The voltage waveforms in a four-stage coupled sawtooth oscillator. Respectively are shown, in the top part of the picture the four capacitor voltages (with the different time intervals that compose a single phase), in the middle part the four output phases $OUT_{1..4}$ and finally, in the bottom part the four signals that come from the respective comparators.

systematic current error is zero because $V_{DS_1} = V_{DS_{13}}$. Transistor M_{16} always work in saturation region ($V_{GS_{16}} = V_{DS_{16}}$) and being $V_{GS_{16}} + V_{DS_{15}} = V_{GS_2} + V_{DS_1}$:

$$\text{if} \quad \left(\frac{W}{L}\right)_{16} = \left(\frac{W}{L}\right)_{2} \quad \Longrightarrow \quad V_{DS_1} = V_{DS_{15}} \tag{5.34}$$

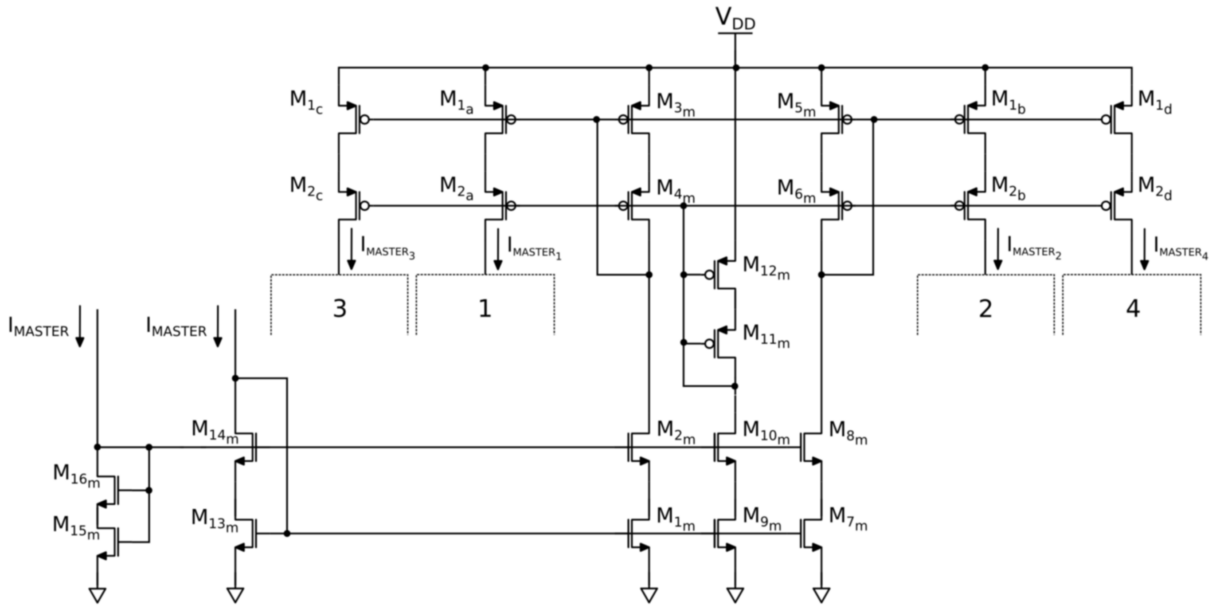


Figure 5.18: Two separate current mirrors supplies the current I_{charge} towards the four oscillator stages.

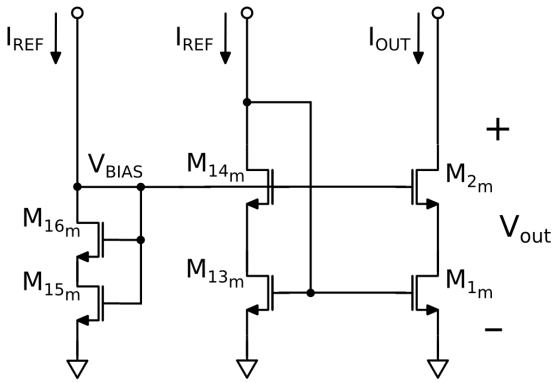


Figure 5.19: High-swing CMOS current mirror with two input branches

because the currents in the two branches are equals and thus: $V_{GS_{16}} = V_{GS_2}$. Transistor M_{15} work in linear region: $V_{DS_{15}} = V_{GS_{15}} - V_{GS_{16}} < V_{GS_{15}} - V_{th_{15}}$. Imposing: $V_{DS_{15}} = V_{ov_1} = V_{ov_2} = V_{ov_{14}} = V_{ov_{16}} = V_{ov}$ and ignoring the body effect, finally, we obtain this condiction that relates the geometry ratio between the MOSs M_{15} and M_{16}

$$\left(\frac{W}{L}\right)_{15} = \frac{1}{3} \cdot \left(\frac{W}{L}\right)_{16} \tag{5.35}$$

The result obtained with relation (5.36) is used also for sizing the PMOS transistors M_{11} and

M_{12}:

$$\left(\frac{W}{L}\right)_{12} = \frac{1}{3} \cdot \left(\frac{W}{L}\right)_{11} \tag{5.36}$$

Each oscillator's stage have a PMOS high-swing cascode current mirror which supplies the current I_{charge}. This impose that the voltage V_x (see Figure 5.7) can't to exceed a maximum voltage value for the correct biasing of the MOSs in their saturation region. This relation implies that the differential pair's MOS and the cascode mirror's MOS have to be opportunily sized. The geometry ratios have to withstand this relation:

$$\begin{aligned} V_x = V_{REF_1} - V_{GS_{2_{diff.\,pair}}} < V_{DD} - 2V_{ov} \quad \Longrightarrow \\ \left(\sqrt{\left(\frac{L}{W}\right)_{diff.\,pair}} + 2\sqrt{\left(\frac{L}{W}\right)_{mirror}}\right) < (V_{DD} - V_{REF_1} + V_{th_p}) \cdot \sqrt{\frac{\mu C_{ox}}{I_{charge_{MAX}}}} \end{aligned} \tag{5.37}$$

Relation (5.37) has to be putted together in a system, with linearity relations (5.16) and (5.24), to detect the geometry sizes of each MOS. To determine a realistic value for the transistor's sizes W and L, consider the following set of specifications:

- $HD_2 = -66\,dB$ which is its typical value for FM sound modulation/demotulation;
- $HD_3 = -90\,dB$ which is its typical value for FM sound modulation/demotulation;
- $I_{charge_{MAX}}$ fixed to $20\,\mu A$ to reduce the power consumption.
- I_{charge_0} fixed to $12\,\mu A$ at the middle of the full current swing.
- ΔI fixed to $16\,\mu A$ equal to the full current swing;

Finally for sizing the load timing capacitor in each stage, you just have to rearrange equation (5.5) as:

$$f_{osc} = \frac{I_{charge}}{n \cdot C_{L_{tot}} \cdot V_{REF_1}} \quad \Longrightarrow \quad C_{L_{tot}} = \frac{I_{charge_{MAX}}}{n \cdot f_{osc_{MAX}} \cdot V_{REF_1}} \tag{5.38}$$

where $C_{L_{tot}}$ is the sum of the load timing capacitor and of the parassitic capacitances.

5.4 Voltage-to-current converter (V2I)

As shown in the block diagram (see Figure 5.3), the master oscillator is controlled by the master current entering into it (I_{MASTER}) this current is the same of I_{charge} that was used in the

previous section.

$$f_{osc} = k_0 \cdot I_{MASTER} \qquad \text{where:} \qquad k_0 = \frac{1}{4 \cdot C_{L_{tot}} \cdot V_{REF_1}} \tag{5.39}$$

When the spread spectrum frequency modulation (SSFM) is disabled, I_{MASTER} is strictly determined by the I_{SET} current. When SSFM is enabled, the current I_{MOD} (modulation current) is subtracted from the I_{SET} current to determine the I_{MASTER} current value.

$$I_{MASTER} = I_{SET} - I_{MOD} \tag{5.40}$$

Here the frequency of the master oscillator is modulated to produce a frequency that is always less than or equal to the frequency set by the I_{SET} current.

$$f_{osc_{UP}} = f_{osc}\Big|_{I_{MOD}=0} = \frac{I_{SET}}{4 \cdot C_{L_{tot}} \cdot V_{REF_1}} = k_0 \cdot I_{SET} \tag{5.41}$$

As explained, we need to allow the user to set the currents I_{SET} and I_{MOD} by two external resistors, respectively R_{SET} and R_{MOD}. In this regard we have implemeted the voltage-to-current (V2I) converter circuit shown in Figure 5.20.

The circuit shown in Figure 5.20 is actually composed by two voltage-to-current converters (and two current mirrors), that are shown in Figure 5.24 and Figure 5.21. Their function is to convert two voltages waveforms, respectively V_{SET} and V_{MOD}, in two currents (I_{SET} and I_{MOD}) which are then subtracted from each other by an internal circuit node.

The voltage on the SET pin is forced to approximately $1.25\,V$ by the PMOS transistor and its gate bias voltage. The R_{SET} resistor, connected between GND and the SET pin, locks together the V_{SET} voltage and the current I_{SET}.

$$R_{SET} = \frac{V_{SET}}{I_{SET}} \tag{5.42}$$

This allows the parts to attain excellent frequency accuracy regardless of the precision of the SET pin voltage. Additionally, the MOD pin has a similar function like the SET pin. The R_{MOD} resistor connected between GND and the MOD pins similarly locks together the MOD pin voltage variation and the I_{MOD}.

$$R_{MOD} = \frac{V_{MOD}}{I_{MOD}} \tag{5.43}$$

When the spread spectrum modulation is toggled off the frequency $f_{osc_{UP}}$ is the fixed master oscillator's output frequency. When SSFM is enabled, $f_{osc_{UP}}$ is the maximum output frequency. In

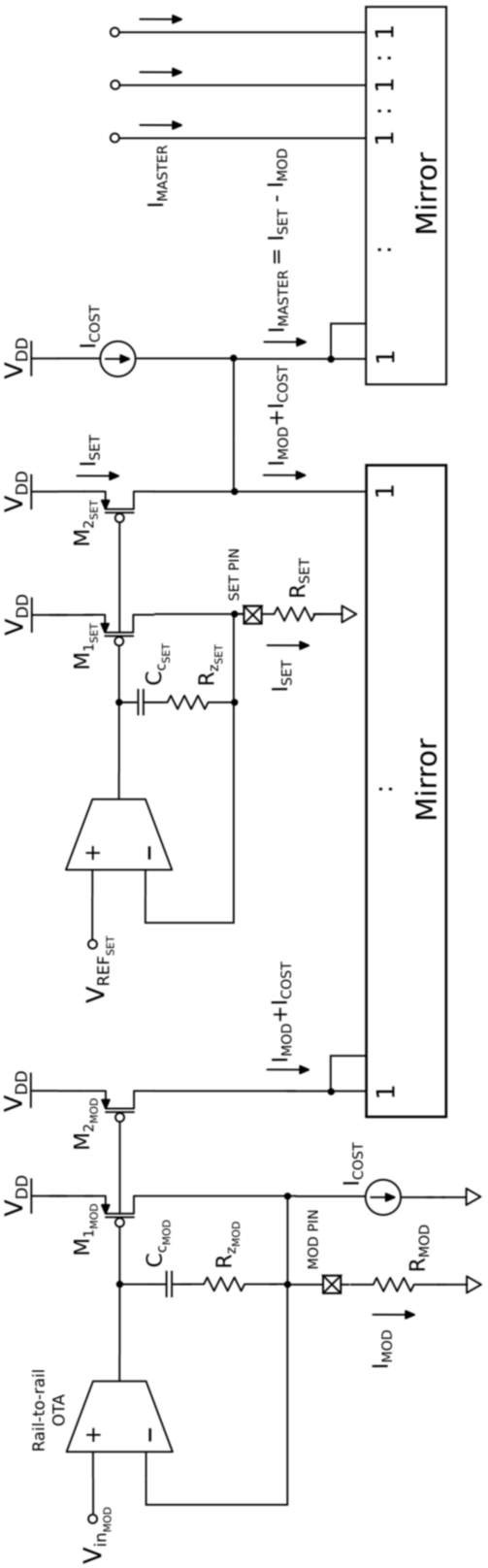


Figure 5.20: Concept schematic of the complete voltage-to-current converter

both cases, $f_{osc_{UP}}$, is determined by the R_{SET} resistor value:

$$f_{osc_{UP}} = \frac{1.5 \cdot 10^{11}}{R_{SET}} \tag{5.44}$$

When the spread spectrum modulation is toggled on the oscillator's frequency is modulated by a programmable triangular signal to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation levels and improves electromagnetic emission (EME) performance. The amount of frequency spreading is determined by the external resistor R_{MOD} and the voltage between GND and the MOD pin. Unlike the stationary SET pin voltage (V_{SET}), the MOD pin voltage (V_{MOD}) is a dynamic signal generated by a programmable analog profile generator, that can range from about $0\,V$ minimum to about V_{DD} maximally.

The ratio of R_{SET} to R_{MOD} determine the amount of frequency spreading. The general formula for the amount of frequency spreading is below:

$$\%_{\text{SPREADING}} = \frac{2R_{SET}}{R_{MOD}} \cdot 100 \tag{5.45}$$

where frequency spreading is defined as:

$$\%_{\text{SPREADING}} = 100 \cdot \frac{\Delta f_{osc}}{f_{osc_{UP}}} = 100 \cdot \frac{f_{osc_{UP}} - f_{osc_{LOW}}}{f_{osc_{UP}}} = 100 \cdot \frac{I_{MOD_{MAX}}}{I_{SET}} \tag{5.46}$$

and the frequency width of the spreading window Δf_{osc} is defined as:

$$\Delta f_{osc} = f_{osc_{UP}} - f_{osc_{LOW}} = \left| f_{osc} \Big|_{I_{SET}=0} \right| = \frac{I_{MOD_{MAX}}}{4 \cdot C_{L_{tot}} \cdot V_{REF_1}} \tag{5.47}$$

The design procedure is to first choose the R_{SET} resistor value to set $f_{osc_{UP}}$ and then choose the R_{MOD} resistor value to set the amount of frequency spreading desired. Note that the frequency is always modulated to a lower value. This is often referred to as a down spread modulation. To disable the SSFM, connect the MOD pin to ground. Grounding the MOD pin disables the modulation and shuts down the modulation circuitry. While leaving the MOD pin open, $R_{MOD} = \infty$, gives a frequency spreading of 0%, this is not a good method of disabling the modulation. The open pin is susceptible to external noise coupling that can affect the output frequency accuracy. Grounding the MOD pin is the best way to disable the SSFM.

The master oscillator has a frequency range spanning 0.64MHz to 2.56MHz. However, accuracy may suffer if the master oscillator is operated at greater than 10MHz. A programmable divider extends the frequency range to greater than three decades. For constant frequency applications,

where SSFM is disabled, the best operating position depends on which parameter is most important in the application. For the lowest clock jitter it is best to set the divider to its highest setting as done above. The divider reduces the master oscillator's jitter. The higher the division number the greater the reduction in the master oscillator's jitter. For the best frequency accuracy it is best to run the programmable divider at its lowest setting, and thus, the master oscillator runs at a lower frequency. The lower master oscillator frequencies are more accurate and use less power. The master oscillator's output is connected to the programmable divider. When the spread spectrum modulation is disabled, the frequency $f_{OUT_{UP}}$ is the final output frequency. When SSFM is enabled, $f_{OUT_{UP}}$ is the maximum output frequency, that is determined by the R_{SET} resistor value and the programmable divider setting. The formula for setting the output frequency, f_{OUT}, is below:

$$f_{OUT_{UP}} = \frac{f_{osc_{UP}}}{N_{DIV}} = \frac{1.5 \cdot 10^{11}}{N_{DIV} \cdot R_{SET}} \tag{5.48}$$

where:

$$N_{DIV} = \begin{cases} 1 & \text{DIV pin} = V_{DD} \\ 4 & \text{DIV pin} = \text{Open} \\ 16 & \text{DIV pin} = \text{GND} \end{cases} \tag{5.49}$$

The programmable divider divides the master oscillator signal by 1, 4 or 16. The divide-by-value is determined by the state of the DIV input. Tie DIV to GND to select ÷1. This is the highest frequency range, with the master output frequency passed directly to the multiphase circuit. The DIV pin may be floated or driven to midsupply to select ÷4, the intermediate frequency range. The lowest frequency range, ÷16, is selected by tying DIV to V_{DD}. After choosing the proper divider setting, determine the correct frequency-setting resistor. Because of the linear correspondence between oscillation period and resistance, a simple equation relates resistance with frequency:

$$R_{SET} = \frac{V_{SET}}{I_{SET}} = \frac{V_{SET}}{4 \cdot C_{L_{tot}} \cdot V_{REF_1} \cdot f_{osc_{UP}}} = \frac{1.5 \cdot 10^{11}}{f_{osc_{UP}}} = \frac{1.5 \cdot 10^{11}}{f_{OUT_{UP}} \cdot N_{DIV}} \tag{5.50}$$

where:

$$f_{osc_{UP}} \in [640\,k \div 2.56\,M]\ Hz \tag{5.51}$$

$$R_{SET} \in [62.5 \div 234.375]\ k\Omega \tag{5.52}$$

The realized solution is optimized for use with R_{SET} resistors between $62.5\,k\Omega$ and $234.375\,k\Omega$. This corresponds to master oscillator frequencies between $640\,kHz$ and $2.56\,MHz$.

Setting the spread spectrum modulation percentage is very simple and straightforward. In general, for greatest EMC improvement, each application should apply as much spreading as possible. The amount of spreading that any particular application can tolerate is dependent on the specific nature of that application. Once the R_{SET} resistor value is calculated to set $f_{osc_{UP}}$ and the desired spreading is determined, the R_{MOD} value is calculated using the simple equation below:

$$R_{MOD} = \frac{V_{MOD_{MAX}}}{I_{MOD_{MAX}}} = \frac{V_{MOD_{MAX}}}{I_{SET}} \cdot \frac{100}{\%_{\text{SPREADING}}} = \begin{cases} 2R_{SET} \cdot \dfrac{100}{\%_{\text{SPREADING}}} \\ \dfrac{3 \cdot 10^{13}}{N_{DIV} \cdot f_{OUT_{UP}} \cdot \%_{\text{SPREADING}}} \end{cases} \tag{5.53}$$

where:

$$\%_{\text{SPREADING}} \in [0.5 \div 50]\ \% \tag{5.54}$$

$$R_{MOD} \in [234\,k \div 50\,M]\ \Omega \tag{5.55}$$

The only limitations for this formula are in the R_{MOD} value range and the spreading percentage range. The range of the R_{MOD} resistor value is from $234\,k\Omega$ to $50\,M\Omega$. The realized solution is specified for spreading from 0.5% to 50%. These are practical limits that would apply to the application systems we have plained. The lower limit is set by internal offsets and mismatches, and in particular by the value that the external resistor R_{MOD} that for spreading percentage less than 0.5% would became too large (ideally a spreading percentage of 0% can be obtained with $R_{MOD} = \infty$). At lower spreading percentages, these mismatches become more significant and the error from the calculated, desired spreading increases. A practical lower end limit would be about 2% spreading, (a spreading percentage less than this practical limit is meaningless for any Switched Mode Power Converter application, but would be usefull for motherboard and microprocessor clock reference applications). At the higher end internal mismatching becomes less significant. However a theoretical limit of 50%, that is $f_{OUT_{LOW}} = f_{OUT_{UP}}/2$, is usually adopted to avoid significant overlapping of near sub-window modulated harmonics. A practical upper limit would be about 40% spreading.

5.4.1 Sizing of the modulation spreading V2I converter

The circuit shown Figure 5.21 converts a variyng voltage waveform, in a current. The amount of frequency spreading is determined by the external resistor R_{MOD} and the voltage between GND and the MOD pin.

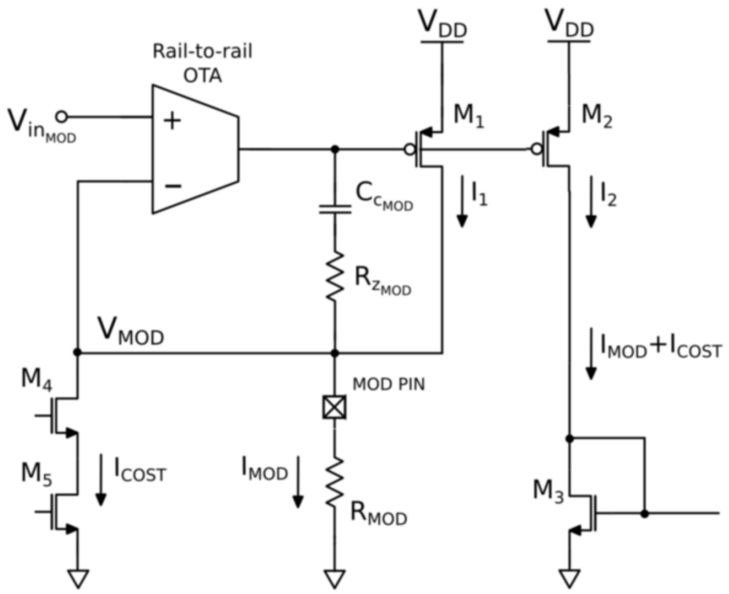


Figure 5.21: Concept schematic of the voltage-to-current converter that only set the modulation spread.

The voltage on the MOD pin is forced to exactly track the converter input voltage V_{in} due to high voltage gain of the OTA and by the PMOS transistor M_1.

$$V_{in_{MOD}} = V_{MOD} \tag{5.56}$$

The converter input voltage $V_{in_{MOD}}$ is a dynamic signal generated by a programmable analog profile generator, that can range from about $0\,V$ minimum to about V_{DD} maximally. This high input swing from a rail to another, involves the use of rail-to-rail OTA, as the one shown in Figure 5.23.

The R_{MOD} resistor connected between GND and the MOD pins locks together the MOD pin voltage variation and the I_{MOD}. The I_{MOD} current flowing through the transistor M_1 imposes a gate-source voltage by:

$$V_{GS_1} = -\sqrt{\frac{I_{D_1}}{\frac{\mu_p C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_1}} + V_{th_p} = V_{GS_2} \tag{5.57}$$

In this way the drain current I_{D_2} of PMOS M_2 tracks I_{MOD}. Indeed the current mirrored is the sum of the modulation current and a costant current:

$$I_{D_2} = I_{D_1} = I_{MOD} + I_{COST} \tag{5.58}$$

where the costant current I_{COST} is supplied for stability purposes, (as explained later in this section) by a low-voltage cascode mirror composed by transistors M_4 and M_5. As already mentioned V_{MOD} varies from rail to rail, but to mantain transistors M_1, M_4 and M_5 correctly biased in their saturation region, the allowed voltage swing of V_{MOD} (and thus also V_{in}) has to be limited:

$$\begin{cases} V_{DS_1} = V_{MOD} - V_{DD} \\ V_{DS_4} + V_{DS_5} = V_{MOD} \end{cases} \quad \Rightarrow \quad V_{ov_4} - V_{ov_5} = 2V_{ov_{4,5}} \leq V_{in} = V_{MOD} \leq V_{DD} - V_{ov_1} \tag{5.59}$$

Even if the disequation in (5.59) give the full range that $V_{in_{MOD}}$ can assume, an exceeding of this limits can be done. In this way the transistor will switch from the saturation region to the linear region. As was subsequently proven by simulation this will add a distortion to the current output signal I_{MOD} at the vertices of the triangular waveform. Therefore, the vertices will change shape, and will became more acute, like in a *hershey-kiss* modulation profile. This is something quite desired, and will take an enhancement for our application. For this reason, we impose a minimum and a maximum boundary limit larger than the limits in equation (5.59).

Moreover, the sizing of transistor M_1 must take account of the condition to mantain it in saturation region:

$$V_{DS_1} < V_{GS_1} - V_{th_p} \tag{5.60}$$

Using (5.57), (5.59), (5.58) and (5.60) equations, the ratio of the sizes of transistor M_1 can be derived as:

$$\left(\frac{W}{L}\right)_{1,2} > \frac{\dfrac{V_{MOD}}{R_{MOD}} + I_{COST}}{\dfrac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{MOD})^2} = \frac{I_{MOD_{MAX}} + I_{COST}}{\dfrac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{MOD_{MAX}})^2} \tag{5.61}$$

$V_{in_{MOD}}$ is a voltage signal with maximum fondamental frequency $f_{m_{MAX}} = 50\,kHz$, but has a triangular (or evev more complex) waveform shape, hence it present an high spectral content. In order to avoid any type of filtering effect or distortion by the rail-to-rail OTA, that would affect the final spectral result, the system must have a bandwith quite large. To have a good margin we impose that the converter gain bandwith (GBW) need to be: $GBW = 20 \cdot f_{m_{MAX}} = 1\,MHz \gg f_{m_{MAX}}$.

The voltage-to-current converter system composed by the OTA, and the PMOS M_1 in series with the R_{MOD} resistor is equivalent to a two-stage OTA. This type of system can became instable, therefore it need an appropriate frequency compensation. The instability is due to the small phase

margin (PM), which is dependent to ratio between the unity-gain frequency (ω_c) and the non-dominant pole (ω_{pd}):

$$PM = 180° - 90° - \arctan\left(\frac{\omega_c}{\omega_{pnd}}\right) \qquad , \qquad PM \propto \frac{\omega_{pnd}}{\omega_c} \tag{5.62}$$

For this purpose a *Miller compensation* was performed. The Miller compensation network consist of the series of a capacitor C_c plus a resistor R_z. The equivalent circuit for a two-stage OTA with a Miller conpensation is shown in Figure 5.22.

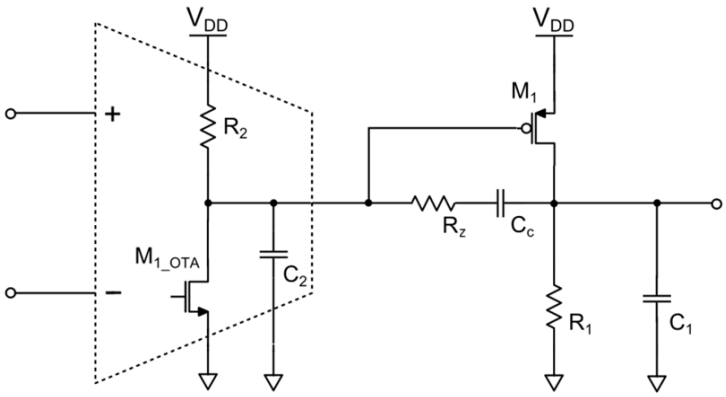


Figure 5.22: Generic schematic of a Miller compensation

With this type of compensation, the converter unity-gain bandwith (GBW) became:

$$GBW = \omega_c = \frac{g_{m_{1_{OTA}}}}{C_c} \tag{5.63}$$

Adding the Miller capacitor C_c, the input capacitance of the second stage will increase. Therefore, assuming C_c is large, the dominant pole (ω_{pd}) can be approximated as:

$$\omega_{pd} \approx \frac{1}{R_1 \cdot R_2 \cdot g_{m_1} \cdot C_c} \tag{5.64}$$

At high frequency the Miller capacitor became a short, and thus M_1 became a diode-connected transistor. Therefore, the non-dominant pole (ω_{pnd}) can be calculated as:

$$\omega_{pnd} = \omega_{p_2} \approx \frac{g_{m_1}}{C_1 + C_2 + \dfrac{C_1 \cdot C_2}{C_c}} \tag{5.65}$$

This is the so called *pole-splitting*. Performing a small-signal analysis, also the presence of a positive real part zero may be highlighted. The effect of this zero is to reduce the avaible phase

margin, therefore this zero must be shifted away to improve the PM. A possible solution is to add the *nulling resistor* R_z, which shift the zero or to ∞ or into the left half-plane to delete the non-dominant pole. This changes the transfer function as:

$$A_v(s) = \frac{A_{v_0} \cdot \left(1 - \frac{s}{z'}\right)}{\left(1 - \frac{s}{p_1}\right) \cdot \left(1 - \frac{s}{p_2}\right) \cdot \left(1 - \frac{s}{p_3}\right)} \tag{5.66}$$

where the DC gain can be calculated as:

$$A_{v_0} = g_{m_{1_{OTA}}} \cdot R_1 \cdot g_{m_1} \cdot R_2 \tag{5.67}$$

and the poles became $p_1 = p_{pd}$, $p_2 = p_{pnd}$ and $p_3 \approx -\frac{1}{R_z \cdot C_1}$. This last pole has frequency $\omega_{p_3} \gg \omega_c$ and don't damages stability. Lastly the zero became:

$$z' = \frac{1}{\left(\frac{1}{g_{m_1}} - R_z\right) \cdot C_c} \tag{5.68}$$

This zero moves to infinity when R_z equals $\frac{1}{g_{m_1}}$.

$$\text{for} \quad z' \longrightarrow \infty \qquad \Longrightarrow \qquad R_z = \frac{1}{g_{m_1}} \tag{5.69}$$

Making the resistor greater than $\frac{1}{g_{m_1}}$ moves the zero into the left half-plane, which can be used to provide positive phase shift at high frequencies and improve the phase margin. In practice, resistor R_z is usually implemented using a MOS transistor biased in the triode region. A MOS transistor operating in the triode region behaves like a linear resistor if $V_{DS} \ll 2 \cdot (V_{GS} - V_{th})$.

In order to achieve a 45° phase margin, the compensation capacitor should be chosen so that the unity-gain frequency equals the non-dominant pole $\omega_c = \omega_{pnd}$ (assuming the zero has been eliminated and $\omega_{p_3} \gg \omega_c$). Therefore:

$$A_{v_0} \cdot |p_1| = 1 \cdot |p_2| \qquad \Longrightarrow \qquad \frac{g_{m_{1_{OTA}}}}{C_c} = \frac{g_{m_1}}{C_1 + C_2 + \frac{C_1 \cdot C_2}{C_c}} \tag{5.70}$$

Rearranging equation (5.70) the value of compensating capacitor C_c can be derived. If $C_c \gg C_{1,2}$ a simple and approximate relation can be calculated as:

$$C_c \approx \frac{g_{m_{1_{OTA}}}}{g_{m_1}} \cdot (C_1 + C_2) \tag{5.71}$$

As already said the input voltage V_{in} is a dynamic rail-to-rail signal, therefore also the current I_{MOD} and the g_{m_1} have large spreads:

$$g_{m_1} = \sqrt{2\mu_p C_{ox} \cdot I_{D_1} \cdot \left(\frac{W}{L}\right)_1} = \sqrt{2\mu_p C_{ox} \cdot (I_{COST} + I_{MOD}) \cdot \left(\frac{W}{L}\right)_1} \tag{5.72}$$

As $I_{D_1} \longrightarrow 0$ also the transconductance $g_{m_1} \longrightarrow 0$. Therefore, a Miller compensation is no longer applicable, because the compensation capacitance and the nulling resistor would take values too large. For this reason, are imposed a lower limit to the current I_{D_1} adding to I_{MOD} a costant current I_{COST} and sizing the compensation network for this minimum current value. The same amount of current I_{COST} are then subtracted in a successive stage, in order to obtain the correct I_{MASTER} current.

Rail-to-rail OTA

Operational amplifiers with p-channel differential stage input devices have an input common-mode range that includes the negative power supply. The positive common-mode range is, however, quite limited below the positive supply. Operatonal amplifiers with n-channel input devices have the opposite properties. They have a positive-input common-mode range that includes the positive power supply, whereas the negative range is quite above the negative supply. For applications where the common-mode input range goes beyond or at least includes both power supply rails, the OTA requires an input stage with an NMOS and PMOS differential pair connected in parallel. Several OTA structures with rail-to-rail common-mode input stage are avaiable. The solution adopted is shown in Figure 5.23.

The OTA input stage is constructed from the parallel connection of p- and n-channel differentail stages made of transistors M_2 to M_3 and M_1 to M_4, respectively. The differential-stage tail current sources are formed from devices M_{14}, M_{18} and M_{13}, M_{15}. The cascode current mirrors M_5 to M_8 and the folded-cascode devices M_9 to M_{10} form the single-ended output stage. The biasing scheme adopted maximize the output voltage range. The open-loop gain is calculated to be:

$$A_v = \left(g_{m_n} + g_{m_p}\right) \cdot R_o \tag{5.73}$$

where R_o is the output impedance of the input stage:

$$R_o = \left[r_{o_9} \cdot g_{m_9} \cdot (r_{o_2} // r_{o_1 1})\right] // \left[r_{o_7} \cdot g_{m_7} \cdot (r_{o_1} // r_{o_5})\right] \tag{5.74}$$

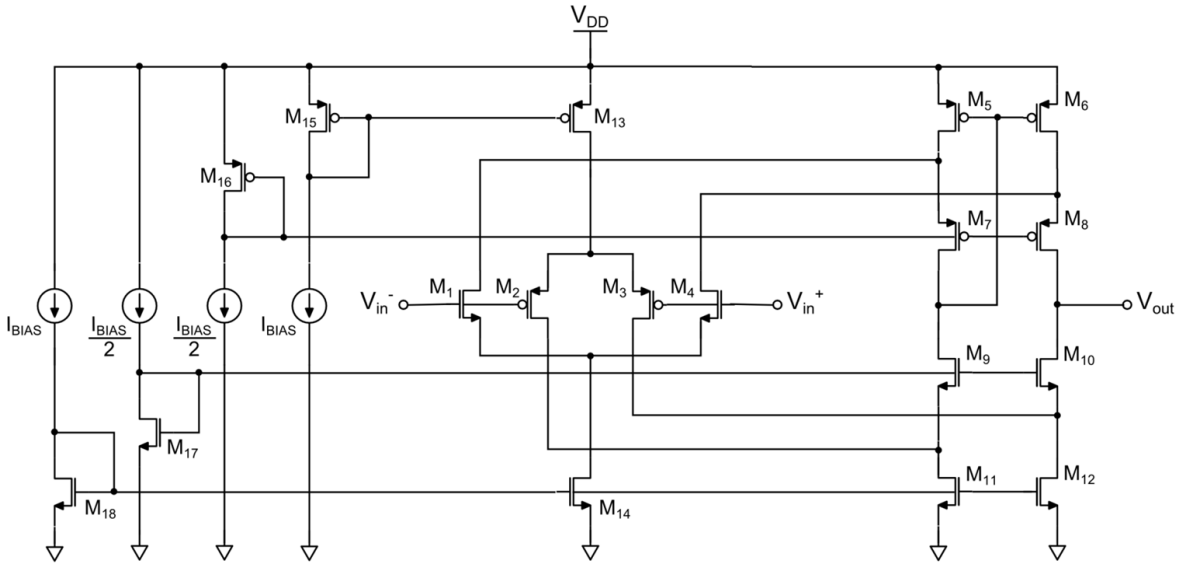


Figure 5.23: Concept schematic of a Rail-to-rail OTA

One major drawback of the rail-to-rail OTA shown in Figure 5.23 is that the transconductance g_m of the input devices varies by a factor of 2 over the input common-mode range. This large variation prevent the OTA from having an optimum frequency compensation over the entire operating range. To mantain a costant g_m value the following condition should be satisfied between the W/L ratios of the p- and n-channel input devices:

$$\text{if} \quad \frac{\mu_n C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_n = \frac{\mu_p C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_p \quad \Longrightarrow \quad A_v = 2g_m \cdot R_o \tag{5.75}$$

5.4.2 Sizing of the setting V2I converter

The circuit shown Figure 5.24 converts a costant voltage reference, in a current, which set the maximum oscillation frequency of the master VCO. The current value is determined by the external resistor R_{SET} and the voltage between GND and the SET pin.

The voltage on the SET pin is forced to exactly track the converter input voltage $V_{REF_{SET}}$ due to high voltage gain of the OTA and by the PMOS transistor M_1 ($V_{SET} = V_{REF_{SET}}$). The reference input voltage is a costant signal generated by a precise bandgap circuit, and has a value of $1.25\,V$. Therefore OTA used is a simple single stage amplifier with NMOS input differential pair.

The R_{SET} resistor connected between GND and the SET pins locks together the SET pin voltage and the I_{SET}. The I_{SET} current flowing through the transistor M_1 imposes a fixed gate-

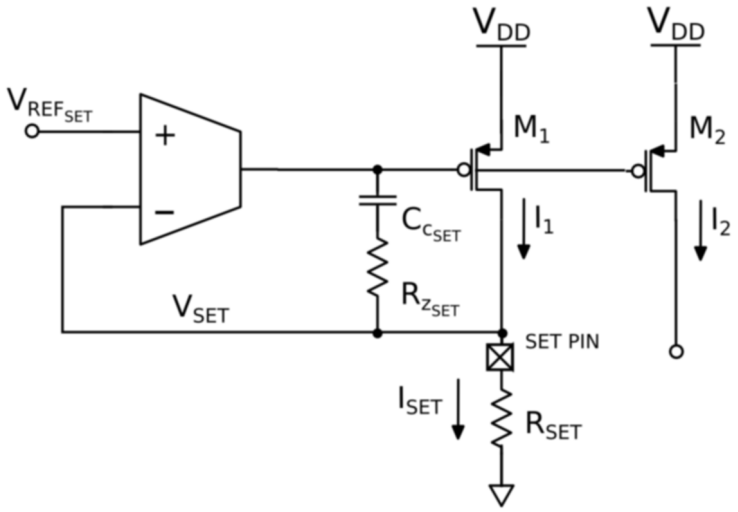


Figure 5.24: Concept schematic of the voltage-to-current converter that only set the maximum oscillation frequency.

source voltage on boths M_1 and M_2 transistors. In this way the drain current I_{D_2} of PMOS M_2 tracks I_{SET}.

This circuit block don't need a stringent sizing as in the previous part. Here, the voltage to convert is costant and the I_{SET} have a limited range of values. Therefore, there isn't bandwith requirements, and don't need, as previously, to add a costant current for stability. The only requirements are on the sizing of PMOSs M_1 and M_2 that must take account of the condition to mantain they in saturation region, the ratio of the sizes of the transistors can be derived as:

$$\left(\frac{W}{L}\right)_{1,2} > \frac{\dfrac{V_{SET}}{R_{SET}}}{\dfrac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{SET})^2} = \frac{I_{SET}}{\dfrac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{SET})^2} \tag{5.76}$$

In order to size the Miller compensation network, just need to use equations 5.69 and 5.71.

5.4.3 Low-Voltage Cascode Mirror

The current mirrors shown in Figure 5.20 need to operate with low headroom while still mantain an high output impedance, to avoid any type of distortions that would affect the final spreading resut. In this regard we have investigated several current mirror architectures from literature.

A current mirror is characterized by the current level it produces, the small-signal output

resistance and voltage drop across it. The *Wilson* and *Modified Wilson current mirrors* require an input voltage of two diode drops and output compliance voltage incorporates a diode drop plus saturation voltage. Such diode drop made Wilson mirror unattractive for low-voltage design. The *low-voltage cascode current mirror*, instead, has the drawback to require for its correct biasing a current that matches its input current.

To overcome these drawbacks, a new Wilson topology was introduced [], which sense the output current at low input voltage of a diode drop plus a saturation voltage whereas output senses only two saturation voltage. As seen from architecture, the diode connected transistor on input side biased by current source I_B, causes the input voltage to decrease much lower than gate voltage needed as in case of simple mirrors to sink input current. This makes it a *low voltage high-swing improved-Wilson current mirror* as shown in Figure 5.25. The mirror achieves high output resistance by using negative feedback and is directly proportional to the magnitude of the loop-gain of the feedback action from the output current to the gate of output transistor M_2. The transistor M_3 and M_4 samples the I_{out} and compares it with I_{in}. In combination with current source load I_{in}, transistor M_3 act as a common source amplifier used to maintain gate voltage of M_2 to avoid mismatching of I_{out} to I_{in}. Neglecting 2^{nd} order effects, the output resistance r_{out} is approximated as:

$$r_{out} \approx g_{m_3} \cdot r_{o_3} \cdot r_{o_2} \tag{5.77}$$

where, g_{m_3} and r_{o_3} are transconductance and output resistance of M_3 whereas r_{o_2} is output resistance of M_2.

The degree to which the bottom transistor is saturated depends on the I_{in}/I_B and $\frac{(W/L)_{5,6}}{(W/L)_{3,4}}$ ratio, the larger these values, the closer V is to $V_{DS_{sat}}$. The systematic gain error could be eliminated by making V' equal to V, but in this way the cascode would be effectively disabled. To overcome this, another copy of I_B is injected into node V', as shown in Figure 5.25. If I_B is generated by a saturated pMOS transistor, we can improve the circuit further by adding a diode-connected transistor, as shown. The resulting mirror has a low systematic transfer error and a high output impedance. The output compliance voltage of this mirror is two saturation voltages, as, the input compliance voltage is a diode drop plus a saturation voltage. The bias current, I_B, does not represent an upper limit on the input current and does not need to track it adaptively.

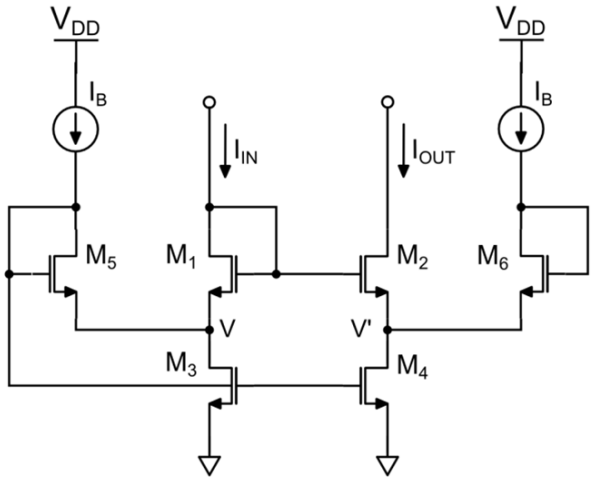


Figure 5.25: Concept schematic of a Low-Voltage Cascode Mirror

5.5 Modulation Profile Generator

As already explained, our choice was to implemente a simple modulation profile like the triangular one, and to avoid a more complex profile like the hershey-kiss even if it would carry better results and performances. Moreover, we choose to implemente a new modulation profile, that claims to be the junction point between triangular and herhey-kiss profiles, and the best trade-off between circuit complexity and performances. This new profile is, the so called, *multi-slope triangular* or *multi-triangular* profile. In this way we can adopte a simple analogic approach.

In general, SSCG modulated the frequency by a single modulation cycle. In addition to the triangular and multi-triangular profiles, we choose also to implemete a new modulation technique, the so called *Multi-Cycle* or *Multiple Cycle Combination Modulation*. By using multiple modulation cycles you can diffuse the spectrum uniformly and realize a larger EMI reduction effect. In a conventional SSCG circuit, a triangular wave shaped modulation signal wich changes in a costant period is used. Therefore, for example, if an oscillation frequency of 1 MHz is modulated with $f_m = 30kHz$, the spectrum conponents are spaced at intervals of 30 kHz, that is for a center-spread modulation, 910 kHz, 940 kHz, 970 kHz, 1 MHz, 1.03 MHz, 1.06 MHz, and 1.09 MHz, with $m_f = 7$ being the modulation index. In contrast to this, if the frequency of the modulating signal is changed in such a way that $f_{m_1} = 30kHz$, $f_{m_2} = 27kHz$, $f_{m_3} = 24kHz$, $f_{m_4} = 33kHz$ and $f_{m_5} = 36kHz$, the spectrum components are divided into five groups, that is, one group in wich they are spaced

at intervals of 24 kHz, another one in which they are spaced at intervals of 27 kHz, and so on, at intervals of 30 kHz, 33 kHz and 36 kHz. As the period of the spread spectrum modulation signal changes so as to take multiple different periods, the spectrum is further spread compared to the case where the period is costant.

This technique can be applied to both the triangular and multi-triangular profiles, with only a modest increase in complexity. In this way, we have four modulation options that can be used to modulate the clock reference, and the profile selection was left to the user, by two digital programmable pins [MT, MC]:

- [11] simple triangular
- [01] multi-triangular
- [10] multi-cycle triangular
- [00] multi-cycle multi-triangular

The simplest way to generate a triangular waveform, with an analogic approach, is by a basic *triangular relaxation oscillator*. It generates a time-varying, periodical signal by alternately charging and discharging a timing capacitor between two threshold levels. In their simplest form, a regenerative circuit exhibiting positive feedback (like for example a Schmitt-trigger) compares the capacitor voltage with two threshold voltages, and reverses the direction of the capacitor current each time the capacitor voltage crosses a threshold level. The basic concept schematic is shown if Figure 5.26.

Alternatively charging and discharging a capacitor through two costant current generators (basically a charge pump with a PMOS current mirror for the charging path and an NMOS current mirror for the discharging path) would lead to a triangular voltage waveform composed by straight and linear pieces with slopes:

$$slope_{charge} = \frac{dv}{dt} = \frac{I_{charge}}{C} \tag{5.78}$$

$$slope_{discharge} = \frac{dv}{dt} = -\frac{I_{discharge}}{C} \tag{5.79}$$

If $I_{charge} = I_{discharge} = I_{FMC}$, then the triangular waveform has the same rise and fall times ($s = 0.5$).

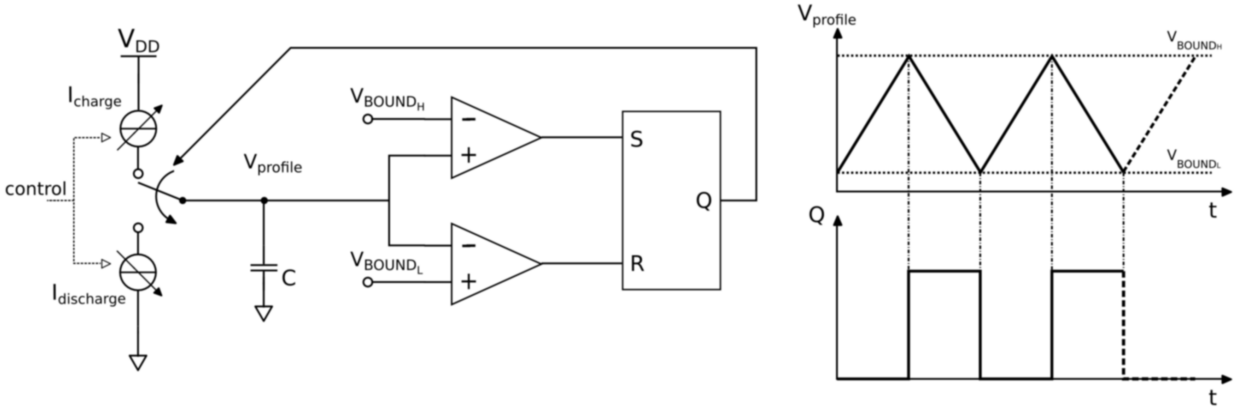


Figure 5.26: Concept schematic of a generic triangular relaxation oscillator

Only one current path has to be enabled at time. This could be achieved by a multiplexer circuit realized by simple digital pass transistors of minimum channel length. The complete concept schematic of the configurable profile generator is shown if Figure 5.27.

To adding the multi-slope profile feature you just need to add more current paths with different mirrored current values. In the implemented solution, there are two different charging paths and two others different discharging paths. A slope selector circuit, that senses the voltage waveform generated, selects the correct path to enable, by three digital signals that drive a multiplexer circuit. The different current values are generated by mirroring one single current I_{FMC} into four different paths: two in the high-side for charging the capacitor and two reported specullarly in the low-side for discharging the capacitor. The two current paths that compose each single side have two different mirror ratio (0.825, 1/0.825), to obtain two currents with values $I_{FMC} \cdot 0.825$ and $I_{FMC}/0.825$.

5.5.1 Slope selector circuit

The slope selector circuit, is composed by two parts. In the first one, the capacitor voltage $V_{profile}$ is compared with two threshold voltages (V_{BOUND_H} and V_{BOUND_L}), to generate the signal S_1, that reverses the direction of the capacitor current each time the capacitor voltage crosses a threshold level, enabling the two high-side current paths for charging the capacitor and enabling the two low-side current paths for discharging the capacitor. In the second part, instead, the capacitor voltage $V_{profile}$ is compared with others two threshold voltages (V_{CROSS_H} and V_{CROSS_L}), to generate S_2 and S_3 signals, that select the capacitor charging/discarging current, between the two current

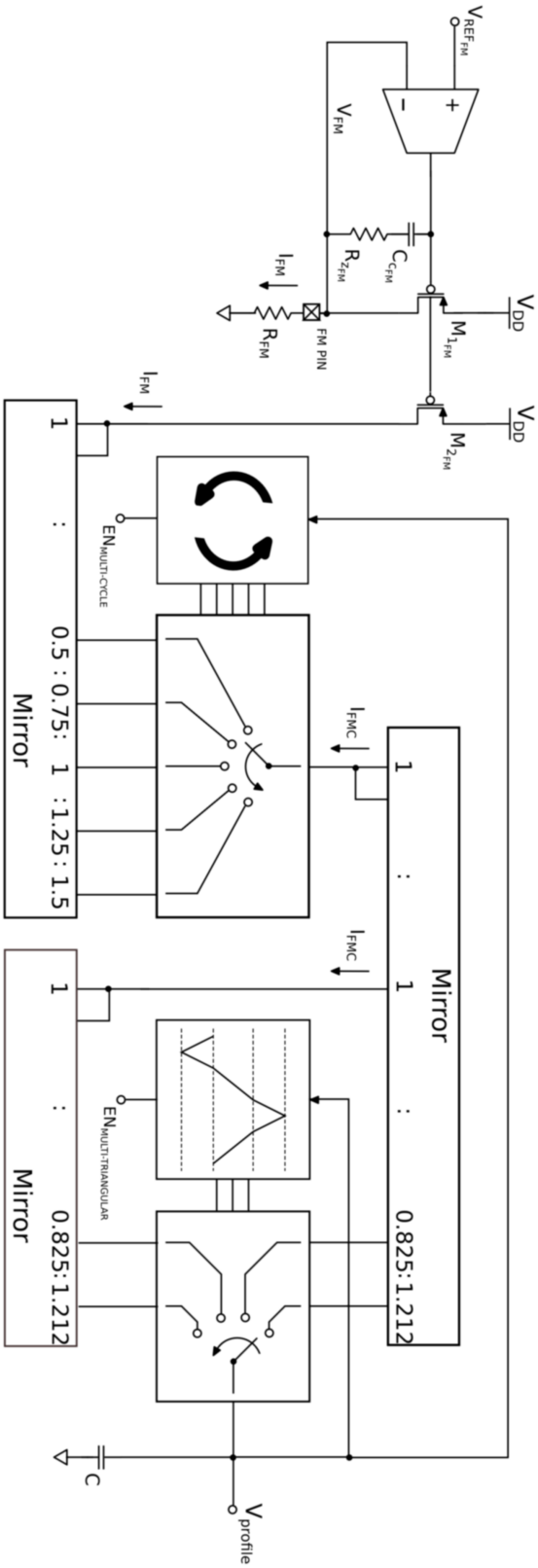


Figure 5.27: Concept schematic of the configurable profile relaxation oscillator

paths into the same side, each time the capacitor voltage crosses a threshold level. S_2 signal is `high` when $V_{CROSS_L} < V_{profile} < V_{CROSS_H}$ and `low` for the external voltage range. S_3 signal is the complementary of S_2 signal. The circuit are composed by only two simple low-power comparator (there is high timing requirements) and an `OR` digital port.

To achieve a better power consumption also the comparators can be disabled for certain times. They don't need to be both enabled at the same time: in the upper side of the voltage profile ($V_{profile} > V_{MIDDLE}$) only the upper threshold comparator is needed, while in the lower side ($V_{profile} > V_{MIDDLE}$) only the lower threshold comparator is needed. The digital signal S_1 that output from the SR-latch can be used, at this purpose, as enabling signal. With these tricks, the overall power consumption is quite reduced, and for almost all the time is due by the power consumption of only one low-power comparator.

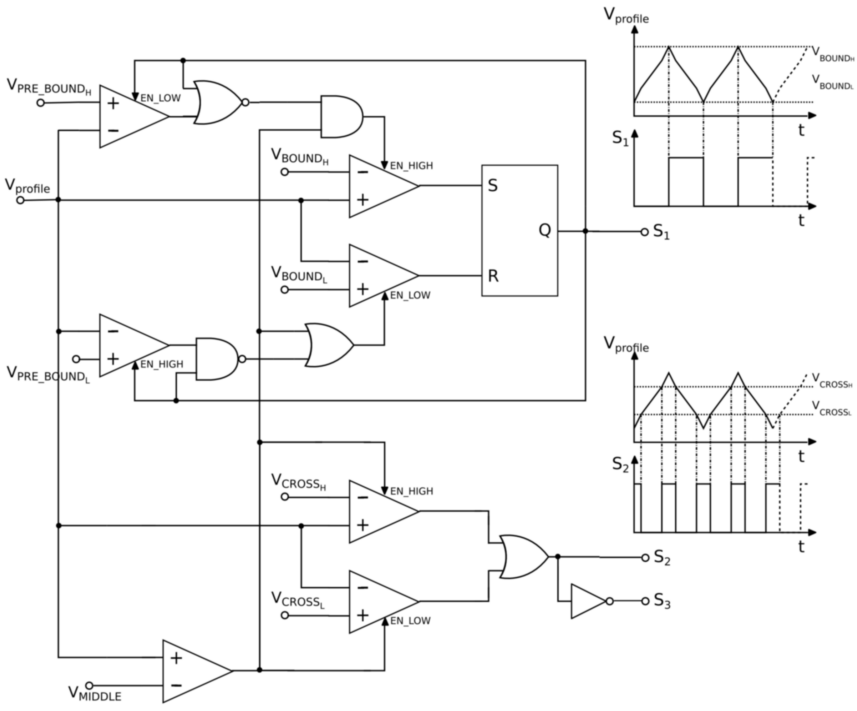


Figure 5.28: Concept schematic of the slope selector circuit

The part of the slope selector circuit that reverses the current direction is basically a *Schmitt-trigger*. The Schmitt trigger is a comparator circuit that incorporates positive feedback. When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output

retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis, and implies that the Schmitt trigger has some memory. Several approaches have been proposed to implement Schmitt trigger. Perhaps the most widely cited single-ended CMOS Schmitt trigger was proposed by Dokic []. Dokic's design piles four transistors between power and ground rails and is therefore not particularly attractive for applications where supply voltages are low. Threshold voltages depend on the ratio of geometry of cascode transistors and transistors which create positive feedback. A common drawback of the proceeding single-ended Schmitt triggers is that the hysteresis is set by the device dimensions and process parameters, and varies with process conditions. Schmitt triggers with tunable hysteresis are highly desirable in overcoming this deficiency. The main limitations of this tipology of circuits is the difficulty to obtain high-swing hysteresis, in fact as the threshold voltages became closer to the supply rails, as the ratio between the aspect ratio of the transistors became bigger. In our application we need threshold voltages very close to the rails, so this circuit solution isn't applicable. Therefore we adopted a SR-latch solution with two comparators: one with NMOS input devices for the lower threshold voltage comparision and one with PMOS input devices for the upper threshold voltage comparision.

To avoid any kind of amplitude modulation over the profile waveform generated, the switching from one state to another, have to be done faster as possible, otherwise the voltage waveform generated would present an varying voltage amplitude when multi-cycle modulation is toggled on, remember that in multi-cycle modulation mode, the current I_{fm} changes at each cycle. Thus, we need an high-speed comparator, such the one discussed in subsection 5.5.4. This kind of comparator have the drawback to have a large power consumption, therefore, in order to reduce it, the high-speed comparators are enabled only for a short time by other comparators but with a very low-power consumption, and therefore slower. Using this architecture, we need others reference voltages with a little lower swing ($V_{\mathrm{PRE\_BOUND}_H} < V_{BOUND_H}$ and $V_{\mathrm{PRE\_BOUND}_L} > V_{BOUND_L}$). To achieve a better power consumption also the pre-comparators can be disabled for certain times. They don't need to be both enabled at the same time: in the rising ramp (when the capacitor are charging) only the upper threshold comparator is needed, while in the falling ramp (when the capacitor are discharging) only the lower threshold comparator is needed. The digital signal S_1 that output from the SR-latch can be used, at this purpose, as enabling signal. With these tricks, the overall power

consumption is quite reduced, and for almost all the time is due by the power consumption of only one low-power comparator. Moreover, this result can be further improved with little changes.

5.5.2 Modulating current selector circuit

In order to add the multi-cycle feature, another feedback path is used. The capacitor voltage is compared with a threshold voltage, and a different capacitor charging/discharging current is selected, between five different values, each time the capacitor voltage crosses a threshold level. It is also possible to change the period of the modulating signal at the point of zero-crossing, or change the period at the point where the amplitude is minimum or maximum, or finally at a predeterminated value. Moreover, the number of variable periods is not limited to five, but it may be more or less as the number is larger than one. The different current values are generated by mirroring one single current I_{FM} into five different paths with five different mirror ratio (0.5, 0.75, 1, 1.25, 1.5), and obtaining five currents I_{FMC} with values $0.5 \cdot I_{FM}$, $0.75 \cdot I_{FM}$, I_{FM}, $1.25 \cdot I_{FM}$ and $1.5 \cdot I_{FM}$. The right current path is selected by a multiplexer circuit driven by five digital signal that comes from a shift register that changes its internal state each time the capacitor voltage crosses a threshold level.

The digital circuit that implement this function is shown in Figure 5.29. The five digital outputs $Q_{0,\ldots,4}$ are enabled to change state only if the `SET_LOW` input (which is directly connected to the external pin `MC`) is `low`, and therefore the chip works in multi-cycle modulation mode. Otherwise if `SET_LOW` is `high`, the chip works in normal periodic modulation mode and therefore only the output Q_4 is kept `high`, while all the others output are kept at `low` state. The circuit is basically a shift register composed by four D-flip-flops, which truth table is shown in Table 5.2.

CLOCK	D	TE	TI	Q
⇑	-	-	-	Q(t-1)
⇓	0	0	-	0
⇓	1	0	-	1
⇓	-	1	0	0
⇓	-	1	1	1

Table 5.2: Truth table of the D-flip-flop used in Figure 5.29

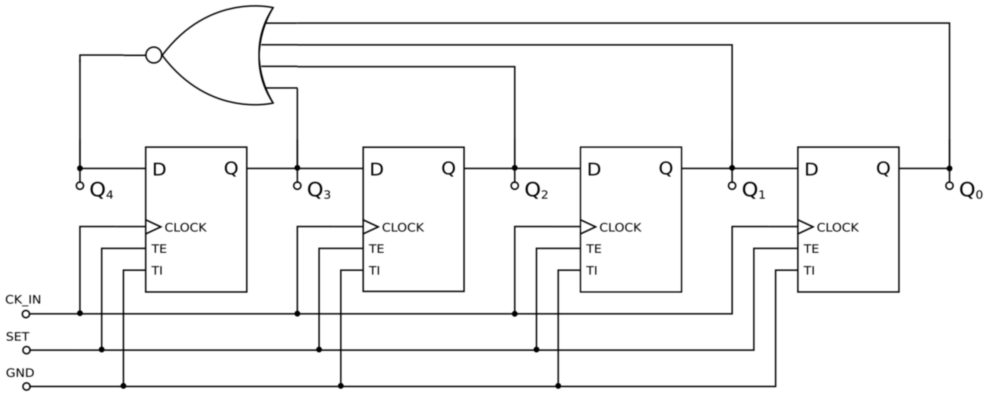


Figure 5.29: Modulating current selector schematic

5.5.3 Sizing of the modulating frequency V2I converter

The circuit shown Figure 5.30 converts a costant voltage reference, in a current, which set the oscillation frequency of the triangular oscillator which is the profile generator's core. The current value is determined by the external resistor R_{FM} and the voltage between GND and the FM pin.

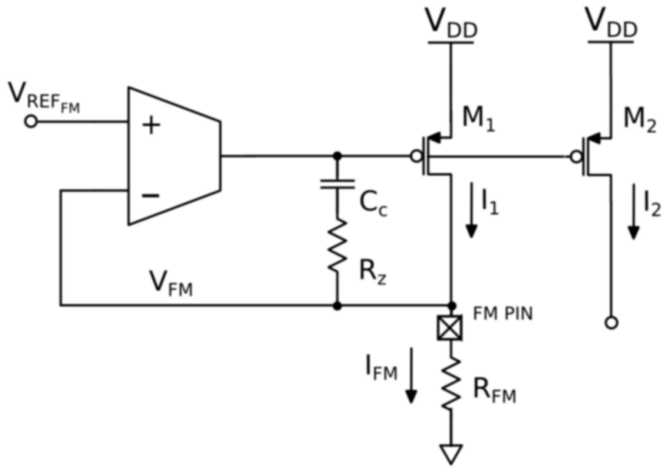


Figure 5.30: Concept schematic of the voltage-to-current converter that only set the frequency of the periodic modulation waveform.

The voltage on the SET pin is forced to exactly track the converter input voltage $V_{REF_{FM}}$ due to high voltage gain of the OTA and by the PMOS transistor M_3 ($V_{FM} = V_{REF_{FM}}$). The reference input voltage is a costant signal generated by a precise bandgap circuit, and has a value of $1.25\,V$. Therefore OTA used is a simple single stage amplifier with NMOS input differential pair.

The R_{FM} resistor connected between GND and the SET pins locks together the SET pin voltage and the I_{FM}. The I_{FM} current flowing through the transistor M_3 imposes a fixed gate-source voltage on boths M_3 and M_4 transistors. In this way the drain current I_{D_4} of PMOS M_4 tracks I_{FM}.

This circuit block don't need a stringent sizing as in the previous part. Here, the voltage to convert is costant and the I_{FM} have a limited range of values. Therefore, there isn't bandwith requirements, and don't need, as previously, to add a costant current for stability. The only requirements are on the sizing of PMOSs M_3 and M_4 that must take account of the condition to mantain they in saturation region, the ratio of the sizes of the transistors can be derived as:

$$\left(\frac{W}{L}\right)_{1,2} > \frac{\frac{V_{FM}}{R_{FM}}}{\frac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{FM})^2} = \frac{I_{FM}}{\frac{\mu_p C_{ox}}{2} \cdot (V_{DD} - V_{FM})^2} \tag{5.80}$$

In order to size the Miller compensation network, just need to use equations 5.69 and 5.71.

5.5.4 High Speed Comparator

The comparator basically can be decomposed into three stages. The stages are input stage (preamplifier), decision stage (latch), output stage. The input stage converts the input voltages to currents level needed to drive the decision stage. The decision stage is a non-linear cross-coupled circuit which switch from one state to another, the feedback speed up the switching. The output stage buffer the decision stage and convert the signal level to digital signal level. The complete schematic of the comparator is shown in Figure 5.31.

Preamplifier The input stage is a differential amplifier with a pull-up network as load. The pull-up network can use passive loads like resistors (poly, diffusion, well, and etc...), or diode connected active loads, see Figure 5.32. NMOS pull-up suffers from body effect, affecting gain setting accuracy, PMOS pull-up has no body effect, but is subject to P/N matching. Lastly, gain accuracy is the worst for resistive pull-up as resistors (poly, diffusion, well, and etc.) don't track transistors. To obtain more gain are added in parallel to the diode connected PMOS (M_3 and M_4) a current generator I_p, that diverts current away from PMOS diodes. The drawbacks are that I_p needs a biasing circuit, and M_3 and M_4 may cut off for large input voltages, resulting in long recovery time. The best solution is to use the *Bult's preamplifier* where the NMOS differential pair

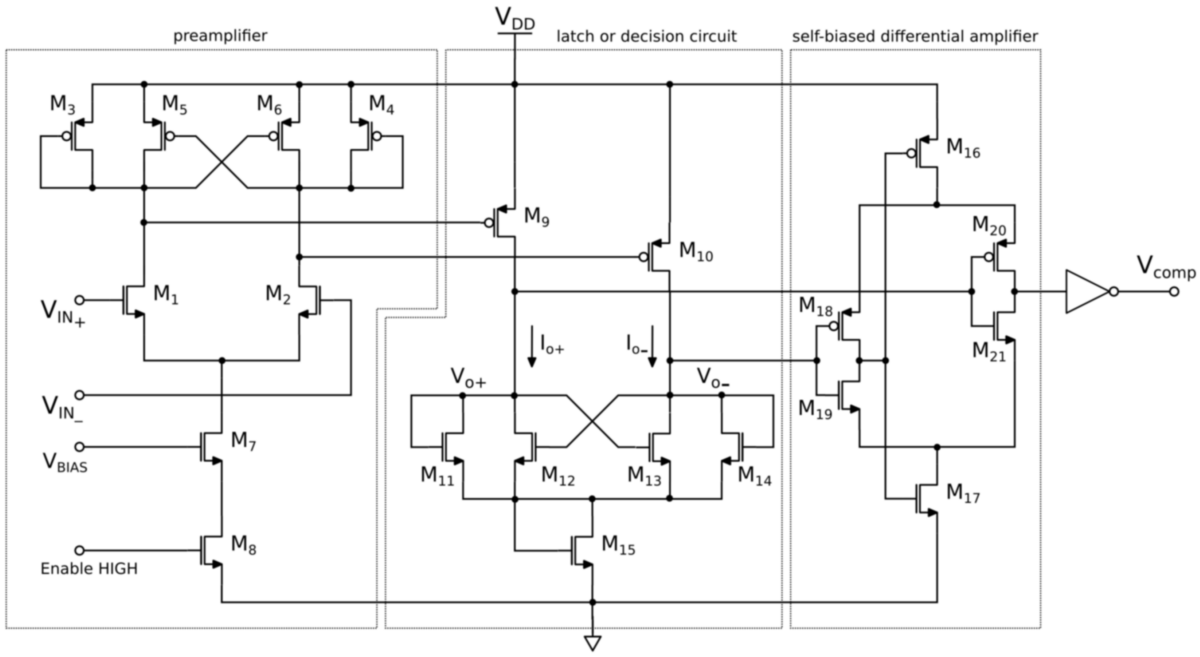


Figure 5.31: Concept schematic of high-speed comparator

are loaded with PMOS diodes and a positive feedback crossed PMOS pair. In this way we obtain an high differential-mode gain, and a low common-mode gain (see Figure 5.33 for the small-signal equivalent circuit for the differential- and common-mode), therefore also a very good *common-mode rejection ratio* (CMRR). The only concern, is that $\left(\frac{W}{L}\right)_{3,4} > \left(\frac{W}{L}\right)_{5,6}$ needs to be ensured for stability.

- Gain with NMOS pull-up loads:

$$A_V = -\frac{g_{m_1}}{g_{m_L}} = -\sqrt{\frac{(W/L)_1}{(W/L)_L}} \tag{5.81}$$

- Gain with PMOS pull-up loads:

$$A_V = -\frac{g_{m_1}}{g_{m_L}} = -\sqrt{\frac{\mu_n}{\mu_p} \cdot \frac{(W/L)_1}{(W/L)_L}} \tag{5.82}$$

- Gain with resistor pull-up loads:

$$A_V = -g_{m_1} \cdot R_L \tag{5.83}$$

- Gain with the parallel of diode connected PMOSs and current generators I_p:

$$A_V = -\frac{g_{m_1}}{g_{m_3}} = -\sqrt{\frac{\mu_n}{\mu_p} \cdot \left(\frac{I_{tail}/2}{I_{tail}/2 - I_p}\right) \cdot \frac{(W/L)_1}{(W/L)_3}} \tag{5.84}$$

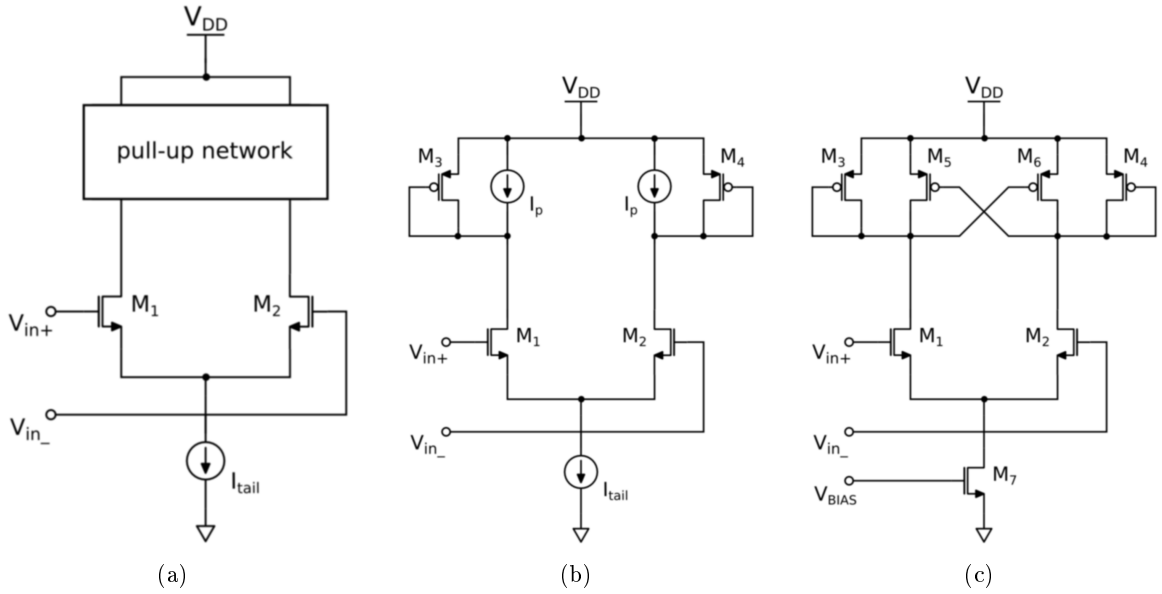


Figure 5.32: (a) Preamplifier with pull-up network (resistors or NMOS diodes or PMOS diodes). (b) Preamplifier with PMOS diodes and current generator network. (c) Preamplifier with positive feedback.

- Differential-mode gain of the Bult's preamplifier:

$$A_V^{dm} = -g_{m_1} \cdot \left[\frac{1}{g_{m_3}} // \left(-\frac{1}{g_{m_5}} \right) // r_{o_1} // r_{o_3} // r_{o_5} \right] \approx -\frac{g_{m_1} r_{o_1}}{3} \tag{5.85}$$

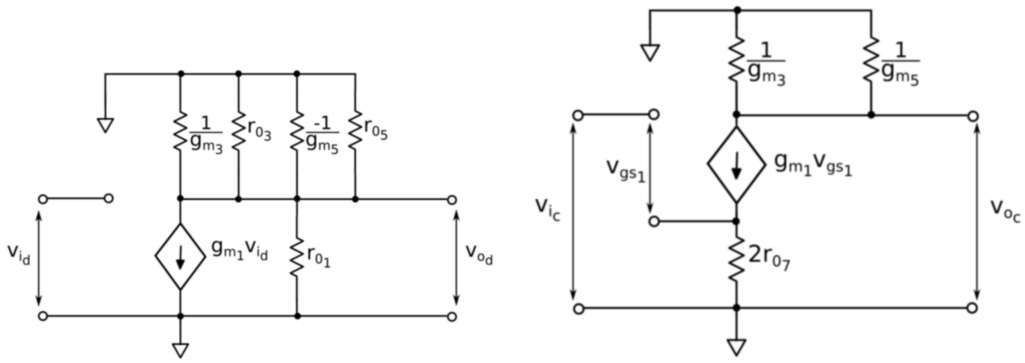
Common-mode gain of the Bult's preamplifier:

$$A_V^{cm} = -\frac{g_{m_1}}{1 + 2 g_{m_1} r_{o_7}} \cdot \left(\frac{1}{g_{m_3}} // \frac{1}{g_{m_5}} \right) \approx -\frac{1}{2\left(g_{m_3} + g_{m_5}\right) r_{o_7}} \tag{5.86}$$

The sizes of M_1 and M_2 are set by considering the diffirential amplifier transconductance and the input resistance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of M_1 and M_2. We will concentrate on speed in the design, and therefore we will set the channel lengths of the MOSFETs to the minimum value $0.8\mu m$.

The input voltages V_{in_+} and V_{in_-} are converted to output currents i_{o_+} and i_{o_-}, used to drive the decision circuit. By symmetry the tail current I_{tail} is split evenly between the two sections. Transistor M_1 converts the V_{GS_1} to current. To determine the total current i_{o_+} the equivalent includes the biasing current of $I_{tail}/2$.

Latch or decision circuit The decision circuit is the heart of the comparator and should



(a) (b)

Figure 5.33: (a) Preamplifier differential-mode small-signal equivalent circuit. (b) Preamplifier common-mode small-signal equivalent circuit.

be capable of discriminating $[mV]$ level signals. The latch is a bistable cross coupled circuit, that uses positive feedback from the cross-gate connection of M_{12} and M_{13} to increase the gain of the decision element. The state is determined by the magnitude of the input currents. If $i_{o_-} \gg i_{o_+}$ M_{12} and M_{14} are ON and M_{11} and M_{13} are OFF. This give $i_{o_-} = i_{D_{13}} + i_{D_{14}} = i_{D_{14}}$ and $i_{o_+} = i_{D_{11}} + i_{D_{12}} = i_{D_{12}}$. Under these conditions, $V_{o_+} = V_{DS_{12}} \approx 0V$ (M_{12} in ON) and V_{o_-} is determined by the value of $V_{GS_{14}}$ when $i_{D_{14}} = i_{o_-}$. That is:

$$i_{o_-} = i_{D_{14}} = \frac{\beta_{M_{14}}}{2} \cdot (V_{GS_{14}} - V_{th_n})^2 = \frac{\beta_A}{2} \cdot \left(V_{o_-} - V_{th_n}\right)^2 \tag{5.87}$$

where $\beta_{M_{11}} = \beta_{M_{14}} = \beta_A$.

To change state, increase i_{o_+} hence decrease i_{o_-} ($i_{o_-} = I_{tail} - i_{o_+}$). This will cause V_{o_-} to decrease, too. $V_{o_-} = V_{GS_{12}}$, hence the decrease V_{o_-} will eventually shut off M_{12}. The value of V_{o_-} just before the M_{12} shut off is given by:

$$i_{o_+} = i_{D_{12}} = \frac{\beta_{M_{12}}}{2} \cdot (V_{GS_{12}} - V_{th_n})^2 = \frac{\beta_B}{2} \cdot \left(V_{o_-} - V_{th_n}\right)^2 \tag{5.88}$$

where $\beta_{M_{12}} = \beta_{M_{13}} = \beta_B$. This will give:

$$\beta_A \cdot i_{o_+} = \beta_B \cdot i_{o_-} \qquad and \qquad V_{o_-} = \sqrt{\frac{2 \cdot i_{o_-}}{\beta_A}} + V_{th_n} \tag{5.89}$$

Re-analyzing the decision circuit starting with the other state. The value V_{o_+} is given by:

$$V_{o_+} = \sqrt{\frac{2 \cdot i_{o_+}}{\beta_A}} + V_{th_n} \tag{5.90}$$

That is, the maximum value of V_{o_-} and V_{o_+} can both be bounded to less than $2 \cdot V_{th_n}$, by adjusting β_A. Adjusting β_A and β_B the decision circuit can show an hysteresis, which trigger voltage is given by:

$$V_{TH} = V_{in_-} + V_T \tag{5.91}$$

$$V_{TL} = V_{in_-} - V_T \tag{5.92}$$

where:

$$V_T = \frac{2}{g_m} \cdot \left(i_{o_+} - \frac{I_{tail}}{2} \right) = \frac{I_{tail}}{g_m} \cdot \left(\frac{2 \cdot i_{o_+}}{i_{o_+} + i_{o_-}} - 1 \right) = \frac{I_{tail}}{g_m} \cdot \left(\frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \right) \tag{5.93}$$

If $\beta_A = \beta_B$ there is no hysteresis. The maximum output voltage of the decision circuit Vo+(max) is obtained as:

$$V_{o_{+MAX}} = \sqrt{\frac{2 \cdot I_{tail}}{\beta_A}} + V_{th_n} \tag{5.94}$$

Lastly the MOSFET M_{15} is added in series with the decision circuit to increase the average voltage out of the decision circuit, to avoid problems in connecting the decision circuit directly to the output buffer.

Output Buffer The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit used as an output buffer in our basic comparator design is a *self-biasing differential amplifier*.

This circuit is derived from two well-known conventional CMOS amplifiers (respectively with NMOS and PMOS input devices) that use current mirror as active load. The current mirror loads from both amplifiers are deleted and the corresponding gates and drains of the input devices are connected together. This circuit has a PMOS and a NMOS current sources which must be biased to achieve identical current. Any differences would results in amplifier output shifts. With two separate bias voltages and different transistors types, this is not a simple task. To solve this, the two bias-voltage inputs are connected together to an internal node (see Figure 5.31). With this bias connection, any variations in processing parameters that shift the nominal operating point, is corrected by shifting the bias voltage by negative feedback.

M_{16} and M_{17} operate in the linear (ohmic) region. With M_{16} and M_{17} operating in the linear region, the buffer can provide output switching currents that are significantly greater than its quiescent current. In contrast, conventional CMOS differential amplifiers cannot provide switching currents that exceed the quiescent current set by the current-source device, which operates in the saturation region.

5.6 Frequency Divider

A frequency divider, also called a clock divider or scaler or prescaler, is a circuit that takes an input signal of a frequency, f_{IN}, and generates an output signal of a frequency:

$$f_{OUT} = \frac{f_{IN}}{n} \tag{5.95}$$

where n is an integer. For power-of-2 integer division, a simple binary counter can be used, clocked by the input signal. The least-significant output bit alternates at $\frac{1}{2}$ the rate of the input clock, the next bit at $\frac{1}{4}$ the rate, the third bit at $\frac{1}{8}$ the rate, etc. An arrangement of flip-flops are a classic method for integer-n division. Such division is frequency and phase coherent to the source over environmental variations including temperature. The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of four of these, such system would be a divide-by-16.

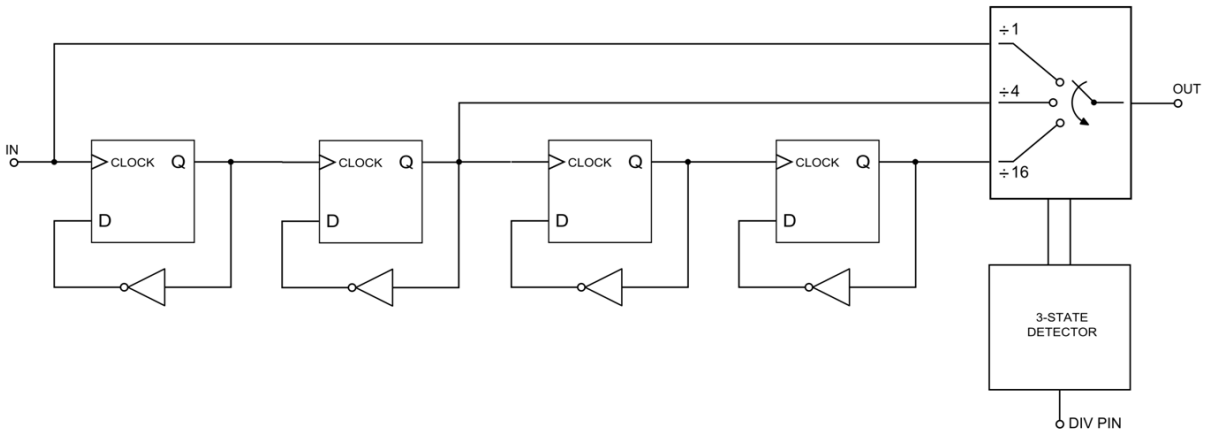


Figure 5.34: Concept schematic of the frequency divider circuit

The divide by two circuit employs one logic D-type flip-flop element. Simply by entering the pulse train into the clock input, and connecting the $\overline{Q}$ output to the D input, the output signal divided by two can then be taken directly from the Q output of the D-type flip-flop.

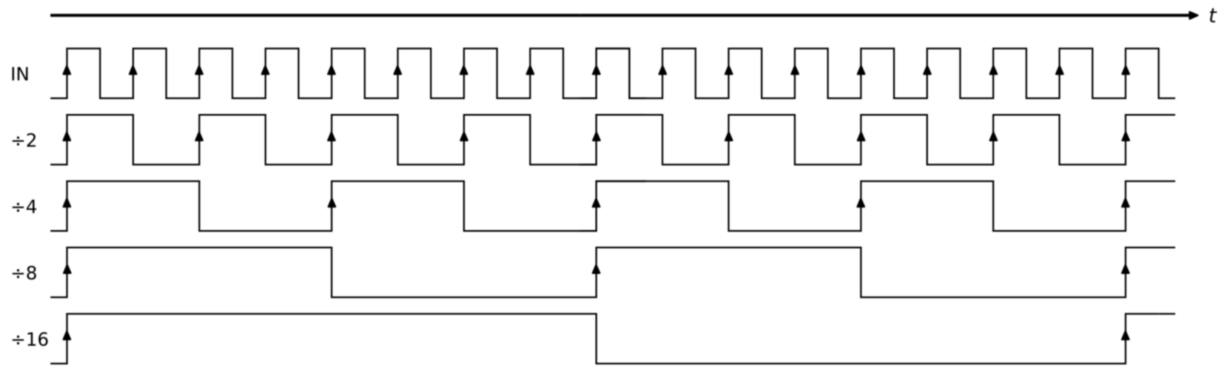


Figure 5.35: Time signals from the various stages of the frequency divider circuit

The circuit operates in a simple way. The incoming pulse train acts as a clock for the device, and the data that is on the D input is then clocked through to the output. To see exactly how the circuit works it is worth examining what happens at each stage of the waveforms shown below. Take the situation when the Q output is `high`. This means that the $\overline{Q}$ output will be `low`. This data is clocked through to the output Q on the next positive going edge from the incoming pulse train on the clock input. At this point the output changes from `high` to `low` state. At the next positive going clock pulse, the data on the $\overline{Q}$ output is again clocked through. As it is now `high` (opposite to the Q output), this is transferred to the output, and the output again changes state. It can be seen that the output of the circuit only changes state on the positive going edges of the incoming pulse clock stream. Each positive edge occurs once every cycle, but as the output of the D-flip-flop requires two changes to complete a cycle, it means that the output from the D-type circuit changes at half the rate of the incoming pulse train. In other words it has been divided by two.

Chapter 6

Simulation results and measurements

This chapter is dedicated to present the simulation results from the spread spectrum clock generator concept designed in the previous chapter. The chapter is structured into different sections. Each of these shows the simulation of the parameters characterizing each circuital block that compose the top SSCG concept. In addition in the last section the simulation results of the whole top SSCG concept, are shown.

6.1 Master CCO

To achieve optimal circuit performance, one should measure and evaluate several CCO characteristics or parameters under varying conditions. As an example,

VCOs suffer from trade-offs between speed, power dissipation, and noise. The VCO measurements in the following sections are calculated using SpectreRF in the analog design environment. The parameters that are covered in this section are listed and described below.

Tuning Sensitivity and Linearity

One fundamental parameter is the plot of CCO output frequency versus tuning current. An extension of this parameter is tuning sensitivity, which is the differential of the output frequency versus tuning current curve. The slope change as a function of frequency is of paramount importance since this is a critical design parameter. Tuning sensitivity is defined as the frequency change per unit of tuning current.

Ideally tuning sensitivity would be constant but in practice this is generally not the case. Plot CCO frequency measurements against tuning current. The slope of this characteristic is the tuning voltage sensitivity which you can calculate at different tuning current.

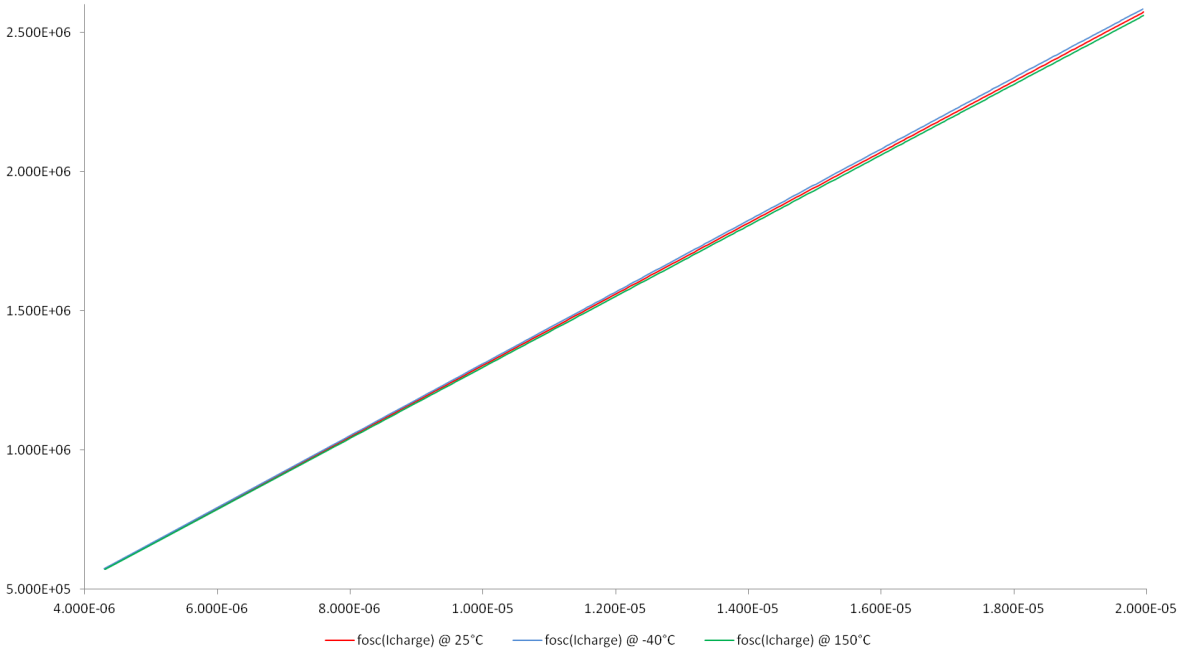


Figure 6.1: Master CCO output frequency versus tuning current $f_{osc}\left(I_{charge}\right)$ at different operating temperatures ($-40°C$, $25°C$ and $150°C$)

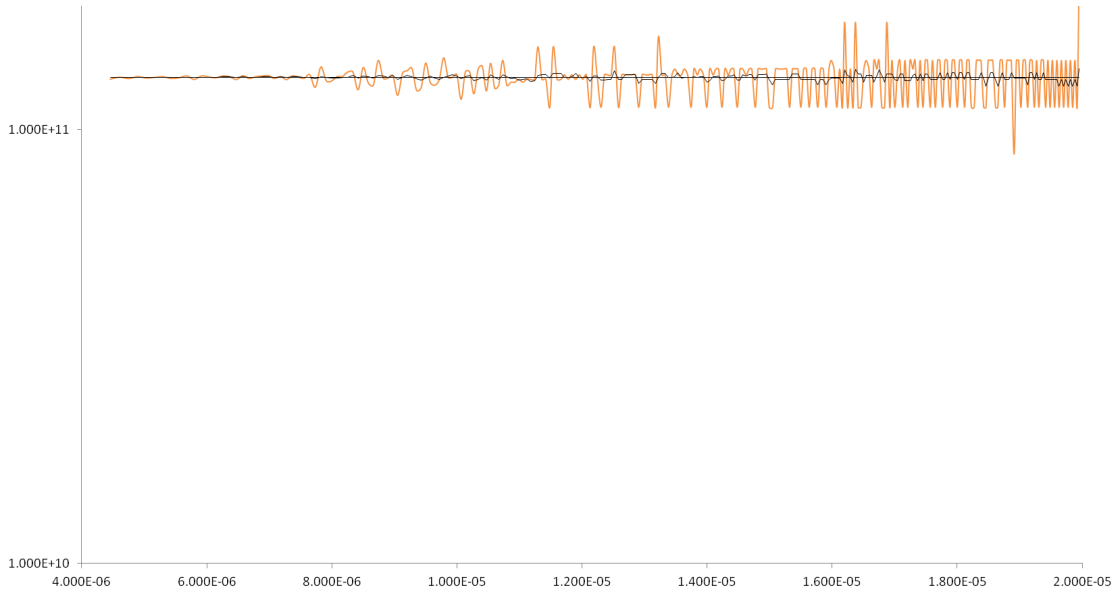


Figure 6.2: Tuning sensitivity of the master CCO, which is the differential of the output frequency characteristic $f_{osc}\left(I_{charge}\right)$ versus tuning current curve I_{charge}. $S_{tune} = \frac{\partial f_{osc}\left(I_{charge}\right)}{\partial I_{charge}}$

Phase Noise

Phase noise is random phase variation in the VCO's output oscillating signal. Close to the carrier phase noise is mainly composed of flicker noise. The flicker noise measured in a VCO is generated only by the active devices, such as the transistor and the tuning diode. The phase noise is measured at distances from 1 KHz off the carrier to several megahertz (MHz) off the carrier in a 1-Hz bandwidth. Phase noise is the ratio of the output power divided by the noise power at a specified value and is expressed in dBc/Hz. Phase noise is the most significant source of noise in oscillators, which makes it a crucial measurement.

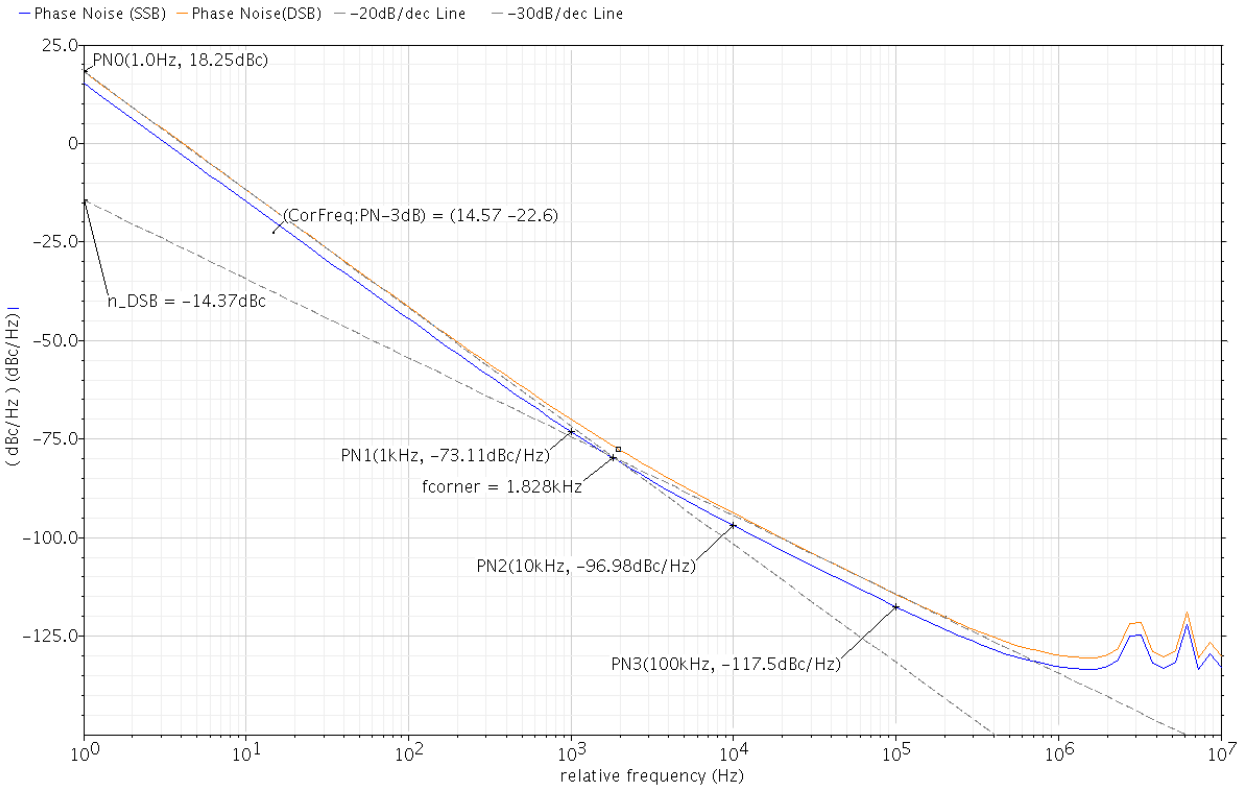


Figure 6.3: Phase noise of the master CCO

To perform a noise analysis, SpectreRF must first compute the steady-state solution of the circuit with its periodic steady state (PSS) analysis. For direct simulation using SpectreRF, simply configure the simulator to perform a PSS analysis followed by a periodic noise (PNoise) analysis. The beat frequency of the PSS analysis should be set to be the same as the reference frequency. The PSS stabilization time (tstab) should be set long enough to allow the VCO's output to oscillate.

Set up a PSS analysis with a Beat Frequency = 1.5 MHz; Number of Harmonics = 3; errpreset = conservative.

Set up a swept Pnoise analysis with a Sweeptype = relative; Relative Harmonic = 1; Frequency Sweep Range (Start = 1, Stop = 10 M); set Sweep type = logarithmic; Number of Steps = 100; and Maximum sideband = 15 for an accurate result which take into account the noise folding.

If the VCO with actual frequency divider is to be simulated, the output of the oscillator will be at the M^{th} harmonic, where M is the divide ratio. The PNoise output offset frequency need to be relative to the M^{th} harmonic.

Long Term Jitter

Long term jitter characterizes the variation in the accumulated width of a large number of clock periods. If a periodic system has a reference time point, we can consider all other events in relation to that time point. For a driven system it could be the crossing by the periodic input signal a particular threshold value. For an autonomous system which is rather self-referenced, the first crossing during the observation time could be used. We expect that the periodic output signal will generate an ideal sequence of events, separated by the period T.

If two transitions are separated in time by k cycles or periods, the standard deviation of the length of k cycles from nominal is computed using the following sequence

$$\left\{J_c^i(kT)\right\} = \{t_{i+k} - t_i - kT\} \tag{6.1}$$

It is characterized by the standard deviation that is also referred as k-cycle jitter or k-period jitter

$$J_c^i(kT) = \sqrt{var\left(t_{i+k} - t_i\right)} \tag{6.2}$$

If the observation time is long and involve many periods, k-cycle jitter will represent the *long term jitter*. For a stationary or T-cyclostationary noise, the metrics will not depend on the location of the events, which is defined by i. Different system will exhibit a variety of the long term jitter behavior as the time of observation increases. Open loop VCO would accumulate the jitter with time and increase as a square root of time for the white noise dominated oscillator. In PLLs, the variation in the clock edges over the long time interval will be partially tracked out by the negative feedback of the loop. The accumulation of the jitter over many periods will be limited by the loop

bandwidth. In general, noise frequency content, system dynamics, type of the measurement and the observation time will define the variation of the long term jitter with time.

We will use SpectreRF to measure the long term jitter. To measure the jitter we will setup PSS and PNoise analyses. The PSS analysis is a regular autonomous simulation. First, we use periodic steady state analysis to find the periodic trajectory or the large signal periodic solution of the system. Next, we use periodic noise analysis to find the phase noise and provide all the information we need to extract the jitter. In our case, we setup PNoise analysis type "jitter". Only if the M divider is attached as the load, PSS will use the divider output to find the period of the large signal solution. The PSS fundamental will be M times smaller then CCO output frequency. The PNoise analysis form is used to setup the jitter measurements. The output is the output of the CCO.

PNoise frequency sweep has maximum set for the half of PSS fundamental. This will be the highest frequency one need for the measurements, beyond that value, certain assumption in phase noise computation of SpectreRF could break down. The minimum frequency is usually defined to account for the longest expected observation time or limited by the system bandwidth.

The PNoise simulation allows us to plot phase noise power spectral density and we will use it to compute the long term jitter. It is helpful to plot phase noise prior to beginning jitter measurements. One can verify the noise frequency content and it also helps to decide about which integration limits to use, since at lower frequency offsets, the phase noise will grow boundless, it could be confusing at first.

Another helpful feature is the $-20\,dB/dec$ curve which could be placed on the phase noise plot at any frequency. The slope of $-20\,dB/dec$ assistant let us to distinguish the regions of the $1/f^3$, $1/f^2$ and $1/f$ phase noise PSD. Using "Calculator" also a "-30dB/dec" assistant curve can be plotted. This assistant curve could be placed on the phase noise curve at very low frequencies. From the intersection on the two lines a corner frequency f_{corner} could be detected. This corner frequency divides a flicker noise region from a white noise region.

Once the phase noise content is known, there are two important parameters that have to be selected for the long term jitter computation: the number of cycles and the minimum frequency of the integration. The maximum frequency doesn't affect the long term jitter computation since the high frequency content of phase noise PSD will be much lower then at small frequency, especially

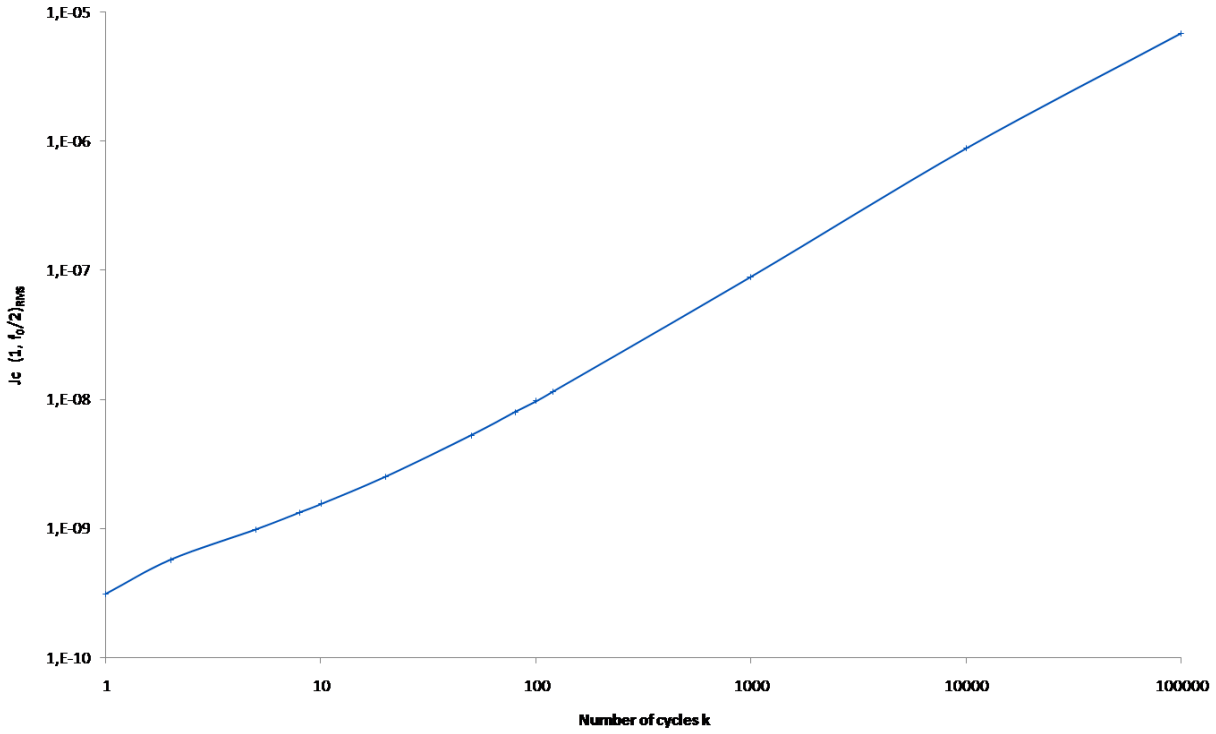


Figure 6.4: k-cycle jitter $J_c(k)$ as function of the number of cycles k with $f_{min} = 1Hz$.

in the presence of the flicker noise. The time of observation is a typical factor that is used to select the "Number of Cycles" k and the "Start Frequency". For lowest frequency of phase noise that can be observed, we have to use the jitter measurement (observation) time T_o. The same information is used to define the number of cycles for jitter computation:

$$f_{min} = \frac{1}{T_o} \qquad , \qquad k = \frac{f_{osc}}{f_{min}} \tag{6.3}$$

The plot of the phase noise in Figure 6.3, indicates the presence of the flicker noise, just below the f_{corner}. This frequency can be used as f_{min}. Using the Direct Plot, the jitter value is plotted for the nominal and a few other values of the bandwidth: 20k, 100k and 500k. The noise is mostly white PM noise and the jitter increases as a square root of observation time, according the to theory. In addition to the long term jitter, the single period jitter is plotted. It confirms that the slow, low frequency components of the phase noise do not affect its value, making the selection of the minimum integration limit less of a problem.

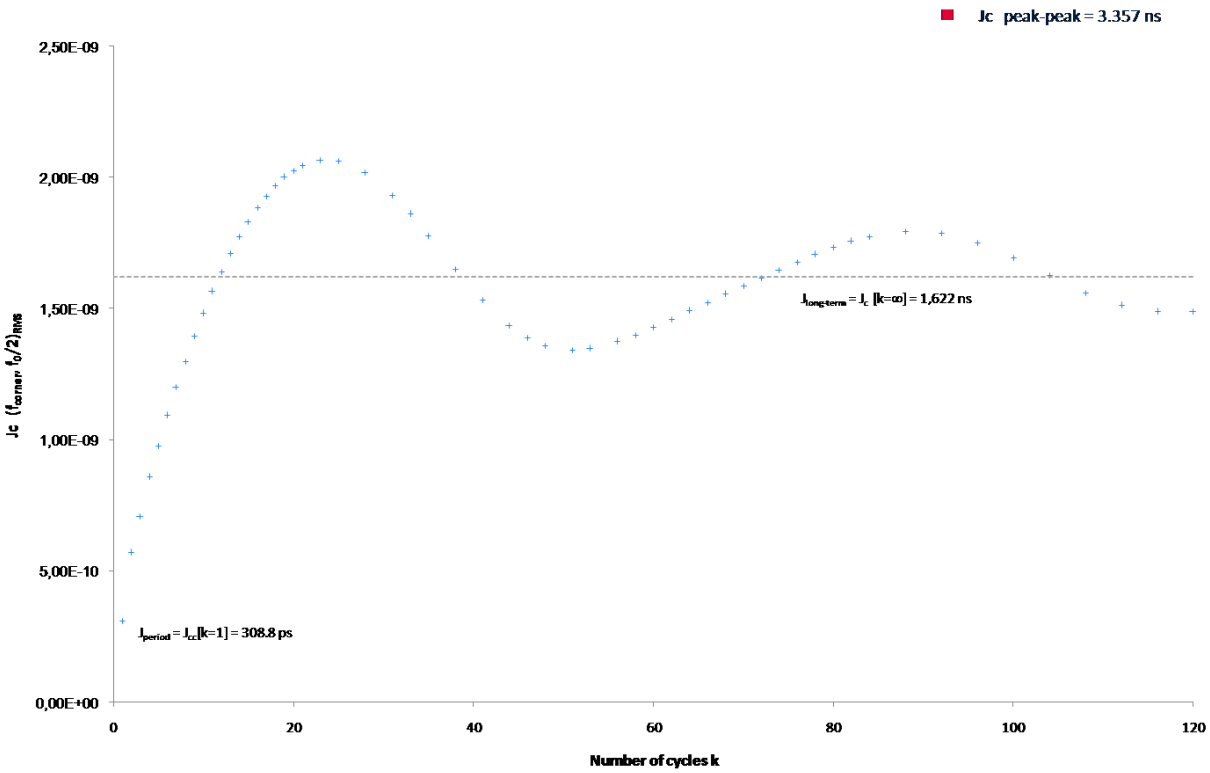


Figure 6.5: k-cycle jitter $J_c(k)$ as function of the number of cycles k with $f_{min} = f_{corner}$.

6.2 Voltage to current converter

The voltage-to-current (V2I) converter has to show good linearity characteristic and a good temperature stability. Figure 6.7 shows the transcharacteristic of the voltage to current converter at different operating temperatures. The linearity is keeped for almost all the voltage sweep range, only at extremes there is a distortion on the transcharacteristic. Moreover, this distortion non-linearity effect have a positive influence on the final spreading of the spectrum, because it avoid the formation of peaks on the side-band harmonic defining the window after modulation.

The V2I converter block is composed by two V2I converters that lets the configuration of the SSCG chip by two external resistors. Each of these converters is a feedback system that has to be opportunily compensated for stability purpose. A verification of a sufficient phase margin (PM) was done for several operating conditions for each converter, through STB simulations in Cadence, and it was found that Phase Margin never drops below 24° for the V2I converter that sets the spreading percentage, and for the one that sets the carrier frequency f_c Phase Margin never drops below 35°.

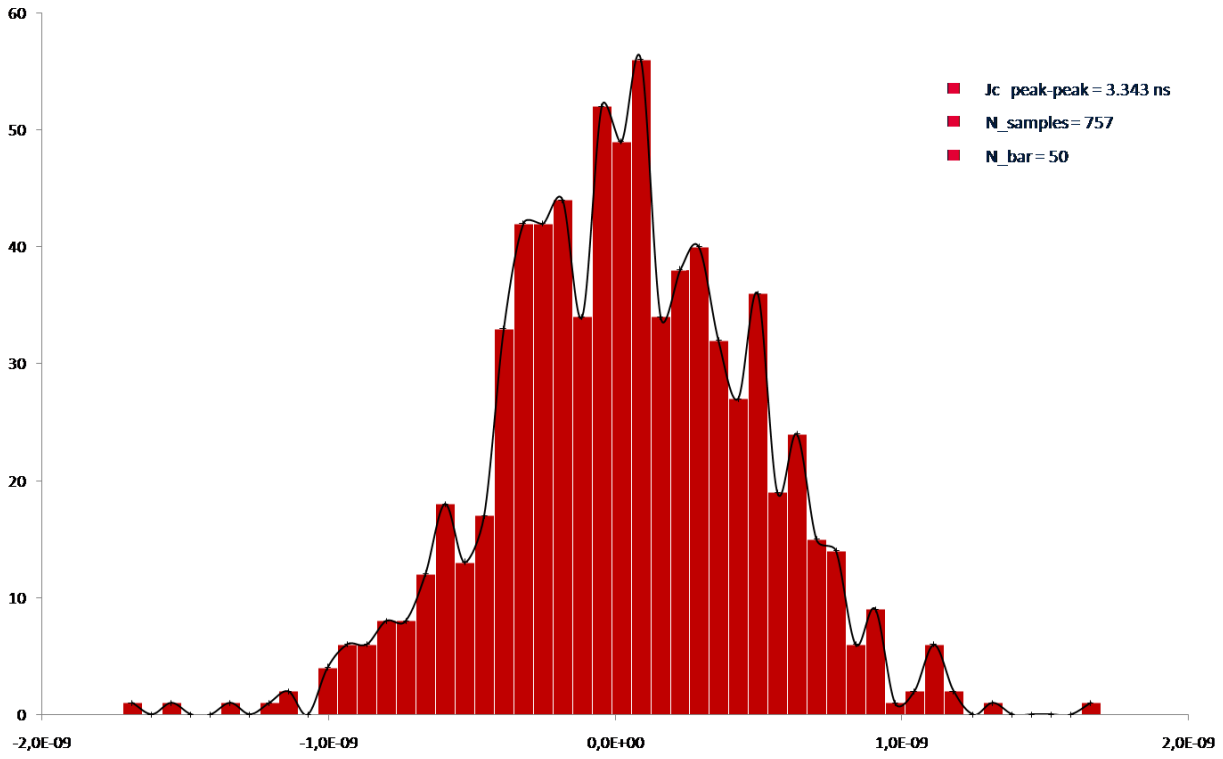


Figure 6.6: Long-term jitter after $2ms$.

Figure 6.8 shows a typical Bode diagram simulation result with Gain and Phase Margins.

6.3 Profile Generator

The profile generator is a modified triangular oscillator with a V2I converter that lets the configuration of the modulating frequency f_m to the user. A verification of a sufficient phase margin (PM) was done for several operating conditions, through STB simulations in Cadence, and it was found that Phase Margin never drops below 37°.

Figure 6.9 shows how to set the value of the external resistor R_{FM} according to the modulation frequency f_m at different operating temperatures ($-40°C$, $25°C$ and $150°C$), in triangular and multi-slope triangular operation modes. As one can see the multi-slope triangular profile frequency is lower than triangular profile frequency for the same value of R_{FM}.

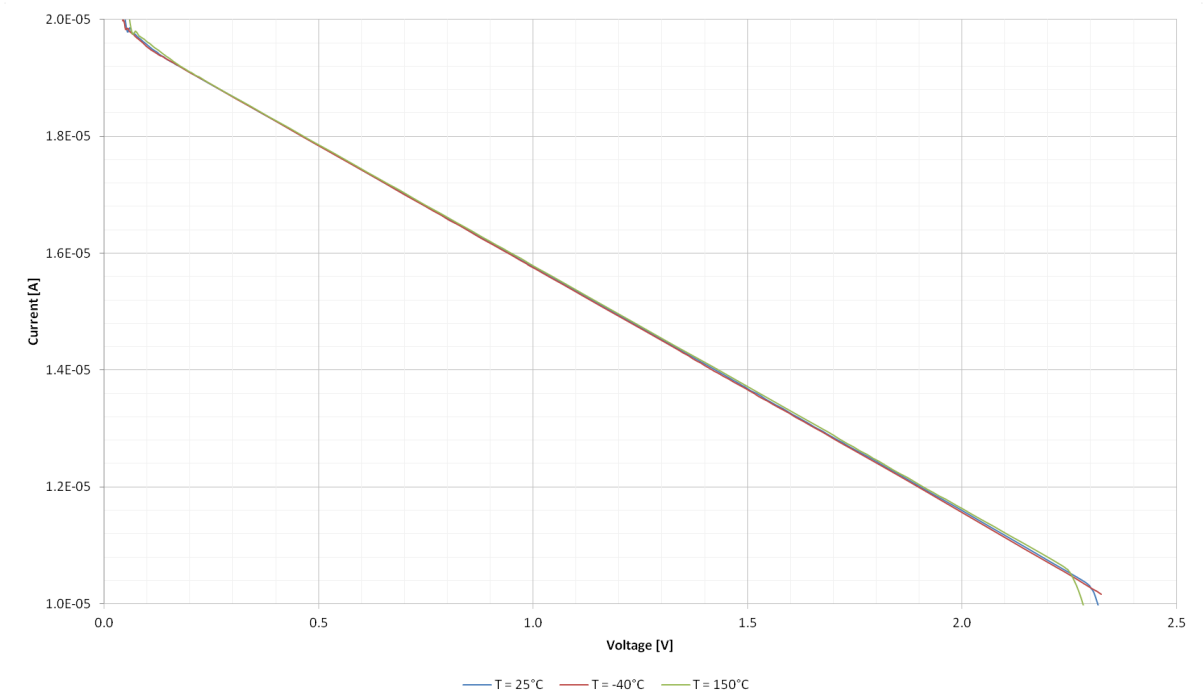


Figure 6.7: Transcharacteristic of the voltage to current converter at different operating temperatures.

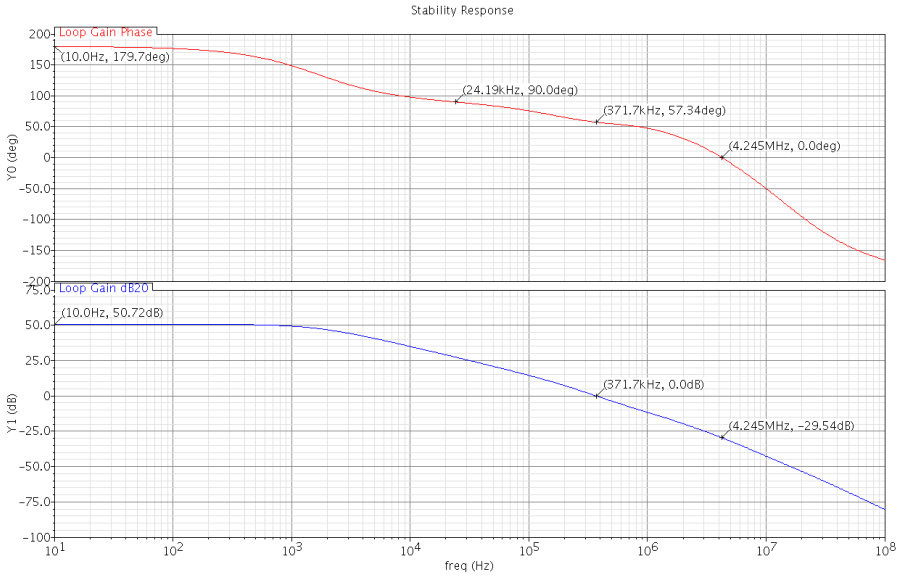


Figure 6.8: Bode diagram of spreading percentuage configurator at maximum current (V_{MOD} at its maximum value, and R_{MOD} at its minimum).

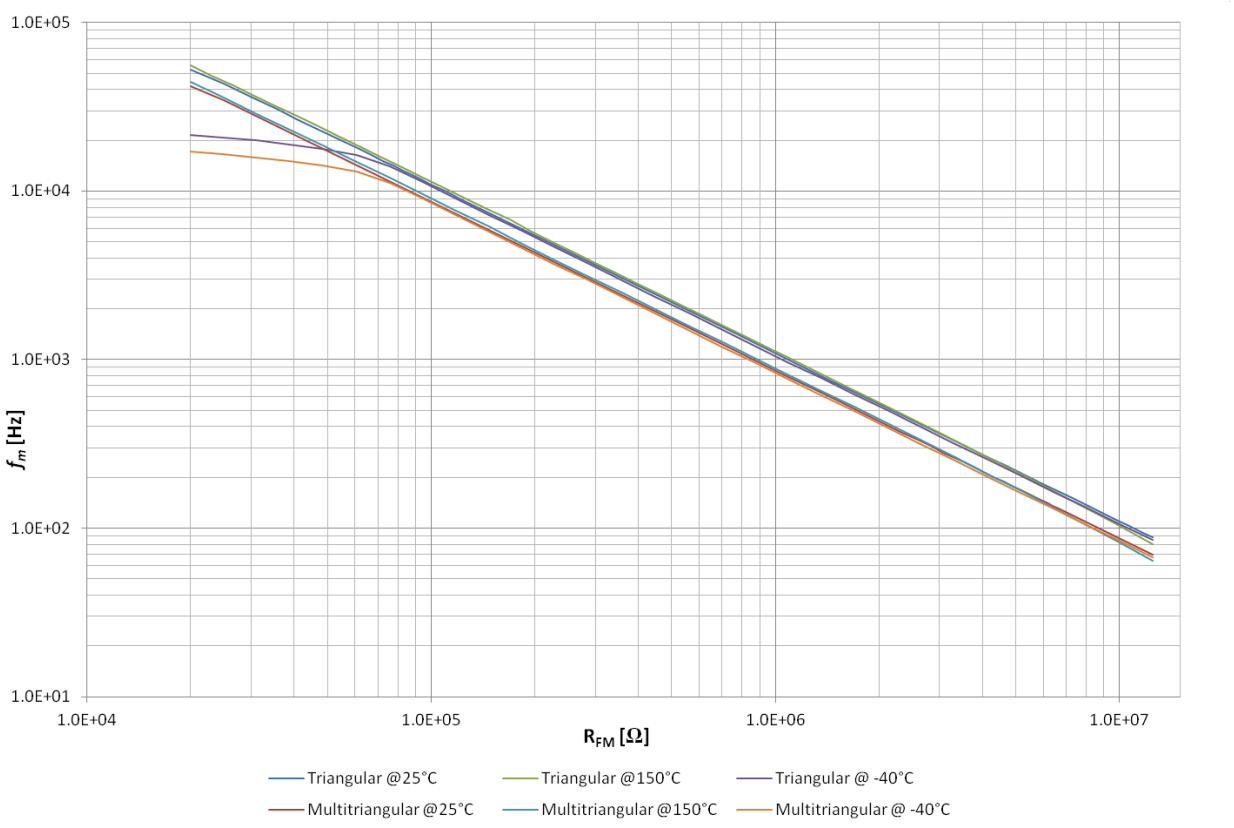


Figure 6.9: Profile Generator output frequency versus external resistor $f_m\,(R_{FM})$ at different operating temperatures ($-40°C$, $25°C$ and $150°C$), in triangular and multi-triangular operation modes.

6.4 Top SSCG concept

6.4.1 Output spectral content at the main sub-harmonic window

Single-cycle single-slope triangular profile

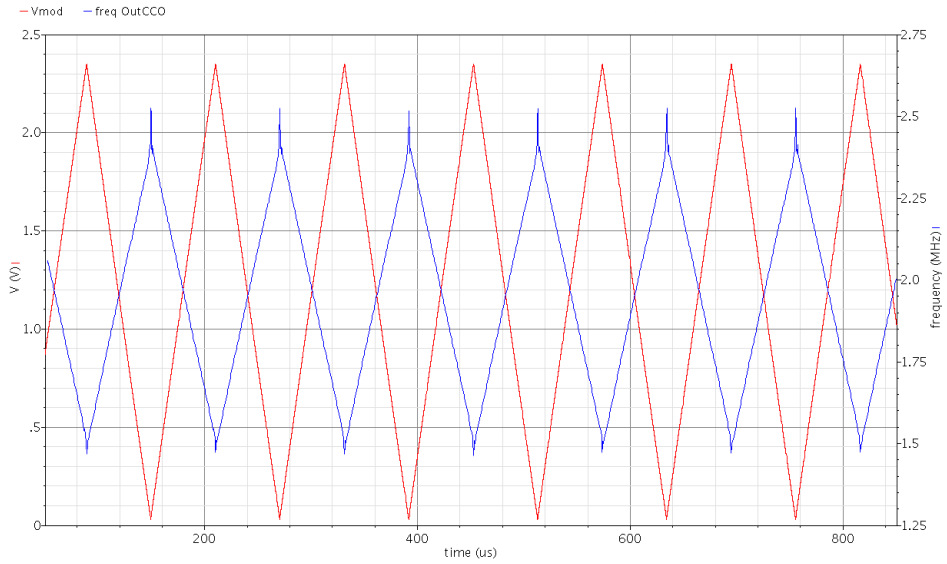


Figure 6.10: Waveform of a triangular profile and the output frequency of CCO with $f_m = 9kHz$

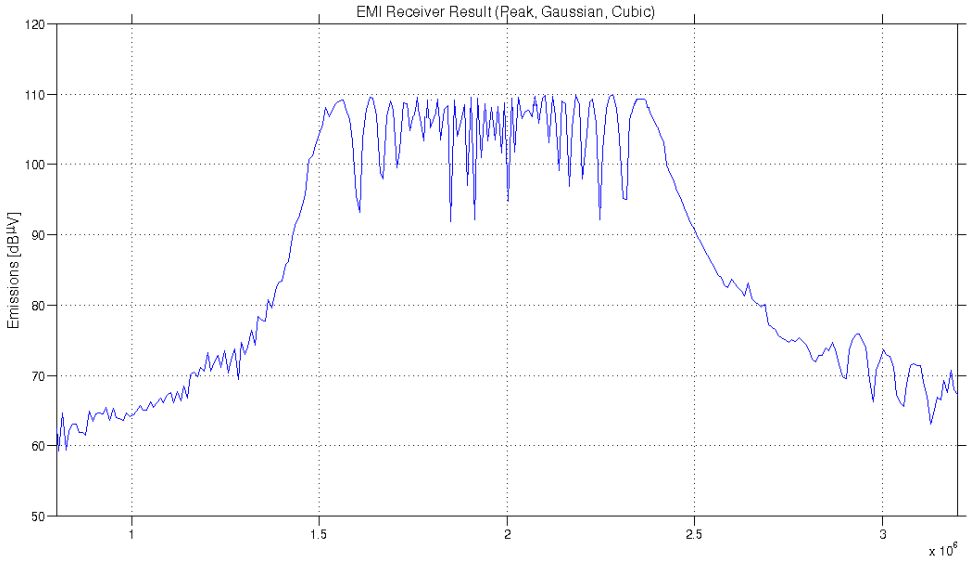


Figure 6.11: Spectral content of a triangular modulation with $f_m = 9kHz$

Multi-cycle single-slope triangular profile

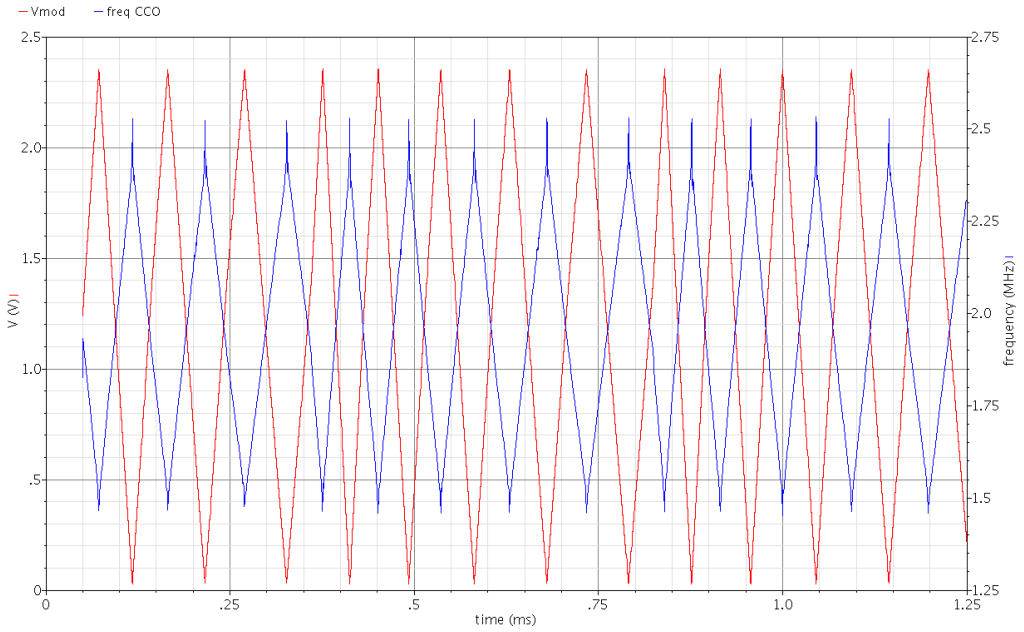


Figure 6.12: Waveform of a multi-cycle triangular profile and the output frequency of CCO with $f_{m_{min}} = 9kHz$

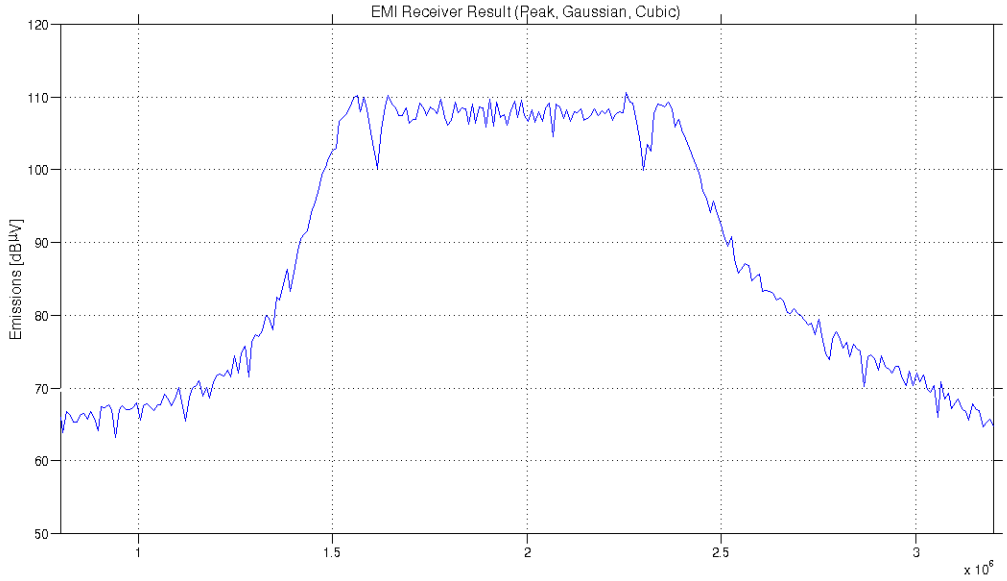


Figure 6.13: Spectral content of a multi-cycle triangular modulation with $f_{m_{min}} = 9kHz$

Single-cycle multi-slope triangular profile

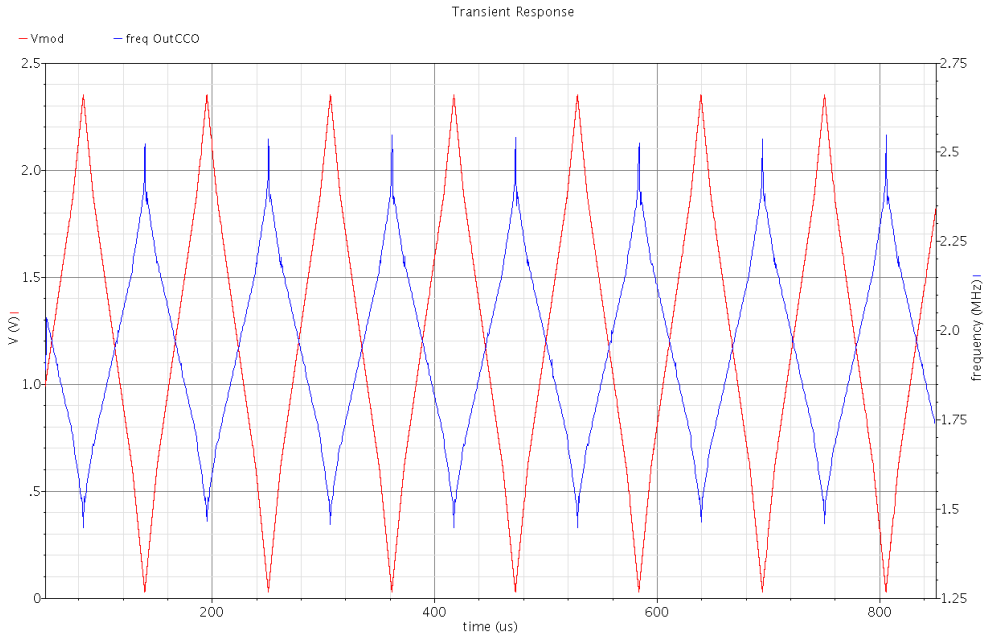


Figure 6.14: Waveform of a multi-triangular profile and the output frequency of CCO with $f_{m_{min}} = 9kHz$

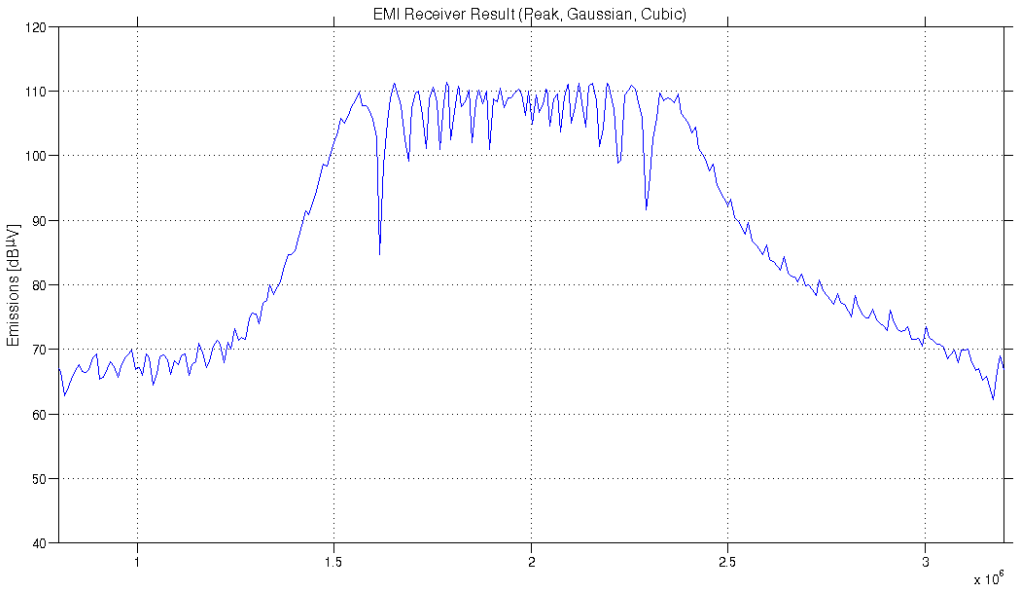


Figure 6.15: Spectral content of a multi-triangular modulation with $f_{m_{min}} = 9kHz$

Multi-cycle multi-slope triangular profile

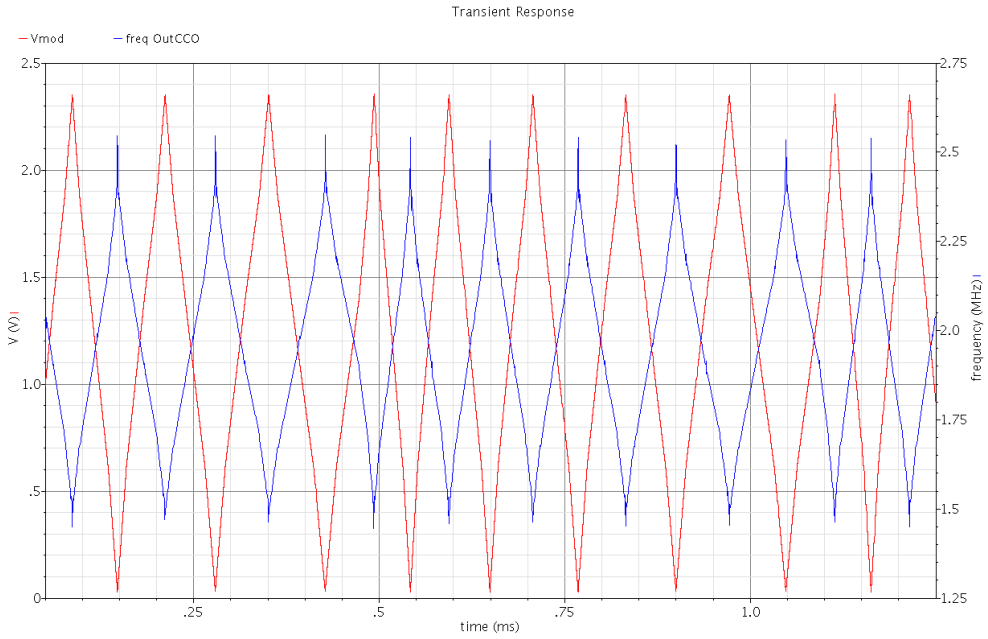


Figure 6.16: Waveform of a multi-cycle multi-triangular profile and the output frequency of CCO with $f_{m_{min}} = 9kHz$

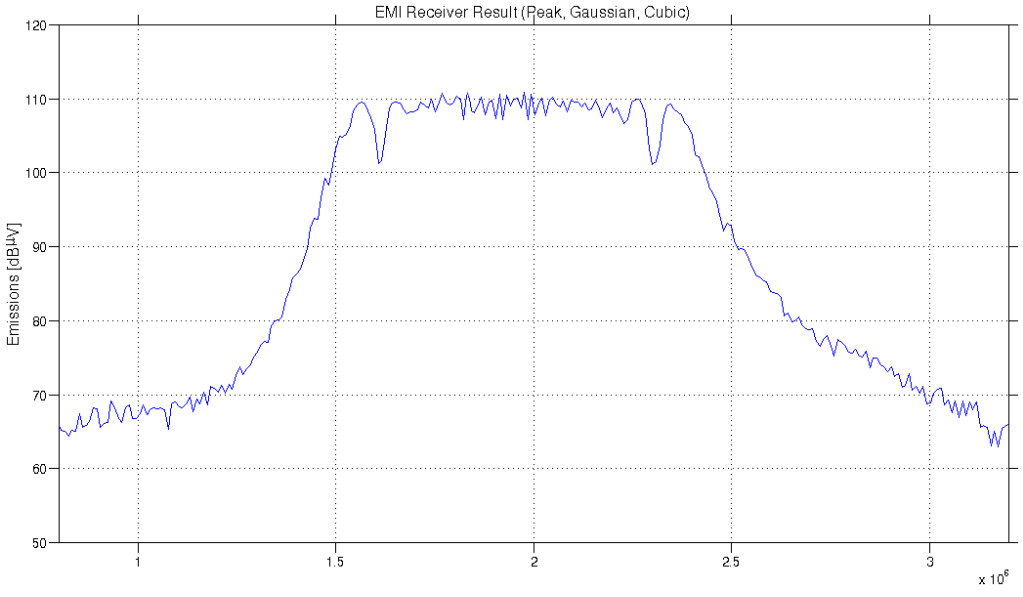


Figure 6.17: Spectral content of a multi-cycle multi-triangular modulation with $f_{m_{min}} = 9kHz$

Results considerations

Above some simulation results are shown, for each modulation profile that the SSCG chip solution can generate, that are single-cycle single-slope, multi-cycle single-slope, single-cycle multi-slope and multi-cycle multi-slope triangular profiles. For each of these profiles are given a time domain diagram showing the voltage profile waveforms and the output frequency of CCO that sweep according to the modilation profile, and finally a frequency domain diagram showing the final spectral content zoomed to the first sub-harmonics window. The sub-harmonics window after modulation shows a different shape according to the choosen modulation profile.

6.4.2 Overall output spectral content

Figure 6.18 shows the conducted EME spectral content in CISPR normative frequency range, from 150 kHz to 108 MHz. As modulation profile a multi-slope triangular with $f_m = 9kHz$ was used. The carrier frequency was set to $f_c = 2.36MHz$ and the spreading percentage to 40%.

The measured reduction of the fundamental in Figure 6.18 was 15 dB, with greater attenuation on subsequent harmonics, up to 20-22 dB.

Spread Spectrum Frequency Modulation techniques help to weak the maximum peak level of conducted emissions from a generic Switched Mode Power Converter and achieve a good attenuation. We benchmarked by simulation the reduction that the SSCG chip solution implemented could give with CISPR 25 standard, being about in the $4 \div 18\,dB$ range, according to the profile selected, the spreading percentuage, the carrier frequency f_c and the modulating frequency f_m.

6.4.3 Power Dissipation

Power Dissipation arises from the following sources:

- Dynamic power dissipation due to switching current from charging and discharging parasitic capacitance.
- Dynamic power dissipation due to short-circuit current when both n-channel and p-channel transistors are momentarily on at the same time.
- Static power dissipation due to leakage current and subthreshold current.

The implemented chip solution never exceed $550\mu A$.

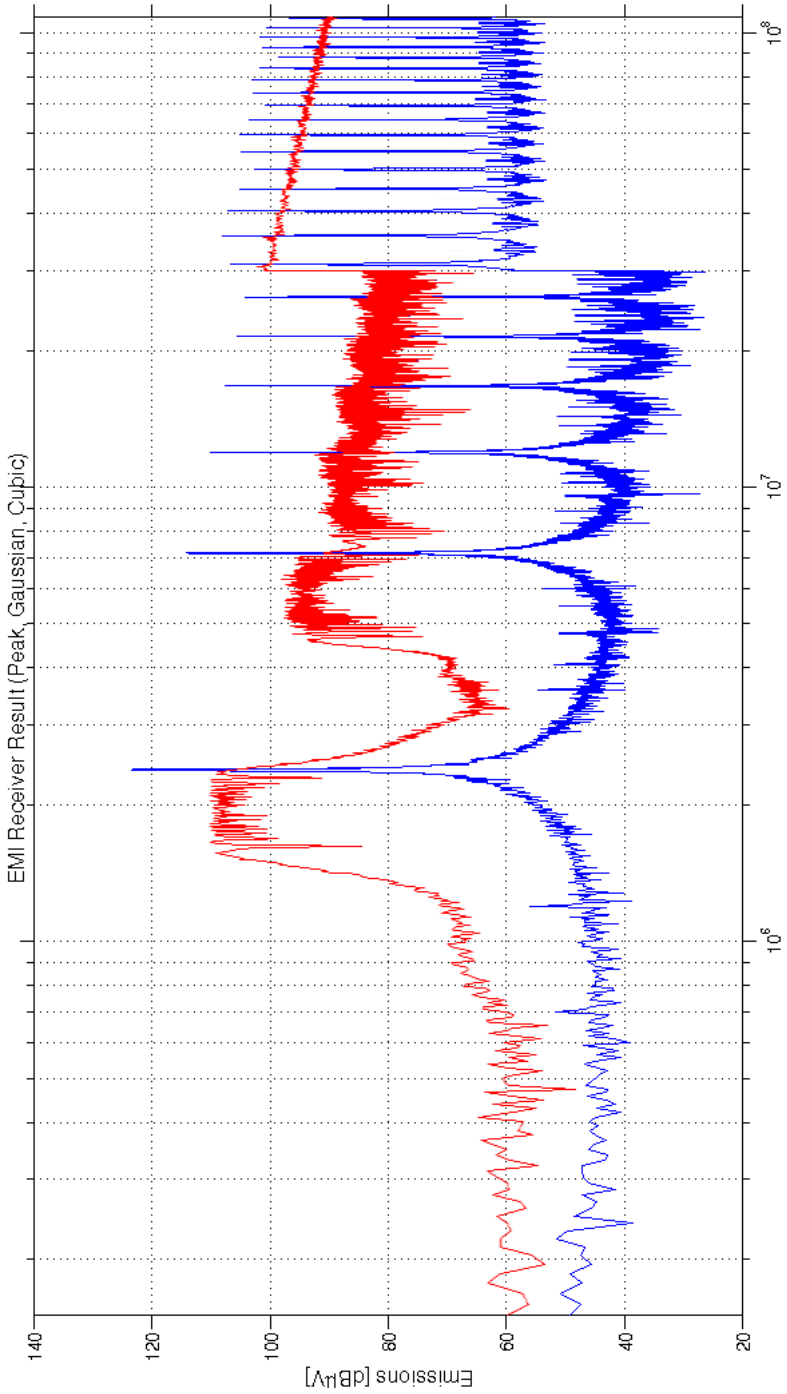


Figure 6.18: Spectral content of a multi-triangular modulation with $f_m = 9\,kHz$ over the entire conducted EMI frequency range against a non-modulated rectangular signal

Chapter 7

Conclusions

Presence of SSCG-techniques in digital systems is not strange in some commercial applications (mainly, in personal computers and microcontrollers) but it is nearly unknown in the world of switching power converters, characterised by lower frequency signals. A first question was related to the worthy possibility of implementing such techniques in switching power converters in order to reduce EMI emissions to battery. This is the main objective of the thesis.

Potential problems related to Electromagnetic Interference (EMI) is a growing concern as more and more systems in our environment are being electrified. The problems related to EMI have of course been present for as long as the presence of electrical equipment, but nowadays electrical equipment is squeezed into smaller volumes. Thus, potential problems are imminent if the design of each equipment or component is not properly considered. However if the interference was related to the airbag deployment of a car, life threatening situations can arise which of course is not acceptable.

The aim of the thesis was to investigate the conducted electromagnetic emission properties, of switching systems like DC-DC converters by simulations, and to develope a solution which can help to mitigate these emissions, in order to accomplish normative standards.

A switch-mode power supply (SMPS) offers many advantages over its linear counterpart, including higher efficiency, smaller size and weight, and the ability to boost output voltage above input voltage. With these benefits comes a major drawback-noise. Since switchers generate high dv/dt and di/dt by their very nature, interference with nearby circuits, devices, or systems is possible. Many techniques may be employed to mitigate noise, either at the source or beyond. Of course, it's best to address noise at the source wherever possible. Common techniques to do so include slowing switching transitions, choosing switching frequency to least disturb the system, snubbing high dv/dt nodes, minimizing high di/dt current loop areas, etc.

When common techniques to mitigate noise fail to provide the necessary margin against required limits for a given application, or when the efficiency of the power converter is an important concern, a technique called spread spectrum frequency modulation (SSFM) may be implemented, whereby the switching frequency is swept within a limited range about a nominal set point. While not suitable for all applications, SSFM is a handy technique for power designers to include in their tool kit.

After modulation, a single harmonic changes into an amount of side-band harmonics with amplitudes smaller than the non-modulated harmonic and separated by a frequency f_m (modulating frequency). Amplitudes of side-band harmonics resulting from modulation show a different aspect or outline depending on the modulation profile. In implementing a frequency modulation technique, it must be ensured that the resulting side bands do not fall into the audible range. Also, overlapping of the side bands of different switching harmonics should be avoided to achieve appreciable spread in spectrum. Such variable switching-frequency techniques are attractive, since they can be realized easily without changes in the topology or power components and with little additional cost, particularly when digital control is used. Many PWM control ICs now have frequency-modulation options.

Even if there is a reduction in the conducted EMI emissions, by applying Spread Spectrum Modulation, these enhancement can be faded by normative and by the standardized test measurement setups. Moreover the final reduction on the conductive EME are very dependent by the modulation parameters and by the normative parameters of the measurement instrument, like the resolution bandwith and detector's type in a scanning receiver. In order to investigate the influence of so many parameters and factors a software tool was developed.

The tool applies frequency modulation theory and Simulink/Matlab co-simulations to clarify and quantify the effect of SSFM. The software suite is standalone and is not bound to any transistor-level simulation softwares like SPICE or Cadence Framework. With the help of the tool we have examined conducted emissions from a DC-DC converter by simulations with automotive standard EMI test setups.

We build a user friendly tool that lets the user "to play" with all the Spread Spectrum Modulation techniques in different test measurements setup. With the help of this tool can be achieved a better understanding of theoretical and real benefits of Spread Spectrum Modulation

techniques. We have verify the techniques available in literature and matched their results. In addition we have benchmarked the reduction of conducted EMI emissions from a generic Switched Mode Power Supply that these techniques can provide, that would be in the $2 \div 20\,dB$ range.

This thesis demonstrated through simulation and analysis that when understood and carefully applied, spread spectrum frequency modulation (SSFM) can be an effective tool for reducing the spectral peak energy that is intrinsic with the operation of a switch-mode power supply. In addition, it has been shown that the modulation waveform (triangular, hershey-kiss, pseudorandom, or otherwise), modulation frequency, and depth of modulation can uniquely impact spectral harmonic spreading and must be carefully selected in accordance with the application and well understood principles of FM modulation.

The first observation is the confirmation that spectral spreading increases as both the modulation frequency and the harmonic order increase. There is greater spreading of the higher harmonics. A triangular modulation produces a flat side-band harmonics spectrum. Considering a triangular profile as the reference base, profiles plotted outside the triangular profile limits seems to concentrate harmonics around the two peaks defining the bandwidth; in the same way, profiles plotted inside the reference triangular profile concentrate harmonics around the carrier frequency. When compared to random or chaotic modulations, such periodic modulation techniques are also said to provide better control over how the EMI energy is spread within the overall EMI spectrum bandwidth. Targeting selected bands within the overall EMI spectrum and even selective elimination of EMI at certain frequencies are also possible. SSCG-techniques offer the capability of moving the modulation spectrum as desired (of course, with certain limitations); this fact can be profitable in order to avoid undesired interferences with other systems.

Potential drawbacks of implementing SSFM include: impact on output voltage ripple, tendency to raise the noise floor, and potential for audible noise. While the long-standing design techniques for reducing interference in switch-mode applications remain unchanged, it was shown that spread spectrum technology, when carefully applied to a switching regulator, has the effect of spreading harmonic energy and changing it from narrowband to broadband emissions. In so doing, measured conducted emissions are reduced, however, the total noise energy is unchanged and other bands can be adversely affected depending on the application.

In order to assolve the main purpose of the thesis, a standalone and configurable clock gener-

ator chip solution that apply a Spread Spectrum Modulation to a DC-DC converter was developed. The solution was specifically designed for automotive target.

The target application of the circuit is an unfair ambient for a chip because when placed inside vehicles, chips must be able to work correctly even with a widely variable supply voltage range and temperature range; they also must be provided of several protection subsystems that will avoid any failure in all the possible working conditions could happen: ESD and short circuits at the output are just some of the issues that must be kept in mind developing a circuit made specifically for this target application.

To give an identity card and to conceptualize the internal structure of the chip solution, simulation results by the Matlab tool has been used and a deep research of competitor chip solutions already in the market and of the several CCO architectures has been performed. We see that CCO control characteristic linearity is a must, since it directly influences the amount of distortion of the modulated signal. Jitter and phase noise requirements are not so stringents, in a SMPC application, to force the use of a PLL as clock generator, thus a free running VCO architecture was adopted, but jitter (and phase noise) introduced must be kept under control because it increases the overall level of noise.

Relaxation oscillators would be optimal because of their linear input control/frequency relationship. Control linearity is limited only by the time delay added by the comparator that detects the threshold crossings of the capacitor voltage and reverses the capacitor current. In order to achieve a good control linearity the decision delay must be made small, thus comparators bandwidth must be chosen large, that give less filtering of decision level noise. Therefore there is a larger noise voltage variance at the output and this increases the jitter. There is a design trade-off and a coupling between jitter and control linearity.

A new relaxation oscillator typology called *coupled sawtooth oscillator* has been chosen. In this architecture the crossing of the threshold level by the capacitor voltage detected using a simple differential pair. This allows the achievement of a very high control linearity (limited only by transistor mismatches). And more importantly, allows to reduce the jitter. Therefore the trade-off between jitter and linearity disappear.

In a SSCG application, the principal aim is to apply the spread spectrum modulation that can achieve the best final conducted EME reduction performances. In this regard, we have investigated,

by using the Matlab Tool several modulation profiles. However, if the profile to generate is composed by complex and non-linear curves, it is hard to develop the analogic circuit needed to generate the profile. Thus, there is the need of an analogic circuit if the profile is quite simple to generate (like a triangular waveform), otherwise, if a complex profile are adopted a digital approach is prefered. This would lead to a trade-off between the EME reduction and the circuit complexity, and so, also with the chip area and the final cost of the developed solution. In particular the choice between an analog and a digital approach have a big influence also on the most appropriate technology's choice.

With these considerations in mind, our choice fell on the use of a BCD smart power technology with a limited digital part, so avoid complex profiles and not linear, but rather profiles easily be generated by analog circuitry. The Matlab Tool shows that the the best compromise is the triangular profile to which can be added some techniques easily implemented to further improve the final result (*multi-slope* and *multi-cycle*). *Multi-slope triangular* or *multi-triangular* profile claims to be the junction point and the best trade-off between circuit complexity and performances.

A standalone SSCG chip was developed with a transistor-level design and simulation environment (Cadence Framework). Its operation was tested and verified through simulations that take into account all the technological parasites.

The standalone chip lets the user to select properly the spreading percentuage, the carrier frequency f_c and the modulating frequency f_m, by some external resistors. In order to be successful in the selection of these values, some considerations must be taken into account. For every modulation profile, amplitude reduction of the side-band harmonics resulting from the modulation process depends on the spreding percentuage. Carrier (or switching) frequency f_c, and modulating frequency f_m (defines the distance in frequency between two consecutive side-band harmonics) are of interest when measuring with spectrum analyzers: their RBW (Resolution Bandwidth) and measure mode (peak, quasy-peak and average) are responsible for giving different measured values of the same physical fact of modulation; as a general asseveration, the larger the selected RBW, the higher the obtained measure because more side-bad harmonics can fall inside this RBW, adding their amplitudes. Switching (carrier) frequency in power converters is not usually too large because the electronics components (diodes and power transistors mainly) are not able to manage larger power with shorter switching times. Anyway, use of higher switching frequencies is advisable in order to reduce the size and power capability of the passive components (filters, inductances, diodes, tran-

sistors and so on) and increase the power efficiency of the converter. As the attenuation increases with larger modulation indexes, higher switching frequencies f_c are preferred. It was found that with the lower switching frequency, a large frequency deviation is required to achieve appreciable spread of EMI spectrum.

As explained along the thesis, real EMI attenuation benefits are always obtained. This true reduction capability can be faded by normative considerations, mainly related to the regulatory RBW to be set on the compliant Spectrum Analyzer. Only when normative measurements are of interest, a special care must be taken to select a proper modulation frequency in order to maintain these EMI attenuation benefits when measuring. Simulation results show that the best conducted EME reduction is achieved for a modulation frequency equal to the RBW of the measurement instrument, that is generally $f_m = RBW = 9\,kHz$. The modulation frequency must be close to or greater than the measurement resolution bandwidth (RBW) set by the standards. This would ensure that besides spreading the spectrum, the achieved spreading will be clearly reflected by the measurement process.

Spread Spectrum Frequency Modulation techniques help to weak the maximum peak level of conducted emissions from a generic Switched Mode Power Converter and achieve a good attenuation. We benchmarked by simulation the reduction that the SSCG chip solution implemented could give with CISPR 25 standard, being about in the $4 \div 18\,dB$ range, according to the profile selected, the spreading percentuage, the carrier frequency f_c and the modulating frequency f_m.

7.1 Further investigations and improvements

Investigation tasks keep a strong similarity with the pioneer who opens the way to a new world but who is neither able to realise the importance of his discovers nor finish the mission. These are the tasks for people coming behind, who take the actual status as a starting point and give their own contribution. Following points are open themes to be dealt with:

The Spread Spectrum Matlab Tool realized during this thesis work, seems to have great possibilities and capabilities, moreover, it can be still improved and above all many new features can be added. In order to make more real the final result, add several non idealities to the simulation, like modulation profile distortions, amplitude noise, jitter and phase noise, limited bandwith of the SSCG system, non-linear voltage-frequency characteristic of the internal VCO; add other modulation

profiles and the multy-cycle modulation; add other tipologies of switching circuit (SMPCs like Boost, Buck-Boost, etc... , Switched Capacitor Circuits and Charge Pumps.

The next step will be the development of a layout and the production of a test chip for a subsequent verification of the results obtained by simulations during this thesis work, with the measurement results from the laboratory.

Appendix A

The buck converter

In this appendix a buck converter is used as an example of DC-DC converter because of its wide use and ease of understanding. The basic operation of a buck converter is overviewed in this appendix addressing the most common modes of operation. Power losses in the converter are addressed as well, in order to motivate, later on, the choice of the operating mode accordingly to the load condition of the converter [1].

A.1 Buck converter operation

A buck converter, also called a step-down converter, produces a lower average output voltage V_{out} than the DC input voltage V_{in}. Figure A.1 shows a buck converter system. The converter consists of a switch network (transistors M_1 and M_2) and a second order LC low pass filter.

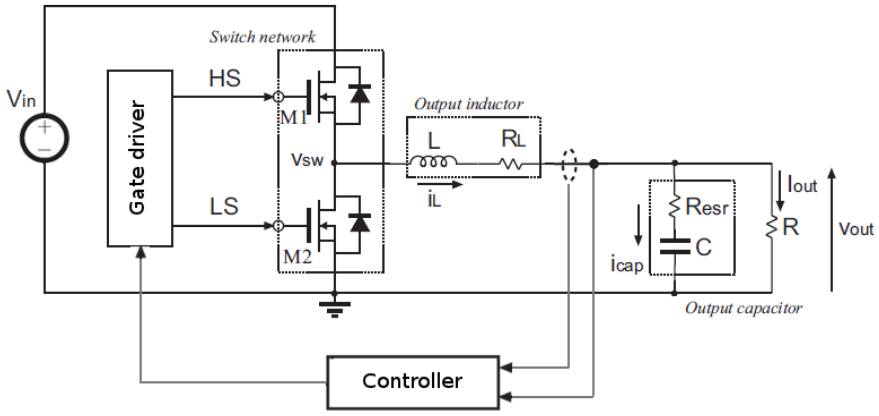


Figure A.1: Buck converter schematic. The two power transistor M_1 and M_2 are driven by the signals HS and LS. The inductor series resistance R_L and the output capacitor ESR R_{esr} are also represented in the schematic.

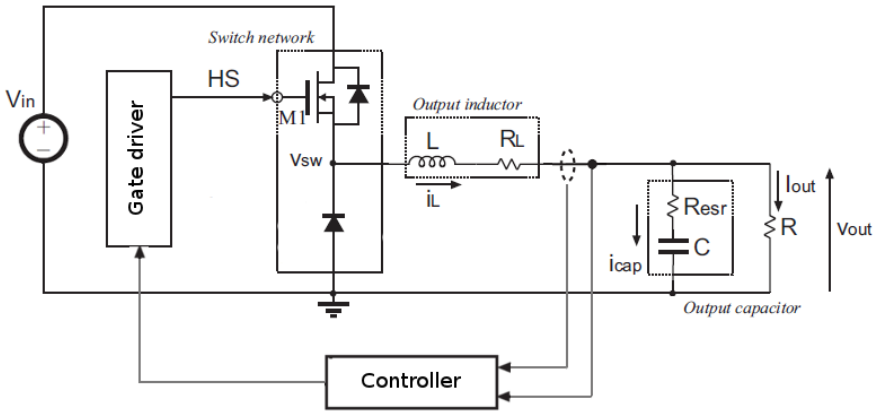


Figure A.2: Asynchronous buck converter. The low side power transistor M_2 is either replaced by a power diode or kept off during the whole length of the switching period allowing its body diode to conduct when M_1 is off.

The input voltage from the battery gets chopped by the power switches and the average input voltage is thus reduced. Assuming ideal switches, the chopped voltage $v_s w$ at the switching node is a square wave with duty ratio $D = t_{on}/T_s$, where $t_o n$ is the on time of the transistor M_1 and T_s the switching period as shown in Figure A.3(a). The low pass filter, instead, is used to pass the DC component of $v_s w$ while attenuating the AC component to an acceptable ripple voltage. Neglecting the loss in the converter, the DC output voltage V_{out} is given by:

$$V_{out} = V_{in} D \tag{A.1}$$

The converter is said to be synchronous or asynchronous whether the low side power switch M_2 is used or is kept off during the whole length of the switching period. Converter state variables are the current flowing through the inductor L (i_L) and the voltage across the capacitor C (v_C) that coincides with the output voltage V_{out} except for the voltage drop across the *Equivalent Series Resistance* (ESR) of the output capacitor C. The controller, therefore, computes the control law based on one or both of the state variables. According to the output current I_{out} the converter can enter two different modes of operation, the *Continuous Conduction Mode* (CCM) and the *Discontinuous Conduction Mode* (DCM). From this point forward we will use the notation PWM-CCM and PWM-DCM to refer to the continuous conduction mode and discontinuous conduction mode of the converter respectively, where PWM indicates that the switching frequency of the converter is kept constant.

A.2 The Continuous Conduction Mode (PWM-CCM)

The waveforms characterizing a buck converter in this CCM operating mode are shown in Figure A.3(a). Moreover, in Figure A.3(a) the waveforms of the output voltage and inductor current are approximated to be piecewise linear functions, approximation that will be adopted from here on. In steady state the output voltage is given by (A.1) while the output current I_{out} equals the average value of the inductor current. The inductor current is always positive for the whole length of the switching period T_s as long as $I_{out} > \Delta i_L/2$, while when $I_{out} < \Delta i_L/2$ the inductor current becomes negative momentarily in the switching cycle and this corresponds to the converter discharging the output capacitor C through the inductor L. As long as i_L flows continuously, the converter is considered to be in continuous conduction mode.

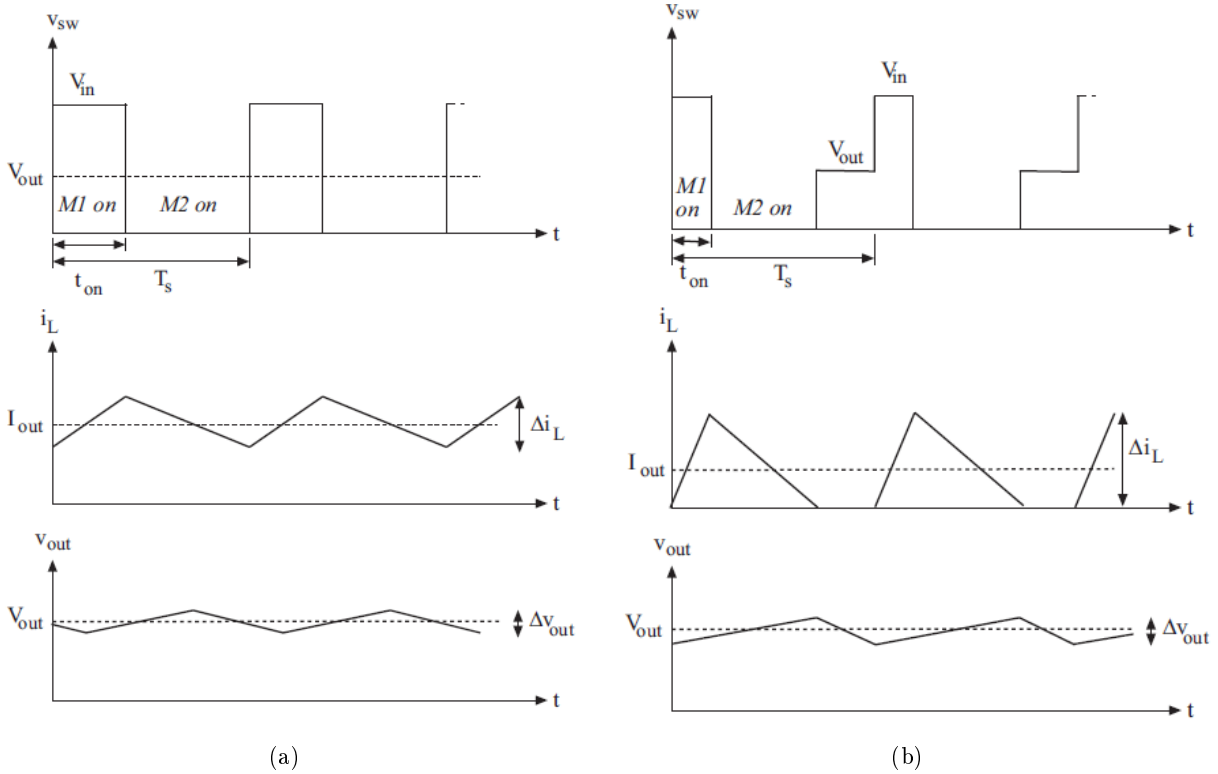


Figure A.3: (a) Converter waveforms in PWM-CCM mode. t_{on} is the on time of the power transistor M_1 while Δi_L and Δv_{out} are the inductor current ripple and the output voltage current ripple respectively. (b) Converter waveforms in PWM-DCM mode of operation. t_{on} is the on time of the power transistor M_1 while Δi_L and Δv_{out} are the inductor current ripple and the output voltage current ripple respectively.

A.3 The Discontinuous Conduction Mode (PWM-CCM)

Replacing the low side switch M_2 in the synchronous converter with a power diode D results in a conventional (or asynchronous) buck converter, as shown in Figure A.2. When output current I_{out} is higher than $i_L/2$, the inductor current flows continuously and the converter still works in continuous conduction mode, with V_{out} satisfying (A.1). When i_{out} is lower than $\Delta i_L/2$, the diode conducts while the inductor current decreases. The inductor discharges stored energy to the output capacitor until the current drops to zero. The diode then blocks the reverse current and the inductor current remains zero until the next switching cycle. This operation mode is called discontinuous conduction mode because the inductor current is zero for finite intervals. Figure A.3(b) shows converter waveforms in this mode of operation. In a synchronous buck converter the body diode of the transistor M_2 is usually used to allow the converter to work in discontinuous conduction mode (M_2 is kept off for the whole length of the switching cycle).

In discontinuous conduction mode, the DC value of the output voltage of the converter Vout does not satisfies (A.1). Instead, the new expression of D is given by:

$$D = \frac{V_{out}}{V_{in}} \sqrt{\frac{I_{out}/I_{out_{cr}}}{1 - V_{out}/V_{in}}} \tag{A.2}$$

where $I_{out_{cr}}$is the maximum value of average inductor current at the edge of continuous conduction mode if V_{out} is constant:

$$I_{out_{cr}} = \frac{T_s \cdot V_{out}}{2L} \tag{A.3}$$

In general, as the average duty cycle value D in (A.2) is lower than the value in (A.1) when the converter is in continuous conduction mode, the output voltage ripple in PWM-DCM is not usually considered as a design variable.

Appendix B

EMC problematics: Conducted Electromagnetic Interference Emissions

The necessity for different circuits to be able to operate in close proximity, implies that electromagnetic interference (EMI) may become a major problem in circuit design. The problem with EMI gets worse as the circuitry becomes smaller, meaning that more circuits are being crowded into less space, which increases the probability of interference. An electronic equipment designer must assure that a system functions correctly when it has other electronic equipment nearby and not only under the ideal conditions in the laboratory. It is important that external noise sources do not affect the system and that it not itself is a source of noise to the environment. This is called electromagnetic compatibility (EMC) and is becoming a very important aspect to be considered in the early part of the product development.

B.1 Definition of EMC, EMI, EMS and EME

Many definitions are applicable in order to describe the principle of electromagnetic compatibility (EMC): *Electrical and electronic devices are said to be electromagnetically compatible when the electrical noise generated by each does not interfere with the normal performance of any of the others. Electromagnetic compatibility is that happy situation in which systems work as intended, both within themselves and within their environment.*

When there is no EMC, this is due to electromagnetic interference (EMI): *EMI is said to exist when undesirable voltages or currents are present to influence adversely the performance of a device. These voltages or currents may reach the victim device by conduction or by electromagnetic field radiation.*

This last precision is not superfluous, and a clear distinction between these two interference types must be made. To be precise, the term *radiated interference* in the above definition comprises

two phenomena, namely *near field coupling* and *far field radiation*. This distinction is important and not a purely academic categorization.

When there is EMI, there is at least one EMI source causing an intolerable emission (be it conducted, near field coupled or far field radiated), and possibly one or more EMI victim(s) which for one or more reasons is (are) susceptible to the emanated disturbance.

IEEE has defined the concept EMC in the following way: *Electromagnetic Compatibility, EMC, is the ability of a device, equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment.*

ElectroMagnetic Compatibility (EMC) is the ability of an electrical installation to work properly in an electromagnetically polluted environment as well as not to disturb other electrical devices due to the emission of electromagnetic interferences. It means that the electrical devices don't influence themselves and one another, e.g. via the common ground of control and power circuits.

A system is electromagnetically compatible if it satisfies three criteria:

- It does not cause interference with other systems.
- It is not susceptible to emissions from other systems.
- It does not cause interference with itself.

Electromagnetic emission (EME) is described by the International Electrotechnical Commission (IEC) as: *The phenomenon by which electromagnetic energy emanates from a source.*

In the same way, the IEC describes electromagnetic susceptibility (EMS) as: *The inability of a device, circuit or system to perform without degradation in the presence of an electromagnetic disturbance.*

Susceptibility is complementary to immunity, the latter describing to what extent EMI may be injected into a system before failures start to occur. Because the acronym for electromagnetic immunity would conflict with the one used for electromagnetic interference, this term is not abbreviated in this work: when used in the text, immunity always signifies the opposite of susceptibility. Care must be taken when using the concepts of immunity and susceptibility without distinction, since this easily leads to confusion. One may break the transfer of electromagnetic energy (with regard to the prevention of interference) into four subgroups: radiated emissions, radiated suscepti-

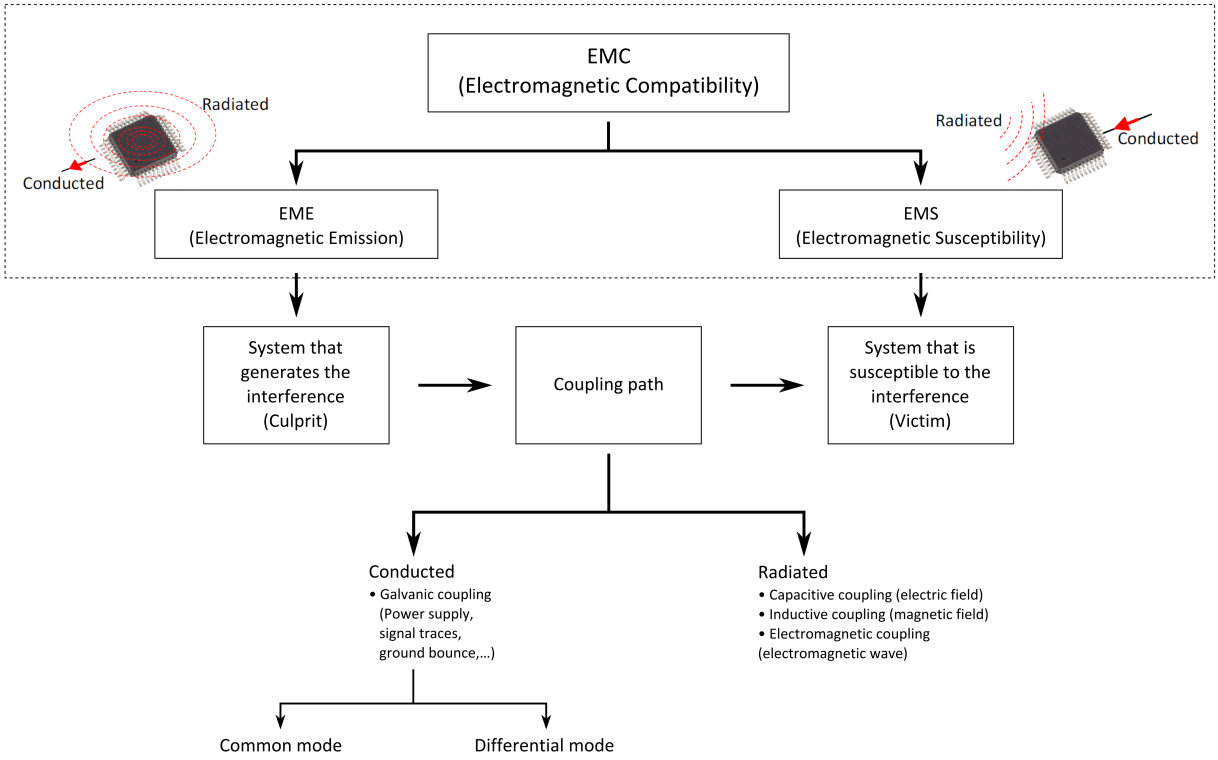


Figure B.1: Electromagnetic Compatibility

bility, conducted emissions, and conducted susceptibility. These four different phenomena and the way they are related to each other are represented schematically in Figure B.1.

EMC is concerned with the generation, transmission, and reception of electromagnetic energy. These three aspects of the EMC problem form the basic framework of any EMC design. In order to define an electromagnetic compatibility problem, three items are necessary:

- a source (also referred to as an emitter, or culprit)
- a coupling channel,
- a susceptible receptor (victim).

A component acting as a noise source at one time could very well be a receptor the next time. This implies that electromagnetic compatibility has two aspects: *emission* and *susceptibility*. Most electronic hardware contains elements which are capable of antenna-like behaviour, such as cables, pcb tracks and internal wiring. These elements can unintentionally transfer energy via coupling

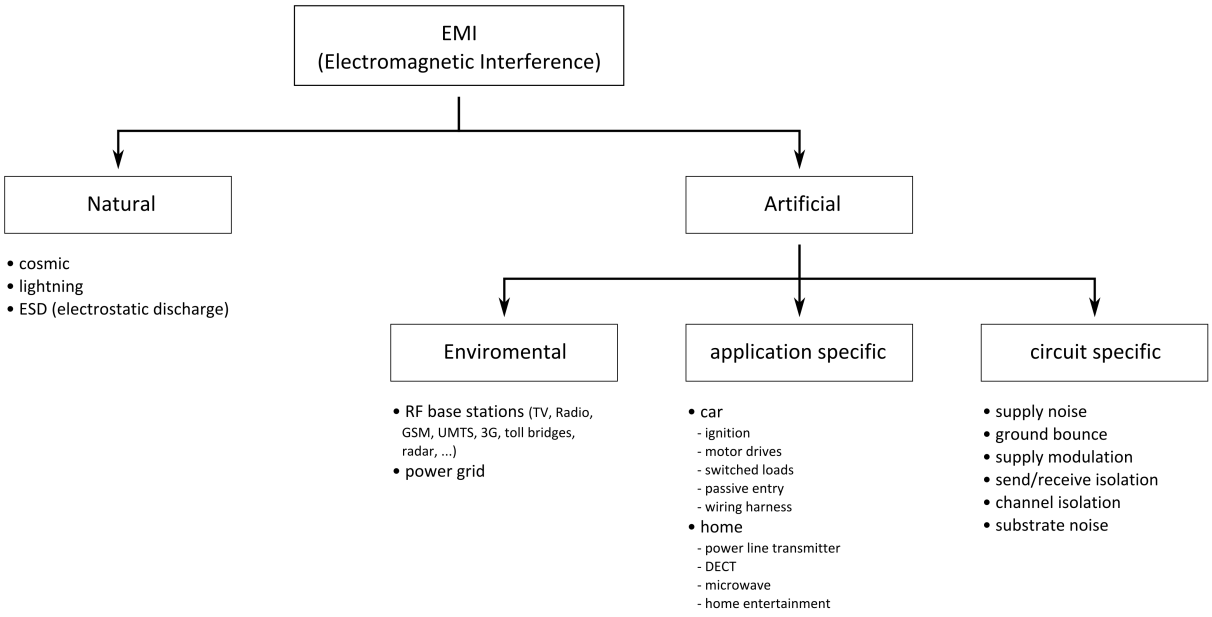


Figure B.2: Typical causes of Electromagnetic Interferences

with the circuits. In practical situations, intra-system and external coupling between equipment is attenuated by the presence of screening and dielectric materials, and by the layout and proximity of interfering and victim equipment and especially their respective cables. Ground or screening planes will enhance an interfering signal by reflection or attenuate it by absorption. There are a number of different ways for the emissions to be coupled into other systems and there are many techniques by which noise can be reduced in an electronic/electromagnetic system. This implies that there does not exist a unique solution to most noise reduction problems.

B.2 Coupling channels for the disturbances

Electromagnetic interference is generated by a varying electric or magnetic field. It is transmitted by means of conductive, inductive or capacitive coupling, through free space or a combination of these means.

In EMC literature and EMC regulations the mechanisms of electromagnetic interference are divided into two categories, *conducted* and *radiated*. Historically, this categorization has been used in the regulations and, unfortunately, it continues today. The word "unfortunately" was used because both *near-field coupling* and *far-field radiation* are lumped under the term *radiated emissions*. While

experts in electromagnetics are quite familiar with the difference between near-field coupling and far-field radiation, the vague terminology in EMC regulations tends to confuse those who are trying to learn the basic concepts. In fact, near-field energy is stored, not radiated. Furthermore, when you couple to the near-field of a circuit, you not only pick up unwanted electromagnetic energy, you also alter the operation of that circuit by extracting and/or redirecting energy that was otherwise being stored in the neighboring space. The terms induced interference is used for near-field coupling and radiated interference for far-field radiation. This distinction is not purely academic.

There are many practical differences between how induced and radiated interference occurs. In fact, one can consider how electromagnetic shields behave in different types of fields: in the near-field, electric fields are reflected by a thin metallic shield quite well, whereas magnetic fields readily penetrate metallic shields unless the shield is several skin depths thick. The far-field behavior of shields is different from both magnetic and electric near-field behavior.

Similar effects occur in how circuits pick up near-field electromagnetic energy. Whereas radiated waves always maintain the impedance of air and are therefore always electromagnetic, near-field waves are usually dominated by one component, electric or magnetic. Circuits will pick up radiated energy if they contain antenna like elements: loops or dangling monopole or dipole antennas. Induced energy coupling has different characteristics. High impedance circuits (unconnected metal conductors) are very susceptible to interference from electric near-fields, and low impedance circuits (with large loops) are very susceptible to interference from magnetic near fields. Both types of induced interference increase when the two circuits are brought closer together.

B.2.1 Near-field coupling

Capacitive coupling

Capacitive coupling, also known as electric coupling, is a result from the interaction of electric fields between circuits. If two conductors are placed next to each other, there will be a stray capacitance between them. Figure B.4 shows an example of this phenomenon and an equivalent circuit.

Capacitance C_{12} in Figure B.4 is the stray capacitance between the two conductors. Capacitor C_{1G} and C_{2G} are the total capacitance between each conductor and ground. The resistance, R, is the resistance of conductor 2 and ground, and is the result of the circuitry connected to this conductor.

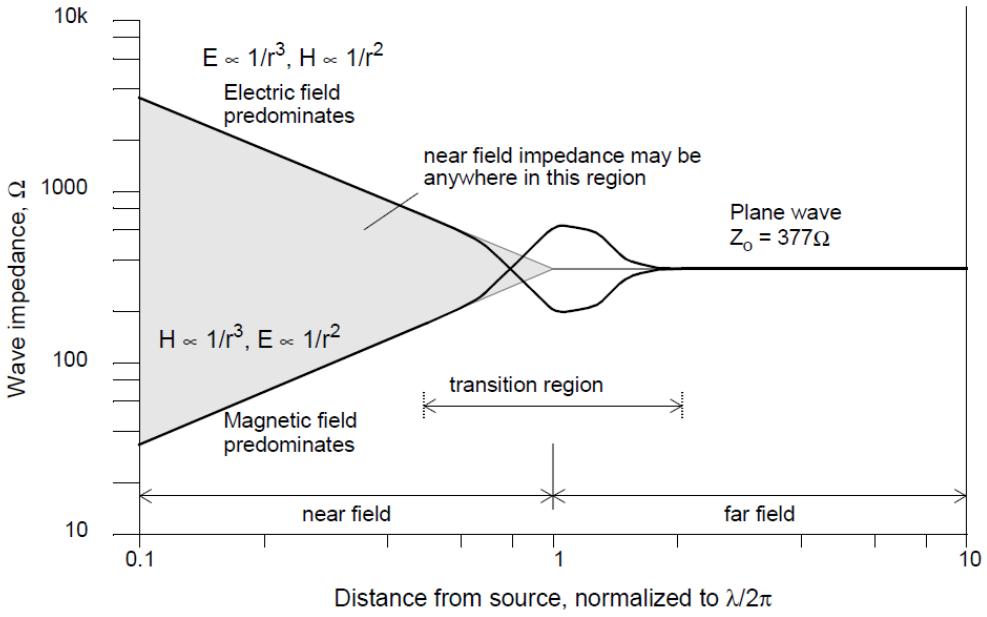


Figure B.3: The wave impedance

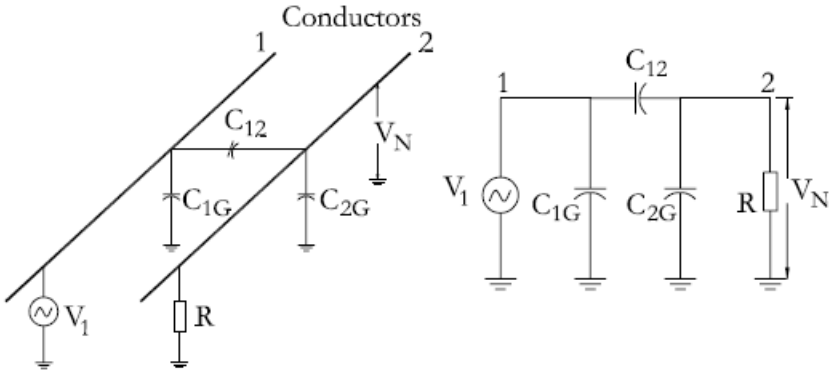


Figure B.4: Capacitive coupling between two conductors

In the figure the voltage V_1 is the source of interference, and circuit 2 the receptor. The noise voltage, V_N, picked up by conductor 2 could be expressed as:

$$V_N = \frac{j\omega \left(\dfrac{C_{12}}{C_{12} + C_{2G}} \right)}{j\omega + \dfrac{1}{R \cdot (C_{12} + C_{2G})}} \cdot V_1 \tag{B.1}$$

In most practical cases the resistance R represents a much lower impedance than the impedance

for the stray capacitance C_{12} plus C_{2G}. Equation (B.1) could therefore be reduced to the following:

$$V_N = j\omega\, RC_{12}V_1 \tag{B.2}$$

If the conductors are moved farther apart, the stray capacitance will decrease. However, only little additional attenuation will be gained by spacing the conductors a distance greater than 40 times their diameter, according to:

$$C_{12} = \frac{\pi\varepsilon}{\cosh^{-1}(\frac{D}{d})} \tag{B.3}$$

where D is the distance between the cables and d the diameter of the cable. The other way to affect the stray capacitance is with electric field shielding of the conductor. When the conductor is shielded, the length of the conductor that extends beyond the shield determines the stray capacitance, and it is therefore important to keep this length short. Also a good ground connection of the shield is necessary in order to provide a good electric field shield.

Inductive coupling

Inductive coupling, also known as magnetic coupling, is a result from the interaction between the magnetic fields of two circuits. A magnetic flux is created as a current flows in a closed circuit. The flux is given by the multiplication of the current in the circuit times the inductance of the circuit. The value of the inductance is depending on the geometry of the circuit and the magnetic properties of the medium that contains the field. A current flow in one circuit may produce a magnetic field in another circuit, and the connection between these two circuits is called the *mutual inductance*, M. M depends on the areas of the source and victim current loops, their orientation and separation distance, and the presence of any magnetic screening. Due to a magnetic field with the flux density $\overline{B}$, the noise voltage, V_N, induced in a loop of area $\overline{A}$ can be derived from Faraday's law as:

$$V_N = -\frac{d}{dt}\int_A \overline{B}\, d\overline{A} \tag{B.4}$$

where $\overline{B}$ and $\overline{A}$ are vectors. For a stationary closed loop with a sinusoidally varying flux density that is constant over the loop area the expression for the noise voltage reduces to:

$$V_N = j\omega\, BA\, \cos\theta \tag{B.5}$$

where θ is the angle between the area and the magnetic flux density. Since $BA\cos\theta$ represents the total flux coupled to the receptor circuit, which means that (B.5) can be rewritten as:

$$V_N = j\omega M I_1 = M\frac{di_1}{dt} \tag{B.6}$$

where I_1 is the current in the source circuit and M the mutual inductance between the receptor and source circuit. The equivalent circuit for magnetic coupling is a voltage generator in series with the victim circuit. Corresponding physical representation and equivalent circuit for the magnetic coupling between two circuits are shown in Figure B.5.

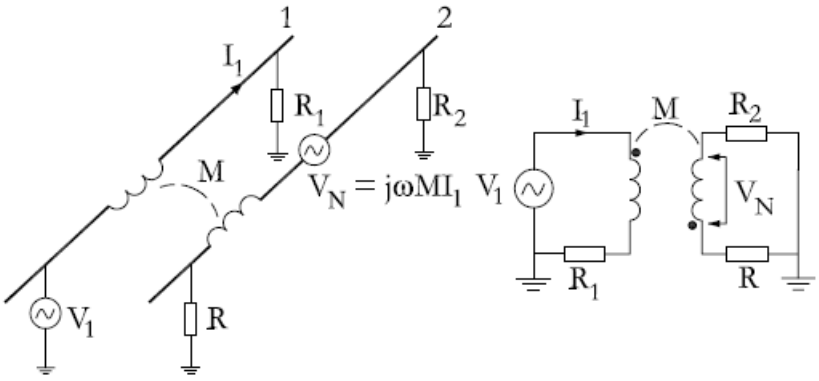


Figure B.5: Inductive coupling between two conductors

The three parameters that are left to modify in order to reduce the noise voltage are then the magnetic flux density, the loop area, and the angle between them. The magnetic flux density can be reduced by physically separating the circuits or by twisting the source wires. Twisting the wires causes a cancellation of the magnetic fields from the wires, but can also be used to decrease the area of the receiver circuit. If the return current of the receiving circuit instead is led through a ground plane, placing the conductor close to the ground plane can decrease the area. A proper orientation of the source and receiver circuits could reduce the $\cos\theta$ term.

B.2.2 Far-field coupling

Electromagnetic coupling or radiation coupling is the transfer of electromagnetic energy over distances generally greater than a few wavelengths (i.e. to the electromagnetic far field). At these distances, fields drop off more slowly with distance than they do very near the source. Both the electric field and the magnetic field are needed to propagate the energy.

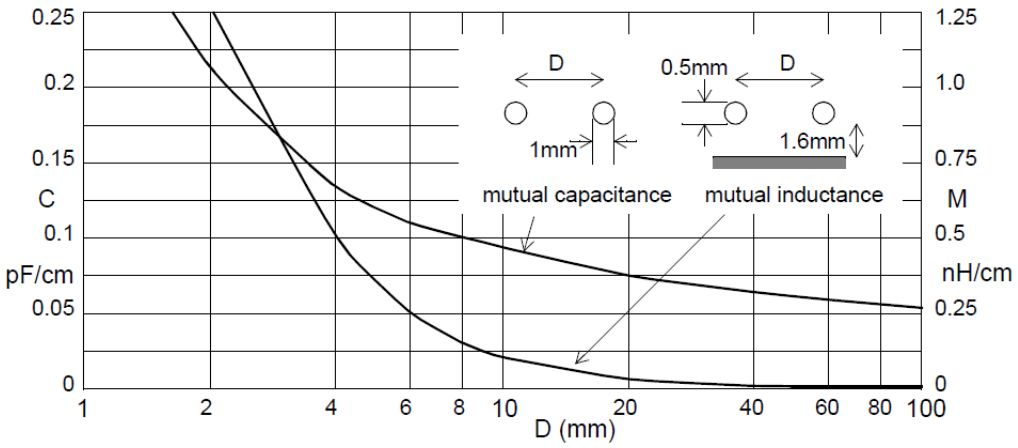


Figure B.6: Mutual capacitance and inductance versus spacing

A conductor carrying a significant di/dt will generate mostly a magnetic field; a circuit node carrying a significant dv/dt will generate mostly an electric field. The structure of these fields will be determined by the physical layout of the source conductors, as well as by other conductors, dielectrics and permeable materials nearby. Further away from the source, the complex three-dimensional field structure decays and only the components which are orthogonal to each other and to the direction of propagation remain.

B.2.3 Conductive coupling

For conducted EMI, noise is coupled via conductors or through parasitic impedances, or power and ground connections. Conducted interference consists of unintended signal energy that leaves a product through its cables. For example, high frequency energy can couple to the power supply and escape the product by traveling out on the power cord. From that point the interference energy can couple to other products directly through the supply lines. The high frequency signals that have escaped a product via cabling may also radiate quite readily from the cable. When an interference source shares a common connection with a victim, then any current due to source's output flowing through the common impedance section develops a voltage in series with victim's input. High frequency or high di/dt components in the output will couple more efficiently because of the inductive nature of the impedance.

Conducted emissions can produces radiated emissions. Consequently, restrictions on the emissions conducted out the product's power lines are intended also to reduce the radiated emissions

from this power distribution system.

B.3 Common mode and differential mode

Conducted interferences can be distinguished into asymmetrical and symmetrical interferences, *common mode* (CM) and *differential mode* (DM) respectively. The differential mode current only flows at the connecting line. The common mode circuit is closed across parasitic capacitors C_p to the earth ground and the connecting lines. The differential mode voltage component of a circuit is a voltage that can be measured between phase conductors and the differential mode current component flows in the supply wires, including the neutral wire. The common mode current component on the other hand flows from the phase and neutral conductor toward earth. The circuit for the common mode current is closed by stray capacitances between the earthed parts and the circuit.

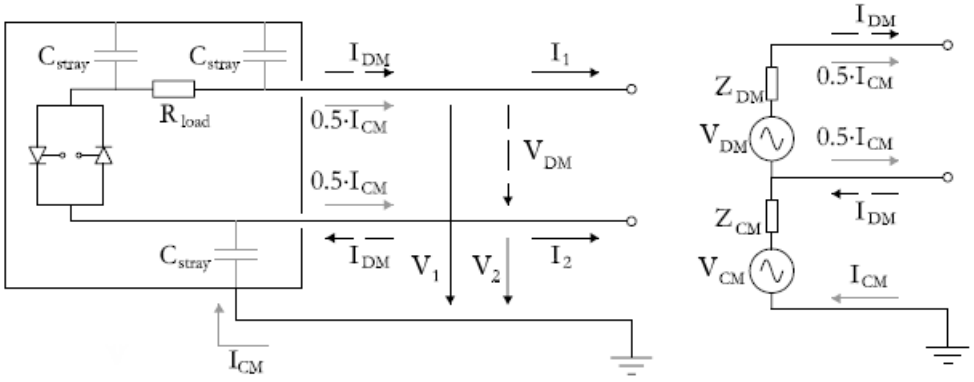


Figure B.7: Common mode and differential mode

$$\begin{cases} V_{DM} = V_1 - V_2 \\ V_{CM} = \dfrac{V_1 + V_2}{2} \end{cases} \qquad \begin{cases} I_{DM} = \dfrac{I_1 - I_2}{2} \\ I_{CM} = I_1 + I_2 \end{cases} \tag{B.7}$$

Appendix C

Measurement instruments

Spectrum Analyzers and Scanning Receivers are often lumped together as the same thing. Although both instruments measure the amplitude of signals in the frequency domain, the units are not the same, and require knowledge to extract correct measurements. Each can be abused, and each can return incorrect measurement results.

The differences between the two can be explored by examining a common test setup (i.e. the parameters necessary to configure each instrument).

Spectrum Analyzer tests set the following parameters:

- Start / Stop Frequency
- Resolution Bandwidth Filter and type (3 or 6 dB)
- Detector(s)
- Sweep Time
- Video Bandwidth

Most spectrum analyzers "couple" or lock the resolution bandwidth, video bandwidth and sweep time together so that critical timing requirements are not violated. These parameters can be manually controlled however, and even forced into modes where incorrect measurements are displayed.

Test Receivers follow a similar setup:

- Start / Stop Frequency
- Resolution Bandwidth Filter and type (3 or 6 dB)

- Detector(s)
- Measurement (dwell) Time
- Step size

The QP, average and CISPR-average[1] detectors have dwell time requirements in order to output correct results. For the QP, a one second dwell time is required in order to fully charge and discharge the filters in the detector. Both average detectors require 100 ms or more. Some spectrum analyzers now offer *zero-span*. This capability is another work around to make the spectrum analyzer work like a test receiver and provide this dwell feature.

Spectrum analyzers can be used for EMI, but various work-around methods must be used in order for the results to be accurate.

Obviously, there are many opportunities for error. Incorrect sub-ranging, violation of dwell time requirements, use of incorrect RBW filters, overloads, and many other issues force us to conclude that the spectrum analyzer may not be the best tool for the job.

CISPR, EN, FCC, MIL-STD and all the other standards bodies recommend using a scanning receiver for EMI applications for all of the above reasons. With a scanning receiver, what you set is what is measured, and these settings are listed right in the test standard.

Parameters which are called out in the standard, entered directly as a test parameter, and now the operator needs only to press start. No sub-ranging, no zero-spanning, no mental conversions from voltage to fieldstrength. Furthermore, with automatic attenuators and preselection, it is possible for a compliant test to run without intervention.

A scanning receiver is a better tool for EMI testing for the below key features:

- Measurement Points: a scanning receiver will measure many tens of thousands of points if needed. This level of accuracy is much improved over a spectrum analyzer's 500 or 1000 points.
- Tune & Dwell: the second key feature is the tune and dwell capability native to a scanning receiver. Dwell time is set as a keystroke parameter, and violations to dwell time requirements of the various detectors are often "flagged" as incorrect.

[1] the differences between a typical average detector and a CISPR-average detector have to do with the averaging time constants used

- EMI Specificity: This key feature rolls up all the issues discussed during the spectrum analyzer exploration, namely the availability of EMI specific features such as 6 dB RBW filters, transducer sets, limit lines and preselector filters.

- Automatic Control: scanning receivers can also take advantage of automatic control of certain parameters. Remember at the beginning when it was stated that certain modes could be forced on a spectrum analyzer that will yield incorrect results. This is also true for receivers, but much less likely since the receiver will "take care of itself" if left in auto-control mode. Automatic control of RF attenuation, preselection filtering, preamplification settings, RBW settings, and the step size is common. Auto-control of these settings can keep the user out of trouble in most cases. The autocontrol of these parameters will follow what is called out in the standards. Since no one starts as an expert, EMI novices may be saved from collecting incorrect data, and worse, making judgments on bad data.

Similar to spectrum analyzers, there are also disadvantages to test receivers. Scanning receivers are the right tool for the job mainly because they were built with EMI in mind. Specialized tools often cost more, and have limited use outside of the area of specialization.

C.1 Scanning Receiver

Conformance test measurements are normally taken with a scanning receiver, which is optimized for the purpose of taking EMC measurements. Typical costs for a complete receiver system to cover the range 10kHz to 1GHz can be anywhere between 15,000/60,000 dollars.

Early measuring receivers were manually tuned and the operator had to take readings from the meter display at each frequency that was near to the limit line. This was a lengthy procedure and prone to error. The current generation of receivers are fully automated and can be software controlled via an IEEE-488 standard bus; this allows a PC-resident program to take measurements with the correct parameters over the full frequency range of the test, in the minimum time consistent with gap-free coverage. Results are stored in the PC's memory and can be processed or plotted at will. The distinguishing features of a scanning receiver compared to a spectrum analyser are:

- lack of a wide spectrum display for instantaneous diagnostics: the receiver output is provided at a spot frequency;

- very much better sensitivity, allowing signals to be discriminated from the noise at levels much lower than the emission limits;
- robustness of the input circuits, and resistance to overloading;
- intended specifically for measuring to CISPR standards, with bandwidths, detectors and signal circuit dynamic range tailored for this purpose;
- frequency and amplitude accuracy better than the cheaper spectrum analysers;
- two units may be required,

C.2 Spectrum Analyzer

A fairly basic spectrum analyser is considerably cheaper than a scanning receiver (typically 10-15,000) and is widely used for "quick-look" testing and diagnostics. The instantaneous spectrum display is extremely valuable for confirming the frequencies and nature of offending emissions, as is the ability to narrow-in on a small part of the spectrum. When combined with a tracking generator, a spectrum analyser is useful for checking the HF response of circuit networks. Basic spectrum analysers are not an alternative to a scanning receiver in a full compliance set-up because of their limited sensitivity and dynamic range, and susceptibility to overload. Figure [] shows the block diagram of a typical spectrum analyser. The input signal is fed straight into a mixer which covers the entire frequency range of the analyser with no advance selectivity or preamplification. The consequences of this are threefold: firstly, the noise figure is not very good, so that when the attenuation due to the transducer and cable is taken into account, the sensitivity is hardly enough to discriminate signals from noise at the lower emission limits (see section [] later). Secondly, the mixer diode is a very fragile component and is easily damaged by momentary transient signals or continuous overloads at the input. If you take no precautions to protect the input, you will find your repair bills escalating quickly. Thirdly, the energy contained in broadband signals can overload the mixer and drive it into non-linearity even though the energy within the detector bandwidth is within the instrument's apparent dynamic range.

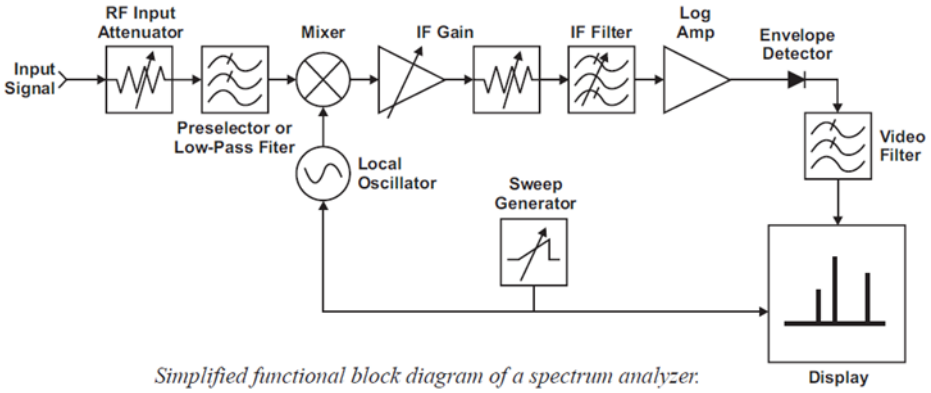


Figure C.1: Simplified heterodyne structure of a spectrum analyzer

C.3 Bandwidth

The actual value of an interference signal that is measured at a given frequency depends on the bandwidth of the receiver and its detector response. These parameters are rigorously defined in a separate standard that is referenced by all the commercial emissions standards that are based on the work of CISPR, notably EN 55011, 55013, EMC for Product Designers 85 55014 and 55022. This standard is CISPR publication 16-1.

CISPR 16-1 splits the measurement range of 9kHz to 1000MHz into four bands, and defines a measurement bandwidth for quasi-peak detection which is constant over each of these bands (Table []). Sources of emissions can be classified into narrowband, usually due to oscillator and signal harmonics, and broadband, due to discontinuous switching operations, commutator motors and digital data transfer. The actual distinction between narrowband and broadband is based on the bandwidth occupied by the signal compared with the bandwidth of the measuring instrument. A broadband signal is one whose occupied bandwidth exceeds that of the measuring instrument. Thus a signal with a bandwidth of 30kHz at 20MHz (CISPR band B) would be classed as broadband, while the same signal at 40MHz (band C) would be classed as narrowband.

C.4 Noise level versus bandwidth

The indicated level of a broadband signal changes with the measuring bandwidth. As the measuring bandwidth increases, more of the signal is included within it and hence the indicated

level rises. The indicated level of a narrowband signal is not affected by measuring bandwidth. Noise, of course, is inherently broadband and therefore there is a direct correlation between the "noise floor" of a receiver or spectrum analyser and its measuring bandwidth: minimum noise (maximum sensitivity) is obtained with the narrowest bandwidth. The relationship between noise and bandwidth is given by equation ([]):

For instance, a change in bandwidth from 10kHz to 120kHz would increase the noise floor by 10.8dB.

C.5 Detector

There are three kinds of detector in common use in RF emissions measurements: peak, quasi peak and average. The characteristics are defined in CISPR 16-1 and are different for the different frequency bands. Interference emissions are rarely continuous at a fixed level. A carrier signal may be amplitude modulated, and either a carrier or a broadband emission may be pulsed. The measured level which is indicated for different types of modulation will depend on the type of detector in use. Figure [] shows the indicated levels for the three detectors with various modulation shapes.

C.5.1 Peak

The peak detector responds near-instantaneously to the peak value of the signal and discharges fairly rapidly. If the receiver dwells on a single frequency the peak detector output will follow the "envelope" of the signal, hence it is sometimes called an envelope detector. Military specifications make considerable use of the peak detector, but CISPR emissions standards do not require it at all. However its fast response makes it very suitable for diagnostic or "quick-look" tests, and it can be used to speed up a proper compliance measurement as is outlined in section [].

C.5.2 Average

The average detector, as its name implies, measures the average value of the signal. For a continuous signal this will be the same as its peak value, but a pulsed or modulated signal will have an average level lower than the peak. EN 55022 and its derivative standards call for an average detector measurement on conducted emissions, with limits which are 10-13dB lower than the quasi-peak limits. The effect of this is to penalize continuous emissions with respect to pulsed

interference, which registers a lower level on an average detector []. A simple way to make an average measurement on a spectrum analyser is to reduce the post-detector "video" bandwidth to well below the lowest expected modulation or pulse frequency [].

C.5.3 Quasi-peak

The quasi-peak detector is a peak detector with weighted charge and discharge times (Table []) which correct for the subjective human response to pulse-type interference. Interference at low pulse repetition frequencies (PRF) is said to be subjectively less annoying on radio reception than that at high PRFs. Therefore, the quasi-peak response de-emphasizes the peak response at low PRFs, or to put it another way, pulse-type emissions will be treated more leniently by a quasi-peak measurement than by a peak measurement. But to get an accurate result, the measurement must dwell on each frequency for substantially longer than the QP charge and discharge time constants. Since CISPR-based tests have historically been intended to protect the voice and broadcast users of the radio spectrum, they lay considerable emphasis on the use of the QP detector. There is a point of view which suggests that with the advent of digital telecommunications and broadcasting this will change, since digital signals are affected by impulsive interference in a quite different way. A study group within CISPR is looking at other means of detector weighting, but at the time of writing there is little to indicate that a new specification is imminent.

C.5.4 Measurement time

Both the quasi-peak and the average detector require a relatively long time for their output to settle on each measurement frequency. This time depends on the time constants of each detector and is measured in hundreds of milliseconds. When a range of frequencies is being measured, the conventional method is to step the receiver at a step size of around half its measurement bandwidth, in order to cover the range fully without gaps (for the specified CISPR filter shape, the optimum step size is around 0.6 times the bandwidth, to give the largest step size consistent with maintaining the accuracy of measurement of any signal). For a complete measurement scan of the whole frequency range, as is required for a compliance test, the time taken is given by:

If the dwell time is restricted to three time constants, the time taken to do a complete quasi-peak sweep from 150kHz to 30MHz turns out to be 53 minutes. For an average measurement the

scan time would be even longer, were it not for the way in which the average limit is applied. The difference between the quasi-peak and average limits is at most 13dB (in CISPR 22, class A) and this difference occurs at a PRF of 1.8kHz. The decisive value for lower PRFs is always the QP indication. Therefore the average indication only has to be accurate for modulated or pulsed signals above this PRF, and this can be ensured with only a short dwell time, such as 1ms. But with quasi-peak, the dwell time must be increased to ensure that the peaks are captured and indicated correctly. It should be at least 1 second, if the signals to be measured are unknown. This has repercussions on the test method, as is discussed later. It places correspondingly severe restrictions on the sweep rate when you are using a spectrum analyser [].

C.6 Narrowband and Broadband

In the field of EMC, the two main categories of signals encountered are of particular importance: narrowband signals and broadband signals. The International Electrotechnical Vocabulary (IEV) defines a narrowband disturbance as *an electromagnetic disturbance, or component thereof, which has a bandwidth less than or equal to that of a particular measuring apparatus, receiver or susceptible device.* Consequently, a broadband disturbance is defined as *an electromagnetic disturbance which has a bandwidth greater than that of a particular measuring apparatus, receiver or susceptible device.* This means that the classification of a signal as narrowband or broadband is determined by the occupied frequency spectrum of the signal under investigation, relative to the resolution bandwidth (RBW) of the instrument used for measurement. If the signal spectrum is completely contained in the passband of the IF filter, it is defined as a narrowband signal. The general definition of a narrowband and broadband signal is depicted in Figure []. It is important to note that continuous wave (CW) signals are a specific case of narrowband signals, since they consist of only one spectral line which is within the passband of the intermediate frequency (IF) filter. This case is depicted in Figure 2 (right). If the occupied signal spectrum exceeds the bandwidth of the filter, the signal is considered to be broadband. This is the case for the spectra of pulses (which are coherent signals) and noise (non-coherent signals). This scenario is shown in Figure 1 (left).

Narrowband and broadband signals can be generated by a variety of sources and usually represent different interference potentials for radio services. Very often an interference spectrum from equipment under test (EUT) contains both signal types. Since both signal categories require

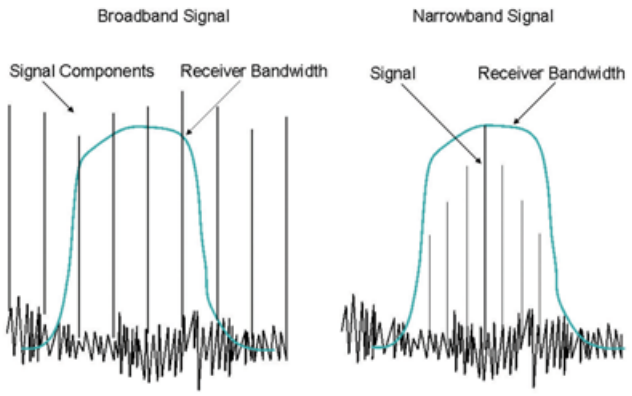


Figure C.2: Generic definition of narrowband and broadband signals

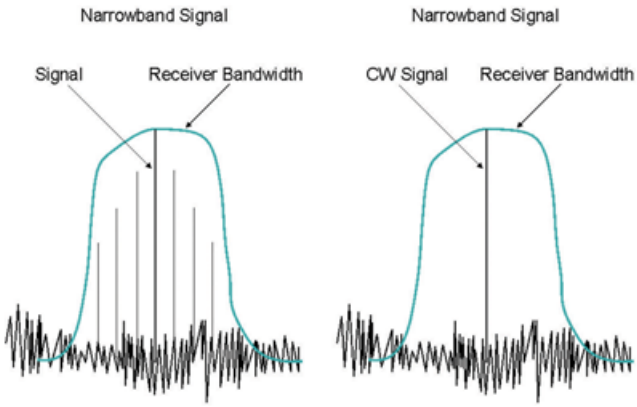


Figure C.3: Two different types of narrowband signals

a different interpretation of the result measured with a spectrum analyzer or EMI receiver, it is essential to know the characteristics of a signal in order to correctly determine its frequency and amplitude. In some cases, the characteristics must be known in order to select the correct limit for the determination of EUT compliance. The measurement results displayed on these instruments are also dependent on some control settings, such as the sweep time and resolution bandwidth. Their impact on the measurement of signal parameters, like frequency and pulse width, must be understood to avoid erroneous interpretations of measurement results.

Most modern scanning receivers, spectrum analyzers and traditional EMI receivers are super-heterodyne receivers using one or multiple stages to convert the frequency of the RF input signal

to a fixed IF. This is achieved by mixing the unknown signal with a local oscillator (LO) signal in a mixing stage. Since a mixer is a non-linear device, its output includes not only the two original signals at the input but also their harmonics and the sums and differences of the input signals and their harmonics. If any of the mixed signals falls within the passband of the IF filter, it is further processed at the IF and finally displayed. After the filtering, the signal is amplified by either a logarithmic or linear amplifier, rectified by the envelope detector, possibly filtered by a low-pass filter (*Video Filter*) and finally graphically or numerically displayed.

EMI receivers as well as spectrum analyzers convert the IF signal to a video signal using an envelope detector. These signals have a frequency range from zero (dc) to some upper frequency which is determined by the detection circuit elements. In its simplest form an envelope detector consists of a diode followed by a parallel RC combination, as shown in Figure 3 (top). The output of the IF chain is applied to the detector. The time constants of the detector are chosen such that the voltage across the capacitor equals the peak value of the IF signal at all times which requires a fast charge and slow discharge time. In case the preceding resolution bandwidth of the receiver has only one spectral line in its passband (meaning, a CW signal is being measured), the IF signal is a steady sine wave with a constant peak amplitude. The output of the envelope detector will be a constant dc voltage without any variation for the detector to follow, as depicted in Figure 3 (top). However, often times there is more than one signal in the IF filter passband. For instance, in case of two sine waves, as shown in Figure 3 (bottom), these interact to create a beat note, and the envelope of the IF signal varies according to the phase change between the two sine waves. The maximum rate at which the envelope of the IF signals can change is determined by the resolution bandwidth. Since IF filters of receivers are not rectangular, the charge time of the detector needs to be a fraction of the reciprocal of the IF bandwidth (e.g. one-tenth) to obtain the envelope of the IF signal.

Specific instrument parameters like the selected detector, resolution bandwidth and sweep time do have an impact on the displayed measurement result, dependent on the characteristics of the signal to be measured. Therefore, they can be used to determine if a signal is broadband or narrowband.

When using spectrum analyzers or receivers for EMI troubleshooting measurements, no standard is to be applied that calls out a specific setting of the IF bandwidth. Therefore, it is mandatory

to know if a measured signal is displayed as a narrowband or broadband signal in order to correctly determine the frequency of signals. Furthermore, some EMI standards like the older MIL-STD 461B provide two different limits for narrowband and broadband signals, which require a determination of the signal characteristic as part of the compliance measurement process. In both cases, suitable discrimination methods are necessary to determine a signal to be narrowband or broadband.

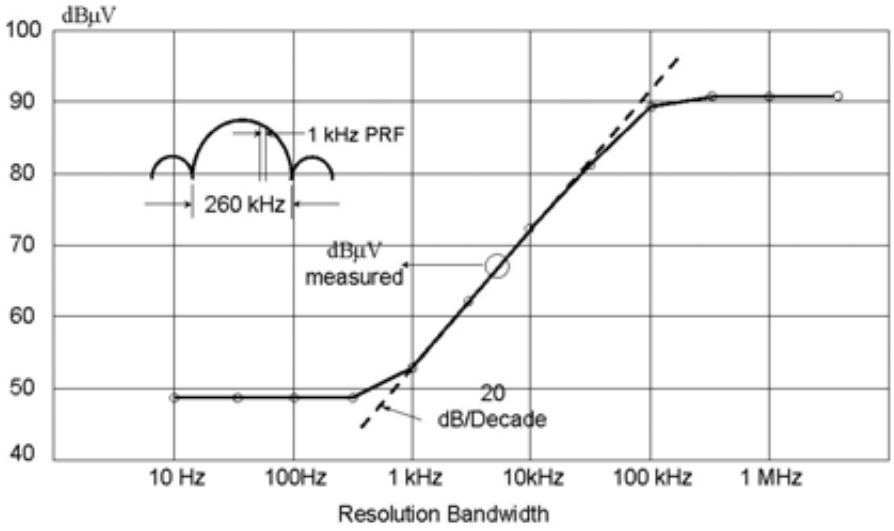


Figure C.4: Impact of resolution bandwidth setting on measured amplitude of broadband signal

As mentioned before, the reference for a signal to be broadband or narrowband is the resolution bandwidth setting of the test instrument used for the measurement. Some standards suggest the variation of the resolution bandwidth of the test instrument and observation of the resultant amplitude change of the signal under investigation. It is stated that an amplitude change, introduced by the variation of the resolution bandwidth, indicates the presence of a broadband signal. Conversely, if no amplitude change is observed, the signal is considered to be narrowband. Figure 4 depicts the measurement of an impulsive signal with a pulse repetition frequency (PRF) of 1 kHz and a pulse width of 7.7 μsec. If this signal is initially measured with a 100 Hz resolution bandwidth and the bandwidth is changed to 300 Hz, no change in amplitude is observed. Bandwidth settings that are lower than the PRF of the signal to be measured will result in the resolution of each individual spectral component. This will result in a narrowband measurement of the signal. A further increase in resolution bandwidth to 10 or 30 kHz will result in multiple spectral components located

in the passband of the IF filter. A change in resolution bandwidth will result in an amplitude change of the measured signal, since wider IF bandwidths will encompass more spectral components and thus result in higher levels at the filter output. Using bandwidth settings that are wider than the PRF will indicate the presence of a broad band signal, since amplitude changes can be observed. Further increases of the resolution bandwidth to 1 MHz or greater will not yield changes in signal amplitude. This would indicate the presence of a narrowband signal, which is incorrect, in accordance with the definition. Large resolution bandwidths encompass the main spectral components of a signal (i.e., the main lobe and the first two side lobes of the spectrum), and do not lead to changes in the measured amplitude. Therefore, the variation of the resolution bandwidth as a means for determining the signal characteristic is of limited usefulness. Further information about the signal to be measured is required to avoid erroneous results. In addition, a change of bandwidth represents a change of the reference for the narrowband-broadband discrimination, which is very often neither permissible (by EMI standards) nor desirable for troubleshooting applications. It should be noted that this method provides conclusive results only when the signal under investigation is a CW signal.

A second discrimination for the determination of signal characteristics is the amplitude comparison between a peak and an average measurement. Both measurements are preferably made with the same instrument settings, especially with an identical resolution bandwidth setting. If no amplitude changes are observed between the two measurements, a signal is considered narrowband. A signal is considered broadband if an amplitude change between the two measurements is observed, with the average measurement yielding the lower amplitude. In practice, EMI standards that call out this discrimination method, like CISPR 25, specify an amplitude difference of, for example, 6 dB which is used as a decision criterion. Per CISPR 25, a signal is considered to be narrowband if the amplitude difference between the peak and average detected signal is less than 6 dB. If the amplitude difference is greater than 6 dB, the signal is determined to be broadband. This approach is meaningful since the relative amplitude accuracy of the instrument is to be considered as well as other uncertainty factors that are introduced by different instrument settings between the two measurements (e.g., change of reference level setting).

Appendix D

Standards and normative

No equipment can sustain gracefully unlimited levels of electromagnetic aggression, without suffering an impaired or reduced operation at a certain point. When designing to achieve an increased EMC behavior, a realistic assessment of the threat levels during normal operation must be made. EMC measurement setups for automotive electronic systems are defined in standards such as in the International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques) (CISPR) 25 for parasitic emissions, and in the International Organization for Standardization (ISO) 11452 for susceptibility to EMI. Since IC's are generally the main cause of EMI related malfunctioning and disturbance in electronic equipment, there has recently been considerable demand for simple, reliable, and standardized measurement methods focusing only on IC's.

The International Electrotechnical Commission (IEC) is one of the international standards organizations which are addressing the need for standardized IC EMC test methods. The IEC's IC EMC standards are sponsored by the IEC sub-committee (SC) 47A (integrated circuits), which is a part of the IEC technical committee (TC) 47 (semiconductor devices). SC 47A created working group (WG) 9 to prepare international standards for test procedures and measurement methods to evaluate the EMC of ICs. Where possible, WG 9 coordinates the preparation of its standardized test methods with methods standardized or in progress with industry and national standards bodies including, but not limited to, the Society of Automotive Engineers (SAE) in the United States and the Verband der Elektrotechnik, Elektronik und Informationstechnik (VDE) in Germany. SC 47A, WG 9 has released two main standards for measuring the EMC of integrated circuits: the first one (released in 2001) for measuring radiated and conducted emission [IEC 61967], and the second one (released in 2003) for measuring immunity [IEC 62132].

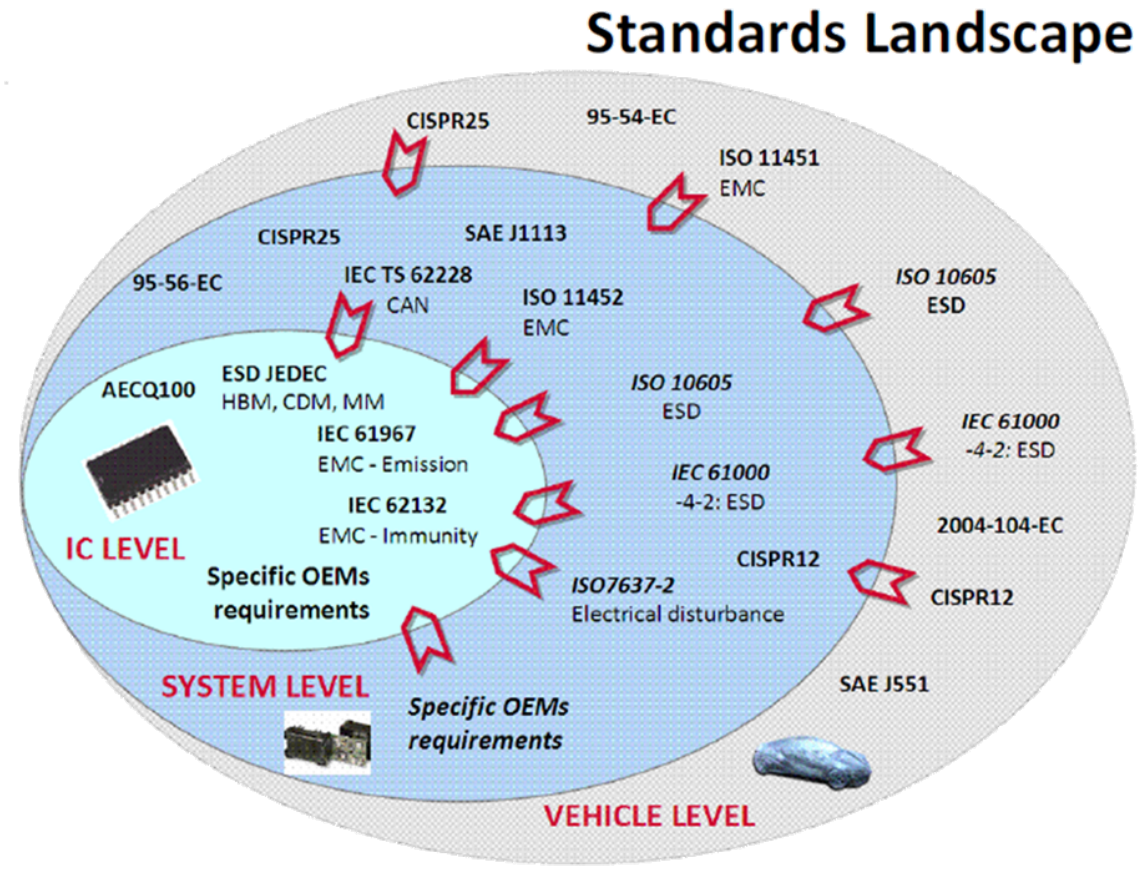


Figure D.1: International EMC standards and normative.

D.1 Precompliance-, Compliance- and Full Compliance

There is no specific direct definition for Precompliance-tests, generally all non conform measurements are handled as Precompliance tests.

- Precompliance tests are mesurements with deviation from the basic standard. From diagnosis measurements during developement up to preparation for certification testing (Precertification).
- Compliance tests are to be done conform with the basic standard, means without any deviation and in accordance with the latest standard issue e.g. CISPR 16-1-1 (Ed 3) with test instruments providing the performance for 20 Hz criterion for pulse repetition freqency (PRF).

- Full Compliance tests are to be done fully compliant without deviation from latest edition CISPR 16-1-1 (Ed 3) with test instruments and measurement performance down to 1 Hz pulse repetition frequencyz, incl. isolated pulse.

D.2 CISPR 25, IEC: 2008, Edition: 3.0

International Standard CISPR 25 has been prepared by CISPR subcommittee D: Electromagnetic disturbances related to electric/electronic equipment on vehicles and internal combustion engine powered devices [24].

CISPR 25 is the primary automotive standard for conducted emissions, containing tests and limit levels for both power and signal line conducted noise. Automotive radiated emissions testing is to ensure the ESA, and hence completed vehicle, does not interfere with equipment external to the vehicle as well as on-board receivers, automotive conducted emissions tests are purely to ensure the ESA does not interfere with other on-board equipment. The wired supply and signalling system for a vehicle is a self contained system and does not directly interface with off-board equipment while in use. There are two test methods for conducted emissions in CISPR 25; measurements via a LISN ($50\Omega/5\mu H$) for power line emissions and measurements from a current probe for signal/control line emissions. There are again 5 classes of limit lines that covers the frequency range 150 kHz to 108 MHz. OEM specifications utilise the test set-up of CISPR 25 for power line emissions and apply their own limits (which are often harder than specified in CISPR 25), most filling in the omitted test bands. A few of the OEM specifications extend the test frequency range (e.g. BMW cover 30 kHz to 120 MHz).

Overall treated, the emission is limited over the whole frequency range (150kHz-108MHz). For several applications like ABS the emission specification can change. This International Standard is designed to protect on-board receivers from disturbances produced by conducted and radiated emissions arising in a vehicle.

The third edition cancels and replaces the second edition published in 2002. The following significant changes were made with respect to the previous edition:

- addition of required measurements with both an average detector and a peak or quasipeak detector;

- addition of methods and limits for the protection of new analogue and digital radio services,

which cover the frequency range up to 2500 MHz;

- deletion of narrowband / broadband determination.

This standard:

- establishes a test method for measuring the electromagnetic emissions from the electrical system of a vehicle;
- sets limits for the electromagnetic emissions from the electrical system of a vehicle;
- establishes test methods for testing on-board components and modules independent from the vehicle;
- sets limits for electromagnetic emissions from components to prevent objectionable disturbance to on-board receivers;
- classifies automotive components by disturbance duration to establish a range of limits.

In all cases the EUT shall conform with the average limit. The EUT shall also conform with either peak or quasi-peaks limits as follows:

- For frequencies where both peak and quasi-peak limits are defined, the EUT shall conform with either the peak or the quasi-peak limits (as defined in the test plan).
- For frequencies where only peak limits are defined, the EUT shall conform with the peak limit.

The general procedure applicable for all frequency bands is described in Figure D.2.

NOTE 1: The conformance should normally be obtained by compliance to both average and peak limits or both average and quasi-peak limits unless the test plan defines that conformance can be obtained by compliance to the single appropriate limit) (depending on the case, peak, or average, or quasi-peak).

NOTE 2: Because measurement with peak detector is always higher or equal to measurement with average detector and applicable peak limit is always higher or equal to applicable average limit, this single detector measurement can lead to a simplified and quicker conformance process.

NOTE 3: This flow-chart is applicable for each individual frequency, e.g. only frequencies that are above the applicable limit need be remeasured with average or quasi-peak detector.

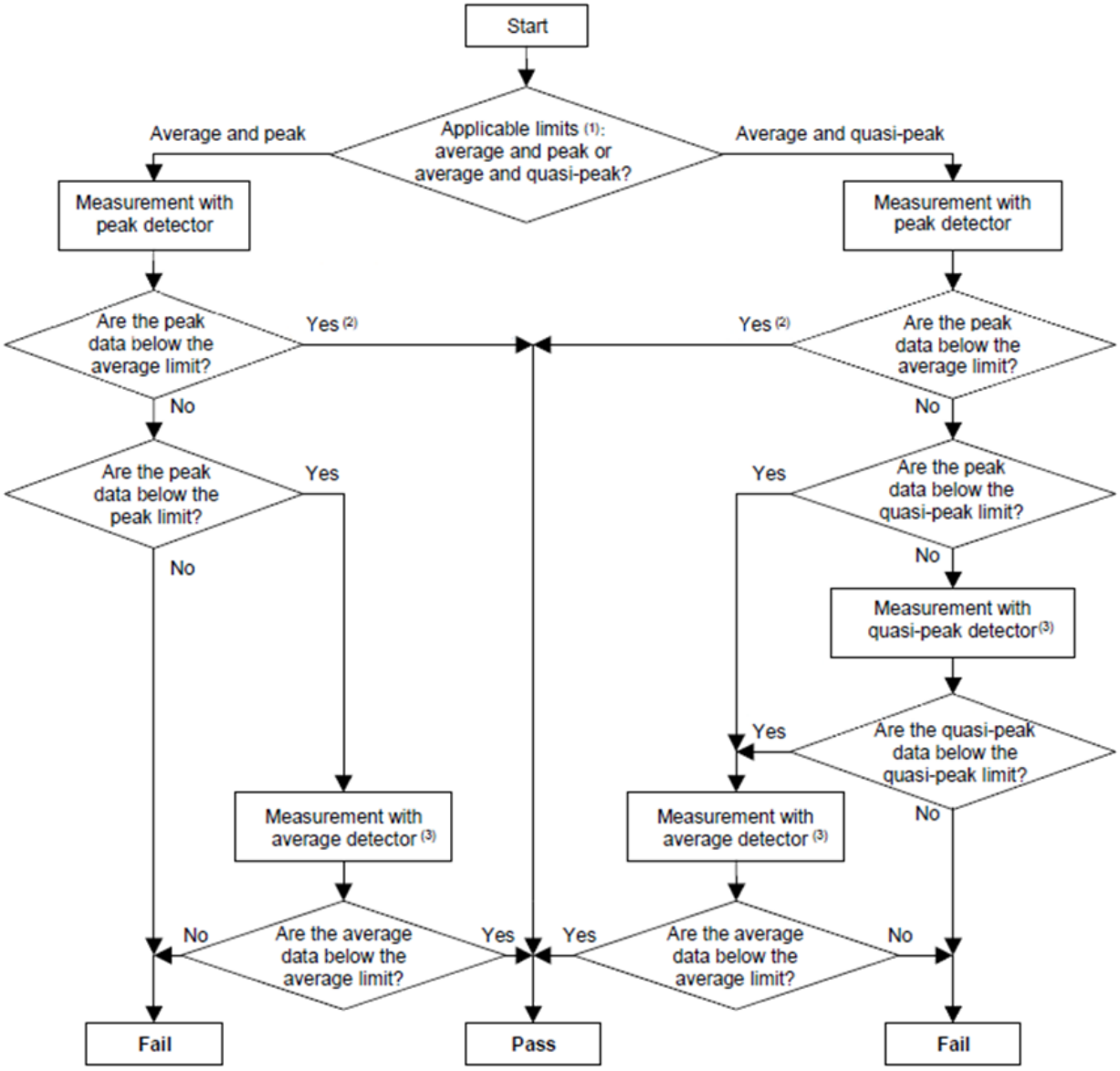


Figure D.2: Method of determination of conformance for all frequency bands

The measuring instrument shall comply with the requirements of CISPR 16-1-1. Either manual or automatic frequency scanning may be used. However Annex D of CISPR 16-2-3 explains the differences between the CISPR AV detector and an AV detector (complying with CISPR 16-1:1999). For the purpose of this standard either detector may be used, since the pulse repetition rate for internal combustion engines is above 10 Hz.

NOTE 1: Spectrum analysers and scanning receivers are particularly useful for disturbance

measurements. The peak detection mode of spectrum analysers and scanning receivers provides a display indication which is never less than the quasi-peak indication for the same bandwidth. It may be convenient to measure emissions using peak detection because of the faster scan possible than with quasi-peak detection.

NOTE 2: A preamplifier may be used between the antenna and measuring instrument in order to achieve the 6 dB noise floor requirements. If a preamplifier is used to achieve the 6 dB noise floor requirement, the laboratory should establish a procedure to avoid overload of the preamplifier, such as using a step attenuator.

Spectrum analysers may be used for performing compliance measurements to this standard providing the precautions cited in CISPR 16-1-1 on the use of spectrum analysers are adhered to and that the broadband emissions from the product being tested have a repetition frequency greater than 20 Hz. The minimum scan time and recommended bandwidth are listed in Table D.1.

Frequency range MHz	Peak detection		Quasi-peak detection		Average detection	
	RBW at -3 dB	Scan time	RBW at -6 dB	Scan time	RBW at -3 dB	Scan time
0,15 - 30	9/10 kHz	10 s / MHz	9 kHz	200 s / MHz	9/10 kHz	10 s / MHz
30 - 108	100/120 kHz	100 ms / MHz	120 kHz	20 s / MHz	100/120 kHz	100 ms / MHz

Table D.1: CISPR25: Spectrum analyser parameters.

When a spectrum analyser is used for measurements, the video bandwidth shall be at least three times the resolution bandwidth (RBW). The dwell time of the scanning receiver shall be adjusted for the CISPR frequency band and detection mode used. The minimum dwell time, maximum step size and recommended bandwidth (BW) are listed in Table D.2.

A line impedance stabilization network serves three purposes:

- The LISN isolates the power mains from the EUT. The power supplied to the EUT must be as clean as possible. Any noise on the line will be coupled to the EMI receiver and interpreted as noise generated by the EUT.

- The LISN isolates any noise generated by the EUT from being coupled to the power mains. Excess noise on the power mains can cause interference with the proper operation of other

Frequency range MHz	Peak detection			Quasi-peak detection			Average detection		
	BW at -6 dB	Step size	Dwell time	BW at -6 dB	Step size	Dwell time	BW at -6 dB	Step size	Dwell time
0,15 - 30	9 kHz	5 kHz	50 ms	9 kHz	5 kHz	1 s	9 kHz	5 kHz	50 ms
30 - 108	120 kHz	50 kHz	5 ms	120 kHz	50 kHz	1 s	120 kHz	50 kHz	5 ms

Table D.2: CISPR25: Scanning receiver parameters.

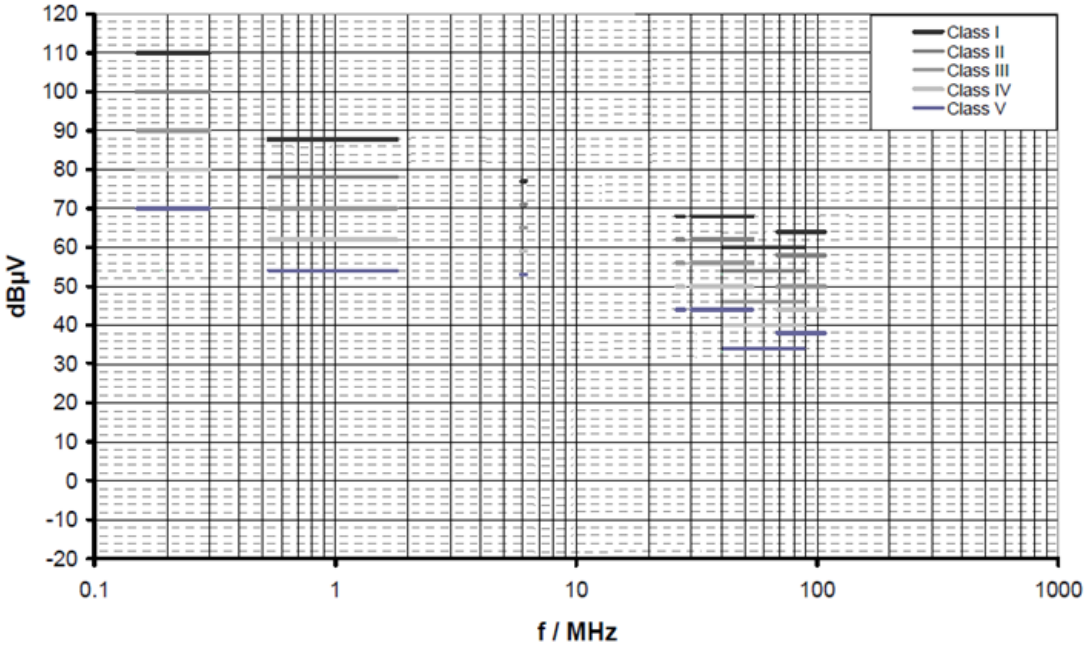


Figure D.3: Conducted emissions CISPR 25 limits for peak detector.

devices on the line.

- The signals generated by the EUT are coupled to the EMI receiver using a high-pass filter, which is part of the LISN. Signals which are in the pass band of the high-pass filter show a 50Ω load, which is the input to the EMI receiver.

The diagram in Figure A-1 below shows the circuit for one side of the line relative to earth ground. The $1\mu F$ capacitor in combination with the $5\mu H$ inductor, is the filter that isolates the mains from the EUT. The $5\mu H$ inductor isolates the noise generated by the EUT from the mains. The $0.1\mu F$ capacitor couples the noise generated by the EUT to the EMI receiver. At frequencies

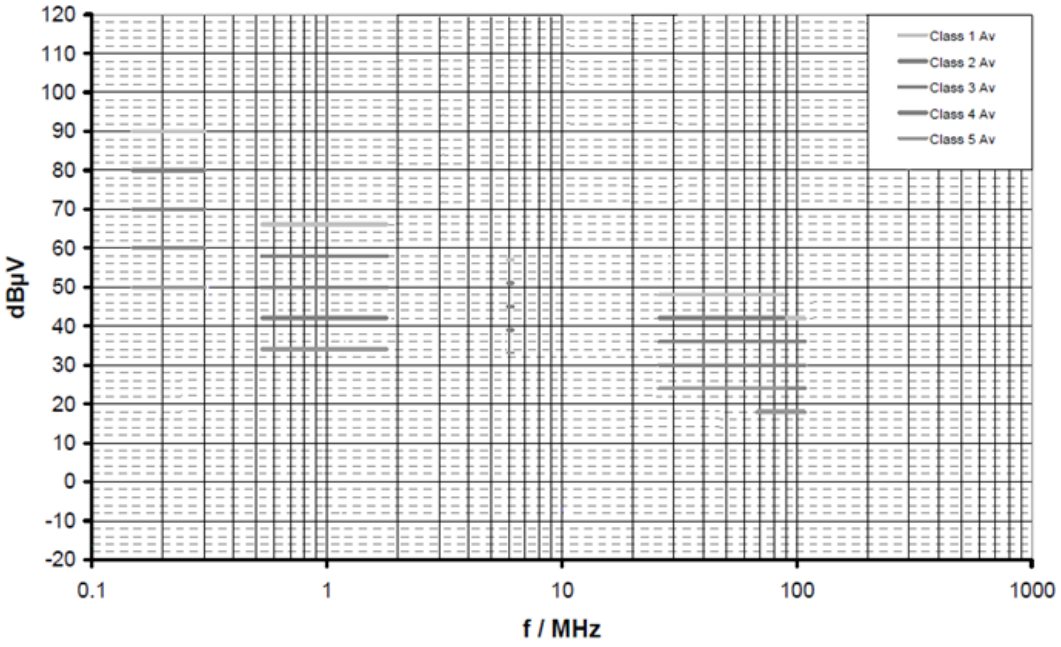


Figure D.4: Conducted emissions CISPR 25 limits for average detector.

Service/ Band	Frequency [MHz]	Levels in [dB(µV)]														
		Class 1			Class 2			Class 3			Class 4			Class 5		
		Peak	Quasi-Peak	Average	Peak	Quasi-Peak	Average	Peak	Quasi-Peak	Average	Peak	Quasi-Peak	Average	Peak	Quasi-Peak	Average
BROADCAST																
LW	0.15-0.30	110	97	90	100	87	80	90	77	70	80	67	60	70	57	50
MW	0.53-1.80	86	73	66	78	65	58	70	57	50	62	49	42	54	51	34
SW	5.9-6.2	77	64	57	71	58	51	65	52	45	59	46	39	53	40	33
FM	76-108	62	46	42	56	43	36	50	37	30	44	31	24	38	25	18
TV Band I	41-88	58	-	48	52	-	42	46	-	36	40	-	30	34	-	24
Band	> 108	Conducted emission – Voltage method not applicable														
MOBILE SERVICES																
CB	26-28	68	55	48	62	49	42	56	43	36	50	37	30	44	31	24
VHF	30-54	68	55	48	62	49	42	56	43	36	50	37	30	44	31	24
VHF	68-87	62	49	42	56	43	36	50	37	30	44	31	24	38	25	28
Band	> 87	Conducted emission – Voltage method not applicable														

Table D.3: CISPR 25 levels in dB·μV divided by class and by detector.

above 150 kHz, the EUT signals are presented with a 50Ω impedance.

D.3 IEC 61967 - part 4

IEC 61967-4: Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions - (1Ω/150Ω) direct coupling method [25]

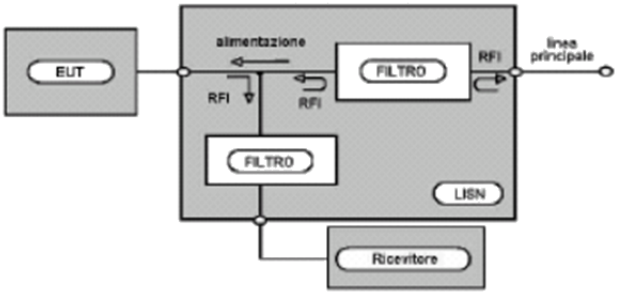
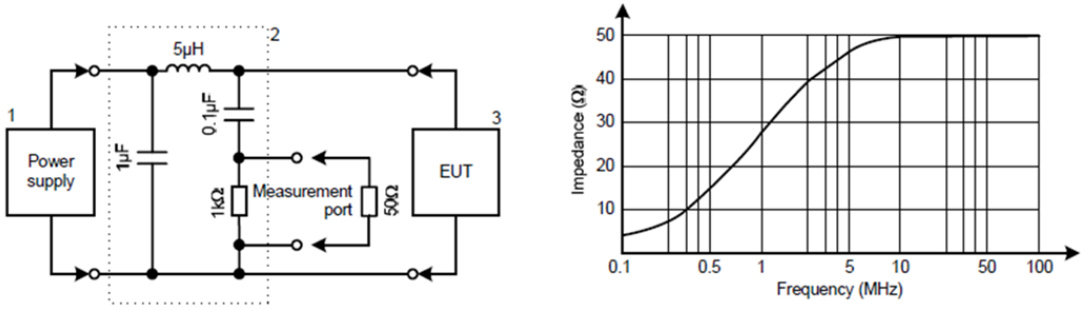


Figure D.5: CISPR 25 Artificial Network test setup



(a) (b)

Figure D.6: CISPR 25 Artificial Network: a) equivalent circuit; b) impedance behaviour

The emission of an IC is generated by sufficiently fast changes of voltages and currents inside the IC. These changes drive RF currents inside and outside the IC. The RF currents cause conducted EME, which is mainly distributed via the IC pins conductor loops in the printed circuit board (PCB) and the cabling. These loops are regarded as the emitting loop antennas. In comparison to the dimension of these loops, the loops in the internal IC structure are considered to be small. The RF currents that accompany ICs action are different in amplitude, phase and spectral content. Any RF current has its own loop that returns to the IC. All loops return mostly via the ground or supply connection back to the IC.

This conducted EME test setup addresses the measurement of voltage spectrum of output drivers. RF currents can also flow in loops on the PCB and the attached wires. These loops are regarded as the emitting antennas. The conducted EME of an IC pin can be measured with an impedance network of 150Ω which represents the typical antenna impedance of lines, as specified in IEC 61000-4-6. Based on IEC 61000-4-6, a cabling network can be represented in most cases

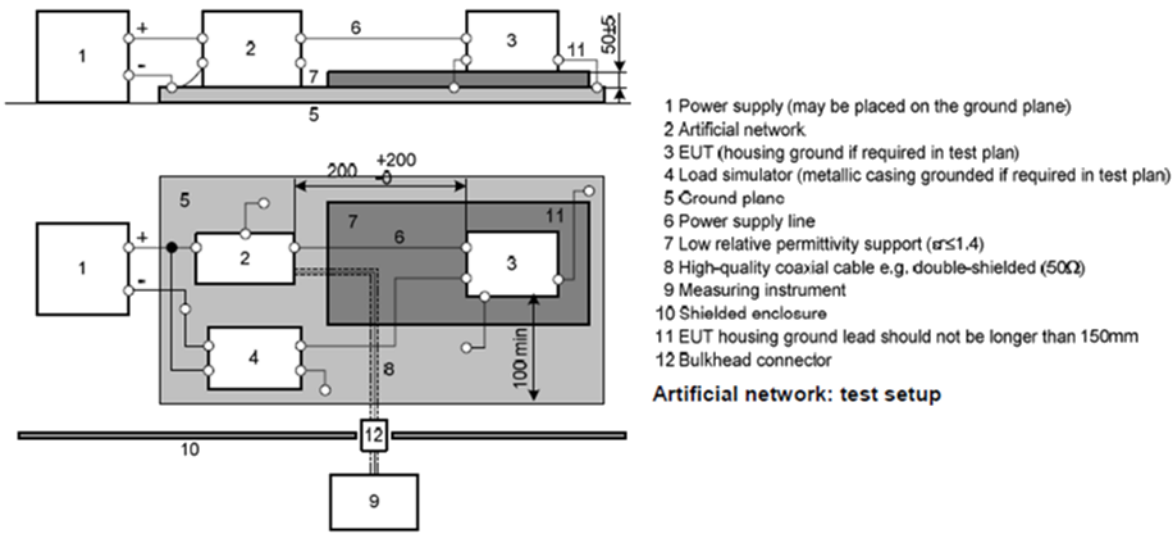


Figure D.7: CISPR 25 Artificial Network test setup

by an antenna with an impedance of 150Ω. In order to get accurate measurement results over the full frequency range, a termination network of $150\Omega \pm 20\Omega$ shall be used. Usual measurement equipment provides an input impedance of 50Ω so that the matching network shall match the signal line impedance to the equipment impedance. The circuitry is shown in Figure D.8, and the characteristics of the impedance matching network used are shown in Table D.4.

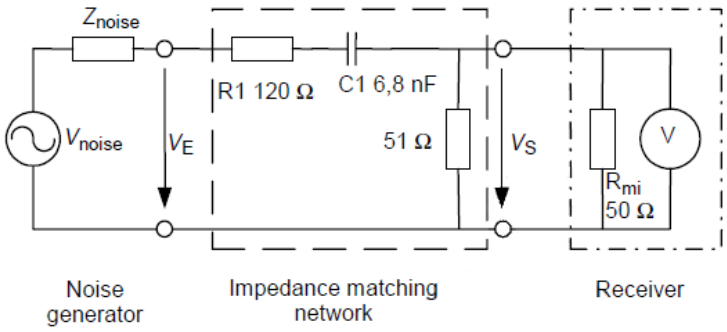


Figure D.8: Impedance matching network corresponding with IEC 61000-4-6

The test set-up shall be in accordance with Figure D.9. This general test configuration can be built up in the form of a special test configuration or in any other configuration, e.g. also in a real application.

Frequency range B_f	150 kHz – 1 GHz
Input impedance with 50 Ω termination Z_i	145 Ω ± 20 Ω
Insertion loss within a 50 Ω system	0,2586 (–11,75 dB ± 2 dB)
Voltage ratio V_{out} / V_{in}	0,1738 (–15,20 dB ± 2 dB)

Table D.4: Characteristics of the impedance matching network

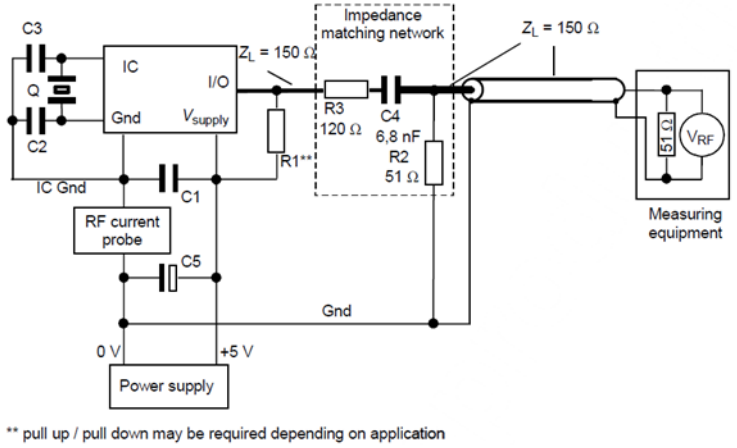


Figure D.9: General test configuration 150Ω-method

A *global pin* carries a signal or power, which enters or leaves the application board. A *local pin* carries a signal or power, which does not leave the application board. It remains on the application PCB as a signal between two components with or without additional EMC components.

All global and supply pins have to be measured. At a global driver pins the emission of the direct pin function, the crosstalk behavior pin to core and the crosstalk behavior port to pin can be measured. Local pin measurements are not mandatory. Local pin measurements are optional and should be performed only on special request or if no pin could be defined as a global pin for measurements.

D.3.1 Definition of emission levels

The diagram in Figure D.11 defines the conducted emissions classification levels used to define the overall envelope of the measured emissions. This diagram can be used to classify both the RF current measured with the RF current probe and the RF voltage at IC pins, measured using the impedance matching network.

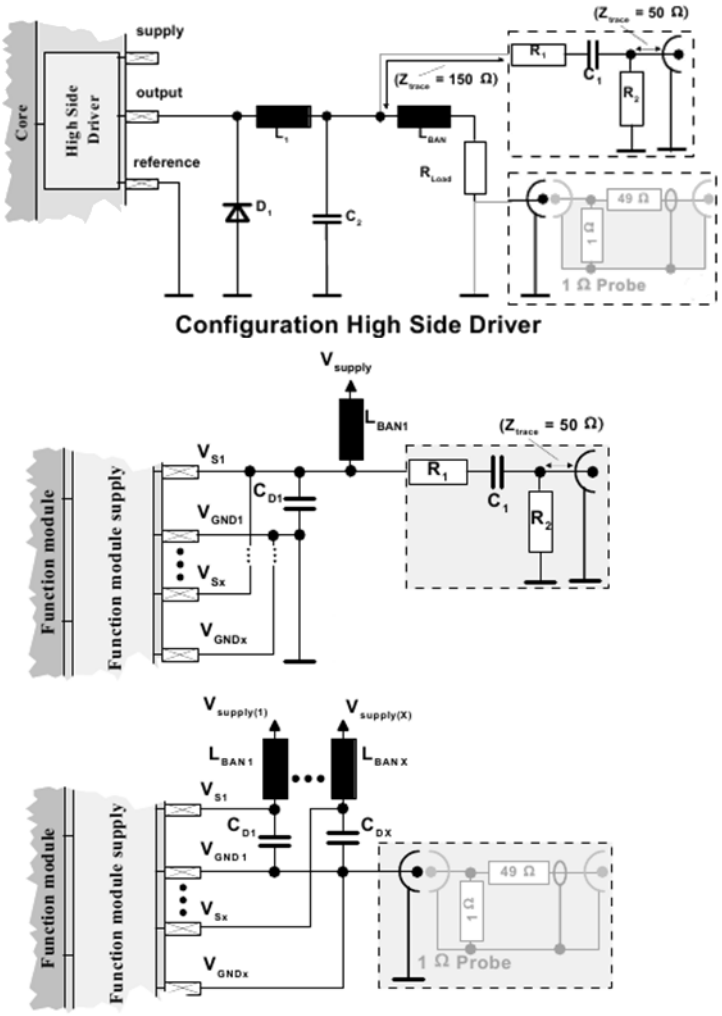
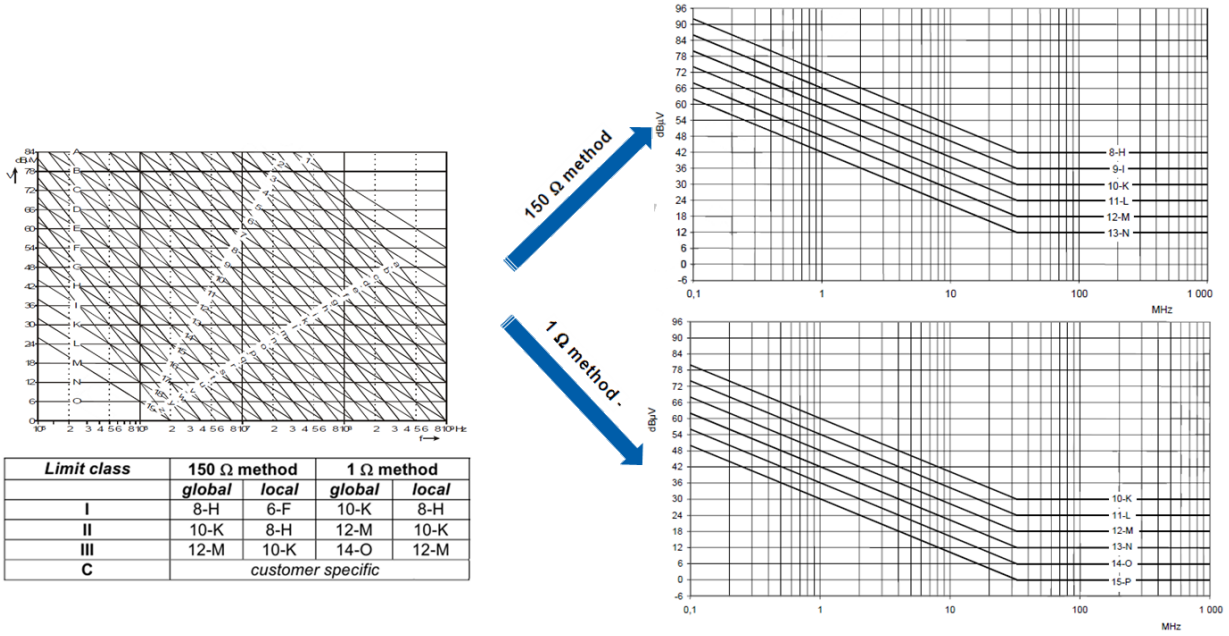


Figure D.10: In addition to IEC61967-4, at 150Ω networks a $5\mu H$ coil for impedance fixing is added.

The scheme follows the theory of a periodical trapezoidal pulse response and offers three different slopes of emission amplitudes with a 6 dB distance:

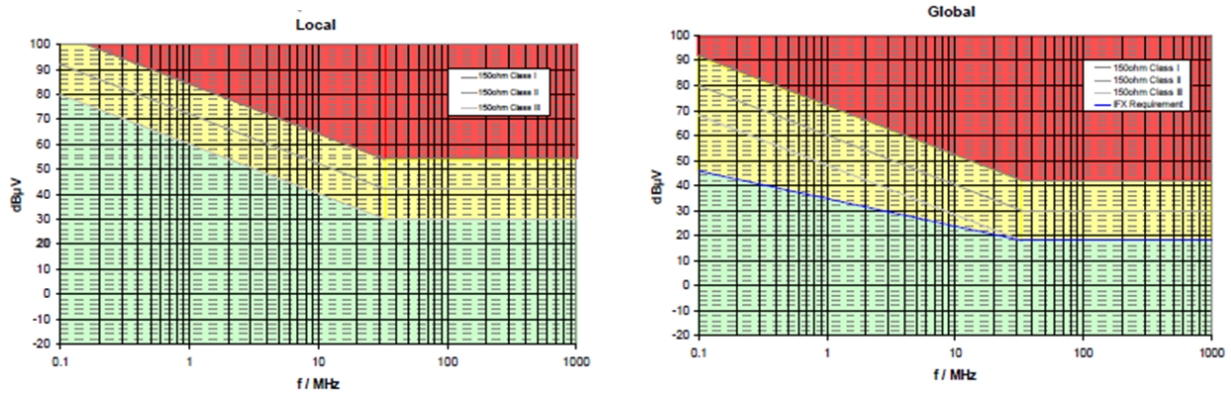
- 0 dB/decade (theory: constant amplitude line till the first corner frequency $\frac{1}{\pi\tau}$)
- -20 dB/decade (theory: decrease of amplitude till second corner frequency $\frac{1}{\pi\tau_r}$)
- -40 dB/decade (theory: decrease of amplitude at frequencies $> \frac{1}{\pi\tau_r}$)

The corner frequencies are dependent on the rise/fall times τ_r and the duration τ of the pulse. The emission level diagram shown in Figure D.11 enables the selection of different slopes for different frequencies to better describe the measured conducted EME.



Limit class	150 Ω method		1 Ω method	
	global	*local*	*global*	*local*
I	8-H	6-F	10-K	8-H
II	10-K	8-H	12-M	10-K
III	12-M	10-K	14-O	12-M
C	*customer specific*			

Figure D.11: Emission level scheme. Reference levels for conducted disturbances from semiconductors (peak detector)



(a) (b)

Figure D.12: IEC 61967-4 emissions level scheme for the classification of the conducted emissions for local (a) and global (b) pins.

The description of the maximum emission level can consist of up to three digits. Each digit represents one of three available slope identifiers as described above and shown in Figure D.11. Capital letters are used to indicate a 0 dB/decade slope. Numbers are used to indicate a -20 dB/decade slope. Small letters are used to indicate a -40 dB/decade slope. Assuming that one

of the three slopes is not needed, then the corresponding letter or number will be left off. The defined maximum emission level in Figure D.11 offers a standardised way to communicate maximum emission levels unambiguously.

In general, the first digit is a capital letter that represents the maximum amplitude of the measured data. The second digit can either be a number or small letter that defines the position of the -20 dB/decade slope or -40 dB/decade slope, respectively. The third digit can be a capital letter, small letter or number. In the case of measured emissions that approximate those resulting from a trapezoidal waveform, the capital letter is first and represents the position of the horizontal line with 0 dB/decade slope. Second is the number which defines the slope of -20 dB/decade. The third and small letter defines the position of the -40 dB/decade slope. The points of intersection of the slopes represent the first and second corner frequencies as described above.

Based on the experience of the automotive industry, semiconductor emission measurements cannot completely characterise the disturbance capability of electronic vehicle components in which they are applied. The reason for this is seen in various effects in the vehicle and vehicle components (e.g. grounding, resonance, attenuation and coupling), which may also contribute to the emission behaviour or change the emission behaviour. Therefore, semiconductor emission measurements cannot fully replace vehicle and component measurements according to CISPR 25.

Figure D.12 shows the emissions level scheme for the classification of the conducted emissions for global and local pins. The green area defines an IC emissions range where usually no emissions issues occur on application level. The upper value in the emissions level scheme for global pins (i.e. the IFX Requirement) represents the internal design target. The yellow area defines a range where additional simple external filtering/decoupling components usually improve the emissions level back to the green range. In the unlikely event that the emissions level is within the yellow range although external components are used, please align with the EMC and AE colleagues on the further proceeding. The red area outlines a severe and non acceptable emissions level of the DUT with and without additional external components.

Appendix E

Real behaviour of discrete component

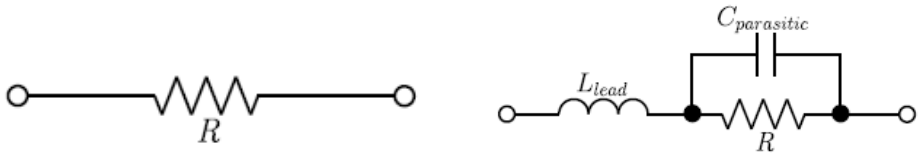
A passive component can no longer be regarded as a perfect resistor, inductor or capacitor, as the frequency contents of the signal or current/voltage increases. For example a resistor begin to behave more and more like an inductor. As the frequency is increased, or decreased depending on the reference point, all parts of the circuit begins to suffer from a behavioral change. The PCB itself could start act as a very effective antenna at a certain operating frequency. If accurate, or at least more realistic, emission results are expected from simulations it is not enough to use conventional component models available in circuit simulation packages such as Cadence. These models needs a refinement in the aspect of details and behavior as they often exhibit a behavior that is not adapted to high power applications such as those found in an SMPS.

E.1 Resistor

If a resistor's behaviour at higher frequencies needs to be accounted for, a more detailed model than the ideal one has to be used, see Figure E.1(a). One way to model the resistor in a better way is depicted in Figure E.1(b). The frequency response of the impedance for both models can be seen in Figure E.2, the phase characteristics also changes with frequency, although not presented here. Resistors can be constructed in different ways; the most common types of resistors are carbon composition, wire wound and thin film where each type has its benefits and drawbacks [27].

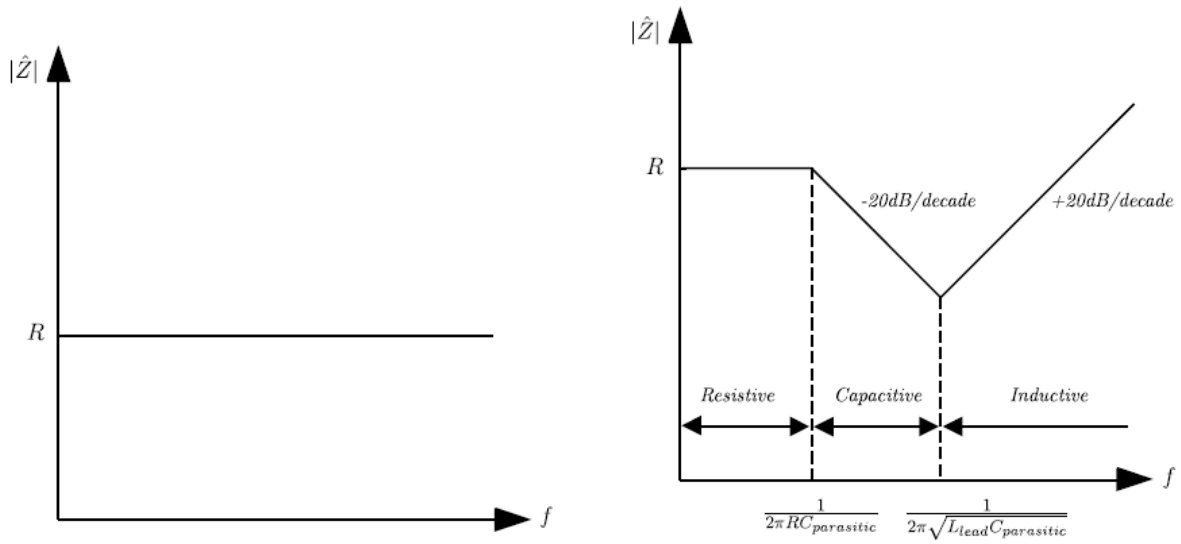
E.2 Capacitor

A common way of modeling capacitors at higher frequencies is depicted in Figure E.3(b) with the corresponding frequency response seen in Figure E.4(b). Just as for the resistor, there are many



(a) (b)

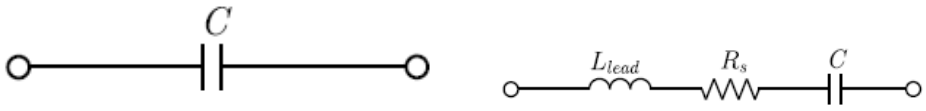
Figure E.1: Ideal resistor model (a) and a nonideal resistor model with parasitic capacitance and lead inductance (b).



(a) (b)

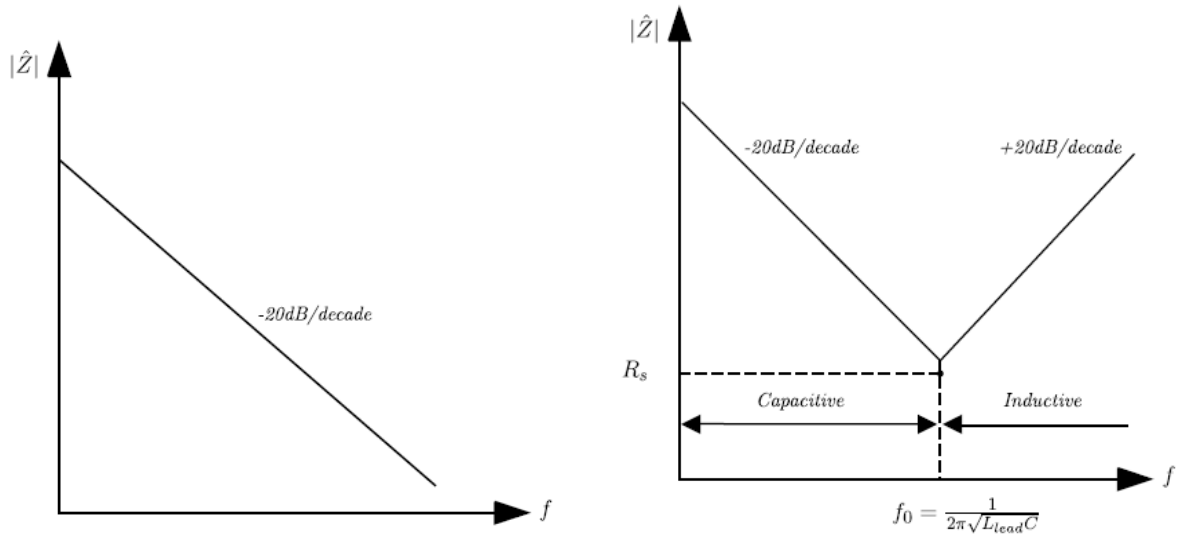
Figure E.2: The frequency dependence of the impedance for the two resistor models, ideal (a), nonideal (b).

different types of capacitors depending on production techniques, thus are some types more suitable for certain types of applications [27].



(a) (b)

Figure E.3: Ideal capacitor model (a) and a model of the nonideal capacitor model with equivalent series resistance, or ESR, and lead inductance (b).

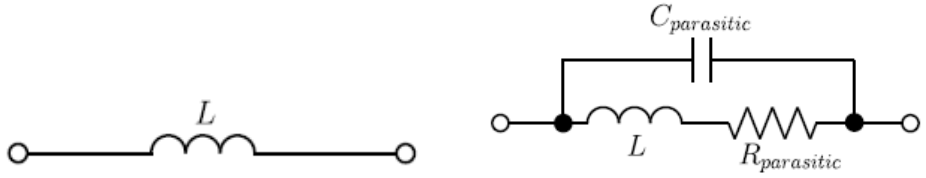


(a) (b)

Figure E.4: The frequency dependence of the impedance for the two capacitor models, ideal (a), nonideal (b).

E.3 Inductor

A common way of modeling inductors at higher frequencies is depicted in Figure E.5(b) with the corresponding frequency response seen in Figure E.6(b) [27].

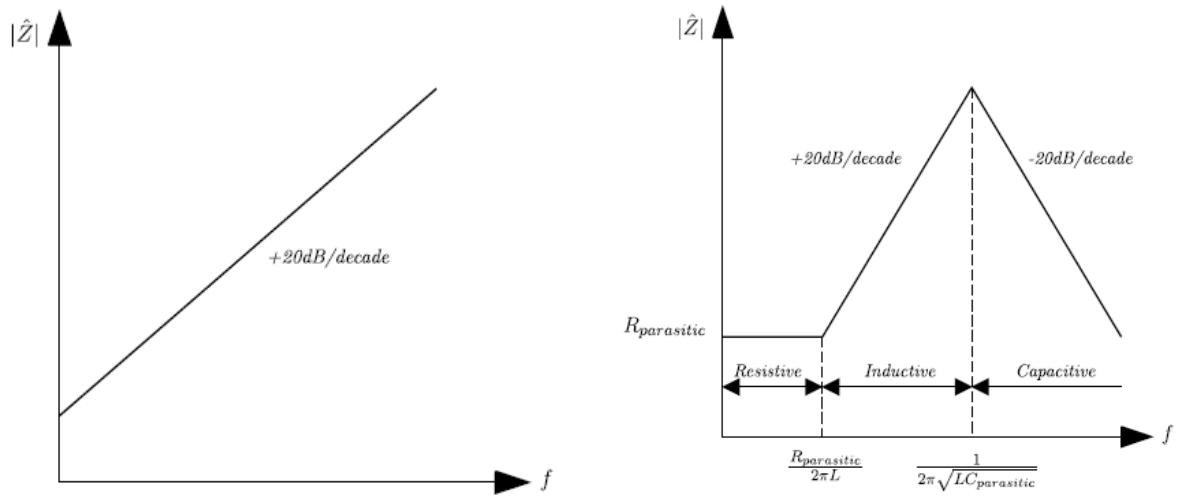


(a) (b)

Figure E.5: Ideal inductor model (a) and a model of the nonideal inductor model with parasitic resistance and lead elements (b).

E.4 PCB strip inductance

Interconnections between components on a PCB are all of different shapes and length which means that each segment has to be considered to be a unique component. A relatively accurate



(a) (b)

Figure E.6: The frequency dependence of the impedance for the two inductor models, ideal (a), nonideal (b).

inductance model of the strip can be expressed as:

$$L = 0.0002 \cdot b \cdot \left[\ln\left(\frac{2b}{w+h}\right) + 0.5 + 0.2235\left(\frac{w+h}{b}\right)\right] \tag{E.1}$$

where L = inductance in $[\mu H]$, b = length in $[mm]$, w = width in $[mm]$ and h = thickness in $[mm]$ [27].

E.5 Wires and leads

All wires and leads present on the PCB are assumed to have a circular cross section, this is of course a simplification, and thus the following equation presents the model of the inductance [27].

$$L = 0.0002 \cdot l \cdot \left[\ln\left(\frac{2l}{r}\right) - 0.75\right] \tag{E.2}$$

In the case that there are a pair of parallel conductors the mutual inductance can be found from:

$$M = 0.0002 \cdot l \cdot \left[\ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right] \tag{E.3}$$

where M = mutual inductance in $[\mu H]$, l = wire length in $[mm]$, D = distance apart in $[mm]$, for $\frac{D}{l} \ll 1$.

Appendix F

Spread Spectrum Modulation

Instead of maintaining a constant frequency, SSCG systems modulate the clock frequency following certain modulation profiles, thereby spreading the harmonic energy into an amount of side-band harmonics having the same energy but smaller amplitude, which normally corresponds to spreading conducted emissions over a wider frequency range. At any frequency, the detected emissions are lower. SSCG held the promise of EMI suppression by way of a clock replacement.

F.1 State of Art

It was only in the past decade when this new technique appeared. The history of SSCG is quite interesting. The concept of frequency hopping was first introduced by Nicola Tesla in 1903 (Figure F.1).

It is normally accepted that the parents of these modulation techniques are George Antheil and the actress Hedy Lamarr (Figure F.2). With the help of an electrical engineering professor from the California Institute of Technology they worked in order to become the idea in a patent, which was finally granted on August 11th, 1942. The patent disclosed a method of frequency hopping used to immunize radio-controlled torpedoes against jamming. In the last two decades, the technique has become a mainstay of the communications revolutions because of its advantages in range, immunity and security.

The first published work on the use of SSCG applied in power converters was a paper presented at the Virginia Power Electronics Center, Tenth Annual Power Electronics Seminar in 1992. The intention of the author was to present how a modulation of the initially constant switching frequency controlling a switching power supply contributed to a significant reduction of EMI emissions. In this paper, author Lin presents a forward converter circuit and the related PWM controller. With

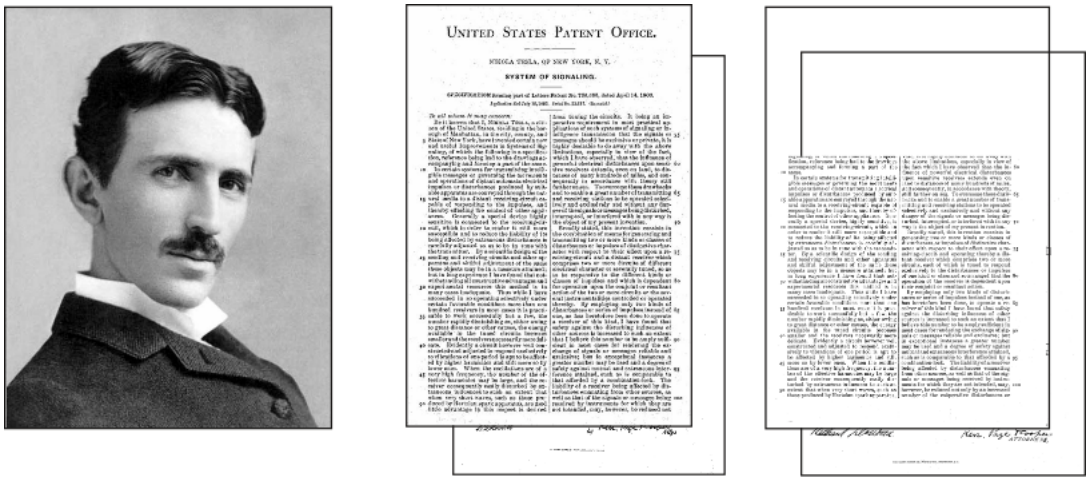


Figure F.1: Nicola Tesla and the US patents (*System of Signaling* and *Method of Signaling*) about the introduction of frequency hopping

Figure F.2: Hedy Lamarr and George Antheil and their US patent

an ingenious modification of the frequency control of this controller in order to inject not a constant but a variable frequency, it generates a variable-frequency PWM, not affecting the duty cycle of this PWM. The experimental verification was tested at a power supply's nominal switching frequency of 90 kHz by following a sinusoidal modulation profile generating a frequency peak deviation lower than 10 kHz and an adjustable modulating frequency. Anyway, some results are also shown at frequency peak deviation of 15 kHz and modulating frequency of 400 Hz showing a substantial reduction in emissions. At the 1994 IEEE International Symposium on EMC, authors K. B. Hardin, J. T. Fessler

and D. R. Bush, from Lexmark International (IBM's Office Products Division) [15], presented the results of their work, about the application of SSCG techniques to the higher frequencies world of CPU clocks in digital devices. The wide modulation frequency proposed by Lin was impractical for use as a clock generator. The authors proposed to vary the frequency of the clock only slightly, thus resulting in a variation of only 0.625% instead of the 16.67% used by Lin. It must be kept in mind that SSCG applied to power converters and CPU clocks have different exigencies. Anyway, this technique resulted in a measured attenuation of the third harmonic, of only 2 dB. However, as the harmonic number increased so did the attenuation. At the 20th harmonic, the measured attenuation was 10 dB.

Early on, it was observed that the sinusoidal waveform used by Lin to frequency modulate the clock in his power supply did not produce optimal EMI suppression. As shown in Figure F.3, modulation of a sinusoidal carrier by following a sinusoidal modulating profile (Figure F.3(a)) generates a spectrum which tends to concentrate side-band harmonics around the two frequencies defining the bandwidth generated during the frequency modulation process, that is, a spectrum peaked at its extremities (Figure F.3(b)). The reason for this effect has to do with the rate of change, or derivative, of the sine wave. Its rate of change slows as the sine wave reaches its peak values. That happens at the ends of the spectra in Figure F.3(b) and it is there that the oscillator "hangs out" a little longer than it does elsewhere. Better results were achieved when a triangular wave (Figure F.3(c)) was used to modulate the clock. But the engineers at Lexmark found that an optimal waveform was that shown in Figure F.3(e) which produced a nearly flat spectra across the deviated range. The waveform of Figure F.3(e) has become known as the "Lexmark Shape". Lexmark filed for, and received a patent on optimal waveforms for use in producing a spread spectrum clock generator.

Anyway, some points in [15] are to be reconsidered in order to clarify some dark aspects in this paper mainly related to the shape of the generated spectrum after modulation depending on the modulation profile. It is known this paper was greeted with a mixture of accolades and unusually harsh criticism but no one questioned the effect was real. Emissions detected by an EMI receiver used in accordance with CISPR Publications 16 and 22 would be significantly less at the higher harmonics when SSCG was used in place of a traditional clock. However, some engineers claimed that the technique did not really reduce emissions, but simply "fooled" the quasi-peak detector in the EMI receiver. That criticism, however, was unfair. A narrow-band look at the spectra produced

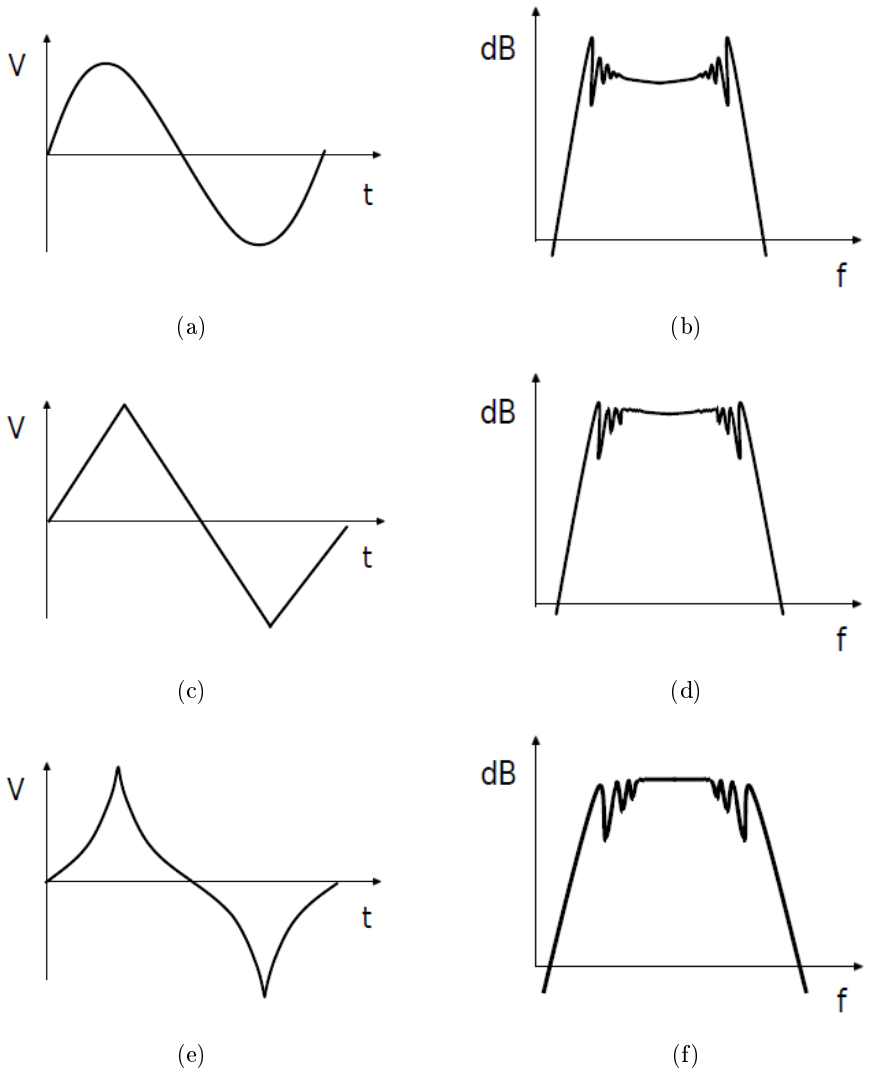


Figure F.3: Different modulation profiles (sinusoidal (a), triangular (c), hershey kiss (e)) produce different frequency spreading effects (b), (d), (f)

by a SSCG will reveal individual harmonics at the modulating clock frequency: each one of the harmonics is stationary and, therefore, will measure the same whether measured on a peak, average or a quasi peak detector. Others argued that spreading the energy does not reduce it, and that receivers which were sensitive to the total energy emitted by a digital device would not see any improvement in their immunity due to the use of spread spectrum clock generators. Also, receivers using bandwidths wider than 120 kHz, such as TV receivers, could be adversely affected. The FCC rules intended to protect a wide variety of devices but fixing a 120 kHz measuring bandwidth

might be an inappropriate way to measure the interference potential of devices employing this new technology. The current FCC rules, and the voluntary standards upon which they are based, specify receiver bandwidths and detectors that were developed decades ago. Anyway, the FCC, which has already reviewed this issue once, does not see an interference threat from SSCGs as currently implemented. In addition, Hardin, Fessler and Bush reported on a detailed Philips Consumer Electronics study on the effects of the use of spread spectrum clock generation in place of fixed frequency clock on television reception [16]. They concluded that most televisions are, more or less, indifferent to the interference caused by either a narrow band or a spread spectrum generated clock, both set to the FCC Class B limits and centered on the same frequency. To avoid interference, the authors did point out that the modulation frequency used should be greater than 20 kHz in order to be beyond the audible range of the human ear. Use of a modulating frequency above 20 kHz helps to ensure that any signals working their way through to the audio system are at frequencies high enough to be filtered out by the receiver, speaker or to be undetectable by the human ear. No timing considerations have been made until now. Certain applications simply cannot tolerate a wandering clock. Video displays, for example, may shiver noticeably unless the horizontal sweep is synchronized with the SSCG. Many forms of communications require a synchronous clock in line with tight specifications. The technique shouldn't be used for timing on Ethernet, Fiber Channel, or ADSL applications. Unless the clock is highly stable, these applications can suffer from poor locking, failure to lock or data errors.

F.2 Modulation

Modulation is the process by which some characteristics of a carrier waveform are modified by another signal in order to obtain some benefits. This process of modulation is widely used in telecommunications where the information of a signal is transferred to the carrier before transmission. The characteristics of the carrier being modulated are normally amplitude and/or angle. In its simplest way, a modulator can vary such characteristics of the carrier proportionally to the modulating waveform: this is called analogical modulation. More complicated modulators make first a conversion to digital and codify the modulating signal before modulation; this is known as a digital modulation. In order to understand the process of modulation, it is a good procedure to present a modulator as a black box with two inputs and one output (Figure F.4).

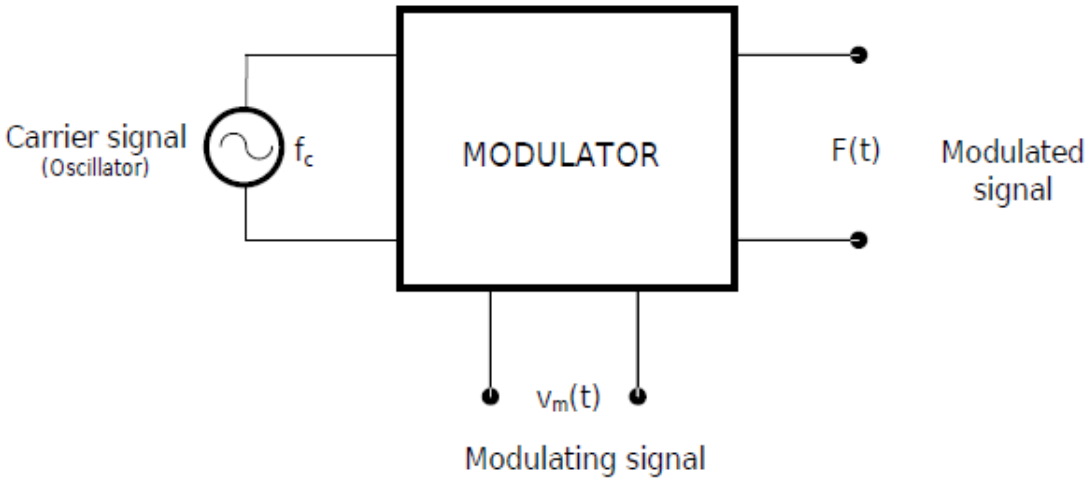


Figure F.4: Black box modelling a modulator

Three signals are taking part in a modulation process:

- Carrier signal: periodic waveform of constant frequency (f_c) and constant amplitude profile.
- Modulating signal $v_m(t)$: waveform responsible for changing (modulating) the initially constant characteristics of the carrier signal.
- Modulated signal $F(t)$: waveform resulting from the modulation process.

The output of the modulation process can be expressed as follows:

$$F(t) = A(t) \cdot \cos[\omega_c \cdot t + \Theta(t)] = A(t) \cdot cos[\phi(t)] \tag{F.1}$$

where:

- $A(t)$ is a time-dependent amplitude
- $f_c(\omega_c = 2\pi f_c)$ is the carrier frequency
- $\Theta(t)$ is a time-dependent phase angle
- $\phi(t)$ is the angle of the modulated signal

The modulating signal $v_m(t)$ controls either the amplitude $A(t)$ or the angle $\phi(t)$ or both together. There are normally two techniques of modulation:

- Amplitude modulation (AM): the carrier envelope $A(t)$ is changed according to the modulating signal $v_m(t)$ while $\Theta(t)$ stays constant.
- Angle modulation: $A(t)$ is a constant value A but the angle $\phi(t)$ is controlled by the modulating signal $v_m(t)$. This angle modulation has two variants depending on the close relationship between the angle $\phi(t)$ and the modulating signal:
  - Phase modulation (PM)
  - Frequency modulation (FM)

Because frequency modulation is the base of this thesis, a more detailed explanation of it is required.

F.3 Frequency Modulation (FM)

F.3.1 Generic Formulation of Frequency Modulation

In frequency modulation, the deviation $\delta\omega(t)$ of instantaneous frequency $\omega(t)$ respect to the constant carrier frequency ω_c is directly proportional to the instantaneous amplitude of the modulating signal voltage $v_m(t)$ as shown in Figure F.5. The instantaneous frequency of the resulting modulated waveform can be expressed as follows:

$$\omega(t) = \frac{d\phi}{dt} = \omega_c + \frac{d\Theta(t)}{dt} = \omega_c + \delta\omega(t) \text{ , where } , \delta\omega(t) = \frac{d\Theta(t)}{dt} = \omega(t) - \omega_c \tag{F.2}$$

In frequency modulation, deviation $\delta\omega(t)$ is supposed to be proportional to the modulating signal voltage $v_m(t)$, that is:

$$\delta\omega(t) = k_\omega \cdot v_m(t) \tag{F.3}$$

where k_ω is a sensitivity factor of the modulator expressed in rad/sec/V or Hz/V. From (F.2) and (F.3), the following expression arises:

$$\Theta(t) = \int_0^t k_\omega \cdot v_m(t) \cdot dt + \Theta(0) \tag{F.4}$$

where $\Theta(0)$ is the initial value of phase and it is commonly taken as zero.

From (F.1) and (F.4), the generic expression of a frequency modulated sinusoidal waveform $F(t)$ takes this aspect:

$$F(t) = A \cdot \cos[\omega_c \cdot t + k_\omega \cdot \int_0^t v_m(t) \cdot dt] \tag{F.5}$$

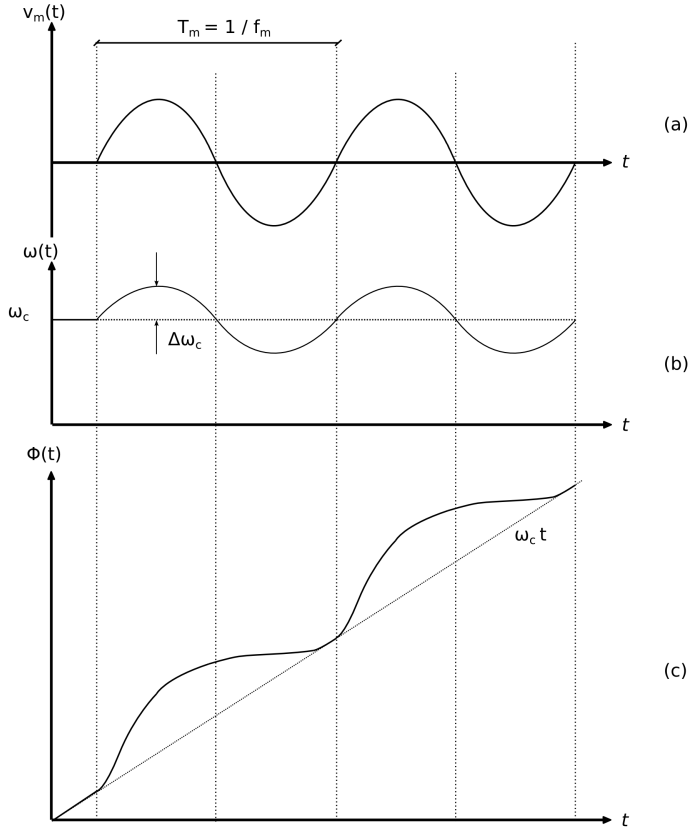


Figure F.5: Effect of sinusoidal frequency modulation. (a) modulating wave; (b) instantaneous frequency of the FM waveform; (c) instantaneous angle of the FM waveform.

A very important ratio in frequency modulation is known as modulation index m_f and is expressed this way:

$$m_f = \frac{\Delta\omega_c}{\omega_m} = \frac{\Delta f_c}{f_m} \tag{F.6}$$

where (according to Figure F.5 (b)):

- Δf_c is the peak deviation of the carrier frequency.
- f_m is the frequency of the modulating signal $v_m(t)$, assuming it is a periodic waveform.

The modulation ratio δ denotes the peak excursion of the switching or carrier frequency referred to itself, that is:

$$\delta = \frac{\Delta f_c}{f_c} \ , \ \delta_{\%} = \frac{\Delta f_c}{f_c} \cdot 100 \tag{F.7}$$

This percentage of modulation normally ranges between 1% and 2.5% for the commercial applications like PC boards at higher frequencies (in order to conserve the minimum-period requirements for control system timing). In the case of switching power converters, where timing requirements are much less important, this percentage can be larger, much more than 2.5%.

Bandwidth is defined as the difference between the limiting frequencies within which performance of a device, in respect to some characteristic, falls within specified limits or the difference between the limiting frequencies of a continuous frequency band. An FM signal actually contains an infinite number of side frequencies besides the carrier and therefore occupies infinite bandwidth. However, the side frequencies quickly decrease in strength and can be considered negligible at some point. In practice, a tradeoff between bandwidth and distortion must be considered. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule (valid for any angle-modulated signal) and can be summarized as follows:

- Total energy of the original signal keeps unaffected
- The 98% of the total energy is contained inside a bandwidth B calculated as follows:

$$B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m) \tag{F.8}$$

F.4 Modulation profiles

The most important parameter defining the shape of the resulting modulated wave spectrum is strongly related to the modulation profile, that is, the shape of the waveform used to modulate but these profiles also influence the displacement of the central frequency up- or down-wards respect to the original signal, as shown in Figure F.6. Instead of shifting the carrier frequency above and below symmetrically, the frequency is only shifted up or downwards respect to the carrier.

Where setup and hold time margins are critical, down spreading technique is preferred. In practice, there are three profiles used for modulation purposes: sinusoidal, triangular and exponential. As seen later on, exponential profile is very easy to be parameterized then giving different aspects ranging from nearly-peaks to nearly-square waveforms. Each modulation profile shows different advantages depending on the system characteristics where it is to be implemented and, at this stage, it is not right to say that a profile is much better than the others.

A line of investigation in this area points necessarily to study how a profile should be in order to obtain the maximum benefits when using SSCG and it will be developed later on.

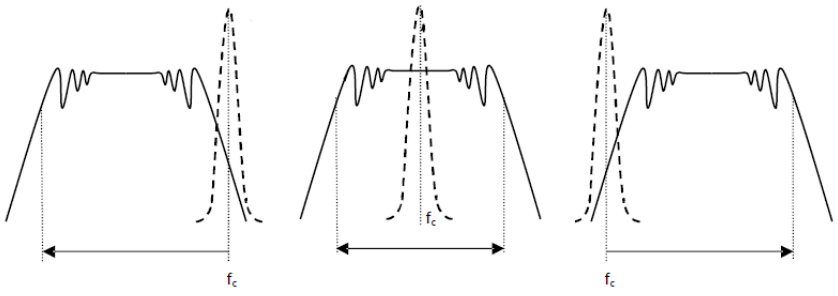


Figure F.6: a) Down-spreading, b) symmetrical or center-spreading, and c) up-spreading SSCG techniques

F.4.1 Sinusoidal carrier vs. a generic carrier: validity of modulation results

Until this point, all considerations and developments have taken into account the fact of modulating a sinusoidal carrier. Most of the carriers (even those intended to be sinusoidal) are not a pure sine wave but a set of harmonics. In switching power converters, a PWM signal is to be found; communication standards define normally trapezoidal waveforms in order to reduce the high-frequency spectral components. The question now is how to deal with these generic waveforms consisting of infinity of harmonics.

Impact of modulation on every spectral component

The distance in frequency between two consecutives harmonics is given by the frequency f_c of the original signal (supposing to be periodic). The frequency f_h of the harmonic F_h is expressed this way:

$$f_h = h \cdot f_c \tag{F.9}$$

where h is the harmonic order varying from 0 to ∞. Each harmonic component is represented as a pair amplitude-phase $(A_h - \Theta_h)$ at a frequency position f_h. If the same frequency modulation is applied to each harmonic component, expressions (F.1), (F.2) and (F.3) can be generalized as the generic expression of a frequency modulated harmonic component, that is:

$$\begin{aligned} F_h^{mod}(t) &= A_h(t) \cdot \cos\big[\phi_h(t)\big] = A_h(t) \cdot \cos\big[h \cdot \omega_c \cdot t + \Theta_h(t)\big] \\ &= A_h(t) \cdot \cos\left[h \cdot \omega_c \cdot t + \theta_h + k_\omega^h \cdot \int_0^t v_m(t) \cdot dt\right] \end{aligned} \tag{F.10}$$

where:

$$\Theta_h(t) = \theta_h + k_\omega^h \cdot \int_0^t v_m(t) \cdot dt \tag{F.11}$$

$$\begin{aligned} \delta\omega_h(t) &= \omega_h(t) - h \cdot \omega_c = \frac{d\Theta_h(t)}{dt} \\ &= k_\omega^h \cdot v_m(t) = h \cdot k_\omega \cdot v_m(t) \end{aligned} \tag{F.12}$$

where k_ω^h was defined for similarity with expression (F.3).

Some conclusions can be obtained from the expressions above:

- From (F.11) and (F.12), the particular harmonic phase θ_h does not affect the results of frequency modulation because of the derivative behaviour of the frequency deviation as expressed in (F.10).

- From (F.9), the peak frequency deviation affecting each harmonic component increases linearly with the harmonic order, that is, $\Delta f_h = h \cdot \Delta f_c$. In other words, the modulation index related to each harmonic component m_f^h will also increase linearly with the harmonic order:

$$m_f^h = \frac{\Delta f_h}{f_m} = h \cdot \frac{\Delta f_c}{f_m} = h \cdot m_f \tag{F.13}$$

- The bandwidth B_h of the frequency modulated harmonic component h increases also linearly with the harmonic order:

$$B_h = 2 \cdot f_m \cdot \left(1 + m_f^h\right) = 2 \cdot (\Delta f_h + f_m) \tag{F.14}$$

$$B_h = B_1 + 2 \cdot \Delta f_c \cdot (h - 1) \tag{F.15}$$

  where B_1 is the bandwidth corresponding to modulation of a sinusoidal waveform of frequency f_c, equivalent to the 1^{st} harmonic of the generic waveform.

F.5 Practical considerations related to FM parameters

It is important to distinguish between a phenomenon itself and the way it is measured. Although theoretical results show a good performance of frequency modulation regarding to EMI

emissions reduction in every case, measurements procedures (normally related to practical limitations of measure equipment or normative aspects) can fade such a good behaviour even making it negligible. In other words, a good theoretical SSCG system is not a guarantee of a good experimental result when measuring; it should be only taken as a start point which, after some modifications, could work properly. Onwards, some practical considerations related to each FM parameter together with its theoretical implication are to be exposed.

F.5.1 Carrier (Switching) & modulating frequencies

As exposed previously, the carrier (switching) signal is the constant frequency f_c wave to be modulated, while the modulating signal (normally a constant frequency f_m wave) is the waveform used to do the modulation. Fourier series is a common way to express any waveform:

$$F(t) = F_0 + \sum_{h=1}^{+\infty} F_h(t) \tag{F.16}$$

where F_0 represents the average DC component of the original signal and F_h, each one of the infinity of harmonics.

When talking about modulation of a base frequency, a common way to operate is modulating each individual component F_h of the base waveform (main harmonics) and, then, obtaining a window of sub-harmonics (side-band harmonics) for each main harmonic (see Figure F.7).

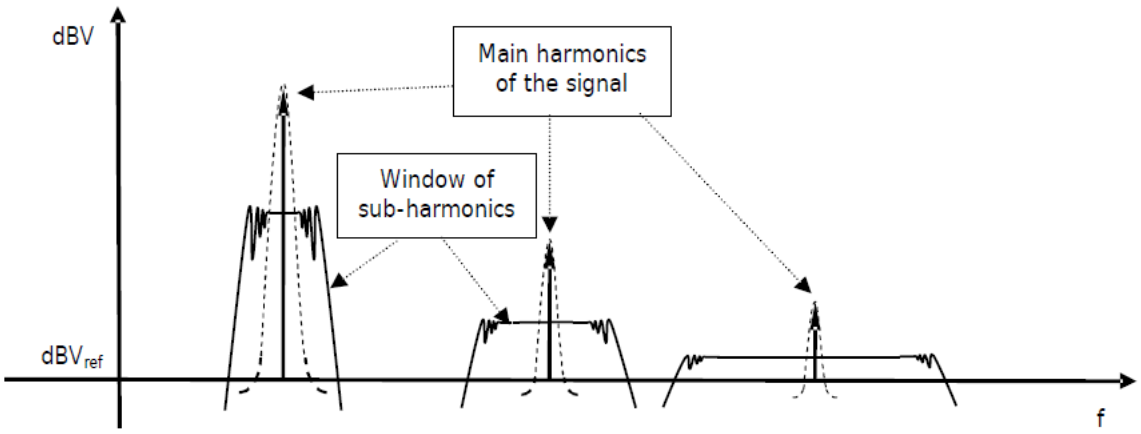


Figure F.7: Only one modulating signal modulates every harmonic of the original signal.

As expressed in (F.8), the bandwidth of the side-band harmonics increases linearly with

the carrier frequency f_c, the modulation ratio δ and the modulating frequency f_m. For periodic frequency modulation, the distance between two consecutive side-band harmonics is given by the modulating frequency f_m (see Figure F.8).

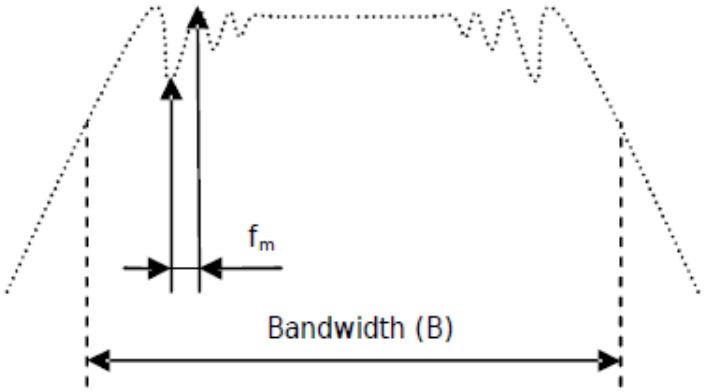


Figure F.8: Distance between two consecutive side-band harmonics (FM modulation)

Common values for the modulating frequency f_m range from 30 kHz to 250 kHz , in order to be above the audio band, (for system clocks). Instead, for power converters, it is advisable to use smaller modulating frequencies down to 9 kHz. In the same way, CISPR 16-1 specifies several RBWs (6 dB) for the different frequency ranges and measurement modes. This way, a RBW of 220 Hz is intended for measurements in the band A (9 kHz-150 kHz); 9 kHz for the band B (150 kHz-30MHz); 120 kHz for the bands C (30 MHz-300 MHz) and D (300 MHz-1GHz) and 1 MHz for frequencies higher than 1 GHz (valid for quasi-peak, peak and average measurement mode). The spectrum analyzer band-pass filter (commonly known as Resolution Bandwidth-RBW) is adjustable, for instance, to accomplish the value defined in a regulatory norm. Two main cases are of significance:

- $f_m < RBW$: It is not possible to distinguish individual side-band harmonics, so the measured value will be higher than expected in theoretical calculations but it can still be worthy if $RBW < B$ (see Figure F.8).
- $f_m > RBW$: Considering no overlap exists, the measured value corresponds to the actual individual side-band harmonic amplitude.

For the second case ($f_m > RBW$) to be reached for the different frequency ranges expressed above,

special care must be taken when selecting the modulating frequency. As the sum of the several side-band harmonics inside this RBW is done by just adding amplitudes (this represents the way a spectrum analyzer actually adds signals in its bandwidth), it is expected to obtain (for the first case) a value higher than the actual one. The larger RBW, the larger the measured value for each side-band harmonic too.

F.5.2 Influence of the frequency peak deviation Δf_c

Carrier frequency peak deviation Δf_c denotes the peak excursion of the switching frequency f_c and it is normally expressed as $\Delta f_c = \delta \cdot f_c$, where the factor δ is the modulation ratio. The resulting window bandwidth B (already presented in expression (F.8)) depends on the modulation ratio δ and it is desired that the side-band frequencies do not fall into the audible range. It is important to remind that the bandwidth resulting from modulation process is wider than two times the carrier frequency peak deviation, the first one given by the Carson's rule.

One important influence of the modulation profile is related to the maximum peak excursion of the switching frequency Δf_c respect to the initially constant carrier frequency. As a general asseveration, a power converter consists of a low-pass filter whose function is to filter out the whole AC components coming after the switch, thus allowing only the DC component to flow across the load resistor. For a step-down power converter, a LC filter is implemented. The cut-off frequency of this filter establishes approximately the minimum high-frequency being rejected. For a constant switching frequency, no problem is normally found and only the DC component flows across the load resistor but, during the frequency modulation process, switching frequency can fall beyond the cut-off frequency, then transmitting this low frequency immediately to the load resistor, making the output voltage V_o oscillate, which is unacceptable.

For a step-down power converter, the gain is:

$$\frac{\overrightarrow{V_o}}{\overrightarrow{V_i}} = \frac{1}{1 - \omega^2 \cdot LC + \omega \cdot \dfrac{L}{R}} \tag{F.17}$$

$$\frac{V_o}{V_i} = \frac{1}{\sqrt{\left(1 - \omega^2 \cdot LC\right)^2 + \left(\omega \cdot \dfrac{L}{R}\right)^2}} \tag{F.18}$$

The damping rate of the ideal LC filter is 40 dB and the cut-off frequency becomes:

$$f_{\text{cut-off}} = \frac{1}{2\pi \cdot LC} \tag{F.19}$$

Frequencies higher than the cut-off frequency are completely filtered out while those frequencies lower go across the system with no attenuation. And this is really the problem. If a modulation system itself is able to generate switching frequencies lower than the cut-off frequency, oscillations are to appear at the output voltage. Frequencies inside the side-band harmonics bandwidth resulting from the modulation process must be filtered out by the low-pass filter. Normally, this bandwidth (given by the Carson's rule) is approximated to $2 \cdot \Delta f_c$ around the carrier (switching) frequency f_c and the minimum frequency present is given by $f_c - \Delta f_c$. Therefore, inferior limit of the peak switching frequency deviation (respect to the central frequency) is given by the cut-off frequency of the LC filter, that is, $f_c - \Delta f_c > f_{\text{cut-off}}$, what must be taken into account when selecting a certain modulation profile and its related parameters.

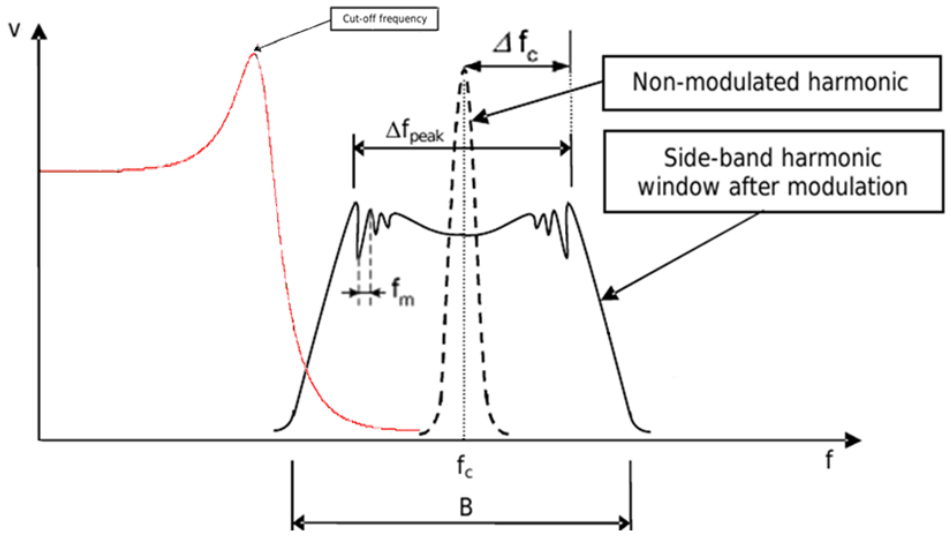


Figure F.9: Bode diagram of a LC filter. Frequencies higher than the cut-off frequency are filtered out while those frequencies lower go across the system with no attenuation.

Another inferior limit of the peak switching frequency deviation (respect to the central frequency) is given by the higher limit of the human audible frequencies $f_{aud_{max}}$ in order to avoid undesirable audio interferences. Note that switching frequencies of power converters are usually low ($f_c < 1MHz$) and special care must be taken to avoid harmonics into the audible band ($f_{aud_{min}} = 20Hz < f_{aud} < f_{aud_{max}} = 20kHz$).

However, the main influence of the parameter Δf_c is related to the possibility of overlap between the side-band harmonics of two consecutive main harmonics. Overlap can be an important

aspect at higher harmonic components because benefits are only obtained only when the sum of side-band harmonics belonging to several main harmonic windows is lower than the related-carrier harmonic.

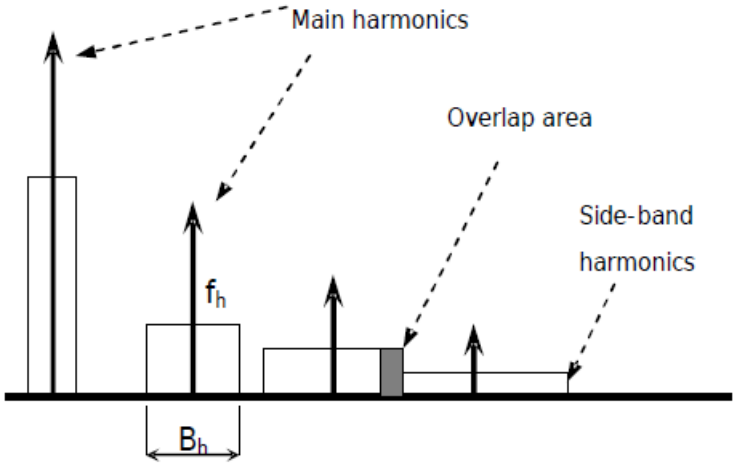


Figure F.10: Side-band windows overlap

Of course, the side-band harmonic window is not a perfect square box as shown in Figure F.10. Moreover, the spectra resulting from a modulating process contains infinity of harmonics which extends over the whole frequency axis. But the Carson's rule establishes that a 98% of the total energy of the modulated signal is contained inside a bandwidth given by the expression (F.14). No information related to the shape of the side-band harmonic window is given by the Carson's rule because this one only depends on the shape of the modulation profile. The square approximation of the window is valid for the purpose of finding the harmonic order at which the overlap effect is starting to appear. Approximately, overlap effect occurs when (see Figure F.10):

$$f_h - \frac{B_h}{2} \leq f_{h-1} + \frac{B_{h-1}}{2} \tag{F.20}$$

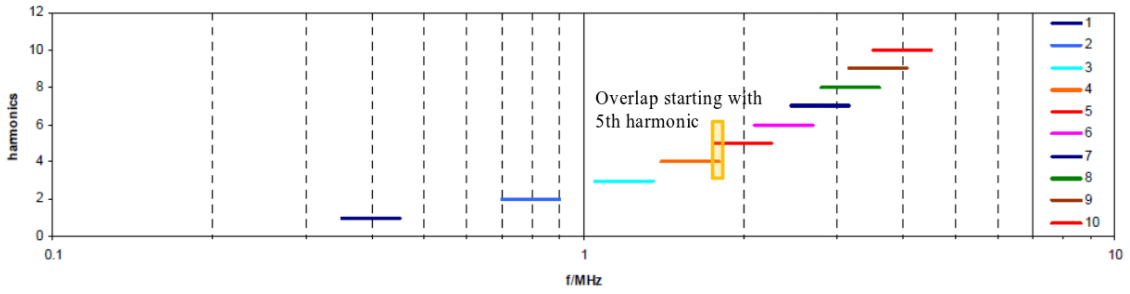
Substituting (F.14) and (F.9) into (F.20), the following expression is derived:

$$f_c \leq \frac{2}{1 + \delta \cdot (1 - 2 \cdot h_{overlap})} \cdot f_m \tag{F.21}$$

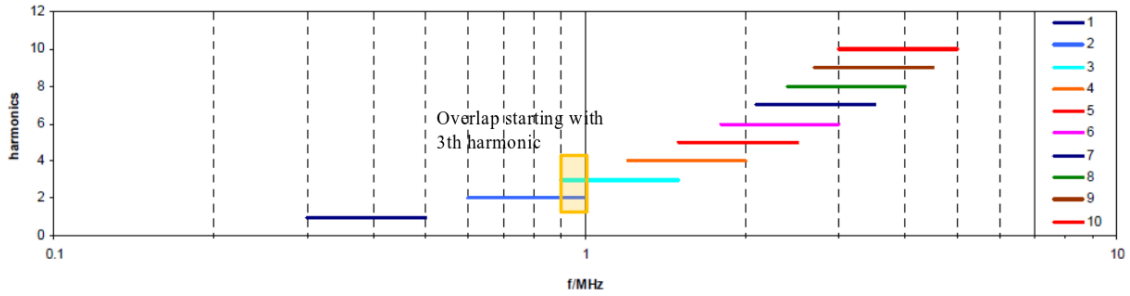
Or, in other terms:

$$h_{overlap} \geq \frac{1}{\delta} \cdot \left(\frac{1}{2} - \frac{f_m}{f_c} \right) + \frac{1}{2} \approx \frac{1}{2 \cdot \delta} + \frac{1}{2} \tag{F.22}$$

where $h_{overlap}$ is the harmonic number at which the overlap effect starts to occur.



(a)



(b)

Figure F.11: a) Frequency ranges for the harmonic content $\Delta f_c = 50\,kHz$, $f_c = 400\,kHz$, and b) $2 \cdot \Delta f_c = 100\,kHz$, $f_c = 400\,kHz$

In other words, larger values of frequency deviation (for a defined f_c) are to produce overlap at lower main harmonic numbers.

F.6 Periodic modulation profiles

F.6.1 Triangular modulation profile

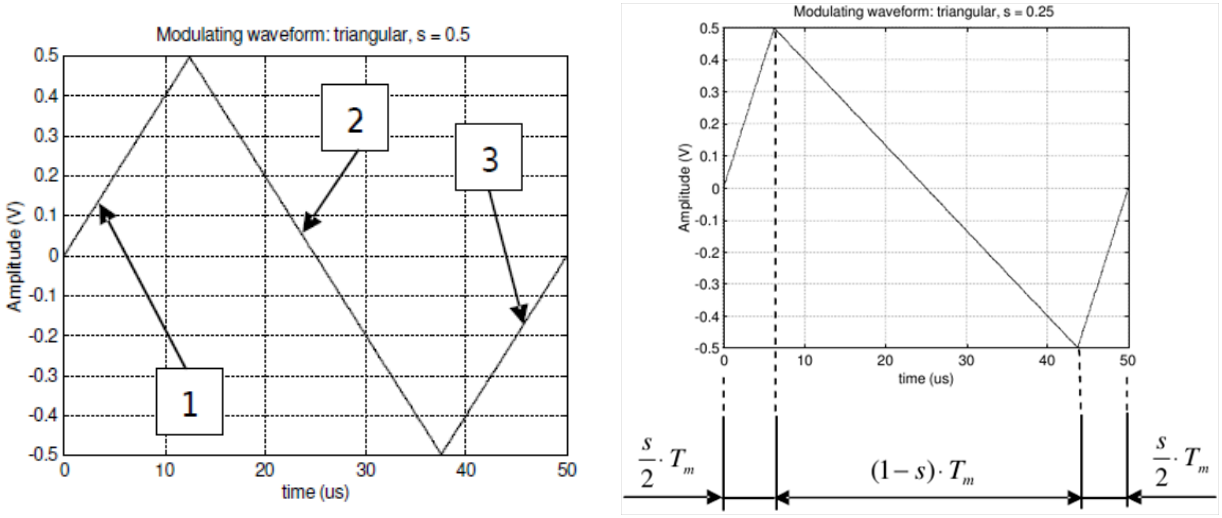
The triangular modulation profile consists of three trams, each one defined by an equation as shown below:

Parameter s controls the position of the vertex of the triangular waveform from 0 to $T_m/2$, thus making the implementation of profiles such a sawtooth waveform very easy. Parameter s can range from 0 to 1, and, for a classical triangular profile, $s = 0.5$.

Analytical expression for each trams can be expressed by means of the following equations:

(1) Valid for t where $0 \leq t < s \cdot \dfrac{T_m}{2}$, $v_m(t) = V_m \cdot f_m \cdot \dfrac{2}{s} \cdot t$

(2) Valid for t where $s \cdot \dfrac{T_m}{2} \leq t < \left(1 - \dfrac{s}{2}\right) \dfrac{T_m}{2}$, $v_m(t) = V_m \cdot \dfrac{1 - 2f_m \cdot t}{1 - s}$



(a) (b)

Figure F.12: Triangular modulating profiles: (a) symmetrical and (b) sawtooth type.

(3) Valid for t where $\left(1-\frac{s}{2}\right)\frac{T_m}{2} \leq t < T_m$, $v_m(t) = 2 \cdot V_m \cdot \frac{f_m \cdot t - 1}{s}$

F.6.2 Exponential

The exponential modulation can be expressed as a waveform consisting of four trams, each one defined by its corresponding analytical equation. The four trams are shown in Figure F.13.

Onwards, a more detailed description of each tram is to be developed, focusing specific attention on the different parameters describing this profile. Analytical expression for each trams can be expressed by means of the following equations:

(1) Valid for t where $0 \leq t < \frac{T_m}{4}$, $v_m(t) = V_m \cdot \frac{1}{e^{\frac{p}{4f_m}} - 1} \cdot \left(e^{p \cdot t} - 1\right)$

(2) Valid for t where $\frac{T_m}{4} \leq t < \frac{T_m}{2}$, $v_m(t) = V_m \cdot \frac{1}{e^{\frac{p}{4f_m}} - 1} \cdot \left(e^{\frac{p}{2f_m}} \cdot e^{-p \cdot t} - 1\right)$

(3) Valid for t where $\frac{T_m}{2} \leq t < \frac{3T_m}{4}$, $v_m(t) = V_m \cdot \frac{1}{e^{\frac{p}{4f_m}} - 1} \cdot \left(1 - e^{-\frac{p}{2f_m}} \cdot e^{p \cdot t}\right)$

(4) Valid for t where $\frac{3T_m}{4} \leq t < T_m$, $v_m(t) = V_m \cdot \frac{1}{e^{\frac{p}{4f_m}} - 1} \cdot \left(1 - e^{\frac{p}{f_m}} \cdot e^{-p \cdot t}\right)$

where parameter p is a function of the modulating frequency, that is, $p = k \cdot f_m$, where k is the concavity factor.

The hershey-kiss modulation profile is an exponential profile with a certain k value.

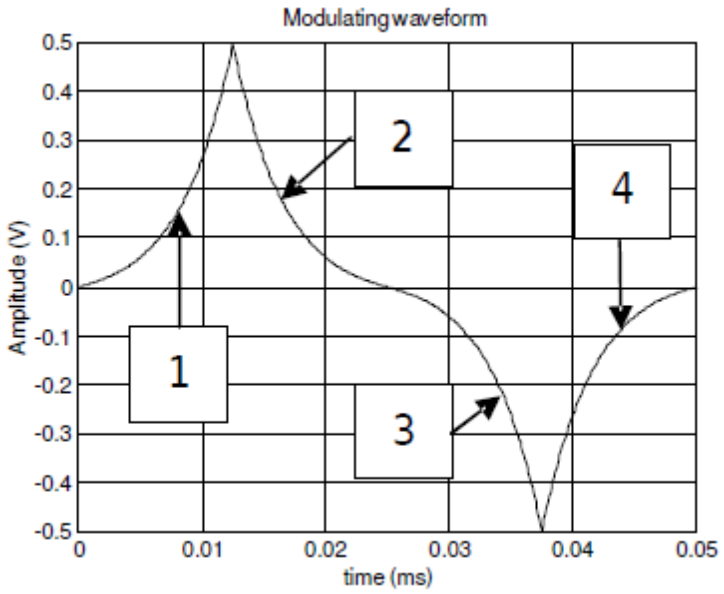


Figure F.13: Exponential modulating profile.

F.6.3 Considerations to the spectra distribution shape

The triangular modulation profile is the unique modulating waveform which produce a complete flat spectrum distribution shape, independently on the slope parameter s. It seems to be that modulation profiles consisting of straight lines, that is, constant slopes during the modulating period are to produce a flat distribution of the side-band harmonics. It is concluded then that modulation profiles, or trams of them, which are inscribed inside the triangular base, as expressed in Figure F.14, it is to obtain a concentration of the side-band harmonics around the carrier frequency, thus giving a peak aspect to the spectra distribution resulting from the frequency modulation process. In the same way, any modulation profiles, or trams of them, which stay outside the triangular base (see Figure F.14) are to produce a concentration of the side-band harmonics not at the carrier frequency but in the opposite sides, that is, a concentration around the two frequencies defining the bandwidth resulting from the modulation process.

Such behaviour can be explained approximately by using the frequency modulation concepts already presented. From expressions (F.2) and (F.3), the instantaneous frequency $\omega(t)$ corresponding to the modulated signal can be expressed as follows:

$$\omega(t) = \omega_c + \frac{d\Theta(t)}{dt} = \omega_c + k_\omega \cdot v_m(t) \tag{F.23}$$

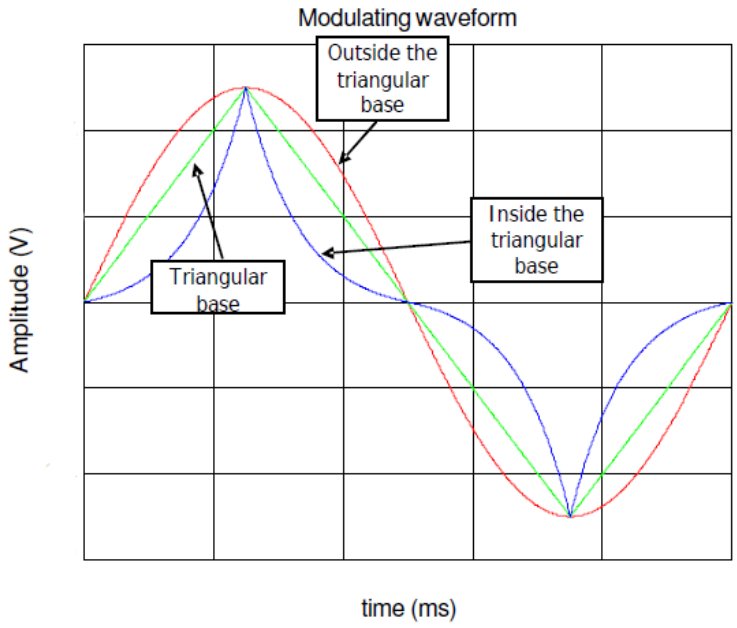


Figure F.14: Different modulation profiles compared to the triangular base

In other words, instantaneous frequency of a modulated waveform is depending only on the modulation profile $v_m(t)$ (as known) with an offset given by the carrier frequency ω_c. But the main interest does not rely on the instantaneous frequency itself but on the variation shape of this instantaneous frequency. This shape can be approximated by the first derivative of $\omega(t)$. From expression (F.23), it is obtained:

$$\frac{d\omega(t)}{dt} = k_\omega \cdot \frac{dv_m(t)}{dt} \tag{F.24}$$

This way, a triangular modulation profile, consisting of only linear trams of constant slope, will have also a constant first derivative. This means that the harmonic energy distribution will be constant along the whole bandwidth of modulation, thus giving a flat distribution shape. But if a modulation profile tends to be with a very low derivative of $v_m(t)$ during nearly the whole modulation period (for instance, an exponential modulation profile with a very high concavity factor k), this means that variation of $\omega(t)$ is very low during nearly the whole modulation period, thus only the carrier frequency will be present and supplying the maximum value to the spectra distribution. This can be the case of the waveforms inside the triangular base in Figure F.14. In a similar way, modulation profiles with a tendency to high derivatives of $v_m(t)$ during nearly the whole modulation period will tend to concentrate the energy far away from the central or carrier frequency ω_c.

F.6.4 The Multi-Slope Triangular or Multi-Triangular profile

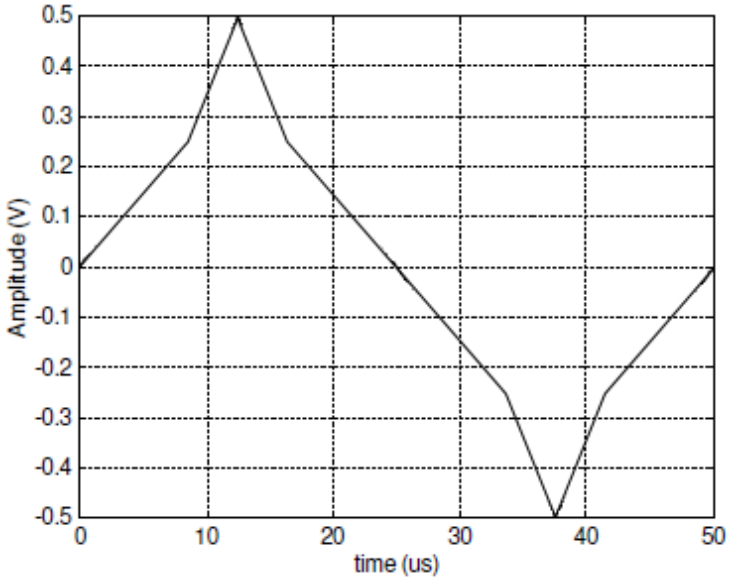


Figure F.15: Multi-Slope Triangular or Multi-Triangular modulating profile.

From different articles in literature the hershey-kiss profile seems to be the best modulation profile to be applied, but it's hard to implement without a digital approach and requires a royalty payment to be used. With these considerations in mind, if the best results and performances isn't the main concern, the choice fell on the implementation of simple modulation profiles like the triangular, and to avoid complex profiles like the hershey-kiss. To avoid this trade-off, we implemente a new modulation profile, that claims to be the junction point between triangular and herhey-kiss profiles, and the best trade-off between circuit complexity and performances. This new profile is, the so called, *multi-slope triangular* or *multi-triangular* profile, and is shown in Figure F.15. This profile is inscribed inside the triangular base, as expressed in Figure F.14, in this way it will obtain a concentration of the side-band harmonics around the carrier frequency, thus giving a peak aspect to the spectra distribution resulting from the frequency modulation process. Moreover, because the multi-triangular profile consists of only linear trams of constant slope, will have also a constant first derivative. This means that the harmonic energy distribution will be constant along the whole bandwidth of modulation, thus giving a flat distribution shape. Adding these two effects, we expect that a final distribution shape with a flat central portion and a with decreasing sideband harmonics as they become more distant from the central harmonic.

F.7 Multi-Cycle Modulation or Multiple Cycle Combination Modulation

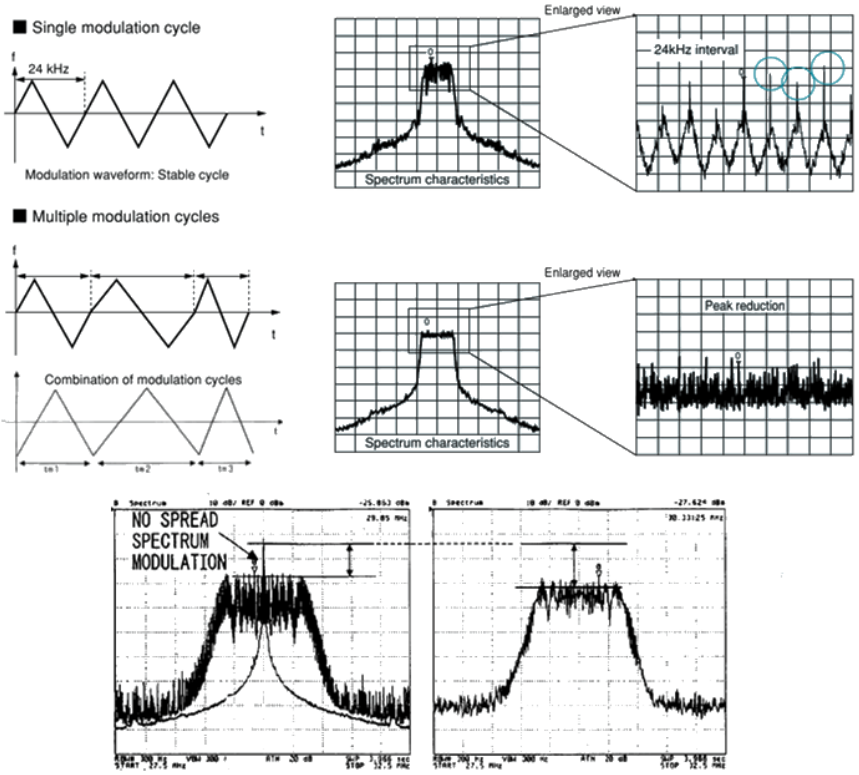


Figure F.16: Modulation by a Single Modulation Cycle and by Multiple Modulation Cycles

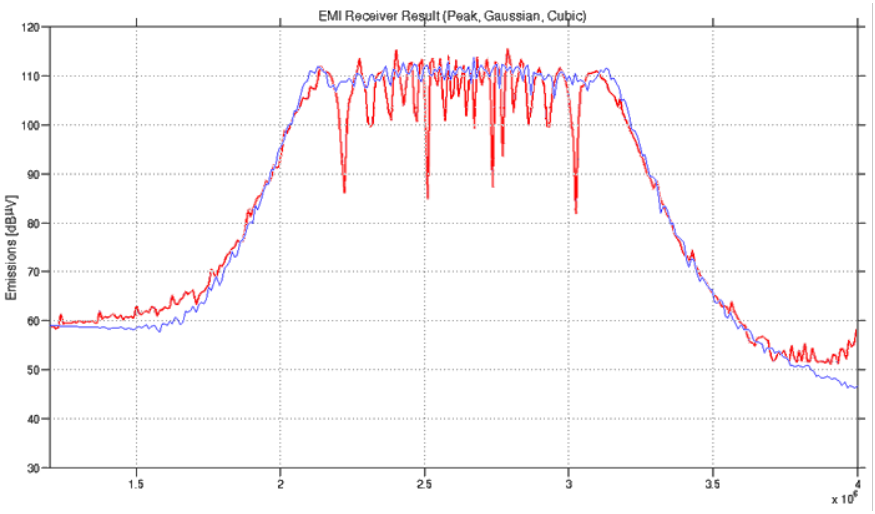


Figure F.17: Modulation by a Single Modulation Cycle and by Multiple Modulation Cycles

In general, SSCG modulated the frequency by a single modulation cycle. It thus caused the formation of a peak in the spectrum by the modulation cycle interval, resulting in an insufficient EMI reduction effect. To solve this problem, we used multiple modulation cycles to diffuse the spectrum uniformly and realize a larger EMI reduction effect. Figure F.16 presents modulation samples by a single modulation cycle and by multiple modulation cycles. In a conventional SSCG circuit, a triangular wave shaped spread spectrum modulation signal wich changes in a costant period, is used. Therefore, for example, if an oscillation frequency of 1 MHz is modulated with $f_m = 30kHz$, the spectrum conponents are spaced at intervals of 30 kHz, that is for a center-spread modulation, 910 kHz, 940 kHz, 970 kHz, 1 MHz, 1.03 MHz, 1.06 MHz, and 1.09 MHz, with $m_f = 7$ being the modulation index. In contrast to this, if the frequency of the modulating signal is changed in such a way that $f_{m_1} = 30kHz$, $f_{m_2} = 27kHz$, $f_{m_3} = 24kHz$, $f_{m_4} = 33kHz$ and $f_{m_5} = 36kHz$, as shown in Figure F.16, the spectrum components are divided into five groups, that is, one group in wich they are spaced at intervals of 24 kHz, another one in which they are spaced at intervals of 27 kHz, and so on, at intervals of 30 kHz, 33 kHz and 36 kHz. As the period of the spread spectrum modulation signal changes so as to take multiple different periods, the spectrum is further spread compared to the case where the period is costant.

It is also possible to change the period of the modulating signal at the point of zero-crossing, or change the period at the point where the amplitude is minimum or maximum, or finally at a predeterminated value. Moreover, the number of variable periods is not limited to five, but it may be more or less as the number is larger than one.

F.8 Influence on the power converter output voltage of the modulation profile

It is of great interest to find out the influence of modulation profiles on the output voltage of the converter. In order to answer this question, a finer development is carried out onwards. As in a real power converter, a square waveform is being frequency modulated following a certain modulation profile (e.g., Figure F.18(c)), which means that the instantaneous frequency of the signal is changing constantly. This way, a new more complicated signal appears, but showing a constant period T_m which repeats indefinitely in time.

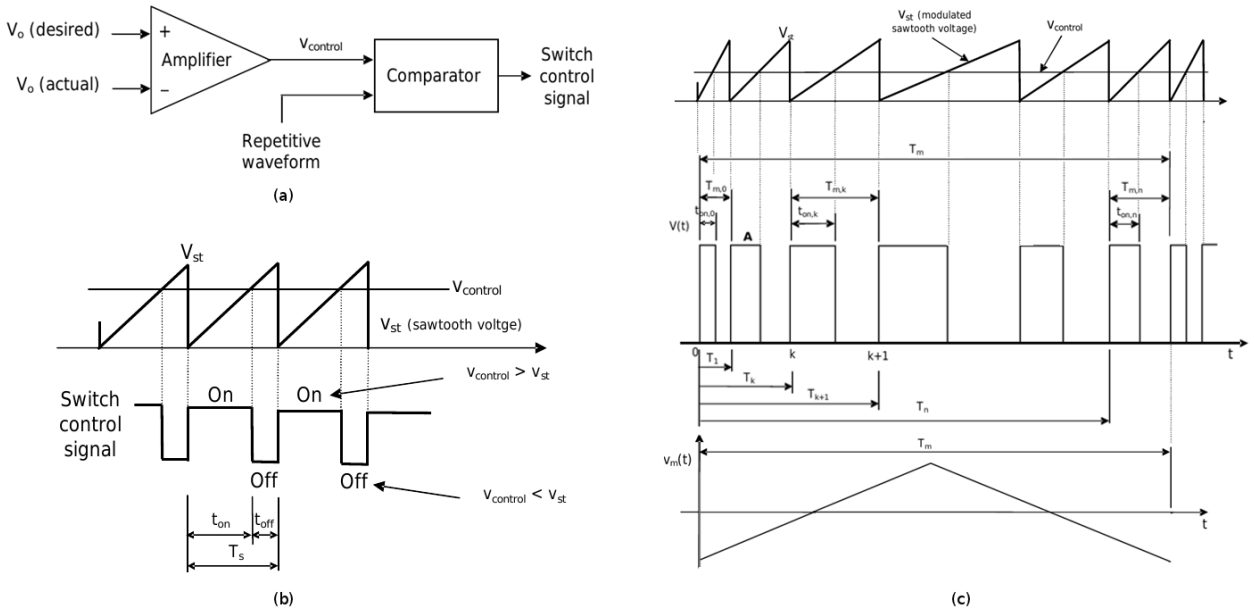


Figure F.18: (a) A typical PWM control schematic, (b) the PWM waveforms and (c) a frequency-modulated PWM waveform by a triangular modulation profile

Calculating the average voltage of the modulated square waveform in Figure F.18(c) yields:

$$V_{average} = \frac{1}{T_m} \cdot \int_0^{T_m} V(t) \cdot dt \tag{F.25}$$

Separating the total integral into different partial integrals yields:

$$V_{average} = \frac{1}{T_m} \cdot \left[\int_0^{T_1} V(t) \cdot dt + \int_{T_1}^{T_2} V(t) \cdot dt + \cdots + \int_{T_k}^{T_{k+1}} V(t) \cdot dt + \cdots + \int_{T_n}^{T_m} V(t) \cdot dt \right] \tag{F.26}$$

with k from 0 to a generic n. A generic partial integral in expression (F.26) can also be expressed as follows:

$$\int_{T_k}^{T_{k+1}} V(t) \cdot dt = \int_{T_k}^{T_k + T_{m,k}} V(t) \cdot dt == \int_{T_k}^{T_k + t_{on,k}} A \cdot dt = A \cdot t_{on,k} \tag{F.27}$$

Because $V(t)$ is zero outside the $t_{on,k}$ period. Duty-cycle D is constant through the whole period T_m, that is, $D = \frac{t_{on,k}}{T_{m,k}}$ thus the generic partial integral in expression (F.27) can be rewritten as follows:

$$\int_{T_k}^{T_{k+1}} V(t) \cdot dt = A \cdot D \cdot T_{m,k} \tag{F.28}$$

Thus, the average voltage of the modulated square waveform results:

$$V_{average} = \frac{1}{T_m} \cdot \left[A \cdot D \cdot \sum_{k=0}^{n} T_{m,k} \right] = \frac{1}{T_m} \cdot [A \cdot D \cdot T_m] = A \cdot D \tag{F.29}$$

because the sum inside the integral is exactly the modulating period T_m.

Therefore, no influence of the modulation profile on the output voltage is expected, at least theoretically, with the condition of guaranteeing a constant instantaneous duty-cycle D during the modulating period T_m.

One easy conclusion to be derived from the previous analysis is that higher modulation indexes are to produce larger attenuations. Therefore, higher modulation indexes should be selected and, through its definition $m_f = \frac{\delta \cdot f_c}{f_m}$, this can be done by increasing the modulation ratio δ or the carrier frequency f_c or decreasing the modulating frequency f_m.

Switching frequency in power converters is not usually too large because the electronics components (diodes and power transistors, mainly) are not able to manage larger power with shorter switching times. Anyway, use of higher switching frequencies is advisable in order to reduce the size and power capability of the passive components (filters, inductances, diodes, transistors and so on) and increase the power efficiency of the converter. Maximum typical commercial switching frequencies are about 2.5 MHz or less.

If limitations in switching frequencies are found in order to increase the modulation index, another possibility consists of decreasing the modulating frequency as many as possible. Depending on the switching frequency, lower modulating frequencies f_m can result in a negligible normative benefit due to the regulatory RBW to be adjusted on the compliant Spectrum Analyzer.

Taking into account the limitations related to the switching frequency f_c and the modulating frequency f_m, the only chance to increase the modulation index m_f comes from increasing the modulation ratio δ as much as possible. But as explained above, carrier frequency peak deviation $\Delta f_c = \delta \cdot f_c$ is limited by power converter's filter considerations.

Appendix G

Performing Spectrum Analysis

Theoretical basis of the thesis is based on the fundaments of the Fourier Transform and the related computational algorithm is a particular implementation of the Fast Fourier Transform (FFT). The computational algorithm hereby developed is intended to obtain the theoretical spectral components resulting from the frequency modulation process. This algorithm was developed for a MATLAB environment, thus, some particularities more must also been taken into account.

G.1 Considerations to apply FFT correctly to the MATLAB algorithm

G.1.1 Limits on FFT analysis

When using FFT anaysis to study the frequency spectrum of signals, there are limits on resolution between different frequencies, and on detectability of a small signal in the presence of a large one. It is easy to gain an insight by thinking about the special case of a pure sine wave. This has a frequency spectrum which is a single spectral line: but the frequency spectrum calculated by the FFT will show a spread out line. Each spectral line will be spread out in the same way. There are two basic problems: the fact that we can only measure the signal for a limited time; and the fact that the FFT only calculates results for certain discrete frequency values (the *FFT bins*). The limit on measurement time is fundamental to any frequency analysis technique: the frequency sampling is peculiar to numerical methods like the FFT.

The mathematical calculation of the frequency spectra by means of the FFT shows some difficulties to obtain accurate and correct results. The *Discrete Fourier transform* (DFT) is expressed as follows:

$$H\left(\frac{n}{NT}\right) = T \cdot \sum_{k=0}^{N-1} h(kT) \cdot e^{-j2\pi nk/N} \qquad n = 0,\, 1,\, L,\, N-1 \tag{G.1}$$

where T is the sampling period (time domain) and N is the number of equidistant samples inside the truncation interval T_0, equated to the modulating period $T_m = 1/f_m$.

The key-point of the DFT is that the result matches exactly the one given by the continuous Fourier transform just preserving the following conditions:

- the time function $h(t)$ must be periodic.
- $h(t)$ must be band-limited. An FM signal actually contains an infinite number of side frequencies besides the carrier and therefore occupies infinite bandwidth. However, the side frequencies quickly decrease in strength and can be considered negligible at some point. In practice, a tradeoff between bandwidth and distortion must be considered. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule.
- the sampling rate must be at least two times the largest frequency component of $h(t)$ Nyquist's theorem.
- the truncation function $x(t)$ must be non-zero over exactly one period (or integer multiple period) of $h(t)$.

DFT assumes that the waveform sampled during this sampling time of T (the period of the signal) repeats itself down- and upwards indefinitely.

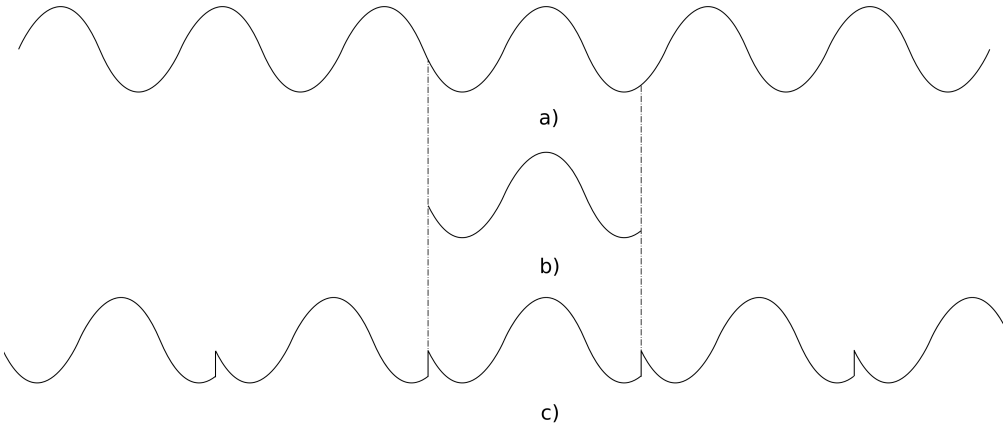


Figure G.1: Real input signal (a), measured interval (b) and the signal assumed by the FFT

The first problem arises because the signal can only be measured for a limited time. Nothing can be known about the signal's behaviour outside the measured interval. We have to assume

something about the signal outside the measured interval, and the Fourier Transform makes an implicit assumption that the signal is repetitive: that is, the signal within the measured time repeats for all time. Most real signals will have discontinuities at the ends of the measured time, and when the FFT assumes the signal repeats it will assume discontinuities that are not really there. Since sharp discontinuities have broad frequency spectra, these will cause the signal's frequency spectrum to be spread out.

The spreading means that signal energy which should be concentrated only at one frequency instead leaks into all the other frequencies. This spreading of energy is called *spectral leakage*.

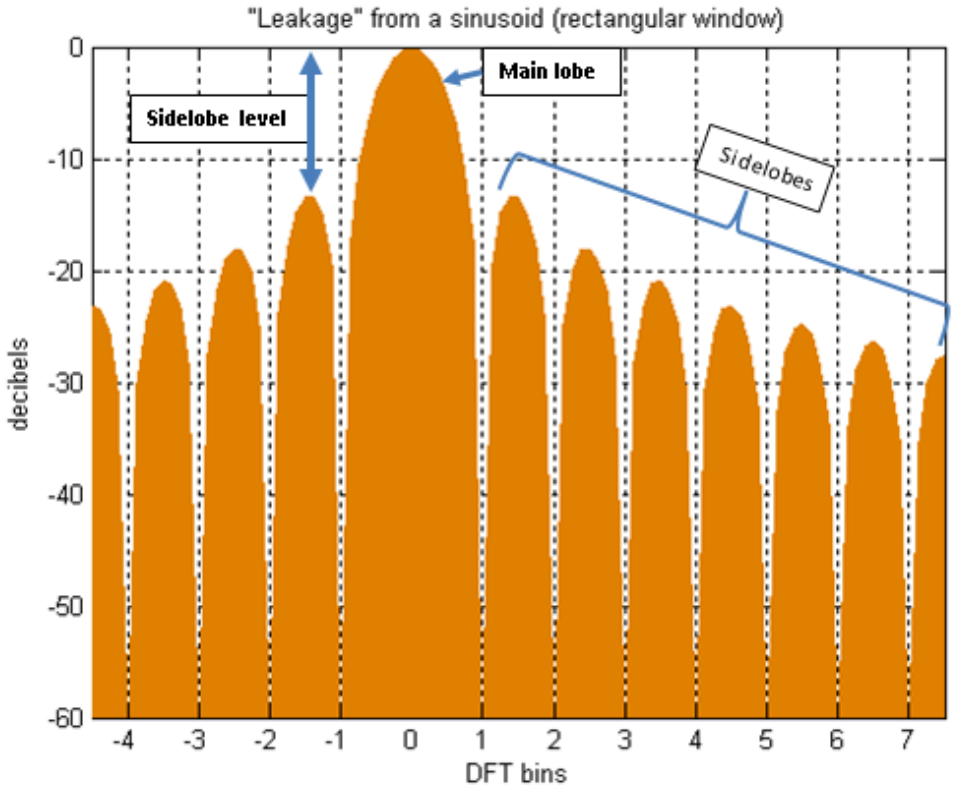


Figure G.2: Zoomed view of spectral leakage

Since spectral leakage is related to discontinuities at the ends of the measurement time, it will be worse for signals that happen to fall such that there are large discontinuities. Some signals may, by coincidence or by design, fall in such a way that there happens to be no discontinuity at the ends of the measurement time: for these signals the effect of spectral leakage may be lessened.

Spectral leakage is not an artifact of the FFT, but is only due to the fact that the signal was

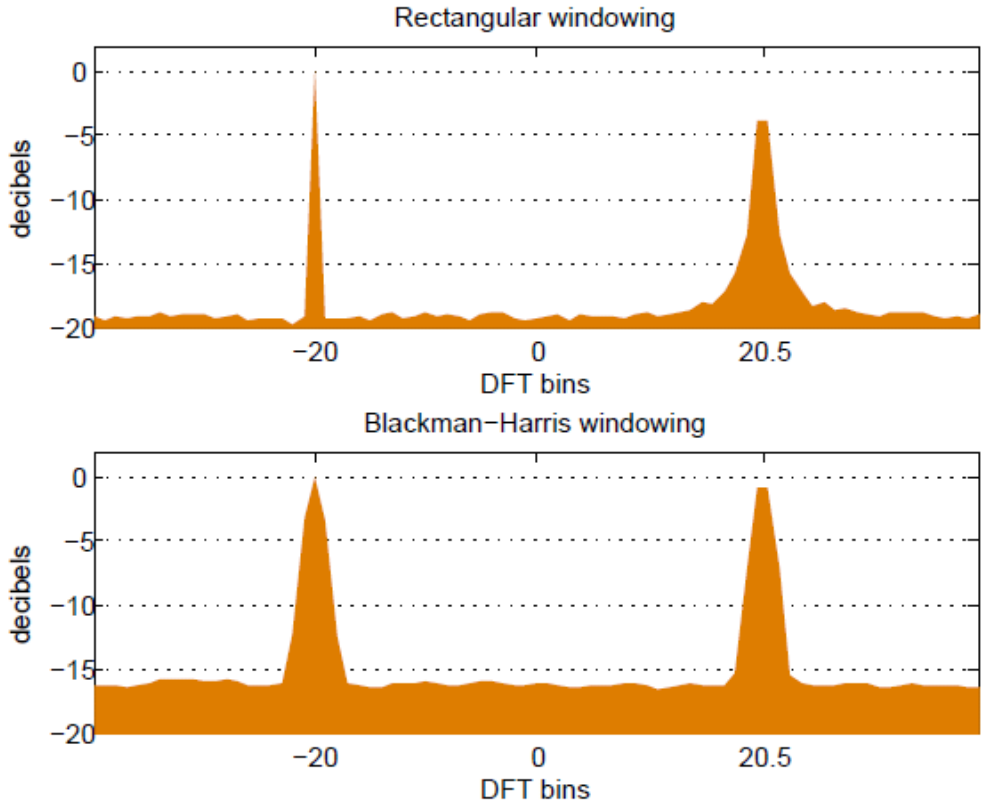


Figure G.3: Comparison of two window functions in terms of their effects on equal-strength sinusoids with additive noise. The sinusoid at bin -20 suffers no scalloping and the one at bin +20.5 exhibits worst-case scalloping. The rectangular window produces the most scalloping but also narrower peaks and lower noise-floor. A third sinusoid with amplitude -16 dB would be noticeable in the upper spectrum, but not in the lower spectrum.

measured only for a finite time. For a sine wave to have a single line spectrum it must exist for all time. Any practical method of calculating the frequency spectrum of a signal suffers from spectral leakage due to the finite measurement time. Spectral leakage causes at least two distinct problems. First, any given spectral component will contain not just the signal energy, but also noise from the whole of the rest of the spectrum. This will degrade the signal to noise ratio SNR. Second, the spectral leakage from a large signal component may be severe enough to mask other smaller signals at different frequencies.

G.1.2 Windowing

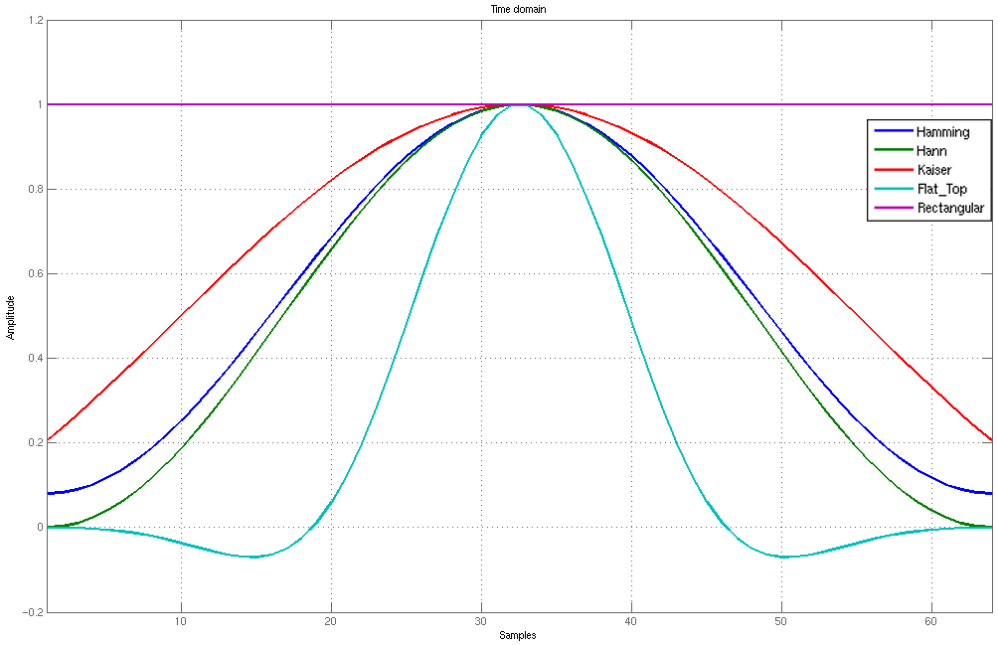
In effect, the process of measuring a signal for a finite time is equivalent to multiplying the signal by a rectangular function of unit amplitude: the rectangular function lasting for the duration of the measurement time. The signal is measured during a finite measurement time or *window*. This idea leads to the rectangular function being called a *rectangular window*. The effects of spectral leakage can be reduced by reducing the discontinuities at the ends of the signal measurement time. This leads to the idea of multiplying the signal within the measurement time by some function that smoothly reduces the signal to zero at the end points: hence avoiding discontinuities altogether. The process of multiplying the signal data by a function that smoothly approaches zero at both ends, is called *windowing*: and the multiplying function is called a *window function*. It is easy to analyse the effect of a window function: the frequency spectrum of the signal is convolved with the frequency spectrum of the window function.

One way to visualise spectral leakage is as spreading of the frequency components. Each frequency should contribute only to one FFT bin but spectral leakage causes the energy to be spread by the window function so it contributes to all other FFT bins. The contribution is weighted by the window function centred at the frequency component and evaluated at the FFT bin. In the special case of the rectangular window (that is, no window at all), the window function is 1 in the interval and 0 outside the interval. Its Fourier transform is known as the *sinc()* function, or more formally the *Dirichlet kernel*. The shape of the Fourier transform of a window function is sometimes called the *kernel*.

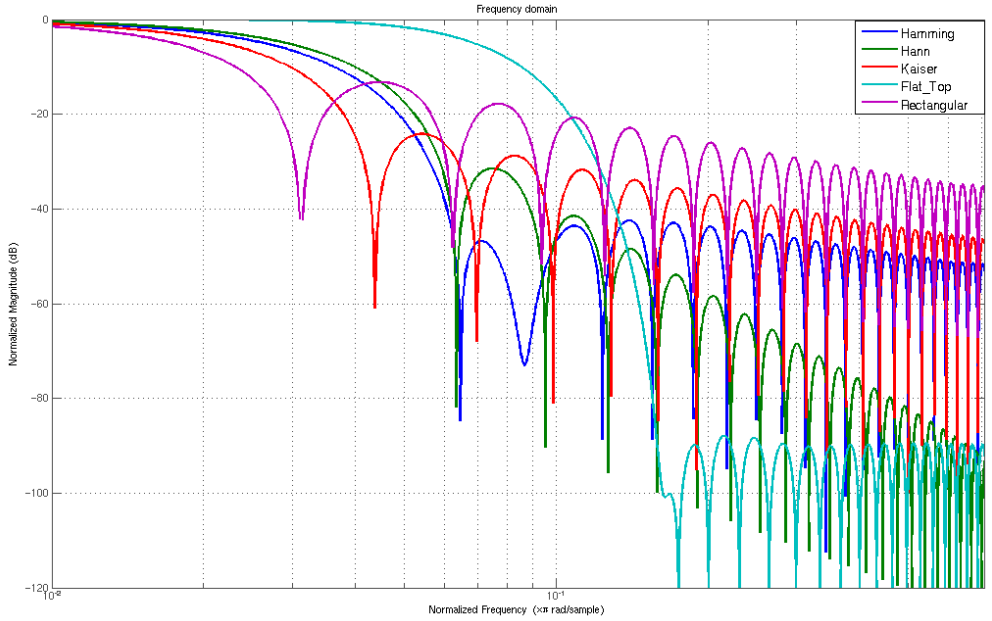
Another productive way to visualise spectral leakage is to regard the FFT as equivalent to a series of filters, centred on each spectral sample. The filter's frequency response is the shape of the window function. This is the inverse of the spectral leakage model. Each FFT bin includes contributions from all other frequencies in the bandwidth of the filter, weighted by the window function. This will include contributions from broad-band noise as well as narrow-band signals at other frequencies.

There are two common situations: detection of a spectral component in the presence of broadband noise; or distinguishing between narrow band spectral components. The choice of window function may be different in the two cases of detection or resolution.

The *Equivalent Noise Bandwidth (ENB)* of the window measures the noise performance of



(a)



(b)

Figure G.4: Hanning, Hann, Kaiser, Flat Top and Rectangular window in (a) time domain and (b) frequency domain.

the window. It is the width of a rectangle filter which would accumulate the same noise power with the same peak power gain.

Coherent Power Gain measures the reduction in signal power due to the window function suppressing a coherent signal at the ends of the measurement interval. For an ideal discrete line frequency component, the noiseless signal contribution to the FFT bin is proportional to the signal amplitude. The proportionality factor is the sum of the window terms, which is just the DC gain of the window and the coherent power gain is the square of this. For a rectangular window the DC gain is N(number of terms in the window): but for any other window the DC gain will be reduced because the window goes smoothly to zero at the ends of the measurement time. The reduction in DC gain is important because it represents a definite scaling of the amplitudes of the frequency spectrum which requires correction for any absolute measurements to be correct. Coherent gain is usually normalised by dividing by N.

Processing Loss is the ratio of input signal to noise to output signal to noise, which is the Coherent Power Gain divided by the noise power. For a signal made up of an ideal discrete line frequency component polluted by white noise, the Processing Loss is, the reciprocal of the Equivalent Noise Bandwidth (ENB).

The model of the FFT as a series of filters centred on the FFT bins suggests that frequencies that do not coincide with the FFT bins will be attenuated as the filter's response falls off away from the centre frequency. This effect will vary as the signal frequency ranges between the adjacent FFT bins, and is called *the picket fence effect* or *scalloping*. It is a reasonable assumption that the worst case occurs when the signal frequency lies exactly half way between FFT bins. *Scalloping Loss* is defined as the ratio of coherent gain for a signal frequency component located half way between FFT bins, to the coherent gain for a signal frequency component located exactly at an FFT bin. This is just the ratio of the window function's value one half a frequency sample off centre, to the its value at the centre frequency.

Worst case processing loss is defined as the sum of Scalloping Loss and Processing Loss. This is a measure of the reduction of output signal to noise ratio resulting from the combination of the window function and the worst case frequency location.

To minimise the effects of spectral leakage, a window function's FFT should have low amplitude sidelobes away from the centre, and the fall off to the low sidelobes should be rapid. The peak

sidelobe level is a useful indicator of how well a window function suppresses spectral leakage: so is the rate of fall off to the sidelobes.

An interesting measure is the minimum separation needed between two frequency components of equal amplitude, so that they can be resolved. By resolved, is meant that there should be a local minimum between the two peaks. The 'rule of thumb' for resolvability is the width of the window at the half power points (the 3 dB bandwidth): because two frequency components of equal strength show a single peak if separated by less than their 3 dB bandwidth, and so cannot be separated. But this assumes incoherent addition. There is an important problem with this criterion when applied to the FFT because the addition which is involved with the FFT is coherent, not incoherent. The FFT output is the coherent addition of frequency components, weighted by the window function at each frequency. Because of the coherence, the 6 dB bandwidth defines resolution rather than the 3 dB bandwidth. If two frequency components are involved the sum of the window functions at the crossover point (halfway between the peaks) must be smaller than the individual peaks if the two peaks are to be resolved. So the gain from each window function must be less than 0.5 (or 6 dB).

G.1.3 Parameter considerations

SSCG techniques are based on modulating the frequency of a carrier signal by following a selected modulation profile. The waveform resulting from this modulation process is a periodic signal whose frequency equates the frequency of the modulating signal f_m, that is, the modulation profile. This is easy to understand taking into account that the carrier signal frequency is constantly varying, following the modulation profile, but showing the same value of frequency (normally the carrier signal frequency) both at the beginning and at the end of the complete cycle of variation through the modulation profile. This way, it is obtained a modulated waveform which repeats itself indefinitely with a period of $1/f_m$. Several points have to be taken into account:

(1) As the period of the modulated signal is perfectly known and equal to the modulating frequency f_m, a truncation window of $T_0 = 1/f_m$ is to be selected in order to avoid any problems. Resolution or distance F in frequency domain between two consecutive samples is given by the following expression:

$$F = \frac{1}{N \cdot T} = \frac{1}{T_0} = f_m = f_s \cdot N \tag{G.2}$$

where T is the sampling period (time domain), N is the number of equidistant samples inside the truncation interval T_0 and f_s is the sampling frequency.

(2) In order to rebuild a sampled waveform without losing any information, the Nyquist's theorem establishes that the sampling frequency must be, at least, twice the largest frequency composing the original waveform. Besides, the Carson's rule specifies that the harmonic spectra resulting from modulating a sinusoidal signal are included inside a bandwidth B_h given by the following expression (for the 98% of the total energy of the original signal):

$$B_h = 2 \cdot f_m \cdot (1 + h \cdot m_f) \qquad \text{with} \qquad m_f = \frac{\Delta f_c}{f_m} \tag{G.3}$$

Supposing this bandwidth to be symmetrically distributed around the non modulated harmonic f_h, the maximum frequency f_{max} of the modulated waveform can be approximately expressed as follows:

$$f_{max} = f_h + \frac{B_h}{2} \tag{G.4}$$

Thus, the sampling frequency fs must meet the following expression:

$$f_s \geq 2 \cdot f_{max} = 2 \cdot f_h + B_h = 2 \cdot (f_h + f_m + h \cdot \Delta f_c) \tag{G.5}$$

$$f_s \geq 2 \cdot (f_c + f_m + \Delta f_c) \text{ for the first harmonic of the non-modulated signal } (h = 1) \tag{G.6}$$

(3) The number of samples N must be a power of 2, that is, $N = 2^k$ where k is a natural number. This aspect improves the efficiency of the FFT which is normally expressed in terms of number of complex multiplications. As said before, a conventional DFT needs approximately a number of N^2 complex multiplications, while for a FFT, a number of $N \cdot \log_2(N)$ is typical.

(4) The FFT algorithm returns a total number of N points but only the $N/2$ first ones are of interest because the rest $N/2$ points are symmetrical respect to the first ones.

(5) The particular frequency of a generic point k from the FFT algorithm is expressed as follows:

$$f_k = k \cdot \frac{f_s}{N} \tag{G.7}$$

From the last point 6), it can be derived that the maximum generic frequency f_k which is able to be displayed corresponds to $k = N/2$ or, in other terms, to a frequency of $f_s/2$.

G.2 Interpolation

In this section we discuss some simple interpolation techniques available in Matlab. Interpolation is a process for estimating values that lie between known data points.

G.2.1 Interpolant Methods

We might get different estimation of values with different types of interpolation. It is impossible to say which estimation gives more accurate answer without studying the dynamics of the physical system. We must always keep in mind that our results will be approximate and should be used with caution.

The type of interpolant to use depends on the characteristics of the data being fit, the required smoothness of the curve, speed considerations, post-fit analysis requirements, and so on. The linear and nearest neighbor methods are fast, but the resulting curves are not very smooth. The cubic spline and shape-preserving methods are slower, but the resulting curves are very smooth.

(1) Nearest neighbor: This method sets the value of an interpolated point to the value of the nearest data point.

```
yi = interp1(x,y,xi,'nearest')
```

(2) Linear: This method fits a different linear polynomial between each pair of data points. Linear interpolation is so named because it is equivalent to connecting the data points with a straight line.

```
yi = interp1(x,y,xi,'linear')
```

(3) Cubic spline: This method fits a different cubic polynomial between each pair of data points. In Spline interpolation we get smooth curve of the function through a set of points rather than sharp edges at data points.

`yi = interp1(x,y,xi,'spline')` or `yi = spline(x,y,xi)` Fit a cubic polynomial of the form

$$y = a + b \cdot x + c \cdot x^2 + d \cdot x^3 \tag{G.8}$$

through pairs of successive points. Match dy/dx and d^2y/dx^2 between adjacent splines at each interior point and set $d^2y/dx^2 = 0$ at end points.

(4) Shape-preserving Piecewise Cubic Hermite spline (`pchip` or `cubic`): This method preserves monotonicity and the shape of the data.

`yi = interp1(x,y,xi,'pchip')` or `yi = interp1(x,y,xi,'cubic')` This is a cubic spline that for each pair of adjacent points matches the end points values and prescribed slopes which are continuous between segments. At the exterior points, Matlab uses the gradient of the segment. At each interior point Matlab determines the slope to be either 0 if the slope changes sign between segments or is zero in either segment. Otherwise by a weighted mean of the slope in the two adjacent segments.

$$\left(\frac{dy}{dx}\right)_k = \frac{(x_{k+1}+x_k-2x_{k-1})}{3\,(x_{i+1}-x_{i-1})}\cdot\frac{(y_{k+1}+y_k)}{(x_{k+1}-x_k)}+\frac{(2x_{k+1}-x_k-x_{k-1})}{3\,(x_{i+1}-x_{i-1})}\cdot\frac{(y_k-y_{k-1})}{2\,(x_k-x_{k-1})} \quad \text{(G.9)}$$

The `pchip` spline preserves the shape of the data and avoids the overshoots common in a standard cubic spline.

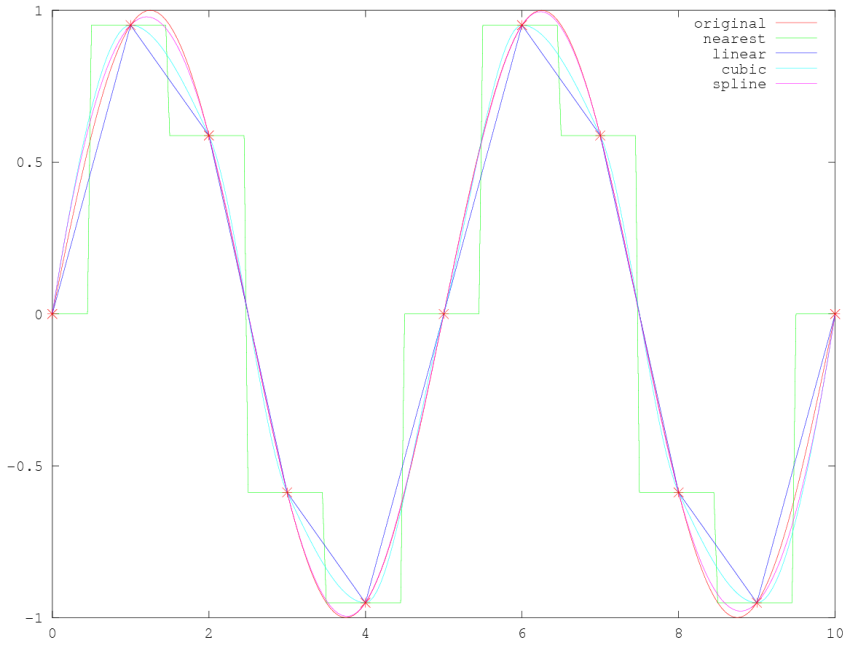


Figure G.5: Comparision of differerent interpolation methods

G.2.2 Spline Interpolant (SI) or Shape Preserving Interpolant (SPI)?

They are both piecewise cubic functions, however, the SPI may not give a continuous second derivative. Internally, for SI, Matlab will call on `spline`, and for SPI, will call `pchip`. Here are

some differences between `spline` and `pchip`:

- spline produces a smoother result, i.e. is continuous.
- spline produces a more accurate result if the data consists of values of a smooth function.
- pchip has no overshoots and less oscillation if the data are not smooth.
- pchip is less expensive to set up.
- The two are equally expensive to evaluate.

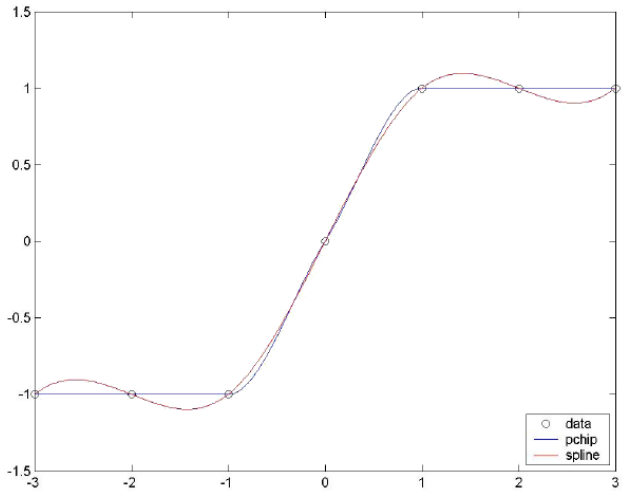


Figure G.6: Note that the spline interpolant overshoots the data, while the shape preserving interpolant does not.

Interpolants are defined as piecewise polynomials because the fitted curve is constructed from many "pieces". For cubic spline and PCHIP interpolation, each piece is described by four coefficients, which the toolbox calculates using a cubic (third-degree) polynomial.

Appendix H

Timing Jitter and Phase Noise

No timing considerations have been made until now. In most applications, the amount of spreading of a SSCG is of significant concern. That is not true, however, for set up and hold times. As the frequency is increased, set up and hold margins decrease. Some designs use such tight set up and hold margins that any frequency increase cannot be tolerated. For this reason, spread spectrum clock generation is sometimes implemented using a "down spreading" only technique. Instead of shifting the clock frequency above or below around the narrow band carrier, the frequency is only shifted downwards, which should only increase the setup and hold margins.

The phase noise of an oscillator specifies an oscillator's frequency instability in the frequency domain, and is observable as spreading of the oscillator's signal power around the intended spectral lines. It is related to the oscillator's susceptibility to modulation by noise, originating from components within the oscillator itself. The jitter is the time domain counterpart of the phase noise specification. Phase noise and jitter are tightly related to each other. The phase noise or jitter is an important oscillator parameter as it plays a role in the signal-to-noise ratio that can be achieved in the signal handling of oscillator based applications like frequency modulation.

Jitter measures undesired fluctuations in the timing of events. In oscillators and frequency synthesizers period jitter quantifies the time domain uncertainty of the output signal, whereas in thresholding and digital period jitter describes the misalignment of the significant edges of a digital signal from their ideal position in time. From communication system's definition, "jitter is an abrupt and unwanted variation of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles or the frequency or phase of successive cycles."

H.1 Oscillator Phase Noise

Nonlinear oscillators naturally produce high levels of phase noise. To see why, consider the trajectory of a fully autonomous oscillator's stable periodic orbit in state space. In steady state, the trajectory is a stable limit cycle, v. Now consider perturbing the oscillator with an impulse and assume that the deviation in the response due to the perturbation is Δv, as shown in Figure H.1. Separate Δv into amplitude and phase variations:

$$\Delta v(t) = [1 + \alpha(t)] \cdot v\left(t + \frac{\phi(t)}{2\pi f_0}\right) - v\,(t) \tag{H.1}$$

where v represents the unperturbed T-periodic output voltage of the oscillator, α represents the variation in amplitude, ϕ is the variation in phase, and $f_0 = 1/T$ is the oscillation frequency.

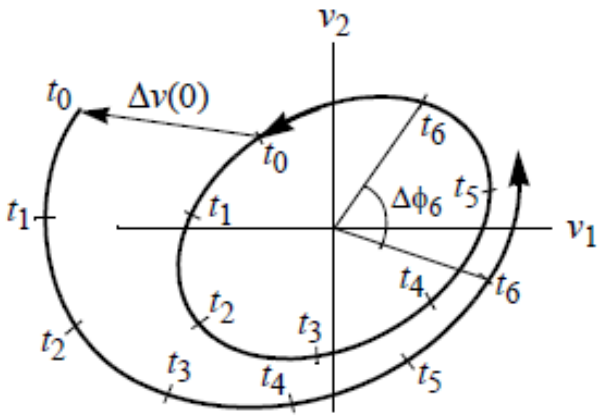


Figure H.1: The trajectory of an oscillator shown in state space with and without a perturbation Δv. By observing the time stamps $(t_0, ..., t_6)$ one can see that the deviation in amplitude dissipates while the deviation in phase does not.

Since the oscillator is stable and the duration of the disturbance is finite, the deviation in amplitude eventually decays away and the oscillator returns to its stable orbit ($\alpha(t) \to 0$ as $t \to \infty$). In effect, there is a restoring force that tends to act against amplitude noise. This restoring force is a natural consequence of the nonlinear nature of the oscillator that acts to suppresses amplitude variations. The oscillator is autonomous, and so any time-shifted version of the solution is also a solution. Once the phase has shifted due to a perturbation, the oscillator continues on as if never disturbed except for the shift in the phase of the oscillation. There is no restoring force on the phase and so phase deviations accumulate. A single perturbation causes the phase to permanently shift ($\phi(t) \to \Delta\phi$ as $t \to \infty$). If we neglect any short term time constants, it can be inferred that

the impulse response of the phase deviation $\phi(t)$. can be approximated with a unit step $s(t)$. The phase shift over time for an arbitrary input disturbance u is:

$$\phi(t) \sim \int_{-\infty}^{\infty} s(t-\tau) j(\tau) d\tau = \int_{-\infty}^{t} j(\tau) d\tau \tag{H.2}$$

or the power spectral density (PSD) of the phase is:

$$S_{\phi}(\Delta f) \sim \frac{S_j(\Delta f)}{(2\pi \Delta f)^2} \tag{H.3}$$

This shows that in all oscillators the response to any form of perturbation, including noise, is amplified and appears mainly in the phase. The amplification increases as the frequency of the perturbation approaches the frequency of oscillation in proportion to $1/\Delta f$ (or $1/\Delta f^2$ in power). Notice that there is only one degree of freedom (the phase of the oscillator as a whole). There is no restoring force when the phase of all signals associated with the oscillator shift together, however there would be a restoring force if the phase of signals shifted relative to each other. This observation is significant in oscillators with multiple outputs, such as quadrature or ring oscillators. The dominant phase variations appear identically in all outputs, whereas relative phase variations between the outputs are naturally suppressed by the oscillator or added by subsequent circuitry and so tend to be much smaller.

H.2 Characterizing Oscillator Phase Noise

Above it was shown that oscillators tend to convert perturbations from any source into a phase variation at their output with an amplification that varies with $1/\Delta f$ (or $1/\Delta f^2$ in power). Now assume that the perturbation is from device noise in the form of white and flicker stochastic processes. The oscillator's response will be characterized first in terms of the phase noise $S\phi$, and then because phase noise is not easily measured, in terms of the normalized single-sideband noise power L. The result will be a small set of easily extracted parameters that completely describe the response of the oscillator to white and flicker noise sources. These parameters are used when modeling the oscillator. Assume that the perturbation consists of white and flicker noise and so has the form:

$$S_j(\Delta f) \sim 1 + \frac{f_c}{\Delta f} \tag{H.4}$$

Then from () the response will take the form

$$S_{\phi}(\Delta f) \sim n \cdot \left(\frac{1}{\Delta f^2} + \frac{f_c}{\Delta f^3} \right) \tag{H.5}$$

where the factor of $(2\pi)^2$ in the denominator of () has been absorbed into the constant of proportionality n and $S\phi$ is chosen to be the single-sided PSD[1] . Thus, the response of the oscillator to white and flicker noise sources is characterized using just two parameters, n and f_c, where n is the portion of $S\phi$ attributable to the white noise sources alone at $\Delta f = 1\,Hz$ and f_c is the flicker noise corner frequency.

As shown in Figure H.2, n is extracted by simply extrapolating to $1\,Hz$ from a frequency where the noise from the white sources dominates.

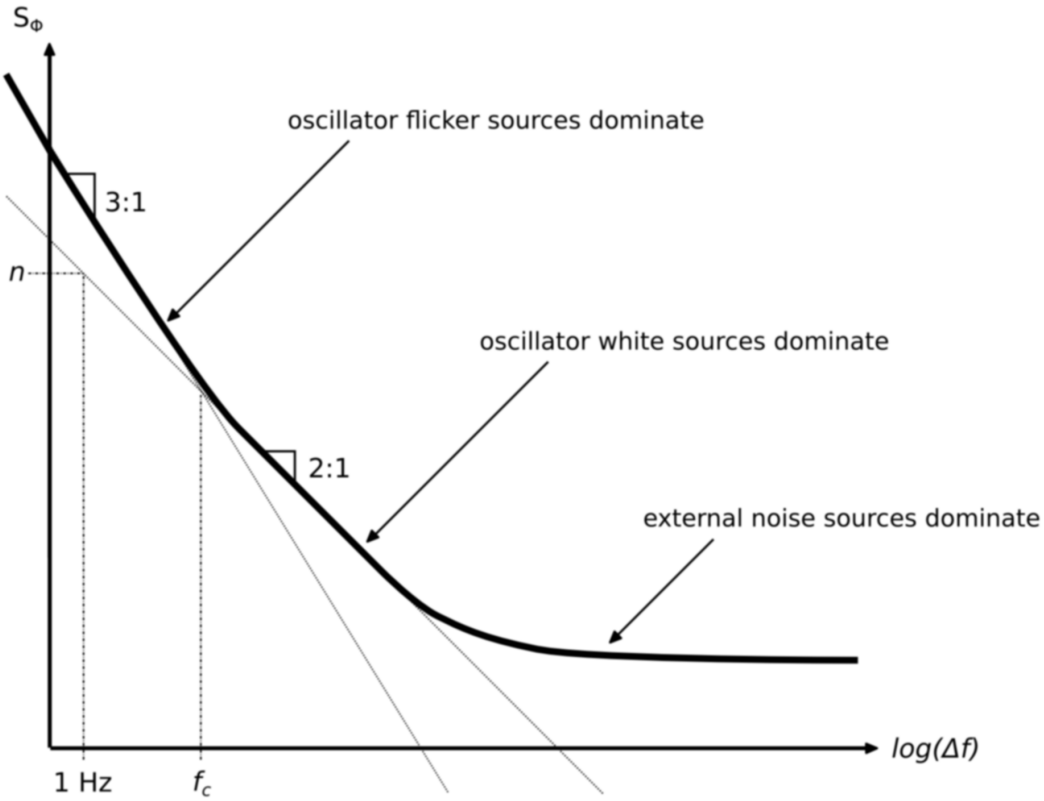


Figure H.2: Typical phase noise curve for an oscillator

$S\phi$ is not directly observable and often difficult to find. So instead oscillator phase noise is often characterized using L, the spot noise power of the output voltage S_v normalized by the power in the fundamental tone. S_v is directly available from either measurement with a spectrum analyzer

[1] A single-sided PSD has a domain of $0 \leq f < \infty$. The double-sided PSD is also commonly used and it has a domain of $-\infty < f < \infty$. They are related in that if S_{DS} and S_{SS} are the double- and single-sided PSDs of a signal, then $S_{DS}(0) = S_{SS}(0)$ and $S_{DS}(f) = \frac{1}{2}S_{SS}(f)$ for $f \neq 0$.

or from RF simulators, and L is defined as:

$$L(\Delta f) = \frac{2}{a_1^2 + b_1^2} S_v(f_0 + \Delta f) \tag{H.6}$$

where S_v is the single-sided PSD normalized to $1\,V$ RMS and a_1 and b_1 are the Fourier coefficients for the fundamental frequency components of v, the noise-free output signal. They satisfy:

$$v(t) = \sum_{k=0}^{\infty} a_k \cos(2\pi k f_0 t) + b_k \sin(2\pi k f_0 t) \tag{H.7}$$

For a free-running oscillator perturbed only by white noise sources:

$$L(\Delta f) = \frac{c f_0^2}{c^2 f_0^4 \pi^2 + \Delta f^2} = \frac{c f_0^2}{f_\Delta^2 + \Delta f^2} \tag{H.8}$$

which is a Lorentzian process with corner frequency of:

$$f_\Delta = c f_0^2 \pi \tag{H.9}$$

The corner frequency is also known as the linewidth of the oscillator. At frequencies well above f_Δ and well below f_0,

$$L(\Delta f) = \frac{c f_0^2}{\Delta f^2} \tag{H.10}$$

Over this same range of frequencies:

$$L(\Delta f) = \frac{1}{2} S\phi(\Delta f) \tag{H.11}$$

The empirical constants c and n are related by using this equation to combine () and:

$$\frac{c f_0^2}{\Delta f^2} = \frac{n}{2} \cdot \left(\frac{1}{\Delta f^2} + \frac{f_c}{\Delta f^3} \right) \tag{H.12}$$

This equation is valid only for $\Delta f \gg f_c$, and so the flicker noise term can be ignored, giving:

$$n = 2 c f_0^2 \tag{H.13}$$

The parameters n, or alternatively c, and f_c are used to describe the noise behavior of an oscillator. To extract these parameters, start by measuring either L or $S\phi$ for a range of frequencies offset from the center frequency. If flicker noise is present, there will be a range of low frequencies for which the noise power drops at a rate of $30\,dB$ per decade. Above this, the rate of drop will be $20\,dB$ per decade. As shown in Figure H.2, the frequency at which the rate switches from $30\,dB$ to $20\,dB$ per decade is f_c. Choose a frequency Δf well above f_c in the region where the noise is dropping at a rate of $20\,dB$ per decade and use either (H.5) or (H.10) and (H.13) to determine n.

H.3 Timing Jitter

The signal at the output of a CCO is a binary signal. The noise on binary signals is commonly characterized in terms of jitter. Jitter is an undesired perturbation or uncertainty in the timing of events. Generally, the events of interest are the transitions in a signal. Time jitter is a key measurement in systems where the periodic behavior or exact event timing is crucial to system performance. The design process requires comprehensive methods for modeling and analyzing both jitter and noise. There are two major approaches to modelling jitter:

- Model jitter as the continuous analog output signal of an autonomous system such as a voltage controlled oscillator (VCO)
- Use an edge-sensitive thresholding circuit to observe and sample the output signal. This approach is primarily used for driven circuits.

One models jitter in a signal by starting with a noise-free signal v and displacing time with a stochastic process j. The noisy signal becomes:

$$v_n(t) = v\left(t + j(t)\right) \tag{H.14}$$

with j assumed to be a zero-mean process and v assumed to be a T-periodic function. j has units of seconds and can be interpreted as a noise in time. Alternatively, it can be reformulated as a noise is phase, or phase noise, using $\phi(t) = 2\pi f_0 j(t)$, where $f_0 = 1/T$ and:

$$v_n(t) = v\left(t + \frac{\phi(t)}{2\pi f_0}\right) \tag{H.15}$$

As you can see, phase noise leads to jitter. One definition of phase noise demonstrates its connection to jitter, "phase noise is rapid, short-term, random fluctuations in the phase of a wave, caused by time domain instabilities".

H.3.1 Jitter Metrics

Define $\{t_i\}$ as the sequence of times for positive-going threshold crossings, henceforth referred to as transitions, that occur in v_n. Various jitter metrics characterize the statistics of this sequence:

- The simplest metric is the *edge-to-edge jitter*, J_{ee}, which is the variation in the delay between

a triggering event and a response event. When measuring edge-to-edge jitter, a clean jitter-free input is assumed, and so the edge-to-edge RMS jitter J_{ee} is:

$$J_{ee} = \sqrt{var(t_i)} \tag{H.16}$$

When a periodic system has a reference time point, you can consider all other events in relation to that time point. For a driven system, such an event can occur when the periodic input signal crosses through a particular threshold value. The periodic output signal generates an ideal sequence of events in response to the input signal, separated by the period T of the system. Ideally the delay from the input edge to the output edge is a constant t_{delay}. This sequence of same direction threshold crossings by the output signal expects periodic threshold crossings at times $\{iT + t_{delay}\}$ where the events are indexed with i.

$$v\left((i+1)\cdot T + t_{delay}\right) = v(iT + t_{delay}) = v\left(iT + t_{delay}\right) = v(iT + t_{delay}) = v_{threshold} \tag{H.17}$$

The actual transition times $\{t_i\}$ of the noisy signal will vary from the expected time as:

$$v_n(t_i) = v\left(iT + t_{delay} + j(t_i)\right) = v_{threshold} \tag{H.18}$$

The uncertainty is represented by the sequence:

$$\{\delta t_i\} = \{\delta t_i - (iT + t_{delay})\} \tag{H.19}$$

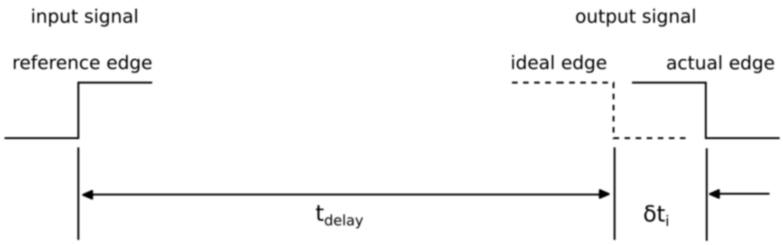


Figure H.3: Edge-to-edge jitter

This variation in the delay between a triggering event and a response event is the *edge-to-edge timing jitter* as shown in Figure H.3. It is also called *absolute* or *aperture jitter*. The presence of a noise free input signal implies that the edge-to-edge jitter metric can only apply for driven systems.

- The cycle or period between two similar output signal transitions is affected by the noise on both edges. The variation in the length of the period from the ideal value (as expressed in Equation (H.20)), is characterized by the standard deviation also known as the *period jitter*[2] or *cycle jitter*, see Figure H.4 and Equation (H.21).

$$J_c^i = \{\delta t_{i+1} - t_i - T\} \tag{H.20}$$

$$J_c^i = \sqrt{var\,(t_{i+1} - t_i)} \tag{H.21}$$

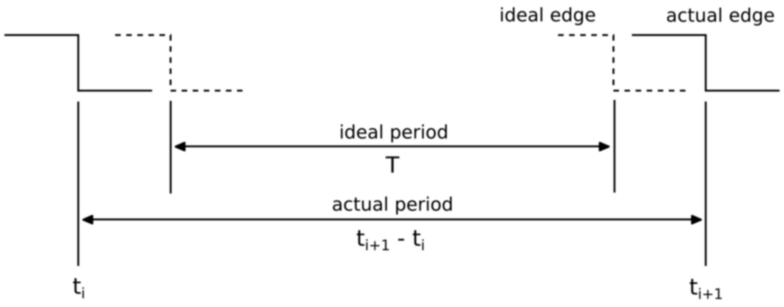


Figure H.4: Period jitter

This metric characterizes the correlations between transitions as a function of how far the transitions are separated in time. If two transitions are separated in time by k cycles or periods, as shown in Figure H.5, the standard deviation of the length of k cycles from nominal is computed using the following sequence.

$$\left\{J_c^i(kT)\right\} = \{t_{i+k} - t_i - kT\} \tag{H.22}$$

It is designated as *long term jitter* or *k-cycle jitter*[3] computed. It is a measure of the uncertainty in the length of k cycles and has units of time. Define $J_c^i(kT)$ to be the standard deviation of $t_{i+k} - t_i$:

$$J_c^i(kT) = \sqrt{var\,(t_{i+k} - t_i)} \tag{H.23}$$

- Another important jitter metric is *cycle-to-cycle jitter*, and is produced by the second difference of *absolute jitter*, as shown in Figure H.6. Define $T_i = t_{i+1} - t_i$ to be the period of

[2] J_c^1, the standard deviation of the length of a single period, is often referred to as the *period jitter*, and it denoted J_c, where $J_c = J_c^1$.

[3] Some people distinguish between k-cycle jitter and long-term jitter by defining the long-term jitter J_∞ as being the k-cycle jitter J_k as $k \to \infty$

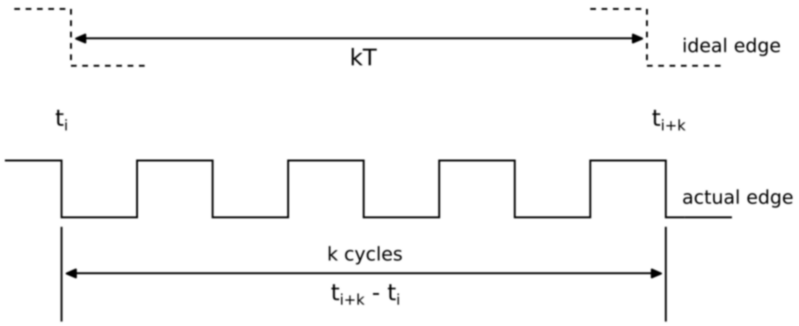


Figure H.5: k-cycle jitter

cycle k. Then the cycle-to-cycle jitter J_{cc} is:

$$\left\{J_{cc}^{i}\right\} = \{(T_{i+1} - T_i)\} = \{(t_{i+2} - t_{i+1}) - (t_{i+1} - t_i)\} \tag{H.24}$$

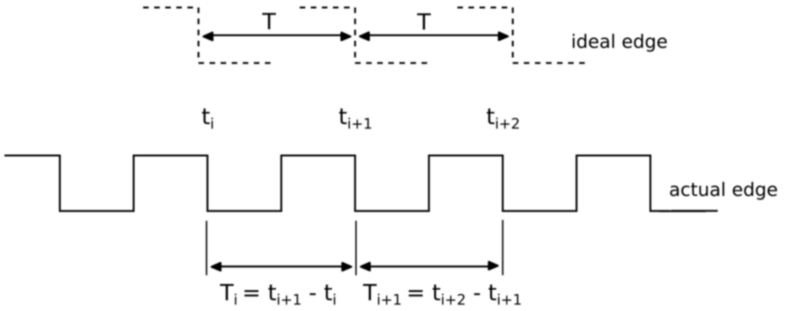


Figure H.6: Cycle-to-cycle jitter or adjacent period jitter

Also called *adjacent period jitter*, it characterizes the local change in the period as Figure H.6 illustrates cycle-to-cycle jitter or adjacent period jitter.

$$J_{cc}^{i} = \sqrt{var\left(T_{i+1} - T_i\right)} = \sqrt{var\left((t_{i+2} - t_{i+1}) - (t_{i+1} - t_i)\right)} \tag{H.25}$$

In the more general case of k cycles adjacent to another k cycles the metric is the sequence:

$$\left\{J_{cc}^{i}(kT)\right\} = \{(T_{i+k} - T_i)\} = \{(t_{i+2k} - t_{i+k}) - (t_{i+k} - t_i)\} \tag{H.26}$$

The standard deviation of the length of k adjacent periods is a long term jitter called either *k-long cycle-to-cycle jitter* or *k-long adjacent period jitter* as:

$$J_{cc}^{i}(kT) = \sqrt{var\left(T_{i+k} - T_i\right)} = \sqrt{var\left((t_{i+2k} - t_{i+k}) - (t_{i+k} - t_i)\right)} \tag{H.27}$$

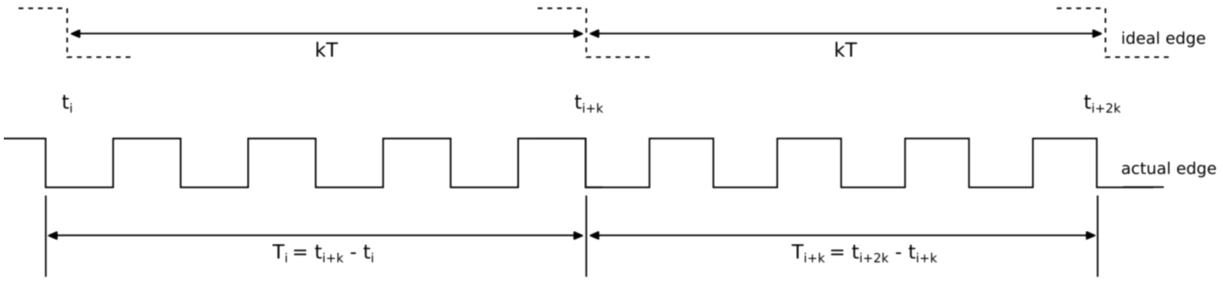


Figure H.7: k-long cycle-to-cycle Jitter

Cycle-to-cycle jitter is a metric designed to identify large adjacent cycle displacements. It is like edge-to-edge jitter in that it is a scalar jitter metric that does not contain information about the correlation in the jitter between distant transitions. However, it differs in that it is a measure of short-term jitter that is relatively insensitive to long-term jitter. As such, cycle-to-cycle jitter is the only jitter metric that is suitable for use when flicker noise is present. All other metrics are unbounded in the presence of flicker noise.

Edge-to-edge jitter assumes an input signal, and so is only defined for driven systems. It is an *input-referred* jitter metric, meaning that the jitter measurement is referenced to a point on a noise-free input signal, so the reference point is fixed. No such signal exists in autonomous systems. The remaining jitter metrics are suitable for both driven and autonomous systems. They gain this generality by being *self-referred*, meaning that the reference point is on the noisy signal for which the jitter is being measured. These metrics tend to be a bit more complicated because the reference point is noisy, which acts to increase the measured jitter.

If $j(t)$ is either stationary or T-cyclostationary, then the sequence $\{t_i\}$ is stationary, meaning that these metrics do not vary with k, and so $J_{ee}(kT)$, $J_c(kT)$, and $J_{cc}(kT)$ can be shortened to J_{ee}, J_c, and J_{cc}.

H.3.2 RMS versus Peak-to-Peak Jitter

All the jitter metrics given so far are typically characterized in terms of root mean squared average (or RMS). It is a natural way to represent the unbounded probability distribution function of a random process. In order to combine or analyze the random jitter with deterministic jitter, which is bounded, there is a way to convert RMS into the peak-to-peak bound under certain conditions.

Notation	Definition
J_{ee}	Edge-to-Edge Jitter
J_c	Cycle Jitter
J_{cc}	Cycle-to-Cycle Jitter
$J_c(k)$	k-Cycle Jitter
$J_{cc}(k)$	k-long Cycle-to-Cycle Jitter

Table H.1: Simplified jitter notations.

If you assume that the noise sources have Gaussian distributions, then strictly speaking the metrics do not have peak-to-peak values because the noise is unbounded. However, one can define the peak-to-peak jitter as the magnitude that the jitter exceeds only a for specified fraction of the time. Assuming that only a finite amount of error is allowed, you can find the value of jitter, beyond which, the error will be less probable than the established limit. A bit error rate (BER) is such a limit. For a Gaussian distribution of the jitter, you can find the scaling factor to convert RMS to the peak-to-peak range. SpectreRF uses a table which has the scaling factor α for the most typical values of BER, that are listed in Table H.2, which is the ratio between the peak-to-peak deviation and the standard deviation. Then the RMS jitter can be converted to peak-to-peak jitter using:

$$J_{PP} = \alpha J_{RMS} \tag{H.28}$$

H.3.3 Long Term Jitter

Long term jitter is of limited use because of the limitation of small signal analyses we use. The variations that SpectreRF models cannot grow large enough to break important assumptions about the validity of small signal approximation. Large low frequency noise components that lead to large long term jitter break the assumption that the noisy curve is smooth on transition. If operating point is affected by the noise, the slew rate of the jitter free signal can not be used to approximate long term jitter.

H.3.4 Jitter Units in SpectreRF

Measuring timing jitter involves several basic units. The default unit is seconds. Absolute units such as seconds are not always optimal. Using absolute units, you cannot see the effect of the

Error Rate	α
10^{-3}	6.180
10^{-4}	7.438
10^{-5}	8.530
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069
10^{-13}	14.698
10^{-14}	15.301
10^{-15}	15.883
10^{-16}	16.444

Table H.2: The ratio of the peak-to-peak deviation of a Gaussian process to its standard deviation where the peak-to-peak deviation is defined as the magnitude that is not exceeded more often than the given error rate.

jitter on the system period or on other timing properties. Relative units such as parts per million (PPM) and the unit interval (UI), UI can be the clock period or another characteristic time cycle.

H.3.5 Types of Jitter

Circuits that are driven by externally generated periodic signals or clocks, exhibit *synchronous jitter*. In this case you can measure the absolute jitter, since the reference input edge exists in the system. The name edge-to-edge jitter is reserved for the input referred jitter in such systems. In these components, an output event occurs as a direct result of, and some time after, an input event. It is an undesired fluctuation in the delay between the input and the output events. If the input is a periodic sequence of transitions, then the frequency of the output signal is exactly that of the input, but the phase of the output signal fluctuates with respect to that of the input. The jitter appears as a modulation of the phase of the output, which is why it is sometimes referred to as phase modulated or PM jitter.

The measurement is between the ideal input signal and the noisy output signal. The cycle (or period) jitter and the cycle-to-cycle (or adjacent period) jitter are also measured for driven systems, but they are different in the sense that the measurement starts and ends with a noisy output signal.

But even in this situation, both transitions are the direct result of a transition by the ideal periodic input signal.

For autonomous circuits, such as oscillators, that generate a stream of spontaneous output transitions and where there are no ideal reference transitions, you are limited to using self-referred jitter metrics. This jitter is *accumulating jitter*. The next cycle transition is the result of the previous cycle output, so the jitter variance accumulates from cycle-to-cycle. Accumulating jitter is characterized by an undesired variation in the time since the previous output transition, thus the uncertainty of when a transition occurs accumulates with every transition. Compared with a jitter free signal, the frequency of a signal exhibiting accumulating jitter fluctuates randomly, and the phase drifts without bound. Thus, the jitter appears as a modulation of the frequency of the output, which is why it is sometimes referred to as frequency modulated or FM jitter. Again assume that η be a stationary or T-cyclostationary process, then:

$$v_n(t) = v\left(t + j_{acc}(t)\right) \qquad \text{where} \qquad j_{acc}(t) = \int_0^t \eta(\tau)\, d\tau \tag{H.29}$$

exhibits accumulating jitter. While η is cyclostationary and so has bounded variance, () shows that the variance of j_{acc}, and hence the phase difference between $v(t)$ and $v_n(t)$, is unbounded. If η is further restricted to be a white Gaussian stationary or T-cyclostationary random process, then v_n exhibits simple accumulating jitter. In this case, the process $\{j_{acc}(kT)\}$ that results from sampling j_{acc} every T seconds is a discrete Wiener process and the phase difference between $v(kT)$ and $v_n(kT)$ is a random walk.

The essential characteristic of simple accumulating jitter is that the incremental jitter that accumulates over each cycle is independent or uncorrelated. Autonomous circuits exhibit simple accumulating jitter if they are broadband and if the noise sources are white, Gaussian and small. The sources are considered small if the circuit responds linearly to the noise, though at the same time the circuit may be responding nonlinearly to the oscillation signal. An autonomous circuit is considered broadband if there are no secondary resonant responses close in frequency to the primary resonance. For systems that exhibit simple accumulating jitter, each transition is relative to the previous transition, and the variation in the length of each period is independent, so the variance in the time of each transition accumulates:

$$J_c(kT) = \sqrt{k} \cdot J_c \tag{H.30}$$

Similarly:

$$J_{cc} = \sqrt{2} \cdot J_c \tag{H.31}$$

Generally, the jitter produced by oscillators are well approximated by simple accumulating jitter if one can neglect flicker noise.

H.3.6 Extracting Accumulating Jitter

The jitter in autonomous blocks, is almost completely due to oscillator phase noise. Oscillator phase noise is a variation in the phase of the oscillator as it proceeds along its limit cycle. In order to determine the period jitter J of $v_n(t)$ for a noisy oscillator, assume that it exhibits simple accumulating jitter so that η in () is a white Gaussian T-cyclostationary noise process (this excludes flicker noise) with a single-sided PSD of:

$$S_\eta(f) = 2c \tag{H.32}$$

and an autocorrelation function of:

$$R_\eta(t_1, t_2) = c\delta(t_1 - t_2) \tag{H.33}$$

where δ is a Dirac delta function. Then $j_{acc}(t) = \int_0^t \eta_T(\tau)\, d\tau$ is a Wiener process, which has an autocorrelation function of:

$$R_{j_{acc}}(t_1, t_2) = c \cdot \min(t_1, t_2) \tag{H.34}$$

The period jitter is the standard deviation of the variation in one period, and so:

$$J_c = \sqrt{var\left(j_{acc}(t+T) - j_{acc}(t)\right)} = \sqrt{E\left[\left(j_{acc}(t+T) - j_{acc}(t)\right)^2\right]} = \sqrt{cT} = \sqrt{\frac{c}{f_0}} \tag{H.35}$$

The procedure to compute the jitter of an oscillator, starts by using an RF simulator such as SpectreRF to compute the fondamental oscillator frequency f_0 and the normalized phase noise L. Its PNoise analysis is used, with the maxsideband parameter set to at least 10 to adequately account for noise folding within the oscillator. The c value can be derived from L applying ():

$$c = L(\Delta f)\frac{\Delta f^2}{f_0^2} \tag{H.36}$$

The period jitter J_c is then computed from () and $J_c(kT)$ is found with ().

H.3.7 Jitter Computation

The synchronous jitter for driven systems is measured using strobed periodic noise simulation in SpectreRF. The slew rate is also automatically computed at the requested threshold crossing events. The final results are presented using the Direct Plot form. The entire simulation is executed in one run as long as you know the values of the threshold and outputs of the system. The accumulating jitter is computed using phase noise measured by SpectreRF.

Both strobed noise and phase noise measurements in SpectreRF produce the power spectral density (PSD) of the random noise which can be converted to the RMS value of random jitter. In the case of synchronous jitter, the slew rate is used to convert the strobed noise PSD into absolute time jitter PSD.

The cycle jitter and the cycle-to-cycle jitter metrics are computed from the spectral density of the absolute jitter using:

$$J_c^2(kT) = 4\int_{f_{lower}}^{f_{upper}} S_j(f) \cdot sin^2(\pi k f T) df \tag{H.37}$$

$$J_{cc}^2(kT) = 16\int_{f_{lower}}^{f_{upper}} S_j(f) \cdot sin^4(\pi k f T) df \tag{H.38}$$

These equations use phase noise and its relationship with the time jitter which follows from Equations () and ().

$$S_j(f) = \frac{S_\phi(f)}{(2\pi f_0)^2} \tag{H.39}$$

H.3.8 Measurements Testbench

To measure the jitter for the autonomous circuit above we will setup PSS and PNoise analyses. The PSS analysis is a regular autonomous simulation. First, we use periodic steady state analysis to find the periodic trajectory or the large signal periodic solution of the system. Next, we use periodic noise analysis to find the phase noise and provide all the information we need to extract the jitter.

Only if the M divider is attached as the load, PSS will use the divider output to find the period of the large signal solution. The PSS fundamental will be M times smaller then CCO output frequency. The PNoise analysis form is used to setup the Jitter measurements. The output is the output of the CCO.

A relative log sweep is recommended for optimal computation. The sweep limits should include the lowest offset frequency of the interest, but one has to realize that at the frequencies close to the LO the small signal approximation will break down and the information at those frequencies is not valid. That depends on the Q of the oscillator and on the presence of the flicker noise. Another factor could be the bandwidth of the circuit itself. The highest limit is usually on the order of $f_{LO}/2$ to f_{LO} since we are only interested in the phase noise around the output harmonic. This will be less accurate for low Q oscillators, when noise tail will extend far beyond $f_{LO}/2$ - part of the noise will not be accounted for in the computations. The bandwidth of the circuit will often be the factor here too. More frequency points are always helpful to increase an accuracy of the jitter computations, you will have to trade off the frequency range, number of point per decade and the maximum sidebands that will be used for folding in PNoise.

The Pnoise output will be used to compute the jitter. Since we are using the phase noise to calculate the jitter, the netlist will have two pnoise analyses in it. They are required to find upper and lower sidebands and their cross correlation in order to separate the total PNoise results into the PM and AM components, just like in modulated PNoise analysis type.

The Phase Noise Measurements

It is helpful to plot phase noise prior to beginning jitter measurements. It lets one determine the appropriate frequency range, and to decide which integration limits to use. Since at lower frequency offsets, the phase noise will grow boundless, it could be confusing at first how to decide on the lower limit of integration. But more careful examination of the meaning of the low frequency contribution to noise tells us that it can only contribute over the very long observation period and will not affect the jitter over reasonable period of time.

Another helpful feature is the $-20\,dB/dec$ curve which could be placed on the phase noise plot at any frequency. The slope of $-20\,dB/dec$ assistant let us to distinguish the regions of the $1/f^3$, $1/f^2$ and $1/f$ phase noise PSD. If you prefer, the quick manual calculations using simple white noise jitter approximation could be used after the proper region of $1/f^2$ slope is determined. The white noise approximation was used in the first release of the jitter measurements. It required the user to select the point for the approximation of the slope. In the later releases of Direct Plot, the integration is numerical, and the selection of the point is not needed anymore. So, the slope assistant is for informative purposes only now. Since jitter is the scalar number, it will be placed

together with the phase noise curve on the same plot.

The Jitter Measurements

Based on the specs requirements, the phase noise curve, the actual values and the slope, one can decide on the limits of the integration to use. User will also select whether to compute period jitter or cycle to cycle jitter. The default units are in second, which could be changed. Number of cycles determines whether one period or k-periods jitter will be computed.

Jitter results confirm the fact the lower frequency have very small contribution to the short term jitter. RMS jitter is typically used, but another option is the peak to peak measurement, which could be done for particular Beat Error Rate. You could also plot Peak to Peak jitter from the same form. Please note that it is only accurate under the assumptions of the Gaussian random noise distribution. The presence of the flicker noise will make it less accurate.

Bibliography

[1] Marco Meola. *Thesis - Design And Modeling Of A Digital Controller For Multi-Mode DC-DC Converters.* Università degli Studi di Trieste, 2008-2009.

[2] J. Rice, D. Gehrke, M. Segal. *Undestanding noise-spreading techniques and their effects in switched mode power applications.*

[3] K. K. Tse, H. Shu-Hung Chung, S. Y. (Ron) Hui, H. C. So. *Analysis and Spectral Characteristics of a Spread-Spectrum Technique for Conducted EMI Suppression.* IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 15, NO. 2, MARCH 2000.

[4] S. Mohseni, A. Roomizadeh. *Study on Periodic and non Periodic Frequency Modulation Techniques for EMI Suppression in SMPS.* 2011 2nd Power Electronics, Drive Systems and Technologies Conference.

[5] A. Knitter, J. Luszcz, P. J. Chrzan. *Conducted EMI mitigation in switched mode DC-DC converters by spread spectrum techniques.* Electrical Power Quality and Utilisation, Journal Vol.XI, No.2, 2005.

[6] K. K. Tse, H. S. H. Chung, S. Y. Ron Hui and H. C. So. *A Comparative Study of Carrier-Frequency Modulation Techniques for Conducted EMI Suppression in PWM Converters.* IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 3, JUNE 2002.

[7] A. Aurasopon, and W. Sangiavibool. *Synchronization Technique for Random Switching Frequency Pulse-Width Modulation.* World Academy of Science, Engineering and Technology 39 2008.

[8] R. Mukherjee, S. Nandi, and S. Banerjee. *Reduction in Spectral Peaks of DC-DC Converters using Chaos-Modulated Clock.* IEEE.

[9] R. Mukherjee, A. Patra and S. Banerjee. *Chaos-modulated ramp IC for EMI reduction in PWM buck converters design and analysis of critical issues.* Department of Electrical Engineering Indian Institute of Technology, Kharagpur, India.

[10] Hong Li , Trillion Q. Zheng , Zhong Li, W. A. Halang. *A Novel Chaotic Carrier with Chaotic Oscillator Used in PWM Control for EMI Suppression.* International Symposium on Electromagnetic Compatibility, April 12 - 16, 2010, Beijing, China.

[11] A. Roomizadeh, S. Mohseni , M. Niroomand. *A Plug-in Chaos-based Controller for EMI Reduction in Switching Converters.* Department of Engineering and Technology, University of Isfahan (U.I.) Iran.

[12] Edward N. Y. Ho and Philip K. T. Mok. *Ramp Signal Generation in Voltage Mode CCM Random Switching Frequency Buck Converter for Conductive EMI Reduction.* IEEE.

[13] Y. Chen, D. LaPorte, R. G. Flatness, R. C. Dopkin. *Methods and Circuits For Frequency Modulation That Reduce The Spectral Noise Of Switching Regulator.* Patent: 2005/0243894.

[14] K. B. Hardin, R. A. Ogleesbee. *Segmented spectrum clock generator apparatus and method for using same.* Patent: 6,404,834. Assignee: Lexmark International, Inc.

[15] K. B. Hardin, J. T. Fessler, D. R. Bush, J. J. Booth. *Spread Spectrum Clock Generator and Associated Methods.* Patent: 5,488,627. Assignee: Lexmark International, Inc.

[16] K. B. Hardin, J. T. Fessler and Donald R. Bush. *Digital Circuit Radiated Emission Suppression with Spread Spectrum Techniques.* Interference Technology Engineers Master (ITEM) 1994.

[17] Dr. G. Winkler, Dr. Bernd Deutschmann. *Einsatz von Spread Spectrum zur Verringerung elektromagnetischer Storemissionen.* TU Graz & Infineon Technologies AG.

[18] M. Rahkala, T. Suntio and K. Kalliomäki. *Effects of Switching Frequency Modulation on EMI Performance of a Converter Using Spread Spectrum Approach.* IEEE.

[19] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez and J. Gago. *EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques.* IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO. 3, AUGUST 2005.

[20] J. Mon, J. Gago, D. Gonzalez, J. Balcells, R. Fernandez, I. Gil. *Thesis - Reduction of EMI by combining interleaving and modulation techniques in multiconverter topology.* Universitat Politecnica de Catalunya.

[21] A. Nasiri. *Thesis - Different Topologies of Active EMI/Ripple Filters for Automotive DC/DC Converters.* Power Electronics and Motor Drives Laboratory University of Wisconsin-Milwaukee.

[22] Q. Zhaoming, W. X. L. Zhengyu, M. H. Pong *Status of Electromagnetic Compatibility Research in Power Electronics.* IEEE.

[23] K. Mainali, and R. Oruganti. *Conducted EMI Mitigation Techniques for Switch-Mode Power Converters: A Survey.* IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 25, NO. 9, SEPTEMBER 2010.

[24] INTERNATIONAL STANDARD - *IEC 61967-4/A1/Ed 1 - 47A/735/FDIS (FINAL DRAFT INTERNATIONAL STANDARD). Amendment 1 to IEC 61967-4: Integrated circuits - Measurement of electromagnetic emission, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions 1 Ohm/150 Ohm direct coupling method*

[25] INTERNATIONAL STANDARD - *COMITÉ INTERNATIONAL SPÉCIAL DES PERTURBATIONS RADIOÉLECTRIQUES: IEC CISPR 25 Edition 3.0 2008-03*

[26] Patrice Besse. *ESD/EMC in an automotive environment.* Seminar at IEW 2010, Freescale Semiconductor.

[27] Gustav Johannesson, Niklas Fransson. *Thesis - EMI measurements and modeling of a DC-DC Buck converter.* Master Thesis in Electrical Engineering, Chalmers University of Technology. Carried out at VOLVO CARS AB.

[28] Feng Zhang. *Thesis - Investigation of Electromagnetic Interference of PWM Motor Drives in Automotive Electrical Systems.* MIT/Industry Consortium on Advanced Automotive Electrical/Electronic Components and Systems. LEES Technical Report TR-99-004 December 8, 1999.

[29] Sabine Marksell. *Thesis - EMC Aspects of PWM Controlled Loads in Vehicles.* Lund University, 2004.

[30] Sabine Alexandersson *Automotive Electromagnetic Compatibility, Prediction and Analysis of Parasitic Components in Conductor Layouts.* Doctoral Dissertation in Industrial Electrical Engineering, Lund University, 2008.

[31] I-The Sha, Albert Chen, Kuang-Yu, and Jeffry Keip. *Spread spectrum and PLL technology combine to reduce EMI.* April 2000.

[32] Hsiang-Hui Chang,I-Hui Hua, and Shen-Iuan Liu. *A Spread-Spectrum Clock Generator With Triangular Modulation.* IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 4, APRIL 2003.

[33] Ming-ta Hsieh, Jim Welch, Gerald E. Sobelman. *PLL performance comparison with application to spread spectrum clock generator design.* Analog Integr Circ Sig Process (2010).

[34] Maxim Integrated Products. *Automotive Applications for Silicon Spread-Spectrum Oscillators.* Application Note 3512, Jun 08, 2005.

[35] M. Kuisma. *Variable Frequency Switching in Power Supply EMI-Control: An Overview.* Lappeenranta University of Technology. IEEE AES System Magazine, December 2003.

[36] D. GonzÃ¡lez, J. Balcells, A. Santolaria, J. Le Bunetel, J. Gago, D. Magnon, S. BrÃ©haut. *Conducted EMI Reduction in Power Converters by Means of Periodic Switching Frequency Modulation.* IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 22, NO. 6, NOVEMBER 2007.

[37] D. GonzÃ¡lez, J. Balcells, A. Santolaria, A. Orlandi, J. Gago. *EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques.* IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO. 3, AUGUST 2005.

[38] K. K. Tse, H. S. Chung, S. Y. Ron Hui, H. C. So. *A Comparative Study of Carrier-Frequency Modulation Techniques for Conducted EMI Suppression in PWM Converters.* IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 3, JUNE 2002.

[39] Feng Lin, Dan Y. Chen. *Reduction of Power Supply EM1 Emission by Switching Frequency Modulation.* IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 9, NO. I, JANUARY 1994.

[40] M. Vilathgamuwa, J. Deng, K. J. Tseng. *EMI suppression with Switching Frequency Modulated DC-DC Converters.* IEEE Industry Applications Magazine, November/December 1999.

[41] Ken Kundert. *Predicting the Phase Noise and Jitter of PLL-Based Frequency Synthesizers.* The Designer's Guide Community.

[42] T. C. Neugebauer and D. J. Perreault. *Parasitic capacitance cancellation in filter inductors.* IEEE Trans. Power Electron., vol. 21, no. 1, pp. 282-288, Jan. 2006.

[43] L. E. LaWhite and M. F. Schlecht. *Active filters for 1 MHz power circuits with strict input/output ripple requirements.* IEEE Power Electron. Spec. Conf., 1986, pp. 255-263.

[44] N. K. Poon, J. C. P. Liu, C. K. Tse, and M. H. Pong. *Techniques for input ripple current cancellation: Classification and implementation.* IEEE Trans. Power Electron., vol. 15, no. 6, pp. 1144-1152, Nov. 2000.

[45] T. Farkas and M. F. Schlecht. *Viability of active EMI filters for utility applications.* IEEE Trans. Power Electron., vol. 9, no. 3, pp. 328-337, May 1994.

[46] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar. *Passive and active hybrid integrated EMI filters.* IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1340-1349, May 2009.

[47] D. C. Hamill and P. T. Krein. *A "zero" ripple technique applicable to any DC converter.* IEEE Power Electron. Spec. Conf., 1999, pp. 1165-1171.

[48] M. Shoyama, G. Li, and T. Ninomiya. *Balanced switching converter to reduce common-mode conducted noise.* IEEE Trans. Ind. Electron., vol. 50, no. 6, pp. 1095-1099, Dec. 2003.

[49] A. J. Sinclair, J. A. Ferreira, and J. D. Van Wyk. *A systematic study of EMI reduction by physical converter layout and suppressive circuits.* Proc. Int. Conf. on Ind. Electron., Control, Instrum., 1993, pp. 1059-1064.

[50] L. Rossetto, S. Buso, and G. Spiazzi. *Conducted EMI issues in a 600-W single-phase boost PFC design.* IEEE Trans. Ind. Appl., vol. 36, no. 2, pp. 578585, Mar./Apr. 2000.

[51] H. W. Whittington. *Switched Mode Power Supplies: Design and Construction.* New York: Wiley, 1996.

[52] A. Consoli, S. Musumeci, G. Oriti, and A. Testa. *An innovative EMI reduction design technique in power converters.* IEEE Trans. Electromagn. Compat., vol. 38, no. 4, pp. 567-575, Nov. 1996.

[53] D. Zhang, D. Y. Chen, and F. C. Lee. *An experimental comparison of conducted EMI emissions between a zero-voltage transition circuit and a hard switching circuit.* IEEE Power Electron. Spec. Conf., 1996, pp. 1992-1997.

[54] P. Caldeira, R. Liu, D. Dalal, and W. J. Gu. *Comparison of EMI performance of PWM and resonant power converters.* IEEE Power Electron. Spec. Conf., 1993, pp. 134-140.

[55] R. Mukherjee, A. Patra, and S. Banerjee. *Chaos-modulated ramp IC for EMI reduction in PWM buck converters design and analysis of critical issues.* Int. Conf. VLSI Design, 2008, pp. 305-310.

[56] J. Paramesh and A. von Jouanne. *Use of sigma-delta modulation to control EMI from switch-mode power supplies.* IEEE Trans. Ind. Electron., vol. 48, no. 1, pp. 111-117, Feb. 2001.

[57] D. E. Quevedo and G. C. Goodwin. *Control of EMI from switch-mode power supplies via multi-step optimization* Amer. Contr. Conf., 2004, pp. 390-395.

[58] D. A. Stone and B. Chambers. *Effect of spread-spectrum modulation of switched mode power converter PWM carrier frequencies on conducted EMI.* Electron. Lett., vol. 31, no. 10, pp. 769-770, May 1995.

[59] Y. F. Zhang, L.Yang, and C.Q. Lee. *EMI reduction of power supplies by bi-frequency modulation.* IEEE Appl. Power Electron. Conf., 1994, pp. 601-607.

[60] A. C. Wang and S. R. Sanders. *Programmed pulsewidth modulated waveforms for electromagnetic interference mitigation in DC-DC converters.* IEEE Trans. Power Electron., vol. 8, no. 4, pp. 596-605, Oct. 1993.