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Design of a Built-In Test Equipment for a X-band phased array radar system in SiGe BiCMOS technology

Relatore:
Prof. Andrea Bevilacqua
Correlatore:
Ing. Dr. Marc Tiebout

Candidato:
Calabrò Rocco

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Abstract

Phased Array systems are widely used in radar applications, where the reception and transmission of radio waves towards specific directions is needed. The precision of these systems, strongly depends on the ability to accurately control the gain and the phase of the signal transmitted and received by each element of the array. For this reason, a reliable method to a characterize the amplitude and the phase shift characteristic of the RX/TX front end is required. Performing a direct, high frequency measurement on a X band system requires instruments having large bandwidth, dedicated high frequency sockets which implies higher production costs and complexity and results in low reliability and reproducibility test conditions. Hence, the possibility to utilize an on-chip solution to reduce the test frequency by one octave, is very appealing from the production cost standpoint. In this work an X band ($8GHz - 12GHz$) Build In Test Equipment (BITE), implemented in the SiGe BiCMOS technology of Infineon, is presented. The possibility to perform precise measurements of phase shift and gain in the X- band, using lower frequency ($4GHz - 6GHz$) automated test equipment (ATE), which is also used in WLAN devices, is investigated leading to the design of the complete test equipment and finally to the full custom layout design.
The device under test (DUT) consist of a cascade of an LNA, a PGA and a phase shifter. X band input signal generation uses a frequency doubler. An

analog multiplier is used to halve the frequency of the DUT's output signal. The blocks that have been analyzed and designed are: a single stage Polyphase filter, which generates the quadrature signal needed by the frequency doubler, an up converting Mixer, which performs the frequency doubling task and a linear multiplier used to down convert the signal at the output of the DUT. Circuit simulations show that the accuracy requested for the BITE which consists in a maximum error in the relative phase measurement of 5^o and a maximum error in the relative gain measurement of 1dB, is robustly achievable with the proposed structure.

CHAPTER 1

Introduction

This chapter gives an introduction on phased-array radar systems explaining their basic operation. Advantages and the issues given by these systems are explored, focusing on the requirements of the test system, which is the subject of this work. Than, Infineon SiGe BiCMOS technology utilized in this work is introduced together with the structure of the BITE system, the required performances and a brief illustration on the Figure Of Merit that characterize the test system.

1.1 Radar systems

The subject of this work is the design of a build in test equipment (BITE) for a radar operating in the X band. It is useful then, to make a brief introduction on the functioning of radars, in order to understand why such a measurement system is needed. Radars are systems that use electromagnetic radiations in the radio waves frequencies, to detect the presence and characteristics of objects in the radar's operating range. There exists several types of radars, operating at different frequencies and using different scan strategies, but all of them share

the same principle of operation. What a radar does, is emitting pulsed or continuos, high power electromagnetic waves in the desired spatial direction, if an object is present, the waves are reflected back in a way that depends on the physical properties of the target. The reflected signal that reaches the receiver, is then processed to obtain the desired informations on the object, which can be: position, dimension and speed. The basic structure of a radar is shown in Fig.1.1. Starting from the baseband signal processing block, the signal that must be transmitted is up converted to radio frequencies and processed by the transmitter to increase its power and prepare it to be sent to the antenna. The signal propagates and when it reaches an obstacle, some of its power is radiated back to the receiving antenna, which is usually the same used for the transmission. The received signal, which has typically low power, is then amplified and down converted by the receiver to be finally sent back to the baseband signal processing block, where its properties are analyzed to obtain informations about the target.

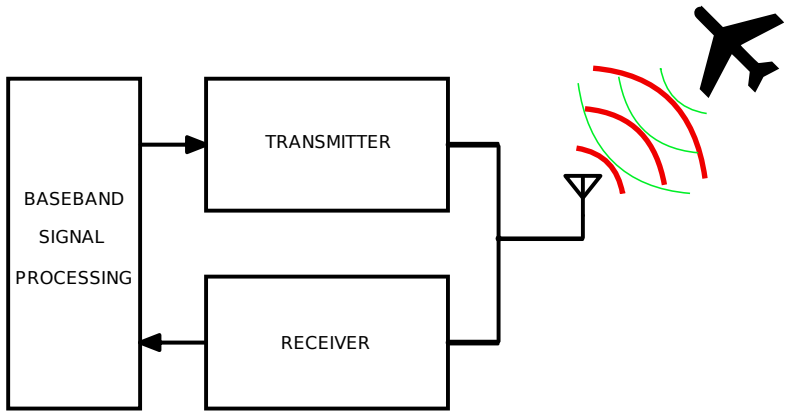

Figure 1.1: Basic structure of a radar system.

To enhance the radar's performance, the transmitted signal should be sent in a precise direction in order to discern which object caused the reflection, and the receiving antenna must have an adequate directivity (or gain), to maximize the power received in the wanted direction. An equation that summarizes the capability of a radar to transmit and receive a reflected signal is the radar

equation[1]:

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 r^4} \tag{1.1}$$

where P_r and P_t are the received and the transmitted powers respectively, G is the gain of the receiver and transmitter antenna which are typically the same, σ is the scattering coefficient of the target and r is the distance between the radar's antenna and the target. To achieve this goals, different types of antennas can be utilized. Some applications use directional antennas which are mechanically tilted to scan the wanted area and some other use multiple antennas in an arrangement called **phased array**.

1.2 Phased array systems

In radar applications, it is important to be able to send and receive electromagnetic waves in narrow and well defined directions. Some radars use directional antennas mounted on a mechanically steered fixture, which focalize the electromagnetic radiation in one specific direction thanks to the geometrical properties of the antenna itself. Other radars instead, use phased arrays, which are sets of antennas at a determined distances one from the other, which transmit and receive with different phase shifts in order to increase the directivity of the equivalent antenna, and null the electromagnetic field in the unwanted directions, thanks to constructive and destructive interference. A scheme which represents such a system is depicted in Fig.1.2.
We want to receive (transmit) a wave in a particular direction denoted by an angle ϕ respect to the array's axis. If the antennas are merely attached to the receiver, it is clear that each of them will receive (transmit) the incident (outgoing) waves with different time delays, due to the different length of the travelled path. In this case, it is easy to see that the incoming (outgoing) direction, in which the waves sum in phase is the one perpendicular to the array. If we want to steer the optimum propagation direction, we need an additional block for every element of the array i.e. a delay line, which introduces different delays at every element of the array. In this way, it is possible to adjust

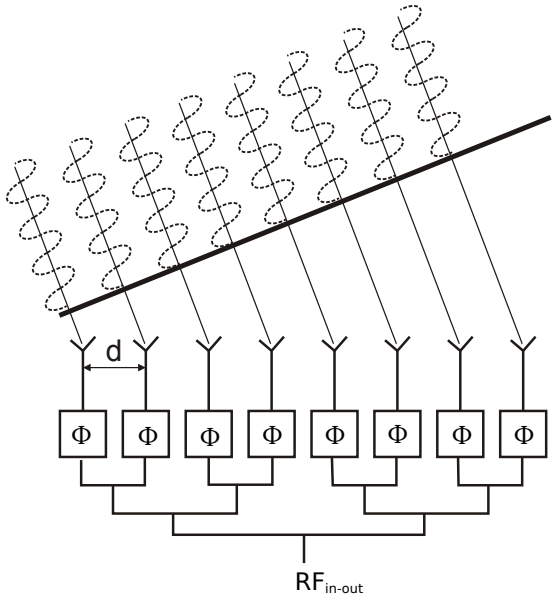

Figure 1.2: Scheme of a phased array system

the shape of the radiation pattern of the phased array making it pointing to the desired direction as shown in Fig.1.3, where an array of 8 equally spaced antennas is steered from 40^o to 140^0.

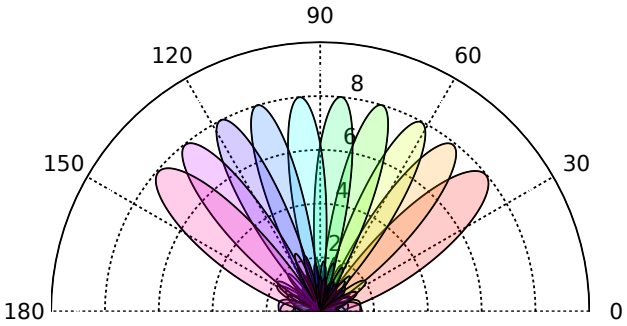

Figure 1.3: Beam steered from 40^o to 140^0

The technique just mentioned is called **analog beam steering** [3] and it is used in several applications in order to remove the necessity to mechanically steer the antenna since the phase shifts of every element can be digitally controlled to accomplish the same task in a faster way, without moving any physical part, hence making the system more robust. The actual configuration for every

element of the array, is shown in Fig.1.4. As we can see, the transmission and reception path of the signal, which share the same antenna, can be selected by means of a switch. A power amplifier (PA) is added in the transmitting path, in order to boost the signal before the transmission and a low noise amplifier (LNA) is added in the receiving part to amplify, introducing the least noise possible, the weak signal reflected by the target. In both the path a programmable gain amplifier (PGA) is used to equalize the loss introduced by the true time delay block.

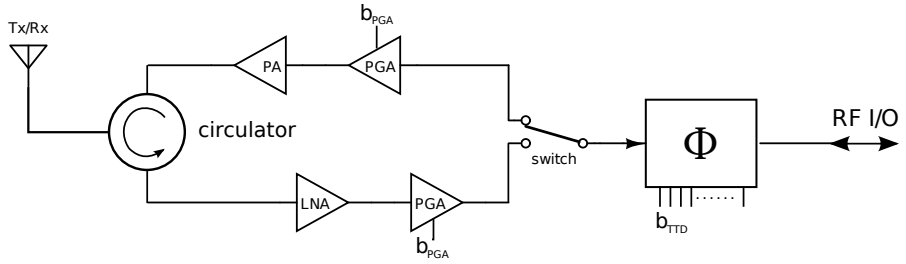

Figure 1.4: Scheme of an array element

It is clear that, if the time delays and the amplitude gains introduced at every element of the array are not precise, the radiation pattern will assume different shapes compared to the wanted one. For this reason, an efficient way to test the operation of every element of the array in the production process is needed. A representation of the error caused by a random 10% error on the phase and on the gain of every element, is shown in Fig.1.5.

1.3 BITE in phased arrays systems

Performing tests directly on the considered radar system, requires an off-chip test equipment, and sockets capable of working in the X band. This implies that non standard procedures and devices must be involved, increasing the production costs. For this reasons a BITE can be designed to relax the off-chip equipment requirements by halving the test frequency and to increase the

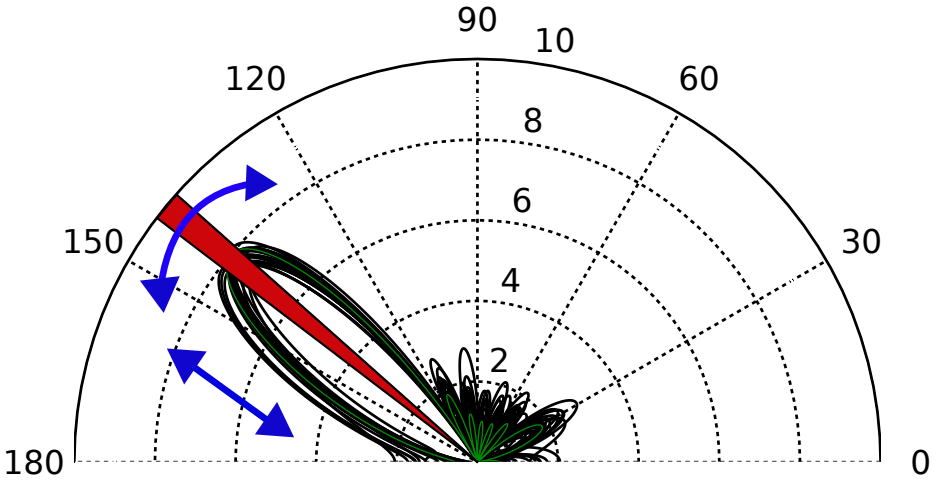

Figure 1.5: Phase and amplitude error representation

reliability and reproducibility of the tests. In Fig.1.6 a scheme of the BITE designed in this work is shown.

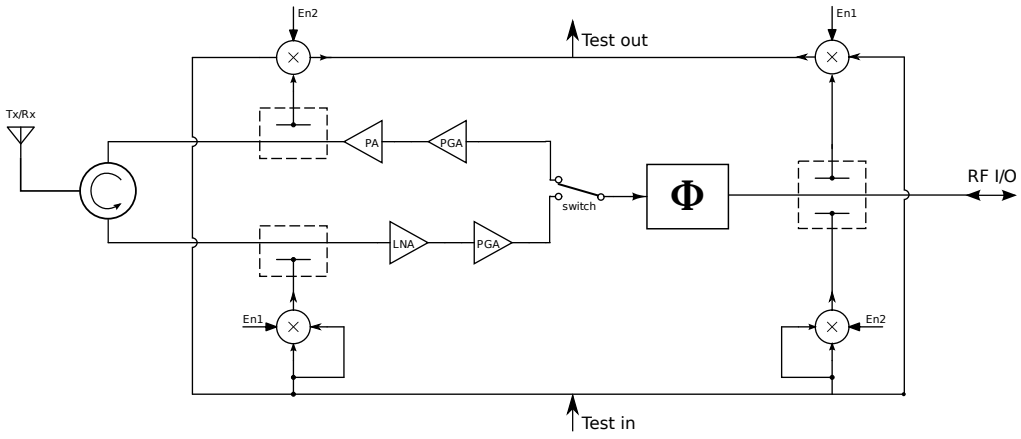

Figure 1.6: Scheme of an array element with the BITE

As we can see, the receiving and transmitting paths can be tested by switching on the proper mixers. Both the measurements operate in the same way. For example in the receiving path, the input test signal is up converted in the X band by means of a frequency doubler, than the X band signal passes trough the amplifiers and the phase shifting block, and finally it is down converted

again at low frequencies. We can than define the device under test (DUT) as the series of a programmable gain amplifier and a TTD phase shifter, as shown in Fig.1.7.

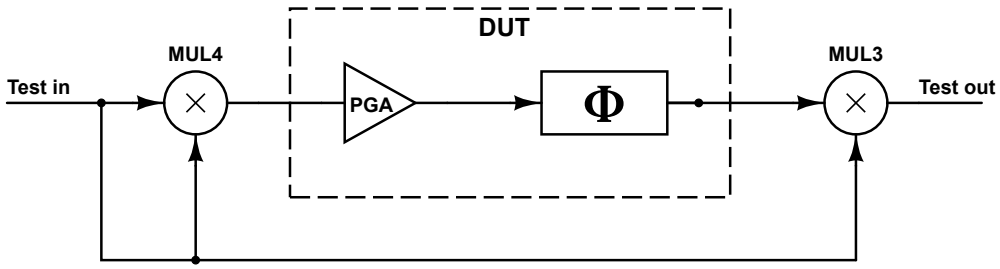

Figure 1.7: Representation of the DUT

1.4 Performances required

The design of the test equipment is based on the specifications given for this project. Basically there are two types of requests, those on the measurement precision and those on the interaction of the system with the rest of the radar system and the off-chip measurement instruments. The measurement system is considered accurate if:

- The relative phase measurement error is below 5^o.
- The relative gain measurement error is below 1dB.
- The previous properties are satisfied for temperatures in the range of $0^o\text{C} - 85^o\text{C}$ and for 5% voltage. supply variations.

Additionally, the following properties must be satisfied:

- The input and output impedances of the BITE must be matched to 50 Ω.

- The output of the frequency doubling part must be matched to the input impedance of the DUT.
- The input of the down converting part, must be matched to the output impedance of the DUT.
- The BITE must be uninfluential on the radar system when it is switched off.
- The silicon area occupied by the test system must be as small as possible.
- Since the area occupied must be small, inductors cannot be used.

An high level description of the device under test is given in order to allow the proper sizing of the circuit that surrounds it. In Tab. 1.1 all the given features of the DUT are listed.

Parameter	**Min**	**Nom**	**Max**	**Units**
Power gain	-15	-	3	dB
Phase shift	0	-	180	deg
IIP3	-	0	-	dBm
P_{1dB}	-	-10	-	dBm
Zin	-	100	-	Ω
Zout	-	100	-	Ω
NF	-	10	-	dB

Table 1.1: DUT parameters

1.5 SiGe BiCMOS technology of Infineon

It is clear that the technology utilized for the radar system, which is the SiGe BiCMOS technology developed by Infineon, must be the same used for the BITE. Hence a brief overview on the features of this technology is useful to understand which devices and structures are available and which are their performance and limits.

1.5.1 BiCMOS

The fabrication of integrated circuits has usually the issue to make analog and digital circuit coexist in the same die, this issue rises since the request of low area and low power consumption of the digital circuits which forces the use of the CMOS technology, does not coincide with the analog circuit requirements which typically prefers a bipolar process. The used BiCMOS process, has the advantage of including both the bipolar devices and the MOS ones using local insulation techniques, at the cost of a higher complexity and a more expensive fabrication process.

1.5.2 SiGe HBTs

Traditional homojunction bipolar transistors, are realized using the same semiconductor i.e. silicon, for the collector, emitter and the base, this choice impose some tradeoffs between different features of the devices, since the only degree of freedom are the doping density of the semiconductor or the geometry of the device and improving one of the parameters usually involves the degradation of the others. In the typical design of bipolar transistors, the emitter is highly doped if compared to the base, in order to increase the emitter junction efficiency[6]:

$$\gamma = \frac{1}{1 + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \tag{1.2}$$

where N_A and N_D are the doping densities in the base and in the emitter respectively, D_p and D_n are the diffusion constant for the holes and the electrons and W_B and L_p are the base width and the holes diffusion length in the emitter. Reducing the doping of the base, however, results in a higher transition time through the base, for the minoritys carrier, hence a lower transition frequency for the device. If the doping density is kept constant and the base width is reduced, the transition time is also reduced, but the base resistance is increased, limiting again the maximum speed of the transistor. Heterojunction bipolar transistors (HBT) introduce an additional degree of freedom, using Germanium in the base of the transistor. This modification, thanks to the different

band gap between silicon and germanium, which inhibits the injection of holes from the base to the emitter, allows to use lower doping densities in the emitter and higher doping densities in the base, which both implies higher speed for the device i.e. higher f_t. A cross section of the described device is shown in Fig.1.8.

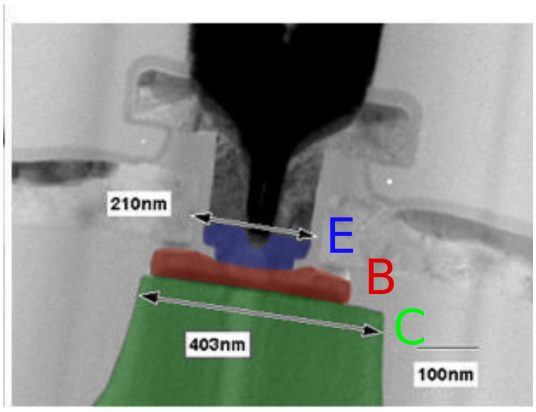

Figure 1.8: HBT cross section [5]

In the considered technology, high speed, and high voltage HBTs are available. The high voltage HBTs are used instead of high speed HBT, when the operating voltage applied at the transistor, exceeds the breakdown voltage of the high speed HBT, which is quite small for the considered technology (as in every BiCMOS process). However, the use of such devices limits the maximum speed of the transistor. The electrical characteristic of the high speed HBT is shown in Fig.1.9, we can see that for collector- emitter voltages over 1.4V the current increases abruptly due to the breakdown mechanism. Hence, such HBT should never be used with collector- emitter voltages close to the breakdown condition.

1.5.3 Metallizations

In this technology six levels of copper metal plus a top aluminum layer are available. The lower levels are suitable for short connections having small currents, since their resistance per unit of length is higher compared to the higher levels and their power dissipation capability is low. Conversely, the top layers are used to carry high currents and to realize high Q inductor, thanks

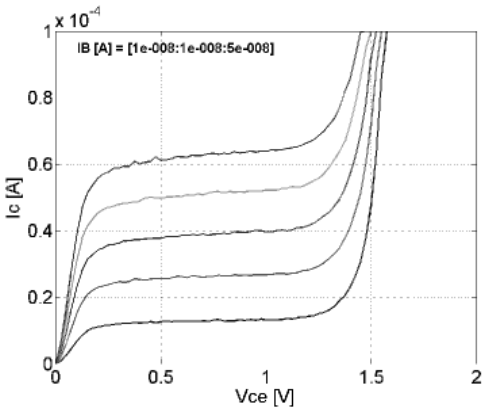

Figure 1.9: High speed HBT characteristic [5]

to their lower resistance per unit of length. A cross section of the metal layers structure is shown in Fig.1.10.

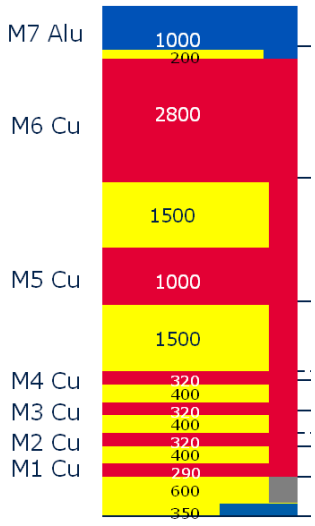

Figure 1.10: Metals structure [5]

1.6 Figures of merit

In this section we introduce the main figures of merit used to define the project specifications and describe the system performance once it has been designed.

1.6.1 Conversion gain

When the input and output impedances of a mixer are equal, the conversion gain is defined as the ratio between the power of its output and the power of its input:

$$Cg_P = \frac{P_{OUT}}{P_{IN}} \quad \rightarrow \quad Cg_P|_{\mathrm{dB}} = 10\log(P_{OUT}) - 10\log(P_{IN}) \tag{1.3}$$

However, since the input and the output ports of the frequency mixers utilized in this work are not matched for optimal power transfer, we define the conversion gain of the mixer as the ratio between the amplitude of its output signal and the amplitude of its input signal :

$$Cg_V = \frac{V_{OUT}}{V_{IN}} \quad \rightarrow \quad Cg_P|_{\mathrm{dB}} = 20\log(V_{OUT}) - 20\log(V_{IN}) \tag{1.4}$$

The power and voltage conversion gain expressed in dB coincides when input and output impedances are equal, hence we will use the power conversion gain to characterize the blocks of the system which have such properties.

1.6.2 Voltage and Power

In this thesis, we refer to signals for their power or their amplitude respectively in dBm and dBV which are defined as:

$$P_{\mathrm{s}}|_{\mathrm{dBm}} = 10\log\left(P_{\mathrm{s}}\right) + 30 = 10\log\left(\frac{V_{\mathrm{s}}^2}{R}\right) + 30 \tag{1.5}$$

$$V_{\mathrm{s}}|_{\mathrm{dBV}} = 20\log\left(V_{\mathrm{s}}\right) \tag{1.6}$$

It is important to state that, to define the power of a signal we always need to know to which resistance it is referred. In this work, we refer the power

of differential signals to 100Ω, even when the signal is not applied to such a resistance. An example could be a multi stage circuit having equal input and output impedances, but no impedance matching between its stages. We can improperly use the power conversion gain in dB from stage to stage, using the same reference resistance and once we consider the whole circuit, we can sum up the gains and the final power conversion gain will get physical meaning again.

1.6.3 IIP3 and 1dB compression point

Mixers are devices that change amplitude and frequency of their input signals. We need to define a way to quantify their distortion properties. The capability of a mixer to suppress the third order intermodulation of two tones at its RF input is measured through the use of of its third order input referred intercept point (IIP3). This figure of merit is typically measured in dBm (or dBV) and indicates the power (or amplitude) of the input signal, where the output wanted component and the one due to the third order intermodulation would have the same power (or amplitude) if their increasing trend was the same as the one at low input signals [7]. Another measurement useful to determine which is the maximum input signal before the gain of the mixer starts to saturate, is the 1dB compression point, which is the power or amplitude of the signal at which the gain of the mixer is reduced by 1dB compared to its regular value. A graphical representation of these figure of merit is given in Fig.1.11.
The IIP3 measurement on a mixer is performed, using the intermodulation distortion measurement IM_3 which is the ratio between the third order intermodulation product in the output to the intermediate frequency fundamental signal in the output [8]. Two signal having the same amplitude but different frequencies : f_1 and f_2 are applied at the input of the mixer. The third order intermodulation product in the output is than given by the output components at frequencies: $(f_0 - 2f_1 + f_2)$ and $(f_0 - 2f_2 + f_1)$ and the fundamental signal in the output is at frequencies: $(f_0 - f_1)$ and $(f_0 - f_2)$ where f_0 is the frequency of the local oscillator signal (LO). Once the IM_3 is calculated at a given input power far from the compression point, we can simply derive the IIP3 using the

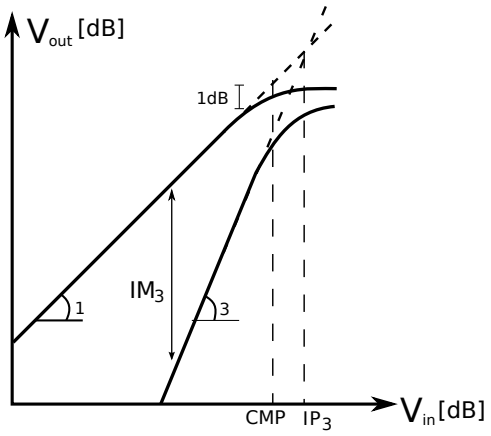

Figure 1.11: Representation of intercept point, intermodulation distortion and compression point

following equation:

$$IIP3_{\mathrm{dB}} = P_{\mathrm{indB}} - \frac{1}{2}\mathrm{IM}_{3\mathrm{dB}} \tag{1.7}$$

1.6.4 Relative phase and gain errors

The test that has to be performed on the DUT aims at assessing the relative phase and gain. In fact only relative measurement are of interest, since an absolute shift in the phase does not change the radiation pattern of the array. We define these quantities as:

- **Relative phase**: it is the difference between the phase shift introduced by the DUT for a given configuration of its phase control bits and the phase shift introduced by the same DUT when its phase controls bits are all zeroes.

- **Relative gain**: it is the ratio between the gain introduced by the DUT for a given configuration of its gain control bits and the gain introduced by the same DUT when its gain control bits are set to zero.

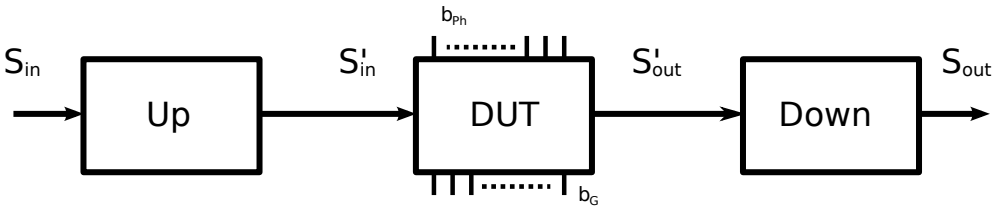

Figure 1.12: Test setup

To understand how the relative phase and gain errors are defined, we refer to Fig.1.12. The measurement of the relative phase error versus frequency is performed by following the subsequent steps:

1. To obtain the reference for the DUT phase, the absolute phase difference is measured from S'_{in} to S'_{out} sweeping the input signal frequency and setting all the phase control bits to zero.

2. The reference phase for the whole setup is measured in the same way but measuring the phase difference between S_{in} and S_{out}.

3. Then the DUT relative phase difference, for every configuration of the phase control bits is measured by subtracting the reference obtained in the first point to the absolute phase measured from S'_{in} to S'_{out} sweeping the frequency.

4. Then the total setup relative phase difference, for every configuration of the phase bits is measured by subtracting the reference obtained in the second point point to the absolute phase measured from S_{in} to S_{out} sweeping the frequency.

5. Finally the relative phase error is measured by subtracting the relative phase difference of the total setup to relative phase difference of the DUT.

   The procedure to obtain the relative gain error is exactly the same as discussed for the relative phase error, but instead of difference between signals phases, we are taking ratios between signals amplitudes.

1.6.5 Scattering parameters

A way to describe how signals propagates through a N port network is the scattering matrix, which is a NxN matrix in the form:

$$\begin{bmatrix} b_1 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1N} \\ \vdots & \ddots & \vdots \\ S_{N1} & \cdots & S_{NN} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ \vdots \\ a_N \end{bmatrix} \tag{1.8}$$

In this matrix the parameters a_i represent the incident wave at the i port and the parameters b_i represent the reflected wave at the i port. We can see that the S_{ii} elements on the diagonal of the scattering matrix, quantifies the reflection at the i^{th} port when all the remaining ports are impedance matched:

$$S_{ii} = \frac{b_i}{a_i} \tag{1.9}$$

This coefficient can vary from one, when all the incident wave is reflected, to zero, when the port considered is impedance matched, hence no reflection exists.

1.6.6 Stability

One of the fundamental steps in the design of RF circuits, is checking its stability. In fact, even if the considered circuit has been designed without explicit feedback, at high frequencies, some feedback paths may exist and if they satisfy the Barkhausen criterion, the circuit becomes unstable. A circuit is said to be unconditional stability, if there is not any combination of passive source and load impedance such that the circuit is unstable[9]. A fast way to check the unconditionally stable, is to use the Rollet's stability factors defined as[10]:

$$K(f) = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{1.10}$$

$$B_1(f) = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta \tag{1.11}$$

where the Δ is defined as:

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{1.12}$$

A two ports circuit is unconditionally stable, if its factor K is larger than one and $B_1(f)$ is bigger than zero.

CHAPTER 2

BITE blocks

In this chapter, the device under test (DUT) and all the blocks of the BITE are presented. The goal of this chapter is to give an high level description of the theoretical behavior of the test system, in order to understand the choices made in the design of the BITE.

2.1 Device Under Test

The DUT is formed by the cascade of a low noise gain stage LNA+PGA and a phase shifter. The combination of these blocks allows to vary in a discrete way the amplitude and the phase of the input signal in determined intervals by varying the input bits of the PGA and the phase shifter. Hence, the whole system has two independent variables which are the bit configurations of the PGA, b_{PGA} and the the bit configurations of the phase shifter, b_{PS} whose combination gives a determined gain and phase shift, for a given frequency of the input signal:

$$S_{out}(b_{PS}, b_{PGA}) = A_{LNA} \cdot A(b_{PS}, b_{PGA}) \cdot S_{in}(\phi(b_{PS}, b_{PGA})) \tag{2.1}$$

Eq.2.1 shows that the phase shift and the gain introduced by the DUT are both a function of b_{PGA} and b_{PS}, since the different configurations of the gain stage will not leave the phase of the signal unchanged and, in the same way, every different configuration of the phase shifting stage will cause different attenuations.

2.1.1 Frequency dependance of the DUT

Phased array systems can be realized using several type of phase shifters to control the phase of the input/output signal of every element of the array. The main distinction that can be made is between true time delay (TTD) element and phase shifter having constant phase shift versus frequency [4]. The first one works in the time domain giving a different time delay for every configurations of the bits. This means that every frequency component of the input signal is shifted in phase of a quantity that is proportional to its frequency, hence, the group delay of the TTD phase shifter is constant. The second one changes the phase of the input signal, depending on its bits configuration, but in contrast to the first one this phase shift is constant with frequency resulting in a non constant group delay[11]. If the system considered is narrowband, the operation of both the phase shifters is approximately equal. The type of phase shifter chosen to model the DUT, is a true time delay phase shifter, since it can be emulated in a simpler way using a transmission line which varies its length. As said before, this type of phase shifter has constant group delay, hence, the phase shift introduced for a given configuration of its bits, will be proportional to the frequency of its input signal.

The purpose of this work, is to provide a test equipment which in combination with ATE, is able to accurately measure the phase shift and the gain introduced by the DUT. These measurements result in a phase-amplitude characterization of the DUT, which is mandatory in a radar system in order to perform a precise orientation of the beam.

2.2 Current commutating mixers

Performing measurements at half of the DUT operation frequency requires to double the frequency of the input test signal and halve the frequency at the output of the DUT. Since frequency shift is needed, and linear time invariant circuits can only perform phase shifting and amplitude scaling of signals, the only way to obtain it, is through the use of a time-varying or a nonlinear device. Such an operation can be mainly achieved in two ways: using the intrinsic nonlinear characteristic of a device, for example a diode, or creating a time varying operation using commutating switches. When two sinusoidal signals V_{LO} and V_{RF} having respectively f_{LO} and f_{RF} frequencies, are elaborated together through a nonlinear device, the result is a signal V_{IF} which has frequency components given by linear compositions of f_{LO} and f_{RF}. This phenomenon is called mixing and the nonlinear device that performs it is a mixer. Typically mixers are used to perform up and down frequency conversions where the output signal V_{IF} has frequency given by the sum of f_{LO} and f_{RF} or by the subtraction of these two frequencies.
In this work, current commutating mixers are used. They are made of three parts as shown in Fig.2.1: the transconductor, the switching cell and the load impedance.

In order to understand how a current steering mixer works, it is easier to first analyze a single balanced current steering mixer whose model is shown in Fig.2.1. Starting from the input signal V_{RF}, i_{RF} is generated by the transconductor who has gain G_m, and summed to the DC bias current of the transconductor, I_B:

$$I_b(t) = I_B + G_m V_{RF}(t) = I_B + i_{RF}(t) \tag{2.2}$$

I_b is then steered from one output branch to the other, and converted again to a voltage signal by the load impedances Z_L which produce the differential voltage output signal V_{IF} :

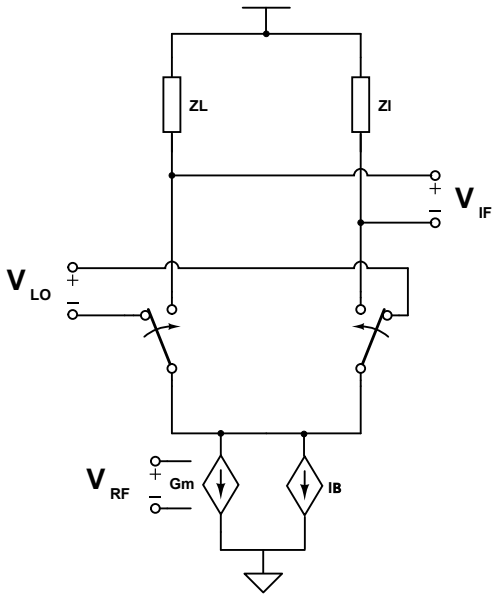

Figure 2.1: Model of a single balanced current steering mixer

$$V_{IF} = Z_L \left[I_B + i_{RF}(t) \right] \cdot \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\sin\left(2\pi f_{LO} t(2n-1)\right)}{(2n-1)} \tag{2.3}$$

The second term in (2.3) is the Fourier series expansion of the square wave function representing the switching action at frequency f_{LO} controlled by V_{LO}. Considering only the first term of the series, corresponding to the fundamental component of the square wave, we have:

$$V_{IF} = i_{RF}(t) \cdot Z_L \frac{4}{\pi} \sin\left(2\pi f_{LO} t\right) + I_B \cdot Z_L \frac{4}{\pi} \sin\left(2\pi f_{LO} t\right) \tag{2.4}$$

The first term of (2.4) is the desired mixing operation between V_{RF} and V_{LO}, while the second is a usually unwanted component at the switching frequency f_{LO} called **LO feedthrough**. In a single balanced mixer, there is no distinction between the input current I_{RF} and the DC bias current I_B. Hence, I_B is also multiplied by the switching cell and appears at the output of the mixer. In the considered application the presence of LO feedthrough highly degrades the performance of the measurement system especially in the down conversion path.

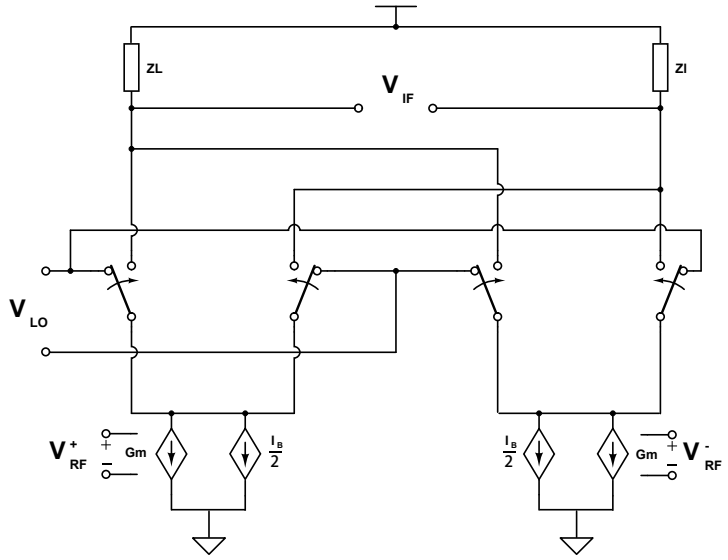

Figure 2.2: Model of a double balanced current steering mixer

To get rid of the LO feedthrough the only viable strategy, is to use a double balanced mixer (DBM) which distinguishes between bias and input currents. A a scheme of the double balanced current steering mixer, called a **quad**[12], is shown in Fig.2.2. In a perfectly symmetric circuit there is no effect of the bias current on the differential output since a constant I_B current flows for the entire switching period through the load impedances, producing exactly the same voltage at the differential outputs. Conversely the input currents i_{RF}^{+} and i_{RF}^{-} given by:

$$i_{RF}^{+} = \frac{V_{RF}}{2} G_m = V_{RF}^{+} G_m \tag{2.5}$$

$$i_{RF}^{-} = -\frac{V_{RF}}{2} G_m = V_{RF}^{-} G_m \tag{2.6}$$

produce equal magnitude but opposite sign voltages on the load impedances, resulting in a differential output signal:

$$V_{LO} = \left(i_{RF}^{+} - i_{RF}^{-}\right) \cdot Z_L \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\sin\left(2\pi f_{LO} t(2n-1)\right)}{(2n-1)} \tag{2.7}$$

$$\tag{2.8}$$

$$= V_{RF} \cdot G_m Z_L \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\sin\left(2\pi f_{LO} t(2n-1)\right)}{(2n-1)} \tag{2.9}$$

As we can see, the output component at frequency f_{LO}, due to the commutation of the bias current has disappeared, leaving only the result of the mixing between the odd frequency components of the square wave at f_{LO} and the frequency components of V_{RF}. This does not mean that there will be no components having frequency f_{LO} at the output, even if the input signal does not show such components. In fact, we will see in the following sections that a linear combination of the input signal's frequency with the frequency components of the square wave generated by V_{LO} can results in output components at f_{LO}.

2.3 Frequency doubler

The frequency doubling operation needed in the test equipment, can be performed using a double balanced mixer. If the two input signals of an ideal mixer are sinusoidal and have the same frequency $f_{IF} = f_{LO} = f_0$, the output signal will be :

$$V_{RF} = V_{IF} \cdot V_{LO} = \sin(\omega_0 t) \cdot \sin(\omega_0 t) = \frac{1}{2}[1 - \cos(2\omega_0 t)] \tag{2.10}$$

Equation (2.10) represent only an approximation of the behavior of the double balanced mixer . If all the higher frequency components of the square wave are taken into account, the spectrum of the output signal will have infinite frequency components. However the higher is the order of the component, the smaller its amplitude. Hence, we can assume that above a certain order those components are negligible. In Fig.2.3 the output frequency components of an up converter having $f_{IF} = f_{LO} = 5GHz$ are illustrated. The input signal are represented in red and the ideal mixing output components are represented

in green, all the remaining components are caused by the higher frequency components of the LO signal.

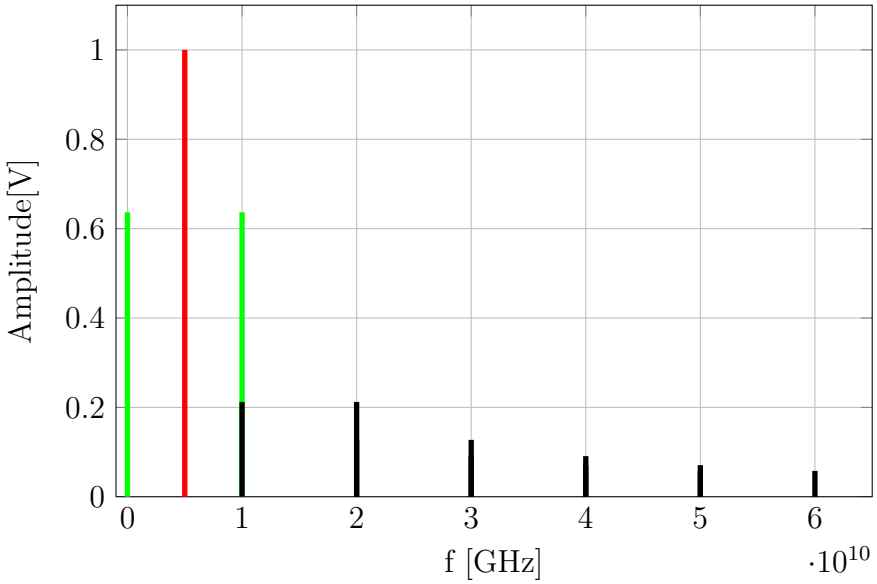

Figure 2.3: Output spectrum of a up converter DBM for $n \leq 12$

As we can see, some of the compositions between the high frequencies components of the LO signal and f_{IF} results in an output signal at $f_{RF} = 2f_{IF}$, the order of these components is given by:

$$2f_{IF} = |f_{IF} \pm (2n-1)f_{LO}| \quad \text{with } n \,\epsilon\, \mathbb{N} \quad \rightarrow n = 1,\ n = 0 \tag{2.11}$$

Hence, the fundamental and the third harmonic of the LO signal mixed with the IF signal, produce an RF signal having frequency $2f_{IF}$. All the other components fall at frequencies higher than $4f_{IF}$ and can be easily filtered out. The issue now is wether this undesired output component at $2f_{IF}$ effects the BITE system. When two sinusoids at the same angular velocity $w_0 = 2\pi f_0$, and arbitrary phase difference are summed together, the result is a sinusoid having the same angular velocity but phase and aptitude depending on the phase difference and the amplitude of the starting signals. If only the the first and the third harmonic of the LO signal are considered, the multiplication with the IF signal can be written as:

$$V_{RF}(t) = \sin(\omega_0 t + \Delta\phi) \cdot \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_o t)\right] =$$
$$\frac{2}{\pi}\left[\cos(\Delta\phi) - \cos(2\omega_0 t + \Delta\phi) + \frac{1}{3}\cos(2\omega_0 t - \Delta\phi) - \frac{1}{3}\cos(4\omega_0 t + \Delta\phi)\right]$$

Where $\Delta\phi$ is the phase difference between the IF signal and the fundamental component of the LO signal. Considering only the components at frequency $2\omega_0$ we have:

$$V_{RF}(t)|_{2\omega_0} = \frac{2}{\pi}\left[\frac{1}{3}\cos(2\omega_0 t - \Delta\phi) + \cos(2\omega_0 t + \Delta\phi + \pi)\right] \tag{2.12}$$

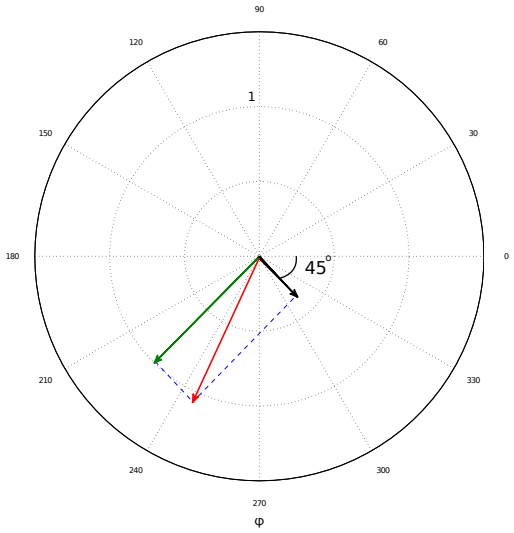

Figure 2.4: Representation of (2.3) with $\Delta\phi = 45^o$

In Fig.2.4, (2.3) is represented as the sum of two phasors. The resulting RF signal can have magnitudes greater or smaller as compared to the ideal mixer output moreover its phase varies with $\Delta\phi$. However, since both the phasors have the same angular velocity ω_0 the magnitude and the phase shift of the output signal remains constants if $\Delta\phi$ is constant. Since the measurement

performed at the output of the DUT are referred to an initial amptitude and phase, a constant shift of phase and amplitude introduced by the third order component of the LO signal does not affect the accuracy of the measurement system. The effect of the third harmonic can be also seen in Fig.2.5 where the amplitude and the phase of the IF signal are traced in function of $\Delta\phi$. The blue dashed line represents the IF signal if the LO third component is neglected, and the thick black line represents the RF signal considering the third harmonic contribution.

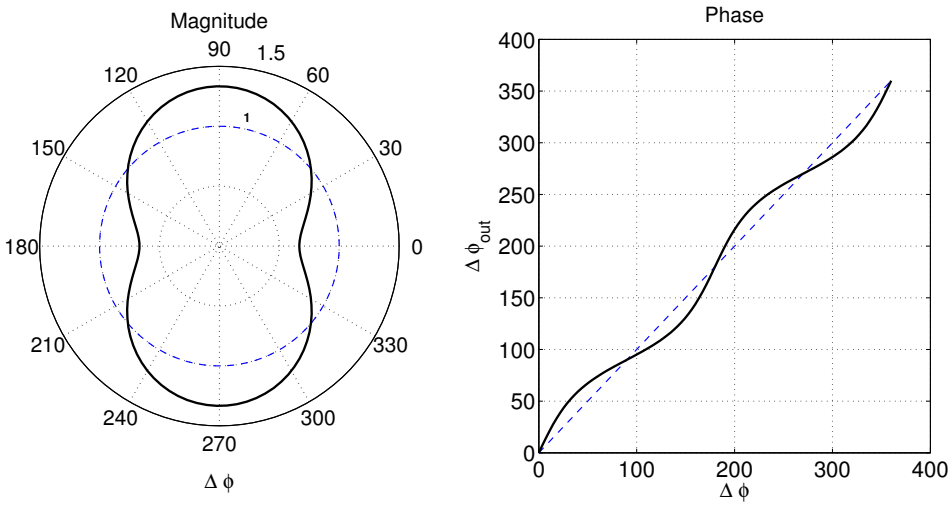

Figure 2.5: Gain and output phase difference versus $\Delta\phi$

It is interesting to calculate the variation of the conversion gain of the frequency doubler with $\Delta\phi$ if the influence of the third harmonic is considered. Considering a DBM used as a frequency multiplier, having a transconductor with gain G_m and a load impedance Z_L, the dependence of the conversion gain on $\Delta\phi$ can be calculated by manipulating the phasor components in Fig.2.4:

$$
\begin{aligned}
G_{DBM} =& \frac{2}{\pi} G_m Z_L \sqrt{\left[\frac{1}{3}\cos(\Delta\phi) - \cos(\Delta\phi)\right]^2 + \left[\frac{1}{3}\sin(\Delta\phi) + \sin(\Delta\phi)\right]^2} \\
=& \frac{4}{3\pi} G_m Z_L \sqrt{\cos^2(\Delta\phi) + 4\sin^2(\Delta\phi)} \qquad (2.13) \\
=& \frac{4}{3\pi} G_m Z_L \sqrt{1 + 3\sin^2(\Delta\phi)}
\end{aligned}
$$

The ratio between the DBM conversion gain and the gain neglecting the third harmonic of the LO signal is than :

$$
\frac{G_{DBM}}{G_{IM}} = \frac{\frac{4}{3\pi} G_m Z_L \sqrt{1 + 3\sin^2(\Delta\phi)}}{\frac{2}{\pi} G_m Z_L} = \frac{2}{3}\sqrt{1 + 3\sin^2(\Delta\phi)}
$$

and is traced in Fig. 2.6, showing that the actual conversion gain of the frequency doubler can be higher or lower compared to the one where the third harmonic is neglected, depending on $\Delta\phi$.

2.4 Polyphase filter

When two in-phase sinusoidal signals at the same frequency, are multiplied, the resulting signal is made of a DC component and a sinusoid whose frequency is doubled compared to the input ones:

$$
\sin(\omega_0 t) \cdot \sin(\omega_0 t) = \frac{1}{2}[1 - \cos(2\omega_0 t)] \qquad (2.14)
$$

Equation (2.14) describes the operation performed by the frequency doubler, if the harmonics of the LO signal are neglected. In addition to the desired component at $2\omega_0$, a DC offset between the two differential outputs exist and even thought this unwanted offset can be completely filtered out using AC coupling, it's desirable to remove it directly at the frequency doubler output.

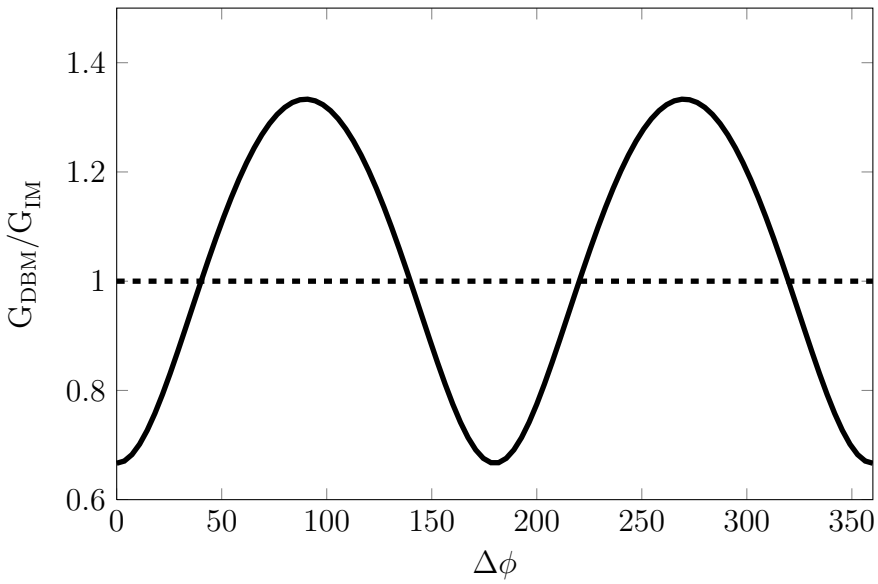

Figure 2.6: Ratio between the frequency doubler gain and the ideal mixer gain.

In fact, a DC voltage difference between the differential outputs of the up converting mixer implies two different operating points of the transistors of the switching cell and could become a serious limitation to the output swing of the frequency doubler. Furthermore, since the breakdown voltage of the High Speed Transistor used in this work is quite small, an additional DC offset, added to the bias voltage could be an issue. The product of two sinusoids at the same frequency, with $\Delta\phi$ phase difference is :

$$\sin(\omega_0 t) \cdot \sin(\omega_0 t + \Delta\phi) = \frac{1}{2}[\cos(\Delta\phi) - \cos(2\omega_0 t + \Delta\phi)] \tag{2.15}$$

When $\Delta\phi$ is $\frac{\pi}{2}$ the DC component is erased.
A polyphase filter can be used to generate two differential sinusoidal signals in quadrature, from a single sinusoidal signal. The quadrature signals can be used as IF and LO signals for the mixer, erasing the unwanted output DC component.
In this work, a singe stage polyphase filter is used to accomplish this task. Referring to Fig. 2.7 it's possible to derive the behavior of the polyphase filter, using the superposition principle. We derive the output signals of the

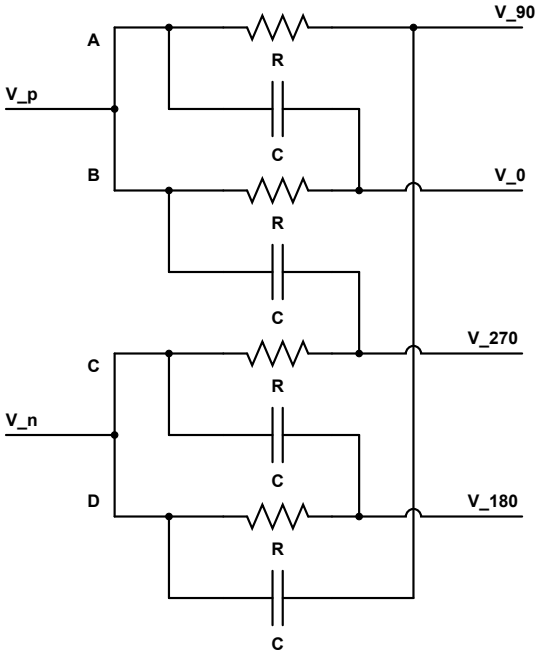

Figure 2.7: Single stage polyphase filter

polyphase filter V_0, V_{90}, V_{180} and V_{270}, making the assumptions that the filter is not loaded, all the capacitors and the resistances are equal and the input voltage source has zero output impedance.

In order to make the polyphase filter works as a differential quadrature signal generator, the inputs A and B must be equal to the positive differential input and C and D, must be equal to the negative differential input. If the V_p generator is switched on and the V_n generator is switched off, we obtain the equivalent circuit in Fig.2.8. Hence, the output signals are:

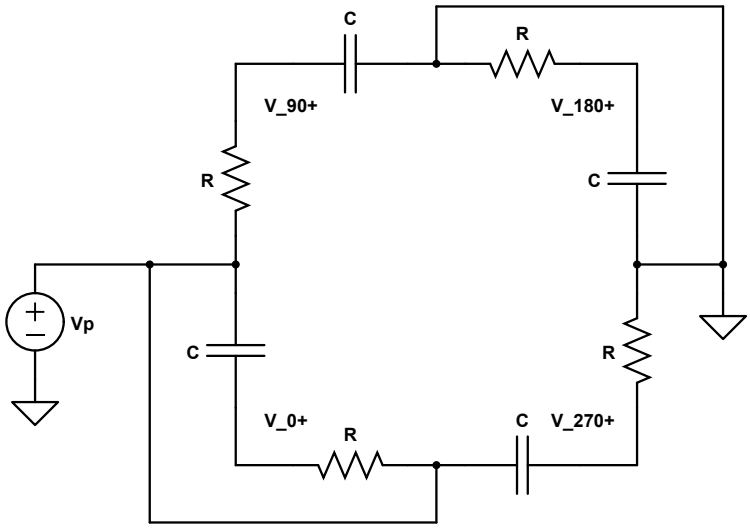

Figure 2.8: Polyphase signal with V_p applied

$$V_0^+ = V_p$$

$$V_{90}^+ = V_p \frac{sRC}{1 + sRC}$$

$$V_{180}^+ = 0;$$

$$V_{270}^+ = V_p \frac{1}{1 + sRC}$$

Likewise, switching on the V_n generator and switching off the V_p generator results in:

$$V_0^- = 0$$

$$V_{90}^- = V_n \frac{1}{1+sRC}$$

$$V_{180}^- = 0$$

$$V_{270}^- = V_n \frac{sRC}{1+sRC}$$

Using the superposition principle, the signal at every output of the polyphase filter, when a differential signal V_{id} is applied at the input, is:

$$V_0 = V_0^+ + V_0^- = V_p$$

$$V_{90} = V_{90}^+ + V_{90}^- = V_p \frac{\frac{s}{\omega_0}}{1+\frac{s}{\omega_0}} + V_n \frac{1}{1+\frac{s}{\omega_0}}$$

$$V_{180} = V_{180}^+ + V_{180}^- = V_n$$

$$V_{270} = V_{270}^+ + V_{270}^- = V_p \frac{1}{1+\frac{s}{\omega_0}} + V_n \frac{\frac{s}{\omega_0}}{1+\frac{s}{\omega_0}}$$

Where $\omega_0 = \frac{1}{RC}$. These equations can be simplified if we use :

$$V_p = \frac{V_{id}}{2} \quad ; \quad V_n = -\frac{V_{id}}{2}$$

After some algebraic manipulations. we get the final expression for the output signal given the differential input signal $V_{id} = V_p - V_n$:

$$V_0 = \frac{V_{id}}{2}$$

$$V_{90}(j\omega) = -\frac{V_{id}}{2} \cdot e^{-j2\arctan\left(\frac{\omega}{\omega_0}\right)}$$

$$V_{180} = -\frac{V_{id}}{2}$$

$$V_{270} = \frac{V_{id}}{2} \cdot e^{-j2\arctan\left(\frac{\omega}{\omega_0}\right)}$$

Two differential signal $VI_{id} = V_0 - V_{180}$ and $VQ_{id} = V_{90} - V_{270}$ are generated. If the filter is not loaded, the amplitude of the output differential signals, is the same as the input one and the phase relation between the signals depends on $\frac{\omega}{\omega_0}$

$$\Delta\phi = -2\arctan\left(\frac{\omega}{\omega_0}\right) \tag{2.16}$$

We need to assess the maximum DC offset produced by the mixing operation when the frequency of the LO and IF signals varies from $4GHz$ to $6GHz$. Using (2.15), the ratio between the DC offset and the amplitude of the wanted component as a function of the input frequency, can be expressed as:

$$\frac{Vod_{DC}}{Vod_{IF}} = \cos\left[-2\arctan\left(\frac{\omega}{\omega_0}\right)\right] \tag{2.17}$$

If ω_0 is set as the geometric mean of the maximum and minimum input frequencies, $\omega_0 = 2\pi\sqrt{f_h f_l}$, the DC offset at the output of the frequency doubler has a maximum magnitude of:

$$Vod_{DC} = Vod_{IF} \cdot \cos\left[-2\arctan\left(\sqrt{\frac{f_l}{f_h}}\right)\right] = 0.2 \cdot Vod_{IF} \tag{2.18}$$

Where Vod_{IF} is the amplitude of the desired output signal. In Fig.2.9, (2.18) is shown, it is possible to see that choosing ω_0 equal to the center frequency (geometric mean) is the best choice, for a singe stage polyphase filter, in the application considered, since the magnitude of the DC offset is minimized.

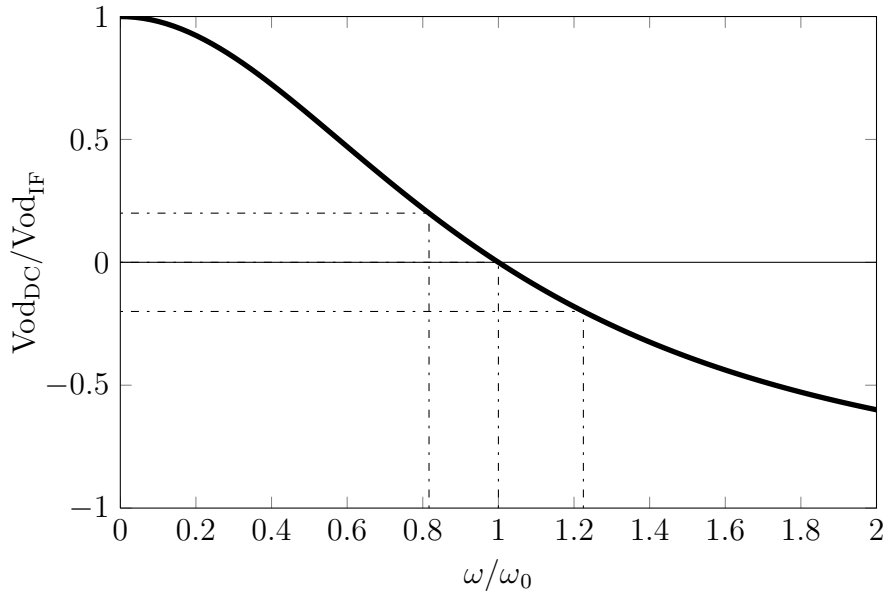

Figure 2.9: Output DC offset at different input frequencies

2.5 Down converter

Once the input test signal goes through the frequency doubler and the DUT, we need to halve his frequency and measure the change in its phase and amplitude characteristics. Since the characterization of the DUT relies on the input-output test signals, the measurement system should not introduce any variation of the phase and the amplitude of the test signal related to the configuration of the DUT control bits.

The down conversion of the signal at the output of the DUT can be performed using a DBM. The mathematical description of the down conversion is exactly the same asthat used for the frequency doubler, but in this case, the LO frequency is different from the RF frequency. In particular, since we want to halve the frequency of the RF signal, we set $f_{LO} = \frac{f_{RF}}{2}$. With this assumptions, the main IF frequency components are:

$$f_{IF}^{h} = f_{RF} + f_{LO} = \frac{3}{2} f_{RF}$$

$$f_{IF}^{l} = f_{RF} + f_{LO} = \frac{f_{RF}}{2}$$

We can than use (2.11) to verify which frequency components due to the LO signal harmonics, are present at the wanted output frequency:

$$\frac{f_{RF}}{2} = |f_{RF} \pm (2n-1)\frac{f_{RF}}{2}| \quad with\ n\ \epsilon\ \mathbb{N} \quad \rightarrow n = 1,\ n = 0 \tag{2.19}$$

As in the frequency doubler case, both the fundamental and the third harmonic components of the LO signal produce components at the IF frequency. In Fig.2.10 the IF signal spectrum is shown taking into account the first 12 harmonics of the LO signal.
Considering only the mixing of the RF signal at frequency $2f_0$ with and the first and third harmonics of the LO signal at frequency f_0, we have:

$$V_{IF}(t) = \sin(2\omega_0 t + \Delta\phi) \cdot \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t)\right]$$

$$= \frac{2}{\pi}\left[\cos(\omega_0 t + \Delta\phi) - \frac{1}{3}\cos(\omega_0 t - \Delta\phi) - \cos(3\omega_0 t + \Delta\phi) - \frac{1}{3}\cos(5\omega_0 t + \Delta\phi)\right]$$

where $\Delta\phi$ is the phase shift between the LO and the RF signal. The presence of this spurious component represent the main issue in the measurement system,

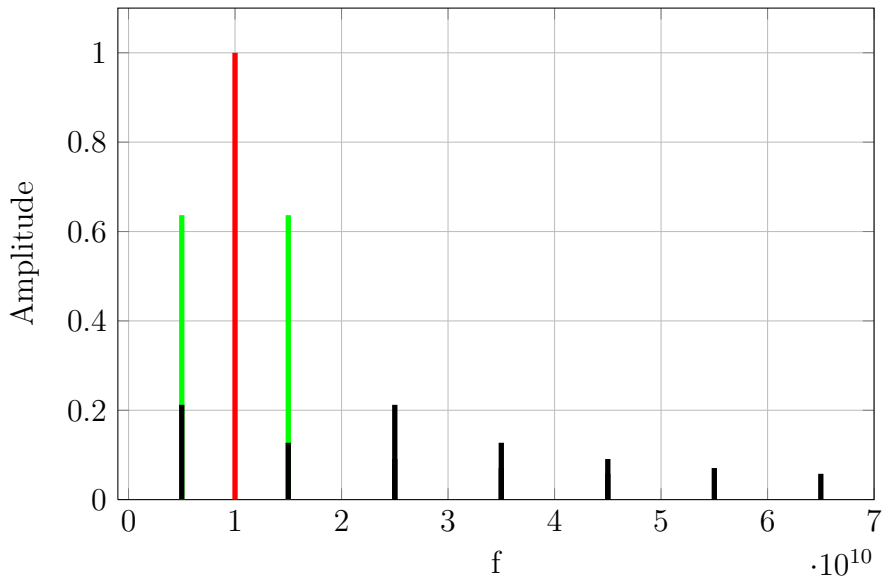

Figure 2.10: Output spectrum of a down converter DBM for $n \leq 12$

since the component of interest for the test, is the one at f_0, we can consider only :

$$V_{IF}(t)|_{\omega_o} = \frac{2}{\pi}\left[\cos(\omega_0 t + \Delta\phi) + \frac{1}{3}\cos(\omega_0 t - \Delta\phi + \pi)\right]$$

This equation is very similar to (2.12) hence produces similar effects on the phase and the amplitude of the output signal. However, in this case $\Delta\phi$ changes with the configuration of the DUT's bits. Thus, the measurement will be severely affected by the presence of the third harmonic of the LO signal. The analytical expressions of the phase and the amplitude of the output signal, as a function of $\Delta\phi$, derived with the aid of the phasor representation of Fig.2.4 are:

$$|V_{IF}(t)|_{\omega_o} = \frac{4}{3\pi}\sqrt{1 + 3\sin^2(\Delta\phi)} \tag{2.20}$$

$$\angle V_{IF}(t)_{\omega_o} = \arctan\left[2\tan(\Delta\phi)\right] \tag{2.21}$$

As opposed to the up conversion case, where $\Delta\phi$ and the amplitudes of the LO and RF signals are constant (if the input frequency is constant), in the down conversion case, these values change accordingly to the phase shift and the gain introduced by the DUT. Hence,the presence of the third harmonic of the LO signal, heavily degrades the measurement precision of the BITE, if no post processing on the output signal is performed. An attempt to remove the error introduced in the measurement using signal post processing has been made, and will be treated in the section: "alternative solutions" along with other explored solutions, that have been discarded due to feasibility and complexity reasons. The approach used in this work, aims at removing the cause of the measurement error, namely the third harmonic of the LO signal. To reduce and try to erase this harmonic the switch have to commutate in a sinusoidal way, in this case, the mixing of the RF and the LO resemble the analog multiplication between the two sinusoidal signal, hence, the device that performs this operation, is usually called **analog multiplier**.

2.5.1 Analog multiplier

The analog multiplier chosen in this work consists in a quad mixer using pre distortion at the LO input in order to make the switching cell commutate in a sinusoidal fashion[12]. This circuit, also called four quadrant translinear multiplier, can be analyzed using the translinear principle formalized by Gilbert in 1975 [13] which states:

"In a closed loop of bipolar junctions having an equal number of junction in the clockwise and in the counterclockwise direction, the product of current densities in the clockwise direction junctions, equals the product of the current densities in the counterclockwise direction"

This principle exploits the linear relation that exists between the transconductance and the collector current of a bipolar transistor to synthesize extremely linear wide band mathematical operations, as the multiplication needed in the down conversion part of the BITE.

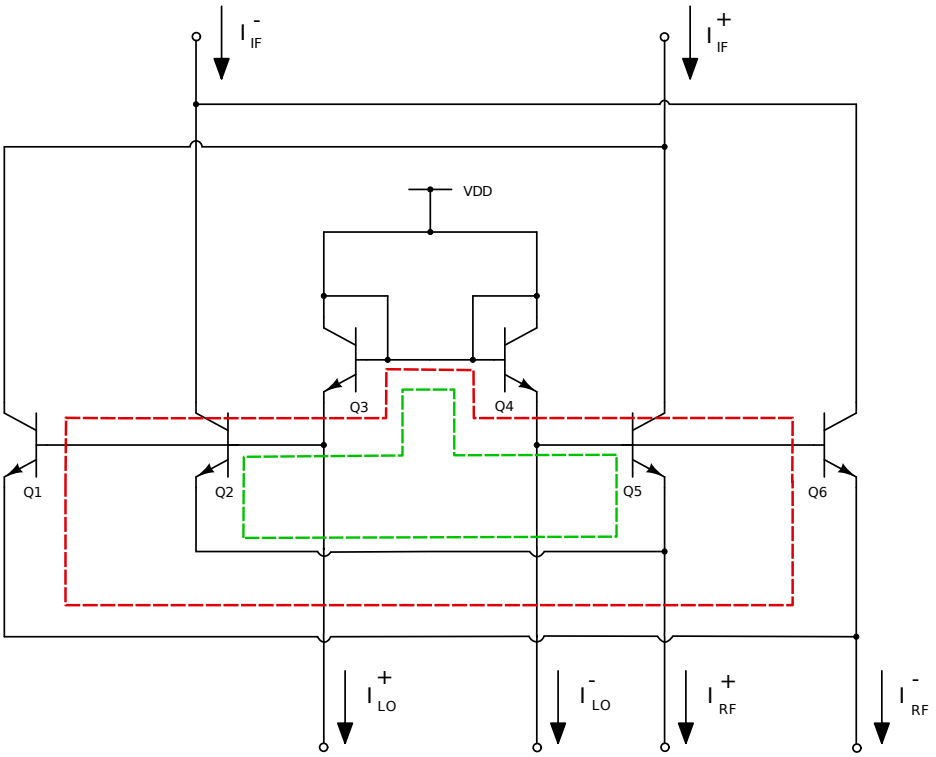

Figure 2.11: Translinear four quadrant curren multiplier

The core of the multiplier is shown in Fig.2.11 where the two nested translinear loops are highlighted. As we will see, the combination of these translinear loops performs a four quadrant multiplication between the RF an the LO current signals. In order to analyze this circuit using the translinear principle, it is useful to define the differential input-output signal as:

$$I_{IF} = I_{IF}^{-} - I_{IF}^{+} \tag{2.22}$$

$$I_{LO} = (I_{LO}^{+} - I_{LO}^{-}) \tag{2.23}$$

$$I_{RF} = (I_{RF}^{+} - I_{RF}^{-}) \tag{2.24}$$

If we neglect the base currents of the transistors, and assume that every transistor is biased with a current $\frac{I_B}{2}$ we have that:

$$I_{IF}^{-} = I_B + \frac{i_{IF}}{2} = I_2 + I_6 \tag{2.25}$$

$$I_{IF}^{+} = I_B - \frac{i_{IF}}{2} = I_1 + I_5 \tag{2.26}$$

$$I_{LO}^{+} = \frac{I_B}{2} + \frac{i_{LO}}{2} = I_3 \tag{2.27}$$

$$I_{LO}^{-} = \frac{I_B}{2} - \frac{i_{LO}}{2} = I_4 \tag{2.28}$$

$$I_{RF}^{+} = I_B + \frac{i_{RF}}{2} = I_5 + I_2 \tag{2.29}$$

$$I_{RF}^{-} = I_B - \frac{i_{RF}}{2} = I_6 + I_1 \tag{2.30}$$

Assuming all the transistor of the circuit are identical and using the translinear principle, we have:

$$I_1 I_3 = I_4 I_6 \tag{2.31}$$

$$I_2 I_3 = I_4 I_5 \tag{2.32}$$

From these equations, we can easily derive the value of each transistor current:

$$I_1 = \frac{I_4 I_6}{I_3} = \frac{I_{LO}^- (I_{RF}^- - I_1)}{I_{LO}^+} \quad \rightarrow \quad I_1 = \frac{I_{LO}^- I_{RF}^-}{I_B} \tag{2.33}$$

$$I_2 = \frac{I_4 I_5}{I_3} = \frac{I_{LO}^- (I_{RF}^+ - I_2)}{I_{LO}^+} \quad \rightarrow \quad I_2 = \frac{I_{LO}^- I_{RF}^+}{I_B} \tag{2.34}$$

$$I_5 = \frac{I_3 I_2}{I_4} = \frac{I_{LO}^+ (I_{RF}^+ - I_5)}{I_{LO}^-} \quad \rightarrow \quad I_5 = \frac{I_{LO}^+ I_{RF}^+}{I_B} \tag{2.35}$$

$$I_6 = \frac{I_3 I_1}{I_4} = \frac{I_{LO}^+ (I_{RF}^- - I_6)}{I_{LO}^-} \quad \rightarrow \quad I_6 = \frac{I_{LO}^+ I_{RF}^-}{I_B} \tag{2.36}$$

The IF port currents are then:

$$I_{IF}^+ = I_1 + I_5 = \frac{I_{LO}^- I_{RF}^- + I_{LO}^+ I_{RF}^+}{I_B} \tag{2.37}$$

$$I_{IF}^- = I_2 + I_6 = \frac{I_{LO}^- I_{RF}^+ + I_{LO}^+ I_{RF}^-}{I_B} \tag{2.38}$$

Hence the differential output current is given by:

$$I_{IF} = I_{IF}^{+} - I_{IF}^{-} = \frac{I_{LO}^{-}I_{RF}^{-} + I_{LO}^{+}I_{RF}^{+} - (I_{LO}^{-}I_{RF}^{+} + I_{LO}^{+}I_{RF}^{-})}{I_B} \tag{2.39}$$

$$= \frac{(I_{RF}^{+} - I_{RF}^{-})(I_{LO}^{+} - I_{LO}^{-})}{I_B} = \frac{I_{RF}I_{LO}}{I_B} \tag{2.40}$$

which is exactly the desired multiplication between the LO and the RF signals[14].

Another way to look at this circuit is to consider it as a quad mixer using a pre-distortion circuit to drive the switches of the quad [8]. In Fig.2.12 the same circuit of Fig.2.11 is shown highlighting all the functional blocks of the frequency multiplier.

The differential input voltage V_{RF} is converted to a differential current I_{RF} which flows through the diodes Q_4 and Q_5, producing a pre-distorted differential voltage V_d. This differential signal is exactly the signal needed by the emitter coupled differential pairs Q_5, Q_2 and Q_1, Q_6 in order to conduct the differential current I_{RF}. In fact a typical emitter coupled pair (ECP) which does not use a degeneration impedance, has an hyperbolic tangent transconductance characteristic. Hence, a large amplitude sinusoidal voltage at the input, such as the LO signal, produces a differential current at the output which is similar to a square wave. This correspond to an abrupt commutation of the emitter coupled switches of the multiplier, hence, to an high influence of the LO third harmonic. However, if a transconductor followed by the pre-distortion circuit is used, the LO signal is converted to a pre distorted one, which is capable to drive the switch in a linear way. In Fig.2.13, a comparison between the input-output signals of an ECP with and without pre-distortion circuit is shown. The effect of the pre-distortion circuit is evident for large input signals when the characteristic of the ECP cannot be approximated as a linear function.

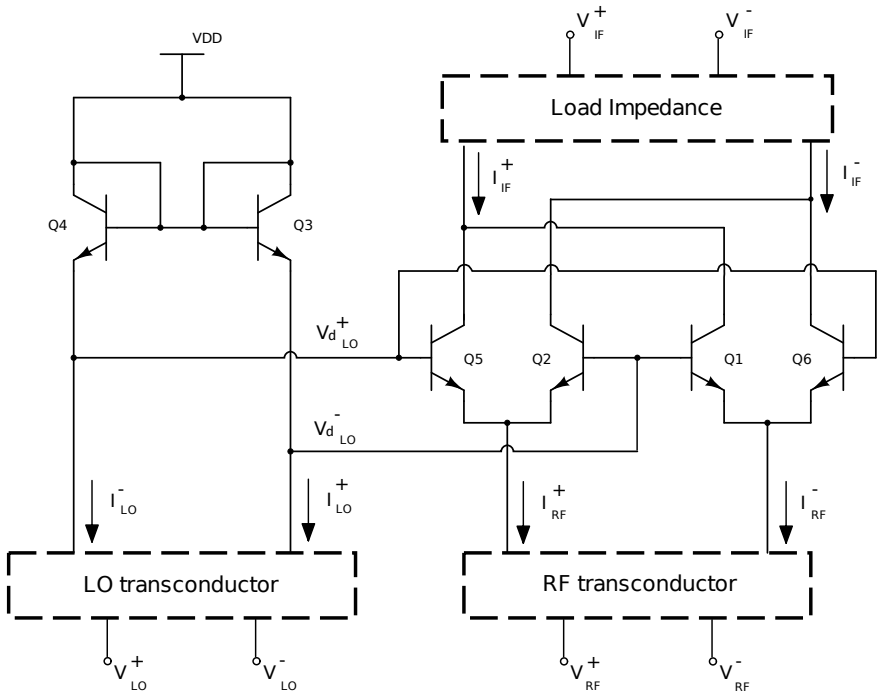

Figure 2.12: Schematic of the four quadrant multiplier as pre-distortion+Quad

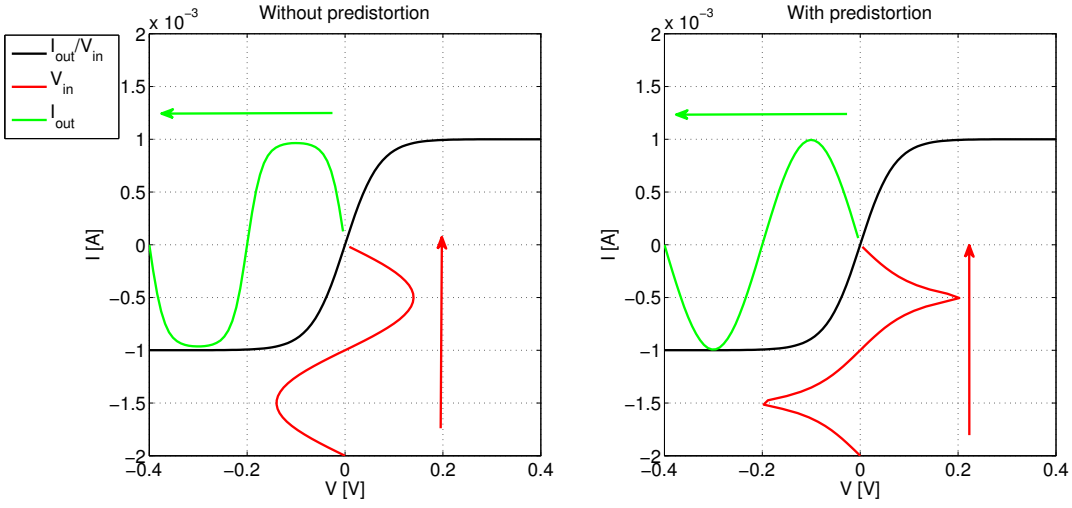

Figure 2.13: Effect of predistortion

2.6 Alternative solutions

A large effort was involved in this work to find a viable solution to down convert the DUT's output signal and avoid the degradation of the measurement introduced by this process. Many different approaches have been explored to analyze their performance. The final topology (Fig.2.12) was chosen because of its performance, robustness against process variation and temperature, and low area implementation. In this section, some of the alternative approaches which have been explored are briefly summarized:

Digital processing of the output signal

The error introduced in the gain and phase measurement by the third harmonic of the LO signal, has a precise mathematical description. For this reason, the first attempt to erase this error source was to estimate its behavior and subtract it from the measured data. In order to achieve a good cancelation of the measurement error, it is mandatory to know which is the effective amplitude of the component introduced by the third harmonic of the LO and which is the phase of the error, in order to sum to the output an error correction signal with opposite phase. This information is analytically derivable from the amplitude variation experienced by the output signal when the DUT sweeps all its bits combinations. In fact, when the maximum, A_{MAX} and minimum, A_{MIN} value of the output signal are known, we can use them to obtain the amplitude of the the desired component and that generated by the LO third order harmonic, which are:

$$S_1 = \frac{A_{MAX} + A_{MIN}}{2} \quad ; \qquad S_{LO} = \frac{A_{MAX} - A_{MIN}}{2}$$

Then, the instantaneous value of the output signal, gives enough information to determine the phase of the error. A simulation made on a fully commutating double balance mixer, used as down converter for the BITE system gives the result in Fig.2.14. The absolute phase measurement error is almost completely erased. Unfortunately, this approach cannot be used, since every different configuration of the DUT's phase shifter, results in a different gain for the

DUT block, which is not known a priori. Hence, it is not possible to precisely estimate the values of S_1 and S_{LO}.

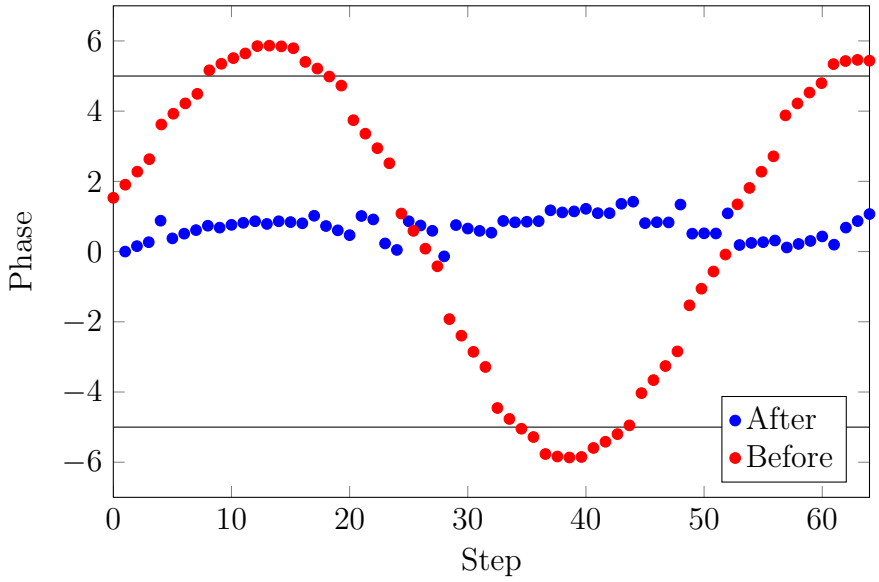

Figure 2.14: Absolute phase error before and after its compensation

Duty cycle variation

The third harmonic of the LO signal, which is the main cause of the measurements errors, can be erase at its source, if the duty cycle of the LO signal is set to particular values. If we consider the Fourier series expansion of the square wave generated by the LO signal having a generic duty cycle D, we have:

$$S_{LO}(t) = (D - 0.5) + \sum_{n=1}^{\infty} 2\frac{\sin(n\pi D)}{\pi n}\cos(2\pi n f_{LO} t) \tag{2.41}$$

where the third harmonic is given by:

$$S_{LO}(t)_3 = 2\frac{\sin(3\pi D)}{\pi n}\cos(2\pi 3 f_{LO} t) \tag{2.42}$$

$S_{LO}(t)_3$ is zero if D is set to $\frac{1}{3}$ or to $\frac{2}{3}$.
A practical and space efficient way to obtain a LO signal with the desired duty cycle, is to use an unbalanced emitter coupled pair without degeneration,

where one of the two transistor has an emitter area bigger than the other. In this way, the voltage to current characteristic is shifted on the voltage axis by:

$$\Delta V = V_T \ln(N) \tag{2.43}$$

Where N is the ratio between the areas of the transistors. If the LO signal amplitude is known, it is possible to find a value for N, for which the output signal has the desired duty cycle. However, since this technique is highly dependent on the LO signal amplitude and temperature through V_T and other methods to generate the desired signal are too complicated for the purpose of this work, this approach has been discarded.

High frequency LO signal

If the LO signal is chosen to be $\frac{3}{2}f_{RF}$ instead of $\frac{f_{RF}}{2}$, we can immediately see from the output spectrum of the down converted signal in Fig.2.15, that no spurious components at frequency $\frac{f_{RF}}{2}$ are superimposed to the desired signal. Hence, there is not amy degradation of the BITE due to the third harmonic of the LO.

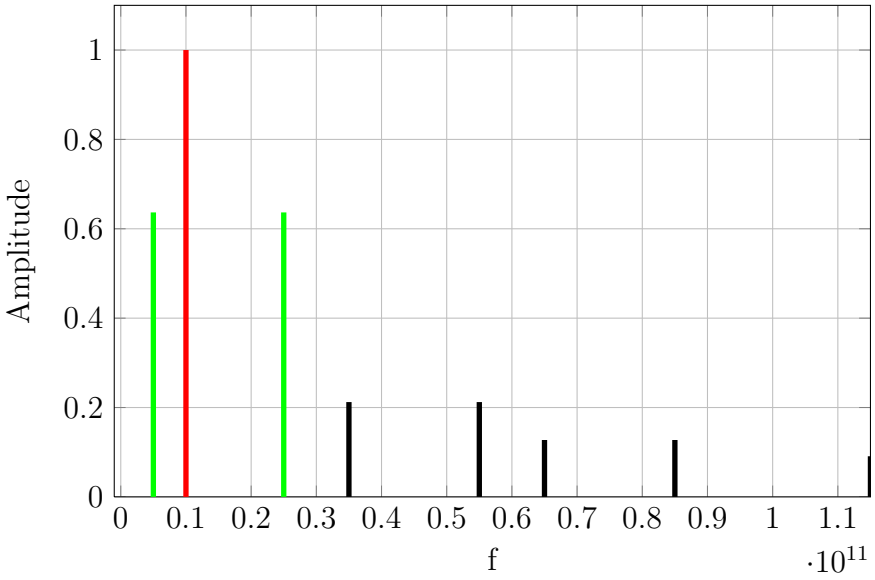

Figure 2.15: Output spectrum of the down conversion with $f_{LO} = \frac{3}{2}f_{RF}$

However, using an LO signal with three times the input test signal frequency, implies the use of a frequency tripler that, if implemented in the same way of the frequency doubler, requires several filter stages or tuned loads, to get rid of the generated spurious components. The implementation of such device has been carried on to verify its performances with good results. The analog multiplier solution was chosen as it requires less silicon area.

CHAPTER 3

Design

In this chapter, the the test circuits design is described in detail. Each block of the system is discussed in a separate section, in a order that takes into account the dependencies and consequently the design constrains of one circuit to the.

3.1 Design goals

The design procedure must be done having in mind all the specifications of the project and the specifications that are not set but desired. The goals for the test system have already been introduced in Chapter 1 and are:

1. The chip must occupy the least possible silicon area..
2. The relative phase error in the measurement of the DUT, must be less than 5^o.
3. The error in the measurement of the relative gain, must be less than 1dB.
4. The temperature range where the measurement must be accurate is from 0^o to 85^o.

5. The input and the output of the test system must be matched to 100Ω.
6. The voltage supply is 3.3V.
7. Power consumption is unimportant since the BITE circuits are disabled during normal operation.

The first condition is related to the fact that the measurement system must be replicated for every element of the antenna array and is necessary only during the test and calibration of the radar system. For this reason, it should be as small as possible, to reduce the costs. The main intrinsic limitation imposed by this condition is that no coils can be used. Accordingly, the only components available for the design are resistors, capacitors and transistors of moderate size. Constraints on power consumption are not directly given, since the considered circuit is switched on only when the DUT is tested. However, the more current flow through the circuit, the wider its components and connections must be, setting an indirect limitation on the power consumption. The second and third conditions, lead to certain design choices already introduced in the previous chapter, especially for what regards the down converter multiplier. The fourth condition is taken into account by paying attention to the parameters of the circuit that change the most with the temperature, as the thermal voltage of the bipolar transistors. Finally, the fifth condition which is on the matching of the input and output of the test system will be treated in the next sections. Some further parameters of the circuit that should be minimized if its possible, are the noise introduced by the circuit and the number of spurious components at the output of the test system.

3.2 Device Under Test

Since the DUT is the subject of the measurements performed by the BITE, it is mandatory to know its detailed characteristics in order to choose the most suitable topology and specifications for the blocks of the measurement system. As introduced in Chapter 2, the DUT is a two port device, formed by the series of a LNA a PGA and a phase shifter.

Parameter	Min	Nom	Max	Units
Power gain	-15	-	3	dB
Phase shift	0	-	180	deg
IIP3	-	0	-	dBm
1dB Cmp	-	-10	-	dBm
Zin	-	100	-	Ω
Zout	-	100	-	Ω
NF	-	10	-	dB

Table 3.1: DUT parameters

Since the complete circuit of the DUT was not available during the BITE design, all the blocks of the measurement system have been designed starting from the DUT properties already mentioned in Chapter , shown again for convenience in Tab.3.1. From these parameters, a model of the DUT has been synthesized combining the available models of an LNA, a transmission line, and an attenuator as shown in Fig.3.1. Phase shift and gain of the model are varied by changing the transmission line length an modifying the attenuator loss respectively. Finally, the non linearities, the input impedance and the noise figure are set in the LNA properties since all the other blocks are ideal.

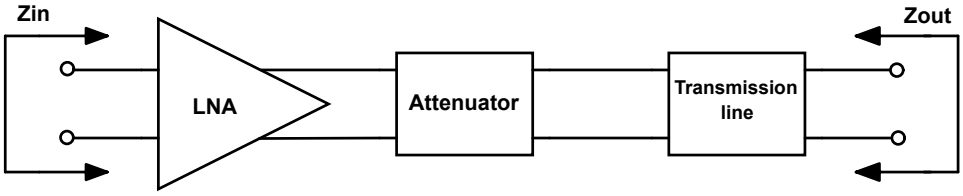

Figure 3.1: Synthesized model of the DUT

Determining the input and output signal properties for the device under test, is a good starting point for the design of the test system since they are the signal generated by the frequency doubler and the signal that must be down converted by the analog multiplier respectively. From Tab.3.1, the 1dB compression point of the DUTis -10dBm hence, the input test signal should be conservatively

smaller than -10dBm but not too small since the resolution of the BITE is enhanced if the test signal is large. In this work, the signal at the input of the DUT is chosen to be at -20dBm which automatically sets the power span of the signal at the output of the DUT from -35dBm to -17dBm.

3.3 Emitter follower buffer

In the design of the BITE, is necessary to make the properties of each stage, independent from the other ones. Typically, in voltage mode circuits, the input stage needs to be driven by a small impedance signal source and the load, where the output signal is taken, should not be further loaded by the following stage. Both of these tasks can be addressed using a voltage buffer which has an high input impedance, unity voltage gain, and low output impedance. In this work, we implement voltage buffers using the common collector stage. The typical configuration for the common collector is the one shown in Fig.3.2. This circuit works using negative feedback given by the impedance seen from the emitter of Q_1 which is the impedance seen at the collector of Q_2, in parallel with the load impedance. If an increasing voltage signal is applied at the base of Q_1, the collector current flowing through Q_1 increases as well and this results in an increasing voltage on the load which decrease the base emitter voltage of Q_1. For this reason, this circuit is also known as emitter follower. What we need to know to properly size this circuit is the input signal amplitude and the load of the buffer. The first one is needed to set the bias voltage, V_b1 , hence the collector-emitter voltage, in order to avoid the saturation of Q_1 and the second one is needed to chose the proper bias current for the stage. As long as the ratio between the amplitude of the voltage signal that needs to be buffered and the load impedance, which is the current that the buffer needs to provide, is low compared to the bias current of Q_1, the buffer properly behaves in a linear way. Conversely, if the current that the emitter follower must provide is comparable with the bias current, the buffer introduces distortion.

A simple large signal analysis, which is sufficient to dimension the emitter follower for the scope of this work, can be done using a low frequency approach

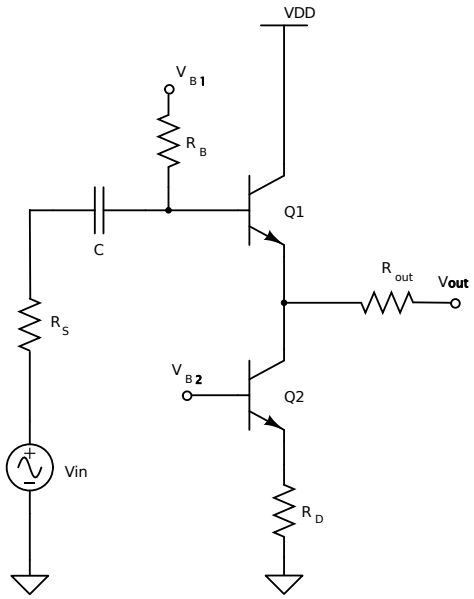

Figure 3.2: Emitter follower circuit

and exploiting the exponential characteristic of the collector current as a function of the base-emitter voltage. Assuming that we need to buffer a signal having voltage amplitude V_{in}, we want the same signal on the load resistance R_L. We assume that the small signal impedance seen at the collector of Q_2 is very high, since it is approximately the output resistance of Q_2 multiplied by $(1 + g_m R_D)$, thus, all the signal current flows through the load. For this reason, the maximum and the minimum currents that Q_1 must provide, are:

$$\hat{I}_C = I_B + \frac{V_{in}}{R_L} = I_B + i_o$$

$$\check{I}_C = I_B - \frac{V_{in}}{R_L} = I_B - i_o$$

The base-emitter voltages needed to produce such currents can be derived using the exponential characteristic of the bipolar transistor :

$$\hat{V}_{be} = nV_T \ln\left(\frac{\hat{I}_C}{I_s}\right)$$

$$\check{V}_{be} = nV_T \ln\left(\frac{\check{I}_C}{I_s}\right)$$

hence the variation of the base-emitter voltage is within the span:

$$\Delta V_{be} = \hat{V}_{be} - \check{V}_{be} = nV_T \ln\left(\frac{\hat{I}_C}{\check{I}_C}\right)$$

Since the V_{be} to I_C characteristic can be considered linear only under the small signal hypothesis, in order to have a proper voltage buffer, the bias current must than satisfy:

$$I_B > \frac{V_{in}}{R_L} \cdot \frac{1 + e^{\frac{\Delta V_{be}}{nV_T}}}{e^{\frac{\Delta V_{be}}{nV_T}} - 1} = \frac{V_{in}}{R_L} \cdot K \tag{3.1}$$

where ΔV_{be} is chosen to be few tenth of millivolt in order to have good performance. In Fig.3.3 the ratio between the input and output signal amplitude is traced as a function of K. As we can see, the emitter follower tends to the ideal buffer behavior as K, i.e. the bias current is increased. A typical value chosen for K is between 7 and 8.
In this work, emitter followers are basically used for three different purposes: Provide a high input impedance voltage buffer, match the input impedance of a circuit and match the output impedance of a circuit.

High input impedance buffer

When we design an analog circuit, we usually want the properties of its output signal to be independent from the external load impedance. For this rea-

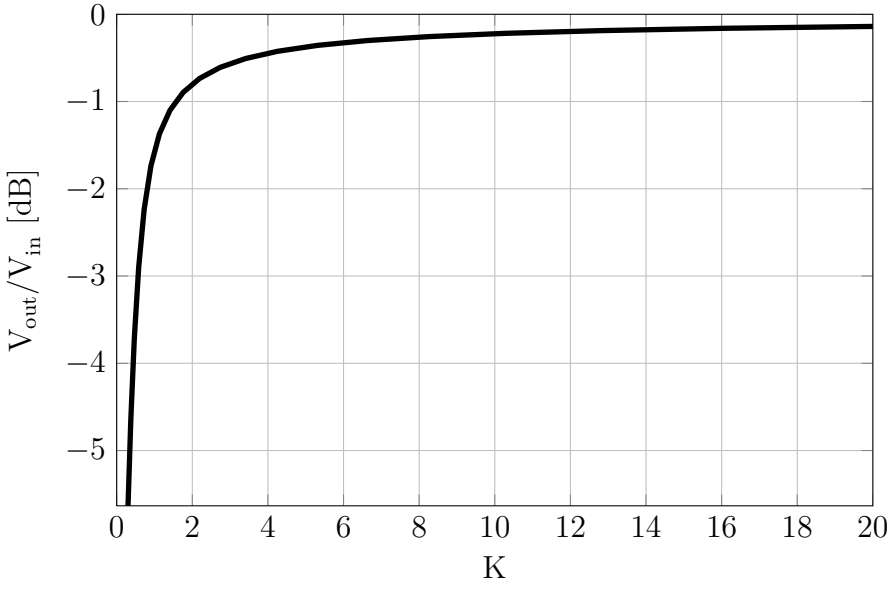

Figure 3.3: $\frac{V_{out}}{V_{in}}$ in function of the parameter K

son, emitter followers are typically used as output buffers since their input impedance is typically high. At high frequencies, can be approximated by:

$$Z_{Qin} = r_b + R_L + \frac{r_\pi}{1 + sr_\pi C_\pi}(g_m R_L + 1) \backsimeq r_b + R_L + \frac{1}{sC_\pi}(g_m R_L + 1) \quad (3.2)$$

Where r_π is neglected at high frequencies, since the capacitive contribution of $Z_\pi = r_\pi // \frac{1}{sC_\pi}$ is predominant. Consequently, if we refer to Fig.3.2 a voltage signal source applied at the input of the emitter follower sees an impedance given by :

$$Z_{in} = Z_{Qin} // R_B \backsimeq \frac{R_B}{1 + sR_B \frac{C_\pi}{(g_m R_L + 1)}} = \frac{R_B}{1 + sR_B C_{eq}} \quad (3.3)$$

Hence, if we use a high value bias resistance, R_B, Z_{in} remains sufficiently high impedance to have negligible effect on the circuit that we want to buffer.

Input impedance matching buffer

When the input impedance matching is requested at the input of a circuit, many techniques exist to provide it by the use of coils and transformers. How-

ever, this kind of matching is typically narrowband and request a substantial amount of area to implement the coils, hence it is not a viable solution for the BITE. In this work the matching condition, which is usually requested at 50Ω, is forced by choosing R_B equal to 50Ω. Using this approach, the magnitude of the input scattering parameter, becomes:

$$|S_{11}| = \left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right| \backsimeq \left|\frac{\omega R_S C_{eq}}{\sqrt{4 + (\omega R_S C_{eq})^2}}\right| \tag{3.4}$$

which starts from zero and rises with frequency depending on the value of $R_S C_{eq}$. However, considering the band of this application and typical values of $R_S C_{eq}$, a good matching is guaranteed.

Output impedance matching buffer

Every output stage which is connected to a transmission line or to an off-chip connection, must be matched in order to avoid reflections. This task is accomplished by using an emitter follower as the output stage. The emitter follower has an output resistance given by $\frac{1}{g_m}$, hence, we only need to provide the remaining resistance by connecting a resistance R_{OUT} in series.

3.4 Frequency doubler

The frequency doubler has been the first block to be designed. This circuit needs to produce a fixed amplitude RF signal having a fundamental frequency which is double respect to the LO and IF signals. From the considerations made on Tab.3.1, we have already determined the desired output signal amplitude. Hence, we need to define the most suitable circuit topology, the active and passive components sizes and the desired input signal that must be generated by the polyphase filter, which will be designed next.
As we have seen in Chapter 2, the frequency doubler mixer uses two quadrature differential signals with the same amplitude as inputs. Having the same amplitude for the LO and the IF signal of a mixer is an issue since the LO signal must be large enough to completely commutate the switches of the mixer and

the IF signal should be sufficiently small, in order to remain in the linearity region of the mixer's transconductor. This issue can be addressed in two different ways: one can design the quadrature signals generator, in order to generate two signal having the amplitude needed for the IF signal and than amplify the LO signal. Otherwise, two large quadrature signals can be generated by the previous stage and the linear region of the IF input transconductor can be extended. Since the linearity region of the transconductor can be easily extended in a more compact way than adding an extra stage to amplify the LO signal and since the LO and IF signals path need to be as similar as possible in order to maintain their quadrature property, the latter approach has been chosen.

3.4.1 Transconductor

The transconductor of the quad mixer strongly influences the performance of the frequency doubler, in fact, once its properties are set, the bias current of the switching cell (unless current bleeding techniques are used), the maximum achievable linearity and the value of the maximum load impedance are automatically imposed, unless the LO port is overdriven [15]. The choice of the circuit topology for the transconductor is related to the maximum available voltage head-room unless folding techniques are used. From the DUT's maximum input signal amplitude derived from Tab.3.1 we can follow the reverse path of the signal in order to estimate the voltage swing at the mixer load. In section 3.3, we have chosen a signal having -20dBm power (referred to a 100Ω differential impedance) to drive the DUT. The mixer output signal will be buffered using an emitter follower which does not further load the mixer, isolate the test system from the DUT when it is switched off and matches the output of the frequency doubler to the input of the DUT. A 6dB voltage attenuation has to be taken into account due to the matching. The result is a 180mV peak to peak differential output swing for the mixer. This means that every single ended output should be able to swing between 45mV and -45mV around its bias voltage. Hence, a minimum DC voltage drop of 45mV is needed across the load. In the design, it was sized to be close to 100mV, in order to take into account possible variations of the conversion gain and input signal.

The voltage drop across the switching cell has its minimum value dependent on the amplitude of the LO signal and its maximum value which is given by the breakdown voltage of its transistors; a reasonable value,which supposes of a -1dBm LO signal, is 1V.
The voltage headroom left for the transconductor, if the supply voltage is set to 3.3V, is 2.2V, which is enough to stack two transistors and have some room left for the current sources emitter degeneration resistors. This means that we can use transistor based current sources which have a very high output resistance to bias the input emitter coupled pair. A resistive differential degeneration, R_D, can be exploited to linearize the tranconductor, as shown in FIg.3.4.

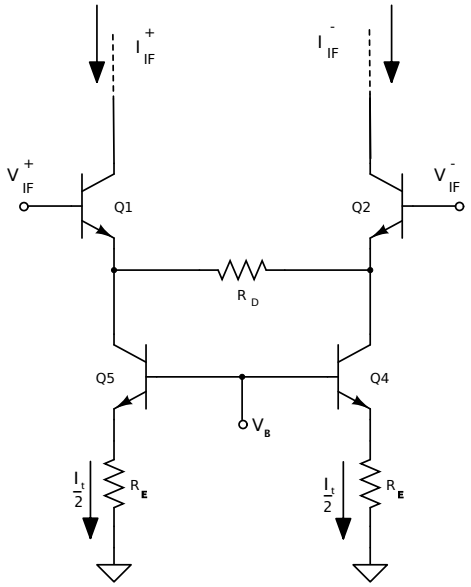

Figure 3.4: Transconductor circuit topology

From the differential signal stand point, a small signal analysis can be performed, using the equivalent model depicted inFig.3.5 which is equivalent to the model of a common emitter stage having emitter degeneration. This model is derived from the small signal model of the entire differential pair by dividing it in two identical parts, since a differential signal sees an equivalent AC ground in the middle of R_D which can than be divided in two identical resistors: $R'_D = \frac{R_D}{2}$. This model, makes also the assumptions that the current sources

Q_4 and Q_5 have an infinite output impedance, which is a good approximation at low frequencies, when the output impedance is mainly resistive and given by:

$$R_o = r_o(1 + g_m R_E) \tag{3.5}$$

but is not completely true at high frequencies, when the capacitive part of the output impedance due to C_μ become important.

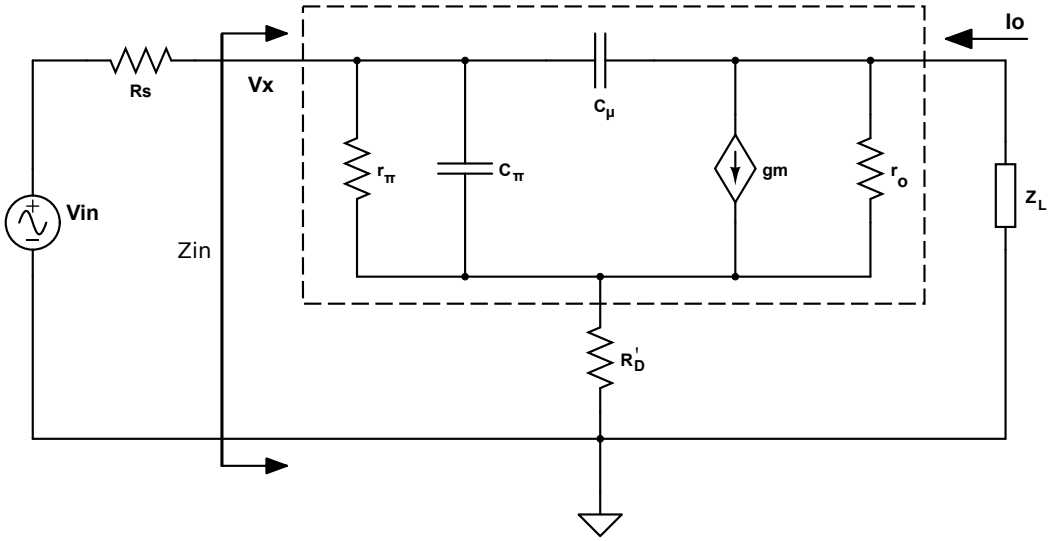

Figure 3.5: Single ended small signal equivalent circuit of the transconductor

The model can be further simplified if we also add some information about the load of the transconductor which is the switching cell of the mixer. Every differential output of the transconductor, goes directly to a switching differential pair, which is supposed to switch as fast as possible, hence, we can look at this load as a cascode stage which acts as a current buffer for the transconductor and isolate the output of the mixer from the output of the transconductor. The consequence on the model in Fig. 3.5 is that the Miller capacitance C_μ has very little effect and can be neglected. Furthermore, the input impedance of a cascode stage is small. Hence Z_L is considered small compared to r_o and neglected too. We now calculate the small signal transconductance, G_m of the simplified model, dividing it in the V_{in} to V_x part and the V_x to I_o part.

$$\frac{V_{in}}{V_x} = \frac{Z_{in}}{Z_{in} + R_S} \tag{3.6}$$

where Z_{in} is the impedance seen at the base of the input transistors Q_1 and Q_2:

$$Z_{in} = Z_\pi + \frac{R_D}{2}(1 + g_m Z_\pi) \tag{3.7}$$

Z_π is the impedance given by the parallel of C_π and r_π:

$$Z_{in} = R_{in} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}} \tag{3.8}$$

Where :

$$R_{in} = [r_\pi + R'_D(1 + g_m r_\pi)]$$

$$\omega_{p1} = \frac{1}{C_\pi r_\pi}$$

$$\omega_{z1} = \left[1 + r_\pi \left(g_m + \frac{1}{R'_D}\right)\right] \frac{1}{C_\pi r_\pi} = \left[1 + r_\pi \left(g_m + \frac{1}{R'_D}\right)\right] \omega_{p1}$$

If we consider typical values of r_π and g_m, the zero is at much higher frequency than the pole, hence its influence is not taken into account. Than, if the signal generator at the input has a purely real output impedance we have:

$$\frac{V_{in}}{V_x} = \frac{R_{in}}{R_S + R_{in}} \cdot \frac{1}{1 + \frac{s}{\omega_{p1}} \frac{R_S}{R_S + R_{in}}} \tag{3.9}$$

The bandwidth of the transfer function is than limited by the pole:

$$\omega'_{p1} = \omega_{p1}(1 + \frac{R_{in}}{R_S}) \tag{3.10}$$

which is shifted at higher frequencies if compared to ω_{p1} especially when $\frac{V_{in}}{V_x}$ is maximized reducing the source resistance R_S. Considering now the transconductance from V_x to I_o we have :

$$\frac{I_o}{V_x} = G_x \cdot \frac{1}{1 + \frac{s}{\omega_{p2}}} \tag{3.11}$$

where G_x and ω_{p2} are respectively:

$$G_x = \frac{g_m}{1 + R'_D \left(g_m + \frac{1}{r_\pi}\right)}$$

$$\omega_{2p} = \frac{1 + R'_D \left(g_m + \frac{1}{r_\pi}\right)}{R'_D C_\pi}$$

Combining the two gains toghter, we obtain:

$$G_m(s) = \frac{I_o(s)}{V_{in}(s)} = G_x \frac{R_{in}}{R_S + R_{in}} \cdot \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{3.12}$$

Some observations can be made upon this transfer function. The relative position of ω'_{p1} and ω_{p2} can be determined by calculating their ratio:

$$\frac{\omega'_{p1}}{\omega_{p2}} = \frac{R'_D}{r_\pi} \frac{1 + \frac{r_\pi + R'_D(1 + g_m r_\pi)}{R_S}}{1 + R'_D \left(g_m + \frac{1}{r_\pi}\right)} \approx \frac{1 + g_m R'_D}{\frac{R_S}{R_D} + g_m R_S} \tag{3.13}$$

Typically R_S and R'_D have similar values, hence the two poles are very close together .

The DC transconductance, depends on the source resistance R_S, the transistor transconductance g_m and the degeneration resistance R'_D. It is customary to use low output impedance sources to drive an emitter coupled pair, hence the transconductance is mainly controlled by g_m and R'_D.

The tail current of the transconductance stage of a mixer, is usually chosen as high as the power consumption limit allows, since increasing the bias current of the transistors, reduces the IM3 [16] of the differential pair and the shot noise introduced by the base-emitter junctions [17]. In this work, no power constraints are imposed, but the layout of the circuit scales with the used power. Hence, a I_T current of 4mA is chosen. This choice sets the transconductance of the input transistors Q_1 and Q_2: to:

$$g_m = \frac{I_T}{2nV_T} \tag{3.14}$$

where n is the ideality factor which can be used to model the effect of the emitter resistance which create an intrinsic degeneration [4] and is typically close to 1.4 for a minimum size transistor. If we now suppose that the switching cell is ideal, we can write the conversion gain of the frequency doubler recalling Eq.2.13 which assumes quadrature input signals :

$$G_{DBM} = \frac{8}{3\pi} G_m R_L = \frac{\Delta V_{RF}}{\Delta V_{IF}} \tag{3.15}$$

where ΔV_{RF} and ΔV_{IF} are the peak to peak amplitudes of the RF and IF signals. Since inductors cannot be used, we have already seen that the minimum voltage drop on the load impedance R_L, is $\frac{\Delta V_{RF}}{4}$, but can be higher if a loss of overhead is tolerable, hence we can write:

$$R_L \frac{I_T}{2} = \Delta V_{LOAD} \tag{3.16}$$

where ΔV_{LOAD} is the voltage drop on the load. Using the approximate low frequency expression for G_m from (3.12) and the (3.14) we get:

$$G_{DBM} = \frac{8 R_L I_T}{3\pi(2nV_T + I_T R'_D)} \tag{3.17}$$

Since the current that flows through the transistors is fixed, once we choose a value of the IF signal amplitude which sets G_{DBM}, a trade off exists between the value of the load resistance R_L that establish ΔV_{LOAD} and the degeneration resistance, R'_D. It is easy to see that, the bigger is the degeneration resistance, hence the more linear is the transconductor, the bigger must be the voltage

drop on the load to achieve the same conversion gain. Once R'_D is determined to achieve the desired linearity, we can than use (3.16) to derive the value for R_L. In order to choose the proper value for the degeneration resistance, we need to know the amplitude of the signal at the input of the transconductor. Both the LO and the IF input are identical despite for their relative phase, hence they will also have the same amplitude, which is set to make the switch transistor commutate properly. For this reason, it is clear that the design flow must move to the switching cell in order to proceed.

3.4.2 Switching cell

The quad switching cell, introduced in Chapter 2, is composed of two emitter coupled pairs driven by the LO signal. From the hyperbolic tangent DC characteristic of the emitter coupled pair, we see that the tail current of the pair flows practically in only in one of the transitors for large values of the differential input voltage. The larger is the sinusoidal LO signal, the steeper the commutation of the switches, and the more ideal the switching behavior of the emitter coupled pair. However this holds up for moderate amplitudes of the LO signal. At large LO amplitudes transistor may enter the saturation region and an excessive current could flow through the base-emitter capacitance, degrading the linearity IM3 of the mixer [18]. Furthermore, since V_{IF} and V_{LO} have the same amplitude, if a large LO signal is chosen, we need a high value of the degeneration resistor (or a high bias current) in order to make the transconductor IIP3 higher. An analytical, low frequency formulation of the conversion gain of the switching cell can be derived[19]:

$$G_s = \frac{1}{2\pi} \int_0^{2\pi} \tanh\left[\frac{V_{LO}}{V_t}\sin(x)\right] \sin(x) dx \tag{3.18}$$

As the LO power is increased, the conversion gain tends to $\frac{2}{\pi}$. In Fig.3.6, (3.18) is shown together with the simulated conversion gain as a function of the LO power, for different emitter lengths. We can observe that the conversion gain deviates from the calculated one at low LO powers, especially for low emitter areas.

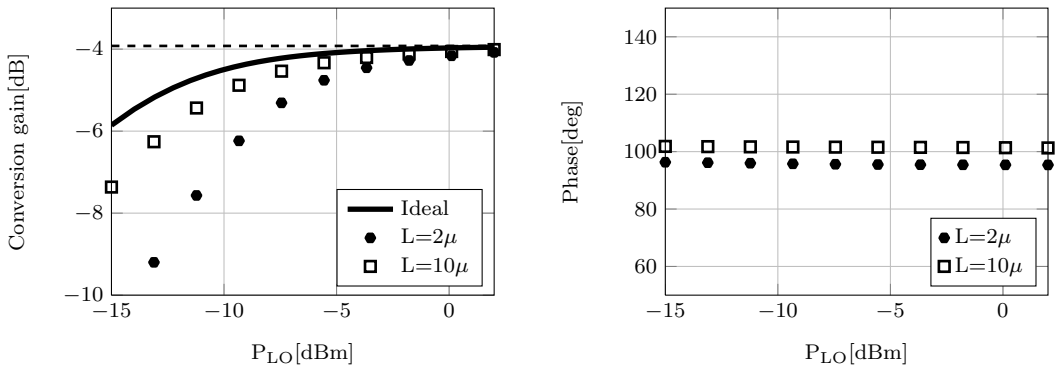

Figure 3.6: Conversion gain and phase, in function of the LO power

The design choice of the LO power, is: −3dBm. This value is chosen because the conversion gain does not improve too much if the LO amplitude is further increased. Moreover, choosing a relatively low level of LO power, loosen the request on the transconductor IIP3.

Once the LO power is determined, ΔV_{IF} is fixed, and we can move again to the sizing of the transconductor degeneration resistances and the load of the mixer. −3dBm corresponds to a IF signal amplitude of $\backsim$ 300mV, a closed form for the calculation of the characteristic of the degenerated emitter pair does not exist, since the equations resulting from the circuit analysis are transcendental. Hence, the rule of thumb which says that the linear span of linear operation is extended by an amount of $R_D I_T$ is used:

$$R'_D = \frac{350\text{mV}}{4\text{mA}} = 87.5\Omega \tag{3.19}$$

Which we approximate conservatively with 100Ω. Substituting R'_D and $G_{DBM} = \frac{\Delta V_{RF}}{\Delta V_{IF}} \approx 0.3$ in (3.17) finally gives:

$$R_L = \frac{3\pi G_{DBM}(2nV_T + I_T R'_D)}{8I_T} \approx 40\Omega \tag{3.20}$$

3.4.3 Load impedance

Up to this point, we only have take into account the frequency components of interest. However, as we have seen in Chapter 2, many spurious components

are generated by the mixer, which are not of interest and may degrade the measurements. For this reason, since a tuned load cannot be used, a capacitor in parallel with the load resistance of every differential output is added. The -3dB frequency of this first order low pass filter is set to 20GHz, in order to attenuate the high frequency components and leave almost unchanged the desired ones that span from 8GHz to 12GHz.

3.4.4 Output buffer

The voltage buffer at the frequency doubler's output has three tasks: the first one is to avoid the excessive load to the mixer output by presenting a high input impedance; the second one, is to isolate the test system from the DUT, when it's switched off and the third one is to match the output impedance of the frequency doubler to the input one of the DUT. Using Eq.3.1, the bias current for the emitter follower is set in order to make every one of the two output emitter follower, capable of driving V_{RF} on their the load impedance. Two resistances are than placed in series to the output in order to match it.

3.5 Quadrature signal generator

The design of the polyphase filter is based on the specifications given on the input signal of the frequency doubler. We need to generate a pair of differential signals in quadrature having an amplitude of 300mV, of driving the frequency doubler IF and LO ports and the analog multiplier LO port. The blocks of the quadrature signal generator are: the input buffer, which must be matched to the 100Ω output impedance of the off-chip signal generator, the polyphase filter which generates the desired quadrature signals and the output buffers which drive the BITE's mixers. The design starts from the choice of the number of stages for the polyphase filter. In Chapter 2, we have already analyzed the behavior of a single stage polyphase filter and we have seen that the phase shift between the two differential signal at the output varies with frequency. This variation implies a DC voltage offset at the up converting mixer load. From (2.18) the DC offset is calculated to be 20% of the signal amplitude at

the up converting mixer's load, which corresponds to an approximative offset of 20mV. This offset can be totally affordable from overhead considerations. Consequently, a single stage polyphase filter is chosen. The capacitors, C and resistors, R values for the polyphase filter must be now determined. Theoretically, every pair of R and C which satisfies the relation:

$$RC = \frac{1}{2\pi\sqrt{f_l f_h}} \tag{3.21}$$

generates the desired quadrature signals at the output of the filter. However, if we make the assumption that the filter is loaded with a high impedance, and we calculate the input impedance seen by every buffer at the input of the polyphase filter, the result is the parallel of the series of R and C:

$$Z_{in}(s) = \frac{1 + sRC}{s2C} \tag{3.22}$$

The current absorbed by the filter when we apply a sinusoidal signal having amplitude V_{in} and frequency f_c at its input is:

$$I_{in}(j\omega_c) = V_{in}\frac{2j}{(1+j)R} = \frac{\sqrt{2}V_{in}}{R}e^{j\frac{\pi}{4}} \tag{3.23}$$

which is a current signal having amplitude $\frac{\sqrt{2}V_{in}}{R}$ and phase $\frac{\pi}{4}$. We can immediately see from this result, and from the previous section on voltage buffers, that the choice of R, changes the sizing of the input buffer for a given signal amplitude. Particularly, if a low value is chosen for R, the input buffer will need a high bias current to work properly[20]. On the other hand, if the value of R is too high, any voltage buffer at the output of the filter which have finite input impedance, will cause a signal attenuation due to the voltage divider at its input. In this work, C and R are chosen to be respectively 100fF and 344Ω. The input buffer is than dimensioned using Eq. 3.1, in order to drive the −3dB signal on the load impedance give by the filter, hence the bias current for each of the two input emitter follower, is set to 7mA. The four output buffers have relaxed specifications, since they need to drive three emitter coupled pair which have high input impedance. For this reason, a 2mA bias current is sufficient.

3.6 Down conversion mixer

The down conversion of the signal at the output of the DUT is performed by means of a four quadrant Gilbert multiplier, which has already been introduced in Chapter 2. Now, we need to determine a suitable transconductor for the LO and the RF voltage signals and properly choose the system parameters, in order to achieve the desired measurement performance. From the circuit schematic in Fig.3.7 we can see that the voltage overhead left for the LO transconductor is approximately $2.45V$ and the overhead left for the RF transconductor, if the stages are DC coupled, is reduced by one base-emitter voltage, hence $1.6V$.

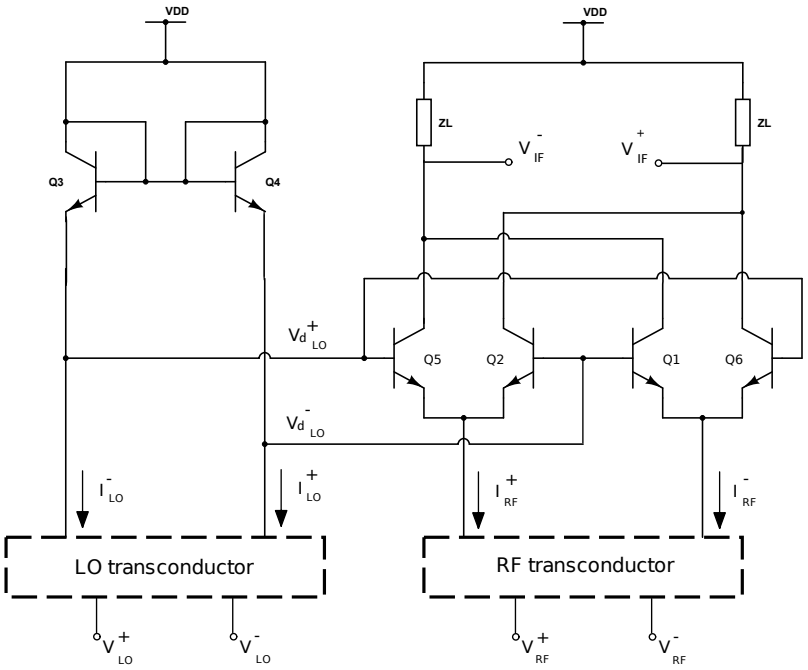

Figure 3.7: Analog multiplier cell

3.6.1 LO transconductor

Starting from the LO transconductor, which drives the switching cell of the analog multiplier, it is important to understand that the transistors of the emitter coupled pair, which implement the switches, will carry exactly the

same current as the one carried by the pre-distortion diodes (if the RF signal is switched off), hence, their tail current will be commutated in a sinusoidal fashion, only if the current in pre-distortion diodes is sinusoidal. In addition, the conversion gain of the multiplier, reaches its maximum value when the tail current of the switches is completely steered from one transistor of the pair to the other. This means that the LO transconductor, which generates the current that flows in the diodes, should be as linear as possible, and should have the maximum possible transconductance. Since the voltage overhead for this transconductor is comparable to the one available for the transconductor of the frequency doubler, the same circuit topology, shown in Fig.3.4 is used. However the goal of the LO transconductor, is different from the frequency doubler one. Hence, it must be designed in a slightly different way. Once the bias current of the transistors is set, the key component in the design of the transconductor is the degeneration resistance. To properly size it, we must understand the specifications on the switching linearity required to satisfy the measurement requirements. In the chapter 2, we have seen that the third harmonic introduced by the abrupt switching of the transistor intermodulates with the RF signal and is generates measurement errors. It is useful to derive the maximum third order harmonic component produced by the switches which is tolerable by the measurement system, without degrading its performance. We consider the product between the following signals, which represent the down conversion process and where a generic third order harmonic of amplitude A is taken into account:

$$S(t) = \sin(2\omega_0 t + \Delta\phi) \cdot [\sin(\omega_0 t) + A\sin(3\omega_0 t)] \tag{3.24}$$

The components that resulting at ω_0 are :

$$S(t)|_{\omega_0} = \frac{1}{2}[\cos(\omega_0 t + \Delta\phi) - A\cos(\omega_0 t - \Delta\phi)] \tag{3.25}$$

This is a sinusoidal signal at ω_0 having amplitude and phase dependent from A and $\Delta\phi$:

$$\frac{1}{2}\sqrt{(1-A)^2 + 4A\sin^2(\Delta\phi)} \cdot \cos\left[\omega_0 t + \arctan\left(\tan(\Delta\phi)\frac{1+A}{1-A}\right)\right] \tag{3.26}$$

We can now derive that the maximum value for the parameter A, in order to satisfy the measurement specifications. Maximum gain and maximum phase errors can be seen as two independent restrictions on the maximum value of A. The more stringent one has to be kept as a design requirement. From (3.26) we observe that the maximum and minimum signal amplitude are given respectively by:

$$|\hat{S(t)}|_{\omega_0}| = \frac{1+A}{2} \quad \text{when} \quad \Delta\phi = k\pi \tag{3.27}$$

$$|\check{S(t)}|_{\omega_0}| = \frac{1-A}{2} \quad \text{when} \quad \Delta\phi = \frac{\pi}{4} + k\pi \tag{3.28}$$

From the specifications of the project, we know that the gain of the DUT, must be measured with a maximum error of 1dB, hence the following must hold true:

$$20\log\left(\frac{1+A}{2}\right) - 20\log\left(\frac{1-A}{2}\right) < 2 \quad \rightarrow \quad A < -18.8\text{dB} \tag{3.29}$$

As opposed to the amplitude, the phase of this signal, varies in a more complex way which has its maximum and minimum that change position with $\Delta\phi$ and A and consequently it is difficult to find an analytical solution, for this reason, a graphical approach is used. The maximum error in the phase measurement in function of A is traced in 3.8.
The condition on A in order to have an error on the phase measurement, smaller than 5^o is :

$$A < -21.3\text{dB} \tag{3.30}$$

The phase measurement condition is more strict than the one on the gain. Hence -21.3dB is the maximum value possible for A.
Now that we know which is the theoretical limit on the third order component introduced by the switches, it is possible to design the LO driver in order to find a compromise between the conversion gain and the measurement performances.

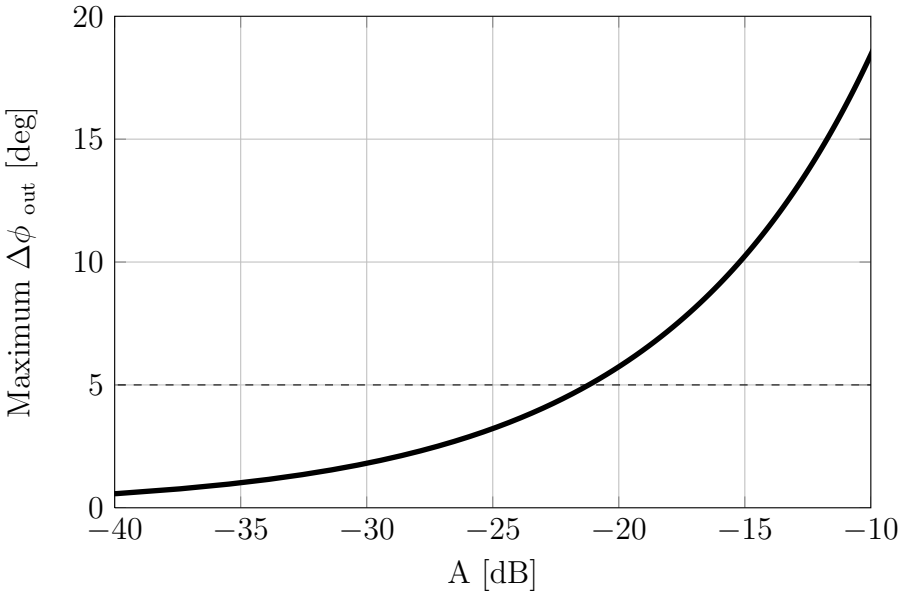

Figure 3.8: Maximum phase measurement error in function of $A = \frac{H_1}{H_3}$

We have already mentioned that the gain is maximized when the switches operates in hard switching mode. This means that the LO transconductor should steer its entire tail current from one diode to the other in a linear way. Unfortunately, the transconductor utilized, cannot be completely linear in the whole input voltage to output current characteristic, since some high frequency harmonics of the output current will become relevant when the input voltage reaches a high amplitude swing. Once the tail current of the transconductor is fixed to 2mA, the degeneration resistance is sized using the graph in Fig.3.9, where the ratio between fundamental of the switching LO signal H_1 and his third harmonic H_3 is shown along with the conversion loss introduced by the switches, as a function of the degeneration resistance R_D.

It can be seen that $\frac{H_1}{H_3} = \frac{1}{A}$, used in Eq.3.26, hence its maximum acceptable value, is given by (3.29). However, since the third harmonic of the LO is just one of the possible sources of measurement error, it is preferable to dimension the degeneration resistance, using a conservative value of 230Ω, which implies $A = -30$dB. The conversion loss introduced by the switches is than at 11dB.

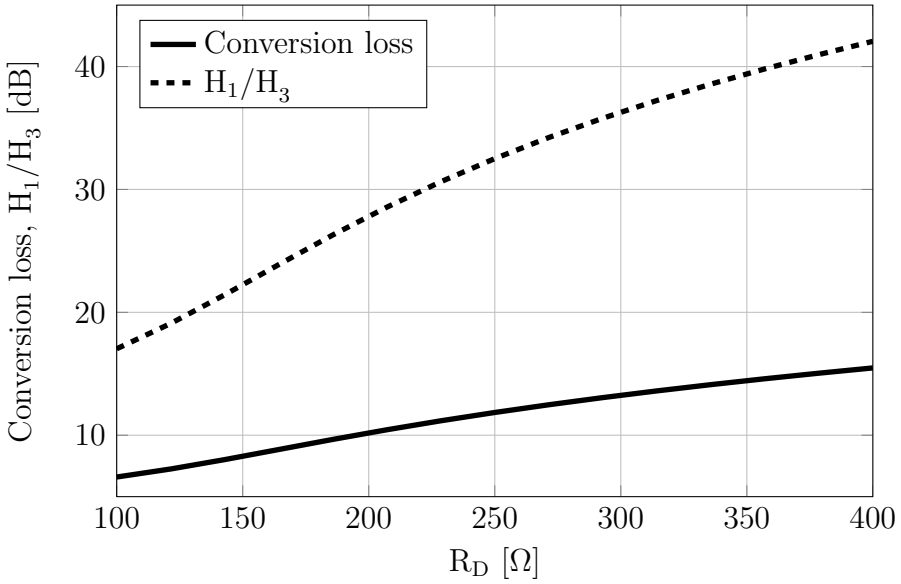

Figure 3.9: Switching cell conversion gain and $\frac{H_1}{H_3}$ as a function of R_D

3.6.2 RF transconductor

The transconductor chosen for the RF signal is slightly different from the one used by the LO due to overhead considerations. If the pre distortion stage is DC coupled to the switching cell, the voltage overhead remaining for the transconductor is approximately $1.6V$, which suggest the use of resistor based current sources.

The used circuit, is the one in Fig.3.10. Its analysis is similar to the one made of the frequency doubler, with the difference that the resistance of the current sources cannot be considered infinite. For this reason, the effect of the degeneration resistance will be weakened since from the small signal standpoint the equivalent degeneration resistance seen by every transistor of the pair is $\frac{R_D}{2}//R_E$ which is always smaller than $\frac{R_D}{2}$. The bias current set for the switching transistor is the same as the one of the pre distortion diodes, hence the tail current of the RF transconductor is set to 4mA. From the system specifications, we know that the signal at the input of the DUT has a maximum power of -20dBm, given that the maximum gain of the DUT is 3dB, the signal at its output will than have a maximum power of -17dBm, which corresponds to a

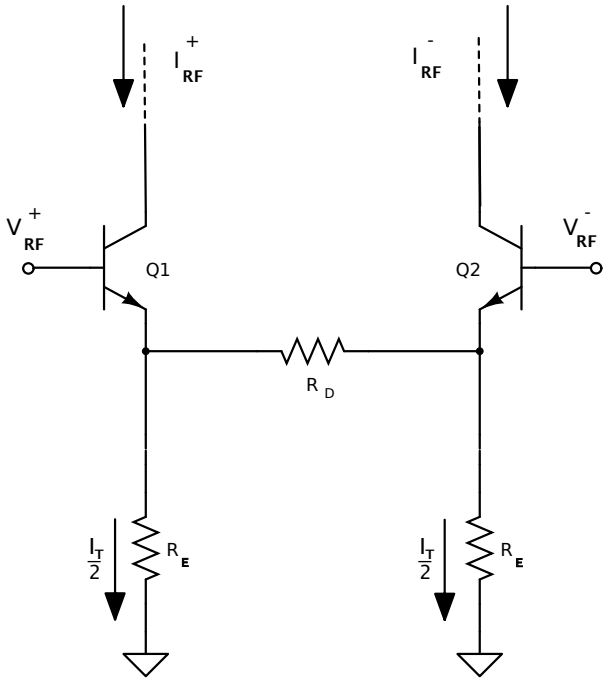

Figure 3.10: RF transconductor

signal having an amplitude of 63mV. R_D is consequently chosen:

$$R_D = 2\frac{V_{RF}}{I_T} = 30\Omega \tag{3.31}$$

3.6.3 Load impedance

Now that the core of the multiplier is sized, we must choose the load resistance in order to maximize the conversion gain, and filter out the unwanted components. From circuit simulations, we have that a -3dB LO signal at the input, generates a distorted signal applied at the bases of the switching transistors whose amplitude is $\hat{v}_d = 80$mV. If we now take into account the conversion loss of the switching cell which from Fig.3.9 is $L_{sw}|_{\text{dB}} = 11$dB and the effective transconductance of the RF transconductor, which can be approximated by:

$$G_{RF} = \frac{g_m}{1 + g_m\frac{R_D}{2}} = 25\text{mS} \tag{3.32}$$

we can calculate the maximum value for R_L that ensure a V_{bc} less than 100mV which prevents the switching transistor to enter the saturation region. Taking also into account the signal at frequency $f_{LO} + f_{RF}$ which is present at the IF output:

$$\hat{v}_d + \hat{v}_{RF}\frac{G_{RF}R_L}{L_{sw}} + \left[(V_{DD} - V_{be}) - (V_{DD} - R_L\frac{I_T}{2})\right] < 100\text{mV} \tag{3.33}$$

$$R_L < \frac{V_{be} + 100\text{mV} - \hat{v}_d}{\frac{I_T}{2} + \hat{v}_{RF}\frac{G_{RF}}{L_{sw}}} \approx 320\Omega$$

where $\hat{v}_{RF}$ is the maximum amplitude of the differential RF signal. As in the frequency doubler case, some spurious components at high frequencies exists at the load of the mixer, and is preferable to filter them out as much as possible. The higher frequency component that must be kept at the output is the one at 6GHz. Hence the pole of the low pass load is fixed at 25GHz in order to preserve the gain in the desired band. The capacitor in parallel with the load resistor is then set to 20ffF.

3.6.4 Output buffer

Since the analog multiplier is the last block of the BITE, its output must be matched to 50Ω, so that the output signal can be measured by the off-chip ATE without having reflections. The matching of the output stage is implemented by a voltage buffer. Since the voltage buffers are DC coupled to the multiplier load, which has a DC voltage drop on it given by :

$$R_L\frac{I_T}{2} = 640\text{mV} \tag{3.34}$$

the buffers collectors cannot be directly connected to the supply voltage, since this would result in a collector-emitter voltage of 1.5V which is very close to the breakdown voltage of the transistors. For this reason, an additional resistance is added at the collector of the two voltage buffers.
From the design of the analog multiplier, we can already predict its conversion gain and theoretical performance. If we suppose the LO signal at the desired

amplitude, the conversion loss of the switches is fixed and the voltage conversion gain from the input of the multiplier to the load is:

$$G_{Mult} = \frac{G_{RF}}{L_{sw}} R_L = 8\text{dB} \tag{3.35}$$

This calculated gain does not take into account the small attenuation introduced by the load filter, and the variation of the gain due to the phase difference between the LO and the RF signal which is anyway smaller than the one tolerable by the measurement system. Once the signal at the load of the multiplier is buffered by the output emitter follower, which also matches the multiplier to 100Ω, its voltage amplitude is halved, resulting in a 6dB loss. Hence, the final input to output voltage conversion gain will be of 2dB. From the choices made on the LO transconductor, some estimations on the measurement precision can be made. The parameter A has been chosen to be −30dB. Then from Fig.3.8 we can immediately see that this correspond to a maximum phase measurement error of 1.73^o. The maximum variation of the multiplier gain is instead 0.54dB which is derived by evaluating (3.29). As we can see, these predicted performance seems to largely satisfy the conditions imposed by the project. However, the effect of the LO feedthrough, which is always present in real multipliers, degrades the performance. This effect should not be present in the used topology since its structure is double balanced. However, the non ideal symmetry of the circuit components, caused by production mismatches, the non perfect common mode rejection of the RF transconductor and the parasitic capacitances of the real circuits, let the LO signal reach the output. Since its frequency is the same as the one of the output signal, this degrades the measurement performance.
The schematic of the analog multiplier, excluding the bias circuit, is shown in Fig.3.11.

3.7 Bias and enable circuit

In integrated circuits, the transistors are typically biased through the use of current mirrors. The goal of these circuits is to replicate in the transistor

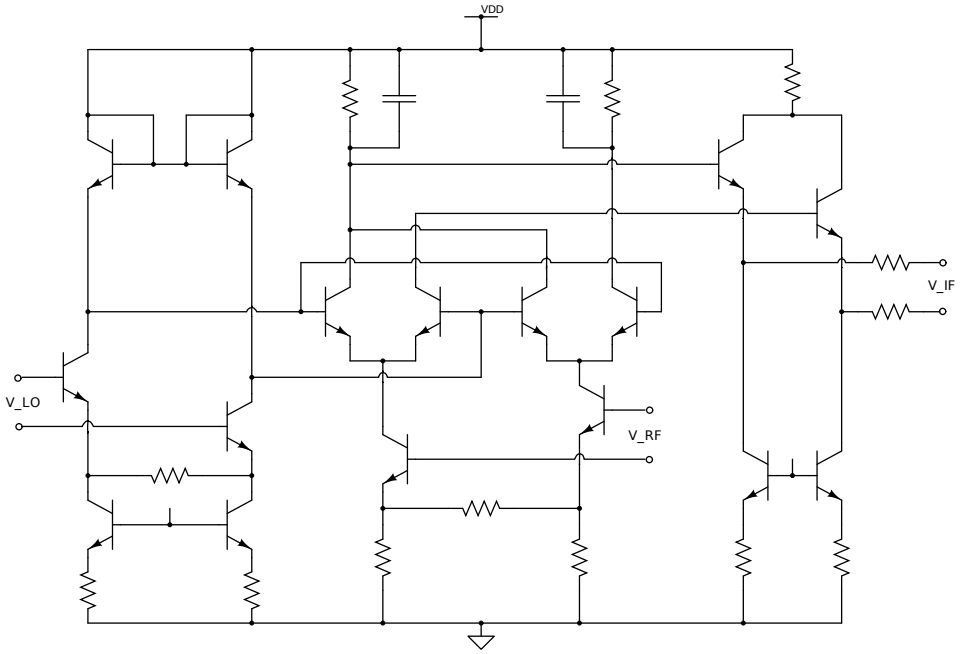

Figure 3.11: Analog multiplier circuit

that needs to be biased the current which flows through a reference branch multiplied by a scaling factor N. The type of current mirror used in this work, is the one shown in Fig.3.12.

A quick analysis of this circuit, using KVL around the loop formed by base emitter diodes and emitter resistances of Q_1 and Q_2, leads to :

$$I_{OUT} = \frac{1}{R_2}\left[I_{REF}R_1 + V_T \ln\left(\frac{I_{REF}}{I_{OUT}}\frac{Is_2}{Is_1}\right)\right] \tag{3.36}$$

If the current in Q_2 is N times the one in Q_1 the emitter area of Q_2 should be N times the one of Q_1, and R_1 should be N times R_2, such that in (3.36) gives:

$$I_{OUT} = NI_{REF} \tag{3.37}$$

We can note that, if the voltage drop on the emitter resistances of the transistors is large compared to V_T, the first term of (3.36) is more influent than the logarithmic one. Hence the ratio between I_{OUT} and I_{REF} depends almost exclusively on the ratio of R_2 and R_1. The output resistance of the current source constituted by Q_2 is increased if compared to that of a simple current

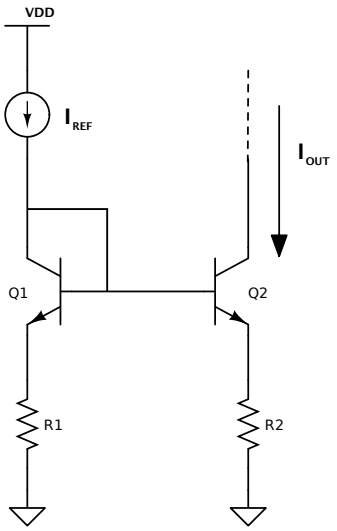

Figure 3.12: Current mirror

mirror, where there is no emitter resistance and N is determined only by the ratio of the emitters area and. Its value is:

$$R_o \backsimeq r_o \left(1 + g_m R_2\right) \tag{3.38}$$

One of the characteristic requested for the measurement system is that it must not cause any effect on the radar system when it is not used. This request translates to a specification on the S_{11} and S_{22} parameters measured at the the DUT' s ports which must have a magnitude smaller than -10dB, when the measurement system is turned off. This means that the test system, which is permanently connected through coupling capacitors to the DUT, must exhibit high impedance at the output of the frequency doubler and at the input of the analog multiplier when it is turned off. From the design of the frequency doubler and the analog multiplier, we know that the output of the frequency doubler and the input of the analog multiplier, are connected to the emitter and to the base of a transistor respectively, which are biased by a current mirror. In order to make these nodes high-impedance, we need to switch off the current source of the mirror.

This task is accomplished by a pMOS transistor placed between the power

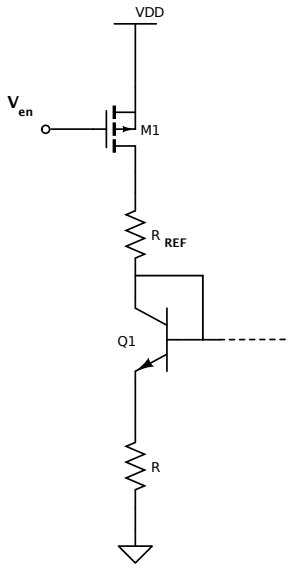

Figure 3.13: Enable circuit

supply and the reference branch of the current generator as shown in Fig.3.13. In this way, the current source is switched off when V_{en} is pulled to V_{DD} and on when V_{en} is pulled to ground. The pMOS transistor must be wide enough to operate in the triode region when it is on, and to have a low on resistance in order to make the the reference current mainly dependent on the resistance R_{REF}.

CHAPTER 4

Layout

In this chapter we will briefly describe the layout that has been realized for each of the blocks of the BITE.

4.1 Layout design

The physical realization of the designed circuit, will inevitably introduce unwanted parasitics effects and mismatches between the components, which can make the circuit work in an unpredicted way. It is possible to minimize these effects by using good design strategies. However there are several rules dictated by the specific technology, which typically concern the minimum distances between traces, vias and components that must be satisfied. Additionally to these design rules, one should carefully dimension the teaces width so they are able to carry the current that should pass through them. Some additional rules for a good layout, which are not strictly dictated by the technology are:

- If the designed structure is differential, the layout should be as symmetrical as possible.

- Avoid long connections for the signals, since they imply relevant capacitive and inductive parasitics.

- Avoid signal lines crossing, and if it is needed make the crossing area as small as possible.

- Keep the emitter followers collectors close together in order to prevent possible oscillations due to parasitic inductances.

- The components that needs to be matched, should be close and arranged in a common centroid fashion, in order to avoid temperature differences and mismatches.

- When possible, use the higher metal levels for the wiring.

- Put several VEE to substrate contacts especially close to the NPN transistors and connect all of them with the main VEE metal grid, avoiding branches that starts from the VEE metal grid and does not end to the VEE metal grid.

- Consider the parasitic inductance of any long wire.

The layout of the BITE has been designed using Cadence Virtuoso Layout Suite, which can run an automatic design rule check (DRC), and a layout versus schematic check (LVS) to make sure that there are no discrepancies between the schematic and the layout. Once the layout is completed and is DRC and LVS clean, its resistive, capacitive and inductive parasitic components, can be extracted from it using the QRC extraction functionality included in the layout editor, and added to the schematic. Then, the circuit can be simulated again and if the specifications required are satisfied, the layout can be considered valid. Otherwise, if the simulations performed taking into account the parasitic components give unsatisfactory results, either the layout or the circuit topology and components dimensions, must be changed.

4.2 Polyphase filter

The layout of the polyphase filter block, which includes the input and output buffers, is shown in Fig.4.1. As we can see, the layout has perfect symmetry in the buffers part, but the polyphase filter part is not completely symmetrical. This is due to the intrinsic structure of the polyphase filter, which is basically a ring of capacitors and resistors connected in series. Hence it is not possible to design a layout that treats every input and every output exactly in the same way. An evident consequence in the designed layout is the long connection at the 90^o output of the filter, highlighted in Fig.4.1, which is not present at the other outputs. Such long connection introduces parasitics inductance and capacitance, which we expect to cause a $90^o - 270^o$ output unbalance. The total chip area occupied by the Polyphase filter is 190x190μm^2.

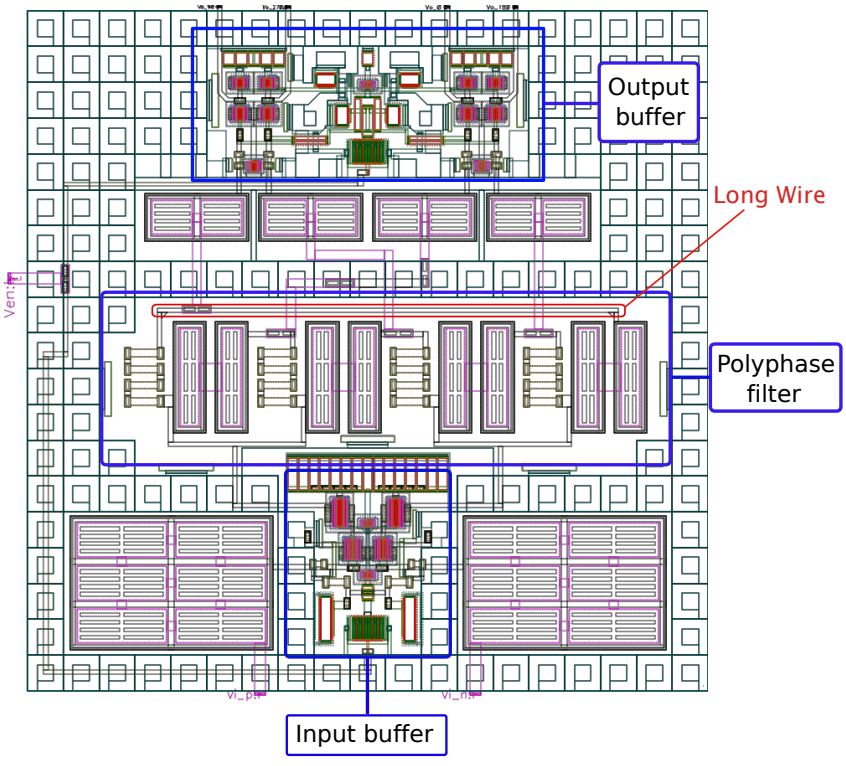

Figure 4.1: Polyphase filter layout 190x190μm

4.3 Frequency doubler

Since the up conversion mixer is directly driven by the Polyphase filter block, the frequency doubling block consists only in the up converting mixer and its output buffer. As we can see in Fig.4.2, the layout has been designed to be as symmetrical as possible. The most challenging part, was the switching cell. The emitters of each emitter coupled pair have been placed as close as possible, implying some wires crossing at their collectors. This has been realized in a way that minimizes the crossing area. The total chip area occupied by the frequency doubler is 130x160μm^2.

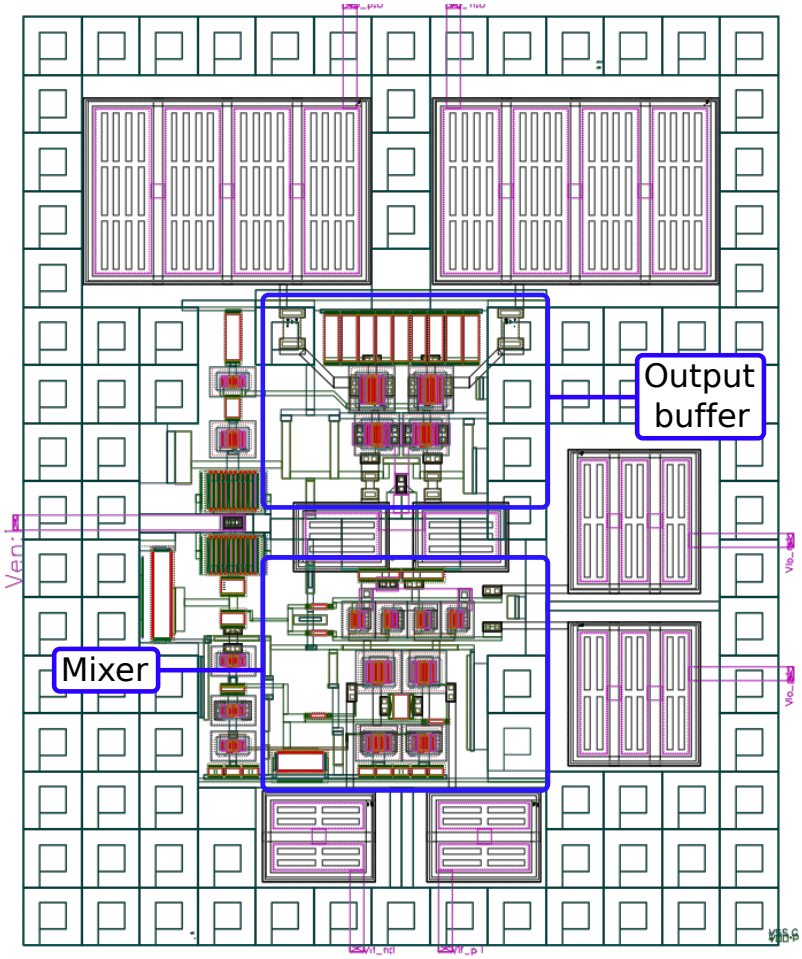

Figure 4.2: Frequency doubler layout 130x160μm

4.4 Analog multiplier

The Analog multiplier consists in a mixer similar to the one used in the frequency doubler where the LO signal is provided by a pre-distortion stage. Some attention must than be paid in the connections between the two stages, which cannot be done without wires crossing if the wires are kept short and we keep the two pre-distortion diodes very close together so they match very well in characteristic and temperature. The same care paid to the frequency doubler should be also put in the layout of the switching cell for the analog multiplier. The total chip area occupied by the Analog multiplier is 140x190μm^2.

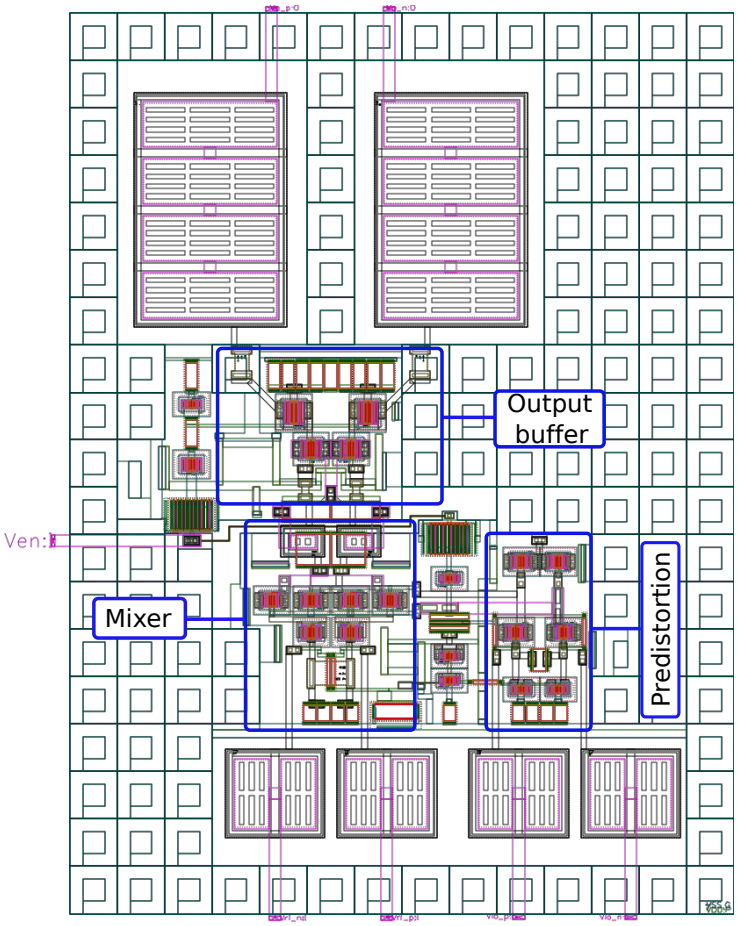

Figure 4.3: Analog multiplier layout 140x190μm

CHAPTER 5

Simulations

In this chapter, the simulations made on the overall test system are presented. In the first part of the chapter, each elementary block of the system is treated in a separate section in order to verify its performance compared to the theoretical one. The performed simulations, are focused on the verification of the system performances once frequency, input power, voltage supply and temperature of operation are varied in the the range of operation for the system. Furthermore, Montecarlo simulations are performed to take into account the possible variations in technological parameters due to the production process spreads and mismatches. Finally the last section of this chapter, illustrates the results obtained by the whole test system including the DUT model. Each of the simulations is performed after the extraction of the parasitics components from the designed layout.

5.1 Polyphase filter

The polyphase filter is simulated in order to verify its capability to generate differential signal in quadrature having a -3dBm power. First of all, we verify

the gain and the phase relation between the two differential output versus frequency and for temperature and supply voltage variations. In Fig.5.1 and Fig.5.2 we see that the polyphase filter gìhas an average gain of -2.5dB, which is considerably lower then the expected one. This can be explained by the fact that the designed polyphase filter has relatively high value resistances (344Ω) in order to loosen the input buffer requirements, hence, a voltage drop is present due to the input impedance of the output voltage buffers at the filter operating frequency. For this reason, we need to drive the polyphase filter with a 0dBm signal, if we want a -3dBm output signal.

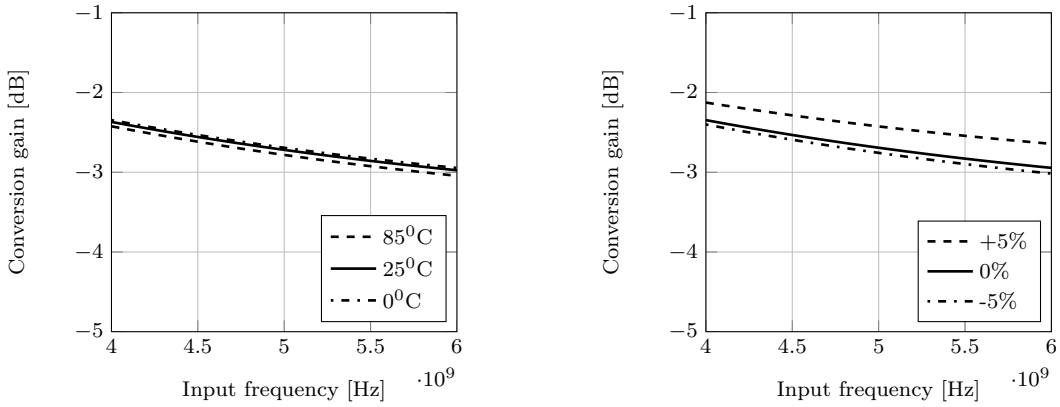

Figure 5.1: Gain versus frequency.

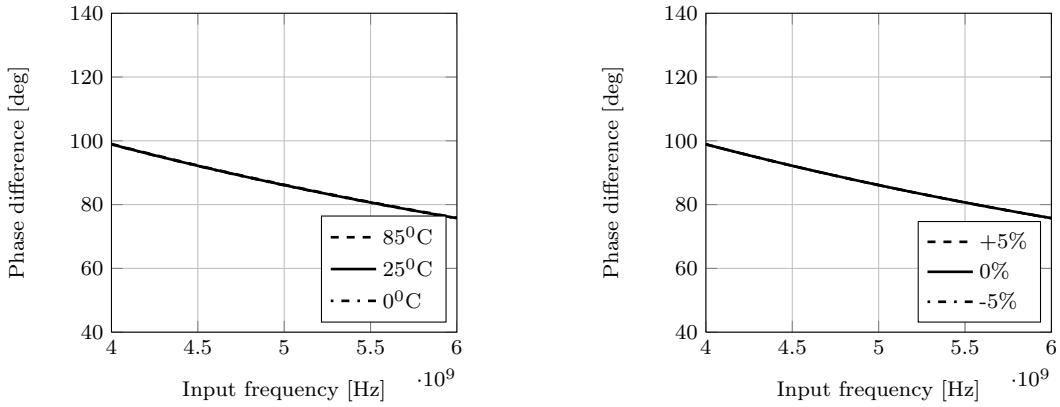

Figure 5.2: Phase difference between the outputs versus frequency.

The input port of the polyphase filter, which will be connected to the ATE, is matched, in order to avoid reflections. From the design specifications, we have

that the S_{11dd} parameter, must be below -10dB and as we can see in Fig. 5.8 this is verified in the frequency range of interest.

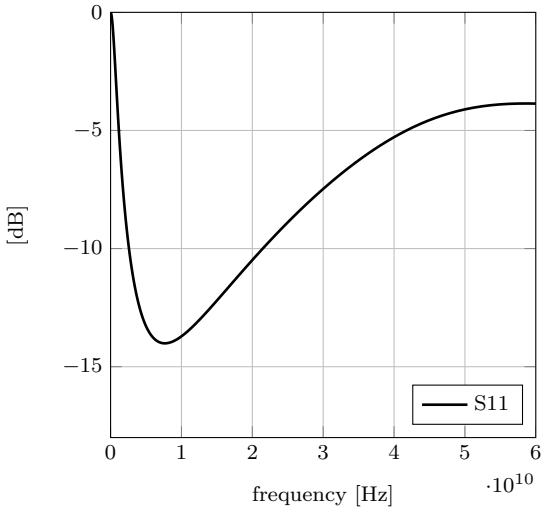

Figure 5.3: S_{11dd} of the polyphase filter

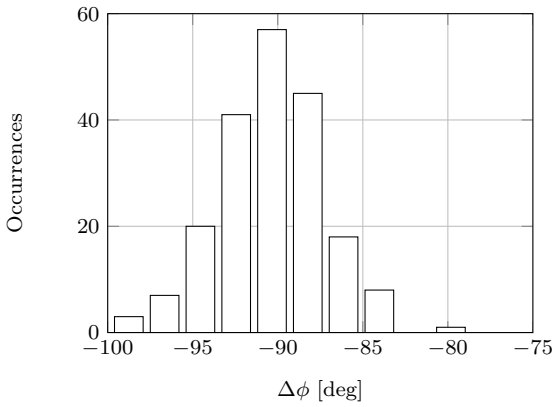

Figure 5.4: Phase difference between the polyphase filter's output signals.

A Montecarlo simulation is performed at the quadrature frequency, to check inbalances in the theoretically differential output of the filter, and the variation from the quadrature condition of the output signals. We can see from the results in Fig.5.5, that the asymmetry introduced in the layout design is visible as a greater imbalance at the $90^o - 270^o$ output.
A transient simulation of the input and output signals is shown in Fig.5.6

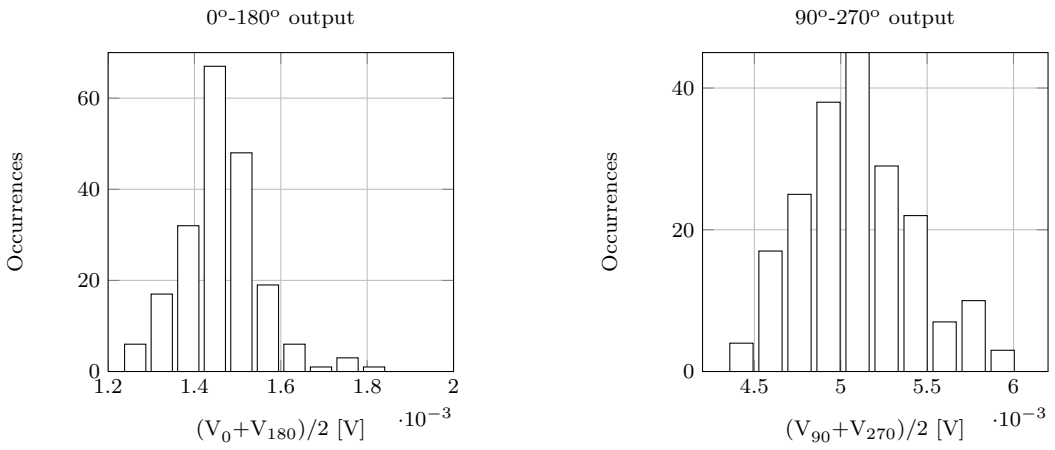

Figure 5.5: Montecarlo imbalance simulation.

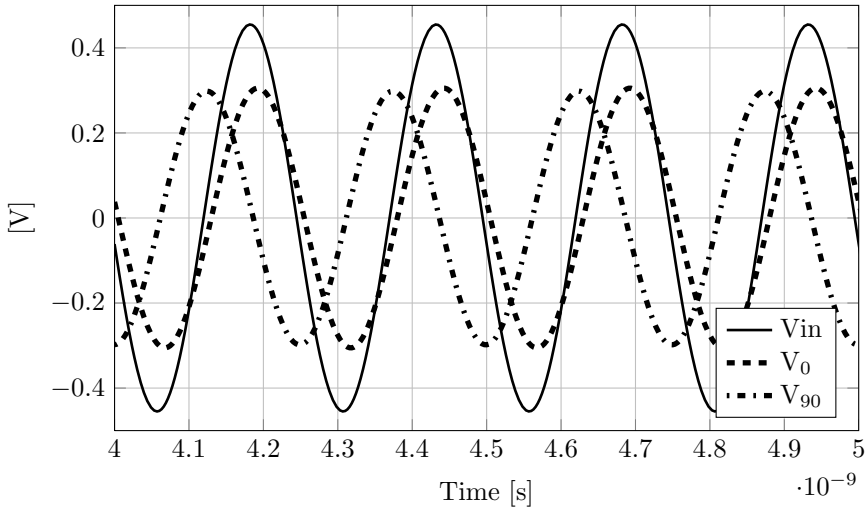

Figure 5.6: Transient input and output signals

The stability of the polyphase filter, has been checked in all of its configuration, giving unconditional stability.

5.2 Frequency doubler

The frequency doubler, is simulated taking into account the cascade of of mixer, output emitter follower and a port having 100Ω resistance, which emulates the DUT. The first performed simulation, verifies that its conversion gain remains close to the predicted one, in order to avoid the saturation of the DUT input, across temperature and supply voltage variations. From Fig.5.13 we can see that the conversion gain of the frequency doubler is in the range from−17dB to −20dB, corresponding to an output signal from −23dBm to −20dBm if a −3dBm LO and IF signal are considered. Hence the DUT input signal stays lower than its maximum allowable value.

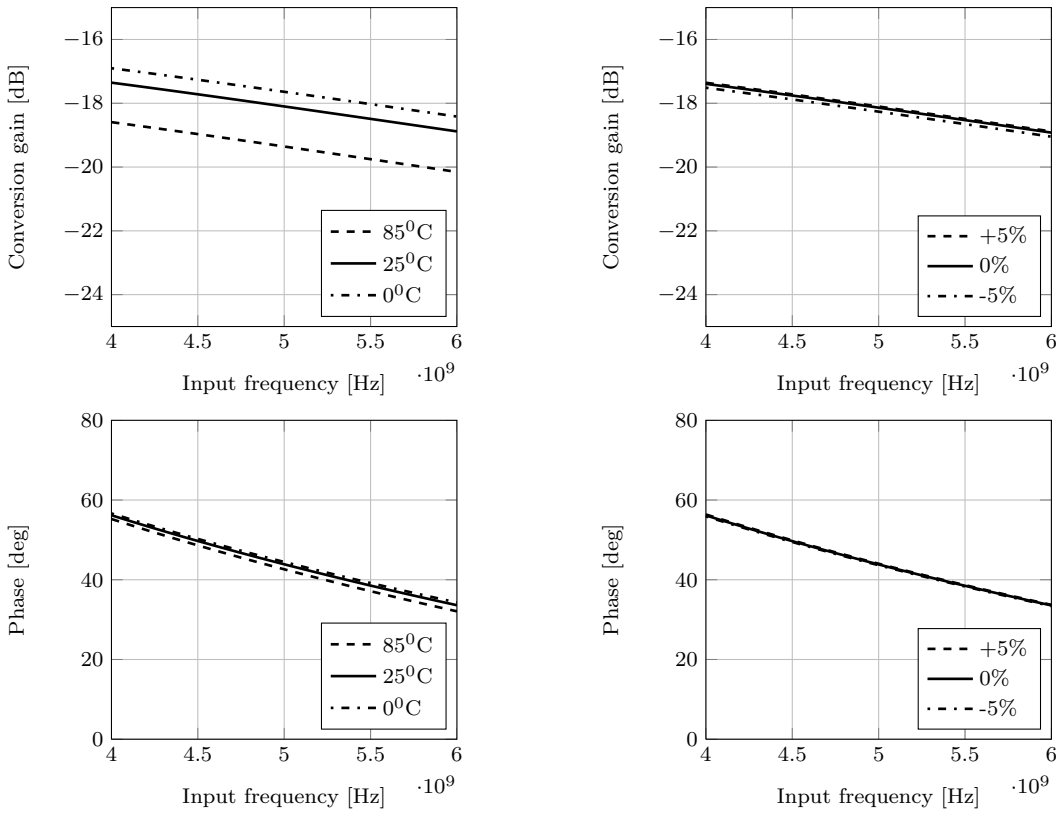

Figure 5.7: Conversion gain versus frequency

From the given specifications, the measurement system should be matched at his output when it is on and being non influent on the performances of the radar

system when it is switched off. This request is translated to a specification on the S_{22dd} of the frequency doubler and on the S_{11dd} at the input of the DUT shunted to the output of the frequency doubler, when the enable signal is pulled to the supply voltage. Both the S_{11dd} and the S_{22dd} must be under -10dB. As we can see in Fig.5.8 these conditions are fully satisfied.

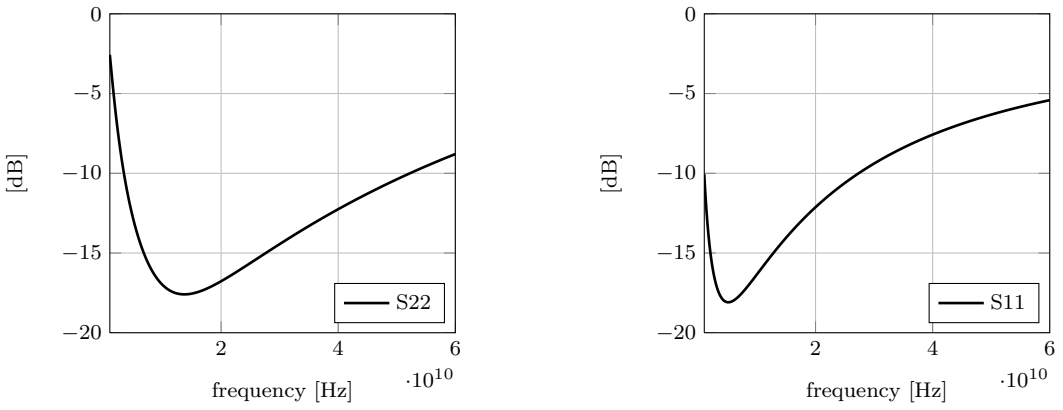

Figure 5.8: S_{22dd} of the doubler and S_{11dd} of the DUT

The amplitude of the largest spurious harmonic at the output, which we expect to be the one at $4f_{IF}$, compared to the wanted one at $4f_{IF}$, can be evaluated through the simulation of the Spurious Free Dynamic Range (SFDR) which is shown in Fig.5.9 versus the frequency of the input signal. From this simulation, we can tell that the simple RC filter at the mixer load, does not heavily attenuate the high frequency spurious components, however we have to consider that using this type of load is the more efficient way to filter out high frequency components in terms of silicon area and since these components only slightly degrade the measurement performance, the design of a more complex filter is not needed.
The Montecarlo simulation in Fig.5.10 shows the value of the conversion gain for a 5GHz, -3dBm LO and RF quadrature signals, demonstrating a good stability of the gain against mismatches and process variations.
A transient analysis of the frequency multiplier is shown in Fig.5.11 where an input 5GHz signal is shown together with the output signal at 10GHz
Further simulations can be made to check that the value of the DC component

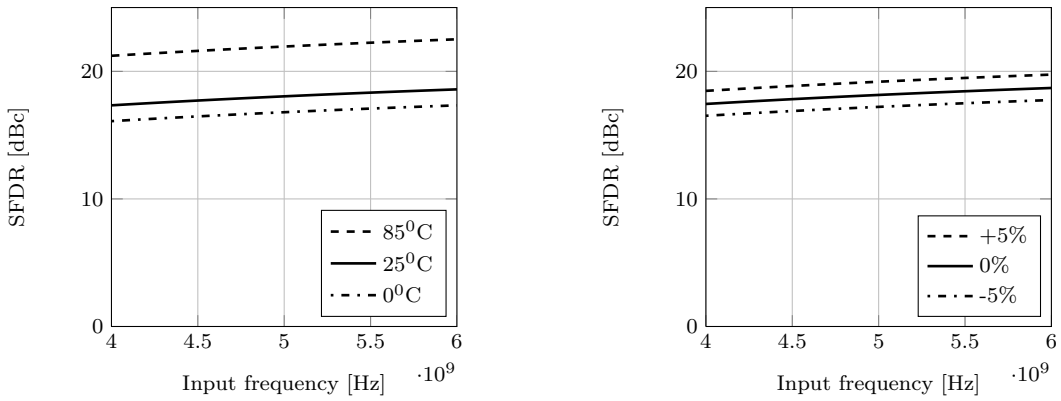

Figure 5.9: SFDR versus frequency for temperature and supply variations

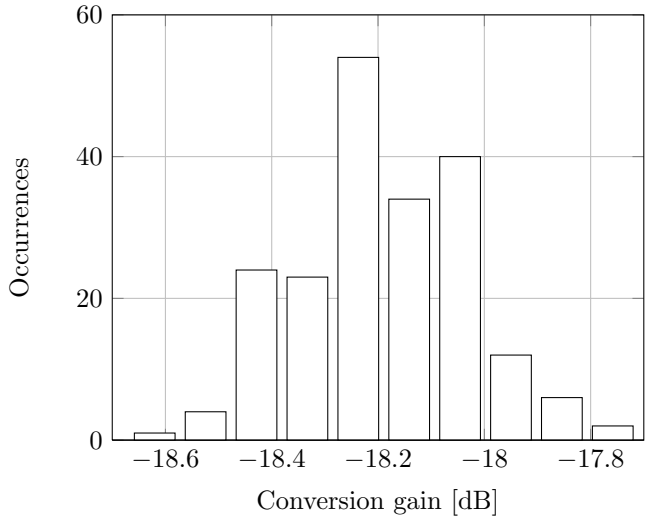

Figure 5.10: Montecarlo Simulation fot the conversion gain at 5GHz.

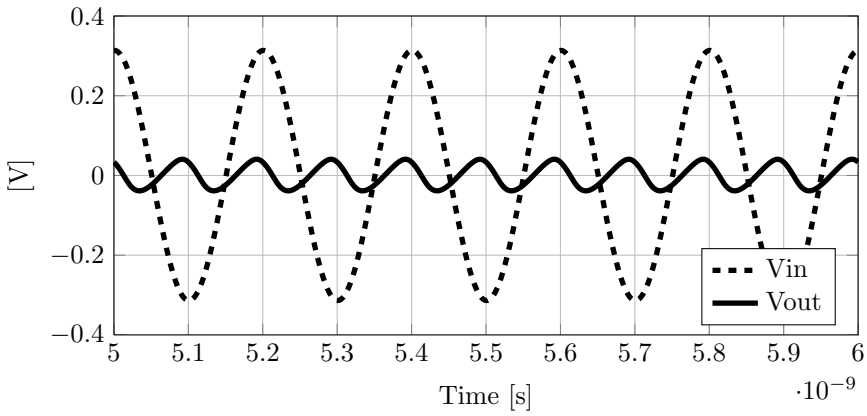

Figure 5.11: Transient input and output signals

at the load of the mixer and the conversion gain when the phase difference between LO and IF signal is swept. In Fig.5.12 we can see that both gain and DC components behave as expected. The highlighted zone of the graph represent the operation area of the frequency doubler, hence the gain in practically constant and and the DC component, as predicted, is the 20% of the fundamental one.

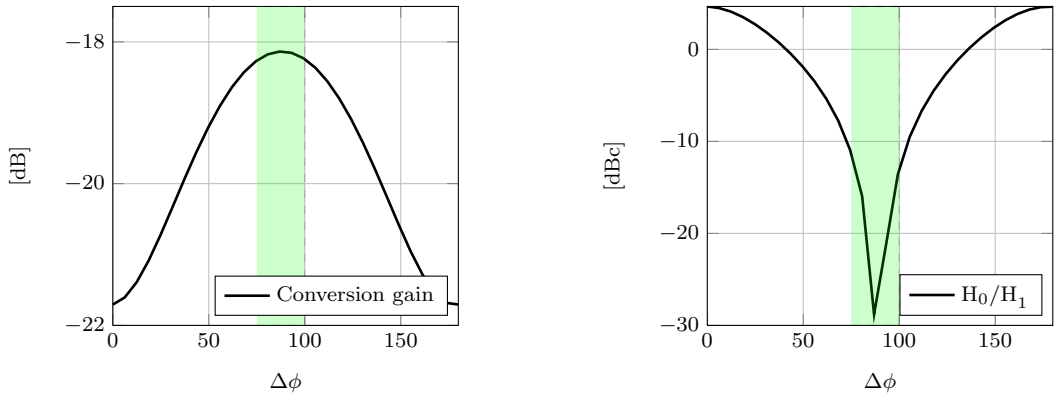

Figure 5.12: Conversion gain and DC component on RL versus $\Delta\phi$

The stability of the multiplier has been checked in all of its configurations, giving unconditional stability.

5.3 Polyphase filter + Frequency doubler

Once the Polyphase filter and the up converting mixer have been simulated separately they are connected together to check their operation. In Fig.5.13 the conversion gain is traced versus frequency at Temperatures and power supply variations.

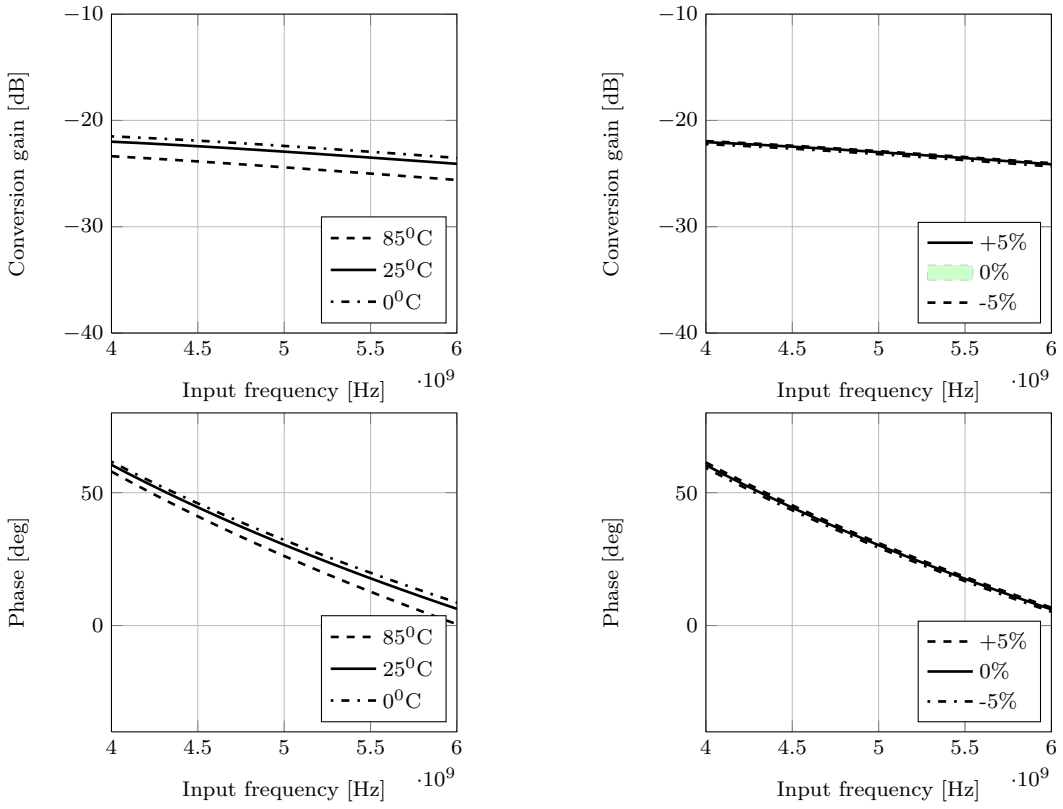

Figure 5.13: Conversion gain versus frequency

5.4 Analog multiplier

Each of the simulations on the analog multiplier have been made considering the output buffer and a 100Ω load. Unless different stated, the RF signal frequency is set to 10GHz and the LO frequency is set to 5GHz at a temperature of 25ºC and 3.3V supply voltage. The conversion gain from the RF port to the

IF port has been simulated versus the input frequency, for temperature and voltage supply variations in the desired range. In Fig.5.14

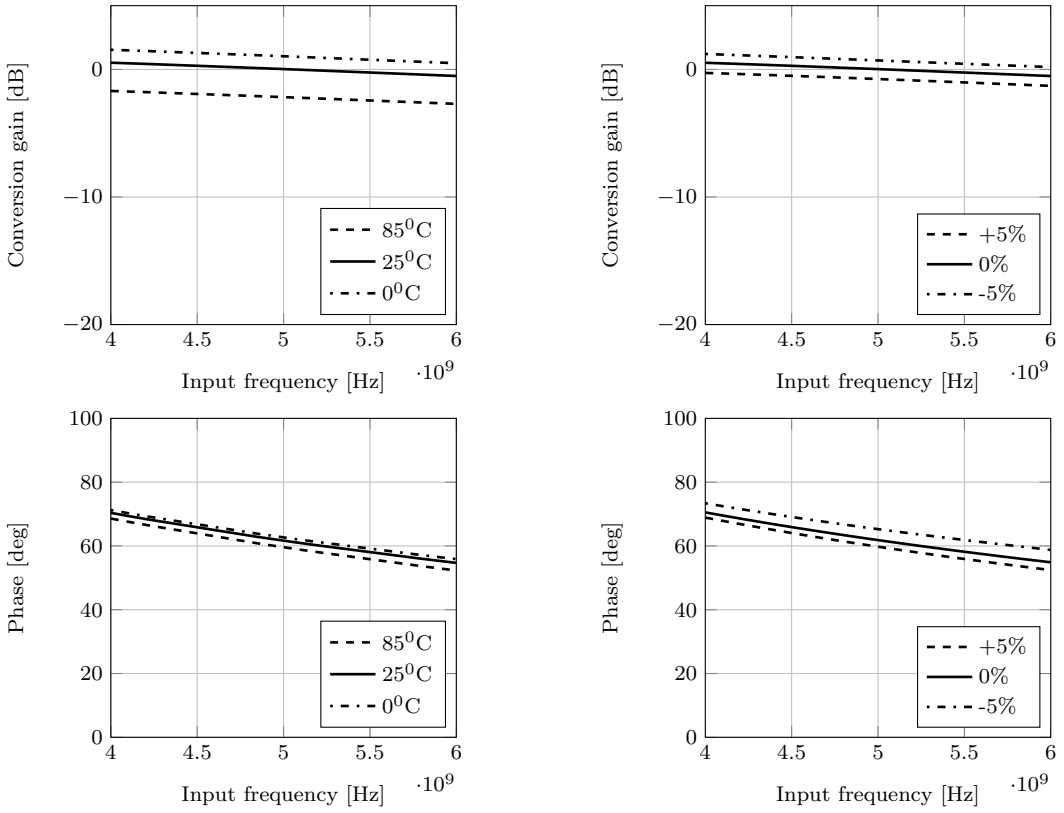

Figure 5.14: Conversion gain of the analog multiplier.

As opposed to the frequency doubler, the analog multiplier, has two independent input ports. In Fig.5.15 the IIP3 of the analog multiplier is traced and in Fig.5.16 the compression point and the Amplitude to phase modulation are plotted, showing an IIP3 of 3dBm and a compression point of −3dBm which are compatible with the maximum input power at the RF port, which is −17dBm. From Chapter 2 the limit for the ratio between the first and the third harmonic introduced by the LO signal should be higher than 21.3dB, in order to limit the degradation of the measurement performance. This ratio is simulated together with the conversion gain, versus theLO power in Fig.5.17. As seen in the Chapter 3, an LO power of −3dBm is low enough to guarantee a negligible

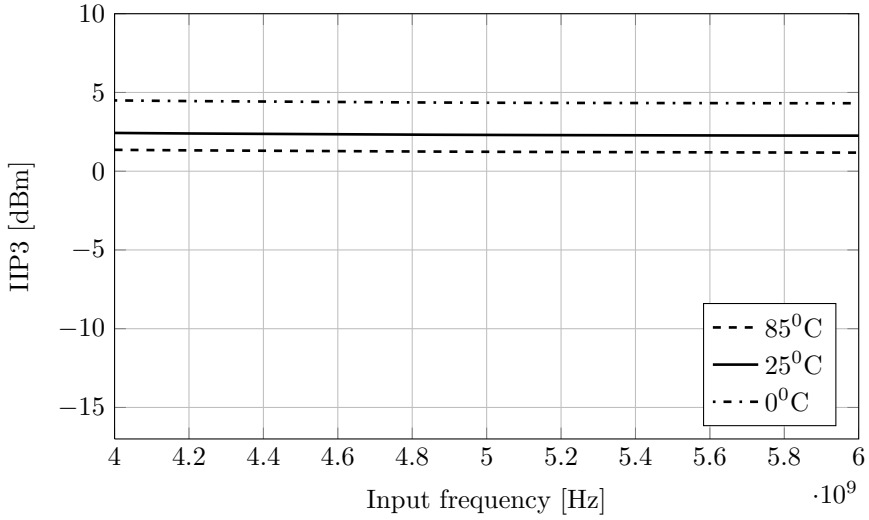

Figure 5.15: IIP3 versus frequency and temperature

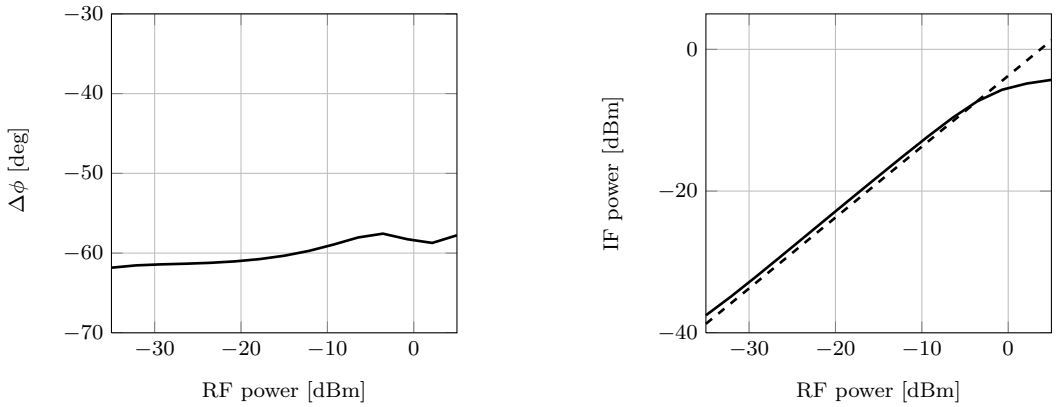

Figure 5.16: AM to PM modulation and compression point.

contribute of the third order harmonic and a conversion gain close to zero.

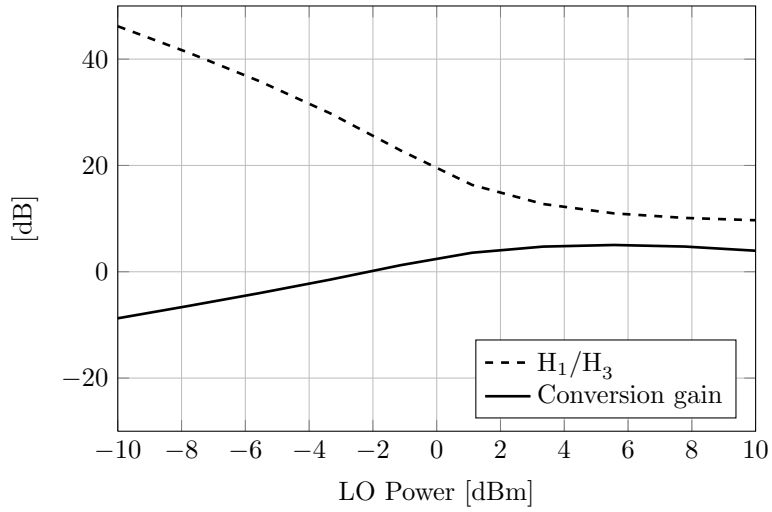

Figure 5.17: Conversion gain and $\frac{H_1}{H_3}$ versus LO power

The most important check on the analog multiplier, is the LO feedthrough, whose presence can influence the measurement performance of the whole system. Since the structure of the multiplier has a theoretically perfect symmetry, the LO signal should not be present at its output. However, in the fabricated circuit, asymmetries in the layout design and components mismatches, will cause the LO signal to leak to the load. A Montecarlo simulation is set up in order to evaluate the relevance of this phenomenon which can be quantified by measuring the magnitude of the LO frequency component, when the RF input is balanced. In Fig.5.18 the Montecarlo simulation results at 4GHz and 6GHz are shown. We see that the effect of the LO feedthrough does not chance much with frequency suggesting an higher dependance on the components mismatch than to layout asymmetries. The simulation values for the LO feedthrough are compatible with the specifications given for the measurement system, since the ratio between the expected output component and the component due to the sum of the LO feedthrough and the third order harmonic of the LO remains below the limit discussed in Chapter 3.

To verify the theoretical calculations made in Chapter 3, the absolute error in phase and gain measurements has been simulated for every possible combina-

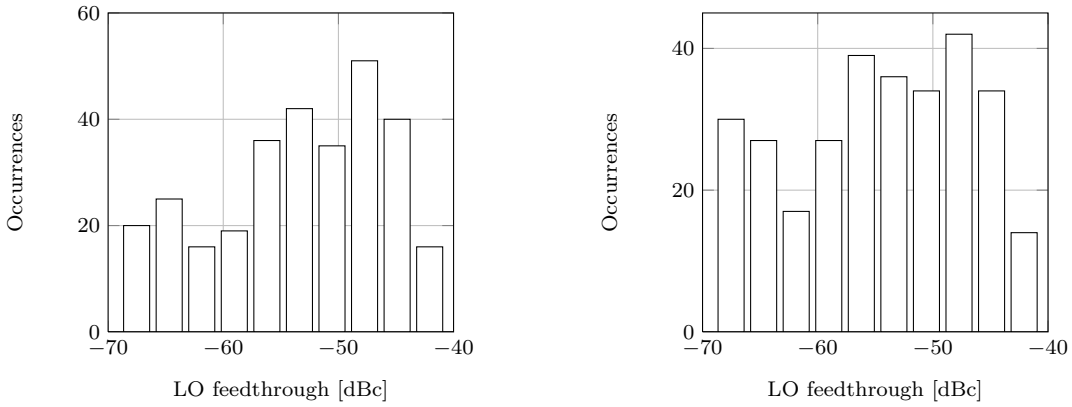

Figure 5.18: Montecarlo simulation of LO feedthrough at 4GHz and 6GHz .

tion of the phase shift and gain introduced by the DUT. In Fig.5.19 and 5.20 the result of such simulations are represented as surfaces. We note that the measurement precision gets worse when the gain of the DUT is lower and the introduced phase shift is larger. This phenomenon is due to the LO feedthrough which becomes more influent as the gain of the DUT decreases. It is clear that the optimum configuration for the phase shift measurement is the one where the DUT has the maximum possible gain and the optimum configuration for the gain measurement is the one with the minimum phase shift, which both imply the minimum effect of the LO feedthrough.
A transient analysis of the analog multiplier, is shown in Fig.5.21 where the input 10GHz signal is showed together with the output signal at 5GHz plus the not completely erased spurious component a t 15GHz
Finally, the stability of the analog multiplier has been checked for all of its configurations, giving unconditional stability.

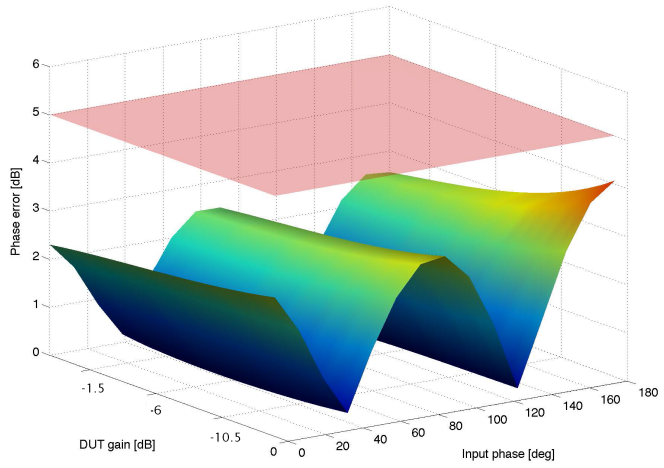

Figure 5.19: Absolute error on phase measurement

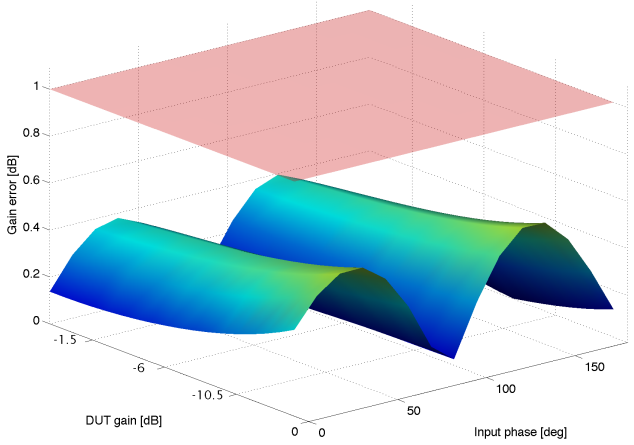

Figure 5.20: Absolute error on Gain measurement

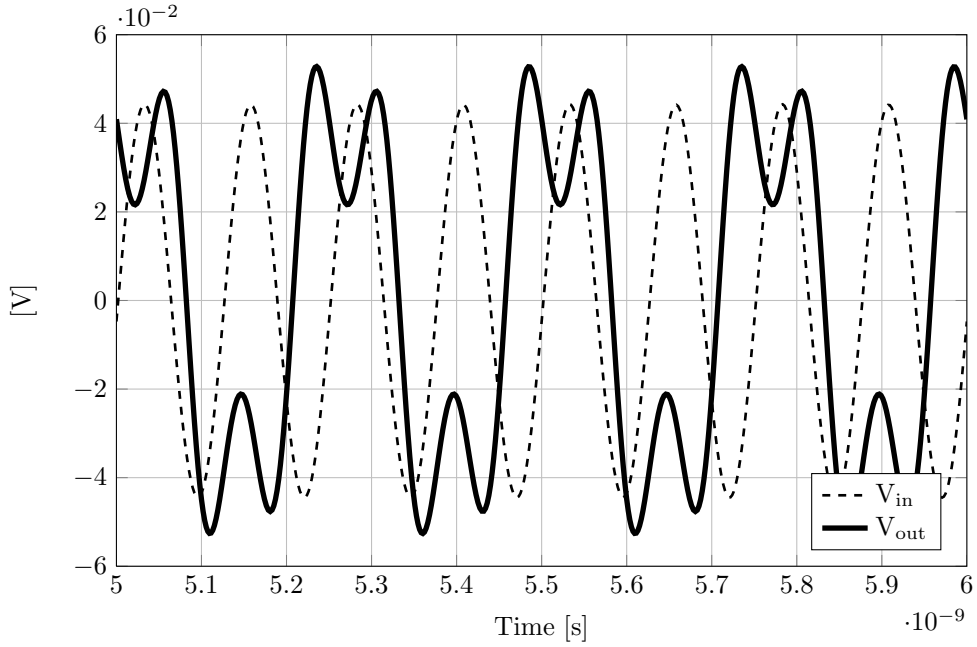

Figure 5.21: Transient input and output signals

5.5 Performance of the BITE system

Once the system has been tested in each of its parts, resulting in a close match to the expected behavior, we can quantify its performance by simulating all its parts connected together. In Fig.5.23 the absolute phase difference between the output and input of the DUT and of the BITE, is shown versus frequency for different configurations of the phase bits. As we can see, the phase difference between the output and input signals of the BITE, is higher, since the signal experiences also the phase delay given by the additional blocks of the BITE. However, since we are interested in the relative phase difference, we need to follow the procedure illustrated in Chapter 1, and subtract the first (the top trace in the figure) measurement from the other. This results in two relative phase difference graphs which are shown in Fig.5.23. Finally, the error in the measurement is derived by the difference between this two graphs and is graphically represented by the surfaces in Fig.5.24-5.25-5.26 at different temperatures.

Even if the error is below the 5^o limit, it still higher than the value predicted.

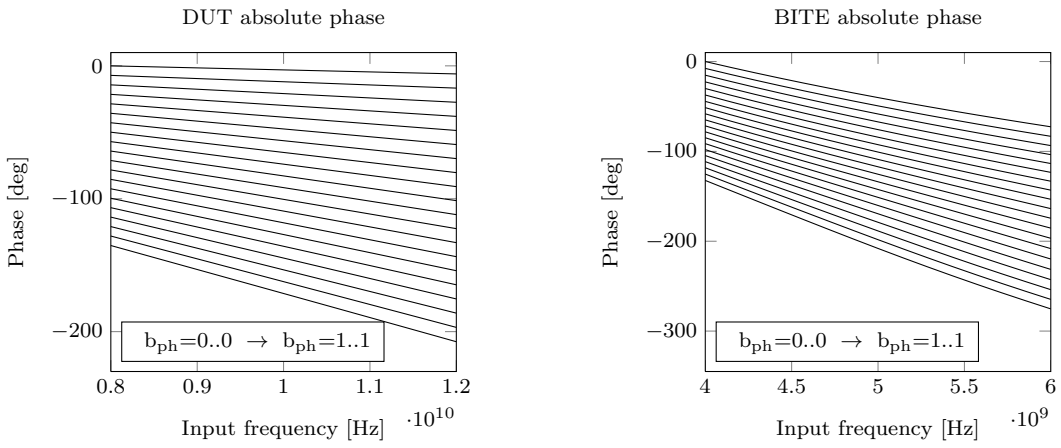

Figure 5.22: Absolute phase difference of DUT and BITE.

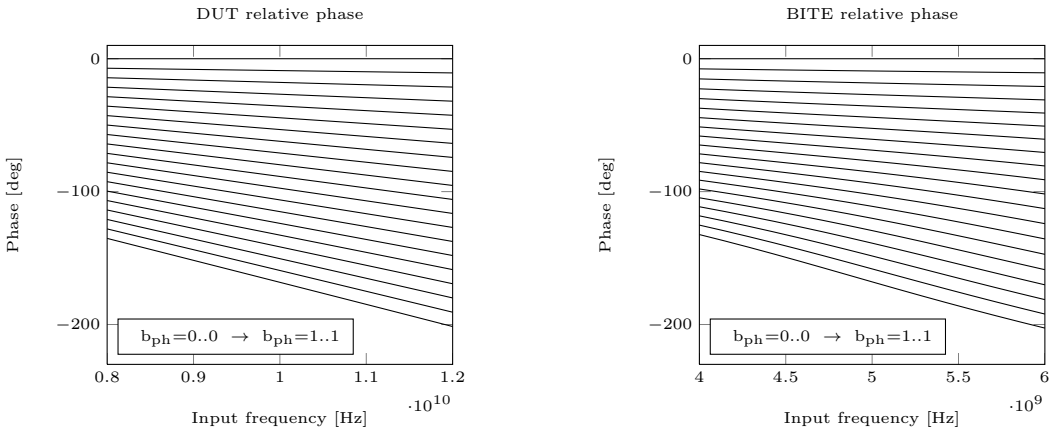

Figure 5.23: relative phase difference of DUT and BITE.

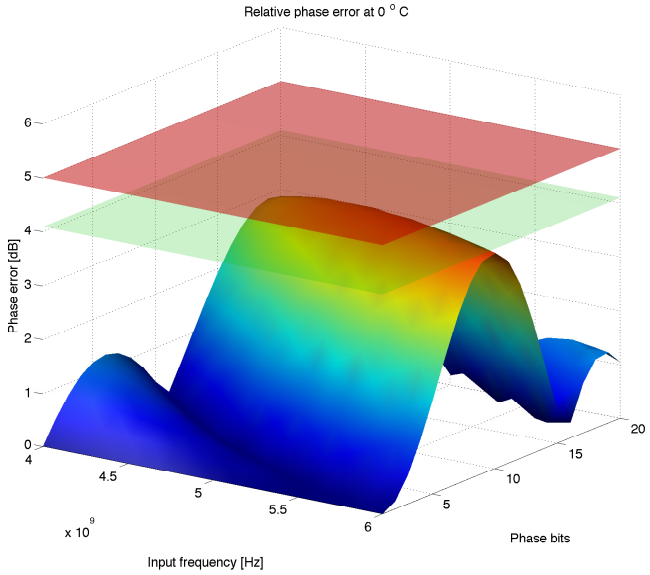

Figure 5.24: Relative phase measurement error at 0^oC

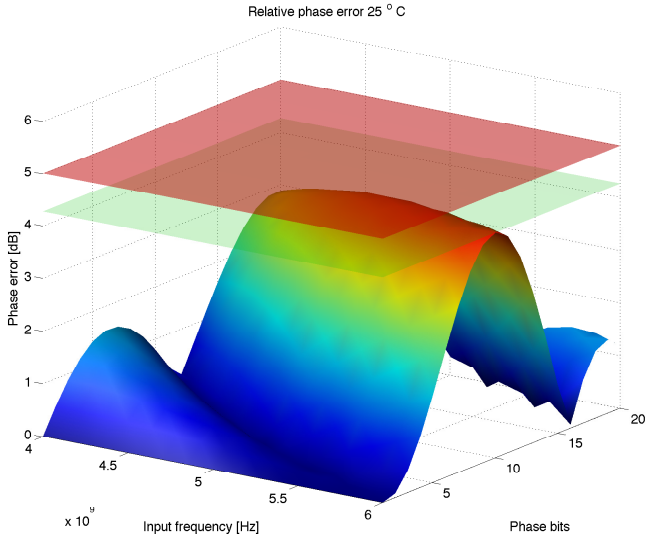

Figure 5.25: Relative phase measurement error at 25^oC

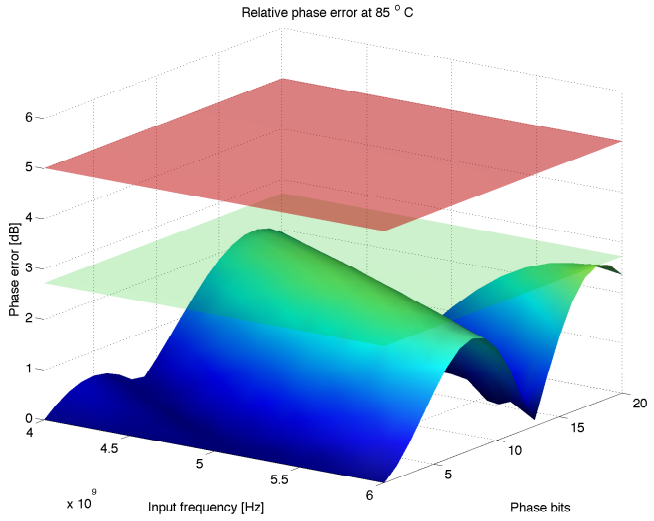

Figure 5.26: Relative phase measurement error at 85^{o}C

This effect was not derived in the theoretical description of the BITE, since it is not due to the third harmonic of the LO signal, but to the LO leakage to the load.

The same procedure is performed to estimate the relative gain measurement error. In Fig.5.27 the absolute gain of the DUT and of the test system are depicted. Then, the relative gain is shown in Fig.5.28. Finally, the error on the relative gain measure which is the difference between the relative gain of the DUT and the relative gain between the input and output of the BIT, is represented in Fig.5.29-5.30-5.31 at different temperatures and in Fig.5.29 at different configurations of the phase's bit word, respectively, the first, the mid one and the last. The measurement error is always smaller than the one given by the specifications.

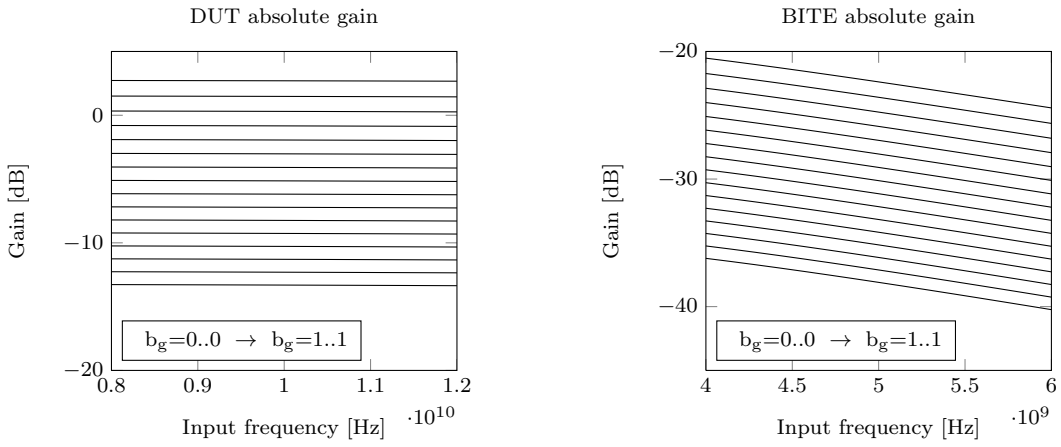

Figure 5.27: Absolute gain difference of DUT and BITE.

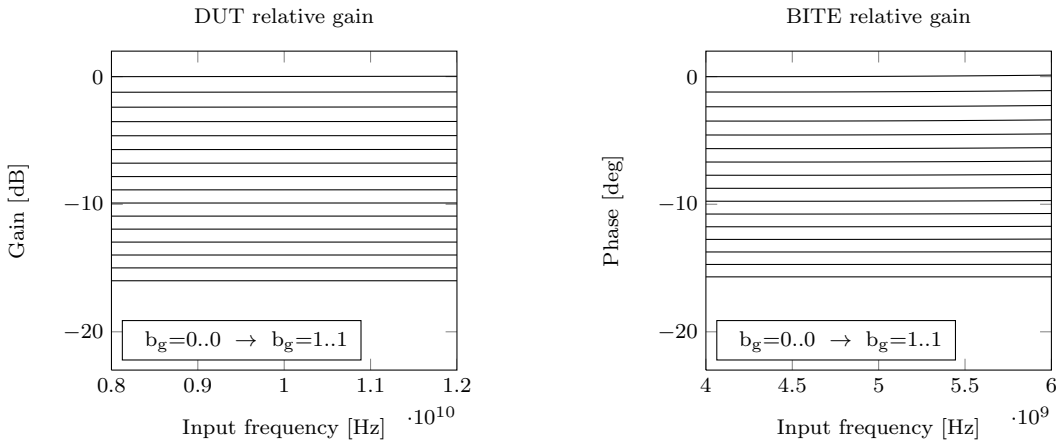

Figure 5.28: Relative gain difference of DUT and BITE.

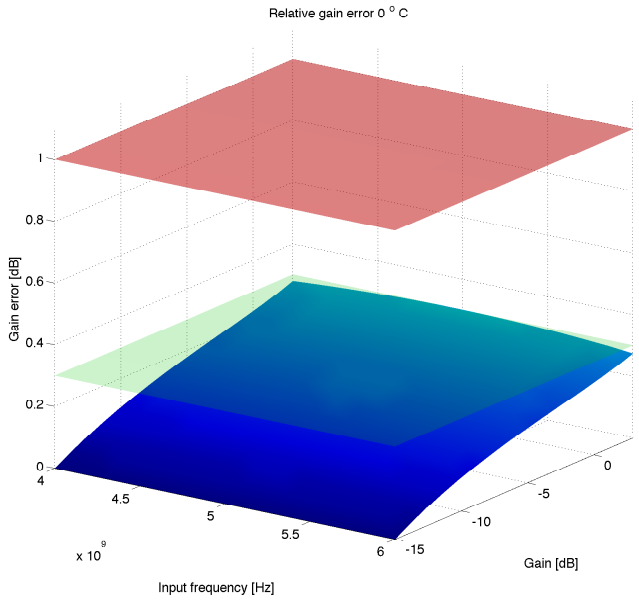

Figure 5.29: Relative phase measurement error at 0^oC

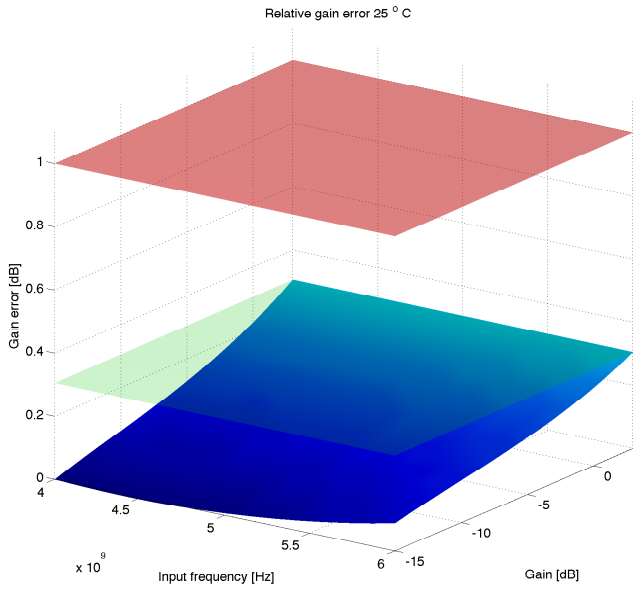

Figure 5.30: Relative phase measurement error at 25^oC

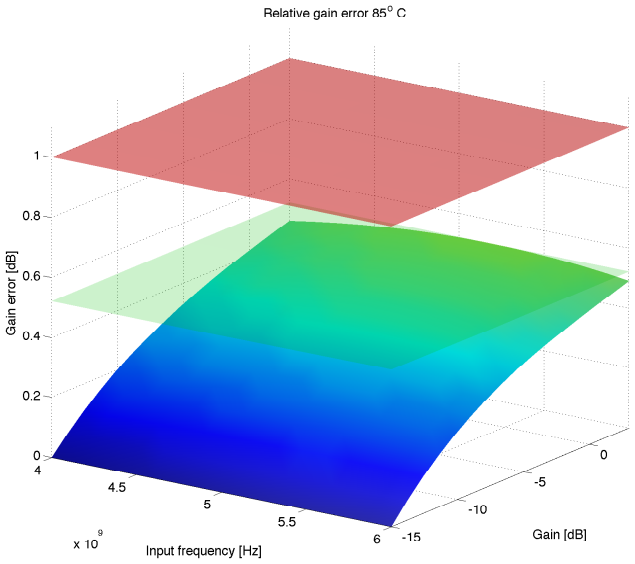

Figure 5.31: Relative phase measurement error at 85^oC

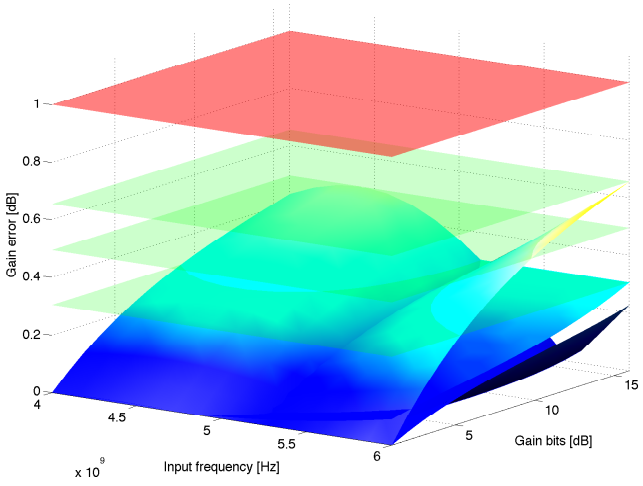

Figure 5.32: Relative phase measurement error at different phase shifts

CHAPTER 6

Summary and conclusions

In this work, a high precision built in test equipment for X band phased array systems has been presented. The first chapter has covered an overview of phased array radars, describing the dependence of the beam steering precision on the time delays introduced by the true time delay block and gain introduced at every element of the array. The DUT characteristics and the performance requirement for the BITE system are presented together with the figures of merit utilized to describe its performance and a brief description of the technology utilized. In the second chapter, the frequency doubler, frequency divider and polyphase filter which are the main components of the BITE, are analyzed using a high level approach in order to investigate their theoretical operation and make some design topology choices based on it. In the conclusion of the chapter, some alternative solutions that have been discarded due to their not optimal affinity with the given specifications are presented. The introduction part of the work is than followed by the design of the BITE building blocks, starting from the frequency multiplier, which is designed to provide the larger possible input test signal for the DUT, without causing problematic distortions or gain compression. Then, the quadrature signal generator is designed, us-

ing a single stage polyphase filter which generates two quadrature differential signals. Finally, the last stage of the BITE, which is the analog multiplier, is dimensioned by translating the measurement precision requirements into specifications on the LO driver of the multiplier. The negative effects introduced by the LO feedthrough are also considered. After the design procedure, and a brief overview of the custom layout developed for every part of the system, the entire BITE is simulated to verify its performance versus temperature, voltage supply, input power, mismatch and process variations. The simulation results provide some advices on how the measurement on the radar chip should be performed to weaken the LO feedthrough influence: the relative phase difference should be measured setting the maximum gain available for the DUT, and the gain measurement should be done by setting the control bits of the phase shifter block to the smallest delay possible, which corresponds to the minimum attenuation of the test signal.

In conclusion, all the specifications are met, starting from the low area request, (area is a tiny $0.1mm^2$), to the relative phase and gain measurement errors which in simulation is below the maximum value allowable. The DC power consumption of the entire BITE, is of 396mW. All the previous considerations have been made by taking into account the simulation results on the system. If the prototype chip confirms in measurements the simulation results, the BITE can be integrated in every element of a X band phased array radar system implying the possibility to use Advanced test equipment to perform tests in a fast and mass market standard way.

List of Figures

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