Università degli Studi di Padova
Facoltà di Ingegneria

Corso di Laurea Magistrale in Ingegneria Elettronica

Tesi di laurea

Implantable active high resolution electrodes for real-time field potential mapping

Elettrodi attivi impiantabili ad alta risoluzione per mappatura in tempo reale del potenziale di campo

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It doesn't seem to me that this fantastically marvelous universe, this tremendous range of time and space and different kinds of animals, and all the different planets, and all these atoms with all their motions, and so on, all this complicated thing can merely be a stage so that God can watch human beings struggle for good and evil - which is the view that religion has. The stage is too big for the drama.

— Richard Phillips Feynman, 1959

Considerate la vostra semenza: fatti non foste a viver come bruti ma per seguir virtute e canoscenza.

— Dante Alighieri, Inferno, Canto XXVI

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ABSTRACT

In this work a novel device for neural field potential measurement and mapping is presented, analysed and tested. After introducing the origin and properties of the signal to be measured, an overview of state-of the art technologies is given. Then the C-100-A active semiconductor needles are presented, and their design layout and structure is detailed. The devices are thoroughly simulated and possible issues and critical points are spotted. Device characterisation is then carried out to verify the behaviour of the device and the criticalities are then evaluated and an origin for some of them is found in the design or in the implementation. Both short term patches to the issues - to immediately employ the needle in measurements - and long term redesign strategies are found and presented. The still open issues, which are planned to be investigated, are clearly exposed. Finally, the results of first ever measurements of *in-vivo* local field potential with this technology are presented.

Keywords: local field potential, needles, recording, in-vivo, fet, active, neural

SOMMARIO

In questo lavoro si presenta un nuovo dispositivo per la misura e la mappatura del potenziale di campo neurale. Dopo aver introdotto le proprietá del segnale da misurare, é data una carrellata dello stato dell'arte delle relative tecnologie. Sono poi presentati gli aghi a semiconduttore attivi C-100-A, e in dettaglio sono visti il loro design layout e struttura. Questi dispositivi sono poi approfonditamente simulati, e i possibili problemi e punti critici sono evidenziati. Viene poi svolta una estensiva caratterizzazione, per verificare il comportamento dei dispositivi cosicché le criticitá sono valutate e per alcune di esse é trovata un'origine nel design o nell'implementazione del dispositivo. Per ovviare a queste problematiche sono poi trovate soluzioni a breve termine - per permettere fin da subito l'utilizzo del dispositivo - e a lungo termine, e ciascuna é presentata. Le questioni tutt'ora aperte, che sono in corso di indagine, sono chiaramente esposte. Infine, sono presentati i risultati delle prime misure del potenziale locale *in-vivo* con questi dispositivi.

Parole chiave: potenziale di campo, aghi, registrazione, in-vivo, fet, attivi, neurale

ACKNOWLEDGEMENTS

Science leads to discovering and understanding something new through a long list of failures. It's not always easy to approach a new attempt with the correct mood, and a real satisfaction can be felt only when a large subset of questions and problems is answered and solved, which, in general, happens at once. We are not always good at failing on our own, and even at reasoning on our own, support of people is important. And support of dear people is even more important, because they are the most desired partners to share enthusiasm after having shared doubts and worries. The first important thanks goes then to Valeria, who without doubts supported my thoughts and beared my shots of craziness during this work, with so nice mood and love that helped me to do always the best. She pushed me when I was too lazy and scolded me when I was asking too much to myself. This journey was pretty long, and overlapped with so many things that can be uneasily counted. I must thank my parents Alessandro and Morena for being so patient yet pushy enough to never divert me from achieving this goal. And Fabio, thank you for helping me to merge this personal journey with the many other ones we are facing together.

This work was approached nearly by chance. Introduced by a good friend of mine, Giacomo Bassetto, this field of study instantly fascinated me so much that I ended up with dedicating to it nearly three years. Professor Vassanelli, from the department of biomedical sciences of University of Padova, always fascinated me with interesting and passionated discussions at the edge of neuroscience, and kept my journey on the right path. Professor Meneghesso, with his unleashed competence in microelectronics and devices, gave me many smith ideas and opinions on theoretical and practical problems, and always gave me the good tip for making smart tests and verifications. While carrying on this work, I had the privilege to work and discuss with a huge cloud of people with the most advanced and various skills in physiology, neuroscience, microelectronics, solid state physics and materials science. Really many people needs to be thanked, and any order would be wrong. Professor Roland Thewes allowed be to enter in the finest details of the technology and engaged with me interesting discussions about design choices, device realisation and improvements. Ph.D. Stefano Girardi, who introduced me the for the first time to this measurement technology and dipped me into the details. Ph.D. Marta Maschietto, who taught me how really those devices are used, and how an experiment is carried on. Discussions with her allowed to identify the important operating requirements of such device. Ph.D. Silvia Lattanzio, Ph.D. Andrea Urbani, Claudia Cecchetto and Roberto Fontana, the whole crew of the neurochip lab in Padova, were always available for engaging useful discussions, sharing their experience and even helping me getting to an idea by talking of something totally different. And finally the whole crew of MDM labs in Milan, for the experience, discussions and ideas shared in material physics and science.

Padova, 1 dicembre 2014 M. B.

INTRODUCTION

...or how the whole is greater than the sum of its parts.

Cognitive science is the interdisciplinary scientific study of the mind and its processes. It examines what cognition is, what it does and how it works. It includes research on intelligence and behaviour, especially focusing on how information is represented, processed, and transformed within live nervous systems and then perhaps foresees the possibility to apply this knowledge to thinking artificial machine systems.

Neuroscience, which the most fundamental part on which all cognitive science branches are built upon, is the study of the mechanisms and inner workings that determine the behaviour, flexibility and power of the nervous system. Not only involving pure neurobiology of neurophysiology - which mostly deal with the actual structure and mechanisms - but also with networking and signal coding theory, it aims to describe how the cooperation of the billion of repeated, simple, and interconnected structures builds a complex, flexible but specialised organ as the nervous system.

Without detracting anything to the peripheral nervous systems, which gives the ability of receiving stimuli, driving muscles and is even able to take automated actions, the most advanced organ of the nervous systems is the brain. In it, such cooperation and networking give rise to memory, experience, consciousness, perception, understanding, smartness, emotions. And, some who believe would say soul. Aristoteles would certainly agree with the conception that brain is one of the most fascinating realisations of his sentence: "ὑπερτέλειοι δέ εἰσιν ὧν τὰ μέρη συντεθέντα μείζονά ἐστι τῶν ὅλων" ("The whole is greater than the sum of its parts"). Brain functions are indeed greatly more complex that the functions of the single devices it is made of, and this scaling phenomenon has no equals of any kinds in nature[1].

Neuroscience is far away from having understood even a small part of what is under the hood, actually «there's plenty of room at the bottom» - would have said Richard Feynman if he was a biologist. Nonetheless, recent discoveries like the discovery of mirror neurons or that of plasticity, are really pushing knowledge at the speed of light in this field.

The ability to measure, detect and see inside the brain is a fundamental part of the scientific process of discovery in Neuroscience. This ability is a branch of Electrophysiology, which pioneer was actually Luigi Galvani in the 1790s with his studies on dissected frogs. He discovered that you can induce a dead frog leg to twitch with a spark [Piccolino, 1997]. And brain electrophysioogy mimics its field of study, as it has many levels of scale, somewhat in the same manner of human brain itself. In fact, it's not only a matter of measuring the behaviour of a single part, but also to collect very big data with large scale measurement spacing in the whole brain or its section. If a traditional scientist does experiments by downscaling simple test cases, in this field the opposite process is somewhat a must. In order to understand the behaviour of such a large population, an experiments can actually be a big stream of events to be investigated in a wide domain. Neuroscience needs powerful instrumentation to measure the electrophysiological phenomena happening both in a single

1 Without entering in the deep of this philosophical discussion, it must be noted that many organs forming systems inside the organism, as well as tissues forming organs, together are able to accomplish a fairly more challenging role than taken alone. But, their organisation for that purpose is *a priori* logical, mechanical and somewhat engineered; and this judgement can be expressed whether or not we are able to know or understand it in the whole part. It is clear that for the brain this is different. Its ending structure is rather auto-enginnering than engineered and its overall behaviour does not seem to be explainable with a plan, a mechanism, a "Ball filled with gears".

neuron and in a population occupying the volume of many cubic centimetres, and it's hard, at first sight, even to imagine how hard this task is. Even the author of this work was not able to figure out from where to where his path went.

The aim of this work is to provide a measurement instrument for the electric potentials inside the brain, which is able to be inserted into a living animal, and record along a two-dimensional array of points such signals track their propagation, detect how neurons interact each other by means of signals. This will help, among other things, to understand how degenerating diseases such as Parkinson [Boraud *et al.*, 2002] or Alzheimer, by coupling detected behaviours to brain functions; or even to revert their course, by developing neural protheses that help of even trains the neuron ensembles that got degenerated. Neural signal extraction and identification will also help to develop complex human-machine interfaces, which can allow always more intelligent protheses to be finely controlled by their wearers, and give sophisticated feedback to who lost part of their body.

This work was done within the framework of the CYBERRAT and REALNET projects investigated at University of Padova. Many of the consideration and experiences here developed are a great body of knowledge for the upcoming RAMP project.

FIRST CHAPTER The considered phenomena - communication of nerve cells and propagation of stimuli - is introduced, beginning from the electrical and chemical basis up to the devices and systems interconnecting a neural network, with a - basic, surely incomplete, but functional to the further speculations - explanation of their workings and interaction.

SECOND CHAPTER The different neural signal recording problems are discussed. Beginning with introducing the different neural signal measurements and then focusing on the *local field potential* LFP, the theory behind its formation is analytically detailed. The analysis leads then to build a source model for the signals that need to be captured.

THIRD CHAPTER Electrical recording is specifically considered. Many other kinds of mixed technologies (magnetic, optic, pressure-based) have been developed and are currently used, but are outside of the purpose of tis work. The state-of-the-art technologies for measurements, both with and without spatial resolution, or with single rather than multi-dimensional measurement point arrays, are briefly introduced, with particular focus to *in-vivo* recording. Their performances are compared in order to spot the actual needs and open issues for the next-generation measurement devices.

FOURTH CHAPTER The design, layout, structure and fabrication process of C-100-A needles is explained. The innovative design ideas, as well as the critical aspects, will be highlighted to that to constitute the substrate for the further characterisation and evaluation process.

FIFTH CHAPTER The C-100-A/CMOS needle chip characteristics are first evaluated theoretically and simulated, and the verified with both ad-hoc and standard characterisation techniques. The problem of correct biasing and the top oxide leakage - which are proven to be critical - are specifically addressed.

SIXTH CHAPTER After recalling the fundamental lessons obtained from the device simulation and characterisation, the execution two experiments is described, where the C-100-A/CMOS needles are employed to record signal in the rat brain. First results ever obtained with this kind of devices are then finally presented.

SEVENTH CHAPTER An evaluation of the work is carried out. Achieved goals, as long as still open issues, are discussed. The stock of the current status of the work is taken, and an overview of what are expected to be the next steps, both in the framework of this project and - more in general - in this niche of study, is given.

1 PHYSIOLOGY OF NEURAL COMMUNICATION

In this chapter, the considered phenomena - communication of nerve cells and propagation of stimuli - is introduced, beginning from the electrical and chemical basis up to the devices and systems interconnecting a neural network, with a - basic, surely incomplete, but functional to the further speculations - explanation of their workings and interaction.

1.1 NEURONS

As discussed, neural probes are sensor used to detect neural signals generated from a live neural tissue. In order to model the signal source types the sensor and recording system will deal with, it is fundamental firstly to understand the inter and outer phenomena that occur during neural signal propagation, and lately to see what physical alteration - that can be captured - the different combination of such phenomena have as a result in different probing configurations.

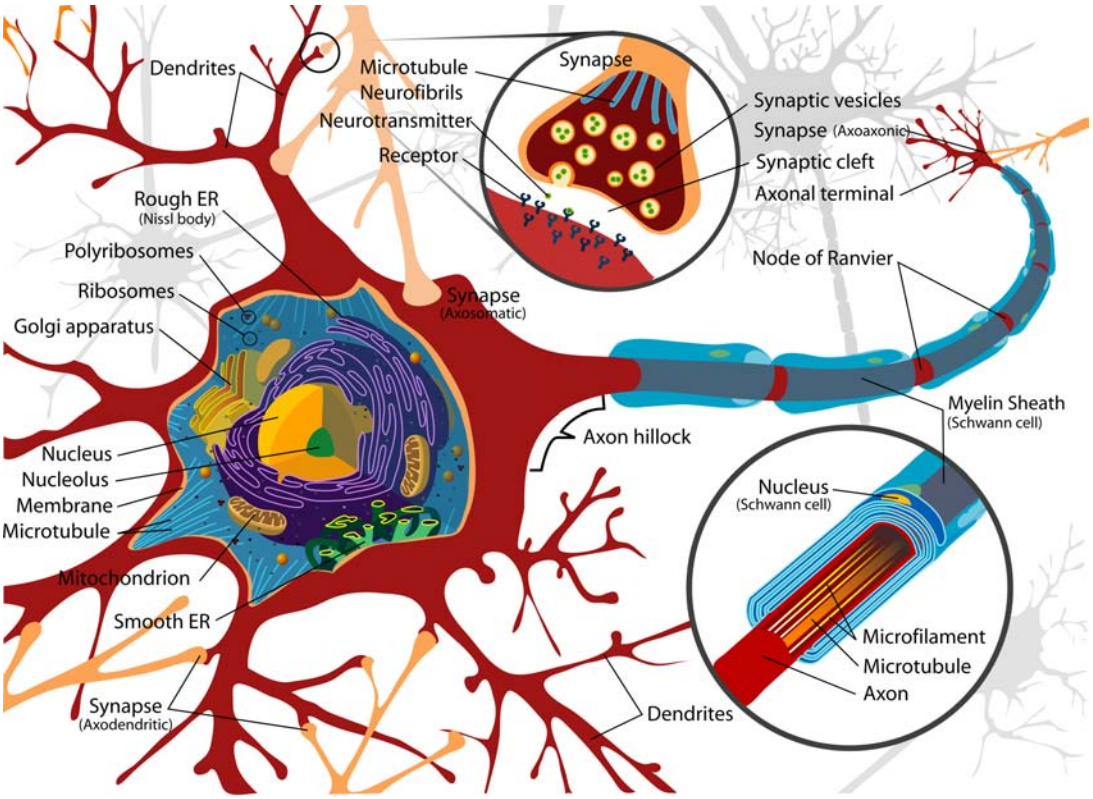

Figure 1: Detailed strutture of a neuron. [Source: Wikipedia]

As it is known, a neuron[1] is an excitable cell, that is a cell which, once stimulated, is capable of generating electrochemical impulses, which are small currents flowing through their

1 Also called *nerve cell*.

membranes. The propagation of such excitation is the second fundamental property of neuron and is the basis for neuronal signal propagation. In [fig. 1] we can see depicted a whole neuron with his main parts: the cell body[2], the dendrites, which are cell protuberances for input signals, and the axon with its terminal, which transmits and delivers the output signal. A neuron is basically a signal processor with multiple (distinguished) inputs and a single output[3].

1.2 ION CHANNELS AND MEMBRANE EXCITABILITY

The cell membrane[4] is a semipermeable[5] lipid bilayer common to all living cells. It contains a variety of biological molecules, primarily proteins and lipids, which are involved in a vast array of cellular processes.
Ions belonging to both sides of the membrane are subject to two kind of phenomena: drift and diffusion. Drift is originated from Coulomb's force and tends to null the point charge in the medium. Diffusion is originated from thermal agitation, whose randomness tends to null the chemical gradient of species, but its effect depends also upon the *membrane permeability* P_{ion} of each ion[6]. Ions are free to move as a result of the combination of the two resulting forces. When themodynamic equilibrium is reached - i.e. the electrochemical potential difference is null - the charge gradient is not null, thus resulting in a potential difference V_m which is also called the *membrane potential*. This potential, which is also described by the Goldman-Hodgkin-Katz equation (1), is usually settled between -40 and -90mV for many biological systems[7] (-70mV is common for mammalian) [Monticelli, 2009] and can be measured with microelectrodes or micropipette, with a setup which is described in [fig. 3]. This means that, being $E = -\Delta V$, there has to be an electric field directed from inside to outside the cell membrane, ad a positive charge buildup in the intracellular fluid.

$$V_m = \frac{RT}{F} \log \frac{P_K \cdot [K^+]_i + P_{Na} \cdot [Na^+]_i + P_{Cl} \cdot [Cl^-]_i}{P_K \cdot [K^+]_e + P_{Na} \cdot [Na^+]_e + P_{Cl} \cdot [Cl^-]_e} \tag{1}$$

in which the external $[\ldots]_e$ and internal $[\ldots]_i$ concentration of ions as long as their membrane permeability P are considered. The charge separation at membrane is depicted in [fig. 2].

Species present in the nearby of the cell membrane are Na^+, K^+, Ca^{2+}, Mg^{2+}, Cl^-, A^- however the former three are much more involved in the phenomena that determine cell membrane potential. Many devices present on the cell membrane contribute to alter membrane permeability to specific ions[8]:

- Passive channels, that allow ion migration according to the electrochemical potential gradient.
- Active channels, which are able to modulate their permeability, but yet allowing the migration according to the electrochemical potential gradient.

2 Also called *soma*
3 This is a generalisation for the sake of introduction. This sentence deserves further explanation in the following.
4 Also called the plasma membrane or *plasmalemma*.
5 I.e. it separates *intracellular* from *extracellular* fluid, allowing small ions and water to pass through it while stopping bigger molecules.
6 A very nice parallelism can be made with semiconductor theory. Carriers in a semiconductor are subject exactly to the same forces. The difference in ion concentration mixed with permeability is to a membrane system as the doping is to a semiconductor junction. The equilibrium at a junction is reached exactly with the same balance process between thermodynamic and Coulomb's forces.
7 Reference voltage for V_m is defined as the extracellular fluid voltage.
8 Or even to non-specific ions, even though this is less common.

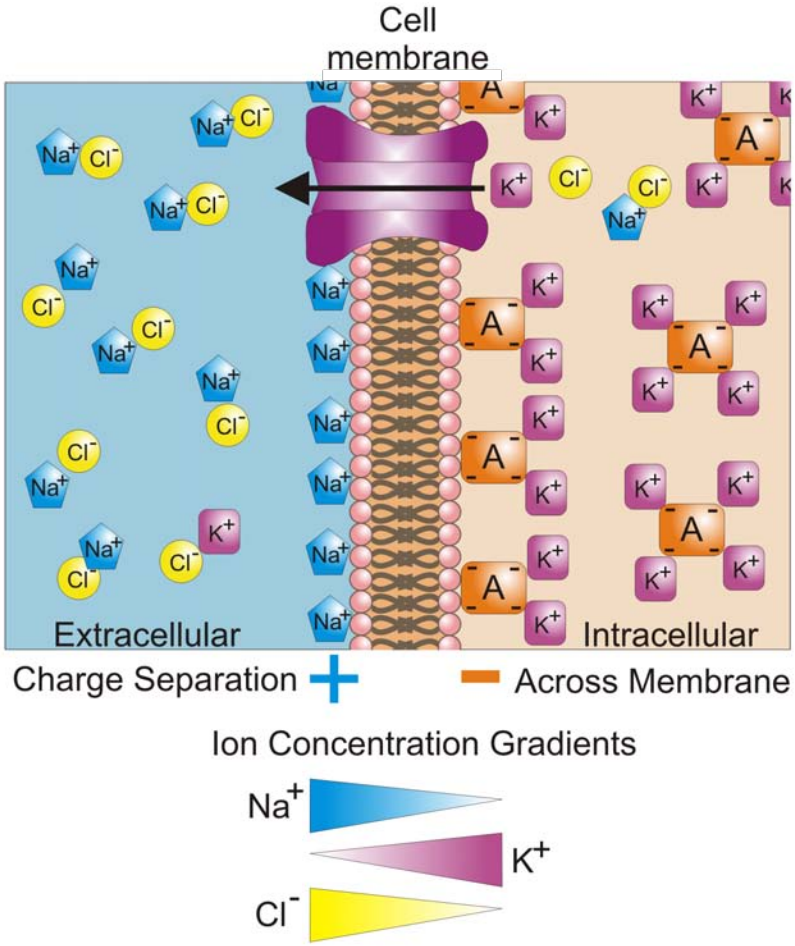

Figure 2: Cell membrane charge separation. The ion channels are represented as responsible for the specific membrane permeability to each ion. [Source: Wikipedia]

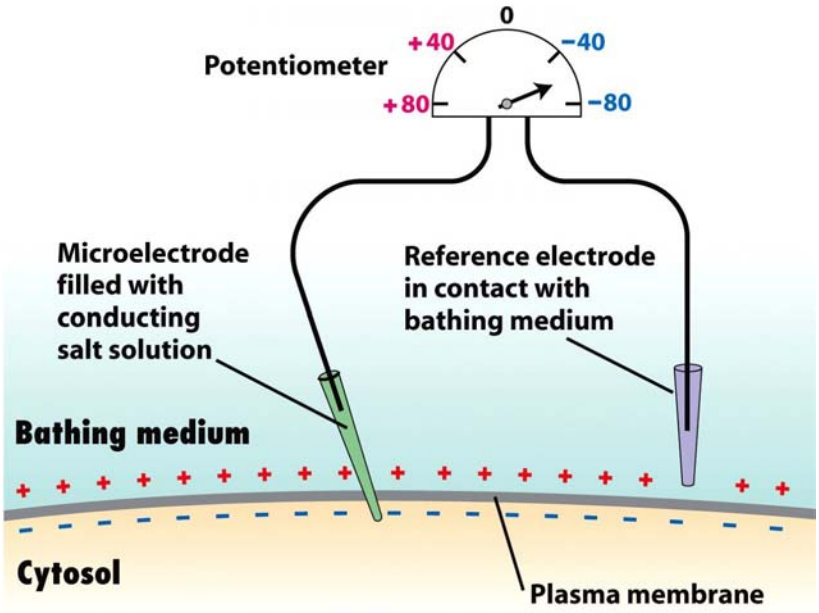

Figure 3: Cell membrane potential measurement setup. A pipette microelectrode and a reference electrode and placed respectively inside and outside the cell; the potential difference is then measured with a high impedance voltmeter (also known as galvanometer). [Source: [Lodish, 2008]]

- Pumps, like the which are Na^+/K^+ pump, which are active devices which are able to transport ions counter the electrochemical potential, at expense of chemical energy.

The third aforementioned devices are fundamental to maintain the equilibrium status: on fact equilibrium is defined with fixed ion concentration at both sides of the membrane. However, ion migration though membrane would alter such concentration, especially in the intracellular fluid, being it limited in volume. The action of the pumps then maintains the overall concentrations unaltered by ion migration.

1.3 GRADED POTENTIAL AND ACTION POTENTIAL GENERATION

The aforementioned active channels can often be activated by different means:

- mechanical stimuli, such as strain, vibrations, which are able to activate some mechanically-controlled Na^+ channels;
- chemical stimuli, such as neurotransmitters which act on ligand-gated Na^+ channels;
- electrical currents which drive Na^+ and Ca^{2+} voltage-dependent channels.

While K^+ ion is much more involved in keeping the membrane potential at rest, Na^+ is responsible for receiving and propagating stimuli.

1.3.1 Synapses and synaptic currents

Synapses are communication devices interconnecting neurons. They are located at the terminal part of an axon of the *presynaptic neuron*, and they can be more than one per axon, or can be located in general at the cell membrane. Synapses receive the stimulus from the

neuron that belong to and are able to transmit it to another nerve cell, through the release of chemical compounds (neurotransmitters) which are able to excite ligand-gated channels, or by allowing the direct migration of ions between two nerve cells. Those are named *chemical* and *electrical* synapses, respectively. The membrane currents exchanges as a consequence of a synaptic stimulus are called *synaptic currents*. A neuron has generally many hundreds of input synapses connected, which often completely tessellate its somatic and dendritic surface [Monticelli, 2009]. Synapses can transmit either an *excitatory* or *inhibitory* stimulus - that are depolarising or hyperpolarising, respectively - and are also able to modulate their gain, that is the strength with which the stimulus is transduced. This modulation, called *synaptic plasticity*, derives from an internal state of the device which tracks memory of the recently transmitted stimuli, making the communication not static, but dynamic and influenced by transmitted data itself. This memory can last from few minutes (*short-term plasticity*) to a few hours (*long-term plasticity*). Although a deep explanation of synapses' inner working being not in the scope of this section, the structure of chemical ones is barely shown in [fig. 1], in which the vesicles delivering neurotransmitters in response to a tumulus, and then exciting receptor's ion channels, are visible.
it is worth to say that synapses are believed to be the real devices constituting the neural network, and giving its properties of learning, and somewhat, intelligence. In the end, neurons are only integrators, but real signal processing and mining of the big amount of data flowing through the neural networks are accomplished thanks to the adaptive properties of the synapses[9].
Two mechanisms contribute to the propagation of the received stimuli: *graded potential* and *action potential*.

1.3.2 Graded potentials

A graded potential is the most intuitive form of potential disturbance that can take place at a cell membrane. It is generally caused by synaptic stimuli[10], thus involving ligand-gated ion channels and not voltage-dependent channels. The activation of such channels determines a net current flow trough the membrane, and so alters local charge density, thus changing the local membrane potential. Such potential difference depends in magnitude on the number of channels activated, that cause variable current intensity. For this reason, and for their exponential fading in the intracellular fluid with respect to the source point, they are called *graded potentials*[11]. The length constant of such exponential decay depends mainly on the membrane and intracellular fluid resistance, and it is typically 1-3mm on most mammalians [Monticelli, 2009]. The described phenomenon is depicted in [fig. 4].

Graded potential can consist in a positive or negative drift of the local membrane potential, which are respectively called *hyper-* and *de-* polarisation. This mainly depends on the type of ion channels involved (Cl^- and K^+ in the former case, Na^+ and Ca^{2+} in the latter). Many mechanisms restore the initial condition of the membrane potential after the transient. Often this process involve an auto-inhibitory mechanisms in the ligand-gated channels or in the end of the original stimulus itself. Then the passive or pumping transports restore the original ion distribution. It is important to notice that, although the potential buildup could seem an integrating mechanism, a longer stimulus always results in a longer membrane polarisation but does not increase the magnitude of the latter.

9 (Author's note)
10 For this reason that are classified as *postsynaptic potentials*.
11 The contamination of potential is due to charge motion to nearby membrane zones and is also called *potential spread*.

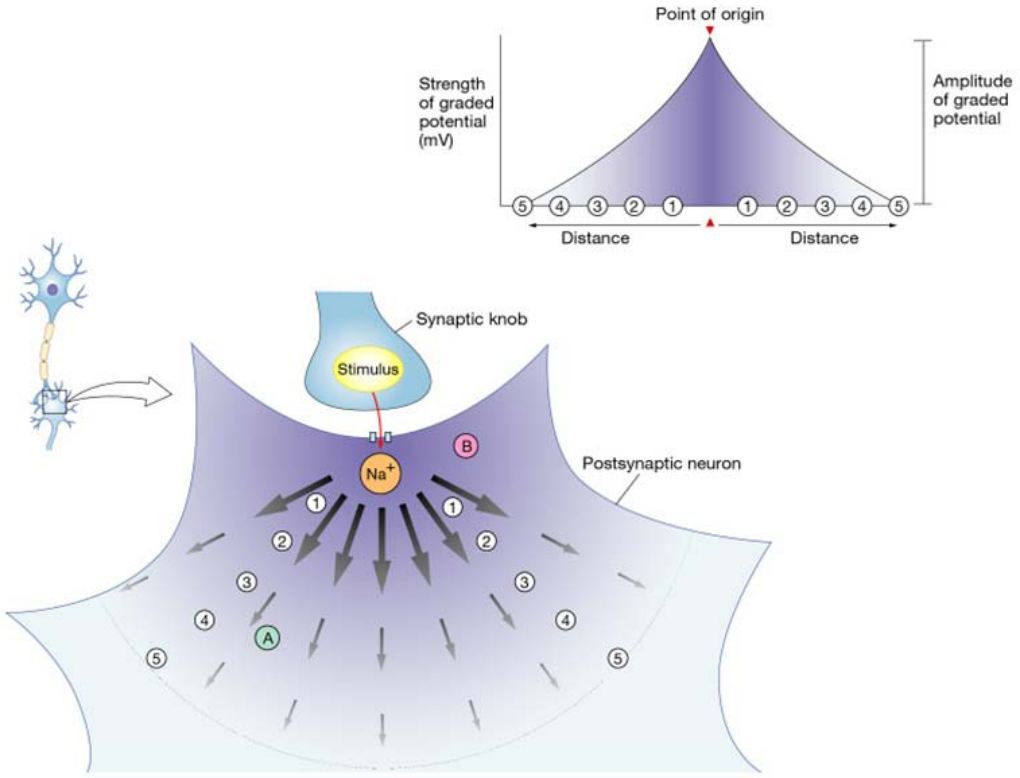

Figure 4: Propagation of a graded potential as a result of a synaptic stimulus. [Source: http://faculty.pasadena.edu]

1.3.3 Summation and triggering

Neuron processing basically consists in integration[12]. When considering a specific point of the cell, the combined effect of multiple graded potentials that originate in different source points at the membrane must be evaluated. A sort of linear combination of the effects comes into help: the resulting signal at a point is approximately the sum of the graded potentials effect at that point, properly scaled with the decay spatial constant. This is actually called *spatial summation* and represents a way in which a higher excitation peak value build up coming from distinct lower signals. Even *temporal summation* can occur, when a unique stimulus is repeated quickly enough that parts of itself superimposes, so that a higher signal is propagated. Of course, signed combination happens, so that the summation of hyper- and de-polarisating[13] potentials results in a lower magnitude signal. Such different contributions can come from different type of synapses acting as inhibitory of excitatory. A schematisation of such phenomena is given in [fig. 5].

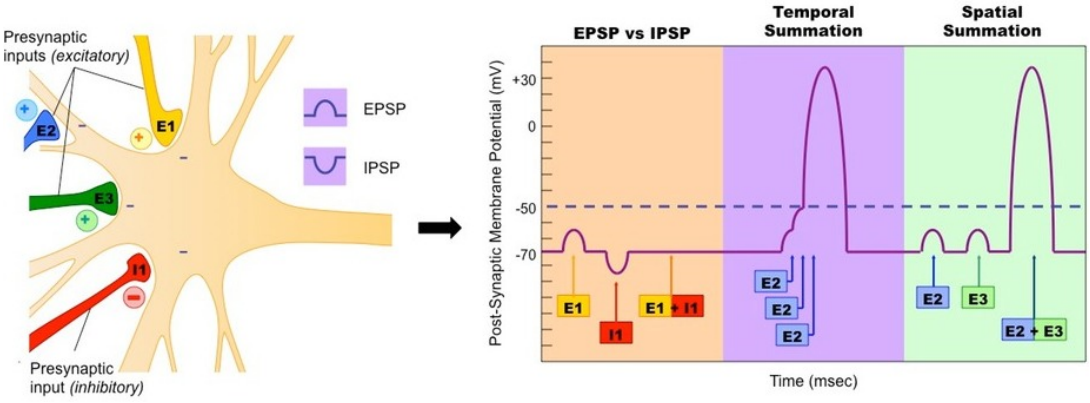

Figure 5: Summation of graded potentials.

When, either by cause of a single potential (which is unlikely to happen) or by summation, a determined threshold is exceeded, voltage-activated ion channels give rise to an avalanche process which results in a much higher signal, called *action potential*. This typically occurs in a predefined neuron cell zone, called the *trigger zone*[14] and a common threshold value for mammalian cells is -55mV [Monticelli, 2009].

1.4 ACTION POTENTIALS

The mechanism giving rise to action potential was discovered by Hodgkin and Huxley[15] [A. L. Hodgkin and A. F. Huxley, 1939]. The mechanism originating action potentials is due to a positive feedback aided by voltage-dependent channels. The process is divided in many phases, that result in the particular shape of the signal which is shown in [fig. 6].

- **Stimulation, rising phase**: typically, the way in which a depolarising stimulus is delivered is the injection of extra sodium cations into the cell and potassium cations outside it, regardless of the mechanism that caused it. For a neuron at rest, Na^+ is concentrated outside the cell, whereas the contrary is true for K^+ ions. If the depolarisation

12 Intended in the Riemann flavour.
13 Also caller *excitatory* (EPSP) and *inhibitory* (IPSP) respectively.
14 It is typically located at the beginning of the axon.
15 Actually studying membrane potentials in the so-called *giant squid axon*.

is relatively small, the outward potassium current overwhelms the inward sodium current and the membrane repolarises back to its normal resting potential. However, if the depolarisation is large enough, the inward sodium current increases more than the outward potassium current and a runaway condition (positive feedback) results: the more inward current there is, the more V_m increases, which in turn further increases the inward current. A sufficiently strong depolarisation causes the voltage-sensitive sodium channels to open; the increasing permeability to sodium drives V_m closer to the sodium equilibrium voltage $E_{Na} \approx +55mV$. The increasing voltage in turn causes even more sodium channels to open, which pushes V_m still further towards E_{Na}. This positive feedback continues until the sodium channels are fully open and Vm is close to E_{Na} [Bullock *et al.*, 1977].

- **Peak, fall phase**: The positive feedback of the rising phase slows and comes to a halt as the sodium ion channels become maximally open. At the peak of the action potential, the sodium permeability is maximized and the membrane voltage V_m is nearly equal to the sodium equilibrium voltage E_{Na}. However, the same raised voltage that opened the sodium channels initially also slowly shuts them off, by closing their pores; the sodium channels become inactivated. This lowers the membrane's permeability to sodium relative to potassium, driving the membrane voltage back towards the resting value. At the same time, the raised voltage opens voltage-sensitive potassium channels; the increase in the membrane's potassium permeability drives V_m towards $E_K \approx -75mV$. Combined, these changes in sodium and potassium permeability cause Vm to drop quickly, repolarising the membrane and producing the "falling phase" of the action potential.

- **Afterhyperpolarisation**: The raised voltage opened many more potassium channels than usual, and some of these do not close right away when the membrane returns to its normal resting voltage. In addition, further potassium channels open in response to the influx of Ca^{2+} ions during the action potential. The potassium permeability of the membrane is transiently unusually high, driving the membrane voltage V_m even closer to the potassium equilibrium voltage E_K. Hence, there is an undershoot or hyperpolarisation (i.e. afterhyperpolarisation) that persists until the membrane potassium permeability returns to its usual value.

- **Refractory period**: Each action potential is followed by a refractory period, which can be divided into an *absolute refractory period*, during which it is impossible to evoke another action potential, and then a *relative refractory period*, during which a stronger-than-usual stimulus is required. These two refractory periods are caused by changes in the state of Na^+ and K^+ channels. When closing after an action potential, sodium channels enter an "inactivated" state, in which they cannot be made to open regardless of the membrane potential. This gives rise to the absolute refractory period. Even after a sufficient number of sodium channels have transitioned back to their resting state, it frequently happens that a fraction of potassium channels remains open, making it difficult for the membrane potential to depolarise, and thereby giving rise to the relative refractory period [Monticelli, 2009].

The absolute refractory period is largely responsible for the unidirectional propagation of action potentials along axons. At any given moment, the patch of axon behind the actively spiking part is refractory, but the patch in front, not having been activated recently, is capable of being stimulated by the depolarisation from the action potential.

It is important to notice that an action potential is an *all-or-none* phenomenon. Regardless on the actual signal magnitude over the threshold, the potential is generated always the same. Shape and duration of action potential are not dependent on the original stimulus

shape, provided it is over the threshold[16]. The ignition of an action potential is also called *firing* and the temporal sequence of action potentials coming from a neuron are called *firing patterns*.

A partial nonlinear differential equation model was developed by Hodgkin and Huxley in 1952 [A. Hodgkin and A. Huxley, 1952] and takes their names. Despite an analytic solution to this model was not found, numerical simulations proved his reliability[17] and the equilibrium and bifurcation points between its behaviours.

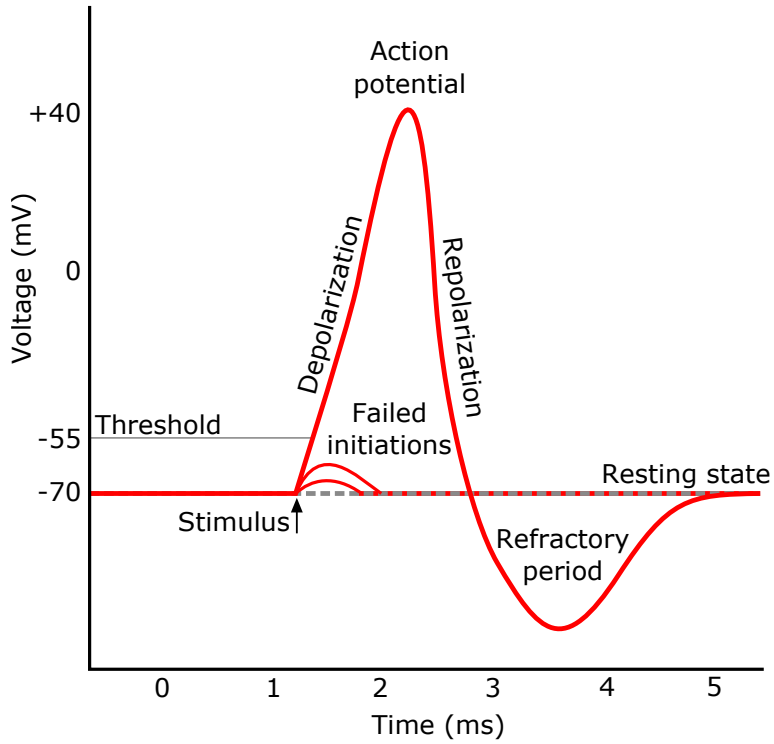

Figure 6: Approximate plot of a typical action potential shows its various phases as the action potential passes a point on a cell membrane. The membrane potential starts out at -70 mV at time zero. A stimulus is applied at time = 1 ms, which raises the membrane potential above -55 mV (the threshold potential). After the stimulus is applied, the membrane potential rapidly rises to a peak potential of +40 mV at time = 2 ms. Just as quickly, the potential then drops and overshoots to -90 mV at time = 3 ms, and finally the resting potential of -70 mV is reestablished at time = 5 ms. [Source: Wikipedia]

1.4.1 Action potential propagation

Inspiring to the properties and behaviour of the action potential, it is pretty strait forward to hypothesize how it propagates along an axon. An axon is actually a membrane tube, which diameter is in the range of $1 - 20\mu m$ for the mammalians[18], and as mentioned is an extension of the cell itself. When an action potential is fired on the trigger zone - which is located at the beginning of the axon - the local section of the axon is immediately depolarised. The propagation of a local graded potential induces depolarisation in the nearby zone, in

16 This suggests an interesting parallelism with digital circuitry, in which information is not codified in signal amplitude but in signal boolean state. It will be clear afterwards that neurons have all the way a coding for original signal amplitude, which makes them behave also like an A/D converter, in a bold analogy.

17 It actually did worth the Nobel Prize in Physiology or Medicine to the two scientists.

18 It is worth to mention the squid axon, largely used for physiology experiments, which diameter is up to 1mm.

which then threshold is exceeded and a new action potential is generated. At this point, only the successive axon section (called *distal*) is excited, being the preceding zone still in refractory status. This way propagation is unidirectional. In [fig. 7] the dynamics of this phenomenon are represented.

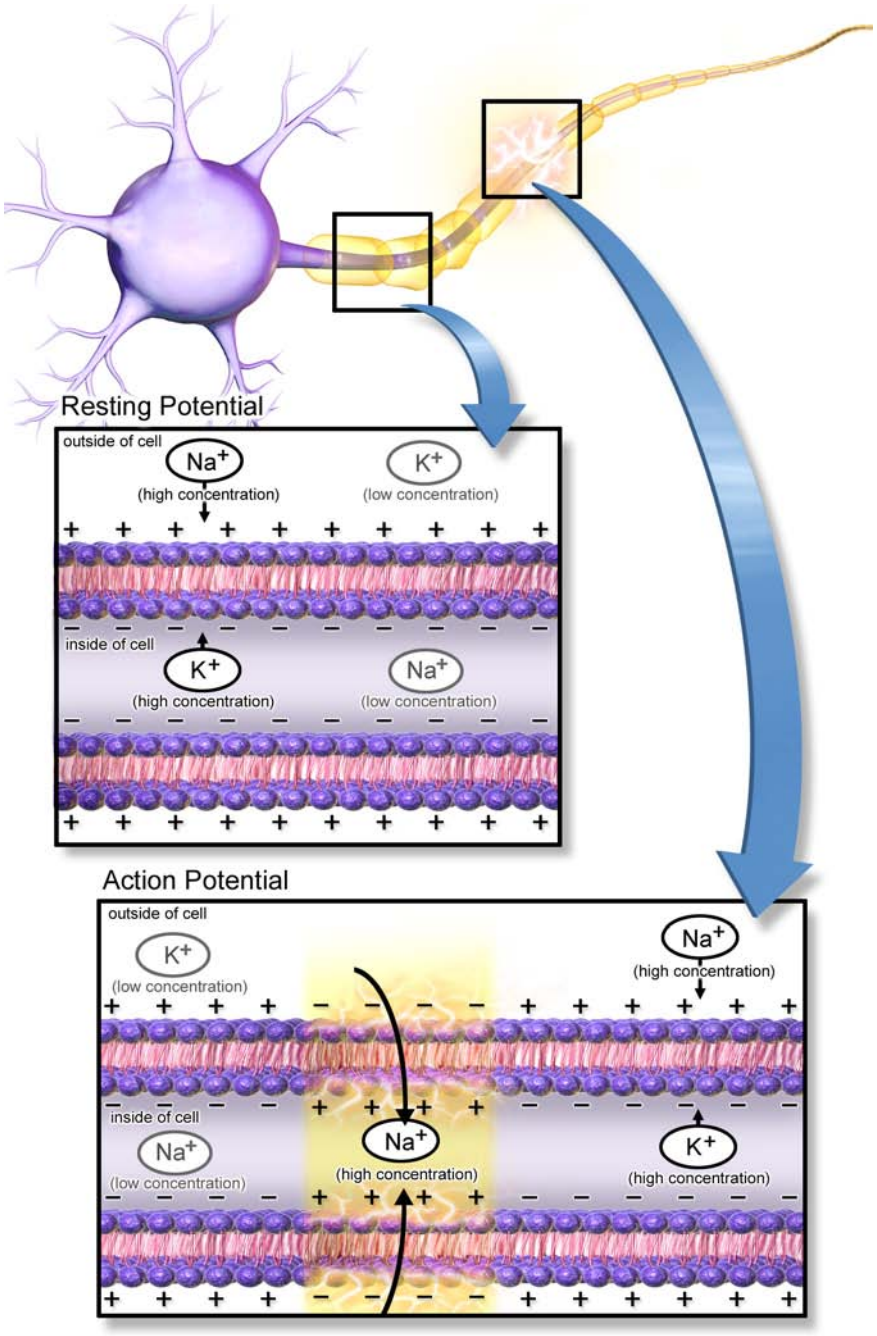

Figure 7: Action potential propagation along an axon. [Source: Blausen.com staff]

PROPAGATION MODEL The physics of the underlying phenomenon suggests an analogy called *cable theory*, that is a theory describing the propagating potential in the same way

as travelling waves in electrical transmission lines[19]. Despite being described as a lumped-element problem, this is actually a continuous space problem with distributed parameters. Actually, Hodgkin and Rushton A. Hodgkin and Rushton, 1946 studied the phenomenon in this flavour, coming to the equation [2] which describes what it to all effects an attenuating wave equation[20].

$$\tau \frac{\partial V}{\partial t} = \lambda \frac{\partial^2 V}{\partial t^2} - V \tag{2}$$

in which V(x,t) is the membrane voltage and $\tau = r_m c_m$ and $\lambda = \sqrt{\frac{r_m}{r_l}}$, which are propagation time and length constant, are calculated upon the discretised equivalent parameters per unit length, calculated on a circular axon. In particular, c_m is the membrane capacity and r_m is the transmembrane leakage resistance. r_l is instead the longitudinal resistance which is internal to the axon and is given by the cylindric volume of cytosol.
It can be easily found that propagation speed depends on the ratio between leak resistance and conduction resistance. Being those parameters dependant from axon geometry and dimension, it can be easily proven that higher axons are less leaky and thus provide a higher propagation speed. Having axons of no relevant section, in mammalians propagation speed lies around some metres per second [Schmidt-Nielsen, 1997].

As the amplitude of a potential propagating through the axon decays, it is regenerated by triggering a new action potential as described before[21]. In the end, as introduced, signal amplitude and shape is not relevant for the transmitted information, but only the timing and repetition of the spikes[22]. It can be seen from [fig. 8] that signal intensity does not cause a higher level of action potential, but rather an increase on repetition pulse of the spikes, which are summed to the original stimulus[23]. After a few propagation steps, the signal component vanishes and only spike frequency is detectable. [fig. 9] shows repetitive neuron firing as a consequence of an artificial stimulation. Firing pattern is superimposed to the stimulus current waveform.

It is worth to say that, as the neuron receiving this signalling will perform integration, thanks to temporal summation of repeated spikes, the original signal amplitude is actually recovered. This closes the *coding* loop.

ACTIVE AND PASSIVE MEMBRANES Cable theory was originally built before the regenerating, nonlinear properties of membrane was discovered. For this reason, it takes into account only passive elements. Although many attempts to improve cable theory for the so-called *active* membranes are being carried on, the formulation proposed here is still useful to describe saltatory propagation, propagation in passive zones and inside passive neurites. Passive neuron models are still a very interesting way to predict extracellular potential sources.

1.4.2 Saltatory conduction

Some nerve fibres are coated with *myelin*, a substance witch forms a sheath made up to many hundreds of spiral layers. Those sheaths are part of distinct cells, called Schwann cells or oligodendrocytes[24]. Their structure, surrounding the axon, is depicted in [fig. 10] and is

19 A topic that is today very dear to who deals with IT and telecommunications.
20 i.e. it is categorised as a particular form of D'Alembert equation, an equation describing the propagation of a wave, a phenomenon patterned both in time and space.
21 This phenomenon is more clear in the next section: saltatory conduction. Actually, when all the interested membrane is active, attenuation can take place only between one sodium channel and another.
22 Again, a parallelism with digital systems arises: amplitude dynamics is superseded by signal timing and noise is fought with signal regeneration.
23 Actually also a persistent stimulus cause a spike repetition.
24 For the peripheral and central (PNS and CNS) nervier system respectively.

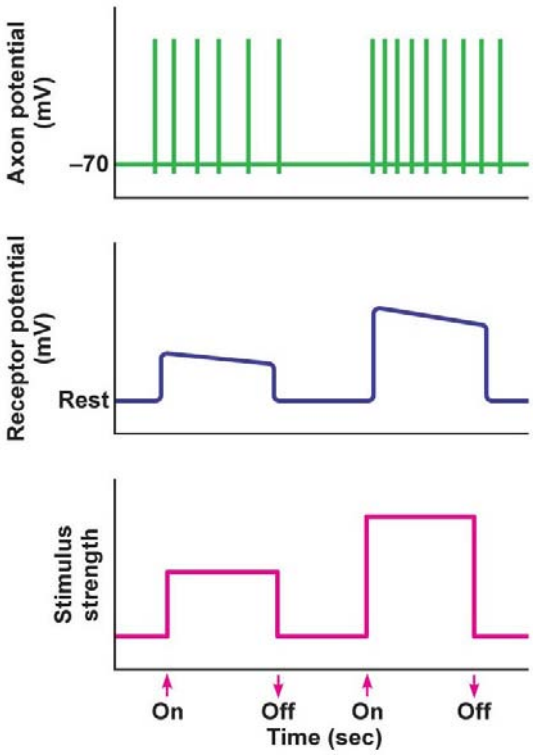

Figure 8: Action potential propagation along an axon. [Source: Pearson Education, Inc.]

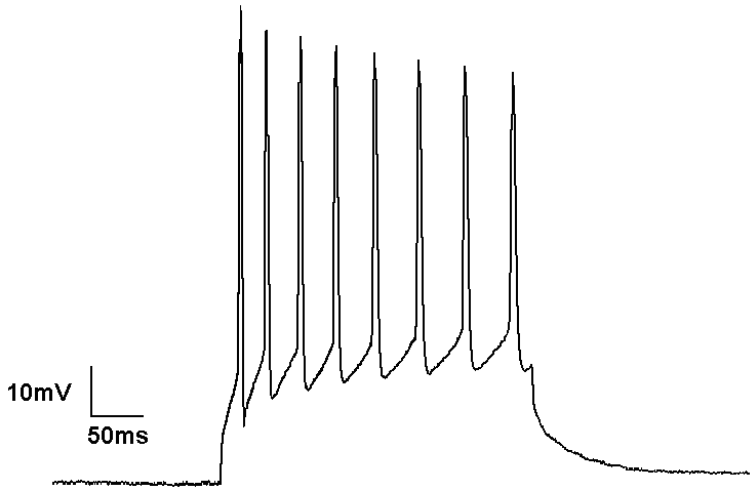

Figure 9: Whole-cell current clamp recording of a neuron firing due to it being depolarized by current injection. [Source: Wikipedia]

generally divided in 1-2mm sections interleaved by $\approx 1\mu m$ of exposed axon, called *Ranvier node*.

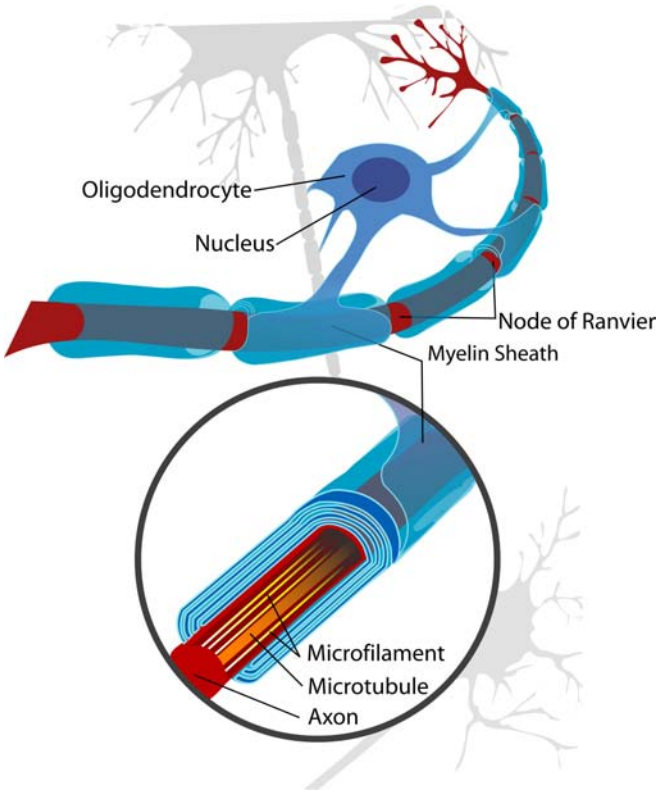

Figure 10: Structure of nerve axon with myelin sheath. [Source: Wikipedia]

The myelinated section of the axon is not provided with ion channels, but the myelin sheath increases greatly the leakage resistance r_m and decreases membrane capacity c_m thus speeding up propagation and decreasing attenuation[25]. Regenerating effect takes places only at Ranvier nodes, in which ion channels are available; however their density is higher than non-myelinated fibres, so that gain is higher. This propagation mode is called *saltatory conduction*. Attenuation is so improved by sheaths that regeneration is actually unnecessary between each Ranvier node.Overall propagation speed is improved even 10 times thanks to myelin, and can reach over 100 m/s in the thicker fibres [Monticelli, 2009]. Finally, there overall amount of ions exchanged by the membrane to perform signal regeneration is greatly lower than the case of an action potential propagated for the same distance without myelin sheaths: this way the membrane is more efficient and less pumping is necessary to support its operation.

25 Perfectly like an improved coaxial cable in which inductance is lowered with a good shield and capacitance is lowered too by using a low-k dielectric (ideally air).

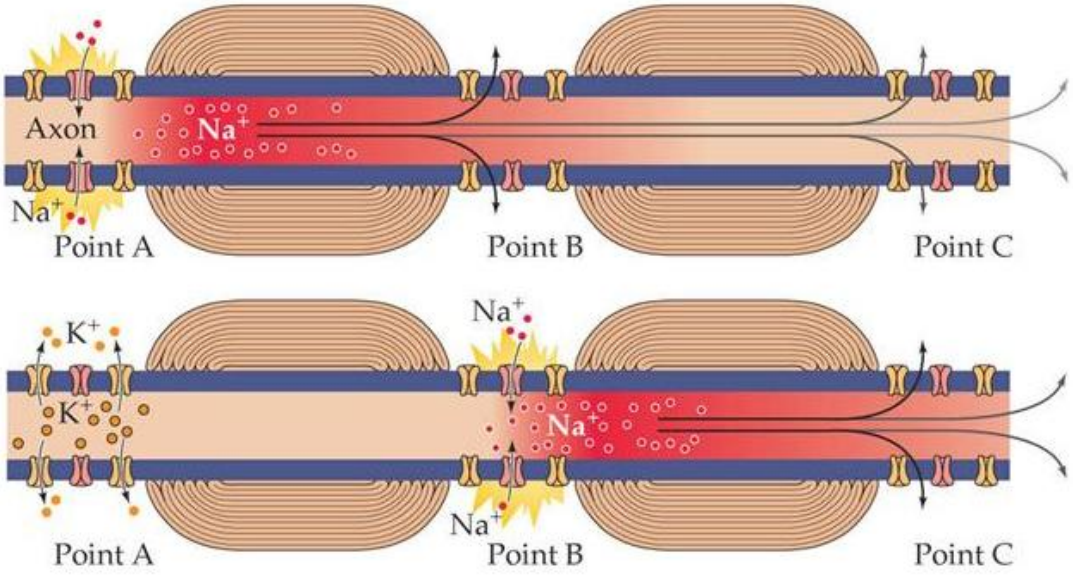

Figure 11: Saltatory signal propagation along an axon. [Source: [Purves *et al.*, 2008]]

2 PROBLEM MODELING

In this chapter, the different neural signal recording problems are discussed. Beginning with introducing the different neural signal measurements and then focusing on the *local field potential* (LFP), the theory behind its formation is analytically detailed. The analysis leads then to build a source model for the signals that need to be captured.

2.1 ORIGIN AND MEASUREMENT OF EXTRACELLULAR FIELD

The extracellular fluid is a conductive medium which volume conductivity σ is in the range of many tenths of mS/m [Dobiszewski *et al.*, 2012]. In the presence of currents, a voltage field is then defined all over the medium. The extracellular voltage V_e is defined as the voltage that can be measured in an arbitrary point of the extracellular space with a setup similar to that in [fig. 3] in which the reference electrode is positioned at a sufficient distance from the measurement point. All the electrical phenomenons influencing the nearby space sum up their contributions to form this *field potential*, which is also called *local field potential*, or LFP[1]. In the summation, amplitude, signs and phase as well as distance[2] from the source must be considered.

Although the major contributor of the extracellular signal is the synaptic transmembrane current, other sources - including Na^+ and Ca^{2+} spikes, ionic fluxes through voltage- and ligand-gated channels, and intrinsic membrane oscillations - can substantially shape the extracellular field [Buzsáki *et al.*, 2012]. In is important to understand, that, regardless the considered source, the current contributing to generate the field will always be a ion channel or membrane leakage current, that is a byproduct of signal propagation which is necessary to allow signal to be regenerated, in the former case, or totally parasitic, in the latter.

- **Synaptic activity** is the most important source of extracellular current flow in most physiological situations. Multiple slow events, such as synaptic currents, have the highest probability to overlap in time to build up a measurable signal. Input synapses often fill all the surface of a neuron and come from nearby, to there is a high chance of many of them to fire simultaneously. Ligand-gated channels, when activated by neurotransmitters, determine the influx of cations in the cell, thus constituting a current *sink*, which is balanced in a medium time by current *sources* along the neuron made up by opposite ion channels or active pumps. This way, a multipole is generated.
- **Fast action potentials** are the so-called *spikes*. Despite the fact their resulting voltage amplitude is often higher that of synaptic current (up to tenths of millivolts), their chance of superposition is much lower, because their time constant is really fast (<2ms). However, high chances of synchronous firing of nearby neurons and phase-locking phenomenons were observed [Buzsáki *et al.*, 2012]. So they contribute to the high-frequency components of the LFP, where other sources do not give contributions.
- **Calcium spikes** are long lasting (10-100ms) high magnitude (10-50 mV) that are able to contribute significantly to the LFP. These are dendritic spikes, often triggered by

1 The term *local field potential* (meaning the electric potential (V_e)), is a regrettable malapropism, but we continue to use the term LFP because it is familiar to most neuroscientists [Buzsáki *et al.*, 2012].

2 In a leaky isotropic conductor voltage decreases as $1/r$.

N-Methyl-D-aspartic acid[3] (NMDA) receptors, which are able to propagate along the membrane by firing action potentials, and even be fired by back propagating stimuli.

- **Intrinsic currents and resonances** the membrane of some neurons can exhibit a resonance behaviour. The voltage-activated channels together with capacitances can respond to specific frequencies and, when intracellular depolarisation is strong enough, a self oscillation can be sustained.[4] If this oscillation is synchronous in a group of neurons, a contribution to LFP can be detected.

- **Spike afterhyperpolarizations (AHPs)** can contribute to LFP because their magnitude depends on the integration of a spike burst: the increase of intracellular ion concentration due to successive spikes can trigger the activation of other ligand-gated channels thus inducing further, long-lasting polarisation, comparable in intensity to synaptic events. This contribute is emphasised when nearby neurons are firing together.

- **Gap junctions** Inter-neuron communication through electrical synapses[5] can affect neuronal excitability and so indirectly contribute to LFP.

- **Ephaptic effects** are essentially electrical couplings between adjacent neurons or axons. Individual neurons are unlikely to be able to interfere each other through *ephaptic coupling*, but group firing can generate strong enough spatial current distributions to alter the field potential of a nearby neuron membrane[6].

2.1.1 LFP power spectrum

It has been observed that LFP has to a flat power spectrum, but rather a $1/f^h$ power law, which is the characteristic of a Brownian noise. Although the actual exponent is not constant, this behaviour suggests that network communication could be a dominant cause of it and different models have been proposed [Milstein *et al.*, 2009]. For sure the low-pass frequency response of dendrites is shaping such signal at a first stage, and this filtering is purely passive and morphology-dependent. However, network mechanism also contribute to that particular feature: in longer time windows the activity of more nearby neurons can contribute to the LFP, therefore generating more intense potential at lower frequencies[7]. Also modulation phenomena of high-frequency resonance driven by lower-frequency signals can contribute to this power spectrum shaping[8]. This spectral composition suggests that the best device for LFP measurement should have not a flat, but rather a flicker noise floor in order to optimise SNR to equal conditions of total noise. However, it is discussed whether this $1/f^h$ characteristic is interesting to capture or not, as it must be remembered that most part of neural computation takes place at pretty higher frequencies, where power spectrum strongly deviates from this. Wide-band $1/f^h$ characteristics in the end captures only statistical aspects of the neural communication [Buzsáki *et al.*, 2012].

3 A neurotransmitter.
4 A negative resistance (the ion channel) coupled with a reactive load (membrane capacitance and possibly inductance): an oscillator.
5 also called gap junctions.
6 This raises a question: this form of coupling, which could be either a form of communication or feedback, seems to suggest that extracellular "leak" currents could also not be only a byproduct of neural communication.
7 It must be noticed that this sentence must admit imperfect effect superposition, due to nonlinear effects, as it is concluded that two signals - for instance with the spectra of a square wave - contribute to create a spectrum which is not the one of summed square waves. But this is not strange, recalling among others the threshold behaviour of the neurons.
8 Although inner workings being nowadays unknown yet, this behaviour can be associated with semiconductor *flicker* noise.

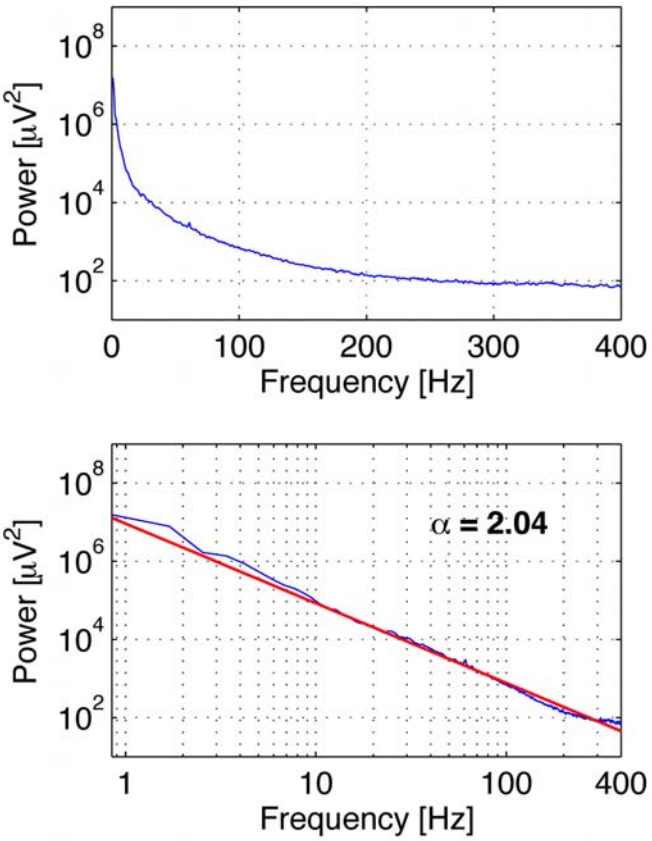

Figure 12: Power law and scaling exponent in local field potentials recorded from the human cerebral cortex. Top: Exemplary power spectrum of local field potentials recorded from a microwire in the temporal lobe. Bottom: The scaling exponent (here a=2.04) was determined by a linear least-square fit of the log-log power spectrum. [Milstein *et al.*, 2009]

2.2 EXTRACELLULAR NEURONAL SIGNAL MEASUREMENTS

The extracellular field potential V_m can be measured with different techniques, which have been developed in neurosciences history, that allow to measure signals in different points with different resolutions both in time, space and dynamics; actually they allow to observe the contributions of the different electrical phenomena at different levels. Newer methods that allow to increase the measurement options and performances are continuously being developed, and one of those is the main subject of this work. They contribute to create new perspectives for understanding the deepest neural inner workings. A smart summary of those can be found in [Buzsáki *et al.*, 2012]. A graphical panoramic of some of the cited measurement types is shown in [fig. 13].

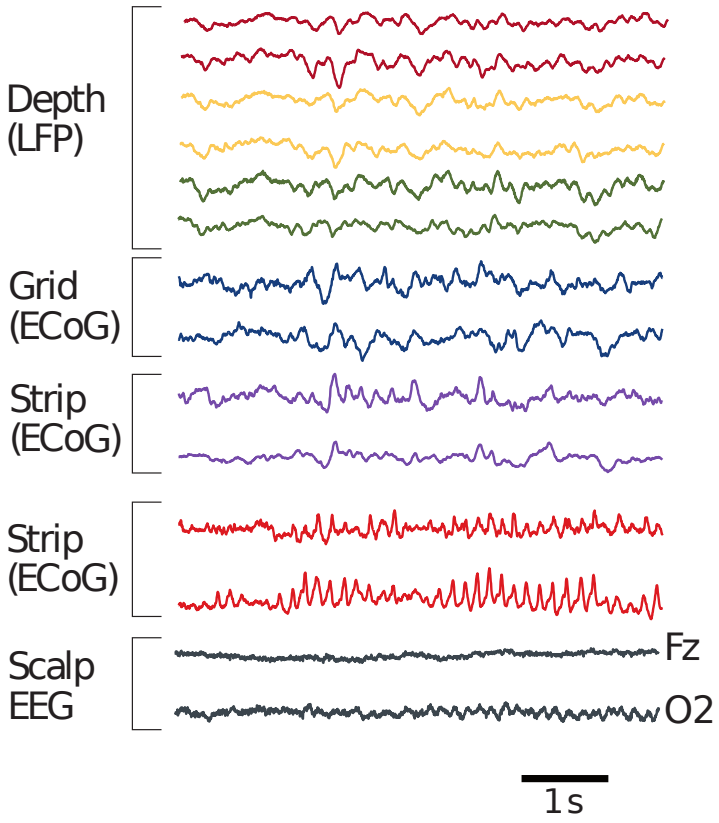

Figure 13: Simultaneous recordings from thee depth electrodes (two selected sites each) in the left amygdala and hippocampus (measuring the local field potential); a 3x8 subdural grid electrode array placed over the lateral left temporal cortex (measuring the electrocorticogram (ECoG); two four-contact strips placed under the inferior temporal surface (measuring the ECoG); an eight-contact strip placed over the left orbitofrontal surface (measuring the ECoG); and scalp electroencephalography (EEG) over both hemispheres (selected sites are the Fz and O2) in a patient with drug-resistant epilepsy. The amplitude signals are larger and the higher-frequency patterns have greater resolution at the intracerebral (LFP) and ECoG sites compared to scalp EEG. [Buzsáki *et al.*, 2012]

2.2.1 EEG

Electroencephalography (EEG) is one of the oldest and most widely used methods for the investigation of the electric activity of the brain. The scalp electroencephalogram, recorded by a single electrode, is a spatiotemporally smoothed version of the local field potential

(LFP), integrated over an area of 10 cm^2 or more. Under most conditions, it has little discernible relationship with the firing patterns of the contributing individual neurons, and this is largely due to the distorting and attenuating effects of the soft and hard tissues between the current source and the recording electrode.

2.2.2 MEG

Magnetoencephalography (MEG) uses superconducting quantum interference devices (SQUIDs) to measure tiny magnetic fields outside the skull (typically in the 10-1,000 fT range) from currents generated by the neurons. Because MEG is non-invasive and has a relatively high spatiotemporal resolution ($\approx$ 1ms and 2-3mm in principle), it has become a popular method for monitoring neuronal activity in the human brain. An advantage of MEG is that magnetic signals are much less dependent on the conductivity of the extracellular space than EEG. The scaling properties (that is, the frequency versus power relationship) of EEG and MEG often show differences, typically in the higher-frequency bands. These differences may be partly explained by the capacitive properties of the extracellular medium (such as skin and scalp muscles) that distort the EEG signal but not the MEG signal.

2.2.3 ECoG

Electrocorticography (ECoG) is becoming an increasingly popular tool for studying various cortical phenomena in clinical settings. It uses subdural platinum-iridium or stainless steel electrodes to record electric activity directly from the surface of the cerebral cortex, thereby bypassing the signal-distorting skull and intermediate tissue. The spatial resolution of the recorded electric field can be substantially improved (<5 mm^2) by using flexible, closely spaced subdural grid or strip electrodes.

2.2.4 LFP

EEG, MEG and ECoG mainly sample electrical activity that occurs in the superficial layers of the cortex. Electrical events at deeper locations can be explored by inserting metal or glass electrodes, or silicon probes into the brain to record the LFP (also known as *micro-EEG*). Recording the wide-band signal (DC to 40kHz) - which contains both action potentials and other membrane potential-derived fluctuations in a small neuron volume - using a micro electrode yields the most informative signal for studiyng studying cortical electrogenesis. Many observation points, with short distances between the recording sites and with minimal impact on brain tissue, are needed to achieve high spatial resolution. In principle, the spiking activity of nearly all or at least a representative fraction of the neuron population in a small volume can be monitored with a sufficiently large density of recording sites. Additional clues about the intracellular dynamics can be deduced from the waveform changes of the extracellular action potentials. Progress in this field has been accelerated by the availability of micro-machined silicon-based probes with ever-increasing numbers of recording sites.

2.2.5 Single-unit recording

Single-unit recordings provide a method of measuring the electro-physiological responses of a single neuron using a microelectrode system. These microelectrodes must be fine-tipped, high-impedance conductors; they are primarily glass micro-pipettes or metal microelectrodes made of platinum or tungsten. In order to capture the contribution of a single neuron, well distinct from the nearby ones, microelectrodes or electrode arrays must be carefully placed within or close to the cell membrane, delivering an intracellular or extracellular single-unit signal. The main difference between all the aforementioned recording methods

and the single unit recording is the fact that single units are not due to the summed contributions of different firing neurons. Differently from the other traces, in a single unit recording the action potentials fired, also called then *spikes* are clearly visible superimposed to the background LFP activity and graded potential, which is temporally correlated with the spikes, as in [fig. 14]. Such signals represent then the single communication between one neuron and another, and can be spike-sorted[9] in order to convert them into purely digital signals to record and represent the population of neurons communicating. Atechnique called *spike sorting* is used to attribute each recorded spike to a precise neuron. Base on the hypothesis that each neuron has a precise firing shape and pattern, the spikes recorded from one site can be clustered and each spike attributed to a neuron with a probability. This digitised information, more than for model evaluations, analysis and speculations, can also be used to interface live and artificial neural sistems with the minimum communication overhead[10] like it is being done within the RAMP European neuroscience project, managed at University of Padova.

It is widely accepted to refer as LFP to the lower frequency band ($\leqslant$ 500Hz) of an extracellular measured signal, because the source non-locality is really proven in this band. Frequencies $\geqslant$ 500Hz are instead caused by local sources and single neuron firings fall in this band.

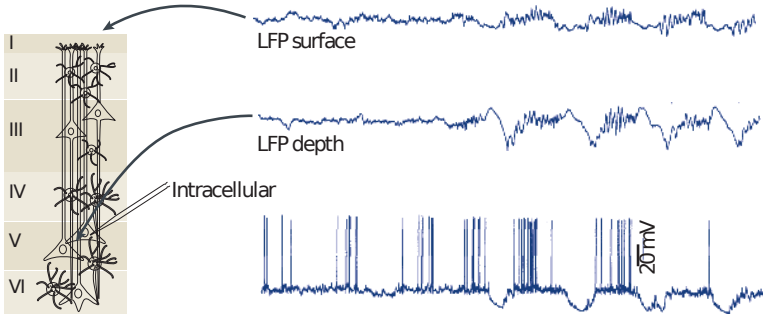

Figure 14: Simultaneously recorded LFP traces from the superficial and deep layers of the motor cortex in an anesthetized cat and an intracellular trace from a layer 5 pyramidal neuron. Note the alternation of hyperpolarization and depolarization (slow oscillation) of the layer 5 neuron and the corresponding changes in the LFP. The positive waves in the deep layer (close to the recorded neuron) are also known as delta waves. iEEG, intracranial EEG. [Buzsáki *et al.*, 2012]

2.3 ORIGIN AND FORMALIZATION OF THE FIELD POTENTIAL

The depicted scenario is a storm of *transmembrane currents* I_n injected in a conductive medium, which is the extracellular fluid, at the point $\mathbf{r_n}$. This storm of *volume current sources* can be described, in general, as a *current density* $\mathbf{j}(\mathbf{r})$[11]. As a result of the large number of contributions, an extracellular potential V_m arises, and is referenced here also as $\phi(\mathbf{r})$.

9 Spikes are detected out from noise, nearby activity and graded potentials and are given a temporal marking.
10 In fact voltage level and pulse shape information is discarded and only timing is stored/transmitted.
11 Of course free charge must always be constant inside the system (no generation of ions is allowed), so integral of current density over membrane surface must always be zero, not identically in any instant, but over a reasonable timeframe.

2.3.1 Preliminary assumptions

Many assumption are necessary to simplify the mathematical description of the phenomenon and are also widely accepted as reasonable approximations. These assumptions are typical in electrostatics, with the difference that often in that case a lossless[12] medium is considered. As discussed, extracellular medium exhibits very low resistance. Moreover, it occupies less than one-fifth of the total volume, in a tightly-packed group of cells. This means that very small potential difference is expected between different points on the medium [Brette and Destexhe, 2012].

QUASI-STATIC APPROXIMATION For frequencies up to a few thousands of Hertz [Hamalainen *et al.*, 1993], it can be assumed that partial derivatives of fields inside Maxwell's equations give non major contribution, so that electric and magnetic field are actually decoupled. This happens when the coupling between the fields is a lot lower than conductivity, or in formula $\omega\epsilon/\sigma \ll 1$[13].

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \approx 0 \tag{3}$$

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{j} + \mu_0 \epsilon_0 \frac{\partial \mathbf{E}}{\partial t} \approx \mu_0 \mathbf{j} \tag{4}$$

This means that no vector potentials need to be defined and electric field is simply the gradient of the scalar potential:

$$\mathbf{E} = -\nabla \phi \tag{5}$$

LINEAR MEDIUM Relation between field and current density is linear over the amplitudes considered. This means that nonlinear phenomena, such as velocity saturation, are not expected.

$$\mathbf{j} = \sigma \mathbf{E} \tag{6}$$

OHMIC MEDIUM Conductivity σ is expected to be a real-valued constant over frequency. This implies that no capacitive effects are generally measured in propagation of local field potential [Logothetis *et al.*, 2007] and for considered bandwidth spectral variation is negligible[14] [Logothetis *et al.*, 2007]. The validity of this last assumption is however still argued [Gabriel *et al.*, 1996].

ISOTROPIC MEDIUM Conductivity σ is expected to be a scalar value and not a tensor. I.e. it is equal in all directions. Actually, conductance components along the three axes have been found to be comparable, however a certain amount of anisotropy was found [Nicholson and Freeman, 1975].

HOMOGENEOUS MEDIUM Conductivity σ is expected to be position independent. This condition is of course the most easily violated at interfaces between different types of matter. However, it holds across lower-scale domains even with slightly different electrolyte concentrations, like in the case of zones differently involved by ion influx or efflux.

These assumption can be partly violated and a closed-form solution still be found. For instance, frequency dependance can be easily circumvented with Fourier analysis; anisotropic conductance can be accounted by modifying the distance norm [Nicholson and Freeman,

12 I.e. with null conductivity.
13 Which is the exact contrary of the lossless medium approximation.
14 This must not be confused with the filtering properties of dendrites or the ones of current sink channels, which actually build a frequency-dependent signal source.

1975] and different piecewise constant conductivity can be solved with *method of images* [Gold *et al.*, 2006].

2.3.2 Current point sources

Much confusion in present in literature upon the electrostatics and electrodynamics origin of current in a conductive medium. Generally, current conservation laws and conduction laws are not properly matched with physical quantities. However, probably [Miyakawa and Aonishi, 2012] gives the best insight, of which the author gives a sketch.

With the aforementioned premises, the conduction equation constrain the system in the domain:

$$\mathbf{j} = \sigma\mathbf{E} + \mathbf{j}_\partial \tag{7}$$

where $\mathbf{j}_\partial$ is the impressed transmembrane current by the neuron and $\mathbf{j}$ is the total current in the medium. In general, as we foresee that $\mathbf{j}_\partial$ will cause sources and sinks of free (ionic) charge, charge conservation law states:

$$\nabla \cdot \mathbf{j}_\partial = \frac{\partial \rho}{\partial t} \;\rightarrow\; \rho \neq 0 \tag{8}$$

so that $\nabla^2\phi = -\rho/\epsilon_0 \neq 0$ differently from classical field electrodynamics. The conventional boundary condition is $\phi(\mathbf{r} \to \infty) = 0$. With a little of manipulation, applying (6) to (7), we get to the more interesting Laplace equation[15]:

$$\nabla\phi = \frac{\mathbf{j} - \mathbf{j}_\partial}{\sigma} \tag{9}$$

and finally, remembering that charge conservation states $\nabla\mathbf{j} = 0$:

$$\nabla^2\phi = \frac{\nabla(\mathbf{j} - \mathbf{j}_\partial)}{\sigma} = \frac{\nabla\mathbf{j}_\partial}{\sigma} \tag{10}$$

It must be noticed that current contributions other than conduction current, such as displacement current, are not taken into account. This is done for simplicity and for the hypothesis that capacitive behaviour of medium is neglectable. However, a complex-domain description of the phenomenon is available [Miyakawa and Aonishi, 2012].

Anticipating dissertations that will follow, a discrete[16] solution of that is shown in (11).

$$\phi(\mathbf{r}) = \frac{1}{4\pi\sigma}\frac{I_0}{|\mathbf{r} - \mathbf{r_0}|} \tag{11}$$

which becomes 12 when multiple current sources are considered:

$$\phi(\mathbf{r}) = \frac{1}{4\pi\sigma}\sum_{n=1}^{N}\frac{I_n}{|\mathbf{r} - \mathbf{r_n}|} \tag{12}$$

Due to the already stated necessity for the sum of all currents to be null, a current monopole cannot exist. The simplest form of current source is a *dipole*, in which current is positive at a point and opposite at the other end. The former is called a *source* and the latter is called a *sink*. However, a neuron is in general modelled a multiple-source and single sink device, in which multiple sources are located at the axon, representing the discrete number of current outputting channels at the Ranvier nodes, and the single sink is condensed at the soma, where compensating ionic pumps and passive channels are present. This structure is shown in [fig. 15]. It is common to say that such a model is split into N *compartments*.

15 Which is very similar to the aforementioned Poisson's equation $\nabla^2\phi = -\rho/\epsilon_0$ but obtained with different hypotheses.

16 I.e. where a single point current value is considered.

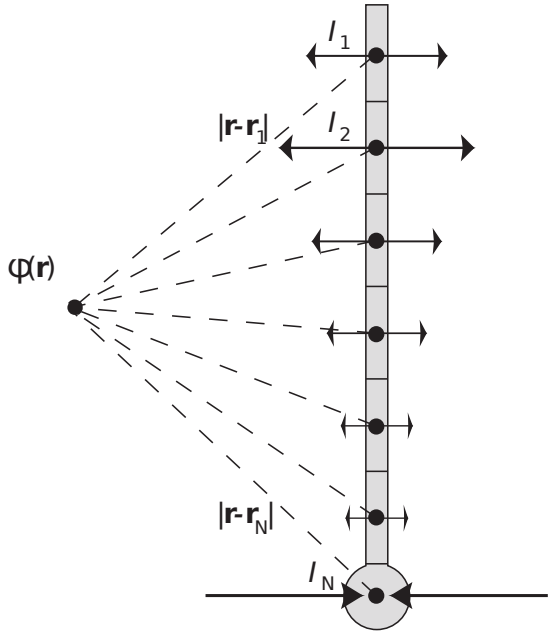

Figure 15: Illustration of the discrete model building up the extracellular potential from transmembrane currents in a single neuron. The size and direction of the arrows illustrate the amplitudes and directions of the transmembrane currents. [Brette and Destexhe, 2012]

2.3.3 Current source density

Shifting to a space-continuous domain for current sources, a new quantity related to current must be defined. *Current source density* (CSD) is defined as $C(\mathbf{r})$ and is the volume density of current entering or leaving the extracellular medium at position $\mathbf{r}$. Although being of no direct physical meaning, this is a useful quantity to describe the neural activity influencing extracellular medium. It allows to quantify the effects of a signal source without actually modelling the source in the domain with boundary (membrane) surfaces and current densities. The definition of $C(\mathbf{r})$ is actually given by naming the second right-hand side of (10):

$$C(\mathbf{r}) \equiv -\nabla \cdot \mathbf{j}_\partial(\mathbf{r}) \tag{13}$$

$C(\mathbf{r})$ has the same sign properties of point source current, and defines either a source or a sink in a given, finite, volume. This allows to write the Laplace equation (10) in a more compact form:

$$\sigma \nabla^2 \phi(\mathbf{r}) = -C(\mathbf{r}) \tag{14}$$

and thus a solution, a version of (12) is given:

$$\phi(\mathbf{r}) = \frac{1}{4\pi\sigma} \iiint_V \frac{C(\mathbf{r})}{|\mathbf{r} - \mathbf{r_0}|} dV \tag{15}$$

Equation (14) is probably more important than his solution: it states that by probing the ϕ field with space resolution it is possible to retrieve the CSD in a closed form, which gives information on the events happening at membrane and then opens a window on the intracellular phenomena and physical quantities that are, as will be explained afterwards, fairly more difficult to measure.

2.3.4 LFP of a single neuron

It is worth to generate a couple of test cases with which the result of a neuron firing is simulated and displayed. The results are cited from [Brette and Destexhe, 2012]. The first case is a pyramidal neuron from cat visual cortex, and the second is a simplified two-compartment model. In both cases, passive membrane signal propagation is considered prior to signal propagation in extracellular medium. The initial post-synaptic current stimulus is modelled ad an α-function:

$$I_s(t) = I_0 \frac{t}{\tau_s} e^{1-\frac{t}{\tau_s}} 1(t) \tag{16}$$

The resulting scenarios are shown in [fig. 16]. We can immediately notice that potential magnitude depends in position in both cases, and in particular in the neuron model current sources are far distributed, differently from current sink, which is unique and gives rise to the most negative potential signal. Neuron model simulation exhibits position-dependent filtering, because the intracellular current that propagates through the axon is passively filtered by the axon itself and then released into the extracellular fluid. as a result, extracellular potential far from soma is not only a scaled version of the somatic membrane potential. This gives a multi-point current radiator with a different, filtered source array. Even biphasic potentials can be seen as a result of this behaviour. Instead, two compartment model cannot exhibit position-dependent filtering because sink current is forced to be identically opposite to source current. This is a perfect current dipole source. At least three compartments are necessary to have a degree of freedom in the Kirchoff's current law. Non local low-pass filtering of synaptic stimulus in however still present [Brette and Destexhe, 2012].

2.3.5 The inverse LFP problem

Intracellular potentials, as discussed, carry the real information and their modelling is relatively simple. They would be the most direct and interesting measurements, however, unfortunately, it is very hard to measure them in large scale (basically because it would be necessary to position and fit an electrode inside each cell). Extracellular potential are instead fairly easy to measure but hard to model [Brette and Destexhe, 2012] and they imply a loss of information, as the measured signal has already been processed[17]. Observation of extracellular potential, together with accurate modelling of its causes, it the major way toward the understanding of neural networking.

LFP signal can actually be generated by a variety of sources, averaged together. Different mechanism can actually cause pretty similar contributions to LFP. When a large signal made up by the sum of different, smaller, signals, is measured, the contributions can be given either by propagation from distant sources through the extracellular fluid, or by networking mechanism that cause correlated firing on nearby neurons. When tissue structure is complex, and conductance is actually anisotropic due to tissue mechanical disposition[18], this ambiguity is worsened. Also neuronal geometry and architecture contributes to form many types of dipoles and field configuration, as is shown in [fig, 18]. Long, thick dendrites cause open, widely spread fields, instead round neurons cause more confined, local fields. Regular, aligned neuronal architectures, like in the cortex, are ideal for field superposition and so for the arise of a reinforced signal, instead casual structure are not subject to this effect, or again shifted-pattern structures are affected by signal subtraction. Due to dendrite organisation, finally, in cortex gyri CSD is higher in the concave side than in the convex side

17 For example, the extracellular measurement of the result of simultaneous inhibitory and excitatory synaptic inputs is often made only by noise, with no trace of what actually happened [Spira and Hai, 2013].

18 such as the *gyri* in the brain cortex

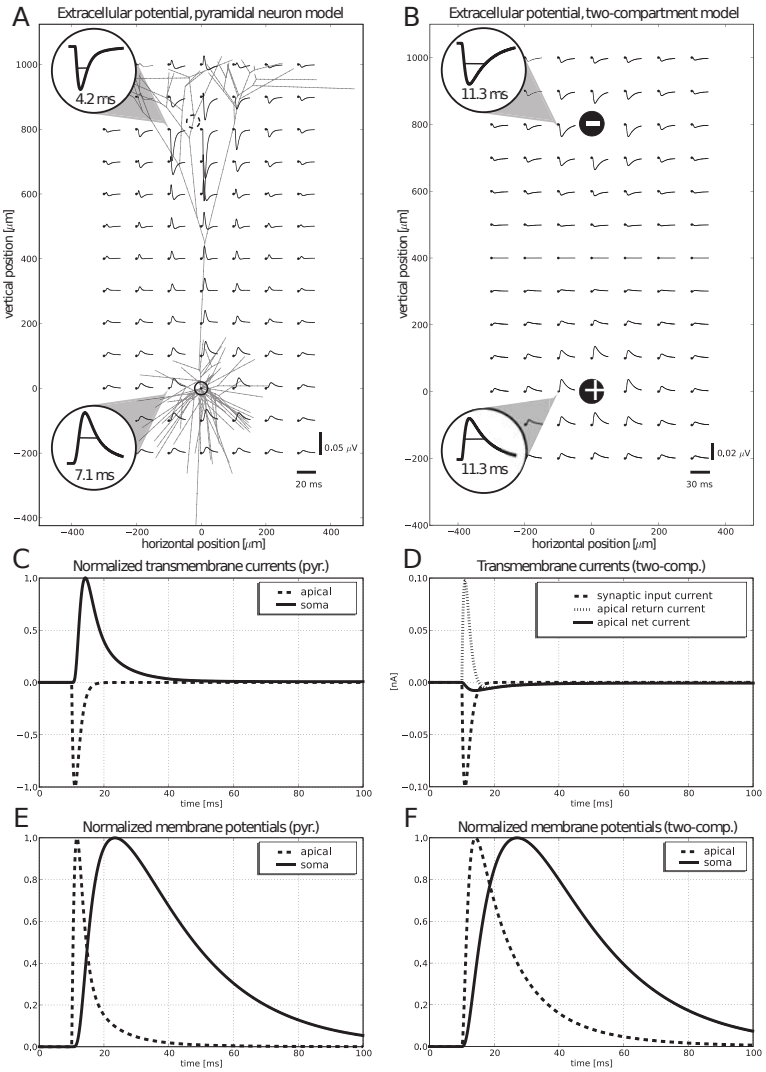

Figure 16: Calculated extracellular potentials following an excitatory synaptic input into purely passive nauron models. The sin apse is current-based and stimulated according to (16). (A) Results for passive L5 pyramidal neuron model. (B) Results for analogous two-compartment neuron model. (C-D) Normalized transmembrane currents. (E-F) Normalized membrane potentials. [Brette and Destexhe, 2012]

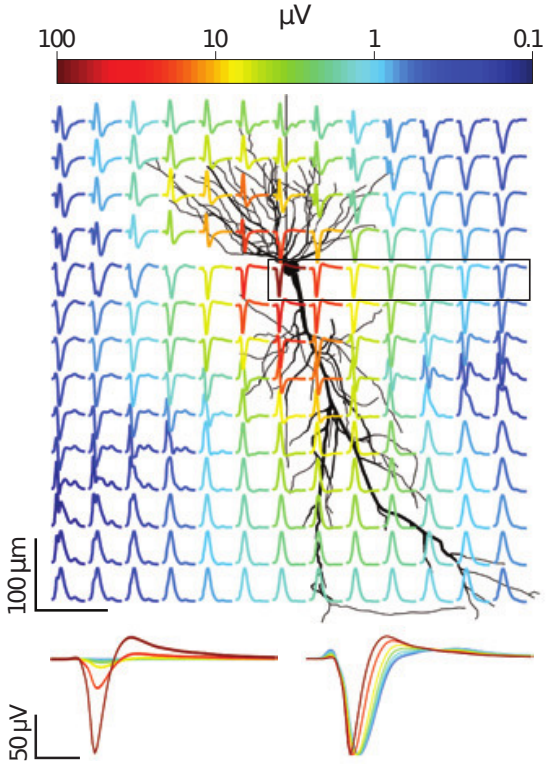

Figure 17: Measured extracellular potentials from a 182-site matrix. [Buzsáki *et al.*, 2012]

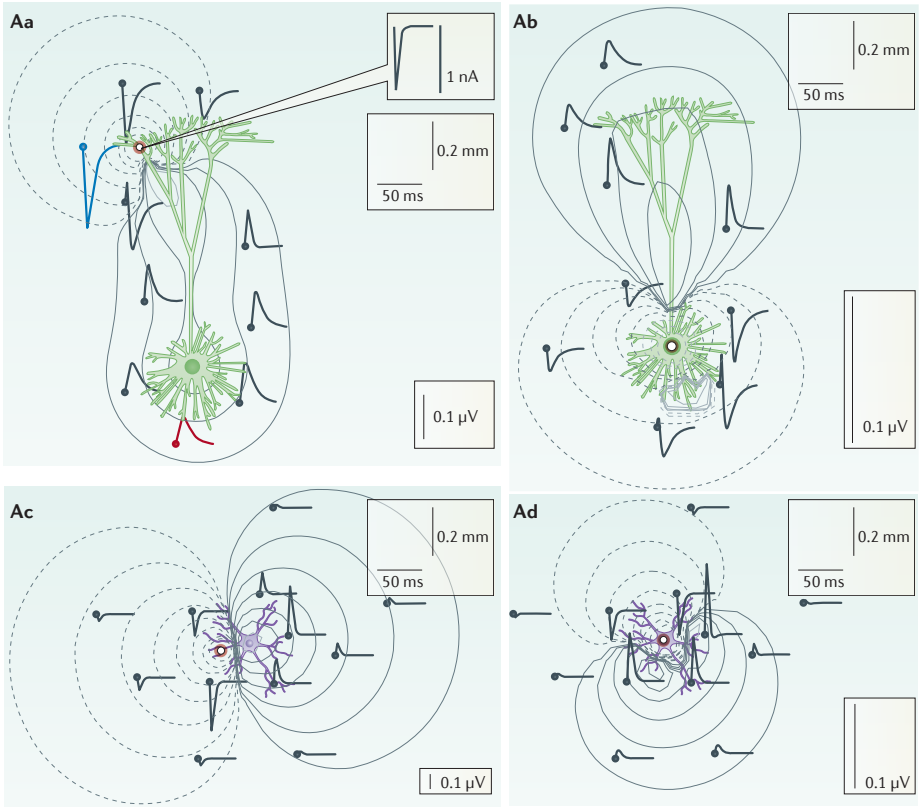

Figure 18: Different neuron models cause very different LFP space distribution. [Einevoll *et al.*, 2013]

of the fold.

The problem of reconstructing the sources of LFP signal is called the *inverse problem*. The common way to deal with this problem is to solve the *forward problem* first, that is modelling all the microscopic events, and identify synaptic and non.synaptic ones, and combining them to obtain different macroscopic results, which are LFP patterns, in different configurations and initial stimuli.

CSD ANALYSIS CSD is an old but very powerful - yet incomplete - analysis tool for LFP. As discussed by observing equation (**??**), it is possible, by having a space-resoluted measurement of ϕ, to spot current sinks and sources by looking to the value of divergence. An example on how the results of a 2D-CSD analysis can be represented to spot sources and sinks is shown in [fig. 19]. CSD analysis exploits equation (14), in a space-discretized N-dimensional form, depending on the available data.

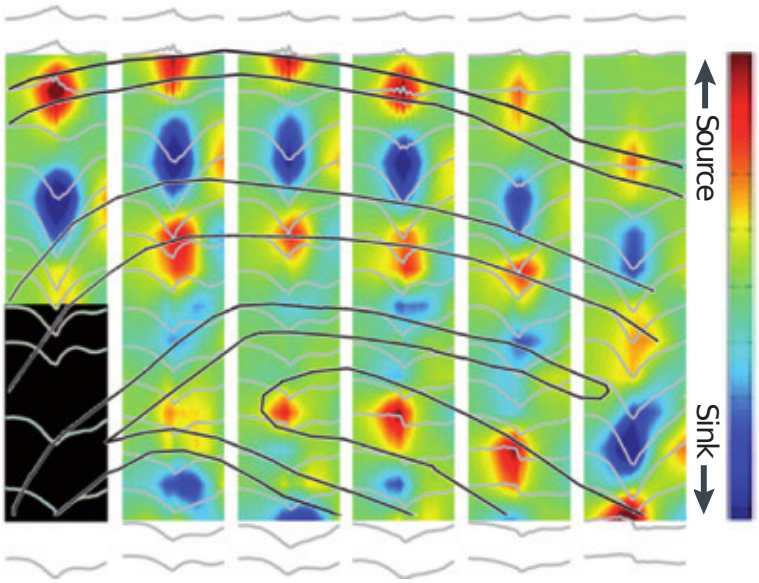

Figure 19: CSD map from a 96-site recording in a behaving rat. Sources and sink can be spotted by strong colours on the map. [Buzsáki *et al.*, 2012]

Unfortunately, CSD on its own is not sufficient to infer definitive information on current origin. For example, it is impossible to distinguish some return currents from synaptic inhibitory currents [Buzsáki *et al.*, 2012] or, sometimes, to detect if a source is synaptic or not. Some other information can be added to the investigation, to provide a complete scenario, such as:

- intracellular recording from key neurons;
- stimulation of the anatomical input sources of the circuit (e.g. rat whiskers);
- extracellular recordings from specific cells;
- knowledge of neuron structure and organisation;
- correlation between LFP and spiking activity, that allows to identify if LFP is caused by near sources (as discussed, it is known that propagation range of spikes is a lot lower than LFP);

- LFP averaging (that will be widely discussed later) that allows to reject statistically irrelevant events, and enhance repetitive, correlated events more likely to be due to networking activity.

LFP measurement is sometimes made with 1D electrode arrays. CSD analysis from 1D potential data can be done only if strong assumption of small lateral variation is made [Buzsáki *et al.*, 2012]. This is rarely verified when structures are not uniform along an axis or when layers are bent, so basically always in cortex, which is a widely investigated region. In this case, 2D data from a matrix array of recording sites[19] is mandatory in order to make a reliable CSD estimation.

ICSD ANALYSIS iCSD or *inverse CSD* is a relatively novel approach to CSD analysis which allows to overcome the transverse invariance assumption limitation and to provide a higher-resolution information. This is allowed at the price of knowing a bit more about the underlying phenomenon: basic, discrete models of the expected sources must be known, they are then interpolated and a solution to CSD equation is looked for.
Other techniques, developed in the last 5 years, such as *spike CSD* (sCSD) and *kernel CSD* (kCSD) in a similar way provide different kinds of flexibility.

CSD, including its variants, is not only a very useful analysis framework, but also a powerful data representation and visualisation tool that can be set to run even in real-time.

2.3.6 Importance of large-scale recording

It is probably now clear how much large-scale recording of neural activity is fundamental to neuroscience. As it's been discussed, large-scale recording with probe arrays can be used to record either LFP signals or single unit firing, or even both. If one of the electrodes falls within 20µm from a nerve cell membrane, it will record single unit firing with a high gain over LFP, so it will be distinguishable. Being unreasonable to record single units from each neuron in a volume, LFP is our only window over large population of neurons. On the other hand, in order to understand how information is coded and processing is carried on in a microscopic scale[20] single unit recording is fundamental. Moreover, higher and higher spatial resolution improvement will lead us to an important breakthrough: understanding single neuron processing dynamics [Buzsáki, 2004]. In fact, there is actually no mean to measure input signals of a designated neuron or neuron group, but only its axon propagating signal which is the output. A possible way is to monitor all the single unit spike patterns of presynaptic neurons, but this approach is really hard to implement due to number of sites and positioning constraints. The most promising way is to have a map of nearby neurons output signal in terms of LFP, and to understand which our neuron is receiving from. Of course, this needs high resolution and a big number of recording sites. However, first characteristic is more important than second: recording from a high number of widely spaced sites could increase tissue damage to a level that destroys local interconnections. More than this, it is known that computation is performed in small scale by local groups of neurons in a relatively small volume. So studying a small volume but with high resolution and as less tissue damage as possible is the actual top goal. Both LFP and single unit recording were conceived in quite old times. At the beginning, single unit spike variability in response to the same input were even considered background noise to be filtered out with averaged measurements in order to highlight an expected invariant response of the brain to input [Shadlen and Newsome, 1998]. This is still true for some fields of study, many of them later explained in this work, but it's somewhat restrictive: it's more wise and interesting to try to consider it as self organising pattern which, once coordinated, can be one of the origins

19 Or by means of multiple 1-D arrays next to each other, an approach which is still used.
20 For instance to study synaptic plasticity.

of cognition [Engel *et al.*, 2001]. Both techniques partially stalled in recent times, until new breakthrough technologies contributed to their revival.
LFP is now causing much more interest due to the advancements in electrode density and quantity (and the upcoming semiconductor electrodes, which have great advantages on old-styled wire N-odes), as well as computing power now available to perform analyses such as CSD, iCSD, etc. even in real-time. In general, real large scale recording is subject to a big limitation which is the number of wires coming out from the probe. Semiconductor technology is the key to overcome this big issue.
Single unit recording, thanks to new and constantly improved spike sorting techniques and data representation, is too promising important results. High resolution recording can seriously help automated and robust classification by use of strong firing correlation of synapse-connected nearby cells. Algorithms to spike sort massive quantities of neuronal signals are now available, and allow to play important analyses on network signalling as well encode them into a data stream that can even be delivered to artificial neural networks or other neuronal cultures to compose novel hybrid networks, as in the RAMP project.
In general, simultaneous recording of multiple sites is fundamental to study the processes in which an internal state is expected and thus their behaviour is not static but has a memory. When the coupling or interconnection of two neuron structure changes in time or depending on the input, for example, due to synaptic plasticity, those two region must be observed with high resolution at the same time, in order to be able to estimate the internal state and the evolution of the coupling. This approach is also fundamentals when studying coupling of independent brain-wave oscillator circuits, in which the interconnecting circuits can change over time or most likely in dependence of an input signal. Again, in this way large scale recording is the only way to study internal states of neuronal circuits which are not directly observable and need a large quantity of data to perform an estimation.
It is clear that one of the most important goals is to avoid neural circuit damage while recording. Many other techniques are available to minimise tissue mechanical damage, such as imaging tools, pharmacological manipulation, molecular biological tools, but those are always indirect observations, which must, at a certain point, be translated into a common currency [Buzsáki, 2004], that is the shape and timing of LFP or spikes, and here comes the necessity of direct recording, which, nowadays, cannot be matched by any other technology in terms of directness, investigation depth, repeatability, precision, parameter control, flexibility and speed.
Such an extensive analysis power will however need a matched power in terms of data storage and availability. Always new and more effective methods for storing recorded data and making it widely available to scientific community must be developed in order not to waste any bit of information.

2.4 SIGNAL SOURCE MODELLING

Now that the quantity - a voltage - that is to be measured has been defined, it is necessary to model electrically the signal source, with the aim to design a matched recording instrument. Due to the high-conductivity properties of the extracellular fluid, this is a simpler task than expected.

2.4.1 Signal amplitudes and bandwidths

In [fig. 20] the amplitudes and frequencies of common electrophysiological signals is shown.
Considering LFPs, amplitudes from 50µV to a few mV are expected and a bandwidth from a few Hertz to 500Hz is observed.
Considering single unit spikes, amplitudes from 10µV to 1mV are expected and a band-

width from a 500Hz to a few kHz is observed.
However, LFP signals of more than 500µV as well as single unit spikes of more than the same voltage are very rare to observe in mammalian cells. Often experiments in which a large signal is desired (for instance to observe particular artefacts oft he same) are done on invertebrate cells rather than mammalian cells. This because, in general, the bigger nerve cells of invertebrates exhibits higher neural signalling levels.

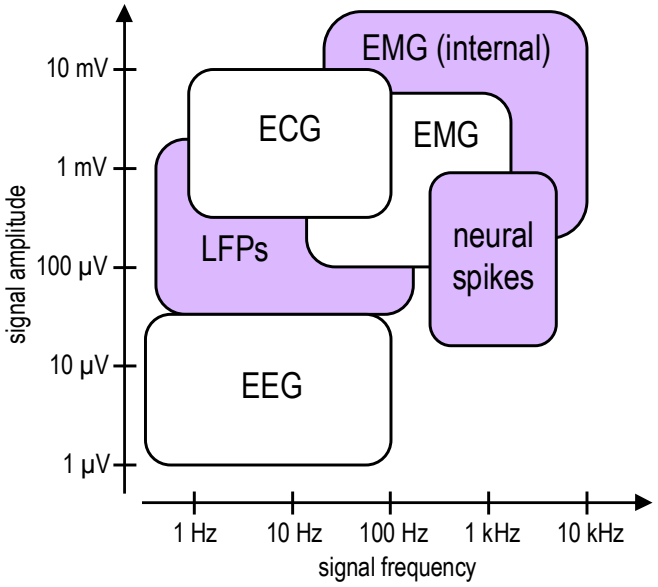

Figure 20: Approximate frequency content and amplitude distribution of common biopotentials recorded from the surface of the skin (white boxes) or internally (shaded boxes). [Harrison, 2007]

In [fig. 21] typical signals are shown: in particular a spontaneous LFP wave can be seen. It is worth to say that this is a spontaneous activity, because also recording of a stimulated activity can be made: in that case often signals have a shape that more resembles that of a spike except for the timing, and can be widely averaged over time to ached fairly better SNR.

2.4.2 Source impedance

As already seen, resistivity of extracellular fluid in brain is very low. When calculated for real-case dimensions, the resistance R_{TISSUE} associated to tissue as shown in [fig. 22] is a few kilo ohms and thus negligible with respect to sensing electrode series resistance in most practical cases.Reference electrode can be placed in any comfortable place with the only condition that it is in contact with extracellular fluid or brain humours. Its size can be arbitrary high[21] so even its reactance can be considered negligible. In general, for this kind of measurements, signal strength degradation is due much more to electrode/amplifier impedance matching than to load effects.[22]

21 With the obvious operative limitations.
22 Note that in this source definition, the electrode contact is not considered part of the source but actually part of the measurement instrumentation.

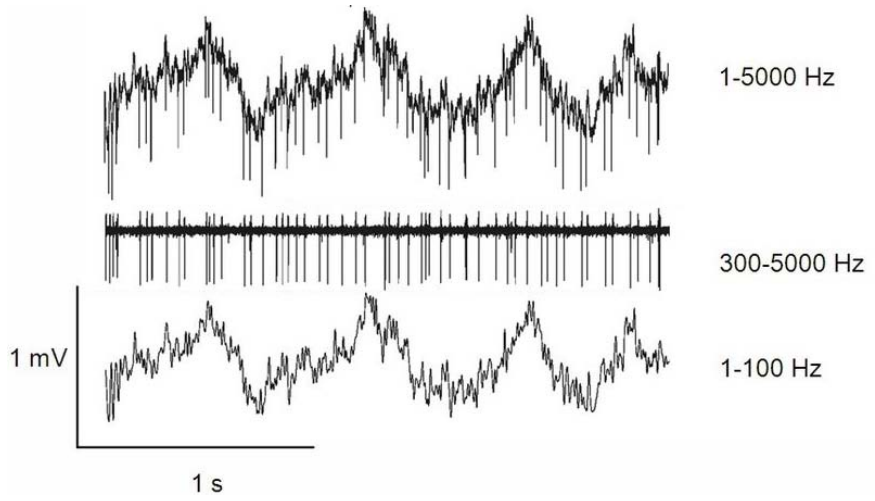

Figure 21: Typical recorded spontaneous signals in mammalian brains. Top: recorded signal. Middle: bandpass-filtered signal to show only spikes. Bottom: lowpass-filtered signal to show only LFP activity.

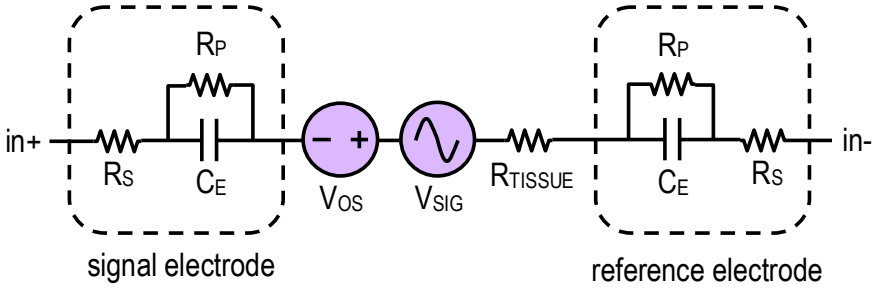

Figure 22: Approximate small-signal model of biopotential recording site with differential measurement using a signal and reference electrode. [Harrison, 2007]

3 STATE OF THE ART

In this chapter electrical recording is specifically considered. Many other kinds of mixed technologies (magnetic, optic, pressure-based) have been developed and are currently used, but are outside of the purpose of tis work. The state-of-the-art technologies for measurements, both with and without spatial resolution, or with single rather than multi-dimensional measurement point arrays, are briefly introduced, with particular focus to *in-vivo* recording. Their performances are compared in order to spot the actual needs and open issues for the next-generation measurement devices.

3.1 MICROPIPETTE RECORDING

Micropipette recording is the first effective and widely-used recording technique for electrophysiological experiments. The aforementioned scientists Hodgkin and Huxley made that fundamental discoveries with this tool.

3.1.1 Structure

A micropipette is a glass fine tip, obtained by pulling a heated glass tube[1] until the tip thins down to a few micrometers in diameter and breaks with a plain cut. A micrograph of a glass pipette is shown in [fig. 23]. Pipette is filled with a conductive electrolyte which is often a KCl buffered solution[2] like Phosphate Buffered Saline (PBS). In the opposite end of the pipette is then inserted a conductive electrode (usually an Ag/AgCl electrode) which is then connected to the instrument. The electrical connection to the measuring tissue is actually made through the electrolyte cylinder inside the pipette. Glass provides isolation down to the measurement location similarly to an insulated wire. Usually such type of electrode has a series impedance of many megaOhms, with a strong capacitive component, and obviously a capacitive coupling with the nearby though the glass tube. So it needs a high impedance amplifier, capable of compensating reactive component.

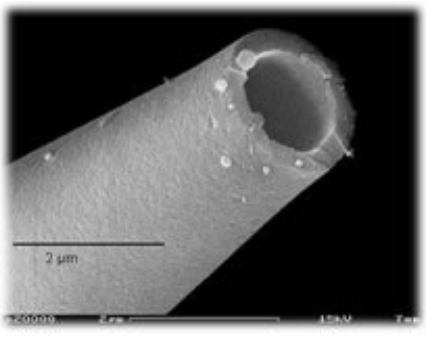

Figure 23: SEM image of a patch pipette. Scale is 2µm. [Source: Wikipedia]

1 With a tricky repeatability instrument called a *micropipette puller*.
2 A buffered solution is a solution containing different chemical species that give it the property to react to ion infusion in a way to maintain an (almost) constant pH.

3.1.2 Operation

Micropipette recording is very flexible in terms of the possible kinds of measurements that can be done with it. It is possible measure both extracellular and intracellular voltages with different techniques. The pipette electrolyte is often selected to be similar in composition and pH to the fluid it's inserted in, so that to minimise alteration of the sample.

INTRACELLULAR RECORDING In intracellular measurements, pipette is inserted through cell membrane and pipette electrolyte comes in contact with intracellular fluid. Reference electrode can be either a pipette or a metal electrode, placed away in the tissue. Different types of pipettes can procure higher or lower damage to the membrane, or higher or lower ionic exchange though the tip. The less interfering pipettes have a much thinner tip (much less than 1µm) and are called *sharp electrodes*. This method is depicted in [fig. 24] and an electrical model of the mentioned impedances is given. It is possible to record spontaneous activity just with a high impedance voltage-mode amplifier, or apply a stimulus with either:

- **voltage clamp**: fixed voltage is imposed with a current-feedback potentiostatic circuit. Varying voltage setpoint, current value at the output of a current-mode amplifier connected to the pipette is recorded and used to study behaviour of voltage-dependent channels.
- **current clamp**: no feedback control is execution in this mode, and a voltage-mode amplifier is connected to the pipette electrode. Voltage response to current stimuli is recorded. This is particularly used to study response to ambulated synaptic stimuli.

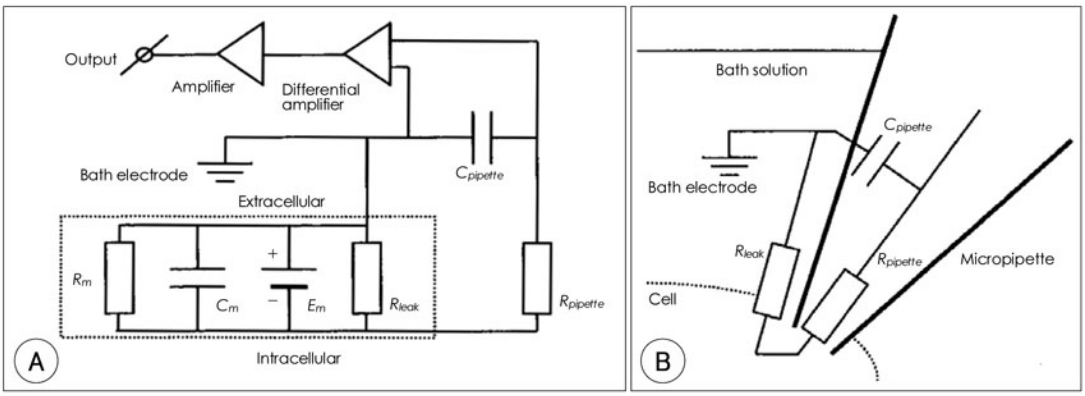

Figure 24: Equivalent circuit for an intracellular recording configuration (A) and cell-pipette system (B). [Molleman, 2003]

A much newer technique, called *pacth-clamping*, avoids the need to impale the cell membrane with ultra-fine tip electrodes. A much larger tip pipette is sticked to the cell membrane by applying a weak suction. In this way a high insulation seal[3] with surroundings is made. At this point, either the system can be used as it is to study the membrane channels or the membrane can be broken applying further suction[4] or perforated with chemical agents[5].

EXTRACELLULAR RECORDING The first method, when just a loose suction is applied to the pipette, is used to measure neuron action potential. This configuration keeps the pipette in place, for example at the firing area, but avoids to break the membrane or influence the intracellular environment in any way. The technique is shown in [fig. 25].

3 Also called *gigaohm seal*.
4 *whole cell recording*
5 *perforated patch*

Pure extracellular measurement can be done with micropipette. Actually, when positioned in an arbitrary location of extracellular space, the pipette internal electrolyte is in con act with extracellular fluid. Thus the recorded voltage will be (with the hypothesis that the pipette is compensated and negligible voltage drop occurs across is) the field potential ϕ at the tip hole location. This method is actually very used in neuroscience when the voltage at a defined depth inside a neural tissue layer needs to be measured. Particularly for *in vivo* experiments, when it is hard or impossible to actually see and position the pipette on a particular neuron group, mechanical reference points are taken and the pipette is positioned with a micromanipulator at precise co-ordinates, where measurement of the field potential, either spontaneous or stimulated, are taken.

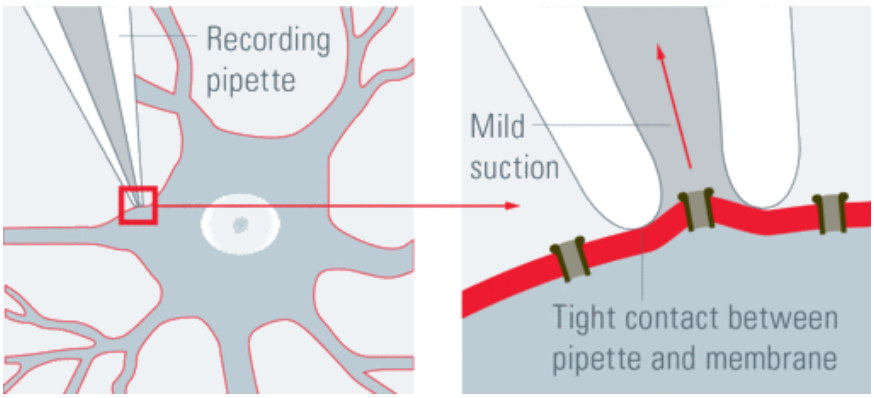

Figure 25: Weak patch clamp method for neuron action potential recording. [Source: Leica Microsystems]

3.1.3 Advantages and known limitations

Major advantage of micropipette recording is flexibility. Almost any voltage can be measured with it. Other advantages are sensitivity (input-referred noise is often less that 40μVrms) and bandwidth (up to 100kHz), depending on the amplifier and on the glass thickness which is responsible of capacitive leakage.

Obvious limitations of such a system are the impossibility of making multiple measurements at a time. It is actually possible to fit more than one pipette into a tissue, but mechanical setup limits often overcome. Mechanical damage due to the fact that section of the pipette gets very bigger after the tip can limit the possibility to reposition the pipette. Actually, multiple measurements with a pipette on a tissue are often done, when the experiment is repeatable. The pipette is moved between each run and a so-called *depth profile* is measured. However, some experiments, due to their investigation objective, could be not repeatable *a priori* or, in any case, the repositioning of the pipette could cause a non tolerable tissue damage.
Repeatability of measurement is also a problem, either because the pipette characteristics are not constant and because the tip can be damaged by mechanical insertion in the tissue. Also, preparation and verification procedure of the whole electrolyte-filled system takes time and requires a good planning of the experiment. Such a system is clearly not much optimisable in terms of readiness to use.

3.2 SINGLE AND MULTIPLE METAL ELECTRODE RECORDING

Metal electrodes are indeed the oldest kind of electrode used for electrophysiological measurements. However they are still of wide use, as that are easier to operate than micropipette and allow chronic implants. They exploit a direct metal-to electrolyte contact, and many metal electrodes have been standardised and are commercially sold. Actually, a micropipette has in it a metal electrode, which floats into the electrolyte inside glass. So, some considerations apply to them too, however many of the mechanical points are distinct.

3.2.1 Structure

In tip electrodes a metal wire is coated with insulator material like glass or polymer (e.g. Parylene), then the tip is exposed and often made very sharp thanks to mechanical or chemical erosion processes. Often the tip diameter can be made fairly smaller than micropipette electrodes. The other end of the wire has a metal contact that can can be connected to a voltage amplifier. In *pellet* electrodes, a thick piece of metal, either in the shape of a disc or a cylinder, is connected to a wire of the same material.
Many metal electrodes, made of different kinds of materials, have been standardised and are commercially sold.

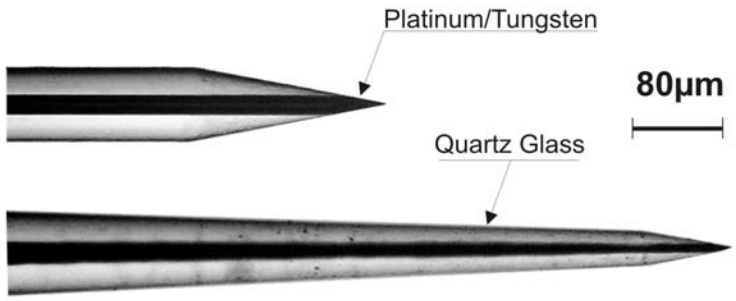

Figure 26: Metal micro electrode tips. [Source: Thomas RECORDING GmbH]

PERFECTLY POLARISABLE ELECTRODES These are electrodes in which no actual charge crosses the electrode-electrolyte interface when a current is applied. The current across the interface is a displacement current and the electrode behaves like a capacitor. An example is the Ag/AgCl electrode, in which charge is displaced into the electrolyte thanks to the redox reaction in (17) and (18).

$$Ag \leftrightarrow Ag^{+} + e^{-} \tag{17}$$

$$Ag + Cl^{-} \leftrightarrow AgCl \tag{18}$$

For example, Ag/AgCl is made by an Ag metal tip or pellet which is then covered with silver chloride thanks to an electrolytic process called *cloruration*. This gives the electrode an amount of charge, that can be lost in case DC current is forced through the electrode. However, should this happen, the electrode can be newly clorurated. These kind of electrodes are widely used for making reference electrodes (which can be arbitrarily big, so can withstand a certain amount of DC current for a long time) like the ones in [fig.27] or for making measurement electrodes.

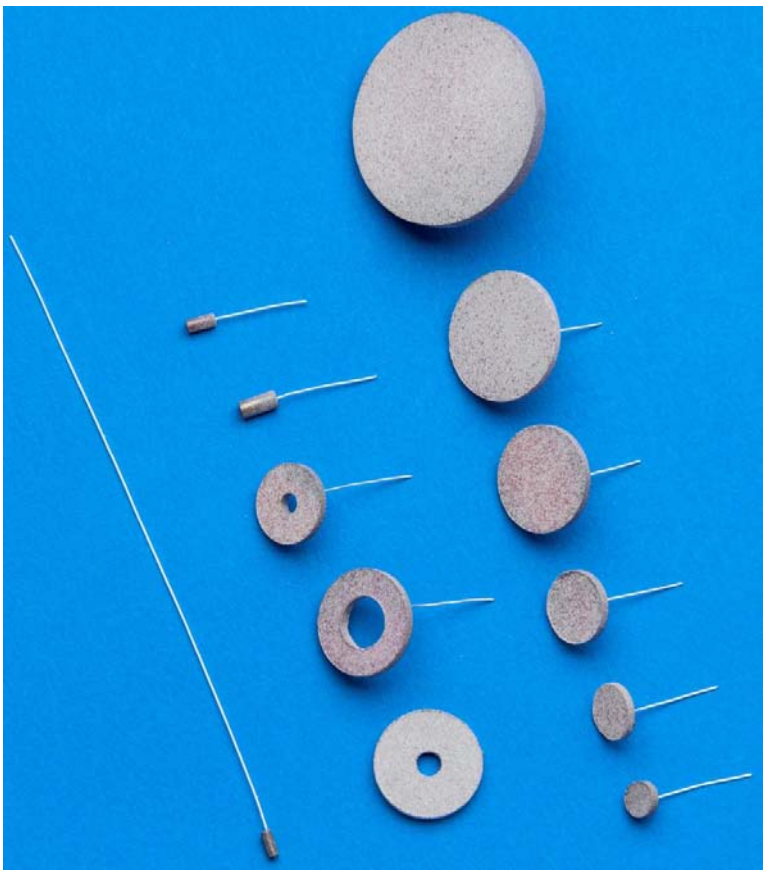

Figure 27: Ag/AgCl sintered pellet electrodes generally used as a reference electrode of for high-current electroporation. [Source: Biomed Products Inc.]

PERFECTLY NON-POLARISABLE ELECTRODES These are electrodes where current passes freely across the electrode-electrolyte interface, requiring no energy to make the transition. Thus they behave similarly to a resistance. This electrode class includes Platinum, Platinum-Iridium, stainless-steel, Tungsten and Gold electrodes. An example of those is given in [fig. 26].

3.2.2 Notes on electrode-electrolyte interface

Electrode-electrolyte interface is far more complex than an ohmic contact. Across history the model of such interface has been reviewed many times. It is worth to clarify a couple of phenomena taking place at this interface.

HALF-CELL POTENTIAL When an electrode in submersed in electrolyte, a non equilibrium condition is present, because the electrode material tends to continuously diffuse into electrolyte solution. Energy levels in the electrode metal and in the electrolyte are than different, giving rise to a potential difference, which is called *half-cell potential* of the electrode. The name half-cell is because a single electrode can be part of an electrolytic cell or a battery. If two electrodes of the same type are submerged in electrolyte, the potential difference between the two is null. Taking the *standard hydrogen electrode* (SHE) as a reference, the electrode potential is given by the Nernst equation (19) with reference to Ag/AgCl electrode.

$$E = E^0_{Ag} + \frac{RT}{nF} \log \frac{1}{a_{Cl^-}} \tag{19}$$

in which a_{Cl^-} is the activity of Cl^- ions in solution. As an example, considering a KCl solution with analogue molarity to PBS, the silver chloride electrode potential is about +288mV [Meites, 1963]. This means that when 0V are applied to the electrode, electrolyte potential is actually below ground. It is important to note that when DC current passes through electrode, ionic activity changes locally in the solution and so does the electrode potential, according to (19). However, often DC transferred charge at physiological current levels is not enough to make this effect visible. Should it be annoying, a potentiostatic control can be used to circumvent.

ELECTRICAL DOUBLE-LAYER This phenomenon was widely studied by Hermann von Helmholtz already two centuries ago [Helmholtz, 1853]. When an electronic conductor is brought in contact with a solid or liquid electrolyte, a common interface among the two phases appears. The charged electrode repel the co-ions of the charge while attracting counterions to their surfaces as shown in [fig. 28]. Two layers of opposite polarity form at the interface between electrode and electrolyte. Within a certain applied voltage, the stored charge is linearly dependent on the voltage applied, so a differential capacitance appears in series to the electrode. However, DC current is still allowed, and thus a resistance is modelled in parallel to the EDL. Different models were developed by Helmholtz, Stern, Guoy-Chapman and Grahame, which adhere with increasing reliability to the experimental results, but present increasing level of complexity.

ELECTRICAL MODEL Thus, as a consequence of the described characteristics, the electrical model of a metal electrode can be summarised in [fig. 29], where C_{dl} is the EDL capacitance, R_{ct} is the DC resistance of the interface, R_s is the series resistance of the electrode.

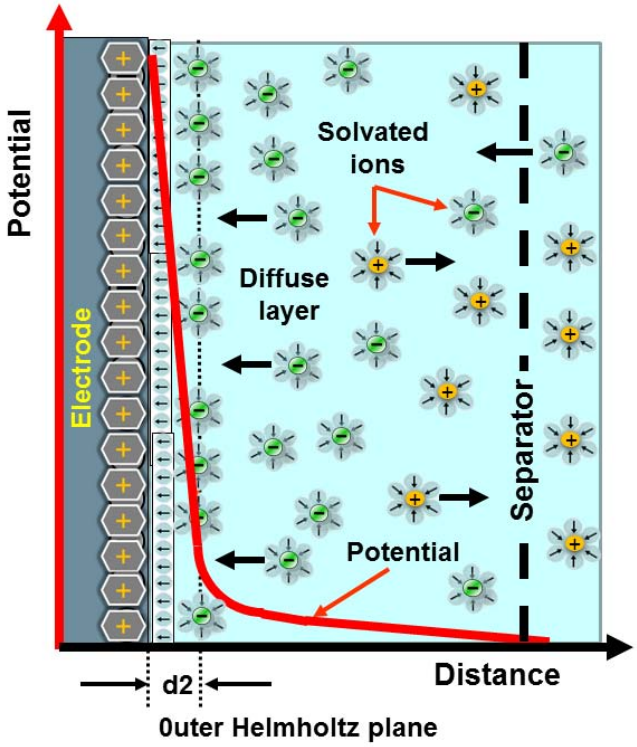

Figure 28: Simplified illustration of the potential and charge development in the electrical double layer. [Source: Wikipedia]

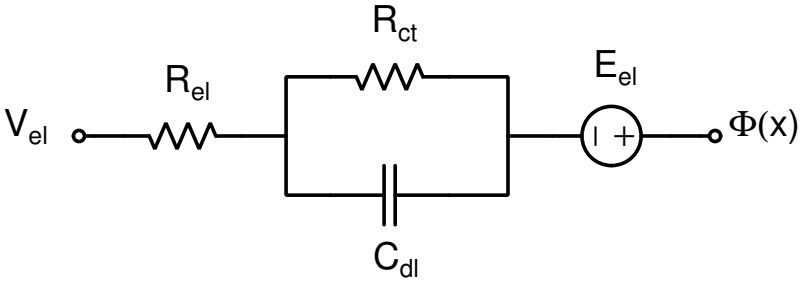

Figure 29: Metal electrode equivalent electrical model.

3.2.3 Multiple metal electrodes

Metal electrodes can have multiple wires and so multiple measurement points for signal. When properly positioned, the availability of multiple signals allows to perform a small-size CSD or, in case of spike recording a triangulation of signal source.

N-ODES These are tips where multiple measurement loins are almost equally distributed in space. *Tetrodes and peptides* are commercially available. These are made by including in a glass rod multiple conductive paths and them exposing them in different points at the electrode tip. Each path then goes with a dedicated wire to an amplifier channel. Typically the distance between adjacent recording contacts is around 50µm. Also rods with electrodes along the side are available. An example of a tetrode is given in [fig. 30].

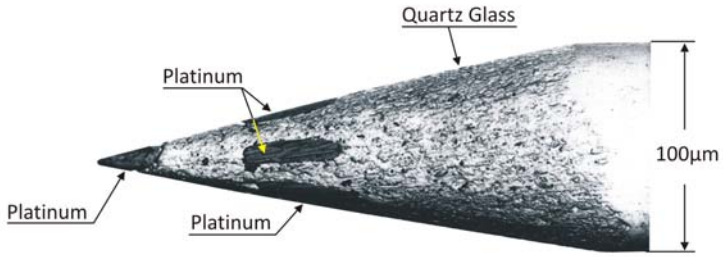

Figure 30: Tetrode electrode tip micrograph. [Source: Thomas RECORDING GmbH]

ELECTRODE ARRAYS Other type of arrays can be conceived, with a verity of substrates. All have in common the necessity to fit each line in a cable or connector in order to get to the amplifier or head stage. Often very thin and flexible rubber or, in the best implementations silicon ribbon cables are used [K. Wise *et al.*, 2004].

- flat blade electrodes (also called *needles* in this work) in which conductive traces are deposited either in glass, semiconductor, polymer or metal films[6]. The exposed tip is then obtained by etching insulator oxide layers and depositing the desired contact material, that can be Platinum, Iridium, Gold and so on. This is done for example by PECVD process. If the blade is large enough, a two-dimension recording matrix can fit in. An example is shown in [fig. 31].

- arrays of needles or N-odes similarly to the preceding case.

- 2D arrays can be mounted on a frame that allows to stack many of them, thus adding a spatial dimension to the array and obtain a 3D volume electrode, like the one by NeuroNexus™ in [fig. 32].

- arrays of single electrodes, possibly trimmed at different length, can be fixed to a 2D matrix, thus allowing a 2D recording but in a parallel plane with respect to the tissue surface. This is shown in [fig. 33].

6 Many attempts, with or without success, are known to find the best biocompatible substrate [K. Wise *et al.*, 2004]. It will be later discussed a solution which is a byproduct of active recording needles: full device coating with biocompatible dielectric layer.

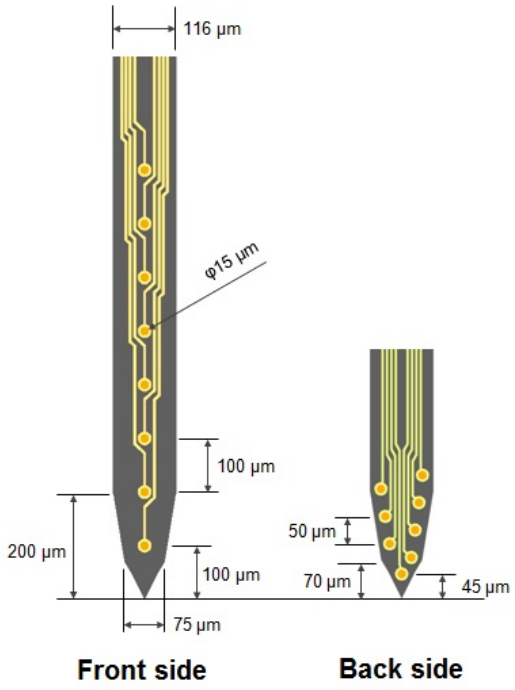

Figure 31: Flat blade electrode with multiple contact points. [Source: Tohoku MicroTec Co., Ltd.]

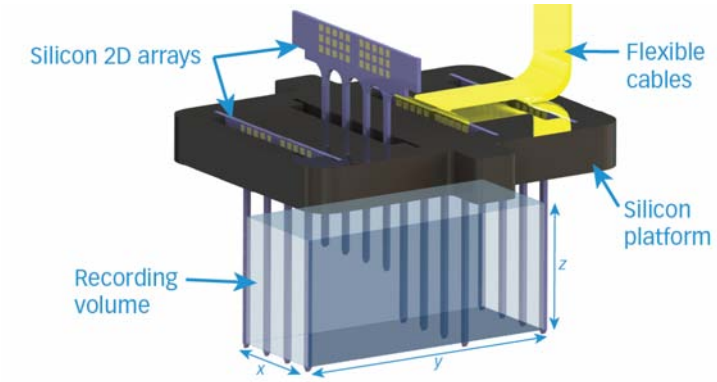

Figure 32: 2D silicon microelectrode arrays installed into a platform. Both the slot spacing and the 2D microelectrode arrays can be customized. [Source: NeuroNexus]

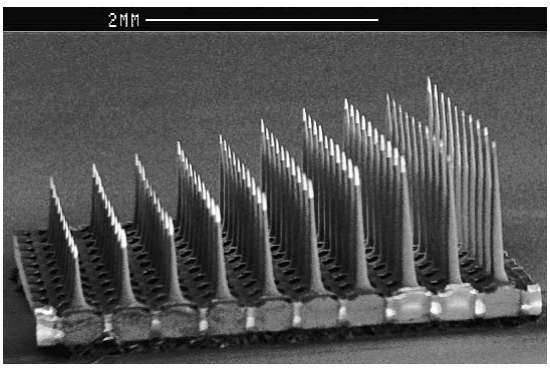

Figure 33: Single tip electrode 2d array. [Source: University of Utah]

3.2.4 Operation

Operation is similar to the micropipette in terms of positioning. In case of 2D or 3D arrays, less degrees of freedom are present and so multiple orientation angles must be accounted when positioning the electrode. A multi-channel high impedance amplifier is used to recover the signal. In case of arrays, the increased tissue damage must be considered when operating the insertion. However, mechanical stiffness is better that micropipettes and contact impedance is generally low even at low frequencies.

3.2.5 Advantages and known limitations

In general, metal electrodes are easier and more straightforward to use. Also preparation time is obviously shorter. Noise performances recently match and even overcome those of micropipettes, reaching even $2\mu Vrms$ [Baranauskas *et al.*, 2011]. However, many drawbacks are present, too. First of all, metal contact aren't properly chemically stable so they undergo oxidation and degradation of characteristics after many uses or in case of prolonged chronic application[7] [Cogan, 2008]. Also, they are often not biocompatible, so they can cause progressive death of the tissue they are inserted in or they can cause a foreign body response by the organism, or be encapsulated in a protective layer called a *glial scar*, which is a conformal layer around their tips and thus alter the contact impedance. Moreover, some metal electrodes don't have metal interconnect tracks, of the same are very thin. This makes the series impedance of the electrode high, and comparable to that of the micropipette. Of course this is not a problem, until capacitive crosstalk between cable lines doesn't come over. Finally, the necessity to bring each signal to the amplifier causes the need of a multi-conductor cable, which generally not only occupies space in the precious field-of-view of the operator, but its flexibility lowers with the number of conductors and can cause the setup to be very difficult to manage. Recently, active structures realised onboard of the base of the needle helped to reduce the number of cables by conditioning and digitising data, as well as reducing the output impedance and argin noise. A first concept of this is given in [fig. 34]. This first attempts to provide a first on-needle data conditioning, along with the advent of silicon as the needle substrate, gave the idea to use active devices directly as sensors, making thus *active semiconductor probes*.

3.3 ACTIVE SEMICONDUCTOR PROBES

An approach which tries to take the best of all its relatives is used by active semiconductor-based probes, which are introduced in this section and then will be developed all throughout this work. Differently from all other kinds of sensors, which are purely passive, those probes are designed to include active elements directly as sensors, instead of only amplification or device management. This was also helped by something that was not actually available at the earliest stage of micro electrode development: very large scale integration microcircuits. This approach opens new design opportunities, above all to include amplification directly on the sensor in-place. The idea comes from one of the basic principles of amplifier chain design: placing the first amplifier stage as close as possible to the source will minimise input-referred noise and susceptibility to external disturbances. This new approach, started no earlier that last decade, represents the new frontier of neuroelectrophysiology.

7 Actually, this depends upon electrode size: larger electrodes, due to lower current density, undergo weak or null degradation effects, differently from thinner electrodes.

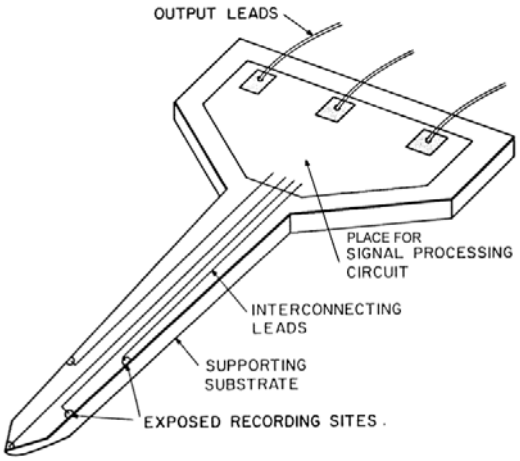

Figure 34: Original design of silicon needle with integrated electronics: the precursor of active semiconductor probes. [Source: [K. D. Wise *et al.*, 1970]]

3.3.1 EOSFET needles

EOSFET needles are based on *Electrolyte-Oxide-Semiconductor field effect transistors*. Those devices come directly from ISFETs (*Ion Sensitive field effect transistors*) which have been largely used to measure pH variation in electrochemical solution. Their structure, shown in [fig. 35] is very similar to that of a conventional MOSFET without gate insulator, but only a SiO_2 dielectric layer exposed[8].

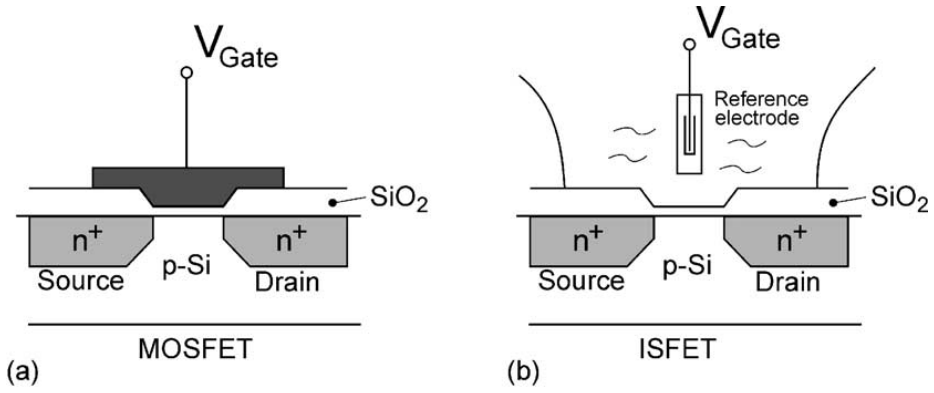

Figure 35: Schematic representation of MOSFET (a) and ISFET (b). [Source: [Bergveld, 2003]]

Electric field is generated by the potential difference between the mosfet source and body contact and the electrolyte. This is responsible for the creation of charge inversion layer and formation of the conductive channel. It is known that threshold voltage of a mosfet is given by equation (20).

$$V_t = \frac{\Phi_M - \Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_F \tag{20}$$

where oxide charge Q_{ox}, interface charge Q_{ss} and depletion charge Q_B are considered. All those terms are trimmable during fabrication process, but, unless high-energy events occur,

8 Different kind of dielectric layers were tried though, like Si_3N_4 and Al_2O_3

are quite stable over time. In the ISFET, the gate voltage is no more directly controlled but is rather the result of applying a voltage to a reference electrode in the electrolytic bath. Thus, an electrochemical term must be added to 20 leading to 21.

$$V_t = E_{ref} - \Psi + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_F \tag{21}$$

where Ψ is a Nernst-like potential depending on pH of the solution and χ^{sol} is the surface dipole potential of the solvent and thus is constant. Metal electrode work function Φ_M has not disappeared but is actually incapsulated in the electrode potential E_{ref} [Bergveld, 2003]. The Ψ parameter was found to depend from electrolyte pH value according to the sub-Nernst equation (22).

$$\Psi = 2.3\frac{kT}{q}\frac{\beta}{\beta+1}(pH_{pzc} - pH) \tag{22}$$

where β is a correction parameter and pH_{pzc} is the pH value that null the oxide surface charge. Further studies saw in (22) the contributes of surface buffer capacity and differential double-layer capacitance. This gave a sensor able to respond to pH variations very quickly.

Actually, an EOSFET is pretty identical to an ISFET, however their uses are different. During experiments with ISFETS with the presence of local field potentials inside the electrolyte, it was discovered that such devices were absolutely not immune to that, and variations in potential ϕ were recorded. Devices were already known for having a good bandwidth (0-40kHz) so, use of such devices for recording of was proposed. pH sensitive devices were typically flat chips, but the idea of designing recording needles for in-vivo in which sensitive element was an EOSFET device came up and first works on this subject were done by [Felderer and Fromherz, 2011] in which the term *transistor needle chip* (TNC) is coined.

A more deep explanation of threshold voltage on EOSFET devices is given in [Fromherz, 2012], however the practical conclusions are the same and such level of detail is out of the purpose of this work.

STRUCTURE OF TNCS In TNCs, also called C1-family needles[9] a multi-transistor array (MTA) is created by lithographic technology on a 400µm Silicon-on-Insulator (SOI) wafer. TNCs are realised on a needle tip shaped section with n-type silicon layer of 100µm thickness. Transistors active area is $10 \times 10\mu m$ and they are connected to bond pads, staying on a bigger support part, with n-doped tracks. Silicon gate oxide is grown on top of the FETs and then all the needle is processed though Atomic Layer Deposition (ALD) to grow a 13nm thick TiO_2 layer. Then, bon pad windows are etched and Al/AlSi metal contacts are deposited. Differently from needles with metal contact, during etching process particle care is taken to protect transistor structures. [Felderer and Fromherz, 2011]. Cutout of the chip is then etched and the single needle is removed and bonded on a support.

STRUCTURE OF C-100-A NEEDLES C-100-A needles[10] are an improvement of C1 family needles:

- 2D disposition of recording sites was designed.
- Recording sites count was increased: 2x8, 2x50, 4x64, 4x4, 10x10, 16x16 arrays are available.
- Different shapes and lengths were designed: TIP_L, TIP_A, SHANK, FLAT shapes are available as shown in [fig. 37]. They basically have different widths and lengths and are useful for measurements at different depths.

9 Nicely called the *Florian chips* within the framework of this project.
10 Nicely called the *Stuttgart needles* within the framework of this project.

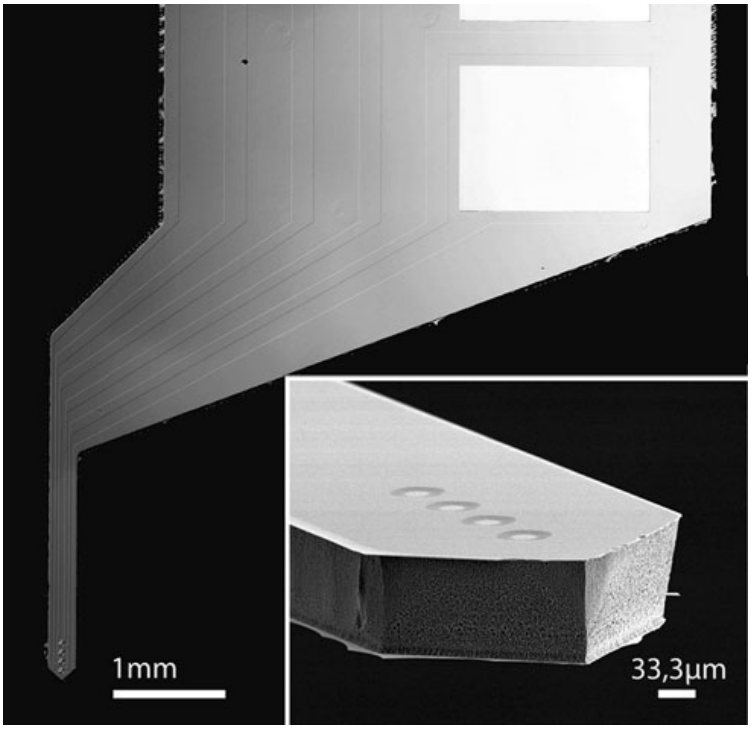

Figure 36: Electron micrograph of a transistor needle chip (TNC). The picture shows the needle with four transistors and a portion of the contact plate with one of the metalized bond pads. The thickness of the needle is 100 ?m. The vertical walls are obtained by a Bosch-like plasma process. [Source: [Felderer and Fromherz, 2011]]

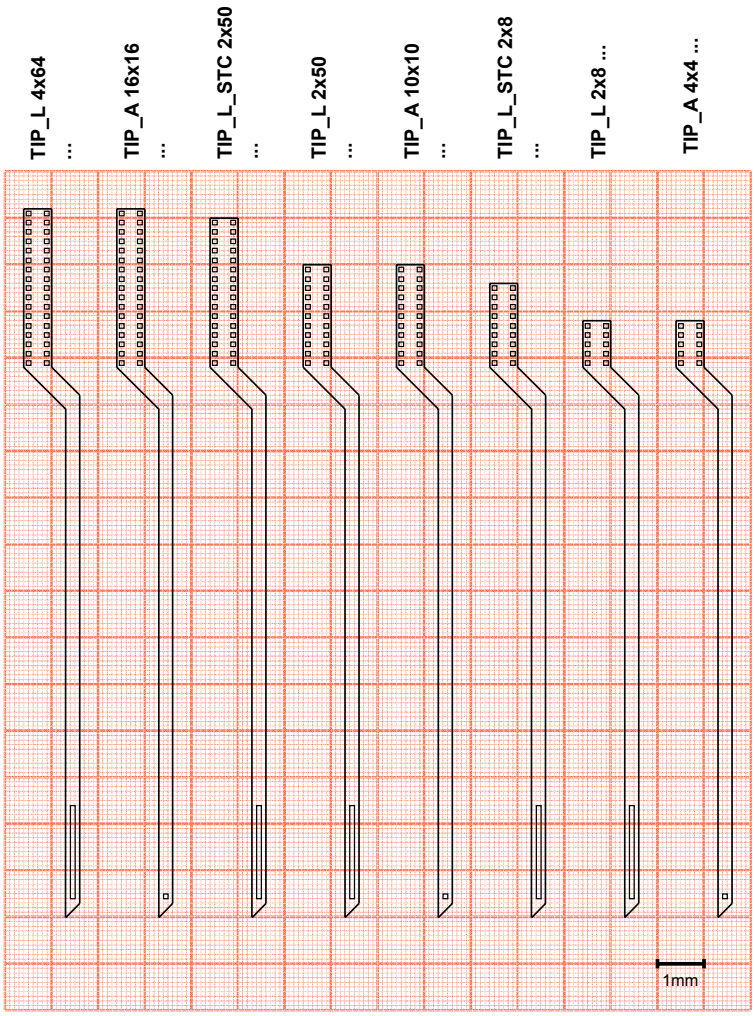

Figure 37: Some of the EOSFET needle shapes.

- Matrix addressing was implemented. As shown in [fig. 38], FETs are matrix-addressed. Each row and column line is connected to source or drains respectively of EOSFETS disposed in a square. Differently from physical disposition that can be rectangular (i.e. 2x50), device address is always as square as possible, for saving control lines. In this way, the number of lines coming out of the sensor array is dramatically reduced from 2N to $2\sqrt{N}$, where N is the number of recording sites.

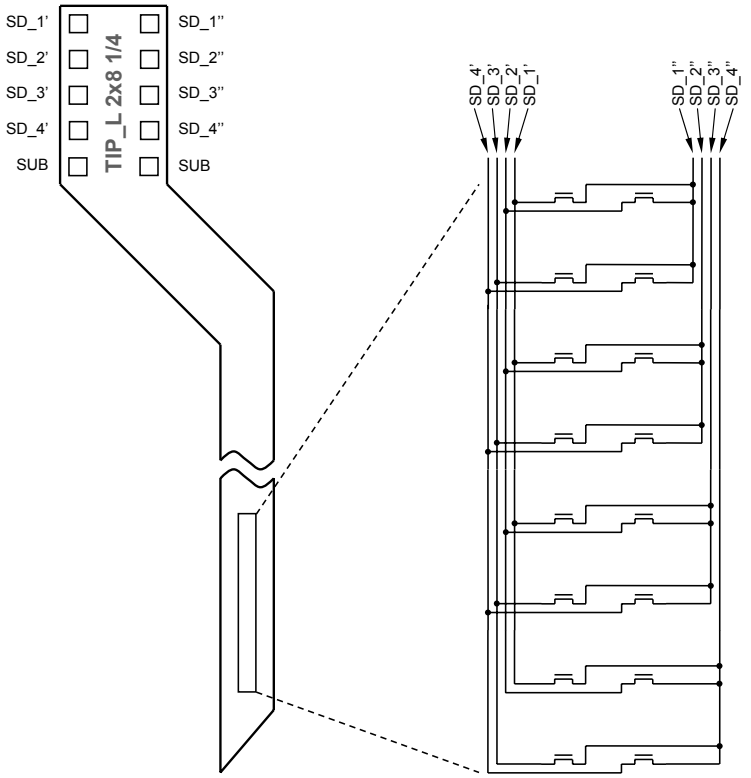

Figure 38: Address lines schematic of the EOSFET chips (a 2x8 chip is taken as an example).

- Stimulation capacitors were added. Although being out of the purpose of this work, it is worth to say that such structures, which are basically metal plates insulated from electrolyte, are useful for stimulating the tissue with a capacitive current.

C-100-A needles are obtained by lithography with a similar process to that of C1 needles, but a standard p-Silicon substrate is used instead of SOI. Doped track interconnects are still used, being the metal layer difficult and expensive to realise in a non-standard process. However, chip is now coated after etching and separation from die, and TiO_2 deposition is now done on single chips. This is more tricky, because a way to fit and dispose multiple devices in ALD machine is more difficult, and handling is very critical. However, this allows to have a more uniform conformal coverage even at the side walls. A standard PCB with wire connector for all needles is available, so that pinout is standardised. Bonding is now done by breaking thru the oxide with ultrasonic bonding machine, and pad metallisation is so under the oxide layer. This choice preserves the chip from a chip from unnecessary acid attacks which are indeed very aggressive in order to etch TiO_2 away.
A photo of the full device, bonded on the connector PCB is shown in [fig. 39].

OPERATION Despite first tests of C1 chips were conducted on in-vitro rat brain slices, devices are in general used for in-vivo recording. Through a micromanipolator, the device is

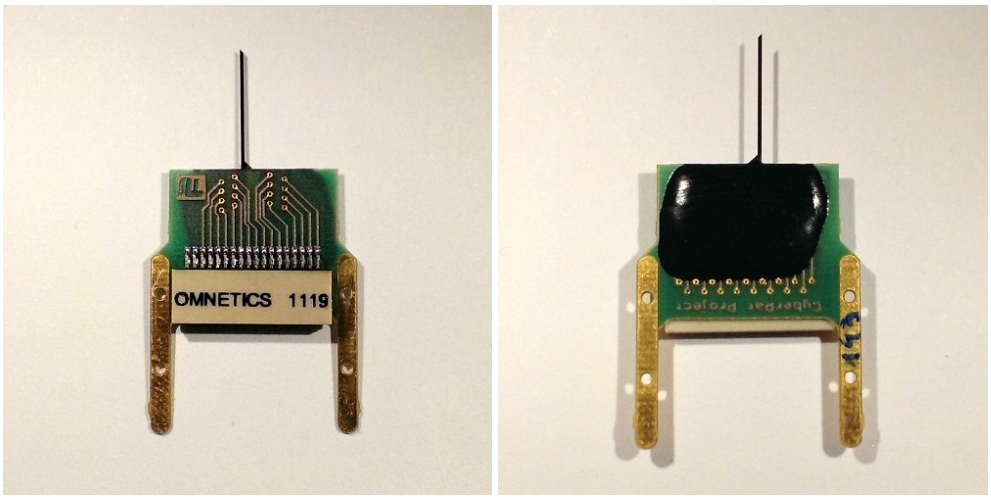

Figure 39: Photo of a C-100-A/EOSFET needle bonded to its PCB board.

inserted in the tissue in right position[11]. Matrix configuration and a sketch of the readout is shown in [fig. 40]

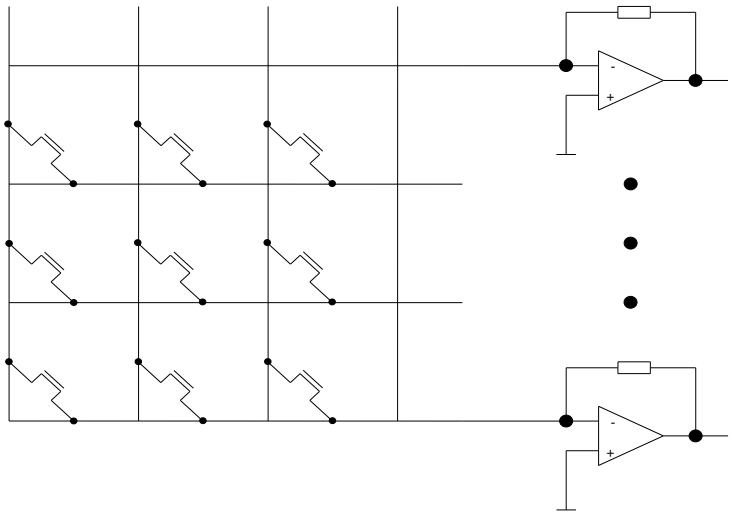

Figure 40: EOSFET matrix schematic and readout amplifier sketch.

As already shown, the gate biasing is given though the bath itself, or in case of in-vivo measurement, the extracellular fluid. A tiny electrode, usually Ag/AgCl, is positioned in contact with the fluid and voltage is applied. Two things must be taken care of:

- A half-cell potential will be present between the potential imposed at the electrode and the effective electrolyte potential. So the electrode voltage should be trimmed accordingly. Moreover, many factors influence the half cell potential, such as charge injection and pH variations. So a variability in gate biasing must be accounted. However, this has not been found to be a problem at the electrode side, despite in some experiment a potentiostatic control is used to provide more steady control.

11 It must be said that often the signal output from the measurement is used as feedback to find the correct position. In fact the micro manipulator is precise enough, but not so much is the initial reference system for positioning.

- Often the animal will be hold on the setup table with a metal stereotaxic mount. Tis means that the body of the animal will be at ground potential. So the bath potential must be not much far from ground, in order to avoid unuseful faradic currents to flow through the electrode.

Each line terminal of the matrix is then connected to a dedicated line amplifier. This is a low noise current-to-voltage amplifier which must provide DC bias point rejection and low-pass filtering. In fact, the variable now observed is the small-signal transistor drain current from which it is possible to recover the small-signal gate voltage thanks to the well-known relation (23).

$$g_m \equiv \frac{\partial i_d}{\partial v_g} \rightarrow \hat{v}_g = \frac{\hat{i}_d}{g_m} \tag{23}$$

In order for this relation to be useful, transconductance g_m at the specific operating point must be known. For this reason a calibration is performed right before the experiment: a sinusoidal bandwidth-centered carrier is injected into the bath though the reference electrode, and the resulting current wave is measured, assuming the gain of the amplifier to be known. Biasing of the transistor drain was not mentioned yet: as this is a matrix, three options are available:

- **single-colums bias**: a single row is active and $V_{ds} = V_{col} - V_{row}$[12], whereas $V_{col} = V_{row}$ is applied to other columns, so that EOSFETS are turned off. In this way, a single column is monitored in real time.

- **multiple-column bias**: like in the preceding case, but with multiple column enabled. This configuration gain a higher transconductance.

- **full scan**: a single column is active at a time, but they are scanned by a multiplexer. This way, in each time frame a single column is observed. If data is then synchronised and assigned to the correct pixel, a rasterised matrix of the measured signal can be recovered. Note that scan frequency must be many times higher than input signal bandwidth: scanning is a form of sampling, to Shannon theorem must be fulfilled.

ADVANTAGES AND KNOWN LIMITATIONS The clear advantage is the possibility to take 2D measurements without a large wiring overhead. Noise level is often not able to match that of the micropipettes and, up to now, even to most single metal electrodes, despite being object of further research as of now. But, thanks to the impedance transformation performed by the transistor, susceptibility to external interference is much lower than that of multi-metal electrodes, even thanks to the reduced amount of wires. However, tracks realised with doped diffusions are not ideally low-impedance paths, so voltage drop happens across them, generating a bias error, and the capacitive crosstalk is enhance by the light line impedance. The absence of an exposed metal contact avoids problems due to oxidation and damage, and the TiO_2 coating makes the whole needle biocompatible even for chronic implant. Next, being the process non-standard, it will hardly allow to scale down or realise on-board amplification or matrix multiplexing. Gate threshold voltage, additionally, is known to be very sensitive to pH and ion concentration at the gate, so often reaching a precise bias point and maintaining it throughout the whole duration of an experiment, when charge injection could be not negligible, is a real pain. The device could slowly increase or decrease its transconductance while being the operator unaware of that, so automatic control is necessary. Potentiostatic control, unfortunately, solves the problem only at the reference electrode side. Also, having the bath voltage related to the desired gate voltage, reduces the degrees of freedom and does no allow, for example, to have the needle substrate ad an arbitrary voltage with respect to the electrolyte (this could help, for instance, to minimise leakage currents from other sides).

12 EOSFET devices are symmetrical, to the choice of a source or drain terminal is arbitrary.

Lastly, EOSFET transistors have been found not very adherent to models from characterisation data, at the point that a two-transistor model was used to describe the behaviour of a single EOSFET. This creates many issues when trying to use many well-known structures from analog integrated circuit design.

3.3.2 CMOS needles

CMOS needles, which will be the main topic of next chapter, are made similarly to EOSFET needles, but an industrial process and CMOS transistor technology is used. This is actually the most promising technology for active recording needle realisation.

3.4 OPEN ISSUES

Here many of the issues and limitations of the different recording systems are summarised:

- **Noise and signal integrity**: electrode input-referred noise level is important, but also susceptibility to external interferences (radio signals, mains voltage, AC-powered light) so wiring paths should pick us the less possible amount of noise.
- **Large scale integration and on-board signal conditioning**: the technology used for the needle realisation should foresee the possibility to scale down recording site sizes and thus incrementing the spatial resolution. The technology should also allow to implement analog and digital circuitry on the same substrate.
- **Biasing**: needle should allow a way to define bias point as independently as possible from external factors, fist of all the electrolyte voltage, and bias point stability must be assured
- **Biocompatibility**: needle should be as much as compatible with tissues and reduce its interferences with living cells. This is a problem that is often neglected in acute implants, but investigation should be far-sighted to chronic implant systems.

Most of those limitations are the starting point for the new CMOS needle technology that tries, with many intelligent solutions, to overcome the limitation of the actual systems and solve many of the open issues, trying to fulfil the experimenter's desires and giving thus the ultimate tool for neuroscience research.

3.4.1 Leakage current damage limit

Any kind of electrode has an unwanted DC leakage resistance towards the electrolyte. This allows a so-called *faradaic* current to be dispersed into the surrounding volume. This current has many consequences such as injection of ionic charge and charge migration, causing in some cases severe tissue damage. Thus it must be limited as much as possible. A general limit not to be exceeded for leakage current density from an electrode is $5\mu A/cm^2$, which is a conservative estimate. Current in the $10\mu A/cm^2$ range have been applied without causing detectable damage, and often are necessary to impose a desired electrode DC bias [Cogan, 2008]. The voice to use p-Silicon substrates instead of SOI dramatically increases the chance of DC substrate leakage towards electrolyte, and thus this parameter must be more critically evaluated.

4 ACTIVE CMOS NEEDLES

In this chapter the design, layout, structure and fabrication process of C-100-A needles is explained. The innovative design ideas, as well as the critical aspects, will be highlighted to that to constitute the substrate for the further characterisation and evaluation process.

4.1 CHIP FAMILIES

The current chip families designed and realized within the framework of this project:

- **C-100-A/CMOS**: this is the evolution of the aforementioned C-100-A/EOSFET needles. Those are realised with minimal further processing over an industry-standard 0.18µm process[1] and 1.8V FET devices. Two variant are available in terms of top electrode: tungsten and titanium/titanium nitride; and many variants are available in terms of dielectric oxide type and thickness: TiO_2, $AlHfO_2$, HfO_2.
- **C-1000**: this further evolution includes on board amplification, signal conditioning, multiplexing and A/D conversion. However, those devices are not yes available for testing.

The C-100-A/CMOS family is subject of study in this work.

4.2 DESIGN

The innovative idea of the C-100-A/CMOS needle design consists in discarding EOSFET technology in favour of standard CMOS process. Of course standard MOSFETs are driven by a voltage at the gate rather than be sensitive to electrolyte field. The idea is to connect a metal plate at the gate, then further insulated with a dielectric, to make a capacitive interface to the electrolyte and thus sense the variations of electrolyte potential Φ. In first approximation, the DC current at MOSFET gate is null, so that is the lower cut-off frequency of the capacitive-coupled sensor. In reality, a leakage path will degrade such figure, and this issue will be one of the most important to be kept under control. The second, major advantage of this choice is that the complete DC decoupling of gate note will help to impose gate biasing voltage with almost no influence from electrolyte potential or electrochemical events happening at the surface, thus saving all the annoying issues related to EOSFET biasing. Of course this will need additional devices to provide correct gate biasing. The new design of the single cells arranged in the matrix - including biasing structures - is shown in [fig. 41].

4.2.1 MOSFET biasing

Of course biasing voltage and input signal will mix at transistor gate. This suggests that biasing the transistor with an ideal voltage generator is anything but a good idea. The input impedance seen from the signal source would be zero and no signal would be picked up. Ideally, the voltage source for bias gin should have the infinite impedance in steady state but still impose the initial bias condition. In more realistic terms, it should be either a switch that

1 Although being called CMOS, only one channel type device is present in the needle at a time.

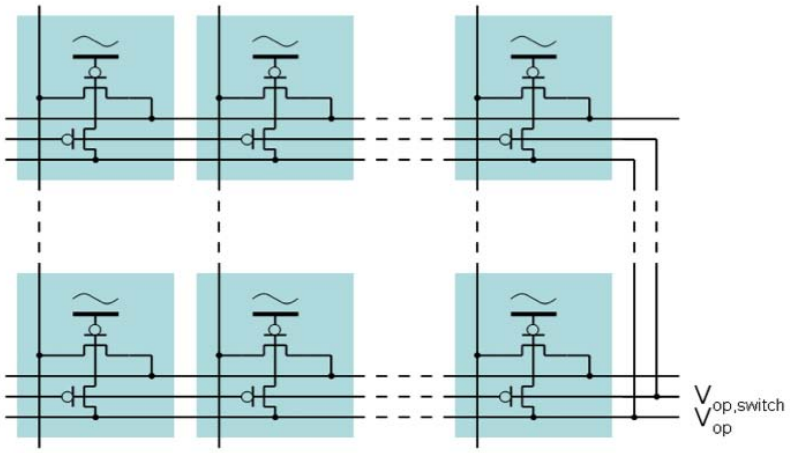

Figure 41: Matrix structure of CMOS needles. The additional control lines for biasing transistor can be seen (In this drawing, p-MOS transistors are shown.).

closes to provide correct bias at the beginning and then opens in order not to degrade input impedance of the system, or a very high output impedance voltage source (once in steady state) which drives current only when bias voltage is not still reached. Both approaches are logical and both are actually followed in literature for same or similar applications[2], but in this case the latter is implemented. A transistor M_{bias} which can be driven in subthreshold region is connected between a control line and the sensing transistor M_{sense}. In this way, a huge impedance is seen from the gate node in steady state, however during transients, when drain-source voltage of M_{bias} is higher, more current is driven into gate so settling time is shortened. This structure is identical for each pixel, and control line V_{op}, which represents the desired gate voltage of M_{sense}, as well as the gate control voltage for M_{bias}, which is named V_{ops}, are shared among all pixels. The choice to provide a control transistor to each pixel is obviously due to crosstalk considerations.

4.2.2 Addressing

Apart for the need to drive V_{op} and V_{ops} lines, the rest of device addressing pattern is identical to C-100-A/EOSFET needles, so reference to [fig. 38] can be made.

4.3 LAYOUT

Different needle shapes are available, and are almost the same of the EOSFET needles, so [fig. 37] can be taken as reference. Longer tips (TIP_XL) are designed, as well as multi-shank (FORK) needles. However, only bigger arrays are available, such as 10×10, 16×16, 2×50 and 4×64. Device size for M_{sense} is fixed to $1 \times 1\mu m$. Different matrix pitches are available. A summary of needle layout versions is shown in [tab. 1][3]. Also needles with stimulation capacitors are available.

The combined structure of M_{bias} and M_{sense} is designed to fit into a $10 \times 10\mu m$ pixel, which is then overlaid by a $8 \times 8\mu m$ top electrode, as shown in [fig. 42]. Matrix interconnects and control lines are then organised and brought away in direction of bounding pads through needle shank as shown in [fig. 43]. Needle tip is given a blade-like or a symmetrical shape,

2 An overview of parallel developments, including this aspect, will be given at the end of this chapter
3 Not every option is actually shown, but only those which are physically available and are currently employed.

Table 1: Different matrix options for C-100-A/CMOS needle chips.

Matrix count	Matrix size [µm]	Pixel pitch [µm]
10×10 (V_s)	100×100 / 150×150	10 / 15
16×16 (V_d)	160×160 / 280×280	10 / 15
2×50	60×1960	30×39.2
4×64	100×1000	25×15.625

depending on the versions.

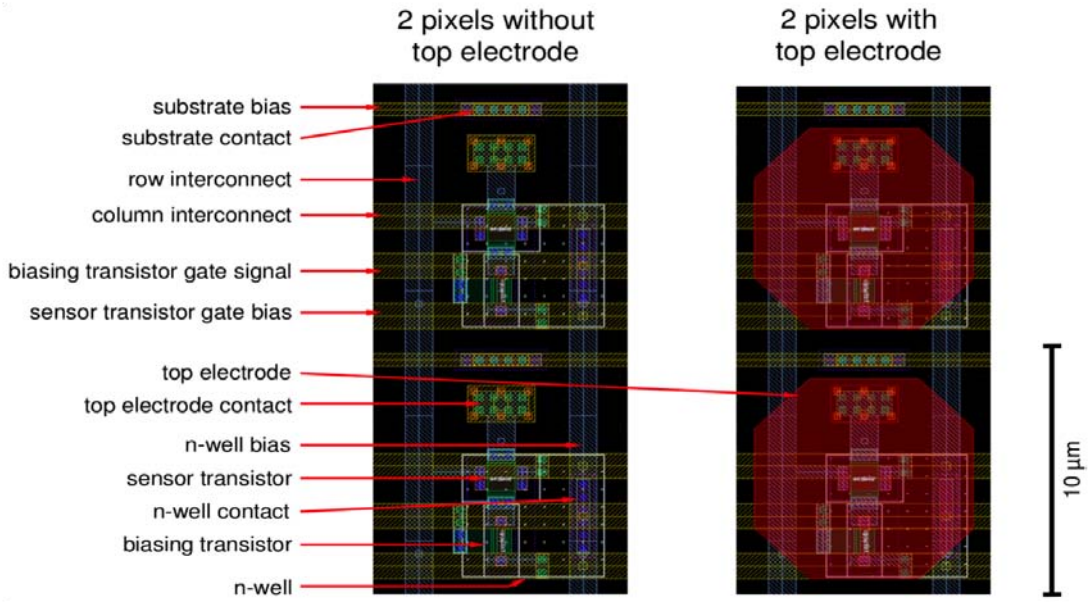

Figure 42: Layout of a couple of pixels next to each other.

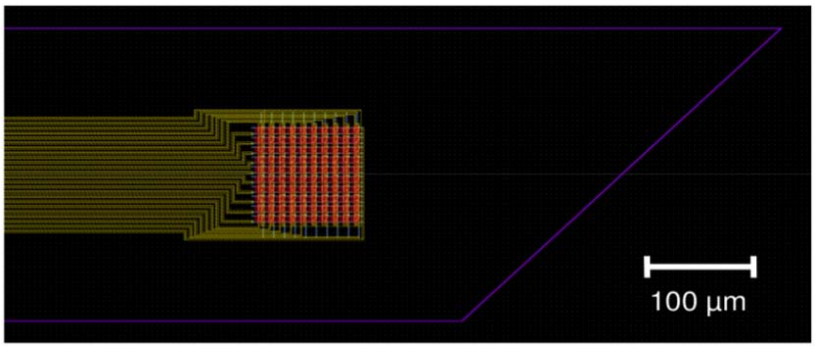

Figure 43: Overall layout of a matrix located on a needle tip.

BONDING PADS Bonding pads are arranged on the end of the needle opposite to the tip, where the device width increases to allow more space. Pads are arranged in specific patterns depending on the device addressing matrix type.
ESD protection structures are realised at the bond pads. These are grounded-gate-MOS

devices, whose behaviour is explained in depth in [Meneghesso *et al.*, 1996]. They are basically made by a MOSFET which gate is connected to substrate together with the source and it is shown in [fig. 44]. Drain is connected to the line to be protected. A parasitic bipolar transistor is then created within he substrate, and a resistance between its base and bulk pad is present. Reverse biasing is avoided by the presence of the drain-body junction, whereas straight ESD impulses are killed by the gg-MOS structure: when a positive ESD event appears upon the protected line, the collector-base junction of the parasitic npn becomes reverse biased to the point of avalanche breakdown. At this point the positive current flowing from the base to ground induces a voltage potential across the parasitic resistor, causing a positive voltage to appear across the base-emitter junction. The positive V_{be} forward biases this junction, triggering the parasistic npn bipolar transistor which then sinks the impulse current.

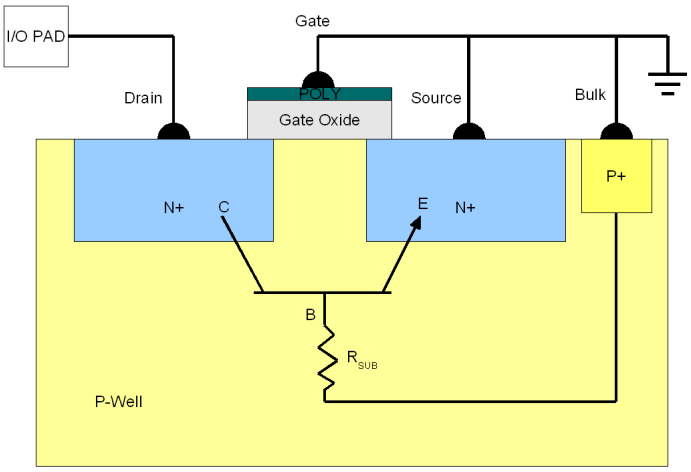

Figure 44: gg-nMOS ESD protection structure, implemented at the bonding pads of the C-100-A/CMOS needles.

Such protection structures have very little influence on signal integrity, however they add a lumped resistor and capacitor to ground at the bond pad. This contribute must be considered when characterising signal and control line impedance.

4.4 STRUCTURE AND PROCESS

The production process was split in roughly four major steps: industry-standard IC process, custom top process and finally needle etching, separation and dielectric coating. Note that for each design both n-MOS and p-MOS version are available, as the design uses only one of the two at a time. The complete layer structure of the device is shown in [fig. 45].

The overall needle thickness is governed by the substrate and is around 100µm. Oxides often present in the back of silicon dies is removed to provide reduced thickness and so less tissue damage at insertions. In most of the possible needle versions, needle tip width is 300µm.

4.4.1 Standard process

Substrate is p-Si where n-MOS are realised. p-MOS can be made too by implementing n-doped wells. Front-end offers three additional metal layers of interconnections which are used for row, column and control lines. Usage of metal layers will provide a much low

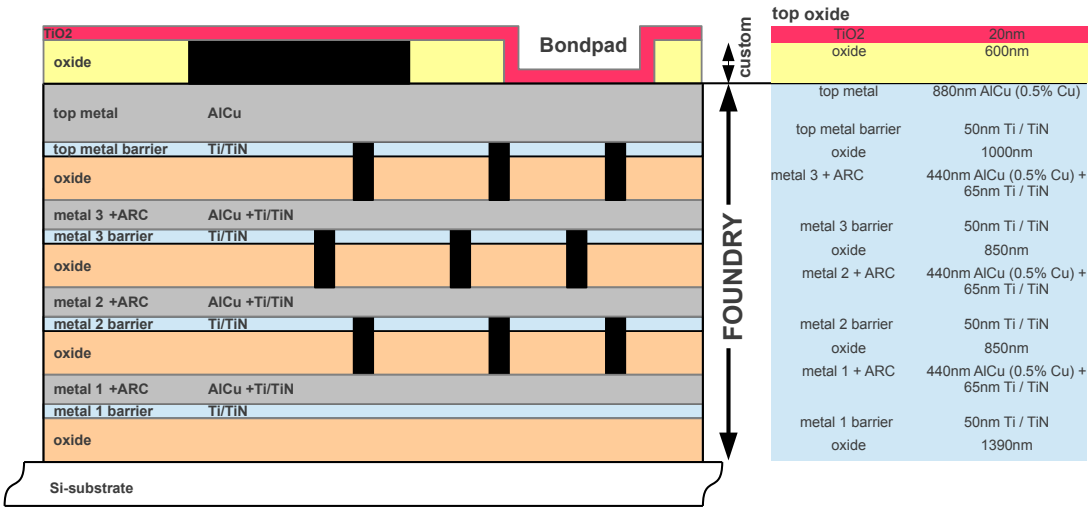

Figure 45: Layer structure of CMOS needles. Industry-standard process is distinguished from custom on-top process.

impedance and crosstalk-proof interfacing than EOSFET needles. One layer is also used to bring interconnects all through the needle to the bonding contacts, which are made of gold coating over the top metal.

METAL FILL Conductive track of metal layers are not completely removed. A squared tile metal fill is left with the aim to improve interference rejection. The tiles are also visible with an optical microscope.

4.4.2 Custom top process

600nm of top oxide (SiO_2) are deposited, and then windows are etched for binding pads and top electrode. Top electrode is made of tungsten of titanium/titanium nitride depending on the production run. Top electrode is in contact with top metal which is then interconnected through vias to transistor gate.

4.4.3 Needle etching

Needles need to be separated from each one. Due to the particular concave form of the needle, no blade cutting can be done, so etching attack is adopted. In the first versions, wet etching with HF acid was done, however with unsatisfying results: acid went under the photoresist, as can be seen from [fig. 46, left] and the side was was decomposed so much to cause the spreading of metal fill tiles. So a new Inductively Coupled Plasma (ICP) etching was performed and a perfectly-cut side wall with no protruding metal fill parts was obtained [fig. 46, right]. Clean etching is very important, because successive dielectric coating will be conformal, and so mechanical strength of the border part of the needle can be affected by irregular shapes, as well as electric field in the dielectric, whose shape can strongly depend on side-wall planarity.

The single needle is the separated from the wafer and undergoes further processing. The etched needles are shown in [fig. 47] from which it is clear why dicing was not an option.

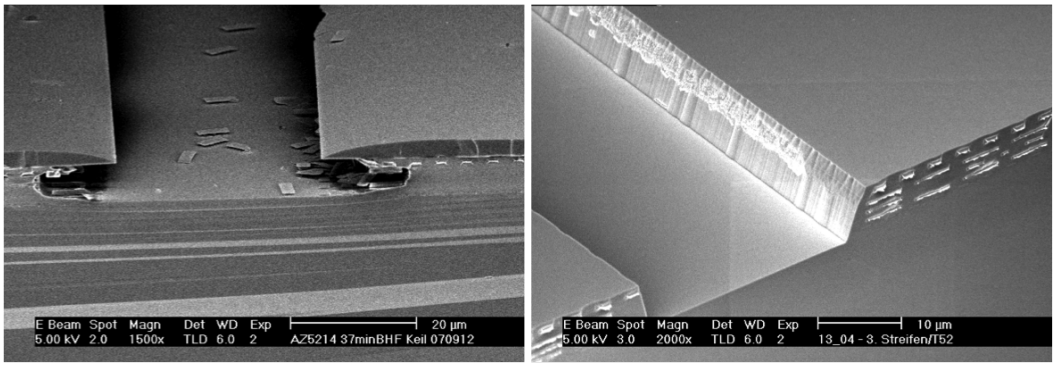

Figure 46: Old HF wet etching process (left) and new ICP dry etching (right). The differences are very evident. The metal tiles are lost from the layer and can be seen in the micrograph.

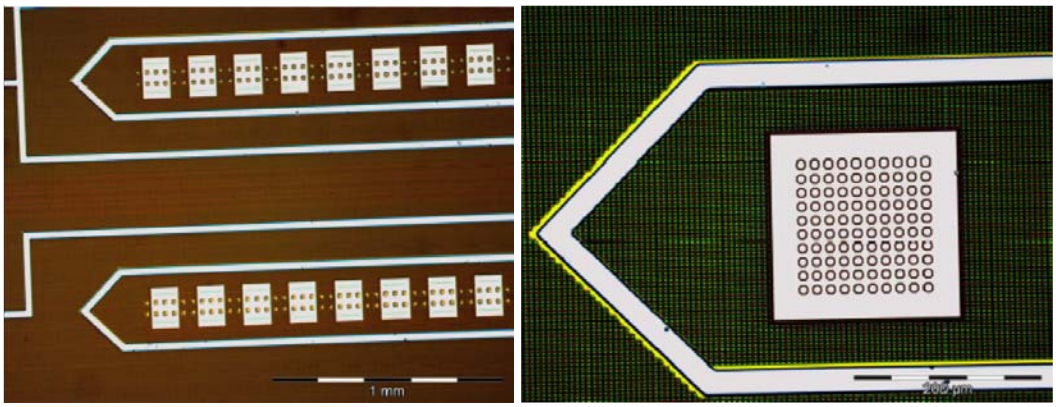

Figure 47: Photos of etch-cut C-100-A/CMOS needles with new ICP process.

4.4.4 Dielectric coating

After being separated from wafer, the needles undergo Atomic Layer Deposition (ALD) of dielectric material. This step is currently executed at MDM-CNR laboratories in Milano and also a process by TUB in Berlin is being tested. The whole needle is covered, rather than only the top electrode. This choice, which is actually a result of not having any mask in the ALD process[4]. Different materials are being tested and so have been deposited, like TiO_2, $AlHfO_2$, HfO_2, as well as different thicknesses from 20nm to 260nm.

ATOMIC LAYER DEPOSITION ALD is a thin film deposition process which applies self-limiting or sequentially self-terminating films via chemical vapor deposition (CVD). ALD uses volatile chemicals called precursors and alternating surface reactions to grow self-limiting layers of film. Each layer is the result of the chemical reaction between two precursors. By repeating the process of growing individual layers, thin films can be applied to surfaces. Some advantages of a self-limiting film include uniform surfaces, high conformity to surface features, high control and accuracy of atomic level thickness, and high reproducibility. ALD does have some limitations including incomplete reaction and slow rate of reaction. ALD realised inside an airtight high temperature chamber, which needs to be fully cleaned, together with its content, between each run to avoid contamination. Cleaning is made with very aggressive acids, so that everything inside the chamber, which is made of quartz crystal, must be made of the same material[5]. Apart from the many limitations, the big advantage of ALD is the low temperature, which avoid device damage or unwanted annealing processes.

DIELECTRIC KEY FIGURES As it will be cleared in the next chapter, the primary keys of selection of the dielectric materials are the dielectric constant k and the leak conductivity σ or the leakage current density j_{leak}. In an ideal capacitor, $k \to \infty$, $\rho \to 0$ is desired. This is because higher k provides a higher capacitor value and thus a better coupling of top electrode with electrolyte potential Φ, whereas low leakage results in lower current to maintain M_{sense} gate bias.
Those two important figures of the considered dielectric candidates are the subject of [tab. 2], in which expected values (from literature) of these are presented. Actually, it must be considered that I/V characteristics of such materials all but resistive. So, a conservative upper bound among a reasonable bias interval is reported. Moreover, tunnelling component of leakage depends heavily on thickness, so data is reported with thickness for reference. In the case of TiO_2, anatase phase was confirmed by MDM-CNR labs.

Table 2: Expected values of dielectric key figures with references.

Material	Expected k	Expected j_{leak} [$\mu A/cm^2$]
TiO_2	33.9 [Wallrapp and Fromherz, 2006]	< 5(15.6nm) [Wallrapp and Fromherz, 2006]
$AlHfO_2$	20-25 [Yoo *et al.*, 2014]	<50 (3nm) [Zhu *et al.*, 2002]
HfO_2	15.4 [Wallrapp and Fromherz, 2006]	< 5(18.3nm) [Wallrapp and Fromherz, 2006]

4 Actually, being ALD process non directional, it is quite hard to mechanically mask any part of the circuit, bonding pads included.

5 It is now easy to understand the difficulty in holding the needle samples in position with no clamps or adhesives available.

4.4.5 Wire bonding and interfacing

After dielectric deposition, device is sticked on a custom-made PCB with pad for wire-bonding and a board-to-wire connector. Wire bonding is performed by breaking the dielectric layer with ultrasonic bonding machine and sticking the wire to the underneath pad. When bonded, the bonding region is coated with epoxy protective material. In principle, miniature neuro connectors by Omnetics®were used. However, the number of connector lines (40) were not so high to require a high level of miniaturisation, and cost of the single connector was high. So that a more commercial alternative was looked for, and now sensor PCB is equipped with Molex®Pico-Clasp^{TM} connector.

A picture of a finished 2×50 needle tip is shown in [fig. 48] whereas a picture of a single recording pixel taken with multifocal shot is shown in [fig. 49].

4.5 METAL–OXIDE–ELECTROLYTE (MOE) CAPACITORS

The top electrode forms with the electrolyte a Metal-Oxide-Electolyte capacitor. The base structure and working principle are very similar to an electrolytic capacitor, in which the buildup of charge at the metal electrode attracts counter-ions to the surface of the insulator and repels co-ions which then screen the electric fields in a characteristic Debye length λ_D, beyond which the potential drop is null. A complete model of a Stern capacitor is fairly complicated, and is deeply discussed in [Jiang and Stein, 2010], however a brief discussion is given in this paragraph. A Stern modelling of the so-formed EDL is suitable.
With reference to [fig. 50.a], let the planar gate electrode of the MOE capacitor be biased at voltage V_g. Electrochemical potential at the insulator surface is denoted as Ψ_0. The insulator is assumed to be in contact with a solution whose pH, bulk electrochemical potential, V_b, and concentration of monovalent salt, n, are all assumed to be constant far away from the surface. Close to the surface, the electric fields from the gate electrode and σ_{chem} induce the formation of the electric double layer. The innermost layer of counterions is known as the Stern layer, which is tightly bound to the surface. The Stern layer is separated from the surface by an effective distance δ comparable to the ionic radius. The electrochemical potential at the Stern layer is denoted Psi_{DL}. The diffuse layer is the portion of the electric double layer that extends farther away from the surface, where the electrochemical potential decays to the bulk value, V_b. The electric double layer screens electric fields, whether they originate from the chemical charge at the oxide surface or from the applied voltage across the capacitor. To treat these two contributions separately, an equivalent circuit model of the MOE capacitor is shown in [fig. 50.b]. The electric double layer part, which is treated as a nonlinear element, can be modelled using the Poisson-Boltzmann equation.
The surface of the insulator can be carpeted with ionizable groups giving rise to the chemical surface charge density, ?chem, when in contact with solution, as depicted.

Analytic study of the system in [Jiang and Stein, 2010], suggests that in the absence of ionisable groups, $\sigma_{chem} = 0$ and each remaining charge contribute is linearly dependent on electric field in the oxide, so a constant value capacitor - even insensitive on pH value - is expected in this case. However, the CV characteristics of such element will be object of further investigations in this work, also to determine which materials have better ideal behaviour.

LEAKAGE MECHANISMS Many mechanisms can contribute to a leakage current through the dielectric layer, which should ideally be a very good insulator due to its wide energy gap. Fowler-nordheim tunnelling is reported for Au contacts on TiO_2 [Aarik *et al.*, 2004], and also trap-assisted tunnelling is a well-known leakage mechanism for TiO_2. Barrier tunnelling depends obviously on contact material workfunction. Moreover, the dielectric-electrolyte interface is dynamic, and so can make voltage dependency of such leakage behaviours worse.

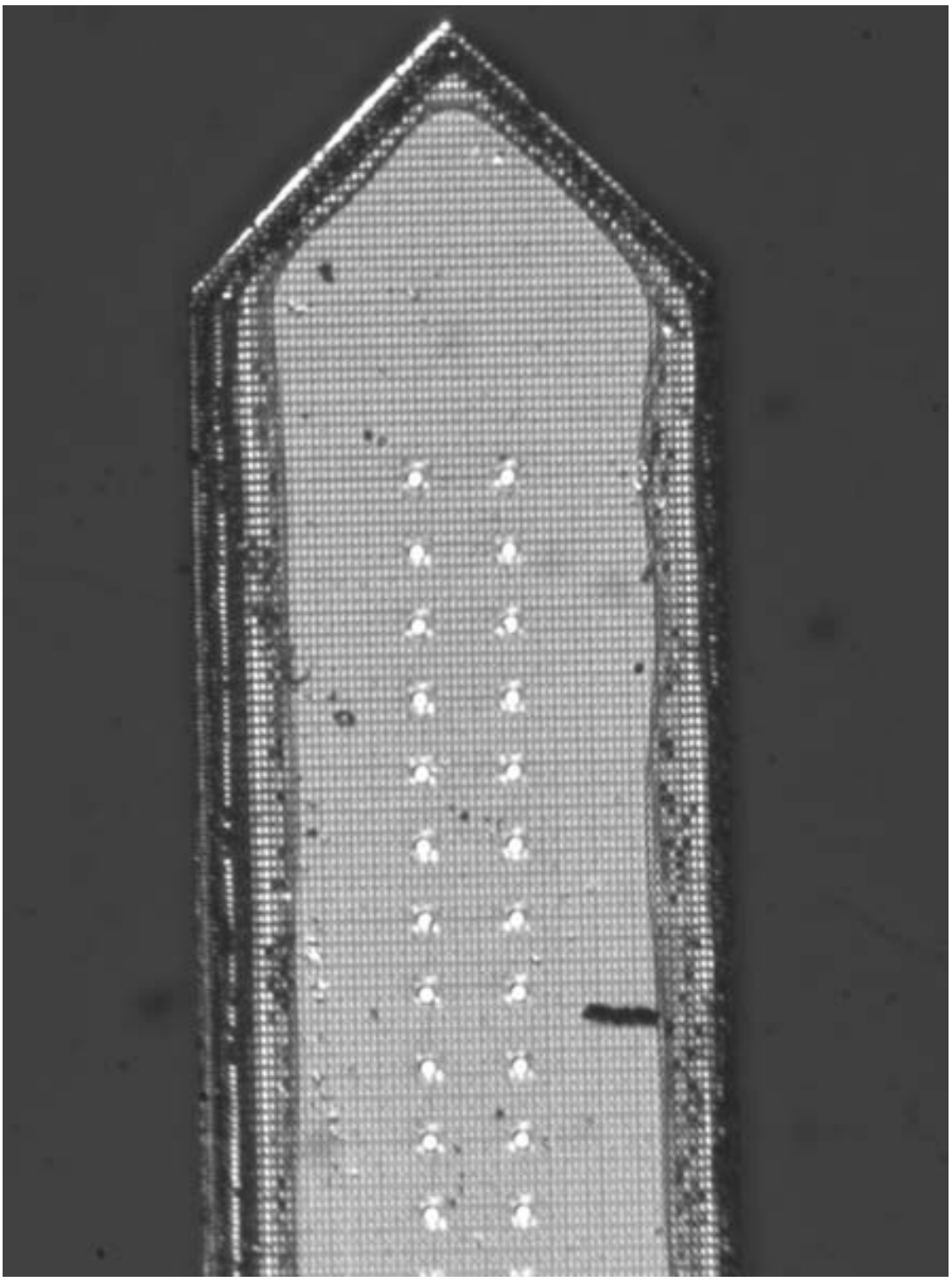

Figure 48: Micrograph of a 2×50 CMOS needle tip.

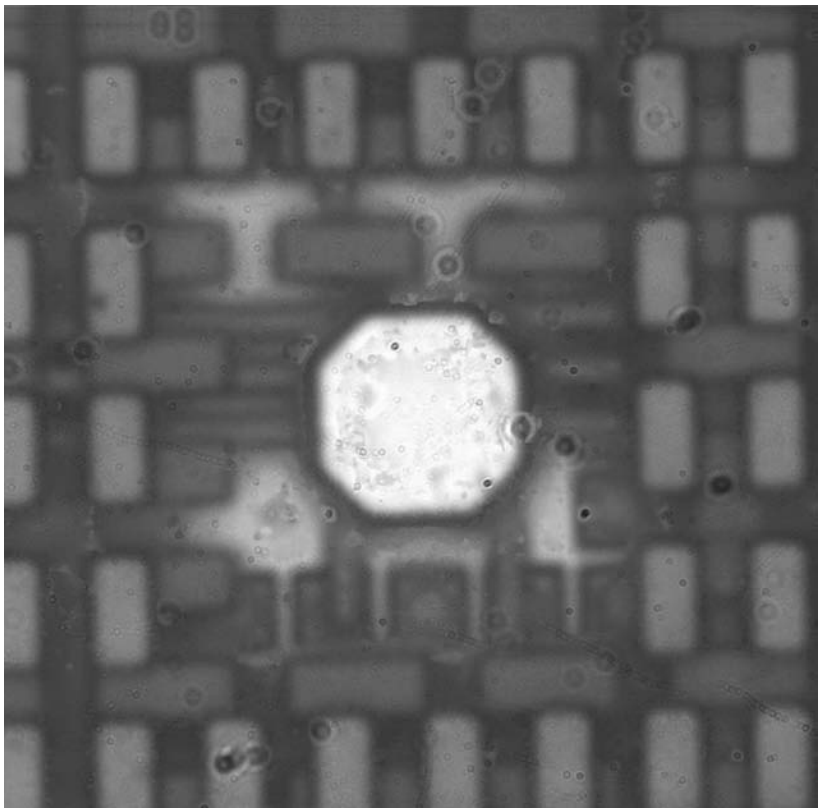

Figure 49: Micrograph of a single pixel of a CMOS needle tip. The octagonal top electrode is clearly visible. SiO_2 insulator between metal layer is transparent to visible light, so it is actually possible to see the structures and tracks under the surface. Multiple shots were taken with different focus depths and then merged into a single one to show the whole. Such technique is called *focus stacking*. Resolution is at limit of the power of the used objective.

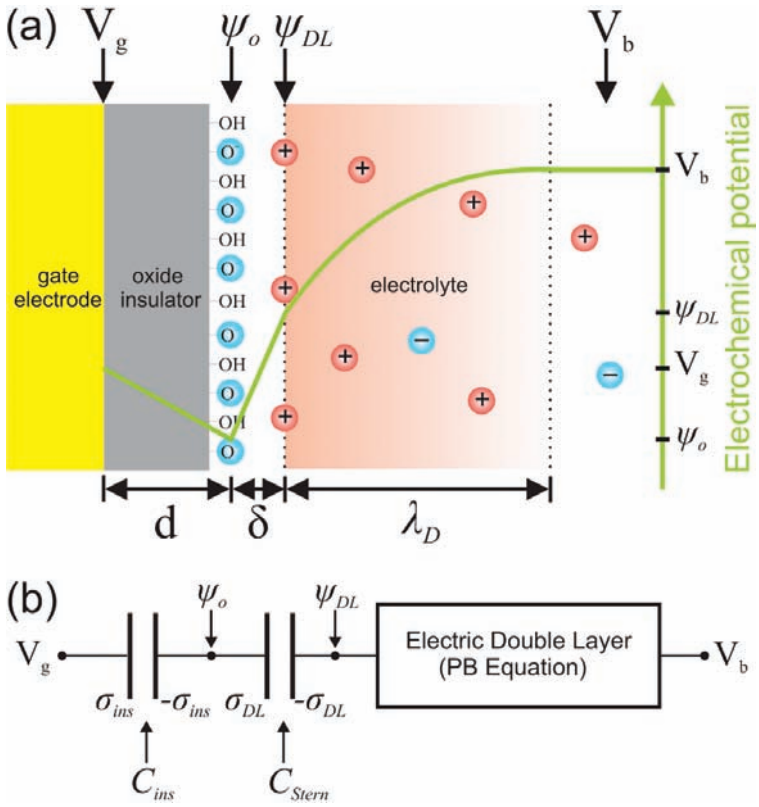

Figure 50: Modeling of a MOE capacitor. [Source: [Jiang and Stein, 2010]]

Investigations on leakage mechanisms of adopted oxides is planned to better understand the optimisations than can be done on the process or on the materials.

4.6 NEEDLE INVENTORY

Many versions of C-100-A/CMOS needles were produced within the framework of this project. A complete inventory of the needles that actually arrived on the laboratory shelf - as they were considered candidates for testing - is reported in [tab. 3]. Newer batches, from Aug 2014 on, have Ti/TiN electrodes. Older have tungsten electrodes.

Finally, a photo of the full device, bonded on the connector PCB is shown in [fig. 51].

4.7 OPERATION

C-100-A/CMOS devices are operated very similarly to the EOSFET needles. The mechanical dimensions, stiffness and break limit are nearly the same, being a property of the silicon substrate. So positioning and insertion arise the same kinds of issues (space, cable hardness, precision of positioning) except for the connector, which is bigger in the C-100-A/CMOS needles. However, the operative advantages of a commercial connector have, until now, overcome the limitations.

Table 3: Inventory of needles updated on November 28th, 2014 (continues...)

Lot	ID	Type	Matrix	Pitch	Ch	Coating
Jan 2014	0197	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0198	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0199	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0200	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0201	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0202	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0203	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0204	TIP_L	2×50	$30 \times 39.2\mu m$	P	Uncoated
	0205	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0206	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0207	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0208	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0209	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0210	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0211	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
	0212	TIP_L	2×50	$30 \times 39.2\mu m$	N	Uncoated
Mar 2014	0164	TIP_A	10×10	$10\mu m$	P	20nm TiO_2 (MDM)
	0165	TIP_A	10×10	$10\mu m$	P	20nm TiO_2 (MDM)
	0166	TIP_A	10×10	$10\mu m$	P	20nm TiO_2 (MDM)
	0167	TIP_A	10×10	$10\mu m$	P	20nm TiO_2 (MDM)
	0168	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0169	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0170	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0171	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0172	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0173	TIP_A	10×10	$10\mu m$	N	20nm TiO_2 (MDM)
	0174	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0175	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0176	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0177	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0178	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0179	TIP_A	10×10	$15\mu m$	N	20nm TiO_2 (MDM)
	0180	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
	0181	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
	0182	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
	0183	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
	0184	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
	0185	TIP_A	10×10	$15\mu m$	P	20nm TiO_2 (MDM)
Jun 2014	0190	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0191	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0192	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0193	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0194	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0195	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)
	0196	SHANK	2×50	$30 \times 39.2\mu m$	N	20nm TiO_2 (MDM)

Table 4: (continued...) Inventory of needles updated on November 28th, 2014.

Lot	ID	Type	Matrix	Pitch	Ch	Coating
Aug 2014	0001	TIP_L_STC	2×50	$30 \times 39.2\mu m$	P	260nm TiO_2 (MDM)
	0002	TIP_L_STC	2×50	$30 \times 39.2\mu m$	N	260nm TiO_2 (MDM)
	0003	SHANK	2×50	$30 \times 39.2\mu m$	P	260nm TiO_2 (MDM)
	0004	SHANK	2×50	$30 \times 39.2\mu m$	N	260nm TiO_2 (MDM)
	0005	TIP_A	10×10	$10\mu m$	P	260nm TiO_2 (MDM)
	0006	TIP_A	10×10	$10\mu m$	N	260nm TiO_2 (MDM)
	0007	TIP_A	10×10	$15\mu m$	P	260nm TiO_2 (MDM)
	0008	TIP_A	10×10	$15\mu m$	N	260nm TiO_2 (MDM)
	0009	TIP_L_STC	2×50	$30 \times 39.2\mu m$	P	260nm TiO_2 (MDM)
	0010	TIP_L_STC	2×50	$30 \times 39.2\mu m$	N	260nm TiO_2 (MDM)
	0011	TIP_L	2×50	$30 \times 39.2\mu m$	P	260nm TiO_2 (MDM)
	0012	TIP_L	2×50	$30 \times 39.2\mu m$	N	260nm TiO_2 (MDM)
	0020	TIP_A	10×10	$15\mu m$	P	60nm TiO_2 (MDM)
	0021	TIP_A	10×10	$15\mu m$	N	60nm TiO_2 (MDM)
	0022	TIP_A	10×10	$10\mu m$	P	60nm TiO_2 (MDM)
	0023	TIP_A	10×10	$10\mu m$	N	60nm TiO_2 (MDM)
Nov 2014	0213	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0214	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0215	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0216	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0217	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0218	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0219	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)
	0220	TIP_L	2×50	$30 \times 39.2\mu m$	N	22nm TiO_2 (TUB)

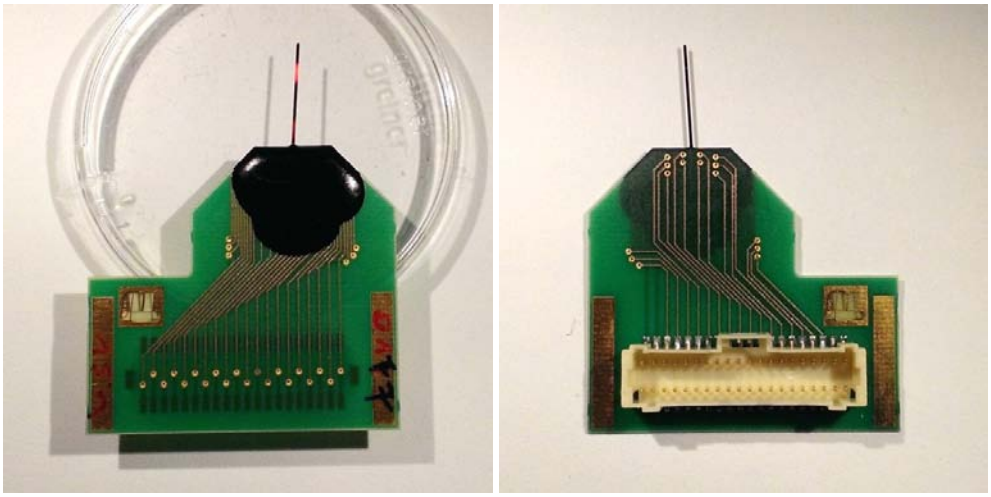

Figure 51: Photo of a C-100-A/CMOS needle bonded to its PCB board.

4.7.1 Bias strategy

In the C-100-A/CMOS needled, the gate biasing circuitry must additionally be managed. Let the substrate voltage $V_sub = 0V$ then the voltage $V_{op} = V_{g*}$ should be equal to the desired gate voltage of the transistor M_{sense}. Switch control voltage V_{ops} should be trimmed to keep M_{bias} in threshold region, considering that $V_{gs,M_{bias}} = V_{ops} - Vop$ in ideal steady state[6] and that the body effect increases threshold voltage V_t of such transistor.

VOLTAGE BIASING Until now, it was took from granted that devices are biased with constant voltages and output signal is the drain current. It could however be objected that current biasing is a much more common approach for low noise amplifiers such in this case. However, the matrix design of the chip suggests voltage biasing: if a FET, as a result of a gate signal, should vary its drain voltage (because it's current-biased) it would carry with itself also all other FETs connected to that line, so this seems illogical. Probably a scenario in which this is handled and the system works in current bias could be elaborated, but it's unlikely to bring advantages.
In the end, constant voltage biasing has also many advantages, among other the absence of miller elect and relative capacitance, as drain voltage is steady; and the fact that, being the input amplifier a current-to-voltage low impedance amplifier, the interconnecting cables are less likely to pick up capacitive interferences, which are most likely to happen that inductive ones (excluding lights and line-conducted disturbances, elements such as piezo drives are a strong source of capacitive-coupled interferences.

MATRIX ADDRESSING The biasing of rows and columns is somewhat tricky: a smart biasing has to enable only the column[7] (or the multiple comumns) that should be observed and minimise influence of remaining rows[8]. The choice to assign drain or source voltages respectively to rows and columns or vice versa is purely arbitrary: the devices are indeed symmetrical by design. Two examples of different choices lead to different bias strategies, which can - depending on the boundary conditions - provide or not particular advantages.

In a first approach, it will be considered that **columns are connected to drains** and **rows are connected to sources**.
A scheme of the biasing strategy is shown in [fig. 52].

As it can be seen, all rows are kept at the desired source voltage level V_{source} which is likely to be the same as V_{sub}. Then, the selected column is drive at V_{drain} whereas all other columns are kept at V_{source}. This way, on the FETs which are not being read, the channel is still formed[9] but no current is flowing because V_{ds}=0.

In a second approach, shown in [fig. 53], it will be considered that **rows are connected to drains** and **columns are connected to sources**.

There is actually not much difference on the two approaches, however there are some practical advantages when also the biasing of other lines, such as substrate or gate, is considered. A transimpedance amplifier is easier to realise when referred to ground voltage. It exhibits better stability, precision and most of all lower noise. So, when it is desired to have source nodes at ground the former strategy is better, when drains are required to be at ground - as in the later discussed *grounded-gate configuration* - the latter should be preferred.

6 That is, when drain and source voltages of M_{bias} are identical.
7 Assuming that scan multiplexing is done by columns.
8 In de end, it should not be forgotten that the FETs are still here despite being not read.
9 This cannot actually be avoided, because V_{gs} is common to the whole row.

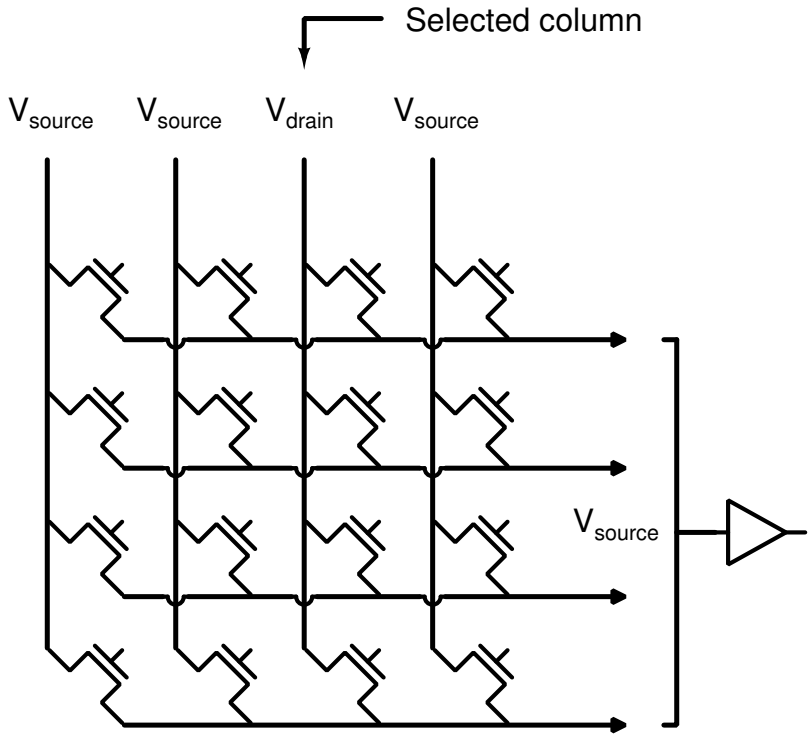

Figure 52: Example of bias strategy for addressing a single column of the matrix (expected current verse for n-MOS devices is shown).

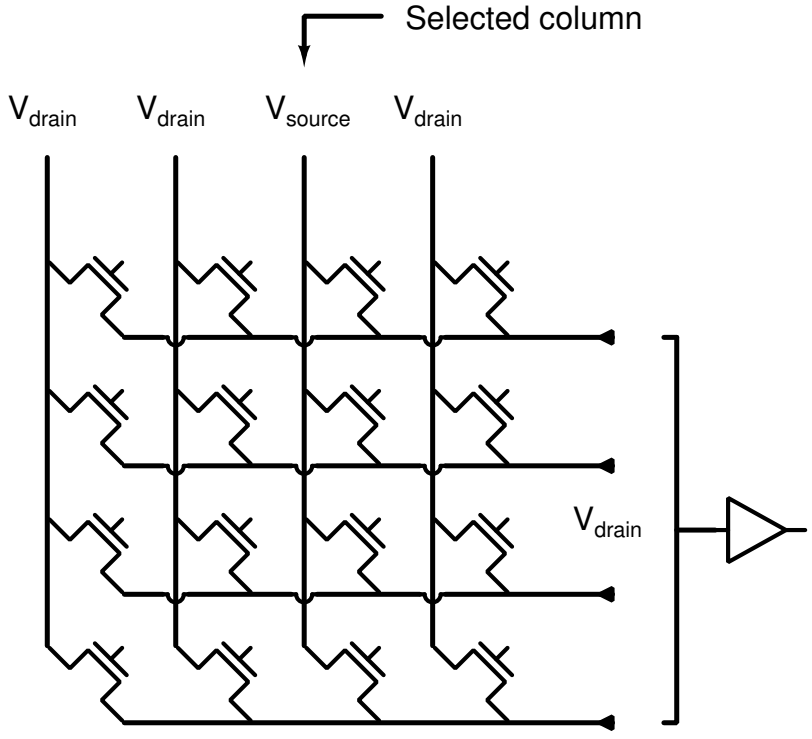

Figure 53: Example of alternative bias strategy for addressing a single column of the matrix (expected current verse for n-MOS devices is shown).

4.7.2 Readout

Readout of current signal is done with an array of transimpedance amplifiers, which design requirements and implementation overview is given in chapter A. If multiplexing is desired, the selected column must be commutated at a specific rate. The data acquisition system must then attribute the correct time frame to the selected row at that time. Further evaluations and calculations (of which an initial sketch will be then given) must be done in order to determine what is the correct scan rate to obtain a desired bandwidth over the entire array, also considering that:

- being the duration of a scan necessarily similar to the scan rate, the samples will be progressively misaligned in time, so that will heel to be accounted when performing time-wise interpolation;
- as bandwidth of the FETs is fairly larger than desired bandwidth of the system and thus of scan rate, consistent noise folding is expected to happen and to give a relevant contribute of total output noise.

4.8 PARALLEL DEVELOPMENTS

CMOS technology applied to neural recording finds a growing number of examples in the recent year, although being the subject of this work the result of the first attempts to gain high performance recording in vivo with CMOS technology. An example of an in-vitro recording application is brought here.

4.8.1 In vitro CMOS matrix sensors

Flat chips, bonded in a classic package, are available for in-vitro recording. These chips are provided with a relevant quantity of high density needles on the is flat top surface, as well as integrated device management, multiplexing, signal conditioning and (in some cases) A/D conversion. An example is given in [Eversmann *et al.*, 2003], in which a 128x128 array was build.

STRUCTURE In [fig. 54] the cross-section structure can be seen. It clearly resembles the one of the C-100-A/CMOS needles, and the distinction between the standard process layer and the custom backend is visible. Also the connection path between top electrode and gate is well shown by that micrograph. The device is then bonded in a traditional square ceramic package and a plastic cup is glued to it, in order to provide a sealed environment for growing the neuron cells and then pouring the electrolyte to be biased with a reference electrode. It must be said that this device is designed to measure mainly single unit firings from neurons that are directly grown attached to the surface, so that requirements are in some ways different.

OPERATION In the case of this kind of devices, the cells are cultured directly inside the chip (so it's important to have a biocompatible coating dielectric). When cells are grown ready for experiment, electrolyte is poured inside the chamber and a reference electrode is used for biasing. Then as an example, a micropipette or metal electrode is used to stimulate a neuron to fire and the resulting data is recorded. Often, as in the case of the mentioned example, on-board amplification is available or even ADC conversion. This kind of devices can, as of now, provide a higher number of recording site as well as improved resolution with respect to needles; of course, in vivo recording is not possible with this kind of devices. At the moment, this is a reliable option to monitor single unit trains over a large community

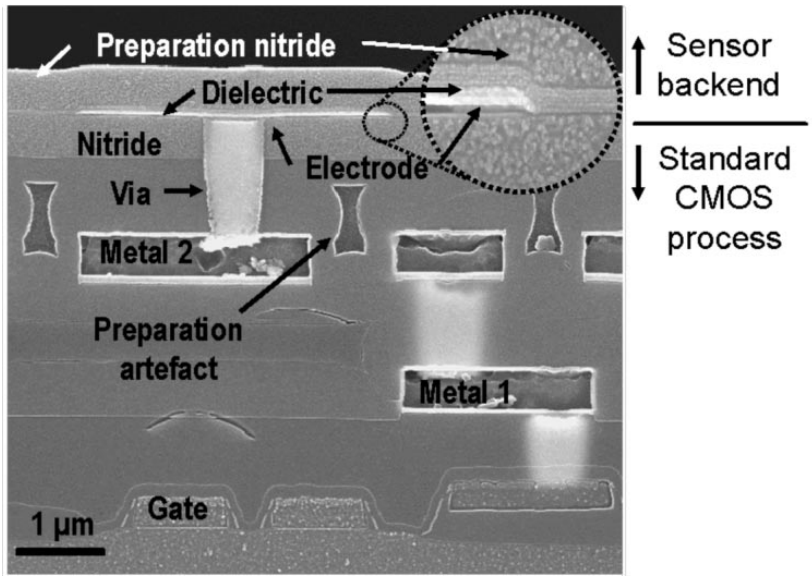

Figure 54: SEM photo of sensor cross section of a 128×128 matrix recording chip. [Source:[Eversmann *et al.*, 2003]].

of neurons. For this reason, it is being implemented at the moment in the framework of the RAMP project to allow communication between alive and artificial networks.

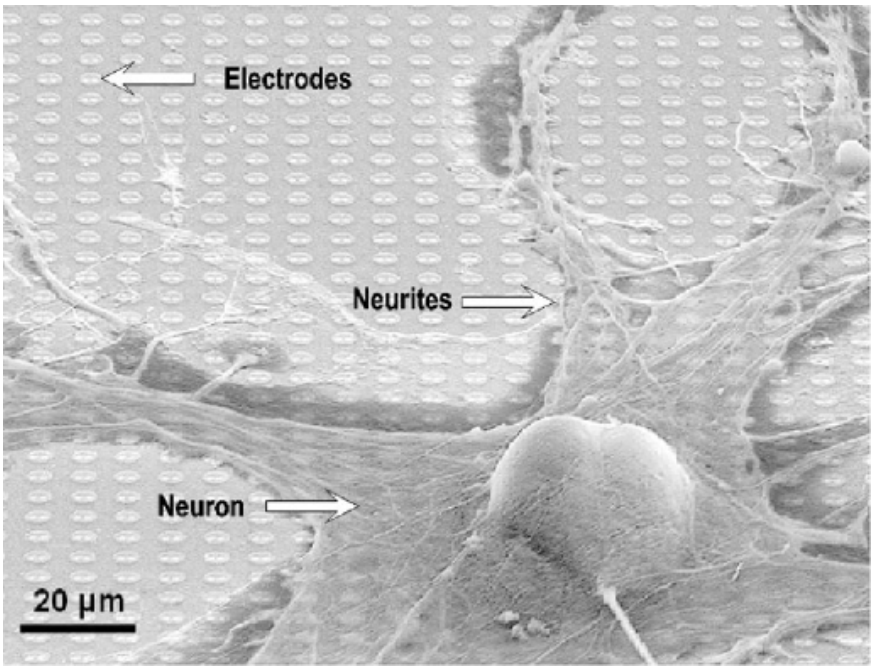

Figure 55: Snail neuron on sensor chip array in culture. [Source:[Eversmann *et al.*, 2003]].

5 SIMULATION AND CHARACTERISATION

In this chapter the C-100-A/CMOS needle chip characteristics are first evaluated theoretically and simulated, and the verified with both ad-hoc and standard characterisation techniques. The problem of correct biasing and the top oxide leakage - which are proven to be critical - are specifically addressed.

5.1 DEVICE SIMULATION

The single pixel cell of a C-100-A/CMOS needle chip is simulated in order to evaluate correct operating points and understand the expected device behaviour. Relevant figures are then extracted in order to compare with further characterisations. The simulation, accounting for the aforementioned reasons, involved only n-channel type devices. Simulation is performed with Cadence® Virtuoso® design environment from schematic layout, using SPECTRE circuit simulator software and proper technolgy file[1].

5.1.1 Preliminary design-driven considerations

With reference to the aforementioned schematic of the single pixel cell, the suggested bias point[2] from the designer is depicted in [fig. 56] and summarised in [tab. 5][3]).
Transistor M_{sense} is biased with $V_{ds} = V_{gs}$ (diode configuration). This choice is taken for esse of biasing and characterisation, even though an optimization of V_{ds} targeting overall SNR is desirable.
Transistor M_{bias} is in kept in deep subthreshold region and has to sustain the leakage currents in order to bring V_{gg} as close as possible to V_{op}, while offering a high output impedance in order not to attenuate signal coupled to V_{gg}.

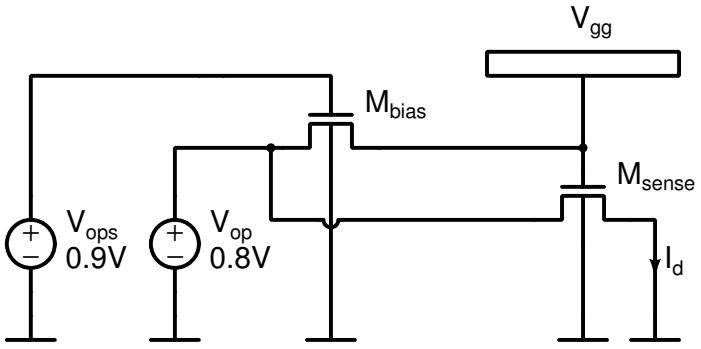

Figure 56: Suggested biaspoint for the single pixel cell.

In order to better evaluate what in a rough evaluation arises no major concerns, it is mandatory to include intrinsic and extrinsic parasitic elements. The schematic, accounting

1 Software availability was kindly granted by Technische Universität Berlin, department of Sensors and Actuators.
2 Bias point is defined in voltage mode. The reason for this choice was already discussed; see chapter 4 for details.
3 As previously discussed, it must be taken into account that devices are perfectly symmetrical, so the definition of a source and drain - as well as its association with row and column - is arbitrary for what concerns the device itself.

Table 5: Suggested biaspoint for the single pixel cell.

Node	Voltage [V]
V_{col} (V_s)	0
V_{row} (V_d)	0.8
V_{op}	0.8
V_{ops}	0.9
V_{sub}	0

for electrode oxide and drain diffusion leakage, is extended to the following single pixel model in [fig. 57].

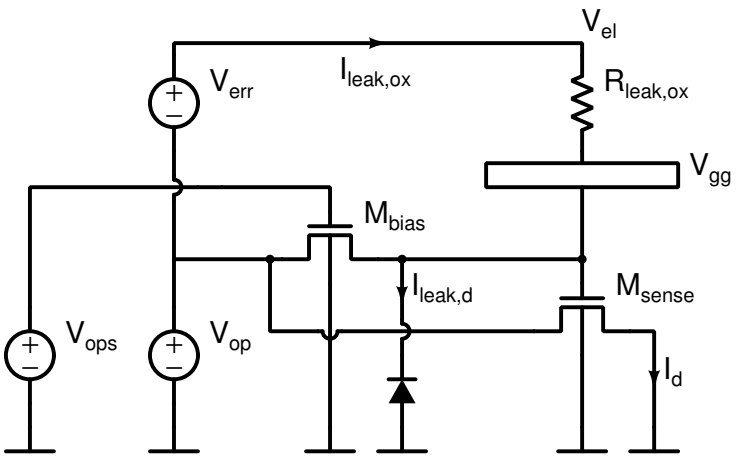

Figure 57: Leakage model for the single pixel cell.

As can be seen, the drain leakage current of transistor M_{bias} is represented as a reverse-biased diode junction, whereas the electrode-oxide leakage is represented by a resistor connected to a V_{err} voltage source which represents the maximum error committed by cause of the reference electrode potential with respect to the V_{op} voltage. In fact $V_{el} = V_{op} = V_{gg}$ would be the ideal condition to minimise $I_{leak,ox}$[4]. From previous evaluations, V_{err} is estimated around $0.25mV$. By inspection, two main concerns arise after evaluating parasitics:

- the voltage drop across M_{bias} in order to balance leakage currents could be significantly big, thus leading to a bias error of V_{gg};
- the channel resistance of M_{bias}[5] could be too low for the input impedance constraint at electrode.

5.1.2 DC Parameters extraction

Technology process specifications were made available to the author, however simulations were performed in order to extract critical DC parameters.

Threshold voltage is often the most uncertain and dispersed parameter in MOS technology. If we consider the triode characteristics of the MOS in (24)[6], we discover it is pretty

4 As discussed - without a potentiostatic circuit - the exact electrolyte voltage is not trimmable with accuracy.
5 Considering the suggested bias point or every other convenient bias point.
6 Please note that, being all the devices involved larger than $1 \times 1\mu m$, large channel MOS models are considered.

linearly dependent on V_{gs} with a negligible offset when V_{ds} is low.

$$I_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{24}$$

A linear interpolation of the I_d-V_{gs} characterstics at $V_{ds} = 100mV, V_{gs} > 1V$ in [fig. 58] leads to an estimation of $V_T = 0.64V$ with an error of about $5mV$ due to V_{ds} bias[7], which is a good match with the declared technology parameter.

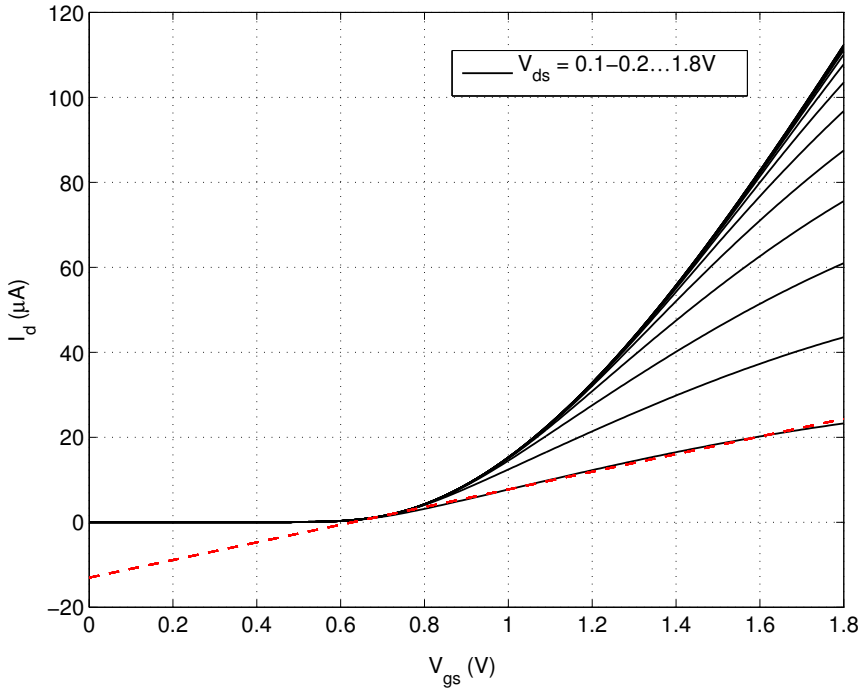

Figure 58: Simulated I_d-V_{gs} characteristics of a $1 \times 1\mu m$ n-MOS transistor like M_{sense}.

Considering I_d-V_{gs} characteristics with $V_{ds} = 1.8V$, the MOS is definitely biased into saturation region. This allows to state that the current value must obey[8] equation (25).

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_T)^2 = \frac{K_f}{2} (V_{gs} - V_T)^2 \tag{25}$$

in which K_f is named the current factor. The equation can be conveniently rewritten in form (26) which allows to spot the possibility for a linear interpolation.

$$\sqrt{I_d} = \sqrt{\frac{K_f}{2}} (V_{gs} - V_T) \tag{26}$$

The square root of the drain current I_d is shown in [fig. 59] and allows to extract a current factor $K_f = 150\mu A/V^2$.

Transconductance with $V_{gs} = V_{ds}$ is simulated and represented in [fig. 60][9] and reproduces the aforementioned "diode configuration".[10]. In the considered bias point range, a

7 This method for extracting V_T was chosen for its simplicity and, due to its effectiveness, was chosen among many other methods the authors is aware of.

8 Neglecting the channel length modulation effect.

9 Of course $g_m = \frac{\partial I_d}{\partial V_{gs}}$ regardless the particular transistor biasing.

10 g_m is relative to a $1 \times 1\mu m$ MOS device, such as M_{sense}, and should be scaled accordingly with the (W/L) ratio in order to infer data concerning M_{bias}.

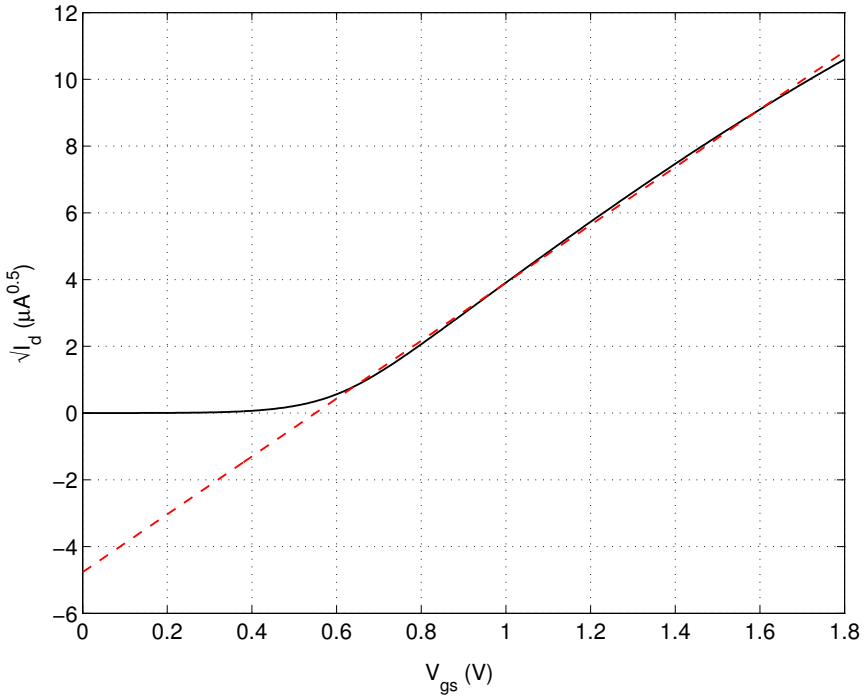

Figure 59: Simulated square root of I_d-V_{gs} characteristics of a $1 \times 1\mu m$ n-MOS transistor like M_{sense} with $V_{ds} = 1.8V$.

transconductance of $40 - 80\mu S$ is expected.

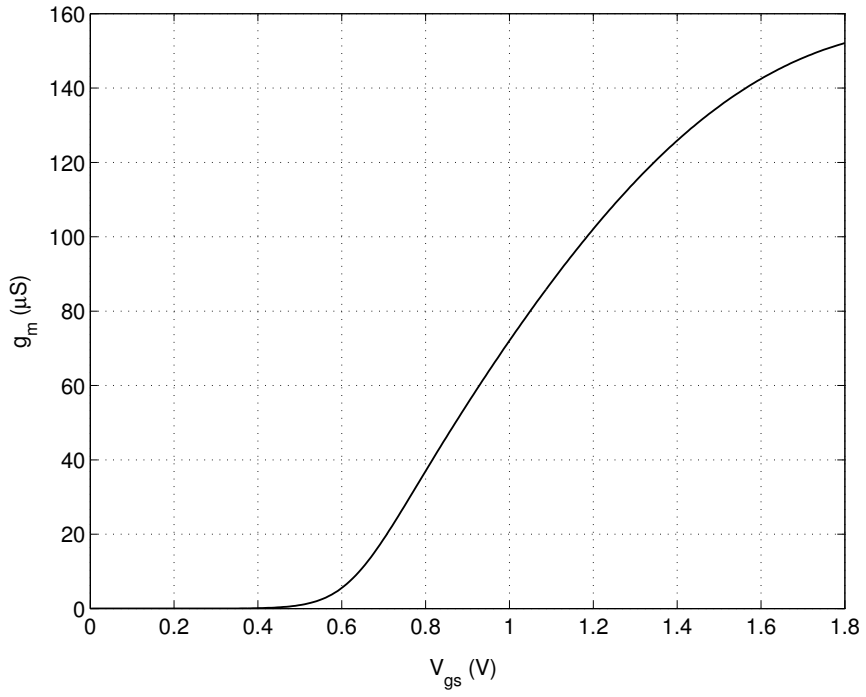

Figure 60: Simulated g_m-V_{gs} characteristics of a $1 \times 1\mu m$ n-MOS transistor like M_{sense} with $V_{gs} = V_{ds}$.

Subthreshold slope was the most interesting parameter to investigate, being involved into the main concern about bias point evaluation. Widely-known subthreshold current expression is represented in (27).

$$I_d = I_{d0} \exp \frac{V_{gs} - V_{th}}{\left(1 + \frac{C_d}{C_{ox}}\right) V_T} \tag{27}$$

The subthreshold slope:

$$S_{s-th} = \log_{10} \left(1 + \frac{C_d}{C_{ox}}\right) V_T \tag{28}$$

is conveniently defined on a base-10 logarithm, from which the whole equation (27) can be rewritten in equation (29) for ease of data extrapolation:

$$I_d = I_{d0} 10^{\frac{V_{gs} - V_{th}}{S_{s-th}}} = \left(I_{d0} 10^{\frac{-V_{th}}{S_{s-th}}}\right) 10^{\frac{V_{gs}}{S_{s-th}}} \tag{29}$$

The simulated I_d-V_{gs} shown in logarithmic scale in [fig. 61] allows to extract $S_{s-th} = 94mV/dec$ and $I_{d0} = 1.5\mu A$ at ST (Standard Temperature condition)[11]. When applying expression (27) to further calculations, $V_{th} = V_{th0} + \gamma \left(\sqrt{V_{sb} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$ must be set, thus taking into account the body effect to which M_{bias} undergoes by design[12].

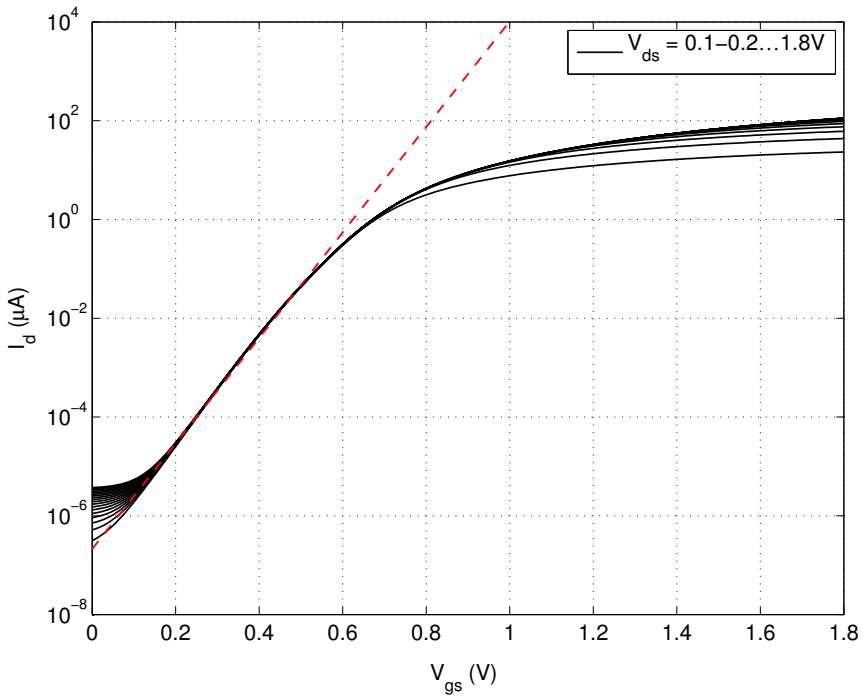

Figure 61: Simulated I_d-V_{gs} characteristics of a $1 \times 1\mu m$ n-MOS transistor like M_{sense}, with focus on the subthreshold region.

Device output resistance is convientionally modeled as dependant on drain current I_d according to (30):

$$R_{ds} = \eta \frac{L}{I_d} \tag{30}$$

thus an exponential dependance of R_{ds} on V_{gs} is expected in the subthreshold region. The R_{ds}-V_{gs} curve plotted in logarithmic scale [fig. 62] confirms this hypothesis, but does not

11 As expected, subthreshold characteristics is almost unaffected by V_{ds}.
12 In this case should be $V_{sb} = V_{gg}$ but actually depends on which terminal is acting as source in M_{bias}.

allow to extract η, as the simulation is done with $V_{ds} = 0V$[13], so without drain current.

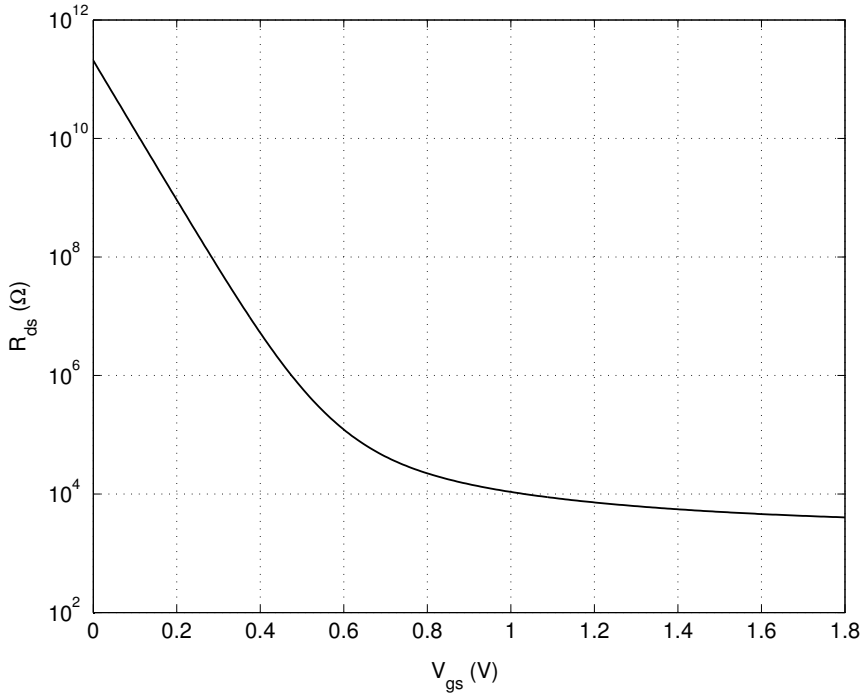

Figure 62: Simulated R_{ds}-V_{gs} characteristics of a $4 \times 2\mu m$ n-MOS transistor like M_{bias}.

5.1.3 Operating point

The operating point of the single pixel cell is simulated. The main purpose of such simulation is to state whether the suggested operating point is a possible circuit state, or in general to identify which operating points can be achieved in the circuit state space. A futher analysis of such operating points will evaluate if the static and dynamic characteristics of the circuit match the desired operating specifications, and possibly highlight the limitations. In the following simulations, real dimensions are considered for the mosfets and realistic parameters are chosen for the leaky elements, so that:

- $\left(\frac{W}{L}\right)_{M_{bias}} = \frac{0.3\mu m}{2\mu m}$ as from design
- $\left(\frac{W}{L}\right)_{M_{sense}} = \frac{1\mu m}{1\mu m}$ as from design
- $R_{leak,ox} = 10G\Omega$[14]

V_{op} value represents the desired value for V_{gg} bias. Increasing V_{ops} value causes the creation of the channel in transistor M_{bias}, thus causing its drain terminal to be brought towards the voltage V_{op}. However, applying LKC at drain terminal allow to see that $I_d = I_{leak,d} - I_{leak,ox}$[15]; in other words drain current has to compensate the sum of those two leakage currents. In practice, M_{bias} voltage drop will depend upon the value of such current, being M_{bias} in weak inversion. Ideally, if electrolyte voltage was trimmed properly, the balance in leakage current could even bring to the condition $V_{gg} = V_{op}$, but this is unlikely

13 This is indeed the most interesting working point to consider.
14 This is a reasonable estimate of the oxide leak resistance, as will be shown afterwards.
15 Neglecting gate leakage current, whose magnitude is found to be far below any other considered here.

to be, being V_{el} dependent on many factors, and above all on electrode or potentiostatic system behaviour[16]. So V_{err} is the error voltage of the electrolyte (i.e. the distance from the V_{op} desired gate voltage). It is expected that, increasing $V_{voltage}$, voltage drop across M_{bias} gets lower, and so V_{gg} is expected to get nearer to the desired bias voltage. More than this, body effect on M_{bias} is expected to dramatically affect threshold voltage.

In [fig. 63] V_{gg} dependance on V_{ops} value is shown, having chosen $V_{op} = 1V$[17] and considering different V_{err} values, both negative and positive. The expected behaviour can be clearly spotted.

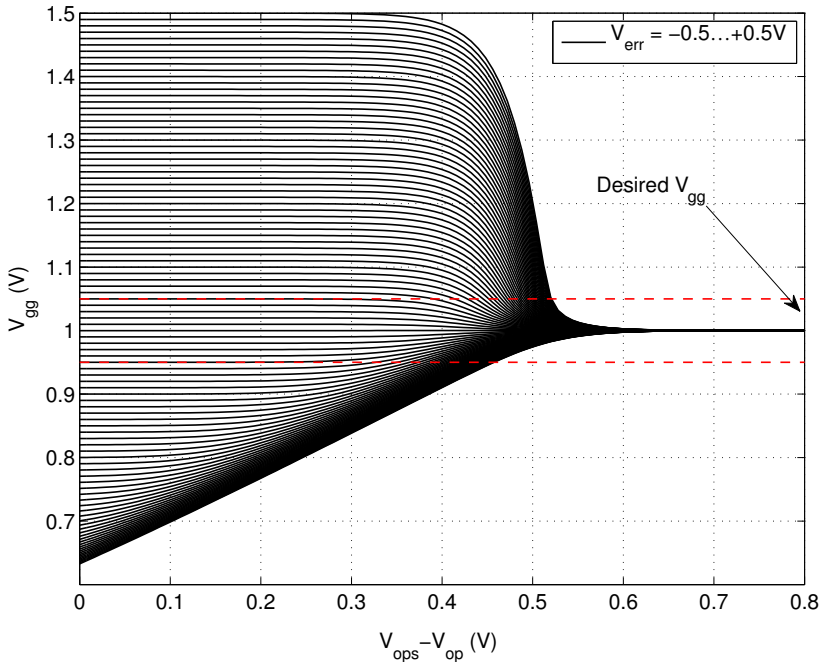

Figure 63: Simulated V_{gg}-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $R_{leak,ox} = 10G\Omega$, $V_{op} = 1V$ and $-0.5V < V_{err} < 0.5V$. Red line represents ±5% of desired value.

Regardless on the value of V_{err}, we met $V_{gg} = V_{op}$ for high V_{ops} drive levels. For almost all values of V_{err} considered, in order to have better than ±5% match between the two voltages, it is necessary to impose $V_{ops} > 1.5V = Vop + 500mV$, which is much higher that the suggested $V_{ops} = Vop + 100mV$..

The same behavior can be seen on the $I_{d,M_{sense}}$ magnitude of the drain current of amplifier transistor which depends obviously on its gate voltage and can be seen also as a desired I_d current magnitude on M_{sense}[18]. Such current, measured in the same condition as before, is shown in [fig. 64].

$$g_m = 2\sqrt{\mu_n K_f I_d} \tag{31}$$

16 As previously discussed and recalled on [Fromherz, 2012]. Moreover sensitivity to this variable is specifically desired to be low.

17 This value is different from $V_{op} = 0.8V$ of suggested bias point. The reason of this choice was both for ease of inspection and for achieving a slightly higher transconductance.

18 Actually, then g_m is bound to that with the square-root law (31), which is far easier to manage than its relationship with V_{gg}.

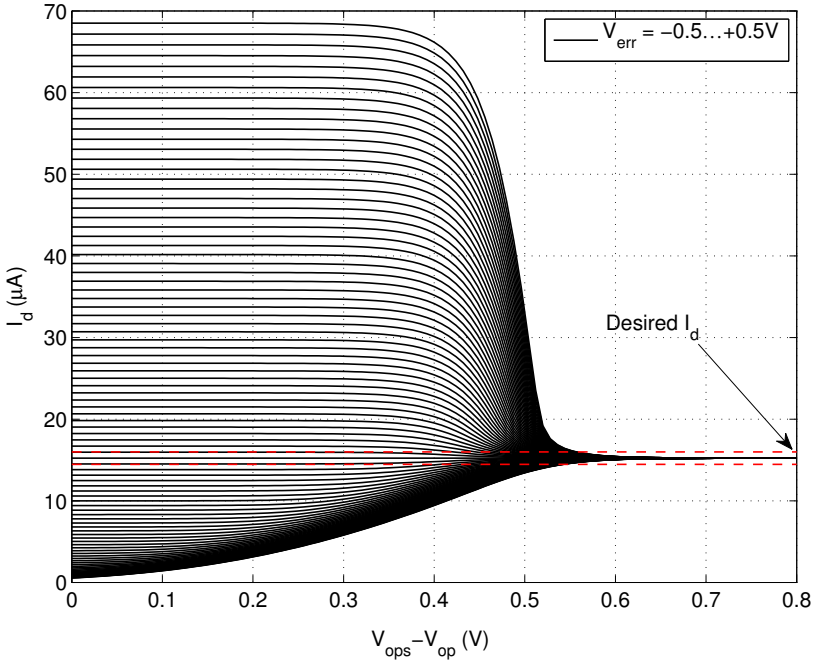

Figure 64: Simulated $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $R_{leak,ox} = 10G\Omega$, $V_{op} = 1V$ and $-0.5V < V_{err} < 0.5V$. Red line represents $\pm 5\%$ of desired value.

The same scenario is evident: in order to match the desired M_{sense} drain current bettern than $\pm 5\%$ in almost all considered conditions, $V_{ops} > V_{op} + 500mV$ is a necessary condition. This boundaries on $I_{d,M_{sense}}$ are even more significant than the boundary on V_{gg}, being g_m easily linked to transistor current.

As first, it is worth to see if this depends on the V_{op} voltage level. This is done by looking at the M_{sense} drain current magnitude when locking $V_{err} = -200mV$ and simulating $I_{d,M_{sense}}$ for different values of V_{op} while changing V_{ops}, and this is shown in [fig. 65].

It is shown that, for $V_{ops} = 0V$, the MOS current is not zero, and this is due to the fact that V_{gg} is biased to a voltage level between V_{op} and $V_{op} + V_{err}$[19] and this causes the current value to be systematically below the desired level, which is reached by increasing V_{ops} and is depicted in the right region of [fig. 64]. Again, it is easy to see that a current bias error of no more than $\pm 5\%$ upon $I_{d,M_{sense}}$ is admitted for any reasonable value of the same, then $V_{ops} > V_{op} + 500mV$ is mandatory.

Finally, it can be investigated how much this depends on the oxide leakage, modelled with $R_{leak,ox}$[20] and how much on the intrinsic device characteristics. For this reason, V_{gg} and $I_{d,M_{sense}}$ values for different values of $R_{leak,ox}$ while varying V_{ops} are shown in [fig. 66] and [fig. 67] respectively[21].

At last, it is clear that the way in which V_{gg} and $I_{d,M_{sense}}$ approach to it final/desired value depends on leakage resistance. Although $R_{leak,ox}$ progression is exponential in the simulations, curves are equally spaced in [fig. 67]. This is due to the fact that also the

19 Provided that $I_{leak,d}$ is not dominating.
20 It has been considered $R_{leak,ox} = 10G\Omega$ until now.
21 It is important to state that, in order to perform such high-impedance affected simulations, simulator parameter g_{min} needed to be carefully handled.

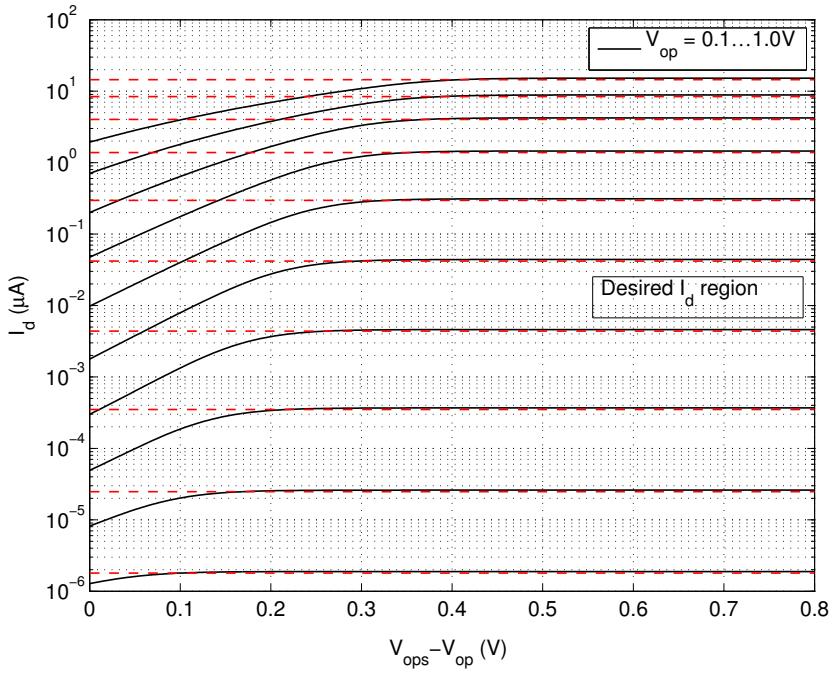

Figure 65: Simulated $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $R_{leak,ox} = 10G\Omega$, $V_{err} = -0.2V$ and $0V < V_{op} < 1V$. Red line represents 95% of desired value.

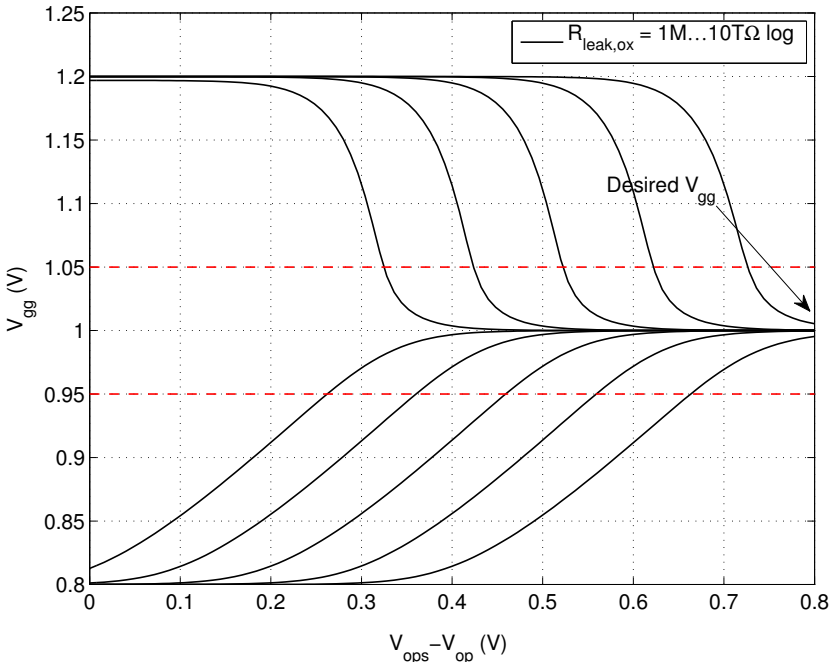

Figure 66: Simulated V_{gg}-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $V_{err} = +0.2/-0.2V$, $V_{op} = 1V$ and $R_{leak,ox} = 1M\ldots10T\Omega$ in exponential progression. Red line represents $\pm5\%$ of desired value.

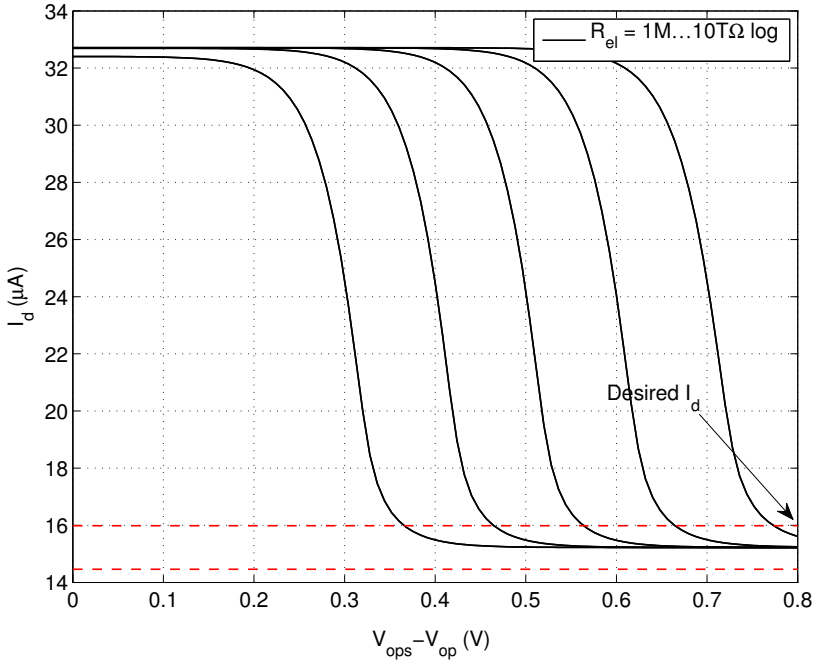

Figure 67: Simulated $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $V_{err} = +0.2V$, $V_{op} = 1V$ and $R_{leak,ox} = 1M \ldots 10T\Omega$ in exponential progression. Being chosen a positive value for V_{err}, M_{sense} is biased even with $V_{ops} = 0V$.

dependance of M_{bias} current on V_{ops} voltage is actually exponential. Remembering the $V_{ops} > V_{op} + 500mV$ condition extracted before and not wanting to further restrict it, keeping a little left with respect to the middle curve seem anyway to cause a quite acceptable error, with no more than $|V_{err}| < 200mV$ in absolute value. This condition gets traduced in $R_{leak,ox} > 10G\Omega$ which justifies the previous evaluations[22].

The main limitation caused by the need to keep $V_{ops} > V_{op} + 500mV$ is given by the lowering of the small-signal output impedance of M_{bias}, which is responsible of lowering the input impedance at M_{sense} gate and thus possibly killing the input signal. From figure

5.1.4 AC Parameters extraction

M_{bias} drain capacitance $C_{dd} = C_{gd} + C_{db}$[23] and M_{sense} input capacitance[24] are both connected to V_{gg}, so they play a major role in determining input bandwidth and gain. It's fundamental to note that, being the device biased with fixed voltages, no Miller effect is affecting the input capacitance. C_{gg} is expected to be dominant and its value is represented in [fig. 68] in function of V_{gg}. Although calculations of other contributes was performed from technology data, the safe value of $C_{gg} = 10fF$ was considered to be the total maximum intrinsic capacitance value at V_{gg} node in every bias condition.

Transit frequency of M_{sense} transistor, despite being a known AC parameter, is not investigated in this context, because it is believed not to be an input bandwidth limiting factor

22 This analysis is actually unnecessary, but it shows nice details on the behaviour with different leakage resistor values.

23 C_{gd} is considered in the drain capacitance because gate voltage is actually connected to small-signal ground.

24 Intended as $C_{gg} = C_{gs} + C_{gd} + C_{gb}$.

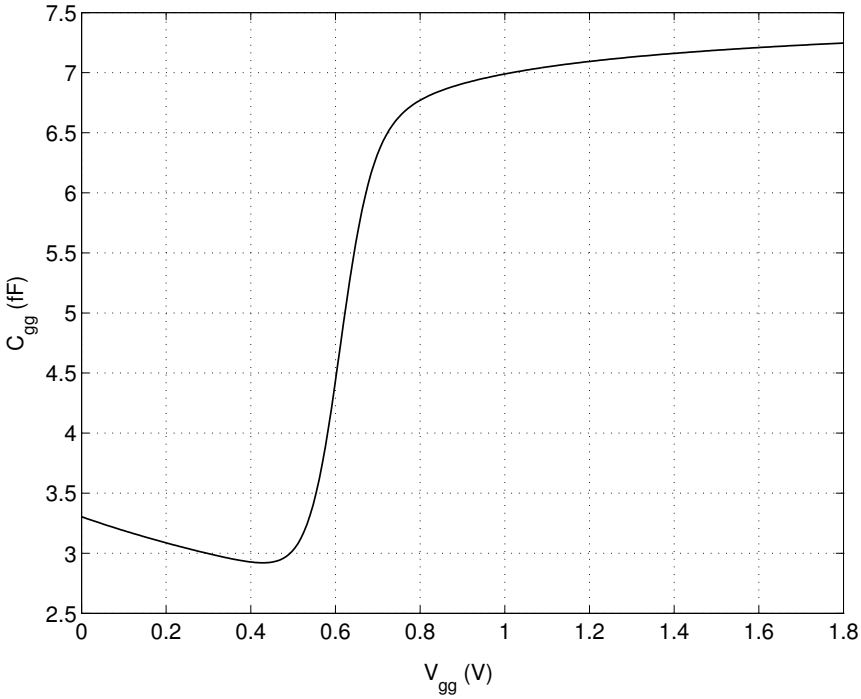

Figure 68: Simulated C_{gg}-V_{gg} characteristics of a single pixel cell, with $V_{op} = 1V$. Note rapid capacitance variation at $Vth \approx 0.65V$ due to population inversion.

at all[25]. Actually, from extracted parameters, it can be estimated with (32), considering $g_m \geqslant 40\mu S$ from [fig. 60].

$$f_{T,M_{sense}} \geqslant \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \approx \frac{g_m}{2\pi C_{gs}} = 630MHz \tag{32}$$

M_{bias} output impedance magnitude within input bandwidth[26] is shown in [fig. 69]. For $V_{ops} > V_{op} + 500mV$, it is $|Z_{out,M_{bias}}| < 850M\Omega$. Although phase being not shown, impedance is pretty resisitive as expected.

5.1.5 Bandwidth and input impedance

For evaluating small-signal AC characteristics of the circuit, the circuit model complete with reactive elements is shown in [fig. 70] and is reduced to the small-signal model in [fig. 71]. The extrinsic capacitance C_{el} was added and represents the electrode-to-electrolyte capacitance. The local potential source is represented by v_{el}, on which no load effect is considered by now.

The input transfer function shown in (33) is clearly high pass, and the gain is determined by the capacitive voltage divider made by C_{el} and C_{gg}.

$$W_{in}(j\omega) = \frac{R_{out,M_{sense}}\left(1+sC_{el}R_{leak,ox}\right)}{R_{out,M_{sense}}+R_{leak,ox}+s^2R_{out,M_{sense}}R_{leak,ox}\left(C_{el}+C_{gg}\right)} \tag{33}$$

25 Actually, input bandwidth will be proven to be limited almost totally by passive parasitic elements upstream of the transistor gate.

26 Which is impedance seen from V_{node} simulated @1kHz.

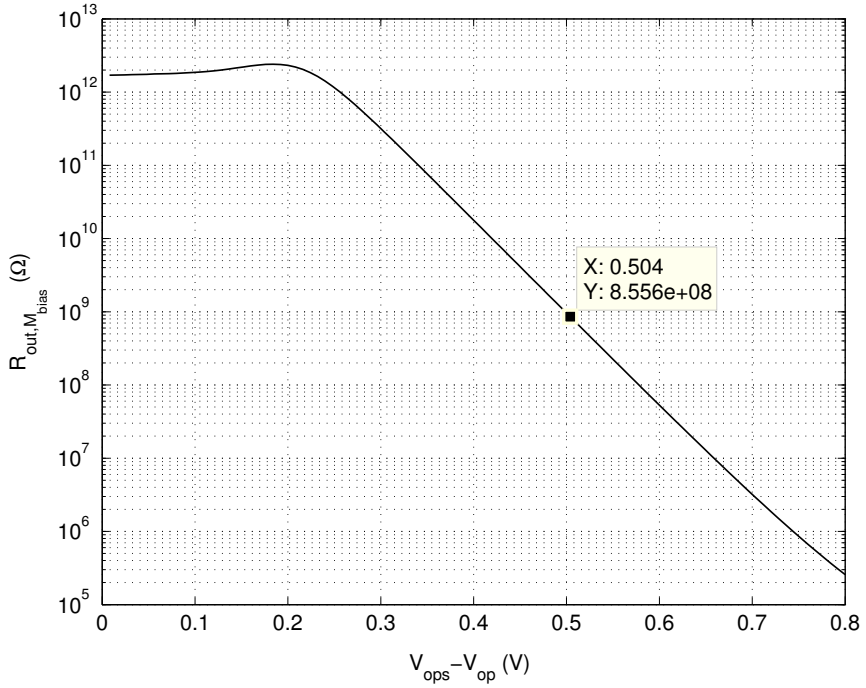

Figure 69: Simulated $Z_{out,M_{bias}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $V_{op} = 1V$.

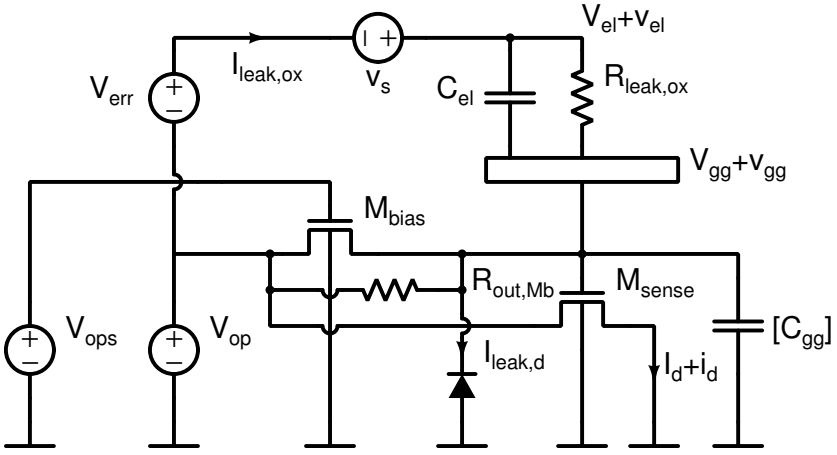

Figure 70: AC model for the single pixel cell.

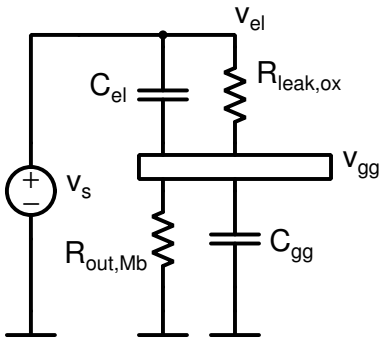

Figure 71: Small-signal model for the single pixel cell.

$$W_{in}(j\omega) \approx \frac{1 + sC_{gg}R_{out,M_{sense}}}{1 + s\left(C_{gg} + C_{el}\right)R_{out,M_{sense}}} \tag{34}$$

in which $R_{leak,ox}$ is supposed to be negligible in fiat approximation due to the fact that it is orders of magnitude higher than $R_{out,M_{sense}}$. In-band gain is then shown in (35), from which it is clear that a minimum capacitor ratio is fundamental to have a robust SNR at M_{sense} input[27].

$$W_{in}(j\omega)|_{w\in B} \approx \frac{C_{gg}}{C_{gg} + C_{el}} \tag{35}$$

Ideal case is that with $C_{el} \to \infty$, and $W_{in}(j\omega)|_{w\in B} = 0dB$. In order to have no more than 10% attenuation with respect to ideal case, $\frac{C_{el}}{C_{gg}} > 15$ is chosen, leading to a minimum value of $C_{el} > 150fF$[28]. This allows to evaluate the lower cut-off frequency for the high-pass transfer function in (36), considering $R_{out,Mbias} \approx 850M\Omega$ at $V_{ops} = V_{op} + 500mV$.

$$f_{c,low} = \frac{1}{2\pi R_{out,Mbias}C_{el}} \approx 1.25kHz \tag{36}$$

This value is obviously too high with respect to the discussed requirements. Low frequency response simulation in [fig. 72] confirms the cut-off frequency estimation. High frequency response is not even discussed, because it is affected by many more limiting factors that the integrated circuit section. Above all, the capacitive coupling C_{el}, which is nonlinear and heavily frequency dependent, which will be discussed later. Even scan rate limitations and interconnection-related issues contribute to limit the overall system bandwidth. From the specifications, frequency response up to 10kHz is considered to be satisfactory.

As the lower cut-off frequency is clearly too high, it is fundamental to understand which parameters can be changed in order to bring it down. Two actions can be taken at first analysis:

- Increase electrode coupling with signal source, which means increasing C_{el}. Being capacitor area limited, this would mean either changing the dielectric matherial or lowering its thickness, with the major drawback of increasing leakage current, so taking V_{gg} out of correct bias.

27 This is for mitigating the transistor noise contribute, and of course resistive and oxide noises still need to be separate considered.

28 This will then become a design constraint for the device.

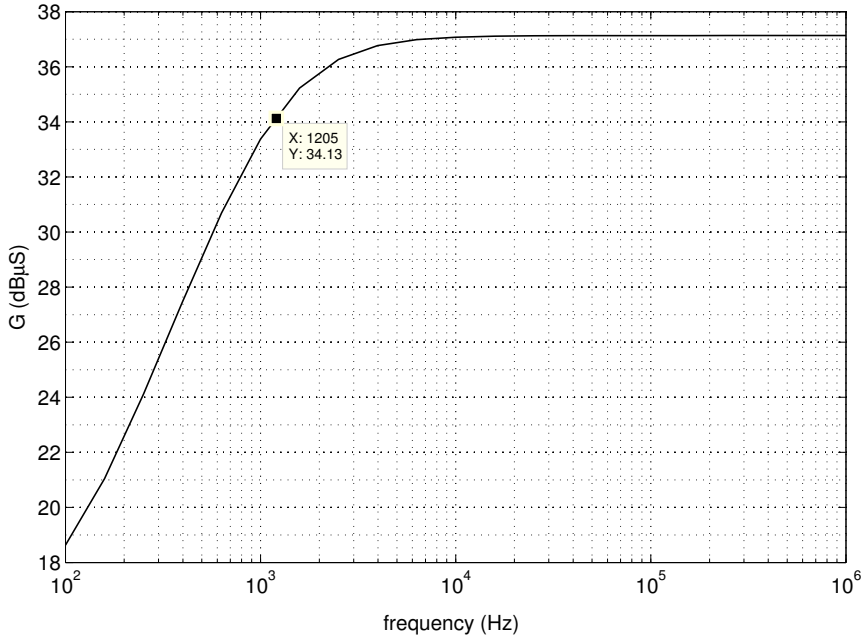

Figure 72: Frequency transimpedance response for the single pixel cell, with $V_{op} = 1V, V_{ops} = V_{op} + 500mV$ Being defined $G(j\omega) = \frac{I_d(j\omega)}{V_s(j\omega)}$, measurement unit is dBμS.

- Decreasing the value of M_{bias} output resistance by lowering V_{op} voltage. Again, this means causing a bigger error on V_{gg} bias. It can be seen from [fig. 69] that impedance increases of a decade roughly every 80mV. By inspection, in order to decrease pole frequency of two decades, $V_{ops} \approx V_{op} + 340mV$ should be chosen. Frequency response for different V_{ops} values is shown in [fig. 73].

It is clear that a compromise between the two actions must be found. This point will be investigate in depth after characterization.

5.1.6 Noise analysis

Finally, noise analysis is discussed. Input noise source is considered at small-signal node voltage v_{gg}, to that to exclude contributions due to electrode-electrolyte interface that will be discussed separate. Noise output is taken at $i_{d,M_{sense}}$ amplifier transistor current. Output noise is shown in [fig. 74], whereas input-referred noise is shown in [fig. 75], with reference to the widely-discussed bias condition and zeroed input signal.

The power spectral density of current noise is known to be made by the two components highlighted in (37), which are thermal noise and flicker noise, respectively.

$$\frac{\bar{i}_n^2}{\Delta f} = \frac{\bar{i}_{n,Th}^2}{\Delta f} + \frac{\bar{i}_{n,1/f}^2}{\Delta f} \tag{37}$$

which are given by the expressions in (38)

$$\frac{\bar{i}_n^2}{\Delta f} = 4k_B T \frac{\gamma}{\alpha} g_{mt}{}^{29} + \frac{k_F I_d}{L^2 C_{ox}} \cdot \frac{1}{f} \tag{38}$$

29 Let be $g_{mt} = g_m + g_{ds} + g_{mb}$. Among the operating points here discussed, $g_m \approx g_{mt}$.

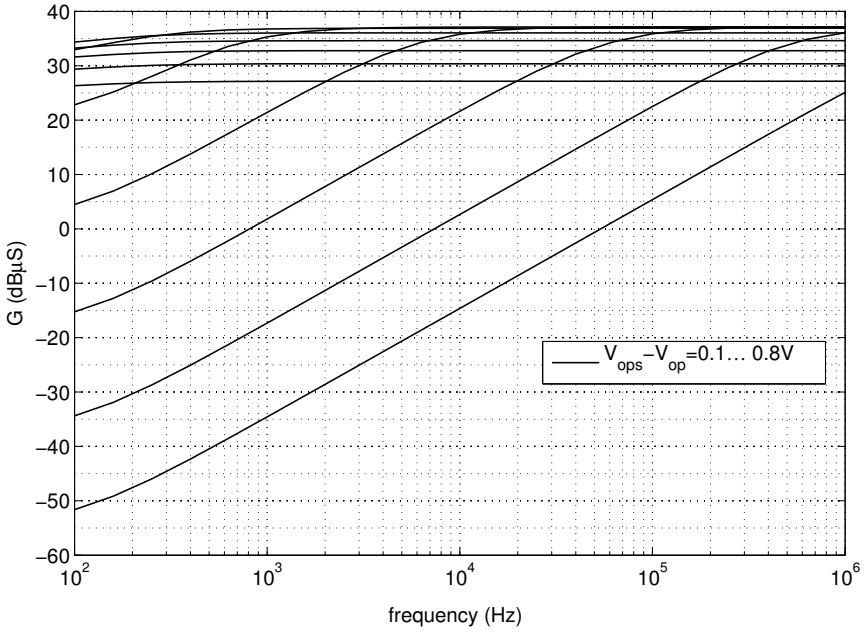

Figure 73: Frequency transimpedance response for the single pixel cell, with $V_{op} = 1V, V_{ops} = V_{op} + 500mV$ Being defined $G(j\omega) = \frac{I_d(j\omega)}{V_s(j\omega)}$, measurement unit is dBμS.

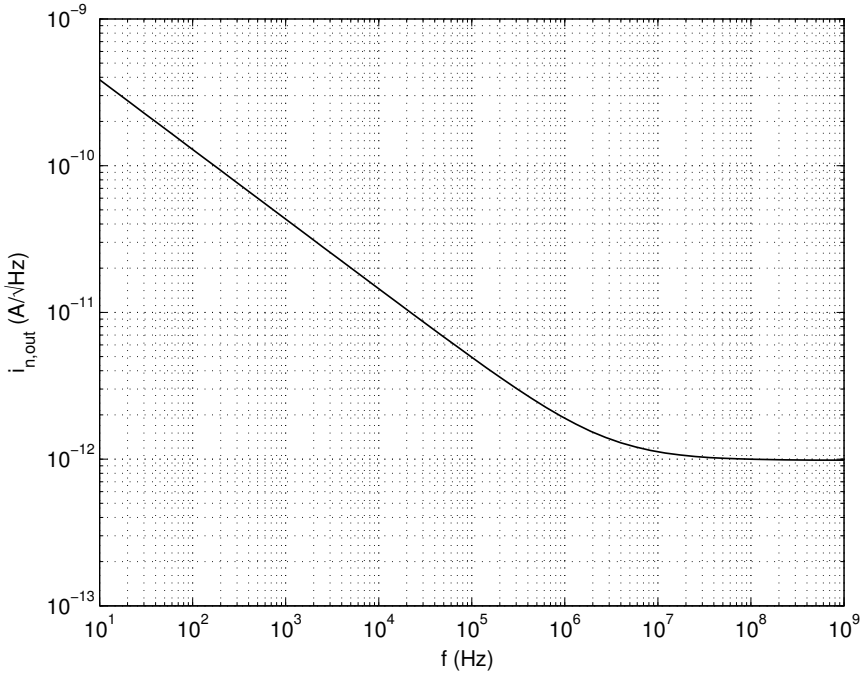

Figure 74: Square root of power spectral density of output current signal $i_{d,M_{sense}}$ with short-circuited input and $V_{op} = 1V$, $V_{ops} = V_{op} + 500mV$.

as can be seen from the spectral plots, flicker noise is dominant over the whole input signal bandwidth. This is because the corner frequency, expressed by (39) is over 2MHz.

$$f_{CO} = \frac{k_F}{4k_B T \frac{\gamma}{\alpha} L^2} \cdot \left(\frac{g_{mt}}{I_d}\right)^{-1} \tag{39}$$

Current noise, integrate by simulator postprocessing over the bandwidth $B = 10Hz \ldots 10kHz$ is $\bar{i}_n = 1.83nArms$ for the complete cell. As could be expected, simulation confirms that M_{bias} contributes less than 1% to total noise buildup.

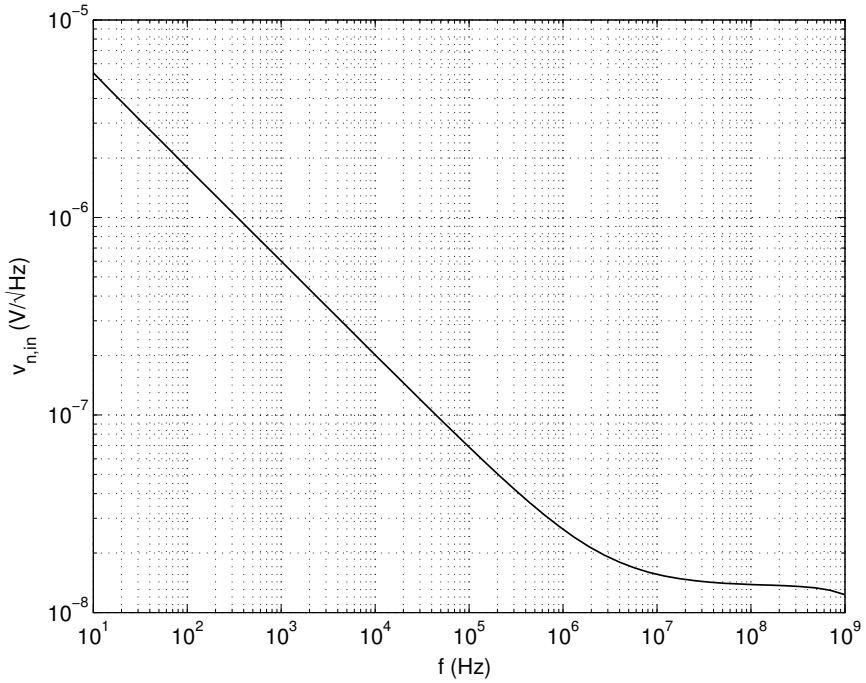

Figure 75: Square root of power spectral density of output current signal $i_{d,M_{sense}}$ with short-circuited input and $V_{op} = 1V$, $V_{ops} = V_{op} + 500mV$, referred to the input voltage v_{gg}.

When referred to the input node V_{gg}, the voltage noise is roughly:

$$\bar{v}_{n,in} = \frac{\bar{i}_{n,out}}{g_m} \approx 50\mu Vrms \tag{40}$$

which gives a nearly perfect approximation of the simulator postprocessing results.

With the hypothesis that flicker noise is dominating our process, it is clear from (38) that output noise depends on bias condition with a square law. However, input noise is explicited by substituting (38) in (40), giving (41), recalling (31).

$$\frac{\bar{v}^2_{n,in}}{\Delta f} \approx \frac{\bar{i}^2_{n,1/f}}{\Delta f} \cdot \frac{1}{g^2_m} = \frac{k_F}{4L^2 C_{ox} \mu_n K_f} \cdot \frac{1}{f} \tag{41}$$

This means that input noise is almost insensitive to bias condition[30], as it is shown in [fig. 76].Of course, corner frequency is expected to chage. This means that a variation of gate voltage is not effective in helping to reduce consistently input noise level[31], but can be considered in case:

30 Provided that the transistor is always in saturation region.

31 As long as transistor remains in the same bias region and corner frequency is over the input band.

- the amplifier stage downstream the transistor has a bad noise figure, so that increasing signal gain on input stage helps to improve overall SNR, or
- the nonlinear behaviour of electrode-to-electrolyte coupling capacitor C_{el} exhibits different noise levels at different bias voltages.

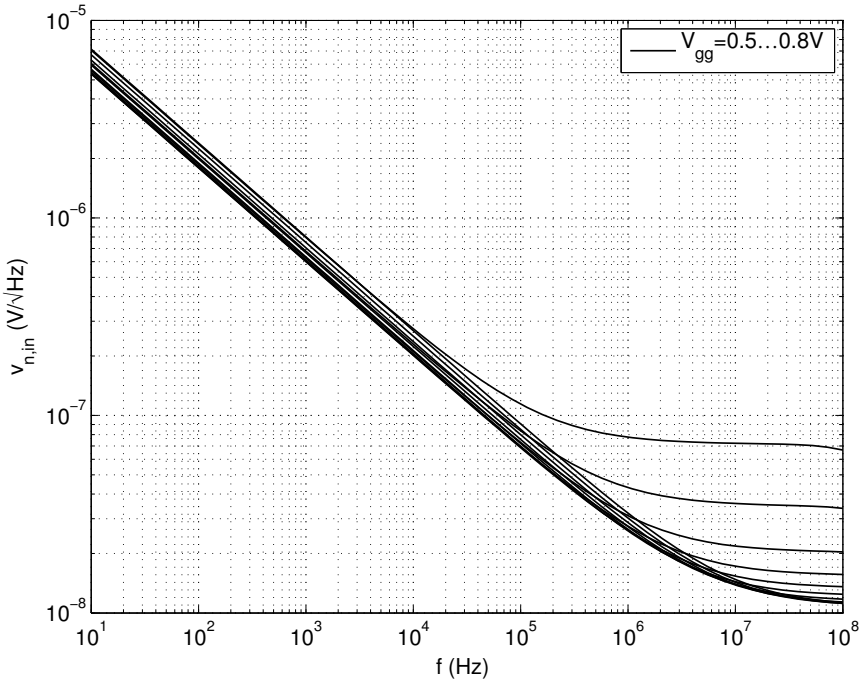

Figure 76: Square root of power spectral density of output current signal $i_{d,M_{sense}}$ with short-circuited input and $V_{op} = 1V$, $V_{ops} = V_{op} + 500mV$, referred to the input voltage v_{gg}.

But (41) also shows that input noise level is decimated by the square power of L. Considering the layout constraints, a reasonable upper bound for L could be $L \leqslant 5\mu m$. Although we could expect a noise scaling by a factor 25, simulation forecasts an input noise level of $\bar{v}_{n,in} = 6\mu Vrms$ which is still a good improvement, with the only major drawback of an increased C_{gg}.

5.2 OXIDE PERFORMANCE CONSIDERATIONS

From the simulations, it is clear that a partial contribute to the non ideal behaviour is given by intrinsic parasitics of the circuit itself, not mitigated by good design choices. The remaining contribute is due to non-ideality of the oxide, whose leakage resistance can dramatically worsen the situation. As it is shown, on one hand, the leakage current would lead to increase the driving level of M_{bias} so that to impose the correct bias, on the other hand this impacts terribly on the frequency response. So the upcoming question is what should be the target characteristics of the dielectric material. It will be pretty clear from literature and from further characterisation that it is unlikely the possibility to increase electrode capacitance, as the dielectric constant of TiO_2 is one of the highest among this type of materials. So, that represents the target value. For what concerns the leakage resistance, evaluating from simulations a reasonable target value should be in the $10T\Omega$ range, with which value it could be possible to lower the V_{ops} value near to $V_{op} + 350mV$ without committing too much error. Considering a maximum voltage drop at the dielectric of 1V, this is translated in currents in

the pA range, and (considering a gate surface of $10 \times 10\mu m = 100\mu m^2$, current densities in the $\mu A/cm^2$ range, which is slightly under the considered limit for tissue damage. It might also be that a lower dielectric constant material could fit the application still well, provided that the leakage resistance is so much better than that of TiO_2 so that the cut-off frequency - which is in the end our main concern within this issue - overall decreases.

5.3 STATIC DEVICE CHARACTERISATION

The device characteristics are now measured and verified for compliance with the simulations. There are many limitation in the characterisation of the device, due to physical impossibility to access to individual devices or measure isolated parasitic contributes. Such verification can be used, however, to validate simulation results when they refer to a non-observable parameter. Note that N-channel needles only are considered for the following characterisation activity.

5.3.1 Breakout board and acquisition system

A breakout board, shown in [fig. 78], was designed to connect instrumentation to the needle chip. As it is known, the chip is provided with a Molex Pico-Clasp 40-pin male board connector. The breakout board allows to select a single FET to be tested. It is provided with the same connector, and a parallel cable is made[32]. The board is designed to have four bias voltages with respect to its ground. This is because the majority of parameter analyser instruments have 4 SMUs available. Dip-switches are available[33] at each row and column line in order to select or de-select it according to the second type biasing strategy discussed. So, it is chosen $V_{drain} = 0V$ and $V_{source} = V_{sub}$ so that only the four lines $V_{row}, V_{sub}, V_{op}, V_{ops}$ are coming out of the board. Of course, only one row - the selected one - is connected to the amplifier, the remaining ones are just directly connected to V_{drain} without being connected to the amplifier. This can be done, similarly to the columns, because it is actually $V_{drain} = 0$ so the dip-switch line is just connected to the ground. A scheme of the bias strategy scaled to this particular case is shown in [fig. 77] and a photo of the board is on [fig. **??**]. The board is connected dot the instrumentation with a DB25 male connector[34]. A board that allowed column switching by mens of an external reed-relay multiplexer was also designed and used, but this is beyond the purpose of this chapter.

This design has many limitations, such as the fact that recording an $I_d - V_d$ characteristics is not a matter of independently sweeping two lines but performing a more complex sweep involving V_{sub} and V_{op} in a combined way. This is because the bias voltage of the current sensing amplifier cannot be moved from the V_{drain} voltage, otherwise other undesired FETs in other lined would turn on. A separate second source for V_{drain} voltage would be need, but, again, the SMU number was wanted to be no more than 4.
The board is connected to a 4-SMU Agilent Technologies 4156C Parameter Analyzer through opportune three-axial to bi-axial connector adapters and then a custom cable is realised to connect to the DB25 board connector. The parameter analyser is used to The sensor is kept as much as possible surrounded by a metal housing in order to make a first attempt of EMI rejection.
Despite being the actual driven voltages being referenced to V_{drain} instead of V_{sub}, the characterisations will always be exposed with reference to $V_{sub} = 0V$, matching the commonly-

32 Actually, the cable is not perfectly parallel, many lines are rearranged to achieve a logical organisation
33 Dip-switches are duplicated for each line, to provide the selection of two alternative paths instead of only an ON-OFF connection.
34 Which was chosen because it is a standard used by National Instrument, whose instrumentation has been used too with this board.

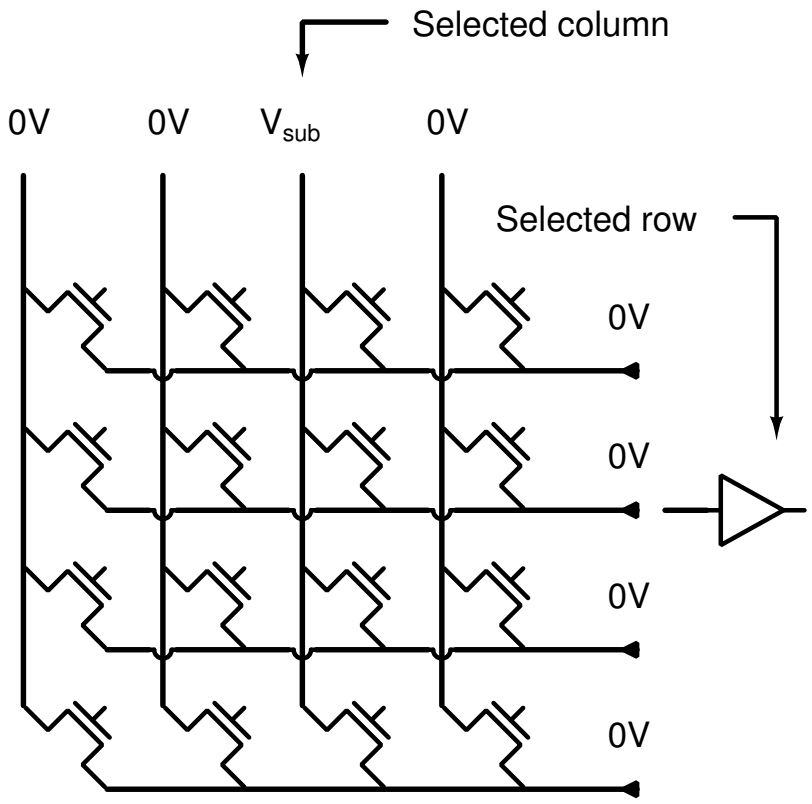

Figure 77: Example of alternative bias strategy for addressing a single column of the matrix (expected current verse for n-MOS devices is shown).

accepted curve plots.

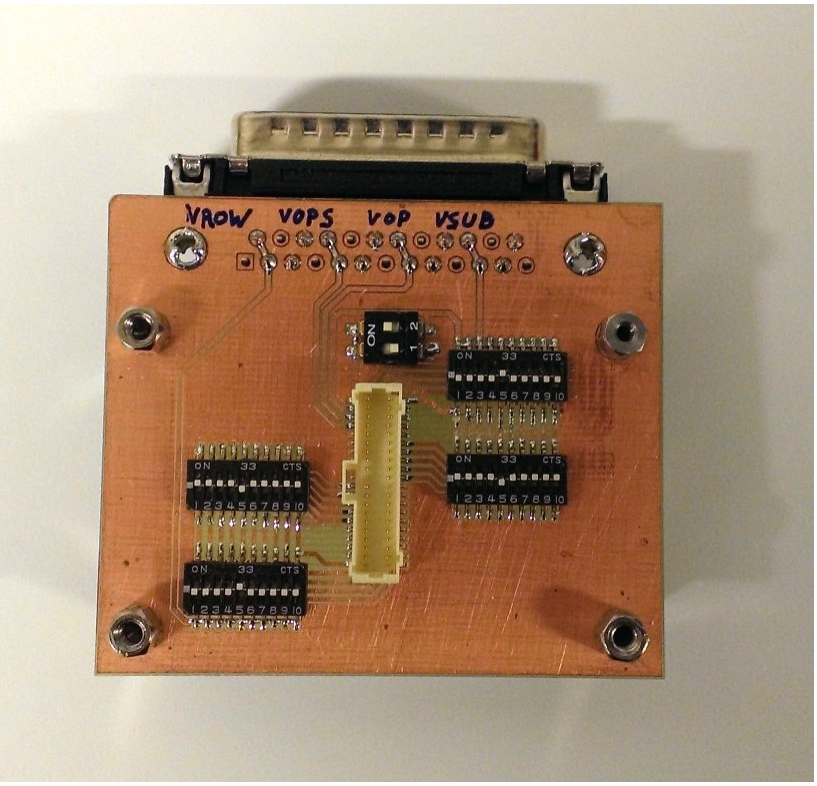

Figure 78: Custom made breakout board for device interfacing with external amplifier, with single device manual addressing though dip-switches.

5.3.2 Input characteristics

The input characteristics of the device was measured. This is done by turning on well[35] the M_{bias} transistor and varying the V_{op} in order to control the gate bias of M*sense*. By having the M_{bias} in a very low on-resistance state, although leak mechanism will for surely affect the system (and they will be later evaluated) there is a good confidence that $V_{g,M_{sense}} = V_{op}$.

GROUNDED-GATE OPERATION Relevant leakage between top recording gate electrode and electrolyte is expected. As it will be further explained in the next chapter specifically for *in-vivo* recording, the strategy to mitigate this issue is to bring the electrolyte voltage as close as possible to the expected gate bias voltage, possibly accounting for the half cell potential of using a potentiostatic control. For in-electrolyte needle characterisation, this strategy is applied. However, it was easier to set reference Ag/AgCl electrode to ground and translate all other voltages accordingly. In particular, desired gate voltage V_{op} will be set to ground too and substrate and source voltage for N-channel devices will be negative.

EXPERIMENT SETUP Needle no. 0177 is used for this experiment. The needle is connected to the breakout board and a random FET address is chosen. The DB25 connector of the breakout board is connected, through an adapter, to the SMU terminals of the 4156C Parameter Analyzer, which is computer controlled though GPIB-over-USB interface. In order

35 Which is a short for letting the FET in strong inversion.

to minimised EMC issues or light sensitivity[36], the chip is then inserted in a aluminium box connected to ground in which cables have connectors or windows to pass through the box wall. V_{op} is kept at ground, while, $V_{ops} = 1V$ and the substrate voltage V_{sub} is swept between 0 and -1.8V. In this case, row 5 and column 5 were selected, so for short data will be referred to $M_{sense(5,5)}$.

METHODS Device is biased with the parameter analyser and appropriate sweeps are executed.

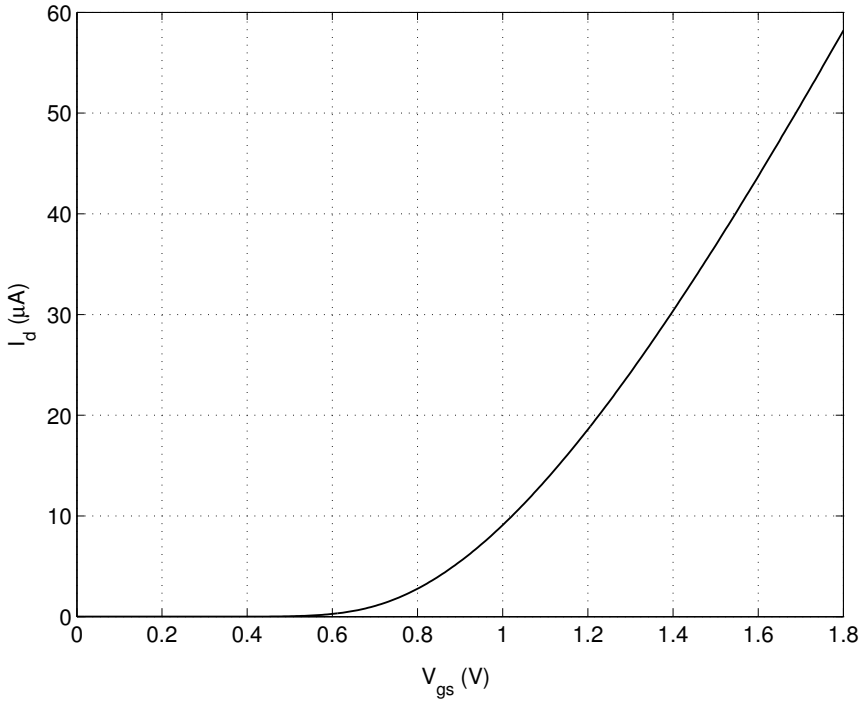

Figure 79: Measured I_d-V_{gs} characteristics of $M_{sense(5,5)}$ with $V_{ds} = V_{gs}$.

RESULTS Unfortunately, the I_d-V_{gs} curve cannot be linearly interpolated to obtain threshold voltage, ad any of the threshold voltage recovery methods based on I_d-V_{gs} require very low V_{ds} very low (e.g. 10-100mV) [Ortiz-Conde *et al.*, 2002] in order to make constant term of (25) negligible.

Interpolating the square root of drain current with reference to (26), $K_f = 74.6\mu A/V^2$ is obtained. By interpolating the curve at the maximum slope point, $V_t = 0.55V$ is found. Both those values are somewhat different from the simulated ones, and in particular K_f. The reasons for this mismatch ($\approx$ 50% in the case of V_t) are still being investigated, and as of now there are two hypotheses:

- a bias error on gate voltage of M_{bias}, resulting in lower real gate bias and so transonductance;
- current loss in other structures of the matrix, or in some matrix devices that could be active despite their $V_{gs} = V_{ds}$.

36 Even if no relevant light sensitivity of such devices was ever measured.

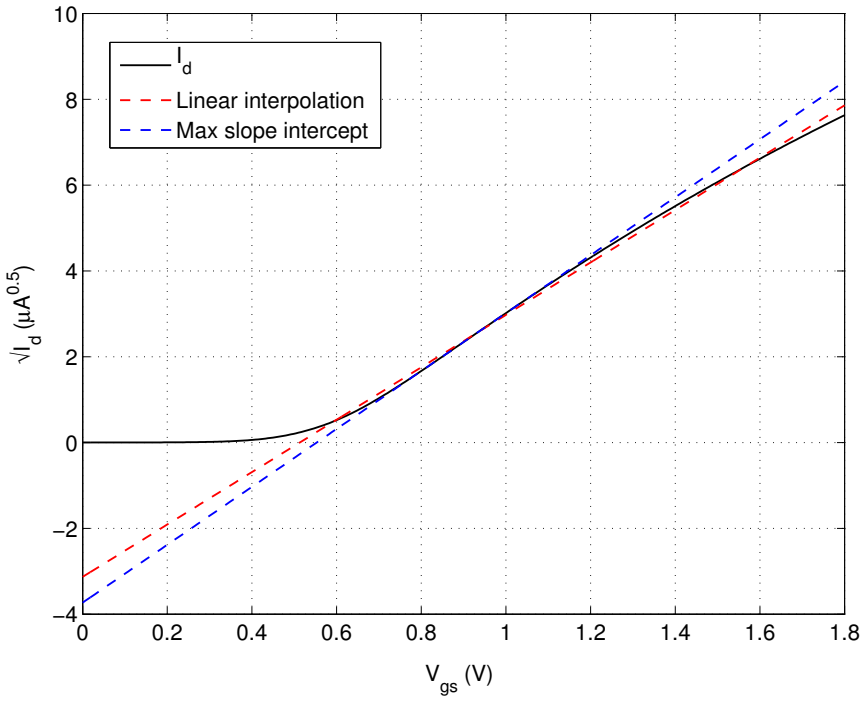

Figure 80: Measured square root I_d-V_{gs} characteristics of $M_{sense(5,5)}$ with $V_{ds} = V_{gs}$. Linear interpolation of the second part of the curve and linear interpolation at maximum slope point are shown.

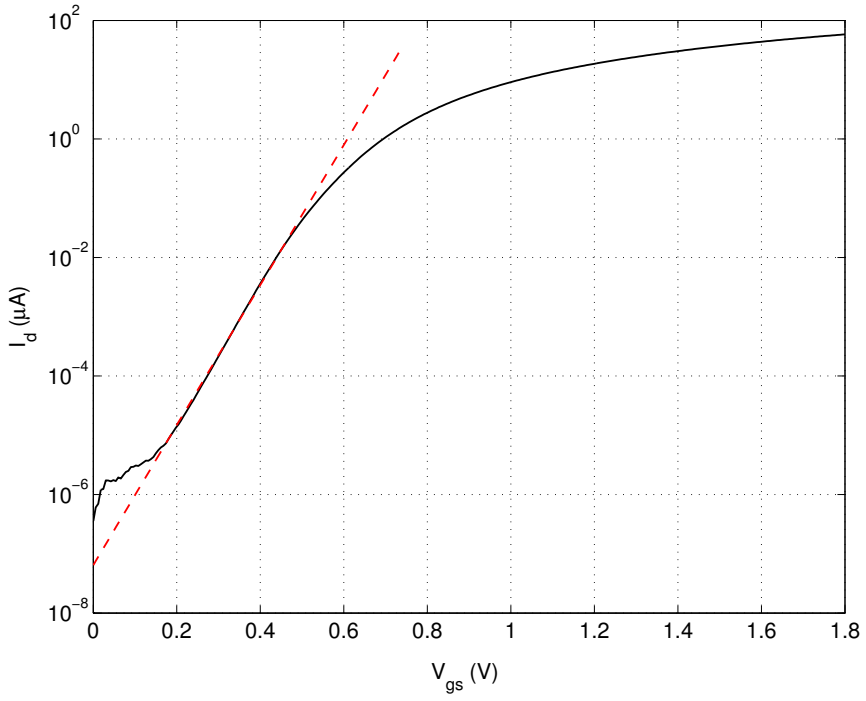

Figure 81: Measured I_d-V_{gs} characteristics of $M_{sense(5,5)}$ with $V_{ds} = V_{gs}$. Subthreshold slope is interpolated and shown.

By interpolating the curve in the subthreshold interval, $S_{s-th} = 84.6 mV/dec$ is found, which is a good match with simulations ($\approx 10\%$). Transconductance in *diode-like* configuration[37] is shown in [fig. 82].

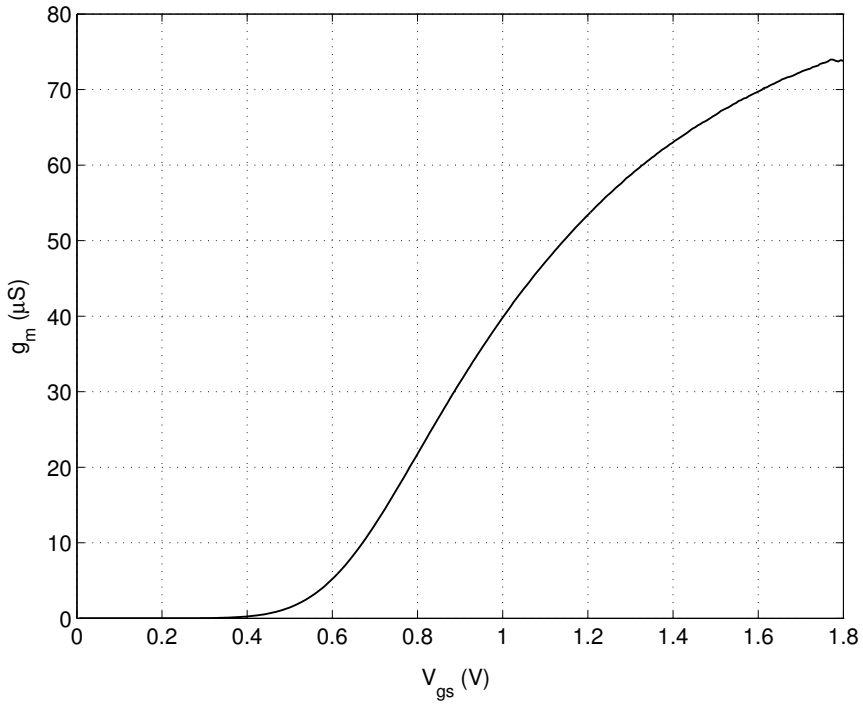

Figure 82: Measured g_m-V_{gs} characteristics of $M_{sense(5,5)}$ with $V_{ds} = V_{gs}$.

5.3.3 Mismatch

Good matching between matrix array FETs is very important for at least a couple of reasons. First of all, this assures similar SNR characteristics at the different recording sites. Lastly, this represent the minimum *dynamic* that an AC-coupled transimpedance readout amplifier should have when multiplexing is active, in order not to saturate in any case. In fact, as different FETs will generally have a different DC bias point current value, when different column is selected, the row current signal will exhibit a yep jump of the corresponding difference of drain currents ΔI_d of the two transistors at adjacent columns. If we suppose that, by means either of DC value trimming of AC coupling, the DC bias value is out of the ADC system range, the maximum step of ΔI_d must be within it, so amplifier will not saturate. The reason for investigating the mismatch so much in depth is that this parameter was a real issue with C-100-A/EOSFET devices.

EXPERIMENT SETUP Needle no. 0177 is used for this experiment. Setup is exactly the same of input characteristics measurements.

METHODS A column (5) and a row (5) are randomly chosen. An input characteristic is measured for each transistor in a row and for each transistor in a column, and a map of the characterised FETs is shown in [fig. 83]. The characteristic of all FETs is plotted in linear scale to verify matching of K_f and threshold voltage V_t. Then the same is plotted in logarithmic scale to estimate mismatch of subthreshold slope S_{th}. Finally, the mismatch in drain

37 Which guarantees saturation condition.

current at maximum gate voltage is evaluated, and this allows to estimate the minimum dynamics of the readout amplifier. The measurement pattern allows to have information on matching spanned in two orthogonal directions.

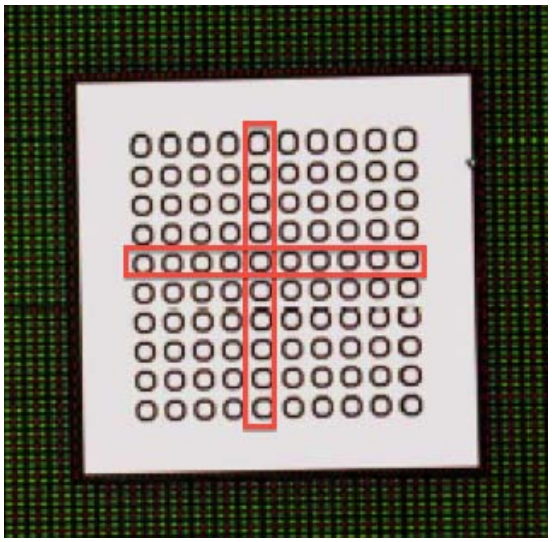

Figure 83: Pattern of characterised devices for mismatch evaluation.

RESULTS The envelope of the 20 curves of input characteristics is shown in [fig. 84] and [fig. 85]. By inspection, the nice matching between row and column transistor can be spotted.

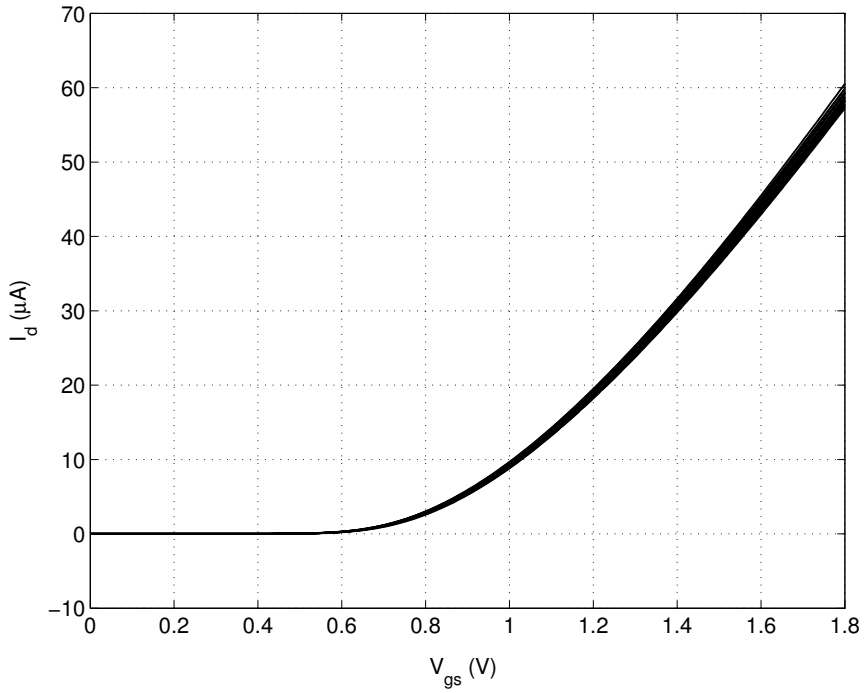

Figure 84: Measured I_d-V_{gs} characteristics of $M_{sense(j,k)}$ with $V_{ds} = V_{gs}$.

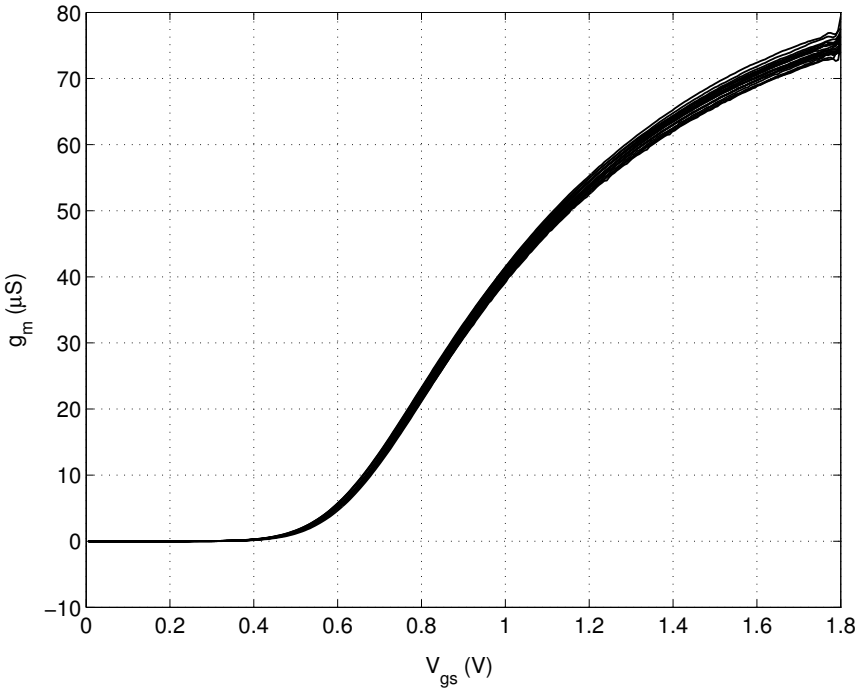

Figure 85: Measured g_m-V_{gs} characteristics of $M_{sense(j,k)}$ with $V_{ds} = V_{gs}$.

The square-root and subthreshold input characteristics are shown in [fig. 86] and [fig. 87] from which single K_f, V_t and $S_{s\text{-}th}$ are obtained.

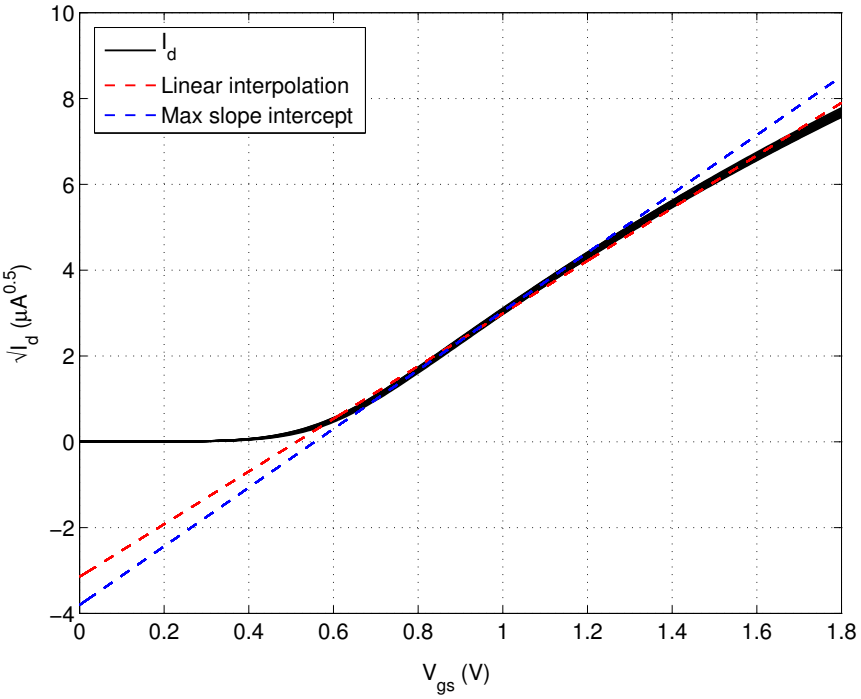

Figure 86: Measured square root I_d-V_{gs} characteristics of $M_{sense(j,k)}$ with $V_{ds} = V_{gs}$. Linear interpolation of the second part of the average curve and linear interpolation at maximum slope point are shown.

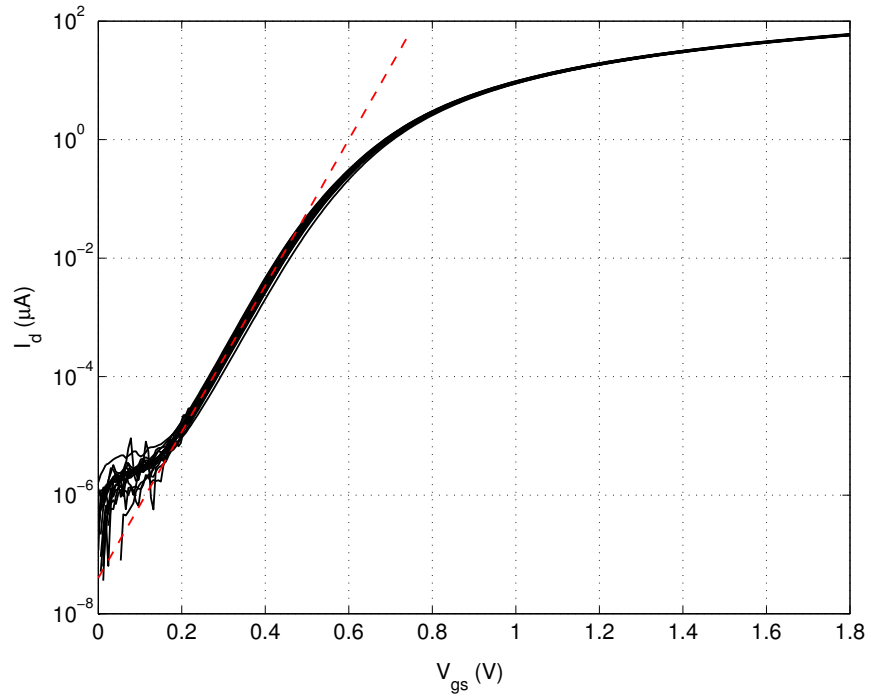

Figure 87: Measured I_d-V_{gs} characteristics of $M_{sense(5,5)}$ with $V_{ds} = V_{gs}$. Average subthreshold slope is interpolated and shown.

Mean values and variances of extracted parameters are shown in [tab. 6].

Table 6: Extracted parameters from 20 transistors to evaluate mismatch

Parameter	μ	σ
S_{s-th}	85.1mV/dec	1.7mV/dec
K_f	75μA/V^2	0.24μA/V^2
V_{th}	0.556V	1.1mV

As previously spotted, the matching between measurements and simulations can be summarised in:

- $S_{s\text{-}th}$ has a very good match ($\approx$ 10%) with simulations;
- K_f has a very bad match ($\approx$ 100%) with simulations. Obvious reason cannot be found for this, however the hypothesis of a leakage somewhere in the device, or a difference between design size and realisation size of the active area of the device are reasonable and must be tested;
- V_t has a bad match ($\approx$ 20%) with simulations, but the author is aware that this is probably the most difficult parameter to properly extract. So further analysis with different curve types must be done.

It must be noted that difference between simulated and measured values is much bigger than estimated variance.

The stochastic distribution of K_f is shown in [fig. 88]. It clearly seems that two values of K_f are mostly frequent, which is not very common for this semiconductor parameter. So, further analysis is done by plotting the series of K_f distinguishing between row and column

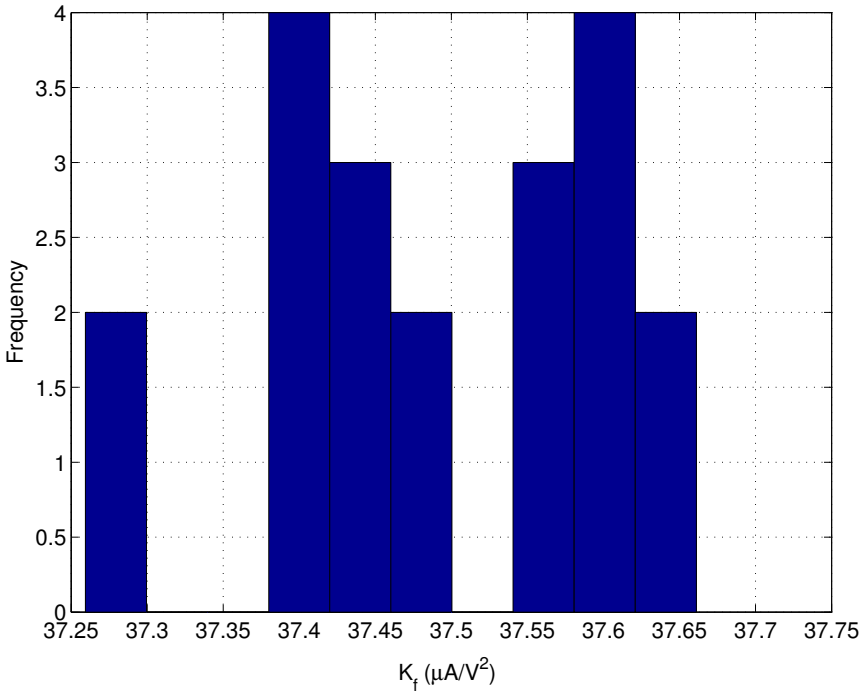

Figure 88: Histogram showing distribution of the different measured K_f parameter values.

in [fig. 89]. A systematic error is clear for the following reasons: first of all, the row K_f values are always higher than the column ones; secondly, K_f measured for $M_{sense(5,5)}$ is different in the two cases. Although the former observation could lead to many different hypotheses regarding the reason of this mismatch, the second one decimates them to a single one: the most probable reason is an evolving systematic error of the instrument or of the device itself due to the different times in which the measurement was taken.

The distributions of $S_{s\text{-}th}$ and V_t are not investigated. In the former case, because the parameter's variance is not so much critical as in the case of K_f, in the latter because it's not clear yet whether the measurement results are reliable. [fig. 90] shows the values of the biasing I_d currents of the different devices at the maximum allowed V_{gs} voltage allowed by the process: $V_{gs} = 1.8V$, under the assumption that this leads to the maximum ΔI_d value.

It's straightforward to calculate that it is always $\Delta I_d \leqslant 4\mu A$, about 6% of the average bias current per device. This amount is the minimum input dynamic that the readout amplifier must tolerate in order to avoid saturations when switching between one column and another. On top of this the small-signal current component due to the input must be added, but most probably Δ_d is the limiting factor.

5.3.4 Biasing characteristics

From the simulations, the issue of correct gate biasing arouse, and it was not trivial to note that keeping M_{bias} transistor in subthreshold not always leaded to $V_{gg} \approx V_{op}$. It was shown that the drive level of M_{bias} needed to be increased with respect to the suggested bias point, in order to correctly bias M_{sense}. In this section, an experiment aimed to verify the M_{sense} drive levels necessary to reach the desired value of V_{gg} is presented.

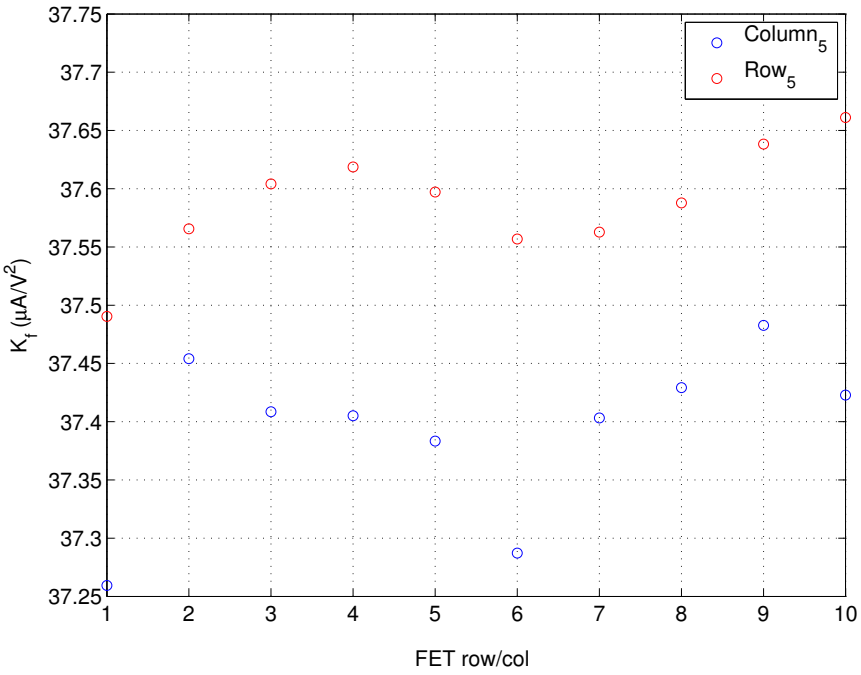

Figure 89: Different measured K_f parameter values for each FET.

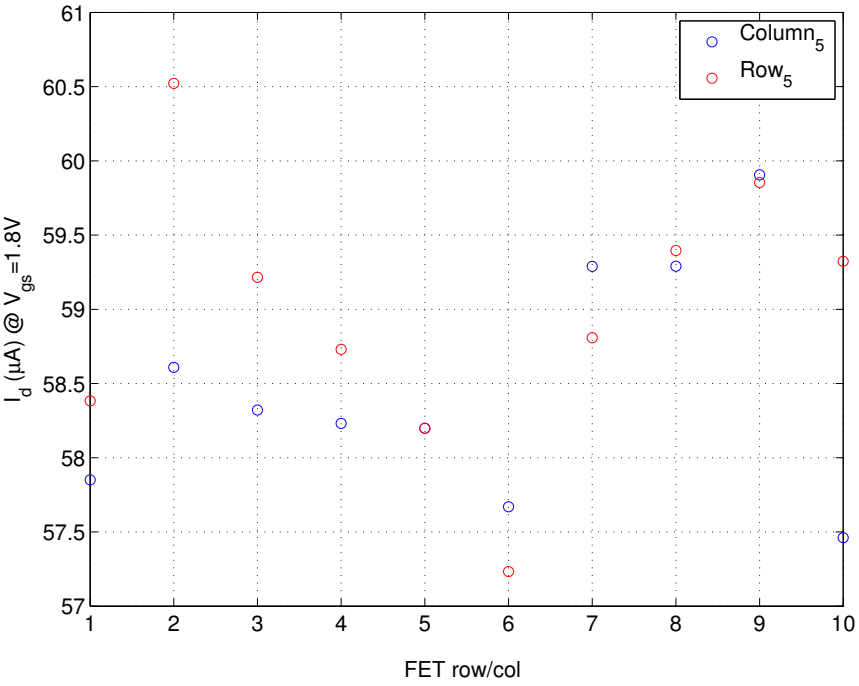

Figure 90: Different measured I_d @ $V_{gs} = 1.8V$ for each FET.

EXPERIMENT SETUP Needle no. 0177 is used for this experiment, then also data from needle no. 0021[38] is presented. The device is connected to the breakout board in the same way of the preceding experiments and $M_{sense(5,5)}$ is selected. The experiment was first run with a dry device, where the lowest leakage values are expected - as the top electrode capacitor is floating - and the device is expected to behave as if it was made only by the standard process layer. Then, the device is submersed in PBS electrolyte solution, with an Ag/AgCl reference electrode connected to ground, in order to check for differences and to verify a more typical use case. The experiment setup, in the case of needle submersed in electrolyte, is shown in [fig. 91].

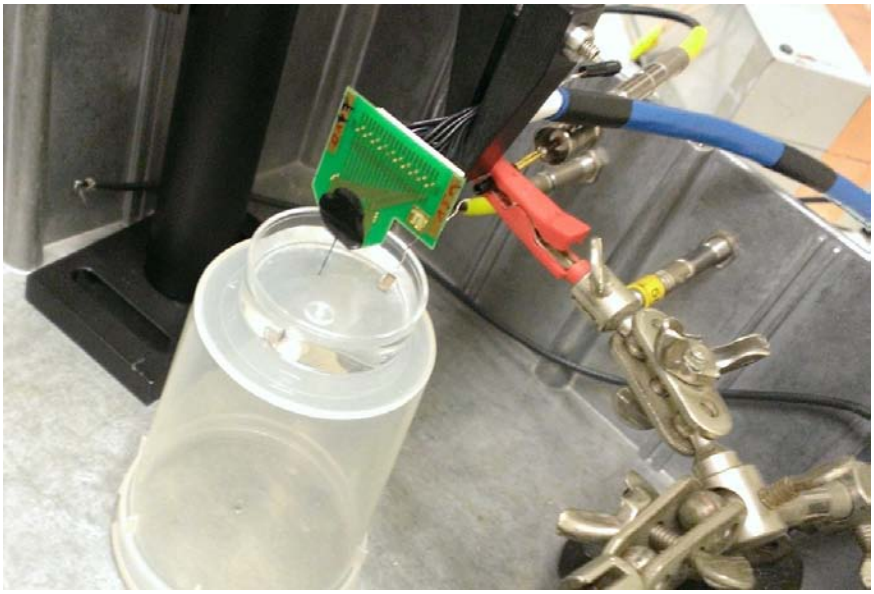

Figure 91: Experiment setup for bias characteristics measurement of a needle chip submersed in electrolyte (PBS solution).

METHODS Different desired values from $V_{gs,M_{sense}}$ are chosen in a span between 0.1 and 1V. The substrate is put at a voltage $V_{sub} = -V_{gs,M_{sense}}$ for each run, and it is imposed also $V_{el} = V_{ops} = 0V$ where V_{el} is the voltage of the reference electrode. This configuration is again a *grounded gate bias* and has the advantage that the electrolyte potential ϕ will not be too much different from the desired gate voltage V_{gg} (depending on electrode half cell potential, $\approx 0.23V$). For each value of V_{sub}, a sweep is made by increasing V_{ops} from 0 to 1V. As gate voltage V_{gg} was not directly measurable, the drain current I_d is used to estimate that value, as previously shown. In fact, from (26) the quire root of drain current is a linear estimator of overdrive voltage $V_{gs,M_{sense}}$-V_T.

RESULTS - DRY DEVICE As shown from [fig. 92] and [fig. 93], at least $V_{ops} = 0.75V$ is needed in order to bring V_{gg} within the 95% of desired value, regardless of the value of V_{sub}, even when the device is dry. This behaviour is quite unexpected, as the device should have the least amount of leakage in dry configuration. This suggests that probably there are two leakage components from the metal electrode:

- the aforementioned leakage current through the oxide to the electrolyte

38 From which lower leakage is expected, being the oxide thickness higher.

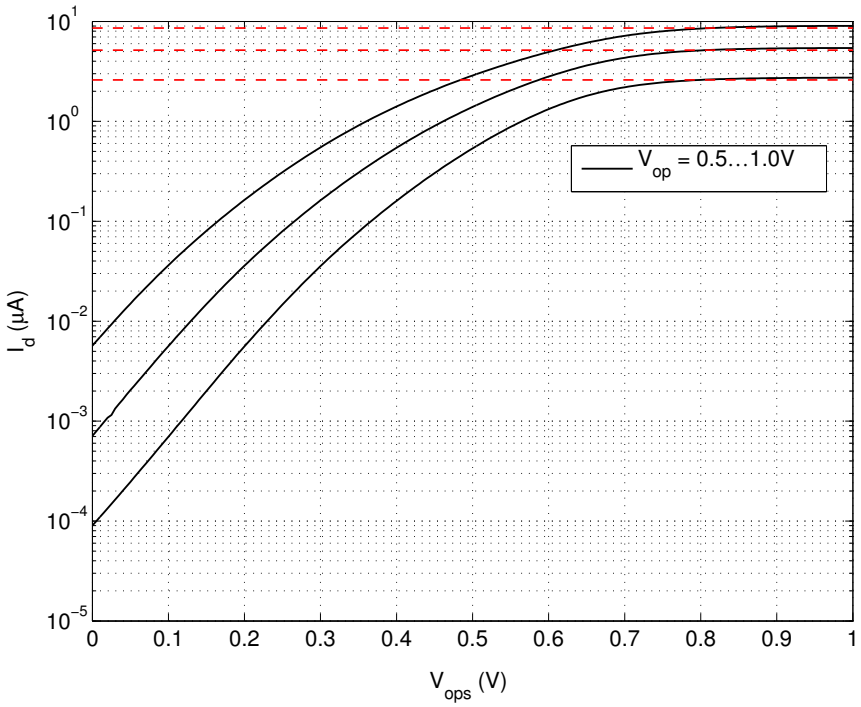

Figure 92: Measured $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a dry single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0177)

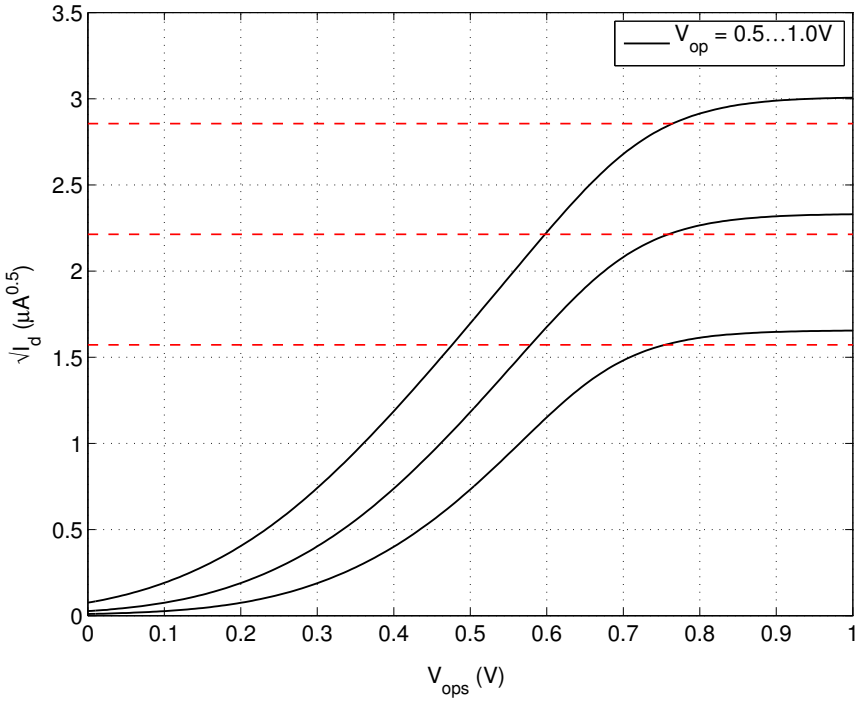

Figure 93: Measured square root of $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a dry single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0177)

- an additional leakage current to the substrate (which could due to the dielectric layer), which tends to steal bias current from the gate of M_{sense} even when the device is dry

The reduced value of K_f measured versus the simulated one could now be imputed to a negative offset on gate bias due to this phenomenon. More investigation needs to be done on this issue. In particular, uncoated needled - which are available - will be tested to see is that behave more ideally.

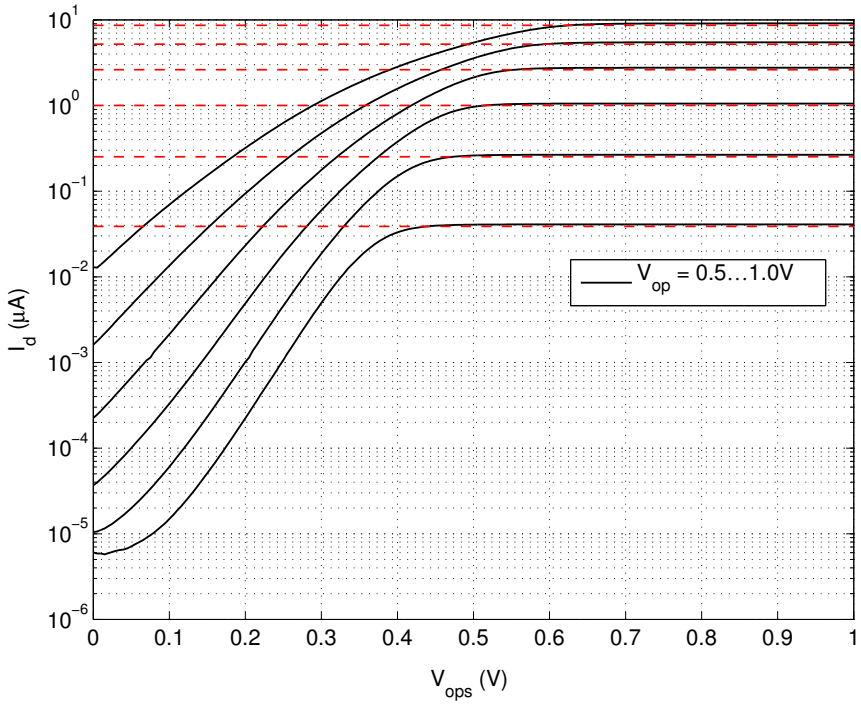

Figure 94: Measured $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0177)

RESULTS - WET DEVICE As shown from [fig. 94] and [fig. 95], at least $V_{ops} = 0.6V$ is needed in order to bring V_{gg} within the 95% of desired value, for each value of V_{sub} in the case of device no. 0177. This behaviour is quite worse than what was expected from simulations, and this will make the right compromise between bias and bandwidth hard to find. However, the voltage needed to correctly bias the transistor is lower than the case of the dry device. This confirms the hypothesis of a gate-to-substrate leakage which is mitigated, in this case, by gate-to-electrolyte leakage. Being the electrolyte potential ϕ near ground, this actually helps gate biasing. But, unfortunately, this is due to the fact that the device is working in *grounded-gate* configuration, and by design this particular configuration should be not needed to operate the device, which should provide good enough insulation to allow above- or below- ground operation of gate electrode. The fundamental point is that V_{gg} bias is not imposed by biasing circuitry (when M_{bias} operated in subthreshold) but depends on a complicate combination of effects. This behaviour is the principal point to address, as id causes much difficulties to correctly bias and operate the device with the needed stability and precision.

As shown from [fig. 94] and [fig. 95], device no. 0021 behaves a bit better, because $V_{ops} = 0.53V$ is enough to bring V_{gg} within the 95% of desired value. Having this device a thicker layer of TiO_2 dielectric (60nm), this was somewhat expected. However, dry characterisation of this needle is not available and considering the presented results on needle no. 0177,

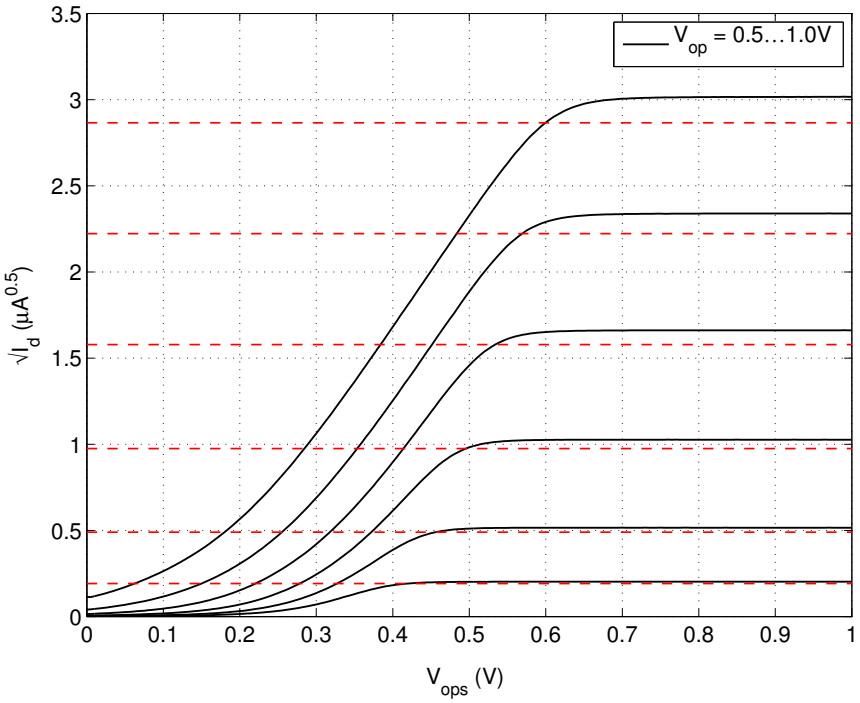

Figure 95: Measured $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0177)

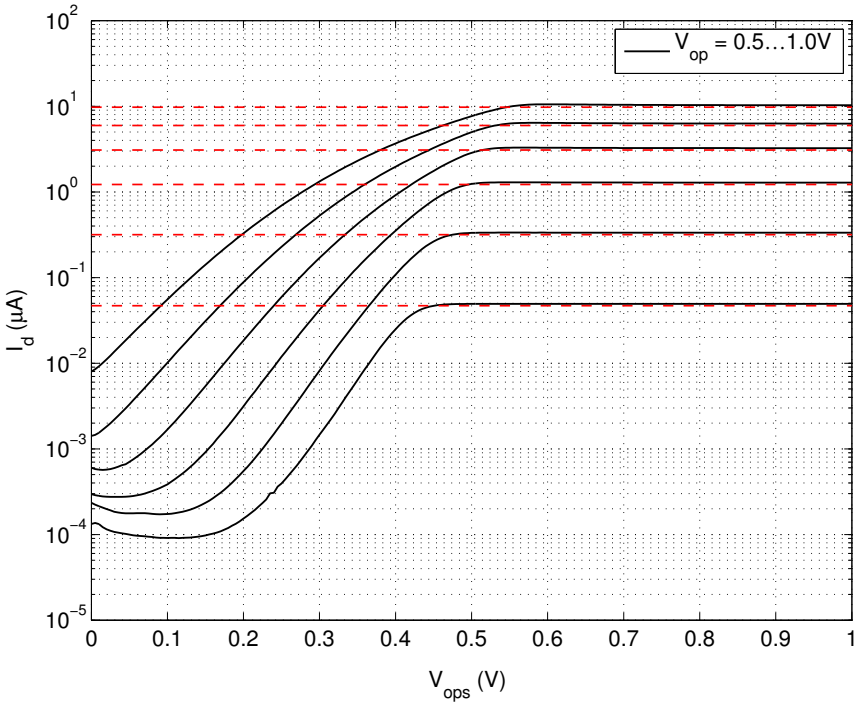

Figure 96: Measured $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0021)

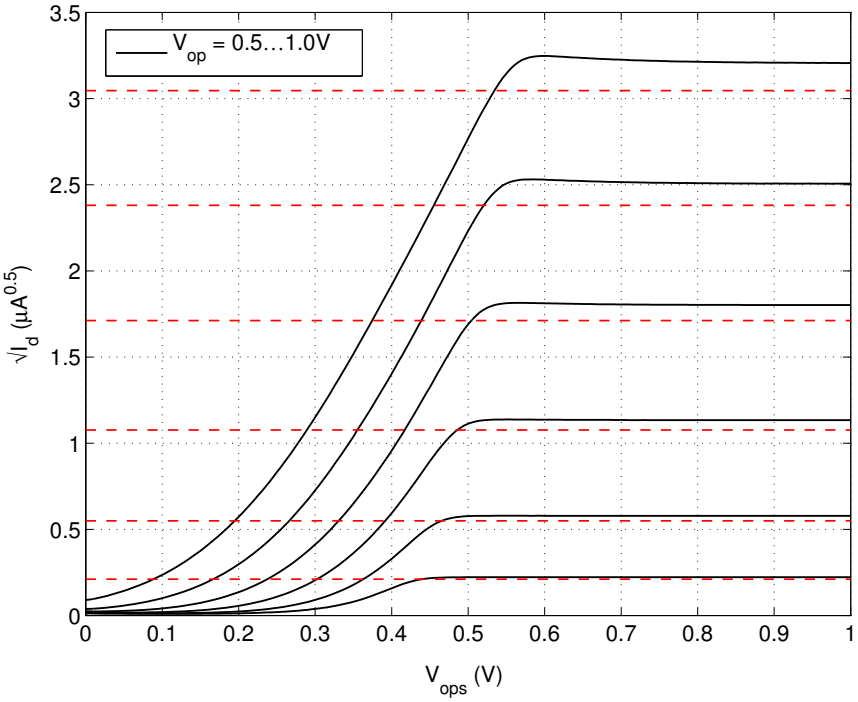

Figure 97: Measured $I_{d,M_{sense}}$-$V_{gs,M_{bias}}$ characteristics of a single pixel cell, with $0.5V < V_{op} < 1V$. Red line represents 95% of desired value. (Needle no. 0021)

more investigation is needed to understand how the two behaviours vary with dielectric oxide properties.

5.3.5 Bonding pads TLM analysis

As discussed, the bonding to the chip is done by breaking the top dielectric layer to reach the Au coated bonding pads underneath. This process, done with an ultrasonic wire bonder, was successfully performed for dielectric thicknesses up to 300nm. But the oxide break is far from being an ideal condition from insulation, and the induced formation of spatial crystal defects could unpredictably cause leakage between pads or between pads and substrate. Moreover, a batch of needles with abnormally high off-state current values arouse the suspect that this leakage could be not negligible. The only leakage that should be ideally seen between bonding pads and ground is caused by the ggMOS ESD protection structure.
A model that fits this physical layout if the Transmission Line Model (TLM), which for this analysis is used without reactive components. The model, properly scaled for this case, is shown on [fig. 98].

The impedance measured between V_{sub} and an arbitrary pad of index n (which is at distance nl from V_{sub} pad, where l is the inter-pad distance) among a total of N pads is governed by (42).

$$R_n = R_p \| R_{n,left} \| R_{n,right} \tag{42}$$

Where $R_{n,left}$ and $R_{n,right}$, which are the left- and right-side impedances seen from pad, are recursively modelled by (43) and (44), respectively.

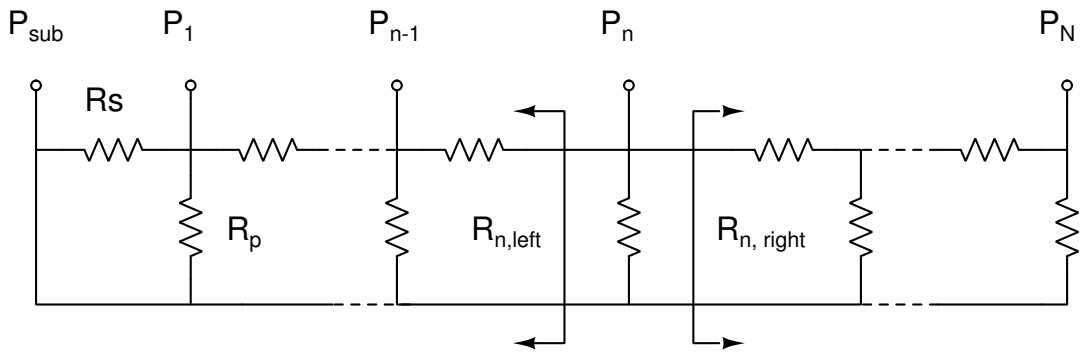

Figure 98: TLM model scaled to the investigated layout.

$$R_{n,left} = R_s + R_p \| R_{n-1,left} \quad (43)$$

$$R_{n,right} = R_s + R_p \| R_{n-1,right} \quad (44)$$

EXPERIMENT SETUP Needle no. 0168, which is coated with 20nm TiO_2, is used for this experiment. The quality of the break point is investigated with optical microscope and, although it is hard to have a good confidence, there seems to be a sharp and definite break edge with no overlapping or shorted metal tracks. In this configuration, the needle is still connected and bonded to the support PCB, but tracks are no more connected to the frontend devices. In this way, insulation and crosstalk of interconnect lines (both on PCB and on needle shank) and bonding pads can be investigated. Needle is positioned into a microprobe station and pins on the PCB connector are contacted and connected to two SMUs of an Agilent Technologies 4156C Parameter Analyzer.

METHODS A negative and positive voltage sweep is applied between V_{sub} and the selected pin, and I/V curve is measured. The procedure is repeated for many adjacent pads on a straight line (with reference to the bonding plan on the semiconductor side) and measured impedance is fitted to the model with a least square fit implemented in MATLAB®. Only positive data is used for fitting, as the contribute of intrinsic protection diode is expected for negative sweeps.

RESULTS Bipolar current on logarithmic scale is shown in [fig. 99]. The characteristic of the protection diode can be seen on the negative voltage side. With positive voltages, reverse current of diode is summed with pad leakage. Pad named "free" is bonded but has no protection structure, and symmetric, leakage-only current can be seen. Pad named "0" is not even bonded, and only leakage from PCB and current noise of the instrument.

Positive side current on linear scale is shown in [fig. 100], resistance is calculated as inverse of slope at each point and shown in [fig. 101], where it is shown to be nicely almost constant over voltage span.

Average resistance value for each pad is then shown in [fig. 102] for a relevant subset of pads, ordered by distance from substrate pad. Model fit is shown, and a good - although not perfect - fit is shown. The parameters extracted from fit are $R_p = 2.8G\Omega$ and $R_s = 41G\Omega$. Being those resistances responsible of a sub-nA DC leakage, they are considered not to

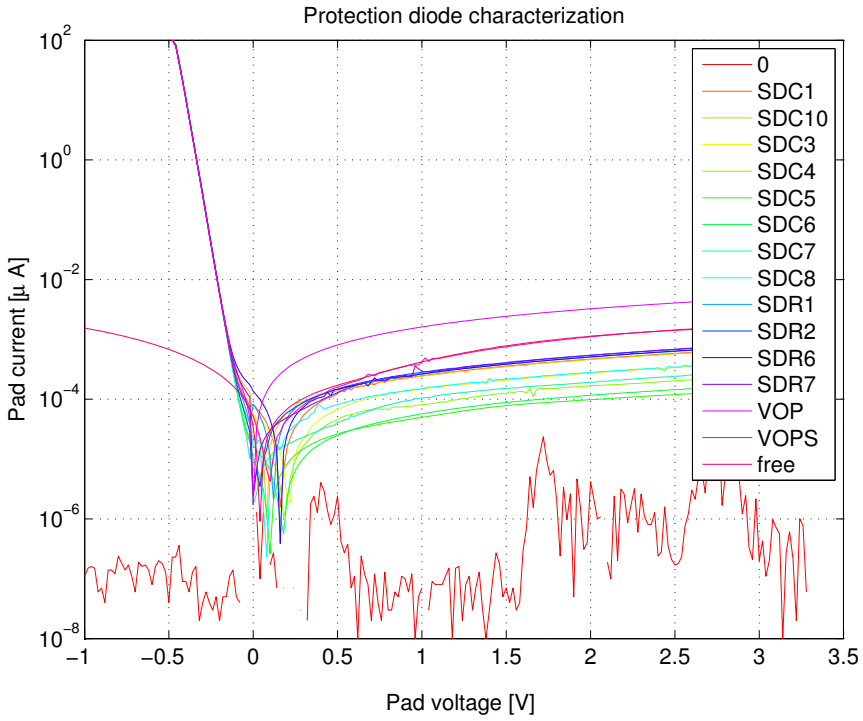

Figure 99: I_{pad}-V_{pad} characteristics on log scale for $-1V < V_{pad} < 3.5V$ with reference to V_{sub}. Series are in order of distance from V_{sub} pad. (Needle no. 0168/broken)

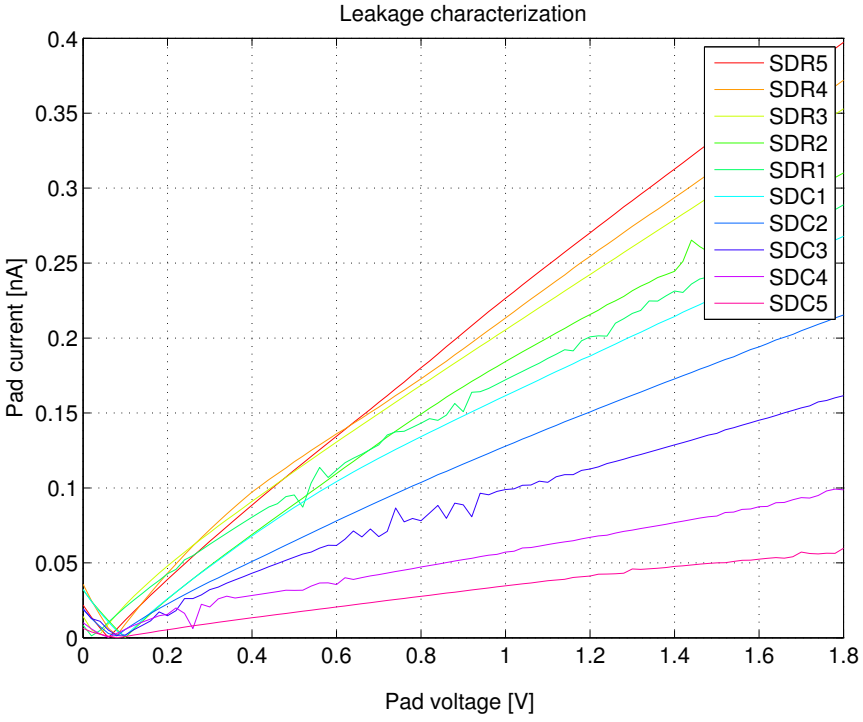

Figure 100: I_{pad}-V_{pad} characteristics on linear scale for $0V < V_{pad} < 1.8V$ with reference to V_{sub}. Series are in order of distance from V_{sub} pad. (Needle no. 0168/broken)

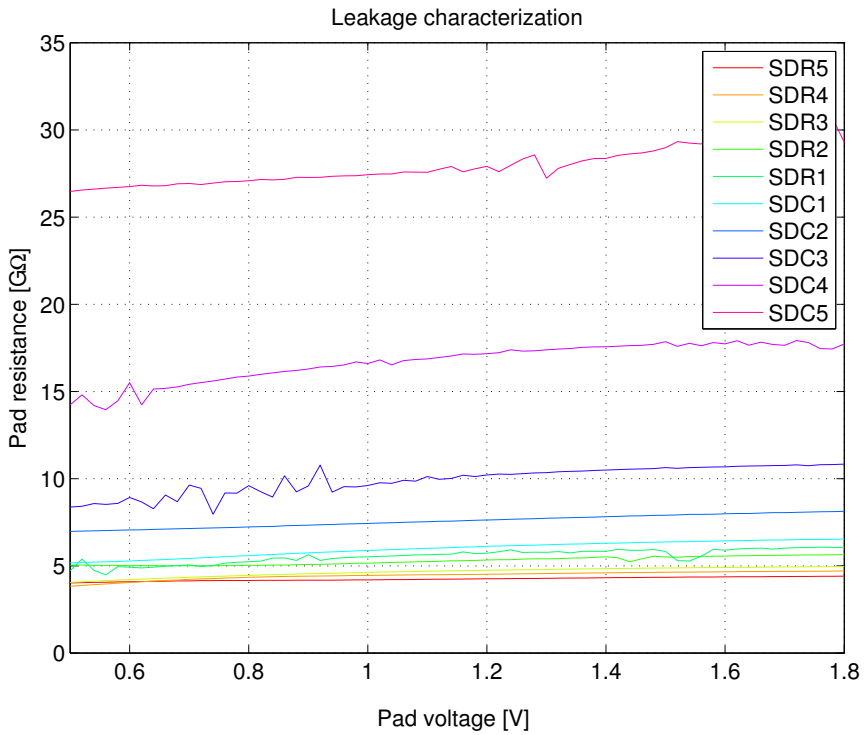

Figure 101: R_{pad}-V_{pad} characteristics on linear scale for $0.5V < V_{pad} < 1.8V$. Series are in order of distance from V_{sub} pad. (Needle no. 0168/broken)

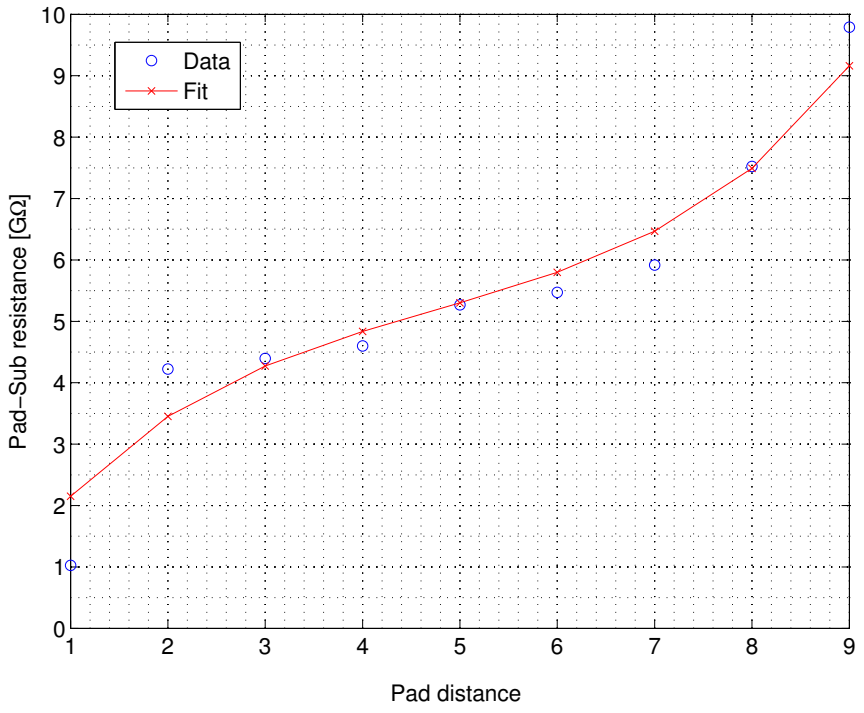

Figure 102: Resistance measured on pads fitted to TLM model, with respect to distance of pad from V_{sub} pad. (Needle no. 0168/broken)

interfere with device bias at all. R_s is not expected to cause relevant crosstalk issues, being the pad a low-impedance line (as it is current-mode driven and amplified). So, bonding is exonerated from causing pad leakage issues.
However, data is relevant for subsequent evaluations of dielectric layer sheet resistance.

5.4 OXIDE CHARACTERISATION

At the moment, all available needles were realised with TiO_2 coating. It is interesting to evaluate the leakage and dielectric characteristics of such material, in particular when deposited over the two kinds of metal electrodes employed: W and Ti/TiN. It is well known, indeed, that structure and properties of oxides, especially when deposited by ALD, depends on type of underlying material and surface properties. So, actually, information about dielectric constants and leakage currents taken from literature or different experiments must account severe variability if materials and methods of deposition are not exactly the same.
To evaluate performances of TiO_2 and other candidate oxides for needle chips, many flat samples were made by MDM labs in Milan, with the same process which is used to coat C-100-A/CMOS needles. Those samples are made on silicon substrate and are uniform, $8 \times 8cm$ in size, in order to have a large surface[39] for testing. A summary of available samples is presented in [tab. 7]. Samples are realised on n++Si substrate and back coated with aluminium for providing a reliable ohmic contact.

Table 7: List of available oxide sample flat chips for testing.

Date	Sample ID	Composition	Oxide thickness
Jul 2014	SAV747	$AlHfO_2$/W/n++Si/Al	20nm
	SAV747	$AlHfO_2$/TiN/Ti/n++Si/Al	20nm
Jul 2014	SAV750	HfO_2/W/n++Si/Al	20nm
	SAV750	HfO_2/TiN/Ti/n++Si/Al	20nm
Oct 2014	SAV768	$AlHfO_2$/TiN/Ti/n++Si/Al	20nm
	SAV769	$AlHfO_2$/TiN/Ti/n++Si/Al	10nm
Oct 2014	SAV770	HfO_2/TiN/Ti/n++Si/Al	20nm
TBD	N/A	TiO_2/TiN/Ti/n++Si/Al	34nm

5.4.1 Electrolyte bath system

A custom test fixture was developed in order to characterise oxide properties with reliability and repeatability. A threaded aluminium rod, being the back contact, is held in vertical position by a table mount. The sample is positioned on top of the rod, with aluminium coated side downside. A plastic cup, with a hole on the bottom being the mating thread, is screwed to the back contact rod. A nitrile O-Ring is inserted in between to allow sealed contact on the rod-sample-oring-cup sandwich. The cup is the filled with electrolyte and a reference electrode, typically Ag/AgCl, in submersed in it. The o-ring, which has inner diameter of 2mm and cross-section of 1mm, limits the contact surface of the top dielectric of the sample to the electrolyte to approximately $7mm^2$. This actually is the maximum possible contact surface when o-ring ideally lays on the sample. In general, surface will be lower due to o-ring compression and care must be taken to ensure repeatability on this parameter between subsequent measurements. Both contacts have wires and terminals for instrument connection. A mechanical drawing of this device is shown in [fig. 103]. A couple of this sys-

39 Without any kind of patterning which can mess up effective area estimation of deflection of electric field.

tem was made for MDM labs, where analogue characterisations are carried out on outgoing samples.

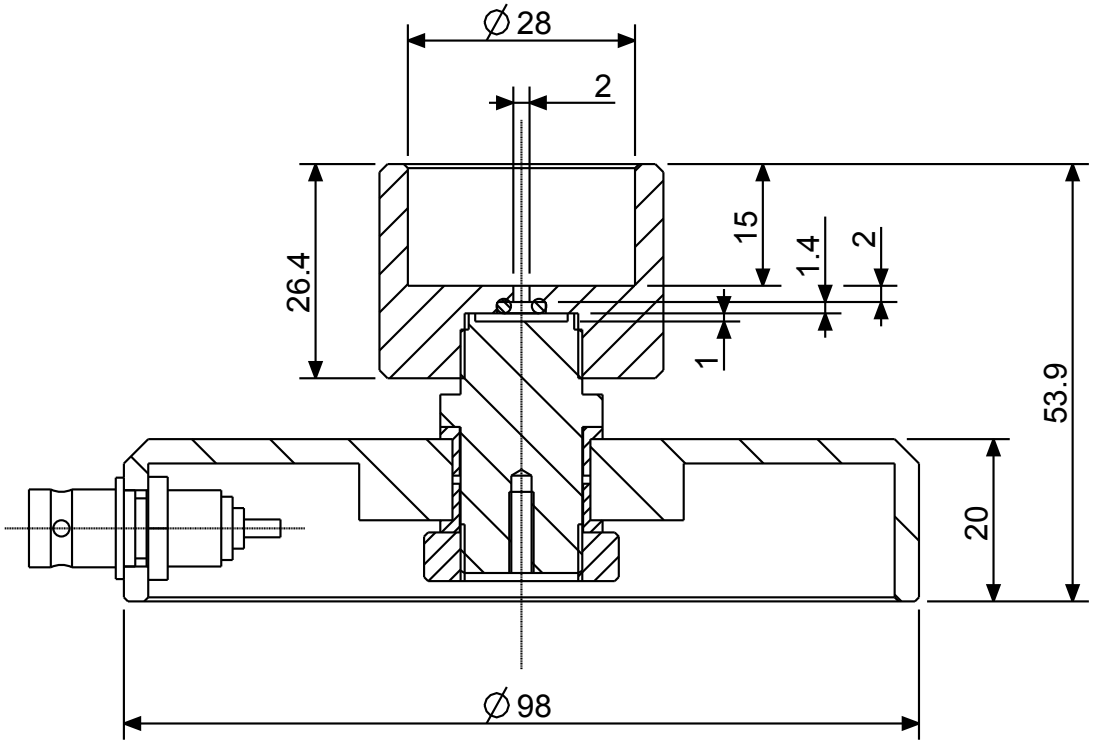

Figure 103: Mechanical section drawing of the electrolyte characterisation system for oxide samples.

5.4.2 Leakage current characteristics

This experiment was designed to measure the I/V characteristics of the different oxides in order to provide a better idea of the leakage current performances. As seen, in the choice of the best oxide for this device, leakage plays a leading role, being responsible for non correct biasing of M_{sense}.

EXPERIMENT SETUP The samples are put in the aforementioned wet characterisation system and the threaded cup is fixed. Electrolyte is poured and reference electrode is dipped inside. The two terminals of the measurement system are connected to the SMUs of an Agilent Technologies 4156C parameter analyser. A top view of the setup, including the reference electrode, is shown in [fig. 104].

METHODS The device substrate voltage is swept from -1.8V and +1.8V, and the current is measured. Reference ground is the Ag/AgCl electrode. Preliminarly, the leakage current budget is considered: the upper limit is represented by the current amount which does not interfere too much with biasing, which is $1\mu A/cm^2$. This value is under the limit for tissue damage so it is took as target.

RESULTS Curves for different measured samples are shown in [fig. 105], [fig. 106], [fig. 107], [fig. 108] and [fig. 109] .

In all samples a huge voltage offset is shown. Zero current value happens at a positive bias voltage value. Even considering the offset contribute due to half cell potential, this is

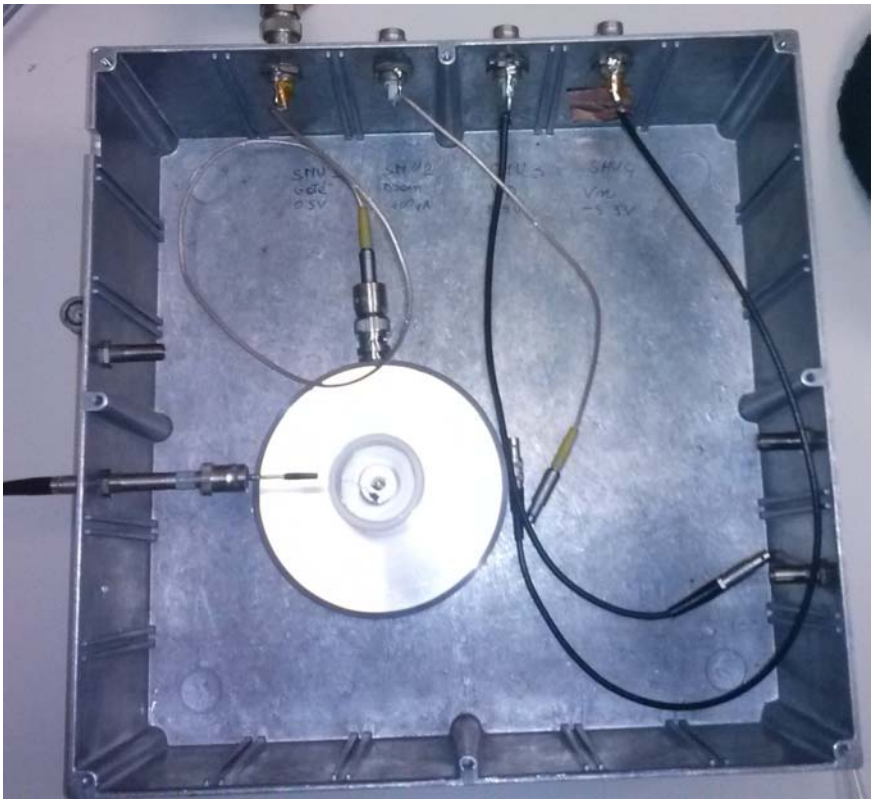

Figure 104: Photo of the electrolyte characterisation setup for oxide samples.

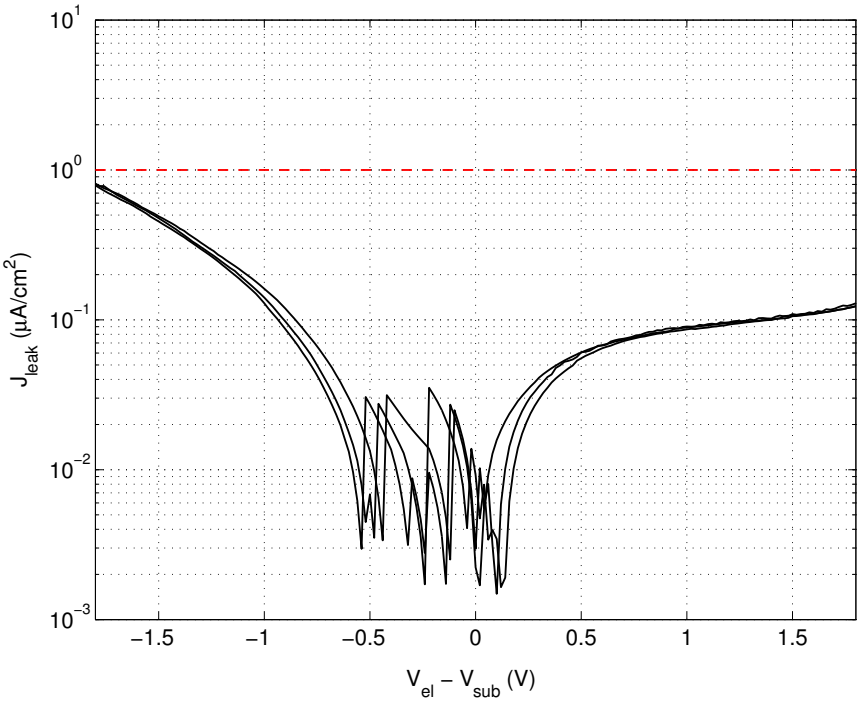

Figure 105: Measured leakage current density from substrate to electrolyte with $-1.8V < V_{sub} < 1.8V$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Sample SAV747/W)

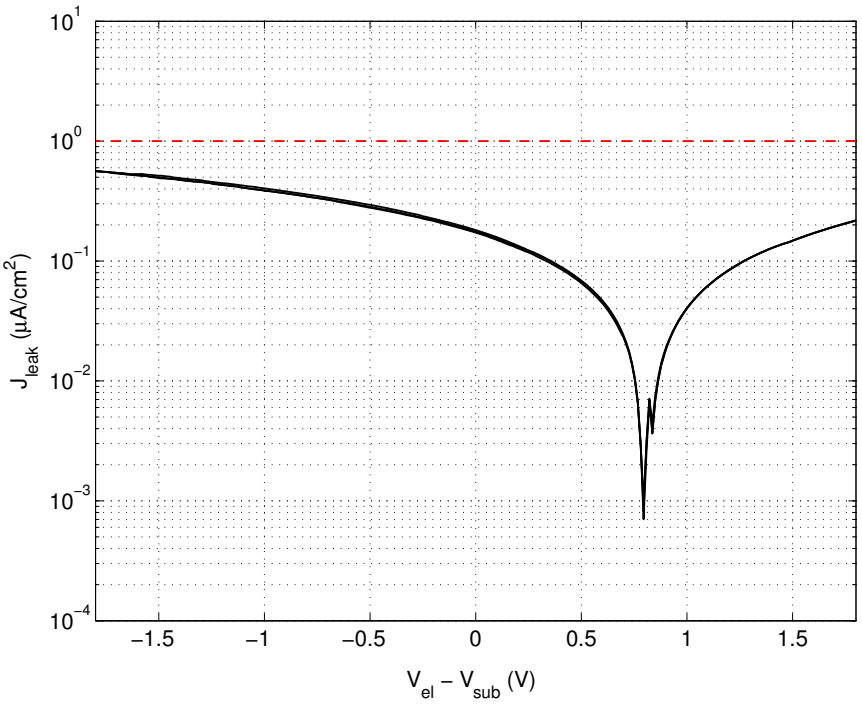

Figure 106: Measured leakage current density from substrate to electrolyte with $-1.8V < V_{sub} < 1.8V$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Sample SAV747/TiN)

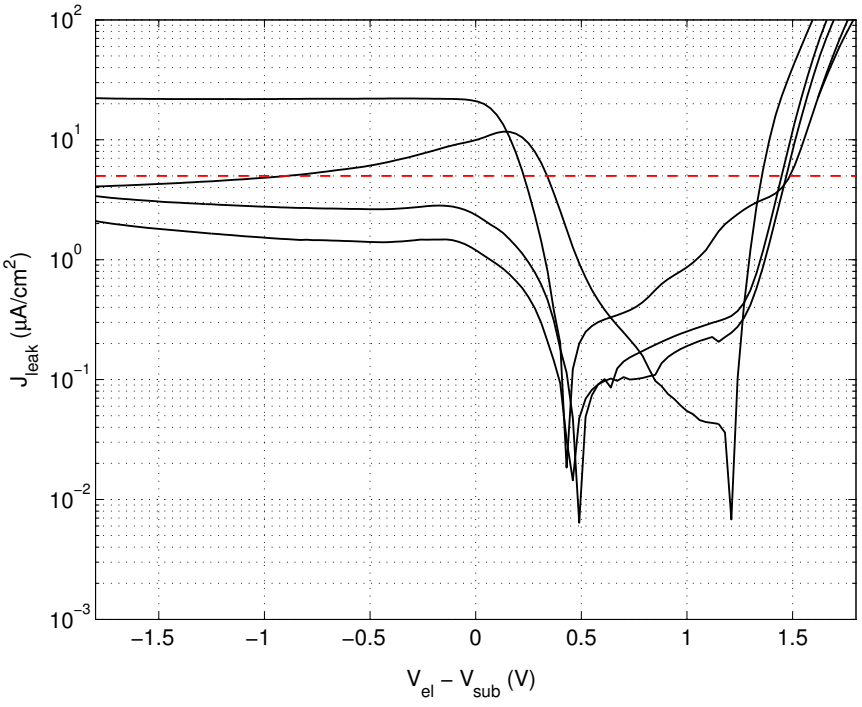

Figure 107: Measured leakage current density from substrate to electrolyte with $-1.8V < V_{sub} < 1.8V$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Sample SAV750/W)

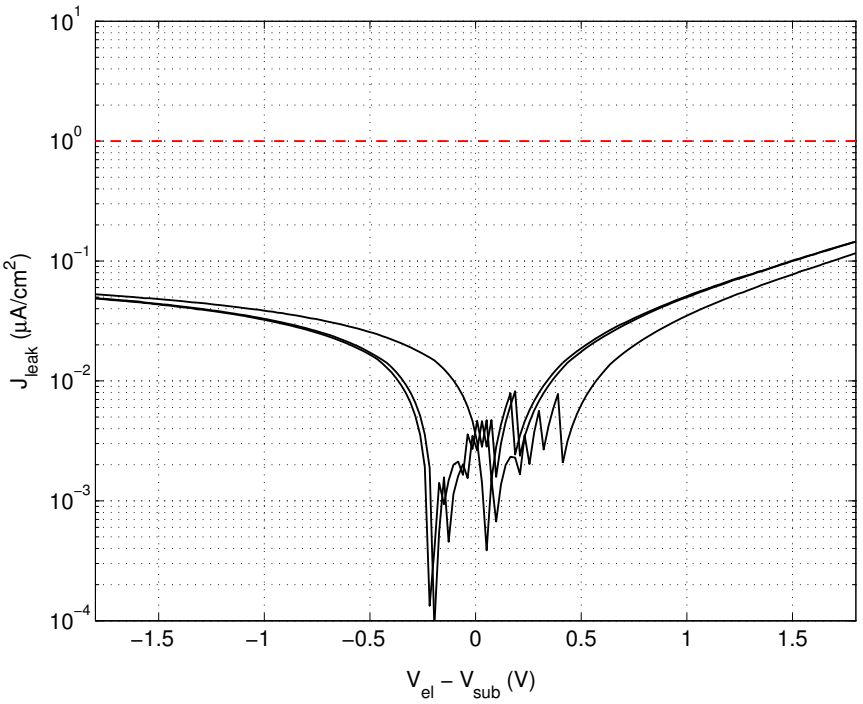

Figure 108: Measured leakage current density from substrate to electrolyte with $-1.8V < V_{sub} < 1.8V$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Sample SAV750/TiN)

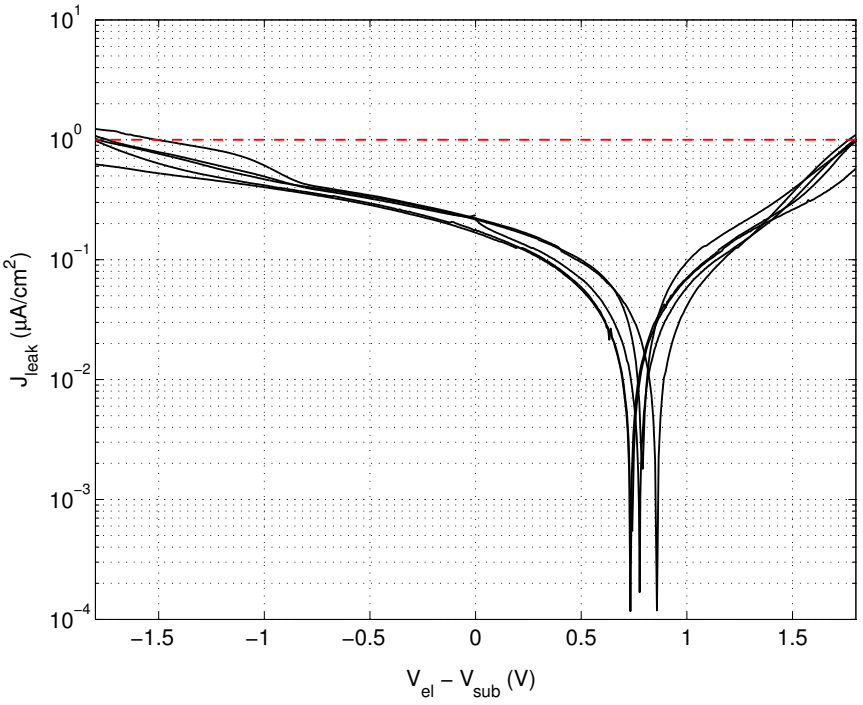

Figure 109: Measured leakage current density from substrate to electrolyte with $-1.8V < V_{sub} < 1.8V$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Sample SAV769)

not sufficient to motivate the magnitude of the offset. Although being outside of the purpose of this section, it could be shown that zero current state depends a lot on sweep direction and speed. This suggests that a huge amount of defects, both superficial and inside the oxide, contribute in making the behaviour of the device time-variant, due to accumulation and release of carriers in traps. Moreover, the hypothesis of ion capture at the surface under certain bias conditions, which can occupy traps thus varying the is concentration, was advances. More investigation is planned on this particular topic. As shown, current densities are below the budgetary threshold in a good bias interval in all samples excepted for SAV750/W, whose composition is 20nm of HfO_2 on tungsten. From those measurements, the best candidate in terms of leakage is HfO_2, which exhibits the best result on TiN electrode, which is actually the chosen material for new needle devices.
Measurements on TiO_2 still need to be performed in Padova, but preliminary data from MDM labs in Milan is available, and is reported in the following for reference.

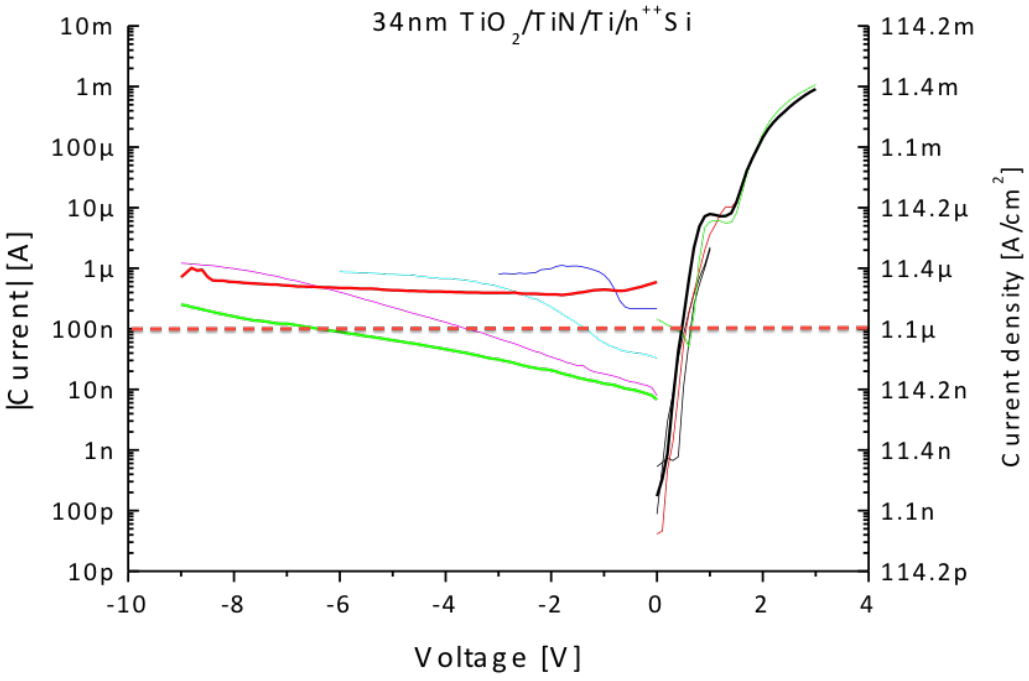

Figure 110: Measured leakage current density from substrate to electrolyte. Red line represents budgetary threshold of $1\mu A/cm^2$. (Unnammed sample TiO_2(34nm)/TiN/Ti/n++Si/Al. TiO_2 is confirmed to be in anatase phase.) [Credits: L. Gelmi, G. Tallarida, S. Spiga, M. Fanciulli - MDM labs, Milan]

This last result is very important: the current magnitude is much higher than the one of all other samples, and almost all the characteristic is above the budgetary limit of $1\mu A/cm^2$ of almost a decade. This strongly suggests that the reason for incorrect correct biasing of M_{sense} gate in TiO_2 needles is the high amount of leakage caused by the dielectric oxide. An effort is then needed either to improve TiO_2 insulation or to select other materials suitable for the application that exhibit lower leakage. Good candidates, as seen, are HfO_2 and $AlHfO_2$, which on the other hand are expected to have lower dielectric constant, so more investigation on those materials is necessary.

5.4.3 Capacitance characteristics

Capacitance measurements have been carried out at MDM labs in Milan and are currently planned in Padova. Although the measurement method is known, it will not be discussed here; the results are presented for reference.

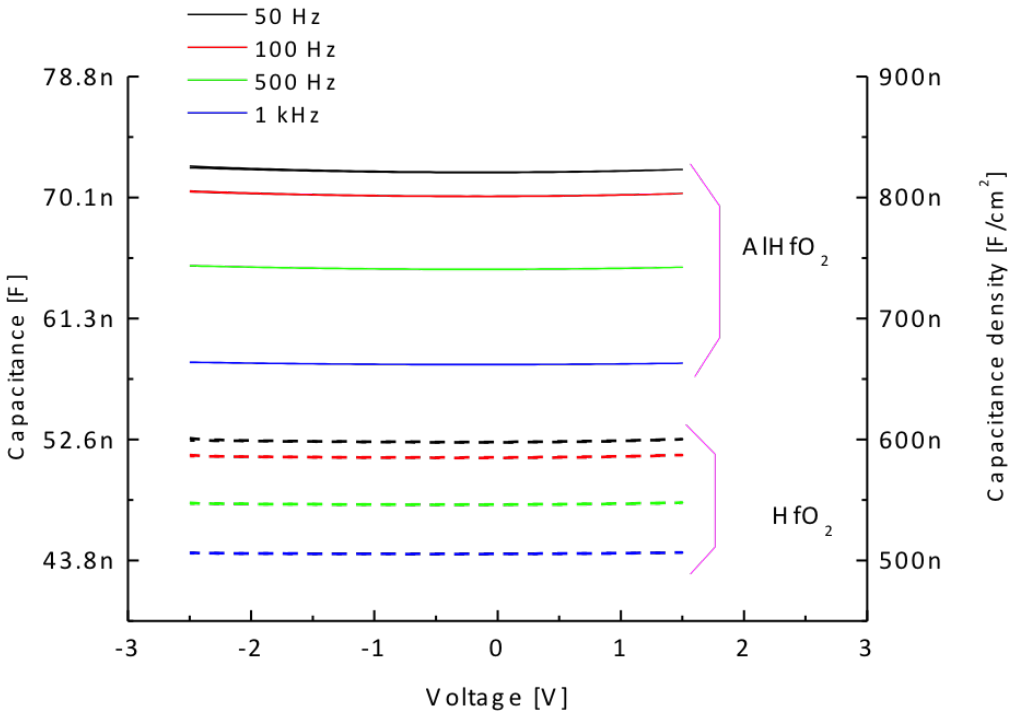

Figure 111: Measured capacitance between substrate and electrolyte. (Sample: SAV747/TiN) [Credits: L. Gelmi, G. Tallarida, S. Spiga, M. Fanciulli - MDM labs, Milan]

As shown in [fig. 111] and [fig. 111], capacity is absolutely constant against bias voltage in the case of HfO_2 and $AlHfO_2$ - as expected for an EOM - but is actually slightly dependent on bias for TiO_2.
Just to give an idea, the area of the top electrode is $64\mu m^2 = 64 \cdot 10^{-8} cm^2$. The resultant EOM capacitance would be 480fF in case of $AlHfO_2$, 350fF in case of HfO_2 and 1pF in case of TiO_2. This values are much higher than the safe minimum value of 150fF considered in the simulations. Thanks to this, the requirements for dielectric can be relaxed and almost all considered materials can be considered suitable for the application. On the other hand, this would allow to use higher drive values of M_{bias} while still having an acceptable low frequency coupling. However, this is not found in the needle used for frequency response characterisation and the reasons for this behaviour are still to be investigated. Other sources of leakage are mainly suspected.

5.5 DYNAMIC DEVICE CHARACTERISATION

Dynamic device behaviour is considered in this section. Some experiments are designed to test fundamental parameters of the device dynamic response, in order to assess the lower cut-off frequency - which is already discussed to be the most important dynamic parameter

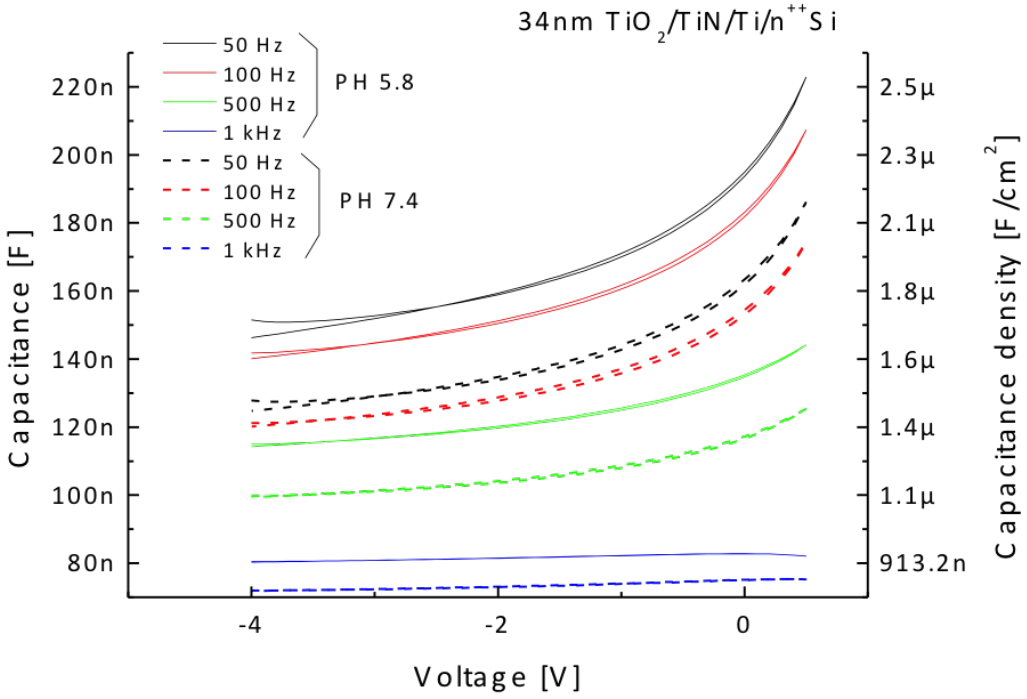

Figure 112: Measured capacitance between substrate and electrolyte. (Unnammed sample TiO_2(34nm)/TiN/Ti/n++Si/Al.) [Credits: L. Gelmi, G. Tallarida, S. Spiga, M. Fanciulli - MDM labs, Milan]

to be kept under control - and many time constants that can be useful to estimate non-directly measurable parameters.

HIGH SAMPLE RATE SMU BOARD In order to perform such dynamic experiments, a PXIe4141 board by National Instruments was procured. The board is equipped with 4 SMUs and is capable to provide up to 600kS/s with 10pA resolution (which, however, is dramatically derated at high sample rates). The board is provided with a DB25 front panel connector that can be pin-to-pin interfaced with the needle breakout board through a low leakage flexible cable. The board is programmed with a LabVIEW®software custom-made by the author to make dynamic device characterisation. A photo of the PXIe4141 is shown in [fig. 113].

Figure 113: Photo of PXIe4141 precision fast SMU board. [Source: National Instruments]

5.5.1 Pixel time constants

Considering the capacity connected to the V_{gg} node, at least two time constants are associated to that. One is the discharge time constant, that is when the node is disconnected from any bias circuitry and is discharged with $\tau_f = C_{gg,tot} R_{leak}$, where $C_{gg,tot}$ is the total node capacitance with respect to ground node and R_{leak} is the total leakage resistance. Another is the charge time constant, that is when the node is connected to bias circuitry and is charged with $\tau_r = C_{gg,tot} R_{out,M_b}$. The ratio between those two resistances is then simply obtained by means of [(45)][40].

$$\frac{\tau_r}{\tau_f} = \frac{C_{gg,tot} R_{out,M_b}}{C_{gg,tot} R_{leak}} = \frac{R_{out,M_b}}{R_{leak}} \tag{45}$$

And this ratio is generally wanted to be high in order to provide a precise DC bias. While the physical quantities involved in the above equation are hard to inspect, the two time constants can be easily measured.

EXPERIMENT SETUP Needle no. 0021, which is coated with 60nm TiO_2, is used for this experiment. The breakout board is connected to the PXIe4141 board, which is then programmed with a LabVIEW®software running on a desktop PC. The needle is connected

40 Actually, the equation holds when capacity at node is not varied when commutations are made. However, capacity contribution by C_{el} is supposed to dominate in all configurations.

to the breakout board and held by a mount. Dry measurement are taken with the device as it is, while wet measurements are taken into electrolyte, where the reference Ag/AgCl electrode is put to ground. Setup is shown in [fig. 114].

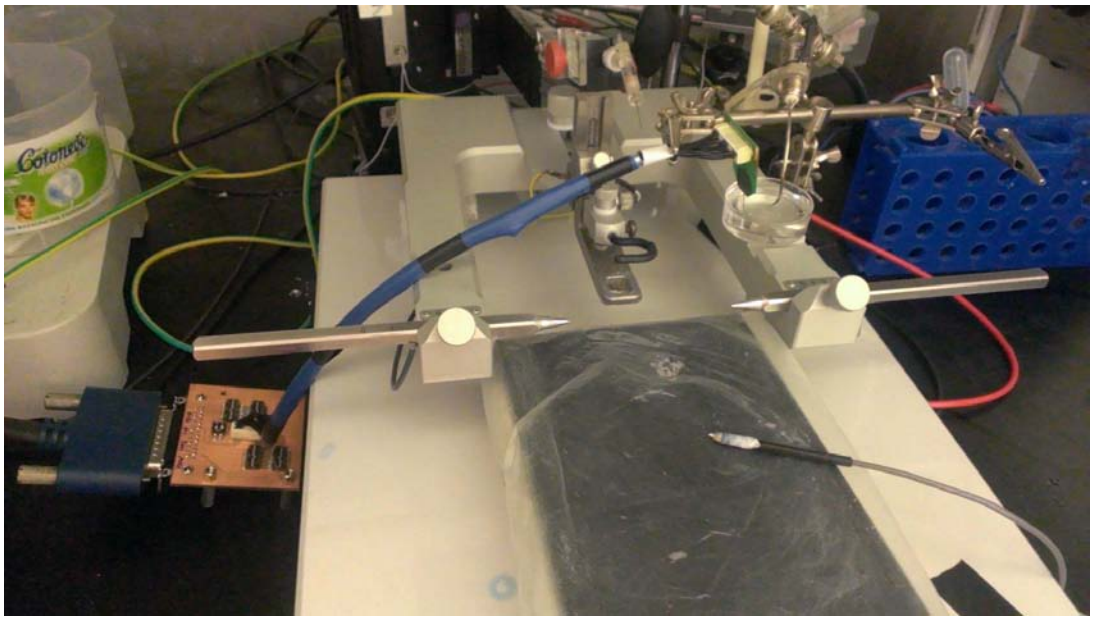

Figure 114: Photo of setup for dynamic device characterisation. Setup is configured in the same bench in which in vivo experiments are performed. Needle connected to breakout board and tip electrode for ground reference or signal injection can be seen.

METHODS Discharge time constant is taken by biasing the needle to a significant operating point ($V_{sub} = -1V, V_{op} = V_{row} = 0V, V_{ops} = 0.5V$) and then bringing V_{ops} to zero, in order to switch off M_{bias}. Square root of the recorded drain current is then used as an estimator of gate voltage of M_{sense}. Charge time constant is instead measured by biasing the needle to the same operating point and then varying V_{op} with a small-signal step, e.g. 10mV. Charge time is measured in wet condition only.

RESULTS Results for charge time are shown in [fig. 115]. A rise time (10-90%) of 4.4ms is measured, giving $\tau_r = \frac{4.4}{2.2} = 2ms$.

Results for discharge time are shown in [fig. 116] where square root of current is calculated. The discharge time of the dry device is longer than that of the wet device[41]. Discharge time seems to be independent, as hypothesised, on V_{ops} value, only a delay is visible. Reason for the initial rise of the current is not yet well understood. For wet device, a fall time (10-90%) of 1.5ms is measured, giving $\tau_f = \frac{1.5}{2.2} = 0.7ms$.

The results confirm that the resistance ratio between output resistance of bias circuitry and leakage resistance is more than one with $V_{ops} = 0.5V$, which is far from the expected (bias is almost precise at $V_{ops} = 0.5V$). In ideal condition, device should take much less time to charge into bias than to discharge. This suggests that the model is not so simple as hypothesised, and other resistive elements are present to interact with this kind of measurements.

41 However this is not much significant, as capacitance is different when device is in air.

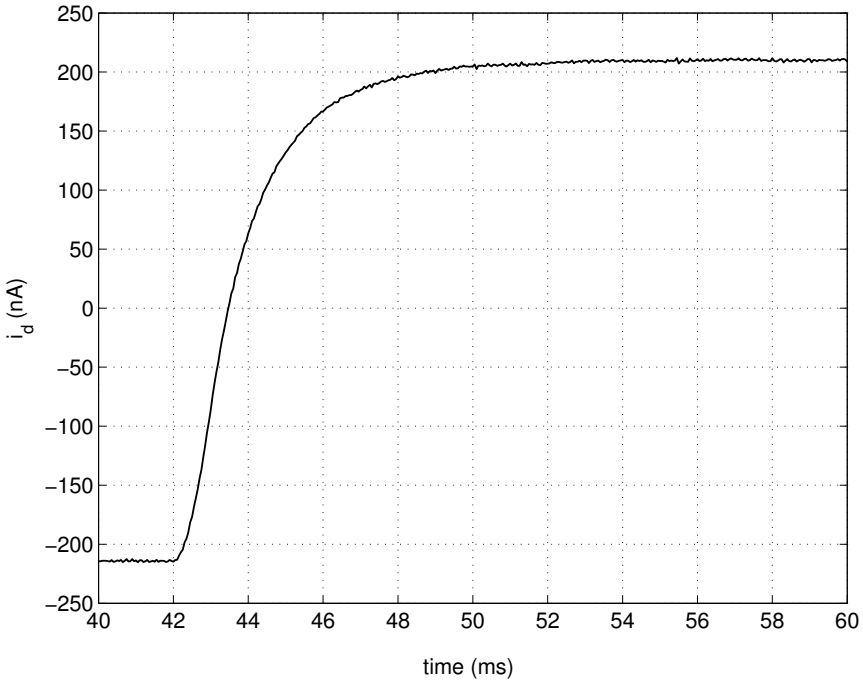

Figure 115: Measured AC response to square wave (2mVrms @ 3Hz) of single pixel cell with two different levels of M_{bias} gate drive. (Needle no. 0021)

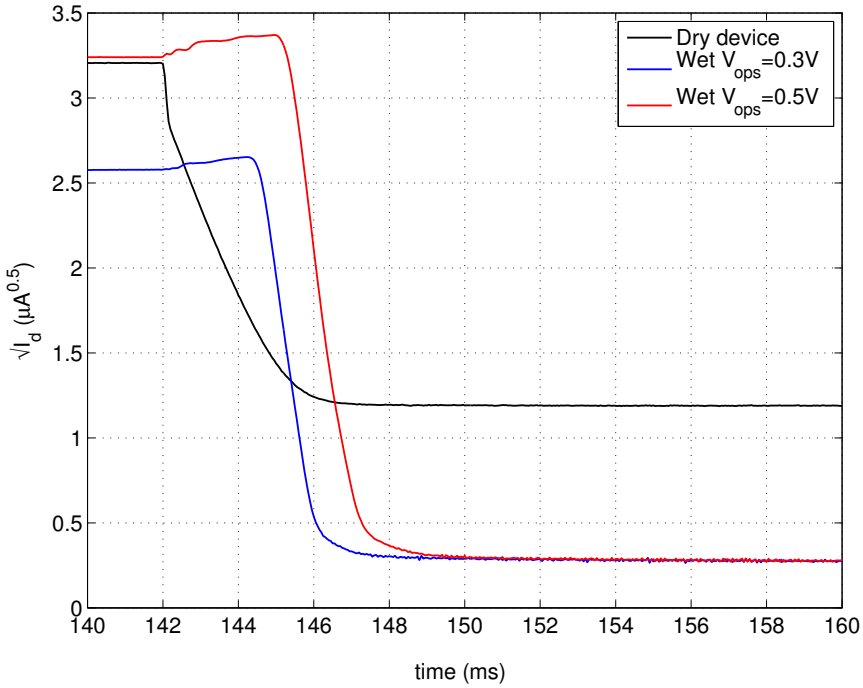

Figure 116: Measured AC response to square wave (2mVrms @ 3Hz) of single pixel cell with two different levels of M_{bias} gate drive. (Needle no. 0021)

5.5.2 Frequency response

Frequency response of the single pixel cell is investigated by sourcing a sinusoidal wave to the device at different frequencies, and the variation of gain is evaluated. Although tis process has not been yet automated, it gives a good idea of the device lower cut-off frequency at different biases.

EXPERIMENT SETUP Needle no. 0021, which is coated with 60nm TiO_2, is used for this experiment. Setup is almost the same used for pixel time constants measurements. However, in this case, the reference electrode is no more connected to ground but to the output of an Agilent Trueform®signal generator with 50Ω output impedance with a coaxial cable. Another 50Ω line terminator is connected near to the electrode, and signal shield is connected to ground.

METHODS The device is then biased with $V_{sub} = -1V$ and with different values of V_{op}. Signal generator is then activated with sinusoidal output at an amplitude of $2mVrms$ and frequency is then manually swept between a few Hertz and 2kHz. Amplitude of small-signal current is detected and recorded.

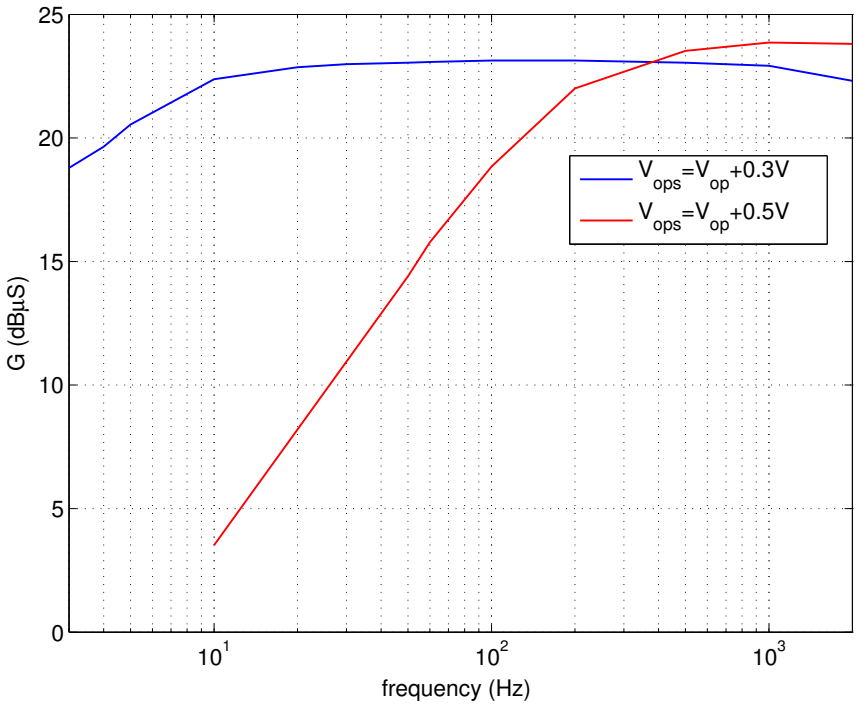

Figure 117: Measured frequency response of single pixel cell with two different levels of M_{bias} gate drive. (Needle no. 0021)

RESULTS Measured frequency response with two different levels of M_{bias} gate drive is shown in [fig. 117]. As expected, cut-off frequency increases together with V_{ops} level, and bandwidth quickly reduces. At $V_{ops} = V_{op} + 300mV = 300mV$, lower cut-off frequency at -3dB gain with respect to centre band is $f_c(V_{ops} = 300mV) \approx 5Hz$, whereas when drive strength is increased to $V_{ops} = V_{op} + 500mV = 500mV$, $f_c(V_{ops} = 500mV) \approx 100Hz$. Overall gain is lower than simulated centre band gain, and this matches with the lower g_m measured during characterisation. With higher V_{ops} voltages, gain is higher, according to

the fact that M_{sense} is biased at higher current level. With lower V_{ops} voltages, gain begins to fall after about 1kHz, probably due to the lower transition frequency of the FET. Unfortunately, $f_c(V_{ops} = 500mV) \approx 100Hz$ is too high to perform LFP measurements, and $f_c(V_{ops} = 300mV) \approx 5Hz$ is a much more acceptable value, so, again, a compromise between bandwidth and gain (and, in the end, noise) must be found.

5.5.3 Square-wave response

Analogue estimate of the pass-band of the system is given, in the time domain, by analysing the response to a square wave stimulus.

EXPERIMENT SETUP Needle no. 0021, which is coated with 60nm TiO_2, is used for this experiment. Setup is exactly the same of frequency response measurement. The only difference is that the stimulus is a square wave signal.

METHODS The device is then biased with $V_{sub} = -1V$ and with different values of V_{op}. Signal generator is then activated with square wave output at an amplitude of $2mVrms$ and 3Hz frequency[42]. Small-signal current is recorded and DC value is rejected numerically.

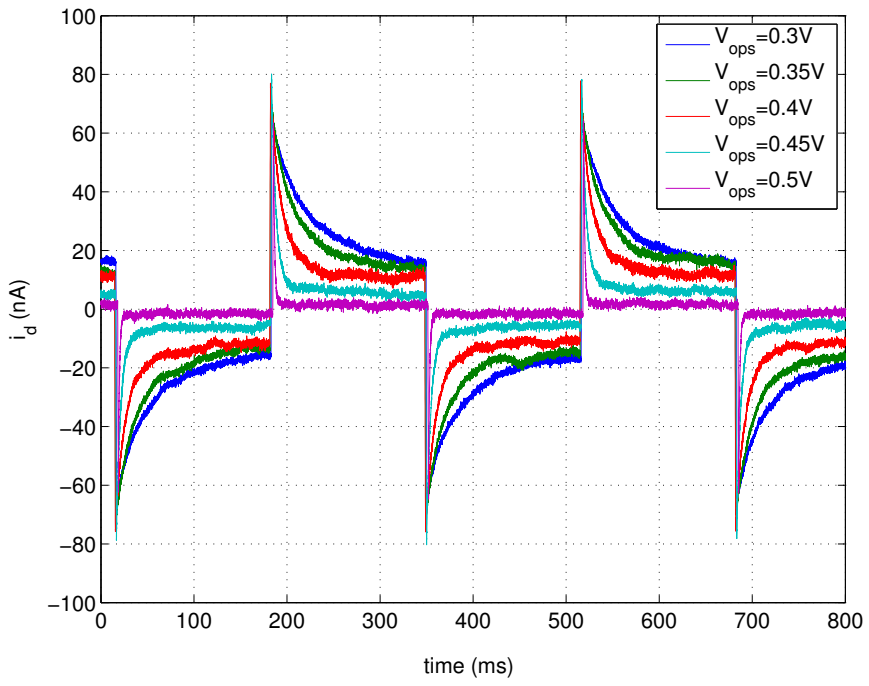

Figure 118: Measured AC response to square wave (2mVrms @ 3Hz) of single pixel cell with two different levels of M_{bias} gate drive. (Needle no. 0021)

RESULTS As shown in [fig. 118], the response in the time domain is very different at each M_{bias} drive level. For low drive levels, the exponential decay can still be viewed, meaning that the time constant is of the same order of magnitude of the wave period. For high drive level, only a needle impulse is shown for each half period, meaning that fundamental frequency is far outside of pass-band. With lowest drive levels, a proportional gain can be seen, as it is the step between settling values for each half-wave response. This means that,

42 Low frequency is chosen to allow transient to settle between each period.

when the output resistance of M_{bias} is low enough, the input voltage divider exhibits a DC gain due to the two resistive components of R_{out,M_b} and $R_{leak,ox}$ (see [fig. 71]).

5.5.4 Needle leakage current

This experiment was designed to try to estimate whether the leakage of TiO_2 dielectric deposited on the needle matched the leakage measured on the flat test device already shown. The idea of the experiment is to measure the I/V characteristic of the substrate of the needle with respect to the electrolyte reference electrode, while the needle is submersed. Basing on the assumption that the substrate is exposed for leakage through TiO_2 only on the back side and on the side wall[43] the current density can be estimated.

EXPERIMENT SETUP Needle no. 0021 is used for this experiment. Similarly to the characterisation procedure of oxide leakage, the needle is submersed in the electrolyte together with reference Ag/AgCl electrode, as in [fig. 91]. Particular care is taken to verify that the submersed length of the needle, from the tip to the electrolyte surface, is 3mm.

METHODS The device substrate voltage is swept between -1.8V and 0V and subsequently between 0V and +1.8V, and the current is measured. Reference ground is the Ag/AgCl electrode. The total back side area exposed to the electrolyte is calculated:

$$A = 3mm \times 300\mu m = 0.9cm^2 \approx 1cm^2 \tag{46}$$

RESULTS A plot of the measured current together with the estimated current density is shown in [fig. 119].

As it can be spotted, the current density is generally a little bit higher that that measured on TiO_2 flat samples. It is lower than tissue damage threshold, which is $5\mu A/cm^2$, in a limited interval. On the other hand, it is safe to operate the needle with V_{sub} between -1.5 and 0.7V without worrying of inducing tissue damage[44]. However, current density is under the budgetary threshold of $1\mu A/cm^2$ only in a reduced bias interval. In grounded-gate configuration, the substrate operates in the right side of the curve. The *diode-like* asymmetric characteristic is very similar to the one of measured test samples.

5.5.5 Needle leakage photoemission test

This experiment was designed to verify if the distribution of leakage current density on the needle surface. When a high current density level is reached in a conductor, a so-called *hot spot* is formed. This condition can be reached, for example, when a small single volume of a bigger drive exhibits much more conductance than the rest of material. In this condition, high speed carriers, called *hot carriers*, are responsible for current density. Hot carriers can undergo relaxation with emission of photons, or in presence of direct junctions can exhibit radiative photoemission. Monitoring photoemission of a device can then spot location where high current densities are present. Highest current values are expected actually on the borders and on sharp edges, where coating is less uniform and can be easily mechanically damaged, and electric field is more intense.

EXPERIMENT SETUP Needle no. 0169 is used for this experiment. The device is submerged into electrolyte bath under the field of view of a Hamamatsu Photonics PHEMOS-200 Emission Microscope. The device is inclined to an angle of about 80° with respect to the plane normal, in such a way to expose the tip surface to the microscope. The device is kept just as

43 The many layers of silicon dioxide that form the backend should properly insulate the substrate on the top side.
44 However, this limit is pretty conservative.

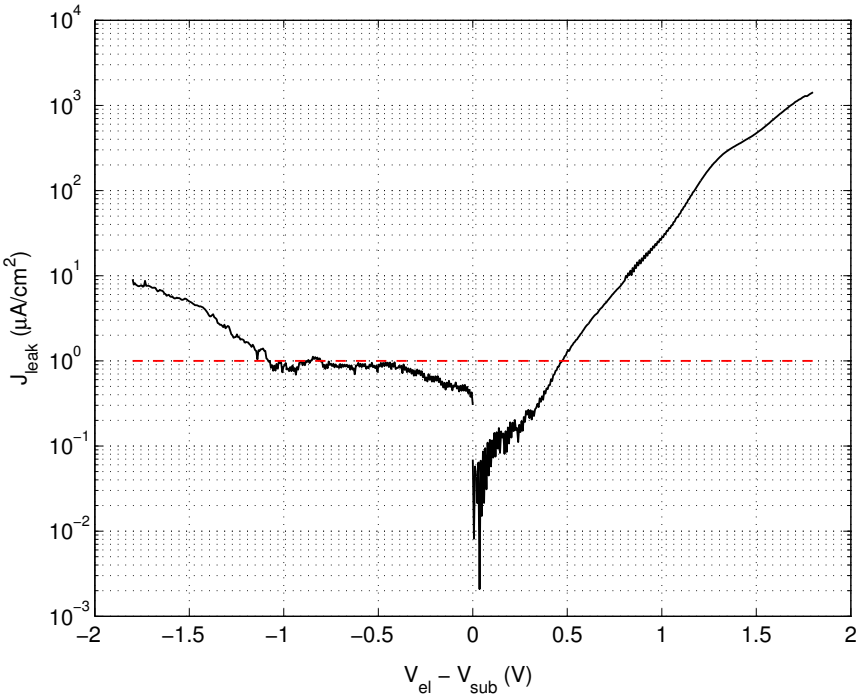

Figure 119: Measured leakage current density from substrate to electrolyte, with 60nm TiO_2 dielectric coating on Ti/TiN top electrode, for $-1.8 < V_{sub} < 1.8$. Red line represents budgetary threshold of $1\mu A/cm^2$. (Needle no. 0021)

less submerged as possible, almost touching the electrolyte surface. Particular care is taken to verify that the liquid meniscus formed by cause of the needle at the surface do not cause too much lens effect, which could distort the acquired image.

METHODS V_{sub} is set to a positive voltage so that to cause a current of at least $1\mu A$ to flow. Shutter of detector camera is then kept open for an exposure time of 30 minutes, while data is integrated into the image. Procedure is repeated for both the front and the back of the device.

RESULTS

RESULTS Photoemission count in arbitrary unit is shown in [fig. 120] or [fig. 121]. False colour scale is used, where blue is the lowest count and red/white is the highest count. No particular hot current spots are shown. Particularly, no hot spots are found on edges, conversely to what was expected[45]. Current is uniformly distributed on the surface, and smoothly gets higher towards the centre of the needle. Note that back and front side measurements are not comparable because gain is not normalised. An experiment with both sides of different needles at the same time is planned to measure leakage difference between sides.
A photoemission micrograph of the whole needle with low magnification and low gain is shown in [fig. 122], where distribution on the whole needle - which is a little less uniform than in previous data - is shown. Bubbles, due to water electrolysis, can be seen in all photos.

45 Even if lens effect must be further investigated, because an uncommon completely blank border is shown in the photo around the needle.

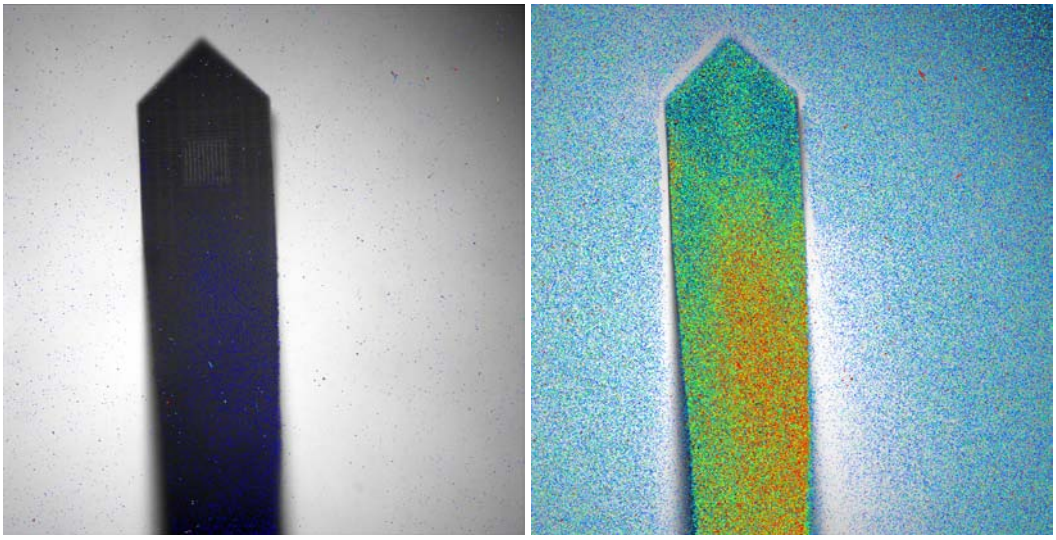

Figure 120: Photoemission microscopy image of the front side of needle leaking current while submerged in electrolyte, with low gain (left) and high gain (right) false colour intensity scale. With low gain, recording matrix can be seen. (Needle no. 0169)

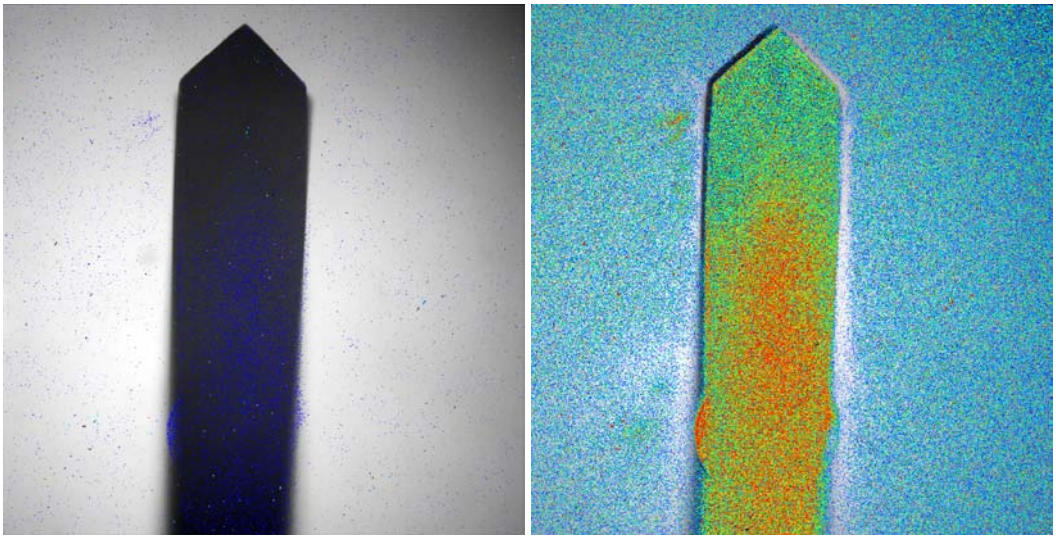

Figure 121: Photoemission microscopy image of the back side of needle leaking current while submerged in electrolyte, with low gain (left) and high gain (right) false colour intensity scale. (Needle no. 0169)

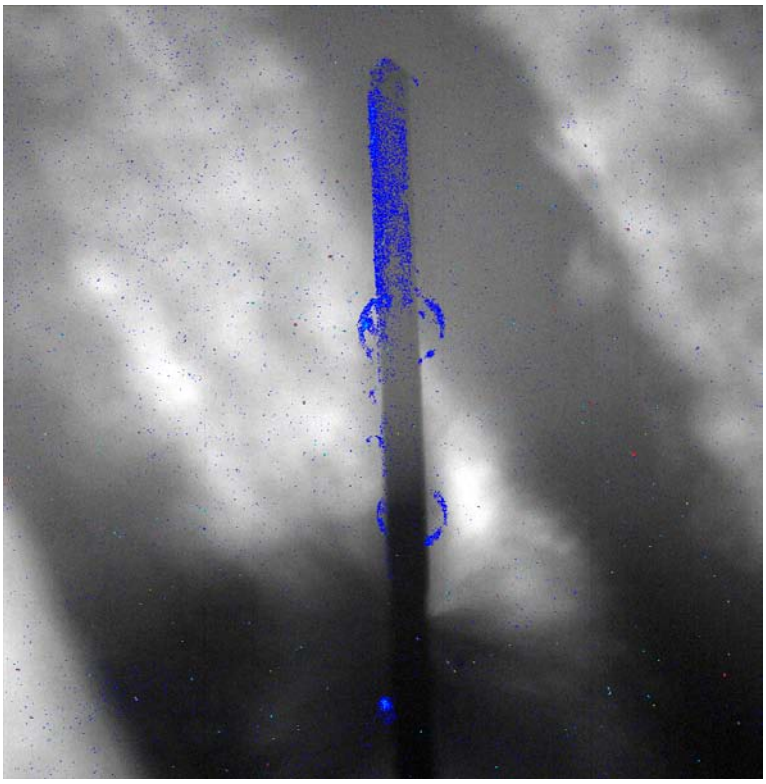

Figure 122: Photoemission microscopy image of the back side of needle leaking current while submerged in electrolyte, with low gain false colour intensity scale. Low magnification (5x) allows to see almost the whole needle. (Needle no. 0169)

5.6 COMMENTS AND REMARKS

In this chapter, an attempt to understand as much as possible of the device has been done. Many limitations have been spotted, but also many configuration in which the device should operate in a functional way. And finally, many controversial points were fund, upon which more investigation and reasoning is necessary. In the end, improvement of ideality of behaviour of device is necessary, either by improving dielectric material or other sources of leakage. The device, should, in the end be operable without worrying too much about interferences of boundary conditions to biasing and bandwidth. This is because the needle is, in the end, only a measurement instrument used in the framework of more complex experiments[46] and, for this reason, it does not have to be a limiting factor for the experimenter, but instead a ready and straightforward to use device. This point of view is fundamental to be able to spot in which direction research should be made to improve the device.

OPERATING POINT However, despite the many limitations found. A better way to operate the device was found too. It was seen that M_{bias} drive level must be put higher that expected in order to correctly bias the sensing transistor, but not too much in order to preserve the pass band. So it's now possible to rewrite the suggested operating point as in [tab. 8].

Table 8: New biaspoint for the single pixel cell, as a result of analysis and characterisation.

Node	Voltage [V]
V_{col} (V_s)	-1
V_{row} (V_d)	0
V_{op}	0
V_{ops}	0.3÷0.4
V_{sub}	-1

NOTE ON THE USAGE OF P-CHANNEL DEVICES As shown, P-channel devices are available too. Of course, with the proper swaps in voltages, it is possible to use those needles with minimum changes (or even none) to the existing measurements setup. Until now, no particular performance improvement was found by using P-channel devices. An attempt to mitigate leakage by exploiting reverse-biasing of n-well where P-mos device is realised, was done, however without significant improvements on signal quality. It is work to say that P-mos devices have a fairly lower current factor and transconductance, so that overall gain is lower. This could impact on signal integrity because it gives more relevance to the noise contribute of the amplifier chain. For this reason, as the readout amplifier design is yet challenging, no reason was found to operate with P-channel devices.

46 Some examples of those are given in the next chapter

6 NEEDLE AT WORK

In this chapter, after recalling the fundamental lessons obtained from the device simulation and characterisation, the execution two experiments is described, where the C-100-A/CMOS needles are employed to record signal in the rat brain. First results ever obtained with this kind of devices are then finally presented.

6.1 LESSONS LEARNED FROM CHARACTERIZATION

A comfortable bias point was found, together with countermeasures to minimise gate oxide leakage.

GATE BIASING The biasing interval which gives the best compromise achievable between bandwidth and biasing accuracy is given in [tab. 8] and is commonly used in all experiment described in this chapter.

GROUNDED-GATE OPERATION When either in-vitro calibration or in-vivo experiments are performed, care is taken to avoid excessive dielectric leakage current with smart biasing of the electrolyte or extracellular medium. Typically, as in in-vivo experiments the animal is kept to ground by means of the stereotaxic holder, also the extracellular medium is put to ground with an Ag/AgCl needle electrode. This allows the aforementioned *grounded-gate* operation of the needle. Nonetheless, the half cell potential was not considered yet, so it can be compensated manually by shifting the bath electrode potential down of 250mV or by applying a potentiostatic control.

6.2 IN-VITRO AND IN-VIVO CALIBRATION

This section explains the procedure to calibrate the needle gain either in artificial electrolyte (to simulate operation) or directly when implanted *in-vivo*. The procedure allows to measure the overall gain of the system in order to correctly recover gate voltage signal (and so an estimate of field potential Φ) starting from drain current data. This procedure is done before and even in-between the employment of the needle for recording, in order to keep track of device stability.

6.2.1 Setup

The setup is identical to the frequency response experiment setup.

6.2.2 Methods

Device is biased into one of the new bias points, so that information of lower cut-off frequency is now known. A sinusoidal signal in the centre band of the pixel cell is injected in the electrolyte, typically 1mV @500Hz and the response is recorded. The current signal amplitude is then related to the calibration signal and so the overall gain G is calculated and stored.

6.3 LFP RECORDING IN CORTEX

This experiment aimed to record signal from the somatosensory area C1 of the rat brain, as a result of an external stimulation. This zone is connected to precise whiskers, laying on the opposite side of the animal's head, from which it receives signal.

6.3.1 Experiment setup

The rat is positioned into a stereotaxic mount, which allows to immobilise the animal and, at the same time, to define a precise coordinate system for opening a window through the skull and positioning the needle. The rat's head is depilated and a section of skin is removed. A square window is opened on the skull with a handheld mill and the underlaying meninges are cut and opened. The needle is then inserted in position and is connected to the breakout board and then to the NI SMU board for biasing and recording.
A piezoelectric mechanical transducer is positioned near the rat's nose and is fixed to a precise whisker, which is known to be connected to the brain area in which the needle is inserted. The piezoelectric transducer allows to stimulate a single whisker with very low time constants, of the order of one millisecond. It exhibits, however, large overshoots and oscillations.
A sketch depicting the signal propagation from whisker stimulation to cortex region is shown in [].

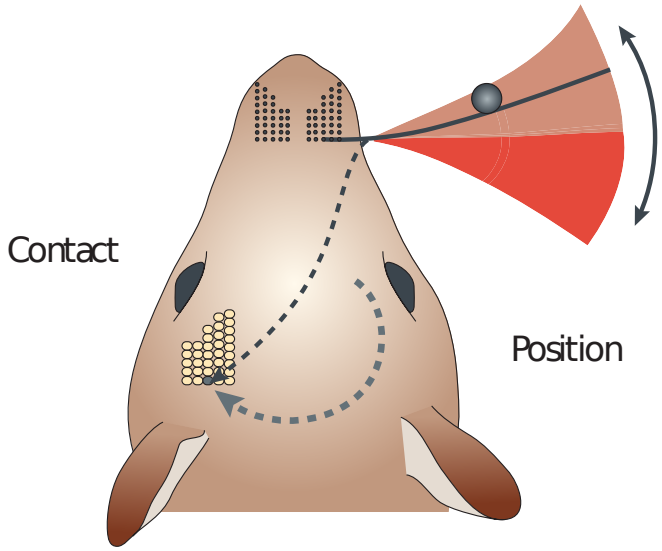

Figure 123: Sketch of response field potential of rat cortex to whisker stimulation. [Source: [Diamond *et al.*, 2008]]

6.3.2 Methods

The stimulation is applied a large amount of times (e.g. 100), while the recording intervals are synchronised with the stimulation instant. Exploiting the static (and thus repeatable) component of the resulting LFP signal, the recorded realisations of the process are averaged in order to suppress noise consistently. Stimulation and measurements are repeated while increasing the insertion depth of the needle.

6.3.3 Results

Example results are shown in [fig. 124], in which the y-coordinate is not only the signal amplitude, but the baseline of the signal represents the depth in brain (from bottom - zero depth - to top - maximum depth) at which the signal itself is recorded. It can be seen how the signal, absent at zero depth, progressively appears and changes shape, intensity and duration at different depths. The large over- and under-shooting part of the curve is the stimulation artifact, which is indeed the EMI caused by the drive signal of the piezo[1] picked up by the recording system. It was verified that this interfering signal is actually amplified by the M_{sense} FET, and is not an immunity problem of the amplifier system, because it disappears as soon as needle biasing is turned off.

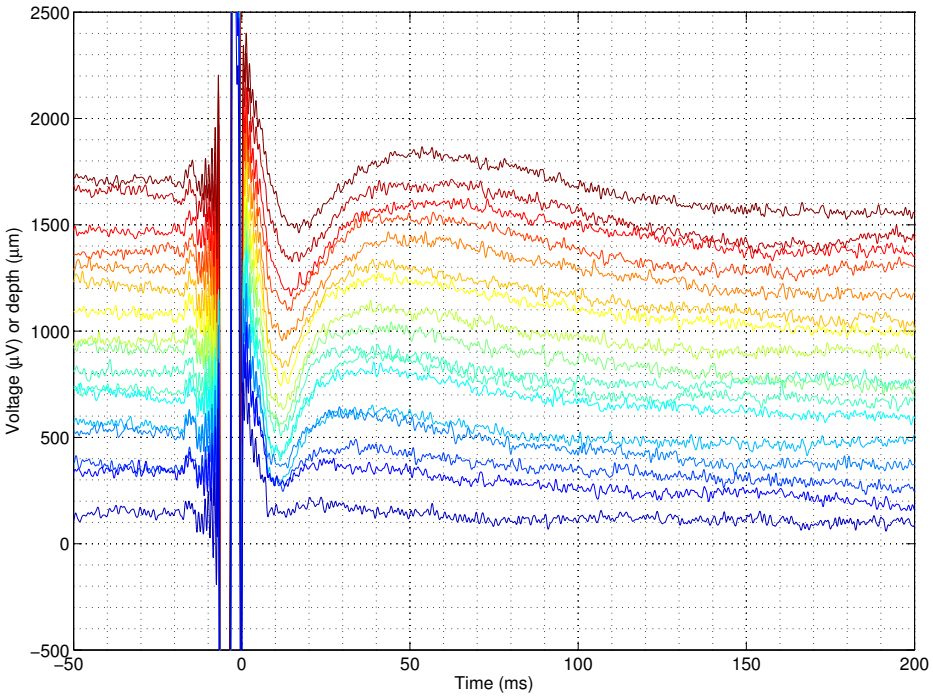

Figure 124: Response field potential in rat C1 cortex to whisker stimulation.

6.4 LFP RECORDING IN CEREBELLUM

In this experiment, the needle is used to measure LFP in cerebellum, and in particular to demonstrate that a particular stimulation protocol, named Theta Sensory Stimulation (TSS), induces long term effects on LFP response that can be attributed to synaptic long-term plasticity phenomena.

1 Which is a parallel plate capacitor driven at high impulsive voltage, or, in other words, an antenna.

6.4.1 Experiment setup

The experiment setup is pretty much the same of the C1 cortex measurements, except for the fact that needle is inserted in the cerebellum (called *CrusIIa*), so a different part of the rat's brain must be surgically operated. Needle is inserted across three layers of the cerebellum, the granular layer (GL) ($\approx$ 600µm depth), the intermediate Purkinje cell layer and the Molecular layer (ML) ($\approx$ 200µm depth). In this experiment, an air puff stimulation is used. This system uses an air flow directed to the whiskers triggered by an electrical signal by means of a fast electrovalve. Despite being less localised than piezo stimulation this has the advantage to cause less or even null stimulation artefact, as no HV pulses run into the setup itself. A photo of the setup with the rat while an experiment is running is shown in [fig. 125].

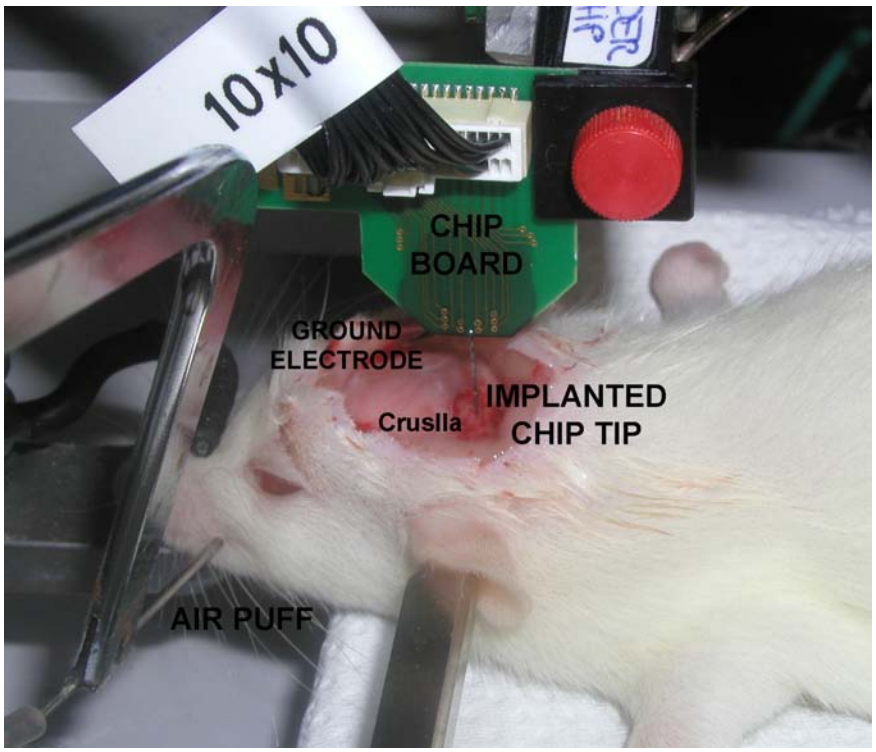

Figure 125: Needle inserted in ret cerebellum for recording.

6.4.2 Methods

The response of both GL and ML layers to a 0.1Hz 30ms on-time square wave, applied with air puff, is measured. The TSS stimulation signal (which is essentially a specifically designed pulse train) is then applied always with the air puff and then a 30' interval is waited. Finally, response of both GL and ML layers to the initial stimulus are newly recorded, and traces are accurately compared. Also in this case, within each measurement, stimulation is repeated multiple times and recording is averaged to suppress noise.

6.4.3 Results

Example results are shown in [fig. 126]. As it is spotted the signal features before and after the stimulation are different, even if they are in response to the same stimulus. (Further amplitude and timing evaluations are done to identify those variations, however they are

outside of the purpose of this chapter.) This behaviour is associated to synaptic long term plasticity: the synapses "store" an internal state as a result of the TSS stimulation and exhibit a different response, as function of this internal state, even at distance of 30 minutes.

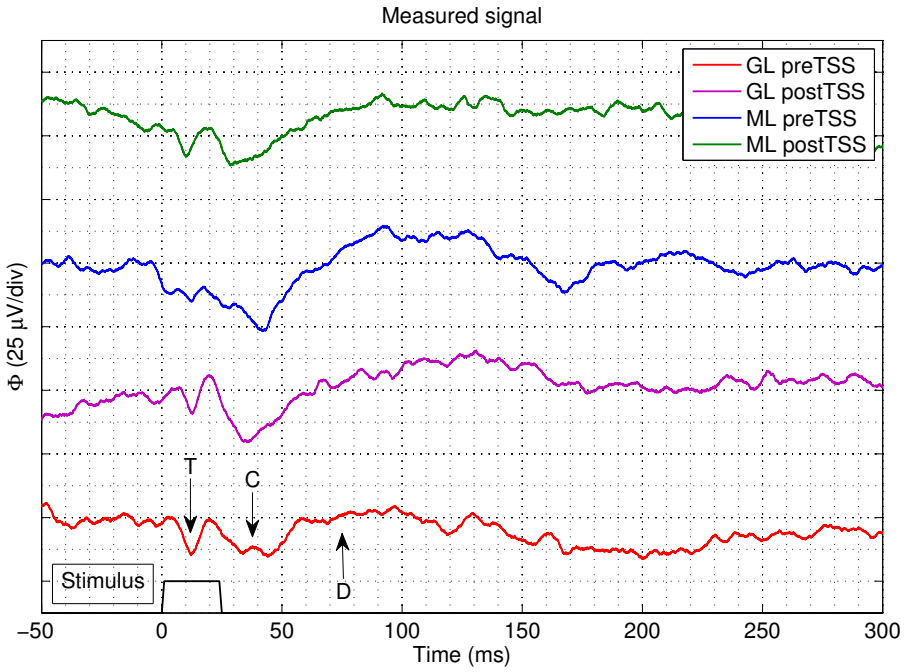

Figure 126: Response field potential in rat cerebellum to whisker stimulation, in GL and ML layers, before and after execution of TSS stimulation protocol.

6.5 COMMENTS AND REMARKS

Although the device was not found to behave as promised by the design, a smart way to use it all the same for recording was found and verified. Those are the first ever measurements done with this new CMOS technology needles and are just examples of the big potentiality of those devices. Although a review of the quality of the results in terms of noise and dynamics is not provided - being outside of the purpose of this work - it is planned. In the described experiments, some issues were encountered, such as blind pixels or very low-gain pixels which make the whole needle not usable, the reasons of which are now being investigated.

7 CONCLUSIONS

In this chapter, an evaluation of the work is carried out. Achieved goals, as long as still open issues, are discussed. The stock of the current status of the work is taken, and an overview of what are expected to be the next steps, both in the framework of this project and - more in general - in this niche of study, is given.

7.0.1 Achieved goals

The work succeeded in giving to the author a deep comprehension of the problem of investigation of neural communication though measurement of field potential. The inner working of the C-100-A/CMOS needles, and a clear understanding of their outstanding advantages on current alternative technologies for measurement of ϕ, as well as their limitations. By simulating and verifying the behaviour of such devices, the goodness of the working principle and the correct, although not ideal, implementation of the device, were proven. More in depth, it was discovered that, the biasing mechanism of the device as it was conceived should ideally work, when no parasitic elements interfere. Though an extensive device characterisation, it was shown that this behaviour is dramatically affected in terms of precision by leakage currents, which origin was mainly found on top dielectric ALD-deposited layer, although other origins are not excluded. The way to overcome this issue, which means increasing bias driving levels, causes a very bad compromise with bandwidth, due to the way in which the bias circuit of the single pixel cell works. However, a compromise between those two figures, - biasing precision and sensitivity versus bandwidth - was found with the help of other side improvements on electrolyte bias, and thus a short term solution that allows employment of the needles for in-vivo signal recording was found and successfully applied. Despite those difficulties on the path, the needle FET technology demonstrated to be superior in a wide range of aspects to current alternative technologies for field potential communication, and also to be the more promising, although many improvements are still to be done. Capacitive isolated coupling with tissue, together with active signal amplification, addressability and high integration are thought to be rare features to be found together in such a device. For the long term reprocessing or redesign of the device, both design solutions to improve noise and process solutions to reduce leakage (new dielectric candidate materials) were presented. The measured device characteristics, along with known signal properties, allowed to build the specifications of the upcoming amplifier design, which are sketched in the appendix. Finally, the experience acquired with this work allowed to create many figures of merit and tests to evaluate new solutions proposals upcoming.

7.0.2 Open issues

However, not every aspect of the device behaviour was understand - a common thing that happens when your goal is to get something to work - and the characterisation process, while giving confidence on some aspects, arouse many and many questions and doubts on other ones. For example, a kind of limitation of subthreshold biasing (even where no extrinsic leakage is present) is suggested from simulations, and still needs to be totally resolved. Then, although a reason for biasing error was found in gate electrode leakage, the different contributions of the top deposited dielectric are not totally clear, as it is strongly suspected to cause leakages towards substrate even when the device is dry. Actually, despite

the concept of those devices being really promising, it is still not clear at what limits and expense a more ideal behaviour can be achieved though redesign of device and/or process.

7.0.3 Current status of the work

Currently, thanks to the experience and information acquired, the needles can be operated to perform field potential measurements (however while acquiring only a couple of channels) as proven in the last chapter. Instrumentation and software to perform such measurements were built. A knowledge of the device ideal and real behaviour is well established, and ways to test upcoming prototypes are available, partly as an obvious byproduct of the work itself.

7.0.4 Future works

As introduced, many tasks are still opened, and they will be the main subject of investigation in the near future in the framework of this project. The characterisation and evaluation of new materials is found to be fundamental to improve devices for neural recording, together with the improvement of quality and reproducibility of the deposition processes. More than this, in this specific field of study, research pushes for higher density, lower noise, integrated signal-conditioned devices, with a special look to the opportunity to make devices for chronic application. Actually, in terms of biocompatibility and stability the features of C-100-A/CMOS needles are compatible with chronic application. Only the integration of conditioning and A/D conversion circuitry is missing, but parallel developed devices already provide this feature. Returning to the scope of the present work, but exiting for a while from that of the needle itself, the most immediate work will be the design and testing of a discrete components readout amplifier for needles providing signal conditioning and matrix multiplexing scan.

The passion of the author with respect to the topic of neural communication measurement literally exploded while the present was carried on. The author's hope is to have been able to give a good contribute to widen the observation window over such fascinating phenomena which somewhat are believed to hide the mystery or ourselves.

A READOUT DESIGN NOTES

In this appendix, starting from the parameters extracted from the characterization process and merging them with the well-known characteristic of the signal source being measured, some preliminary notes on readout amplifier design are given, with the purpose to give a reference point for future developments. Despite having used with success the breakout board + NI SMU board also for measurements, obvious limitations are the input bandwidth, the resolution and the impossibility to perform multi-channel recordings or even column multiplexing. So a custom-made amplifier is being designed from scratch for the purpose.

A.1 FUNCTIONAL REQUIREMENTS DEFINITION

The measured characteristics of the device, along with the ones of the signal, are used to extrapolate the functional - mainly electrical - requirements of the readout amplifier.

A.1.1 Channels

The amplifier should have a minimum of 16 channels (considering the largest matrix available), so that it will be possible to read from all matrix rows simultaneously.

A.1.2 Multiplexing

The amplifier shall be able to multiplex up to 16 columns. So an electronic switch array should be designed to switch each column between two values: one that disables the line (generally 0V, but not always) and one which enables the line (V_{col}). The multiplexer should have lowest possible output impedance and noise.
The desired bandwidth over the whole matrix is 5kHz, keeping a reserve upon the expected bandwidth of *single unit* signals. This means that the poll rate of the matrix is at least 10kHz, and the column scan rate is $16 \times 10\text{kHz} = 160\text{kHz}$. So the rise time (which is easier to deal with than settling time) of the multiplexer loaded with the column line must be at least 1/5th of scan period, that is $\frac{1}{5 \cdot 160\text{kHz}} = 1.25\mu\text{s}$.

A.1.3 Gain

The amplifier is in transimpedance mode, and so it is also called a current-to-voltage amplifier. As seen, a reasonable value for g_m of single pixel cell is 50µS. The maximum expected values for input signals is $\phi < 2\text{mV}$, which can be translated on a $50\mu\text{S} * 2\text{mV} = 100\text{nA}$. The amplifier needs to interface to a NI DAQ board, which have -10 to 10V input, so the desired overall gain is:

$$G = \frac{10V}{100nA} = 100G\Omega \tag{47}$$

However, the mismatch issue must not be forgot. The maximum expected mismatch current between columns is 4µA. Considering that AC coupling or offset trimming can happen only after the first transimpedance stage, assuming that a maximum output value of this stage to avoid saturation is 10V, its maximum gain needs to be $10\text{V}/4\mu\text{A} = 2.5\text{M}\Omega$. The remaining gain must be obtained by further amplification.

A.1.4 Bandwidth

It is easier to reason in the time domain when a multiplexing system is being used. Considering the expected scan rate of 160kHz, the settling time of the amplifier should match that of the multiplexer, which is 1.25µs, we should have $B = 0.35/t_r = 280\text{kHz}$ which we can approximate to 300kHz.

A.1.5 Noise

As seen, output current noise by single pixel cell is expected to be 2nArms although it has been only simulated and not yet measured. A target is to scale this noise in future devices at least down to 0.5nArms. In order to have an amplifier which noise figure is not dominating, a reasonable target for input-referred noise of the amplifier is no more than 0.1nArms.

A.1.6 Immunity

As shown, the immunity to power source conducted interferences as well as radiated interferences is critical. Despite many efforts are done to keep experiment setup as clean as possible with respect to EMI, many sources can be the same instruments used for running the experiment itself (e.g. the piezoelectric transducer).
Power source conducted interferences can be eliminated by switching to battery power, however the actual advantage against a good main filter still needs to be assessed. Cable shielding, appropriate PCB routing and chassis shielding are fundamental to improve EMI immunity of the device, along with splitting the amplifier chain in critical parts that should be separately shielded.

A.2 OPERATIVE REQUIREMENTS DEFINITION

From the operator's point of view, as already said, the use of the needle should be straightforward in order not to be a limiting factor for the good success of the experiment.

A.2.1 Interfacing

The amplifier should interface with well-established PC multi-channel acquisition boards such as those generally available from National Instruments. This means that the output signal should be limited from -10V to +10V and a custom female connector can be used in the amplifier to directly connect all input lines correctly through the NI connection cable for the board.

A.2.2 Operation

Device should be easy to switch on and off, and should have a single power button. In case it is battery-powered, the battery recharge should not prevent device operation while charging, and, in general, mechanisms to avoid full battery discharge or even breakup should be designed.

A.3 PHYSICAL REQUIREMENTS DEFINITION

Amplifier dimensions and weight is not a real concern for acute experiments. It is ally required for the amplifier to fit into the setup bench, so the best choice is to locate it into a 9" rack chassis. An head stage, containing only the first amplifier stage of each channel, could be made and located very near to the needle, in order to avoid interference picked up by interconnecting cables.

A.4 NOTES

All those information, when wisely interpreted, constitutes the basis point for the development of a high performance amplifier for the C-100-A/CMOS needles.

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Padova, 1 dicembre 2014

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