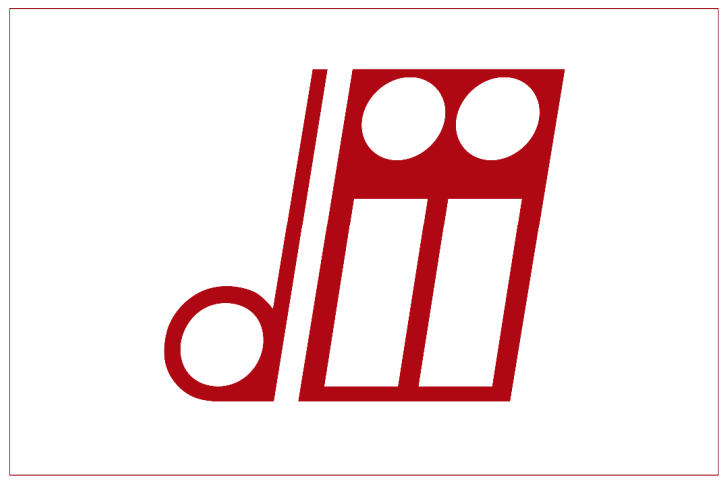

UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Dipartimento di Ingegneria Industriale
Fachgebiet Energiewandlungstechnik (Technische Universität München)
Corso di Laurea Magistrale in Ingegneria dell'energia Elettrica

TESI DI LAUREA MAGISTRALE IN
INGEGNERIA DELL'ENERGIA ELETTRICA

DEVELOPMENT OF A TEST BENCH FOR CASCADED H-BRIDGE CONVERTER

Sviluppo di un banco prova per inverter multilivello CHB

RELATORE A PADOVA: Prof. Andriollo Mauro
RELATORE ALL'ESTERO: Prof. Herzog Hans-Georg
SUPERVISORE ALL'ESTERO: M. Sc Lahlou Taha

LAUREANDO: Roman Michele

ANNO ACCADEMICO 2015-16

UNIVERSITÀ DEGLI STUDI DI PADOVA

UNIVERSITA' DEGLI STUDI DI PADOVA

Dipartimento di Ingegneria Industriale DII

Fachgebiet Energiewandlungstechnik (Technische Universität München)

Corso di Laurea Magistrale in Ingegneria dell'Energia Elettrica

DEVELOPMENT OF A TEST BENCH FOR CASCADED H-BRIDGE CONVERTER

Sviluppo di un banco prova per inverter multilivello CHB

Relatore a Padova: Prof. Andriollo Mauro

Relatore all'estero: Prof. Herzog Hans-Georg

Supervisore all'estero: M. Sc Lahlou Taha

Roman Michele

1105633

Anno Accademico 2015/2016

Sommario

Questa tesi descrive lo sviluppo di un banco prova per un inverter multilivello cascaded H-bridge (CHB) che ha la funzione di connettere un sistema di accumulatori con la rete e di scambiare energia in base al controllo. Il banco prova consiste in un sistema trifase costituito da inverter a ponte intero che fungono da unità di base. Il progetto completo prevede per ogni fase otto moduli, ciascuno alimentato da un sistema di batterie a 48 V. Questa configurazione permette di connettere il sistema di accumulo con la rete. Inoltre è possibile, sfruttando la modularità ed il trasformatore variabile collegato tra rete e banco prova, regolare la tensione e sviluppare il progetto 'step by step'.

Per il corretto funzionamento del sistema è stato necessario eseguire un'analisi incrociata tra la scelta della frequenza di switching ed il dimensionamento del filtro tenendo conto delle peculiarità del sistema. Con i risultati ottenuti, è stato possibile individuare la combinazione ottimale da adottare appena sarà disponibile il nuovo filtro di rete: in via provvisoria è stata utilizzata una configurazione di compromesso. Essa permette il buon funzionamento dell'inverter, con il filtro già installato e una maggiore frequenza di switching, pur presentando qualche svantaggio rilevabile in fase di raccolta dati.

La nuova configurazione ha permesso di eseguire delle misure sperimentali rilevanti al fine di migliorare il modello usato nelle simulazioni. A tale scopo è stato sviluppato un comune work cycle, semplificando la raccolta dati e la comparazione in diverse condizioni di lavoro. In fase di confronto è stato constatato come la presenza del trasformatore, che si trova tra la rete e l'ingresso del banco prova e non considerato nel modello per le simulazioni, sia molto rilevante. Per ovviare a questa discrepanza, è necessario tener conto dell'impedenza di corto circuito del trasformatore per sintetizzare più fedelmente la potenza di corto circuito della rete. Inoltre nel modello adottato sarà necessario considerare batterie reali, riferendosi alla caratteristica di scarica in rapporto anche all'elevata corrente nominale del sistema.

In conclusione, nonostante gli sviluppi apportati, non è stato possibile eseguire le prove sperimentali per tutte le configurazioni previste (con otto moduli per fase). A tal scopo risulta raccomandabile: la sostituzione dei moduli con una nuova più efficiente ed affidabile versione; la sostituzione del filtro di rete con l'utilizzo di una frequenza di switching ottimale; lo sviluppo di un battery management system per gestire in modo appropriato il sistema di accumulo.

Abstract

Extensive research have been done in the field of power converters, in order to face the decentralization of the production and to integrate the new numerous renewable energy plants. Among these, multilevel converters promise good power quality and low switching losses than ordinary and commonly used three level inverters. Therefore, this thesis aims to develop a test bench for cascaded H-bridge converter which has the task of connecting an energy storage system with the grid. With the test bench results it will be possible to improve the simulation model for an easier develop of the seventeen level cascaded H-bridge prototype from EEBatt team.

Contents

1 Introduction

1.1 Motivation

Due to the recent high penetration of the decentralized energy production and environmental problems, many investigations have been started to improve the efficiency of the electrical systems. Indeed, a more efficient energy use brings numerous advantages, such as: lower energy prices, less dependency on fossil ores, environmental benefits, enrichment of local areas, improvement of security and of service quality [15].
More and more, energy storage systems combined with power electronic converters are becoming a suitable solution to energy management. Having overcome the technological problems related to control complexity and reliability, the multilevel converters are now a mature technology. Among the available topologies, the cascaded H-bridge converter has the best characteristics in terms of efficiency, modularity, number of components, control complexity and fault tolerance, making this family the strongest candidates for most low and medium voltage applications [12] [14] [15] [29]. This thesis reports the development of a test bench for cascaded H-bridge that connects a energy storage system with the grid. This converter is a part of a wider project from the EEBatt team [8] of the Technical University of Munich.

1.2 Overview and methodology

The test bench consists of a three phase cascaded H-bridge converter, which will have eight modules for each phase. On the DC-side the modules will be powered by a 48 V battery, which allows it to connect to the grid.

The system is schematically represented in Figure 1.1.

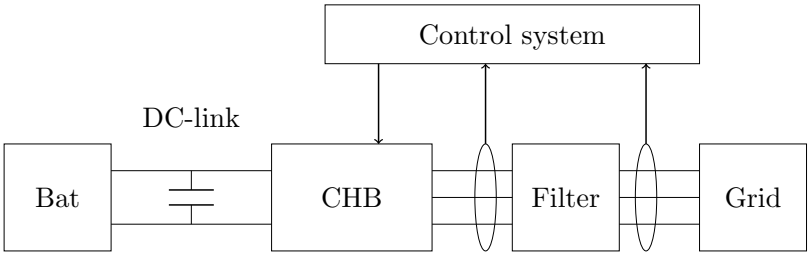

Figure 1.1 – Basis scheme of the CHB test bench

In the beginning, the test bench has two H-bridges installed per phase (CHB 5 levels) and each of them is feeded only by a 12 V battery. The work details the development of the test bench, implementing and testing the new level configurations.
Due to the modularity of the system, it has been possible to proceed step by step, optimizing the system for each new configuration. The new configuration is then analized and the results compared with the simulations in [20].

During the development of the test bench, many drawbacks have been faced. The main problems have been the reliability of the modules and of the measurement system.
Furthermore, the filter and the switching frequency have been important to the well-functioning of the inverter, and had to be carefully chosen.

1.3 Report description

The thesis is divided into five chapters. After the introduction, the second chapter reports the theoretical notions at the base of the thesis, which is useful for understanding how the test bench works. Chapter three gives an overview of the test bench, highlighting the more important aspects and characteristics in order to have a complete and satisfactory functioning report. Relevant details such as: project design steps and methodologies are also included. Chapter four includes the results obtained from the experimental measures and the comparison with the simulations previously done. Chapter five concludes the thesis and give recommendations for the future development of the test bench.

2 Theoretical basis for the test bench

In this Chapter are reported the theoretical basis necessary to comprehend the functioning of the test bench, to understand the operations done in Chapter 3 and the results in Chapter 4. In particular there are notions about: the matching of the grid with energy storage system, a review about the H-bridge and multilevel converters, a report about the control technique used and the modulation schemes, an overview of the most relevant power quality and power losses aspects involved in the model and notions about the energy storage system and the filter design.

2.1 Control of active and reactive power in electrical systems

In this Section is reported the power flow control theory. These concepts are at the base of the electrical systems and explain how it is possible to inject or to absorb power in the grid using a generation system.
In the past this operation was possible just through rotating generators, but nowadays with the development of the power electronic, it is possible to perform the connection even if in one side there is a DC source, using an inverter.

Figure 2.1 shows the schematic connection of the grid with a energy storage system through the use of a generic three phase inverter. Indeed, if well led and synchronized, an inverter powered with an energy storage system can synthetize a suitable waveform.

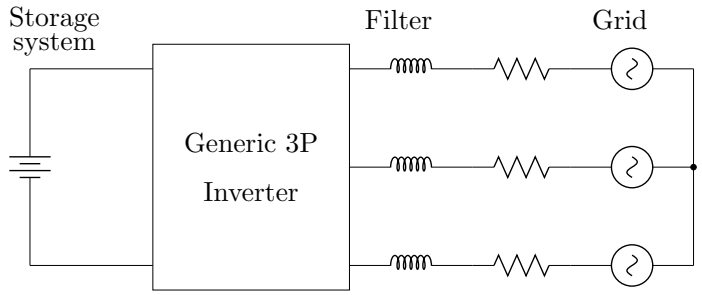

Figure 2.1 – Scheme of the coupling between a system of energy storage and the grid through a generic inverter

To perform a proper coupling between an external system with the grid, it is mandatory to satisfy some important specifications. Considering that the external system has to be integrated with the grid, and not vice versa, it has to be complied with the values of the grid. In particular, the power output of the synchronous generator/inverter must have [22]:

- Identity of the rms values;
- Identity of frequency;
- Concordance of phase.

Once all these requirements are satisfied it is possible to connect the two systems.

To understand instead how the power flows are controlled, it is necessary to summarized the problem with the equivalent circuit in Figure 2.2, which is made of: the external power source, the grid and an inductance as filter (resistance is neglected):

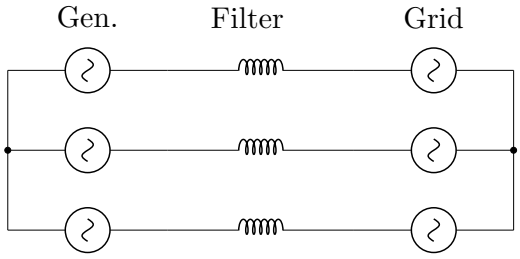

Figure 2.2 – Equivalent three phase coupling circuit between an external power source and the grid

Considering that the scheme shown in Figure 2.2 is symmetric and equilibrated, it can be simplified with the related single phase equivalent circuit in Figure 2.3.

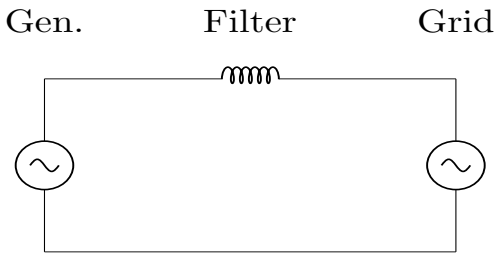

Figure 2.3 – Equivalent single phase coupling circuit between an external power source and the grid

The differential equation, associated at the circuit in Figure 2.3, results (2.1).

$$e(t) + L\frac{di}{dt} - v(t) = 0 \tag{2.1}$$

Being sinusoidal values, it is possible to study the problem in the phasor frame utilizing the Steinmetz's transformation. If the matching conditions are satisfied the voltage phasors generated at the output of the inverter and the ones coming from the grid are perfectly aligned and rotating with same speed. In these conditions, the coupling is possible but, if performed, there is not power flow toward one side or the other.
Hence considering the phasor of the grid fixed (because it is related to the whole electrical system), to obtain a power flow is necessary to change the phasors of the external generator, anticipating or delaying the phase, either increasing or decreasing the amplitude. A new

differential voltage phasor is so created due to the difference with the others, and a power flow now exists. The flowing current in the circuit is calculated as (2.2).

$$\vec{I} = \frac{\vec{V}_{gen} - \vec{V}_{grid}}{j\omega L} = -jI_L \tag{2.2}$$

Analyzing the four cases it is possible to see that, changing the phase of the $\vec{V}_{gen}$ an active power flow is obtained, while modifying the amplitude a reactive power flow results.

Active Power In the vector diagrams, in Figure 2.4 and Figure 2.5, is shown how the active power flows are conveyed through the control of the vector $\vec{V}_{gen}$.

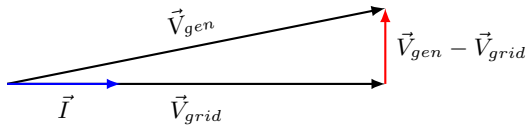

Figure 2.4 – Active power from the generator to the grid P>0, Q=0.

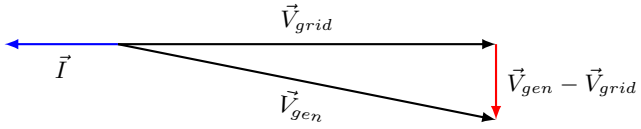

Figure 2.5 – Active power from the grid to the generator P<0, Q=0.

Reactive Power In these next vector diagrams, in Figure 2.6 and Figure 2.7, it is shown how the reactive power flows are conveyed through the control of the vector $\vec{V}_{gen}$.

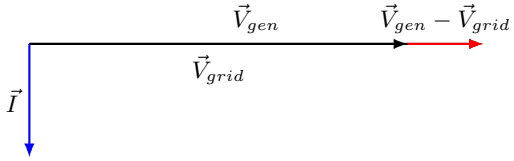

Figure 2.6 – Reactive power from the generator to the grid P=0, Q>0. The generator is seen, from the grid, as a capacitor.

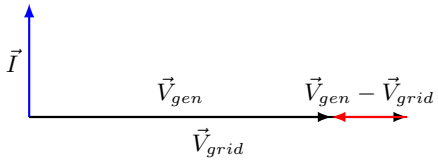

Figure 2.7 – Reactive power from the grid to the generator P=0, Q<0. The generator is seen, from the grid, as an inductor.

2.2 H-bridge converter and PWM modulation

In order to understand how a CHB converter works, it is important to have a presentation of the simple H-bridge, which is the basic module of this kind of converter. A H-bridge consists of four switching devices (in the project MOSFETs are used) and four diodes connected in anti parallel. The basic scheme is shown in the Figure 2.8:

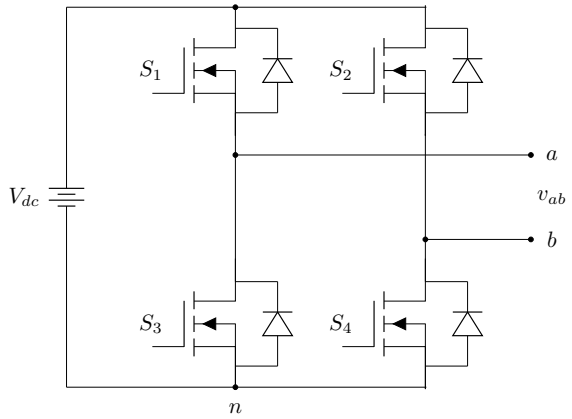

Figure 2.8 – Scheme of a H-bridge

To avoid short circuits, it is necessary that the switches in the same branch are led in opposite way. This means that: if one is closed the other in the same branch must be open. Having at the same time the switching S_1 and S_4 closed (consequentially S_2 and S_3 are opened), it is obtained at the node a and b the voltage V_{dc}. Vice versa with S_2 and S_3 closed the output voltage is $-V_{dc}$. Instead, if they are closed at the same time, S_1 and S_3 or S_2 and S_4, the output voltage is null.
Table 2.1 summarized the output voltage according to the switching states.

Table 2.1 – Switching states of a H-bridge

Output Voltage	Gate Signal	
v_{ab}	S_1	S_2
0	1(0)	1(0)
$-V_{dc}$	0	1
V_{dc}	1	0

To lead a H-bridge, it is necessary to send a gate low voltage signal to each switching device in order to get the desired output voltage. One way to obtain the drive signal is through the comparison of two different waveforms; if one is bigger than the other the signal is high, vice versa it is null.
The fixed signal, that is the one compared with the signal that has to be achieved, is called carrier and it consists of a periodic triangular waveform of higher frequency. The other signal, that is the object waveform, is called modulator.
If the modulator is a constant signal, the H-bridge will work as a DC-DC converter, while

if it is a sinusoidal signal, an alternated output (for which the fundamental is a sinusoidal signal) is obtained. When the modulator is a sinusoidal waveform, the result is a signal made of pulses of different width, commonly called PWM (pulse width modulation) [4] [23].

The amplitude modulation index m_a is defined as the relationship between modulator v_{mod} and v_{car} carrier amplitude as in (2.3).

$$m_a = \frac{v_{mod}}{v_{car}} \tag{2.3}$$

The value of amplitude of the fundamental harmonic for different values of m_a is in (2.4).

$$\begin{cases} v_1 = m_a V_{dc} & m_a \leq 1 \\ V_{dc} \leq v_1 \leq V_{dc}\dfrac{4}{\pi} & m_a > 1 \end{cases} \tag{2.4}$$

The frequency modulation index m_f, defined as the relationship between modulator f_{mod} and carrier frequency f_{car}, is in (2.5).

$$m_f = \frac{f_{mod}}{f_{car}} \tag{2.5}$$

The harmonic contents, calculated with the Fourier decomposition (Paragraph 2.6.1), is defined in Table 2.2. The table is given for $m_a = 1$ and m_f entire.

Table 2.2 – Amplitude of the harmonics produced of a H-bridge with PWM m_f entire [23]

Harmonic order m_f	$\frac{(V_o)_h}{V_d} = m_a = 1$
$1^{st} fundamental$	1
m_f	0.601
$m_f \pm 2$	0.318
$m_f \pm 4$	0.018
$2m_f \pm 1$	0.181
$2m_f \pm 3$	0.212
$2m_f \pm 5$	0.033
$3m_f$	0.113
$3m_f \pm 3$	0.062
$3m_f \pm 4$	0.157
$3m_f \pm 6$	0.044
$4m_f \pm 1$	0.068
$4m_f \pm 3$	0.009
$4m_f \pm 5$	0.119
$4m_f \pm 7$	0.050

As indicated in (2.4), the highest value of the fundamental is thus reached with an over modulated configuration also called square wave functioning. On the other hand, for this work condition, the harmonic spectrum includes low frequency harmonics as explained in [4] [23].

Unipolar modulation

The PWM signal can be bipolar or unipolar. The first one is characterized by a single modulator signal, while the second one has two modulator signals, with one opposite of the other.
The advantages achieved with the unipolar modulation are [4] [23]:

- Double switching frequency;
- Elimination of the harmonic 2 m_f;
- Variation of v_{ab} equal to V_{dc} instead of $V_{dc}/2$.

Being used in the project the unipolar modulation for leading the switching devices of each H-bridge, in this paragraph is shown the typical result achievable with this kind of PWM modulation.
The carrier, as already underlined, is compared with the reference signal and with its opposite. An example, considering a value of m_a=1 and m_f=20 (f_m=50 Hz and f_s=1 kHz), is shown in Figure 2.9.

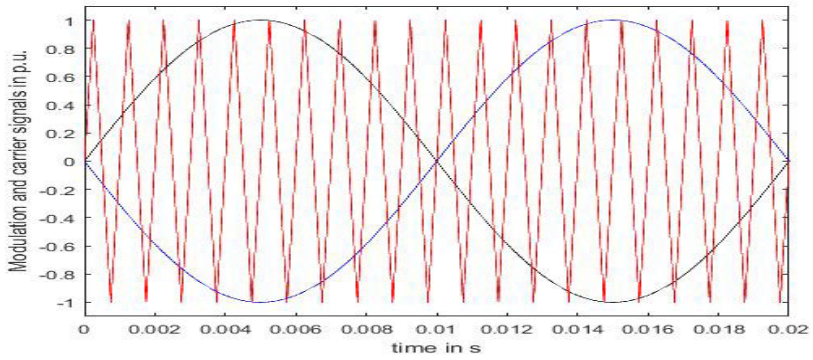

Figure 2.9 – Unipolar PWM for H-bridge

Having as reference the scheme in Figure 2.8, and as modulator and carrier signals the ones in Figure 2.9, the voltage obtained is the voltage v_{ab} that is the potentials difference taken from the clamps a n and b n. The output waveforms are shown in Figure 2.10.

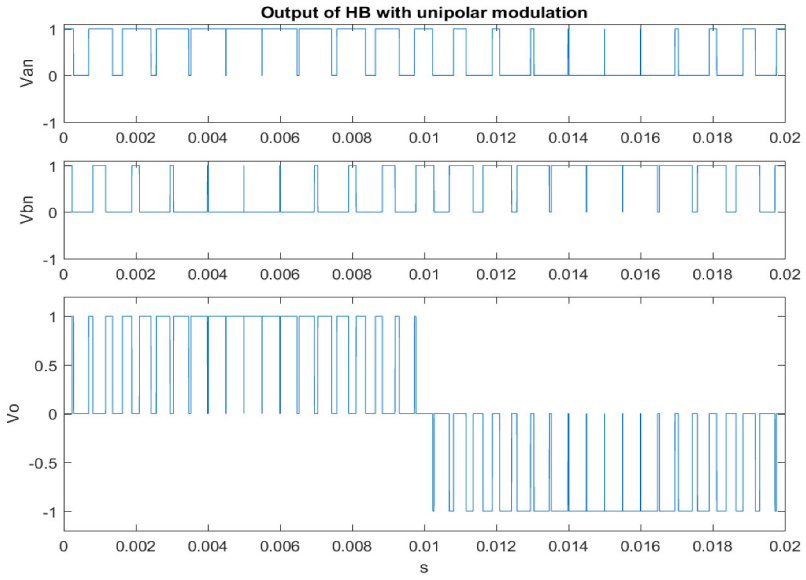

Figure 2.10 – Output voltage of a H-bridge $V_o = v_{an} - v_{bn}$

The harmonic spectrum, calculated through the Fourier decomposition 2.6.1, and readable from Table 2.2, results as shown in the graph of Figure 2.11.

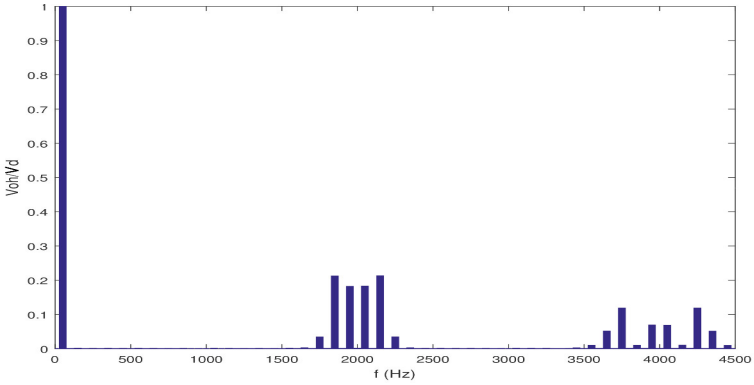

Figure 2.11 – Harmonic content of a H-bridge led with unipolar PWM

2.3 Multilevel inverters topologies

In this section are illustrated the most important topologies of the multilevel inverters. Recently, they are taking hold as a concrete alternative to the common two and three level inverter. This fact is due to high quality waveform, low switching losses, high voltage capability and low electromagnetic compatibility (ECM) [12] [14] [27].

The concept at the base of these converters is the generation of a stepped waveform overlaying the output contributes of more stages. The aim is to synthesize better the sinusoidal wave-

form, reducing the total harmonic distortion (THD) and the power losses. The drawbacks of multilevel converters, which have not allowed a quick development are: the control complexity, the implementation of the modulation method and the reliability [15].
A general way to represent a multilevel converter is shown in Figure 2.12.

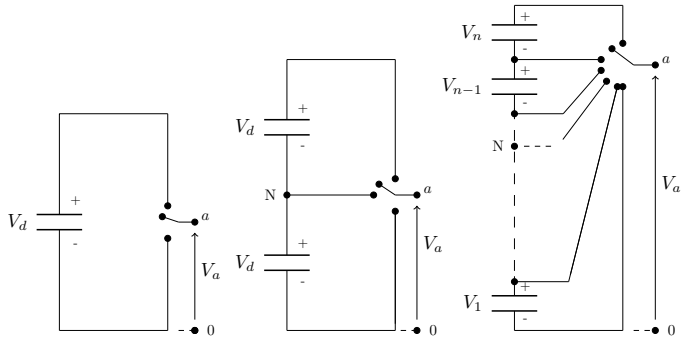

Figure 2.12 – One leg of an inverter with two levels, three levels, and n levels [27].

The general associated output is the stepped waveform shown in Figure 2.13.

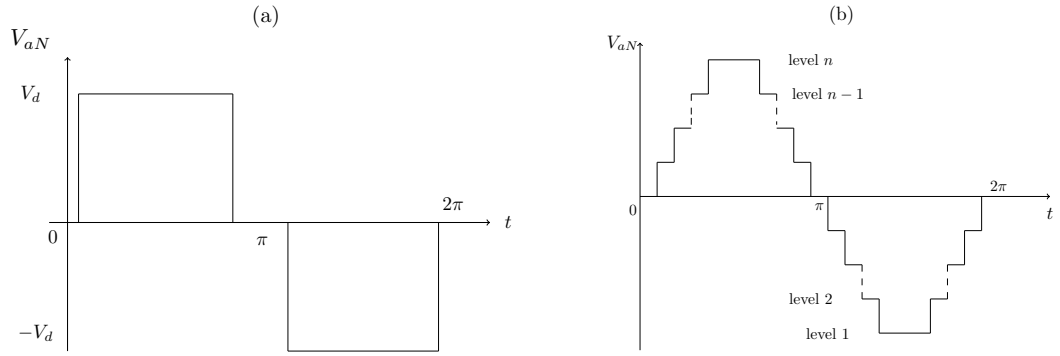

Figure 2.13 – Generalized output voltage of a three level (a) and of a multilevel (b) inverter

To define the levels number of a multilevel output waveform, it is enough to count the voltage steps, from the lower to the higher, including the null step. If the considered system is a three phase and the line to line voltage is measured, the number of steps countable will be $2n - 1$, with n number of level of the multilevel. For instance, a 17 level converter counts 33 voltage steps in the line to line measure.

Even if the width and the high of the steps can be modify, usually the high of the step is the same and the width of it is set according to the desired waveform [26]. A different level of the singles step brings the presence of not expected harmonics. Thus, it is important to monitor the voltage at the DC link to avoid the problem.

The most common and practically used multilevel converter topologies are:

- Neutral point clamped converters (NPC);

- Flying capacitors converters (CF);
- Cascaded H-bridge converters (CHB)

2.3.1 Neutral point clamped converters (NPC)

The NPC converters are the most used among the high power applications (up to 6 kV) [12]. In Figure 2.14 is shown the base scheme of a three and five level NPC converter.

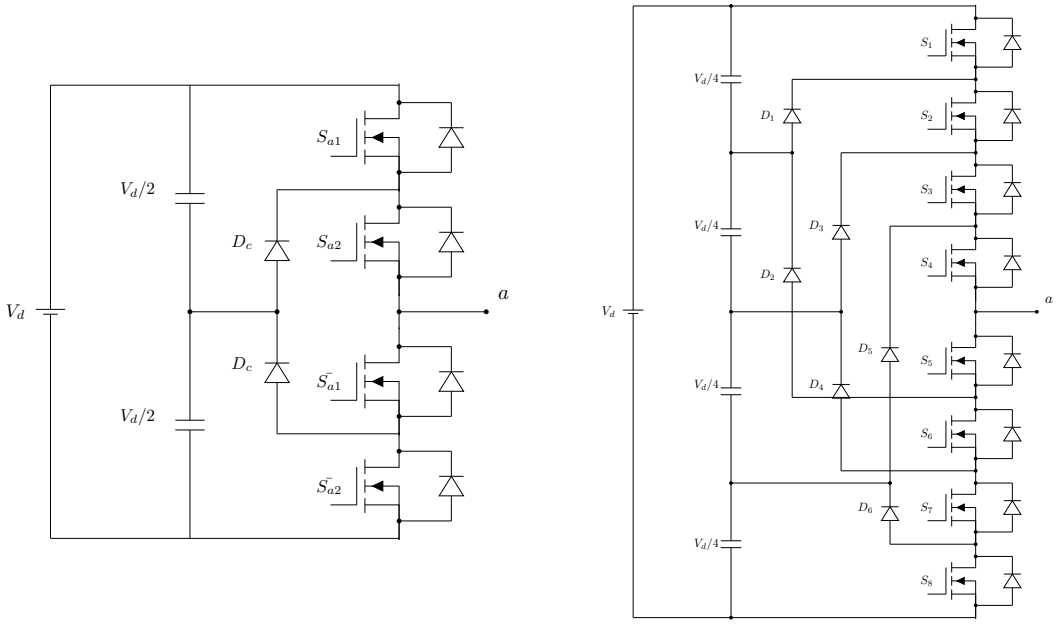

Figure 2.14 – Base scheme of a three and five level NPC converter [11]

The voltage applied at the input is divided among the capacitors according to the number of levels. The middle point is defined as neutral point. The voltage at the output changes among $V_d/2$, 0 and $-V_d/2$ in the three level; while varies among $V_d/2$, $V_d/4$, 0, $-V_d/4$ and $-V_d/2$ in the five level topology according to the statement of the switches. The behaviour is reported in Table 2.3.

Table 2.3 – Output of a three level NPC converter according to the switching states

Output Voltage	*Gate Signal*	
v_{an}	S_{a1}	S_{a2}
$V_{dc}/2$	1	1
0	0	1
$-V_{dc}/2$	0	0

The advatages of the NPC are [13]:

- Not necessity of the filter, if the number of the levels is big enough;
- High efficiency because the switching devices are led at the fundamental frequency;
- Reactive power flow can be controlled.

The disadvantages instead are [13]:

- Large number of clamping diodes is required when the level grows;
- It is difficult to implement a high level NPC because of the clamping diodes recovery time [12];

2.3.2 Flying capacitors converters (FC)

The flying capacitor converters, otherwise from the NPCs, use capacitors to clamp the voltage. The characteristic name, derives from the fact that the output voltage floats respect to the ground potential. The base schemes of a flying capacitors converters are illustrated in Figure 2.15.

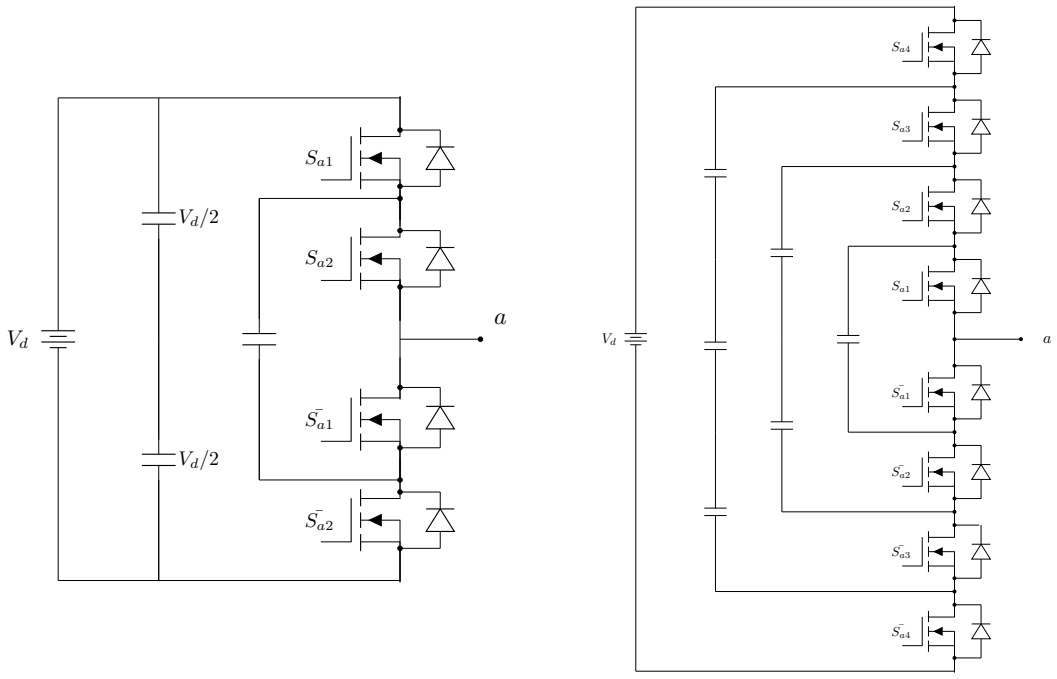

Figure 2.15 – Base scheme of a three and five level FC converter [11]

Choosing the state of the switches is possible to obtain different voltage levels. For the three level considered, it is verify what reported in Table 2.4.

Table 2.4 – Switching states of a Flying Capacitors multilevel inverter

$Output\ Voltage$	$Switching\ states$				i_c
	S_1	S_2	S_3	S_4	
$\frac{V_d}{2}$	1	1	0	0	0
0	1	0	1	0	$-i$
0	0	1	0	1	i
$-\frac{V_d}{2}$	0	0	1	1	0

The advantages of these converters are [13]:

- High redundancy for voltage levels (many voltage level can be achieved with different switching states);
- Not necessity of the filter if the number of the levels is big enough;
- Active and reactive power flow can be controlled.

On the other hand, the disadvantages of the FC are [13]:

- A large number of capacitors is required with the growth of the level;
- At the beginning the charge of the capacitors has to be regulated;
- Difficult control with high losses in the active power transmission.

2.3.3 Cascaded H-bridge converters (CHB)

The cascaded H-bridge converter consists of more H-bridge connected in series along the AC-side, allowing in this way to sum the singles contributes.

In Figure 2.16 is reported the mono-phase cascaded H-bridge scheme.

The main advantages of the CHB are [12] [27]:

- Low number of components compared with other topologies;
- High modularity of the multilevel;
- Soft switching methods can be used to avoid losses in the snubber [6].

The main drawbacks of the CHB is that it needs isolated DC sources for each H-bridge.
The relevant advantages of this type of topology affirms it at the center of the actual research. In particular: it requires the lowest number of components and the high modularity allows to reach a relevant number of levels (not easy with the other topologies).

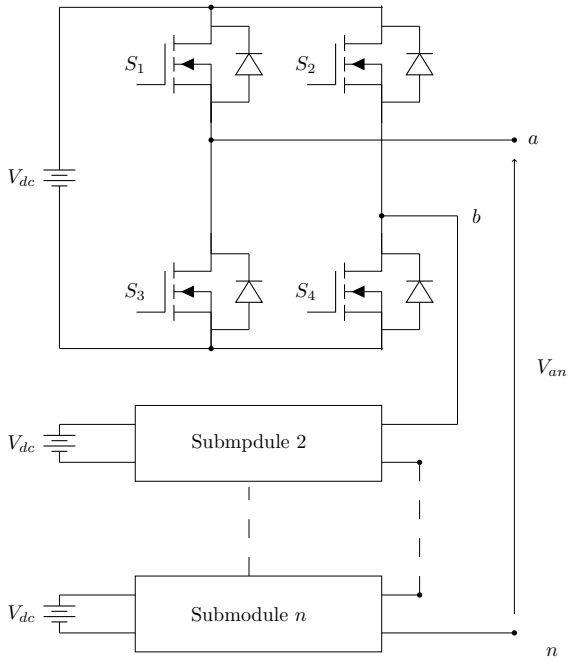

Figure 2.16 – Scheme of a cascaded H-bridge

2.4 Control Technique

As underlying in the beginning of the thesis in Section 2.1; when an external power source have to be connected with the grid, some technical specifications have to be satisfied to obtain a proper integration of that source.
These specifications are provided from the control system, with which it is possible to synchronise the voltage phasors and decide if move power flow. Setting a certain value of reference current, the external source voltage phasors are modified having in this way the desired power flow. Hence, to perform the control are necessary some measures for the synchronization system.

2.4.1 Vector transformations

In order to understand this method is necessary to introduce some theoretical basis on space vector transformations. Through these transformations it is possible to change the reference frame of the voltage and current phasors. Through the Clarke transformation the vectors are represented in a stationary frame (fixed with the stator if it is considered the example of a rotating machine); while, passing from the Clarke representation to the Park one it is obtained the configuration in a rotating frame (fixed with the rotor always thinking to the rotating machine). The main advantage of this approach is the possibility control separately active and reactive power [5]. Figure 2.17 illustrates the different frames.

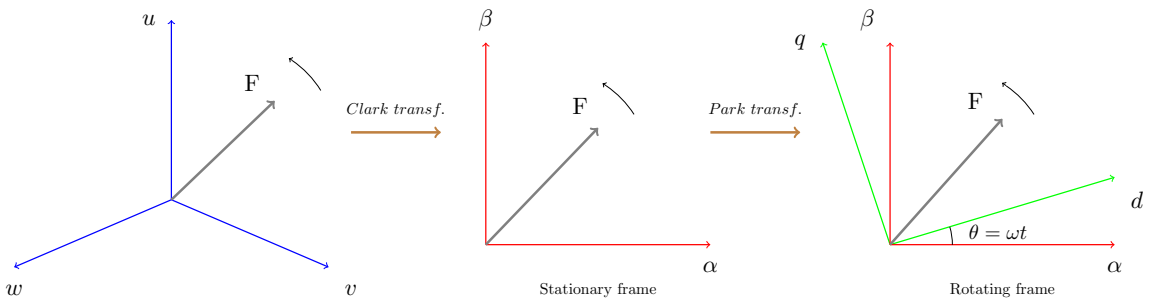

Figure 2.17 – Space vector in different frames [4]

The following matrices describe the Clarke (2.6) and Park (2.7) transformations starting from the conventional frame:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.6}$$

The constant 2/3 is present inasmuch this transformation is not conservative for the power. On the other hand, it is conservative for the amplitude values [5].

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos(\theta) & -sin(\theta) \\ sen(\theta) & cos(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.7}$$

In order to operate this transformations to achieve the dq decomposition, it is required the information of the angle θ, angle between the $\alpha\beta$ and the dq axes. This duty is usually made by a phase locked loop block, which having as input the voltage values gives as output the angle θ useful for the transformation. A deeper explanation is reported in 3.6.

Considering the equivalent electrical scheme 2.18, obtained as reported in Section 2.1.

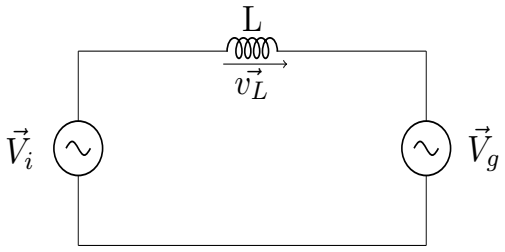

Figure 2.18 – Equivalent single phase coupling circuit between an external power source and the grid

The differential equation associated at circuit in Figure 2.18 results (2.8).

$$V_i(t) + R_f i + L_f \frac{di}{dt} - V_g(t) = 0 \tag{2.8}$$

Operating the Clarke and Park transformations, as shown before it is achieved the dq decomposition in (2.9).

$$\begin{cases} V_{i,d} = I_d(R_f + L_f s) - 2\pi f L I_q + V_{g,d} \\ V_{i,q} = I_q(R_f + L_f s) - 2\pi f L I_d + V_{g,q} \end{cases} \tag{2.9}$$

2.4.2 Voltage oriented control

This method is characterized by having the phasor of the voltage space vector oriented in the direction of the d-axis, in the dq-frame representation. With this configuration, as it is possible to see in Figure 2.19 is performed a direct control to the active and reactive power. Indeed, increasing the value of i_d it is achieved an increment of active power, while increasing the value of i_q it is obtained an increment of reactive power [27].

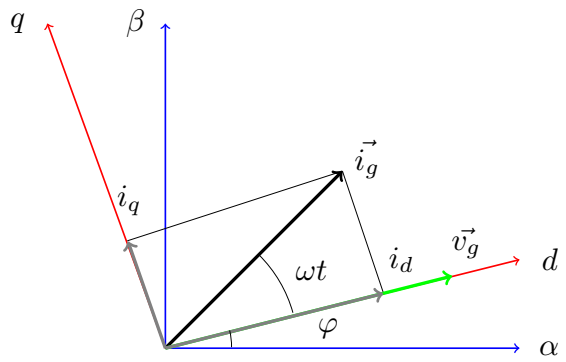

Figure 2.19 – The space vector of the voltage is in the same direction of the d-axis [27]

The dq decomposition is not conservative for the power [5] so the active and the reactive power are scaled of a constant 3/2 as reported in (2.10).

$$\begin{cases} P = \frac{3}{2} V_d I_d \\ Q = -\frac{3}{2} V_q I_q \end{cases} \tag{2.10}$$

2.4.3 Stability and system response

In order to have stability and good system response, a closed loop for each axes is implemented. A PI controller will be used in order to have good dynamic response and low steady state error.

The blocks schemes are reported in Figure 2.20 and 2.21.

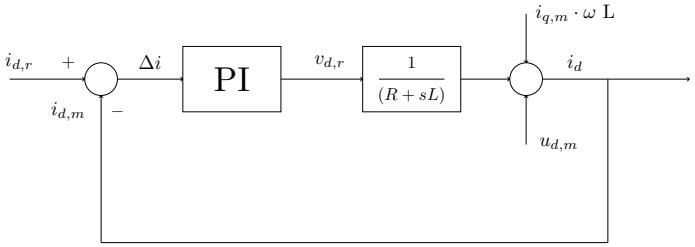

Figure 2.20 – Current control system for d axis

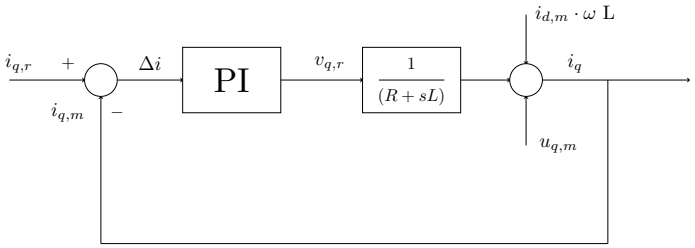

Figure 2.21 – Current control system for q axis

If the current reference value changes, the error at the input of the controller is different from zero. This error, integrated from the PI controller gives a voltage increment at the voltage vector. Thus, having a new voltage vector, considering the system equations in the dq-frame (2.9), a power flow come to exist as explained in Section 2.1.
This functioning process is true for positive or negative reference values and for d or q axes.

The stability of the system is determined from the study of the transfer function of the system. For instance, if is considered a generic system made of the controller, the inverter and the electrical circuit, as reported in Figure 2.22, the transfer function is calculated as in (2.11).

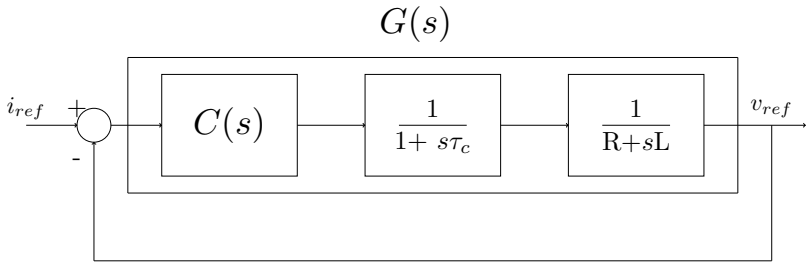

Figure 2.22 – Closed loop scheme of a generic conversion controlled system

$$Y_{tf}(s) = \frac{G(s)}{1 + G(s)} \tag{2.11}$$

If the roots of the poles of $Y_{tf}(s)$ lay in the negative real part, the system is stable; otherwise the system results instable. In Figure 2.23 are reported the possible response that the system

can have according to the roots of the transfer function.

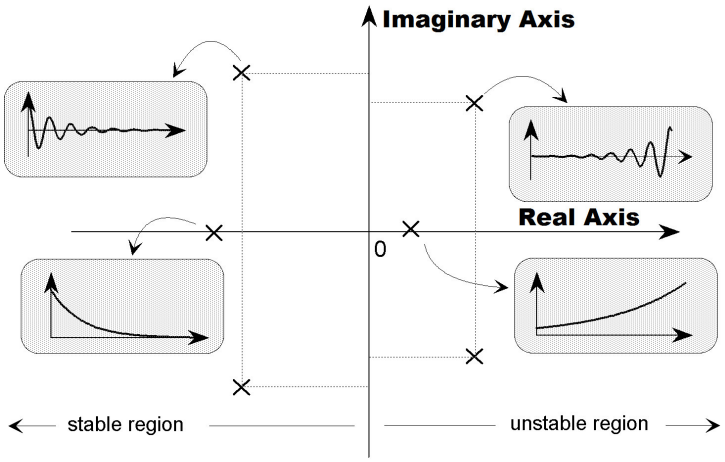

Figure 2.23 – System response according to the transfer function roots [24]

2.5 Multicarrier modulation schemes for cascaded H-bridge

To lead the modules of a cascaded H-bridge the PMW modulation is used. However, having more modules, which need of different control, it is necessary to provide a proper signal according to the number of modules in order to achieve the stepped output.
This PWM modulation scheme is called multicarrier PWM and, as the name said, it is characterized by a number of carriers equal to the number of modules used [4].
The multicarrier PWM schemes, explained in deep in Paragraph 2.5.1 and 2.5.2, are:

- Phase shift PWM;
- Level shift PWM.

2.5.1 Phase shifted PWM

This technique has a number of carriers equal to $m-1$ (m number of the levels) and their are shifted each other of an angle of:

$$\varphi_c = \frac{360}{m-1} \tag{2.12}$$

This angle allows to achieve the minimum distortion level [4]. The angle is such that the half period of the modulator waveform is divided in equal parts according to the number of modules. An graphical example is reported in Figure 2.24.

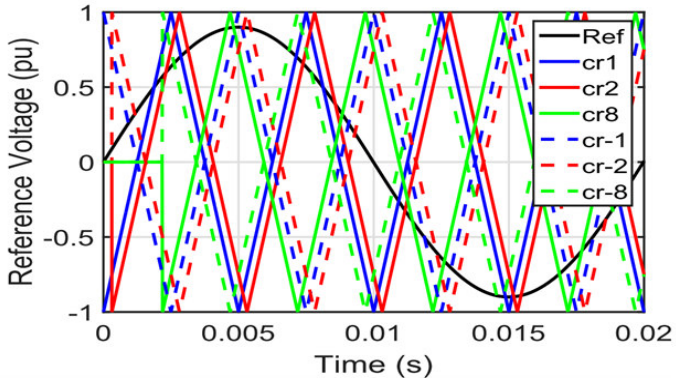

Figure 2.24 – Multicarrier phase shift PWM for a 17 level CHB [20]

The harmonics content is shown in Figure 2.25.

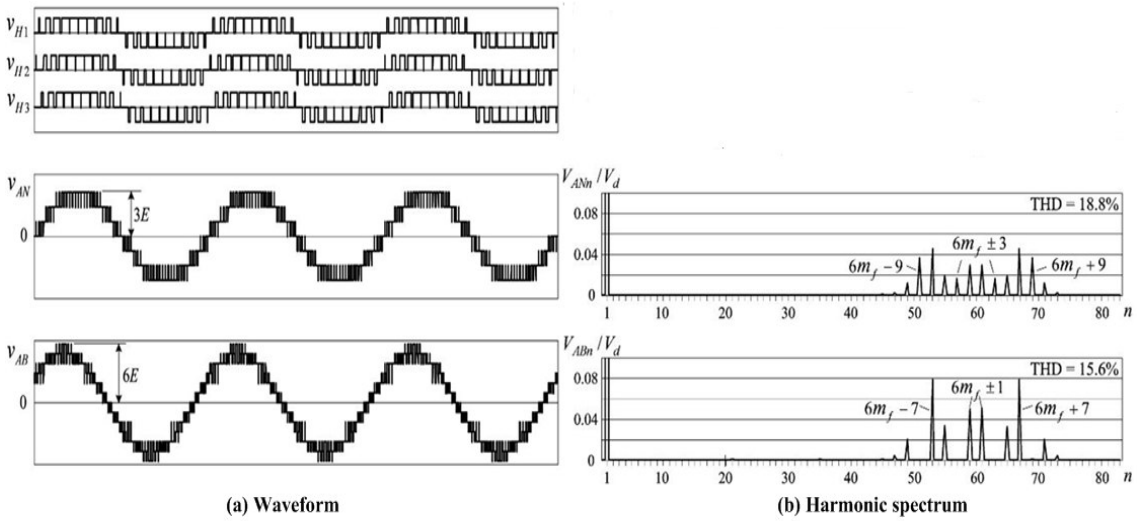

Figure 2.25 – Line and line to line output voltage of a seven level CHB with phase shifted PWM modulation (a) with their relative harmonic spectrum (b) [4]

2.5.2 Level shifted PWM

In this multicarrier PWM modulation scheme, the carriers are arranged in more layers and their amplitude is a fraction of the modulator amplitude according to the level. If the number of level that has to be achieved is n, there will need of $n-1$ carriers. The amplitude of these carriers will be $1/(n-1)$ the amplitude of the modulator signal. They will lay in order along the y-axis covering all the modulator signal [4].

This modulation scheme can be implemented in different way according to the mutual position of the carriers. Indeed, it is possible to deal with:

- Phase disposition
- Phase opposite disposition
- Alternative opposite disposition

The graphical examples are reported in Figure 2.26.

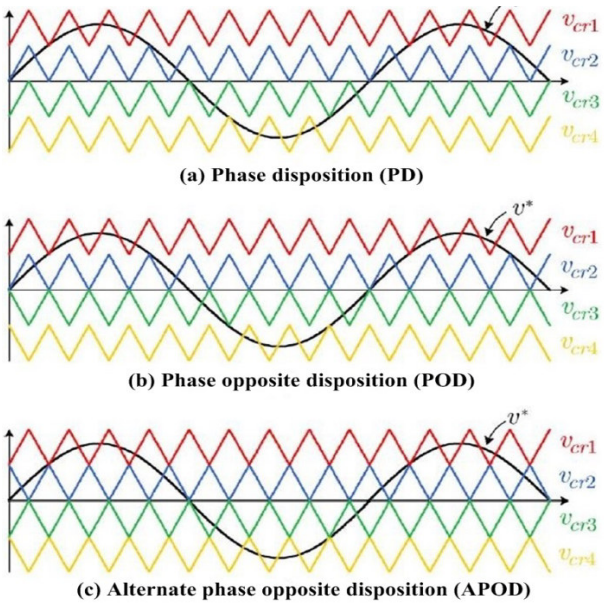

Figure 2.26 – Multicarrier level shift PWM for 5 level CHB [28]

The harmonic content which results, it is shown in 2.27.

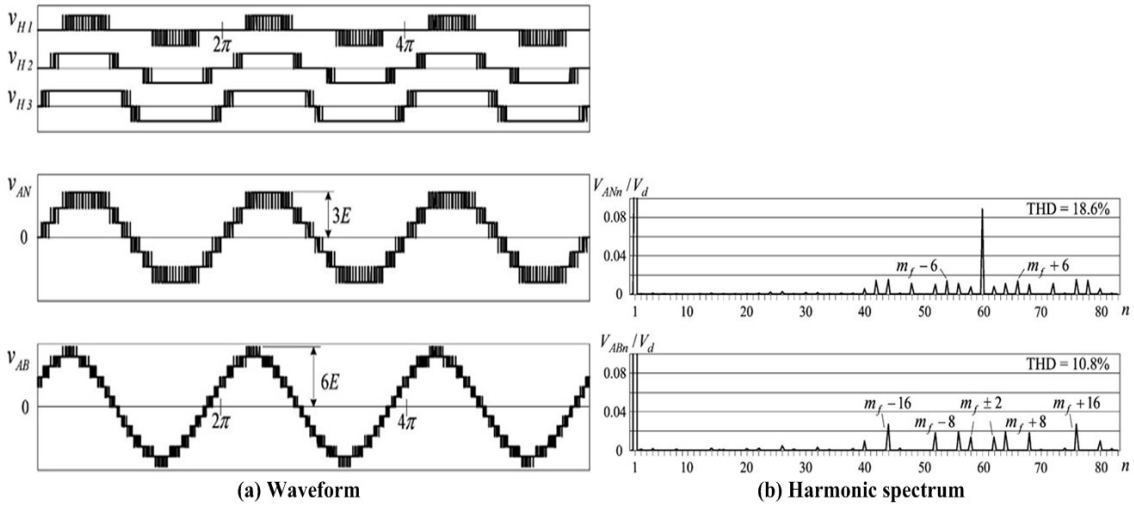

Figure 2.27 – Line and line to line output voltage of a seven level CHB with level shifted PWM modulation (a) with their relative harmonic spectrum (b) [4]

2.6 Power quality

At this point it is important to give some definitions in order to define what power quality means. This concept is related to the waveform shape and indicates the degree of precision with the expected ideal one.
Before the definition of total harmonic distortion (THD), it is presented the Fourier decomposition theory.

2.6.1 Fourier decomposition

Using the Fourier decomposition, it is possible to synthetize a not-sinusoidal periodic waveform as the sum of more sinusoidal waveforms of multiple frequency. Thus, a generic not-sinusoidal periodic waveform can be written as in (2.13)[23] [4].

$$f(t) = F_0 + \sum_{k=1}^{\infty} f_k(t) = \frac{1}{2}a_0 + \sum_{k=1}^{\infty} a_k \cos(k\omega t) + b_k \sin(k\omega t) \tag{2.13}$$

Where:

$$a_k = \frac{1}{\pi}\int_0^{2\pi} f(\theta)\cos k\theta \, d\theta \rightarrow = \frac{\omega}{\pi}\int_0^{2\pi/\omega} f(\omega t)\cos k\omega t \, dt = \frac{2}{T}\int_0^{T} f(\omega t)\cos k\omega t \, dt \tag{2.14}$$

$$b_k = \frac{1}{\pi}\int_0^{2\pi} f(\theta)\sin k\theta \, d\theta \rightarrow = \frac{\omega}{\pi}\int_0^{2\pi/\omega} f(\omega t)\sin k\omega t \, dt = \frac{2}{T}\int_0^{T} f(\omega t)\sin k\omega t \, dt \tag{2.15}$$

$$F_0 = \frac{1}{2}a_0 = \frac{1}{T}\int_0^{T} f(\omega t), dt \tag{2.16}$$

Symmetries Dealing in the thesis with regular waveform, having as characteristics: null average value, parity (2.17) and symmetry along the half wave (2.18); it is possible to obtain the relation in (2.19) [23].

$$f(t) = f(-t) \tag{2.17}$$

$$f(t) = -f(t + \frac{T}{2}) \tag{2.18}$$

$$b_k = 0 \forall k; a_k = \begin{cases} \frac{4}{\pi} \int_0^{\pi/2} f(\omega t) \cos(k\omega t) d\omega t & \text{for } k \text{ odd} \\ 0 & \text{for k even} \end{cases} \tag{2.19}$$

For each harmonic, the rms value is obtainable as in (2.20).

$$F_k = \sqrt{\frac{a_k^2 + b_k^2}{2}} = \frac{a_k}{\sqrt{2}} \tag{2.20}$$

While for the whole signal the rms value is obtained in (2.21).

$$F = \sqrt{F_0^2 + \sum_{k=1}^{\infty} F_k^2} \tag{2.21}$$

Thus, the distortion power is defined as (2.22).

$$F_{dis} = \sqrt{F^2 - F_1^2} = \sqrt{\sum_{k \neq 1}^{\infty} F_k^2} \tag{2.22}$$

2.6.2 Total harmonic distortion (THD) and harmonic spectrum

With the Fourier decomposition, it is possible to build the harmonic spectrum which consists of all the harmonics ordered by increasing frequencies. Representing their contributes in a graph, it is possible to see the singles contributes, making possible a system analysis in order to evaluate the waveform quality.
The total harmonic distortion (THD) is defined as the ratio between the harmonic content except the first harmonic and the first harmonic, expressed in percentage. The relationship is given in (2.23).

$$THD_{percent} = 100 \frac{F_{dis}}{F_1} = 100 \frac{F^2 - F_1^2}{F_1} = 100 \sqrt{\sum_{k \neq 1}^{\infty} (\frac{F_k}{F_1})^2} \tag{2.23}$$

2.7 Filter design

The output filter is a fundamental part of the model. Firstly it would not be possible to connect two voltage sources in parallel without a load; and secondly, it limits the current transient.
When it is used a synchronous generator connected to the grid, the filter also takes into account of the machine windings, but in the case of an inverter this contribute it is not present. Hence it has to be fully provided.

The effects of the filter are [29]:

- Reduction of current ripple;
- Improvement of power factor;
- Reduction of output voltage.

In order to understand how to design the filter, it is important to analyze the behaviour of voltage and current values between two systems connected through an inductance in steady state condition. The situation is illustrated in Figure 2.28.

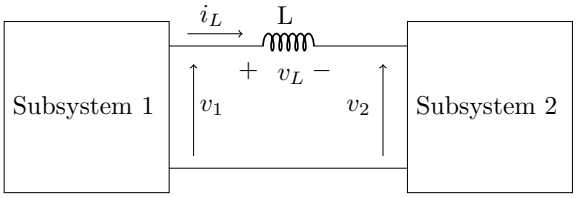

Figure 2.28 – Two generic subsystem connected by an inductor

The relationship which links voltage and current in an inductance is shown in (2.24),

$$v_L = L \cdot \frac{di_L}{dt} \tag{2.24}$$

and moving the dt to the voltage side and developing the integral, it is possible to obtain (2.25).

$$\Delta i_L = v_L \cdot \frac{\Delta t}{L} \tag{2.25}$$

In a switching period, according to (2.24), the behaviour of voltage and current is represented in Figure 2.29.

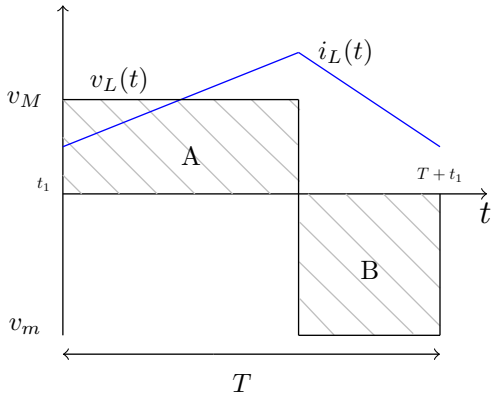

Figure 2.29 – Behaviour of voltage and current in the inductor connected between two system in steady state [23]

From Figure 2.29 it is possible to note that: the value in the beginning and at the end is equal, being the area A and B the same (steady state).
Thus the current ripple, that is the oscillation of the current over and under the average value, it is so depending on:

- Frequency;
- Value of filter inductance;

What has to be taken into account in the filter design, is that the value of the current THD cannot overpass: the limit allowable THD = 5 % at full power; and THD = 8 % at different level of power operation, reported in the EN 61000-2-4 [10] [25] [29].
Many strategies have been developed to design these line filters. In Paragraph 2.7.1 the maximum current ripple is reported, while in Paragraph 2.7.2 an iterative algorithm method is explained [29].

2.7.1 Current ripple method

The current ripple is defined as difference between the peak and the average current value. Considering the voltage and current behaviour shown in Figure 2.29, and the relation (2.24), at the clamp of an inductor, it is possible to write (2.26).

$$L \cdot \frac{\Delta I_L}{T_{on}} = v_M \tag{2.26}$$

With D duty cycle and T_{sw} switching period. The current ripple results (2.27).

$$\Delta I_L = \frac{v_M \cdot D \cdot T_{sw}}{L} \tag{2.27}$$

From this value of ripple is possible to obtain the optimal value for the filter using (2.28).

$$L_L = \frac{v_M \cdot D}{f_s \cdot \Delta I_L} \tag{2.28}$$

2.7.2 Iterative algorithm method

As the name hints, this method is based on an iterative algorithm. Starting from the input data, regards the values of the system and the performances researched, it is possible to obtain an optimal minimum value of L_L to satisfy the required standard in Table 2.5 [10] [25].

Table 2.5 – Maximum harmonic current distortion as a percentage of the fundamental

Odd harmonics	Distortion limit (%)
3rd - 9th	4
11th - 15th	2
17th - 21st	1.5
23rd - 33rd	0.6
35th -	0.3

The schematic flowchart is reported below in Figure 2.30.

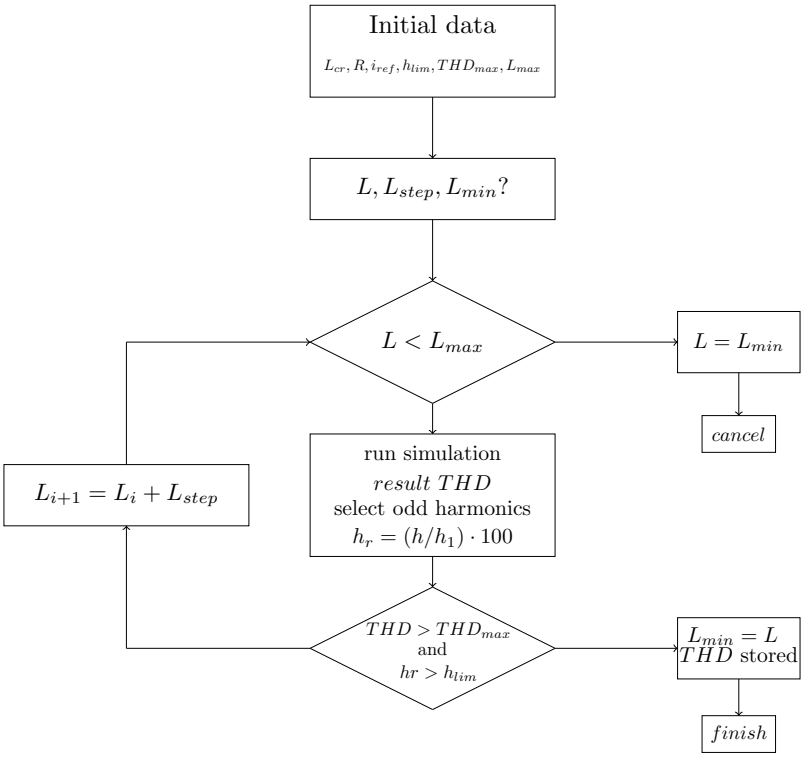

Figure 2.30 – Iterative algorithm flowchart for filter design [29]

2.8 Energy storages review

The test bench uses a energy storage system made of lead acid batteries, being them safety and cheap. However in the final project, Li-ion batteries will be used because of their better performances.
In this Section, it is reported a short comparison between these technologies in order to underlying the advantages of one against the others. Moreover it will be evaluated whether, the common lead acid batteries are suitable enough for stationary applications.

In general a battery can be represent with the equivalent circuit shown in Figure 2.31.

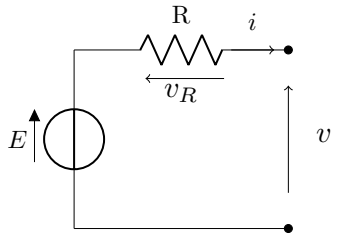

Figure 2.31 – Equivalent electric scheme of a general battery

The associated equation is the (2.29).

$$v = E - Ri \tag{2.29}$$

with R_i which depends on: temperature, state of charge and operating mode.

To characterize a battery, some quantities are defined. They evaluate the performance of the batteries or the operating conditions.
The main quantities are:

- voltage (nominal, cut off) [V];
- capacity [Ah];
- state of charge and state of discharge [%];
- energy and power (specific and density)[kWh/kg, kW/kg] [kWh/m^3, KW/m^3];
- life time [year];
- efficiency [%];
- cycles of life [n];
- inner resistance [Ω];
- operating temperature [°C];
- self discharge[% / $time$];
- State of health;

The average characteristics of the Li-ion and lead acid batteries are briefly reported in Table 2.6.

Table 2.6 – Li-ion and lead acid battery comparison [3]

Characteristics of the battery	Li-ion battery	Lead acid battery
Specific Energy [kWh/kg]	100-150	30-50
Energy density [kWh/m^3]	250-350	60-100
Power density [kW/m^3]	250-350	60-100
Specific Power [kW/kg]	500-1800	250-350
Inner resistance mΩ	150-250 7.2 V	$<$ 100 (12 V)
Life cycle (80 % of Capacity)	500-1200	400-500
Charging time [h]	2-4	8-16
Cell nominal voltage [V]	3.6	2
Discharge current [A]	1C	0.2C
Operating temperature [deg]	-20 - 60	-20 - 60
Self discharge [%/month]	5-10	3-20
Costs [€ /kWh]	500-800	100

2.9 Battery management system (BMS)

The state of the batteries in these applications is a central point in order to get an efficient behaviour from the energy storage system. To face this matter, battery management systems (BMS) have been developed. These devices are able to manage smartly the charging and the discharging process.

The BMS monitors the battery cells to prevent:

- Charge with inverse polarity;
- Over-under charge;
- Overheating and explosion.

A basic scheme is shown in Figure 2.32.

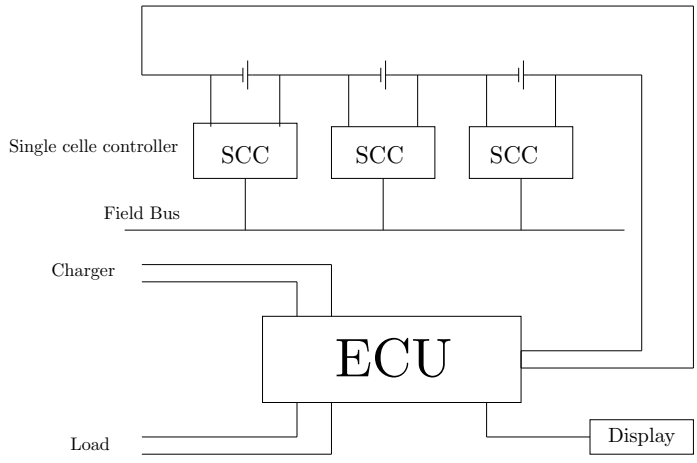

Figure 2.32 – Battery management system [3]

The main parts of the BMS are:

- One ECU;
- One controller, which controls voltage, current and temperature, communicating with the ECU through the fieldbus;
- One switch, which disconnect the battery if the current or the temperature goes out of the security range.

Being this device quite expensive, it is usually installed just on the more expensive and delicate Li-ion batteries.

2.10 Power losses in switching devices

The losses in a switching devices can be mainly attributed to [2]:

- conduction losses;
- commutation losses.

In the ideal case, they are zero, being the resistance of conduction null and the switching process instantaneous. However, the real trend is different and it shown in Figure 2.33.

In particular, the switching time in the real case is not instant, and moreover, the voltage at the clamps of the switching device is not null in the conduction time.

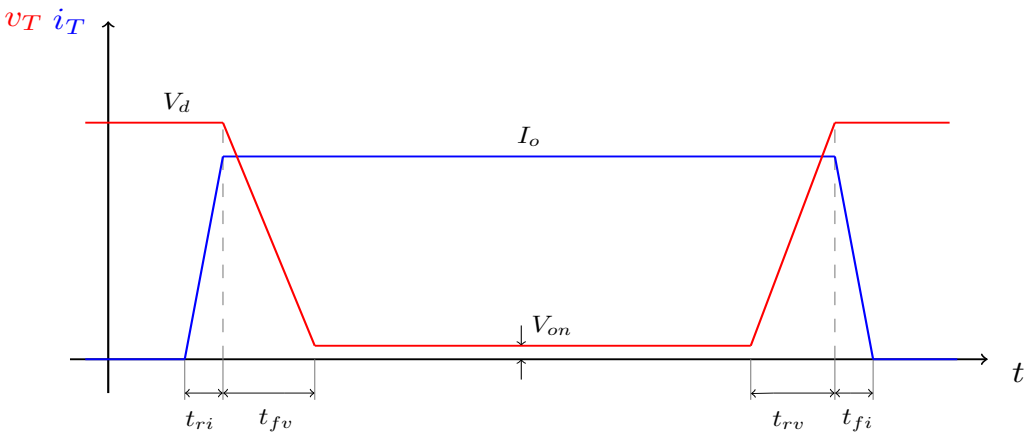

Figure 2.33 – Voltage and current in an operating MOFSET [23]

Of all these losses, it is important to take care in the simulation stage in order to get more precise results. These have been calculated as shown in next paragraphs.

Conduction losses These losses are associated to the MOSFET conduction. During the conduction, it is approximated to a simple resistor due to the resistance between drain and source in the *np*-junction of the MOSFET [2]. They are calculated in (2.30).

$$P_{con} = I_{on}^2 R_{on} D \tag{2.30}$$

I_{on} is the value of the current, R_{on} is the inner resistance of the switching device and D the duty cycle calculated in (2.31) [2].

$$D = \frac{T_{on}}{T_{cycle}} \tag{2.31}$$

The time T_{on} is calculated through the product of the sample period for the number counted by the encoder.

Commutation losses These losses are related to the not-instant switching process of the switching device.

These losses are calculated considering the period of ignition and of shutdown of the switching devices [2]. The power losses are calculated in (2.32).

$$P_{sw,on} = E_{on} \cdot f \cdot n_{sw,on} \quad P_{sw,off} = E_{off} \cdot f \cdot n_{sw,off} \tag{2.32}$$

With the energies $E_{sw,on}$ and $E_{sw,off}$ calculated in (2.33) [2].

$$E_{on} = V_{ds} \cdot I_{d,on} \cdot ((t_{ri} + tfu)/2 + Q_{rr} \cdot V_{ds} \quad E_{off} = V_{ds} \cdot I_{d,off} \cdot ((t_{ru} + t_{fi})/2) \tag{2.33}$$

where Q_{rr} is the recovery charge in capacitance, obtainable from the data sheet [2].

3 The Test Bench

In this chapter the test bench is described in details, from the beginning to the state of art at the end of the thesis. Moreover the methodologies used for the design choices are particularly explained.

3.1 System description

Firstly, it is important to understand how the system is done, of which parts is made and how they are connected in order to perform a proper connection between the grid and the energy storage system.
A basic scheme of the system is reported in Figure 3.1.

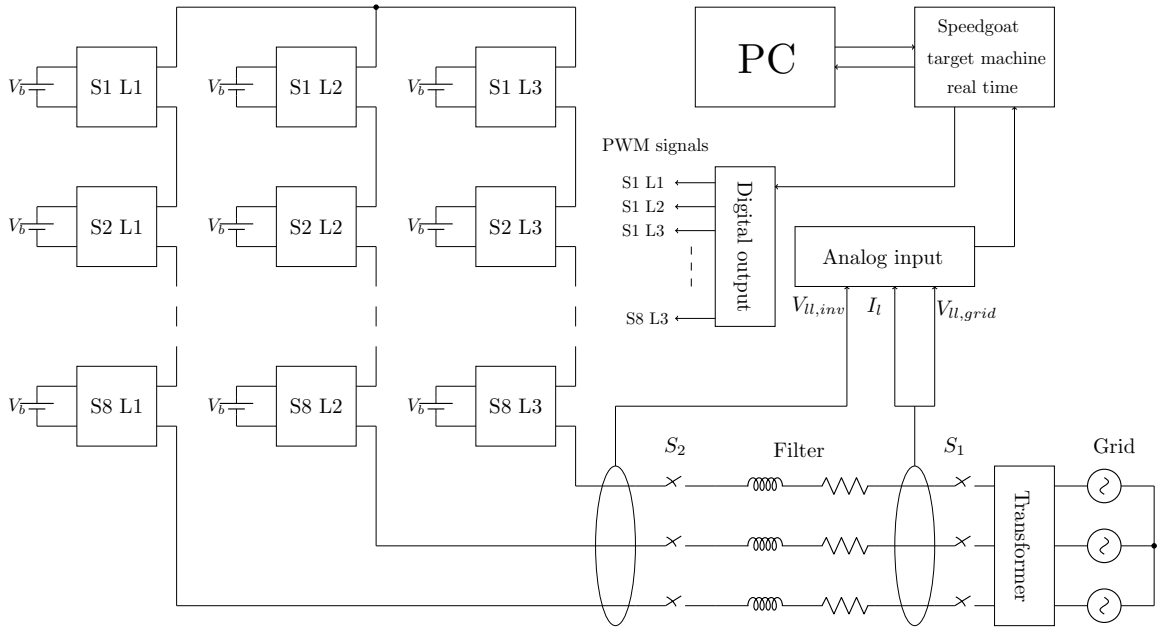

Figure 3.1 – Basic scheme of the test bench

The main parts involved, as shown in Section 1.2, are:

- The grid, which is connected to the test bench through a transformer in order to set the appropriate input voltage for each test;
- The energy storage system, made of lead acid batteries;

- The cascaded H-bridge converter;
- The control system, including interface and measurement system.

Having seen the main parts involved in the system, it is now fundamental to understand how the system performs a synchronized output with the voltage grid.

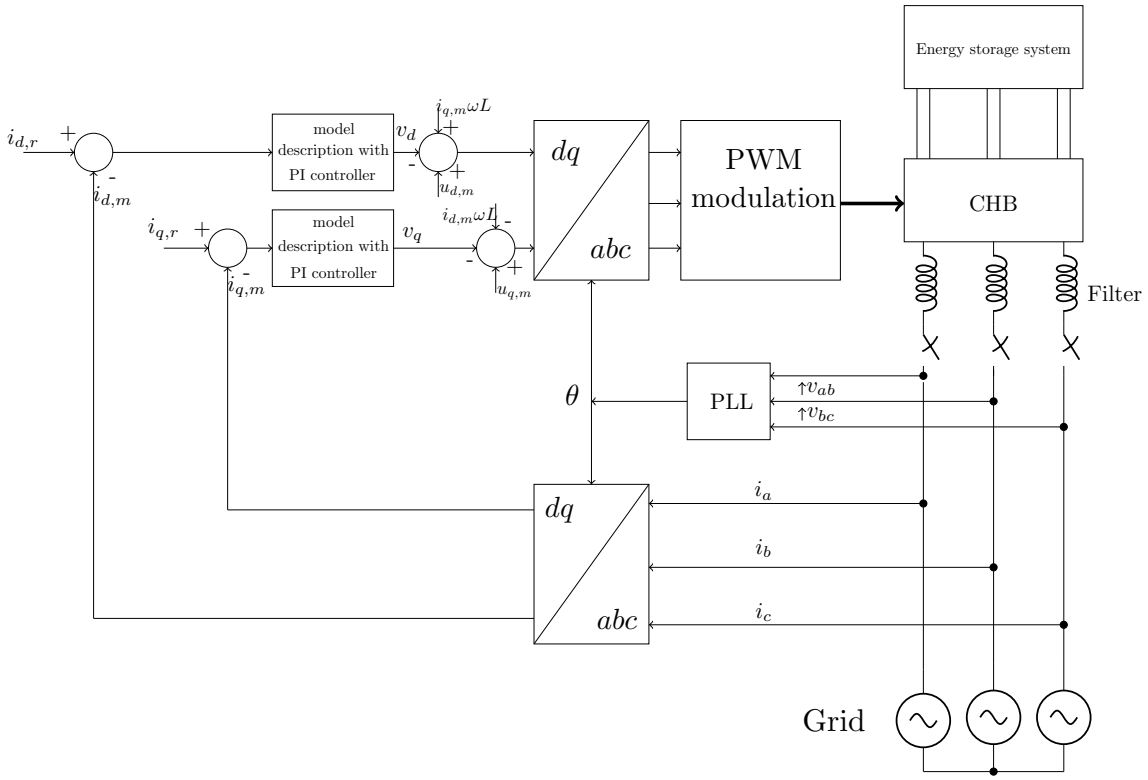

Figure 3.2 – General scheme of the control system of the thest bench

In the right part of Figure 3.2, there is still the hardware part with: the energy storage system, the CHB, the switch and the grid as shown in previous Figure 3.1; while in the left side there is the part related to the control. It is a system controlled with current, as seen in Paragraph 2.4.2 with the decoupling of the components d and q. In this way it is possible to move active and reactive power independently.

The model is summarized with a transfer function that considers the characteristics of the circuit and the controller.

The controller consists of a PI, which is in charge to give as output the variance of the voltage to obtain the desired reference current.
Form the control system is obtained the reference signal. This signal consists of a three phase of unit amplitude signal, which is synchronized with the grid and modified in order to get the requested power flow.

Starting from the reference signals, it is possible to synthesize the PWM for each module. For this purpose it is used a modulation scheme as seen in Section 2.5. Thus the system is controlled with a Simulink model.
But, how to get the measures from the hardware and how to send the output PWM signal to each submodule? It is possible through a Speedgoat real time target machine (SRTM), which allows to get the analog inputs (current and voltage measures) and provides the digital PWM output for each module (Section 3.5). It is the interface of the system, and moreover gives the possibility to monitoring the behaviour of the system in real time thanks to the scope functions.

3.2 Test bench at the beginning of the thesis

In Figure 3.3 is reported the test bench at the beginning of the work.

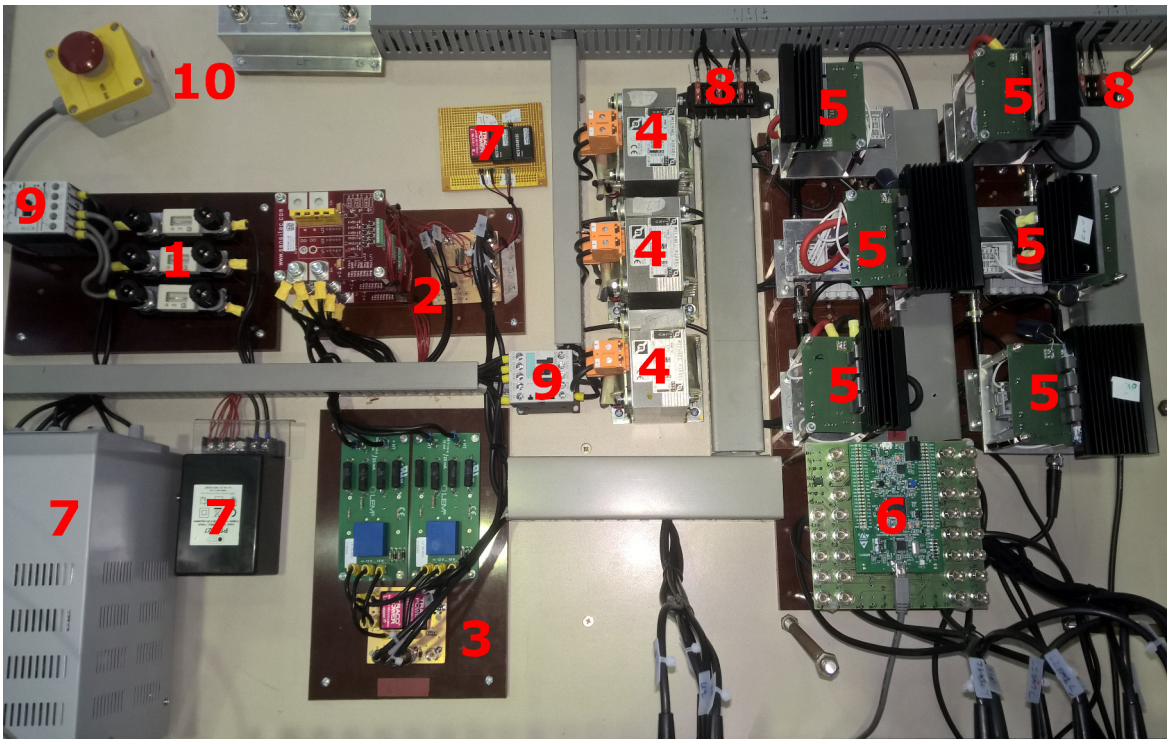

Figure 3.3 – State of the test bench at the beginning of the thesis [9]

The main parts are:

1. Line fuse (30A);
2. Current measurement system;
3. Voltage measurement system;
4. Line filter;
5. Submodules(H-bridges);
6. Microcontroller;

7. Power supply System;
8. DC side fuses;
9. Relay;
10. Emergency button;

As it is possible to see, there are 6 modules per phase that is, it is a 5 level CHB ($2n+1$ with n number of modules per phase).
The microcontroller indicated with the number 6 will be useful for further development of the control system.

3.3 Design of the energy storage system

Being the purpose of the test bench the connection of a energy storage system with the grid, it is necessary that the design of the energy storage system is related to the grid voltage value. For the test bench are used common 12 V lead acid batteries. The main characteristics are reported in Table 3.1.

Table 3.1 – Characteristics of the used batteries [1]

Characteristics	Values
Nominal voltage	12 V
Max Voltage	12.7 V
Min voltage at 0.4C	10.3 V
Capacity	7 Ah
Inner resistance	23 mΩ

For the energy storage system design:

- the batteries have to be shared among the available H-bridges;
- the minimum battery voltage has to be comparable with the maximum grid voltage, so the minimum battery voltage has to be considered.

Considering a storage unit made of 4 batteries (for each module $V_n = 48$ V), the total number of modules per phase is given by Formula 3.1:

$$n_{Hb} = \frac{V_{ll,eff} \cdot \sqrt{2}}{\sqrt{3} \cdot 4 \cdot V_{min}} = 7.92 \simeq 8 \tag{3.1}$$

To perform a proper connection with the grid are necessary 8 modules per phase (24 in total), each one with 48 V lead acid battery (96 batteries in the total system).

3.4 The module at the base of the test bench

Every module consists of an H-bridge, powered on the DC-side with a 48 V battery and as input an unipolar PWM signal coming from the control system. A module is shown in Figure 3.4.

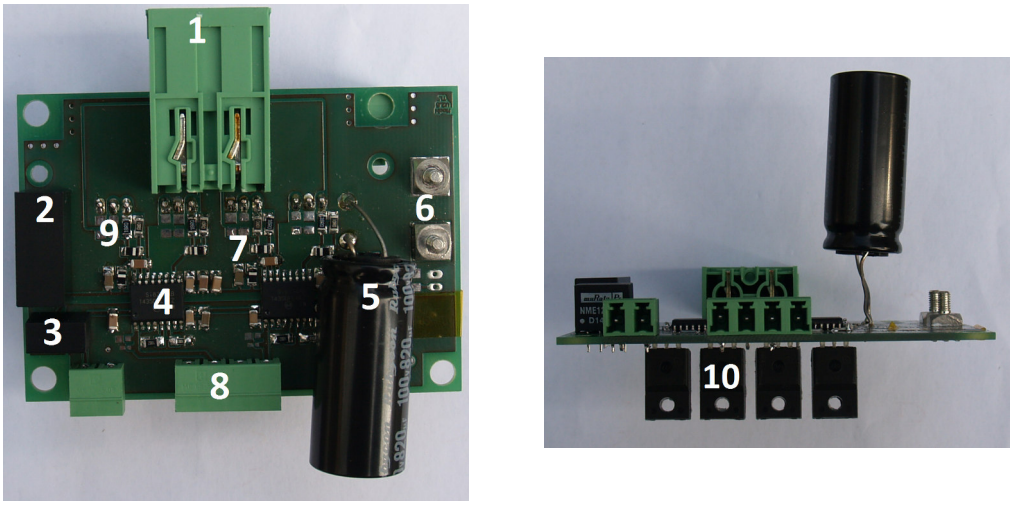

Figure 3.4 – Layout of an H-bridge module

The component parts are:

1. AC output;
2. DC-DC converter (12 V output);
3. DC-DC converter (5 V output);
4. Gate drivers;
5. DC-link capacitors;
6. DC-link input;
7. Block diodes;
8. PWM input;
9. RC Snubbers;
10. MOFSETs;

As it is possible to note, the board is divided in two zones; they are feeded with two different DC-DC converters with an output of 5 V and 12 V. They are galvanic isolated, having different ground, and they are connected by the gate drivers (4). The gate drivers are in charge to transform the digital signal provided by the modulation scheme to a 12 V signal suitable to lead the MOSFETs [17].

3.5 The Speedgoat real time target machine (SRTM)

As reported in Section 3.1, the Speedgoat real time target machine (SRTM) represents the interface between the hardware and software part.
Hence, it allows to collect information from the grid through the analog input IO106-64/32-MDR (64 single-ended or 32 differential simultaneous-sampling analog input channel) and to send the PWM signal to each module through the digital output IO316-100k (64 selectable

3.3 V/ 5 V front TTL I/O lines) as shown in Figure 3.1.

Moreover, this machine has some scope functions which allow the real time monitoring of the system. In particular the scope functions are:

- Target scope, which sends the measured signal to an external monitor;
- File scope, which collects data during the real time in a file;
- Host scope, which allow to see in the PC the real time behaviour of the system variables.

It is important to underline that the ground of SPRT machine is connected with the ground of the measurement system, which is reviewed in deep in Section 3.8. [17].

3.6 System synchronization

A decisive role for the good functioning of the test bench is played by the synchronization. It guarantees that the output space voltage phasor:

- is rotating at the same speed of the grid phasor;
- is in phase with the grid phasor;
- have the same amplitude of the grid phasor.

To sum up, it verifies the matching conditions seen in Section 2.1. Whether they are not respected a random current comes to flow, causing bad functioning or short circuit.

The voltage measurement system (Paragraph 3.8.1) provides the information about the voltage, they are elaborated in the model and the synchronization of the reference signal is performed.

To obtain the information of the position $\theta = \omega t$, useful for the dq transformation (Paragraph 2.4.1), it is used a MathWorks block called Phase lock loop (PLL) [21]. Starting from the three voltage phasors, it gives the value of the position θ. A schematic block diagram is shown in Figure 3.5.

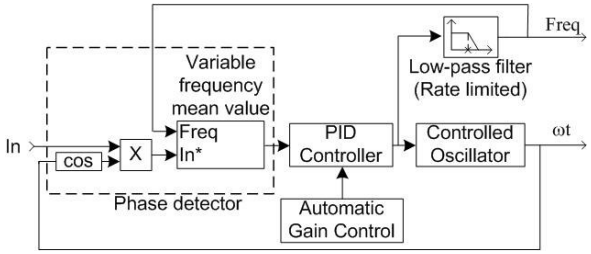

Figure 3.5 – Phase lock loop block (PLL) [21]

In particular, the voltage phasors have to be provided with the right order. Indeed, if the voltage phasors are given with a wrong sequence, a fake value of θ it is obtained and the SRTM CPU goes overload.

3.7 Design choices for the test bench

In Paragraph 3.7.1, 3.7.2 and 3.7.3 choices and the methodologies used to design some fundamental parts of the test bench are reported.
Particularly, the choice of the filter and of the switching frequency, have to be chosen considering their influence on the current ripple, power losses and harmonic content.

3.7.1 Choice of the filter

As described in Section 2.7, the choice of the filter represents one of the more important system features, having a relevant impact on the current ripple and power quality. Because of this it has to be carefully designed.
The sizing of the filter depends also from the switching frequency. In the beginning of the project, in order to underline the good low frequency functioning of multilevel inverters compared with the others, a frequency of 1 kHz has been chosen. However in Paragraph 3.7.2, a more detailed report about the switching frequency is given.
Hence to choose the inductance filter value, are applied the maximum current ripple and the iterative methods explained in Section 2.7.1.

Maximum current ripple method Being the parameters of the system:

- $P_n = 21$ kW;
- $V_n = 400$ V;
- $I_n = \dfrac{P_n}{\sqrt{3} \cdot V_n} = 30.3\text{A}$;
- $V_{b,max} = 4 \cdot 12.7$ V.

And knowing that the admitted maximum current ripple has to be within the 5 %, the maximal oscillation of current is calculated in (3.2).

$$\Delta I_{L,max} = 0.05 \cdot \sqrt{2} \cdot i_n = 2.05 \quad \text{A} \tag{3.2}$$

So the filter inductance is calculated as in (3.3).

$$L_{filter} = \frac{T_s}{2} \cdot \frac{V_{b,max}}{2} \cdot \frac{1}{\Delta I_{L,max}} = 0.00619 \quad \text{H} \tag{3.3}$$

Iterative algorithm method Applying the iterative algorithm method shown in Paragraph 2.7.2, the obtained filter inductance results of just 1 mH.
In order to save on the project, and considered that the smaller filter satisfies the requested characteristics, a filter of about 1 mH has been initially chosen.

However, using the frequency of 1 kHz the current ripple is too pronounced and the output reference signal results very distorted as shown in the graph in Figure 3.6.

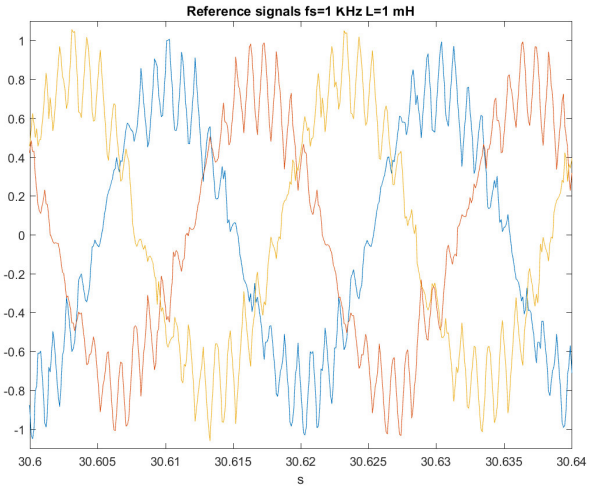

Figure 3.6 – Reference signal from the control system using $L_f = 1$ mH and $f = 1$ kHz (Figure 3.2)

Being the iterative algorithm tuned just on the harmonic content, at 1 kHz, it does not satisfy the maximum current ripple value required and the frequency will have to be increased. The chosen of the best value of frequency is reported in Paragraph 3.7.2.

3.7.2 Switching frequency

The choice of the switching frequency is a focus point in the project. Indeed, from its value depends:

- the value of current ripple;
- the losses in the MOSFETs caused by the recovery time;
- the harmonic spectrum configuration.

Increasing the frequency, it is possible to obtain a lower current ripple, but on the other hand, the losses will be increased because of the operations in the switching devices. An optimum value, considering these two parameters, has to be found.

Efficiency and power losses It has been measured the MOSFET efficiency at different frequencies and at different current values. The data are reported in Table 3.2 [18].

Table 3.2 – Efficiency of a H-bridge MOSFET for different frequencies values and current [18]

Current values	Evaluated frequencies				
[A]	1 kHz	2 kHz	4 kHz	8 kHz	16 kHz
9	99.03	98.84	98.71	98.59	98.03
15	99.06	98.86	98.82	98.67	98.32
22	98.98	98.91	98.81	98.64	98.53

The results are illustrated also in the graph in Figure 3.7.

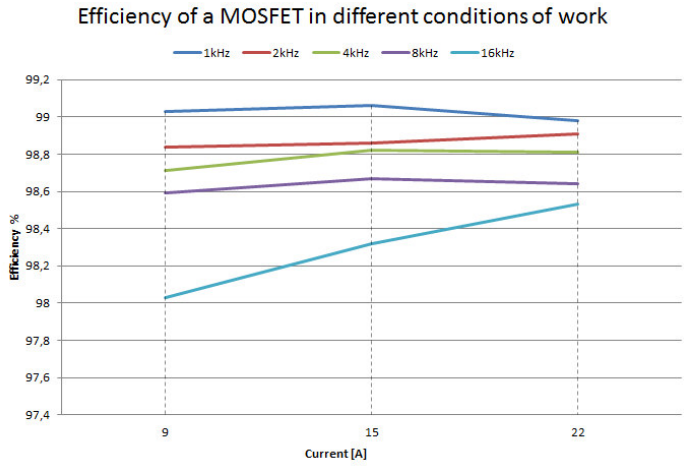

Figure 3.7 – Efficiency of a H-bridge MOSFET for different frequency values and current

Current ripple The current ripple is calculated according to what explained in Paragraph 2.7.1 with the relationship (3.4).

$$\Delta I_L = \frac{v_M \cdot D \cdot T_{sw}}{L} \tag{3.4}$$

For this evaluation are considered:

- different switching period with duty cycle D = 0.5;
- maximum battery voltage value $V_{max} = 4 \cdot 12.7 = 50.8$ V;
- different inductance filter values: filter initially installed ($L_1 = 0.915$ mH) and filter designed in Paragraph 2.7.1 ($L_2 = 6.19$ mH).

The current ripples are reported in Table 3.3.

Table 3.3 – Current ripple values calculated for different frequencies and line filters

Inductance filter values	Evaluated frequencies				
[mH]	1 kHz	2 kHz	4 kHz	8 kHz	16 kHz
0.915	13.87	6.93	3.47	1.73	0.865
6.18	2.05	1.02	0.51	0.26	0.13

Considering the results obtained from this study, it is decided to use a switching frequency of 8 kHz combined with the inductance filter $L_1 = 0{,}915$ mH. This configuration permits to have good efficiency performances and to respect the maximal current ripple indicated in (3.2).
New analysis will be done in future with the installation of the new filter, allowing in this way to work with lower switching frequency.

Symmetries Using a three phase system, it is possible to avoid some specific harmonic considering some symmetries [23]. In particular, if m_f is:

- odd, the harmonic spectrum is without the even harmonics,
- multiple of three, the harmonics spectrum is without multiple of three harmonics.

3.7.3 Controller design

To assure the stability of the system, good control and dynamic response , it is useful to analyze the transfer function of the system in order to design a suitable controller. The equivalent circuit of the test bench is represented in Figure 3.8.

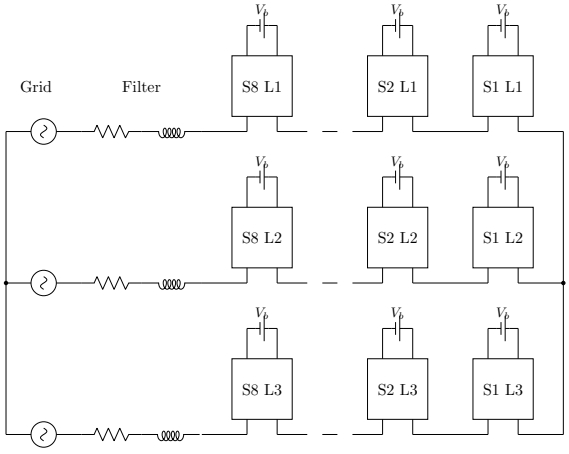

Figure 3.8 – Equivalent coupling circuit between the energy storage system and the grid

Considering the equivalent single phase circuit as done in Paragraph 2.4.1, the associated differential equation is (3.5).

$$V_i(t) + Ri + L\frac{di}{dt} - V_g(t) = 0 \tag{3.5}$$

Operating the dq transformations as shown in Paragraph 2.4.1, it is obtained the dq decomposition (3.6),

$$\begin{cases} V_{i,d} = I_d(R_f + L_f s) - 2\pi f L I_q + V_{g,d} \\ V_{i,q} = I_q(R_f + L_f s) - 2\pi f L I_d + V_{g,q} \end{cases} \tag{3.6}$$

for which it is possible to give the block diagram representation, of one axis, in Figure 3.9.

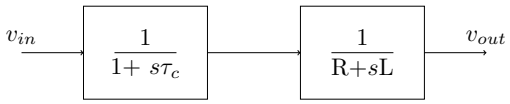

Figure 3.9 – Open loop block diagram including test bench and filter

It involves the contribute of the filter, where the parameters are taken from the filter datasheet, and a term imputed to the inverter delay, dependent on the switching frequency [5]. The considered values are:

- R_f=0.0131 mΩ(parameter taken from the nominal values of the filter);
- L_f=0.915 mH (parameter taken from the nominal values of the filter);
- τ_e=0.0698 s;
- τ_i= $T_s/2 = 1/(2 \cdot f_s) = 1/(2 \cdot 8000) = 0.0000625$ s.

The open loop transfer function results (3.7).

$$Y(s) = \frac{1}{(1 + s\tau_i)(1 + s\tau_e)} \tag{3.7}$$

Considering the two contributes, a second order transfer functions would result. However, being the inverter delay contribute negligible, the transfer function is good synthetized by the only filter block. The frequency response of the system is represented in the following Bode's diagrams in Figure 3.10 and 3.11.

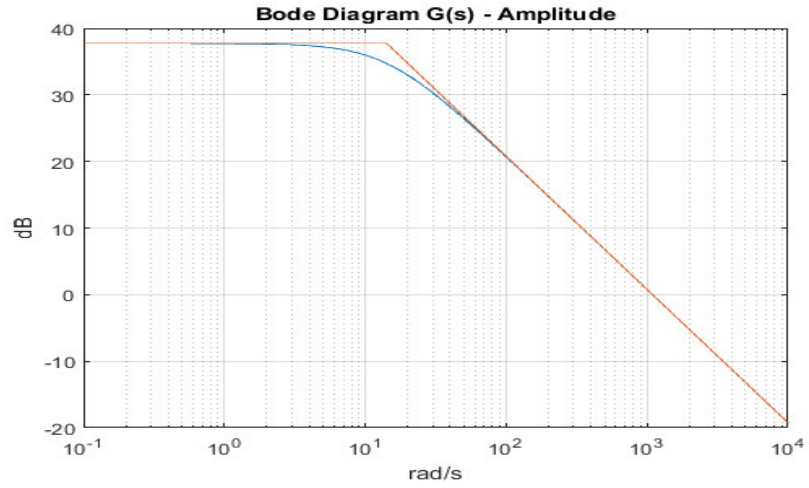

Figure 3.10 – Bode's diagram: amplitude of G(s)

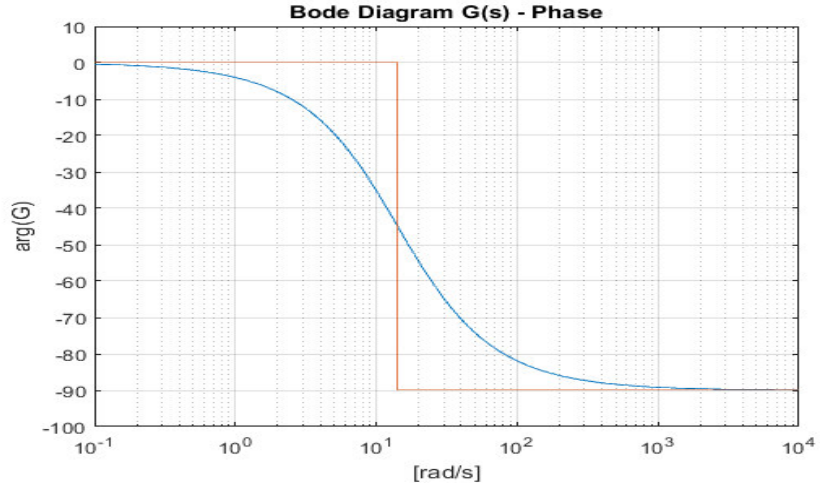

Figure 3.11 – Bode's diagram: phase of G(s)

As it is possible to see, the system is intrinsically stable, but to implement the current control, it is used a closed loop with a PI controller for d and q axes as shown in Figure 3.12.

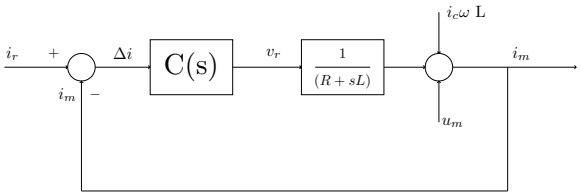

Figure 3.12 – Block diagram of the closed loop with the controller

Considering that, the controller C(s) is a PI, it has the transfer function described in general as (3.8).

$$C(s) = k_P + \frac{k_I}{s} = \frac{k_I}{s}(1 + \frac{k_P}{k_I}s) \tag{3.8}$$

Thus, the new open loop transfer function results (3.9),

$$G'(s) = \frac{k_I}{s}(1 + \frac{k_P}{k_I} \cdot s)(\frac{\frac{1}{R}}{(1 + sL)}) \tag{3.9}$$

While, the closed loop transfer function, with G'(s) made of the controller and filter contributes, is 3.10.

$$W(s) = \frac{G'(s)}{1 + G'(s)} = \frac{C(s) \cdot G(s)}{1 + C(s) \cdot G(s)} = \frac{\frac{k_i}{s}(\frac{k_p s}{k_i} + 1)(\frac{\frac{1}{R}}{1 + s\tau_e})}{1 + \frac{k_i}{s}(\frac{k_p s}{k_i} + 1)(\frac{\frac{1}{R}}{1 + s\tau_e})} \tag{3.10}$$

The controller parameters have to satisfy in the system the conditions of:

- stability ($m_\varphi \geq 45$);
- steady state error constant and less than 10 %;
- $\omega_a \cong 1700$ rad/s that corresponds to a rise time $t_r = 0.45/\ f_{bw} = 1.6$ ms;

Being the type of the system 1, that is W(0)=1 and $\frac{dW(0)}{dt} = 0$ [19], the steady state error can be written as (3.11):

$$e_s \leq \frac{1}{k_B(G')} = \frac{1}{k_I \cdot R} \quad \Rightarrow \quad k_I \geq \frac{1}{R \cdot e_s} = 769\frac{1}{s} \tag{3.11}$$

Then, by imposing $\omega_a = 1070$ rad/s, it is obtained the k_P value in (3.12).

$$|G'(s)| = 1 \quad \Rightarrow \quad \frac{k_I}{\omega}\sqrt{1 + (\frac{k_P}{k_I}s)^2}\frac{1/R}{\sqrt{1 + (\tau_e\omega)^2}} = 1 \quad \Rightarrow \quad k_P = 1.51 \tag{3.12}$$

The new Bode's diagrams are shown in Figure 3.13 and 3.14. From them it is possible to evaluate and verify the value m_φ, which results about 75, in line with the requested value.

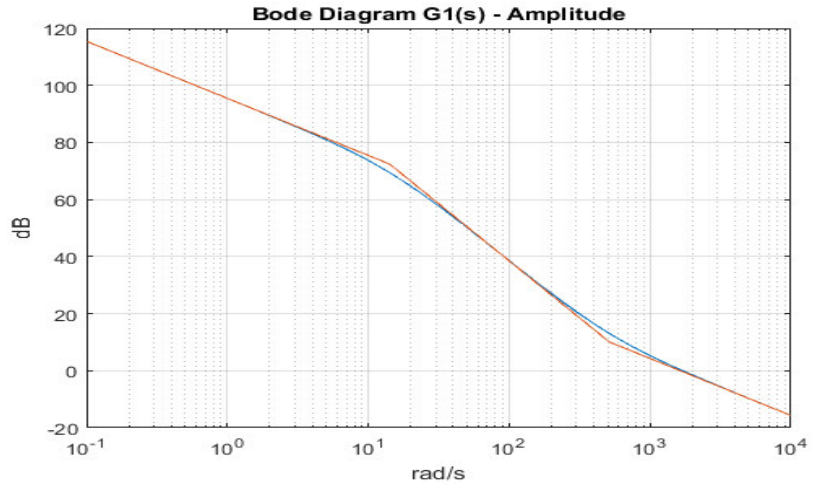

Figure 3.13 – Bode's diagram: amplitude of G'(s)

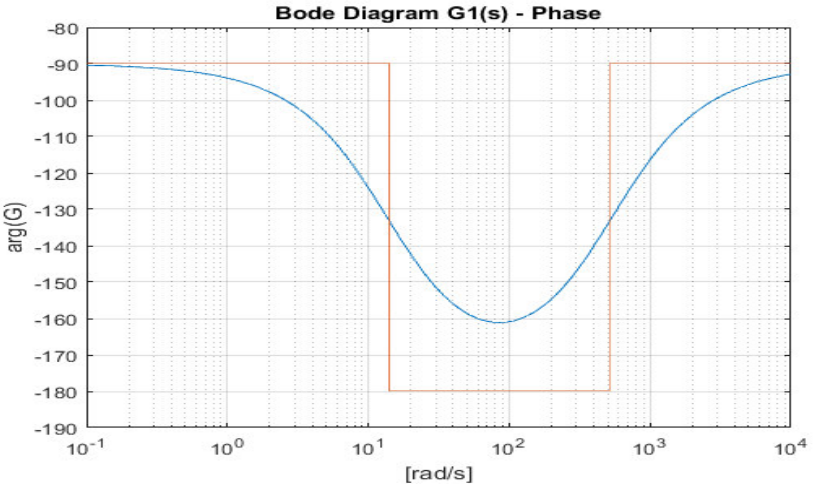

Figure 3.14 – Bode's diagram: phase of G'(s)

3.8 Measurement system

3.8.1 Voltage measurement system

The voltage measurement system, it is useful to get the information about the line voltage vectors. It uses voltage transducers in order to obtain a proper signal readable from the SRTM. Indeed, the analog input voltage range admitted by the SRTM is between ± 10 V.

The transducer is the LEM Voltage transducer LV 25-600 [30], having as a input maximal voltage of 600 V_{rms} and as output a current within 25 mA.

This kind of transducer guaranties [30]:

- excellent accuracy;
- good linearity;
- low temperature drift;
- high immunity to external interference.

The basis scheme of this device is shown in the following Figure 3.15:

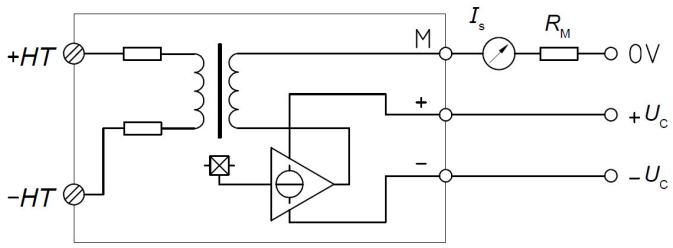

Figure 3.15 – Voltage trasducer circuit [30]

Being the output a current, there is necessary to have an external circuit in order to obtain a voltage signal suitable for the analog input. As suggest from the data sheet [30], it is inserted in series with the output resistor (100 Ω). The proportional voltage signal is so obtained, and through a BNC cable, it is sent to the SRTM input.

Of these voltage measurement systems, two couples are installed. The first couple is used for two line to line grid voltages, while the second one for two line to line inverter side voltages. The third value of line to line voltage is calculated as the difference of the other two values. Beyond the information about the position of the voltage phasors, the measurement system is also used for the monitoring of the voltage values through the target scope cited in Section 3.5. This monitoring is very important, inasmuch allows to compare the voltage signals, from inverter and grid, in order to understand if the coupling of the system is possible.

A couple of voltage measurement system is shown in the Figure 3.16.

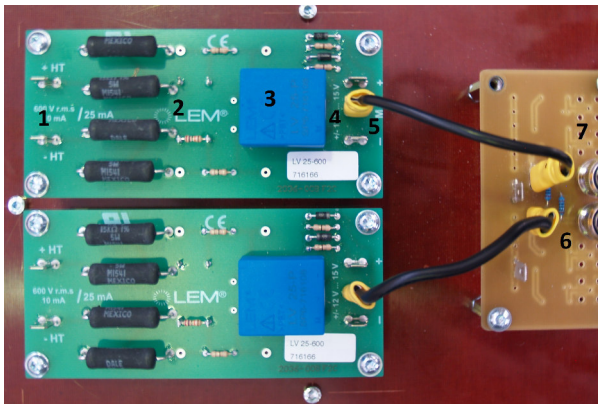

Figure 3.16 – Circuit of the voltage measurement system

The main parts are:

1. measured voltage input;
2. input circuit;
3. voltage sensor;
4. operational supply clams (± 15 V);
5. sensor output (M);
6. 100 Ω resistors;
7. output through BNC cable;

3.8.2 Current measurement system

The current measurement system consist of three magneto resistive current sensors Sensitec CMK3000 installed in the relative demo-boards [7]. The current sensors are in charge to measure the line current values during the matching between the two systems.
The functioning principle of the CMS sensor results in a current compensation, proportional to the magnetic field gradient caused by the primary current. A laser trimmer resistance converts the compensation current into an accurate output voltage.

Figure 3.17 shows the demo board of the current measurement system.

The schematic circuit of the sensor is reported in Figure 3.17.

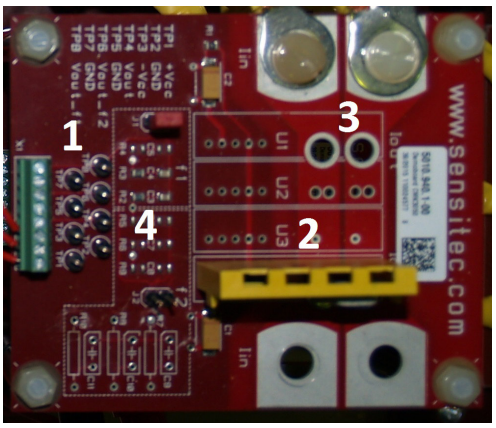

Figure 3.17 – Circuit of the Current measurement sensor [7]

The main parts are:

1. sensor output and operational supply clams (± 15 V)
2. current sensor
3. current input
4. preset and custom filter

Through the available jumper, it is possible to insert a RC filter in order to get a filtered output signal.
Working with magnetic variations, it is important to take care of the electromagnetic compatibility disturbs. The sensors have to be placed at a suitable distance each others and metallic parts has not to be in the nearby.

The current values, even in this case, are available in monitor through the scope functions seen in Section 3.5.

3.9 Security system agianst overcurrent

One of the most common module failure was caused by over-currents. To avoid this problem two security switches have been installed. They have been placed in the relay circuit, and they are led by a digital signal coming from the SRTM.
When the current monitored from the measurement system overtake the imposed limit, the signal is sent and the circuit opens.

3.10 Stage overview of the test bench during the thesis

In Figure 3.18 is presented the test bench complete of all the parts. It is possible to observe all the 24 submodules, in the back the energy storage system and the SPRM with the analog input and the digital output.

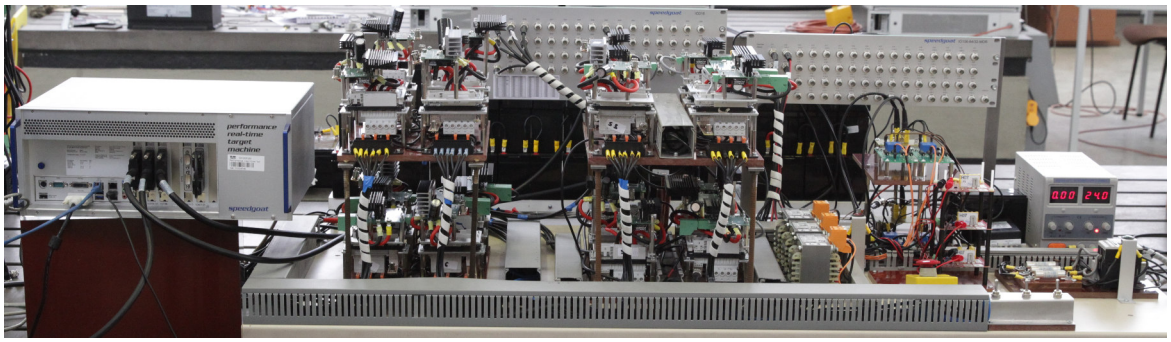

Figure 3.18 – Complete CHB 17 level

After to have developed the structure until the seventeen level, it has been needful to work on a solution to improve the functioning. Indeed, during the charge and discharge operation the result was noisy and distorted. A better trend has been reached with the increasing of the switching frequency. Regards this, it is also important to say that this choice has some drawbacks, that is:

- The increasing of the power losses in the inverter, as shown in Section 3.7.2;

- The harmonic content is shifted to higher frequency (in the result chapter, using the level shift PWM modulation, the relevant harmonics start around at 8 kHz)
- Being the sample rate of the SRTM 10 kHz the results obtained from the test bench are not acceptable at all.

Considering these points, a new filter has been ordered in order to have in future a lower frequency functioning.

With the new setting configuration, having also developed a common work cycle (Section 4), it has been decided to restart from the three level configuration in order obtain the same measures for each level. However, with the increasing of the level, problems due the reliability of the modules have been found. Being them in series, a small bad functioning of one is enough to get a not proper operation of the whole test bench during charge and discharge. At the end of the thesis, it has been possible to collect results just until the eleven level (results shown in Chapter 4).

4 Results and Comparisons

In this Chapter the significant results taken from the test bench developed during the thesis are reported. The comparison with the simulation is done in Section 4.3 and 4.4. The differences between the three the eleven level converter are analyzed, underlining the interesting characteristics and the issues.

For an easier comparison, between simulations and test results, a common work cycle has been developed. It has been designed to analyze the trends in different working conditions in order to have an overall overview. Moreover, it considers some particular issues of the system, for instance, the long term of charge before the discharge at I_d = -1 it is insered to avoid the problem presented in Section 4.2. This signal is built through a signal bilder from MATLAB/Simulink. An example of the the sequence is reported in Figure 4.1.

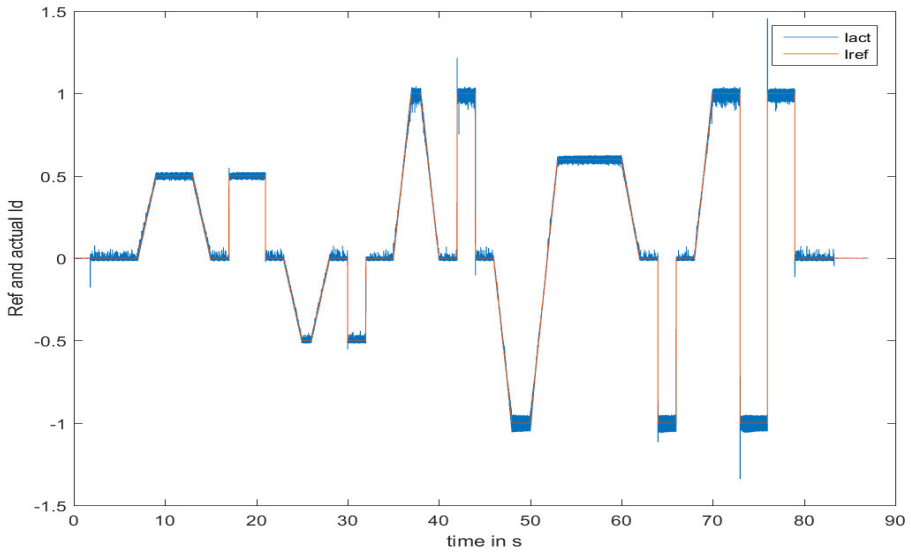

Figure 4.1 – Working cycle of the simulation and experimental tests

Before the results of the different level configurations, will be considered:

- The step response of the test bench compared with the simulation response;
- The reference signal values obtained from the control system of the test bench.

Then, for the considered level configurations, for simulations and experimental tests, voltage and current waveforms with the pertinent harmonic spectrums will be reported.

4.1 Step response comparison

In the following figures, it is possible to observe the step responses from the simulation model 4.2 and from the test bench 4.3.

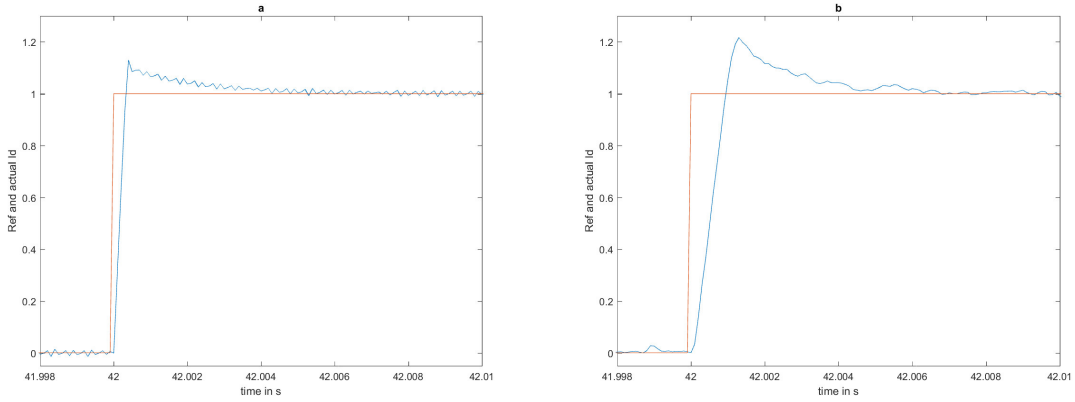

Figure 4.2 – Step response, I_d from 0 to 1 from the simulations (a) and from the test bench (b)

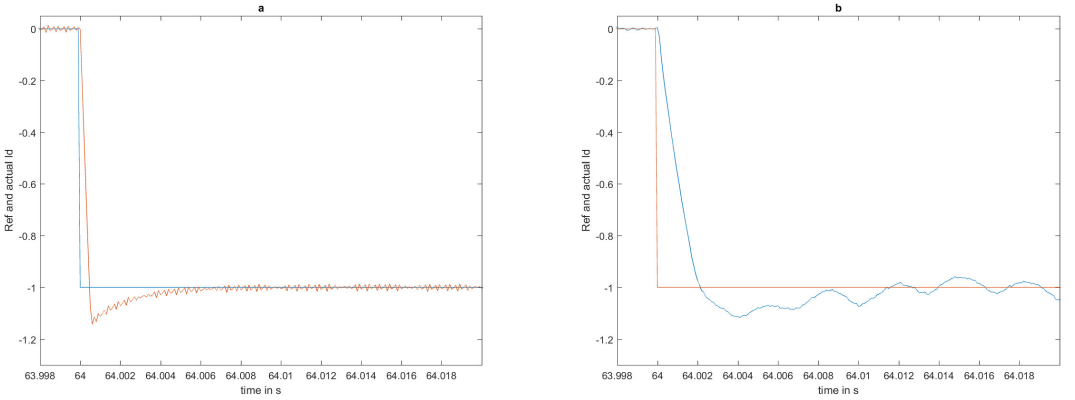

Figure 4.3 – Step response, I_d from 1 to 0 from the simulations (a) and from the test bench (b)

Comparing the figures, it is possible to see that the trends of the two models are different. Indeed, the simulation model has a more reactive response compared with the test bench. Moreover, the overshoot in the real model it is almost double. This behaviour is imputable to a not exact description of the system. The parameters used to describe the system indeed, consider just the filter data sheet, and not the real overall system. A different evaluation of the model parameters has to be developed.
To evaluate the real resistance value in the model a volt-amper measure has been done. Plugging the ammeter upstream and the voltmeter downstream a better accuracy is obtainable. The measured resistance results:

$$R_{real} = 0.07103 \pm 0.0003\ \Omega$$

that is, more than five times bigger in respect the value reported in the filter data sheet.

Regarding the inductance estimation, it should be considered the grid and transformer contributes. Being the grid contribute small compared with the filter inductance, it is negligible, while the transformer inductance will have to be evaluated.

4.2 Reference signals in different working conditions

In Figure 4.4, it is shown the typical reference signals in different work conditions. There is one signal for each phase and it is obtained at the output of the control system. Each of them depends on: the measurement system, the external input given and on the controller. From this signal, through the modulation scheme, will be synthetized the PWM signals for every single module according to the level configuration considered.

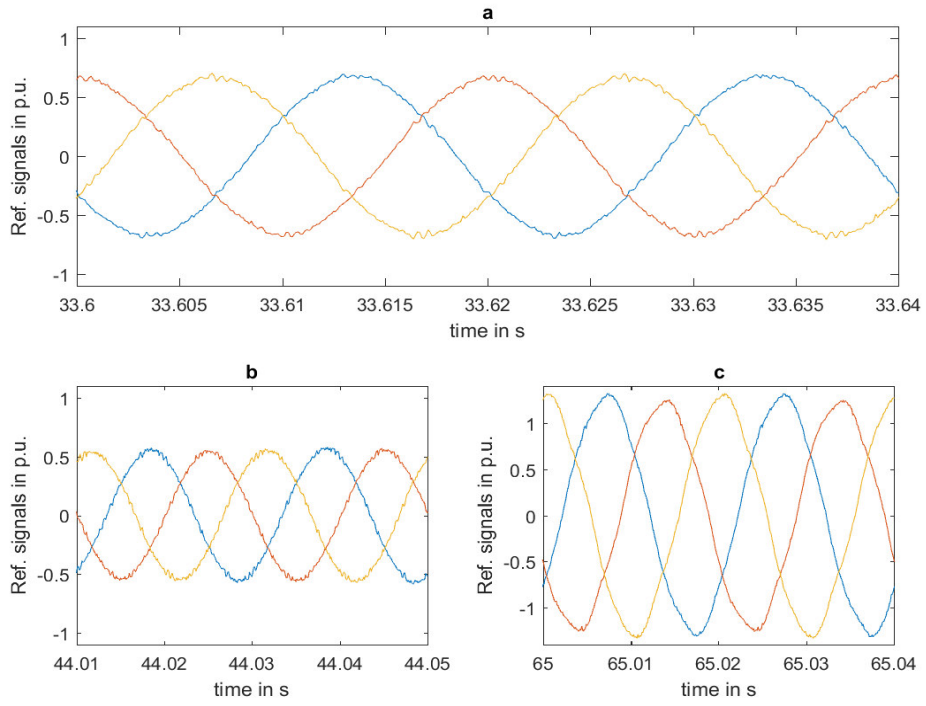

Figure 4.4 – Reference signals in different working conditions: (a) inverter connected with the energy storage system (I_d = 0); (b) charging phase (I_d = 1); (c) dischargin phase (I_d = -1)

As it is possible to observe, also during the simple matching connection, the amplitude reference values is less than one. This happens because of the input voltage value chosen. Indeed, for each battery in series, it has been considered an increment of line to line voltage of just 10 V, even if the suitable value should be as calculated in (4.1).

$$\frac{V_{batt}\sqrt{3}}{\sqrt{2}} \quad if \quad V_{batt} = 12.5\text{V} \quad \frac{12.5\sqrt{3}}{\sqrt{2}} = 15.3\text{V} \tag{4.1}$$

The used value is lower than 50 %. The reason of this choice has to be found in the discharging phase. Indeed, during the tests, many times happened that the batteries could not provide the requested power. This trend is caused by the low state of charge or state of health of the batteries involved. An instance case, where the system could not provide the energy requested, is shown in Figure 4.5.

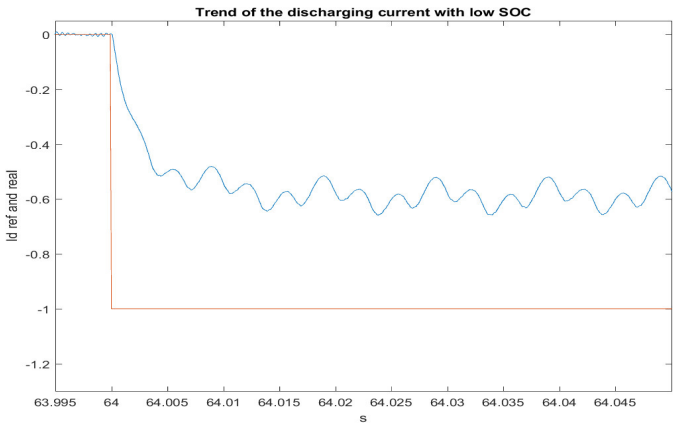

Figure 4.5 – Step response in case of low SOC

In condition of maximum power, the batteries have to provide a current equal to 4C, that is much higher than the nominal value. Even if in the beginning the battery voltages seemed enough, with a so high request it used to fall down very quickly if the state of charge was not sufficient. This trend is explained in Figure 4.6 taken from the data sheet of the batteries [1].

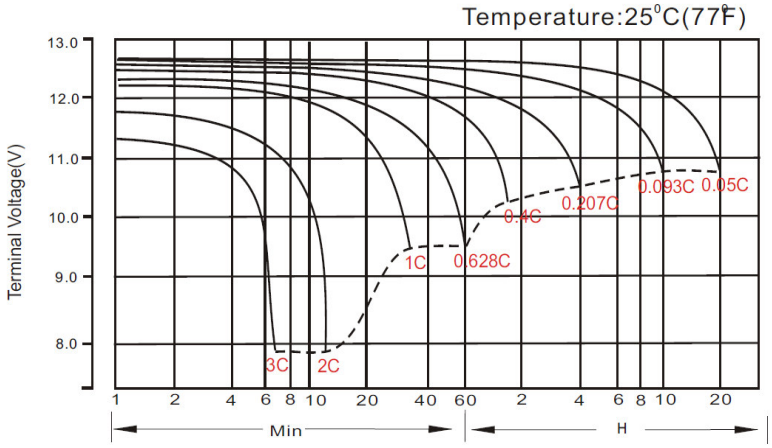

Figure 4.6 – Discharge characteristic of a lead acid battery with different discharge current [1]

A future solution could be the implementation of a control system which consider also the SOC of the batteries as in [16]. In this case, the control system will allow the requested value of current only if the SOC is high enough.

4.3 Three level cascaded H-bridge

The three level CHB, it is a common used three level inverter made of one H-bridge per phase. It is considered because it is the base configuration, and can be easily compared with the multilevel topology.

The values uses in the simulation, that is the values present in the test bench, are shown in Table 4.1.

Table 4.1 – Parameter used for the three level simulation and test

Quantities	Values
Grid	
f_{grid}	50 Hz
V_{ll}	40 V
S_{grid}	100 MVA
$I_{l,rms}$	30.3 A
Energy storage unit	
V_{bat}	50 V
Inverter	
f_{sw}	8 kHz
PWM modulation	level shifted
Filter	
R	13 mΩ
L_f	0.915 mH
Controller	
k_P	1.51
k_I	769

The sample time used for the measures is 10 kHz. This value is enough to build the 50 Hz fundamental signal. However it is not enough to appreciate the harmonic content and to have a good estimation of the THD, being the relevant distortions near 8 kHz having used the level shifted PWM (see harmonic content in Figure 2.27).

Thus the harmonic spectrum is evaluated until the frequency of 5 kHz. This is acceptable inasmuch, for higher frequency values the voltage harmonic contributes are strongly attenuate because of the effect of the line filter. All the harmonics over the frequency of 5 kHz are reduced at least of 95 %.

4.3.1 Three level configuration: line to line voltage

Three level configuration: grid voltage in charging phase

In this paragraph, it is shown the line to line voltage trends from the simulation and from the test bench during a charging phase ($I_d = 1$). In Figure 4.7 are represented the line to line voltage measured at the inverter and grid clamps, while in Figure 4.8, there are the associated harmonic spectrums.

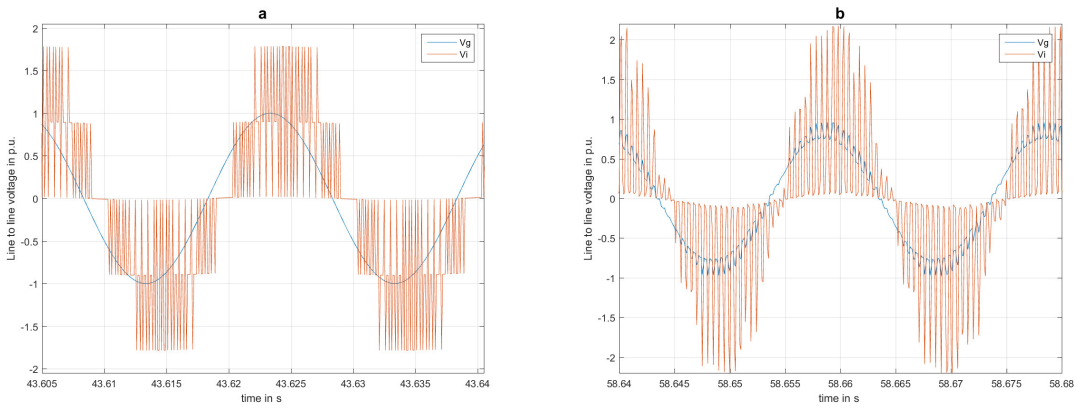

Figure 4.7 – Three level configuration: line to line voltage in charging phase ($I_d = 1$), from the simulation (a) and from the test bench (b)

In the charging phase, it is possible to note that the grid voltage waveform is anticipating the inverter waveform, so the power is flowing from the grid to the energy storage system.

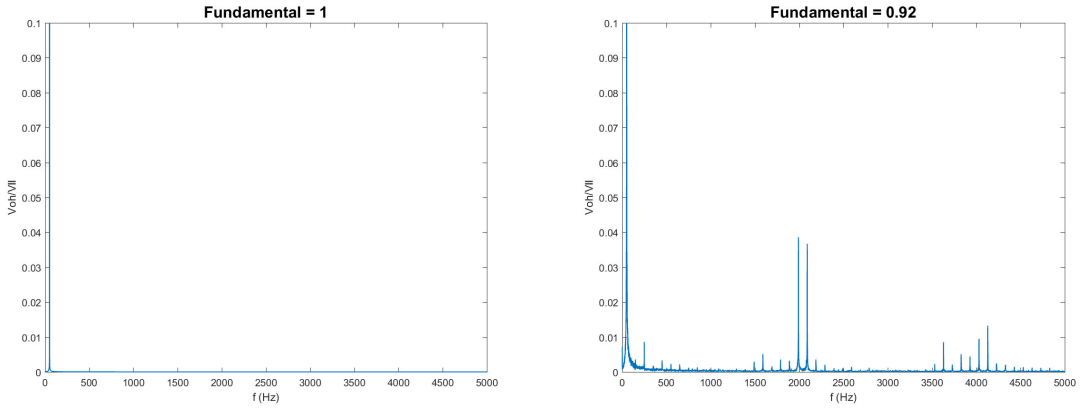

Figure 4.8 – Three level configuration: harmonic contents of the line to line voltage in charging phase ($I_d = 1$), from the simulation and from the test bench

Three level configuration: grid voltage in discharging phase

In this paragraph, it is shown the line to line voltage trends from the simulation and from the test bench during a discharging phase (I_d = -1). In Figure 4.9 are represented the line to line voltage measured at the inverter and grid clamps, while in Figure 4.10, there are the associated harmonic spectrums.

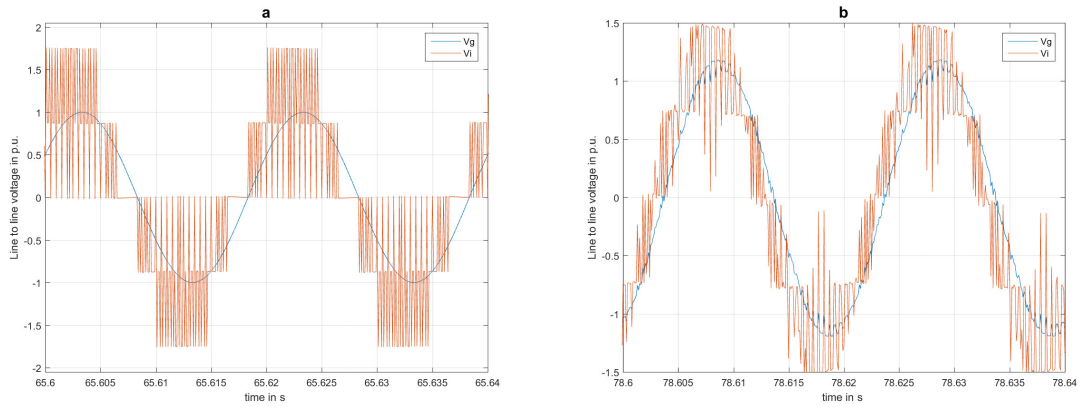

Figure 4.9 – Three level configuration: line to line voltage in discharging phase (I_d = -1) from the simulation (a) and from the test bench (b)

In the discharging phase, it is possible to note that the grid voltage waveform is anticipated from the inverter waveform. This means that the power is flowing from the energy storage system to the grid as seen in Section 2.1.

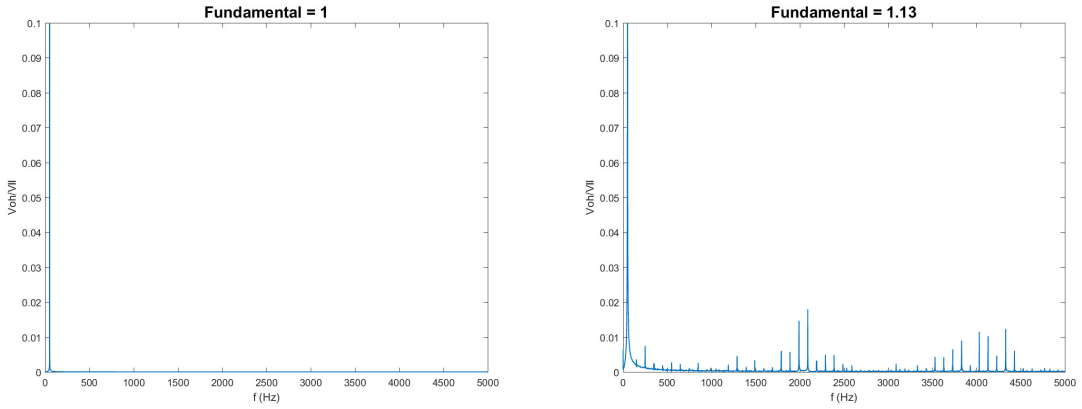

Figure 4.10 – Three level configuration: harmonic content of the line to line voltage in discharging phase (I_d = -1), from the simulation and from the test bench

4.3.2 Three level configuration: line current

Three level configuration: line current in charging phase

In this paragraph, it is shown the line current trends from the simulation and from the test bench during a charging phase ($I_d = 1$). In Figure 4.11 are represented the line currents, while in Figure 4.12, there are the associated harmonic spectrums.

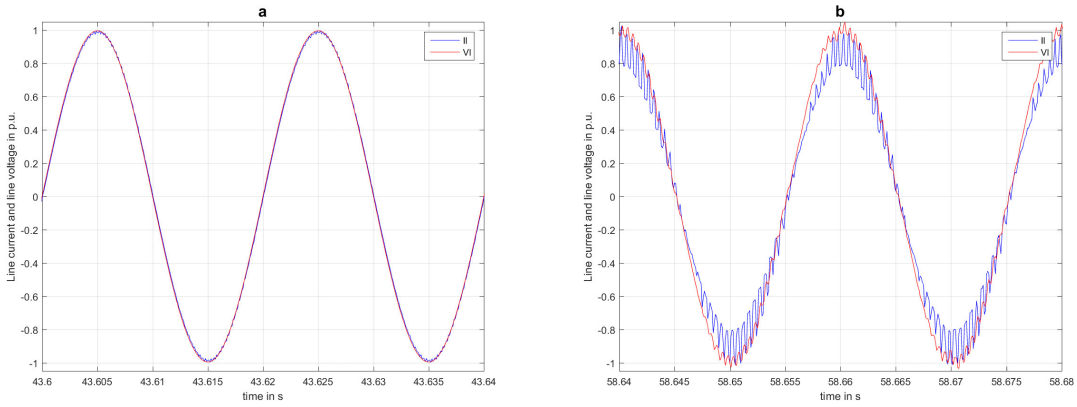

Figure 4.11 – Three level configuration: line current and line voltage in charging phase ($I_d = 1$), from the simulation (a) and from the test bench (b)

The active power is positive; the grid is charging the batteries.

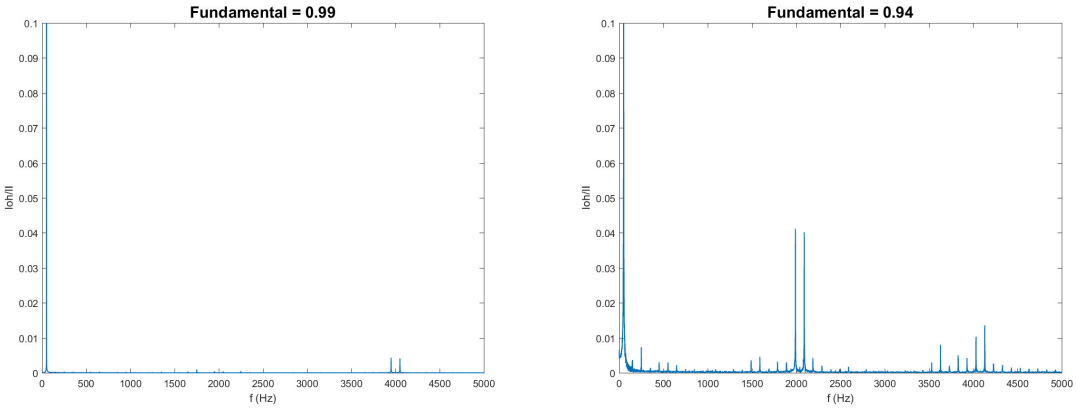

Figure 4.12 – Three level configuration: harmonic content of the line current in charging phase (I_d = -1), from the simulation and from the test bench

As it is possible to notice the harmonics of current have the same amplitude indicated in Table 2.5. The is due to the chosen of the filter. Being the filter designed with the iterative algorithm method, it is obtained the minimum value of inductance to satisfy the IEEE standard as shown in 2.7.2. With a different frequency the harmonics content is shifted causing the overcoming of the limits for some harmonic orders. With the installation of the new filter this problem will be solved.

Three level configuration: line current in discharging phase

In this paragraph, it is shown the line current trends from the simulation and from the test bench during a discharging phase (I_d = -1). In Figure 4.13 are represented the line currents measured, while in Figure 4.14, there are the associated harmonic spectrums.

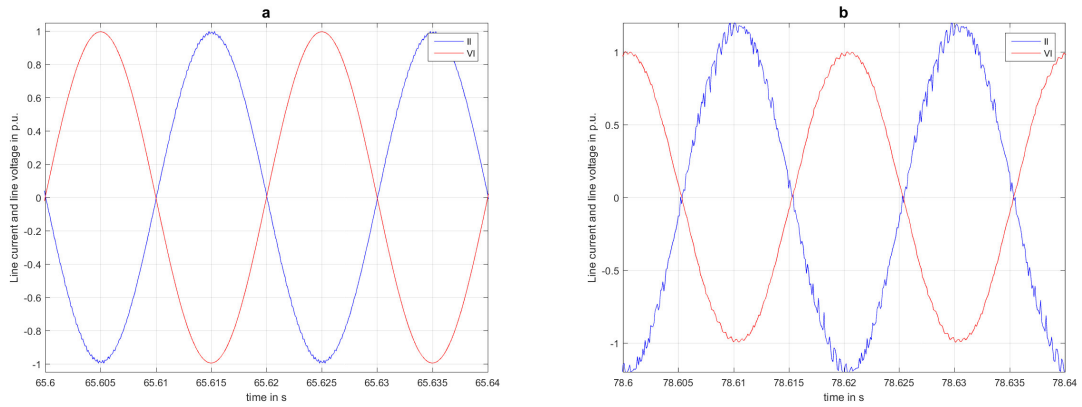

Figure 4.13 – Three level configuration: line current and line voltage discharging phase (I_d = 1), from the simulation (a) and from the test bench (b)

In the discharging phase, it is possible to note that the current has the opposite phase of the line to ground voltage. The active power is negative; the batteries are providing power.

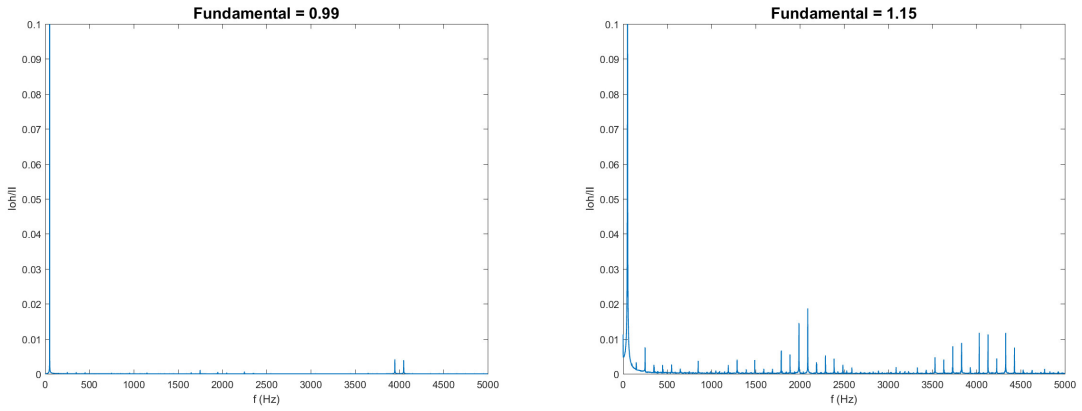

Figure 4.14 – Three level configuration: harmonic contents of the line current in discharging phase (I_d = -1), from the simulation and from the test bench

The fundamental of the line to line grid voltage results smaller during the charging time, while it is bigger in the discharge period. This has to be imputed to a not precise parameter imposition in the simulation. Using a transformer, the test bench grid are not in line with the parameter used in the simulations. The transformer has to be integrated in the simulation considering its short circuit inductance. It can be added in the filter or included using a lower grid power.

4.4 Eleven level cascaded H-bridge

In this Section, the results from the eleven level configuration are reported. It is the higher level run with the signal bilder presented at the beginning in Section 4. For higher level configurations, run with the signal bilder, are necessary more tests and on the test bench. A optimization work is required. Indeed, the sum of the contributes of many modules can easily bring to system instabilities, even if just a module it is not working properly. The values uses in the simulation are:

Table 4.2 – Parameter used for the three level simulation and test

Quantities	Values
Grid	
f_{grid}	50 Hz
V_{ll}	50 V
S_{grid}	100 MVA
$I_{l,rms}$	30.3 A
Energy storage unit	
V_{bat}	12.5 V
Inverter	
f_{sw}	8 kHz
PWM modulation	level shifted
Filter	
R	13 mΩ
L_f	0.915 mH
Controller	
k_P	1.51
k_I	769

For the eleven level configuration are reported the same measures of the three level in order to show the differences. In this case the voltage measures during the charging and the discharging phase have been taken with the oscilloscope. The sampling period of the data stored with the oscilloscope is of 100 kHz, which would be enough for a proper spectrum analysis. In spite of everything the easiest way to collect data is through the file scope of the SRTM running the work cycle (Section 3.5). In this case indeed it has been developed some scripts for collecting plots and spectrum analysis. This will be possible once that the new filter will be installed.

4.4.1 Eleven level configuration: line to line voltage

Eleven level configuration: grid voltage charging phase

In this paragraph, it is shown the line to line voltage trends from the simulation and from the test bench during a charging phase ($I_d = 1$). In Figure 4.15 are represented the line to line voltage measured at the inverter and grid clamps, while in Figure 4.16, there are the associated harmonic spectrums.

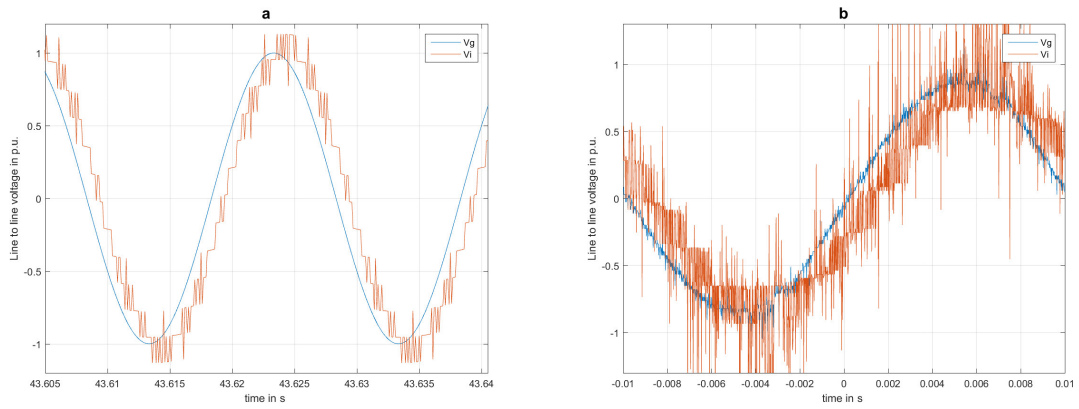

Figure 4.15 – Eleven level configuration: line to line voltage in charging phase ($I_d = 1$), from the simulation (a) and from the test bench (b)

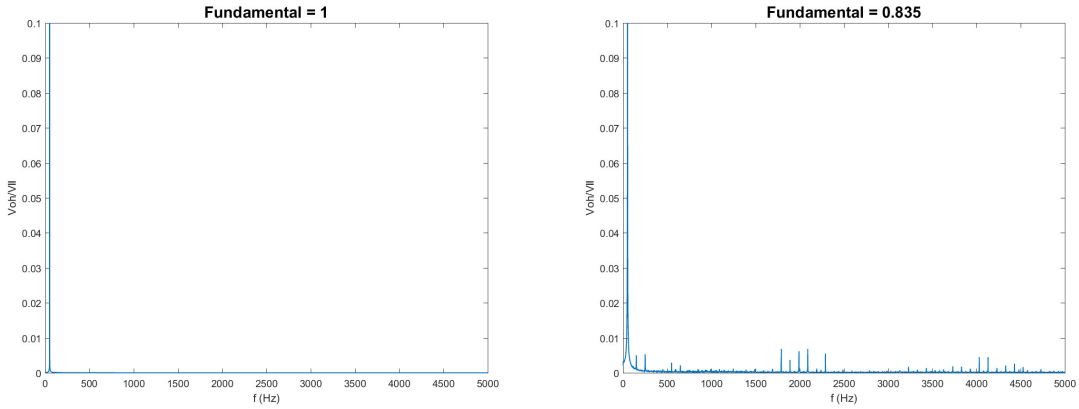

Figure 4.16 – Eleven level configuration: harmonic content of the line to line voltage in charging phase ($I_d = 1$), from the simulation and from the test bench

Looking at the voltage harmonic spectrums, it is possible to state that they are lower in the discharging phase. Moreover comparing with the three level configuration it improves with the increasing of the inverter level.

Eleven level configuration: grid voltage discharging phase

In this paragraph, it is shown the line to line voltage trends from the simulation and from the test bench during a discharging phase (I_d = -1). In Figure 4.17 are represented the line to line voltage measured at the inverter and grid clamps, while in Figure 4.18 there are the associated harmonic spectrums.

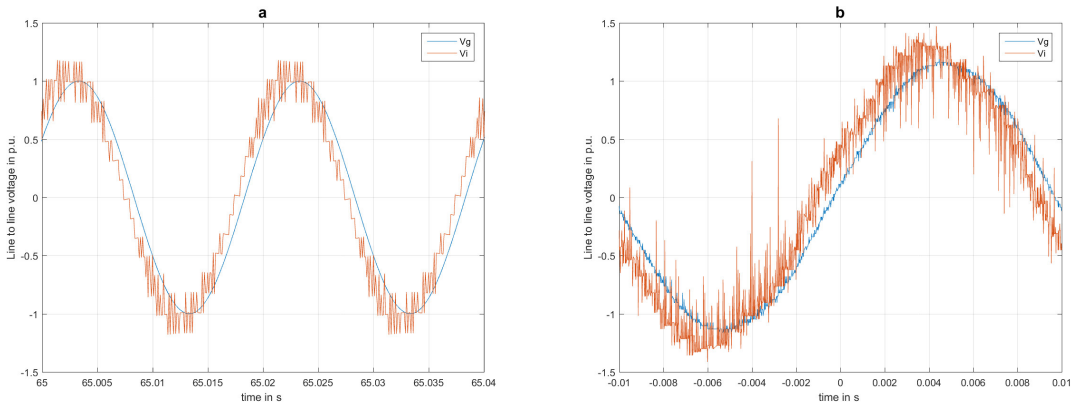

Figure 4.17 – Eleven level configuration: line to line voltage in discharging phase (I_d = -1) from the simulation (a) and from the test bench (b)

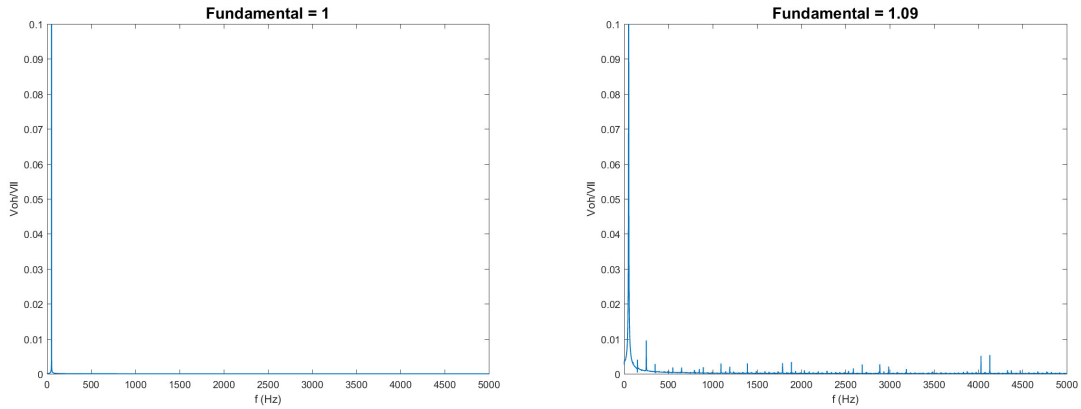

Figure 4.18 – Eleven level configuration: harmonic content of the line to line voltage in discharging phase (I_d = -1), from the simulation and from the test bench

In the case of the eleven level configuration the upper level of the line to line voltage is not perfectly horizontal in charging and discharging case. This trend is due to the change of the charge in the batteries. The direction of the slope change from the charging to the discharging phase.

4.4.2 Eleven level configuration: line current

Eleven level configuration: line current in charging phase

In this paragraph, it is shown the line current trends from the simulation and from the test bench during a charging phase ($I_d = 1$). In Figure 4.19 are represented the line currents measured, while in Figure 4.20, there are the associated harmonic spectrums.

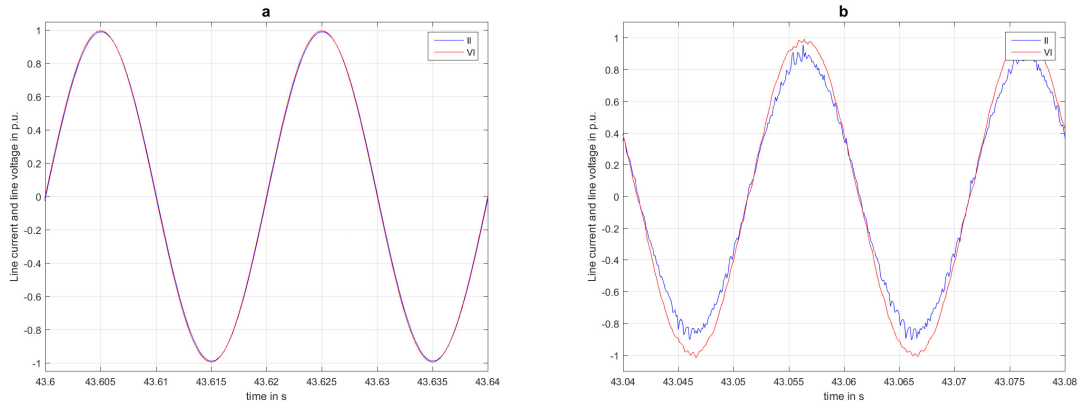

Figure 4.19 – Eleven level configuration: line current and line voltage in charging phase ($I_d = 1$), from the simulation (a) and from the test bench (b)

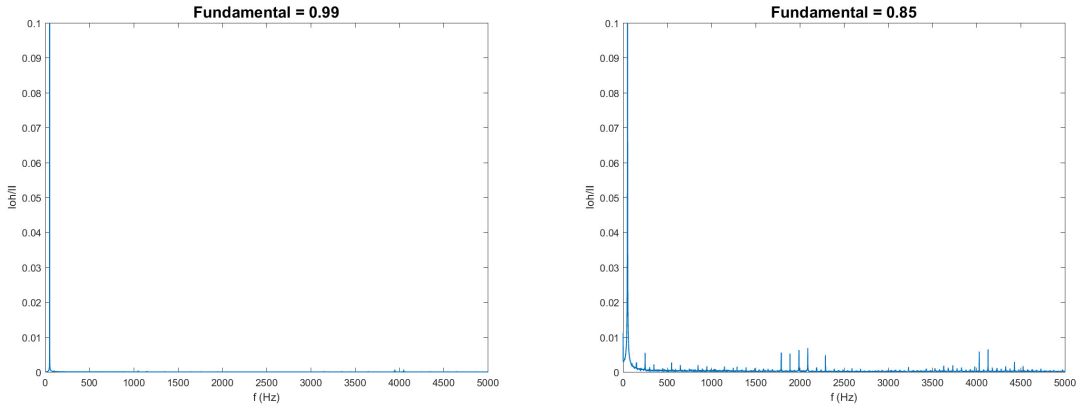

Figure 4.20 – Eleven level configuration: harmonic content of the line current in charging phase (I_d = -1), from the simulation and from the test bench

Comparing the harmonic spectrums of the current of three and eleven configuration, it is possible to see how the results it is much better in the eleven level configuration. The harmonic content and THD improve with the increasing of the level.

Eleven level configuration:line current in discharging phase

In this paragraph, it is shown the line current trends from the simulation and from the test bench during a discharging phase (I_d = -1). In Figure 4.21 are represented the line currents measured, while in Figure 4.22 there are the associated harmonic spectrums.

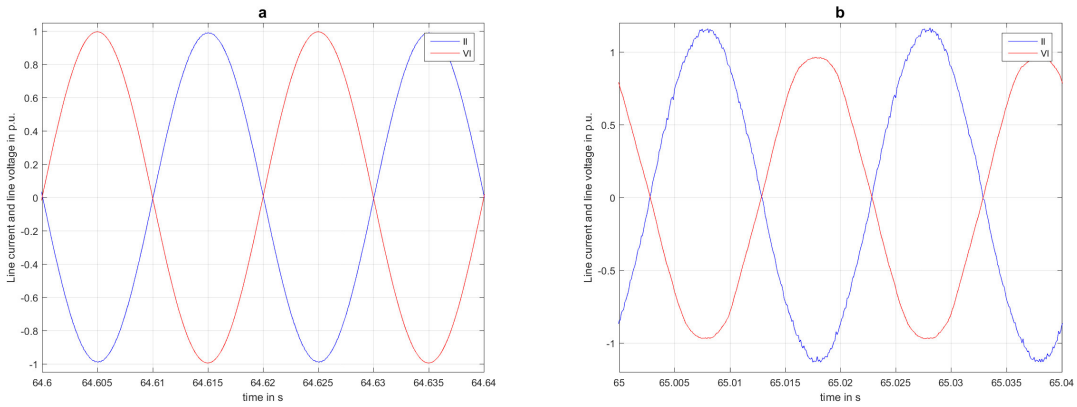

Figure 4.21 – Eleven level configuration: line current and line voltage in discharging phase (I_d = 1), from the simulation (a) and from the test bench (b)

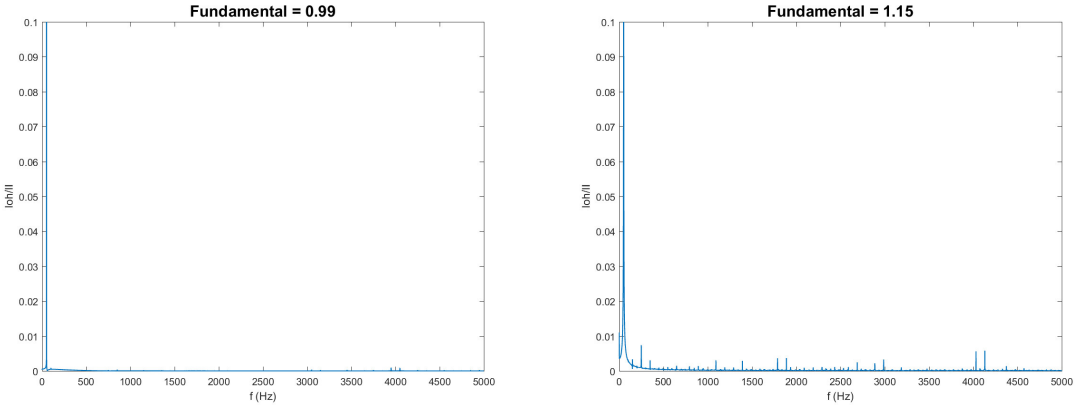

Figure 4.22 – Eleven level configuration: harmonic contents of the line current in discharging phase (I_d = -1), from the simulation and from the test bench

To sum up at the end of these analysis:

- The main issue in the measures is the value of the sample rate. It is inadequate for a complete spectrum analysis. This problem come from the switching frequency choice, due to the small size of the filter in order to obtain a proper operation of the system.
- On the other hand the most important aspect not considered in the simulation has been the transformer. In the next steps it has to be included considering its short circuit impedance. Once it will be included it will be possible to make a more accurate comparison.

5 Conclusions

5.1 Developments and results

The goal of the thesis is to improve the test bench to 17 level with 48 V batteries, looking for critical issues and peculiarities, in order to compare the analysis results with the simulations done in [20].

During the thesis, many aspects of the test bench has been analyzed and many improvement for the development have been done. Among these, the most important themes have been:

- The sizing of the line filter;
- The choice of the switching frequency;
- The controller design;
- The development of the test bench structure (increment of the level);
- The implementation of a more effectiveness security system;

This modifications have been verified with practical tests, which have allowed to improve and verify the solution found in the design stage. All the steps, that has brought to each choice are reported in Chapter 3.

Having implemented the improvements, the results and the comparisons with the simulations, considering the three level and the eleven level configuration, have been collected. From the analysis important aspect have been found, such us the different step response and the relevance of the transformer between grid and test bench. The seventeen level configuration has been reached, however, problems and bad functioning during the matching between the systems, have not allowed the data collection.

5.2 Further implementations

The test bench it is not still able to be connected with the real grid, thus new studies and tests have to be done. An optimization and careful work is necessary in order to obtain a properly operation of the system.
The expected further implementations will be:

- The change of the modules with a new more reliable and effective version. The old modules during the tests have been damaged and repaired many times causing a worsening of efficiency and reliability. Then, being them disposed in series, the problems are overlapped with possible bad functioning of the entire system.
- The new filter has to be installed in order to do measures with lower frequency. The new filter, already bought, is a variable inductance, which will allow to test with different filter inductance values. With lower frequency, a better overview on the harmonics spectrum will be possible with the available instruments. A new filter means new controller parameters, simulations and tests.
- A battery management system (BMS) for the energy storage system is recommended because of the use of a so large amount of batteries. Indeed, considering the working conditions (current until 4C) and their different utilization, the batteries management has been a central point in order to obtain considerable results during the tests.

Bibliography

[1] Sealed Lead-Acid Battery 12V7.0Ah. *Website RS*. 2014. URL: `http://uk.rs-online.com/web/p/lead-acid-rechargeable-batteries` (visited on 09/18/2016).

[2] Infineon Technologies AG. *MOSFET power losses calculation using the data-sheet parameters*.

[3] M. Bertoluzzo. "Internal note from electrical vehicles lectures". 2016.

[4] Bin Wu. *High power converter and AC Drives*. project edition. 445 Hoes Lane Piscataway, NJ 08854: IEEE Press, 2006.

[5] S. Bolognani. "Internal note from electrical drive lectures". 2016.

[6] J.S. Lai R.W. Young G.W. Ott C.P. White J.W. Mckeever D. Chen. "A novel resonant snubber based soft switching inverter". In: *Green High Performance Computing (ICGHPC) 2013*. Ed. by Proceedings of 1995 IEEE Applied Power Electronics Conference and Exposition. 2013.

[7] *CMK2000 CMK3000 magnetoresistive current sensor demoboards data sheet and application notes*.

[8] EEBatt Team. *Website EEBatt team*. 2016. URL: `https://www.eebatt.tum.de/en/technology` (visited on 03/16/2015).

[9] U. A. Egenhofer. "Aufbau und Inbetriebnahme eines prüfstande für dreiphasige fünf Level Cascaded H-bridge Umrichter". Technical University of Munich, 2016.

[10] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems. *Piscataway, NJ, USA, 2003.10.1109/IEEESTD.2003.94285.(Visited on 24/04/2016).*

[11] J. Rodrigez S. Bernet B. Wu J. Ponnt S.Kouro. "Multilevel voltage source converter topologies for industrial medium voltage drives". In: (2007).

[12] J. Rodriguez and Jih-Sheng Lai and Fang Zheng Peng. "Multilevel inverters: a survey of topologies, controls, and applications". In: (2002).

[13] Jih-Sheng Lai and Fang Zheng Peng. "Multilevel converters a new breed power converters". In: (1996).

[14] L. Baruschka A. Mertens. "Comparison of cascaded H-Bridge and modular multilevel converters for BESS application". In: (2011).

[15] L. G. Franquelo and J. Rodriguez and J. I. Leon and S. Kouro and R. Portillo and M. A. Prats. "The age of multilevel converters arrives". In: (2008).

[16] L. Maharjan T. Yamagishi H. Akagi. "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter". In: (2012).

[17] Silicon labs. *Gate driver data sheet 0.5 AND 4.0 AMP ISODRIVERS (2.5 AND 5 KVRMS)*.

[18] Sebastian Lohr. "Internal result data from not already published Bachelor Thesis". 2016.

[19] M. E. Valcher and M. Bisiacco. *Controlli automatici*. Padova: Edizioni libreria progetto Padova, 2008.

[20] S. N. Malik. "Simulation and Analysis of Control and Modulation Schemes for Cascaded H-Bridge Multilevel Inverter". Technical University of Munich, 2016.

[21] MathWorks. *Matlab library PLL block*. 2016. URL: `http://de.mathworks.com/help/physmod/sps/powersys/ref/pll` (visited on 07/18/2016).

[22] M. Andriollo G. Martinelli A. Morini. *Macchine elettriche rotanti*. 1981.

[23] N. Mohan T.M. Undeland W.P. Robbins. *Elettronica di potenza*. Hoepli, 2005.

[24] Nise S. Norman. *Control systems engineering*. 2004.

[25] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems. *in IEEE Std 519-2014 (Revision of IEEE Std 519-1992), pp. 1–29, 2014*.

[26] S. Daher. *Analisys design and implementation of a high efficiency multilevel converter for renewable energy system*. Kassel: Kassel University press, 2006.

[27] L. A. Serpa. "Current Control Strategies for Multilevel Grid Connected Inverters". Swiss institute of technology Zurich, 2007.

[28] Z. Shen. "Control techniques of a modular CHB multilevel converter". Technical University of Munich, 2014.

[29] T. Lahlou M. Abdelrahem S. Valdes. "Filter design for grid connected multilevel CHB inverter for battery energy storage systems". In: (2016).

[30] *Voltage trasducer LV 25-600 data sheet*.

List of Figures

List of Tables