Università degli Studi di Padova

DIPARTIMENTO DI INGEGNERIA DELL' INFORMAZIONE

Corso di Laurea Magistrale in Ingegneria Elettronica

Design of a UWB Pre-Driver Amplifier in 130 nm BiCMOS Technology for Sub-6GHz Applications

Tesi svolta presso Infineon Technologies Austria AG

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Anno Accademico 2021-2022
11 Aprile 2022

Sommario

La presente tesi propone il progetto di un amplificatore di potenza Pre-Driver a banda ultra-larga per applicazioni delle radio frequenze (RF), in particolare quelle inerenti al 5G al di sotto dei 6 GHz. Gli amplificatori di potenza RF ricoprono un ruolo importante nella catena di trasmissione, ovvero quello di essere i principali responsabili dell'amplificazione del segnale modulato in ingresso. Allo stesso tempo, però, tali amplificatori possono rappresentare una sorgente di distorsione non trascurabile che tende a distorcere il segnale modulato, e questo può portare ad un peggioramento generale delle prestazioni dell'intero sistema di comunicazione. Lungo il percorso del segnale al trasmettitore, l'amplificatore Pre-Driver assume un ruolo chiave nel processo di amplificazione, aiutando l'intero sistema con le sue prestazioni in termini di linearità. Lo scopo principale di questo lavoro è quello di analizzare, tramite modelli e simulazioni, le architetture allo stato dell'arte e le tecniche principali utilizzate per il miglioramento delle prestazioni in termini di banda e linearità di amplificatori Pre-Driver che operano nel range dei GHz, secondo lo standard 5G FR1. Il progetto è stato realizzato utilizzando la tecnologia di Infineon SiGe BiCMOS 130 nm.
La tesi inizia con un capitolo introduttivo sulle principali applicazioni dell'amplificatore Pre-Driver, per poi presentare la struttura del lavoro svolto. A seguire, viene introdotto il secondo capitolo, che racchiude le figure di merito e le nozioni base riguardanti gli RF Power Amplifier (PA), in modo da poter poi comprendere al meglio il contenuto dei capitoli successivi. Il cuore di questo lavoro, invece, è racchiuso nel capitoli tre e quattro, i quali presentano l'analisi e il progetto dell'amplificatore Pre-Driver a banda ultra-larga in versione single-ended. Attraverso la presentazione dei criteri di progetto adottati, vengono evidenziati anche i suoi passi più cruciali e l'approccio risolutivo con cui sono stati affrontati. La tesi si conclude con l'illustrazione del layout del test chip e dei risultati ottenuti. In particolare, l'amplificatore a banda ultra-larga Pre-Driver mostra alla frequenza operativa ($f_0 = 3.6\ GHz$) un livello di potenza in uscita al P1dB di 27.4 dBm, un guadagno in potenza di 19.5 dB, e un OIP3 di 37 dBm, ad una tensione di alimentazione di 5 V. Una delle caratteristiche principali del progetto è sicuramente il fatto che tutte le prestazioni sono raggiunte in una larghezza di banda molto ampia di 3.2 GHz, che spazia tra 1.8 GHz e 5 GHz.

Abstract

This thesis proposes the design of a Ultra-Wide-Band (UWB) Pre-Driver radio frequency (RF) Amplifier for sub-6GHz 5G applications.
The RF Power Amplifiers (PAs) play the significant role of the main amplification of the input modulated signal in the RF transmit chain. At the same time, they could represent a not negligible source of distortion, which can distort the input signal and worsen the general performances of the whole communications system. Through the transmitter signal path, the Pre-Driver acts as a key element in the amplification process by aiding the whole system with its competitive linearity performances.
The main purpose of this work is the investigation, via modeling and simulation, of state-of-the art architecture and techniques focused on bandwidth and linearity improvement of Pre-Driver RFPA design in Infineon BiCMOS 130 nm technology operating in the GHz range, according to 5G FR1 standard. The thesis starts with an introduction chapter containing the main Pre-Driver applications and the thesis organizations. After that, the main figures of merit and the basic notions concerning the RFPAs are presented in the second chapter, since this can aid to deepen the following ones. The core of this work is embodied in the third and the fourth chapters which present the analysis and the design of the concerned UWB Pre-Driver amplifier in single-ended fashion. The design criteria adopted will be presented next to the main though steps that could affect the amplifier performances, with their relative proposed solutions. The thesis concludes with the presentation of the test chip layout and the simulation results. In particular, the UWB class AB single-ended Pre-Driver shows, at $f_0 = 3.6\ GHz$, a P1dB output power level of 27.4 dBm, with a power gain of 19.5 dB, and a OIP3 of 37 dBm, at a supply voltage of 5 V. One of the main characteristic of the proposed design is that the performances are almost achieved in a wide bandwidth range of 3.2 GHz, spacing from 1.8 GHz to 5 GHz.

Ringraziamenti

Questo lavoro è il frutto del mio percorso di tirocinio trascorso presso Infineon Technologies a Villach, ma è anche la conclusione di un'esperienza molto più lunga vissuta durante i miei anni di studio a Padova. In questi pochi spazi, vorrei ringraziare le persone più significative che hanno contribuito alla mia crescita, sia professionale che personale.

Prima di tutti, vorrei ringraziare la mia grande famiglia, in particolare i miei genitori Michela e Mario, i miei fratelli Francesca e Matteo e i miei nonni Francesco e Paola, che hanno sempre creduto in me, esortandomi a dare il meglio in ogni situazione. Senza di loro, nulla di tutto questo sarebbe stato possibile.

Ringrazio il mio relatore, il Prof. Bevilacqua, e il mio responsabile presso l'ente ospitante, Simone, per l'opportunità lavorativa concessa che mi ha permesso di arricchire le mie conoscenze. Ringrazio anche il mio supervisore, e mentore, Stefan, che con estrema calma e precisione mi ha insegnato non solo nozioni preziose, ma anche un approccio efficace alla risoluzione di problemi. Un sentito ringraziamento anche a Jacopo che mi ha aiutato negli step finali della realizzazione del chip e ha contribuito a migliorare le giornate tra una chiacchiera e un caffè.

Ringraziamento particolare al mio collega, coinquilino e amico, Marco. In questi mesi abbiamo maturato un buon rapporto di amicizia, supportandoci a vicenda nei momenti sia di traguardo che di sconforto. Ringrazio anche il mio collega tesista, Cristian, con cui ho condiviso le mie giornate di lavoro, tra pensieri e risate.

Infine, ma di sicuro non per importanza, un ringraziamento speciale a Irene per essere sempre stata al mio fianco in questi ultimi anni, per avermi appoggiato ed anche sopportato. Hai sempre creduto in me e mi hai spinto ad essere una persona migliore.

Davide Regis

Padova, 11 Aprile 2022.

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Chapter 1

Introduction

The wireless communications industry has been undergoing tremendous shifts in the last few years. With the ever-growing demand of higher data-rates and improved user experience, the RFICs production increases sharply, especially with the new 3GPP standards. As a matter of fact, every wireless communications system transmits through an antenna which is connected to a PA. The new 5G technology development is steering the RF PAs research trend, which leads to an investigation of ever-more performing PAs in terms of bandwidth, linearity and efficiency.

The majority of the world's RF wireless power amplifiers products are still designed in III-V semiconductors nowadays. However, by taking advantage of *nm* silicon devices and novel RF system-on-a-chip (SoC) design techniques, highly competitive silicon RF PAs in SiGe BiCMOS technologies have recently reported in many works with performance rivaling those of the III-V RF PAs.

In the RF transmit chain, the Pre-Driver building blocks play a significant role. The main purpose of this chapter is to introduce their usefulness for sub-6GHz 5G applications. Afterwards, the thesis organization will be presented.

1.1 Applications

A Pre-Driver RFIC is an high linear RF power amplifier. In this kind of circuit, the high linearity is a primary target to achieve, even more relevant than the efficiency. Its major use is at the transmitter in a typical wireless communications system.

The primary issue of the power amplification of amplitude modulated RF signals is that the envelope, and hence the modulating signal, will be distorted if the amplifier is used at its full nominal power level. This is due

to the highly non-linear behavior of this kind of devices. After witnessed that, the most remarkable trade-off in the RF PAs design which has to be considered is the *linearity-efficiency* one. This can be also shown on the four types of PAs class operation: in class A, for example, we can achieved high linearity but with a significant loss of efficiency, whilst in class B, we gain more efficiency at the price of linearity.

In order to deepen the Pre-Driver's job in the RF transmit chain, a streamlined block scheme is reported in Fig 1.1. It can be seen that the Pre-Driver stage is placed before the driver one and the Doherty PA. The latter is a performing efficiency enhancement technique which involves the use of two power amplifiers called main (M) and peak (P). This technique allows to realize an amplification process with higher efficiency over a wide range of output power at the expense of linearity and consumption.

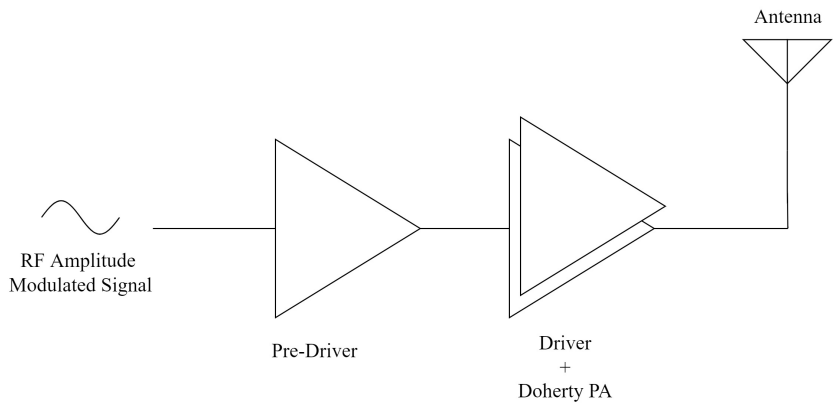


Figure 1.1: General RF transmit chain

Basically, the Pre-Driver's pursuit is to amplify a weak RF amplitude (or phase) modulated signal with high-linearity performance. The resulting signal will be given in input to the driver and Doherty PA stage. One of the most considerable facts is that the output signal of the Pre-Driver has to be much linear as far as possible, in order to minimize any distortion in the further stages. Given that, the Class AB will be probably the best choice of operating class for this circuit topology, since it offers a worthy trade-off between a desirable linearity and a reasonable efficiency. It is important to realize that the Pre-Driver stage acts as a key element in the RF transmit chain, and his performance affects the whole signal process.

1.2 Thesis Organization

In chapter 2 are presented the main figures of merit and the most remarkable considerations in the RF PAs design. It will be also reported the technology involved and the radio frequency design information concerning stability.

In chapter 3 are illustrated the target specifications and the design of a Ultra-Wide-Band (UWB) class AB Pre-Driver amplifier in single-ended version. There will be also presented the design criteria adopted for the main building blocks, including the core stage and the input and output matching networks.

In chapter 4 are shown the on-chip coils design and their performances at different temperature corner conditions.

In chapter 5 are shown the whole layout of the test-chip, including also the layout of the different building blocks.

In chapter 6 are presented the simulation results and their comments.

In chapter 7 are summarized the conclusions of this work.

Chapter 2

RF Power Amplifier Design

2.1 Figures of merit

In this section, there will be presented the main figures of merit that are extremely relevant during the principal RF PA design steps.

2.1.1 Output Power

The *output power* is defined as the power flowing into the load. Consider the generic power amplifier schematic reported in Fig. 2.1. It is important to notice that the output voltage and current are sinewaves, therefore the desired output power will be referred to a single operating frequency and the harmonics power is suppressed.

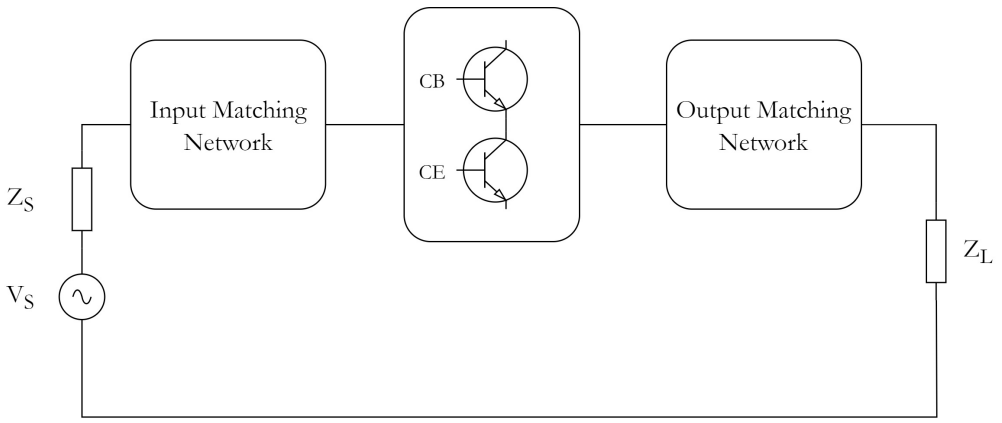


Figure 2.1: Generic PA schematic

Assuming that the load is purely resistive (typically 50 Ω), so $Z_L = R_L$, we can defined the output power as:

$$P_{out} = \frac{V_{out}^2}{2 \cdot R_L} \tag{2.1}$$

2.1.2 Linearity - OP1dB and IP3

The distortion is a significant phenomenon that involved the majority of electronic circuits, since they are composed by non-linear devices, such as transistors and diodes. They are the main origin of spurious frequency contribution. When a typical small signal analysis is performed, it is assumed that the input signal is small enough in order to consider the circuit response as linear while neglecting the spurious frequency terms.

In order to deeply understand the role of the distortion, we can represent a generic transfer function of a non-linear system with a power series in the following fashion:

$$s_{out} = a_0 + a_1 s_{in} + a_2 s_{in}^2 + a_3 s_{in}^3 + \cdots \tag{2.2}$$

where s_{out} and s_{in} are, respectively, the output and the input signals, while a_i coefficients represent the response of the system. The coefficient a_0 stands for the DC component of the system, a_1 is the linear gain of the system (*which can be seen as the small-signal gain*), whilst a_2, a_3, ..., represent the distortion of the system.

Assuming that the input signal is a pure, sinusoid $s_{in} = A_{in} \cdot \cos(\omega t)$, the output signal can be expressed as:

$$\begin{aligned} s_{out} &= a_0 + a_1 A_{in} \cos(\omega t) + a_2 A_{in}^2 \cos(\omega t) + a_3 A_{in}^3 \cos(\omega t) + \cdots \\ &= \left(a_0 + \frac{a_2 A_{in}^2}{2}\right) + \left(a_1 A_{in} + \frac{3 a_3 A_{in}^3}{4}\right) \cos(\omega t) + \\ &\quad + \frac{a_2 A_{in}^2}{2} \cos(2\omega t) + \frac{a_3 A_{in}^3}{4} \cos(3\omega t) + \cdots \end{aligned} \tag{2.3}$$

where in the last step of Eq. 2.3, the known trigonometric relations $\cos^2(x) = (1+\cos(2x))/2$ and $\cos^3(x) = (3\cos(x)+\cos(3x))/4$ are used. It can be noticed that the distortion produces harmonics at multiple of fundamental frequency. It can be also seen that the second order distortion generates a DC offset too, and the third order distortion is responsible for gain compression, since often $a_3 < 0$.

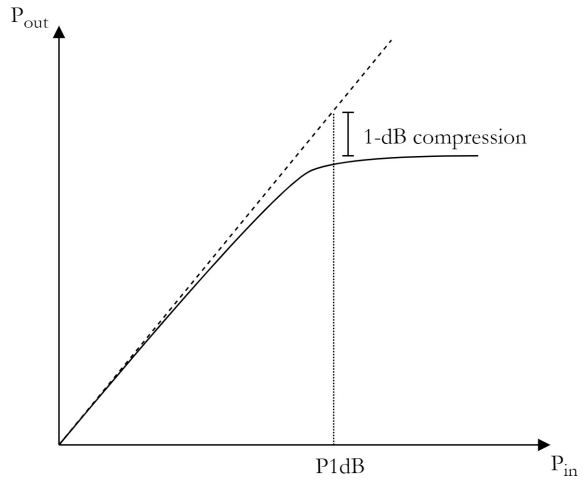


Figure 2.2: Illustration of 1-dB compression point concept

There are several figures of merit which can describe the distortion. The two most relevant for this work are *1-dB compression point* (P1dB) and *third-order intercept point* (IP3). The first one is defined as the input power level which produces a gain drop of 1 dB with respect to the ideal case. This concept is illustrated in Fig. 2.2.

For what concerned the IP3, it is necessary to introduce the concept of Intermodulation Distortion (IMD) before. Since now, we consider a single tone at the input of our non-linear system, but we need to analyze its behavior with two tones. Let's apply two sinusoids at the input, so now the input signal can be written as:

$$s_{in} = A_1 \cdot \cos(\omega_1 t) + A_2 \cdot \cos(\omega_2 t) \tag{2.4}$$

Hence, if we substitute the Eq. 2.4 in the Eq. 2.2, it can be noticed that few terms will appear at the sum or the difference of the two fundamental tones ($\omega_1 - \omega_2$, $\omega_1 + \omega_2$, $2\omega_1 + \omega_2, \cdots$), which are called *nth-order intermodulation products* (IM_n). Hence, we can derive a general expression for the IM_n:

$$IM_n = \frac{amplitude\ of\ nth - order\ IM\ product}{amplitude\ of\ the\ fundamental} \tag{2.5}$$

Witnessed that, it can be established that IP3 indicates how large a signal the device can process before the IM_3 occurs. The Fig. 2.3 reports this notion. The higher the output at the intercept, the better the linearity and the lower will be the IM distortion.

Generally speaking, PAs operating at or beyond the 1-dB compression point require more careful treatment, since the nonlinearities become "strong" and arise through the cutoff and clipping behavior of the transistor. The third-order nonlinearity is, undoubtedly, an important contributor to compression and saturation effects.

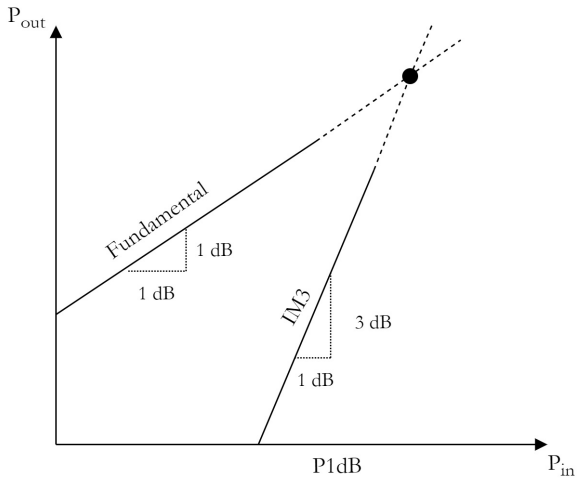


Figure 2.3: Illustration of IP3 curves

2.1.3 Power Gain

Consider a generic series impedance $Z = R + jX$ crossed by a current I and with a voltage V at its terminals. In many electronics application, the signal which carry a useful information is usually the voltage V, like in the filters where V stands for the state variable. At High Frequencies (HF), we could also take *active power* as the useful signal, which is defined as:

$$P = \Re\left(\frac{1}{2}VI^*\right) = \frac{1}{2}R_S|I|^2 = \frac{1}{2}\cdot\frac{|V|^2}{R_S} \tag{2.6}$$

Now let's consider a generic source impedance $Z_S = R_S + jX_S$ and a load impedance $Z_L = R_L + jX_L$. Given Z_S, we might wonder what is the value of Z_L that maximizes the power delivered to the load. The voltage across the load is:

$$V_L = V_S \cdot \frac{R_L}{R_L + jX_L + R_S + jX_S} \tag{2.7}$$

Hence, the active power delivered to the load will be:

$$P_L = \frac{1}{2} \cdot \frac{|V_L|^2}{R_L} = \frac{1}{2} \cdot \frac{|V_S|^2}{R_L} \cdot \frac{R_L^2}{(R_L + R_S)^2 + (X_S + X_L)^2} \tag{2.8}$$

Clearly, the choice of $X_L = -X_S$ minimizes the denominator of P_L. With this condition, $\frac{\partial P_L}{\partial R_L} = 0$ yields $R_L = R_S$, so the condition for maximum power delivered to the load is:

$$Z_L = Z_S^* \tag{2.9}$$

The state of Eq. 2.9 is called *power matching*. The power to the load under this condition is the maximum power the source can deliver, that is the *available power*. So one has:

$$P_{av,S} = P_L\Big|_{Z_L = Z_S^*} = \frac{1}{2} \cdot \left|\frac{V_S}{2}\right|^2 \cdot \frac{1}{R_S} = \frac{1}{8} \cdot \frac{|V_S|^2}{R_S} \tag{2.10}$$

Now, if we consider the generic two-port network scenario reported in Fig. 2.4, we can define two relevant figures of merit. The *transducer gain* of the two-port network will be the ratio of the power delivered to the load and the source available power, that is:

$$G_T = \frac{P_L}{P_{av,S}} \tag{2.11}$$

Whereas, the *power gain* of the two-port network is the ratio between the power to the load and the input power:

$$G_P = \frac{P_L}{P_{in}} \tag{2.12}$$

Furthermore, it can be noticed that if $Z_S^* = Z_{in}$, we are in power matching condition, so $P_{in} = P_{av,S}$, and therefore:

$$G_P\Big|_{Z_S^* = Z_{in}} = G_T \tag{2.13}$$

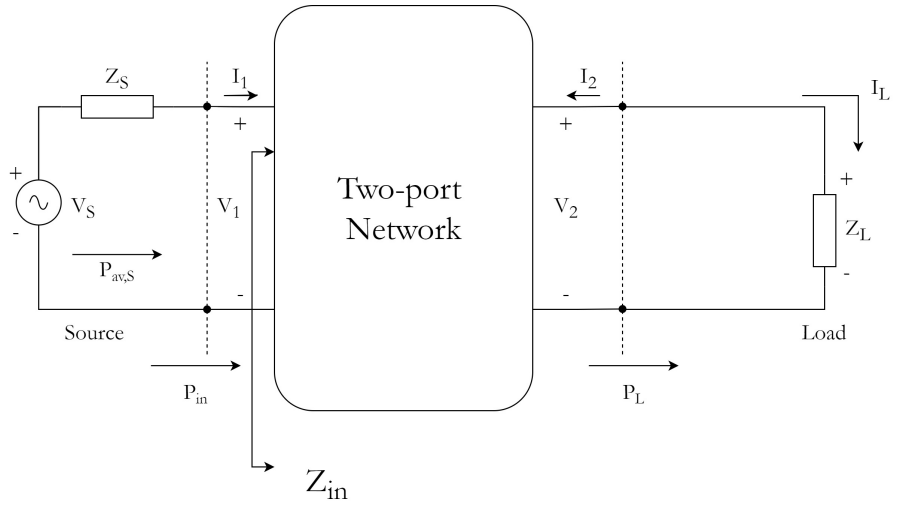


Figure 2.4: Generic 2-port network power transfer scenario

2.1.4 Efficiency

Efficiency is a crucial parameter for RF power amplifier. It can be a useful yardstick for the different classification of the PA, but also it can help to deeply understand how the input power is handled and how much the DC power consumption affects. Two efficiencies will be relevant for this work: the *collector efficiency (CE)* and the *power added efficiency (PAE)*.

The *collector efficiency* is defined as the ratio between the output power and the power provided from the DC source:

$$CE = \frac{P_{out}}{P_{DC}} \tag{2.14}$$

The *Power Added Efficiency* (PAE) is the ratio between the output power and the input power to the DC power supply:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.15}$$

It can be noticed that PAE takes into account the input drive power. For this reason, it is preferable choose devices with higher PAE than higher CE.

2.2 Network Analysis Basics

The aim of this section is to recall some useful basics tools for a typical network analysis which have been used in this work. Furthermore, a brief derivation of Smith Chart is presented, reproposing the analysis reported in [2] .

2.2.1 Smith Chart

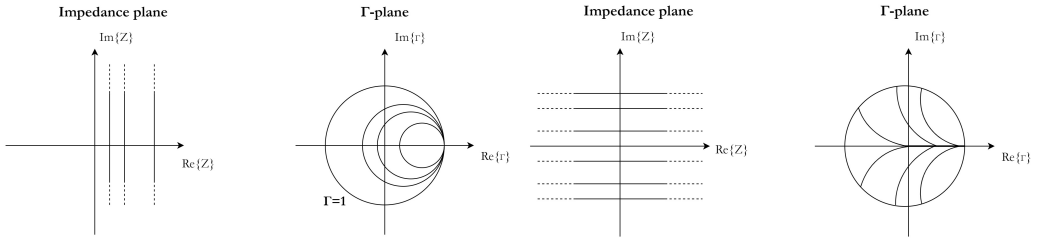
The primary role of the Smith chart is to provide a standard way to present impedance or reflectance data. Recall the well-known expression of the reflection coefficient in terms of the normalized load impedance:

$$\Gamma = \frac{\frac{Z_L}{Z_0} - 1}{\frac{Z_L}{Z_0} + 1} = \frac{z_L - 1}{z_L + 1} \tag{2.16}$$

where z_L indicates the normalized load impedance. It is important to emphasize that the relationship between z_L and Γ is bi-unique, so the familiar curves of the Smith Chart are simply a plotting, in the Γ-plane, of contours of constants resistance and reactance. Moreover, we can state that this mapping is a *bilinear transformation* because it is a ratio of two linear functions. Among the various properties of bilinear transformations, a particularly relevant one is that circles remain circles when mapped. In this context, a line is considered a circle of infinite radius.

With the aid of Eq. 2.16, it is straightforward to show that the imaginary axis of Z-plane maps into the unit circle in the Γ-plane, while other lines of constants resistance in the Z-plane map into circles of varying diameter that are all tangent at the point $\Gamma = 1$. Lines of constant reactance are orthogonal to lines of constant resistance. Since lines map to lines or circles, we expect constant-reactance lines to transform to the circular arcs. An illustration of this concept is reported in Fig. 2.5.

The center of the Smith Chart corresponds to $\Gamma = 0$ and so a resistance equal to the normalizing impedance. The bottom half of the Z-plane maps into the bottom half of the unit circle in the Γ-plane, therefore, capacitive impedances are always found there. Likewise, the top half of the Z-plane corresponds to the top half of the unit circle and inductive impedances. Progressively smaller circles of constant resistance correspond to progressively larger resistance values.



(a) (b)

Figure 2.5: Mapping of constant-resistance lines in Z-plane to circles in Γ-plane (a). Mapping of constant-reactance lines in Z-plane to contours in Γ-plane (b).

2.2.2 The Scattering Matrix

It is often valuable to use a higher-level description of the device under test, especially to simplify the analysis of the system concerned. With the aid of *scattering parameters*, the reflectance behavior of the whole system can be derived. If we consider a generic n-port network, we can defined the normalized voltage and current waves at each port as:

$$\begin{aligned} a_i &= \frac{V_i^+}{\sqrt{Z_{0,i}}} = I_i^+ \sqrt{Z_{0,i}} \\ b_i &= \frac{V_i^-}{\sqrt{Z_{0,i}}} = I_i^- \sqrt{Z_{0,i}} \end{aligned} \tag{2.17}$$

where a_i is the *forward wave*, meanwhile b_i is the *backward wave*. It is useful to link these quantities especially when we are dealing with radio frequencies applications. Hence, we can express the behavior of any linear time invariant n-port network as the superposition of normalized waves:

$$\begin{bmatrix} b_1 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots \\ \vdots & \ddots & \\ S_{n1} & & S_{nn} \end{bmatrix} \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} \tag{2.18}$$

Each scattering parameter is defined as:

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0,\ \forall\ k \neq j} \tag{2.19}$$

Furthermore, it can be noticed that:

$$\frac{b_i}{a_i} = \frac{V_i^-}{V_i^+} = \Gamma_i \tag{2.20}$$

The normalized waves are linked to the active power of the forward and backward waves in the following fashion:

$$\begin{aligned} P_i^+ &= \frac{1}{2} V_i^+ (I_i^+)^* = \frac{1}{2} \frac{|V_i^+|^2}{Z_{0,i}} = \frac{1}{2} |a_i|^2 \\ P_i^- &= \frac{1}{2} V_i^- (I_i^-)^* = \frac{1}{2} \frac{|V_i^-|^2}{Z_{0,i}} = \frac{1}{2} |b_i|^2 \end{aligned} \tag{2.21}$$

Hence, the active power that flows into one port is:

$$\begin{aligned} P_i = \Re\left(\frac{1}{2} V_i I_i^*\right) &= \Re\left(\frac{1}{2Z_{0,i}} (V_i^+ + V_i^-)(V_i^+ - V_i^-)\right) \\ &= \frac{1}{2}\left(|a_i|^2 - |b_i|^2\right) \end{aligned} \tag{2.22}$$

2.2.3 Z-matrix

If we combine $V_i = V^+ + V^-$ and $I_i = I^+ - I^-$ with the definition of a_i, b_i, we can state:

$$\begin{aligned} V_i &= \sqrt{Z_{0,i}} (a_i + b_i) \\ I_i &= \frac{1}{\sqrt{Z_{0,i}}} (a_i - b_i) \end{aligned} \tag{2.23}$$

Hence,we can defined the *Z-matrix* in a similar fashion with respect to the *S-matrix* in order to find out the behavior of the various impedances of the different ports. It can be expressed as:

$$\begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \dots \\ \vdots & \ddots & \\ Z_{n1} & & Z_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} \tag{2.24}$$

Furthermore, the S and Z matrices are related as:

$$\underline{Z} = (U + S)(U - S)^{-1} \tag{2.25}$$

where $\underline{Z}$ is the normalized impedance matrix with $Z_{ij} = \frac{Z_{ij}}{\sqrt{Z_{0,i}Z_{0,j}}}$.

In addition, we can use the reflection coefficient to evaluate how close Z is to the target value Z_0. In the case of a two-port network, the S-parameters S_{11} and S_{22} could be a well yardstick to represent the *return loss* (RL) at the input and output port, respectively. This mean that if, for example, $S_{11}[dB] = -10\ dB$, then only the 10 % of the power is reflected back.

2.2.4 H-Parameters

Hybrid parameters are known as "hybrid" as they use Z-parameters, Y-parameters, voltage and current ratios to represent the relationship between V and I in a two-port network. H-parameters are useful in describing the input-output characteristics of circuits where it is hard to measure Z or Y parameters such as the active devices. They encapsulate all the important linear characteristics of the circuit and the relationship between voltages and currents in H-parameters can be represented as:

$$\begin{aligned} V_1 &= h_{11}I_1 + h_{12}V_2 \\ I_2 &= h_{21}I_1 + h_{22}V_2 \end{aligned} \tag{2.26}$$

Hence, it can be turned out the different H-parameters afterwards. The ratio of input voltage to input current at short circuited output port is:

$$\left.\frac{V_1}{I_1}\right|_{V_2=0} = h_{11} \tag{2.27}$$

This is referred as the *short circuit input impedance*. Then, the ratio of the output current to input current at the short-circuited output port is:

$$\left.\frac{I_2}{I_1}\right|_{V_2=0} = h_{21} \tag{2.28}$$

which is the *short-circuit current gain* of the network. Now, if we open circuit the port 1 ($I_1 = 0$), we can derive the *open circuit reverse voltage gain* as follow:

$$\left.\frac{V_1}{V_2}\right|_{I_1=0} = h_{12} \tag{2.29}$$

and the *open circuit output admittance* as:

$$\left.\frac{I_2}{V_2}\right|_{I_1=0} = h_{22} \tag{2.30}$$

2.3 Conduction Angle

One of the most important parameter in RF PA design is certainly the *conduction angle*. It is a very valuable yardstick to classify the different class of operation of the PAs. Basically, the conduction angle (α) indicates the portion of the signal period in which the active devices conduct. It is immediately evident that if α is equal to the whole period, *i.e.* 2π, the transistors are always conducting and so the efficiency will drop sharply. At the same time, the linearity of the circuit increases because the active part (transistor) is never switched off during the entire period.

The basic process of reducing the conduction angle is illustrated in Fig 2.6. The analysis recalls the one proposed in [4] and it will be performed using the conduction angle to characterize the waveforms of each class of operation of PAs. The concerned device is biased to a quiescent point beyond the Class A condition, toward cutoff. Under the hypothesis of working with quiescent voltage V_q and signal voltage V_S both normalized, it is possible to define:

$$V_S = (1 - V_q) \tag{2.31}$$

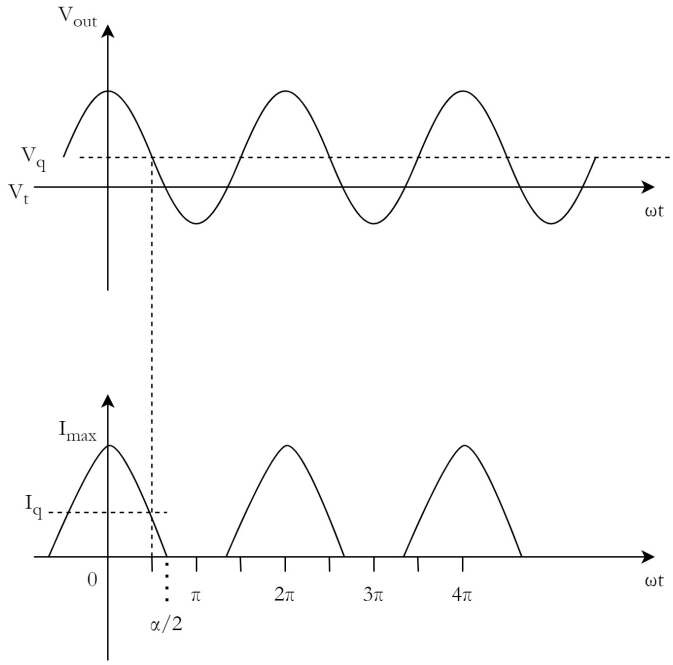


Figure 2.6: Generic voltage and current waveforms of the described amplifier.

Initially, it will be assumed that I_{max} is maintained constant while V_q and V_S change. Furthermore, it will be assumed that the concerned device

is ideally transconductive, and that the output voltage is being maintained above zero to keep the device turned on.

As stated before, the conduction angle α indicates the proportion of the RF cycle for which conduction occurs. The figure 2.6 reported the described waveforms, where to obtain the right value for the normalized voltage V_q must be $V_t = 0$ and $V_0 = 1$. Looking at the current waveform, it is quite intuitive that the bias level I_q decreases as the conduction angle α is reduced. In order to deepen the behavior of the fundamental component, it is necessary to perform the Fourier analysis of the concerned waveforms.

The RF current waveform can be written as:

$$i_c(\theta = \omega t) = \begin{cases} I_q + I_{pk}\cos\theta, & -\alpha/2 < \theta < \alpha/2 \\ 0, & -\pi < \theta < -\alpha/2; -\alpha/2 < \theta < \pi \end{cases} \tag{2.32}$$

At this point, it is possible to state:

$$I_{pk} = I_{max} - I_q \tag{2.33}$$

and since $i_c(\theta) = 0$ for $\theta = \alpha/2$, then:

$$\cos\left(\frac{\alpha}{2}\right) = -\left(\frac{I_q}{I_{pk}}\right) \tag{2.34}$$

hence i_c can be rewritten as:

$$i_c(\theta) = \frac{I_{max}}{1 - \cos(\frac{\alpha}{2})}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right) \tag{2.35}$$

Now it is possible to perform the Fourier analysis on the current waveform in order to decompose it in its spectral components, like the mean value, which is the DC component (maximum):

$$I_{dc,max} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\frac{\alpha}{2})}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right) d\theta \tag{2.36}$$

and the magnitude of the n-th harmonic, given by:

$$I_{n,max} = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\frac{\alpha}{2})}\left(\cos\theta - \cos\left(\frac{\alpha}{2}\right)\right)\cos(n\theta)\, d\theta \tag{2.37}$$

Solving the integrals for the mean value and the first harmonic, one has:

$$I_{dc,max} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{2.38}$$

$$I_{1,max} = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \tag{2.39}$$

Examines the curve of Figure 2.7 more closely, it is evident that the DC component decreases monotonically as the conduction angle is reduced. In particular, it can be turned out:

$$\begin{aligned} I_{dc,max}(\text{Class B}) &= I_{max}/\pi \\ I_{dc,max}(\text{Class A}) &= I_{max}/2 \\ I_{1,max}(\text{Class B}) &= I_{max}/2 \\ I_{1,max}(\text{Class A}) &= I_{max}/2 \end{aligned}$$

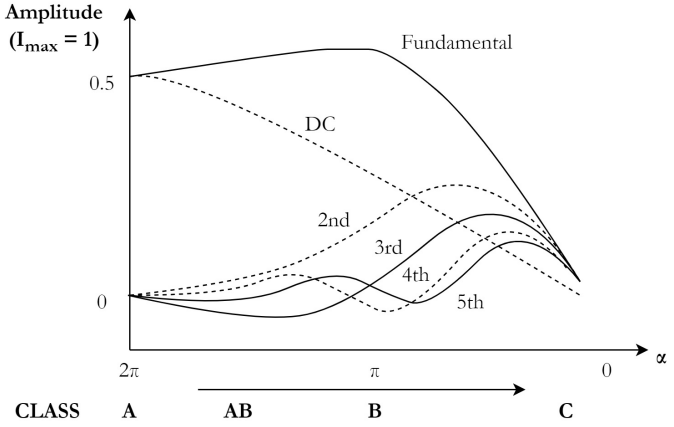


Figure 2.7: Fourier analysis of reduce conduction angle current waveforms [4].

In addition, it can be noticed that throughout the Class AB range, and up to the midway Class B condition ($\alpha = \pi$), the largest harmonic, other than the fundamental, is the second due to the action of the partially cutoff transistor. Basically, this action leads to a significant reduction of the dips of the fundamental sinewave and a sharpness of the peaks. Furthermore, the odd harmonics can be seen to pass through zero at the Class B point, but in AB mode, the third harmonic is undoubtedly not negligible.

Typically the Class AB condition is the most suitable choice for RFPAs design, since it offers a worthy trade-off between linearity and efficiency. The illustration reported in figure 2.8 supports this choice. As it is possible to observe, between Class A and Class B modes the delivered RF output power is the same, but with a significant difference in terms of efficiency due to the reduced DC biasing.

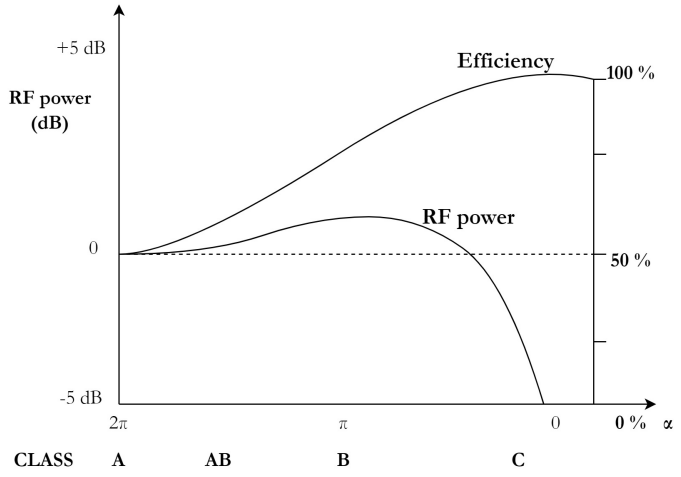


Figure 2.8: RF power and Efficiency vs conduction angle [4].

2.4 Stability Analysis

Nyquist theorem provides a safe indication of stability at low frequency. As the frequencies goes up, it is necessary to looking for other aids in order to guarantee a stable system, not only in the band of interest. In this section, some useful stability check tools and hints on avoiding RF oscillation will be presented.

2.4.1 Sources of instability

Before getting specific, it might be worthwhile to recognize the main origins of instabilities in RF circuits. Clearly, the RF transistor might be one of them, since it is in charge of the power amplification. In order to deepen the mechanism, the proposed analysis shown in [4] is summed up here, aiming to show in a pragmatic approach which are the possible causes of oscillation.

In figure 2.9 it is reported the schematic of a generic RF BJT model where the output is decoupled with a series load impedance Z_L. In this analysis,

input and output capacitors are supposed to be negligible at the frequency of interest.

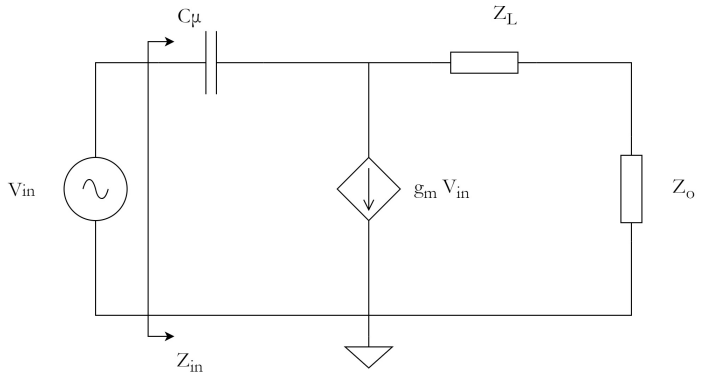


Figure 2.9: Simplified RF BJT equivalent model [4].

If we compute the input impedance Z_{in}:

$$Z_{in} = \frac{Z_L + \frac{1}{j\omega C_\mu}}{1 + g_m Z_L} \tag{2.40}$$

It is possible to analyze the two extreme cases of open and short circuit terminations:

$$\begin{aligned} Z_{in} &= \frac{1}{g_m}, \qquad \text{if } Z_L \longrightarrow \infty \\ Z_{in} &= \frac{1}{j\omega C_\mu}, \qquad \text{if } Z_L \longrightarrow 0 \end{aligned} \tag{2.41}$$

Nevertheless, considering the output termination as a short or an open circuit is not so realistic. In fact, there is always some parasitic inductance connected to the output of the device. For this reason, a more realistic condition is to consider $Z_L = j\omega L$, obtaining:

$$Z_{in} = \frac{j\left(\omega L - \frac{1}{\omega C_\mu}\right)}{1 + j g_m \omega L} \tag{2.42}$$

and making the very likely assumption that $\frac{1}{\omega C_\mu} \gg \omega L$, we obtain:

$$Z_{in} = \frac{1}{(1 + g_m \omega L)^2} \cdot \left(\frac{1}{j\omega C_\mu} - \frac{g_m L}{C_\mu}\right) \tag{2.43}$$

which shows a global negative resistance component at the input and this means probable oscillation. It can be further noticed that the reciprocal situation can be applied, where the input is decoupled through a series load Z_L. Somewhat remarkably, we obtain the same expression for the output impedance Z_{out}:

$$Z_{out} = \frac{Z_L + \frac{1}{j\omega C_\mu}}{1 + g_m Z_L} \tag{2.44}$$

Furthermore, there is no doubt that also *feedback* can cause instability. Feedback may have been include by the engineer in the original design scheme or it may be completely unintentional. Oscillator designers use positive feedback deliberately, but an unwary amplifier designer may achieve it and find that his amplifier is actually an oscillator, due possibly to such feedback effects as poor grounding.

Let's now focus on finding out if a generic active two-port may oscillate with an arbitrary set of source and load termination (Figure 2.10). We will assume that the concerned terminations have positive real parts, *i.e.* the reflection coefficients whose magnitudes exceed one [6].

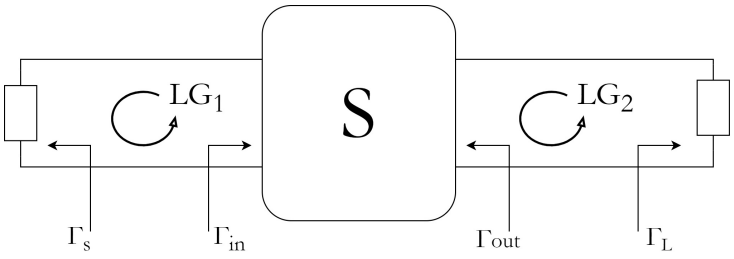


Figure 2.10: Generic active two-port characterized by its S-matrix with input and output terminations.

An active two-port may oscillate if either of the loop-gain products $LG_1 = |\Gamma_S \Gamma_{in}|$ or $LG_2 = |\Gamma_{out} \Gamma_L|$ exceeds unity. If the source and load terminations $|\Gamma_S|$ and $|\Gamma_L|$ are passive, then $|\Gamma_{in}|$ or $|\Gamma_{out}|$ must be greater than unity to satisfy the minimum loop-gain requirement. The key point is that the main purpose of stability design is to achieve *unconditional stability*, *i.e.* the two-port device has to be stable for any value of passive source and load impedance, and more importantly, at all ω.

2.4.2 Rollet Criterion

A measure of stability is a crucial requirement in RF PAs design and so a valid check tool is necessary in order to operate safely during different design steps. The *Rollett Criterion* [7] is a useful, widely established criterion that tells us whether a linear two-port, which was intrinsically stable, will exhibit at its ports negative resistance for any value of passive source or load impedances.

Recalling the section 2.4.1, a linear two-port is unconditionally stable if, with arbitrary passive terminations, its characteristic frequencies remain in the left half of the complex plane. An equivalent statement is that the real part of the immitance looking in at only one of the two ports remains positive with arbitrary passive terminations at the other, provided also that the characteristic frequencies of the two-port with ideal terminations (*infinite immitances, i.e. open or short circuits, as appropriate*) lie in the left-half plane [6]. Always referring to figure 2.10, it means mathematically that:

$$\begin{aligned} |\Gamma_S \Gamma_{in}| &< 1 \\ |\Gamma_L \Gamma_{out}| &< 1 \end{aligned} \tag{2.45}$$

for all $|\Gamma_S| \leq 1$ and $|\Gamma_L| \leq 1$. The equation 2.45 implies that:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_S} \right| < 1$$

The above is guaranteed when the *stability (K)-factor* is greater than unity:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.46}$$

and the determinant of the S-matrix has a magnitude less than one:

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1 \tag{2.47}$$

If the two-port satisfies both requirements, it is defined to be *unconditionally stable*. Otherwise it is called *potentially unstable*. It can be noticed that the above equations must remain valid for all the frequencies. In fact,

a common mistake is to examine only the pass band of the system, unfortunately not always sufficient. Out-of-band instability may show up in unwanted oscillation if they are neglected, particularly at low frequencies.

Witnessed that K-factor is a useful stability check tools, it will be valuable to notice that there are few limitations in its applications. To begin with, K-factor is not a full stability test, since it does not conclude on the actual start up condition of the oscillation because it does not analyze the condition on the imaginary part. If for example $K < 1$ for a certain frequency range, it does not necessary mean that the system will surely oscillate, but it might be. In addition, one may notice that the analysis is performed for small-signal operations, and hence the Rollett Criterion might not be directly applicable to circuits operating in the large signal regime. However, K-factor is a full-fledged well starting point for stability analysis. A further pole-zero identification can fill out perfectly the whole stability check. In conclusion, K-factor might not be appropriate to predict internal instabilities which are not observable at external ports like in multistage amplifiers.

2.4.3 Stability Circles

Sometimes may happen that it is not possible to achieve unconditional stability for certain frequencies. For this reason, the *stability circles* aid to visualize and fix the issue in the Smith Chart. A visual illustration of RF stability circles is reported in Figure 2.11.

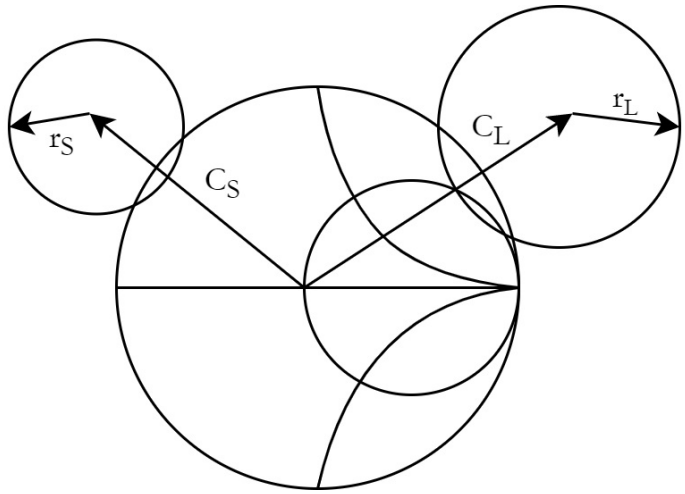


Figure 2.11: Single frequency source and load stability circles of a typical RF transistor, indicating potential instability.

Stability circles are computed from the frequency dependents small-signal S-parameters of the device. As a consequence, stability circles also change with frequency. Interpretation of the stability circles would be quite straightforward if they would consistently indicate the stable and unstable regions, but it is necessary to determine which is the stable side. Before that, the equations to calculate the source stability circles are reported in the following:

$$\begin{aligned} C_S &= \frac{S_{11} - \Delta S_{22}^*}{|S_{11}|^2 - |\Delta|^2} \\ r_S &= \left| \frac{S_{12} S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \end{aligned} \tag{2.48}$$

where C_S is the center of the circle and r_S represents the radius. Similarly, for the load stability circles:

$$\begin{aligned} C_L &= \frac{S_{22} - \Delta S_{11}^*}{|S_{22}|^2 - |\Delta|^2} \\ r_L &= \left| \frac{S_{12} S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \end{aligned} \tag{2.49}$$

Let's now focus on determining the stable side of a source stability circle. The following reasoning can be applied in a similar fashion for the load stability ones.

As noted, the circumference of a source stability circle represents the locus of all source terminations that leads to the borderline case between stable and potential unstable output, *i.e.* $|\Gamma_{out}| = 1$. We need to find at least one other source termination that is not on the circumference and investigate whether it causes $|\Gamma_{out}|$ to be less than unity (stable), or greater than unity (potentially unstable), and an obvious choice is 50 Ω. Then, we want to know the magnitude of the Γ_{out} when the source is equal to 50 Ω. Taking the S_{22} of the device, the following condition can be highlighted [6]:

- if $|S_{22}| < 1$ then the 50Ω source is classified as a termination leading to *stable* output;
- if $|S_{22}| > 1$ then the 50Ω source is classifies as a termination leading to *potentially unstable* output.

In Figure 2.12, four different cases of source stability circles are reported. In case (a) $|S_{22}| < 1$, and the source stability circle does not enclose the

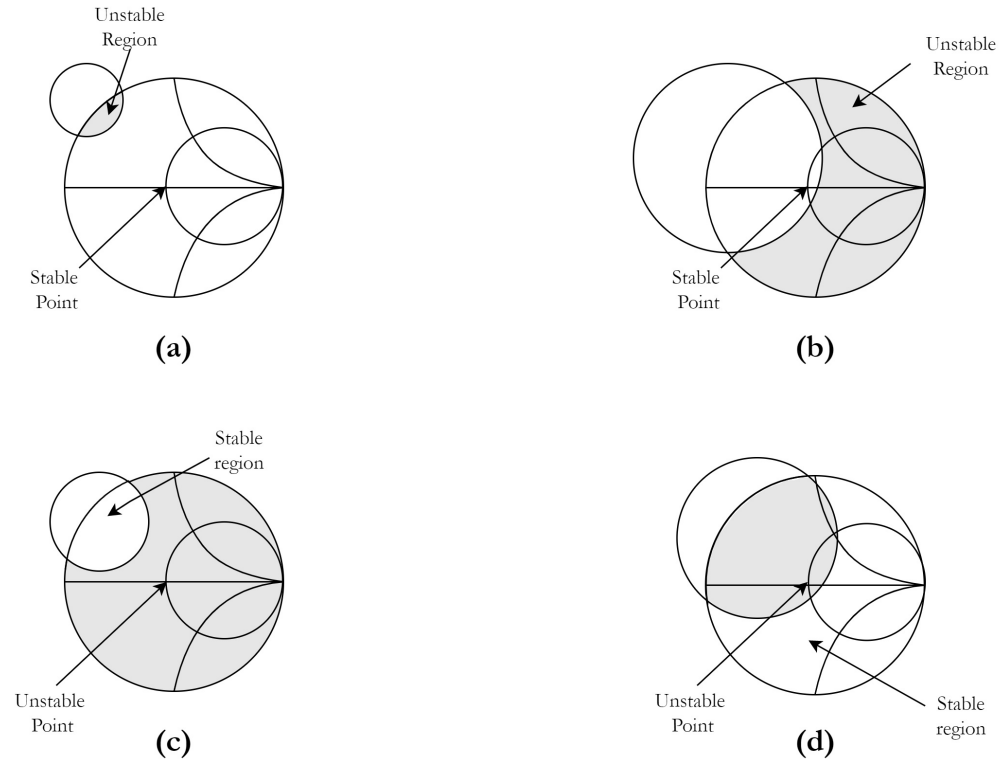


Figure 2.12: Illustration of four different cases of source stability circles with $|S_{22}| < 1$ (2.12(a) and 2.12(b)) and $|S_{22}| > 1$ (2.12(c) and 2.12(d)).

center of the Smith Chart (*stable point*), so the outside region is stable and the inside one, in gray, is unstable. On the other hand, in case (b), $|S_{22}|$ is always less than one but the source stability circle encloses the center of the Smith Chart, so, in conclusion, inside region is stable and outside region, in gray, is unstable. The opposite situations in which $|S_{22}| > 1$ are reported in the cases (c) and (d), and the same reasoning can be applied.

2.4.4 Stabilizing an active two-port

Once the potentially unstable regions are identified for a specific frequency, a simple and effective stabilization technique can be used. This approach involves the use of an appropriate cascode resistor, as reported in Figure 2.13. However, adding a dissipative element throws away transducer gain and also sacrifices output power performance, so an efficient and valuable trade-off between stability and RF PAs performances has to be considered.

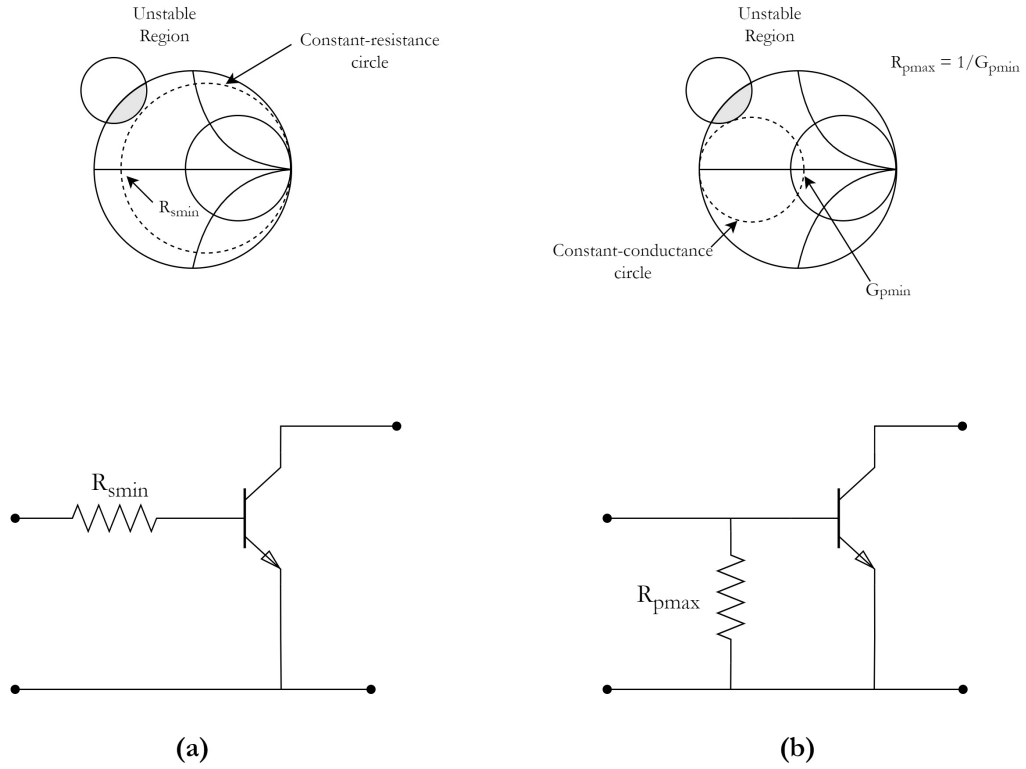


Figure 2.13: Illustration of stabilization techniques using the source stability circles.[6]

To find out the exact value of the resistor, it is possible to proceed in two ways. For the series resistor (2.13(a)), the constant resistance circle tangent to the stability one is traced within the impedance Smith Chart, and it indicates the minimum value R_{smin} required to stabilize the device. On the other hand, in the admittance chart (2.13(b)), the same procedure is applied but this time the tangent constant reactance circle represents the minimum value G_{pmin} and so the maximum shunt resistance $R_{pmax} = \frac{1}{G_{pmin}}$. Once again, increasing R_{smin} or R_{pmax} lead to greater stability margin, at the price of more loss.

In the above illustration, stabilization is performed at the input of the device, and depending on the signal and noise level of the amplifier, it may be better to stabilize at the output. Sometimes splitting the loss between the input and output leads to the best system performance. Adding the appropriate amount of minimum loss to the input or output stabilizes both sides of the device [6].

2.5 Technology and Modeling

In this section, the employed technology will be presented, focusing on the SiGe HBT structure and the equivalent model used for the different BJT types.

2.5.1 Infineon Technology Overview

The involved Infineon's technology is a 130 nm SiGe BiCMOS process with copper metallization for analog mixed signal mm-Wave applications. This technology is based on the previous generations of Infineon's SiGe high-speed bipolar technology and it can provide high performances at lower consumption.

It has been widely believed that SiGe BiCMOS is one of the most attractive technology since it offers worthy trade-off between RF performances and technology costs. BiCMOS technology incorporates the main benefits regarding the SiGe and CMOS technologies, becoming ideally suitable for producing RF systems on a single chip because of:

- High amplification in the RF/mm-Wave front-end;
- More than 10 dBm of output power in the mm-Wave frequencies and before;
- Good-frequency behavior for high-frequency passive devices;
- Better noise performances;
- Technology reliability in terms of process and temperature.

2.5.2 SiGe HBT: Medium and High Speed npn transistors

SiGe Hetero-Junction Bipolar Transistor (HBT) is an improved BJT version which can handle signals over a high-frequencies range. The term "Hetero" refers to the fact that the BE junction is made of a different materials with respect to BC one. In particular, the p+ SiGe base layer is grown after oxide isolation formation and it is followed in the same growth step by the growth of a p-type Si cap [8].

The primary consequence is to limit the injection of holes from the base contact into the emitter region since the potential barrier into the valence band is higher than the conduction band. Unlike BJT technology, this lead

to a high doping concentration in the base and so its resistance is reduced and the gain maintained. A simple schematic cross-section of a generic npn SiGe HBT is reported in figure 2.14.

While superior RF performance has been demonstrated, through vertical and lateral scaling, on low power, high-speed SiGe HBTs [9] [10], the heterostructure design of SiGe HBTs for high power amplification, including region thickness, doping profile and Ge profile, differs from that for low-power and high-speed amplifications. Most SiGe HBTs integrated in SiGe BiCMOS adopt the typical doping profile of silicon BJT with a trapezoidal Ge profile, *i.e.* the high-to-low doping concentration declines from emitter to base and then to collector region. However, there was also presented SiGe HBTs with a different doping profile like a much higher doping concentration in the base region than in the emitter one in order to minimize the base resistance [11].

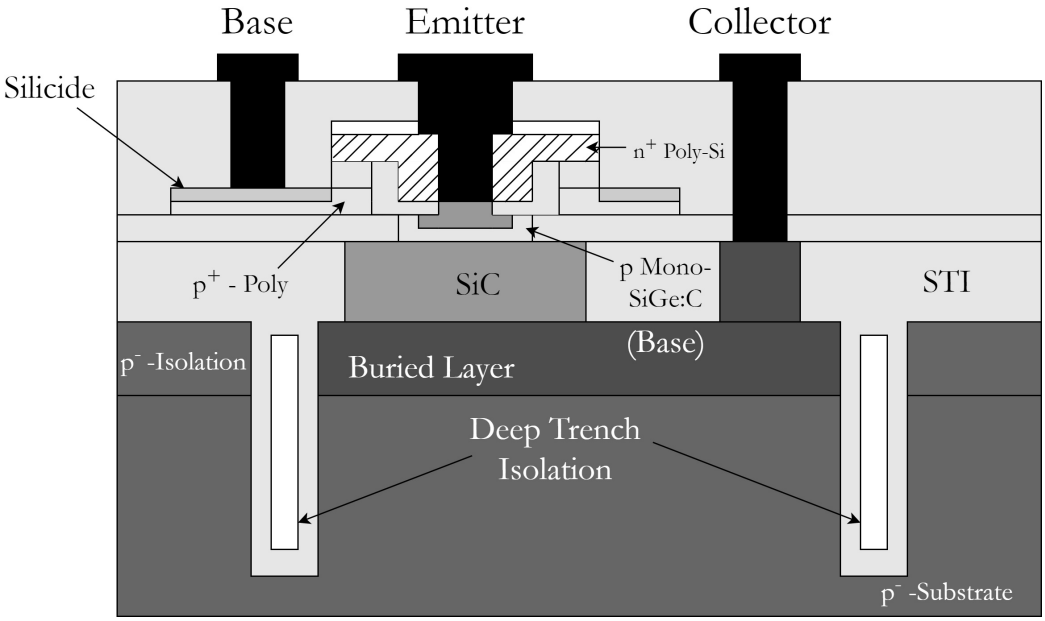


Figure 2.14: Schematic cross-section of an integrated npn SiGe bipolar transistor using poly-silicon contacts and a self-aligned emitter-base-complex [12].

Two kind of npn SiGe bipolar devices have been used for this work. The high-speed (HS) npn transistor and the medium-speed (MS) one. The configuration adopted is the same for both the devices, *i.e.* the CBEBEBC.

2.5.3 Transistor Modeling

A really accurate representation of the transistor equivalent model is critically relevant to design properly. The CAD environments have to provide valid models in order to be able to estimate parasitic effects with a certain high accuracy. This requirement is especially needed in RF design, where high-order effects tend to dominate. Hence a continuous research for ever-more accurate models is necessary to improve the design methodology. The mainly used models for bipolar transistors are Gummel-Poon and the HICUM. They will be briefly described here:

- Gummel-Poon, this model is widely used by the majority of circuit simulators to represent the behavior of bipolar transistors. It was presented for the first time in its complete version in [13] and it is based on the schematic reported in figure 2.15. Every coefficient of the model is found using a data fitting procedure based on different measurement setups and, for this reason, the Gummel-Poon is a model lack of physical background, *i.e.* the model cannot predict properly the behavior of the device in different setup conditions, such as in high-speed/high-frequency and high-collector current densities;

- HICUM, this model was born with the aim to fill the gaps of the Gummel-Poon one by deriving its behavior from physical modeling of the transistor. The HICUM model takes into account also the technology parameters and geometries of the bipolar device, becoming so a preferable choice in order to get more accuracy. In addition, it can model also the breakdown and high current effects, which are pretty relevant for PAs design.

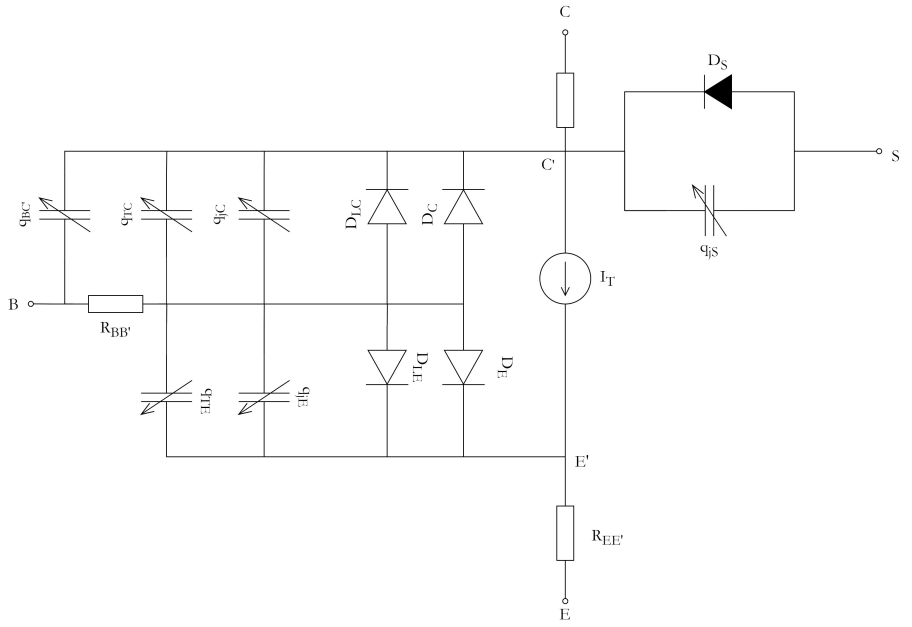


Figure 2.15: Schematic of the equivalent model Gummel-Poon.

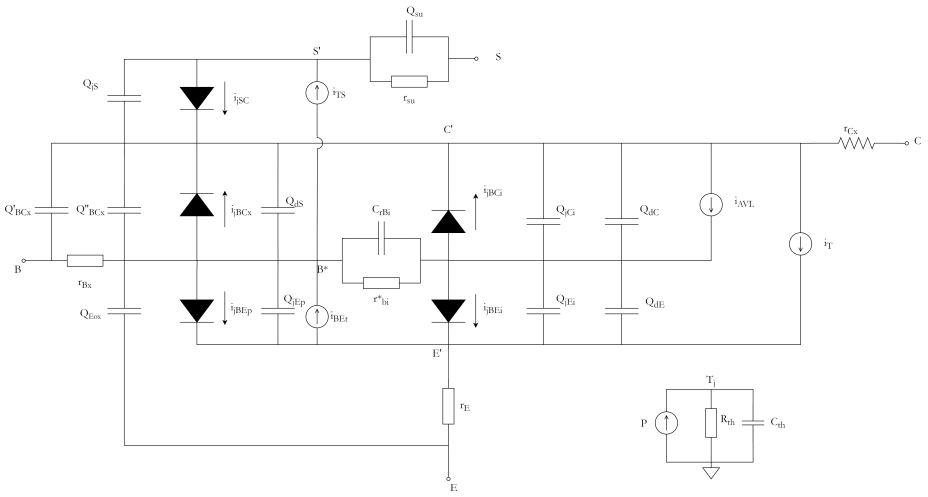


Figure 2.16: Schematic of the equivalent model HICUM.

2.6 Power Gain in CE and CB Configurations

It can be valuable to deepen in the amplification process of the CE and CB stages, since the concerned cascode amplifier has been designed in this configuration. The proposed analysis recalls the one reported in [11] [14] and it has the aim to show the main difference between CE and CB stages at

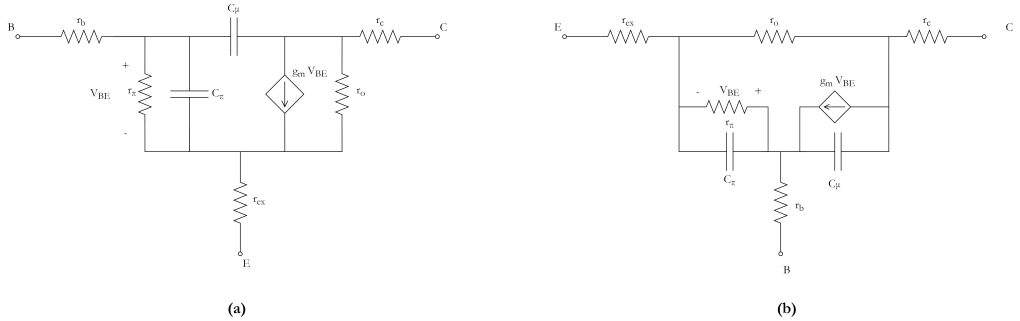


Figure 2.17: (a) Small-signal hybrid-π model for CE SiGe HBTs. (b) Small-signal T model for CB SiGE HBTs. [11]

small signals, with a special consideration regarding power gain.

The small-signal hybrid-π model equivalent circuit of SiGe HBTs, for CE configuration, and the small-signal T-model equivalent circuit for the CB configuration are shown in Fig. 2.17. The parasitic emitter resistance (r_{ex}) and the collector resistance (r_c) are included in these two equivalent circuits for the fullness of the analysis since they were usually ignored in the equivalent circuits of Si BJT due to their negligible values in comparison to total base resistance (r_b). Also r_{ex} and r_c have been included in the equivalent circuit.

The H-parameters of the two-port network representing the CE configuration are derived as follow:

$$\begin{aligned}
h_{11,ce} &= r_b + \frac{\left(\frac{1}{j\omega C_\mu} + r_c\right)\left[Z_1 + r_{ex}(1+g_m Z_1)\right]}{\frac{1}{j\omega C_\mu} + Z_1 + (r_{ex}+r_c)(1+g_m Z_1)} \\
h_{12,ce} &= \frac{r_{ex}(1+g_m Z_1) + Z_1}{\frac{1}{j\omega C_\mu} + Z_1 + (r_{ex}+r_c)(1+g_m Z_1)} \\
h_{21,ce} &= \frac{\frac{g_m Z_1}{j\omega C_\mu} - Z_1 - r_{ex}(1+g_m Z_1)}{\frac{1}{j\omega C_\mu} + Z_1 + (r_{ex}+r_c)(1+g_m Z_1)} \\
h_{22,ce} &= \frac{1+g_m Z_1}{\frac{1}{j\omega C_\mu} + Z_1 + (r_{ex}+r_c)(1+g_m Z_1)} + \frac{1}{r_0}
\end{aligned} \tag{2.50}$$

Where Z_1 is given by $Z_1 = r_\pi/(1+j\omega r_\pi C_\pi)$. Similarly, the H-parameters for the CB configuration equivalent circuit can be derived as:

$$
\begin{aligned}
h_{11,cb} &= \frac{r_b(1 - g_m Z_2 + j\omega r_c C_\mu)}{1 + j\omega C_\mu (r_b + r_c)} \\
h_{12,cb} &= \frac{r_b \left(\frac{1 - g_m Z_2}{Z_2 + r_0} + j\omega C_\mu \right) + \frac{Z_2}{Z_2 + r_0}}{1 + \left(\frac{1 - g_m Z_2}{Z_2 + r_0} + j\omega C_\mu \right) (r_b + r_c)} \\
h_{21,cb} &= -\frac{g_m Z_2 + j\omega r_b C_\mu}{1 + j\omega C_\mu (r_b + r_c)} \\
h_{22,cb} &= \frac{1}{r_b + r_c + \frac{1}{j\omega C_\mu + \frac{1 - g_m Z_2}{Z_2 + r_0}}}
\end{aligned}
\tag{2.51}
$$

where Z_2 is given by $Z_2 = r_e/(1 + j\omega r_e C_\pi)$ and $r_e = 1/(g_m + (1/r_\pi)) = \beta/(g_m(1 + \beta)) = \alpha/g_m$. Once the H-parameters have been derived for the two different configurations, we can consider the maximum stable power gain (MSG) in the intermediate frequency range, since most of SiGe HBTs operate in the frequency range within the f_{max} and the devices are potentially unstable there. MSG can be expressed in terms of H-parameters as following:

$$
MSG = \left| \frac{h_{21}}{h_{12}} \right| \tag{2.52}
$$

At this point, we can know substitute $h_{21,ce}$, $h_{12,ce}$ and $h_{21,cb}$, $h_{12,cb}$ in Eq. 2.51 in order to turn out the MSG for the CE and CB configuration. After performing the assumptions and the simplifications reported in [11], we can compute the MSG_e and MSG_b in the following fashion:

$$
\begin{aligned}
MSG_e &\approx \frac{1}{\omega C_\mu (r_{ex} + r_e)} \\
MSG_b &\approx \frac{\alpha}{\omega r_b C_\mu}
\end{aligned}
\tag{2.53}
$$

It can be noticed that MSG_e is dependent on $r_{ex} + r_e$ and MSG_b is dependent on r_b. For the CB configuration, MSG_b increases as r_b decreases. Similarly, for the CE configuration, MSG_e is inversely proportional to $r_{ex} + r_e$. One can also notice that neither MSG_e nor MSG_b is dependent on the parasitic collector resistance r_c. Although increased r_c can increase the RC delay $C_{bc} \cdot r_c$ of SiGe HBTs, which in turn reduces the device cut-off frequency f_T, there is no significant effect of r_c on small-signal power gain within the frequency range of concern. Finally, the maximum available power gain (MAG) can be expressed as:

$$MAG = \frac{|h_{21}|^2}{4Re(h_{11})Re(h_{22}) - 2Re(h_{21}h_{12})} \tag{2.54}$$

The proposed analysis will be useful in the next chapter for understanding the role between RF and bias circuitry. See the [11] [14] for further insight concerning the different power handling between CE and CB stages.

Chapter 3

UWB Single-Ended Class AB Pre-Driver

This chapter will describe the involved circuit topology, starting from the target specifications through out to the design of the main building blocks and the most challenging steps of the project.

3.1 Target Specifications

One of the principal requirement for this work is the single-ended input/output interface. As seen before, the main aim is to design a UWB single-ended Class AB Pre-Driver amplifier, which will be the output stage of an overall cascaded amplifier.

Parameter	Min	Typ	Max
P_{dc} $[mW]$	–	500	–
Frequency $[GHz]$	1.8	–	5
RL_{in} $[dB]$	–	15	–
RL_{out} $[dB]$	–	12	–
$Gain$ $[dB]$	–	18	–
$OP1dB$ $[dBm]$	–	26	–
$OIP3$ $[dBm]$	–	33	–
NF $[dB]$	–	5	–

Table 3.1: Table containing the project target specifications.

Another relevant aspect is undoubtedly the bandwidth. As the term suggests, the circuit needs to provide competitive performances in a wide band, more precisely in three defined bandwidths: $2.3\ GHz - 2.7\ GHz$, $3.3\ GHz - 4.2\ GHz$ and $4.4\ GHz - 5\ GHz$. In order to extend the possible applications, we decided to expand more the frequency range, since the whole bandwidth is within $1.8\ GHz - 5\ GHz$. The other specifications are summarized in Table 3.1 and they are intended in nominal corner conditions, *i.e.* $V_{DD} = 5\ V$ and $T = 25°\ C$.

3.2 Biasing and Sizing

The configuration adopted for this work is the cascode one since it leads to several advantages, such as increased operation voltage, output power and gain, bandwidth and improved isolation between the input and the output, leading in turn to higher stability.

If we consider the HS-MS cascode branch reported in figure 3.1, it can be noticed that in order to maximize the power delivered to the load, the voltage swing across the branch has to be closer to the supply voltage. However, the *knee voltage* V_k of the transistors gives rise to a decrease of the overall swing and so a more realistic output voltage swing is $(V_{DD} - V_{k,HS} - V_{k,MS})$.

Assuming now a loss of approximately $1.5\ dB$ at the output due to layout and package parasitics, it can be turned out the values of the maximum optimal resistance and the fundamental current which can achieve the OP1dB requirement:

$$\begin{aligned} R_{opt,max} &= \frac{(V_{DD} - V_{k,HS} - V_{k,MS})^2}{2 \cdot (OP1dB + 1.5\ dB)} \approx 16\ \Omega \\ I_{1,max} &= \frac{V_{DD} - V_{k,HS} - V_{k,MS}}{R_{opt,max}} \approx 265.88\ mA \end{aligned} \tag{3.1}$$

Recalling the equations reported in Section 2.3, we can choose a proper conduction angle $\alpha = 197°$ in order to operate in deep-B Class AB region (see figure 3.2). The choice $\alpha = 197°$ comes from an initial estimation of $\alpha = 195°$ which has been changed by tuning the collector current afterwards. This was done in order to obtain the optimum bias point that yields to a certain conduction angle. After that, the maximum peak current and the bias collector current can be derived as follow:

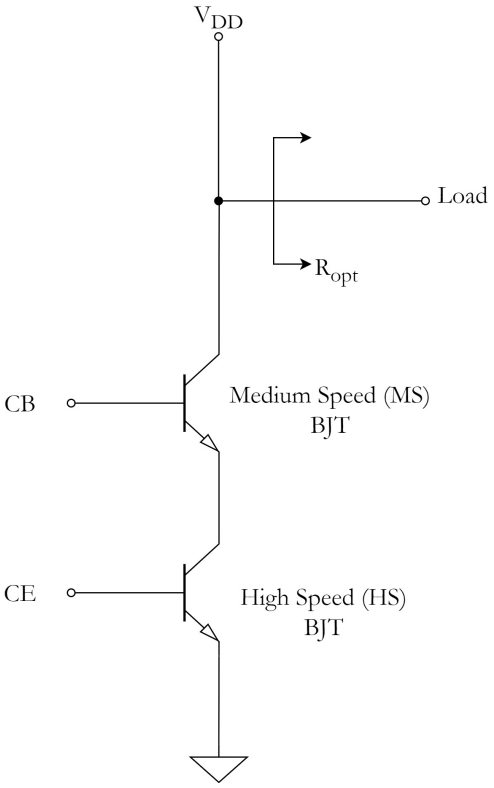


Figure 3.1: Illustration of the amplifier's cascode branch. It combines the benefits of the HS and MS configuration, *i.e.* HS in the CE configurations yields to more bandwidth since it has less parasitics, whilst MS in the CB configuration leads to more voltage swing.

$$\begin{aligned} I_{max} &= 2\pi \cdot I_{1,max} \cdot \frac{1-\cos\left(\frac{\alpha}{2}\right)}{\alpha - \sin\alpha} \approx 514\ mA \\ I_q &= -I_{max} \cdot \frac{\cos\left(\frac{\alpha}{2}\right)}{1-\cos\left(\frac{\alpha}{2}\right)} \approx 66.2\ mA \end{aligned} \tag{3.2}$$

At this point, the effective area of the transistors $A_{eff} = W_{eff} \cdot L_{eff}$ can be computed as follow:

$$\frac{I_{max}}{A_{eff}} = J_C \tag{3.3}$$

where for the sake of design reliability, J_C is the current density defined by technology reliability.

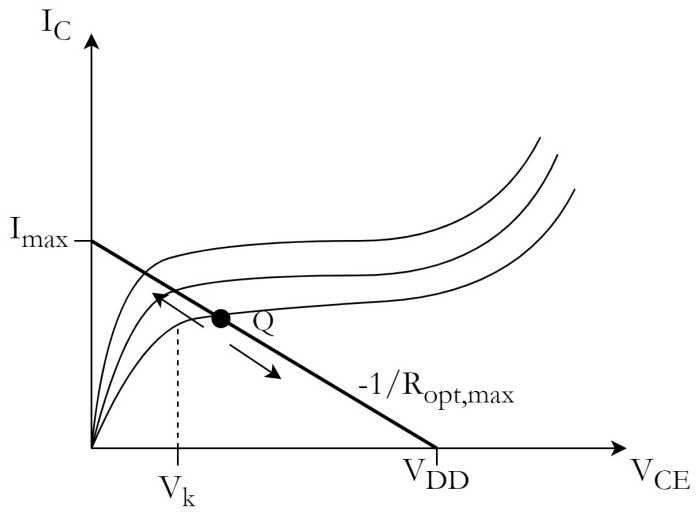


Figure 3.2: Graphical representation of the I-V BJT transcharacteristics with the loadline and the bias point in evidence.

3.3 Ground Connection Impact

Before showing the topology adopted and the main building blocks, it is necessary to briefly introduce a relevant parasitic effect which can severely affect the whole performance of the amplifier. The concerned effect is the ground connection from the emitter contact of the HS npn-BJT and the actual V_{SS} potential, which is ideally a short but in reality it shows an inductive behavior. Hence, it can be represented as a degenerative inductance L_{deg} as shown in figure 3.3, where it can be noticed that the input stage starts to become like an inductive degeneration one.

To better deepen this effect, we can compute the small-signal input impedance of the cascode branch as follow:

$$Z_{in}(\omega) = j\omega L_{deg} + \frac{1}{j\omega(C_\mu + C_\pi)} + \left(\frac{g_m}{C_\mu + C_\pi}\right) \cdot L_{deg} + r_e + r_b \qquad (3.4)$$

where r_e and r_b are the parasitic emitter and base resistor, respectively, C_π is the parasitic base-emitter junction capacitance and C_μ is the Miller capacitance. The primary effect is the emergence of a local reactive feedback at the input due to the inductive degeneration, and this leads to an increase of the input impedance Z_{in} (as shown in Eq. 3.4) and a squeeze of the bandwidth of the CE stage. As a consequence, the small-signal gain $|S_{21}(\omega)|$ starts to roll-off since the higher will be L_{deg}, the higher will be also Z_{in} and the lower will be the voltage gain, which can be briefly shown as follow:

$$\frac{v_{out}}{v_{in}} = \frac{Z_{out}(\omega) i_{out}}{Z_{in}(\omega) i_{in}} = \frac{Z_{out}(\omega) \cdot [\beta(\omega) i_{in}]}{Z_{in}(\omega) i_{in}} = \frac{Z_{out}(\omega)}{Z_{in}(\omega)} \cdot \beta(\omega) \qquad (3.5)$$

where $\beta(\omega)$ is the current gain of the transistor.

For the purpose of this work, we assumed that $L_{deg} \approx 40\ pH$ and built our design on this assumption. It is essential to try to minimize this effect, since it can seriously worsen the overall performances. A further increasing of the inductive degeneration can not only affect the small-signal behavior, but also the large signal one. Moreover, the bandwidth worsening at the input stage is extremely crucial especially in such UWB applications.

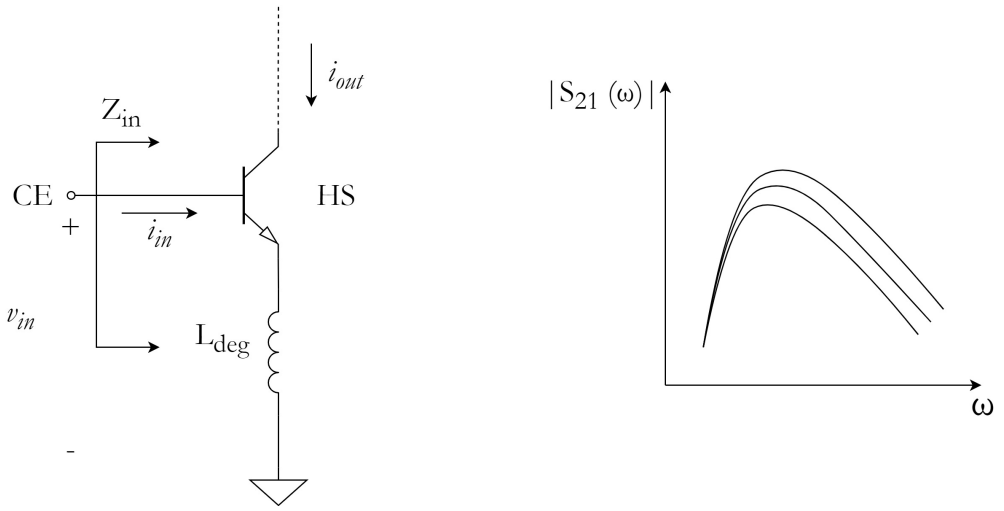


Figure 3.3: Schematic of input cascode branch with inductive degeneration due to ground connection and a visual representation of its impact on the small-signal gain.

3.4 Topology

A schematic representation of the whole Pre-Driver amplifier is reported in figure 3.4. The circuit is divided into four main principal parts:

- Active Core, which is the main block of the RF PA. It is the stage accountable for the amplification of the RF input drive signal and it includes also the stabilization network for improved stability.

- Input Network, which is in charge to provide a well-performed matching between the source impedance and the input impedance of

the active core. Clearly, the input network has to be consist of only reactive element in order to avoid the power dissipation as far as possible.

- Output Network, which is used with the same purpose of the input one, *i.e.* it matches the output impedance of the active core with the load one. It has been designed also to feed DC power to the cascode and to prevent any DC dissipation to the load.
- Bias, which is composed by two high swing cascode current mirrors in order to provide the proper bias to CB and CE base nodes.

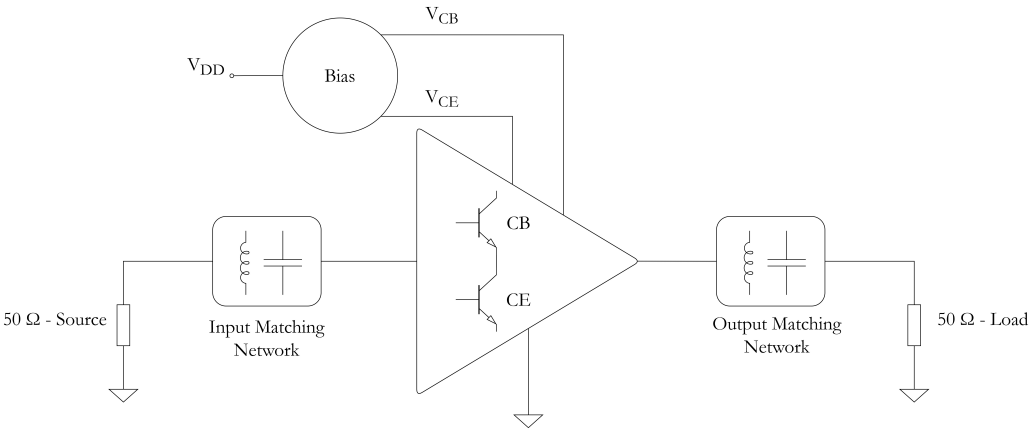


Figure 3.4: Schematic of the main building blocks of Pre-Driver amplifier.

3.4.1 Active Core

As the name suggest, this building block is the core of Pre-Driver amplifier which is the main responsible for the amplification and stabilization. The active core's schematic is reported in figure 3.5.

One of the first thing that probably stands out is the usage of two feedback networks. The first one is composed by the resistance R_{FB}, which has the aim to stabilize the circuit, and the DC block DCB_{FB}, which is needed to prevent that bias current pour out into feedback branch. Only the passive resistance is in charge to improve stability and no other reactive elements, like inductors, have been involved since they can affect the bandwidth. As well known, the smaller will be R_{FB}, the lower will be gain and the higher will be the bandwidth. Hence, the feedback resistance value has to be chosen in order to provide a reasonable gain-bandwidth trade-off.

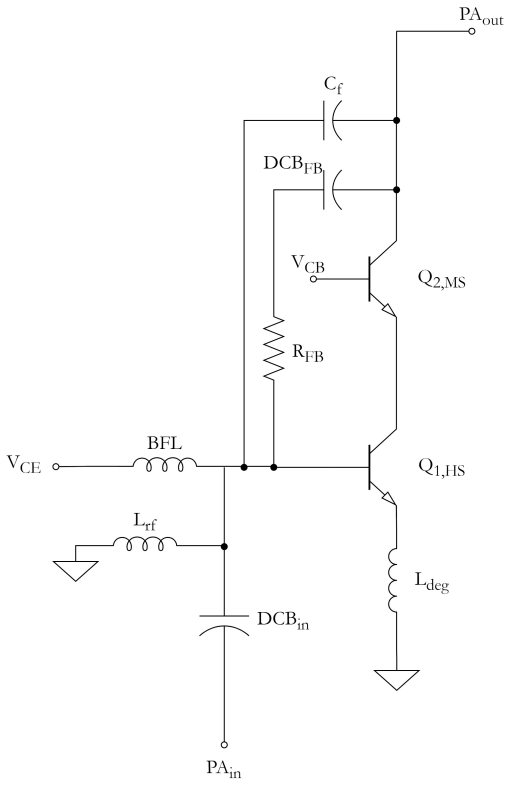


Figure 3.5: Schematic of the Pre-Driver active core.

The second feedback branch is the one composed by the capacitance C_f which it was added to compensate the ground connection effect due to L_{deg}. At first, it can seem counter intuitive since C_f tends to increase the feedback coupling between the input and the output. On the other hand, C_f aids to balance the input and output impedance on the Smith Chart and to compensate the gain roll-off by adding a zero in the *feedforward* path. The value of C_f is small enough to adjust the gain worsening and try to minimize the L_{deg} impact.

Finally, the inductance L_{rf} is adding to resonate input capacitance, whilst the *"big, fat"* inductance BFL decouples the RF signal from the CE bias circuit.

3.4.2 Output and Input Networks

The output network is composed by LC cascaded matching network in order to match the R_{opt} with the 50 Ω load. Before showing its topology in detail, it is necessary to introduce the broadband impedance transformation technique

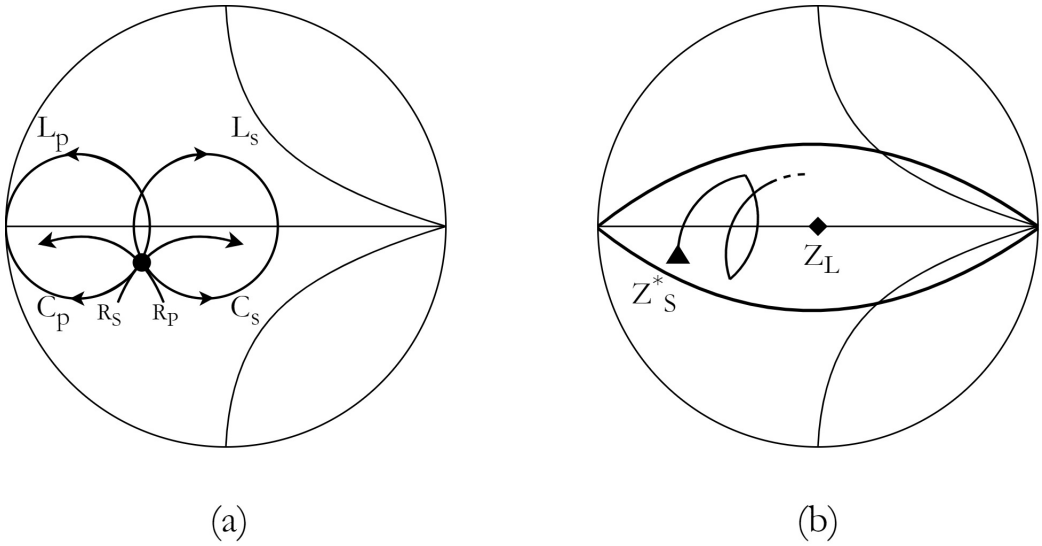


Figure 3.6: Graphical illustrations of Smith Chart tool (a) and broadband impedance transformation with Q curves (b).

with the aim to understand the adopted methodology.

In order to match properly the two concerned impedances, the Smith Chart aids a lot and it gives a graphical representation on impedance transformation. Since we are dealing with UWB applications, it is essential to achieve a well-performed matching without affecting the amplifier bandwidth. Hence, the Q factor has to be considered since it is integral to bandwidth. In fact, it can be expressed as:

$$Q = \frac{f_c}{BW} \tag{3.6}$$

where f_c is the center frequency and BW is the 3 dB bandwidth.

From a generic point in the Impedance Smith Chart, we can move over a constant reactance or resistance circle (see figure 3.6a). By moving up or down, a series inductance or capacitance will be placed, respectively. On the other hand, sliding over the Admittance Chart, a parallel reactive elements will be placed with the same reasoning as the series one.

Witnessed that, consider a general impedance matching problem, in which the source impedance Z_S has to be matched to the 50 Ω load Z_L. On the Smith Chart, we plot on a single frequency (preferentially the center frequency) the conjugate source impedance Z_S^*, since we want power matching condition, and the load impedance Z_L. Hence, by moving on the Impedance or the Admittance Smith Chart, Z_S^* can reach Z_L and a cascaded LC match-

ing network will be built. Furthermore, since we want to achieve a good matching over a wide frequency range, we should consider the Q curves on the Smith Chart. Plotting Q of the load as constant ratio will define a constant Q curve. These Q curves are used as a guideline boundaries for broadband transformations.

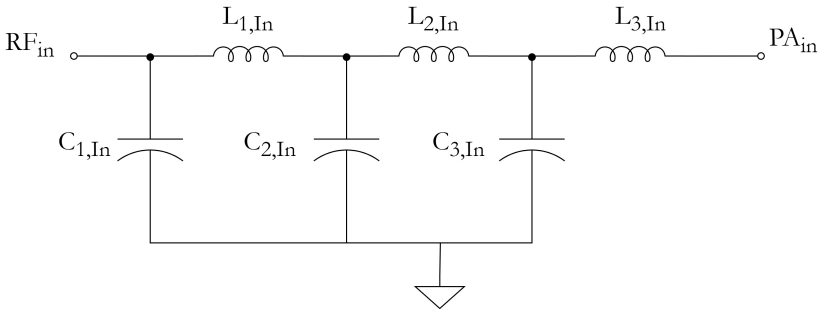


Figure 3.7: Schematic of the input matching network.

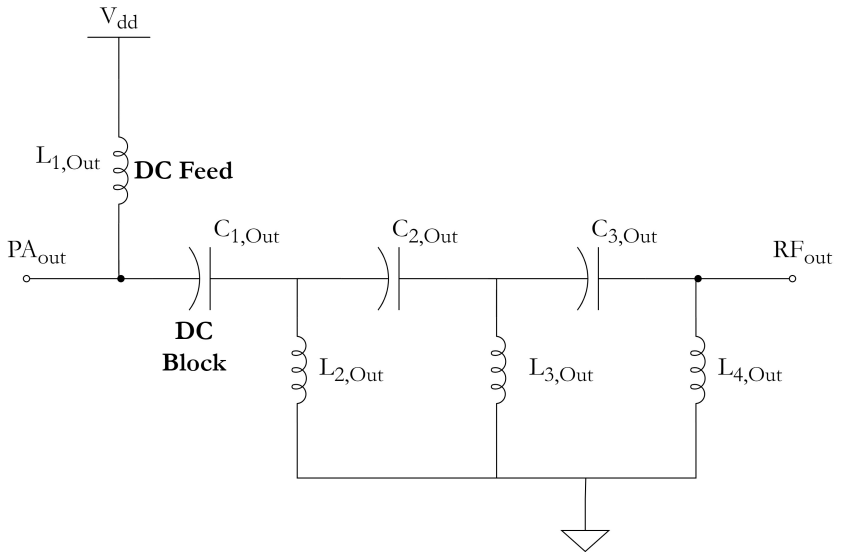


Figure 3.8: Schematic of the output matching network.

As a rule in broadband transformations, maintaining a lower Q curve for a given transformation by increasing the number of n-sections will yield a higher bandwidth. For a single section transformation where the resistive line and a constant Q of the load curve bounds the transformation, the relationship between the Q of the load and the resistive transformation ratio is given by:

$$1 + Q^2 = R_{ratio} \tag{3.7}$$

where R_{ratio} is the ratio between the two resistive impedance to be matched. For increasing bandwidth by increasing the number of n-sections having equal Q, the relationship becomes:

$$1 + Q^2 = (\sqrt[n]{R_{ratio}}) \tag{3.8}$$

Clearly, using a lot of sections in the designed matching network will not lead to several advantages on the bandwidth, since it has to be considered that more sections will lead to more parasitic elements and hence more losses. In practice using more than a four-sections matching network will not yield greater bandwidth [15].

Once the broadband matching design criteria has been introduce, the input and output matching network's topology can be reported in figures 3.7 3.8. It could stand out that the output matching network has been designed in order to also feed DC power to the collector node with the DC feed and to prevent any DC dissipation to the load with the DC block. This two latter ones have been embedded in the output matching network in order to minimize the number of components to be used.

3.4.3 Bias

As already mentioned, the bias circuitry has the aim to provide bias voltages at the CE and CB base nodes. Two high swing cascaded current mirrors have been used in order to provide the required V_{CE} and V_{CB}. The CE base node has been attached to the current mirrors with a diode connected transistors in order to provide a 1/8 mirror ratio. At the CB base node, instead, a bias voltage is applied and its value will affect the output voltage swing behavior. In fact, increasing V_{CB} yields to a further increase of the CB BJT output swing and tends to minimize the CE BJT one. An higher CB voltage will lead to avoid breakdown at the CE transistor and tends to minimize the clipping behavior in the cascode output swing. However, an undue voltage stress on the CB configuration could lead to an excessive output swing increase which turn into breakdown effects. Hence a proper CB bias voltage trade-off has to be consider in order to avoid breakdown effects on both CB and CE configurations.

Finally, the two reference currents $I_{ref,1}$ and $I_{ref,2}$ are provided by a bias core in CMOS technology with digital gates. A simple illustration of the overall bias mechanism is represented in the following figure.

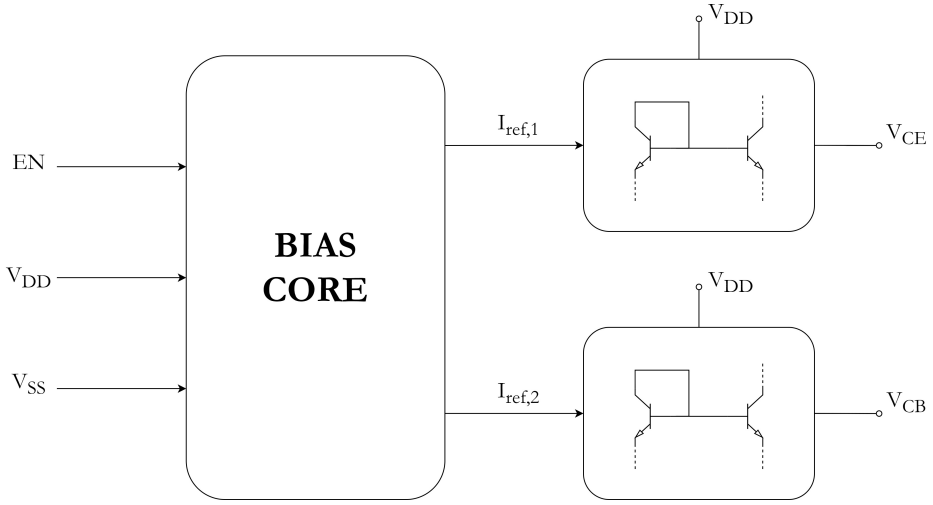


Figure 3.9: Schematic of bias circuitry.

3.5 RF- Bias Interaction

It might be worthwhile to analyze the interaction between the RF signal and the bias circuitry, in particular at the base contact of the CB transistor. In the ideal case, the bias voltage V_{CB} is provided by an ideal voltage source and so a nil impedance will be shown at small-signal. Clearly, the bias impedance is not negligible in practice but it is necessary to provide a low impedance behavior in order to avoid instabilities. Any remarkable load effects will lead to oscillation on the bias voltage and so CB instabilities.

In order to deepen the main consequences of this interaction, let us consider a generic bias impedance Z_{bias} connected at CB base. In other words, if Z_{bias} is too high, the primary effect is to increase the voltage feedback at CB base (C_μ) which turn into an increase of the input impedance with respect to $1/g_m$. This will lead to a generation of an emphasized current divider between $1/g_m$ and all the parasitic capacitance connected to the CB emitter. Hence, a non-dominant pole will be added at high frequencies and if Z_{bias} increased, the pole concerned will slide down to lower frequencies and an overall gain reduction will be shown. Clearly, this will affect also large signal behavior and so the output power.

The concerned bias circuit shown a considerable high impedance at the CB base node, hence we need to find out a proper way in order to minimize its impact. The most intuitive solution will probably be to connect *"big,fat"* capacitance BFC in shunt with the bias impedance. This yields to a decrease of the input impedance at the CB node. The impedance seen from the

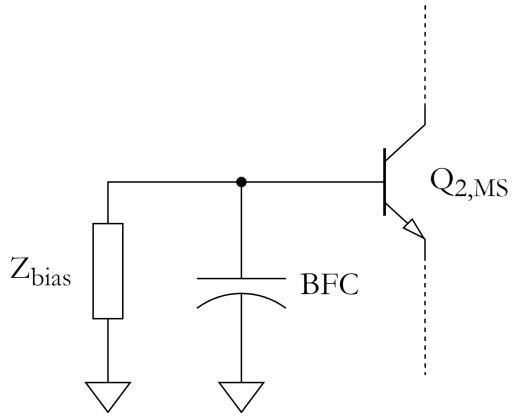


Figure 3.10: Graphical illustration of the adopted solution to reduce the high impedance bias impact.

transistor can be approximated as:

$$Z_{b,CB} = Z_{bias} \;/\!/\; \left(\frac{1}{sC_{BFC}}\right) \tag{3.9}$$

With this simple solution, we can prevent the gain roll-off and the overall reduction of PA performances. Furthermore, as the analysis proposed in Section 2.6, the CB configuration is extremely sensitive to the base resistance and that is also the reason for the gain worsening. Clearly, the BFC has to be big enough in order to neglect the bias impact, and this will lead to a huge area employment in the layout.

Chapter 4

Inductors Design

In this chapter, the design methodology adopted for the coils will be presented. Furthermore, the layout of each single inductance of the cascode amplifier and their relative performances will be shown.

4.1 Mohan's equation

Research attempts in predicting the behavior of inductors have always been made since it is extremely relevant to deepen their physical condition, especially for RF applications. The lack of well performed inductor is by far the most conspicuous shortcoming of standard IC processes due to the fact that there are many electromagnetic effects that have to be considered [2].

The most widely used on-chip inductor is the *planar spiral*, which can assume many shapes. Depending on the technology, the IC designer should be feel free to choose the proper shape without many considerations, as a first step. However, one shape can differ by the others in terms of quality factor and area performances, since the current distribution will be different and so the electromagnetic field. For the purpose of this work, the main choice falls on only two shapes, *i.e.* the square and the octagonal one (Figure 4.1).

When designing a coil, four main parameters might be considered: the *outer diameter* d_{out}, the *inner diameter* d_{in}, the *strip width* w and the *strip spacing* s. In addition, one of the most intuitive parameter that affects the inductance is undoubtedly the *number of turns* n, as the Ampere's law suggests. All of them can be used to turn out the value of the wanted inductance as a first approximation. Furthermore, it can be noticed that in planar device the $\vec{H}$ field is not uniform, hence the value of the inductance L will be proportional to the coil diameter rather than the coil area.

A vast amount of analytical formulas could be found in the literature,

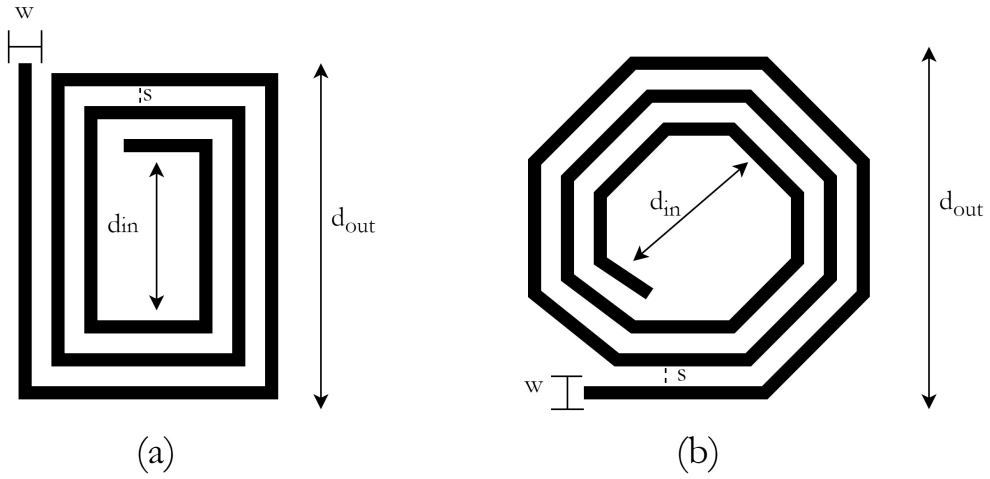


Figure 4.1: Planar spiral inductors square (a) and octagonal (b) shape.

each one with a reasonable accuracy in terms of inductance estimation. The difficulty with behavior prediction expressions is not just to find formulas that give precise results, but to find simple low-entropy expressions (as defined in [16]). A collection of three of these formulas will be briefly presented as follow:

- Modified Wheeler Formula, which comes out from the previous RF designers generations. It is the most widely diffuse formula in coil design. The original Wheeler formula presented in [17] was intended for discrete inductors. Mohan *et al.* in [18] state that minors modifications on the original Wheeler formula can be applied in order to make it suitable for spiral planar coils, obtaining:

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{4.1}$$

  where K_1 and K_2 are geometry dependent parameters (see Table 4.1), d_{avg} is the average diameter between d_{out} and d_{in}, ρ is the *fill factor*, which indicates how hollow the inductor is. It is defined as:

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{4.2}$$

  Clearly, as the term suggests, ρ approaches unity as the inductor windings fill the entire space, and it approaches zero as the inductor becomes progressively hollower.

- Current Sheet Approximation, which has been used in this work for the inductance estimation to give initial perspective. This approximation aims to substitute the coil with a current sheet with equal current density, and summing self inductances, according to the direction of currents. The value of the estimated inductance has the following expression:

$$L_{csa} = \frac{\mu_0 n^2 d_{avg} c_1}{2} \cdot \left(\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2 \right) \tag{4.3}$$

where c_1, c_2, c_3 and c_4 are the geometry dependent coefficient which are reported in table 4.2.

- Monomial Data Fitting, which is an expression based on data fitting presented in [18], *i.e.*:

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \tag{4.4}$$

where w represents the trace width, n the number of windings, s is the windings separation, whilst β and α_i are layout dependent coefficient which are reported in Table 4.3. Considering the logarithm of the expression showed yields:

$$\begin{aligned} y &= \log L_{mon} \\ &= \log\beta + \alpha_1 \log w + \alpha_2 \log d_{avg} + \alpha_3 \log n + \alpha_4 \log s \\ &= \alpha_0 + \alpha_1\chi_1 + \alpha_2\chi_2 + \alpha_3\chi_3 + \alpha_4\chi_4 + \alpha_5\chi_5 \end{aligned} \tag{4.5}$$

where $\alpha_0 = \log\beta$. This is a linear-plus-constant model of y as a function of x, and it is easily fit by various regression or data-fitting techniques. In [18] a least squares fit has been used to minimize the error over $N \approx 19000$ inductors.

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Table 4.1: Table of Modified Wheeler Formula coefficients.

LAYOUT	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 4.2: Table of Current Sheet Approximation coefficients.

LAYOUT	β	α_1	α_2	α_3	α_4	α_5
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-}3$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-}3$	-1.21	-0.163	2.43	1.75	-0.049

Table 4.3: Table of Monomial Data Fitting coefficients.

The resulting absolute errors of the three proposed expressions are reported in figure 4.2. The plots show that the typical errors are in the $1-2\%$ range, and most of the errors are smaller than 3%.

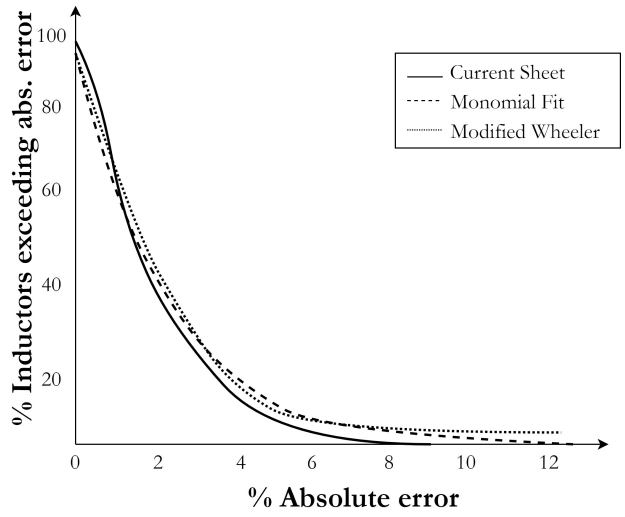


Figure 4.2: Comparison of the absolute error of the three formulas vs Field Solver simulation. The maximum absolute error on the prediction value is around $\epsilon = 10\%$ [18].

4.2 Inductors Equivalent Model

The large area potentially consumed is one of the most relevant issue of spiral inductors, since the hollow part could lead to unnecessary waste of area. However, another serious problem with this kind of inductors is their relatively large loss.

Before deepen in this loss mechanism, it might be valuable to recall the *skin effect*. Basically, the skin effect is where alternating current tends to avoid travel through the center of solid conductor leading into a non uniform current distribution. The AC current conduction will be limited near the surface of the conductor. This effectively limits the cross-sectional conductor area available to carry alternating electron flow, increasing the shown electrical resistance. In RF applications, this effect is exploited since at high frequencies the AC current avoids traveling through most of the conductor's cross-sectional area and it seems like hollow for the purpose of the conducting current. An estimate for the series resistance may be obtained from the following equation:

$$R_S \approx \frac{l}{w \cdot \sigma \cdot \delta(1 - e^{(-t/\sigma)})} \tag{4.6}$$

where σ is the conductivity of the material, l is the total length of the winding, w and t are the width and the thickness of the interconnect, and the skin depth is given by:

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma}} \tag{4.7}$$

In addition to series resistive loss, capacitance to the substrate is another conspicuous problem of on-chip spirals. The proximity to the substrate yields to the emergence of a parallel plate capacitor which resonates with the inductor at the frequency $\omega_{srf} = 1/\sqrt{LC_{par}}$. This resonance frequency sets an upper useful frequency limit of the inductor, since the desired operating frequency ω_0 should be far away from ω_{srf}. If the self-resonance frequency will be so closed to the operating one, the inductor is useless. Moreover, the proximity with the substrate also degrades quality factor of the energy coupled into the lossy substrate.

An additional parasitic element is the shunt capacitance across the inductor that arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn to turn usually has a negligible overall effect because it is the series connection of these capacitances that ultimately appears across the terminals of the inductor [2].

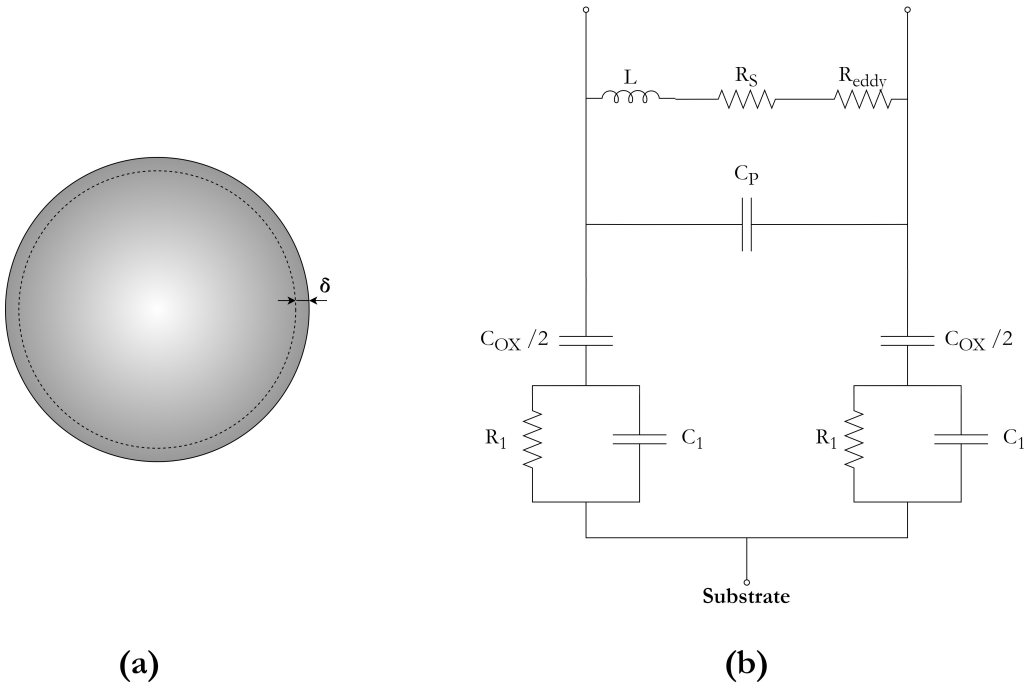


Figure 4.3: Illustration of skin effect with a generic conductor (a) and a simplified model for on-chip spiral inductor (b) [2].

Although an ex-ante precise inductance estimation is quite complicated to achieve, since there are a lot of parasitic effects that have to be considered, a simplified equivalent model for on-chip spiral inductor is reported in figure 4.3. It can be noticed that the total series resistance will be the sum of R_S and the eddy-current resistance R_{eddy}, which can be represented in a resulting crude formula [2]. Meanwhile, the shunt capacitance C_P is:

$$C_P = n \cdot w^2 \cdot \frac{\epsilon_{ox}}{t_{ox}} \tag{4.8}$$

where t_{ox} is the thickness of the oxide between the cross-under and the main spiral. The capacitance between the spiral and the substrate proper is C_{ox} and it is here approximated with a simple parallel plate formula, where the total area is that of the winding:

$$C_{ox} = w \cdot l \cdot \frac{\epsilon_{ox}}{t_{ox}} \tag{4.9}$$

Furthermore, the resistance R_1 and the capacitance C_1 models the substrate dielectric loss and the capacitance of the substrate as well as other reactive

effects related to the image inductance, respectively. They are given by the following equation:

$$R_1 \approx \frac{2}{w \cdot l \cdot G_{sub}} \tag{4.10}$$

$$C_1 \approx \frac{w \cdot l \cdot C_{sub}}{2} \tag{4.11}$$

where G_{sub} and C_{sub} are fitting parameters of the substrate.

With the foregoing set of equations, we are able to estimate the main parasitic elements of our spiral inductors. This can be a conspicuous aid in the first step of the coil design, since we can reach a well-known perspective of what affects our on-chip inductors.

4.3 Output Network Coils

In this section, there will be presented the output matching network coils with their performances in terms of Q factor within the 10 GHz range. Moreover, a comparison between their performances at different temperature corner conditions will be shown.

The output network is the most relevant in terms of power delivery to the load. For this reason, we decided to design its coils with the octagonal shape, since it can achieve good performances in terms of quality factor. However, the improved Q of the network suffers the expense of area, as mentioned in the previous sections.

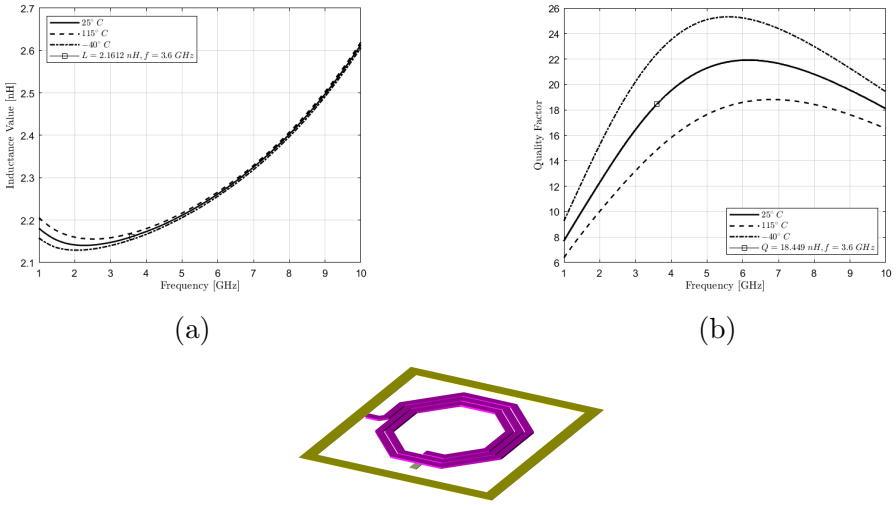
Referring to figure 3.8, the performance of $L_{1,out}$, $L_{2,out}$, $L_{3,out}$ and $L_{4,out}$ are shown in the following list of figures respectively with the evidence of inductance and Q value at the operating frequency f_0. The results of this section and of the next ones are achieved using the EM simulation tool ®Momentum, developed by ©Keysight Technologies. Momentum is 3-D planar electromagnetic simulator used for passive circuit analysis and a partial equation solver of Maxwell's equations based on the method of moments.

Analyzing the results obtained, it can be seen that in nominal corner condition ($T = 25°\ C$) all the coils can achieve a fairly high Q factor at f_0, since the lowest one is $Q = 17.27$ of $L_{4,out}$, which is also the biggest inductance in the output network. Clearly, for high inductance value it might be quite tough to achieve high Q factor. Moreover, as the operating frequency increases, the maximum achievable inductance value will decrease.

One more compelling fact is that Q factor will decrease at higher temperature, like $T = 115°C$. This effect is due to the increase of the series losses

since the metal will shown an higher resistance at high temperature. As a result, it can be also noticed that for $T = -40° \ C$ an high Q factor can be achieved with respect to the other corner conditions.

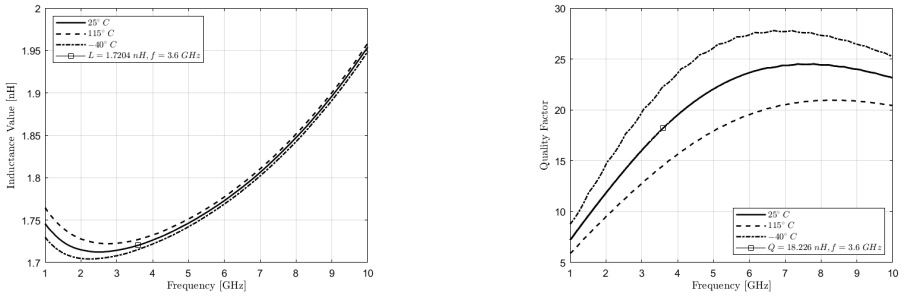
Furthermore, we reported also the inductance 3D view. It can be noticed that each coil is framed by a guard ring in a lower metal level with respect to the coil windings. This is used to minimize mutual inductance coupling with the other coils. The distance between the guard ring and the coil is also important since the guard ring has not to be much closer to the coil because a degradation of its Q factor and enhance EM couplings can occur.



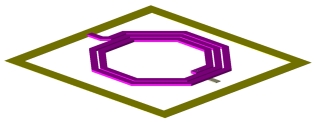
(a) (b)

(c)

Figure 4.4: Performance of $L_{1,out}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).

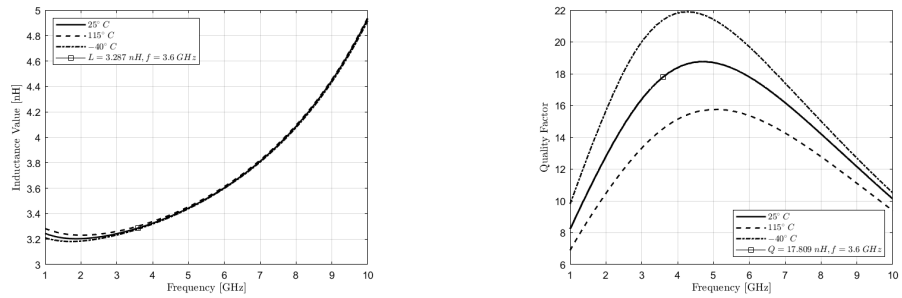


(a) (b)

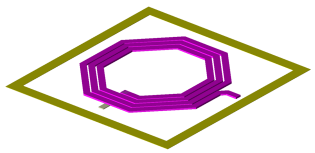


(c)

Figure 4.5: Performance of $L_{2,out}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).

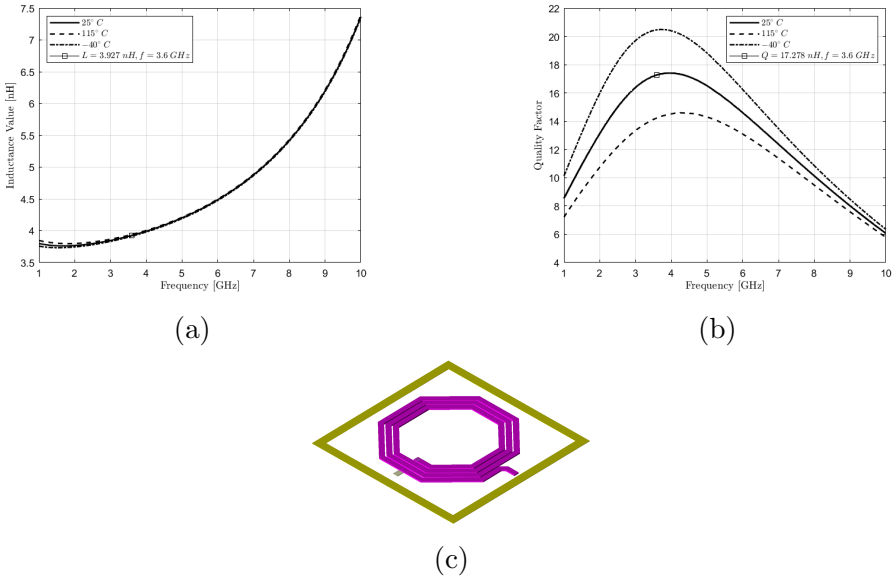


(a) (b)



(c)

Figure 4.6: Performance of $L_{3,out}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).



(a) (b)

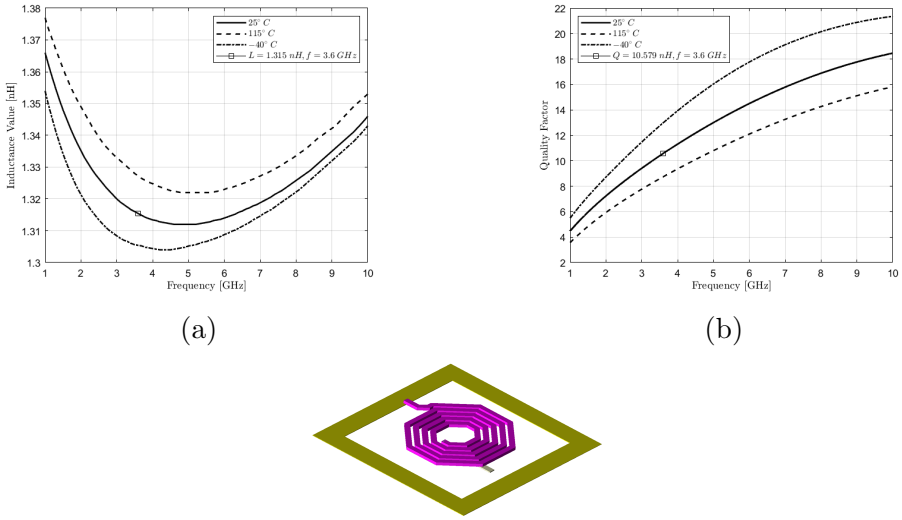
(c)

Figure 4.7: Performance of $L_{4,out}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).

4.4 Input Network Coils

The inductors of the input network have been designed in a similar fashion to the output one. Since the input matching network is not so critical with respect to the output one, we decided to design its coils with octagonal shape, but with less area occupation. This leads to more stretched coils with more turns in order to achieve the desired inductance value.

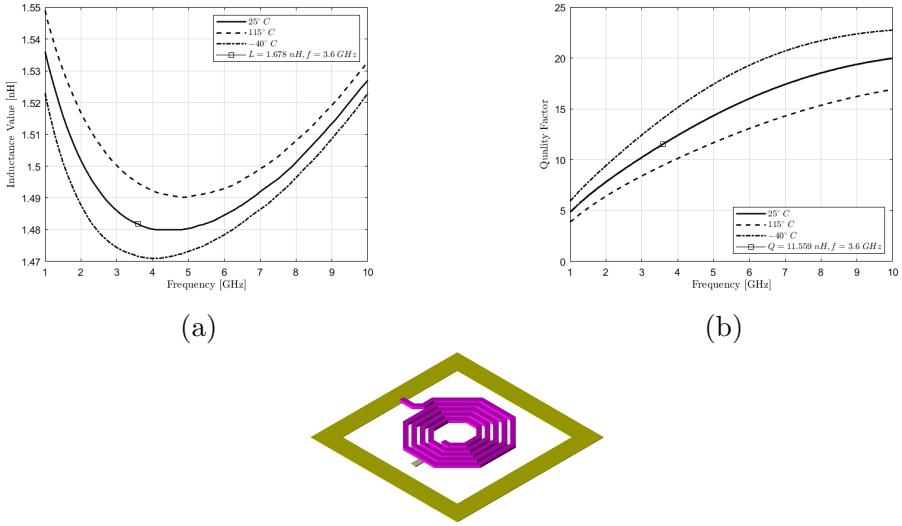
As the previous section, the performances of $L_{1,in}$, $L_{2,in}$ and $L_{3,in}$ are presented in the following list of figures. It can be noticed that the inductance values are fairly similar and the highest Q factor is achieved from $L_{2,in}$ at f_0, *i.e.* $Q = 11.559$. The previous reasoning concerning the variation of the Q factor for different temperature corner condition are still valid for the input network.



(a) (b)

(c)

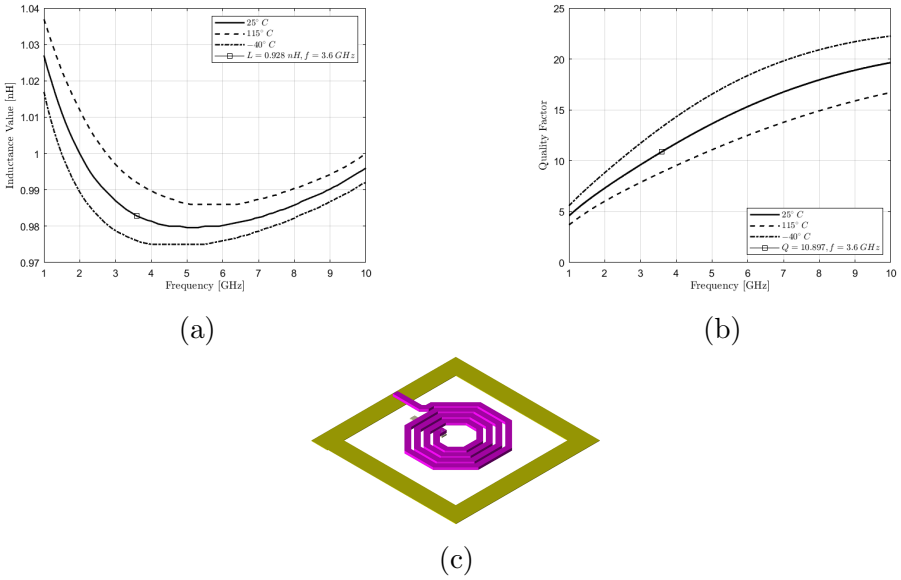
Figure 4.8: Performance of $L_{1,in}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).



(a) (b)

(c)

Figure 4.9: Performance of $L_{2,in}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).



(a) (b)

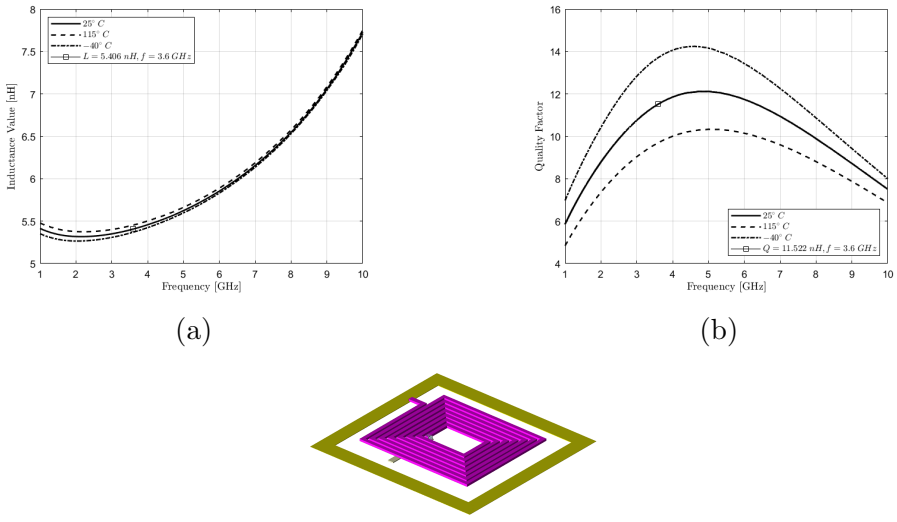
(c)

Figure 4.10: Performance of $L_{3,in}$ within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).

4.5 Active Core Coils

The two coils of the core building block have been designed with two different shapes. For what concerned the *"big,fat"* inductor BFL, we decided to use the square shape, since its inductance value is the largest one within the chip's coils because it has to provide a well-performed decoupling between the CE stage bias and the RF signal. The square shape choice yields undoubtedly to an advantage in terms of area. On the other hand, for the resonant inductor L_{rf}, the octagonal shape has been implemented since its inductance value is not too large and we can achieve better performance for what concerned Q factor.

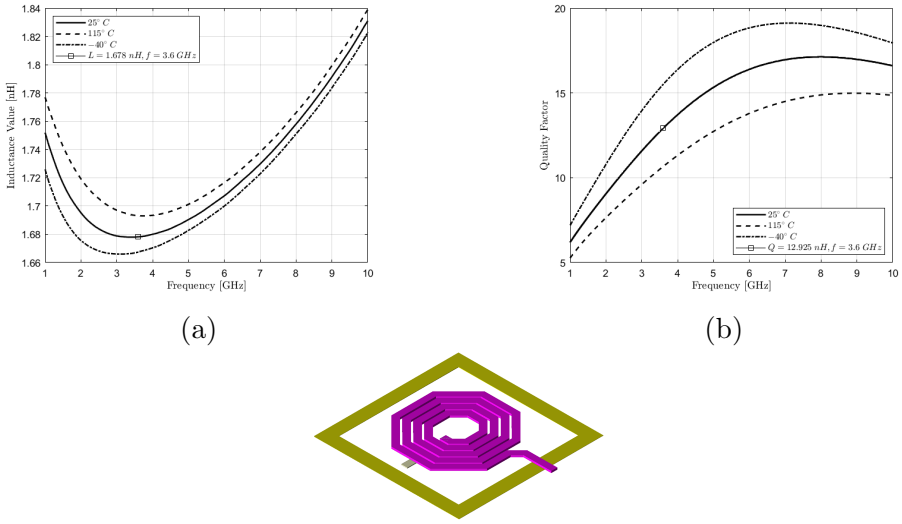
As shown before, the performance of BFL and L_{rf} are presented in the following list of figures, respectively. Once again, the consideration regarding Q factor at different corner conditions are the same reported in Section 4.3.



(a) (b)

(c)

Figure 4.11: Performance of BFL within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).



(a) (b)

(c)

Figure 4.12: Performance of L_{rf} within the 10 GHz range: inductance value (a) and quality factor (b) at different temperature corner condition, and inductance 3D view (c).

Chapter 5

Layout

After the schematic design, the simulation including real components and the coils touchstone, the next step is undoubtedly the layout, since it yields to put things more in perspective with the area occupation and with the impact of the parasitic effects that cannot be seen in the schematic. Basically, the layout step consists in the design of the physical representation of the circuit components according to the requirements imposed by the manufacturing process, such as the minimum distance between metal strips, strip width and so on.

In this chapter the layout of the output and input matching networks, and the active core building block will be presented, with brief comments. Afterwards, the layout of the whole test chip will be shown. All the layout presented has been designed using ©Cadence Virtuoso Layout Suite, which includes two useful tools, Design Rule Check (DRC) and Layout Versus Schematic (LVS). The first one is needed to verify that the layout matches the manufacturing process requirements, whilst the latter is used to check that there is no discrepancies between the schematic and the layout of the circuit concerned.

5.1 Output Matching Network

The output network occupies undoubtedly a relevant space of the whole chip's area, since its coils have been designed to achieved high Q factor and therefore their dimensions are quite huge. Also its MIM capacitors fill a considerable area occupation because they are in the order of pF magnitude.

The layout of the output matching network is shown in figure 5.1. It can be noticed that all the coils are attached together in the same ground plane. The distance between the coils has been minimized in order to prevent any

waste area but at the same time, try to not enhance any mutual inductance effects between the inductors.

The output matching network occupies a total area of $743 \times 782\ \mu m^2$.

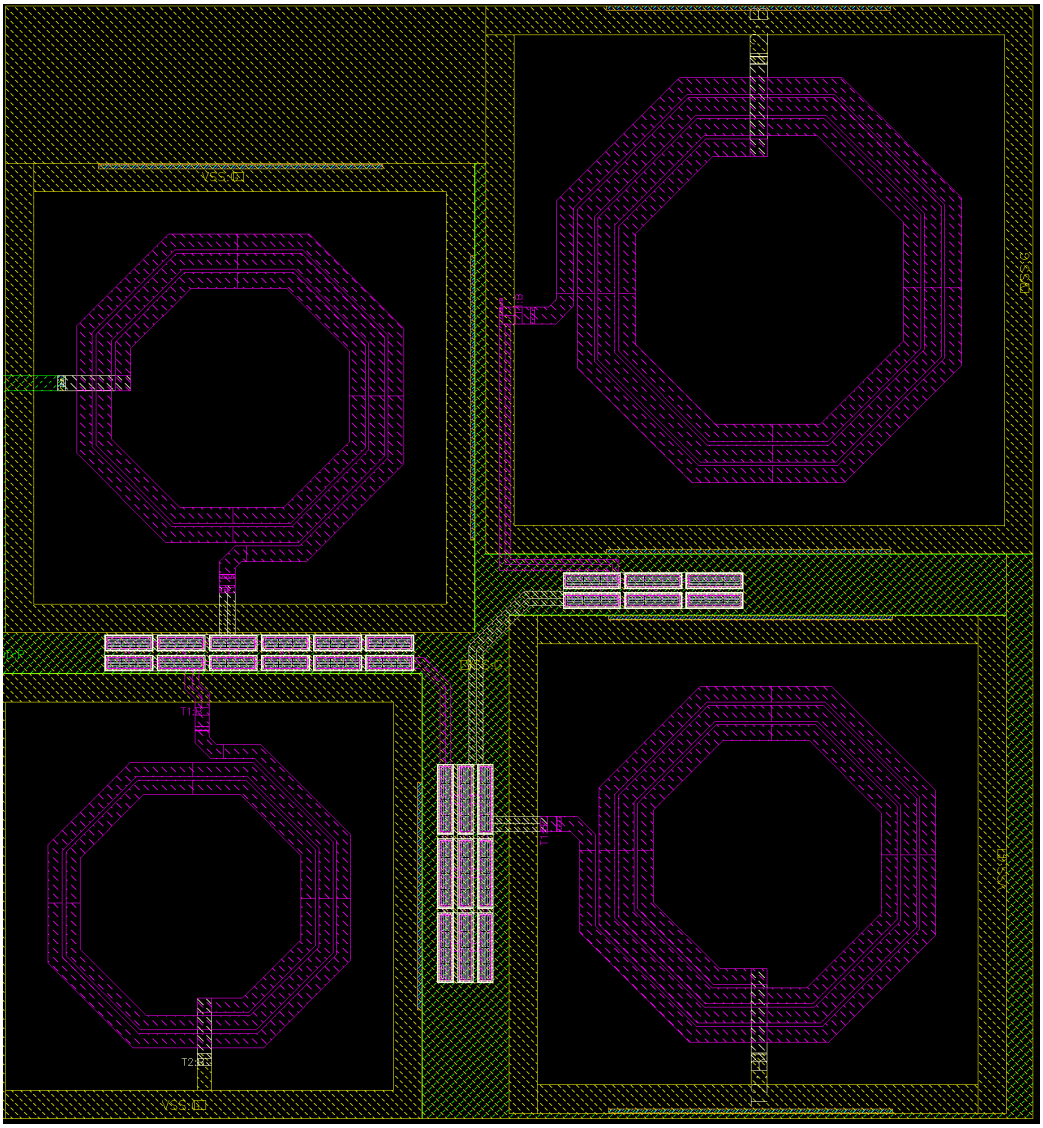


Figure 5.1: Output Matching Network Layout.

5.2 Input Matching Network

Unlike the output network, the input one occupies less area and this is certainly an advantage. Its coils does not need a such higher Q factor as the output ones and so their octagonal shape can be ever stretched. Also its MIM capacitors are not so high in terms of capacitance magnitude, and as a results we obtain the layout reported in figure 5.2. The total area occupied is $450 \times 416\ \mu m^2$.

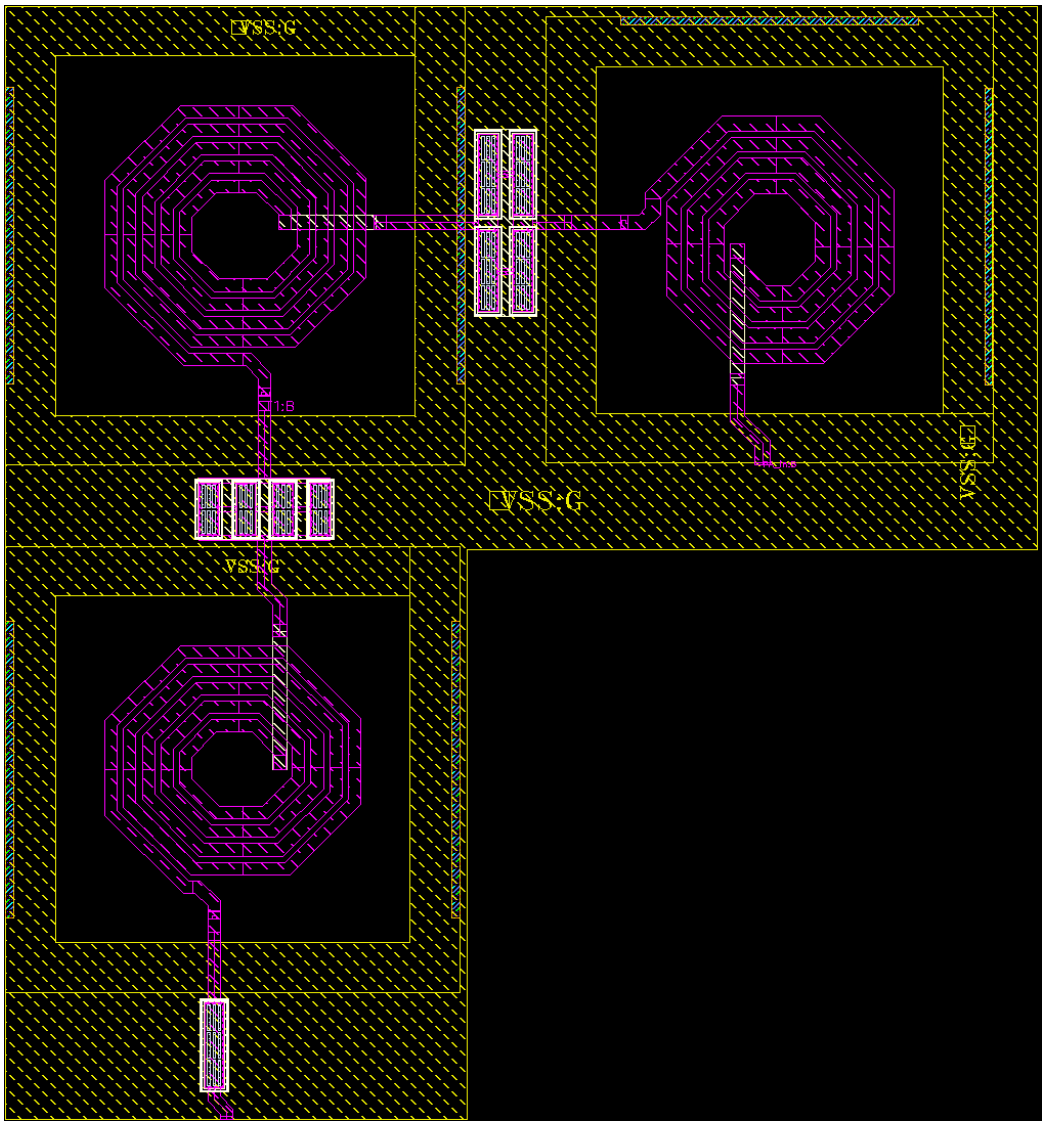


Figure 5.2: Input Matching Network Layout.

5.3 Active Core

The core building block is composed by the layout of the cascode branch HS-MS with their proper guard ring including also the contacts to the p-substrate. In addition, the resistive feedback is realized with a poly resistance with a proper width that can guarantee the rms current flow. The *"big,fat"* shunt capacitance BFC is also included and it can be noticed that its area occupation is relatively significant.

The cascode core layout is reported in the following figure. It can be noticed that there are also included the resonant inductance L_{rf} and the BFL inductor. The wee hollow at the center will be occupied by the CE bias circuitry. The active core occupies a total area of $462 \times 465\ \mu m^2$.

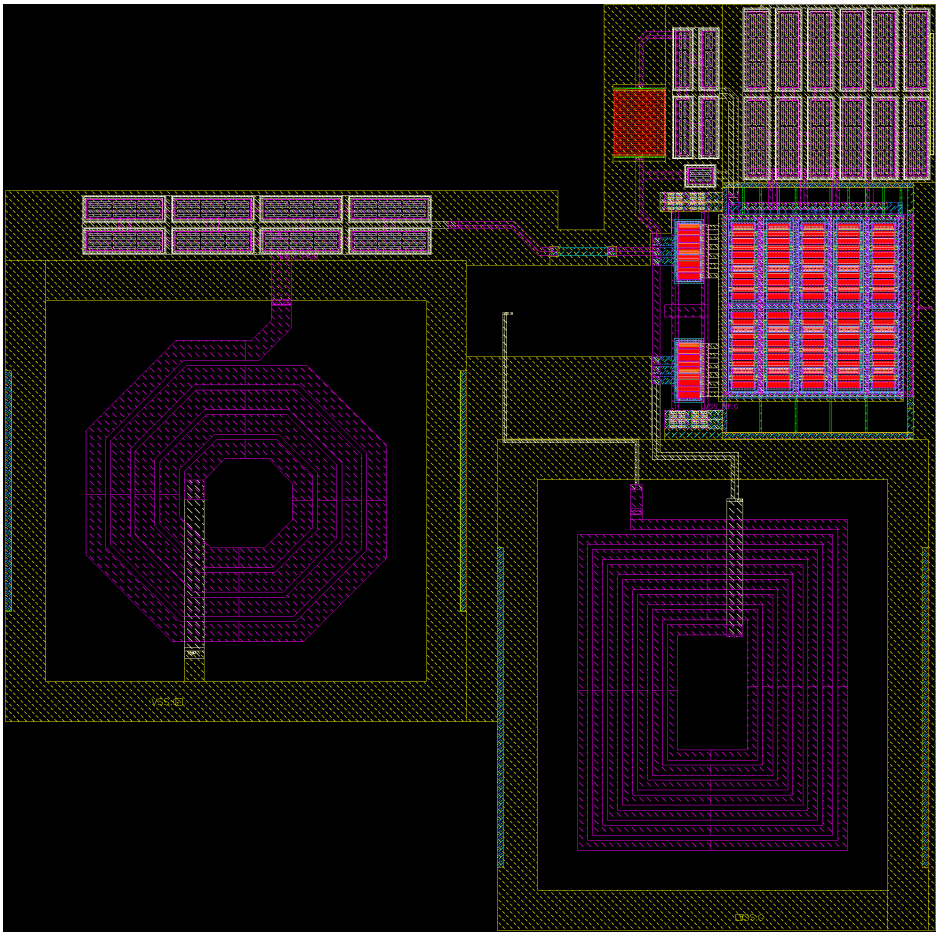


Figure 5.3: Active Core Layout.

5.4 Test Chip

By piecing all the pieces together, the layout of the whole test chip can be obtained which is the one reported in figure 5.4.

It can be noticed that we added the bias circuitry needed to provide the reference bias voltages and currents. As shown in Section 3.4.3, the bias block is composed by two high swing cascode current mirrors which their reference currents are provided the bias core. The latter is shown in the top left part of the test chip. Furthermore, there are also the aluminum pad for Ground-Signal-Ground (G-S-G) input and output ports, and the one for supply voltage and enable signal. An additive ground pin is added in order to streamline the ground connection closure.

In addition, it can be noticed the presence of a slight purple box around the test chip, which represents the target maximum area, *i.e.* $1448 \times 930\ \mu m^2$. As a results, the test chip layout fits perfectly inside this box, so much so that the total occupied area is $1427 \times 851\ \mu m^2$.

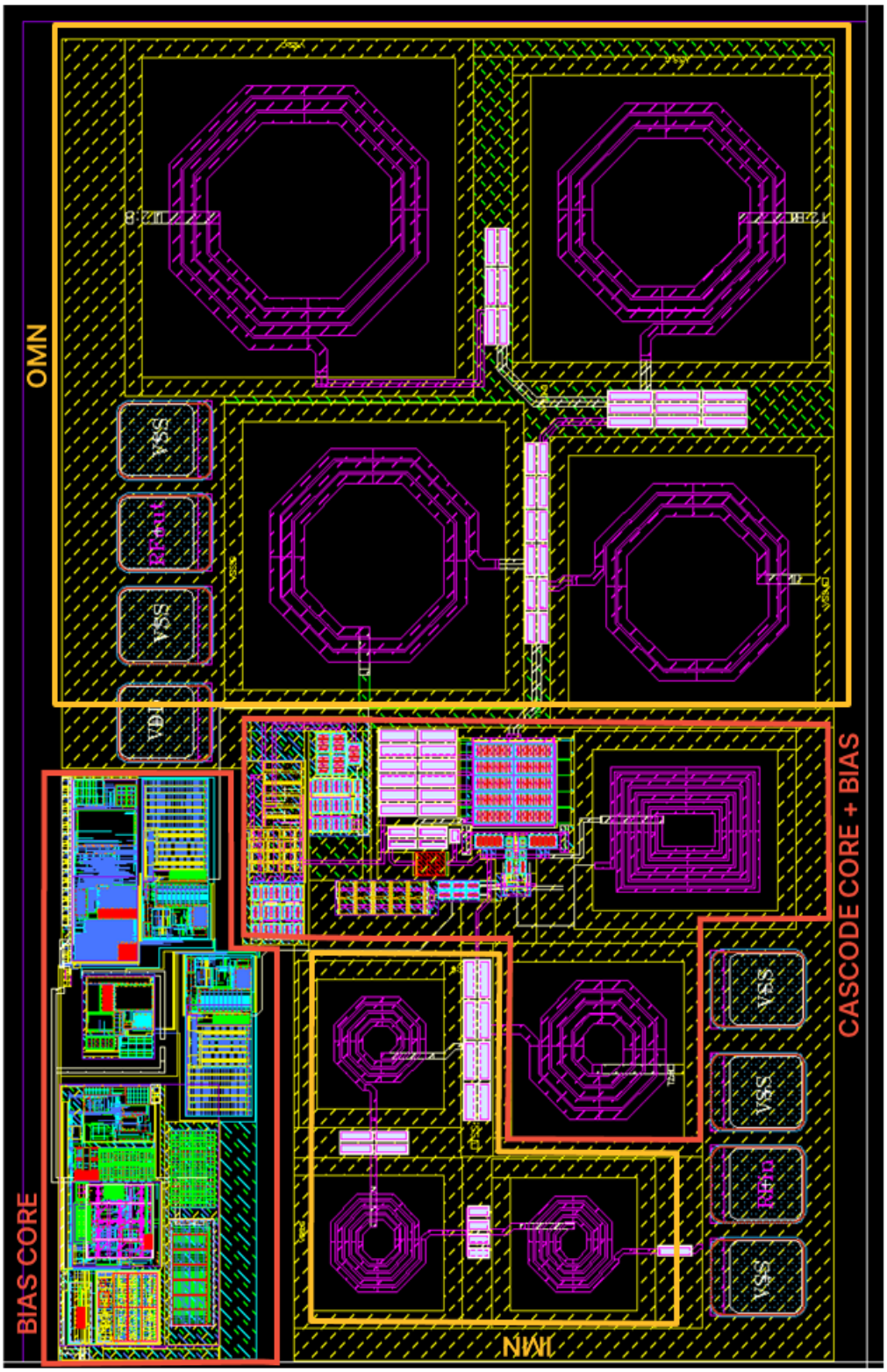


Figure 5.4: Test Chip Layout.

Chapter 6

Simulation Results

In this chapter a list of the achieved results is presented with the purpose to illustrate out RFIC single-ended Pre-Driver performances. Although the results refers to simulations, they are carried out considering real components and parasitic effects.

The chapter is organized in three main sections: in the first one, the small signal behavior with S-parameters performances are shown, taking into account also the stability. In the second one instead, there will be shown the results concerning power sweep and all the classical PAs figures of merit, such as OP1dB, efficiency, and, obviously, the OIP3, since we wanted to enhance linearity with this work. Finally, a brief section containing the DC consumption concludes the presentation.

Moreover, for the completeness of the analysis, we reported also the simulation in different temperature corner conditions ($T = 25° \ C$, $T = 115° \ C$ and $T = -40° \ C$) and for power supply variations in the order $\pm 5\%$ ($V_{DD} = 5 \ V$, $V_{DD} = 4.75 \ V$ and $V_{DD} = 5.25 \ V$). In addition, we recall that all the simulations are performed using HICUM models.

6.1 S-Parameters

6.1.1 Nominal Simulations

Examines the following list of figures more closely, it can be noticed that a well-performed matching is achieved for input and output ports. Both S_{11} and S_{22} enclose the center of the Smith Chart (50 Ω) properly. For what concerned the small-signal gain S_{21}, it can be seen that it is characterized by a slight remarkable steepness, but in the three band of interest, the flatness of 0.5 $dB/100\ MHz$ is guaranteed.

In addition, the concerned amplifier is unconditionally stable, since $K > 1$ within all the 10 GHz range, as illustrated in figure 6.4.

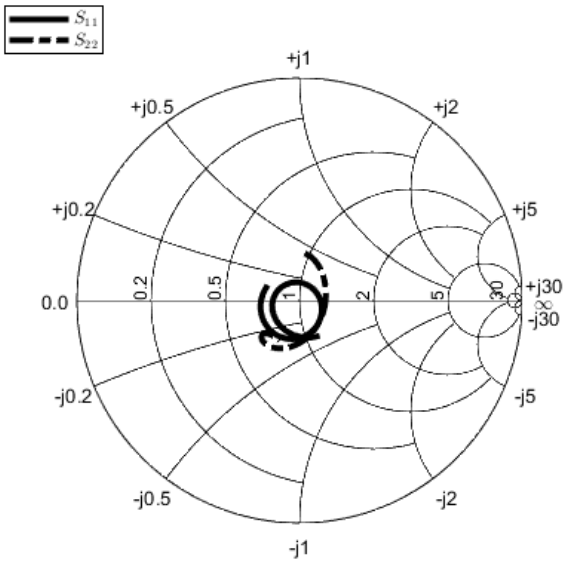
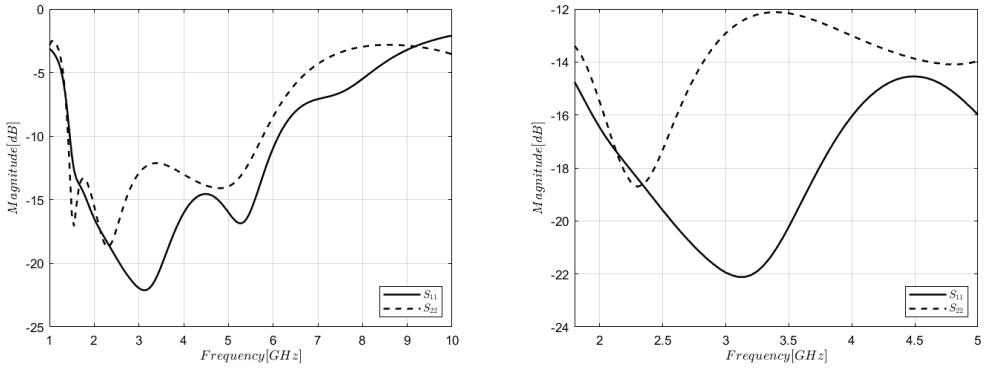
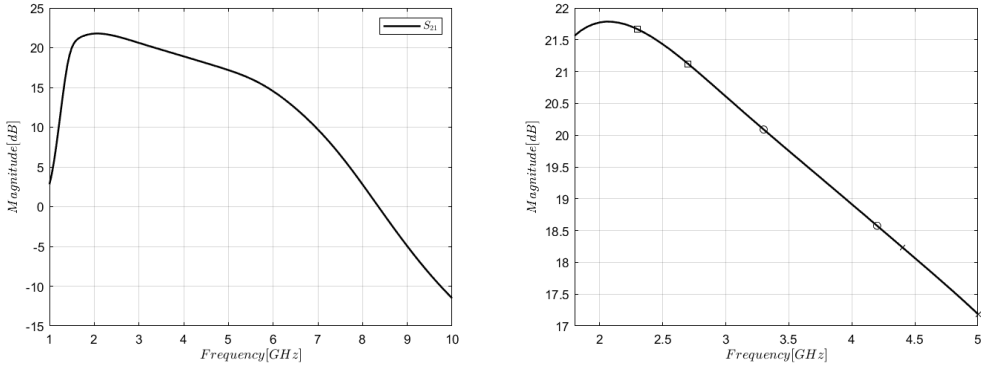


Figure 6.1: S_{11} and S_{22} for the Pre-Driver in the Smith Chart within 1.8 $GHz - 5\ GHz$ range.



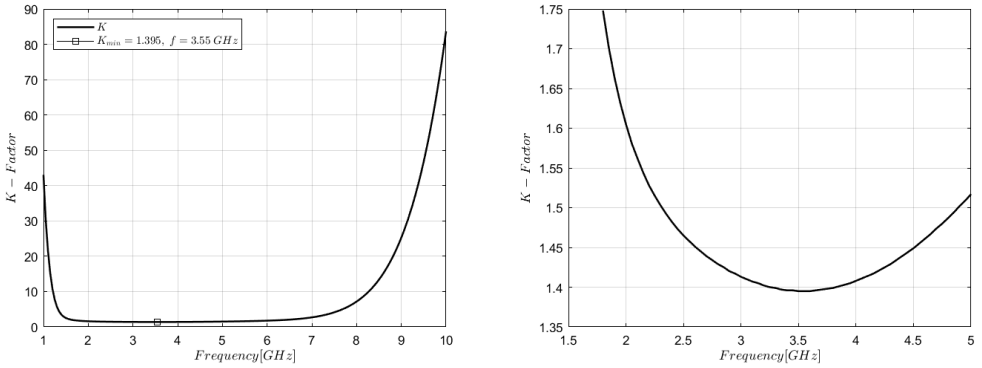
(a) (b)

Figure 6.2: Rectangular S_{11} and S_{22} for the Pre-Driver within 10 GHz range (a) and within 1.8 $GHz - 5$ GHz range (b). The input and output matching are satisfactory in the entire frequency range of interest ($|S_{11}| < -15\ dB$, $|S_{22}| < -12\ dB$).



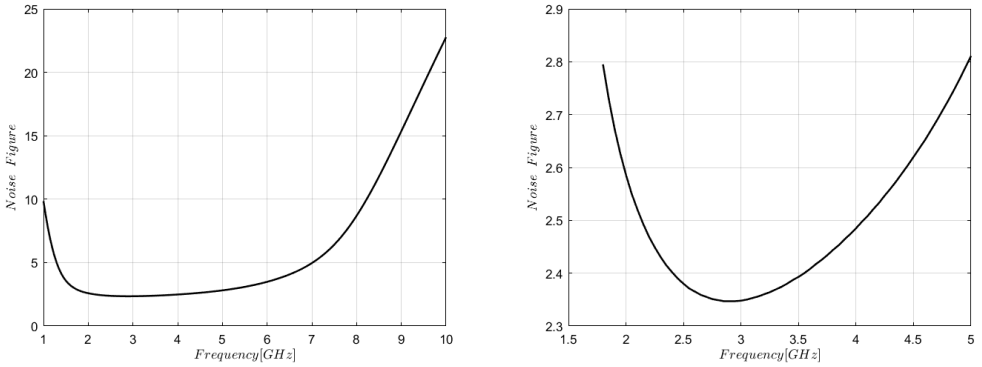
(a) (b)

Figure 6.3: Rectangular S_{21} for the Pre-Driver within 10 GHz range (a) and within 1.8 $GHz - 5$ GHz range (b). In the latter figure the three bands of interests reported in Section 3.1 are emphasized with markers. In particular, the sloped of the three bandwidths are: $Slope_{2.3-2.7GHz} = 0.544\ dB$, $Slope_{3.3-4.2GHz} = 1.515\ dB$ and $Slope_{4.4-5GHz} = 1.050\ dB$



(a) (b)

Figure 6.4: Rollet Factor for Pre-Driver within 10 GHz range and the evidence of its minimum (a) and within 1.8 $GHz - 5\ GHz$ range (b). $K > 1$ in all the frequencies ranges, so unconditional stability is achieved.

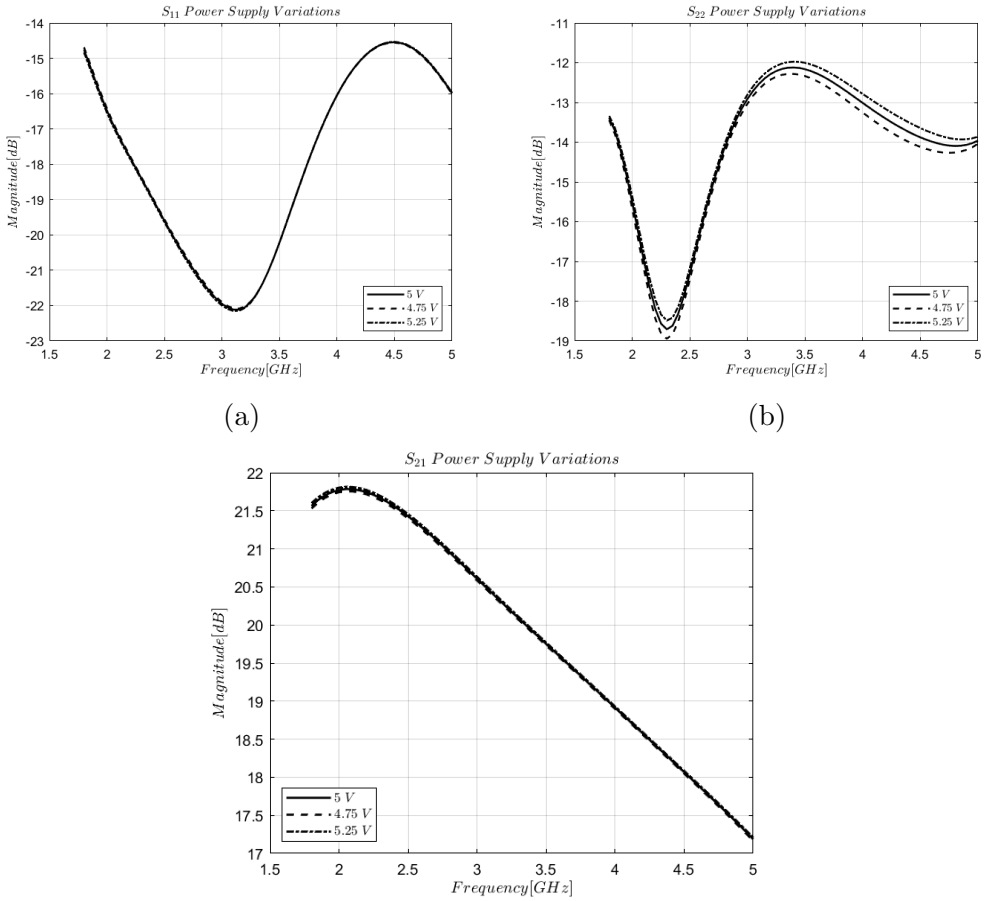


(a) (b)

Figure 6.5: Noise Figure for Pre-Driver within 10 GHz range (a) and within 1.8 $GHz - 5\ GHz$ range (b).

6.1.2 Power Supply Variations

After performing the simulations in nominal conditions, it is necessary to verify the behavior of Pre-Driver for slightly changings of the power supply. In particular, the assumed variation is around ±5%. Clearly, the expectation is that there will not be so much shifts for S-parameters, and this is confirmed by the results reported in the following. The simulations are intended in nominal temperature corner condition $T = 25° \ C$.



(a) (b)

(c)

Figure 6.6: Rectangular S_{11} (a), S_{22} (b) and S_{21} (c) for the Pre-Driver within 1.8 $GHz - 5\ GHz$ range. The figure shows the sensibility of the input and output reflection coefficients to the power supply variations of ±5%. The variations are minimal and almost imperceptible for S_{11}, S_{21} and slightly remarkable for S_{22}.

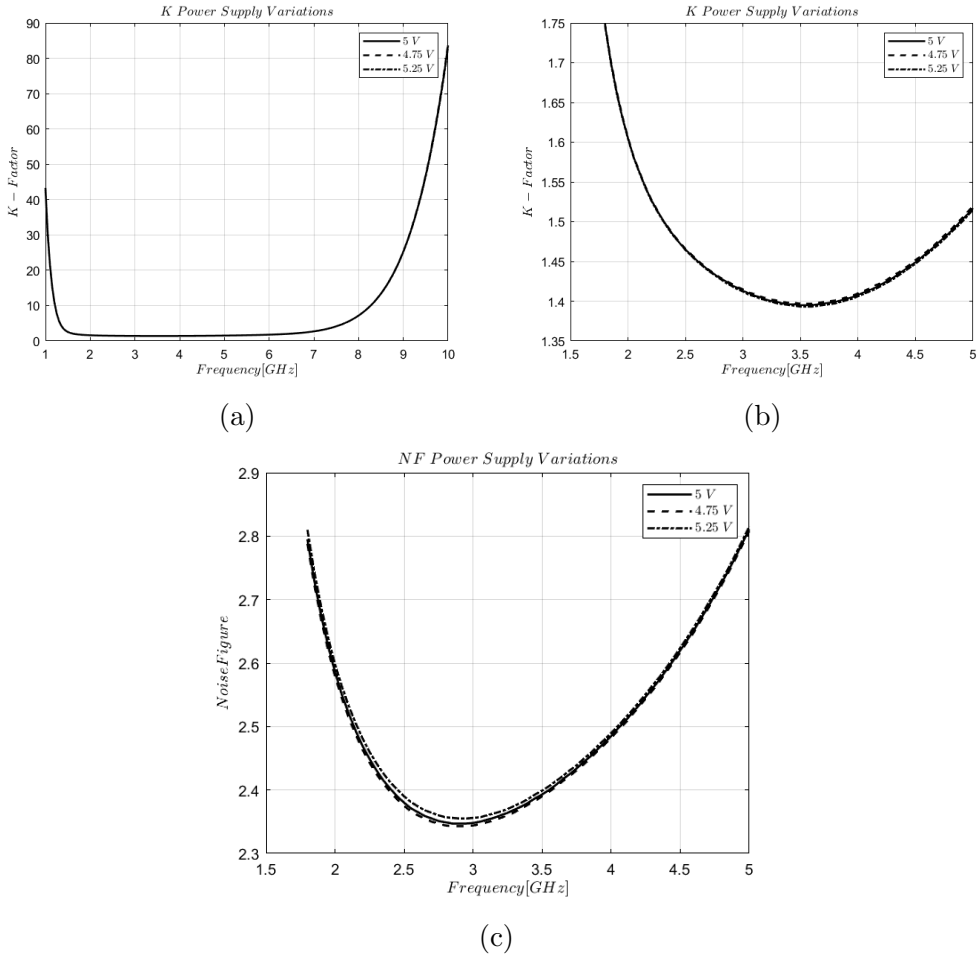


Figure 6.7: Rollett Factor for Pre-Driver within 10 GHz range (a) and within the band of interest 1.8 GHz−5 GHz (b). Noise Figure for Pre-Driver within 1.8 $GHz - 5$ GHz (c). $K > 1$ in all the different power supply variations and so unconditional stability is achieved. Furthermore, it can be noticed that the variations are again minimal and almost indistinguishable.

6.1.3 Temperature Variations

The simulation results regarding three different temperature corner conditions are reported in the following list of figures. In particular, the circuit has been simulated at $T = 25\ ^\circ C$ (nominal), $T = 115^\circ C$ and $T = -40\ ^\circ C$.

As already mentioned in chapter 4, the main difference between the three different temperatures is that at the higher ones, the metals will exhibit more resistive loss. Not only that, also the transistors and poly resistance has a not negligible impact on the RF signal and the bias current at different tem-

peratures. As a result, general performance worsening can occur especially at higher T corners. This means that, for example, the small signal gain will be lower at $T = 115°\ C$ with respect to $T = -40°\ C$. Furthermore, it can be noticed that there is a remarkable difference between the noise figure of the Pre-Driver at the different temperatures. Clearly, higher temperature yields to higher thermal noise and so higher will be the noise figure.

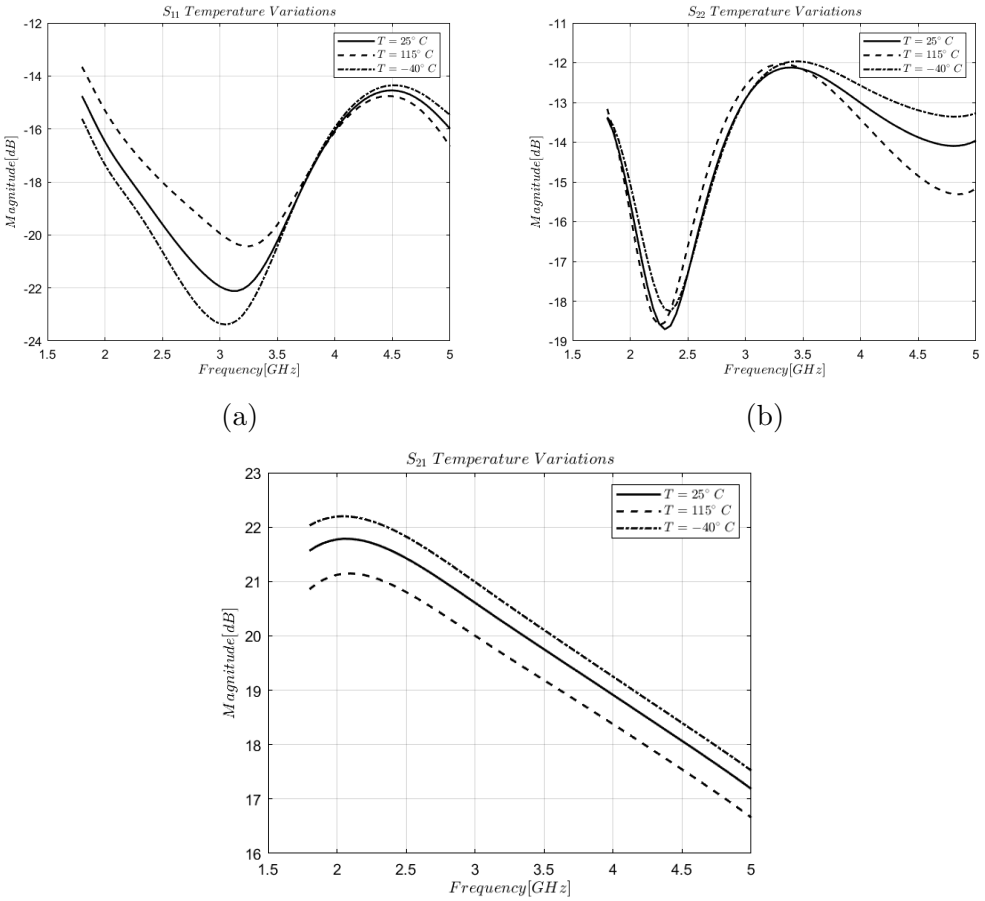


Figure 6.8: Rectangular S_{11} (a), S_{22} (b) and S_{21} (c) for the Pre-Driver within 1.8 $GHz - 5\ GHz$ range. The figure shows the sensibility of the input and output reflection coefficients to the temperature variations. The input and output matching are satisfactory in the entire frequency range of interest ($|S_{11}| < -14\ dB$, $|S_{22}| < -12\ dB$). Furthermore, it can be noticed that the small-signal gain S_{21} is higher at lower temperature since there are less losses.

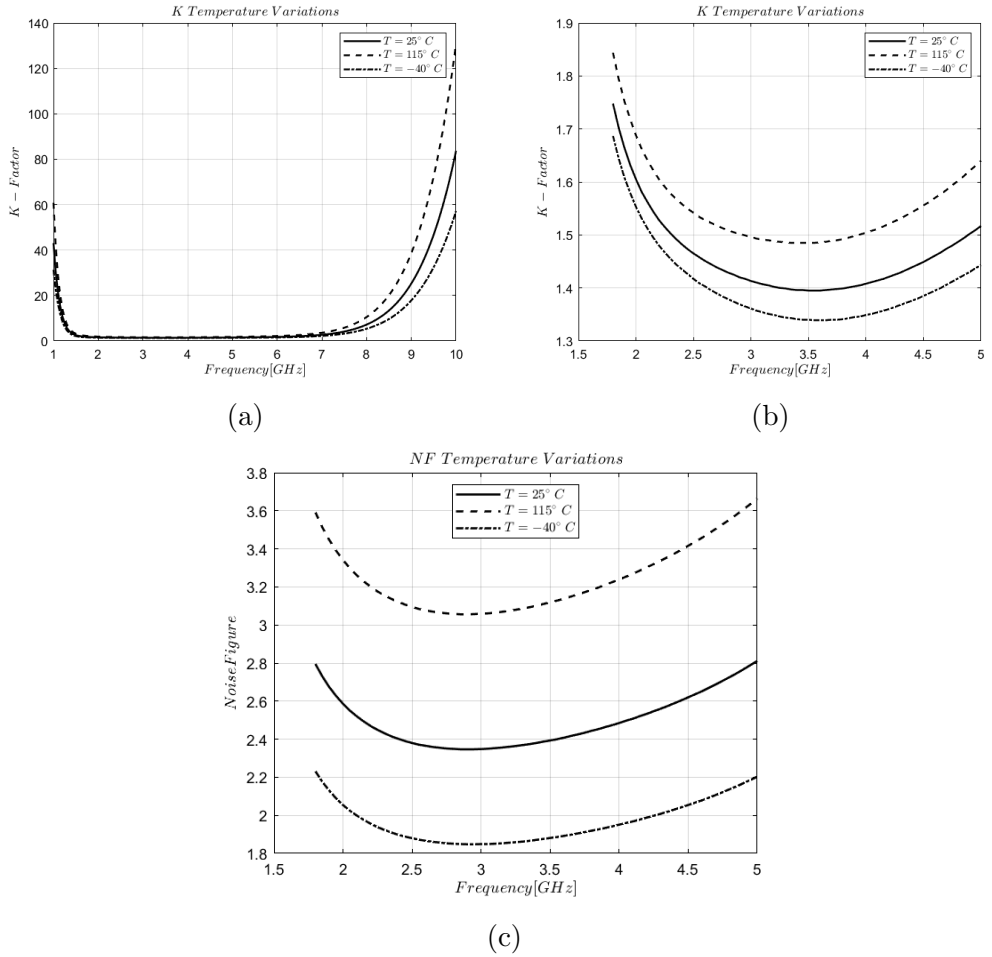


Figure 6.9: Rollett Factor for Pre-Driver within 10 GHz range (a) and within the band of interest 1.8 GHz−5 GHz (b). Noise Figure for Pre-Driver within 1.8 $GHz - 5$ GHz (c). $K > 1$ in all the temperature corner conditions and so unconditional stability is achieved. In addition, it can be noticed that the variations regarding NF are almost considerable, since higher temperatures leads to higher thermal noise. However, in all the three cases, the NF is below the maximum target requirement.

6.2 Power Sweep

After analyzing the Pre-Driver's small signal behavior, it is necessary to simulate the large signal one by performing power sweep simulations. As the previous section, a list of figures containing the simulation results is presented in nominal conditions and with temperature and power supply variations. The simulations have been performed in five frequency points concerning the

boundaries of internal bandwidths and the operating frequency, *i.e.* 1.8 GHz, 2.3 GHz, 3.6 GHz, 4.2 GHz and 5 GHz. This is done in order to deepen the large signal behavior of the amplifier within the band of interest.

6.2.1 Nominal Simulations

The presentation of the nominal power sweep simulations can only begin with the most relevant specification, *i.e.* the OP1dB. It can be noticed in figure 6.10 that the Pre-Driver is able to achieve a maximum OP1dB of 27.4 dBm nearby the operating frequency $f_0 = 3.6\ GHz$, and on the whole band of interest the OP1dB is larger than 25 dBm.

The list of figures continues with the simulation results concerning the power gain, the collector efficiency and the power added efficiency. All the plots are referred to P_{out}, in order to put things more in perspective in terms of output power.

Moreover, we reported also the insertion loss (IL) of the output matching network, since at the beginning we assumed a loss of 1.5 dB at the frequency of interest. As a result, the IL is almost smaller than 2 dB within the bandwidth. In addition, the load lines at $P_{in} = -10\ dBm$ and at $P_{in} = 10\ dBm$ of the Pre-Driver are reported in figure 6.15.

OP1dB

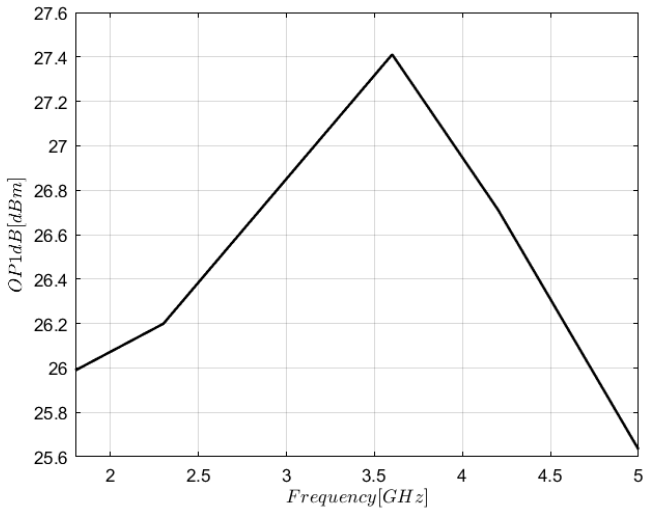


Figure 6.10: OP1dB within the 1.8 $GHz - 5\ GHz$ range. The specification regarding the OP1dB of 26 dBm (TYP) is satisfied.

OIP3

In order to check Pre-Driver linearity performance, a two tone test has been performed for all the same previous frequency points. The offset spacing between the two input tones is $\Delta_{offset} = 1\ MHz$. In the following figure, it is reported the OIP3 for both higher and lower spectrum tones, referred to $P_{in} = -20\ dBm$. In particular, it can be seen that the Pre-Driver exhibits a OIP3 (higher tone) of 37.5 dBm and a OIP3 (lower tone) of 40.4 dBm for the operating frequency $f_0 = 3.6\ GHz$. Moreover, the Pre-Driver is able to provide the required OIP3 on all over the band of interest.

The difference between the two OIP3 quantities highlighted the presence of memory effects. The concept of memory in RF amplifier is crucial for many applications and deserves the worth attention. Memory effects are caused by time variations in the amplifier's transfer characteristics and since the RF PA has to provide a stable power to the antenna, any time variations may be concern.

However, the situation is not as dire as it sounds. Memory effects do not affect the normal operation of a linear amplifier. They are realized only as a time-dependent variation in the amplitude of distortion. Hence, this kind of effects could be safely ignored even in nonlinear amplifiers whose distortions are below specification. It is important to take them into consideration when distortions exceed specifications and the amplifier needs linearization [3] [19].

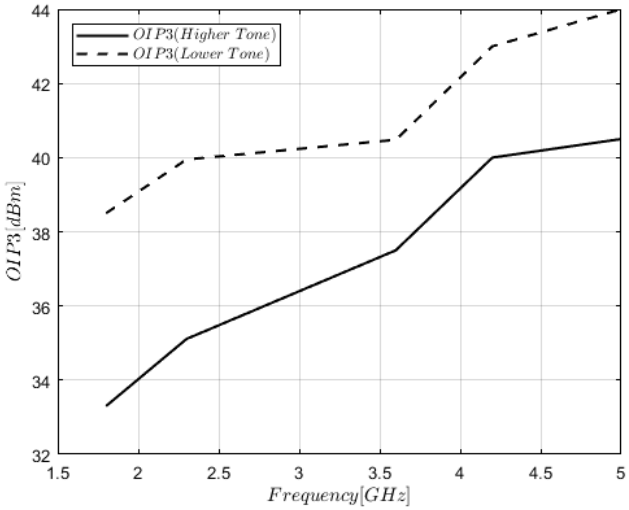


Figure 6.11: Output IP3 curves at $T = 25°\ C$ in the band of interest. The required OIP3 of 33 dBm is satisfied on all over the bandwidth.

Power Gain

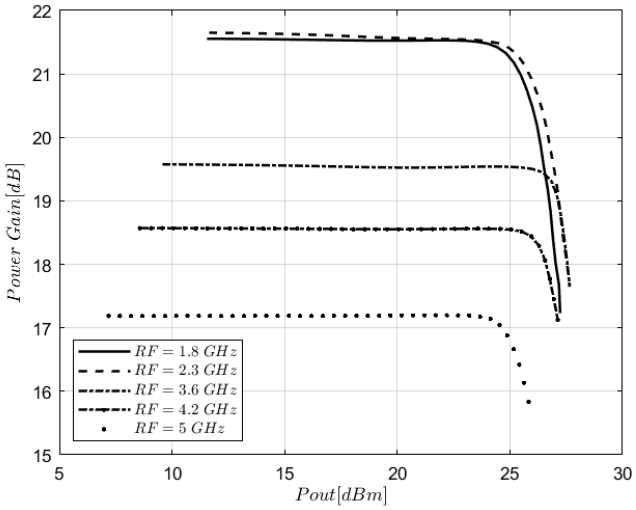
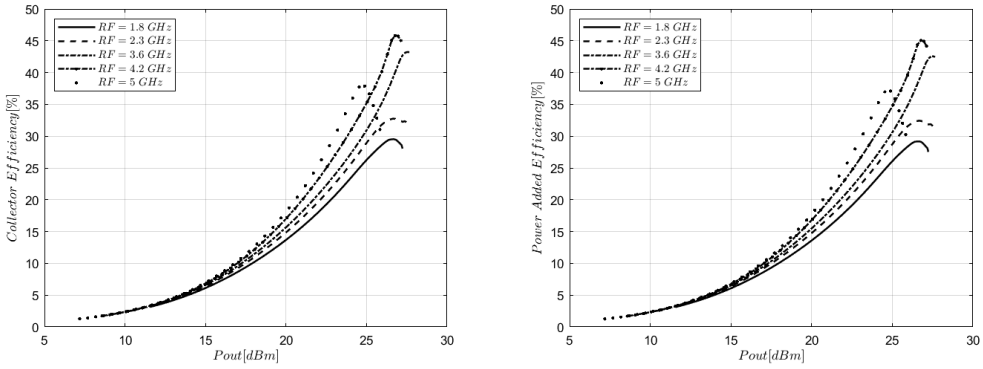


Figure 6.12: Power Gain for the five frequency points. It can be noticed that at f_0, the Pre-Driver is able to achieve a power gain of 19.5 dB, meanwhile at 5 GHz it is lower, according to the slight compression on the right boundary of the bandwidth in OP1dB.

Efficiency



(a) (b)

Figure 6.13: Collector Efficiency (a) and PAE (b) for Pre-Driver within the band of interest. It can be noticed that the amplifier can achieve maximum peak efficiency at 4.2 GHz. At the same time, the peak efficiency for f_0 is $CE = 42.55\%$ and $PAE = 43.23\%$.

Output Network IL

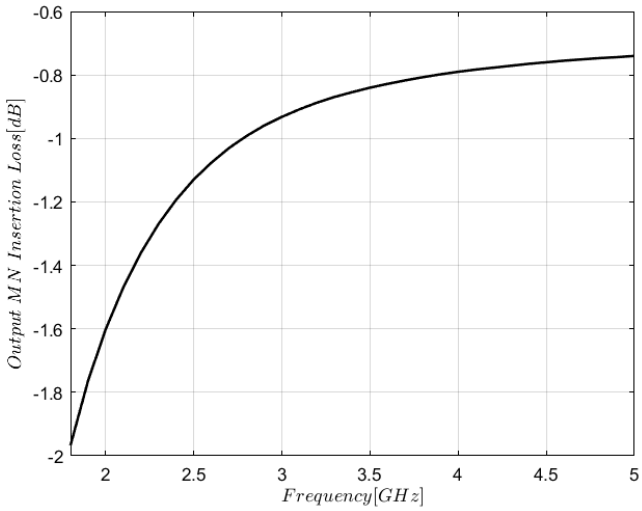
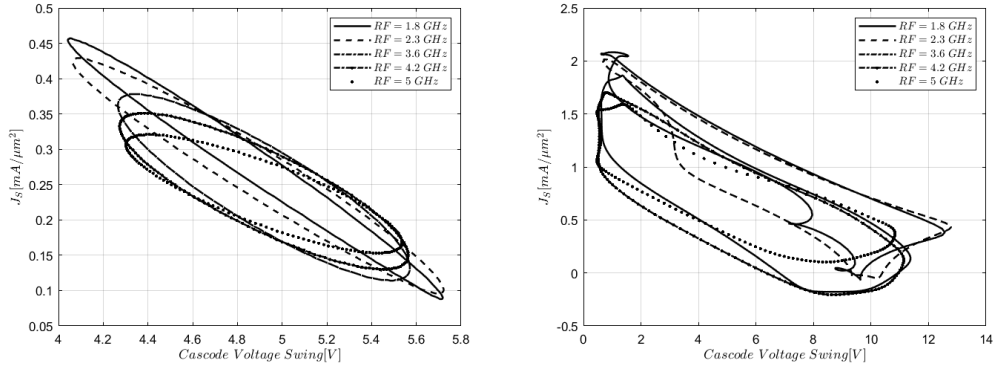


Figure 6.14: Insertion loss of the output matching network. IL is smaller than $-2\ dB$ on all over the bandwidth. The figure aids to deepen the loss mechanism at the output for the different frequencies.

Load lines



(a) (b)

Figure 6.15: Pre-Driver load lines for $P_{in} = -10\ dBm$ (a) and for $P_{in} = 10\ dBm$ (b). The load lines are referred to the cascode voltage swing vs. the cascode collector current density. It can be notice in figure (b) that at high input power level, the load lines become to be distorted and the cascode voltage swing increases a lot.

Bias Voltage CB configuration

The cascode voltage swing reaches high values and this may raise warnings concerns breakdown effects and CB instabilities. However, if we plot the bias voltage at the base contact of the CB stage to vary the input power, we can turn out few engaging reasoning.

Ideally, the bias voltage should show a monotonically descending behavior as the input power increases, and this is shown by the following figure. If the bias voltage increases within the input power range, this could be a serious problem since it might yield to CB instabilities and uncontrolled breakdown effects. However, it can be seen that the behavior of the curves is pretty similar to the ideal case, and this is enough to ensure that the high cascode voltage swing does not lead to the issues described above.

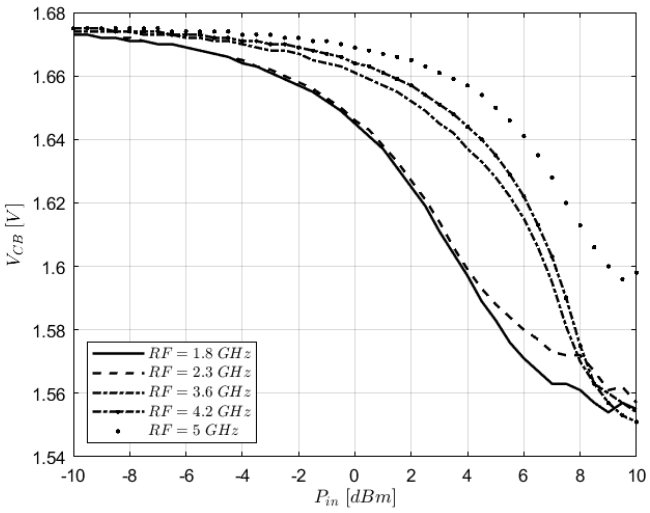


Figure 6.16: Bias voltage at the base contact of CB stages for the Pre-Driver to vary P_{in}. The figure shows the behavior for the five frequency points of interest.

6.2.2 Power Supply Variations

As the previous section, it is valuable to simulate the behavior of the Pre-Driver for power supply variations in nominal T corner condition. In order to avoid too much superposition between the curves, we decided to report the variations regarding the operating frequency $f_0 = 3.6\ GHz$.

Clearly, the expectation is that there will not be too much changes with respect to the nominal case, and this is almost satisfied by the following list of figures. Basically, when the power supply varies to $+5\%V_{DD}$, the cascode voltage swing is greater than the nominal condition and so larger output power delivered to the load can be achieved.

The figure 6.20 shows the bias voltage provided at the base contact of the CB stage by sweeping the input power level. Again, it can be seen that the curves are pretty similar to the nominal case and so no much worries regarding CB instabilities or breakdown effects can occur.

OP1dB

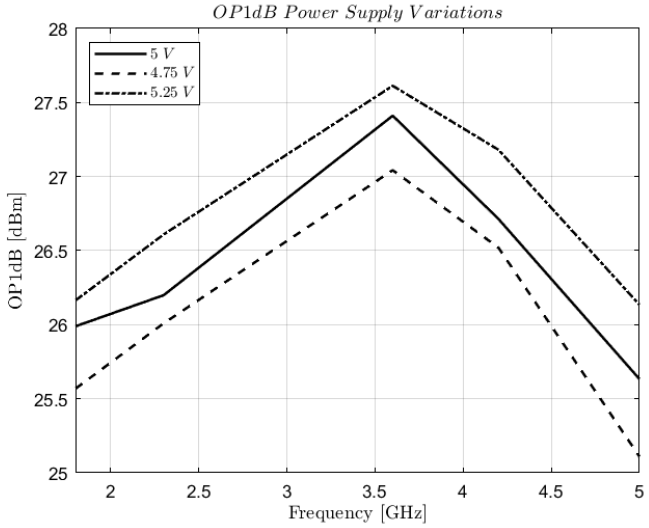


Figure 6.17: Power supply variations of OP1dB within the band of interest. It can be noticed that with $+5\%V_{DD}$, the Pre-Driver is able to reach higher OP1dB level, since the output swing is bigger with respect to the nominal case. However, the variations are not so remarkable in the three cases.

Power Gain

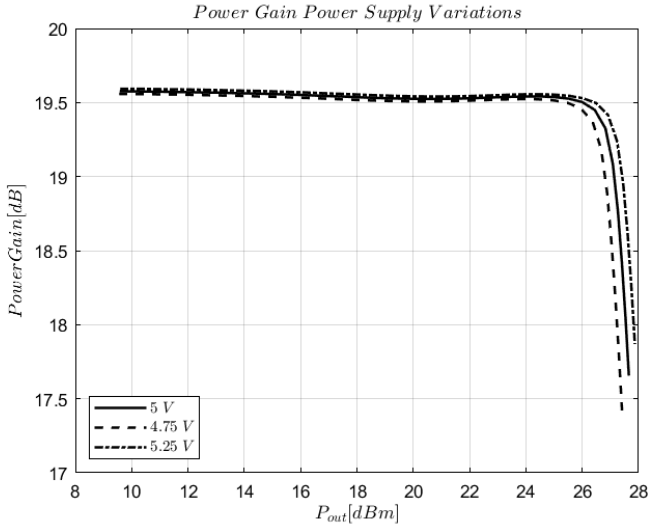
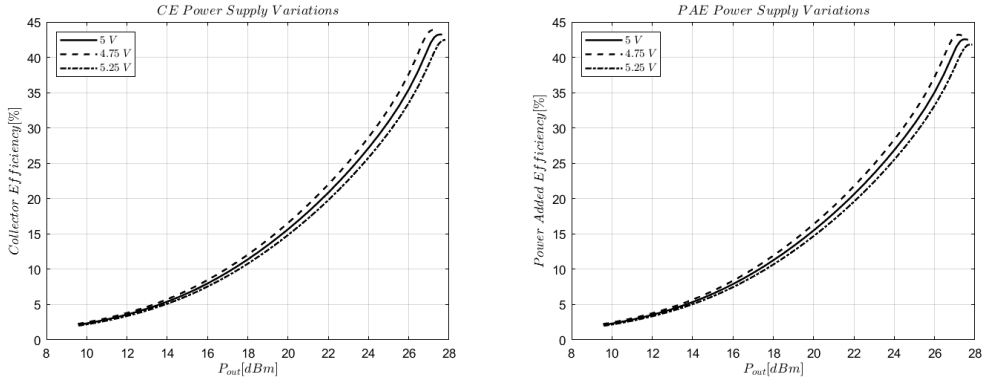


Figure 6.18: Power supply variations of power gain for f_0. The variations are pretty small, according to the ones regarding OP1dB.

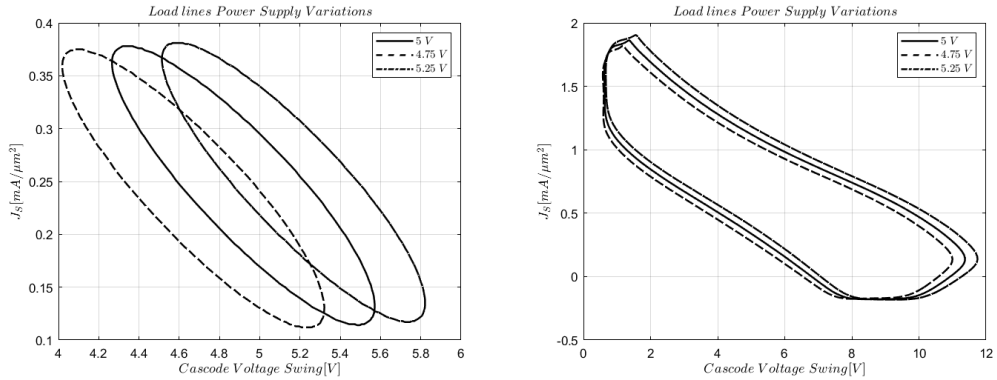
Efficiency



(a) (b)

Figure 6.19: Power supply variations of Collector Efficiency (a) and PAE (b) for Pre-Driver within the band of interest. Also here, the variations are slightly remarkable and almost imperceptible for both the efficiencies.

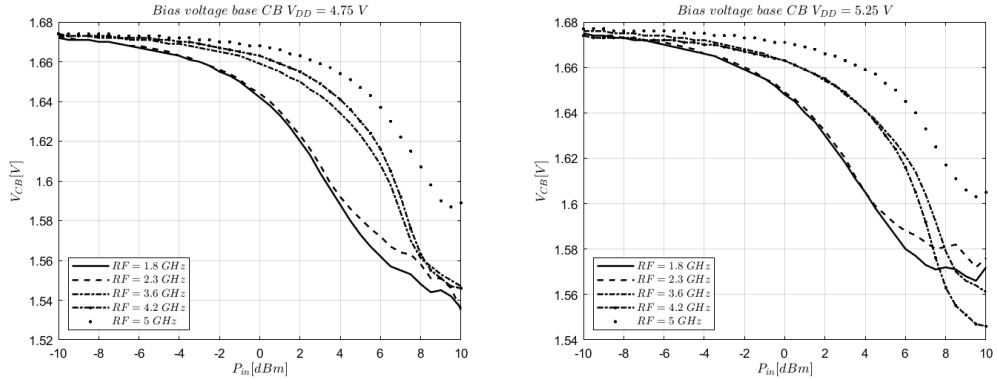
Load lines



(a) (b)

Figure 6.20: Power supply variations for the Pre-Driver load lines with $P_{in} = -10\ dBm$ and with $P_{in} = 10\ dBm$. The voltage swing is higher in $V_{DD} = 5.25\ V$ condition, and so the load lines are more stretched towards right.

Bias voltage at the base CB stage



(a) (b)

Figure 6.21: Power supply variations for the bias voltage provided at the base contact of CB transistors at $V_{DD} = 4.75\ V$ and $V_{DD} = 5.25\ V$. It can be seen that also here there is not much critical sign of CB instabilities and of breakdown effects, although the cascode voltage swing is pretty high. The curves are almost similar to the nominal condition.

6.2.3 Temperature Variations

Finally, we need to perform temperature variations for power sweep simulations. Although there were not so much changes with the S-parameters, the expectation here is pretty less optimistic especially for higher temperature, *i.e.* $T = 115° \ C$. As seen before, higher operation temperature yields to higher resistive losses for the metals, and this means that the power delivered to the load will be undoubtedly smaller with respect to the nominal condition. To sum up, we expect few remarkable shifts in the Pre-Driver's power sweep behavior.

The presentation of the results is presented in the following list of figures. It can be noticed that the OP1dB decreases sharply at $T = 115° \ C$, since the maximum output power level is 25.8 dBm. However, this changing is not so impressive, since the Pre-Driver is able to provide a OP1dB larger than 24 dBm on all over the bandwidth. On the other hand, at $T = -40° \ C$, higher OP1dB level can be achieved with respect to the nominal condition.

OP1dB

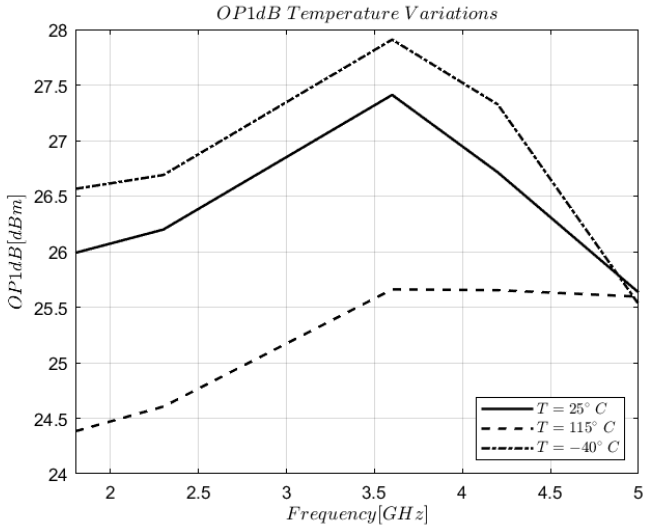


Figure 6.22: Temperature variations of OP1dB within the band of interest. As stated before, it can be noticed the remarkable shift at $T = 115° \ C$.

Power Gain

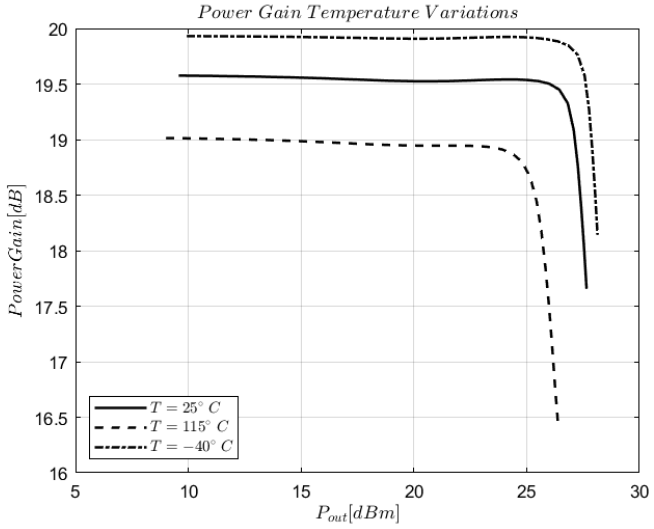
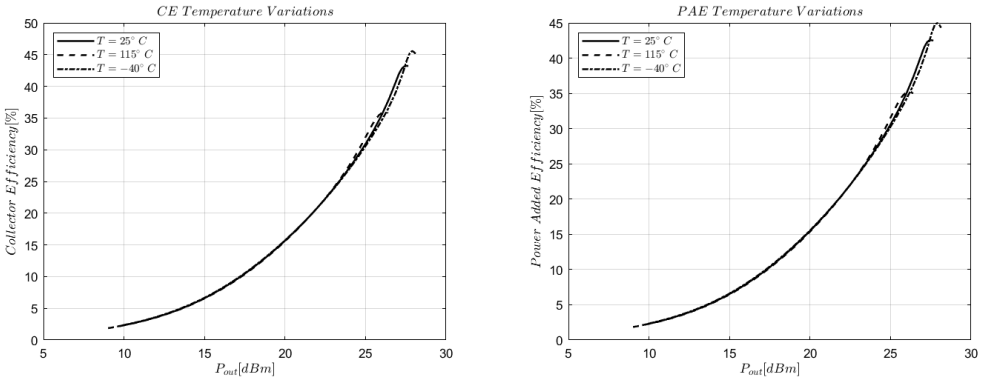


Figure 6.23: Temperature variations of power gain for f_0. The variations are relatively consistent, in particular at higher temperature where the power gain is lower according to the OP1dB performances.

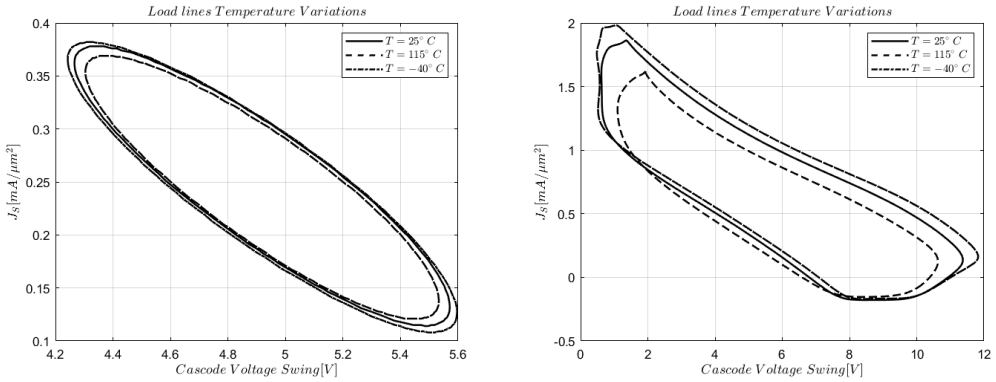
Efficiency



(a) (b)

Figure 6.24: Temperature variations of Collector Efficiency (a) and PAE (b) for Pre-Driver within the band of interest. Clearly, higher efficiency can be achieved at lower temperature, since the output power level is higher with respect to the highest temperatures.

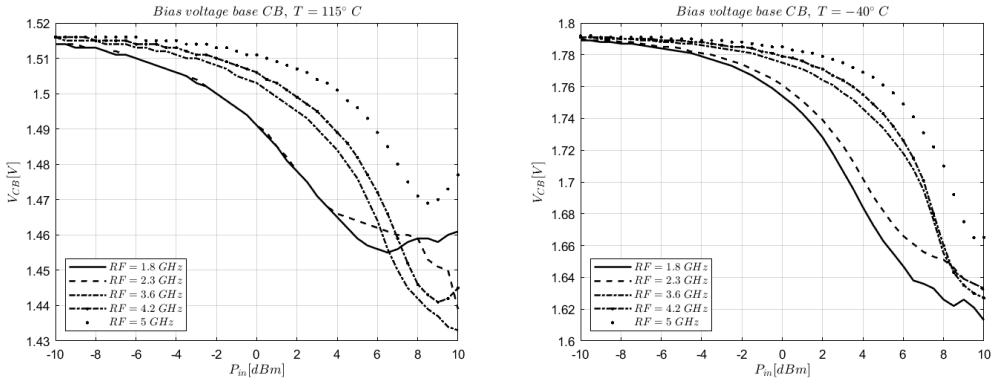
Load lines



(a) (b)

Figure 6.25: Temperature variations for the Pre-Driver load lines with $P_{in} = -10\ dBm$ and with $P_{in} = 10\ dBm$.

Bias voltage at the base CB stage



(a) (b)

Figure 6.26: Temperature variations for the bias voltage provided at the base contact of CB transistors at $T = 115^\circ\ C$ and $T = -40^\circ\ C$.

The list of figures concludes with the usual load lines and bias voltage to vary the input power. Unlike the previous section, this latter results highlighted a worthy warning for what concerned the cascode voltage swing at higher temperature. In particular, it can be seen that at higher P_{in} the cascode swing reaches values similar to the previous case, whilst, at the same time, the bias voltage at $f = 5\ GHz$ starts to increase sharply before with

respect to the other cases. This deserves some attention since uncontrolled bias voltage increase can lead to instabilities and breakdown voltage effects, as stated before.

6.3 DC Consumption

To conclude with, the DC consumption are reported in the following figure. In particular, the curves show the circuit DC consumption by varying the supply voltage in the range ±5% and the operating temperature. It can be shown that in all the presented cases, the P_{DC} satisfied the target requirement.

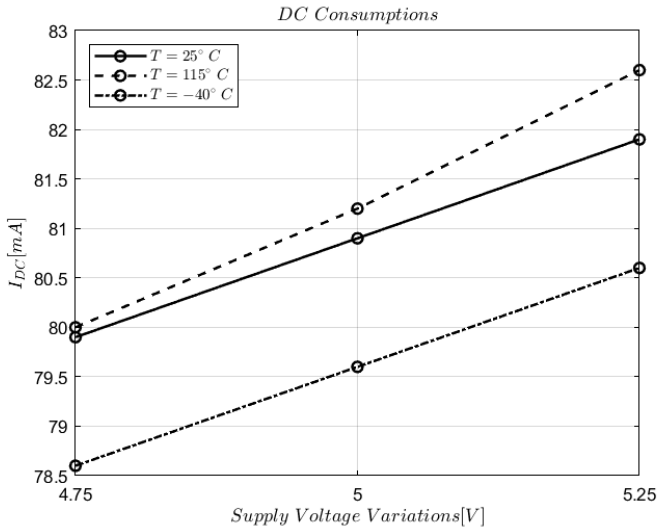


Figure 6.27: Pre-Driver DC consumption for power supply and temperature variations.

Chapter 7

Summary

The design of UWB single-ended Class AB Pre-Driver RF amplifier in SiGe 130 nm BiCMOS technology has been showed. The main results are summarized in the following table. Moreover, it has been proposed also the layout of the whole test chip.

The achieved performances are pretty competitive and they fully satisfied the target specifications of this work. In particular, the designed Pre-Driver matches the requirement in all over the bandwidth, ensuring its UWB applications. It is important to point out that the performances of the concerned RFPA shown in this thesis haven't been measured, but only achieved in simulation. In addition, further developments will include the test chip tape out in order to perform data measurements.

Parameter	Target (TYP)	Results (TYP)
P_{dc} $[mW]$	500	404.5
RL_{in} $[dB]$	15	19.75
RL_{out} $[dB]$	12	12.3
$Gain$ $[dB]$	18	19.5
$OP1dB$ $[dBm]$	26	27.4
$OIP3$ $[dBm]$	33	37
NF $[dB]$	5.3	2.45
$Area$ $[\mu m^2]$	1448×930	1427×851

Table 7.1: Table summarizing the Pre-Driver's final performances. The results are intended in nominal corner conditions ($V_{DD} = 5\ V$, $T = 25°\ C$) for the operating frequency $f_0 = 3.6\ GHz$.

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