Università degli Studi di Padova

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Analysis and design of a Series Resonant Current-Fed Dual Half-Bridge converter

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Abstract

In this thesis, the Series Resonant Current-Fed Dual Half-Bridge (SR-CFDHB) converter topology has been studied and designed.
This topology is very similar to the standard Current-Fed Dual Half-Bridge (CFDHB), and has some of the advantages of the original topology, such as filtered input current.
This characteristic could make the converter useful in automotive applications or in cases where a smooth input/output current is needed.
The topology has been studied under four degrees of freedom, then a modulation strategy and design procedure that minimize losses (both due to conduction and switching) have been proposed.
Finally, a prototype has been designed, simulated and realized to validate the study results.

Contents

Chapter 1

Introduction

The increasing need for decarbonization of our energy production means and transportation methods has been the fundamental driver of power electronics development.
Power electronics converters enable efficient managing of electric power, while maintaining low size.
Some application fields of DC/DC converters are Electric Vehicle (EV) chargers and, more in general, energy storage systems. For example, a general architecture of an EV battery charger can be seen in Figure 1.1.

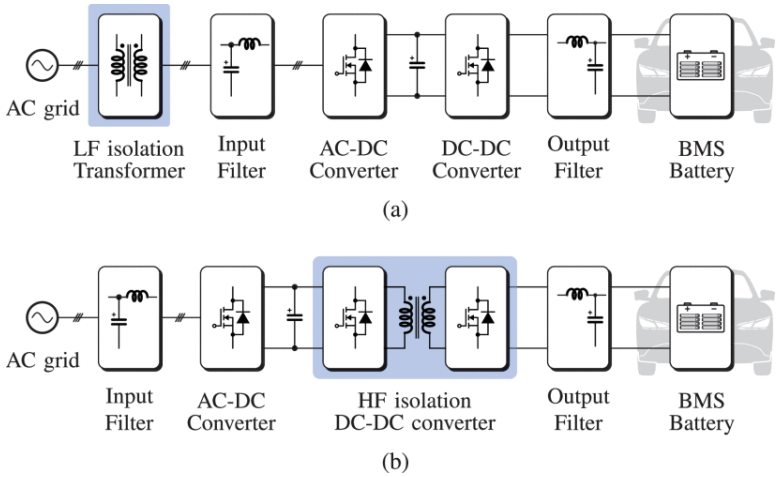


Figure 1.1: General structure of an EV battery charger from [1]

The system consists in a input section, where the charger is interfaced with the AC grid, a rectifier, often implementing Power Factor Correction (PFC), which is interfaced with the DC/DC converter via a DC-Link, the output filter and then

the battery with its Battery Management System (BMS).
The required galvanic isolation can be implemented at grid (low) frequency or integrated in the power conversion stages, using a high-frequency transformer.
The role of the DC/DC converter is to regulate the power transfer to the battery according to indications provided by the BMS. The power rating of domestic vehicle chargers range in the 1 kW to 22kW [1], so relatively high power values must be delivered at very high efficiency while minimizing the necessary space.
Another interesting application for DC/DC converters is as fundamental blocks of DC micro-grids.

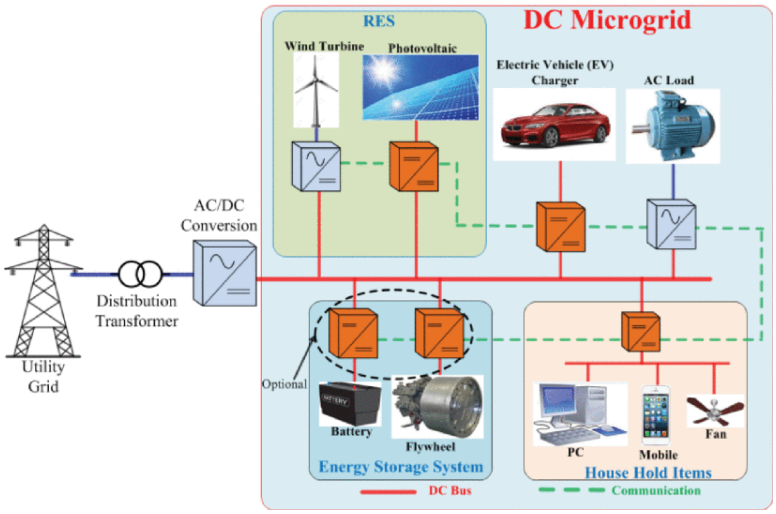


Figure 1.2: Architecture of a DC micro-grid [2]

The orange blocks represent the use cases for DC/DC converters. In particular, the ones which interface the grid to Energy Storage Systems (ESS) must have bidirectional power capabilities, to allow to utilize the stored energy in case of a blackout and charge the storage system when the grid operation is restored.
In particular, together with big, centralized ESS, domestic energy storage is present when renewable energy sources (e.g. photovoltaic) are employed. This could allow to integrate the domestic storage systems into the grid, obtaining a more stable energy distribution and, potentially, economic benefits for the house owners.
The employed DC/DC converters must be capable of high-efficiency bidirectional power transfer, while maintaining reliable operation, implementing galvanic isolation and reducing as much as possible injected electromagnetic disturbances.

Among the popular topologies consisting in the state of the art for this application, the dual half-bridge topology presents a cost-effective solution due to its reduced component count with respect to the Dual Active Bridge converter. This topology has many variations, which include different energy transfer impedance configurations (resonant or purely inductive) and combinations of current-fed (CF) and voltage-fed (VF) input/output half-bridges.
In particular, the Series-Resonant Current-Fed Dual Half-Bridge (SR-CFDHB) is explored in this thesis, with the objective of obtaining a control strategy and a design procedure to reach high-efficiency operation of this converter.
The converter is studied from a theoretical point of view in chapter 2. A control strategy to minimize the conduction losses is then proposed in chapter 3. Then, ZVS and its implication on the converter control are explored in chapter 4.
Guidelines to decide the component values and parameters are then given in chapter 5.
To validate the design, a prototype has been built in the laboratory. The procedure used to design the magnetic components is explained in chapter 6. The results from simulations and tests carried out in the laboratory are presented in chapter 7. Finally, a control architecture is proposed in chapter 8.

Chapter 2

SR-CFDHB analysis

In this chapter, the SR-CFDHB converter is going to be analysed in steady-state conditions. Subsequently, a preliminary analysis of the ZVS conditions for the converter is going to be carried out.
The SR-CFDHB circuit is represented in Figure 2.1. The resonant capacitance can be obtained by adding an external capacitor, which is totally equivalent to reducing the capacitance value of the voltage-fed side capacitive leg.

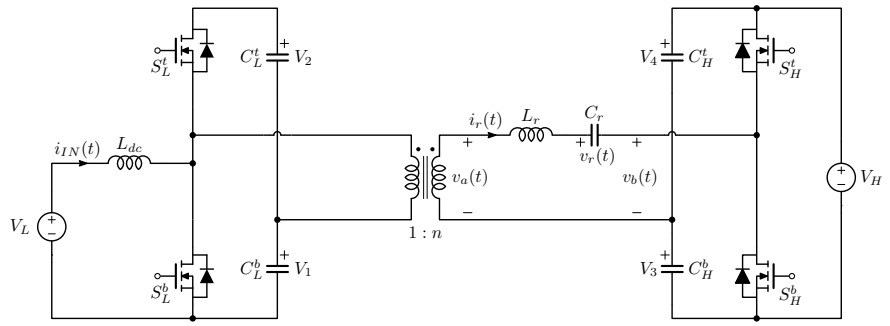


Figure 2.1: Series-Resonant Current-Fed Dual Half-Bridge converter circuit

For ease of calculations, the converter has been analysed in normalized form, by defining the following base and normalized variables:

- *Base time:* $T_N = 1/f_{sw}$
- *Base frequency:* $f_N = f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$
- *Base voltage:* $V_N = V_H$
- *Base impedance:* $Z_r = \sqrt{L_r/C_r}$

- *Base current:* $I_N = V_N/Z_r$
- *Base power:* $P_N = V_N^2/Z_r$
- *Normalized current:* $j_x = i_x/I_N$
- *Normalized voltage:* $u_x = v_x/V_N$
- *Normalized power:* $\Pi_x = P_x/P_N$
- *Normalized time:* $\tau = f_{sw}t$
- *Normalized frequency:* $f_n = f_{sw}/f_r$

2.1 Steady-state analysis

The CF side integrates a Boost converter cell, which can be controlled by the bottom switch (S_L^b) duty cycle D_b. For uniformity, also the VF duty cycle will be referred to the bottom switch (S_H^b).
At steady-state, the same simplifying assumptions of the non-resonant case [3] still hold.
This means that the bridge capacitors voltages can be considered constant during the switching period for the analysis.
Considering the Boost cell, its output voltage can be expressed as:

$$V_B = V_1 + V_2 = \frac{1}{1 - D_b} \tag{2.1}$$

From volt-second balance on the input inductance and on the transformer's primary side magnetizing inductance, voltages V_1 and V_2 (on capacitors C_L^b and C_L^t respectively) can be computed.
For the voltage-fed side, volt-second balance on the resonant inductance and on the transformer's secondary side magnetizing inductance yields voltages $V_3 + V_{C_r}$ and $V_4 + V_{C_r}$.
Since V_{C_r} (the average voltage across C_r) can be assumed as equal to zero without loss of generality, the Vs balances give the values of voltages V_3 and V_4 on C_H^b and C_H^t respectively.
The values of the capacitors voltages are summarized in Table 2.1.

Table 2.1: Average capacitors voltages

V_1	V_2	V_3	V_4
V_L	$\frac{D_b}{1-D_b}V_L$	$(1-D_h)V_H$	D_hV_H

Being a resonant converter, the SRCFDHB has 4 potential degrees of freedom:

1. The Boost cell duty cycle D_b
2. The voltage fed leg duty cycle D_h
3. The phase shift between the two legs D_φ
4. The switching frequency f_{sw}

This preliminary analysis focuses on the first three, leaving the switching frequency fixed at a value greater (e.g. 110%) than that of the resonant frequency, such as to obtain an inductive behaviour of the resonant tank impedance.
The phase shift is defined as the normalized time difference between the midpoints of the two legs' duty cycles and is considered positive when D_b leads D_h.
The assumption of constant capacitors voltages means that the resonant tank can be considered excited by two square-wave voltages, thus leading to current and voltage waveforms that are concatenations of sinusoidal shapes. This allows to carry out the analysis on the equivalent circuit shown in Figure 2.2.

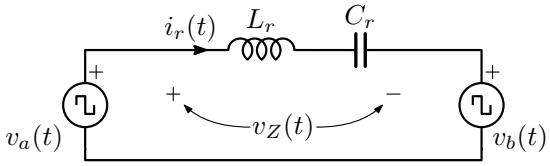


Figure 2.2: Equivalent circuit for resonant current and voltage analysis

Being this topology Dual Half-Bridge based, the switching period can be divided in four sub-intervals. During the k-th sub-interval ($\theta_{k-1} \leqslant \theta \leqslant \theta_k$, where $\theta = 2\pi\tau$), the current through inductor L_r and the voltage across capacitor C_r can be expressed in normalized form as follows:

$$\begin{cases} j_r(\theta) = j_r(\theta_{k-1})\cos\left(\frac{\theta-\theta_{k-1}}{f_n}\right) - u_r(\theta_{k-1})\sin\left(\frac{\theta-\theta_{k-1}}{f_n}\right) + U_{Z_k}\sin\left(\frac{\theta-\theta_{k-1}}{f_n}\right) \\ u_r(\theta) = j_r(\theta_{k-1})\sin\left(\frac{\theta-\theta_{k-1}}{f_n}\right) + u_r(\theta_{k-1})\cos\left(\frac{\theta-\theta_{k-1}}{f_n}\right) + U_{Z_k}\left[1-\cos\left(\frac{\theta-\theta_{k-1}}{f_n}\right)\right] \end{cases} \tag{2.2}$$

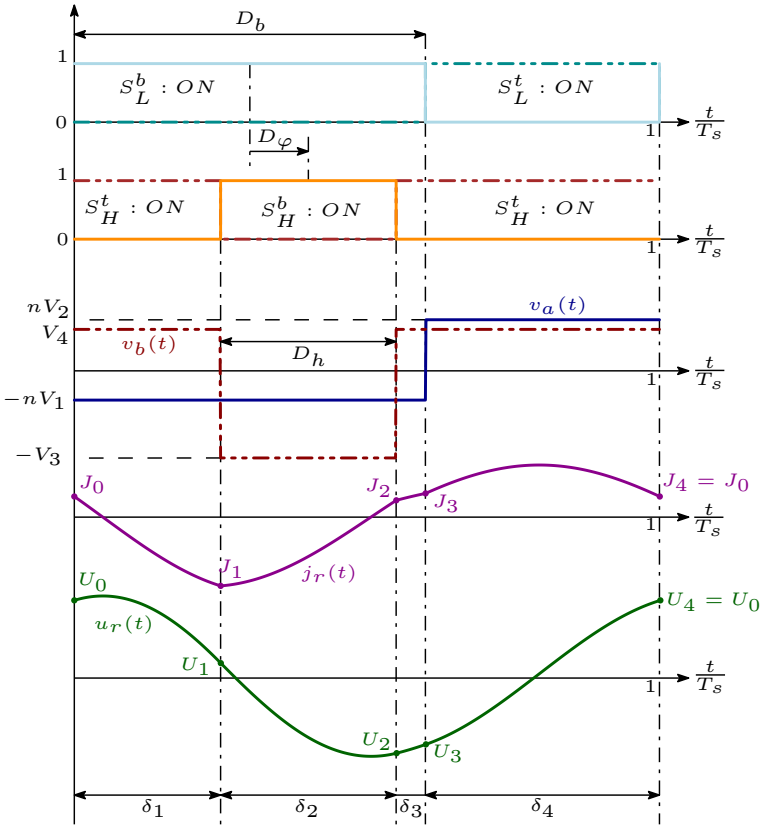


Figure 2.3: Generic waveforms during one switching period, including the switches' command signals

Using (2.2), the energy transfer impedance state variables ($x_k = [J_k U_k]^T$) at the end of the k-th topological state can be related to the previous one as

$$\begin{bmatrix} J_k \\ U_k \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{2\pi\delta_k}{f_n}\right) & -\sin\left(\frac{2\pi\delta_k}{f_n}\right) \\ \sin\left(\frac{2\pi\delta_k}{f_n}\right) & \cos\left(\frac{2\pi\delta_k}{f_n}\right) \end{bmatrix} \begin{bmatrix} J_{k-1} \\ U_{k-1} \end{bmatrix} + \begin{bmatrix} \sin\left(\frac{2\pi\delta_k}{f_n}\right) \\ 1-\cos\left(\frac{2\pi\delta_k}{f_n}\right) \end{bmatrix} U_{Z_k} \tag{2.3}$$

where $\delta_k = \tau_k - \tau_{k-1}$ is the normalized duration of the k-th interval. (2.3) can be expressed in compact form as

$$x_k = M_k x_{k-1} + N_k U_{Z_k}. \tag{2.4}$$

Since each switching period can be divided in $N = 4$ intervals, steady-state is reached when $x_4 = x_0$. This allows to use (2.4) iteratively to compute the initial state variables of the resonant tank, obtaining (2.5).

$$x_0 = \left[I_{2\times 2} - \prod_{i=0}^{N-1} M_{N-i} \right]^{-1} \cdot \left[\sum_{j=1}^{N-1} \left(\prod_{n=0}^{N-j-1} M_{N-n} \right) N_j U_{Z_j} + N_N U_{Z_N} \right] \tag{2.5}$$

With the initial conditions from (2.5), the ideal waveforms can be calculated numerically in normalized form by using (2.2).
Depending on the relative values of D_b, D_h and D_φ the converter can operate in different modes, which boundaries and conditions are the same as the ones of the non-resonant converter.
Example waveforms for each mode are reported in Figure 2.4.

Table 2.2: Normalized sub-interval durations for modes M1-M3

Operating mode	**M1**	**M2**	**M3**
δ_1	$\frac{D_b-D_h}{2} + D_\varphi$	$\frac{D_b-D_h}{2} + D_\varphi$	$\frac{D_b-D_h}{2} + D_\varphi - \frac{1+sgn(D_\varphi)}{2}$
δ_2	D_h	$\frac{D_b+D_h}{2} - D_\varphi$	$1 - D_h$
δ_3	$\frac{D_b-D_h}{2} - D_\varphi$	$\frac{D_h-D_b}{2} + D_\varphi$	$\frac{D_b-D_h}{2} + D_\varphi + \frac{1+sgn(D_\varphi)}{2}$

Table 2.3: Normalized sub-interval durations for modes M4-M6

Operating mode	**M4**	**M5**	**M6**
δ_1	D_b	$\frac{D_b+D_h}{2} + D_\varphi - 1$	D_b
δ_2	$D_\varphi + \frac{1-sgn(D_\varphi)}{2} - \frac{D_b+D_h}{2}$	$1 - D_\varphi + \frac{D_b-D_h}{2}$	$\frac{D_h-D_b}{2} + D_\varphi$
δ_3	D_h	$D_\varphi - \frac{D_h+D_b}{2}$	$1 - D_h$

Table 2.4: Tank voltage V_{Z_k} for each sub-interval in modes M1-M6

Mode	V_{Z_1}	V_{Z_2}	V_{Z_3}	V_{Z_4}
M1	$-nV_1 - V_4$	$-nV_1 + V_3$	$-nV_1 - V_4$	$nV_2 - V_4$
M2	$-nV_1 - V_4$	$-nV_1 + V_3$	$nV_2 + V_3$	$nV_2 - V_4$
M3	$-nV_1 + V_3$	$-nV_1 - V_4$	$-nV_1 + V_3$	$nV_2 + V_3$
M4	$-nV_1 - V_4$	$nV_2 - V_4$	$nV_2 + V_3$	$nV_2 - V_4$
M5	$-nV_1 + V_3$	$-nV_1 - V_4$	$nV_2 - V_4$	$nV_2 + V_3$
M6	$-nV_1 + V_3$	$nV_2 + V_3$	$nV_2 - V_4$	$nV_2 + V_3$

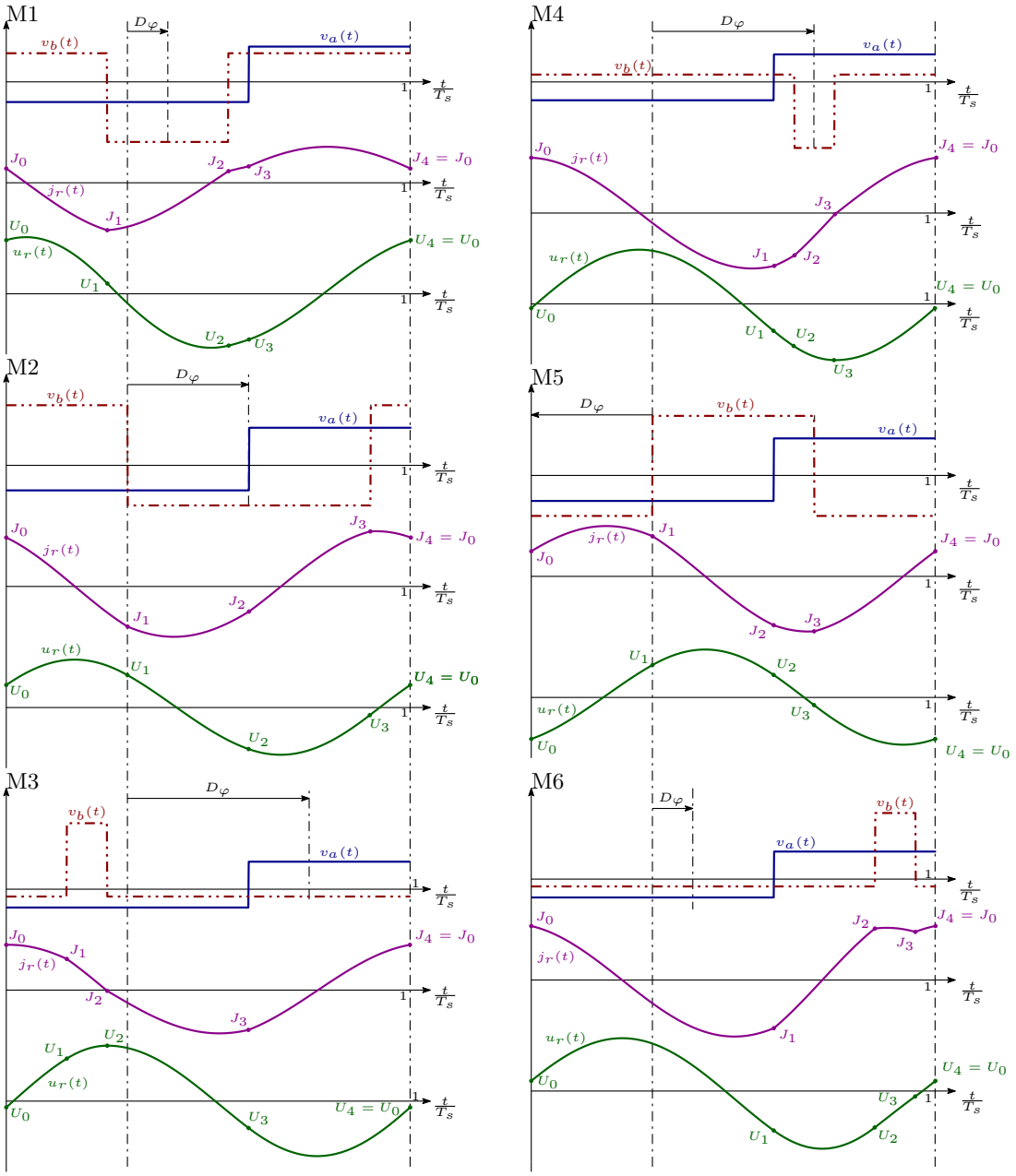


Figure 2.4: Steady-state waveforms for each operating mode

The normalized RMS inductor current can be calculated as:

$$J_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} j^2(\theta)d\theta}. \tag{2.6}$$

Using the first of (2.2), we obtain

$$J_{RMS}^2 = \sum_{k=1}^{N} \left(\frac{1}{2\pi} \int_{\theta_{k-1}}^{\theta_k} j^2(\theta) d\theta \right) = \frac{f_n}{4\pi} \sum_{k=1}^{N} \left\{ J_{k-1}^2 \left[\frac{\delta_k}{f_n} + \frac{1}{2} \sin\left(\frac{4\pi\delta_k}{f_n} \right) \right] + (U_{Z_k} - U_{k-1})^2 \left[\frac{\delta_k}{f_n} - \frac{1}{2} \sin\left(\frac{4\pi\delta_k}{f_n} \right) \right] + J_{k-1}(U_{Z_k} - U_{k-1}) \left[1 - \cos\left(\frac{4\pi\delta_k}{f_n} \right) \right] \right\} \tag{2.7}$$

The normalized average transferred power can be calculated from the general definition as

$$\Pi_t = \frac{1}{2\pi} \int_0^{2\pi} u_a(\theta) j(\theta) d\theta = \sum_{k=1}^{N} U_{A_k} \left(\int_{\theta_{k-1}}^{\theta_k} j(\theta) d\theta \right). \tag{2.8}$$

where $N = 4$ is the number of sub-intervals and $u_a(\theta)$ is the normalized voltage at the transformer's secondary winding.
By using once again the first of (2.2), the average normalized transferred power can be obtained as

$$\Pi_t = \frac{f_n}{2\pi} \sum_{k=1}^{N} U_{A_k} \left\{ J_{k-1} \sin\left(\frac{2\pi\delta_k}{f_n} \right) + (U_{Z_k} - U_{k-1}) \left[1 - \cos\left(\frac{2\pi\delta_k}{f_n} \right) \right] \right\}. \tag{2.9}$$

With (2.7) and (2.9) it is now possible to compute the normalized RMS current and power transfer to better understand the converter's behaviour at different operating points.
All the following plots are referred to a converter with $U_L = 0.5$ and $n = 0.5$.

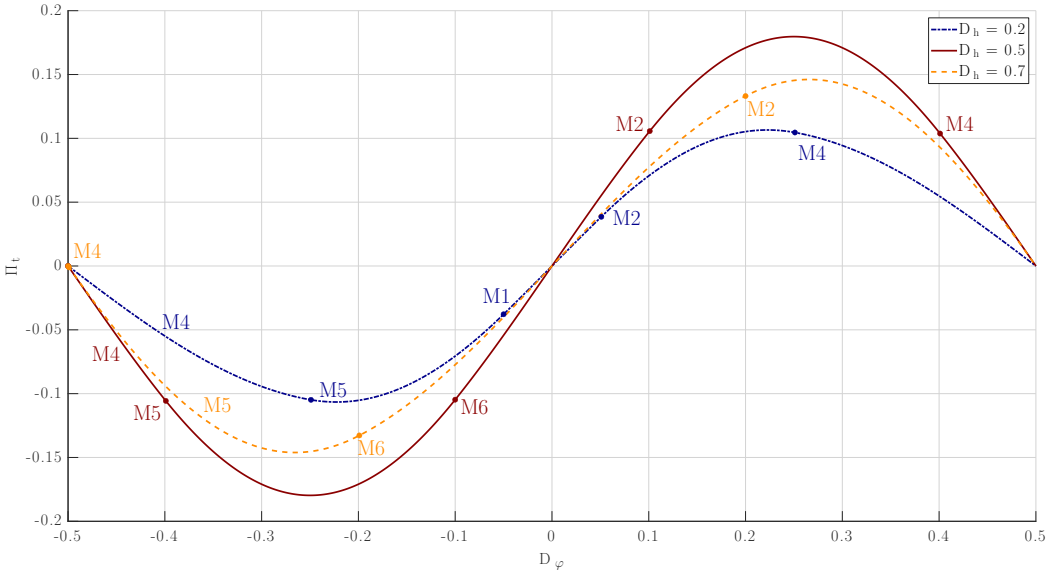


Figure 2.5: Normalized average power transfer at 3 values of D_h as function of D_φ. Operating mode transitions are also indicated by the dots

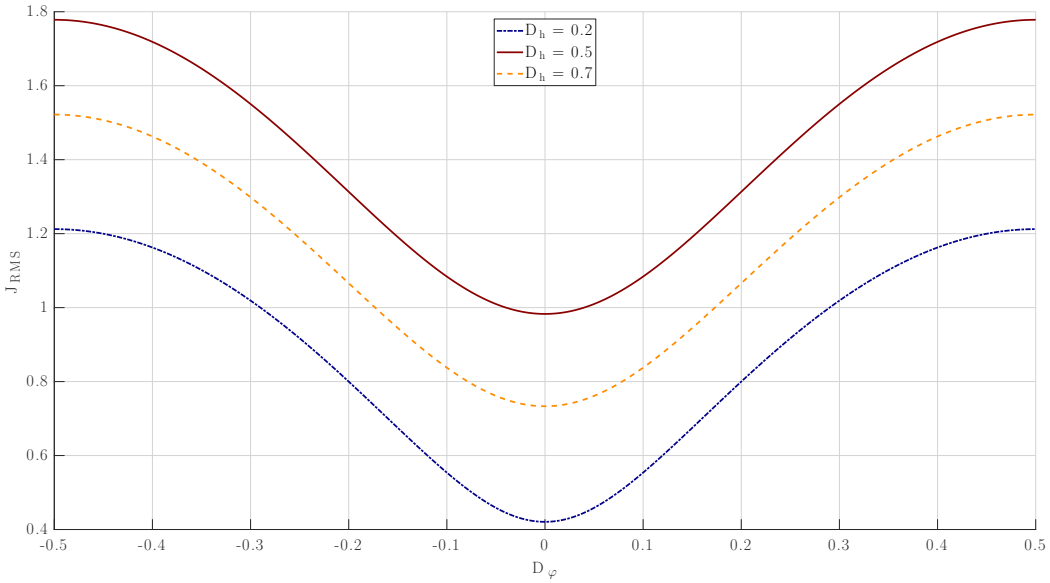


Figure 2.6: Normalized RMS inductor current at 3 values of D_h as function of D_φ

As it can be seen from Figure 2.5 the sign of the transferred power is equal to the one of D_φ. This means that the phase shift between the two bridges' command signals can be used to regulate the power flow direction (from CF side to VF side if $D_\varphi > 0$, from VF side to CF side if $D_\varphi < 0$) and also its magnitude.
Power is monotonic only in a range of D_φ values. It is paramount to operate in

this conditions (if D_h is set to a fixed value) to guarantee power controllability. Note that the value of D_h also influences this range: values of the voltage-fed leg duty cycle below 0.5 will reduce the available monotonicity interval. Having $D_h = 0.5$ ensures maximum power delivery and monotonic power transfer in $-0.25 \leqslant D_\varphi \leqslant 0.25$. The value of D_h also influences the magnitude of the transferred power and can thus be used to regulate it.

The maximum inductor RMS current is also obtained at $D_h = 0.5$, while D_h values further from 0.5 yield lower current (if D_φ is kept constant). J_{RMS} is also symmetrical with respect to D_φ.

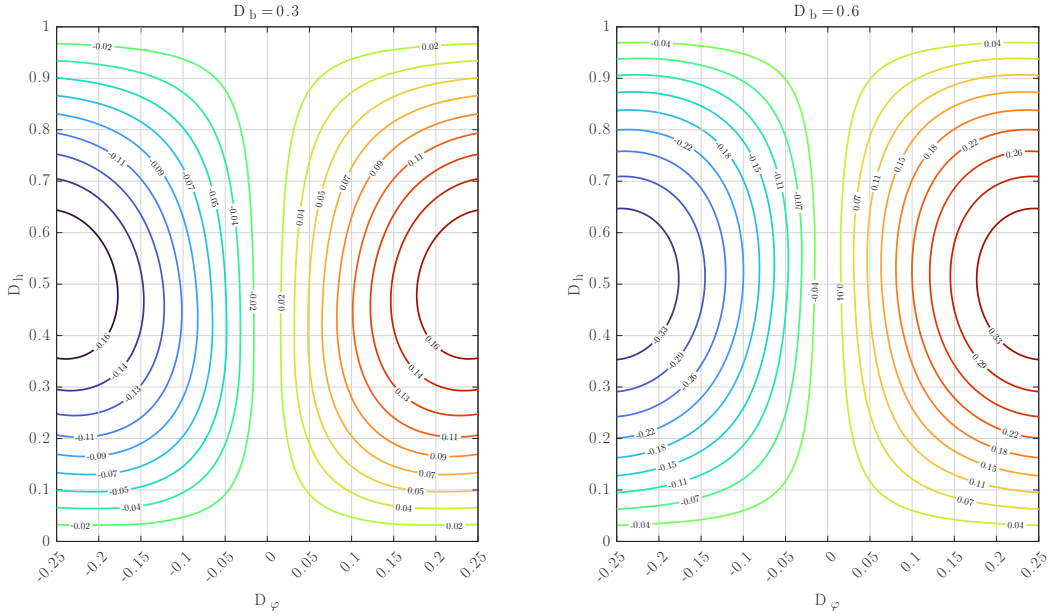


Figure 2.7: Average normalized power contours mapped at different D_h and D_φ values

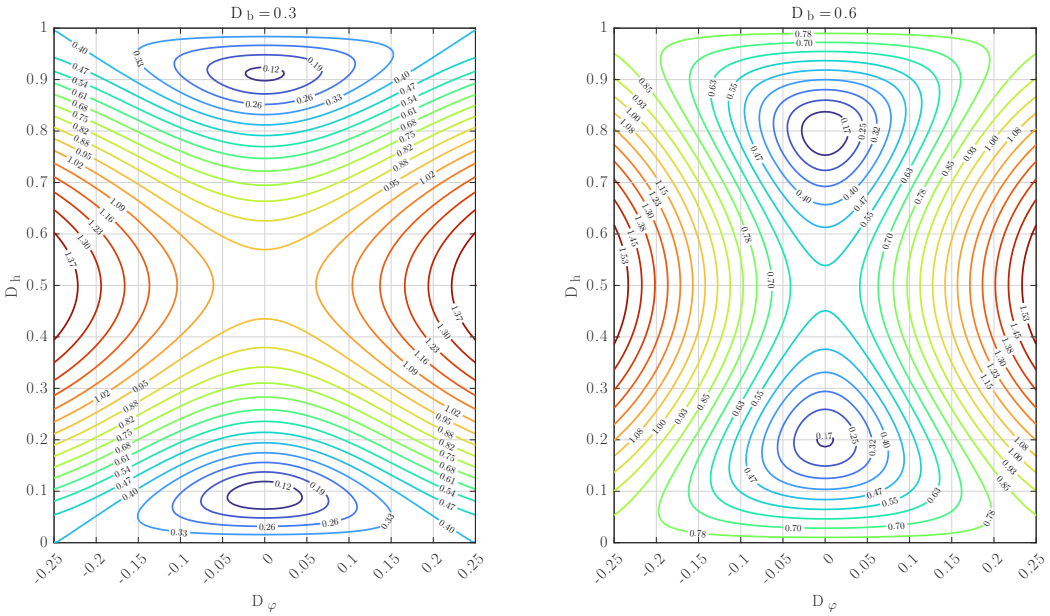


Figure 2.8: RMS normalized current contours mapped at different D_h and D_φ values

The contour maps in Figure 2.7 and 2.8 show that every power level can be obtained by combinations of D_φ and D_h values. The choice of this values could be also optimized based on the value of D_b and efficiency/ZVS range requirements.

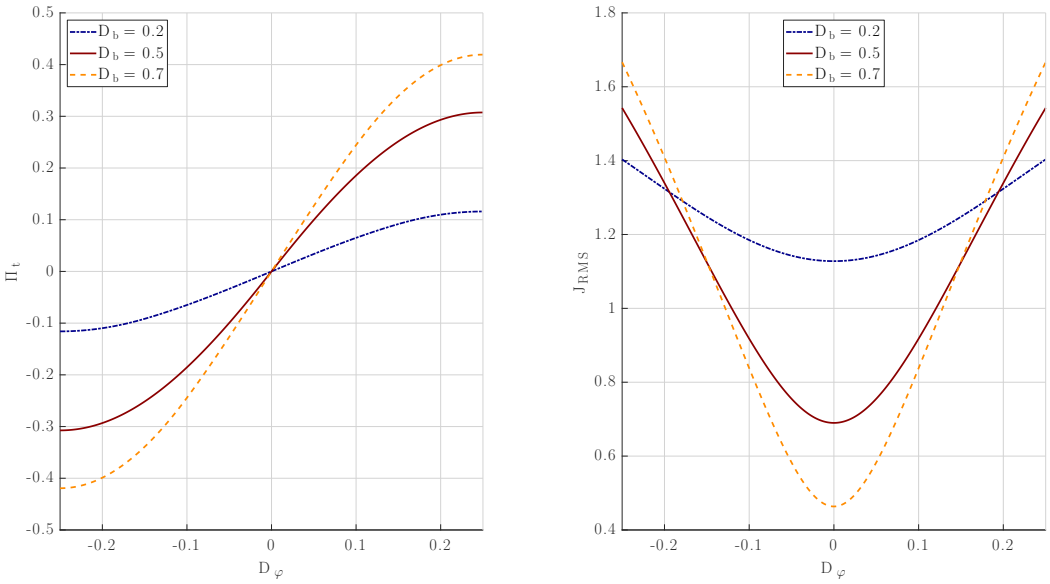


Figure 2.9: Normalized average power transfer and tank RMS current at 3 values of D_b as function of D_φ, at $D_h = 0.5$.

In Figure 2.9 is highlighted the behaviour of power and RMS current when D_b

is changed. Note that increasing the Boost cell duty-cycle increases transferred power, but also the maximum inductor RMS current.
However, higher values of D_b reduce the minimum RMS current value, thus potentially reducing conduction losses at light load.

2.2 ZVS turn-on analysis

In modern power electronics converters, a key way to improve efficiency is by guaranteeing Zero Voltage Switching (ZVS) at the turn-on of the switches.
ZVS is obtained when the current exiting (or entering) the switching node is of the correct sign and magnitude to properly charge or discharge the switch output capacitance in order to turn on the switch body diode (assuming MOSFET switches are used) during the dead-time. This eliminates the switching turn-on losses, thus improving efficiency.
To verify if the ZVS condition is met, the switches' turn-on current must be calculated. To do this, the inductor currents (both for L_{dc}, L_r and the transformer magnetizing inductance L_μ) can be assumed to be constant during the dead-time, since this time interval is significantly short compared to the switching period.
This assumption allows to use the equivalent circuits in Figure 2.10.

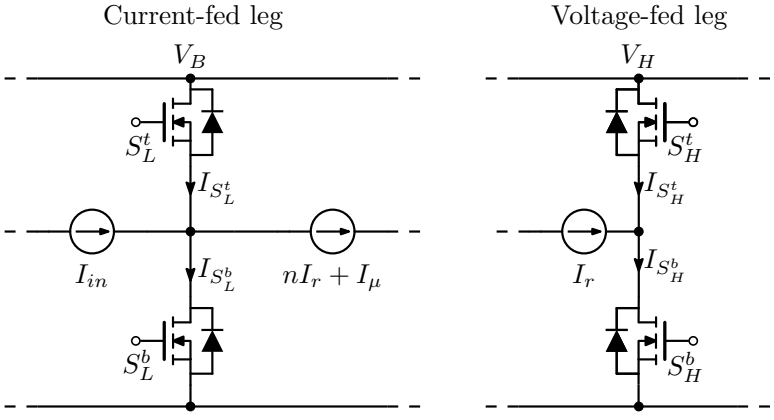


Figure 2.10: Equivalent circuits for switch current calculation

With the sign conventions of Figure 2.10, the ZVS conditions for the voltage-fed side switches are

$$\begin{cases} S_H^b \implies I_r(\tau_{S_H^b}) \leqslant -|I_{ZVS}| \\ S_H^t \implies I_r(\tau_{S_H^t}) \geqslant |I_{ZVS}| \end{cases} \tag{2.10}$$

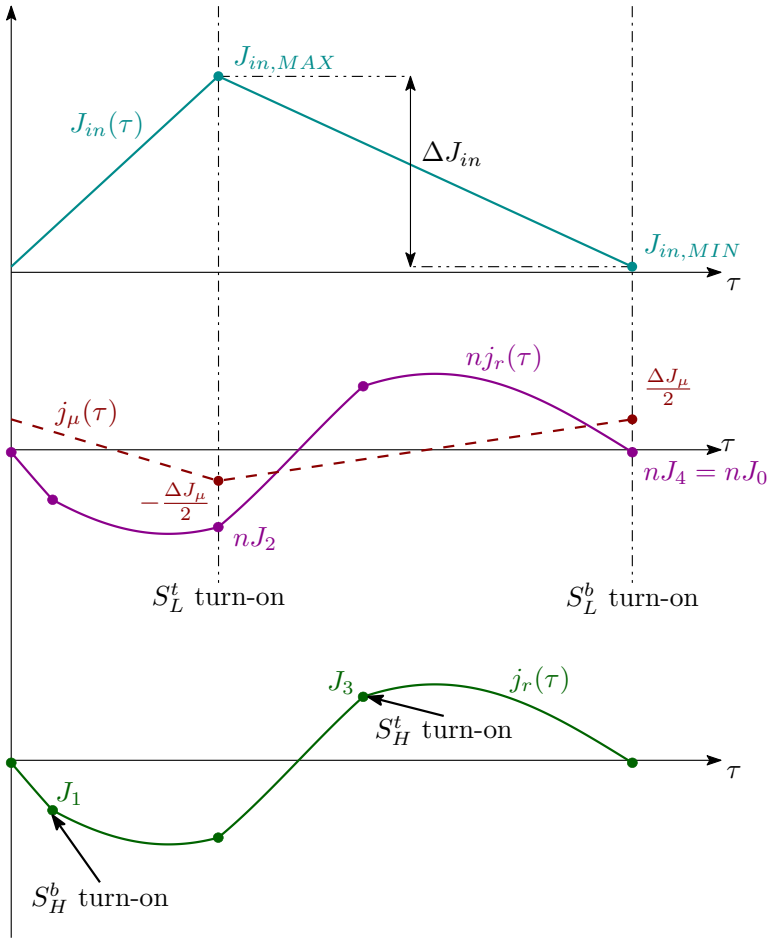


Figure 2.11: Example of the normalized current waveforms at the switches turn-on instants

where $\tau_{S_H^b}$ and $\tau_{S_H^t}$ are the switches' turn-on instants. I_{ZVS} is the current needed to discharge (or charge) the switch capacitance in the given dead-time, and depends on the selected device.

For the current-fed side, the input and magnetizing current must also be considered. This gives the following conditions

$$\begin{cases} S_L^b \Longrightarrow I_{in}(0) - nI_r(0) - I_\mu(0) \leqslant -|I_{ZVS}| \\ S_L^t \Longrightarrow I_{in}(D_bT_s) - nI_r(D_bT_s) - I_\mu(D_bT_s) \geqslant |I_{ZVS}| \end{cases} \tag{2.11}$$

where $I_{in}(0) = I_{IN,MIN}$ and $I_{in}(D_bT_s) = I_{IN,MAX}$ depend on the load, whereas $I_\mu(0) = I_{\mu,MAX}$ and $I_\mu(D_bT_s) = I_{\mu,MIN}$ are independent on load conditions.

Assuming unitary efficiency, the average normalized current through inductor L_{dc} is

$$J_{IN} = \frac{\Pi_t}{U_L}. \tag{2.12}$$

The input inductor's current ripple can be calculated (in normalized form) as follows:

$$\Delta I_{in} = D_b \frac{V_L}{L_{dc} f_{sw}} \Longrightarrow \Delta J_{in} = \frac{D_b}{f_{sw}} U_L \frac{Z_r}{L_{dc}} = 2\pi \frac{D_b}{f_n} U_L \lambda_{dc} \tag{2.13}$$

where $\lambda_{dc} = \frac{L_r}{L_{dc}}$ can become a design parameter based on ZVS range specifications.
Combining the results of (2.12) and (2.13), $I_{IN,MIN}$ and $I_{IN,MAX}$ can be easily calculated in normalized form as

$$\begin{cases} J_{in,MIN} = J_{IN} - \frac{\Delta J_{in}}{2} \\ J_{in,MAX} = J_{IN} + \frac{\Delta J_{in}}{2} \end{cases} \tag{2.14}$$

The same procedure can be applied on the magnetizing inductance. Considering that its average current is zero, the normalized current ripple on the magnetizing inductance L_μ is

$$\Delta J_\mu = \frac{D_b}{f_{sw}} U_L \frac{Z_r}{L_\mu} = 2\pi \frac{D_b}{f_n} U_L \lambda_\mu \text{ where } \lambda_\mu = \frac{L_r}{L_\mu} \tag{2.15}$$

so that the minimum and maximum value of the magnetizing current are given by

$$\begin{cases} J_{\mu,MIN} = -\frac{\Delta J_\mu}{2} \\ J_{\mu,MAX} = +\frac{\Delta J_\mu}{2} \end{cases} \tag{2.16}$$

The resonant current terms depend on the operating mode instead.
The conditions in the various operating regions are recapped in normalized form in Table 2.5 and 2.6.

Table 2.5: Normalized switch turn-on currents for the current-fed side devices

Mode	**M1**	**M2**	**M3**
S_L^b	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$
S_L^t	$J_{in,MAX} - nJ_3 + \frac{\Delta J_\mu}{2}$	$J_{in,MAX} - nJ_2 + \frac{\Delta J_\mu}{2}$	$J_{in,MAX} - nJ_3 + \frac{\Delta J_\mu}{2}$
Mode	**M4**	**M5**	**M6**
S_L^b	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$	$J_{in,MIN} - nJ_0 - \frac{\Delta J_\mu}{2}$
S_L^t	$J_{in,MAX} - nJ_1 + \frac{\Delta J_\mu}{2}$	$J_{in,MAX} - nJ_2 + \frac{\Delta J_\mu}{2}$	$J_{in,MAX} - nJ_1 + \frac{\Delta J_\mu}{2}$

Table 2.6: Normalized switch turn-on currents for the voltage-fed side devices

Mode	M1	M2	M3	M4	M5	M6
S_H^b	J_1	J_1	J_2	J_2	J_3	J_3
S_H^t	J_2	J_3	J_1	J_3	J_1	J_2

As it can be seen, both the magnetizing inductance and input inductor can help the ZVS conditions of the CF-side devices with their current ripple, while the average input current opposes ZVS of S_L^b during forward power transfer while aiding soft-switching of S_L^t (the opposite happens during reverse power transfer). Since the switches' turn-on currents are heavily influenced by the converter parameters and control strategy, a reliable analysis of the ZVS ranges is not feasible beforehand. More considerations regarding ZVS will be made in chapter 4.

2.3 Below-resonance operation

The relative value of switching and resonant frequency influences the tank waveforms.
In particular, the effects of having $f_{sw} < f_r$ are explored in this section.
An example of the main converter waveforms is reported in Figure 2.12.

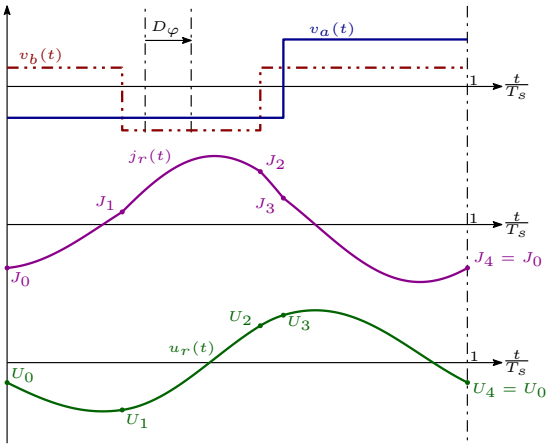


Figure 2.12: Example waveforms for $f_{sw} = 0.9 f_r$ in mode M1

Note that the energy balances are unchanged because no asynchronous device (e.g. diode bridges) are present in the converter, leading to the absence of discontinuous modes. This means that the capacitive legs voltages, the normalized sub-interval

durations and the operating modes boundaries remain the same, regardless of the switching frequency.
An effect of operating below the resonant frequency is the reversal of the power flow, as shown in Figure 2.13.

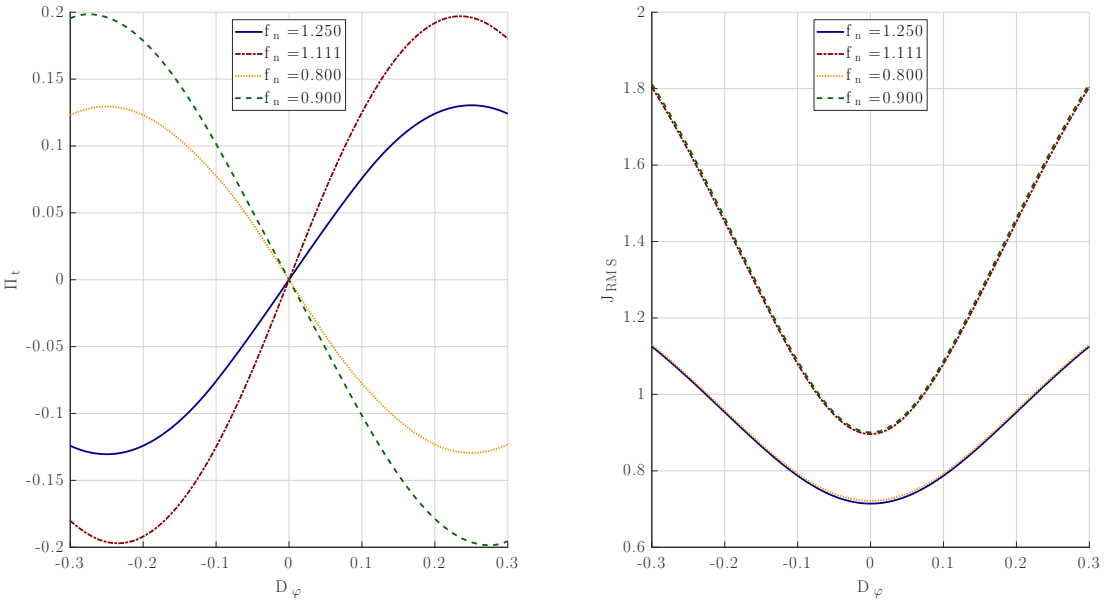


Figure 2.13: Comparison of average normalized power and inductor normalized RMS current as function of D_φ. $f_n < 1$ refers to below-resonance operation, while $f_n > 1$ refers to the above-resonance case. $D_h = 0.5$ for $f_n = 1.25$ and $f_n = 0.8$ while $D_h = 0.25$ for $f_n = 1.111$ and $f_n = 0.9$.

The effect of D_h on the monotonicity interval is also reversed: lower values of D_h increase such interval. The RMS current behaviour with respect to D_φ is unchanged. When the same power is delivered, the inductor RMS current in the above and below resonance cases is identical. Getting closer to the tank resonant frequency increases both the delivered power and RMS current, as expected.
The switch turn-on instants remain the same as per the above-resonance case, so the conditions reported in Table 2.5 and 2.6 are the same but with different values of the currents. This will obviously influence the ZVS ranges, which will be further studied in chapter 4.

Chapter 3

Minimum current operation

The contour maps of Figure 2.7 and 2.8 suggest the existence of optimal trajectories to deliver every desired power level with minimal tank RMS current.
An approach based on [4] is developed in this chapter, to guarantee minimum current operation of the SR-CFDHB converter by employing the Minimum Current Trajectory (MCT). Subsequently, strategies to select the Boost cell duty-cycle are explored, to minimize the overall value of the tank RMS current. At the end, some considerations regarding the ZVS operation of the converter are made.

3.1 Derivation of the MCT

As anticipated, every normalized power level can be achieved with infinite combinations of D_b, D_h and D_φ.
Among such combinations, those that minimize the RMS tank current value define the MCT.
Choosing to work with a three-dimensional problem implies a constraint on one of the control variables. This approach chooses to keep D_b as constant when considering the regulation of the power transfer. This means that different MCTs will exist for different values of D_b. The Boost cell duty-cycle could nonetheless be used to compensate input voltage variations, and its choice is discussed in section 3.2.
Note also that the converter parameters (such as turns ratio, normalized frequency and input/output voltages) influence the power and current contours, thus leading to different MCTs. In this preliminary investigation those parameters are kept constant.
The derivation of the MCT thus can be expressed by the following constrained minimization problem, using (A.11) and (A.12) under the FHA approximation:

$$\min_{D_b=\tilde{D}_b, D_h\in[0.5,1], D_\varphi\in[0,0.25]} \{J_{RMS}(D_b, D_h, D_\varphi)\}$$
$$\begin{cases} \Pi_t(D_b, D_h, D_\varphi) = \tilde{\Pi}_t \\ -\Pi_{t,max} \leqslant \tilde{\Pi}_t \leqslant \Pi_{t,max} \end{cases} \tag{3.1}$$

By using an optimization tool such as the MatLab function *fmincon* for every power level in the desired range, the (D_h, D_φ) points describing the MCT can be found.

Note that a totally equivalent MCT can be found be using the complement of D_h.

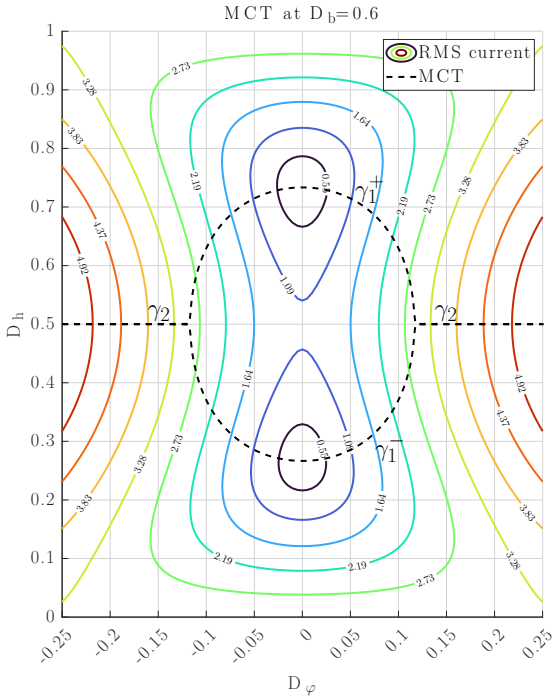


Figure 3.1: Normalized tank RMS current contours under the FHA together with the MCT

As it can be seen from Figure 3.1, the MCT consists of two branches:

- At low and medium load the γ_1 branch of the MCT avoids the regions of high RMS current
- At high load, branch γ_2 coincides with the standard phase shift modulation with $D_h = 0.5$

By fitting the (D_h, D_φ) points in the γ_1 branch as function of the normalized

power, one can obtain an expression for the control points.
Both $D_h(\Pi_t)$ and $D_\varphi(\Pi_t)$ are well approximated by a degree-six polynomial.
Real-time calculation of the MCT can be simplified by following the solution proposed in [4], leading to the formulation of the Piece-Wise Linear MCT (PWL-MCT).
The PWL-MCT consists of three segments:

1. A constant-D_h segment located at $D_h = D_{sat}$ at light load;
2. A linear segment $D_h = D_0 + mD_\varphi$ at intermediate load;
3. A constant D_h segment located at $D_h = 0.5$;

and is subsequently defined by the following parameters (shown in Figure 3.2):

- Light-load voltage-fed side duty cycle: $D_h = D_{sat}$;
- Transition point between $D_h = D_{sat}$ and linear segment: $D_\varphi = D_1$;
- Linear segment slope: m (the zero-phase intercept D_0 can be determined univocally with D_1 and m);
- Transition point between linear segment and $D_h = 0.5$ segment: $D_\varphi = D_2$.

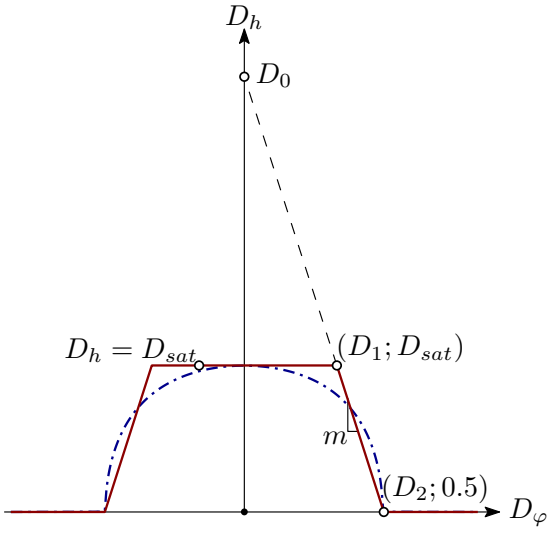


Figure 3.2: PWL-MCT and its parameters

These parameters can be determined by analysing the first numerical derivative of D_h with respect to D_φ along the MCT. Starting at light load, the MCT becomes almost constant, so D_{sat} can be chosen as the value of D_h at zero phase shift. When the first derivative falls under a certain value, chosen numerically to minimize the mean squared error (3.2), the first transition point can be found as the corresponding value of D_φ.
The second transition point, when the MCT transitions from the γ_1 to the γ_2 branch, is the first value of D_φ for which $\frac{\partial D_h}{\partial D_\varphi}$ becomes zero. This can be used to identify the second breakpoint D_2. The linear segment parameters are those who allow to join the (D_1, D_{sat}) and the $(D_2, 0.5)$ points.

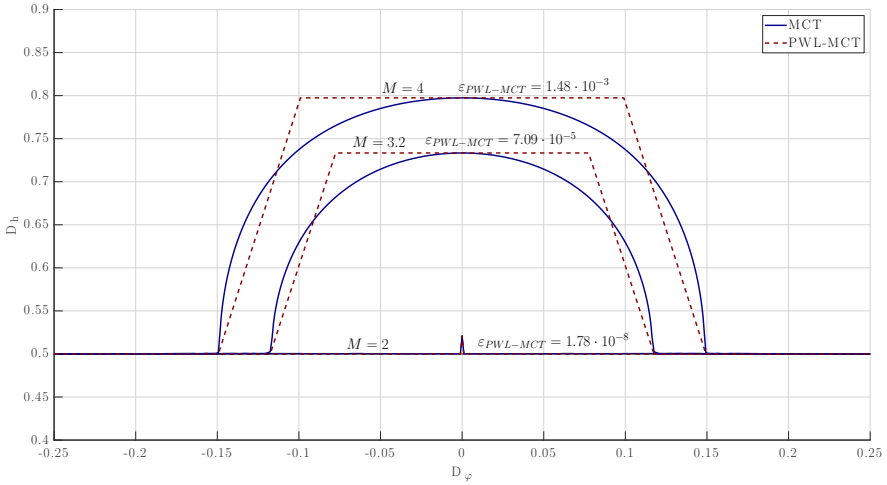


Figure 3.3: MCT and PWL-MCT at different voltage conversion ratios, with $n = 0.5$ and $D_b = 0.6$

Figure 3.3 shows the MCT and PWL-MCT trajectories at different M values and the corresponding mean squared errors, defined as

$$\varepsilon_{PWL-MCT} \triangleq \int_0^{0.25} |\gamma_{MCT}(D_\varphi) - \gamma_{PWL-MCT}(D_\varphi)|^2 \, dD_\varphi \tag{3.2}$$

Note that the PWL-MCT parameters are defined by the values of M and D_b, which can be known beforehand. This allows to calculate once and for all the parameters, greatly reducing the complexity of the required calculations when digitally controlling the converter.
Furthermore, expressions of the PWL-MCT parameters as function of M or D_b can be found by polynomial fitting, allowing easy, on-the-fly calculation of such parameters.

In conclusion, the PWL-MCT approximates quite well the real MCT, especially at low-load values, while greatly reducing the implementation complexity. Faster and simpler calculations also reduce the delay introduced by the control algorithm, thus improving the overall controllability of the converter. Furthermore, the possibility of obtaining expressions for all parameters of the PWL-MCT completely avoids the use of Look-Up Tables (LUT), thus greatly reducing the implementation complexity of the control algorithm.

3.2 Choice of the Boost cell duty-cycle

The control variable D_b influences many aspects of the converter, such as the maximum transferred power and the value and location of the minimum RMS current in the (D_φ, D_h) plain.
The choice of the value of the Boost cell duty-cycle thus heavily influences the converter operation.
In particular, this section explores two choice criteria:

1. Fixed Boost cell duty-cycle
2. Input voltage dependent D_b

3.2.1 Fixed Boost cell duty-cycle

This is the simplest approach to the selection of D_b. The reasoning at the foundation of this criterion is to ensure that the maximum current-fed side MOSFETs voltage stress doesn't reach unwanted levels.
In fact, the voltage stress on devices S_L^t and S_L^b is given by the Boost-cell voltage $V_B = V_1 + V_2 = \frac{V_L}{1-D_b}$, and thus related to its duty-cycle.
Knowing the input voltage range $V_L \in [V_{L,min}\ V_{L,max}]$, the minimum value of the Boost cell duty-cycle is simply

$$D_{b,min} = \frac{V_B - V_{L,max}}{V_B} \tag{3.3}$$

If V_B is constrained to be the desired maximum voltage stress on the current-fed side devices $V_{sw,L}^{max}$, the value of D_b can be chosen as

$$D_{b,min} = \frac{V_{sw,L}^{max} - V_{L,max}}{V_{sw,L}^{max}} \tag{3.4}$$

This simple approach allows to keep D_b constant throughout the whole operation range, but note that this does not imply that input and output voltage sensing

is not required.
In fact, the MCT depends on M, so to operate at minimum RMS current both voltages must be known.
Another disadvantage of this approach is that the maximum transferable power can vary in quite a wide range when V_L changes (Figure 3.5), potentially leading to over-speccing of some components.

3.2.2 Input voltage dependent Boost cell duty-cycle

This approach consists in keeping the Boost cell output voltage ($V_B = V_1 + V_2$) constant for every value of the input voltage. If its value reflected to the secondary side of the transformer is chosen to be equal to V_H, the following formulation for the Boost cell duty-cycle is given

$$nV_B = V_H \Longrightarrow D_b = 1 - n\frac{V_L}{V_H}. \tag{3.5}$$

The lower bound of D_b can still be calculated with (3.4), but with a possibly different value of $V_{sw,L}^{max}$. Since the switch voltage stress is kept constant by this selection strategy, it can become a design variable to obtain a more advantageous converter behaviour. A good choice could be to decide the switch voltage stress in such a way to have $D_b = 0.5$ at the middle point of the input voltage range. This way the values of D_b are symmetric with respect to its value at this middle point. This gives the following constraint on the current-fed side switches voltage stress:

$$V_{sw,L}^{MAX} = 2\left(\frac{V_{L,max} - V_{L,min}}{2} + V_{L,min}\right) = V_{L,max} + V_{L,min}. \tag{3.6}$$

This constraint still needs to be within a safety margin of the switch voltage rating to avoid damaging the devices, so consideration depending on the application must be made when designing the converter.
Since D_b changes with the input voltage, a constraint on the transformer's turns ratio is also necessary. Keeping $nV_B = V_H$ gives the following equation

$$M' = \frac{V_H}{nV_B} = \frac{1}{n}(1 - D_b)\frac{V_H}{V_L} = 1. \tag{3.7}$$

Ensuring that 3.7 is verified for the whole V_L range gives the following constraint on n

$$n = (1 - D_{b,min})\frac{V_H}{V_{L,max}}. \tag{3.8}$$

The advantage of this approach is that the minimum tank RMS current at zero power is zero for the entire V_L range, as shown in plot b) of Figure 3.6. The value of D_h that corresponds to the minimum value of J_{RMS} is equal to D_b, which is the same condition for a flat-top inductor current in the non-resonant CFDHB. The flat-top condition refers to a choice of duty cycles that, in the non-resonant CF-DHB, results in the inductor voltage being zero during some intervals. During those intervals, the inductor current will be constant. If the duty cycles are chosen as $D_h = D_b = D = 1 - n\frac{V_L}{V_H}$, the inductor current will have a trapezoidal shape, hence the name flat-top.
In the SR-CFDHB the current won't be constant during the intervals in which $v_Z(t) = 0$, as shown in Figure 3.4. Nonetheless, the choice $D_h = D_b = 1 - n\frac{V_L}{V_H}$ will still be referred to as the flat-top condition.

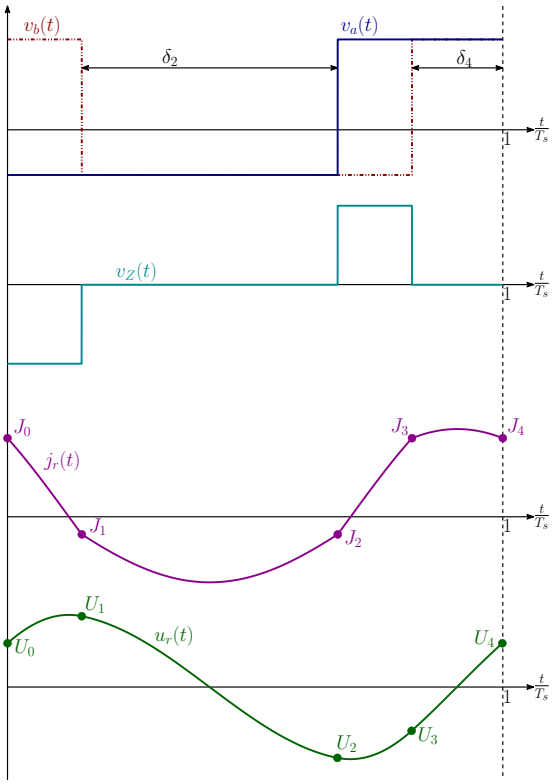


Figure 3.4: Example theoretical waveforms in the Flat-Top condition $D_b = D_h = 1 - n\frac{V_L}{V_H}$. During δ_2 and δ_4, $v_a = v_b$ and thus $v_Z = 0$

With a MCT control strategy, the flat-top condition is achieved only at zero power transfer, while with the PWL-MCT this condition is ensured for $-D1 \leqslant D_\varphi \leqslant D_1$, where D_h is kept constant and equal to its value at the zero power-minimum

current point, which coincides with ($D_h = D_b = 1 - n\frac{V_L}{V_H}$; $D_\varphi = 0$). A comparison between the two methods is provided in the next subsection, together with some considerations regarding the value of f_n.

3.2.3 Comparison between the choices of the current-fed side duty cycle

A comparison between the two choices of D_b is presented in this subsection. The relevant parameters of the converter used for the following plots are:

- Output voltage: $V_H = 400\ V$ (kept fixed at this value for all plots)
- Input voltage range: $V_L \in [250\ V; 500\ V]$
- Maximum Boost voltage: $V_{B,max} = 750\ V$
- Transformer turns ratio (from 3.8): $n = 0.53$

In Figure 3.5 and 3.6, some plots are presented to allow more clear comparison between the two choices.

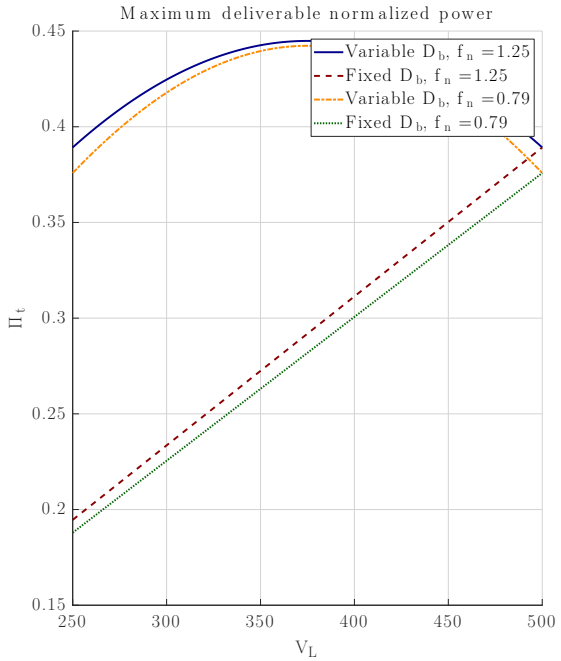


Figure 3.5: Maximum normalized power as function of V_L, at two different values of f_n. The control parameters are $D_h = 0.5$ and $D_\varphi = 0.25$, which give the maximum possible transferred power at every given V_L.

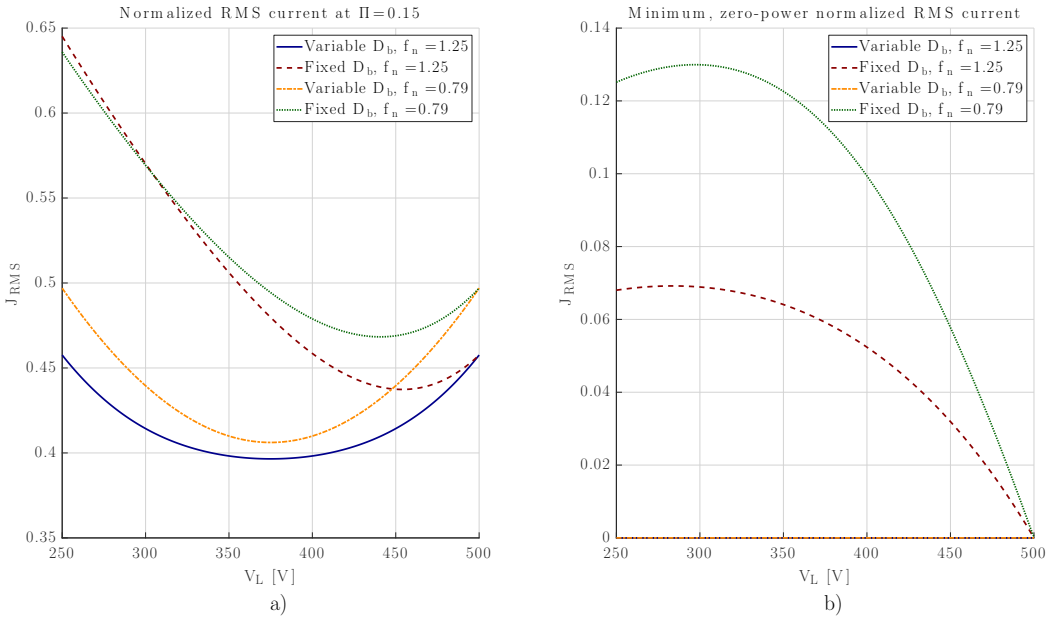


Figure 3.6: **a)** Maximum normalized RMS current at $\Pi_t = 0.15$ as function of V_L, at two different values of f_n. D_h is kept at 0.5 while D_φ is calculated to have $\Pi_t = 0.15$.
b) Minimum zero-power normalized current as function of V_L, at two different values of f_n.

As predicted in the preliminary analysis,the maximum deliverable power is higher with the variable D_b, which always gives higher CF side duty-cycle values.
With the variable D_b choice, however, the minimum RMS current at zero power is always lower (in fact, as can be seen from plot b) of Figure 3.6,it is zero) than the one resulting from the fixed D_b value given by 3.4.
Furthermore, if the V_L-dependent modulation of D_b is combined with a MCT control strategy, the tank RMS current is always the minimum possible at every power level, so that conduction losses are mitigated.
Another advantage brought by the variable D_b is that the maximum power transfer is less influenced by the input voltage variation, thus allowing a more tailored design of the converter components.
If the transferred power is fixed, the variable D_b strategy gives lower maximum inductor RMS current than the fixed D_b choice, as shown in plot a) of Figure 3.6.
In conclusion, a combination of the input voltage dependent D_b and the PWL-MCT could allow a relatively easy, resource-efficient way to achieve minimum current operation of the SR-CFDHB converter.

Chapter 4

ZVS considerations

ZVS turn-on is fundamental to achieve high efficiency operation of the converter. The selection of the values of f_n and of the duty-cycles (through the chosen control strategy) heavily influences the switches ZVS turn-on range.
Due to the topology, an accurate study of the ZVS turn-on range is not possible for all the switches without previously designing the converter. In fact, from (2.11), it is clear that the input inductor and magnetizing current heavily affect the current-fed side switches ZVS range. The voltage-fed side switches' ZVS range, instead, is not dependent on the input inductor current.
The following ZVS analysis considers only the sign of the tank current at the switches' turn-on instants, thus allowing a more general study.
However, the presented plots are still relevant only for the example case, which is still the one considered in subsection 3.2.2.

4.1 ZVS turn-on along the PWL-MCT

Since the PWL-MCT and the switches' turn-on current change radically with the input voltage (and consequently D_b, with the chosen control strategy), different values of V_L will lead to different ZVS ranges.
Concerning the voltage-fed side, it can be seen that ZVS for all load levels could be achieved by simply lowering the value of the D_{sat} parameter of the PWL-MCT. The situation for the current-fed side is, however, more complex due to the influence of the input and magnetizing current on the switches' turn-on current. At forward power transfer, $I_{in,MAX}$ is positive, thus helping the zero-voltage turn-on of S_L^t, as shown in (2.11). However, if the input current ripple is not big enough to make $I_{in,MIN} \leqslant 0$, the input current opposes ZVS at the turn-on of S_L^b. The opposite happens at reverse power transfer, when the average input

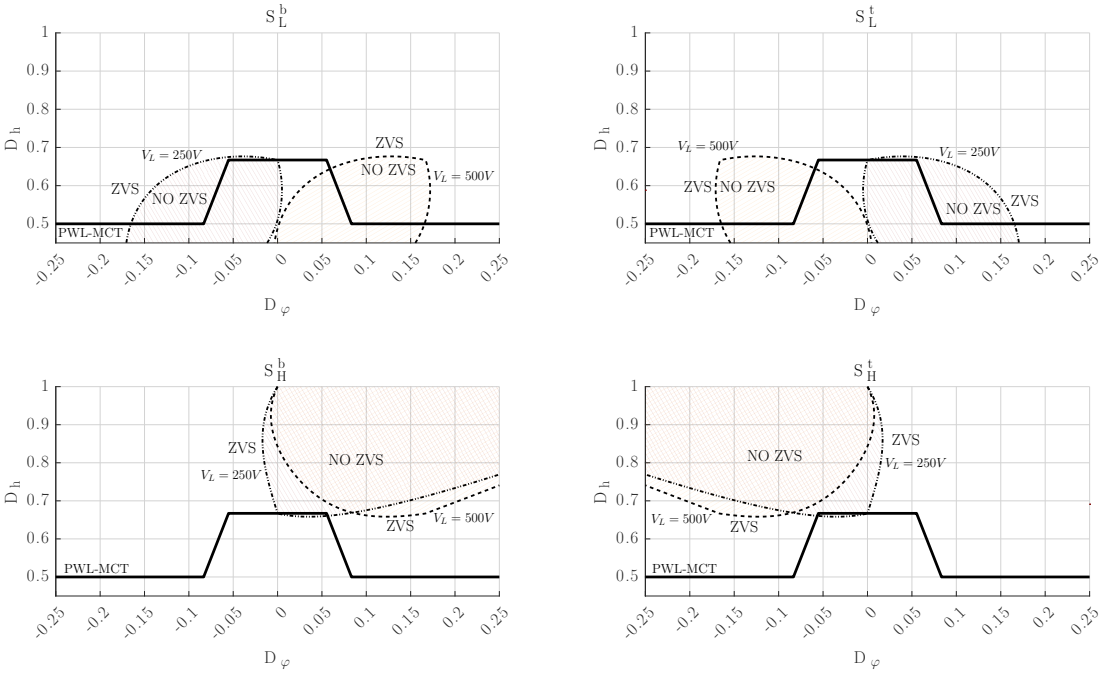


Figure 4.1: Approximated ZVS ranges with the PWL-MCT and input voltage-dependent D_b, at $V_L = 250V$ and $V_L = 500V$. Only the sign of the tank current at the turn-on instant is considered.

current becomes negative, making $I_{in,MIN}$ always negative and $I_{in,MAX}$ positive only if the current ripple is big enough.

Combining this with the plots of Figure 4.1, it can be deduced that the ZVS range of both S_L^t and S_L^b is increased for $V_L = 250$ V, while the situation is worsened at $V_L = 500$ V. In fact, the areas where ZVS is not achieved by the resonant current alone at $V_L = 250$ V are in operating points in which the input current helps achieve ZVS. The opposite happens instead at $V_L = 500$ V, where ZVS of S_L^b is not achieved at forward power transfer and at reverse power transfer for S_L^t, where it is further opposed by the input current.

ZVS of the CF-side devices can thus be helped by a huge input current ripple or by exploiting the transformer magnetizing inductance, which always helps ZVS in every load condition (as can be seen from (4.1) and Figure 2.11).

Figure 4.2, instead, shows a particular case when $D_b = 0.5$. In this condition, the PWL-MCT becomes a pure phase-shift modulation and the ZVS ranges appear to be optimal. However, this happens because only the sign of the resonant current has been considered as the ZVS condition. If the input current is taken into account and the current necessary to obtain ZVS is non-zero, areas where ZVS is not achieved are inevitable, especially for the VF-side devices, which rely on the resonant current alone to achieve ZVS.

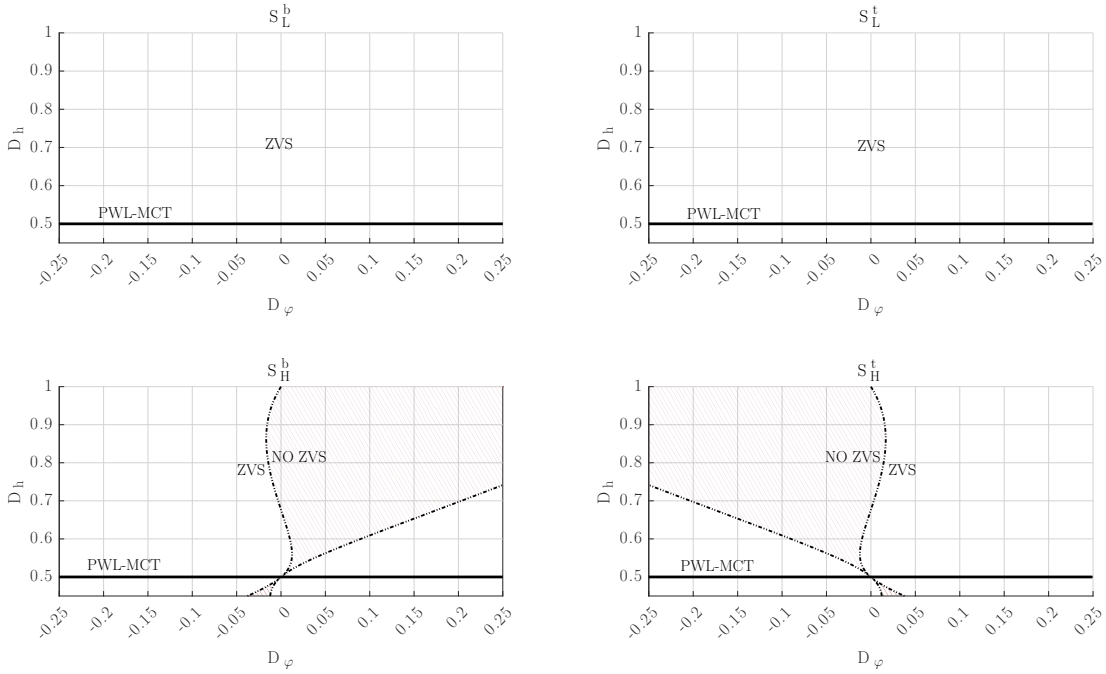


Figure 4.2: Approximated ZVS ranges with the PWL-MCT and input voltage-dependent D_b at $V_L = 375V$. Only the sign of the tank current at the turn-on instant is considered.

4.2 Influence of the switching frequency

In the previous section, the ZVS ranges have been studied considering the value of f_n as constant. The value of the switching frequency could be changed during operation, if it leads to increased ZVS ranges.
Figure 4.3 shows a plot of the approximated switch turn-on currents at different values of f_n.

Unfortunately, the ZVS capabilities of the converter are not aided by modulating the switching frequency.
The main problem is that operation at $f_n < 1$ also reverses the sign of the power flow with respect to D_φ.
Consider S_L^b. At $f_n > 1$, ZVS is lost mainly at reverse power flow ($D_\varphi < 0$). To achieve ZVS, the switching frequency could be changed to have $f_n < 1$. However, the resulting equivalent operating point (in terms of transferred power) still undergoes hard switching. Similar considerations can be made also for the other switches.
This near duality of the switches current sign with respect to f_n is extensible to all the considered input voltage levels.
Also from Figure 4.3, when in the above-resonance case getting further away

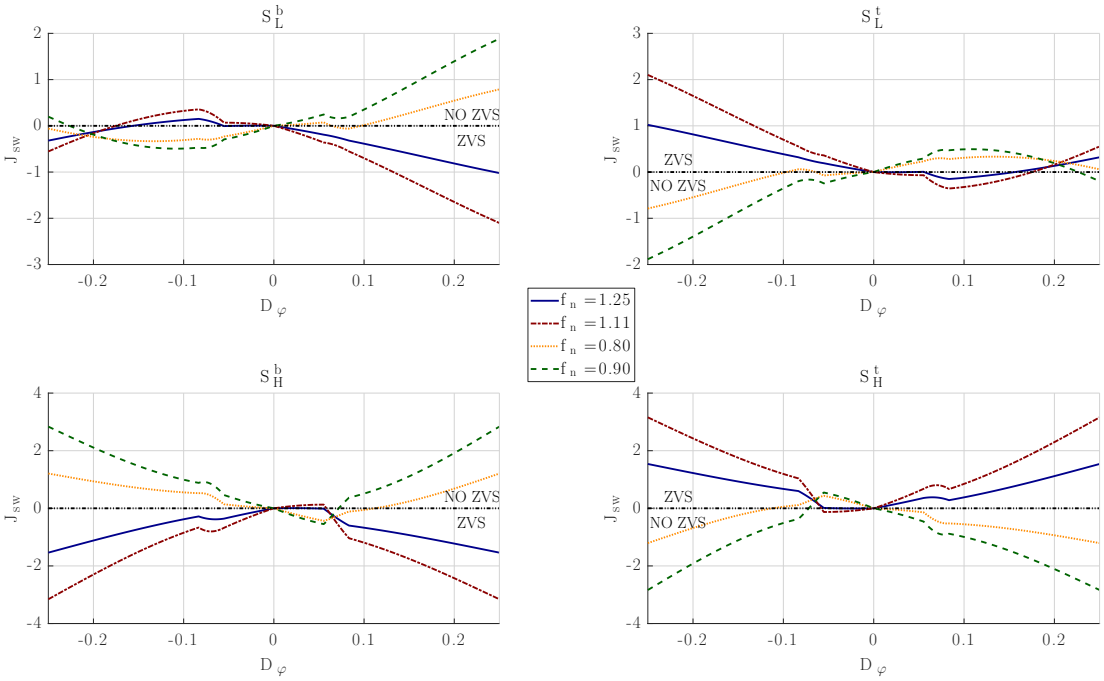


Figure 4.3: Switching nodes currents at the switch turn-on along the PWL-MCT at $V_L = 250V$. $f_n > 1$ means that the switching frequency is greater than the tank resonant frequency. Only the sign of the tank current at the turn-on instant is considered

from the resonant frequency (so having higher f_n) yields higher ZVS ranges, when considering only the resonant current at the switching instants. The same happens win the below-resonance case, where lower values of f_n (and thus when the switching frequency is further away from the resonant frequency) bring better ZVS ranges.

By looking at the two bottom plots of Figure 4.3, where S_H^b and S_H^t are considered, it can be seen that the ZVS range when working below resonance is very limited, when compared with the one obtained in the above-resonance case.

With the proper considerations, changing the value of the switching frequency does not appear to be an effective way to increase the ZVS range.

4.3 Modified PWL-MCT

A way to increase the ZVS range of the voltage-fed side switches could be to simply lower the value of the PWL-MCT parameter D_{sat}. This, in turn, would inevitably increase the inductor RMS current along the trajectory, but this disadvantage is trumped by the increased ZVS range, which brings much more benefits.

The modification is straight forward: instead of choosing D_{sat} as the value of D_h obtained from the MCT at zero power, it can be chosen numerically to guaran-

tee ZVS of the VF-side switches. The proposed method consists in iteratively reducing the value of D_{sat} and verifying if the resulting Modified PWL-MCT (M-PWL-MCT) satisfies the ZVS condition for the VF-side switches. D_{sat} is lowered by the smallest amount possible, in order to mitigate the RMS current increase. Figure 4.4 shows a comparison between the two trajectories, highlighting the lower D_{sat} value.

The main advantage of this control trajectory is shown in Figure 4.5, where the ZVS condition for the VF-side switches is now met with the M-PWL-MCT, where the PWL-MCT didn't allow soft-switching of these devices. The M-PWL-MCT has lower D_{sat} value, so the ZVS process of the CF-side switches can be hindered, but this can be countered by proper component design.

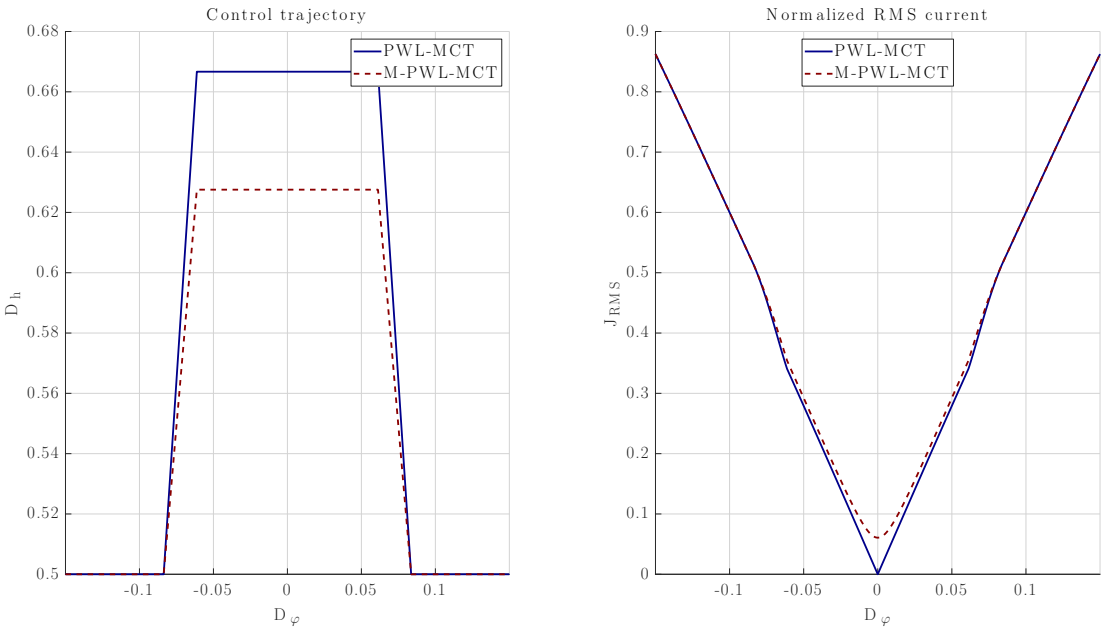


Figure 4.4: Comparison between the PWL-MCT and M-PWL-MCT at $V_L = 250\ V$, $f_n = 1.25$. The normalized ZVS current is $J_{ZVS} = 0.1$ as an example to highlight the differences.

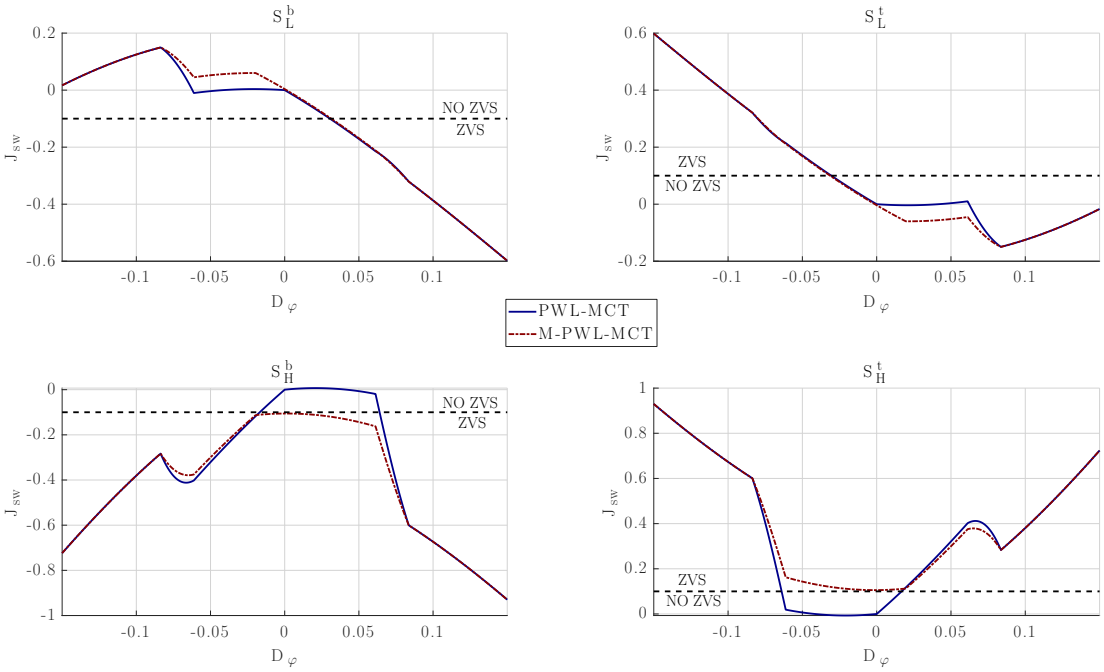


Figure 4.5: Approximated switch currents along the M-PWL-MCT at $V_L = 250\ V$, $f_n = 1.25$. The normalized ZVS current is $J_{ZVS} = 0.1$ as an example to highlight the differences. Only the tank current at the turn-on instant is considered.

Chapter 5

Design guidelines

In this chapter, the values of the converter's components are going to be chosen, in order to build a prototype with the following specifications:

Table 5.1: Prototype specifications

Parameter	Value
Current-fed side voltage (V_L)	250-500 V
Voltage-fed side voltage (V_H)	400 V
Nominal output power ($P_{o,nom}$)	2.5 kW
Switching frequency (f_{sw})	200 kHz

The components are selected in such a way to accommodate the M-PWL-MCT control strategy with the input voltage dependent D_b and guarantee ZVS in the widest possible range of input voltage and output power.

5.1 Turns ratio

The turns ratio can be selected from (3.8), once the maximum CF-side voltage stress is known. Using (3.6) gives $V_{sw}^{MAX} = 750\ V$. This allows to use 1200 V devices within a 25% range of their voltage rating, thus increasing the converter reliability.
By using (3.4), the CF-side duty cycle ranges from 0.33 at $V_L = 500\ V$ to 0.67 at $V_L = 250\ V$. the transformer turns ratio is subsequently given by

$$n = (1 - D_{b,min})\frac{V_H}{V_{L,max}} = 0.533.$$

5.2 Resonant tank parameters

The selection of the resonant tank parameters starts with deciding the value of the resonant frequency. The range for the normalized switching frequency is assumed to be $1.05 \leqslant f_n \leqslant 1.25$ [4]. From the previous study it is clear that values at the top of this range give better ZVS performance, so the value $f_n = 1.25$ is selected. With this choice of f_n, the tank has a resonant frequency specification of

$$f_r = \frac{f_{sw}}{f_n} = 160\ kHz \tag{5.1}$$

To obtain the values for the tank components, another equation is needed. The proposed approach chooses to design the inductor based on the nominal output power specification. Using the FHA (and thus (A.8)) and choosing $D_b = 1 - n\frac{V_L}{V_H}$, an expression for the energy transfer inductor is:

$$L_r = \frac{V_H^2}{\pi^3 P_{o,nom} f_{sw}} \frac{f_n^2}{f_n^2 - 1} |sin(\pi D_b)||sin(\pi D_h)|sin(2\pi D_\varphi). \tag{5.2}$$

To evaluate this expression, an operating point at which the nominal power delivery is ensured must be decided.

Since D_b is 0.5 at the middle-point of the input voltage range ($V_L = 375\ V$), the maximum output power delivery capabilities are at this voltage value. The worst-case scenario is indifferently at minimum or maximum input voltage. Let's select $V_L = 250\ V$ and thus $D_b = 0.67$. The other parameters to be decided are the VF-side duty cycle and phase shift at which the nominal power is delivered: $(D_\varphi^{MP}, D_h^{MP})$.

Operating in a region of the M-PWL-MCT where $D_h = 0.5$ ensures the maximum range where power control is maintained, so D_φ^{MP} can be chosen in the range $D_{2,V_{L,min}} \leqslant D_\varphi^{MP} \leqslant 0.25$, where $D_{2,V_{L,min}}$ is the value of the D_2 parameter of the M-PWL-MCT when $V_L = 250\ V$. The static gain of the power characteristic (namely $\frac{\partial P}{\partial D_\varphi}$) is lower when getting closer to $D_\varphi = 0.25$, while operating with lower values of D_φ gives more power control gain. However, the controller implementation must also be considered.

If the converter is digitally controlled by a microcontroller, the timers' resolution is a limiting factor when modulating the phase shift. Choosing a value of D_φ^{MP} which is too low has the effect of introducing limit cycles in the power control, because the timer of the microcontroller will not have the necessary resolution to provide the proper phase shift values when regulating the output power. With these consideration made, the chosen operating point is ($D_\varphi^{MP} = 0.15, D_h^{MP} =$

0.5) as a trade-off between control gain and implementability.
With this choice, the value of L_r can be calculated from (5.2) and the resonant capacitance value can be determined from the following equation. The obtained values are $L_r = 20\ \mu H$ and $C_r = 50\ nF$.

$$C_r = \frac{1}{(2\pi f_r)^2 L_r}. \tag{5.3}$$

With this tank parameters, the nominal output power, calculated from the theoretical waveforms, at $V_L = 250\ V$ and $500\ V$ is 2.5 kW, as expected. The phase shift necessary to reach nominal power is 0.15 at $V_L = 250\ V$ and $500\ V$ and, as expected, is lower when V_L gets closer to 375 V, where $D_b = 0.5$ and the maximum transferable power is achieved.

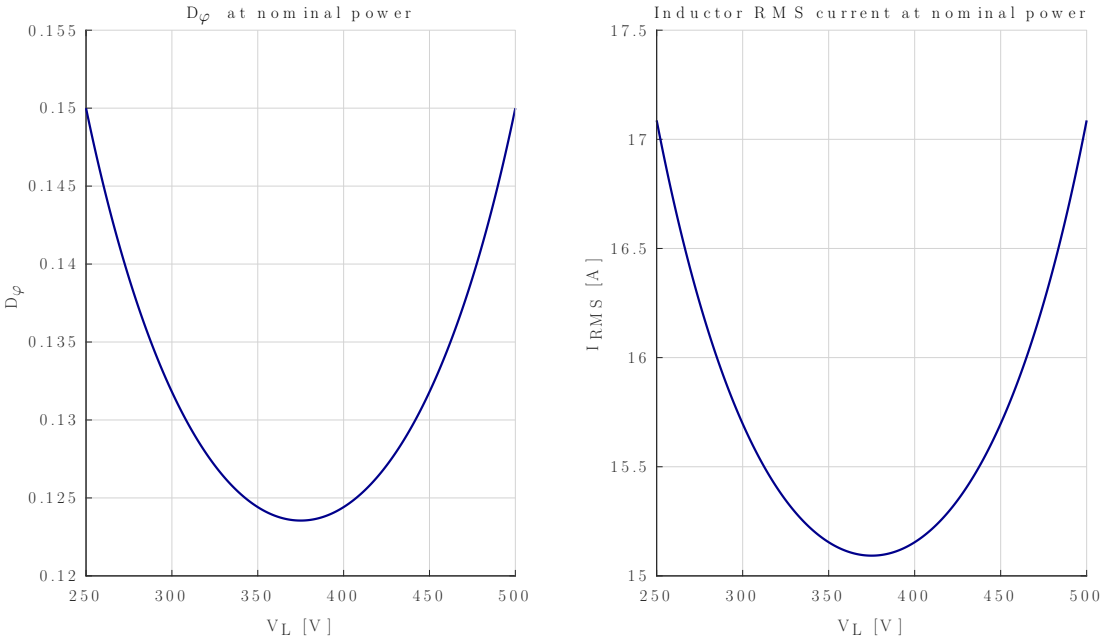


Figure 5.1: Phase shift D_φ and RMS inductor current at nominal power at different values of the input voltage range.

From Figure 5.1, the maximum inductor RMS current at nominal load results to be 17.08 A at minimum and maximum input voltage.

5.3 ZVS conditions

The input inductor L_{dc} and the transformer magnetizing inductance will be designed to obtain the maximum ZVS range possible of the CF-side devices. To do this, a condition to obtain ZVS must be defined.

Consider the circuit shown in Figure 5.2. During the dead-time between the switches commands the current at the switching node can be considered constant. This current will divide between the two parasitic output capacitances. If the current is of the right sign and magnitude, the voltage across the C_{oss} capacitor of the switch that will turn on will reach zero during the dead-time, thus turning on the body diode and ensuring ZVS turn-on of the switch.

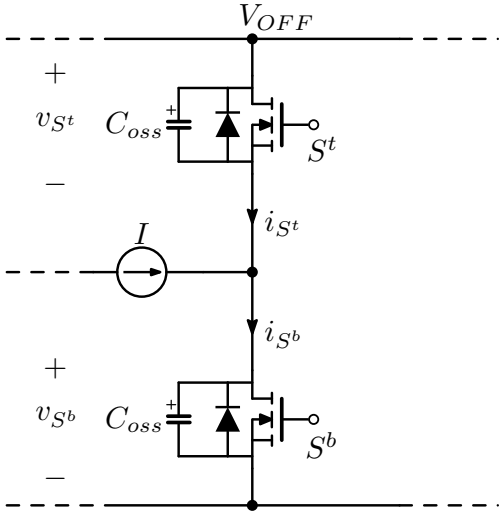


Figure 5.2: Switching leg circuit during the dead-time

To determine the necessary current, an equivalent capacitance is needed to represent C_{oss}. In fact, like other parasitic capacitances, the output capacitance is strongly non-linear with respect to the MOSFET Drain-Source voltage. Thus, the charge-equivalent capacitance [5] is defined as follows

$$C_{Q,eq}(V_{DS}) = \frac{\int_0^{V_{DS}} C_{oss}(v)dv}{V_{DS}} \tag{5.4}$$

The selected MOSFETs are the GeneSiC **G3R3MT12K** for all four devices. These are 1200V SiC MOSFETs, with $R_{DS,on} = 30\ m\Omega$ and a current rating of $I_D = 63\ A$ at 100 °C.

Figure 5.3 shows plots of $C_{oss}(V_{DS})$ and the area corresponding to the calculation of the charge-equivalent capacitance. The CF switches have a constant V_{OFF} of 750 V, while the VF side switches have a V_{OFF} of 400 V. Evaluation of (5.4) for the two cases gives the following charge-equivalent capacitance values:

$$C_{CF} = C_{Q,eq}^{CF}(750V) = 130.97\ pF$$

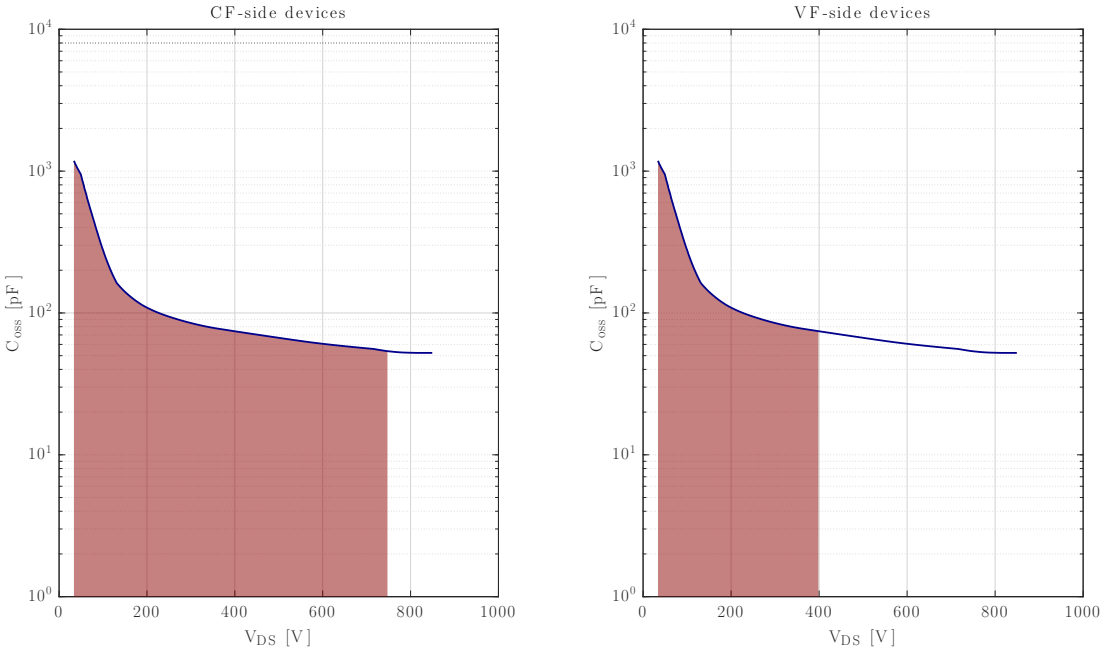


Figure 5.3: $C_{oss}(V_{DS})$ plots for the CF and VF devices

$$C_{VF} = C^{VF}_{Q,eq}(400V) = 190.65\ pF$$

To finally evaluate the ZVS current, a simplified behaviour (shown in Figure 5.4) is considered.

Note that, in reality, the current does not divide equally between the two output capacitances. In fact, from Figure 5.3, even if the two devices on the leg are identical, the output capacitance changes its value dramatically during the dead-time. Consider, for example, the turn-on process of S^b. Being charged to V_{OFF}, its output capacitance is nearly 100 lower than the one of the top device, which is at nearly zero volts. This means that the current will flow mostly through the C_{oss} of S^t, rapidly charging its output capacitance. When the two capacitance values (and thus their voltages) become similar, the current will divide equally between the two devices. The current considered in Figure 5.4 can be though as a charge-equivalent current, which is the current necessary to move the charge contained in the two output capacitances.

With the considered hypothesis, during t_1, the switch output capacitance is discharged by a constant current. When v_{S^b} reaches $-V_R$ the body diode turns on, clamping the voltage until the dead-time has elapsed. Then the switch turns on at very low voltage. During $0 \leqslant t \leqslant t_{dead}$ both voltage and current are non-zero, implying that some power is transferred. During t_1 power is recovered to the

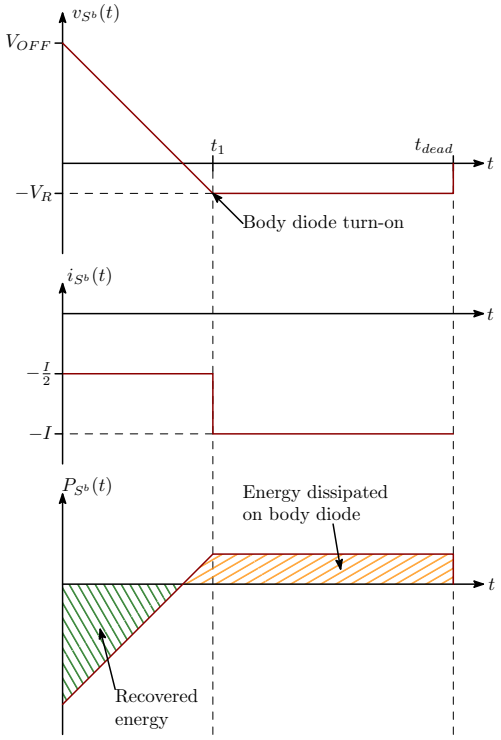


Figure 5.4: Simplified waveforms during the dead-time between the turn-off of S^t and the turn-on of S^b

source, since no device is on. During $t_1 \leqslant t \leqslant t_{dead}$, while the body diode is on, the power P_D is instead dissipated on the device.
The dissipated power can be estimated with the following expression

$$P_D \cong f_{sw}|I|V_R(t_{dead} - t_1) \tag{5.5}$$

while t_1 can be calculated (neglecting V_R, since it's much lower that V_{OFF}) from the charge that is transferred during the $0 \leqslant t \leqslant t_1$ interval, giving

$$t_1 \cong \frac{2C_{Q,eq}V_{OFF}}{|I|}. \tag{5.6}$$

Using (5.5) and (5.6), the following bounds on the dead-time can be defined:

$$t_1 \leqslant t_{dead} \leqslant \frac{P_D}{f_{sw}|I|V_R} + t_1 \tag{5.7}$$

P_D is decided to be 1.25 W, to keep the upper value of the dead-time range below 200 ns, and thus reducing its influence on the current waveforms when low phase shift values are used. The value of $|I|$ is considered to be the minimum of the absolute value of switch turn-on currents at nominal power, as shown in

Figure 5.5. For the VF-side switches I is the tank current at the turn-on instant. For the CF-side switches, instead, only the tank current (reflected to the primary side) at the turn-on instant is considered, because the values of the input and magnetizing current ripple are not known.

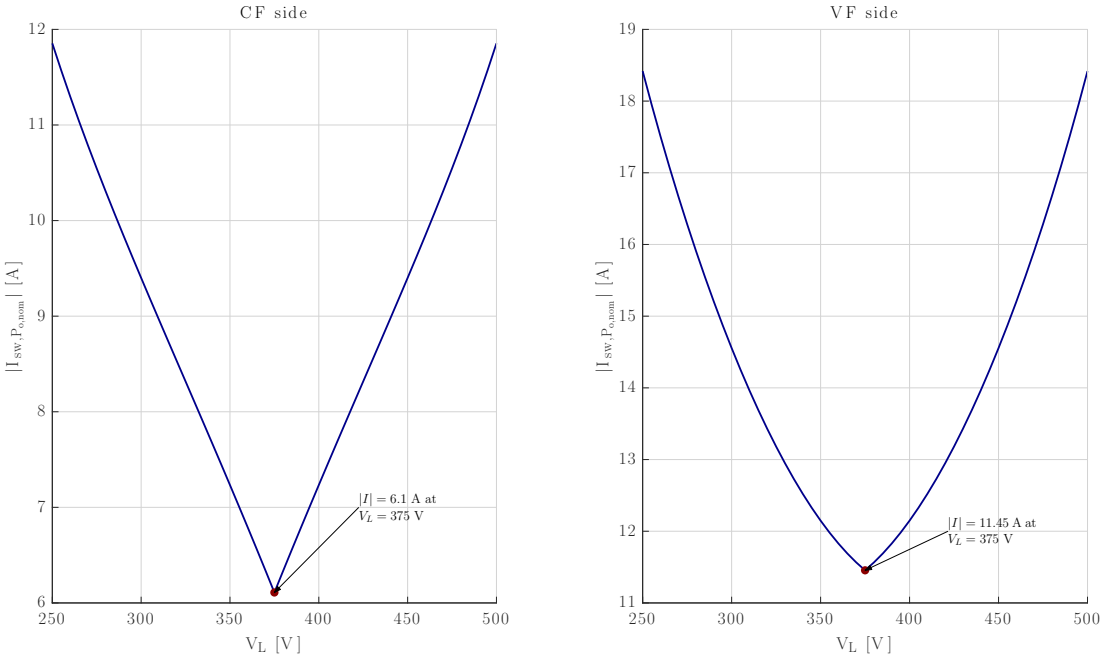


Figure 5.5: Absolute value of the switches turn-on currents at nominal power, considering only the resonant current.

Choosing $|I|$ to be the minimum current value (Figure 5.5), the value of $|I|$ is 6.1 A for the CF-side switches while it is 11.45 A for the VF side. Calculation of (5.7) with these current values and $P_D = 1.25$ W gives the following ranges for the dead-time interval duration:

- 32.37 $ns \leqslant t_{dead} \leqslant$ 199.39 ns for the current-fed side
- 13.48 $ns \leqslant t_{dead} \leqslant$ 102.56 ns for the voltage-fed side

The dead-time is chosen to be 70 ns, to reduce the influence on the converter waveforms and accommodate both ranges. Once t_{dead} is known, the minimum current necessary to obtain ZVS can be calculated as

$$I_{ZVS} = \frac{2C_{Q,eq}V_{OFF}}{t_{dead}}. \tag{5.8}$$

Evaluation of (5.8) with the chosen dead-time value gives:

- $I_{ZVS}^{CF} = 2.82\ A$ for the current-fed side;
- $I_{ZVS}^{VF} = 2.21\ A$ for the voltage-fed side.

5.4 Input inductor and magnetizing inductance

Once the ZVS currents are known, the input inductor and the transformer's magnetizing inductance are designed in order to force ZVS of the CF-side devices for the entire input voltage range.
To design them, the current ripples necessary to obtain ZVS need to be calculated. Consider (2.11). To have ZVS, the input and magnetizing current ripples must compensate the average input current value and the resonant current reflected to the primary side at the switch turn-on instant. At any given input voltage level, the switching node current value along the M-PWL-MCT at the switch turn-on is calculated. The value of this current that is furthest away from the ZVS condition is the highest on for S_L^b and the lowest one for S_L^t (as shown in Figure 5.6).

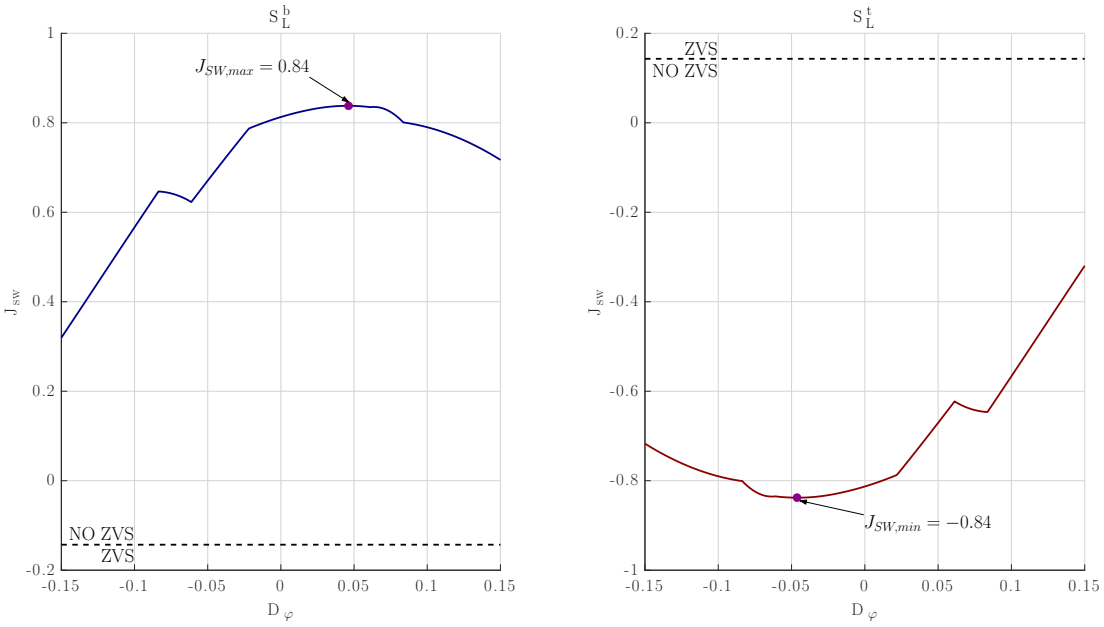


Figure 5.6: Normalized CF-side switching node currents at turn-on, along the M-PWL-MCT at $V_L = 250$ V. Only the resonant current and the average input current are considered.

These critical current values are calculated for a series of input voltage levels, obtaining the plots of Figure 5.7.
To have ZVS for the entire input voltage range, the switch turn-on current must

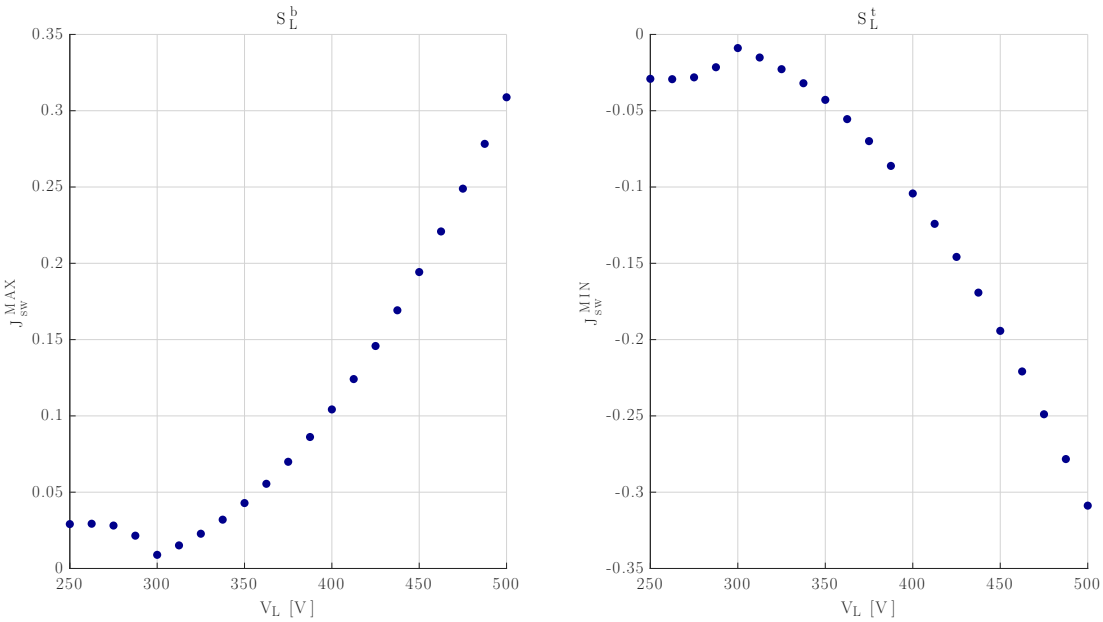


Figure 5.7: Normalized critical values of the switch turn-on currents, considering the resonant and average input current.

respect the ZVS conditions at worst-case, which, from Figure 5.7, is when $V_L = 500\ V$ for both switches. Since both the input and magnetizing current have minimal ripple at this input voltage value, if their ripple can ensure ZVS of the CF-side devices at this point, it is guaranteed for all the other input voltage values of the range.
The required total normalized current ripple is computed, from which the total inductance ratio can be calculated.
The total inductance ratio is defined as

$$\lambda = \lambda_{in} + \lambda_{\mu} = \frac{L_r}{L_{dc}} + \frac{L_r}{L_{\mu}}. \tag{5.9}$$

Using (2.13) and (2.15) gives the total normalized current ripple

$$\Delta J_{TOT} = \frac{\Delta J_{in}}{2} + \frac{\Delta J_{\mu}}{2} = \pi \frac{D_b}{f_n} U_L(\lambda_{dc} + \lambda_{\mu}) = \pi \frac{D_b}{f_n} U_L \lambda. \tag{5.10}$$

To achieve ZVS, the ripple must be constrained as

$$\Delta J_{TOT} = |\pm J_{ZVS} + J_{ON}| \ \text{ where } J_{ON} = \left\{ J_{sw}^{MAX}; J_{sw}^{MIN} \right\} \tag{5.11}$$

thus the total inductance ratio to obtain ZVS at worst-case is

$$\lambda = \Delta J_{TOT,WC} \frac{f_n}{\pi D_b} \frac{1}{U_L} \text{ where } \Delta J_{TOT,WC} = \max\{\Delta J_{TOT}\} \tag{5.12}$$

The worst case yields the same result for both switches, that is $\lambda \cong 0.451$. Dividing the inductance ratio equally between L_{dc} and L_μ, the two inductor values are:

- Input inductance: $L_{dc} = \frac{2L_r}{\lambda} = 88\ \mu H$
- Magnetizing inductance: $L_\mu = \frac{2L_r}{\lambda} = 88\ \mu H$

To verify both the M-PWL-MCT optimization and the inductors design, the switch currents can now be plotted by considering the current ripples.

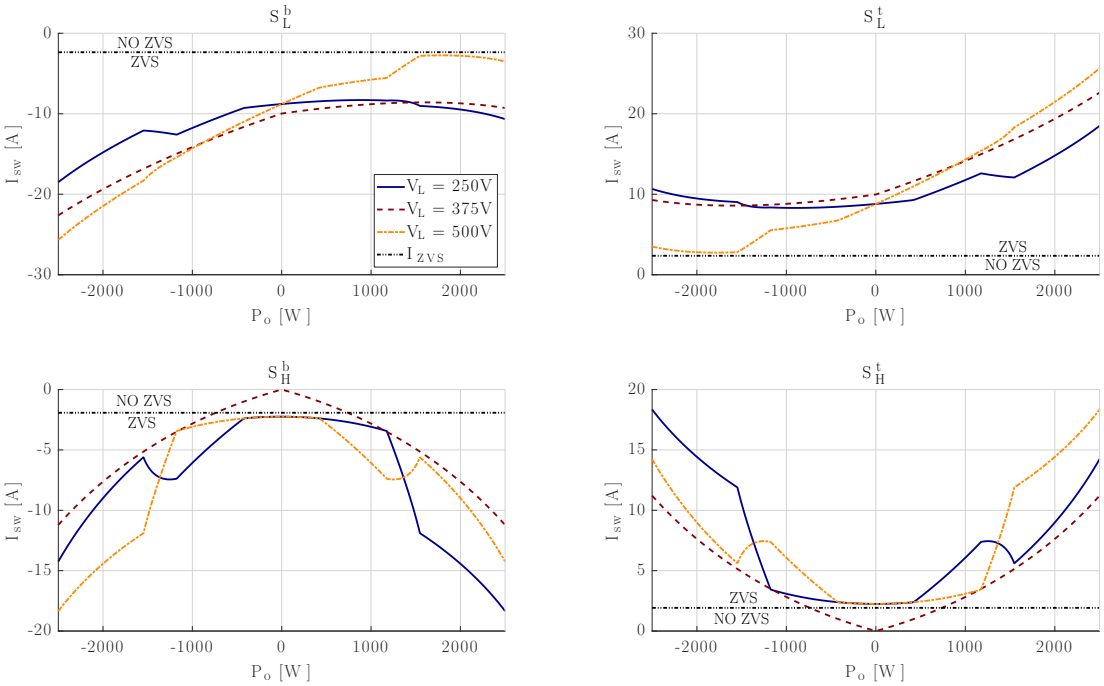


Figure 5.8: ZVS ranges along the M-PWL-MCT at three different input voltage levels

As it can be seen from Figure 5.8, ZVS is lost in the VF-side devices only around $V_L = 375\ V$ at light load. In this case the M-PWL-MCT becomes a pure phase-shift modulation and avoiding the regions where ZVS is not achieved is impossible.

5.5 Half-bridge capacitive legs

The last components values to be decided are the capacitive bridge legs. Starting from the CF side, the capacitor values can be computed to have a voltage ripple

below a specified one.
If $V_B = V_1 + V_2$ is constant, the voltage variations on the two capacitors are equal and opposite. Assuming that the two capacitors are identical ($C_L^b = C_L^t = C_L$) and considering the circuit of Figure 5.9, the following relationship between their currents is obtained:

$$i_{C_L^b} = -i_{C_L^t} = \frac{ni_r + i_\mu}{2} \tag{5.13}$$

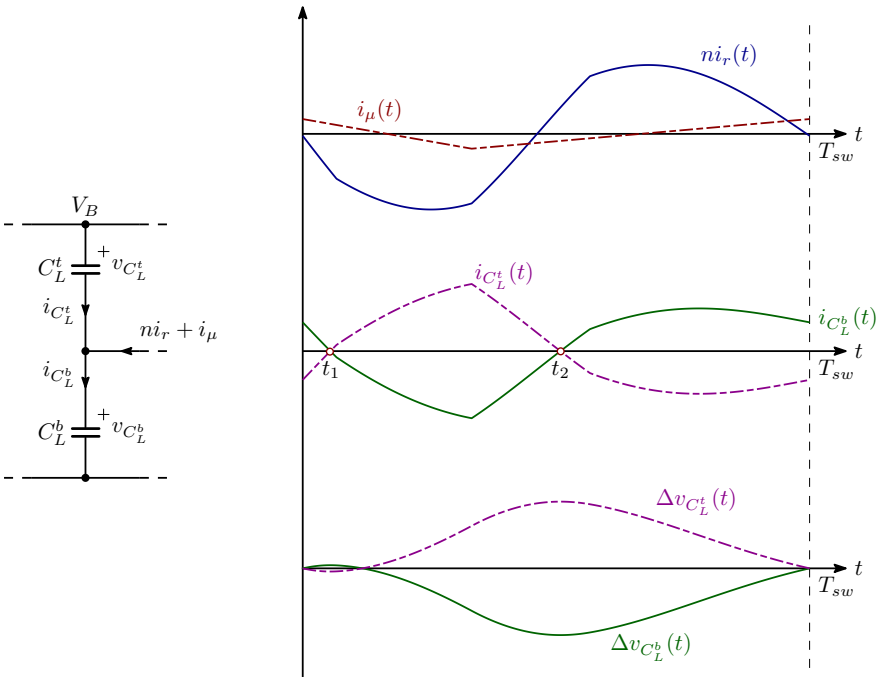


Figure 5.9: Theoretical waveforms on the CF-side capacitive leg

The maximum peak value of the capacitor current is found numerically to be in the operating point corresponding to $V_L = 500\ V$ at nominal power. This point yields the maximum voltage ripple.
The peak-to-peak voltage ripple can be calculated by numerical integration of the current waveforms as expressed by

$$\Delta V_{C,pp}^{CF} = \frac{1}{C_L} \int_{t_1}^{t_2} i_{C_L^t}(\tau) d\tau \tag{5.14}$$

where $t_1 \leqslant t \leqslant t_2$ is the time interval where $i_{C_L^t}$ is positive.
Specifying a maximum peak-to-peak voltage ripple of 10 V, the value of C_L is calculated as

$$C_L \geqslant \frac{1}{\Delta V_{C,pp}^{CF}} \int_{t_1}^{t_2} i_{C_L^t}(\tau) d\tau = 1.37\ \mu F \Longrightarrow C_L = 2\ \mu F \tag{5.15}$$

Considering the VF-side capacitive leg instead, the resonant capacitance can be integrated into the leg, reducing the component count. Figure 5.10 shows the equivalent circuit when integrating the resonant capacitor.

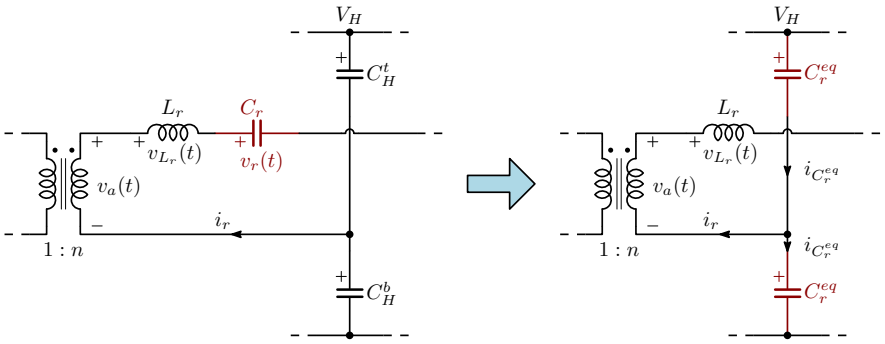


Figure 5.10: Equivalent circuit to integrate the resonant capacitance into the VF-side capacitive leg.

To maintain topology equivalence, the tank resonant current must be unchanged when integrating the resonant capacitor. The tank current with the circuit of Figure 5.10 is

$$i_r = C_r \left(\frac{dv_a(t)}{dt} - \frac{dv_{L_r}(t)}{dt} \right) \tag{5.16}$$

If the two equivalent resonant capacitors are identical, the resonant current is divided equally between the two, such that

$$|i_{C_r^{eq}}| = \frac{i_r}{2}. \tag{5.17}$$

The current in the equivalent capacitors is

$$i_{C_{r,eq}} = C_r^{eq} \left(\frac{dv_a(t)}{dt} - \frac{dv_{L_r}(t)}{dt} \right) \Longrightarrow i_r = 2C_r^{eq} \left(\frac{dv_a(t)}{dt} - \frac{dv_{L_r}(t)}{dt} \right) \tag{5.18}$$

Equating (5.16) and (5.18) gives that $C_r^{eq} = \frac{C_r}{2} = 25\ nF$. Applying the same reasoning as per the CF-side leg, C_H^b and C_H^t would have the same value of 2 μF as C_L^b and C_L^t. Placing a small capacitance in series with these capacitor will make C_H^x negligible. Thus the converter circuit becomes the one shown in Figure 5.11

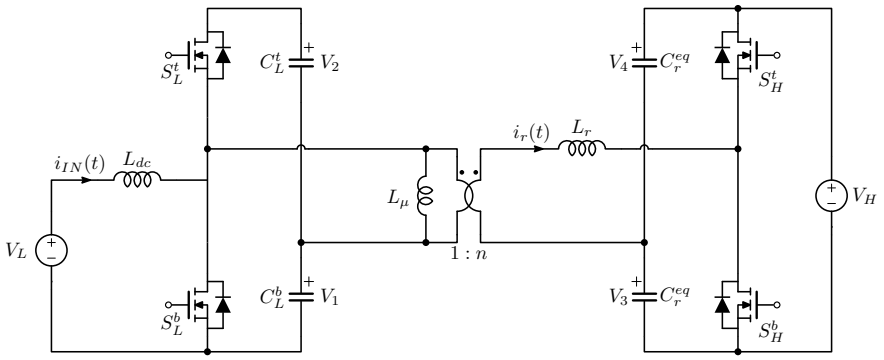


Figure 5.11: SR-CFDHB circuit with the integrated resonant capacitor.

5.6 Component values recap

The chosen component and parameters values are recapped in the following table

Table 5.2: Chosen component values.

Component/parameter	Value
Input inductor L_{dc}	88 μH
Resonant inductor L_r	20 μH
Resonant capacitor C_r	50 nF
Equivalent resonant capacitor C_r^{eq}	25 nF
Resonant frequency f_r	160 kHz
Transformer turns ratio n	0.53
Magnetizing inductance L_μ	88 μH
CF-side half-bridge capacitive leg C_L	2 μF
VF-side half-bridge capacitive leg C_H	2 μF
MOSFETs	$G3R3MT12K$

Chapter 6

Design of the magnetic components

The design of the magnetic components has two main objectives:

- Obtain the wanted component parameters (e.g. inductance and turns ratio)
- Minimize the component losses

In this chapter, all three magnetic components are designed to minimize the losses (explained in Appendix B) and obtain proper converter operation.

6.1 Transformer

The transformer waveforms present big and fast variations of the magnetic flux density, so that core losses become significant and can't be ignored.
The design procedure follows the one presented in [6].
Starting from the Faraday's law, the magnetic flux density variation can be calculated as follows

$$B_{pk} = \frac{\int_{t_1}^{t_2} |v_1(t)|dt}{2N_1A_c} = \frac{\Lambda_1}{2N_1A_c} \tag{6.1}$$

where $t \in [t_1; t_2]$ is the portion of the switching period where $v_1(t)$, the transformer primary-side voltage, is negative.
The numerator of (6.1) is the Volt-second applied to the transformer primary side. Referencing Figure 6.1 and knowing that $D_b = 1 - n\frac{V_L}{V_H}$, evaluation of the integral gives

$$\Lambda_1 = \int_{t_1}^{t_2} |v_1(t)|dt = \frac{1}{f_{sw}} \left(V_L - n\frac{V_L^2}{V_H} \right). \tag{6.2}$$

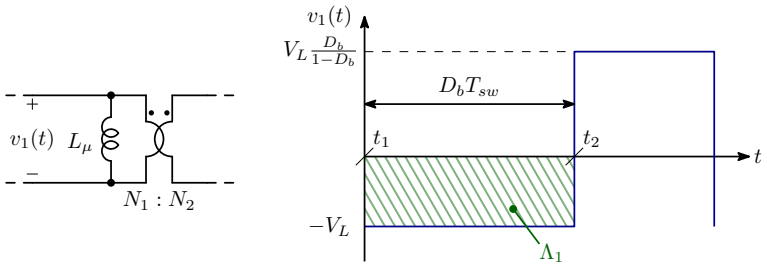


Figure 6.1: Transformer primary side voltage waveform

By looking at $\frac{\partial \Lambda_1}{\partial V_L}$ and at its sign, it can be seen that the applied Volt-second is maximum at the middle of the input voltage range, where $D_b = 0.5$. In the considered design, the maximum applied Volt-second is $\Lambda_1 \cong 938\ V\mu s$. The core and copper losses are dependent on B_{pk}, core geometry and properties, applied Vs, RMS current and winding arrangement.
The core losses can be estimated using the Steinmetz equation, which gives

$$P_{core} = C_m f^x B_{pk}^y Vol = K_{core} B_{pk}^y. \tag{6.3}$$

The copper losses instead, are estimated by starting from the joule losses in the windings. A loss minimization procedure, explained in Appendix B, gives (B.14) as an expression for the wire losses in a multi-winding component. The sum in the numerator of (B.14) is the total RMS current, referred to the primary side, from here on referred to as I_{tot}. An expression for N_1 can be found from (6.1) and substituted into (B.14), resulting in the following expression for the transformer windings copper losses

$$P_{Cu} = \rho F_R \frac{MLT}{Aw} I_{tot}^2 N_1 = \rho F_R \frac{(MLT) I_{tot}^2 \Lambda_1^2}{4 K_u W_A A_c^2} \frac{1}{B_{pk}^2} = K_{Cu} \frac{1}{B_{pk}^2} \tag{6.4}$$

where $F_R = \frac{R_{AC}}{R_{DC}}$ is the wire resistance ratio considering the proximity and skin effect.
In this case, the transformer has only two windings, so I_{tot} can be calculated as

$$I_{tot} = \sum_{j=1}^{2} \frac{N_j}{N_1} I_j = I_1 + \frac{N_2}{N_1} I_2 = I_{prim} + n I_{sec}. \tag{6.5}$$

The core losses increase with the magnetic flux density (so having more turns will reduce the core losses), while the opposite happens for the wire losses. Thus exists a point that minimizes the total losses.
The total losses can be expressed by combining (6.3) and (6.4), obtaining

$$P_{tot} = P_{core} + P_{Cu} = K_{core} B_{pk}^{y} + K_{Cu} \frac{1}{B_{pk}^{2}}. \tag{6.6}$$

Posing $\frac{\partial P_{tot}}{\partial B_{pk}} = 0$ and solving for B_{pk} gives the value of magnetic flux density which minimizes the losses.

$$B_{pk,opt} = \left(\frac{2K_{Cu}}{yK_{core}} \right)^{\frac{1}{y+2}} \tag{6.7}$$

The transformer design starts with the selection of a suitable core shape and material. To do this, the core geometrical constant has been used.
Following the approach explained in [6], the core geometrical constant considering the core and copper losses ($K_{g,Fe}$) can be calculated by substituting (6.7) into (6.3) and (6.6), obtaining the following equation for the total power loss

$$P_{tot} = [A_c l_m C_m f^x]^{\frac{2}{y+2}} \left[\rho F_R \frac{\Lambda_1^2 I_{tot}^2}{4K_u} \frac{MLT}{W_A A_c^2} \right]^{\frac{y}{y+2}} \left[\left(\frac{y}{2} \right)^{-\frac{y}{y+2}} + \left(\frac{y}{2} \right)^{\frac{2}{y+2}} \right]. \tag{6.8}$$

This equation can be rearranged, obtaining the following expressions for $K_{g,Fe}$

$$K_{g,Fe} = \frac{W_A A_c^{\frac{2(y-1)}{y}}}{(MLT) l_m^{\frac{2}{y}}} \left[\left(\frac{y}{2} \right)^{-\frac{y}{y+2}} + \left(\frac{y}{2} \right)^{\frac{2}{y+2}} \right]^{-\frac{y+2}{y}} = \rho F_R \frac{\Lambda_1^2 I_{tot}^2 (C_m f^x)^{\frac{2}{y}}}{4K_u P_{loss}^{\frac{y+2}{y}}} \tag{6.9}$$

where l_m is the average magnetic path length and P_{loss} is the specified maximum allowed loss.
The left side of (6.9) contains only core-dependent parameters, while the right side contains both specifications and core parameters. Since some parameters of the selected core are present in both sides of the equation, the selection of a proper core is an iterative process. If a core is suitable, the core geometrical constant calculated using the left side of (6.9) is grater that the one calculated using the right side, satisfying the following inequality

$$K_{g,Fe} \geqslant \rho F_R \frac{\Lambda_1^2 I_{tot}^2 (C_m f^x)^{\frac{2}{y}}}{4K_u P_{loss}^{\frac{y+2}{y}}} \tag{6.10}$$

Initially, the value of F_R must be assumed, as the winding configuration is not yet known (2 is a good starting value). The total allowed losses must also be specified.

After a core is selected, $B_{pk,opt}$ can be calculated. The ideal number of turns of both windings can then be calculated from

$$\begin{cases} N_{1,ideal} = \frac{\Lambda_1}{2A_c B_{pk,opt}} \\ N_{2,ideal} = nN_{1,ideal} \end{cases} \tag{6.11}$$

The conductor to be used as the winding must then be chosen, based on the current rating. After that, the implemented number of turns and winding arrangement must be chosen, preferably as close as possible to the ideal ones, if physically realizable.
The implemented peak magnetic flux density and losses can then be calculated
Since in this design the primary side magnetizing inductance is used, a value for the air gap length must also be calculated, once the core geometry is known.
After all the parameters are decided, $K_{g,Fe}$ can then be calculated again from the right side of (6.9) by using the actual value of F_R and P_{loss}, to verify if the selected core is actually suitable. If the inequality is not satisfied, the process must be reiterated.
The required specifications are recapped in the following table.

Table 6.1: Transformer specifications

Parameter	**Value**
n	0.53
L_μ	88 μH
T_{max}	100 $°C$
P_{loss}	17 W
I_{tot}	18.2 A

After a few iterations, the decided core is the **PQ 40/40** made with the **N97** ferrite material. Their characteristics are summarized in the following tables.

The optimum point $B_{pk,opt} = 99.52\ mT$ achieves around 12 W of total losses, with $N_{1,ideal} = 24.94$ and $N_{2,ideal} = 13.29$.

Table 6.2: PQ 40/40 core parameters

Parameter	Value
Central leg cross section A_c	1.89 cm^2
Window area W_A	2.48 cm^2
Window height l_w	29.5 mm
Core volume Vol	17580 mm^3
Mean turn length MLT	86 mm
Average magnetic path length l_m	93 mm

Table 6.3: Steinmetz coefficients of the N97 material at 200 kHz

Parameter	Value
C_m	1.26
x	1.47
y	2.40

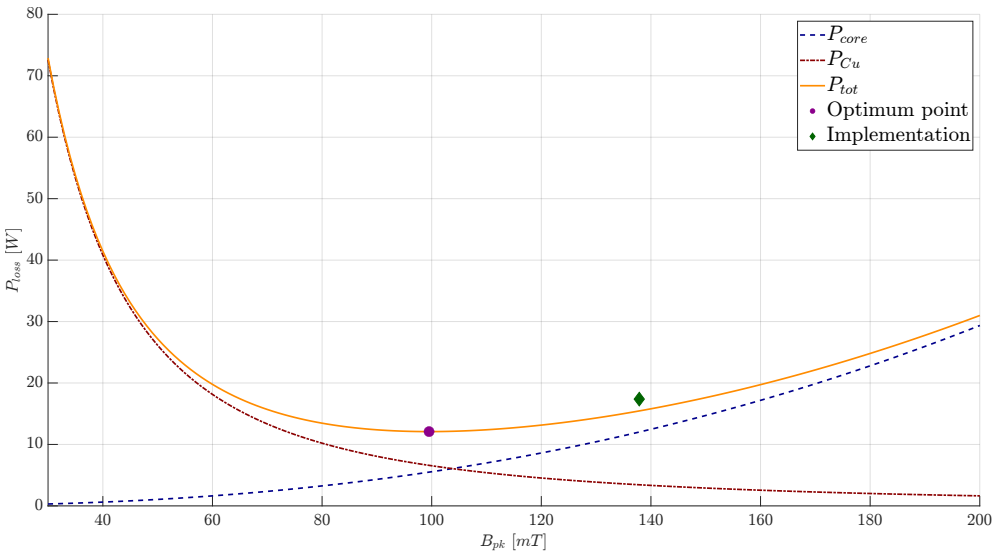


Figure 6.2: Estimated transformer losses for the ideal and implemented operating point

The implemented number of turns are $N_1 = 18$ and $N_2 = 10$. This choice is sub-optimal, so this will result in higher losses. The 1050x50 μm Litz wire has been chosen to implement the windings, which are arranged as displayed in Figure 6.3. This wire's strand diameter is a good fit for the operating frequency of the converter. According to selected Litz wire manufacturer's data-sheet, a good choice of strand diameter satisfies $d_o \leqslant \frac{\delta}{3}$, where δ is the penetration depth

in copper at the desired frequency. At 200 kHz ($\delta = 0.148\ mm$) a strand diameter of 50 μm is a suitable choice.

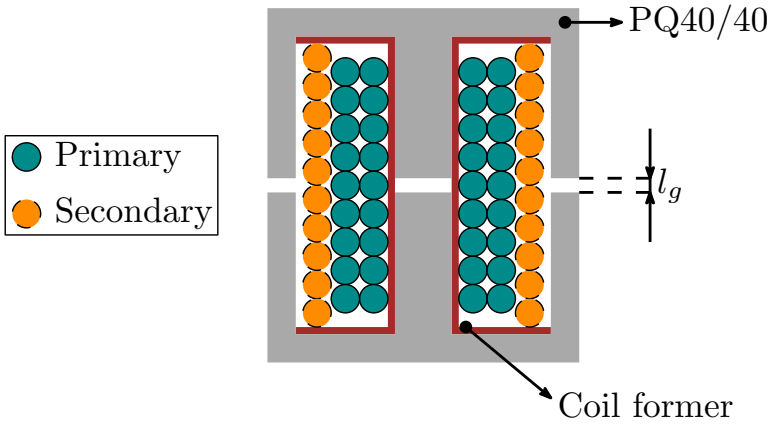


Figure 6.3: Implemented transformer structure. The primary side is divided in two layers, each composed by 9 turns. The secondary is made by a single layer.

With this winding arrangement the copper losses (using (B.23) as an expression for F_R) can be calculated as:

- Primary side: $F_{R,1} = 1.44$, $P_{Cu,1} = F_{R,1}\rho\frac{(MLT)N_1 I_{prim}^2}{A_s N_s} = 2.06\ W$;
- Secondary side: $F_{R,2} = 1.18$, $P_{Cu,2} = F_{R,2}\rho\frac{(MLT)N_2 I_{sec}^2}{A_s N_s} = 3.29\ W$.

The core losses of the implemented transformer are estimated to be 12.02 W, bringing the total estimated losses to **17.38 W**. To finalize the design, the air gap length must be decided to obtain the wanted magnetizing inductance. The primary side magnetizing inductance is given by

$$L_\mu = \frac{N_1^2}{\Re_{tot}} \tag{6.12}$$

where $\Re_{tot}$ is the total reluctance of the magnetic path. To calculate the total reluctance, an equivalent circuit can be used.
The core is made by a ferromagnetic material, so the core reluctance $\Re_c$ can be neglected. The air gap is distributed between one central leg and two lateral legs. The cross section of the external legs is half of the one of the central leg, so the reluctances can be calculated as

$$\begin{cases} \Re_{g,c} = \frac{l_g}{\mu_0 A_c} \\ \Re_{g,l} = \frac{2l_g}{\mu_0 A_c} \end{cases} \tag{6.13}$$

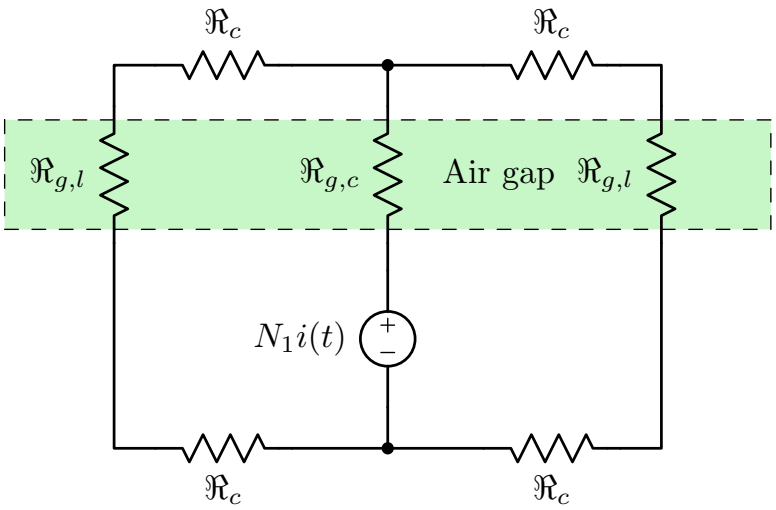


Figure 6.4: Equivalent circuit used to calculate the magnetic path reluctance

The total reluctance can then be approximated as

$$\Re_{tot} \cong \Re_{g,c} + \frac{\Re_{g,l}}{2} = 2\Re_{g,c}. \tag{6.14}$$

Substituting (6.14) into (6.12) yields the final expression of the primary side magnetizing inductance, that can be used to obtain the air gap length, giving

$$l_g \cong N_1^2 \frac{\mu_0 A_c}{2L_\mu} = 0.44\ mm \tag{6.15}$$

This value is calculated by neglecting a lot of phenomena that take place in a real magnetic components, such as fringing flux and finite core permeability. This means that more accurate methods must be used to calculate the air gap length or it must be tuned using measurements on the physical component. In particular, due to fringing flux which increases the equivalent surface area of the air gap, the air gap will be bigger than the calculated one, introducing higher losses, especially in the wires.

Once the transformer has been built, it must be characterized to obtain its parameters. A model, neglecting the winding resistance, for the two-winding transformer is the one shown in Figure 6.5.

The model is described by the following impedance matrix

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} s(L_{l1} + L_\mu) & sL_\mu n \\ sL_\mu n & s(L_{l2} + n^2 L_\mu) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{6.16}$$

To extract the parameters of (6.16), three measurements can be carried out with

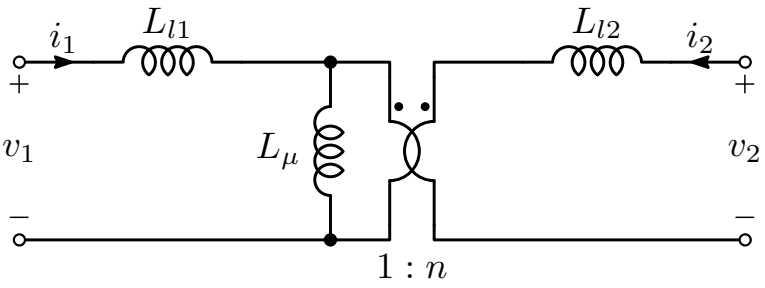


Figure 6.5: Transformer three-inductance model. The winding resistances are neglected.

the impedance analyser:

- $L_1^{SO} = L_{l1} + L_\mu$: Primary-side inductance with the secondary in open circuit;
- $L_1^{SS} = L_{l1} + \left(L_\mu // \frac{L_{l2}}{n^2}\right)$: Primary-side inductance with the secondary short-circuited;
- $L_2^{PO} = L_{l2} + n^2 L_\mu$: Secondary-side inductance with the primary in open circuit.

However, this model cannot be fully characterized by only three measurements, since it has four independent parameters. From (6.12), one can see that the magnetizing inductance referred to the primary side is proportional to N_1^2. A ratio between the magnetizing inductance reflected to the secondary side and the magnetizing inductance referred to the primary side will thus yield the value of the turns ratio squared. Neglecting the leakage inductances, the turns ratio can be imposed as

$$n \cong \sqrt{\frac{L_2^{PO}}{L_1^{SO}}}. \tag{6.17}$$

Once the value of the turns ratio has been found, the model's inductances can be calculated as

$$\begin{cases} L_\mu = \sqrt{\frac{(L_1^{SO} - L_1^{SS}) L_2^{PO}}{n^2}} \\ L_{l1} = L_1^{SO} - L_\mu \\ L_{l2} = L_2^{PO} - n^2 L_\mu \end{cases} \tag{6.18}$$

The model used in the steady-state analysis and in the design, however, is the one shown in Figure 6.6, characterized by the following impedance matrix

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} sL_{\mu,eq} & sL_{\mu,eq}n_{eq} \\ sL_{\mu,eq}n_{eq} & s(L_{l,eq} + n_{eq}^2 L_{\mu,eq}) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{6.19}$$

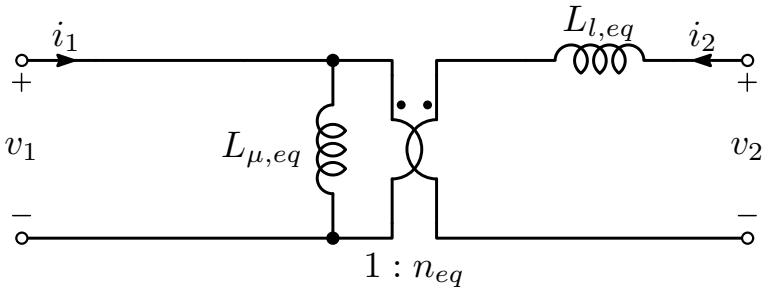


Figure 6.6: Transformer two-inductance model. The winding resistances are neglected.

Equating (6.16) and (6.19) yields the following expressions for the parameters of the two-inductance model

$$\begin{cases} L_{\mu,eq} = L_{l,1} + L_\mu \\ n_{eq} = n\frac{L_\mu}{L_{\mu,eq}} \\ L_{l,eq} = L_{l2} + nL_{l1}n_{eq} \end{cases} \tag{6.20}$$

Table 6.4 recaps the obtained transformer parameters. The final implemented air gap is $l_g = 0.72$ mm.

Table 6.4: Transformer's three-inductance and two inductance model parameters, obtained from the impedence analyser measurements

Three-inductance model	
$L_{l,1}$	1.976 μH
$L_{l,2}$	626.1 nH
L_μ	77.587 μH
n	0.563
Two-inductance model	
$L_{l,eq}$	1.236 nH
$L_{\mu,eq}$	79.563 μH
n_{eq}	0.549

6.2 Resonant inductor

The tank inductor must consider also $L_{l,eq}$. The series between this inductor and an eventual external inductor $L_{r,ext}$ should result in $L_r = L_{l,eq} + L_{r,ext} = 20\ \mu H$. The transformer equivalent leakage inductance is too small, so an external inductor needs to be built to obtain the wanted resonant tank inductor value.
Since $L_{r,ext}$ is an AC inductor, core losses will be significant, so the same procedure used for the transformer design must be utilized. To do this, the maximum applied Volt-second must be calculated.

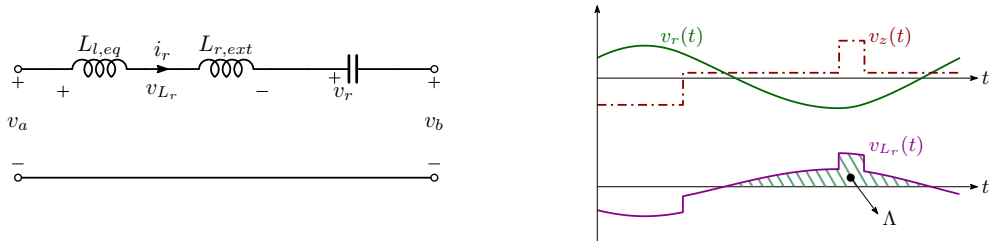


Figure 6.7: Resonant inductor voltage waveforms

By looking at the circuit shown in Figure 6.7, the voltage on the total resonant inductance is

$$v_{L_r}(t) = v_z(t) - v_r(t) = v_a(t) - v_b(t) - v_r(t). \tag{6.21}$$

This voltage divides between $L_{l,eq}$ and $L_{r,ext}$, so the Volt-second applied to the external tank inductor can be calculated as

$$\Lambda = \int_{t_1}^{t_2} \frac{L_{r,ext}}{L_{l,eq} + L_{r,ext}} v_{L_r}(t)dt = \int_{t_1}^{t_2} \alpha(v_a(t) - v_b(t) - v_r(t))dt. \tag{6.22}$$

Analytical evaluation of this integral is cumbersome, so it has been chosen to numerically calculate it and find its maximum value. This resulted in a maximum applied Volt-second value of $\Lambda = 870.62$ V μs.
The inductor specifications are recapped in the following table.

The selected core is the **PQ 35/35** in **N97** material, while the windings are made of Litz 1050x50 μm. The same procedure of the transformer design is employed, leading to $B_{pk,opt} = 112.28\ mT$ with $N_{ideal} = 22.673$ turns.

Table 6.5: External tank inductor specifications

Parameter	Value
$L_{r,ext}$	18.763 μH
I_{RMS}	17.08 A
T_{max}	100 $°C$
P_{loss}	20 W

Table 6.6: PQ 35/35 core parameters

Parameter	Value
Central leg cross section A_c	1.71 cm^2
Window area W_A	1.55 cm^2
Window height l_w	25 mm
Core volume Vol	13650 mm^3
Mean turn length MLT	77 mm
Average magnetic path length l_m	79.7 mm

The decided number of turns is $N = 16$, split in two equal layers (as shown in Figure 6.8). This yields the following losses:

- Wire losses: 5.94 W
- Core losses: 13.16 W
- Total losses: 19.10 W

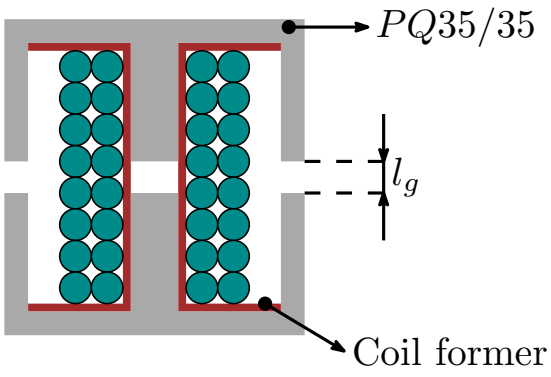


Figure 6.8: Winding structure of inductor $L_{r,ext}$

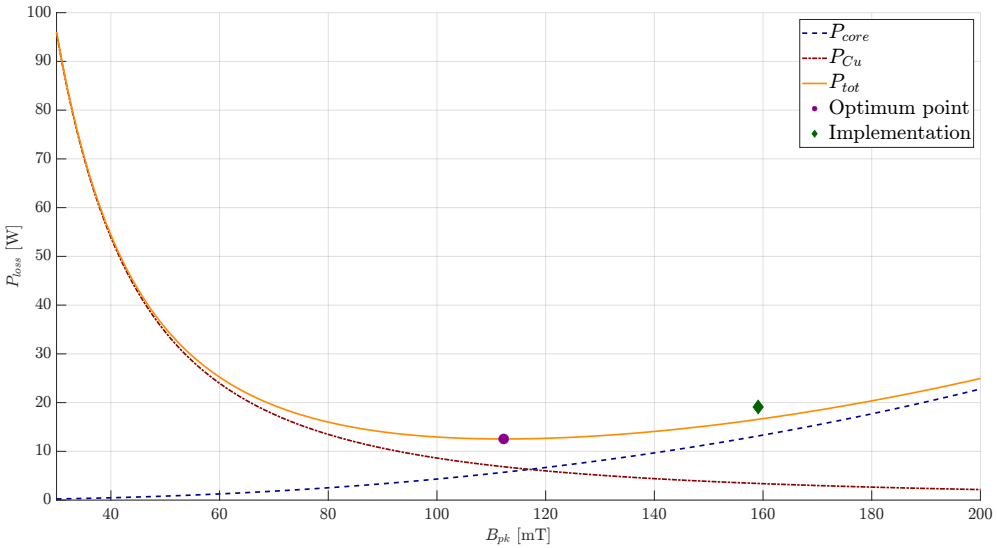


Figure 6.9: Estimated resonant tank inductor losses for the ideal and implemented operating point

This choice increases losses, but the lower number of turns allows to have a smaller air gap, reducing flux fringing effects. Since the core has the same geometry as the one used for the transformer, the air gap can be calculated as

$$l_g \cong N^2 \frac{\mu_0 A_c}{2L} = 1.44\ mm \tag{6.23}$$

The inductor built for the prototype has an inductance value of 20 μH (measured with the impedance analyser), with a 3 mm air gap.

6.2.1 Resonant capacitor

At this point, it is possible to design the resonant capacitor, which is placed in series with L_r in the prototype for ease of implementation. Implementing a 50 nF capacitance that can carry the nominal RMS current of 17.08 A with a single capacitor is arduous at best, so the resonant capacitance has been built by paralleling multiple smaller capacitors.
In particular, the resonant capacitance built for the prototype is made by:

- 6 × 4.7nF ECW-H8472HVB film capacitors, rated at 800 V;
- 2 × 5.6nF ECW-H10562JVB film capacitors, rated at 1 kV;
- 1 × 6.8nF ECW-H8682HVB film capacitor, rated at 800 V.

So that the total external capacitance is $C_{r,ext} = 46.2$ nF. Neglecting the parasitic capacitances introduced by the MOSFETs and the circuit, the resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{L_{r,eff}C_{r,ext}}} = 161\ kHz \tag{6.24}$$

which is very close to the desired one.

6.3 Input inductor

The input inductor has been designed following the same procedure employed for the other magnetic components. Since it is used to help ZVS of the CF-side devices, its current presents a significant ripple. This means that both wire losses and core losses must be considered.
The inductor specifications are shown in the table below.

Table 6.7: Input inductor design specifications

Parameter	Value
L_{dc}	$94\ \mu H$
T_{max}	$100\ °C$
P_{loss}	$7\ W$

Assuming unity efficiency, the maximum average inductor current can be calculated as

$$I_{IN,max} = \frac{P_o}{V_{L,min}} = 10\ A. \tag{6.25}$$

The maximum inductor current ripple is then

$$\Delta I_{in,pk-pk} = \frac{D_b V_L}{L_{dc} f_{sw}} = \frac{1}{L_{dc} f_{sw}} \left(V_L - n\frac{V_L^2}{V_H} \right) \cong 10\ A \tag{6.26}$$

Since the current waveform is triangular, the RMS value of the input inductor current is

$$I_{in,RMS} = I_{IN}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta I_{in,pk-pk}}{2I_{IN}}\right)^2} = 10.4\ A \tag{6.27}$$

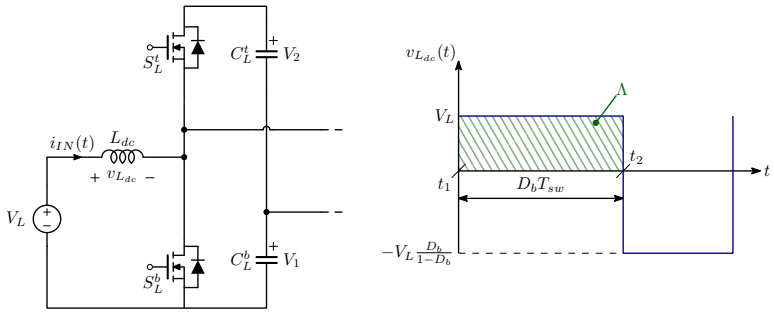


Figure 6.10: Input inductor voltage waveform

As can be seen from Figure 6.10, the applied volt-second is the same that is applied to the transformer primary side, so $\Lambda \cong 938\ V\mu s$.
Application of the design procedure leads to choosing the **PQ 40/40** in **N97** material, while the winding is implemented by $N = 30$ turns of Litz 1050x50 μm, arranged as shown in Figure 6.11.

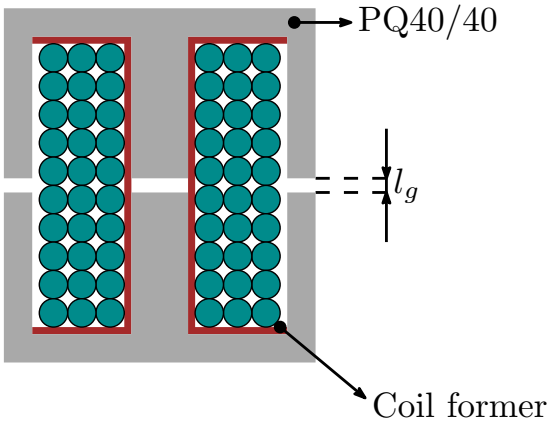


Figure 6.11: Winding structure of inductor L_{dc}

The losses of the implemented inductor are estimated to be:

- Wire losses: 3.39 W
- Core losses: 3.53 W
- Total losses: 6.92 W

Evaluation of (6.23) for the desired value of L_{dc} yields a theoretical air gap of 1.21 mm.

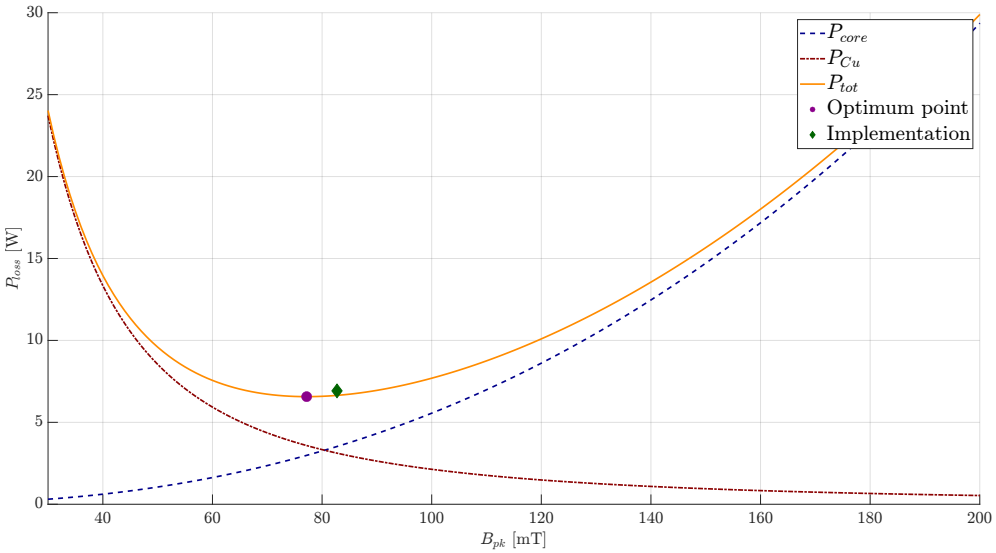


Figure 6.12: Estimated input inductor losses for the ideal and implemented operating point

The inductor built for the prototype has an inductance of 88 μH (measured with the impedance analyser) with an air gap of 2.5 mm.

Chapter 7

Simulation and experimental validation

In this chapter simulation results are shown and analysed, to validate the results of the study carried out.
After that, the prototype that has been built in the laboratory is presented, together with some measurement results.

7.1 Simulation

Simulations using the PLECS block-set in the SimuLink environment have been carried out to validate the theoretical study. The PLECS circuit is implemented as a block in Simulink, as shown in Figure 7.1.

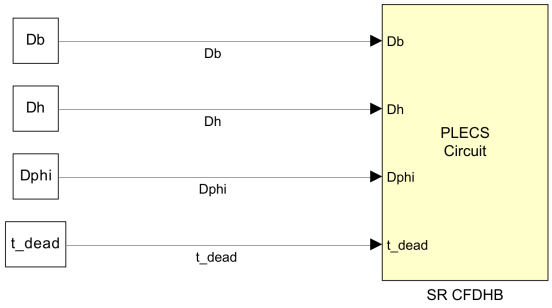


Figure 7.1: Simulink model containing the PLECS circuit. The values of the constants D_b, D_h, D_{phi} and t_{dead} are initialized in a separate script.

The PLECS circuit implements the converter circuit and the PWM modulator, together with all the necessary measurements, as shown in Figure 7.2. The parameters used in the simulation are recapped in Table 7.1.

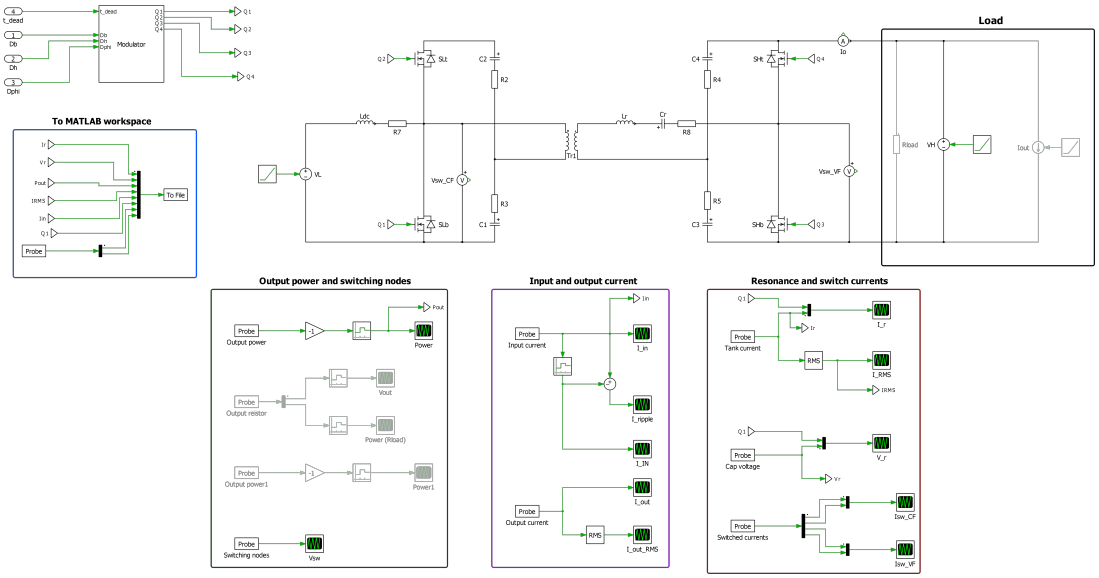


Figure 7.2: PLECS circuit, comprising the modulator and the measurements.

Table 7.1: Parameters used in the PLECS simulation. All series resistances are the ones of the components used in the prototype, as well as the transformer turns ratio. The resonant inductor value considers also the transformer equivalent leakage inductance of the two-inductance model of Figure 6.6. The resonant capacitor value is the one used in the prototype.

Parameter	Value
Switching frequency f_{sw}	200 kHz
Input inductor L_{dc}	89 μH
Series AC resistance $r_{L_{dc},AC}$	187.7 mΩ
Transformer turns ratio $n = \frac{N_2}{N_1}$	0.549
Primary side magnetizing inductance L_μ	80 μH
Resonant inductor L_r	21 μH
Series AC resistance $r_{L_r,AC}$	57.3 mΩ
Resonant capacitor C_r	46.2 nF
Half-bridge capacitors C_1, C_2, C_3, C_4	2 μF
CF-side capacitor ESR	12.5 mΩ
VF-side capacitor ESR	40 mΩ
Switch on-resistance	30 mΩ

This environment allows to simulate the steady-state behaviour of the converter. In particular, the output power with different load setups, the switching nodes voltage, switch currents, input and output power and resonance waveforms can be observed and the data is saved in a .mat file allowing further analysis.
The transformer is implemented as an ideal transformer, with a magnetizing inductance value equal to the one used in the model of Figure 6.6.
The modulator circuit (shown in Figure 7.3) allows also to take into account the effects of the dead-time, using turn-on delay blocks.

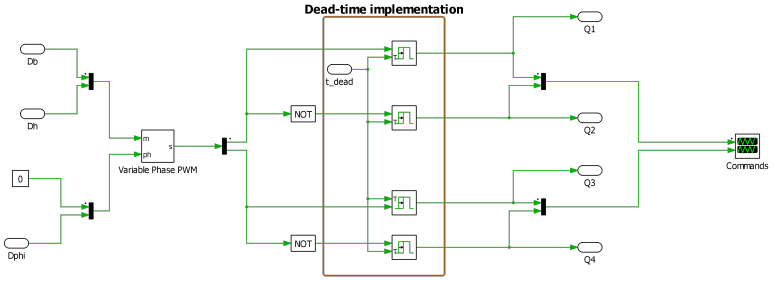


Figure 7.3: PWM modulator circuit used in the PLECS simulation.

As can be seen from Figure 7.4, there is a good match between the theoretical and simulated waveforms. The slight mismatch is due to the higher delivered power in the simulation (as can be seen in Table 7.2), which results in higher current and voltage in the resonant tank. Figure 7.5 shows the voltage at the two switching nodes. The CF-side switching node voltage is not constant during the switches conduction intervals because of the capacitors voltage ripple, while the VF-side switching node voltage remains constant during the switch conduction intervals because the load is a voltage source, imposing 400 V at the converter output port.
The simulation environment has also been used to validate the switch turn-on current calculation. By the use of a PLECS probe, the switch current can be plotted as a function on time and its value at the turn-on instant can be measured with cursors. This allows comparison with the theoretical values, as shown in Table 7.3.

Table 7.2: Comparison between the theoretical and simulated values of the resonant current corner points I_k $k = 0, 1, 2, 3$ at $V_L = 250$ V, $V_H = 400$ V, $D_b = 0.666$, $D_h = 0.5$, $D_\varphi = 0.15$

Parameter	Theoretical value	Simulated value
I_0	21.9 A	22.04 A
I_1	-18.1 A	-18.94 A
I_2	0.8 A	1.45 A
I_3	14.2 A	15 A
P_o	2485 W	2525 W
I_{RMS}	16.93 A	17.45 A

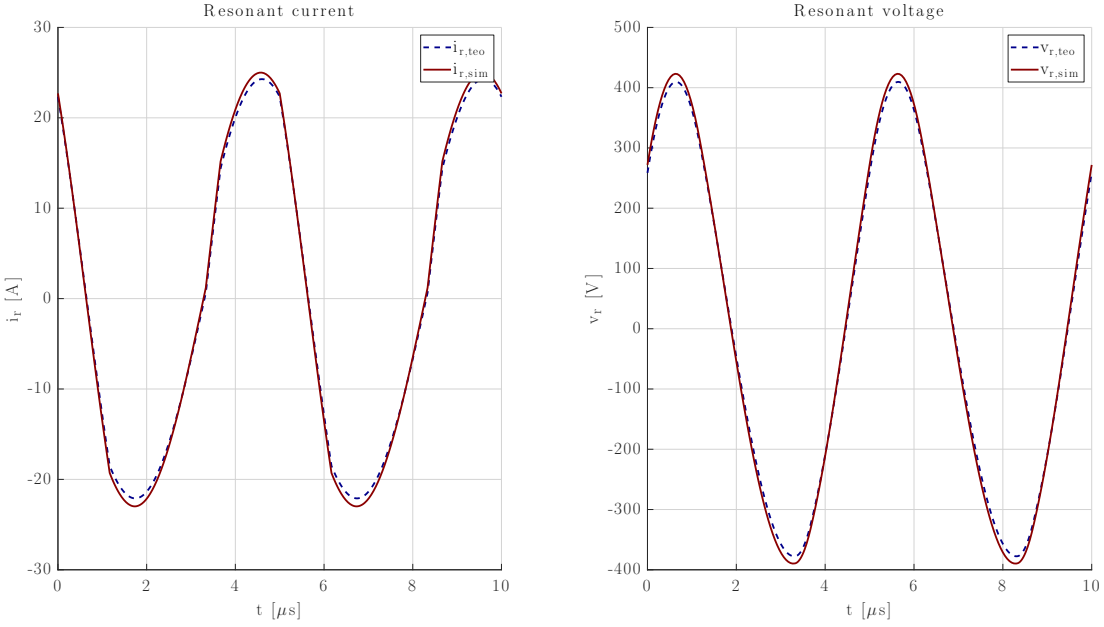


Figure 7.4: Resonance waveforms comparison at $V_L = 250$ V, $V_H = 400$ V, $D_b = 0.666$, $D_h = 0.5$, $D_\varphi = 0.15$, $t_{dead} = 0$ with a constant voltage load.

Table 7.3: Comparison between the theoretical and simulated values of the switches turn-on currents at $V_L = 250$ V, $V_H = 400$ V, $D_b = 0.666$, $D_h = 0.5$, $D_\varphi = 0.15$

Switch	Theoretical turn-on current	Simulated turn-on current
S_L^b	-11.6 A	-11.27 A
S_L^t	-19.4 A	-19.22 A
S_H^b	-18.1 A	-18.94 A
S_H^t	-14.2 A	-15 A

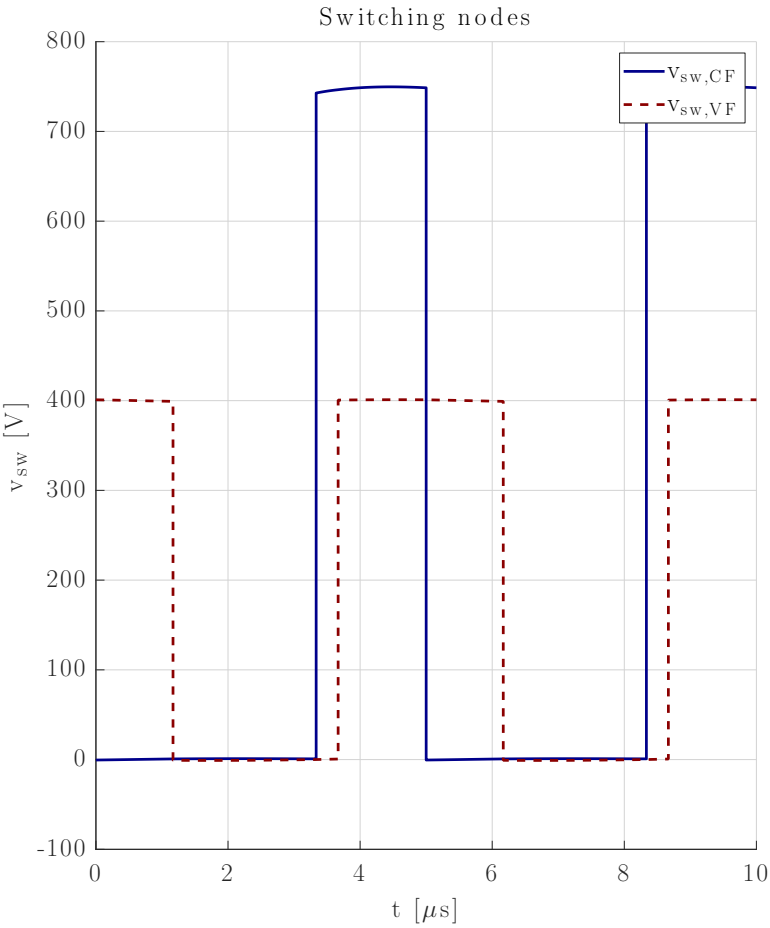


Figure 7.5: Simulated switching nodes voltage at $V_L = 250$ V, $V_H = 400$ V, $D_b = 0.666$, $D_h = 0.5$, $D_\varphi = 0.15$, $t_{dead} = 0$ with a constant voltage load.

7.2 Experimental validation

In this section, the prototype that has been built in the laboratory is presented, together with some waveforms and an efficiency measurement.

7.2.1 Prototype construction

The prototype is built by 3 main blocks:

- Two half-bridge leg boards (HB-LB), made by a switching leg board connected via screws to a capacitive leg board
- The passive components, namely the two inductors, the transformer and the resonant capacitor

A HB-LB (shown in Figure 7.6) comprises two MOSFETs, which make up the switching leg, two capacitors, which make up the capacitive leg, and the necessary driving circuit, together with screw connection points to easily mount the circuit. An additional capacitance C_{DC} is also placed between the positive and negative terminals of the Input/Output port of the half-bridge leg to provide voltage stabilization.

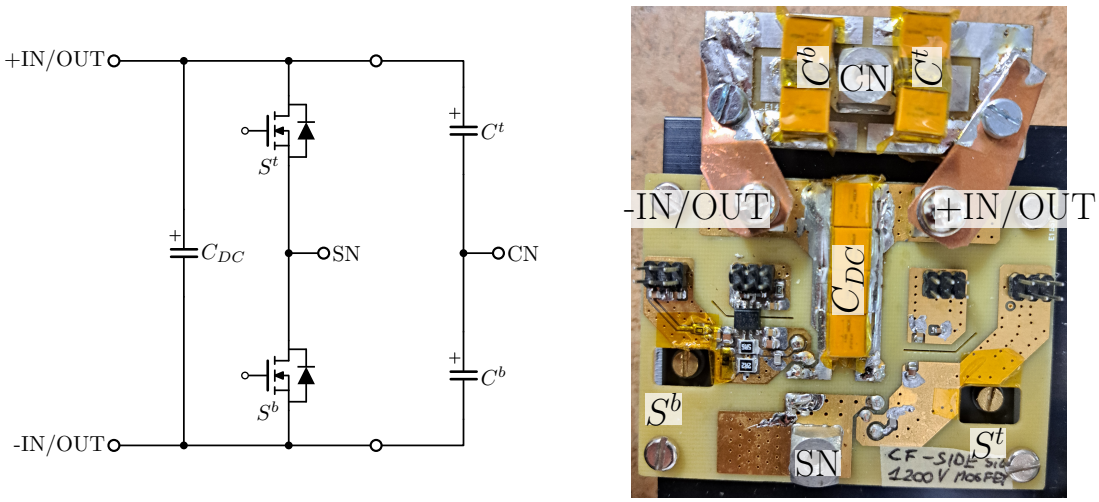


Figure 7.6: Half-bridge leg board schematic and physical implementation

On top of the HB-LB is placed an interface board (IB). This board generates the required isolated power supplies, which are brought to the HB-LB via some connectors, together with the MOSFETs command signals.

These signals reach the IB with some optical fibres. This increases system robustness regarding electromagnetic disturbances. In fact, having the command signals reach the board through an optical fibre link means that the board that generates the command signals is completely isolated from the HB-LB, so that EM noise generated by the fast commutations of the MOSFETs is far less likely to cause unwanted switch driving.
The switches command signals are generated by a microcontroller (the Texas Instruments TMS320F28379D), which is mounted on a different board.
The magnetic components are connected to the two HB-LB with screws, as shown in Figure 7.7.

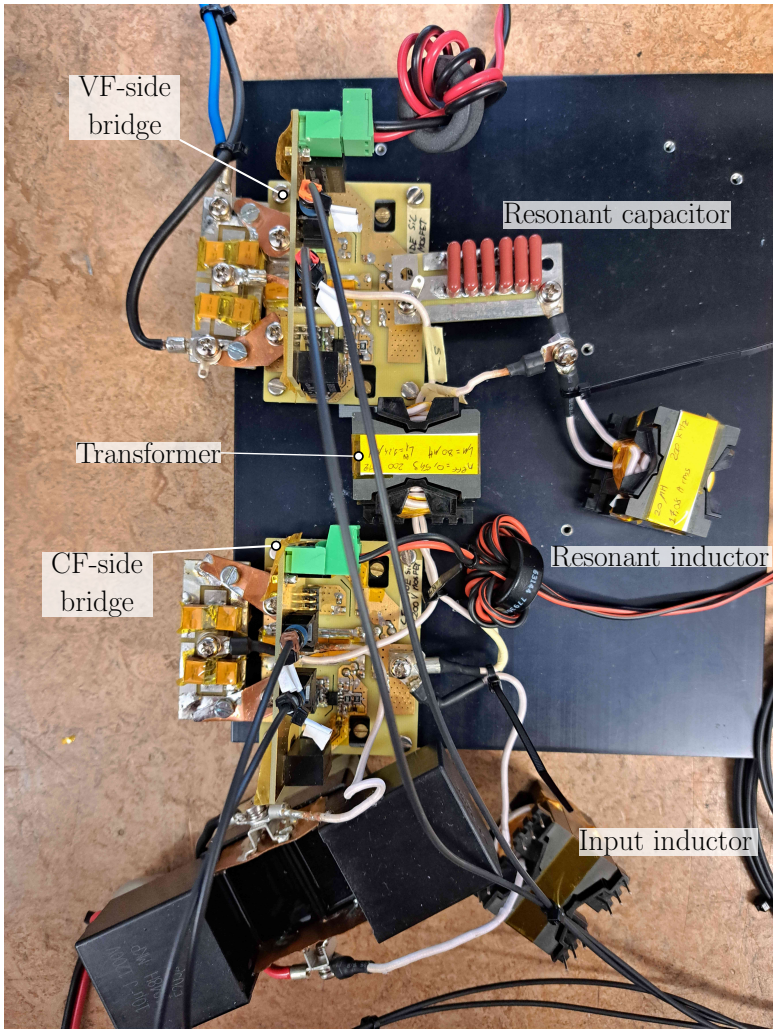


Figure 7.7: SR-CFDHB prototype

7.2.2 Overview of the microcontroller setup

In this section, the microcontroller setup used to control the converter is discussed. As said previously, the converter is controlled by the Texas Instruments TMS320F28379D microcontroller, which is mounted on a custom board (shown together with the converter in Figure 7.8) allowing the generation of the optical driving signals and connection to the PC.
The prototype has been controlled in open-loop, with the Texas Instruments IDE (Integrated Developing Environment) Code Composer Studio (CSS) allowing to change the duty cycle and phase shift values manually.

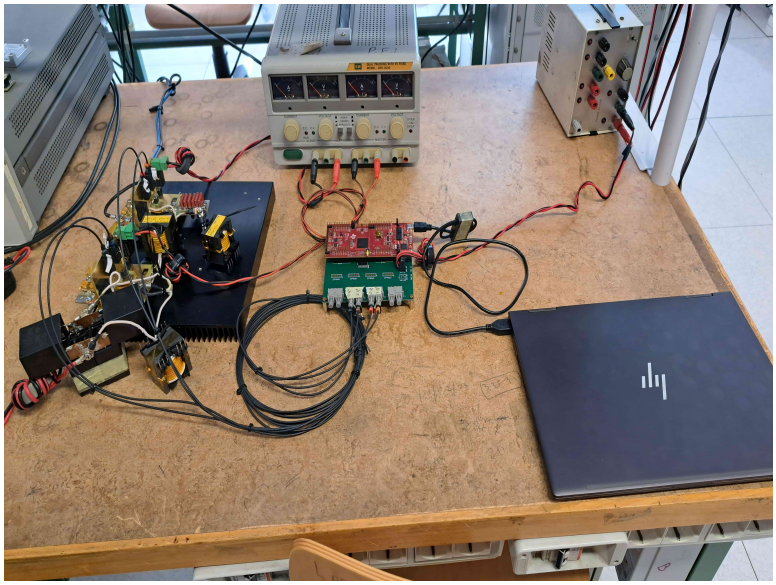


Figure 7.8: The prototype connected to the microcontroller board

The utilized microcontroller has various peripherals that are optimized for control of power electronics converters. Among these, the enhanced PWM (ePWM) have been used to generate the command signals for the MOSFETs.
The ePWM peripheral is organized in different, independent modules (ePWMx, where x is the number identifying the module). Each module has two channels: ePWMxA and ePWMxB, which can be configured independently. A simplified structure of an ePWM module is shown in Figure 7.9.
To control the converter, the ePWM modules have been setup in the following manner. ePWM1 controls the CF-side devices, while ePWM2 controls the VF-side MOSFETs. Channel A of each module generates the bottom switch command signal, while channel B the high-side's one. The time base of each module

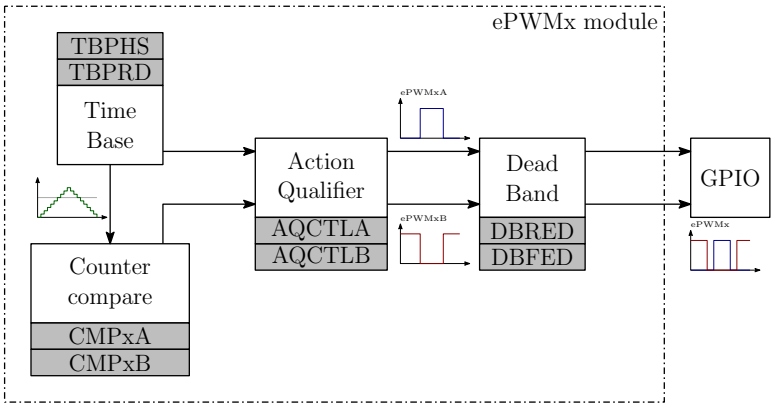


Figure 7.9: Simplified structure of an ePWM module and its registers, highlighted with the grey squares.

counts in a double ramp mode, counting from zero up until the value stored in TBPRD is reached an then counting to zero.
The counter value is compared by the counter compare with the values stored in registers CMPxA and CMPxB. When these values are reached, signals are sent to the action qualifier sub-module, which sets the channels outputs as programmed. The output signals are then sent to the Dead-Band sub-module, which applies the desired dead-time. The final PWM signals are then sent out from the microcontroller by the GPIO peripheral.
To generate complementary driving signals for the bottom and top side devices, the compare values are set to be identical (CMPxA=CMPxB) and the action qualifier is set to generate the signals in a complementary manner.
The phase shift is implemented by synchronizing the two ePWM modules in a particular way. When the time base of ePWM1 reaches zero, a sync-out signal is sent to ePWM2. When this signal is received, the value of the ePWM2 counter is set to the value stored in the TBPHS register. If the wanted phase shift is positive (ePWM2 lags ePWM1), the counter continues counting in the same direction as before the synchronization signal was received. If the wanted phase shift is negative, the counting direction is reversed. In this way, the wanted phase shift with respect to the centre of the duty cycle is easily implemented.
From the microcontroller manual, the PWM period, duty cycles and phase-shift values can be calculated from the register values with the following expressions:

$$T_{PWM} = 2(TBPRD)T_{TB_{clk}} \tag{7.1}$$

$$D_b = 1 - \frac{CMP1A}{TBPRD} - \frac{t_{dead}}{T_{PWM}} \tag{7.2}$$

$$D_h = 1 - \frac{CMP2A}{TBPRD} - \frac{t_{dead}}{T_{PWM}} \tag{7.3}$$

$$D_\varphi = \frac{TBPHS}{2(TBPRD)} \tag{7.4}$$

where $T_{PWM} = \frac{1}{f_{sw}}$ and TB_{clk} is the inverse of the time-base clock frequency, which has been set to 100 MHz. From the above expressions, the register values corresponding to the control parameters are

$$TBPRD = \frac{1}{2f_{sw}(T_{TB_{clk}})} \tag{7.5}$$

$$DBRED = DBFED = \frac{t_{dead}}{T_{TB_{clk}}} \tag{7.6}$$

$$CMP1A = (1 - t_{dead}f_{sw} - D_b)TBPRD \tag{7.7}$$

$$CMP2A = (1 - t_{dead}f_{sw} - D_h)TBPRD \tag{7.8}$$

$$TBPHS = (2D_\varphi)TBPRD \tag{7.9}$$

7.2.3 Experimental results

Some measurements have been carried out on the converter prototype to validate the design and obtain an efficiency profile. The measurement setup is depicted in Figure 7.10.

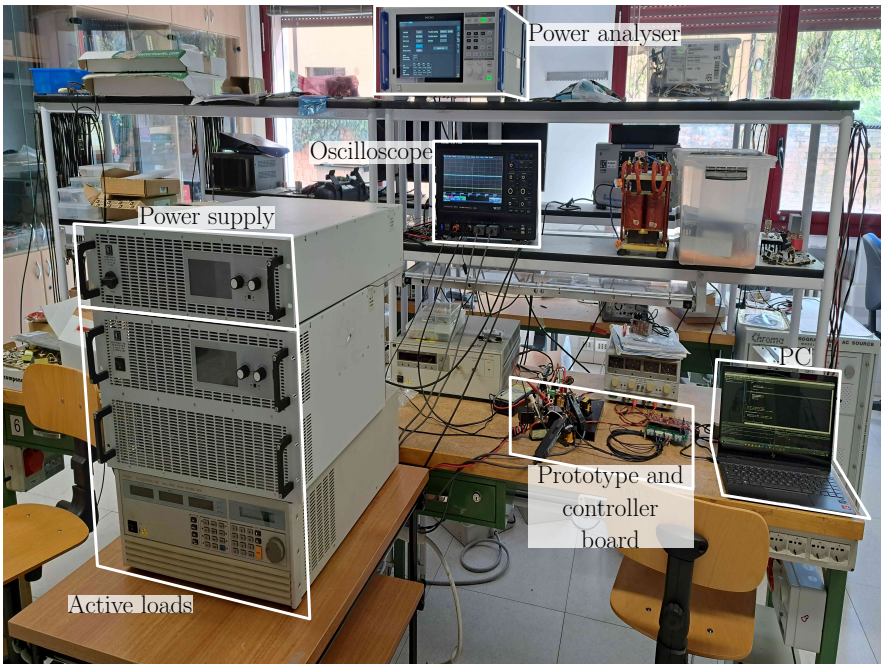


Figure 7.10: Measurement setup used in the lab.

The measurements have been carried out using the active loads in constant resistance mode, to emulate a resistive load, with the power supply connected to the CF-side and the load connected to the VF-side, to evaluate operation at forward power transfer. Using a resistive load allows safe test of the converter, avoiding large changes in load current or voltage, which can easily happen when using a constant voltage or current load.
Separate power supplies have been used for the IBs and microcontroller board, to ensure that no disturbances generated by the converter could reach the controller.
The converter waveforms have been studied using the oscilloscope, which was connected with probes as shown in Figure 7.11.
To acquire the wanted waveforms, the load resistor has been set to dissipate the wanted power (at forward power transfer) at the nominal output voltage, $\left(R_L = \frac{V_H^2}{P}\right)$, then the parameters of the control point needed to achieve the

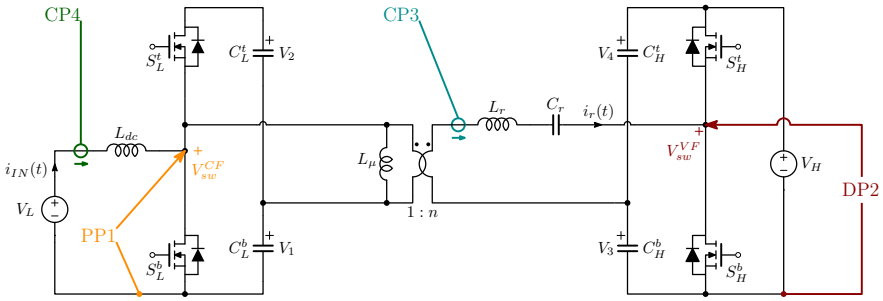


Figure 7.11: Schematic representation of the probe set up used to analyse the converter waveforms.

- Channel 1: 1:100 Passive probe PP1, measuring the CF-side switching node voltage V_{sw}^{CF};
- Channel 2: 1:1000 Differential probe DP2, measuring the VF-side switching node voltage V_{sw}^{VF};
- Channel 3: Current probe CP3, measuring the resonant current i_r;
- Channel 4: Current probe CP4, measuring the input current i_{IN}.

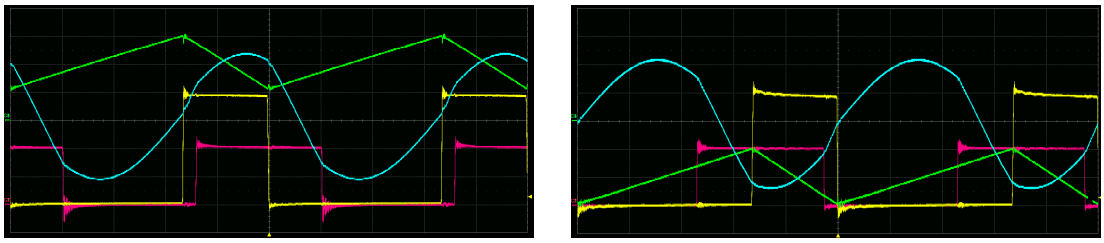
wanted output power must be calculated and set. After that, the input voltage V_L can be increased from zero until the output voltage reaches the desired level.

If the wanted voltages are not reached, the input voltage must be brought back to zero, the control parameters adjusted and the procedure repeated until the obtained voltages reach the desired value.

The procedure is similar to obtain the waveforms at reverse power transfer, but the load must be connected to the CF-side and the power supply must be connected to the CF-side. The load resistor must be calculated as $\left(R_L = \frac{V_L^2}{P}\right)$.

With this procedure, the waveforms at nominal power (in both power transfer directions) shown in Figure 7.12 and 7.13 have been acquired.

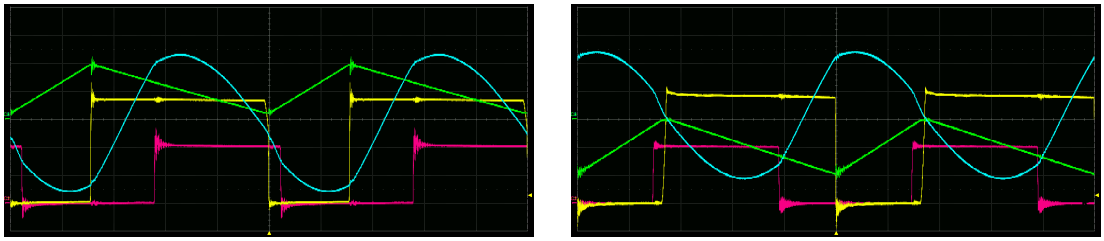
As can be seen from the waveforms, all switches achieve ZVS at turn-on. The oscillations that are present in the switching node voltages (yellow and red oscilloscope traces) are resonances of the parasitic components, triggered during the dead-time by the high commutated currents and $\frac{dv}{dt}$ values.



a) b)

Figure 7.12: Converter waveforms: **a)** $V_L = 253.9$ V, $V_H = 400.9$ V, $P_{out} = 2.5$ kW, $D_b = 0.657$, $D_h = 0.5$, $D_\varphi = 0.126$, **b)** $V_L = 250.4$ V, $V_H = 402.6$ V, $P_{out} = -2.5$ kW, $D_b = 0.657$, $D_h = 0.5$, $D_\varphi = -0.134$
Scope setup:

- CH1: 200 V/div, offset of -600V;
- CH2: 200 V/div, offset of -600V;
- CH3: 10 A/div, no offset;
- CH4: 5 A/div, no offset;
- Time: 5 μs/div, no offset;
- Trigger: Falling edge of CH1, 54 V.



a) b)

Figure 7.13: Converter waveforms: **a)** $V_L = 499.9$ V, $V_H = 400$ V, $P_{out} = 2.5$ kW, $D_b = 0.314$, $D_h = 0.5$, $D_\varphi = 0.15$, **b)** $V_L = 500.1$ V, $V_H = 401.7$ V, $P_{out} = -2.5$ kW, $D_b = 0.314$, $D_h = 0.5$, $D_\varphi = -0.13$
Scope setup:

- CH1: 200 V/div, offset of -600V;
- CH2: 200 V/div, offset of -600V;
- CH3: 10 A/div, no offset;
- CH4: 5 A/div, no offset;
- Time: 5 μs/div, no offset;
- Trigger: Falling edge of CH1, 54 V.

An efficiency profile of the converter has also been obtained, at the two extremes

of the input voltage range and nominal output voltage. The efficiency has been measured using the power HIOKI PW8001 power analyser. The converter efficiency can be calculated (for forward and reverse power transfer respectively) as

$$\eta_{forward} = 100\frac{P_{OUT}}{P_{IN}} \tag{7.10}$$

$$\eta_{reverse} = 100\frac{P_{IN}}{P_{OUT}}. \tag{7.11}$$

where P_{IN} is the power at the CF port and P_{OUT} at the VF port, with positive sign when power is transferred from CF-side to VF-side.
Assuming that the absolute errors on the measurements are not correlated, the absolute error on the efficiency estimation has been calculated as

$$\Delta\eta = \pm 100\sqrt{\sum_{i=1}^{K}\left(\frac{\partial\eta}{\partial X_i}\right)^2 \Delta X_i^2} \tag{7.12}$$

where $K = 2$ and $X_i \in \{P_{IN},\ P_{OUT}\}$. ΔX_i are the absolute errors on the measurements.
For the DC power measurement of the power analyser, these errors can be calculated as:

$$\Delta P = \pm[0.0002P + 0.0003P_{range}] \tag{7.13}$$

Knowing the absolute error on the measurements, the error on the efficiency value can be calculated, using (7.10), (7.11) and (7.12), as

$$\Delta\eta_{forward} = \pm 100\sqrt{\frac{P_{OUT}^2}{P_{IN}^4}\Delta P_{IN}^2 + \frac{1}{P_{IN}^2}\Delta P_{OUT}^2}. \tag{7.14}$$

$$\Delta\eta_{reverse} = \pm 100\sqrt{\frac{P_{IN}^2}{P_{OUT}^4}\Delta P_{OUT}^2 + \frac{1}{P_{OUT}^2}\Delta P_{IN}^2}. \tag{7.15}$$

The measured values are recapped in the following tables.

Table 7.4: Power analyser efficiency measurements at V_L = 250 V, V_H = 400 V. The reported control parameters values were manually adjusted from the ones calculated by using the M-PWL-MCT to obtain the desired transferred power.

	V_L [V]	I_{IN} [A]	V_H [V]	I_{OUT} [A]	P_{IN} [W]	P_{OUT} [W]	η [% ± %]	D_b	D_h	D_φ	R_L [Ω]
500 W	249.9	2.03	401.2	1.19	507.5	477	94 ± 0.12	0.657	0.6	0.006	320
1 kW	250.9	4.19	403.9	2.52	1051	1002	96.9 ± 0.13	0.657	0.6	0.036	160
1.5 kW	250	6.16	400.2	3.75	1545	1502	97.2 ± 0.11	0.657	0.5	0.068	106.67
2 kW	251.7	8.24	401	5.01	2073	2008	96.88 ± 0.10	0.657	0.5	0.095	80
2.5 kW	254	10.2	400.4	6.25	2597	2504	96.44 ± 0.12	0.657	0.5	0.126	64
Reverse power transfer											
-500 W	250.9	-2.01	400.9	-1.34	-504.8	-538.8	93.7 ± 0.065	0.657	0.6	-0.04	125
-1 kW	250.4	-4	400.84	-2.6	-1003	-1042	96.3 ± 0.081	0.657	0.6	-0.06	62.5
-1.5 kW	250.4	-6	400.78	-3.87	-1504	-1549	97.07 ± 0.059	0.657	0.5	-0.078	41.67
-2 kW	251.8	-8.05	400.77	-5.22	-2024	-2089	96.9 ± 0.051	0.657	0.5	-0.104	31.25
-2.5 kW	250.4	-10	402.6	-6.44	-2503	-2503	96.46 ± 0.067	0.657	0.5	-0.134	25

Table 7.5: Power analyser efficiency measurements at V_L = 500 V, V_H = 400 V. The reported control parameters values were manually adjusted from the ones calculated by using the M-PWL-MCT to obtain the desired transferred power.

	V_L [V]	I_{IN} [A]	V_H [V]	I_{OUT} [A]	P_{IN} [W]	P_{OUT} [W]	η [% ± %]	D_b	D_h	D_φ	R_L [Ω]
500 W	501.9	1.07	400	1.28	537	514	95.7 ± 0.12	0.314	0.36	0.012	320
1 kW	508	2.02	400.2	2.5	1030	1001	97.2 ± 0.13	0.314	0.36	0.04	160
1.5 kW	507	3.07	400.4	375	1555	1503	96.7 ± 0.11	0.314	0.5	0.08	106.67
2 kW	500.8	4.16	400.3	4.99	2084	2000	95.9 ± 0.10	0.314	0.5	0.114	80
2.5 kW	500	5.22	400	6.25	2612	2499	95.7 ± 0.12	0.314	0.5	0.15	64
Reverse power transfer											
-500 W	502.2	-0.89	400.9	-1.19	-477	-449	94.2 ± 0.074	0.314	0.36	-0.036	500
-1 kW	500	-1.97	400.8	-2.55	-987	-1021	96.7 ± 0.082	0.314	0.36	-0.058	250
-1.5 kW	500.6	-3	398.8	-3.88	-1505	-1549	97.1 ± 0.059	0.314	0.5	-0.078	166.67
-2 kW	499.9	-3.99	401.8	-5.13	-1998	-2059	97.1 ± 0.051	0.314	0.5	-0.1	125
-2.5 kW	500.1	-4.99	401.7	-6.43	-2498	-2584	96.6 ± 0.067	0.314	0.5	-0.13	100

The peak efficiency of 97.2 ٪ is measured at 1.5 kW (V_L = 250)V and 1 kW (V_L = 500 V) at forward power transfer.

Also from Figure 7.14 it can be seen that, from 1kW to 2.5 kW at forward power transfer, the efficiency at V_L = 500 V is lower with respect to the one obtained at V_L = 250 V. This is counter-intuitive, because one would expect higher efficiency when lower average current is required to deliver the same power. However, from measurements performed on the converter waveforms, the turn-on currents at V_L = 500 V are higher then the ones at V_L = 250 V, especially for S_L^t and S_H^t, increasing switching losses and thus reducing the efficiency.

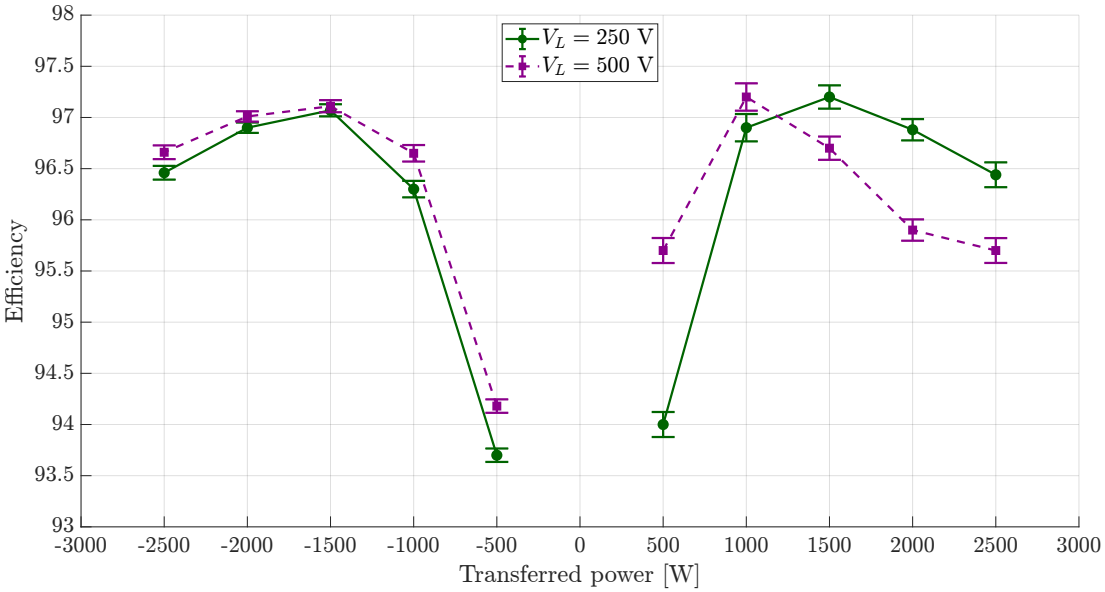


Figure 7.14: Efficiency profile at $V_L = 250$ V and $V_L = 500$ V, $V_H = 400$ V

Regarding the reverse power transfer, it can be seen that the efficiency profile is not symmetrical with respect to the zero-power axis. Furthermore, the efficiency at $V_L = 500$ V is higher that the one at $V_L = 250$ V. The latter can be explained by the lower switched currents that have been measured in the converter, while the non-symmetry of the efficiency can be attributed do the circuit not being perfectly symmetrical regarding power transfer and some differences in the switched currents.

The phase shift values have been decreased from the theoretical ones for all points except $P_{OUT} = 2.5$ kW at $V_L = 500$ V. Needing a lower phase shift than expected to obtain a wanted output power level means that the prototype has a higher power transfer capability. From (A.8) it can be seen that both the values of L_r and f_n influence the transferred power. In fact, lower values of L_r increase both f_n (by reducing the resonant frequency) and the transferred power, if the voltages and control parameters remain constant. Since the resonant capacitance is implemented with film capacitors, which have negligible capacitance non-linearity with respect to the applied voltage, the power overhead can be attributed to the effective resonant inductance value being lower than expected.

Consider, for example, the operating point of Table 7.6.

Starting from (A.8), the following expression can be written

$$\chi = \frac{1}{L_r}\frac{f_n^2}{f_n^2 - 1} = P_{OUT}\frac{\pi^3 f_{sw}}{V_H^2}\frac{1}{|\sin(\pi D_b)|}\frac{1}{|\sin(\pi D_h)|}\frac{1}{\sin(2\pi D_\varphi)} \tag{7.16}$$

Table 7.6: Operating point considered in determining the effective resonant inductance

Parameter	Value
V_L	254
V_H	400.4
P_{OUT}	2504
D_b	0.657
D_h	0.5
D_φ	0.126

which has the dimensions of H^{-1}. Assuming that the resonant capacitance value is constant at $C_r = 46.2$ nF, evaluation of (7.16) at the operating point of Table 7.6 gives $\chi_{OP} = 1.546 \times 10^5\ H^{-1}$. To find the effective value of the resonant inductance, the following equation can be solved numerically

$$\chi_{eff} = \frac{1}{L_{r,eff}} \frac{(2\pi f_{sw}^2) L_{r,eff} C_r}{(2\pi f_{sw}^2) L_{r,eff} C_r - 1} = \chi_{OP}. \tag{7.17}$$

Still assuming that C_r is constant, the obtained resonant inductance value is $L_{r,eff} = 20.17\ \mu$H, which is lower than the expected one. With this inductance value, there is a good match between the measured current and power values and the theoretical ones at the operating point.

Chapter 8

Proposed control scheme

In this chapter, a control scheme for the SR-CFDHB is proposed. The controlled variables are the two duty-cycles (D_b and D_h) and the phase shift D_φ.
As it can be seen from Figure 8.1, the control system is composed by two sections:

- The Boost cell output voltage controller
- The output voltage control loop

The Boost controller aims to keep the flat-top condition discussed in chapter 4, while the objective of the output voltage control loop is to maintain a constant output voltage.

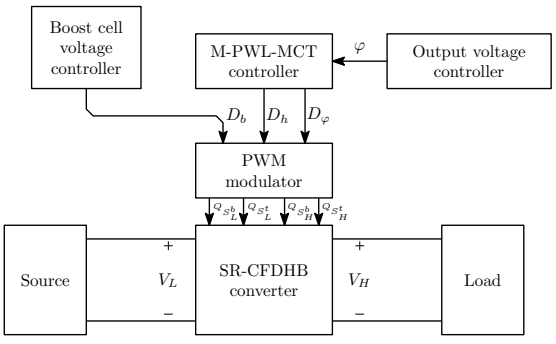


Figure 8.1: Block diagram of the control system

8.1 Boost cell voltage controller

As can be seen from Figure 8.2, the boost voltage control can be implemented as e feedback loop, regulating the integrated Boost cell output voltage $V_B = V_1 + V_2$.

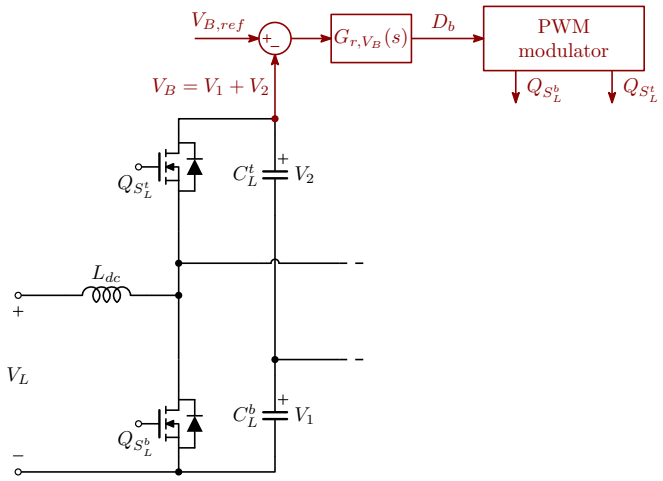


Figure 8.2: Boost voltage control loop

The voltage reference for the controller can be computed as

$$V_{B,ref} = \frac{V_H}{n} \tag{8.1}$$

in order to obtain the flat-top condition $D_b = 1 - n\frac{V_L}{V_H}$.

8.2 Output voltage controller

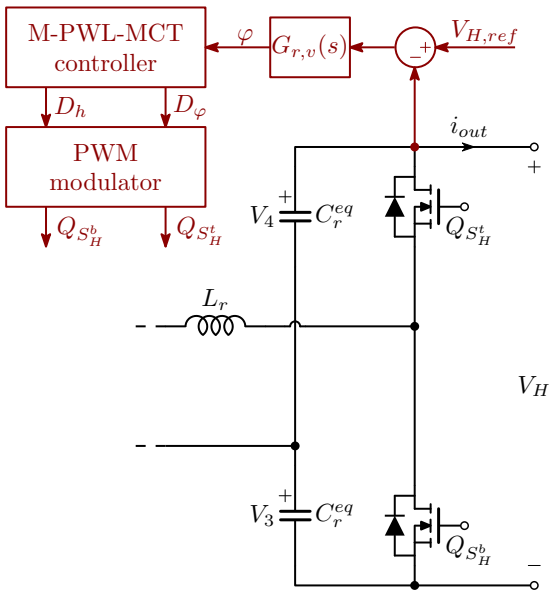


Figure 8.3: Output voltage control loop

The output voltage controller (Figure 8.3) provides to the trajectory controller the proper phase-shift value to maintain a constant output voltage.
Depending on the load, the regulator $G_{r,v}(s)$ must be designed to regulate the output power or the output current.

8.2.1 M-PWL-MCT controller

The trajectory controller receives the phase shift produced by the voltage controller and outputs the corresponding value of D_φ and D_h as shown in Figure 8.4. As explained in chapter 4, D_h is calculated from D_φ as defined by the M-PWL-MCT. The values of the trajectory parameters depend on the relative values of V_L and V_H. In particular, for $\frac{V_H}{V_L} \leqslant 1$, D_{sat} (so in step-down mode) is between 0 and 0.5, while $0.5 \leqslant D_{sat} \leqslant 1$ holds in step-up mode $\left(\frac{V_H}{V_L} \geqslant 1\right)$.

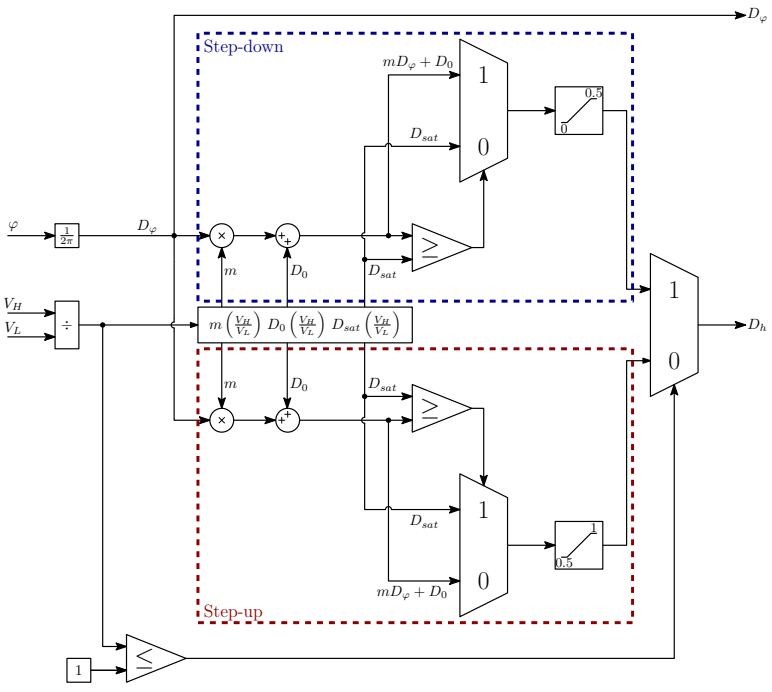


Figure 8.4: M-PWL-MCT controller

To understand the working principle of the trajectory controller, let's look at the step-down case. At first, the value of D_{sat} and $mD_\varphi + D_0$ are calculated based on V_H/V_L. These values are then compared: since the value of D_h in the trajectory ranges in $[0; 0.5]$, the greater one between D_{sat} and $mD_\varphi + D_0$ is passed on to the limiter block. This block avoids the crossing of the allowed value range.
The dual procedure happens in the step-up case: the trajectory ranges in $[0.5; 1]$,

so the smaller one between D_{sat} and $mD_{\varphi} + D_0$ is passed to the limiter.
The M-PWL-MCT changes with the input voltage, so the expressions $m\left(\frac{V_H}{V_L}\right)$, $D_0\left(\frac{V_H}{V_L}\right)$ and $D_{sat}\left(\frac{V_H}{V_L}\right)$ must be obtained.
The procedure to find these equations consists in calculating the M-PWL-MCT and its parameters for different input voltage levels. After that, polynomial fits can be performed to obtain the expressions.
As said previously, this approach allows to control the converter by completely avoid the use of LUTs, thus greatly simplifying the control implementation.

Chapter 9

Conclusions and further developments

The converter has firstly been analysed under four degrees of freedom. In the end, the switching frequency was excluded from the control parameters, due to the complexity in finding an optimal control strategy employing all four parameters. The developed theoretical framework is validated by simulations and experimental results, with some variations due to parasitic elements and component non-idealities.

Due to time limitations, an optimal design of the converter has not been done. For example, the high commutated currents could be reduced by optimizing the dead-time interval durations and component values. Nonetheless, the prototype achieves acceptable levels of efficiency in a reasonably wide power range. The possible future developments include optimization of the existent design and experimental implementation of the proposed control architecture. The prototype built in the laboratory allows quick easy testing of modifications and the developed microcontroller code can be a starting point to implement a closed-loop control for the converter.

Appendix A

SR-CFDHB under the FHA

Since the normalized power and RMS current equations depend on the converter operating mode, and subsequently on the relative values of the three control variables (D_b, D_h, D_φ), obtaining reasonable expressions for Π_t and J_{RMS} is quite the task.
This simplification is achieved by using the Fundamental Harmonic Approximation (FHA), which approximates the rectangular waveforms generated by the two half-bridges with their sinusoidal fundamental frequency component.
For what concerns the fundamental component, the Fourier series analysis of the half-bridges' output waveforms is equivalent to the one corresponding to the waveform of Figure A.1. The amplitude of the rectangular wave is V_B for the current-fed side half bridge, while its value is V_H for the voltage-fed side.

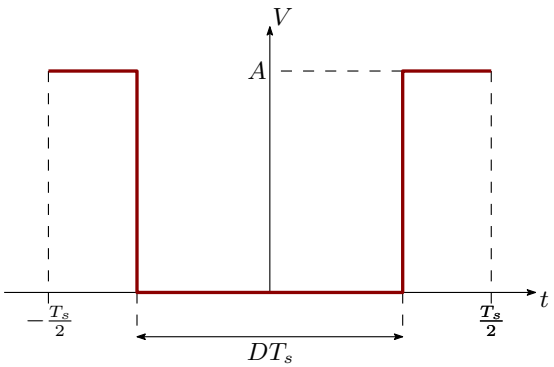


Figure A.1: Equivalent waveform used for the Fourier analysis

The Fourier series analysis gives the following expressions for the fundamental components of the two bridges' output voltages:

$$\begin{cases} v_a(t) \cong -\frac{2}{\pi}\frac{nV_L}{1-D_b}\sin(\pi Db)\cos(\omega_s t) \\ v_b(t) \cong -\frac{2}{\pi}V_H \sin(\pi D_h)\cos(\omega_s t - \varphi) \end{cases} \tag{A.1}$$

where $\varphi = 2\pi D_\varphi$.
The peak values of the fundamental components thus are

$$\begin{cases} V_a^{pk} = \frac{2}{\pi}\frac{nV_L}{1-D_b}|\sin(\pi D_b)| \\ V_b^{pk} = \frac{2}{\pi}V_H|\sin(\pi D_h)| \end{cases} \tag{A.2}$$

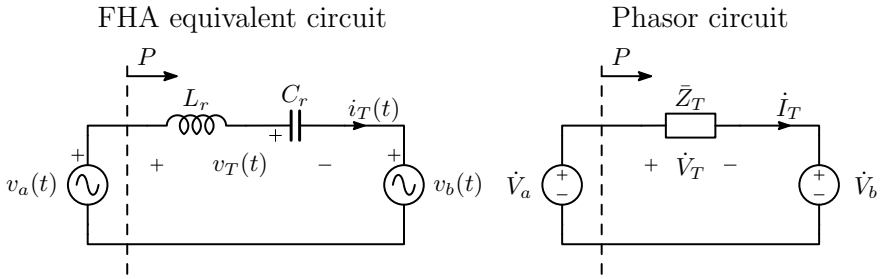


Figure A.2: Equivalent circuits for the SRCFDHB converter under FHA

By using the phasorial representation of Figure A.2, where the magnitude of the phasor represents the RMS value of the represented signal, the apparent power can be expressed as

$$\dot{S} = \dot{V}_a \dot{I}_T^*. \tag{A.3}$$

The tank voltage and impedance are

$$\dot{V}_T = \dot{V}_a - \dot{V}_b \tag{A.4}$$

$$\dot{Z}_T = jZ_r\frac{f_n^2 - 1}{f_n} = jZ_T \tag{A.5}$$

which yield the tank current phasor expression of A.6.

$$\dot{I}_T = \frac{\dot{V}_T}{\dot{Z}_T} = \frac{V_b \sin\varphi + j(V_b\cos\varphi - V_a)}{Z_T} \tag{A.6}$$

The active power can be calculated as the real part of the apparent power, resulting in A.7.

$$P = \mathrm{Re}\left[\dot{S}\right] = \frac{V_a V_b}{|Z_T|}\sin\varphi. \tag{A.7}$$

Being the amplitude of a phasor the RMS value of the corresponding sinusoidal signal, the transferred power can be calculated from A.7 by using A.2.

$$\begin{aligned} P_t^{FHA} &= \frac{1}{|Z_T|}\frac{V_a^{pk}V_b^{pk}}{2}\sin(2\pi D_\varphi) \\ &= \frac{2nV_LV_H}{\pi^2(1-D_b)}\frac{1}{|Z_T|}|\sin(\pi D_b)||\sin(\pi D_h)|\sin(2\pi D_\varphi) \\ &= \frac{nV_LV_H}{\pi^3(1-D_b)f_{sw}}\frac{f_n^2}{L_r(f_n^2-1)}|\sin(\pi D_b)||\sin(\pi D_h)|\sin(2\pi D_\varphi). \end{aligned} \tag{A.8}$$

Similarly, the tank RMS current can be calculated from A.6 as

$$\left|\dot{I}_T\right| = \frac{1}{|Z_T|}\sqrt{V_a^2+V_b^2-2V_aV_b\cos\varphi} = \frac{1}{|Z_T|}\frac{\sqrt{2}V_H}{\pi}f(M,D_b,D_h,D_\varphi) \tag{A.9}$$

where

$$f(M,D_b,D_h,D_\varphi) = \sqrt{\begin{aligned}&\left[\frac{1}{M(1-D_b)}\right]^2\sin^2(\pi D_b)+\sin^2(\pi D_h) \\ &-\frac{2}{M(1-D_b)}|\sin(\pi D_b)||\sin(\pi D_h)|\cos(2\pi D_\varphi)\end{aligned}} \tag{A.10}$$

where $M = \frac{1}{n}\frac{V_H}{V_L}$ is the converter voltage conversion ratio.
Finally, the normalized transferred power and the inductor RMS current under the FHA can be calculated as follows:

$$\Pi_t^{FHA} = \frac{2}{M\pi^2(1-D_b)}\frac{f_n}{f_n^2-1}|\sin(\pi D_b)||\sin(\pi D_h)|\sin(2\pi D_\varphi) \tag{A.11}$$

$$J_{RMS}^{FHA} = \frac{\sqrt{2}}{\pi}\frac{f_n}{f_n^2-1}\sqrt{\begin{aligned}&\left[\frac{1}{M(1-D_b)}\right]^2\sin^2(\pi D_b)+\sin^2(\pi D_h) \\ &-\frac{2}{M(1-D_b)}|\sin(\pi D_b)||\sin(\pi D_h)|\cos(2\pi D_\varphi).\end{aligned}} \tag{A.12}$$

It is easy to see that, if D_b is kept at a constant value $D_b = \tilde{D}_b$, the maximum power $\Pi_{t,max}$ is achieved at $(\tilde{D}_b, D_h = 0.5, D_\varphi = 0.25)$ in the positive direction

and at $(\tilde{D}_b, D_h = 0.5, D_\varphi = -0.25)$ in the negative direction.
To validate the FHA, the relative error introduced by the approximation can be calculated using A.13. This error can then be averaged in a range of (D_h, D_φ) values (e.g. $D_h \in [0; 1]$ and $D_\varphi \in [-0.25; 0.25]$) to obtain the average relative error resulting from the FHA. Repeating this procedure for some D_b values results in the plot of Figure A.3.

$$\varepsilon_{FHA} \triangleq \left| \frac{X - X_{FHA}}{X} \right|, \text{ where } X = \{\Pi_t, J_{RMS}\} \tag{A.13}$$

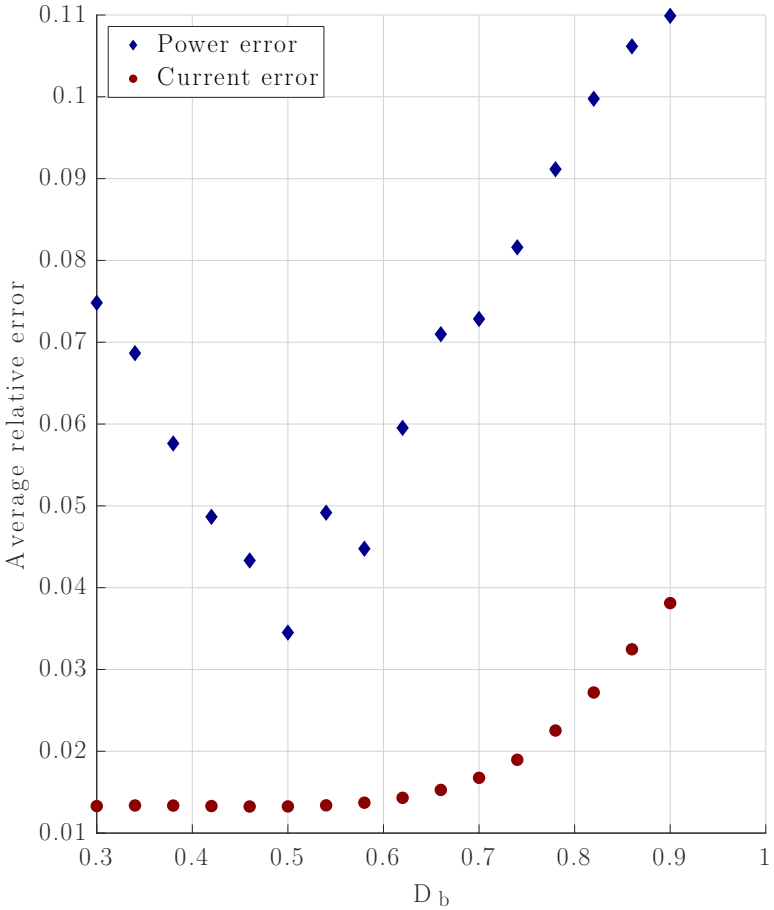


Figure A.3: Average relative error on the FHA at different values of D_b

In the considered D_b range, the error on the average power is around 7% while the current averages an error around 1.83%. This means that, especially for the tank RMS current, the FHA provides a good estimation.

Appendix B

Losses mechanisms in magnetic components

In this appendix, the main mechanisms which lead to losses in magnetic components are presented and explained, to gain better insight into the design of the magnetic components employed in the converter.

B.1 Core losses

In a ferromagnetic material, the atomic interactions lead to spontaneous magnetization. However, a macroscopic material is divided into Weiss domains, separated by the so called Bloch walls. Inside each domain, the atoms' magnetic moments (resulting from the electrons rotation around the nucleus) are oriented in the same direction.

When no external magnetic field is applied, the magnetization resulting from all the domains is zero, so that the material is at minimum energy.

If an external magnetic field is applied to the material, the domain walls shift and the net magnetization becomes non-zero. After magnetization, the material magnetization curve is similar to the one shown in Figure B.1.

During the magnetization process, rapid jumps of the Bloch walls cause losses, by leading to localized eddy currents and thus heating of the material. Because of this, the magnetization process is irreversible [7].

The energy required to change the material magnetization from a to b is given by

$$W_{ab} = \int_a^b H dB \tag{B.1}$$

When the applied magnetic field is periodic $\left(\oint H dH = 0\right)$, the lost energy per

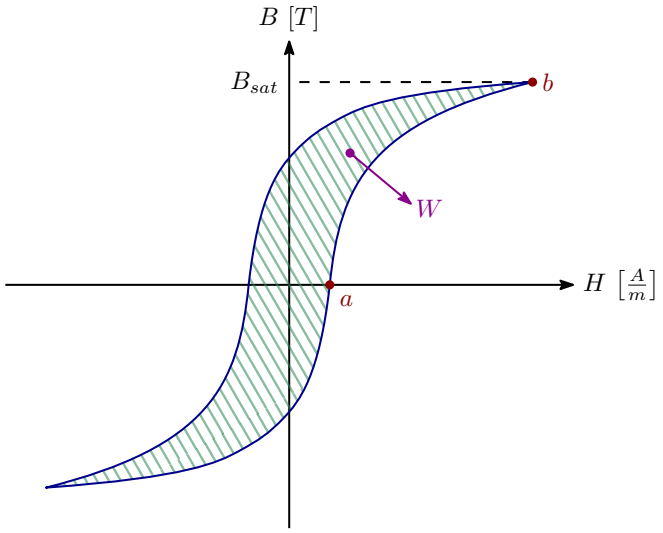


Figure B.1: Typical hysteresis loop of a ferromagnetic material

closed loop can be calculated as

$$W = \oint H dB \tag{B.2}$$

If the magnetic flux density variation does not span the entirety of the $[-B_{sat}; B_{sat}]$ range, a secondary loop can be considered when calculating this energy.
This is the main loss mechanism in modern core materials. Note that the eddy currents that cause these losses are not the macroscopic scale eddy currents usually discussed when talking about magnetic materials. The latter are minimized in modern materials by lamination or by building the core with small, bounded and individually insulated particles, so that the available area for eddy currents to circulate is reduced.
The most common method to evaluate core losses is the Steinmetz equation

$$P_V = C_m f^x \hat{B}_{pk}^y \left[\frac{W}{m^3}\right]. \tag{B.3}$$

$\hat{B}_{pk}$ is the peak magnetic flux density under sinusoidal excitation and f is the operating frequency. Plots of P_V as function of f and B_{pk} are commonly available in core data-sheets, thus fitting of these plots can be used to determine the Steinmetz coefficients C_m, x and y.
This method allows easy estimation of core losses. However, since in power electronic converters the excitation waveforms are rarely sinusoidal in nature, this approach leads to some error in the estimated power loss.

B.2 Copper losses

In an inductor or a transformer winding, non-constant current flows in conductors that are close together and invested by a magnetic field. The two leading causes of conductor losses are:

1. The skin effect
2. The proximity effect

As it will be seen, both of these effects reduce the available conductor section, thus increasing resistance and losses. The effects of these mechanisms can be modelled by the correcting factor

$$F_R = \frac{R_{AC}}{R_{DC}}. \tag{B.4}$$

For windings in which the current presents a DC component, the copper losses related to this components is simply the power dissipated by Joule effect on the conductor resistance. The losses due to high-frequency (e.g. power electronic converters switching frequency) components are the Joule losses on the resistor $R_{AC} = F_R R_{DC}$.

B.2.1 Skin effect

A changing current flowing in a conductor induces a varying magnetic field. This field will induce eddy currents in the conductor, which will generated a field opposite to the one induced by the current $i(t)$, as shown in Figure B.2.

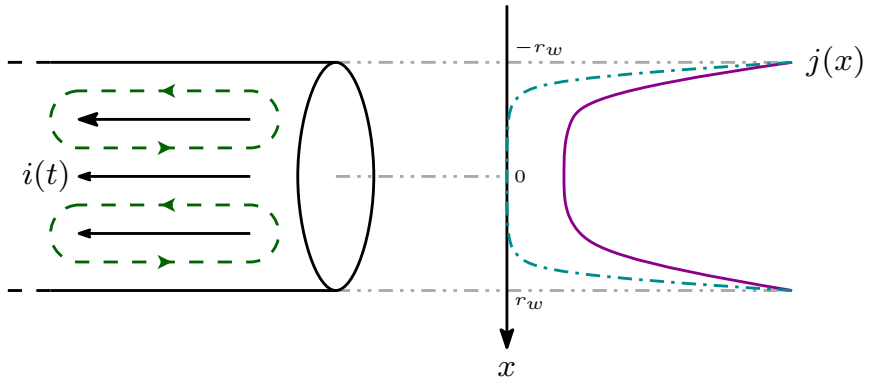


Figure B.2: Induced eddy currents (indicated by the green dashed loops) in a round conductor and resulting current density. The dash-dotted line in the right-hand plot represents the situation where a higher frequency current $i(t)$ flows in the conductor

The induced currents sum with the original current at the periphery of the conductor while subtracting at the inside, reducing the effective conductor area and creating a non-uniform current distribution.
The severity of this effect increases with frequency, depending on the penetration depth

$$\delta = \sqrt{\frac{\rho}{\pi \mu_r \mu_0 f}} \tag{B.5}$$

B.2.2 Proximity effect

The proximity effect manifests itself when two conductors crossed by a current are close to each other, as shown in Figure B.3.

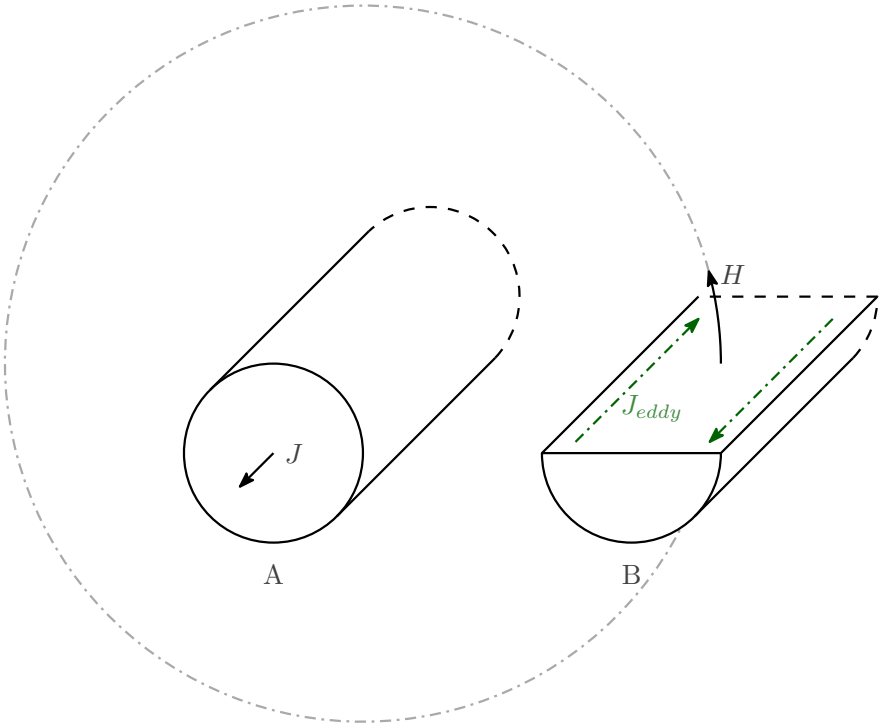


Figure B.3: Currents induced by the proximity effect (green dashed lines)

Parasitic currents are induced in conductor B. These currents have the opposite sign as J in the A-facing side, while the contrary happens at the opposite side of conductor B. If in B flows current equal and opposite to the one in conductor A, the currents will concentrate on sides of the conductor which face each other. This, again, reduces the available conductor surface area, increasing resistance.

B.2.3 Copper losses in a multi-winding magnetic component

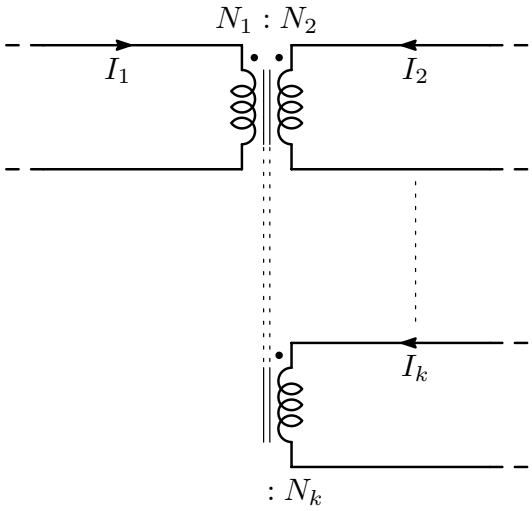


Figure B.4: General multi-winding magnetic component

The copper (wire) losses for a general, multi-winding magnetic component can be calculated starting from the Joule effect losses on the windings resistances.

$$P_{Cu,TOT} = \sum_{j=1}^{k} I_j^2 R_j \text{ where } R_j = \rho \frac{l_j}{A_{w,j}} \tag{B.6}$$

where I_j is the j-th winding RMS current, l_j is the wire length of winding j, $A_{w,j}$ is the copper cross-section of the wire, k is the total number of windings and ρ is the copper resistivity at the operating temperature. l_j and $A_{w,j}$ can be expressed as

$$l_j = (MLT)N_j \tag{B.7}$$

$$A_{w,j} = \frac{W_A K_u \alpha_j}{N_j},\ 0 \leqslant \alpha_j \leqslant 1 \tag{B.8}$$

where MLT is the core's mean turn length, W_A is the core window area, N_j is the number of turns of the j-th winding, α_j is the fraction of the window area allocated to winding j and K_u is the window utilization factor.
The window utilization factor K_u is a number between zero and one that is used to take into account that round wires don't pack perfectly and that some window area is taken up by the coil former and insulation.

Substituting (B.7) and (B.8) into (B.6) gives the following expression for the total wire losses

$$P_{Cu,TOT} = \rho \frac{MLT}{W_A K_u} \sum_{j=1}^{k} \left(\frac{N_j^2 I_j^2}{\alpha_j} \right). \tag{B.9}$$

As explained in [6], the value of α_j heavily influences the copper losses. Optimum values of α_j can be found through Lagrange multipliers minimization.
The equation to be minimized is (B.9), under the following constraint

$$\begin{aligned} &0 < \alpha_j < 1 \\ &\alpha_1 + \alpha_2 + \cdots + \alpha_k = 1 \end{aligned} \tag{B.10}$$

The following function is defined

$$f(\alpha_1, \alpha_2, \cdots, \alpha_k, \nu) = P_{Cu,TOT}(\alpha_1, \alpha_2, \cdots, \alpha_k) + \nu g(\alpha_1, \alpha_2, \cdots, \alpha_k) \tag{B.11}$$

where

$$g(\alpha_1, \alpha_2, \cdots, \alpha_k) = 1 - \sum_{j=1}^{k} \alpha_j \tag{B.12}$$

is the constraint that must equal zero and ν is the Lagrange multiplier. The optimum point is found by solving the following system of equations

$$\begin{cases} \frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \nu)}{\partial \alpha_1} = 0 \\ \frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \nu)}{\partial \alpha_2} = 0 \\ \vdots \\ \frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \nu)}{\partial \alpha_k} = 0 \\ \frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \nu)}{\partial \nu} = 0 \end{cases} \tag{B.13}$$

Solving this system gives

$$P_{Cu,TOT} = \nu = \rho \frac{MLT}{W_A K_u} \left(\sum_{j=1}^{k} N_j I_j \right)^2 = \rho \frac{N_1^2 MLT}{W_A K_u} \left(\sum_{j=1}^{k} \frac{N_j}{N_1} I_j \right)^2 \tag{B.14}$$

and

$$\alpha_m = \frac{N_m I_m}{\sum_{j=1}^{k} N_j I_j} = \frac{V_m I_m}{\sum_{j=1}^{k} V_j I_j} \text{ where } m \in [1, 2, \cdots, k]. \tag{B.15}$$

(B.15) states that the window area portion for each winding needs to be allocated according to the winding's apparent power. In fact, the numerator of (B.15) is the m-th winding apparent power and the denominator is the sum of all the apparent powers. When the window areas are allocated in this way, the copper losses are minimized and are given by (B.14).

B.3 Losses in a winding employing Litz wire

A Litz wire is a particular kind of conductor made of a number on thin strands, which are twisted around the centre of the conductor. This means that each strand occupies every portion of space throughout the length of the conductor. This reduces the proximity effect at the conductor level.
The fact that the conductor is made of multiple thin strands, instead, reduces the skin effect.

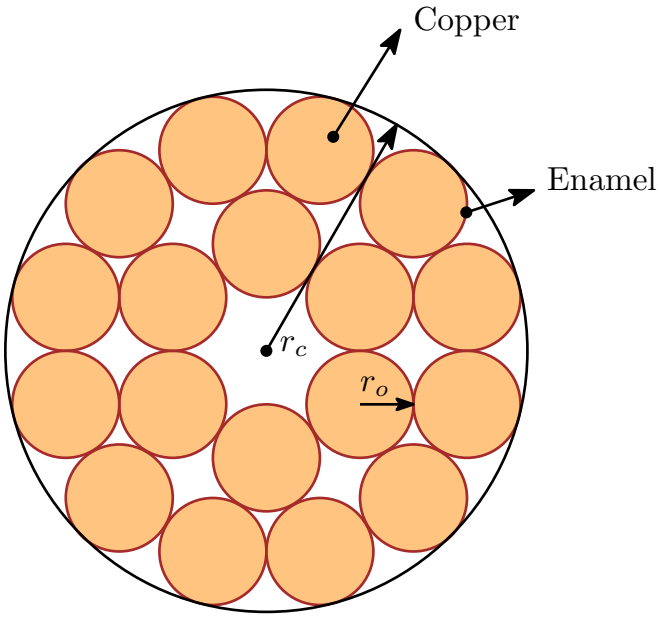


Figure B.5: Simplified cross section of a Litz wire

The relevant parameters of a multi-layer winding composed by Litz wire are:

- N_t: number of turns per layer;
- m: number of layers;
- N_s: number of strands in a conductor;
- r_o: radius of a strand;
- r_c: radius of the conductor;
- l_w: core window height.

To evaluate the AC losses in a winding employing Litz wire, the formulation of F_R found in [3] is used. The approach, based on [8], is briefly summarized here. Starting from the Maxwell equation, under the assumptions of zero external magnetic field and sinusoidal quantities, the losses per unit length due to skin effect in a round conductor of radius r_o can be expressed as

$$P_C^{skin} = \frac{|\dot{I}_o|^2}{2\pi\sigma\delta d_o}\psi_1(\xi) \tag{B.16}$$

where δ is the penetration depth from (B.5), $\dot{I}_o$ is the phasor corresponding to the wire current, $\sigma = 1/\rho$ is the copper conductivity and

$$\xi = \frac{d_o}{\delta\sqrt{2}} \tag{B.17}$$

$$\psi_1(\xi) = \frac{ber_0(\xi)bei_1(\xi) - ber_0(\xi)ber_1(\xi) - bei_0(\xi)bei_1(\xi) - bei_0(\xi)ber_1(\xi)}{ber_1^2(\xi) + bei_1^2(\xi)}. \tag{B.18}$$

(B.16) can be rewritten considering the DC resistance per unit length $r_{DC} = \frac{4}{\sigma\pi d_o^2}$

$$P_C^{skin} = \frac{1}{2}r_{AC}|\dot{I}_o|^2 = \frac{1}{2}F_R r_{DC}|\dot{I}_o|^2, \text{ where } F_R = \frac{\xi}{2\sqrt{2}}\psi_1(\xi). \tag{B.19}$$

Considering a round conductor invested by a uniform external magnetic field allows to compute the losses per unit length due to proximity effect as

$$P_C^{prox} = \frac{1}{2}r_{DC}G_R|\dot{H}|^2 \tag{B.20}$$

where

$$G_R = \frac{\xi\pi^2 d_o^2}{\sqrt{2}}\psi_2(\xi) \tag{B.21}$$

$$\psi_2(\xi) = \frac{ber_1(\xi)bei_2(\xi) - ber_1(\xi)ber_2(\xi) - bei_1(\xi)bei_2(\xi) - bei_1(\xi)ber_2(\xi)}{ber_0^2(\xi) + bei_0^2(\xi)}. \tag{B.22}$$

Finally, the copper losses in a winding employing Litz wire can be computed starting from (B.19) and (B.20) and following the approach in [9].

The approach uses the following simplifying assumptions: the current divides equally between the strands, the magnetic field inside the wire is only in the φ direction and the external magnetic field is only along the z axis (referencing

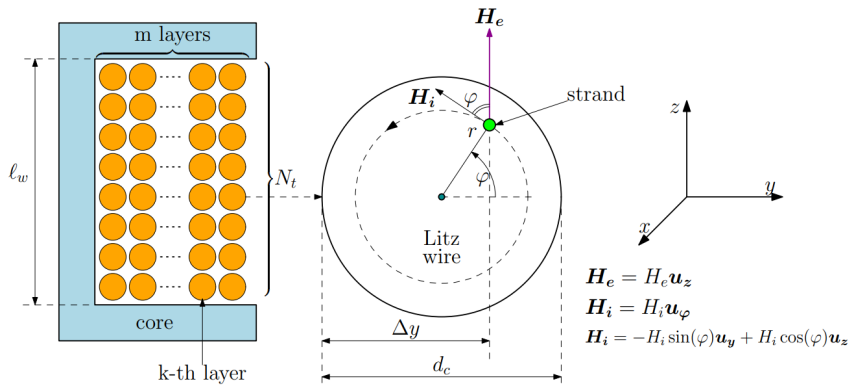


Figure B.6: Analysed structure of a winding employing Litz wire. The conductor is assumed to be infinitely long in the x direction.

Figure B.6).

Calculation of the total copper losses due to both skin and proximity effect results in the following formulation of F_R.

$$F_R = \frac{\xi}{2\sqrt{2}} \left\{ \psi_1(\xi) + \left[\frac{8N_s^2\pi^2 r_o^2 N_t^2 m^2}{3l_w^2} + N_s^2 \frac{r_o^2}{r_c^2} \left(1 - \frac{\pi^2 r_c^2 N_t^2}{6l_w^2} + \frac{\pi r_c N_t}{l_w} \right) \right] \psi_2(\xi) \right\}. \tag{B.23}$$

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