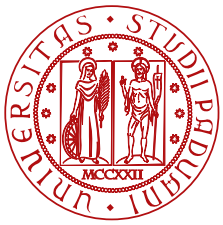

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DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

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Evaluation of an adaptive driving beam system used in automotive front light applications

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Be the change that you wish to see in the world.
To my family and friends.

Sommario

Questa tesi di laurea si concentra sulla ”Valutazione di un sistema di guida adattiva del fascio luminoso (ADB) utilizzato nelle applicazioni di illuminazione frontale automobilistica”. In un contesto dove la sicurezza stradale e l’efficienza luminosa sono di crescente importanza, i sistemi ADB rappresentano una tecnologia all’avanguardia, capace di adattare dinamicamente il pattern luminoso dei fari veicolari per massimizzare l’illuminazione della strada senza abbagliare gli altri utenti.

Nel capitolo 1 (”Theory Notes”) vengono esplorati i principi fondamentali che sottostanno al funzionamento di tali sistemi, con un’attenzione particolare alle tecnologie chiave come i LED (Light Emitting Diode) e ai convertitori DC-DC, indispensabili per l’efficiente gestione dell’energia e il controllo della luce.

In seguito, nel capitolo 2 (”Software Development”) viene descritto il codice usato per il funzionamento del dispotivo fornito da Infineon, un carico di LEDs, dove è possibile osservare il comportamento dei LED grazie al matrix manager installatovi nel carico.

Nel capitolo 3 (”Simulations”) vengono presentate delle simulazioni di controllo, con particolare attenzione al comportamento del driver TLD6099-2ES. Viene effettuata un’analisi delle forme d’onda e dell’effetto della variazione della capacità di uscita.

Attraverso l’analisi delle diverse strategie di protezione ESD (Electrostatic Discharge) illustrate nel capitolo 4 (”LAB Measurements”) la tesi evidenzia l’importanza cruciale della robustezza e dell’affidabilità dei componenti elettronici che costituiscono questi sistemi avanzati. Si fornisce un’analisi comparativa delle diverse tipologie di protezione, valutando il loro impatto sulla durabilità e sulle performance dei dispositivi in scenari operativi reali. Vengono valutati due tipi di configurazione hardware, e confrontati in seguito.

L’obiettivo finale di questo studio è fornire una comprensione approfondita delle potenzialità e delle complessità dei sistemi ADB, contribuendo a delineare future direzioni di ricerca e sviluppo nel campo dell’illuminazione automobilistica intelligente.

Abstract

This thesis focuses on the *”Evaluation of an Adaptive Driving Beam (ADB) System Used in Automotive Front Lighting Applications”*. In a context where road safety and lighting efficiency are becoming increasingly important, ADB systems represent a cutting-edge technology capable of dynamically adapting the light beam pattern of vehicle headlights to maximize road illumination without dazzling other road users.

In Chapter 1 (”Theory Notes”), the fundamental principles underlying the operation of such systems are explored, with particular attention to key technologies such as LEDs (Light Emitting Diodes) and DC-DC converters, which are essential for efficient energy management and light control.

Subsequently, Chapter 2 (”Software Development”) describes the code used for the operation of the device provided by Infineon, a LED load, where the behavior of the LEDs can be observed thanks to the matrix manager installed within the load.

Chapter 3 (”Simulations”) presents control simulations, focusing in particular on the behavior of the TLD6099-2ES driver. An analysis is conducted on the waveforms and the effects of varying the output capacitance.

Through the analysis of different Electrostatic Discharge (ESD) protection strategies illustrated in Chapter 4 (”LAB Measurements”), the thesis highlights the crucial importance of robustness and reliability of the electronic components that make up these advanced systems. A comparative analysis of different types of protection is provided, evaluating their impact on the durability and performance of the devices in real-world operating scenarios. Two types of hardware configurations are evaluated and subsequently compared.

The ultimate goal of this study is to provide an in-depth understanding of the potential and complexities of ADB systems, contributing to shaping future research and development directions in the field of intelligent automotive lighting.

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Introduction

Vehicle lighting technology has undergone remarkable development over the past century. From the rudimentary glow of incandescent bulbs to today's fully adaptive, software-controlled digital headlamps, the role of lighting in automobiles has evolved beyond simple visibility [1]. As vehicles become increasingly connected, autonomous and electrified, the demand for intelligent lighting systems capable of enhancing safety and user experience has grown rapidly. Among the most prominent solutions addressing these needs are Automotive Adaptive Lighting Systems. Among the most prominent solutions addressing these need are Automotive Adaptive Lighting Systems, particularly Adaptive Driving Beam (ADB) technologies, which rely heavily on advanced LED-based innovations.

The journey of automotive lighting began with basic incandescent lamps. Through they were dependable for the time, their efficiency and durability left much to be desired. In the 1990s, halogen lamps provided an incremental improvement, offering better brightness and somewhat longer lifespan. However, the true transformation in vehicle lighting came with the introduction of Light Emitting Diode (LED) technology. LEDs offered a range of advantages that made them ideally suited for automotive applications: they are highly energy-efficient, boast long operation lifespans, turn on instantly and allow for compact and flexible design integration. These features have not only replaced older technologies but also enabled entirely new lighting architectures [2].

At the core of modern LED operation lies the principle of electroluminescence. When an electric current passes through the diode's semiconductor material, electrons recombine with holes, releasing energy in the form of photons. This light emission process is far more efficient than the thermal radiation mechanisms used in incandescent or halogen bulbs. Additionally, LEDs can be modulated with high-speed control techniques such as pulse-width modulation (PWM), making them suitable for intelligent systems that require dynamic brightness and directional control.

In recent years, Adaptive Driving Beam systems have emerged as a groundbreaking development in automotive lighting. These systems mark a departure from traditional headlights that rely on static low and high beams toggled manually by the driver. Instead, ADB systems contin-

uously adapt the headlight beam pattern in real time based on several factors, including vehicle speed, steering angle, road curvature and the presence of other road users. ADB headlights enhance visibility for the driver while reducing glare for oncoming traffic, thereby improving overall read safety without requiring any input form the driver. One of the key enablers of ADB functionality is the matrix LED headlamp [3]. Unlike conventional headlamp systems that use a single light source per beam, matrix LEDs consist of an array of small, individually controllable light elements arranged in a grid. Each LED or pixel in the array can be dimmed or turned off independently, allowing the system to sculpt the light beam with remarkable precision. This fine-grained control is handled by a dedicated module known as the matrix manager. Acting as an intermediary between the vehicle's sensors and the LED array, the matrix manager determines the optimal activation state for each individual LED segment. It modulates brightness levels using high-frequency PWM signals, selectively dims or deactivates specific pixels, and ensures smooth transitions in the beam pattern. Additionally, it manages thermal protection and monitors system diagnostics to maintain reliable operation under varying driving conditions.
This makes it possible to illuminate road signs, pedestrians, or curves ahead while simultaneously masking out sections of the beam to avoid blinding oncoming drivers. The result is a lighting system that offers both maximum illumination and optimized safety.
The adaptive functionality of these systems is achieved through a tightly integrated network of sensors and control electronics. Front-facing cameras and radar systems detect oncoming vehicles and obstacles, while steering angle sensors and GPS data provide contextual awareness about the vehicle's position and movement. This information is processed by a dedicated lighting control unit that executes software algorithms to determine the appropriate lighting response. The control unit then adjusts the LED output accordingly, managing power delivery, voltage levels, and PWM signals to ensure precise control over the light distribution.
Modern headlight systems have thus become far more than just illumination tools—they are complex mechatronic systems that interface with the vehicle's network architecture. This includes integration with the CAN and LIN communication protocols, as well as interaction with other electronic control units (ECUs) involved in advanced driver-assistance systems (ADAS). In many cases, the software controlling these lighting systems is updatable via over-the-air firmware updates, allowing manufacturers to improve system performance or add new features after the vehicle has been sold. This level of adaptability is particularly crucial for electric and autonomous vehicles, where the efficiency and intelligence of every subsystem—including lighting—are paramount. As regulations in regions like Europe and Japan begin to accommodate these new technologies, ADB systems are becoming more widespread in production vehicles. The use of adaptive lighting not only improves night-driving comfort but also plays a critical role in the safety architectures of autonomous driving platforms.

The future of automotive lighting is likely to see even more integration of advanced technologies such as laser light sources, OLED displays, and digital micromirror devices (DMDs), further pushing the boundaries of what headlamps can achieve. However, the foundation for this future has been firmly laid by the combination of LED advancements, matrix lighting architectures, and adaptive beam control, which together form the backbone of today's most sophisticated automotive lighting systems.

Chapter 1

Theory notes

1.1 LEDs - Light Emitting Diode

LEDs don't get their color from their plastic cover. The color of the light comes from the semiconductor materials inside. The specific wavelength, and thus the color, is determined by the properties of the materials used to make the LED [4].

In 1962, General Electric engineer Nick Holonyak created the first visible-spectrum LED, which emitted a faint red light. A few years later, engineers at Monsanto developed a green LED. However, for decades, only red and green LEDs were available. This limited their use to simple applications like indicator lights, calculators, and digital watches. Blue LEDs, essential for full-spectrum white light, proved extremely difficult to create. Throughout the 1960s and beyond, major electronics companies around the world, including IBM, GE, and Bell Labs, raced to develop a working blue LED. Despite the efforts of thousands of researchers, success remained elusive. Ten years passed, then twenty, then thirty. Hopes of using LEDs for general lighting slowly faded.

Yet everyone knew LEDs had the potential to revolutionize lighting. Traditional incandescent bulbs, symbolized by the classic glowing lightbulb, are actually very inefficient. They generate light by passing current through a tungsten filament, which gets so hot that it glows. But most of the energy is lost as infrared radiation, heat, while only a small portion becomes visible light. LEDs, or Light Emitting Diodes, are fundamentally different. They produce light directly from electrical energy, making them far more efficient. A diode is a simple two-terminal electronic device that allows current to flow in only one direction, so here's how a LED works.

In an isolated atom, each electron occupies a distinct energy level. But when atoms are brought together to form a solid, things change. The outer electrons begin to feel the influence not just of their own nucleus, but of neighboring atoms as well. This interaction causes their energy levels to split into a large number of closely spaced levels, forming what's known as an energy

band. The highest energy band that still contains electrons is called the valence band, while the next higher, typically empty band is called the conduction band. The energy gap between these two bands, known as the band gap, is what determines the color of light the LED emits when electrons fall from the conduction band back into the valence band, releasing energy as photons [5]

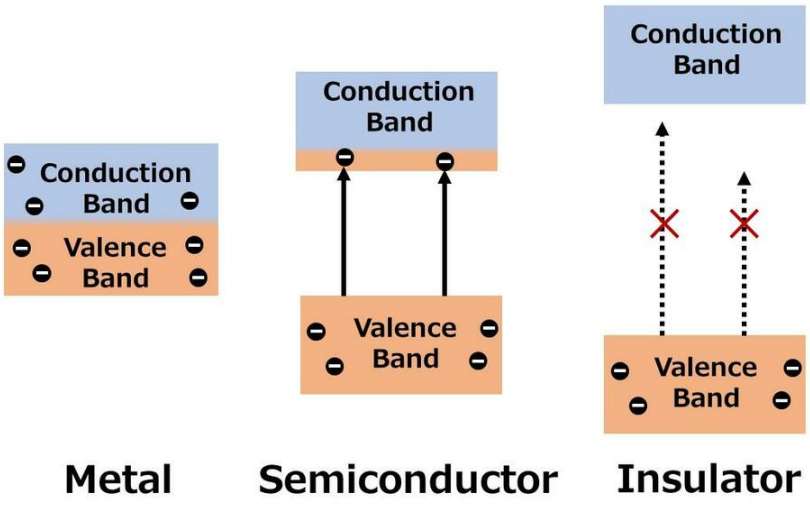


Figure 1.1: Conduction Band and Valence Band

In conductors, the valence band is only partially filled. This means that even a small amount of thermal energy allows electrons to jump into nearby empty energy states. When an electric field is applied, these electrons can easily move from one empty state to another, enabling current to flow through the material.

In insulators, the situation is very different. The valence band is completely full, and the energy gap between the valence band and the conduction band—called the band gap—is very large. As a result, when an electric field is applied, electrons can't move. There are no empty states within the valence band, and the band gap is too wide for electrons to jump into the conduction band. No current flows.

This brings us to semiconductors, which are similar to insulators but with a much smaller band gap. At room temperature, a small number of electrons in a semiconductor have enough thermal energy to jump from the valence band into the conduction band. Once in the conduction band, they can move freely and conduct electricity. But that's not all. When electrons leave the valence band, they create empty energy states, called holes, that nearby electrons can jump into. From a distance, it appears as if the hole itself is moving, carrying positive charge in the opposite direction of the negatively charged electrons in the conduction band. Pure semiconductors (like pure silicon) aren't very useful on their own. To enhance their conductivity, we introduce a

small amount of impurity atoms, a process known as doping.For example, if we add phosphorus atoms to silicon, we create what's called an n-type semiconductor. Phosphorus has one more valence electron than silicon, and this extra electron is loosely bound. It sits in a donor energy level just below the conduction band, and with minimal thermal energy, it can easily jump up and conduct current. Since most of the mobile charge carriers are negatively charged electrons, we call this "n-type" (n for negative), even though the material as a whole remains electrically neutral. On the other hand, if we dope silicon with boron, which has one fewer valence electron than silicon, we get a p-type semiconductor. Boron introduces an empty acceptor level just above the valence band. With a bit of thermal energy, electrons from the valence band jump up into this acceptor level, leaving behind holes. These holes behave like mobile positive charge carriers, so we call it "p-type" (p for positive).
Now, when you place a piece of p-type material next to a piece of n-type, something interesting happens, even without an external circuit. Electrons from the n-type region diffuse into the p-type region and fall into available holes. This movement leaves behind a slight positive charge in the n-region and a slight negative charge in the p-region, setting up an internal electric field. Eventually, this built-in field becomes strong enough to stop further diffusion. This forms what's called the depletion region, an area around the junction where there are no free electrons or holes. It's essentially an insulating layer. If you connect a battery to this diode in the reverse direction, the depletion region widens. The battery's electric field reinforces the internal field, preventing current flow. But if you connect the battery in the forward direction, the external field opposes the internal one, shrinking the depletion region. Once it becomes small enough, electrons can once again cross the junction—from the n-side into the p-side—where they fall into holes.
When an electron recombines with a hole, it drops from the conduction band to the valence band, releasing energy. If the material is right, this energy is emitted as a photon, a particle of light. This is the basic working principle of a Light Emitting Diode (LED).

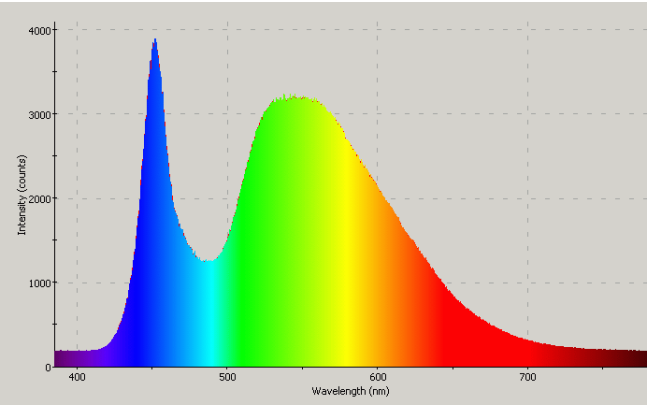


Figure 1.2: Spectrum LED

The color of the emitted light depends on the size of the band gap. In silicon, the band gap

is about 1.1 electron volts, which produces infrared light, not visible to the human eye. That's why silicon LEDs are used in things like TV remote controls because you can't see the light, but a camera can. To get visible light, you need materials with larger band gaps. That's why the first visible LEDs emitted red, then green, and why creating blue LEDs was so difficult. Blue photons require significantly more energy—meaning a much wider band gap and more advanced materials.

1.2 DC-DC Converters

1.2.1 DC-DC Buck Converter

DC-DC converters are switching converters supplied by a dc voltage source and regulating one or more dc output voltages. We will begin the study by analyzing the simplest topology, i.e. the Buck converter, also known as "step-down" or, in the past, also "series chopper" due to the presence of a switch in series between input and output terminals.
The switching diagram of the Buck converter is shown in Figure 1.3. The dc input voltage v_i is transformed by the switching unit into a square-type voltage v_D: when the switch S is conducting (interval t_{on}) voltage v_D is zero. This voltage consists of a continuous term V_D added to multiple frequency harmonic components of the fundamental frequency $f_s = \frac{1}{T_s}$, also called switching frequency. This voltage is applied to the second-order non-dissipative filter realized by the reactive elements L and C. Assuming a resistive load equal to R_o, the transfer function of this filter is given by :

$$F(s) = \frac{v_o(s)}{v_D(s)} = \frac{1}{1 + s\frac{L}{R_o} + s^2 LC} \tag{1.1}$$

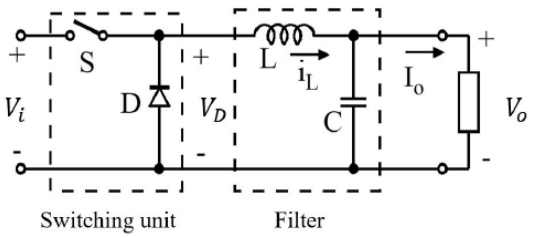


Figure 1.3: DC-DC Buck Converter

The purpose of the output filter is to eliminate the harmonic components present in the voltage v_D so that the output voltage v_o is practically constant and coincides with the average component V_D of v_D, i.e.:

$$v_o = V_o = V_D = \frac{t_{on}}{T_s} V_i = \delta V_i \tag{1.2}$$

where δ is called "duty-cycle". The output voltage is therefore less than or at most equal to the input voltage ($0 < \delta < 1$)

1.2.2 DC-DC Boost Converter

The Boost converter, also called "step-up" or, in the past, also "parallel chopper" due to the presence of the switch placed in parallel to the power flow converts the voltage input voltage V_i in a positive output voltage V_o of a value greater than or, at minimum, equal to that of the input voltage. The schematic diagram of the Boost converter is shown in Figure 1.4.
As you can see, the Boost converter scheme contains the same elements as the Buck converter: a one-way switch (that is, one that conducts current in one direction only), an inductor a diode and a capacitor. However, the mutual arrangement of the various elements is different, and the resulting operation is very difficult. In particular, it can be observed how this converter can be obtained from the Buck converter scheme simply by inverting the power flow, and then exchanging the input with the output (this modification also involves the exchange of positions between switch and diode). Unlike the Buck converter, the input inductance allows for a current absorbed by the power supply with a harmonic content at a reduced switching frequency and therefore does not require an additional input filter.

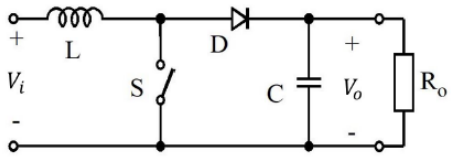


Figure 1.4: DC-DC Boost Converter

1.2.3 DC-DC converter : SEPIC

Overview of SEPIC converter

The Single-Ended Primary-Inductor Converter (SEPIC) is a type of DC-DC converter that allows the output voltage to be greater than, less than, or equal to the input voltage. The SEPIC converter operates by controlling the duty cycle of the main switching element. Similar to other switch-mode power supply converters, the SEPIC regulates voltage by exchanging energy between inductors and capacitors.

Unlike simpler buck, boost, and buck-boost topologies, the SEPIC converter incorporates an additional inductor and capacitor, making it a fourth-order converter.

Advantages of SEPIC converters

A key advantage of the SEPIC converter is its ability to both step up and step down voltage, which is particularly useful in applications where the input voltage varies, such as battery-powered or fuel-cell-based systems. Unlike a boost converter, which can only increase voltage, the SEPIC provides greater control and protection. For instance, in fault conditions where voltage reduction is required, a boost converter would fail to limit the voltage, potentially causing excessive current flow through the circuit.
Additionally, the SEPIC topology includes an input inductor, which reduces switching harmonics, a limitation found in buck and buck-boost converters. A related fourth-order topology is the Cuk converter, which also offers voltage step-up and step-down capabilities. However, the Cuk converter produces an inverted output voltage and has an inductor at the output, resulting in reduced ripple on the output capacitor compared to SEPIC.

SEPIC converter analysis

To analyze the SEPIC topology, we determine the component values and operational characteristics using steady-state conditions. Instantaneous current and voltage values are denoted by lowercase letters (i, v), while their average values are represented by uppercase letters (I, V) [6].

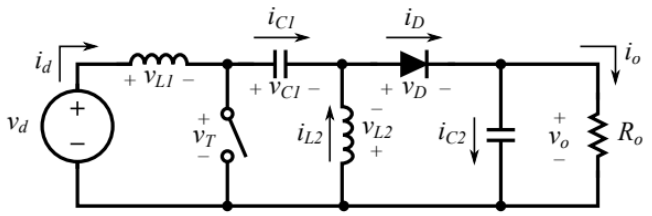


Figure 1.5: SEPIC diagram

The conversion ratio (or duty cycle) is derived using the volt-second balance principle, which states that in steady-state operation, the average voltage across an inductor over a switching cycle must be zero. For the inductor L_1,where the voltage and current waveforms are shown in Figure 1.6 [7]:

- When the switch T is ON (closed), the voltage across L_1 is $v_{L_1} = V_d$

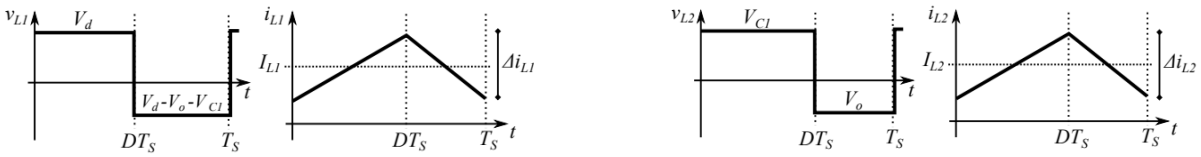
- When the switch T is OFF (open), the voltage across L_1 is $v_{L_1} = V_d - V_o - v_{C_1}$

When taking the average voltage and equaling it to zero it is obtained that

$$\begin{aligned} \frac{1}{T_s}\int_0^{T_s} v_{L_1} dt = 0 \\ V_o + V_{C_1} = \frac{V_d}{1-D} \end{aligned} \tag{1.3}$$

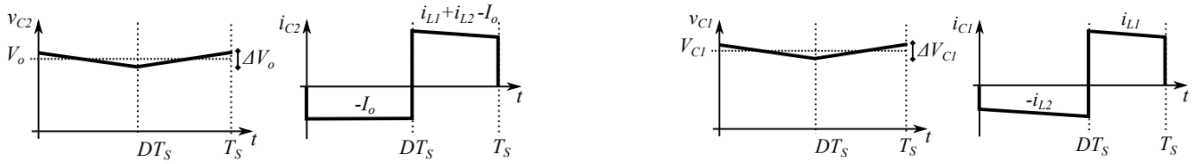
Similarly, by applying the volt-second balance on L_2:

$$\begin{aligned} \frac{1}{T_s}\int_0^{T_s} v_{L_2} dt = 0 \\ V_o + V_{C_1} = \frac{V_o}{D} \end{aligned} \tag{1.4}$$



(a) Voltage and Current waveforms of L_1 (b) Voltage and Current waveforms of L_2

Figure 1.6: Voltage and Current waveforms of inductors L_1 and L_2.



(a) Waveforms of C_1 (b) Waveforms of C_2

Figure 1.7: Voltage and Current waveforms of capacitors C_1 and C_2.

Combining Equations 1.3 and 1.4, the transfer ratio of the SEPIC converter [8] is obtained as

$$\begin{aligned} \frac{V_o}{D} = \frac{V_d}{1-D} \\ \frac{V_o}{V_d} = \frac{D}{1-D} \end{aligned} \tag{1.5}$$

The average voltage of capacitors C_1 can be determined by combining Equation 1.3 and 1.4, while for C_2 is obtained assuming that the capacitor is sufficiently large to maintain a constant output voltage:

$$V_{C_1} = \frac{V_d}{1-D} - V_o \qquad\qquad V_{C_2} = V_o \tag{1.6}$$

From the power balance between input and output, it is possible to find the average and ripple currents of the two inductor, using

$$V_d I_d = V_o I_o \tag{1.7}$$

From Fig. 1.6(a), it is observed that $I_{L_1} = I_d$. To determine I_{L_2}, we note that the average current in the capacitors is zero during steady-state operation. Therefore, the output current is entirely supplied through the diode, which conducts only during the time interval $t = DT_s$ to $t = T_s$, leading to:

$$\begin{aligned} I_o &= \frac{1}{T_s}\int_{DT_s}^{T_s} i_D\, dt = \frac{1}{T_s}(I_{L_1} + I_{L_2})(1-D)T_s \\ I_{L_1} &= I_d = \frac{D}{1-D} I_o \\ I_{L_2} &= I_o \end{aligned} \tag{1.8}$$

The current ripple, Δi_L, is derived from the applied voltage during the ON or OFF states using the fundamental relation $v_L = L\frac{di}{dt}$. Assuming constant voltage we obtain $v_L = L\frac{\Delta i}{\Delta t}$. During the switch on-time the applied voltage to L_1 is $v_{L_1} = V_d$. Thus for the two inductors L_1 and L_2, the current ripple is determined by:

$$\begin{aligned} \Delta i_{L_1} &= \frac{(1-D)V_o T_s}{L_1} \\ \Delta i_{L_2} &= \frac{(1-D)V_o T_s}{L_2} \end{aligned} \tag{1.9}$$

As for the voltage ripple ΔV of the capacitors C_1 and C_2, neglecting the current ripple, we obtain the following:

$$\begin{aligned} \Delta V_{C_1} &= \frac{I_o D T_s}{C_1} \\ \Delta V_{C_2} &= \frac{I_o D T_s}{C_2} \end{aligned} \tag{1.10}$$

1.3 Charge Pump

Charge Pumps are useful little DC/DC converters that use a capacitor to store energy instead of an inductor. So far, the reported efficiencies of the charge pump circuits achievable during voltage conversions are up to 90-95% [9].
It converts the supply voltage Vdd to a DC output voltage V_{out} that is several times higher than Vdd. CPs are only made of capacitors and switches, thereby allowing integration on silicon.

They wew originally used in smart power ICs and nonvolatile memories.
In current applications, CPs may be either loaded by a simple capacitor (or equivalently the gate of a MOS transistor) or by complex electronic circuits. Generally speaking, they are:

- More forgiving than DC/DC converters
- Good for output currents in the tens of milliamps range

1.3.1 One Stage Charge Pump

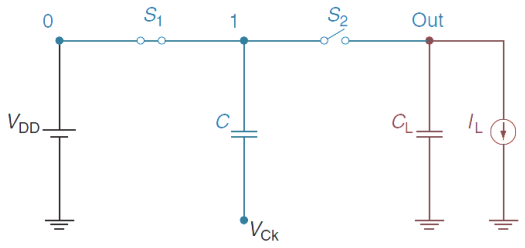


Figure 1.8: One Stage Charge Pump

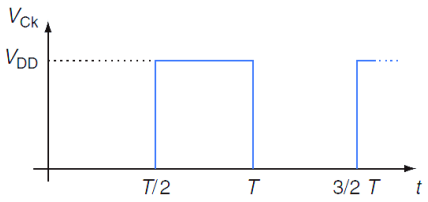


Figure 1.9: Segnale di clock V_{Ck}

The One-Stage Charge Pump consists of two switches, S1 and S2, controlled by a clock signal V_{Ck}, whose amplitude is equal to the power supply voltage V_{DD}. The circuit also includes a load capacitor C_L and a current generator I_L connected as the load.

First Half Period

During the first half period [0,T/2], when $V_{Ck} = 0$, switch S1 is closed while S2 is open. In this phase, capacitor C, being connected to V_{DD}, charges up to V_{DD}. Meanwhile, the output node discharges due to the load current I_L

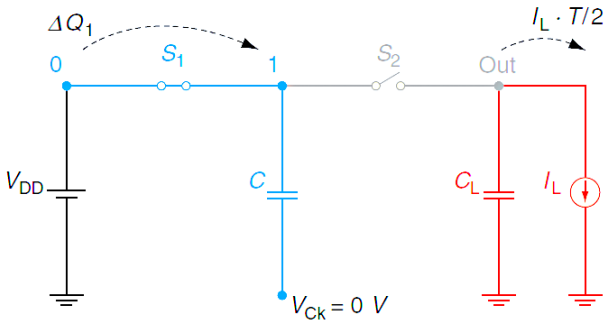


Figure 1.10: First half period

Second Half Period

In the second half period [T/2,T], when $V_{Ck} = V_{DD}$, the switches change state: S1 opens and S2 closes. In this condition, part of the charge stored in C is transferred to the capacitor C_L, while another part, equal to $I_L \cdot T/2$, is supplied to the load current generator.
The output voltage V_{Out} initially increases gradually and eventually stabilizes at its final value. In conclusion, the charge pump extracts charge from the power

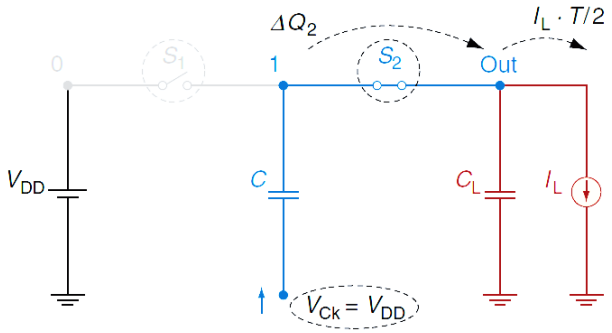


Figure 1.11: Second half period

1.3.2 N-Stage Charge Pump

The one -stage CP topology can be generalized by including additional cascaded stages as shown in figure 1.12, where a generic N-stage CP is depicted. Each stage is made of a pumping capacitor C and a switch S_i. Moreover, the N-stage CP needs a two-phase clock and, to properly connect the output load to the final stage, switch S_{Out} is also required.
The behavior is similar to that of a one-stage CP. During the first half clock period, V_{Ck} is low and only the odd switches are closed. The first pumping capacitor C is thus charged to V_{DD} and all the other pumping capacitors in the odd stages receive the charge from the capacitor of the previous stage. During the subsequent half period, the signal V_{Ck} is equal to V_{DD} and only the even switches are closed. Now all the capacitors in the odd stages give the charge to the capacitor in the subsequent stage. In summary, in a complete clock period, each CP capacitor receives an amount of charge from the capacitor at its right side. Thus, in each period there is a charge transfer from the power supply to the output load.

Two stage CP

Let's consider a two-stage CP with a current load, as shown in figure 1.13. During the first half period, or steady state, the first capacitor is connected to V_{DD} and is recharged by ΔQ, which is the same amount of charge provided by the CP to the output.

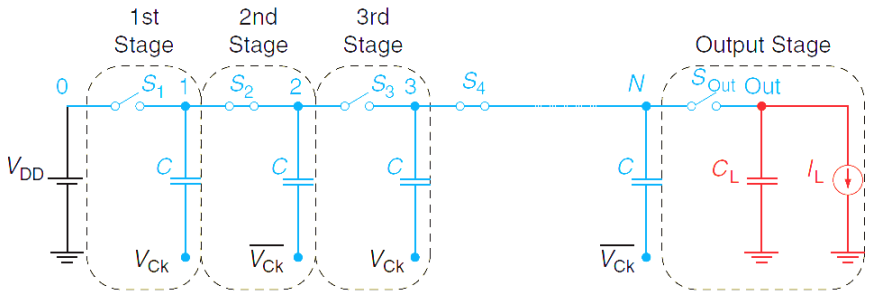


Figure 1.12: N-Stage Charge Pump

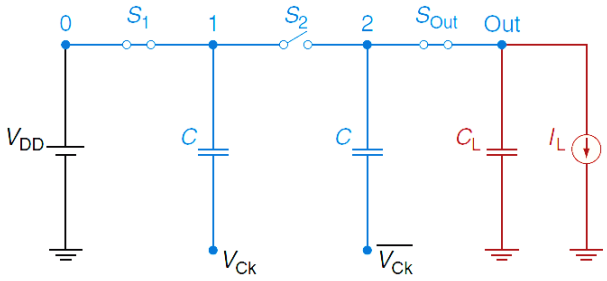


Figure 1.13: First Half Period

In the next half period, when the first and the second pumping capacitors are connected together (Fig. 1.14) since switch S_2 is closed, they exchange the same amount of charge, ΔQ, and the highest node voltage results to be:

$$V_{1|V_{Ck}=V_{DD}} = V_{2|\overline{V_{Ck}}=0V} = 2 \cdot V_{DD} - \frac{I_L \cdot T}{C} \tag{1.11}$$

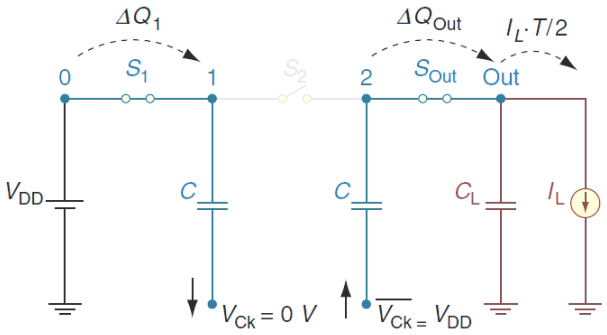


Figure 1.14: Second half Period

Finally, in the subsequent first half period, when the switches S_1 and S_{Out} are closed (Fig. 1.15), the output voltage is :

$$V_{Out} = V_{2|\overline{V_{Ck}}=V_{DD}} = 3 \cdot V_{DD} - 2 \cdot \frac{I_L \cdot T}{C} \tag{1.12}$$

Extending the reasoning to an N-stage CP, we get the well known output voltage asymptotic value

$$V_{Out|Steady\_State} = (N+1) \cdot V_{DD} - N \cdot \frac{I_L \cdot T}{C} \tag{1.13}$$

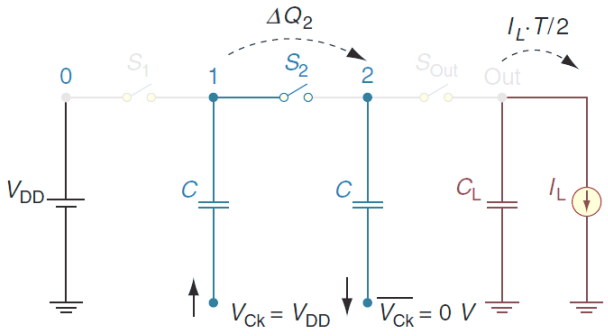


Figure 1.15: Subsequent first half

It is worth noting that, when switches close, assuming them almost ideal, the charge transfer occurs in a very short time(ideally zero). Thus, when S_{Out} closes, the output voltage suddenly reaches its maximum value and then, due to the presence of the current load I_L, during all the time period it slightly decreases. This effect results in an output voltage ripple, V_γ, which, assuming the charge pump capacitor C much smaller than the load capacitor, is equal to

$$V_\gamma = \frac{I_L \cdot T}{C_L} \tag{1.14}$$

1.4 Adaptive Output Discharge - AOD

Automotive manufacturers are increasingly integrating advanced safety lighting features - such as glare-free high beams and matrix LED system - into their vehicles. These systems often consolidate multiple lighting functions onto the same LED string to lower system costs. However, this evolution introduces new challenges for LED lighting designers, particularly in managing power delivery, thermal performance and system complexity.
Figure 1.16 illustrates a common setup for LED driving that uses a combination of a DC-DC converter and a Matrix Manager [10]. The Matrix Manager includes a series of bypass switches with adjustable slew rates, enabling dynamic control of which LEDs in the string are active. The light intensity of the LED string is regulated by controlling the current flowing through it. In typical automotive scenarios, the system operates from a $12\ V$ battery input, with the output voltage ranging from $2.5\ V$ to over $70\ V$, depending on how many LEDs are in series.

When LEDs are dynamically bypassed, the total forward voltage of the string drops abruptly. As a result, the output capacitor (connected in parallel with the load) discharges

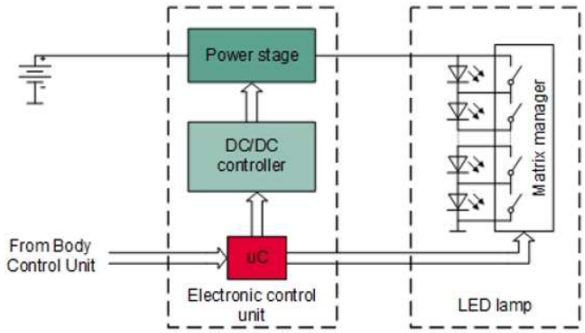


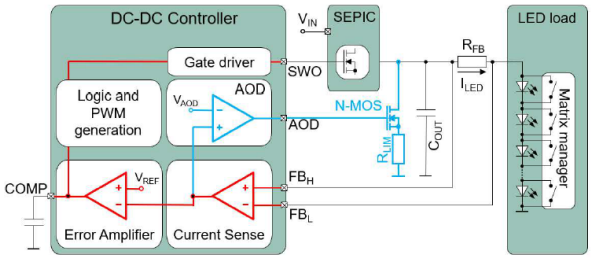
Figure 1.16: Application of LED driver

rapidly, causing a sudden current spike through the active LEDs. This spike can potentially damage the remaining LEDs in the string.
To address this issue, here is proposed a new control system that powers a fully dynamic adaptive lighting application using a single device. Figure 1.17 presents the proposed solution, which includes a dedicated control device managing a DC-Dc converter based on a SEPIC topology and an additional NMOS transistor that provides a secondary path to ground. The DC-DC converter regulates the current through the LED string under normal operation. The parallel NMOS transistor remains OFF during steady-state conditions. However, when some LEDs are bypassed, the resulting drop in load voltage and series resistance causes a temporary surge in output current.

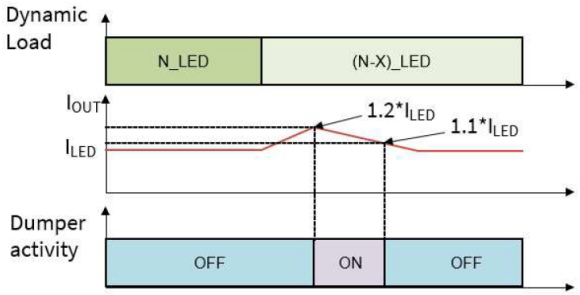
To mitigate this, the system uses a current-sensing mechanism:

- A sense resistor (RFB) monitors the LED current
- The voltage across RFB is amplified by an internal Current Sense Amplifier
- This amplified signal is compared against an internal reference voltage (VAOD) using a comparator

If the sensed current exceeds 120% of the target value (as shown in Figure 3.13), the comparator output goes high, turning ON the NMOS transistor. This creates an alternate path for the excess current, discharging the output capacitor (C_{Out}) and reducing the spike through the LEDs. The NMOS stays ON untile the output current drops below 110% of the target value, at which point it is turned OFF.
This dynamic discharge mechanism ensures that the output voltage and current remain within safe limits, protecting the LED string during rapid configuration changes. To prevent excessive current through the dump path, a current-limiting resistor (Rlim) is placed in series with the



(a) System overview



(b) System behavior

Figure 1.17: Adaptive Output Discharge

NMOS. The discharge path must be fast enough to complete before the bypass switches close, ensuring stable system behavior during LED transistor.

1.5 TLP and ESD

Transmission Line Pulse (TLP) testing is a methodology employed to assess the behavior of integrated circuit technologies and circuit responses when subjected to transient events, particularly electrostatic discharge (ESD) [11]. This technique involves the application of short, rectangular pulses to a device under test (DUT) to simulate the rapid energy transfer characteristic of ESD events. By precisely controlling the parameters of these pulses and monitoring the resulting current-voltage (I-V) characteristics of the DUT, engineers can gain a comprehensive understanding of its susceptibility and robustness to ESD [12]. The fundamental principle behind TLP testing involves utilizing a charged transmission line as a source to generate a constant amplitude rectangular pulse that is then discharged into the DUT. The specific characteristics of the pulse, such as its width and rise time, can be readily adjusted by modifying the length of the transmission line cable and the properties of any filters incorporated in the test setup. This allows for a versatile approach to simulate a wide range of ESD scenarios. In essence, TLP testing can be viewed as a form of pulsed I-V measurement that is particularly relevant to the time scales and energy levels associated with ESD phenomena. Furthermore, by employing time-domain reflectometry (TDR), the changes in the DUT's impedance can be observed as a

function of time during the application of the pulse. This capability provides additional insights into the device's dynamic response to ESD stress. The controlled nature of TLP testing offers significant advantages over relying on uncontrolled real-world ESD events, which are often unpredictable and challenging to measure accurately. By providing a repeatable and quantifiable method to stress devices with ESD-like pulses, TLP enables a systematic evaluation of device robustness under various ESD conditions achieved by adjusting pulse parameters to mimic different scenarios [13].
TLP testing presents several key advantages when compared to traditional ESD testing methods such as the Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) [14]. Unlike these methods, which often provide a binary pass or fail outcome, TLP testing yields a quasi-static I-V characteristic that thoroughly describes electrical behavior of the DUT under ESD stress [15]. A significant benefit of TLP is its ability to pinpoint the exact test pulse within a sequence that causes damage to the DUT, providing critical data for determining failure thresholds. The capacity of TLP to generate I-V curves offers a deeper understanding of device behavior under ESD stress, a level of detail not readily available from the binary results of traditional methods.

Standard TLP testing employs pulses with a width centered around 100 nanoseconds. This specific pulse duration is often selected because it approximates the energy associated with a typical HBM event, making standard TLP a valuable tool for predicting how a device might perform when subjected to electrostatic discharge from a human body. The rise time f these pulses, which is the time it takes for the pulse to reach its peak amplitude, generally falls within the range of 0.2 to 10 nanoseconds. To obtain a point on the I-V curve of the DUT, measurements are typically taken during a stable portion of the pulse, often within the 70% to 90% region of its total duration. The current levels achieved during standard TLP testing can reach up to a few Amperes, depending on the specific test conditions and the characteristics of the DUT. The selection of a 100 ns pulse width is not arbitrary; it is grounded in the desire to replicate the thermal stress experienced by a device during an ESD event originating from human contact. By using a pulse of similar duration to the energy dissipation time of an HBM event, standard TLP aims to provide a realistic assessment of the device's ability to withstand such stress

1.6 Control Methods

1.6.1 Voltage Mode Control

Voltage Mode Control (VMC) stands as a fundamental and often considered the most basic method for controlling DC-DC converters. In this control strategy, the primary objective is to directly monitor and regulate only the output voltage of the converter. The defining character-

istic of VMC is its single feedback loop structure, where the output voltage serves as the sole feedback signal utilized for regulation. This approach represents the most straightforward application of classical single-loop feedback control to power converters. In VMC, the duty cycle of the power switch is directly proportional to a control voltage. This control voltage is derived from the continuous comparison of the sensed output voltage with a precise reference voltage. The Pulse Width Modulation (PWM) signal, which ultimately drives the power switches, is generated by comparing the error signal from this voltage feedback loop with a fixed-frequency, fixed-amplitude sawtooth or triangular ramp waveform. This ramp is typically generated internally within the controller. By directly regulating the output voltage without explicit current information in the primary control loop, VMC simplifies the conceptual design. However, this approach places the entire burden of managing the power stage's inherent two-pole dynamics squarely on the voltage feedback loop, which can introduce complexities in compensation.

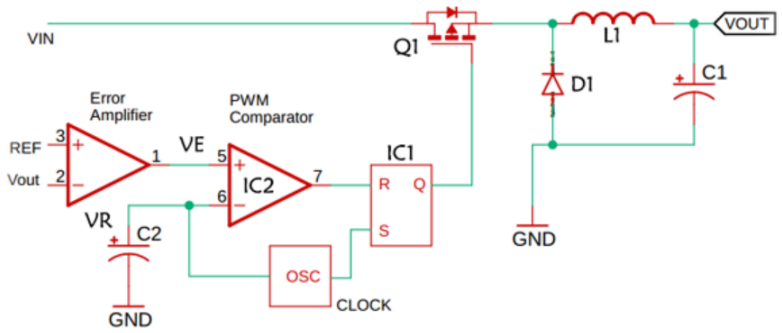


Figure 1.18: Voltage Mode Control

Voltage Mode Control offers several distinct advantages that make it suitable for a range of power converter applications. Here are some advantages:

- **Simpler design and implementation**: VMC is generally considered easier to design and implement compared to current mode schemes. Its single feedback loop simplifies the analysis and stabilization process, making it a more intuitive choice for certain applications.
- **Good noise margin**: The use of a relatively large-amplitude ramp waveform for PWM generation provides a robust noise margin. This contributes to a more stable modulation process and helps minimize the impact of signal and noise problems through the error amplifier.
- **Constant Switching Frequency**: VMC typically operates at a constant switching frequency. This is advantageous for Electromagnetic Interference (EMI) control, as the frequency of potential noise spikes is predictable, simplifying filtering and compliance efforts.

- **Good cross-regulation**: For power supplies with multiple outputs, VMC can offer better cross-regulation. This is attributed to its low-impedance power output, which helps ensure that changes in one output load have minimal impact on the voltage levels of other outputs.
- **Flexibility in component selection**: VMC often allows for greater flexibility in selecting inductor values and capacitor types, providing designers with more options during the component selection and optimization phases.
- **Effective voltage feed-forward**: VMC can effectively incorporate voltage feed-forward techniques. By making the slope of the PWM ramp proportional to the input voltage, the controller can achieve instantaneous and automatic correction of the duty cycle in response to input voltage variations. This maintains a more constant control loop gain and provides immediate response to line changes without solely relying on the feedback loop's reaction time.

Despite its advantages, Voltage Mode Control presents several challenges and limitations that can impact the performance and design complexity of power converters.

- **Slow response time**: One of the most significant drawbacks of VMC is its relatively slow response to dynamic changes in input voltage or output load. The control loop must first sense a deviation in the output voltage, and then the corrective action propagates through the entire feedback path and the output filter. This sequential process can result in an unacceptably slow response for systems that require high levels of regulation and fast transient recovery. This slowness is primarily due to the inherent two-pole response of the LC output filter in the power stage.
- **Complex compensation network**: The presence of two poles (from the inductor and output capacitor) in the power stage's transfer function makes the feedback loop compensation more complex. To ensure stability and achieve an adequate phase margin, especially at higher frequencies, VMC often necessitates more elaborate compensation networks, such as Type II or Type III compensators, around the error amplifier. If the crossover frequency increases without proper compensation, the phase margin can decrease, potentially leading to system instability. This is a deep-seated challenge in VMC design, as the fundamental physics governing the LC output filter's two-pole response directly dictates the core stability and transient limitations.
- **Degraded performance in parallel operation**: VMC can exhibit degraded reliability, stability, or performance when multiple converters are connected in parallel to supply a common load. Achieving accurate current sharing between these parallel units can be

challenging without the addition of complex external circuitry, which adds to the overall system cost and complexity.

- **Difficulty in power factor correction**: VMC is generally less suitable for Power Factor Correction (PFC) applications compared to current mode control. Current mode control inherently facilitates input current shaping, which is crucial for achieving high power factor, whereas VMC typically requires more complex external circuitry to achieve similar performance.

1.6.2 Current Mode Control

Current Mode Control (CMC), also known as current-programmed mode or current-injected control, represents an advanced control strategy for switching power supplies that addresses several limitation of Voltage Mode Control. . Unlike VMC, CMC employes a multi-loop control scheme characterized by an inner current feedback loop nested within an outer voltage feedback loop. This hierarchal structure is a defining feature of CMC. The core principle of CMC involves directly measuring the inductor current waveform (or the current through the main power switch) and utilizing this measurement as a primary control variable for Pulse Width Modulation (PWM) generation. This direct current sensing allows the controller to overcome some of the inherent limitations of VMC, such as slow response times and the lack of inherent current limiting capabilities. The introduction of this inner current loop fundamentally transforms the system's control-to-output transfer function. The inner current loop effectively ”hides” or ”absorbs” the complex dynamics of the inductor from the outer voltage loop, simplifying the overall system from a second-order (two-pole) system to a first-order (single-pole) system. This simplification significantly eases the compensation requirements for the outer voltage loop, making the overall control design more manageable in certain aspects.

- **Faster transient response**: The inner current loop allows CMC to react much more quickly to sudden changes in load or input voltage compared to VMC. This cycle-by-cycle control enables rapid adjustments, leading to superior transient response.

- **Inherent cycle-by-cycle current limiting**: a direct benefit of sensing the inductor or switch current is the ability to implement immediate, cycle-by-cycle shutdown or limiting in the event of an overcurrent or short-circuit condition. This significantly enhances system reliability and provides robust protection.

- **Simplified compensation**: As a direct consequence of the ”disappearing inductor” effect, the power stage's control-to-output transfer function, as perceived by the outer voltage loop, is simplified to a single-pole response. This dramatically simplifies the design of

the feedback compensation network, often allowing for the use of simpler compensators and enabling stability with low-ESR ceramic output capacitors, which can lead to smaller solution sizes and improved performance. This simplification of the control loop directly translates into practical benefits such as faster transient response, easier compensation design, and the ability to utilize smaller, lower-Equivalent Series Resistance (ESR) ceramic capacitors. These combined effects contribute to the development of more compact, efficient, and higher-performing power supply designs.

- **Easy and accurate current sharing**: CMC inherently facilitates accurate current sharing when multiple converters are connected in parallel or in multiphase designs. Since the output current is directly controlled and proportional to the control voltage, parallel power stages can be forced to share current equally, which is crucial for high-current applications

- **Inherent line feed-forward**: CMC naturally offers an ingerent line feed-forward property. This means it can automatically compensate for input voltage variations without requiring explicit feed-forward circuitry, thereby improving line regulation and dynamic response to input changes.

- **Improved power factor correction**: Particularly with average current mode control, CMC is highly effective in shaping the input current to achieve very low harmonic distortion. This makes it an ideal choice for high power factor preregulators, contribuiting to better power quality in electrical systems.

While Current Mode Control offers significant advantages, it also introduces its own set of complexities and limitations that designers must carefully consider.

- **Increased complexity**: Despite simplifying the voltage loop compensation, CMC inherently increases the overall complexity of the control circuit due to the addition of an inner current feedback loop. This dual-loop structure makes the design and analysis more intricate than that of a single-loop VMC system. This illustrates a fundamental trade-off: ”simpler” in one aspect often translates to ”more complex” in another, requiring a holistic design approach.

- **Increased complexity**: A significant challenge in CMC is the susceptibility of the current sense signal to switching noise and voltage transients. Since the current waveform is directly used for PWM generation, any noise on this signal can lead to false triggering, jitter, and instability. This often necessitates additional noise filtering techniques, such as RC networks or ”leading-edge blanking” (ignoring the initial part of the current signal), which can sometimes compromise minimum ON-time or fault protection capabilities.

- **Right-half-plane zeros (RHPZ)**: For certain converter topologies like Boost and Buck-Boost, the undesirable Right-Half-Plane Zero (RHPZ) remains present even with current mode control. RHPZs introduce a phase lag instead of a phase lead and can cause a momentary reduction in output voltage with a sudden increase in duty cycle. This behavior, effectively an inversion at higher frequencies, makes compensation more challenging, particularly for high-bandwidth designs.

- **Limited transconductance bandwidth**: While the inner current loop simplifies the outer loop, the bandwidth of the voltage-to-current converter (transconductance) itself is limited, typically to 1/6 to 2/3 of the switching frequency. Beyond this frequency, the transconductance gain falls, effectively reintroducing a second pole into the overall control-to-output transfer function, complicating high-frequency compensation.

1.6.3 Peak Current Mode Control (PCMC)

Peak current mode control is a widely adopted and popular variant within the broader category of Current Mode Control. In PCMC, the control strategy dictates that the main power switch is turned off when the instantaneous peak value of the inductor current reaches a predetermined threshold or ”programmed level”. This current threshold is dynamically set by the output of the outer voltage error amplifier., thus linking the current regulation to the overall voltage regulation objective. Like other current mode control schemes, PCMC operates with a cascaded dual-loop structure. It features an outer voltage feedback loop, typically monitored by a compensator to maintain output voltage regulation, and an inner current feedback loop, which is usually monitored by a fast analog comparator to control the peak current. This dual-loop approach allows for the benefits of current mode control, such as faster transient response and inherent current limiting. PCMC stands out as the most prevalent implementation of current mode control, leveraging the direct control of peak current for its inherent advantages like fast response and cycle-by-cycle protection. Its widespread adoption in consumer electronics, computer peripheral power management, and automotive applications underscores its practical utility and proven effectiveness. However, this widespread adoption necessitates a deep understanding of its unique stability challenges, particularly subharmonic oscillations, which are a direct consequence of this peak-sensing mechanism.
Subharmonic oscillation represents a critical and inherent form of instability that can occur in current mode switching regulators, particularly in Peak Current Mode Control. This phenomenon is characterized by the inductor ripple current failing to return to its initial value by the start of the next switching cycle. When observed on an oscilloscope, this instability often manifests as alternating wide and narrow PWM pulses at the switch node, creating an erratic

and undesirable switching pattern.

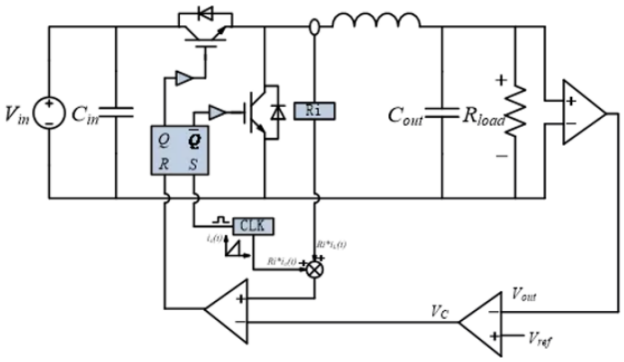


Figure 1.19: DC-DC Buck converter with Peak Current Mode Control

The root cause of this instability inherently arises when the converter operates in continuous conduction mode (CCM) and the steady-state duty cycle (D) exceeds 50% (D > 0.5). If a small perturbation or disturbance occurs in the inductor current under these conditions, this perturbation will not damp out but will instead grow larger with each subsequent switching cycle, leading to progressive system instability. This is a fundamental instability in PCMC when the duty cycle exceeds 50%. It is not a minor design imperfection but a critical consequence of the sampled-data nature of the current loop under these conditions. The impact of subharmonic oscillations on system performance is severe. They lead to an unstable power supply , resulting in erratic output voltage, increased ripple, and potentially causing damage to components due to uncontrolled current and voltage stresses. Furthermore, the alternating pulse widths generate significant electromagnetic interference (EMI) broadcasting issues. The beat frequency, which occurs at half the switching frequency, can interfere with other electronic systems and radio bands, such as the AM band in automotive applications. This instability must be addressed for stable and reliable operation, making its mitigation a non-negotiable design consideration in PCMC applications.
Peak Current Mode Control offers a compelling combination of performance benefits that make it a highly desirable control strategy for many modern power converter applications.

- **Fixed frequency operation**: PCMC typically operates at a fixed switching frequency. This is a significant advantage for Electromagnetic Interference (EMI) control and filtering, as the frequency of noise spikes is predictable and easier to manage.

- **Consistent bode plot**: Compared to Voltage Mode Control, PCMC often exhibits a more consistent Bode plot (gain and phase response) across variations in input voltage. This simplifies the loop compensation design, as the control loop's characteristics remain more predictable over different operating conditions.

- **Simpler compensation**: The effective single-pole response of the power stage, resulting from the inner current loop, significantly simplifies the compensation network design for the outer voltage loop. This often requires fewer external components and can eliminate the reliance on the output capacitor's Equivalent Series Resistance (ESR) for stability, contributing to smaller and more robust designs.

- **Fast transient response**: PCMC provides excellent transient response to sudden changes in load or input voltage. Its cycle-by-cycle control of the inductor current allows for rapid adjustments, ensuring quick recovery and stable output under dynamic conditions.

- **Inherent cycle-by-cycle current limit**: The direct sensing of peak current enables immediate, cycle-by-cycle current limiting. This offers robust protection against overloads and short circuits, enhancing the reliability and safety of the power supply.

- **Easy current sharing**: PCMC inherently facilitates accurate current sharing when multiple power stages are connected in parallel. This is crucial for high-current applications where distributing the load evenly among parallel converters is essential for efficiency and reliability.

- **Potentially smaller transformer**: In discontinuous conduction mode (DCM), PCMC can allow for a smaller transformer size. This is due to its ability to operate at higher switching frequencies while maintaining efficiency, which can lead to more compact power supply designs.

Despite its numerous advantages, Peak Current Mode Control is not without its challenges and limitations. Many of these are shared with Current Mode Control in general, but some are particularly pronounced or critical for PCMC.

- **Subharmonic oscillation (without slope compensation)**: As extensively discussed, this is the primary inherent instability of PCMC. It occurs when the duty cycle (D) exceeds 50% in Continuous Conduction Mode (CCM). This fundamental instability necessitates the careful and precise implementation of slope compensation to ensure stable and reliable operation.

- **Noise sensitivity**: PCMC is inherently more susceptible to switching noise and voltage transients on the current sense signal. Since the current waveform is directly used for PWM generation, any noise can lead to false triggering, jitter, and instability. This often requires additional noise filtering techniques, such as RC networks or "leading-edge blanking" (ignoring the initial part of the current signal), which can sometimes compromise minimum ON-time or fault protection capabilities.

- **Challenges in accurate current measurement**: Accurately measuring the inductor or switch current with sufficient bandwidth and precision can be difficult in PCMC. Factors such as parasitic inductance in the sense resistor, charging and discharging currents of parasitic capacitances around the power switch, and the need for large filter capacitors to mitigate spikes can introduce inaccuracies and additional poles into the feedback loop. Historically, low DCR inductors in high-current applications also struggled to produce a sufficient voltage ramp signal for stable current mode operation, though newer controllers are addressing this.

- **Inaccuracies with changing line/duty cycle**: The peak-to-peak and average current values of the inductor can change with varying input line voltage and duty cycle. This can lead to inaccuracies in the transconductance (the voltage-to-current conversion gain) because the average current may not perfectly track the controlled peak current, affecting regulation accuracy.

- **Right-half-plane zeros (RHPZ)**: For certain converter topologies like Boost and Buck-Boost, the undesirable Right-Half-Plane Zero (RHPZ) remains present even with PCMC. RHPZs introduce a phase lag instead of a phase lead and can cause a momentary reduction in output voltage with a sudden increase in duty cycle. This behavior, effectively an inversion at higher frequencies, makes compensation more challenging, particularly for high-bandwidth designs.

- **Limited transconductance bandwidth**: While the inner current loop simplifies the outer loop, the bandwidth of the voltage-to-current converter (transconductance) itself is limited, typically to 1/6 to 2/3 of the switching frequency. Beyond this frequency, the transconductance gain falls, effectively reintroducing a second pole into the overall control-to-output transfer function, complicating high-frequency compensation.

Chapter 2

Software Development

The project utilizes Python to develop a graphical user interface (GUI) that enables the control of 12 LEDs on the board via a Matrix Manager. The implementation is primarily based on the tkinter library, which facilitates the creation of interactive elements such as buttons and drop-down menus. Later on, a different code is used for the 16-LED board, as it relies on a different chip with distinct registers compared to the previous one. Finally, we analyze the code implemented on the XMC4700 microcontroller, which allows for byte transmission at a significantly higher baud rate.

2.1 12 LEDs Code

The code is organized into several modules, one of which is the register_map file. This file, imported in the main script as rm, contains a series of functions that establish key-value pairs. In this context, each key is a string representing a parameter, and each value is a hexadecimal number corresponding to a specific register as defined in the datasheet

2.1.1 GUI development using tkinter package

The GUI is constructed using tkinter package, with a design that includes:

- Start Button: A prominently paced green ”START” button initiates the execution of the main function, `thread\_send\_serial()`. This function is called with several arguments, such as COMport_thread, INIT_thread, DEV_ID_thread and REGADDR_thread

- Stop Button: A ”STOP” button is provided to halt the ongoing data transmission via the function `stop\_thread\_serial()`.

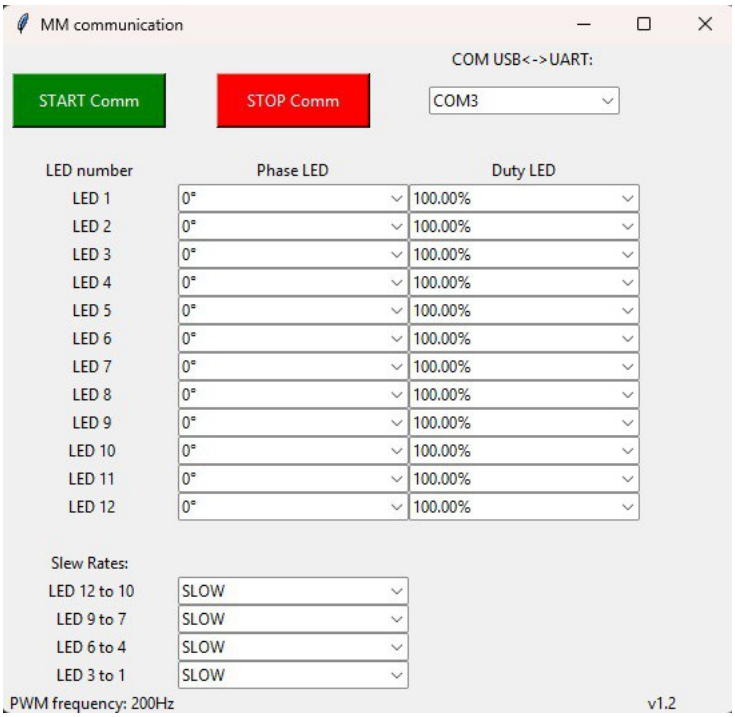


Figure 2.1: GUI 12 LEDs

- Dropdown Menus: Multiple dropdown menus are available to adjust parameters such as the duty cycle, phase and slew rate of the LEDs. The values populated in these menus are retrieved from the register_map file

```
    global combophase1box
    combophase1box = tk.StringVar()
    combophase1box = ttk.Combobox(form, textvariable = combophase1, width = 25)
    combophase1box.grid(row = 6, column = 1)
    phaselist = []
    for i in rm.FRAME_OPT.PH_SH_LEDs:
        phaselist.append(i)
    combophase1box['values'] = phaselist
    combophase1box.current(0)
```

Listing 1: Configuration of the GUI

PWM dimming

Let us now analyze the behavior of the duty cycle, phase shift and slew rate as configurable through the graphical user interface. The pulse width of each LED is programmed by setting a value in the WIDTHx register. A 10-bit counter, called TCNT, continuously counts from 0 to 1023 and then resets to zero. When the value in the PHASEx register is reached, which is

selected via a dropdown menu in the GUI, the LED turns on, as the switch placed in parallel with the LED is turned off (i.e. opened). Simultaneously, a second counter, WCNT, starts counting. When this counter reaches the value specified for the duty cycle in the GUI, the LED turns off, as the switch is turned back on. The slew rate is the rate at which an amplifier's output voltage changes over time, typically measured in volts per microsecond.

2.1.2 Communication protocol and frame composition

The second part of the system is dedicated to establishing and managing UART communication between the microcontroller unit (MCU) and the Matrix Manager devices. This communication is governed by a command and response protocol, which facilitates reading from and writing to device registers.

Serial communication initialization

The function `thread\_send\_serial()` is responsible for initializing the serial communication. It configures the serial port with parameters such as the baud rate, bytesize, parity and timeout. Following this setup, the function initiates the Matrix Manager by transmitting a set of essential configuration data:

- DATA_SYSCFG: We assign the hex value of 0x90 (in binary, 10010000). Doing this, the SEPTR pin enables separate TX/RX, signals on TX do not appear on RX, and putting 1 on the PSON pin the LED phase shifts apply to LED turn-on times

- DATA_PWMTCK: This register determines the divisor value applied to the input CLK, which generates the PWM clock cycle. Assigning the value of 0x06 (in binary, 00000110), the first divisor factor DIV1 is equal to 0 while the second divisor factor DIV2 is equal to 10. So the PWM clock is equal to:

$$PWM_{CLK} = \frac{CLK}{DIV1 \cdot DIV2}, \quad with \quad CLK = 16MHz \tag{2.1}$$

- DATA_SLEWRT: The LED bypass switch gate drivers have variable slew rates, one setting per LED sub-string. This is controlled by the SLEWRATE register, which we set to 0xFF as default

These data values are transmitted once at the beginning using the `send\_single\_serial\_command()` function

```
DATA_SYSCFG = bytearray()
DATA_SYSCFG.append(0x90)
send_single_serial_command(
    ser_obj     = ser,
    INIT_ser    = "W1",
    DEV_ID_ser  = "BROAD",
    REGADDR_ser = "SYSCFG",
    DATA_ser    = DATA_SYSCFG
```

Listing 2: Declaration and initialization of SYSCFG

```
def send_single_serial_command(ser_obj = serial.Serial(),
                               INIT_ser = rm.FRAM_OPT.INIT_FRAME["W1"],
                               DEV_ID_ser = rm.FRAM_OPT.INIT_FRAME["BROAD"],
                               REGADDR_ser = rm.FRAM_OPT.INIT_FRAME["SLEWRATE"],
                               DATA_ser = bytearray()):
    ser_obj.write(
        frame_composer(
            INIT    = INIT_ser
            DEV_ID  = DEV_ID_ser
            REGADDR = REGADDR_ser
            DATA = DATA_ser
        )
    )
```

Listing 3: Function for MM configuration

Data transmission and command functions

After the initial setup, the function `send\_serial\_command()` is invoked repeatedly to manage the cyclic transmission of data frames through the serial port.
The `send\_single\_serial\_command()` function is specifically designed to send the initial set of commands to the Matrix Manager. Its construction of the frame is accomplished through the `compose\_data\_frame()` function, which assembles a bytearray containing the values of the duty cycle, phase and slew rate.
Note that the duty cycle and phase values, which range from 0 to 1023, require 10 bits for representation. Since each register accommodates only 8 bits, these values are split across two registers. Following the register configuration specified in the datasheet, the values are rearranged and correctly stored in the data frame. Specifically:

- ”& 0xFF” : allows extracting the 8 least significant bits (LSBs), from 0 to 7, of the input value
- ”& 0x300” : extracts the higher part (MSBs), specifically bits 8 and 9

- ”$\gg 8$” : is used to shift the obtained value by 8 positions.

The proper organization of the data is ensured by using bit masking and bit shifting operations, in accordance with the datasheet specification.

```
def compose_data_frame(i = 0):
    data_frame = bytearray()
    if i == 1:
        global cd1box
        global cp1box
        data_frame = bytearray()
        data_frame.append(rm.FRAME_OPT.PH_SH_LEDs[cp1box.get()] & 0xFF)
        data_frame.append((rm.FRAME_OPT.PH_SH_LEDs[cp1box.get()] & 0x300) >> 8)
        data_frame.append(rm.FRAME_OPT.PH_SH_LEDs[cd1box.get()] & 0xFF)
        data_frame.append((rm.FRAME_OPT.PH_SH_LEDs[cd1box.get()] & 0x300) >> 8)
```

Listing 4: Function for the data frame

2.1.3 Frame structure as defined by the datasheet

The command frames follow a strict structure, as defined in the datasheet, which includes the following elements:

- Initialization Byte (INIT): This byte identifies the transaction type, whether it is a read or write operation, and indicates the number of data bytes contained in the frame. In this project, the strings `"W1"` and `"W4"` are used to denote the writing of 1 byte and 4 byte, respectively
- Device ID Byte (DEVID): Contains the unique identifier of the destination device
- Register Address Byte (REGADDR): Specifies the starting address of the register to be accessed
- Data Bytes: These bytes hold the actual data to be written, with the total number determined by the initialization byte
- CRC Bytes (CRCL and CRCH): The frame concludes with two bytes that represent a cyclic redundancy check (CRC), calculated using the CRC-16-IBM algorithm. These bytes ensure that any errors during transmission are detected

The Cyclic Redundancy Check (CRC) stands out as a powerful and widely adopted method for detecting detecting accidental alterations to raw data [16] . It serves as a validation method that uses mathematical formulas to generate a unique value, known as a checksum, for a block of data. This checksum, which is a fixed-size value, is then appended to the data block before

it is transmitted or stored. Upon receiving the data, the receiving device performs the same CRC algorithm to independently calculate a checksum based on the received data [17]. The integrity of the data is verified by comparing the calculated checksum with the checksum that was transmitted along with the data. If these two values match, it is highly probable that the data was transmitted or stored correctly.
CRC-16-IBM is a specific and widely used variant of the Cyclic Redundancy Check algorithm that generates a 16-bit checksum. In the context of CRC, a 16-bit CRC signifies that the resulting check value is 16 bits in length. The defining characteristic of CRC-16-IBM lies in its specific generator polynomial, which is mathematically expressed as $x^{16}+x^{15}+x^2+1$. This polynomial is of degree 16, indicating that it comprises 17 terms or coefficients. In hexadecimal notation, this polynomial is commonly represented as $0x8005$, assuming the most significant bit is either omitted or implied in the representation. It is also frequently encountered in its reversed form, $0xA001$, which is often preferred in software implementations and when using lookup tables for efficiency. Another crucial parameter in the CRC-16-IBM specification is the initial value of the CRC register. While some implementations initialize this register to $0x0000$, others utilize an initial value of 0xFFFF. The choice of initial value can influence the final CRC result. The XOR-out value, which is XORed with the final CRC result, is typically $0x0000$ for CRC-16-IBM , indicating that no such post-processing is applied. Below, we can see the code used to calculate the CRC-16-IBM and used later in the project to be able to communicate with the chip.

```
def crc16_ibm(data: bytes) -> int:
    """
    Calculate CRC-16-IBM
    Polynomial: 0x8005 (reflected 0xA001)
    Initial value: 0x0000
    Input and output are reflected.
    No final XOR.
    """
    crc = 0x0000
    for b in data:
        crc ^= b
        for _ in range(8):
            if crc & 0x0001:
                crc = (crc >> 1) ^ 0xA001  # Reflected polynomial
            else:
                crc >>= 1
    return crc
```

Listing 5: CRC-16-IBM function

This is the function used to calculate the CRC-16-IBM. The CRC is initialized to zero, as specified by the IBM variant. This initial state will be modified as each byte of the input data

is processed. Later on, the function iterates through each byte in the data sequence. Each byte is immediately XORed with the current CRC value. This operation injects the new data byte into the CRC register. Due to the reflected input convention, this XOR is performed directly on the least significant byte of the CRC. Now, for every bit in the byte the algorithm inspects the lowest bit of the CRC.
If it is 1, the CRC is shifted right by one position. This shift introduces a problem tho: we've lost a bit. So, to simulate the correction a real CRC circuit would perform, we XOR the CRC with $0xA001$, playing the tole of a divisior in this binary form of long division. If the lowest bit is 0, we shift to the right without XOR. No correction is needed; the data flowed as expected. This loop processes one byte, bit by bit, modifying the CRC in a wat that makes it sensitive to every little change in the input data.

```python
def compute_crc_bytes(frame: list) -> tuple:

    data = bytes(frame)
    crc = crc16_ibm(data)
    crc_low = crc & 0xFF
    crc_high = (crc >> 8) & 0xFF
    return crc_low, crc_high
```

Listing 6: Compute CRC frame

This function takes a list of bytes, computes CRC-16-IBM and returns CRC low and high bytes

```python
def main():
    # Example Modbus frame (slave ID = 0x01, function = 0x03, address = 0x0000, count
    ↪  = 0x000A)
    command_frame = [0x87, 0xBF, 0x38, 0x00]

    crc_low, crc_high = compute_crc_bytes(command_frame)

    full_frame = command_frame + [crc_low, crc_high]

    print("Original Frame (without CRC):", command_frame)
    print("CRC Low Byte:  0x{:02X}".format(crc_low))
    print("CRC High Byte: 0x{:02X}".format(crc_high))
    print("Full Frame (with CRC):", full_frame)

if name == "main":
    main()
```

Listing 7: Main function

In the main function we simply recall the functions explained above. Given a list of bytes, the code returns us the CRC low and high bytes

2.2 16 LEDs Code

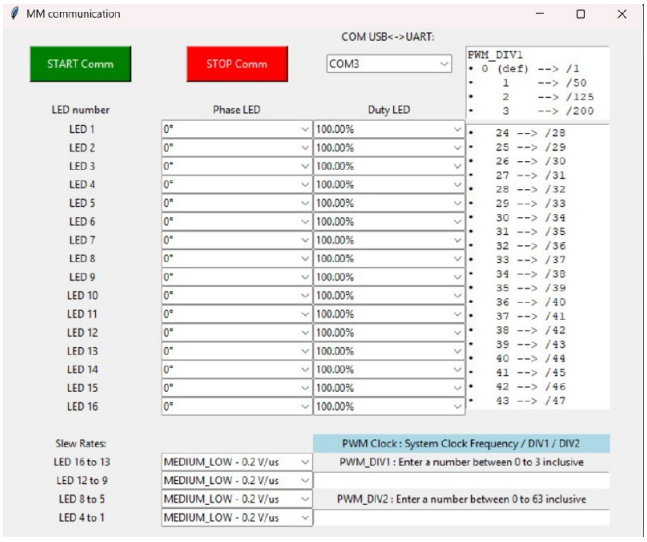


Figure 2.2: GUI 16 LEDs

We will now analyze the GUI used for the 16-LED device and highlight the main differences between the two codes and datasheets.
As can be seen, several new features have been added to the interface. Specifically, to the right of the Slew Rate control, there are two new input fields: PWM_DIV1 and PWM_DIV2. These allow the user to input values in order to set the PWM frequency. To provide a better understanding, an equation is displayed in the blue box showing how the PWM frequency is calculated, along with the corresponding divisors based on the values entered. These elements are shown in Figure 2.2. One of the main differences compared to the previously analysed code lied in the initialization of registers. In this updated version, in addition to the existing registers, the SLEWRTL, SLEWRTH, MTPCFG and OUTCTRL registers are also initialized using the same approach as before, specifically the `send_single_serial_command()` function.
The key difference, however, is in how the registers are managed. With a more advanced and recent version of the chip, the register structure has been redesigned and reorganized to make more efficient use of the available space. To accommodate this change, I had to update the `frame_composer` function to contruct the data frame in accordance with the new datasheet.
To achieve this, I developed four new functions to handle the high and low parts of the duty cycle and phase shift, naming them `frame_composerdl`,`frame_composerdh`, `frame_composerpl` and `frame_composerph`. These follow the same logic as the previous implementation, but use different

increments and include additional `if` conditions. Due to the confidential and proprietary nature of the new datasheet, I am unable to share further technical details.

2.3 DAvE IDE

The Digital Application Virtual Engineer (DAvE) represents a significant offering from Infineon, serving as a comprehensive software development and code generation tool specifically designed for microcontroller applications programmed in the C/C++ languages [18]. As the official Integrated Development Environment (IDE) from Infineon, it is inherently positioned to provide optimal support for their extensive range of microcontroller hardware. A key feature of DAvE lies in its capability for automatic code generation, which is achieved through the utilization of pre-configured and tested software modules known as DAVE Apps. Complementing the software environment is the Infineon XMC4700 Relax Kit [19], and evaluation board meticulously engineered to thoroughly assess the capabilities of the XMC4700 microcontroller. At the heart of this kit is the high-performance ARM Cortex-M4F core, capable of operating al clock speeds up to 144MHz. Facilitating seamless development is an integrated on-board debugger, the XMC4200 Debug IC, which supports both SWD (Serial Wire Debug) and SWO (Serial Wire Output) functionalities via a USB interface. The Relax Kit offers a comprehensive suite of connectivity options, including an Ethernet PHY and RJ45 Jack for network integration, a microSD Card slot for expandable data storage, and USB ports for communication and power.

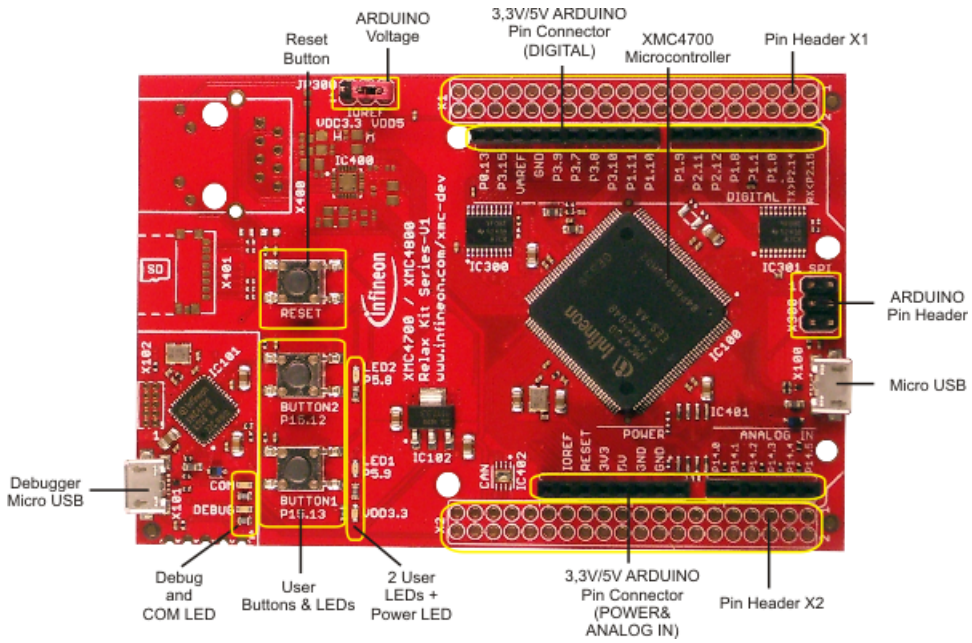


Figure 2.3: XMC4700 Relax Kit

2.3.1 Code implemented on the XMC4700

We will now analyze the code I developed, which is designed to receive data via USB and retransmit it through UART. To send data to the microcontroller, we use the program Hterm, which allows us to configure the data format and verify the correctness of the transmission by displaying the sent data.

```
1    #include  "DAVE.h"
2    #include <string.h>
3    #define BUFFER_SIZE 64
4    uint8_t rx_buffer[BUFFER_SIZE] = 0;
5    uint8_t tx_buffer[BUFFER_SIZE] = 0;
```

Listing 8: Libraries used in DAvE IDE

In the presented code snippet, the necessary libraries for peripheral initialization and memory-manipulation operations are first included: `"DAVE.h"`, automatically generated by Infineon DAvE tool for configuring XMC4700 microcontroller, and `<string.h>`, which provides standard functions for buffer copying and initialization. Next, the directive `#define` introduces a symbolic constant that defines, in bytes, the length of the two buffer employed in the system. The arrays `rx_buffer` and `tx_buffer`, both of type `uint8_t`, are each allocated 64 elements and explicitly initialized to zero; they serve, respectively, as the reception and transmission area for data. The former collects incoming bytes while the latter accumulates the information to be sent. Thanks to the explicit zero initialization, every element of both buffers is cleared at program load, ensuring a known and reproducible state at the start of communications.

```
1  static uint8_t UART_IsTxReady(void)
2  {
3      return -1;
4  }
```

Listing 9: UART_IsTxReady() function

The function `UART_IsTxReady` defines that the UART transmitter is ready, but can be replaced with a hardware-specific check of the UART status register to provide an accurate readiness indication

In the`UART_InitApp` function, the UART peripheral is configured and its initialization status is immediately verified. First, a variable of type `UART_STATUS_t` is assigned the result of calling `UART_INIT(&UART_0)`. If the returned status differs from the success code `UART_STATUS_SUCCESS`, an error message is emitted via the `XMC_DEBUG` macro

```
void UART_InitApp(void)
{
    UART_STATUS_t uart_status = UART_Init(&UART_0);
    if (uart_status != UART_STATUS_SUCCESS)
    {
        XMC_DEBUG("main: Application initialization failed");
        while(1U);
    }
}
```

Listing 10: UART_InitApp() function

```
static void UART_SendByte(unit8_t byte)
{
    UART_Transmit(&UART_0, &byte, 1);
}
```

Listing 11: UART_SendByte(unit8_t byte) function

In this implementation, the `UART_SendByte` function serves as a simple, statically-scoped helper that transmits exactly one byte over the UART interface. Internally, it invokes the more general `UART_Transmit`, given by DAvE IDE, passing the address of the single `uint8_t` datum and a length of 1, to enqueue the byte for transmission on `UART_0`.

In the main function, two local variables, `init_status` and `bytes`, are first declared: `init_status` stores the outcome of `DAVE_Init()`, which applies the clock,pin, peripheral and middleware configurations generated by the DAvE toolchain, while bytes will later record how many bytes have arrived from the USB Virtual COM port in each iteration of the processing loop. The program immediately calls `DAVE_Init()` and if this initialization succeeds it invokes `UART_InitApp()`, which in turn calls `UART_Init(&UART_0)` to configure the USIC channel for UART communication; on failure at either stage, a debug message is emitted via `XMC_DEBUG` and the system enters an infinite loop to prevent running in an uninitialized state. One the UART is ready, the code brings up the USB CDC interface by calling `USBD_VCOM_Connect()` and then blocks in `while(!USBD_VCOM_IsEnumDone());` until the host has fully enumerated the device. Thereafter, the application enters its perpetual data-forwarding loop: it queries `USBD_VCOM_BytesReceived()`, and whenever this returns a nonzero value it reads that many bytes into the 64-bytes `rx_buffer` using `USBD_VCOM_ReceiveData()`. Those same bytes are immediately duplicated into `tx_buffer` via `memcpy` and echoed back to the host with `USBD_VCOM_SendData()`. Concurrently, each byte is forwarded out the UART interface by first polling `UART_IsTxReady()`, which in this stubbed implementation always indicates readiness, and then transmitting

the byte with `UART_Transmit(&UART_0, &rx_buffer[i], 1)`, utilizing whichever transfer mode (interrupt, DMA, or direct polling) was configured. Throughout each loop iteration, `CDC_Device_USBTask(&USBD_VCOM_cdc_interface)` is called to service the USB stack's background tasks, such as state transitions, endpoint management and zero-length packet handling, thus maintaining a seamless, bidirectional bridge between the USB host and the serial peripheral.

```
int main(void)
{
    DAVE_STATUS_t init_status;
    uint16_t bytes = 0;
    init_status = DAVE_Init();
    if (init_status == DAVE_STATUS_SUCCESS)
    {
        UART_InitApp();
    }
    else
    {
        XMC_DEBUG("main: Application initialization failed");
        while(1U);
    }
    if (USBD_VCOM_Connect() != USBD_VCOM_STATUS_SUCCESS)
    {
        return -1;
    }
    while (!USBD_VCOM_IsEnumDone());
    while(1U)
    {
        bytes = USBD_VCOM_BytesReceived();
        if (bytes)
        {
            USBD_VCOM_ReceiveData(rx_buffer, bytes);
            memcpy(tx_buffer, rx_buffer, bytes);
            USBD_VCOM_SendData((const int8_t *)&tx_buffer[0], bytes);
            for(uint16_t i = 0; i < bytes; i++)
            {
                while (!UART_IsTxReady());
                UART_Transmit(&UART_0, &rx_buffer[i], 1);
            }
        }
        CDC_Device_USBTask(&USBD_VCOM_cdc_interface);
    }
    return 1U;
}
```

Listing 12: Transmitting data frames to the MCU

In Figure 2.4 we can see an example of some bytes sent via UART through the microcontroller explained previously and observe how this works. The data sent is:

$0x87 \quad 0xBF \quad 0x2A \quad 0xFF.$

It is possible noticing how the data is sent. There is a ”Start bit” equal to 0 (0 V), before every byte, and a ”Stop bit” equal to 1 (3.3V) after every byte. Let’s analyze the first byte, $0x87$ that is equal to 10000111. At the beginning of the data frame, we see that from 3.3V we drop

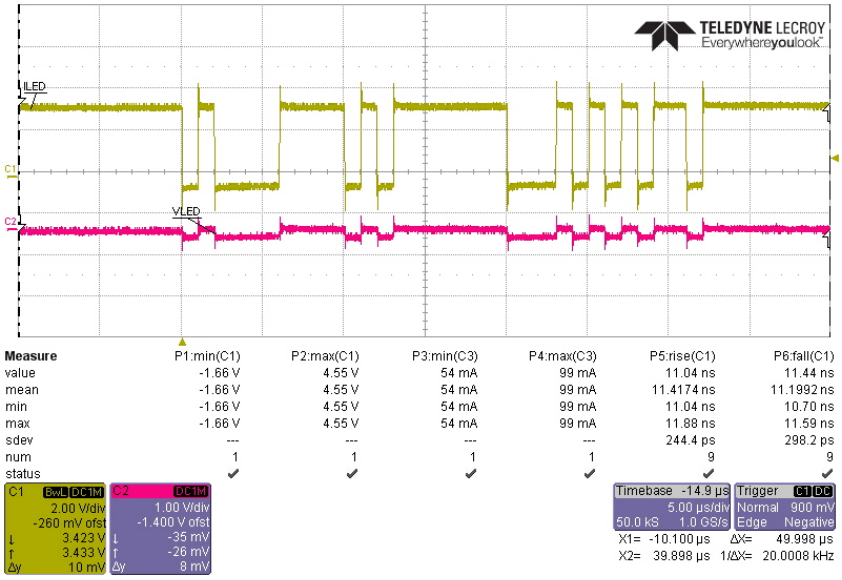


Figure 2.4: Example of data sent

2.4 MATLAB code

Below, is an example of a code written in MATLAB when I was able to communicate to the chip. In this code, I create a snake that moves turning on and off the LEDs.
Firstly, we configure the serial port used to communicate with the microcontroller XMC4700, creating and opening an object of the serial port. Secondly, we initialize some variables that we want to write to the chip, writing the register, the data, ecc. Lastly, we used the method `write()` to send to the chip the variables created before to create the shape of the snake that moves.

```
% --- Configuration ---

portName = "COM8";
baudrate = 115200;

% --- Open Serial Port ---

s = serialport(portName, baudrate);

% --- clear any old data

flush(s);

% --- Prepare your byte array ---

SYSCFG = uint8([0xXX, 0xXX, 0xXX, 0xXX, 0xXX, 0xXX]);
MTPCFG = uint8([0xXX, 0xXX, 0xXX, 0xXX, 0xXX, 0xXX]);

LED1_ON = uint8([0xXX, 0xXX, 0xXX, 0xXX, 0xXX, 0xXX]);
% ... rest of the LEDs data frame

% --- Send the byte

write(s, SYSCFG, "uint8");
% read(s,6,"uint8")
pause(1);
write(s, MTPCFG, "uint8");
% read(s,6,"uint8")
pause(1);
for i = 1:5
    write(s, LED16_ON, "uint8");
    % read(s,6,"uint8")
    pause(0.1);
    write(s, LED15_ON, "uint8");
    % read(s,6,"uint8")
    pause(0.1);
    write(s, LED14_ON, "uint8");
    % read(s,6,"uint8")
    pause(0.1);
    write(s, LED16_OFF, "uint8");
    write(s, LED13_ON, "uint8");
    pause(0.1);
    write(s, LED15_OFF, "uint8");
    write(s, LED12_ON, "uint8");
    % ecc...
    flush(s);

end
```

Listing 13: Snake shape in MATLAB

Chapter 3

Simulations

3.1 Peak current mode control simulation

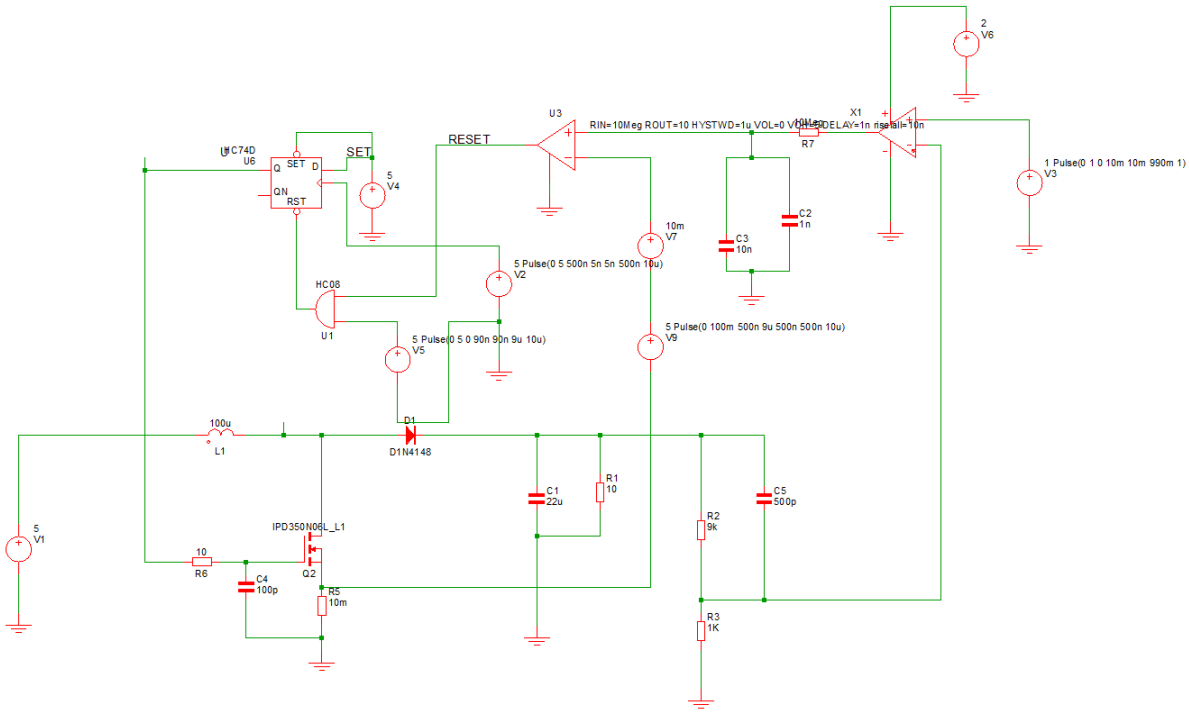


Figure 3.1: PCMC simulation

In this simulation, a Boost converter operating under Peak Current Mode Control (PCMC) was implemented to evaluate its dynamic performance and regulatory behavior in comparison to voltage mode regulation. The power stage consists of a $100\mu H$ inductor (L1), a low R_{DS} N channel MOSFET (Q2, IPD350N06L), a fast switching diode (D1, 1N4148), and an electrolytic output capacitor (C1, $22\mu F$). The inductor value was selected to balance the trade-off between current ripple and dynamic response at the target switching frequency range, and the output

capacitor ensures low voltage ripple at the load. The MOSFET is driven by SET and RESET signals generated by a clock-like SET signal (V4) and a current-threshold-based RESET signal derived from comparator U3.
The peak inductor current is sensed via the voltage across a $10m$ current sense resistor (R5) placed between the MOSFET source and ground. This sensed voltage is compared against a reference (V7) using a high-impedance comparator (U3), configured with $R_{IN} = 10M$ to model minimal loading on the current signal. The very high resistance of R7 ($10M$), placed in series with the comparator's positive input, serves to isolate the comparator from the RC filtering network (C2 = 1nF and C3 = 10nF) while preserving the integrity of the current signal. This setup ensures that only the low-frequency content of the current ramp reaches the comparator, effectively rejecting high-frequency noise and spurious spikes, which is essential for avoiding false triggering and ensuring clean switching transitions. The comparator's output acs as a RESET signal to the SR flip-flop (U6). When the flip-flop is SET by the rising edge of V4, Q2 turns ON, allowing current to ramp up in the inductor. As soon as the sensed current exceeds the threshold set by V7, U3 toggles the flip-flop via the RESET input, turning OFF the MOSFET immediately. This cycle-by-cycle current limiting mechanism provides precise control over peak current, enhancing converter stability, improving transient response, and inherently protecting against overcurrent conditions.
The AND gate (U1, 74HC08) is used to gate the SET signal with auxiliary logic pulses (V5), allowing conditional enabling of the convert. This could emulate a soft-start, enable pin or system-level condition. A diode (D1, 1N4148) provides a fast and efficient path for inductor current during the OFF state. Though it is typically a small-signal diode, its fast recovery and low forward voltage drop make is suitable for simulation purposes where switching speed and clean transitions are prioritized.
Gate driver is managed through a 10 resistor (R6) and a $100pF$ capacitor (C4) models parasitic gate capacitance and contributes to noise shaping. On the output side, a resistive divider (R2 = $9k$, R3 = $1k$) steps down the output voltage for potential feedback or monitoring. To further reduce high-frequency switching noise, a small filtering capacitor (C5 = 500pF) is placed at the divider midpoint. THe control loop ensures that each switching cycle starts with Q2 turning ON and ends precisely when the peak current threshold is reached. This peak current control, unlike voltage mode regulation, provides faster response to line and load transients, better damping of duty cycle instability (especially at duty cycle > 50%) and eliminates the need for an artificial ramp to prevent subharmonic oscillation. Additionally, the high input impedance path through R7 avoids loading the sense signal while allowing adequate filtering, demonstrating how component choices and values play a critical role in shaping the loop dynamics. Simulation stimuli such as V2, V5 and V9 inject controlled pulses and disturbances into the system to validate the

converter's behavior under realistic dynamic conditions. The entire simulation aims to replicate typical startup, steady-state and transient behavior of a digitally-triggered, analog-controlled Boost converter with precise peak current regulation.

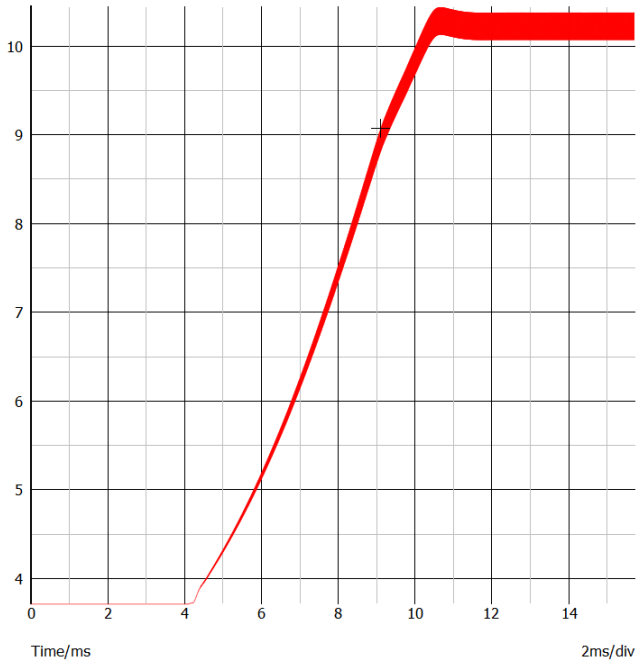


Figure 3.2: PCMC graph

3.2 TLD6099-2ES Simulations

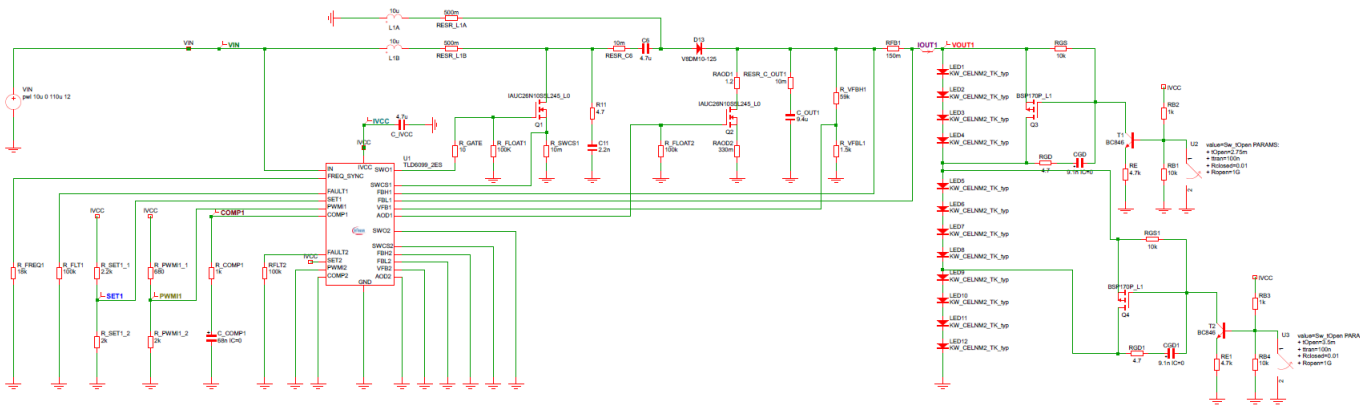


Figure 3.3: TLD6099-2ES

The core of the TLD6099-2ES is its dual, independent switching regulator channels. Each channel employs a peak current control loop to regulate the output current with a specified

accuracy of $\pm 3.5\%$ (under no analog dimming conditions). To ensure stability, particularly at high duty cycles ($> 50\%$), the device incorporates an internal slope compensation mechanism to prevent sub-harmonic oscillations. This architecture provides significant flexibility, allowing for implementation in various DC/DC converter topologies, including Boost-to-ground, Boost-to-battery, SEPIC, and Flyback configurations.
A soft start routine is integrated into each channel to manage inrush currents and prevent output voltage overshoot during power-up or recovery from fault conditions. This routine incrementally adjusts the internal reference voltage over a defined period ensuring a smooth and controlled rise in output current.

Frequency Management

The switching frequency is configurable via an external resistor connecter to the FREQ_SYNC pin (R_FREQ1), allowing operation in a range from 100 kHz to 500kHz, or at a fixed high frequency of 2.2MHz. This flexibility allows designers to balance efficiency, component size and thermal performance. To mitigate electromagnetic interference (EMI), a significant challenge in high-frequency modulator. This feature dithers the switching frequency around a central point, distributing switching noise across a broader band to facilitate compliance with stringent emission standards. Furthermore, the device can be synchronized to an external system clock.

Dimming Capabilities

The controller supports two distinct dimming methodologies per channel:

- Analog dimming: The average output current is adjusted by applying an analog voltage to the SETn pin. This voltage directly modulates the internal reference voltage providing a linear and continuous method of brightness control.
- Digital PWM dimming: The PWMIn pin accepts a pulse-width modulated signal to gate the output current on and off. This method preserves the LED's chromaticity across a wide range of brightness levels by modulating the average current over time

Adaptive Output Discharge - AOD

To manage rapid load changes, such as those occurring in adaptive driving beam (ADB) matrix managers or when switching between high and low beams, the device includes an Adaptive Output Discharge function. This feature drives an external NMOS transistor to quickly discharge the output capacitance, preventing current spikes and protecting the LEDs from electrical overstress.

3.2.1 Waveform analysis

The provided graph illustrates the dynamic performance of a single channel of the TLD6099-2ES controller during startup and under varying load conditions. The waveforms represent key operational parameters: the error amplifier output (COMP1), the regulated output current (IOUT1), the output voltage (VOUT1), the input voltage (VIN), the internal regulated voltage (IVCC) and the analog dimming setpoint (VSET1).

Phase 1: Initialization and soft start

This initial phase demonstrates the controlled power up sequence of the controller, governed by the soft-start mechanism.
The green trace, representing the input voltage (VIN), steps up to approximately 12.5V, providing power to the system. Concurrently, the cyan trace, identified as the internal 5V supply (IVCC), begins to ramp up. As per the datasheet, the TLD6099-2ES becomes operational once IVCC crosses its undervoltage switch-on threshold enabling the internal logic.
The blue trace, representing the analog dimming input VSET1, ramps linearly from $0V$ to $2.5V$. According to the datasheet, the SET1 pin voltage directly controls the internal reference voltage, thereby commanding the target output current.
The controller initiates its softstart routine, a feature designed to prevent output overshoot and limit inrush current. This is visible in several traces:

- COMP1 (Brown trace): the error amplifier output begins to ramp steeply. The controller is increasing the duty cycle of the power switch to build up current and volttage at the output.
- IOUT1 (Purple trace): The output current begins to rise smoothly, following the command set by the softstart and the VSET1 ramp
- VOUT1 (Red trace): The output voltage rises in correspondence with the output current. The voltage must increase to match the forward voltage of the LED string at the target current

By $t = 2.0ms$, the soft-start routine is complete. The system has reached a steady state where IOUT1 is regulated at approximately $0.9A$, and the output voltage VOUT1 has stabilized at $32V$ to drive this current through the specific LED load.

Phase 2: Steady-state regulation

During this period, the controller is in stable, closed loop operation. All key parameters are held constant, demonstrating the controller's ability to maintain precise current regulation under

a static load.

Phase 3: Load Transient

This phase testes the controller's response to a sudden change in load impedance.

- Load Change: At $t = 2.8ms$, the output voltage VOUT1 is intentionally reduced from 32V to 25V. This simulates a scenario where several LEDs in the string are shorted or bypassed, reducing the total forward voltage of the load.
- Controller response: To prevent the output current from surging due to the lower loa impedance, the TLD6099 control loop reacts instantly. The COMP1 voltage drops sharply, which reduces the switching duty cycle.
- Re-regulation: The output current IOUT1 exhibits a brief transient but is rapidly brought back under regulation at a new, slightly higher steady-state value of $1.05A$. This demonstrates the fast transient response of the peak current control loop.

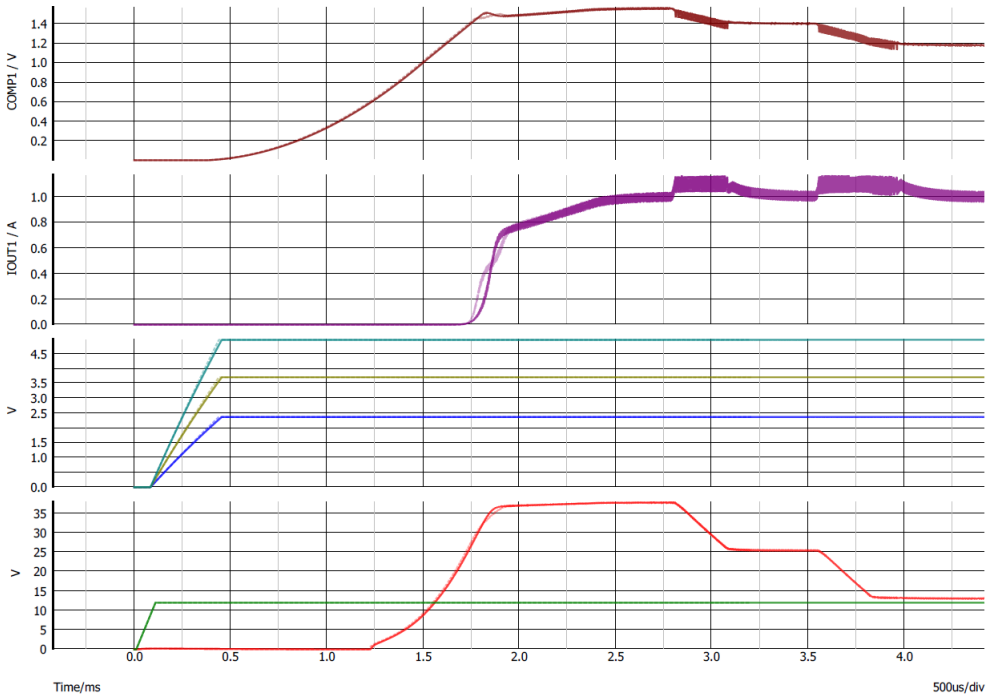


Figure 3.4: TLD6099-2ES graph

3.2.2 Changing the value of C_OUT1

This analysis investigates the performance of the TLD6099-2ES controller when the output capacitance C_OUT1 is increased to $100\mu F$, a more than tenfold increase from the previous

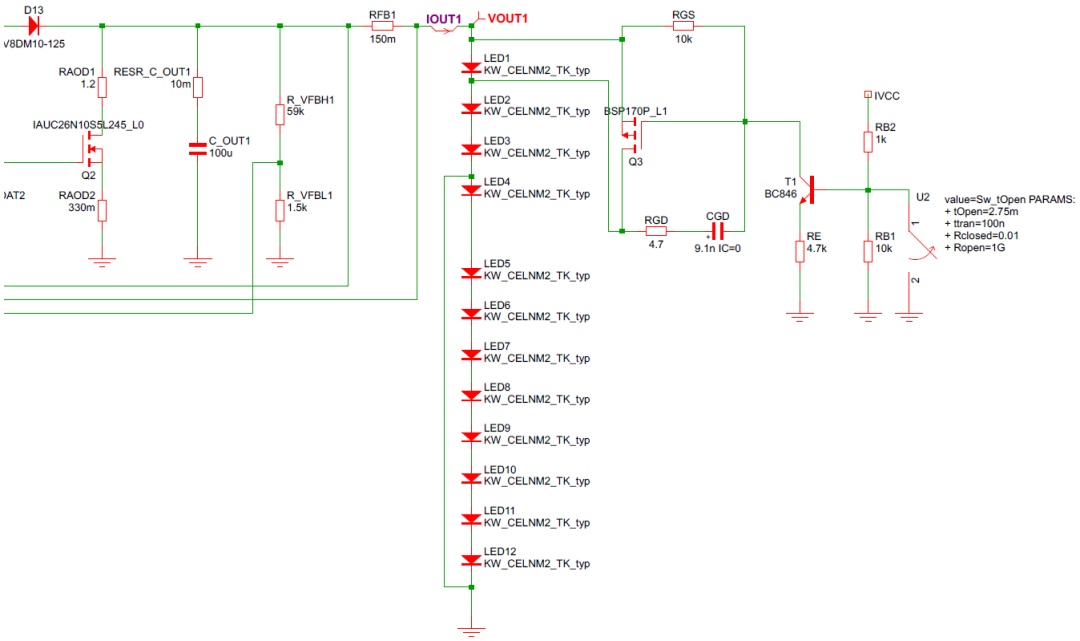


Figure 3.5: TLD6099-2ES with $C\_OUT1 = 100\mu F$

case. This modification significantly alters the system's output filter characteristics, leading to noticeable changes in both the startup transient and the response to dynamic load changes.

The initial powerup sequence remains conceptually the same, but the timing is extended due to the larger output capacitance. The output current begins its ramp at approximately $t = 1.6ms$. The most prominent difference is the significantly slower rise time of the output voltage VOUT1 (red trace).

One the initial charging transient is complete, the controller demonstrates stable regulation. In this phase, IOUT1 is held constant at $0.8A$. A key benefit of the larger output capacitor is evident here: it provides a larger energy reservoir, which effectively filters high frequency ripple, resulting in a smoother DC output current and voltage compared to a system with a smaller capacitor.

At $2.8ms$, the output voltage is forced to drop from $9.5V$ to $7V$, simulating a sudden decrease in load impedance. Unlike the wellbehaved response in the previous scenario, the output current exhibits a large, uncontrolled spike, peaking at approximately $1.1A$. This spike is not generated by the controller; it is the direct result of the energy stored in the $100\mu F$ capacitor being rapidly discharged into the new, lower-impedance load path. The control loop is too slow to prevent this initial discharge event. The TLD6099 control loop detects this current surge and reacts aggressively by sharply decreasing the COMP1 voltage, attempting to cut off the current. However, the large capacitor introduces significant phase lag into the feedback loop. This lag reduces the system's phase margin, a critical metric for stability.

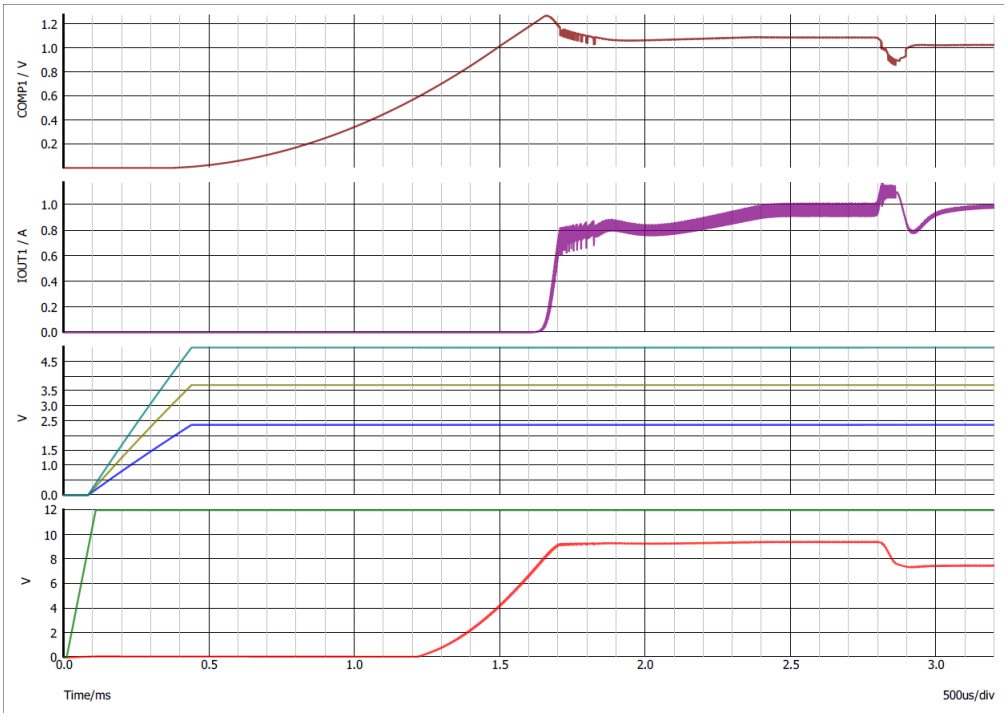


Figure 3.6: TLD6099-2ES simulation with $C\_OUT1 = 100\mu F$

Chapter 4

LAB Measurements

4.1 Evaluation with the 12LEDs board

In this section we will analyze the behavior of the 12 LEDs board, using the TLD6099-2ES and the current generator, confronting later on the two different setups and explaining the differences.

4.1.1 Evaluation with the TLD6099-2ES

Configuration 1

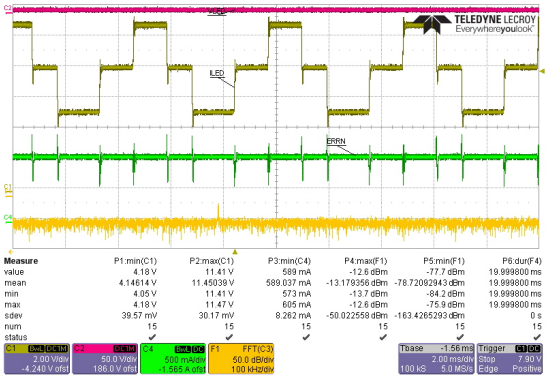
We first analyze the behavior with the TLD6099-2ES. The first configuration use is shown in Table 4.1

LEDs	DUTY CYCLE	PHASE
$LED01$	100%	0°
$LED02$	53%	90°
$LED03$	53%	180°

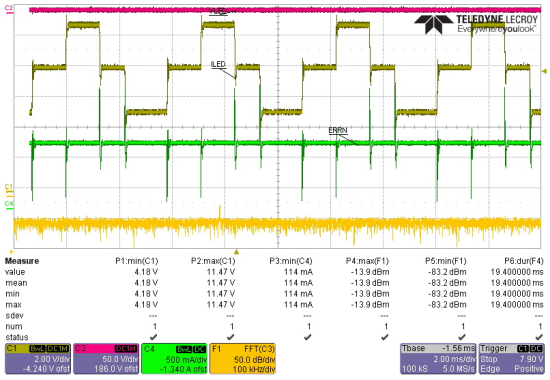
Table 4.1: Config 1 : Phase $\neq 0$

From Table 4.1 we observe that LED01 is always ON, while LED02 and LED03 have a duty cycle of 53%, meaning that they will stay ON for half a period, and are phase shifted of 90° and 180° respectively.

Figure 4.1(a) displays the voltage and current waveforms of the LED string operating under configuration 1, as previously described. The setup employs the TLD6099-2ES controller using a SEPIC DC-DC converter topology with an Adaptive Output Driver (AOD) for precise current regulation. The voltage was measured across the putput terminals of the SEPIC stage, while the



(a) Configuration 1 with slow slope



(b) Configuration 1 with fast slope

Figure 4.1: Configuration 1 with TLD6099-2ES

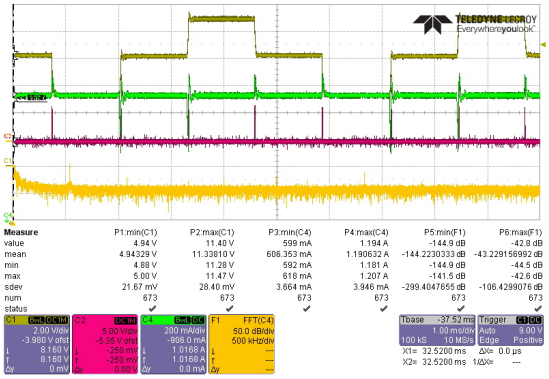
current was measured using a current probe placed in series with the LED string.

From the waveforms, we can observe pronounced current spikes that occur each time the output voltage steps up or down, corresponding to an LED turning on or off. When a single LED is active, the output voltage is approximately $4.18V$; when all three LEDs are on, the voltage reaches $11.47V$. This confirms a voltage drop of around $3.5V$ per LED, which is consistent with standard high-brightness LED characteristics.

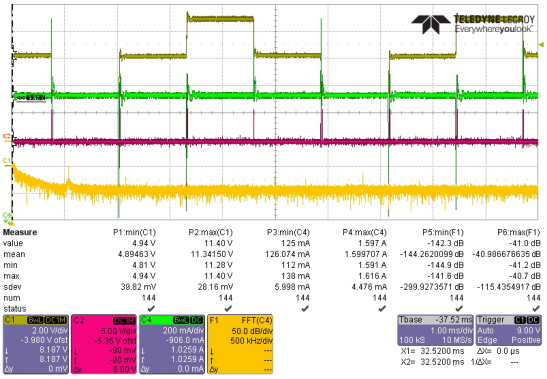
Despite these abrupt changes in voltage, the AOD ensures that the current quickly stabilizes at $\sim 1.2A$, demonstrating the effectiveness of the control loop. The yellow trace (Fast Fourier Transform FFT of the current signal) reveals small voltage transients that occur at each switching event. While output capacitors help to buffer and smooth these transitions, their effectiveness is limited under fastslope conditions, and some high-frequency noise still propagates through the system.

Comparing Figure 4.1 (b) to Figure 4.1 (a) highlights the impact of slope control. In Figure 4.1 (b), a steeper voltage slope is applied, leading to higher and sharper current spikes, as the system has less to respond to rapid load changes. In contrast, the slower slope in Figure 4.1 (a) allows the TLD6099-2ES to better regulate current during transitions, resulting in lower peak amplitudes. Controlling the slope is not only important for proper current regulation, but also plays a crucial role in reducing electromagnetic interference (EMI) and minimizing stress on power components, thereby enhancing the longterm reliability of the system.

Thanks to Figures 4.2 (a) and 4.2 (b), it is possible to clearly observe when the Adaptive Output Discharge becomes active. The purple trace (Channel C2) shows the AOD activation events: each pulse represents a control action aimed at limiting the current overshoot. As a result, the current waveform (green) exhibits reduced peak amplitudes and faster settling times, confirming the effective intervention of the AOD loop. This behavior not only enhances regulation but also contributes to lower EMI, reduced power losses, and better reliability of the overall



(a) Configuration 1 with slow slope and AOD



(b) Configuration 1 with fast slope and AOD

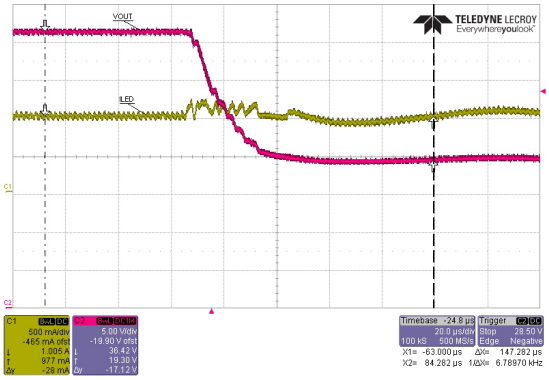
Figure 4.2: Configuration 1 with TLD6099-2ES and AOD

system.

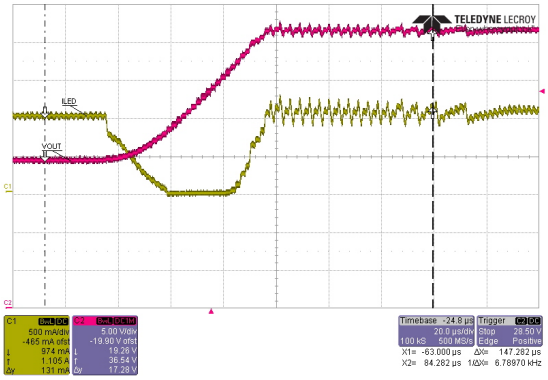
From Figures 4.3(a) and 4.3(b), the operation of the Adaptive Output Driver (AOD) can be clearly observed. In both cases, it effectively limits the output current, preventing it from rising beyond a certain threshold even during sudden load transitions.

In Figure 4.3(a), a different configuration is used compared to the previous tests: a step change occurs where 6 LEDs are turned on simultaneously, resulting in a sharp voltage increase from 19.26 V to 36.54 V. Despite this large voltage step, the current remains well-regulated and does not exceed 1.25 A, demonstrating the AOD's capability to suppress overcurrent peaks.

In Figure 4.3(b), the opposite situation is shown, where the system transitions from 12 LEDs to 6 LEDs, reducing the load. Once again, the AOD intervenes to stabilize the current rapidly and prevent oscillations, ensuring safe and stable operation under dynamic conditions.



(a) Jump from 12 LEDs on to 6



(b) Jump from 6 LEDs on to 12

Figure 4.3: AOD behavior

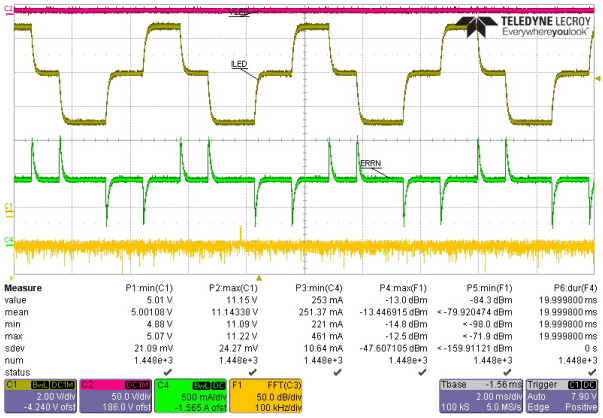


Figure 4.4: 12 LED load using the current generator

4.1.2 Evaluation with an ideal current generator

The test bench consists of a 12-LED string arranged in configuration 1 driven by a programmable, ”ideal” current source rather than the TLD6099-2ES and AOD. The output current was set to $\sim 1A$, and both voltage and current waveforms were captured on a LeCroy waveRunner 64Xi oscilloscope. Voltage was measured across the entire LED string (Channel 1, yellowbrown), while current was monitored in series with the LEDs using a high-bandwidth current probe (Channel 4, green). An FFT analysis (Channel F1, yellow trace) was also recorded to assess high-frequency content during each switching event. In the oscilloscope screenshot above (Figure 4.4), you can see the voltage waveform stepping each time an LED in the matrix turns on or off. The current trace exhibits sharp transients at each switch event, then rings and slowly settles toward the programmed current.

Because the ideal current source forces a fixed current regardless of load, it does not react instantaneously by stepping its output voltage. Instead, it modulates its internal voltage smoothly until the LED string conducts the set current. There is therefore no abrupt voltage jump (spike) as seen when driving from a fast-acting DC-DC converter without proper slope control. An ”ideal” current source in practice still has internal dynamics (compliance voltage limits, control loop bandwidth, output capacitance). When the LED string suddenly changes its forward voltage, the generator’s loop takes finite time to adjust its output voltage to maintain the set current. This causes transient overshoots and undershoots (ringing), visible as spikes and damped oscillations in the green trace.

Without the AOD’s fast, dedicated clamp action, the generator’s regulation loop is slower. It may take several hundred microseconds, or more, to settle to the target current after each load step. During this unsettled period, the instantaneous current can exceed safe limits, stressing the LED junctions thermally or electrically. Prolonged or repeated over-current events could degrade lifetime or even cause immediate damage, which is why a fast-acting current.limiting

driver (like the AOD) is critical for protecting the LEDs under dynamic switching conditions.

When compared to the slow slope case, the fast slope waveform exhibits noticeably larger current overshoots and significantly sharper transient edges that generate more pronounced ringing, as you can see in Figure 4.5 . These steeper transitions also translate into richer high-frequency content in the FFT, reflecting the abrupt nature of each voltage step. Although both configurations rely on the same currentsource control loop and therefore require a finite settling time to return to the expected value set point, the fast-slope scenario produces a larger initial deviation before stabilization. This behavior underscores how increasing the voltage ramp rate stresses the loop's bandwidth limits and why a fast-acting AOD driver is essential to suppress such excursions.

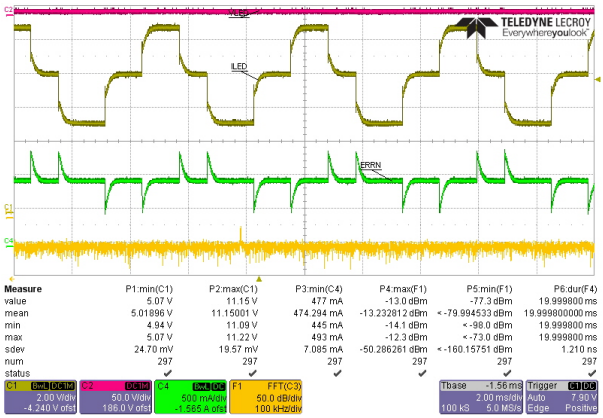


Figure 4.5: 12 LED load using the current generator with fast slope

4.2 Testing with the Evaluation Kit

In this section we will analyze the behavior of the Evaluation Kit given by Infineon.

4.2.1 Eval. Kit with Configuration 1

As shown in Figure 4.6, the current and voltage waveforms produced by the Evaluation Kit differ markedly from those we examined in the previous section. In the slowslope setting, the familiar voltage spikes that occurred each time another LED was switched in have all but disappeared, and the current no longer exhibits the severe overshoot that risks damaging the LEDs. Instead, the LED string voltage rises smoothly through its three forward drops, up to $10.6V$ when all three are conducting, forming gentler, less pronounced steps. Meanwhile, the current loop maintains a nearly constant level during each on-state. Overall, the result is a much gentler ramp both in voltage and current, offering enhanced LED protection and cleaner system behavior.

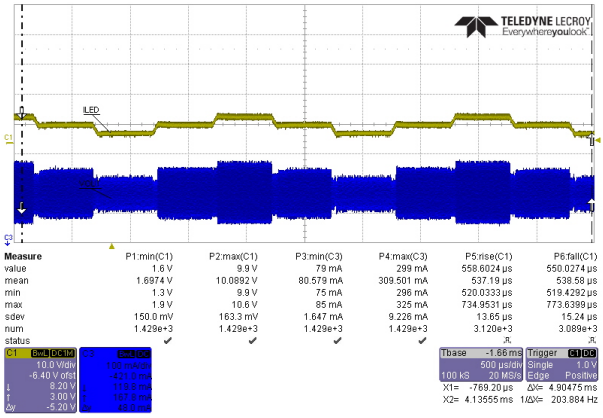
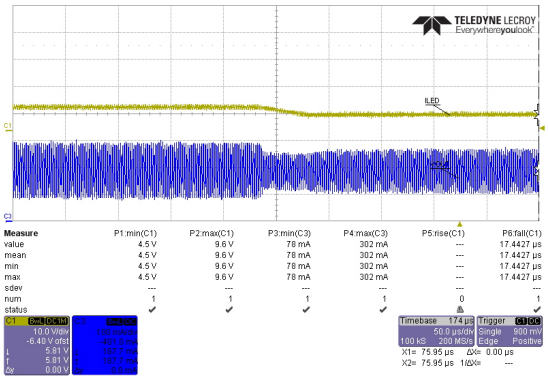
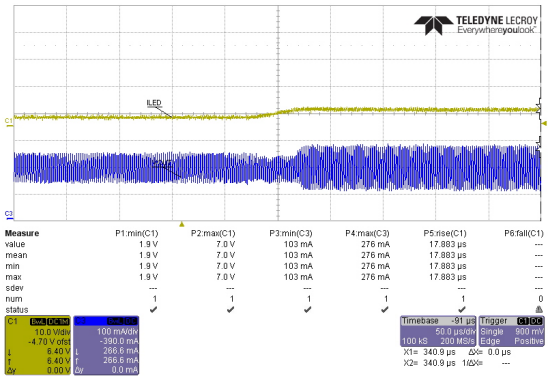


Figure 4.6: Configuration 1 with Eval. Kit and slow slope

By observing Figure 4.7(a) and Figure 4.7(b) we can see the rise and fall times of the voltage waveform corresponding to a single LED voltage drop. The rise time is measured to be $17.883\mu s$, while the fall time is $17.4427\mu s$.



(a) Configuration 1 – Fall time with slow slope



(b) Configuration 1 – Rise time with slow slope

Figure 4.7: Configuration 1 – Fall and rise times with slow slope

Unlike the slow slope, the medium slope (see Figure 4.8) produces a cleaner and more stable waveform. It exhibits fewer overshoots and spikes compared to the fast slope, though still more than with the slow slope. In the voltage waveform, the LED voltage steps have sharper transitions. The medium enables faster transitions and less smoothing than the slow slope, resulting in sharper edges. This can lead to marginally higher switching losses, but it also improves efficiency and responsiveness.

In Figure 4.9(a) and Figure 4.9(b), we notice the fall and rise time with medium slope. Compared to the slow slope, the medium one significantly reduces the transition times. Specifically, the fall time is $2.7885\ \mu s$ and the rise time is $3.070\ \mu s$, both nearly $15\ \mu s$ shorter than those observed with the slow slope.

Finally, in configuration 1 with the fast slope setting (Figure 4.10), a very sharp and

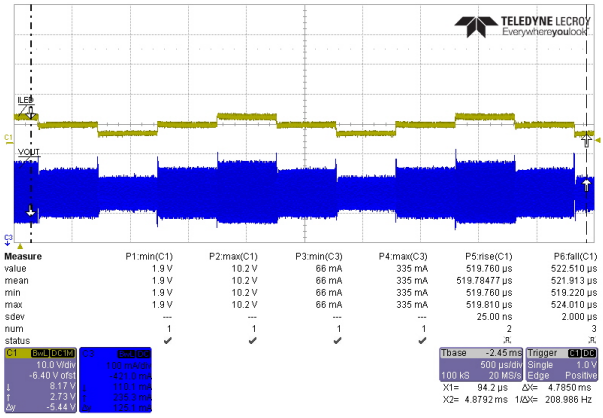
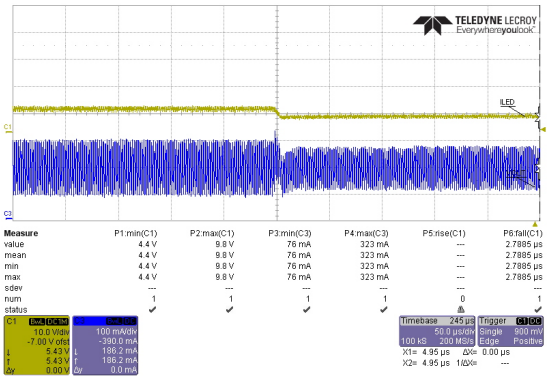
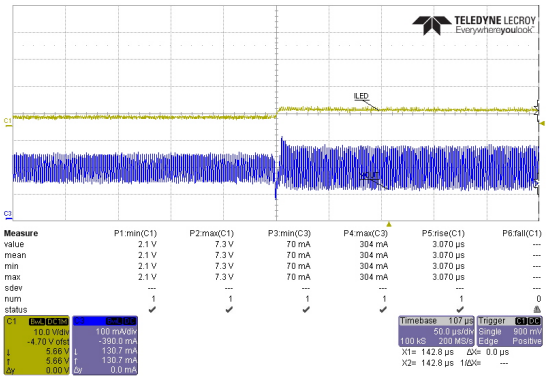


Figure 4.8: Configuration 1 with Eval. Kit and medium slope



(a) Configuration 1 Fall time with medium slope



(b) Configuration 1 Rise time with medium slope

Figure 4.9: Configuration 1 Fall and rise times with medium slope

fast switching behavior can be observed. The current waveform (C3) shows very distinct, rectangularshaped pulses, with a peak value of approximately $379\ mA$ and a minimum of $24\ mA$. The voltage (C1) also exhibits extremely steep and welldefined edges, rising sharply from $1.6\ V$ to $10.2\ V$, indicating the high speed of the slope control mechanism. This behavior results in a very responsive and fast system, but it may also cause increased electromagnetic interference and greater stress on the components due to the steep transitions and large current spikes.

In the end, we can notice in Figure 4.11(a) and Figure 4.11(b) the fall and rise times with fast slope. The fall time is equal to $2.178\ \mu s$, while the rise time is $1.527\ \mu s$

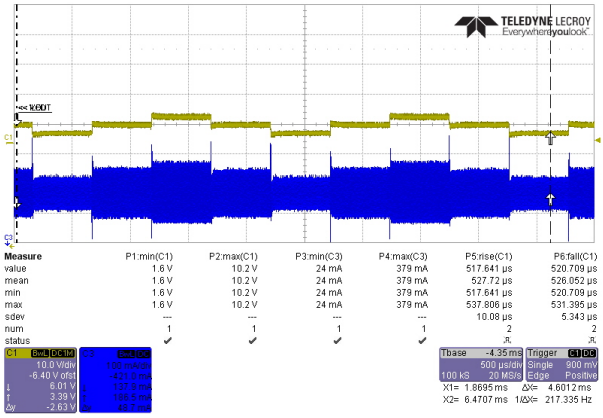
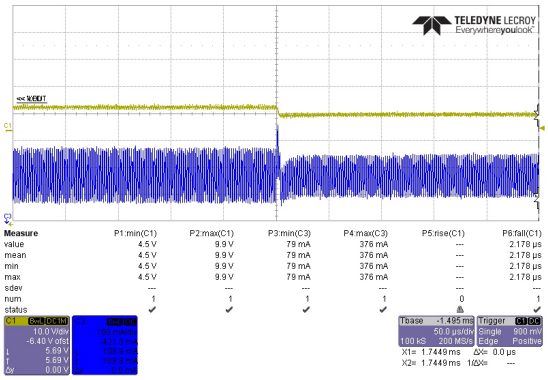
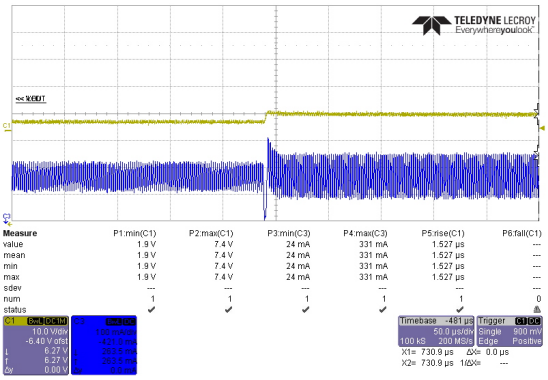


Figure 4.10: Configuration 1 with Eval. Kit and fast slope



(a) Configuration 1 Fall time with fast slope



(b) Configuration 1 Rise time with fast slope

Figure 4.11: Configuration 1 Fall and rise times with fast slope

4.2.2 Eval. Kit with Configuration 2

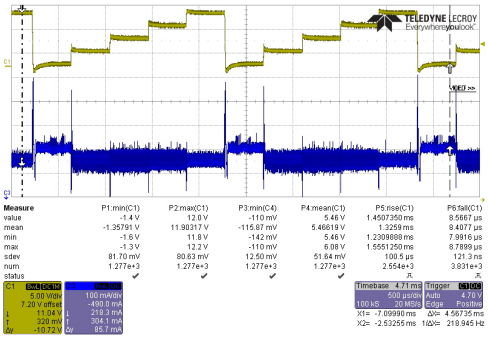
In configuration 2, with fast slope, four LEDs share the same phase but have different duty cycle. At some point, all four LEDs turn off simultaneously, causing the bus voltage to drop by about $12\ V$ and producing a current spike of roughly $300\ mA$.

From the waveform measurements (see Figure 4.12(b)), we also see that the voltage fall time stretches to about $7.2107\ \mu s$, substantially longer than the $1-2\ \mu s$ we observed in the previous subsection when just one LED switches off, because four diodes are discharging in unison.

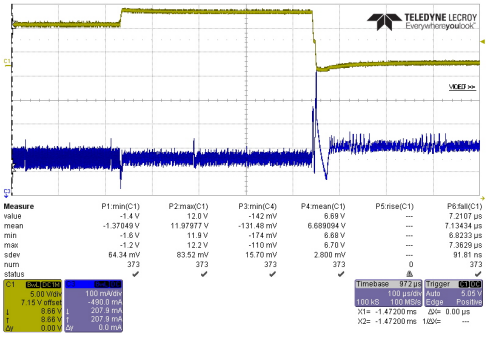
Overall, Configuration 2 highlights the classic trade-off in fastslope charge pump driving: engaging more diodes per edge speeds up average switching but amplifies voltage transients, current spikes and thermal stress.

LEDs	DUTY CYCLE	PHASE
$LED01$	80 %	0°
$LED02$	60 %	0°
$LED03$	40 %	0°
$LED04$	20 %	0°

Table 4.2: Configuration 2 : Phase $= 0$



(a) Configuration 2 with fast slope



(b) Configuration 2 with fast slope Fall time

Figure 4.12: Configuration 2 with Eval. Kit

4.3 TLP measurements

We will now discuss about the results taken in the laboratory about TLP method discussed in Chapter 2 - Theory Notes.

4.3.1 PIN1 - PIN2

In this initial configuration, it can be observed that the device begins to conduct significantly at around $3V$. Below this threshold, the current is almost negligible, The device has an activation threshold near $3V$, making it suitable for protecting circuits operating below this voltage level. Between approximately $3.5V$ and $5V$, the current rises rapidly, displaying typical clamping behavior. In this region, the pin functions as an ESD protection element, absorbing current and maintaining a relatively stable voltage. The curve reaches a peak current of about $0.75 - 0.78A$ at $5V$ before abruptly stopping.

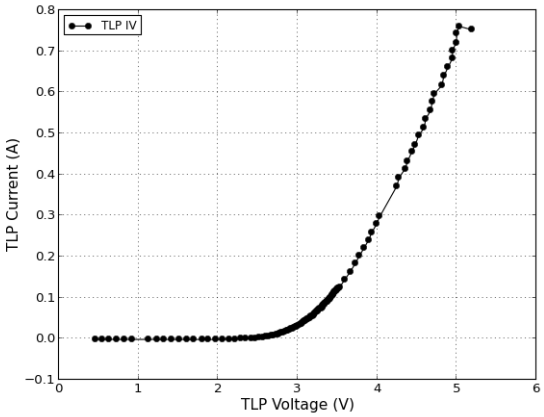


Figure 4.13: IV plot of PIN1 - PIN2

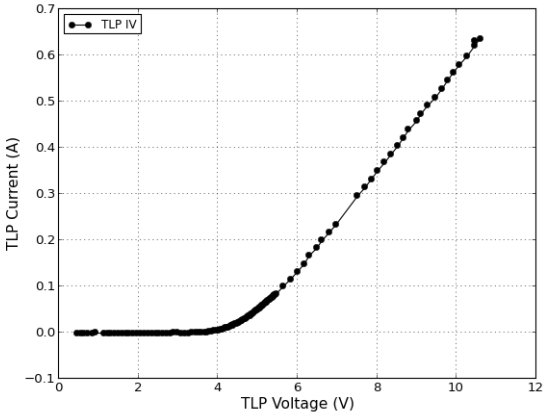


Figure 4.14: IV plot of PIN1 - PIN18

4.3.2 PIN1 - PIN18

This graph (Figure 4.14) exhibits behavior similar to the one previously analyzed, but with notable differences. In this case, the pin starts conducting significantly around $5V$; below this value, the current is almost zero. This higher threshold compared to the first graph may indicate that the pin is designed for higher supply voltages, or that the ESD protection is less sensitive, or that the device is intended not to activate too early. From $5V$ to $10V$, the current gradually rises up to about $0.65A$. The curve is very linear, with no signs of saturation, reflecting behavior more akin to a variable resistor than a sharp clamp.

4.3.3 PIN10 - PIN18

Figure 4.15 paints a picture of a highly sensitive ESD protection circuit. As the voltage across this pin increases from zero, the current remains virtually non-existent until it reaches a

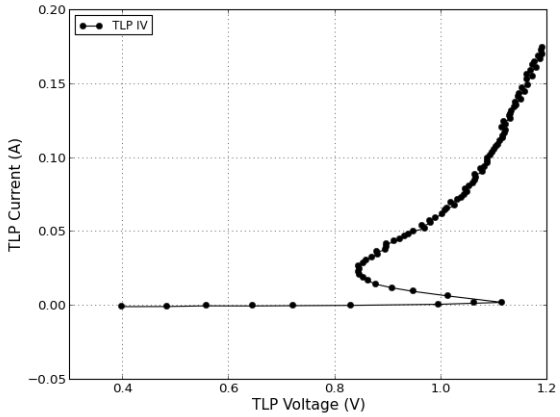


Figure 4.15: IV plot of PIN10 - PIN18

critical point, the trigger voltage, which is quite low at approximately 0.8 V. At this threshold, the device abruptly switches from a high-impedance (off) state to a low-impedance (on) state. This rapid transition is evident in the near-vertical jump in current.
However, what's particularly characteristic here is the snapback phenomenon. Immediately after triggering, the voltage across the pin actually decreases even as the current continues to rise. This is a hallmark of protection structures based on thyristors or SCR-like elements. The voltage then settles at a lower value, known as the holding voltage, around 0.9 V, which is the minimum voltage required to keep the device in this conductive state.
Beyond the holding voltage, the current increases steadily with the applied voltage, and the slope of this region indicates the dynamic resistance of the protection element in its ”on” state. Here, the dynamic resistance appears to be relatively low, suggesting that once triggered, the device can effectively shunt current away from the sensitive internal circuitry connected to this pin, limiting the voltage stress it experiences during an ESD event.
In essence, this pin is equipped with a very sensitive, fast-acting protection that triggers at a low voltage and becomes highly conductive to divert ESD current. This type of protection is likely used for very delicate I/O lines or internal nodes that cannot tolerate even small voltage overshoots. However, the low holding voltage also implies a potential susceptibility to latch-up if the current is not properly limited after the ESD event.

4.3.4 PIN11 - PIN18

The TLP signature of this pin reveals a more complex ESD protection behavior. We observe a clear trigger voltage, this time at a higher level of approximately 6 V. Below this voltage, the pin exhibits a high impedance. Upon reaching the trigger voltage, the device switches to a conductive state, again showing a characteristic snapback with a decrease in voltage as the current

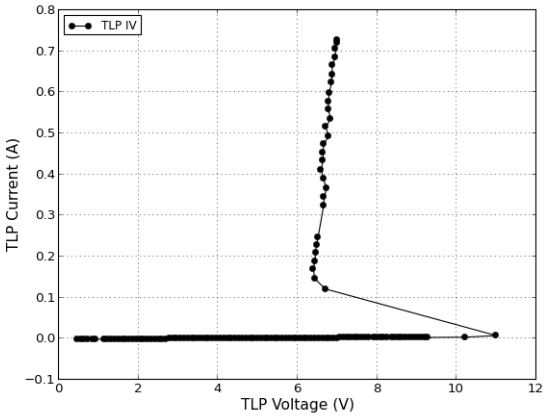


Figure 4.16: IV plot of PIN11 - PIN18

increases. The holding voltage here is also higher than in Figure 4.13, around 6.5 V.
However, the behavior at higher current and voltage levels distinguishes this pin's protection. Instead of a simple, monotonic increase in current, we see a peak in the current followed by a decrease before it starts to rise again. This non-linear response suggests a more intricate underlying protection circuit or the activation of different conduction mechanisms as the stress level increases. It could also be indicative of potential instabilities or even the onset of a secondary breakdown phenomenon that is being somewhat controlled by the protection structure.
This pin likely employs a thyristor-based protection designed for a higher voltage threshold. The complex behavior at higher stress levels warrants further investigation as it might indicate a specific design intended to handle unusual ESD scenarios or potentially a less robust response under extreme conditions compared to a more linear I-V characteristic.

4.3.5 PIN13 - PIN18

The TLP graph for this pin presents a different picture, one without the abrupt trigger and snapback seen in the previous two. Here, as the voltage increases, the current starts to rise more gradually around a turn-on voltage of approximately 3.5 V. This behavior is characteristic of a TVS diode, where the protection relies on the controlled breakdown of a PN junction.
After the initial turn-on, the current increases with the voltage, but the relationship is not strictly linear. The slope of the curve, representing the dynamic resistance, appears to decrease as the current increases. This means that the effectiveness of the voltage clamping improves (lower resistance) as the ESD stress becomes more severe. At higher voltages (above 6 V), the curve becomes more linear, indicating a more stable dynamic resistance in this operating region.
This pin is likely protected by a TVS diode designed to start clamping at a moderate voltage. The gradual turn-on and the variable dynamic resistance suggest a controlled limiting of the

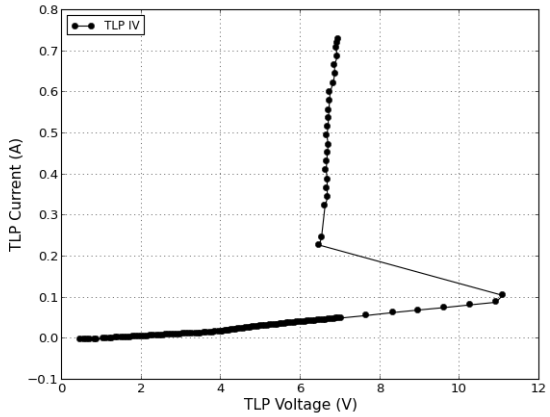


Figure 4.17: IV plot of PIN13 - PIN18

voltage, and the absence of snapback mitigates the risk of latch-up. This type of protection is often used for general-purpose I/O lines.

4.3.6 PIN29 - PIN18

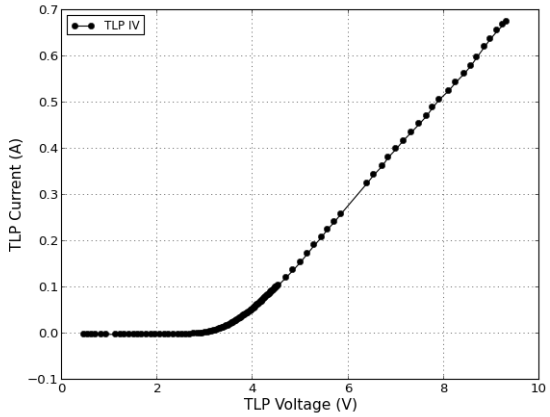


Figure 4.18: IV plot of PIN29 - PIN18

This TLP signature indicates a protection mechanism designed for high-voltage events. The current remains near zero until the voltage reaches a significantly higher turn-on threshold of around 16 V. Beyond this point, the current begins to increase, initially somewhat gradually, but then exhibits a very rapid rise for only a small increase in voltage (above 18 V). This steep slope signifies a very low dynamic resistance in the high-current regime.
There is no snapback observed, suggesting a diode-based TVS as the likely protection element. The high turn-on voltage indicates that this pin is meant to tolerate relatively high voltage levels during normal operation and only engage protection when a substantial overvoltage occurs. The

very low dynamic resistance at high currents is crucial for effectively clamping large ESD events and preventing excessive voltage stress on the connected circuitry.
This pin is likely a power supply pin or a high-voltage I/O, protected by a robust TVS diode designed to handle large ESD currents at high voltages while maintaining a stable clamped voltage.

4.3.7 PIN30 - PIN18

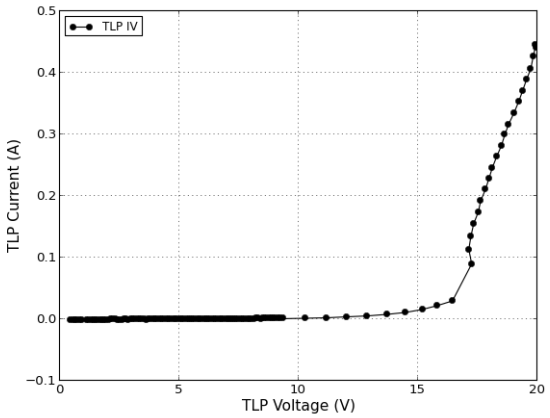


Figure 4.19: IV plot of PIN30 - PIN18

The final TLP graph shows a protection behavior with a turn-on voltage around $9V$. Once the turn-on voltage is reached, the current increases with the voltage in a relatively linear fashion, indicating a fairly constant dynamic resistance in the conductive region. There is no evidence of snapback, again suggesting a diode-based TVS as the protection mechanism.
The moderate turn-on voltage implies that this pin is designed to tolerate a certain range of voltage fluctuations before the ESD protection kicks in. The relatively linear I-V characteristic after turn-on suggests a predictable and stable voltage clamping action.
This pin likely serves an I/O function with a moderate voltage tolerance range and is protected by a TVS diode that provides reliable clamping without the risk of latch-up. The turn-on voltage is chosen to be above the normal operating levels of this specific pin.
By analyzing each graph individually, we gain a deeper understanding of the specific ESD protection strategies implemented on different pins of the same chip, highlighting the diverse approaches taken by the designers to ensure the overall robustness of the integrated circuit.

This table provides a side-by-side comparison of the key parameters extracted from each TLP graph, highlighting the distinct characteristics of the ESD protection circuitry implemented on the different pins. It allows for a clear visualization of the diverse strategies employed, ranging from highly sensitive, snapback-based protection for delicate interfaces to robust, high-voltage

Table 4.3: TLP Graph Comparison

Feature	**Figure 1.8**	**Figure 1.9**	**Figure 1.10**	**Figure 1.11**	**Figure 1.12**
Trigger Voltage V_{trig}/V_{on}	~ 0.8 V	~ 6 V	~ 3.5 V	~ 16 V	~ 9 V
Snapback	Yes	Yes	No	No	No
Holding Voltage V_h	~ 0.9 V	~ 6.5 V	N/A	N/A	N/A
Dynamic Resistance R_{dyn}	Low	Complex/Var.	Var. (Dec.)	Very Low (High V)	Rel. Const.
High V Beh.	Grad. Inc.	Peak & Dec.	Near-Lin. Inc.	Very Rapid Inc.	Lin. Inc.
Prot. Type	Thyristor	Thyristor	Diode	Diode	Diode
Latch-up Risk	Higher	Higher	Lower	Lower	Lower

clamping for power and high-stress I/O pins. The Potential Latch-Up Risk is inferred from the presence of snapback and the holding voltage levels.

Chapter 5

Conclusions

This thesis has thoroughly explored the evaluation of an adaptive driving beam (ADB) system within the scope of automotive front lighting applications. The analysis has shown how ADB systems represent a significant step towards optimizing visibility and road safety, overcoming the limitations of traditional lighting systems.

Throughout the thesis, the technological foundations on which ADB systems are based were examined, with particular reference to LEDs and DC-DC converters. The efficiency and precision offered by LEDs, together with the flexibility and control guaranteed by DC-DC converters, emerged as key factors for the realization of high-performance and reliable adaptive lighting systems. The ability to modulate the light beam in real-time, avoiding glare and maximizing road illumination, underscores the innovative potential of these technologies.

A fundamental aspect that emerged from the study is the need to ensure high robustness and reliability of electronic components, especially in a demanding environment such as the automotive one. The analysis of ESD protection strategies, presented in Chapter 4, allowed for an understanding of how different solutions are employed to safeguard the integrity of integrated circuits from electrostatic discharges. The comparison between various protection techniques (e.g., thyristor- or diode-based) and the evaluation of the latch-up risk highlighted the importance of accurate design to ensure the long-term durability and performance of the device. The selection of the most suitable protection strategy for each pin, based on its specific functionalities and its exposure to electrical stress, proved crucial for the overall reliability of the integrated circuit.

In summary, this thesis confirms that ADB systems are a mature and promising technology for the future of automotive lighting. The remaining challenges primarily concern the further optimization of control algorithms, the reduction of production costs, and standardization for wider dissemination. The results obtained in this work can serve as a basis for future research aimed at developing even more intelligent and integrated ADB systems, capable of fully exploit-

ing the potential offered by new sensor technologies and artificial intelligence for increasingly safe and efficient night driving.

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