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Design and Implementation of a Battery Management System for a Formula Student Electric Vehicle

Relatore: Prof. Matteo Meneghini

Laureanda: Felicia Protuc

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Abstract

A Battery Management System (BMS) is an integrated system responsible for monitoring battery circuits and implementing protective measures during fault conditions.

This thesis presents the design and implementation of a reliable low-voltage BMS for an electric vehicle (EV), specifically a Formula Student car. In this application, the system monitors the temperatures and voltages of 12 cells, as well as the current drawn by the entire system, powering the 48V low-voltage system of the car in compliance with the Formula SAE rules and safety requirements. In addition, the cells are passively balanced through the LTC6811 battery monitoring IC.

In the next chapters, an overview of the Formula Student rules, BMS systems and the vehicle SGe08 is presented, followed by the hardware design of the board and its prototyping and testing phases.

Sommario

Un Battery Management System (BMS) è un sistema responsabile della gestione del pacco batteria e dei relativi circuiti di protezione e dell'implementazione delle misure di sicurezza in caso di malfunzioni.

In questa tesi vengono analizzati il design e l'implementazione di un BMS per un veicolo elettrico di Formula Student. In particolare, l'applicazione sviluppata prevede il monitoraggio continuo delle temperature, delle tensioni delle 12 celle della batteria (bilanciate passivamente tramite l'integrato LTC6811) e della corrente assorbita dal sistema. Inoltre, il BMS alimenta l'intero sistema a bassa tensione a 48 V in conformità con il regolamento Formula SAE.

Nei prossimi capitoli sarà fornita una panoramica del regolamento, dei sistemi BMS e della vettura SGe-08, seguita dalla presentazione della progettazione hardware, della prototipazione e delle fasi di test della scheda.

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Abbreviations

AIR	Accumulator Isolation Relay
ATC	Analog To CAN
AMS	Accumulator Management System
ASMS	Autonomous System Master Switch
BMS	Battery Management System
BOTS	Brake Over-Travel Switch
BSPD	Brake System Plausibility Device
EBS	Emergency Brake System
ECU	Electronic Control Unit
EV	Electric Vehicle
HV	High Voltage
IMD	Insulation Monitoring Device
LV	Low Voltage
LVMS	Low Voltage Master Switch
LVS	Low Voltage System
PCU	Power Control Unit
RTD	Ready To Drive
SCS	System Crytical Signal
SDC	Shutdown Circuit
SMU	Sensoring Monitoring Unit
TS	Tractive System
TSAC	Tractive System Accumulator Container
TSAL	Tractive System Active Light
TSMP	Tractive System Measuring Point
TSMS	Tractive System Master Switch

Chapter 1

Introduction

This thesis presents the design, development, and testing of a Battery Management System (BMS) for a Formula Student Electric Vehicle.

The primary purpose of this year's BMS is to have a reliable BMS working at 48V, capable of properly balancing the cells and managing the output.

1.1 Formula Student

Formula Student (or Formula SAE) is a university competition that challenges students to think, design, and fabricate a prototype of a single seated racing car, similar to a Formula One car.

The type of vehicles that participate in the competition can be divided into three categories: combustion, including hybrid vehicles using an internal combustion engine, electric, fully powered by an electric motor, and driverless, where the electric vehicle drives itself. Recently, some events have begun to include vehicles powered by hydrogen fuel cells.

Teams must be exclusively student. In the summer, they compete in national and international competitions with peers from all over the world. They are evaluated based on different types of events that will be specified in 1.1.1.

Each vehicle must comply with a series of strict rules defined by the SAE to ensure safety for both the vehicle and the driver during competition.

1.1.1 Overview of the Evaluation Events for EV Vehicles

Every competition has seven evaluation areas, divided into Static Events and Dynamic Events, each with the respective points as per the following table.

	CV & EV	DC
Static Events:		
Business Plan Presentation	75 points	-
Cost and Manufacturing	100 points	-
Engineering Design	150 points	150 points
Dynamic Events:		
Skidpad	50 points	-
Driverless (DV) Skidpad	75 points	75 points
Acceleration	50 points	-
Driverless (DV) Acceleration	75 points	75 points
Autocross	100 points	-
Driverless (DV) Autocross	-	100 points
Endurance	250 points	-
Efficiency	75 points	-
Trackdrive	-	200 points
Overall	1000 points	600 points

Figure 1.1: Event points

1. **TECHNICAL INSPECTION**: To participate in the dynamic events, each vehicle must successfully complete all parts of the technical inspection. This ensures the safety of the car and the driver. The Emergency Brake System (EBS) Test and Autonomous System Inspection must be passed only if competing in DV dynamic events.

   The technical inspection includes the following aspects:

   - *Pre-Inspection*: the helmets, driver's equipment and tires are inspected
   - *Accumulator Inspection*: Inspection of the Battery Cart, of the charger and the boards and cells inside the accumulator
   - *Electrical Inspection*: The insulation between the Tractive System (TS) and the Low Voltage System (LVS) ground is measured. The Insulation Monitor Device is

also tested by connecting a resistor between the Tractive System Measuring Point (TSMP) and the LVS ground connection. Also, the Brake System Plausibility Device (BSPD) is tested by sending a signal that represents the current to achieve less than 5 kW whilst pressing the brake pedal.

- *Autonomous System Inspection*: The datasheets for the perception sensors, the Remote Emergency System (RES), and other documents regarding autonomous systems are checked.
- *Mechanical Inspection*
- *Rain Test*: The vehicle must be in Ready to Race conditions with the TS active, is then sprayed with water in any direction. The IMD must not trigger during and for 120 seconds after the test.
- *Brake Test*: After accelerating, the driver is required to deactivate the TS by using the shutdown button located in the cockpit, and the driver must rely solely on the mechanical brakes to slow down.
- *Tilt Test*: The vehicle is positioned on the tilt table at a 60-degree angle with the pilot inside. There should be no fluid leakage, and all wheels must stay in contact with the surface of the tilt table.
- *Vehicle Weighing*
- *EBS Test*: This procedure evaluates the brake system in autonomous driving. During the brake test, the vehicle must accelerate in autonomous mode to a minimum speed of 40 km/h within 20 meters. Once the RES is triggered, the vehicle must come to a complete and safe stop within a maximum distance of 8.5 meters.

2. **STATIC EVENTS**

- *Business Plan Presentation*: Each team presents a business model that offers a product or service based on the team's specific vehicle. The team must convince the jury, which will be potential partners, to invest in the project.

- *Cost Analysis*: Teams must evaluate the cost of all components and manufacturing processes. They must also explain their understanding of the subject, presenting, for example, trade-offs and make-or-buy decisions.
- *Engineering Design*: Teams must present every design choice made for the vehicle, highlighting design concepts and features. This method evaluates the student's engineering process and effort in designing the vehicle.

3. **DYNAMIC EVENTS**

- *Acceleration*: The track is a straight line of 75 m. The event consists of an acceleration test from a standing start.
- *Skidpad*: An eight-shaped track composed of two concentric circles. The vehicle must complete two laps around each circle.
- *Autocross*: It does not have one fixed track, but it has to present a circuit with turns, straights, and slaloms and its length must be less than 1.5 km.
- *Endurance and Efficiency*: The layout is variable, but should be 22 km long. In this race, energy consumption is also evaluated.

In Driverless mode, Acceleration, Skidpad, and Autocross are pretty similar to those in non-driverless mode. The key difference between the two is that in DV mode, the vehicle has to perform the Trackdrive instead of the Endurance event. The Trackdrive layout consists of a closed loop circuit that includes straight sections, turns, and hairpins. The circuit length is 200 to 500 meters, and the vehicle must complete ten laps.

1.2 Mandatory Rules and Requirements of the BMS

To participate in the international competition, the car must comply with the regulations [1] set by Formula SAE. Generally, the rules of Formula Student Germany are followed throughout Europe. Each event also has its own handbook [2] that outlines specific rules applicable to that competition.

As a result, every design decision must take these regulations into account. Below are some of the most important rules that influenced the design of the BMS and give a comprehension of the car's electrical system.

EV: Electric Vehicles

- TS is every part that is electrically connected to the motors and TS accumulators.
- High Current Path is defined as any path of a circuitry that, during normal operation, carries more than 1A.
- All used fuses must have an interrupt current rating that is higher than the theoretical short circuit current of the system that they protect.
- All overcurrent protection devices must be rated for the highest voltage in the systems they protect. All devices used must be rated for DC.

T 11: Electrical Components

- The maximum allowed voltage that may occur between any two electrical connections in the LVS is 60VDC or 50VACRMS.
- The LVS must be grounded to the chassis.
- An LVMS (Low Voltage Master Switch) must completely disable power to the LVS.
- Master switches must be a mechanical switch of the rotary type, with a red, removable handle. They must be direct acting, i.e. they must not act through a relay or logic.
- Each shutdown button must be a push-pull or push-rotate mechanical emergency switch where pushing the button opens the SDC.

T 11.7: Low Voltage Batteries

- LV batteries are all batteries connected to the LVS.

- LV batteries must be securely attached to the chassis and located within the rollover protection envelope.
- Any wet-cell battery located in the cockpit must be enclosed in a non-conductive, water-proof (according to IPX7 or higher, IEC 60529) and acid-resistant container.
- LV batteries must have a rigid and sturdy casing
- Battery packs based on lithium chemistry other than lithium iron phosphate (LiFePO4) and all hybrid system energy storages regardless of chemistry type:
  - Must have a fire retardant casing.
  - Must include overcurrent protection that trips at or below the maximum specified discharge current of the cells.
  - Must include overtemperature protection of at least 30% of the cells that trips when any cell leaves the allowed temperature range according to the manufacturer's datasheet, but not more than 60 Celsius degrees, for more than 1 s and disconnects the battery.
  - The protection include the voltage of all cells to trip when any cell leaves the allowed voltage range according to the manufacturer's datasheet for more than 500 ms and disconnects the battery.
  - It must be possible to display all cell voltages and measured temperatures, e.g. by connecting a laptop.

Chapter 2

Electrical Overview of the Vehicle

The SGe-08 is the electric vehicle developed by students of the University of Padua's Formula Student team, RaceUP, for the 2024/2025 season.

This thesis focuses on electric vehicles (EVs) that incorporate driverless technology.

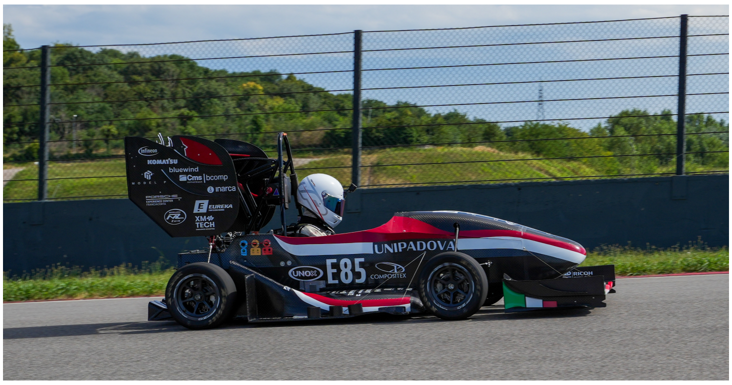

Figure 2.1: SGe-08 Electric Vehicle

2.1 Powertrain

The powertrain department manages all the high-voltage components. There have been no significant changes in this area compared to the previous season.

As a matter of fact, the high-voltage battery pack remains unchanged. It is cond in a 132s1p arrangement, delivering a nominal voltage of 564.96 V and a total energy capacity of 6.34 kWh. The pack utilizes Cosmx pouch cells. The tractive system is based on AMK inverters, which communicate with the Electrical Control Unit (ECU) through a dedicated CAN1 bus. The tractive system's maximum output is limited to under 80 kW, in accordance with the Formula Student regulations.

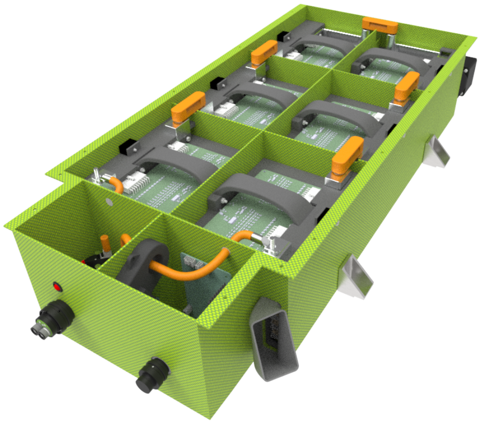

Figure 2.2: Render of the HV Battery of the SGe-08

2.2 Driverless integration

The most crucial innovation of the 2024/2025 vehicle is the integration of a driverless system.

The upgrade involved integrating an onboard computer, a LiDAR sensor, and a steering actuator, all of which required new electronic components.

Significant additions include the Autonomous System Status Indicator (ASSI), which shows the status of the autonomous system (AS); the implementation of the Remote Emergency System (RES); and the Emergency Brake System (EBS) board.

Also, the DV System has a dedicated CAN3 line to communicate with the Engine Control Unit (ECU).

2.3 Electronics

The Electronics Department manages the Low Voltage (LV) System. Compared to the previous model year, a significant change for the 2024/2025 vehicle is the transition of the entire system from 24V to 48V.

The integration of the driverless (DV) system also contributed to this transition, as it requires significantly more power. A 24V battery pack was sufficient to support manual driving for up to 23 minutes, but was inadequate for DV track driving, providing only 14 minutes of operation, which is insufficient to complete a full run. Switching to a 48V battery pack increased the time to 67 minutes of manual mode driving and 27 minutes of DV driving. These values were obtained through rough general estimates.

Battery pack	Requested power Manual [W]	Requested power DV [W]	Peak current Manual [A]	Peak current DV [A]	Duration Manual [min]	Duration DV [min]	Estimated Weight gain [Kg]
24V 6s2p	500	1200	25,9	62,3	28	14	ref.
24V 6s4p	/	/	25,9	63,3	67	27	+2,104
48V 12s2p	/	/	13,2	33,26	67	27	+1,314

Figure 2.3: LV Configuration Choice

The LV System powers all the vehicle's sensors, specifically the Sensor Monitoring Unit (SMU) board, the Inertial Measurement Unit (IMU), the Angle Position Sensor, the Brake Pedal Potentiometer, the Suspension Potentiometer, the Steering Wheel Sensor, the Temperature Sensor, and the Pressure Sensors for the front and rear brake lines. The power provided by the LV Battery is converted and distributed by the Power Control Unit (PCU).

The data sent by the boards is then processed by the vehicle's Electrical Central Unit (ECU), which acts as the "brain" of the vehicle, activating components based on the received information. The second CAN line (CAN2) is dedicated exclusively to all low-voltage sensor measurements.

2.4 Security System of the Vehicle

2.4.1 Shutdown Circuit

The Shutdown Circuit (SDC) is the vehicle's main security system. It is designed to allow all safety devices to intervene and deactivate the Tractive System (TS) during malfunctions. The SDC consists of a series connection that includes at least two master switches, three shutdown

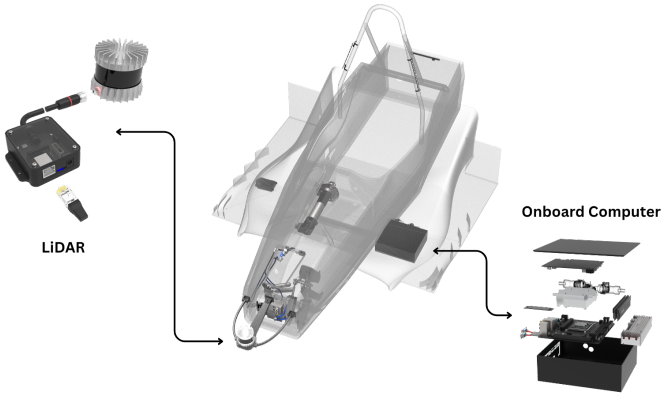

Figure 2.4: Render of the Driverless System of the SGe-08

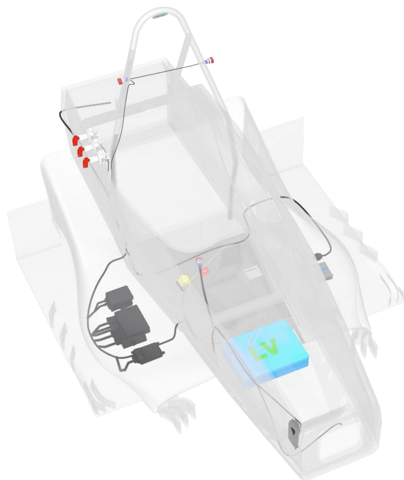

Figure 2.5: Render of the LV System of the SGe-08

buttons, the Battery Over-Travel Switch (BOTS), the IMD, an inertia switch, the BSPD, all required interlocks, and the Accumulator Management System (AMS).

If any single component in the SDC is opened, the TS must be shut down immediately by opening all Accumulator Isolation Relays (AIRs) and the pre-charge relay. The voltage in the TS must drop below 60 V DC and 50 V AC RMS within five seconds. Additionally, all current flow from the TS accumulators must stop immediately, preventing the vehicle from entering Ready To Drive mode.

All circuits that form part of the SDC must be designed to open in a de-energised or disconnected state. Each system that can open the SDC must have its own non programmable power stage to achieve this. These power stages must be capable of handling the SDC current, including the inrush currents of the AIR, ensuring that a failure does not result in electric power being fed back into the electric SDC. The following diagram illustrates the SDC for the SGe-08. It shows that the Low-Voltage (LV) Battery Pack within its Battery Management System (BMS) powers all components of the SDC.

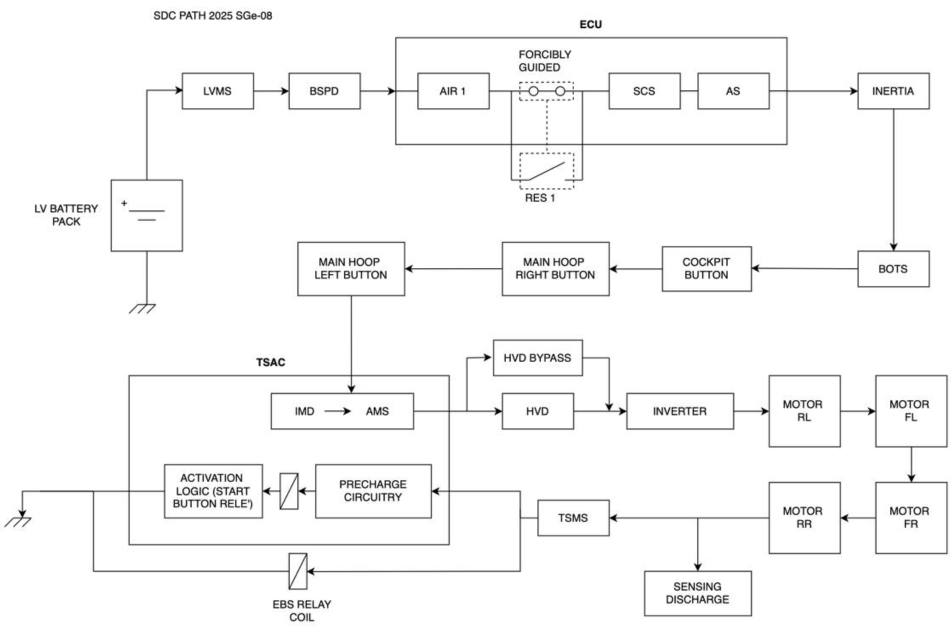

Figure 2.6: Shutdown Circuit of SGe-08

2.4.2 Tractive System Active Light

The other main security system is the Tractive System Active Light (TSAL), which indicates the state of the Tractive System (TS). Specifically:

- The TSAL must display a red light that flashes continuously at a frequency between 2 Hz and 5 Hz, with a duty cycle of 50%. This red light is active only when the Low Voltage System (LVS) is active and the voltage across any DC-link capacitor exceeds the lesser of either 60VDC or half the nominal TS voltage.

- The TSAL must have a green light, continuously on, active only if the LVS is active All AIRs are opened, The pre-charge relay is opened and the voltage at the vehicle side of the

AIRs inside the TSAC does not exceed 60 V DC or 50 V AC RMS.

Chapter 3

LV battery and BMS functions

3.1 Overview of Battery technologies

Electric and Hybrid vehicles have a high voltage and sometimes also a low voltage pack that consists of individual modules and cells organized in series and parallel. In those, chemical energy is converted into electrical energy and then used as a source of power.

There are many different types of rechargeable batteries, each with different properties. These characteristics make each battery more or less suitable for specific applications such as electric vehicles, portable electronics, renewable energy storage and others.

3.1.1 Technical Specification of a Battery

Looking at the battery technical specification sheets, it is possible to see many parameters used to describe the battery cells. An overview of the main ones is presented below.

- **Nominal voltage**: the average voltage the cell outputs when fully charged.
- **Cut-off voltage**: the minimum allowable voltage to ensure the safety state of the battery.
- **Nominal capacity**: the amount of charge in Amp-hours delivered by a fully charged battery.

- **Nominal energy**: the amount of energy in Watt-hours that the battery can store. It is calculated as nominal voltage multiplied by nominal capacity.

- **Maximum continuous discharge current**: the maximum amount of electrical current that a battery can continuously deliver over a given period of time without damage.

- **Energy density**: the nominal battery energy per unit volume. It is determined by the battery's chemical composition and how it is packaged.

- **Power density**: the maximum available power per unit volume. It is determined by the battery's chemical composition and how it is packaged.

- **Cycle life**: the number of complete charge and discharge cycles a battery can undergo.

3.1.2 Battery Condition

- **SOC - State of Charge**: It is defined as the ratio of the remaining charge in the battery to the maximum charge that the battery can deliver. It is represented as 100% when the battery is fully charged and 0% when the battery is fully discharged. This parameter is used to determine changes in battery capacity over time.

$$\mathrm{SoC}(t) = \frac{Q_{\mathrm{remaining}}(t)}{Q_{\mathrm{max}}} \times 100\% \tag{3.1}$$

  where:

  - $Q_{\mathrm{remaining}}(t)$ = remaining charge of the battery at time t
  - Q_{max} = maximum charge the battery can deliver

- **SoH - State of Health**: It describes the difference between a fresh battery and an old cell. It is defined as the ratio of the maximum battery charge to its rated capacity. The lower the SoH, the faster the battery is discharged.

$$\mathrm{SoH} = \frac{C_{\mathrm{actual}}}{C_{\mathrm{rated}}} \times 100\% \tag{3.2}$$

where:

- C_{actual} = current capacity of the battery
- C_{rated} = rated (nominal) capacity of a new battery

- **DOD - Depth of Discharge**: It represents how much of the battery's total capacity has been used, expressed as a percentage, with a discharge of 80% or more considered a deep discharge. Note that: DoD = 100% - SoC

3.1.3 LV Battery of the SGe-08

LV configuration

The battery pack is configured in a 12s2p arrangement to achieve a nominal voltage of 48V for the reasons explained in 2.3.

Cells type

The LV battery uses Li-Polymer pouch rechargeable cells. The main alternative considered was LiFePO4 (Lithium Iron Phosphate).

The differences between the two chemistries are that LiFePO4 offers a higher cycle life (over 2000 cycles) and excellent thermal stability, while LiPo cells are lighter and provide higher energy density, a higher nominal voltage, but a shorter cycle life (up to 500 cycles).

While LiFePO4 offers longer cycle life, the slightly shorter lifespan of Li-ion pouch cells is acceptable given the performance priorities of the vehicle.

Specifics of the cells

In the following tab, you will find the specifics of the cells used in the LV Battery of the Electric Vehicle SGe-08.

Name of the Cell	Melasta SLPBA843126
Nominal Voltage	3.7 V
Maximum Voltage	4.2 V
Cutoff Voltage	3 V
Nominal Capacity	6350 mAh
Maximum Continuous Discharge Current	95.25 A
Weight	131 g

Table 3.1: Specifics of the Cell

Figure 3.1: Melasta Cells

3.1.4 Case

As per T 11.7, if the battery packs used is based on lithium chemistry other than LiFePO4, they must have a fire retardant casing. Thus, the case of the LV Battery is made out of Kevlar. It is a synthetic fiber resistant to corrosion and heat, extremely strong and lightweight.

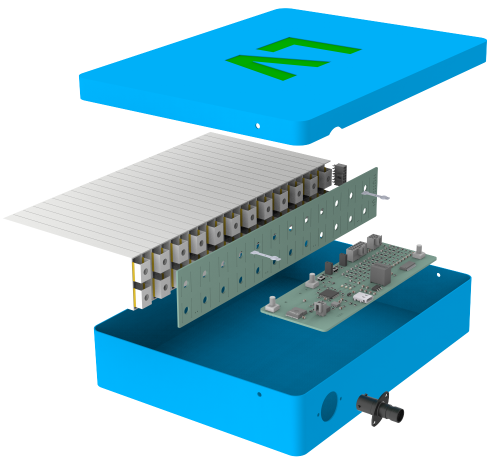

Figure 3.2: Render of the LV's Battery Case with LV components

3.2 BMS Functions & requirements

A BMS is an electronic and software-based control system designed to monitor and regulate rechargeable batteries, whether as single units or multiple modules, in an energy storage system.

Its primary purpose is to maintain the battery within safe operating limits, maximizing performance and lifespan, while protecting against conditions that could cause degradation or safety risks.

The fundamental functions that a generic BMS is required to provide include data acquisition, data communication, cell balancing, and safety management.

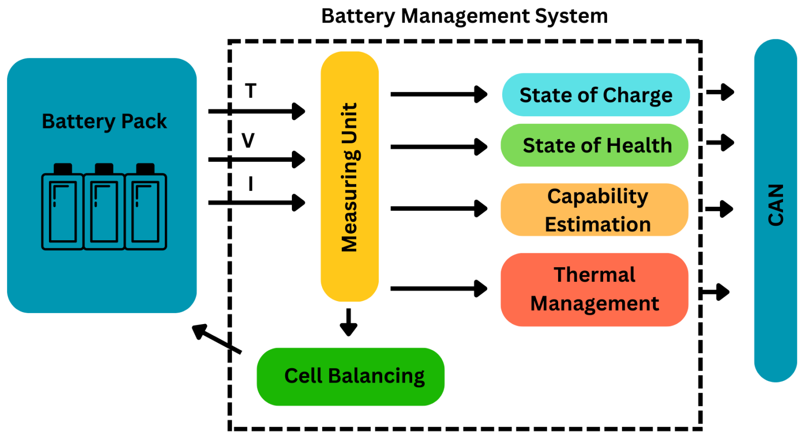

Figure 3.3: Function of a generic BMS

3.2.1 Data acquisition, monitoring, and processing

The primary function of the BMS is to measure, monitor, and process key battery parameters, including cell voltage, current, and temperature. Real-time monitoring of these parameters is essential to ensure safe operation and to maintain battery performance and longevity.

- **Voltage monitoring**

  Voltage monitoring ensures that each cell remains within defined safety thresholds. This process enables detection of overvoltage and undervoltage conditions, both of which can reduce battery life.

In this application, as required by T 11.7, the voltage of every cell is measured, providing precise control over battery health. If any cells leave the allowed voltage range defined by the manufacturer's datasheet for more than 500ms, the BMS disconnects the battery from the vehicle system.

- **Current monitoring**

  Current sensing is essential for detecting short circuits and overcurrent events, thereby protecting both charging and discharging processes.

  The overcurrent protection trips at or below the maximum specified discharge current of the cells. In this application, current is measured using an LEM sensor on the BMS board.

- **Temperature monitoring**

  Temperature is a critical factor for batteries, influencing lifespan, safety, and efficiency. Indeed, extreme temperatures, whether overheating or freezing, can create hazardous conditions.

  According to T 11.7, a minimum of 30% of the cells should be continuously monitored in terms of temperatures. In this application, 4 cell pairs out of 12 are monitored. When the temperature exceeds the allowed range established by the manufacturing datasheet, or remains above 60 Celsius degrees for more than 1 second, the BMS disconnects the battery.

3.2.2 State Estimation

Data acquisition enables the management of all parameters and the estimation of SOC, SOH, and DOD, which are essential to maintain battery health and to extend battery's life. In HV traction packs, these estimates are vital for energy management, predicting the remaining range, and ensuring safety.

In this application, at the moment, there is no state estimation, however it would be an interesting further development.

3.2.3 Data communication

After data acquisition and processing, the information must be exchanged with other vehicle systems, such as the electronic control unit (ECU).

In this application, communication occurs via the Controller Area Network (CAN) or other protocols such as Serial Peripheral Interface (SPI). Effective data communication enables real-time telemetry and continuous battery health monitoring, which are necessary for optimal performance and reliability.

3.2.4 Cell balancing

Battery cells connected in series, even if initially identical, frequently develop imbalances over time. This issue accelerates cell degradation and reduces overall battery longevity. Without effective balancing, disparities among series connected cells increase, resulting in a reduced total capacity. Effective cell balancing reduces the risk of damage and extends the battery's cycle life.

Imbalances primarily result from manufacturing imperfections. In lithium batteries, small variations in electrode geometry or assembly lead to performance differences among cells. Additional contributing factors include temperature gradients due to uneven heat distribution, differences in cell aging, and internal defects that accelerate degradation.

There are two types of balancing [3]:

- **Passive Balancing**

  Passive balancing discharges higher voltage cells using resistors, converting excess energy into heat. This method is less efficient but is simpler and more cost-effective to implement.

- **Active Balancing**

  Active balancing redistributes charge among cells during charging and discharging cycles without significant energy loss. This approach is more complex and costly than passive balancing but offers greater efficiency and speed.

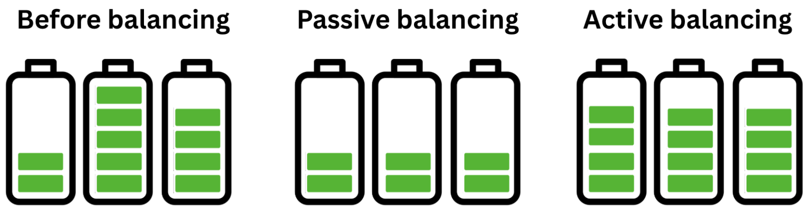

Figure 3.4: Balancing of the cells

The selection of a balancing strategy depends on the specific application. In this case, passive balancing was chosen for its cost effectiveness, minimal spatial requirements, and the lack of a requirement for rapid balancing.

3.2.5 Safety Management

According to the rules, if any problem arises, the BMS should disarm the entire system within one second to ensure the safety of the vehicle and its pilots.

This requirement is critical because a single malfunction can create significant safety risks. For example, overcharging may cause cell venting, releasing flammable gases, and creating a severe hazard.

3.3 Environmental Impact of a BMS

It is essential to recognize the benefits that a BMS offers. A BMS, indeed, contributes not only to the same and reliable operation of electrochemical storage by also to significant environmental and sustainability benefits. Obviously, it yields also practical and economical benefits since it extends the lifetime of the battery pack. In this way, fewer batteries need to be produced and replace over the system's lifetime reducing overall system cost.

The following points outline specific environmental and sustainability advantages associated with the implementation of a battery management system (BMS).

- **Reduction in CO_2 emissions:** A reduction in CO2 emissions by a rate of 40% is possible when a battery is controlled by BMS to store off-peak clean electricity to serve peak demand [4]. Optimized charge and discharge cycles decrease reliance on fossil-fuel peaking plants, lowering emissions and air pollution

- **Greenhouse gas (GHG) benefits:** The greenhouse gas (GHG) benefits of batteries could be doubled using BMS and better use of clean off-peak electricity.
- **Metal depletion impacts:** BMS can be efficient in controlling charging and discharging cycles, as well as the operation frequency. It impacts the materials that have high environmental and energy impacts. This process extends battery life, decreases replacement frequency, and lowers demand for critical materials such as lithium, cobalt, and nickel.
- **Temperature control impacts:**

  Two types of temperatures, electrochemical reaction temperature and battery environment temperature, can be controlled in the battery pack by BMS. Thermal management increases energy efficiency and minimizes the environmental impact of thermal stress, as well as the shortened battery lifespan.
- **Extended lifetime and sustainability impacts:** In addition to environmental benefits, a BMS offers practical and economic advantages by extending battery life. This results in fewer batteries being manufactured and replaced, lowering operational costs and reducing the environmental impact associated with production, transport, and disposal.

Chapter 4

Battery Management System design

The board's schematic, layout, and software were designed in accordance with standard industry practices and guidelines to ensure reliability and cost-effectiveness.

Development was conducted to comply with Formula SAE regulations while preserving flexibility for future modifications and debugging. Jumpers, test points, and configurable components were incorporated to facilitate troubleshooting and iterative improvements. This design strategy enabled efficient testing, experimentation, and optimization throughout the development process.

4.1 LTC6811-2

4.1.1 Features and Functions

The main component of the BMS is the integrated circuit LTC6811.

This IC has multiple purposes. It consistently monitors the cells' voltage and temperature, enabling the BMS to intervene promptly. It also balances the cells when necessary, ensuring system stability and longevity.

It's a *12 Channel Multicell Battery Monitor* with an Addressable Interface. It is also used in commercial hybrid and EV cars. This is because it is certified AEC-Q100 and ISO 26262. These are important automotive certifications for electronics. The ISO 26262 standard addresses functional safety, while the AEC-Q100 is a stress test qualification standard for integrated circuits. It defines which ICs are considered automotive qualified. Because the LTC6811 complies with both regulations, it provides both safety and reliability. This was also taken into consideration when selecting the component.

The LTC6811 also offers useful features compared to competitors, such as:

- It achieves a total measurement error (TME) of less than 1.2 mV, whereas many competitors have a typical error range of 2-3 mV. This lower error results in improved accuracy in cell voltage measurement.
- Daisy Chain configuration and isoSPI are available; although they are not required for this particular application, their presence, combined with the fact that the IC is also used in the HV Battery, where these functions are utilized, justifies the decision to use the same model for consistency across the system.
- 290 μs to measure all cells in a system
- 16-bit ADC with programmable noise filter
- GPIOs for temperature sensing
- configurable as both I2C and SPI master
- onboard 5V regulator: useful to reduce the components on board
- ultra-low sleep mode current for long-term battery storage: 4 μA
- passive cell balancing: reducing the onboard components since MOSFETs are internal

In this application, the LTC6811-2 is used to monitor the entire battery pack and acts as a slave to the STM32, which serves as the microcontroller that acts as the BMS's "brain". The two communicate with each other via SPI, while the SMT32 exchanges information with other vehicle system boards via CAN.

To better understand the hardware setup, the following details highlight the pinout and how the LTC6811 interfaces with other components.

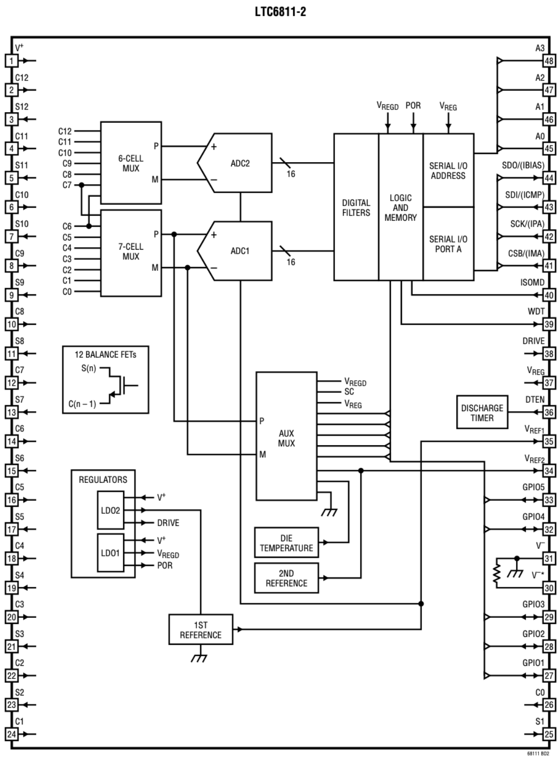

Figure 4.1: LTC6811-2 Block Diagram

4.1.2 Pinout:

- **C0 TO C12**: the cell inputs.
- **S1 TO S12**: the 12 internal N MOSFETs.
- **VREF2**: must be bypassed with an external 1uF capacitor. It's used as a voltage reference for the NTC 10k thermistors. It must have a voltage of around 3V to ensure it's working properly.
- **VREF1**: is the ADC Reference Voltage, which must be bypassed with a 1uF capacitor. It cannot have loads and should normally be around 3V.
- **DTEN**: Discharge Timer Enable. To enable it, it must be connected to VREG. It's used to keep the discharge switches turned ON for a programmable time duration. If it's used, the discharge switches are not turned OFF when the watchdog timer is activated. In this case, a jumper is used to select the preferred configuration at the moment via hardware.

- **DRIVE**: If an NPN is connected to this pin, it's possible to power the IC. On this board is left unconnected.
- **VREG**: 5V Regulator Input, should be bypassed with an external 1uF capacitor.
- **ISOMD**: Serial Interface Mode. In this case, it is connected to GND (V-) to configure the LTC6811 for 4-wire SPI mode. If isoSPI is wanted, it should be connected to V+.
- **WDT**: Watchdog Timer Output Pin. It is connected to VREG via a 1M resistor. If the LTC6811 does not receive a valid command within 2 seconds, the watchdog timer circuit will reset the LTC6811, and the WDT pin will go to high impedance. It can also be left unconnected.
- **CSB, SCK, SDI, SDO**: 4-pin for the SPI communication with the STM32. SDO (MISO) should be connected with a 5k pull-up resistor.
- **A0 to A3**: address pins. Connected to ground V- since it's the only device that communicates in the SPI line with the STM32. It could be connected to V+ if there were multiple ICs.

4.1.3 Voltage Acquisition

As previously said, the LTC6811 provides up to 12 cell voltage measurement inputs. The inputs are high impedance, thus there is no need for additional buffer circuitry.

ADC

The ADCs have a range from -0.2V to 5.73V.

For voltage acquisition, delta-sigma ADCs are used. This is the most common and preferred choice in EV and EES applications. A delta-sigma ADC samples the input signal at a rate much higher than the Nyquist rate. This spreads quantization noise across a wider bandwidth. Its modulator also pushes quantization noise into higher frequencies. This improves resolution inside the bandwidth and causes noise above the signal bandwidth to increase. The digital filter

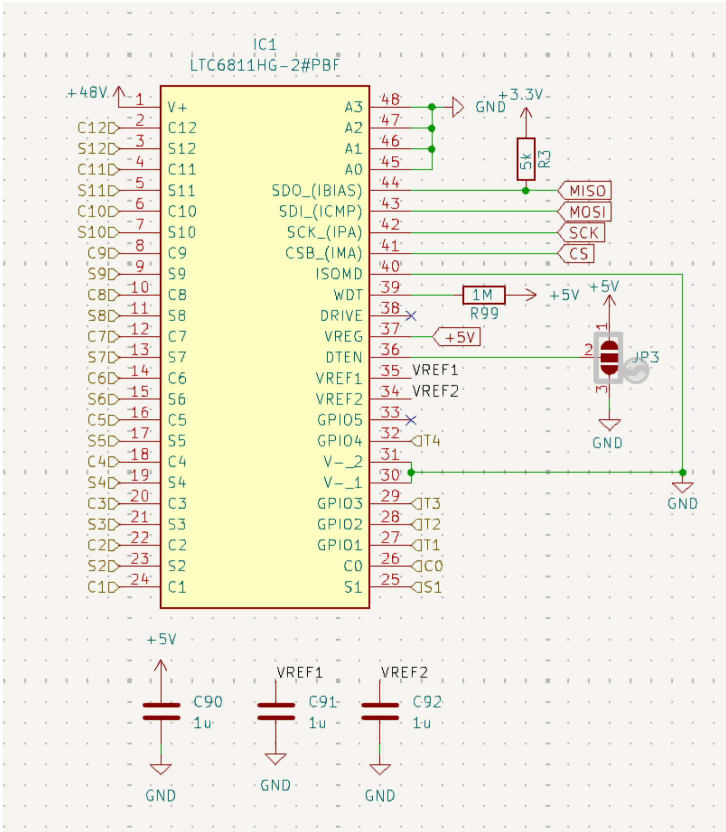

Figure 4.2: LTC6811 Schematic and connections

then removes the out of band noise and downsamples the signal. As a result, these ADCs are robust against DC/DC converters. Other solutions, such as the SAR ADC, may alias switching noise into the measurement band.

It offers up to 16-bit resolution, strong common mode rejection, and is configurable in multiple modes, to be discussed later.

4.1.4 Temperature Acquisition

Temperature is measured with 103 JT-025 thermistors: ultra-thin (500 μm), well-insulated, 10kΩ $\pm$1% at 25°C. Being NTC, resistance drops as temperature rises.

The thermistor is in a voltage divider with a 22kΩ resistor powered by 5V reference from LTC6811 VREF2. Data goes through four GPIO pins to the STM32.

The value of 22kOhm was chosen to maximize the temperature reading within the common range of 20 to 60 degrees, which is typical for the cells [5].

Figure 4.3: 103 JT-025 Thermistor

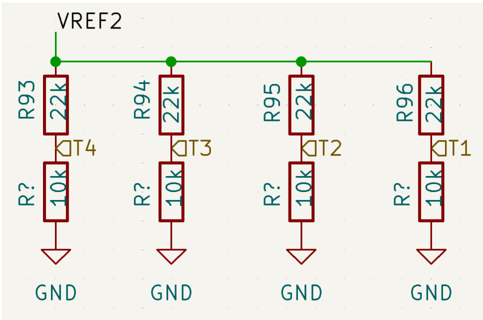

Figure 4.4: Thermistors connection schematic

4.1.5 Balancing:

One of the main functions and features of the LTC6811 is the balancing of the cells .

As described in Chapter 3, passive cell balancing is implemented on this board. When a cell becomes overcharged and the BMS enters balancing mode, an S output discharges the cell through an external resistor. This S output is connected to an internal N-channel MOSFET with a maximum on-resistance of 25 Ω, and the external resistor is placed in series with the MOSFET. In this way most of the heat is dissipated outside the IC, which enhances safety and prevents overheating of the chip.

The circuit configuration is identical for each cell. From the cell terminal, a ferrite bead suppresses high-frequency noise and is placed in series with a fuse. Following that, a discharge resistor is connected in parallel with the MOSFET, along with an LED that indicates when the cell is balancing. Additionally, an anti-aliasing filter is installed on the input to the LTC6811 to improve measurement accuracy.

Discharge Resistor

The target balancing current was set to slightly less than 50 mA, just below the datasheet [6] maximum of 60 mA. This value ensures a reasonable discharge time while minimizing heat generation. If the LTC6811 die temperature exceeds 150°C, the thermal shutdown feature is triggered, turning off all discharge switches, resetting the Configuration Register Group.

To further reduce component stress and improve thermal performance, a 100 Ω resistor was chosen. Indeed, based on the design target of 50 mA, the ideal resistor would be $R = V/I = 3.7\,\mathrm{V}/50\,\mathrm{mA} \approx 74\,\Omega$. For practical and economical reasons, a standard 100 Ω resistor was used instead, which results in a balancing current of 37 mA and a power dissipation of 0.137 W, slightly lower than the 0.185 W at 50 mA. This choice reduces heat generation, minimizes component stress, and increases the thermal margin, which is especially important when multiple cells are balanced simultaneously.

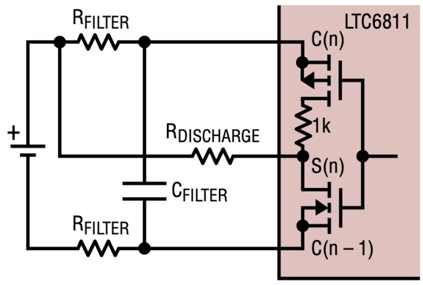

Figure 4.5: Internal Balancing Circuit

Balancing Time Estimation

It should be noted that the balancing time increases as the balancing current decreases. The balancing time can be estimated as:

$$t_{\text{balancing}} = \frac{\Delta Q}{I_{\text{balancing}}}$$

Since $Q = C \cdot \Delta V$, we have:

$$t_{\text{balancing}} = \frac{C \cdot \Delta V}{I_{\text{balancing}}} \quad \text{[hours]}$$

where, in this case, $C = 6.35\,\text{Ah}$.

For comparison, the estimated balancing times at 37 mA (chosen) and 50 mA are:

ΔV	$t_{37\text{ mA}}$	$t_{50\text{ mA}}$
0.01 V	1h 43min	1h 16min
0.05 V	8h 35min	6h 21min
0.10 V	17h 10min	12h 42min
0.20 V	34h 19min	25h 24min

However, since the voltage differential (ΔV) is typically less than 0.05 V and there are no strict timing requirements, a 37 mA current is acceptable.

Anti-Aliasing Filter

To improve signal quality, an anti-aliasing filter is implemented using an RC circuit with:

$$R = 10\,\Omega, \quad C = 10\,\text{nF}$$

The cutoff frequency is:

$$f_c = \frac{1}{2\pi RC} = 1.59\,\text{MHz}$$

This is set above the effective bandwidth of the ADC, thereby eliminating high-frequency noise from DC-DC converters or gate drivers, and suppressing components that could alias into the signal band. This approach helps maintain ADC accuracy and precision.

In the schematic, a switch is also presented, which is useful for disabling the board without physically disconnecting it from the battery. The two connectors are Molex Nanofit.

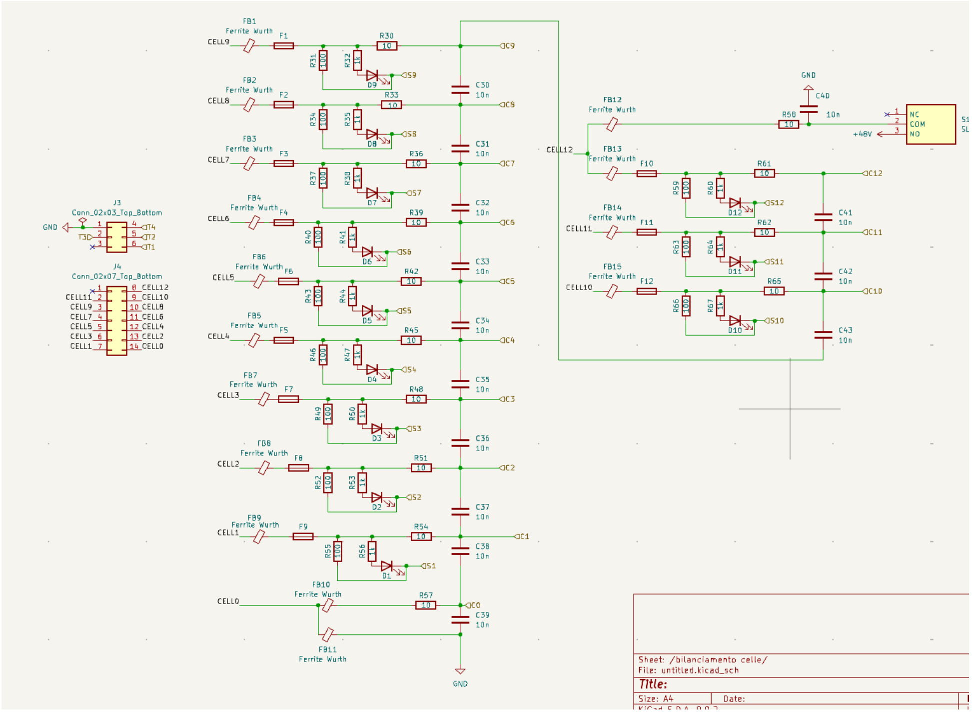

Figure 4.6: Balancing Schematic

4.2 STM32 and Schematic

4.2.1 STM32

The STM32F405RG microcontroller was selected as the main processor of the BMS. It offers strong computational performance, memory resources, and peripheral integration, which are essential for reliable cell monitoring, balancing, and fault detection.

This microcontroller was chosen because, when compared directly to other competitors in the same price range, such as the Renesas RA4M3, it offers distinct advantages in ecosystem support, performance, and tool availability. These comparative advantages are detailed as follows:

- **Ecosystem and Development Familiarity**: The STM32 platform is used across multiple vehicle boards, supporting standardized maintenance. Its large developer community provides robust technical support. Additionally, HAL and CubeMX tools enable faster prototyping and debugging than the Renesas platform.

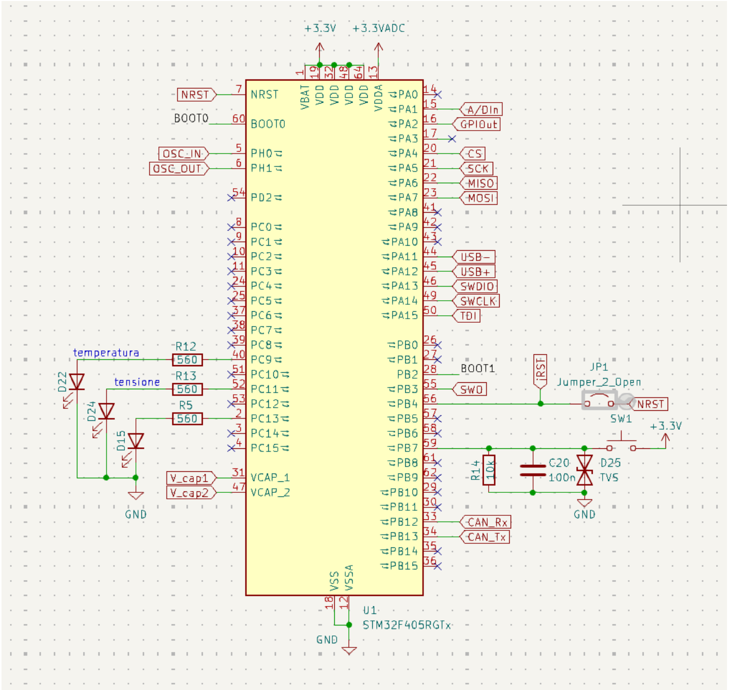

Figure 4.7: STM32F405 pinout

- **Performance and Resources** :
  - Cortex-M4 core operating at up to 168 MHz and includes single-precision FPU and DSP capabilities. In contrast, the RA4M3 supports operation up to 100 MHz.
  - Powering voltage from 1,8 to 3,6 V.
  - 1 MB of embedded Flash memory and 192 KB of SRAM, enabling the implementation of advanced diagnostic routines and data logging functionalities.
  - Two integrated 12-bit digital-to-analog converters (DACs) that generate analog signals for calibration and system diagnostics.
  - Three I2C, four UART, two CAN, three SPI, and SDIO ports enable high-speed, reliable data exchange between the BMS, cell monitoring ICs, the vehicle CAN bus, and diagnostic equipment. This ensures flexible integration within the EV architecture.
  - Support for advanced low-power operating modes enables the BMS to minimize energy consumption during standby or fault conditions, enhancing vehicle efficiency

and safety.

- Advanced USB connectivity, enabling efficient firmware updates, diagnostics, and direct interfacing with external programming/debugging tools.
- Integrated JTAG and Serial Wire Debug (SWD) interfaces enable non-intrusive real-time debugging and in-system programming. They are crucial for rapid development cycles and robust fault analysis in automotive environments.

- **Programming language** support also influenced the selection of the microcontroller. A key requirement from the software engineering team was compatibility with the Rust programming language, which is increasingly adopted in safety-critical embedded systems for its focus on memory safety and concurrency. The STM32 ecosystem benefits from a Rust developer community and mature toolchains, while Renesas platforms have limited Rust support and resources.

4.2.2 STM32 pinout and schematic description

- **NRST**: Is the *reset* of the microcontroller. A CMOS driven pin that requires a defined logic level to ensure reliable device operation. To avoid metastability or unintended resets, it is permanently pulled up to VDD through a resistor. Without this biasing, the pin would remain floating, potentially causing spurious resets due to noise coupling or leakage currents. When the button is pressed, the microcontroller connects NRST to GND, triggering a reset. The capacitor is there to ensure a clean reset pulse, filtering glitches, while the TVS diode protects against ESD spikes or surges, clamping any voltage above 5-6 V to protect the input.

- **Capacitors C6–C13**: *Decoupling capacitors* are strategically placed adjacent to each VDD supply pin to counteract transient voltage dips and high-frequency noise generated during rapid internal logic switching events. These capacitors, typically rated at 100 nF, act as local charge reservoirs, ensuring a stable supply voltage and minimizing electromagnetic interference (EMI). Proper placement and sizing of decoupling capacitors are

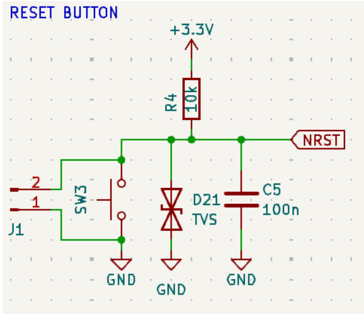

Figure 4.8: Reset schematic

critical for maintaining microcontroller reliability.

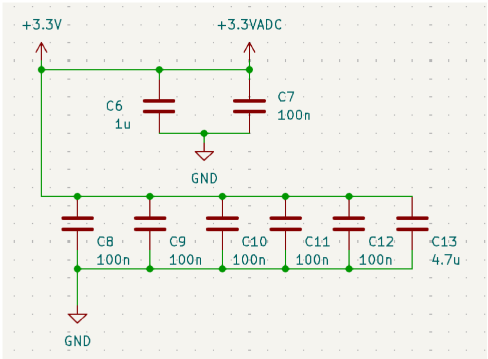

Figure 4.9: Decoupling capacitor schematic

- **VCAP**: According to the STM32F405 datasheet [3], the VCAP pins require two external 2.2 μF capacitors to stabilize the integrated low-dropout (LDO) voltage regulator, which is crucial for maintaining core voltage integrity and rejecting noise. If the internal regulator is not used, bypass these pins with 100 nF decoupling capacitors to maintain signal integrity and prevent spurious oscillations.

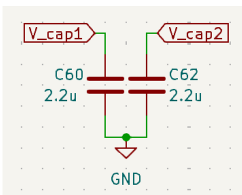

Figure 4.10: VCAP schematic

- **Oscillator (PH1, PH2)**: While the STM32F405 integrates a 16 MHz internal High-Speed Internal (HSI) oscillator with a ±1% frequency tolerance, this level of precision is inadequate for time-critical interfaces such as USB and CAN. Thus, an external *high-speed crystal oscillator* (HSE) was selected to ensure reliable synchronization and frequency stability, in accordance with USB and CAN protocol requirements.

The oscillator circuit incorporates two 10 pF capacitors, forming a parallel-resonant LC network that defines the oscillation frequency and minimizes phase noise. This configuration enhances both signal integrity and system robustness, as recommended in IEC 60747 guidelines and the STM32 application notes.

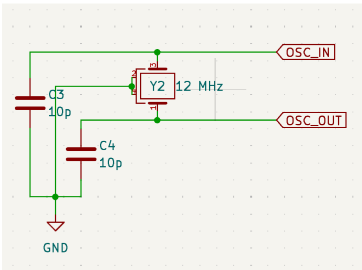

Figure 4.11: Oscillators schematic

- **Boot Configuration**: The STM32F405 features two boot configuration pins *(BOOT0 and BOOT1)*, which determine the microcontroller's boot source after a reset. The BOOT0 circuit is similar to the NRST configuration but is typically pulled down to ground, with a TVS diode and capacitor for ESD protection and glitch filtering.

  BOOT1 is hardware-selectable via a jumper, allowing flexible boot mode selection. Depending on the logic levels at startup, the device can boot from main flash memory (application code) or system memory (embedded bootloader), supporting both normal operation and firmware programming.

- **PA1 and PA2**: Each of these pins supports multiple functions, such as USART (Universal Synchronous/Asynchronous Receiver/Transmitter), UART (Universal Asynchronous Receiver/Transmitter), TIM (Timer), ADC (Analog-to-Digital Converter), and general I/O. In this application, PA1 and PA2 are configured as *I/O* and *ADC* channels for the *output delivery* .

- **PA4 to PA7**: These pins are configured for *SPI* (Serial Peripheral Interface) commu-

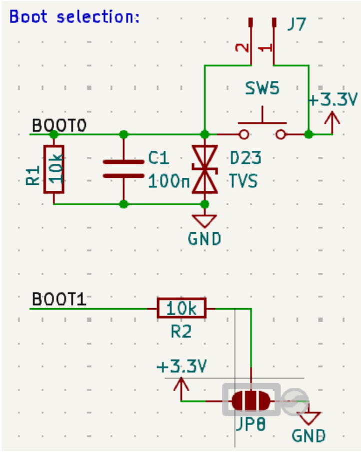

Figure 4.12: Boot selection schematic

nication. The microcontroller interfaces with LTC6811 using the SPI protocol. Proper routing of SPI signals is crucial to ensure the correct operation of the device. Additional implementation details are discussed in the software section.

- **PA11 and PA12**: These pins function as *USB+* and *USB–* data lines. A vertical USB-C port is used for board programming due to spatical constraints. The USB-C interface includes power filtering, ESD protection, and optimized data line routing.

  The VBUS line supplies USB bus power from the connector, with a TVS diode providing overvoltage protection during connection or disconnection. An ESD array protects against electrostatic discharge, and the diode ensures reverse voltage protection, which is critical due to the USB connection to external devices. A bulk capacitor stabilizes the VBUS voltage.

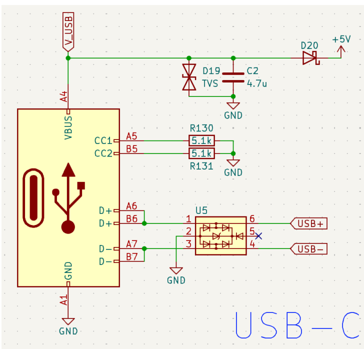

Figure 4.13: USB-C schematic and connections

- **SWDIO, SWCLK, TDI, SWO, and jRST**: These are all pins needed for *JTAG*, which will be discussed later.

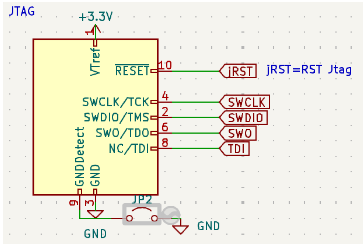

Figure 4.14: JTAG schematic and connections

- **PB7**: Standard switch button used to activate *balancing mode*.

- **PC9 and PC11**: These pins control LEDs that illuminate when a *temperature* or *voltage fault* is detected. This configuration facilitates testing and fault identification during system operation.

- **PC13**: This pin is assigned to an LED that is used for *debugging* purposes during board development and testing.

- **PB12, PB13**: *CAN communication*

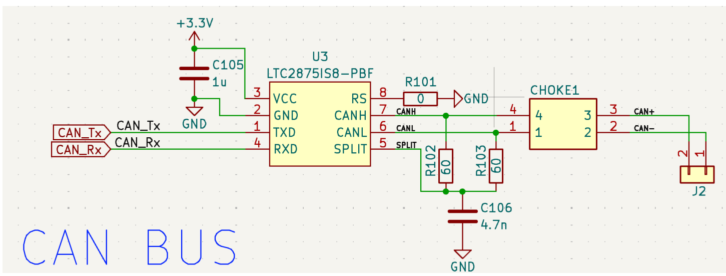

Figure 4.15: CAN communication module

The CAN bus communication module is built around the LTC2875 CAN transceiver [7]. This device features high ESD protection (±25kV on interface pins and ±8kV on all other pins), high noise immunity, and low electromagnetic emission, and is designed to withstand the demanding environments of automotive and industrial applications.

It translates the signals from the microcontroller (*CanTx* and *CanRx*), which are logic-level transmit and receive lines, into *CANH* and *CANL*, which are differential signals required by the CAN bus.

To ensure stable operation, decoupling capacitors are placed close to the transceiver to stabilize its supply voltage.

The operating mode of the transceiver is determined by the RS pin. In this design, the RS pin is tied to GND through a 0 Ω resistor, setting the transceiver in active high-speed mode. Alternatively, if the resistor has a different value, it can be used to control the slew rate, as the output edges are shaped according to the current sourced from the RS pin when it is pulled below 1.1V. This feature can help limit electromagnetic emission while reducing speed.

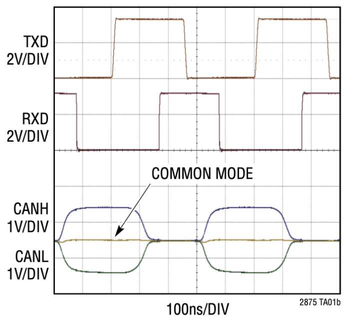

Figure 4.16: LTC2875 Transmitting at 4Mbps from a 3.3V Supply

This allows for a trade-off between EMI performance and speed; in this design, speed is prioritized, while still allowing future modifications.

For reliable communication, the CAN bus must be terminated to match the characteristic impedance of the transmission line. This value is typically 120 Ω . In this circuit, this differential termination is implemented using a split termination network. Two 60 Ω resistors are placed between CANH and CANL. Their midpoint connects to the transceiver's SPLIT pin and is stabilized with a capacitor to ground.

After translation, the signal passes through a common-mode choke. This helps block high-frequency EMI from propagating either into or out of the board while leaving the differential channel signals unaffected.

In summary, this design provides a robust CAN interface that ensures stable communication and signal integrity while minimizing noise and EMI. These features make the module a suitable foundation for automotive and industrial applications where reliable performance is essential.

4.3 Current Sensing

To provide continuous monitoring of current in the circuit, the BMS uses a LEM HOB 50-P/SP33 Hall effect current transducer. This component was selected for several reasons. First, it operates from a single 3.3V supply. Its output is compatible with the system's measurement requirements. The measurement range of $\pm$ 125 A covers the expected operating current of 0-50A. The sensor has a response time of less than 200 ns. This is crucial for the initial transient that occurs when the load is attached to the battery. The raw analog output values of the transducer are acquired by the STM32 through the microcontroller's Analog-to-Digital input. The electrical connections are implemented according to the device's datasheet. [8]

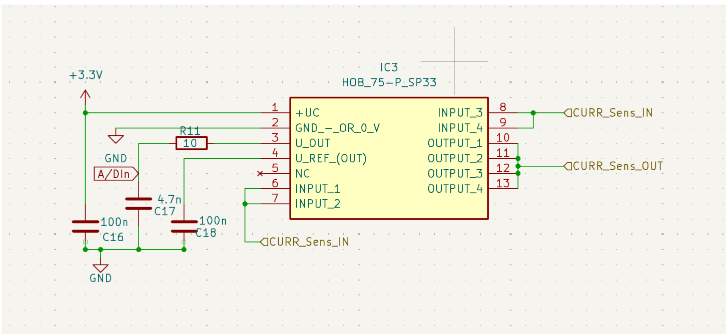

Figure 4.17: Current LEM sensor schematic

4.4 Output delivering

Once the STM32, in accordance with the LTC6811, has confirmed that the battery is operating within a safe range, the BMS enables the output power to supply all the low-voltage systems of the vehicle.

The adopted configuration is a high-side switch based on the 1EDL8011 gate driver and N-channel MOSFETs.

4.4.1 Gate Driver

The 1EDL8011 was selected among the alternatives for the following features [9]:

- Operation up to 80V (supply and source voltage)
- An internal charge pump for reduced EMI and to ensure proper operation at low supply voltages. The charge pump is a circuit that utilizes capacitors as energy storage elements to generate a gate voltage higher than the supply voltage, eliminating the need for an additional high-voltage supply. This is the main reason that led to the choice.
- Blanking time is used to prevent the inrush current from triggering an OCP event. However, in this specific application, it is unused since the inrush current occurs each time a new load is connected. In the vehicle, however, the BMS output remains permanently enabled, and the inrush current occurs when the external switch connects the LV battery to the entire system.

PINOUT and schematic description:

The connections are made according to the example in the datasheet:

- IN pin: receives the enable signal from the STM32.
- I_{limit}: not useful since it could read the inrush current as a fault and shut down the system. The current is instead monitored via the LEM sensor, and eventually, the STM32 will disable the gate driver, thereby disabling the output.
- C_{fpn}, R_{ser}: external components required for the charge pump to work properly, to reduce stress on the internal device and prevent potential damage by the inrush current. In this case, the highest capacitor, thus the lowest turn-off and turn-on time, was selected.

- GATE - R_{goff}/R_{gon}: optional gate resistors to select the desired turn-on and turn-off timing. In this case, based on the graphs of the drive evaluation board for the 1EDL8011 (EVAL-1EDL8011), 3.3k and 5.1k values were chosen, resulting in a turn-on time of approximately 150us and a turn-off time of approximately 30us. The important parameter in this design is the turn-off time, as the BMS is always in output mode when properly functioning [10].

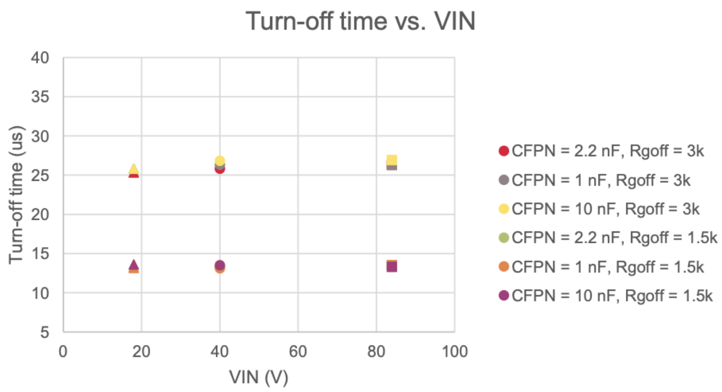

Figure 4.18: Expected Approximate Turn Off time

- VIN and VS : connected to the MOSFET's source and drain

4.4.2 MOSFETs configuration

The MOSFETs selected are the Infineon IAUT200N08S5N023 (OptiMOS 5, 80 V) [11]. The main characteristics are:

- $R_{DS(on)} = 2.3\text{m}\Omega$ at $V_{GS} = 10\text{V}$
- $I_D(\text{max}) = 200\text{A}$ (package-limited)
- $V_{GS(max)} = \pm 20\text{V}$

To achieve the specified $R_{DS(on)}$, the gate must be driven to $V_S + 10$–12V. That is ensured by the charge pump of the 1EDL8011.

Once the required voltage is applied to the gate, the MOSFET enters the ohmic region allowing the current to flow with minimal resistance and thus the output is activated.

The conduction losses are:

$$P_{cond} = I^2 \cdot R_{DS(on)}$$

For a nominal current of $I = 30\,\text{A}$:

$$P_{cond} = (30\,\text{A})^2 \cdot 2.3 \times 10^{-3}\,\Omega \approx 2.07\,\text{W}$$

At elevated junction temperature ($T_j = 125°\text{C}$), the $R_{DS(on)}$ typically increases by a factor of ≈ 1.8:

$$R_{DS(on,125°C)} \approx 1.8 \cdot 2.3\,\text{m}\Omega \approx 4.1\,\text{m}\Omega$$

$$P_{cond,125°C} = (30\,\text{A})^2 \cdot 4.1 \times 10^{-3}\,\Omega \approx 3.7\,\text{W}$$

In this way it's confirmed that condition losses remain acceptable but require proper thermal management.

The MOSFETs are used in a back-to-back common-source configuration to form a BPS (Bidirectional Power Switch) which is an active switch that can support bidirectional current flow when it is in the ON condition and bidirectional voltage blocking when it's turned OFF [12], thereby solving the problem.

This is necessary because, as specified in 1.2, overvoltage protection must also be present in the charging state. If only a single MOS is connected, current can flow through the antiparallel diode.

Finally, a 30 A fuse is present at the output, as required by the rules.

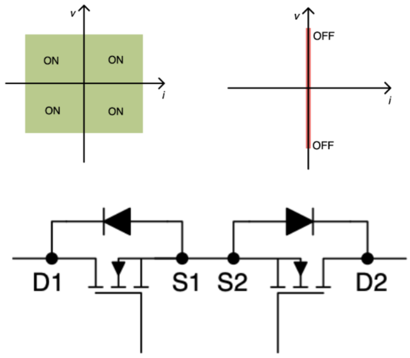

Figure 4.19: BPS Configuration and its characteristics in ON and OFF system

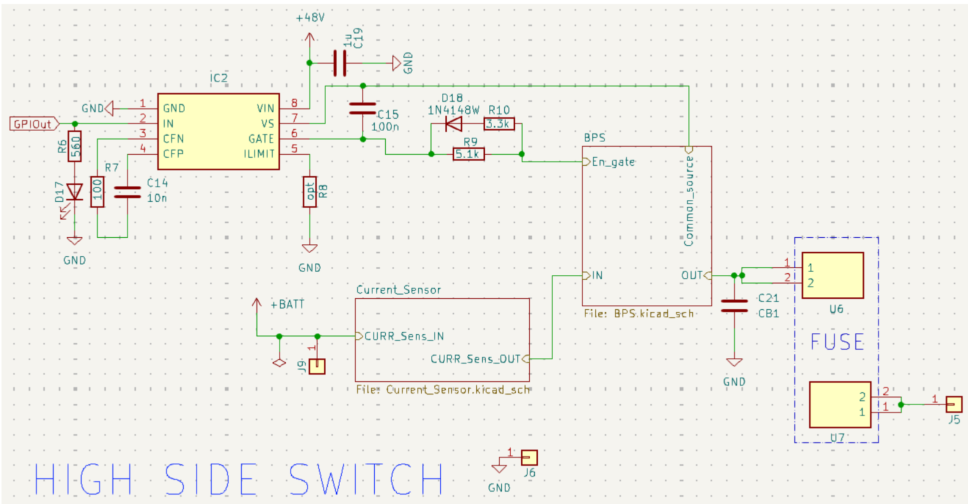

Figure 4.20: Output Delivering Circuit

4.5 Power Management

The power architecture of the board employs a two-stage design to prevent excessive thermal stress. The system draws power from a 48V battery supply. It can also be powered directly from the onboard USB-C port.

- **48 V to 5V** :

  The first stage uses a DC/DC switching regulator (R-788HE5.0-0.3), configured with two 2.2μF capacitors placed next to the input for decoupling and stability. This minimizes thermal dissipation and powers the LTC6811 directly, eliminating the need for extra components like transistors.

- **5V to 3.3V** :

  The second stage uses an LDO regulator (LD1117S33TR) to provide a 3.3V line for the microcontroller. The capacitor network, as specified in the datasheet, supports stability and noise suppression.

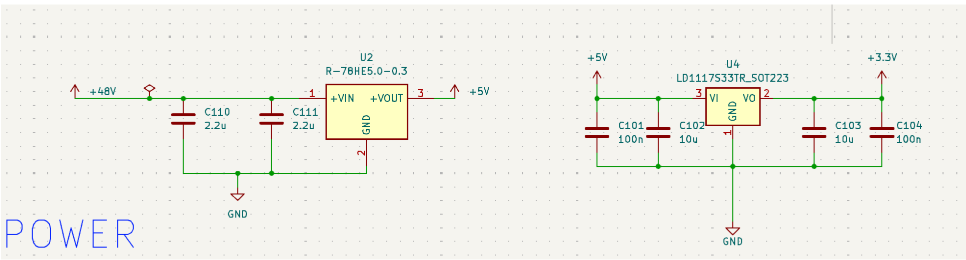

Figure 4.21: Power management schematic

Chapter 5

Layout design

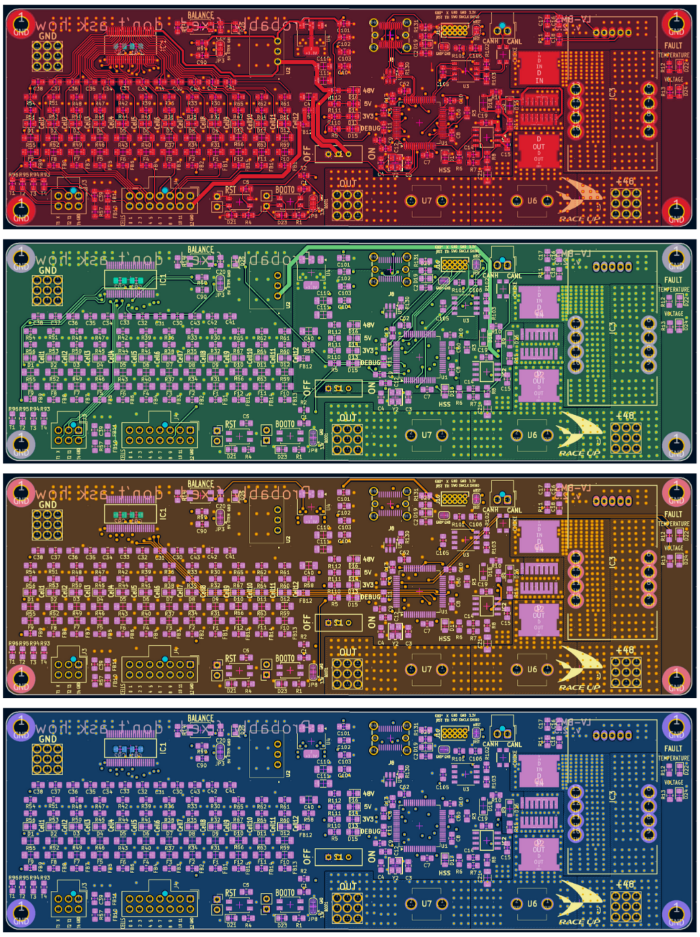

Figure 5.1: Layout of the PCB

5.1 PCB Layout

When designing a PCB, it is crucial to understand that the layout affects not just the physical arrangement of components but also the functionality, safety, and reliability of the BMS. Poor layout can lead to electromagnetic interference (EMI), voltage drops, thermal issues, and compromised signal integrity.

This design must handle both high voltage (48V) and high current power electronics, as well as sensitive low voltage control circuits.

The layout for this project follows best practices to ensure reliable operation. Shorter traces were implemented to minimize parasitic inductance.

5.2 Layering and Zoning

The board is a 4 layer PCB, enabling effective current distribution, greater routing flexibility, and reduced dimensions to fit within the narrow LV case. Its final size is 53 by 169 mm.

The board is physically divided into two main parts:

- CONTROL : The left central side contains low voltage control electronics, including the microcontroller, balancing circuit, LTC6811, DC-DC converter, and communication interfaces.

- POWER : The right side contains the high current stage, which handles up to 30 A at 48 V for battery connections, current sensing, and output delivery.

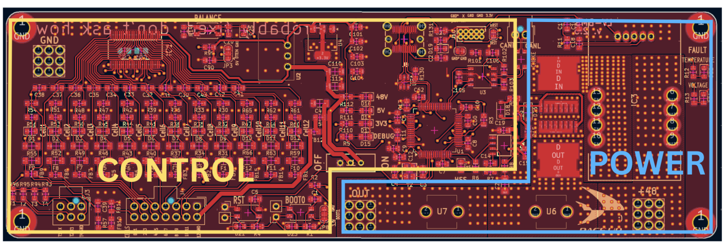

Figure 5.2: Layout division

The zoning minimizes noise from switching currents, thereby improving accuracy and stability in sensitive measurement and logic circuits.

The top layer is used for component placement and signal routing. One inner layer features a 3.3V zone near the microcontroller, providing a stable digital control supply and easier routing. The bottom layer is a continuous, low impedance ground plane. Remaining areas on each layer are filled with ground to improve EMC and reduce path impedance. Three large copper zones, connected by vias, carry high voltage and current on all layers, reducing resistive losses and aiding heat dissipation.

Thus, there is no rigid separation of functions per layer, but rather a layered strategy that combines routing flexibility with power integrity and thermal reliability.

5.3 High Current Paths and Thermal Management

A critical aspect of the board's right side is the potential for 30 A at 48 V through the MOSFET, current sensor, and fuse. Instead of thin copper traces, zones were used to reduce resistance. The minimum required trace width can be estimated using IPC-2221 guidelines. For external layers, the required trace width can be estimated using the IPC-2221 empirical formula:

$$W = \left(\frac{I}{k \cdot (\Delta T)^{0.44}} \right)^{\frac{1}{0.725}}$$

where:

- W is the trace width [mils],
- I is the current [A],
- $k = 0.048$ for external layers,
- ΔT is the permissible temperature rise [°C].

For a current of 30 A and a temperature rise of 20 °C, the calculated trace width is 29.6mm, justifying the use of copper zones over single traces. While 30A is the maximum current, typical values will be lower.

Thermal vias were added below MOSFETs, current sensors, and power regulators to transfer heat into internal copper planes. This improves dissipation, mechanical reliability, and reduces resistance and parasitic inductance.

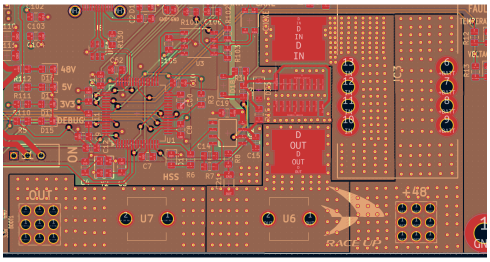

Figure 5.3: High-current zones with the VIAs

5.4 Signal Integrity

- Due to the high-speed communications and sensitive analog signals, careful routing is necessary. CAN bus and USB differential pairs must be short, symmetric, and kept at a constant distance whenever possible.

- Oscillator traces are kept as short as possible and shielded from power paths to reduce noise coupling.

- Signal traces have a width of 0.25mm.

- Power distribution must ensure high-frequency noise suppression and stable supply. Otherwise, the overall system can be affected.

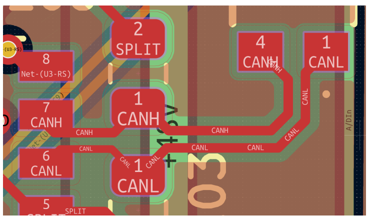

Figure 5.4: Differential traces for the CAN signals

  - All decoupling capacitors were placed as close as possible to the voltage source. For example, in the LTC, they were placed on the bottom layer adjacent to the pins.

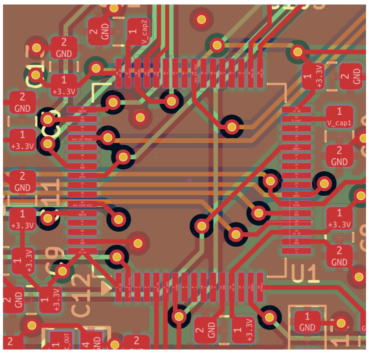

Figure 5.5: Decoupling capacitors positioning near the STM32

- The 48V line feeding the DC-DC converter was routed with increased trace width to ensure low resistive losses.

5.5 Silkscreen and Manufacturing

To facilitate testing, every connector, jumper, and test pad is clearly labeled.

Most boards were hand soldered; therefore, the footprints were chosen to facilitate hand soldering and simplify assembly. Additionally, vias have a diameter of 0.3mm to minimize additional costs.

5.6 Grounding

The bottom layer is a continuous ground plane. This is important because it provides low impedance return paths and EMC improvements by minimizing loop areas.

Chapter 6

Testing and Software design

6.1 Testing

Initial testing was conducted in functional mode to verify the basic operations of each module, including voltage sensing, current sensing, temperature measurement, balancing, output delivery, and communication. Due to the occurrence of various errors during testing, focus was on identifying root causes and implementing solutions to prevent recurrence. During this phase, certain components, such as the MOSFET, underwent testing. After individual modules passed initial testing, all modules were integrated, and more comprehensive system testing was performed to ensure reliability. After several months of iterative development and bug resolution, testing confirmed consistent sensor readings. The balancing function also operated correctly.

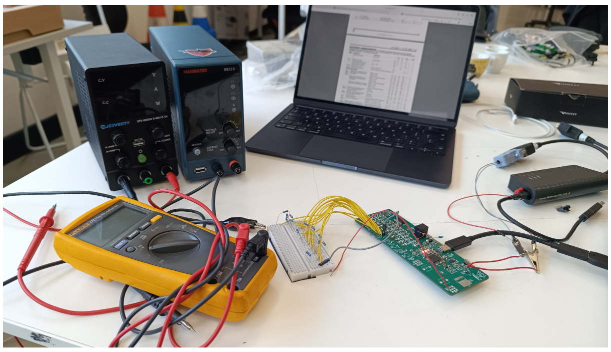

Figure 6.1: Example of a Testing Setup

6.1.1 Instrumentazion Used

Hardware

To test the board, multiple instruments were used: multimeters (specifically, the Fluke 177, CAT III, 1000V), oscilloscopes, wave generators and power sources, which were also used to charge the battery. power sources, which were also used to charge the battery.

Software

KiCad is the main software used for designing the board. While, for the firmware part, Git and Rust are implemented. Git is the main resource used by the software department to share and work on the code. Rust is the main programming language used for the BMS and other boards that are part of the vehicle's system.

6.1.2 Telemetry

In order to test the BMS with the entire vehicle system and monitor data in real time, a telemetry system was designed for the whole vehicle, including the low voltage battery pack. This system permits the simultaneous observation of the BMS and other subsystems in dynamic conditions (e.g., during acceleration, braking, and varying loads), which cannot be fully replicated in the laboratory.

For the purposes of this project, Grafana was selected because of its real time data visualization as well as parameter flexible configuration on its customizable dashboards. Moreover, since it is a web based application, telemetry data can be accessed without the installation of additional software by the entire team.

6.2 Software design

Although the main focus of this thesis is the hardware design of the BMS, the software layer plays obviously a crucial role in monitoring and controlling the battery cells.

Figure 6.2: Grafana Telemetry: LV data

The hardware related task including schematic, design and PCB layout were carried out by the author while the control software of the BMS was developed by another member of the RaceUP team in the software department. The complete code repository is available at `https://github.com/raceup-electric/bms_lv_rust`.

6.2.1 Communication

CAN

The Controller Area Network (CAN) is a communication bus used in the automotive industry, developed by Bosch in the 1980s. It has become an institution because it doesn't need a host computer, is very reliable, and features robust error detection. The baud rate is at 1 Mbit/s. It is physically formed of two differential lines, and the CAN bus must be terminated with a 120 Ω resistor.

In the car, there are three CAN lines: the first is dedicated to the inverter for messages regarding the motors, the second is for driverless control, and the third is for all the other boards. The BMS operates thus on the third line.

SPI

The SPI (Serial Peripheral Interface) line is one of the most commonly used interfaces between microcontrollers and peripheral ICs. In this case, the STM32 is used to interface with the LTC6811.

Its connection has 4 wires:

- Clock (SPI, CLK, SCLK)
- Chip select (CS)
- Main Out, Subnode In (MOSI)
- Main In, Subnode Out (MISO)

MISO and MOSI are the data lines used to send and receive information, and their connection is the same for all devices. SCLK is the clock that keeps everything in sync, while CS (chip select) is used to tell which device should listen and talk at a given moment. In this setup, the STM32 is the master and the LTC6811 is the slave.

Looking at the bigger picture, CAN and SPI have different purposes in the car. CAN is designed to connect multiple control units and maintain reliable communication, even in the presence of noise or interference. SPI, on the other hand, is much faster but only works over short distances, like between a microcontroller and a sensor or chip. CAN is better for sending messages across the entire system, while SPI is well suited for fast and direct communication with a single device. Using both provides the car with a combination of reliability on the network side and speed on the hardware side.

6.2.2 LTC6811

State Diagram

The LTC6811 behaves as a finite state machine, controlled by a set of commands transmitted via the SPI. Each command is a 16 bit word sent MSB first along with a 15 bit packet error code for error checking.

Description of the state diagram:

- *Sleep State*: References and ADCs are powered down to minimize current consumption. All the internal state machines are reset, and a wake up signal brings the IC to standby.

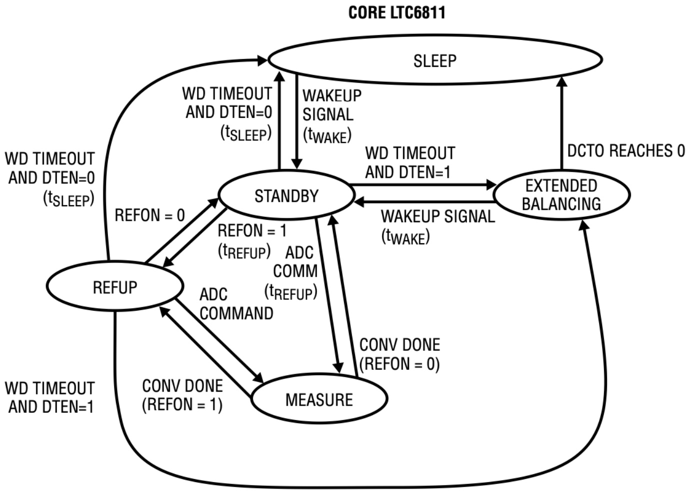

Figure 6.3: LTC6811-2 State Diagram

- *Standby State*: References and ADCs are off, but the watchdog and discharge timer are active. When a valid ADC command is received, the references are enabled, and the IC transitions to *Refup* or *Measure*. If no activity occurs, it returns to sleep or enters extended balancing.

- *Refup*: Only the voltage references are active, while the ADCs remain off. When a valid ADC command is received, it goes into *Measure* state to begin the conversion. Otherwise, it can get to *Standby*, *Extended Balancing*, or *Sleep*.

- *Measure state*: Reference and ADCs are on. Once the conversion is done, it transitions either to *Refup* or *Standby*.

- *Extending Balancing State*: Occurs when the watchdog timer has expired but the discharge timer is still running. In this state, discharge of the cells may be in progress. If there is a wakeup, it goes to *Standby*.

6.2.3 ADCs

As already stated, the LTC6811 incorporates two 16 bit Delta-Sigma ADCs. They operate simultaneously when measuring twelve cells, but only one ADC is used to measure the general purpose inputs.

These ADCs provide high measurement accuracy, depending on the selected mode. The filter bandwidths are mainly three, but others can also be selected. The main are Normal at 7kHz, which ensures high resolution and low tme and is better since it's more precise, FAST at 27kHz with some increase in TME and noise but it's more fast that can be useful of fast charge/discharge or fault detection, and 26Hz which is the filtered mode, the accuracy is similar to the normal mode but it the noise is lower and of course is slower.

In this application, fast mode was implemented, as it offers a good trade-off between the three main uses, particularly for the dynamic phase. In this way, the Total Measurement Error (TME) is $\pm$ 4.7mV at 3.3V at 25 degrees Celsius.

6.2.4 Main Commands

The LTC6811 uses several key commands for operation. All the specific configurations of each bit can be found in the LTC6811 datasheet. Here are reported the most important ones:

- **WRCFGA = [0x00, 0x01]** and **RDCFGA = [0x00, 0x02]**: write and read configuration registers.
- **RDCV A-B-C-D = [0x00, 0x04-6-8-A]**: read battery cell voltages.
- **RDAUXA = [0x00, 0x0C]** and **RDAUXB = [0x00, 0x0E]**: read auxiliary GPIO voltages, typically from thermistors for temperature monitoring.
- **ADCV = [0x02, 0x60]**: initiates measurement of the cell voltages.
- **ADAX = [0x04, 0x80]**: initiates measurement of GPIO inputs.
- **PLADC = [0x07, 0x14]**: checks the ADC conversion status.

6.2.5 Current Measurement

Current sensing is performed by sampling the voltage from a current sensor connected to the ADC. The procedure involves:

1. Setting the ADC to 12 bit resolution.
2. Taking multiple readings (10 samples) to determine the zero current offset.
3. Averaging additional samples (50) to reduce noise.
4. Converting the measured voltage to current using the sensor's sensitivity (9.2 mV/A).

This allows the software to continuously monitor the battery current and update the BMS state.

6.2.6 Temperature Management

Temperature is monitored using thermistors connected to GPIO pins. The software:

- Reads the GPIO voltage corresponding to each thermistor.
- Calculates the thermistor resistance using the voltage divider formula:

$$R_{\text{thermistor}} = R \cdot \frac{V_{\text{GPIO}}}{V_{\text{ref}} - V_{\text{GPIO}}}, \quad R = 22\,\text{k}\Omega$$

- Converts resistance to temperature using the Beta equation:

$$\frac{1}{T} = \frac{1}{T_0} + \frac{1}{B}\ln\left(\frac{R}{R_0}\right), \quad B = 3435,\ R_0 = 22\,\text{k}\Omega,\ T_0 = 25^{\circ}\text{C} = 298.15\,\text{K}$$

- Converts the temperature from Kelvin to Celsius and scales it for the BMS representation.

6.2.7 Cell Balancing

Balancing is implemented in software by comparing each cell voltage to the minimum cell voltage. If a cell voltage exceeds the minimum by a threshold (5 mV), a corresponding discharge bit is set in a 16 bit variable. The lower 8 bits and upper 4 bits are written to the IC's configuration registers to enable discharge for selected cells.

Chapter 7

Conclusion and future developments

The BMS developed in this thesis was validated in-vehicle over several months and demonstrated- strates robust operational performance, ensuring high reliability for the SGe-08 Formula Stu- dent electric vehicle. The system continuously monitors cell voltages, currents, and temperatures across 12 battery cells, implements passive cell balancing using the LTC6811, and supplies the low-voltage subsystem at 48 V to meet Formula SAE compliance.

Despite these successes, there remain areas for further improvement:

- **State of Estimation** (SoE): As previously stated, the current BMS does not include State of Charge (SoC), State of Health (SoH), or other SoE algorithms. Adding these features would enhance diagnostics, optimize operation, and extend battery life. Future versions could use predictive models and machine learning-based diagnostics to improve energy management and maintenance. This advanced approach may be more appropriate for the HV battery system.

- **Active Balancing**: The current BMS uses passive balancing due to its design simplicity and cost efficiency. Future development could investigate active balancing architectures, which, as discussed in the thesis, can improve energy transfer efficiency and minimize dissipation losses.

In conclusion, the BMS of this project provides a robust platform for safe, reliable, and efficient battery operation in Formula Student vehicles, while still leaving room for improvement.

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