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Active load emulator for VRM

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Abstract

In this document, a brief introduction to the increasing power demands in data centers and their structure is presented. An analysis of single-phase and multi-phase voltage regulation modules (VRMs) is carried out to highlight the most important aspects of these topologies. Information about VRM PCB design is provided to emphasize critical issues related to high current derivatives. Load emulator analysis and possible solutions are then investigated. Two feedback networks are analyzed, and simulation results are reported. Finally, load emulator tests are performed to validate one of the two proposed solutions.

Sommario

In questo documento viene presentata una breve introduzione all'aumento della domanda di potenza nei data center e alla loro struttura. Viene effettuata un'analisi dei moduli di regolazione della tensione (VRM) monofase e multifase per evidenziare gli aspetti più importanti di queste topologie. Vengono fornite informazioni sulla progettazione dei PCB dei VRM per sottolineare le criticità legate alle alte variazioni di corrente. Successivamente, vengono analizzati l'emulatore di carico e le possibili soluzioni realizzative. Vengono esaminati due reti di retroazione e riportati i risultati tramite delle simulazioni. Infine, vengono riportati i risultati dei test condotti sull'emulatore per validare una delle due soluzioni proposte.

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1 Data center evolution and structure

This chapter would like to analyze voltage regulation modules and why they are used in several applications. It will focus on data centers structure, their evolution in recent years and why voltage regulation modules are essential to obtain the best performance from cards like GPUs and CPUs.

1.1 Data centers efficiency and power demanding evolution

First, it is important to emphasize one of the main applications of VRMs. The structure and characteristics of this component will be examined later in this document. For now, it is sufficient to note that VRMs are primarily used to supply power to data center boards. To fully appreciate their significance in this context, it is necessary to consider how they have become so essential in this field.

Starting from 2010, it is possible to identify three distinct phases in the evolution of data centers. Each of these phases is characterized by significant events or trends. To analyze this evolution over the past 15 years, a definition is necessary to fully understand the topic.

This first figure of merit is the Power Usage Effectiveness (PUE). It is defined as the ratio between the total energy consumed by the system to operate properly (E_T) and the energy used exclusively for computational tasks within the data center (E_C) [1].

$$PUE \triangleq \frac{E_T}{E_C} \tag{1.1}$$

This metric is a key indicator of data center efficiency. The closer the ratio approaches 1, the more efficiently the system operates, as it implies that nearly all of the consumed energy is devoted to computation. Most common infrastructures which are involved to support the data center are the following:

- Cooling system. It is the one which control operating temperature of all computational devices in data centers.
- Uninterruptible Power Supply (UPS). This system supply all device connected when a grid faults occurs. It operated also against operating voltage fluctuations. It is equipped by batteries and can provide energy to connected device for a brief period of time, such 3 or 5 minutes.
- Lighting. Which refers to data centers lights.

Phase 1: Server virtualization and initial efficiency gains (2010 2015) This phase is characterized by server virtualization and consolidation. With this approach, a physical server can be partitioned into multiple virtual servers also called virtual machines (VMs). Without virtualization, running an application required a dedicated physical server. With virtualization, multiple applications can run on the same server. There are several advantages to this approach:

- Efficiency. By employing virtual machines, multiple workloads can share the same hardware.
- Isolation. If one VM crashes all the others still run independently.
- Flexibility. VMs can be created, moved or deleted. The hardware can be keep the same.
- Cost and energy saving. Less number of data centers are needed for the same number of compute instances.

All these advantages led to various improvements. Most organizations adopted server virtualization. Electricity use per computation of a typical volume server has dropped by a factor of four. The watts per terabyte of installed storage have dropped by an estimated factor of nine. This resulted in substantial power savings, with electricity use increasing only moderately from approximately 194 TWh in 2010 [2]. In addition, the average PUE decreased from 2.5 in 2007 to 1.65 in 2014 [3]. This is a significant change in such a short period of time. These improvements are mainly the result of better-performing cooling designs and more efficient power distribution equipment.

Phase 2: Hyperscale migration and cloud consolidation (2015 2020) In that evolution phase dominates the hyperscale cloud adoption. This is cloud infrastructure which runs on globally distributed data centers. This evolution was carried on by big companies like Microsoft, Google and Amazon Web Services (AWS) whose purpose was the the reduction of PUE. By investing on this type of infrastructure lots of improvements derived:

- Higher resource utilization. Traditional data centers typically run at low server utilization, usually only 10–20%. Hyperscale ones use multi-tenancy[1] to increase utilization up to 40–70%, by exploiting the same hardware more efficiently.
- Better energy efficiency. Investments go mostly into liquid cooling improvements. This enhances energy usage, as most of the energy is no longer wasted on cooling.

[1]Multi-tenancy refers to multiple customers (tenants) sharing the same physical infrastructure while keeping their data separate

- Automation and error reduction. Automated monitoring reduces the need for manual operators, leading to fewer errors and enabling dynamic load balancing across servers.

- Custom infrastructure. By designing custom hardware, workloads run more efficiently compared to executing the same operations on generic chips.

This gives access to more users than before. During this phase, compute instances increased by roughly 550% from 2010 to 2018, while energy consumption grew by only about 6%, stabilizing around 205 TWh by 2018 [2]. Power Usage Effectiveness (PUE) was also reduced, thanks to advancements in energy efficiency. New cooling systems, high-level automation, and custom infrastructures contributed to achieving a PUE of 1.59 in 2020 [3].

In 2018, however, an efficiency plateau was reached, with PUE recorded at 1.58. Early in this phase, many improvements were made, but progress then slowed due to practical design limits.

Phase 3: AI-driven exponential growth (2020–2025) The last phase is the one dominated by exponential grows of data center driven by AI and digital acceleration catalyzed by COVID-19 pandemic.

The advent of COVID led a surge in cloud usage, remote work and streaming usage. Millions of employees start to use remote work, which last still today. Lockdown pushes also streaming services, as well as gaming platforms. In a brief period of time Workload demand grew significantly, thus increasing data center electricity consumption. The other main character is the IA diffusion. IA training and use require computational resources which vastly exceed traditional workloads. As an example, a single web search energy consume ten times lower than a single AI query. This power demand drives to an increase of power density and moved technology to liquid and immersion cooling systems.

All these changes drives from a $350\,TWh$ in 2020 to a approximately $460\,TWh$ in 2022 and will lead to data center total electricity consumption up to $1000\,TWh$ in 2026 (estimated) [4]. Average PUE instead slightly decreased from 1.59 to 1.56. Nevertheless many recent builds consistently achieve a PUE of 1.3, and some times much better [3]. This slight improve in efficiency is due to several factors:

- Most of data centers are older enterprise, not hyperscalers (PUE of 1.1 or 1.2). These are not provided with advanced cooling systems.

- Rack[2] power density is increasing. Comparing data between 2023 and 2024, rack power of $7\,kW$ to $9\,KW$ becomes more common [3]. Higher density means more heat per unit of volume which leads to higher cooling demand, expecially for older sites.

[2]This is basically the metal framework (cabinet) that holds servers, storage, and networking equipment

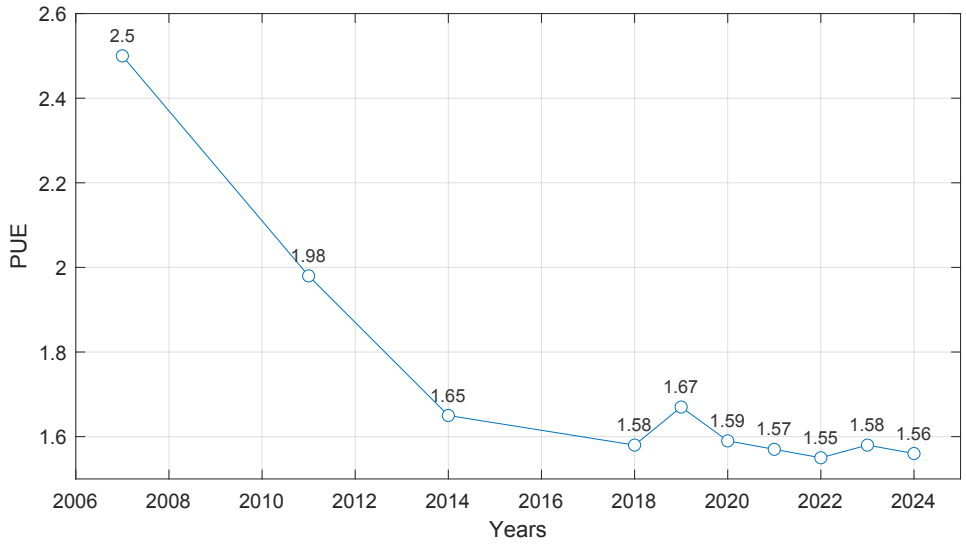


Figure 1.1: PUE and data center power demanding evolution from 2007 to 2024 [3]

- PUE does not account for IT systems energy performance. As more future facilities specialize in denser architecture as the limitations of PUE as a useful metrics increase. IT systems obtained substantial efficiency gains but these are not relevant in the PUE evaluation.

At the end of this phase, data center upgrades focus mainly on increasing energy density in order to support more powerful hardware. This is driven by the growing demand for data computation and management from AI, IoT devices, cryptocurrency mining, virtual reality, and high-definition streaming. To maximize efficiency, it is preferable to have fewer but more powerful racks. This shifts the attention to another key factor in data center structure, the power system.

PUE evolution from 2007 to 2024 is reported in Fig.1.1.

1.2 Data centers power supply systems

Up to now, the focus has been on data center needs and their evolution in recent years. PUE was once a fundamental factor, but in recent years it no longer accounts for most of the changes taking place. To understand the key role of VRM, the discussion now moves to the architecture of a data center's power supply system.

1.2.1 General overview of power supply systems

A typical data center power supply system from medium voltage (MV) grid to server PSU is reported in figure 1.2. It is composed by the automatic transfer switch (ATS), Low Voltage Power Distribution (LVPD), UPS, a power distribution units (PDUs) and power supply units (PSUs). ATS is involved to

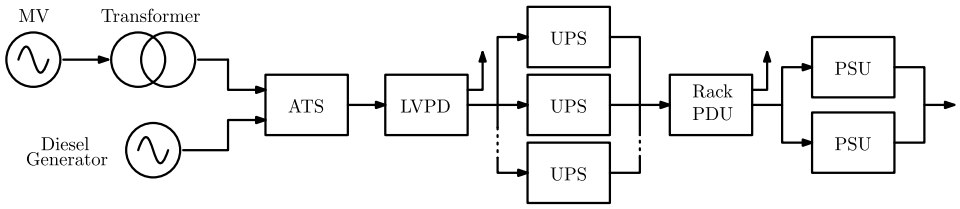


Figure 1.2: Typical data center power supply system from MV grid to server PSU

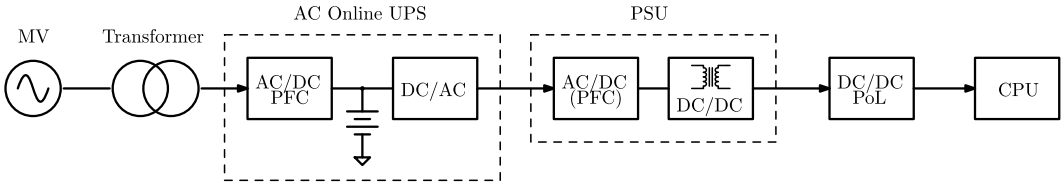


Figure 1.3: Data center power supply AC architecture scheme

select the optimal power source. LVPD which is involved to ensure safe and reliable delivery of low-voltage power and enable monitoring of power flow at distribution level [5].

Starting from the general scheme, power system architectures can be divided into three macro-groups. These are ac architectures, dc architectures, and hybrid architectures.

AC power architecture As is possible to see in Fig. 1.3, an AC architecture is built up with UPS, power supply unit (PSU) and PoL converter. A typical UPS employs a three-phase ac-dc stage for power factor correction (PFC) and a three-phase dc-ac stage, usually a back-to-back converter. The PSU instead involves two conversion stages, usually a boost-type PFC with $400\,V$ output and an isolated DC-DC stage converting $400\,V$ to a $12\,V$ or $48\,V$ bus. At the end there is the point of load (PoL) converter. Commercial UPS have two conversion stages, which efficiency is usually around $96\% - 97\%$. Instead 230-Vac input PSU must be in the range od 96% half-load efficiency and 91% full-load efficiency. The six conversion stages create a long conversion path which decreases the overall system efficiency and reliability. Nevertheless this type of configuration is consolidated and relatively cheap [5].

DC power architecture The main components of a DC power architecture are similar to those of an AC one, including a DC online UPS and a high-voltage direct current (HVDC) system that distributes power at the rack level. UPS uses the same three-phase PFC converter together with an isolated DC–DC topology, typically an LLC converter, to supply $240\,V$- $336\,V$ to the battery strings. The system also includes a PSU with only a DC–DC stage, thus avoiding the additional PFC stage that characterizes AC architectures, as shown in Fig.1.4(a). This solution reduces the number of conversion stages compared to the AC approach.

In a more simplified DC system, batteries are installed directly on the HVDC bus of the AC PSU, as illustrated in Fig. 1.4(b). This further reduces the number of conversion stages. In general, DC architectures with fewer conversion stages can achieve higher efficiency. However, HVDC breakers and protection systems are significantly more expensive than their AC counterparts. Other DC architectures are discussed in the literature, such as the Panama power supply system and those employing solid-state transformers (SSTs), but their discussion will not be addressed here [5].

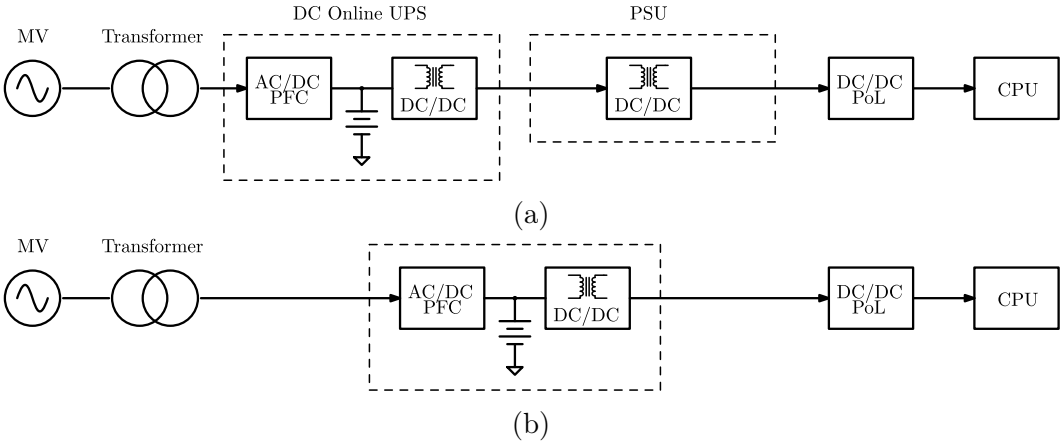


Figure 1.4: Two DC architectures. (a) HVDC architecture with dc PSU. (b) Simplified LVDC architecture

Hybrid power architecture This system involves two independent power distribution paths. Typically, these paths correspond to the systems shown in Fig. 1.3 and Fig. 1.4, which are summarized in Fig. 1.5. During normal operation, power is equally shared between the two paths. Efficiency is improved compared to two separate systems by removing the UPS from the AC path, which also reduces production costs. However, this configuration implies that there is no UPS protection in the AC path, resulting in lower reliability compared to two fully independent systems.

All these systems describe different methods to provide a $48\,V$ constant voltage (DC) to the PoL converter starting from the grid voltage. Architecture

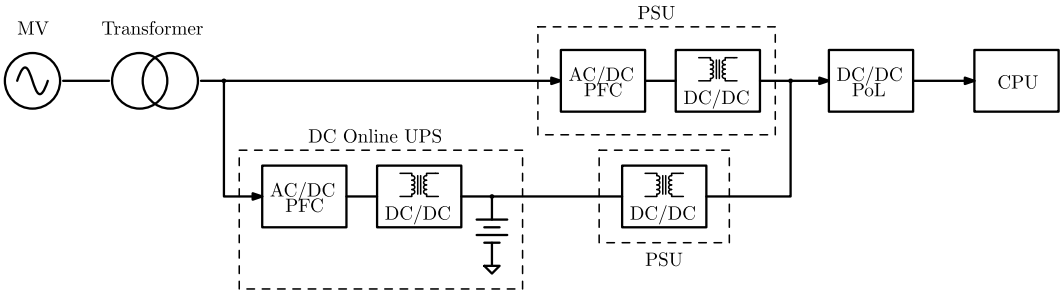


Figure 1.5: Data center power supply hybrid architecture scheme

choice depends on different factors, like efficiency, dimensions and distribution voltage. In fact, higher the distribution voltage, can significantly reduce cable loss.

1.2.2 PoL converters

The last conversion stage consists of PoL converters, which take a $48\,V$ input voltage and produce an output voltage, most often lower than $1\,V$. Point-of-load (PoL) converters, or power supply units, deliver power from the rack to the end loads, such as CPUs, GPUs, and storage devices. They are critical components for the overall efficiency of data centers. In fact, PoL converters are the least efficient devices in the entire power supply system. This is due to several challenges, starting from high conversion ratio, more than 10, high output current, more than $100\,A$, and high load transients. Up to 2023, typical Pol solutions involves single-stage multiphase buck topologies as voltage regulation module (VRM). Due to high nominal output current, hard-switching operation and very small nominal duty cycle, the peak efficiency just reaches 90%. Nowadays data center industry is moving to new $48\,V$ PoL solutions. [5] classifies four intermediate bus architectures (IBA) with a regulated bus and an unregulated bus.

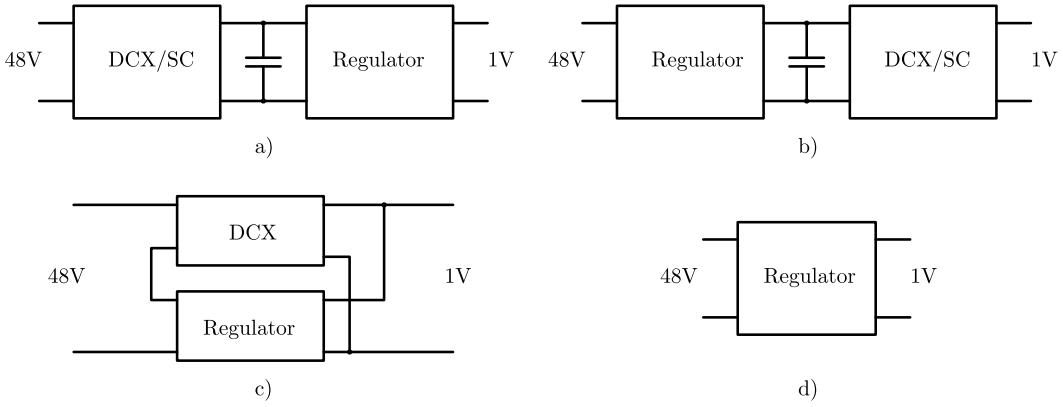


Figure 1.6: Pol architectures. (a) DCX-SC two-stage IBA. (b) Two-stage IBA with preregulation. (c) ISOP architecture. (d) Single stage converter.

- **DCX-SC two-stage IBA.** This structure involves a DC transformer (DCX) or a switched-capacitor (SC) topology in series with a VRM. DCX and SC converters do not require voltage regulation, since another upstream stage already regulates the input voltage. Their purpose is only to step down the input voltage by a specified factor. When properly driven, a DCX or SC converter can reach an efficiency of up to 99%, but the VRM limits the overall efficiency. (Fig. 1.6(a))

- **Two-stage IBA with preregulation.** This structure consists of a buck-boost converter followed by an LLC-DCX converter. (Fig. 1.6(b))

- **ISOP architecture.** In this architecture, the input terminals are connected in series while the outputs are connected in parallel. (Fig. 1.6(c))
- **Single-stage architecture.** This type of converter can be realized using different approaches, such as employing a current doubler or combining the SC principle with inductors. (Fig. 1.6(d))

2 VRM circuit analysis

In chapter 1 investigation on data center structure led to the analysis of PoL converters. This chapter will discuss data center power supply last stage, the VRM.

2.1 VRM definition and characteristics

VRM is the acronym for voltage regulation module. In practice, most of the time that block is a buck converter which provides to microprocessors, CPUs or GPUs the appropriate supply voltage, usually lower or equal than $1.8\,V$. The buck converter scheme is reported in Fig. 2.1. It involves 4 components, an upper switch, a lower switch, an inductor and a capacitor. The lower switch substitute a diode in the easiest buck topologies. Due to the presence of the bottom switch, this topology is also called synchronous buck. By proper driving the switches with a modulated square wave of period T_S is possible to achieve a step down of the output voltage.

2.1.1 Buck converter operation and conversion ratio

The most important parameters for a converter is the conversion ratio M and the duty cycle δ.

$$M \triangleq \frac{V_O}{V_I} \qquad \delta \triangleq \frac{t_{on}}{T_S} \tag{2.1}$$

V_I is the converter input voltage, V_O the converter output voltage, T_S the switching period and t_{on} which indicates the closed switch time. To analyze the buck converter, mode operation can be investigated. Only one mode is present thanks to the bottom switch, that is called continuos conduction mode (CCM). In CCM 2 operation phases can be found, while discontinuous conduction mode (DCM) is not present in that synchronous buck. Thanks to the bottom

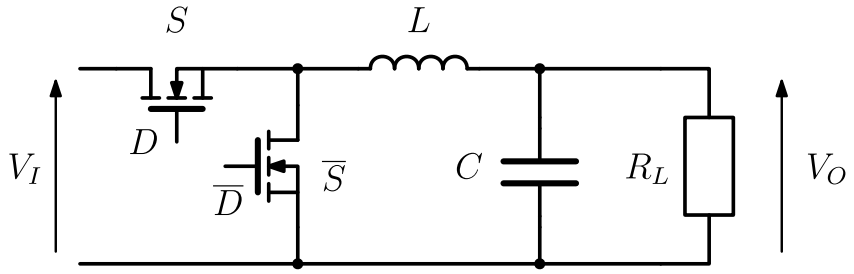


Figure 2.1: Buck converter basic circuit

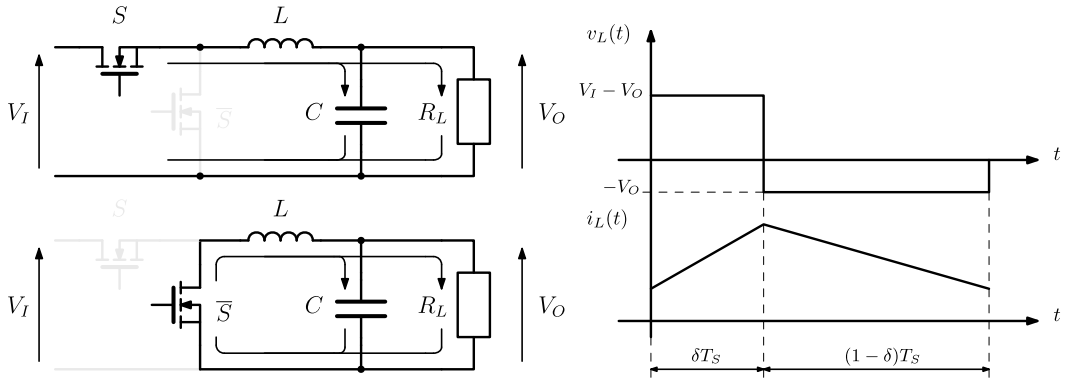


Figure 2.2: Buck converter CCM operation

switch inductor current can be lower than zero, thus avoiding DCM operation. Starting from CCM, is possible to evaluate the conversion ratio M by looking at the inductor current $i_L(t)$ and inductor voltage $v_L(t)$ waveforms in Fig. 2.2.

$$\begin{aligned}
0 \le t \le \delta T_S \qquad & v_L(t) = V_I - V_O \\
& i_L(t) = i_L(0) + \frac{1}{L}\int_0^t v_L(t)dt = i_L(0) + \frac{V_I - V_O}{L}t \\
\delta T_S \le t \le T_S \qquad & v_L(t) = -V_O \\
& i_L(t) = i_L(\delta T_S) + \frac{1}{L}\int_{\delta T_S}^t v_L(t)dt = i_L(\delta T_S) - \frac{V_O}{L}t
\end{aligned} \tag{2.2}$$

These equations show a rectangular inductor voltage shape and a triangular inductor current behavior. Then consider the voltage second balance (VSB) principle. In steady state, the relation 2.3 must hold.

$$\overline{v_L} = \frac{1}{T_S}\int_0^{T_S} v_L(t)dt = 0 \tag{2.3}$$

This can be used to evaluate M.

$$\overline{v_L} = \frac{1}{T_S}\int_0^{T_S} v_L(t)dt = \frac{1}{T_S}\int_0^{\delta T_S} V_I - V_O dt - \frac{1}{T_S}\int_{\delta T_S}^{T_S} V_O dt = 0$$

$$(V_I - V_O)\delta T_S - V_O(1-\delta)T_S = 0 \quad \Rightarrow \quad V_O = \delta V_I$$

$$M_{CCM} \triangleq \frac{V_O}{V_I} = \delta \tag{2.4}$$

This relation between input and output voltage of the converter is exclusively dependent on δ in CCM operation. δ can be easily controlled by an external MOS driver and controller.

2.1.2 Buck converter small signal model

The conversion ratio M provides information only in steady state, no transient information is provided. In this section, an investigation of small signal models, in buck converter case, is carried on.

A buck converter is not a linear time invariance system, this is due to the presence of non-linear devices like switch and diode. To analyze it, some precautions must be taken. Small signal model analysis will be done only in continuous conduction mode. First, the two topological states are considered.

$$S=1 \quad \& \quad \overline{S}=0 \quad \begin{cases} L\frac{\partial}{\partial t}i_L(t) = v_I(t) - v_O(t) \\ C\frac{\partial}{\partial t}v_O(t) = i_L(t) - i_O(t) \end{cases}$$

$$S=0 \quad \& \quad \overline{S}=1 \quad \begin{cases} L\frac{\partial}{\partial t}i_L(t) = -v_O(t) \\ C\frac{\partial}{\partial t}v_O(t) = i_L(t) - i_O(t) \end{cases}$$

These are two differential systems of equations that represent the two buck topological states. To obtain a general model it is necessary to have only one system of equations. Introducing a function $q(t)$ that is equal to 1 when $S=1$ and viceversa, it is possible to obtain only one differential equation system.

$$q(t) = \begin{cases} 1 & S=1 \\ 0 & S=0 \end{cases} \qquad \Rightarrow \qquad \begin{cases} L\frac{\partial}{\partial t}i_L(t) = q(t)v_I(t) - v_O(t) \\ C\frac{\partial}{\partial t}v_O(t) = i_L(t) - i_O(t) \end{cases} \tag{2.5}$$

This system of equations still represents a non-continuous system, because the current $i_L(t)$ is a triangular shape waveform. By considering average quantities, it is possible to deal with continuous waveforms. By considering small ripple approximation the following system is derived.

$$x(t) = \frac{1}{T_S}\int_{t-T_S}^{t} x(\tau)d\tau \qquad \Rightarrow \qquad \begin{cases} L\frac{\partial}{\partial t}\overline{i_L}(t) = \delta(t)\,\overline{v_I}(t) - \overline{v_O}(t) \\ C\frac{\partial}{\partial t}\overline{v_O}(t) = \overline{i_L}(t) - \overline{i_O}(t) \end{cases} \tag{2.6}$$

This average model is continuous but not linear, so it is linearized around the operating point I_O, V_I, D. Every quantity can be expressed as a steady state part X_I and a perturbation part x_i. When two quantities are multiplied by each other then only first-order terms are considered, second-order ones are neglected.

$$\overline{x_i} = X_I + x_i \qquad \Rightarrow \qquad \begin{cases} L\frac{\partial}{\partial t}i_l(t) = D\,v_i(t) + V_I\,\delta(t) - v_o(t) \\ C\frac{\partial}{\partial t}v_o(t) = i_l(t) - i_o(t) \end{cases} \tag{2.7}$$

This is a continuous and linear system considering only the perturbation part. By now applying the Laplace transform is possible to obtain the system 2.8.

$$\begin{cases} sL\,i_l(s) = D\,v_i(s) + V_I\,\delta(s) - v_o(s) \\ sC\,v_o(s) = i_l(s) - i_o(s) \\ v_o(s) = R_L i_o(s) \end{cases} \tag{2.8}$$

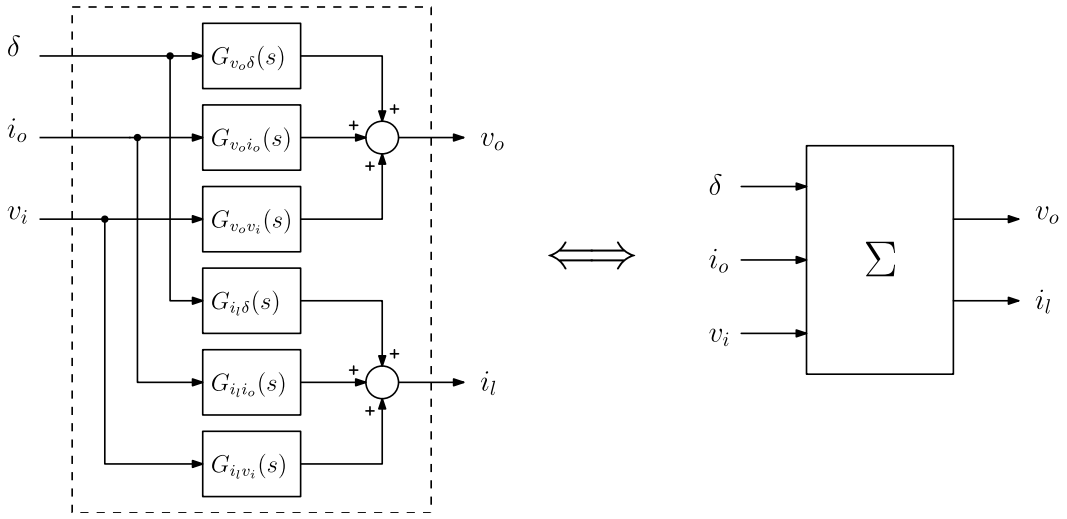


Figure 2.3: Buck small signal model scheme

This system has 3 inputs, duty cycle δ, input voltage v_i and output current i_o and 2 outputs or state variables, inductor current i_l and output voltage v_o. The outputs are obtained by a linear combination of the inputs as shown in figure 2.3. Weights of every contribution are frequency dependent and are defined as ratios. Some coefficients definitions are reported below.

$$G_{v_o\delta}(s) = \left.\frac{v_o(s)}{\delta(s)}\right|_{V_I=0,I_O=0} = \frac{V_I}{1 + s\frac{L}{R_L} + s^2LC}$$

$$G_{i_l\delta}(s) = \left.\frac{i_l(s)}{\delta(s)}\right|_{V_I=0,I_O=0} = \frac{V_I}{R_L}\frac{1 + sR_LC}{1 + s\frac{L}{R_L} + s^2LC}$$

All these coefficients or transfer functions give information about how the buck converter behaves when small input perturbations are applied to the system, such as a step load change, i_o variation.

2.2 Multiphase VRM

Today data center PoL converters are not classic buck converters. Due to the low voltage, lower than $1.2\,V$, and high current supply, above $40\,A$, classic buck converters are not suitable.

2.2.1 Multiphase buck description and motivations

A multiphase buck converter employs more than one triple of inductor, bottom and upper switch as shown in Fig. 2.4. This triple is also called phase of the converter. More than one phase gives multiple paths for the output current, and thus increases the maximum output current I_O. Switches driving signal is different in each phase, this is the key point of this topology. By interleaving

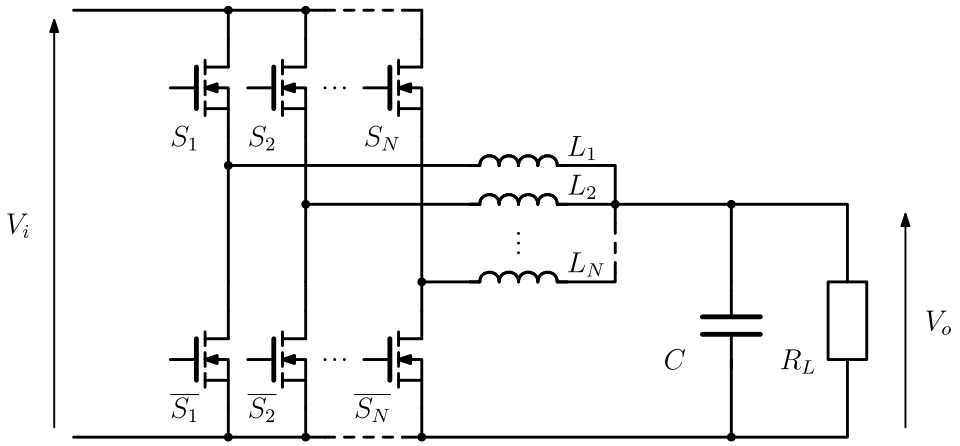


Figure 2.4: N-phases buck converter scheme

driving signals, current waveforms can sum and subtract and generate a lower ripple output current. This is not the only advantage of employing a multiphase buck. Several advantages of this topology are reported in the following.

- **Smaller components**.
  Considering a reference output current I_O^*, smaller components are necessary. Since each phase carries only a fraction of total I_O^*, inductor can be smaller in dimensions. At the same time, phase interleaving provides a lower output current ripple ΔI_O at an higher frequency than the switching frequency f_S. Considering the capacitor design equation, a lower current ripple Δi_C and a higher frequency means a lower capacitance C for the same maximum output allowed ripple Δv_O. Employing a N-phases converter the design equation results:

$$C = \frac{\Delta i_C}{8\Delta\, v_O\, N\, f_S} = \frac{\Delta i_{L,TOT}}{8\Delta\, v_O\, N\, f_S} \tag{2.9}$$

- **Lower losses**
  Considering a reference output current I_O^*, respect to a single phase converter, a multi-phase buck handle lower current per phase. Thus, losses on MOSFETs and inductors are reduced, preventing overheating.

- **Improved transient response**
  By increasing the number of phases the converter bandwidth increase. This is due to interleaving. Each phase has a proper control signal at the switching frequency f_S. In closed loop, if a step load occurs, phases can react to this change in a faster way. This will be discussed later when small signal model is introduced.

- **Scalability and redundancy**
  Designing a multiphase buck converter is easier if load current requirement changes. The entire converter design only needs to be adjusted

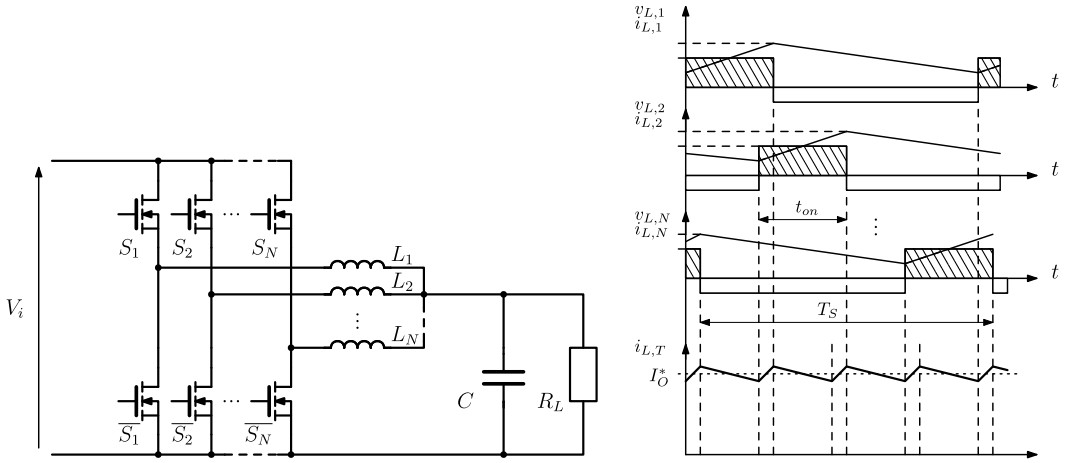


Figure 2.5: Multiphase Buck converter CCM operation

by increasing or decreasing the number of phases. At the same time, redundancy can be exploited. If one phase fails, then all the others keep the system running.

2.2.2 Multiphase buck operation and small signal model

The multiphase buck can work in both CCM and DCM, but, with respect to single-phase topology, a partial number of phases can be disabled. This is called phase shedding and can be achieved by modern analog and digital controllers. This saves power and increases efficiency at light load. For this reason only CCM operation will be analyzed.

With respect to single-phase buck converters, a lot of sub topologies can be found. These are derived from different switch combinations. In CCM for an N-phases buck converter, 2^N combinations can be found (if dead times[1] are not considered). With this hypothesis, the conversion ratio M is still equal to the single phase buck. In fact, by exploiting the VSB for every inductor the result is always the same, independently on the number of phases N.

$$M_{CCM} = \frac{V_O}{V_I} = \delta \tag{2.10}$$

Multiphase CCM operation is shown in Fig. 2.5.

The small signal model changes, instead. For every passive components it

[1]Dead time is a short, intentional delay inserted between the switching actions of two complementary devices (like the high-side MOSFET and low-side MOSFET in a buck converter leg) to ensure that both are never on at the same time.

is possible to write his characteristic differential equation.

$$\begin{cases} C\frac{\partial}{\partial t}v_O(t) = \sum_{i=1}^{N} i_{L,i}(t) - i_O \\ L_1\frac{\partial}{\partial t}i_{L,1}(t) = q_1(t)v_I(t) - v_O(t) \\ \qquad\qquad \vdots \\ L_N\frac{\partial}{\partial t}i_{L,N}(t) = q_N(t)v_I(t) - v_O(t) \end{cases} \iff q_j(t) = \begin{cases} 1 & S_j = 1 \\ 0 & S_j = 0 \end{cases} \tag{2.11}$$

By considering the average quantities, analyzing the system at a specific operating point, and applying the Laplace transform, the resulting set of equations is reported in Eq. 2.12. A schematic view of the small signal model is reported in Fig. 2.6.

$$\begin{cases} sC\, v_o(s) = \sum_{i=1}^{N} i_{l,i}(s) - i_o(s) \\ sL_1\, i_{L,1}(s) = D_1\, v_i(s) + V_I\, \delta_1(s) - v_o(s) \\ \qquad\qquad \vdots \\ sL_N\, i_{L,N}(s) = D_N\, v_i(s) + V_I\, \delta_N(s) - v_o(s) \\ i_o(s) = \frac{v_o(s)}{R_L} \end{cases} \tag{2.12}$$

For example, the transfer function between v_o and δ_i generic with all equal

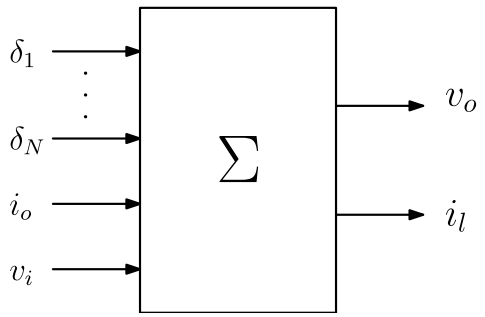


Figure 2.6: Multiphase buck converter small signal model scheme

inductance L is reported in Eq.2.13.

$$v_o(s) = \frac{1}{N}\frac{V_I}{1 + s\frac{L}{N\,R_L} + s^2\frac{L}{N}C}\delta_1(s) + \cdots + \frac{1}{N}\frac{V_I}{1 + s\frac{L}{N\,R_L} + s^2\frac{L}{N}C}\delta_N(s) \tag{2.13}$$

As can be seen, each phase contributes partially to the evolution of v_o. Exactly, it contributes as $1/N$. Then dynamics can be considered, two poles decrease the effect of $\delta_i(s)$ at higher frequencies. All transfer functions from $\delta_i(s)$ to $v_o(s)$ are equal if all inductance are equal. This means a perfect balance between phases. If the phase number increases, the effective inductance is decreased, thus increasing the pole frequency position and the whole controller bandwidth.

2.2.3 Multiphase buck application field

Nowadays VRM involves more than 10 phases to supply a xPU [2] [6]. In table 2.1 are reported some commercial graphic card including the employed VRM number of phases.

Product Name	**Producer**	**VRM phases**
NVIDIA Titan V	NVIDIA	16-phases [7] [8]
NITRO+ AMD Radeon™ 7900 XTX Vapor-X	Sapphire	20-phases [9]
GeForce RTX 3090	MSI	20-phases [10]

Table 2.1: VRM phases per commercial graphics cards

This shows how much are relevant the number of phases in VRM. Today, xPUs require very high current to work properly. But the high number of phases is not due only to nominal output current specifications, it depends on other factors.

2.3 VRM PCB displacement

Another important factor regarding power distribution is related to physical realization of multiphase VRM. In this section, a brief discussion about the evolution of PCB displacement and motivations is carried out. In the end, a state-of-the-art and a new emerging solution is presented. First of all is important to recall the definition of resistive power losses and resistance evaluation equation.

$$P_{R,LOSS} \triangleq R\,I^2 \qquad R\,(T) = \frac{L}{\mathcal{T}W} \cdot \rho_0 \cdot (1 + \alpha \cdot (T - T_0)) \tag{2.14}$$

I is the current flowing into a resistance R. The conductor portion is characterized by three dimensions, length L, width W and thickness $\mathcal{T}$. ρ_0 is the conductor resistivity at the reference temperature T_0. α is the conductor thermal expansion coefficient. Losses are associated to high currents and high value of resistance. This can be associated to energy-intensive loads or long PCB traces. Parasitic inductance, as well, plays an important role in power dissipation and must be taken into account when fast current transients occur.

2.3.1 VRM PCB early design

During the 1990s, the power supply generator was relatively far from the processor, as shown in Fig. 2.7(a). Initially, the operating voltage of the processors

[2] The term "xPU" is used in this text to indicate different devices like Graphics Processing Units (GPUs), Field-Programmable Gate Arrays (FPGAs), Tensor Processing Units (TPUs) and Application-Specific Integrated Circuits (ASICs)

was in the range of $2 \div 3\,V$, and the operating currents were no more than a few tens of amps (around $10\,A$). This means resistive losses in few centimeters were very low so distance between VRM and CPU was not a restrictive parameter. With the arrival of the Millennium core operating voltages drop below $1.5\,V$, and currents rise up to hundreds of amperes. Voltage drop between VRM and CPU increases to tens of millivolts, which was a great portion of the CPU supply voltage. Consequently, also $R \cdot I$ product becomes relevant. This led to designs in which the VRM was closer to the CPU like in Fig. 2.7(b). By reducing trace length, resistance R between VRM and CPU reduces, thus reducing also losses.

2.3.2 Multiphase VRM with horizontal power delivery

Until the early 2010s, VRMs used only a single phase to power xPUs. The high current demand of this approach became unsustainable. As a result, technology shifted toward multiphase VRM topologies, and PCB design evolved accordingly. To minimize trace length and avoid high-resistance paths, VRM phases are placed around the xPU, as shown in Fig. 2.7(c). This configuration is still used in data center PoL converters. In table 2.2 are the advantages and disadvantages of horizontal PCB placement reported. However, alternative VRM PCB design strategies are currently being developed.

The biggest problem with this horizontal design is exactly the same one it was created for. Even a few trace centimeters at low voltage (below $0.7\,V$) and high currents (above $2000\,A$) cause many unacceptable voltage losses and drops. Also parasitic inductance L_p plays a relevant role in the evaluation of voltage drop between VRM and xPU. Current transient in AI workloads can reach more than $3000 A/\mu s$. So also a small parasitic inductance (around

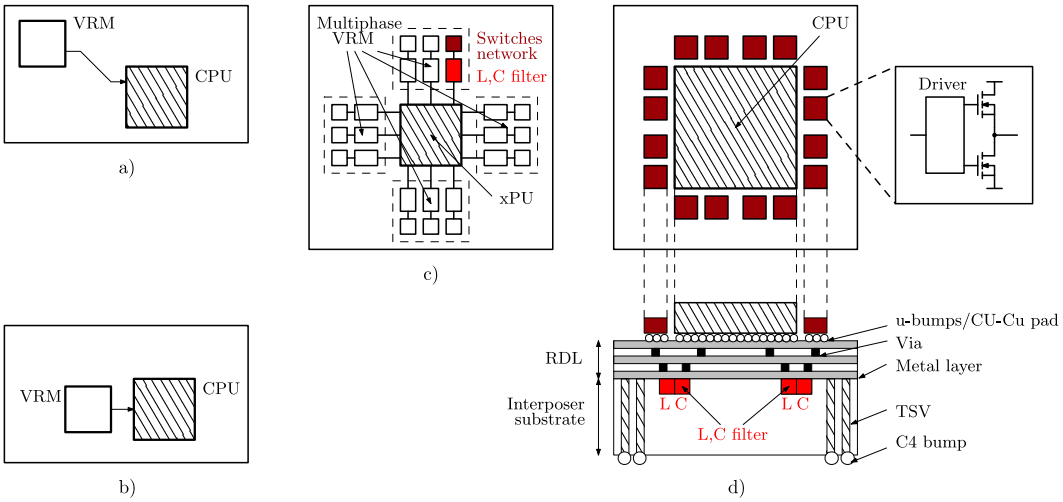


Figure 2.7: PCB layouts evolution. a) PCB layout during 1990s. b) PCB layout during 2000s. c) Multiphase VRM lateral distributed PCB layout. d) Multiphase VRM vertical distributed PCB layout.

Advantages	Disadvantages
Technological maturity: Well-known solutions with broad industrial support (e.g., Intel GPU VRM designs).	**Resistive loss ("Last Inch Problem"):** Even a few millimeters of low-voltage traces carrying high currents cause significant losses and voltage drop.
Modular scalability: VRM phases can be added around the die to increase output current.	**PCB footprint:** VRMs occupy significant space around the processor, limiting routing and placement of I/O components.
Reliability: Established layout and cooling solutions, with the possibility of using shared heat spreaders (VRM + GPU/CPU).	**Complex thermal management:** VRMs dissipate heat near the main load, increasing local thermal density.
	Scalability limit: Beyond certain current levels, the lateral space around the package is insufficient to mount all required phases.

Table 2.2: Advantages and disadvantages of horizontal multiphase VRM PCB design.

$100\,nH$) will provide tens of mV voltage drop.

$$v_{L,Drop} = L_p \frac{\partial i_O(t)}{\partial t} \tag{2.15}$$

To reduce all these effects the only solution is to involve a more compact VRM PCB design.

2.3.3 Multiphase VRM Vertical power delivery

The high power demands of recent years have driven significant evolution in multiphase PCB design. In some applications, load currents have exceeded $2000\,A$, while xPUs operate at voltages as low as $0.7\,V$, resulting in increased power losses on PCB traces. To address these challenges, vertical PCB design has been developed, as shown in Fig. 2.7(d) [11]. Different vertical design already exist, but in Fig 2.7(d) only one is reported. Instead of placing all VRM components in the same PCB plane, modules are placed vertically. Often they are inserted in different stacked layers above or under the package. Different layers communicate through "via" and through-silicon-via (TSV). Typical characteristics of vertical interconnections can be resumed in table 2.3. Two different components can be identified in this table. The motherboard represents the PCB, while the interposer and die are chip-incorporated layers. It is important to note that in Fig. 2.7(d), the package substrate and PCB

Packaging level	**Connection type**	**Material**
PCB/PKG	BGAs	solder
PKG/Interposer	C4 bumps	solder
Through-Interposer	TSVs	Cu
Interposer/Die	μ-bumps	solder
Interposer/Die	advance pad	Cu

Table 2.3: Typical characteristics of vertical interconnections [11].

are not shown. Referring to Table 2.3, the 3D layer structure is illustrated in Fig. 2.8. Ball grid arrays (BGAs), controlled collapse chip connection (C4) bumps, and μ-bumps are different types of interconnections. A BGA is an array of solder balls located on the bottom of a chip package, providing both mechanical and electrical connections between the chip package and the PCB. BGAs are preferable to pin grid arrays (PGAs) because they enable thousands of interconnections while offering a smaller footprint, lower inductance paths for power delivery, and cleaner digital signals. C4 and μ-bumps serve the same function as BGAs but with smaller diameters and at different integration layers, as summarized in Table 2.3.

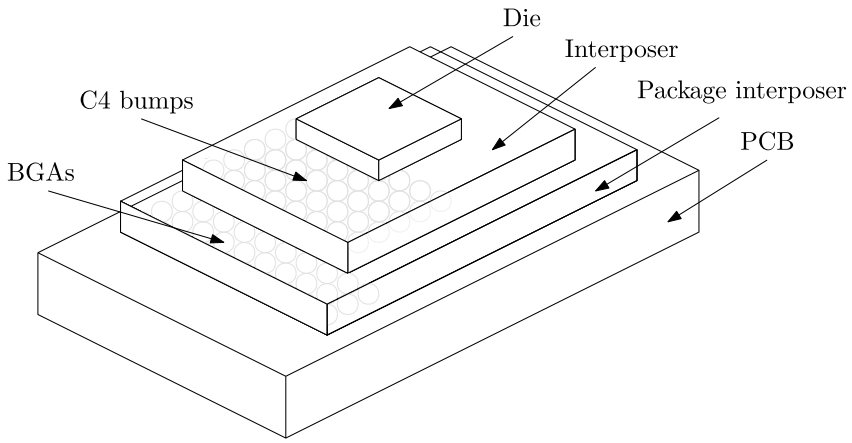


Figure 2.8: VRM vertical power delivery layer disposition

Advantages	Disadvantages
Drastic reduction of resistive losses: vertical connections have much lower inductance and resistance compared to PCB horizontal planes.	**Packaging complexity:** new technologies (interposer, co-packaging) are required and not trivial to industrialize.
Improved transient response: VRM is closer to the die, leading to smaller voltage oscillations.	**High costs:** 3D packaging and high-density materials increase the cost per component.
Power scalability: easier delivery of thousands of amperes without requiring massive copper planes.	**Thermal management challenges:** placing VRM above/below the die means heat must be dissipated very close to the chip, creating potential hotspots.
PCB space savings: less area occupied around the package, enabling freer routing.	

Table 2.4: Compact pros and cons of advanced vertical power delivery in IC packaging

3 Active load emulator

In chapter 2 VRM topology and his characteristics have been exploited. In this chapter a specific description of active load emulator is carried on. Starting from typical specifications, going on with principle of operation, emulator design, and the analysis of feedback topologies.

3.1 Load emulator characteristics

Load emulators, also called transient load testers or slammers, complexity increased in recent years accordingly with converters evolution. Greater demand on voltage sources to provide adequate power supply and voltage regulation led to an increase in testing sophistication.

VRMs are focus of this document, as previously explained in chapter 2. Relevant parameters to validate this type of converter are output voltage ripple and noise regulation, dynamic response and output impedance. Today, VRM output voltage v_O for data center applications are in the range of $0.7\,V$ and $1.5\,V$, while the maximum output voltage variation Δv_o depends on the load. To test these devices load emulators must have specific characteristics.

- **Step transition rate or slew rate** SR. It refers to the emulator capability of adequately exercise converter dynamic response. There is no common definition of slew rate in this context. In this document two definitions are used. The first one is similar to the one used for operational amplifiers. Slew rate is defined as the maximum current derivative over time during load transients. The second definition is defined as the ratio between the step load current ΔI_{LOAD} and the rise time t_R. These last two quantities are measured between the 10% and 90% of the current step.

$$SR_1 \triangleq \left.\frac{\partial i_{LOAD}(t)}{\partial t}\right|_{MAX} \qquad and \qquad SR_2 \triangleq \frac{0.8\Delta I_{LOAD}}{t_R} \tag{3.1}$$

  This type of stress depends on load step current, higher the current step ΔI_{LOAD} for the same system rise time t_R, higher could be the slew rate. At the same time, smaller is the rise time t_R for the same current step ΔI_{LOAD}, higher could be the slew rate. Is possible to associate slew rate to t_R and so to the system bandwidth.

  Another key factor is the parasitic inductance of connectors and board traces. The maximum variation of the current is limited by the value of parasitic inductance and voltage applied to it. At the same time,

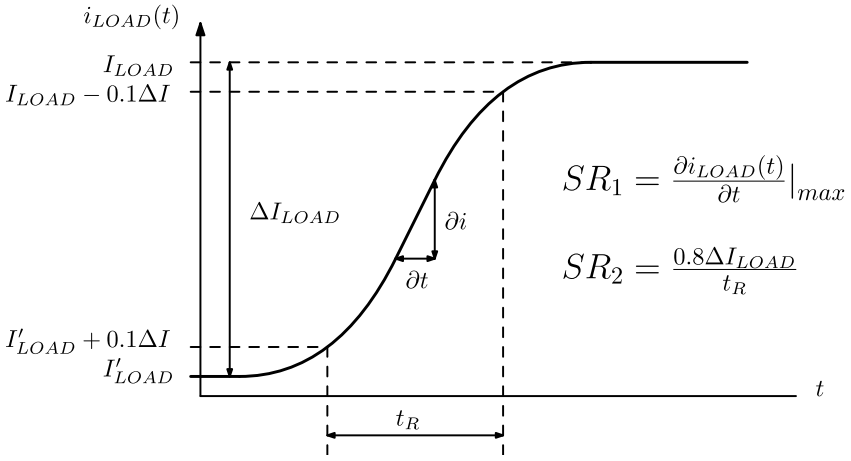


Figure 3.1: Emulator current waveform. Focus on slew rate definition.

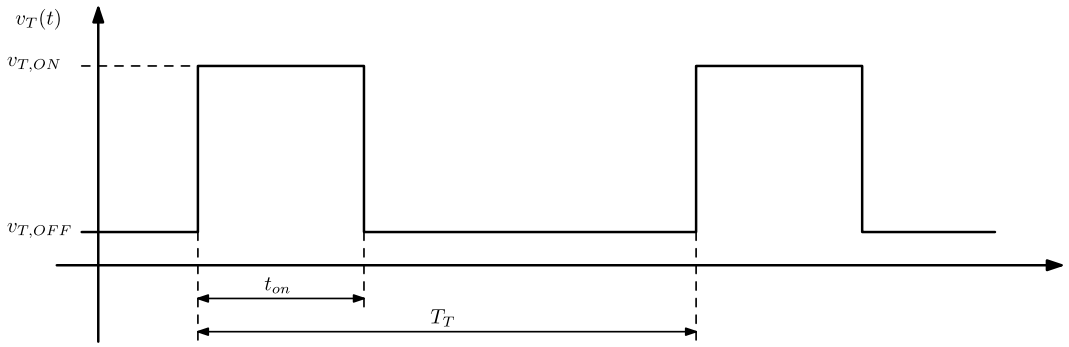


Figure 3.2: Emulator current waveform. Focus on test frequency f_T and duty cycle δ definition.

current sensing must be compensated to for their parasitic inductance if it is relevant.

$$\left.\frac{\partial i_{L_p}}{\partial t}\right|_{MAX} = \frac{\Delta v_{L_p,MAX}}{L_p} \tag{3.2}$$

A controllable slew rate is also a factor to take into account, since not all converters require high slew rate. Nevertheless an high SR is always useful to verify the system.

- **Controllable on time t_{on} and test frequency f_T.** Some times is needed to analyze multiple transient tests. To provide this capability, the emulator must involve a system to select test frequency $f_T = 1/T_T$ (T_T is the test period). Also test on time t_{on} have to be regulated, depending on device under test (DUT) transient time response. These parameters are reported in Fig.3.2.

- **Low-impedance connection to the board**. Typically, there is no room to place a load emulator directly on the DUT board. A multi-pin, low-inductance connector must therefore be employed to avoid limiting the SR, as previously explained, and to provide a low-resistance path.

This connector can later be removed when assembling the final board.

- **Adequate dissipation capability**. The load emulator must be able to withstand the maximum DC load current, and its safe operating area must be outlined for transients. The temperature of the device's internal components must remain below the maximum allowable limit. If small emulator dimensions are an important design factor, power dissipation design becomes critical. In such cases, smaller heatsinks must be used, or alternative devices must be selected.

- **Protection circuitry**. This is needed to preserve the device from overvoltage, overtemperature or reverse-voltage.

- **Instrumentation output**. Load emulators must provide information on the drained current. The converter or DUT output voltage can also be analyzed, but this is not strictly necessary.. The bandwidth of the slammer must be sufficiently high to reproduce the exact transient waveform. Instrumentation connectors, once again, must ensure a low-inductance path [12].

3.2 Load emulator design

First of all, specifications and constrains for the device are reported in table 3.1. A typical way to implement a current sink is by using a transistor, an op-amp,

Description	Symbol	Value
Emulator slew rate	SR	$3000\,A/\mu s$
Emulator drained current	I_{LOAD}	$640\,A$
Converter output voltage	v_O	$0.7\,V$

Table 3.1: Load emulator specifications and constrains

and a resistor, as shown in Fig. 3.3. By selecting the non-inverting operational amplifier configuration is possible to achieve v_S control. The drained current of $I_{LOAD} = 640\,A$ is far too high to be handled by a single MOSFET device. The solution is to divide the total current among multiple transistors. The number of transistors is, in fact, a free design parameter. If too few devices are used, for example, 4 or 6, the cost increases due to the strict specifications required for the nominal drain current I_D. On the other hand, the emulator cannot be made excessively large. In this work, 16 devices were chosen. Each MOSFET must provide a nominal drain current of $I_D = 40\,A$. The choice of 16 is not arbitrary: it matches the number of VRM phases used to test the device.

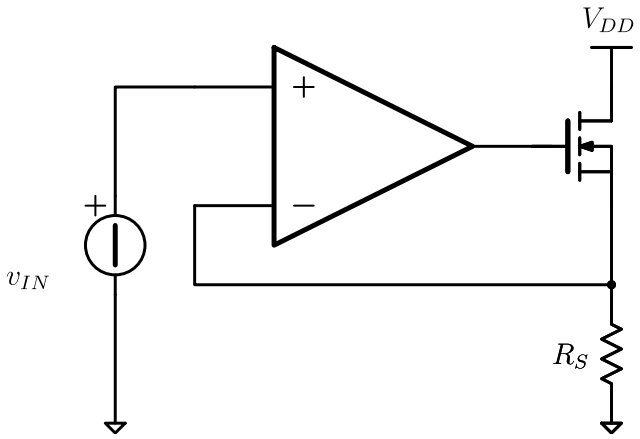


Figure 3.3: Basic controlled current sink

3.2.1 MOSFET selection

Now is necessary to select for a suitable device which is able to handle a nominal current $I_D = 40\,A$, able to withstand power dissipation without an heatsink, a gate to source voltage lower than $5\,V$, in order to not stress the operational amplifier and a small threshold voltage, lower than $3\,V$. The component selection was carried out using the Mouser distributor's filtering tool. The search began with an N-channel device based on Infineon's OptiMOS technology, with specifications of $I_D \geq 50\,A$, $-16\,V \leq V_{GS} \leq 16\,V$, and $V_t \leq 3\,V$. The $BSC009NE2LS5$ n-channel MOSFET has been chosen. Main characteristics are reported in table 3.2.

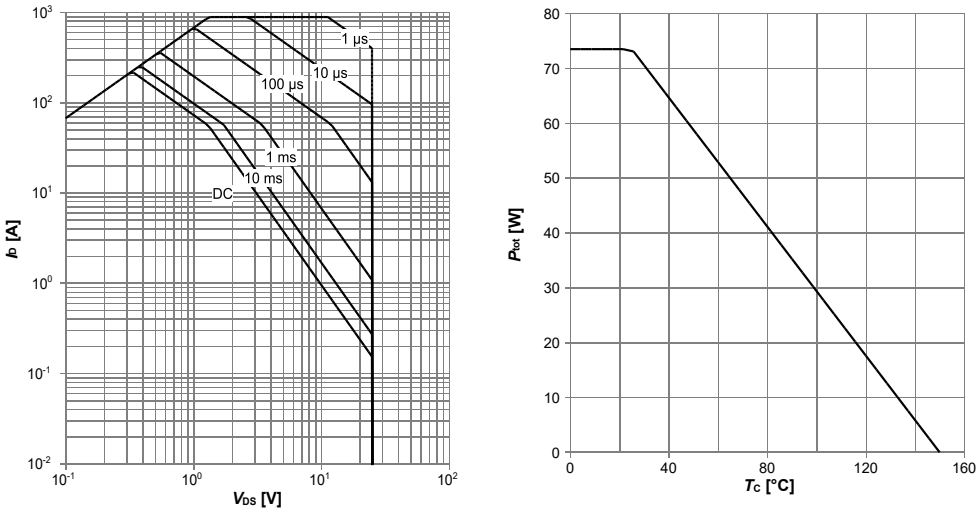
Description	Symbol	Value
Length x Width	L x W	$5.49\,mm$ x $6.35\,mm$ [1]
Package type		SuperSO8
Maximum current	$I_{D,MAX}$	$892\,A$
Maximum drain-source voltage	$V_{DS,MAX}$	$25\,V$
Threshold voltage	V_t	$1.6\,V$ [2]
On resistance	$R_{DS,on}$	$0.9\,m\Omega$ [3]

Table 3.2: $BSC009NE2LS5$ Infineon MOSFET main characteristics

OptiMOS power MOSFETs deliver best-in-class performance, combining high efficiency with high power density. Key features include ultra-low $R_{DS,on}$ as well as excellent efficiency and power density [13]. This means, a very compact device and high current-handling capability. The maximum current rating is not the primary selection criterion; in fact, the device can reach much higher

[1] Maximum values are reported
[2] This is a typical value
[3] This is a typical value

currents. Fig. 3.4(a) shows the safe operating area (SOA), which guided the MOSFET selection. The emulator must sustain an external converter voltage of $v_O = 0.7\,V$ and a drain current of $I_D = 40\,A$. DC operation is ensured by the intersection of these two parameters on the SOA graph. Nevertheless, the device is capable of handling higher currents for brief periods. Threshold voltage instead is equal to $V_t = 1.6\,V$, lower to $V_t = 3\,V$ initially imposed. This device can sustain a drain-to-source voltage of up to $V_{DS,MAX} = 25\,V$.



(a) (b)

Figure 3.4: $BSC009NE2LS5$ datasheet graphs. a) $BSC009NE2LS5$ safe operating area (SOA). b) $BSC009NE2LS5$ maximum power dissipation P_{TOT} vs case temperature T_J.

For this application, a smaller $V_{DS,MAX}$ would also have been sufficient. The elevated value, compared to $v_O = 0.7\,V$, is a consequence of the other design choices made. However, this also means that the load emulator can be used to test other types of converters with higher output voltages, up to $25\,V$.

To complete the MOSFET discussion, a brief and simplified thermal analysis is carried out. Section 3.2.3 discusses and motivate how many MOSFETs must be included in the Emulator. Here, 16 MOSFETs are considered. This means that each device must sustain a nominal current of $I_{D,NOM} = 40\,A$ to obtain a $I_{LOAD} = 640\,A$. To perform a thermal analysis $I_{D,NOM} = 40\,A$ is considered as a DC value and worst case. This can be verified by looking at Fig. 3.4(a). Considering a maximum $v_{DS} = 0.7\,V$ (VRM voltage v_O) and nominal current $I_D = 40\,A$, the intercept lead to DC operation can be performed. Datasheet also provide the maximum value of $R_{ds,MAX} = 0.9m\,\Omega$. Then single MOSFET maximum power dissipation $P_{D,MAX}$ can be evaluated.

$$P_{D,MAX} = R_{ds,MAX}\, I^2_{D,NOM} = 1.44\,W \tag{3.3}$$

Thermal resistances are considered to perform the thermal analysis. MOSFET datasheet reports three different values, they are reported in 3.3 The junction-

Description	Symbol	Value (MAX)
Thermal resistance, junction - case bottom	$R_{th,JC,b}$	1.7 K/W
Thermal resistance, junction - case top	$R_{th,JC,t}$	20 K/W
Thermal resistance, junction - ambient	$R_{th,JA}$	50 K/W

Table 3.3: $BSC009NE2LS5$ thermal resistances

to-case thermal resistance $R_{th,JC}$ has two different values depending on the considered surface. The top one is the plastic case, this means a poor heat transmission. This explain the high value of $R_{th,JC,t}$. The bottom surface is provided by a metal exposed paddle. In that case the $R_{th,JC,b}$ is much lower respect to $R_{th,JC,t}$, thanks to metal high heat conductivity. The equivalent thermal system is reported in Fig. 3.5. In this model only the thermal re-

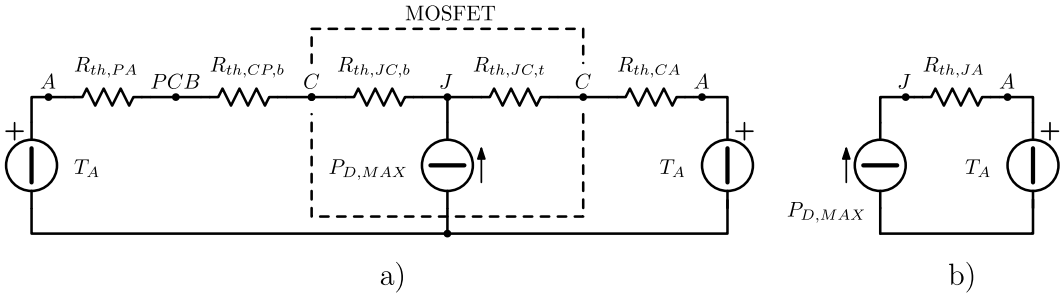


Figure 3.5: MOSFET equivalent thermal model

sistances reported in Table 3.3 are known. So instead of to evaluate $R_{th,PA}$ (PCB-to-Ambient), $R_{th,CP,b}$ (Bottom Case-to-PCB) and $R_{th,CA}$ (Top Case-to-Ambient), a simplified thermal model is used. That model is reported in Fig.3.5(b). Thanks to this model the junction temperature T_J can be evaluated considering $T_A = 25°C$.

$$T_J = T_A + P_{D,MAX}\, R_{th,JA} = 97°C \tag{3.4}$$

To verify if the device is capable of sustaining that power dissipation without an external heatsink, the case temperature T_C must also be evaluated. Since both $R_{th,JC}$ are known and heat transfer flows in both top and bottom surfaces, the case temperature T_C can be evaluated.

$$T_C = T_J - R_{th,JC,t}//R_{th,JC,b}\, P_{D,MAX} = 94.74°C \tag{3.5}$$

Looking at Fig. 3.4(b) with a case temperature $T_C = 94.74°C$ a single device is capable to sustain a power dissipation equal to $P_{TOT} \simeq 30\,W$. This value is much higher than the one evaluated at eq:3.3. This means no heatsink is needed.

Description	Symbol	Value
Length x Width	L x W	$7.35\,mm$ x $4.45\,mm$
Package type		GMR320
Nominal resistance	R	$5\,m\Omega$
Tolerance	F	$\pm 1\%$
Maximum power dissipation	$P_{D,MAX}$	$10\,W$

Table 3.4: $GMR320HJAAFD5L00$ ROHM Semiconductor resistor characteristics

3.2.2 Shunt resistor selection

The selection of R_S comes down to power dissipation versus precision. Smaller values of R_S yield smaller voltage drops for the same amount of current and ultimately dissipate less power. However, since the R_S voltage drop is smaller, higher precision components may need to be used to achieve the same error tolerance. A maximum dissipation power is set to $10\,W$, to have a resistor comparable to MOSFET dimensions $A_{MOS} \simeq 35\,mm^2$. This because above $P_{D,MAX} = 10\,W$ dissipation power, resistors are considerable in size, above $500\,mm^2$. This choice limits the R_S value.

$$R_{S,MAX} = \frac{P_{D,MAX}}{I_D^2} = 6.25\,m\Omega \tag{3.6}$$

Now if a lower resistor value is set, power dissipation will be lower. A suitable resistor is the $GMR320HJAAFD5L00$ from ROHM Semiconductor, which characteristics are reported in table 3.4. $P_{D,MAX}$ changes with temperature. Maximum power is constant if the device terminals temperature is kept below $70\,°C$. Above that temperature, its capability decreases linearly as $-1\%\,P_{D,MAX}/1°C$, up to $170\,°C$, at which maximum power dissipation is $0\,W$. The power dissipated by the resistor can be evaluated.

$$P_D = R_S I_D^2 = 8\,W \leq P_{D,MAX} \tag{3.7}$$

Then is possible to evaluate the voltage which presents at the opamp inverting input V^- when $I_D = 40\,A$.

$$V^+ = V^- = R_S I_D = 0.2\,V \tag{3.8}$$

This represents the controlled voltage to be applied to the operational amplifier in order to obtain a drain current I_D of $40\,A$.

3.2.3 Suitable operational amplifier analysis

The final component to be choose is the operational amplifier. This drives MOSFETs and keep the current I_D stable. To choose the optimal operational

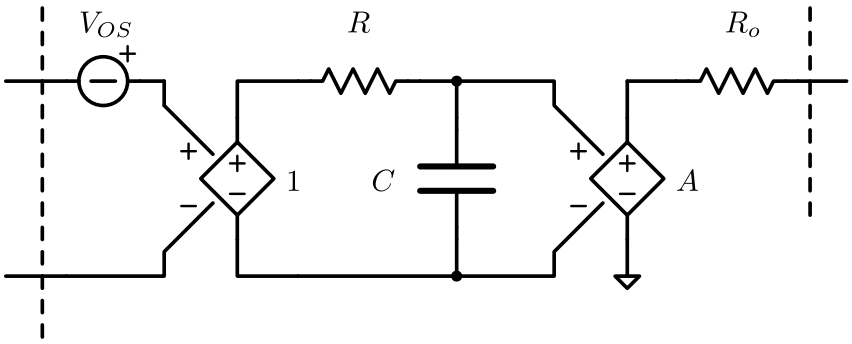


Figure 3.6: Operational amplifier LTspice self made model

amplifier a suitable LTspice model has been made. The operational amplifier model is reported in figure 3.6. A represent the amplifier DC gain, R and C sets the single pole of the device, R_o is the output resistance and V_{OS} the offset voltage. The pole location depends on R and C values. By imposing $R = 100\,\Omega$ and the pole frequency f_p then C can be evaluated.

$$C = \frac{1}{2\pi R f_p} \tag{3.9}$$

As a first simulation V_{OS} and R_o are set to zero for simplicity. Gain is set to $A = 80\,dB$, which is a typical and not prohibitive gain value, and the pole frequency is swept between $10\,Hz \leq f_p \leq 1k\,Hz$. The upper frequency is a relatively high value as an opamp first pole, but in that system the high slew rate specification lead to this selection. Circuit in figure 3.3 is reproduced in

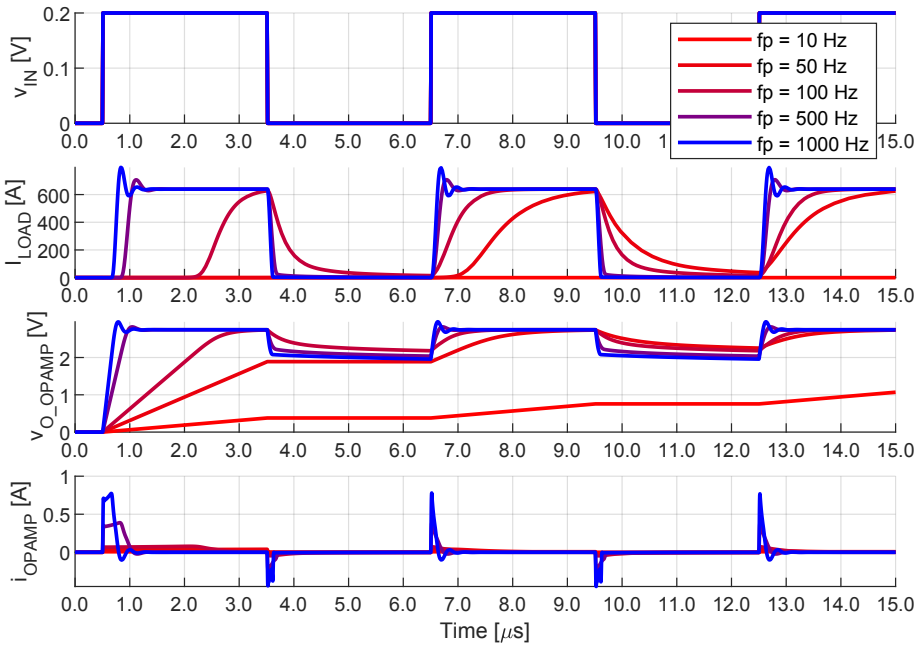


Figure 3.7: Main waveforms, f_p sweep LTspice simulation

LTspice, but in this case, 16 MOSFET are drived by a single opamp. Input signal is set as a square wave. Square wave period $T = 6\,\mu s$, on time $t_{on} = 3\,\mu s$, rise and fall times $t_R, t_F = 10\,ns$, an initial delay $T_{delay} = 0.5\,\mu s$ and amplitude $A = 0.2\,V$, which is the value evaluated at eq 3.8.

Now some simulations results are reported, in particular the input signal v_{IN}, the load drained current i_{LOAD}, the operational amplifier output current i_{OPAMP} and the MOSFETs gate voltage, which correspond to the amplifier output voltage $v_{O,OPAMP}$. In all simulations the LTspice MOSFETs model is involved. In figure 3.7 is reported the first simulation.

Above $f_p^* = 100\,Hz$, the current i_{LOAD} reaches the desired value, $640\,A$, within the on time t_{on}. For frequencies below this threshold, $f_p^* = 100\,Hz$, the system requires more time to fully charge the input capacitance of the MOSFET. Nevertheless, at the third v_{IN} step, the four i_{LOAD} waveforms are aligned, allowing the step response to be compared. This occurs because the MOSFET capacitance is fully charged in all four cases. The output amplifier voltage $v_{O,OPAMP}$ exhibits a characteristic pattern. After the MOSFET input capacitance is charged during the on phase, it does not return to zero instantly during the off phase, but instead decreases with an exponential behavior. The time constant is smaller for higher f_p. For example, the time constant is $\tau \simeq 0.3\,ms$ ($f_p = 500\,Hz$) and $\tau \simeq 0.5\,ms$ ($f_p = 1\,kHz$).

In Table 3.5, the measured current slew rate SR and the operational amplifier maximum output current $i_{O,OPAMP}$ are reported. Simulations show that SR increases as the first pole location f_p increases. At the same time, the amplifier output current $i_{O,OPAMP}$ also increases with f_p. The specification on SR is satisfied for both $f_p = 500\,Hz$ and $f_p = 1\,kHz$, but the amplifier output current $i_{O,OPAMP}$ reaches prohibitive values for this type of device. Reducing this current is the next step.

All MOSFET gates are connected together, resulting in a very high input capacitance that cannot be driven by a single device. Therefore, the adopted solution is to employ two different operational amplifiers. Now by simulating only half of the circuit, 8 MOSFET are drived by a single amplifier. In table 3.5 are reported SR and $i_{O,OPAMP}$ simulated values.

	16 MOSFET driving		8 MOSFET driving	
f_p [Hz]	$SR\ [A/\mu s]$	$I_{OPAMP}\ [mA]$	$SR\ [A/\mu s]$	$I_{OPAMP}\ [mA]$
10	no data	6.84	no data	3.45
50	500	38.95	259	20.3
100	1000	70.4	500	35.17
500	4400	381.5	2220	190.6
$1k$	7641	770	3834	382

Table 3.5: SR and i_{OPAMP} for different f_p location. 16 MOSFET driving simulated data and 8 MOSFET driving simulated data.

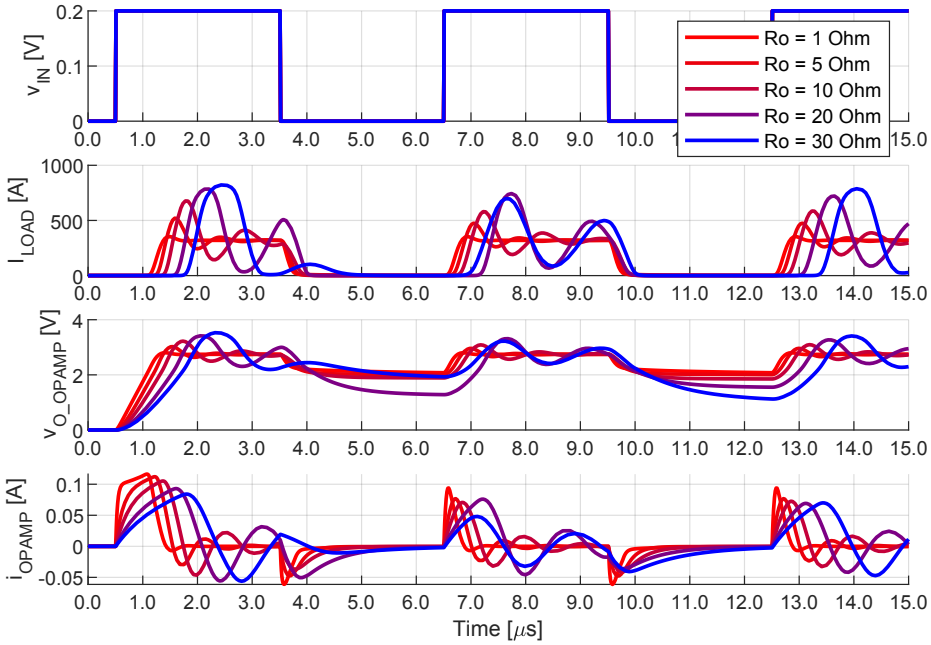


Figure 3.8: Main waveforms, R_o sweep LTspice simulation

Practically all values are halves, but considering the whole circuit is composed by two identical circuits, effective SR is kept identical while current per operational amplifier is halved. This relax the requirements for $i_{O,OPAMP}$. To obtain a minimum value of $SR = 3000A/\mu s$ a minimum pole frequency location is $f_p \simeq 330\,Hz$, with a maximum current $i_{O,OPAMP} = 123\,mA$.

Up to now, operational amplifier output resistance has been considered approximately $R_o \simeq 0\,\Omega$. Now it must be take into account. To simulate the effect of output resistance a little research has been done. Looking on Mouser, typical operational amplifier which can supply at least $100\,mA$ have output resistance in the order of $1\,\Omega \leq R_o \leq 30\,\Omega$. From this information a parametric LTspice simulation has been set up. The circuit is the same of figure 3.3. After the previous analysis, a single operational amplifier drives 8 MOSFETs. In figure 3.8 the input signal v_{IN}, the drained current i_{LOAD}, the output voltage of the amplifier $v_{O,OPAMP}$ and his output current i_{OPAMP} are reported.

These plots demonstrate that relatively high output resistance R_o leads the system to an unstable behavior. This is true for all values except $R_o = 1\,\Omega$, for which the drain current i_{LOAD} overshoot is sustainable. Looking for an operational amplifier with $A \geq 80\,dB$, $GBW \triangleq A \cdot f_p \geq 3.3M\,Hz$, $I_{O,MAX} \geq 125\,mA$, $R_o \leq 1\Omega$, any device was found. This implies that for every operational amplifier a compensation network must be designed to dump these oscillations.

The offset voltage V_{OS} is the last parameter to be addressed. It refers to the input voltage unbalance and affects both static and dynamic behavior

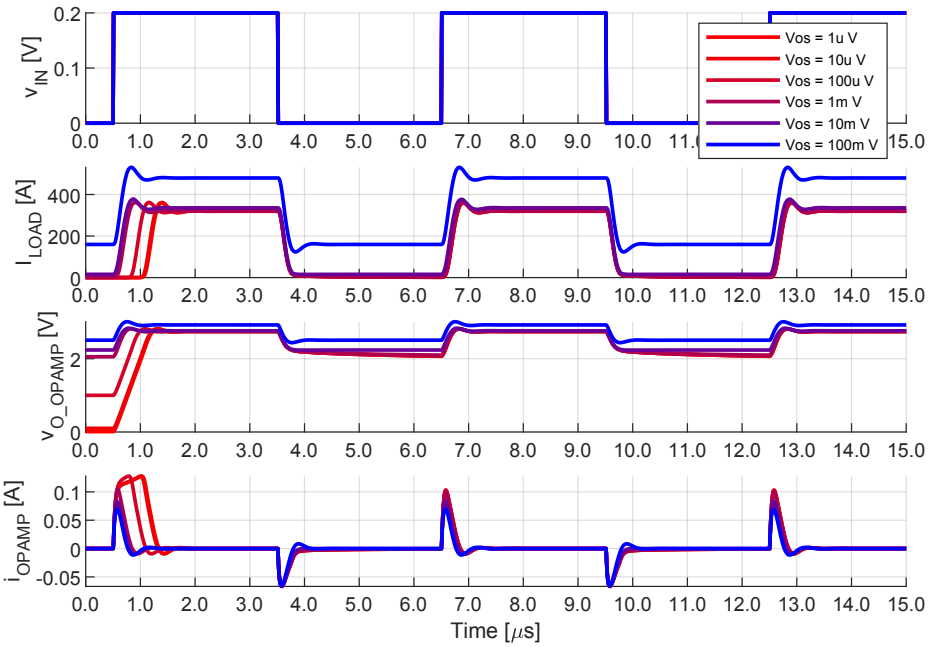


Figure 3.9: Main waveforms, V_{OS} sweep LTspice simulation

of the amplifier. In the circuit in Figure 3.3 the main effect of V_{OS} is the deviation of the nominal current I_{LOAD}. This simulation is set with $A = 80\,dB$, $f_p = 330\,Hz$ and $R_o = 1\,\Omega$ only to see the effect of V_{OS} but avoiding ring behavior. v_{IN} is always the same signal and the reported waveforms are the same. Results are reported in figure 3.9 and table 3.6.

V_{OS} changes, as expected, the nominal current I_{LOAD} and the off time current. As can be seen in 3.6, the offset voltage does not change significantly the nominal current I_{LOAD} and $I_{OFF,min}$ up to $V_{OS} = 100\mu\,V$. Above this threshold, the effect of V_{OS} cannot be neglected. Looking at $v_{O,OPAMP}$, it is possible to notice a different behavior depending on V_{OS}. Above $V_{OS} = 10m\,V$,

V_{OS} $[\mu V]$	I_{LOAD} $[A]$	$I_{OFF,min}$ $[A]$
1	319.57	1.55
10	319.58	1.56
100	319.73	1.65
1k	321.17	2.41
10k	335.56	15.63
100k	479.53	159.59

Table 3.6: Nominal current I_{LOAD} and the off phase minimum current $I_{OFF,min}$ for different values of V_{OS}

the voltage of the MOSFETs V_{GS} is always above the threshold voltage V_t. This means a continuous current drain from the source, v_{IN} only modulates the current value. This is not a desired behavior and, therefore, V_{OS} must be kept below $10m\,V$. Also other factors can be taken into consideration, like the input bias current, but have not significant impact on the system behavior. Specifications are summarized in table 3.7. Looking on Mouser, a suitable operational amplifier has been found. The $LM7171A$ is a very high speed, high output current, voltage feedback amplifier. In table 3.7 the main characteristics are summarized. This is also a very high voltage slew rate

		Specifications	$LM7171A$
Description	Symbol	Value	Value
DC gain	A	$\geq 80\,dB$	$85\,dB$
Gain bandwidth product	GBW	$\geq 3.3M\,Hz$	$160M\,Hz$
Output resistance	R_o	$\leq 30\,\Omega$	$19\,\Omega$
Offset voltage	V_{OS}	$\leq 10m\,V$	$0.2m\,V$
Output current	I_O	$\geq 125m\,A$	$140m\,A$
Power supply voltage	V_{CC}	$\geq 5\,V$	$15\,V$

Table 3.7: Operational amplifier specifications required and $LM7171A$ characteristics

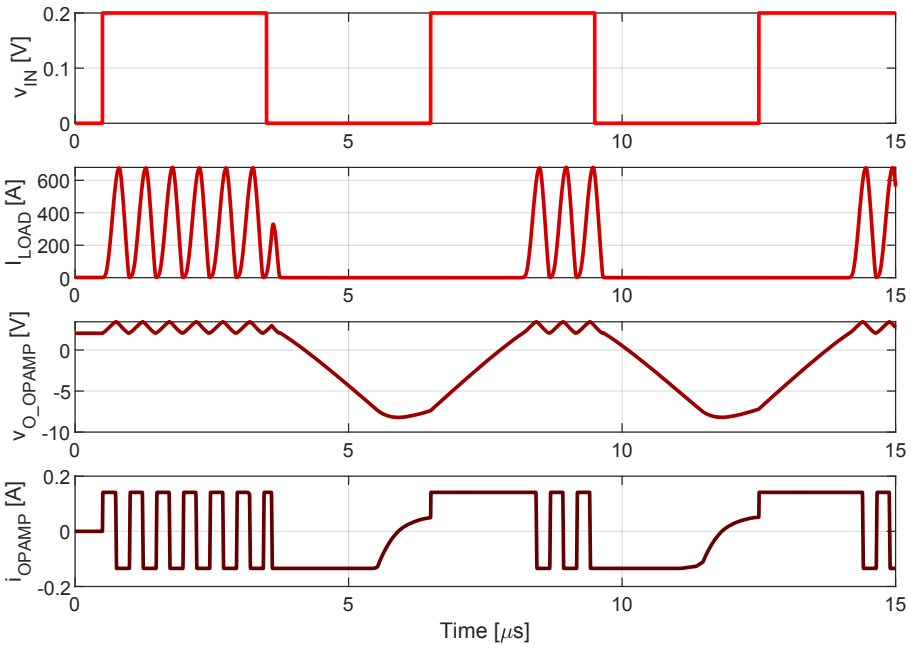


Figure 3.10: LTspice simulation, introduction of $LM7171A$ model

device $SR_V = 4100\,V/\mu s$ if supplied with $15\,V$.

The $LM7171A$ is then imported to LTspice in order to see the system behavior also with this component. The simulation is reported in Fig. 3.10. The input reference signal v_{IN} is the same, but it is clear that the system is not stable for $V_{IN} = 0.2\,V$. This was expected due to $R_o = 19\,\Omega$ and other factors included in $LM7171A$ model. In this configuration, the system is not stable. To visualize where the instability comes from, an AC measure set-up is configured. The goal is to analyze the loop gain T. Looking at Fig. 3.11 it is possible to see a DC generator which imposes the operating point at $V_{IN} = 0.2V$ while an AC generator imposes a $1\,V$ sine wave signal to perturb the system. v_P is the perturbation signal, v_O is the output voltage of the opamp or the controlled variable and v_R is the return signal. In Fig. 3.12

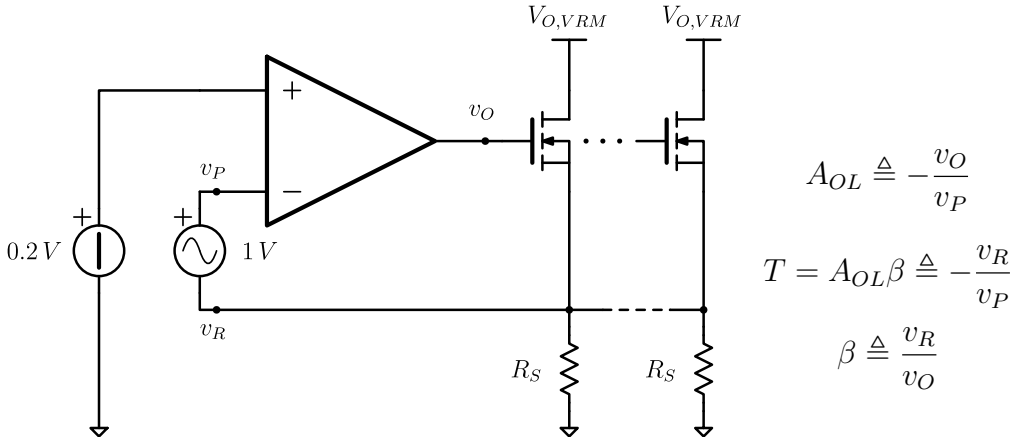


Figure 3.11: Emulator LTspice circuit

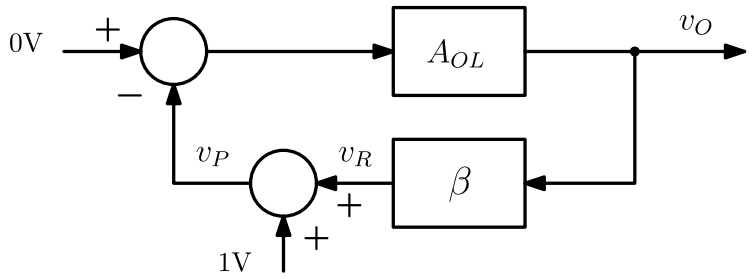


Figure 3.12: Circuit block scheme

is reported the equivalent block scheme. From this, open loop gain A_{OL}, loop gain T and feedback network β are defined. Then an AC simulation has been performed considering model parameter as $A = 80\,dB$, $f_p = 25k\,Hz$, $R_o = 19\,\Omega$ and $V_{OS} = 0.2m\,V$. Simulation is reported in Fig. 3.13. Discrepancies can be highlighted at high frequencies, above $f = 100M\,Hz$. These are probably due to a more complex $LM7171A$ internal model, but will not be investigated. Up to $f = 100M\,Hz$, the model is capable of fully describing the frequency

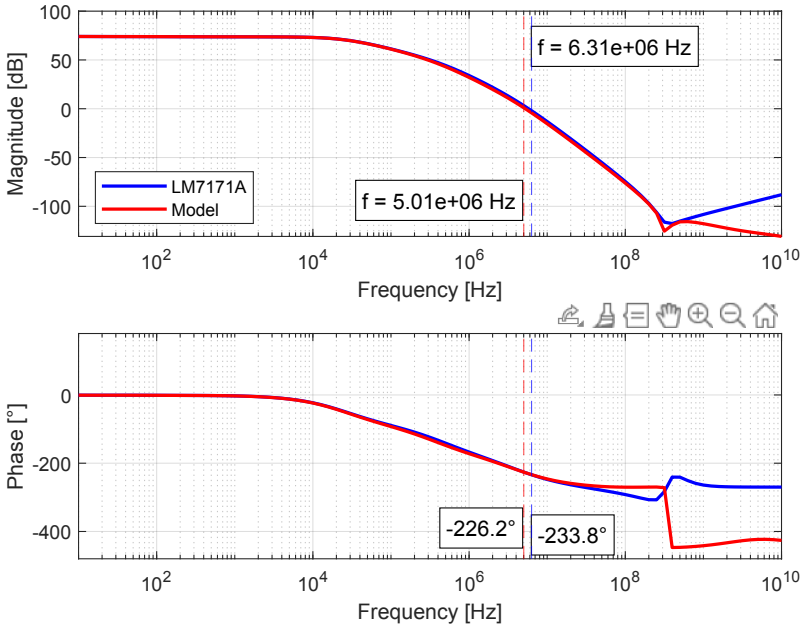


Figure 3.13: Comparison of system open loop transfer function T with operational amplifier model and $LM7171A$. LTspice simulation.

behavior of $LM7171A$. The crossover frequency f_{CR} in the model is slightly smaller respect to the $LM7171A$. As well, the phase is smaller and the phase margin is negative in both cases. The system must be compensated to have a stable response. So two feedback topologies are analyzed.

3.3 First feedback network analysis

Without any compensation network and with reference Fig. 3.11, the transfer functions A_{OL}, β, and T are reported in figure 3.14. To analyze the system, opening and closing ratios are introduced. The opening ratio O_R is defined as the difference between the slope A_{OL} and the slope $1/\beta$ evaluated before the crossover frequency f_{CR}. Similarly, the closing ratio C_R is defined as the difference between the slope $1/\beta$ and the slope A_{OL} evaluated after the crossover frequency f_{CR}. To ensure stability, the opening and closing ratios must be around $-20\,dB/dec$. If the ratios are below $-20\,dB/dec$, then the resulting phase margin will be quite small. In figure 3.14 $|A_{OL}|$ presents 2 poles $(-40\,dB/dec)$ before f_{CR} while $1/\beta$ presents one zero $(+20\,dB/dec)$. Ratios can be evaluated.

$$O_R = SL_{A_{OL}} - SL_\beta \simeq -60\,dB/dec$$

$$C_R = SL_\beta - SL_{A_{OL}} \simeq 60\,dB/dec$$

As expected, the system is not stable. A first compensation inserts a high frequency pole to reduce $1/\beta$. This is done by inserting a series of resistors R_1 and capacitor C_1 between v^- and v_O, as shown in figure 3.20. Placing the pole

around $f^* = 350M\,Hz$, $1/\beta$ can be reduced at high frequency. R_1 and C_1 are two degrees of freedom, so the capacitor is set to $C_1 = 100p\,F$. Then R_1 has been evaluated.

$$R_1 = \frac{1}{2\pi\, f^* C_1} = 4.54\,\Omega \quad \Rightarrow \quad R_1 = 4.7\,\Omega \tag{3.10}$$

C_1 is not a random value, a smaller or bigger value of C_1, like below of $10p\,F$ and above $1n\,F$, does not affect $|1/\beta|$. This because eq:3.10 is not more valid. The result are reported in figure 3.15. This compensation does not affect the behavior around the crossover frequency f_{CR} too much but helps to reduce $1/\beta$ for high frequencies. The next compensation involves a capacitor C_2 in parallel to the series of R_1 and C_1. This creates a unity gain buffer configuration at high frequencies introducing another pole into $1/\beta$. This is possible if the impedance of C_2 is small enough, less than $Z^* = 1m\,\Omega$. The corner frequency for which the unity gain buffer works is chosen as $f^* = 1G\,Hz$ as an initial value. Then the value of C can be evaluated.

$$C_2 = \frac{1}{2\pi Z^* f^*} = 159n\,F \quad \Rightarrow \quad C_2 = 150n\,F \tag{3.11}$$

Fig. 3.16 shows that $1/\beta$ goes to $0dB$ for frequencies above $1G\,Hz$. However, O_R and C_R are still equal to $\mp 60\,dB/dec$, and the phase margin is also still negative. The idea is to have O_R and C_R equal to $\mp 20\,dB/dec$. Due to the fact $1/\beta(0) \geq 0\,dB$, a pole-zero behavior in $1/\beta$ can achieve that goal. A suitable resistor R_2 and a capacitor C_3 can be involved to obtain this behavior. As

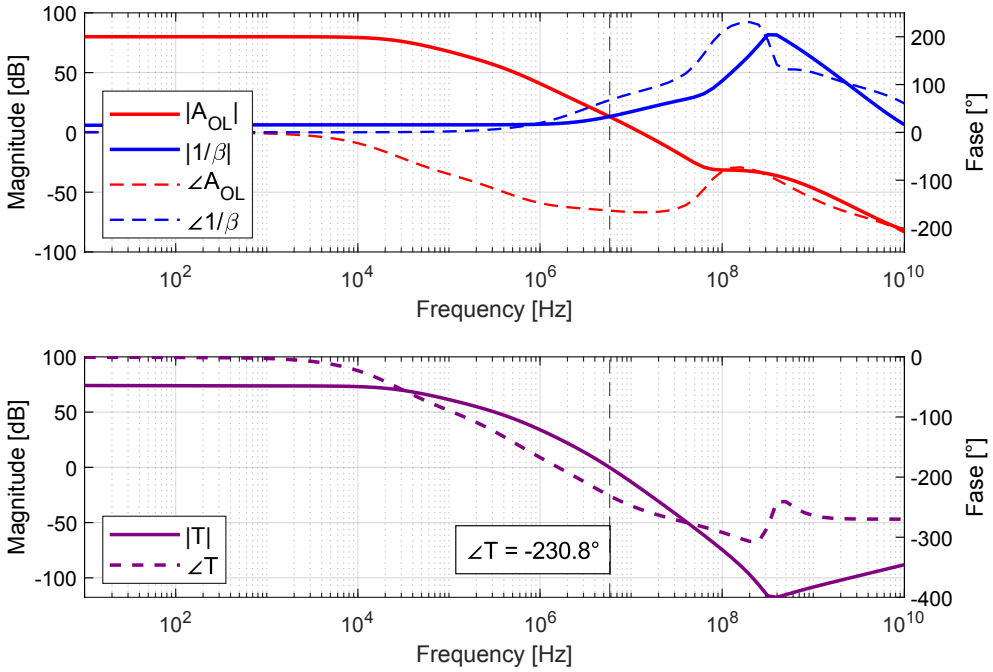


Figure 3.14: LTspice AC simulation of A_{OL}, β, and T with no compensation

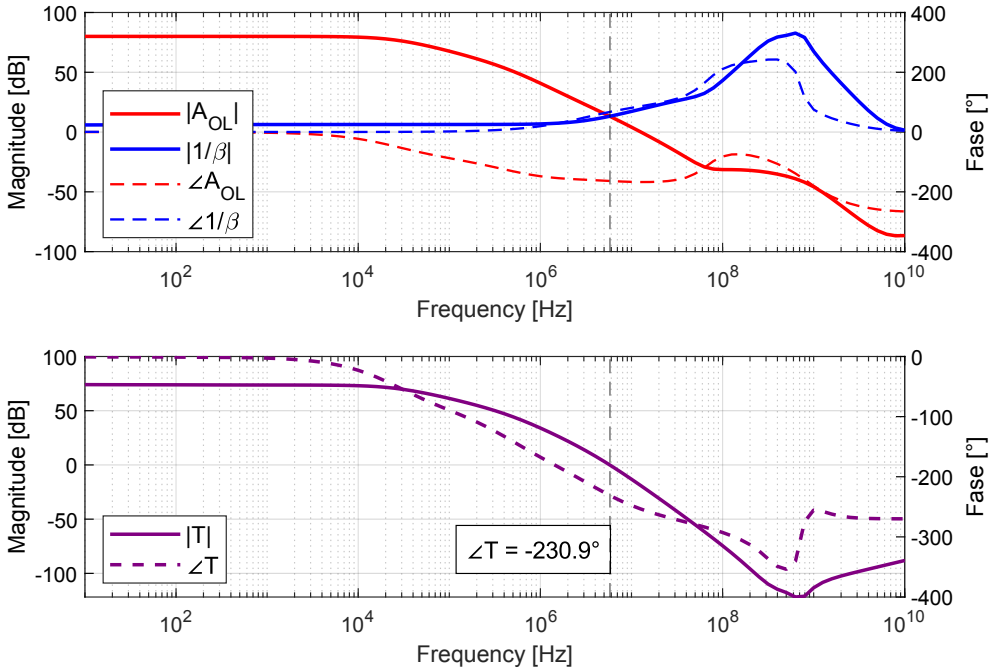


Figure 3.15: LTspice AC simulation of A_{OL}, β, and T with R_1, C_1 compensation

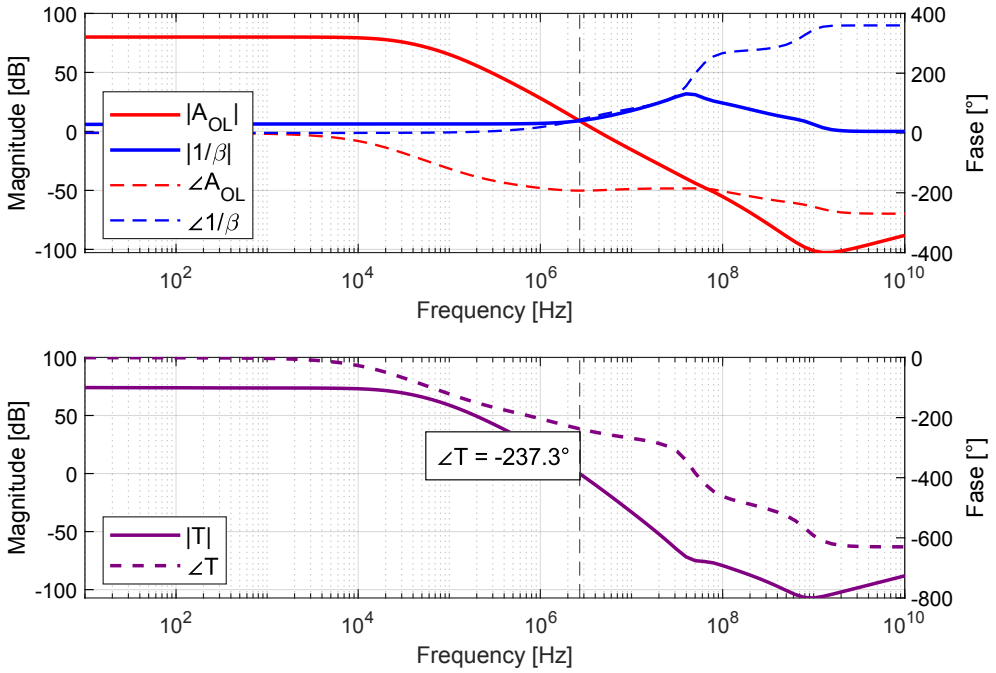


Figure 3.16: LTspice AC simulation of A_{OL}, β, and T with R_1, C_1, C_2 compensation

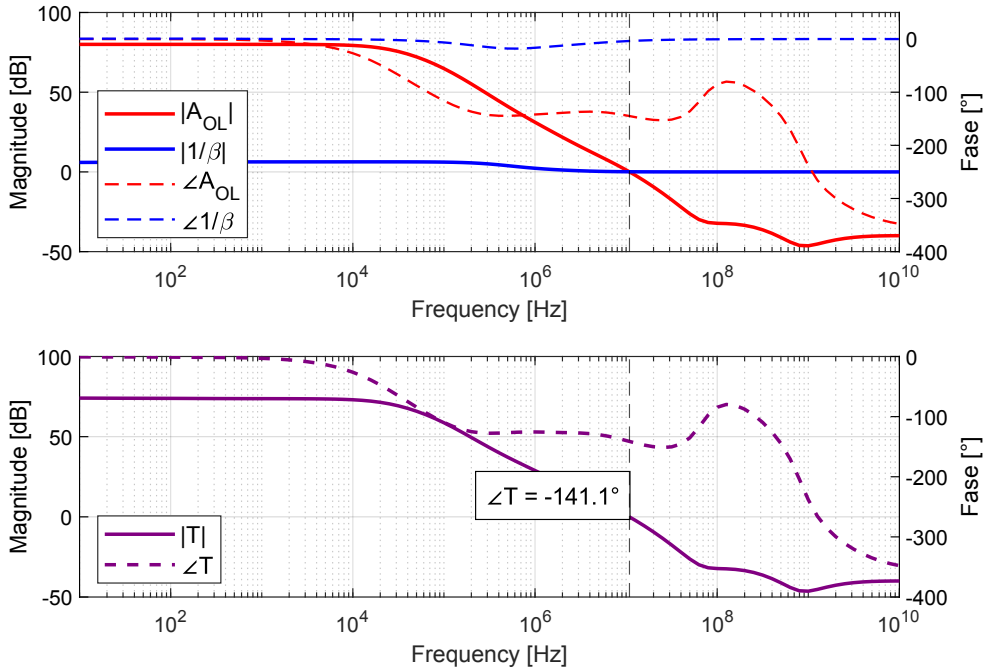


Figure 3.17: LTspice AC simulation of A_{OL}, β, and T with R_1, C_1, C_2, R_2, C_3 compensation

before, with 2 degrees of freedom, $C_3 = 100pF$ is imposed. To select the suitable value for R_2, a sweep between $0.1\,\Omega \leq R_2 \leq 10\,\Omega$ has been performed. Outside of this range, the effect of R_2 and C_3 compensation is negligible. Then $R_2 = 1.5\,\Omega$ has been chosen and simulation has been performed.

In Fig. 3.17 the $1/\beta$ magnitude presents only a zero and a pole. The zero is also present in the magnitude A_{OL} due to the load effect at the output of the operational amplifier. This zero effect increases the A_{OL} phase, resulting in 38.9° phase margin. The crossing frequency is close to a pole in A_{OL}, leading to an approximate $O_R = -20\,dB/dec$ and $C_R = 40\,dB/dec$. However, the system is stable with a low phase margin. Then, by slight adjustment of C_2 and C_3, a better phase margin can be obtained. To have the best slew rate possible, the phase margin cannot be greater than 50°. A too stable system will not reach the desired SR. The definitive values for the feedback network are reported in Table 3.8. AC simulation is reported in Fig. 3.18 and the transient simulation in Fig. 3.19. The transient behavior shows that the system is stable. The current i_{LOAD} settles to $I_{LOAD} = 321.1\,A$ as expected with an overshoot of $37.6\,A$ which is considered acceptable to obtain the desired slew rate. The slew rate achieved according to definition 1 is $SR_1 = 1983\,A/\mu s$, and with definition 2 is $SR_2 = 1332\,A/\mu s$. This results in a total of $SR_1 = 3966\,A/\mu s$ and $SR_2 = 2664\,A/\mu s$ when the 2 stages works together. The current $i_{O,OPAMP}$ saturates at the maximum value $I_{O,MAX}$ due to the high frequency position of $f_{p,1}$. The value of $v_{O,OPAMP}(t = 0) = 2.12\,V$, this is probably due to the offset voltage of $LM7171A$. The offset voltage V_{OS} could also cause the

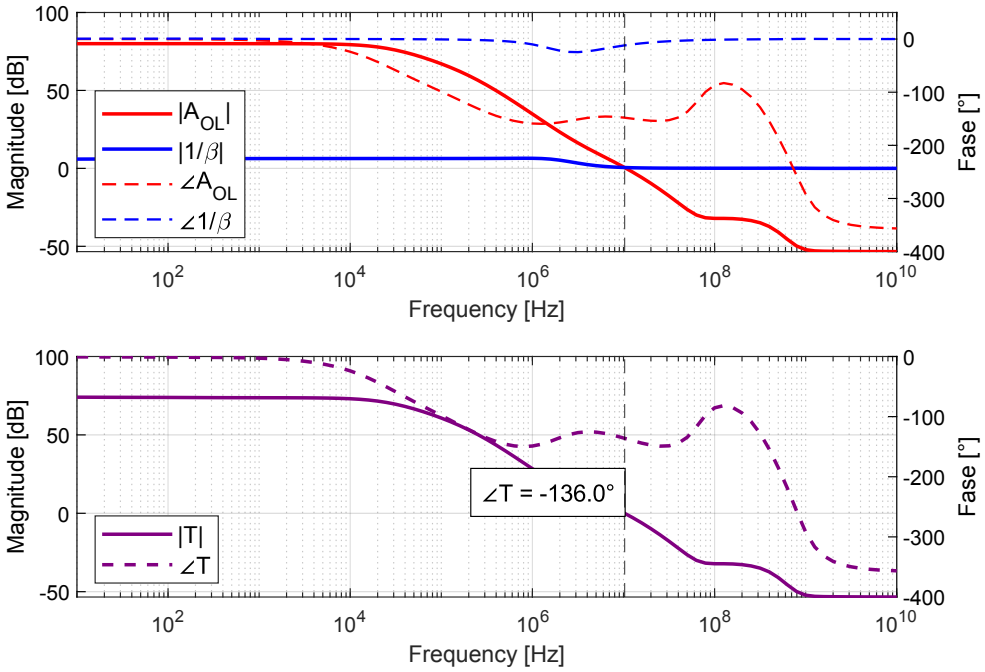


Figure 3.18: LTspice AC simulation of A_{OL}, β, and T with adjusted R_1, C_1, C_2, R_2, C_3 compensation

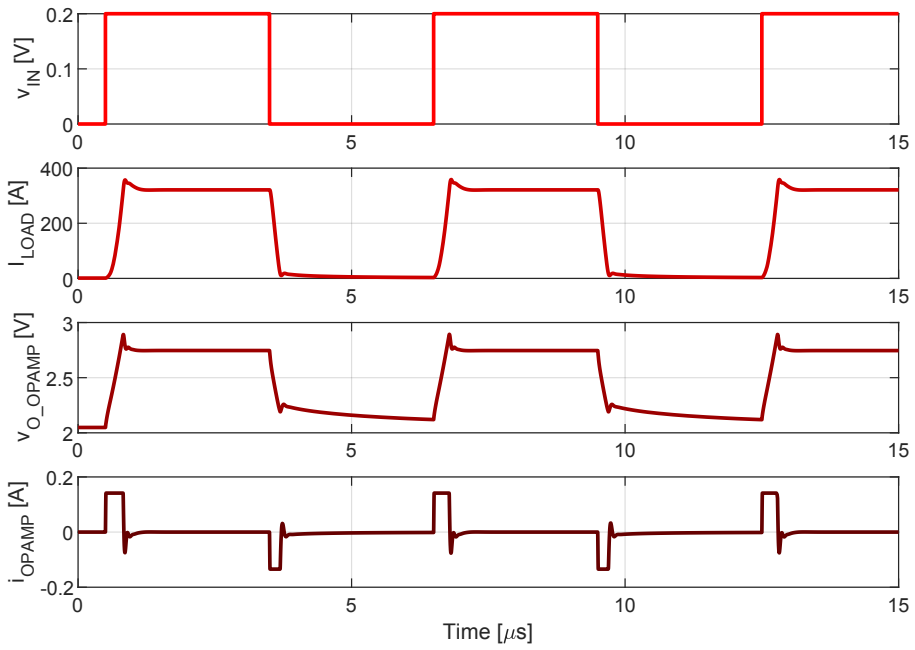


Figure 3.19: LTspice transient simulation of v_{IN}, i_{LOAD}, $v_{O,OPAMP}$ and i_{OPAMP} with adjusted compensation

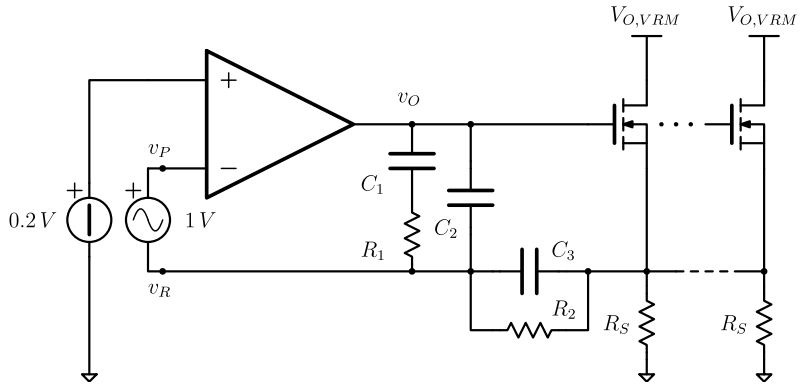


Figure 3.20: First compensation network

$I_{OFF,min} = 3.63\,A$. This is also considered acceptable because all MOSFETs are not conducting when $v_{IN} = 0\,V$. The compensation network is reported in Fig. 3.20.

Component	R_1	R_2	C_1	C_2	C_3
Value	$4.7\,\Omega$	$1.5\,\Omega$	$100p\,F$	$47n\,F$	$470p\,F$

Table 3.8: First compensation network parameters

3.4 Second feedback network analysis

In order to have a slightly higher slew rate SR_2 and satisfy specifications, another feedback topology has been studied. With reference to Fig. 3.11 and Fig. 3.14 stability must also be ensured in that case. To do so, the input capacitance of the MOSFET is the subject of this discussion. First, from the MOSFET small signal model, a two-port model is derived. Consider the MOSFET small signal model that involves C_{gs}, C_{gd}, C_{ds}, g_m and r_o.

$$\begin{cases} i_o = G\,v_{gs} + \frac{1}{Z_o} v_{ds} \\ i_g = \frac{1}{Z_i} v_{gs} + G^*\,v_{ds} \end{cases}$$

$$Z_i \triangleq \left.\frac{v_{gs}}{i_g}\right|_{v_{ds}=0} = \frac{v_{gs}}{s(C_{gs}+C_{gd})v_{gs}} = \frac{1}{sC_{iss}}$$

$$G \triangleq \left.\frac{i_o}{v_{gs}}\right|_{v_{ds}=0} = g_m + sC_{gd} = g_m\left(1 + s\frac{C_{gd}}{g_m}\right)$$

$$Z_o \triangleq \left.\frac{v_{ds}}{i_o}\right|_{v_{gs}=0} = r_o // \frac{1}{s(C_{gd}+C_{ds)}} = r_o // \frac{1}{sC_{oss}} = \frac{r_o}{1+sr_oC_{oss}}$$

$$G^* \triangleq \left.\frac{i_g}{v_{ds}}\right|_{v_{gs}=0} = -\frac{sC_{gd}v_{ds}}{v_{ds}} = -sC_{gd}$$

In this model, the input impedance is purely capacitive and depends on $C_{iss} = C_{gs} + C_{gd}$, which is called the input capacitance. Datasheet of the MOSFET report the value for input capacitance as a function of V_{DS}. In that case $V_{DS} \leq 1, V$ than $C_{iss} \simeq 4000p\,F$. Considering that 8 MOSFETs are connected in parallel, the new input capacitance becomes $Z_i^* = 8C_{iss} \simeq 32n\,F$. The equivalent scheme to analyze is reported in figure 3.21. Considering the

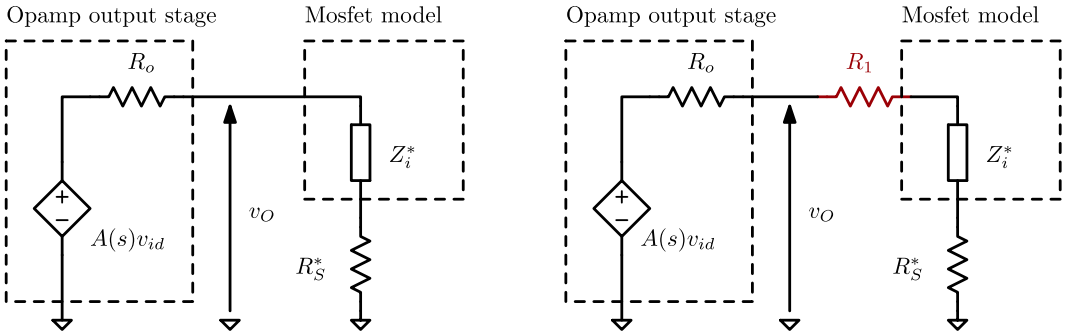


Figure 3.21: Simplified equivalent operational amplifier loading circuit with and without R_1

output equivalent model of the operational amplifier and the MOSFET model neglecting G, Z_o, G^* it is possible to evaluate the effect on the output voltage of the operational amplifier $v_{O,OPAMP}$ by applying the voltage divider equation. Resistance $R_S^* = R_S/8 = 625\mu\,\Omega$, parallel combinations of 8 shunt resistors.

$$\begin{aligned} v_{O,OPAMP} &= \frac{Z_i^* + R_S^*}{R_o + Z_i^* + R_S^*} A(s) v_{id} \\ &= \frac{1 + sR_S^*\,8C_{iss}}{1 + s(R_o + R_S^*)\,8C_{iss}} A(s) v_{id} \\ &= \frac{1 + \omega/\omega_{z,LOAD}}{1 + \omega/\omega_{p,LOAD}} \frac{A_0(1 - \omega/\omega_z)}{(1 + \omega/\omega_{p,1})(1 + \omega/\omega_{p,2})} v_{id} \end{aligned} \tag{3.12}$$

$A(s)$ is the gain of the operational amplifier and is dependent on the frequency. $LM7171A$ model includes 2 poles and an unstable zero. $\omega_{p,1} = 2\pi f_{p,1} \simeq 2\pi\,20k\,Hz$, $\omega_{p,2} = 2\pi f_{p,2} \simeq 2\pi\,200M\,Hz$ and $\omega_z = 2\pi f_z \simeq 2\pi\,10G\,Hz$. These poles and zero values are present in the $LM7171A$ LTspice model, they are not reported in datasheet and can be measured by simulating the AC response. Eq. 3.12 presents a pole at $f_{p,LOAD}$ and a zero in $f'_{z,LOAD}$.

$$f_{p,LOAD} = \frac{1}{2\pi(R_o + R_S^*)\,8C_{iss}} \simeq \frac{1}{2\pi R_o\,8C_{iss}} = 261.7k\,Hz \tag{3.13}$$

$$f_{z,LOAD} = \frac{1}{2\pi R_S^*\,8C_{iss}} = 7.95G\,Hz \tag{3.14}$$

On Fig.3.14 the crossover frequency is $f_{CR} \simeq 5.9M\,Hz$. This means that both $f_{p,1}$ and $f_{p,LOAD}$ lead to a poor phase margin at the crossover frequency. The idea is to insert an isolation resistor R_1 to lower the location of $f_{z,LOAD}$ and so increase the phase margin. To mitigate the effect of $f_{p,LOAD}$, $f_{z,LOAD}$ is set to the crossover frequency $f_{CR} = 5.9M\,Hz$. An assumption is made, R_1 must be at least ten times grater than R_S^* and at least ten times smaller than R_o.

$$\begin{aligned} v'_{O,OPAMP} &= \frac{R_1 + Z_i^* + R_S^*}{R_o + R_1 + Z_i^* + R_S^*} A(s) v_{id} \\ &= \frac{1 + s(R_1 + R_S^*)\,8C_{iss}}{1 + s(R_o + R_1 + R_S^*)\,8C_{iss}} A(s) v_{id} \\ &= \frac{1 + \omega/\omega_{z,LOAD}}{1 + \omega/\omega_{p,LOAD}} \frac{A_0(1 - \omega/\omega_z)}{(1 + \omega/\omega_{p,1})(1 + \omega/\omega_{p,2})} v_{id} \end{aligned} \tag{3.15}$$

$$f'_{p,LOAD} = \frac{1}{2\pi(R_o + R_1 + R_S^*)\,8C_{iss}} \simeq \frac{1}{2\pi R_o\,8C_{iss}} \tag{3.16}$$

$$f'_{z,LOAD} = \frac{1}{2\pi(R_1 + R_S)\,8C_{iss}} \simeq \frac{1}{2\pi R_1\,8C_{iss}} \tag{3.17}$$

$$R_1 = \frac{1}{2\pi f_{CR}\,8C_{iss}} = 0.843\Omega \quad \Rightarrow \quad R_1 = 0.82\,\Omega \tag{3.18}$$

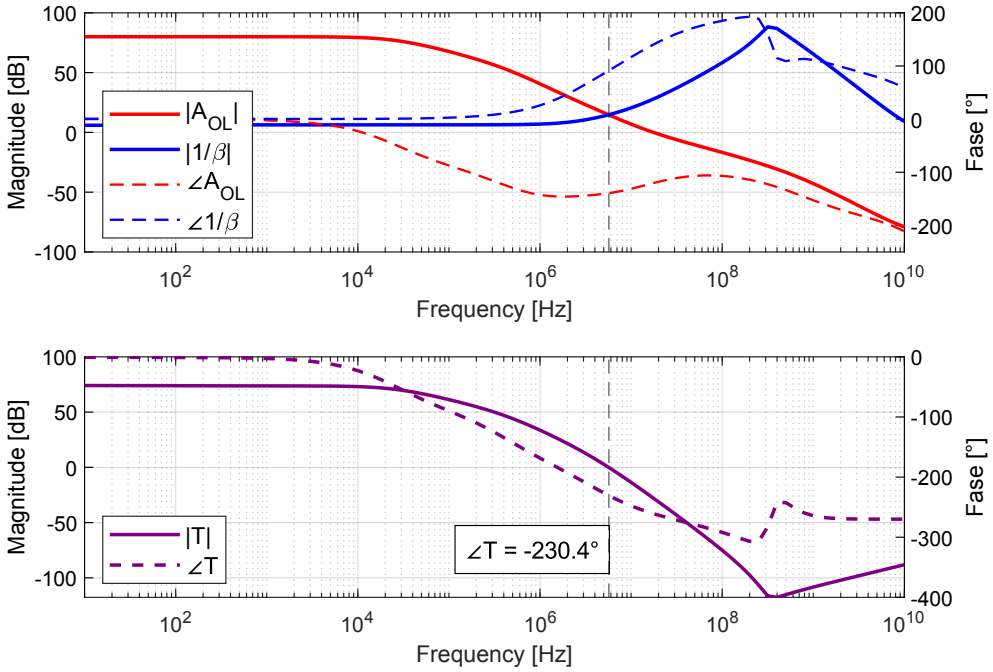


Figure 3.22: LTspice AC simulation of A_{OL}, β, and T with R_1 compensation

The value of R_1 satisfies the hypothesis made initially. Simulation with only R_1 compensation is reported in Fig.3.22.

$|A_{OL}|$ now has a zero around the crossover frequency f_{CR} but also $|1/\beta|$ presents the same zero. Thus, provide the same phase margin as without compensation. Now it is possible to add the same compensation as in the previous topology by inserting a capacitor C_1 between v^- and v_O. By imposing $1/\beta$ on $0\,dB$ at high frequencies, a decreasing behavior of $1/\beta$ will be created. C_1 create a pole f_p^* in the $1/\beta$. That pole should be placed around $f_p^* = 40M\,Hz$ to mitigate the effect of the 2 zeros.

$$C_1 = \frac{1}{2\pi R_1 f_p^*} = 4.85n\,F \quad \Rightarrow \quad C_1 = 4.7n\,F \tag{3.19}$$

C_1 alone is not capable of stabilizing the system. This is due to the interaction between MOSFETs and two different loops. The first loop is the one that passes through the $LM7171A$, the other one interacts with C_1. To avoid this, another isolation resistor R_2 is placed between the MOSFETs source and v_O. The value of R_2 is sweep between $0.1\,\Omega$ and $100\,\Omega$. The optimal value is set to $R_2 = 10\,\Omega$ to obtain a good phase margin. By adding R_2, the new pole location is due to R_2 and C_1. This because R_2 is quite bigger than R_1. The simulation results are reported in Fig.3.23.

In Fig.3.23 now it is possible to see various contributions. The zero introduced by R_1 and C_{iss}, which is present in both A_{OL} and β. The pole due to C_1 and R_2 is present only in $1/\beta$.

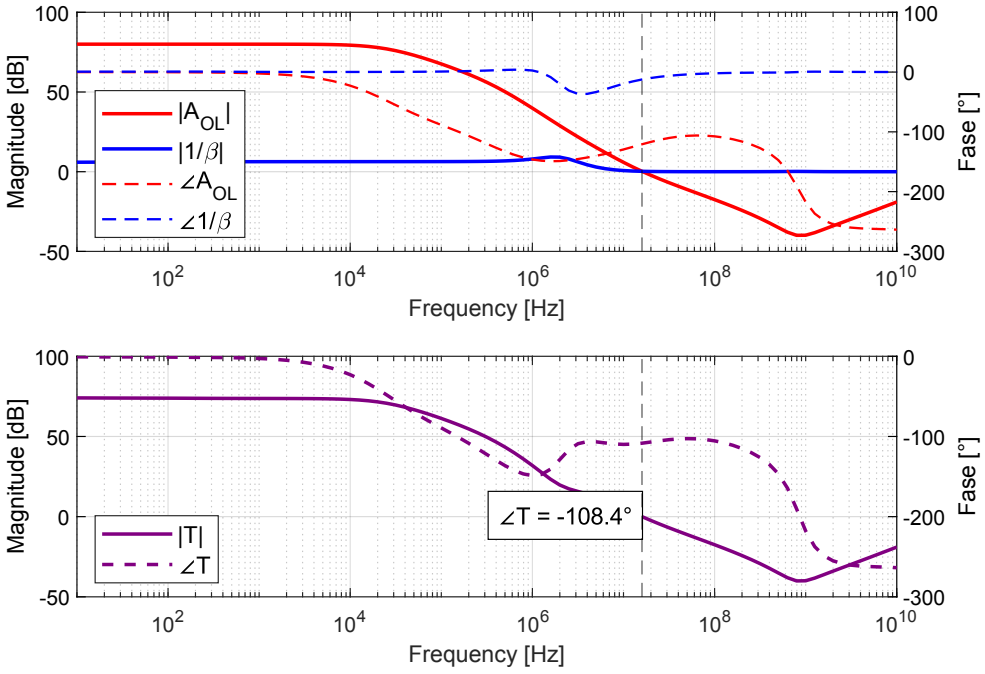


Figure 3.23: LTspice AC simulation of A_{OL}, β, and T with R_1, C_1, R_2 compensation

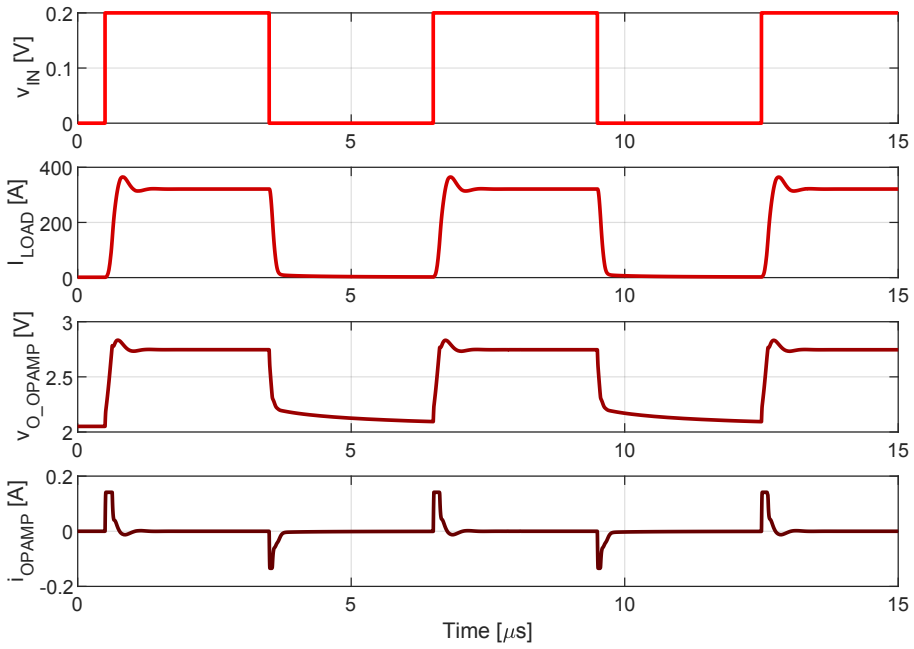


Figure 3.24: LTspice transient simulation of v_{IN}, i_{LOAD}, $v_{O,OPAMP}$ and i_{OPAMP} with adjusted R_1, C_1, R_2 compensation

With R_1, C_1 and R_2, the time response is stable but does not reach a very high slew rate. To increase it, little adjustment on R_1 helps regulate the phase margin and stability. Compensation network values are reported in table 3.9. The compensation network is reported in Fig. 3.25.

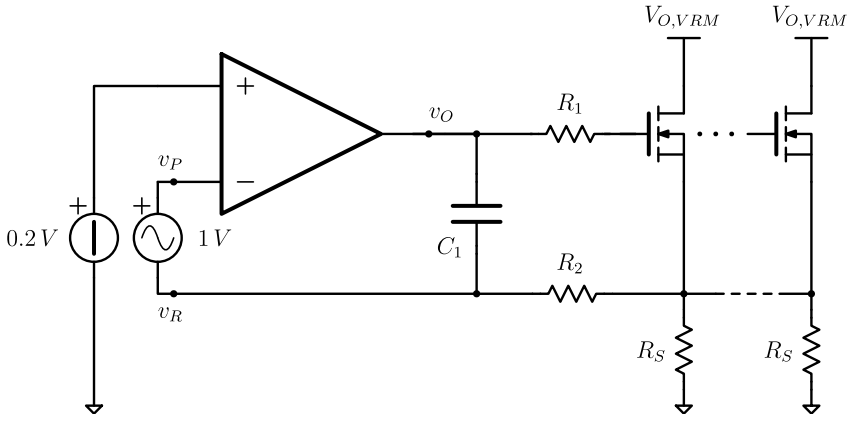


Figure 3.25: Second compensation network

Component	R_1	R_2	C_1
Value	$0.68\,\Omega$	$10\,\Omega$	$4.7n\,F$

Table 3.9: Second compensation network parameters

Time response is reported in Fig. 3.24. The current i_{LOAD} settles to $I_{LOAD} = 321.1\,A$ as expected with an overshoot of $42.9\,A$ which is considered acceptable to obtain the desired slew rate. The value of $v_{O,OPAMP}(t = 0) = 2.05\,V$, this is probably due to the offset voltage of $LM7171A$. The offset voltage V_{OS} could also cause $I_{OFF,min} = 2.25\,A$. This is the same behavior as in the previous compensation network. This means that also in that case V_{OS} is should be compensated for having a more ideal behavior. The slew rate achieved according to definition 1 is $SR_1 = 2665\,A/\mu s$ and according to definition 2 is $SR_2 = 1783\,A/\mu s$ for a single stage. This results in a total of $SR_1 = 5328\,A/\mu s$ and $SR_2 = 3566\,A/\mu s$ when both stages work together. Again, the current $i_{O,OPAMP}$ saturates at the maximum value $I_{O,MAX}$ due to the high frequency position of $f_{p,1}$. But in that configuration, the saturation time is lower, due to the higher SR.

4 Active load measurements and validation

This chapter presents the experimental tests conducted in the laboratory, the primary objective of which is to evaluate the behavior of the load emulator, assess its performance, and compare the experimental results with the theoretical predictions.

4.1 Board and setup description

The top and bottom views of the load emulator board are reported in Fig.4.1 and 4.2. MOSFET and shunt resistors are soldered in the top layer, as can

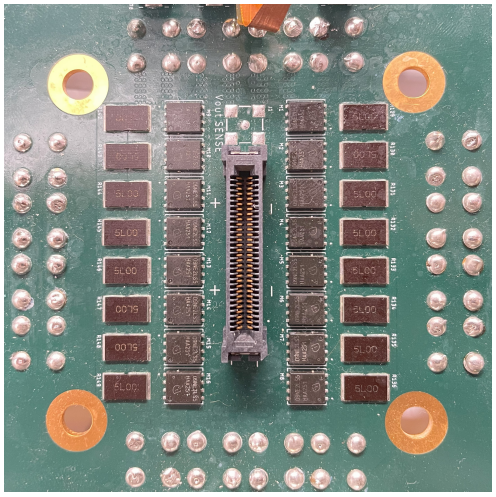


Figure 4.1: Emulator board top view

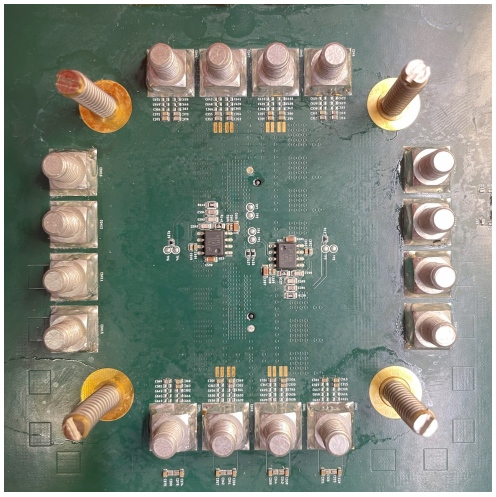


Figure 4.2: Emulator board bottom view

be seen in Fig.4.1. Instead the operational amplifiers and feedback network components are placed in the bottom as shown in Fig.4.2. The central socket can be used to plug other loads to the board. The emulator circuit is inserted on the same VRM board. The screws on the four sides are used to insert capacity banks, to modify the output filter capacitor of the VRM. The VRM used is not capable of testing the emulator at the best performance $I_{LOAD} = 640\,A$. VRM in fact, is a parallel project, still in evolution. This means that tests can be performed only with a nominal current of $I_{LOAD} = 40\,A$. To verify the correct operation of the emulator, 4 different signals are taken from the board. First, the load current i_{LOAD} is sensed across the parallel shunt resistor through two $100\,\Omega$ resistors, as reported in Fig.4.3. In this model input operational

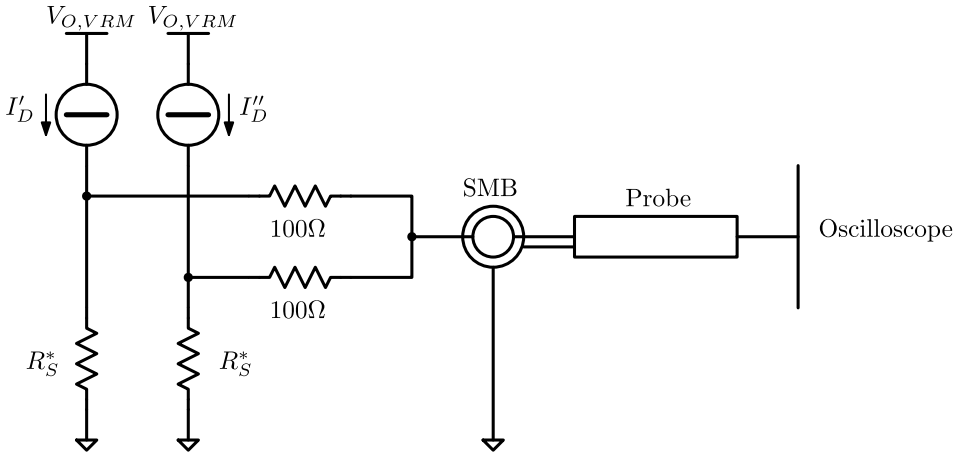


Figure 4.3: Current measure setup

amplifier impedance, as well as the feedback network, are neglected. In this way, the voltage $V_{R^*_S}$ can be sensed. Then to visualize the real of the load current i_{LOAD} a multiplication factor must be added. This coefficient can be derived by applying the superposition effect.

$$v'_{R^*_S} = I'_D \frac{200\Omega \cdot R^*_S}{200\Omega + 2R^*_S} \simeq I'_D R^*_S \qquad v''_{R^*_S} \simeq I''_D R^*_S$$

$$\begin{aligned} v_{BNC} &= \frac{100\Omega + R^*_S}{200\Omega + R^*_S} v'_{R^*_S} + \frac{100\Omega + R^*_S}{200\Omega + R^*_S} v''_{R^*_S} \\ &\simeq \frac{1}{2}(v'_{R^*_S} + v''_{R^*_S}) = \frac{R^*_S}{2}(I'_D + I''_D) = \frac{R^*_S}{2} i_{LOAD} \end{aligned}$$

$$k_A \triangleq \frac{2}{R^*_S} \qquad i_{LOAD} = k_A v_{SMB} \tag{4.1}$$

The coefficient $k_A = 3200\,S$ is used on the oscilloscope to see the current waveform. The next signals are the output voltage of the VRM $v_{O,VRM}$ and the input and output voltage of the amplifier v_{IN}. These are taken by a probe thanks to the SMB connector placed on the board. The output voltage of the output amplifier v_O is taken with a probe. In that case, no SMB connector is present. The operating amplifier output current i_{OPAMP} is not accessible and no measure configuration can be realized to measure it.

Since the second feedback topology has been studied after the realization of the board, the second topology cannot be tested. In order to compare the results between the simulation and the physical measurements, another simulation with $I_{LOAD} = 40\,A$ is performed. The amplitude of the input signal is $v_{IN} = 0.0125\,V$. Also, the on-time changes $t_{on} = 250\,\mu s$ to be comparable. The simulation of a single branch is reported in Fig.4.4.

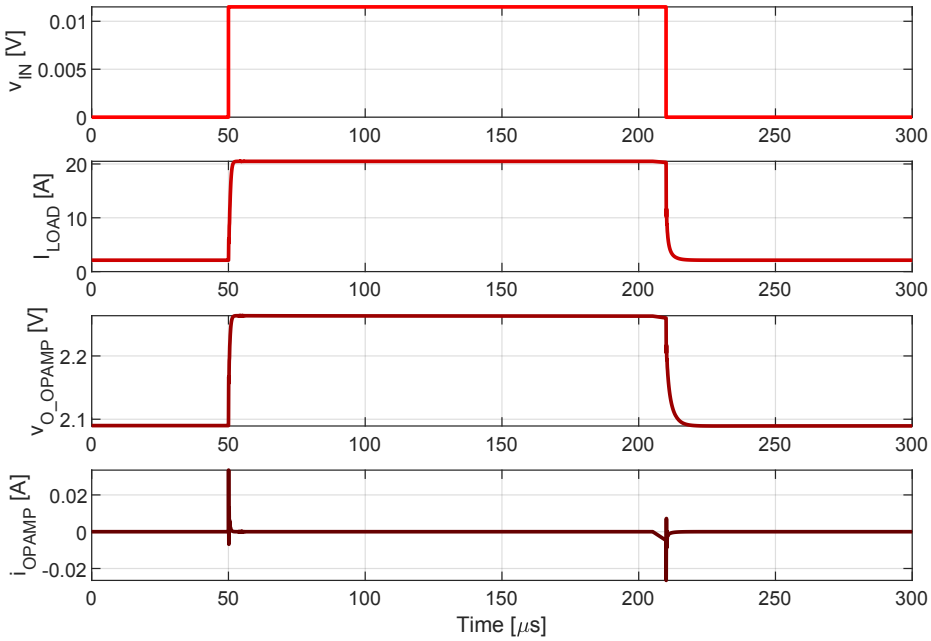


Figure 4.4: Feedback network 1 LTspice simulation with $I_{LOAD} = 40\,A$

The slew rate achievable in these conditions is $SR_1 = 17.6\,A/\mu s$ and $SR_2 = 13.9\,A/\mu s$. The voltage $v_{O,OPAMP}(t = 0) = 2.09\,V$ and produces a load current of $2.11\,A$. The opamp current i_{OPAMP} does not saturate in that case. This is due to the slow response required for that current step, which is lower than $I_{LOAD} = 640\,A$.

4.2 Simulation and measurements comparison

In this section are reported measures and data from the experimental testing. In Fig.4.5 are reported the operational amplifier input and output voltage v_{IN} $v_{O,OPAMP}$, the VRM voltage $v_{O,VRM}$ and the VRM output current i_{LOAD}.

Several discrepancies can be observed between the simulation in Fig.4.4 and measurements in Fig.4.5. The most significant concerning the output voltage of the operational amplifier, $v_{O,OPAMP}$. When $v_{IN} = 0$, the $v_{O,OPAMP}$ voltage settles at the negative power rail of the operational amplifier. This behavior is likely attributable to the amplifier offset voltage V_{OS}. Specifically, if V_{OS} is negative, then $v^+ = v_{IN} + V_{OS} = 0 + V_{OS} < 0\,V$. This condition holds even for very small negative values of V_{OS}. Consequently, the operational amplifier attempts to impose an output voltage $v_{O,OPAMP}$ such that $v^- = v^+ < 0\,V$. However, v^- cannot assume negative values because I_{LOAD} is always positive. As a result, $v_{O,OPAMP}$ is driven to its minimum possible value, the negative supply rail, approximately $V_{CC} = -15\,V + V_P$, where V_P represents a voltage drop due to device polarization.

The main consequence of this effect is the introduction of a delay time,

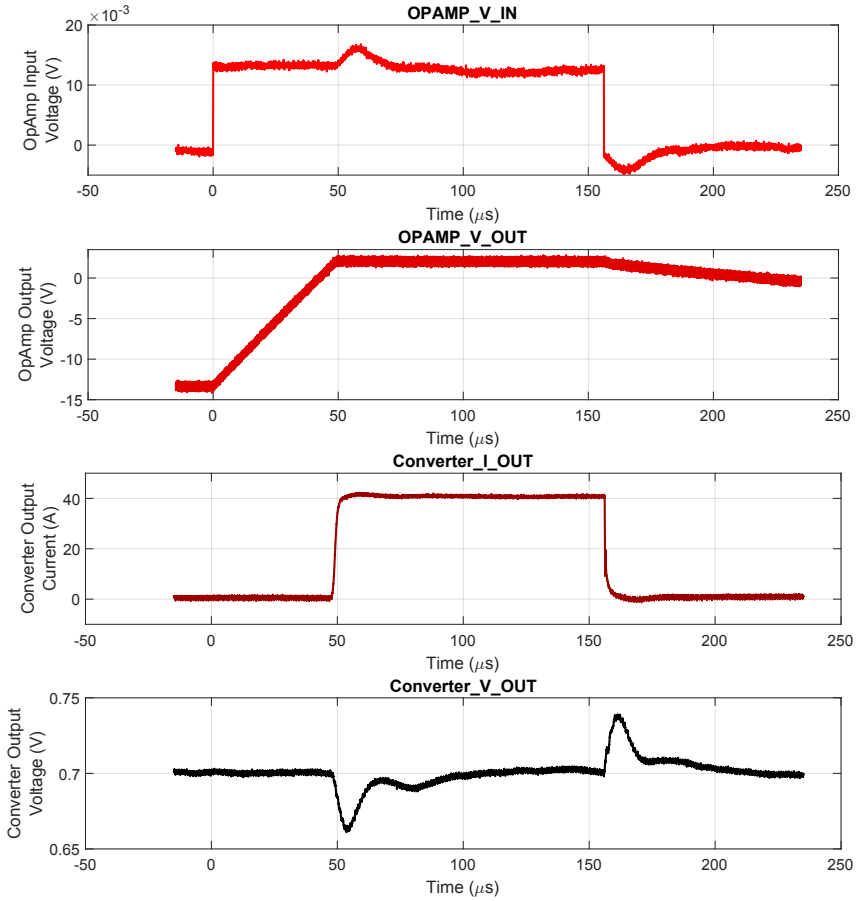


Figure 4.5: Emulator experimental measurements

$t_D \simeq 50\,\mu s$, between v_{IN} and i_{LOAD}. While this delay is not critical if only the nominal current I_{LOAD} and its slew rate SR are of interest, it prevents the circuit from achieving smaller values of t_{on}. Furthermore, during the on-time, the influence of V_{OS} can again be observed: $v_{O,OPAMP} = 2.056\,V$, which is lower than the simulated value of $v_{O,OPAMP} = 2.26\,V$. This discrepancy further suggests the presence of a negative offset voltage.

Additionally, analysis of the input signal v_{IN} reveals both an upward and downward peaking around the I_{LOAD} step edges. This phenomenon is attributable to the VRM output voltage $v_{O,VRM}$. The input signal source compensates for variations in v^-, resulting in small peaks in i_{LOAD} that, although barely visible in Fig. 4.5. Nevertheless dynamic performance of the emulator

	SR_1 $[A/\mu s]$	SR_2 $[A/\mu s]$
Simulated	35.24	13.92
Measured	21.73	10.34

Table 4.1: Operational amplifier specifications required and $LM7171A$ characteristics

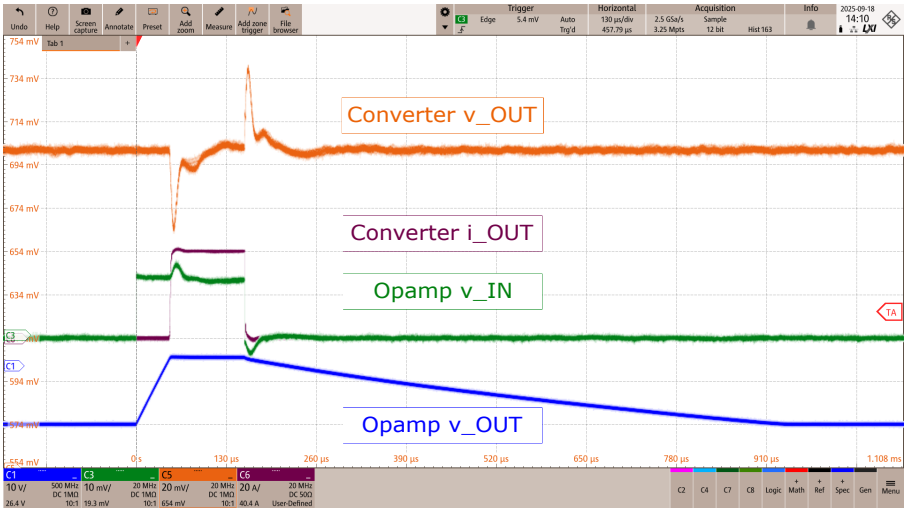


Figure 4.6: Oscilloscope picture, focus on transient

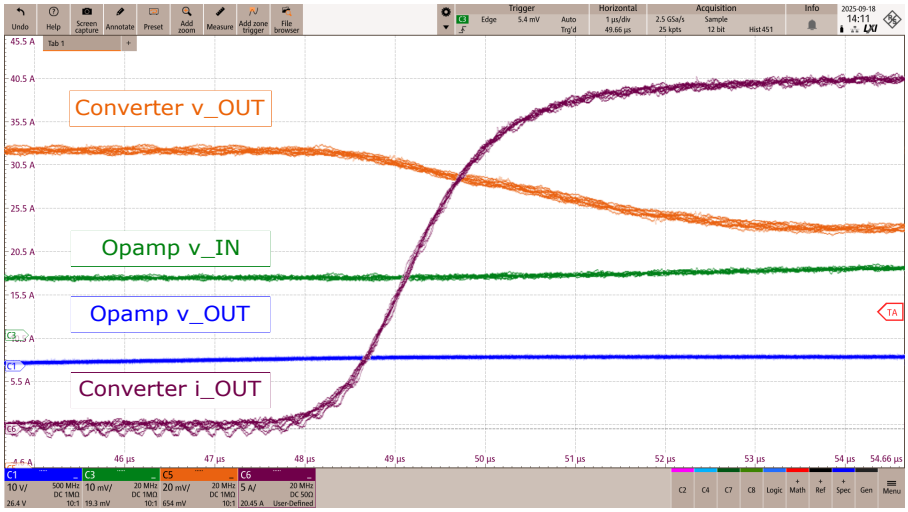


Figure 4.7: Oscilloscope picture, focus on current slew rate

can be analyzed. The nominal current I_{LOAD} settles around 41 A as expected. The measured slew rate is reported in table 4.1.

Both measured slew rates are lower than the simulated values. In the case of SR_1, the discrepancy is not negligible; however, it is primarily related to the definition of SR. The maximum derivative is highly sensitive to the waveform shape, which can vary from cycle to cycle, producing different results even within the same circuit. Another contributing factor is the non-idealities of the LTspice model. The second definition is more conservative, and in this case the results are more consistent. Therefore, it is likely that the observed discrepancy is mainly attributable to limitations in the LTspice model. In addition, these discrepancies on SR can be due to the operational amplifier

output current i_{OPAMP}. In the simulation, the current does not saturate, it reaches a maximum value of $34.28m\,A$. Instead, looking at the linear behavior of $v_{O,OAPMP}$ in Fig. 4.5, can lead to a hypothesis. This linear behavior suggests a saturation of i_{OPAMP}. When the output current saturates, the response time slows down. This could be a possible cause of lower SR values. Finally, two oscilloscope waveforms are reported in Fig. 4.7 and Fig. 4.6.

5 Conclusions

The objective of this project was to design a VRM load emulator with a target slew rate of $SR = 3000\,A/\mu s$ and a nominal current of $I_{LOAD} = 640\,A$, within a compact area. Regarding the feedback topology design and simulation, the system is stable and capable of providing both the nominal current in both topologies and the desired slew rate. However, the experimental results did not verify the simulated ones. By performing measurements on the board, several critical issues were identified, such as the effect of the offset voltage V_{OS}.

For future work, a second prototype may be developed. This prototype should be designed to support both feedback topologies and should incorporate either V_{OS} compensation or an operational amplifier with a reduced offset voltage. In addition, an appropriate test point for monitoring the output current of the operational amplifier should be included. Furthermore, the influence of $v_{O,VRM}$ during transients must be investigated and isolated from the driving input signal v_{IN}.

References

[1] V. Avelar, D. Azevedo, and A. French, "Pue: A comprehensive examination of the metric," *The green grid*, 2012.

[2] E. Masanet, A. Shehabi, N. Lei, S. Smith, and J. Koomey, "Recalibrating global data center energy-use estimates," *Science*, 2020.

[3] D. Donnellan, A. Lawrence, D. Bizo, *et al.*, "Uptime institute global data center survey 2024," *uptime intelligence*, 2024.

[4] GamersNexus. "Electricity 2024 - analysis and forecast to 2026." (Jan. 2024), [Online]. Available: `https://www.iea.org/reports/electricity-2024`.

[5] Y. Chen, K. S. M. Chen, and D. Xu, "Data center power supply systems: From grid edge to point-of-load," *IEE*, 2003.

[6] H. Sanogo, "Impacts of transients on ai accelerator card power delivery," *Analog Devices*, 2023.

[7] GamersNexus. "Nvidia titan v vrm analysis and shunt mod guide." (Dec. 2017), [Online]. Available: `https://www.gamersnexus.net/guides/3174-nvidia-titan-v-vrm-analysis-and-shunt-mod-guide`.

[8] HWBOT. "Gamersnexus: Nvidia titan v vrm analysis and shunt mod guide [newsflash]." (Dec. 2017), [Online]. Available: `https://hwbot.org/newsflash/5010_video_gamers_nexus_nvidia-titan-v-vrm-analysis-and-shunt-mod-guide`.

[9] TechPowerUp. "Sapphire nitro+ radeon rx 7900 xtx vapor-x specifications." (), [Online]. Available: `https://www.sapphiretech.com/en/consumer/nitro-radeon-rx-7900-xtx-vaporx-24g-gddr6`.

[10] wccftech. "Msi geforce rtx 3090 suprim x rtx 3080 suprim x graphics cards review." (Nov. 2020), [Online]. Available: `https://wccftech.com/review/msi-geforce-rtx-3090-rtx-3080-suprim-x-gddr6x-graphics-cards-review/`.

[11] S. Krishnakumar and I. Partin-Vaisband, "Vertical power delivery for emerging packaging and integration platforms - power conversion and distribution," *IEE*, 2023.

[12] D. Baretich. "Optimizing regulator output capacitance using loadslammers (part 1)." (), [Online]. Available: `https://prograanalog.com/resources/`.

[13] Infineon. "Optimos™ and strongirfet™ family selection guide." (), [Online]. Available: `https://www.infineon.com/products/power/mosfet/n-channel/optimos-strongirfet`.