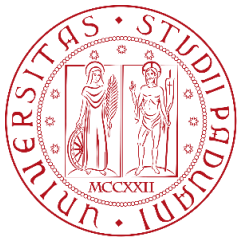

UNIVERSITY OF PADOVA

DEPARTMENT OF INFORMATION ENGINEERING

MASTER THESIS IN ELECTRONIC ENGINEERING

DESIGN OF THE EXPERIMENTAL SETUP AND TESTING OF A WIRELESS INTEGRATED CIRCUIT FOR ARTIFICIAL RETINA

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Desidero ringraziare in primis la mia famiglia, che mi ha permesso di svolgere e completare questi studi credendo sempre in me e il prof. Neviani, che mi ha seguito con molta pazienza in tutto il percorso e mi ha aiutato in particolare nel design delle reti di matching per gli induttori.

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Infine, vorrei cogliere l'occasione per ringraziare anche tutti gli altri che in questi anni abbiano contribuito al mio miglioramento personale.

Abstract

The purpose of this thesis is to build a laboratory setup for testing an artificial retina neurostimulator with wireless power and data transmission to treat chronic diseases of the eye like retinitis pigmentosa and age-related macular degeneration (AMD), to which there is no cure at the moment.

The goal of the artificial retina is to recover the loss of vision caused by damaged photoreceptors through electrical stimulation. Power must be supplied by an external case containing a battery and the the neurostimulator requires an integrated circuit for power and data transmission across the human body.

Right now existing artificial retina devices are very limited and rudimental so there is a need to do more research to find new devices for the market. The main problem is power consumption, since high power is required to implement an adequate resolution of recovered vision. The integrated circuit also dissipates too much heat and has a large area.

Other problems that need to be addressed are an insufficient vision resolution, incomplete level of packaging, and crosstalk between the electrodes which release electrical stimulation currents.

The proposed neurostimulator uses the technique called pulse delay modulation (PDM) for transmitting the data. This technique allows to transmit power and data signals across human skin in medical applications with a reduced power consumption and a good efficiency.

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Chapter 1: Introduction

1.1 Thesis overview

This thesis project aimed at designing 3 different PCBs (Printed circuit boards) with the Kicad software to test, after fabricating them, a prototype chip named GAMCHAN made by Jisung Kim and Hyunbeen Jeong, two PhD students of Seoul National University. This Chip is an IC representing an implantable neurostimulator for the retina to treat chronic diseases of the eye where people lose sight due to damaged retinal ganglion cells in the visual system: it is composed of a transceiver, for both power and data, and a neurostimulator for generating the impulses for the retinal tissue.

Jisung Kim focused on implementing the power and data transmission system part of the chip, while Hyunbeen Jeong focused on the design of the neurostimulator and the surgical aspect, such as the study of the electrodes with ex-vivo tests or the anatomy of neural tissue.

The first PCB is for mounting all the components required for the testing except for the inductors pairs which, due to their size and to the fact that they need to be perfectly coaxial when operating testing, require two separate PCBs which need to be plugged via pin connectors to the main PCB. The inductors serve as near-field antennas to transmit signals across the human skin thanks to magnetic field theory without the need of cables. There are 2 pairs of inductors in total: one pair is for transmitting the power and the other pair for transmitting the data to the receiver.

Since both transmitter and receiver are inside of the same chip, it is also required to use 2 different copies of the first PCB to simulate a real scenario, if someday this device will be available for the market, where an external transmitter powers a receiver that is implanted inside the eye as a separate chip.

In this way, connecting the small PCB with the inductors of the transmitter to one copy and connecting the inductors of the receiver to the second copy, by powering only the first PCB (Tx), theoretically it should be possible to see and measure some signals induced in the second PCB (Rx).

The thesis work is divided in the following chapters:

Chapter 1. Introduction on neurostimulation and historical background.

Chapter 2. Drawing a block diagram to understand the theoretical background and functioning principles of the chip, both when is used as an implantable terminal for receiving power and data signals to generate impulses for the electrodes implanted in the retina and when is used as a transmitter.

Chapter 3. Experimental setup description to identify the used instrumentation: i.e. DC, AC generators, oscilloscope, and signal amplifier. Describing the layout of the three PCBs made with Kicad: one for all the components required for the proper operation of the chip and the other two for the coupled antennas, realized as planar inductors with the respective matching network made of capacitors.

Chapter 4. Testing of the PCB at the ICARUS lab and reporting the results.

Chapter 5. Conclusion.

1.2 Neurostimulation intro

1.2.1 Neuron anatomy

The neuron is a fundamental building block of the nervous system: the simplified structure consists of three essential components: the cell body, dendrites, and axon. The cell body, which contains the nucleus, processes the incoming signals from the dendrites and generates new integrated signals that are transmitted to the axon. Dendrites are fibers responsible for receiving impulses from other neurons or receptors. The axon is the fiber for carrying electrical impulses away

from the cell body. Axons can transmit signals over considerable distances in the nervous system: from a receptor, such as those in the eye or ear, to a more central location in the nervous system, such as the spinal cord or brain [6].

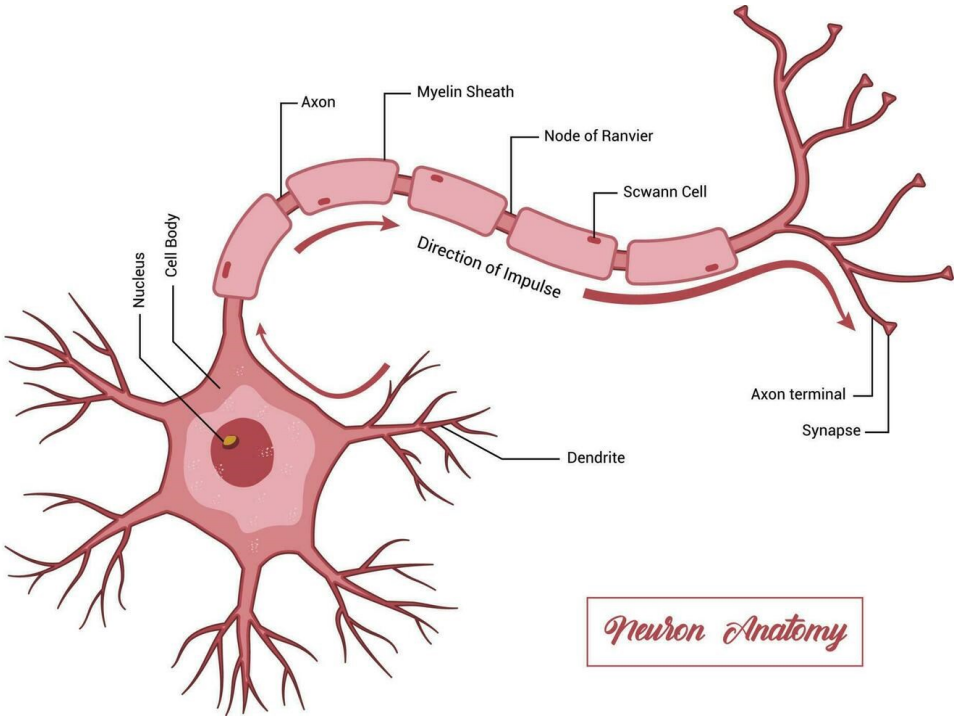


Figure 1.1: Neuron anatomy [7]

When an electrical impulse reaches the end of an axon, it triggers the release of neurotransmitters.

A pain state is generated by high-intensity input stimuli, tissue injury or inflammation.

1.2.2 What is a neurostimulation device

Implantable neurostimulators are the tools used by clinicians to execute various and diverse neuromodulation therapies. Such as the cardiac pacing, gastric neurostimulator or the neurostimulator for epilepsy. The term “neuromodulation”

refers to the therapeutic administration of electrical stimulation (or chemical agents) directly to the nervous system (spinal cord, brain or peripheral nerves) in order to modulate nerve cell activity.

The functioning principle of this device is generating defined currents or voltages and applying them to the electrodes in direct contact with the neural tissue.

An implantable neurostimulator is composed of three main components: a centralized implantable pulse generator (IPG), leads and electrodes (for stimulating and possibly for recording) [8] [9].

Neurostimulation is designed to disrupt pain signals as they move to the brain. These devices provide much-needed therapeutic relief to an unprecedented number of people affected by debilitating neurologic and psychiatric disorders worldwide. The rise of modern-day neuromodulation therapies extends over half a century, which are rich with serendipitous discoveries and technological advances that have led to different types of neurostimulation strategies. Within the past 2 decades, innovation in medical device technology has begun to speed up the evolution of these neurostimulation systems.

Due to a discovery that the stimulating electrodes just anterior to the somato-sensory cortex inhibited pain, there have been many additional studies to understand the therapeutic mechanisms of MCS, in comparison to DBS and SCS techniques, to alleviate chronic pain.

For epilepsy VNS (Vagus nerve stimulation) devices are a current treatment as well as for depression.

VNS devices are programmed to provide regular intervals of on and off stimulation with 1.0-3.0 mA currents at frequencies of 20-30 Hz. As for VNS surgery, a linear incision is made in the mid left neck area to place the electrode carefully. Next, careful dissection is carried out through the platysma muscle, through the carotid sheath, to the left vagus nerve. Then, a portion of the vagus nerve is dissected such that a cuff-type electrode is placed around it. The wire is

then tunneled through the subcutaneous tissue and connected to a battery that is placed just below the clavicle [10].

Pacemakers consist of a can containing the battery, the electronics for pulse generation, and the leads, which travel to the myocardium to deliver a depolarizing pulse and to sense intrinsic cardiac activity. Pacing occurs when a potential difference (voltage) is applied between the potential difference occurs between the lead tip (cathode) and a proximal ring electrode (anode).

The minimum amount of energy required to depolarize the myocardium is called stimulation threshold. The delivered stimulus is described by 2 characteristics: its amplitude (V) and its duration (ms). The energy required to pace the myocardium depends on the programmed pulse width and on the voltage delivered between the electrodes [11].

The output stage of the neurostimulator circuit must source and sink current pulses of several hundreds of uA to biological tissue featuring a series resistance in the order of tens of kΩ.

Intra-body and body area networks will allow for the integration of implanted stimulators, internal and external sensors, and programming and monitoring systems. Because of postoperative stability, most artificial retinas use pars plana as a place for the intraocular implantation of the device. The anatomy of the retina will be discussed in section 1.3.

Existing neurostimulation devices for the retina are, for example, Argus II, Alpha AMS and its predecessor Alpha IMS.

Argus II system, which has already been implanted in more than 300 people worldwide, includes an external component, consisting of a camera or photodiode array, a VPU (video processing unit), a transmitting coil and an internal component, which consists of a receiving coil, an application-specific integrated circuit (ASIC) with metal casing and the 60-channel epiretinal microelectrode array (MEA) with polyimide packaging.

Images captured outside by the camera are converted to electronic signals by the VPU and then wirelessly transmitted to the internal component of implanted device through the coils using inductive coupling. After transmitting and recovering the power and data by the internal electronics, the ASIC generates the stimulus signals the signals are delivered to the microelectrode array which induce epiretinal stimulation.

Various reasons have been reported for the devices' failure to recover the desired level of high-resolution vision, excessive power and area consumption in the ASIC, incomplete level of packaging, and crosstalk in the electrolyte between generated currents.

ASIC typically comprises a wireless power and data management circuit, a digital controller, a digital-to-analog converter (DAC), a voltage and current reference, a pulse generator, a demultiplexer, and a charge balancing circuit [12].

None of the existing packaging methods satisfies all conditions required by the artificial retina. Thus, there is a need for a new packaging method that can be processed into a form that satisfies both the surgical constraints and form factor requirements proposed above with negligible heat dissipation and integrated into a small chip area.

Also, postoperative infection, inflammation and retinal detachment were a few side effects reported by people with Argus II and 80% of patients required surgical intervention.

Alpha AMS, implanted on much fewer patients, also had the side effect of retinal detachment, and intraocular pressure was found in 3-40% of patients [5].

1.2.3 History of Neurostimulation

The history of neurostimulation begins after Scribonius Largus, the court physician to the Roman emperor Claudius, discovered that gout pain could be

treated with the electricity of a torpedo fish, around 63 AD. A famous scientist of the 17th century named William Gilbert also wrote about the electromagnetic qualities of the lodestone, a piece of iron ore, to manage painful symptoms of headaches and mental disorders with varying degrees of success.

An important step was made when Pieter van Musschenbroek, a physicist of the University of Leiden, developed the Leyden jar (Figure 1.2), a metal container filled with water suspended by ropes of insulating silk and with a brass wire inserted through a Cork. He observed that this jar had the capability of storing an electric charge. This is a fundamental part of electrostatics and can be considered as one of the first versions of the capacitor.

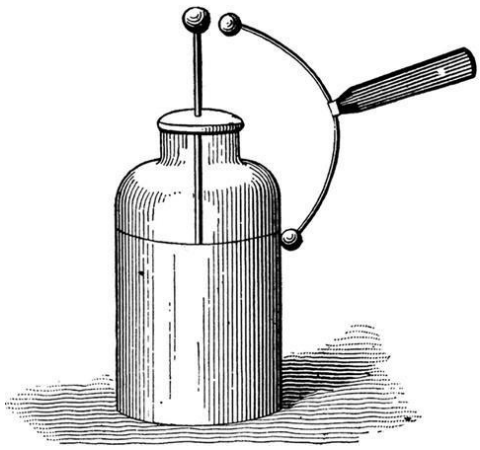


Figure 1.2: Bottle of Leiden also known as Leyden jar

The Leyden jar was used in 1746 by Jean Jallabert, who discovered that the electricity contained in the jar could be used to stimulate muscle fibers. He cured a paralyzed limb in a blacksmith causing involuntary contractions, regeneration of muscles and increased blood flow. This discovery inspired many scientists and, over the next twenty years, there were numerous reports of effective treatments of diseases and neuromuscular disorders. Electricity was considered by many one

miracle cure for many diseases and its use to stimulate areas of the body had far-reaching applications.

The first proof that human brain worked with electrical impulses and all the attempts to study its functions through electric stimulation came with the experiments of Luigi Galvani and Giovanni Aldini on animal electricity during the eighteenth century.

A new method to study cerebellar functions arose from the works of Luigi Galvani (1737–1798). Galvani's observation that electric sparks induced muscle contractions in frogs' legs led him to propose that the brain generated electricity, and that this electricity was distributed via the nerves to the muscles by triggering so-called natural electricity. The first publications of Galvani's observations and experiments on natural electricity were received with enthusiasm. Consequently, Galvani's work fostered the use and application of electricity in research. Giovanni Aldini (1762–1834), Galvani's nephew and collaborator, continued to work on natural electricity. In 1798, he initiated a series of experiments on warm-blooded animals. In one of his studies, he demonstrated motor responses following electric stimulation of the cerebellum and corpus callosum of an ox

Between 1884 and 1886, British scientist Sir Victor Horsley introduced the first practical application of intraoperative neurostimulation when electrical stimulation was used in a patient with epileptic foci to identify a specific cortical.

In the early 1900s, many devices were commercially available for the treatment of painful conditions, like devices for transcutaneous electrostimulation of the nerves, comparable to current TENS units, as well as devices such as the Electreat, which in 25 years sold up to 250,000 units. These electrical devices were used to treat medical problems such as gout, baldness, arthritis, and marital "problems". While these rudimentary devices may have produced few positive

results, they foreshadowed the development of therapeutic options in municipalities today.

The use of electric stimulation in neurophysiological research regained popularity during the second half of the nineteenth century. Groundbreaking research like the discovery of the motor cortex through electric stimulation prompted interest in the use of electric stimulation to study the cerebellum [1][2].

1.3 Human retina

The retina is a light-sensitive, multi-layer tissue for image acquisition and signal conversion. In the center of the retina there is the optic nerve, a circular to oval white area measuring about 2 x 1.5 mm across. The center of the optic nerve is the origin of the major blood vessels of the retina.

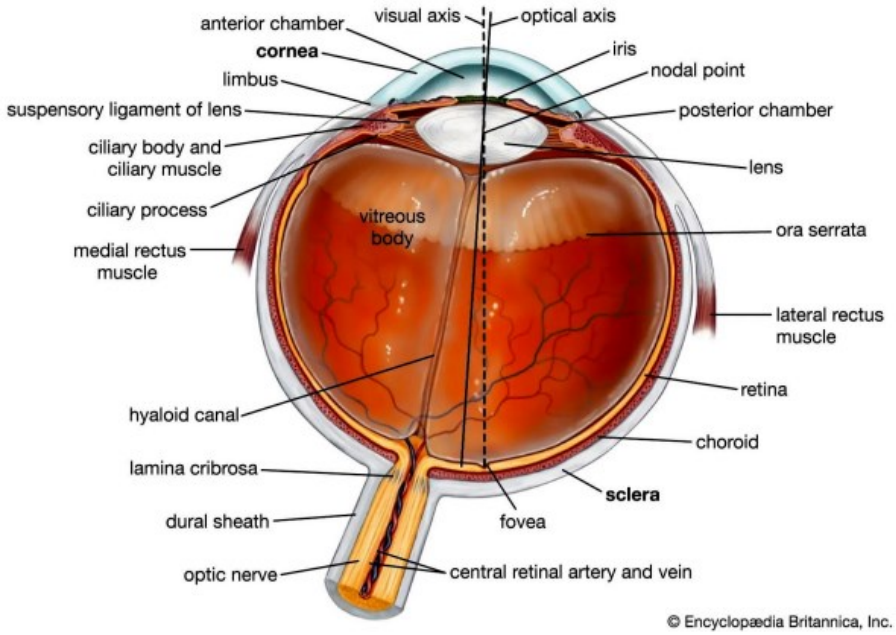


Figure 1.3: Structure of the eye

A circular field of approximately 6 mm around the fovea is considered the central retina while beyond this is peripheral retina stretching to the ora serrata, 21 mm from the center of the retina (fovea). The total retina is a circular disc of between 30 and 40 mm in diameter.

Outside the fovea rim, the retina gradually thins as it moves away from the fovea, and completely disappears in the pars plana region.

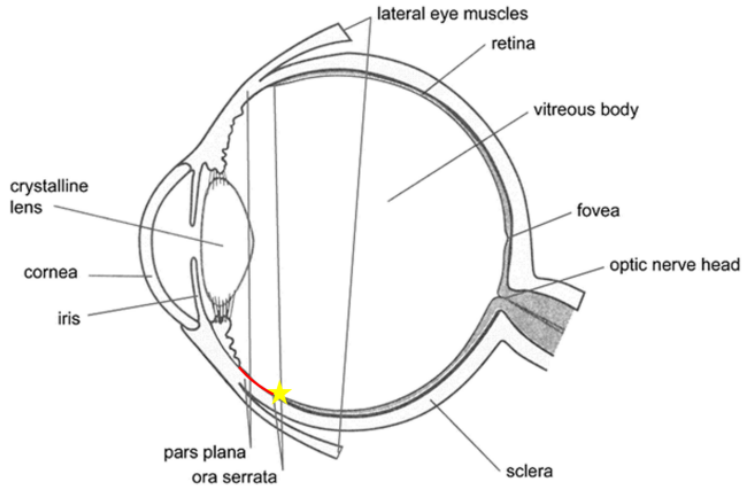


Figure 1.4: Location of pars plana and ora serrata [5]

The optic nerve contains the ganglion cell axons running to the brain and, additionally, incoming blood vessels that open into the retina to vascularize the retinal layers and neurons. A radial section of a portion of the retina reveals that the ganglion cells (the output neurons of the retina) lie innermost in the retina closest to the lens and front of the eye, and the photosensors (the rods and cones) lie outermost in the retina against the pigment epithelium and choroid. Light must, therefore, travel through the thickness of the retina before striking and activating the rods and cones.

All vertebrate retinas are composed of three layers of nerve cell bodies and two layers of synapses. The outer nuclear layer contains cell bodies of the rods and cones, the inner nuclear layer contains cell bodies of the bipolar, horizontal and amacrine cells and the ganglion cell layer contains cell bodies of ganglion cells and displaced amacrine cells. Dividing these nerve cell layers are two neuropils where synaptic contacts occur.

The central retina is a cone-dominated retina whereas peripheral retina is rod-dominated. Thus in central retina the cones are closely spaced and the rods are fewer in number between the cones.

The outer nuclear layer (ONL), composed of the cell bodies of the rods and cones is about the same thickness in central and peripheral retina. However in the peripheral the rod cell bodies outnumber the cone cell bodies while the reverse is true for central retina. In central retina, the cones have oblique axons displacing their cell bodies from their synaptic pedicles in the outer plexiform layer (OPL). These oblique axons with accompanying Muller cell processes form a pale-staining fibrous-looking area known as the Henle fibre layer. The latter layer is absent in peripheral retina.

The inner nuclear layer (INL) is thicker in the central area of the retina compared with peripheral retina, due to a greater density of cone-connecting second-order neurons (cone bipolar cells) and smaller-field and more closely-spaced horizontal cells and amacrine cells concerned with the cone pathways. Cone-connected circuits of neurons are less convergent in that fewer cones impinge on second order neurons, than rods do in rod-connected pathways.

A remarkable difference between central and peripheral retina can be seen in the relative thicknesses of the inner plexiform layers (IPL), ganglion cell layers (GCL) and nerve fibre layer (NFL). This is again due to the greater numbers and increased packing-density of ganglion cells needed for the cone pathways in the cone-dominant foveal retina as compared the rod-dominant peripheral retina. The

greater number of ganglion cells means more synaptic interaction in a thicker IPL and greater numbers of ganglion cell axons coursing to the optic nerve in the nerve fibre layer.

The first area of neuropil is the outer plexiform layer (OPL) where connections between rod and cones, and vertically running bipolar cells and horizontally oriented horizontal cells occur. The second neuropil of the retina is the inner plexiform layer (IPL), and it functions as a relay station for the vertical-information-carrying nerve cells, the bipolar cells, to connect to ganglion cells. In addition, different varieties of horizontally- and vertically-directed amacrine cells, somehow interact in further networks to influence and integrate the ganglion cell signals. It is at the culmination of all this neural processing in the inner plexiform layer that the message concerning the visual image is transmitted to the brain along the optic nerve.

The human retina is a delicate organization of neurons, glia and nourishing blood vessels. In some eye diseases, the retina becomes damaged or compromised, and degenerative changes set in that eventually lead to serious damage to the nerve cells that carry the vital messages about the visual image to the brain and blindness may be the end result.

1.3.1 Diseases of the retina

Retinitis pigmentosa is a nasty hereditary disease of the retina for which there is no cure at present. It comes in many forms and consists of large numbers of genetic mutations presently being analyzed. Most of the faulty genes that have been discoverd concern the rod photoreceptors.

The rods of the peripheral retina begin to degenerate in early stages of the disease. Patients become night blind gradually as more and more of the peripheral retina (where the rods reside) becomes damaged.

Eventally patients are reduced to tunnel vision with only the fovea spared the disease process. Characteristic pathology is the occurence of black pigment in the peripheral retina and thinned blood vessels at the optic nerve head [13].

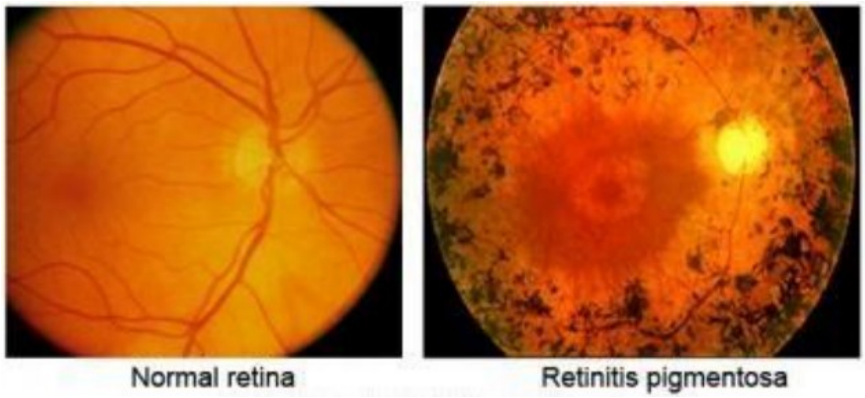


Figure 1.5: Retinitis pigmentosa

Age-related Macular Degeneration (AMD) is a common eye disease with aging, which causes damage to the macula and consequent vision loss. There are two types of AMD:

In wet AMD, choroidal neovascularisation breaks through to the neural retina, leaking fluid, lipids, and blood. In late dry AMD, progressive atrophy of the retinal pigment epithelium, choriocapillaris, and photoreceptors occurs.

Most severe visual loss from age-related macular degeneration occurs in the late stages of the disease. Major risk factors include cigarette smoking, nutritional factors, cardiovascular diseases, and genetic markers. This disorder is heritable and up to 20 genes are associated with age-related macular degeneration [14].

The number of patients suffering from AMD was estimated to be 196 million worldwide in 2020.

No effective preventive drug treatments exist for retinitis pigmentosa and AMD.

Researchers around the world are working on an artificial retina: the goal of the artificial retina is to recover the loss of vision caused by damaged photoreceptors through electrical stimulation. High-resolution images of more than 1000 pixels must be provided through the artificial retina in order to recover vision at a level that can distinguish faces, letters, and objects.

Neural prostheses work by recording or stimulating neural activity in the brain. For the treatment of diseases, the stimulation method is usually used. Stimulating neural activity involves delivering electrical impulses or other forms of stimulation to a specific nerve system. This can be used to bypass damaged or dysfunctional neural pathways and directly activate target regions [5].

Chapter 2: Theoretical background and functioning principles of the chip

2.1 Wireless power transmission intro

2.1.1 Battery problem

All neurostimulators require an energy source to generate the electric fields which modulate the nervous system [15].

The power can be supplied by a source that is either internal to the implantable device or external to the body. Usually internal power sources are small batteries that convert chemical energy into electrical energy through reduction–oxidation (re-dox) reactions: they are containing an anode, a cathode, and an electrolyte, allowing ions to move and form an electric current. If the space into which they are being implanted is small, however, power must be supplied to the system via an external power source which usually consist of inductive RF coupling. As a reliable source for long-term applications such as cochlear implants, pacemakers, defibrillators, or drug delivery, these Li batteries are widely used to provide the appropriate power levels from microamps to amps required by many types of implantable medical devices (IMDs). However, further implementations on implants have been limited by remaining hurdles of size and questions related to potential toxicity.

Another downside is that batteries also need to be replaced periodically, so for this reasons numerous power sources for IMDs have been extensively investigated over the past few decades, as most IMDs must rely on a permanent and sufficient power supply to ensure proper operation [8].

Different power approaches can allow the autonomous operation of IMDs by generating power to replace or supplement existing battery power. The main traditional challenges have been size limitations, inaccessibility, the need for

continuous work and biocompatibility. The power required to drive a biomedical device ranges from a few uW to hundreds of mW.

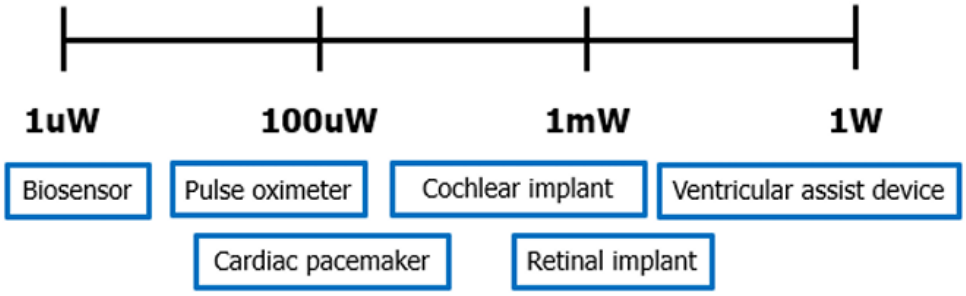


Figure 2.1: Different power requirements for IMDs

Among them, in the case of the cochlear implant described above, since the number of electrodes driven is smaller than that of the artificial retina, it is driven with the power of several hundred uW. In contrast, in the case of the artificial retina, correspondingly high power is required to implement a resolution similar to human vision [4].

2.1.2 Inductive links in RFID

The inductive data link acts as a band-pass filter only letting through the narrow pulse harmonics around fd with a small bandwidth around it, which results in a decaying sinusoidal waveform at f_d, following each data pulse, which represents a “1”.

High frequency carrier (50 MHz) is required for the data link while the power carrier frequency f_p, should be kept below 20 MHz.

Two separate links are used for power (L_1-L_2) and data (L_3-L_4) transfer to keep both PTE and bandwidth as high as possible. The coils need to be miniaturized and co-located inside the IMD but cross-coupling between the two pairs of coils

can be a challenge, since strong power carrier interference can dwarf the weak data signal on the receiver (Rx) side and make data recovery quite difficult.

In order to achieve a low bit-error rate (BER), a large signal-to-interference ratio (SIR) is needed. While innovative coil designs can help with reducing the coils' cross-coupling, it is still necessary to filter out the power carrier interference at the Rx input electronically at the cost of adding to the power consumption and complexity of the IMD [3].

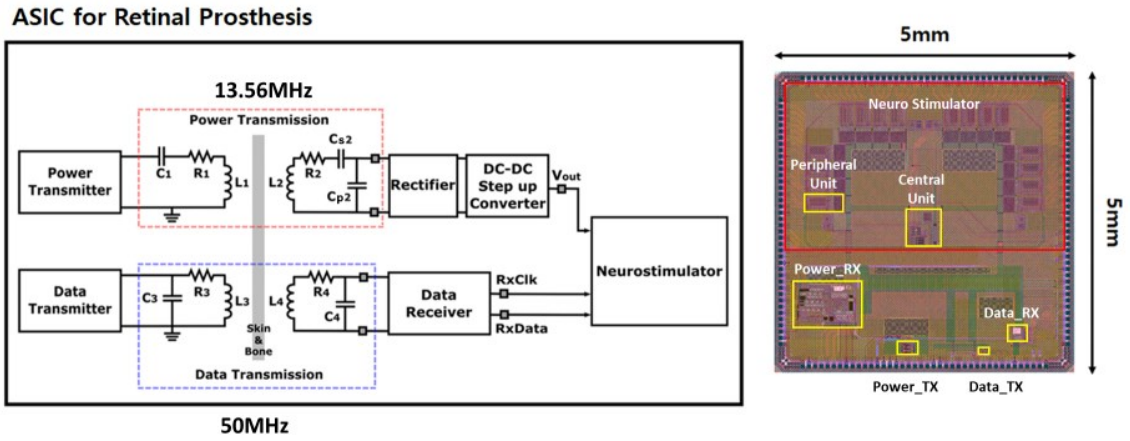


Figure 2.2: Inductive links for power and data

2.1.3 Pulse delay modulation technique

In this technique two narrow pulses are transmitted instead of every data carrier, thus increasing the data rate. PDM has also a good feasibility.

The main reason to choose this technique is power consumption, which is lower than traditional modulation techniques such as shift keying techniques. Undesired power carrier interference across Rx input, due to the proximity of power and data coils, is utilized to deliver the data bits, thus saving power and space needed for filtering out the power carrier interference on the Rx side.

Operation of PDM transceiver and internal structure

The PDM transceiver prototype was designed to operate at f_p=13.56 MHz within the industrial-scientific-medical (ISM) band.

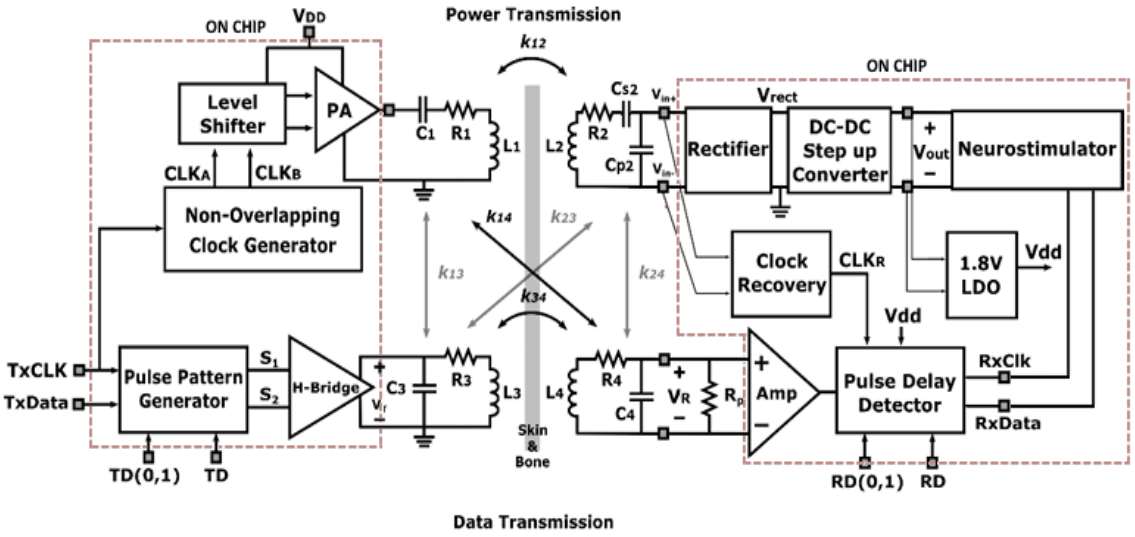
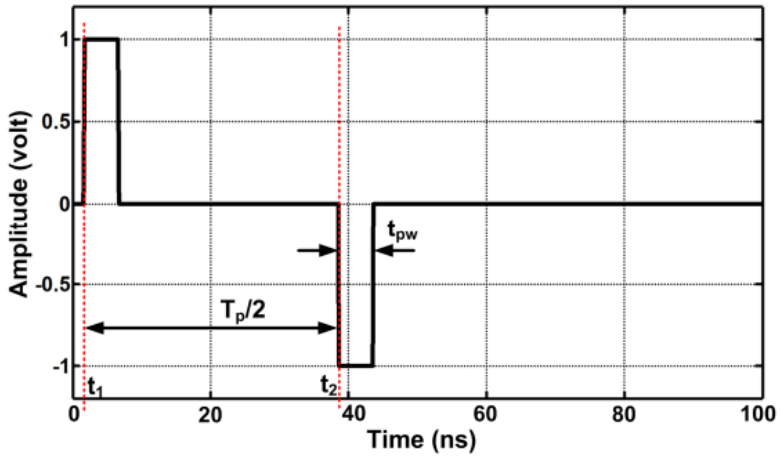
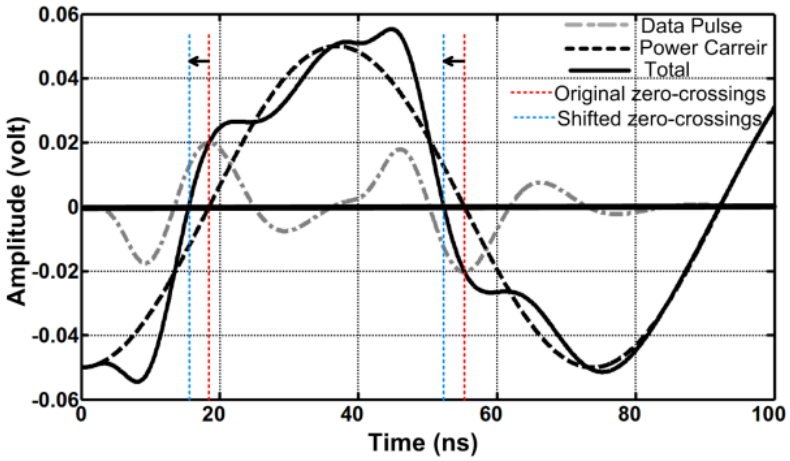


Figure 2.3: Block diagram of the full power and data transmission circuit system

In the presence of narrow pulses across L_3C_3 tank an oscillatory pattern at $f_d = \frac{1}{2\pi\sqrt{L_4C_4}}$ appears across L_4C_4 tank due to k_{34}. The inductive data link acts as a band-pass filter, only letting through narrow pulse harmonics around f_d, which results in a decaying sinusoidal waveform following each data pulse, which represents a "1" [16].



a) Narrow pulses generated at Tx for data bit "1"



b) Data signal received at L_4C_4 tank

Figure 2.4: Pulse delay modulation theoretical operation

2.1.3.1 Power transmitter

A clock generator block creates two non overlapping clocks from an external master clock signal at the desired carrier frequency f_p, for a class-D power amplifier. By passing the level shifter, the generated clock signals were converted to external V_{DD}: Class-D PA supply is adjustable from 1.8 V to 5 V to control the output power of PA.

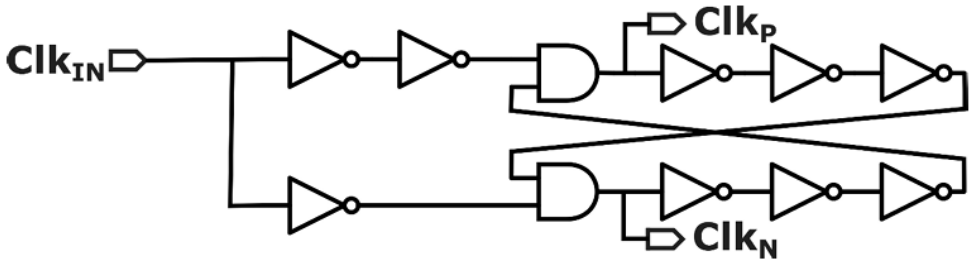


Figure 2.5: Non overlapping clock generator diagram

The power carrier signal at a desired output power level that can be adjusted by its supply voltage PA_V_{DD}. Power carrier is delivered to L_1 after passing through a matching circuit to induce a current in L_2.

The Class-D amplifier has a complex structure but can achieve up to 90% energy efficiency and can be designed in a small size. The PA is made of a tapered buffer and structure similar to a CMOS inverter, with a PMOS and an NMOS transistor.

Since the PA has high output currents, more than 1 PA is placed in parallel inside the chip.

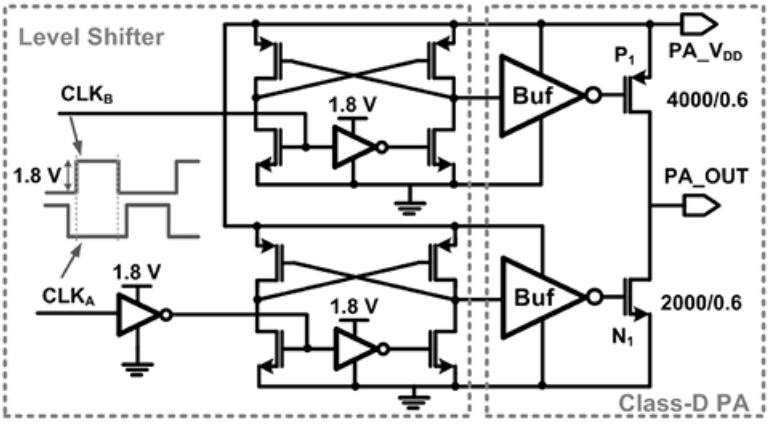


Figure 2.6: Level shifter, tapered buffer and output stage of PA

2.1.3.2 Power receiver

A passive full-wave rectifier followed by a reconfigurable DC-DC step-up converter and a regulator, as well as a clock recovery circuit that extracts the internal clock of the received signal from L_2C_2 tank compose the power receiver. The signal process part of the DC-DC converter commands its operation.

L_1C_1 and L_2C_2 tanks are both tuned at f_p, they need to be designed with high Q factor to have a narrower bandwidth and the induced power carrier on the L_2C_2 tank is much stronger than that of the low Q L_4C_4 tank.

The geometries of a printed spiral coil in the Tx and Rx were optimized at 13.56 MHz for power transmission.

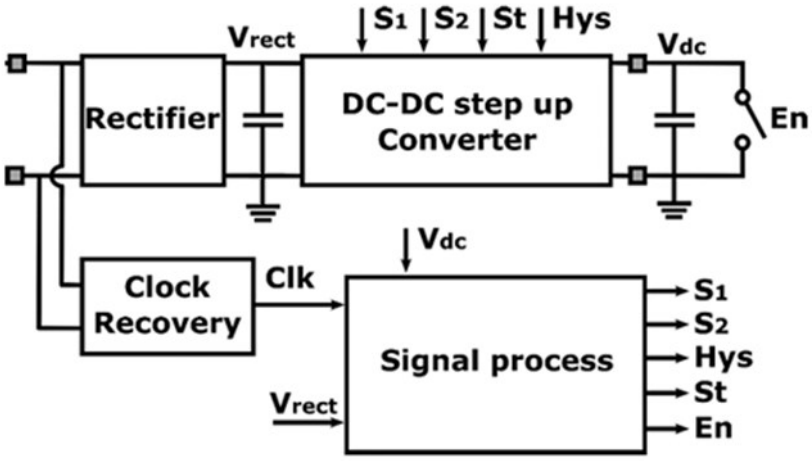


Figure 2.7: Power receiver block diagram

Small implanted systems consist of electrodes with a built-in receiver: the battery and transmitter are contained in an external, wearable device. The implanted system is activated (pulse generated) when the external device is placed on the skin.

Wave rectification removes the negative input voltage with one diode and converts it into direct current. However, for IC applications, full wave rectifiers must be realized entirely using CMOS technology to avoid excessive voltage drops. However, when operating as a switch, there is an unwanted leakage current between the MOSFETS.

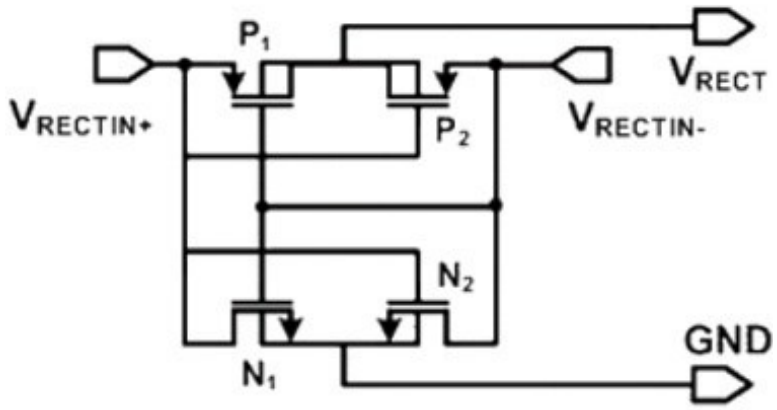


Figure 2.8: Diagram of the CMOS rectifier

Where V_{rect} is the voltage at the load capacitor of the rectifier output (CINUP).

After having been rectified, the power signal must go through the DC-DC step-up converter to bring the rectifier output voltage, which is estimated to be around 1,4 V - 3,3 V, to 5 V.

The architecture used is the Dickson charge pump step-up converter, which is made primarily of switches, realized with NMOS transistors, and four flying capacitors. The circuit counts 4 flying capacitors and 13 switches driven by a two-phase clock.

The flying capacitors CF_k are used for energetic charge storage to raise voltage and the values must be chosen large enough in order to guarantee that the

coverter operates in FSL, which is the fast switching limit. Given the required output power level, capacitors must be realized with external SMD on the PCB.

The conversion ratios n_i determine which flying capacitors are shunted by driving the gate of the MOS switches.

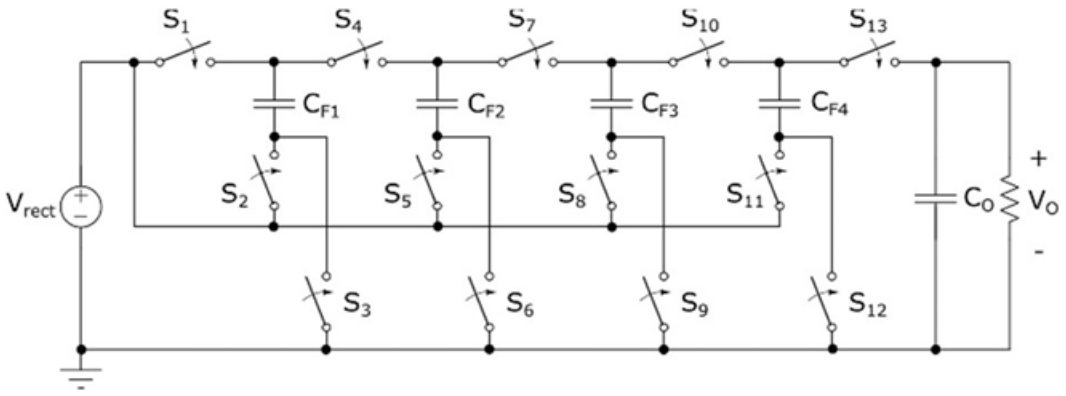


Figure 2.9: Simplified model of Dickson step-up converter with programmable conversion ratios n_i = (2, 3, 4, 5).

Besides the Dickson reconfigurable converter, the complete Step-Up Switched Capacitor Converter includes a start-up circuit, to manage the WPT turn-on transient, an automatic configuration selector, that sets the conversion ratio value n_i according to the input voltage value, an hysteretic controller to regulate the output voltage value V_O in steady state, a non-overlapping, two-phase clock generators and a voltage reference [17].

The last block of the power receiver is the Low drop out voltage regulator creates the necessary 1.8 V supply from the power supplied by the step-up converter for the MOSFETs used in data receiver. It consists of an error amplifier with a resistive feedback network, an NMOS transistor on the second stage and an output capacitor.

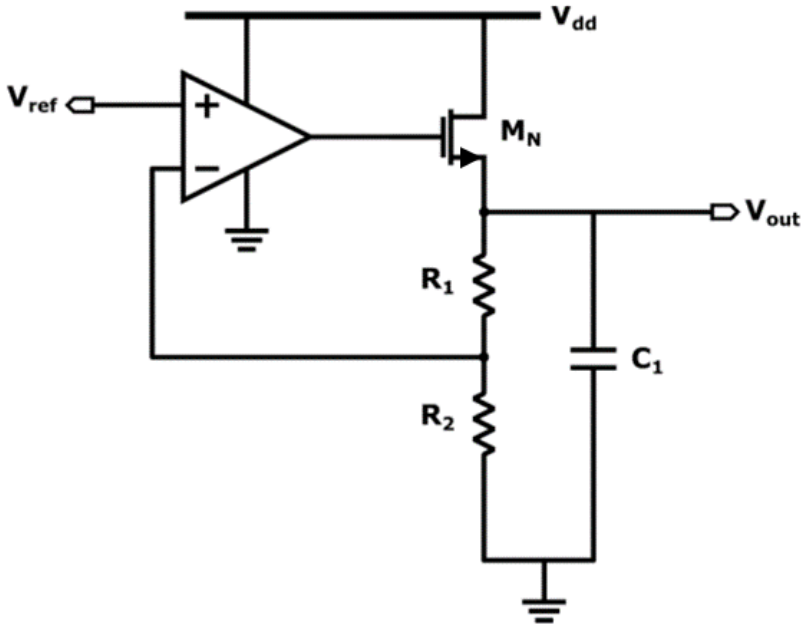


Figure 2.10: Low drop out voltage regulator (LDO)

2.1.3.3 Data transmitter

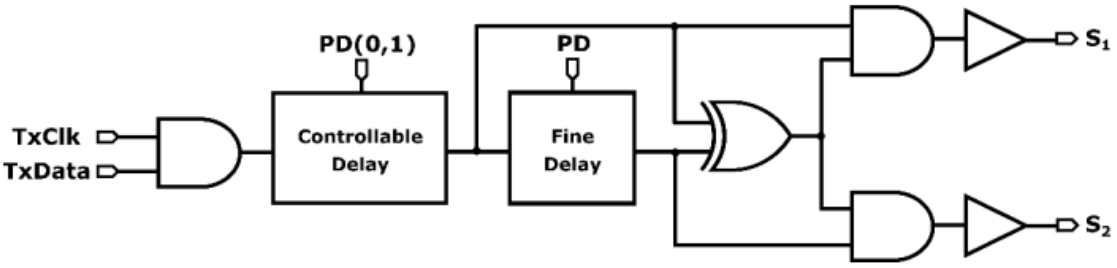
Inside data transmitter circuit, a pulse pattern generator (PPG) generates two narrow pulses in sync with the power carrier spaced by $T_p/2 = \frac{1}{2f_p}$. For Tx data bit "0" no pulses are transmitted.

Instead of an LC driver an H-bridge circuit is used to transmit each pulse across L_3-L_4 data link. Each data pulse generates decaying ringing response at a carrier harmonic frequency L_4C_4 is tuned at.

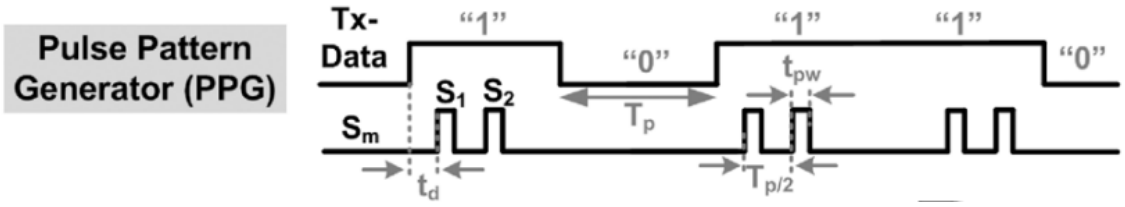
Within every data bit "1" period, ringing from these two pulses alter the timing of the power carrier interference zero-crossings across L_4C_4 tank, which is induced through k_{14} and k_{24} cross couplings.

To avoid inter-symbol interference with the next pulse of data bit "1", it is important for these ringing to dampen quickly. The damping rate depends on the

quality factor of the L_4C_4 tank so one way to dampen oscillations quickly is to reduce the quality factor of L_4.



a) Pulse pattern generator diagram



b) Pulse pattern generator operation

Figure 2.11: Pulse pattern generator diagram and operation

The purpose of a H-bridge is to reverse the poles of the two narrow pulses generated by the pulse pattern generator to control the flow direction of the current through L_3.

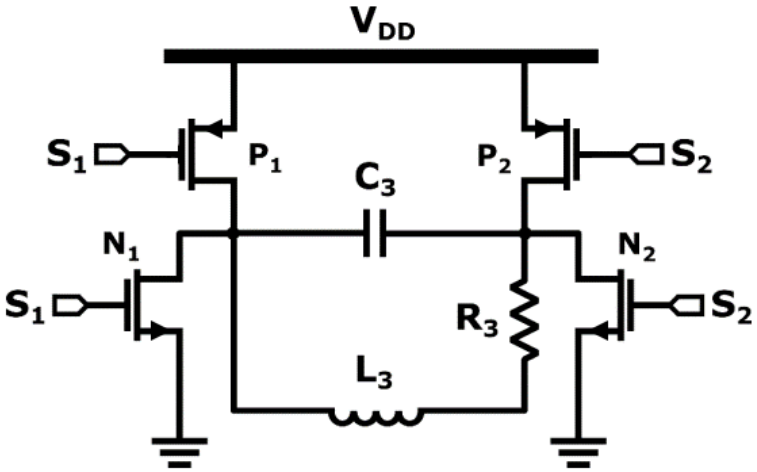


Figure 2.12: H-bridge

2.1.3.4 Data receiver

The two narrow pulses transmitted across L_3C_3 tank at $T_p/2$, which generate data ringing, change the shape of the received power carrier interference across L_4C_4. Delay time t_d needs to be adjusted based on the delay between data ringing and power carrier interference zero-crossing times across the tank, as it can be seen in fig. 2.13. The jitter in Tx-Clk and any changes in the link impulse response due to coupling variations can vary t_d.

Since no pulses are transmitted for a bit "0", any delay between signals across L_4C_4 and L_2C_2 tanks represents a bit "1", which can be easily detected using a simple phase detector circuit.

A high gain amplifier (fig. 2.14) amplifies the received signals of power interference with data ringing. The amplifier has 22.2 dB of gain at f_d = 50 MHz.

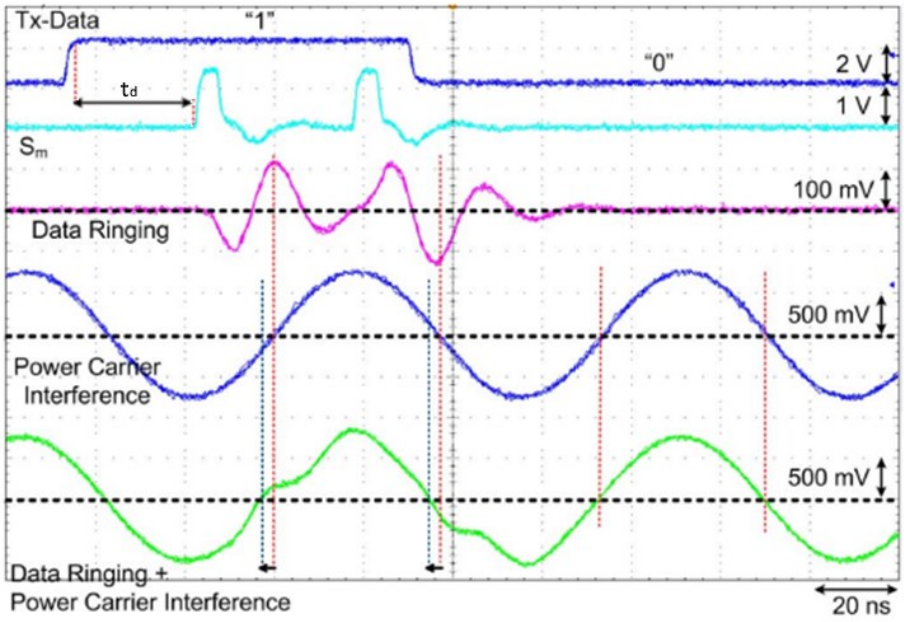


Figure 2.13: PDM theory example [3]

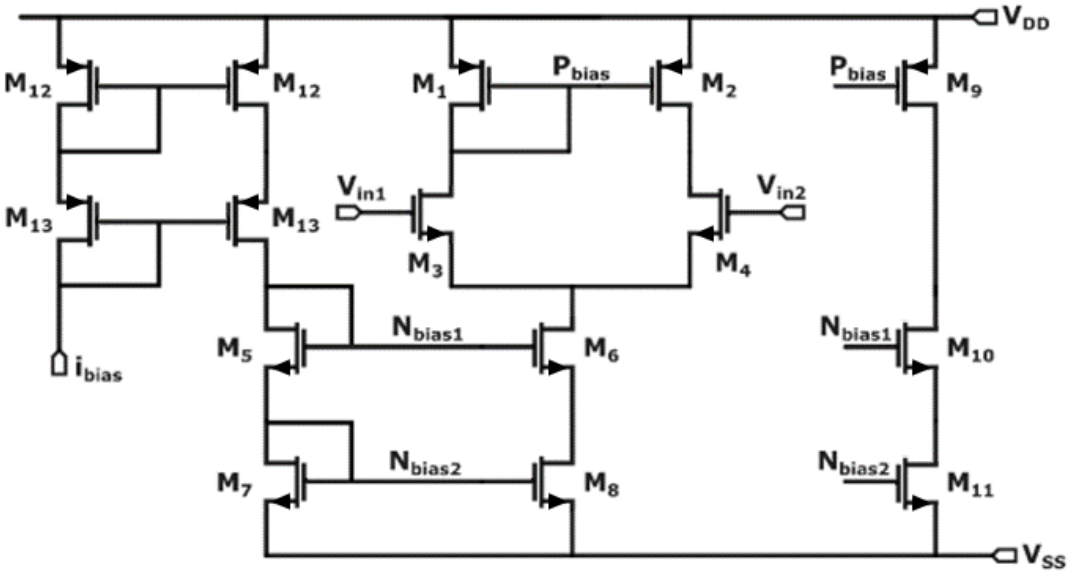


Figure 2.14: Data receiver amplifier

A pulse delay detector compares the input signal of the amplifier with the recovered clock to detect the delay between them. Two signals generated from a NOR and a XOR logic gate, V_{reset} and V_{PD}, go through an integrator circuit that charges/discharges a capacitor.

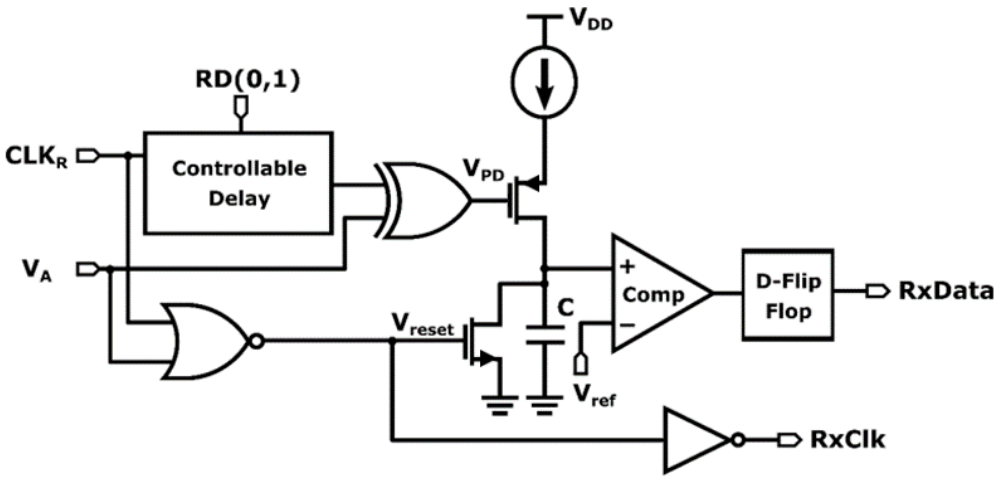


Figure 2.15: Pulse delay detector

The output of the integrator is then compared with an adjustable external reference voltage (V_{ref}): when $V_{INT} > V_{ref}$, data bit '1' is detected, otherwise '0'.

Lastly, a D-Flip Flop synchronizes RxData with the rising edge of the clock [3] [4].

2.2 LQFP package

The Low Profile Quad Flat Package (LQFP), is an enhanced version of the standard QFP package designed to provide improved heat dissipation capabilities and a thinner, lighter profile. With the growing trend of miniaturization in the electronics industry, PCBA companies use this package to reduce the size and weight of PCBA board.

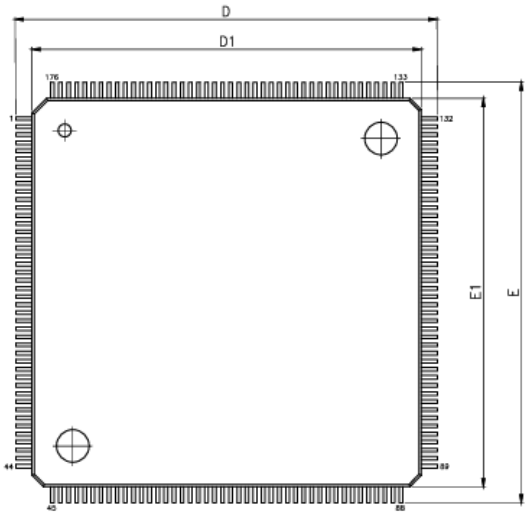
LQFP package footprint features gull-wing-shaped leads that are located on all four sides of the package and can be soldered directly to the PCB surface. The package is available in various body sizes, typically ranging from 32 to 176 pins,

with the most popular ones being 32, 48, 64, 100, and 144. The pin spacing values used by the LQFP package range from approximately 0.5 mm to 1.27 mm.

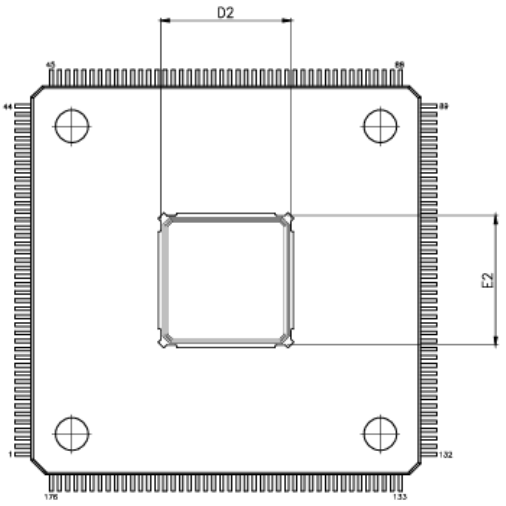
LQFP package is an excellent choice for applications that require improved heat dissipation and miniaturization [18].

The chip utilized is LQFP-176 surface mount (SMT) package with 160 used pads and it needs to be soldered at the center of the main PCB.

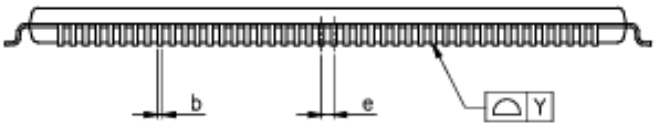
As previously said, for convenience reasons, the transmitter and receiver are both built inside the same prototype chip so, in order to do the testing, 2 PCBs are needed, one used as transmitter and the other as receiver.



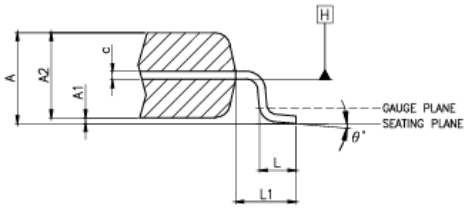
a) Front



b) Back



c) Side



d) Pin length & angle

Figure 2.16: LQFP-176 with all measures

In the bottom a metal square with side D2=E2 connects the chip to GND and also works as a heat dissipator.

Table 2.1: Table of variations of the LQFP-176 package

PARAMETER	MIN	NOM	MAX
A	-	-	1,60 mm
A1	0,00 mm	-	0,15 mm
A2	1,35 mm	1,40 mm	1,45 mm
b	0,17 mm	0,22 mm	0,27 mm
c	0,09 mm	-	0,20 mm
D	-	26,00 mm	-
D1	-	24,00 mm	-
E	-	26,00 mm	-
E1	-	24,00 mm	-
e	-	0,50 mm	-
L	0,45 mm	0,60 mm	0,75 mm
L1	-	1,00 mm	-
θ	0°	3,5°	7°
Y	-	0,08 mm	-
D2	7,90 mm	8,00 mm	8,15 mm
E2	7,90 mm	8,00 mm	8,15 mm

The bonding diagram (Figure 2.17) indicates the correspondence between the names of input-output pads of the chip and the pin number of the package. The pads that must stay unconnected on the PCB are highlighted in black.

All the V_{SS} pads guarantee a return of the current on every section of the chip thus limiting parasitic inductance effects typical of large circuit rings.

The first 2 and last 2 pads of each side of the chip are unused, while the V_{SS} pads are connected internally to a metal substrate, which is in turn connected to the ground square electrode of fig. 2.16b), visible externally.

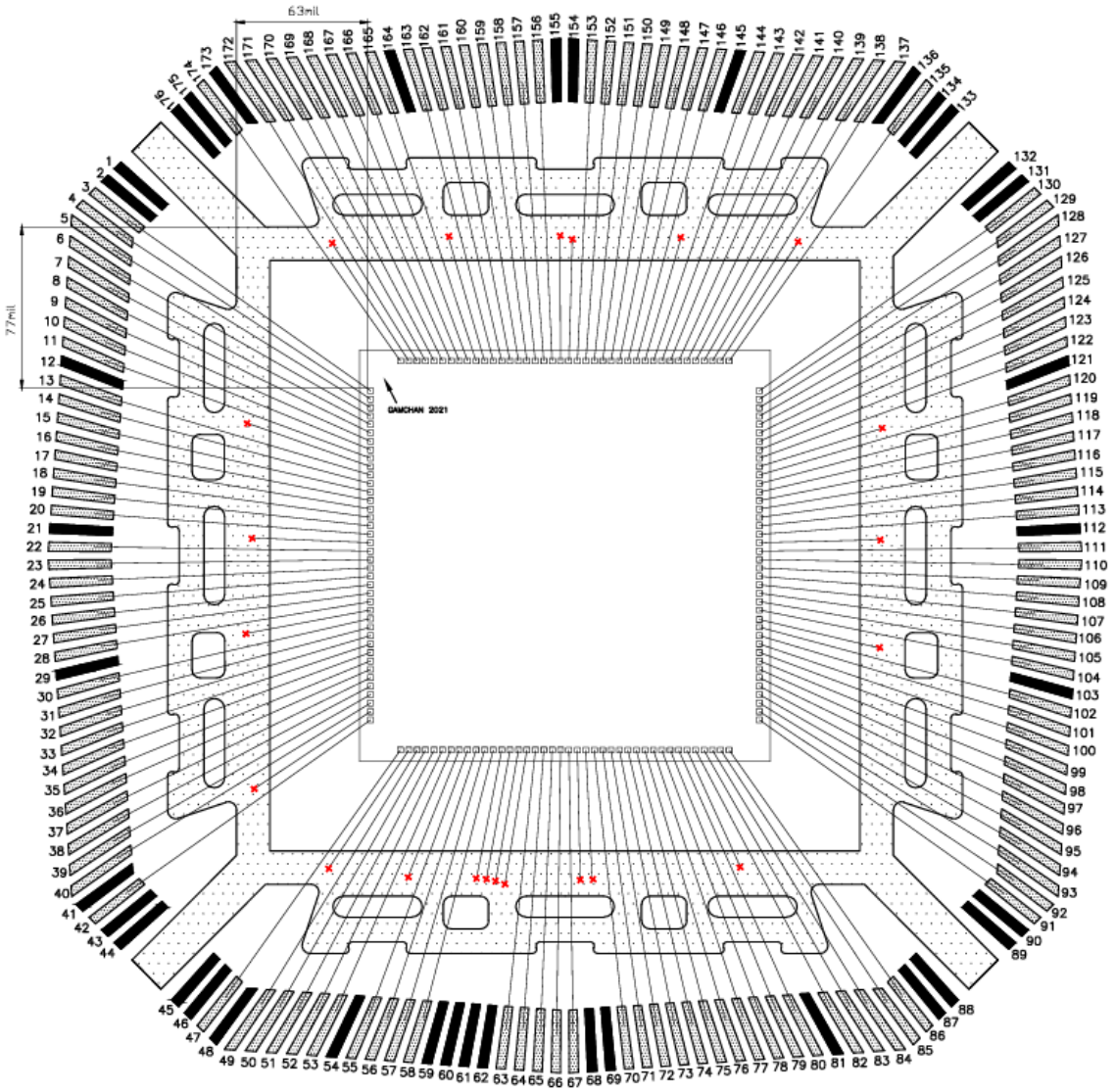


Figure 2.17: Bonding diagram of GAMCHAN

2.2.1 Pads

The neurostimulator is divided in groups of 8 electrodes alternated by V_{SS} for a total 64 electrodes plus 2 reference electrodes to be used as a reference to measure the currents. The choice is to connect all electrodes to 2x4 male pin connectors at the periphery of the PCB.

V_{DD_ESD} is the protection against electrostatic discharges to minimize the probability of permanent damage to components inside the chip.

2.2.1.1 Chip units

Fig. 2.18 reports all the units the chip is composed of: a more detailed list of the chip pads is reported in Appendix A.

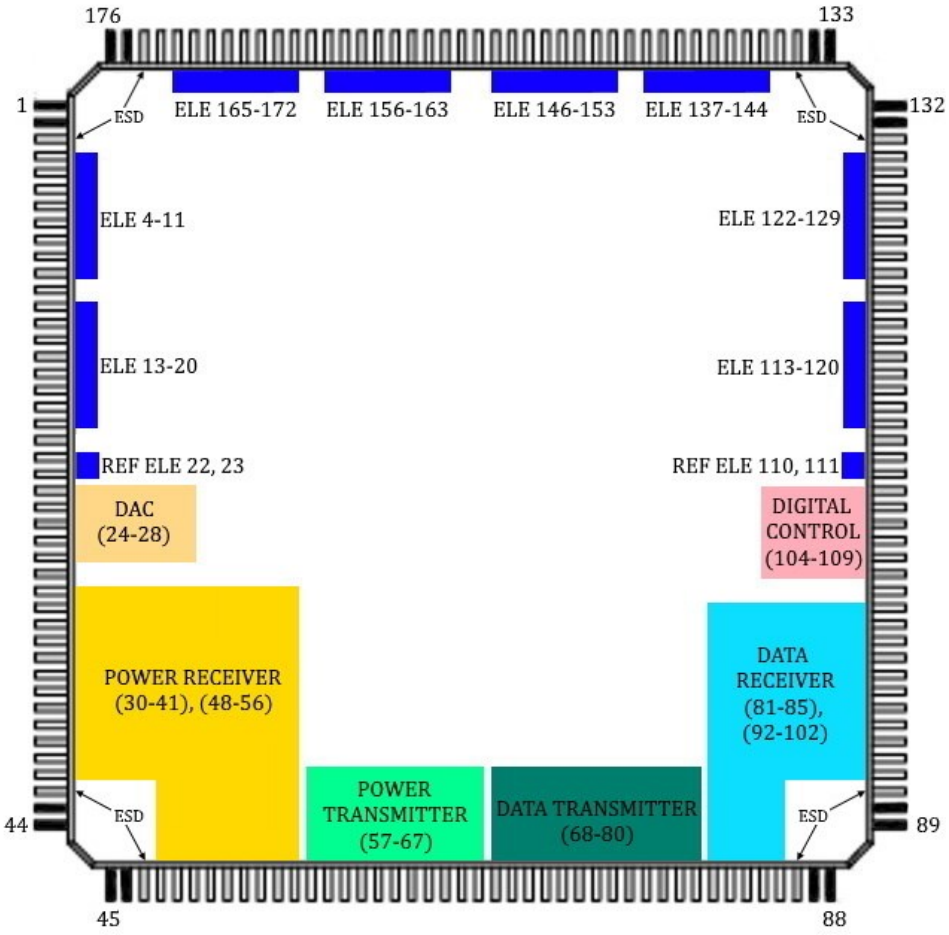


Figure 2.18: Different units of the chip

The units of the chip are:

Power transmitter unit The power transmitter unit contains the pads of the PA power supply (V_{DD_PA}), the output of the PA (PA_OUT), the input master clock signal (CLK_IN), and the power supply for the non overlapping clock generator ($V_{DD\_CLK\_IN}$).

Power receiver unit The power receiver unit has all the input/output voltages of the rectifier (RECTIN+/-, CINUP) and of the DC-DC converter (CINUP, VOUT_5).

Data transmitter unit The data transmitter unit has the input data pad (D_TX_IN), L_3-L_4 data link input (L+/-), and the power supply for data transmission circuit (V_{DD_TX}).

It also includes the input pads of bias currents and control voltages of the pulse pattern generator controllable delay block (Fig. 2.11).

Data receiver unit The data receiver unit has the L_3-L_4 data link output pad(AMPIN+/-) and pulse delay detector controllable delay block voltages.

DAC unit The DAC unit is an analog part with a 4-bit binary weighted DAC with a cascode mirror which received the voltage signal from the global DAC, including a demultiplexer [5].

Pin 28 is connected to 5 V supply through a 200 kΩ resistor.

Digital control unit The digital control unit is for collecting data from the receiver and transmit them to the digital control circuits of the outputs of the neurostimulator.

The informations of the data to be controlled are amplitude and length of bipolar impulses, consisting of an output and an input current: each of 64 outputs must have impulses of programmable amplitude and duration to avoid residual charge in the neural tissue of the retina.

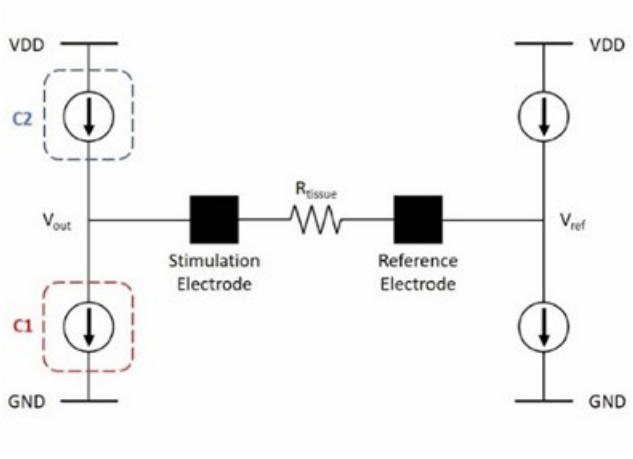
Pins 104, 105 need to be read with Logic Analyzer (or Raspberry PI) and pins 106-109 to be driven with Digital Pattern Generator (or Raspberry PI).

Electrodes When testing the outputs of the neurostimulator, an equivalent circuit to substitute the electrode implanted inside the eye must be realized on a millefori or a breadboard and connected between one of the 64 electrodes and a reference electrode.

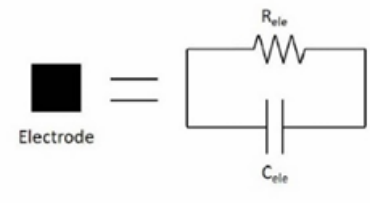
A resistance of retinal tissue is modeled as R_{tissue}. A voltage of the output stage and the reference electrode are marked as V_{out} and V_{ref}. Also, an electrode model based on Helmholtz double layer was used.

According to this model, electrode could be represented as a parallel connection of a resistance and a capacitance.

The stimulation electrode would be modeled as a parallel connection of R_{sti} and C_{sti} and the reference electrode was modeled as a parallel connection of R_{ref} and C_{ref}.



a) Equivalent model



b) Electrode interface

Figure 2.19: Interface between stimulator and retinal tissue

Considering that $R_{sti}C_{sti} \gg T_{MAX}$ and that $C_{ref} \gg C_{sti}$ it is possible to approximate:

$$V_{out,max} = 0{,}5 * V_{DD} + I_{MAX}(R_{tissue} + T_{MAX}C_{sti}) \quad (3.26)$$

$$V_{out,min} = 0{,}5 * V_{DD} - I_{MAX}(R_{tissue} + T_{MAX}C_{sti}) \quad (3.27)$$

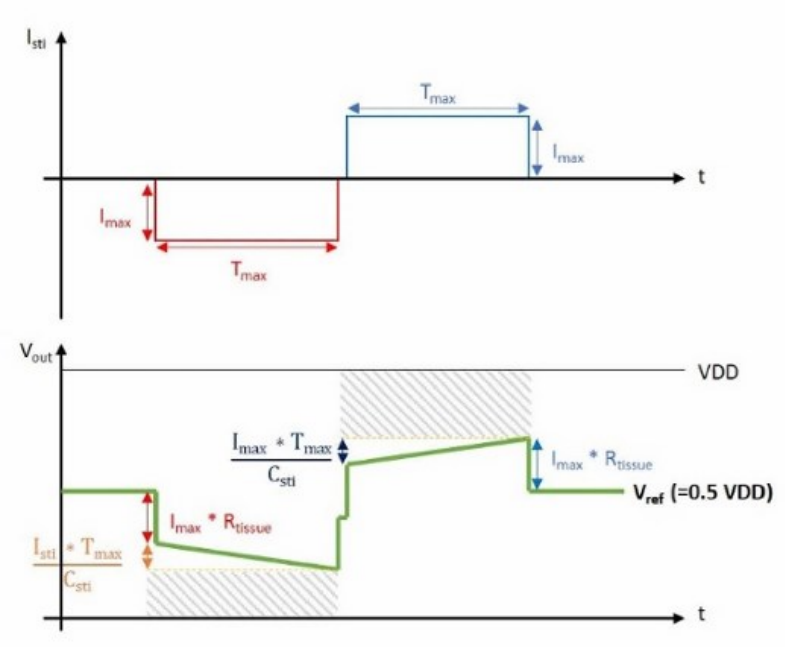


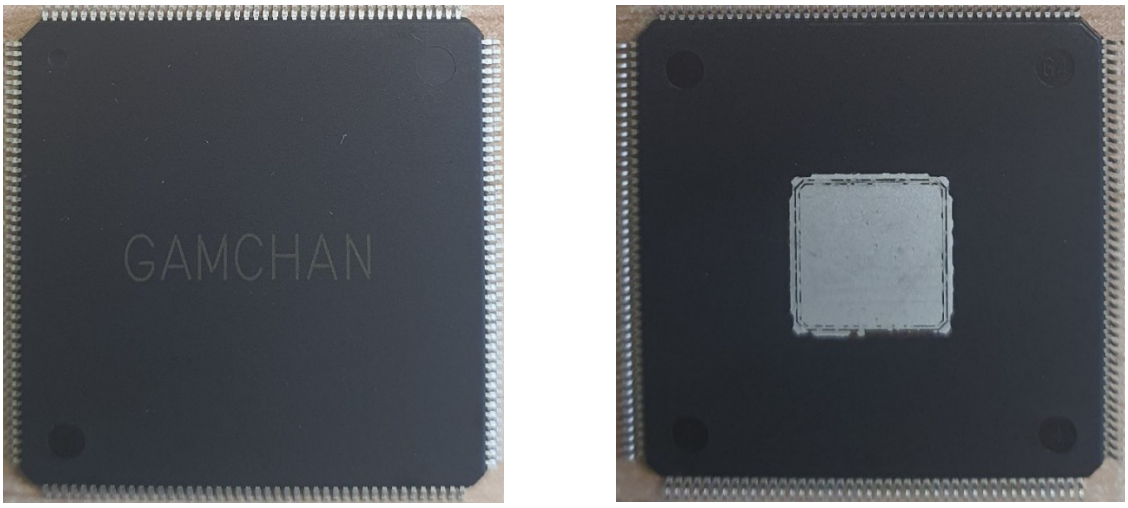
Figure 2.20: Current and output voltage change during stimulation

The term $I_{MAX}(R_{tissue} + T_{MAX}C_{sti})$ can be considered as the multiplication of stimulation current and the impedance of the electrodes ($Z_{electrode}$), which is $R_{sti}//\frac{1}{j\omega C_{sti}}$ plus tissue resistance.

Table 2.2: Stimulation parameter for DC calculation

Variable	**MIN**
$I_{cathodic/anodic,max}$	500 µA
R_{tissue}	10 kΩ
R_{sti}	1 MΩ
R_{switch}	10 Ω
C_{sti}	300 nF
T_{period}	1/60 s
t_{sti}	2 ms
$t_{discharge}$	10 ms

To remove harmful direct current (DC) after the stimulation caused by an unbalanced bi-phasic pulse, residual charge should be neutralized, since in real applications no charge must accumulate in the human eye [12].



a) Front b) Back

Figure 2.21: GAMCHAN chip of Seoul University, South Korea

Chapter 3: Experimental Setup

3.1 Lab instrumentation

DC and AC voltage generators Agilent E3631A and E3630A DC voltage generators with low output ripple and noise: Their outputs were connected with wires to the V_{DD} POW-GND connectors on the PCB for power supply.

Figure 3.1: Agilent E3631A DC voltage generator

Agilent 33250A waveform generator was used to generate the 13,56 MHz square wave required for the clock of the chip and to characterize the inductors. The maximum frequency for sine and square waves is 80 MHz and the output impedance of the generator is 50 Ω. The output of the generator highly depends on the value of the selected output impedance.

Figure 3.2: Agilent 33250A 80MHz arbitrary waveform generator

Oscilloscope Tektronix TDS6804B was the oscilloscope utilized all the time for displaying, scaling and measuring the signals.

Figure 3.3: Tektronix TDS6804B digital storage oscilloscope

Differential amplifier DA1855A is intended to act as signal conditioning preamplifier for oscilloscopes, spectrum analyzers and other instruments, providing differential measurement capability to instruments having only a single-ended input. The bandwidth is of 100 MHz.

Figure 3.4: DA1855A amplifier

3.2 Kicad scheme

The PCB (80 x 80 mm) has a copper pour on both front and back layer to connect components to GND. This copper pour is also filled with a hole density of 280 holes/dm^2 in order to keep the 2 layers always strictly connected together.

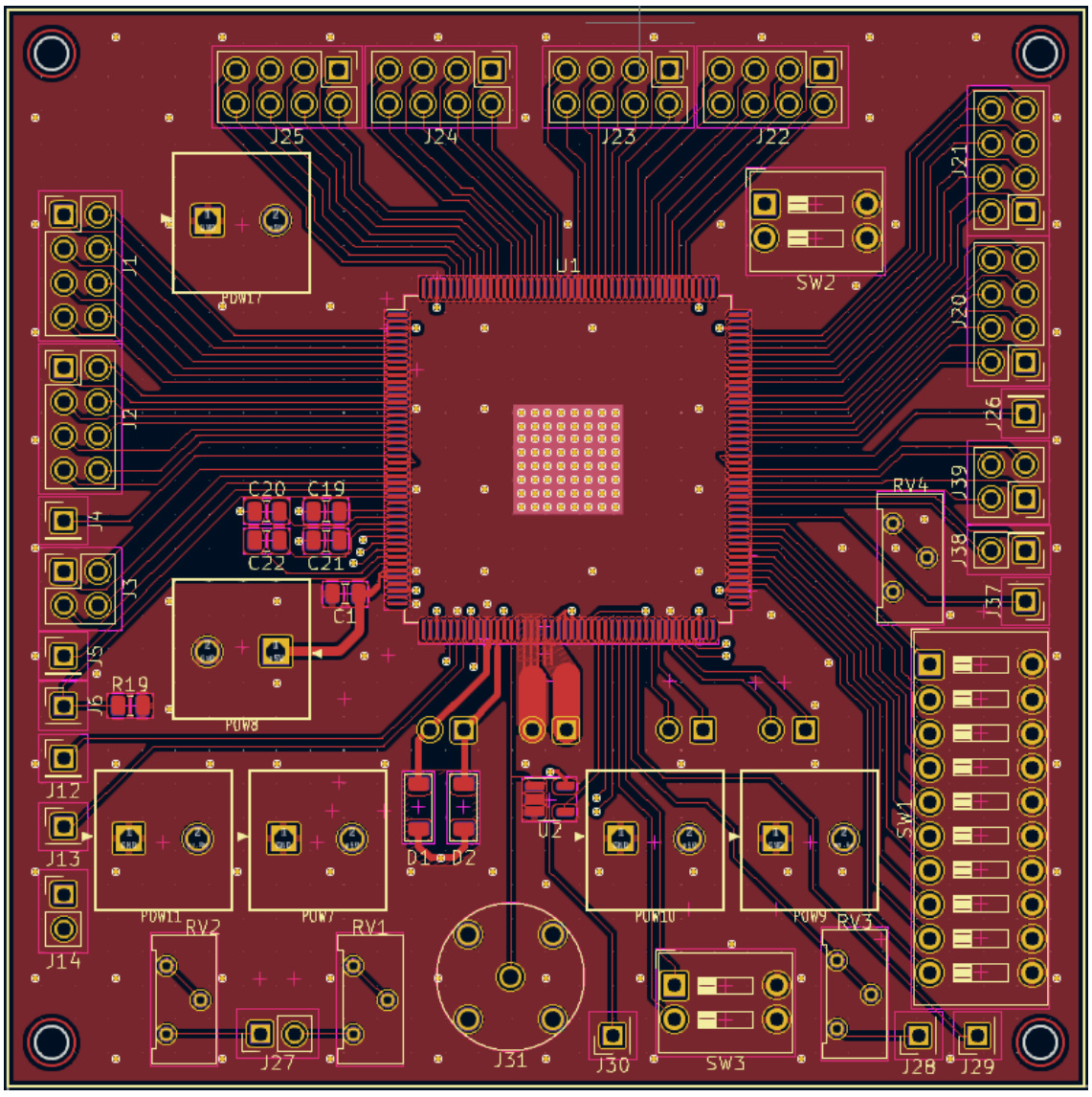


Figure 3.5: Front design scheme of the main PCB in Kicad

At the center of the PCB is mounted the GAMCHAN chip, which is connected to the footprints of the components through all the tracks, which are 0,15 mm large and spaced at least 0,3 mm from each other. The tracks of power transmitter output and PA_V_{DD} are 2 mm wide since there is a high current flowing in them. The thickness of copper layer is 35 µm and the minimum outer layer ring of through vias (OAR) is set to 0,125 mm.

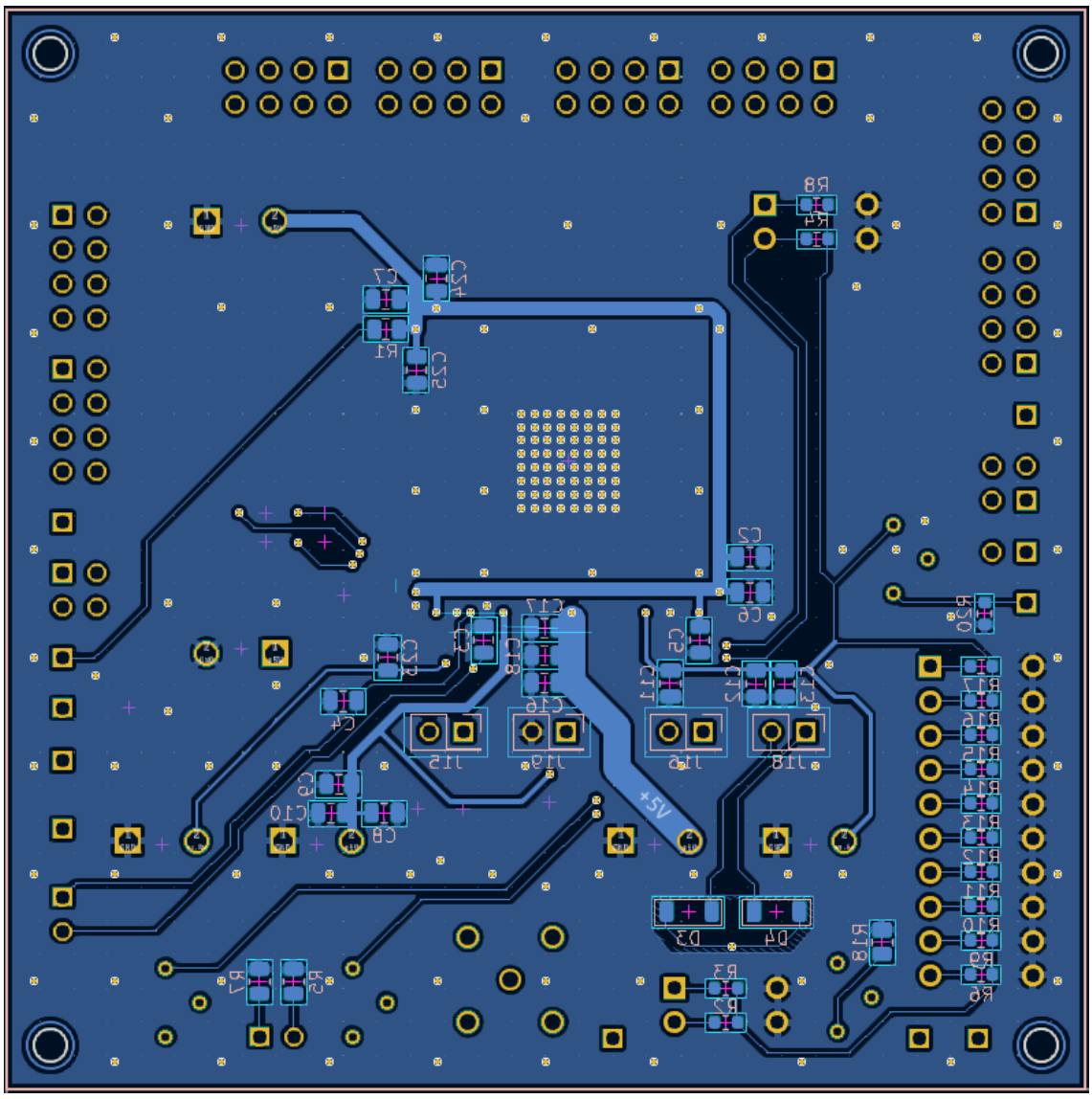


Figure 3.6: Back design scheme of the main PCB in Kicad

Under the chip, a square electrode made with solder paste filled with vias has the function of connecting all the V_{SS} pads of the bonding diagram to GND and also heat dissipation and anchoring.

Connectors J15, J16, J18, J19 are perfectly aligned and they are distant multiples of 2,54 mm from each other just in case there would have been the need to use a millefori to realize the network for the inductors.

3.3 Components

Pin header connector At the PCB periphery are placed the connectors J, which are male pin connectors, to which most of the pads of the chip are connected.

a) b) c)

Figure 3.7: Pin header (male connectors) with different rows and columns

Figure 3.8: Pin header (female connectors)

POW-GND connector Connectors POW are used for external power supply and wires connected to DC generators can be inserted directly and fixed with a screw.

Table 3.1: Power supply connectors list

CONNECTOR	SUPPLY	PURPOSE
POW7	5 V	Power Amplifier non-overlapping clock generator V_{DD}
POW8	5 V	V_{OUT} 5 V monitor (if DCDCOFF=0) or external supply (if DCDCOFF=1)
POW9	1,8 V	Data transmitter V_{DD}
POW10	5 V	Power amplifier V_{DD}
POW11	1,8 V	External 1.8V supply (to be used in case of step-up converter malfunction)
POW17	5 V	V_{DD_ESD}

a) b)

Figure 3.9: POW-GND connector 897-0803

Coaxial connector Connector J31 is a coaxial connector placed for CLK_IN signal, to get a better performance and bandwidth compared to pin connectors.

Figure 3.10: CT4510 BNC female connector

SMD Capacitor The copper 3-sided square line behind the GAMCHAN chip, connected to POW17, has 6 bypass capacitors attached:

Table 3.2: List of bypass capacitor and values

DESIGNATOR	VALUE
C_2	100 pF
C_6	100 nF
C_5	100 µF
C_{25}	100 pF
C_7	100 nF
C_{24}	100 µF

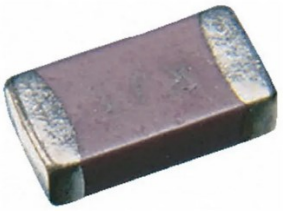


Figure 3.11: Generic SMD Multilayer Ceramic Capacitor

The other bypass capacitors of 100 pF, 100 nF and 100 µF are located on POW7, POW8 and POW10, while the emergency-only POW8 and POW11 have just 1 SMD capacitor of 22 nF. C_{19}, C_{20}, C_{21}, C_{22} are the four flying capacitors needed for the Dickson step-up converter.

C_3 is the rectifier output capacitor (CINUP) and C_1 is the DC-DC converter output capacitor (V_{OUT_5}).

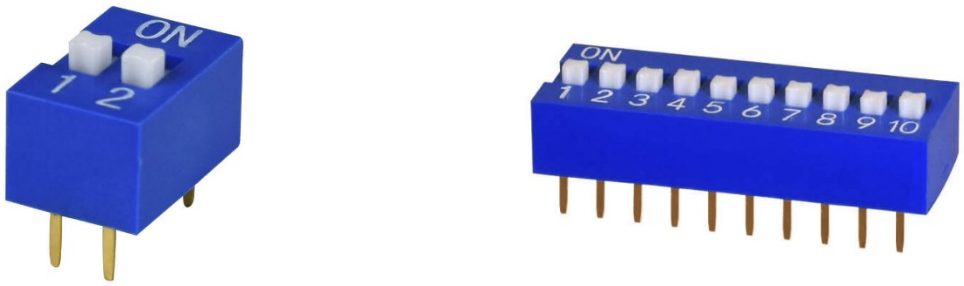
All the SMD capacitors on the PCB use the 0805 [2012 Metric] footprint.

Resistor Variable resistor (trimmer) is used to adjust the value of the resistance needed in order to control currents coming out of the chip from the PMOS of a p-type current mirror, which determine the amplitude of the impulses of the pulse pattern generator. The nominal value of the current at pins 72 and 73 should be 8 µA to have a voltage drop of 1 V at the 130 kΩ SMD resistor placed between connector J27 and GND. Likewise, at pin 76 there should be an 11 µA current to get 1 V between connector J28 and GND.

Figure 3.12: Bourns Inc. 3296Y-1-503LF, 50 kΩ, Through Hole Trimmer

Figure 3.13: Generic SMD resistor

Switch SW1, SW2, SW3 are pull-down DIP switches, used for controllable delay bias control voltage signal. When switches are turned OFF signal is connected to 1,8 V supply through a 10 kΩ resistor and when is turned ON signal is shorted to GND.



a) 2 positions (DS01-254-L-02BE) **b)** 10 positions (DS01C-254-L-10BE)

Figure 3.14: SPST DIP switches s positions (a) and 10 positions (b)

Zener diode 4,7 V and 1,8 V Zener diodes to regulate the voltage across RECTIN and AMPIN, making sure that it does not exceed these values.

Figure 3.15: Zener diode MMSZ4678T1G (1,8) and MMSZ4688T3G (4,7)

AND logic gate Inside the chip is missing an AND gate which synchronizes the digital input data of the neurostimulator with CLK_IN, so it has been necessary

to find some space to place a 1 Channel AND IC Gate which uses a SOT-23-5 footprint. This gate has as inputs A and B the data and clock signals and the output Y goes to the pulse pattern generator inside the chip.

a) AND gate SOT-23-5 package **b)** AND gate pin description

Figure 3.16: Texas Instruments SN74AHC1G08DBVRE4 AND logic gate

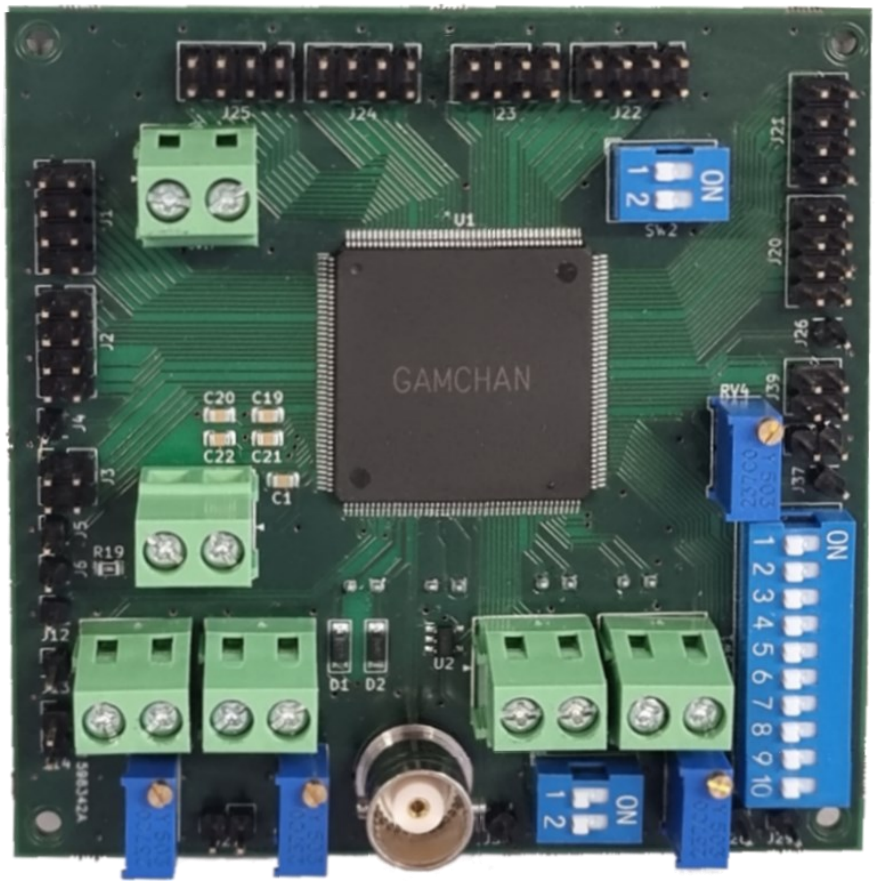


Figure 3.17: Fabricated main PCB with mounted components

3.4 Inductor coil design

3.4.1 Power transmission

Near-field magnetic systems are more efficient than conventional far-field systems, especially for power transmission, since they experience much less energy absorption in a lossy medium.

The goal is to design an LC network on the second PCB such that the inductor resonates with the capacitors at 13,56MHz to increase the efficiency of wireless power transmission.

Considering the inductor network as a two-port model, in order to find the optimum load Z_{Lopt} we resort to matching network theory:

Maximum achievable power efficiency is defined by:

$$\eta = \frac{P_L}{P_L} \tag{3.1}$$

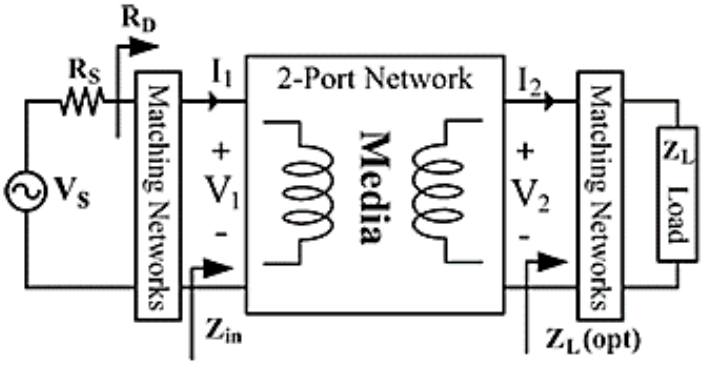


Figure 3.18: 2-Port network model for matching network calculation

It can be shown that the max power efficiency η is:

$$\eta_{max} = \eta_{amp} * \frac{\chi}{(1+\sqrt{1+\chi})^2} \tag{3.2}$$

where η_{amp} is the power amplifier efficiency and:

$$\chi = \frac{|Z_{12}|^2}{Re\{Z_{11}\}Re\{Z_{22}\} - Re\{Z_{12}\}^2} \tag{3.3}$$

The optimum value of the impedance allowing the maximum efficiency is:

$$R_{Lopt} = \frac{\sqrt{(Re\{Z_{11}\}Re\{Z_{22}\} + Im\{Z_{12}\}^2)(Re\{Z_{11}\}Re\{Z_{22}\} - Re\{Z_{12}\}^2)}}{Re\{Z_{11}\}} \tag{3.4}$$

$$B_{Lopt} = \frac{Im\{Z_{12}\}Re\{Z_{12}\} - Im\{Z_{22}\}Re\{Z_{11}\}}{Re\{Z_{11}\}} \tag{3.5}$$

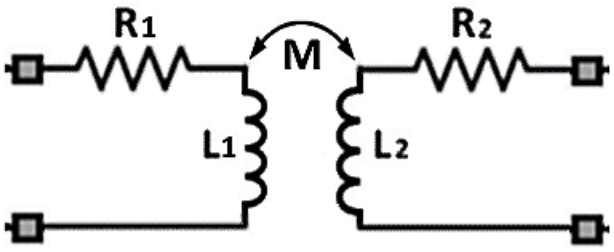


Figure 3.19: Simple model for inductive power transfer

Defining the quality factor Q as:

$$Q = \frac{\omega L}{R} \tag{3.6}$$

From the simple model of fig. 3.19:

$$\chi = \frac{M^2\omega^2}{R_1 R_2} = k^2 Q_1 Q_2 \tag{3.7}$$

$$\eta_{max} = \eta_{amp} * \frac{k^2 Q_1 Q_2}{(1 + \sqrt{1 + k^2 Q_1 Q_2}^2} \tag{3.8}$$

With the above and simplifying the model assuming that the capacitances are cancelled out by the matching network, optimum load becomes:

$$R_{Lopt} \cong R_2 \sqrt{1 + \frac{M^2\omega^2}{R_1 R_2}} = R_2 \sqrt{1 + k^2 Q_1 Q_2} \tag{3.9}$$

$$B_{Lopt} \cong -j\omega L_2 = -jQ_2 R_2 \tag{3.10}$$

So:

$$Z_{Lopt} = R_{Lopt} + B_{Lopt} = R_2 \sqrt{1 + k^2 Q_1 Q_2} - jQ_2 R_2 \tag{3.11}$$

In all these calculations we have assumed no losses but, in reality, these matching networks are not lossless and power transmission can be affected.

It is needed to design the $L_1 - L_2$ matching network in order to maximize power transmission between the two inductors at the target frequency of $f_0 = 13{,}56$ MHz.

Modeling the rectifier equivalent input impedance as a differential circuit made of the parallel of two resistors and capacitor, whose values have been obtained from circuit simulation:

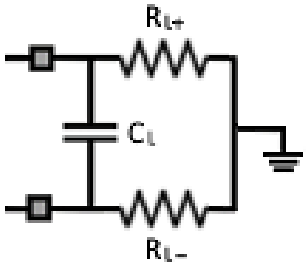


Figure 3.20: Equivalent input impedance of the rectifier

Table 3.3: Component values of fig. 3.20

Component	Value
$\mathbf{R_{L+}}$	22 Ω
$\mathbf{R_{L-}}$	22 Ω
$\mathbf{C_L}$	18 pF

The designed planar spiral coil has as design parameters; metal track width, inter-winding gap, outer inductor diameter (d_{out}), inner inductor diameter (d_{in}) and number of turns.

Inductance of planar spiral printed inductors can be estimated with the modified Wheeler's formula:

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{3.12}$$

Where:

$$d_{avg} = \frac{d_{out} + d_{in}}{2} \tag{3.13}$$

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{3.14}$$

N is the number of turns and $K_1 = 2{,}34$, $K_2 = 2{,}75$ are the constant dimensionless parameters for a square spiral inductor.

Both L_1 and L_2 should have a high Q factor. A reasonable assumption of the parasitic resistances of the coils, keeping into consideration the resistivity of the copper, is $R_1 \cong 1{,}04\,\Omega$, $R_2 \cong 0{,}324\,\Omega$.

This gives an estimation of the Q factor of the two inductors, being

$Q_1 = \frac{2\pi f_0 L_1}{R_1} = 77{,}82 \cong 80$ and $Q_2 = 49{,}96 \cong 50$ respectively [19] [20].

Assuming k_{12} to be equal to 0,03, considering the harshest implant environment, from (3.11) optimal impedance is given by:

$$Z_{Lopt} = R_2\sqrt{1 + k^2 Q_1 Q_2} - jQ_2R_2 = (0{,}694 - j16{,}2)\ \Omega \qquad (3.15)$$

Considering now the two differential load resistances of 22 Ω as an unique resistance of 43,6 Ω, it is required to find a matching network for L_2 that transforms Z_L into Z_{Lopt}:

The output matching network can be calculated via analytical calculations or via simulation. Considering a generic scheme with a series and a parallel reactance:

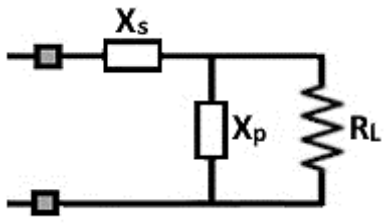


Figure 3.21: Generic scheme of the output matching network

$$Z_{Lopt} = \left(\frac{1}{jX_p} + \frac{1}{R_L}\right)^{-1} + \text{jXs} = \frac{jX_pR_L}{R_L + jX_p} + \text{jXs} =$$
$$= \frac{R_L{X_p}^2}{{R_L}^2 + {X_p}^2} + \frac{j{X_p}{R_L}^2}{{R_L}^2 + {X_p}^2} + \text{jXs} \quad (3.16)$$

$$\frac{R_L{X_p}^2}{{R_L}^2 + {X_p}^2} = 0{,}694\ \Omega \quad (3.17)$$

From which: $|X_p| = 5{,}545\ \Omega$, also:

$$\frac{j{X_p}{R_L}^2}{{R_L}^2 + {X_p}^2} + \text{jXs} = -\text{j}16{,}2\ \Omega \quad (3.18)$$

Both the rectances X_p and X_s can be chosen to be negative so that they correspond to two capacitors. From (3.18):

$X_s = -10{,}743\ \Omega$, $C_{s2} = \frac{1}{\omega_0|X_s|} \cong 1{,}1\ nF$ and $C_{p2} = \frac{1}{\omega_0|X_p|} \cong 2{,}1\ nF$.

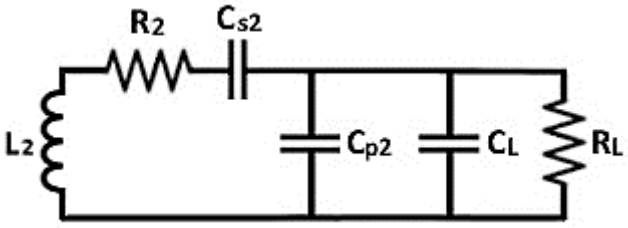


Figure 3.22: Complete output matching network

At input matching network, the equivalent input impedance of the figure below must be equal to the desired load impedance R_d for maximum power transmission.

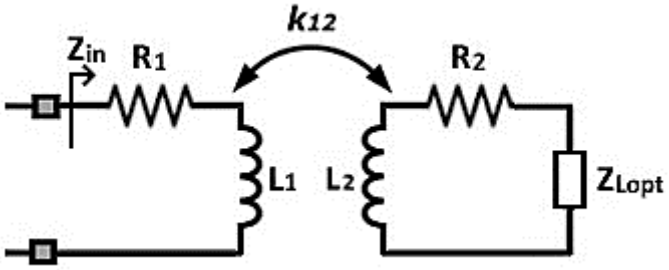


Figure 3.23: Input impedance seen at the input matching network

Simulating the above circuit it's easy to calculate the value of input impedance Z_{in} and of R_d:

$$R_{in} = \frac{V_{in}}{I_{in}} cos\big(\phi(V_{in}) - \phi(I_{in})\big) = 2{,}18\ \Omega \tag{3.19}$$

$$X_{in} = \frac{V_{in}}{I_{in}} sin\big(\phi(V_{in}) - \phi(I_{in})\big) = 80{,}7\ \Omega \tag{3.20}$$

$$L_{in} = \frac{X_{in}}{\omega_0} = 947{,}1\ nH \tag{3.21}$$

$$R_d = 1{,}7\ \Omega \tag{3.22}$$

Assuming $R_{in} \cong R_d$ for simplicity, since its is purely resistive, the input matching network only needs one series capacitor $C_1 = \frac{1}{\omega_0{}^2 L_{in}} = 145\ pF$ to cancel the component X_{in} of input impedance.

Hence the complete design of the power transmission tank:

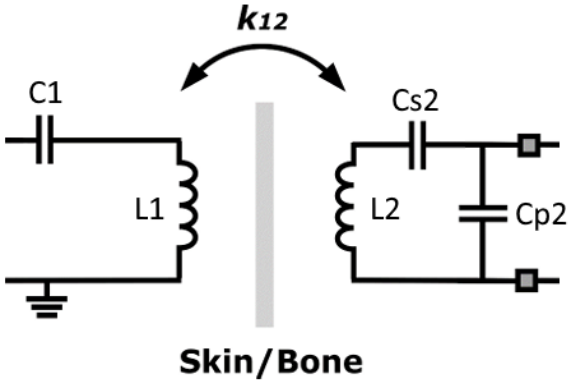


Figure 3.24: Power tank final scheme

3.4.2 Data transmission

For the data, the matching network of a capacitor in parallel with the inductor:

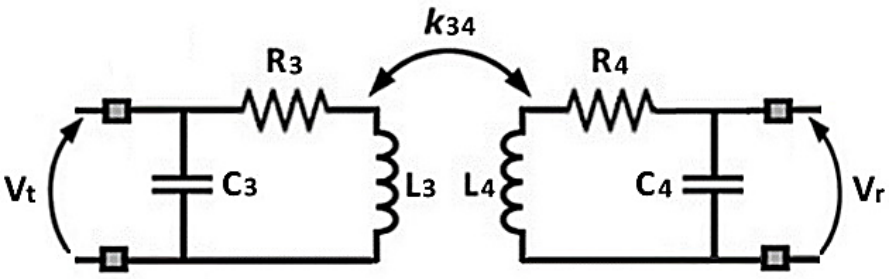


Figure 3.25: Data link equivalent circuit

To simplify equations, assuming that M_{34} does not influence the operation of L_3C_3 tank but only the operation of the L_4C_4 tank, the expression of the current flowing in L_3 can be derived as:

$$I_3 = \frac{V_t}{L_3C_3R_s(s^2 + s\left(\frac{R_3}{L_3} + \frac{1}{C_3R_s}\right) + \frac{1}{L_3C_3} + \frac{R_3}{L_3C_3R_s})} \qquad (3.23)$$

Since $R_s \gg R_3$ the value of the parasitic resistance R_3 can be neglected

The expression of the voltage across C_4, which is the received voltage V_r:

$$V_r = \frac{sM_{34}I_3}{L_4C_4(s^2 + s\left(\frac{R_4}{L_4}\right) + \frac{1}{L_4C_4})} \tag{3.24}$$

So, the complete transfer function between V_t and V_r is:

$$H_{34} = \frac{V_r}{V_t} = \frac{1}{L_3C_3R_s(s^2 + s\left(\frac{1}{C_3R_s}\right) + \frac{1}{L_3C_3})} * \frac{sM_{34}}{L_4C_4(s^2 + s\left(\frac{R_4}{L_4}\right) + \frac{1}{L_4C_4})} \tag{3.25}$$

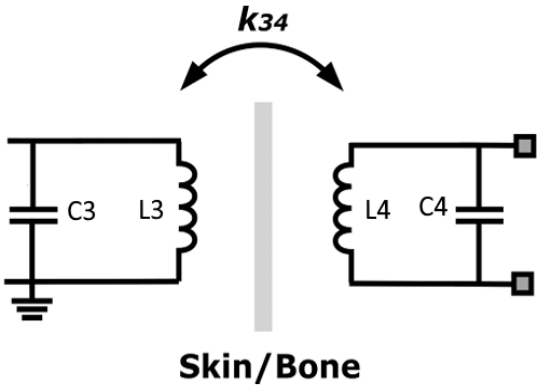


Figure 3.26: Data tank final scheme

Interference of data inductors with power inductors k_{14}, k_{13}, k_{23}, k_{24} should be taken into consideration.

8-shaped inductors present a higher inductance density than traditional square or octagonal inductors with quasi-similar performances and present also interesting parasitic coupling reduction. The shape is made of 2 consecutive twisted loops with a cross-link at the center of the structure [21].

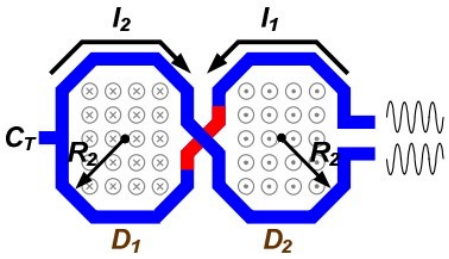


Figure 3.27: 8-shaped inductor

The conventional spiral inductors often cost large chip area and have low Q-factors, resulting in poor phase noise performance. The 8-shaped design achieves a significant increment of the density of integration, self-resonator frequency, and the Q-factors compared to the planar spiral inductor.

In fact, in a conventional spiral inductor the self-inductance in each branch is exactly only 60 % of that of 8-shaped under the same Q factor and diameter [22].

The printed inductors that have been fabricated in the second PCB have the following design obtained by simulation, which reflects the wanted values for all the inductances:

Table 3.4: Inductor final design parameters

	Track width (mm)	**Inter-winding gap (mm)**	**N° of turns**	**Outer inductor diameter (mm)**
L_1	0,75	0,75	5	30
L_2	0,5	0,75	3	15
L_3	0,75	1	1*	34
L_4	0,5	1	1*	19

* 8-shaped layout

3.4.3 Inductor PCBs designed with Kicad

In the first PCB, it has been chosen to place coaxially the inductors of the transmitter (L_1 and L_3), one on the front and the other in the back, whereas in the second section the inductors of the receiver (L_2 and L_4).

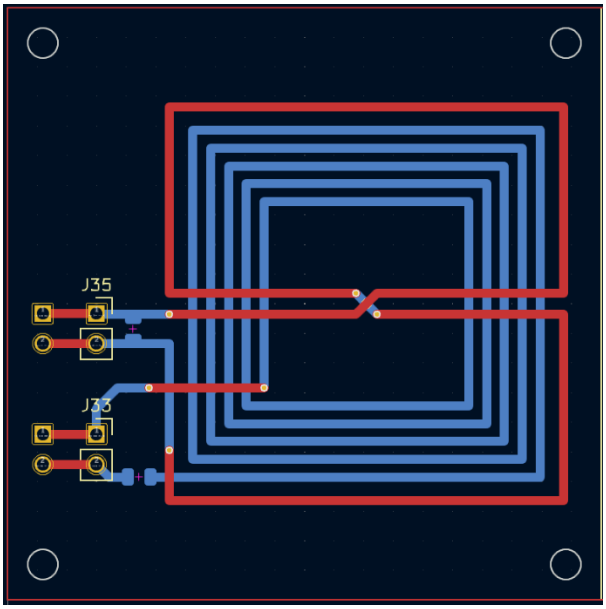


Figure 3.28: Tx printed inductors PCB (L_1, L_3)

Where J33 is the connector of L_1 and J35 is the connector for L_3. Another connector is placed before to monitor the signal with the oscilloscope.

The size of each inductor PCB is 50 x 50 mm.

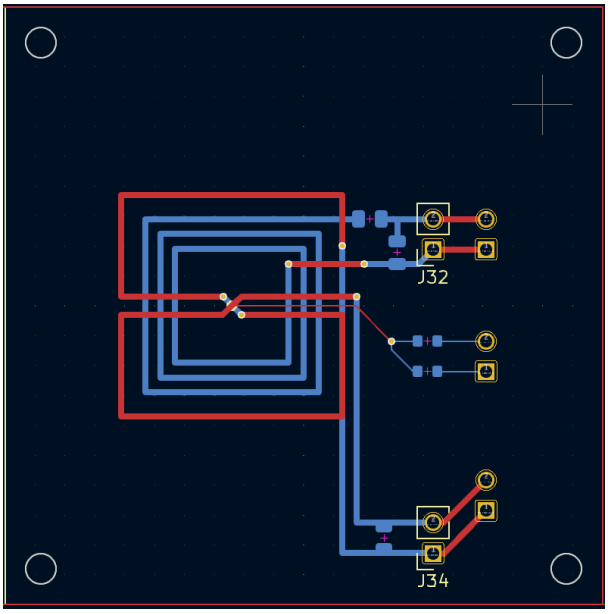
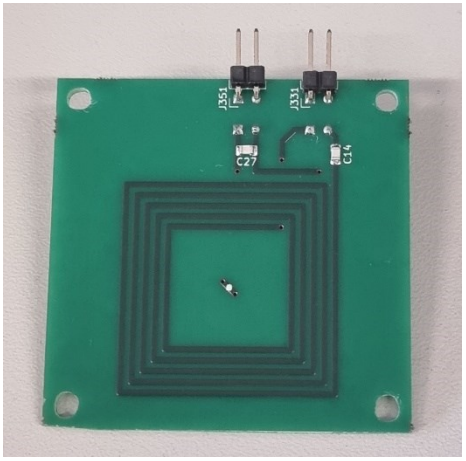


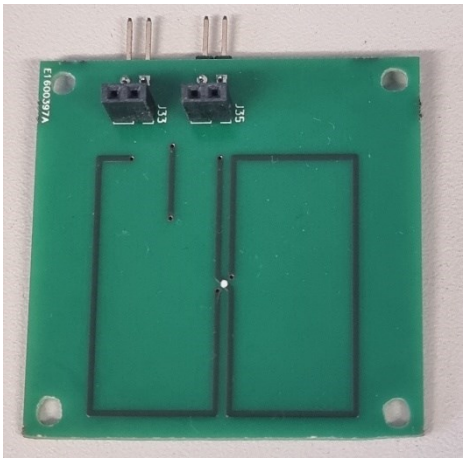
Figure 3.29: Rx printed inductors PCB (L_2, L_4)

Where J32 is the connector of L_2 and J34 is the connector for L_4.

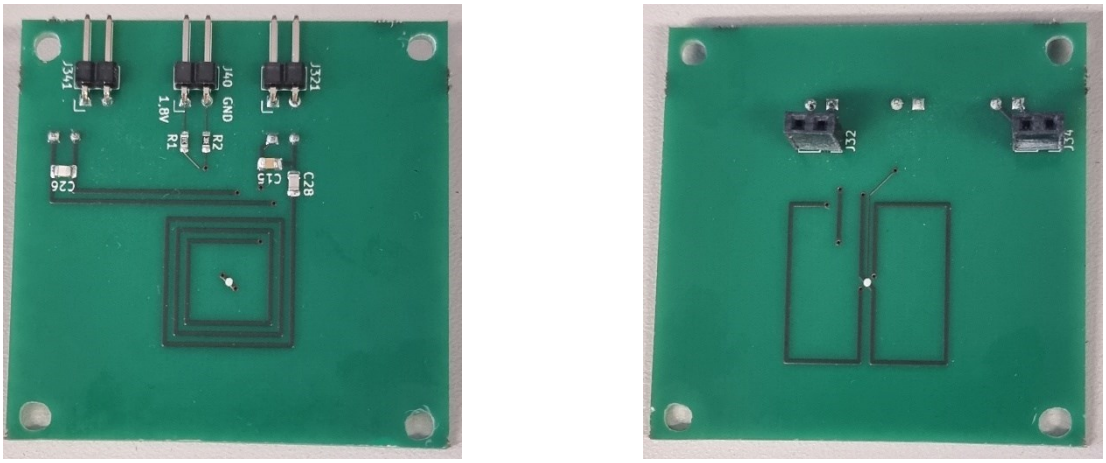
Please note that a resistive voltage divider has been added as a fix to polarize the center of L_4 inductor with 1,2 V to give a DC value to the transistors of the amplifier, since inside the chip is missing a circuit that is able to give this polarization internally.



a) L_1



b) L_3



c) L_2 **d)** L_4

Figure 3.30: Fabricated inductor PCB of Tx (a, b) and Rx (c, d)

Chapter 4: Results

To measure the frequencies the different inductors are tuned at, the waveform generator was connected to the terminals of the inductor PCB. Between the positive terminal of the generator and one terminal of the PCB a 47 Ω series resistance was placed.

An oscilloscope probe was connected to the terminals of the 47 Ω resistor to measure when the voltage had the smallest amplitude, since at the resonance frequency the current that flows in the network, equal to the measured voltage divided by 47 Ω, is minimum.

The measured resonance frequency of L_1C_1 tank was 12,8 MHz instead of the expected 13,56 MHz.

The L_2C_2 tank had two resonances for 11,8 MHz and 13,6 MHz, since 2 capacitors are placed in the network, one in series and one in parallel.

As a final test before testing the PCB with the chip, L_1 and L_2 were placed at a 1 cm distance using 4 PCB spacers to see the optimum trade-off frequency at which the received signal from L_2 was the greatest.

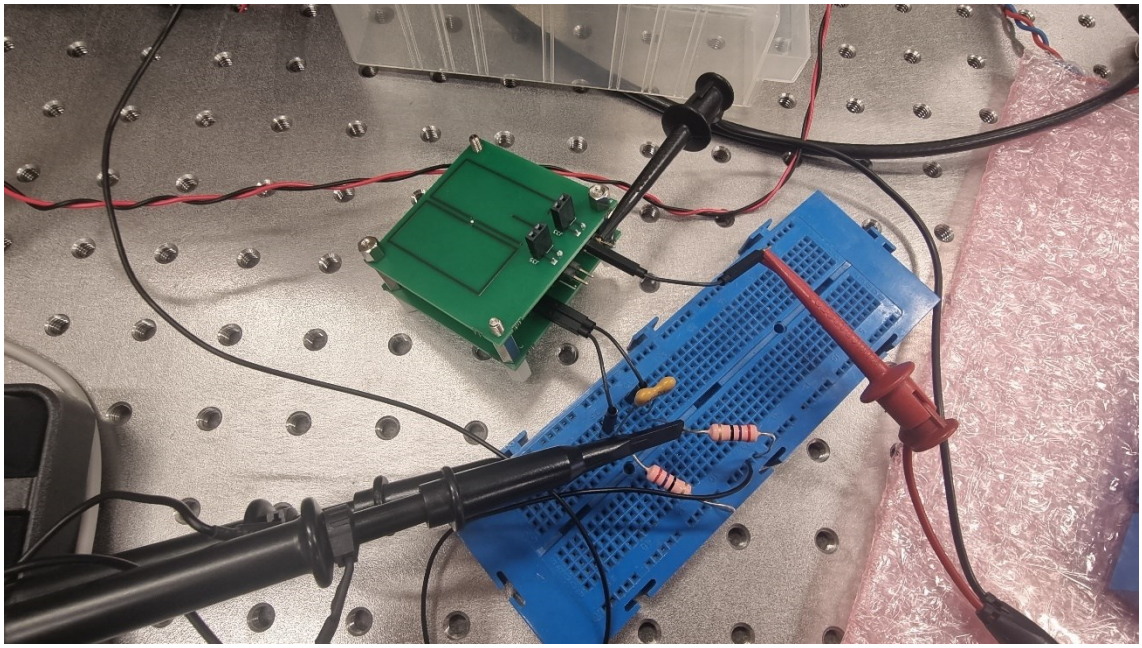


Figure 4.1: Lab setup for measuring L_1-L_2 operating frequency

The load of fig. 3.20, realized using a breadboard, was connected to L_2 and a test sinusoid was applied directly at the terminals of L_1 without a series resistor. Different amplitudes of the sinusoid, from 300 mV up to 1 V, have been tested. Due to the fact that L_1 has a high Q factor, too high amplitudes of the voltage could damage the series capacitor C_1.

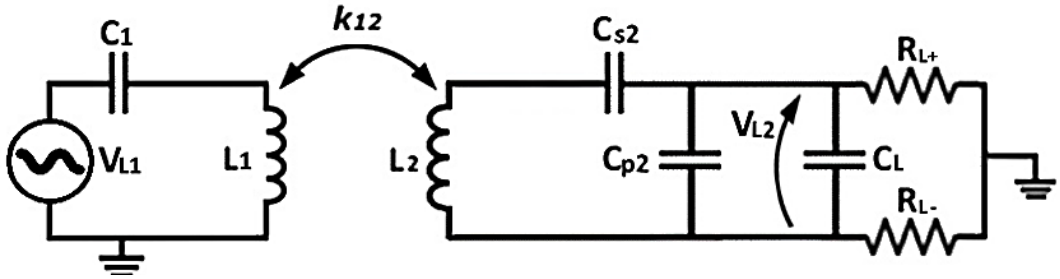


Figure 4.2: Setup scheme for the measurements of tab. 4.1

From these results, varying the frequency, it has been observed that maximum power transfer between L_1 and L_2 occurred at 13,3 MHz for every amplitude of V_{L1}.

For frequencies smaller than 12,8 MHz and bigger than 13,8 MHz the measured amplitude of V_{L2} sinusoid decreased significantly.

Table 4.1: Maximum power transfer measurements

V_{L1} input (Vpp)	**Frequency (MHz)**	**Measured V_{L1} (mVpp)**	**Measured V_{L2} (mVpp)**
300m	12,8	31	64
300m	13,3	67	82
300m	13,8	66	76
600m	12,8	60	115
600m	13,3	129	154
600m	13,8	125	133
1	12,8	95	183
1	13,3	214	247
1	13,8	208	212

At 12,8 MHz (resonance frequency of L_1) measured V_{L1} becomes very small, since the series capacitor C_1 cancels the impedance of the inductor L_1 and the waveform generator only sees a small impedance given mainly by the parasitic resistance of L_1.

This impedance is much smaller than the output resistance of the generator R_s= 50 Ω, so the waveform generator is unable to give the desired value of V_{L1}.

In fact, the Agilent 33250A has a fixed series output impedance of 50 Ω to the front-panel Output connector.

If the actual load impedance is different than the value specified, the displayed amplitude and offset levels will be incorrect.

The same experiment has been done for L_3C_3 and L_4C_4 tanks, which have a resonance at 36 MHz and 33 MHz respectively: this means that the expected optimal frequency for L_3-L_4 data link would be between 33 MHz and 36 MHz.

C_3 is a parallel capacitor and the network of L_3 is a short circuit so, unlike the test of L_1-L_2, it is needed to place a 47 Ω series resistor as a protection.

The voltage V_{L3} will be measured both at the terminals of the generator (before the resistor) and at the terminals of L_3 (after the resistor).

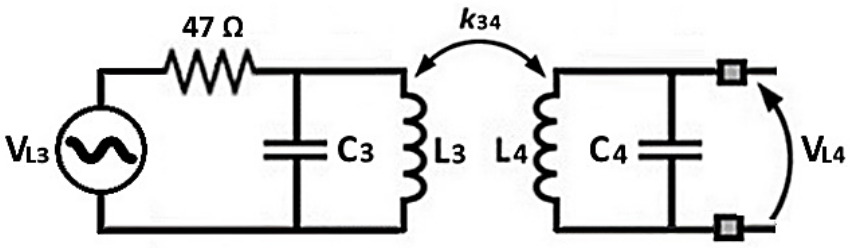


Figure 4.3: Setup scheme for the measurements of tab. 4.2

According to measurements, the following table gives optimal transfer frequency at around 33,5 MHz.

Table 4.2: Maximum data transfer measurements

V_{L3} input (Vpp)	Frequency (MHz)	Measured V_{L3} (Vpp)	Measured V_{C3} (Vpp)	Measured V_{L4} (mVpp)
600 m	33	590 m	493 m	60
600 m	33,5	585 m	480 m	61
600 m	34	585 m	483 m	60
1	33	975 m	795 m	101
1	33,5	965 m	775 m	102
1	34	960 m	780 m	101
2	33	1,97	1,63	190
2	33,5	1,96	1,59	190
2	34	1,98	1,6	188
5	33	4,84	4,12	478
5	33,5	4,82	4,05	480
5	34	4,85	4,08	470

4.1 Power transmission results

To test the chip, an output of the Agilent E3631A DC generator was connected to POW17 (V_{DD_ESD}). After that the voltage was slowly increased to 5 V in order to make sure that the absorbed current did not exceed 10 μA, since this would be a clear indication of malfunctioning.

The second output (V_{DD}) was connected to POW7 ($V_{DD\_CLK\_IN}$) and POW10 (V_{DD_PA}) and the waveform generator was connected to the coaxial connector J31 (CLK_IN) to generate a 13,3 MHz square wave with $V_{high}=V_{DD}$ and $V_{low}=0$ V. V_{DD} was initially set to 0. The GND of the circuit was connected to the chassis of the DC generator.

The inductors L_1 and L_2 were placed at an initial distance of d=1 cm and connected to the main PCB. Before connecting the receiver PCB, the circuit of fig. 3.20, which represents the equivalent input impedance of the rectifier, was connected to the output of L_2 and the differential voltage seen at the terminal of the 18 pF capacitor was measured to determine which amplitude of V_{DD} was the minimum required to obtain a stable sinusoid at the output of L_2.

It has been observed that for V_{DD} =2 V the output sinusoid was highly unstable. For V_{DD}>2 V signal gained more stability but the minimum voltage for correct PA operation was observed to be V_{DD}=4 V. Tab reports the amplitudes of V_{L2} measured for different values of d for V_{DD}=4 V.

Table 4.3: Measured power transfer with only the Tx PCB connected

d (cm)	Measured V_{L2} (Vpp)
1	4,44
1,5	3,82
2	3,5
2,5	2,7
3	1,9

The measured data gives an idea of how signals are transmitted by the inductors. Finally, the Rx PCB was connected to L_2 and powered only with V_{DD_ESD} for component safety.

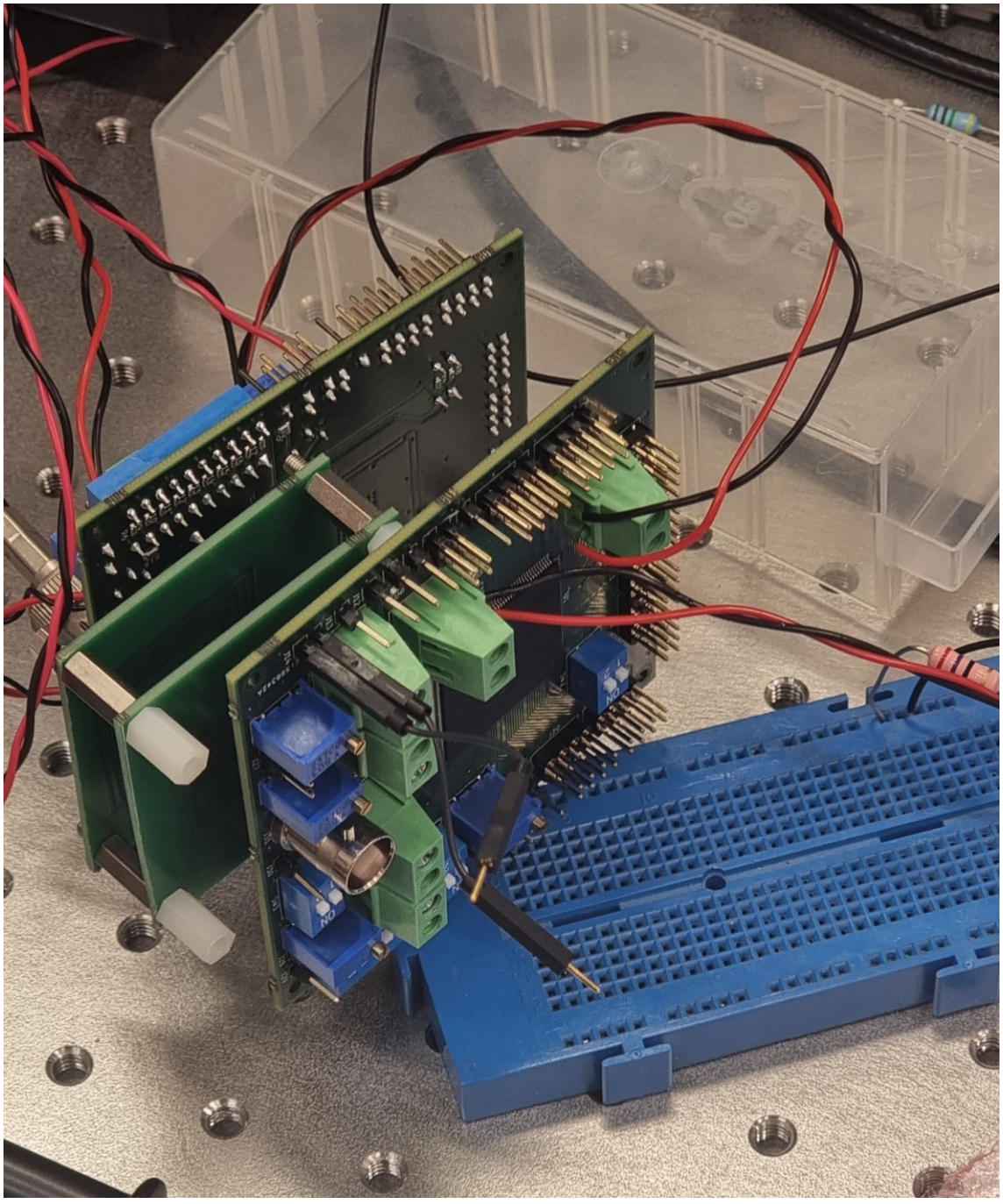
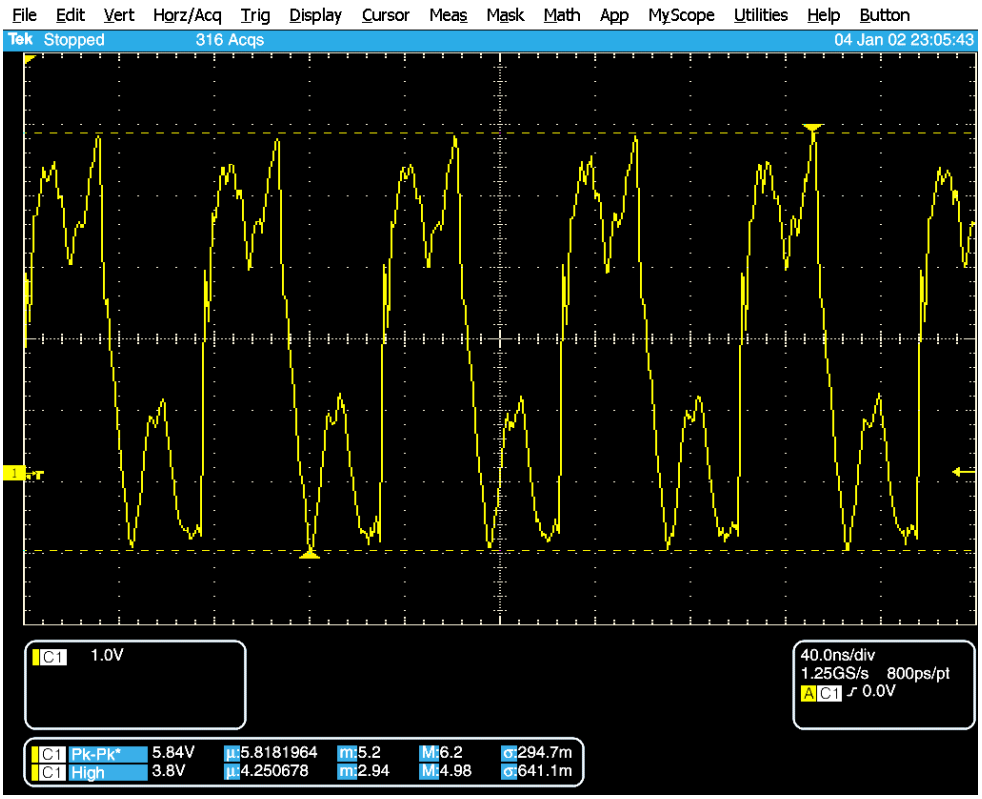


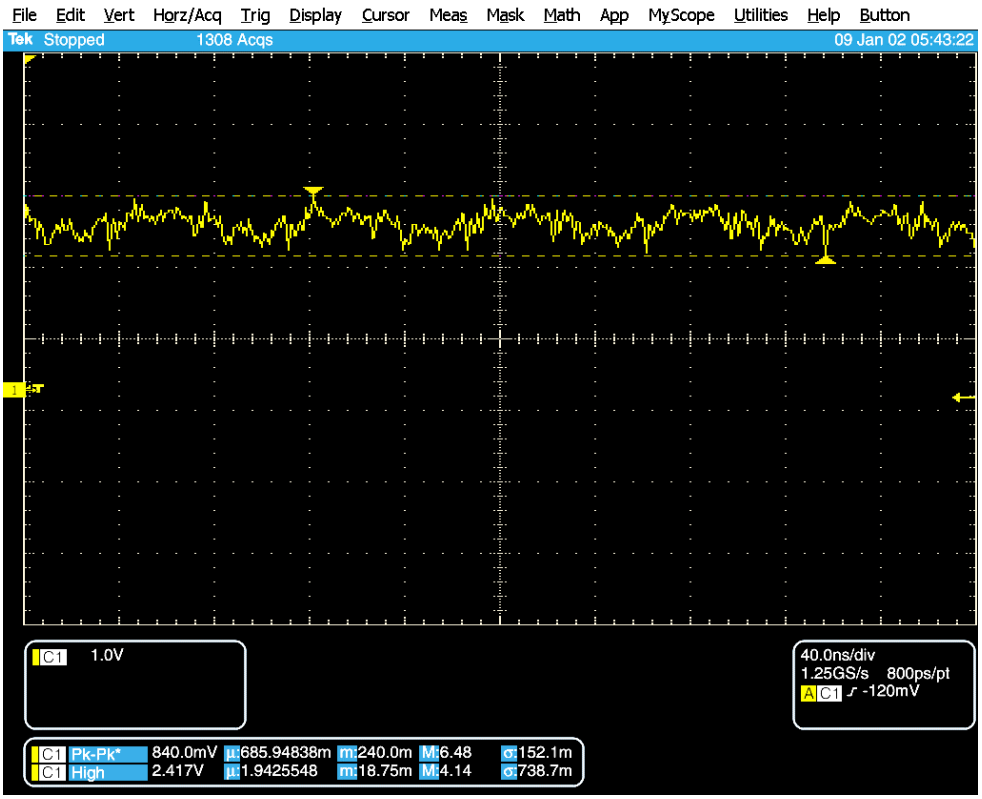
Figure 4.4: Lab setup for the measurement with both the Tx and Rx PCB

With d=1 cm, the oscilloscope probe was placed on the connectors corresponding to the output of the PA (PA_OUT), the input and output of the rectifier (V_{rectin}, V_{cinup}) and the output of DC-DC converter (V_{OUT_5}).

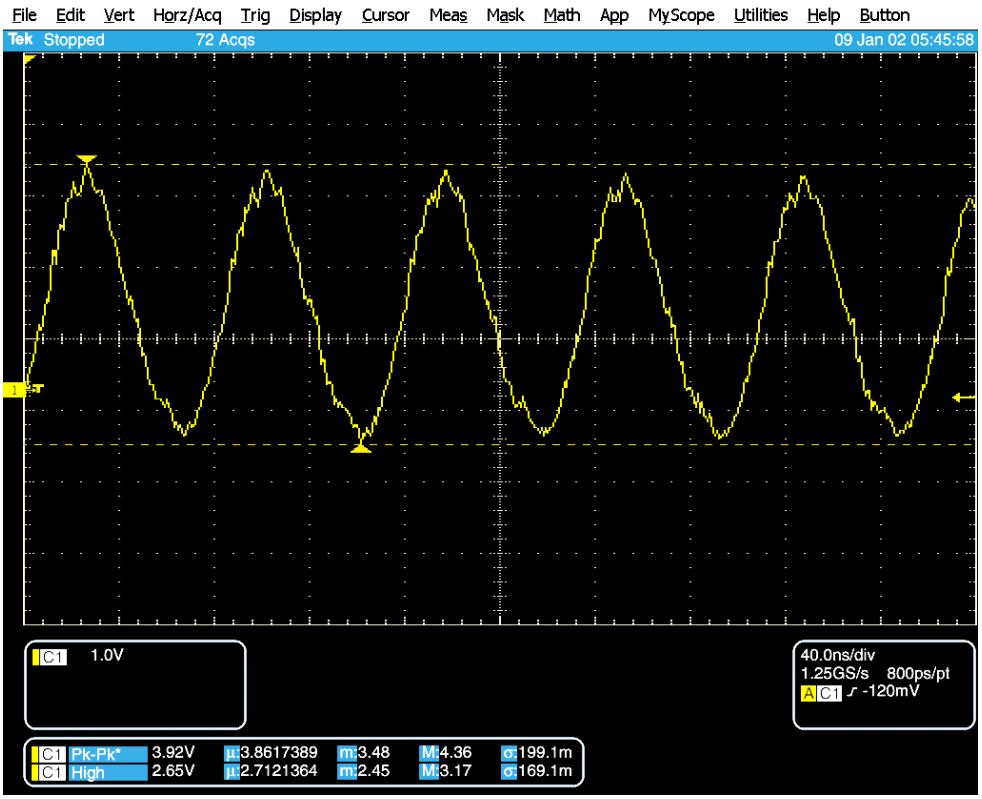
The concave voltage spikes on the high level on fig 4.5a) are due to the charge of PMOS of the output stage of Pa and the ones on the low level of the wave are due to the NMOS.



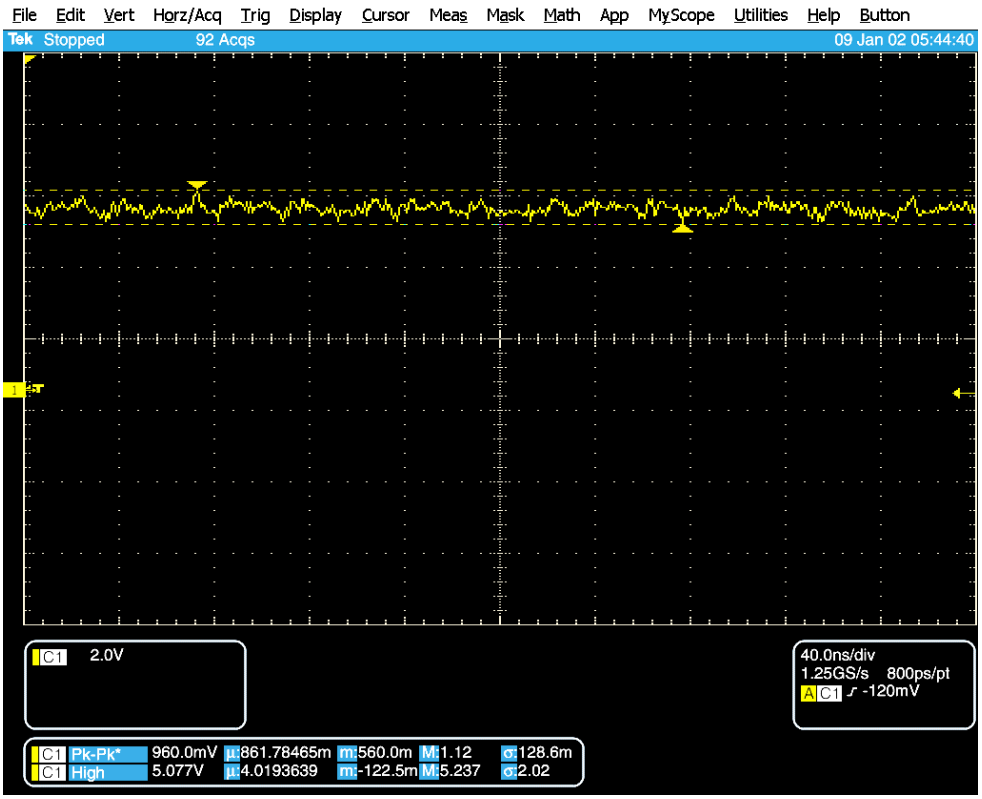
a) PA_OUT



b) V_{cinup}



c) V_{rectin} (taken single endedly)



d) V_{OUT_5}

Figure 4.5: Results of power transmission on the complete setup Tx-Rx

The above has been repeated for d=1,5 cm, d=2 cm, d=2,5 cm, d=3 cm. It has been observed that, increasing d, the signal received from the rectifier is weaker, but the DC-DC converter is still able to bring the voltage received from the rectifier to 5 V up to d=2,5 cm.

On the other hand, for d=3 cm the input voltage of the converter is insufficient to raise the voltage up to 5 V as it only gives that V_{OUT_5} is equal to 2 V.

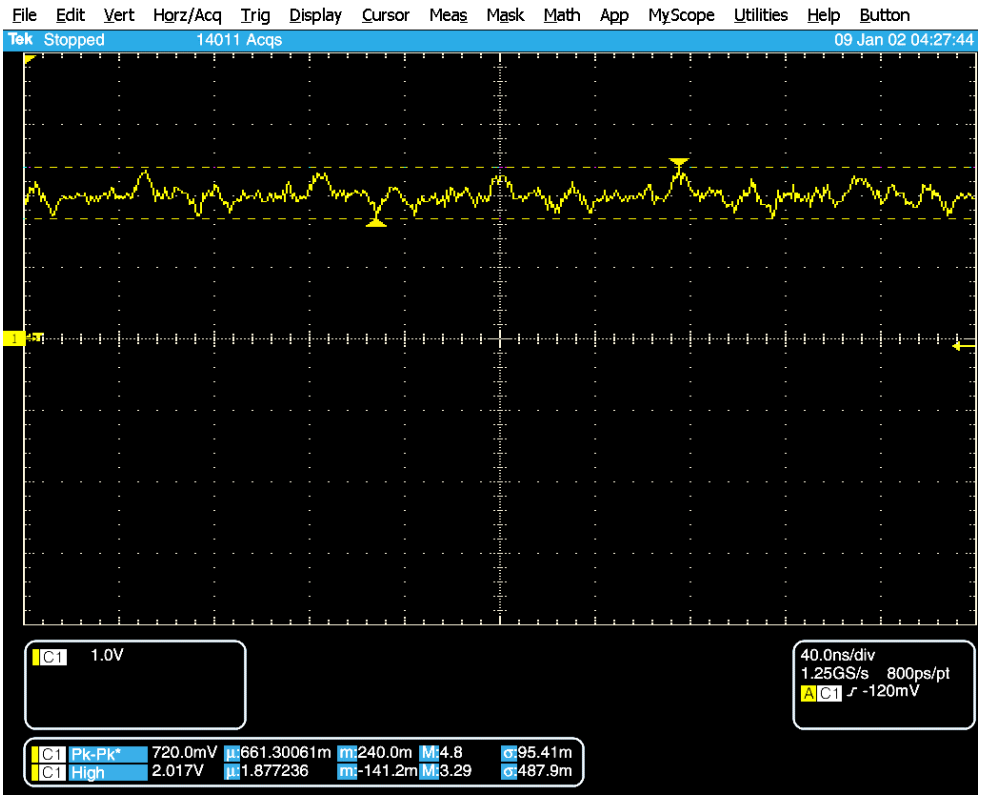


Figure 4.6: V_{OUT_5} at d=3 cm

4.2 Data transmission results

The following table gives an estimation of the interference of power transmitter inductor L_1 on data receiver inductor L_4:

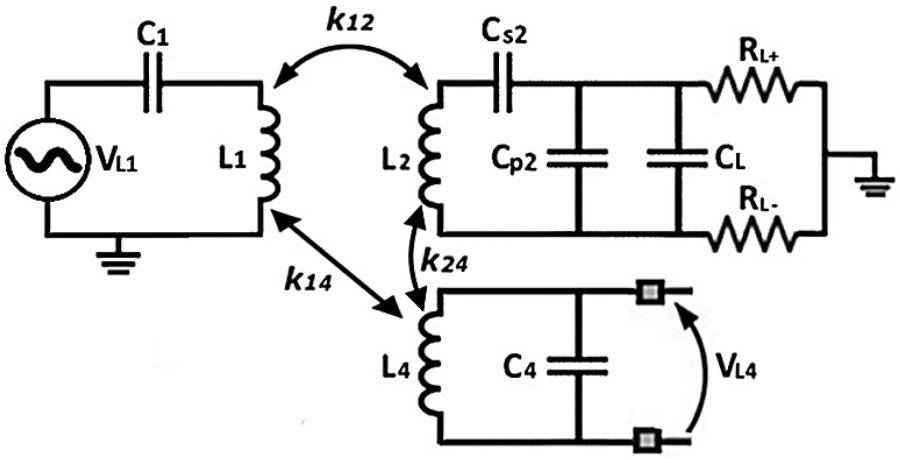


Figure 4.7: Setup scheme for measuring power carrier interference on L_4C_4 data tank

Table 4.4: Measurements of power carrier interference on L_4C_4 data tank

V_{L1} input (Vpp)	Measured V_{L1} (Vpp)	Measured V_{L4} (mVpp)	d (cm)
1	580 m	60	1
1	265 m	20	2
2	1,11	113	1
2	500 m	36	2
4	2,12	216	1
4	1	71	2
5	2,64	268	1
5	1,24	87	2

For testing the pulse pattern generator of data transmitter, a random data signal made with a 20% duty cycle 1 MHz square wave with amplitude V_{DD}=5 V was tested.

For the moment, CLK_IN will be set to a constant DC value of 5 V for debug reasons, so that the output of the AND gate is equal to the data signal.

Coupling the oscilloscope in AC and measuring SINGLE ENDEDLY the voltage of L+/- across L_3, the pulse sequence of fig. 4.8 was obtained.

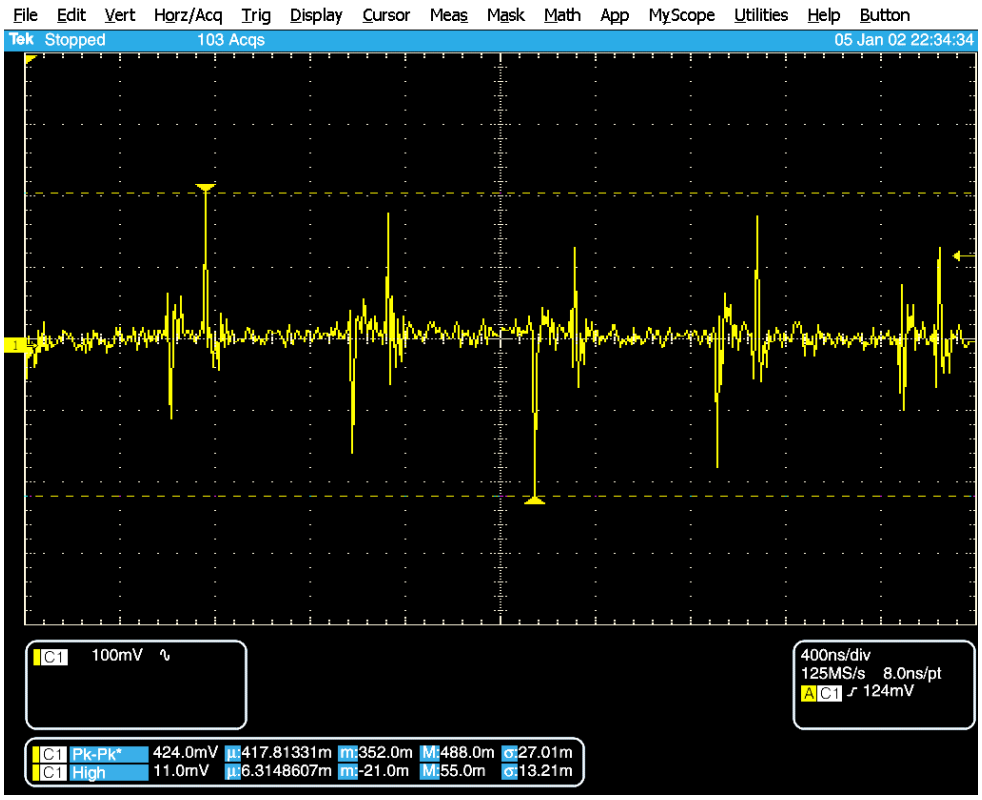


Figure 4.8: Single ended test measurement of L+/L- with CLK_IN=5 V

Zooming fig. 4.8, it can be seen that the pulses have oscillations with period t_{osc}=11,4 ns.

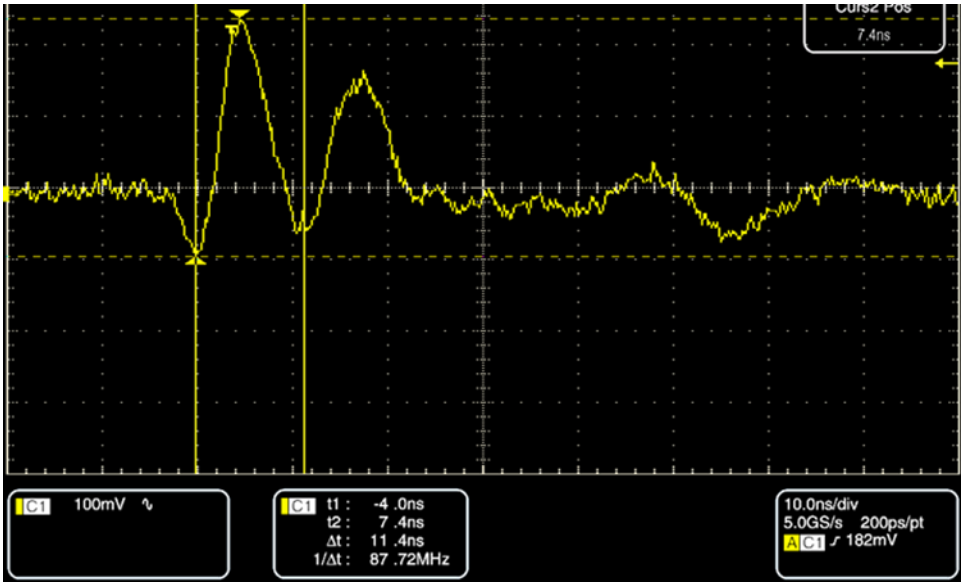
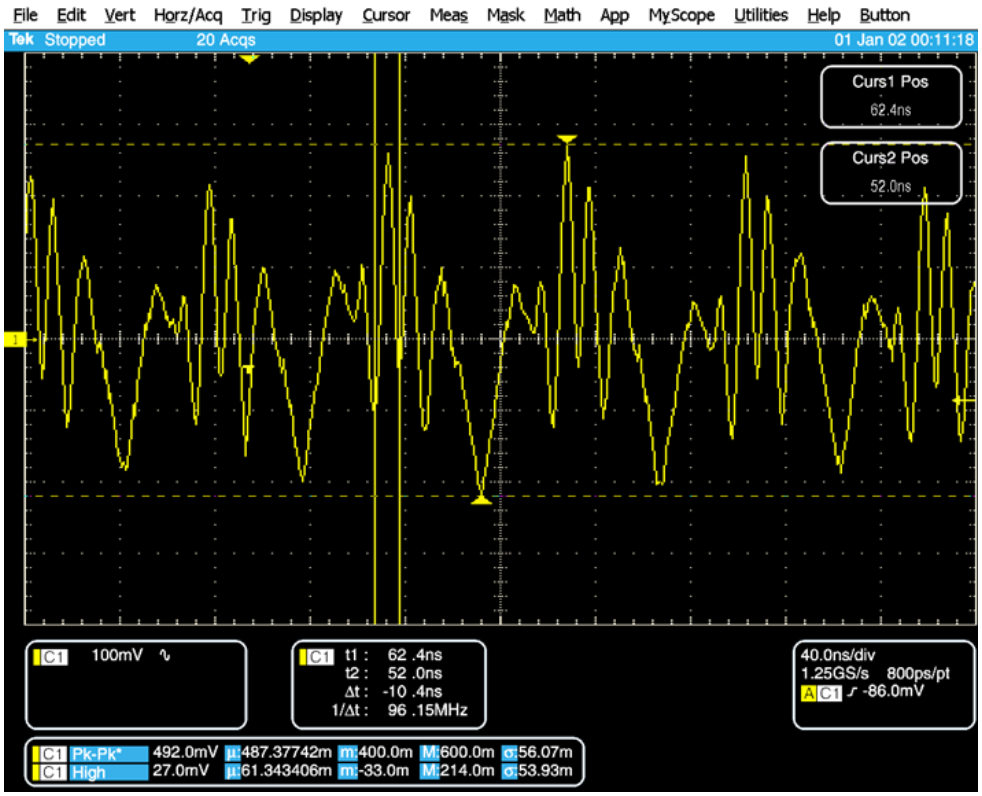
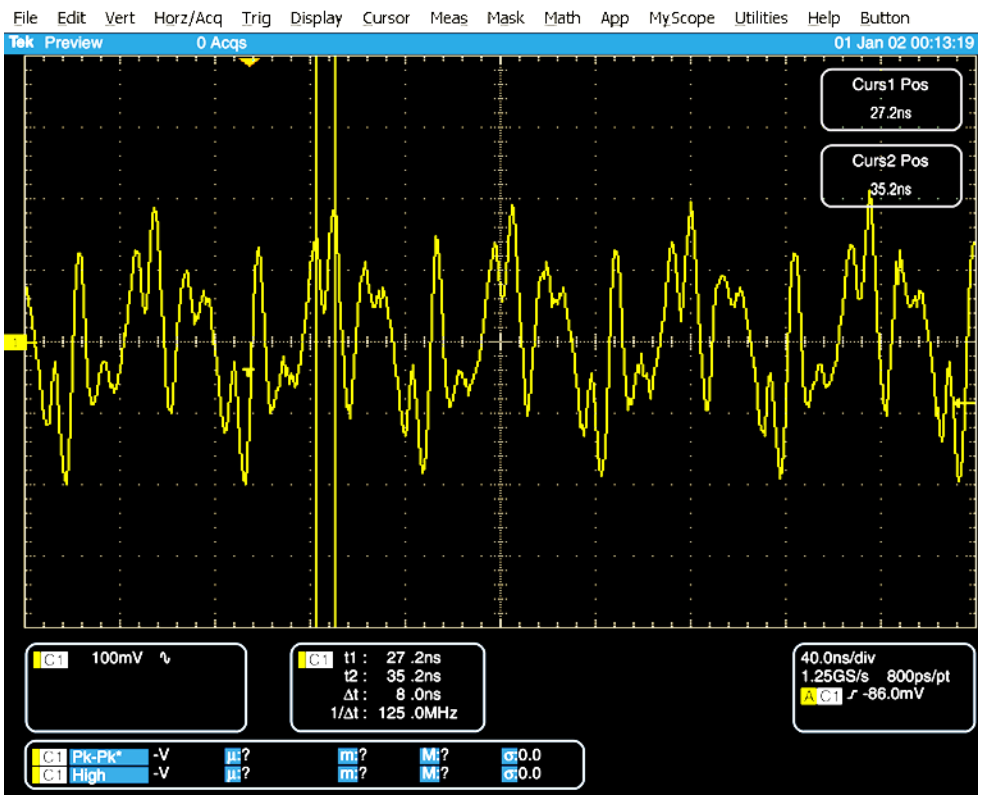


Figure 4.9: Zoom of fig. 4.8

The measurement was repeated setting both CLK_IN and Input data to a 13,3 MHz square wave. Duty cycle of input data was varied between 20 and 50%:



a)



b)

Figure 4.10: Single ended measurement of L+/L- with input data duty cycle 20% (a) and 50% (b)

As a final test, the complete setup Tx-Rx PCB like in fig. 4.4 was mounted to measure the input of the data amplifier (Ampin+/-).

The Tx was powered with V_{DD_ESD} (5 V), Power Amplifier non-overlapping clock generator V_{DD} (5 V), Data transmitter V_{DD} (1,8 V), Power amplifier V_{DD} (5 V) and the Rx only with V_{DD_ESD}.

As before, CLK_IN was a 13.3 MHz square wave and the input data was a 13.3 MHz square wave with 20% duty cycle.

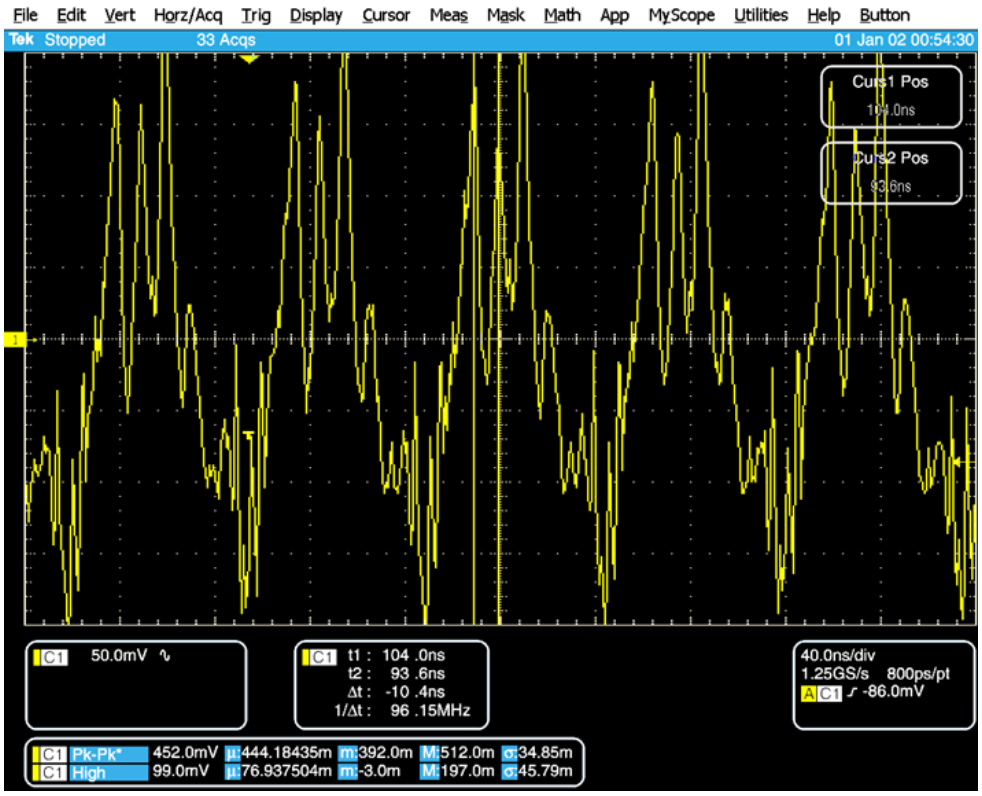


Figure 4.11: Single ended measurement of Ampin+/- with input data duty cycle 20%

Chapter 5: Conclusion

The results of this thesis continued the previous work conducted at Seoul National University by the PhD students Hyunbeen Jeong and Jisung Kim and tested the feasibility of the proposed ASIC with reduced power consumption and health risks.

Much remains unknown on the role of the cerebellum in different psychopathologies and further clinical research is warranted to establish the potential of cerebellar neurostimulation in clinical practice.

In order to test and confirm the correct operation of the electrodes of the neurostimulator and the productiveness of stimulating neurons, ex-vivo and in vivo tests are required. Moreover, electrodes must be realized using inorganic materials which are insoluble when exposed to body fluids to ensure a long lifetime of the artificial retina.

Future developments may include minimizing the power consumption to simplify the system complexity and lessen the tissue damage, optimizing power and area consumption in the ASIC design and information of bit error rate (BER).

Also, the fabrication and designing of the proper coil for wireless operation should be continued in the future to have long-term reliability and to find an optimal post-process shaping technique for inserting it in the eye avoiding post operative infection problems: a good solution would be to insert the intraocular part of the device into the eyeball through a minimal hole in the pars plana and nearby area.

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Appendix A

In this appendix is reported a more detailed list of the chip input/output pads with the description.

Table A.1: Pad names and description

PIN	NAME	DESCRIPTION	INPUT/ OUTPUT	SIGNAL TYPE
3	VDD_ESD	VDD_ESD 5V	I	P, 5V
4	ELE16	Electrode pad n. 16	O	A, Current
5	ELE15	Electrode pad n. 15	O	A, Current
6	ELE14	Electrode pad n. 14	O	A, Current
7	ELE13	Electrode pad n. 13	O	A, Current
8	ELE12	Electrode pad n. 12	O	A, Current
9	ELE11	Electrode pad n. 11	O	A, Current
10	ELE10	Electrode pad n. 10	O	A, Current
11	ELE09	Electrode pad n. 9	O	A, Current
12	VSS	GND	-	P, GND
13	ELE08	Electrode pad n. 8	O	A, Current
14	ELE07	Electrode pad n. 7	O	A, Current
15	ELE06	Electrode pad n. 6	O	A, Current
16	ELE05	Electrode pad n. 5	O	A, Current
17	ELE04	Electrode pad n. 4	O	A, Current
18	ELE03	Electrode pad n. 3	O	A, Current
19	ELE02	Electrode pad n. 2	O	A, Current

20	ELE01	Electrode pad n. 1	O	A, Current
21	VSS	GND	-	P, GND
22	REF	Reference electrode for the electrode array	O	A, Current
23	REF	Reference electrode for the electrode array	O	A, Current
24	B_gDAC_1_2	Bit 1 (weight 2^1) of global DAC	O	D, 5V
25	B_gDAC_1_3	Bit 2 (weight 2^2) of global DAC	O	D, 5V
26	B_gDAC_1_4	Bit 3 (weight 2^3) of global DAC	O	D, 5V
27	SYNC_FLAG	Control Unit flag: synchronization achieved when HIGH	O	D, 5V
28	IOUT_FLAG	Copy of the gDAC's reference current (nom. 5.33uA) monitor	O	A, Current
29	VSS	GND	-	P, GND
30	FLY4DN	Flying capacitor CF4 bottom plate	O	A, 5V
31	FLY3DN	Flying capacitor CF3 bottom plate	O	A, 5V
32	FLY2DN	Flying capacitor CF2 bottom plate	O	A, 5V
33	FLY1DN	Flying capacitor CF1 bottom plate	O	A, 5V
34	FLY4UP	Flying capacitor CF4 top plate	O	A, 5V
35	FLY3UP	Flying capacitor CF3 top plate	O	A, 5V
36	FLY2UP	Flying capacitor CF2 top plate	O	A, 5V
37	FLY1UP	Flying capacitor CF1 top plate	O	A, 5V
38	DCDCOFF	Active-high DCDC step up converter turn-off signal (1: converter OFF; 0: converter ON)	I	A, 5V
39	VOUT_5	VOUT 5V monitor (DCDCOFF=0) or external supply (DCDCOFF=1)	I/O	A, 5V
40	VOUT_5		I/O	A, 5V
41	VSS	GND	-	P, GND
42	VDD_ESD	VDD_ESD 5V	I	P, 5V

47	VDD_ESD	VDD_ESD 5V	I	P, 5V
48	VSS	GND	-	P, GND
49	VOUT_1.8V	VOUT 1.8V monitor or external supply	I/O	A, 1.8V
50	EX_VIN+	External 1.8V supply to be used in case of step-up converter malfunction	I	P, 1.8V
51	EX_CLK_VIN+	External 1.8V clock to be used in case of step-up converter malfunction	I	A, 1.8V
52	VREF	DCDC converter reference voltage, generated internally by a scaled band-gap generator.	O	A, 1.8V
53	CINUP (Vrect)	Rectified voltage check	I/O	A, 5V
54	VSS	GND	-	P, GND
55	RECTIN+	Rectifier input	I	A, sin, 5V
56	RECTIN-	Rectifier input	I	A, sin, 5V
57	VDD_CLK_IN	Power Amplifier non overlapping clock generator VDD	I	P, 5V
58	CLK_IN	Power Amplifier input clock	I	D, 5V
59	VSS	GND	-	P, GND
60	VSS	GND	-	P, GND
61	VSS	GND	-	P, GND
62	VSS	GND	-	P, GND
63	PA_OUT, A	Power transmitter output	O	A, sin, 100Vpp
64	PA_OUT, A	Power transmitter output	O	A, sin, 100Vpp
65	VDD_PA (5V, A)	Power amplifier VDD	I	P, 5V
66	VDD_PA (5V, A)	Power amplifier VDD	I	P, 5V
67	VDD_PA (5V, A)	Power amplifier VDD	I	P, 5V
68	VSS	GND	-	P, GND
69	VSS	GND	-	P, GND
70	VDD_TX (1.8V, A)	Data transmitter VDD	I	P, 1.8V
71	D_TX_IN (was CLK_IN, datain)	Data transmitter data input signal	I	D, 5V

72	I1U_F	Controllable delay bias current (nom. 8uA). Pad goes to a diode-connected pMOSFET	I	Current, 1.8V
73	I1U_C	Controllable delay bias current (nom. 8uA). Pad goes to a diode-connected pMOSFET	I	Current, 1.8V
74	D2_TX	Controllable delay control voltage signal	I	D, 1.8V
75	D1_TX	Controllable delay control voltage signal	I	D, 1.8V
76	I1U_F2	Controllable delay bias current (nom. 11uA). Pad goes to a diode-connected pMOSFET	I	Current, 1.8V
77	SM	Transmitting data pulse chain check	O	D, 1.8V
78	VDD_TX (1.8V, A)	Data transmitter VDD (Connected to 70)	I	P, 1.8V
79	L-	Data transmitter tank input	O	A, 1.8V
80	L+	Data transmitter tank input	O	A, 1.8V
81	VSS	GND	-	P, GND
82	AMPIN-	Data receiver amplifier input	I	A, sin, 1.8V
83	AMPIN+	Data receiver amplifier input	I	A, sin, 1.8V
84	D1	Controllable delay switch: D1=0, bypass coarse delay; D1=1 insert coarse delay	I	D, 1.8V
85	D2	Controllable delay switch: D2=0, bypass fine delay; D1=1 insert fine delay	I	D, 1.8V
86	VDD_ESD	VDD_ESD 5V	I	P, 5V
91	VDD_ESD	VDD_ESD 5V	I	P, 5V
92	I1	Controllable delay bias control voltage signal	I	D, 1.8V
93	I2	Controllable delay bias control voltage signal	I	D, 1.8V
94	I3	Controllable delay bias control voltage signal	I	D, 1.8V
95	I4	Controllable delay bias control voltage signal	I	D, 1.8V
96	I5	Controllable delay bias control voltage signal	I	D, 1.8V
97	I11	Controllable delay bias control voltage signal	I	D, 1.8V
98	I12	Controllable delay bias control voltage signal	I	D, 1.8V
99	I13	Controllable delay bias control	I	D, 1.8V

		voltage signal		
100	I14	Controllable delay bias control voltage signal	I	D, 1.8V
101	I15	Controllable delay bias control voltage signal	I	D, 1.8V
102	VREF_COMP	Data recovery comparator reference voltage input	I	A, 1.8V
103	VSS	GND	-	P, GND
104	RX_CLK	Data recovery clock signal check	O	D, 1.8V
105	RX_DIN	Data recovery data signal check	O	D, 1.8V
106	EXT_POR	Digital circuit control signal	I	D, 1.8V
107	EXT_SEL	Digital circuit control signal	I	D, 1.8V
108	EXT_CLK	Digital circuit control signal	I	D, 1.8V
109	EXT_DIN	Digital circuit control signal	I	D, 1.8V
110	REF	Reference electrode for the electrode array	O	A, Current
111	REF	Reference electrode for the electrode array	O	A, Current
112	VSS	GND	-	P, GND
113	ELE64	Electrode pad n. 64	O	A, Current
114	ELE63	Electrode pad n. 63	O	A, Current
115	ELE62	Electrode pad n. 62	O	A, Current
116	ELE61	Electrode pad n. 61	O	A, Current
117	ELE60	Electrode pad n. 60	O	A, Current
118	ELE59	Electrode pad n. 59	O	A, Current
119	ELE58	Electrode pad n. 58	O	A, Current
120	ELE57	Electrode pad n. 57	O	A, Current
121	VSS	GND	-	P, GND
122	ELE56	Electrode pad n. 56	O	A, Current
123	ELE55	Electrode pad n. 55	O	A, Current
124	ELE54	Electrode pad n. 54	O	A, Current
125	ELE53	Electrode pad n. 53	O	A, Current
126	ELE52	Electrode pad n. 52	O	A, Current

127	ELE51	Electrode pad n. 51	O	A, Current
128	ELE50	Electrode pad n. 50	O	A, Current
129	ELE49	Electrode pad n. 49	O	A, Current
130	VDD_ESD	VDD_ESD 5V	I	P, 5V
135	VDD_ESD	VDD_ESD 5V	I	P, 5V
136	VSS	GND	-	P, GND
137	ELE48	Electrode pad n. 48	O	A, Current
138	ELE47	Electrode pad n. 47	O	A, Current
139	ELE46	Electrode pad n. 46	O	A, Current
140	ELE45	Electrode pad n. 45	O	A, Current
141	ELE44	Electrode pad n. 44	O	A, Current
142	ELE43	Electrode pad n. 43	O	A, Current
143	ELE42	Electrode pad n. 42	O	A, Current
144	ELE41	Electrode pad n. 41	O	A, Current
145	VSS	GND	-	P, GND
146	ELE40	Electrode pad n. 40	O	A, Current
147	ELE39	Electrode pad n. 39	O	A, Current
148	ELE38	Electrode pad n. 38	O	A, Current
149	ELE37	Electrode pad n. 37	O	A, Current
150	ELE36	Electrode pad n. 36	O	A, Current
151	ELE35	Electrode pad n. 35	O	A, Current
152	ELE34	Electrode pad n. 34	O	A, Current
153	ELE33	Electrode pad n. 33	O	A, Current
154	VSS	GND	-	P, GND
155	VSS	GND	-	P, GND
156	ELE32	Electrode pad n. 32	O	A, Current
157	ELE31	Electrode pad n. 31	O	A,

				Current
158	ELE30	Electrode pad n. 30	O	A, Current
159	ELE29	Electrode pad n. 29	O	A, Current
160	ELE28	Electrode pad n. 28	O	A, Current
161	ELE27	Electrode pad n. 27	O	A, Current
162	ELE26	Electrode pad n. 26	O	A, Current
163	ELE25	Electrode pad n. 25	O	A, Current
164	VSS	GND	-	P, GND
165	ELE24	Electrode pad n. 24	O	A, Current
166	ELE23	Electrode pad n. 23	O	A, Current
167	ELE22	Electrode pad n. 22	O	A, Current
168	ELE21	Electrode pad n. 21	O	A, Current
169	ELE20	Electrode pad n. 20	O	A, Current
170	ELE19	Electrode pad n. 19	O	A, Current
171	ELE18	Electrode pad n. 18	O	A, Current
172	ELE17	Electrode pad n. 17	O	A, Current
173	VSS	GND	-	P, GND
174	VDD_ESD	VDD_ESD 5V	I	P, 5V