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Industrial Engineering Department

Master's degree in Electrical Energy Engineering

Master's thesis in Electrical Energy Engineering

Design and implementation of a GaN based dual active bridge converter for electric vehicle charger

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Contents

List of Tables

List of Figures

Abstract

Nowadays electric mobility is arousing a lot of interest from the major car manufacturers. Despite the fact that outboard fast direct current chargers represent the most immediate response to the problem of recharging the batteries, AC on-board chargers are of fundamental importance to guarantee the use of the domestic infrastructure. After the conversion of the voltage from AC to DC, carried out by the power factor corrector, a DC/DC converter is necessary to be able to charge the battery with the desired current value.
In this context, the dual active bridge converter represents a good solution since it allows to satisfy the aforementioned request, guaranteeing the minimum bulk, the minimum number of components and galvanic isolation.
In this thesis the study of the aforementioned converter operating at a frequency of 500 [kHz] is presented; the realization of the high frequency transformer with integrated leakage inductance is documented in detail and finally a possible alternative to the classic control with single phase shift between the two active bridges is described, in order to extend the range of soft switching even at small levels of transmitted power, especially necessary to accomplish the final stage of the battery charging process, during which the load current becomes very small.

Sommario

Oggigiorno la mobilità elettrica sta suscitando grande interesse da parte dei maggiori costruttori di veicoli elettrici. Malgrado le colonnine fast charge in corrente continua rappresentino la risposta più immediata al problema di ricarica delle batterie, i caricatori di bordo in alternata sono di fondamentale importanza per sfruttare la capillare rete di alimentazione domestica.
In seguito alla conversione da AC in DC che è realizzata mediante il power factor corrector, un convertitore DC/DC è necessario per essere in grado di ricaricare la batteria con la corrente desiderata. In tale contesto il convertitore a doppio ponte attivo rappresenta un'ottima soluzione poiché permette di soddisfare la sopracitata richiesta, garantendo un minimo ingombro, un minimo numero di componenti e l'isolamento galvanico.
In questa tesi si affronta lo studio del suddetto convertitore, operante alla frequenza di 500 [kHz]; viene inoltre presentata la progettazione del trasformatore ad alta frequenza ed infine viene descritta una possibile alternativa al classico controllo con singolo sfasamento tra i due ponti attivi, al fine di estendere il funzionamento in soft switching anche con piccoli livelli di potenza trasmessa, in particolare durante l'ultimo stadio di carica della batteria.

1 Introduction

For more than a century the development of industrialized countries has been dependent upon fossil fuels. Current trends in energy supply are not more sustainable and climate changes are starting to become irreversible.
Governments are focusing on the major fields of air pollution, among them the transportation sector. In the next few years it'll be necessary to think back the way through which people can move. Electrical energy use in the transport sector is considered the best solution in order to reduce the mainly exhaust gasses that cause greenhouse effect, especially CO_2 and $NO_x s$, the last ones are generated in internal combustion engines that work at high pressure ratio, like the diesel ones.
With respect to traditional engines, electric vehicles, especially those that rely only on batteries supply, can reach a plug-to-wheel efficiency that is more than the double; although all these good perspectives, penetration rates of electric vehicles are still too low. The reason could be search on the following drawbacks:

- high battery cost;
- range anxiety;
- a narrow spreading of charging infrastructures, especially along the highway;
- long charging time.

Decarbonizing transport is providing to be one of the largest research and development projects of the 21st century [1].

1.1 Energy efficiency

The great driver for electric mobility (beyond climate change) is the capability to operate locally without creating emissions, this aspect is very important, especially in big cities: it's known that a central plant, to product the energy required for a fleet of cars, releases into the air a smaller quantity of pollutants with respect a myriad of small widespread burners, in which it's impossible to set powerful electrostatic filters. Hence the growing amount of electric vehicles can give a big "footprint" to improving air quality in urbanized regions.
Taking a look at the histogram in figure 1.1, it's clear that a real climate benefit in the shifting from oil to electricity is reached only when renewable energy sources will get a big slice in the circle of the production sources; on one hand with a proper energy baking, it will be possible to go below 50 [gCO_2/km] in WLTP cycle, but on the other hand relying exclusively on coal exploitation, the pollution caused by electric vehicles overcomes the top boundary of combustion engines.
An important aspect of electric vehicles has to be found in their ability to get advantages from kinetic energy: despite combustion that is irreversible, during breaking and downhill, inverting the sign of the current in the windings, electric motors can act like a "brake forward" and so they are able to recover a certain amount of this energy and act like generators, while maintaining the same rotation direction; in this way a considerable energy saving can be reach not only in battery electric vehicles (BEVs), but especially in plug-in hybrid electric vehicles (PHEVs), since the energy recovered can be used in the following acceleration, leaving the combustion engine to work in a range of maximum torque and minimum fuel consumption.

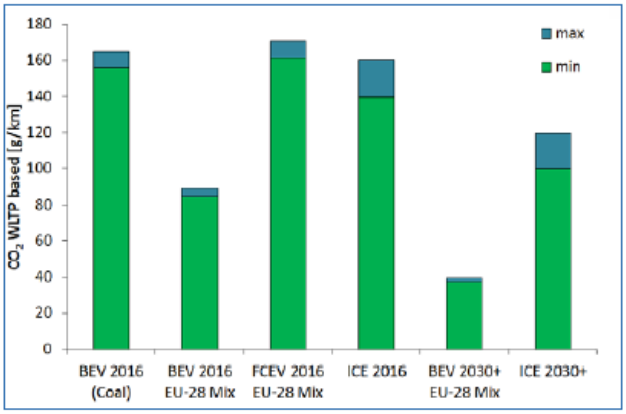


Figure 1.1: Comparison of CO_2 emissions for different power trains, considering different ways of energy production [2].

1.2 Challenges

As written above, the reasons for the scepticism of public opinion in face of electric mobility relied on economic and physical boundaries. To increase the available range, a bigger battery stack is needed but it would cause an increasing of the weight and subsequently a decreasing of efficiency.
Fast charging is another requirement: at the beginning of this year Tesla presented the third generation of its Superchargers that can reach a peak charging power of 250 [kW], allowing to obtain 120 [km] in just five minutes (of course the power will decrease as the charge status of the battery increases).
In order to achieve the goal of a widespread electron mobility it's necessary to obtain important developments in the following fields:

- energy storage systems;
- drivetrain technologies;
- grid integration.

The work of this thesis is focused on one power electronic system that allows an efficient energy management and it's connected downstream an active power factor corrector converter: the DC/DC isolated dual active bridge converter.

1.3 Automotive applications of DAB converter

The reasons for what it has become necessary to put more and more effort on the developing of electric mobility can be summarized in three points:

- shrinking of fossil fuel reserves;
- growth of word population;
- increasing of welfare also in poor countries, that means a large number of people would like to access the exploitation of energy to ensure economic growth.

The energy demand can be differentiated into three major "subjects": civil, industrial and transportation activities.
Apart from increasing the energy efficiency, it's not possible to make heavier changes in the first two groups, instead it

Table 1.1: Different energy demands.

Power train	Electric	Combustion
Energy consumption tank to wheel [Wh/km]	+30	+400
Energy consumption well to tank [Wh/km]	+180	430

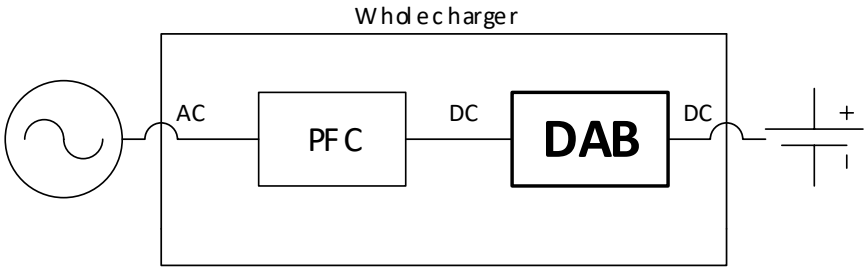


Figure 1.2: Schematic block of the entire charger.

results possible to re-design the third one, bringing interesting amount of energy saving and consequently air pollution decreasing.
In order to understand if the electrical technology is the right direction to be followed, a short energy balance is mandatory: on one hand in internal combustion engines, beyond road energy and power train consumptions, there are also losses regarding the extraction, refining and transportation of oil; on the other hand in battery electric vehicles (BEVs), besides traction energy, losses occur in the transmission and distribution electric grid.
Below there's a fast computation that underlines the milestones of the two different propulsion systems: consumptions are distinguished in two categories, id est from tank to wheel (assuming that tank represents both fuel sink and battery stack) and from well to tank (assuming that well stays also for electric energy plants).
The average propulsion energy required by a C segment car is about 120 [Wh/km]. Through the values listed in table 1.1, making a sum it appears that the total energy well to wheel is equal to 330 [Wh/km] for BEVs and 950 [Wh/km] for ICEs [3], hence there is a saving of about 65 %. In the middle there are hybrid electric vehicles that would be the most popular in the next few years, also remembering that from 2021 all cars manufacturers should respect the average limit of 95 [gCO_2/km]. In all electric vehicles the dual active bridge DC/DC converter plays a fundamental role in the charging and discharging process of the battery, allowing galvanic isolation and managing the difference voltages between battery and rectified DC voltage. Picture 1.2 presents all the voltage conversions that occur inside the charger: the AC voltage at the input port is rectified by means of the PFC converter, then the DC voltage is modified by the dual active bridge in order to get the suitable magnitude to charge the battery stack. The following paragraph describes an ancillary use of the first stage of the charger, instead the dual active bridge will be discussed in details in the second chapter.

1.3.1 V2G technology

The whole charger consists of two stages: a power factor corrector (PFC), which interfaces with the grid, and a dual active bridge, that allows to manage the DC voltage between the DC link and the battery. Thanks to this particular architecture it's possible not only to charge the battery, but also to discharge it, for traction aim or to fulfil the so called "vehicle to grid".
The daily power demand plot has two humps that the network manager has to provide in order to ensure the stability of the electric system. EVs store a big amount of energy in their battery stacks and for this reason they could be a good

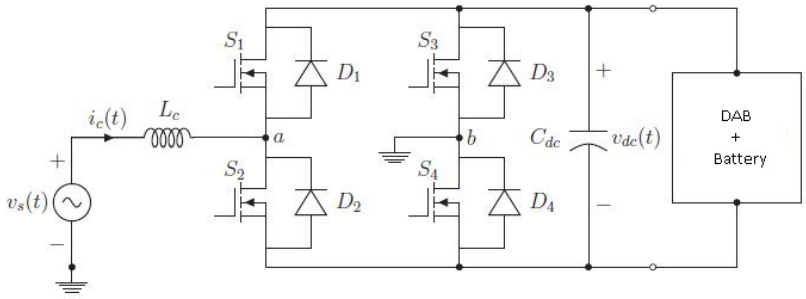


Figure 1.3: Full active bridge AC/DC converter.

solution to smooth these two humps of the power demand trend; however some researches have demonstrated that this further exchange of energy, increasing the number of charging/discharging processes, will decrease the lifetime of the traction battery.

On the other hand it's rising the idea to employ the chargers inside electric vehicles to compensate locally the reactive power in the transmission grid. It's known that for long distance, the reactive component (inductive one) of the transmission lines is higher than the resistive one, also considering that a big part of loads connected to the grid is of inductive nature. The reactive current doesn't contribute to the transmission of active power, but it just flows from one side to another, congesting the grid and increasing the losses on transformers. For these reasons the possibility to produce at the distribution level and locally the reactive power required by passive loads is reaching a lot of interest. Through a punctual management of the reactive power it's possible to accomplish some of the bigger problems that afflict the grid stability: voltage and frequency regulation.

The on board charger can provide positive or negative reactive power independently from the state of charge of the battery, not afflicting its lifetime. The first stage of the chargers is drawn in figure 1.3. To make an analysis of the circuit it's possible to refer to an equivalent simplified one, considering only the grid and the input converter voltages (respectively v_s and v_c), interleaved by the inductance L_c. The last one takes into account not only the transmission lines inductance, but also that one used downstream the power factor corrector that is used to limit the current oscillation in the DC bus.

Looking at the full bridge from right to left side, the DC voltage of the capacitances is the input parameter, instead the AC voltage, made through a PWM modulation, represents the output parameter. Considering a switching frequency quite high, the passive filters on both sides of the converter could be regarded so small that they don't absorb power. Thinking the grid voltage perfectly sinusoidal, since the transfer of power between the two subjects (the grid and the converter) is possible just among isofrequential quantities, all the harmonics generated by the switching can be neglect and it's possible to focus on fundamental:

$$v_s(t) = \sqrt{2}V_s sin(\omega t) \tag{1.1}$$

Since normally the grid acts like the tank of energy, the voltage downstream the inductance L_c has to lag $v_s(t)$ of an angle δ that it's called "load angle":

$$v_c(t) = \sqrt{2}V_c sin(\omega t - \delta) \tag{1.2}$$

The source voltage v_s and the charger voltage v_c, being at the same frequency, can be expressed as phasors:

$$\mathbf{V_s} = \sqrt{2}V_s e^{-j\pi/2} \tag{1.3}$$

$$\mathbf{V_c} = \sqrt{2}V_s e^{-j(\pi/2+\delta)} \tag{1.4}$$

The phasor of the current I_c that flows through the inductor is given by the ratio between the inductance voltage and the respective impedance. The final expression of the current in time domain is given by:

$$i_c(t) = \sqrt{2}I_c sin(\omega t - \theta) \tag{1.5}$$

in which

$$I_c = \frac{1}{\omega L_c}\sqrt{V_c^2 + V_s^2 - 2V_c V_s cos(\delta)} \tag{1.6}$$

and

$$\theta = tan^{-1}(\frac{V_s - V_c cos(\delta)}{V_c sin(\delta)}) \tag{1.7}$$

Knowing the expression of the line current $i_c(t)$ and the voltage $v_s(t)$ it's possible to compute the instantaneous power delivered by the grid:

$$\begin{aligned} p_s(t) &= v_s(t)i_c(t) = \sqrt{2}V_s sin(\omega t) \cdot \sqrt{2}I_c sin(\omega t - \theta) \\ &= V_s I_c cos(\theta) - V_s I_c cos(2\omega t - \theta) \end{aligned} \tag{1.8}$$

The instantaneous power through the coupling inductance is equal to:

$$p_L(t) = v_L(t)i_c(t) = L\frac{di_c}{dt}i_c(t) \tag{1.9}$$

Substituting the expression (1.5) into the equation of the inductance power (1.9), it results:

$$p_L(t) = \omega L_c I_c^2 sin(2\omega t - 2\theta) \tag{1.10}$$

Finally, taking into account equations (1.8) and (1.10) it's feasible to compute the instantaneous power in the AC side of the converter:

$$p_c(t) = p_s(t) - p_L(t) = V_s I_c cos(\theta) - V_s I_c cos(2\omega t - \theta) - \omega L_c I_c^2 sin(2\omega t - 2\theta) \tag{1.11}$$

Like shown in equation (1.11), the instantaneous charger input power consists of two terms: the first one at the grid frequency is the average power, the second one at a double frequency is the ripple power. Focusing on the ripple contribute, it's possible to refer both terms to a sinusoidal waveform (since they have the same frequency) and calculate the module of this power component:

$$P_{ripple} = \sqrt{(V_s I_c)^2 + (\omega L_c I_c)^2 - 2\omega L_c V_s I_c^3 sin\theta} \tag{1.12}$$

The active, reactive and apparent power can be express in function of the load angle θ:

$$P_s = V_s I_c cos(\theta) \tag{1.13}$$

$$Q_s = V_s I_c sin(\theta) \tag{1.14}$$

$$S = V_s I_c \tag{1.15}$$

Substituting the equations from (1.13) to (1.15) in (1.12), the module of the ripple input charger power results function of the reactive power:

$$P_{ripple} = \sqrt{S^2 + (\omega L_c \frac{S^2}{V_s^2})^2 - 2\omega L_c \frac{S^2}{V_s^2} Q_s} \tag{1.16}$$

The amplitude of the ripple in the input power is directly linked to the sign of the reactive power of the source: if the full bridge converter absorbs an inductive reactive power (hence it delivers capacitive reactive power to the grid) the ripple will be smaller, contrariwise if the converter absorbs a capacitive reactive power (so it delivers inductive reactive power to the grid), the ripple will be greater. The sign of the reactive power absorbed by the charger depends on the modules of the grid and converter voltages: if V_s is greater than V_c, Q_s will be positive and the PFC looks like an inductor, otherwise it will be negative and the full bridge acts like a capacitance. Dividing the ripple power by the working pulsation (at a double frequency with respect that one of the grid) gives the module of the energy ripple which is present in the DC link supported by the capacitances:

$$E_{ripple} = \frac{1}{\omega} \sqrt{S^2 + (\omega L_c \frac{S^2}{V_s^2})^2 - 2\omega L_c \frac{S^2}{V_s^2} Q_s} \tag{1.17}$$

Considering the frequency of the energy ripple, the maximum variation of the energy stored by the capacitor bank corresponds to:

$$E_{\Delta cap} = \frac{1}{2} C (V_{dcmax}^2 - V_{dcmin}^2) \tag{1.18}$$

Equating the two energy equation (1.17) and (1.18) it's possible to get the minimum required value of capacitance at the DC link of the charger to accomplish the task of the local reactive power compensation.
The capacitance bank in the laboratory charger consists of four Nichicon capacitances connected in parallel in order to get a total amount of 1560 [μF], a reasonable value to make this charger suitable also for the aforementioned ancillary aims (the minimum and maximum value of the DC link voltage are respectively 380 [V] and 420 [V]).
It has to be outlined that the required capacitance value directly depends on the total inductance L_c. Taking into account all the inductive objects connected to the grid, this value could be quite big: for this reason the v2g reactive power compensation has a positive impact only if a large number of EVs accomplish this task.
Since the aim of this thesis is focused on the study of the DC/DC converter and not on the PFC stage, the vehicle to grid operation won't be analyzed anymore; this short section has been necessary just to outline that a possible use of the EVs as active subjects towards the electric system has to be taken into account in the design of the charger, since the reactive power could create instabilities downstream the AC/DC conversion.

Table 1.2: Properties of different semiconductors

Parameters	Si	GaN	SiC
Band gap $[eV]$	1.12	3.39	3.26
Critical field E_c $[MV/cm]$	0.23	3.3	2.2
Electron mobility $[cm^2/Vs]$	1400	1500	950
Permittivity	11.8	9	9.7
Thermal conductivity $[W/cmK]$	1.5	1.3	3.8

1.4 GaN

1.4.1 Why to use gallium nitride

Before the coming of power electronic switches, all the energy management was passive: resistors were used to regulate the speed of a motor and in this way it was possible, for example, to regulate the quantity of fluid that a pump could manage; all the components were very heavy and bulky, since the working frequency was that one of the grid. Through switching semiconductor devices, it became possible to manage the energy flow in a more efficient way, changing directly the module of voltage and current applied to electric motors and electronic devices. Increasing the working frequency means reducing the weight and volume of power electronic converters, ensuring both efficiency and reliability. For over three decades mosfets have improved their capabilities, but since the last years the rate of improvement has slowed, because this technology has almost got its theoretical boundaries.
The requirement to get further improvements, in order to increase the working frequency and ensure the capability of withstand high voltage, involves researchers to investigate new materials that could substitute silicon and silicon carbide in the manufacturing of field effect transistors. Semiconductors used in power conversion have to ensure:

- efficiency;
- reliability;
- controllability;
- cost effectiveness.

In order to make a comparison between different kinds of semiconductor, there are some parameters that have to be taken into account, especially band gap and critical field. The crystal parameters contained in table 1.2 make it possible to understand because gallium nitride can be superior than other semiconductors. The band gap of a semiconductor is related to the strength of its bonds inside the crystal lattice: an higher value can be translated in the capability of material to work with high temperatures and ensure lower leakage currents.

$$V_{br} = \frac{1}{2} w_{drift} E_c \tag{1.19}$$

A consequence of strong chemical bonds is an higher electric field needed to cause avalanche breakdown. The breakdown voltage V_{br} is proportional to the width of the drift region (w_{drift}), i.e. the region low doped, as it can be seen in eq. (1.19). In the case of GaN and SiC, the drift region can be 10 times smaller than in silicon for the same breakdown voltage.

In order to support a such big electrical field, it's necessary that the majority carriers are depleted away. Assuming an N-type semiconductor, it's possible to use the Poisson's equation to calculate the number of electrons between the

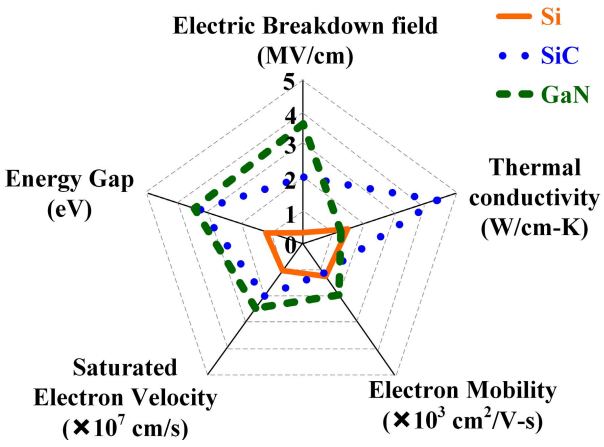


Figure 1.4: Performances schematic plot of Si, SiC and GaN.

two terminals of the device (drain and source):

$$qN_D = \xi_o \xi_r \frac{E_c}{w_{drift}} \tag{1.20}$$

In the equation (1.20) q is the electron's charge ($1.6{\cdot}10^{-19}$ coulombs), N_D is the number of electrons contained in the volume, ξ_o and ξ_r are respectively the vacuum and relative permittivity. Since the critical electric field inside gallium nitride devices can be 10 times bigger than inside silicon ones, it's possible to design the electrical terminals 10 times tighter, hence the number of electrons can be 100 times greater and this one is the reason for what GaN and SiC overcome Silicon in power conversion. The wide band gap semiconductors result in devices with lower on-resistance R_{on} and switching losses. Unfortunately, as can be seen in figure 1.4 GaN shows a lower thermal conductivity rather than SiC, but it's superior for what concern high-efficiency and high-frequency possibilities of working.

$$R_{DS_{on}} = \frac{w_{drift}}{q\mu_n N_D} \tag{1.21}$$

The theoretical on resistance is proportional to the width of the drift region (see (1.21), where μ_n is the electrons' mobility).

1.4.2 Two dimensional electron gas

The lattice of gallium nitride has a hexagonal structure (see figure 1.5). Since it's very stable, this material can work with high temperatures without destroying itself; furthermore it has some piezoelectric properties that allow to create a small electric field when there's a strain applied.

In order to create a conduction path, it's necessary to build up a heterojunction, for example facing a layer of GaN with another one of AlGaN. In this way a strain will grow at the interface of the two layers and a two dimensional electron gas (2DEG) appears. Applying an external electron field, it's possible to almost "short-circuit" the drain and source, creating a path with high concentration and high mobility of electrons, that causes a negligible voltage drop during switch conduction (see figure 1.6).

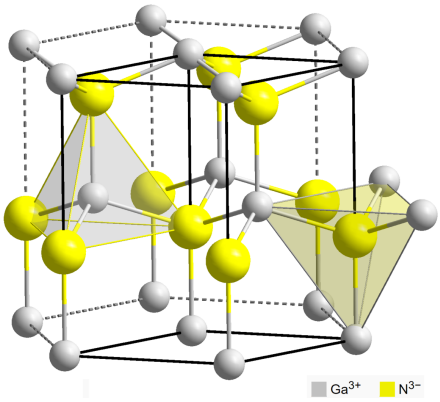


Figure 1.5: Crystal lattice of GaN.

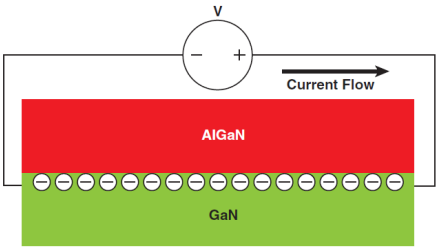


Figure 1.6: Two dimensional electron gas under external field.

1.4.3 Depletion and enhancement mode

Nowadays most of the GaN devices available are lateral heterojunction field-effect transistors (HEMTs); they are rated to work with voltages up to 600-650 [V]. As can be seen in figure 1.7 both source and drain terminals pierce through the AlGaN layer, in order to almost create an ohmic contact with the 2DEG. The substrate is typically made of Si, sapphire and other materials; it's necessary also to create a buffer layer between the substrate and the GaN layer. After this small description, it's clear that the HFET is inherently a depletion-mode device and so, without applying any negative voltage at the gate,with respect to drain or source potential, the two external terminals are normally "short-circuited". This behaviour is not desirable for voltage-source converters, because it creates very big circulating current at the start up of the device if no negative voltage is before applied to the gate.
In order to overcome this disadvantage, researchers and manufacturers put a lot of effort in the design process, in order to modify the internal structure of the switches and make them normally off at "rest" position. These devices are called enhancement-mode transistors. Principally there are four popular structures to create these desirable devices: recessed gate, pGaN gate, cascade and implanted gate.
The first topology is based on the simple idea that, etching the thickness of the AlGaN layer, the piezoelectric effect will decrease and hence the bias voltage is easily smaller than the built-in voltage of the Schottky gate metal and

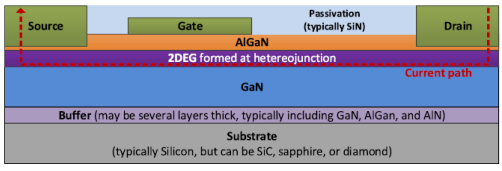


Figure 1.7: Depletion-mode lateral GaN HFET.

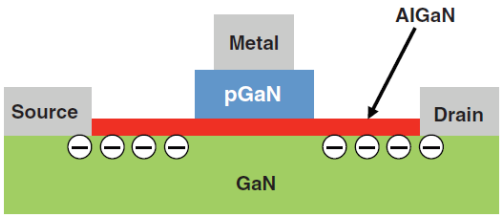


Figure 1.8: Schematic section of a pGaN enhancement transistor.

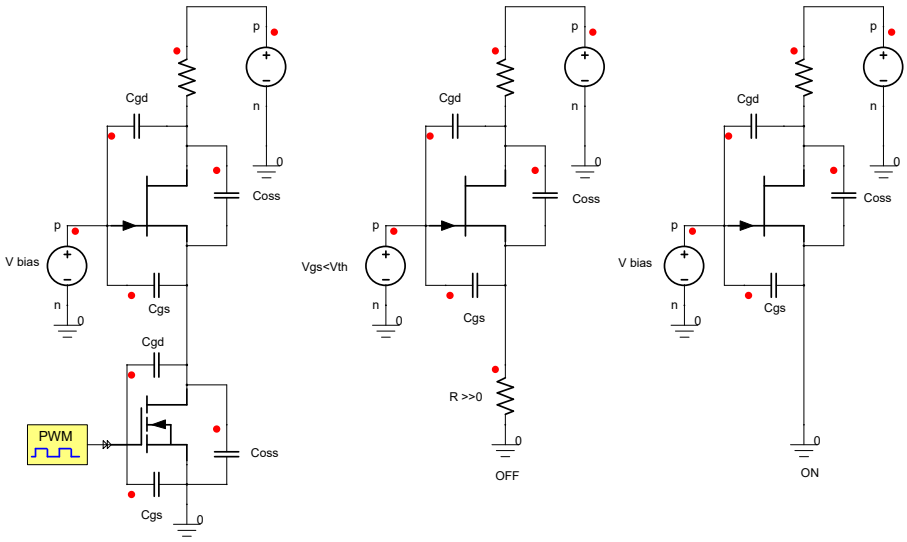


Figure 1.9: Cascade hybrid configuration and operating stages.

in this way it's possible to deplete the region below the gate surface, interrupting the short path created by the high concentration of electrons.

The second topology is based on the same idea of the first one, but instead of decreasing the natural piezoelectric field induced in the interface between the two layers of AlGaN and GaN, it's put a p-type GaN layer over the AlGaN one and over it there's the metal gate. Since the positive charges of this doped layer have a built-in voltage greater than that one generated by the piezoelectric effect, the 2DEG is split in the two opposite side of the gate surface, making impossible a current flow without applying a positive voltage between gate and source, as can be seen in figure 1.8.

The third way to get a normally off device is the so called "cascade hybrid mode". In the cascade mode two series transistors are required (figure 1.9): the first one has a bias voltage and the second one is driven by means of a pulse signal. Following the stages shown in the aforementioned figure, when Q2 is in the off state, id est the drive signal is null, it appears a sort of very big resistance and so, whatever current will flow through the depletion-mode GaN HFET (Q1), it will generate an increasing of the voltage. Meanwhile, as the pin source voltage goes up, that one between gate and source falls down, until when it becomes smaller than the threshold voltage ($V_{gs} < V_{th}$) and so also the first transistor will turn off. In this way we could identify the low voltage mosfet (Q2) like a master and the HEFT like a slave (Q1).

When a positive pulse is applied on the gate of Q2, the resistance between its drain and source terminals falls down and hence the potential on the source side of Q1 becomes like the ground one. Applying the opportune bias voltage on the gate of the HEFT, V_{gs} grows over V_{th} and so there's a flow of current, but only in presence of a positive bias voltage in the mosfet Q2 (enhancement mode transistor). This configuration allows to design very fast switches: taking a look at

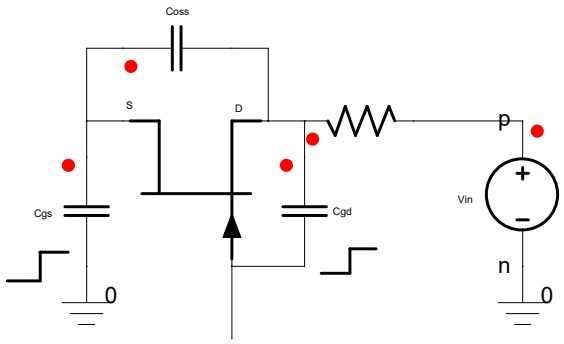


Figure 1.10: Schematic circuit during conduction of low voltage mosfet.

the first transistor Q1 (figure 1.9), there's a bias voltage applied on the gate terminal, but the control signal is applied by the source terminal (in this way it's possible to change the potential of the source terminal), so it's a quite different control technique rather than standard one.

$$C_{Mill_{PWM}} = C_{gd}(1 + \frac{V_{in}}{V_{gs}}) \tag{1.22}$$

In normal transistors there are two parassitic capacitances between gate-source and gate-drain; the last one has a significant impact on the commutation behaviour, since Miller's effect appears. This effect causes that C_{gd} seems bigger than in reality, depending on the voltage gain, as can be seen in equation (1.22), that appears like the capacitance behaves in the same way of a boost converter. With a very large capacitance it's necessary a big amount of charges in order to charge C_{gd} and C_{gs}, furthermore these capacitances are not linear and their modules change with voltage changing. This gain in the gate to drain capacitance is due to the so called "phase reversal": when a positive gate to source voltage is applied at control terminal, the drain to source voltage falls down and this is the reason for the positive gain in the Miller equation (1.22). On the other hand, when the control pulse is given through the source terminal of the depletion mode transistor, it appears the circuit shown in figure 1.10. In this case the capacitance C_{gs} is grounded.

$$C_{Mill_{PWM}} = C_{gd}(1 - \frac{V_{in}}{V_{gs}}) \tag{1.23}$$

$$C_{Mill_{PWM}} = C_{gd_{Q2}}(1 + \frac{\Delta V_d}{V_{gs}}) \tag{1.24}$$

In this particular case, the Miller capacitance becomes quite small, since the voltage gain is not more added (see equation (1.23)) due to the fact that there isn't the "phase reversal" phenomenon; as a result the charge required to charge and discharge the parasitic capacitances is approximately that one of the C_{oss}, hence enough small to guarantee a high switching frequency. Anyway, the low voltage mosfet Q2 is still driven with standard technique (pulse inside the gate), but the voltage swing at its drain terminal (linked in series with the source terminal of the GaN transistor) is quite small, since the maximum voltage variation that can occur at the input of the second transistor is equal to the threshold voltage of the GaN HEFT. Thanks to the small voltage oscillation at the drain terminal of the common mosfet, the resultant Miller capacitance between drain and gate doesn't suffer the voltage gain, since the last one is very small, like stated in equation (1.24). It's important to underline that, in order to get high switching frequency, the stray

inductances have to be reduced as minimum as possible, otherwise, since in the circuit there are high rate of current variations, the voltage swing in the drain terminal couldn't be any more negligible. Since the on resistance $R_{ds_{ON}}$ in the GaN HFET increases with the increasing of the voltage, the cascade mode is convenient when the working range of voltage is above 200 [V], in this way the added mosfet resistance will be just 3% of the total resistance.
The fourth topology establishes to deplete the two dimensional electron gas by putting some negative fluorine atoms inside the AlGaN layer: in this way the transistor becomes normally off and only applying a positive voltage through the Schottky gate it's possible to reconstruct the very high conductivity electron path.

1.4.4 Bidirectional current flow

In a conventional Si mosfet the current can change its direction through the path created by the p-n junction. The GaN HEFT hasn't got any body diode, but the bidirectional way is guaranteed by its symmetric structure. Differently from other enhancement mode devices, in the cascode mode, when the direction of the current changes, the body diode of the low voltage Si mosfet turns on and consequently also the GaN transistor turns on, but once the current starts to flow inside the mosfet, there's a peak due to the reverse recovery charge, however this spike of current expires in a narrow time and it's vary order of magnitude smaller than the spikes of current that occur in power mosfet.
In the GaN enhancement HEFT the electron channel is built up when the voltage across gate and source exceeds the threshold one; furthermore it is restored also when the voltage among drain and gate overcomes its own threshold one, $V_{th_{gd}}$, approximately the same between gate and source.
When the output of the device is reverse biased, the gate to drain voltage becomes:

$$V_{gd} = V_{gs} - V_{ds}.$$

The voltage drop in self commutated reverse conduction mode (SCRC) is computed as:

$$V_{sd} = V_{gd_{th}} - V_{gs} + I_d R_{sd_{rev}}.$$

The reverse resistance between source and drain ($R_{sd_{rev}}$) is usually higher than that one in the direct conduction mode and varies with the junction temperature T_j. Compared with the voltage drop that appears during the body diode conduction on a mosfet, the V_{sd} is quite higher (3-5 [V]) and for this reason the losses in reverse conduction mode could be excessive for long dead time, but the lack of a real body diode allows to ensure zero voltage switching condition also with small dead time.

1.4.5 Variable on resistance

The breakdown voltage in the super junction devices is related to the distance between the external electrodes; since the on-resistance is directly proportional to the length of the drain-source path, it's clear that it depends linearly by the breakdown voltage.
The total resistance of the aforementioned path is given by the sum of the channel resistance, R_{ch}, and the drift region resistance, R_d.

$$R_{ch} = \frac{L_g}{W_g}\frac{1}{q\mu N_s} \tag{1.25}$$

$$R_d = \frac{L_d}{W_g}\frac{1}{q\mu N_s} = \frac{1}{W_g}(\frac{B_v}{E_c}\frac{1}{q\mu N_s}) \tag{1.26}$$

As can be seen in the equations (1.25) and (1.26), both contributes to on-resistance depend on design geometry parameters, in fact W_g is the gate width; L_g is the gate length; μ is the electron mobility inside the two dimensional electron gas; N_s states the density of majority carriers.

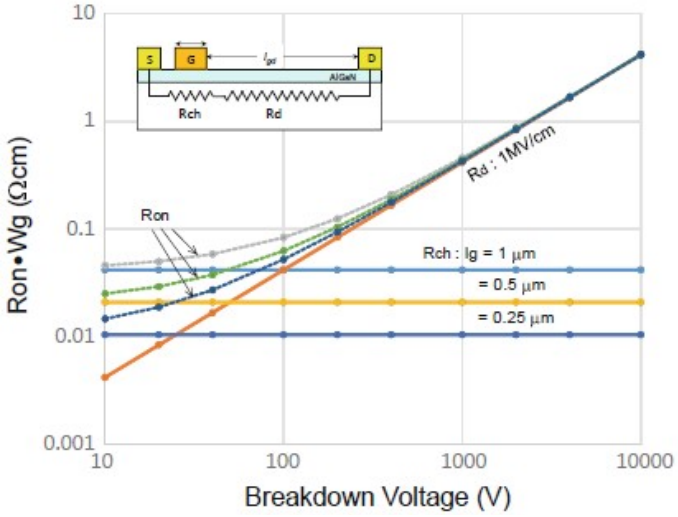


Figure 1.11: Changing of R_{on} varying gate length, with E_c equal to 1 [MV/cm].

In figure 1.11 is represented the trend of different resistance contributes. Looking at the plot, it's possible to understand that R_{ch} and R_d have a different contribute on the value of R_{on}, depending especially by the breakdown voltage: in the low-voltage range R_{on} tends to the value of R_{ch}, instead in the high-voltage range R_d has the heavier effect. From this short analysis it emerges that decreasing the gate-length is useless in high-voltage range [4].

Low and high voltage device shrewdness

Decreasing on-resistance is one of the most important goal to be followed during the design of a power device, since it's related to device's efficiency. For what concern low-voltage working range, as said in the previous sentences, R_{ch} represents the major contribute to the total on-resistance. In a first approach it seems sufficient to decrease the gate-length, but in this way also the critical field E_c will be smaller and won't satisfy any more the requirement for blocking voltage. For this reason a minimum space between source and drain has to be ensured. From this point of view wide band gap semiconductors, like SiC and GaN have advantages with respect to Si, since the bigger specific E_c [V/μm] makes possible to miniaturize their structure, about 40 times smaller than Si devices. The most important aspect of miniaturizing is regarded the switching losses: with smaller devices, the charge required to charge and discharge the parasitic capacitances during each commutation is order of magnitude less, allowing for better efficiency and higher switching frequency than those ones obtained with band gap semiconductors. Since the on-resistance can be decreased also increasing the gate width, some attentions are involved in vertical structures, that can allow also higher range of voltage; these kind of devices are still at research step and not yet commercially available.

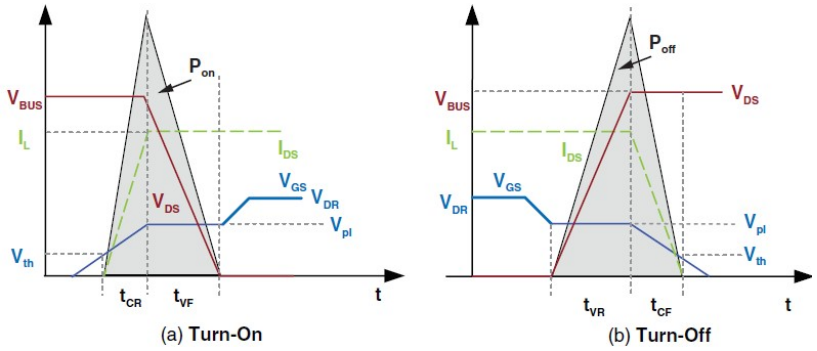


Figure 1.12: Switching power losses during turn-on (a) and turn-off (b) of a power device.

In high frequency converter one of the heavier "stones" on conversion efficiency is linked to switching losses, since conduction losses, thanks to small time period and low on-resistance, are negligible. As it's possible to see in figure 1.12, switching losses are linked to the contemporary presence of current and voltage. The switching power loss can be determined taking into account both voltage and current transition power losses (P_{Vt} and P_{Ct}) and summing the two contributes like can be seen in the equation:

$$P_{sw} = P_{Vt} + P_{Ct} = \frac{1}{2} V_{BUS} I_L (t_{CR} + t_{VF}) f_{sw}.$$

In the aforementioned figure it emerges the slower slope of the gate-voltage during the switching time, which is linked to Miller's effect: as explained in previous paragraph, since the gate-drain capacitance C_{gd} is positively affected by the voltage gain, the time constant is smaller and hence the "reactivity" of the RC circuit becomes slower.
The other losses that occur in the enhancement mode HEMTs are regarded conduction in forward mode and during dead time. The first one can be computed taking into account the current that flows through the 2DEG and the total resistance of this "conduction pipe":

$$P_{forward} = R_{ds_{on}} I_D^2.$$

The second one is linked to the threshold voltage of the body diode V_o, the drain current I_D and the reverse resistance between source and drain $R_{sd_{rev}}$, through the following equation:

$$P_{dead} = I_D V_o + I_D^2 R_{sd_{rev}}$$

Hetero junction AlGaN/GaN FETs have the breakdown voltage proportional to the characterizing dimension of the

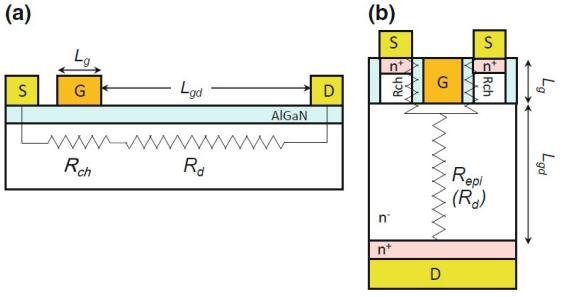


Figure 1.13: Resistive models of lateral (a) and vertical (b) GaN power switches.

drift region and for this reason vertical power device are expected to provide both high blocking voltage and high current handling capability, in fact increasing packing factor has a narrow gain in reducing the on-resistance [4].

$$R_{epi}\ \alpha \frac{W_d}{\mu N_d} = \frac{B_v^2}{\mu \epsilon_{GaN} E_c^3} \quad \text{being} \quad E_c = \frac{qN_d}{\epsilon_{GaN}} W_d \tag{1.27}$$

Taking a look at figure 1.13 it seems that with vertical structure the drift region resistance would increase; in reality the drift region in this configuration is doped and the resistance in the epitaxial layer is directly proportional to the gate-width but especially inversely proportional to the cubic of the critical field E_c [5], that is quite bigger than later devices, as stated in equation (1.27).

Current collapse

Lateral devices suffer the so called "current collapse", a phenomenon that produces an increase of the on-resistance during conduction.

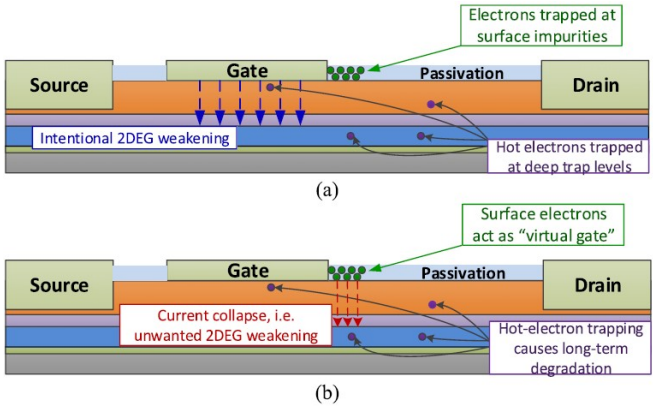


Figure 1.14: Events that cause an increase of R_{on}: charges trapped in off-state (a); consequent current collapse (b).

There are two main mechanisms that bring to such swing in the resistance (shown in fig. 1.14):

- trapping of surface charges;
- injection of electrons in deeper layer.

Regarding the first mechanism, during the off-state the lateral design makes the gate-drain electric field to be stronger and impurities in the passivation layer trap some charges; subsequently, during conduction mode, these trapped charges create a virtual gate that weakens the 2DEG and increases the drain-source resistance.
In the second case, some hot electrons, with big momentum, are able to penetrate in the deeper layers of the buffer, decreasing the density of majority carriers in the epitaxial substrate and hence the conductivity of the bidirectional electron path.
Some manufacturers presented a way to limit this current collapse, putting two plates over the source and gate terminals, in this way the gate-drain electric field is redistributed in a more wide volume [6].

1.4.6 Power converter design

Taking into account the high working frequency, the designers have to pay more attention in aspects regarding packaging: as stated before, in order to limit suddenly peak of voltage, that could overcome the characteristic breakdown

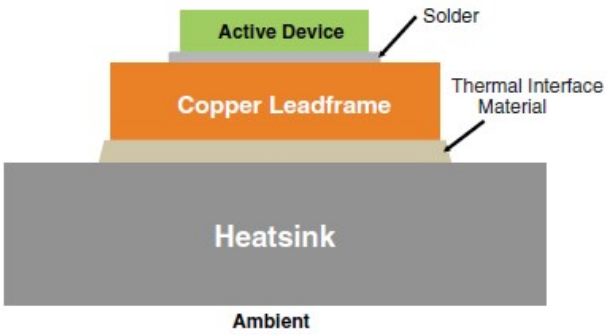


Figure 1.15: Section of proposed thermal conductivity improvement.

voltage of the device, it's necessary to avoid any parasitic inductance.
Like shown in table 1.2, GaN HEMTs have a smaller thermal conductivity than SiC devices. The switching and conduction losses are dissipated from the devices to the environment in the form of heat. In [7] a thermal measurement of a GaN device has been made : due to its small thermal conductivity, the heat generated during operation doesn't spread easily towards the ambient and the HEMT reaches temperature above 80 [°C]. In order to identify the steps of heat dispersion, it's necessary to think the packaged device in terms of equivalent thermal resistances, especially two are most important: junction to case $R_{\theta JC}$ and junction to ambient $R_{\theta JA}$ thermal resistances. The generic equation of a thermal resistance is equal to:

$$R_\theta = \frac{h}{A\lambda}$$

in which:
h is the orthogonal length of the path through each material that heat has to cross;
A is the cross section area of the aforementioned material layer;
λ is the thermal conductivity coefficient, that is related to chemical characteristics.
In figure 1.15 it's shown the improvement model proposed in [7]: the active device is soldered to a copper leadframe and this one, through a thermal interface material (TIM), to a finned heat sink, in order to get a big dispersion surface. In this proposed design, the total thermal resistance between junction and ambient $R_{\theta JA}$ is equal to the sum of three contributes, id est:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta TIM} + R_{\theta SA}$$

where:
$R_{\theta JC}$ is the junction to leadframe bottom thermal resistance;
$R_{\theta TIM}$ is the TIM thermal resistance;
$R_{\theta SA}$ is the heat sink to ambient thermal resistance.
This improvement allows to decrease the thermal conductivity gap between GaN and SiC devices, keeping a working temperature lower than about 20 [°C] [7].

1.4.7 GaN System GS66516B

This section describes the main aspects of the GaN HFETs used in the dual active bridge implemented. The GS66516B is an enhancement mode gallium nitride on silicon power transistor bottom-side cooled, that offers very low junction-to-case thermal resistance, in order to accomplish high power density and high switching frequency, paying attention

to obtain great value of efficiency [8].

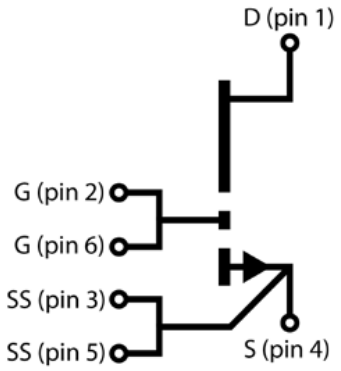


Figure 1.16: Circuit symbol of GS66516B.

Figure 1.16 depicts the electrical circuit of the normally off transistor. In order to turn it on, a positive gate to source voltage pulse has to be provided; the recommended drive voltages are 0 [V] to off state and 6 [V] to on state, these values to get optimal performance, long life and minimum value of $R_{ds_{ON}}$.

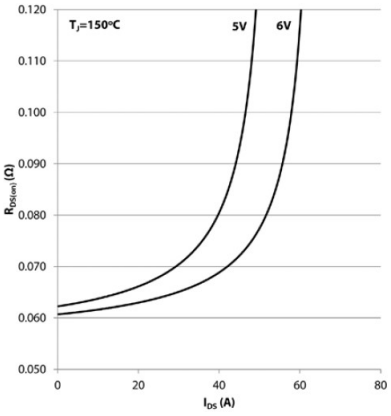


Figure 1.17: On resistance trend with different values of gate driver pulse and direct current, for fixed temperature.

It's possible to control the devices with a smaller magnitude gate voltage, but this will bring worst performances, in fact, as can be seen in the plot 1.17, the forward conduction resistance is inversely proportional to the gate voltage. Observing the circuit draft in figure 1.18, it's possible to understand what it's going on in terms of the requirements for the driver. PS2 is the power supply that provides a voltage range between 0 to 9 [V], after that this range is split into two voltages through the branch in which there's the zener diode DZ2 and the R16 resistance: 6 [V] and -3 [V] with reference ground in the middle that is in the source of the GaN GS66516T transistor. In this way, during the off state time interval, in reality the transistor gets a small reverse biased voltage. This negative bias ensures safe operation against the voltage spike on the gate, but it increases the reverse conduction loss [8].
This type of transistor is extremely sensitive to the gate voltage and normally the breakdown value is just slightly upper than the operation voltage, id est 7 [V]. Cause by some parasitic oscillations on the gate driver, it could be possible to overcome the allowed threshold and consequently to damage the gate terminal.

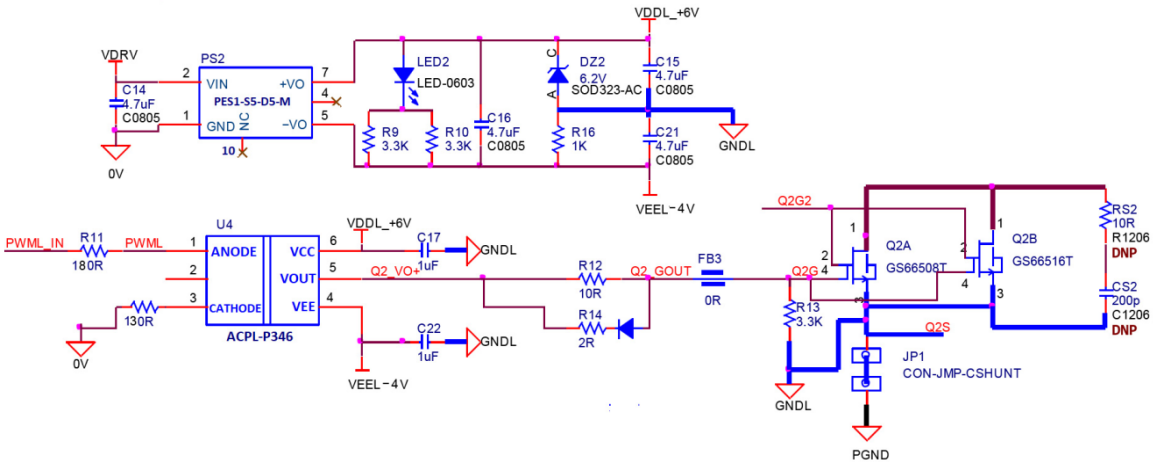


Figure 1.18: Gate bias and driver circuit.

1.4.8 Deep view on field effect transistor driver

The voltage required to turn on a field effect transistor depends on its characteristics, since there are always some parasitic capacitances between gate, drain and source terminals (C_{gd} and C_{gs}).

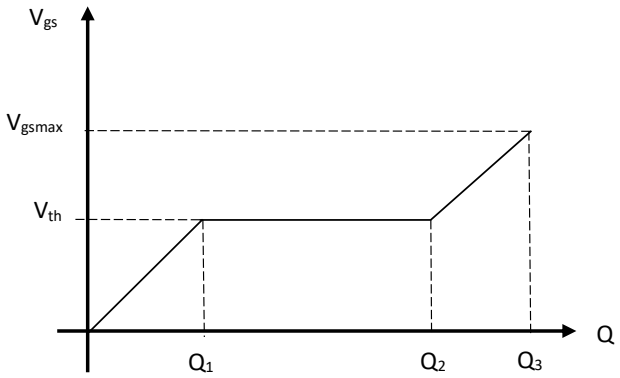


Figure 1.19: Gate to source voltage waveform vs provided charge.

In order to rise the gate potential from zero to a given voltage (in this case 6 [V] to reach saturation), it's necessary to charge these capacitances very fast, getting high frequency switching. At the beginning some charges have to be fed through the gate until the threshold voltage is obtained (Q1), like shown in fig. 1.19. At this point the drain potential starts to go down and consequently the C_{gd} charge varies rapidly. This behaviour causes the aforementioned "Miller effect" and for this reason the voltage goes up barely, although the driver is pumping more and more charges through the gate. When the drain potential is almost zero, the transistor works in saturation.
To compute the required gate current in order to turn on-off the transistor within a desired time, it's necessary to compute an equivalent capacitance that is able to match quite well the two non linear parasitic capacitances between gate and other two terminals. To do that it's needed to evaluate the voltage across the parasitic capacitance at $t = 0$ [s] and $t = \infty$ [s]:

$$V_{C_{gs}}(0) = 0[V] \quad V_{C_{gd}}(0) = -Vout \qquad \Delta V_{C_{gs}}(\infty) = V_{gs_{max}} \quad \Delta V_{C_{dg}}(\infty) = V_{gs_{max}}.$$

The voltage across the parasitic gate to drain capacitance plays an important role because it's exposed to very large

changes, in fact the drain potential at off state is equal to V_{out}, instead in fully conduction it could reach a narrow value, almost equal to the ground one. Taking into account all these aspects, it's possible to compute the total charge required and subsequently the equivalent capacitance, as shown in the following equations:

$$Q_{total} = V_{gs}C_{gs} + (V_{gs} + V_{out})C_{gd}$$

$$C_{eq} = \frac{Q_{total}}{V_{gs_{max}}} = C_{gs} + C_{gd}(1 + \frac{V_{out}}{V_{gs_{max}}})$$

The last contribution in the second equation represents the Miller's effect, that corresponds to the plateau path in the waveform plotted in figure 1.19. Once computed the equivalent capacitance, the required gate current will be equal to:

$$Q_{total} = I_g t_{on} = C_{eq}V_{gs_{max}} \quad \text{hence} \quad I_g = \frac{C_{eq}V_{gs_{max}}}{t_{on}}.$$

As written in the paragraph about converter design, in spite of all efforts, there will always be minimal stray inductance in connections and therefore there would be a series resonant circuit.

$$Q = \frac{Z_{resonant}}{R_{gate}} = \frac{\sqrt{\frac{L_{stray}}{C_{eq}}}}{R_{gate}} \tag{1.28}$$

If the quality factor (see equation (1.28)) is high, oscillations will occur in the gate voltage signal and their peak value could damage the device. After all the design measures, it's clear that to get a value of Q near the unit, the gate resistance has to be increased, in order to control the switching speed.
From the considerations made in the previous paragraphs it follows that for a controllable switch the following characteristics are desirable:

1. small reverse current during the lock state;
2. small drop in direct voltage to minimize conduction losses;
3. short switching times;
4. ability to block high values of direct and inverse voltages;
5. high direct current values;
6. a positive temperature coefficient for conduction resistance (this ensures that the devices in parallel share the current equally).

Since the GaN HEMTs reach all these requirements, they are the right successors to Si mosfets.
The following chapters will be organized as follow: chapter 2 explains the steady state operation of the dual active bridge; chapter 3 presents the simulation and the total power losses during the charging path; chapter 4 describes the design of the high frequency transformer; chapter 5 describes the SPS control loops; chapter 6 tells the results; chapter 7 describes alternative control techniques.

2 Analysis of dual active bridge converter

The dual active bridge converter (DAB) is the most feasible to operate a DC/DC conversion, since it has a simple structure, high power density, capability of soft-switching, possibility to work in buck/boost mode, small number of devices, capability of bidirectional power flow (needed to accomplish regenerative braking and v2g operations) and easy control way with single phase shift modulation.
The corresponding circuit is drawn in figure 2.1: there are two active full bridges that can operate both as inverter or as rectifier, interleaved by a high frequency transformer that guarantees galvanic isolation and makes possible to connect parts of the circuit with different voltage ranges.
The converter can work in two different mode:

- forward mode: in this case the power flows from the grid towards the load; the input bridge acts as an inverter, transforming the voltage from DC to AC, instead the output bridge transforms the voltage from AC to DC; the AC conversion is necessary to transfer the power through the high frequency transformer;

- backward mode: if an active load is linked at the output bridge, through an opportune modulation technique it is possible to transfer the power towards the grid, thanks to the symmetry of the converter.

Downstream the output bridge, in parallel to the load (battery), there's a capacitance that on one hand smooths the DC voltage across the load, on the other hand it acts like a short circuit for all the high order harmonics present in the output current, due to the switching converter.
Upstream the input bridge there are the inductor and the four electrolytic capacitances that allow to smooth the voltage and the current outgoing from the power factor corrector. The quantity of power transmitted by the converter can be regulated varying the phase shift dT_{hf} between the two bridges. This chapter describes the steady state operation in forward and backward mode (considering ideal switches), investigates the magnitude of the current that flows in the devices, discusses the soft switching behaviour, introduces a procedure to find the optimal value of the leakage inductance in order to minimize the current stress and presents a fast computation for what concern the output parallel capacitance.

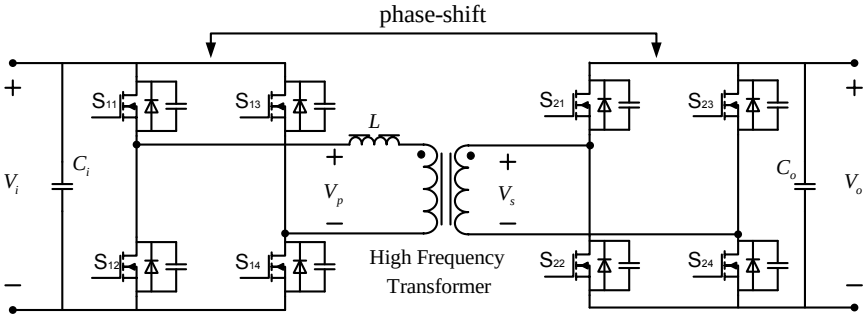


Figure 2.1: DAB circuit with single phase shift control.

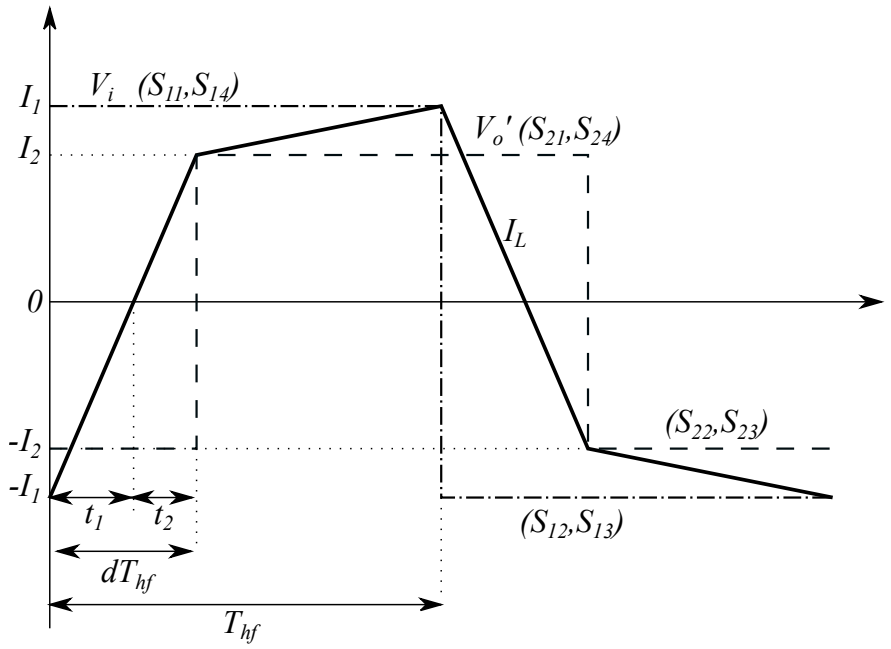


Figure 2.2: Voltage and leakage inductance waveforms in buck mode.

2.1 Forward mode

The easiest and most widely used control technique for the dual active bridge is the single phase shift (SPS). In this control strategy each switch is controlled by a square-wave gate signal with 50% duty ratio. Imaging in this first analysis to neglect the dead time, the cross-connected switches pairs in both full bridges are switched in order to generate phase shifted voltage square waves with 50% duty cycle to the transformer's primary and secondary windings [9]. It's clear that in this way the only freedom degree to manage the value of the output power is the phase shift between the two bridges and no other inner control variables. This shift can assume both positive and negative values: if it's desired to transfer power from the input to the output bridge, the first one has to lead the second one and so the phase shift will be positive (forward mode), otherwise it will be negative (backward mode).
The control of the power flow relies on the transformer's leakage inductance and this will lead to circulating current when the magnitude of the two square-wave voltages, applied to both sides of the transformer, doesn't match. Another drawback is the restrict region in which the converter can exhibit zero voltage switching (ZVS) turn on of the switches. In order to overcome these problems, other control techniques have been proposed, all focused to increase the number of freedom degrees in which it would be possible to act to guarantee small value of reactive power and increase the ZVS capability. In this work, however, the SPS modulation has been applied, in order to verify its limits and after that apply some efforts to overcome them.
In figure 2.2 are represented the two voltage waveforms applied to the transformer and the leakage inductance current, referred to the primary side of the transformer. The operating mode is buck (the voltage applied by the input bridge is greater than that one of the output bridge) and forward, since the input bridge leads the output one. Neglecting the parasitic capacitances of each switch, the current presents a trapezoidal shape, consisting of straight lines with different slopes. It has to be underlined also that the converter operates in continuous conduction mode.
The voltage and current waveforms have half-wave symmetry and hence in their Fourier expansion the even terms lack. Another consequence of this half-symmetry is the possibility to deduce the equations of the leakage inductance current for half cycle (T_{hf}).

Taking in mind Faraday's law, the leakage inductance current can be calculated integrating its derivative:

$$\frac{di_L}{dt} = \frac{v_i - \frac{v_o}{n}}{L} \tag{2.1}$$

Looking at the draft in figure 2.2, along the half switching period, it's possible to identify two main time intervals, in which the current slope changes since the voltages applied at the inductance terminals change their sign:

$$\begin{cases} v_i + \frac{v_o}{n} = L\frac{I_1+I_2}{dT_{hf}}, & \text{for } 0 < t < dT_{hf} \\ v_i - \frac{v_o}{n} = L\frac{I_1-I_2}{(1-d)T_{hf}}, & \text{for } dT_{hf} < t < T_{hf} \end{cases} \tag{2.2}$$

In the above system I_1 represents the absolute value of the leakage inductance current when the leading bridge is switched, whilst I_2 represents the absolute value of the current when the lagging bridge is switched. From the first equation of the system (2.2) it's possible to express the I_1 current in function of I_2 and substitute it in the second equation, in order to find an expression of the lagging bridge switched current as a function of the design parameters:

$$\begin{cases} I_1 = (v_i + \frac{v_o}{n})\frac{dT_{hf}}{L} - I_2 \\ v_i - \frac{v_o}{n} = L\frac{(v_i+\frac{v_o}{n})\frac{dT_{hf}}{L} - I_2 - I_2}{(1-d)T_{hf}} \end{cases} \tag{2.3}$$

After some mathematical steps, the final expressions of the switched currents are:

$$\begin{cases} I_1 = \frac{T_{hf}}{2L}(2\frac{v_o}{n}d + v_i - \frac{v_o}{n}) \\ I_2 = \frac{T_{hf}}{2L}(2v_i d - v_i + \frac{v_o}{n}) \end{cases} \tag{2.4}$$

Focusing on the phase shift time interval dT_{hf} it's possible to make an equality between the triangle with t_1 as base and that one with t_2 as base:

$$\frac{I_1}{t_1} = \frac{I_2}{t_2} \quad \text{where } t_1 + t_2 = dT_{hf} \tag{2.5}$$

The final expression of the two time intervals are the following:

$$t_1 = T_{hf}(\frac{2\frac{v_o}{n}d + v_i - \frac{v_o}{n}}{2(v_i + \frac{v_o}{n})}) \tag{2.6}$$

$$t_2 = T_{hf}(\frac{2v_i d - v_i + \frac{v_o}{n}}{2(v_i + \frac{v_o}{n})}) \tag{2.7}$$

The equation (2.6) allows to compute the current shift time instant. Looking at the system (2.4) it appears that both the currents could be negative and this fact would compromise the theoretical soft switching capabilities of the converter. The boundary shift time dT'_{hf} can be computed putting I_2 equal to zero and it results:

$$0 = 2v_i dT'_{hf} - v_i T_{hf} + \frac{v_o}{n}T_{hf} \tag{2.8}$$

$$dT'_{hf} = \frac{T_{hf}}{2}(1 - \frac{v_o}{nv_i}) \tag{2.9}$$

The load current, i.e. that one that flows inside the load, is calculated as the average value of the output current, depicted in figure (2.3); this value is equal to the sign sum of the area under the graph, divided by the half switching

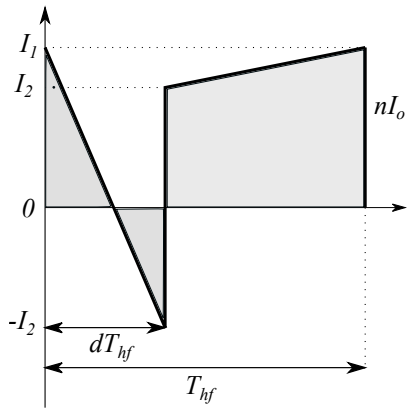


Figure 2.3: Output current referred to the primary side.

period T_{hf}:

$$I_{o,avg} = \frac{1}{nT_{hf}}(\frac{1}{2}I_1t_1 - \frac{1}{2}I_2t_2 + (1-d)T_{hf}I_2 + (1-d)T_{hf}\frac{1}{2}(I_1 - I_2)) \tag{2.10}$$

Substituting the expressions of I_1 and I_2 (found in the system (2.2)) and those ones of t_1 and t_2 (see equations (2.6) and (2.7)), it's possible to obtain a relationship between the average output current and other parameters of the circuit, as shown in the following steps:

$$\begin{aligned} I_{o,avg} = {} & \frac{1}{nT_{hf}}(\frac{1}{2}\frac{T_{hf}}{2L}(2\frac{v_o}{n} + v_i - \frac{v_o}{n})T_{hf}(\frac{2\frac{v_o}{n}d + v_i - \frac{v_o}{n}}{2(v_i + \frac{v_o}{n})}) - \\ & \frac{1}{2}\frac{T_{hf}}{2L}(2v_id - v_i + \frac{v_o}{n})T_{hf}(\frac{2v_id - v_i + \frac{v_o}{n}}{2(v_i + \frac{v_o}{n})}) + (1-d)T_{hf}\frac{T_{hf}}{2L}(2v_id - v_i + \frac{v_o}{n}) + \\ & \frac{1}{2}(1-d)\frac{T_{hf}^2}{2L}(2\frac{v_o}{n}d + v_i - \frac{v_o}{n} - 2v_id + v_i - \frac{v_o}{n})) \end{aligned} \tag{2.11}$$

Leaving to the reader the simple mathematical developments, here it's stated the final expression:

$$I_{o,avg} = \frac{(1-d)dT_{hf}v_i}{nL} \tag{2.12}$$

Equation (2.12) is obtained considering an output current waveform that doesn't take into account the presence of the parasitic output capacitances of the switches; for this reason the average output current depends just on:

- the phase shift time interval between the two bridges;
- the input voltage;
- the leakage inductance of the high frequency transformer.

Since it doesn't depend on the output voltage, it means that, downstream the output maintenance capacitance, the converter acts as a current generator which value is independent on the load rate. To make a plot of the output current as function of the dimensionless phase shift d, it's possible to divide it by its base value $I_{base} = \frac{v_i}{nL}$, getting the per unit expression:

$$I_{o,pu} = (1-d)d \tag{2.13}$$

Making the derivative of $I_{o,pu}$with respect d and putting it equal to zero, it's possible to see that it reaches a maximum

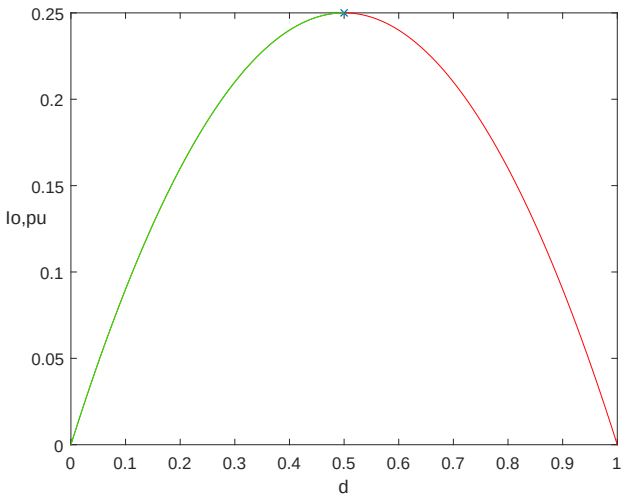


Figure 2.4: Load current as a function of the dimensionless phase shift d.

value with a phase shift of the 50%, as can be seen in figure 2.4. It appears evident that for a stable working the value of the parameter d has to be smaller than 0.5, in order to move on an almost straight line way of the output current.
Multiplying the average output current of equation (2.12) by the load resistance R_L, it figures the expression of the output voltage:

$$v_o = R_L \frac{(1-d)dT_{hf}v_i}{nL} \tag{2.14}$$

The voltage v_o directly depends on the load resistance: if the load is heavy (small value of R_L) then the converter will work in buck mode, otherwise it will shift into boost mode. The limit boundary between these two operation modes is obtained equating the input and output voltage of the converter:

$$v_i = R_L \frac{(1-d)dT_{hf}v_i}{nL} \tag{2.15}$$

$$R_{L,bound} = \frac{nL}{(1-d)dT_{hf}} \tag{2.16}$$

Equation (2.16) shows the value of the load resistance that makes the converter shifts among the two modes: if the external resistance is smaller than $R_{L,bound}$, then the converter will be in buck mode, otherwise it will work in boost mode.
The delivered active power is equal to the product among the average output current and the output voltage:

$$P_o = v_o \frac{(1-d)dT_{hf}v_i}{nL} \tag{2.17}$$

As stated before, in order to work in a stable range, the phase shift should be smaller than the 50%. The input current waveform is shown in figure (2.5). Through the area analysis, the average input current figures as:

$$I_{i,avg} = \frac{1}{T_{hf}}(\frac{1}{2}I_2t_2 - \frac{1}{2}I_1t_1 + (1-d)T_{hf}I_2 + (1-d)T_{hf}\frac{1}{2}(I_1 - I_2)) \tag{2.18}$$

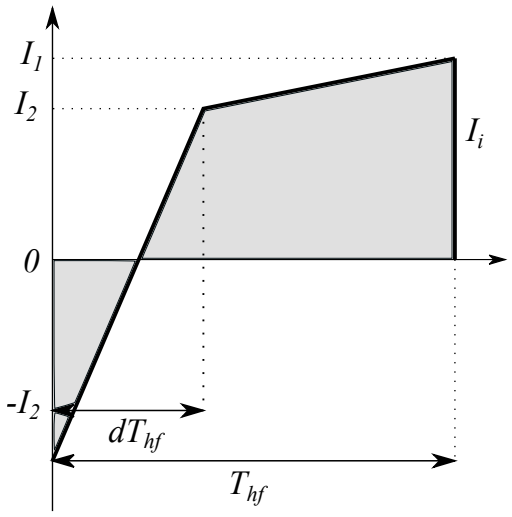


Figure 2.5: Input current.

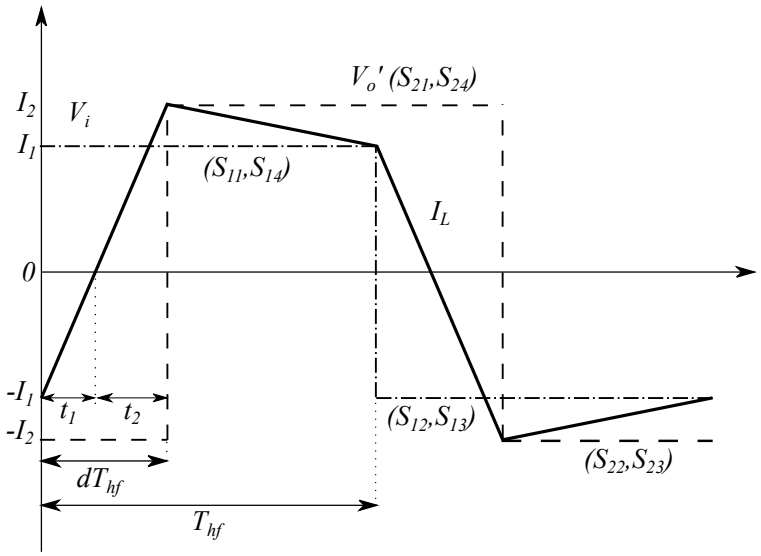


Figure 2.6: Converter current and voltages in boost mode.

Like done for the computation of the average output current, substituting (2.4), (2.6), (2.7) into (2.18) the final expression results:

$$I_{i,avg} = \frac{(1-d)dT_{hf}v_o}{nL} \tag{2.19}$$

As written above, if the output voltage is higher than the input one, the converter will work in boost mode: in this case, the leakage inductance current reaches its peak value after the phase shift interval dT_{hf} and so I_2 will be greater than I_1. In this case the current shift time t_1 will be smaller with respect the buck mode. The expression of the average output current in boost mode is the same of that one found for the buck mode (the main waveforms are plotted in picture 2.6); as a consequence of it, also the output voltage and the transmission power equations don't change.

2.2 Reverse mode

If at the output port of the DC/DC converter is linked an active load, as in the case of a battery in an automotive application, making the output bridge leads the input bridge, it's possible to invert the power flow and so get power from the battery to passive loads or to the grid. To do that, the dimensionless phase shift d has to assume negative values.

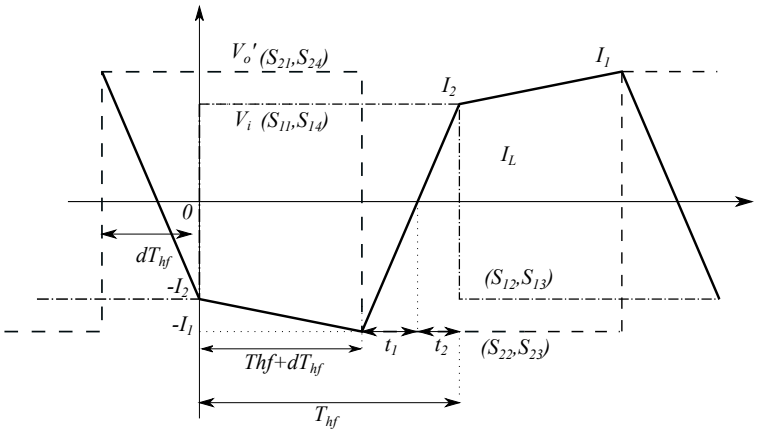


Figure 2.7: Current and voltage waveforms in reverse buck mode.

To study the behaviour of the current in the leakage inductance, it has to be noted that now the voltage of the output bridge is the input converter voltage (hence it has to be referred to the primary side) and the voltage of the input bridge is the new output voltage of the whole DC/DC converter, as shown in figure 2.7, so the buck backward mode is obtained with $V_o' > V_i$. Looking at the time intervals shown in figure 2.7, it's possible to deduce the following mathematical expressions:

$$\begin{cases} v_i - \frac{v_o}{n} = L\frac{-I_1+I_2}{T_{hf}+dT_{hf}}, & \text{for } 0 < t < T_{hf} + dT_{hf} \\ v_i + \frac{v_o}{n} = L\frac{I_1+I_2}{-dT_{hf}}, & \text{for } T_{hf} + dT_{hf} < t < T_{hf} \end{cases} \tag{2.20}$$

This time I_1 represents the absolute current value at the instant in which the output bridge is switched, instead I_2 is the absolute value at the instant in which the input bridge is switched.
Rearranging the system equations (2.20) it's possible to express I_1 as a function of I_2:

$$\begin{cases} (v_i - \frac{v_o}{n})(\frac{T_{hf}+dT_{hf}}{L}) = \frac{dT_{hf}}{L}(v_i + \frac{v_o}{n}) + 2I_2 \\ I_1 = (v_i + \frac{v_o}{n})(\frac{-dT_{hf}}{L}) - I_2 \end{cases} \tag{2.21}$$

Solving the (2.21), the two current values in the buck backward operation are equal to:

$$\begin{cases} I_1 = \frac{T_{hf}}{2L}(\frac{v_o}{n} - v_i - 2dv_i) \\ I_2 = \frac{T_{hf}}{2L}(v_i - \frac{v_o}{n} - 2\frac{v_o}{n}d) \end{cases} \tag{2.22}$$

Once again, doing an equality between the triangles with t_1 and t_2 like bases:

$$\frac{I_1}{t_1} = \frac{I_2}{t_2} \tag{2.23}$$

and remembering that the sum of t_1 and t_2 is equal to dT_{hf}, the two time intervals result:

$$t_1 = \frac{2v_i d - \frac{v_o}{n} + v_i}{2(\frac{v_o}{n} + v_i)} T_{hf} \tag{2.24}$$

$$t_2 = \frac{2\frac{v_o}{n} d + \frac{v_o}{n} - v_i}{2(\frac{v_o}{n} + v_i)} T_{hf} \tag{2.25}$$

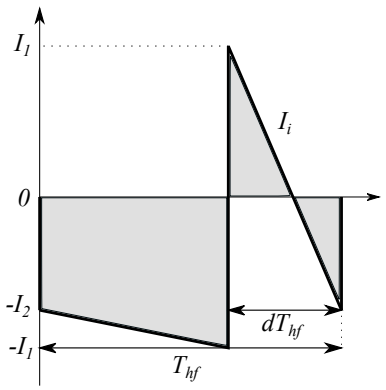


Figure 2.8: Output current in the buck reverse mode.

Also in this case, applying the criterion of the areas at the waveform in figure 2.8, the average value of the output current can be computed as:

$$I_{o,avg} = \frac{1}{T_{hf}}(-I_2(T_{hf} + dT_{hf}) - \frac{1}{2}(T_{hf} + dT_{hf})(I_1 - I_2) + \frac{1}{2}t_1 I_1 - \frac{1}{2}t_2 I_2) \tag{2.26}$$

Substituting (2.22), (2.24) and (2.25) into (2.26), the average value of the output current in the backward mode corresponds to:

$$I_{o,avg} = \frac{(1+d)dv_i T_{hf}}{L} \tag{2.27}$$

Multiplying (2.27) by the primary referred voltage of the output bridge $\frac{v_o}{n}$, the average output power results:

$$P_o = \frac{v_o}{n}\frac{(1+d)dv_i T_{hf}}{L} \tag{2.28}$$

The module of the maximum power (obtained in correspondence of $d = \pm\frac{1}{2}$) of the isolated bidirectional converter with SPS control is:

$$P_n = \frac{v_i v_o T_{hf}}{4nL} \tag{2.29}$$

Dividing both (2.28) and (2.17) by (2.29) it's possible to express the transmitted power in per unit value for positive and negative phase shift:

$$P_{t,pu} = 4d(1 - |d|) \tag{2.30}$$

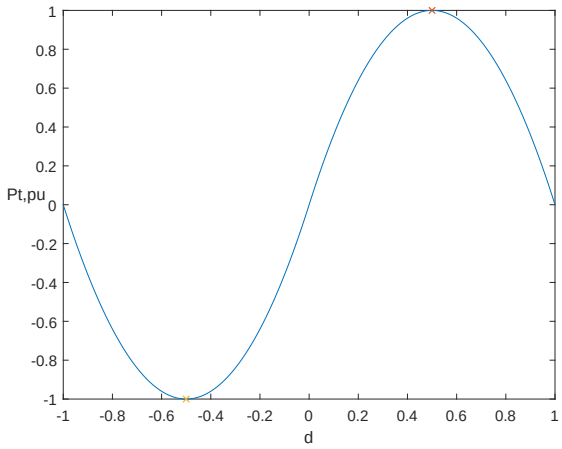


Figure 2.9: Normalized transmitted power as a function of d.

Figure 2.9 shows the power waveform under single phase shift control. As stated before on the occasion of the analysis of the average output current of the converter, to guarantee stability the value of d has to be in the range $[-0.4; 0.4]$. The boost backward mode is not explored since the main function of the converter is to transfer the power from the grid towards the battery, however it's quite unusual the boost backward mode since the battery stack voltage of modern EVs is in the order of 500 [V] and it should be stated that the battery could inject power in the grid especially when it's full charged, preventing deep discharging that could damage its interior structure.

2.3 Soft switching

The study of the soft switching capability is made only for the forward mode.
In circuits that have some inductance, it's important to put diodes in anti-parallel to the ideal switches, in order to create a flow path for the current when the switches are opened. In the hard operating mode the circuit-breakers are subjected to high stresses which give rise to large losses, the latter being linearly dependent on the switching frequency.

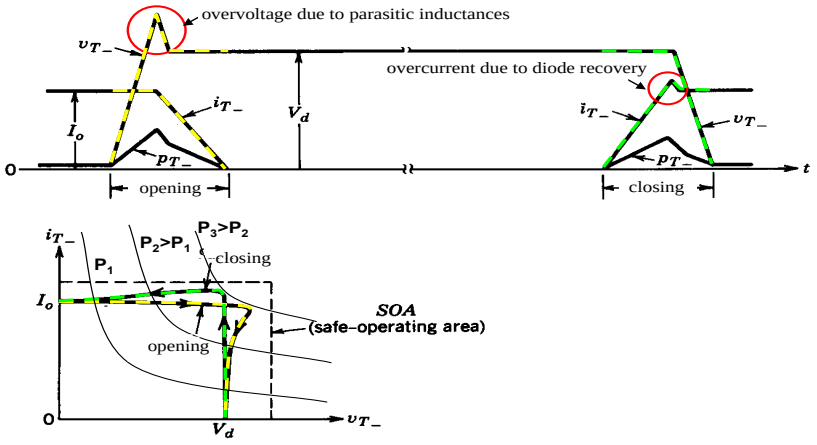


Figure 2.10: Opening and closing hard switching stresses.

Another disadvantage of the hard operation is related to the high derivatives of voltage and current, which cause the appearance of problems of electromagnetic interference. In order to reduce the aforementioned drawbacks, each switch of the converter shifts from opened to closed (or vice versa) at the instant in which the voltage and/or current passing through it are null; in order to operate this switching technique the resonance of the LC circuits is exploited.
As it can be seen in figure 2.10, during hard switching commutation it is possible to overcame the boundaries of the safe-operating area (SOA), destroying the semiconductor devices. The stresses in the circuit-breakers can be reduced by inserting simple protection dissipative circuits, consisting essentially of diodes and passive components (inductances and capacitors) placed in series or in parallel with the switches themselves. If it is true that on one hand the snubber circuits allow the stresses to be reduced, they become a source of losses and delays in switching speed.

2.3.1 DAB working regarding output parasitic capacitances

In half switching period two commutations happen: one inside the input bridge and the other one inside the output bridge, hence it's possible to individuate 2 major intervals of switches conduction, as shown in figure 2.11. The four switches in each full bridge are driven in cross couples, in order to prevent short circuit of the input source voltage or across the output load; furthermore, a sufficient dead time has to be put between the turned off signal of a couple of switches and the turned on signal of the complementary couple, to avoid simultaneous conduction of switches belonging to the same leg of the converter. The AC stage of the dual active bridge consists of a transformer: it's known that it's not possible to suddenly interrupt an inductive source current. To simplify the analysis, a primary referred equivalent circuit is considered: the transformer is replaced by its leakage inductance (it's assumed that its magnetizing inductance is such high that it can be considered like an open circuit, making possible to neglect the magnetizing current); the coupling capacitances and resistances of the windings are neglected.
Considering the first interval $[0 < t < dT_{hf}]$, in figure 2.12 is presented the different distribution of the current in the output bridge devices. Picture 2.12(a) shows fully switches conduction. At time instant dT_{hf} the input bridge semiconductors S_{11} and S_{14} are in full conduction, whilst the devices in the output bridge are switched each other: S_{22} and S_{23} will be turned off and after an appropriate dead time S_{21} and S_{24} will be turned on. Thanks the very high switching frequency feasible by GaN HEMTs, additional snubber capacitances are not required to ensure a small voltage derivative value, in fact if the output capacitances aren't enough big, there would be a high rate of initial current fall ($\frac{di}{dt}$) and consequently voltage spikes across the semiconductor devices (as shown in figure 2.10). At the beginning of the transition between interval 1 and 2, the conducting switches are turned off and the stored inductive energy causes the leakage inductance current to continue to flow. Thanks the previous parallel switches conduction, the voltages across the output capacitance C_{s22} and C_{s23} are zero (neglecting the voltage drop across the transistors while they conduct). On the other side, the initial voltages of C_{s21} and C_{s24} are equal to v'_o. During the dead time, in which all the four power switches are interdicted, the leakage inductance current has to flow through other devices: it can't flow through diodes D_{21} and D_{24} since they are reversed polarized due to the initial voltage v'_o, on the other hand it can't neither flow through diodes D_{23} and D_{22} since they are able to conduct just negative current; for this reason it divides in two equal parts to discharge the capacitances C_{s21} and C_{s24} and charge the capacitances C_{s22} and C_{s23}, as can be seen in figure 2.12(b). Once this resonance interval is finished, the voltage across the capacitances C_{s21} and C_{s24} is clamped to zero thanks to the anti-parallel diodes D_{21} and D_{24} that start to conduct (see figure 2.12(c)): after this moment it is possible to send the gate signal and turn on simultaneously the switches S_{21} and S_{24}, getting a zero voltage switching turning on, as shown in fig. 2.12(d). The capacitances and diodes behaviours are summarized in table 2.1. It appears that to ensure soft turning on of S_{21} and S_{24} it's necessary that their anti-parallel diodes conduct and this is possible only if the leakage inductance current in the transition between interval 1 and interval 2 has a positive value I_2: this is the first ideal restriction for what concern the output bridge.
At the end of interval 2 (see fig. 2.11) there's a commutation between the switches in the input bridge: S_{11} and S_{14}

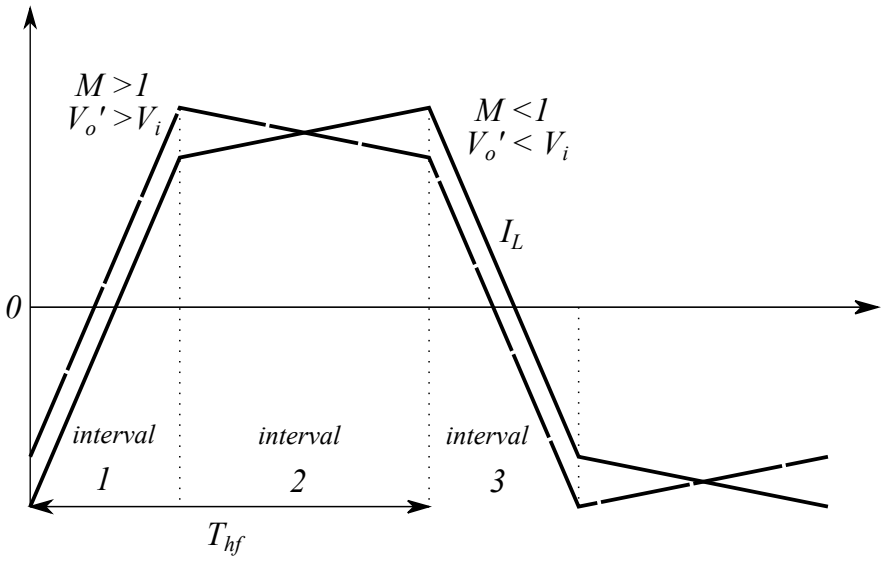


Figure 2.11: Steady-state conduction intervals in buck/boost mode.

Table 2.1: Roles of the devices involved in ZVS turning on of output bridge switches with positive inductive current.

ZVS in the output bridge			
C_{s21}	$V_o' \to 0$	D_{21}	off $\to$ on
C_{s24}	$V_o' \to 0$	D_{24}	off $\to$ on
C_{s22}	$0 \to V_o'$	D_{22}	off
C_{s23}	$0 \to V_o'$	D_{23}	off

will be turned off, instead S_{12} and S_{13} will be turned on. During the dead time, in which all the four switches are opened, the leakage inductance current has to continue to flow: since it's positive, it can't flow through diodes D_{11} and D_{14}, neither through the remaining two diodes since they are reversed biased; for this reason it splits in equal parts into the four capacitances in order to charge capacitances C_{s11} and C_{s14} and discharge the capacitances C_{s12} and C_{s13}. When the voltage across these last ones tends to become negative, since the inductance current at the transition instant I_1 is positive, the diodes D_{12} and D_{13} turn on, clamping the voltage across their anti-parallel switches to zero. The statuses of the devices conduction in the input bridge are summarized in table 2.2. Downstream this analysis it appears that in order to ensure ZVS in the input bridge, the value of the inductance current at the transition instant has to be positive, in order to allow "body diodes" conduction before sending the gate signal to the transistors.
In power electronics there are two main ways in order to decrease the switching power losses:

- turning on the switch with zero current (ZCS);
- turning on the switch with zero voltage (ZVS).

Table 2.2: Roles of the devices involved in ZVS turning on of input bridge switches with positive inductive current.

ZVS in the input bridge			
C_{s11}	$0 \to V_i$	D_{11}	off
C_{s14}	$0 \to V_i$	D_{14}	off
C_{s12}	$V_i \to 0$	D_{12}	off $\to$ on
C_{s13}	$V_i \to 0$	D_{13}	off $\to$ on

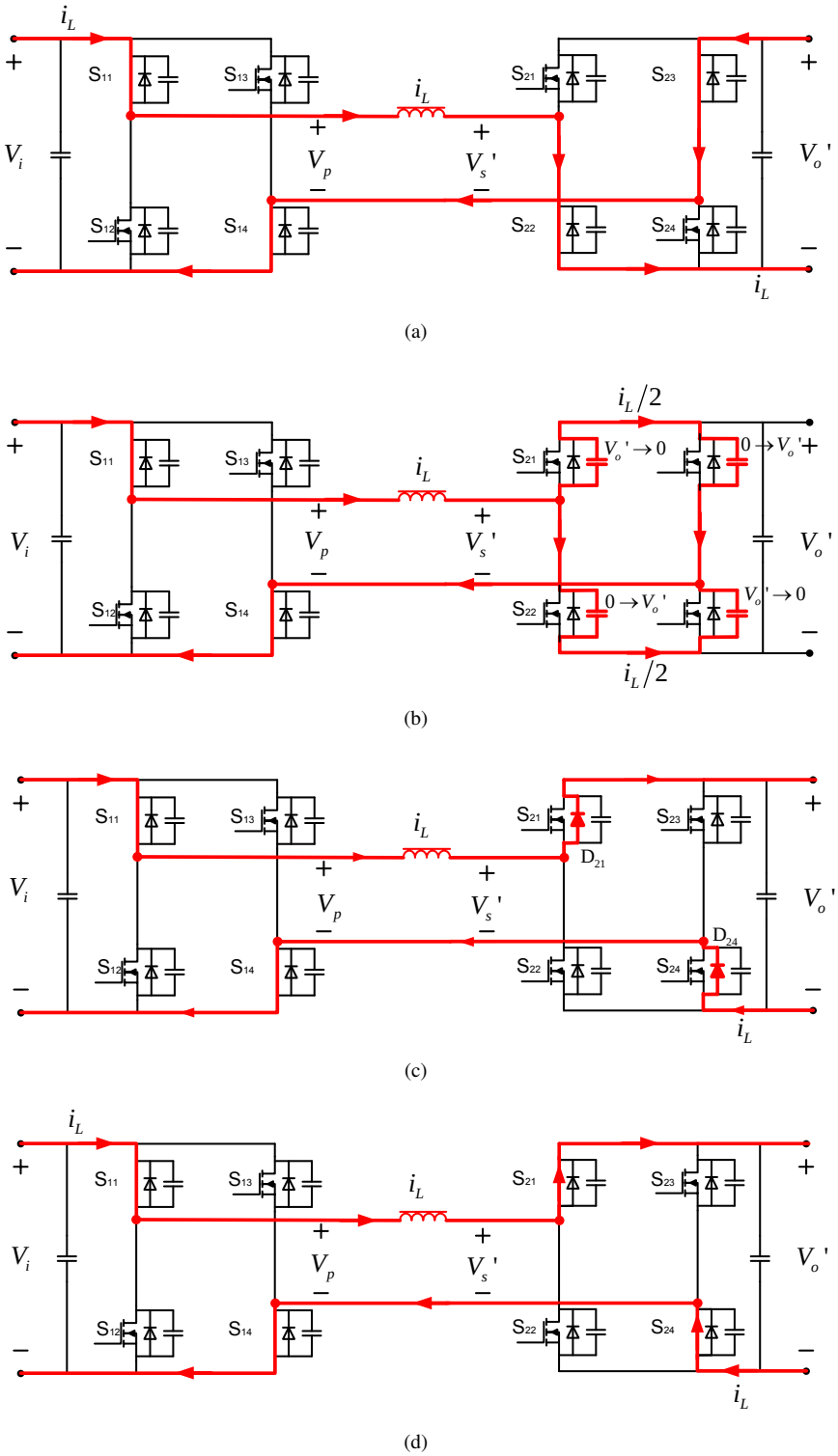


Figure 2.12: Current paths in the output bridge during a commutation interval.

Considering the very high switching frequency of the charger, devices with field effect are used. They presented some parasitic capacitances (as explained in the GaN chapter) that are dangerous if big voltage derivatives occur across the power device: for this reason, in such a case, ZVS must be sought.
Neglecting the energy required to charge/discharge the parasitic output capacitances, it's possible to define the boundaries of ZVS for the input and the output bridges.
Defining the ratio between the primary referred output voltage and the input voltage as:

$$M = \frac{v_o}{n v_i} \tag{2.31}$$

the current expressions (2.4) can be rewritten as:

$$\begin{cases} I_1 = \frac{T_{hf} v_i}{2L}(2Md + 1 - M) \\ I_2 = \frac{T_{hf} v_i}{2L}(2d - 1 + M) \end{cases} \tag{2.32}$$

It appears that if $M = 1$, both I_1 and I_2 are greater than zero and so the ZVS can be obtained also with narrow load. Contrariwise, when $M \neq 1$, the necessary condition to execute ZVS can be fulfilled only with minimum values of phase shift and hence a minimum output power flow [10].
Distinguishing the two cases:

- if $M < 1$ the converter works in buck mode and I_1 is always positive, instead I_2 could be negative, causing hard switching operations in the output bridge;
- if $M > 1$ the converter works in boost mode and I_2 is always positive, whilst I_1 could be negative, not allowing soft switching in the input bridge.

In order to comply with the two limitations mentioned above, it's necessary to not overcome some boundaries in the working region. For the output bridge the boundary is defined just with $M < 1$, so to get positive value of I_2, a minimum value of dimensionless phase shift has to be got:

$$0 < 2d - 1 + M \tag{2.33}$$

$$d > \frac{1 - M}{2} \tag{2.34}$$

For what concern the input bridge the boundary appears just with $M > 1$ and hence, to match positive value of I_1, a minimum rate of phase shift must be got:

$$0 < 2Md + 1 - M \tag{2.35}$$

$$d > \frac{M - 1}{2M} \tag{2.36}$$

The minimum load rates (minimum values of output current) to ensure the ZVS turning on in both bridges are plotted in figure 2.13; as it can be seen, with high phase shift values, the zero voltage switching is achieved also with value of voltage ratio quite different from 1. These boundaries take into account only the aspect regarding the requirement of clamping null voltage across the switches through body diode conduction (although in GaN HEMTs the voltage drop during their conduction is not negligible as for usual diodes).
Without the parasitic output capacitances that act like snubber capacitances, at the instant of turning off, the voltage across the transistors would instantaneously rise to the voltage of the respective bridge; since capacitors accept current discontinuity, they conduct the devices turn off current, reducing the derivative of the voltage across the switches. In this way, since the current device can flow through the capacitances and the voltage rises slowly, the turning off losses

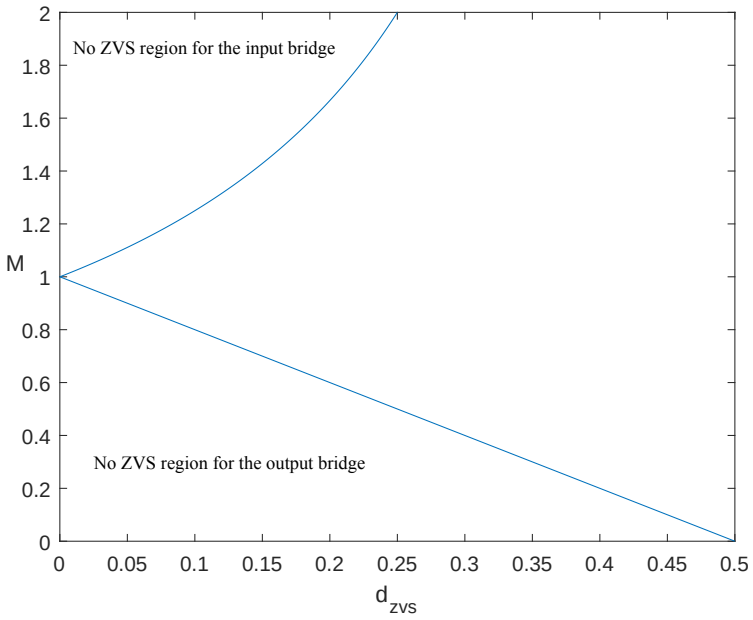


Figure 2.13: Necessary condition to achieve ZVS in the leading and lagging bridge.

are minimized.

2.3.2 Required minimum current to ensure ZVS

The presence of the parasitic output device capacitances on one hand ensure to decrease the slope of the rising voltage across the turning off transistors, but on the other hand it requires more energy to be stored in the leakage inductance in order to get zero voltage switching. To make an energy balance, an equivalent primary referred circuit is considered during input bridge commutation, as shown in figure 2.14, where $v_o' = \frac{v_o}{n}$. The voltages across the two full bridges are considered to remain constant during the resonant transient. It's assumed that an instant before the switches S_{11} and S_{14} were in full conduction (their respective output capacitances were discharged) instead S_{12} and S_{13} were interdicted (their respective parallel capacitances were charged). All the capacitances have the same value and remembering that the current is alternated, it looks like the two capacitances in each leg are in parallel (hence the equivalent capacitance of one leg is $2C_s$). Since the inductance current flows in both legs, the two equivalent capacitances are also in series, so the total capacitance of the resonant circuit is C_s.
To ensure ZVS and a small interval of time in which the circuit is in "free development" (in fact during the capacitances charging/discharging process there's no active control on the circuit, the oscillations are related to hardware), the resonance frequency $\omega_o = \frac{1}{\sqrt{LC_s}}$ has to be much higher than the operating frequency of the converter. As stated before, the inductance current charges the capacitances C_{s11}, C_{s14} and discharges C_{s12} and C_{s13}. As can be seen in the equivalent circuit 2.14, the inductance current splits in two equal values in a leg and recombines itself in the other leg. Remembering that the capacitor current is related to the derivative of the voltage, $I_{Cs} = C_s \frac{dv_c}{dt}$, the leakage inductance current is expressed as:

$$I_L = 2C_s \frac{dv_c}{dt} \tag{2.37}$$

Considering negligible the internal resistance in parallel to the output capacitances, it appears that to ensure the ZVS operation, the energy stored in the leakage inductance has to be at minimum equal to the energy required to charge

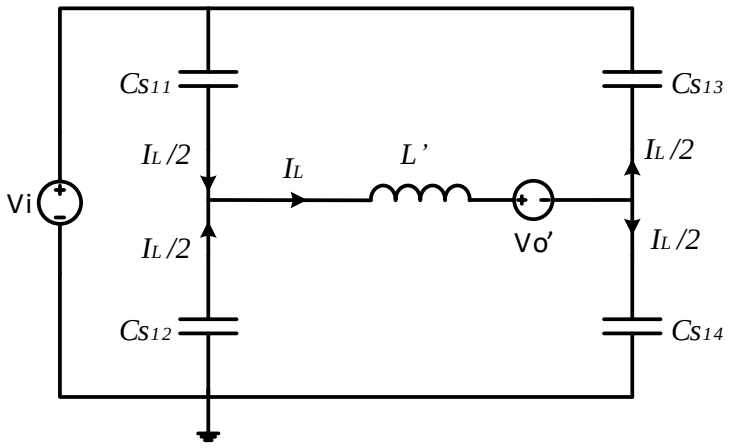


Figure 2.14: Equivalent circuit during turn off of S_{11} and S_{14}.

and discharge the aforementioned passive components:

$$\frac{1}{2}LI_L^2 = E_{Cs} \quad \text{where} \quad E_{Cs} = \frac{v_o}{n}I_L \tag{2.38}$$

The required energy can be computed integrating the expression of E_{Cs} over the device turn off time, $toff$:

$$E_{Cs} = \int_0^{toff} \frac{v_o}{n} I_L \, dt = \int_0^{toff} \frac{v_o}{n}(2C_s\frac{dv_c}{dt}) \, dt = 2C_s\frac{v_o}{n}\int_0^{toff} \frac{dv_c}{dt} \, dt = 2C_s\frac{v_o}{n}v_i \tag{2.39}$$

Equating the energy stored in the leakage inductance with that one required to charge/discharge the capacitances, the minimum required inductance current can be found:

$$\frac{1}{2}LI_L^2 = 2C_s\frac{v_o}{n}v_i \tag{2.40}$$

$$I_L = 2\sqrt{\frac{C_s\frac{v_o}{n}v_i}{L}} \tag{2.41}$$

Defining the characteristic impedance Z_o as the square root of the ratio between the leakage inductance L and the total capacitance C_s, the final expression of the minimum leakage inductance current is:

$$I_L = \frac{2}{Z_o}\sqrt{v_i\frac{v_o}{n}} \tag{2.42}$$

The current I_1 at the commutation instant of the input bridge could be negative in boost mode operation, hence, considering the switches' capacitances, the current I_1 has not more to be just greater than zero, but it has also to be greater than the minimum value of I_L:

$$\frac{T_{hf}v_i}{2L}(2Md + 1 - M) > \frac{2}{Z_o}\sqrt{v_i\frac{v_o}{n}} \tag{2.43}$$

Solving (2.43) with respect of d, a new restricting limitation is got for the input bridge, especially in boost mode operation:

$$d > \frac{1}{2} - \frac{1}{2M} + \frac{2}{T_{hf}}\sqrt{\frac{LC_s}{M}} \tag{2.44}$$

The same reasoning can be done for the output bridge: in that case the current value I_2 has to be greater than the minimum current required for charging/discharging the capacitances:

$$\frac{T_{hf} v_i}{2L}(2d - 1 + M) > \frac{2}{Z_o}\sqrt{v_i \frac{v_o}{n}} \tag{2.45}$$

Making some simplification it's possible to extract from (2.45) the expression of the minimum required dimensionless phase shift to ensure ZVS in the output (lagging) bridge, especially in buck mode operation:

$$d > \frac{1}{2} - \frac{M}{2} + \frac{2\sqrt{LC_sM}}{T_{hf}} \tag{2.46}$$

Although inclusion of parasitic capacitances allows to decrease the devices stress, it restricts the ZVS available region [11].
Furthermore the soft switching commutations result strictly dependent on the hardware, the value of the designed leakage inductance and the working frequency.

2.3.3 Current and voltage equations during resonance interval

As stated in the previous paragraph, during each commutation the leakage inductance resonates with the output devices capacitances.

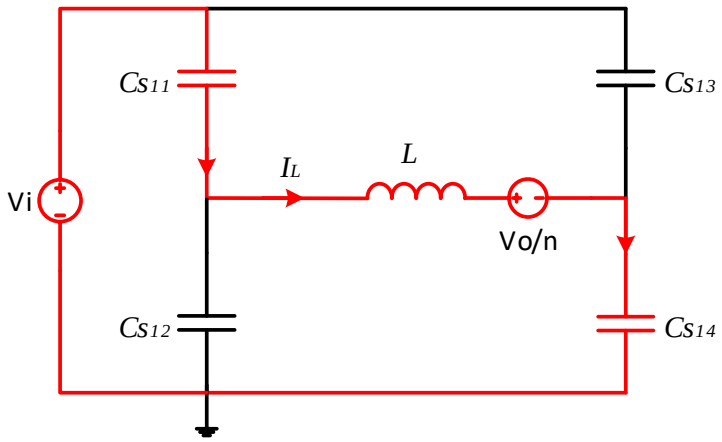


Figure 2.15: Equivalent circuit during turn off S_{11} and S_{14} showing the voltage mesh.

In order to find the expression of the leakage inductance current and of the voltage across an output capacitance, the equivalent circuit plotted in figure 2.15 is considered. The circuit refers to the transition from interval 2 to interval 3 (remembering fig. 2.11), hence the commutation occurs in the input bridge.
The ZVS turn on time for switches S_{12} and S_{13} is defined as the interval between the turn off instant of S_{11} and S_{14} and the moment in which the inductance current, decreasing from I_1 positive value, intersects the abscissa axis. During the resonance the input and output voltages are considered constant.

The initial conditions in the input bridge are:

$$\begin{cases} U_{Cs11}(0) = 0 \\ U_{Cs14}(0) = 0 \\ U_{Cs12}(0) = v_i \\ U_{Cs13}(0) = v_i \\ I_L(0) = I_1 \end{cases} \tag{2.47}$$

The final conditions are:

$$\begin{cases} U_{Cs11}(t_1) = v_i \\ U_{Cs14}(t_1) = v_i \\ U_{Cs12}(t_1) = 0 \\ U_{Cs13}(t_1) = 0 \end{cases} \tag{2.48}$$

Considering the red mesh in fig. 2.15, using the current and voltage Kirchhoff's laws, the following equation system is obtained:

$$\begin{cases} v_i - U_{cs11}(t) - v_L(t) - \frac{v_o}{n} - U_{cs14}(t) = 0 \\ U_{cs11}(t) + U_{cs12}(t) = v_i \\ I_L(t) = C_{s11}\frac{dU_{cs11}}{dt} - C_{s12}\frac{dU_{cs12}}{dt} \end{cases} \tag{2.49}$$

Making clear $U_{cs12}(t)$ from the second equation of (2.49) and substituting it in the third equation, remembering that all capacitances have the same value (C), the expression of I_L is obtained:

$$\begin{cases} v_i - U_{cs11}(t) - L\frac{dI_L}{dt} - \frac{v_o}{n} - U_{cs14}(t) = 0 \\ U_{cs12}(t) = v_i - U_{cs11}(t) \\ I_L(t) = 2C_{s11}\frac{dU_{cs11}(t)}{dt} \end{cases} \tag{2.50}$$

In order to solve the resonant circuit, all the constant voltage sources are short circuited; substituting the last inductance current expression in the first equation of the system (2.50), the following differential equation is obtained:

$$2CL\frac{d^2U_{cs11}(t)}{dt^2} + 2U_{cs11}(t) = 0 \tag{2.51}$$

Solving the characteristic equation, two imaginary roots result: $s_{1,2} = \pm j\frac{1}{\sqrt{LC}} = \pm j\omega_o$, where $\omega_o = \frac{1}{\sqrt{LC}}$ is the resonance frequency.
The set of solutions of (2.51) is a vector space of dimension two. Considering the constant voltage sources, the permanent settlement solution (remembering that $U_{cs11} = U_{cs14}$) is:

$$U_{cs11} = \frac{v_i - \frac{v_o}{n}}{2} \tag{2.52}$$

The whole expressions are given by the sum of the permanent settlement solution and the transitory one, as shown

Table 2.3: Working parameters of the charger.

Parameter	Value
Nominal power	3.7 [kW]
Input voltage	380-420 [V]
Output voltage	270-470 [V]
Maximum output current	10 [A]
Switching frequency	500 [kHz]
Equivalent parasitic capacitances	850 [pF]

below:

$$\begin{cases} U_{cs11}(t) = \frac{v_i - \frac{v_o}{n}}{2} + Acos(\omega_o t) + Bsin(\omega_o t) \\ I_L(t) = -2C\omega_o Asin(\omega_o t) + 2CB\omega_o cos(\omega_o t) \end{cases} \tag{2.53}$$

To find the expressions of variables A and B, the initial conditions are used:

$$\begin{cases} 0 = \frac{v_i - \frac{v_o}{n}}{2} + A \quad \text{resulting } A = \frac{\frac{v_o}{n} - v_i}{2} \\ I_1 = 2CB\omega_o \qquad \text{getting } B = \frac{I_1}{2C\omega_o} = \frac{I_1 Z_o}{2} \end{cases} \tag{2.54}$$

The final expressions of the output capacitances voltage and inductance current during the resonance are:

$$\begin{cases} U_{cs11}(t) = \frac{v_i - \frac{v_o}{n}}{2} + \frac{\frac{v_o}{n} - v_i}{2} cos(\omega_o t) + \frac{I_1 Z_o}{2} sin(\omega_o t) \\ I_L(t) = I_1 cos(\omega_o t) - \frac{\frac{v_o}{n} - v_i}{Z_o} sin(\omega_o t) \end{cases} \tag{2.55}$$

2.4 Design of the leakage inductance and the output capacitance

Once the circuit specifications are given, the design of the converter rests on two parameters: the phase shift between the two bridges and the value of the leakage inductance. Usually the main goal is to obtain the maximum efficiency at full load condition but in the case of the dual active bridge, since the operation range is quite wide, there should be a trade off between the efficiency at maximum power and the efficiency over the whole operation range. As stated in the previous paragraph the switches losses increase rapidly when the commutations are hard; in order to ensure a big ZVS range, the leakage inductance should be as high as possible, allowing to use a big value of phase shift to transfer the required power and hence staying far from the boundaries of the zero voltage switching region.
On the other side, a big value of leakage inductance means a big value of reactive power and hence a higher value of the root mean square current that flows through the transformer's windings and the switches, increasing the conduction losses: for this reason, if it's known that the converter works almost all the time in full load condition, a small value of phase shift should be chosen, giving also a small leakage inductance in order to handle the maximum power, as it's possible to deduce remembering equation (2.17).

In order to compare these two main design strategies, it's necessary to consider the requirements of the dual active bridge that are summarized in table 2.3 for clarity. The value of the equivalent parasitic capacitances is the same for all the eight switches and it has been got by the data sheet: in each power device three different capacitances are present, id est the input (C_{iss}), the output (C_{oss}) and the reverse transfer (C_{rss}) ones. In particular the aforementioned

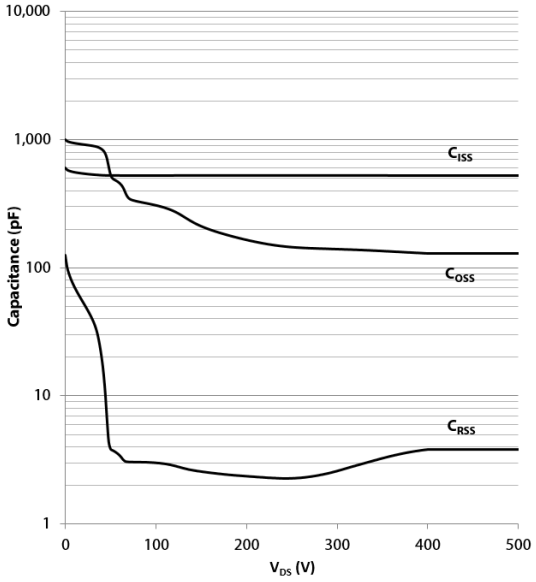


Figure 2.16: Parasitic capacitances of the GaN HEMT.

quantities are defined as:

$$C_{iss} = C_{GS} + C_{GD} \qquad \text{with } C_{DS} \text{ short circuited} \tag{2.56}$$

$$C_{rss} = C_{GD} \tag{2.57}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{2.58}$$

Among all the capacitances between gate, drain and source, the gate to drain one (C_{GD}) has a "heavy weight" in the real behaviour of the switch, because it's a non linear function of the voltage with respect the other ones that are linear functions with respect the applied voltage; this special behaviour is "the root" of the so called Miller capacitance, since it causes the total dynamic input capacitance to be grater than the static ones, increasing the energy required in each commutation to guarantee the soft switching turn on (and as a consequence it increases also the charging/discharging time and so the dead time required to be sure not incur in hard switching). Since at each commutation the voltage across each power device shifts from the maximum (on average 400 [V]) to zero volt, a reasonable design capacitance can be computed as the difference between the output and the reverse ones.

Taking a look in the graph 2.16, a proper value of the parasitic capacitance is equal to 850 [pF], as documented in the previous table.

2.4.1 Differences in the two opposite design strategies

This sub-paragraph presents the main differences that appear following the goal of increasing the ZVS range or maximizing the efficiency at full load working. Remembering the per unit power plot in figure 2.9, the maximum value of the phase shift can't be 0.5, since in this condition the transmitted power won't be any more linear, so a lower boundary of d_{max} has to be set, around 0.4. Substituting this value and the value of the nominal power in the expression (2.17), it's possible to compute the maximum value of the leakage inductance that allows to increase the soft switching range:

$$L = \frac{(1 - d_{max}) d_{max} T_{hf} v_i v_o}{nPn} \tag{2.59}$$

The turn ratio should be chosen in order to get a primary referred voltage ratio M equal to 1; considering the nominal value of the input voltage equal to 400 [V] and that one of the output voltage equal to 370 [V], it results a turn ratio $n = \frac{v_{o,nom}}{v_{i,nom}} = 0.925$. Since it's impossible to get such a value with a small number of turns (considering that the designed transformer is expected to be as small as possible), the turn ratio is selected equal to 1. Substituting the nominal value of the input and output voltages, nominal power, half switching period, maximum phase shift and turn ratio inside (2.59), it results a leakage inductance equal to 9.6 [μH].

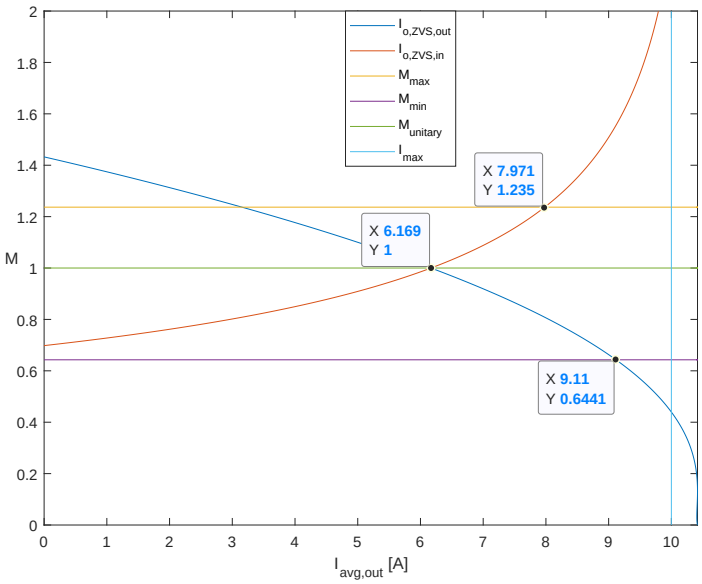


Figure 2.17: Minimum output current required to ensure ZVS with L=9.6 [μH].

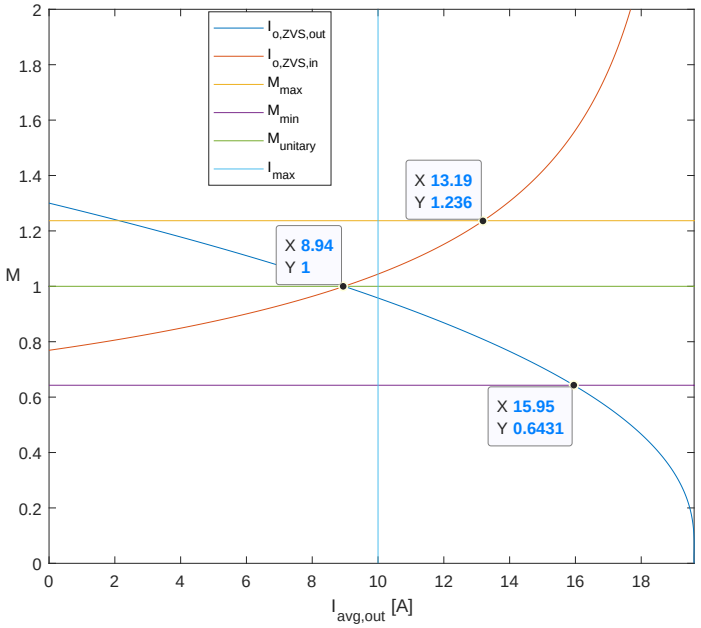


Figure 2.18: Minimum output current required to ensure ZVS with L=5.1 [μH].

On the other hand, following the aim to maximize the efficiency at full load, a minimum value of phase shift has to

be chosen that could also ensure ZVS at full load. A reasonable value for this kind of design is 0.15, giving a resultant inductance of 5.1 [μH].
As it's possible to see in figure 2.17, a bigger value of leakage inductance allows to get a wider ZVS range, making the minimum required load current not very high.
On the other hand, looking at picture 2.18 it's possible to see that the strategy to ensure the maximum load efficiency leads to a worst ZVS range and also the minimum load current required is higher with respect the previous case.

2.4.2 Reactive current consideration

A first step to do, in order to find an optimal trade off between the two opposite design strategies discussed above, is to compute how the amount of the reactive current, that flows in the circuit, varies changing the value of the voltage ratio (M) and of the phase shift (d).
Taking in mind the plot 2.3, the average reactive current in half period corresponds to the negative area under the waveform, i.e.:

$$I_{reac,o} = \frac{1}{2T_{hf}} t_2 I_2 = \frac{T_{hf}}{8L} \frac{[(2d-1)v_i + \frac{v_o}{n}]^2}{v_i + \frac{v_o}{n}} \tag{2.60}$$

Remembering the voltage ratio $M = \frac{v_o}{nv_i}$, the previous equation can also be written in the following way:

$$I_{reac,o} = \frac{T_{hf}}{8L} \frac{[(2d-1)+M]^2 v_i}{1+M} \tag{2.61}$$

Dividing the last equation by the total amount of the output average current (see eq. (2.12)), the percentage of the reactive current injected inside the output cell of the converter (hence the branch in which the battery is linked), remembering that $n = 1$, results:

$$\lambda_o = \frac{(2d-1+M)^2}{8(1-d)d(1+M)} \tag{2.62}$$

The average amount of the reactive current absorbed by the input bridge can be computed starting from figure 2.5:

$$I_{reac,i} = \frac{1}{2T_{hf}} t_1 I_1 = \frac{T_{hf}}{8L} \frac{[(2d-1)\frac{v_o}{n} + v_i]^2}{v_i + \frac{v_o}{n}} = \frac{T_{hf}}{8L} \frac{[(2d-1)M+1]^2 v_i}{1+M} \tag{2.63}$$

Following the same reasoning for the output current, dividing the reactive input current by the average input current (2.19), the percentage is equal to:

$$\lambda_i = \frac{[(2d-1)M+1]^2}{8d(1-d)M(1+M)} \tag{2.64}$$

The total reactive current amount in percentage is equal to:

$$\lambda_t = \lambda_i + \lambda_o = \frac{[(2d-1)M+1]^2}{8d(1-d)M(1+M)} + \frac{(2d-1+M)^2}{8(1-d)d(1+M)} \tag{2.65}$$

Through this equation it is possible to select a desirable value of reactive current and, from the circuit specification, get the optimal phase shift value required to find the value of the leakage inductance [12].

2.4.3 Current stress optimization

As observed in previous sections, when the voltage conversion ratio is not equal to one, the leakage inductance current during the time interval $(1-d)T_{hf}$ won't be flat, but it will present a peak value: this one can be expressed by the value I_1 if the converter is working in buck mode, otherwise I_2 if the converter is working in boost mode. Remembering equations (2.32), the maximum current stress is a function of the voltage ratio M, the leakage inductance L and the maximum phase shift value d.
The values of the maximum phase shift and leakage inductance are linked to the desired maximum output power [13]:

$$P_{max} = \frac{v_i v_o d_{max}(1 - d_{max})T_{hf}}{nL} \tag{2.66}$$

in which v_i and v_o can shift from their minimum to their maximum value. From equation (2.66) it is possible to extrapolate the expression of the leakage inductance:

$$L = \frac{v_i v_o d_{max}(1 - d_{max})T_{hf}}{nP_{max}} \tag{2.67}$$

Replacing the expression (2.67) into (2.32), the maximum current values are:

$$\begin{cases} Ics_{M_{min}} = \frac{nP_{max}(2M_{min}d_{max}+1-M_{min})}{2v_o d_{max}(1-d_{max})} \\ Ics_{M_{max}} = \frac{nP_{max}(2d_{max}-1+M_{max})}{2v_o d_{max}(1-d_{max})} \end{cases} \tag{2.68}$$

The steps followed (in both buck and boost mode) to define the searched value of the leakage inductance are:

- calculate the maximum and minimum values of the voltage conversion ratio;
- substitute them in the respective current stress equations;
- compute the derivatives of the aforementioned currents in order to extrapolate the optimal value of the phase shift that allows to get the minimum value of the current;
- substitute the optimal phase shift found in the expression (2.67).

Remembering the design requirements, the minimum value of the voltage conversion ratio is $M_{min} = 270/420 = 0.6428$. In figure 2.19 are plotted different waveforms that represent the trend of the current stress as a function of the two main variables (M and d). As it can be noted, the maximum current flows with minimum output voltage and its lowest value allows to define the optimal value of the phase shift. To verify analytically the result plotted, it's necessary to compute the partial derivative of Ics_{Mmin} with respect d_{max} and put it equal to zero:

$$\frac{\partial Ics_{Mmin}}{\partial d_{max}} = 0 \tag{2.69}$$

$$2M_{min}v_o(2d_{max} - 2d_{max}^2) - (2M_{min}d_{max} + 1 - M_{min})(2v_o - 4d_{max}v_o) = 0 \tag{2.70}$$

$$2d_{max}^2 M_{min} + 2d_{max}(1 - M_{min}) + M_{min} - 1 = 0 \tag{2.71}$$

Solving the above second order equation, the two values of the phase shift that allow to minimize the current stress are equal to:

$$d_{opt,M_{min},1,2} = \frac{-1 + M_{min} \pm \sqrt{1 - M_{min}^2}}{2M_{min}} \tag{2.72}$$

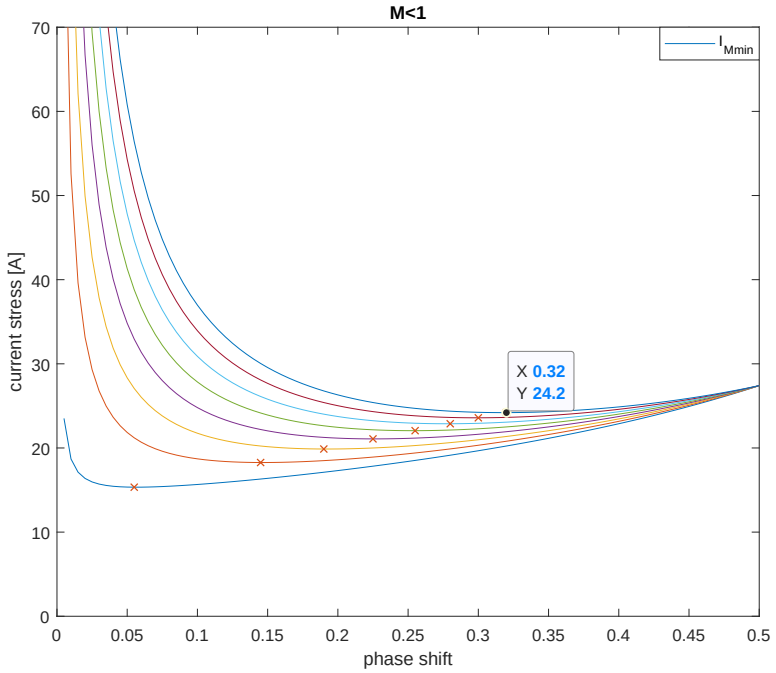


Figure 2.19: Current stress varying the value of M and d in buck mode.

By the last equation, to make possible that the converter operates in a stable region, the smallest value has to be taken into account. Substituting the value of the parameter, the quantity shown in figure 2.19 results, i.e. $d_{opt,M_{min}} = 0.318$.
On the other hand, the current stress in boost mode operation is plotted in figure 2.20, in which case the maximum

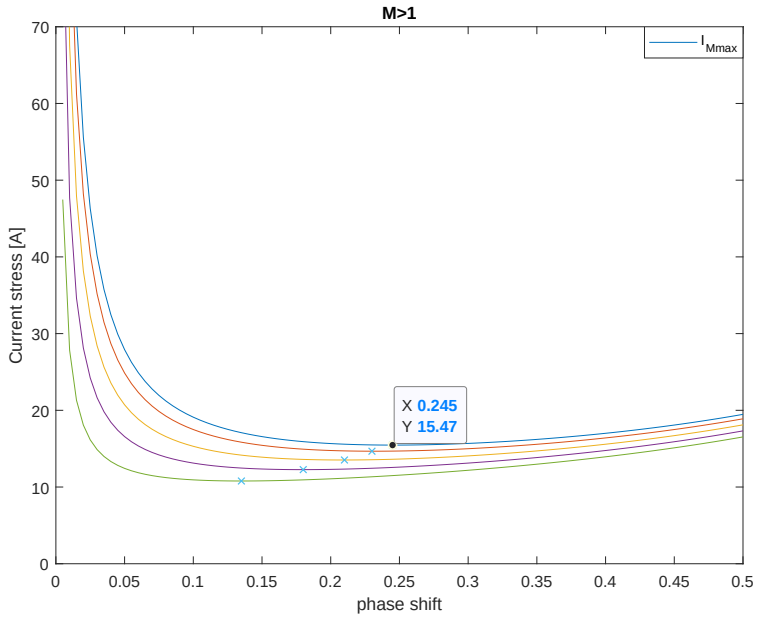


Figure 2.20: Current stress varying the value of M and d in boost mode.

value for the voltage conversion ratio is equal to $M_{max} = 470/380 = 1.2368$.
Once again, following the same reasoning for the buck case, deriving the equation of $Ics_{M_{max}}$ with respect d_{max} the

optimal value of the phase shift is found:

$$\frac{\partial Ics_{M_{max}}}{\partial d_{max}} = 0 \tag{2.73}$$

$$2(2v_o d_{max}(1-d_{max})) - (2d_{max} - 1 + M_{max})(2v_o - 4v_o d_{max}) = 0 \tag{2.74}$$

Leaping some intermediate mathematical steps, the two optimal values of the phase shift that permit to minimize the current stress are given by:

$$d_{opt,M_{max,1,2}} = \frac{1 - M_{max} \pm \sqrt{M_{max}^2 - 1}}{2} \tag{2.75}$$

Once again, in order to ensure a stable working condition, the minimum phase shift has to be chosen, resulting in the same value shown in figure (2.20), i.e. $d_{opt,M_{max}} = 0.2455$. Substituting the two value of the optimal phase shift into the expression of the leakage inductance (2.67), taking into account the design range for the input and the output voltages, these two distinguished results appear:

$$\begin{cases} L_{M_{min}} = \frac{v_{i,max} v_{o,min} d_{opt,M_{min}} (1-d_{opt,M_{min}}) T_{hf}}{n P_{max}} = 6.6468 * 10^{-6} & [\mu\text{H}] \\ L_{M_{max}} = \frac{v_{i,min} v_{o,max} d_{opt,M_{max}} (1-d_{opt,M_{max}}) T_{hf}}{n P_{max}} = 8.9413 * 10^{-6} & [\mu\text{H}] \end{cases} \tag{2.76}$$

After this analysis, it emerges that the biggest current stress happens in buck mode condition.
Since the converter will work for a reasonable long time in boost mode (during the final step of the charging process of the battery), a good design choice is to adopt a leakage inductance that has a value included between these two boundary results. In this mind, the value of leakage inductance chosen has been around $L = 7.3$ [μH].
Knowing the value of this component, it's possible to go back and computing the waveforms of the current and voltage during the resonant intervals (shown in fig. 2.21) and the boundaries for the soft switching operation in accordance to the energy computation (plotted in fig. 2.22).

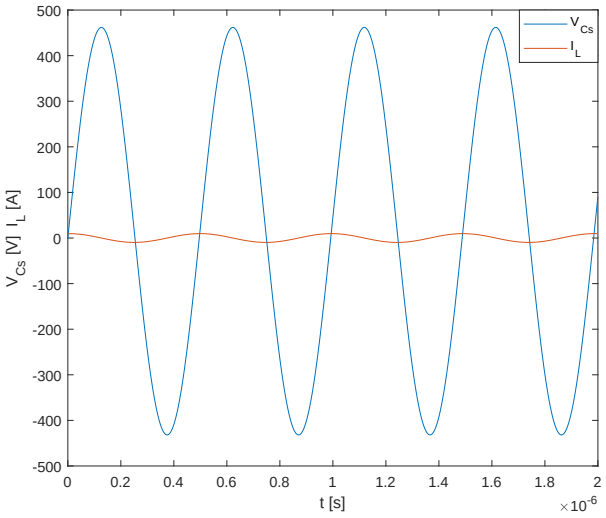


Figure 2.21: Voltage and current waveforms during the resonant intervals.

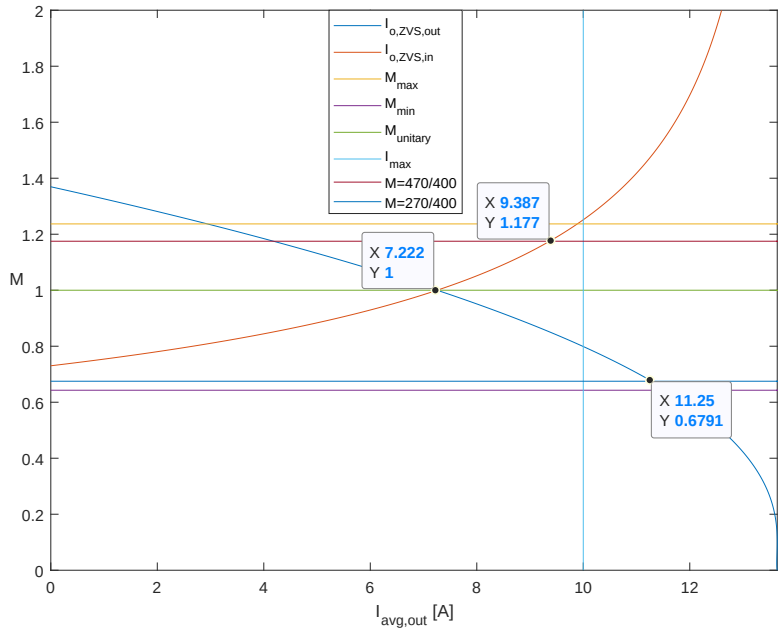


Figure 2.22: Minimum output current required to ensure ZVS with L=7.3 [μH].

2.5 Ripple of the output voltage

The current flowing from the output bridge towards the battery, since it has been rectified through switching devices, presents high frequency harmonics superimposed to the average output value: for this reason, a capacitance is used in parallel to the output port.

The current that flows inside the capacitance depends on the intervals during a switching period; considering the operating boost forward mode, the capacitance current is equal to:

$$\begin{cases} i_c = -(I_o + i_L), \text{ if } & 0 \leq t \leq dT_{hf} \\ i_C = i_L - I_o, \text{ if } & dT_{hf} \leq t \leq T_{hf} \end{cases} \tag{2.77}$$

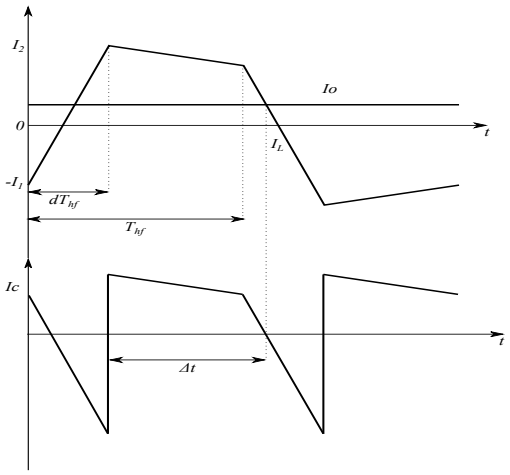


Figure 2.23: Inductance, output average and capacitance currents.

As can be seen in fig. 2.23, the current in the capacitance is null when the value of the inductance current equals that one of the average output one. In order to find the expression of Δt, i.e. the time interval needed to the inductance current to decrease from the upper value I_2 to the average output current I_o, the following equation has to be solved:

$$I_2 + \frac{nv_i - v_o}{Ln^2}\Delta t = I_o \tag{2.78}$$

$$\Delta t = \frac{I_2 - I_o}{v_o - nv_i} Ln^2 \tag{2.79}$$

Referring the current I_2 to the secondary side of the transformer, after some substitution steps, the expression of the searched interval of time is:

$$\Delta t = \frac{v_o - nv_i + 2nd^2 v_i}{4f_{sw}(v_o - nv_i)} \tag{2.80}$$

The voltage ripple downstream the output bridge can be finally computed, solving the following integral:

$$\Delta v_o = \frac{1}{C}\int_{dT_{hf}}^{dT_{hf}+\Delta t} (i_L(t) - I_o)dt = \frac{\Delta t}{C}\frac{I_2 - I_o}{2} \tag{2.81}$$

Making some substitutions, the expression for the output capacitance results:

$$C = \frac{[v_o + (2d^2 - 1)nv_i]^2}{32 f_{sw}^2 L \Delta v_o (v_o - nv_i)} \tag{2.82}$$

Considering the working condition with maximum voltage conversion ratio, i.e. $v_o = 470$ [V] and $v_i = 380$ [V], a phase shift ratio equal to 0.2753, the leakage inductance desired and a maximum ripple in the output voltage of 28 [mV], it results a smoothing capacitance of 147.42 [μF], approximated to a commercial value of 150 [μF].

2.6 Effect of the dead time

The switches that belong to the same leg can't be turned on at the same time, otherwise dangerous short circuit would occur. For this reason it's required an opportune dead time between the gate signals of both switches. What it happens during the dead time t_d relies on the sign of the inductance current. Through the simplified circuit in fig. 2.24 it's possible to observe the effects of the dead time on the alternating voltage V_p. In the aforementioned plot the switches are considered ideal, i.e. lacking the parasitic capacitances.

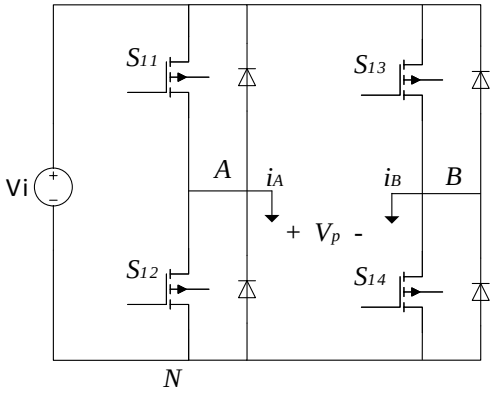


Figure 2.24: Ideal circuit of the input bridge to analyze the dead time effects on the primary voltage V_p.

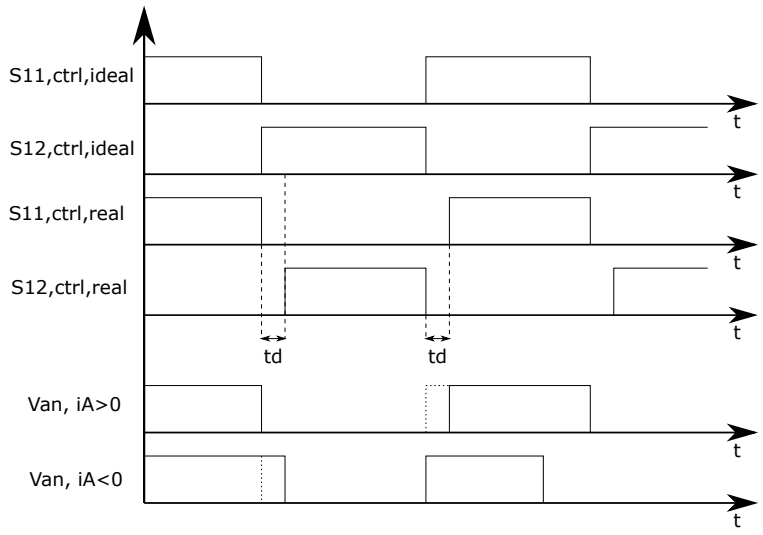


Figure 2.25: Control signal and output voltage for the first leg in ideal and real case.

As a first analysis, taking into account just the first leg A, to generate the gate signals for the two switches, a saw tooth waveform is compared with a constant reference, in order to get a 50% duty cycle. In this ideal case, the voltage V_{AN} is positive when S_{11} is turned on and it's null when S_{12} is on.
During the dead time the switches of the same leg are both turned off and hence the value of the voltage V_{AN} depends on the sign of the current i_A, since it determines which anti-parallel diode conducts. As plotted in fig. 2.25, if the current i_A is positive, turning off the S_{11} the diode in anti-parallel to S_{12} starts to conduct, and hence the voltage is the same like in the ideal case; contrariwise when S_{12} is turned off, during the dead time the voltage remains to zero, since it's anti-parallel diode starts to conduct: in this case the dead time causes a reduction in the average output voltage V_{AN}, as can be seen in the second-last waveform in the same plot.
On the other hand, if the current i_A is negative, when S_{11} is turned off, it's anti-parallel diode conducts during the dead time, so there's a gain of positive voltage during the dead time with respect the ideal case in which the dead time is not considered; instead when S_{12} is turned off, since the upper diode conducts, the voltage behaviour is the same of the ideal case. To summarize:

- if $i_A > 0$, then $V_{AN,real} = \frac{dT_{hf} - t_d}{T_{hf}} V_i$;
- otherwise if $i_A < 0$, then $V_{AN,real} = \frac{dT_{hf} + t_d}{T_{hf}} V_i$.

Considering the full input bridge, two different cases arise:

- if the currents $i_A > 0$ and $i_B < 0$, it appears a voltage drop for what concern V_{AN} and a gain for V_{BN}, as shown in the system:

$$\begin{cases} \Delta V_{AN} = \frac{t_d}{T_{hf}} V_i \\ \Delta V_{BN} = -\frac{t_d}{T_{hf}} V_i \end{cases} \tag{2.83}$$

- if $i_A < 0$ and $i_B > 0$, it appears a voltage drop for V_{BN} and a gain for V_{AN}, like stated below:

$$\begin{cases} \Delta V_{AN} = -\frac{t_d}{T_{hf}} V_i \\ \Delta V_{BN} = \frac{t_d}{T_{hf}} V_i \end{cases} \tag{2.84}$$

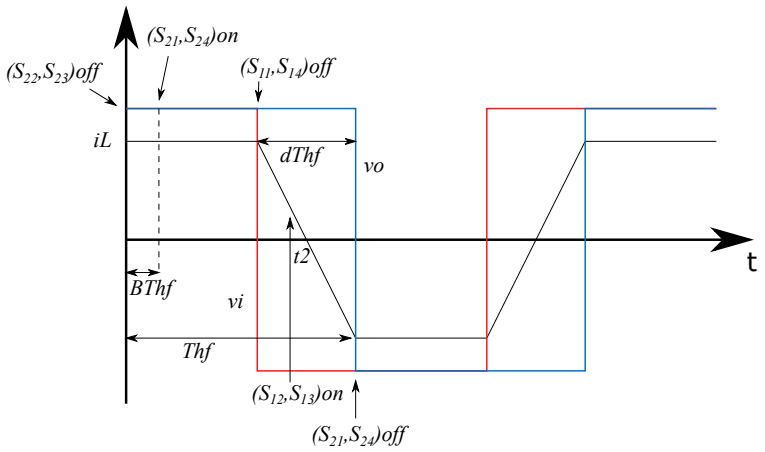


Figure 2.26: Operation waveforms when the dead time doesn't influence the converter behaviour.

Making the difference between $V_{AN} + \Delta V_{AN}$ and $V_{BN} + \Delta V_{BN}$, the input bridge voltage is obtained and it differs from the ideal case for a quantity equal to: $\Delta V_p = \pm 2 \frac{t_d}{T_{hf}} V_i$. The fact that the voltage output bridge is greater or smaller than its ideal value relies just on the sign of the inductance current: this difference, thinking on the fundamental component of the voltage in the ideal and real case, makes bigger the phase between the voltage and the inductive current.

In addition to the aforementioned problems, the dead time can create also other two phenomena: the inversion in the voltage polarity and a phase drift in the characteristic of the output power [14]. The inversion in the voltage polarity can appear in all the three buck, boost and matching state modes; the reason for this event is that the dead time is longer with respect the time required to the current to shift its sign. To explain this phenomenon, the matching state is considered hereinafter, but a similar reasoning can be applied also to the buck and boost mode, although there would be six different states for each of these two modes. In the following, the dead time is expressed indirectly through its relative ratio with respect the half switching period, resulting in $B = \frac{t_d}{T_{hf}}$.

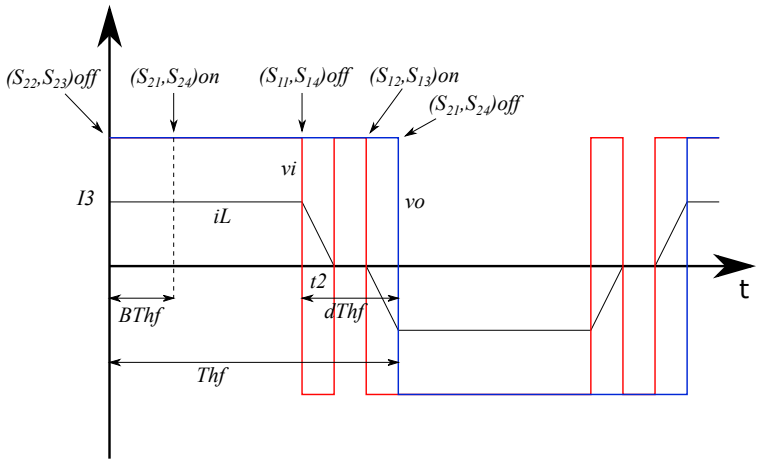


Figure 2.27: Operation waveforms in presence of reverse voltage polarization.

Once again, considering ideal switches (neglecting the output parasitic capacitances), two different stages are found in the matching state mode:

- if the initial inductance current is equal or greater than zero and $t_2 - (1-d)T_{hf} \geq BT_{hf}$, the waveforms plotted

in fig. 2.26 appear;

- if the initial inductance current is still like the previous case, but $t_2-(1-d)T_{hf} < BT_{hf}$, the waveforms shown in fig. 2.27 result.

In the first case, since the dead time is not too much big, the complementary switches S_{12} and S_{13} in the input bridge are turned on before that the inductance current changes sign, in this way the input bridge output voltage hasn't oscillations and the real converter behaviour matches the ideal one (without dead time). Looking at picture 2.26, the expression of the time instant t_2 can be computed as:

$$t_2 = T_{hf} - \frac{dT_{hf}}{2} = T_{hf}\frac{2-d}{2} \tag{2.85}$$

Knowing that the dimensionless phase shift d has to be smaller than 1, the following boundaries for this working condition appear:

$$2M \leq d \leq 1 \tag{2.86}$$

In this case, since the voltage ratio between input and output bridge is unitary, the expression of the average transmitted power remains (2.17), recalled below:

$$P_o = v_o\frac{(1-d)dT_{hf}v_i}{nL} \tag{2.87}$$

In the second case, since the dead time is bigger than the maximum time interval $t_2-(1-d)T_{hf}$, after switching off the switches S_{11} and S_{14}, remembering the ideal switches configuration, since the current in the inductance is still positive, the anti-parallel diodes of S_{12} and S_{13} start to conduct; when the current becomes zero, also the diodes stop to conduct: the voltage across the leakage inductance is clamped to zero and there is no current flowing until the switches S_{12} and S_{13} are turned on.
Looking at the waveforms in fig. 2.27, the expression of the time instant t_2 is derived as:

$$t_2 = T_{hf}(1-B) \tag{2.88}$$

Substituting it inside the inequality that defines the boundaries for d value, the following expression results:

$$B \leq d < 2B \tag{2.89}$$

In this case, the average output current is different with respect the ideal case and it figures as:

$$I_{o,avg} = \frac{1}{T_{hf}}[I_3(1-d)T_{hf}] \text{ where } I_3 = \frac{v_i+v_o}{L}T_{hf}(d-B) \tag{2.90}$$

Substituting the expression of I_3 into $I_{o,avg}$, remembering that in the studied case $v_i = v_o$ and multiplying the resulting current for the input voltage, the following equation for the output power is obtained:

$$P_o = \frac{T_{hf}2v_i^2}{L}(d-B)(1-d) \tag{2.91}$$

The analytical computation is verified in the simulation made in Simplorer Ansys. Figure 2.28 shows the polarization effect of the voltage considering negligible the parasitic capacitances; instead in figure 2.29 their presence is taken into account: as it can be seen, if the dead time is too long, when the switch S_{11} is turned off (S1.CTRL goes down),

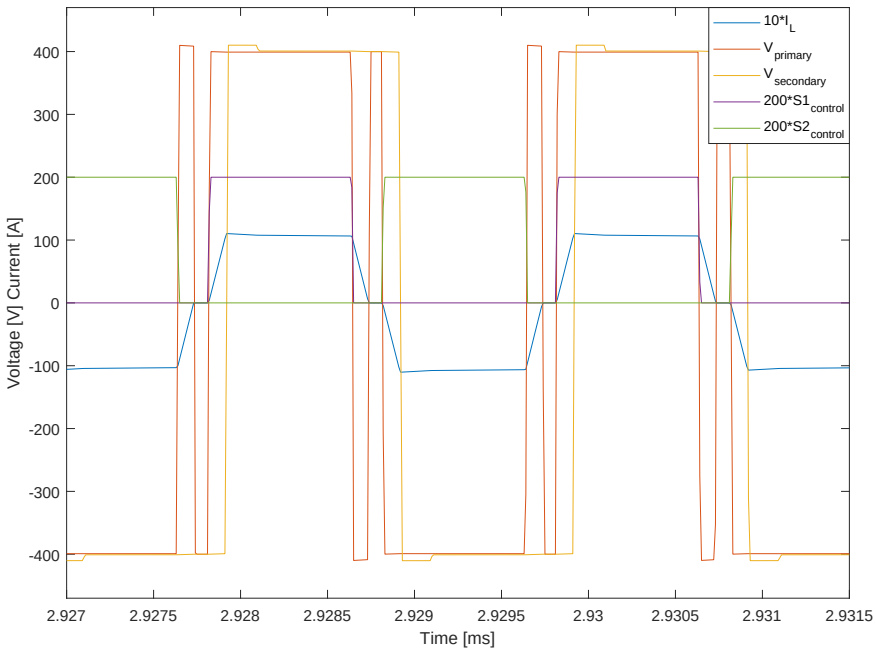


Figure 2.28: Simulation result of the voltage reverse polarization effect without parasitic output capacitances.

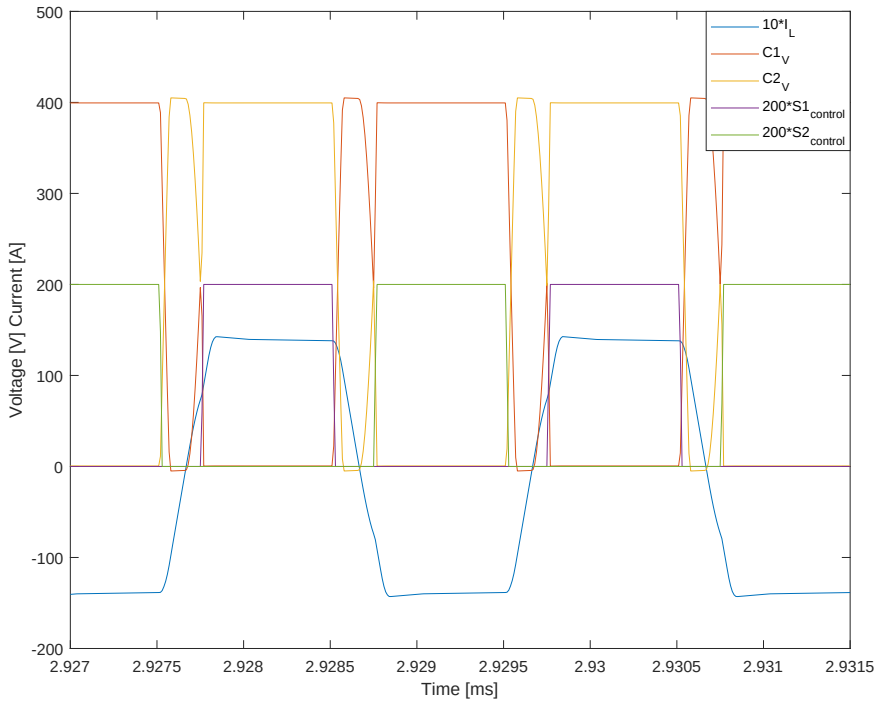


Figure 2.29: Simulation of the voltage reverse polarization with parasitic output capacitances.

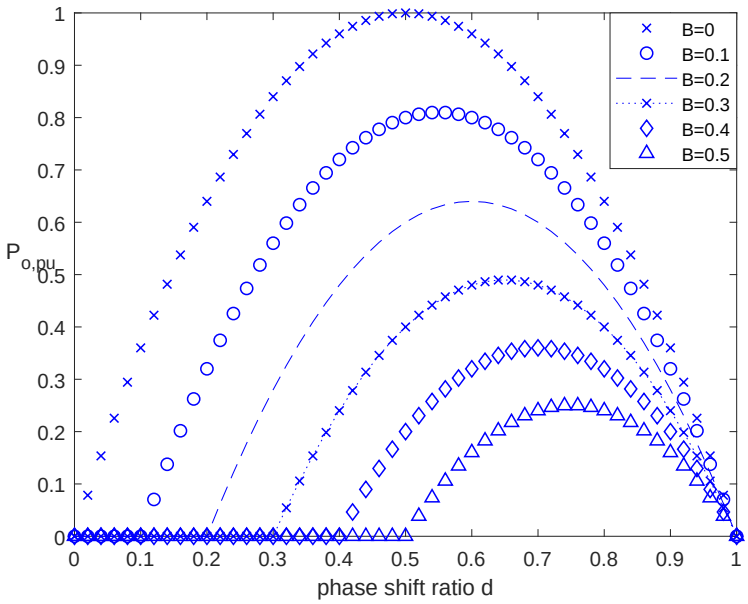


Figure 2.30: Per unit transmitted power in matching state taking into account the dead time.

its anti-parallel capacitance starts to charge (brown line), but if the control signal of S_{12} arrives too late, the inductance current changes its sign and in this way the capacitances of S_{11} and S_{14} discharge again and on the other side the capacitances of S_{12} and S_{13} charge themselves again; this condition causes not only deep sags in the voltage applied to the transformer, but especially hard switching turning on. As stated before, furthermore voltage reverse polarization, another important phenomenon that could occur in presence of big dead time values is the so called "phase drift". As can be seen in 2.30, the output transmitted power in per unit, i.e $P_{o,pu} = 4(d - B)(1 - d)$, decreases while the relative dead time value B increases; the power peak value decreases and until the phase shift is smaller than the dead time, the power flows in the opposite direction (in the aforementioned plot it has been set to zero since it's referred to the transmitted power towards the battery stack). This phenomenon decreases the power density of the converter and increases the back flow power, arising the whole losses during the charging process.

3 Charging process, circuit simulation and total power lost trend

As stated in the first and second chapters, one of the main application field of the dual active bridge is the automotive sector. In this contest, the charger has to link the grid with the battery stack, in particular the DAB connects the rectified DC voltage with that one at the battery terminals. To make a simulation of the charger that will reflect the real behaviour, it appears necessary to characterize the load.
In this chapter an hypothetical battery stack is designed in order to get the resistance value to link at the output port of the secondary full bridge and also to simulate the charging process; after that the circuit is simulated in Simplorer in order to check the waveforms and the values of voltage and current in the several devices and finally a model that allows to predict the total losses during the whole charging process has been developed.

3.1 Battery stack and charging model

The first step has been to choose the type of battery: lithium iron phosphate battery HW-40152S 15 [Ah] by Headway has been selected since it's the kind of battery that is applied in the IMAB racing car. The main specifications of the single cell are summarized in table 3.1. Since the nominal voltage of the battery stack has to be equal to 370 [V], the number of cells to be connected in series corresponds to: $\frac{370}{3.2} = 116$; however with just 116 cells, remembering that the maximum voltage for each cell is equal to 3.7 [V], the maximum stack voltage would be of 429 [V], not enough for the goal of 470 [V] at full charge condition. For this reason the number of series cells has been increased to 128.
Looking at table 3.1 the capacity of the whole stack results of 15 [Ah]. The energy stored in a single battery, expressed in [Wh], is equal to the electric charge Q [mAh] times the voltage and divided by 1000: $E_{nergy} = \frac{15000 \cdot 3.2}{1000} = 48$ [Wh]; the total energy stored in the whole stack is equal to 128 times that one of a single cell, i.e. 6.144 [kWh]. The equivalent resistance of the stack is equal to 0.512 [Ω]: this value will be used in the circuit simulation to validate the current and voltage waveforms. To close the loop about the battery stack, since each cell weighs 0.48 [kg], the weight of the stack, taking into account also the chassis, could be around 85 [kg].
In order to simulate the charging process, a model using only the information about the state of charge of the battery (the so called "SOC") has been utilized: it's a modified approach of the original Shepherd model, since in the previous one the non linear battery voltage depends on both the current amplitude and the instantaneous charge of the battery, but since this model presents instability in simulation software, the amplitude current dependence has been neglected. As itemized in [15], this simplified model presents some assumptions:

Table 3.1: Specification of the lithium iron battery.

Parameter	Value	Unit
Nominal voltage	3.2	V
Nominal capacity (0.5 C, 25 [°C])	15000	mAh
Charge voltage	$\pm$ 3.7	V
Internal resistance	4	$m\Omega$

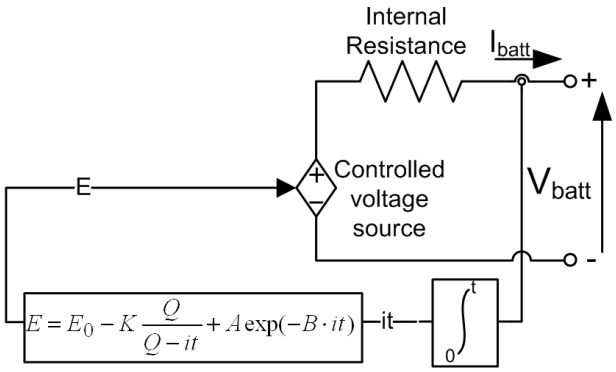


Figure 3.1: Simplified battery model.

- the internal resistance is independent on the state of charge of the battery, so it's supposed to stay constant both during charging and discharging process;
- the parameters of the model are deduced directly form the manufacturer's data sheet;
- the temperature doesn't affect the battery parameters, the self discharge and the memory effect are neglected.

It appears that when the state of charge of the battery is null, the voltage is null and no upper limit exists. The battery non linear model is represented by means of a constant resistance in series with a controlled voltage source, as it can be seen in fig. 3.1. The controlled voltage source is "driven" through the following non linear equation:

$$E = E_0 - K\frac{Q}{Q - it} + Ae^{-Bit} \tag{3.1}$$

in which:

- E is the no-load voltage;
- E_0 is the battery constant voltage;
- K is the polarization voltage;
- Q is the battery capacity;
- the integral term idt represents the actual state of charge;
- A is the voltage at the end of the first knee exponential zone;
- B is defined as the exponential zone inverse time constant, expressed in $[\text{Ah}]^{-1}$.

The stack capacity can be expressed in coulombs simply multiplying the ampere-hour value by 3600, getting a result of $C_{aps} = 54000$ [C]. Other values useful for the simulation are:

- $E_{full} = 470$ [V] is the maximum voltage of the battery stack;
- $E_{exp} = 128{\cdot}3.3 = 422.4$ [V] is the voltage at the end of the first exponential zone along the discharging path (the 3.3 [V] has been got looking at the plot in the manufacturer data-sheet regarding a single cell);
- $E_{nom} = 128{\cdot}3 = 384$ [V] is the nominal voltage at the end of the voltage plateau;
- $B = \frac{3}{0.75{\cdot}3600} = 0.0011$ $[\text{As}]^{-1}$, in which 0.75 [A] is the discharging optimal current for the considered cell;

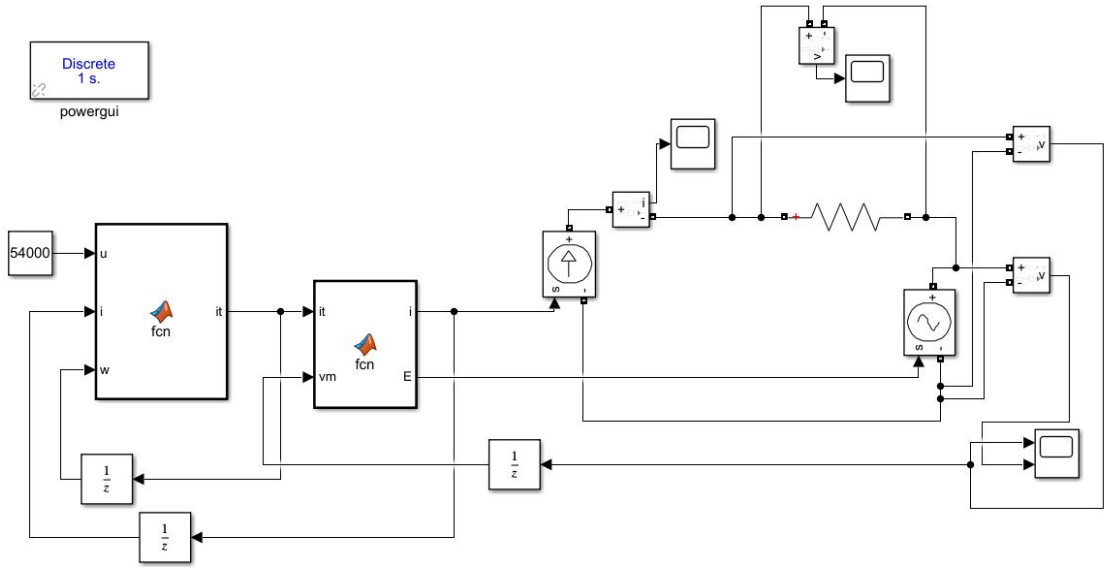


Figure 3.2: Simulink model of the battery.

- $Q_{nom} = 13.57 \cdot 3600 = 48852$ [C] is the nominal battery stack capacity.

Employing the aforementioned values, the exponential zone amplitude A and the polarization voltage K can be computed as:

$$A = E_{full} - E_{exp} = 47.60 \ [V] \tag{3.2}$$

$$K = \frac{(E_{full} - E_{nom} + Ae^{-BQ_{nom}} - 1)(C_{aps} - Q_{nom})}{Q_{nom}} = 4.0466 \ [V] \tag{3.3}$$

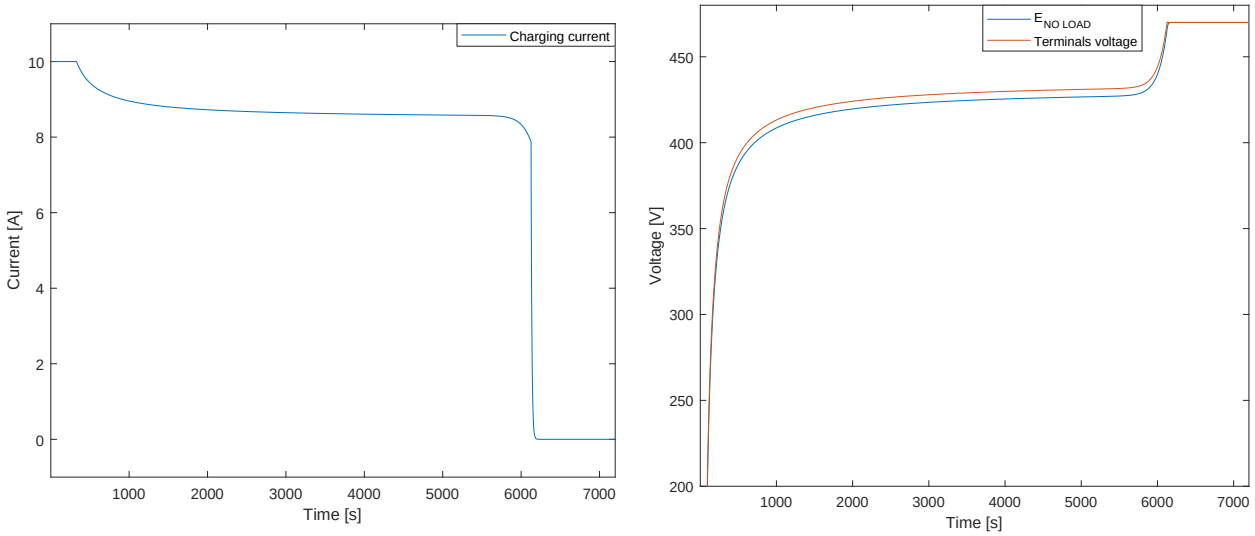
The battery constant voltage E_0 is hence computed:

$$E_0 = E_{full} + K + RI - A = 431.5666 \ [V] \tag{3.4}$$

in which the current value I is equal to 10 [A]. As it's presented in picture 3.2, to simulate the charging path of the battery both current and voltage controlled sources are necessary; the simulation is done over an interval time of 2 hours with discrete time steps of 1 second. The value of the equivalent resistance is that one computed above. In the described model, the first function block implements some useful logical steps:

```
function it = fcn(u,i,w)
if w==0
    it=u-i;
else
     it=u-(u-w)-i;
end
```

The first if question is needed to initialize the model, since at the beginning the feedback value w is null and hence the capacity it is put equal to the total battery stack capacity, in this way in the iteration steps this value is decreased until it reaches zero, when the battery is full charged (the current value i is multiplied by no time value since the integration step is related to the discrete solution step of 1 second).
The second function block computes at each cycle the value of current and voltage to apply to the two controlled



(a) (b)

Figure 3.3: Current and voltage battery waveforms.

sources:

```
function [i,E] = fcn(it,vm)
Eo=431.5666;
K=4.0466;
A=47.6;
R=0.512;
B=0.0011;
Caps=54000;
E=Eo-K*Caps/(Caps-it)+A*exp(-B*it);
if vm<=370
    i=10;
elseif vm>370 && vm<470
    i=3700/vm;
else vm=470
    i=(vm-E)/R;
end
```

It has to be observed that in the voltage range 370-470 [V] the charging process is at constant power: for this reason the current to apply is computed as the ratio among the maximum output power ($P_{max} = 3.7$ [kW]) and the voltage at the battery terminals vm. In picture 3.3(a) the current waveform during the charging process is plotted, instead in fig. 3.3(b) the internal and at terminals voltages are shown. The charging simulation has been implemented separately from the circuit model cause of the different time ranges (milliseconds in the case of the circuit and hours in the case of the battery); furthermore the battery block already implemented in Simulink hasn't been employed because it creates instability at the end of the charging process.

3.2 Circuit simulation

The circuit is simulated in Simplorer Ansys.

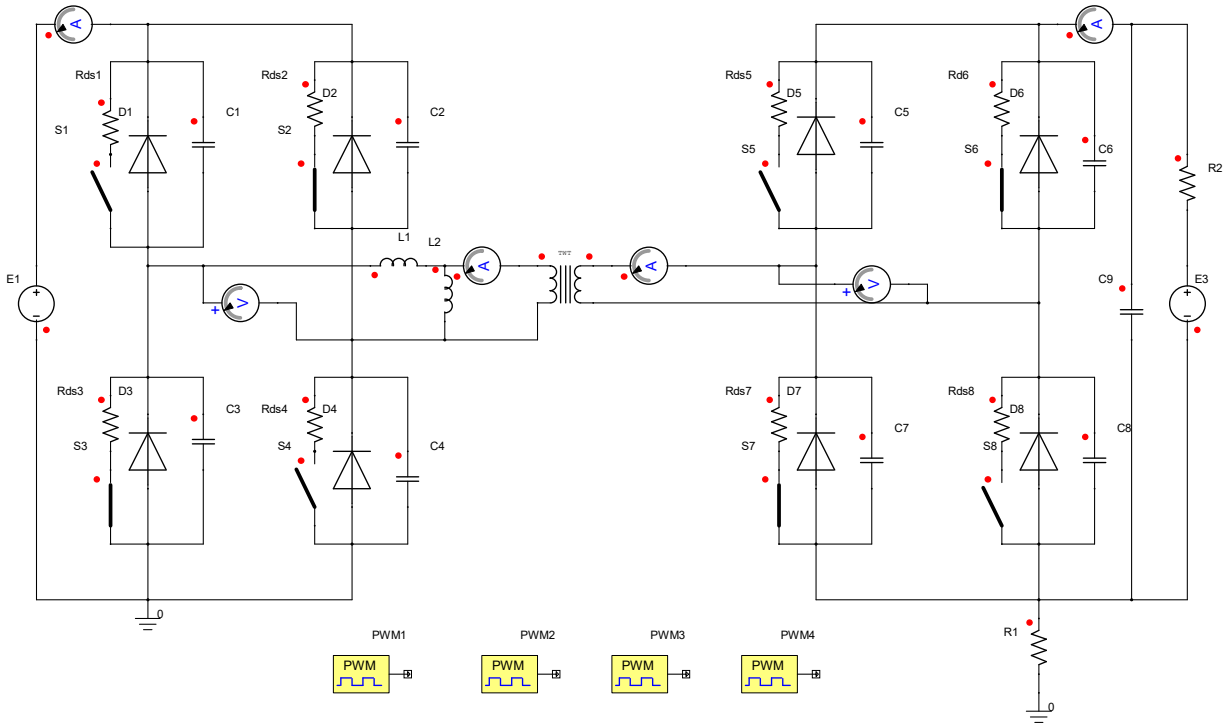


Figure 3.4: Schematic circuit of the DAB converter.

As shown in figure 3.4 each GaN device has been model through a resistance in series with the ideal switch, furthermore an anti-parallel diode and the parallel parasitic capacitance have been modelled. The transformer is considered ideal and two external inductances represent the series leakage one and the magnetizing one in derivative position. Downstream the output full bridge, the smoothing capacitance is put in parallel to the branch that represents the battery, i.e. the DC voltage source and the small resistance.

The main parameters of the schematic are summarized in table 3.2.

For what concern the four PWM blocks, the gate signal is sent to cross pair switches with the following restrictions:

Table 3.2: Circuit simulation parameters.

Parameter	Value	Unit
Input bridge voltage	400	$[V]$
Device internal resistance	40	$[m\Omega]$
Threshold diode voltage	4.3	$[V]$
Parasitic capacitance	850	$[pF]$
Leakage inductance	7.2	$[\mu H]$
Magnetizing inductance	292	$[\mu H]$
Transformer turn ratio	1	
Output bridge voltage	270-470	$[V]$
Smoothing capacitance	150	$[pF]$

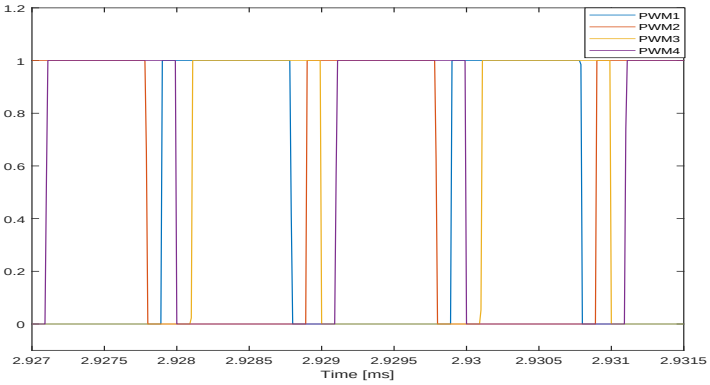
- dead time of 100 [ns] in order to prevent short circuit inside each leg;

- duty cycle D ideally equal to 50%, but taking into account the dead time it becomes smaller ($D' = D - t_{dead} \cdot f_{sw}$);
- the phase shift between the cross pairs inside each bridge is equal to 180°, instead the phase shift between the primary and the secondary bridge at the moment is decided manually (the design of the current control loop is described in a separate chapter).

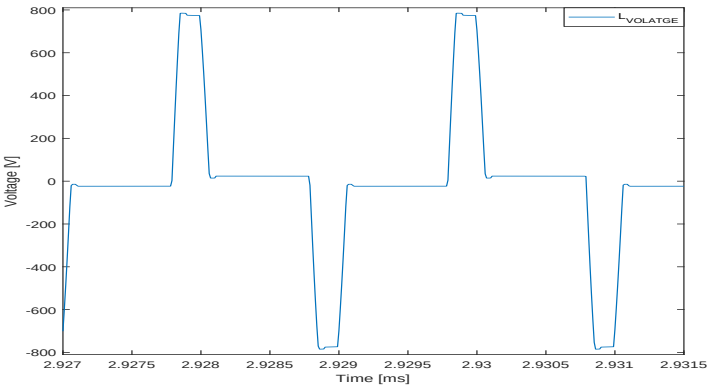
Pictures 3.5 show the resulting simulation waveforms. Just to itemize the representations, in fig. 3.5(a) the PWM signals are shown: it's clear that there are no superposition between gate signals inside each bridge; fig. 3.5(b) reports the voltage across the leakage inductance of the transformer, resulting as the difference between the two alternate square wave voltages applied across the transformer; picture 3.5(c) demonstrated that in nominal working condition there aren't hard commutations in the input bridge, since the voltage across the parasitic capacitances C_1 and C_2 reaches zero before that the gate signal of the respective parallel switch is sent; in particular, with a deep view, it's possible to see some sags in the capacitances' voltages: they are due to the anti-parallel diodes that have a threshold voltage of 4.3 [V] (remembering that the GaN devices, in order to be normally off, need a negative applied voltage, in fact this is the reason for what the diode conduction has to be established as short as possible, since the threshold voltage in the reverse conduction mode is quite high with respect that one of common diodes) and finally figure 3.5(d) presents the same soft switching confirmation in the output bridge. This working condition is the buck forward mode; similar waveforms can be obtained also in the case of boost mode.
Making three simulations considering different voltage ratios between input and output bridges, the current values and switching conditions summarized in table 3.3 appear. Without reporting all the simulation plots that would make "heavy" the end of this paragraph, just the waveforms in hard switching condition in the output bridge are shown in fig. 3.6: as it can be seen, the voltage across the capacitances goes completely down only when the switch control signal goes up; to take away every doubts a simulation with longer dead time has been done and the result doesn't change.

Table 3.3: Circuit simulation results.

Operating mode	Parameter	Value	Switching input	Switching output
Buck mode, 10 [A]	Inductance current peak value	17.65 [A]	Soft	Hard
Matching mode, 9 [A]	Inductance current peak value	12.24 [A]	Soft	Soft
Boost mode, 3 [A]	Inductance current peak value	7.78 [A]	Very hard	A bit hard



(a)



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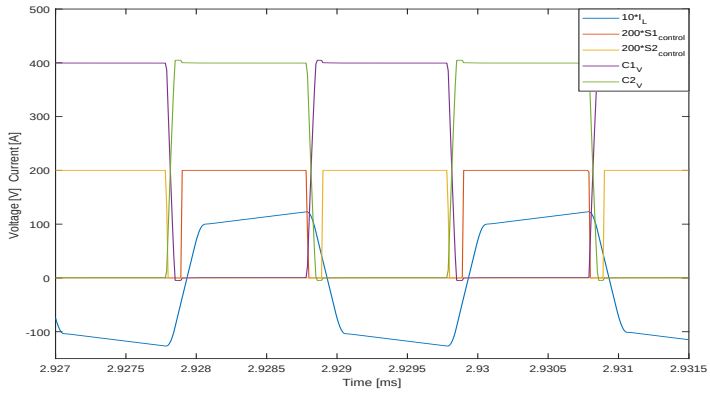
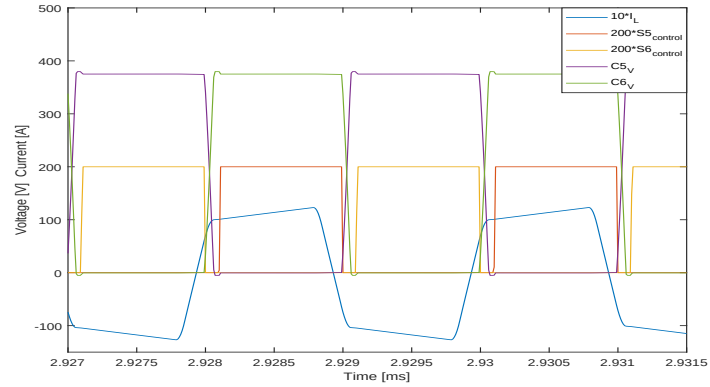


(c)



(d)

Figure 3.5: Main simulation results.

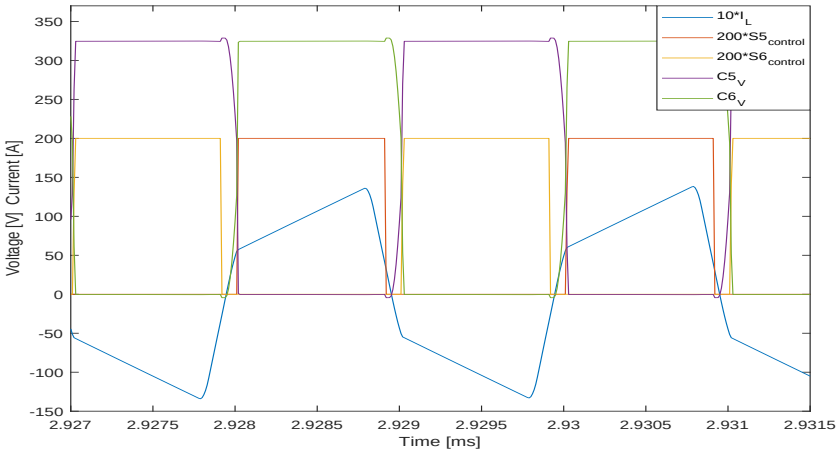


Figure 3.6: Hard switching in the output bridge.

3.3 Total power losses during the charging process

In this paragraph a computation of the total dissipated power made through Matlab is presented. The computation starts from the simulation of the charging path: the charging current is taken into account as the reference output current that should be obtained through the opportune phase shift value between the two bridges, maintaining constant the input bridge voltage (that one got by means the power factor corrector) and taking into account the variation of the battery voltage, so the operation mode will shift from buck to boost; obviously all the aspects regarding zero voltage switching area (ZVS) are considered, in order to identify when and which commutations are hard or soft.
In the ideal case, where no dead time is considered, the duty cycle of the gate signals is 50% and the output bridge current waveform is that one drawn in the DAB chapter, with continuous conduction, so the expression of the average output current is equal to the ideal one presented in the aforementioned chapter, reported below:

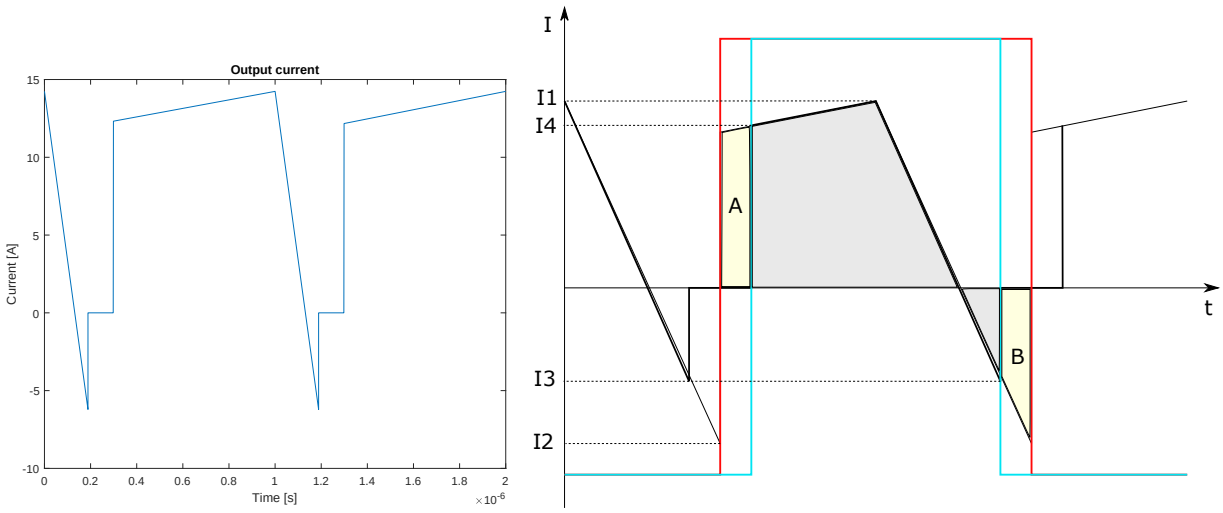
$$I_{o,avg} = \frac{(1-d)dT_{hf}v_i}{nL} \tag{3.5}$$

From the above equation, knowing by means the charging simulation the desired value of the feeding current, it's possible to compute the value of the needed phase shift, as:

$$d = \frac{(T_{hf}v_i - \sqrt{(T_{hf}v_i)^2 - 4T_{hf}v_i I_{o,avg}L})}{2T_{hf}v_i} \tag{3.6}$$

where the turn ratio n has been considered unitary. However the dead time can't be neglected and it makes the output DAB current looks like shown in figure 3.7(a). The time intervals in which the output current is equal to zero corresponds to the instants in which there are commutations in the output bridge and the circuit is not feeding the battery, since the inductance current splits itself between the two legs of the full bridge. It's evident that the above expressions of the average output current and of the required duty cycle are not more valid. For the sake of clarity, the real output current has been replotted in fig. 3.7(b), where the ideal PWM signal (red waveform) and the real PWM signal (blue waveform) are painted; furthermore the areas lost A and gained B with respect the ideal case (highlighted in yellow) are shown. The dead time acts in the same way in both rising and falling edges ($\frac{t_{dead}}{2}$ respectively) of the PWM signal. The real average output current becomes:

$$I_{o,avg,real} = I_{o,avg} - A + B \tag{3.7}$$



(a) (b)

Figure 3.7: Real average output current.

To find the new expression of the average output current, the two areas A and B have to be computed. I_3 and I_4 are expressed in function of the dead time, applying the definition of straight line waveform:

$$I_3 = \frac{2dT_{hf} - t_{dead}}{2dT_{hf}}(-I_2 - I_1) + I_1 \tag{3.8}$$

$$I_4 = \frac{\frac{t_{dead}}{2}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \tag{3.9}$$

Developing (3.7) the equation of the searched parameter corresponds to:

$$I_{o,avg,real} = \frac{(1-d)dT_{hf}v_i}{nL} - \Big[\frac{t_{dead}}{2T_{hf}}I_2 - \frac{t_{dead}}{4T_{hf}}(I_4 - I_2)\Big] + \Big[\frac{t_{dead}}{2T_{hf}}I_3 + \frac{t_{dead}}{4T_{hf}}(I_2 - I_3)\Big] \tag{3.10}$$

in which the second term represents the surface A and the third one the surface B. Knowing that:

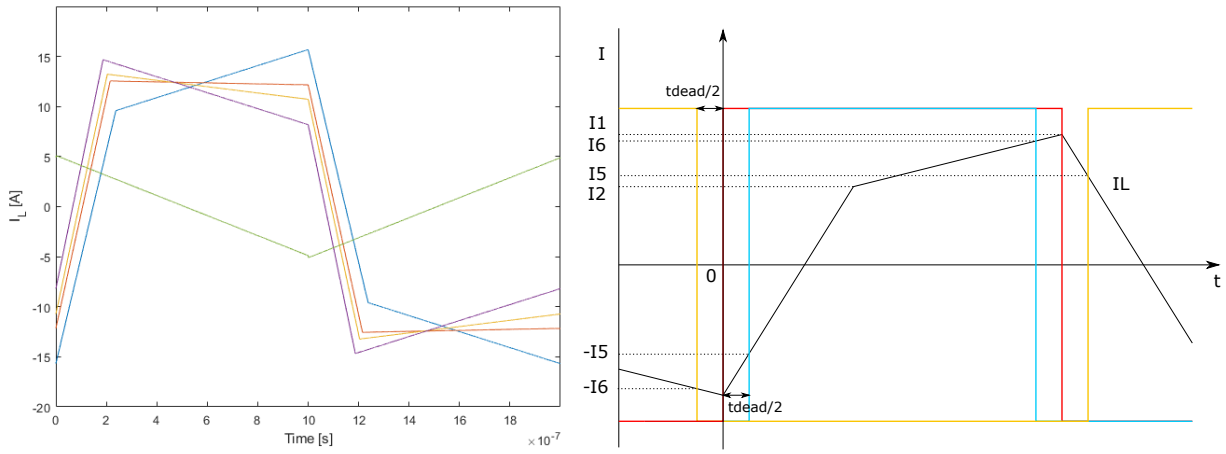
$$-I_1 - I_2 = (\frac{-v_i - v_o}{L})dT_{hf} \tag{3.11}$$

$$I_1 - I_2 = \frac{v_i - v_o}{L}(1-d)T_{hf} \tag{3.12}$$

The expressions of the two areas become:

$$A = \frac{1}{8T_{hf}L}\big[-4t_{dead}dT_{hf}v_i + 2t_{dead}T_{hf}v_i - 2t_{dead}T_{hf}v_o - t_{dead}^2(v_i - v_o)\big] \tag{3.13}$$

$$B = \frac{t_{dead}^2(v_i + v_o)}{8T_{hf}L} \tag{3.14}$$



(a) (b)

Figure 3.8: Inductance current waveforms.

Substituting the two above equations in the general expression of the real output current, it is possible to compute the expression of the desired phase shift, written below leaping some mathematical steps:

$$d_{1,2} = \frac{-2v_i T_{hf} t_{dead} + 4v_i T_{hf}^2}{8v_i T_{hf}^2} \pm \\ \pm \frac{\sqrt{(2v_i T_{hf} t_{dead} - 4v_i T_{hf}^2)^2 - 4(4v_i T_{hf}^2)(-v_i t_{dead} T_{hf} + v_o t_{dead} T_{hf} - t_{dead}^2 v_o + 4T_{hf} L I_{o,avg})}}{8v_i T_{hf}^2} \tag{3.15}$$

In fig. 3.8(a) the current waveforms during the charging process are plotted; it's possible to see that at the beginning the charger works in buck mode, then in boost mode and when the battery is full charged the current waveform becomes triangular with a small peak value.
Starting from the charging current values plotted in 3.3(a), by means of (3.15), taking the smallest value (negative sign before the root), the several phase shifts required during the charging process are got. In figure 3.8(b) the inductance current in buck mode is reported, in order to outline the current values during the switching instant times in the input bridge in the case in which the duty cycle isn't 50%.
The algorithm starts with the computation of the current values when the switches in the input bridge start to conduct (I_5) and when they are opened (I_6):

$$I_5 = \frac{t_{dead}}{2dT_{hf}}(I_2 + I_1) - I_1 \tag{3.16}$$

$$I_6 = \frac{T_{hf} - \frac{t_{dead}}{2} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \tag{3.17}$$

Just for the sake of clarity the different current values at the switching times can assume both positive and negative signs. The voltage step across the parasitic output capacitances is considered equal to the input or output bridge voltages plus the threshold voltage of the anti-parallel diodes. In this analysis the half currents $I_{3,hf}$ and $I_{6,hf}$ are important to compute the required time to charge and in particular discharge the capacitances in parallel to switches

that have to be closed, as clarified in the two following equations:

$$t_{d,in} = \frac{C(v_i + v_{th,d})}{I_{6,hf}} \tag{3.18}$$

$$t_{d,ou} = \frac{C(v_o + v_{th,d})}{I_{3,hf}} \tag{3.19}$$

in which v_i is supposed constant during all the charging time, instead v_o states the terminals battery voltage and changes dynamically during the charging path. Once computed these time intervals, it's possible to separate the instants in which the diodes in the input and output bridge conduct, computing the difference between the dead time and the required time to discharge the capacitances (d_{input} and d_{output}): if the difference is positive, it means that there's soft switching "ignition" and hence diodes conduct.
Afterwards the "body" diodes losses in the input bridge have been computed. Taking in mind the zero time reference shown in picture 3.8(b), considering only positive value for d_{input}, the time instants in which the input bridge diodes start and end to conduct are computing as:

$$t_{start,in} = t_{d,in} - \frac{t_{dead}}{2} \tag{3.20}$$

$$t_{end,in} = t_{start,in} + d_{input} \tag{3.21}$$

Through the above results, the current values at those instants are computed as:

$$I_{start,d} = \frac{t_{start,in}}{dT_{hf}}(I_1 + I_2) - I_1 \tag{3.22}$$

$$\begin{cases} I_{end,d} = \frac{t_{end,in}}{dT_{hf}}(I_1 + I_2) - I_1 \quad \text{if} \quad 0 < t_{end,in} \leq dT_{hf} \\ I_{end,d} = \frac{t_{end,in} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \quad \text{if} \quad dT_{hf} < t_{end,in} \end{cases} \tag{3.23}$$

Once got these boundary values, some discrete samples have been computed inside their range and after that, the rms quantities have been found, remembering that for discrete samples the computation becomes:

$$x_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} \tag{3.24}$$

Knowing the rms current value, the instantaneous power lost in each diode corresponds to:

$$P_{diode,in} = v_{th,d} I_{rms,diode} + R_d I_{rms,diode}^2 \tag{3.25}$$

where R_d represents the resistance during the "body" diode conduction, computed from the manufacturer's data sheet as the angular coefficient of the plotted waveform and equal to 74 [mΩ]. Finally the average value of "diode" conduction power lost in half switching period is:

$$P_{diode,in,avg} = 2P_{diode,in}\frac{d_{input}}{T_{hf}} \tag{3.26}$$

in which just 2 diodes are considered since the computation is made in half switching period.
The same reasoning has been followed to compute the conduction losses in the output bridge "body" diodes: first it

has been found the vector of starting and ending time instants of conduction, described as:

$$t_{start,out} = d_{output} + dT_{hf} - \frac{t_{dead}}{2} \tag{3.27}$$

$$t_{end,out} = t_{start,out} + d_{output} \tag{3.28}$$

In a second instance the current conduction boundaries have been computed:

$$I_{start,out} = \frac{t_{start,out} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \tag{3.29}$$

$$I_{end,out} = \frac{t_{end,out} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \tag{3.30}$$

Once again the medium power lost is computed and then the total diodes losses are defined as the sum of the two contributes related to input and output bridges.
Subsequently, the losses linked to hard switching are computed before in the input bridge and after in the output one. The times when hard switching occurs in the input bridge are got looking at the negative value of the vector d_{input} and the instant time in which hard switching turning on appears ($t_{in,h}$) is equal to $\frac{t_{dead}}{2}$ (remembering the waveform plotted in 3.8(b)). Afterwards the current magnitude in those time instants is computed:

$$\begin{cases} I_{hard,in} = \frac{t_{in,h}}{dT_{hf}}(I_1 + I_2) - I_1 & \text{if} \quad t_{in,h} \leq dT_{hf} \\ I_{hard,in} = \frac{t_{in,h-dT_{hf}}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 & \text{if} \quad t_{in,h} \geq dT_{hf} \end{cases} \tag{3.31}$$

As stated before, the maximum voltage step across the parasitic capacitances is equal to the bridge voltage plus the threshold diode voltage; however, to compute the exact power lost during hard switching, the punctual value has to be considered, remembering that I_6 is the current in the opening switches instant, the instantaneous voltage across the capacitances is:

$$v_{cs,in} = (v_i + v_{th,d}) - \frac{1}{C}\frac{I_6}{2}t_{dead} \tag{3.32}$$

Looking at the data sheet of the power devices, it's reported the switching energy required during an hard commutation (E_{on}) with 400 [V] and 20 [A] and equal to 134 [mJ]. At the end, the expression of the averaged hard switching losses in the input bridge looks like:

$$P_{hard,in} = \frac{2}{T_{hf}}\frac{E_{on}}{400 \cdot 20} v_{cs,in} I_{hard,in} \tag{3.33}$$

The same reasoning can be done for the output bridge: in the cases in which d_{output} is negative, the time instant in which hard switching occurs in the output bridge is $t_{out,h} = \frac{t_{dead}}{2} + dT_{hf}$ and the corresponding current value is equal to:

$$I_{hard,out} = \frac{t_{out,h} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 \tag{3.34}$$

Once again the voltage across the output bridge capacitances at the instant in which the switches are turned on in a hard mode is equal to:

$$v_{cs,out} = (v_o + v_{th,d}) - \frac{1}{C}\frac{I_3}{2}t_{dead} \tag{3.35}$$

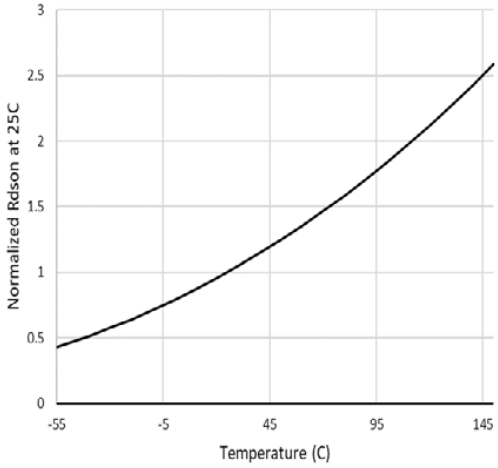


Figure 3.9: Normalized power devices on resistance as a function of the temperature.

The power lost for this case, averaged in half switching period corresponds to:

$$P_{hard,out} = \frac{2}{T_{hf}} \frac{E_{on}}{400{\cdot}20} v_{cs,out} I_{hard,out} \tag{3.36}$$

The total losses for hard switching are the sum of the two aforementioned contributes.
The shutdown losses appear always and are computed starting from the value of energy lost declared in the data sheet, equal to $E_{off} = 14.7$ [mJ] at 400 [V] and 20 [A]. Reporting this value at the normal operating condition and averaging it, the results for the input and output bridge are:

$$P_{off,in} = \frac{2}{T_{hf}} \frac{E_{off}}{400{\cdot}20} v_i I_6 \tag{3.37}$$

$$P_{off,out} = \frac{2}{T_{hf}} \frac{E_{off}}{400{\cdot}20} v_o I_3 \tag{3.38}$$

The next step is to compute the conduction losses in both bridges. The time interval in which the switches conduct t_{cond} goes from $\frac{t_{dead}}{2}$ to $T_{hf} - \frac{t_{dead}}{2}$. The current vector can be computed taking in mind that the waveform changes its slope during this time interval:

$$\begin{cases} I_{cond,in} = \frac{t_{cond}}{dT_{hf}}(I_1 + I_2) - I_1 & \text{if} \quad t_{cond} \leq dT_{hf} \\ I_{cond,in} = \frac{t_{cond} - dT_{hf}}{T_{hf} - dT_{hf}}(I_1 - I_2) + I_2 & \text{if} \quad dT_{hf} \leq t_{cond} \leq T_{hf} - \frac{t_{dead}}{2} \end{cases} \tag{3.39}$$

Computing the rms discrete value of the conduction current, the conduction losses can be obtained considering the resistance between drain and source ($R_{ds,on}$), this corresponds to 25 [mΩ] at 25 [°C] and looking at the plot in the data sheet reported in fig. 3.9 in which the normalized resistance is presented as a function of the junction temperature, a value of 40 [mΩ] has been selected for this computation, which corresponds to consider a junction temperature equal to 75 [°C]. The averaged conduction power lost in the input bridge is equal to:

$$P_{cond,in,avg} = 2 R_{ds,on} I^2_{cond,in,rms} \frac{t_{cond}}{T_{hf}} \tag{3.40}$$

For what concern the output bridge, the basic steps are the same: the conduction time is always t_{cond}, whereas the conduction current is expressed as:

$$\begin{cases} I_{cond,out} = \frac{t_{cond}}{T_{hf}-dT_{hf}}(I_1 - I_2) + I_2 \quad \text{if} \quad t_{cond} \leq (1-d)T_{hf} \\ I_{cond,out} = \frac{t_{cond}-(1-d)T_{hf}}{dT_{hf}}(-I_1 - I_2) + I_1 \quad \text{if} \quad (1-d)T_{hf} \leq t_{cond} \leq T_{hf} - \frac{t_{dead}}{2} \end{cases} \tag{3.41}$$

Computing the rms value of the above current, the conduction losses in the output bridge, averaged in half switching period, correspond to:

$$P_{cond,out,avg} = 2R_{ds,on}I^2_{cond,out,rms}\frac{t_{cond}}{T_{hf}} \tag{3.42}$$

For what concern the transformers, the two PQ5050 designed are considered (they are documented in the transformer chapter): in the first case, just for sake of clarity, the litz wire with 2250 strands has been used with 9 turns and the specific power lost was 1000 [kW/m^3]; in the second case two litz wire with 450 strands have been twisted and connencted in parallel, in this case the number of turns was 12 and the specific power lost around 180 [kW/m^3]. In both cases, the rms value of the leakage inductance current I_L has been computed starting from the expression of the whole waveform:

$$\begin{cases} I_L = \frac{t_{cond}}{dT_{hf}}(I_1 + I_2) - I_1 \quad \text{if} \quad t_{cond} \leq dT_{hf} \\ \\ I_L = \frac{t_{cond}-dT_{hf}}{(1-d)T_{hf}}(I_1 - I_2) + I_2 \quad \text{if} \quad dT_{hf} \leq t_{cond} \leq T_{hf} \end{cases} \tag{3.43}$$

Once obtained the rms component, the core P_c and DC P_{dc} power losses are computed through the expressions described in the next chapter about the transformer and shown below:

$$P_c = P_v A_e l'_e \tag{3.44}$$

$$P_{dc} = 2\frac{\rho N l_w}{N_s A_{awg,44}} I^2_{L,rms} \tag{3.45}$$

The power lost due to proximity effect is computed starting from the computation of the vectors that describe the incremental ratios (the expression is explained in the transformer chapter):

$$d_{er,1} = (\frac{I_2 - (-I_1)}{dT_{hf}})^2 dT_{hf} \tag{3.46}$$

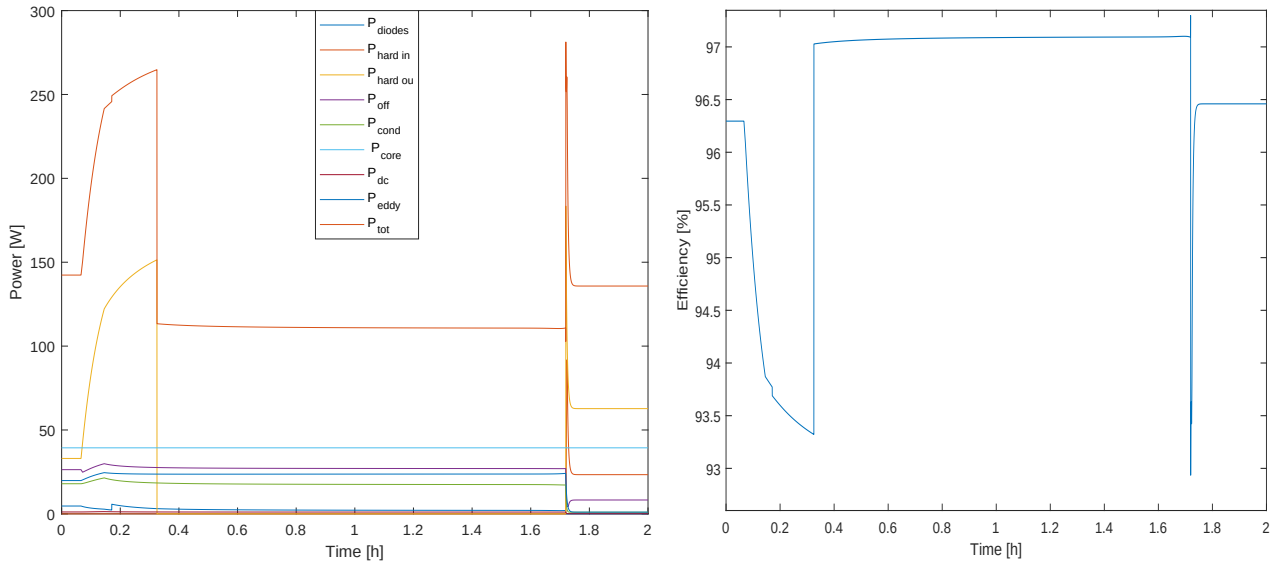
$$d_{er,2} = (\frac{I_1 - I_2}{(1-d)T_{hf}})^2 (1-d)T_{hf} \tag{3.47}$$

The eddy current losses in both the windings are computed by means:

$$P_{eddy} = 2\frac{\mu_0^2 \pi N N_s l_w d_c^4}{192\rho r_w^2}\frac{d_{er,1} + d_{er,2}}{T_{hf}} \tag{3.48}$$

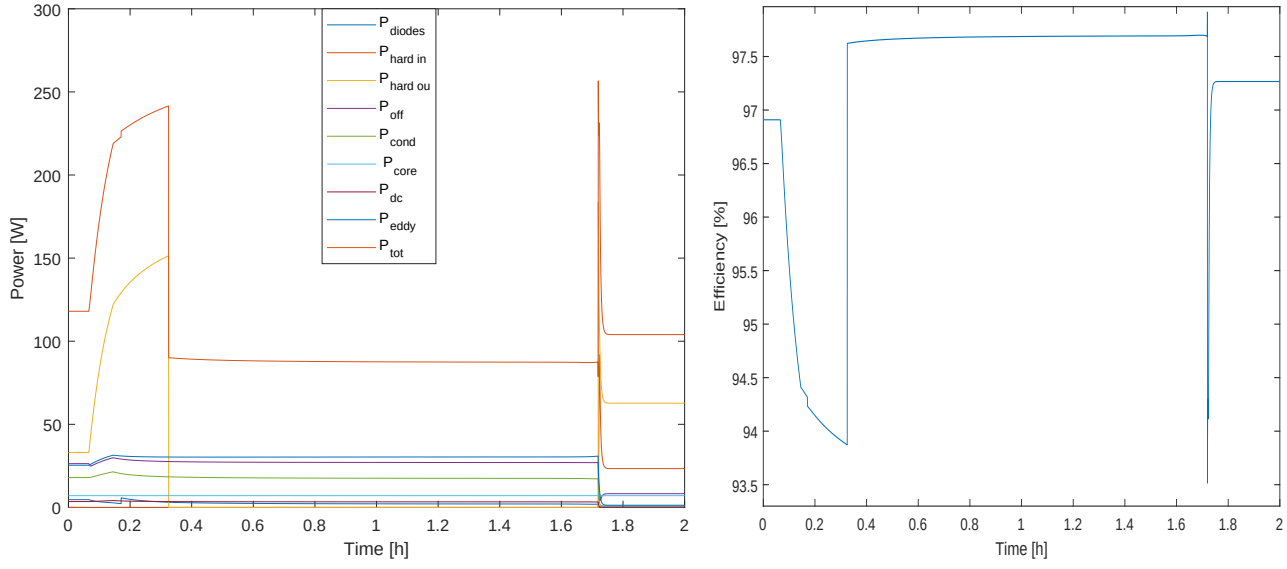
In fig. 3.10(a) the total power lost and the different contributes are plotted in function of the charging time, in the case of the transformer with the biggest litz wire but the smallest turns number; besides in picture 3.10(b) the efficiency curve is presented. The last plateau in both graphs represents the time in which the battery stack reaches the full charge condition and maximum terminals voltage.

Just to make a comparison, the total power lost in the case of PQ5050 transformer with 12 turns, 900 strands and a leakage inductance of 7 [μH] has been reported in fig. 3.11(a) and the respective efficiency in picture 3.11(b). As



(a) (b)

Figure 3.10: Total power losses and efficiency during a charging process in the case of PQ5050 transformer with 9 turns.



(a) (b)

Figure 3.11: Total power losses and efficiency during a charging process in the case of PQ5050 transformer with 12 turns.

can be seen, since the core loss is lower, the efficiency is higher than the previous case, but it has to be outlined that the losses due to proximity effect are bigger in the reality than those ones computed by means the analytical formula cause of the four not interleaved secondary winding layers. In both cases it appears that the whole charger efficiency drastically decreases in buck and boost mode boundaries, since the total power lost reaches high values. The graphs about the designed PQ4040 haven't been reported to not make heavy the conclusion of this chapter, since it's supposed that the aforementioned transformer will present high winding losses due to the high current density (as it's described in the next chapter).

4 High frequency transformer design

The high frequency transformer represents the central component for the dual active bridge, since it accomplishes different tasks:

- it guarantees the galvanic isolation between the two bridges;
- it allows to interface parts of the circuit with different voltage ranges;
- it acts like a sink of energy, stored in the leakage flux, that is useful to guarantee the ZVS switching mode, permitting to charge and discharge the switches parasitic output capacitances.

In this chapter a general characterization of the high frequency transformer is presented, taking into account all the aspects that make its design tortuous; furthermore, the several transformers designed are described: in each of them, the goals of minimum losses, minimum volume and big leakage inductance stored in the leakage flux are excluded each other, for this reason a trade off has been taken into account, in order to get an acceptable result for all the requirements.

4.1 General characterization of a high frequency transformer

A transformer is able to link two parts of a circuit without any direct connection, but taking advantage of the Faraday's law:

$$v = -\frac{d\lambda}{dt} = -N\frac{d\phi}{dt} = -NA_e\frac{dB}{dt} \tag{4.1}$$

The aforementioned law states that the electromotive force (EMF) induced in a circuit is equal to the rate of change of the flux linked with that circuit; in addition Lenz's law proves that the sign of the induced voltage is that the induced electromotive force will oppose to the flux creating it, like shown in (4.1), where:

- λ is the linked flux;
- N is the winding number of turns;
- ϕ is the flux through the surface of a single turn;
- A_e is the effective area of the core.

Considering the ideal circuit of an un-gapped transformer, like shown in fig. 4.1, the flux through the two windings can be considered to be the same, hence, taking in mind the Faraday's law, the relationship between the voltage conversion ratio and the turn ratio is found: $\frac{V_1}{n_1} = \frac{V_2}{n_2}$. Again, considering a magnetizing inductance quite high to be negligible the current that flow through the path in derivation, the magnetizing current can be neglected. In this way, the currents in the primary and secondary windings have the same magnitude; as a consequence of it, the magneto motive force in the primary side is equal to that one in the secondary side, since for the hypothesis no magnetic energy is stored in the core, bringing to the following equality: $n_1 I_1 = n_2 I_2$. In any transformer the core losses are distinguished into two different groups:

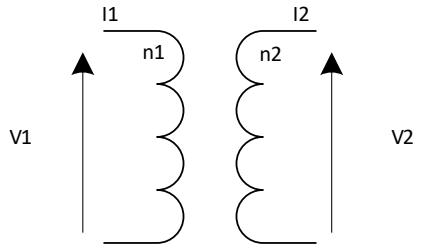


Figure 4.1: Ideal circuit of a single phase transformer.

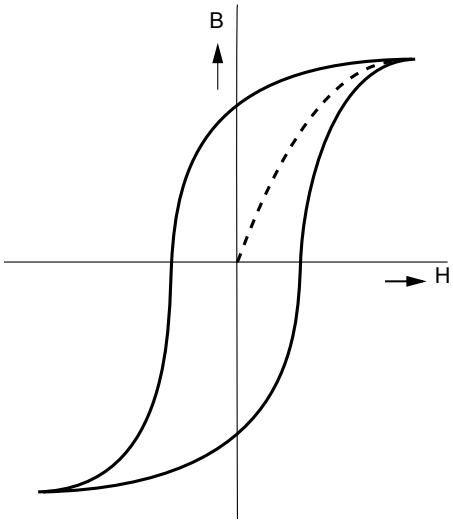


Figure 4.2: Hysteresis loop.

- hysteresis losses;
- eddy current losses.

A typical $B-H$ characteristic loop of a magnetic material is shown in fig. 4.2. During the magnetization process, the Weiss domains inside each magnetic crystal have to be aligned with the direction of the magnetic field that is applied to the transformer.
To accomplish this aim some energy barriers have to be overcome and this is the reason for the arising of the hysteresis loop: the energy required to magnetize the core won't be completely returned during the demagnetization path, the area inside the $B-H$ curve represents losses in the core that decrease the efficiency of the magnetic coupling and increase the working temperature. In each magnetic material (laminated and ferrite types), some parameters are quite important:

- the maximum allowed flux density;
- the coercitive magnetic field;
- the Curie temperature.

The first one is regarded to the saturation of the core: if the boundary value of the magnetic flux density is overcome, the rate of change of the magnetic field strength and the flux density is not more linear, hence big increases in the

magnetic field won't produce big increases in the flux density. A consequence of this effect is a fall in the permeability of the core. During a magnetizing cycle, since the energy won't be returned completely, applying a null magnetic field through the core, a residual flux density will result: the second parameter refers to the negative magnetic field necessary to get cross zero flux density. The third one states the upper limit of the working temperature, above what the magnetic properties of the core are faded (the process is reversible).
The hysteresis losses are directly dependent on the alternate flux density B_{ac}, the frequency and a coefficient k that depends on the type of the core material, like stated in the following equation:

$$P_{hy} = k f^{\alpha} B_{ac}^{\beta} \tag{4.2}$$

The exponents in the above equation are linked to the kind of material; this equation applies over a limited range of frequency and flux density (the frequency is expressed in kHz and the flux density in mT) [16]. The apparent power in a transformer is proportional to the product fB_{ac} and this term, called "performance factor", is of fundamental importance in the choice of the type of material to be used for the core. As the performance factor has a non linear behaviour and it decreases at very high frequency, the equation (4.2) can't be applied to compute the hysteresis losses in transformer working at very high frequency.
The other source of losses in the core has to be found in the presence of eddy currents that flow in the magnetic circuit in opposite direction with respect the main current that produces the main flux. These eddy currents are produced by fast varying magnetic fields. The effect of the eddy currents is to create a kind of "mirror" in deeper region of the core against the desired flux.
The skin depth can be computed in conducting material as:

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \tag{4.3}$$

where:

- ω is the working pulsation;
- μ is the permeability of the material;
- σ is the material conductivity.

The expression of the skin depth presents a decaying exponential behaviour. Also at quite low frequency (50-60 Hz) it results a skin depth quite small: for this reason the bulky structure of power transformer is made of laminated steel sheets. The power lost caused by eddy currents can be computed through the equation:

$$P_{ed} = k_{ed} f^2 B_{ac}^2 \tag{4.4}$$

in which k_{ed} is a constant that depends on the material. In the case of both high power and frequency, laminated cores don't present an enough big resistivity against the induced currents: for this reason, ferrite materials composed of manganese and zinc (MnZn) are used. In this case the core is made of very small conductive crystals that are isolated each other, in order to show a high magnetic permeability meanwhile taking high the resistivity. In the case of ferrite cores the eddy current losses are negligible. In high frequency transformer the limitation in the flux density is not dictated by the saturation but by the specific core losses, as it will be discussed in a future paragraph.

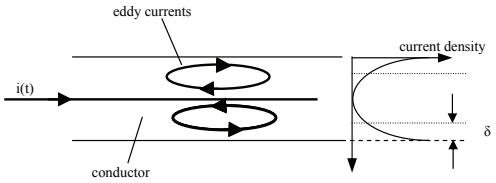


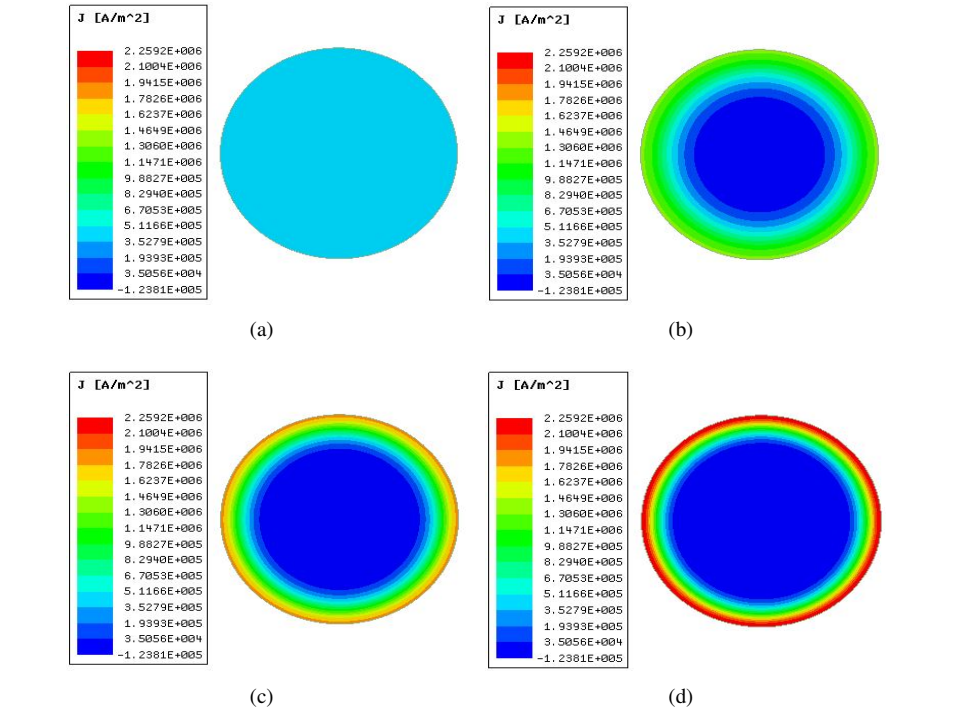
Figure 4.3: Current distribution on a bare wire carrying high frequency current.

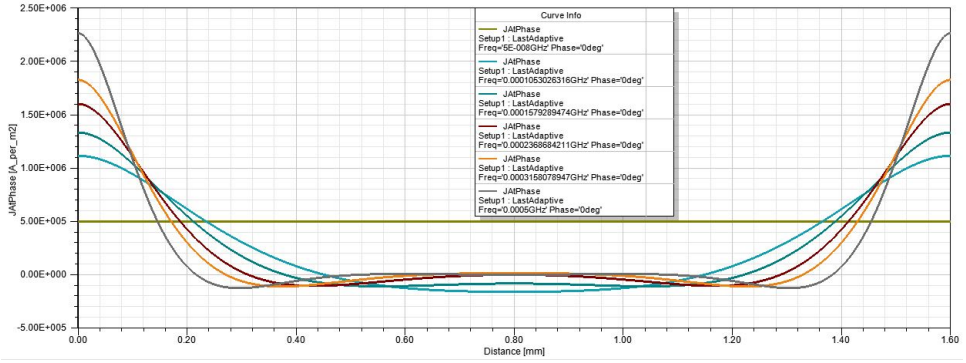
4.2 High frequency effects on the windings

For what concern the windings, high frequency creates a not homogeneous distribution of the current inside the conductor, giving arise to two main effects: the skin effect and the proximity effect. The first one is linked, as stated for the core of the transformer, to the skin depth (4.3). In the case of this work, substituting in the aforementioned equation the value of the copper parameters:

- the copper magnetic permeability is considered equal to that one of the air, i.e. $\mu = 4\pi 10^{-7}[H/m]$;
- the copper resistivity (the inverse of the conductivity σ) is equal to $\rho = 0.0171[\frac{\Omega mm^2}{m}]$ at a temperature of 20 [°C];

it results a skin depth at ambient temperature equal to $\delta = 92.2[\mu m]$. Since the resistivity is in the numerator of the skin depth equation, it's a good design choice to consider the ambient value, in order to take into account a smaller value of the skin depth. As can be seen in fig. 4.3, the main time-varying current generates an alternating magnetic field which in turn "gives life" to eddy currents. The last ones flow in opposite direction, with respect the main current, in the inner section of the wire, creating a sort of shield and for this reason it appears a smaller cross section area for the main flow of the current; the consequence of this effect is a concentration of the current in the surface, which implies a bigger current density and a bigger resistance with respect the direct current case.
Figure 4.4 is a FEM simulation of the skin effect in a copper wire of 1.6 [mm] diameter, carrying a current of 1 [A]. Shifting from fig. 4.4(a), in which the working frequency is 50 [Hz], to fig. 4.4(d) where the operating frequency is 500 [kHz], it's possible to see that the current distribution won't be any more on the whole cross section area of the conductor, but it tends to concentrate in a smaller ring near the surface. As expected, in a solid wire the resistance is directly proportional to the frequency: in fig. 4.5 it appears that the resistance is about 7 times bigger at 500 [kHz] with respect the case at low frequency, in which the conductor diameter is smaller than the respective skin depth.
Besides the skin effect there's also the proximity effect, due to the field generated by the adjacent wires, that contributes to create a not homogeneous current distribution. The proximity effect is bigger if a lot of conductors, carrying alternate current, are wrapped closely, like in the case of a transformer coil. The proximity effect is highlighted increasing the magnetic field strength, making a lot of turns carrying a current of the same direction, as can be seen in fig. 4.6. In the aforementioned FEM simulation it appears how the proximity effects strongly relies on the working frequency: shifting from a frequency of 250 [kHz] (plot. 4.6(a)) to a frequency of 500 [kHz] (plot 4.6(b)), the shielding effect of the parasitic currents increases and hence the main current is forced to flow in a narrow surface, creating a lot of Joule losses and high temperature in the windings. In the simulation, a foil wire with a rectangular surface has been taken into account, in particular the first two and last one wires are conducting a positive current, instead the three central ones are conducting a negative current. It emerges that the current distribution tends to concentrate in the face to face surfaces if wires with opposite currents are near, otherwise it tends to move in the opposite surfaces of the wires. It can be concluded that the proximity effect emphasizes the bad consequences of the aforementioned skin one.





(e)

Figure 4.4: Current density distribution in a bare wire increasing the operating frequency.

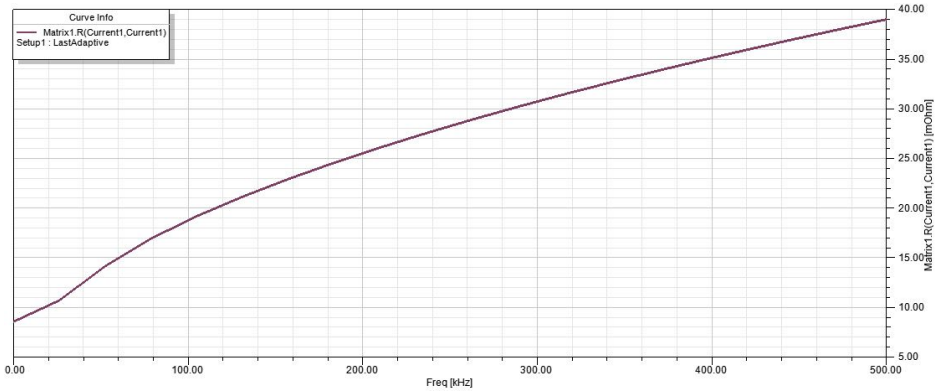
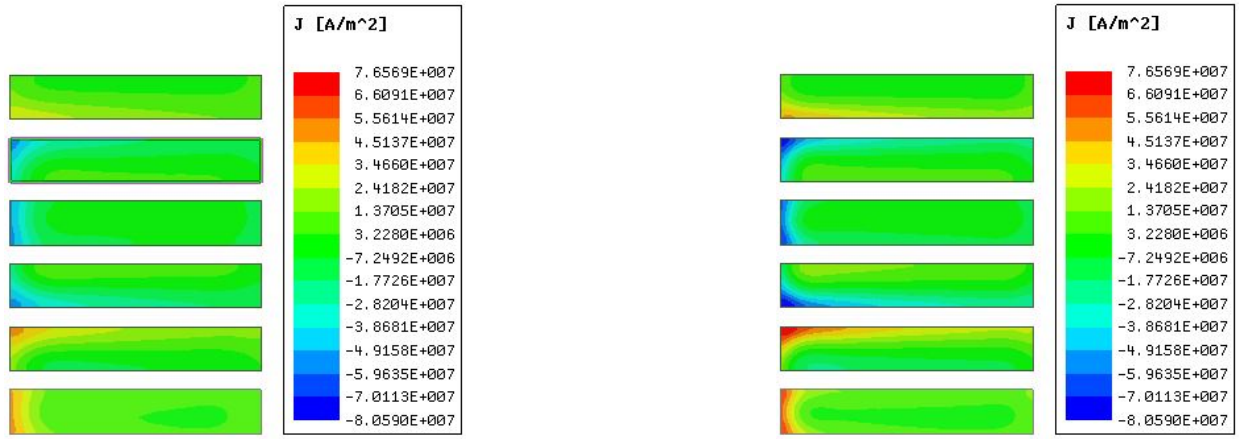


Figure 4.5: Increasing wire resistance with the frequency.



(a) (b)

Figure 4.6: Proximity effect in multilayer windings.

In order to increase the useful cross section of the wire and increase the whole efficiency of the transformer, it's necessary to decrease the dimension of the single wire and, in order to carry high currents, put multiple wires in parallel: such a kind of design is called litz wire. This conductor is composed of thin enamelled copper filaments, then isolated from each other, wrapped in a helix and enclosed by an external sheath. All these parallel strands have to be twisted, in order that each single filament moves periodically around all the space of the whole wire; this periodic transposition allows a compensation between the voltage induced in two successive half twisting paths: in this way, since the induced voltage has opposite sign, the net eddy current in the twisted strands will be almost negligible. The litz wire are classified in different ranges of thickness (AWG); a good design choice is to apply a conductor with strands diameter smaller than two time the skin depth, in order to ensure that all the cross section will carry current. As a coin, there are always two faces: on one hand it's possible to decrease the increase of resistance (alternating resistance R_{ac}), but on the other hand the filling factor is not high and furthermore, since the single strands are twisted, the total copper length overcomes that one measured making the coils.

4.3 General design steps

As stated before in the paragraph about the characterization of power electronic transformer, the upper boundary for the flux density is not more related to saturation (in that case, when the transformer reaches that boundary, the inductance goes down, creating a dangerous operation mode), but to core losses that increases with the frequency. Starting from (4.1), it's possible to isolate the term regarding the derivative of the flux density and subsequently, making integration, the following equation results:

$$\Delta B = \frac{1}{NA_e} \int_0^{T_{hf}} V_o dt \tag{4.5}$$

The effective area A_e, already mentioned at the beginning of this chapter, can be found in each manufacturer's data sheet regarding the particular core geometry. Together with the effective length l_e and the effective volume V_e, it's used to express the non-uniform core shape like that one of an equivalent ring core, described by the aforementioned parameters. Taking advantage of these equivalent parameters, the computation, in square wave operation, of the peak

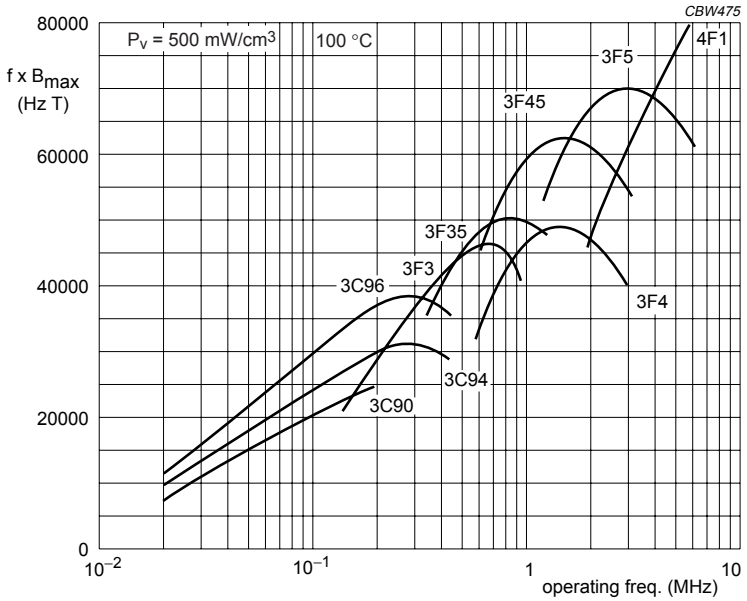


Figure 4.7: Performance factor of different ferrite materials produced by Ferroxcube.

magnetic flux density and magnetic field is made:

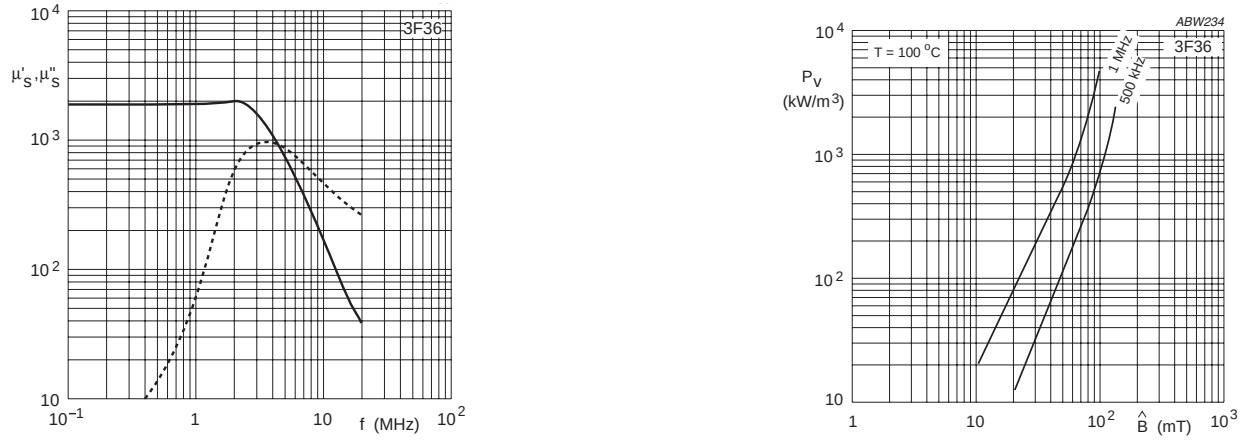
$$\widehat{B} = \frac{\widehat{V}}{4fNA_e} \tag{4.6}$$

$$\widehat{H} = \frac{IN\sqrt{2}}{l_e} \tag{4.7}$$

in which $\widehat{V}$ states the peak voltage applied. Depending on the type of the winding, the operation of the transformer can be symmetric or asymmetric: as it will be explained hereafter the first mode is more desirable, since it makes possible to limit both windings and core losses. The first step of the approach followed starts with the choice of the core: the Ferroxcube PQ core shape has been selected, since it has a central leg that allows to minimize concentrated losses in the coils. Taking a look in the manual of the manufacturer [17], a fundamental parameter, linked to the apparent power that flows in the transformer, is taken into account, in order to choose the best material for the required working frequency (500 [kHz]): the so called "performance factor", defined as:

$$P_{fc} = f\widehat{B} \tag{4.8}$$

As stated before, this product has a non linear behaviour with a peak value at different frequency for different core materials. Through the plot 4.7, it appears that at low frequency almost all the materials have the same performance factor: this is due to the fact that in this operation range, the flux density in the core is limited by saturation and not by core losses; the waveforms diverge at bigger frequency, where each material shows an optimal working point, in which the power density will be the maximum. Remembering the working frequency, the material 3F35 presents the best performance. Since the material 3F35 has been replaced, 3F36 has been taken into account. From the data sheet, the complex permeability and the specific power losses are considered. In order to represent the permeability of the core as a function of the frequency, like shown in fig. 4.8(a), it's necessary to take into account that the coil, made up of the winding and the core, won't behave as an ideal inductance, but there's always a resistive component that causes a shift in the angle between the voltage and the current; this fact creates magnetic losses that are taken into account



(a) (b)

Figure 4.8: Complex permeability and specific power losses in ferrite 3F36.

through a complex representation of the permeability:

$$\mu = \mu_s' - j\mu_s'' \tag{4.9}$$

For what concern the core losses, as stated before, they can't be computed with classical formulas in which a sinusoidal excitation is supposed, because in a square wave mode, high order harmonics will contribute to increase the losses. Obviously also the core temperature is affected by the specific losses, but this kind of ferrite presents lower losses at temperature in the range of 80-90 [°C], for this reason a design focused on keeping low the temperature of the core, i.e. shifting the main amount of power lost in the windings, couldn't result in the best solution.

4.3.1 General loss model

To start the design iter, a consideration based on the Faraday's law is necessary [18]. The nominal condition considered is the nominal output voltage, i.e. 370 [V] peak value. The voltage-second exerted in the core is equal to:

$$V_{sec} = NB_{peak-to-peak}A_e = 370[\mu sV] \tag{4.10}$$

where:

- N is the number of turns in the primary or secondary winding, since the turn ratio is unitary;
- $B_{peak-to-peak}$ is the maximum ΔB that can occurs during a half switching period (since the voltage waveform is symmetric), in particular it can be equal to $\widehat{B}$ if the operation mode is asymmetric or to the difference between both positive and negative $\widehat{B}$ if the working condition is symmetric;
- A_e is the effective area, as described in the previous paragraph.

To explain the reason because the maximum flux variation is equal to 370 [μVs], some considerations on the circuit 4.9 have to be done: in a magnetic circuit the magneto motive force is the equivalent of the electro motive force in an electric circuit, whereas the flux ϕ is the homologous of the current. Remembering that the current through the transformer is trapezoidal the variation of the current in a half switching period can be approximated through the

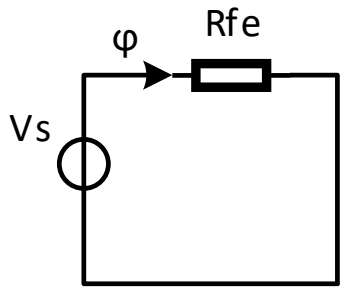


Figure 4.9: Magnetic circuit of the transformer.

trapezi expression, since the time step is very small:

$$\Delta I = \frac{V_L \Delta t}{L} \tag{4.11}$$

Considering an unitary length solenoid, the following system can be used to get the expression of the self inductance:

$$\begin{cases} H = \frac{NI}{1}, & [A/m] \\ \phi = \frac{H}{R_{fe}}, & [Wb] \\ \lambda = N\phi, & [Wb] \\ L = \frac{\lambda}{I}, & [H] \end{cases} \tag{4.12}$$

in which:

- H is the magnetic field;
- λ represents the linked flux;
- R_{fe} is the core reluctance, since there aren't air gaps.

From the last equation of the above system (4.12), the expression of the self inductance results:

$$L = \frac{N\frac{NI}{R_{fe}}}{I} = \frac{N^2}{R_{fe}} \tag{4.13}$$

The variation of the flux can be computed as:

$$\Delta\phi = \frac{N\Delta I}{R_{fe}} = \frac{NV_L\Delta t}{R_{fe}L} = \frac{370}{N} \tag{4.14}$$

The right side term of the last equation is the demonstration of the Faraday's equation, since $\Delta\phi = \Delta B A_e$. To keep the thermal stability of the core, the specific power loss is chosen equal to 500 [kW/m^3]; taking advantage from the plot 4.8(b), the corresponding peak flux density is 88 [mT] and, imaging to start the design approach with a symmetric transformer, the maximum ΔB is 176 [mT]. In fig. 4.10 the bobbins layout is presented: the grey rectangles represent the primary winding split into two layers, instead the two internal white stand for the secondary winding. With such disposition, it's possible to get a symmetric magnetic field and keep low the proximity effect since there are no multi layers side to side creating big flux density value, in this way the magneto motive force MMF reaches its peak after the first layer and it's null between the two layers of the secondary winding. The magnetizing current is neglected, in this way the magnitude of the current in both windings is the same.

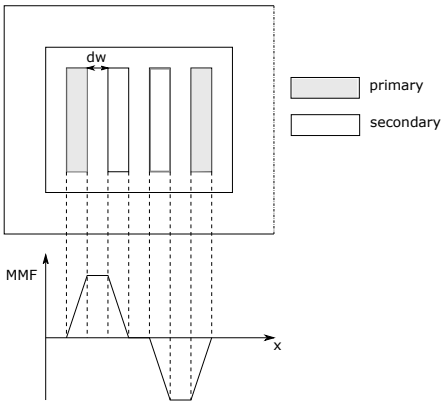


Figure 4.10: Magnetic field in half symmetric transformer.

As stated previously, litz wire are used. In the laboratory PACK RUPALIT V155 AWG 44 is available, with a single strand diameter of 0.05 [mm]. From this assumption, the bundle wire radius can be computed as a function of the number of strands:

$$r_{wire} = \sqrt{\frac{N_s A_{awg44}}{\pi F}} \tag{4.15}$$

where:

- A_{awg44} is the cross section area of a single strand;
- F is the filling factor for the bundle wire, typical value for litz wire is 0.4;
- N_s is the number of strands.

Since in PQ cores the central leg is round, obtaining the effective area A_e from the equation (4.10), the radius of the central leg can be expressed as a function of the number of turns, like shown in the following equation:

$$r_c = \sqrt{\frac{A_e}{\pi}} = \sqrt{\frac{V_{sec}}{\pi N \Delta B}} \tag{4.16}$$

Assuming to wish to wrap the bobbins in the way illustrated in picture 4.10, the medium length MLT per turn of both primary and secondary windings is:

$$MLT = 2\pi(r_c + 4r_{wire} + 1.5d_w) = l_w \tag{4.17}$$

where d_w is the clearance between each layer.
In the interleaved symmetric layout, the MMF reaches its peak value after the first layer of the primary winding and it's equal to:

$$\widehat{MMF} = \frac{N}{2} i(t) \tag{4.18}$$

The magnetic field produced by the the first layer of each winding, that can be seen like a solenoid, is equal to:

$$H(t) = \frac{N}{2} \frac{i(t)}{h} \tag{4.19}$$

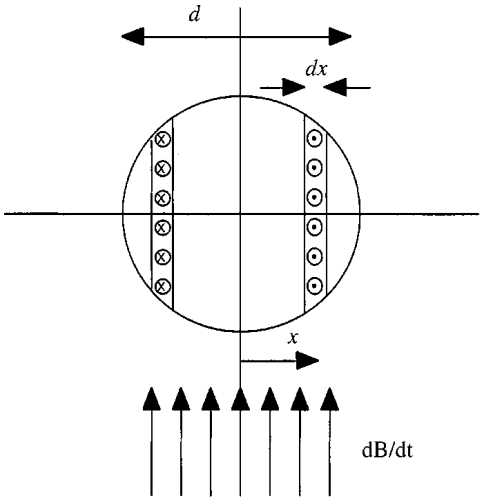


Figure 4.11: Cylinder conductor in a uniform magnetic field.

in which h states the height of the coil, so it can be simply computed as a function of the number of turns: $h = 2r_w \frac{N}{2}$. Making the opportune simplification, the expression of the magnetic field penetrating each layer is:

$$H(t) = \frac{i(t)}{2r_w} \tag{4.20}$$

To take into account the eddy current effects in high frequency transformer with finite element method, scale problems arise during the mesh computation, since in the same project components with several different order dimensions coexist, i.e. litz wires that require a very high resolution mesh, air and core that are bigger with a different resolution requirement. To overcome this problem, in [19] the so called "squared-field-derivative method" is presented. This method is based on some assumptions:

- the diameter of the single round wire, i.e. the single strand, has to be quite smaller with respect the skin depth;
- a 2-D analysis in considered, meaning that only the component of the field perpendicular to the wire axis is considered, instead the component parallel to it is neglected, since it has been demonstrated that in components in which the third dimension is regular, the loss contribution is negligible.

The first assumption allow to consider constant the field in the conductor surface; although this assumption lets to neglect the loss contribution due to skin effect, it appears that, especially in multi-layers winding, the proximity effect will contribute to unexpected power lost. The first step of this method consists in the computation of loss in a wire immersed in an unified field. Considering the geometry shown in fig. 4.11, a closed loop of thickness dx that goes from x to $-x$ is considered, in order to compute the derivative of the flux in the identified section:

$$\frac{d\phi}{dt} = 2xl\frac{dB}{dt} \tag{4.21}$$

in which l represents the length of the cylinder in the third dimension, in fact the product $2xl$ describes the section of the aforementioned closed loop.
The resistance of this path is equal to:

$$R = \frac{2l\rho}{2\sqrt{\frac{d^2}{4} - x^2}dx} \tag{4.22}$$

in which ρ is the copper resistivity at 90 [°C], computed as:

$$\rho = \rho_{20}(1 + \alpha(90 - 20)) = 2.2083{\cdot}10^{-5}\ [\frac{\Omega mm^2}{mm}] \tag{4.23}$$

Remembering the fundamental Faraday's equation, the electro motive force induced in a closed path is equal to the rate of flow change, hence the power dissipated in the differential elements dx is equal to $(\frac{d\phi}{dt})^2 \frac{1}{R}$; integrating this last equation, the instantaneous power loss in the single strand is:

$$P_{eddy}(t) = \int_0^{\frac{d}{2}} (2xl\frac{dB}{dt})^2 \frac{\sqrt{\frac{d^2}{4} - x^2}}{l\rho} dx = \frac{\pi l d^4}{64\rho}(\frac{dB}{dt})^2 \tag{4.24}$$

where:

- ρ is the copper resistivity;
- d is the conductor diameter.

As highlighted in [19], this method consider only the "strand-level" effects, hence the ac loss due to eddy currents circulating inside the single strand, and neglect eddy currents circulating between each strands, because with an opportune twisting, the induced voltages will cancel each other. Substituting the derivative of the induction B with that one of the magnetic field, since the permeability of the copper doesn't change, and making the spatial average, the eddy current loss in a single strand is equal to:

$$\left\langle P_{eddy}(t) \right\rangle = \left\langle \frac{\mu_o^2 \pi N l_w d^4}{64\rho}(\frac{dH}{dt})^2 \right\rangle \tag{4.25}$$

$$= \frac{\mu_o^2 \pi N l_w d^4}{192\rho}(\frac{dH}{dt})^2 \tag{4.26}$$

$$= \frac{\mu_o^2 \pi N l_w d^4}{768\rho r_w^2}(\frac{di}{dt})^2 \tag{4.27}$$

in which l_w is the medium winding length increased of the 5% in order to take into account the effect of twisting. The current derivative can be computed starting from the waveform simulation of the circuit and the time averaged eddy current loss due to proximity effect in each of the two windings in a switching cycle is given by:

$$P_{eddy} = \frac{N_s}{T}\int_T \left\langle P_{eddy}(t) \right\rangle dt \tag{4.28}$$

$$= \frac{\mu_o^2 \pi N N_s l_w d^4}{768\rho r_w^2 T}\int_T (\frac{di}{dt})^2 dt \tag{4.29}$$

The formula above has a general character necessary to get a power lost information as a function of both number of strands and number of turns, since both of them could change also the volume of the selected core, the winding area and hence the current density; furthermore, the squared current derivative refers to the current that flow through the leakage inductance in the Simplorer circuit model and for this reason doesn't take into account the different current distribution due to the currents that flow in the interleaved layers with different signs. Furthermore there are no information about the winding geometry, i.e. how the total number of turns of each winding is distributed in a multi-layer configuration, how the different layers are interleaved each other and so on.
To overcome these drawbacks, a more accurate computation of eddy current losses can be done knowing the transformer design and through the use of FEM (Finite Element Method) software.

As underlined in [19], in a given winding the magnetic flux density $\vec{B}$ is not independent from the flux density produced by the current that flows in the other winding, but it results in a superimposition of them; after this reasoning, the eddy current loss in one of the two windings becomes:

$$P_{eddy_{p,s}} = \gamma_j \frac{1}{T} \left\langle \int_T (|\frac{d\vec{B_p}}{dt}|^2 + \frac{d\vec{B_p}}{dt} \cdot \frac{d\vec{B_s}}{dt} + \frac{d\vec{B_s}}{dt} \cdot \frac{d\vec{B_p}}{dt} + |\frac{d\vec{B_s}}{dt}|^2) \right\rangle \tag{4.30}$$

where $\gamma_j = \frac{\pi N_j l_w d^4}{64\rho}$ is the so called "loss constant". As can be seen in the above equation, the power lost due to eddy currents in strand level computation is not more dependent on just the magnetic flux density on the regarded winding, but it takes into account also the effect due to the presence of the other winding. If the strand diameter is smaller than the skin depth, the magnetic flux density can be thought proportional to the current that flows inside each cylindrical conductor, hence (4.30) for both coils becomes:

$$P_{eddy,tot} = \frac{1}{T} (\int_T [\frac{di_p}{dt} \quad \frac{di_s}{dt}] \mathbf{D} \int_T [\frac{di_p}{dt} \quad \frac{di_s}{dt}]') \tag{4.31}$$

in which the matrix **D** is called "dynamic resistance matrix" and has dimension of $[\Omega s^2]$, it takes into account not only the internal resistance of each winding, but also the mutual resistances. The formulation of this matrix is as follow:

$$\mathbf{D} = \gamma_p \left\langle \begin{bmatrix} |\hat{\vec{B_p}}|^2 & \hat{\vec{B_p}} \cdot \hat{\vec{B_s}} \\ \hat{\vec{B_s}} \cdot \hat{\vec{B_p}} & |\hat{\vec{B_s}}|^2 \end{bmatrix} \right\rangle_p + \gamma_s \left\langle \begin{bmatrix} |\hat{\vec{B_p}}|^2 & \hat{\vec{B_p}} \cdot \hat{\vec{B_s}} \\ \hat{\vec{B_s}} \cdot \hat{\vec{B_p}} & |\hat{\vec{B_s}}|^2 \end{bmatrix} \right\rangle_s \tag{4.32}$$

The field calculation can be simplified putting a specific current density in the winding area, without making the single turn of each winding. However the solution of (4.30) doesn't seem easy to compute analytically, since the expression of the induction vectors is not known, furthermore the amplitude changes during a switching period, since the flux density is proportional to the trapezoidal current waveform. A simplified idea to compute the matrix **D** could be: excite the transformer with the current in each single winding distinctly in FEM software with maximum current, take the square of the module of B and perform the spatial average, in order to find the diagonal terms; then excite both windings together, make the scalar product and the spatial average and lastly subtract the first and last terms of the matrix in order to find the out-diagonal terms. From theory, the scalar product between two vectors is equal to the product among their modules with the cosine of the angle between them: since an expression of the vectors lacks, another simplification could be to regard the two vector in phase opposition, so that the cosine argument could become unitary (in module); this assumption lays on the fact the the magnetizing current is considered negligible. The last aspect to emphasize is that the spatial average relies on the geometry that can't be known at priori. For this reason, this deeper calculation path won't be followed in this job.

Another different approach to take into account the proximity effect in eddy current losses is that one presented by Dowell for copper foil wire; in order to apply it to litz wire, the thickness of the foil h is replaced by the quantity $h_c = 0.886d$, where $d = 0.05[mm]$ is the diameter of the single strand. As discussed in [20], the analysis starts with the ratio between h_c and skin depth δ that is function of the temperature T:

$$y = \frac{h_c}{\delta(T)} \tag{4.33}$$

Dowell presented two equations that allow to compute some coefficients, both to skin effect and proximity one. Since the skin effect is considered negligible in this design, only the corrective coefficient for the proximity effect is taken

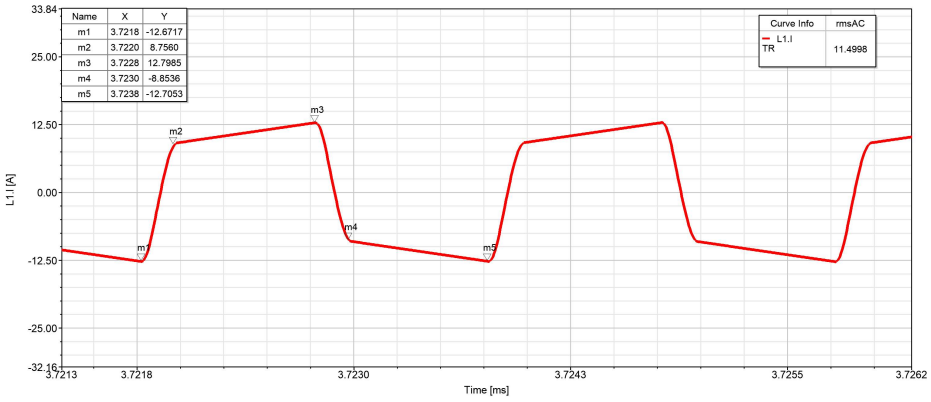


Figure 4.12: Leakage inductance current at nominal working condition.

into account:

$$F_p = \frac{2}{3}y(m^2-1)\frac{sinh(y)-sin(y)}{cosh(y)+cos(y)} \tag{4.34}$$

in which m represents the number of layers of each winding if foil conductors are considered, but with litz wire it should be considered as the number of turns that make the magnetic field strength to arise in one direction. The above equation regards to a sinusoidal excitation; other researchers focused themselves on a way to expand it to square waveform operation, rich of high order harmonics, through an expansion in Fourier's series, shifting from the time to frequency domain.
For what concern the DC winding loss, the computation is lighter, since the winding resistance is not influenced by the AC effects, as it's shown in the equation:

$$P_{dc} = I_{rms}^2 R_{dc} = \frac{\rho N l_w}{N_s A_{awg44}} I_{rms}^2 \tag{4.35}$$

Since the turn ratio is unitary and the transformer structure is quite symmetric, the total winding losses for both windings can be computed as:

$$P_{wind} = 2(P_{dc} + P_{eddy}) \tag{4.36}$$

Focusing the attention on the core, knowing the specific power loss of 500 [kW/m^3], the core loss is given by:

$$P_c = P_v A_e l'_e \tag{4.37}$$

The effective length of the core can be approximated by the mean magnetic path length, as a function of the number of turns:

$$l'_e \simeq l_c = 2(8r_w + 4r_c + Nr_w) \tag{4.38}$$

Knowing all the three power loss components (4.29), (4.35) and (4.37), the total power lost can be computed as the sum of them. To compute the DC power lost the root mean square value of the trapezoidal current in needed. In figure 4.12 the leakage inductance current at nominal working condition, hence 400 [V] as input and 370 [V] as output, with an average output current of 10 [A] is plotted. The simulation has been made in Simplorer Ansys and it allows to rapidly compute the rms current value and the squared derivatives of the current. Since the waveform has a straight

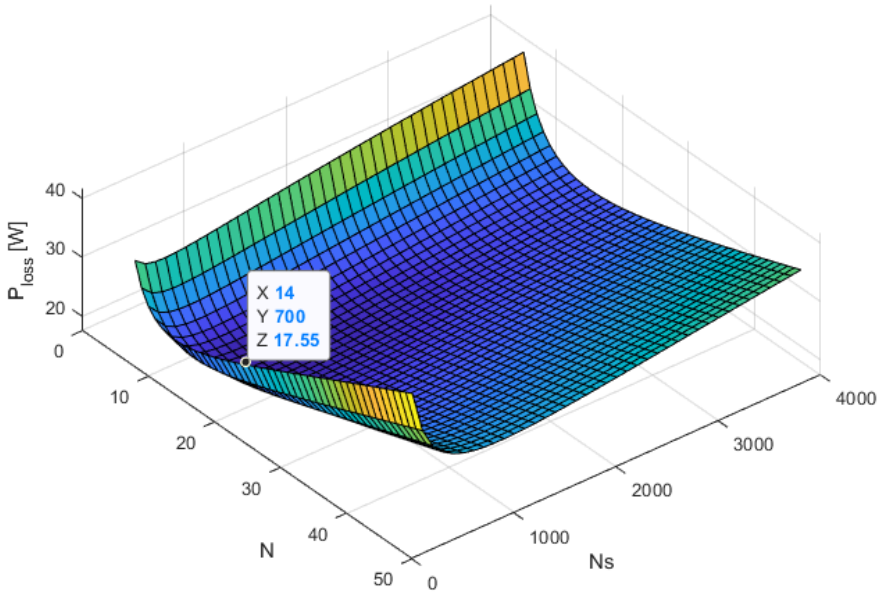


Figure 4.13: Total power lost in the transformer as a function of the number of turns and strands.

line shape and the delta intervals of time are quite small, the total derivative will be approximated with the sum of partial incremental ratio, starting from the values shown by the markers in the aforementioned plot:

$$\begin{cases} \Delta i_{m1,m2} = 21.4277\ [A] \quad \Delta t_{m1,m2} = 0.2[\mu s] \\ \Delta i_{m2,m3} = 4.0425\ [A] \quad \Delta t_{m2,m3} = 0.8[\mu s] \\ \Delta i_{m3,m4} = -21.6521\ [A] \quad \Delta t_{m3,m4} = 0.2[\mu s] \\ \Delta i_{m4,m5} = -3.8517\ [A] \quad \Delta t_{m4,m5} = 0.8[\mu s] \end{cases} \tag{4.39}$$

The incremental ratios are useful to explicit the integral of the total squared derivative, exploiting the integral linearity. As shown in figure 4.13, there is a combination of strands and turns that allow to get minimum transformer power lost, i.e. 700 parallel strands and 14 turns for each winding. Since the available litz wires have 450 or 2250 strands, the smallest configuration is chosen, getting an amount of total losses equal to 18.4194 [W], slightly bigger with respect the optimal choice, so divided:

- $P_c = 6.9228$ [W];
- $P_{eddy} = 2.5886$ [W];
- $P_{dc} = 3.1597$ [W].

remembering that the total winding power lost is equal to $P_{winding} = 2(P_{dc} + P_{eddy})$. With the chosen combination, the cross section area of the core needed results $A_c = 150.1623\ [mm^2]$. The only computation of the cross section area is not sufficient to decide which core is needed, in fact one of the main goal of this design is to store enough leakage energy in order to get the desired value of leakage inductance.

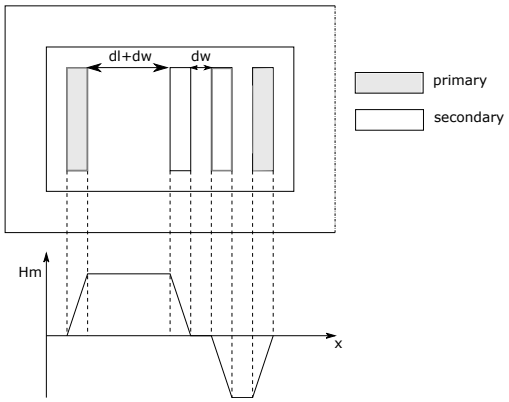


Figure 4.14: Field distribution with bigger space between primary and secondary windings.

4.4 Integrated leakage inductance

It's known that the energy stored in per unit of volume in the magnetic field is given by:

$$w_m = \frac{1}{2}BH = \frac{1}{2}\frac{B^2}{\mu} = \frac{1}{2}\mu H^2 \ [\frac{J}{m^3}] \tag{4.40}$$

The aforementioned relationship is valid if the material has a linear behaviour, that is also the case of high frequency power transformer, since, as it has been said in previous paragraph, the magnetic flux density is not limited by saturation but by core losses. Making the integral in the volume of the magnetic circuit, it results:

$$W_m = \int_{vol} \frac{1}{2}BHd_{vol} = \frac{1}{2}\int_l Hdl \cdot \int_S BdS \tag{4.41}$$

$$W_m = \frac{1}{2}(NI)\Phi = \frac{1}{2}\Psi I = \frac{1}{2}LI^2 \tag{4.42}$$

where:

- Φ is the flux through the surface of a turn;
- Ψ is the linked flux.

It happens that not all the flux generated by the alternated current links both windings: some flux leaks the magnetic core and it encloses itself through the air, the winding, the insulator, i.e. path with bigger reluctance with respect the core one, this will cause a worst coupling between the two windings. To make easier the calculation of the leakage energy, it has been supposed that the magneto motive force generated by each winding is the same, it means that the primary and secondary currents are almost equal (neglecting the small magnetizing current): a consequence of this assumption is that the main flux that links both windings can be neglected and just the leakage flux will be considered. Since the working frequency is very high, the series inductance required is quite small, but in any case bigger than that one stored in a transformer designed to manage a small quantity of reactive power that increases the rms value of the current and hence the losses in the transformer. For this reason, the interleaved structure has to be modified as shown in picture 4.14, in which it has been put a bigger space (dl) between the primary and secondary windings, where the magnetic field strength (and hence the magneto motive force) is maximum. From this plot it can be assumed another hypothesis: the magnetic field varies linearly inside the winding thickness; this assumption is true at low frequency, but a little bit less at higher frequency, where the proximity effect is not negligible, also if it has been observed that in the case of litz wire the variation won't be high. Obviously the field strength along the leakage path depends on

the number of ampere-turns. The computation of the leakage energy will be done just in the two interface between primary and secondary windings, since between the two secondary layers the magnetic field strength is null:

$$W_{lk,p,s,inner} = (\frac{2}{3}\mu_o H_m^2 r_w + \frac{1}{2}\mu_o H_m^2 d_w) N r_w l_{w,p,s,inner} \tag{4.43}$$

$$W_{lk,p,s,outer} = (\frac{2}{3}\mu_o H_m^2 r_w + \frac{1}{2}\mu_o H_m^2 d_w) N r_w l_{w,p,s,outer} + \frac{1}{2}\mu_o H_m^2 dl N r_w 2 r_{3,inner} 2 \tag{4.44}$$

in which:

- dl represents the required space needed to store enough leakage energy in order to match the goal of the required leakage inductance;
- H_m is the peak of the magnetic field strength between the primary and secondary layers;
- $l_{w,p,s,inner}$ is the medium magnetic length of the two inner layers (starting form the center leg of the transformer);
- $l_{w,p,s,outer}$ is the medium magnetic length of the two outer layers;
- $r_{3,inner}$ is the total radius of the three inner layers.

In particular, the three last quantities above enumerated can be expressed in the following manner:

$$l_{w,p,s,inner} = 2\pi(r_c + 2r_w + \frac{1}{2}d_w) \tag{4.45}$$

$$l_{w,p,s,outer} = 2\pi(r_c + 6r_w + \frac{5}{2}d_w) + 2dl \tag{4.46}$$

$$r_{3,inner} = r_c + 6r_w + \frac{5}{2}d_w \tag{4.47}$$

From equation (4.20), the peak current can be computed as:

$$I_m = 2r_w H_m \tag{4.48}$$

Substituting it in the expression of the total energy stored in the leakage flux, it results:

$$W_{lk,tot} = \frac{1}{2} L I_m^2 = 2L H_m^2 r_w^2 \tag{4.49}$$

in which $W_{lk,tot}$ is the sum of the two contributes presented in (4.43) and (4.44). The peak of leakage inductance current appears in buck mode (with 270 [V] output voltage and 10 [A] of dc output current) and it's equal to 20.06 [A]. With this value, the core radius and cross section area values of the core as a function of the number of turns, it's possible to plot the trend of the leakage inductance:

$$L = \frac{W_{lk,tot}}{2H_m^2 r_w^2} \tag{4.50}$$

as it has been done in plot 4.15; observing this trend, it appears that an additional lateral space of 21 [mm] is required. Remembering that the transformer designed has to ensure also a small occupied volume, looking at the data sheets of Ferroxcube, the biggest transformer that can be chosen in order to match the hole inside the charger is the PQ5050, which has a winding area with a lateral width of 22 [mm], hence not enough to put the additional space and also the four winding layers, each one with a thickness of about 1.5 [mm]. In all the Matlab computation made previously to get the surface and the 2-D plots, the clearance dw between each layer has been put equal to 0.4 [mm], this choice

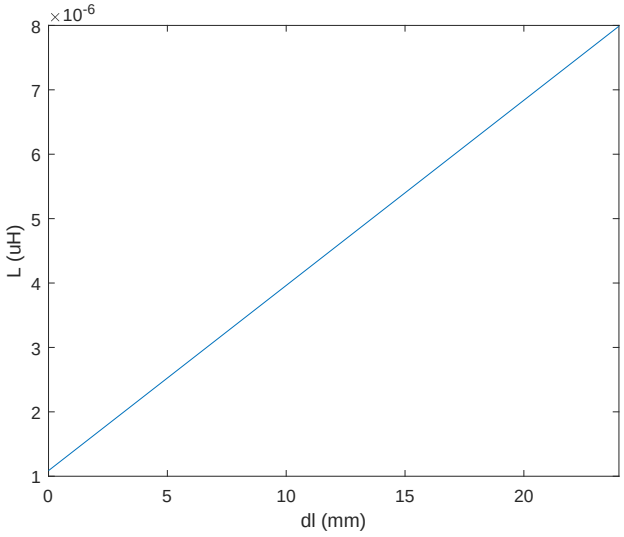


Figure 4.15: Module of the leakage inductance as a function of the space between layers.

reflects the impossibility to make the bobbins wrapped very tight by hand.

4.4.1 Not interleaved configurations

Since the vertical interleaved configuration discussed is not suited, remembering that the core losses reach their minimum value at a temperature around 80-90 [°C], not interleaved configurations have been explored.
As stated before, an important design parameter is the so called "performance factor", because it allows to identify the material that lets to use the smallest core volume (the highest power density) to transmit the desired power. This parameter is related to the apparent power of the transformer and hence to the total power lost. To understand this relationship, a brief analytical path is described hereinafter. Starting from Faraday's equation (4.1), it's possible to make the integration of the derivative flux density term between zero and it's maximum value B_m and average the results in that time interval:

$$< v >= \frac{1}{\tau}\int_0^{\tau} NA_e\frac{dB}{dt}dt = \frac{1}{\tau}NB_mA_e \tag{4.51}$$

Through this average value, the form factor, defined as the ratio between the rms value and the average value, can be computed: $k = \frac{v_{rms}}{<v>}$. It has to be outlined that the rms value of a square wave, like those ones applied in the input and output ports of the transformer, is equal to its maximum value.
Substituting the expression of the average voltage, the root mean square value results:

$$v_{rms} = k < v >= \frac{kT}{\tau}fNB_mA_e = KfNB_mA_e \tag{4.52}$$

The K factor, also called "waveform factor", in the case of square waveform is equal to 4. The total apparent power managed by the transformer is equal to the sum of the two contributes related to both windings:

$$S = \sum_{x=1}^{2} V_xI_x = KfB_mA_e\sum_{x=1}^{2} N_xI_x \tag{4.53}$$

Considering the nominal working condition, which transformer current is shown in fig. 4.12, the rms value can be expressed also like the product between the current density J and the cross section area of the wire A_{wire} (in the case of 450 parallel strand with a diameter of 0.05 [μm] it's equal to 0.883 [mm^2]). Defining the ratio between the area of the two bobbins with the winding area of the transformer as:

$$k_u = \frac{2NA_{wire}}{A_{winding}} \tag{4.54}$$

the apparent power equation becomes:

$$S = \sum_{x=1}^{2} V_x I_x = KfB_m A_e J k_u A_{winding} \tag{4.55}$$

Taking in mind the expression of the medium winding length (4.17) (also called l_w), the copper losses can be expressed as:

$$P_{cu} = \rho J^2 l_w A_{winding} k_u \tag{4.56}$$

$$= \rho V_{winding} k_u J^2 \tag{4.57}$$

where $V_{winding}$ is the volume of the winding window and multiplying it by k_u it's possible to get the conduction volume.
Furthermore the copper losses can be expressed as a function of the frequency and of the magnetic flux density, substituting J with the related terms that appear in (4.55):

$$P_{cu} = \rho V_{winding} k_u \left[\frac{\sum_{x=1}^{2} V_x I_x}{KfB_m k_u A_e A_{winding}} \right]^2 \tag{4.58}$$

On the other hand, the core losses can be computed in an approximate way without using the plot of the specific power lost that can be found in the data sheet of the core, but through the following analytical equation:

$$P_{kernel} = \rho_k V_k K_k f^{\alpha} B_m^{\beta} \tag{4.59}$$

in which:

- ρ_k is the mass density of the ferrite (4800 [kg/m^3]);
- V_k is the kernel volume;
- K_k, α and β are constants of the specific material; in particular for Mn-Zn ferrite their values are respectively $1.9{\cdot}10^{-3}$, 1.24 and 2.

Summing the kernel and the copper losses and making the sum varying as a function of the frequency and the flux density, the surface plot shown in fig. 4.16 is got. The most important meaning of this plot is that, as the frequency goes up, to ensure thermal stability, the magnetic flux density B has to decrease, otherwise the core losses will diverge. For this reason choosing a material that presents a big value of the "performance factor" $f{\cdot}B$ is important, because it means that with that kind of ferrite a bigger flux density B can occur without bringing instability in the transformer. The magnetic flux density becomes high when the number of turns is small, furthermore it will be seen that non interleaved winding layers will emphasize the drawbacks linked to proximity effect.

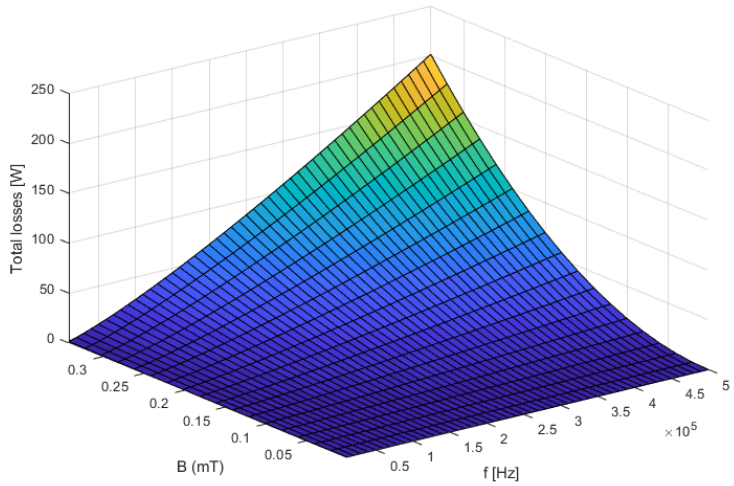


Figure 4.16: Total power losses trend varying the frequency and the flux density.

4.4.2 Concentric bobbins inside a PQ4040 core

The first assumption made in this design step has been the acceptable flux density peak: since the two windings don't create a symmetric structure, the maximum ΔB is not more linked to the peak to peak values, but only to positive maximum value. Wishing to design the first transformer as small as possible, a specific power lost P_v in the core equal to 1 [kW/m^3] has been considered and the corresponding peak flux density appears to be around 130 [mT]. This design choice could seem strange, because of the very high specific losses, but it has to be remembered that the core volume is quite small and its stability is good near 100 [°C].

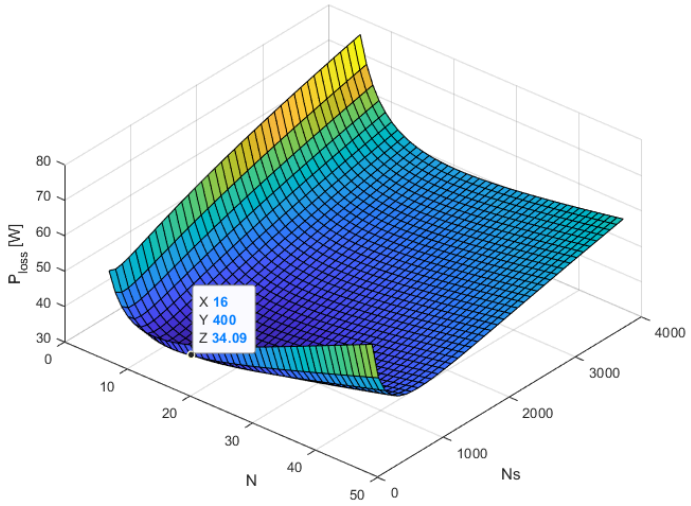


Figure 4.17: Transformer total power losses in the case of asymmetric configuration.

Computing the total losses in the transformer, i.e. eddy current contribute due to proximity effect (4.29), dc power lost (4.35) and core losses (4.37), it appears a surface plot different with respect the symmetric case, as can be seen in fig. 4.17, where it's possible to see that the core losses make the total power lost to be never smaller than 32 [W], with respect the symmetric case in which the transformer power lost could reach a minimum value around 18 [W]. From this computation, wishing to wrap the wires into two concentric vertical bobbins and storing enough leakage flux, a

winding area height at least equal to 27 [mm] has to be searched, since the turns won't never be very enclosed each other.

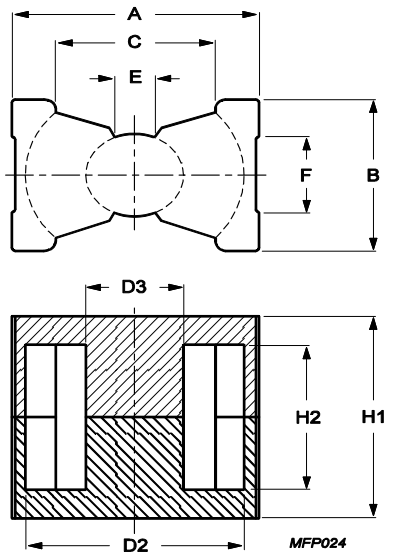


Figure 4.18: Cross section view of PQ 4040 core.

For this reason, looking in Ferroxcube's catalogue, the core PQ4040 has been chosen. Figure 4.18 refers the main characteristic dimensions of this core shape, that are summarized in table 4.1. Filling all the winding area in vertical direction, each winding can be composed of 16 series turns, a quite enough big number that allows to get a big magnetic field strength in the free space between the primary and secondary layers, where the main leakage flux concentrates itself. With this design choice, employing the analytical formulas explained in the previous section, the detailed contributes to total losses can be computed.
First of all, the medium length of each winding has been computed, neglecting the clearance dw since each layer is separated by the insulation thickness:

$$l_{w,inner} = 2\pi(r_c + r_w + c_t) = 54.592\ [mm] \tag{4.60}$$

$$l_{w,outer} = 2\pi(r_c + 3r_w + c_t + i_t) = 104.3987\ [mm] \tag{4.61}$$

where:

Table 4.1: Main dimensions of PQ4040 transformer

Symbol	Parameter	Value	Unit
V_e	effective volume	20500	mm^3
L_e	effective length	102	mm
A_e	effective area	201	mm^2
A	total width	41.5	mm
B	thickness	28	mm
H1	total height	39.8	mm
H2	internal height	29.5	mm
D2	internal width	37	mm
D3	central leg diameter	14.9	mm

- r_c is the radius of the transformer central leg equal to 7.45 mm;
- c_t is the coil former column thickness equal to 0.4 [mm];
- i_t is the insulator thickness corresponding to 6.25 [mm].

The dc resistance of the two windings are equal to:

$$R_{dc,inner} = \frac{\rho N l_{w,inner}}{N_s A_{awg44}} = 0.0218 \ [\Omega] \tag{4.62}$$

$$R_{dc,outer} = \frac{\rho N l_{w,outer}}{N_s A_{awg44}} = 0.0417 \ [\Omega] \tag{4.63}$$

The effective magnetic path length can be approximated through this equation:

$$l'_e = 2(4r_w + r_c + 3\frac{H1 - H2}{4} + 2Nr_w + i_t) = 103.224 \text{ mm} \tag{4.64}$$

Taking in mind these geometric quantities, the several power losses contributes are summarized hereinafter:

$$P_{dc,inner} = I^2_{rms} R_{dc,inner} = 2.887 \ [W] \tag{4.65}$$

$$P_{dc,outer} = I^2_{rms} R_{dc,outer} = 5.521 \ [W] \tag{4.66}$$

$$P_{eddy,inner} = \frac{\mu_o^2 \pi N N_s l_{w,inner} d^4}{768 \rho r_w^2 T} \int_T (\frac{di}{dt})^2 dt = 2.3855 \ [W] \tag{4.67}$$

$$P_{eddy,outer} = \frac{\mu_o^2 \pi N N_s l_{w,outer} d^4}{768 \rho r_w^2 T} \int_T (\frac{di}{dt})^2 dt = 4.5434 \ [W] \tag{4.68}$$

$$P_c = P_v A_e l'_e = 20.748 \ [W] \tag{4.69}$$

$$P_{tot} = P_{dc,inner} + P_{dc,outer} + P_{eddy,inner} + P_{eddy,outer} + P_c = 36.085 \ [W] \tag{4.70}$$

Computation of the series leakage inductance

The hypothesis on which the analytical calculation is based is to consider an infinite value for the permeance outside the cylindrical volume occupied by the windings and the isolation layer, therefore only the flux lines dispersed within the windings and the channel separating them are considered; the flux density lines are parallel to the windings layers. In reality the induction is not null also in the core of the transformer, but since it's value is due to the magnetizing current, it can be considered negligible with respect the value presents in the winding space. The induction B has hence only an axial component and its module relies on the distance from the central leg of the core, as can be seen in plot 4.19. The induction vanishes at the outer edge of each winding and grows linearly up to the inner edge, remaining constant throughout the thickness of the insulating layer, as expressed in the following system:

$$\begin{cases} B(r) = \mu_0 \frac{NI}{h} \frac{r - R_2 + a_2}{a_2} & \text{for } R_2 - a_2 \leq r \leq R_2 \\ B(r) = \mu_0 \frac{NI}{h} & \text{for } R_2 \leq r \leq R_1 \\ B(r) = \mu_0 \frac{NI}{h} \frac{R_1 + a_1 - r}{a_1} & R_1 \leq r \leq R_1 + a_1 \end{cases} \tag{4.71}$$

Stating that $a_2 = a_1 = a$, the differential volume of each winding layer and the isolation layer is given by: $d_{vol} = h \cdot l_w \cdot dx$, in which l_w can assume the meaning of the medium magnetic length of the inner/outer winding layer or the medium length of the hollow cylinder of isolation: the first two quantities have been computed above in (4.60) and (4.61), whereas the last one can be computed taking in mind the average radius between those ones of the two

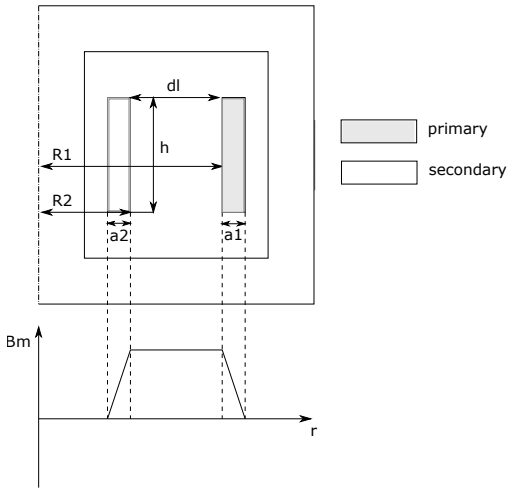


Figure 4.19: Axial component of the flux density in radial position.

windings, as:

$$l_{w,isol} = 2\pi(r_c + 2r_w + c_t + \frac{i_t}{2}) = 79.495\ [mm] \tag{4.72}$$

Referring the magnetic flux density as a function of the magnetic field strength, the total energy can be computed as the sum of the energy stored in each radial layer, as:

$$W_m = \frac{\mu_0}{2}\sum_{x=1}^{3}\int_0^{a_x} H^2 l_{w,x} h dx \tag{4.73}$$

where dx can be shifted to take into account a_1, a_2 or dl; $l_{w,x}$ can assume the value of the two windings or of the isolation layer. The field strength along the magnetic path that includes the windings layers depends on the number of turns that composes each bobbin. For the reason explained above, the energy is computed only in the volume consisting of the two windings and the isolation between them. The magnetic field can be considered linear varying the radial distance from the axis of the core:

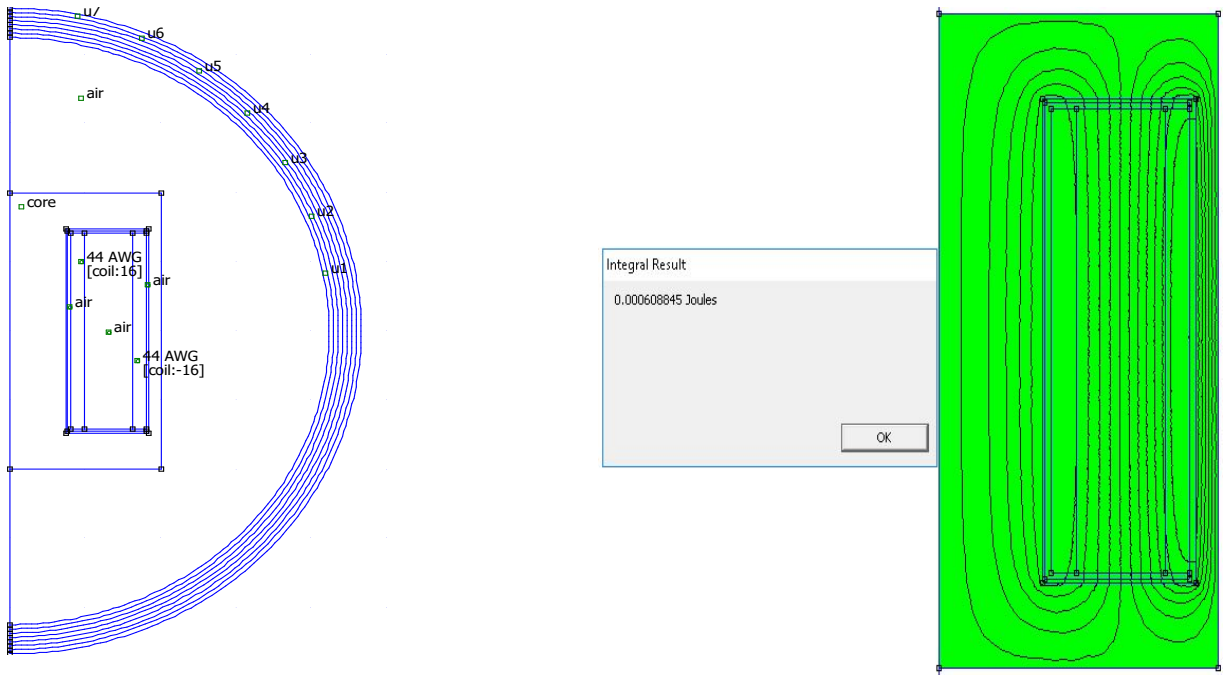
$$H = \frac{I}{h}\frac{x}{a} \tag{4.74}$$

According to (4.73), the total amount of energy stored in the leakage flux can be computed in first approximation through the following equation (remembering that the turn ratio is unitary):

$$W_m = \frac{\mu_0}{2}\left[l_{w,inner} h \int_0^a (\frac{NI}{h}\frac{x}{a})^2 dx + l_{w,isol} h (\frac{NI}{h})^2 dl + l_{w,outer} h \int_0^a (\frac{NI}{h}\frac{x}{a})^2 dx\right] = \frac{1}{2} L I^2 \tag{4.75}$$

in which $dl = i_t$, i.e. the isolation layer thickness. From the above equation it's clear that the value of the leakage inductance is independent from the current; making the computation it results:

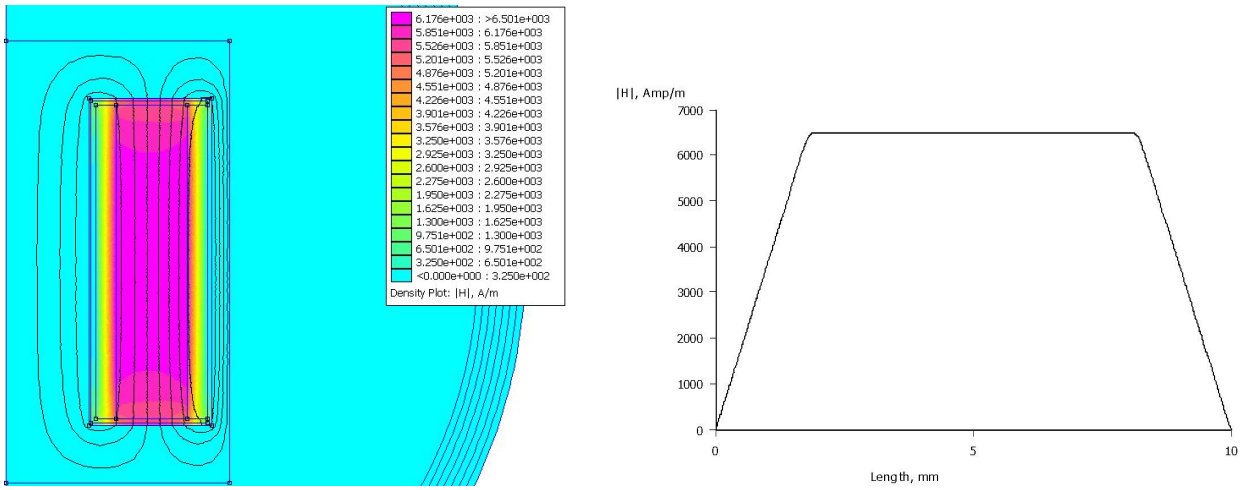
$$L = \frac{\mu_0 N^2}{h}\left[l_{w,inner}\int_0^a (\frac{x}{a})^2 dx + l_{w,isol} dl + l_{w,outer}\int_0^a (\frac{x}{a})^2 dx\right] = 6.734\ [\mu H] \tag{4.76}$$



(a) (b)

Figure 4.20: Magnetic problem simulation of the designed PQ4040 transformer.

In order to verify the analytical computation of the leakage inductance, a FEM simulation has been done. Since the result searched is the magnetic field energy, a magnetic problem solver has been employed in Femm software, at null frequency. In the axisymmetric simulation model the two windings have been modeled as rectangular copper foils, each one excited with 16 turns and a root mean square current of 11.4998 [A], with opposite sign. The coil former and the isolation layer are described as air, since the permeability of plastic is the same like that one of the air. To make the simulation, Dirichlet's boundary condition has been established, in this way the normal component of the flux density at the boundary is null; the copper conductivity is equal to 58 [MS/m] (see fig. 4.20(a)). After running the simulation, the magnetic field energy in all the volume (remembering that the problem is axysimmetric) has been computed, resulting in a value equal to 0.608845 [mJ], as can be observed in picture 4.20(b). Multiplying by 2 the computed energy and then dividing the result by the squared value of the rms current, a leakage inductance equal to 6.85 μH is obtained.



(a) (b)

Figure 4.21: Magnetic field strength in magneto-static simulation.

In fig. 4.21 the surface plot of the magnetic field strength in magneto-static solution is presented, next to the waveform that describe the trend of the field module over the winding width: as stated before, the transformer working mode is asymmetric.

One aspect that has to be outlined is that, with the selected wire (450 parallel strands), the current density at nominal condition is equal to: $J = \frac{I_{rms}}{A_w} = \frac{11.4998}{0.8836} = 13[\text{A/mm}^2]$; this value seems very big, but it has to be remembered that the dc resistance of the litz wire is in the order of milliohms, like computed above. It will be seen in the chapter of results that this high current density isn't a problem in the wire itself, but it becomes very important inside the transformer's bobbins, since the magnetic field strength is very high and the proximity effect will make greater the real resistance with respect the ideal one computed in the dc case.

After all these computations, being sure to get a leakage inductance value in the range of the desired one, the coil former has been designed in SolidEdge, a CAD software made by Siemens.

Afterwards the coil former has been printed with the 3D printer of the laboratory, like shown in photo 4.23(a), and then the wire has been wrapped, as shown in 4.23(b). Once building up the whole transformer, the computation of the main and leakage inductances has been made through a RLC meter, getting the following results:

- $L_{outer} = 659$ [μH] is the primary winding main inductance;

(a) (b)

Figure 4.22: CAD design of the insulator and the total assembly.

(a) (b)

Figure 4.23: 3D printing and construction of the PQ4040 transformer.

- $L_{inner} = 657.8$ [μH] is the secondary winding main inductance;
- $L_k = 6.76$ [μH], this value has been computed measuring the inductance with the secondary winding (inner one) short circuited.

Figure 4.24: Leakage inductance measurement in the PQ4040.

In order to compute the real leakage inductance L, remembering that the transformer turn ratio n is unitary, the following equations system has been solved:

$$\begin{cases} L_m = \sqrt{(L_{outer} - L_k) n^2 L_{inner}} = 655 & [\mu\text{H}] \\ L_1 = L_{outer} - L_m = 3.9859 & [\mu\text{H}] \\ L_2 = L_{inner} - \frac{L_m}{n^2} = 2.7859 & [\mu\text{H}] \\ L = L_1 + L_2 = 6.7718 & [\mu\text{H}] \end{cases} \tag{4.77}$$

where:

- L_m is the magnetizing inductance;
- L_1 is the leakage inductance of the primary winding;
- L_2 is the leakage inductance of the secondary winding;
- L represents the total leakage inductance referred to the primary side of the transformer.

For this transformer and also the following the working condition will be analysed in a separated chapter.

4.4.3 Horizontal winding design in PQ5050 transformer

Since in the previous transformer it is believed that the current density is too high and can cause high losses due to the proximity effect, a bigger core has been taken into account, i.e. the PQ5050 always made by 3F36 material by Ferroxcube.

Table 4.2: Main dimensions of PQ5050 transformer.

Symbol	Parameter	Value	Unit
V_e	effective volume	37100	mm^3
L_e	effective length	113	mm
A_e	effective area	328	mm^2
A	total width	51	mm
B	thickness	32	mm
H1	total height	50	mm
H2	internal height	36.1	mm
D2	internal width	44	mm
D3	central leg diameter	20	mm

Remembering the cross section view of the PQ core 4.18, in table 4.2 the main quantities have been summarized. In such transformer, in order to make a design involved in decreasing the current density, the litz wire AWG 44 with 2250 parallel strands has been used; since it's bigger, a different winding horizontal design has been followed.
Adopting the aforementioned wire, the current density in nominal condition results equal to: $J = \frac{I_{rms}}{A_w} = \frac{11.4998}{4.4179} = 2.6$ [A/mm^2]. In this design the copper losses are expected to be small, but since the wire requires big space and the requirement of the leakage inductance has to be satisfied, the number of turns will be small and this fact will translate in big core losses. Imaging to build up 9 turns for each winding, divided into three layers and interleaved by means of two insulator rings, the total losses can be computed with precision, substituting to expressions depending on the number of turns and strands, the core parameters which are reported into table 4.2.
First of all, the medium turn length and the medium magnetic path are computed as:

$$l_w = 2\pi(r_c + 3r_w + d_w) = 100.06\ [mm] \tag{4.78}$$

$$l'_e = 2(6r_w + r_c + 3\frac{A - D2}{4} + 12r_w + 2i_t + 2d_w) = 120\ [mm] \tag{4.79}$$

where:

- $d_w = 0.3$ [mm] is the clearance between each turn;
- $i_t = 6.2$ [mm] is the thickness of the isolation rings.

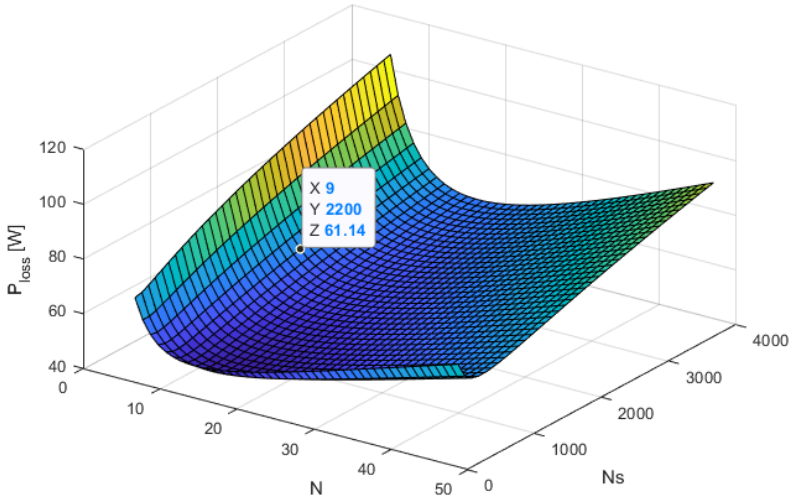


Figure 4.25: Total power losses in asymmetric PQ5050 transformer.

With the effective area, the flux and the number of turns, exploiting the Faraday's law, the variation of the flux density results:

$$\Delta B = \frac{VDT}{A_e N} = 125\ [mT] \tag{4.80}$$

to which a specific power of 1 [kW/m^3] corresponds, as supposed also for the computation of the surface plot 4.25, since the transformer is asymmetric. As the two windings are spread all over the winding area width, they have the same medium length and hence the same dc resistance:

$$R_{dc,p,s} = \frac{\rho N l_w}{N_s A_{awg44}} = 0.0045\ [\Omega] \tag{4.81}$$

The different power lost contributions are equal to (in this case $H = \frac{i(t)}{r_w}$):

$$P_{dc,p,s} = I_{rms}^2 R_{dc,p,s} = 0.6040\ [W] \tag{4.82}$$

$$P_{eddy,p,s} = \frac{\mu_o^2 \pi N N_s l_w d^4}{192 \rho r_w^2 T} \int_T (\frac{di}{dt})^2 dt = 9.8958\ [W] \tag{4.83}$$

$$P_c = P_v A_e l_e' = 40.4413\ [W] \tag{4.84}$$

$$P_{tot} = 2(P_{dc,p,s} + P_{eddy,p,s}) + P_c = 61.44\ [W] \tag{4.85}$$

Computation of the series leakage inductance

The winding layout chosen consists of 9 turns for both primary and secondary winding, with 3 turns for each layer; the last one has been regarded as a rectangular conducting foil in the schematic view 4.26. As can be seen in that picture, in order to store enough leakage flux in correspondence of the two insulator rings, not interleaved structure has been chosen: in this way the current density arises cause of the proximity effect that becomes big, but it allows to get the desired leakage inductance, as it will be demonstrated hereinafter. Starting from the top side of the picture, the layers distribution is: primary, primary, isolation, secondary, primary, isolation, secondary, secondary. Once again the energy stored in the leakage flux can be computed exploiting equation (4.73); the infinitesimal volume of the winding layers can be computed as $d_{vol,w} = h l_w dx$ and that one of each isolation ring as $d_{vol,r} = h l_w dr$. Defining N_l as the

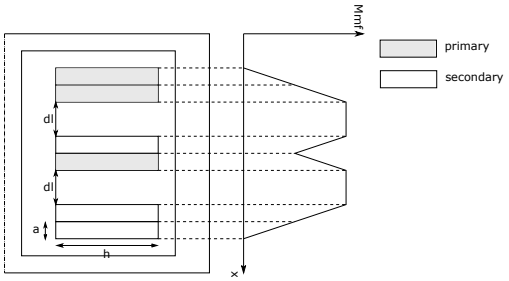
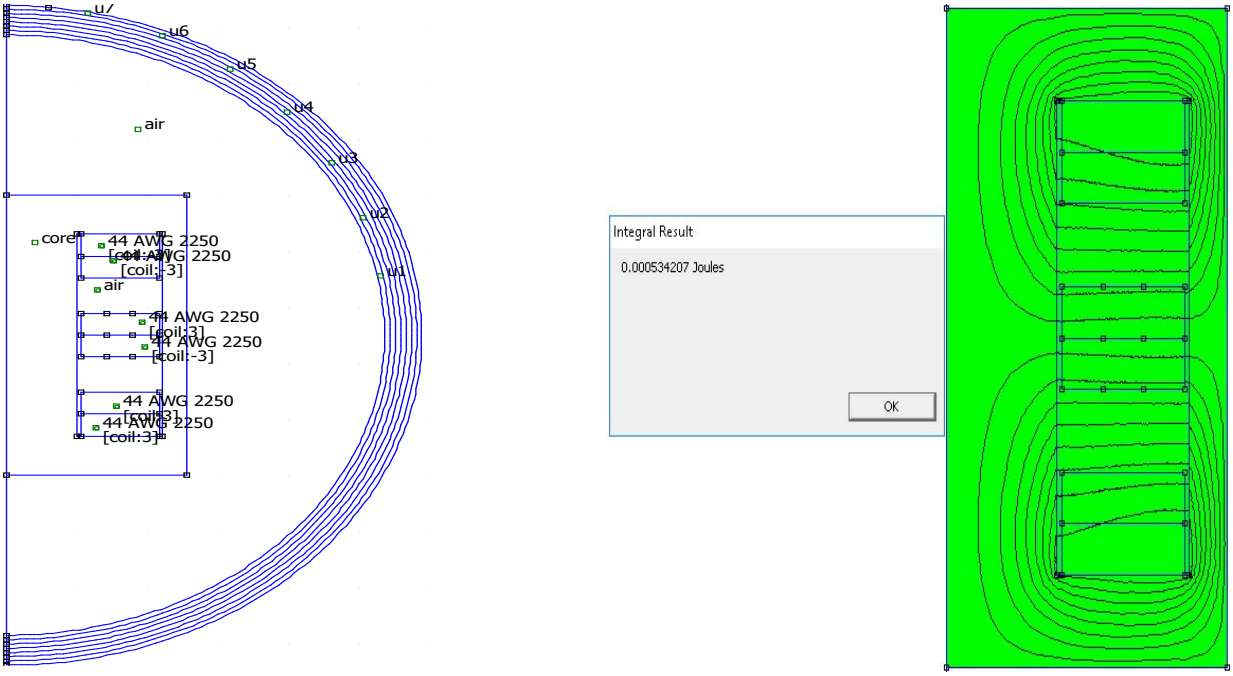


Figure 4.26: Radial component of the magneto motive force in axial position.



(a) (b)

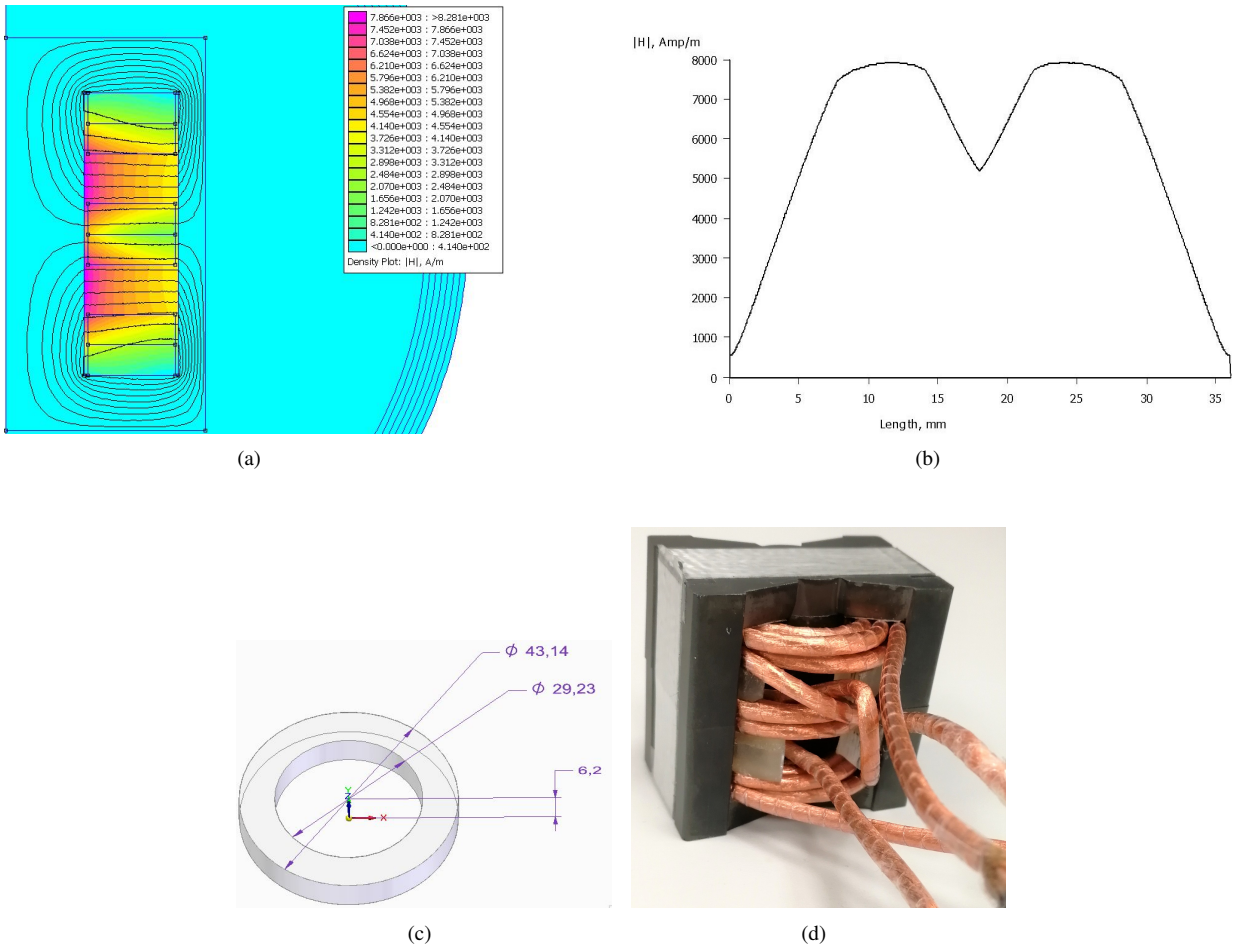
Figure 4.27: Magnetic problem simulation of the designed PQ5050 transformer.

number of turns for each layer (three in this case), the total energy can be computed as the area under the magneto motive force plot in fig. 4.26:

$$W_m = \frac{\mu_0}{2} l_w h \Big[6 \int_0^a \Big(\frac{N_l I_{rms}}{h} \frac{x}{a} \Big)^2 dx + 4a \Big(\frac{N_l I_{rms}}{h} \Big)^2 + 2dl \Big(\frac{2N_l I_{rms}}{h} \Big)^2 \Big] = \frac{1}{2} L I_{rms}^2 \tag{4.86}$$

where $dl = i_t$, i.e. the isolation thickness. Solving the above equation, the leakage inductance results: $L = 7.2023$ [μH]. Once again, in order to verify the analytical computation, a FEM simulation has been done: the layer has been drawn like rectangular copper foil with 3 turns for each one, as it's shown in picture 4.27(a). Multiplying by two the magnetic energy of 0.5342 [mJ] and dividing the result by the square of the rms current, a leakage inductance value around 8 [μH] is got.

By the way of completion, the graph of the spatial distribution of the magnetic field (fig. 4.28(a)) and its radial distribution (plot 4.28(b)) have been reported in this thesis. As can be seen from the surface plot of the magnetic field, its magnitude is bigger with respect the case of the vertical arrangement in the PQ4040 transformer since the magnetic path length is shorter; this fact will translate in worst proximity effect, although the current density is quite small.



(a) (b)

(c) (d)

Figure 4.28: Designed PQ5050 transformer.

For what concern the construction of this transformer, two insulator rings have been designed and printed (fig. 4.28(c)) and the whole transformer is reported in picture 4.28(d). Once again, the inductances have been computed by means of the RLC meter and their values are summarized hereinafter:

- $L_{primary} = 295.6$ [μH];
- $L_{secondary} = 295.5$ [μH];
- $L_k = 7.320$ [μH] is the value obtained with the secondary winding short circuited.

As done in the first designed transformer, the real value of the leakage inductance has been computed solving the following system:

$$\begin{cases} L_m = \sqrt{(L_{primary} - L_k) n^2 L_{secondary}} = 291.86 & [\mu\text{H}] \\ L_1 = L_{primary} - L_m = 3.7369 & [\mu\text{H}] \\ L_2 = L_{secondary} - \frac{L_m}{n^2} = 3.6369 & [\mu\text{H}] \\ L = L_1 + L_2 = 7.3738 & [\mu\text{H}] \end{cases} \tag{4.87}$$

in which the several parameters have the same meaning as in the case of the PQ4040 transformer. The working conditions will be described in a separated chapter.

4.4.4 Symmetric not interleaved transformer

The last transformer that has been designed arises from the necessity of both decreasing the core losses (hence increasing the number of windings turns) and meanwhile maintaining the current density inside an acceptable range, with always the restriction of the minimum stored leakage flux. Since the available litz wires belong to two opposite sides, it has been decided to take the smallest one, put two wires in parallel and twist them (as described before, creating closed loop with parallel wires, in order to compensate the induced voltages, along the length of the loop, the wires have to be transposed). In this way the total number of strands results equal to 900 and hence the current density is the half as in the case of the first designed transformer, i.e. $J = \frac{I_{rms}}{A_w} = \frac{11.4998}{1.77} = 6.49$ [A/mm^2]. However it has to be highlighted that this design idea is not one of the best, since the twisted bare wires require much more space than a single wire with the same number of strands, furthermore the twisting pitch won't never be as tight as that one between each strand, so the induced voltages compensation is a little bit coarse, translating in bigger eddy currents and so in bigger winding losses with respect those ones that could be obtained in a single litz wire with the same number of strands. Since the idea is just to put more turns inside the PQ5050 transformer (12 turns), without changing their layout disposition and making the operation mode symmetric, the average magnetic and winding path length remains the same as those ones computed in the previous designed PQ5050, referenced below:

$$l_w = 2\pi(r_c + 3r_w + d_w) = 100.06\ [mm] \tag{4.88}$$

$$l'_e = 2(6r_w + r_c + 3\frac{A - D2}{4} + 16r_w + 2i_t + 2d_w) = 120\ [mm] \tag{4.89}$$

where the isolation thickness i_t is around 5 [mm].

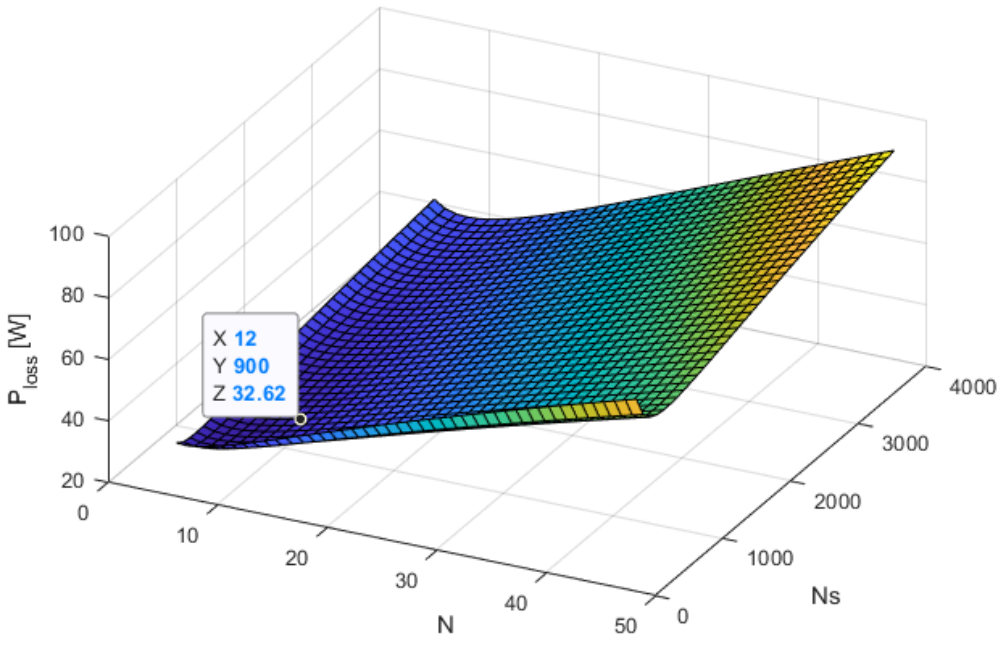


Figure 4.29: Total power losses as a function of the number of strands and turns in the PQ5050 symmetric transformer.

With the effective area, the flux and the desired number of turns, through Faraday's law, the maximum variation of the flux density is equal to:

$$\Delta B = \frac{VDT}{A_e N} = \frac{370}{328{\cdot}12} = 94\ [mT] \tag{4.90}$$

Since the working condition is symmetric, the peak flux density value is quite small: $\widehat{B} = \frac{\Delta B}{2} = 47$ [mT], to which a specific power lost of about 180 [kW/m^3] corresponds. The first important aspect that can be observed looking at the surface plot 4.29 is that the total power lost (computed taking in mind the geometry of the core reported in table 4.2) is decreased a lot with respect that one resulted in the case of asymmetric PQ5050 transformer.
The dc resistance at 90 [°C] of each winding is:

$$R_{dc,p,s} = \frac{\rho N l_w}{N_s A_{awg44}} = 0.0142 \ [\Omega] \tag{4.91}$$

Using all the above computed parameters, the various power lost contributes are ($H = \frac{i(t)}{r_w}$):

$$P_{dc,p,s} = I_{rms}^2 R_{dc,p,s} = 1.7539 \ [W] \tag{4.92}$$

$$P_{eddy,p,s} = \frac{\mu_o^2 \pi N N_s l_w d^4}{192 \rho r_w^2 T} \int_T (\frac{di}{dt})^2 dt = 11.4949 \ [W] \tag{4.93}$$

$$P_c = P_v A_e l'_e = 6.1176 \ [W] \tag{4.94}$$

$$P_{tot} = 2(P_{dc,p,s} + P_{eddy,p,s}) + P_c = 32.6153 \ [W] \tag{4.95}$$

Computation of the series leakage inductance

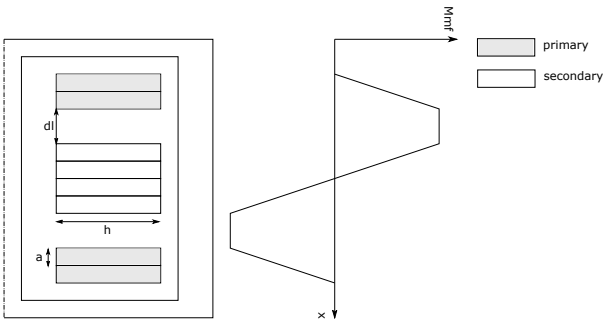


Figure 4.30: Radial component of the magneto motive force in axial position.

The winding layout chosen consists of 12 turns for each winding, primary and secondary, arranged as shown in picture 4.30, where the grey rectangles represent the primary winding layers. As it can be seen, the working waveform is symmetric with respect the "x" axis, in this way the core losses are supposed to be small with respect the previous two configurations described above; starting from the top side of the schematic, the layers distribution is: two times primary, isolation, four times secondary, isolation, two times primary.
Once again the energy stored in the leakage flux can be computed exploiting equation (4.73); the infinitesimal volume of the winding layer can be computed in the same way explained in the case of the asymmetric PQ5050 transformer. Remembering that N_l is the number of turns for each layer (three in this case), the total energy can be computed as the module of the area under the magneto motive force plot in fig. 4.30:

$$W_m = \frac{\mu_0}{2} l_w h \big[8 \int_0^a (\frac{N_l I_{rms}}{h} \frac{x}{a})^2 dx + 4a(\frac{N_l I_{rms}}{h})^2 + 2dl(\frac{2N_l I_{rms}}{h})^2 \big] = \frac{1}{2} L I_{rms}^2 \tag{4.96}$$

in which d_l represents the thickness of each isolation layer, equal to about 5 [mm]. Solving the above equation, the leakage inductance results: $L = 7.23$ [μH]. As done in the previous designs, a FEM magneto-static simulation has been done in order to check the analytical computation of the desired leakage inductance. Looking at the schematic drawn in fig. 4.31, an energy equal to 0.485 [mJ] is obtained; multiplying this value by two and dividing the result by

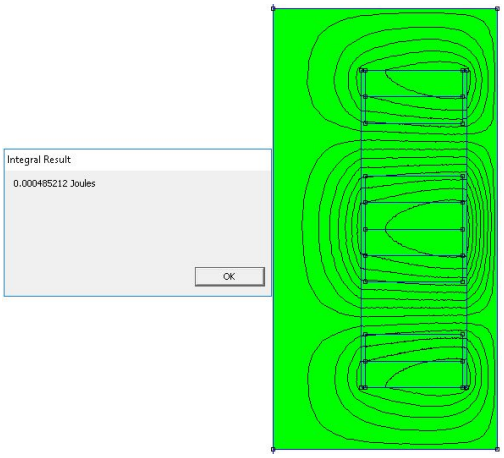
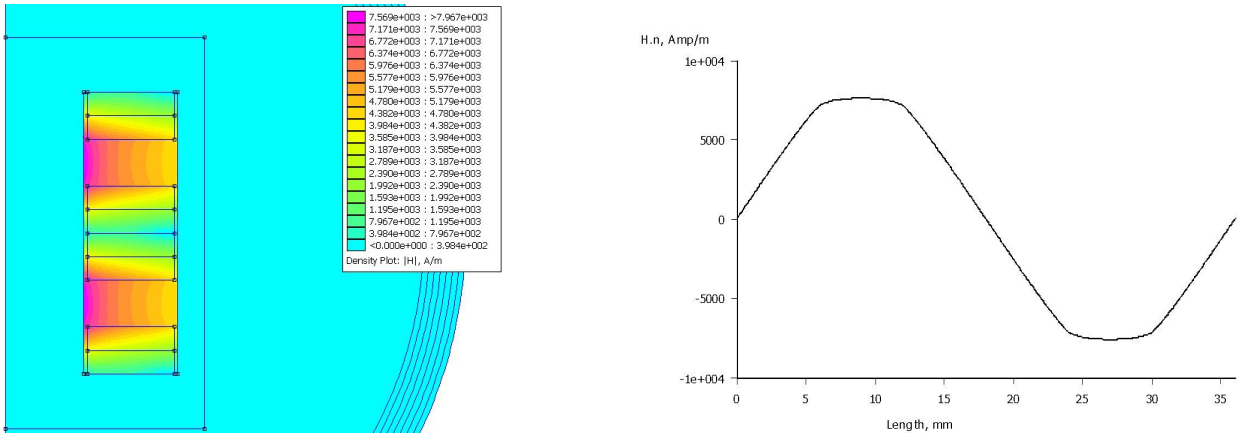


Figure 4.31: FEM computation of the magnetic energy in the symmetric transformer.



(a) (b)

Figure 4.32: Magnetic field strength in magneto-static simulation in the case of symmetric design.

the square of the rms current, the searched parameter becomes: $L = 7.33$ [μH]. Furthermore, the density plot of the module of the magnetic field strength (picture 4.32(a)) and the trend of the normal component of H field (fig. 4.32(b)) have been reported; as can be seen, along the total height of the transformer, the normal component of the magnetic field is now alternate and this allows to decrease the core losses. However, the analytical power lost computed won't match with real power lost, because although the core losses are small, the proximity effect in the not interleaved 4 secondary layers will be big, also if the magnetic field is changing its direction.

"Strong" of these matches for what concern the computation of the leakage inductance, the transformer has been built up and the result is shown in picture 4.33. After this step, the computation of the mains inductances has been performed by means the RLC meter, obtaining:

- $L_{primary} = 497.1$ [μH];
- $L_{secondary} = 497$ [μH];
- $L_k = 7.018$ [μH] is the value obtained with the secondary winding short circuited.

Wishing to find the most exact value of the leakage inductance, starting from the above measurements, the system

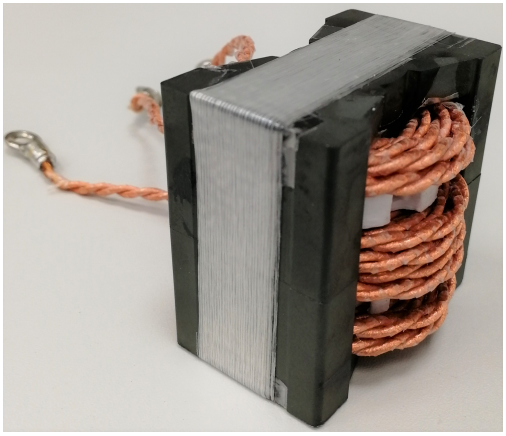


Figure 4.33: Symmetric built up transformer.

Table 4.3: Leakage inductances and different power losses in the three designed transformers.

	PQ4040	PQ5050 asymmetric	PQ5050 symmetric
L	6.7718 [μH]	7.3738 [μH]	7.0422 [μH]
P_{dc}	8.408 [W]	1.208 [W]	3.5078 [W]
P_{eddy}	6.9289 [W]	19.7916 [W]	22.9898 [W]
P_{core}	20.748 [W]	40.4413 [W]	6.1176 [W]
P_{tot}	36.085 [W]	61.44 [W]	32.6153 [W]

below has been solved:

$$\begin{cases} L_m = \sqrt{(L_{primary} - L_k) n^2 L_{secondary}} = 493.53 & [\mu\text{H}] \\ L_1 = L_{primary} - L_m = 3.5711 & [\mu\text{H}] \\ L_2 = L_{secondary} - \frac{L_m}{n^2} = 3.4711 & [\mu\text{H}] \\ L = L_1 + L_2 = 7.0422 & [\mu\text{H}] \end{cases} \tag{4.97}$$

For the sake of clarity in table 4.3 the main parameters of the different transformers are summarized. As it can be understood, the symmetric configuration allows to decrease a lot the core losses.

5 Small signal model and control loops

There are two main ways to control a system: the first one is the open loop control instead the second one is the close one. If on one hand the open loop is easier to implement and cheaper, since no sensors are needed, on the other hand this kind of control can cause instability because there aren't feedbacks about the status of the system. In this thesis a closed loop scheme has been implemented since it's impossible to have a complete knowledge of the real system. In this chapter a simplified small signal model of the dual active bridge is derived and used to compute the ranges of the gains that have to be applied in the controller; however it will be explained that these parameters can't be directly used in the real system, because delays introduced by microcontroller, sensors, ADC converters and all other electronic devices aren't taken into account and they influence the behaviour of the real system, as it will be documented hereinafter.

5.1 Small signal model

In order to describe a physical converter two paths can be followed: the averaged model and the small signal model. Both of theme are finalized to describe a system, that in the time domain is represented through differential equations, by means of algebraic equations in the Laplace domain. In this thesis, the small signal model presented in [21] has been employed in order to get a description of the real system in the frequency domain. In the chapter about the dual active bridge, the expression of the transmitted power has been derived and it's reminded below:

$$P_o = \frac{v_o(1-|d|)dT_{hf}v_i}{nL} \tag{5.1}$$

Also the expressions of the average input and output bridges currents have been derived and reported below:

$$I_2 = \frac{(1-|d|)dT_{hf}v_i}{nL} \tag{5.2}$$

$$I_{i,avg} = \frac{(1-|d|)dT_{hf}v_o}{nL} \tag{5.3}$$

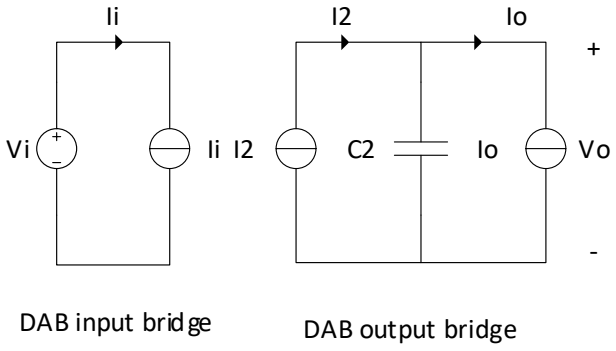


Figure 5.1: Average model of the DAB.

and looking at the average model in fig. 5.1, they are called respectively I_2 and I_i. The main goal of the small signal model is to describe the system behaviour in presence of some perturbations in the parameters that don't remain constant during the working state. Applying this concept, the above average currents can be perturbed around their equilibrium values, as shown below:

$$i_{i,avg} = I_{i,avg} + \widehat{i_{i,avg}} \tag{5.4}$$

$$i_2 = I_2 + \widehat{i_2} \tag{5.5}$$

in which the right side quantities of both equations state the perturbations around the equilibrium point E_q, defined as:

$$\widehat{i_{i,avg}} = \frac{\partial i_{i,avg}}{\partial d}|_{E_q} \cdot \widehat{d} + \frac{\partial i_{i,avg}}{\partial v_o}|_{E_q} \cdot \widehat{v_o} \tag{5.6}$$

$$\widehat{i_2} = \frac{\partial i_2}{\partial d}|_{E_q} \cdot \widehat{d} + \frac{\partial i_2}{\partial v_i}|_{E_q} \cdot \widehat{v_i} \tag{5.7}$$

Computing the partial derivatives, substituting the half switching period with the switching frequency f_{sw} and remembering that the turn ratio is unitary, the following terms are got:

$$F_1 = \frac{\partial i_{i,avg}}{\partial d}|_{E_q} = \frac{(1-2|d|)v_o}{2f_{sw}L} \tag{5.8}$$

$$F_2 = \frac{\partial i_{i,avg}}{\partial v_o}|_{E_q} = \frac{(1-|d|)d}{2f_{sw}L} \tag{5.9}$$

$$F_3 = \frac{\partial i_2}{\partial d}|_{E_q} = \frac{(1-2|d|)v_i}{2f_{sw}L} \tag{5.10}$$

$$F_4 = \frac{\partial i_2}{\partial v_i}|_{E_q} = \frac{(1-|d|)d}{2f_{sw}L} \tag{5.11}$$

Therefore, the expressions (5.6) and (5.7) are defined as:

$$\widehat{i_{i,avg}} = F_1 \cdot \widehat{d} + F_2 \cdot \widehat{v_o} \tag{5.12}$$

$$\widehat{i_2} = F_3 \cdot \widehat{d} + F_4 \cdot \widehat{v_i} \tag{5.13}$$

To explicit the small signal model, some shrewdnesses have to be accounted:

- the independent voltage sources are grounded;
- the independent current sources are opened;
- passive components like resistors and capacitances remain the same.

Downstream the above computation it appears that the perturbation of $i_{i,avg}$ can be computed as the superimposition of two parallel current sources, i.e. $F_1\widehat{d}$ and $F_2\widehat{v_o}$, whereas that one regard i_2 is described as the sum of the two contributes given by the current sources $F_3\widehat{d}$ and $F_4\widehat{v_i}$. Taking in mind that the DC voltage at the input bridge is "supported" by a big capacitor bank, its perturbation can be neglected: this allows to rewrite the currents equation (5.12) and (5.13) in the following simplified manner:

$$\widehat{i_{i,avg}} = F_1 \cdot \widehat{d} + F_2 \cdot \widehat{v_o} \tag{5.14}$$

$$\widehat{i_2} = F_3 \cdot \widehat{d} \tag{5.15}$$

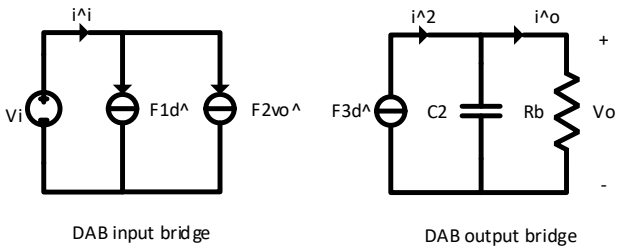


Figure 5.2: Simplified small signal circuit.

and finally, the alternated current that flows inside the smoothing capacitance C_2 is calculated as:

$$C_2 \frac{d\widehat{v_o}}{dt} = \widehat{i_2} - \widehat{i_{o,avg}} \tag{5.16}$$

Since the battery is approximated like a controlled voltage source and a series resistance, the perturbation across its terminals voltage can be considered as the effect of a small variation in the output average current that flows through the internal resistance, as drawn in picture 5.2.
The next step is to build up the control loops. Taking in mind the charging path of the battery, two main techniques arise: the first one is directed to control the current (during the first step of the charging path) and the second one to control the voltage (during the last step of the process); the constant power control is neglected because to make it a real battery simulator should be implemented in the model together the charger, but it would create very long simulations since the time ranges are very different.

5.2 Current control loop

The first control loop implemented in Simulink is that one regarding the current control. Looking at the equivalent second bridge circuit in picture 5.2, from equation (5.16), the small signal output current corresponds to:

$$\widehat{i_{o,avg}} = \widehat{i_2} - C_2 \frac{d\widehat{v_o}}{dt} \tag{5.17}$$

Remembering the expression of $\widehat{i_2}$ and that $\widehat{v_o} = R_b \widehat{i_{o,avg}}$ the aforementioned equation is solved in the time domain as:

$$\widehat{i_{o,avg}} + C_2 R_b \frac{d\widehat{i_{o,avg}}}{dt} = F_3 \widehat{d} \tag{5.18}$$

Shifting it to the Laplace domain, the transfer function that relates the perturbation in the battery output current with that one in the phase shift is:

$$T(s) = \frac{\widehat{i_{o,avg}}}{\widehat{d}} = \frac{F_3}{1 + sC_2R_b} = \frac{(1 - 2|d|)v_i}{2f_{sw}L} \frac{1}{1 + sC_2R_b} \tag{5.19}$$

The system is linearized by means the above transfer function, around an equilibrium point: in the case of the constant current step, the following equilibrium conditions have been considered:

- battery voltage $v_o = 320$ [V], i.e. the middle value in the range of 270-370 [V];
- output average current $i_{o,avg} = 10$ [A];

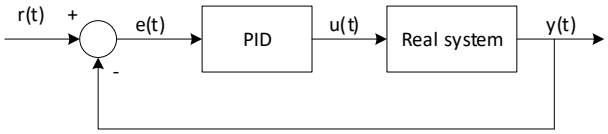


Figure 5.3: Feedback control loop of a real system.

- output power around 3.2 [kW];
- phase shift around 0.27;
- input bridge DC voltage $v_i = 400$ [V].

Substituting the design parameters values inside the transfer function $T(s)$ the result is:

$$T(s) = \frac{25.555}{1 + s0.0000768} \tag{5.20}$$

The s-domain equation is already in an irreducible form. The most common technique used in industrial world to control real systems is the PID control. The acronym summarizes the three different actions that the controller does in the error ($e(t)$ in the time domain and $e(s)$ in the s-domain):

- proportional;
- integrative;
- derivative.

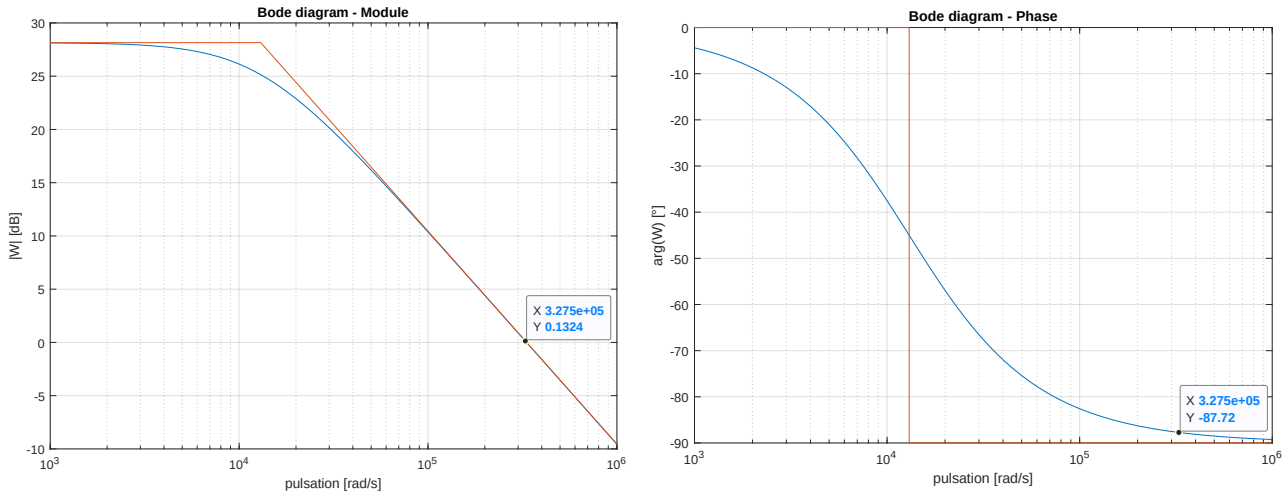
It's possible to give a simple representation of a closed control loop through the flow chart plotted in fig. 5.3, in which:

- $r(t)$ is the desired reference signal to get at the output port;
- $e(t)$ is the error due to the difference between the reference and the measured value;
- $u(t)$ is the control signal, the result of the PID controller action;
- $y(t)$ is the exit signal of the controlled system.

The control law that links the error to the control signal, applied by the PID controller, in the time domain is:

$$u(t) = K_p e(t) + K_i \int_{t_o}^{t} e(\tau) d\tau + K_d \frac{de(t)}{dt} \tag{5.21}$$

where K_p, K_i and K_d are the proportional, integrative and derivative gains. From the above equation it's clear that the control signal is the sum of the three actions applied by the controller on the error signal. Since the controlled system is of first type, with a simple proportional action it's not possible to get a zero steady state error at the output port, furthermore increasing a lot the proportional gain in order to make the steady state error smaller would cause a very fast answer that could go against the physical inertia of the real system. In this thesis job the PI version has been employed because the derivative action, that damps the oscillations of the step answer, if some noise appears would emphasize it and create instability of the system. For what concern the PI controller, the proportional part does not modify the map of the zeros and poles of the open loop transfer function, but simply translates the module diagram vertically and leaves the phase diagram unchanged; the integrative action is necessary in order that the charger follows the set current reference. Overall, at low frequency the regulator will perform a mainly integrative action whereas at



(a) (b)

Figure 5.4: Module and phase Bode diagrams of the open loop transfer function.

high frequencies it will behave like a normal P type controller.
The first step to design the desired PI controller is to study the frequency response of the system in open loop condition by means Bode diagrams (the leakage inductance has been considered equal to 7.2 [μH] in order to match both the two PQ5050 transformers inductance values). In picture 5.4(a) the module plot of the direct transfer function is drawn: it's possible to see that the module (in decibel) doesn't go to infinite near zero frequency and the cross pulsation ω_c is 330 [krad/s]. Besides there is the phase diagram 5.4(b), in which it's possible to see that at the cross pulsation the phase is equal to about -88°, it means a phase margin of 92°. Considering the dynamic behaviour of the battery, it's not necessary such a fast response and so the cross pulsation of the closed loop system can be smaller, instead the phase margin is desired to be 95°. The PI(s) transfer function is:

$$PI(s) = K_i \frac{1 + s\tau_r}{s} \tag{5.22}$$

in which $\tau_r = \frac{K_p}{K_i}$ is the time constant of the controller: if this value is too small, the step answer of the system can present big oscillations around the reference value and the system saturation can be easily reached. The cross pulsation ω_c is chosen equal to 9000 [rad/s] and the open loop transfer function, including also the PI controller, becomes:

$$T(s)_{OL} = K_i \frac{1 + s\tau_r}{s} \frac{25.555}{1 + s0.000078} \tag{5.23}$$

The value of the constant time can be computed imposing the desired phase margin, as shown below:

$$95° = tan^{-1}(\omega_c \tau_r) + 90° - tan^{-1}(\omega_c 0.000078) \tag{5.24}$$

Solving the above equation it results $\tau_r = 92$ [μs]. To compute the proportional gain, the PI controller transfer function is rewritten as:

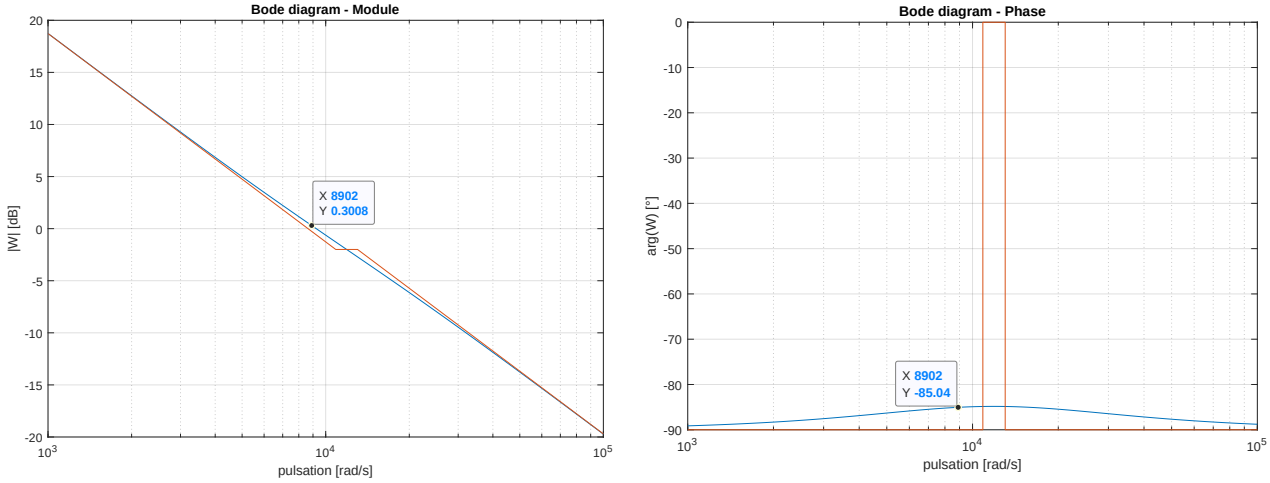
$$PI(s) = K_p \frac{1 + s\tau_r}{s\tau_r} \tag{5.25}$$

Imposing that the module diagram has to be null at the desired cross pulsation (i.e. in decibel the module has to be unitary), the equation below is solved:

$$1 = \frac{K_p \cdot 25.555}{s\tau_r} \frac{\sqrt{1+(s\tau_r)^2}}{\sqrt{1+(s0.0000768)^2}} \tag{5.26}$$

The results are itemized below:

- $K_p = 0.031$;
- $K_i = \frac{K_p}{\tau_r} = 337.97$.



(a) (b)

Figure 5.5: Module and phase Bode diagrams of the open loop system with PI controller.

The module and the phase diagrams of the transfer function with the PI controller are plotted respectively in pictures 5.5(a) and 5.5(b).

By means of the aforementioned computation, the simulation of the closed loop control has been done in Simulink, like shown in fig. 5.6. In this model the real system closed loop and that one containing the linearized transfer function of the system are parallel linked to check if the last one is able to follow the step response behaviour of the real system. Just for the sake of clarity, in the upper closed loop a reference signal and a delayed step input are applied and go inside the saturation block, which limit is 10 [A]; the current reference is then compared with that one measured at the output branch of the system and the error goes inside the PI controller; downstream the PI controller there is another saturation block (with upper limit equal to 0.4) and the result goes inside the gate signal subsystem, where the dimensionless phase shift is multiplied by T_{hf} and goes inside two delay blocks that act in the two PWM blocks referred to the output bridge, delaying them; a dead time always equal to 100 [ns] has been selected. For what concern the lower loop, in the left side there's a switch with a threshold value of 10 [A]: if the reference plus the step input overcome the threshold value then it will apply a step input equal to the difference between the upper limit of 10 [A] and the reference value of 9 [A].

Furthermore in picture 5.7 the matching state between the two closed loop systems is shown. From the diagram of the module 5.5(a) it's obvious that the behaviour at low frequencies is different from that one of the physical system, in fact in that case the action of the integrator is predominant and the transfer function tends to infinity for the pulsation that tends to zero, ensuring a null steady state error.

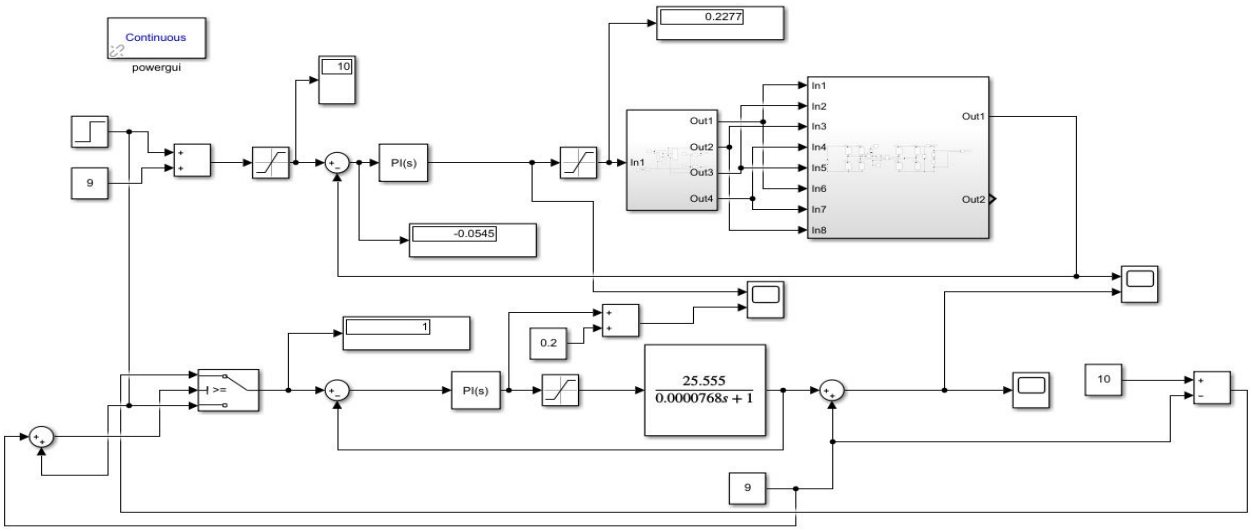


Figure 5.6: Simulink model of the current control loop

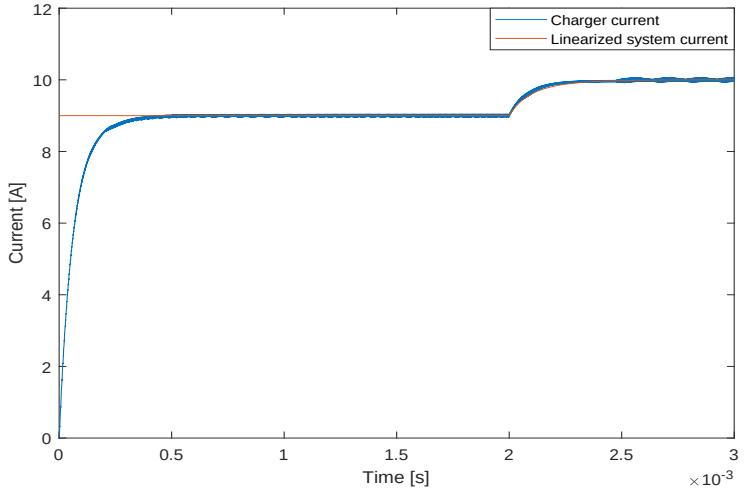


Figure 5.7: Step response of the current control loop.

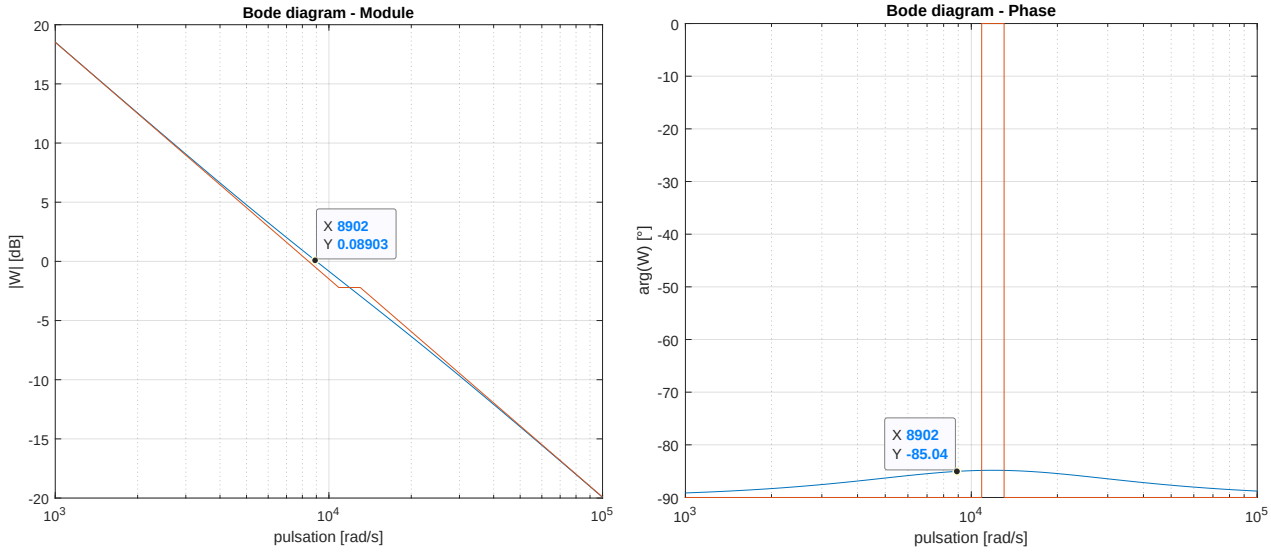
5.3 Cascade control loop

The last step of the charging path requires the control of the voltage but also the current, since the voltage has to remain constant but the battery still continues to charge. For these reasons a cascade control loop is necessary: it's made of an inner fast current control loop and an outer slow voltage control loop. The transfer function of the inner loop is the same of expression (5.19), instead that one of the outer loop links the perturbation of the battery voltage with that one in the phase shift and it's simply equal to the battery resistance R_b:

$$T(s)_V = \frac{\widehat{v_o}}{\widehat{d}} = R_b \tag{5.27}$$

In this case, the new equilibrium point is around the following quantities:

- average output current $I_{o,avg} = 2.5$ [A];
- phase shift $d = 0.13$;



(a) (b)

Figure 5.8: Module and phase Bode diagrams of the inner current control loop.

- battery voltage $v_o = 470$ [V];
- input voltage $v_i = 400$ [V];
- output power $P_o = 1175$ [W].

The first step is to study and tune the inner current control loop in order to derive the closed loop transfer function to put it in series with basically the battery internal resistance. With the new equilibrium point the current linearized transfer function becomes:

$$T(s) = \frac{\widehat{i_{o,avg}}}{\widehat{d}} = \frac{41.111}{1 + s0.0000768} \tag{5.28}$$

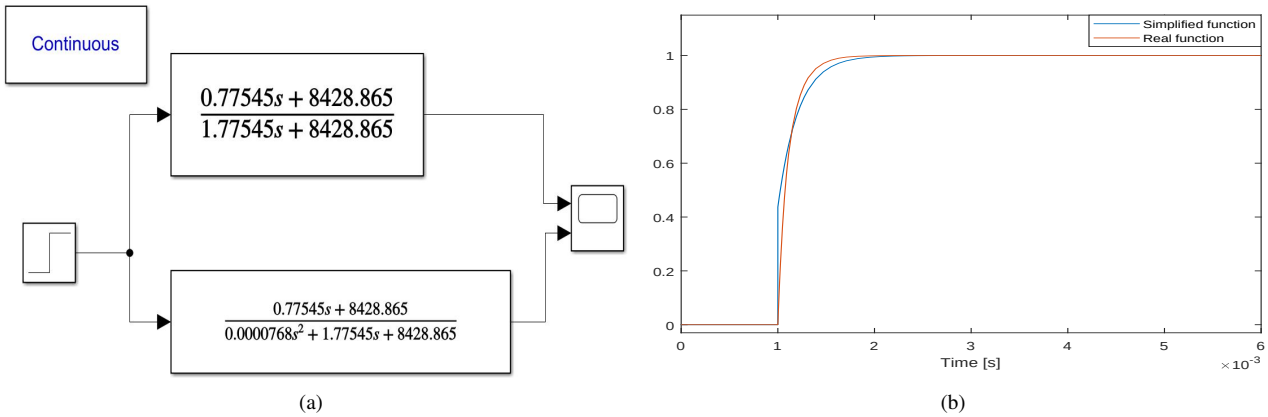
Plotting the Bode diagrams of the above equation, it appears that the physical system has a cross pulsation $\omega_c = 533.4$ [krad/s] and a phase margin of 91.4° (the plots about the open loop system are not presented in order to not make heavy the presentation of this control step). Since such a big cross pulsation is not needed, a smaller value has been selected, i.e. 9000 [rad/s] and a phase margin of 95°. Doing the same computations, already explained in the previous paragraph, to get the value of the proportional and integrative gains, the results are:

- $K_p = 0.01886$;
- $K_i = 205.027$;
- $\tau_r = 92$ [μs].

The open loop transfer function with the PI controller connected in series to the linearized system is:

$$T(s)_{OL} = K_i \frac{1 + s\tau_r}{s} \frac{41.111}{1 + s0.000078} \tag{5.29}$$

To verify the analytical computation, the module diagram 5.8(a) and the phase one 5.8(b) are shown in their respective



(a) (b)

Figure 5.9: Step response of the two transfer functions.

pictures. Afterwards the closed loop transfer function of the inner current control is computed and it results:

$$T(s)_{CL} = \frac{T(s)_{OL}}{1 + T(s)_{OL}} = \frac{s0.77545 + 8428.865}{s^2 0.0000768 + s1.77545 + 8428.865} \tag{5.30}$$

The aforementioned transfer function can replace the total current closed loop and the open loop transfer function of the cascade control corresponds to the product of this one by the battery resistance, getting:

$$GT(s) = T(s)_{CL} T(s)_V = R_b \frac{s0.77545 + 8428.865}{s^2 0.0000768 + s1.77545 + 8428.865} \tag{5.31}$$

The above second order transfer function can be simplified making the following assumptions:

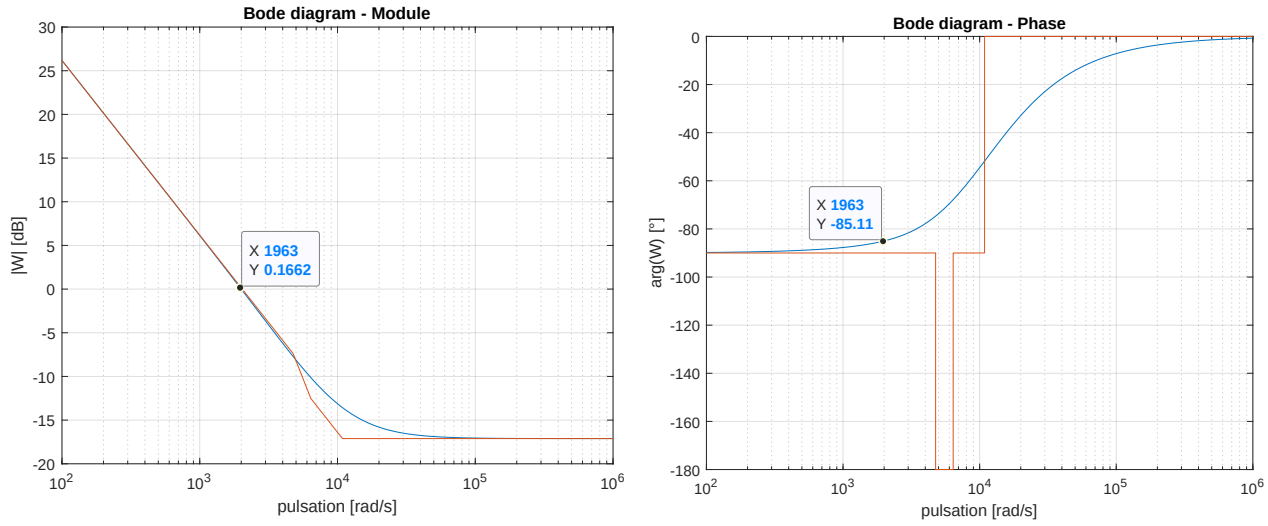
- the coefficient of the first degree term in the denominator is always greater or at minimum equal to 1 (when the phase shift d is equal to 0.5 and so the expression F_3 becomes null), furthermore this value is got taking into account the equilibrium point that can change during the working operation of the charger;
- on the other side the coefficient of the second degree term is stated by the hardware design and remains constant during all the charging process, it's always positive and quite smaller than one, so this pole acts at very high frequency and it won't influence the system behaviour at low frequency; furthermore it has to be outlined that the simplified function (without the second order term) is still causative.

Taking advantage from the above considerations, just to design the PI controller for the output loop, the second order term is neglected and the transfer function can be approximated as a first order one:

$$GT(s)' = R_b \frac{s0.77545 + 8428.865}{s1.77545 + 8428.865} \tag{5.32}$$

Just to clarify the aforementioned assumption, the two transfer functions have been linked in parallel (as shown in fig. 5.9(a)) and the step responses are reported in the picture beside. The time range is in the order of tens milliseconds, obviously decreasing it the deviation between the two waveforms would increase but since the voltage of the battery hasn't got a such fast development, it's reasonable to apply the assumption and consider the simplified transfer function for the design of the outer PI controller. A phase margin equal to 95° and a cross pulsation ω_c of 2000 [rad/s] are chosen as the final goal for the voltage outer loop. The simplified transfer function written in Bode form results:

$$GT(s)' = R_b \frac{s0.000092 + 1}{s0.00021 + 1} \tag{5.33}$$



(a) (b)

Figure 5.10: Module and phase diagrams of the cascade open loop control.

Imposing the desired phase margin it's possible to get the time constant of the controller, that it's equal to $\tau_r = 156.27$ [μs]; finally, stating the wished cross pulsation, the proportional gain is got and after that also the integrative one, equal to: $K_p = 0.6215$ and $K_i = 3977$. In order to close the reasoning the module and phase plots of the cascade open loop control are plotted in figures 5.10(a) and 5.10(b); as it's possible to see the goals are reached. To conclude the cascade

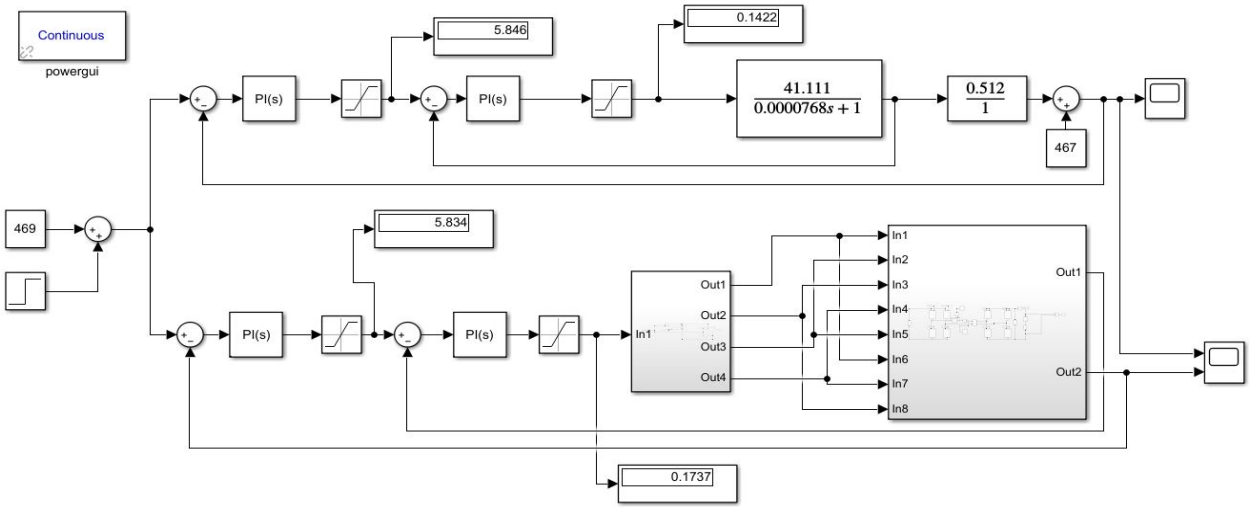


Figure 5.11: Simulink model of the cascade control.

control design, a Simulink model of the real circuit has been connected in parallel with the linearized one (taking into account the real transfer function and not the simplified one), as shown in fig. 5.11. Below, the output voltage step response is reported: looking at the waveforms in fig. 5.12, it appears that at the beginning, during "ignition" of the circuit, there's a small undershoot in the voltage of the battery branch, due to the fact that the battery acts, for a small time, like an energy source feeding the smoothing capacitor; also a small overshoot during the shifting range appears with respect the linearized system. In any case, taking in mind all the simplifying hypotheses, the behaviour of the two system models results good.

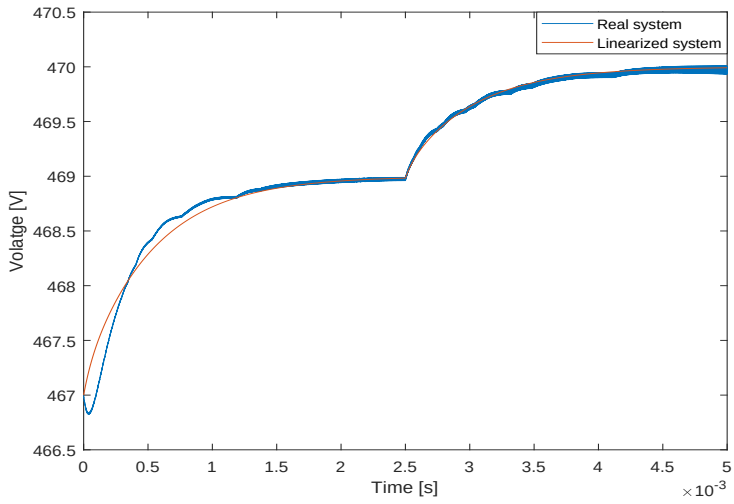


Figure 5.12: Output voltage step response in the cascade mode.

5.4 Anti-windup strategies

Both aforementioned control loops present a drawback due to the presence of the integration action: when the system reaches its saturation condition, the so called "windup" phenomenon occurs and it causes degradation in the automatic control, since the integrator discharges itself in a long time after the saturation happens. To overcome this problem some methods have been developed and the two most famous are:

- conditional integration;
- back calculation.

The first method consists in turning off the integrative path (in other words the error is put equal to zero) when the two following conditions are verified:

- the control variable saturates, i.e. the parameter value downstream the PI controller block is different with respect the value that is applied to the PWM generator subsystem, hence that one that comes out from the saturation block in each Simulink model shown above;
- the integration is stopped when the first condition is verified but furthermore the control variable and the error have the same sign, it means that the product $e(t) \cdot u(t)$ is positive.

The second method (that one that has been used in this thesis) is plotted in fig. 5.13. The main idea of this technique is to recompute the integral quantity when saturation occurs. From the plotted scheme it emerges that when the controller output is greater or smaller than its boundaries (dictated by actuator limitations), the integral value is reduced or increased respectively, by summing to the parameter that is going inside the integration the feedback difference between the saturated and unsaturated control signals; the variable τ_t is called "tracking time constant" and it's value has been imposed equal to the constant time τ_r of the controller. Since in the praxis just the current control loop has been implemented (simply because the current control loop is always present and it's the most important), the back calculation method is shown in fig. 5.14 referred to the current control loop.

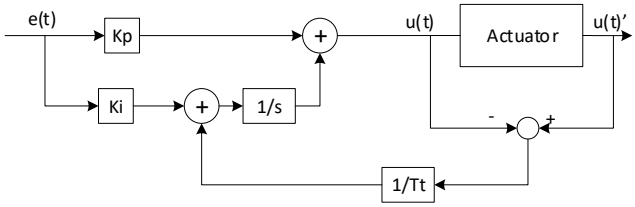


Figure 5.13: Back calculation scheme.

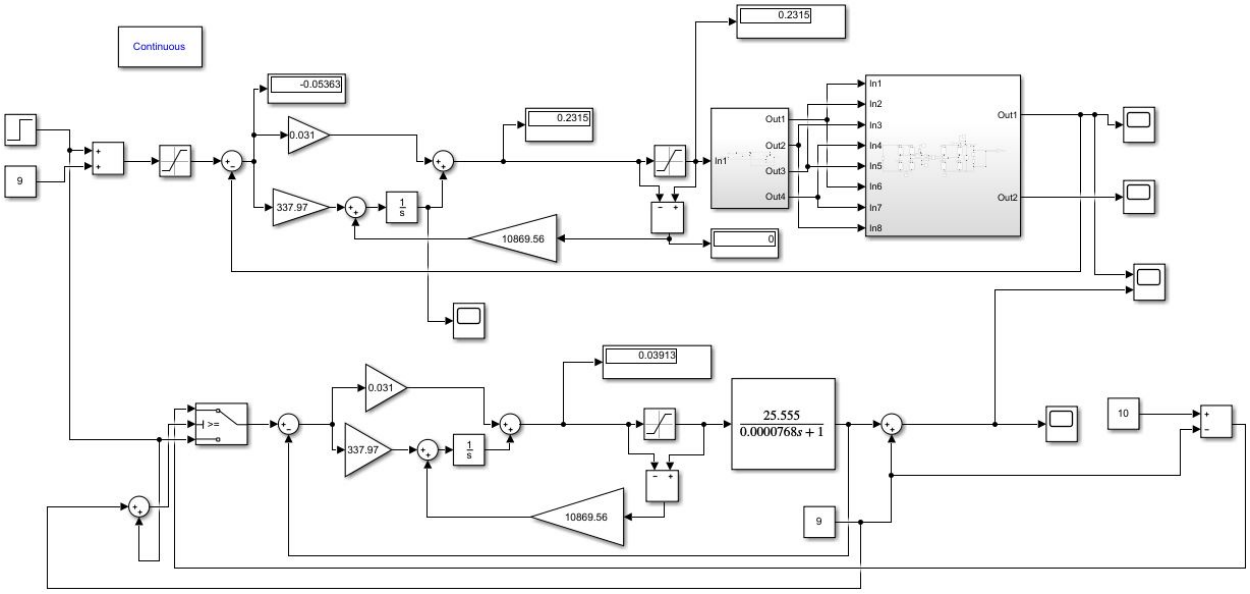


Figure 5.14: Simulink model with anti-windup strategy.

From analog to digital implementation

This sub-paragraph is a brief outlook on the problems that arise moving from continuous plant simulation to discrete implementation. Nowadays almost all the control logic is implemented by means of digital microcontroller instead of analog circuits, this implies that the signals are discretized. In addition to loss of information discrete systems add delays into the feedback loop because it takes time to read a measurement, digitize it and then run the control algorithm. By the time the command is issued, the measurement that command is based off is old; as a consequence of it, the bandwidth of the controller is smaller and this one is the main reason because in praxis the gains computed before have been decreased a lot, otherwise the control would have been unstable with high frequency oscillations.

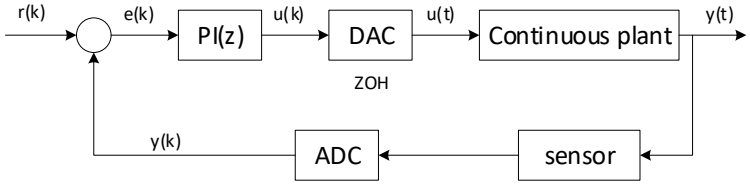


Figure 5.15: Analog to digital conversions along the control loop.

Since the digital control has to interact with the real system, the discrete quantities have to be shifted into continuous

ones by means of the zero order hold (also known as digital to analog converter): it simply receives in input the discrete quantity and maintains it constant for the whole sampling time, creating a continuous step signal, in this way the control applied to the plant doesn't change punctually but its updating relies on the sampling time. The zero order hold (ZOH) can be described also through a transfer function (the demonstration is not reported because it would make the explanation long and it's not the topic of the thesis): starting from the continuous signal, the Laplace transformation of its samples is computed and after that the Zeta transformation is got. Subsequently, starting from the samples value, the zero order hold creates a staircase waveform; expressing each star as the difference of two step functions, transforming the expression got into the Laplace domain and dividing it by the Laplace transformation of the "samples train", the following non linear ZOH transfer function results:

$$ZOH(s) = \frac{1 - e^{-Ts}}{s} \tag{5.34}$$

The term e^{-Ts} can be rewritten as $e^{-Ts} = \frac{e^{\frac{-Ts}{2}}}{e^{\frac{Ts}{2}}}$; expanding this ratio with the Taylor series and applying the Padé approximation (it consists on considering just the first order terms for both numerator and denominator expansions), the following solution results:

$$e^{-Ts} \simeq \frac{1 + \frac{sT}{2}}{1 - \frac{sT}{2}} \tag{5.35}$$

and finally the DAC approximated transfer function becomes:

$$ZOH(s) \simeq \frac{1}{1 + s\frac{T}{2}} \tag{5.36}$$

This "small bracket" demonstrates the inadequacy of the ideal control loops designed in Simulink since all the delays and hence all the digital devices that control the plant should be described in the Laplace domains (sensors, DAC, ADC, quantizer ect) and it would drastically complicate the design of the analytical controller; for this reason in the praxis implementation the tuning of the PI controller has been empirical.

6 Laboratory results

In this chapter the real implementation of the single phase shift control is presented. After a very brief description of the circuit topology, the current control loop into Simulink embedded ambient will be presented and finally the current waveforms and the temperature measurements by means of a thermal camera are shown.

6.1 Circuit layout

The existing charger is composed by the series of a power factor corrector and a CLLC resonant DC-DC converter, for this reason the first task has been to remove the resonant capacitances banks existing at the output and input of the input and output DC-DC converter bridges respectively and the conducting rails have been linked by means of two small steel bridges. Taking a look to the top view of the charger in fig. 6.1, a brief description of its design layout is summarized hereinafter.
The circuit power supply is 12 [V], i.e. that one of the vehicle. Starting the "journey" from the left bottom side:

- in the yellow rectangle are enclosed the 12 [V] and CAN filters;
- inside the two white rectangles the voltage is converted into different ranges: 24 [V] for the relays; 5 [V] to feed the switches' drivers; 3.3 [V] and 1.2 [V] to turn on respectively the complex programmable logic drive (CPLD) and the two digital signal processors (DSPs), one to control the PFC and another one to the DC-DC converter;
- the green rectangle encloses the voltage sensors for both the DC link capacitors bank and the grid instead besides the violet boundary delimits the temperature sensors;
- in the red box there is the DC link discharge unit, useful when the whole charger works, in fact it could happen that at the "ignition" instant of the PFC the big capacitances are not fully discharged and so, by means of the voltage sensor, it's possible to drive a switch that links the DC link with the three series resistances; since in this thesis job the circuit is fed just in the DC-DC side, these resistances don't conduct;
- in the central and right side there is the power electronics unit, composed of both the PFC full bridge (blue rectangle) and the two bridges of the dual active bridge; in both of them each driver switch is fed by means of a DC-DC converter (the black high box near each power device), necessary to maintain the integrity of the module of the signals;
- under the PFC area there are two fuses, at the bottom side of the PCB there are the AC filters (small thanks to the high frequency, as briefly stated in the first chapter) and the free space for the smoothing inductance;
- inside the orange box there is the full DC-DC converter: in this particular case, since the original layout was that one of the CLLC, in each bridge there are shunt resistances and Smith trigger that allow to detect the zero current crossing; obviously in the DAB they are not necessary and create a small amount of power lost;
- the brown rectangle encloses an opto coupler to guarantee the galvanic isolation of the digital signals, instead the green one in the right side corner represents the ADC converter for the output voltage measurement;

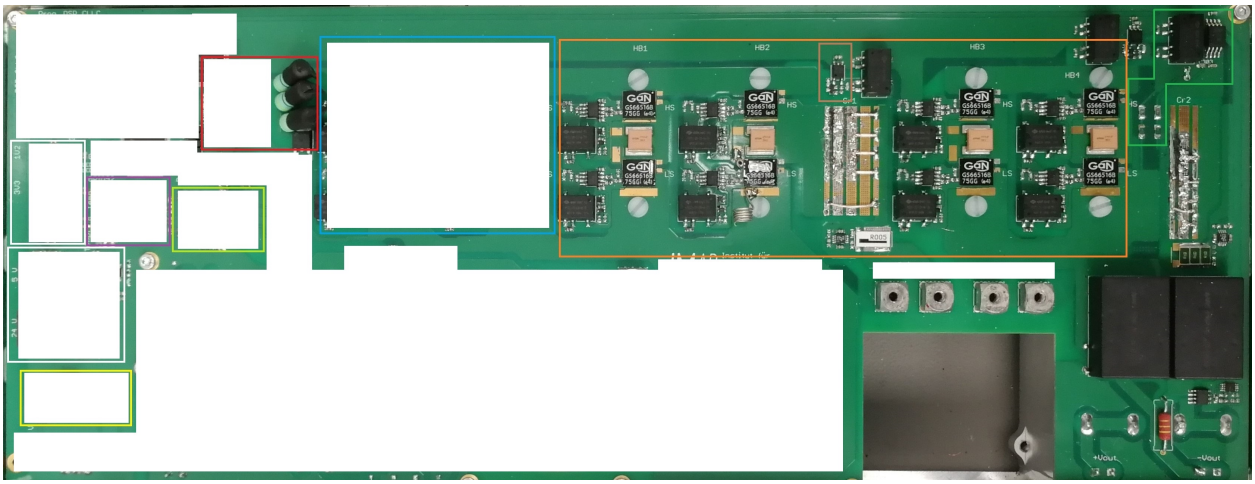


Figure 6.1: Top view of the whole charger.

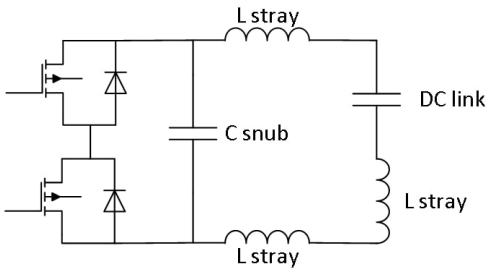


Figure 6.2: Schematic circuit to explain the need of the snubber capacitances.

- finally, in the right bottom side there are the "transformer hole", two parallel capacitances to smooth the rectified voltage to which the orange discharge resistance is always linked in series (it creates losses in this configuration, but the circuit complexity and cost are lower) and the current measurement unit.

In the real DAB are needed some further snubber capacitances in parallel to each leg of each full bridge, as it's described in the circuit in fig. 6.2. To connect the DAB to the DC link there are long paths of conductors and therefore stray inductances; moreover, the real model of a capacitor consists of capacitance with an inductance in series. When the switches quickly commutate, there are big rates of change in the current of the circuit and therefore, due to these inductances, voltage overshot greater than 600 V could be created and would destroy the FETs. The snubber capacitors act as a "funnel" to these large current variations.

6.2 Current control loop

The first step has been to program the CPLD by means of Quartus software, in which the different pins have been assigned to the desired control signals (in this case it has been selected the input bridge to be driven by the slave ePWM block and the output bridge by the master one, since the slave signal anticipates the master one with positive phase shift values); after that the two ePWM blocks have been synchronized and then, by mean of Simulink embedded coder, downloaded into the DSP of the DC-DC converter. To synchronize the two blocks the Delfino microcontroller manual has been considered [22]. In each ePWM block there are 5 main sub-modules:

- the time base (TB) one;

- the counter compare (CC) one;
- the action qualifier (AQ) one;
- the dead band (DB) one;
- the event trigger (ET) one.

The first one allows to the user to specify the time base counter directions: it can be set in up or down count mode for asymmetric PWM signal or in up-down mode for symmetric working condition; in the last case, since the counting mode is symmetric, the input time base period has to be the half of the desired switching period; furthermore it's possible to declare the phase shift between two ePWM blocks that work synchronized (in this case the value inside the phase register is uploaded in the counter register after an useful event), decide the counter direction of a synchronization event.
The second one has in input the value of the time base counter and compares it with the values of the two comparators: when a match between the two value occurs, the counter compare puts high a bit inside the action qualifier.
The aforementioned third block allows to declare which actions have to be done after a valid counter compare event, they are divided into: set, clear and toggle. By means of the CC and the AQ it's possible to decide the duty cycle of the PWM signals. It has to be underlined that when the synchronization event occurs, the PWM signal in the slave block is generated with an internal delay equal to two clock periods if the time base clock matches the ePWM one (in the case of the Delfino TMS320 F28377S the value is equal to 20 [ns], since the clock frequency is 100 [MHz]), for this reason a compensation of 2 clock times has been stated inside the program.
The fourth block acts in the PWM signals in both rising and falling edges, decreasing the previous computed duty cycle of a value equal to the number of clock times.
At last the event trigger manages the events generated by the CC sub-module to create an interrupt inside the CPU

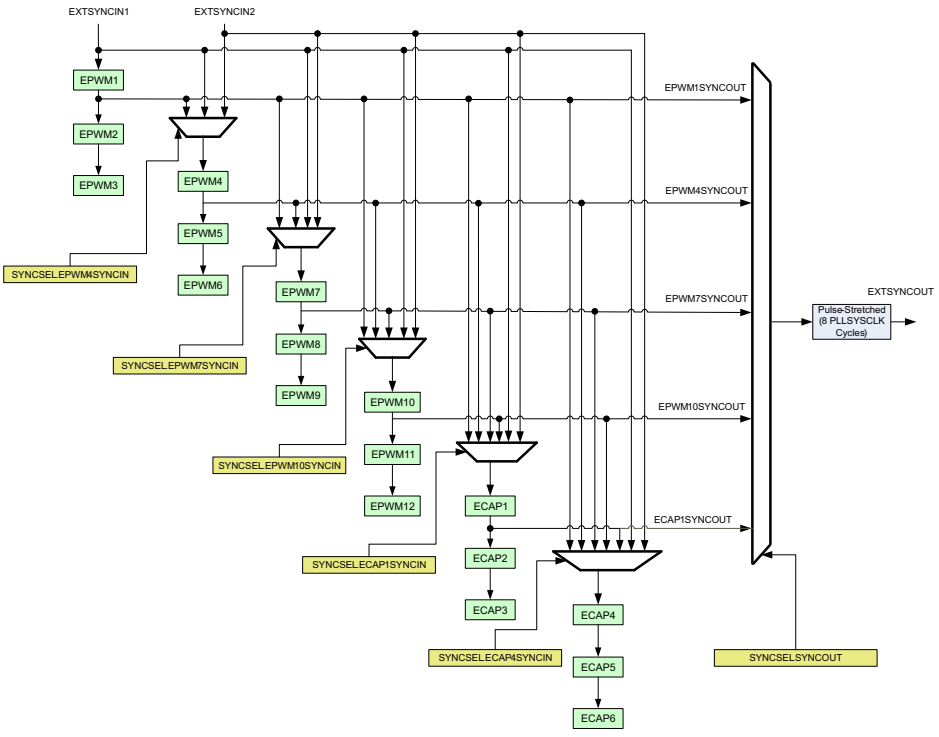


Figure 6.3: Delfino microcontroller time base counter.

that starts the ADC conversion. To decide which ePWM blocks can be linked together the flow chart shown in fig. 6.3 has to be taken into account: it's not possible to link ePWM blocks that don't share a synchronization signal. In this design the seventh and eighth blocks have been linked together with the following settings for the master one (seventh):

- time base period equal to 1 [μs];
- duty cycle equal to 50%;
- reload time base period register when the counter is equal to zero;
- counting mode up-down in symmetric operation;
- synchronization action disabled, since it's the master and no action has to be implemented when the counter compare equals the time base counter;
- synchronization output when the counter is equal to zero;
- since each ePWM can create two complementary signals, the first one is set high when the time base counter matches the counter compare value on up-count and low when the same event happens on down-count, instead the second one has opposite settings in the action qualifier;
- dead time band equal to 180 [ns], since due to RC circuit of the drivers the PWM signals don't look like ideal square waves, but they have a rising and falling exponential shape delay of about 90 [ns] and for this reason other 90 [ns] of real null signal have been declared. For what concern the slave block, it has the time base period linked to the master one and the synchronization action enabled, in order to upload the time base counter with the value put inside the phase register when the time base counter value is equal to the counter compare one.

The whole control loop is shown in picture 6.4: starting from the top left side, the ADC current measurement is modified by means of two gains used to calibrate the current sensor and it's sent, by means CAN communication, to the vehicle; the measured value is compared with the reference one that comes from the vehicle and the difference is multiplied both by proportional and integrative gains (the two gain blocks are used to convert the sent integer values in floating point, in order to not congest the CAN buffer). Following the integrative path, the back calculation is implemented: the feedback signals are delayed of a unit and the Matlab function block simply implements the following function:

```
function y = fcn(e,pwm_en,int)
if pwm_en==0
    int=single(0);
    e=0;
else
    e=e/15000;
end
y = e+int;
end
```

If the PWM is not enabled, the integral value is put to zero as well as the error one, otherwise the error is overwritten with its previous value divided by 15 [kHz], i.e. the uploading frequency of the ADC converter, and the output y becomes the sum of the previous results and the actual increment or decrement. Downstream the two PI contributes

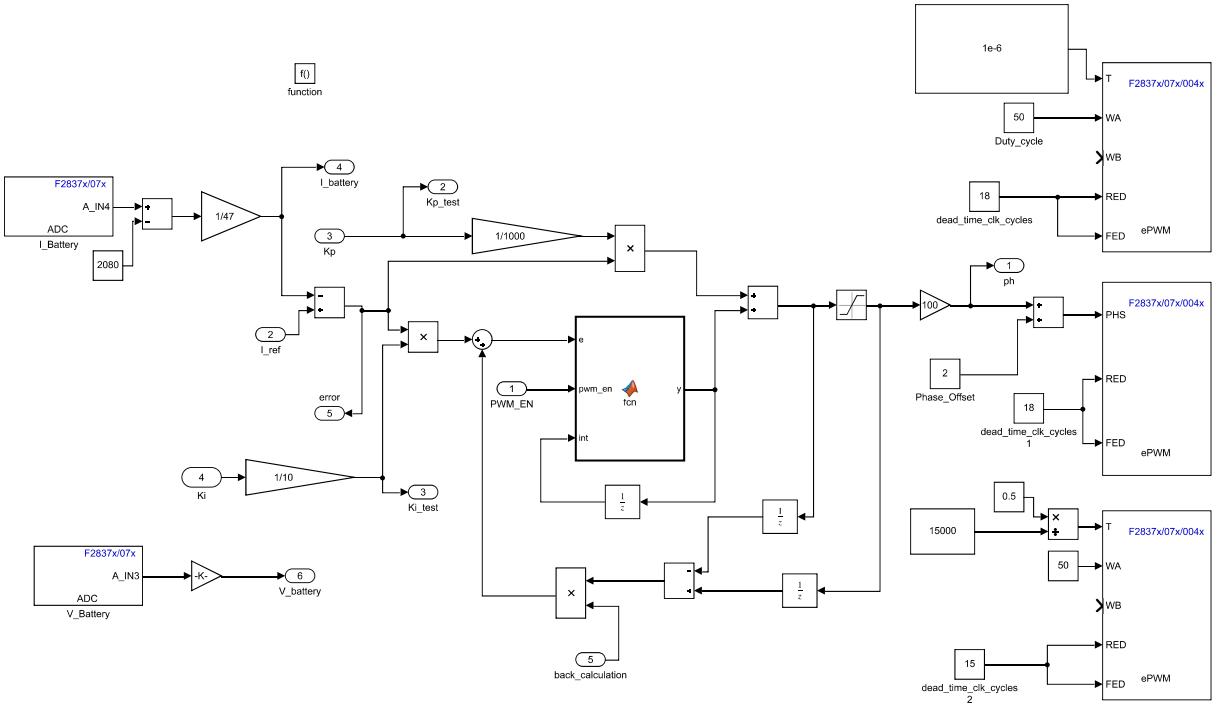


Figure 6.4: Current closed control loop.

are added up and the final value is multiplied by 100 in order to send to the phase register an integer number of clock cycles of delay.

Finally, in the bottom right side there is an ePWM block used to generate the interrupt in the CPU to start the analog

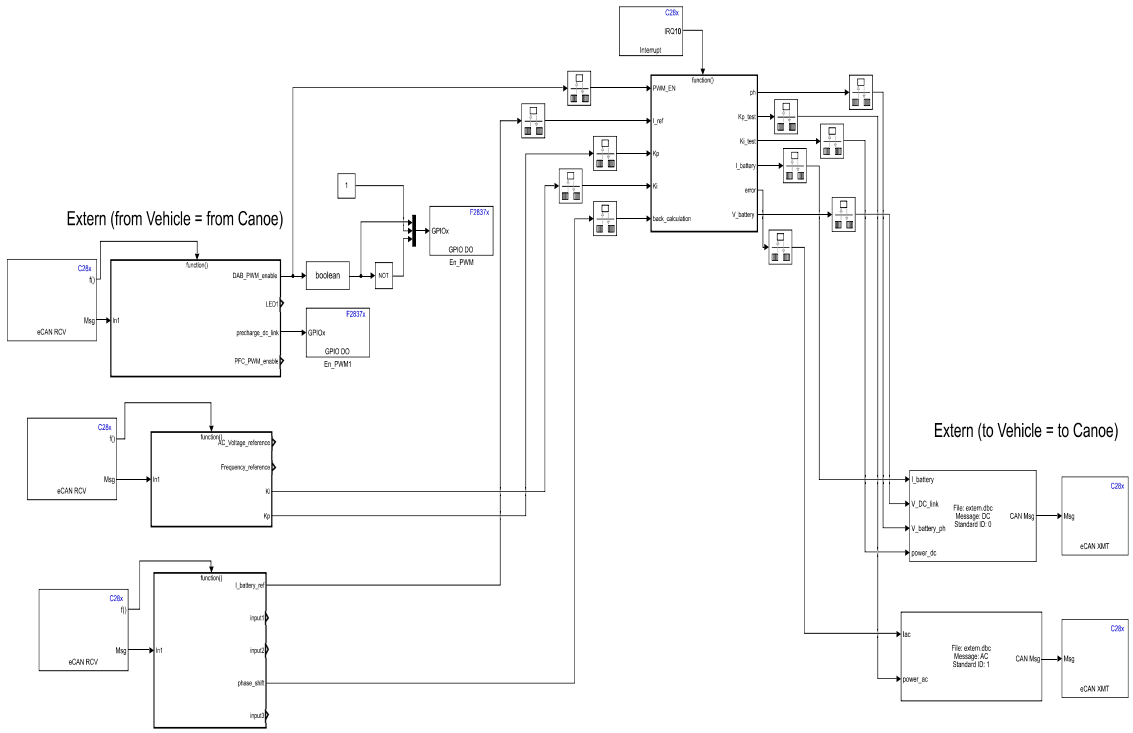
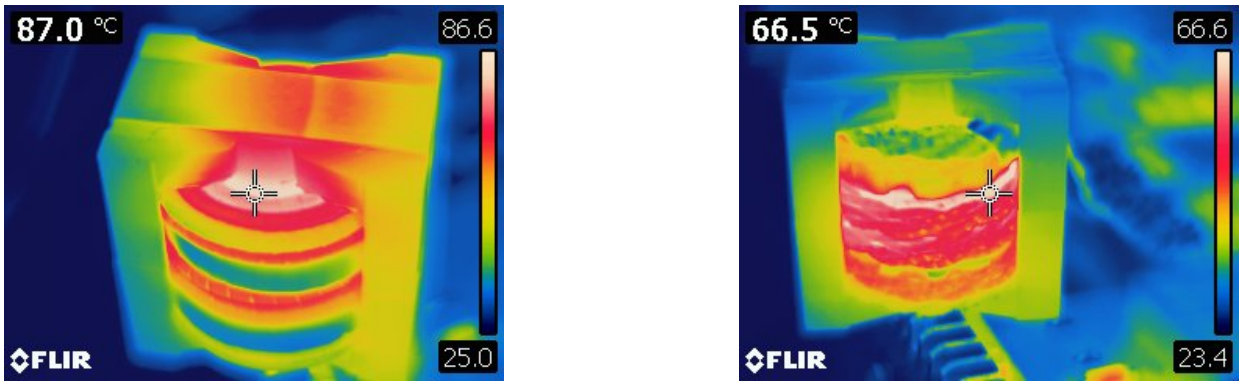


Figure 6.5: External system of the current control loop.



(a) (b)

Figure 6.6: Thermal measurements on the PQ5050 transformers.

to digital conversion of the current and voltage measurements.
"To close the circle" the external system of the Simulink embedded scheme is presented in fig. 6.5: in the left side there are the blocks that allow to receive the informations from the vehicle (in this case represented by Canoe, a CAN communication software in which it has been created a control panel through which send and receive informations) and create a function signal to the respective CAN unpacks, in which the extern.dbc files are recalled, in order to set the signals that have to be received and managed by the control loop subsystem; in the right side there are the blocks useful to transmit the charger measurements to the control panel in the vehicle (there are some signals not used for the DAB but already presented in the .dbc file made for the CLLC previous layout).

6.3 Working conditions

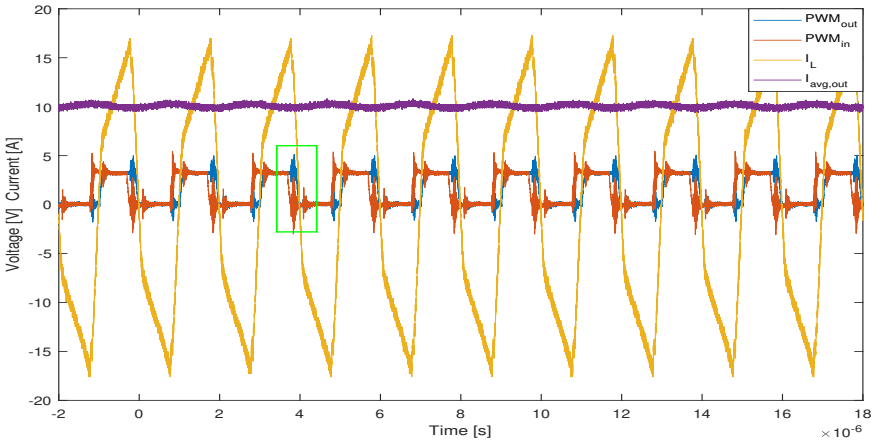
This paragraph summarizes the three different transformers working states at maximum output power (around 3.7 [kW]) in matching state, in order to not have problems of hard switching in the circuit. Furthermore, with the transformer having the bigger leakage inductance an efficiency characterization has been made and documented. The thermal measurements have been made by means of FLIR thermal camera and with the charger and two outer fans turned on; picture 6.6(a) reports the maximum stable temperature (after 30 minutes) reached in the PQ5050 asymmetric transformer (just to remember, the primary and secondary windings consist of 9 turns of 2250 parallel strands litz wire) instead figure 6.6(b) shows the maximum temperature in the PQ5050 symmetric transformer (built up with 12 turns for each windings and two twisted 450 parallel strands litz wire); in the last case the total power lost of the charger corresponds to 100.37 [W] in matching state, hence an efficiency around 97.22%. As supposed in the chapter about the transformer design the maximum temperature is reached in opposite elements in the two PQ5050 transformers: in the first case, since the current density is very small and the not interleaved layers with current of the same sign are at maximum two, the biggest power lost amount is concentrated in the core, cause of the high peak flux density and high specific power losses, it has also to be outlined that the reactive power is high due to the leakage inductance; in the second case the core losses are quite small since the magnetic flux density has both signs in each time instant, but the winding power losses are high, especially in the four not interleaved secondary winding layers and also due to the bigger value of the current density, furthermore in this case the reactive power is a little bit smaller with respect the first case, since the leakage inductance is smaller, this aspect could seem positive for the transformer power lost, but it has to be remembered that the charger efficiency relies much more on the hard switching losses.

(a) (b)

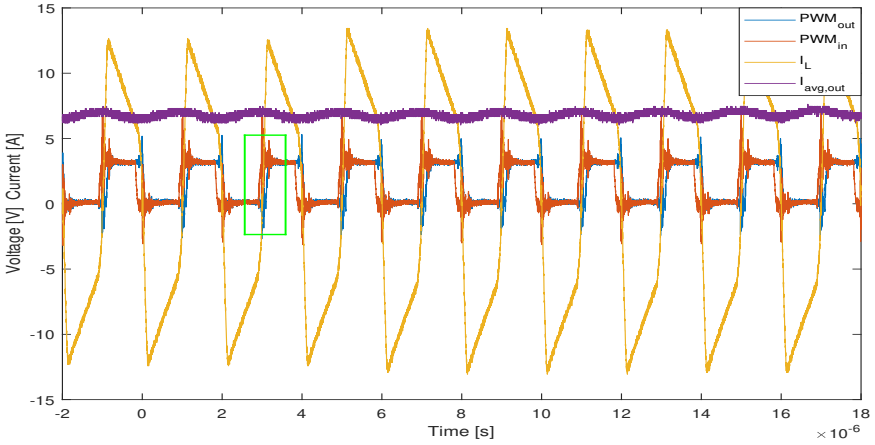
Figure 6.7: Thermal measurements on the PQ4040 transformer and switches.

Finally in picture 6.7(a) the maximum temperature reached in the PQ4040 transformer is shown: as predicted, the major amount of power lost is concentrated in the windings, especially cause of proximity effect and high current density; beside in fig. 6.7(b) the average switches temperature reached is presented: as it's possible to understand GaN power devices suffer for the low thermal conductivity.

In figure 6.8 the waveforms in buck mode (input voltage of 400 [V], output voltage of 270 [V], output average current



(a)



(b)

Figure 6.8: Buck and boost mode waveforms.

of 10.15 [A]) and boost mode (input voltage of 400 [V], output voltage of 470 [V], output average current of 7.1 [A]) are shown; as it can be seen in fig. 6.8(a) (the PWM signals refer just to one switch pair for each bridge) there is a bit of hard switching in the output bridge since the gate signal goes down with positive current and the complementary gate signal (not shown in the picture cause of the number of oscilloscope channels) goes down with negative current, not allowing the complete charge and discharge of the parasitic output capacitances; on the other hand looking at picture 6.8(b) there is a bit hard switching in the input bridge since the switches are turned on with positive leakage inductance current. As explained below, smaller values of output current would make greater the hard switching losses in both cases, confirming the ZVS boundaries plotted in the DAB chapter. Table 6.1 presents a comparison between different working conditions for all the three modes, these tests have been made using the transformer with the biggest leakage inductance in order to have the biggest ZVS area. In the table there aren't operating points with small currents, especially in buck and boost mode, cause of high temperature in the switches (around 75 [°C]) due to the lost of soft switching commutations.

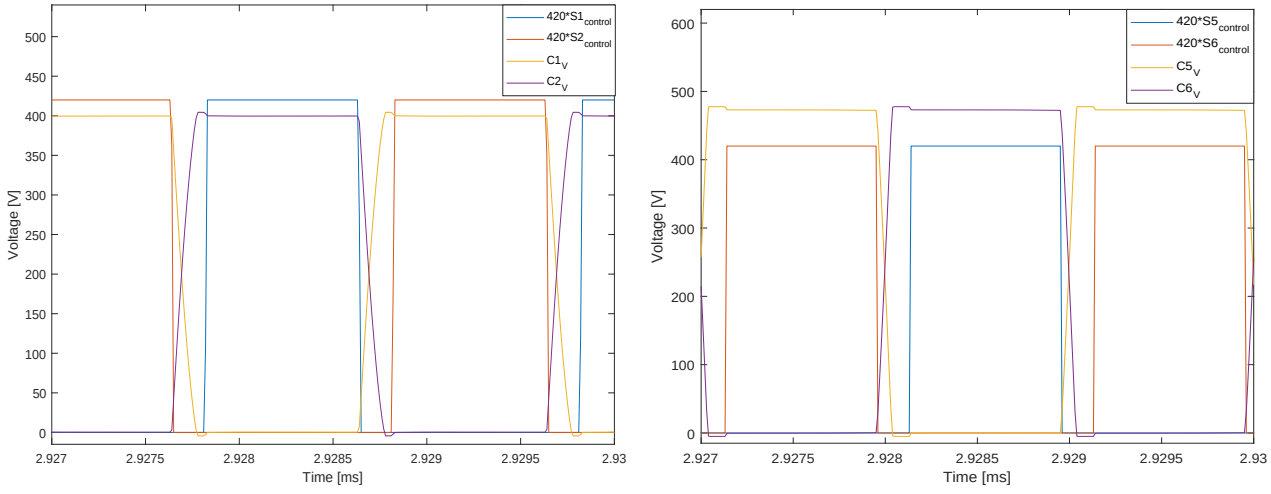
Table 6.1: Efficiency trend in buck, matching and boost modes.

Input/output voltages [V]	Output current [A]	Input/output power [kW]	Efficiency η [%]
Buck mode			
400-370	9.14	3.45-3.364	97.507
400-370	8.12	3.06-2.991	97.7
400-370	7.08	2.7-2.612	96.48
400-350	9.14	3.27-3.1865	97.446
400-350	8.12	2.917-2.8364	97.237
400-330	9.14	3.088-3.003	97.2323
400-311	9.14	2.9276-2.82585	96.52445
400-311	10.16	3.23267-3.14058	97.15
400-291	10.15	3.032-2.93789	96.89
400-270	10.15	2.8508-2.73852	96.06
Matching mode			
400-400	9.14	3.735-3.642	97.5
400-400	8.1	3.31-3.233	0.9767
400-400	7.09	2.9-2.8277	97.51
400-400	6.07	2.51-2.42	96.4
Boost mode			
400-416	9.14	3.878-3.777	97.39
400-416	8.1285	3.443-3.36	97.589
400-416	7.1	3.0147-2.93878	97.48
400-416	6.08	2.608-2.51558	96.456
400-436	9.14	4.075-3.96	97.177
400-436	8.11	3.6098-3.51524	97.38
400-436	7.08	3.162-3.074	97.213
400-436	6.08	2.7397-2.636	96.22
400-456	9.15	4.272-4.145	97.02
400-456	8.12	3.79-3.684	97.2
400-456	7.09	3.32-3.22	96.98
400-470	8.13	3.929-3.81	96.97
400-470	7.1	3.455-3.33	96.382

7 Alternative control techniques

In chapter two the design of the leakage inductance has demonstrated that the DC/DC converter suffers for the limited soft switching area and this drawback is appeared also in the real simulation of the circuit, making it impossible to go down below a minimum load current; it has been observed that a "direct" way to circumvent this obstacle could be to increase the value of the leakage inductance as it emerges in the comparison between the two opposite design methods of increasing the ZVS area or maximizing the efficiency at nominal output power. To verify that analytical trend, a simulation of the circuit, controlled by means of the back calculation PI method, has been done with the following properties:

- leakage inductance equal to 16 [μH];
- dead time corresponding to 180 [ns];
- an output average current of 5.25 [A];
- boost mode with output voltage of 470 [V].

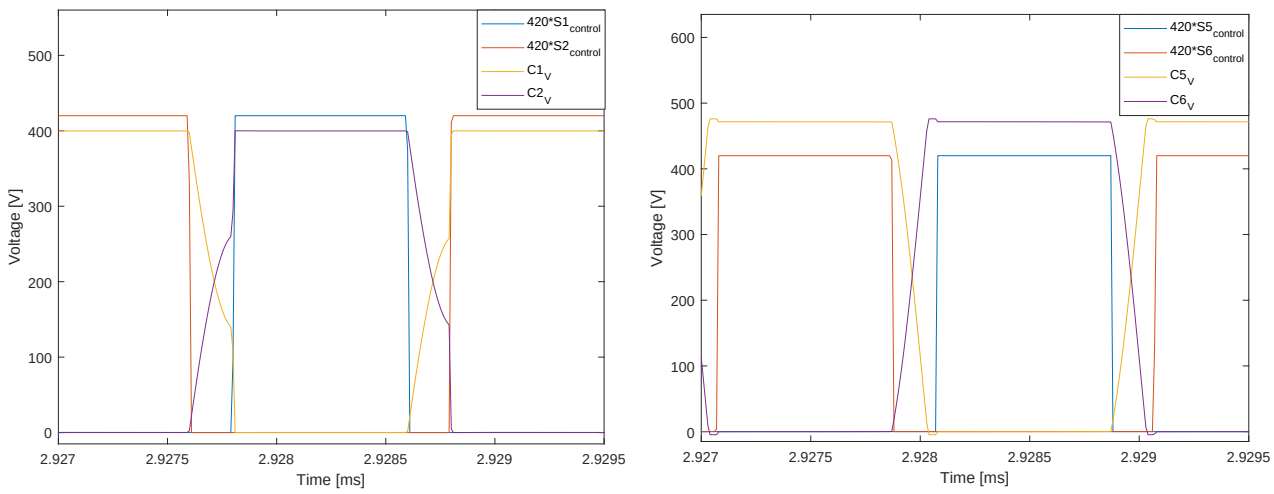


(a) (b)

Figure 7.1: Input and output bridge soft switching in boost mode with a leakage inductance of 16 [μH].

Taking in mind the schematic circuit in chapter three, the voltage waveforms of the parasitic capacitances for the input and output bridges are plotted in pictures 7.1(a) and 7.1(b) respectively. It emerges that the soft switching area is increased with respect the designed case of a leakage inductance around 7.3 [μH]. Since in this case the output power is still too high to perform the last step of the charging path (P_o=2467 [W]), another simulation has been done with the new settings enumerated below:

- leakage inductance equal to 25 [μH];
- dead time corresponding to 200 [ns];



(a) (b)

Figure 7.2: Hard and soft switching in the input and output bridges respectively with L=25 [μH].

- an output average current of 2.8 [A];
- boost mode with output voltage of 470 [V].

As can be seen in picture 7.2(a) the soft switching is not verified in the input bridge, although the value of the leakage inductance is very big. There are three main settings in which it's possible to act to extend the ZVS area:

- dead time;
- leakage inductance magnitude;
- control technique.

The first two have been explored above with the single phase shift control, but they present some drawbacks:

- integrate such a big value of leakage inductance inside the high frequency transformer is not easy and not recommended, since it would be necessary to create big values of the magneto motive force that as a consequence would increase a lot the proximity effect, making the windings very hot;
- use an external inductance would increase the cost and the volume of the magnetic devices, but one of the main goal in the transformer design has been to match the free space available in the charger case;
- since the transmitted power is inversely proportional to the leakage inductance, in order to guarantee a nominal power of 3.7 [kW] bigger values of the phase shift have to be applied, near to the maximum peak of 0.5 in which there is a lot of reactive power that flows inside the charger; furthermore a big voltage drop would occur across the leakage inductance, since the switching frequency is high.

For this reason it becomes necessary to apply different control strategies for lower load current. In the following paragraphs the single PWM technique and the double one are described and their results are presented in the simulation, considering a leakage inductance value equal to 7.3 [μH].

7.1 Single PWM control

To understand why there is hard switching also if in the ideal case it seems that it's soft, a new simulation in buck mode with the following settings has been done: output voltage of 330 [V]; L=7.33 [μH]; output current equal to 7.8 [A]; dead time of 160 [ns].

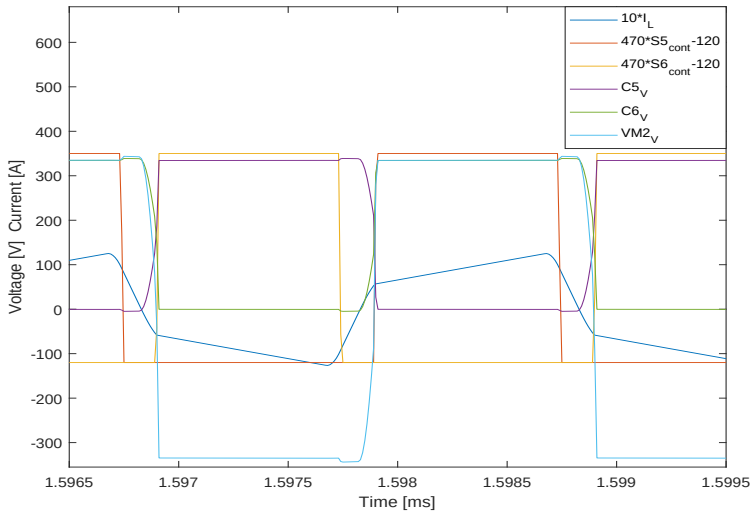


Figure 7.3: Hard switching commutations in the output bridge with SPS control.

Taking in mind the schematic Simplorer circuit plotted in chapter three and remembering that the switches layout is

$$\begin{bmatrix} S_1 & S_2 \\ S_3 & S_4 \end{bmatrix}$$

for the input bridge and

$$\begin{bmatrix} S_5 & S_6 \\ S_7 & S_8 \end{bmatrix}$$

for the output one, looking at the plot 7.3 it's possible to see that, although in the ideal case it seems there's soft switching, in the reality, cause of the dead time, the commutation in the output bridge is hard, for this reason: the control signal S6 goes down with an angle of $t_{dead} f_{sw} 360°$ before that S5 signal goes up, in this way the switches S6 and S7 turn off when the inductance current is still negative and this implies that their anti-parallel diodes conduct, clamping the voltage at the "same" magnitude as when S6 and S7 conduct (there's also the diodes threshold voltage of 4.3 [V]); in this way until the inductance current is negative, the dead time is going on but the parasitic capacitances don't start to charge and discharge. As soon as the current becomes positive and both S6 and S5 control signals are low, the current can't pass through the diodes D5 and D8 because they are inversely polarized by the positive voltage across both C5 and C8, so it flows inside the four capacitances, to charge C6 and C7 and discharge C5 and C8, although the interval time to accomplish this resonance between inductance and capacitances is not enough and hard switching appears, since the voltage VM2 (that one across the output port of the transformer) goes up when S5 and S8 gate signals are high, without the conduction of their anti-parallel diodes. Downstream this brief analysis an aspect is remarked: the dead time changes the working conditions of the charger and during it's interval the voltage applied across the leakage inductance depends on the current sign that decides if capacitances or diodes will conduct. This aspect is the reason for why in the following explanations there could be discrepancies between analytical and simulation results. To overcome the problem of high switching losses other control techniques have been exploited, as

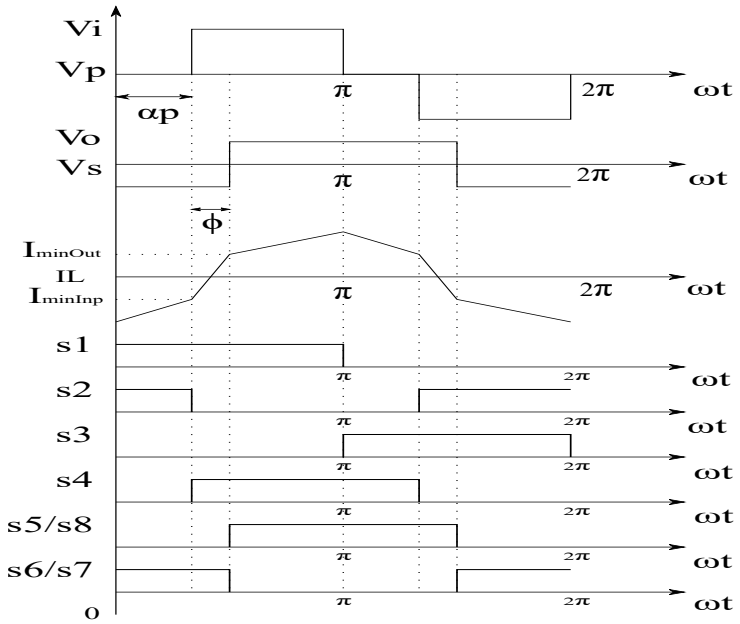


Figure 7.4: Working waveforms and switching path in the case of single PWM control.

the single PWM and the double PWM, both presented in [23].

7.1.1 Buck mode

When the output power is not very low, in order to increase the ZVS area with respect the case of SPS modulation it's necessary to introduce a further control variable that doesn't act between the two bridges, but between the two legs of the input bridge; in this way the AC voltage applied to the input port of the transformer has three levels, since with the inner bridge phase shift α_p it's possible to create some freewheeling intervals. In fig. 7.4 the operation waveforms in buck mode and the switches signals are shown: it's clear that the lagging leg in the input bridge is delayed of a further angle α_p, instead the output bridge presents a two level AC voltage, as in the case of SPS control. The current expressions $I_L(0)$, $I_L(\alpha_p)$ and $I_L(\alpha_p + \phi)$ can be computed taking in mind the Faraday's law. Leaping some basic mathematical steps, the results are (M is the voltage ratio defined in the DAB chapter):

$$I_L(0) = -\frac{V_i}{\omega L}[M\phi + (M - \frac{1}{2})\alpha_p + \pi(\frac{1-M}{2})] \tag{7.1}$$

$$I_L(\alpha_p) = -\frac{V_i}{\omega L}[M\phi - \frac{\alpha_p}{2} + \pi(\frac{1-M}{2})] \tag{7.2}$$

$$I_L(\alpha_p + \phi) = \frac{V_i}{\omega L}[\phi + \frac{\alpha_p}{2} - \pi(\frac{1-M}{2})] \tag{7.3}$$

With this kind of modulation the transmitted power is not more directly linked to the phase shift ϕ, but it depends on both the shift between the two fundamentals of V_i and V_o (i.e. ϕ_f) and the inner variable α_p, as stated in the following equation [23]:

$$P_o = \frac{V_i^2}{\omega L} M[\phi_f(1 - \frac{\phi_f}{\pi}) - \frac{\alpha_p^2}{4\pi})] \tag{7.4}$$

in which $\phi_f = \phi + \frac{\alpha_p}{2}$. In this and next paragraphs the analysis is done considering ideal gate signals, since all the expressions derived in the DAB chapter relies on this assumption, so the duty cycle is 50%.
Looking at the current waveform the constraints to get soft switching are found:

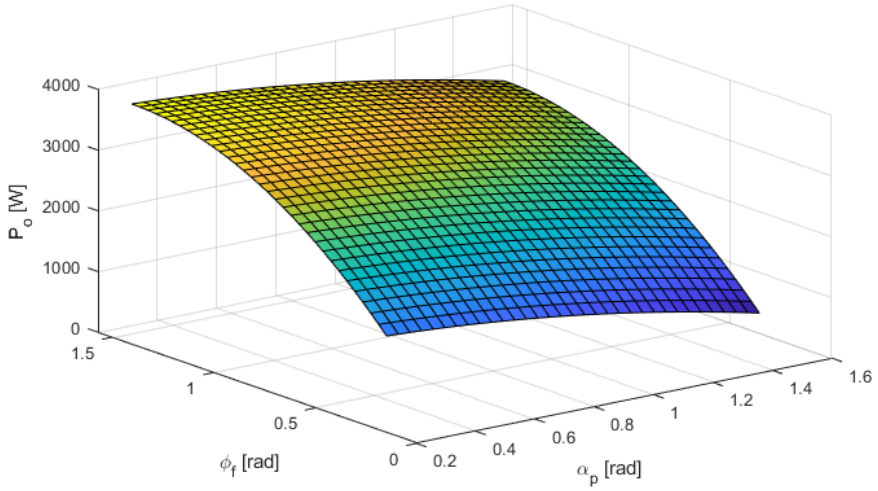


Figure 7.5: Output power as a function of ϕ_f and α_p.

- for the leading leg of the input bridge: $I_L(0) < 0$;
- for the lagging leg of the input bridge: $I_L(\alpha_p) < 0$;
- for both the output bridge legs: $I_L(\alpha_p + \phi) > 0$.

Remembering the current expressions (7.1) and (7.2) and the voltage and current waveforms, it appears that increasing the value of α_p makes the current to remains negative for more time, rising the ZVS area of the leading leg of the input bridge, but the drawback is that the magnitude of $I_L(\alpha_p)$ decreases, getting worse the soft switching in the lagging leg of the input bridge. The maximum allowable value for α_p can be computed putting equal to zero the respective inductance current and it results equal to:

$$\alpha_{p,max} = 2M\phi + \pi(1 - M) \tag{7.5}$$

The output power can be plotted as a function of both α_p and ϕ_f, in order to see which variable has the major "weight" in its variations. Looking at the surface plot 7.5 it emerges that the power changes rapidly with big variations in the phase shift ϕ_f, furthermore it has to be highlighted that the equation (7.4) becomes equal to that one got in the case of the SPS control (expressing the phase shift in radiants) when α_p is null, permitting to restore the maximum transmitted power. Putting ϕ equal to zero, the boundary values for α_p and ϕ_f are got:

$$\alpha_{p,bound} = \pi(1 - M) \tag{7.6}$$

$$\phi_{f,min} = \pi\frac{1 - M}{2} \tag{7.7}$$

Substituting the above results in equation (7.4), the power limit to get theoretically soft switching in buck mode corresponds to:

$$P_{o,zvs} = \frac{V_i^2}{\omega L}\frac{\pi}{2}(1 - M)M^2 \tag{7.8}$$

Substituting to V_i, L and M the respective values in buck mode with the minimum output voltage, it results $P_{o,zvs} = 1.62$ [kW]; in reality the minimum required power is bigger since the current $I_L(\alpha_p)$ can't be too small. If the required power becomes smaller than the boundary value (ϕ has to be negative), hard switching will appear in both the output

bridge legs; this aspect shows the small gain gets by means of this control technique.

Energy computation

As stated before $I_L(\alpha_p)$ and ϕ can't be almost null.

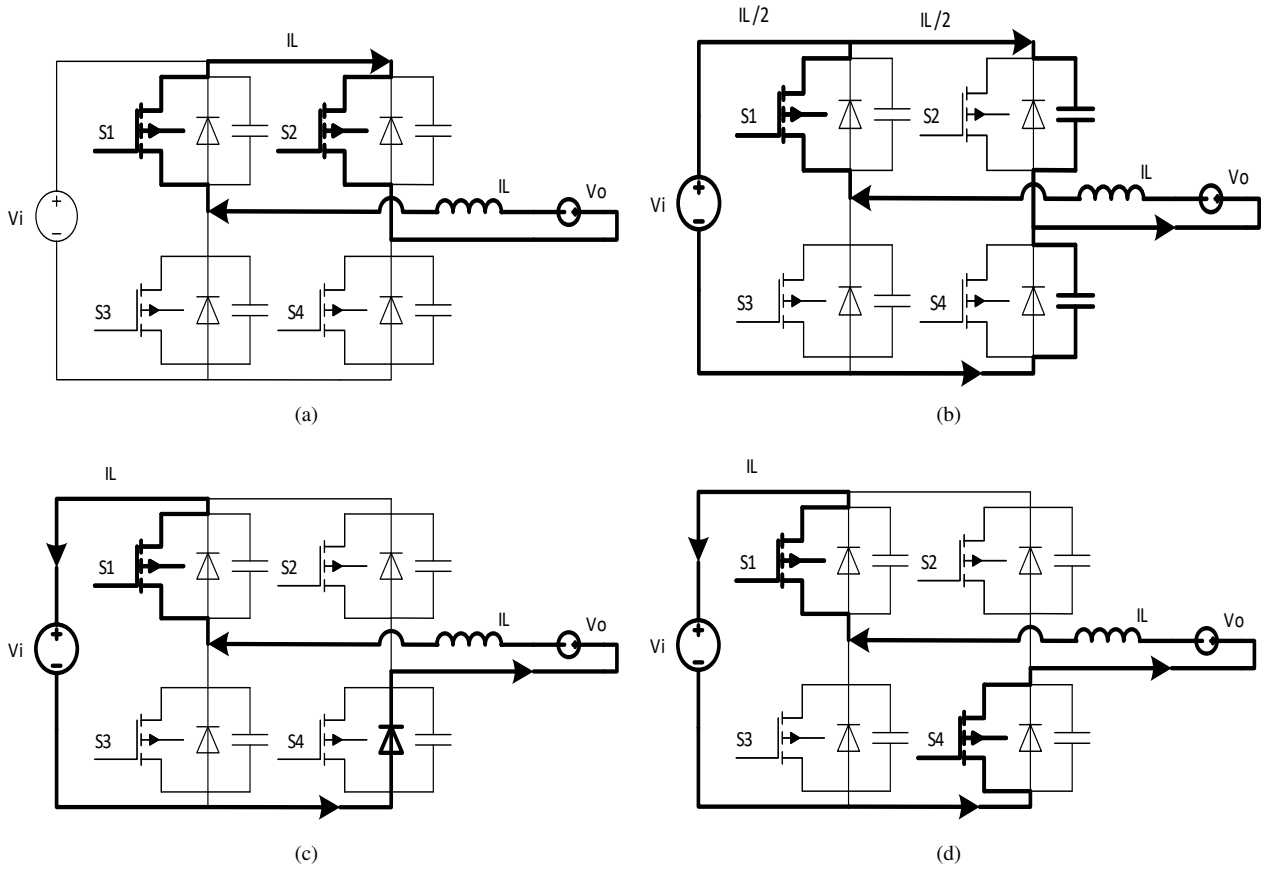


Figure 7.6: Soft switching commutation in the input bridge at α_p.

In fig. 7.6 the soft switching commutation in the lagging leg of the input bridge is shown; the inductance current is supposed to be negative for all the time interval. At the beginning the switches S1 and S2 are conducting (see fig. 7.6(a)), making null the voltage applied to the input port of the transformer; as soon as the gate signal of S2 goes down, the inductance current splits itself to charge C_{S2} and discharge C_{S4} (fig. 7.6(b)); when the voltage across the capacitance C_{S4} reaches -4.3 [V] (this one is the typical voltage threshold of GaN power devices in reverse conduction), since the current is still negative the "body" diode starts to conduct (fig. 7.6(c)) clamping the voltage at its threshold value; finally, as soon as the gate signal of S4 goes up, the current starts to to flow inside the switch and the voltage V_i becomes positive (fig. 7.6(d)). Since some energy is required to charge and discharge the capacitances, a correction in the maximum value of $\alpha_{p,bound}$ is needed, getting (as explained in [24]):

$$\alpha_p = \alpha_{p,bound} - \Delta_p \tag{7.9}$$

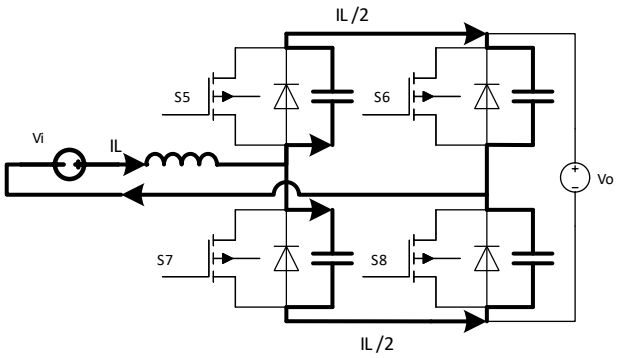


Figure 7.7: Commutation in the output bridge.

For what concern the commutation in the input bridge, the initial conditions are:

$$\begin{cases} I_L(\alpha_p) = -I_{min,Inp} \\ V_{C,s2} = 0 \\ V_{C,s4} = V_i \end{cases} \tag{7.10}$$

at the end of the resonant interval t_{off} the final conditions are:

$$\begin{cases} I_L(t_{off}) = 0 \\ V_{C,s2} = V_i \\ V_{C,s4} = 0 \end{cases} \tag{7.11}$$

In the above final conditions it has been assumed that the inductance current is null when the charging/discharging process of the capacitances is completed, in order to simplify the analysis. As shown in fig. 7.6(b) the inductance current that flows inside each capacitance is equal to: $\frac{I_L}{2} = C\frac{dV}{dt}$; during the commutation of the input bridge the sum of the energy stored in the leakage inductance plus that one supplied by the output port has to be equal to that one required by the input port, hence the following energy balance is got:

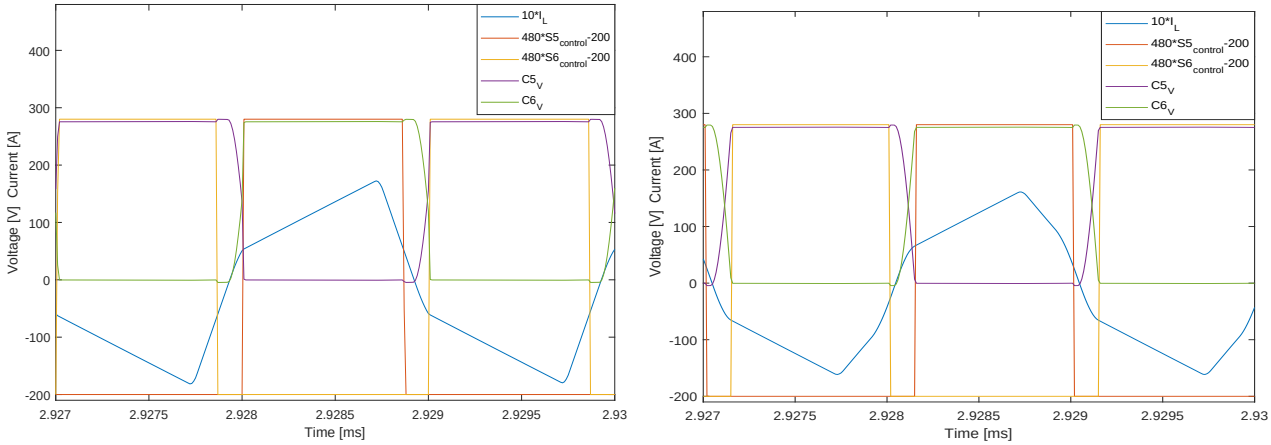
$$\frac{1}{2}LI^2_{min,Inp} + \int_{t_{off}} -V_o I_L dt = \int_{t_{off}} V_i \frac{I_L}{2} dt \tag{7.12}$$

The required time t_{off} to charge and discharge the capacitances is unknown, but the derivative of the voltage can be approximated with its maximum variation, so the above integrals are solved:

$$CV_i^2 = \frac{1}{2}LI^2_{min,Inp} - 2CV_oV_i \tag{7.13}$$

$$I_{min,Inp} = \frac{\sqrt{2V_i^2(1+2M)}}{Z_o} \tag{7.14}$$

in which Z_o represents the characteristic impedance. For what concern the output bridge commutation, since there are no freewheeling intervals, the leakage inductance current splits half in both legs, as shown in fig. 7.7; in this case the sum of energy stored in the inductance and that one delivered by the input port has to match a null value, since no



(a) (b)

Figure 7.8: Hard and soft output bridge in the case of SPS and single PWM respectively.

energy is consumed in the output port, hence the energy equation is:

$$\frac{1}{2}LI_{min,Out}^2 + \int_{t_{off}} V_i I_L dt = 0 \tag{7.15}$$

From the above equation it appears that the minimum required inductance current during the commutation of the output bridge can be considered equal to zero. In this way, substituting eqn. (7.9) into the current expressions (7.2) and (7.3) and equating them to the minimum required currents, the system below appears:

$$\begin{cases} \frac{V_i}{\omega L}(M\phi_{min} + \frac{\Delta_p}{2}) = I_{min,Inp} \\ \frac{V_i}{\omega L}(\phi_{min} - \frac{\Delta_p}{2}) = 0 \end{cases} \tag{7.16}$$

Leaping some basilar substitutions, the final expressions are:

$$\phi_{min} = \frac{\sqrt{2(1+2M)}}{1+M}\frac{\omega}{\omega_r} \tag{7.17}$$

$$\Delta_p = 2\phi_{min} \tag{7.18}$$

where ω_r is the resonant pulsation. Since the value of Δ_p is dimensionless in the Simplorer simulation it has been multiplied by ϕ_f that comes from the current control loop. To verify the advantage introduced by the single PWM control two simulations have been done: in fig. 7.8(a) the hard switching in the output bridge with SPS is shown, with an output voltage of 270 [V], an output current of 10.3 [A] and a dead time of 140 [ns]; beside in fig. 7.8(b) the soft switching condition is verified in the output bridge with the same settings except the output current that is of 9.4 [A] and the control is the single PWM, with an $\alpha_p = 36.03°$. A gain in the soft switching is got, but it's lower than expected: a smaller value of α_p would make the working condition similar to the SPS control, instead a bigger one would cause the lost of soft switching in the lagging leg of the input bridge. Also in this case a big role is played by the dead time that "shifts" the gate signals with respect the ideal case.

7.1.2 Boost mode

When the converter operates in boost mode the voltage applied to the input port of the transformer is a two levels waveform, instead that one applied to the output port has three levels, since there are some "freewheeling" intervals in which both upper switches or lower ones are conducting, due to an inner phase shift between the two legs.

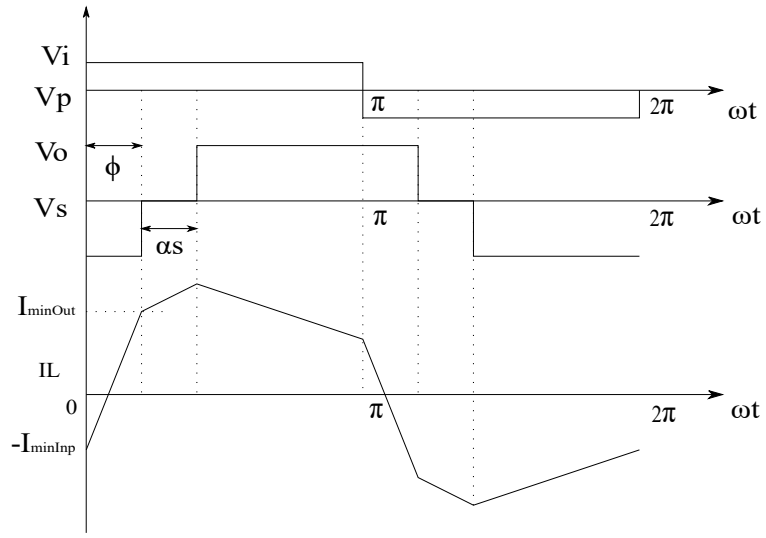


Figure 7.9: Working waveforms with single PWM in boost mode operation.

Looking at the current waveform shown in fig. 7.9, it's possible to derive the expressions of the current in three main instants:

$$I_L(0) = -\frac{V_i}{\omega L}[\frac{\pi}{2}(1-M) + M(\phi + \frac{\alpha_s}{2})] \tag{7.19}$$

$$I_L(\phi) = \frac{V_i}{\omega L}[\phi - M\frac{\alpha_s}{2} + \pi(\frac{M-1}{2})] \tag{7.20}$$

$$I_L(\phi + \alpha_s) = \frac{V_i}{\omega L}[\phi + \alpha_s(1 - \frac{M}{2}) + \pi(\frac{M-1}{2})] \tag{7.21}$$

Once again the transmitted power depends on the phase $\phi_f = \phi + \frac{\alpha_s}{2}$ between the fundamentals of the two AC voltages applied to the transformer ports; the expression of the transmitted power is the same like in buck mode, only that now the inner phase shift is applied in the output bridge. As done before, to compute the boundary values for α_s and ϕ_f the phase shift ϕ and the current $I_L(\phi)$ are put equal to zero, getting:

$$\alpha_{s,bound} = \pi\frac{M-1}{M} \tag{7.22}$$

$$\phi_{f,min} = \frac{\pi}{2}\frac{M-1}{M} \tag{7.23}$$

Substituting equations (7.22) and (7.23) in the expression of the output power (7.4), the theoretical minimum power that ensures to get ZVS in boost mode is got:

$$P_{o,ZVS} = \frac{V_i^2}{\omega L}\frac{\pi}{2}\frac{M-1}{M^2} \tag{7.24}$$

Looking at the current and voltage waveforms in picture 7.9, some remarks can be done: in the boost mode the major probability to lost soft commutations appears in the input bridge; taking in mind equations (7.19) and (7.20) it emerges that using big values of α_s it's possible to increase the range of soft switching for the input bridge, but at the same

time it gets worse in the leading leg of the output bridge, since the magnitude of the current $I_L(\phi)$ decreases rapidly; furthermore the magnitude of α_s is desired large to decrease the output power.

Energy computation

As done in the buck mode case, an energy computation is needed to define the required value of α_s and ϕ.

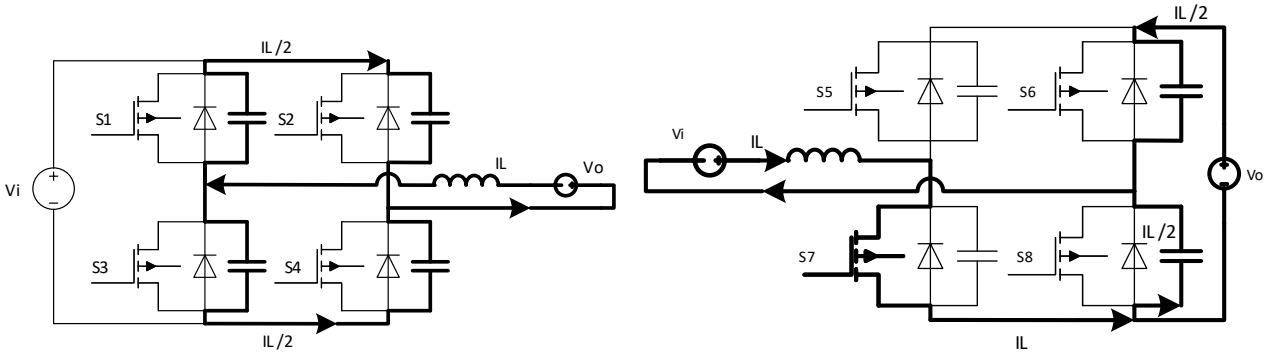


Figure 7.10: Input and output bridge commutations in boost mode.

Picture 7.10(a) shows the current distribution during the commutation in the input bridge; as it can be seen, there is no energy consumed by the input port and so the sum of the energy stored in the inductance current plus that one delivered by the output port has to be null:

$$\frac{1}{2}LI_{min,Inp}^2 + \int_{t_{off}} -V_o I_L dt = 0 \tag{7.25}$$

Solving the above equation, a minimum value of inductance current results:

$$I_{min,Inp} = 2\frac{\sqrt{V_o V_i}}{Z_o} \tag{7.26}$$

Equating $I_{min,Inp}$ (negative sign) with equation (7.19), after some rearrangements the equation below appears:

$$2\sqrt{M}\frac{\omega}{\omega_r} = \frac{\pi}{2}(1-M) + M(\phi + \frac{\alpha_s}{2}) \tag{7.27}$$

The current distribution in the case that the commutation happens in the output bridge is shown in fig. 7.10(b). In this case there's an amount of energy consumed by the output port, hence the energy equation is:

$$\frac{1}{2}LI_{min,Out}^2 + \int_{t_{off}} V_i I_L dt = \int_{t_off} V_o \frac{I_L}{2} dt \tag{7.28}$$

After some rearrangements the minimum current required during the commutation in the output bridge results:

$$I_{min,Out} = \frac{\sqrt{2V_i(V_o M - 2V_o)}}{Z_o} \tag{7.29}$$

Since M<2 (at maximum it's equal to 1.175), the above equation doesn't give a real result, for this reason the value of $I_{min,Out}$ is considered null and it's equated to eqn. (7.20). Finally, remembering eqn. (7.27), the following system is

got:

$$\begin{cases} \phi - M\frac{\alpha_s}{2} + \pi\frac{M-1}{2} = 0 \\ 2\sqrt{M}\frac{\omega}{\omega_r} = \frac{\pi}{2}(1-M) + M(\phi + \frac{\alpha_s}{2}) \end{cases} \tag{7.30}$$

Leaping all the substitution steps, the final expressions of α_s and ϕ are:

$$\alpha_s = 4\frac{\omega}{\omega_r\sqrt{M}(M+1)} - \pi\frac{1-M}{M} \tag{7.31}$$

$$\phi = 2\sqrt{M}\frac{\omega}{\omega_r(M+1)} \tag{7.32}$$

For what concern the minimum output current required to ensure ZVS, a small gain around 1[A] appears with respect the SPS control: with 470 [V] in the output bridge, hard switching in the input bridge happens when the output current is below 9.4 [A] and 8.5 [A] for the SPS and single PWM control respectively.

7.2 Dual PWM control

To overcome the limitations presented by the single PWM, the triple phase shift (TPS), also known as dual PWM, has been studied. This control technique is much more complex since a lot of modes arise depending on the relative values of α_p, α_s and ϕ, as shown in [23]. The idea to introduce at the same time an inner phase shift in both bridges arises from the need to shape the current waveform in order to get theoretically ZVS condition until almost null power.

7.2.1 Buck mode

Considering $\phi_f = \phi + \frac{\alpha_p}{2} + \frac{\alpha_s}{2} > 0$ and $M < 1$, four main modes are found and their working ranges depend on the value of the output power; as explained in [23] only the first and the fourth modes allow theoretically to get ZVS in all switches, instead the intermediate modes present hard switching in some bridges' legs. Hereinafter only the fourth mode is explored because scholars demonstrated by simulations that the rms current in the first mode is comparable to the value got in the case of SPS control, so this mode seems to not add advantages. As shown in picture 7.11 both input and output port transformer voltages are three levels square waves, with a duty cycle less than 50% since the two different inner phase shifts create freewheeling intervals. Applying the Farady's law, the main current expressions are:

$$I_L(0) = -\frac{V_i}{\omega L}(\frac{1-M}{2}\pi + M\phi_f + \frac{M-1}{2}\alpha_p) \tag{7.33}$$

$$I_L(\alpha_p + \phi) = \frac{V_i}{\omega L}(\frac{M-1}{2}\pi + \frac{\alpha_p}{2} - M\frac{\alpha_s}{2}) \tag{7.34}$$

$$I_L(\alpha_p + \phi + \alpha_s) = \frac{V_i}{\omega L}(\frac{M-1}{2}\pi + \frac{\alpha_p}{2} - M\frac{\alpha_s}{2}) \tag{7.35}$$

$$I_L(\alpha_p) = -\frac{V_i}{\omega L}(\frac{1-M}{2}\pi - M\phi_f + \frac{M-1}{2}\alpha_p) \tag{7.36}$$

The transmitted power depends on ϕ_f and α_p [23]:

$$P_o = \frac{V_i^2}{\omega L}M\phi_f(1 - \frac{\alpha_p}{\pi}) \tag{7.37}$$

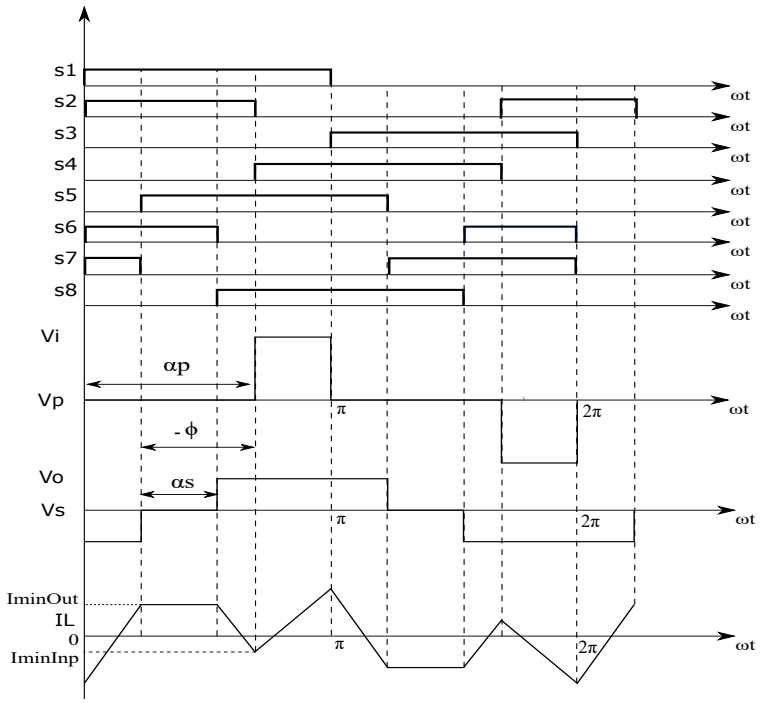


Figure 7.11: Working waveforms and switching path in the case of dual PWM control (buck mode).

Once again to achieve the ZVS in all switches (considering ideal gate signals), the following requirements have to be accomplished:

$$I_L(0) < 0 \tag{7.38}$$

$$I_L(\alpha_p + \phi) > 0 \tag{7.39}$$

$$I_L(\alpha_p + \phi + \alpha_s) > 0 \tag{7.40}$$

$$I_L(\alpha_p) < 0 \tag{7.41}$$

As done for the case of the single PWM, the boundary values $\alpha_{p,bound}$ and $\alpha_{s,bound}$ are searched. Looking at the current waveform in plot 7.11 it appears that in order to decrease the rms value of the current and the freewheeling energy inside both input and output bridges, the currents $I_L(\alpha_p + \phi)$, $I_L(\alpha_p + \phi + \alpha_s)$ and $I_L(\alpha_p)$ have to be put equal to zero, allowing to get the desired values of the inner phase shifts:

$$\alpha_{p,bound} = \pi - \frac{2M\phi_f}{1-M} \tag{7.42}$$

$$\alpha_{s,bound} = \pi - \frac{2\phi_f}{1-M} \tag{7.43}$$

Substituting equations (7.42) and (7.43) inside that one of ϕ_f it results:

$$\phi_f = \frac{(1-M)(\pi+\phi)}{2} \tag{7.44}$$

The phase between the fundamentals of V_p and V_s can reach zero when $\phi = -\pi$ and remembering the power equation (7.37) theoretically the ZVS region can be extended until zero power. On the other hand when the output power increases, ϕ increases until it becomes null and this causes $\alpha_{s,bound}$ equals to zero, hence the charger starts to work in

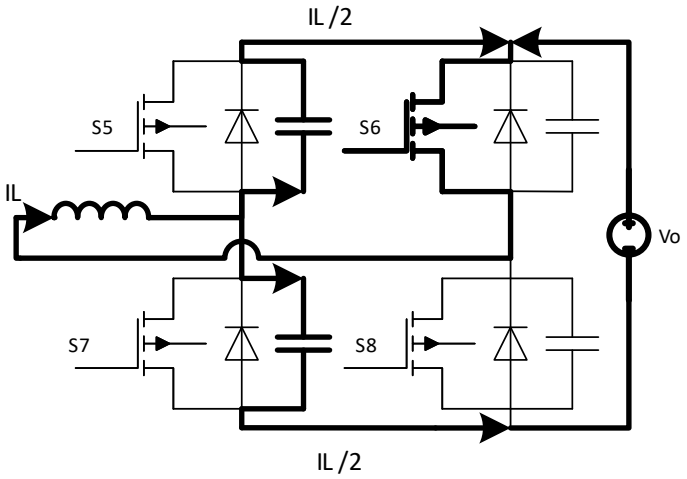


Figure 7.12: Equivalent circuit during the commutation in the output bridge at instant $\alpha_p + \phi$.

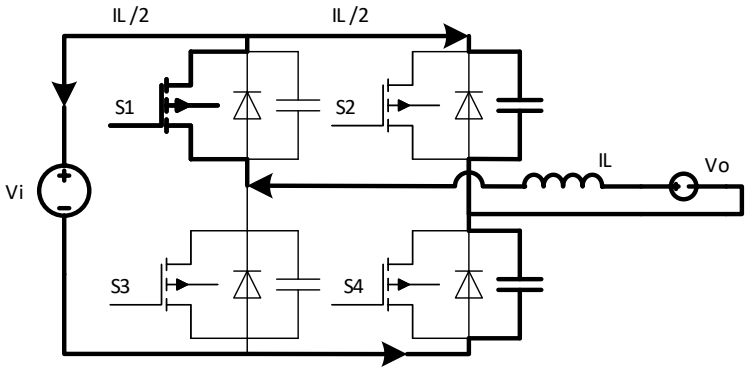


Figure 7.13: Equivalent circuit during the commutation in the input bridge at instant α_p.

single PWM modulation.

Energy computation

As in the case of single PWM some corrections have to be applied to the two boundary values of the inner phase shifts, since the current at the commutation instant can't be null but a minimum energy has to be stored in the leakage inductance to charge and discharge the parasitic capacitances. Figure 7.12 represents a simplified circuit during the commutation at instant $\alpha_p + \phi$ in the output bridge, in which $S7$ is turned off and $S5$ is turned on. Since the primary voltage is null, no energy is flowing from the input to the output bridge and the energy equation becomes:

$$\frac{1}{2}LI_{min,Out}^2 = \int_{t_{off}} \frac{I_L}{2} V_o dt \tag{7.45}$$

Remembering that $\frac{I_L}{2}$ is the current that flows inside each capacitance to discharge C_{S5} and charge C_{S7}, it results:

$$I_{min,Out} = \frac{\sqrt{2}}{Z_o} M V_i \tag{7.46}$$

Picture 7.13 shows the simplified circuit during the commutation in the input bridge at instant α_p, in which the inductance current splits itself to discharge C_{S4} and charge C_{S2}. In this case, in order to ensure ZVS in the input

bridge, the energy supplied by the output port has to be taken into account, obtaining the following energy equation:

$$\frac{1}{2}LI_{min,Inp}^2 + \int_{t_{off}} I_L V_o dt = \int_{t_{off}} \frac{I_L}{2} V_i dt \tag{7.47}$$

Remembering the expression of the current inside each capacitance, the minimum required current for the commutation of the input bridge results:

$$\begin{cases} I_{min,Inp} = \frac{\sqrt{2(1-2M)}V_i}{Z_o} & \text{if} \quad M < 0.5 \\ I_{min,Inp} = 0 & \text{if} \quad 0.5 < M < 1 \end{cases} \tag{7.48}$$

Substituting the expressions $\alpha_p = \alpha_{p,bound} - \Delta_p$ and $\alpha_s = \alpha_{s,bound} - \Delta_s$ inside the current equations (7.34) and (7.36) and equating them to the respective minimum required current, taking in mind that the minimum voltage ratio equals to 0.675, the system below is obtained:

$$\begin{cases} \frac{V_i}{\omega L}(-\frac{1}{2}\Delta_p + \frac{M}{2}\Delta_s) = I_{min,Out} \\ -\frac{V_i}{\omega L}(\frac{1-M}{2}\Delta_p) = -I_{min,Inp} \end{cases} \tag{7.49}$$

Leaping some substitution steps, the final values corresponds to:

$$\begin{cases} \Delta_p = \frac{2\sqrt{2(1-2M)}}{1-M}\frac{\omega}{\omega_r} & \text{if} \quad M < 0.5 \\ \Delta_p = 0 & \text{if} \quad 0.5 < M < 1 \end{cases} \tag{7.50}$$

$$\begin{cases} \Delta_s = 2\sqrt{2} + \frac{2\sqrt{2(1-2M)}}{M(1-M)}\frac{\omega}{\omega_r} & \text{if} \quad M < 0.5 \\ \Delta_s = 2\sqrt{2}\frac{\omega}{\omega_r} & \text{if} \quad 0.5 < M < 1 \end{cases} \tag{7.51}$$

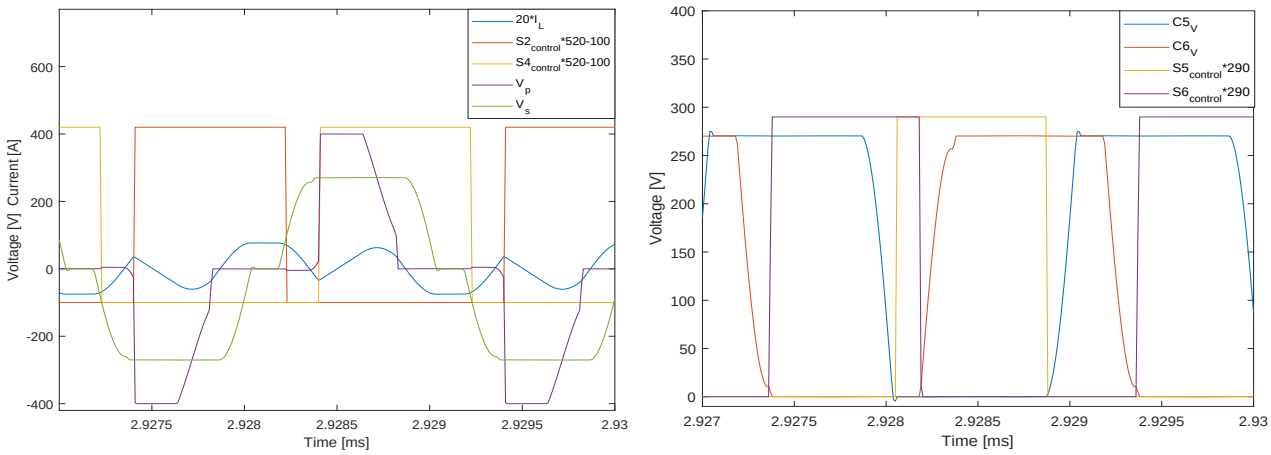
As can be seen Δ_s is dimensionless and for this reason in the simulation its value has been multiplied by ϕ_f that comes from the current control loop. Observing the current expression $I_L(\alpha_p)$ it's evident that α_p (since $M < 1$) and ϕ_f are negatively related to $I_L(\alpha_p)$ and hence some their increments could decrease the soft switching region especially in the lagging leg of the input bridge; on the other hand looking at the expression of $I_L(\alpha_p + \phi)$ it appears that an increment of α_p is useful to ensure ZVS for both legs of the output bridge, instead an increment of α_s could decrease it; finally observing the current equation of $I_L(0)$ it's possible to see that α_p is positively related to the current by means of ϕ_f and negatively by means the last term in eqn. (7.33), but the gain of ϕ_f is bigger, so it can be concluded that greater values of α_p help to get ZVS in the leading leg of the input bridge.
Taking in mind the switching path shown in fig. 7.11, a simulation in Simplorer has been done in the case of minimum voltage ratio ($V_o = 270$ [V]) with the following settings: $\phi_f = 18°$, $I_{out,avg} = 0.738$ [A] and $t_{dead} = 180$ [ns]. With this settings, the angles values are equal to:

$$\alpha_p = 105.23° \tag{7.52}$$

$$\alpha_s = 56.605° \tag{7.53}$$

$$\phi = -62.918° \tag{7.54}$$

Picture 7.14(a) shows the voltage, current and control signal waveforms (the last ones referred to the lagging leg of the input bridge, i.e. that one that experiments hard switching commutation). As it's possible to see, the shape of the current waveform is the same as in the ideal case (depicted in fig. 7.11), however hard switching occurs since the



(a) (b)

Figure 7.14: Hard switching in the lagging leg of the input bridge and almost total soft switching in the output bridge.

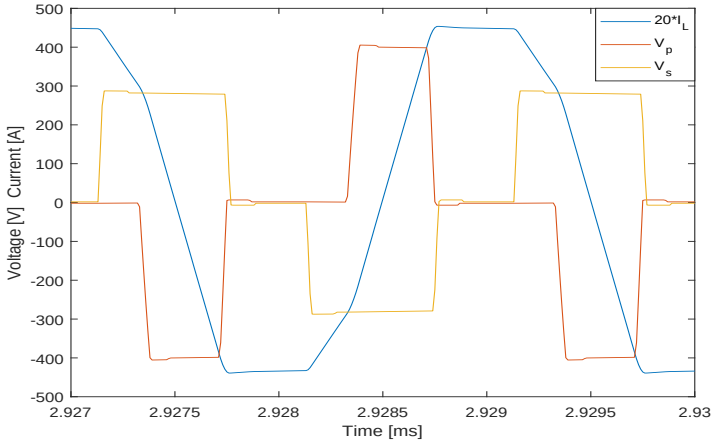
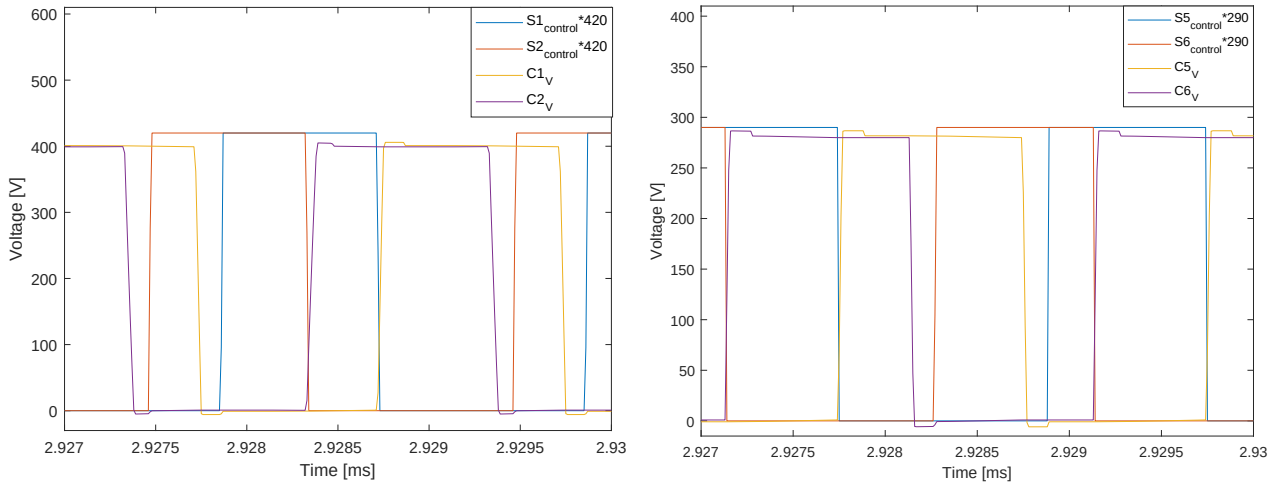


Figure 7.15: Voltage and current waveforms within ZVS in buck mode.

control signals have a duty cycle smaller than 50% due to the dead time and both go down with the wrong current sign but since the current is positive when $S2_{control}$ goes down and negative when $S4_{control}$ goes down, their anti-parallel diodes clamp the voltage (the two "teeth" can be observed in the voltage waveform V_p). Beside fig. 7.14(b) represents the almost total soft switching in both legs of the output bridge.

At this point a remark is necessary: before, in the analytical study it has been observed that the control shifts from dual PWM to single PWM when ϕ is null, since $\alpha_{s,bound}$ becomes zero. In the simulation, the control signals of $S5$ and $S6$ are delayed respectively of $t_{dead}f_{sw}360° - (\alpha_p + \phi)$ and $t_{dead}f_{sw}360° - (\alpha_p + \phi) - \alpha_s - 180°$: it appears that if $t_{dead}f_{sw}360° - \alpha_s > 0$ there is no superimposition between the two aforementioned control signal, hence it can be concluded that α_s has to be greater than $t_{dead}f_{sw}360°$ to work in dual PWM control, for this reason asking for a bigger output current, i.e. a bigger ϕ_f, would bring to shift the three levels AC secondary voltage to a two levels one, as in the case of single PWM control.

To overcome the problem introduced by the dead time and accepting a greater rms current (making bigger the switches conduction losses), a trick has been applied: instead of shifting the total output bridge of $-(\alpha_p + \phi)$ with respect the input one, it has been delayed of $-\alpha_p + \phi$, decreasing almost completely the superimposition between the two AC voltages, as shown in fig. 7.15, in this case the inductance current has a peak value around 22 [A].



(a) (b)

Figure 7.16: Soft switching in both input and output bridges.

Pictures 7.16(a) and 7.16(b) show the soft switching condition in both legs of input and output bridges. The aforementioned results appear with an output average current of 1.92 [A] and simulations demonstrated that the ZVS region extends until a value of 5 [A] with $\phi_f \simeq 17.5°$.

7.2.2 Boost mode

For what concern the boost mode a similar analysis can be done rapidly.

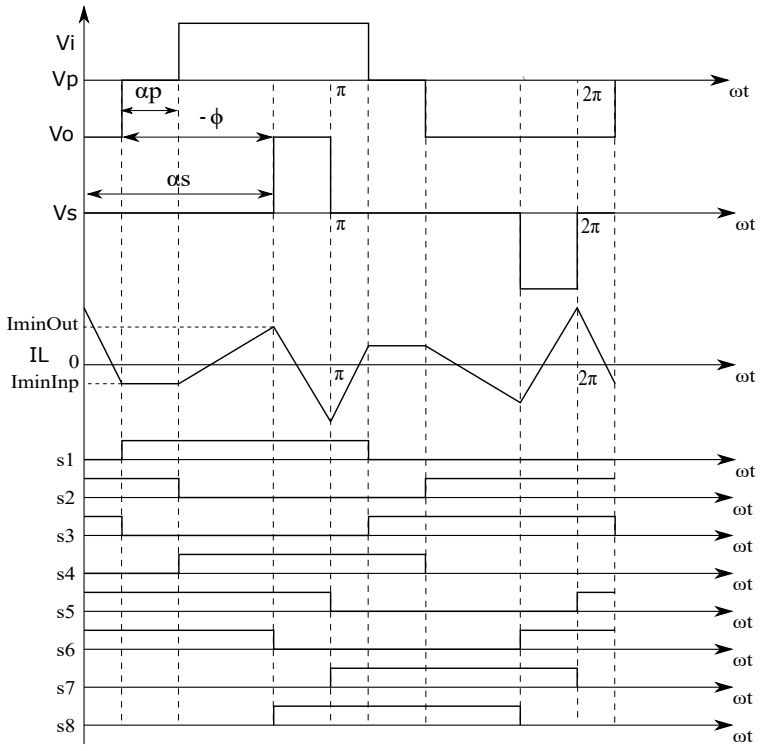


Figure 7.17: Working waveforms and switching path in the case of dual PWM control.

Looking at the current and voltage waveforms plotted in fig. 7.17 and taking in mind the Faraday's law, the following main current equations can be computed:

$$I_L(0) = \frac{V_i}{\omega L}(\phi_f + \frac{M-1}{2}\pi + \frac{1-M}{2}\alpha_s) \tag{7.55}$$

$$I_L(\alpha_s + \phi) = -\frac{V_i}{\omega L}(-\frac{\alpha_p}{2} + \frac{1-M}{2}\pi + M\frac{\alpha_s}{2}) \tag{7.56}$$

$$I_L(\alpha_s + \phi + \alpha_p) = -\frac{V_i}{\omega L}(-\frac{\alpha_p}{2} + \frac{1-M}{2}\pi + M\frac{\alpha_s}{2}) \tag{7.57}$$

$$I_L(\alpha_s) = \frac{V_i}{\omega L}(\frac{M-1}{2}\pi - \phi_f + \frac{1-M}{2}\alpha_s) \tag{7.58}$$

It appears that in order to get soft commutations in all the legs of input and output bridges, the following requirements have to be ensured:

$$I_L(0) > 0 \tag{7.59}$$

$$I_L(\alpha_s + \phi) < 0 \tag{7.60}$$

$$I_L(\alpha_s + \phi + \alpha_p) < 0 \tag{7.61}$$

$$I_L(\alpha_s) > 0 \tag{7.62}$$

In boost mode the transmitted power depends on ϕ_f and α_s:

$$P_o = \frac{V_i^2}{\omega L} M\phi_f(1 - \frac{\alpha_s}{\pi}) \tag{7.63}$$

For the same reasoning done in the paragraph about buck mode, the equations (7.56), (7.57) and (7.58) are put equal to zero, in this way it's possible to find the boundary values of the two inner phase shifts that result:

$$\alpha_{p,bound} = \pi + \frac{2M\phi_f}{1-M} \tag{7.64}$$

$$\alpha_{s,bound} = \pi + \frac{2\phi_f}{1-M} \tag{7.65}$$

Substituting the two expressions (7.64) and (7.65) into the expression of the phase shift between the fundamentals, the following equation results:

$$\phi_f = \frac{(1-M)(-\pi - \phi)}{2M} \tag{7.66}$$

As for the buck mode ϕ_f can reach zero if $\phi = -\pi$, allowing theoretically to extend the ZVS area until null power. On the other hand if ϕ becomes zero, the control will shift in single PWM boost mode, since $\alpha_{p,bound}$ decreases to zero.

Energy computation

As explained in the case of buck mode, the current expressions (7.56), (7.57) and (7.58) can't be null since it's necessary a certain amount of energy to charge and discharge the output capacitances. Figure 7.18(a) presents the equivalent circuit during the commutation in the input bridge at instant $\alpha_s + \phi$, in which $S3$ is turned off and $S1$ is turned on. Since there is no energy that comes from the output port, the energy stored in the leakage inductance has to match that one consumed by the input port:

$$\frac{1}{2}LI_{min,Inp}^2 = \int_{t_{off}} V_i \frac{I_L}{2} dt \tag{7.67}$$

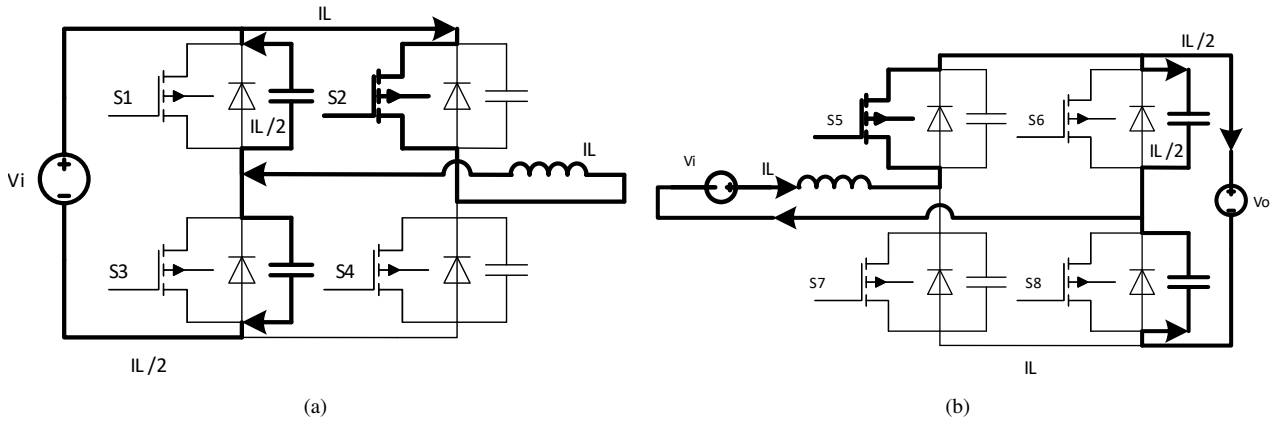


Figure 7.18: Equivalent circuits during commutations in the input and output bridges.

Leaping some basic steps, the minimum required current for the commutation in the input bridge results:

$$I_{min,Inp} = \sqrt{2}\frac{V_i}{Z_o} \tag{7.68}$$

Picture 7.18(b) shows the equivalent circuit during the commutation in the output bridge: in this case $S6$ is turned off and $S8$ is turned on. The sum of the energy stored in the leakage inductance plus that one delivered by the input port has to match that one consumed by the output port:

$$\frac{1}{2}I_{min,Out}^2 + \int_{t_{off}} V_i I_L dt = \int_{t_{off}} V_o \frac{I_L}{2} dt \tag{7.69}$$

After some rearrangements, the minimum current required for the commutation in the output bridge results:

$$I_{min,Out} = \frac{\sqrt{2V_i(MV_o - 2V_o)}}{Z_o} \tag{7.70}$$

Remembering that the maximum value of the voltage ratio is 1.175, the above equation has no real solution and for this reason it has been considered $I_{min,Out} = 0$ [A]. Equating the two values of $I_{min,Inp}$ and $I_{min,Out}$ to the current expressions (7.56) and (7.58) respectively, the following system is got:

$$\begin{cases} \frac{V_i}{\omega L}(\frac{M-1}{2}\pi - \phi_f + \frac{1-M}{2}\alpha_s) = 0 \\ \frac{V_i}{\omega L}(-\frac{\alpha_p}{2} + \frac{1-M}{2}\pi + M\frac{\alpha_s}{2}) = \sqrt{2}\frac{V_i}{Z_o} \end{cases} \tag{7.71}$$

Making some substitution steps, the final values for α_s and α_p are obtained:

$$\alpha_s = \frac{2\phi_f}{1-M} + \pi \tag{7.72}$$

$$\alpha_p = \pi + \frac{2M\phi_f}{1-M} - 2\sqrt{2}\frac{\omega}{\omega_r} \tag{7.73}$$

Looking deeply the expressions of α_p and α_s and remembering that M=1.175 when $V_o = 470[V]$ it emerges that the two inner phase shifts can become negative if big values of ϕ_f are applied, shifting the control to SPS. Also in the boost mode, like the buck one, the dead time plays a crucial role.

8 Conclusion

In this thesis the dual active bridge DC/DC converter has been studied and tested. The steady state working conditions have been presented in detail and a charger efficiency characterization during the battery charging process has been computed: from the analytical computation appears that power losses rapidly increase when the converter works in buck and boost modes with small current values.
A high frequency transformer (500 [kHz]) with integrated leakage inductance has been designed, trying to both minimize the volume, the copper and core losses, ensuring a leakage inductance enough big. Furthermore a small signal model has been derived in order to tune the current and voltage control loops in the simulations. After that the circuit has been turned on in order to see its behaviour (power losses, transformer and switches maximum temperatures, hard switching) in each possible operating point during the whole charging process, shifting from buck to matching mode and finally to boost one.
It has been observed that hard switching power losses cause a big loss of efficiency and could damage the power devices; for this reason the final step of this work has been to simulate the circuit behaviour with different control techniques, in order to find out how to bypass the problems related to the single phase shift modulation: it emerges that although theoretically it's possible to extend the ZVS area until zero output power with the dual PWM control, in reality the dead time effects make this assumption "weak".

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