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Monolithic Millimeter-Wave Frequency Multipliers

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1 Introduction

1.1 Imaging System

The field of imaging for radar, imaging system security, medical and industrial applications is receiving more and more interest and thanks to the advances of silicon technology, high integration densities are possible even at mm-wave ranges. A highly integrated radar chip minimizes the number of critical millimeter-wave interfaces improving the performance of devices.

The cost for the millimeter-wave chipset and for testing is a major part of the sensor cost. Silicon-based technologies allow higher integration levels and improve testability with a significant cost reduction.

In the range of millimeter wavelength, the W-band covers a frequency range from 75 to 110 GHz which is used for satellite communication, imaging, millimeter radar and military/industrial applications. Development in silicon semiconductor technology make active and passive components available in integrated SiGe circuits fabricated for mass market and for frequency up to 200 GHz and beyond. The low cost of silicon and high quality enable it to be a good substitute of the semiconductors based upon III-V compound semiconductors which have been dominated during the past years these frequency ranges. At the same time, SiGe technologies achieve much higher f_T and f_{max} values than CMOS technologies at the same lithography node [Knapp:08].

As frequency increases into the millimeter wave range it becomes increasingly difficult to build fundamental frequency oscillators with good power, stability and noise characteristics. An alternative approach, which increase the flexibility of the system, is based on the frequency multiplication by using a low phase noise oscillator with a high spectral purity at lower frequencies [Poza:05]. Frequency multipliers are attractive for their building cost-effective and stable sources at high frequency as long as technology allows comparable or better results using direct realization of oscillators at the same frequencies [Altaf:07].

Disadvantage of frequency multipliers is the output noise level which increase ideally by $20\log(N)$ with N frequency multiplication factor, thereby for a doubler the output noise floor increase by 6dB while for a octupler by 18 dB.

For imaging applications, range resolution d_{max} is a fundamental point, which depends on relationship $d_{max} = \frac{c}{2B}$ where c is the speed of the light, B the bandwidth and $1/2$ is due to the two way travel time [Altaf:07]. To achieve a wide bandwidth in a ranging system, which is traduced is a better range resolution, frequency multiplier system based is preferred over a VCO/PLL especially at high frequency since the band provided is higher.

1.2 Objective of this Work

The aim of this work is to design and layout a frequency multiplier $\times 8$, hereafter called octupler, in Infineon's SiGe:C B7HF200 Bipolar Technology.

Since the octupler is composed by a chain of three frequency doubler and an output buffer, a careful design has to be done in order to achieve a high spectral purity.

Due to the nature of the frequency multipliers and the input signal frequency as well, the operative frequency range from input (X-Band) to output (W-Band) is such broad that different solutions at different frequencies must be used. This is due to signal wavelength within the transmission line. Up to 20 GHz the wavelength in silicon dioxide is longer than 7 mm so transmission line on chip cannot be used efficiently and the choice must fall on lumped elements like inductors. Vice versa, for frequencies higher than 40/80 GHz transmission lines are suitable, concurring with their use, since inductor design at these frequencies is costly in terms of modeling, self resonance and quality factor, whereas (since the wavelength is of few millimeters) with transmission lines shorter than $\lambda/10$ already a good inductance can be provided with low area occupancy at the same time.

In a frequency range within 20-40 GHz, there's a trade-off between lumped and distributed solution. Inductor based design needs many iterations to achieve optimal performances, but its electromagnetic behavior is well known. If more than one inductor is implemented in the same chip, a careful layout has to be done in order to avoid coupling between each other. Transmission lines are easy to design, model and layout, but the turns act as discontinuities which are site of reflections and losses that are not possible or easy to simulate during the design process. The major tradeoff is played on the area occupancy between these two options.

Since different solutions has been discovered, two different octuplers has been designed and layouted, hereafter called *capacitive (Cap)* and *inductive (Coil)* version. Each octupler chip implements a cascade of three frequency doublers, an output buffer and a power detector (in fig. 1.1 not shown). Doubler no. 1, 2, 3 has an output frequency respectively of 20, 40 and 80 GHz.

Different solutions have been investigated in order to provide 90° phase shift between LO and RF signal path in each doubler, to achieve the maximum performances in terms of conversion gain and spurious suppression.

The difference between octuplers *Cap* and *Coil* version lies in the doubler no.2, the 40 GHz frequency doubler, which is different for each version.

The octupler name is taken from the version of 40 GHz doubler used.

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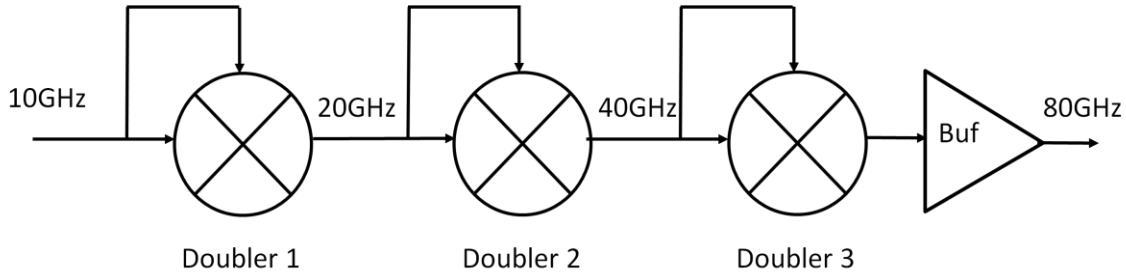


Fig. 1.1: Top view schematic of the octupler *Cap/Coil* version.

To achieve the phase quadrature (90°) between LO and RF signals, the first doubler implements an active phase shift network made of one stage of emitter followers. The second and third doubler own a passive network which will be shown afterwards.

The main difference between the two 40 GHz frequency doublers versions consist in the phase shift network implemented. In the *Cap* version the delay is provided using a distributed network composed of transmission lines and capacitors; in the *Coil* one, the phase shift occur from resonance between inductor and base-emitter transistor capacitance.

The third doubler implements a distributed LC low pass filter.

Since the output buffer and power detector are library components, their design and layout will not be discussed.

During this work five chips have been designed and layouted. The 80 GHz frequency octuplers *capacitive/inductive* versions chips implement each one: three frequency doublers, output buffer and power detector. The third chip implements the 80 GHz frequency doubler and output buffer. The fourth chip implements the 40 GHz frequency doubler *inductive* version standalone. Fifth chip the 20 GHz doubler standalone. The chips don't include the input matching network, so as fig. 1.1 depicts, the input port of doubler no.1 is directly connected to the input pads. The same reasoning is valid for the other chips.

Target specifications for the frequency octupler are given in Table 1.

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Parameter	Min	Typ	Max	Unit/Comment
Input Frequency	9.37		10.62	GHz
Output Frequency	75		82	GHz / 3 dB bandwidth
Input Power	0			dBm
Spurious harmonic suppression	30			dBc/Input and Output
Input Impedance		50		[Ω] / Single-ended
Output Impedance		100		[Ω] / Differential
S11, S22			-10	dB
Supply Voltage	-5%	3.3	+5%	V
Temperature range	25		95	$^{\circ}$ C

Table 1: Frequency octupler target specifications.

Phase noise is not specified for a frequency doubler, since in the ideal case the output phase noise is given by:

$$\text{Output Phase Noise} = \text{Input Phase Noise} + 20\log N$$

Where N is the multiplication factor. In this work N=8, therefore the output phase noise increase ideally by 18 dB respect to the input one.

Indeed, took an oscillator as input source, it has amplitude and phase fluctuations:

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$$u(t) = A(t) \cos[\omega(t)t] = A(t) \cos \left[\omega_0 t + \frac{d\phi(t)}{dt} t \right] \quad (1.1)$$

And the noise spectral density of the signal is:

$$S_\phi(f) = 10 \log \Delta\phi_{rms}^2 = 20 \log \Delta\phi_{rms} \quad (1.2)$$

Then after multiplication per N results:

$$v(t) = B_0 \cos[N\omega_0 t + N\Delta\phi(t)] \quad (1.3)$$

Hence the output noise spectral density become:

$$S_\phi^n(f) = 20 \log(N\Delta\phi_{rms}) = 20 \log N + 20 \log \Delta\phi_{rms} \quad (1.4)$$

From (1.4) the term $20 \log N$ is the phase noise degradation due to the multiplication factor. In addition, the output noise is deteriorate from the noise introduced by the doublers and the output buffer.

The input power of 0 dBm on the input impedance of 50Ω produce a peak to peak differential voltage of $\sim 300\text{mV}$. This swing is such to drive with large signal the transistors in the LO stage. Since the input source is common for both RF/LO stages, also the RF stage is driven by large signal. Large-signal condition change the transistor voltage-dependent parameters respect to the small signal analysis. Therefore the results of the linear approach on the RF stage are used as first design and have to be further optimized by large signal analysis.

2 Silicon Germanium Bipolar Technology

2.1 Infineon's B7HF200 Technology

SiGe bipolar is the technology of choice for many high frequency applications like mobile communications, optical data communications at 10 and 40 Gbit/s, or microwave radio links. Advances in technology development enabled impressive transistor parameters like maximum oscillation frequencies and transit frequencies in excess of 300 GHz and even gate delay times down to 3.6 ps. Since its costs are lower than the other technology III-V based, the address of this technology is especially for the automotive industry. SiGe bipolar technology is optimized for a balanced compromise between the most important transistor parameters to achieve good circuit performance at 77 GHz. Special care has been taken on manufacturability and reliability to achieve the high quality requirements needed for automotive applications [Böck:04]. In table 2.1 the key process features are shown.

B7HF200: Key Process Features

■ Process type	200 GHz SiGe Bipolar
■ Lithography node	0.35 μm
■ Substrate	p, 20 Wcm, 8"
■ Isolation	Deep & Shallow Trench
■ Effective emitter width	0.18 μm
■ Base Layer	SiGe:C
■ Metallization	4 layers of Copper Metal + 1 top layer of Al Metal
■ Bonding Pads	Au
■ Devices	UHS / HS / MS / HV NPN, Poly-R, Met- R, MIM-Cap, Varactor, VPPN

Table 2.1: Key process features.

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To enable high performance circuit design, three types of NPN devices with different $f_T - BV_{CE0}$ trade-offs are available, modifying the collector implant dose [Böck:04]. Ultra high speed (UHS) transistor has got a 200 GHz transit frequency, but due to its low breakdown voltage $BV_{CE0} \geq 1.2V$ its use is problematic. High speed (HS) transistor, the most common used in this work, since its $f_T = 170$ GHz is still high enough to provide gain and at the same time $BV_{CE0} \geq 1.4V$ results less troublesome. High voltage transistor (HV) with $f_T = 35$ GHz and $BV_{CE0} \geq 3.8V$ result useful especially at low frequency for some applications as will be shown in the next chapters. Vertical pnp (VPNP) used for bias network.

Figure 2.1 shows the cross section view of an NPN transistor of Infineon SiGe:C B7HF200 Technology.

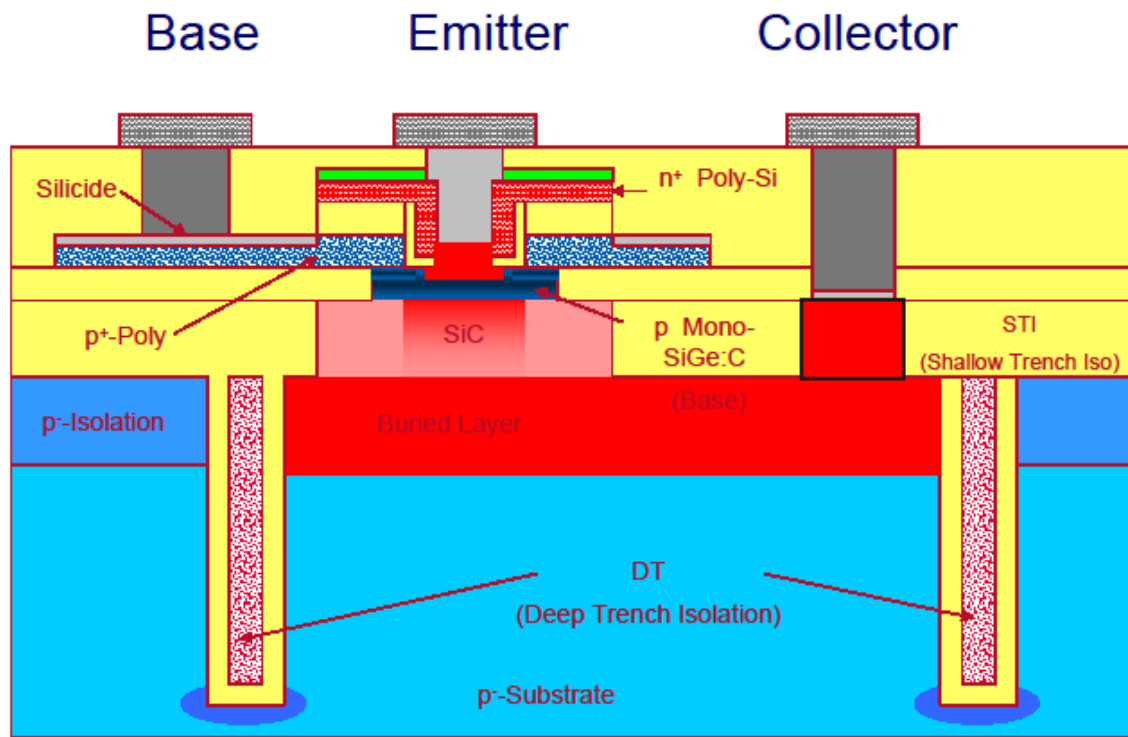


Fig. 2.1: NPN transistor cross section view.

This process is based on a double-polysilicon selfaligned transistor configuration with a selective epitaxial grown SiGe base layer. "Double-polysilicon" means that both, emitter and base contact are realized with polysilicon. This configuration exhibits low parasitic capacitances and a low extrinsic base resistance. The term "self-aligned" refers to the emitter-base isolation which is realized by thin dielectric layers [Perndl:04,2]. The emitter-base isolation has been improved to increase the base current ideality and the manufacturability of the technology. The transistor have a monocrystalline emitter contact to guarantee a small emitter resistance and a reproducible interface between emitter contact and active silicon area [Böck:04].

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Further, the collector-substrate capacitance is reduced by more than 40% by introducing deep trench (DT) and shallow trench isolation. The integration of Ge into the base of the transistor enables bandgap engineering and the fabrication of heterojunction bipolar transistors (HBTs) in silicon-based materials. In the SiGe HBT, germanium is selectively introduced into the base region of the transistor. The smaller base bandgap of SiGe compared to Si enhances electron injection, producing a higher current gain for the same base doping level compared to a Si device. Thus, the base can be doped more heavily in the SiGe HBT in order to lower the total base resistance. At the same time, the Ge content is graded across the base in order to achieve an accelerating drift field for the electrons to increase the cutoff frequency. A doping profile of the fabricated transistors is shown in Fig. 2.2. The N-type emitter is typically doped with arsenide (As), the doping material for the N-type collector is typically phosphor (P), and as acceptor material for the P-type base usually boron (B) is used. At the emitter side the base is lowly doped in order to obtain a small emitter-base capacitance. For realizing high cutoff frequency the thickness of the boron spike must be kept as thin as possible. The incorporation of carbon into the highly boron-doped SiGe base prevents the broadening of the base profile by subsequent processing steps [Perndl:04,2].

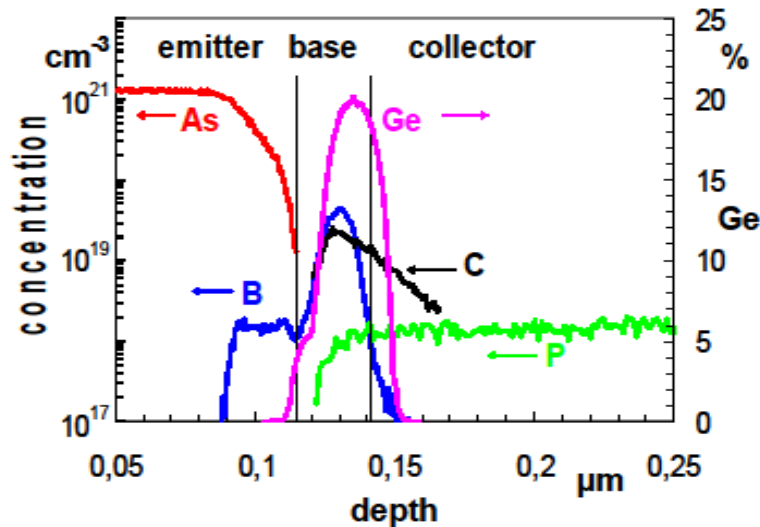


Fig 2.2: Transistor doping profile.

2.2 Electrical Characteristic

Figure 2.3 shows the common emitter DC output characteristics of High Speed Transistors with an effective emitter area of $0.18 \times 2.6 \mu\text{m}^2$. The collector-emitter breakdown voltage BV_{CE0} , which is measured with open base, is 1.7V and the open-emitter collector-base breakdown voltage BV_{CB0} is 5.8 V.

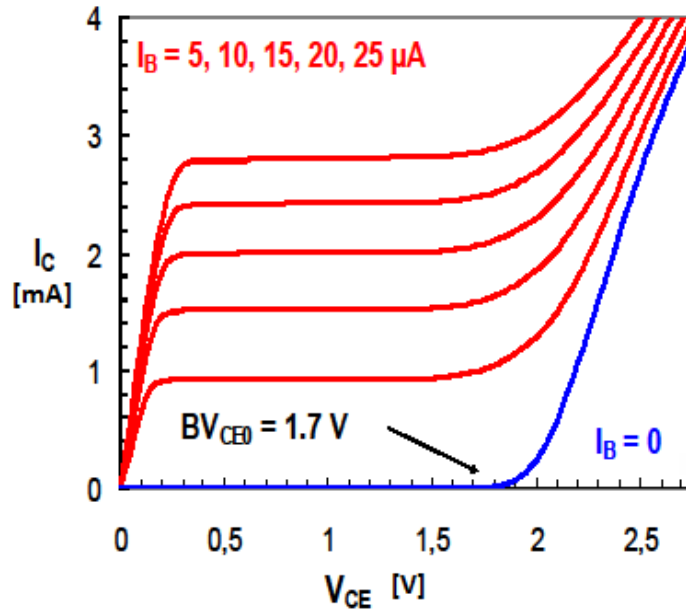


Fig 2.3: Output characteristic I_C vs. V_{CE} .

The cutoff frequency f_T has been extrapolated from the small signal current gain using Ultra High Speed Transistor with an effective emitter area of $0.18 \times 2.6 \mu\text{m}^2$. Figure 2.4 shows the dependency of cutoff frequency f_T on the collector current I_C for different base collector voltages V_{BC} . The transit frequency reaches its maximum of 200 GHz at $V_{BC} = 0\text{V}$ and a collector current density of $7.5 \text{ mA}/\mu\text{m}^2$.

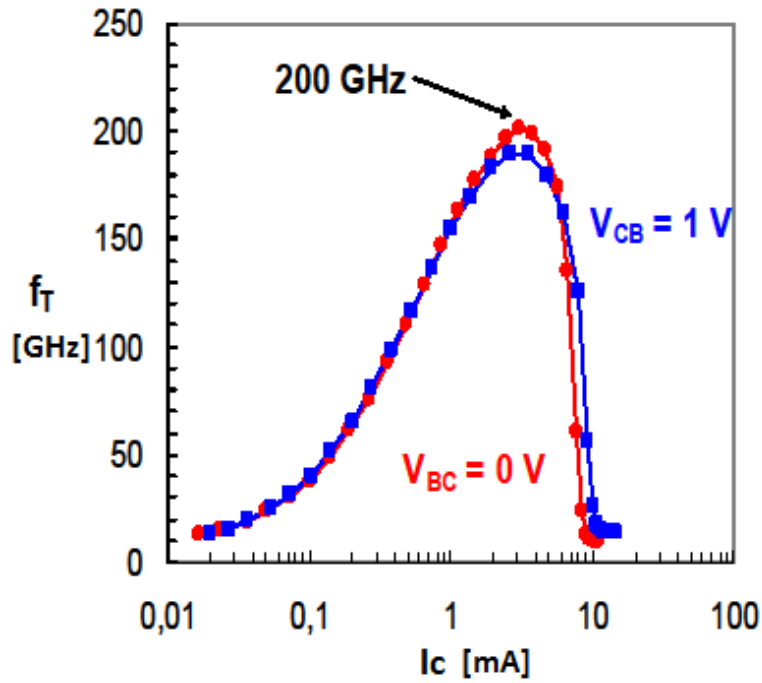


Fig. 2.4: Cutoff frequency f_T vs. collector current I_c .

Figure 2.5 shows the dependency of the maximum oscillation frequency on collector current. At $V_{BC} = -1$ V the maximum oscillation frequency peaks at 275 GHz.

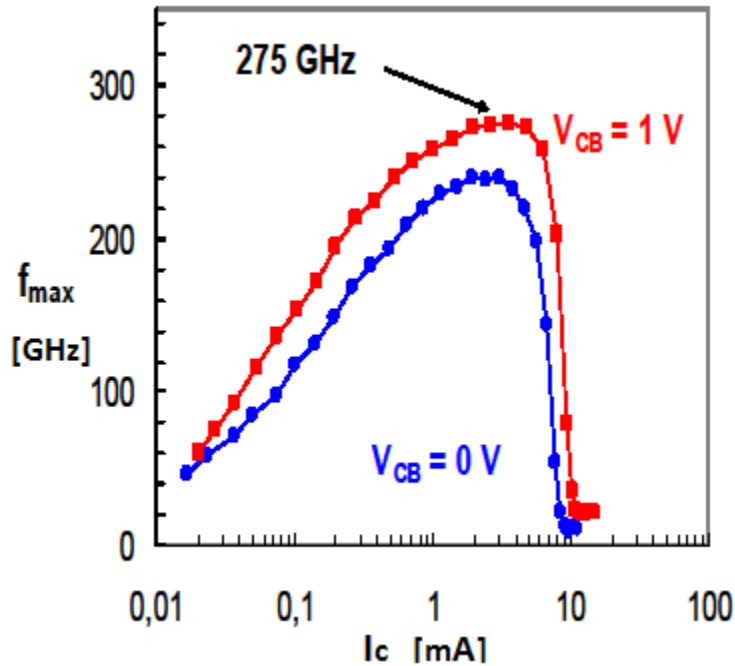


Fig. 2.5: Maximum oscillation frequency f_{MAX} vs. collector current I_c .

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The high values of f_{MAX} originate from the integration of thin base layer into a self-aligned transistor architecture providing low capacitances and extrinsic series resistances as well as a careful optimization of the highly boron doped base for achieving simultaneously high cutoff frequency and low base sheet resistance [Perndl:04,2].

Transistor Geometries

The choice of the correct transistor geometry is of great importance in order to minimize the influence of parasitic capacitances and resistances. In case of maximizing the high frequency capability of the transistor, the optimum collector current $I_{C,OPT}$ is defined by the effective emitter area and the collector current density at maximum cutoff frequency. In this case, the emitter width is usually chosen as small as possible, according to the design rules, in order to assure the lowest base resistance which is possible. The emitter length results from the desired collector current. The ratio of the “external” to the “effective” emitter area of transistor becomes worse as the transistor area is reduced.

Base, emitter and collector contacts can be arranged in various ways, for bipolar transistors the contacts are typically arranged as parallel bars, because this configuration exhibits a good tradeoff between all transistor parameters. The double base transistor (BEBC) shows a reduced base resistance compared to the single base transistor (BEC), because the base is contacted from both sides. However the base-collector capacitance of this configuration is higher, because there is a larger overlap between collector and base contact. The collector-substrate capacitance is increased as well, because of the larger buried layer area. Further, there is a higher collector contact resistance because the distance between active transistor and collector contact is enlarged [Perndl:04,2].

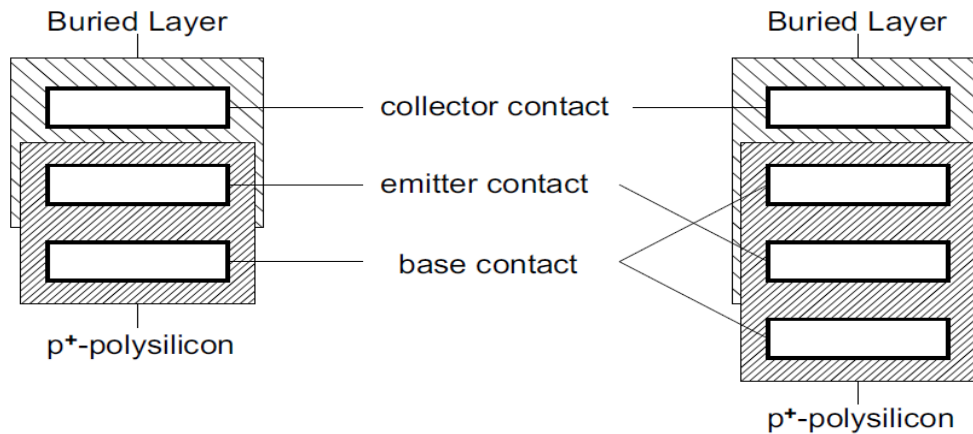


Fig. 2.6: Single and double base transistor configuration.

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In RF circuits such as mixers Gilbert cell based, the main sources of thermal noise in RF and LO stages are the transistors base resistance r_b . A method for reduce its impact is to use devices with multiple base configuration [Trotta:07,1].

In the Gilbert cell, the transistors collector of LO stage are crosswise connected. In order to reduce the parasitic effects due to interconnection layer and to reduce the area occupancy, a double transistor with one collector shared has been used BECEB. Fig. 2.7 shows the BECEB transistors configuration with the collector shared.

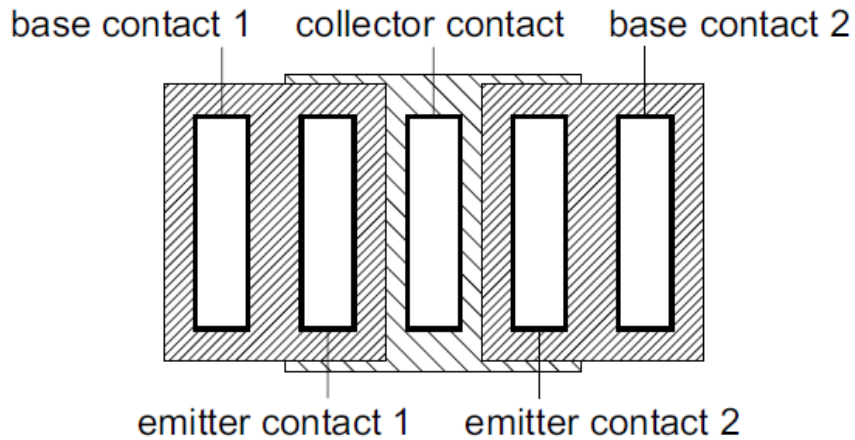


Fig. 2.7: Double transistor with the same collector contact, BECEB configuration.

Passive Devices

To enable high performance circuit applications several additional devices have been added to the high frequency NPN transistors. Three types of resistors and a MIM capacitor are available. Two poly resistors with sheet resistances of 150, 1000 Ohm/sq and a high precision TaN thin film resistor with 20 Ohm/sq. A MIM capacitor with an Al_2O_3 dielectric and a specific capacitance of $1.4 \text{ fF}/\mu\text{m}^2$ is integrated between the second and third metallization layer. The TaN metal resistor is placed between the first and the second copper metallization layer [Böck:04] [Perndl:04,2].

2.3 HBT Transistor Model

The design of radio-frequency integrated circuits require a model of bipolar transistor for an accurate design. Here the large signal model is not shown since it doesn't reflect well large signal operations for high current rate. For signal levels smaller than bias currents and voltages, a small-signal model linearized around the bias point can be used, which allow calculation of gain and terminal impedances without the necessity of include the bias quantities [Gray:01].

2.3.1 Small Signal Model

In forward operation, a small signal model can be derived based upon the bias conditions. For reliable results a complete small signal model should be used, since at this frequencies (order of tens/hundreds GHz) the parasitic effects due to r_c , C_{CS} , C_μ start to be considerable. However, as first analysis, they can first be neglected and only afterwards their effects can be considered by support of simulation.

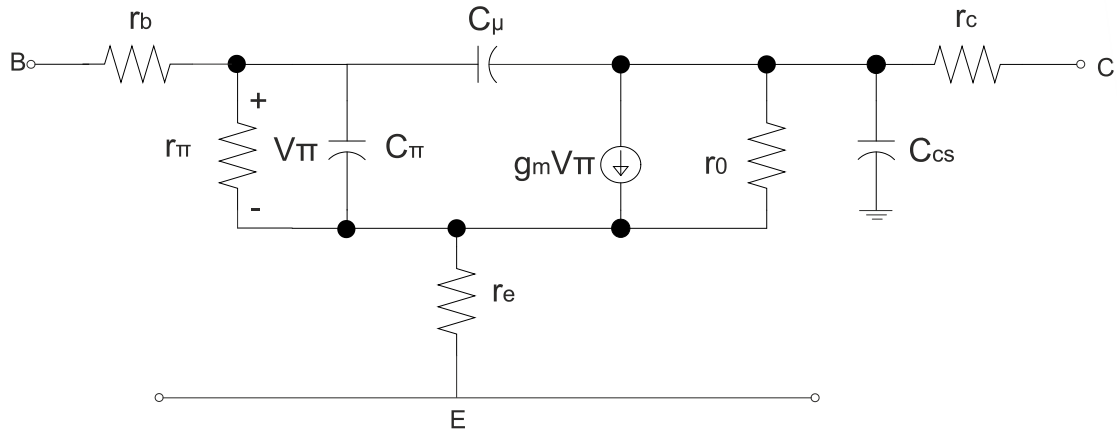


Fig. 2.8: Complete bipolar transistor small signal equivalent circuit.

The small signal parameters are given by the relationship:

$$r_\pi = \frac{\beta_0}{g_m} \quad (2.1)$$

$$C_\pi = C_{je} + \tau_F * g_m \quad (2.2)$$

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Where β_0 is the small signal current gain, g_m the transconductance, C_{je} the depletion capacitance of the base-emitter junction and τ_F the base forward transit time. The output resistance and base-collector capacitances are given by:

$$r_o = \frac{1}{\eta g_m} \quad \text{with } \eta = \frac{kT}{qV_A} \quad (2.3)$$

$$C_\mu = \frac{C_{\mu 0}}{\left(1 - \frac{V}{\psi_0}\right)^n} \quad (2.4)$$

Where V is the forward bias to the base-collector junction and n is an exponent between about 0.2 and 0.5 [Gray:01].

The other parameters such as r_b, r_e, r_c, C_{CS} are mainly given by the technology, in table 2.2 are shown for a High Speed NPN transistor with $f_T = 200 \text{ GHz}$.

Emitter Area	0.14 x 2.6 μm^2
β	250
BV_{CE0}	1.7 V
BV_{CB0}	5.8 V
C_{EB}	6.3 fF
C_{BC}	5.5 fF
C_{CS}	3.7 fF
R_B	50 Ω
R_E	3.5 Ω
R_C	7.5 Ω

Table 2.2: Device parameters of the High Speed NPN.

3 Frequency Multiplier

3.1 Frequency Multiplier Architecture

RF frequency multipliers are devices that produce an output signal with a frequency larger than that one corresponding to the input thanks to their nature to be nonlinear devices. They operate in a specific band of the input signal and are able to reduce the unwanted harmonics from the output signal. This feature, the harmonics spurious suppression at the output, is one of the main goal of the frequency doublers that is going to be presented.

There are two basic types of multipliers, passive and active. Passive RF multipliers, as it can infer from the name, is a kind of circuits with zero DC power consumption which provide negative conversion gain (dB refereed). Their use in a chain of doublers should be avoid, since they need one or more stages of amplification to regenerate the signal increasing the circuit complexity and the power consumption. Active RF multipliers are more attractive since they provide frequency multiplication together with positive conversion gain allowing to cascade several doublers without losing the signal integrity.

In the field of active RF multipliers, to generate upper harmonics there are two main approaches: by exploiting the intrinsic non-linearities within the semiconductor device, or using a Gilbert mixer cell where the frequency multiplication is made by a time varying current path.

Obviously for achieve good even order spurious suppression and a high common mode rejection ratio a fully differential architecture has been chosen.

The circuit topology chose, which can provide at the same time positive conversion gain, good spurious/fundamental suppression and good CMRR is based on the Gilbert cell double balanced mixer [Gilbert:68].

3.2 Starting Topology Circuit

Fig. 3.1 shows the basic starting topology from which this work is begun. It shows the Gilbert Cell [Gilbert:68] which is formed by two stages: the transconductance one, called RF stage (T21, T22) and the mixing core called LO stage (T1,T0).

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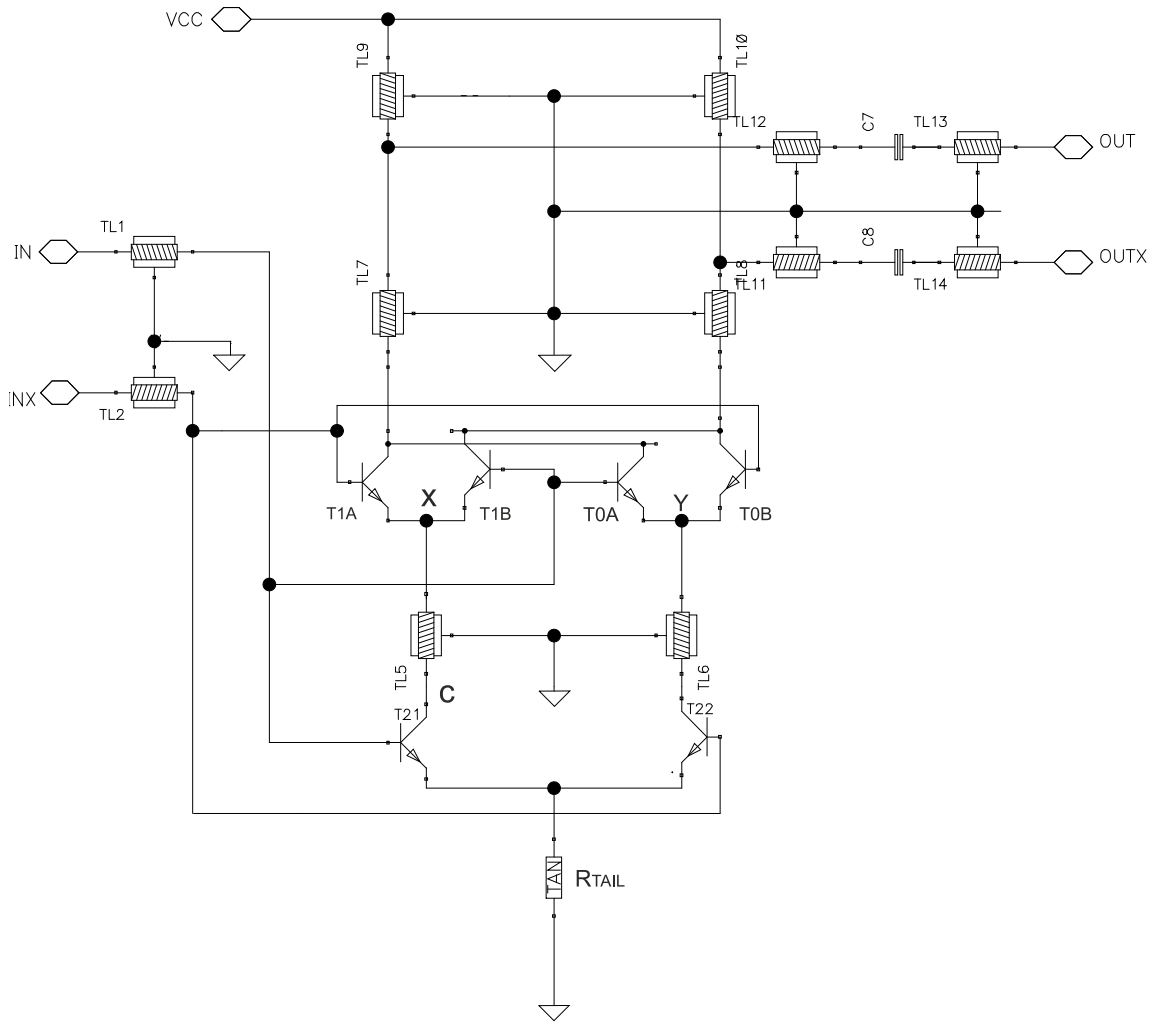


Fig. 3.1 Gilbert cell as frequency doubler.

Since the circuit works as frequency doubler, both RF and LO stages are driven from the same common source at the input terminals IN/INX and the output frequency $2f_0$ is double respect to the fundamental one f_0 at the input. TL1, TL2 are the input transmission lines, which together with the output matching network of previous doubler realize the voltage matching. C_8, C_7 are the DC blocking capacitors while R_{TAIL} is the tail current source. The effects of TL5,6 on the circuit performance will be discussed afterwards.

RF stage is a transducer which convert the input voltage $V_{id} = V_{IN} - V_{INX}$ into a output current $I_{o,RF} = I_{c,T21} - I_{c,T22}$ by the follow relationship [Gray:01]:

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$$I_{c,T21} = \frac{I_{EE}}{1 + \exp\left(\frac{-V_{id}}{V_T}\right)} \quad (3.1)$$

$$I_{c,T22} = \frac{I_{EE}}{1 + \exp\left(\frac{V_{id}}{V_T}\right)} \quad (3.2)$$

Where I_{EE} is the (tail) DC bias current which flows into resistor R_{TAIL} .

Assuming that the forward current gain $\beta_F = \frac{I_C}{I_B}$ is well higher than 1, the base current can be neglected, so combining formulas (3.1)-(3.2) the differential output current versus input differential voltage becomes:

$$I_{o,RF} = I_{c,T21} - I_{c,T22} = I_{EE} \tanh\left(\frac{V_{id}}{2V_T}\right) \quad (3.3)$$

If V_{id} is smaller than thermal voltage V_T , the RF stage works in linear zone so the small signal analysis can be used and the output spurious harmonics suppression achieved is good.

$$I_{o,RF} = I_{EE} \tanh\left(\frac{V_{id}}{2V_T}\right) \approx I_{EE} \left(\frac{V_{id}}{2V_T}\right) \quad \text{for } \frac{V_{id}}{2V_T} \ll 1 \quad (3.4)$$

For a driver input signal V_{id} larger than $2V_T$, the small signal analysis fail since the signal variations are not longer small comparable to the bias signal. In this case the RF stage transistors are overdriven and the strong nonlinearities of the devices are excited.

RF stage transistors have been biased with the optimum current density in order to achieve the maximum transconductance gain g_m together with the best performances especially at high frequency since the maximum cutoff frequency is reached. Experimental results show that the best linearity in the heterojunction bipolar transistors come with highest C_{bc} and lowest r_b [Trotta:07,1]. Further, as the transistor base resistance r_b is in series with the RF signal path, a lower r_b produce a lower output noise floor since its thermal noise produced is smaller. To achieve the best linearity and noise performance multiple base configuration BEBC has been chosen.

LO stage works as current buffer providing a time commutating current path. As already said in chapter 2.2, the transistors are layouted in a BECEB configuration with one collector shared between two transistors. Transistors size is the same of RF transistors but with DC current halve. For a good switching behavior, in order that the total tail current is alternately steered from the two branches of double balanced Gilbert cell a large signal drive is needed. A large voltage swing shortens the rise and fall time of the signal and thereby reduce the

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noise introduced by complementary transistors. The choice of multiple base configuration helps also to reduce the thermal noise due to the LO stage.

Since the input is common for both stages, while a large input signal is suitable for the LO stage, at the same time it is unsuitable for RF one because its transistors are overdriven. So one of the first options for improving the performance is the resistive/inductive degeneration, which however present some drawback:

Resistive degeneration: soft degeneration decrease the conversion gain without lowering significantly the spurious components at the output. Strong degeneration, although reduce the spurious components, it lower at the same time the transconductance (G_m) of the transducer (transducer composed of transistor and degeneration resistor) reducing the conversion gain. Furthermore, since the resistor is in series with the signal path, it could be relevant in function of its value on the output noise budget since it introduces thermal noise. All these unwanted effects become significantly on the signal integrity when more doublers are cascaded.

Inductive degeneration: inductors have the advantage that their inductive reactance increase linearly with frequency. Hence at the targeted frequency a good conversion gain is achievable, whereas for the upper frequencies the reactance degenerates the transducer reducing the gain G_m .

Moreover the thermal noise introduced is lower than resistive degeneration since it is only due to the parasitic resistance. This option however presents still several main problems: in a chain of three doublers as in this work, fit two or more inductors in the same chip is troublesome for many point of view: mutual coupling, area occupancy (especially for the first doubler at 10GHz) and performance in terms of quality factor and self resonance frequency.

Distributed solution, hence transmission line shorter than $\frac{\lambda_g(f_0)}{10}$ used as inductor, is not helpful since for achieve a good inductance the length has to be too long to be cost-effective in terms of layout implementation.

Afterwards a solution to achieve a high spurious suppression will be presented, but first the analytical study of the Gilbert cell is continued.

From figure 3.1, transmission lines TL5-6 are inserted in order to reduce the amplitude of the second spurious harmonic delivered to the LO stage and for decouple the two RF/LO stages from the parasitic capacitances. Their length is approximately equal to $\frac{\lambda_g(2f_0)}{4}$, hence they operate a inversion of impedance for the second harmonic from X node to the C one (fig 3.1).

Therefore being the impedance at X node low (as the input impedance of a common base transistor [Gray:01]), the impedance at C node will be high and the second harmonic will be well attenuated. The second harmonic generated in the RF stage, is delivered to the LO stage and is mixed with LO signal producing at the output two

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spurious components at f_0 and $3f_0$. Since the second harmonic comes from even distortion, the two output components produced will be in phase and being the circuit fully differential they will be strongly suppressed.

The third harmonic $3f_0$ generated in the RF stage, once mixed with LO signal at frequency f_0 produces two output components at $4f_0$ and $2f_0$ and since they come from odd distortion (third harmonic) the fully differential structure doesn't help to reduce their presence at the output. In a frequency octupler, also the contribution of the third harmonic although low could be significantly after several stages of doubling.

Transmission lines TL5,6 moreover decouple the parasitic capacitances from RF/LO stage; parasitic capacitance at C node arises from the collector-substrate and base-collector junctions of transistor T21, while at X node the capacitance comes from base-emitter junctions of the two complementary transistors T1A, T1B. Since both stages own multiple configuration transistors, the effects of the parasitic capacitances could be significant if they are coupled, especially at high frequency, indeed assuming an ideal switching behavior of LO stage, T1A, T1B are approximately on for half of the LO period injecting noise because the parasitic capacitance at node X is such to provide a low path to ground [Trotta:07,1]. Transmission lines TL5, TL6 decouples these parasitic capacitances providing a high path to ground.

While for the second and higher harmonics, TL5, TL6 are seen as distributed circuit which provide a change of impedance, for the fundamental input frequency f_0 these devices can be considered as lumped circuits, or inductors indeed:

$$\text{Length}_{\text{TL5,6}} < \frac{\lambda(2f_0)}{4} = \frac{\lambda(f_0)}{4*2} = \frac{\lambda(f_0)}{8} \quad (3.5)$$

Since the length is shorter than $\approx \frac{\lambda(f_0)}{10}$ the transmission line is handled as lumped element. In fig. 3.2 the simulated inductance is shown at 20 GHz:

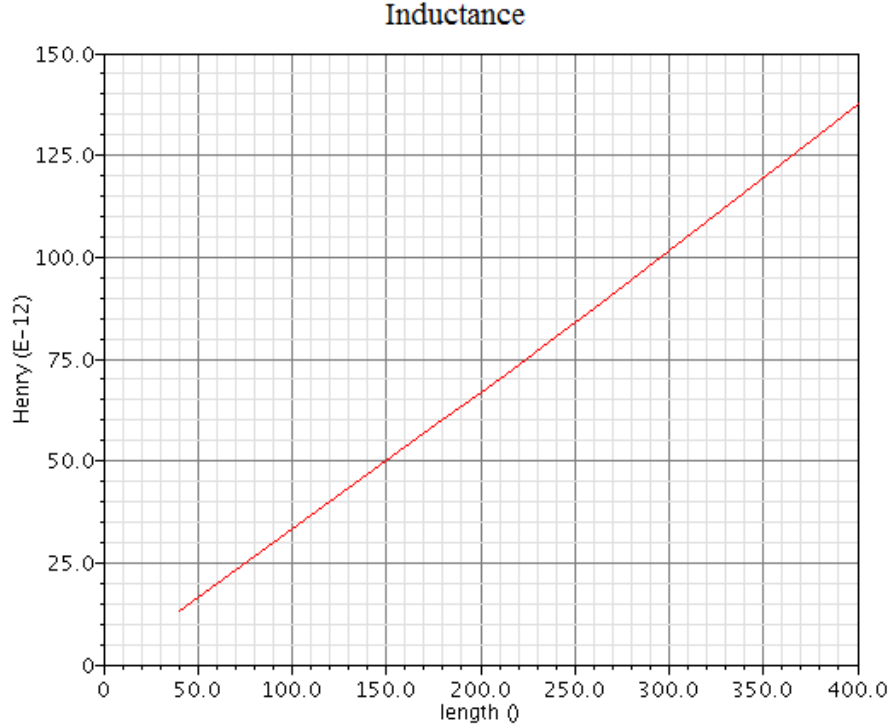


Fig 3.2: Inductance versus transmission line length @ 20GHz.

For a transmission line with a real or virtual short at the end correspond an effective inductance of :

$$L = \frac{Z_0}{2\pi f} \tan\left(\frac{2\pi l}{\lambda_g}\right) \quad \text{for } l \leq \lambda_g/4 \quad (3.6)$$

Where Z_0 is the characteristic impedance, λ_g is the wavelength inside the transmission line, l denotes the length and f the frequency. As fig. 3.2 depicts, for length shorter than a quarter wavelength the relationship between length and inductance is linear.

The quality factor, around $Q=4$ @ 20GHz is not much sensitive to the length variation being the inductance as well as resistance linear function of that.

Passing the schematic in fig. 3.1 and concerning only the fundamental frequency f_0 , it is possible to replace transmission line TL5,6 with two equivalent inductors as showed in fig. 3.3. Since the circuit is symmetric, only one branch is shown. C_X is the base-emitter capacitance due to LO stage transistors at X node, while R_{p5} represent the losses associated to the transmission line. This network is a LC filter which introduces a phase shift in the RF path, the current at X node will has got an amplitude and phase which depends on the transfer function of this filter. From

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simulation, at fundamental frequency of 20 GHz the phase lag introduced from this LC network is 60° . In the RF transistor, if the frequency associated to the pole of current gain transfer function $\beta(f)$ is placed at $f_p = \frac{f_T}{\beta_0}$, for fundamental input frequencies higher than f_p the effect of base-emitter capacitance C_π is considerable introducing itself a further phase shift.

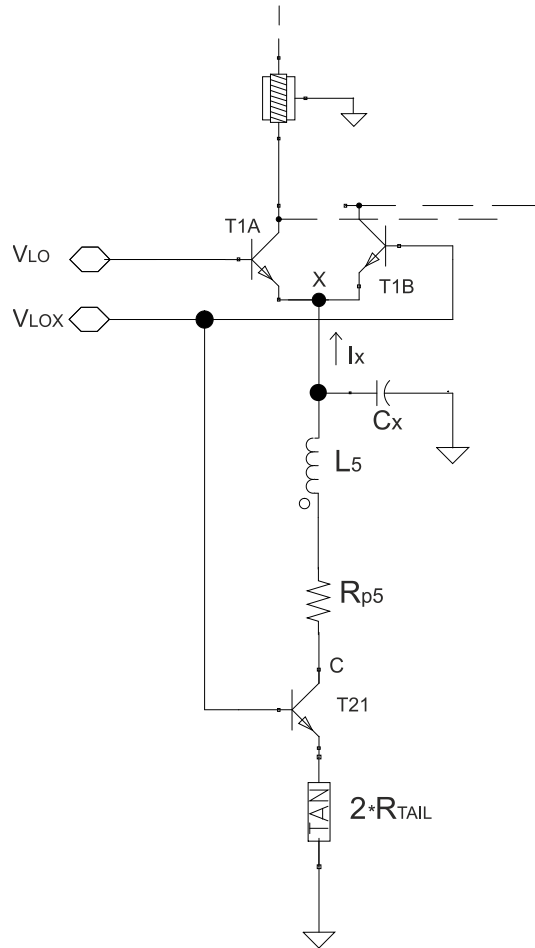


Fig 3.3: Equivalent network at fundamental frequency f_0 .

As the length of the transmission line change, the phase shift provided change as well; however achieve a high phase shift is not possible since the inductance is too small and for long transmission line the circuit start to be distributed.

3.3 Gilbert Cell as Frequency Doubler

After has introduced the features of the starting topology, let's do a step ahead about how the Gilbert cell perform the frequency doubling and what are the main issues. Since both inputs are connected to one common source and the input signal is large in order to guarantee a good switching behavior at LO stage, the Gilbert cell works as phase detector; it produces an output DC component proportional to the phase difference between the two inputs and another output component (the desired one) at double frequency corresponding to the fundamental input one. If the input signal is large in amplitude (as in this case), the actual waveform shape is unimportant since the transistor simply switches to one state to the other at the zero crossings of the waveform [Gray:01]. Therefore the transistors of Gilbert cell work as switches commutating from "open" to "close". In figure 3.4, a square wave shape represent the state of the signals on different nodes of the circuit. However since the real input signal is sinusoidal and since the RF stage is still able to produce a sinusoidal shape output current, (RF stage is not completely saturated yet) the output waveform still has a sinusoidal shape.

Taking as reference the schematic in fig. 3.1/3.3, in fig 3.4 V_{LO}, V_{LOX} signal drivers are shown together with the signal currents I_X, I_Y and the output voltage $V_o = V_{OUT} - V_{OUTX}$. I_X, I_Y are the currents generated from RF stage delivered to LO stage already shifted by the phase shift network (fig. 3.3).

The output DC component is given by:

$$V_{average} = \frac{1}{2\pi} \int_0^{2\pi} V_O(t) d(\omega_o t) = \frac{-1}{\pi} (A_1 - A_2) \quad (3.7)$$

Where areas A_1 and A_2 are as indicated in fig. 3.4, thus [Gray:01]:

$$V_{average} = -I_{TAIL} R_{OUT} \left[\frac{(\pi - \phi)}{\pi} - \frac{\phi}{\pi} \right] = I_{TAIL} R_{OUT} \left(\frac{2\phi}{\pi} - 1 \right) \quad (3.8)$$

I_{TAIL} is the bias current which flows into R_{TAIL} while R_{OUT} is the resistance of the output network and ϕ is the phase delay between I_X and V_{LOX} .

For suppress the DC component, the two areas A_1, A_2 must be equals and in order to reach this condition the RF current I_x must be in phase quadrature with V_{LO} and V_{LOX} signal (fig. 3.3/3.4) so $\phi = \frac{\pi}{2}$ and $V_{average} = 0$.

From fig. 3.4, without phase quadrature between I_x and V_{LO}/V_{LOX} a DC output component is always present.

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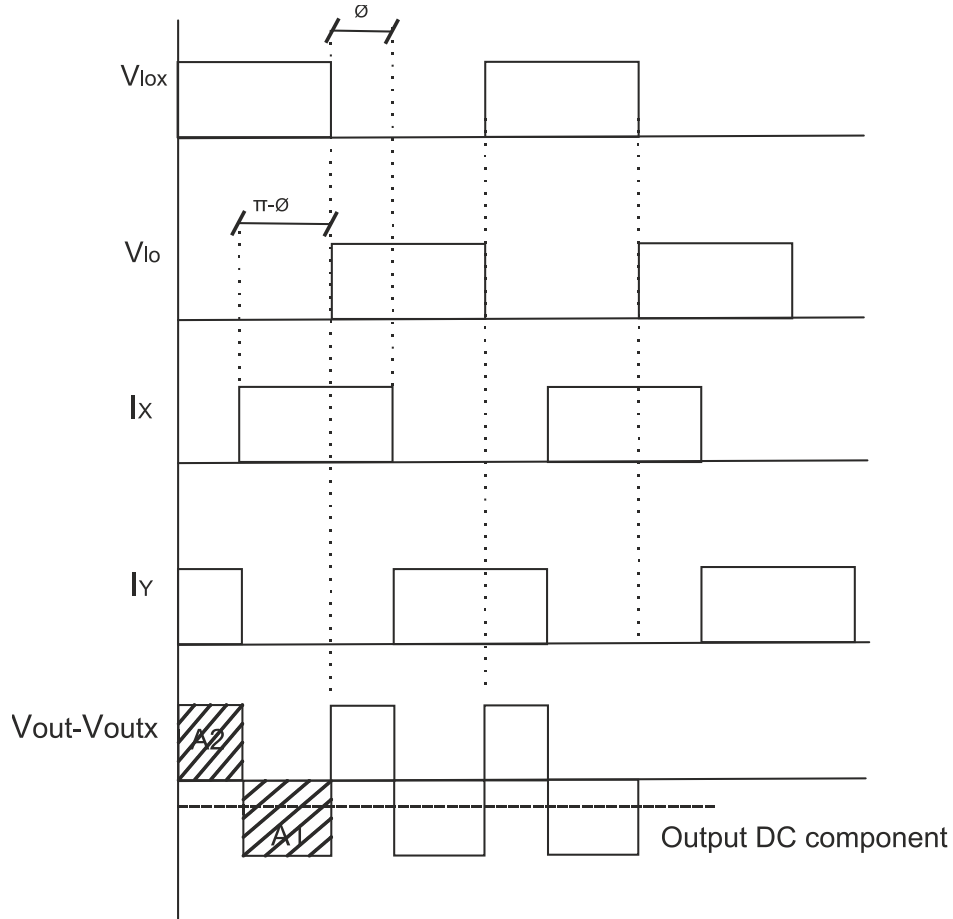


Fig 3.4: Signal waveforms in a Gilbert cell with NO phase quadrature.

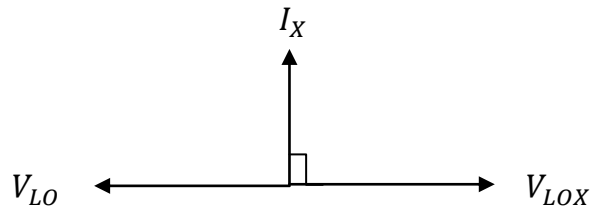


Fig. 3.5: Phase quadrature between LO and RF signal for provide zero DC output component.

Although the phase quadrature provide a zero DC output component, the major benefits of this technique are others. From simulation, without phase quadrature the two output branches are strongly unbalanced in amplitude with a common mode much higher than the differential one, meaning that the common mode disturbs and all even order harmonics are badly suppressed. With this kind of output, in a chain

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of three frequency doublers a filter should be necessary to improve the spurious rejection.

This lack of balance is due to the LO stage; indeed the two complementary transistors T1A/B draw a different current each one because the difference between their two V_{BE} produce a strong difference in the two I_C since the relationship I_C-V_{BE} is exponential.

Whether transistors T1A/B act as good switches, the fundamental f_0 at X node is suppressed and only a strong second harmonic component is present neglecting the higher ones [Trotta:07,1]. Indeed since they are driven from the same differential signal at frequency f_0 and since that node is electrically in the middle no components at fundamental frequency f_0 are presents and the V_{BE} of T1A/B are equals. However this behavior is only ideal, actually this happens just partially because the couple is not perfectly complementary and therefore a component of voltage $V_X(f_0)$ is still present which bring a mismatch in the two V_{BE} of T1A/B transistors as depicted in fig. 3.6. “X” is a low impedance node, hence $V_X(f_0)$ is small compared to V_{LO}, V_{LOX} , however since the current draw from each transistor depends strongly on its V_{BE} , $V_X(f_0)$ is able to cause an imbalance on the output signal. Let’s have a look on the vector diagrams of the phases:

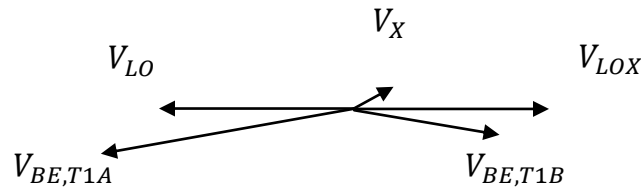


Fig 3.6: Base emitter voltages with a generic phase shift.

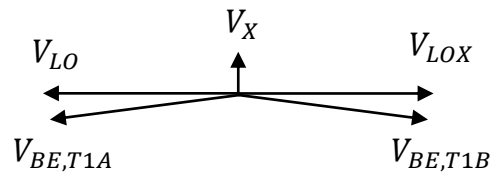


Fig 3.7: Base emitter voltages with phase quadrature.

With phase quadrature (fig.3.7), the two V_{BE} have the same magnitude so the currents drew are the same and the output swing is maximized increasing the

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conversion gain, common mode rejection ratio and the even order spurious harmonics suppression.

The two T1A/B transistors however are not totally complementary as in the ideal case because the phase difference between the two V_{BE} is smaller than π , hence LO stage contribute to increase the output noise [Trotta:07,1].

With a generic phase shift (fig.3.6) the two V_{BE} are different, (how much depends on amplitude and phase of V_X) so the two outputs currents are different causing an imbalance at the output.

3.4 Overview on the Phase Shift Networks

This section provides an overview on the design implementation of the theoretical analysis behind which the phase shift was developed. In literature, work [Forstner:09] provide a method for a physical implementation of the phase shift between LO/RF signal in a frequency doubler. The authors, at 19 and 38 GHz use microstrip respectively of 1600 and 800 μm between the RF/LO stages in order to provide a phase shift of 75° at the fundamental frequency. This solutions however, besides to be costly in terms of chip area, doesn't provide the phase quadrature so the two outputs differ by several dB without maximizing the conversion gain and the spurious harmonic suppression.

In this work other solutions have been discovered in order to get the phase quadrature keeping the area occupancy limited also at low frequency where the microstrip cannot be used.

Since the frequency range from the first to the third doubler is wide, the proposed solutions are different. For the 80 GHz frequency doubler a distributed LC filter has been used since at this frequency the transmission lines are cost-effective. The phase shift network was implemented between RF/LO stages as "interstage network". For the 40 GHz doubler, two solutions have been developed since for an input frequency of 20 GHz both lumped and distributed solutions can be used. One solution, *Coil*, provide 90° phase shift by using the resonance that occurs at the fundamental input frequency between inductor and base-emitter junction capacitance of RF transistor. The other version, *Cap*, uses a distributed network with transmission lines and capacitors, but slightly different from the LC filter previously mentioned in order to fix potential stability problems of the 80 GHz doubler.

Coil version allows an area saving of almost 20% respect to the *Cap* one. The 20 GHz frequency doubler uses an active phase shift network composed of a capacitively loaded emitter follower in front of the Gilbert cell which resonance frequency is tuned at the fundamental input one at 10 GHz.

Looking more in detail the basic starting topology in fig. 3.8, in both input signal paths there are a high pass filters composed of DC blocking capacitors C_{1-4} and bias resistors R_{1-4} . These filters can provide a further relative phase lead, however

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has been chosen to don't take advantage of this technique since the drawbacks introduced are more than the advantages.

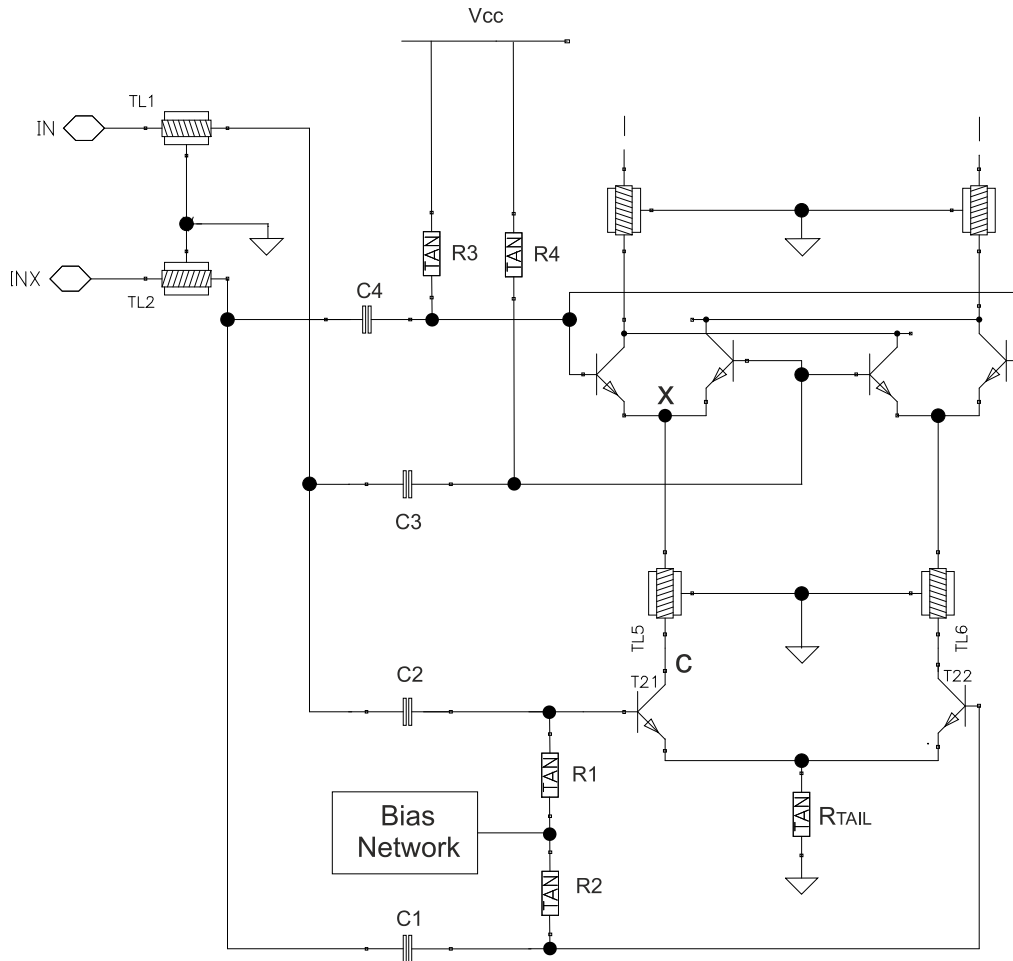


Fig 3.8: Detail on the bias network.

In the LO path, the transistor input impedance participate to the high pass filter, so for a fixed phase lead the signal attenuation is higher than expected since the resistive-capacitive input impedance is involved. Once estimated the attenuation to the corresponding phase lead, has been chosen to avoid any phase shift since already for a small delay the signal attenuation is significant and a large signal is necessary in order to keep a good switching behavior.

In the RF path, any phase lead provided from the filter R_{1-2} and C_{1-2} is unwanted since the phase shift network introduce a phase lag.

4 80 GHz Frequency Doubler

4.1 80 GHz Frequency Doubler Design

The 80 GHz frequency doubler (with 40 GHz input frequency) is based on the same structure of the basic starting topology as fig. 4.1 shows. The transistors of the Gilbert cell are High Speed devices with $f_T=170$ GHz. The phase shift network implemented is a LC filter composed of microstrip TL3-6, capacitors C_{5-6} and the base-emitter junction capacitance of LO stage transistors.

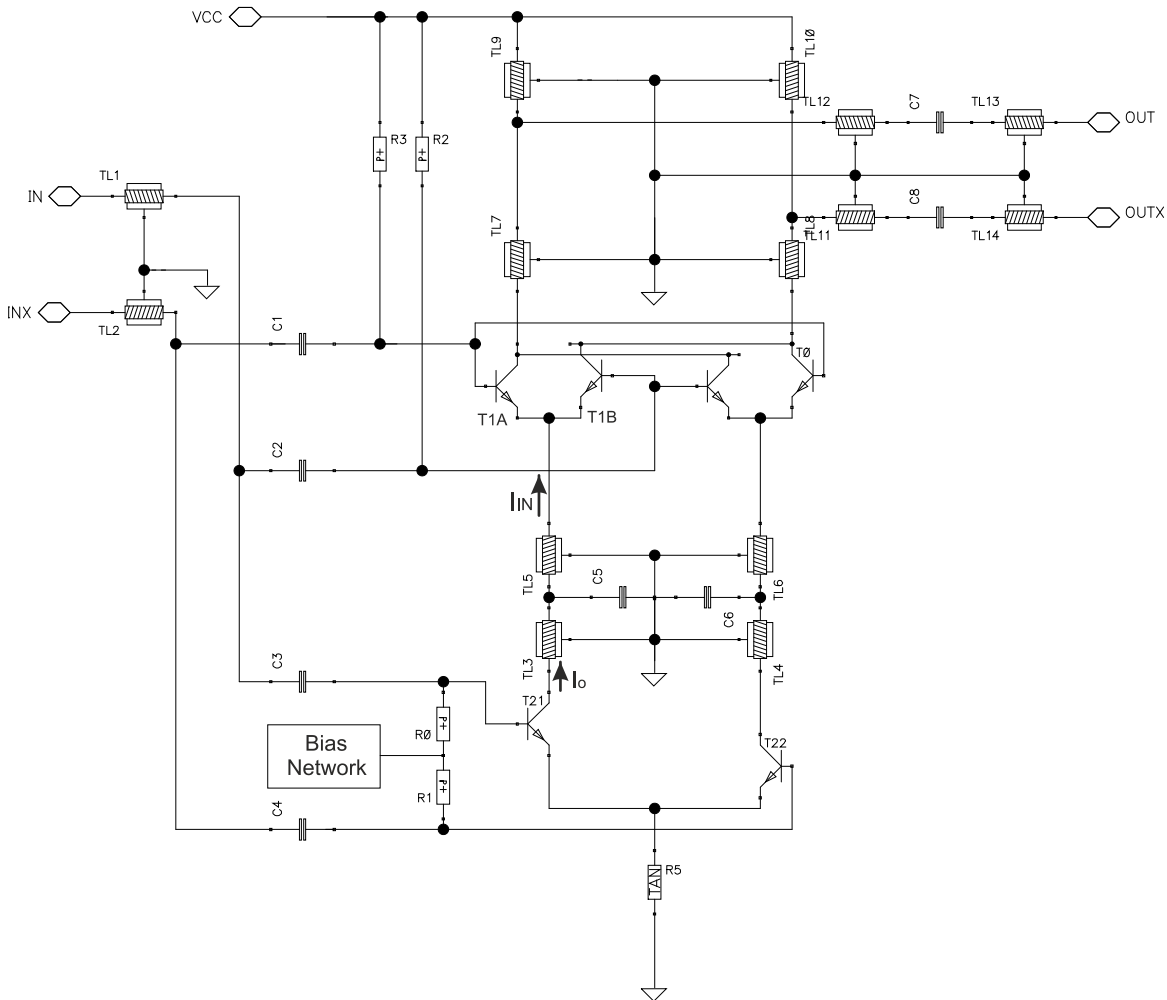


Fig. 4.1: 80 GHz frequency doubler.

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The main idea is to insert a phase lag network which provide, together with the phase shift due to RF transistors, 90° phase shift so the RF current delivered to the LO stage is in quadrature with LO signal driver and the outputs are balanced.

Schematic of fig 4.2 shows the equivalent circuit of one branch of the Gilbert cell in fig 4.1. A dotted rectangle represent the small signal circuit of RF transistor T21, L_3, L_5 are the equivalent inductances of TL3, TL5, $C_{BE, T1A}$ is the base-emitter junction capacitance of transistor turn off and T1B is the transistor turn on. Parasitic resistance of TL3, TL6 here is not considered in order to simplify the analysis, however its effect is to lower the quality factor of the filter. From small signal analysis point of view (fig.4.2), the input impedance Z_{IN} of T1B transistor is resistive at low frequency with an inductive behavior as frequency increase [Gray:01]:

$$Z_{IN} \approx \frac{\frac{1}{g_m} + \frac{r_b}{\beta_0} + sC_{\pi} r_{\pi} \frac{r_b}{\beta_0}}{r_b + sC_{\pi} r_{\pi} \frac{r_b}{\beta_0}} * r_b \quad (4.1)$$

Microstrips TL3-6 have to be designed in order to behave as lumped elements within the band of the input signal. In this work the length is set to 150 μm each one, so for the fundamental at 40 GHz and for the second and third harmonics they behave as inductors introducing a phase shift for the fundamental and attenuating the other ones.

For the higher spurious harmonics this network provide a impedance transformation.

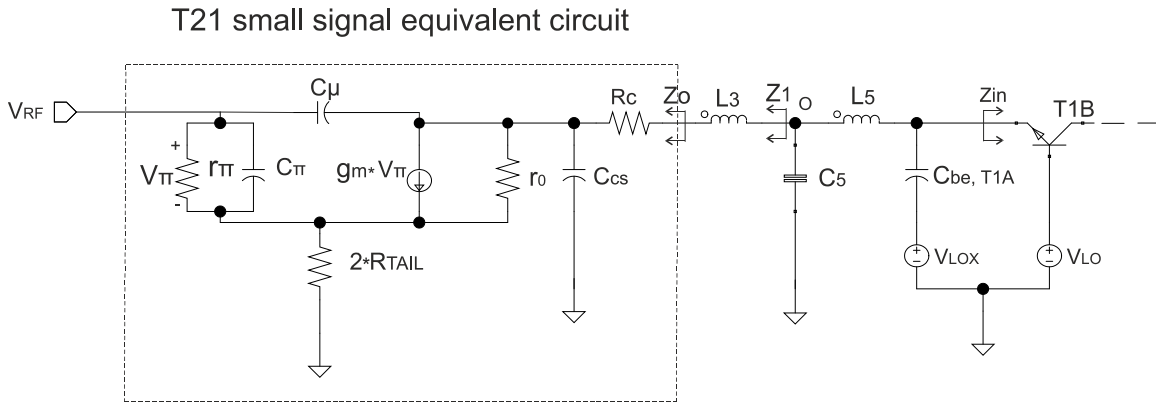


Fig 4.2: Equivalent circuit of phase shift network with T21 transistor small signal circuit.

In the design of the phase shift network there are some rules to keep in consideration to reduce instability issues. If transmission line TL5 is short, to achieve the necessary phase lag a bigger capacitance C_5 and a longer TRL3 are

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needed; in this conditions the T21 output impedance (Z_o) together with the equivalent inductance L_3 provide a high impedance path as frequency increase, while the impedance provided from C_5 being much lower in the parallel results dominant.

$$Z_1 = Z_o + j\omega L_3 \quad (4.2)$$

$$Z_5 = \frac{1}{sC_5} \quad (4.3)$$

$$Z_{parallel} = Z_1 // Z_5 \approx Z_5 \quad (4.4)$$

Therefore whether node O is mainly capacitive and L_5 has a low inductance, T1B is capacitive degenerated and an instability can occur since the capacitive degeneration could generate a negative input real part impedance.

The influence of the phase shift network on T21 input impedance instead increase as well the input frequency increase since the base-collector capacitance C_μ trend to short-circuit the two terminals. Long TL3 reduce the stability making the real part on that input impedance more negative [Trotta:07,1].

In order to extract some useful relationship between the current delivered to LO stage and that one generates from RF one, the circuit of figure 4.2 has been simplified taking several assumption.

Let's include R_c in the series resistance of TL3 and neglect base-collector capacitance C_μ although could be relevant at 40 GHz. At the same time, let's consider the input resistance of T1B just resistive ($Z_{IN} = \frac{1}{g_m}$) neglecting any inductive behavior. These considerations bring to the schematic shows in fig. 4.3.

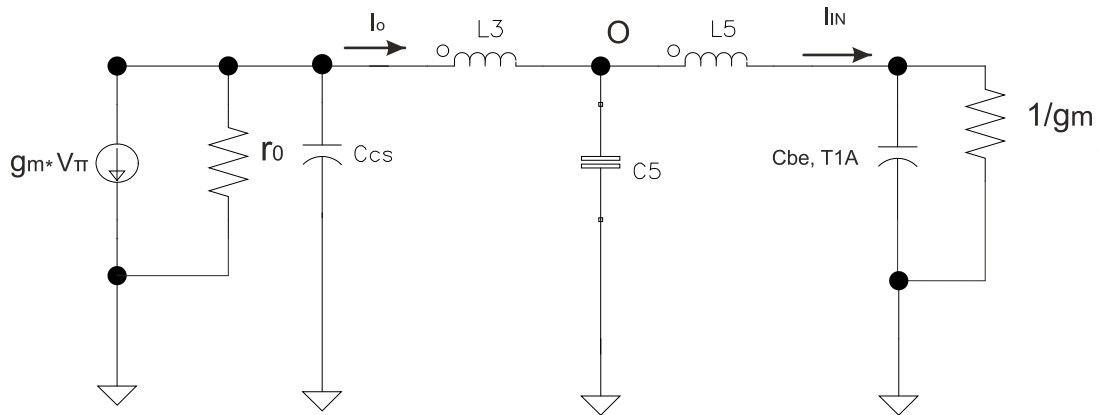


Fig 4.3: Simplified schematic of equivalent circuit in fig.4.2.

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The simplified network of fig. 4.3 is based on the same topology of the ladder filter. It implements a fifth order filter with two couple of poles complex and conjugate. This topology is highly insensitive to the parameter variation. Once set the length for the transmission lines, following the rules previously exposed in order to reduce the instability issues, C_5 is chosen to achieve the phase quadrature. Choose an appropriate length for the microstrips afford to set a value for C_5 that doesn't lower the conversion gain of the doubler.

By changing the length of TL3, TL5, the instability points are able to be shifted in frequencies range where the instability can be easily filtered out. Whether instability occurs at lower frequency than the fundamental one, it can be filtered by a high pass filter provided from the bias network with the drawback previously mentioned. Whether it occurs at higher frequency, it can be suppressed by adding two external capacitors from *collector to ground* of the RF/LO transistors in order to reduce the bandwidth.

Up to now the RF stage has been considered working with small signals, however with this input power (paragraph 1.2, Target Specifications) it works close to large signals so also the current delivered to LO stage results as large signals; in this case the analysis can be optimized and the equivalent circuit of fig. 4.3 can be reviewed considering large signal operations also for the RF stage as in fig. 4.4.

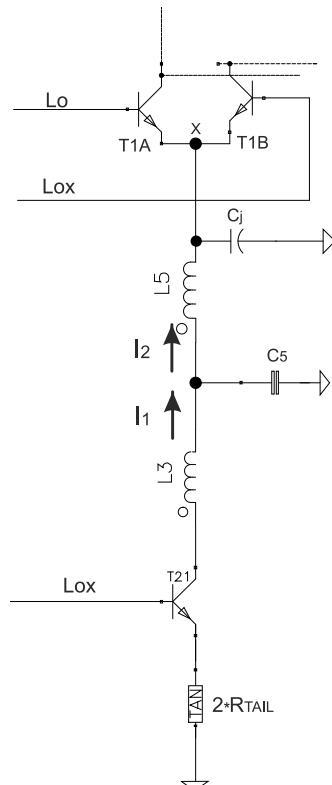


Fig 4.4: Equivalent circuit with large signal current delivered to LO stage.

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Since the current delivered to the LO stage is at large signals, the input impedance Z_{IN} in (4.1) is not longer valid. C_j represent the base-emitter junctions capacitance of T1A/B transistors.

An exact relationship for the input/output current from the phase shift network it's hard to define because many parasitic effects are involved at these frequencies. A more practically design formula is given in (4.5) which shows especially the effect of C_5 on the conversion gain.

$$\frac{I_2}{I_1} = \frac{C_j}{(C_j + C_5)(1 + s^2 L_5 \frac{C_j * C_5}{C_j + C_5})} \quad (4.5)$$

Obviously, the quality factor of the couple of poles is not infinite but depends on the series resistance of the transmission lines.

With short transmission lines, big capacitor C_5 is needed to achieve the phase quadrature. Hence whether C_5 becomes comparable or bigger than junctions capacitance C_j the current delivered to the LO stage is low and then the conversion gain decrease. For avoid this drawback, the length of the transmission lines shouldn't be too small and the configuration and size of LO stage transistors have to ensure $C_j \gg C_5$. For reach the last condition a multiple contact configuration BEBCBEB for the LO transistors has been chosen. Multiples bases guarantee low resistance decreasing the output thermal noise.

With a length of $150 \mu m$ for TL5, TL3 which provide an inductance of 50 pH each one and a junction capacitance of $C_j = 2 * (C_{BE,T1A} + C_{BE,T1B}) \cong 150 \text{ fF}$ where $C_{BE,T1A/B} = C_{je} + \tau_F g_m$, the current ratio $\frac{I_2}{I_1}$ is depicted in figure 4.5.

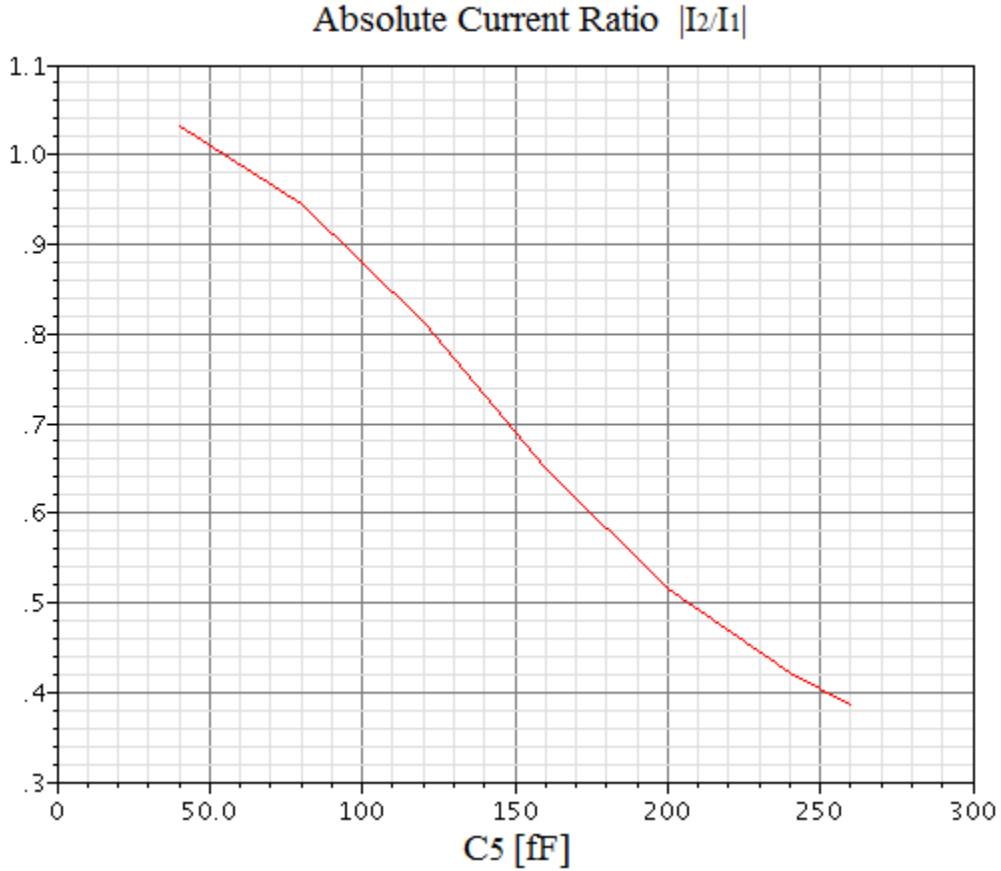


Fig.4.5: Absolute ratio between current delivered to the LO stage I_2 and current from RF stage I_1 .

More detailed results simulated with harmonic balance response come from simulation in figs. 4.6/4.7, where the magnitude and phase of ratio between LO stage input current and RF stage output current is depicted for the fundamental and upper harmonics.

The fundamental signal at 40GHz is left unchanged in amplitude and delayed only by 66° degree since the RF transistor already provide a phase shift at this frequency to get the phase quadrature. For the second and third harmonics the transmission lines still behave as lumped elements so these two spurious are attenuated since are at frequencies higher than cut-off frequency. For the fourth harmonic microstrips behave as distributed elements so they, together with capacitor C_5 , provide a change of impedance along the path. This change result in a low impedance at node collector of T21, here-hence explained the high gain for the fourth spurious. Even though the gain for the fourth harmonic is high, the current delivered to LO stage is about few μ Ampere.

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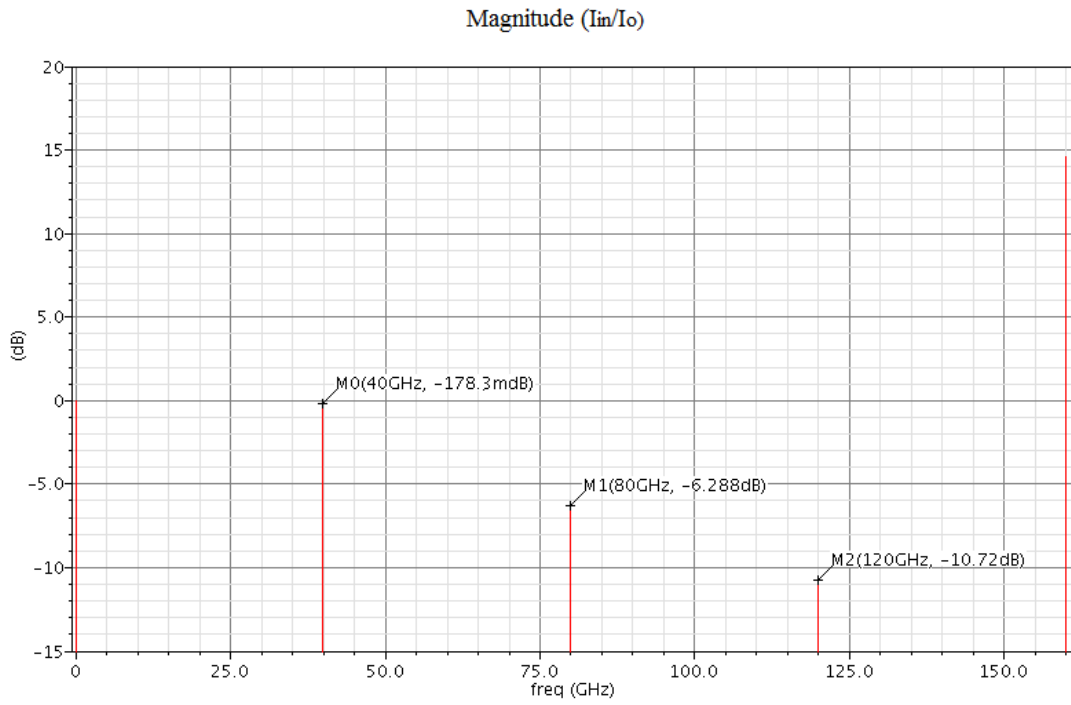


Fig 4.6: Magnitude transfer function between RF stage output current and LO stage input current.

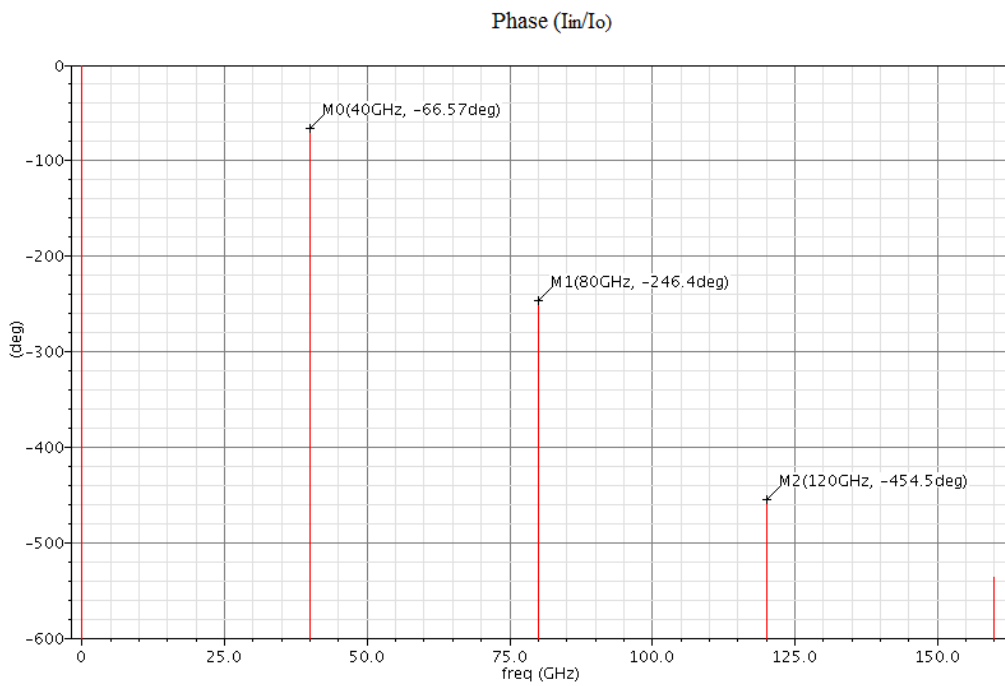


Fig. 4.7: Phase transfer function between RF stage output current and LO stage input current.

4.2 Stability Issue

In this paragraph the stability of the 80 GHz frequency doubler is discussed. For further information about this topic refer also to paragraph 8.2.

This doubler is the most problematic from the stability point of view, probably due to the presence of the phase shift network.

Potential instability originally comes out when the 80 GHz doubler, with matched load at the output, is driven by an 40 GHz frequency doubler based on the same topology. Instability instead is not triggered when, with the same conditions, it is driven by the 40 GHz frequency doubler *inductive* version. This study brought as result to develop another topology called 40 GHz frequency doubler *capacitive* version which own a phase shift network slightly different as shows is fig. 5.1.

The same way the 80 GHz frequency doubler, with matched load at the output, results potential unstable when is driven by a 50 Ω source impedance (fig.4.8).

The stability has been checked using SpectreRF from Cadence with $k - \Delta$ test, where for an unconditional stability these two conditions must be respected:

$$\begin{cases} Kf > 1 \\ B_1f > 0 \end{cases}$$

In figure 4.8 the stability check configuration is shown, it includes the 80 GHz doubler standalone, the input PORT device with $R_{PORT1} = 50 \Omega$ and the output PORT with $R_{PORT2} = 100 \Omega$. The output is matched. Since the 80 GHz doubler is potential unstable when is driven by a resistive source impedance, this simple configuration has been studied first to investigate on the possible causes.

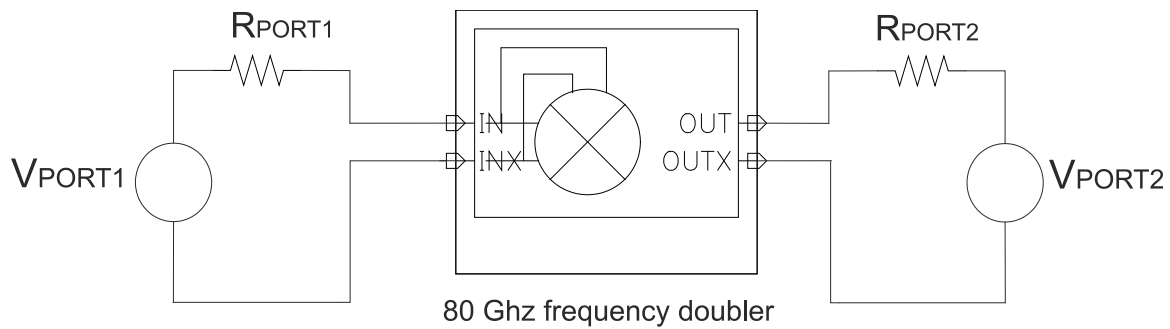


Fig. 4.8: Stability test configuration.

This topology, with $V_{PORT2} = 0 \text{ V}$, affords to plot the input port impedance when the doubler is driven by a resistive source allowing to study the device input impedance without any other effect due to the chain of doublers.

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In this configuration, while B_{1f} is greater than 0 in all frequency range, the parameter K_f for a wide range of frequencies lower than the fundamental one is smaller than 1, hence a potential instability can be present.

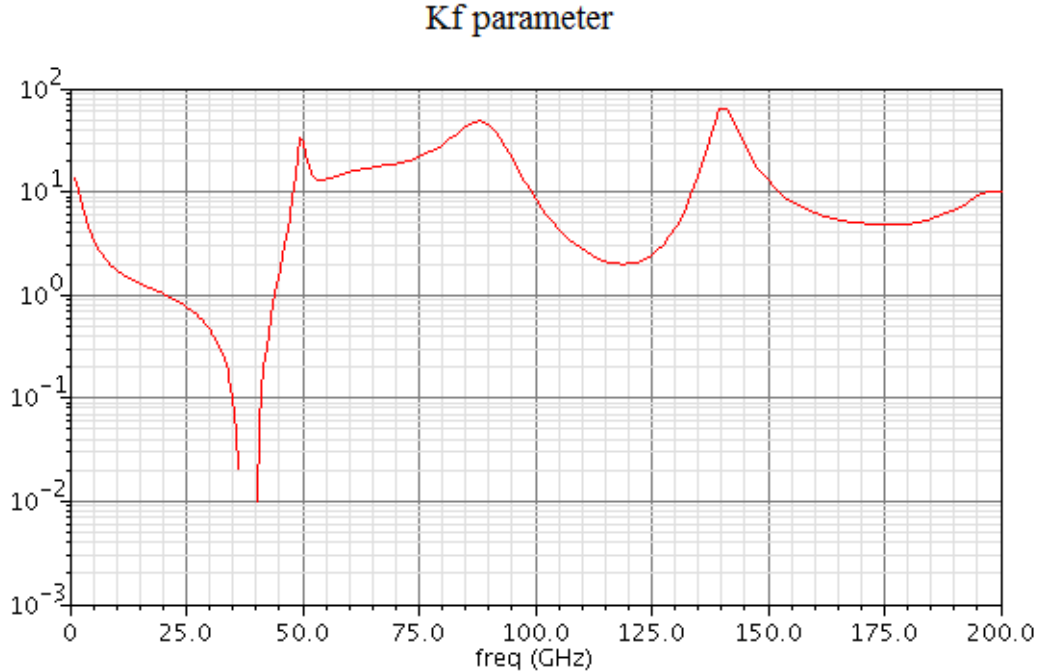


Fig. 4.9 : K_f parameter, potential instability occurs between 21 and 44 GHz.

Here a practical method for fix the instability is shown, however this topic has to be study more in depth to find the causes of its origin.

In the circuit of fig. 4.8, oscillations can be triggered if either the input or output port impedance has a negative real part [Pozar:05]. The 80 GHz doubler in a certain frequency range shows a negative input impedance (fig. 4.11). Within the same frequency range $S_{11} > 1$ so also the input reflection coefficient $|\Gamma_{in}| > 1$ and since Γ_{in} depends on the source and load matching network by the (4.6) the stability of the doubler inserted in the chain depends on the output matching network of the 40 GHz frequency doubler and from the load impedance.

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \right| \quad (4.6)$$

Looking at fig. 4.10/4.11, from 10 to 40 GHz the 80 GHz doubler input impedance, $Z_{IN,3^{\circ} DOUBLER}$, shows a capacitive behavior (because the magnitude of input impedance decrease as frequency increase) with a negative real part because the phase is around 180° , thus it can be modeled as $Z_{IN,3^{\circ} DOUBLER} = R_{IN}(\omega) - j/\omega C_{IN}(\omega)$. If the source has a resistive/inductive

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output impedance, $Z_{OUT,SOURCE} = R_{OUT}(\omega) + j\omega L_{OUT}(\omega)$, oscillations and instability result at frequencies where $R_{IN}(\omega) + R_{OUT}(\omega) < 0$ [Trotta:07,2].

Magnitude input impedance of the 80 GHz doubler

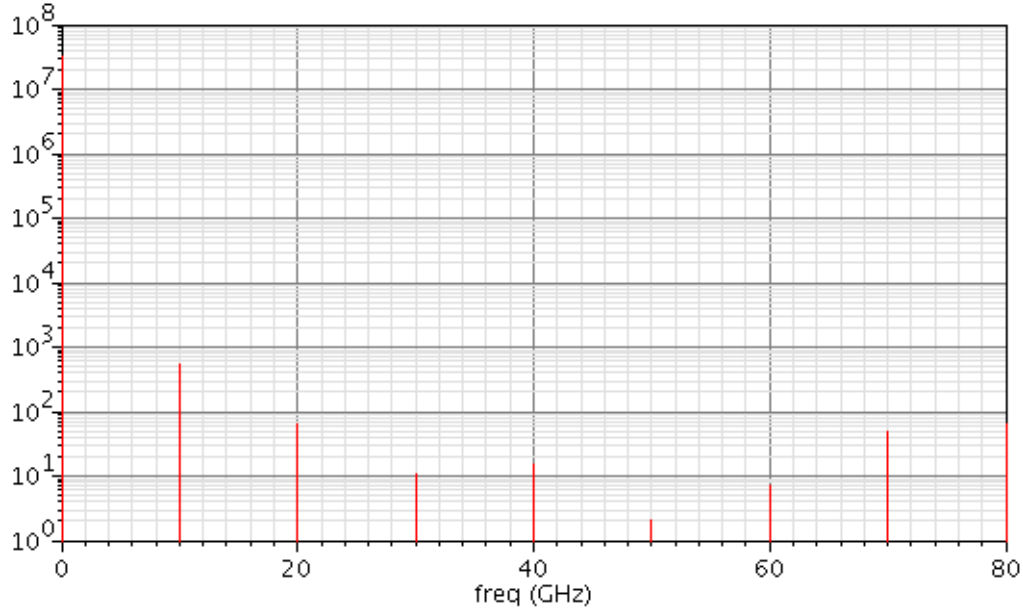


Fig. 4.10: Magnitude of the input impedance referred to fig. 4.8.

Phase input impedance of the 80 GHz doubler

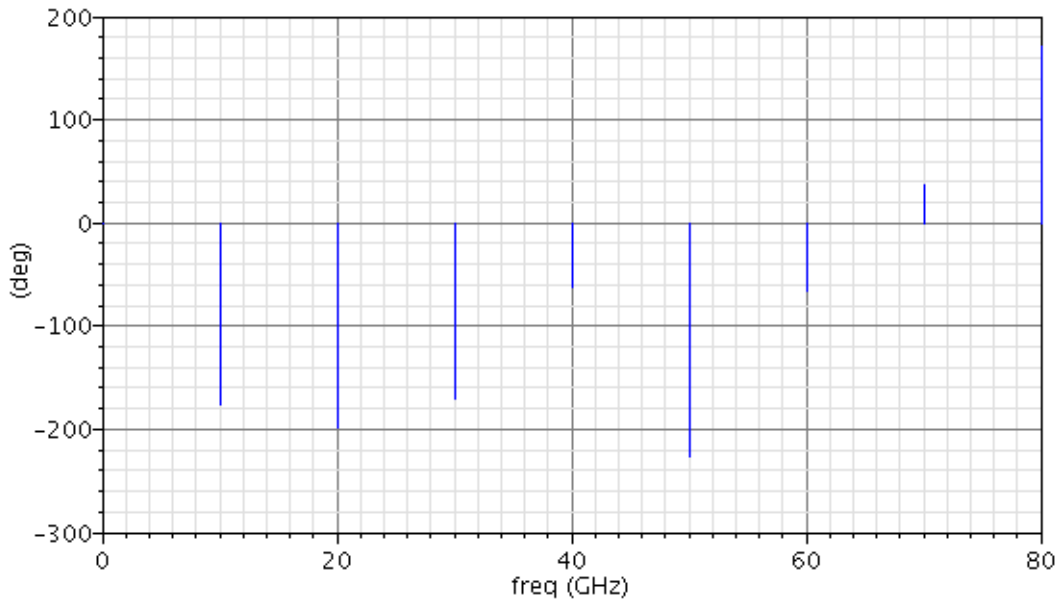


Fig. 4.11: Phase of the input impedance of fig. 4.8.

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When the doubler is inserted inside the chain, the impedances change so the frequency range where the instability occurs change as well. In this case, when the 80 GHz doubler is connected to the 40 GHz doubler, the range of frequencies within the potential instability occur become narrow.

First approach involved the study of the 40 GHz doubler output matching network in order to further narrow the frequency range within the potential instability occurs. By using the stability circles is possible reduce that around 10-20 GHz.

Now that the potential instability is shifted at lower frequency than the fundamental at 20 and 40 GHz (corresponding to the 2nd and 3rd doubler), the idea is to place a capacitor in series with the signal path in order to introduce a zero to suppress the spurious harmonics at lower frequencies. The bias network of each doubler as already said provide a zero at $j\omega = 0$, however for the drawback that it introduces has not been used.

The solution used, which at the same time provide phase quadrature for the fundamental signal and makes the overall chain of three doublers unconditionally stable is implemented in the 40 GHz frequency doubler *capacitive* version. It make use of a slightly different network than that one presented in the 80 GHz doubler with the addition of two further capacitors to introduce zeros at low frequency (fig.5.1). The zeros at low frequency filter out the spurious harmonics previously mentioned whereas the higher spurious harmonics are suppressed by lowering the transistors bandwidth. The design and schematic of the 40 GHz doubler *capacitive* version is presented in the next chapter 5.

With this solution, the 80 GHz frequency octupler *capacitive* version becomes unconditionally stable.

In paragraph 1.2 is made mention that one of the chips made is composed by the 80 GHz frequency doubler and an output buffer. This chip reflects the circuit topology depicted in fig. 4.8 where in place of the output PORT a buffer is connected. This topology is potential unstable as shows fig. 4.9. The stability issue in this chip has been solved matching the input impedance of the 80 GHz doubler with the source impedance by adding two resistors from IN/INX terminals to ground.

4.3 Results

The results showed come from post-layout simulations. The testbench used is illustrated in paragraph 7.1. In fig. 4.12 the nominal conversion gain versus input power is plotted. In fig. 4.13 the suppression of the spurious harmonics close to the 8th harmonic at 80 GHz is shown. Fig. 4.14 depicts the balance of the output branches; an outputs difference close to zero results in a phase quadrature between RF and LO signal that maximize the output swing producing best performance in terms of conversion gain and spurious suppression. As fig. 4.14 shows, the phase quadrature provided from this phase shift network is little sensitive to frequency variation.

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The DC current is 13.5 mA for a DC power absorption of 45 mW.
The doubler chip size is $520 \times 200 \mu\text{m}^2$.

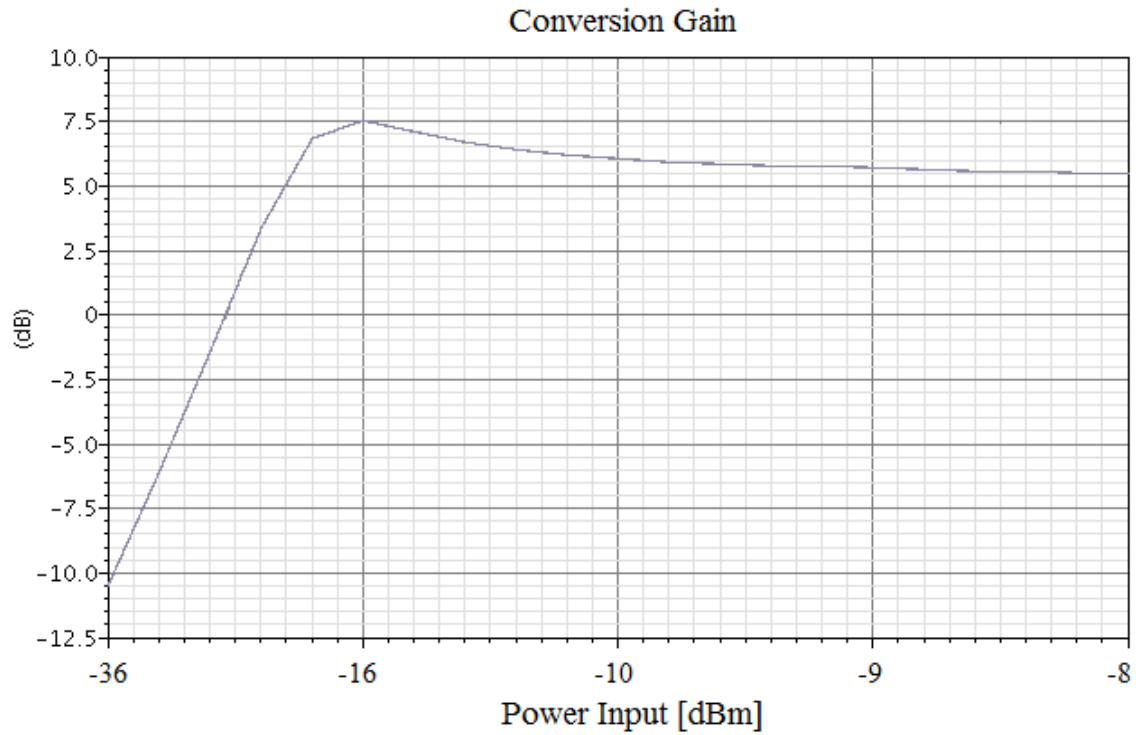


Fig. 4.12: Nominal conversion gain versus input power, reference terminals $OUT, OUTX$ and IN_3, INX_3 .

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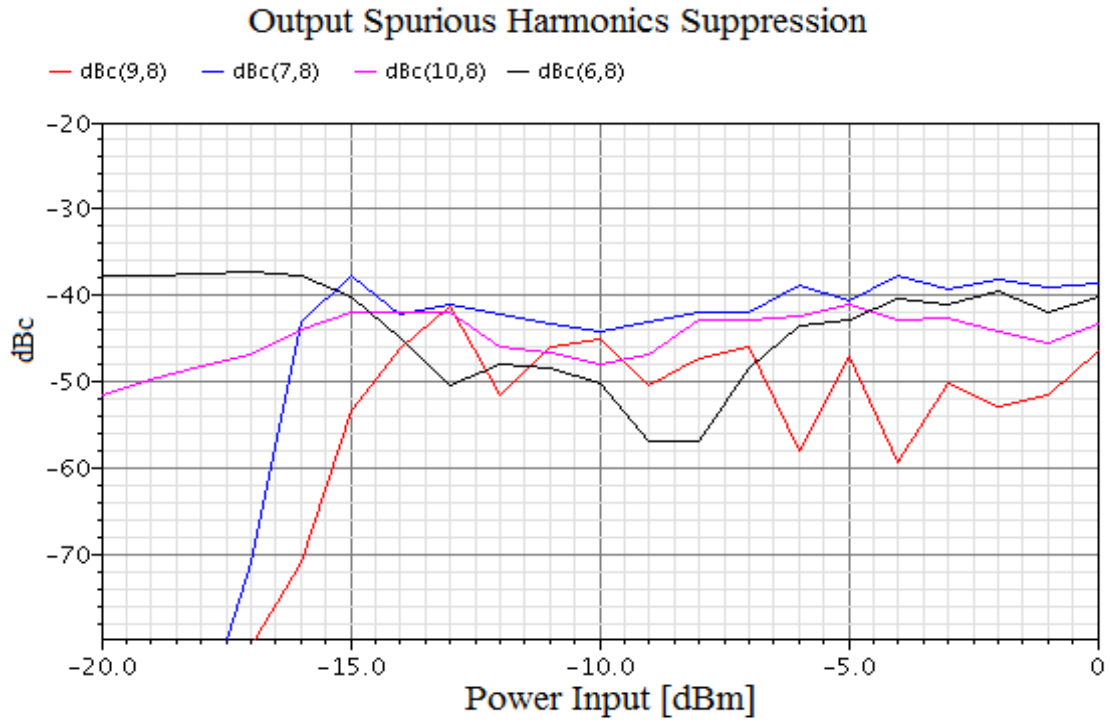


Fig. 4.13: Nominal spurious harmonics suppression versus input power.

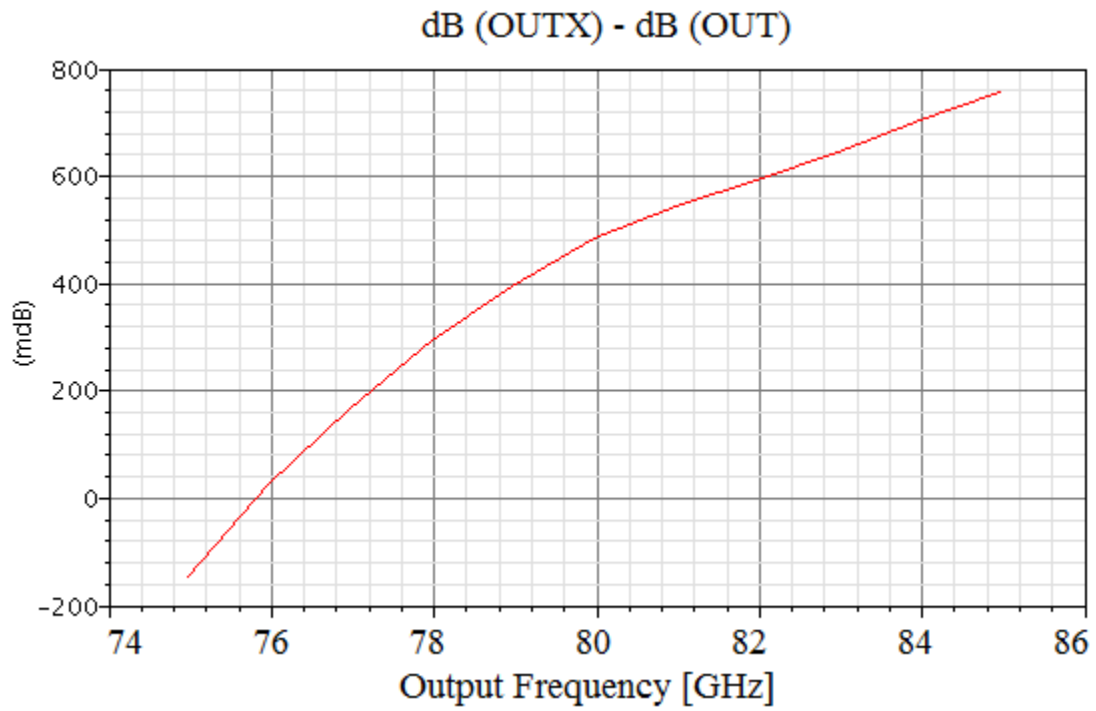


Fig 4.14: Output power difference versus input frequency.

5 40 GHz Frequency Doubler

5.1 40 GHz Frequency Doubler *Capacitive Version Design*

The 40 GHz frequency doubler *Cap* version (input frequency at 20 GHz) own a topology slightly different from the 80 GHz doubler.

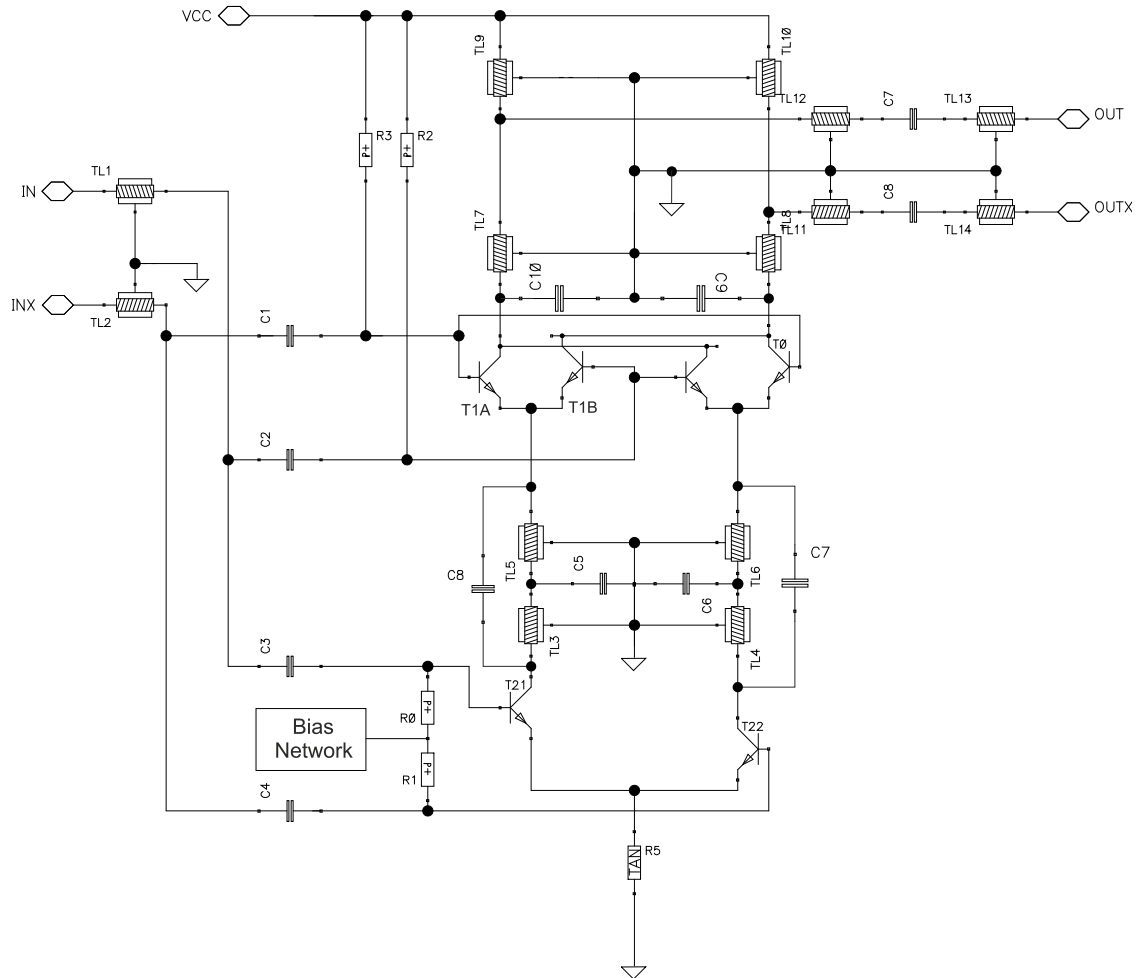


Fig 5.1 : 40 GHz frequency doubler *Cap* version.

The phase shift network implements a transfer function that provide low gain at low frequency thanks to the presence of capacitors $C_{7,8}$ which insert zeros at low

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frequency. The low gain reduces the amplitude of the spurious harmonics at low frequency makes the chain of doublers unconditionally stable. These two capacitors moreover change the doubler output impedance providing more freedom degrees on its design. The network poles are placed to achieve the phase quadrature for the fundamental signal. Capacitors $C_{9,10}$ reduce the bandwidth of the transistors to prevent potential instabilities at high frequency. Since the instability was the main issue on the design of the octupler *Cap* version, two big capacitors $C_{9,10}$ was been necessary with the drawback of lower the conversion gain as will shows afterwards. In fig. 5.2, 5.3 the magnitude and phase of the current ratio between output and input current of the phase shift network are shown.

As fig. 5.2, 5.3 depicts, the zero has got a positive real part since at low frequency when the magnitude rise the phase decrease.

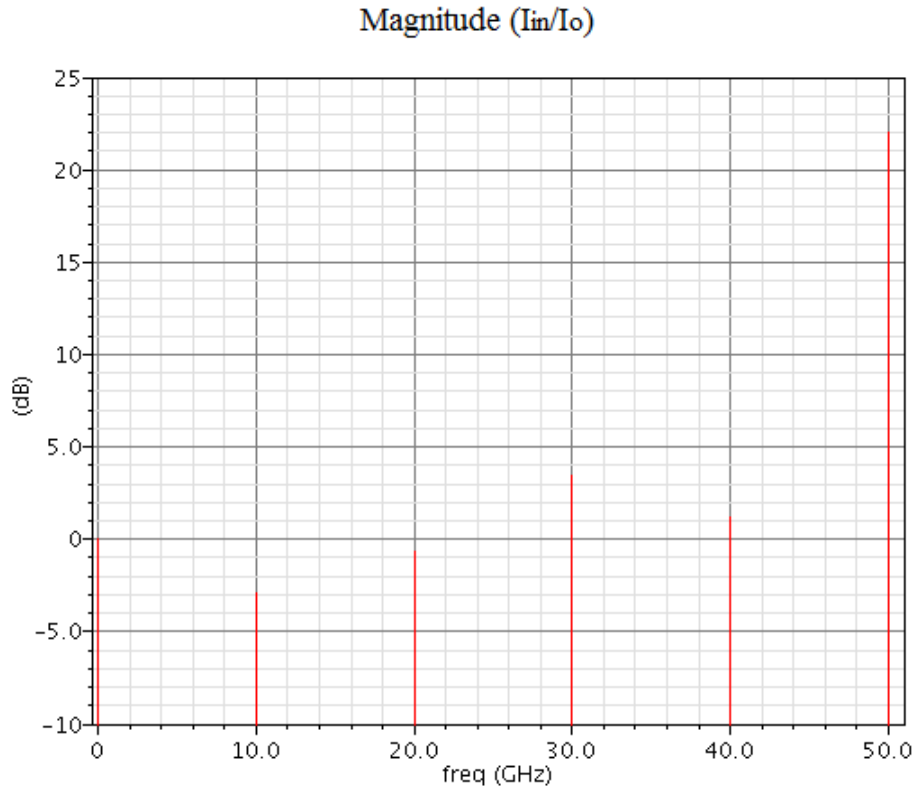


Fig. 5.2: Magnitude transfer function between LO stage input current, I_{IN} , and RF stage output current, I_O .

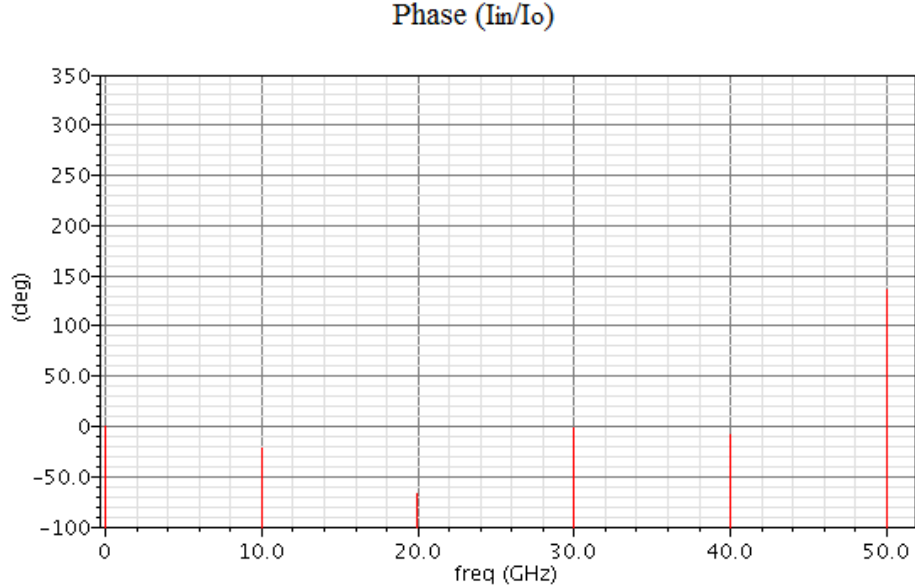


Fig. 5.3: Magnitude transfer function between LO stage input current, I_{IN} , and RF stage output current, I_O .

5.2 Results

The results showed come from post-layout simulations. The testbench used is illustrated in paragraph 7.1.

As fig. 5.4 shows, this doubler provide negative conversion gain due to different reasons: an imbalance on the output signal (as fig. 5.6 shows) due to the miss of phase quadrature doesn't maximize the voltage swing resulting in a lower conversion gain, furthermore capacitors $C_{9,10}$ reducing the bandwidth reduce the gain at high frequency as well. Fig 5.6 depicts the output balance versus the input frequency. This doubler is much more sensitive to the frequency variation respect to the previous one.

The DC current is the same for each doubler, so the DC power absorption is of 45 mW.

The doubler chip size is $640 \times 200 \mu m^2$. Obviously the chip size increase as frequency decrease since a bigger devices as transmission lines are needed.

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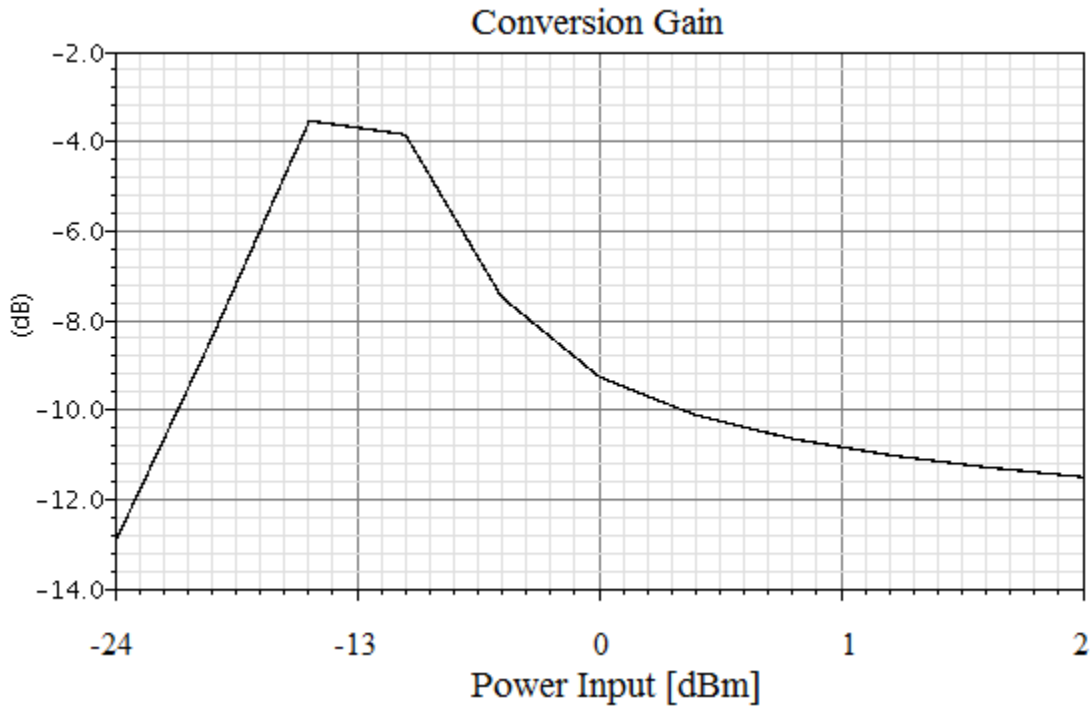


Fig. 5.4: Nominal conversion gain versus input power, reference terminals $OUT_2, OUTX_2$ and IN_2, INX_2 .

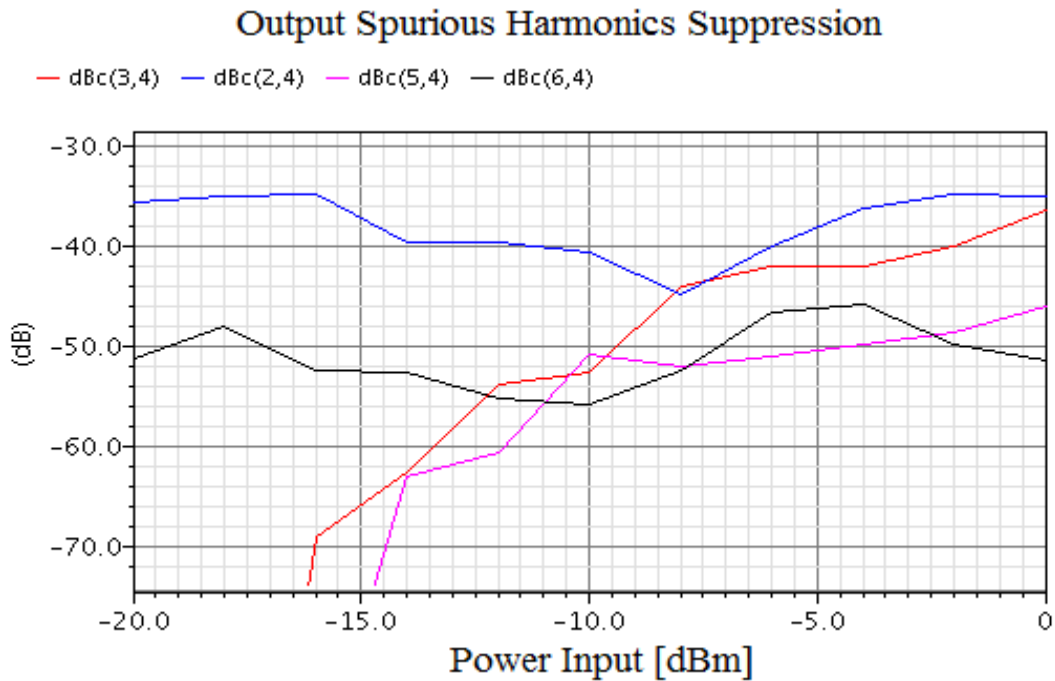


Fig. 5.5 : Nominal spurious harmonics suppression versus input power.

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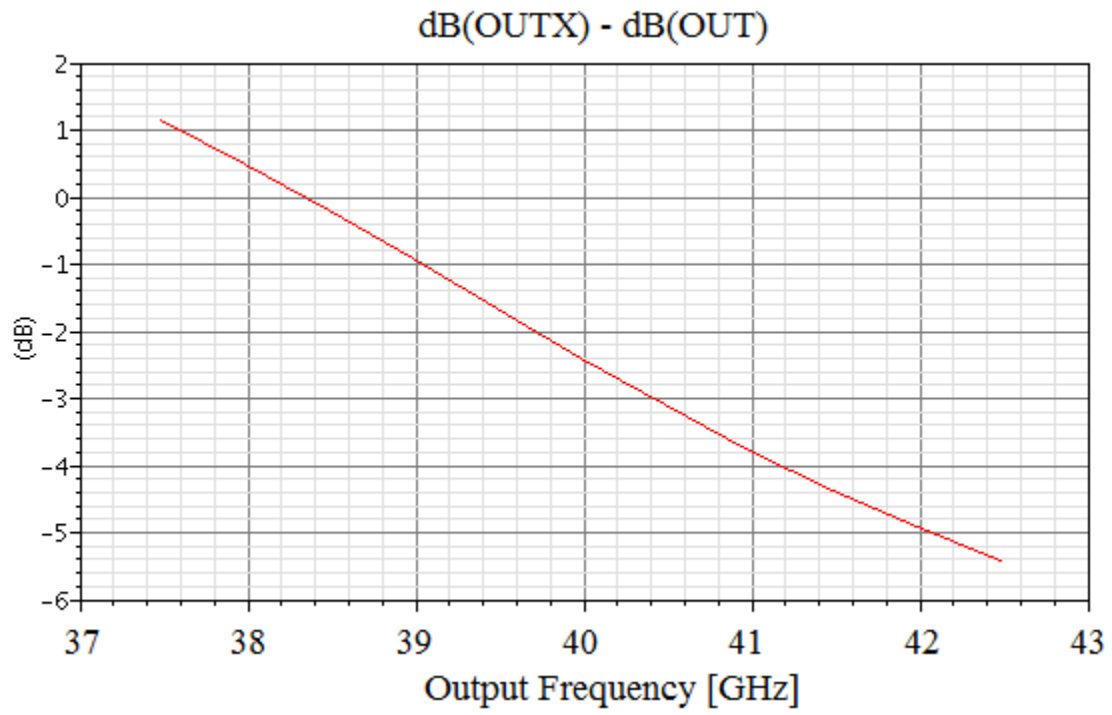


Fig 5.6 : Output power difference versus input frequency.

5.3 40 GHz Frequency Doubler *Inductive Version Design*

For the 40 GHz frequency doubler, another solution, which avoid the use of transmission lines has been designed. Since for the fundamental frequency at 20 GHz the area costs concern the microstrips start to be expensive, a lumped solution has been used, allowing an area saving of 23% respect to the previous *Cap* version. The 40 GHz frequency doubler *inductive* version as well as the 80 GHz octupler *inductive* version doesn't present potential instabilities. Both circuits are unconditionally stable.

Phase quadrature is achieved still using a LC network, but in this circuit the two elements are the base-emitter junction capacitance of the RF transistors T1,T2 and the inductor L_1, L_2 at their emitter node.

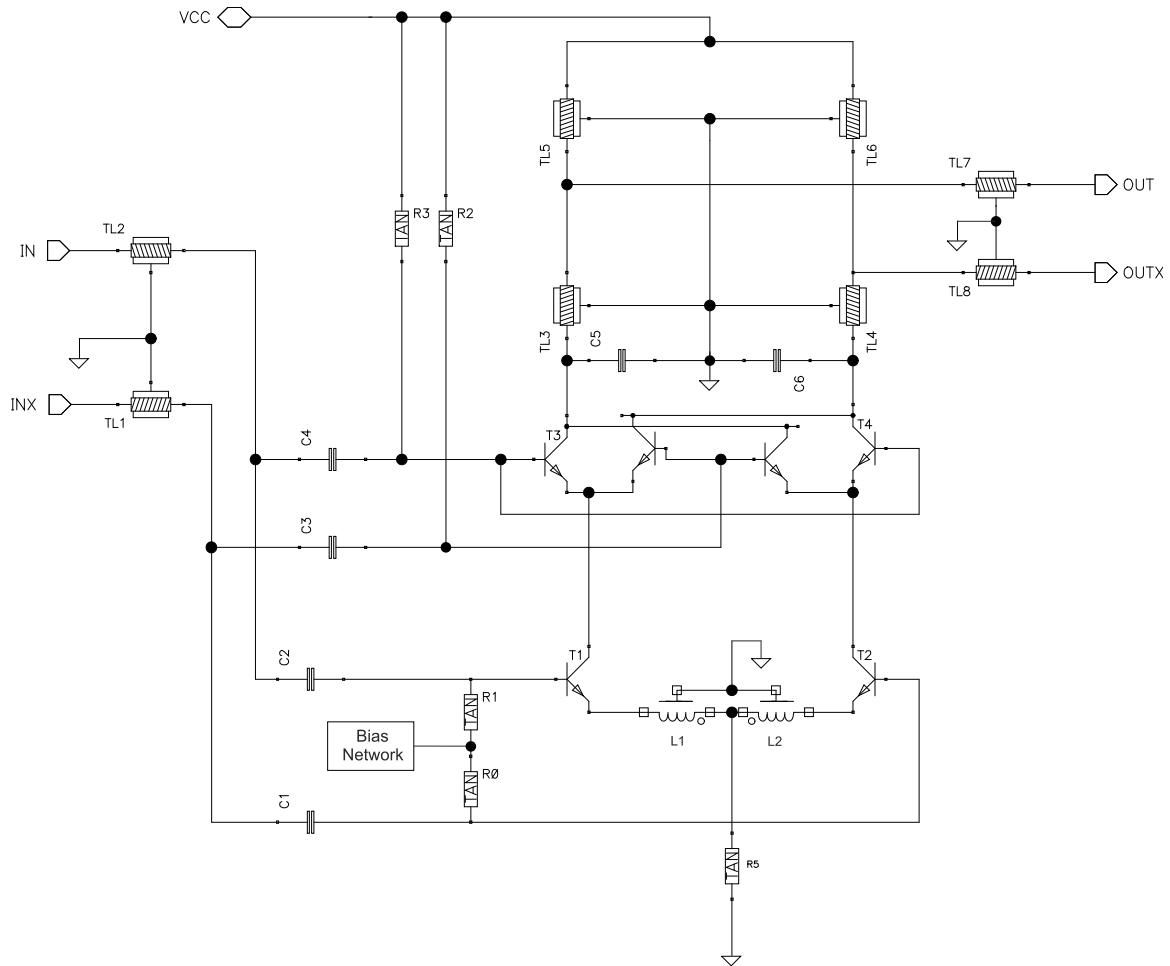


Fig. 5.7: 40 GHz frequency doubler *Coil* version.

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The challenge in the design of these inductors is to provide a high quality factor and a self resonance frequency higher than the fundamental frequency in order that these devices have a good inductive behavior.

Each inductor is used together with base-emitter capacitance to create a RLC filter tuned at the fundamental frequency in order to achieve the phase quadrature since at the resonance frequency the phase shift achieved is 90° . The resistive element “R” is provided from the inductor parasitic resistance and from the base-emitter resistance of RF transistor. Resistive elements have an influence on the filter quality factor.

The RF stage small signal circuit is showed in fig. 5.8, where the relationship between the output current I_o and the driver voltage V_{in} is given by (5.1) through (5.2). Base resistance r_b is low since the transistor configuration is BEBC while R_p includes the parasitic resistance due to the inductor and the emitter resistance.

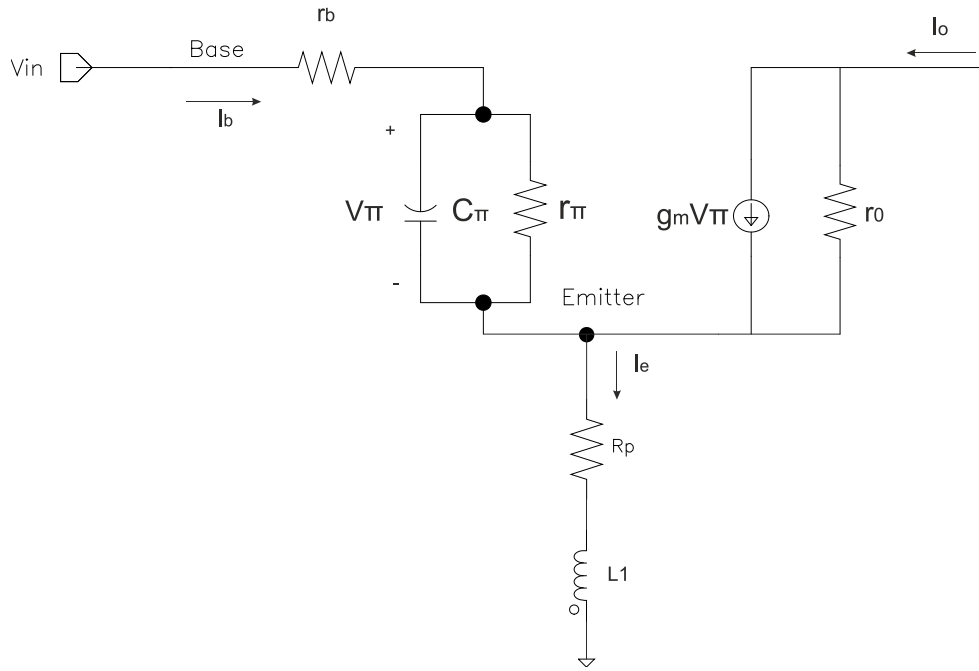


Fig 5.8: RF stage small signal circuit.

Neglecting r_o since is around several $K\Omega$, the output current is given by:

$$I_o \cong g_m * V_\pi = g_m * f(V_{in}) \quad (5.1)$$

The relationship between V_π and the input voltage V_{in} is given by (5.2):

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$$\begin{aligned} V_{\pi} &= V_{in} - r_b * i_b - (R_p + sL_1) * i_b * [\beta(j\omega) + 1] \\ &= V_{in} - \frac{V_{\pi}}{Z_{\pi}} * [r_b + (\beta(j\omega) + 1) * (R_p + sL_1)] \end{aligned}$$

Considering $\beta(j\omega) \gg 1$ at 20 GHz the final formula results:

$$\frac{V_{\pi}}{V_{in}} \cong \frac{1}{1 + g_m \left(R_p + \frac{r_b}{\beta(j\omega)} \right) + s \left(C_{\pi} r_b + L_1 g_m + C_{\pi} r_{\pi} R_p g_m \right) + s^2 [\beta(j\omega) L_1 C_{\pi}]} \quad (5.2)$$

The DC term “ $g_m \left(R_p + \frac{r_b}{\beta(j\omega)} \right)$ ” influences the quality factor, the resonance frequency and the transducer gain, however assuming $\beta(j\omega) \gg 1$ and $g_m R_p \ll 1$ its effect is negligible.

The resonance frequency f_r associated to the poles complex and conjugate is given by:

$$f_r \cong \sqrt{\frac{1}{\beta(j\omega) L_1 C_{\pi}}} \quad (5.3)$$

Hence placing the resonance frequency at 20 GHz (fundamental frequency) the RF stage output current I_o is shifted by 90° respect to V_{in} therefore the phase quadrature between RF and LO path is achieved. Resistances R_p , r_b cause a lowering of the filter quality factor reducing the peak gain. Since the poles lie at the same frequency of the input signal, the quality factor plays an important role. A low quality factor has a peak gain bell-shaped wider, providing lower gain but more constant over frequency; a high quality factor instead produce a higher bell-shaped peak gain, however the gain is more frequency sensitive being more selective. Since the input signal has a specified bandwidth, it is desirable that the gain and phase shift within this range don't change much, thus the quality factor of the couple of poles has to be smaller than that one corresponding to the input signal so the phase shift provided is the same over all frequency band.

If the input signal has a bandwidth f_{-3dB} centered at the fundamental frequency f_0 , the filter quality factor Q_{RLC} has to be:

$$Q_{RLC} < \frac{f_0}{f_{-3dB}} \quad (5.4)$$

Since the resonance frequency (5.3) depends on the current gain $\beta(j\omega)$, the transistor is optimally biased to achieve the maximum gain in order to reduce the inductor size.

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A low quality factor Q_{RLC} is also necessary since several transistor parameters depend on the operative conditions; the forward DC current gain β_0 for example is highly temperature sensitive as shown in figure 5.9. With a high quality factor Q_{RLC} together with β variations, the poles of the transfer function can move resulting in a phase shift not longer 90° . With a low Q_{RLC} instead the filter is much less sensitive from parameter variations.

The technology of the HBT transistors already provide a considerable base resistance which keep the Q_{RLC} much lower than that one corresponding to the input signal and as proof the outputs difference between OUT/OUTX is shown versus frequency and temperature variation (fig. 5.15, 5.10). From fig. 5.15, within the frequency range the difference between the two outputs is smaller than 1 dB. From fig. 5.10, although β_0 is strongly temperature sensitive the two outputs slightly differ by 0.1 dB within the specified temperature range.

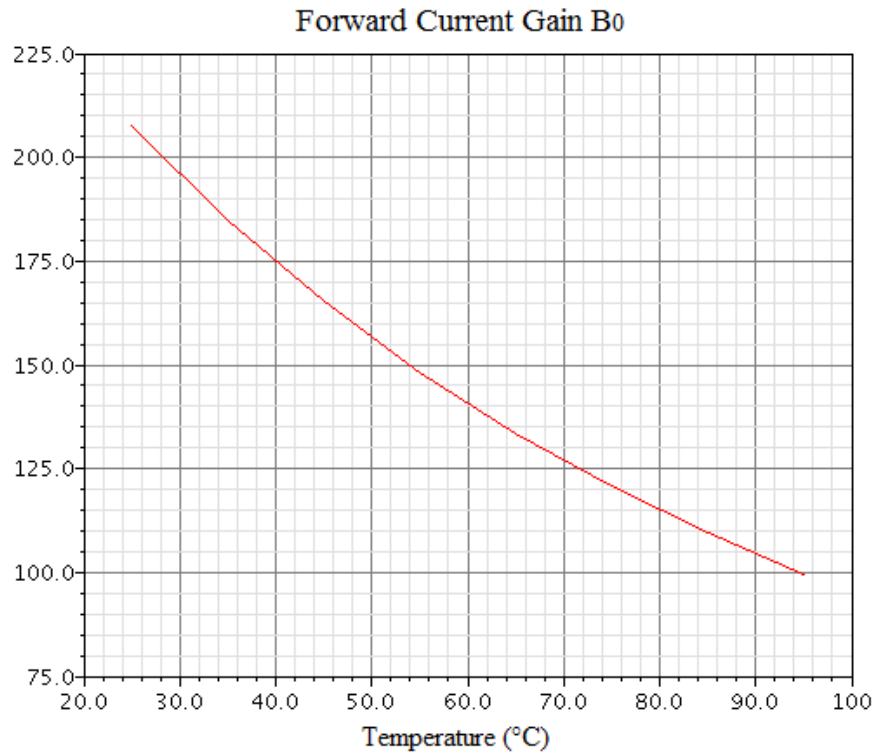


Fig. 5.9 : Forward current gain β_0 versus temperature.

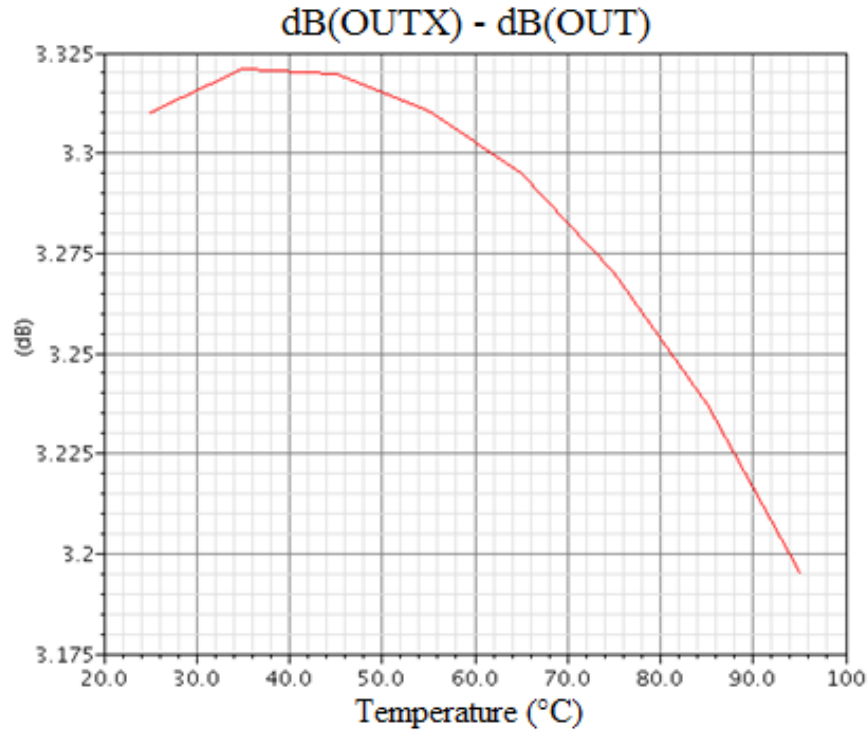


Fig. 5.10: Difference between the two output branches versus temperature.

The inductor design require several iterations before to achieve the performance expected. The topmost metal layer has been used since is the thickest and lowest in resistance. Furthermore, maximizing the distance from the substrate the parasitic capacitance between inductor and substrate is minimized. In order to get the maximum performance, an octagonal shape for the planar spiral inductor has been used which show moderately better characteristics than squares typically on the order of 10% [Lee:98].

The inductor self resonance frequency has to be higher than the second/third harmonic thus the inductive reactance, which increase linearly with the frequency, degenerate the RF transistor lowering the gain for the upper spurious harmonics. Above the self resonance frequency the inductor behaves as parasitic capacitor.

Once specified the features of the inductor, inductance can be calculate from the formula (5.3) since current gain $\beta(j\omega)$ and base-emitter capacitance C_π are already known from simulation. In particular C_π is given by the junction capacitance C_{je} and the base charging capacitance C_b :

$$C_\pi = C_{je} + C_b = C_{je} + \tau_F \frac{I_C}{V_T} \quad (5.5)$$

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From (5.3), set $f_r = 20 \text{ GHz}$, has been obtained an inductance for each inductor of $L_1 = L_2 = 0.37 \text{ nH}$. The parasitic resistance due to the metallization layer is around 0.8Ω .

For an accurate inductor design, *Sonnet EM* simulator provide S-parameters analysis that allows to develop a high accuracy double- π model which is used to simulate the behavior of the device in the schematic.

The self resonance frequency, extracted from S-parameters, is almost at 40 GHz because of the value of inductance that is such big that a big inductor is needed, so the parasitic effects increase lowering the self resonance frequency. Although the inductor is considerably big, its length is of $550 \mu\text{m} < \frac{\lambda_g(20\text{GHz})}{10}$ so it can effectively be considered as lumped element for the fundamental frequency.

As shows in fig. 5.11, for frequencies around 40 GHz inductor behaves as parasitic capacitor, so the small signal circuit of fig. 5.8 can be considered capacitive degenerated with a resistor in parallel to provide a DC path. These considerations bring to the equivalent circuit as in fig. 5.12. It is necessary to keep in mind that this model has to be used just above the inductor resonant frequency and where the imaginary part shows a capacitive behavior.

Since in this frequency range lie the second harmonic, the influence of capacitive degeneration has been studied.

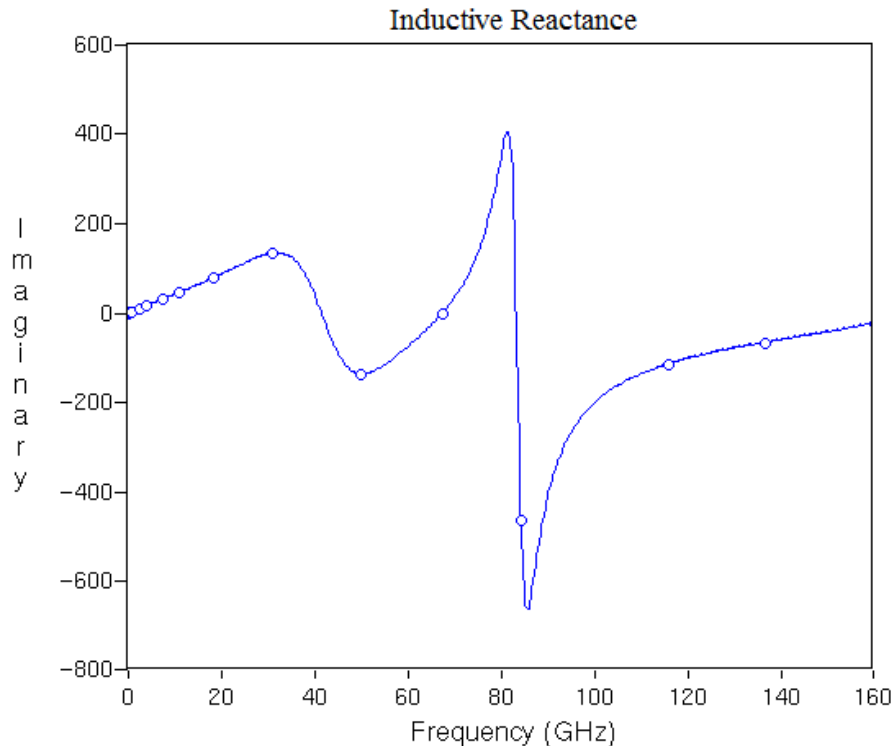


Fig 5.11: Imaginary part of inductor input impedance.

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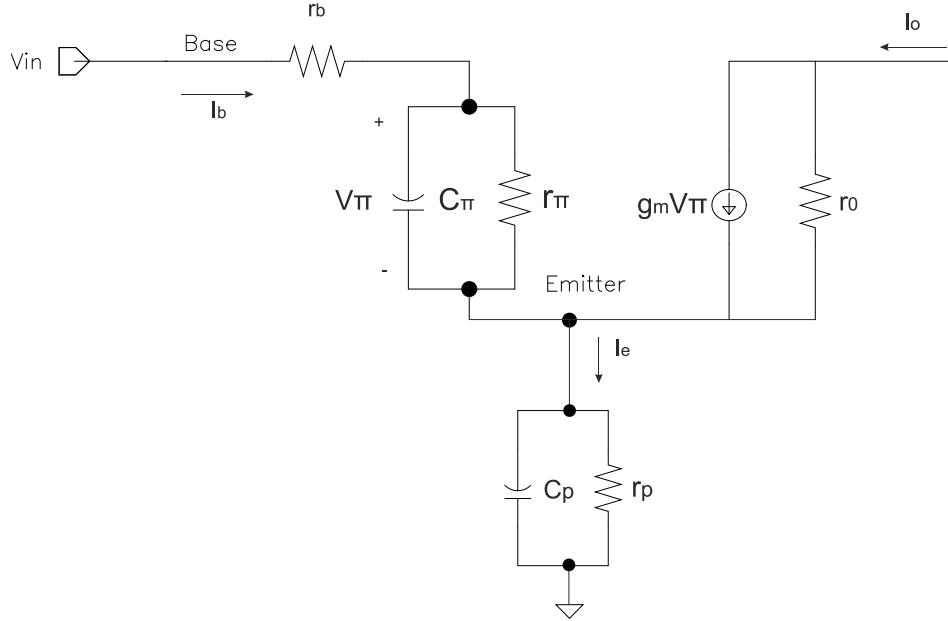


Fig. 5.12: RF stage small signal circuit @ 40 GHz.

The analysis performed is the same of the previous one (5.1), (5.2). Since the output current depends on the voltage across base-emitter, the V_{π}/V_{in} relationship has been re-examined.

From fig. 5.12 the output current is given by (neglecting r_o):

$$I_o \cong g_m * V_{\pi} = g_m * f(V_{in}) \quad (5.6)$$

$$V_{\pi} = V_{in} - r_b * \frac{V_{\pi}}{Z_{\pi}} - V_{\pi} * \left(g_m + \frac{1}{Z_{\pi}} \right) * \frac{R_p}{1 + sC_p R_p} \quad (5.7)$$

Assuming that $r_{\pi} \gg r_b, R_p, g_m R_p r_{\pi}$ results:

$$\frac{V_{\pi}}{V_{in}} \cong \frac{1 + sC_p R_p}{1 + s(C_p R_p + C_{\pi} r_b) + s^2 C_{\pi} R_p C_p R_b} \quad (5.8)$$

Therefore whether up to the self resonance frequency the inductor degenerate the transistor decreasing the transducer gain, above that the parasitic capacitor C_p together with C_{π} create two poles complex and conjugate with a quality factor Q_p that could increase the gain for the upper spurious harmonics.

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The zero and poles in (5.8) are far apart being the product $C_p R_p$ very small since is due to parasitic elements.

The frequency f_p associated to the poles and their quality factor Q_p are given by:

$$f_p = \frac{1}{2\pi\sqrt{C_\pi R_p C_p r_b}} \quad (5.9) \quad Q_p = \sqrt{\frac{C_p R_p}{C_\pi r_b}} * \frac{1}{1 + \frac{C_p R_p}{C_\pi r_b}} \quad (5.10)$$

If f_p is placed around 40 GHz, a high quality factor Q_p can provide unwanted gain for the spurious harmonics.

From fig. 5.11, around 40 GHz, $C_p = 30 \text{ fF}$ has been calculated that results many time smaller than C_π , moreover being the metallization layer very less resistive its parasitic resistance R_p results much smaller than base resistance. Hence $\frac{C_p R_p}{C_\pi r_b} < 1$ therefore $Q_p < 1$ and the gain provided for the spurious harmonics within this frequency range is always ≤ 1 .

Capacitors C_5, C_6 (fig. 5.7) as mentioned are implemented to reduce the transistors bandwidth, in this way the gain at high frequency is reduced as well the potential instability issues.

5.4 Results

The results showed come from post-layout simulations. The testbench used is illustrated in paragraph 7.1.

Fig. 5.13 shows the conversion gain which is always negative. The main reason is probably due to the low Q_p that provides a low transducer gain.

Capacitors $C_{5,6}$ also have a role in the conversion gain reduction since they limit the bandwidth. The spurious harmonics suppression is always greater than 30 dBc. The outputs difference versus input frequency (fig. 5.15) show that the phase shift network is little sensitive to frequency variation and this thanks to low Q_p .

The DC current is the same for each doubler. The DC power absorption is 45 mW.

The doubler chip size is $520 \times 200 \mu\text{m}^2$.

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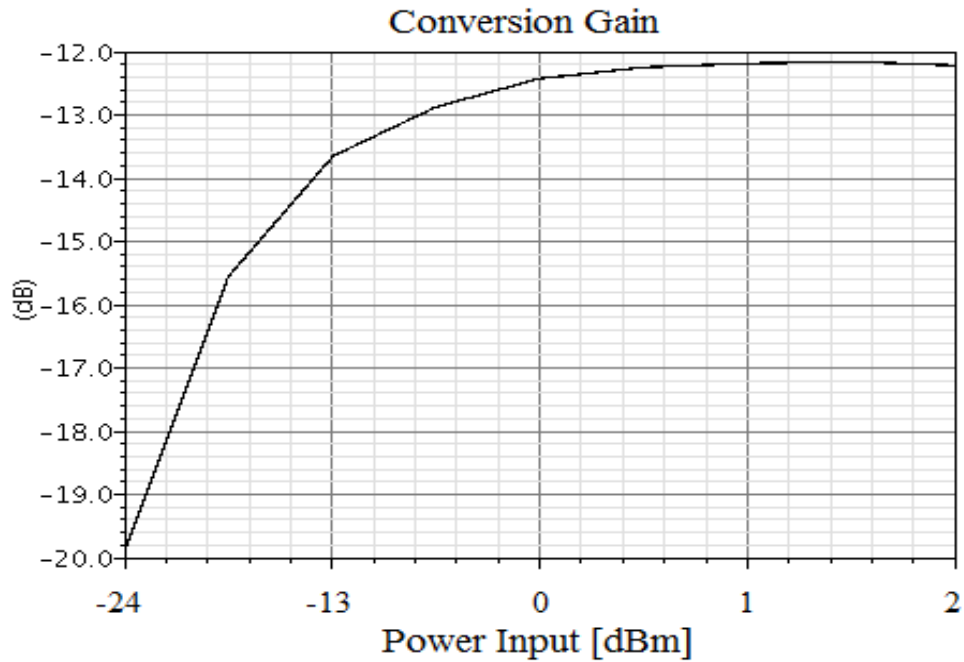


Fig. 5.13: Nominal conversion gain versus input power, reference terminals $OUT_2, OUTX_2$ and IN_2, INX_2 .

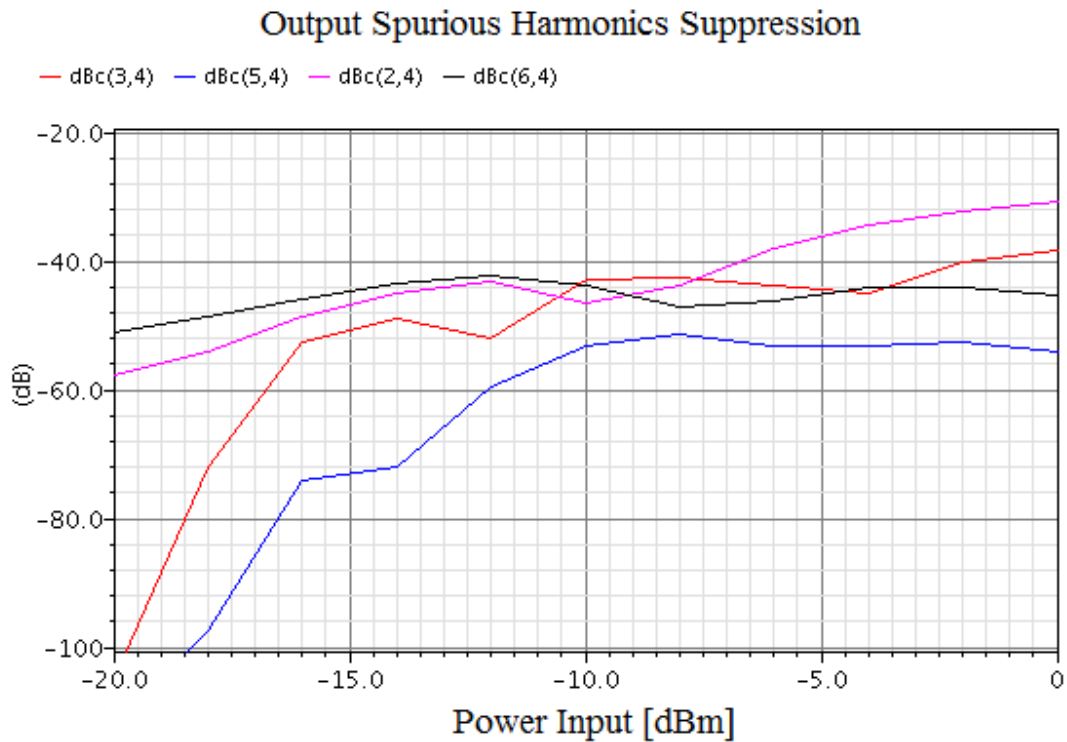


Fig. 5.14: Nominal spurious harmonics suppression versus input power.

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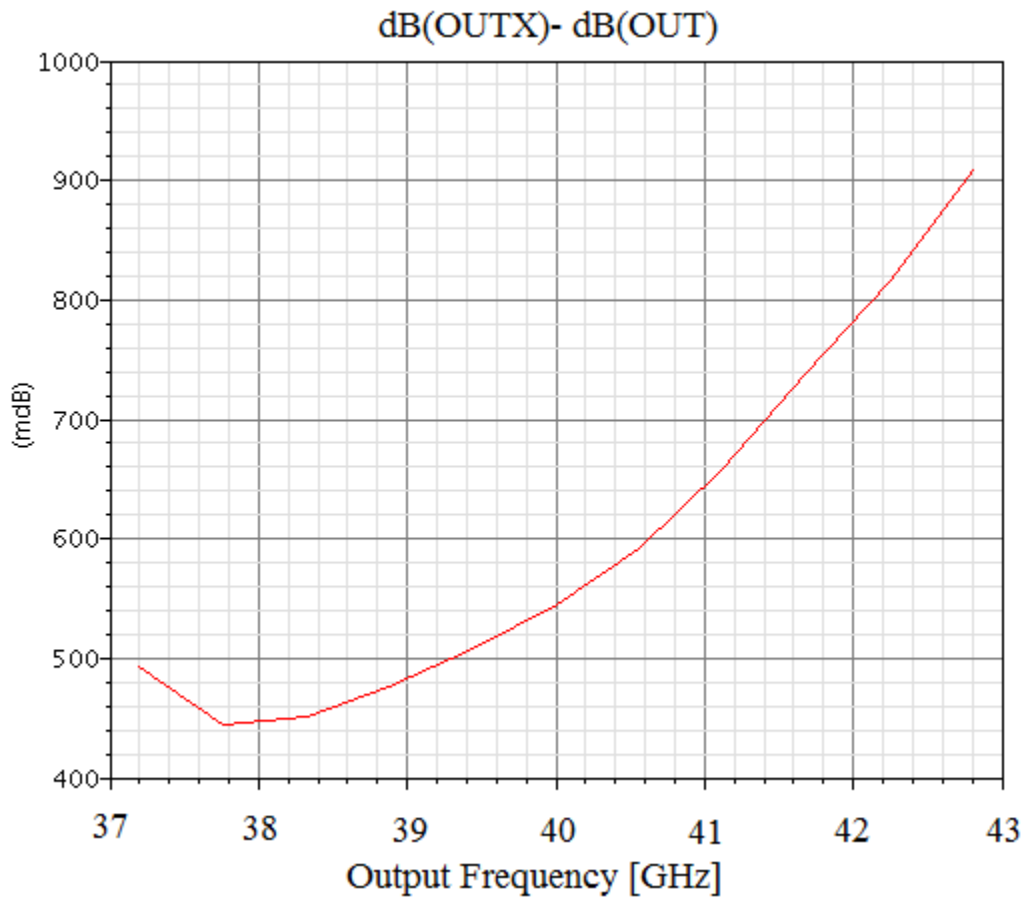


Fig. 5.15: Output power difference versus input frequency.

6 20 GHz Frequency Doubler

6.1 20 GHz Frequency Doubler Design

For the 20 GHz frequency doubler, only lumped solutions can be used since the fundamental signal at 10 GHz has a wavelength comparable to the chip size. For achieve the phase quadrature, although a RLC network as in the 40 GHz frequency doubler *inductive* version is possible, it might results costly in terms of area and troublesome for the chip functionality since in one single chip several inductors will be implemented and mutual coupling might be triggered. Moreover since the input signal is at low frequency, (low for this technology) smaller transistors has been used resulting in a lower base-emitter capacitance; therefore to achieve the phase quadrature large inductors should be necessary resulting in a even more large area occupancy.

The new circuit topology is composed of an active network made of emitter followers which introduce the necessary phase shift. A slightly different bias network than that one described in paragraph 8.1 has been implemented with one more mirror transistor stacked (T11). Although it is different it works at the same way as described in the paragraph previously mentioned.

Inductors $L_{1,2}$ and parasitic inductances $L_{C\ 1,2}$ together with the parasitic capacitors at the collector nodes of LO stage tune the output matching network to maximize the voltage matching at 20 GHz within the specified frequency band.

$L_{1,2}$ are connected to node collectors of LO stage by a long path due to layout requirements (see octuplers layout), so $L_{C\ 1,2}$ represent the parasitic inductances of these interconnections.

The phase shift network in fig. 6.1 is composed of resistors $R_{4,5}$, emitter followers T1, T2 and differential capacitor C_{diff} .

The transistors belong to the Gilbert cell are High Speed devices with $f_T = 170$ GHz while the emitter followers T1,T2 are High Voltage Transistors with $f_T = 35$ GHz.

The transistors configuration belong to the Gilbert cell is the same as in the previous doublers.

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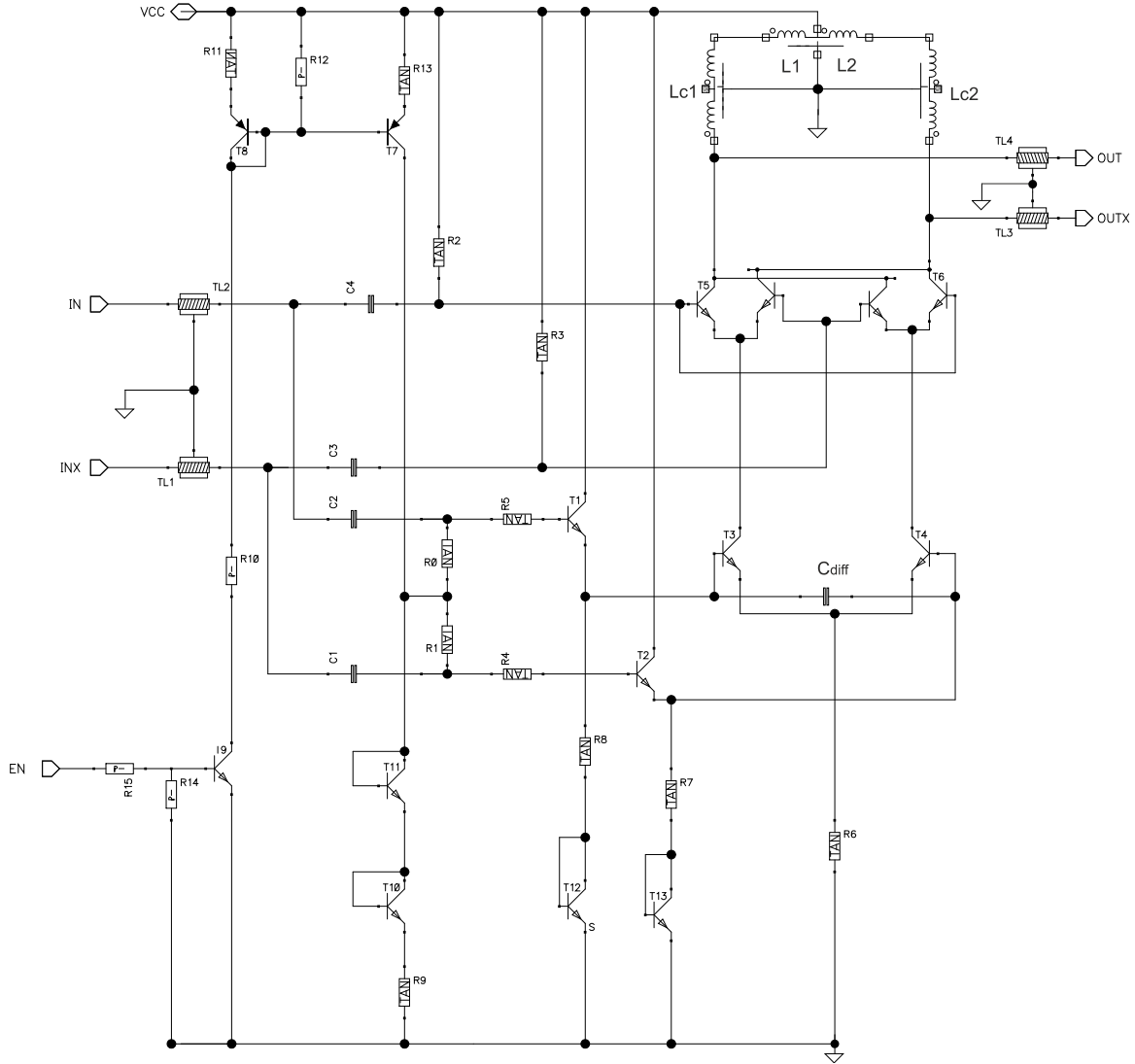


Fig 6.1: 20 GHz frequency doubler.

In fig. 6.2, 6.3 the phase shift network and its small signal circuit are depicted, where R_{eq} denotes the parallel connection of the emitter follower (E.F.) output resistance and the load resistance, R_s is composed of series resistance R_5 plus the transistor base resistance r_b , while C_L is the capacitive load at the output due to the parasitic capacitance of T12 and input capacitance of RF transistor T3. Although C_L is not directly connected in parallel with $2 * C_{diff}$ because there are R_8 and R_6 that decouple, in this study to extract a useful formula a simplification has been taken and C_L has been placed in parallel with $2 * C_{diff}$.

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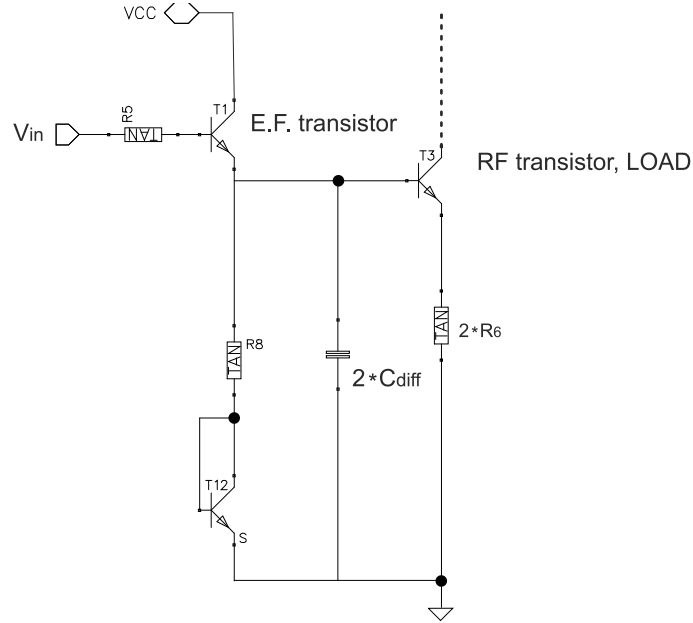


Fig. 6.2: Phase shift network.

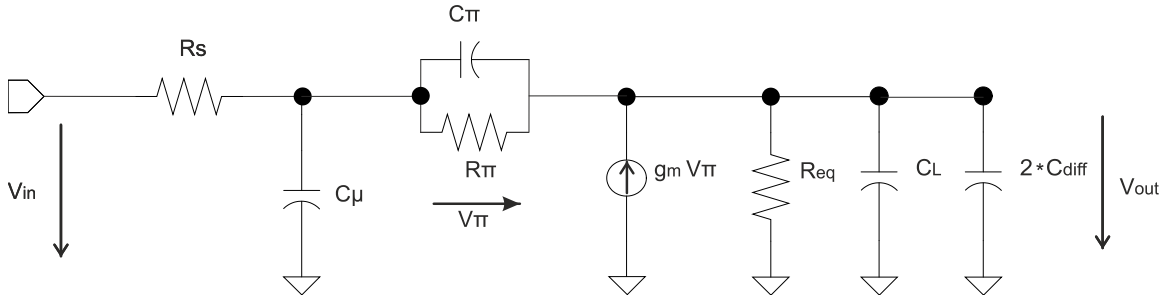


Fig. 6.3: Small signal model of a capacitive loaded emitter follower.

The voltage gain of the capacitive loaded emitter follower has a frequency dependence that is analogous to the frequency dependence of the transfer function of an RLC series resonant circuit [Trotta:07,2].

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{1}{1+s\left[R_S C_\mu + \left(\frac{1}{g_m} + \frac{R_S}{\beta}\right)(C_L + 2*C_{diff}) + \frac{R_S*(C_L + 2*C_{diff})}{\omega_T R_{eq}}\right] + s^2 \frac{R_S*(C_L + 2*C_{diff})}{\omega_T}} \quad (6.1)$$

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With a resonance frequency given by:

$$f_r = \sqrt{\frac{f_T}{R_s*(C_L+2*C_{diff})}} = \sqrt{\frac{f_T}{(r_b+R_{4,5})*(C_L+2*C_{diff})}} \quad (6.2)$$

And a damping factor:

$$\delta = \left(\frac{C_\mu}{2*(C_L+2*C_{diff})} + \frac{1}{2R_s g_m} + \frac{1}{2\beta} \right) \omega_T + \frac{1}{2R_{eq}(C_L+2*C_{diff})} \quad (6.3)$$

As in the second order system, once knew the transition frequency f_T from the biasing current (fig. 2.4), R_s and C_{diff} can be choose in order to set the resonance frequency f_r to equals the fundamental input frequency. Since in this doubler $f_r = 10 \text{ GHz}$, the $f_T = 170 \text{ GHz}$ of High Speed transistor is too high to afford of use small values for the components R_5 and C_{diff} . A big R_5 introduce wideband losses in the signal path, lowering the voltage delivered to RF stage and reducing the conversion gain. A big capacitor C_{diff} instead should to be avoided in order to keep the damping factor large enough to prevent oscillations and instability [Trotta:07,2]. Moreover a low damping factor is unwanted in order to keep the sensitivity of the voltage gain versus frequency low at the resonance frequency.

Therefore the study focused on an transistor with low transition frequency f_T to reduce the values of R_5 and C_{diff} . Since this technology provide further NPN devices, a High Voltage transistors with $f_T = 35 \text{ GHz}$ for T1 and T2 have been chosen. The transistors configuration is BEC in order to maximize the base resistance which helps to choose a low value for $R_{4,5}$ and at the same time to prevent potential instability issues due to capacitive degeneration that might create a negative input resistance.

Since the two terminals at which C_{diff} is connected are symmetrical, C_{diff} is composed of two capacitors cross coupled to reduce the mismatch due to bottom and top plates. Upon T12, T13 resistors $R_{7,8}$ minimize the capacitive parasitic effects due to collector-substrate capacitances.

The main problem in using emitter follower capacitive loaded is a potential instability that could comes from the input impedance real part that could becomes negative at high frequencies. Especially oscillations can be triggered when an inductive source impedance supported by an inductive behavior of the connection line drive a capacitive input impedance combined with negative real part as could be in this case. In this case the complex and conjugate poles of the voltage transfer function move to the imaginary axis, bringing the emitter follower in the unstable region. The inductive source impedance in series with the capacitive reactance form a LC tank where oscillation and instability result at frequencies where

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$R_{source}(\omega) + R_{input,E.F.}(\omega) < 0$. Since $R_{source}(\omega)$ is fixed, in order to prevent that, $R_{4,5}$ must to be chosen large enough to compensate the negative real part of the input impedance produced by C_{diff} .

The frequency at which the input impedance real part of the circuit showed in fig. 6.3 becomes negative is approximately given by (neglecting C_{μ}) [Trotta:07,2]:

$$\omega_0 = \sqrt{\frac{\omega_T}{\beta_0[R_{eq}(C_L + 2 * C_{diff}) - 1/\omega_T]}} \quad (6.4)$$

Where β_0 is the low frequency current gain of E.F. transistor.

The formula (6.4) shows that choose a device with low ω_T allows a high time constant $R_{eq}(C_L + 2 * C_{diff})$ without encounter any instability issue since ω_0 is shifted at high frequency whereas f_r is at low frequency.

The final values are: $R_{4,5} = 180\Omega$ and $C_{diff} = 230\text{fF}$.

6.2 Results

The results showed come from post-layout simulations. The testbench used is illustrated in paragraph 7.1.

The conversion gain is almost always positive providing high gain for low input power. This result comes since the phase shift network provide the phase quadrature maximizing the output swing and the RF transistors have a high gain working at low frequency. Moreover in this doubler there are not the capacitors at collector nodes of LO stage so the gain at high frequency is unaffected.

Fig 6.6 shows that the 90° phase shift network is very less sensitive to frequency variations and this thanks to the high damping factor δ of the network.

Since there are more transistors than the other doublers, but the size is reduced, the DC current is the same. The DC power absorption is of 45 mW.

The doubler chip size is $520 \times 260 \mu\text{m}^2$.

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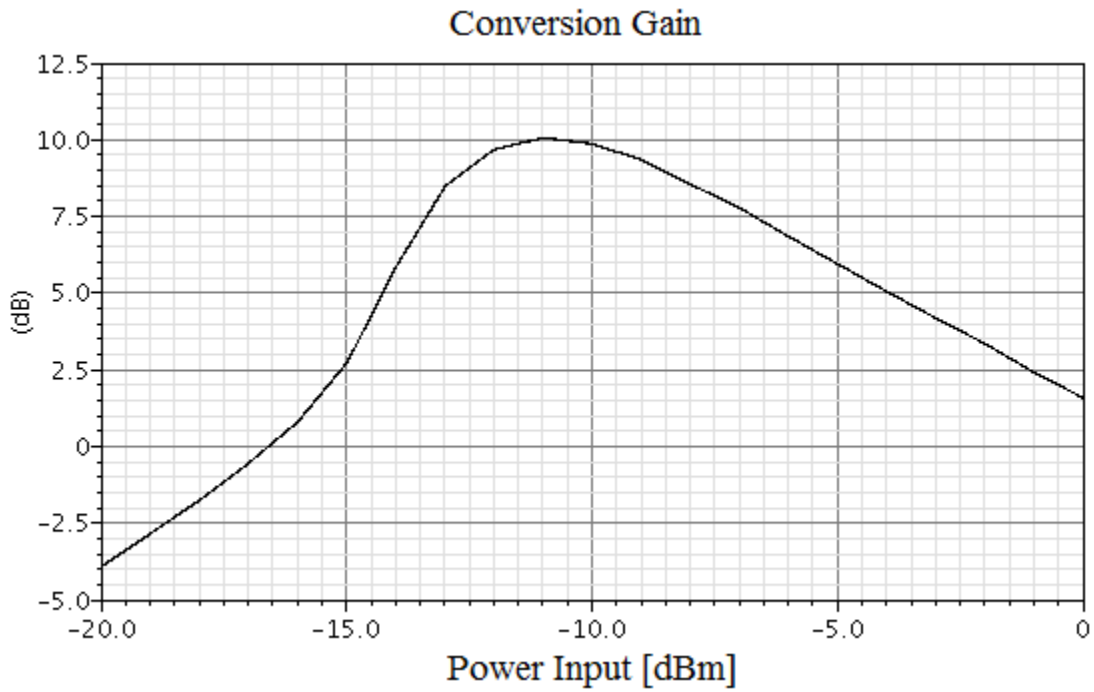


Fig. 6.4: Nominal conversion gain versus input power, reference terminals $OUT_1, OUTX_1$ and IN, INX .

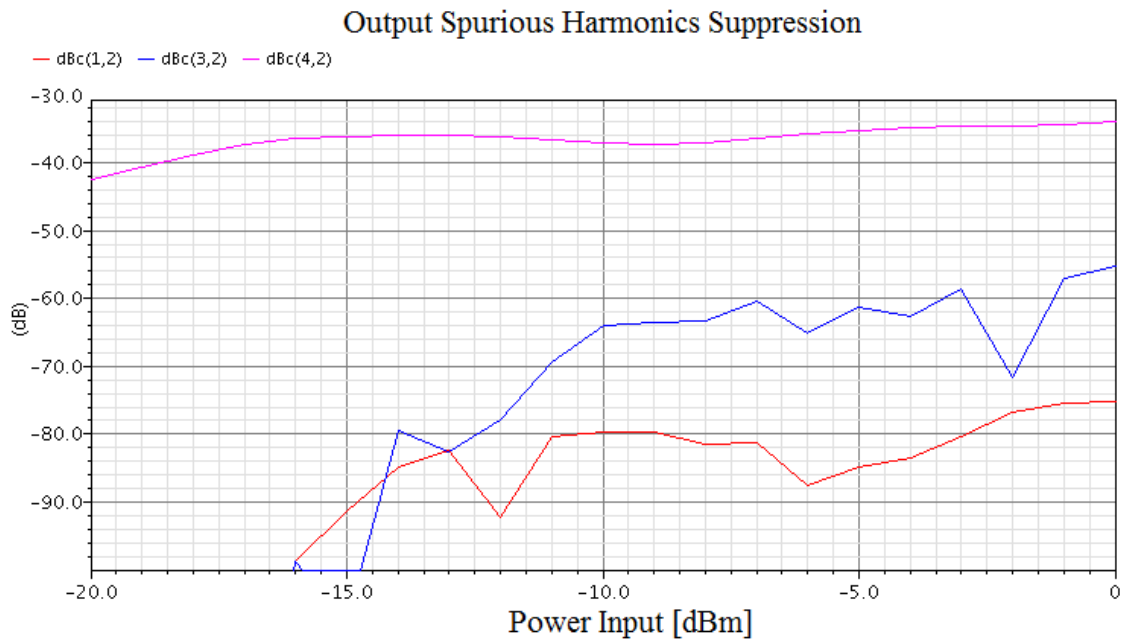


Fig. 6.5: Nominal spurious harmonics suppression versus input power.

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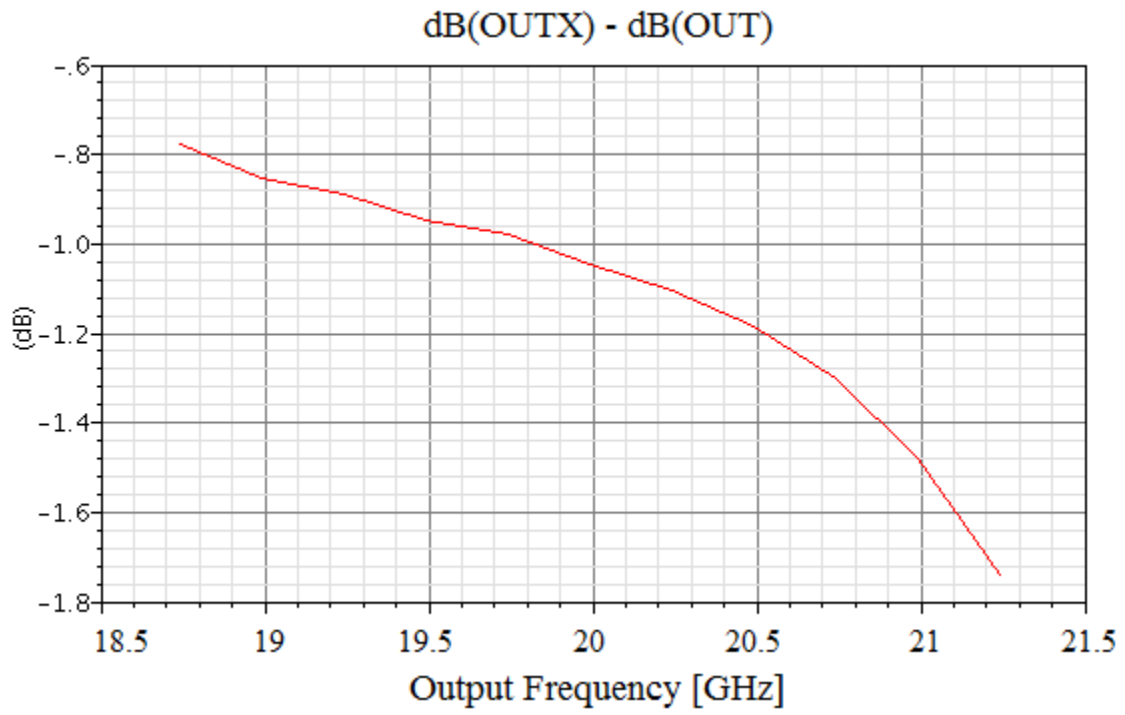


Fig. 6.6: Output power difference versus input frequency.

7 80 GHz Frequency Octuplers

7.1 80 GHz Frequency Octuplers Design & Layout

This chapter aim to present the results of the cascade of three frequency doublers in both topologies, *Cap* and *Coil* version. Each octupler take the name from the version of 40 GHz frequency doubler that they implement.

Best performances come from the octupler *capacitive* version although the area occupancy is higher than *inductive* one.

The most problematic from the design point of view was been the octupler *Cap* version since a strong instability lied within the signal bandwidth between the second and third doubler (now fixed).

From layout point of view, since the frequency range is within the millimeter waves the signal paths must be as much as possible symmetrical to avoid any delay in one single way that would be traduced in a signal not longer differential. The distributed phase shift networks as in the 40 and 80 GHz doublers need a careful layout since the parasitic effects due to the interconnection wires between transmission lines and capacitors are not well known. As the capacitors must be very close to the transmission line, at the same time also the transmission lines have to be close to the collector/emitter nodes to avoid any inductive path from the interconnections.

Also the capacitors at the collector nodes of LO stage in fig. 5.1, 5.7 have to be very close each other as well as to the collector nodes in order that the connections in the schematic reflect the connection in the layout.

Parasitic inductance of interconnection lines from DC blocking capacitor to transistor base terminal has been simulated and result around 15-23 pH for each doubler. Implemented in the simulation schematic it hasn't shown a considerable lowering of the performances since the signal frequency is still low enough to encounter a low inductive reactance.

About the octupler *Coil* version, inductor design flow recommend to keep the devices 40 μm away from inductor. Since in this octupler the inductors are two the distance between each other was kept higher to avoid coupling. The main task of this layout was focused onto fit the two inductors in the same chip at considerable distance between each other.

The same distance was kept for the transmission lines.

Blocking layers have been used in the critical points of the circuit, such as in the interconnections of two transmission lines where otherwise the auto-filler short-circuit different layers.

Parasitic extraction after layout has been done for the capacitive elements. For the inductive parasitic paths, the rule of thumb gives 0.5 nH/mm, however for more

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reliable results Sonnet EM simulator has been used giving results pretty close to the previous rule.

Both version of octupler chips include a power detector to measure the output power and a ESD protection for each pad to avoid electrostatic discharge. To prevent supply voltage oscillation a thick grid of MIM capacitors has been implemented.

A thick ground and feed planes have been implemented in order to reduce the resistive as well as the inductive path for the current especially important during the switching transient. At the same time, many pads for ground/supply are places around the chip allowing a current to be well distributed.

Testbench

The two octuplers chips made include a chain of three doublers with an output buffer as fig. 1.1 shows. The buffer implemented is a library component so the performances are already well known.

The results presented in this work are referred to the testbench depicted in fig. 7.1. It doesn't include the output buffer since is not significant because here the purpose is to present the results of new frequency multipliers topologies. Components C_{MATCH} , L_{MATCH} represent the input matching network in order to satisfy the specifications about the input reflection coefficient S_{11} (paragraph 1.2, table 1). This network is implemented only in the testbench, not in the chips (see octupler chip layout). In each chip, the input source is directly connected to the input terminals of the doubler.

Components V_1 , R implement the input PORT device, while V_2 , R_{LOAD} are the output PORT. Both R and R_{LOAD} match the corresponding input/output matching networks. V_2 is set equals to 0 V.

All $ENABLE_{1,2,3}$ are connected to VCC supply.

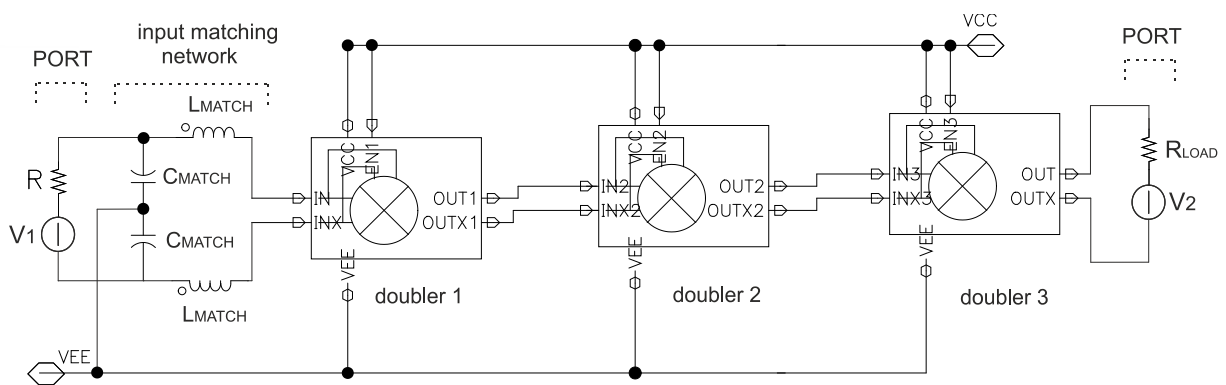


Fig.7.1: Testbench schematic.

The output matching network of doubler no. 1 and 2 is designed to achieve the voltage matching with the input network of the next doubler. The output matching network of the third doubler is matched to a resistive load of 100 Ω .

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The doubler conversion gain is simulated taking as reference terminals OUT/OUTX_X and IN/INX_X of each device sweeping the power available from PORT device.

Doubler conversion gain is simulated from the doublers inserted in the chain since only this configuration represent the real working conditions.

The input/output power graphs are referred to input/output PORT devices.

7.2 80 GHz Frequency Octupler *Capacitive* Version Results

Here the results of the 80 GHz frequency octupler *capacitive* version are shown. All the results are post layout simulations. Montecarlo simulations take in account both process and mismatch variations. The power output of the 8th harmonic is within the range of -1,+2.7 dBm already with an input power of -10 dBm. With an input power of 0 dBm the output power is between 0,+2.9 dBm.

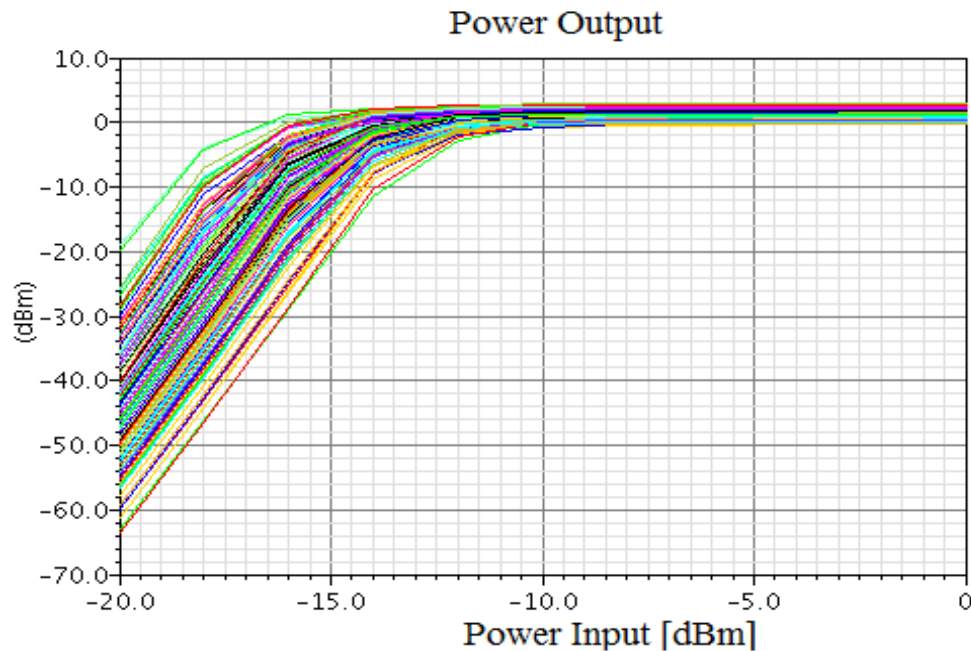


Fig. 7.2 : 80 GHz output power versus input power over 128 montecarlo iterations.

Fig. 7.3 depicts the output signal 3dB bandwidth and as shown it is larger than the specification resulting in a higher resolution for imaging application system. The bandwidth result larger also compared to that one produced from a VCO. The 3dB bandwidth is of 19 GHz centered at 80 GHz.

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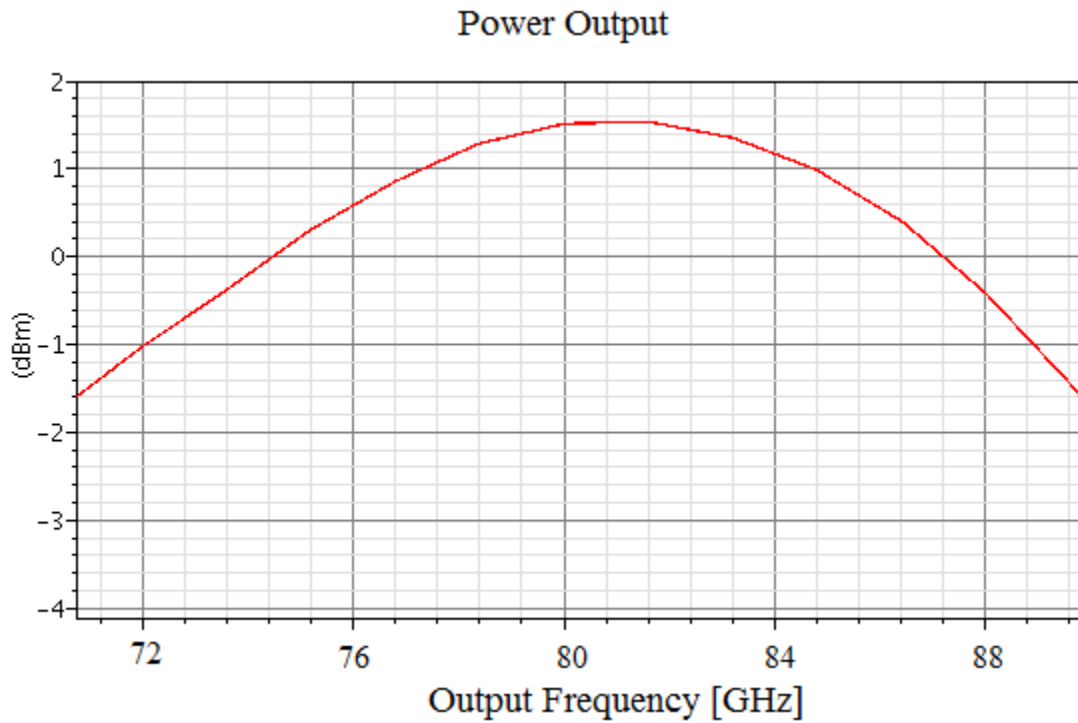


Fig 7.3: 3dB bandwidth of the 8th output harmonic.

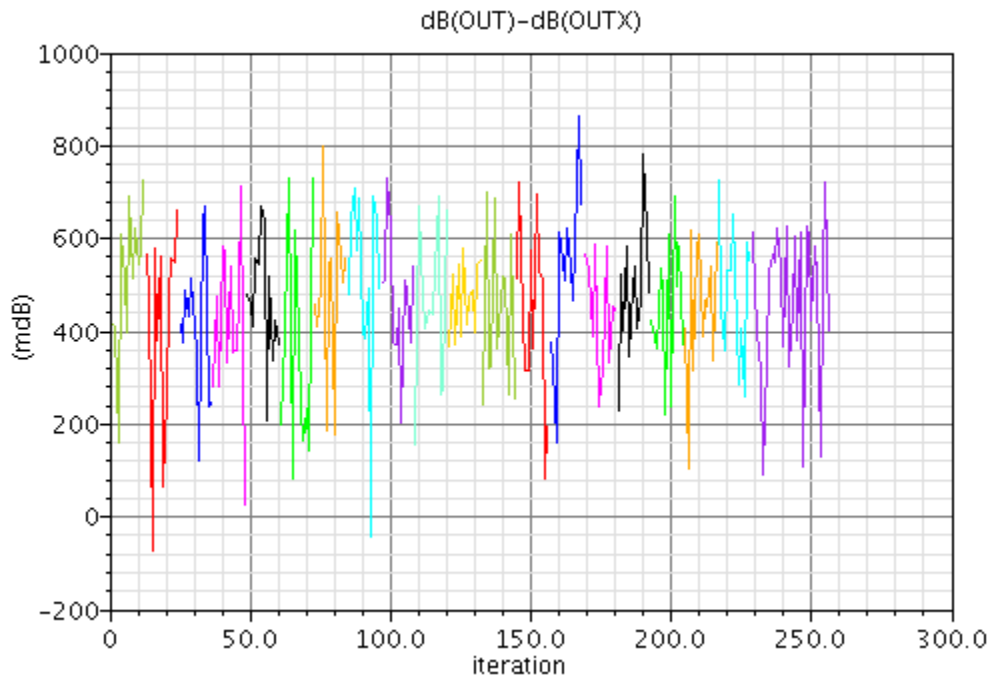


Fig 7.4: Outputs difference versus montecarlo iterations for 0 dBm input power.

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As from specification, suppression of the spurious harmonics closest to the fundamental versus input power for 128 montecarlo iterations is always higher than 30 dBc as depicted from fig. 7.5 to 7.8.

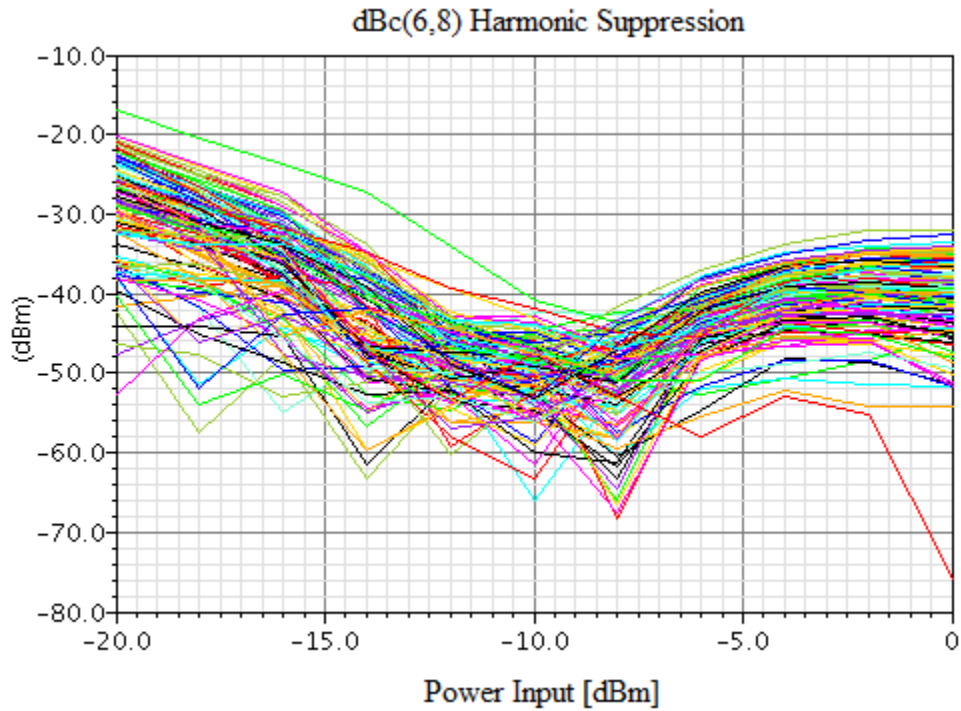


Fig 7.5: Suppression of the 6th spurious harmonic.

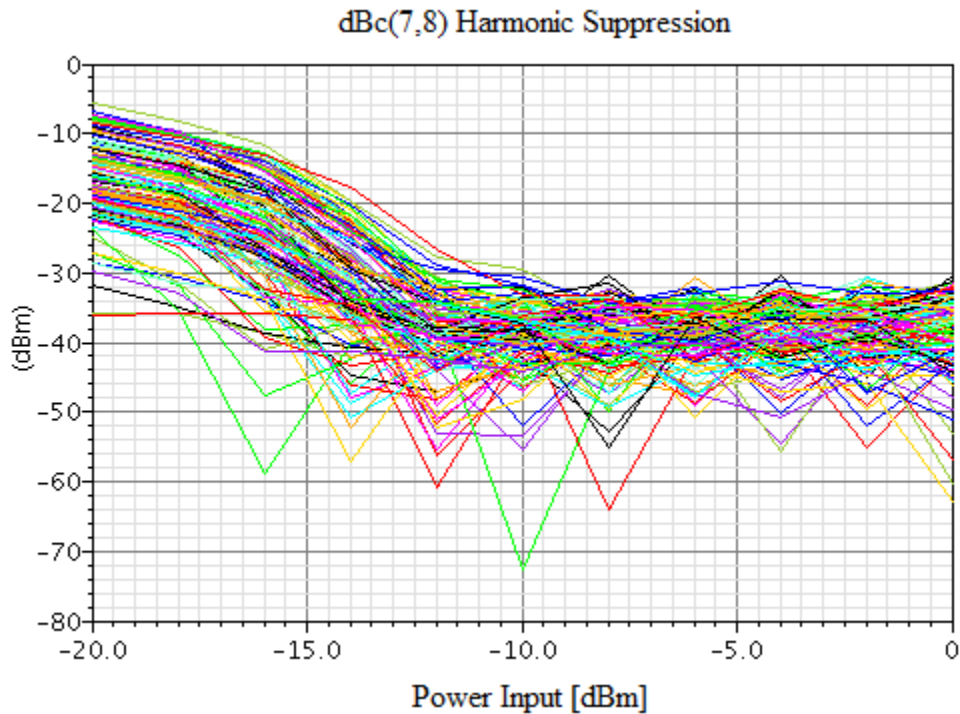


Fig 7.6: Suppression of the 7th spurious harmonic.

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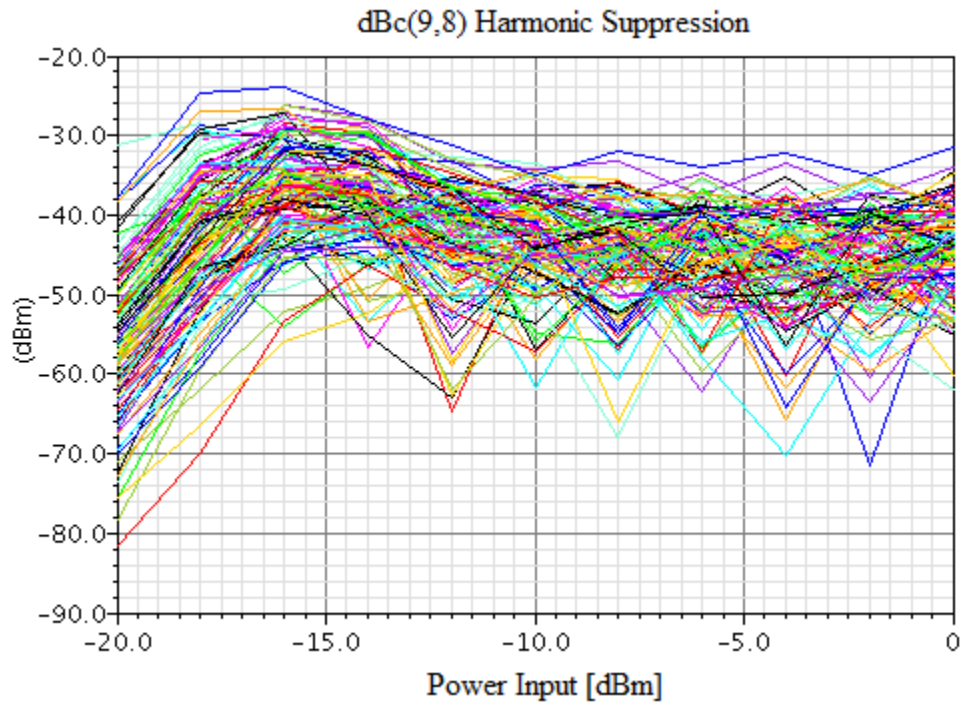


Fig 7.7: Suppression of the 9th spurious harmonic.

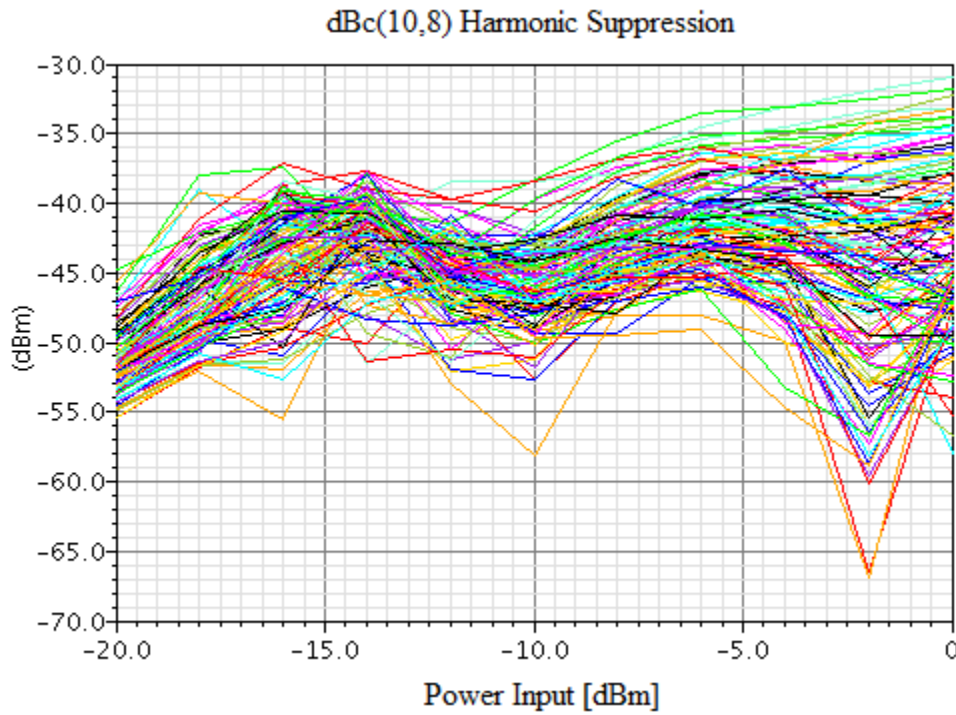


Fig 7.8: Suppression of the 10th spurious harmonic.

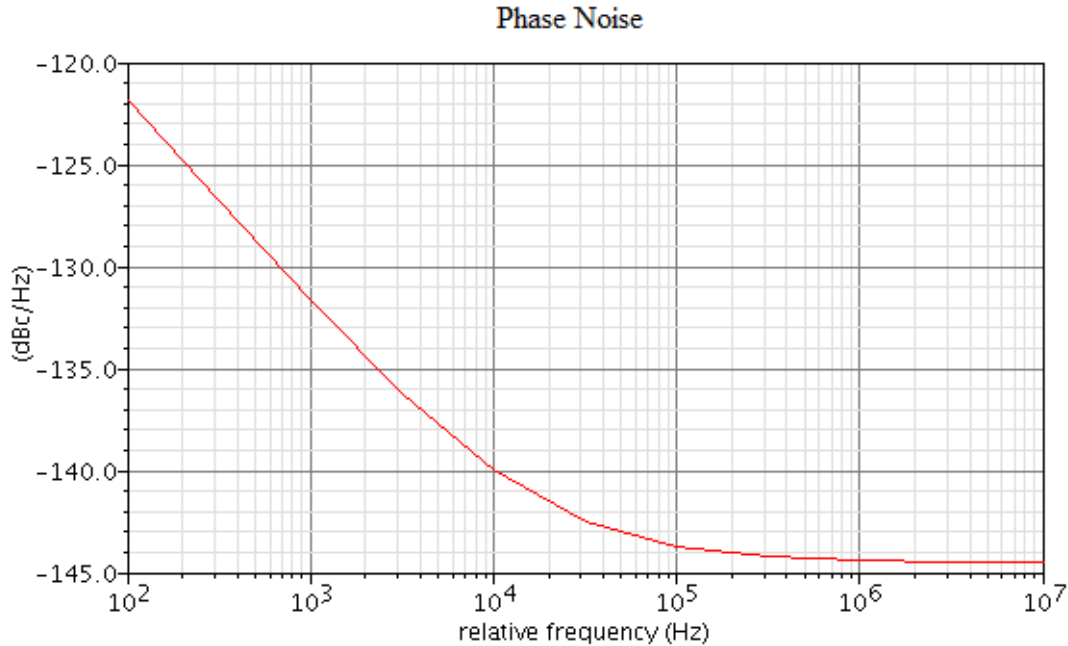


Fig. 7.9: Output phase noise floor at the 8th harmonic using a noise-free input signal.

The input S_{11} and output S_{22} reflection parameters are lower than -10 dB over a frequency range concurring with target specifications.

Within 10% variation of voltage supply, the 8th harmonic output power change by ~ 1.3 dBm.

The $K_f - B_1 f$ test shows that the octupler is unconditional stable versus 512 montecarlo iterations in all the four topologies showed in paragraph 8.2.

Finally, the top level layout of the octupler *capacitive* version is shown in figure 7.10. The chip size is $928 \times 1228 \mu\text{m}$.

Looking at chip layout, on the lower side the 20 GHz frequency doubler is connected to the input pads IN/INX by long transmission lines without any input matching network. Going up, the 40 and 80 GHz are layouted and on the top, as label "BUF" depicts, connected to the output pads OUT/OUTX the output buffer and power detector are implemented.

Same considerations are valid for the octupler *inductive* version chip.

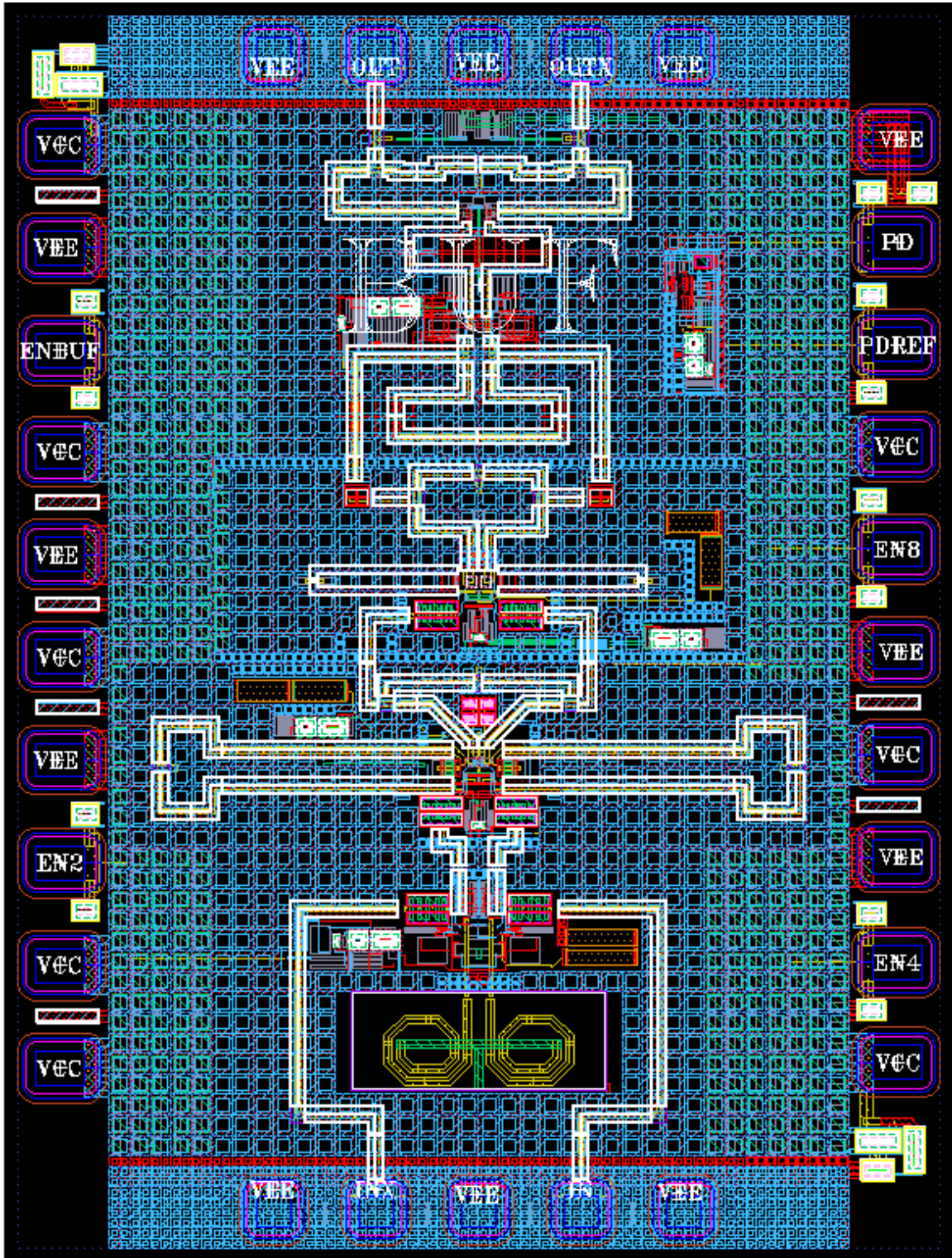


Fig. 7.10: Octupler *capacitive* version chip.

7.3 80 GHz Frequency Octupler *Inductive* Version Results

Here the results of the 80 GHz frequency octupler *inductive* version are shown. All the results are post layout simulations. Montecarlo simulations take in account both process and mismatch variations. The power output of the 8th harmonic is within the range of -6,+0.5 dBm for an input power of -10 dBm and between -2.3,+2 for input power of 0 dBm.

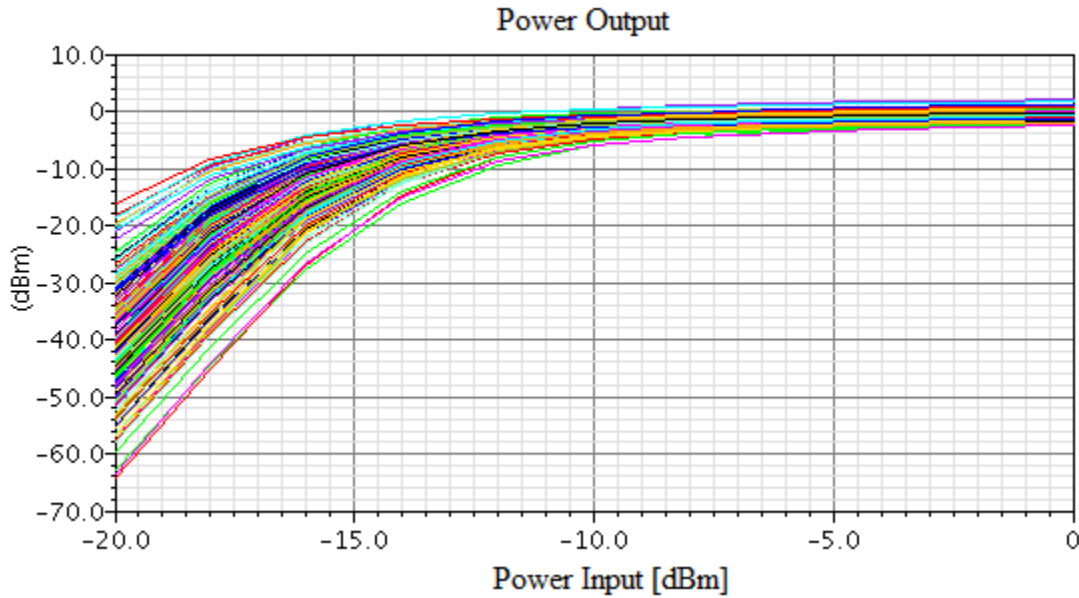


Fig. 7.11: 80 GHz output power versus input power over 128 montecarlo iterations.

The 3dB bandwidth is of 16.6 GHz, narrower than the *Cap* version and centered at 76.4 GHz.

From fig. 7.13, unlike from *Cap* version, the outputs are more balanced since the average is centered at 0 dB.

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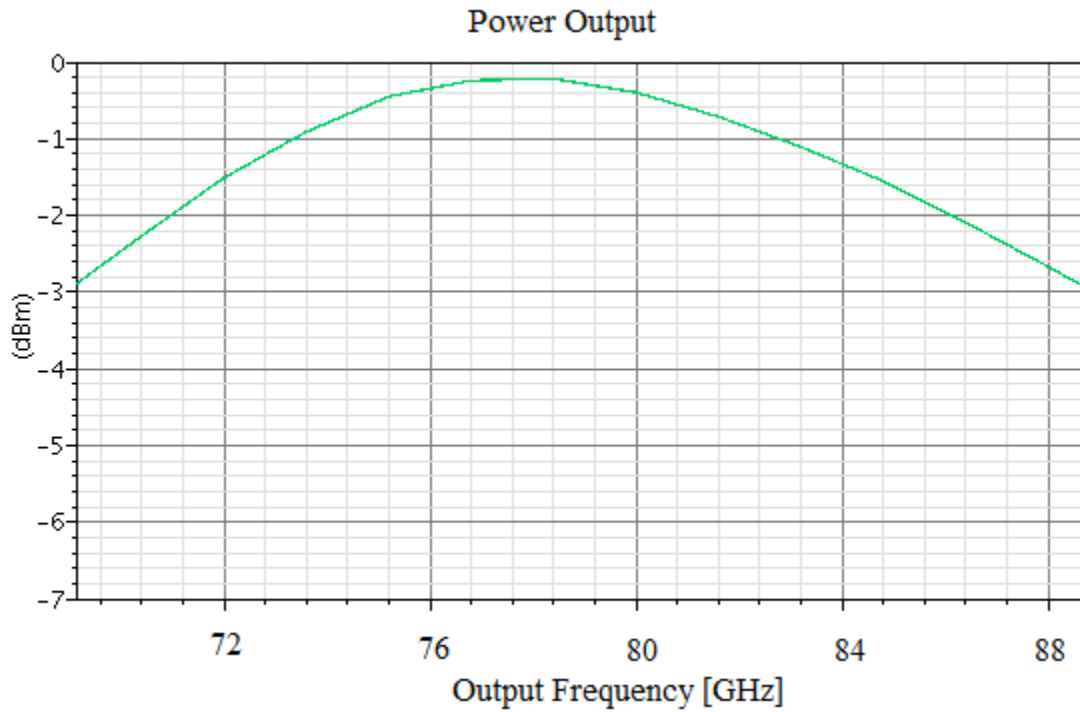


Fig 7.12: 3dB bandwidth of the 8th output harmonic.

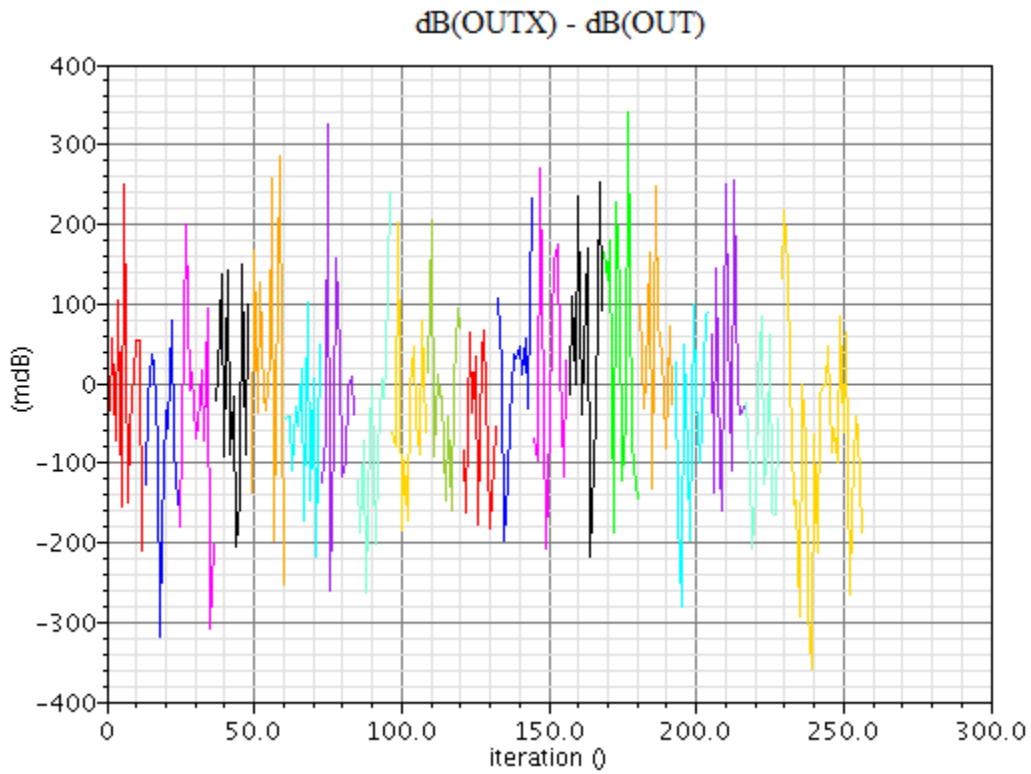


Fig 7.13: Outputs difference versus monte carlo iterations for 0 dBm input power.

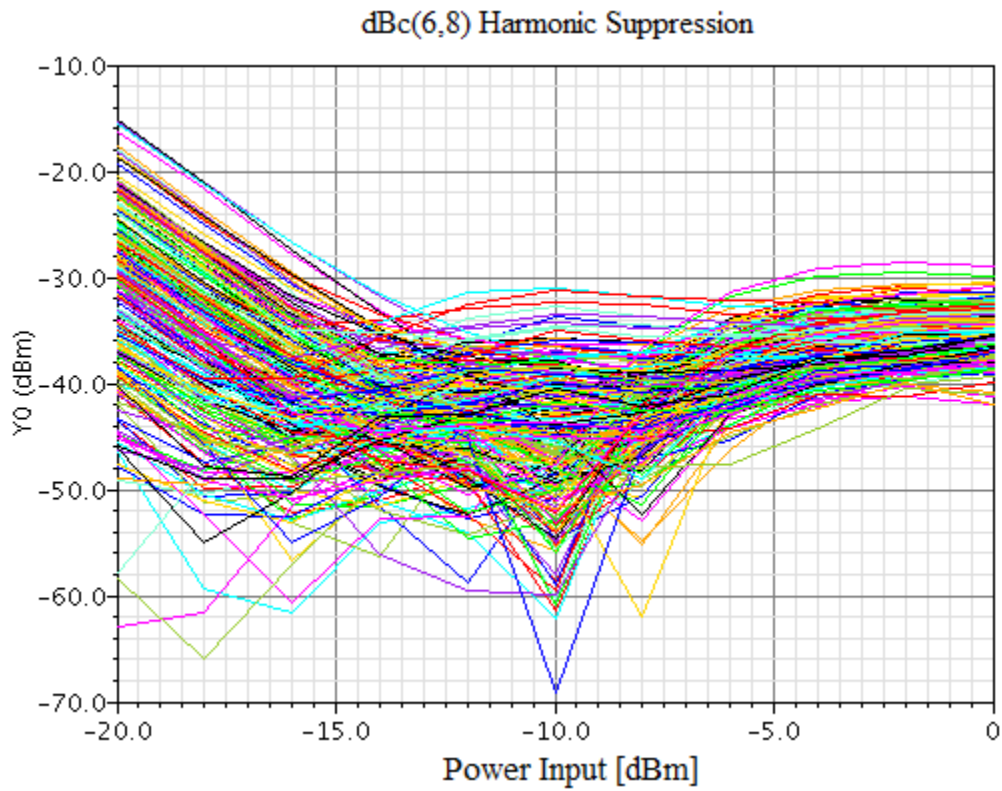


Fig 7.14: Suppression of the 6th spurious harmonic.

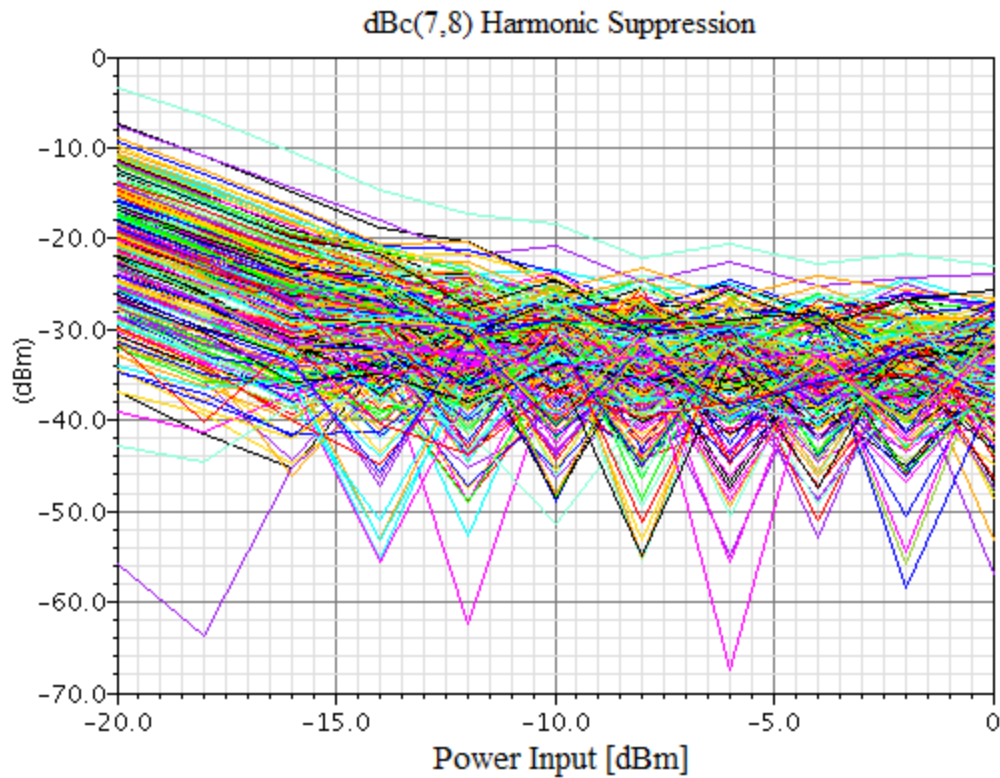


Fig 7.15: Suppression of the 7th spurious harmonic

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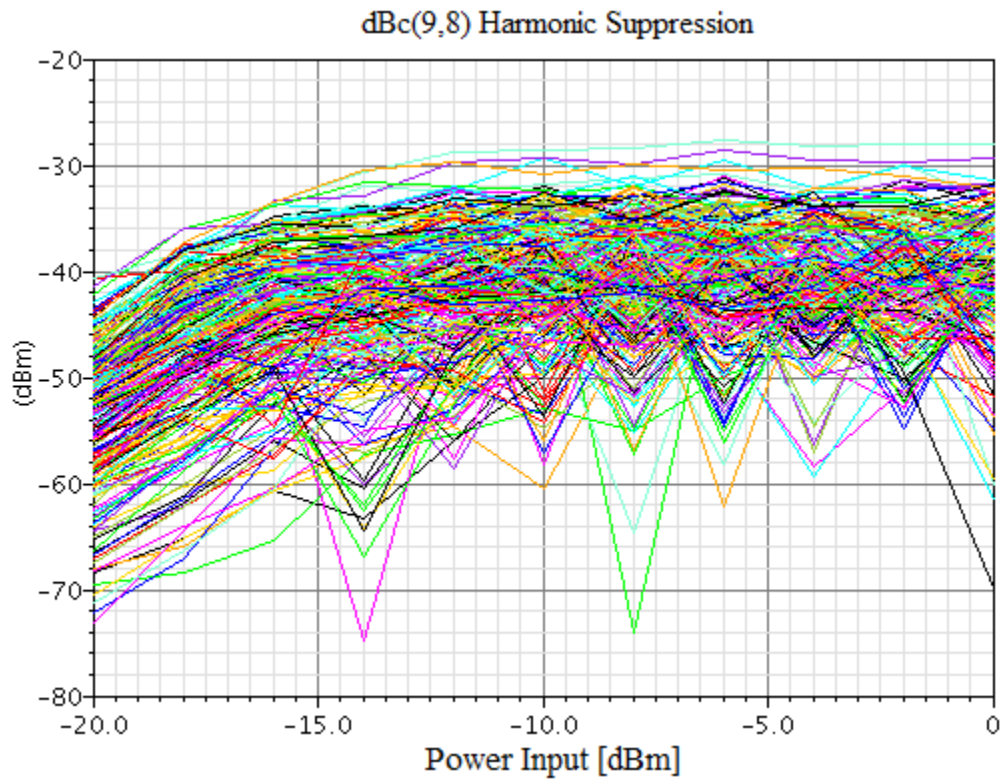


Fig 7.16: Suppression of the 9th spurious harmonic

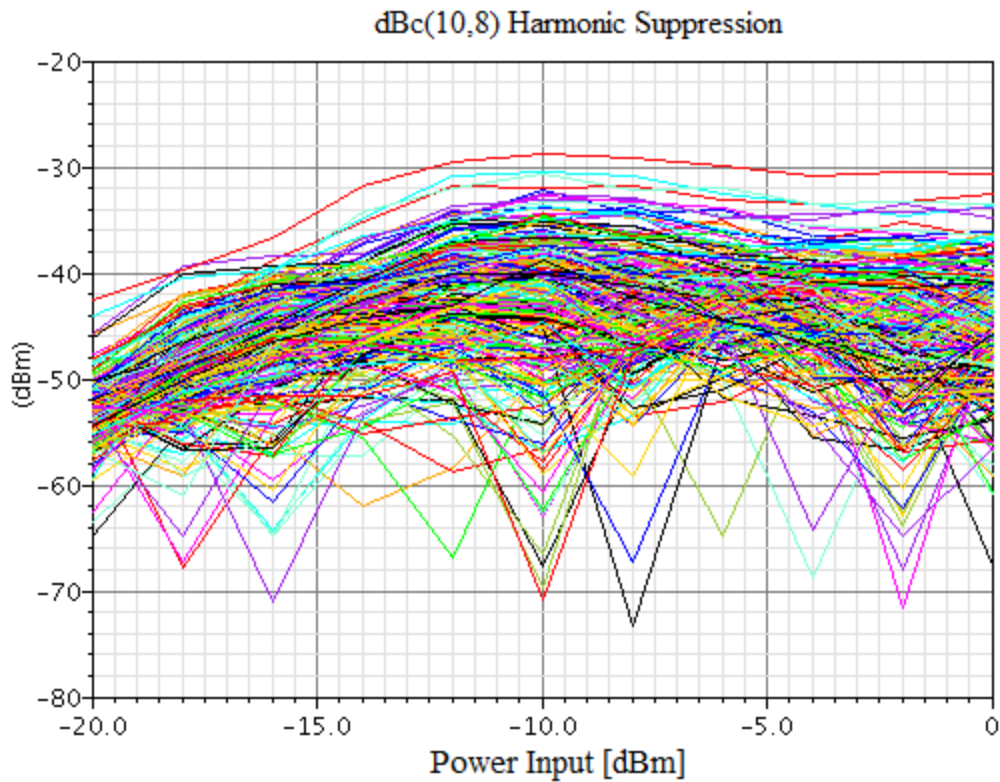


Fig 7.17: Suppression of the 10th spurious harmonic.

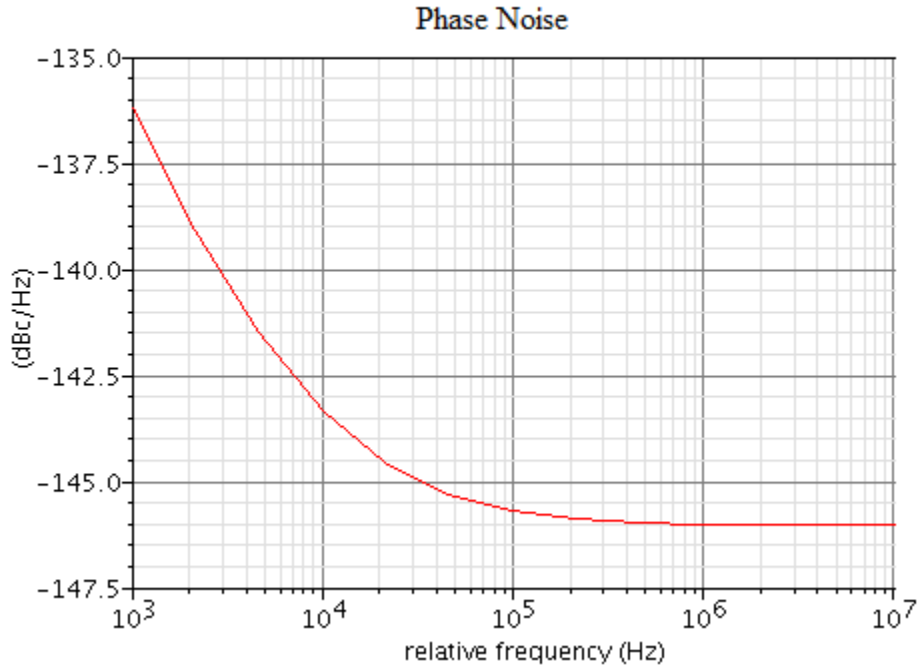


Fig. 7.18: Output phase noise floor at the 8th harmonic using a noise-free input signal.

The input S_{11} reflection parameter is lower than -10 dB over a frequency range concurring with target specifications. For the S_{22} parameter the condition is respected almost all over the frequency range since the priority was given first to solve the stability issue and afterwards to the output reflection parameter.

Within 10% variation of voltage supply, the 8th harmonic output power change by 1 dBm.

The $K_f - B_1 f$ test shows that the octupler is unconditional stable versus 512 montecarlo iterations in all the four topologies showed in paragraph 8.2.

Finally, the top level layout of the octupler *inductive* version is shown in figure 7.19. The chip size is $728 \times 1228 \mu\text{m}$.

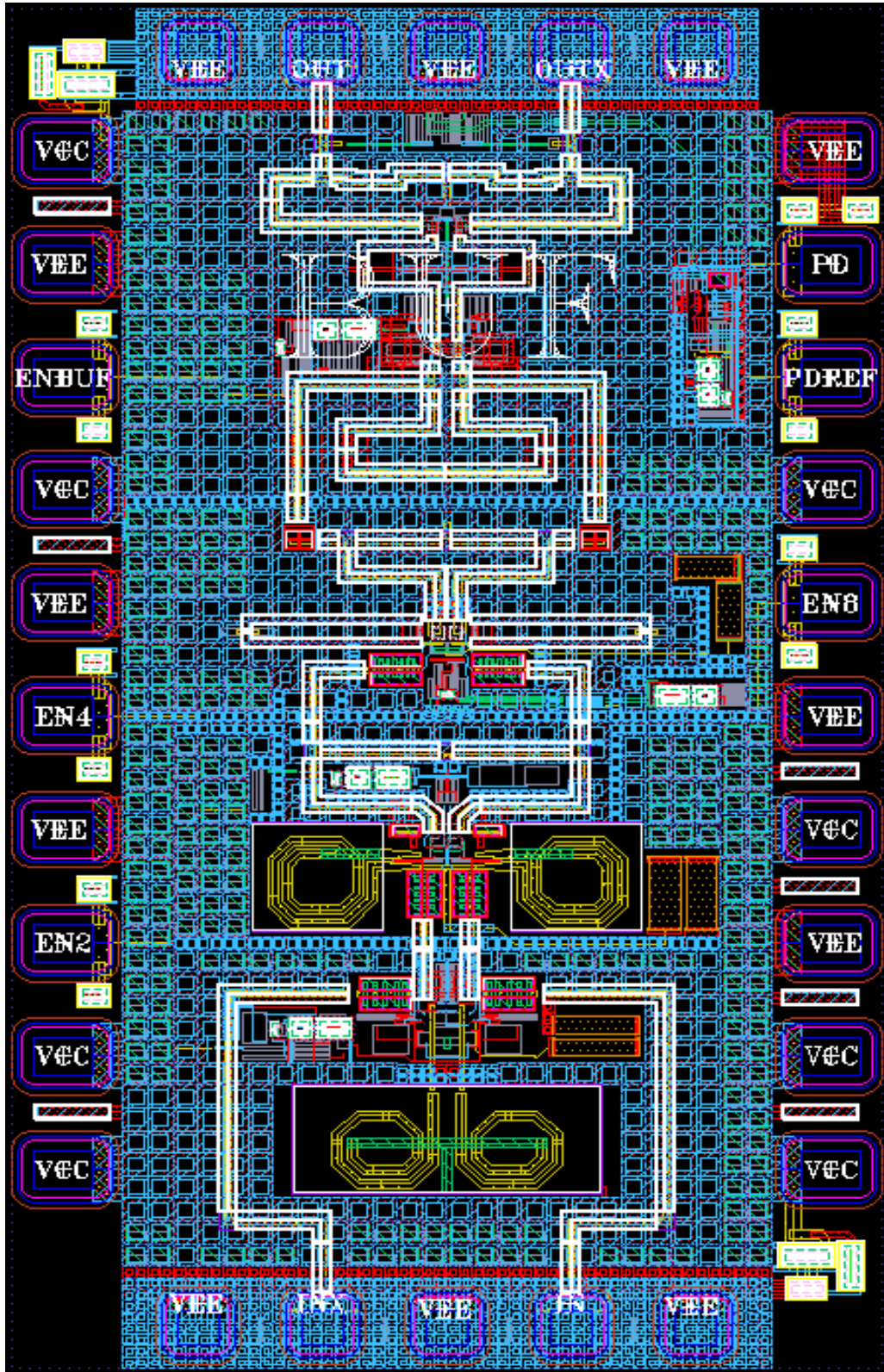


Fig. 7.19: Octupler *inductive* version.

8 Conclusion and Outlook

8.1 Bias Network

The 40 and 80 GHz frequency doublers implement a bias network as here below shows. It is responsible for the biasing of RF stage, whereas for the LO one two simple resistors connected to the voltage source are used. The 20 GHz frequency doubler implements a bias circuit based on the same topology of the other doublers, but with one more transistor stacked since one stage of emitter follower has been used.

The bias circuit is based on a simple current mirror with emitter degeneration. The input signal *enable* (EN) permit to switch on/off the bias network and therefore the functionality of the doubler. The current source is provided from resistor R_8 together with transistor T1 (fig.8.1), the mirror stage is made by T3, T4 with the emitter resistors R_5 , R_7 and the final mirror is composed of T2, R_3 . With EN connects to VCC, T1 works is region of saturation drawing a current $I_{c,T1}$ given by (8.1):

$$I_{c,T1} = \frac{V_{cc} - V_{be,T3} - V_{ce,sat,T1}}{R_5 + R_8} \quad (8.1)$$

Where $V_{be,T3} \approx 0.8 V$ and $V_{ce,sat,T1} \approx 0.25 V$.

That current is mirrored in transistor T4 through the ratio primarily gave from R_5, R_7 . Indeed the purposes of the emitter degeneration are twofold: boost the current mirror output resistance and move the input/output current ratio from the transistors emitter areas to the resistors ratio improving greatly the matching between the input and output current. R_5, R_7 are TaN resistors with 10% of tolerance. The current in the other branch, $I_{c,T4}$, is given by:

$$I_{c,T4} = \frac{1}{R_7} \left(I_{c,T1} * R_5 + V_T \ln \left(\frac{I_{c,T1} I_{s,T4}}{I_{c,T4} I_{s,T3}} \right) \right) \quad (8.2)$$

In this circuit the resistors ratio is $\frac{R_5}{R_7} = 2$ while the areas emitter ratio slightly differs from 2. As previously said, the current mirror ratio is primarily given by the resistors ratio.

Increase the output resistance has as result to decrease the component of systematic gain error that stems from finite output resistance.

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T2 together with R_3 mirror the current in the RF stage transistor with ratio of 5. Use a resistor as current source in the RF stage (R_{TAIL}) helps to reduce the instability issues since it shows less parasitic capacitance compared to a current mirror, thus the capacitive load is quite small [Trotta:07,1]. The output terminal (OUT) is connected to the bias resistor at the RF stage.

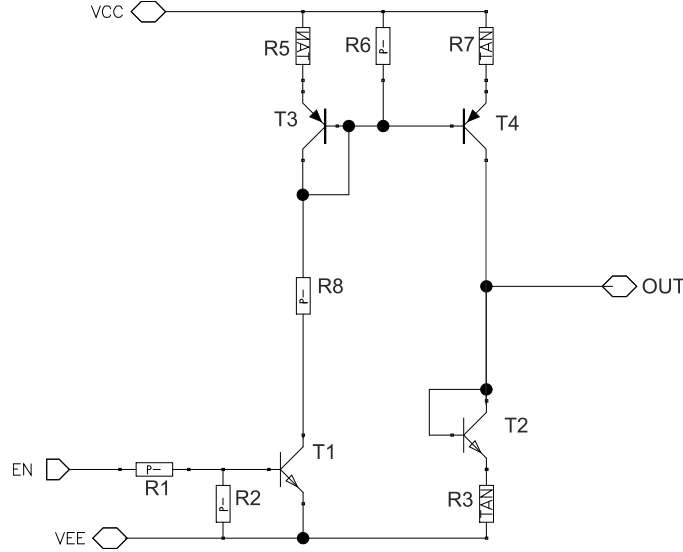


Fig. 8.1: Bias network.

8.2 Stability Test

During the design of non-linear RF circuits, stability topic is one of the major point of interest. Especially as frequency increase the frequency multiplier is not longer unidirectional hence a feedback can exist around the device. The presence of a feedback can be shown from S_{12} scattering parameter that differs from 0. In this feedback system, the loop gain can trigger oscillations if the Barkhausen criteria is respected, therefore if the effective loop gain equals unity and the loop phase shift equals 360° at the oscillations frequency.

To check the stability the $k - \Delta$ test has been used, where a device is unconditionally stable if Rollet's conditions (8.3), (8.4) are simultaneously satisfied.

$$Kf = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \quad (8.3)$$

$$B_1f = 1 + |s_{11}|^2 - |S_{22}|^2 - \Delta^2 > 0 \quad (8.4)$$

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If the device S parameters do not satisfy this test, it is not unconditional stable and stability circles can be used to determine if there are values of source/load impedance for which the device is conditionally stable.

The stability has been checked for each of five chips with different PORT configurations in order to verify all the critical topologies. Moreover the parasitic inductances due to the supply and ground paths have been included since they reduce further the device stability. In the next figures the four PORT configurations are shown. Each resistor and voltage generator represent a PORT device, while the device under test (D.U.T.) represent the single frequency doubler or the chain of three doublers.

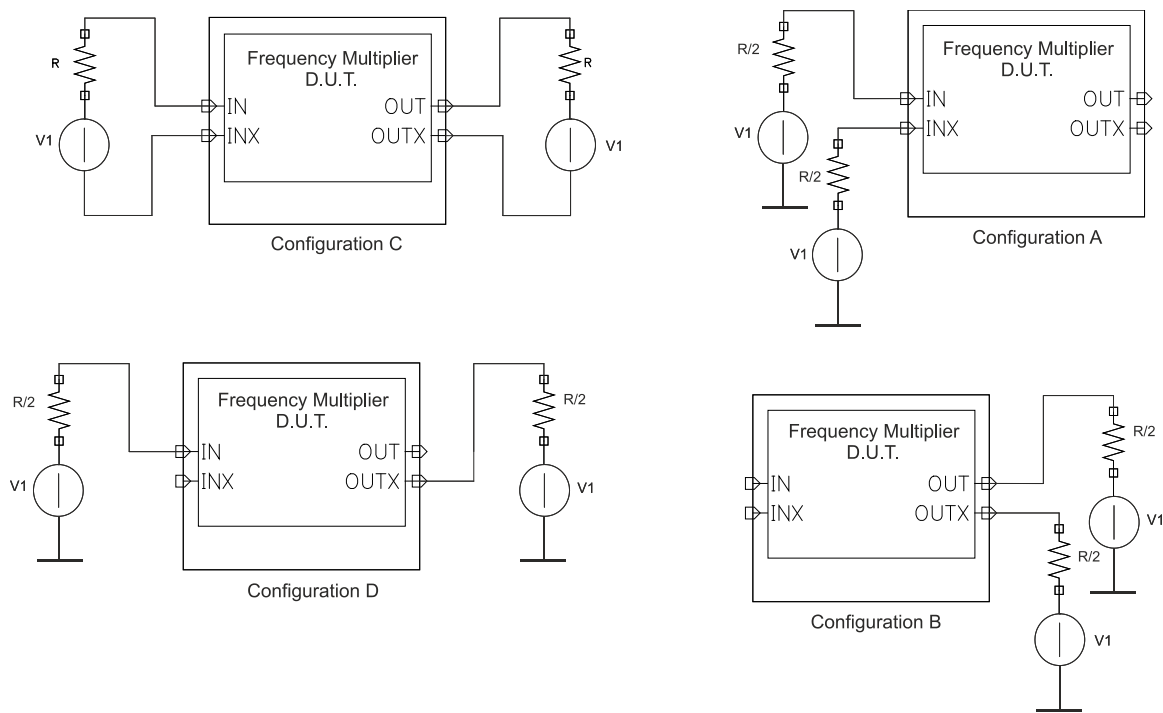


Fig. 8.2: Four PORT stability test.

The most problems topologies from stability point of view are the configurations "A", "B" and in consequence "D", since in these cases the input/output terminals are open and at one of the device ports (IN-INX, OUT-OUTX) the incoming wave is equals to the outgoing one so the corresponding S reflection parameter is close to unity.

8.3 Outlook To New Solution

Looking out to new and more efficient solutions, a new stacked frequency quadrupler/octupler can be designed following the idea presented in [Forstner:09] and implementing the phase shift networks here showed instead of transmission lines equals to $\frac{\lambda_g}{4}$. The circuit presented in [Forstner:09] indeed suffers from the fact that a transmission line equals to $\frac{\lambda_g}{4}$ at $\sim 20/40$ GHz is too long to be implemented and as results a shorter one has to be chosen providing a lower phase shift and degrading the performances.

With the phase shift network presented in this work, the phase quadrature is easy to achieve also at low frequency reducing at the same time the area occupancy compared to [Forstner:09].

The main idea is to stack two frequency doublers allowing to reduce (ideally halve) the DC power consumption and the amount of devices used since the output matching network of the first doubler and the RF stage of the second one are not longer necessary. Although this topology increase the efficiency, the output spurious rejection is lower; also the stability has to be studied in depth since the presence of the phase shift networks could be troublesome. Stack more than two doublers can result problems from the spurious rejection and stability point of view, therefore a new octupler can be composed of two doublers stacked and followed by a doubler and an output buffer. Using the topology presented in [Forstner:09] together with the phase shift networks presented in this work, new frequency multipliers can be discovered improving at the same time power and area efficiency.

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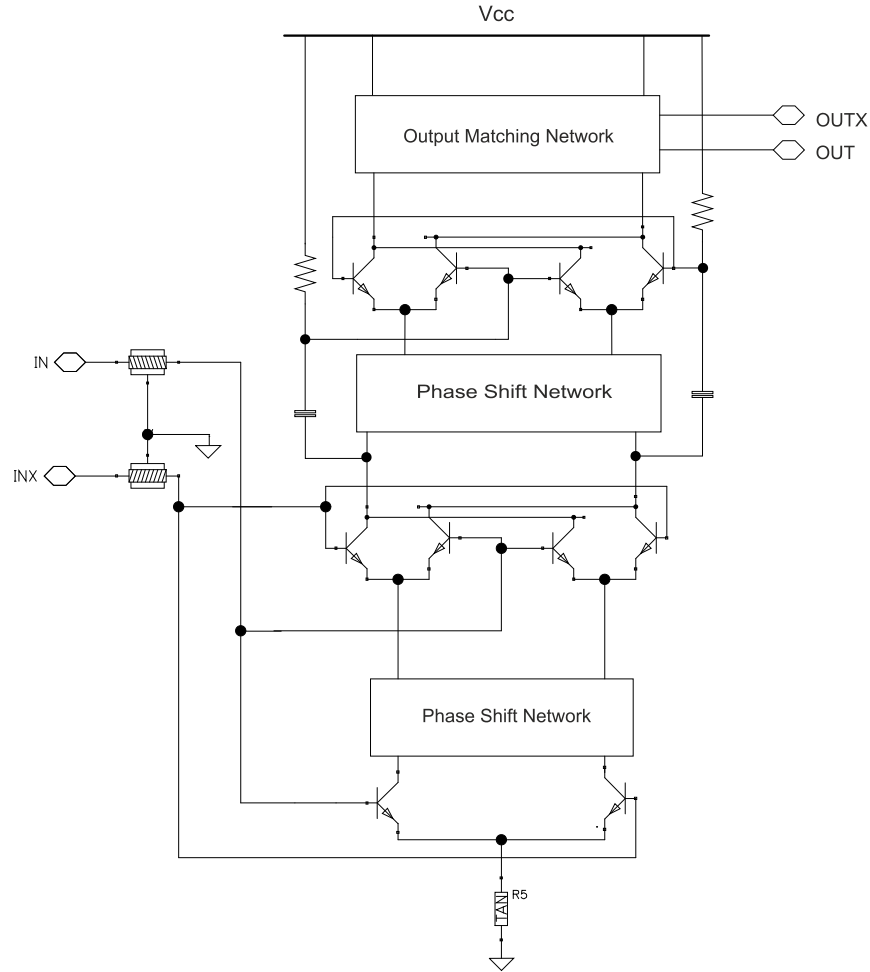


Fig. 8.3: Stacked frequency quadrupler.

8.4 Conclusion

In the presented work, monolithic millimeter-wave frequency multipliers in low-cost SiGe bipolar technology have been designed and layouted. Due to the operation frequencies, the on-chip wavelength is comparable with the chip size so the propagation effects must to be considered also in the integrated circuits and while this bring difficulties in the chip design at the same time allow to discover new solutions as has been demonstrated. The work presented showed as is possible achieve the phase quadrature also at frequencies such low that the transmission lines are too expensive to be used.

Five chips have been designed and layouted and then delivered to the foundry. Devices are expected to become available from mid of 2011.

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Multiplier	Power Output [dBm]	Spurious Suppression [dBc]	Bandwidth [GHz]	Chip Size [$\mu\text{m} \times \mu\text{m}$]
Octupler <i>Capacitive</i> Version	[0,+2.9] @ 0 dBm Input Power	$> 30 \text{ dBc}$	19	928 x 1228
Octupler <i>Inductive</i> Version	[-2.3,+2] @ 0 dBm Input Power	$\geq 30 \text{ dBc}$	16.6	728 x 1228

Table 8.1: Frequency octuplers technical data.

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