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MASTER'S DEGREE IN ELECTRONIC ENGINEERING

"Design of an ultra-low-power integrated amplifier for cardiac signal implantable sensors"

Advisor: Prof. Andrea Neviani

Candidate: Emanuela Dicarolo

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Abstract

Nowadays, health monitoring is a crucial area of research, given the increasing need to detect vital parameters in order to obtain accurate diagnoses in a short time, continuously collect informations about the health status of patients, and quickly intervene in critical circumstances. This thesis focuses on electrocardiogram (ECG) signals recording, being of the utmost importance for the diagnosis of cardiovascular diseases. Implantable devices are often used for this purpose, because they allow unobtrusive measurements, resulting in reliable signals with better rejection of interferences and artifacts. An ultra-low power amplifier intended for implantable sensors is presented. The overall system has a limited battery capacity, thus making power consumption a key aspect when it comes to design choices. Furthermore, ECG signals have a limited amplitude and are often affected by large DC offsets, thus emphasizing the need to design ac-coupled amplifiers that introduce minimal noise levels. This circuit topology employs stacked inverter-based operational transconductance amplifiers (OTAs), that add up each transconductance, but using the same current, thereby implementing the current-reuse technique, in order to improve noise and power efficiency, while providing high gain. The design was implemented in a 130-nm CMOS process. A stacked inverter-based operational transconductance amplifier (OTA) designed to process ECG signals is then presented. It achieves a differential mode gain A_{dm0} of $23.9\,dB$ in-band, a bandwidth BW of $10.53\,kHZ$, a common-mode rejection ratio $CMRR$ of $59\,dB$, a power supply rejection ratio $PSRR$ of $62\,dB$ and thermal noise of $116\,nV/Hz$.

Sommario

Al giorno d'oggi, il monitoraggio della salute è un'area di ricerca cruciale, data la crescente necessità di rilevare i parametri vitali per ottenere diagnosi accurate in tempi brevi, raccogliere continuamente informazioni sullo stato di salute dei pazienti e intervenire rapidamente in circostanze critiche. Questa tesi si colloca nell'ambito della registrazione di segnali ECG, essendo di estrema importanza per la diagnosi delle malattie cardiovascolari. I dispositivi impiantabili sono spesso utilizzati per questo scopo, in quanto consentono misurazioni poco invasive, ottenendo così segnali affidabili con una migliore reiezione di interferenze e artefatti. Viene presentato un amplificatore a bassissima potenza per sensori impiantabili. Il sistema nel suo complesso ha una batteria di capacità limitata, il che rende il consumo di potenza un aspetto fondamentale nelle scelte di progettazione. Inoltre, i segnali ECG hanno un'ampiezza limitata e sono spesso affetti da ampi offset in DC, evidenziando così la necessità di progettare amplificatori accoppiati in AC, che introducano livelli di rumore minimi. Questa topologia circuitale impiega amplificatori operazionali di transconduttanza (OTA) realizzati con inverter di tipo stacked, che sommano ciascuna transconduttanza, utilizzando la stessa corrente, implementando quindi la tecnica del riutilizzo di corrente, al fine di migliorare l'efficienza di rumore e di potenza, fornendo al contempo un elevato guadagno. Il progetto è stato implementato in un processo CMOS a 130 nm. Si presenta quindi un amplificatore operazionale di transconduttanza basato su inverter di tipo stacked, pensato per processare segnali ECG. Esso presenta un guadagno di modo differenziale A_{dm0} pari a $23.9\,dB$ in banda, una larghezza di banda BW di

$10.53\,kHz$, un rapporto di reiezione di modo comune $CMRR$ di $59\,dB$, un rapporto di reiezione della tensione di alimentazione $PSRR$ di $62\,dB$ e rumore termico pari a $116\,nV/Hz$.

Ringraziamenti

Vorrei esprimere la mia sincera graditudine al Professor Andrea Neviani, che mi ha pazientemente seguito durante il percorso di tirocinio e tesi.
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List of Acronyms

AF Atrial Fibrillation

AFE Analogue Front-End

CMRR Common Mode Rejection Ratio

CVDs Cardiovascular diseases

DIBL Drain Induced Barrier Lowering

ECG Electrocardiogram

EMG Electromyography

ICU Intensive Care Unit

ILRs Implantable Loop Recorders

LPF Local Field Potential

NEF Noise Effinciency Factor

OTAs Operational Transconductance Amplifiers

PEF Power Efficiency Factor

PSRR Power Supply Rejection Ratio

1 Introduction

The first chapter of this thesis aims to outline the background to this work and the deep reasons for approaching this field. The project's topics of interest will first be introduced in order to clarify to the reader the context of the work and the motivations that drive further studies in this area. A brief presentation of how the work is organized and the distribution of the subsequent sections will then be provided.

1.1 Motivation

According to the World Health Organization (WHO) cardiovascular diseases (CVDs) are the leading cause of death globally[1]. An estimated 17.9 million people died from CVD in 2019, which is 32% of all deaths worldwide. Furthermore, among these deaths, 85% were caused by heart attack and stroke.

It is evident both the importance of developing early and accurate diagnoses in order to prevent the onset of serious problems, and the need to continuously monitor critical pathological conditions.
The above circumstances require non-traditional monitoring of the electrical activity of the heart. In fact, recording the ECG signal in a traditional way or using devices such as the cardiac Holter is often not enough. It is therefore necessary to use a device that allows for more extensive monitoring of cardiac activity over time, in this way it is possi-

[1] https://www.who.int/news-room/fact-sheets/detail/cardiovascular-diseases-(cvds).

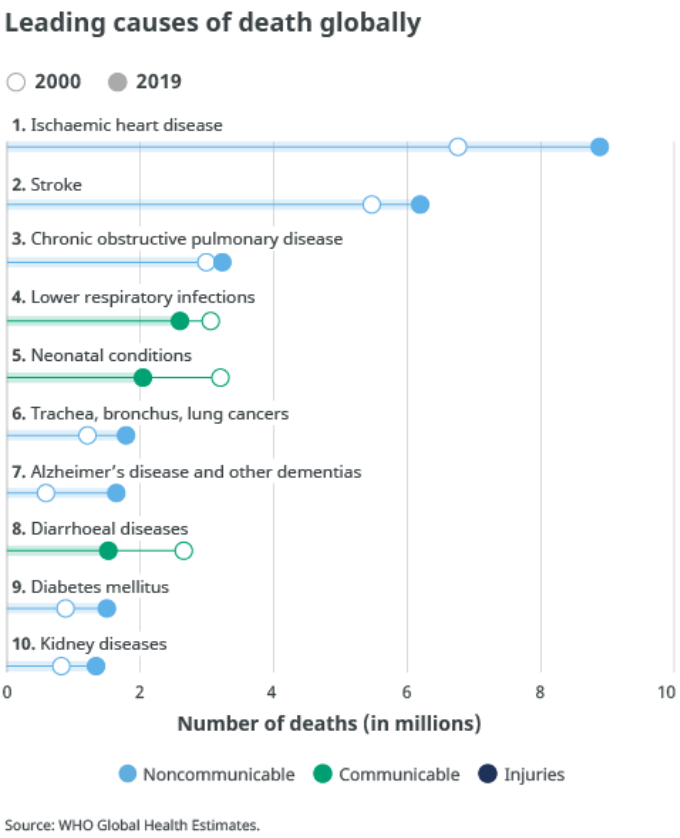


Figure 1: Chart of the leading causes of death globally in 2019.

ble to detect extremely infrequent arrhythmias and intervene promptly if an anomaly is detected.

For this purpose, implantable ECG recorders are used. Implantable ECG recorders are solid-state devices, which are characterized by being minimally invasive, and are used to monitor the patient's ECG without the need for cardiac leads [3].

Introduced for the first time in 1995, they are particularly suitable for patients suffering from infrequent and often unexpected heart rhythm abnormalities, which are suspected to be linked to a cardiac system malfunction [3]. These phenomena include syncope, lightheadedness, or palpitations.

Also known as implantable loop recorders (ILRs), these devices are capable of detecting syncope, dizziness, palpitations and other relevant

issues. Besides the former applications, ILRs are also employed to monitor atrial fibrillation (AF), the most common cardiac arrhythmia. The latter becomes evident with a change in heart rate, which often becomes irregular and particularly fast.

AF could be also subclinical, which means that it is detected in asymptomatic patients, who have not received any previous diagnosis by ECG [4]. Experimental evidence has suggested that subclinical AF is strongly associated with cryptogenic stroke. That said, knowing that rediagnosing AF following a stroke carries a higher risk of the stroke occurring again, it follows that detecting subclinical AF after cryptogenic stroke is vital to tailoring therapy and ensuring good health of the patient. [4]. This necessary premise highlights the growing importance of devices for accurate diagnoses and timely interventions in case of need.

In recent years, research on this topic is pushing for a transition toward implantable devices, because of the many reasons why these ones are often preferable to traditional biopotential recording techniques. In addition to the reasons set out above, implantable devices are more suitable for monitoring those biological signals that can only be obtained in vivo, since they exhibit an improved environmental artifact tolerance and an unobtrusive nature [1].

Last point is the key reason why traditional pacemaker or holter devices are not the best solution when it comes to monitoring hearth activity. Pacemakers feature various limitations and a primary drawback: the whole device must be implanted in the body, along with the battery and long lead [5]. Pacemakers exhibit a massive battery suitable for long-term operation, but due to the large amount of space required, various

side effects and wireinduced issues were experimented by many patients. Thus, new technologies should be investigated in order to reduce the battery size and the distance between the device and the sensing/stimulation site. In particular referring to an electrocardiogram (ECG) recording, implantable devices own many interesting features, such as a stronger signal, a better rejection of interference and immunity to motion artifacts and baseline wander due to a more robust electrode-tissue contact [1].

The thesis work, presented here, focuses on the design and simulation of an amplification stage for an implantable device that records the ECG subcutaneously. The circuit architecture, designed in a 130-nm CMOS process and simulated in *Cadence Virtuoso*, is a three-stack inverter-based operational transconductance amplfier (OTA).

1.2 Thesis Outline

The following thesis work is divided into six sections.

In this *first section* an introduction to the subject has been provided, in order to make clear to the reader the context in which this thesis is placed, highlighting the need to continue doing research in this sector to contribute to the design of increasingly accurate devices for the diagnosis and treatment of cardiovascular diseases.

The *second section* illustrates in a general way an already existing monitoring system for the ECG [1], and to which this thesis is inspired.

The *third section* describes some basic concepts, necessary to deal with the study of the device, which will then be recalled in the following sections.

The *fourth section* talks about the design of the main blocks: the amplifier, the bias circuit and the pseudo-resistors.

The *fifth section* summarizes the results obtained, highlighting the salient aspects.

The *sixth, and final, section* briefly reviews the work carried out, drawing conclusions and offering some suggestions for possible future improvements of the implemented system.

2 Review of Existing ECG Monitoring Systems

This thesis work is inspired by the circuit in [1].

The latter is an example of some of the most efficient ILRs in the literature.

They presented a two-stage amplifier that exploits the chopping technique and is extremely competitive in terms of energy efficiency. Being, in fact, a device intended to be implanted for subcutaneous ECG recording, it cannot ignore stringent specifications on power consumption and noise levels.

They propose to implement the technique of current-reuse by stacking OTAs. This technique is currently used for general ECG signal processing, but could also be used for more specific applications, such as local field potential (LPF) recording or peak detection.

The work that they carried out, of which a general schematic is reported in Fig. 2, involved the implementation of two different configurations for the first amplification stage: one with three stacks and one with five. In the second case, they obtained a *noise efficiency factor* NEF of 0.86, a *power efficiency factor* PEF of 0.99 with a current consumption of only $13.9\,nA$.

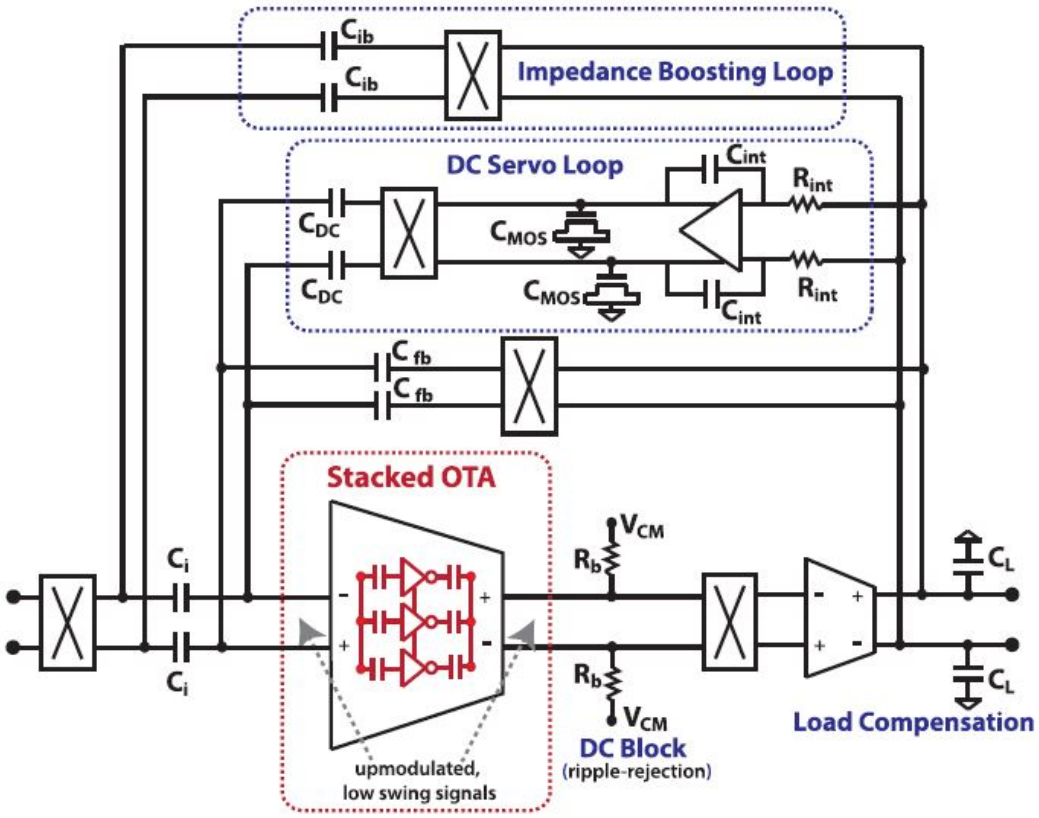


Figure 2: Architecture of the chopper-stabilized ECG amplifier in [1].

3 Preliminary Concepts

This section will review some theoretical concepts in order to help in the understanding of this thesis project.

3.1 Sub-threshold MOS Operating Region

Sub-threshold operating region, also known as *weak inversion*, is a working region characterized by a MOS transistor gate-source voltage lower than the threshold voltage V_t, but still high enough to create a depletion region at the surface of the silicon. In the weak inversion region, the channel charge is much less than the charge in the depletion region, and the drain current arising from the drift of majority carriers is negligible. By the way, the total drain current in weak inversion region is not only determined by drift, since there is a diffusion current determined by a gradient in minority-carrier concentration [2]. The drain current for an n-channel MOS operating in sub-threshold is the following [6]:

$$i_{DS} = I_{DS0} \cdot exp\left(\frac{v_{GS}}{nV_{th}}\right) \cdot \left[1 - exp\left(-\frac{v_{DS}}{V_{th}}\right)\right] \tag{3.1.1}$$

where

$$I_{DS0} = 2n\mu C'_{OX}\left(\frac{W}{L}\right)V_{th}^2 \cdot exp\left(-\frac{V_T}{nV_{th}}\right) \tag{3.1.2}$$

where v_{GS} is the gate-to-source voltage, v_{DS} is the drain-to-source voltage, $V_{th} = k_B T/q$ is the thermal voltage (k_B is the Boltzmann constant, T the absolute temperature, and q the elementary charge), n is the so-

called sub-threshold slope and may be computed as $n = (qI_D/k_BTg_m)$ [7], C'_{OX} is the gate oxide capacitance per unit area, μ is the mobility of majority carriers, (W/L) is the transistor aspect ratio, and V_T is its threshold voltage. Furthermore, the threshold voltage V_T depends inherently on V_{DS} due to the drain induced barrier lowering (DIBL), and on V_{BS}, the body-to-source voltage, due to the body effect [8]. This relationship can be expressed as [8]:

$$V_T = V_{T0} - \lambda_{DS}V_{DS} - \lambda_{BS}V_{BS} \tag{3.1.3}$$

where V_{T0} is the so-called zero-bias threshold voltage (i.e. the value extrapolated when $V_{DS} = V_{BS} = 0V$), while λ_{DS} and λ_{BS} are technology-dependent parameters, which estimate the amount of threshold voltage change related to V_{T0} for a determined value of V_{DS} or V_{BS}.

In weak inversion a MOSFET behaves in a similar way to a bipolar transistor, as suggested by the exponential dependence of the drain current i_{DS} on the gate-to-source voltage v_{GS}.

A sub-threshold biased MOS transistor can be modeled as a V_{GS}-controlled current source if the v_{DS} term in the drain current i_{DS} expression can be neglected, in other words this means that the dc drain-to-source voltage V_{DS} satisfies the following condition [9]:

$$V_{DS} \geq 4V_{th} \approx 100\,mV \tag{3.1.4}$$

thus, the saturation condition for a MOS trainsistor biased in sub-threshold is verified starting from approximately $V_{DS} = 100\ mV$, as

observed in Fig. 3.

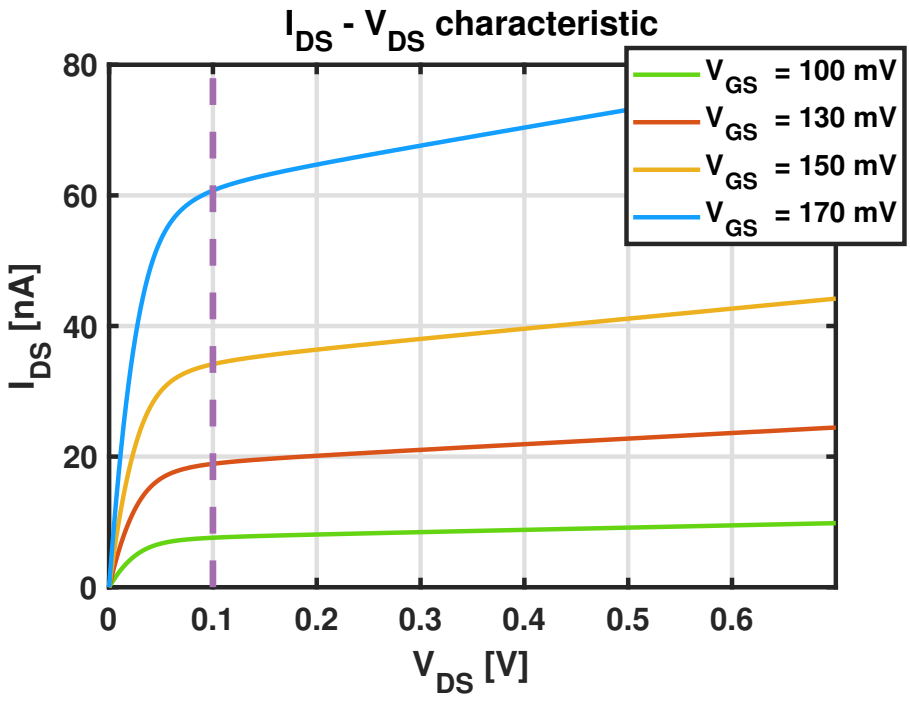


Figure 3: Output characteristic of a sub-threshold biased MOSFET.

3.2 Small Signal Analysis in Sub-threshold Operating Region

In order to derive the ac small-signal model for a MOS in weak inversion, some parameters are extracted.

The transconductance g_m of a MOS transistor operating in weak inversion is evaluated as follows:

$$g_m = \left.\frac{\partial i_{DS}}{\partial v_{GS}}\right|_Q \tag{3.2.1}$$

where Q is the operating point in which the MOS transistor is biased:

$$Q = \{v_{GS} = V_{GS}, v_{DS} = V_{DS}, v_{BS} = V_{BS}\}. \tag{3.2.2}$$

Thus, the following expression for the transconductance g_m is obtained:

$$g_m = \frac{1}{nV_{th}} \cdot I_{DS0} \cdot exp\left(\frac{V_{GS}}{nV_{th}}\right) \cdot \left[1 - exp\left(-\frac{V_{DS}}{V_{th}}\right)\right] \tag{3.2.3}$$

which corresponds to:

$$g_m = \frac{I_{DS}}{nV_{th}} \tag{3.2.4}$$

as can be observed from equation (3.2.4), the transconductance g_m of a MOS transistor operating in weak inversion is a purely function of I_{DS}. Instead, the output resistance r_o is calculated as follows:

$$r_o = \left(\frac{\partial i_{DS}}{\partial v_{DS}}\bigg|_Q\right)^{-1} \tag{3.2.5}$$

carryng out some computations, the following result is obtained:

$$r_o = \frac{V_{th}}{I_{DS}} \cdot \frac{1}{\frac{\lambda_{DS}}{n} + \frac{1}{\left[exp\left(-\frac{V_{DS}}{V_{th}}\right)-1\right]}}. \tag{3.2.6}$$

Then, for high values of V_{DS} the equation (3.2.6) can be rewritten in the subsequent form:

$$r_o \simeq \frac{nV_{th}}{\lambda_{DS} I_{DS}} \simeq \frac{1}{\lambda_{DS} g_m}. \tag{3.2.7}$$

In a similar manner, it is possible to compute the substrate transconductance g_{mb} of a MOS transistor operating in weak inversion.

$$g_{mb} = \left.\frac{\partial i_{DS}}{\partial v_{BS}}\right|_{Q} \tag{3.2.8}$$

Thus, the following expression for the substrate transconductance g_{mb} is obtained:

$$g_{mb} = \frac{\lambda_{BS} I_{DS}}{n V_{th}} = \lambda_{BS} g_m. \tag{3.2.9}$$

Finally, the intrinsic MOSFET DC gain A_{v0} is computed:

$$A_{v0} = g_m \cdot r_o \simeq \frac{1}{\lambda_{DS}}. \tag{3.2.10}$$

Once all the needed parameters are derived, it is possible to represent the small signal equivalent circuit of a sub-threshold biased MOS transistor. The aforementioned schematic is shown in Fig. 4.

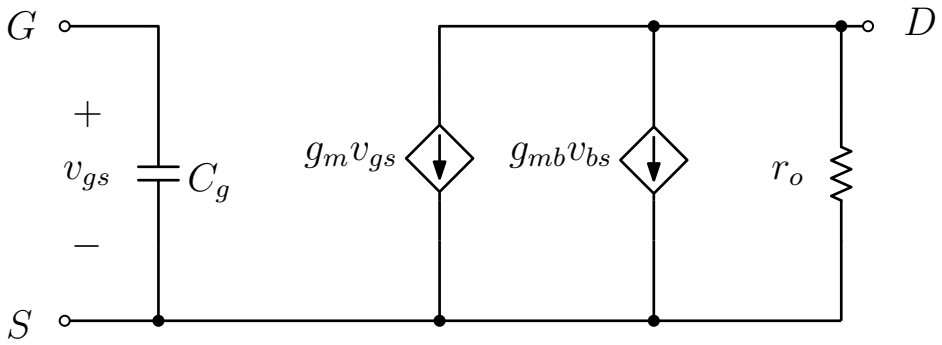


Figure 4: Small signal equivalent circuit of a sub-threshold biased MOSFET.

The capacitance C_g in the circuit in Fig. 4 is the input capacitance seen from the gate terminal. It is worth noting, that in weak inversion the gate-to-source and drain-to-source capacitances are almost zero $C_{gs} \simeq C_{gd} \simeq 0$, since the inversion layer contains little charge [2]. Thus, the gate-to-bulk capacitance can be regarded as the combination of the oxide capacitance C_{OX} in series with the depletion capacitance C_{js}. Thus, the following expression is obtained [2]:

$$C_{gs} + C_{gb} + C_{gd} \simeq C_{gb} = WL \cdot \left(\frac{C_{OX} C_{js}}{C_{OX} + C_{js}} \right). \tag{3.2.11}$$

In order to summarize the computed small-signal parameters, they are reported in Table 1.

Small-signal parameters	**Expression**
Transconductance	$g_m = \frac{I_{DS}}{nV_{th}}$
Output resistance	$r_o \simeq \frac{1}{\lambda_{DS} g_m}$
Substrate transconductance	$g_{mb} = \lambda_{BS} g_m$
Intrinsic DC gain	$A_{v0} \simeq \frac{1}{\lambda_{DS}}$

Table 1: Small-signal sub-threshold parameters.

3.3 MOS Pseudo-Resistors

Nowadays the miniaturization of circuits makes it extremely complex to design and integrate high-value resistors in standard CMOS technology. Indeed the minimum doping level of silicon and poly-silicon structures enables the realization of typical values of sheet resistance in a range from few $\Omega/\square$ to few $k\Omega/\square$ [6]. Such high values would result in long

resistors, making it difficult to create a compact layout. Beyond the area consumption and considerable cost, integrating long resistors allows the formation of large distributed parasitic capacitances with their associated noise issues. The resistors presented in this thesis, given their high resistance value, were designed through alternative solutions to avoid the significant disadvantages associated with the fabrication of traditional resistors. Such circuit architectures are made by means of MOS transistors and exhibit a high equivalent resistance, while covering considerably less area than that occupied by a conventional resistor of the same value. These types of "devices" are called **pseudo-resistors** because electronically they behave like resistors.

The reduced area occupation, while being a remarkable result, is not the only aspect that motivates the search for similar circuit solutions. In fact, pseudo-resistors have noise levels well below those of a physical resistor of equal value. Therefore, they are suitable for applications that require low noise, such as weak signal processing, including biological signals. Pseudo-resistors have architectures that differ in their performance in terms of response linearity, symmetrical dynamic range, frequency behavior, and simplicity of implementation.

In the following, two different symmetric architectures are briefly described: the series configuration and the parallel configuration. The former sets the current by meaning of the least conductive element; while the latter, has a current that is the sum of each element in the structure [6].

3.3.1 Series Architectures

The series architecture presented here uses two PMOS transistors and two dc voltage generators V_{Gen}, connected between source and gate, that are needed to implement a tunable pseudo-resistor. Generators must be matched in order to mantain the symmetry of the device and ensure its linear behavior. Despite the drawback of requiring two matched generators instead of one, there are advantages associated with this design choice: among the types of pseudo-resistors in series configuration, this one may be easier to implement, since the two voltage generators V_{Gen} are referred to the outer pins. In addition, their parasitic capacitances do not load the internal nodes of the pseudo-resistor, thus yielding a broader frequency response [6].

Let V_{AB} be defined as the dc voltage across the terminals of the pseudo-resistor in Fig. 5. When V_{AB} is approximately equal to $0\,V$, the MOS transistors operate in sub-threshold region.

Consequently, the equivalent resistance of a single PMOS transistor may be computed using the equation for the drain current in sub-threshold operating region, where $V_{SG} = V_{Gen}$.

$$i_{SD} = I_{SD0} \cdot exp\left(\frac{V_{Gen}}{nV_{th}}\right) \cdot \left[1 - exp\left(-\frac{v_{SD}}{V_{th}}\right)\right] \tag{3.3.1}$$

where

$$I_{SD0} = 2n\mu C'_{OX}\left(\frac{W}{L}\right)V_{th}^2 \cdot exp\left(-\frac{|V_T|}{nV_{th}}\right). \tag{3.3.2}$$

Then, the equivalent small-signal resistance $r_{eq,S}$ of a pseudo-resistor in

series configuration may becomputed as the sum of the small-signal resistances of the two PMOS transistors:

$$r_{eq,S}|_{V_{AB}=0} = 2 \cdot \left(\left. \frac{\partial i_{SD}}{\partial v_{SD}} \right|_{V_{SD}=0} \right)^{-1} \tag{3.3.3}$$

thus, getting the following expression:

$$r_{eq,S}|_{V_{AB}=0} = 2 \cdot \frac{V_{th}}{I_{SD0}} \cdot exp\left(-\frac{V_{Gen}}{nV_{th}}\right) \tag{3.3.4}$$

where the assumption of two identical transistors with the same small-signal resistance was made.

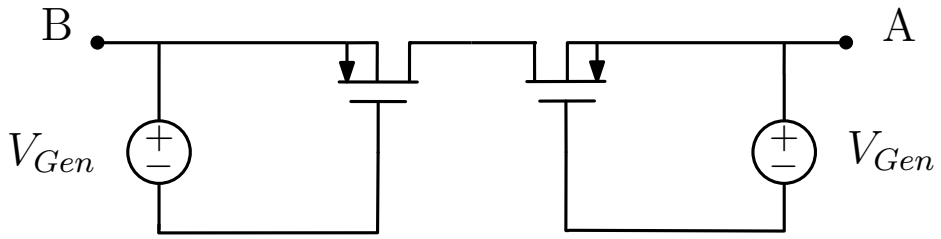


Figure 5: Schematic of a symmetric series pseudo-resistor.

Being V_{AB} the dc voltage across the pseudo-resistor and I_{AB} its dc current, it is possible to get a qualitative idea of the sub-linear behavior of the pseudo-resistor from the $I_{AB} - V_{AB}$ characteristic, which is shown in Fig. 6. Indeed, when large V_{AB} signals are applied, the cumulative effect of bias (dc) and signal (ac) may result in some significant distortions [6]. In the device shown in the Fig. 5 the current is always constrained by the saturation of one of the two transistors, which makes the overall structure symmetrical and sub-linear.

When $V_{AB} = 0\,V$, the device exhibits a small-signal resistance $r_{eq,S}$ and

a linear behavior.

Conversely when a constant bias voltage V_{dc} different from $0\,V$ is applied, the operating point varies and the device enters the non-symmetrical sub-linear region. In this case, a sinusoidal voltage signal superimposed to the bias voltage V_{dc} results in different current amplitudes on each half-wave, leading to an average current I_{AB} which is different from I_{dc}, in particular lower than that flowing without the signal. Accordingly, the dc accuracy of the pseudo-resistor is affected by the presence of ac signals.

Nevertheless, this behavior can be advantageous if the application demands a device that automatically limits its own dc current, as both the on-bias and on-signal behaviors tend to reduce the dc current compared to a fully linear element [6].

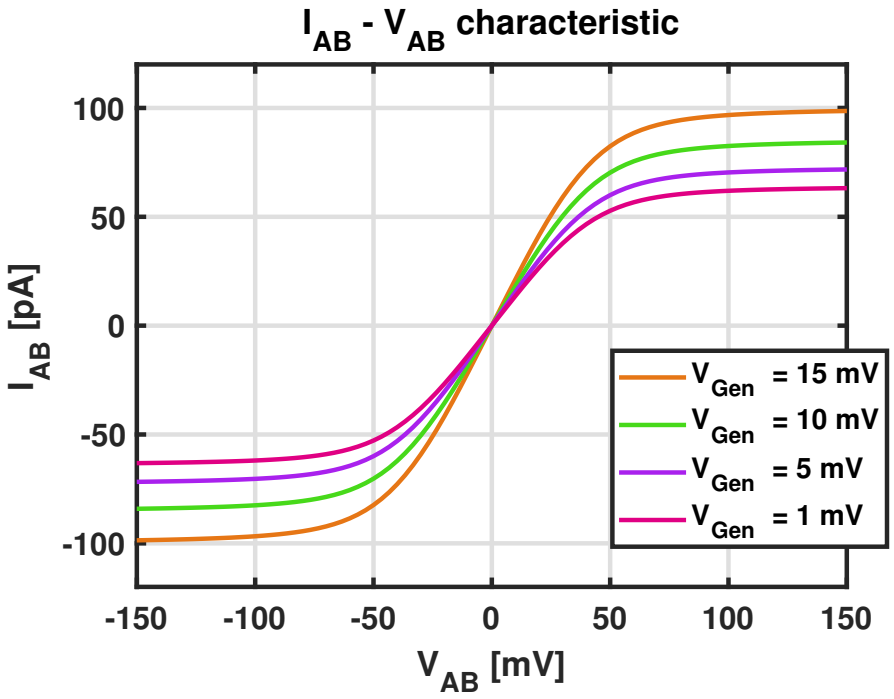


Figure 6: Characteristic curves of a sub-linear pseudo-resistor in series configuration, referred to devices having $(W/L) = (1\,\mu m/1\,\mu m)$ and $|V_T| \simeq 254\,mV$.

3.3.2 Parallel Architectures

The parallel architecture, presented in Fig. 7, employs two PMOS transistors and two dc voltage generators V_{Gen}, connected between drain and gate, that are needed to implement a tunable pseudo-resistor.
The small-signal equivalent resistance $r_{eq,P}$ of a parallel pseudo-resistor, estimated around $V_{AB} = 0\,V$ is defined as the parallel of the small-signal resistances of the two PMOS transistors. Thus, $r_{eq,P}$ may be computed as:

$$r_{eq,P}|_{V_{AB}=0} = \frac{1}{2} \cdot \left(\frac{\partial i_{SD}}{\partial v_{SD}}\bigg|_{V_{SD}=0} \right)^{-1} \tag{3.3.5}$$

hence, getting the following expression:

$$r_{eq,P}|_{V_{AB}=0} = \frac{1}{2} \cdot \frac{V_{th}}{I_{SD0}} \cdot exp\left(-\frac{V_{Gen}}{nV_{th}}\right) \tag{3.3.6}$$

where the assumption of two identical transistors with the same small-signal resistance was made.

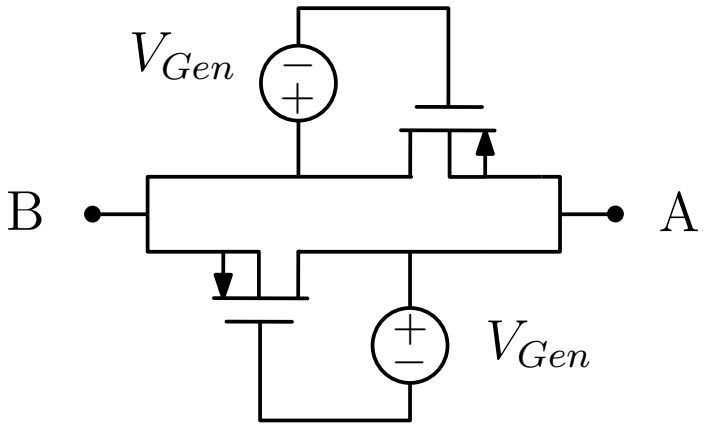


Figure 7: Schematic of a symmetric parallel pseudo-resistor.

When a constant bias voltage V_{dc} different from $0\,V$ is applied, the operating point varies. If the voltage applied is not sufficient to turn on the well diodes, the overall structure exhibts a super-linear quadratic behavior, resulting from the turn-on of MOS transistors. The aforementioned behavior can be seen in Fig. 8. In this case, a sinusoidal voltage signal superimposed to the bias voltage V_{dc} results in different current amplitudes on each half-wave, leading to an average current I_{AB} which is different from I_{dc}, in particular lower than that flowing without the signal. Accordingly, the dc accuracy of the pseudo-resistor is affected by the presence of ac signals.

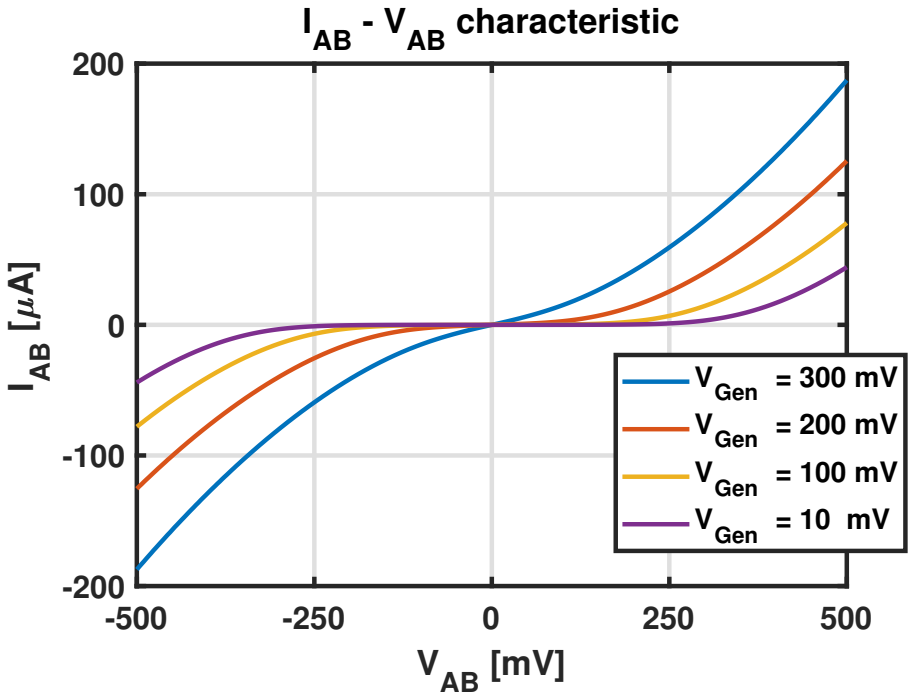


Figure 8: Characteristic curves of a super-linear pseudo-resistor in parallel configuration, referred to devices having $(W/L) = (5\,\mu m/0.29\,\mu m)$ and $|V_T| \simeq 251\,mV$.

3.4 Noise in Analogue Integrated Circuits

Noise is a major concern for the performances of electronic circuits. Its description in the time domain is not easy to treat, so it is often modeled as a random process, characterized by a set of realizations. The random process is assumed to be ergodic and stationary in the strict sense. Noise is often characterized through power spectral density, also called PSD.

3.4.1 Types of noise

This paragraph briefly discusses the types of noise most relevant to electronic circuits.

- *Resistor thermal noise*, whose power spectral density (PSD) may be written as:

$$\left.\frac{\overline{v_n^2}}{\Delta f}\right|_{\Delta f=1} = \overline{v_n^2} = 4k_BTR \quad \left[\frac{V^2}{Hz}\right] \tag{3.4.1}$$

$$\left.\frac{\overline{i_n^2}}{\Delta f}\right|_{\Delta f=1} = \overline{i_n^2} = \frac{4k_BT}{R} \quad \left[\frac{A^2}{Hz}\right] \tag{3.4.2}$$

  where $k_B \simeq 1.38 \cdot 10^{-23} J/K$ is the Boltzmann constant and T is the absolute temperature.

  The thermal noise associated with a resistor can be modeled with a voltage noise generator put in series with the resistor, or with a current noise generator put in parallel with the resistor, as shown in Fig. 9.

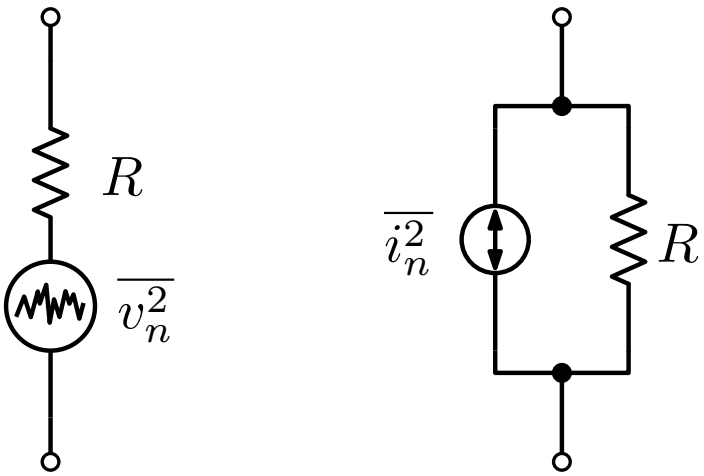


Figure 9: Equivalent resistor thermal noise model.

- *MOS transistor thermal noise*, which can be modeled as a randomly varying current caused by the thermal agitation of carriers in the channel:

$$\left.\frac{\overline{i_{th}^2}}{\Delta f}\right|_{\Delta f=1} = \overline{i_{th}^2} = 4k_BT\frac{\gamma}{\alpha}g_m \quad \left[\frac{A^2}{Hz}\right] \tag{3.4.3}$$

  where γ and α are technology dependent parameters.

- *MOS transistor flicker noise*, which is due to the random mechanisms of carrier release and capture caused by traps at the interface between channel and oxide:

$$\left.\frac{\overline{i_{1/f}^2}}{\Delta f}\right|_{\Delta f=1} = \overline{i_{1/f}^2} = \frac{K_f}{f}\frac{g_m^2}{WLC_{OX}^2} \quad \left[\frac{A^2}{Hz}\right] \tag{3.4.4}$$

  where K_f is a process dependent parameter.

  The noise related to a MOS can be modeled with an equivalent current generator placed in parallel with the transistor, as shown

in Fig. 10, where the current $\overline{i^2_{noise}}$ is the sum of the contribution due to the thermal noise $\overline{i^2_{th}}$ and the contribution due to the flicker noise $\overline{i^2_{1/f}}$.

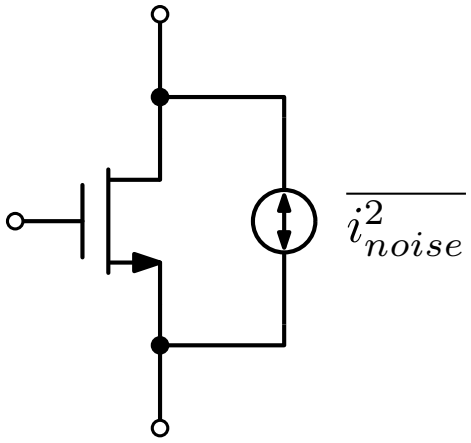


Figure 10: Equivalent MOS transistor noise model.

The above expressions related to noise in MOS transistors are based on the assumption that the device is saturated in *strong inversion*.

3.4.2 Noise in Sub-Threshold MOS

The previous expressions may be rewritten for a saturated MOSFET in *weak inversion*.

- *MOS transistor thermal noise*:

$$\left.\frac{\overline{i^2_{th}}}{\Delta f}\right|_{\Delta f=1} = \overline{i^2_{th}} = 2k_B T n g_m \quad \left[\frac{A^2}{Hz}\right]. \tag{3.4.5}$$

- *MOS transistor flicker noise*:

$$\left.\frac{\overline{i^2_{1/f}}}{\Delta f}\right|_{\Delta f=1} = \overline{i^2_{1/f}} = \frac{K_f}{f}\frac{g_m^2}{WLC_{OX}^2} \quad \left[\frac{A^2}{Hz}\right]. \tag{3.4.6}$$

3.5 Current-Reuse Technique

Amplification of biological signals requires low noise levels, but noise suppression often implies high power consumption. However, an amplifier designed to be inserted into a wearable or implantable sensor must necessarily meet stringent requirements about power consumption, which must be kept at a low level. This ensures that several specifications are met: the limited size of the battery, the robustness of the device with respect to heat dissipation, and a reasonable lifetime without battery replacement [7].

Thus, circuit solutions that achieve a good compromise between power and noise are pursued.

The main goal is to minimize the product of power and noise for the target amplifier. Therefore, keeping the noise constant, the amplifier's power may be decreased; otherwise, keeping the power constant, the amplifier's noise may be minimized. Assuming the latter solution is pursued, one way to implement it could be to increase the transconductance g_m of the amplifier, nevertheless keeping the bias current I_D unchanged [7]. In fact the power consumption P may be written as follows:

$$P = V_{DD} \cdot I_{tot} \tag{3.5.1}$$

where V_{DD} identifies the power supply voltage and I_{tot} identifies the amplifier's total current. While so as to characterize the noise performance of an amplifier, it might be useful to compute the *noise efficiecy factor*, also known as NEF:

$$NEF = v_{ni,rms} \cdot \sqrt{\frac{2}{\pi} \cdot \frac{I_{tot}}{4k_B T \cdot V_{th} \cdot BW}} \tag{3.5.2}$$

where $v_{ni,rms}$ is the input-referred *rms* noise voltage of the amplifier in a given bandwidth BW, $V_{th} = k_B T/q$ is the thermal voltage (k_B is the Boltzmann constant, T the absolute temperature, and q the elementary charge), BW is the amplifier's bandwidth (the same in wich the noise is computed) and I_{tot} is the amplifier's total current. The NEF is a unitless value, wich basically expresses the noise of a certain amplifier normalized with respect to the shot noise generated by a bipolar transistor biased using the equivalent total current as the amplifier [10]. Furthermore, it is useful to estimate an additional figure of merit, the *power efficiency factor* PEF, which allows a fair comparison of performance in terms of power consumption and noise levels between amplifiers having different supply voltages V_{DD}:

$$PEF = NEF^2 \cdot V_{DD}\,. \tag{3.5.3}$$

Thus, rewriting the expression in (3.5.3) for a single MOS transistor, whose only contribution to the noise is the thermal one, it follows:

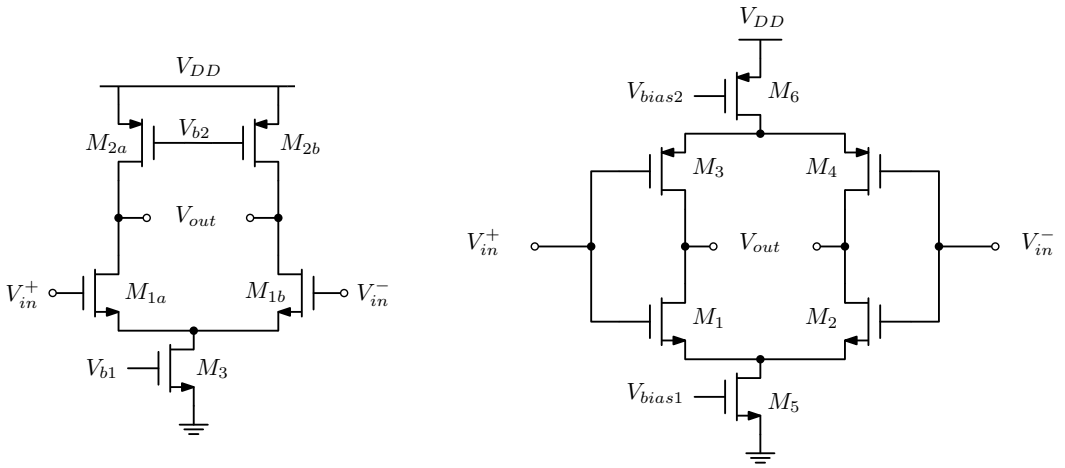
$$PEF \simeq \frac{\gamma n}{\pi V_{th}} \cdot \frac{I_D}{g_m} \cdot V_{DD} \tag{3.5.4}$$

where I_D is the dc drain current of the MOS transistor. It is then strainghtforward that keeping the drain current I_D and the power supply voltage V_{DD} unchanged, while boosting the transcoductante g_m, the

PEF decreases, thus the NEF decreases, meaning a more noise and power efficient circuit. Usually, in order to maximize the transconductance efficiency g_m/I_D, that is, to maximize the transconductance g_m while keeping the transistor drain current I_D constant, the choice of biasing the transistors in **weak inversion** is adopted. To further improve the transconductance g_m, a PMOS input pair can be stacked on top of an NMOS input pair, thereby designing an **inverter-based input stage**. In the assumption for which both pairs exhibit the same transconductance g_m, the transconductance g_m of the overall amplifier has been doubled, while keeping the bias current unchanged, since it is shared between the NMOS and PMOS pair. This implemented the **current-reuse** technique.

3.6 Inverter-Based Fully Differential Operational Transconductance Amplifier (OTA)

Current-reuse circuits are at the forefront of efficiency [10].
However, there are some disadvantages associated with implementing current-reuse in circuits that use inverters, such as in the topology shown in figure. A major drawback is the reduced swing of the output signal with respect to a classical fully differential common-source amplifier; in any case this can be mitigated by cascading a second amplifier stage. In addition, other disadvantages include: higher system requirements for the supply voltage, greater input capacitance and decreased common mode input range [7]. However, when it comes to ensuring extremely low power consumption and noise levels, the incurrence of these challenges is a price worth paying.



(a) (b)

Figure 11: (a) Fully differential common source amplifier. (b) Inverter-based amplifier.

The circuit in Fig. 11(b), exhibits a 2× transconductance g_m improvement, thus resulting from the stacking of a PMOS differential input pair (*consisting of transistors* $M_3 - M_4$) on top of an NMOS differential input pair (*consisting of transistors* $M_1 - M_2$).

In order to make the dc operating point of each inverter symmetrical, the stage should be self-biased using resistive feedback between the input and output terminals, as shown in Fig. 12. These feedback resistors from the dc point of view behave like short circuits, which makes the gate-to-source voltage equal to the drain-to-source voltage $V_{GS} = V_{DS}$ in each MOS transistor of the inverter.

This property, which is necessary to make the operating point stable with respect to changes in the supply voltage and bias current, is guaranteed if the resistors are of extremely high value, so it is chosen to implement them through pseudo-resistors. The voltage V_{bias1} is the *reference voltage* V_{ref} of a constant-G_m biasing circuit, which is employed to produce the bias current.

Moreover, the voltage V_{bias2} is the output common-mode voltage of the circuit. For low-supply voltage operation, it is critical that the output common-mode voltage is fixed to maximize signal swing, avoid undesirable distortion, and reduce the complexity of the common-mode feedback (CMFB) circuit to a minimum [11]. In fact, the common-mode output voltage is sensed through a resistive feedback path, consisting of two resistors R_{cm}.

Furthermore, AC-coupling capacitors are employed at the input and at the output so as to reject low frequency disturbances, such as baseline wander or power line interferences, and dc offset voltage, caused by electrode polarization, typical of those circuits used to sense weak and slow-varying biological signals.

Hence, the circuit described is presented as follows:

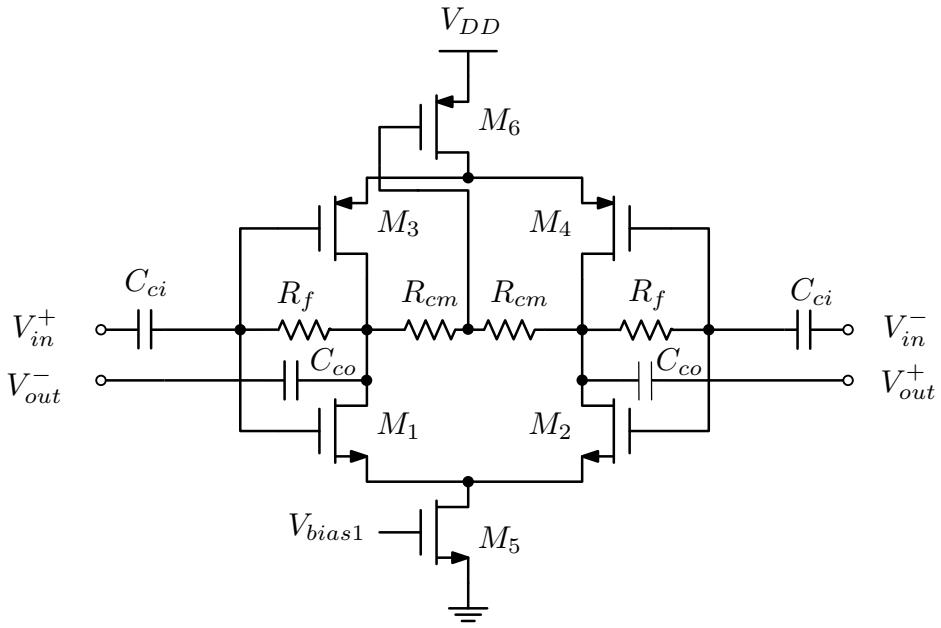


Figure 12: Final scheme of a single stack inverter-based amplifier.

3.6.1 Stacking Principle

In order to further reduce noise levels, current reuse can be implemented multiple times, that is to say, increasing the number of times the current is shared. Hence, it follows that the transconductance G_m of the overall circuit can be further increased, while NEF and PEF can be further decreased. A straightforward way to increase the number of current-reuse is to vertically stack inverter-based amplifiers, where the number of times current is reused is equal to the number of stacks [7]. A direct consequence of increasing the number of stacks is a drop in flicker noise and thermal noise, compared to a circuit with only one stack, as shown in Fig. 13.

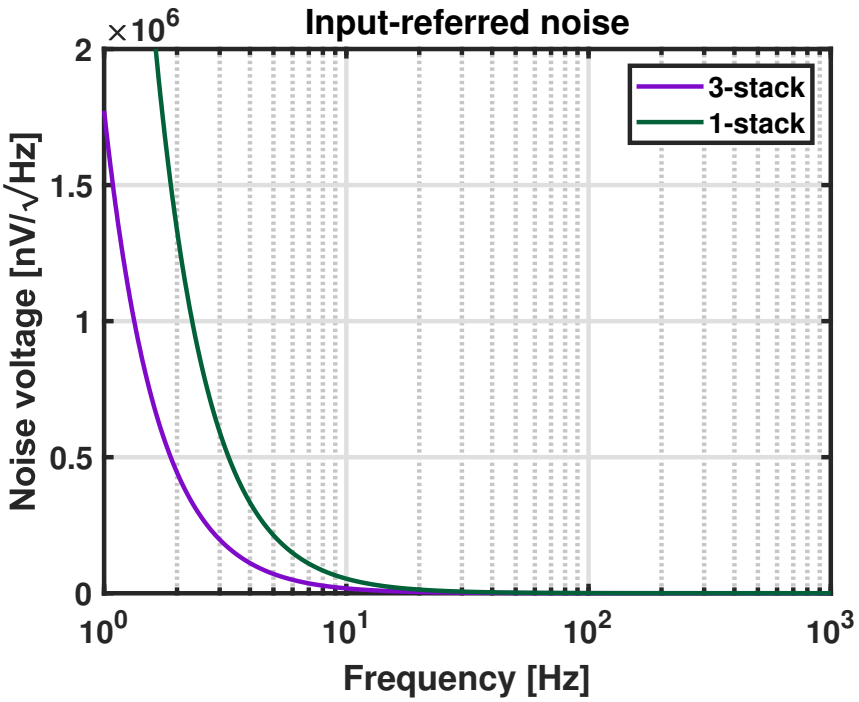


Figure 13: Input-referred noise of a stacked OTA.

3.7 Common Mode Rejection Ratio (CMRR)

Now, let *differential-mode* gain A_{dm} be defined as the change in the differential-mode output per unit change in the differential-mode input:

$$A_{dm} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} \tag{3.7.1}$$

where v_{od} is the output differential-mode signal, v_{id} is the input differential-mode signal and v_{ic} is the input common-mode signal.
Whereas, define *common-mode* gain A_{cm} as the change in the common-mode output per unit change in the common-mode input:

$$A_{cm} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} \tag{3.7.2}$$

where v_{oc} is the output common-mode signal.
Ideally, it might be desirable to obtain $A_{cm} = 0$. However, this does not happen even in the case where perfect symmetry is guaranteed, so to quantify the ability of a circuit to reject the common-mode, the common-mode rejection ratio CMRR is defined. This figure of merit expresses the ratio of the desired differential-mode A_{dm} gain to the undesired common-mode gain A_{cm} [2], and is stated as in equation (3.7.3).

$$CMRR \equiv \left|\frac{A_{dm}}{A_{cm}}\right| \tag{3.7.3}$$

3.8 Power Supply Rejection Ratio (PSRR)

As long as the supply voltages are constant, the output voltage of the amplifier depends only on the differential and common-mode input voltages. However, the supply voltage is only theoretically constant; in reality it may have some variations that are directly reflected on the output of the amplifier [2]. To quantify the circuit's ability to reject these variations, a block diagram of an amplifier with varying power-supply voltages is drawn in Fig. 14, where the small-signal variation on the positive and negative supply voltages is v_{dd} and v_{ss}, respectively.

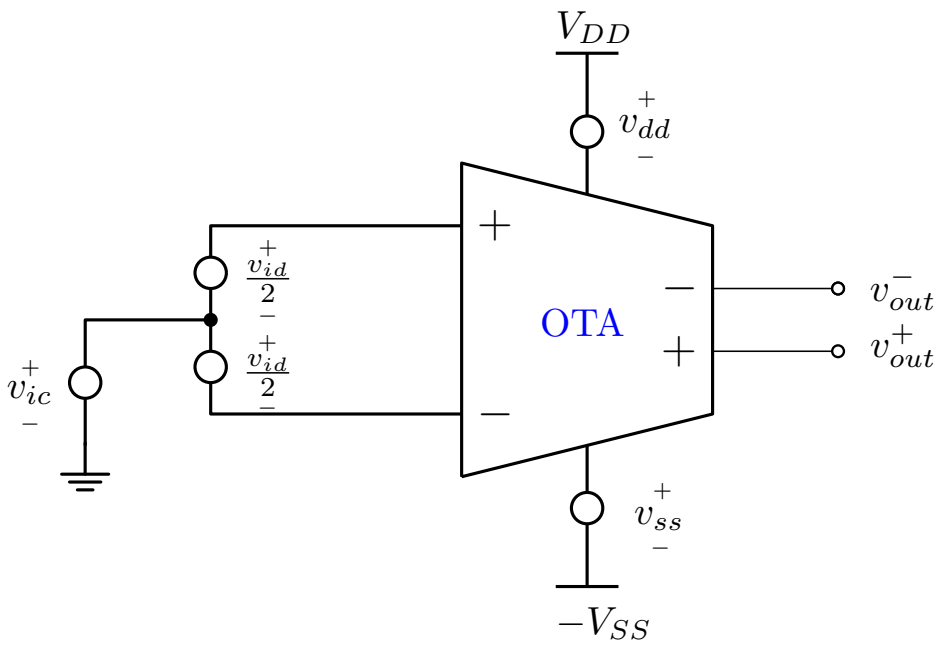


Figure 14: Block diagram of an OTA with varying power-supply voltages [2].

For simplicity $v_{ic} = 0$ is assumed, then the small-signal otput voltage v_o is written:

$$v_o = A_{dm} v_{id} + A^{+} v_{dd} + A^{-} v_{ss} \tag{3.8.1}$$

where A^+ and A^- are defined as the small signal gain from the positive and negative supply voltages to the output, respectively [2]. The above equation can be rewritten in the following way:

$$v_o = A_{dm}\left(v_{id} + \frac{v_{dd}}{PSRR^+} + \frac{v_{ss}}{PSRR^-}\right) \tag{3.8.2}$$

where $PSRR^+$ is defined as:

$$PSRR^+ = \frac{A_{dm}}{A^+} \tag{3.8.3}$$

and $PSRR^-$ is defined as:

$$PSRR^- = \frac{A_{dm}}{A^-}. \tag{3.8.4}$$

Thus, from the equations above it is straightforward that the power-supply rejecton ratios should be maximized in order to minimize unwanted voltage contributions at the output, superimposed to the desired signal.

4 Design of the amplifier

The design of the amplifier is based on the circuit architecture in [1] and will be analyzed in more detail in the following paragraphs. Starting from a brief overview of the overall system, next a detailed discussion will be given on the design of the amplifier, bias circuit, and MOS pseudo-resistors.

The design specifications are closely related to the characteristics of the signal to be acquired and to the characteristics of the implantable device. ECG is an extremely weak signal with amplitude values between $0.5\,mV$ and $5.0\,mV$, which are often dominated by a DC voltage component of up to $\pm 300\,mV$ [12]. The latter is a direct consequence of the contact made between electrode and skin, and together with a potential common-mode component (up to $1.5\,V$), arising instead from the potential established between electrodes and ground, is one of the first causes of an ineffective measurement. The ECG is a slowly varying signal; in fact, it has a narrow bandwidth, which, however, varies depending on the application. For ICU (intensive care unit) monitoring applications, the useful bandwidth of an ECG signal can range from $0.5\,Hz$ to $50\,Hz$, up to $1\,kHz$ for late-potential measurement (pacemaker detection). In principle, an ECG having a bandwidth between 0.05 Hz and 100 Hz is considered for a standard detection [12].

Furthermore, ECG signals can be corrupted by several types of noise [12], the main sources of which are:

1. power-line interference $(50 - 60\,Hz)$

2. electrode contact noise, i.e., associated with variable contact between electrode and skin, accounting for baseline wander

3. motion artifacts, which result in a change in the electrode-skin impedance, causing a drift in the baseline

4. muscle contraction, this in fact stimulates the generation of electromyographic signals (EMG), which are then mixed with ECG signals

5. respiration, which causes baseline drift

6. electromagnetic interference and coupled noise from other electronic devices

The following section briefly summarizes the characteristics that an analogue front-end (AFE) must have in order to process ECG signals, according to the disturbances outlined above.

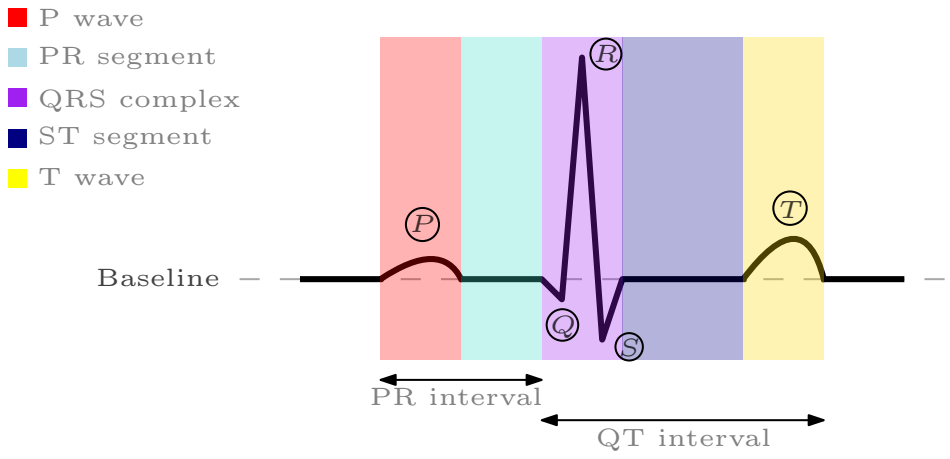


Figure 15: ECG trace example.

4.1 Design Specifications

Therefore, it has been understood that one of the fundamental requirements for the correct amplification of ECG signals implies the introduction of minimal noise so as not to distort the signal. However, the noise specification should not be so tight that it results in excessive power consumption, which would make the development of an implantable device prohibitive.

Considering the in-band signal occupation, it is straightforward to highlight the relevance of attenuating **flicker noise**, which would otherwise be critical [1].

In this regard, the amplifier is thought to be integrated into a device that implements chopper modulation. It follows, that the **bandwidth** of the amplifier depends on both the ECG signal bandwidth and the chopper frequency. The former is considered to be between $0.05\,Hz$ and $100\,Hz$ for this application, where the minimun signal frequency f_{min} is $0.05\,Hz$ and the maximum f_{max} is $100\,Hz$. The latter, on the other hand, must be chosen such that the minimum signal frequency, i.e., $0.05\,Hz$, is shifted beyond the corner frequency f_c between flicker noise and thermal noise. More precisely, it was observed that the corner frequency f_c is around $150\,Hz$. Therefore, assuming the following requirement:

$$f_{chopper} + f_{min} > f_c \tag{4.1.1}$$

it is found that f_c must be greater than $150\,Hz$.

Recalling that $f_{chopper} + f_{min}$ and $f_{chopper} + f_{max}$ must be within the amplifier bandwidth, it can be assumed that $f_{chopper}$ is $10 \times 150\,Hz$. Then it is obtained that $f_{chopper} + f_{min} \simeq 1.5\,kHz$ and $f_{chopper} + f_{max} \simeq 1.6\,kHz$.

Therefore, the bandwidth of the amplifier must be between $300\,Hz$ and $8\,kHz$.

For the **mid-band gain**, on the other hand, it is necessary to consider the possibility that the overall device has other circuit blocks, concerning which, however, it is not possible to determine a priori the gain that they introduce. Thus, a minimum target of $20\,dB$ can be formulated for the first amplification stage (the one whose design is the subject of this thesis), so as to significantly reduce the impact of noise introduced by subsequent blocks.

Moreover, electrode polarization induces a large dc offset at the amplifier input, so **offset rejection** is critical for the sake of not saturating the output voltage.

Besides, at the interface of the electrode to the skin tissue, an impedance is usually generated in the order of $100\,k\Omega$. As a result, it is clear that the AFE **input impedance** must be high enough to cause the interface impedance to be negligible. This prevents signal attenuation and avoids issues/artifacts as a result of electrode mismatch [1].

Moreover, the recording environment is often exposed to disturbances (e.g., power line interference at 50/60 Hz) and motion artifacts; therefore, it is strictly necessary for the amplifier to exhibit high **common mode rejection ratio (CMRR)** and **power supply rejection ratio (PSRR)** [1].

The amplifier, shown in Fig. 16, is ac-coupled through capacitors C_{ci} and C_{co}. However, given the low-frequency occupancy of the ECG signal, implementing ac-coupling at these frequencies would require large capacitors to such an extent that their integration to the circuit would

be compromised. Thus, a possible solution would be to modulate the baseband signal to higher frequencies by means of the chopper stabilization technique. The latter is also useful in mitigating flicker noise, the problematic nature of which was previously mentioned.

Finally, although stacking OTA allows the same current to be reused several times, for the same V_{dd}, it limits the headroom of the transistors and thus the output swing. Thus, OTA stacking could be used only in low-swing nodes, such as the first stage of a two-stage amplifier.

4.2 Stacked Inverter-Based Operational Transconductance Amplifier (OTA) Design

The circuit was implemented in 130-nm CMOS technology, considering a supply voltage V_{dd} equal to $1.2\,V$.

Then, power consumption P was set equal to that of the work in [1], $P = 13.2\,nW$, so as to obtain the design specification on the dissipated current I_{tail}:

$$I_{tail} = \frac{P}{V_{dd}} = \frac{13.2\,nW}{1.2\,V} = 11\,nA. \tag{4.2.1}$$

The tail current I_{tail} is split into the two branches, resulting in the following design specification on the drain current I_d of each MOS of the stacked-OTA:

$$I_d = \frac{I_{tail}}{2} = 5.5\,nA. \tag{4.2.2}$$

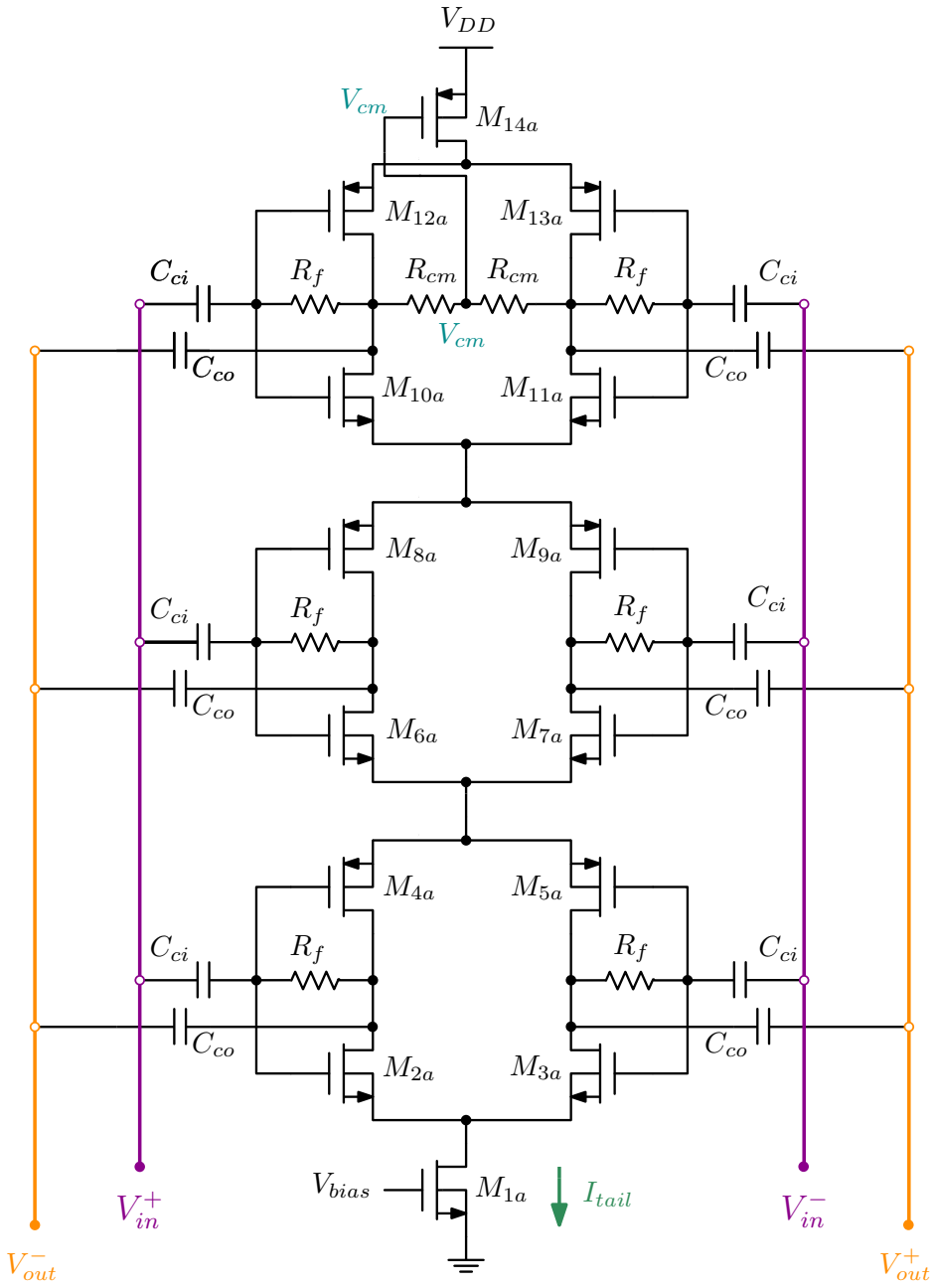


Figure 16: Circuit schematic of the fully differential 3 stack OTA.

Also, it is worth mentioning that each MOS must be sized so that the power-supply V_{dd} is equally distributed among all transistors. That is, the dc drain-to-source voltage V_{DS} ($|V_{DS}|$ in absolute value for PMOS transistors) must be the same for each transistor and equal to $150\,mV$.

4.2.1 DC behavior analysis and sizing of transistors

In the following the dc behavior of the amplifier and the sizing of the transistors will be analyzed.

In terms of dc behavior, R_f feedback resistors behave like short-circuits, so that the gate-to-source voltage V_{GS} of each transistor within the stack is fixed equal to the value of its drain-to-source voltage V_{DS}. R_f resistors implement self-biasing, as they fix the operating point and keep it stable, enabling robust operation. All transistors have the body-source terminals short-circuited to prevent threshold voltage variation due to the body effect, ensuring symmetrical operation of the circuit [1].

Thus, taking into account the very low power consumption and current values to be achieved, it is appropriate to bias the transistors in **weak inversion**, while also ensuring **saturation** operation; so it is necessary for the drain-to-source voltage V_{DS} to be at least greater than $100\,mV$.

The sizing of the transistors, which is necessary to identify the values of W and L, is then carried out through the g_m/I_D technique. The latter method often provides more reliable results than those that would be obtained by sizing the transistors using the I_D saturation drain current equation (square-law model), which is often more appropriate for

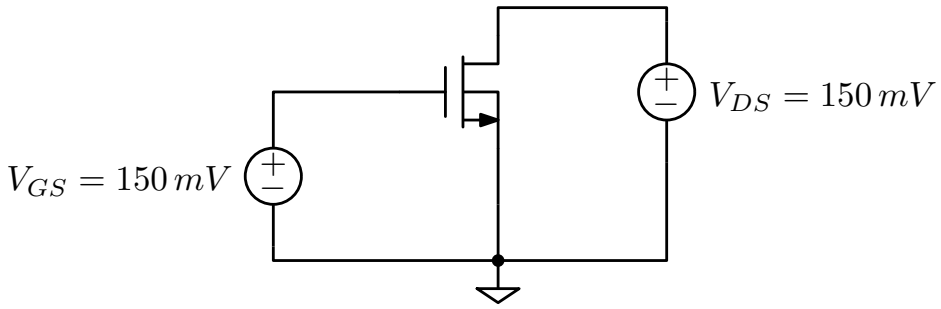


Figure 17: Circuit schematic of the inverter's NMOS for the g_m/I_D technique.

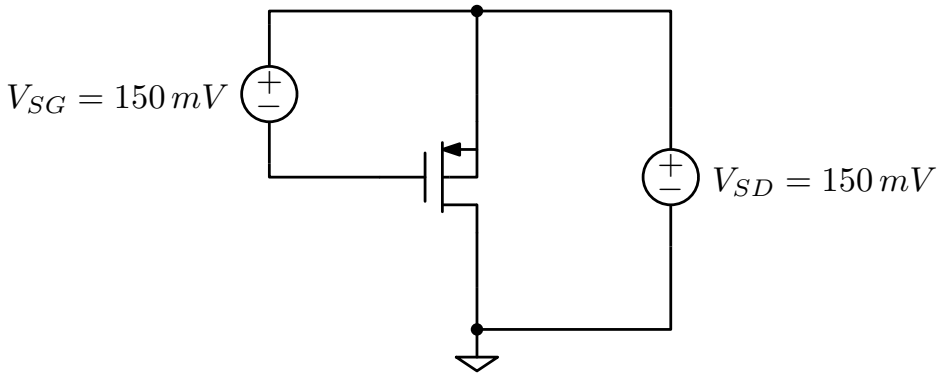


Figure 18: Circuit schematic of the inverter's PMOS for the g_m/I_D technique.

MOS biased in strong inversion. The circuit configurations for NMOS and PMOS, respectively, through which the g_m/I_D technique was implemented are the ones in figures 17 and 18.

A dc analysis was then performed by varying the value of V_{GS} (V_{SG} for PMOS) and the value of channel length L. For each NMOS, it is possible to calculate the value of the overdrive voltage V_{OV}, as the difference between the desired gate-to-source voltage V_{GS}, which is $150\,mV$, and the treshold voltage V_T set by the operating point (for PMOS, the similar approach applies, considering the signs of the voltages appropriately). Then, first the curves of g_m/I_D versus overdrive voltage V_{OV} were plotted, and for each curve the value of g_m/I_D corresponding to the pre-

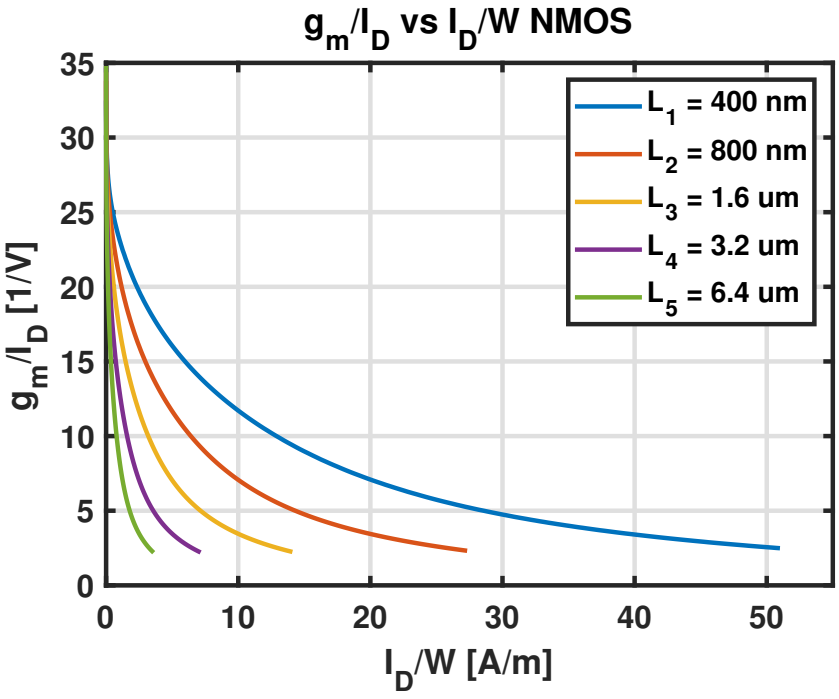


Figure 19: g_m/I_D curves versus I_D/W for different channel lenghts.

viously calculated overdrive value was identified. Finally, the curves of the g_m/I_D versus current density I_D/W were plotted, and for each curve a value of the I_D/W was identified, from which, knowing the value of the desired drain current I_D, the value of the width W was extrapolated. As an example, Fig. 19 shows a plot for several curves of the g_m/I_D versus I_D/W. The sizing was then modified iteratively in order to find the values of W and L that were best suited to meet the specifications, and is now reported in Table 2.

4.2.2 AC differential-mode small-signal analysis

In the following, the frequency behavior of the amplifier will be discussed through a small-signal ac analysis with purely differential inputs.
Under such assumptions, the decoupling of adjacent stacks is verified in-

MOS	*Width W*	*Length L*
$\mathbf{M_{1a}}$	2.6 μm	20 μm
$\mathbf{M_{n,inverter}}$	0.65 μm	9.2 μm
$\mathbf{M_{p,inverter}}$	7 μm	9.2 μm
$\mathbf{M_{14a}}$	0.85 μm	20 μm

Table 2: 3-stack OTA sizing.

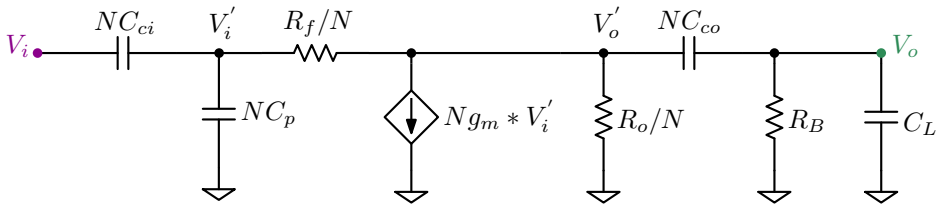


Figure 20: Differential-mode small-signal model of the stacked OTA [1].

trinsically. In fact, the intermediate nodes between the stacks are virtual shorts, so the stacks are independent of each other in terms of ac behavior. Thus, no explicit capacitors are needed for decoupling. Moreover, decoupling affects differential-mode analysis, while it does not interfere with common-mode analysis; therefore, high $CMRR$ and $PSRR$ values are obtained [1]. Overall, one can think of a single small-signal ac model of the circuit, identical for each stack, in which, however, the contributions of the various stacks are taken into account. As shown in Fig. 20, a single small-signal ac schematic is obtained in which the resistances are decreased by a factor N, equal to the number of stacks, and the capacitances and transconductances are increased by the same factor. Thus, although there is an increase equal to N in the total value of the transconductance G_{mo} and a decrease equal to N in the value of the output resistance R_o, the static gain of the circuit, equal to $G_{mo}R_o$, remains unchanged from that of a single stack.

For completeness, the differential-mode mid-band voltage gain A_v is reported as evaluated in the reference paper [1]:

$$A_{v1} \approx \frac{C_{ci}}{C_{ci}+C_p} G_{mo} R_o \frac{NC_{co}}{NC_{co}+C_L}. \tag{4.2.3}$$

While the open loop differential-mode voltage gain transfer function A_v is computed as follows:

$$A_v(s) \;=\; \frac{R_o+R_f}{1+G_m R_o}\cdot\left(\frac{1}{R_f}-G_m\right)\cdot(R_o\|R_f)\cdot(NR_B C_{co}C_{ci})\cdot\frac{s^2}{D(s)} \tag{4.2.4}$$

then the expanded expression for the denominator polynomial $D(s)$ is stated as follows:

$$\begin{aligned} D(s) = \; & 1 + s\Big\{R_B\,(NC_{co}+C_L) + \frac{1}{1+G_m R_o}\big[R_o C_{co} + \\ & + (R_o+R_f)(C_P+C_{ci})\big]\Big\} + s^2\Big\{\frac{R_o+R_f}{1+G_m R_o}\big(C_P + \\ & + C_{ci}\big)\Big[R_B\big(NC_{co}+C_L\big) + \big(R_o\|R_f\big)C_{co} + \frac{R_B R_o C_L C_{co}}{1+G_m R_o}\Big]\Big\} + \\ & + s^3\Big\{\frac{R_o+R_f}{1+G_m R_o}\big(R_o\|R_f\big)R_B C_L C_{co}\big(C_P+C_{ci}\big)\Big\} \end{aligned} \tag{4.2.5}$$

where C_{ci} is the input ac-coupling capacitor, C_{co} is the output ac-coupling capacitor, C_p is the input capacitance seen from the gate, C_L is the load capacitance, R_o is the output resistance and G_{mo} is the total transconductance, given by the sum of the NMOS and PMOS transconductances $g_{m,n} + g_{m,p}$.

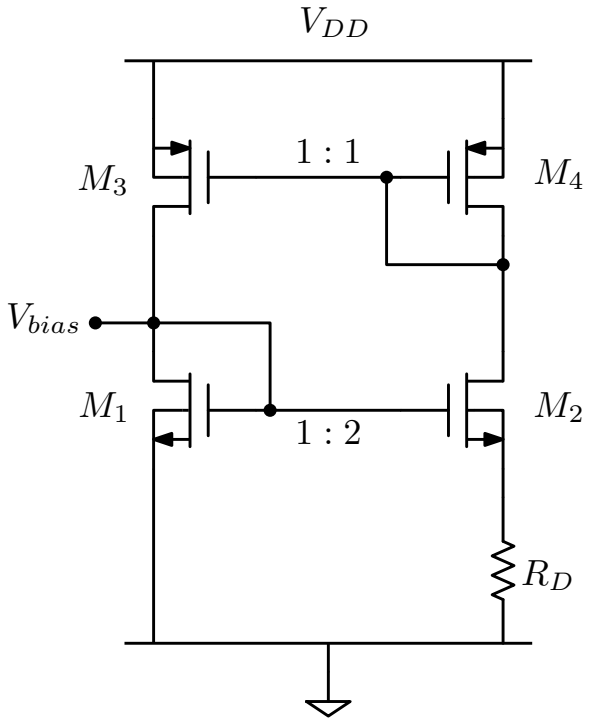


Figure 21: Constant g_m biasing circuit.

4.3 Biasing Circuit Design

There are many techniques for biasing an analog circuit, some guaranteeing constant gain, others constant voltage swing, constant power consumption or constant current consumption. The choice of one technique or another depends on what one wants to achieve, in this case a constant g_m *biasing circuit* was adopted. The bias voltage V_{bias} of the circuit in Fig. 16 can be established through a constant transconductance circuit.

The bias circuit in Fig. 21 consists of a PMOS current mirror, including M_3 and M_4, having mirror ratio of 1, an NMOS current mirror, which consists of M_1 and M_2, having mirror ratio of 2, and a resistor R_D on the source of M_2. The PMOS current mirror forces the same drain current in the two branches of the circuit:

$$I_{D3} = I_{D4} \tag{4.3.1}$$

thus, a Kirchoff's voltage law can be written around the loop consisting of M_1, M_2 and R_D:

$$V_{GS1} = V_{GS2} + I_{D2}R_D. \tag{4.3.2}$$

The expressions of V_{GS1} and V_{GS2} may be derived from the dc drain current of a subthreshold saturated MOS:

$$I_D = I_0\, exp\left(\frac{V_{GS} - V_T}{nV_{th}}\right), \tag{4.3.3}$$

$$I_0 = 2n\mu C'_{OX}\left(\frac{W}{L}\right)V_{th}^2 \cdot \left[1 - exp\left(-\frac{V_{DS}}{V_{th}}\right)\right]. \tag{4.3.4}$$

Then, the Kirchoff's voltage law may be rewritten as follows:

$$nV_{th}ln\left(\frac{I_{D1}}{I_0}\right) + V_T = nV_{th}ln\left(\frac{I_{D2}}{I_0}\right) + V_T + I_{D2}R_D \tag{4.3.5}$$

which, assuming that M1 and M2 are matched and with the same threshold voltage, can be simplified as:

$$nV_{th}ln\left(\frac{I_{D1}}{I_0}\right) = nV_{th}ln\left(\frac{I_{D2}}{I_0}\right) + I_{D2}R_D. \tag{4.3.6}$$

Thus, remembering that $I_{D1} = I_{D2}$, the expression in (4.3.6) may be rewritten as:

$$I_{D1}R_D = nV_{th}\left[ln\left(\frac{I_{D1}}{I_0}\right) - ln\left(\frac{I_{D1}}{2I_0}\right)\right] = nV_{th}ln(2), \tag{4.3.7}$$

which leads to:

$$I_{D1} = \frac{nV_{th}ln(2)}{R_D}. \tag{4.3.8}$$

Recalling the following expression for the transconductance of M1, saturated in subthreshold:

$$g_{m1} = \frac{I_{D1}}{nV_{th}} \tag{4.3.9}$$

this relatioship is obtained:

$$g_{m1} = \frac{ln(2)}{R_D}. \tag{4.3.10}$$

Neglecting channel length modulation and the body effect, this bias circuit should guarantee that the transconductance g_{m1} is inversely proportional to the resistance R_D [13]. That said, if temperature changes, and so μ_n and C_{OX}, the change in gate-to-source voltage V_{GS1} at the terminals of M1 is such that g_{m1} remains almost unchanged as the temperature changes. The behavior of transconductance g_{m1} as temperature changes over a range from 0 °C to 70 °C, processed from a parametric

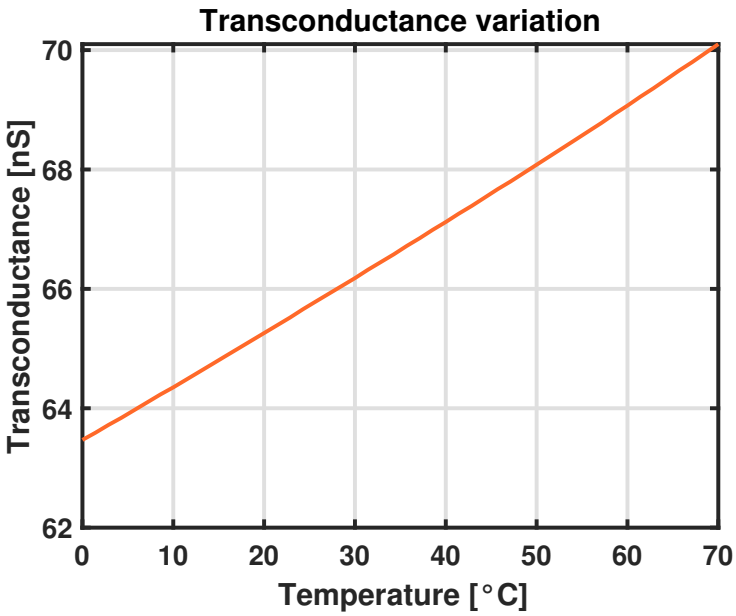


Figure 22: Simulated g_m as a function of temperature.

simulation in *Cadence Virtuoso*, is shown in Fig. 22. The simulation shows a linear variation of the transconductance g_{m1} from the value at 27 °C, that is $g_{m1} = 65.92\,nS$. The change of in the transconductance g_{m1} with respect to temperature is about $6.63\,nS$, corresponding to 10% of the value obtained at 27 °C.

In conclusion, sizing of MOS transistors in the biasing circuit is summarized in Table 3, where a resistance $R_D = 9.2\,M\Omega$ was considered:

MOS	***Width W***	***Length L***
$\mathbf{M_1}$	0.65 μm	20 μm
$\mathbf{M_2}$	1.3 μm	20 μm
$\mathbf{M_3}$	2.6 μm	20 μm
$\mathbf{M_4}$	2.6 μm	20 μm

Table 3: Biasing circuit sizing.

4.4 MOS Pseudo-Resistors Design

The resistors implemented through pseudo-resistors are the ones that follow: the load resistor R_B, the resistor R_f, which achieves a local feedback loop, and the resistor R_{cm}, which senses the common-mode output voltage v_{cm}.

The values of the dc voltage generator V_{Gen}, MOS width W and length L were determined such that the equivalent impedance Z_{eq}, emulated by the pseudo-resistor, exhibits these characteristics:

- Low-frequency amplitude equal to the desired resistance value.
- Cut-off frequency greater than the amplifier's higher cut-off frequency f_H, so as not to distort the input signal.

Resistor	**Pseudo-resistor type**	**Required value**	**Obtained value**
$\mathbf{R_B}$	Parallel	20 $M\Omega$	20.4 $M\Omega$
$\mathbf{R_f}$	Series	700 $M\Omega$	732.97 $M\Omega$
$\mathbf{R_{cm}}$	Series	700 $M\Omega$	732.97 $M\Omega$

Table 4: MOS pseudo-resistors design features.

4.4.1 Parallel Architecture Design

The parallel configuration, shown in Fig. 24, consists of MOS M_{1p} and M_{2p}. This architecture was chosen to implement resistors R_B and R_f, whose target resistance value is at least 700 $M\Omega$.

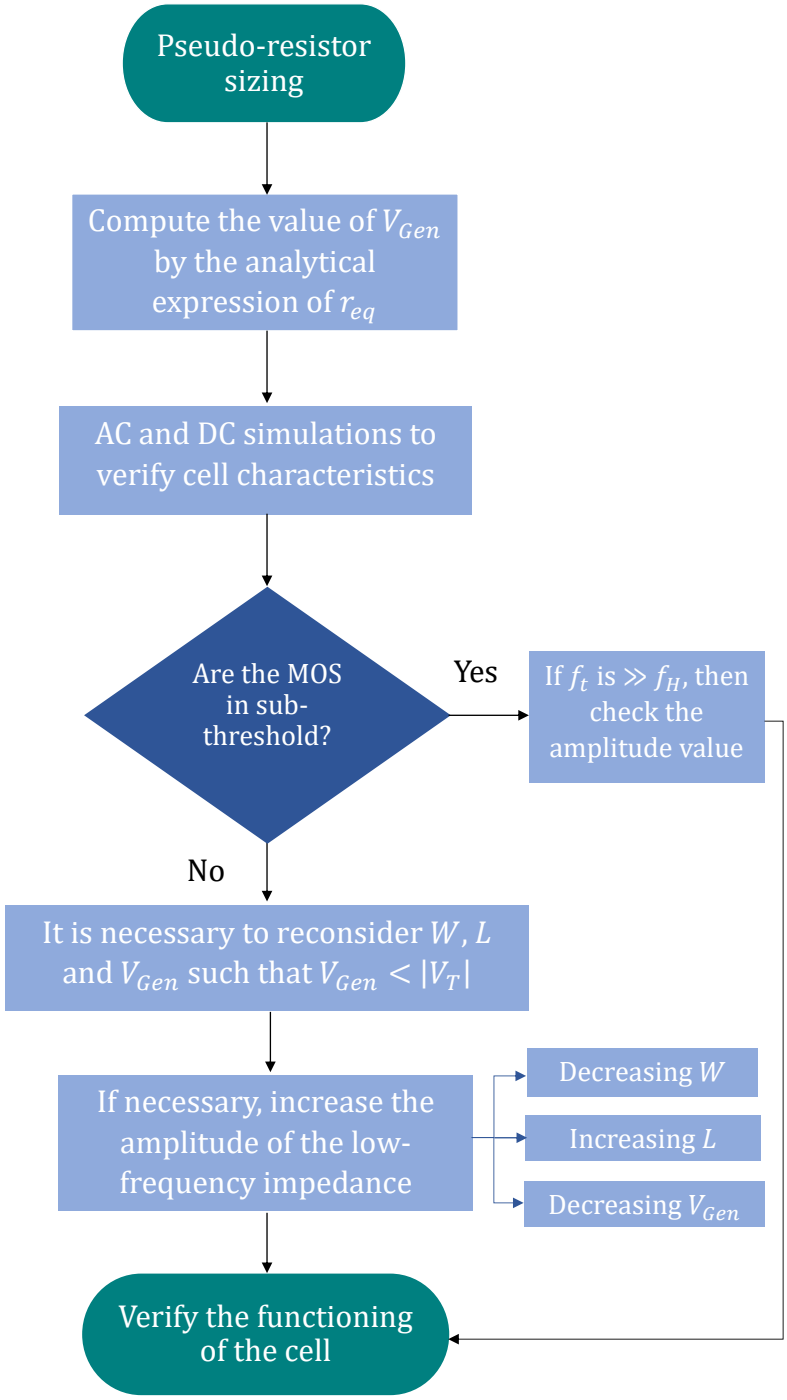


Figure 23: Pseudo-resistors design flow.

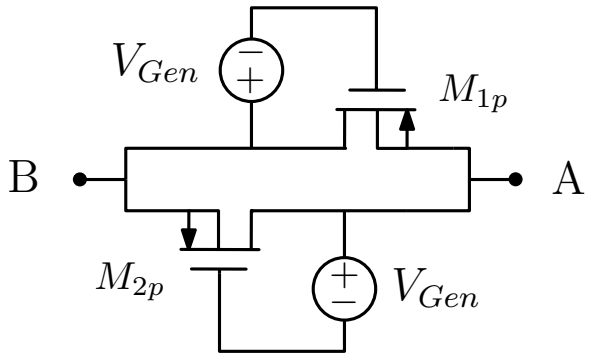


Figure 24: Parallel pseudo-resistor configuration (single cell).

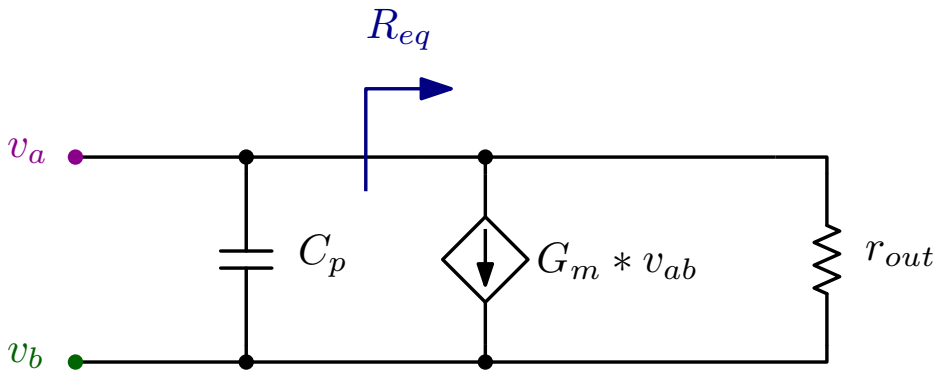


Figure 25: Small-signal equivalent circuit of a pseudo-resistor in parallel configuration.

The small-signal circuit of the parallel pseudo-resistor is shown in Fig. 25. C_p is the equivalent parasitic capacitance seen between terminals A and B in Fig. 24, given by the parallel of the source-to-gate C_{sg} and gate-to-bulk C_{gb} capacitances of the two PMOS transistors. Thus, r_{out} is the equivalent output resistance of the cell, computed as the parallel of the two output resistances r_{eq}, which, given that the two transistors are identical, is the same for each of them. G_m is the total transconductance of the cell, equal to the sum of each MOS transconductances g_m.

Then, from the small-signal model of the pseudo-resistor an estimate of the cut-off frequency f_T, associated with the equivalent impedance Z_{eq} transfer function, can be derived. The cut-off frequency f_T can be expressed as:

$$f_T = \frac{1}{2\pi} \cdot \frac{1}{R_{eq} C_p}, \tag{4.4.1}$$

where the small-signal equivalent resistance value R_{eq} of the cell may be written as:

$$R_{eq} = \frac{r_{out}}{1 + G_m r_{out}}. \tag{4.4.2}$$

Then, if the condition $G_m r_{out} \ll 1$ is verified, R_{eq} may be simplified as:

$$R_{eq} = r_{out} = r_{eq} \| r_{eq} = \frac{r_{eq}}{2}. \tag{4.4.3}$$

Then, r_{eq} might be computed from the expression for the drain current of a PMOS transistor in sub-threshold, which is recalled in the following:

$$i_{SD} = I_{SD0} \cdot exp\left(\frac{v_{SG}}{n V_{th}}\right) \cdot \left[1 - exp\left(-\frac{v_{SD}}{V_{th}}\right)\right] \tag{4.4.4}$$

where

$$I_{SD0} = 2n\mu C'_{OX} \left(\frac{W}{L}\right) V_{th}^2 \cdot exp\left(-\frac{V_T}{n V_{th}}\right). \tag{4.4.5}$$

Thus, r_{eq} may be written as the inverse function of the derivative of the drain current with respect to the source-to-drain voltage:

$$r_{eq}|_{V_{AB}=0} = \left(\left.\frac{\partial i_{SD}}{\partial v_{SD}}\right|_{V_{SD}=0}\right)^{-1} = \frac{V_{th}}{I_{SD0}} \cdot exp\left(-\frac{V_{Gen}}{n V_{th}}\right). \tag{4.4.6}$$

Therefore, by expanding the expression of I_{SD0}, r_{eq} may be written as a function of the voltage betwen gate and source V_{Gen}:

$$r_{eq} = \frac{1}{2n\mu C'_{ox} V_{th}} \cdot \frac{L}{W} \cdot exp\left(\frac{|V_T| - V_{Gen}}{nV_{th}}\right). \tag{4.4.7}$$

While the equivalent parasitic capacitance C_p, given that the two transistors are in weak inversion, may be simplified as:

$$C_{eq} \simeq 2 \cdot C_{gb}. \tag{4.4.8}$$

Recall that the gate-to-bulk capacitance C_{gb} can be expressed in the following way for a sub-threshold MOS:

$$C_{gb} = W \cdot L \cdot \left(\frac{C_{ox} C_{js}}{C_{ox} + C_{js}}\right), \tag{4.4.9}$$

where C_{ox} is the oxide capacitance, C_{js} is the junction capacitance, W and L are, respectively, the width and length of the MOS transistor.
Thus, the analysis of the behavior of a pseudo-resistor in parallel configuration is carried out with the aim of obtaining an equivalent impedance Z_{eq}, with a low-frequency value equal to $r_{eq}/2$, in the order of $700\,M\Omega$, and a cut-off frequency above $f_H = 10.8\,kHz$.
The design flow, shown in Fig. 23, can be summarized as follows: first, the value of the dc voltage generator V_{gen} is calculated as a function of the desired equivalent resistance value r_{out}, through the previously mentioned relationship between r_{eq} and V_{gen}. Through simulation, it should

be verified that the transistors are in sub-threshold operating region and that the r_{out} value is satisfactory; if so, it must be verified that the condition on the cut-off frequency f_T is fulfilled. If, on the other hand, the small signal equivalent resistance r_{out} value is out of specification, and therefore much lower than $700\,M\Omega$ (if it were higher it would still be acceptable, the specification is at least $700\,M\Omega$), the values of the parameters W, L and V_{Gen} must be changed.
In order to increase r_{eq} there are three possible ways:

1. decrease W
2. increase L
3. decrease V_{gen}

In the first case, it was observed that by decreasing the value of W, the modulus of the threshold voltage $|V_T|$ does not vary appreciably. Therefore, since there is a direct proportionality relationship between W and the junction capacitance C_{js}, decreasing the width W decreases C_{js} and so does C_{gb}, as a direct consequence an increase in f_T is obtained. This condition is favorable, in fact an increase in the value of r_{out} is obtained and the cutoff frequency f_T moves to even higher frequencies.
From the second case, it was observed that C_{js} remains almost unchanged as L increases, whereas the modulus of $|V_T|$ decreases. However, this is nevertheless helpful as it means that even lower value of V_{Gen} can be used, thus increasing the value of r_{out}.
The third case must be evaluated wisely, since, it is true that, decreasing the value of V_{Gen}, the value of r_{eq} increases, however, if $V_{Gen} \ll |V_T|$ the

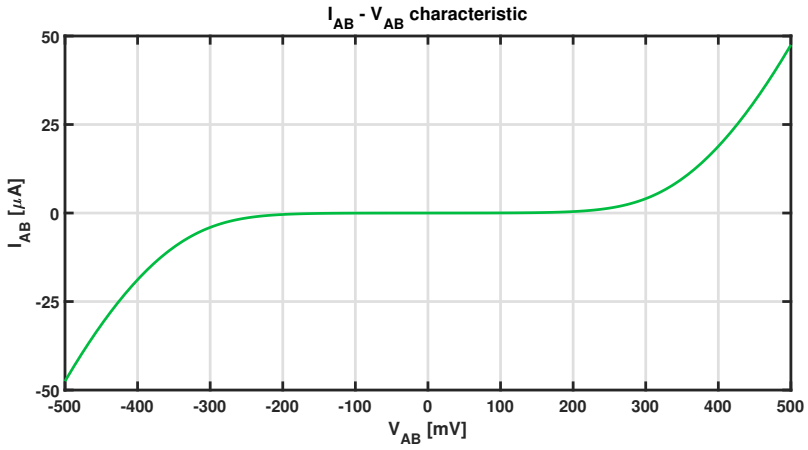


Figure 26: $I_{AB} - V_{AB}$ characteristic.

transistors go into interdiction and this must be avoided in any case.

Table 5, shown below, displays the sizing of transistors for a single cell in parallel configuration, where a V_{Gen} value of $20\,mV$ was chosen.

MOS	***Width W***	***Length L***
$\mathbf{M_{1p}}$	5 μm	0.29 μm
$\mathbf{M_{2p}}$	5 μm	0.29 μm

Table 5: Parallel pseudo-resistor configuration sizing.

Some graphs are given for completeness. The first one in Fig. 26, is related to the $I_{AB} - V_{AB}$ characteristic and highlights the DC behavior of the pseudo-resistor. The one in Fig. 27 and the one in Fig. 28 represent the transfer function of the equivalent impedance emulated by the cell, in dB and Ω, respectively. From the latter two, it can be seen that although the cut-off frequency $f_T = 921\,kHz$ is in specification, the low-frequency amplitude $r_{out} = r_{eq}/2 = 10.2\,M\Omega$ does not match what was initially predicted.

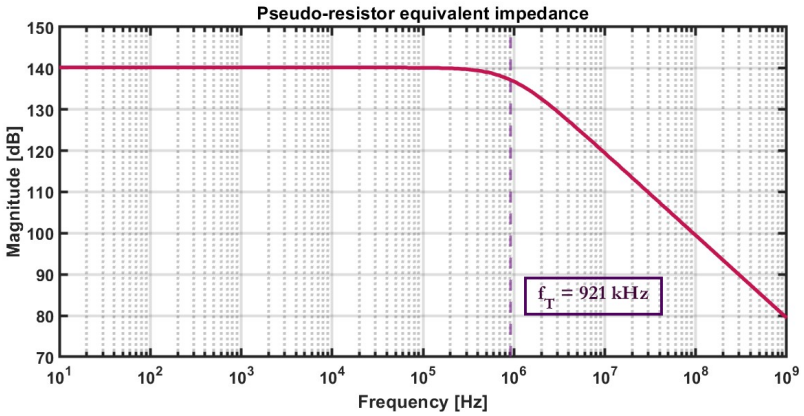


Figure 27: Parallel pseudo-resistor equivalent impedance in dB.

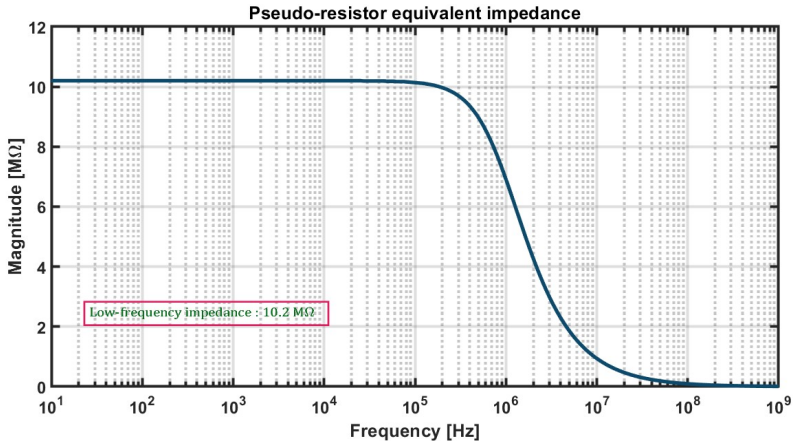


Figure 28: Parallel pseudo-resistor equivalent impedance in Ω.

Table 6 summarizes what has just been observed.

Parameter	***Target value***	***Obtained value***	***Assessment***
$\mathbf{r_{out} = r_{eq}/2}$	20 $M\Omega$	10.2 $M\Omega$	*Not enough*
$\mathbf{f_T}$	$\gg 10.8\,kHz$	921 kHz	✓

Table 6: Parallel pseudo-resistor obtained features.

But since an impedance of $20\,M\Omega$ is required, it was chosen to place two identical cells in cascade, as shown in Fig. 29. In this way the low-frequency impedance r_{out} is doubled, but the cut-off frequency f_T remains almost unchanged. What has just been stated is a direct consequence of cascading two identical cells in a parallel configuration. In fact, the equivalent small-signal resistance r_{out} doubles, while the total capacitance is halved, so the cut-off frequency does not vary appreciably. It is therefore possible, to obtain an impedance with a low-frequency amplitude of $20.4\,M\Omega$, as shown in the two graphs reported in Fig. 30 and in Fig. 31.

Parameter	***Target value***	***Obtained value***	***Assessment***
$\mathbf{r_{out} = r_{eq}/2}$	20 $M\Omega$	20.4 $M\Omega$	✓
$\mathbf{f_T}$	$\gg 10.8\,kHz$	921 kHz	✓

Table 7: Features of the parallel pseudo-resistor with two cells.

In addition, cascading two identical cells results in a more linear $I_{AB} - V_{AB}$ characteristic, as shown in Fig. 32.

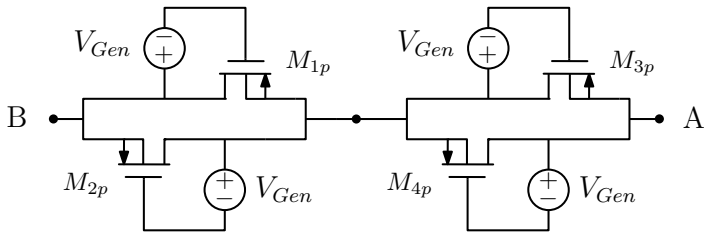


Figure 29: Parallel pseudo-resistors configuration (two cells configuration).

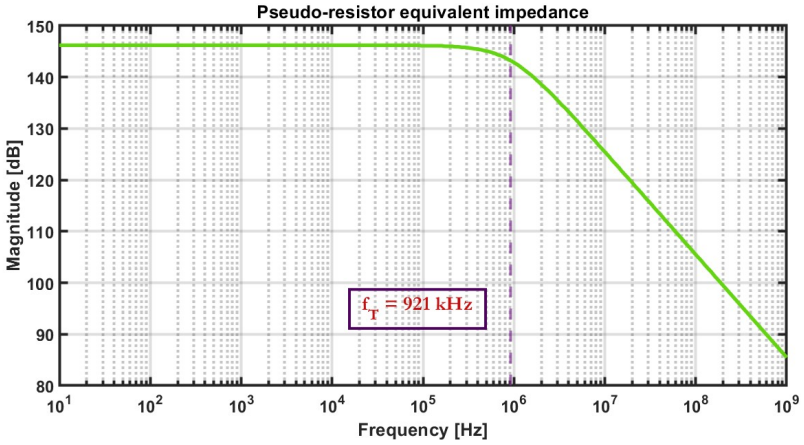


Figure 30: Parallel pseudo-resistor equivalent impedance in dB (two cells configuration).

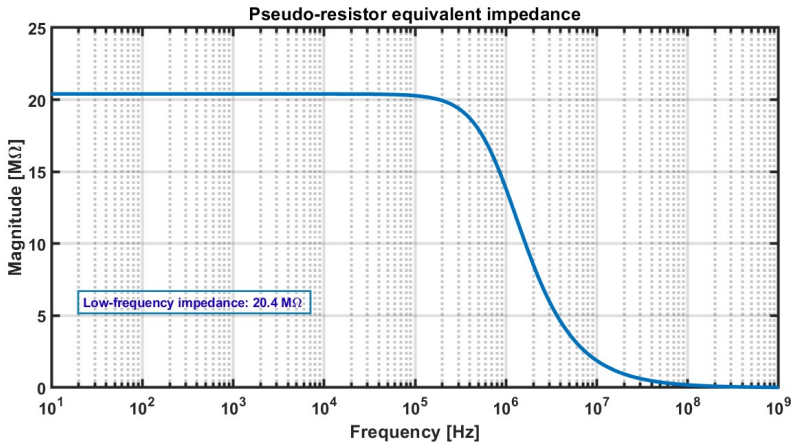


Figure 31: Parallel pseudo-resistor equivalent impedance in Ω (two cells configuration).

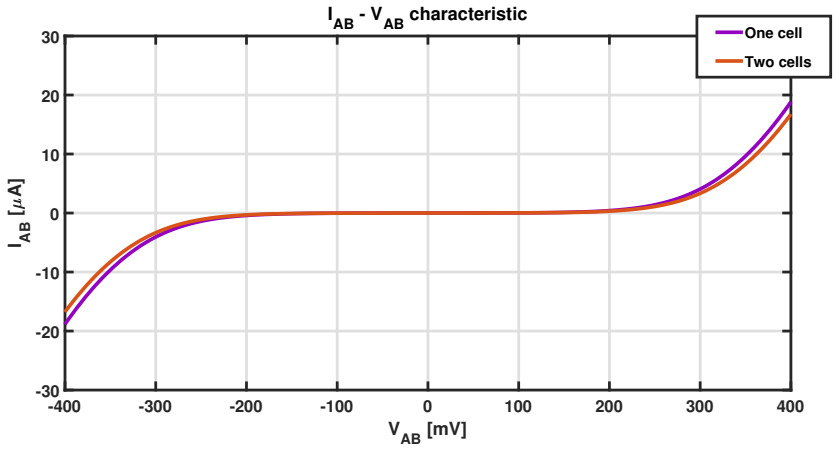


Figure 32: Extension of linearity as the number of cascaded stages increases.

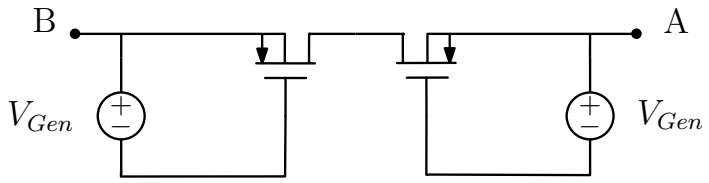


Figure 33: Series pseudo-resistors configuration.

4.4.2 Series Architecture Design

The resistors R_{cm} and R_f were implemented through a series configuration, whose schematic is represented in Fig. 33. Indeed, a series configuration makes it easier to obtain high resistance values in the order of $700\,M\Omega$. The design procedure is conceptually similar to that for the parallel configuration. In Table 8 the sizing of a cell in series configuration is given, where a value of V_{Gen} equale to $1\,mV$ was considered. Table 9 shows the features achieved. And finally, the graphs in Fig. 35 and Fig. 36 show the impedance transfer function of the pseudo-resistor, implemented in series configuration, in dB and in Ohm, respectively.

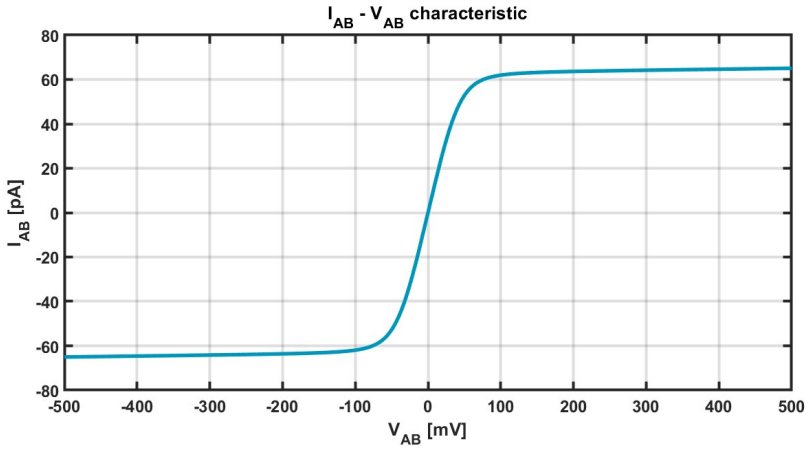


Figure 34: $I_{AB} - V_{AB}$ characteristic.

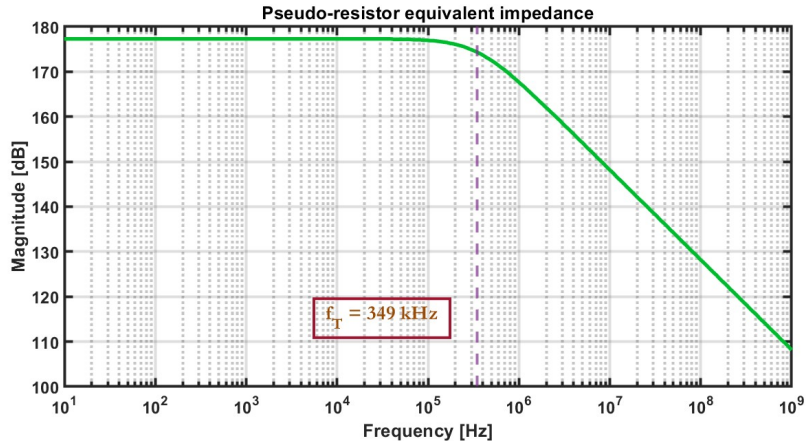


Figure 35: Series pseudo-resistor equivalent impedance in dB.

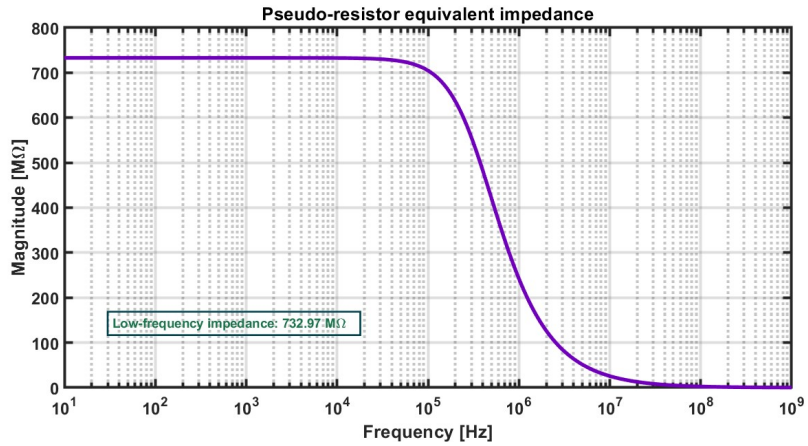


Figure 36: Series pseudo-resistor equivalent impedance in Ω.

MOS	$Width\,W$	$Length\,L$
$\mathbf{M_{1s}}$	1 μm	1 μm
$\mathbf{M_{2s}}$	1 μm	1 μm

Table 8: Series pseudo-resistor configuration sizing.

$Parameter$	$Target\,value$	$Obtained\,value$	$Assessment$
$\mathbf{r_{out} = r_{eq}/2}$	700 $M\Omega$	732.97 $M\Omega$	✓
$\mathbf{f_T}$	$\gg 10.8\,kHz$	349 kHz	✓

Table 9: Features of the series pseudo-resistor configuration.

5 Results

This chapter provides results for the differential-mode gain A_{dm}, common-mode gain A_{cm}, input-referred noise voltage v_n, common-mode rejection ratio ($CMRR$), and power supply rejection ratio ($PSRR$).
Simulations were carried out in CADENCE VIRTUOSO, while plot editing was performed in MATLAB.

5.1 Simulation Setup

The simulation setup, shown in Fig. 37, is made up as follows: the core consists of an instance, in which the amplification and bias circuits are present, the differential inputs are connected via an ideal balun to two voltage generators, one for the differential-mode and one for the common-mode, while for each branch of the differential output there is the parallel of the load resistor R_B and the capacitor C_L.

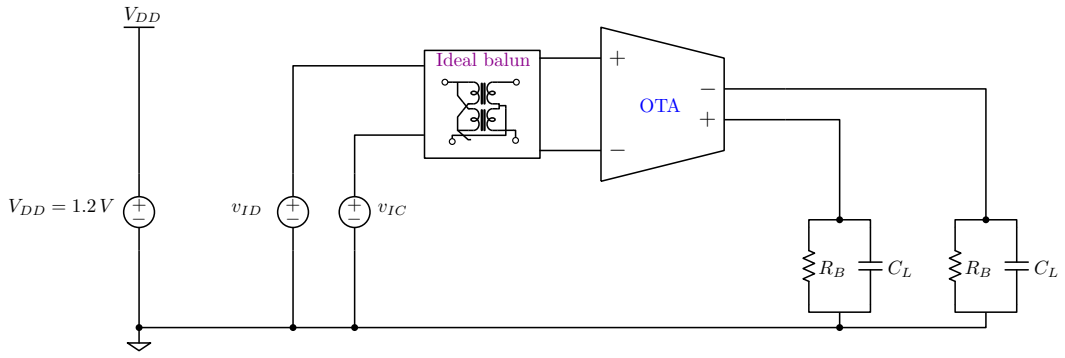


Figure 37: Simulation setup in Cadence

5.2 Differential Mode Gain A_{dm}

The differential-mode gain A_{dm}, simulated by setting the ac magnitude value of the differential-mode voltage generator equal to 1 (while the ac

magnitude value of the common-mode voltage generator is fixed at 0), is shown in Fig. 38. The in-band differential gain A_{dm0} is 23.9 dB, the lower cut-off frequency f_L and upper cut-off frequency f_H are, respectively, 289 Hz and 10.8 kHz. The bandwidth BW, on the other hand, is equal to 10.5 kHz. The results obtained are in accordance with what was expected.

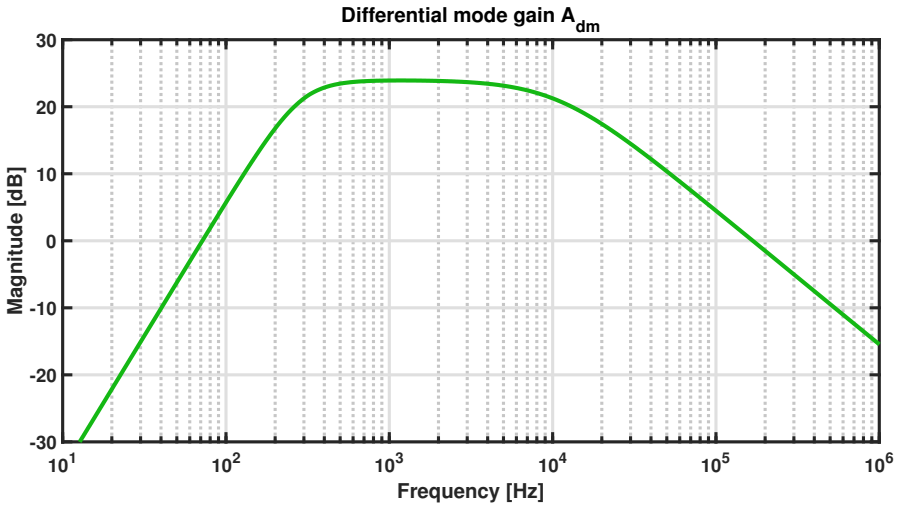


Figure 38: Open-loop differential-mode gain A_{dm}.

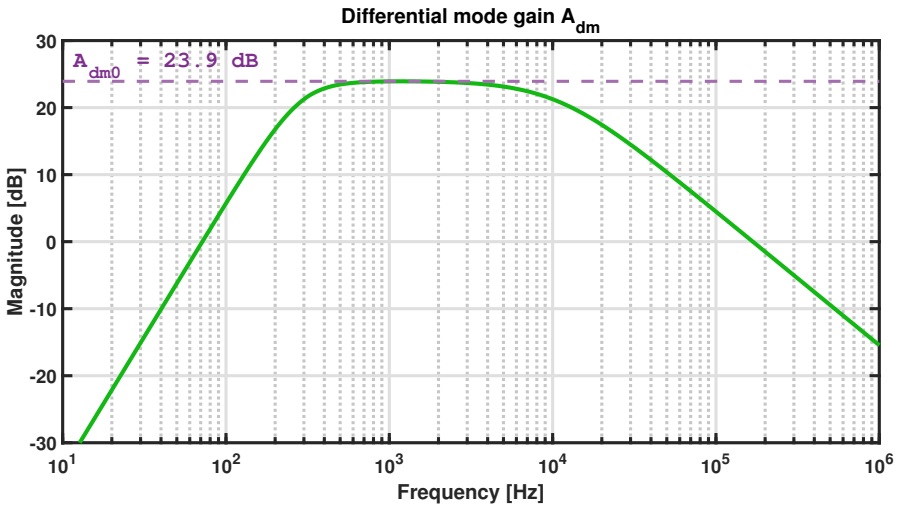


Figure 39: Open-loop differential-mode gain A_{dm}.

As shown in Fig. 40, there's a high frequency zero located at f_Z =

$15\,MHz$. As expected, it does not modify the differential-mode signal transfer function A_{dm}, as it does not interfere with the position of the poles.

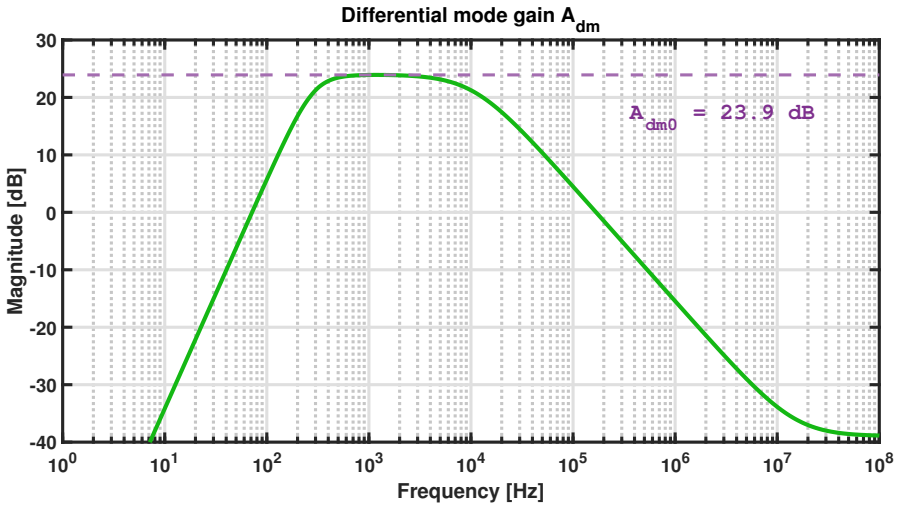


Figure 40: Open-loop differential-mode gain A_{dm}.

The results of the ac small-signal differential-mode analysis are summarized in Table 10.

Parameters	**Simulated results**
In-band differential-mode gain $\mathbf{A_{dm0}}$	23.9 dB
Low frequency pole $\mathbf{f_L}$	289 Hz
High frequency pole $\mathbf{f_H}$	10.8 kHz
High frequency zero $\mathbf{f_Z}$	15 MHz
Bandwidth **BW**	10.5 kHz

Table 10: Differential-mode analysis results.

5.3 Common Mode Gain A_{cm}

The common-mode gain is shown in Fig. 41. It can be observed that it always assumes amplitude values below $-24\,dB$, where the latter value

was measured at the frequency of 269.15 Hz. Whereas at the lower cut-off frequency f_L and the higher cut-off frequency f_H, the following results are observed:

$$\begin{cases} A_{cm} = -24.5\,dB \;\; for\, f = f_L = 289\,Hz \\ A_{cm} = -33\,dB \;\; for\, f = f_H = 10.8\,kHz \end{cases} \tag{5.3.1}$$

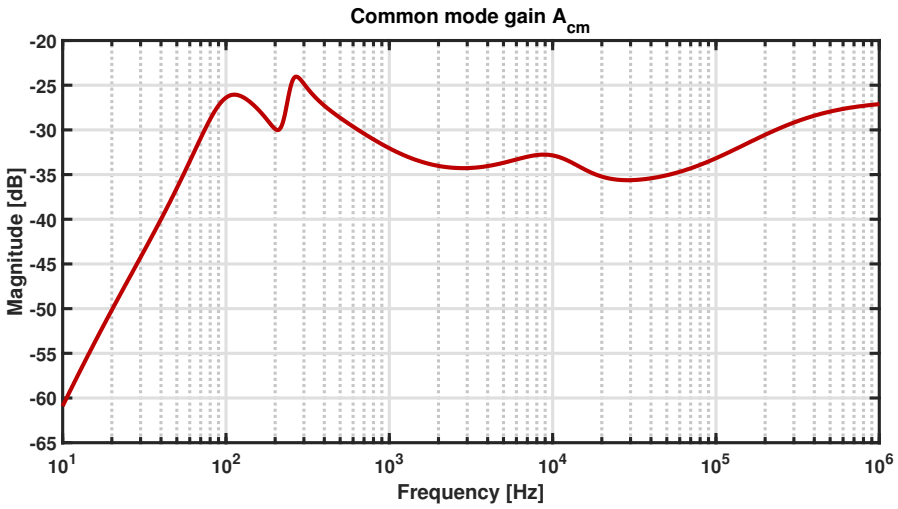


Figure 41: Open-loop common-mode gain A_{cm}.

so the results obtained show good attenuation of the common-mode component within the band of interest.

5.4 Noise Analysis

In the following the results of the NOISE simulation will be discussed. The input-referred noise voltage, expressed in dB, is shown in Fig. 42. The output-referred noise voltage was first calculated; then, by dividing the latter by the square of the differential-mode gain, an expression for the input-referred noise voltage was obtained:

$$\overline{v_{n,in}^2} = \frac{\overline{v_{n,out}^2}}{A_v^2}. \tag{5.4.1}$$

Then substituting the expressions computed for $\overline{v_{n,out}^2}$ and A_v^2, results in:

$$\begin{aligned}\overline{v_{n,in}^2} = \Bigg(&\frac{4k_BT}{R_L} + 4k_BT\frac{\gamma}{\alpha}Ng_{m,n} + 4k_BT\frac{\gamma}{\alpha}Ng_{m,p} + \\ &+ \frac{K_n}{f}\frac{N\cdot g_{m,n}^2}{(WL)_nC_{ox}} + \frac{K_p}{f}\frac{N\cdot g_{m,p}^2}{(WL)_pC_{ox}}\Bigg)\cdot\frac{1}{G_m^2}\end{aligned} \tag{5.4.2}$$

where G_m is the sum of the transconductances of NMOS and PMOS of each inverter. Thus, assuming them to be equal, which is reasonable given the values of $g_{m,n} = 152.92\,nS$ and $g_{m,p} = 154.68\,nS$, obtained previously, the expression in (5.4.2) is simplified as follows:

$$\begin{aligned}\overline{v_{n,in}^2} = &\frac{4k_BT}{R_L}\cdot\frac{1}{4Ng_m^2} + \frac{4k_BT\cdot\gamma/\alpha}{2Ng_m} + \\ &+ \frac{1}{4Nf}\cdot\left[\frac{K_n}{(WL)_nC_{ox}} + \frac{K_p}{(WL)_pC_{ox}}\right].\end{aligned} \tag{5.4.3}$$

Therefore, the input-referred noise voltage at the lower cut-off frequency f_L and at the higher cut-off frequency f_H takes on these values:

$$\begin{cases} v_{n,in} = -136.4\,dB \;\; for\, f = f_L = 289\,Hz \\ v_{n,in} = -138.7\,dB \;\; for\, f = f_H = 10.8\,kHz \end{cases} \tag{5.4.4}$$

the latter correspond to the following values in $nV/\sqrt{Hz}$, as highlighted in (5.4.5).

$$\begin{cases} v_{n,in} = 152\,nV/\sqrt{Hz} \;\; for\, f = f_L = 289\,Hz \\ v_{n,in} = 116\,nV/\sqrt{Hz} \;\; for\, f = f_H = 10.8\,kHz \end{cases} \tag{5.4.5}$$

For completeness, the results for NEF and PEF are reported below:

$$NEF = v_{ni,rms} \cdot \sqrt{\frac{2}{\pi} \cdot \frac{I_{tot}}{4k_B T \cdot V_{th} \cdot BW}} \; = \; 0.47 \tag{5.4.6}$$

$$PEF = NEF^2 \cdot V_{DD} \; = \; 0.27 \tag{5.4.7}$$

where an *rms* input-referred noise voltage equal to $v_{rms,in} = 1.20 \cdot 10^{-5}\,V$ was considered.

As seen in Fig. 42, the results for the input-referred noise voltage are in agreement with what was originally predicted.

The results obtained are summarized in Table 11.

Parameters	**Simulated results**
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_L})$	-136.4 dB
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_H})$	-138.7 dB
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_L})$	152 $nV/\sqrt{Hz}$
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_H})$	116 $nV/\sqrt{Hz}$
Noise Efficiency Factor **NEF**	0.47
Power Efficiency Factor **PEF**	0.27

Table 11: Noise analysis results.

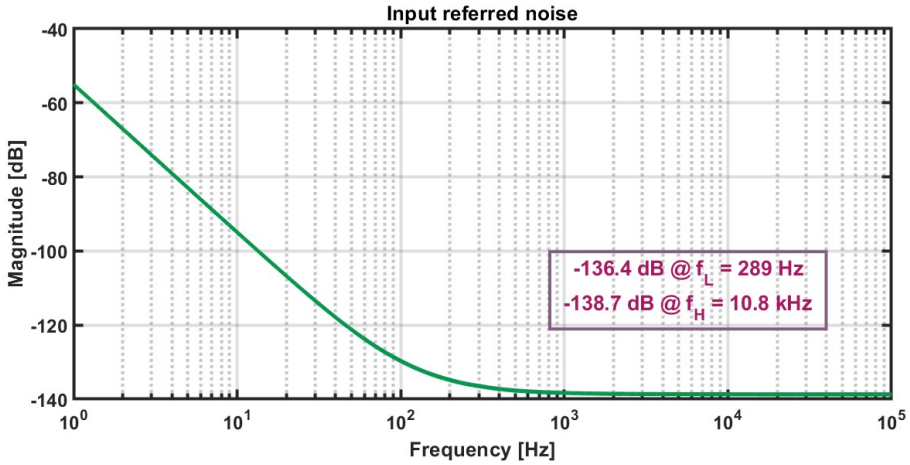


Figure 42: Simulated input-referred noise voltage in dB.

5.5 Common Mode Rejection Ratio (CMRR) - Results

As anticipated in Chapter 3, a change in the input common-mode voltage causes a change in the output voltage. However, this property is undesirable and therefore should be contained.

In order to quantify the latter, the common-mode rejection ratio (CMRR), defined as the ratio of the differential-mode voltage gain to the common-mode voltage gain, is evaluated:

$$CMRR \equiv \left| \frac{A_{dm}}{A_{cm}} \right|. \tag{5.5.1}$$

The higher the $CMRR$, the better the rejection of a common-mode signal applied to the amplifier inputs.

Fig. 43 shows the result obtained, in which it is observed that the $CMRR$ reaches a maximum value of $58\,dB$ at the frequency of $2.5\,kHz$, which is in-band. The latter is considered a good result.

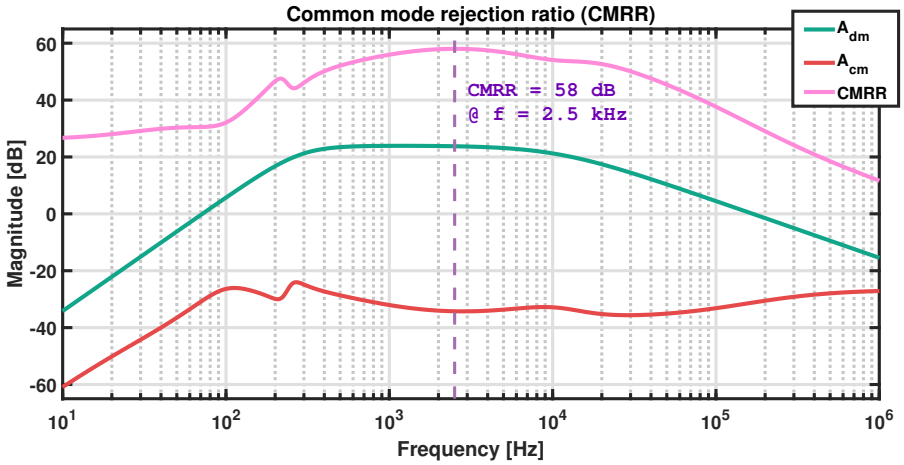


Figure 43: Simulated common-mode rejection ratio $CMRR$ frequency response.

5.6 Power Supply Rejection Ratio (PSRR) - Results

As anticipated in Chapter 3, ideally the output voltage of the amplifier should depend only on the differential mode input voltage and the common-mode input voltage. However, this is only the case if the supply voltage is constant. Otherwise, variations associated with the supply voltage could be reflected at the output. In fact, in order to ensure robust operation, it is essential that a circuit has great ability to reject variations associated with the supply voltage.

To quantify the circuit's ability to reject these variations, the $PSRR$ is introduced. The latter is defined as the ratio of the differential mode gain A_{dm} to the gain associated with the supply voltage A^+.

More precisely, the gain A^+ is defined as the ratio of the small-signal AC component of the differential output voltage v_o to the small-signal AC component of the positive supply v_{dd}, as shown in equation (5.6.1):

$$A^+ = \frac{v_o}{v_{dd}}\,. \tag{5.6.1}$$

Thus, the higher the PSRR, the better a circuit's ability to reject variations in supply voltage:

$$PSRR = \frac{A_{dm}}{A^{+}} \,. \tag{5.6.2}$$

The $PSRR$ was elaborated through a Monte Carlo simulation in CADENCE VIRTUOSO with 100 runs, which takes into account the mismatch. The graph obtained is shown in Fig. 44. A histogram around the frequency $f = 10^3\,Hz$ was then created, as shown in Fig. 45. From the latter, it is observed that at the frequency $f = 10^3\,Hz$, which is in-band, the average value of the $PSRR$ is $62\,dB$, demonstrating a good ability to reject variations in the supply voltage.

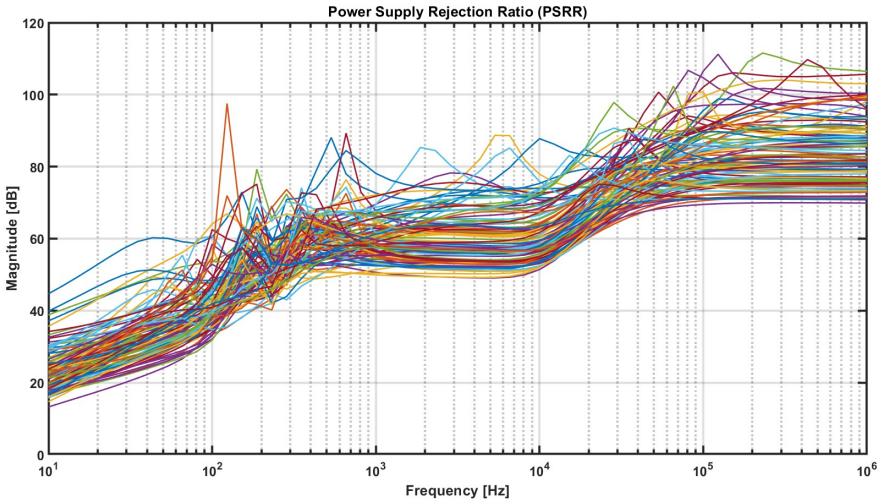


Figure 44: Simulated power-supply rejection ratio $PSRR$ of the amplifier, extracted from a Monte Carlo simulation with 100 runs.

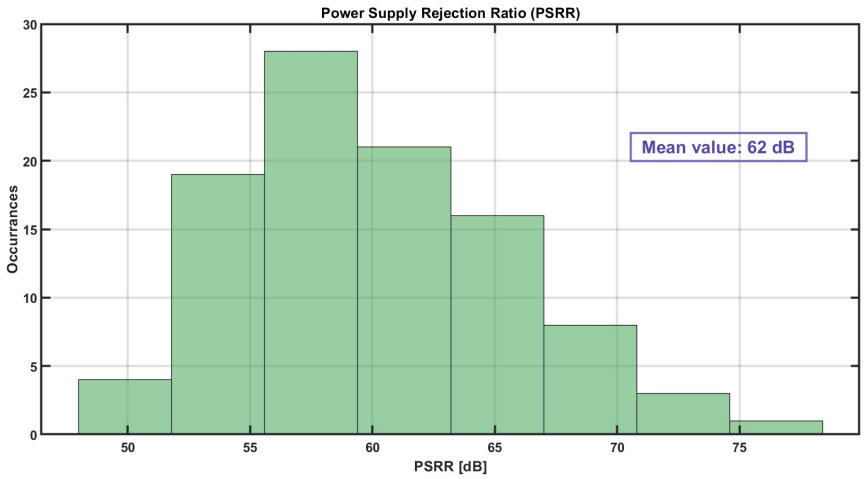


Figure 45: Histogram of the power-supply rejection ratio $PSRR$ of the amplifier, extracted from a Monte Carlo simulation with 100 runs.

6 Conclusions and Future Works

Reaching the conclusion of this thesis, a brief summary of the overall project will be provided and the salient aspects to be considered for possible future improvements will be highlighted.

This thesis project focused on the design and simulation of an integrated amplifier for processing ECG signals. The device, intended to be inserted into a subcutaneous implantable loop recorder (ILR), was designed to meet stringent specifications regarding power consumption and noise levels. The latter conditions motivate the decision to implement the CURRENT REUSE TECHNIQUE. The device, a THREE STACK INVERTER-BASED AMPLIFIER, was implemented in 130-nm CMOS technology.

Design and simulations were carried out in CADENCE VIRTUOSO, and plot computing was done using MATLAB.

The results obtained are summarized in Table 12.

Parameters	**Simulated results**
In-band differential-mode gain $\mathbf{A_{dm0}}$	23.9 dB
Low frequency pole $\mathbf{f_L}$	289 Hz
High frequency pole $\mathbf{f_H}$	10.8 kHz
High frequency zero $\mathbf{f_Z}$	15 MHz
Bandwidth **BW**	10.5 kHz
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_L})$	152 $nV/\sqrt{Hz}$
Input-referred noise voltage $\mathbf{v_{n,in}}$ $(\mathbf{f = f_H})$	116 $nV/\sqrt{Hz}$
Noise Efficiency Factor **NEF**	0.47
Power Efficiency Factor **PEF**	0.27
Common Mode Rejection Ratio **CMRR**	58 dB
Power Supply Rejection Ratio **PSRR**	62 dB

Table 12: Final results.

Possible future improvements predict:

- the design of a start-up circuit so as to ensure that the constant-Gm bias circuit always operates at a stable operating point, i.e., one in which all transistors are turned on;
- the design of a second amplification stage of higher gain, which is present in the device from which this thesis is inspired [1].

From the work that has been performed, is apparent the possibility of realizing an ECG signal acquisition system taking advantage of more scaled technologies than the 180 nm, in which the device in [1] was designed, so as to significantly reduce the area occupancy, while still ensuring that the specifications are fulfilled.

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