UNIVERSITY OF PADUA

Department of Information Engineering

Master's degree in Automation Engineering

MEASUREMENT-BASED MODELING OF A DC-DC CONVERTER FOR THE BILL OF MATERIAL PREDICTION

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Contents

Abstract

The thesis has been developed at 'Infineon Technologies Italia S.r.l.' in Padua, a leading company in the automotive market.

The topic of the project is the modeling of a DC-DC converter that allows to predict its behavior. The idea is to create a systematic methodology that reduces the amount of time, costs and complexity of the stability assessment for these type of devices. The proposed procedure has the purpose to be automated, fast, non-invasive, reliable and replicable. In this way the laboratory technicians can characterize the devices with a reduced effort and this can be very useful and productive. The basic idea is to exploit both a set of measures and a mathematical model. The mathematical model has to model only the well known part of the circuit, while the measures has the role to 'cover' the rest. In this way it is possible to predict the behavior of the DC-DC converter and in particular its stability to vary of the bill of of material.

The thesis has the main purpose of explaining a general procedure, replicable for different converters and for explaining that it is subdivided into two main chapters.

In Chapter 1 it is reported the theoretical background used for the project. In particular it is explained what is a DC-DC converter and how it is possible to establish its stability. The comparison between the actual methodology and the proposed one is here explained and well argued.

In Chapter 2 is instead reported a specific laboratory evaluation on an Infineon product. Here it is possible to see how to idea has been tested in a practice case. All the theoretical concepts of the first chapter is here evaluated in with a relevant effort in laboratory.

At the end, all the results and the possible improvements are reported in the chapter 'Conclusions'. Here it is visible the progress done exploiting the new 'hybrid' methodology in comparison to the actual procedures.

It is then present an 'Appendix' section, where it is possible to see some insights of the project.

Chapter 1

Innovative methodology for stability prediction of a DC-DC converter

1.1 Introduction

The aim of this thesis is to propose a new operating procedure that allows to predict the stability of a DC-DC converter, an important device in the power electronics field. All the theoretical ideas proposed are subsequently verified by means of laboratory analysis. In particular this project focuses on a particular device: a Buck converter. However it is worth to underline that the main aspect of the thesis is the innovative methodology of prediction and not the specific application that is reported. The smart goal of the project is in fact to explain a general idea that permits to avoid a relevant amount of measurements introducing as little error as possible. The procedure exploits a black-box approach in conjunction with a mathematical model, before explaining it, it worth to recap what a DC-DC converter is, with a particular focus on Buck, and how it is convenient to evaluate its stability.

1.2 DC-DC Converter power supply

A DC-DC converter is an electronic circuit that converts a source of DC voltage from a level to another. The input voltage is typically denoted by V_{in} or V_g, the output one instead is V_{out} or simply V. The role of converters is to produce a regulated voltage independently from the load present, and then they are used in portable electronic devices such as cellular phones, laptop computers and vehicles, which are supplied with power from batteries primarily. In fact such objects contain several sub-circuits, each with its own voltage level requirement different from that supplied by the battery or an external supply. Additionally, the battery voltage declines as its stored energy is drained. DC-DC converters offer a method to increase voltage from a partially lowered battery voltage thereby saving space instead of using multiple batteries to accomplish the same thing. They are preferred to transformers because the latter must be large and heavy for powers exceeding a few watts. This makes them expensive, and furthermore they are subject to energy losses due to their composition. Besides that the transformer works only for AC voltage, and so they are not usable for DC waveforms.

There are two types of converter: linear and switching. The latter converts one DC voltage level to another, which may be higher or lower, by storing the input energy temporarily and then releasing that energy to the output at a different voltage. The storage may be in either magnetic field storage components (inductors, transformers) or electric field storage components (capacitors). Switching conversion is often more power-efficient

(typical efficiency is 75% to 98%) than linear voltage regulation, which dissipates unwanted power as heat. For these reasons they are the most used in practice, even if the first is the simplest to be used.

Although they require few components, switching converters are electronically complex. Like all high-frequency circuits, their components must be carefully specified and physically arranged to achieve stable operation and to keep switching noise at acceptable levels.

The typical way to schematize a switching converter is the scheme in Figure 1.1, where, in addition to the main block that regulates the voltage level, there is a control block. It represents all the network necessary for commanding the switching elements present, that are typically transistors (MOSFET) or diodes. The controller needs to be fed by a reference and by some signals that depicts the current status. In the picture there is both a feedforward and a feedback path, but the first one is not present sometimes. The reference is instead the desired voltage level at which the converter aims, or typically a scaled version of it.

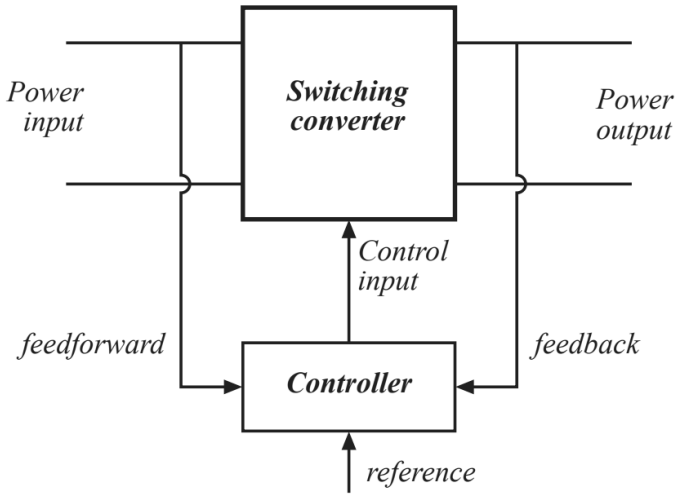


Fig. 1.1: Basic scheme of DC-DC converter

1.2.1 Types of Switching DC-DC Converter

There are three basic types of switching DC-DC converter: the buck, the boost and the buck-boost. The buck has the role of regulate the voltage to a lower level, i.e. $V_{out} < V_{in}$, and for this reason is also called step-down converter. The boost, vice versa, has the role of regulate the voltage to a higher level, i.e. $V_{out} > V_{in}$, and for this reason is also called step-up converter. The buck-boost is a mixture of the others two, in fact it can regulate to both lower and higher level. The basic schemes of these three types of converters are reported in Figure 1.2 (*Note*: this figure and some others have been taken from the book [3], where V_{in} is denoted with V_g and V_{out} with V, however in the images it is always pretty clear what each voltage reference represents). Here the switching part is represented for simplicity by a single ideal switch that selects two different circuit topologies and the load of the converter is represented by a resistor. As it can be noticed, the elements that

composed the three circuits are the same, but obviously, their different relative positions cause different behaviors. By the way, the common relation that describe their behaviour is the following:

$$V = M(D) \cdot V_g \tag{1.2.1}$$

where D is the duty cycle of the periodic signal after the switching action and $M(\cdot)$ is a function that varies for each type of converter. From what reported above the value that the value of $M(D)$ depends from each converter type in the following way:

$$M(D) \in \begin{cases} [0,1] & \text{for buck converter} \\ [1, +M_{max}] & \text{for boost converter} \\ [-M_{max}, 0] & \text{for buck-boost converter} \end{cases} \tag{1.2.2}$$

where M_{max} indicates the maximum value of voltage amplification that can be reached by the circuit.

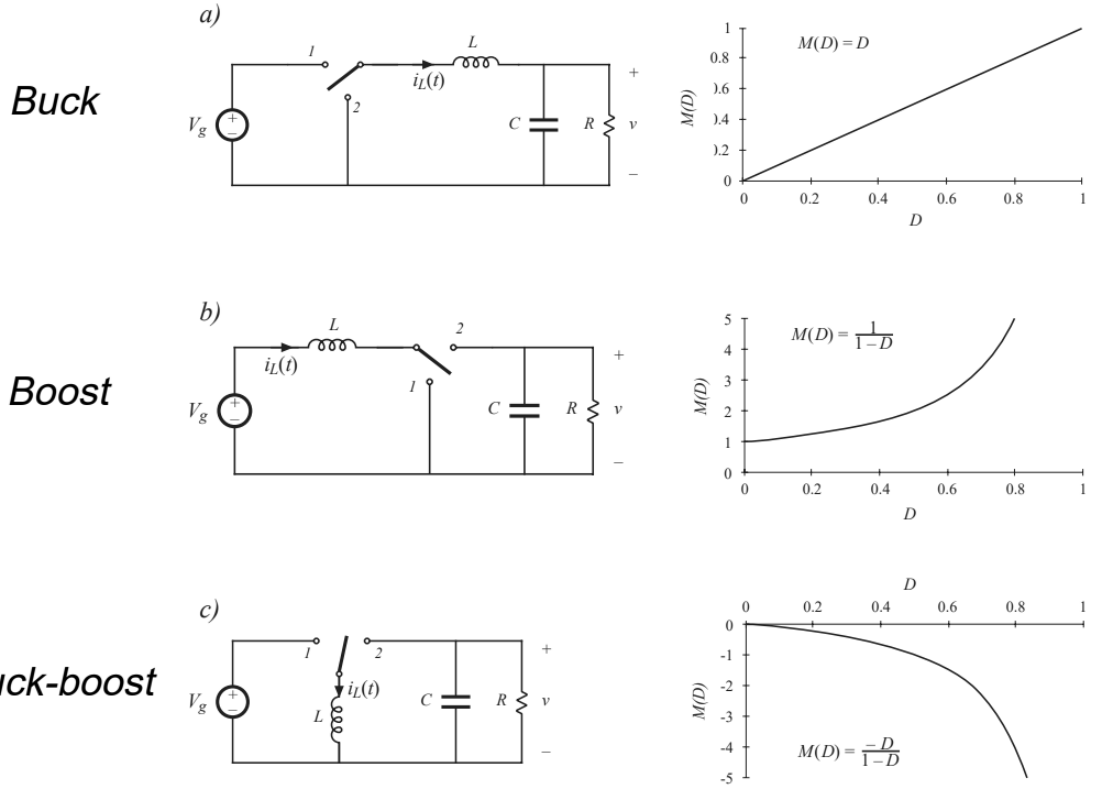
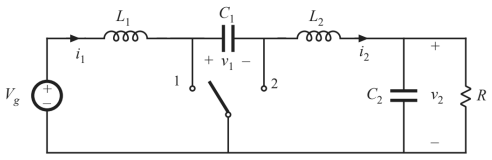


Fig. 1.2: Basic types of DC-DC converter.

It is also reported another type of converter, that differs from the previous three for the presence of more components. It is called Cuk and its circuit and its function $M(D)$ is reported in Figure 1.3, where it is possible to see that the behaviour is similar to the buck-boost.

Definitely for what regards the behaviour of the ideal switching converter at DC level it can be schematized as a simply transformer with a ratio of $M(D)$ like Figure 1.4. However, it is important to remember that this is only a intuitive scheme for understanding the basic behavior but the converters do not contain any transformer.

Cuk



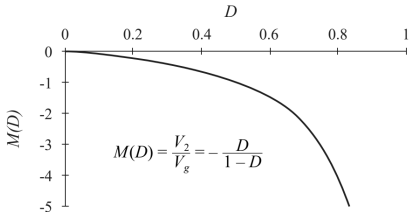


Fig. 1.3: Cuk converter.

The analysis could be more accurate inserting the equivalent series resistance (ESR) of the inductor and of the capacitor, i.e. the resistive value of the real components. This parasitic components will be taken into account in the calculation explained in the next chapter for a buck converter.

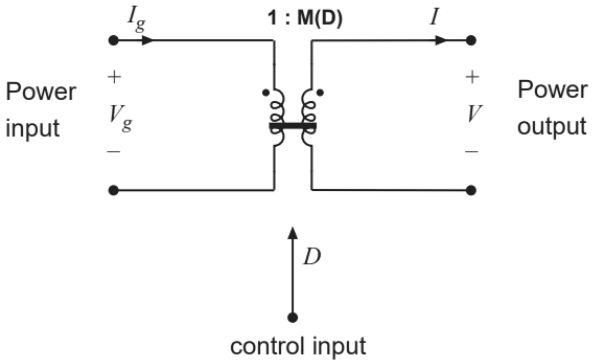


Fig. 1.4: DC model of ideal DC-DC converter

Buck Converter

- **Basic operation**

  Focusing on the Buck type, the basic operation are shown in the block diagram and in the timing charts reported in Figure 1.5 and 1.6 . The input DC voltage is converted to pulsed voltage with a switch. Its condition is controlled by a feedback loop circuit that it is explained in the following sections, at the moment it is important only to understand that its position selects two different topologies. The pulsed voltage is then transformed in the output DC voltage by the charging and discharging operation of the output LC filter. Let analyze the two different configurations of the network:

  – when the switch is in *position 1*, the current i_{L-1} flows through the inductor L and the power is delivered to the output capacitor C and the load, then the output voltage is increased.

  – If v reaches a certain high level, the switch is turned in *position 2* and the energy that was charged to L by the current i_{L-1} generates the current i_{L-2} and delivers the power to the load together with the energy that was charged to C, then output voltage is decreased.

  If the output reaches a certain low level, the switch is turned in *position 1* and it is increased again. The output voltage level is determined by the pulse duty ratio of

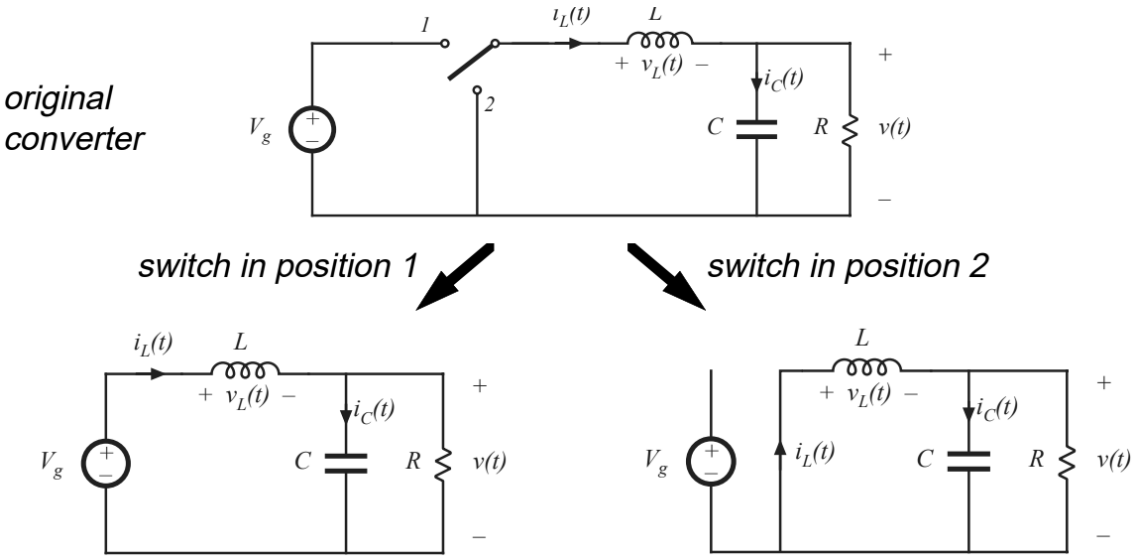


Fig. 1.5: Basic diagram of a generic buck.

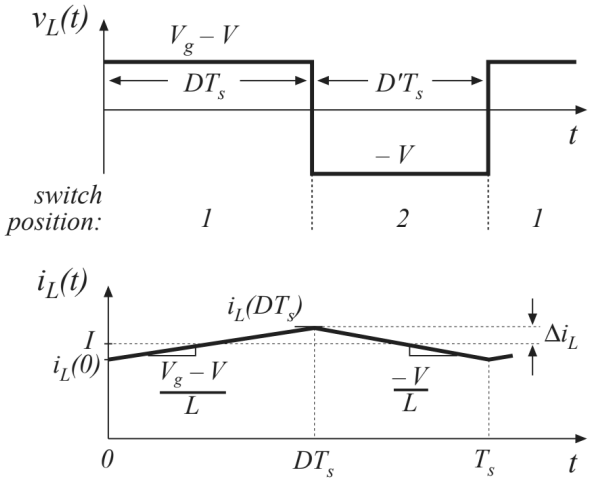


Fig. 1.6: Time chart of a generic buck.

the switch. The longer the period T_1, the higher the output voltage; the shorter the period T_1, the lower the output voltage. By repeating this on-off operation while monitoring the output voltage and adjusting the pulse duty ratio, the regulated output DC voltage is obtained regardless of the load variations. It is worth to notice that the current over the inductor (the union of i_{L-1} and i_{L-2}) never reaches the zero value. When this happens this way of working mode of the circuit is called Continuous Conduction Mode (CCM). Otherwise if the current saturates for some interval at the zero value it is said Discontinuous Conduction Mode (DCM). The slope of the inductor current and, consequently, the output voltage is easily calculated with an elementary analysis of the configurations of Figure 1.5. When

the circuit is in the first configuration it is:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(Vg - V) \\ \dfrac{dv}{dt} = \dfrac{1}{C}\left(i_L - \dfrac{V}{R}\right) \end{cases} \tag{1.2.3}$$

while it is in the second configuration:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{-V}{L} \\ \dfrac{dv}{dt} = \dfrac{1}{C}\left(\dfrac{V}{R} - i_L\right) \end{cases} \tag{1.2.4}$$

The presence of a LC filter allows to remove switching harmonics and as a rule of thumbs its cutoff frequency must be chosen much smaller than the switching one.

- **Derivation of DC steady state equations of converters**

To derive the DC steady state equations of the converters there are introduced two principles. The first one is the 'principle of inductor volt-second balance', which states that the average inductor voltage over one switching period is equal to zero in steady state. In fact, when the buck is in an equilibrium point of work it is necessary that the net change in inductor current is zero over every switching period, and from the definition:

$$v_L(t) = L\frac{di_L(t)}{dt}, \tag{1.2.5}$$

it is immediate to derive that also $\langle v_L \rangle = 0$. The symbol $\langle \cdot \rangle$ represents the mean value over a switching period.

In similar way it is obtainable also the 'principle of capacitor amp-second balance', which states that the average capacitor current over one period is zero in steady state, i.e. $\langle i_C \rangle = 0$.

Exploiting these two principles it is easy to derive the DC steady state point of work of the converters. Here it is reported the ones of the buck type. Starting from the principle relative to the inductor and from the circuit equations 1.2.3 1.2.4, it results:

$$\langle v_L \rangle = 0 = \frac{1}{T_S}\int_0^{T_S} v_L(t) = \frac{1}{T_S}\left[(Vg - V)DT_S - VD'T_S\right] \tag{1.2.6}$$

where it has been defined $D' = 1 - D$, with D indicate the duty cycle of the switching waveform. With some manipulation it results that the output voltage in steady state is:

$$V = DV_g \tag{1.2.7}$$

This relation states that the output voltage V is given by the input voltage V_g multiplied by the duty cycle D of the switch, as it was already sentenced in a quick

first analysis (equations 1.2.1 and 1.2.2). Similarly it holds:

$$\langle i_c \rangle = 0 = \frac{1}{T_S}\int_0^{T_S} i_C(t) = \frac{1}{T_S}\left[(I_L - V/R)DT_S + (V/R - I_L)D'T_S\right] \tag{1.2.8}$$

and it brings to the steady state value of the inductor current:

$$I_L = \frac{V}{R} = \frac{DV_g}{R}. \tag{1.2.9}$$

- **How to command the switches**

  After understanding the basic operation it is worth to explain how typically the switch elements are commanded. It is important because, as already said, the frequency at which this elements changes position affects directly the value of the output voltage. To describe clearly how this happens it is reported a typical diagram in Figure 1.7. The idea is to create a path that reports the current value of the output voltage, typically in a scaled version, and compares it with a reference (v_{ref} in the picture). This is the classic concept of negative feedback that is the basis of systems theory. The voltage reference is generated by an internal circuit, which guarantees an almost perfectly constant value independent from the rest of the network and from temperature changes. The resulting signal, that represents an error signal, is converted in the desired pulse signal by a pulse width modulator (PWM). The aim of this block is to regulate the value of the duty cycle according to the needs. In particular, when the output voltage is too low the duty cycle has to increase, and vice versa when the output voltage is too high the duty cycle has to decrease. This is the basic idea of the switching conversion: when the output is too low the circuit is forced to be in the configuration 1 of Figure 1.5, so that the output tries to reach the voltage input and so it increase; instead when the output is too high the circuit is forced to be in the configuration 2, so the output tries to discharge itself and so it decrease. Increasing the duty cycle means to prefer the configuration 1, while decreasing the duty cycle means to prefer the configuration 2. For this purpose, a common way to regulate the duty cycle, is to compare the error signal with a periodic sawtooth waveform; the output will be at high level if the error is higher then the sawtooth, otherwise it will be on a low level (see Figure 1.8). The compensator block, indicated with $G_c(s)$, adjusts the gain and phase delay of the error amplifier to improve the feedback loop stability. This topic is well explained in the following sections.

1.3 Small signal analysis

There are different aspects that can perturb the desired steady state value of the output. In particular there may be mainly disturbances in the input voltage or in the load. The load is typically considered like a resistive element, this choice is acceptable if the real load application is a processing unit because it can be seen like a resistor that varies instantly its

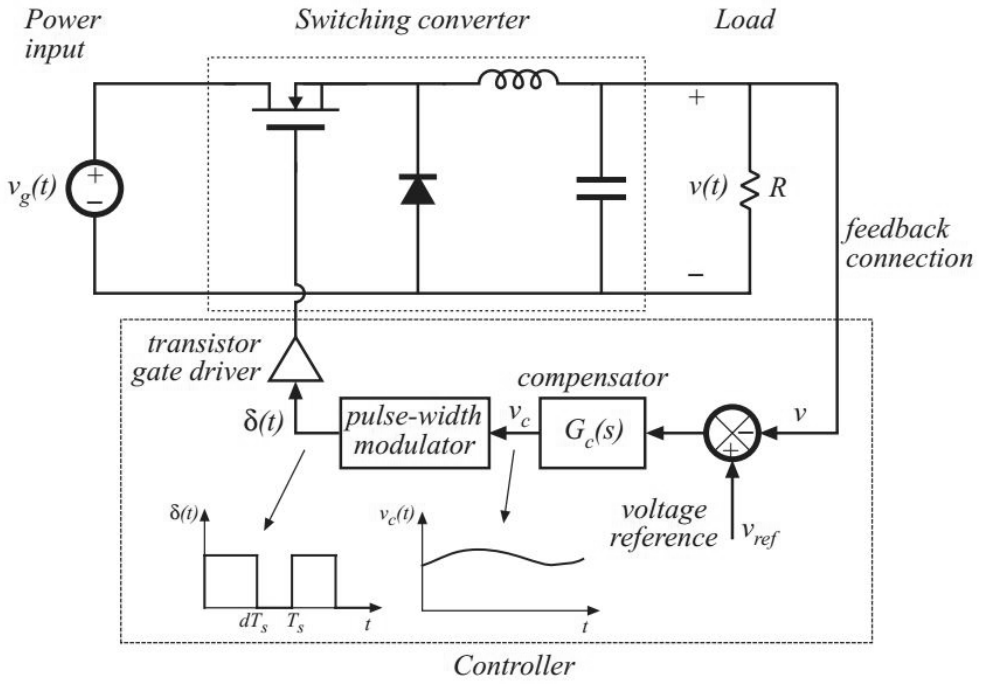


Fig. 1.7: Diagram of generic buck with feedback action.

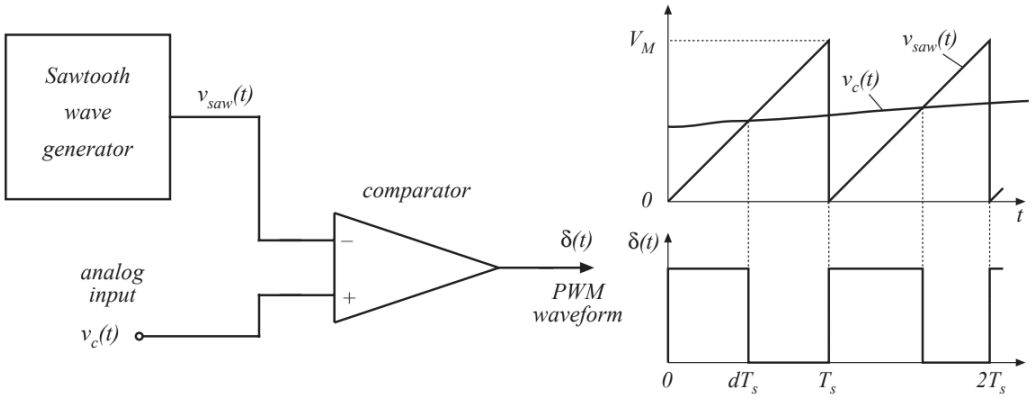


Fig. 1.8: PWM block scheme and its time chart.

value, but obviously it is an approximation. Also the value of the BOM (Bill of Material) elements can be affected by some uncertainties and so it is important to study how these aspects affect the output voltage. At this purpose it is useful to build an AC model, in order to predict how low-frequency variations of duty cycle induce low-frequency variations in the converter voltage and currents. For this purpose, in the following explanation it will be neglected the small switching ripples on the waveforms. A typical strategy commonly used for cancel the effect of switching ripples in the inductor current and capacitor voltage waveforms, is averaging the equations over one switching period. Hence the low-frequency components of the inductor and capacitor waveforms are modeled by equations of the form:

$$\begin{cases} L\dfrac{d\langle i_L(t)\rangle}{dt} = \langle v_L(t)\rangle \\ C\dfrac{d\langle v_C(t)\rangle}{dt} = \langle i_C(t)\rangle \end{cases} \tag{1.3.1}$$

where $\langle\cdot\rangle = \frac{1}{Ts}\int_t^{t+T_s}\cdot d\tau$, that allows to neglect the high-frequency switching ripple keeping the low-frequency ones.

In general the equations 1.3.1 of a converter present nonlinear terms, and so a standard strategy is to linearize the mathematical model about a quiescent operating point. The idea is to consider the circuit response at some small variations of the physical quantities with respect to the DC value. For this reason the model obtained from this procedure is called *small-signal model*.

For better understanding it is now reported the buck converter case. The equations that explain the DC behavior of a buck are replaced with the AC version, merging the two configuration of the switcher to have the time evolution over one complete period:

$$\begin{cases} L\dfrac{\langle i_L(t)\rangle}{dt} = d(t)\big[\langle v_g(t)\rangle - \langle v(t)\rangle\big] - d'(t)\langle v(t)\rangle \\ C\dfrac{\langle v(t)\rangle}{dt} = d(t)\big[\langle i_L(t)\rangle - \langle v(t)\rangle/R\big] + d'(t)\big[\langle v(t)\rangle/R - \langle i_L(t)\rangle\big] \end{cases} \tag{1.3.2}$$

where $d(t)$ represent the time evolution of the duty cycle. In addition it is important to understand how the current delivered by the voltage generator varies in the time. A simple network analysis gives this relation:

$$\langle i_g(t)\rangle = d(t)\langle i_L(t)\rangle \tag{1.3.3}$$

From these relations it is possible to construct the small variations model at a quiescent point (V,I_L). At this aim it is assumed that the input voltage $v_g(t)$ and the duty cycle $d(t)$ are equal to some given quiescent values V_g and D, plus some superimposed small ac variation.

$$\begin{aligned} \langle v_g(t)\rangle &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \tag{1.3.4}$$

In response of these inputs, and after some transient have subsided, the averaged inductor current, the averaged capacitor voltage and the averaged input current waveforms will have the same structure:

$$\begin{aligned} \langle i_L(t)\rangle &= I + \hat{i}_L(t) \\ \langle v(t)\rangle &= V + \hat{v}(t) \\ \langle i_g(t)\rangle &= I_g + \hat{i}_g(t) \end{aligned} \tag{1.3.5}$$

Note: the assumption adopted is that $|\hat{x}(t)| \ll |X|$, where the letter x has been used for generalizing the concept to all the waveforms. This is the small-signal assumption.

For the inductor equation, it is:

$$L\frac{d(I_L + \hat{i}_L(t))}{dt} = [D + \hat{d}(t)]\cdot[V_g + \hat{v}_g(t) - V(t) - \hat{v}(t)] - [D' - \hat{d}(t)]\cdot[V + \hat{v}(t)] \tag{1.3.6}$$

By doing some calculations on this equation is possible to obtain a relation that contains three types of terms: the DC term, the 1^{st} order AC term and the 2^{nd} order AC one. Exploiting the assumption of dealing with small variations the 2^{nd} order AC term can be neglected. Furthermore, by definition, the DC terms simplify each others in the steady

state, so it remains only the 1^{st} order AC term. It is:

$$L\frac{d\hat{i}_L(t)}{dt} = \hat{d}(t)V_g + D[\hat{v}_g(t) - \hat{v}(t)] - D'\hat{v}(t) \tag{1.3.7}$$

This is the desired result: the small-signal linearized equation that describes variations in the inductor current.

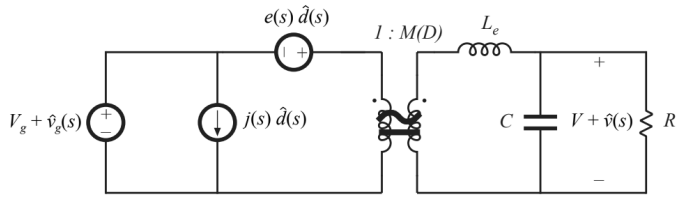
Similarly the other two small-signal equations can be obtained:

$$C\frac{d\hat{v}(t)}{dt} = D[\hat{i}_L(t) - \hat{v}(t)/R] + D'[\hat{v}(t)/R - \hat{i}_L(t)] \tag{1.3.8}$$

and

$$\hat{i}_g(t) = I_g\hat{d}(t) + D\hat{i}(t). \tag{1.3.9}$$

Referring to the book [3] it is also possible to obtain a general approach for all the previous mentioned DC DC converters, see Figure 1.9, where a canonical scheme is reported. In this case it is described the basic properties shared by the standard DC-DC PWM converter operating in continuous conduction mode. The core of the model is the ideal M(D) transformer, already introduced, to represent the basic DC-DC conversion function, and generalized here to include AC variations. The converter reactive elements introduce an effective low-pass filter into the network. The model also includes independent sources which represent the effect of duty cycle variations. The parameter values in the canonical models of several basic converters are tabulated in the figure for easy reference.



Converter	*M(D)*	L_e	*e(s)*	*j(s)*
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1-\frac{s\,L}{D'^2\,R}\right)$	$\frac{V}{D'^2\,R}$
Buck-boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D^2}\left(1-\frac{s\,DL}{D'^2\,R}\right)$	$-\frac{V}{D'^2\,R}$

Fig. 1.9: Block diagram for small variation of three standard converters.

- **Modeling PWM block**

  It is necessary to modeling also the small-signal behavior of the PWM block in the same way. The equation that regulates the time evolution is:

$$d(t) = \frac{v_C(t)}{V_M} \quad \text{for} \quad 0 < v_C(t) < V_M \tag{1.3.10}$$

This time chart is visible in Figure 1.8. The linearized and perturbed equation results:

$$D + \hat{d}(t) = \frac{V_C + \hat{v}_C(t)}{V_M} \quad \text{for} \quad 0 < v_C(t) < V_M \tag{1.3.11}$$

It is then easy to see that the AC component of this relation is simply given by $\frac{1}{V_M}$. Futhermore it is worth to notice that the input voltage is a continuous function of time, but there can be only discrete value of the duty cycle for each switching period. Therefore, the PWM samples the control waveform, with sampling rate equal to the switching frequency. In practice, this limits the useful frequencies of AC variations to values much less than switching frequencies. Control system bandwidth must be sufficiently less than Nyquist rate $f_S/2$. The small-signal scheme results to be the one reported in Figure 1.10

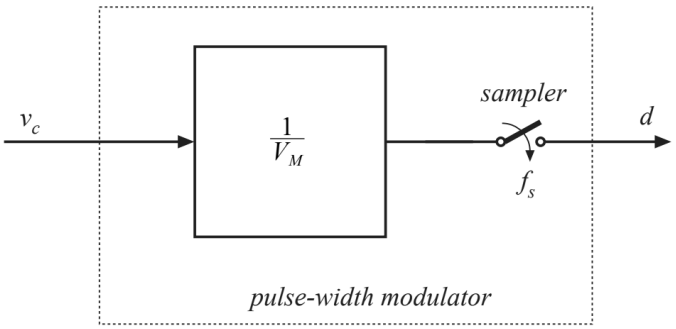


Fig. 1.10: Block diagram for small-signal of PWM block.

- **Transfer Functions**

Starting from the perturbed equations obtained in the previous section that described the small-signal behavior and taking their Laplace transformations it is possible to derive the more practical transfer functions. The inputs of the system are the duty cycle variation $\hat{d}(s)$ and the input voltage variation $\hat{v}_g(s)$. Furthermore the output voltage depends on the load current variations, i.e. on the current that flows on the load (considered simply a resistor like already explained). Hence, the AC output voltage variations can be expressed as the superposition of the terms arising from these waveforms:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) - Z_{out}(s)\hat{i}_{load}(s) \tag{1.3.12}$$

where $G_{vd}(s)$ is the so called control-to-output transfer function and $G_{vg}(s)$ is the line-to output one. In Figure 1.11 is possible to see the three different standard converters transfer functions, that have been derived in standard form. $Z_{out}(s)$ is instead the output impedance that it is reported in Figure 1.12 for the ideal case.

The study of the overall scheme must take into account also the feedback path, comprising the compensation and the pulse-width modulator, like exposed in Figure 1.13.

$$G_{vd}(s) = G_{d0}\frac{\left(1-\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right)} \qquad G_{vg}(s) = G_{g0}\frac{1}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2}$$

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
boost	$\frac{1}{D'}$	$\frac{V}{D'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{L}$
buck-boost	$-\frac{D}{D'}$	$\frac{V}{D\,D'^2}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2\,R}{D\,L}$

Fig. 1.11: Transfer Functions of the three standard converters

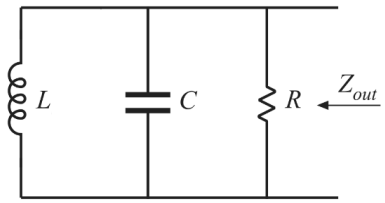


Fig. 1.12: Scheme of ideal output impedance $Z_{out}(s)$.

Incorporating all the component into schematic blocks the scheme becomes like the Figure 1.14, where it is possible to see the chain of the transfer functions. Resolving this block diagram it is possible to obtain the complete equation that rules the output voltage variations, i.e. the closed loop transfer functions (for convenience the Laplace variable s is tacit here):

$$\begin{aligned}\hat{v} &= \hat{v}_{ref}\cdot\frac{G_cG_{vd}/V_M}{1+HG_cG_{vd}/V_M}+\hat{v}_g\cdot\frac{G_{vg}}{1+HG_cG_{vd}/V_M}-\hat{i}_{load}\cdot\frac{Z_{out}}{1+HG_cG_{vd}/V_M}\\ &= \hat{v}_{ref}\cdot\frac{1}{H}\frac{T}{1+T}+\hat{v}_g\cdot\frac{G_{vg}}{1+T}-\hat{i}_{load}\cdot\frac{Z_{out}}{1+T}\end{aligned} \tag{1.3.13}$$

where it has been defined

$$T(s) = \frac{1}{V_M}H(s)G_c(s)G_{vd}(s) \quad := \textbf{Loop Gain} \tag{1.3.14}$$

The so called loop gain is equal to the products of the gains around the negative feedback loop. It is immediate to notice that this function appears in the denominators of each transfer function present in equation 1.3.13. In such a way it reduces the effects of the input variations on the output voltage variations. In fact with the addition of the feedback path the open-loop original transfer functions are rearranged in the closed-loop versions like exposed in Table 1.1:

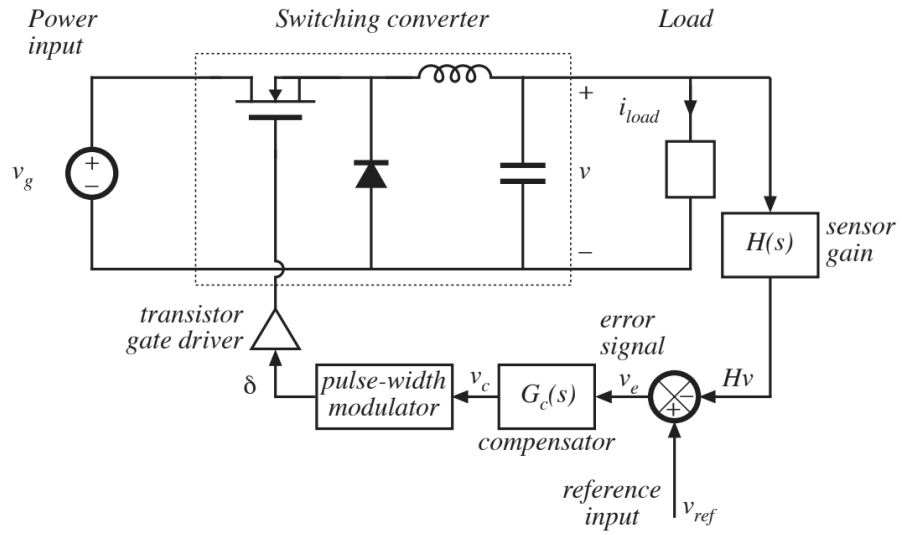


Fig. 1.13: Scheme of overall system with feedback path.

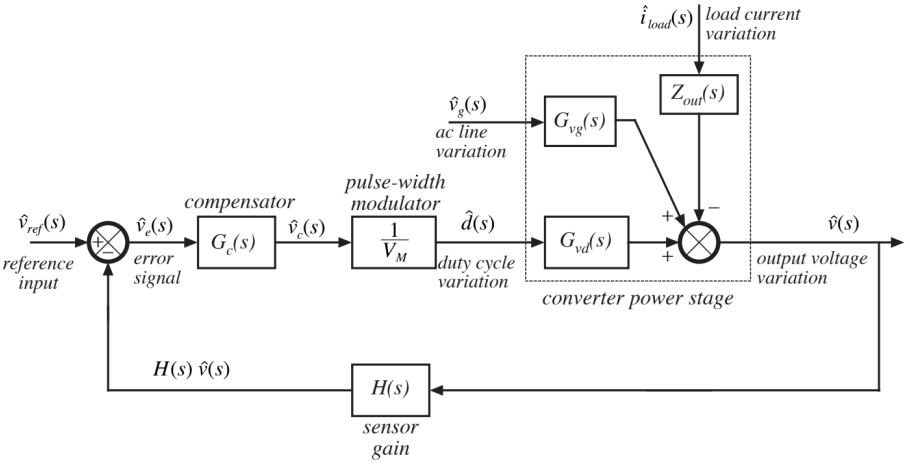


Fig. 1.14: Block diagram of overall system.

1.4 Stability Criterion and Compensation Network

Like already said the aim of the DC-DC converter is to maintain constant the value of the output voltage $v(t) = V$, regardless of disturbances in input voltage, load current or variations in component values. For this purpose the correct design of the negative feedback is fundamental. Like saw in the previous section the introduction of the feedback line modifies the transfer functions in such a way that when the magnitude of loop gain $T(s)$ is large the influence of disturbances on output voltage is small. A large loop gain also causes the output voltage to be nearly equal to $v_{ref}/H(s)$, with very little dependence on the gains in the forward path of the feedback loop. However, the introduction of a feedback loop can introduce problems on the stability of the system, so it is important to impose a good behavior of the final transfer functions. Feedback can in fact introduce oscillations, ringing, overshoot and other undesired behavior. A practical principle that gives a good assessment of the stability of a DC-DC is the phase margin criterion (see the appendix for a discussion of it). As a first idea, when the phase of the loop gain $T(s)$ at the so called

	Open-Loop T.F.	Closed-Loop T.F.
Control to Output	$G_{vd}(s)$	$\frac{1}{H(s)}\frac{T(s)}{1+T(s)}$
Line to Output	$G_{vg}(s)$	$\frac{G_{vg}(s)}{1+T(s)}$
Output Impedance	$Z_{out}(s)$	$\frac{Z_{out}(s)}{1+T(s)}$

Tab. 1.1: Open-loop and closed-loop transfer functions.

crossover frequency, is greater than $-180°$ the overall system results being stable. The gap between the phase and $-180°$ is exactly called phase margin. Moreover, there may be different level of stability, so it is possible to establish if the system transient response has a good behavior, with less overshot and ringing. In principle, it is designed a compensation network to attain adequate phase margin and so good rejection of expected disturbances. In particular, looking on the basic compensators well known, the lead compensators and the PD controllers (proportional and derivative) are used to improve the phase margin and extend the bandwidth of the feedback loop. Lag compensators and PI controllers (proportional and integrative) are used to increase the low-frequency loop gain, useful for reaching a very low steady state error. Obviously, more complicated compensator (PID) can achieve the advantages of both approaches. Let then see in details how the phase margin criterion works in this contest.

A possible practical way to establish the stability of a DC-DC converter is to obtain the phase margin of the loop gain $T(s)$. In fact this variable tells if the value $1 + T(s)$ contains right-half plane poles, i.e. the closed-loop transfer functions 1.3.13 are unstable.

In Figure 1.15 it is reported two typical examples of bode plot of the loop gain $T(s)$ of a converter. In the plot on the right the loop gain leads to a stable closed-loop system, the phase margin has in fact a quite positive value and then the above proposition holds. In the left plot instead the closed-loop system results to be unstable since the phase margin is negative.

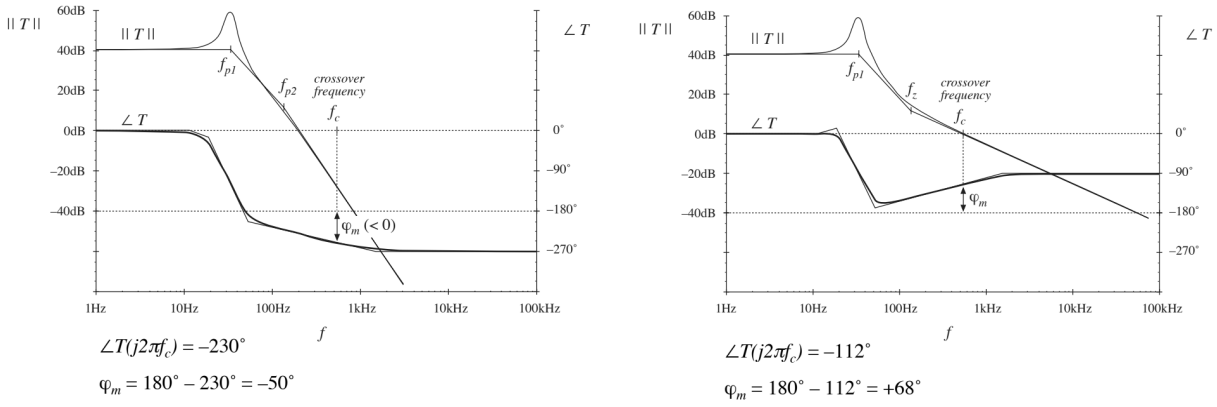


Fig. 1.15: Examples of loop gains of converters. Unstable system on the left and stable system on the right.

A positive phase margin but with a small value (let think about 0 or 15°) leads to a stable system having a transient response that presents large overshoot and ringing. It is

not acceptable and then it is important to design a good regulator that imposes a quite positive phase margin of $T(s)$ (about 40° or more).

On the other hand, if the crossover frequency becomes low as a result of excessive feedback compensation, the response speed to the load variations will be slower. Therefore, it is necessary to design the feedback compensation circuits so that the stability and the response speed are optimized for the requirements of targeted applications. In fact, like showed in Figure 1.15, the behavior of converter loop gain present a large magnitude at low frequency, but as the frequency of the variations increases, the loop gain decreases and as the loop gain becomes lower than 1, the regulation will not work. Substantially, the higher the crossover frequency is, the faster is the response to load variations.

The idea is to add some zeros and some poles in the loop chain, being careful to the frequencies at which they appear. This allows to modify as you like the bandwidth and the phase of the loop gain. For clearness it is reported a simple example taken from the book [3].

- **Example**: The loop gain before the compensation (denoted with $T_u(s)$) is reported in the Figure 1.16.

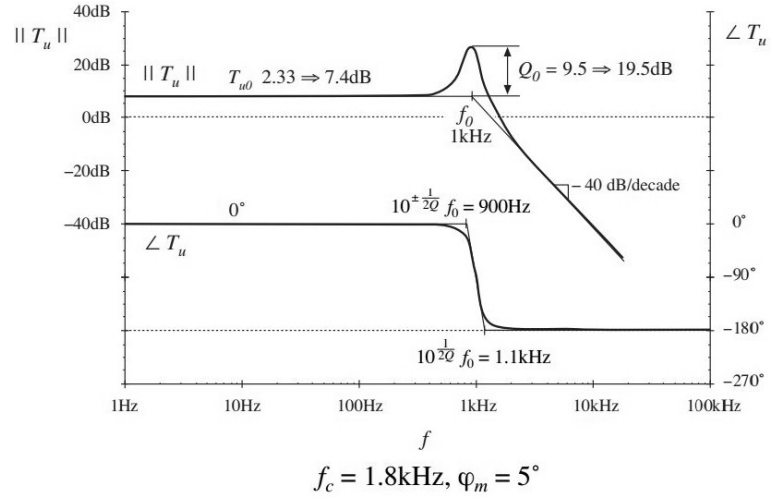


Fig. 1.16: Example of uncompensated loop gain.

The crossover frequency is equal to 1.8kHz, while the phase margin is only 5°, that is a positive value but almost zero. The aim is then to increase the latter to a more reassuring value (in particular the desired phase margin is $\varphi^* = 52°$). In this example it is required to increase also the bandwidth ($f_C^* = 5$kHz). Given this evolution of $T_u(s)$ a good choice for the compensation is the so called lead compensator, which is none other that a PD compensator. $T_u(s)$ has a magnitude of -20.6dB at f_C^*, so definitely the compensator must have a phase of $+52°$ and a magnitude of $+20.6$dB at f_C^*. A typical way to obtain the frequency of the pole and zero of a lead compensator is the following:

$$\begin{cases} f_z = f_C^* \cdot \sqrt{\frac{1 \pm \sin\theta^*}{1+\sin\theta^*}} \\ f_p = f_C^* \cdot \sqrt{\frac{1+\sin\theta^*}{1 \pm \sin\theta^*}} \end{cases} \tag{1.4.1}$$

where $\theta = \angle G_C(f_C)$. For the example this equations bring to $f_z = 1.7$kHz and

$f_p = 14.5$kHz. For what regards the DC gain of the compensator it holds:

$$G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} \tag{1.4.2}$$

where f_0 is the resonant frequency of $T(s)$ and T_{u0} its dc gain. This brings to $G_{c0} = 11.3$dB.

The Bode diagram of the compensator $G_c(s)$ is reported in Figure 1.17, where it is possible to see the position of the pole and zero frequencies. The zero anticipates the pole allowing to increase the phase. The distances between f_P and f_Z regulates the amount of this increment. In Figure 1.18 it is possible to see the effects of the compensation on the loop gain, i.e. $T(s) = T_u(s) \cdot G_c(s)$. The phase margin is now enough positive to guarantee a good behavior of the overall system and at the same time the bandwidth of the system is the desired one.

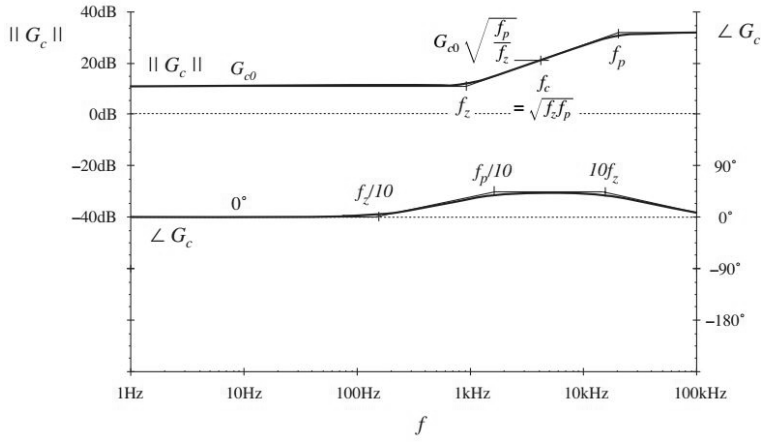


Fig. 1.17: Example of lead compensator.

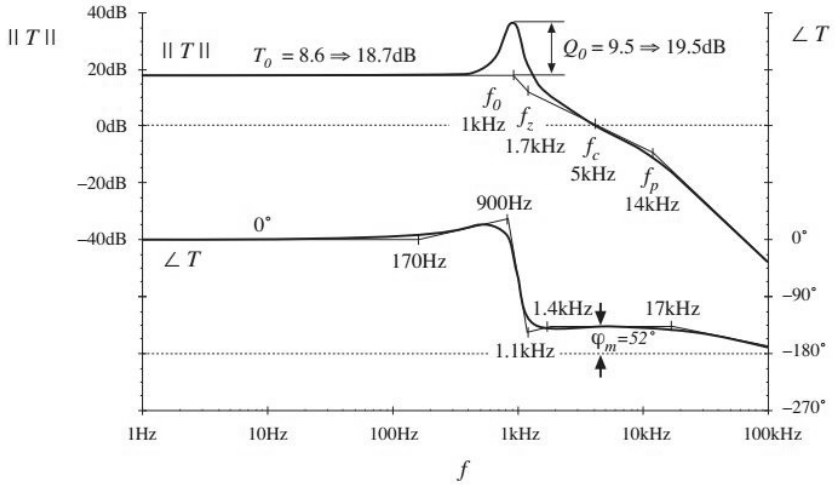


Fig. 1.18: Example of loop gain after lead compensation.

The lead compensator of this example can be improved by adding an integral part that introduces a low frequency pole. The results obtainable from a compensator of this type

are reported in Figure 1.19. Here it is possible to see the compensated loop gain $T(s)$ and the value $1/(1+T(s))$ which is the characterizing element of the closed-loop transfer functions.

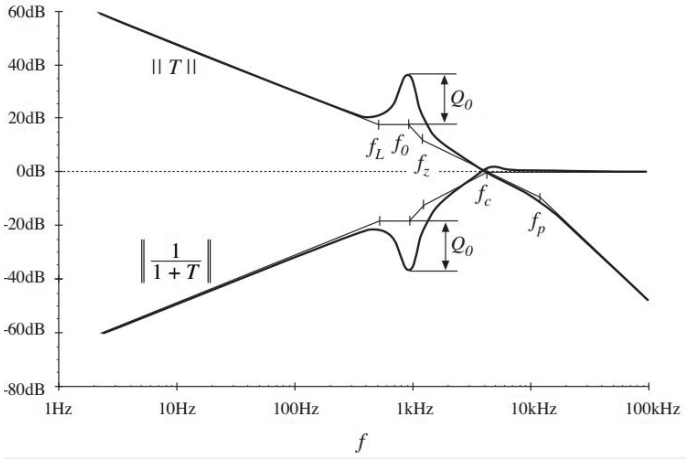


Fig. 1.19: Example of loop gain after PID compensation.

1.5 DC-DC Integrated Circuit description

An important aspect that must be highlighted is that on the market there are different types of integrated converters. This circuits, in fact, are packed into small chips that can then be installed in the phones, in the laptops or in the cars. This chip can be designed in different configurations and the main difference lies in which part of the network is inside the integrated circuit and which is not. Here are reported some application schemes provided by Infineon Technologies, leading company in the automotive world. In Figure 1.20 it is possible to see an integrated circuit that substantially contains only the control blocks that coordinate the overall system. Compensation network, switching MOSFETs and voltage divider are instead external. This means that these components must be inserted by the costumer.

In Figure 1.21 instead it is possible to see another chip that presents an internal MOSFET. The other switching component is in this case a diode and inductor, capacitor and resistor divider are external. There exist also other configurations in which some other parts of the circuit are integrated. A typical case is when the chip is built in 'fixed' configuration. It means that the feedback path present a fixed voltage divider into the chip, and then the output voltage value is imposed by the dealer. This differs from the two reported figures where the user can decide at which voltage level the device should work. In this case the device is called 'adjustable'.

Note: in the laboratory evaluation made in this thesis it has been used the circuit in Figure 1.20, like explained in the next Chapter.

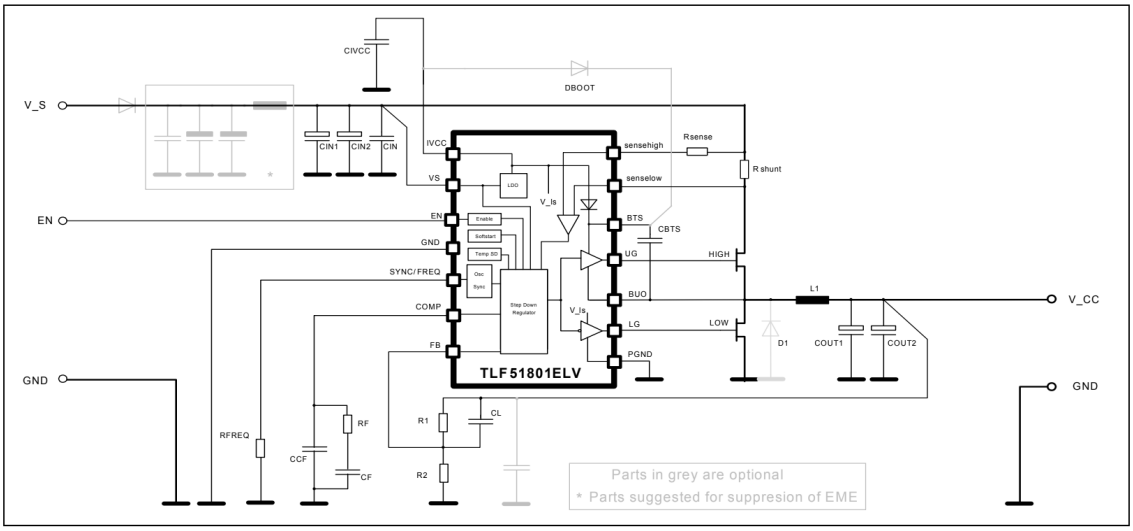


Fig. 1.20: Block diagram of an Infineon product TLF51801ELV.

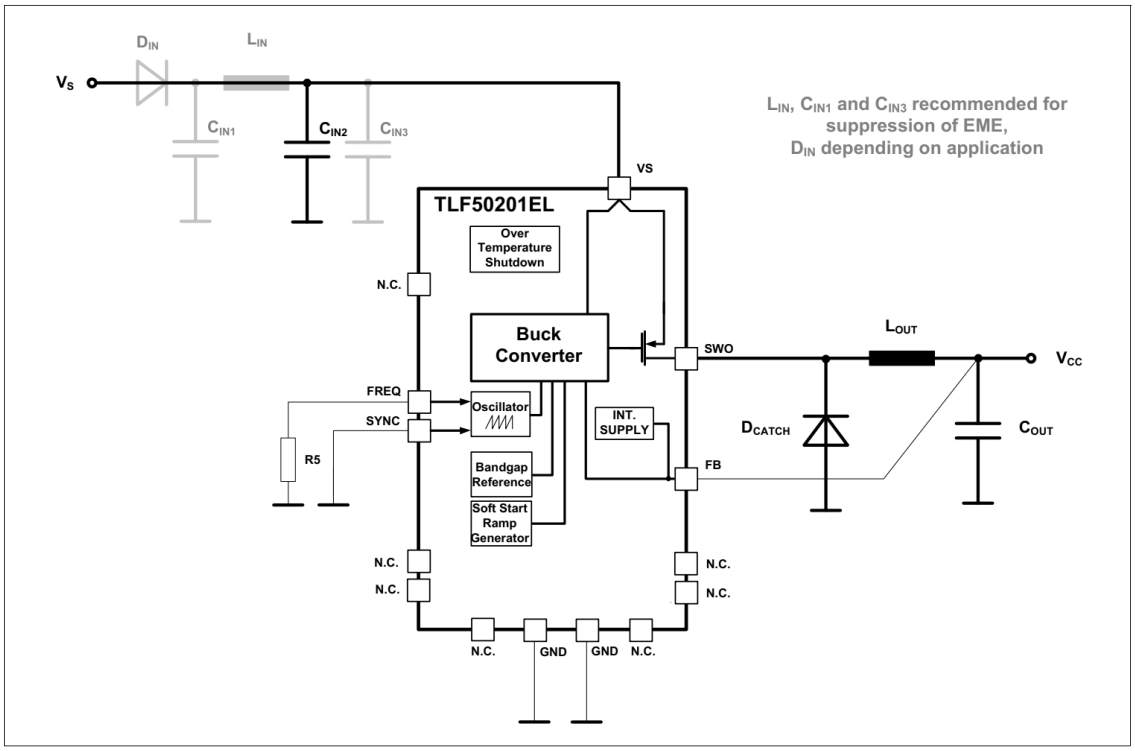


Fig. 1.21: Block diagram of an Infineon product TLF50201EL.

1.6 Stability Assessment of DC-DC integrated circuit - State of Art

1.6.1 Mathematical model

The small-signal modeling of the DC-DC converter obtained previously can be exploited for evaluation of the stability like reported in the easy example of section 'Stability Criterion and Compensation Network'. With a mathematical model, developed for example in Matlab environment, it is possible to change the value of the components with simply

changing the value of each programming variable. In this way one can obtain the value of the phase margin at every point of work and for every desired value of LC-filter.

- **Limits of mathematical model**

  The drawbacks of using a mathematical model are different. The first one is the complicated studies that are necessary for obtaining a well-tuned model. The real electrical components in fact present different behavior from the ideal one, for example at frequency variations. Furthermore, the value of the components are always different from the nominal ones, so one can not simply rely on the declared value but should make some measurements. Another important problem is that the model is derived for small signal, in the sense that the variations of the waveforms are smaller in respect of respect to the DC point, and this is not always verified in practice. It is possible in fact to have a large signal change of the overall system when a single component is changed. The switching DC-DC converter have a non-linear behavior when they are used in large signal context. Lastly, like explained in the section 1.5, the commercial products present different topologies and sometimes some networks are integrated in the chip. Some internal nodes are typically not available and so he can not analyze the physical behavior for building the model.

1.6.2 Load step test

The current methodology used in practice to test the loop stability is the so called 'load step', or equivalently 'load transient'. It is a quick way to assess power converter behavior on several aspects. Beside the stability check, in fact, it checks the converter regulation speed, the input supply stability, slope compensation issues and layout problems. The idea of the load step test is to simulate a very quick and relevant load variation. This is useful because it replicates the microcontroller behavior. The current i_{load} that flows on the resistive load is forced to perform a certain variation that is a good percentage of the maximum value reachable. This implies that the response of the converter is not well described by the AC small signal analysis, because the hypothesis that the variations of the waveforms are small is not verified. The test of stability consists so in measure the output voltage response. If it presents a smooth evolution without ringing or excessive overshoot the system is considered stable, otherwise there are some issues. It is possible to construct a relationship between the voltage response and the phase margin, like reported in the example of Figure 1.22. This figure has been taken from an application paper [5]. The mathematical theory behind this relation is not so easy, in the appendix it is reported for the case of system that can be approximated with a second order transfer function, like in converter case.

- **Limits of load step test**

  The procedure just explained presents some limits. The main one is the amount of possible operations needed for a good evaluation. The converter may in fact seem to be quite stable under some configuration conditions, but results unstable under other ones. Then the laboratory technicians have to take a lot of measurements to

test in a exhaustive way the product. Lets, for example, think that the requirements of a validation test need to have an output voltage response for n different final load currents, each for m different input voltages. The measurements needed are then $m \times n$. If it is now requested to verify the stability of these $m \times n$ points of work for different values of of the LC-filter it is easy to understand that the number of measurements grows rapidly. If it is required to change p times the value of the capacitor and q times the value of the inductor, the total effort is $m \times n \times p \times q$ measurements. It is worth to notice that, if the change of the m values of the input voltage requires a small effort (it is sufficient to change the value of the input supply), the others $n \times p \times q$ measurements requires a big effort. It is in fact necessary to change the electrical components present on the board. It is therefore required to remove the old components and solder the desired ones.

Another limit of this procedure is that, even if the test regards a large-signal analysis, the sizing of the components are executed with a small-signal analysis. This means that is not possible to discern the two different types of analysis. This can brings to a not correct conclusions.

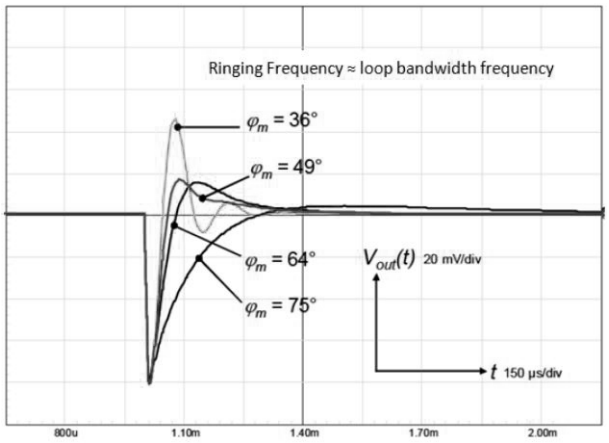


Fig. 1.22: Example of load step response and phase margin comparison for a second order system.

1.7 Stability Prediction of DC-DC integrated circuit - New Methodology

As anticipated, the purpose of the methodology proposed is to reduce substantially the amount of measurements required for a complete assessment of the stability of a DC-DC converter. Like said, the current practical method of load steps test can request a lot of measurements for a wide range analysis of the converter. Furthermore, even making a lot of measures the results are discrete, in the sense that the points evaluated are precise and if it is needed to test the circuit in a new point, all the procedure must be done again. This is not acceptable and so this project try to remedy this issue.

The idea is to treat the converter like a composition of two blocks, a block that represents the well known part of the circuit and a block that contains the rest. In particular

the latter contains all what is included into the integrated chip and the parts that can undergo changes based on user needs. This is the black box approach that allows to make the analysis independently from the tested device. This is the key point of the thesis.

Refreshing the small-signal model of DC-DC converter in Figure 1.23, it is possible to notice which part is suggested to consider either known (in green) or unknown (red). The

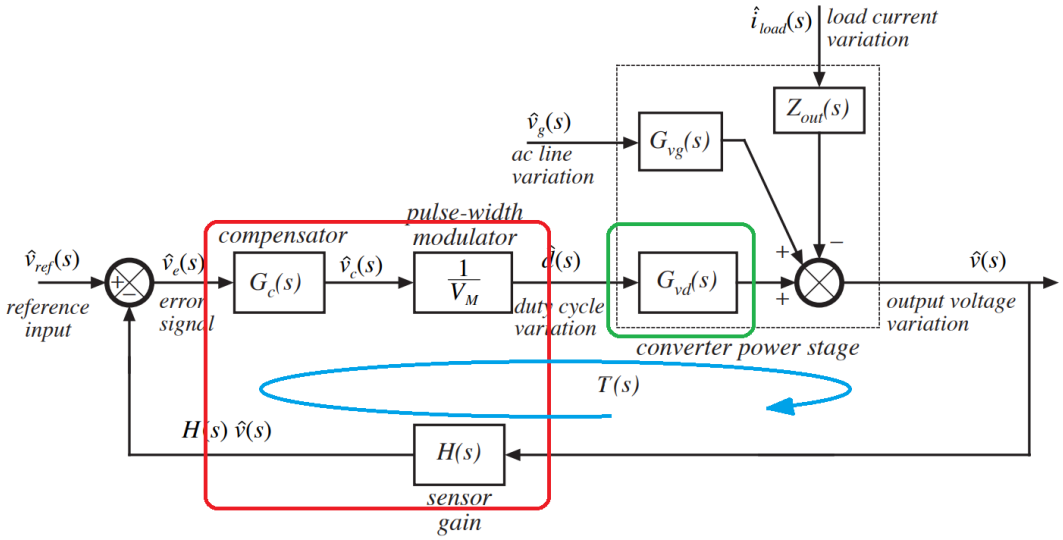


Fig. 1.23: Converter transfer functions: in green the known part, in red the unknown one, in blue the loop gain.

phase margin is obtained from the loop gain that is marked with the blue arrow. It is in fact the product of the four blocks present in the loop: $T(s) = G_{vd}(s)H(s)G_c(s)\frac{1}{V_m}$. The green block is the transfer function that describes the variations of the output voltage due to duty cycle variations $\hat{d}(t)$, called $G_{vd}(s)$, and its ideal form what was reported in Figure 1.11 for the different types of converter. This is the function that is supposed to be known, in fact it represents the basic structure of the converter. It is important to model more precisely as possible this function, adding the parasitic elements and measuring the real value of the components. In the case that the device has a fixed and well known feedback path, also the function $H(s)$ can be added in the known block. The red part is instead obtained exploiting only some measurements. The idea is to measure the entire loop gain $T(s)$ in a certain bias condition (input voltage, output voltage, output current, BOM...)(a practical method is explained later) and, with some calculation, obtain the red part, that should be independent from the bias conditions. If the unknown part is denoted with $Y(s)$, the loop gain results being: $T(s) = Y(s) \cdot G_{vd}(s)$, and so inverting this formula it is simple to obtain the desired function:

$$Y^1(s) = \frac{T^1(s)}{G^1_{vd}(s)} \tag{1.7.1}$$

where the apex indicate that is obtained from a direct measurement.

At this point if it is requested to establish the stability of the overall system with different values of the bias conditions it is needed only to merge the two blocks studied separately and calculate the new loop gain and so the new phase margin. The function

$Y(s)$ does not depend from the BOM parameters, that are the elements that are typically changed during the analysis, and that belong to the known block. For this reason $Y^1(s) = Y(s) = Y^i(s)$ can be stored and used for the i-th prediction. The function $G_{vd}(s)$ can be easily changed in the mathematical model and so the desired loop gain can then predicted with the formula:

$$T^2(s) = Y^2(s)G^2_{vd}(s) = Y(s)G^2_{vd}(s) == \frac{T^1(s)}{G^1_{vd}(s)}G^2_{vd}(s). \tag{1.7.2}$$

Coming back to the buck, the known part contains the basic elements of the converter, i.e. the LC-filter. In addition also the power supply is known and the load can be considered known, in fact either it is a resistor or it can be rapidly measured. For better understanding it is suggested to see the Figure 1.24. The known block is highlighted in green, and it contains elements just mentioned. The rest of the circuit is considered unknown or it is irrelevant to the analysis.

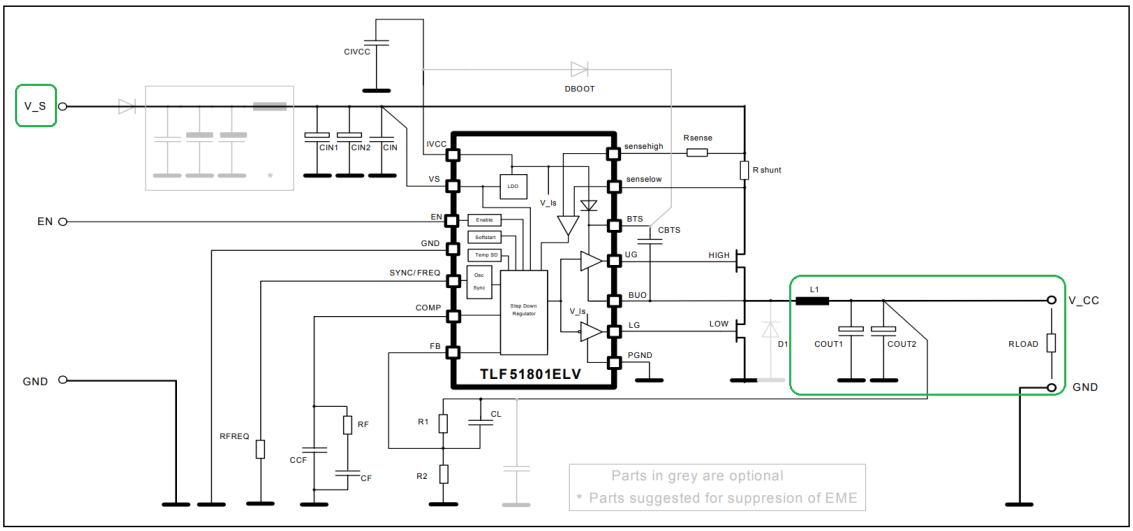


Fig. 1.24: Scheme of buck with the known part highlighted in green.

As reported in the section regarding the load step test the practical parameters that are usually changed are the load current, the input voltage (i.e. the power supply) and the inductor and the capacitor of the LC-filter. Trivially, a change of the load current means a change of the load impedance , in particular if it is simply resistive, the relation is reduced to the standard Ohm's law: $I_{load} = V/R_{load}$. So, having the possibility of changing the value of the four parameters $V_{in}, L,\ C,\ R_{load}$, gives the possibility of evaluating the behavior of the system in a very wide range. It is important to make sure that the variations of the parameters does not change the bias of the system, i.e. the point of work around which it has been made the linearization. For this reason a different approach for changing of the battery V_{in} and of the load current I_{load} must be taken into account.

In the Chapter 2 it is well explained how the procedure can be followed for the case of a buck converter, but ideally it can be adopted for different topologies also. The basic concept is to reduce the amount of measures needed to the set of measures that allows to characterize only the unknown part.

In the flow chart of Figures 1.26 is reported the load step measurement procedure (in brackets are reported the parameters that are typically interested), while in Figure 1.27 there is the new method. It is possible to see that the difference between the two charts stays on the loop needed for evaluating the stability of a new configuration. In the first case in fact it is necessary to remake all the procedure. If it is desired to change even a single parameter it is necessary to reorganize all the electrical board and retest it. In the second case instead it is not required to remake all the procedure, or at least not in any case. The technician have to decide if the change interferes on the bias value or if it is possible to update only the small signal model part. If the second option holds then it is sufficient to update the mathematical function that model the known part. In this way the amount of measurements needed for a complete stability analysis goes from $m \times n \times p \times q$ to $m' \times n'$, where $m' < m$ and $n' < n$ are the new numbers of different input voltages and load currents respectively. The value of the new number p' and q', i.e. the measurements taken with different values of L and C , ideally reduce to one. In Table 1.2 it is reported a simple example of possible laboratory requirements, and the aim of this table is to show the reduction of the effort needed. The number of the required different parameters is reported in the column *Current Method*, in fact the number of measurements needed in this case coincides with them.

	Required values	**Measures with Current Method**	**Measures with New Method**
Input Voltage V_{in}	5	m=5	m'=3
Load Current I_{load}	5	n=5	n'=3
Filter Inductor L	3	p=3	p'=1
Filter Capacitor C	3	q=3	q'=1
Total Measures	/	225	9

Tab. 1.2: Example of possible requirement table for a complete assessment of converter stability, with a comparison between current e new method.

It is worth to notice that in the new chart of Figure 1.27 is present a block that says *Measure Phase Margin*. This indicates that the technician have to find a way to measure efficiently the value of this parameter. The load step response can be related to phase margin, like reported above, but typically it is not so easy, so a different strategy has to be adopted. A possible approach is proposed in Chapter 2. The load step in the practice is used to have only a quick binary response: the system is stable or not.

A summary of the differences between the current methods used and the proposed one is visible in Figure 1.25, where in a simple and schematic way the main features of the different methods are listed. The two features considered are the possibility of making the analysis without knowing in details all the circuit and the possibility of evaluate the stability with a prediction instead of a measure. These features can coexists in the new methodology.

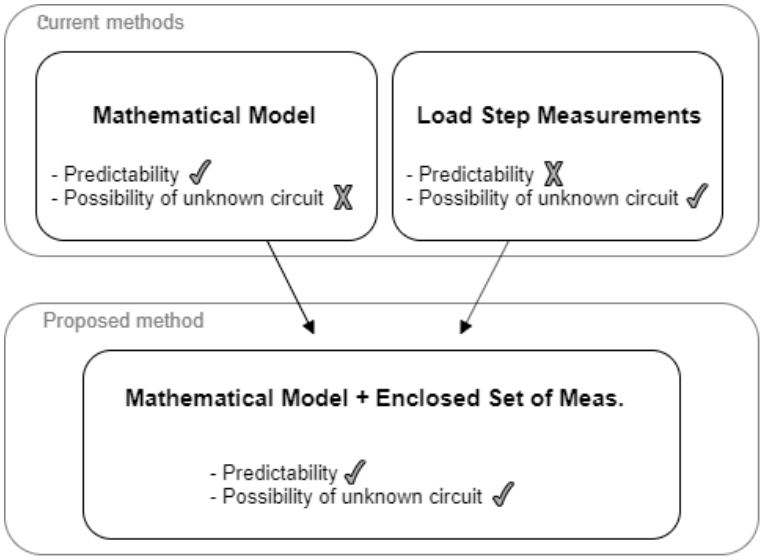


Fig. 1.25: Comparison between current and new method features.

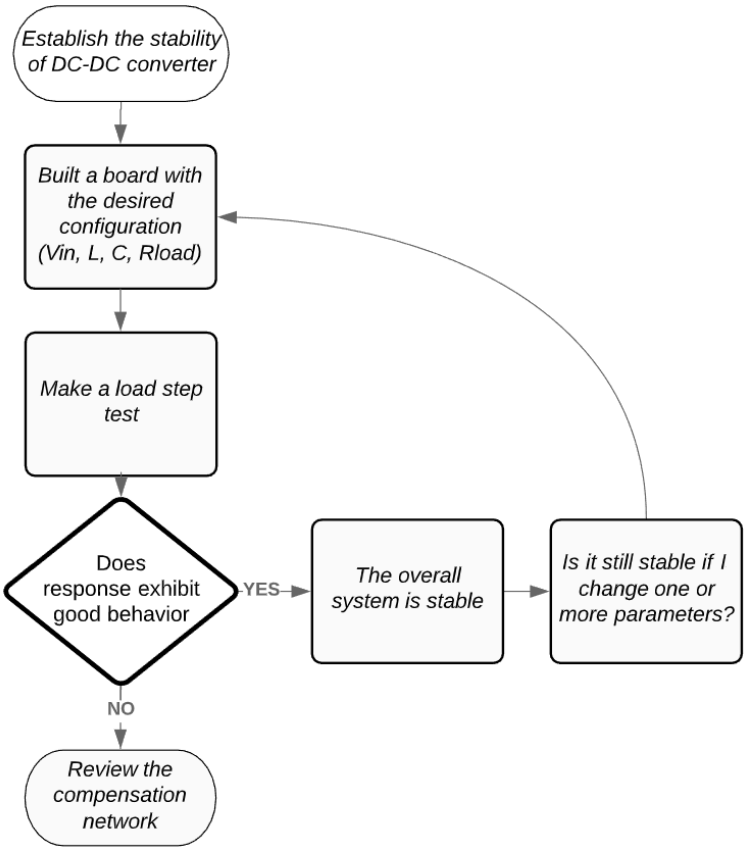


Fig. 1.26: Flow chart of current method for establish stability of DC-DC converter.

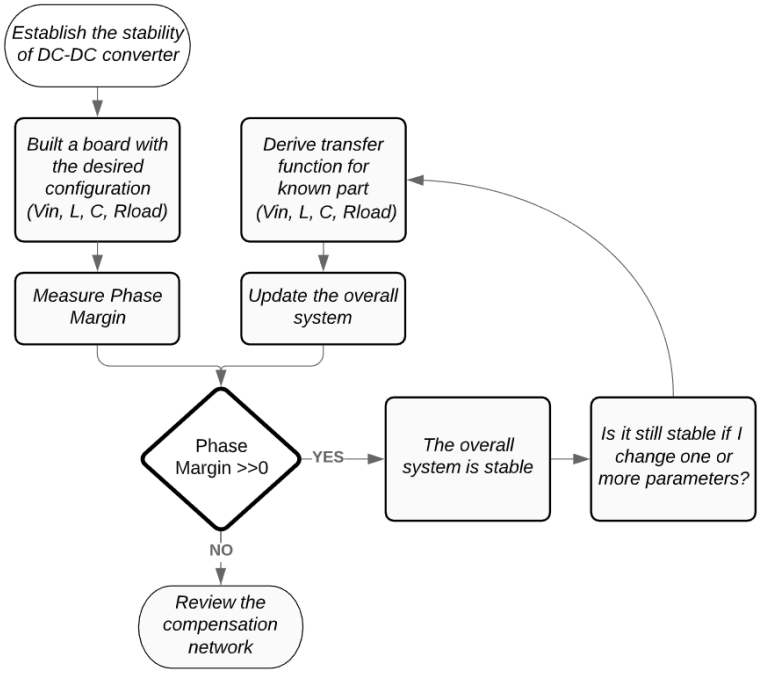


Fig. 1.27: Flow chart of proposed method for establish stability of DC-DC converter.

Chapter 2

Laboratory evaluation of the methodology

2.1 A specific Buck Converter: Infineon 'TLF51801ELV'

In this section it is described a specific buck converter released by 'Infineon Technologies'. The integrated circuit is identified by the code 'TLF51801ELV'. The Figure 2.1 reports the application scheme used in this project for testing the methodology introduced. It is possible to notice that the switching elements consist of two MOSFETs that are not embedded into the integrate circuit (in the figure they are denoted with HIGH and LOW). This strategy is not always followed, but in this particular case is useful for heat dissipation, this commercial product in fact can work with high value of load current (maximum 10 Amperes). Also the voltage divider on the feedback path is external, and this allows to have an adjustable output voltage. The reference voltage level at which the chip calculates the error is $V_{ref} = 1.2\ [V]$ and then, with an easy equation it is possible to impose the value of V_{out}:

$$V_{out} = V_{ref} \cdot \frac{R_1 + R_2}{R_2}, \tag{2.1.1}$$

that is simply the voltage divider relation. For example, in the laboratory evaluation made for this project the output voltage has been set equal to $V_{out} = 5.6\ [V]$ and so a possible choice is to take $R_1 = 100\ [k\Omega]$ and $R_2 = 27\ [k\Omega]$.

An important network presents in the application is the compensation. It is referred to the ground and its full description is reported in a dedicated section. At a first look it is possible to notice that it is composed by a capacitor C_{CF} in parallel to a RC path (R_F and C_F). Also the capacitor C_L have a compensation role even if it is inserted in the feedback path. In this configuration is also present a capacitor group (top left in the figure) to guarantee a stable V_{in}, in the sense that the voltage that comes into the chip has an almost perfectly constant value, i.e. it has a negligible ripple. In the following the voltage variations $\hat{v}_{in}$ are then considered null.

Another relevant pin of the chip is the one relative to Frequency. Here it is possible to set the switching frequency of the MOSFETs, simply connecting a precise resistor. The relation resistor-frequency is reported in the data sheet, for this project it has been used $R_{FREQ} = 20\ [k\Omega]$ that imposes $f_{SW} = 300\ [kHz]$.

The scheme is completed by other few components useful for the protection and current limitation of the chip. This regulator works in voltage mode, it means that it is designed with a single voltage feedback path and the pulse width modulation is performed by comparing the voltage error signal with a constant ramp waveform. The system has no feedforward function but only the feedback one. Furthermore, it operates in continuous conduction mode (CCM) only, it means that the current on the inductor does not reach the zero level. The following list (Tab. 2.1) summarizes the main features of the chip

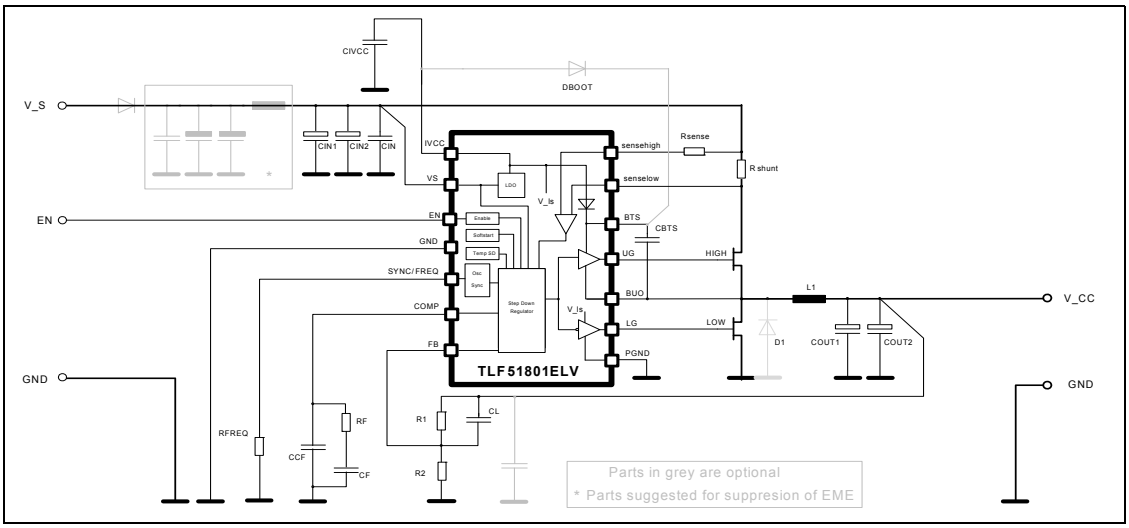


Fig. 2.1: Diagram of specific Infineon buck: TLF51801ELV.

used:

- 10 Amperes synchronous DC-DC step down controller
- Current limitation adjustable with Shunt resistor or Rdson
- Adjustable output voltage
- $\pm 2\%$ output voltage tolerance
- External power transistors
- Integrated bootstrap diode
- PWM regulation
- Very low dropout operation: max Duty Cycle higher than 99%
- Input voltage range from 4.75V to 45V
- Adjustable switching frequency from 100 to 700 kHz
- Synchronization input
- Very low shutdown current consumption ($< 2\mu A$)
- Soft-start function
- Input undervoltage lockout
- Suited for automotive applications: $T_j = -40°C$ to $+150°C$
- Green Product (RoHS compliant)
- AEC Qualified

Tab. 2.1: Features of buck converter TLF51801ELV.

2.1.1 Transfer Functions of the specific configuration

The transfer functions derived in the Chapter 1 is referred to the ideal case and then they introduce several approximations that are not acceptable in the real case. This is a typical issue well known in the engineering environment and for this reason a fine-tuning process of the mathematical model is needed. It is worth to recap that the only transfer function used in the final procedure is the control-to-output one, but for better understanding the overall system and also for highlight the improvements introduced all the transfer functions are now studied.

The more detailed model is obtained introducing the so called Equivalent Series Re-

sistance (ESR) of the inductor and of the capacitor. It is the resistive component that is present in every electronic element and make them differ from the ideal behavior. In order to build the transfer functions it is possible to follow the article [1], where the the averaged small-signal analysis has been adopted.

Now it is reported the basic idea of this paper but for a detailed analysis of the procedure it is suggested to read the paper [1]. The PWM converter is subdivided into two parts: linear analog part and nonlinear discrete part. The linear part consists of linear components such as capacitors and inductors with their equivalent series resistances. The nonlinear part consists of nonlinear semiconductor devices such as transistor and diode operated as switches that is as discrete components. The nonlinear part may be replaced by an average circuit model which emulates its average low frequency behaviour. The only difference between the mentioned paper and this thesis is that the low switch is a diode instead of a MOSFET, but it is not difficult to replace it. The diode is modeled with a resistor in series to a voltage generator, while the MOSFET is modeled with the drain-source resistor. The averaged model obtained in the paper is reported in Figure 2.2 where the switching network has been replaced with linear components that allow to facilitate the transfer functions derivation.

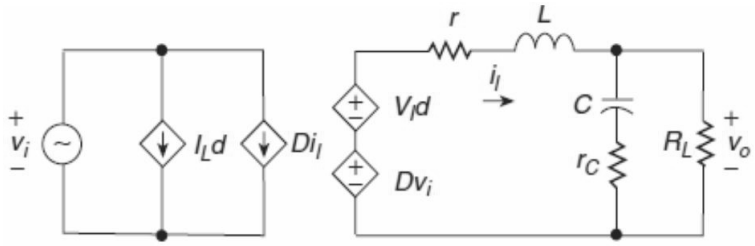


Fig. 2.2: Small-signal equivalent scheme of buck converter with ESRs.

At this point in order to obtain the different functions it is sufficient to exploit the superposition principle and resolve the resulting networks. Here they are reported the final results for the control-to-output transfer function that is the core of the buck:

$$G_{vd} = V_g \frac{R_o}{R_o + r_L} \frac{s r_C C}{1 + s\left(\frac{L}{R_o + r_L} + \frac{C(R_o r_L + R_o r_C + r_C r_L)}{R_o + r_L}\right) + s^2\left(LC\frac{R_o + r_C}{R_o + r_L}\right)} \tag{2.1.2}$$

where R_o is the load resistor, while r_C and r_L are the ESR of the LC-filter. The bode plots of all the different transfer functions are reported in the Figure A.1, present in the Appendix section.

The transfer function that are meaningful for the stability analysis is the loop gain $T(s)$, like explained in the previous Chapter it is equal to the product of the transfer functions present in the loop path: $T(s) = G_C(s)G_{vd}(s)H(s)\frac{1}{V_m}$ (see Figure A.2 of the Appendix). This is the compensated version, but in order to obtain it, it is needed to study the uncompensated one $T_u(s) = \frac{1}{V_m}G_{vd}(s)$ ($\frac{1}{V_m} = 1/1.25 = 0.8$). The function $H(s)$ is considered a compensation part also because it presents also a capacitor that interferes the frequency response of the overall system. Analyzing the bode diagram of T_u is then important to build a suited compensator and a schematic version of it is then reported

in Figure 2.3. The value of the resonant peak depicted in the figure, is given by the approximated relation: $Q \approx R_o\sqrt{\frac{C}{L}}$. It is easy to see that the phase margin is very small, approximately null, or equivalently that the magnitude of $T_u(s)$ reaches the zero dB axis with a slope of -40dB/dec.

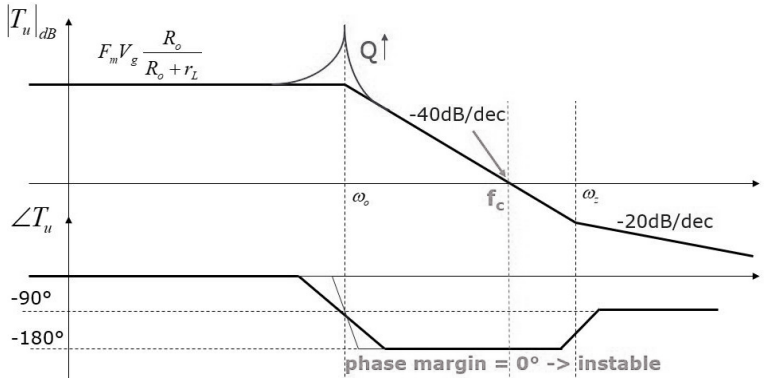


Fig. 2.3: Schematic Bode diagram of uncompensated loop gain T_u.

From this bode diagram it is possible to build a compensation and the process is explained in the next section.

2.1.2 Compensation Network

To increase the phase margin of the system used in the laboratory evaluation a PID compensator is present. It allows to adjust the frequency evolution of T_u in the desired way. A PID has this standard structure:

$$G_C(s) = \frac{G_0}{s}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_1}\right)} \tag{2.1.3}$$

where the ω_{z1}, ω_{z2}, ω_{p1}, ω_{p2} are the zeros and poles frequencies that must be carefully chosen for regulating the system. In particular, a pole has to cancel the ESR zero of G_{vd} while the other pole has to be placed in order to get maximum attenuation of the switching ripple and high frequency noise with the minimum phase lag at the crossover frequency. The two zeros have to be lower than the resonance frequency in order to compensate the pole in the origin and raise up the phase. In this way, even if there is a rapid phase shift at the resonance, the possibility of having negative phase margin is avoid. The result is shown in Figure 2.4, while the electronic circuit that allows to have a PID action is reported in the Figure 2.5.

Here it is visible the error amplifier that compares a reference voltage with the feedback voltage. The feedback voltage is a rearranged version of the output voltage (the network on the left side of the figure is $H(s)$). The error signal that comes out from the error amplifier feeds the compensation network (the network on the right side of the figure is in fact $G_c(s)$). It is interesting to notice that this network is connected to ground, and not to the Feedback-pin like usually, because the designer of Infineon noticed a problem for

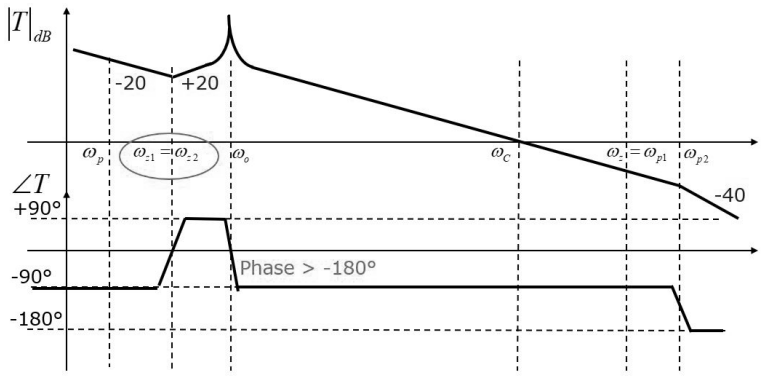


Fig. 2.4: Schematic Bode diagram of compensated loop gain $T(s)$.

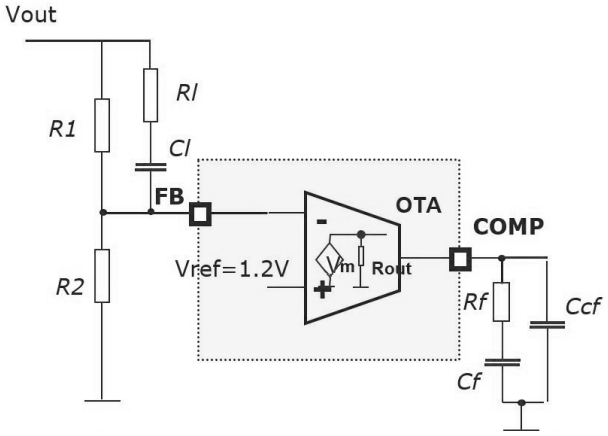


Fig. 2.5: Compensation network of Infineon buck.

the Over-voltage controller and this is a good strategy to remedy it. The error amplifier used is an OTA (Operational Transconductance Amplifier) and the values of parameters of this element are $V_m = 1.25$ and $R_{out} = 10[M\Omega]$. This circuit allows to adjust the phase margin, like explain above, and in particular it allows to introduce a transfer function from v_{out} to v_{comp} equals to:

$$\frac{v_{comp}}{v_{out}} \simeq Ak \cdot \frac{1 + sR_FC_F}{(1 + sR_{out}C_F)(1 + R_FC_{CF})} \cdot \frac{1 + s(R_L + R_1)C_L}{1 + sC_L\frac{R_1R_2+R_1R_L+R_2R_L}{R_1+R_2}} \tag{2.1.4}$$

where $A = g_m \cdot R_{out}$ and $k = \frac{R_2}{R_1+R_2}$. The symbol $\simeq$ indicate that the dominant pole approximation has been introduced.

Then the values of the the passive elements can be set according to the needs in order to create the desired evolution of $T(s)$. In particular for the specific configuration adopted they are set like reported in Table 2.2:

The theoretical values indicates the results of a mathematical calculation done in Matlab, while the laboratory values indicates the nominal values of the components used to build the electrical board. The mathematical values are then replaced with the nominal values found in laboratory, in order to have a match between the two environments.

	R_1 [kΩ]	R_2 [kΩ]	R_L [kΩ]	R_F [kΩ]	C_F [nF]	C_{CF} [nF]	C_L [nF]
Theoretical value	100	27.3	0	6.65	15	12	120
Laboratory value	100	27	0	6.8	15	12	120

Tab. 2.2: Passive elements values of the compensation network $G_C(s) \cdot H(s)$

2.1.3 Bill of Material (BOM)

With the term 'bill of material', shortened in BOM, it is indicated the set of all the components to manufacture an end product. It corresponds to the parameters that characterize the final behaviour of the system and that the user can change as he likes. The aim of this section is to clarify which is the BOM of the particular case taken into account, i.e. a buck converter. The components that can be changed during the stability assessment are first of all the inductor and the capacitor, included their ESRs. Also the value of the voltage divider can be chosen by the user, but once set it does not change during the analysis, so it is not contemplated for the aim of this project. The voltage divider is in fact included into the black box model and maintains its value fixed. The same reasoning can be done for the compensation network. In fact, the values of the passive components that compose this network are chosen with an a priori simulation on Matlab, but once set they are kept fixed. This choice is taken also in respect of commercial requirements, in fact the final user prefers not to have problems regarding the compensation. Definitely, the components that belongs to the BOM are: L, ESR_L, C, ESR_C, R_{load}. Also the input voltage V_{in} changes during the analysis but it is not typically considered part of BOM because it is not an electrical component but an active power source. However it is important to take into account also this parameter.

2.2 Small-signal variation analysis and prediction

The aim of the thesis is to predict the stability at BOM variation. The starting point is to consider variations of the LC-filter, i.e. try to understand how the stability of the system change when either the inductor or the capacitor is changed. This is the first evaluation because it is possible to exploit the small signal mathematical model of this filter, i.e. the function $G_{vd}(s)$, already studied. The change of this two parameters, and of their ESR, in fact, does not interferes the large-signal behavior. Restricting to the case of LC-dependant prediction the procedure used is easily schematised:

- a measure of the loop gain is executed with the network analyzer and memorized on a Matlab file. The instrument provides two traces, one for the magnitude and one for the phase, so the transfer function is obtained with the relation:

$$T(s) \mid_{s=j\omega} = T(j\omega) = |T(j\omega)|e^{j\angle T(j\omega)}. \tag{2.2.1}$$

- A measure of the real BOM is executed, again with the network analyzer, and the

values of the elements C, L, ESR_C, ESR_L are memorized.

- The prediction is made on Matlab, without the necessity of new laboratory effort. Here the new desired values of BOM can be inserted to replace the ones used for the measure.

In the following sections these three points are described one by one.

2.2.1 How to measure Loop Gain and Phase Margin

In this section it will be described how to evaluate the feedback loop characteristic of a DC-DC converter. Like said, a fundamental parameter for establish the stability is the phase margin of the loop gain transfer function. So the aim is to measure the loop gain, focusing on the frequencies that contain the crossover frequency f_C. The DC-DC converters have typically a bandwidth (that corresponds to the value of f_C) of around $f_{SW}/10$, where f_{SW} is the frequency of the switching elements (the project circuit has a switching frequency of $f_{SW} = 300$[kHz]). The feedback loop circuit in its operating condition can be measured with a low-frequency network analyzer. The network analyzer is a measurement tool that allows to characterize the behavior of any electronic network, either active or passive (see Appendix for a detailed explanation of its operation). The idea is to measure the effects produced by the network in response of a known signal injected. The strength of the network analyzer is the possibility of determining the phase and magnitude of the measured signal. Substantially, it allows to obtain the transfer function of a device stimulated by an AC signal that can be controlled in frequency or in power and it is injected via a dedicated circuit. The analyzer measures, in fact, the ratio of the AC voltages at both ends of the injection circuit with the receiver ports R and T that have high impedance inputs. The signal should be injected in a point of the circuit where the relative input impedance Z_{in}, seen from this point, is high, while the relative output impedance Z_{out} is low (see Figure 2.6).

In the case of the DC-DC converters, the test signal is generally injected at the point just before the divider circuit on the feedback path by using the floating injection circuit that consists of a transformer and a resistor (see Figure 2.7). By injecting the test signal at the point where the relation $Z_{in} \gg Z_{out}$ is satisfied and using the resistor R that satisfies $Z_{in} \gg R \gg Z_{out}$, we can measure the round transfer function $-T(s)$ with the ratio measurement T/R, without disturbing the original loop characteristics.

It is important to select an injection transformer that presents a flat transmission response in the entire test frequency range. The transformer should have an impedance that is not extremely smaller than the analyzer's source output impedance of 50 [Ω], which means the self inductance should be large enough. Also, the transformer must work properly in the high-frequency region without making a self resonance. Given these constraints, a typical choice is to use a so called 'balun' (bal-anced to un-balanced) transformer. Such transformer is used to avoid the connection between circuits whose ground-level voltages are electrically incompatible. It is also useful to avoid that the output DC voltage of the converter load the AC source of the network analyzer. In this project it has been used the

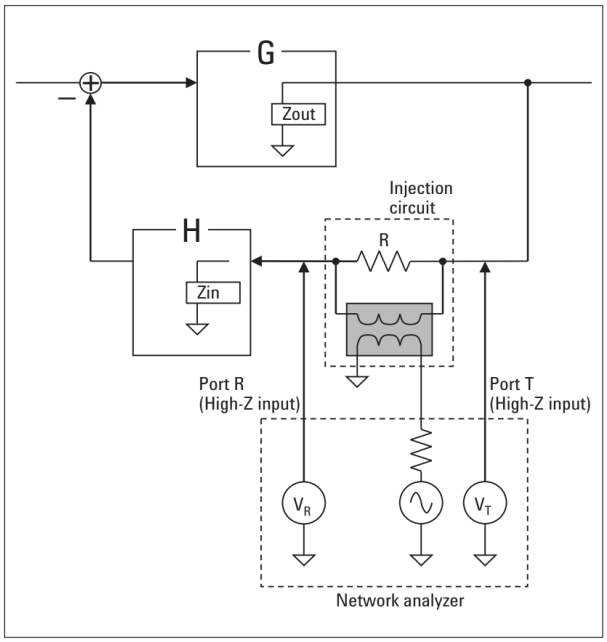


Fig. 2.6: Scheme of how to measure generic loop gain via Network Analyzer.

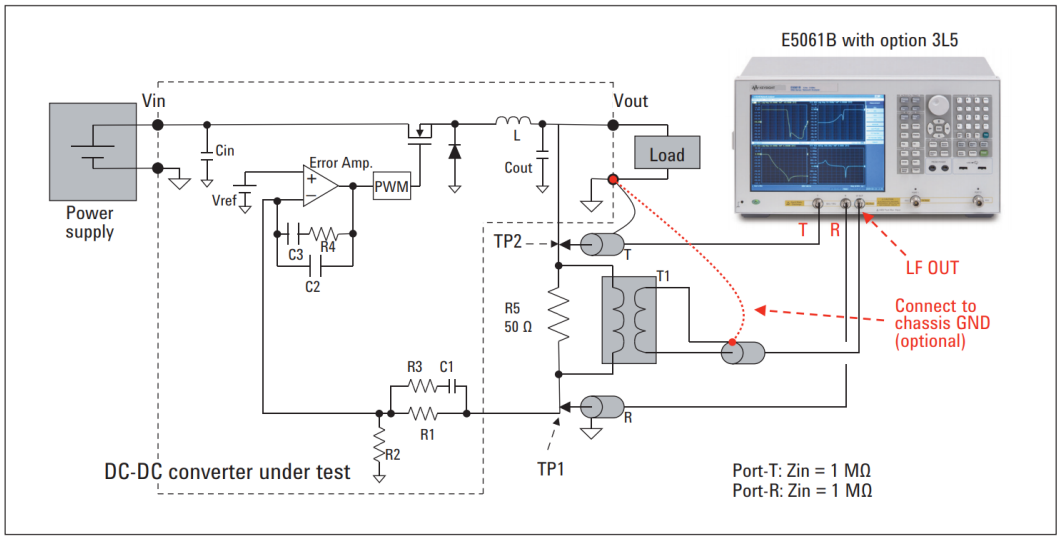


Fig. 2.7: Scheme of how to measure converter loop gain via Network Analyzer.

'Picotest J2101A' with ratio 1:1 (for some specifics of this tool go to the Appendix).

The injected signal level should not be very high to prevent the feedback loop circuit from getting into the nonlinear region. The probing should be done with the high input impedance as not to affect the operation of the feedback loop circuit. As for the measurement frequency range, it's common that the measurement is started from the low frequencies like 100Hz. But in general, the important frequency range for evaluating the loop characteristics of DC-DC converters goes typically from several kHz to several hundreds of kHz where the LC filter's resonant frequency and the loop crossover frequency exist. Therefore, the measurement at the low-frequency range does not have to be so strict. Note that the measurement method discussed here is basically applicable to the linear voltage-mode control loops only. It is not applicable to the current-mode control

loops and nonlinear control loops.

In the Figure 2.8 is reported an example of measure of loop gain, compared with its mathematical model. The picture reports the magnitude and the phase of the loop gain, i.e. the bode plot and it is possible to notice that the measure has a quite similar behavior in respect to the model but does not perfectly fit it. In particular it is visible a different behavior at high frequencies, where typically the parasitic elements act. Also in low frequencies domain the magnitude of the two quantity present a not negligible difference, considering that the lines represent the dB values. The example reported is referred to the set up of Table 2.3, where the nominal values are used.

V_{in}	10 [V]
R_{load}	1 [Ω]
L	5.6 [μH]
C	165 [μF]
ESR_L	16 [mΩ]
ESR_C	10 [mΩ]

Tab. 2.3: Nominal values of parameters used in the example reported in Figure 2.8.

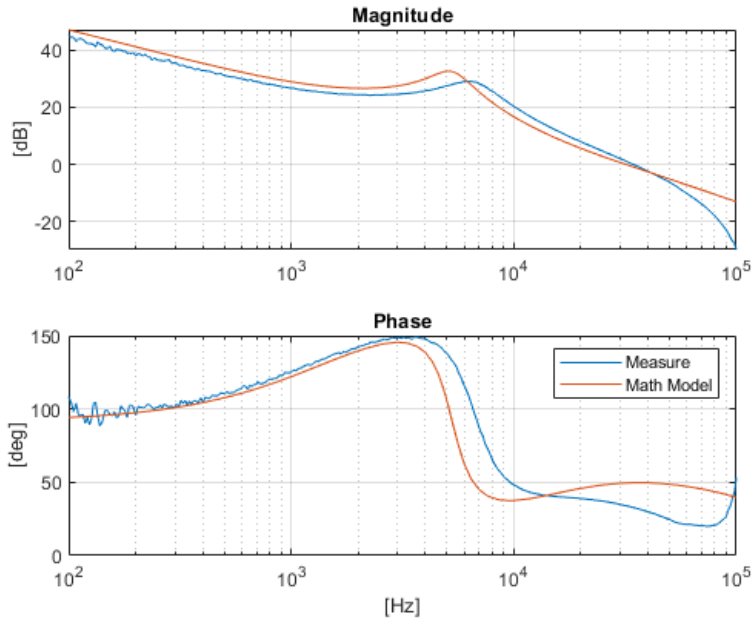


Fig. 2.8: Loop gain bode plot - Comparison between measure and mathematical model. In blue the measure and in orange the mathematical model. *Note*: the phase plot is shifted of +180°.

2.2.2 Measurement of real BOM

For a well-tuned mathematical model it is important to use the real values of the passive elements present. In the engineer world it is known that the nominal value reported on the components does not always coincides with the effective one. For a capacitor or an inductror the tolerance value can be even about 20%, so the real value can be very different from the nominal one and consequently the transfer functions can be untruthful. Here it is reported a possible method to measures the output impedance of the buck.

The instrument used is again the network analyzer that allows to measure the behavior as a function of frequency and then calculate the value of equivalent circuit. If it is desired to measure a single component it is sufficient to set the equivalent circuit equal to a series of resistor, capacitor and inductor.

The channels T and R of the instrument can measure only voltage so to perform an impedance measure a specific measurement setup is needed. For example, measuring the ratio T/R, T must measure a voltage and R must be associated to a current:

$$Z = \frac{V_T}{V_R} = \frac{V}{I} \tag{2.2.2}$$

The application note present on the Agilent website describes five techniques to perform an impedance measurement. In this project, it has been implemented the technique called shunt-thru and showed in Figure 2.9.

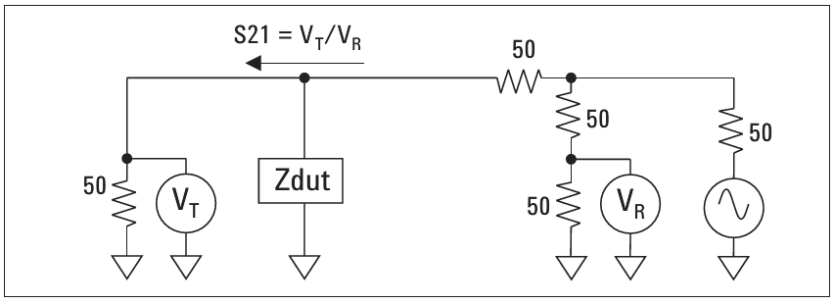


Fig. 2.9: Shunt-thru configuration for impedance measurement.

This configuration includes a so called power splitter to weight the current flowing into the measured impedance as a voltage measured across a resistor, that is precisely the strategy that allows to measures an impedance via a voltage ratio as required. This is the suggested configuration because the aim impedance is the output impedance of a regulator, that must be low impedance, at least inside its working frequency range. On the application note is in fact explained which configuration use for different type of impedance and Figure 2.10 summarizes it.

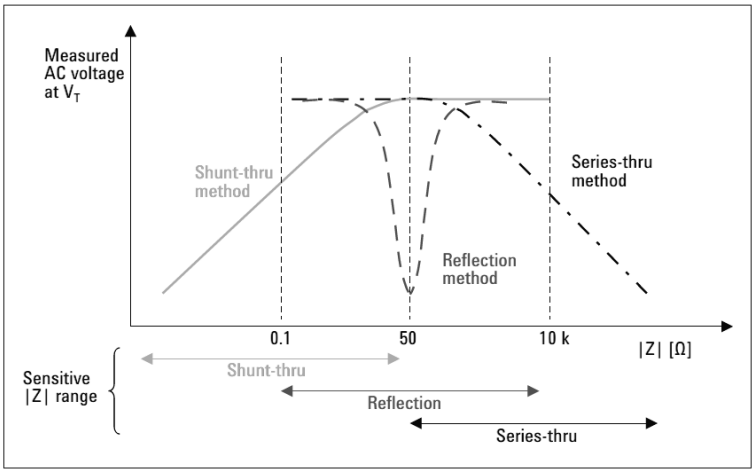


Fig. 2.10: Impedance measurement methods with network analyzer.

From Figure 2.9 it is possible to understand that the transmission coefficient s_{21} is measured by connecting the DUT in the shunt connection between the signal line and GND, and then the impedance is derived from s_{21}. The relation between the DUT impedance $Zdut$ and s_{21} is easily derivable and it results:

$$Z_{dut} = 25 \cdot \frac{s_{21}}{1 - s_{21}} \tag{2.2.3}$$

Where $s_{21} = V_T/V_R$.

For a good measure it is needed to calibrate the instrument in a proper way. For impedance measurement the network analyzer requires a so called SOL-calibration. The acronym SOL stands for Short-Open-Load and it describes how this operation is performed: the technician has to prepare the set up as for the desired measure, but instead of the desired impedance (Z_{dut} of the Figure 2.9) he has to measure three known resistive values: $R = 0,\ R = \infty\ R = 50[\Omega]$.

Another possible strategy is to measure the entire impedance and then obtain a desired equivalent circuit, in this case the parallel of output resistor and LC-filter. For this purpose it is needed a different configuration of the measurement set-up: the integrated circuit has to be cut off from the measure, and for this a short to ground has to be done. It means that the technician has to create a link between the inductor and the ground level (see Figure 2.11).

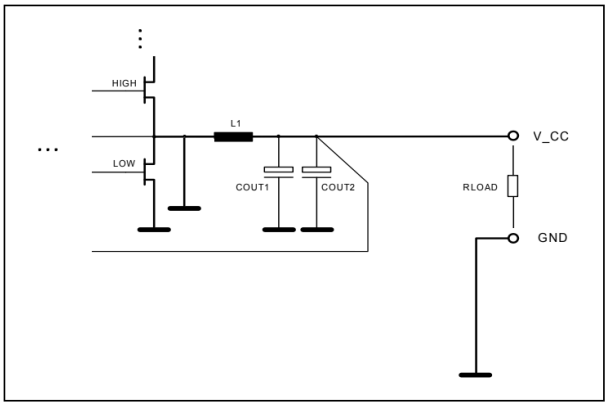


Fig. 2.11: Circuit with the short-to-ground for output impedance measure.

In this case the mathematical model needed is the one that does not consider the ESRs, in fact there are now integrated into the R_{load}. The comparison between the two procedure are visible in Table 2.4.

	R_{load} [Ω]	L [μH]	ESR_L [$m\Omega$]	C [μF]	ESR_C [$m\Omega$]
Nominal Value	1	5.6 ± 20 %	∈ [15.7,17.5]	165 (33 ± 20% × 5)	≈ 2 (10/5)
Measured Single Value	0.98	6.12	15.30	144.40	2.91
Measured Total Z_{out}	0.59	4.9	/	143.4	/

Tab. 2.4: Comparison between nominal and measured values of passive components.

2.2.3 The prediction on LC variation

The prediction on Matlab consist of few easy steps. First of all the transfer function $G_{vd}(s)$ is calculated, this function is in fact completely derived from mathematical studies reported above. It allows to obtain the function defined here as $Y(s)$, i.e. the ratio between the measured loop gain $T(s)$ and the latter: $Y(s) = T(s)/G_{vd}(s)$. The detailed description of this calculus is reported in the following, however the basic idea is to make a calculation point by point. This strategy is adopted because the network analyzer provides files that contain quantized values of the loop gain, in particular it is possible to extract two 'comma separated values' (csv) files, one for the magnitude trace and one for the phase trace.

The number of frequencies at which the network analyzer measures the loop gain, i.e. the x-axis of the figures reported, is settable by the user and a suggestion is to set one hundred of frequencies for each decade of the bode plot. Looking again at the example of Figure 2.8, the network analyzer is set to measure the loop gain from 10^2=100[Hz] to 10^5[Hz]=10[MHz], so the switching frequency, which varies around $f_{SW} = 300[kHz]$, is certainly present. The total number of samples is given by: 3 [decades] $\times$ 100 [samples/decade] +1 [sample] = 301 [samples], where the last sample is needed to include the two extreme values. It is worth to notice that the phase measured by the network analyzer provides directly the phase margin, in the sense that the function measured is not exactly $T(s)$ but is $-T(s)$, due to the negative sign introduced by the error amplifier. For this reason for detecting the phase margin it is sufficient to detect the crossover frequency and then read the value of the phase at that frequency, without the need to calculate the difference between the phase and the value -180°.

- **Loop Gain as a function of LC-filter**

  The thesis is oriented to a prediction action and during the laboratory analysis this has been always taken into account, but a first study of the loop gain has been done exclusively via a set of measures. The aim of this first analysis is to understand how the loop gain is in practice and how it varies when the parameters of interest are changed. In particular the change of LC-filter has been studied, and the Figure 2.12 allows to make some first considerations. In this figure there are two graph, the one on the left represents the evolution of the crossover frequency, while the right one represents the phase margin evolution. Both of them are reported as a function of the L parameter, while the value of C has been kept constant to $C = 231$ $[\mu F]$. The input voltage is kept at $V_{in} = 20$ $[V]$ and the output current $I_{load} = 5.6/36 = 0.16$ $[A]$. The blue circles represent the measures done in laboratory, where for each value of L the loop gain has been measured, and consequently the value of the two desired variables. An easy elaboration on Matlab has allowed to build the blue lines that are mathematical interpolations on the measures. The cyan lines represent a sort of confidence interval of $\pm 10\%$ in respect to the interpolation. The same analysis has been done considering the loop gain as a function of C, i.e. keeping L fixed to the constant value $L = 3.9$ $[\mu H]$ and changing the value of the capacitor (see Figure 2.13). To validate this interpolation lines others measurements have been

done and reported in the graphs with the black stars. It is possible to notice that all of them are included in the confidence interval and furthermore that the trends of the interpolations are confirmed also with values of L that exceed the extreme values of the starting measures. It is also reported a red diamond for each graph, it represents an example of the predicted value obtained with the final procedure. As it is easy to see, also these predicted values belong to the desired regions. This example is a prediction done for $L = 9\ [\mu H]$, obtained starting from a measure done with the same value of input voltage and output current, and with a LC-filter given by $C = 165\ [\mu F]$ and $L = 5.6\ [\mu H]$. The prediction is obtained with the procedure explained in details in following section. Like said, this study is only a first analysis of the loop gain and it involves a set of measures that, even if is not so big, it is reducible with the predictions. However the results are quite good and so they can be adopted if a brief analysis of the buck is required.

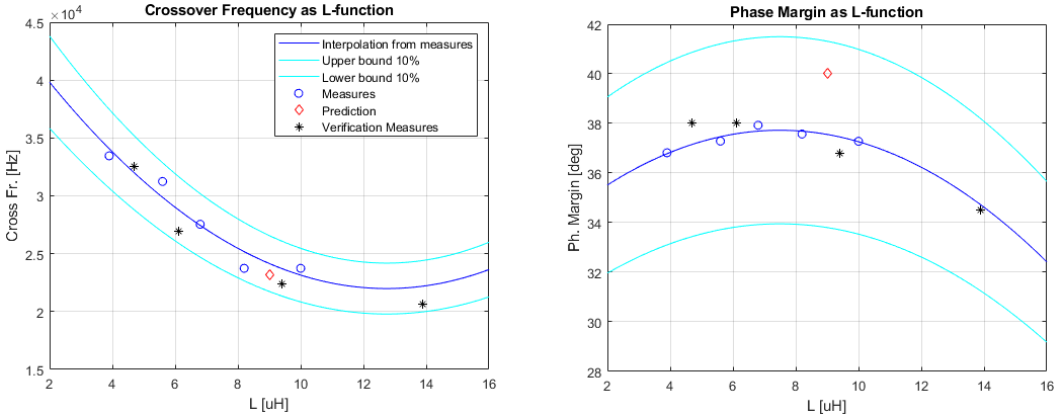


Fig. 2.12: Crossover Frequency and Phase margin as a function of L. Interpolation between measures in blue, confidence interval in light blue, verification measures in black and a prediction result in red.

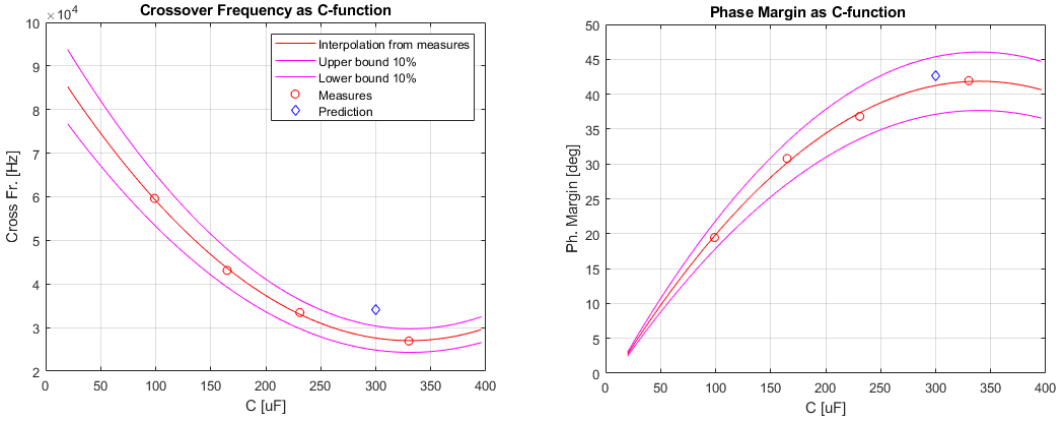


Fig. 2.13: Crossover Frequency and Phase margin as a function of C. Interpolation between measures in red, confidence interval in magenta and a prediction result in blue.

A further analysis can be done creating the same graphs but exploiting some predicted values instead of measures. The interpolation lines obtained exploiting the predictions are reported in the Figure 2.14, where the comparison between differ-

Inductor L [μH]	3.9	5.6	6.8	8.2	10.0
Capacitor C [μF]	99	165	231	330	/

Tab. 2.5: Nominal values of LC-filter used to built the matrix of interpolation lines.

ent interpolations is present. The blue line is the interpolation just described for the previous figure, i.e. it exploits five measures, while the other three lines are obtained exploiting only one measure and deriving the other four points with the predictions. The single measure used for each interpolation line corresponds to the point represented by a star with the same color of the line. It is possible to notice that these different interpolation lines differs not so much from the one obtained with the measures. Only the magenta line seems quite different in the phase margin graph, but if it is noticed that the maximum difference is about 7 degrees, it can be consider acceptable. This consideration brings to highlight that the prediction procedure can reduces substantially the amount of measurements without interfering so much the reliability. In the following it is then reported with more details this prediction approach, that here has been validated in an empirical way.

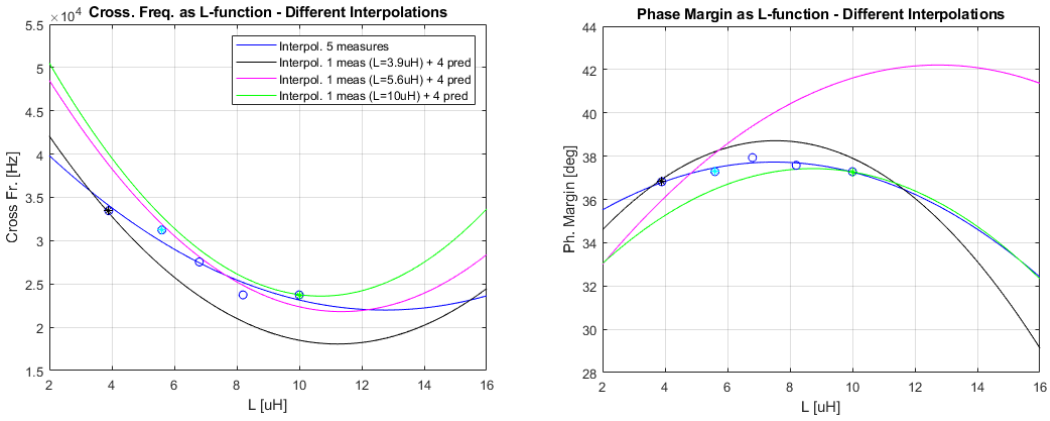


Fig. 2.14: Crossover Frequency and Phase margin evolution as a function of L. Interpolation between measures in blue and three different interpolation lines built with one measure and four predictions.

The interpolation line in Figure 2.12, obtained from five different values of L and with a fixed value of C, has been obtained also for different values of the latter. In the same way, different interpolation lines have been obtained for the opposite version, where the value of L is fixed and the variable parameter is C (Figure 2.13). In this way it has been built a matrix of interpolation lines with few values of L and few values of C, both for the crossover frequency analysis and the phase margin one. The different values that compose the matrix are reported in the Table 2.5.

For an intuitive comprehension of the results obtained, two 3D-graphs are reported in Figure 2.15. Here it is possible to understand how the crossover frequency and the phase margin change as LC-function: the surfaces obtained characterize the small-signal behavior of the loop gain and the stability of the overall system.

To build these 3D plots the laboratory effort is quite big, so the aim of the project is

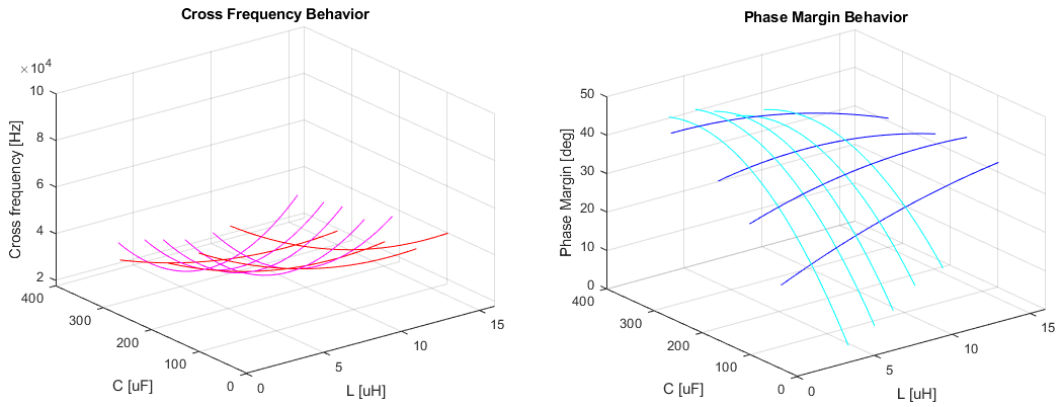


Fig. 2.15: Crossover Frequency and Phase margin as a function of LC-filter.

not completely caught, but however it can be consider a good first tool to predict the stability for a large range of LC variations. With this surfaces it is in fact possible to predict how the loop gain reacts to any variation of L, C or both of them, exploiting a finite set of measurements of cardinality equals to $p \times q$, where again p and q are the number of measures with different values of L and C respectively. In particular, the value of $p \times q$ for the case reported is equals to $5 \cdot 4 = 20$, that means that 20 measurements has been done, and for each measure one electrical component has been replaced with another one. This requires a lot of time and also a number of components that can be not always immediately available.

- **LC-dependant prediction**

  After understanding how the loop gain varies as a function of L and C, it is now reported how this behavior is predicted. The basic idea behind the prediction has been already explained in previous chapter but here, for better understanding this operation it is reported a flowchart (Figure 2.16) and some code rows of the Matlab script .

  The first block of the flowchart is simply the implementation on Matlab of the transfer function $G_{vd}(s)$, reported at the at the beginning of the chapter. Clearly, the values of L, C, V_{in} and R_{load} have to be set as the one used in the laboratory set up:

```
% PARAMETERS
Vo = 5.6;          % output voltage
Vi = 20;           % input_ voltage
Ro = 36;           % output resistor
Iload = Vo/Ro;     % output current
L = 5.6e-6;        % inductor
C = 165e-6;        % capacitor
ESRl = 16e-3;      % inductor ESR
ESRc = 10e-3;      % capacitor ESR

% BUCK POLE
omega0_buck = 1 / sqrt(L*C*(Ro+ESRc)/(Ro+ESRl));
```

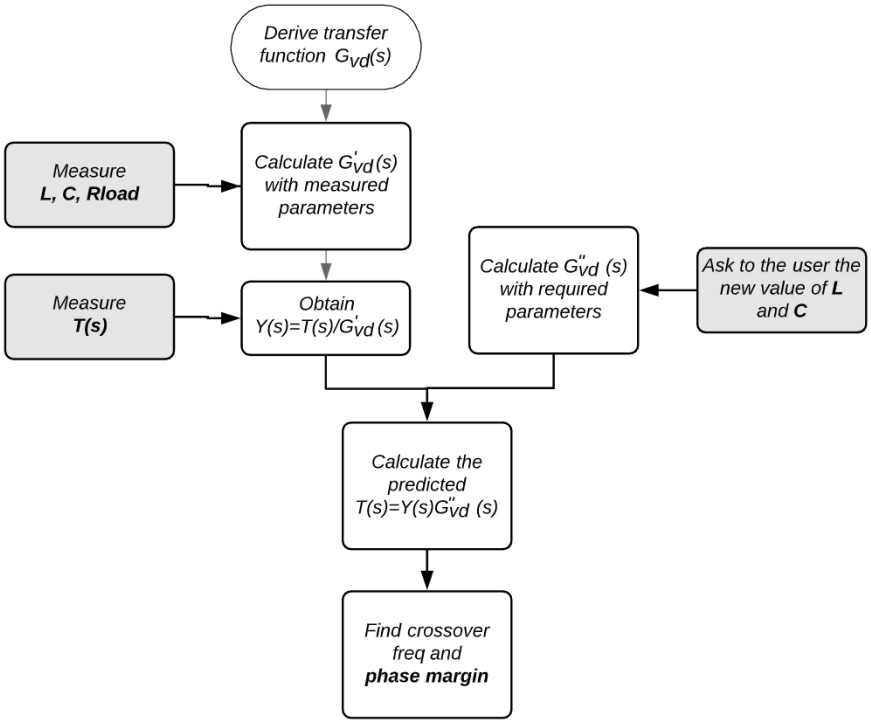


Fig. 2.16: Flowchart of Matlab code for LC-dependant prediction.

```
Q0_buck = 1/omega0_buck/(L/(Ro+ESRl)+C*(Ro*ESRl+Ro*ESRc+ESRl*ESRc)/(Ro+ESRl)
      );
Buck_pole = tf([1], [1/(omega0_buck^2) 1/(omega0_buck*Q0_buck) 1]);

% Gvd: CONTROL-TO-OUTPUT TRANSFER FUNCTION
Gvd0 = Vi * Ro / (Ro + ESRl);
Gvd0_dB = db(Gvd0);
omega_z_Gvd = 1 / (C*ESRc);
Gvd_zero = tf([1/omega_z_Gvd 1], [1]);
Gvd = Gvd0 * Gvd_zero * Buck_pole;
```

The transfer function `Buck_pole` has been defined for more clarity on the code and because it is the common denominator that appears also in the other functions of the overall model studied.

The second step is the calculation of the transfer function $Y(s)$ that describes the unknown part of the circuit. It is obtained with a calculation for points, like reported in the following section

```
% UNKNOWN TRANSFER FUNCTION
Ymag_mod = Tmag_mod./Gmag_mod;
Ymag_db = 20*log10(Ymag_mod);
Yph_deg = Tph_deg - Gph_deg;
Yph_rad = Yph_deg * pi/180;
Y = Ymag_mod.*exp(j.*Yph_rad);
```

where the letter `T`, `Y` and `G` indicates the three different transfer function of interest:$T(s) =$

$Y(s) \cdot G_{vd}(s)$ (the subscript $_{vd}$ is tacit). The labels `mag` and `ph` indicates the magnitude and the phase respectively, `mod` and `db` indicates the absolute value and the dB value, and finally `rad` and `deg` indicates the unity for the phase: radiants or degree.

The flowchart presents then another block that calculates again the function $G_{vd}(s)$, where this time the parameters values are inserted by the final user that can choose the desired values via the *input* Matlab function. After these two parallel operation, one obtained from the measures and one obtained only from mathematical calculation, there is a block that merges them. Here the predicted loop gain is derived, again with a for points calculation:

```
% LOOP GAIN PREDICTION
Tmag_mod_predLC = Gmag_mod.*Ymag_mod;
Tmag_db_predLC = 20*log10(Tmag_mod_predLC);
Tph_deg_predLC = Gph_deg + Yph_deg;
Tph_rad_predLC = Tph_deg_predLC*pi/180;
Tpoints_predLC = Tmag_mod_predLC.*exp(j.*Tph_rad_predLC);
```

where the label `predLC` indicates that the prediction regards only the LC-dependant prediction.

Finally it is easy to obtain the desired stability parameters detecting the minimum dB-value of the loop gain (theoretically the zero dB value should be found, but in practice there is no perfectly zero point due to the fact that the derivation is done for points).

```
% CROSSOVER FREQUENCY & PHASE MARGIN
[~,index] = min(abs(Tmag_db_predLC));
fcross_pred = f_hz(index);
margin_pred = Tph_deg_predLC(index);
```

where `f_hz` is the array that contains the frequencies in Hertz of the network analyzer.

2.3 Bias effects on stability

The variation of the voltage battery V_{in} and of the load current I_{load} has to be consider in a different way in respect to the LC-filter variation.

This is suggested because the value of these parameters influence the point of work of all the active components present in the integrated chip. The several of hundreds of active components present in the chip, that are essentially transistors, have typically a non linear behavior that is not so easy to take in consideration, so a practical procedure must be adopted.

2.3.1 Interpolation approach on AC signal model

The strategy adopted for extending the prediction to bias variation is an empirical, measured-based method. The idea is to acquire some measures obtained with different bias values and interpolate them in order to allow a complete variability of the bias

parameters. In particular, this interpolation involves two parameters, V_{in} − I_{load}, and then two steps are needed.

- The first step provides the loop gain at the desired value of load current. The interpolation is done between n different loop gains, obtained with n different values of the current, while the input voltage is kept fixed (the LC-filter is formed by $L = 5.6[\mu H]$ - $C = 165[\mu F]$). This operation is then repeated for m different value of input voltage. In this way m loop gains are obtained starting from $m \times n$ loop gains.

- At this point the second step of interpolation procedure provides the loop gain at the desired value of input voltage, starting from the m loop gains just obtained. In this way it is finally derived the single desired loop gain with the desired bias.

The measurements needed are then $m \times n$ and here it is reported the code rows that execute this interpolation:

```
Vvec = [10 20 30];                    % m different voltages
Rvec = [0.857 1 1.6 3.9 10 36 inf];   % n different currents
Ivec= 5.6./Rvec;

%INTERPOLATION FIRST STEP - From mxn to m
[Xi,Yi]=meshgrid(f_hz,Ivec);
Tmag_db_inter_step1(1,:) = griddata(Xi,Yi,MV10,f_hz,Idesired);
Tmag_db_inter_step1(2,:) = griddata(Xi,Yi,MV20,f_hz,Idesired);
Tmag_db_inter_step1(3,:) = griddata(Xi,Yi,MV30,f_hz,Idesired);

Tph_deg_inter_step1(1,:) = griddata(Xi,Yi,PV10,f_hz,Idesired);
Tph_deg_inter_step1(2,:) = griddata(Xi,Yi,PV20,f_hz,Idesired);
Tph_deg_inter_step1(3,:) = griddata(Xi,Yi,PV30,f_hz,Idesired);

%INTERPOLATION SECOND STEP - From m to 1
[Xv,Yv]=meshgrid(f_hz,Vvec);
Tmag_db_inter = griddata(Xv,Yv,Tmag_db_inter_step1,f_hz,Vdesired);

Tph_inter = griddata(Xv,Yv,Tph_deg_inter_step1,f_hz,Vdesired);
```

where:

- `Vdesired` and `Idesired` are scalar variables inserted manually by the user. In the example reported below they are: `Vdesired` = 15[V] and `Idesired` = 5[A].

- The vectors `Vvec` and `Ivec` indicate the values of V_{in} − I_{load} at which the measurements has been taken. In the example reported they are: `Vvec` = [10, 20, 30][V] and `Ivec` = [6.54, 5.6, 3.5, 1.44, 0.56, 0.16, 0][A], then $m = 3$ and $n = 7$.

- The function `meshgrid` creates a matrix starting from the two input vectors, and for this project it creates a matrix of values at which the value of the loop gain has been measured.

- The function `griddata` calculates the interpolation in the way reported here, extrapolated from the Matlab Documentation:

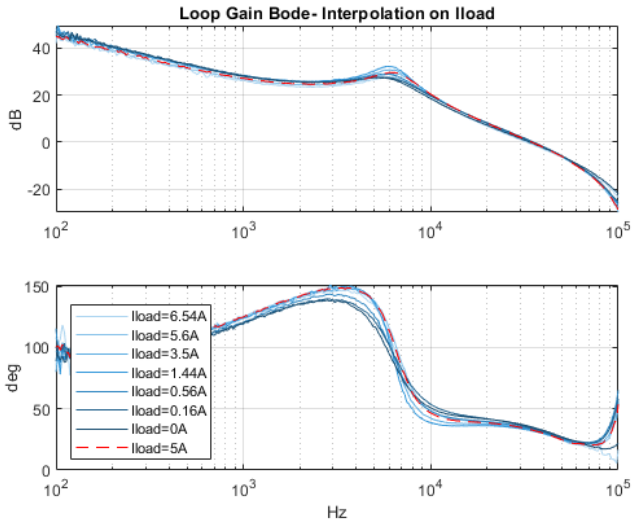
  vq = griddata(x,y,v,xq,yq) fits a surface of the form v = f(x,y) to the scattered data in the vectors (x,y,v). The griddata function interpolates the surface at the query points specified by (xq,yq) and returns the interpolated values, vq. The surface always passes through the data points defined by x and y.

  In particular, for the project case the variable v is represented by the measures acquired varying one of the two bias parameters and keeping the other fixed. As said in the first step of the interpolation procedure the value of the input voltage is kept fixed while the load current varies. This variable is then a vector of acquired measures and its name expresses which measures are contained in the following way:

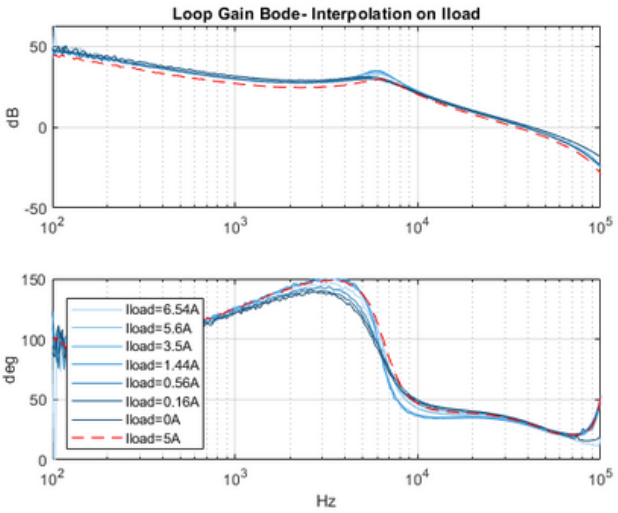
  - the first letter distinguishes the magnitude (`M`) from the phase (`P`);
  - the second letter `V` stands for (Input) Voltage, for remarking that it remains fixed;
  - the final number indicates the fixed value of the input voltage in volts.

An example of the results obtained is visible in the following Figure 2.17. In particular for what regards the first step it is possible to see the different measures in different shades of blue. They represents the loop gain at I_{load} variation, when the battery V_{in} instead remains fixed at the different values of `Vvec`. For each value of `Vvec` is then obtained a red dashed line that represent the loop gain at the desired value of I_{load}. The m red lines obtained, where again $m = |\texttt{Vvec}|$, are then used as input for the second step. In this way the current is set at the desired value, that is not a measured one. Finally, the interpolation between the obtained red lines allows to derive the green dashed one. It represents the final loop gain where the value of the battery and of the load current are set manually at the desired values. The only constraint that this procedure introduces is that these desired values have to belong to the ranges :

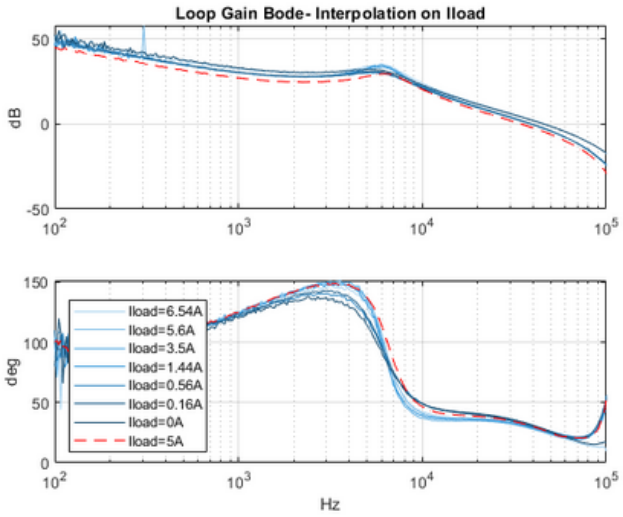
$$\begin{cases} \texttt{Vdesired} \in [min(\texttt{Vvec(i)}),\ max(\texttt{Vvec(i)})] & i \in \mathbb{N} \\ \texttt{Idesired} \in [min(\texttt{Ivec(j)}),\ max(\texttt{Ivec(j)})] & j \in \mathbb{N} \end{cases} \tag{2.3.1}$$



(a) V_{in}=10V



(b) V_{in}=20V



(c) V_{in}=30V

Fig. 2.17: First step of the interpolation procedure for V_{in} fixed. In red the predicted lines.

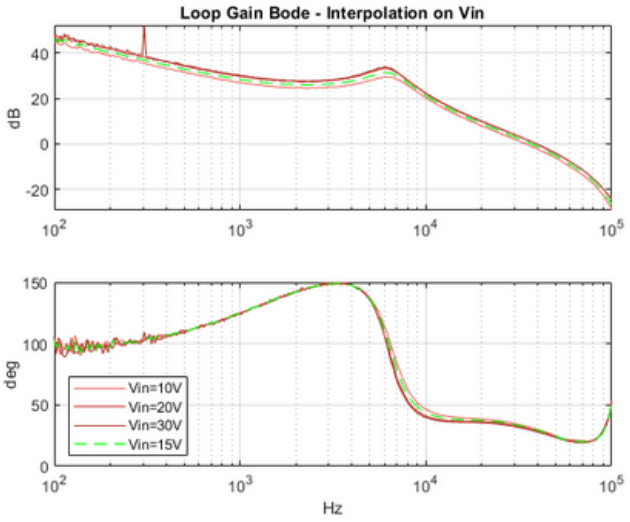


Fig. 2.18: Second step of the interpolation procedure. In green the predicted line.

2.4 Final Methodology Complete Flow

The total methodology explained up to here is now recapitulated for a better clarity to the reader. The steps that the technician has to make are the following:

- **Study the buck converter** circuit, understanding which part can be considered known and which one has to been treated in a black box way. The case studied consider the LC-filter as the only part known.
- **Derive the transfer function of the known part**, paying attention to consider also the Equivalent Series Resistances. In this project it results:

$$G_{vd} = V_g \frac{R_o}{R_o + r_L} \frac{sr_C C}{1 + s\left(\frac{L}{R_o+r_L} + \frac{C(R_o r_L + R_o r_C + r_C r_L)}{R_o+r_L}\right) + s^2\left(LC\frac{R_o+r_C}{R_o+r_L}\right)}. \quad (2.4.1)$$

- **Build an electrical board and organize the measurement set up**. The suggested set up involves use of the network analyzer and is well described above. The technician has to prepare also a set of passive components and be ready to substitute them on the board. In particular some power resistors are needed to change the load current and some inductors and capacitors to change the buck filter.

  Note: the power resistors must be enough big to be able to dissipate a lot of power, in fact the power that is present on the load resistor can reach high value. For the project case the output voltage is equal to 5.6[V] and the load current can be also equal to 10[A], so $P_{out} = V_{out} \cdot I_{load}$ has an upper bound of 56[W].

- **Collect a set of $m \times n$ measures**, where m is the number of different voltages and n the number of load current. The suggested value is at least 3 or 4 for both of them, so the interpolation procedure has enough arguments to deal with. This implicates a number of acquired measures equal to 15 more or less. The example reported above has $m = 3$ and $n = 7$ for a well tuning results. However the effort of these measurements is not so big because the voltage is easily modifiable simply rotating the power supply knob and the power resistor can be rapidly replaced with a predisposed board.

- **Collect the measures traces** (magnitudes and phases of the loop gains) **on Matlab and elaborate them to have predictions**. The prediction is divided in two steps: the interpolation of the measures and the calculation of the new LC-filter transfer function:

  - Interpolation of measures: it allows to obtain the loop gain imposing the desired input voltage and load current. The key code rows written for this aim are reported in the section 'Bias effects on stability'.

Figure	V_{in} $[V]$	R_{load} $[\Omega]$	I_{load} $[A]$	L $[\mu H]$	C $[\mu F]$
a	25	6	0.93	4.7	198
b	10	0.857	6.53	8.6	264
c	15	7.83	0.72	8.6	264
d	20	36	0.16	10	99

Tab. 2.6

  - Calculation of new LC-filter transfer function: it allows to prediction the small-signal behavior of the buck converter modifying the loop gain obtained in the previous step. This part is done completely on Matlab without the need of new measurements. It in fact exploits the mathematical transfer function obtained in the first point of this recap. It is well described in the section 'The prediction on LC variation'.

- Analyze the final loop gain obtained, in particular it is useful **detecting the crossover frequency and subsequently the phase margin**. Typically, if the latter is greater than 30 degrees the system can be considered quite stable, but this type of consideration must be based on the needs of the case.

2.5 Graphical Results

In the following figures there are some examples of results obtained with this methodology. The Figures 2.19 reports in fact the Bode plots of the final loop gains obtained with the prediction.

In the four examples reported it is possible to notice how the predicted loop gain fit the real ones. The prediction was done starting from the measurements executed at the `Vvec` and `Ivec` values of input voltage and load current, and with (nominal) value of $L = 5.6[\mu H]$ and $C = 165[\mu F]$. The examples reported cover a good range of different values for all the four parameters interested in the analysis, so the results can be considered satisfactory. The value of the different plots are reported in Table 2.6.

Some mismatches are visible between measures and prediction when at the resonant frequencies, where the behavior of the buck is changing rapidly with a double pole. This is however an acceptable drawback because for the stability evaluation what is most important is the behavior around the crossover frequency. The results obtained at that frequency are quite precise, like visible in the circles drawn in the plots.

2.5.1 Comparison between Mathematical Model and New Methodology

In Figure 2.20 is reported an example of loop gain Bode plot in three different versions. This comparison regards a measured loop gain, its simulated version, derived exploiting only the mathematical model and finally its predicted version. It is easy to see that the predicted line fit absolutely better the measured one, and this simple observation shows the

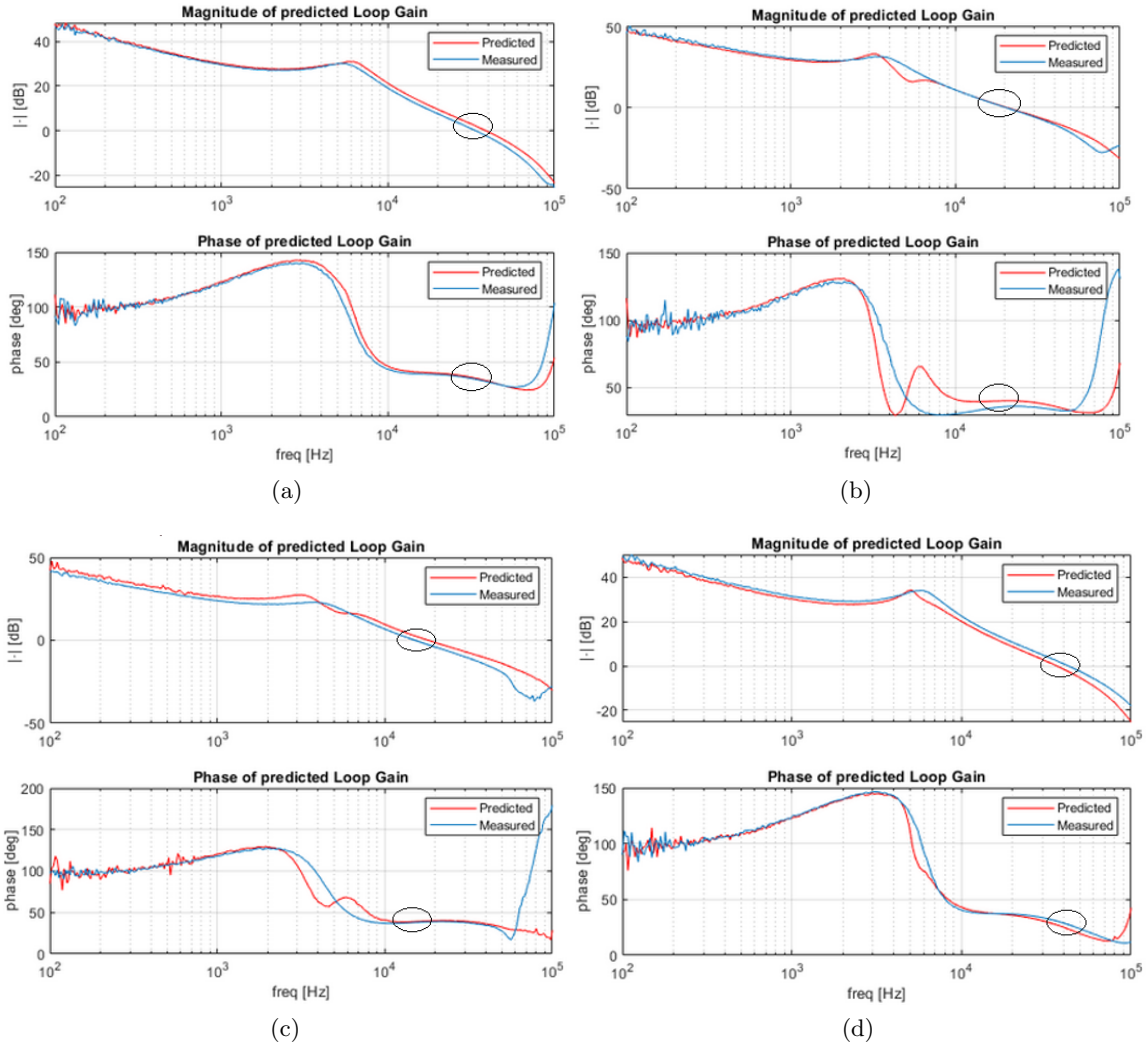


Fig. 2.19: Bode plots of four examples. In blue the loop gain measured and in red the same loop gain but predicted from different starting measures. For the respective parameters values see Table 2.6.

improvement introduced with the new hybrid methodology. The term hybrid indicates the fact that the proposed procedure is a composition of mathematical and black box model.

2.6 Possible Improvements

There could be different ways to improve or continue the project just described. Here some ideas and suggestion are exposed and developed in part. A first try could be of make a rigorous validation of the methodology proposed. This means that the example reported is not enough to consider the methodology perfectly working and replicable. A good idea could be to test the procedure with different types of buck converter or even more general DC-DC converters. In this way the results could be considered more reliable and truthful. Another interesting idea could be instead a sort of continuation of the project. The analysis has been done in AC domain, i.e. exploiting the transfer function obtained linearizing the system around a point of work, but if a more general analysis is required

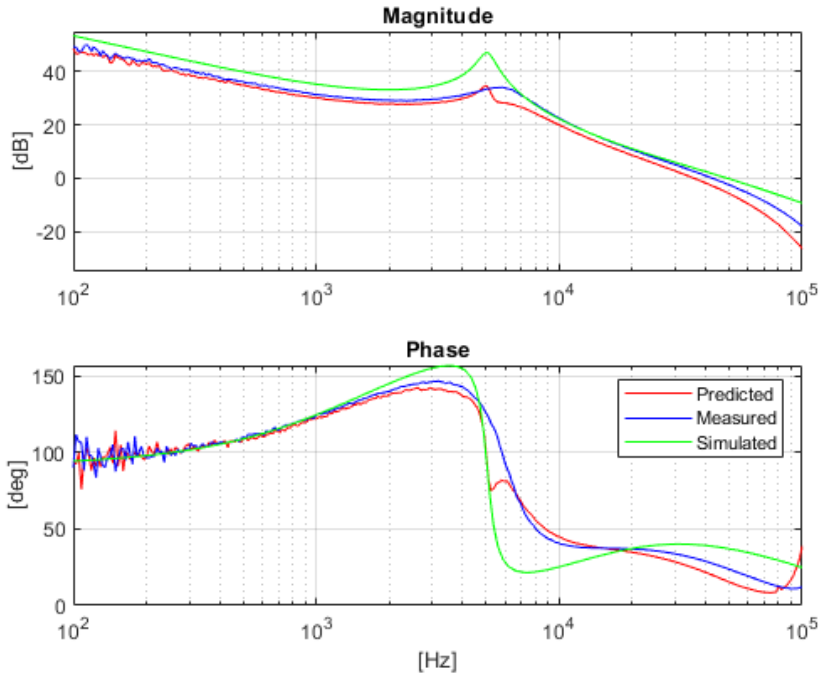


Fig. 2.20: Comparison between measured, mathematically simulated and predicted loop gain.

this strategy could bring some issues. A possible suggestion for resolving this problem could be to develop a sort of load step prediction, like explained in the next section.

2.6.1 Load Step Prediction

Load step prediction means that the prediction procedure involves also a large signal analysis, in the sense that the device is stressed with a big variation of the point of work. The load step procedure executed in laboratory has been already described in the first chapter, and here a prediction of this operation is proposed. The idea is to exploit the measurements already done to predict the time response of the system to a large variation of I_{load}. The general model of the buck is refresh in Figure 2.21.

The transfer function of interest has been defined with the letter $X(s)$, and it represents the transfer function from the load current to output voltage. Considering the other inputs off, $X(s)$ is given by the output impedance $Z_{out}(s)$ in series with the loop gain and then it results:

$$X(s) = -Z_{out} \cdot \frac{1}{1+T(s)}. \tag{2.6.1}$$

The transfer function $T(s)$ has been already measured (or eventually predicted), so the only additional effort is to measures the Z_{out}, but also this transfer function has been indeed measured. This measurement is in fact the same needed for obtaining the real value of the passive components. The only difference is that the network analyzer has to be set in a different way. In this case a bode plot is needed, with the same frequency range of the loop gain in order to allow calculation for points. An example of a measure of Z_{out} is reported in Figure 2.22, where $R_{load} = 1[\Omega]$, $L = 5.6[\mu H]$ and $C = 165[\mu F]$. It is worth

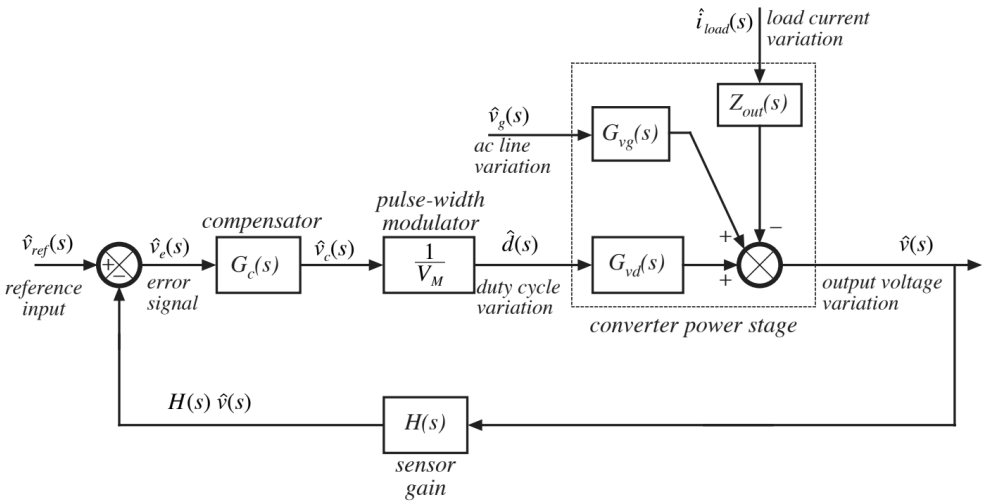


Fig. 2.21: Scheme of buck converter with focus on the load current to output voltage transfer function.

to notice that the magnitude does not represent a dB value but an absolute one.

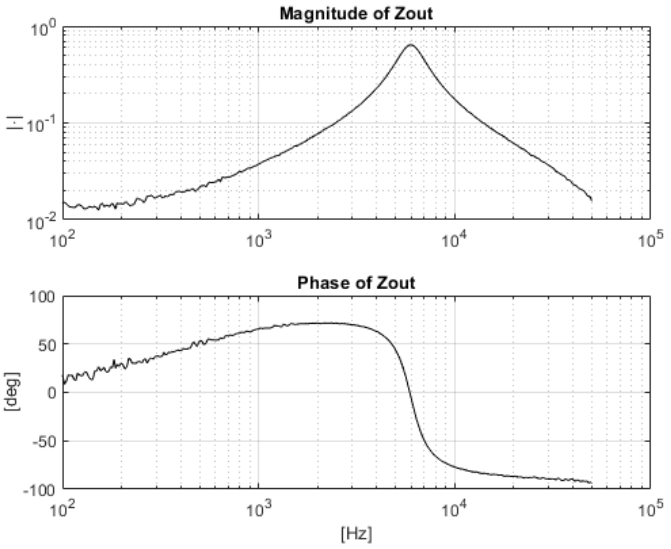


Fig. 2.22: Bode plot measure of Z_{out}, where $R_{load} = 1[\Omega]$, $L = 5.6[\mu H]$ and $C = 165[\mu F]$.

In this way it is possible to derive the function $X(s)$ and then its step response. In the Figure 2.23 it is possible to see an example of this prediction. Here it is reported the time response of the output voltage, in terms of variations from the steady value, in the face of an instantaneous large variation of the load current. In particular this current variation is equal to +5.6[A], done with a rapid change of the load resistor from an open circuit, i.e. $R_{load} = \infty$, to $R_{load} = 1[\Omega]$. There are three different graphs that represent: the measured response obtained with an oscilloscope, a predicted response exploiting the mathematical model and a prediction obtained exploiting the network analyzer measures. It is possible to notice that using the measures the results are quite good, while using the model they get worse, for this reason it is needed a more accurate study of the mathematical model and of the predicted loop gain. A possible strategy could also be to make a sort of hybrid

evaluation, i.e. exploit the direct measure of the impedance and the predicted loop gain.

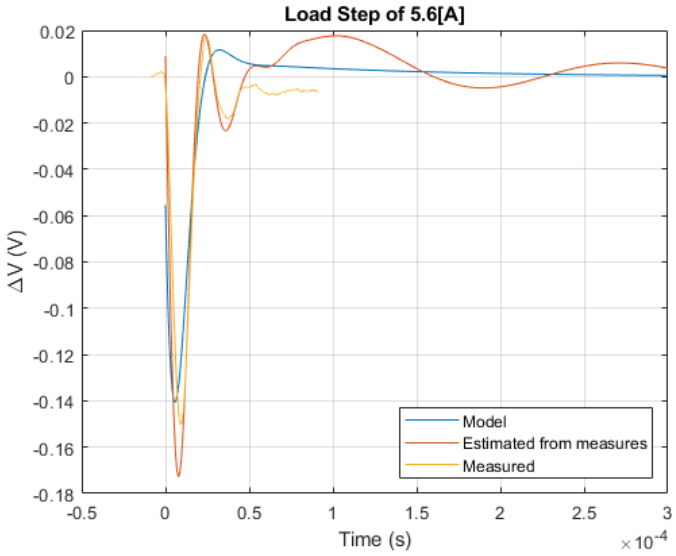


Fig. 2.23: Load step response: measured, predicted from network analyzer measures and predicted from mathematical model.

Bibliography

[1] A.Skandarnezhad, A.Rahmati, A.Abrishamifar, A.Kalteh, *Small-Signal Transfer-Function Extraction of a Lossy Buck Converter Using ASM Technique*, International Journal of innovative research in electrical, electronics, instrumentation and control engineering Vol. 2, 2014

[2] Wikipedia, https://it.wikipedia.org/

[3] Robert W. Erikson and Dragan Maksimovic, *Fundamentals of Power Electronics*, 2nd edition, 2001.

[4] Keysight Technologies, *Evaluating DC-DC Converters and PDN with the E5061B LF-RF Network Analyzer*, https://www.keysight.com , 2014.

[5] Roland van Roy, *DC/DC Converter Testing with Fast Load Transient*, https://www.richtek.com, 2016.

[6] Francesco Verenini, *Metodologia per la valutazione della stabilita' dei regolatori di tensione mediante misura di impedenza*, Thesis at University of Padua, 2013.

[7] Mohamed Nabeel Haris Marikkar, *Systematic Methodology and Predictive Model for Linear Voltage Regulator Stability Evaluation*, Thesis at University Sapienza of Rome, 2017.

[8] Infineon Technologies AG , *TLF51801ELV - 10 A synchronous DC/DC Step-Down Controller*, https://www.infineon.com, 2013.

[9] Infineon Technologies AG , *TLF50211ELV50 - 2.2 MHz Step-Down Regulator 500 mA, 5 V, low quiescent current*, https://www.infineon.com, 2018.

[10] Flaibani Marco, *Phase Margin calculation*, Documents of Infineon Technologies Italia S.r.l., 2004.

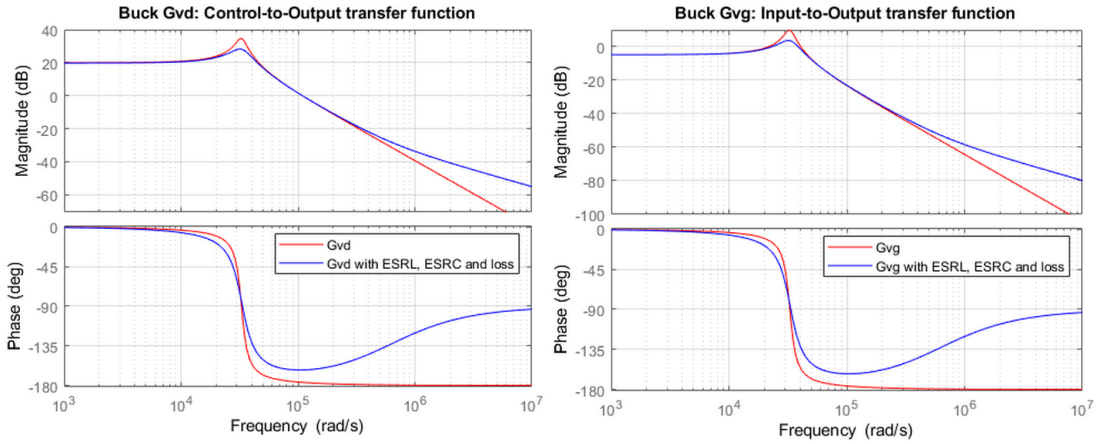
[11] Picotest,*J2101A Injection Transformer 10Hz - 45MHz*, https://www.picotest.com, 2011.

[12] Picotest,*J2111A Current Injector*, https://www.picotest.com, 2011.

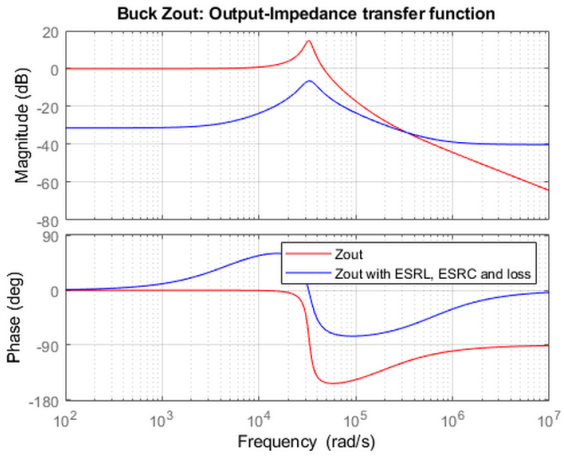
Appendix A

Matlab Model of the specific buck

Here the transfer functions elaborated in Matlab are reported in the form of Bode plots. In particular they are reported both the ideal case and the more accurate version that includes the losses (Figure A.1). Finally the loop gain is reported, both in the original version and in the compensated version. The total compensation reported correspond to the product between $G_c(s)$ and $H(s)$ (Figure A.2).

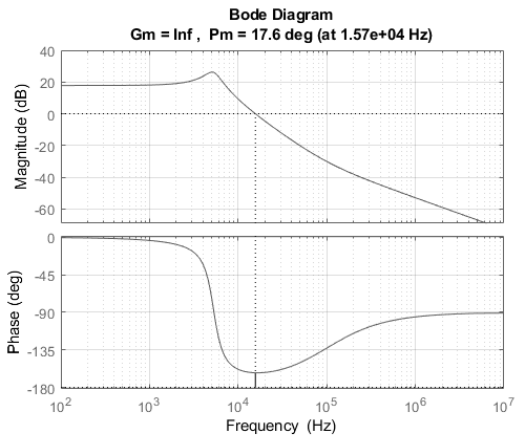


(a) Control-to-output transfer function $G_{vd}(s)$. (b) Input-to-output transfer function $G_{vg}(s)$.

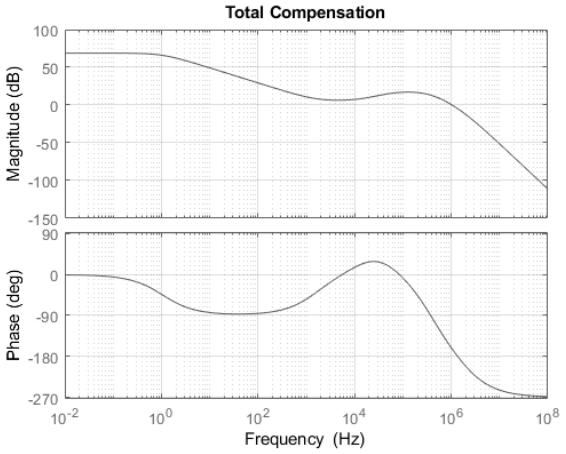


(c) Impedance transfer function $Z_{out}(s)$.

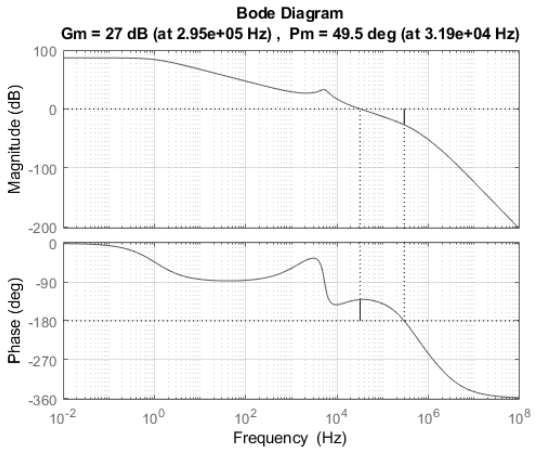
Fig. A.1: Bode plots of mathematical model transfer functions.



(a) Uncompensated loop gain $T_u(s)$.



(b) Compensation: $G_c(s) \cdot H(s)$.



(c) Compensated loop gain $T(s)$.

Fig. A.2: Bode plots of mathematical model: loop gain uncompensated, its compensation and the result.

Appendix B

Stability of Linear System

A system is said to be stable, if its output is under control. This means that the system is able to receive input changes without altering excessively its output. Roughly speaking, if a system is stable, a perturbation on the input, in the initial state or in the characteristic parameters of the system, generates changes that tend to decrease increasing the time. For what regards the linear and time invariant system the output response $y(t)$ to a perturbation depends on the modes associated to the transfer function of the system. The response behavior is a consequence of the modes of this function, depending on the poles of the system (the roots of the denominator). From the theory, there are three types of responses that are based on the positions of the poles in the Gauss plane.

- Response asymptotically converging to zero: there exists a constant $M > 0$, big enough but finite, such that:

$$|y(t)| \leq M \quad \forall t \geq 0 \quad \text{and} \lim_{t\to\infty} |y(t)| = 0 \tag{B.0.1}$$

  In this case the system is asymptotically stable. The necessary and sufficient condition is that the transfer function has all the poles with negative real part.

- Limited response: there exists a constant $M > 0$, big enough but finite, such that:

$$|y(t)| \leq M \quad \forall t \geq 0. \tag{B.0.2}$$

  In this case the system is critically stable. The necessary and sufficient condition is that the transfer function has one or more poles with real part null.

- Diverging response: there not exists a constant $M > 0$ that limits the response amplitude. In this case the system is unstable. The necessary and sufficient condition is that the transfer function has at least one pole with positive real part.

B.1 Feedback System

A feedback loop is a common and powerful tool when designing a control system. Feedback loops take the system output into consideration, enabling the system to adjust its performance to meet a specified output response. The typical negative feedback scheme is the one in Figure B.1. The closed loop transfer function results:

$$G(s) = \frac{A(s)}{1 + A(s)B(s)} = \frac{A(s)}{1 + T(s)} \tag{B.1.1}$$

where $T(s)$ is the so called loop gain. The assessment of the system stability can be carried out evaluating the poles of the denominator of the closed loop system $D(s) = 1 + T(s)$.

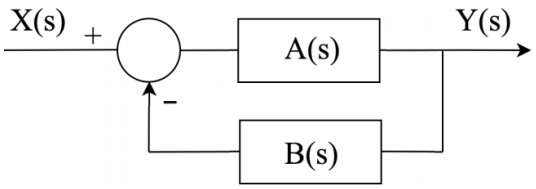


Fig. B.1: Negative feedback system

In the thesis has been used the Bode stability criterion that determine the stability of a feedback system studying directly the loop gain $T(s)$ on the Cartesian diagram. This criterion can be applied only if these hypothesis holds:

- The open loop transfer function $T(s)$ is in a stable condition.
- The feedback system must be a negative feedback system.
- The system is minimum phase system, i.e. also the zeros of the system have negative real part.

Bode Criterion : an open loop system, stable and with minimum phase, is stable even with closed loop, if at crossover frequency of the open loop transfer function, its absolute phase is less than 180°.

In practical applications, it is necessary to evaluate the theoretical stability of a system and define the margins of safety, because the system has to be stable even if an unwanted disturbance is present and/or variations of one or more parameters can determines, as for example, a gain boost. The parameters for evaluating the degree of stability of a system are the phase margin and gain margin. The phase margin is the amount of phase required to reach the stability limit, this margin is uniquely defined for system that have only one crossover frequency. The mathematical definition of crossover frequency f_C, phase margin φ and gain margin γ are the following:

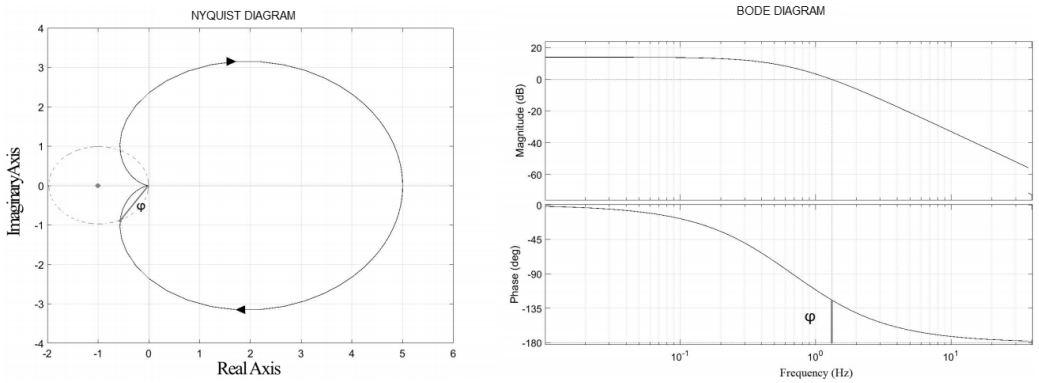
$$\text{Crossover Frequency:} \quad f_C : \ ||T(2\pi j f_C)|| = 1 = 0dB \tag{B.1.2}$$

$$\text{Phase Margin:} \quad \varphi_m = 180^\circ + \angle T(2\pi j f_C) \tag{B.1.3}$$

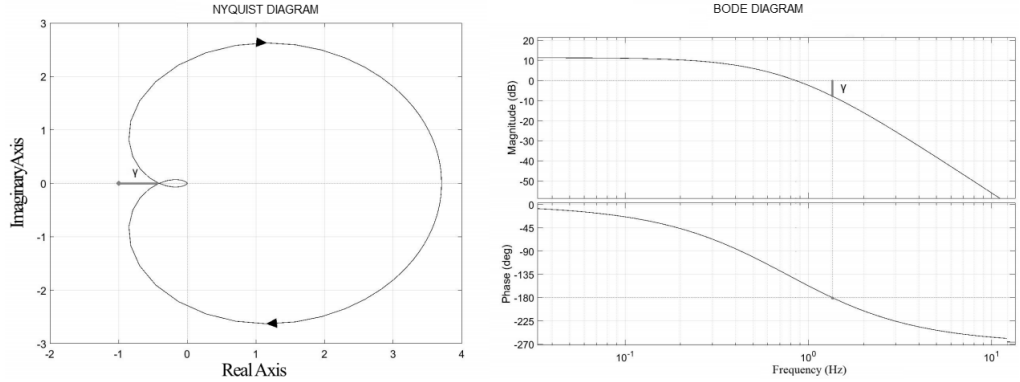
$$\text{Gain Margin:} \quad \gamma = \frac{1}{|T(2\pi j f_G)|} \tag{B.1.4}$$

where f_G is the smallest frequency at which the phase of the loop gain function is $-180°$. It represents how much the controller gain can be increased before reaching the instability limit. Two simple examples are reported in Figure B.2 for clarifying the meaning of these parameters.

In the thesis the stability has been evaluated in reference to the value of the phase margin. The desired value is at least 30/35°.



(a) Phase Margin.



(b) Gain Margin.

Fig. B.2: Phase Margin and Gain Margin on Nyquist and Bode diagram.

B.2 Phase Margin Calculation for Second Order System

There exists a relation between the phase margin of a second order system and its step respons. In the following this relation is derived. A second order system can be writen, in Laplace domain, like:

$$W(s) = \frac{O(s)}{I(s)} = \frac{K\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{B.2.1}$$

and the step response results being:

$$W(s)\frac{1}{s} = \frac{K\omega_n^2}{s(s^2 + 2\xi\omega_n s + \omega_n^2)} = \frac{K}{s} - \frac{K(s + \xi\omega_n)}{(s + \xi\omega_n)^2 + \omega_n^2(1 - \xi^2)} - \frac{\frac{K\xi}{\sqrt{1-\xi^2}}\omega_n\sqrt{1 - \xi^2}}{(s + \xi\omega_n)^2 + \omega_n^2(1 - \xi^2)} \tag{B.2.2}$$

that brings to the time evolution:

$$o(t) = K - \frac{K}{\sqrt{1 - \xi^2}} e^{\xi\omega t} \sin\left(\omega_n\sqrt{1 - \xi^2}t + \arctan\left(\frac{\sqrt{1 - \xi^2}}{\xi}\right)\right) \tag{B.2.3}$$

The purpose is to find the peaks, i.e. $\frac{do(t)}{dt} = 0$, it results:

$$\dot{o}(t) = \frac{K\omega}{\sqrt{1 - \xi^2}} e^{-\xi\omega_n} \sin(\omega_n\sqrt{1 - \xi^2}t) = 0 \tag{B.2.4}$$

that is verified in:

$$t = \frac{M\pi}{\omega_n\sqrt{1-\xi^2}} \quad M \in \mathcal{Z}. \tag{B.2.5}$$

It is now possible to calculate the ratio between consecutive peaks:

$$c = \frac{o(t_1) - o(t_2)}{o(t_3) - o(t_2)} = e^{\frac{\xi}{\sqrt{1-\xi^2}}\pi} \tag{B.2.6}$$

that can be inverted in the domain $\xi \in [0, 1]$, obtaining:

$$\xi = \frac{\ln(c)}{\sqrt{\ln^2(c) + \pi^2}}. \tag{B.2.7}$$

So now there is a relation between the peaks of the step response and the parameter ξ that characterizes the second order transfer function. At this point it is derive a relation between ξ and the phase margin of a feedback system, and so, for the transitive property, a relation between the step response and the phase margin is obtainable.

In particular, supposing that the open loop system has transfer function:

$$A(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s} \tag{B.2.8}$$

and that the feedback function is unitary, $B(s) = 1$, the closed loop transfer function results:

$$G(s) = \frac{A(s)}{1 + A(s)B(s)} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \tag{B.2.9}$$

The loop gain is $T(s) = A(s)B(s)$ and it is necessary to find where its magnitude is unitary:

$$|T(s)| = \frac{\omega_n^2}{\sqrt{\omega^4 + 4\xi^2\omega_n^2\omega^2}} = 1. \tag{B.2.10}$$

Squaring and rearranging gives:

$$\omega^2 = \omega_n^2(-2\xi^2 + \sqrt{4\xi^2 + 1}). \tag{B.2.11}$$

The phase margin at this frequency results being:

$$PM = \arctan\left(\frac{2\xi}{\sqrt{-2\xi^2 + \sqrt{4\xi^2 + 1}}}\right) \tag{B.2.12}$$

and this is the desired relation to obtain the phase margin from the step response of the system.

Appendix C

Instruments used

C.1 Network Analyzer - Agilent VNA E5061B

A Network Analyzer is a tool used to analyze the properties of electricity networks, especially the behavior associated with the reflection and transmission of electrical signals. They are used mainly for high frequencies (from few kHz to several GHz). There are mainly two types: Scalar Network Analyzer, that scans only the amplitude of the signals, and Vector Network Analyzer, that instead analyzes both the amplitudes and the phase of signals. The main concept of high-frequency network analysis involves incident, reflected and transmitted waves traveling along transmission lines.

The network, in fact, measures the ratios of the reflected signal (R) of the device under test (DUT) in respect of the incident signal, and the transmitted signal (T) with the incident signal. In order to characterize an unknown linear two-port device, it is necessary to test it under various conditions and compute a set of parameters. The total voltage at the input or output port of a device or the current at the nodes of a network must be measured. Since it is difficult to measure the total current or voltage at higher frequencies, the scattering (S) parameters are generally measured. The number of these parameters is equal to the square of the number of ports (there are then 4 S-parameters for a two-ports device, like Figure C.1).

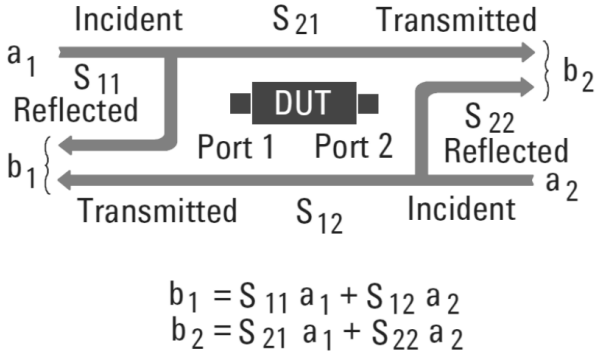


Fig. C.1: Scattering parameters for two-ports device

The measurements reported in this thesis were performed by using the Vector Network Analyzer Agilent E5061B, that allows to operate in a frequency range of 5 Hz - 3 GHz. In order to operate at low frequencies, there are three additional ports, called T, R and LF OUT (see Figure C.2).

The LF OUT port provides output, in fact it is connected to an internal oscillator and so it allows to inject a sinusoidal wave into the DUT. It has 5 Hz and 30 MHz as lower and upper frequency limit respectively. The other ports are instead the input ones (T stand for transmitted, R stand for received). They measures the complex signal at which

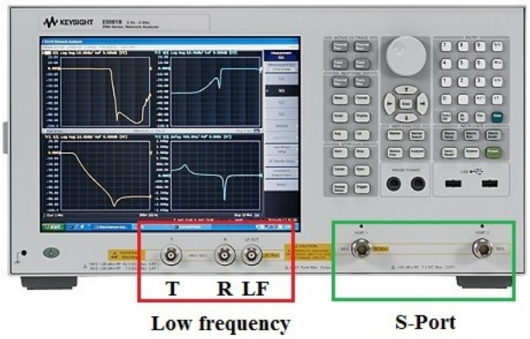


Fig. C.2: Photo of VNA Agilent E5061B.

they are connected in voltage form. The tool allows to directly calculate the ratio between this two signals, and in this way it is possible to obtain the bode of the desired transfer function. In fact, if the probes of these input ports are correctly connected to the network, one has the ratio $\frac{V_{out}(s)}{V_{in}(s)}$, that is the definition of transfer function.

An important part of the measurement with the network analyzer is the calibration. It is important to keep in mind that every measurement is subject to measurement uncertainly, which is the statistical deviation of the measured values from their true value. Calibrating a VNA is possible to remove the largest contributor to measurement uncertainties, which are systematic errors. Systematic errors are repeatable, non-random errors that can be measured and removed mathematically. A vector-error-corrected VNA system provides the best picture of the true performance of the device under test (DUT). A network analyzer measurement is true only as good as is its calibration. There are two types of calibration: SOLT (short, open, load, thru) and TRL (thru, reflect, line). The differences in the calibrations are related to the types of calibration standards they use and how the standards are defined. TRL calibration, or Thru calibration is a directly connection between the two reading ports. Input ports must read the same value in order to have a good measure, otherwise it is applied a corrective factor, which will be the calibration itself. TRL calibration, when properly implemented, can be extremely accurate, which is helpful because SOLT standards in a connectorless environment are much more challenging than TRL standards to be implemented. SOLT calibration is perhaps the most familiar and more precise of all VNA calibrations. It uses a well-defined short, open, and load (of characteristic impedance, usually 50Ω) DUTs. One by one, the reference DUTs are connected to the VNA that can measure them. When these three steps are completed, the two reading ports are connected together to form a through (thru) connection for the final measurement.

C.2 Balun Transformer - Picotest J2101A

The key features of the balun transformer used in laboratory for injecting an AC signal in the loop gain of the converter, are listed in the following table, taken from the product specifics sheet on Picotest website.

Performance at -10dBm input level		
Characteristics:	**Rating:**	**Conditions:**
DCR		25 degC
Ratio	1:1	
Termination Impedance	5 Ohms	
Nominal 3dB Bandwidth	10Hz-45 MHz	100mHz~100Hz, 10Hz~500MHz
Isolation Voltage	600V / CATII	3kVrms/1min
Isolation Capacitance	150pF	1kHz
DC Current	10mA	DC current at which inductance (@1kHz) drops 10% (typ) from its value without current
Temperature Range	0 - 50C	
Maximum Altitude	6000 Ft	

Fig. C.3: Balun - Picotest J2101A specifics.

C.3 Current Injector - Picotest J2111A

The key features of the current injector used in laboratory for the impedance measurement are listed in the following table, taken from the product specifics sheet on Picotest website.

Specifications		
Characteristic	**Typical**	**Units**
Output Current Variation (Controllable)	50	mA
Total Output Current Variation (Controllable+Bias)	74	mA
Max input voltage DC+AC	+/-5	A / V
Output voltage	40	V
Current Monitor	1	V / A
Modulator Gain	10m	A / V
Offset Current (typical)	+24m/0/-24m	A
Usable Bandwidth	DC-40M	Hz
Temperature Range	0 - 50	C
Maximum Altitude	6000	Ft

Fig. C.4: Current Injector - Picotest J2111A specifics.

Appendix D

Graphic Interface

The final step of the project was to build a smart graphic interface that allows to some user to predict the stability without the need of using a less intuitive Matlab code written by somebody else. For this purpose some code rows have been written on the Matlab tool *App Design*. It allows to create a nice and clear interface with easy buttons and with the possibility of uploading files. Here some screenshots are reported (Figure D.1, D.2, D.3).

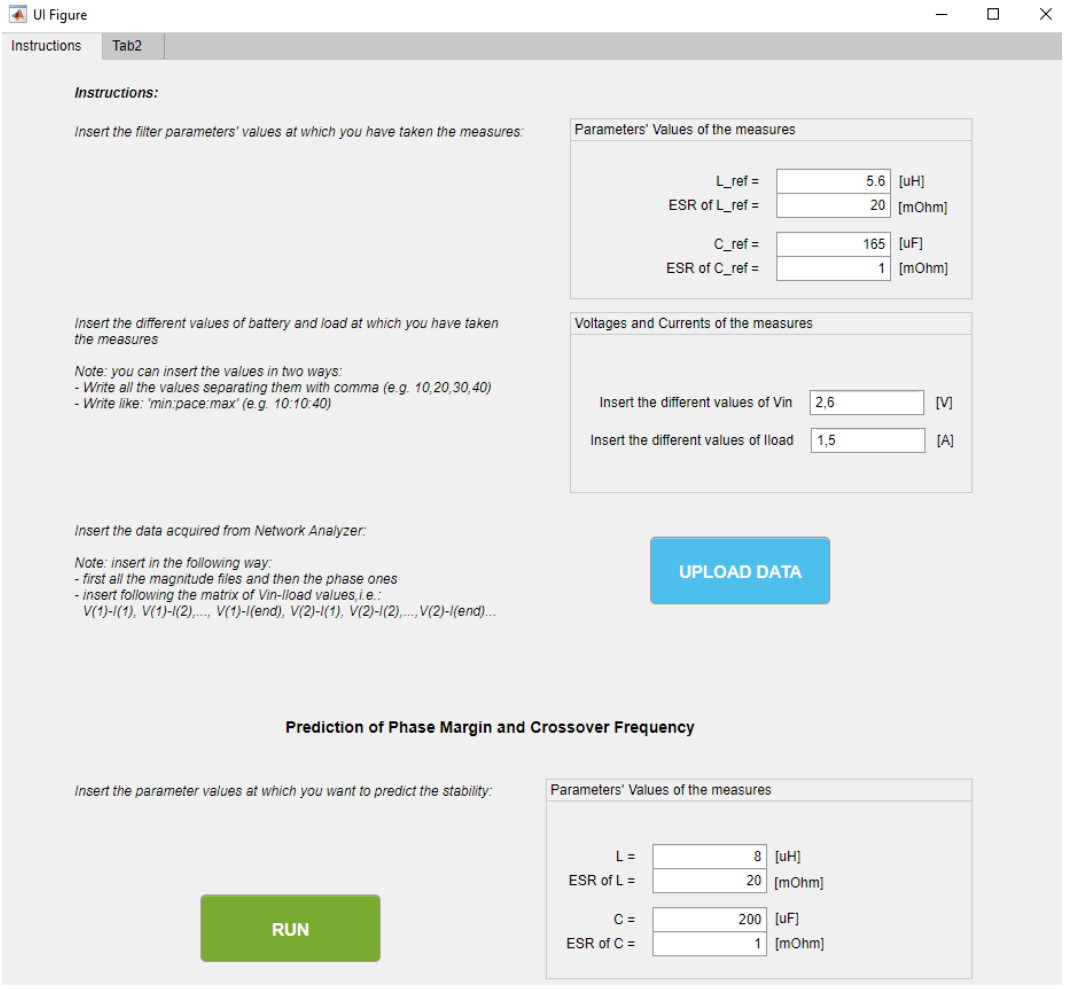


Fig. D.1: Screenshot of graphic interface: initial tab where the acquired measures can be loaded.

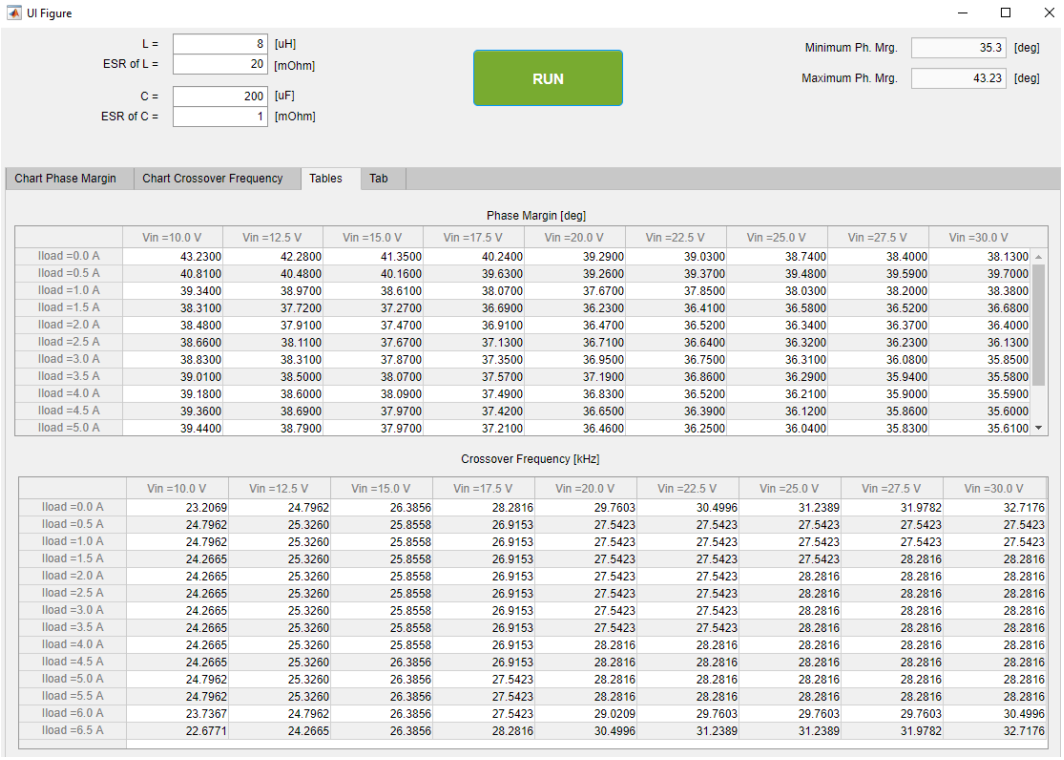


Fig. D.2: Screenshot of graphic interface: prediction results in table form.

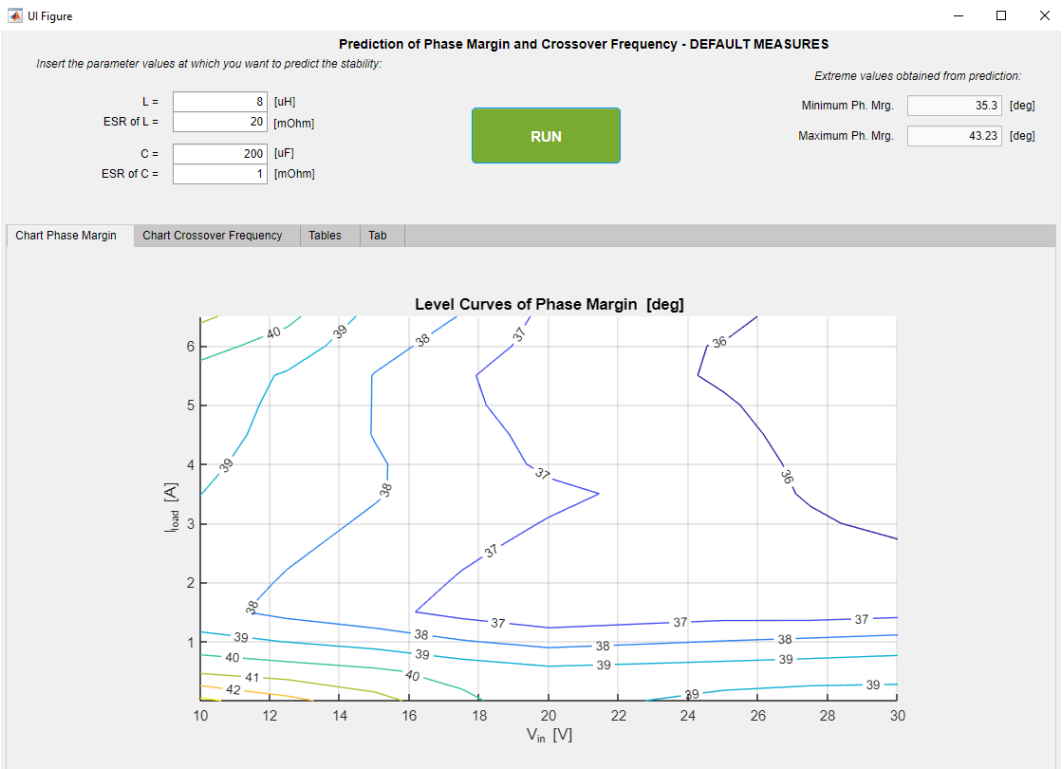


Fig. D.3: Screenshot of graphic interface: prediction results in level curves form.

Special thank goes to my parents and my brother for the constant support given to me during all my school career.

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