UNIVERSITÀ DEGLI STUDI DI PADOVA

FACOLTÀ DI INGEGNERIA

CORSO DI LAUREA MAGISTRALE IN INGEGNERIA ELETTRONICA

Design of a 10GHz IF-receiver for backhaul gbit point to point communication link in SiGe bipolar technology

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July 2012

Acknowledgements

I want to thank Prof. Andrea Bevilacqua, thesis supervisor, and my tutors at Infineon Austria, Dr. Marc Tiebout and Dr. Koen Mertens.
Special thank goes to my parents and my brother, who always supported me.
Finally, many thanks to Leonardo, with whom I have shared this adventure, for the help he gave me.

Tommaso Pieretti

Contents

Abstract

Due to rapid technological evolution and the strong increase of people and devices using data connections, structures that support the network begin to present limits that are no longer ignorable. Optical fiber is widely used to replace or enhance the backhaul infrastructure, thanks to the enormous data stream that it is able to convey. Unfortunately the installation presents high costs and often requires long periods of time due to the difficulty of the wiring in complex urban environments. A commonly adopted solution are wireless point-to-point communication links. Original signal is up-converted to high frequencies, outside the range of normal communications (tens of GHz), transmitted to the receiver for down-conversion and redistributed to the network. Transceivers can be placed on building top and, thanks to their directionality, coexist with many other links. In this work an E-band heterodyne receiver design (71-76 GHz or 81-86 GHz) will be discussed, focusing on the conversion from the intermediate frequency of 10 GHz to baseband by using a quadrature mixer. Analysed circuits are a low noise amplifier, the quadrature mixer and programmable gain amplifier. The first two blocks have been redesigned, the last block has only been simulated to report its performance and characteristics. Initial goal was to verify whether it is possible to build a complete channel device which, when connected to source and load with 100 Ohms impedance, shows variable gain in the range 12-70dB, maximum noise figure of 3.5 dB and IIP3 higher then 3dBm. As simulations have shown that it was not possible to obtain the required linearity, it has been decided to develop separate test-chips for LNA and mixer. Both circuits are designed to work with 100Ωs-differential sources and load. LNA has a simulated -2 dB bandwidth of 4 GHz centred at 10 GHz). It adopts a supply voltage of 3.3 V, has a current consumption of 43 mA and implements a programmable gain, 6.8 dB or 13.4 dB. Noise figure is 2.8 dB at 10 GHz and IIP3 has a value of 4.7 dBm (in high gain configuration).
The quadrature mixer is designed to work with $f_{LO} = 10GHz$ and f_{RF} from 9 to 11GHz. It adopts two supply voltages: 3.3V for the LO driver circuits and 5V for mixers and output buffers. It has a current consumption of 37.4mA@3,3V and 162.6mA@5V, and shows a gain of 8.2dB. DSB noise figure and IIP3 are respectively 10.9dB and 15.1dBm. Image rejection is around -37 dB. All this data are related to an LO input power of 0dBm.

Chapter 1

Introduction

This chapter introduces in the first section the W-band transceiver, where and why it is used, concentrating on backhaul application; particular attention is given to the subsystem represented by the receiver at 10 Ghz, its characteristics and fields of use.
The second section gives some basic concepts and definitions useful in understanding the work done. Finally third section presents the theory behind the receiver and circuit topologies used in the design phase.

1.1 Overview

Wireless transmissions are at the center of technological development due to strong demand for high-speed data connections. New communication standards are needed. Next communication technology step is *4G* (*fourth-generation*) represented by two standards: *LTE* and *WiMAX*.
With Long-Term Evolution (LTE) cellular networks forthcoming and WiMAX already expanding, the weakness in 4G systems is the **backhaul** [1].

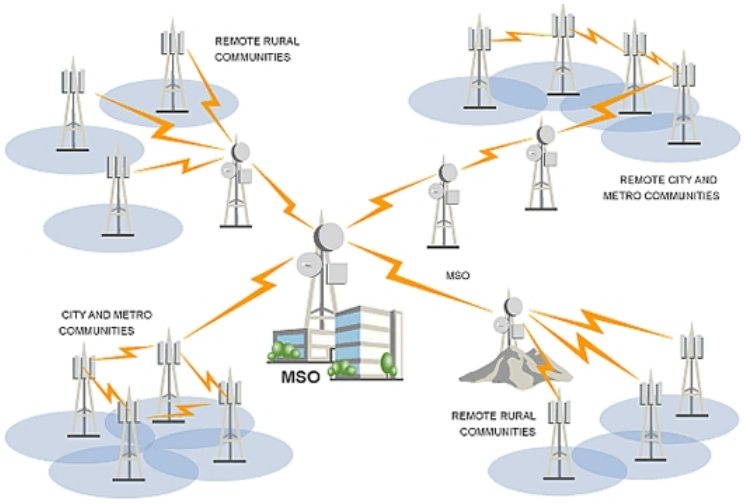


Figure 1.1: Example of network using backhaul connections.

In a hierarchical telecommunications network the backhaul portion of the network comprises the intermediate links between the core network, or backbone, and the small subnetworks at the "edge" of the entire hierarchical network [2]
. These systems are generally used in the cities to provide data connections to all the devices. Many options are available talking about the media used for these connections. Less expensive one is copper wire, used in many cities for the telephone network, but the performances are not enough to ensure the enormous stream of data needed. Another solution is optic fiber, the best one looking at performance. The problem are the installation costs of the cables (100k-500k/km,[3]), in particular in a big city.

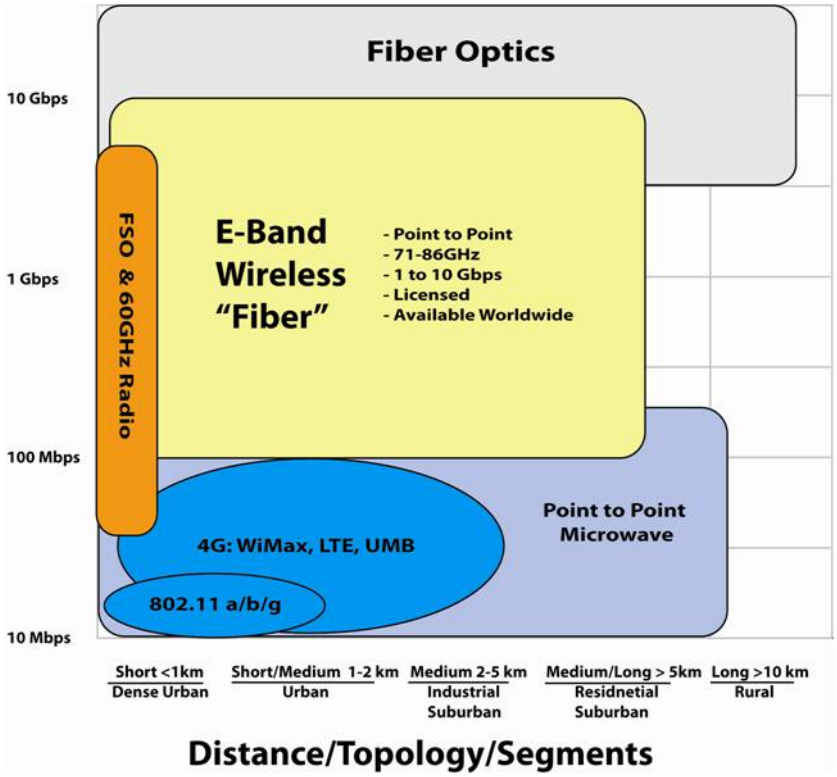


Figure 1.2: Utilization of the various technologies based on data volume and distance.

The last and best solution is point-to-point wireless transmission (microwave links). Costs are lower, installation doesn't need much time and is less problematic for the citizens. Right now about 85% of all backhaul connection in the U.S. is by multiple T1/E1 wirelines (typical Ethernet cables) with roughly 10% fiber and 5% microwave links. While T1 lines are basically adequate for 3G, they can no longer deliver the data throughput necessary for the new 4G systems. And it is often difficult to get the right of way, much less afford the cost of fiber.
The trend is to follow the European model where over 70% of backhaul is microwave. But even that is getting difficult. The traditional microwave bands devoted to backhaul (6 to 38 GHz) are filling up, and in big cities and metro areas there is already an interference problem or lack of additional space and licenses. The solution is to push higher into the

spectrum. That is why there are multiple 60-GHz backhaul solutions on the market and a growing presence of 80-GHz systems (E-band)[1]. 80 GHz links are most appropriate for urban backhaul scenarios, where gigabit capacities are most needed and where required backhaul distances are consistent with 80 GHz link deployments at 99.995% or better availability at up to 2 miles (3 kilometers). In Europe it is interesting to note that 80 GHz link operating at full gigabit data rates offer virtually identical link distances availabilities as 38 GHz links operating at only 311 Mbps. Another benefit that 80 GHz brings to dense urban deployment scenarios is the ability to deploy a very large numbers of high-capacity links within a given geographic area. The combination of a very large spectrum allocation (10 GHz) coupled with tightly focused antenna beam-widths provides for virtually unbounded link deployment densities. The fact that high data-rates can be realized using low-order modulation (e.g. QPSK or 16QAM) with 80 GHz links supports much shorter frequency re-use distances than is possible using high-order modulation in lower frequency bands, further improving maximum link deployment densities. Several country spectrum regulators view 80 GHz links as a means for addressing lower-frequency congestion issues that are becoming increasingly common in major urban areas as the number of cellular base station sites grows [4].
Digital signal used to transport data has to be up- converted to E-band by a transmitter and down-converted the baseband by the receiver. This is an analogue modulation provide by the typical super-heterodyne structure. Next subsection will explain function and required characteristics for the receiver.

1.1.1 E-band transceiver

The demodulation is done in two steps, a first down-conversion from E-band (71-76 GHz or 81-86 GHz) to an intermediate frequency, IF, in this case equals to 10 GHz, then a second down-conversion from intermediate frequency to the baseband. The scheme in Figure 1.3 shows the structure of the system. The mixers are preceded by an LNA to enhance the final signal-to-noise ratio. This because LNA introduces much less noise then the mixer and strongly amplify the signal. The bigger signal at the input of the mixer is less affected by noise introduced by this circuit, thus maintaining a good SNR. After the first process of down-conversion the signal is filtered to limit the bandwidth to the desired signal (9-11 GHz). Components outside this bandwidth can affect the second down-conversion output overlapping the original signal. Filtered signal becomes the input of the second stage of down-conversion. Unlike the first, the second stage uses a quadrature mixer to enable complex demodulation. At the output of each branch of the mixer there is a programmable gain amplifier to amplify baseband signal. In this stage is possible to regulate the gain in a wide range with a step of some dBs. A VCO (voltage controlled oscillator) signal is used as LO of the two down-converters, properly multiplied

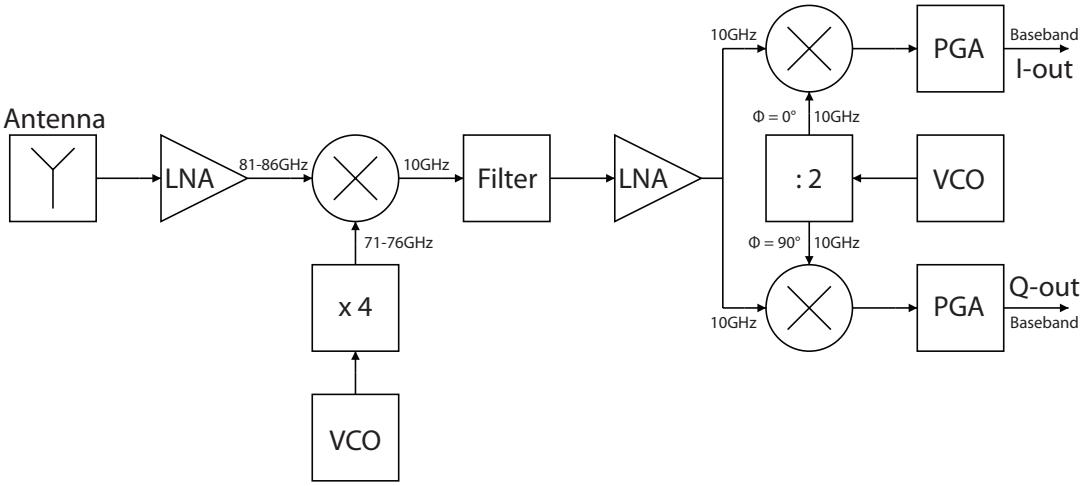


Figure 1.3: RF section of a E-band receiver.

or divided. The signal transmitted by the system is digital and usually modulated using complex schemes (16QAM, 64QAM, ...) which involve more complicated transceiver and significantly higher power consumption but enable really high data rates and many channels.

1.1.2 X-band down-converter

The design will concentrate on this circuit that performs the conversion from the intermediate frequency of 10 GHz to the baseband. Table 1.1 summarizes most important requests for this component.

parameter	**min**	**typ**	**max**	**unit**	**conditions**
Gain	12.0	-	70.0	dB	T=27℃, $f_{OUT} = 10.GHz$
Noise figure	-	-	3.5	dB	T=27℃, $f_{OUT} = 10.GHz$
IIP3	3.0	-	-	dBm	T=27℃
Center frequency	-	10.0	-	GHz	
Baseband BW	0.5	-	-	GHz	-1dB attenuation

Table 1.1: Performance required initially for the X-band downconverter.

Technology used is **200 GHz SiGe bipolar process of INFINEON**.
The system has 3 blocks which will be discussed in section 1.3: low noise amplifier (LNA), Gilbert double-balanced mixer and two programmable gain amplifier (PGA). Gain, noise figure and linearity become really important to provide a good signal to the digital section of the receiver.
Digital modulation scheme commonly used in this systems are PSK (Phase-shift keying) and its evolution, QAM. They convey data by changing, or modulating, the phase and the amplitude of a reference signal (the carrier wave) [5]. Figure 1.4 shows how different

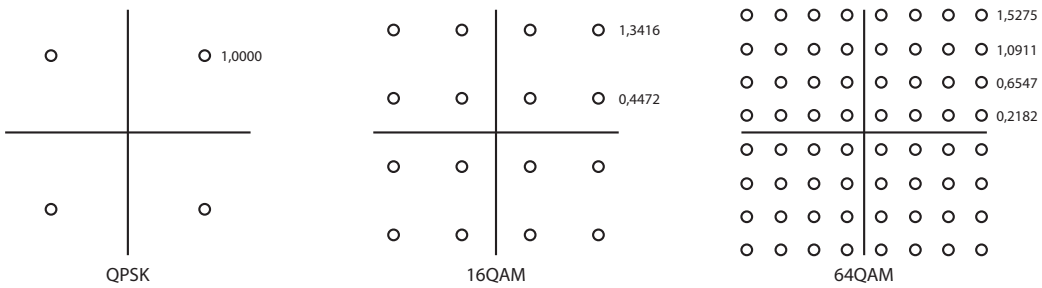


Figure 1.4: QPSK, 16QAM and 64QAM modulation schemes on complex plane.

binary words are mapped in a PSK modulation. Looking at the 64QAM it is evident how close two different words are. Distortion of the signal, in phase and amplitude, due to non-linearity or noise introduced by the system can produce incorrect detection of the symbol. So the characteristics of the down-converter previously indicated directly affect the bit-error rate (BER) of the transmission system.

1.1.3 Competitiveness of bipolar technology

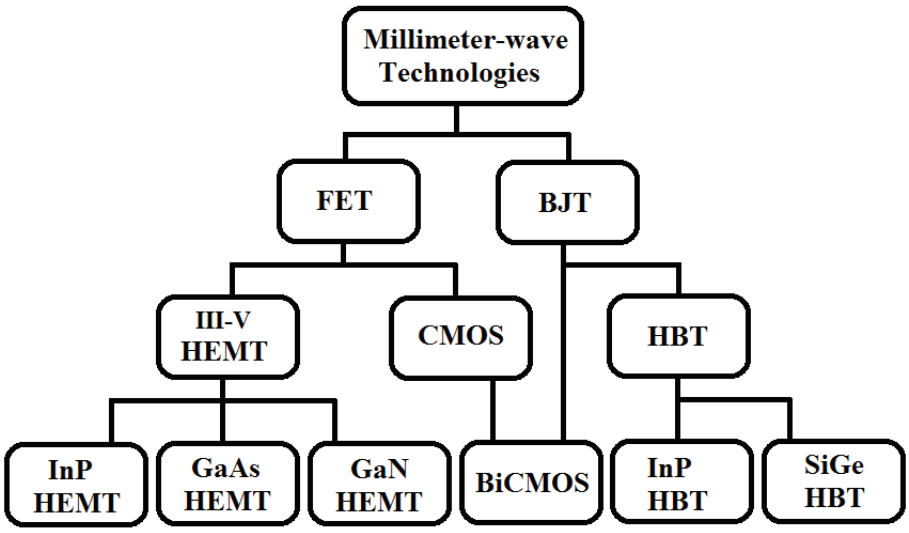


Figure 1.5: Main technologies in millimetre-wave frequencies.

Looks important to dwell on the choice of bipolar technology. There are in fact technologies with which it's often possible to get higher performance and lower power consumption. This is the case, for example, of MOSFETs and HEMTs. In 1999 Dr. O. Berger [6] made a comparison between different technologies of the same manufacturer. The analysis focuses on the use of devices in RF circuits and Table 1.2 summarize his results.
SiGe HBT has a very good gain but it lacks on noise introduction and efficiency at very high frequency. As further proof, Table 1.3 shows the confrontation between different technologies considering their use in an LNA [7]. In a decade these devices have seen

	GaAs based Technology			Si based Technology	
parameter	*MESFET*	*HEMT*	*HBT*	*Si BJT*	*SiGe HBT*
Low noise					
LF <100MHz	-	-	+	++	++
RF 2GHz	++	++	++	+	+
RF 10GHz	+	++	+		-
Gain	+	++	++	++	++
Power					
<0.5W	++	++	++	+	+
>2.0W	++	++	++		
Efficiency	+	++	+	-	-
Low voltage	+	++	+	+	+

Table 1.2: Performance comparison between different technologies (++ best, + good, - moderate).

Ref.	**Tech.**	**Freq.**	**NF(dB)**	**Gain**	**S_{11}(dB)**	**IIP3 (dBm)**	**Power**
[8]	0,25μm PHEMT	5,4GHz	0,76	16	-15	N/A	N/A
[9]	0,4μm GaAs	5,2GHz	1,7	14,5	N/A	-10	3mA (3V)
[10]	GaAs HBT	5,7GHz	2,9	16,2	-7	-11	21mA (3,5V)
[11]	SiGe HBT	5,8GHz	1,6	17	N/A	N/A	7,5mA (4,5V)
[12]	0,6μ CMOS	2,4GHz	2,3	17,5	-19	1,8	8mA (3,3V)
[13]	0,24μ CMOS	5GHz	4,8	18	-12	N/A	3,6mA (2V)
[14]	0,25μ CMOS	5GHz	2,5	16	-9,5	N/A	16mA (3V)

Table 1.3: Comparative between LNAs using different technologies.

strong growth, the operating frequencies have increased significantly, but the balance of forces have remained almost unchanged, at least looking at HEMT.

Now the question is: "Why to use this technology instead of the top performing ones?" The answer is simple: *production costs*.

SiGe HBT is less expensive than MOS and HEMT.

HEMT (GaAs, InP, GaN) is more expensive due to the more complex production process. Principal problem is the substrate that has to present a molecular structure compatible with used III-V materials couple. Wafers of suitable material are usually fragile, expensive and their size is limited. GaAs HEMT are the cheaper ones and are commonly used for very high frequencies PA where the performance is needed [15].

MOS and SiGe HBT are both compatible with silicon wafers and use cheaper production

process, which means HEMT cannot compete in costs with them. It's not completely true that MOS is always more expensive than Si-Ge HBT. Comparing the two technologies at a fixed scaling node MOS results cheaper. But if the two technologies are compared considering the same performance SiGe is the winner. In fact, it has the same performance using a less aggressive lithography (usually two steps less than Si-MOS). SiGe has also higher breakdown voltage and gain per area, making it ideal for the design of PAs [16].
Extra design time and costs sometimes needed to achieve the same performance of other technologies are widely covered by the lower cost. Obviously this is not sufficient in the case performance is not equal to that obtained with other devices. One way to ensure a place in the market for these devices is to make the circuits created as versatile as possible. In this perspective has been made the choice to implement a down-converter tuned to 10 GHz (X-band) that can be used as part of a W-band receiver or as a stand-alone component.

1.1.4 Other fields of use

In the first part of the chapter is discussed only one possible use of this 10 GHz down-converter, most related to original Infineon project. But this component can be easily reused in other fields.
Input bandwidth of this receiver is part of the X-band, the segment of the microwave radio region of the electromagnetic spectrum that goes roughly from 7.0 to 11.2 GHz for communication engineering (8.0-12.0 GHz for radar engineering).
X-band transceivers are used in the following systems:

- **military satellite communications** (7-8 GHz);
- **civil, military and government radar application** for weather monitoring, air traffic control, maritime vessel traffic control, defence tracking, and vehicle speed detection for law enforcement;
- **terrestrial communications and networking** eg. terrestrial broadband;
- **space communications** eg. deep space telecommunications;
- **satellite television broadcast**.

1.2 Base concepts

An analogue system can be divided in a certain number of blocks (1, 2, ...). Considering the down-converter, the blocks are three, so it's good take a 3-blocks system as example. Any block is characterized by some parameters: gain, linearity, noise figure, input and

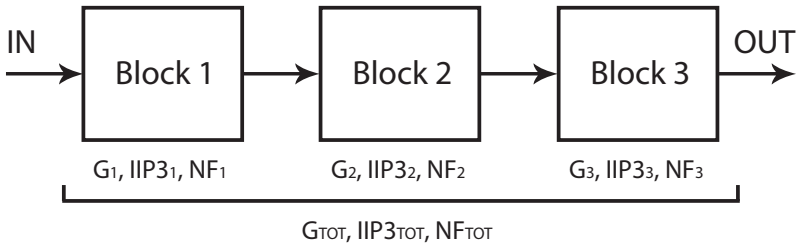


Figure 1.6: 3 blocks structure.

output impedance. These parameters are not exhaustive to describe the block, but enough to understand if they can work together and the approximate performance of the complete system.

1.2.1 Gain and conversion gain

The word "gain" doesn't represent anything if is not specified which gain is considered. In this document power gain is commonly used, unless otherwise specified. It corresponds to the ratio between output and input power of a block.

$$G = \frac{P_O}{P_I} \tag{1.1}$$

$$G_{dB} = 10log(G) \tag{1.2}$$

It depends not only on block characteristics but also on source and load impedances. In this work 100Ωs are used as characteristic impedance (Z_0). If perfect matching is reached between the blocks of a system total gain can be expressed by the equation

$$G_{tot} = G_1 \cdot G_2 \cdot ... \cdot G_n \tag{1.3}$$

$$G_{tot,dB} = 10log(G_{tot}) = G_{1,dB} + G_{2,dB} + ... + G_{n,dB} \tag{1.4}$$

Unmatched input and output between two blocks involves an attenuation of the signal and a lower total gain. Evaluating power gain of a block considering a good matching (S-parameter $<$ -10dB, see section 1.2.4) with Z_0 at input and output allows to use 1.3 and 1.4 with good approximation. When the mixer is considered, the ratio between the output signal and the input one is called conversion gain, where the two signal have different frequency. This to distinguish with the gain which considers the same frequencies for both the input and the output signals.

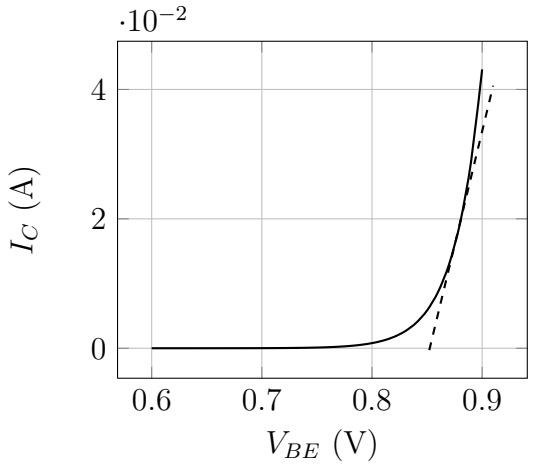


Figure 1.7: Example of non-linearity of a bipolar transistor.

1.2.2 Linearity

When a block has a non-linear transfer characteristic it produces a distortion of the signal. For example, the application of a sinusoidal waveform to the exponential characteristic of a bipolar transistor causes a sharpening of a side and flattening of the other one. This corresponds to the generation of a number of harmonic frequencies of the input sinusoidal waveform. These are the **distortion components**.
Consider an amplifier with a weak non-linearity (see Figure 1.7). Input and output signal are u(t) and y(t). The relation between these signals can expressed with a power series

$$y(t) = a_0 + a_1 u(t) + a_2 u^2(t) + a_3 u^3(t) \tag{1.5}$$

Coefficient a_0 represents the DC component, a_1 the linear gain and a_2, a_3, ... the distortion. Under low-distortion conditions only second and third order distortion components can be considered.
Using as input a cosine signal

$$u(t) = U cos(\omega t) \tag{1.6}$$

and the trigonometric identities

$$cos^2 x = \frac{1}{2}(1 + cos2x) \tag{1.7}$$

$$cos^3 x = \frac{1}{4}(3cosx + cos3x) \tag{1.8}$$

equation 1.5 becomes

$$y(t) = \left(a_0 + \frac{a_2}{2}U^2\right) + \left(a_1 + \frac{3}{4}a_3 U^2\right) U cos(\omega t) + \frac{a_2}{2}U^2 cos(2\omega t) + \frac{a_3}{4}U^3 cos(3\omega t) + ... \tag{1.9}$$

To note that non-linearity produces not only the generation of second- and third-harmonic components but also modifies the amplitude of the DC and first harmonic ones.
Now consider application of the sum of two cosine waveform of frequencies f_1 and f_2 and both with amplitude U. At the output is possible to see now signal components at all combination of f_1,f_2 and their multiples. To simplify the analysis, under low-distortion condition, only components due to a_2 and a_3 coefficients can be considered. The graph below shows the most important distortion components produced by non-linearity. The

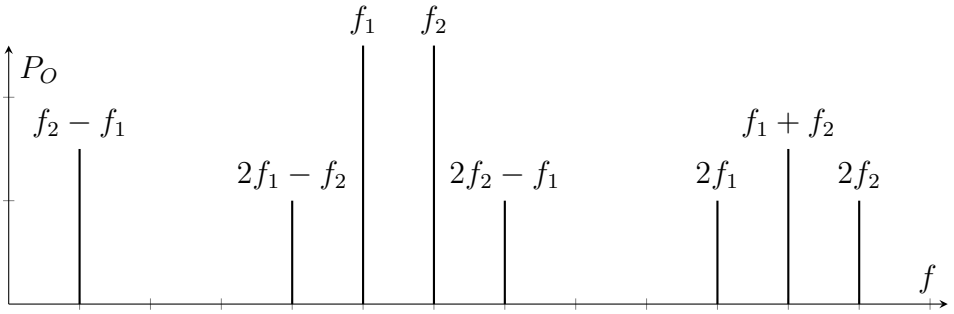


Figure 1.8: Distortion components in an amplifier.

differential structure of the system described in this work allows to concentrate on the components due to a_3. In fact this kind of structure ideally delete the even distortion components. This will be explained better later in the subsection.

IM3 and IP3

Third-order intermodulation distortion (IM3) is visible at frequencies $2f_1 \pm f_2$ and $2f_2 \pm f_1$. It's given by the ratio of the component at one of the these frequencies, which is $\frac{3}{4}a_3U^3$, to the fundamental, which is a_1U, as given by

$$IM3 = \frac{3}{4}\frac{a_3}{a_1}U^2 \tag{1.10}$$

IM3 is more important than the ratio between second- and third-harmonic components and the fundamentals, because represents a component really close to the original signal and cannot be easily filtered. Another important characteristic and often used point is the IM3 intercept, or **IIP3**.

"IIP3 is the value of the input signal where the extrapolated curves of the components of IM3 and the fundamental coincide."

Figure 1.9 helps to explain this concept.

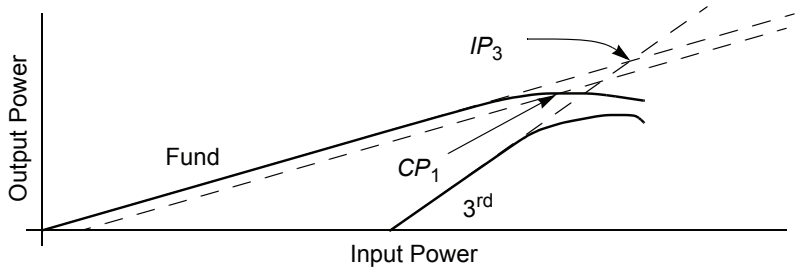


Figure 1.9: IP3 derivation from linearization of fundamental and IM3 curves.

Using 1.10 it's easy to calculate IIP3

$$IIP3 = IM3 = U \Longrightarrow IIP3 = \sqrt{\frac{4}{3}\frac{a_1}{a_3}} \tag{1.11}$$

The equation is valid if the transfer function is known and this is not the case. The simulation of a block can only return a graph similar to 1.9. How is possible to determinate IIP3 looking at the graph? First step is to plot the output power spectrum. Power will be used instead of voltage to simplify the analysis of the results. It's important to choose an input power value inside the range where is possible to extrapolate the linear characteristic of the fundamental and third-harmonic intermodulation components. Three values are necessary: input power, $P_I(f_1)$ or $P_I(f_2)$, fundamental output power, $P_O(f_1)$ or $P_O(f_2)$, and third-harmonic intermodulation component output power, $P_O(2f_1-f_2)$ or $P_O(f_2-f_1)$. Equation 1.10 shows that the component at $(2f_1 - f_2)$ or grows three times faster than the fundamental (the first is proportional to U^3, the second to U) when the input power is increased. With this information is possible to calculate the IIP3 value. δ is the extra input power needed to match the two components at the output.

$$P_{O,dBm}(f_1) + \delta = P_{O,dBm}(2f_1 - f_2) + 3\delta \tag{1.12}$$

$$\delta = \frac{P_{O,dBm}(f_1) - P_{O,dBm}(2f_1 - f_2)}{2} \tag{1.13}$$

IIP3 expression in dBm is

$$IIP3_{dBm} = P_{I,dBm}(f_1) + \delta = P_{I,dBm}(f_1) + \frac{P_{O,dBm}(f_1) - P_{O,dBm}(2f_1 - f_2)}{2} \tag{1.14}$$

The goal is to reduce intermodulation products as much as possible to keep signal integrity and help subsequent blocks to process information without errors. It's clear that an higher IIP3 means a circuit more linear and less signal distortion [17], [18].
In a multi-block system to evaluate total IIP3 starting from singular block parameter is not easy. Interface between blocks heavily influences the performance as in the total gain evaluation. In case of perfect matching between the blocks the total IIP3 of the n-blocks

system is

$$IIP3_{tot} = \frac{1}{\frac{G_n}{IIP3_{n-1}} + \frac{1}{IIP3_n}} \tag{1.15}$$

$$IIP3_{tot,dBm} = 10log\left(\frac{IIP3_{tot}}{1mW}\right) \tag{1.16}$$

$IIP3_{n-1}$ refers to the subsystem composed by the first n-1 blocks and G_n the gain of block n [19].

Inductive degeneration

Feedback is commonly used to linearize an amplification stage. There are several ways to introduce a feedback in the circuit; degeneration in common emitter stages is the most used; an impedance introduced between the emitter of the transistor and ground or a common mode node. This, as any feedback path, reduces gain and introduces noise as it will explain in the sequent subsection. Degeneration can be resistive, capacitive or inductive. Meyer and Fong analyse in a really interesting paper [20] these different configurations. Their results are now reported. The sequent circuit is considered, Z_B is the

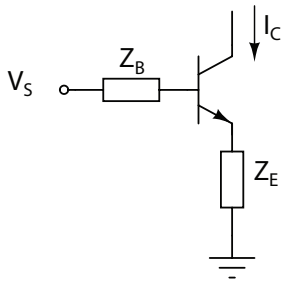


Figure 1.10: Degenerated common emitter stage.

impedance at the base of the transistor, which includes source resistance (Z_S), base resistance (r_b) and matching network. Z_E is the impedance at the emitter which includes the parasitic emitter resistance of the transistor and impedance of the degeneration elements. C_{BE} is the base-emitter capacitance.

$$|IM_3| \propto [1 + sC_{be}Z_B(s) + sC_{BE}Z_E(s)] \tag{1.17}$$

IM_3 equation is much more complicate, but 1.17 allows to understand the choice of inductive degeneration. If Z_E is an inductance the term $sC_{BE}Z_E(s)$ is real and negative, so it cancels partially the 1 reducing third-order intermodulation. If it is a resistor the third term is a positive imaginary value that adds to the second one increasing IM_3. The same problem if the degeneration is capacitive: third term is a positive value that increases the real part of the equation reducing linearity. The analysis of the complete formula confirms that the choice of inductive degeneration gives the best results in terms

of linearity. It's important also to note that second and third terms directly depend on C_{BE}, which can be generally considered the total capacity between the base and emitter, including also external capacitors. Accordingly to the equation, a device with a large parasitic capacitance, or with a capacitor added in parallel between the two contacts, leads to a reduction of the linearity, or an increase of the degeneration component to compensate (higher noise).

Differential pair

The easiest way to increase CMRR (common mode rejection ratio) and to increase linearity ("ideally deleting" second-order harmonic distortion components) is the use of differential stages. All the blocks described in this work are differential.
Most important structure in a differential circuit is the differential pair,

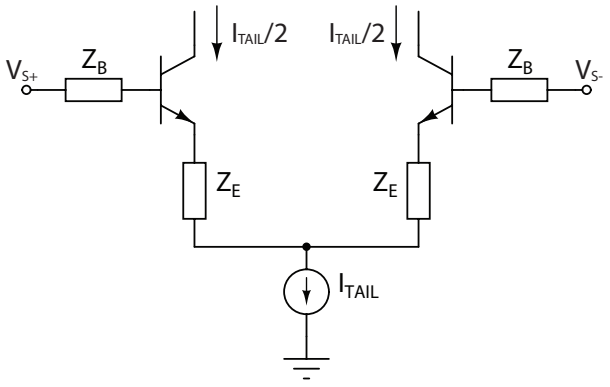


Figure 1.11: Degenerated differential pair.

The signal is shared by two transistors, instead of only one. The characteristics are subtracted deleting even-harmonics distortion. The graph above shows the characteristic of

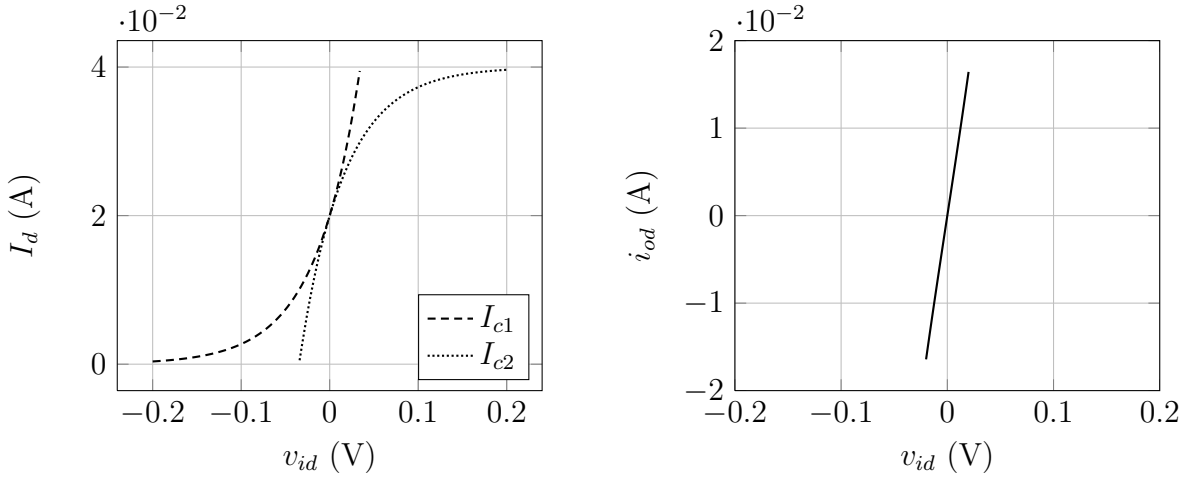


Figure 1.12: Characteristics of the two transistors of the differential pair and their combination.

the differential with the combination of the collector currents of the two transistors. To note that has been considered the ideal curve of a transistor, ignoring, eg, the compression). Linearity is higher at the cost of an higher noise figure and power consumption, because of the increased number of components.

1.2.3 Noise figure

In analog circuits is common to use SNR (signal-to-noise ratio) to define the performance. In RF design, for computational convenience, **noise figure (NF)** is preferred.

$$NF = 10log(F) = 10log\left(\frac{SNR_{out}}{SNR_{in}}\right) = SNR_{in,dB} - SNR_{out,dB} \tag{1.18}$$

SNR_{in} and SNR_{in} are the signal-to-noise ratios measured at the input and output of a block, respectively.

"Noise figure is a measure of how much the SNR degrades as the signal passes through a block."[21]

In a multi-blocks system the overall noise figure is define by

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 \cdot G_2 \cdot ... \cdot G_n} \tag{1.19}$$

$$NF = 10log(F) \tag{1.20}$$

where G_n and F_n are, respectively, gain and noise figure of the n-block, to consider not in dB.
Equation 1.19, called also Friis equation [19, p. 43-46], indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that *"the first few stages in a cascade are the more critical"*.
Let's do some generic consideration about the noise. Every real component added to the circuit increase the amount of noise introduced by the system. If the component is before the active device which produces gain, its noise is amplified. In passive components the noise is introduced by resistive part, so ideal caps and inductors do not introduce noise. But lumped components are not ideal and their resistivity cannot be ignored. As example, the parasitic resistance presents in a coil is proportional to length and inversely proportional to the width of the section of the wire used. It's important to keep in mind this thing when designing the degeneration coils. They are part of the feedback of the high-gain transistors, so the noise introduced is directly injected at the input of the stage, without any possibility to reduce it.

1.2.4 Input and output impedance

Input and output impedances are important parameters as already seen. To match this factors between two blocks means to optimize the structure and to simplify evaluation of overall performance using singular blocks parameters. Impedance varies within the input bandwidth of a block so the evaluation of matching is not easy.
A way to do it is the use of S-parameters. Consider a single block as a two-port network. It's possible to define the *scattering matrix* relates outgoing waves b_1, b_2 to incoming

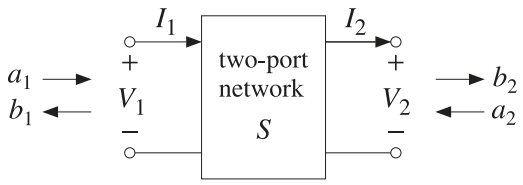


Figure 1.13: Two-port network.

waves a_1, a_2 that are incident on the two-port:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1.21}$$

The matrix elements are referred as to *scattering parameters* or *S-parameters*. S_{11} and S_{22} are *reflection coefficients*, S_{12} and S_{21} are *transfer coefficients*. Talking about matching between the blocks, first two parameters are really useful to evaluate the quality of the interface. Reflection coefficient represents the ratio between outgoing and ingoing waves

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{Z_O=Z_L} \tag{1.22}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{Z_I=Z_S} \tag{1.23}$$

The range of these parameters is [0 1] where 0 means the complete transmission of the signal, a perfect matching (no reflection wave is present), and 1 means the signal is blocked by the interface and the sequent block doesn't receive the information. The goal is to get as close as possible to 0 to reduce signal losses. Talking about impedance and considering two blocks connected together, to reach the perfect matching, output impedance of input stage has to be the complex conjugate of input one of second stage. In this work the single blocks are evaluated with $100\,\Omega$ source and load impedance so the way is to design circuits with input and output impedances close to this value [22]. Usually dBs are used

to define S-parameters, using sequent equation:

$$S_{dB} = 20log(S) \tag{1.24}$$

Quality of the matching can also be expressed as **return loss**, the loss of signal power resulting from the reflection caused at a discontinuity of the impedance [23]. It's simply the opposite of S_{dB},

$$RL_{dB} = -S_{dB} = 20log(\frac{1}{S}) \tag{1.25}$$

1.2.5 Stability

The stability of a block is not easy to determinate and several methods are used to check this parameter. A common used method considers two coefficients: $\mathbf{K_f}$ and $\mathbf{b_1}, \mathbf{f}$.

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}S_{21}|} \tag{1.26}$$

$$b_1, f = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta^2 \tag{1.27}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{1.28}$$

S-parameters are calculated with different configuration of load and source, even if the circuit is designed to work only in a particular setup. Furthermore a wide range of frequency is considered, not only the bandwidth of the input and output signals. All this to ensure the absence of oscillations in all possible conditions. Block is unconditionally stable if

$$K_f > 1 \qquad b_1, f > 0 \tag{1.29}$$

These parameters indicate if the stability has been reached, but not if a block design version is more or less stable than another or which way to go to stabilize the circuit [24]. If the complete system is considered it's not possible to say if it's stable or not only looking at the stability of single blocks. Feedbacks also depend on how the blocks are placed inside of the wafer, i.e. which parasitic components are added to the circuit. Evident is the need to model these components as precisely as possible and to check stability of the complete system also. Often a circuit, which is stable during design phase, presents oscillations due to coupling and routes that have not been considered after layout phase.

1.3 X-band downconverter

The system, as already said, is fundamentally composed by three blocks:

- low noise amplifier (LNA);

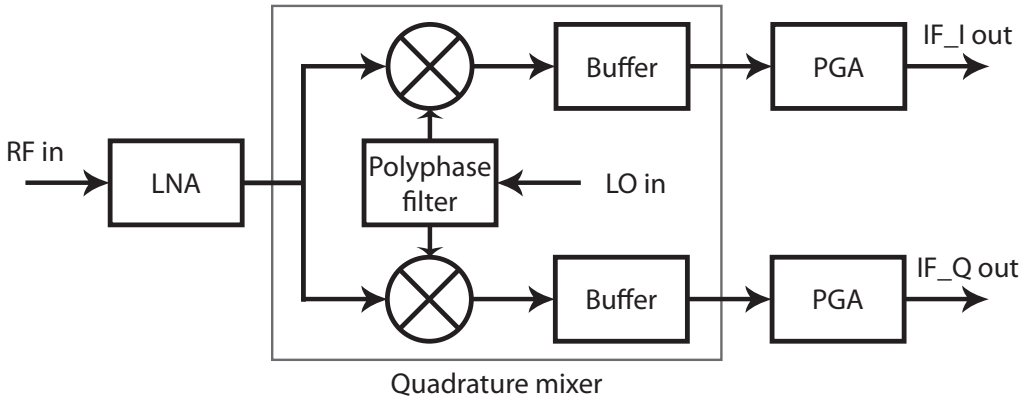


Figure 1.14: X-band down-converter structure.

- quadrature mixer;
- programmable gain amplifiers (PGA).

The two branches of structure starting from LNA's output are symmetrical, only the phase of the ingoing LO signal is 90° shifted between the two. LNA and PGA have fundamentally the task to amplify the signal and match the gain and noise requests. Quadrature mixer is the core of the circuit. It's responsible of the down-conversion and, consequently, the most critical block. But the blocks and the relative theory at the base of them will be discussed following the order they appear in the system. Before to begin the discussion of individual blocks, it's necessary to make some general remarks.

1.3.1 General remarks

The two redesigned blocks, mixer and LNA, have similar structures. Both use an inductive degenerated differential pair, a cascode stage (switching stage of the mixer can be seen in this way), passive load and an output buffer. Then some general considerations are necessary to simplify the description of the single block. Use of degenerated differential pair has been already motivated before in the chapter, at least as regards linearity. Here will be discussed how the transistor and its configuration influence performance.

Transistor linearity and added noise

Linearity of an amplification stage strongly depends on the characteristics of the transistors used and how they are biased. It's easy to understand the wider is the signal treated by the device the lower is the linearity achieved because of the non-ideal characteristic. Before to start to argue about the effect of transistor layout on linearity it's necessary to summarize which kind of device are available. The two principal categories are:

- **High Speed Transistor**. This device has an f_T really high, so it can afford high gain at high frequencies. The range of V_{CE} values tolerable is limited by the avalanche effect.

- **High Voltage Transistor**. This device has a range for V_CE much wider then HST but it presents lower f_T and it's ten times bigger, if the same biasing current is considered.

Both the typologies allow the use multi-finger layout. Generally the use of more fingers for base, emitter and collector doesn't reduce parasitic capacitances but reduces parasitic resistivity of the contacts. Should also be noted that the misalignment between the masks has more influence on a multi-finger structure, reducing the size and the performance of the device.
Equation 1.17 has already been used to understand why the inductive degeneration is chosen for the common emitter stages of the differential pairs used in LNA and mixer. But it can also been used to understand which transistor configuration is better. Basically the reduction of resistive parasitic components helps to reduce the real part of Z_B and Z_E, then a lower IM3 component is achieved. So multi-finger helps to increase linearity at the cost a less robust layout. But how this choice influence noise figure?
Represent the input-referred noise of a bipolar transistor by a series resistor ($NF = 1+R_{eq}/R_S$)(device capacitances and other resistances are neglected here). Input-referred noise voltage per unit bandwidth is given by

$$\overline{V_n^2} = 4kT\left(r_b + \frac{1}{2g_m}\right) \tag{1.30}$$

$$= 4kT\left(r_b + \frac{V_T}{2I_C}\right) \tag{1.31}$$

To reduce the noise introduced by the transistor is necessary to have a low r_b and high g_m that means a a big device biased at a high current. The solution is to use a bias current close to the maximum current tolerable by the device. From the point of view of noise figure is therefore not necessary to oversize the transistors in order to obtain the best performance [19, p. 166-167]. Also the reduction of r_b helps to reduce the noise introduced by the device. Multi-finger helps also with the noise figure. Now are available some guide-lines for the choice of the transistors to use in the blocks.
The biasing of these components is another question. From the noise figure analysis a rule for the collector current is derived. The other parameter to consider is the voltage between collector and emitter. It influences principally the linearity. Figure 1.15 show the characteristics of a High Speed SiGe HBT device. A V_{CE} of about 1 V ensures best compromise between output voltage range and linearity.

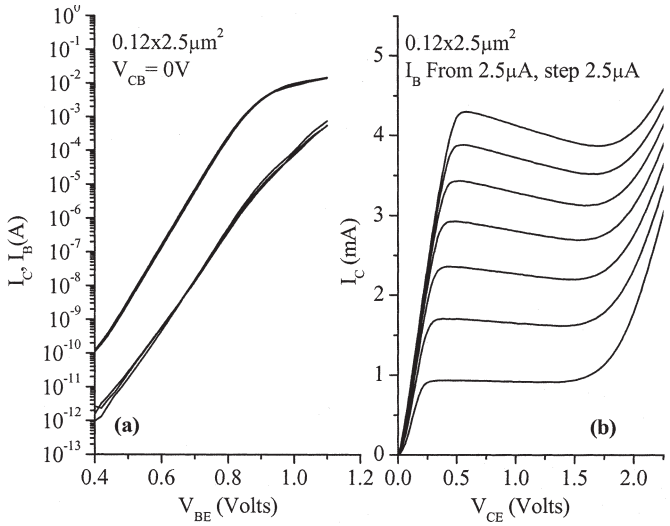


Figure 1.15: Example of SiGe HBT device characteristics (not related to Infineon technology)

Input matching

Parasitic components strongly depend on the size of the transistor, so is better to consider that a bigger device means bigger capacitances. These elements reduce the bandwidth and influence the input impedance of the circuit.
The input network return loss of the differential circuit can be expressed by

$$\Gamma_{dB} = 20log|\Gamma| = 20log\frac{Z_{in} - Z_S}{Z_{in} + Z_S} \tag{1.32}$$

$Z_S = R_0 = 100\Omega$ and, considering only the real part, $Zin = R_0 + \Delta R_0$, 1.32 becomes

$$\Gamma_{dB} = 20log|\Gamma| = 20log\frac{\Delta R_0}{2R_0 + \Delta R_0} \tag{1.33}$$

As example, for a return loss of -15 dB, ΔR_0 has to be maximum 43 Ωs. Then the value of the input impedance can vary in the range $60 \div 140\Omega$. The same goes for the output impedance.

Transistor configuration

As amplification stage, between the three most used configurations, common emitter is the only one that fit with the purpose of high power gain and low noise figure. Another thing to consider is the feedback. In case of emitter degeneration the best choice is too use an inductive element. Other kinds of feedback will be discussed in subsection 2.2.2. Also common base and common collector (emitter follower) are used: the first in cascode stage as current buffer, the second in the output stages as voltage buffer.

Stability

Another parameter to consider is the stability of the circuit. In the presence of feedback paths from the output to the input, the circuit may become unstable for certain combinations of source and load impedances. 1.26 suggests that stability improves as S_{21} decreases, that means reverse isolation increase. In RF design this is accomplished by "neutralizing" the input-output capacitive path, often due to parasitic components. One of the possible solutions is the use of a cascode configuration, but at the cost of a somewhat higher noise figure.

1.3.2 Low noise amplifier (LNA)

LNA is a circuit used in the RF frequency range to amplify the signal reducing as much as possible the amount of noise added by the block. Input matching network and load are tuned to the needed bandwidth. This allows to attenuate the influence of components outside this bandwidth. Generally the circuit is used to amp weak RF signal as the ones from antennas, so it is usually the first block of the receiver. As already said, looking at Friis' formula, the overall noise figure of the receiver's front-end is dominated by the first few stages (or even the first stage only). Also overall linearity strongly depends on first stage characteristics. Therefore gain, noise figure and linearity of this part of the system are really important. Razavi overview on LNA design [19, p. 166-177] is a good starting point for the development of the circuit. An LNA is basically an amp, so most important component is the active one, the transistor.

LNA structures

Consider first the structure in Figure 1.16, a single-ended LNA, Q_1 is the principal transistor, it produces gain and influences input network. Input impedance equation, taking into account only C_π and r_b of the transistor, is

$$Z_{IN}(\omega) = j\omega L_B + \underbrace{r_b + \frac{g_m L_E}{C_\pi} + j\omega L_E + \frac{1}{j\omega C_\pi}}_{Z'_{IN}} \tag{1.34}$$

If L_B, L_E and C_π are properly chosen, imaginary part of 1.34 can be eliminated at the frequency of interest. It becomes

$$Z_{IN}(\omega_0) = r_b + \frac{g_m L_E}{C_\pi} \tag{1.35}$$

Sizing the transistors and selecting biasing current (I_C) appropriately, it's possible then get a perfect matching with a $50\,\Omega$-source.
The transistor and the input matching network strongly affect also linearity and noise

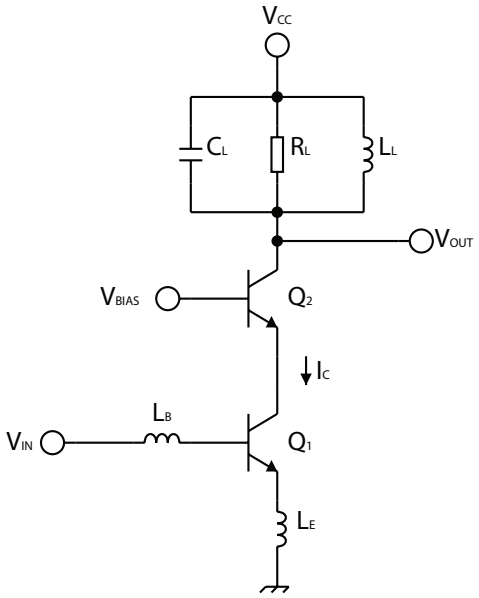


Figure 1.16: Single-ended LNA structure.

figure of the block. Actually to get a good matching is not so easy. The dependence of the linearity and noise figure from the network input, limits the choice of the reactive components by imposing a compromise between the various parameters of the circuit. This will be clearer during the design phase.
As already said, cascode stage (Q_2) is used to reduce capacitive path between output and input and to eliminate oscillations due to the instability of the circuit. But its primary task is to act as a current buffer and increase the gain of the LNA. Common base as also high output impedance that helps to simplify the tuning of the load; in first approximation it's possible to consider only the elements of the RLC filter.

$$Z_L(\omega) = R_L + j\omega L_L + \frac{1}{j\omega C_L} \tag{1.36}$$

As for the input network, choosing the correct values of C_L and L_L, it's possible delete the imaginary part of this impedance at the frequency of interest.
The ratio between collector and base current can be defined has

$$\frac{i_C}{i_B} = \frac{g_m}{sC_\pi} \tag{1.37}$$

Considering now matching and load networks (R_S is the source impedance) the voltage gain of the LNA at the center frequency is expressed by the following equation:

$$G = \frac{v_{OUT}}{v_S} = \frac{1}{2R_S} \cdot \frac{g_m}{sC_\pi} \cdot R_L \tag{1.38}$$

The circuit used in this work has a differential structure, differential input and output. A simplified example is shown in figure 1.17.

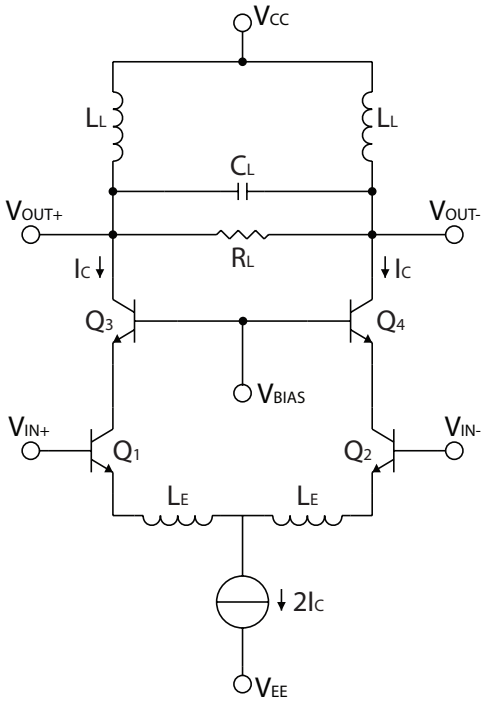


Figure 1.17: Differential LNA with cascode stage.

Impedance at the differential input is

$$Z'_{IN} = 2 \cdot Z'_{IN} = 2 \cdot \left[r_b + \frac{g_{m,1} L_E}{C_{\pi,1}} + j\omega L_E + \frac{1}{j\omega C_{\pi,1}} \right] \tag{1.39}$$

Basically only the load has a different structure but, if the differential input and output signals are considered, equations are quite similar. Gain and impedance formulas are reported in Section 2.1.1.

Differential version of the circuit as a higher linearity at the cost of higher noise and power consumption, but it can drive a differential mixer. Improvements resulting from the use of a mixer with a differential structure, with particular reference to the structure of Gilbert, justify per se the use of this type of LNA. It is a fortiori important to keep under control the noise figure of this block, due to the increased number of components. Fundamentally to reach a low NF is made difficult by the necessity to match the input with the source impedance and to keep a good gain across the bandwidth. The interface between an antenna or previous demodulation stage and the LNA entails an issue that divides analogue designers and microwave engineers; who thinks is better a voltage matching ($Z_{IN} = \infty$) who a power matching ($Z_{IN} = Z_S^*$). But, as already said and following actual trend in RF design, in this work the second option is preferred. To input

stage is therefore required:

- good matching with a 100 Ω source (return loss 10 dB);
- high gain only in the band of the signal, to reduce the risk of instability;
- high linearity;
- low noise figure in the band of the signal.

All these conditions are in contrast and it is therefore necessary to look for, as already said, a compromise.

1.3.3 Mixer

Theory about mixer reported in the section refers to Prof. Razavi book [25] through the summary presented in RF-design course slides of Prof. Bevilacqua.
Mixer is definitely the most important and difficult to design part of down-converter structure. It's a non-linear circuit and a 3-port block, so also simulation setup and parameters extraction are not easy. RF signal and LO signal are the two inputs of the block. The first contains the original signal translated at high frequencies by the transmitter. The second is a periodic signal at a fixed frequency. This frequency is the same of the carrier of RF signal if the baseband signal is the output wanted.

$$V_{RF}(t) = A(t)cos[\omega_0 t + \phi(t)] \tag{1.40}$$

$$V_{LO}(t) = Bcos(\omega_0 t) \tag{1.41}$$

Basically mixer multiplies the RF signal and the LO signal

$$\begin{aligned} V_{IF}(t) &= V_{RF} \cdot V_{LO} \\ &= \frac{A(t)\cdot B}{2} cos[\omega_0 t + \phi(t) - \omega_0 t] + \frac{A(t)\cdot B}{2} cos[\omega_0 t + \phi(t) + \omega_0 t] \\ &= \underbrace{\frac{A(t)\cdot B}{2} cos[\phi(t)]}_{baseband\ signal} + \frac{A(t)\cdot B}{2} cos[2\omega_0 t + \phi(t)] \end{aligned} \tag{1.42}$$

A low-pass filter attenuates the high frequency component providing the down-converted signal. But this simple mixer is not able to discriminate between the signal and its image. Considering an input sine signal at frequency $f_{RF} = f_{LO} + f_0$, the image signal is at $f_{RF}^{IM} = f_{LO} - f_0$. Positive and negative frequencies are translated in opposite directions and their overlap preventing the reconstruction of the original signal.
Two systems are used to reduce the influence of image signal during down-conversion process:

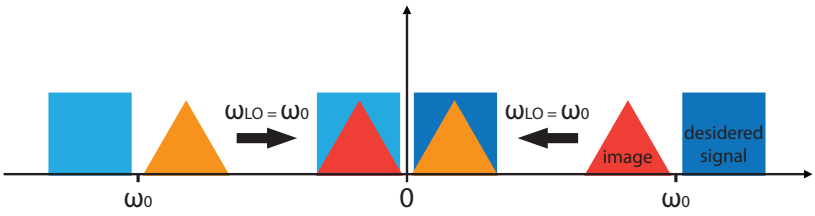


Figure 1.18: Signal and image bands translation in simple mixer.

- pass-band filter to attenuate image bandwidth;
- **quadrature mixer** configuration.

1.3.4 Quadrature mixer

In this technique there are two mixers with LO signals in quadrature.
Output signals are considered as a singular complex entity,

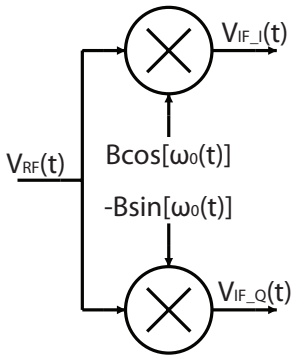


Figure 1.19: Diagram of a quadrature mixer.

$$\begin{aligned} v_{IF}(t) &= v_{RF}(t) \cdot Bcos(\omega_0 t) + v_{RF}(t) \cdot [-Bsin(\omega_0 t)] \\ &= B \cdot v_{RF}(t) e^{-j\omega_0 t} \end{aligned} \tag{1.43}$$

Transforming this signal in frequency domain

$$V_{IF}(\omega) = \mathcal{F}[v_{RF}(t)] = V_{RF}(\omega + \omega_0) \tag{1.44}$$

Therefore the translation is only in one direction of the spectrum. A complex filter can delete the image of the wanted signal. It's clear that the two mixers used must be perfectly symmetrical to allow the complete suppression of the image signal. To represent the system's ability to suppress unwanted bandwidth image rejection ratio (IMRR) is used (see Section 1.3.5).

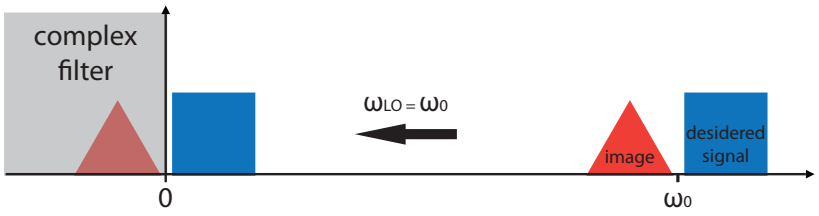


Figure 1.20: Signal and image bands translation in a quadrature mixer.

1.3.5 Image rejection ratio - IMRR

Two are the causes of a not complete suppression of image rejection:

- asymmetry of the quadrature mixer and polyphase filter due to mismatches between the components. It depends fundamentally on production process quality and topology robustness;
- polyphase filter output offsets, in phase and amplitude, due to a non-perfect tuning of the circuit.

Also the kind of PPF chosen set the maximum IMRR affordable (see Section 1.3.9). But this cannot considered as cause of a low IMRR because is a parameter that depends directly on the designer choice. It's necessary to consider the two output voltages of the system to calculate the parameter

$$V_{OUT,I} = A_I(t)cos\left(\omega_{IF}(t) + \Phi_I\right) \tag{1.45}$$

$$V_{OUT,Q} = A_Q(t)cos\left(\omega_{IF}(t) + \frac{\pi}{2} + \Phi_Q\right) \tag{1.46}$$

Are then defined the following two ratios

$$\delta = \frac{A_I}{A_Q} \qquad \phi = \Phi_I - \Phi_Q \tag{1.47}$$

δ and ϕ represent respectively amplitude and phase mismatches [26]. To calculate the IMRR the sequent equation is used

$$IMRR = 20log\left[\frac{1 + \delta^2 + \delta cos(\phi)}{1 + \delta^2 - \delta cos(\phi)}\right] \tag{1.48}$$

Graph in Figure 1.21 shows some values of this parameter relating to typical range phase and amplitude mismatches.

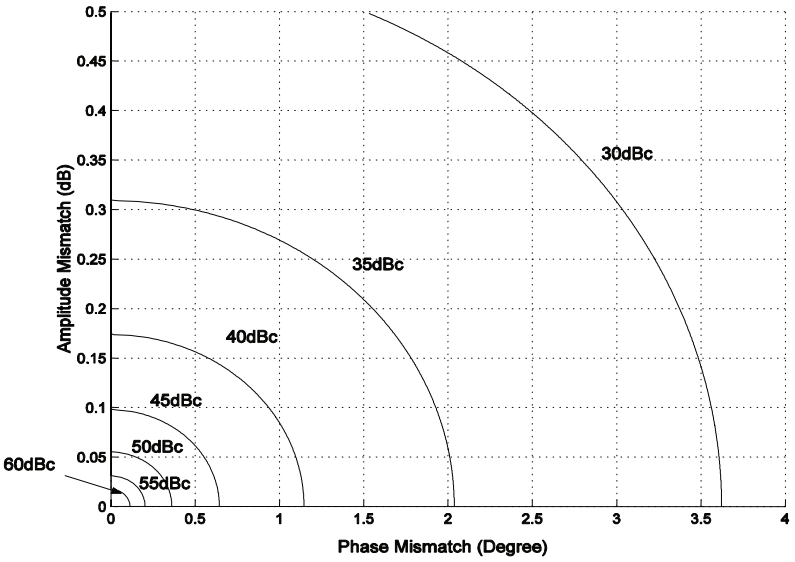


Figure 1.21: IMRR dependence on phase and amplitude mismatches.

1.3.6 Current-switching mixer

Current-switching is a commonly structure used for mixers. Base concept is to switch the path of the current at the same frequency of signal carrier (in a down-conversion to the baseband). A typical topology and its operation are shown in Figure 1.3.6. Consider the switching pair ideal, RF current is multiplied by the square wave

Differential current can be written in the sequent way

$$i_d(t) = i_{c,1} - i_{c,2} = m(t) \cdot i_{RF} \tag{1.50}$$

Representing $m(t)$ as Fourier series

$$m(t) = \sum_{-\infty}^{+\infty} M_k e^{jk\omega_{LO}t} \qquad M_{K\neq 0} = sinc\left(\frac{k}{2}\right) \qquad M_0 = 0 \tag{1.51}$$

RF current is representable as sine signal with an angular speed of ω_{RF}. The differential current at the intermediate frequency IF is

$$i_d(t) = M_{-1}\widehat{I}_{RF}e^{j\omega_{IF}t} = \frac{2}{\pi}\widehat{I}_{RF}e^{j\omega_{IF}t} \tag{1.52}$$

Transistor Q_1 converts v_{RF} in i_{RF} and the load impedance Z_L converts the differential current into the output differential voltage. Then voltage conversion gain has the sequent equation

$$G_C = \frac{2}{\pi}g_m Z_L \tag{1.53}$$

Conversion gain represents the ratio between the output power at the intermediate frequency and the input power at the radio frequency. As example, if $f_{RF} = 10.5\,GHz$ and

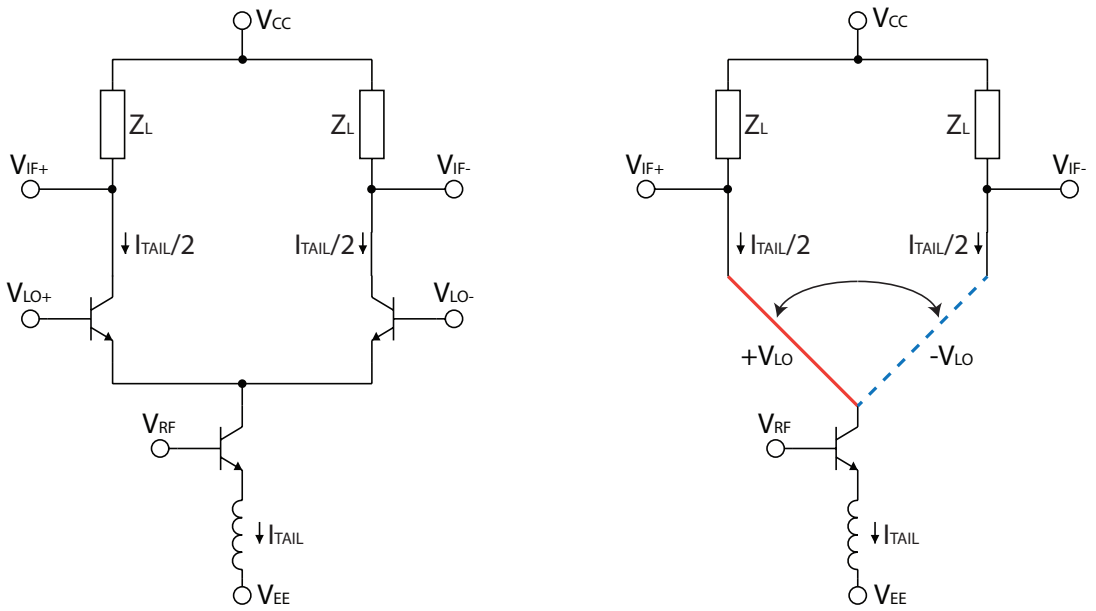


Figure 1.22: Current switching mixer scheme and its theoretical functioning.

$$m(t) = sign\left[\widehat{V}_{LO}cos(\omega_{LO}t)\right] \tag{1.49}$$

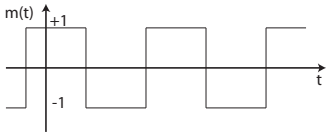


Figure 1.23: Ideal LO square wave.

$f_{LO} = 10\,GHz$ resulting f_{IF} is 500 MHz and the conversion gain is the ratio between $P_{OUT}(500\,MHz)$ and $P_{IN}(10.5GHz)$.
$i_{RF}(t)$ overlaps biasing current of Q_1, I_C.

$$I_{Q1}(t) = I_C + i_{RF}(t) \qquad I_d(t) = m(t) \cdot I_{Q1}(t) \tag{1.54}$$

This produces unwanted components to all the odd harmonics of the LO signal.

$$V_{d,OUT}(t)|_{i_{RF}(t)=0} = Z_L \cdot I_C \cdot m(t) = Z_L I_Q \sum_{-\infty}^{+\infty} M_k e^{jk\omega_{LO}t} \tag{1.55}$$

The phenomenon is called **LO feedthrough** and two ways are commonly used to reduce its influence:

- low-pass filter as load of the mixer;
- Gilbert double-balanced mixer.

Second solution will be explained in Section 1.3.7. Using a load with a band-pass o low-pass behaviour means to attenuate all the components outside the bandwidth of the signal. Equation 1.55 contains not only the original signal and LO produced disturbs but also all the harmonic components due to non-linearity, so this kind of load helps to reduce also this phenomenon. This increase linearity reducing the unwanted possibility of intermodulation between the signal and the harmonics inside the circuit. Therefore the choice to use a Gilbert double-balanced structure doesn't mean giving up the use of a load acting as a filter.

1.3.7 Gilbert double-balanced mixer

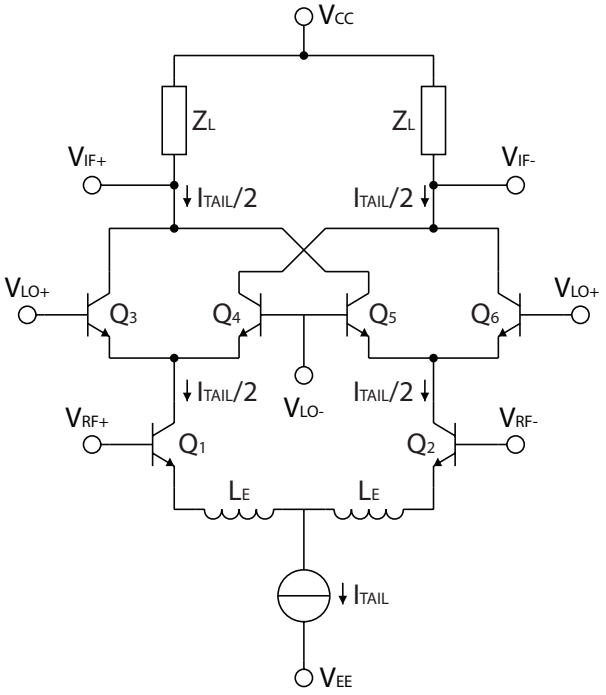


Figure 1.24: Gilbert double-balanced mixer structure [27].

In this structure two single-balanced cells are combined. RF input becomes differential. Now two I_{RF} are present:

$$I_{RF,Q1} = I_C + g_{m,Q1}\frac{v_{RF}}{2} \qquad I_{RF,Q2} = I_C - g_{m,Q2}\frac{v_{RF}}{2} \tag{1.56}$$

Both the cells produce multiplication between the wave $m(t)$ and the

$$I_d(t) = m(t) \cdot \left[I_C + g_{m,Q1}\frac{v_{RF}}{2}\right] - m(t) \cdot \left[I_C - g_{m,Q2}\frac{v_{RF}}{2}\right] \tag{1.57}$$

$$= m(t) g_m v_{RF} \qquad (g_m = g_{m,Q1} = g_{m,Q2}) \tag{1.58}$$

In 1.57 the term I_C disappears, then the problem of LO feedthrough is solved. This is

true if there are not mismatches between the two cells. Gain is the same of the single-balanced mixer, but the current consumption is doubled. The drawback is compensated by the isolation obtained between LO and IF ports.

1.3.8 SSB and DSB noise figure

The definition of mixer noise figure is sometime confused. In this subsection will be shortly defined the difference between SSB and DSB noise figure.
If the input frequency response of the mixer is the same for the signal band and the image band the output SNR is decreased by 3 dB due to the overlapping of the image and signal bands noise. The ratio between this value and the input SNR is the SSB-NF (Single Side Band-Noise Figure). In case of a double-balanced mixer image band doesn't overlap the signal band, then only the signal band noise has to be taken in account. Basically between the two values there is a difference of 3 dB [28].

1.3.9 Polyphase filter

When a quadrature mixer is used, most difficult and important thing to obtain is the 90° phase-shifting between the two LO signals. If the LO input of the mixer is differential four signals are needed.

VCO produce a differential sine signal, so a block to transform this wave is necessary.

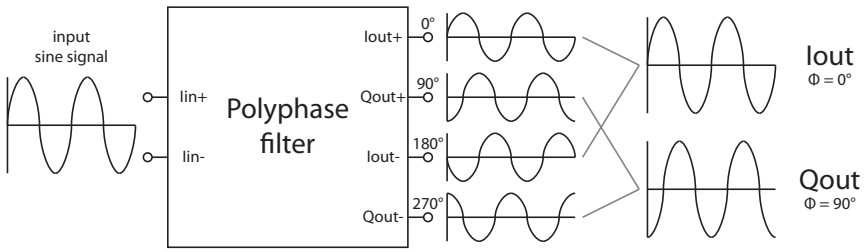


Figure 1.25: Diagram of operation of a polyphase filter.

Commonly used in RF circuits, polyphase filter (PPF) is a simple and efficient solution. Scheme below shows a 3-stage PPF. A stage is composed by 4 RC couples and the value of these components depends on the LO frequency and the number of stages of the filter. Inputs are connected in the way shown in figure 1.3.9. Then, using this differential input and driving the filter with a sine signal, are obtained the 4 signals in quadrature to drive the mixer.
Amplitude and phase balance of the generate I and Q signals affect strongly the image rejection capability of the receiver, thus the reception quality. The circuit needs to be

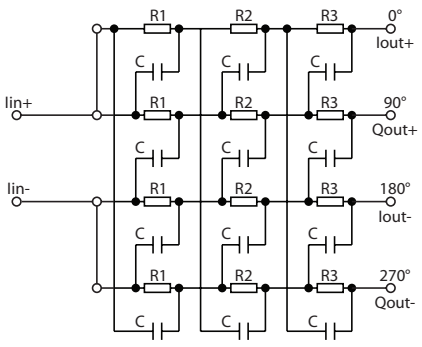


Figure 1.26: 3-stage polyphase filter scheme.

tuned to the LO frequency to increase image rejection and to reduce attenuation, thus also parasitic components become relevant.
Also the use of more stages improves IRR. An increase of the number of stages produces, however, a greater attenuation of the signal. Table 1.4 shows typical values for 2, 3, 4-stages filters. [29].

n° **of stages**	**typical IRR**	**typical att.**
2	25dB	6.0dB
3	40dB	8.4dB
4	56dB	-

Table 1.4: Affordable IMRR and attenuation of an n-stage polyphase filter.

Mismatches, parasitic components and the load detune the filter reducing IMRR and increase attenuation. To keep in mind these factors during design and layout is therefore important.

1.3.10 Programmable gain amplifier (PGA)

The block will be discussed extensively in the design chapter. It's basically composed by several signal amplifiers with different gain. Coupling different stages together a specific gain is obtained. The selection of the gain is made by a digital input properly converted to enable the biasing circuit of wanted amps.
Basic structure of an amp stage is shown below.
Two common emitter stages form the differential amplifier. Voltage gain of each branch has the sequent relation

$$G_{CE} = -\frac{\beta R_C}{r_\pi + (1+\beta)R_E} \approx -\frac{R_C}{R_E} \qquad (\beta >> 1) \vee (\beta R_E >> r_\pi) \qquad (1.59)$$

Considering each common emitter receives half of the input voltage, this also the differential voltage gain. Therefore it's possible to say that gain is fixed only by R_E and R_C.

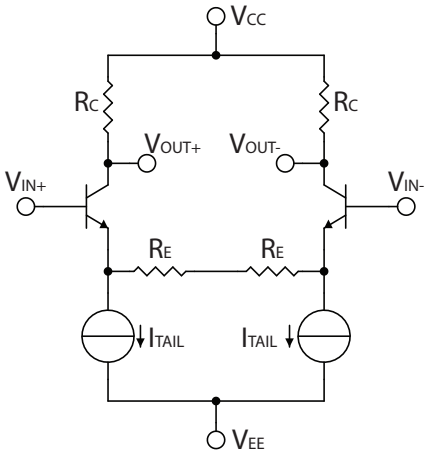


Figure 1.27: Amplification stage structure.

In addition to this structure are used also selection circuits, associated with the biasing circuit of the amplifier, buffers, to reduce influence of the load on the gain of the stage, and AC-coupling stages to match different biasing points.

Chapter 2

Design

First purpose was to redesign blocks and to combine them in a single circuit representing the whole 10 GHz down-converter. Table 2.1 contains initially requests, that are different from the one indicates in the first chapter.

parameter	**value**	**unit**	**conditions**
Conv. gain	≥ 30	dB	$f_{RF} = 10.5GHz$, $f_{IF} = 10GHz$, $P_{LO} = 0dBm$, T=27℃, standard supply voltages (3.3V or 5V)
DSB-NF	≤ 3.5	dB	$f_{RF} = 10.5GHz$, $f_{IF} = 10GHz$, $P_{LO} = 0dBm$, T=27℃, standard supply voltages (3.3V or 5V)
Input IP3	≥ 3	dBm	$f_{RF} = 10.5GHz$, $f_{IF} = 10GHz$, $P_{LO} = 0dBm$, T=27℃, standard supply voltages (3.3V or 5V)

Table 2.1: Initially requests for the downconverter.

A first study with ideal components has shown that the requests are not easily accessible through the structures and the technology used. It has been therefore decided to design test-chips of individual blocks, with inputs and outputs adapted to 100 Ω, to understand which are their maximum performance and which results are achievable when combining them. The guide-lines for the design are parameters indicated in Table 1.1.
In this chapter will be discussed principally the design of the single block test-chips, with some references to the choices made during the first step for the integration of these into a single test-chip.
The chapter is divided in four parts. The first three refer to the three blocks of the down-converter, the last one refer to the biasing circuit. It has been attempted to use the same structure for all the circuits of the project, minimally varying characteristics in the various cases. The target for each block will be presented in the respective section.

2.1 Low noise amplifier

This circuit, as already said, has to show high gain and low noise figure principally. Linearity and input matching are also quite important.
Table 2.1, extrapolated from Table 1.1 , is the design guideline.

parameter	min	typ	max	unit	condition
Supply voltage	-5%	3.3	+5%	V	-
Center frequency	-	10	-	GHz	-
Power gain	10	-	-	dB	T = 27°C, Sup. voltage = 3.3V, f = 10GHz
Noise figure	-	-	4	dB	T = 85°C, Sup. voltage = 3.3V
Output IP3	-	-	4	dBm	T = 27°C, Sup. voltage = 3.3V, f = 10GHz
Input return loss	10	-	-	dB	T = 27°C, Sup. voltage = 3.3V, f = 10GHz
Output return loss	10	-	-	dB	T = 27°C, Sup. voltage = 3.3V, f = 10GHz
-2dB bandwidth	4	-	-	GHz	-
-3dB bandwidth	5	-	-	GHz	-
Op. temperature	-40	-	120	°C	-

Table 2.2: LNA parameters guideline.

Basic structure of the LNA is shown in Figure 2.1.

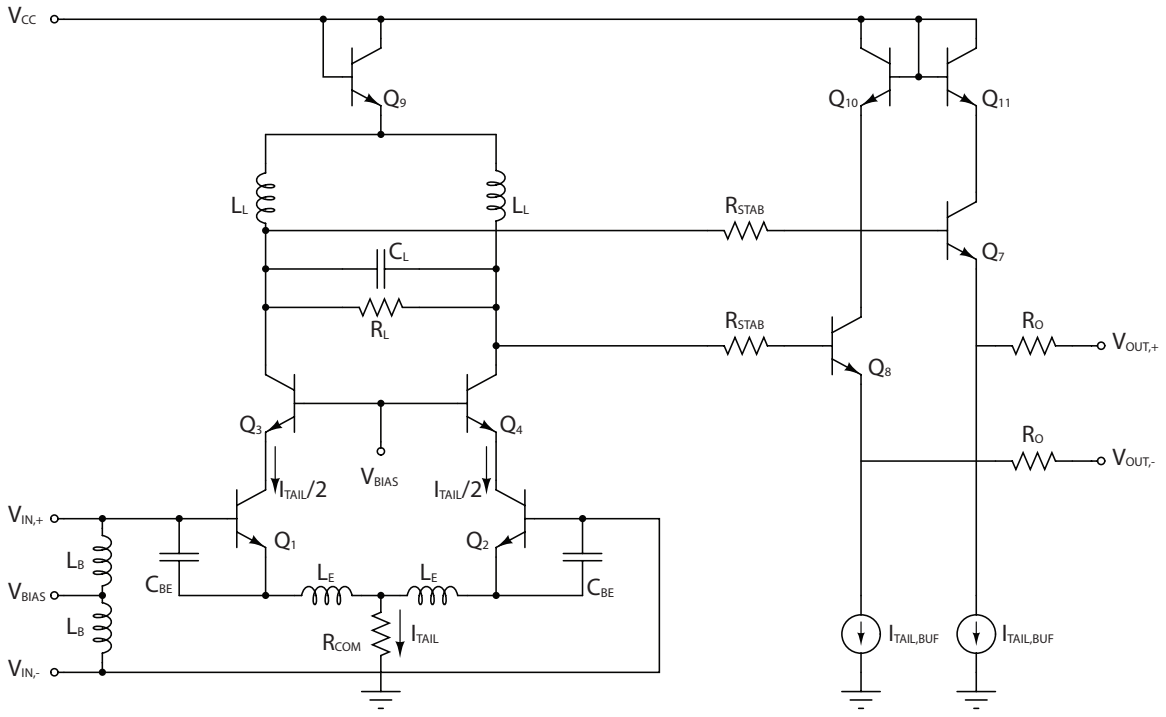


Figure 2.1: LNA structure with buffer.

Three elements are present in the topology:

- input matching network with a differential pair;

- cascode stages;
- tuned load.

Starting circuit has also an output buffer to reduce influence of the external load on the tuned load of the LNA, this at the cost of a slight worsening of the noise figure and limitation of the linearity. It's possible to remove the buffer if the input impedance of the block connected to the output on the LNA is known. This impedance has not to be too small to not limit the gain of the system (see Section 2.1.1).
Original circuit is marginally modified. After the insertion of a second cascode stage to implement the possibility of gain selection between two values (see 2.1.2), the rest of the circuit is simply retuned to 10GHz. This means a redesign of inductors and capacitors, to fit the requests. The tuning will be discussed for first. It's necessary to consider that buffer and gain selection circuit influence the load of the LNA. Any change on these parts of the circuit involves a retuning of the system.

2.1.1 Input network and load tuning

Input network

First thing to do is to analyze the input network. The circuit is in Figure 2.2. The same

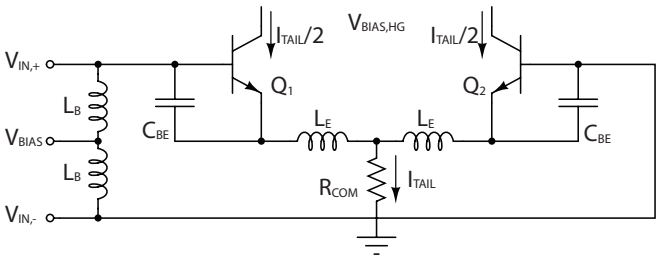


Figure 2.2: LNA input network.

circuit is now represented using the small signal model of the transistor and considering only the differential signal (Figure 2.3).

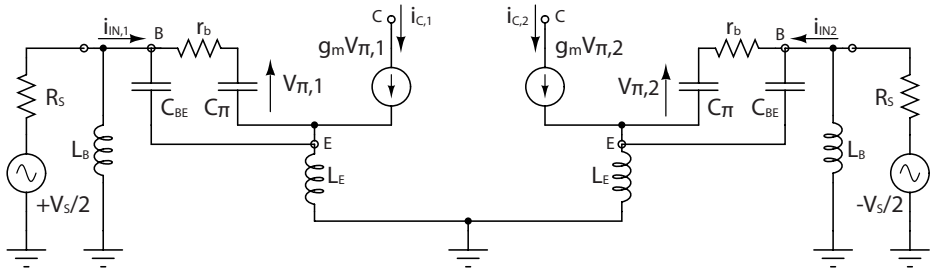


Figure 2.3: Differential small-signal model of LNA input network.

The circuit is symmetrical so it's possible to analyse only an half of it and then properly combine the results. Relation between collector and input currents, not considering influence of C_μ and r_b, is

$$\frac{i_C,1}{i_{IN,1}}(s) = \frac{i_C,2}{i_{IN,2}}(s) = \frac{g_m}{s(C_{BE}+C_\pi)} \cdot \frac{1}{1+s(C_{BE}\|C_\pi)r_b} \tag{2.1}$$

If the condition $C_{BE} \gg C_\pi$ id verified and the equation is considered at lower frequency then it's possible to rewrite it as

$$\frac{i_C}{i_{IN}}(s) = \frac{g_m}{sC_{BE}} \tag{2.2}$$

Through 2.2 impedance seen at the base of the each transistor is easily determinable.

$$Z'_{IN}(s) = g_m\frac{L_E}{C_{BE}} + \left(sL_E - \frac{1}{sC_{BE}}\right) \tag{2.3}$$

An appropriate selection of the values of g_m, L_E and C_{BE} allows to cancel the imaginary part and to match the real part with the impedance of the source. Circuit differential input impedance is given by the parallel of the two transistors input impedance of the differential pair and the two inductors L_B.

$$\begin{aligned} Z_{IN}(s) &= 2sL_B \parallel 2Z'_{in}(s) = 2\frac{sL_BZ'_{in}(s}{sL_B + Z'_{in}(s)} \\ &= 2sL_B\frac{1+sg_mL_E+s^2L_EC_{BE}}{1+sg_mL_E+s^2\left(L_E+L_B\right)C_{BE}} \end{aligned} \tag{2.4}$$

Equation shows L_B multiplied by two complex-conjugate zeros and two complex conjugate poles. Properly choosing the components it's possible to delete the imaginary part of the impedance and to match the source impedance inside the band of interest.
Let's make an example to show how the input matching is achieved. Consider the values showed in Table 2.3. They are not the final values but good enough to explain the concept. Using these parameters in equation 2.4 the result is

parameter	**value**	**unit**
g_m	50	mS
L_E	0.2	nH
L_B	1.0	nH
C_{BE}	300	fF

Table 2.3: Example parameters.

$$Z_{IN}(\omega_0) = 2j\omega_0L_B \cdot (0.13 - j1.3) = (163.4 + j16.4)\Omega \tag{2.5}$$

Imaginary port of the impedance is close to zero. This matching network allows to have pure resistive input impedance. But is not so easy to reach the correct value, in this case $Z_0 = 100\,\Omega$, to match perfectly the source impedance. It's good to have a look the return loss reached with this value of Z_{IN}. First thing to do is to calculate S parameter at input port.

$$S = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0} = 0.244 + j0.047 \tag{2.6}$$

With this value is possible to determinate the return loss,

$$RL_{IN} = 20log|S| = 12.1\,dB \tag{2.7}$$

The value found is already above the minimum required, but it's mandatory to consider that the presence of parasitics, the simplifications made on the equations and the temperature influence on matching quality. Maintain a certain margin during design ensures the respect of project parameters in all conditions.
It's now possible also determinate the relation between the collector current of the differential pair, i_d, and the source voltage, v_s. The Equation 2.8 refers to the transfer function between the two signals.

$$\frac{I_d(s)}{V_s(s)} = g_m \frac{s\frac{L_B}{R_S}}{1 + s\left(g_m L_E + \frac{L_B}{R_S}\right) + s^2\left[\left(L_E + L_B\right)C_{BE} + g_m\frac{L_E L_B}{R_S}\right] + s^3\frac{L_E L_B C_{BE}}{R_S}} \tag{2.8}$$

There are one zero and three poles. Zero is produced by the presence of L_B which is a short to ground for low frequencies. To determinate the position of the poles is not easy. Let's try with an example by replacing the same parameters used for input impedance.

$$\begin{aligned}\frac{I_d(s)}{V_s(s)} &= g_m \frac{2\cdot 10^{-11}s}{1 + 3\cdot 10^{-11}s + 6.6\cdot 10^{-22}s^2 + 1.2\cdot 10^{-33}s^3} \\ &\approx g_m \frac{2\cdot 10^{-11}s}{\left(1 + 2.8\cdot 10^{-11}s + 6\cdot 10^{-22}s^2\right)\left(1 + 0.2\cdot 10^{-11}s\right)}\end{aligned} \tag{2.9}$$

So, one pole is at really high frequencies and can be ignored. There also two complex conjugate poles. Combining these poles with the zero the module of the transfer function represents a band-pass filter with a center frequency around 6.5 GHz, as expected for the input network of an LNA.
It's possible also to calculate module of this equation to understand which gain is available. Figures 2.4 and 2.5 show, as example, how L_E and C_{BE} influence the results of the LNA.
These results are coherent with the Equations 1.17, 2.4 and 2.8. They will be discussed in design summary of this section.

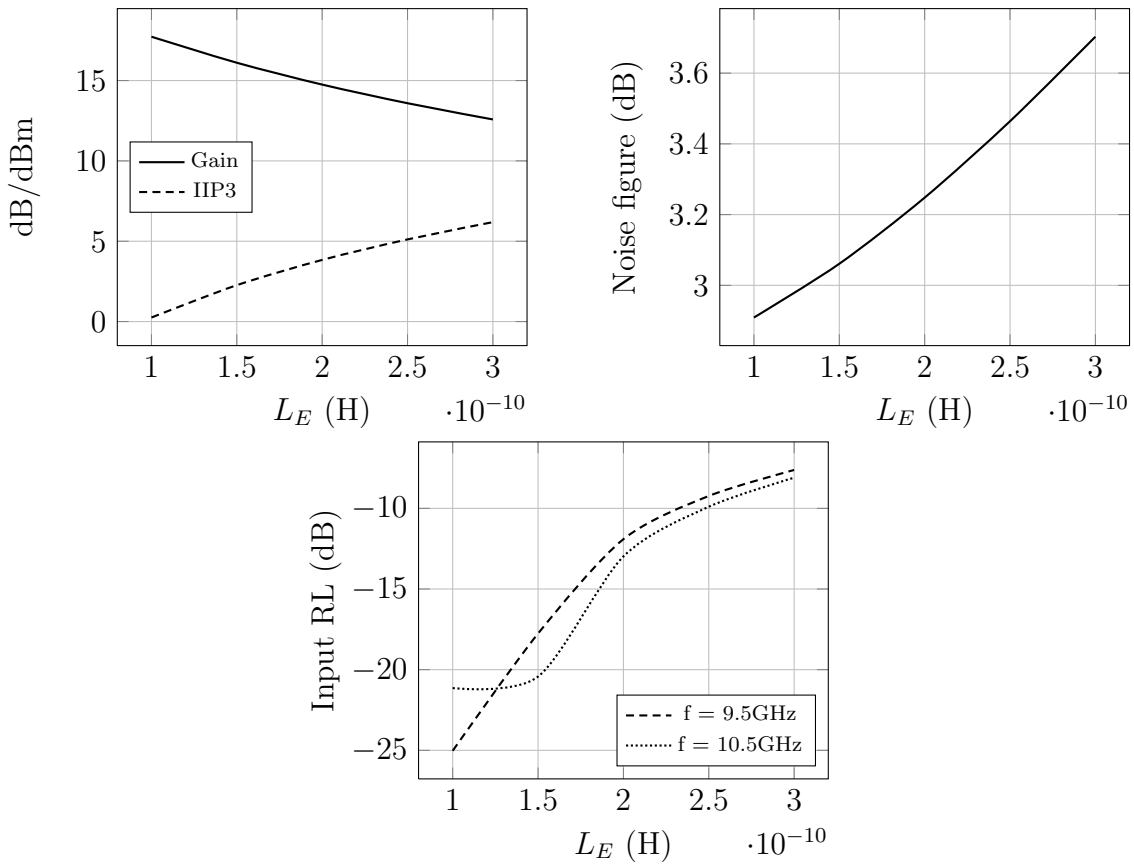


Figure 2.4: LNA's power gain, IIP3, noise figure and return loss dependency to L_E.

Tuned load

If it is considered the current due to the differential signal at the entrance, $i_d(t)$, the load becomes an RLC resonant circuit as shown in Figure 2.6.
The equation of this circuit is

$$v_{od}(s) = Z_L(s) \cdot i_d(t) = \frac{s2L_L}{1 + \frac{s2L_L}{R_L} + s^2 2L_L C_L} \cdot i_d(t) \tag{2.10}$$

that shows the pass-band behaviour of the load of the LNA, whose need has been discussed previously. All the parameters of this element are summarized in Table 2.4.

The value of R_L directly fixes the gain of the stage and indirectly all the other parameters.

parameter	**equation**	**unit**
f_0	$\frac{1}{2\pi\sqrt{2L_L C_L}}$	Hz
$v_{od}(f_0)$	$R_L \cdot i_d(t)$	V
Q	$\frac{R_L}{2\pi f_0 2L_L}$	-
B_{-3dB}	$\frac{f_0}{Q}$	Hz

Table 2.4: RLC filter parameters.

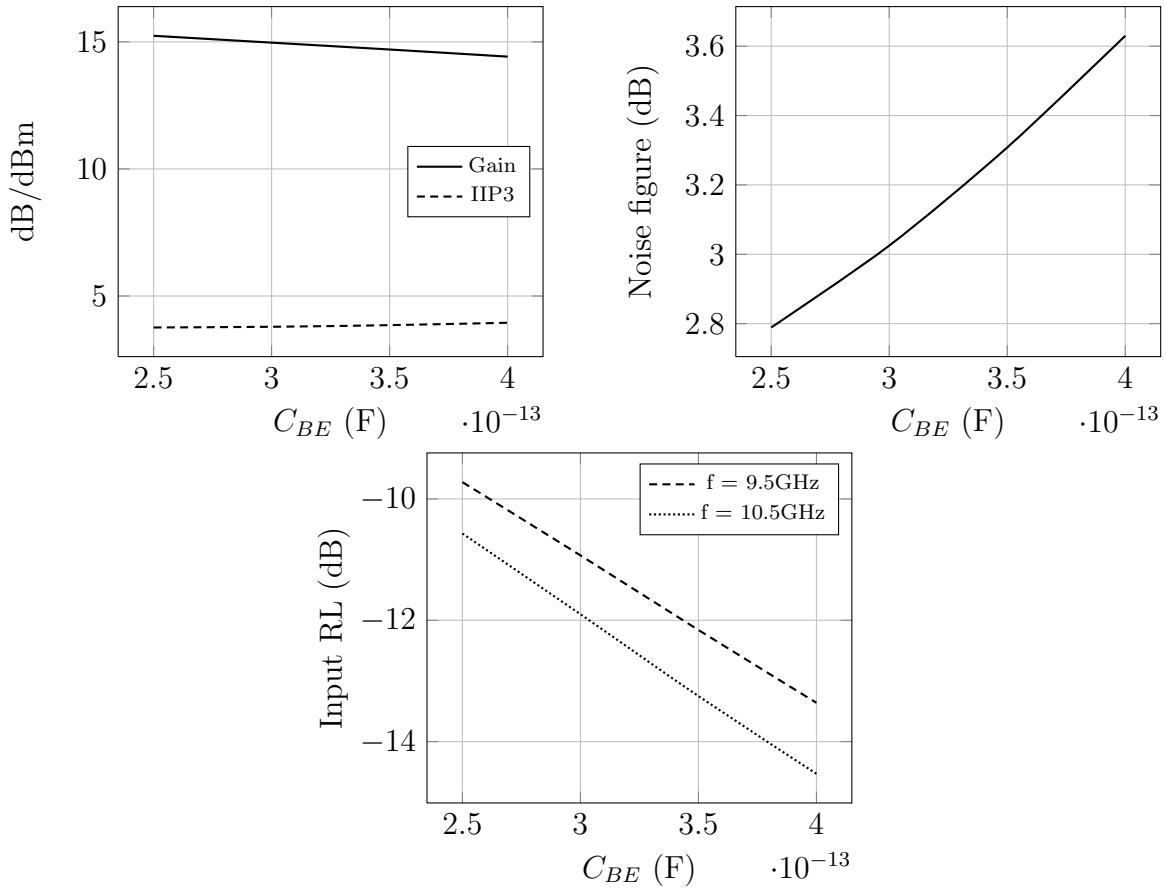


Figure 2.5: LNA's power gain, IIP3, noise figure and return loss dependency to C_{BE}.

The bandwidth it's a project constant so L_L is obtainable through the equation

$$L_L = \frac{B_{-3dB}}{2 \cdot 2\pi f_0} \cdot R_L \tag{2.11}$$

Also the value of C_L is now calculable.

$$C_L = \frac{1}{(2\pi f_0)^2 2L_L} \tag{2.12}$$

But this is valid if the impedance seen by the resonant load is infinite. To the same two nodes where the RLC is connected there are also the differential input of the buffer and obviously the collectors of the cascode stage. Ideally both these "ports" show high impedance so their influence could be negligible. At high frequency this is not completely true because of the presence of parasitic components and paths. Let's represent these extra components by an impedance Z_{par} in parallel with the resonant load. Equation 2.10 becomes

$$Z_L(s) = \frac{s2L_L}{1 + \frac{s2L_L}{R_L \| Z_{par}(s)} + s^2 2L_L C_L} \tag{2.13}$$

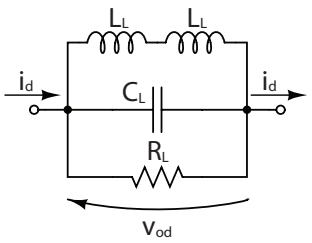


Figure 2.6: Differential small-signal model of LNA input network.

If only the influence of the buffer input is considered, that typically has an input impedance characterized by an high resistance and a capacitance in series ($Z_{par}(s) = R_p + \frac{1}{sC_p}$), it's possible to rewrite equation 2.13.

$$Z_L(s) = \frac{s2L_L\left(1 + sR_pC_p\right))}{1 + s\left(\frac{2L_L}{R_L} + R_pC_p\right) + s^2 2L_L\left[C_L + C_p\left(1 + \frac{R_p}{R_L}\right)\right]} \tag{2.14}$$

An important change is the appearance of a zero in the formula. This element is generally ignorable during the tuning because it usually influences the behaviour at higher frequency ($f_0 \ll \frac{1}{2\pi R_pC_p}$). But should take this into account when considering the stability of the system. Table 2.5 shows how the parameters of the RLC load are changed. The

parameter	**equation**	**unit**
f_0	$\frac{1}{2\pi\sqrt{2L_L\left[\frac{C_L}{2} + C_p\left(1+\frac{R_p}{R_L}\right)\right]}}$	Hz
$v_{od}(f_0)$	$R_L\frac{1}{1+\frac{R_L}{2L_L}R_CC_C} \cdot i_d(t)$	V
Q	$\frac{R_L}{2\pi f_0 2L_L}\frac{1}{1+\frac{R_L}{2L_L}R_pC_p}$	-
B_{-3dB}	$\frac{f_0}{Q}$	Hz

Table 2.5: RLC filter parameters considering Z_{par}.

introduction of buffer input impedance changes the tuning of the circuit. f_0 is shifted to lower frequency, gain is reduced and bandwidth increased. Independently on the quality of the buffer is necessary to consider its presence when tuning the load of the LNA. The same is true for the gain selection circuit, which basically change only the value of the resistive part of the load. Equations for the tuning become really complicate and it's difficult to determinate mathematically good values for all the components. During the design the circuit has been tuned using parametric simulations in Cadence. Theoretical analysis was useful, with extensive approximations, to determine which parameters to change. Graph in figure 2.7 represent how the performance of the LNA changes when R_L varies between 250 and 600 Ωs. Load and input network have already been tuned to 10 GHz by simulation. With the increase of load resistance greatly improve the gain and, as a consequence of greater signal amplification, also the noise figure. IIP3 slightly

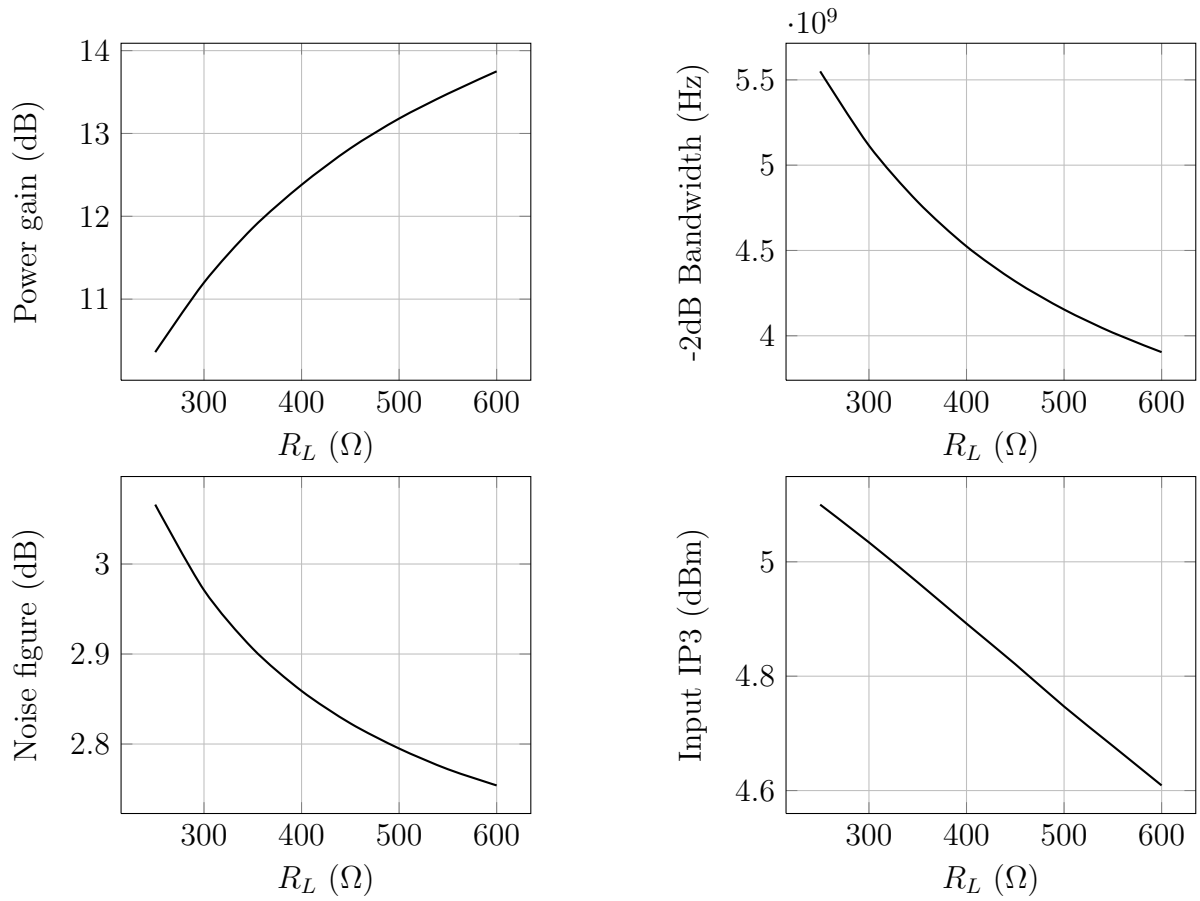


Figure 2.7: LNA power gain, -2dB bandwidth, noise figure and input IP3 according to R_L variation.

decreases because of the wider signal present between the collector and emitter of differential pair transistors. Higher Q factor reduces the bandwidth of the amplifier. 550 Ωs looks to be the maximum value to achieve a -2 dB bandwidth of at least 4 GHz.
Graph in Figure 2.8 represents the Output IP3 versus the load resistance. As already said, OIP3 combines gain and IIP3 and can be used as figure of merit. Looking at the graph is clear the possibility to increase the R_L above 600 Ω to reach an OIP3 close to 20 dBm and even better noise figure. The problem is the bandwidth. Bandwidth depends on center frequency, fixed to 10 GHz, and the Q-factor. As a first approximation the equations of table 2.4 can be used.

$$B_{-3dB} = \frac{f_0}{Q} = \frac{f_0(2\pi f_0 2L_L)}{R'_L} = 2\pi f_0^2 \frac{2L_L}{R'_L} \tag{2.15}$$

In the formula is used R'_L instead of R_L because the effective value of the resistive part of the load depends also on the gain selection circuit and buffer presence. The only way to have a bandwidth higher then 5 GHz is to keep the ratio $\frac{R'_L}{2L_L} \leq 1.25 \cdot 10^{11}$. A bigger inductor doesn't come for free: it needs more layout area and probably it's necessary to check if the lower resonance frequency affects or not the stability of the system. Finally

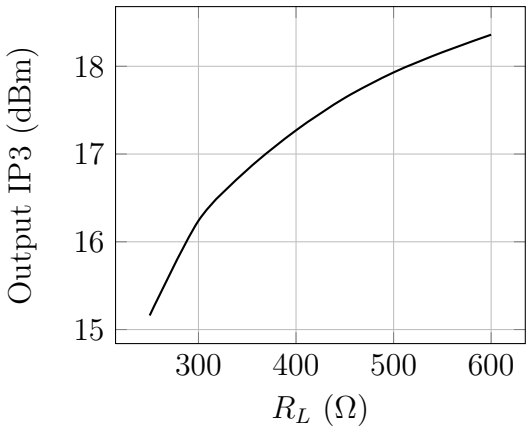


Figure 2.8: LNA output IP3 according to R_L variation.

the value taken for L_L (see 2.1.3) is around 1 nH, that means

$$R'_L \leq R'_{L,max} \approx 250\,\Omega \tag{2.16}$$

R'_L represents the resistive part of the RLC filter considering also the influence of buffer and gain selection circuit. When the load is tuned to 10 GHz these two circuit can be taken in account considering their influence as two resistors (R_{buf} and R_{sel}, respectively) in parallel with R_L,

$$R'_L = R_L \parallel R_{buf} \parallel R_{sel} \tag{2.17}$$

2.1.2 Gain selection circuit

To implement gain selection the following circuit is used:

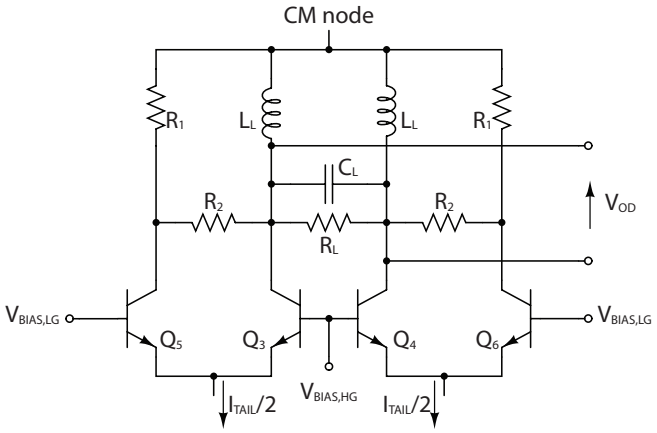


Figure 2.9: Gain selection circuit.

This structure has been described and tested by Garcia and Belot [30]. Concept at the base is really simple:

- **High Gain (HG) cascode pair selected**. LG cascode pair is switched off so the two R_1 and R_2 series are in parallel with the load. Behaviour of the LNA is the same without gain selection circuit, but with a different load resistive part.

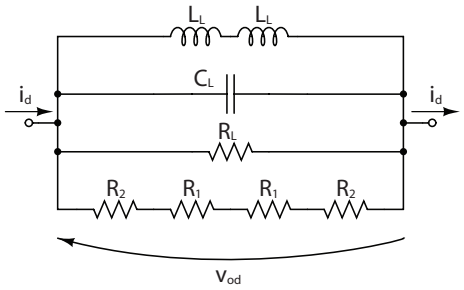


Figure 2.10: HG configuration equivalent load.

- **Low Gain (LG) cascode pair selected**. HG cascode pair is switched off, the original load is inside a current divider as shown in figure 2.11, so it receives only a fraction of the current set by the value of the resistors R_1 and R_2

In the first case the series of the 4 resistors is in parallel with R_L. It's possible to redefine the resistive part of the RLC filter as

$$R'_L = (2R_1 + 2R_2) \parallel (R_L \parallel R_{buf}) \tag{2.18}$$

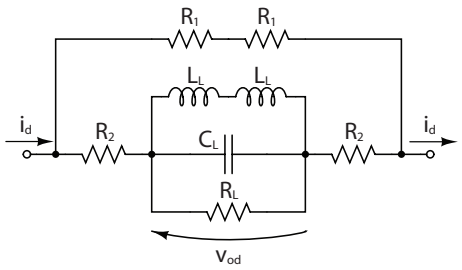


Figure 2.11: LG configuration equivalent load.

Formulas of the filter are the same shown in table 2.5 replacing R_L with R'_L. It's important to note that the series $(2R_1 + 2R_2)$ fixes the maximum value of R'_L, a limit to consider for all the parameter of the filter. If low gain option is selected the situation is different. Let's consider the load at the resonance frequency. The circuit can be redrawn as in Figure 2.12

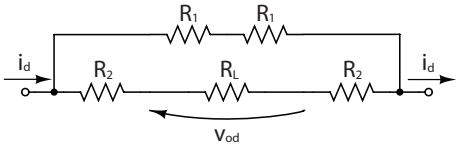


Figure 2.12: LG configuration equivalent load at f_0.

then the output voltage is

$$v_{od}(f_0) = (R_L \parallel R_{buf}) \frac{2R_1}{2(R_1 + R_2) + (R_L \parallel R_{buf})} i_d(t) \tag{2.19}$$

The other parameters of the filter are not, in first approximation, influenced. Attenuation introduced by the selection of the LG cascode stage is ideally independent from the value of $R_L \parallel R_{buf}$.

$$\begin{aligned} \Delta &= 20log\left[(2R_1 + 2R_2) \parallel (R_L \parallel R_{buf})\right] - 20log\left[(R_L \parallel R_{buf}) \frac{2R_1}{2(R_1 + R_2) + (R_L \parallel R_{buf})}\right] \\ &= 20log\left(1 + \frac{R_2}{R_1}\right) \end{aligned} \tag{2.20}$$

Δ is the difference in dBs between the two gain settings of the LNA. It depends only on the ratio between R_1 and R_2, then ideally any value for these resistors is acceptable. The problem comes out when looking at the formula of HG setting. A lower gain corresponds to a lower value of the sum of these two resistors. Then the rule is to keep them as big as possible. Analysing the circuit in detail a main drawback appears; DC current flowing in R_1, when LG option is selected, fixes collector voltage of relative cascode stage. This voltage drops with increasing current and resistance, reducing the linearity of the cascode.

Emitter voltage is fixed by the biasing circuit and cannot be reduced because it's also the voltage of input transistor collector (V_CE around 1 V means better linearity of the input stage).
Simulation of the circuit confirms this problem. A reduction of the gain usually means an improvement of the linearity of the same magnitude. In this case the linearity increases very slightly That means the maximum value for R_1 is basically fixed by the lowest

parameter	**HG**	**LG**
Power gain (dB)	13.5	9.4
Input IP3 (dBm)	4.4	5.5

Table 2.6: LNA parameters guideline.

acceptable voltage between collector and the emitter of the cascode stage to keep a good linearity (0.4÷0.6 V). The diode-connected transistor reduce the DC voltage common-mode node where R_1 and L_E are connected to 2.4 V. The biasing is set to keep the V_{CE} of the HG gain cascode stage to 1 V to afford the maximum linearity. This voltage is reduce by $(R_1 \parallel R_2) \cdot \frac{I_{tail}}{2}$ in the case of the LG cascode stage. With a biasing current of 16÷171,mA it's necessary to keep the value of the parallel of the two resistors around 60 Ω to keep a good linearity. In the pre-layout version of the LNA $R_1 = 200\,\Omega$ and $R_2 = 100\,\Omega$, then their parallel is around 67 Ω.

2.1.3 Coil design

Circuit is characterized by the presence of three couples of symmetrical inductors: L_{deg}, L_{match} and L_{load} (which coincides respectively with L_E, L_B and L_L). These have been designed with Cadence and simulated with Sonnet to determinate their S-parameters. After first simulations with ideal coils, set the required values for these components, several versions of them have been designed to find the best solution. L_{deg} and L_{match} have to be studied together because they are pretty close in the layout so it's not possible to ignore how they affect each other. In all the coils is used the minimum size for the copper (metal) layer four traces (less resistive layer for connections). This means the resistive components is relatively high and consequently Q-factor of the inductances is low; in this circuit the resistive parasitic component of the coils is not a priority, since it does not greatly affect the performance. The use of paths with small width allows to reduce the size of the coil or, using the same area in the layout, to obtain higher inductance. The path has also to support the current that flows inside it. For LNA to use the minimum size is not a problem considering the small currents present in the circuit.

Matching and degeneration coils

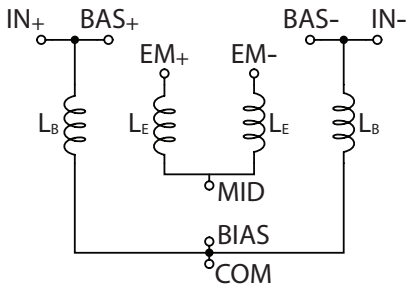


Figure 2.13: Scheme of component used in layout.

The two couples of coils are studied as single components in SONNET. Resulting S-parameter file considers all the internal relations between the single coils. The two L_E inductors are the most important part of the component because they affect directly the differential pair behaviour. These elements have to be as more similar as possible to reduce the imbalance between the two branches of the circuit. Coils occupy a certain area of the wafer so temperature and process quality non-uniformities affect the symmetry. A way to reduce this problem is to draw the turns of the inductors crossed, so that both are influenced in the same way by characteristics of the wafer. Matching inductors, characterized by a simple spiral, are placed at the sides of the structure just described and develop towards the outside while maintaining a constant height. This guarantees

the possibility to change their value while maintaining a constant size, then a simple integration into the layout. Figures 2.1.3 and 2.1.3 show the electrical scheme and the original layout of the complete component. The component has been modified during

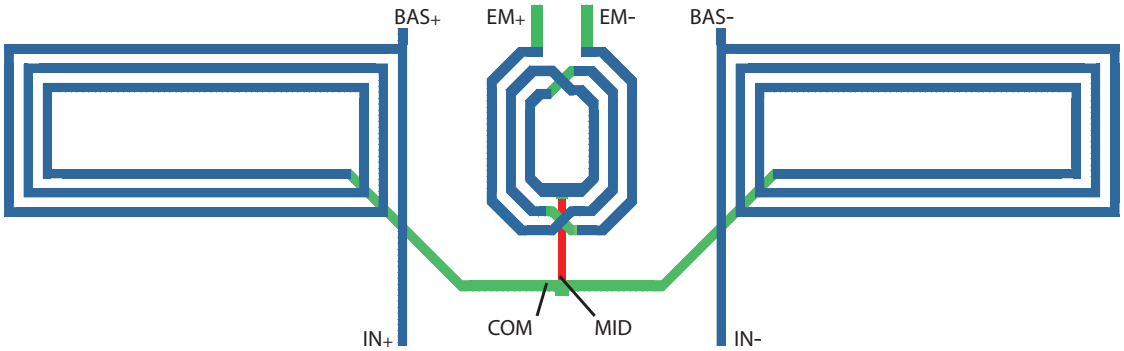


Figure 2.14: Layout of matching and degeneration coils, original version.

the layout phase. The connections of the component are changed to fit in the new layout of the LNA. During this phase it has been also decided to increase the value, then the length, of the two L_{match} coils to enhance input matching.

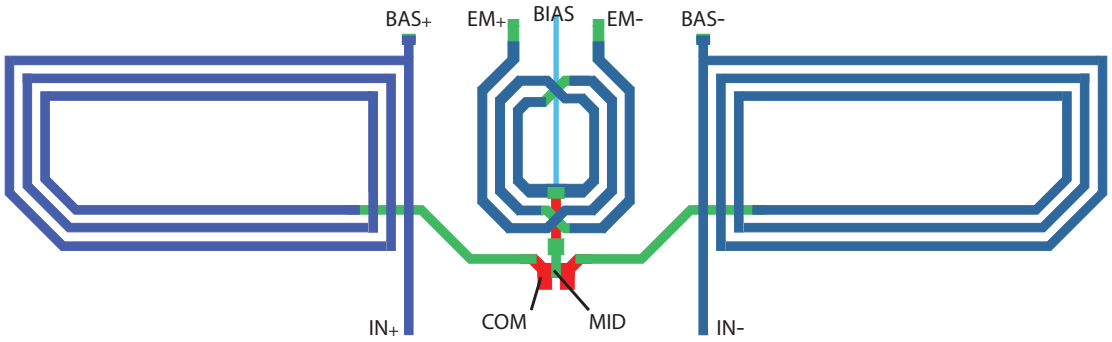


Figure 2.15: Layout of matching and degeneration coils, second version for higher return loss.

Load coils

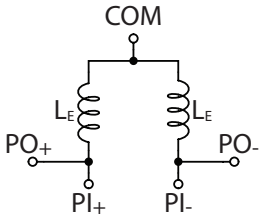


Figure 2.16: Scheme of loads inductors used in layout.

As for L_{match} the structure used for these coils is the spiral. The two inductors are placed symmetrically with respect to the main axis of the circuit and they have the

possibility to be enlarged without the need to vary the length along this axis. Original version has a good inductance value, close to 0.8 nH. It is interesting to see if can be increased this value slightly, given the proportional relationship it has with respect to the bandwidth of the amplifier. Two more version of this coil have been developed, both try to reach the target keeping the same size of the original one ($L_{load,1}$).
$L_{load,2}$, a prototype not shown here, introduces one more turn into the spiral of each coil to the first version. Inductance is higher the 1.2 nH but the resonance frequency is really close to the center frequency of the amplifier, where the gain is still high. It easily produces instability of the system. $L_{load,3}$ uses the same number of turns of $L_{load,1}$ but

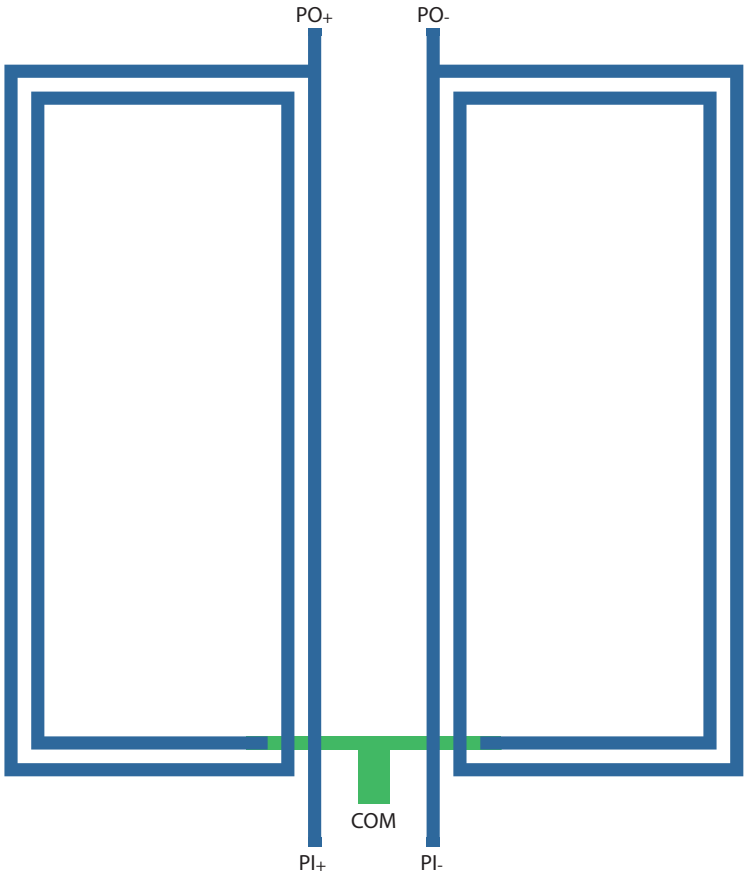


Figure 2.17: Layout of load inductances, first version with overlapped coils ($L_{load,1}$).

overlapped; the first turn is on copper (metal) layer four, the second one on copper (metal) layer three. This method reduce the Q-factor a little because of the higher resistivity of copper layer three, but the two turns are better coupled so the inductor value is increased. In this case the inductance showed by each coil is around 0.93 nH, close to the 1 nH used during first simulations.

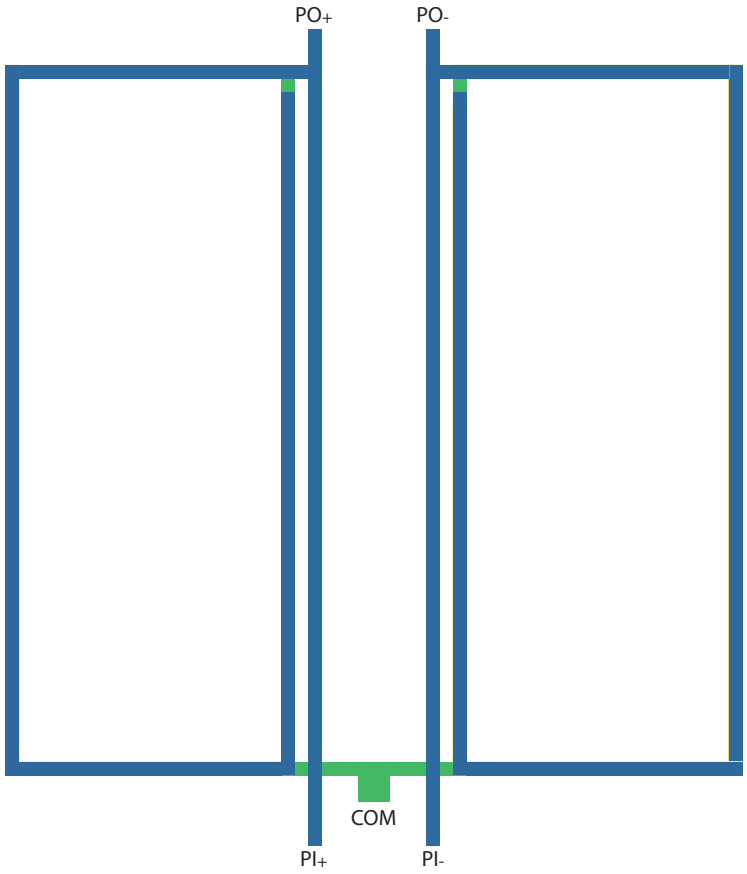


Figure 2.18: Layout of load inductances, second version with overlapped coils ($L_{load,3}$).

2.1.4 Output buffer

The structure is the same used in the original circuit: two emitter follower stages. This structure has good linearity and noise figure, quite high input impedance and the possibility to match the load easily by a resistor in series to the output paths. Output resistors value influence also gain because they create an output voltage division.

$$V'_O = \frac{R_L}{R_L + 2R_O} V_O \tag{2.21}$$

The attenuation in dB is expressed as

$$G_{Ro} = -20log\left(1 + 2\frac{R_O}{R_L}\right) \tag{2.22}$$

The approximate formula is reflected in the simulation of the circuit as can be observed in Figure 2.19. If R_O increases of $10\,\Omega$ gain is attenuated of above 1 dB. Now is necessary to observe how the output matching changes. The two graphs in Figure 2.20 show the return loss variation during simulation with different value of the output resistor.
The same variation of R_O, $10\,\Omega$, that produces an attenuation of 1 dB, increases the

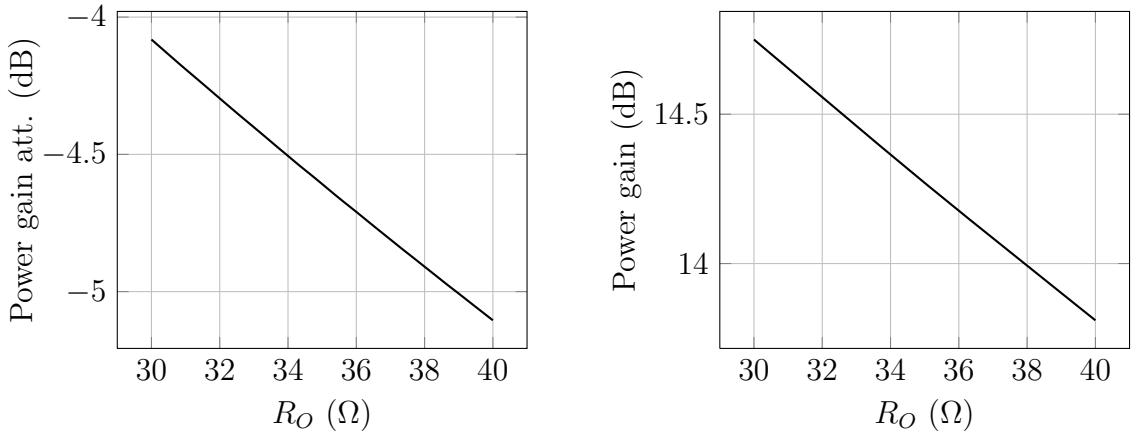


Figure 2.19: Attenuation and LNA power gain according to R_O variation.

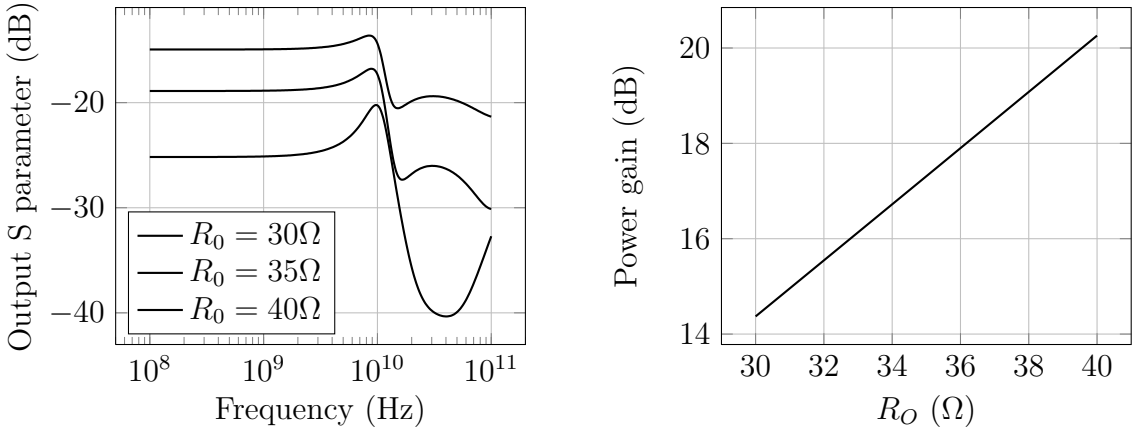


Figure 2.20: Buffer output S-parameter.

return loss of 6 dB. The request for the LNA is to have a return loss at least of 10 dB. 30 Ω looks to be a good value that doesn't decrease the gain so much and keeps a quite good matching with a 100 Ω load.

Biasing current had initially the value of 10 mA for each branch of the buffer with a total current consumption of 20 mA (66 mW @ 3.3 V). All the components have been up scaled to drive a current of 12 mA each branch (79 mW) because the buffer was limiting linearity of the LNA.

2.1.5 Design summary

In this subsection will be given all the changes made to the circuit and summarized the choices made regarding the components. It's not possible to indicate the value of all components because they are property of Infineon company.
Final structure is shown in Figure 2.21.

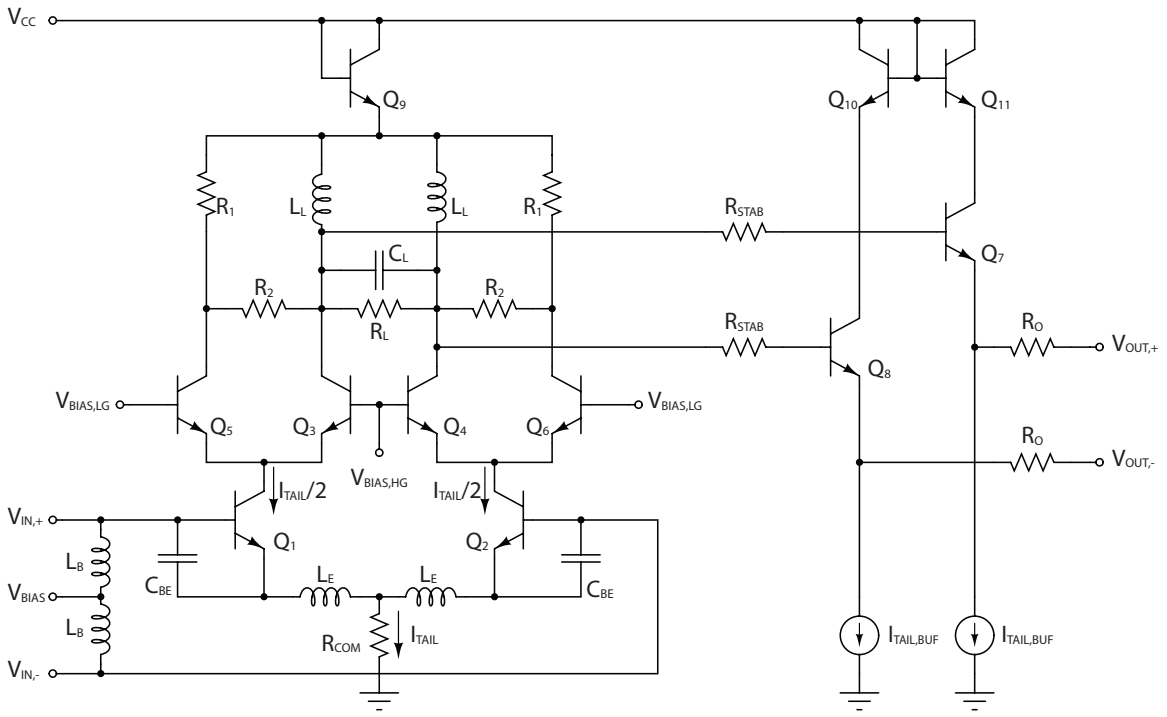


Figure 2.21: LNA structure with buffer and gain selection circuit.

Table 2.7 summarize how the principal components influence performance of the LNA. The core of the circuit is biased at 17 mA, each emitter follower of the buffer is biased

parameter	**Gain**	**NF**	**IIP3**	**BW**	**In-RL**	**Out-RL**
$L_E \uparrow$	-	-	+	o	-	o
$C_{BE} \uparrow$	-	-	+	o	+	o
$L_B \uparrow$	+	+	-	o	+	o
$R_L \uparrow$	+	+	-	-	o	o
$R_O \uparrow$	-	o	+	o	o	+

Table 2.7: LNA sensibility to components variation (+ better, - worse, o irrelevant).

at 10 mA. Relevant transistors are all high-speed NPN biased close to the maximum current tolerable to ensure good noise figure and gain. The LNA has been designed to show the highest OIP3 and the lowest noise figure without an excessive increase in power consumption. Furthermore, two configurations with different gain (+13.5 dB and +10 dB) are available. This is possible thanks to the presence of two cascode stages, with

different load biasing currents, instead of one, like in the original circuit. At the output of the LNA is connected an emitter follower differential stage (EF) as buffer, that helps to match the load at the output. Power supply voltage, V_{CC}, is set to 3.3V, V_{EE} to 0 V. The same voltages are used for the enable pins, ENI to control the LNA and EN0 to control the EF. Input and output ports are designed to match a 100 Ω differential source/load.
To select the gain are used two resistors properly biased to change the DC voltage of the respective cascode stage bases. The current flowing in these resistors is controlled by current mirrors. Reference current is given by an external source trough the two pins HG and LG. To enable a cascode stage a 0.5 mA current is needed, to disable it the current has to be increased to 1 mA. This kind of enabling circuit has been chosen to allow the control of the cascode stage biasing point during lab's measurements.
Through various parametric simulations was carried out the selection of components to achieve the required performance. Simulation results are shown in the next section.

2.1.6 Design results

The circuit is tested using two 100 Ω PORTs, as source and load. Simulations used in SPECTRE are:

- **DC analysis** to check DC biasing parameters.
- **SP analysis** to check S- paramters, noise figure, center frequency, bandwidth;
- **HB analysis** to check IIP3;

Tables summarize the results.

Freq. GHz	**Gain** dB	**NF** dB	**In-RL** dB	**Out-RL** dB	**IIP3** dBm	**f_0** GHz	**-3B BW** GHz	**-2B BW** GHz
9.5	9.35	3.10	10	20.7	5.5	9.8	5.41	4.23
10.0	9.40	3.20	-	-				
10.5	9.18	3.33	11.4	20.6				

Table 2.8: Low gain configuration LNA results (T = 27 ℃, V_{CC} = 3.3 V, P_{IN} = -40 dBm).

Freq. GHz	**Gain** dB	**NF** dB	**In-RL** dB	**Out-RL** dB	**IIP3** dBm	**f_0** GHz	**-3B BW** GHz	**-2B BW** GHz
9.5	13.35	2.52	9.9	20.7	4.4	10.0	5.37	4.17
10.0	13.48	2.60	-	-				
10.5	13.33	2.71	11.3	20.7				

Table 2.9: High gain configuration LNA results (T = 27 ℃, V_{CC} = 3.3 V, P_{IN} = -40 dBm).

Following graphs show the sensitivity of the various parameters to changes in operating temperature and supply voltage.

Power gain

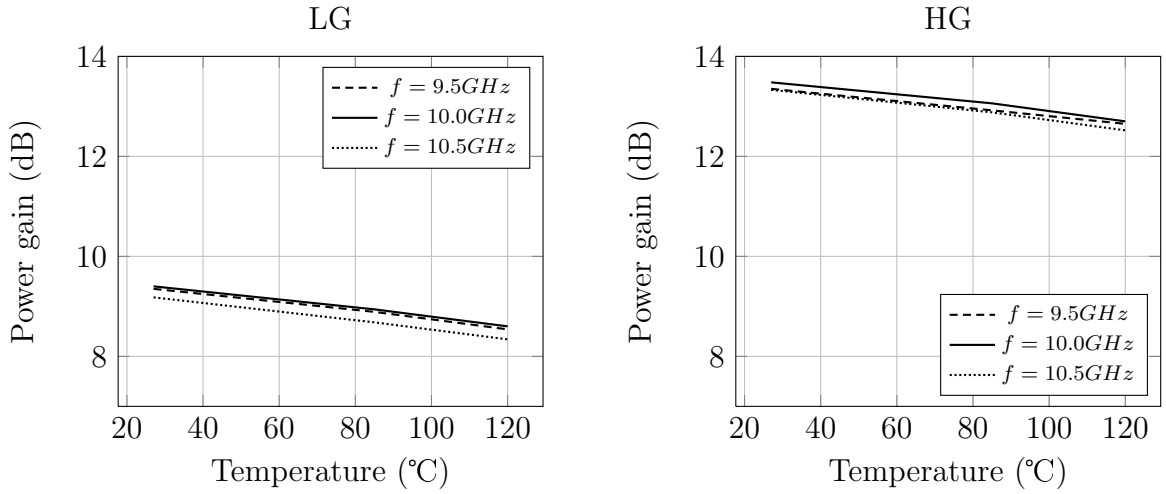


Figure 2.22: Power gain versus temperature ($V_{CC} = 3,3V$)

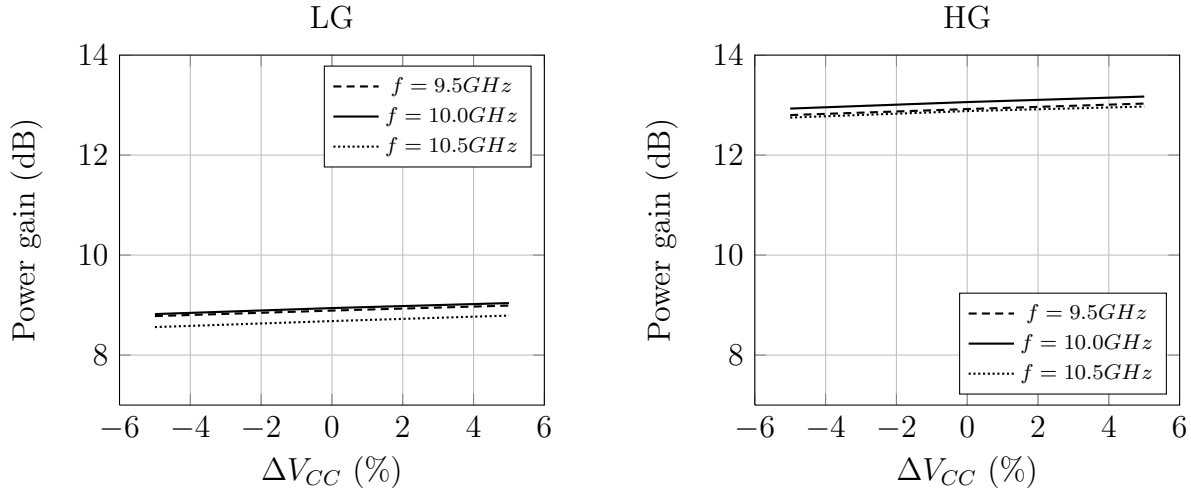


Figure 2.23: Power gain versus supply voltage variation (Temperature = 85℃)

Noise figure

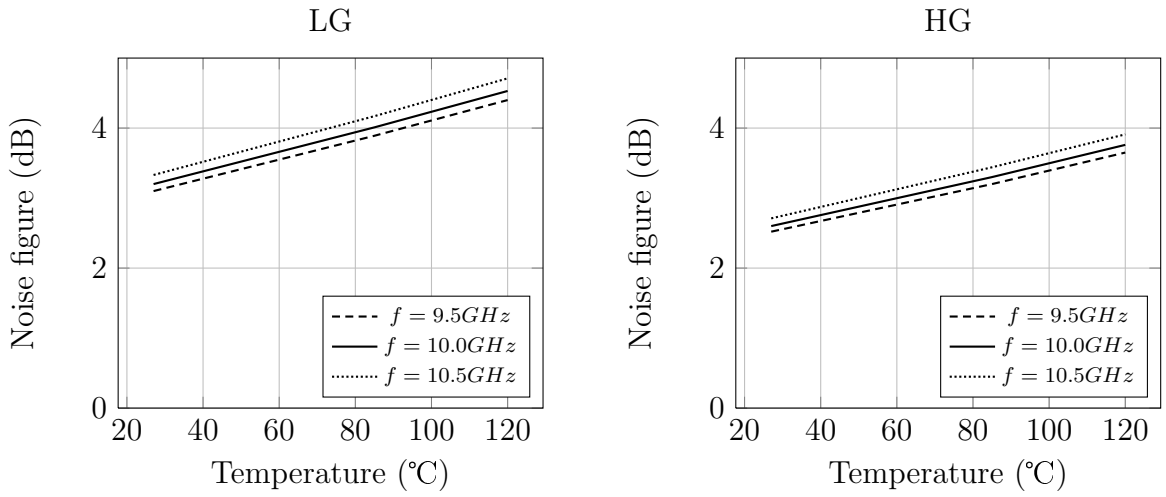


Figure 2.24: Noise figure versus temperature ($V_{CC} = 3,3V$)

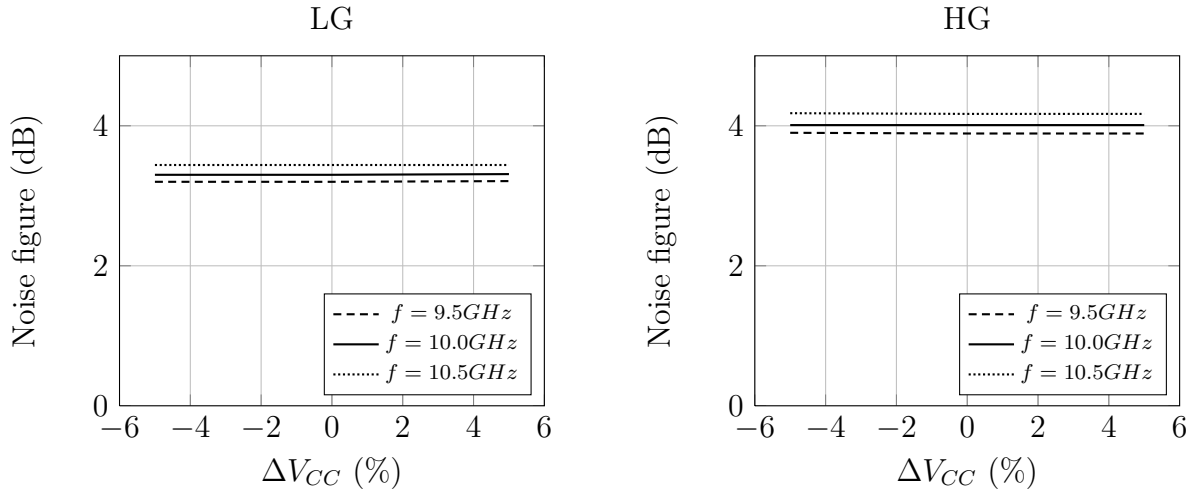


Figure 2.25: Noise figure versus supply voltage variation (Temperature = 85°C)

Input IP3

Simulation condition: $P_{RF} = -40dBm$, $f_{IN,1} = 10,5GHz$, $f_{IN,2} = 10,51GHz$. Low

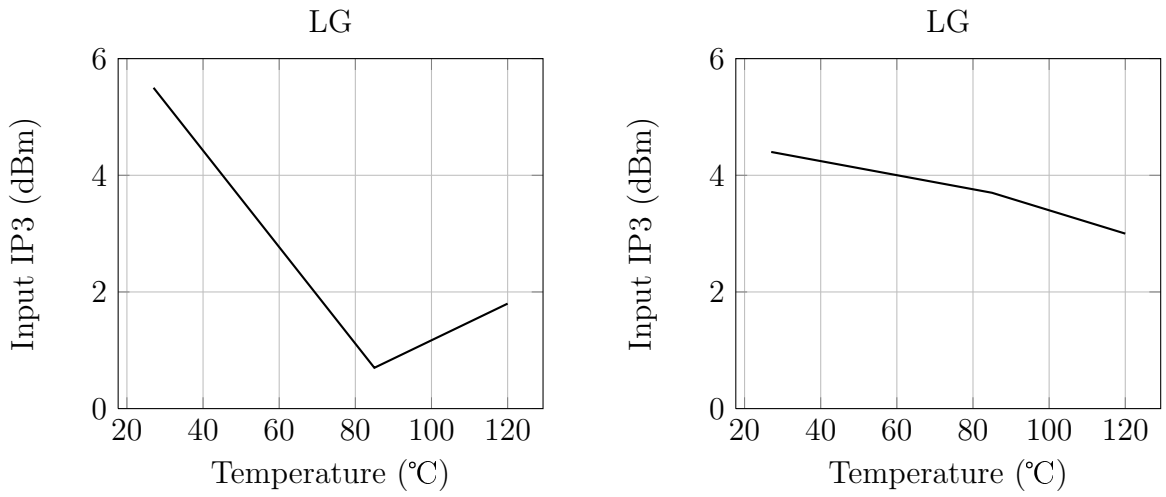


Figure 2.26: Input IP3 versus temperature ($V_{CC} = 3,3V$)

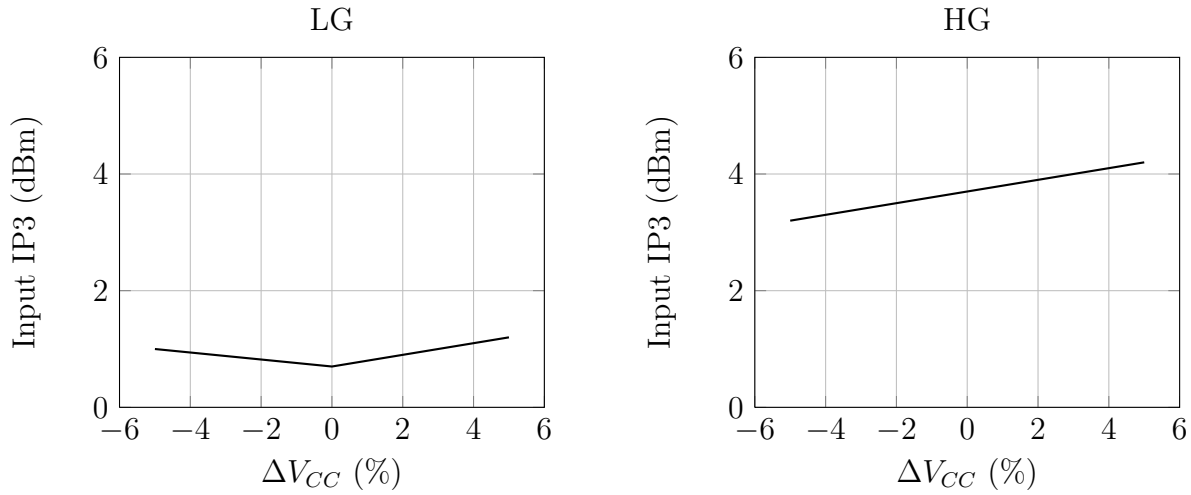


Figure 2.27: Input IP3 versus supply voltage variation (Temperature = 85℃)

gain configuration is particularly sensible to the temperature. This is due to the biasing circuit of the cascode stages. Resistors used to fix the voltage of the bases vary within the temperature reducing V_{CE}, that has already been reduce by the use of R_2 resistors. The transistor is close to the saturation region and the linearity is really low. It's necessary to compensate this drawback increasing the current injected in LG and HG pads.

Input return loss

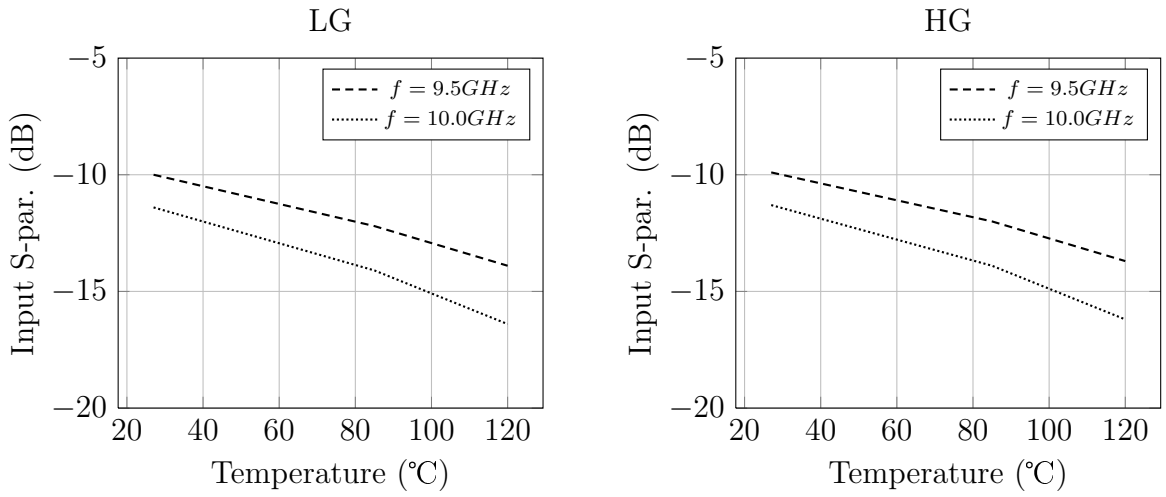


Figure 2.28: S_{11} versus temperature ($V_{CC} = 3,3V$)

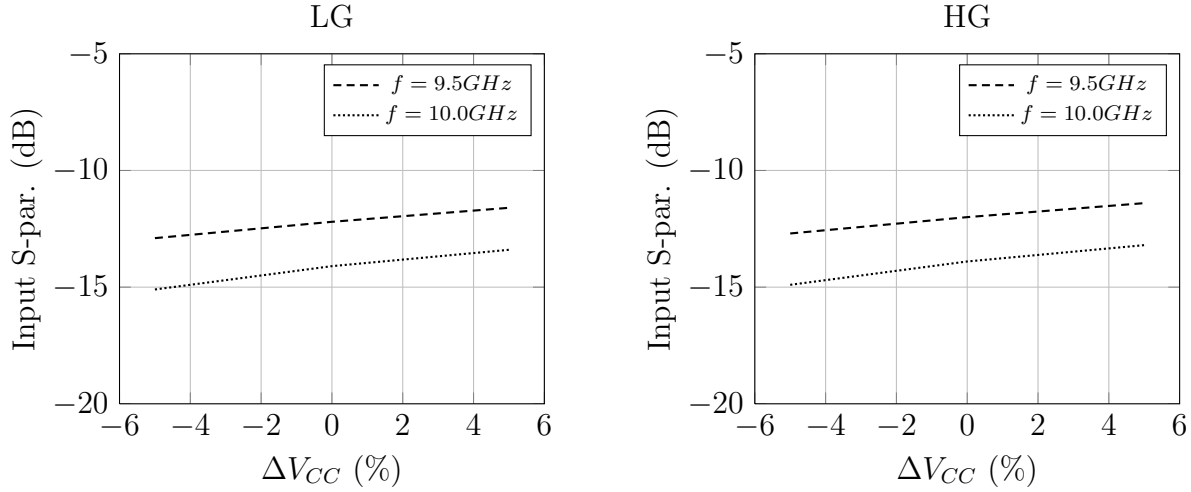


Figure 2.29: S_{11} versus supply voltage variation (Temperature = 85°C)

Input return loss is really close to the minimum value of 10 dB. In particular, at a temperature of 27C, it's below the limit (9.9 dB). Considering the negative influence of parasitic components coming from the layout phase, it's necessary to improve this parameter. The solution is to use the second version of the matching inductors which presents bigger coils.

Output return loss

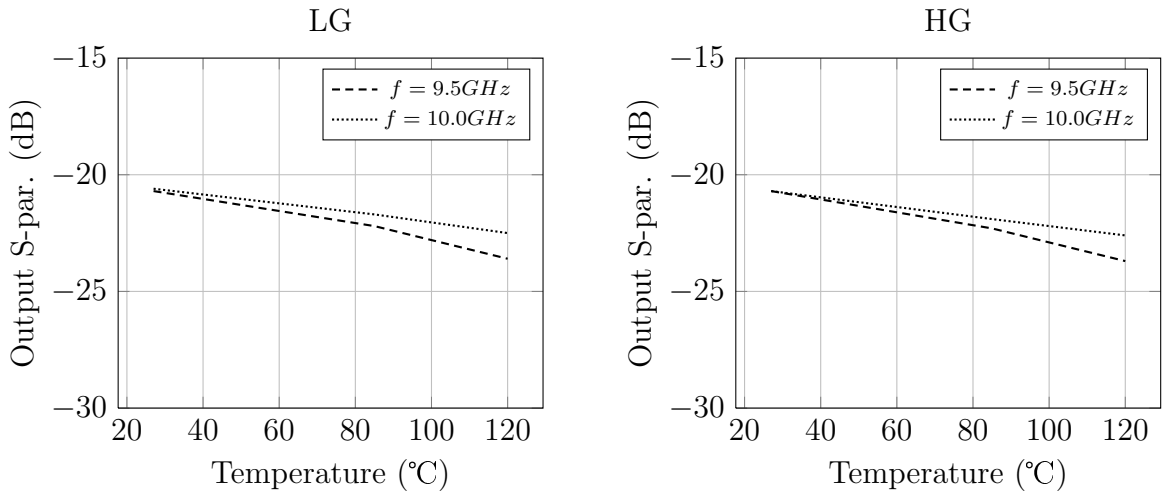


Figure 2.30: S_{22} versus temperature ($V_{CC} = 3,3V$)

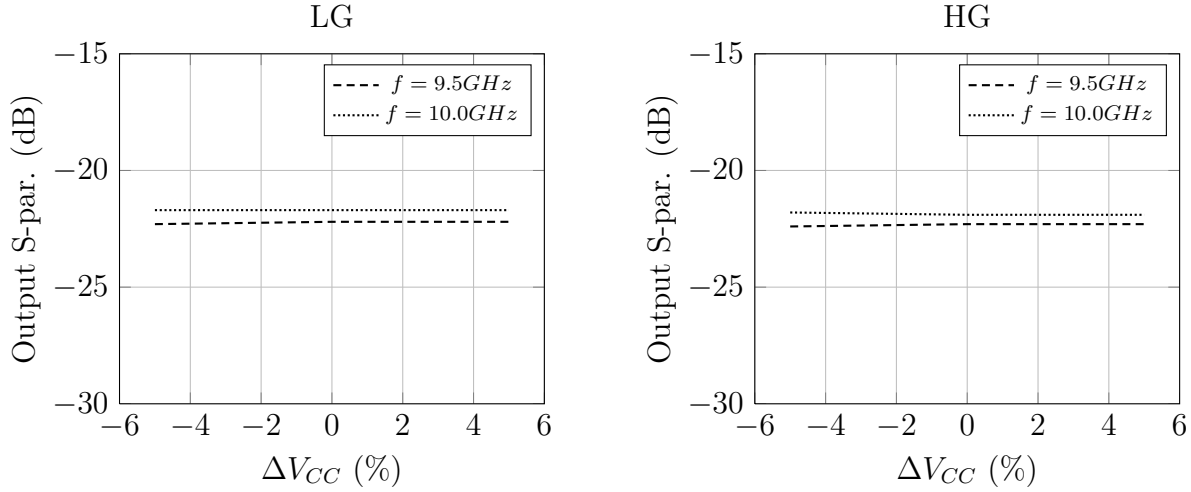


Figure 2.31: S_{22} versus supply voltage variation (Temperature = 85℃)

Power consumption

Conf.	27 °C	85 °C	120 °C
LG	133 mW	131 mW	127 mW
HG	133 mW	131 mW	127 mW

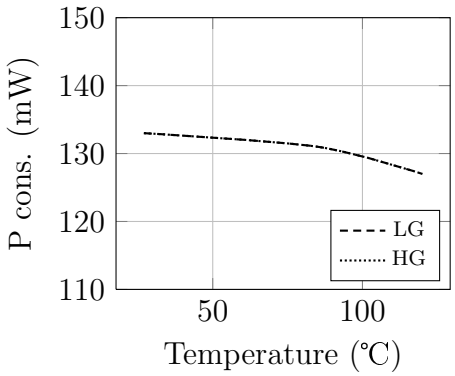


Figure 2.32: LNA power consumption sensibility to temperature variation ($V_{CC} = 3.3\,V$).

The power consumption due to the circuits for the control of the gain selection, the also the biasing of the two cascode stages, is not considered here.

Conf.	-5%	0	-5%
LG	117 mW	133 mW	147 mW
HG	117 mW	133 mW	147 mW

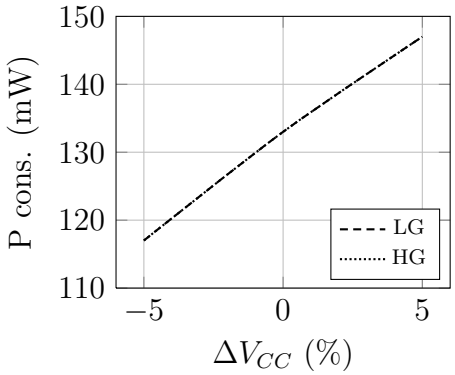


Figure 2.33: LNA power consumption sensibility to supply voltage variation (T = 85°C).

Power gain and noise figure versus frequency

Simulation condition: $T = 27\,℃$, $V_{CC} = 3.3\,V$.

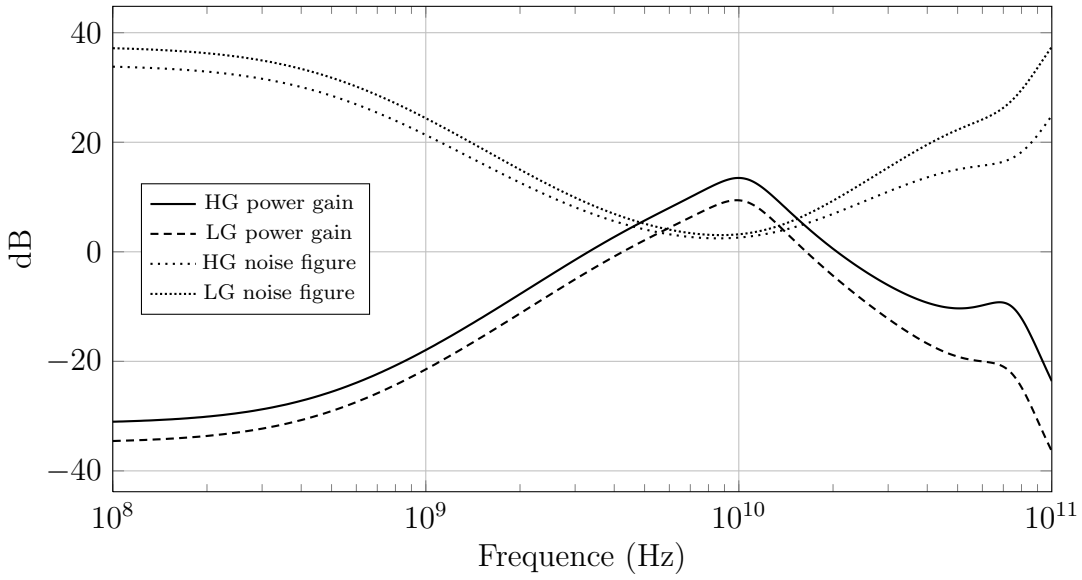


Figure 2.34: Power gain and noise figure versus frequency.

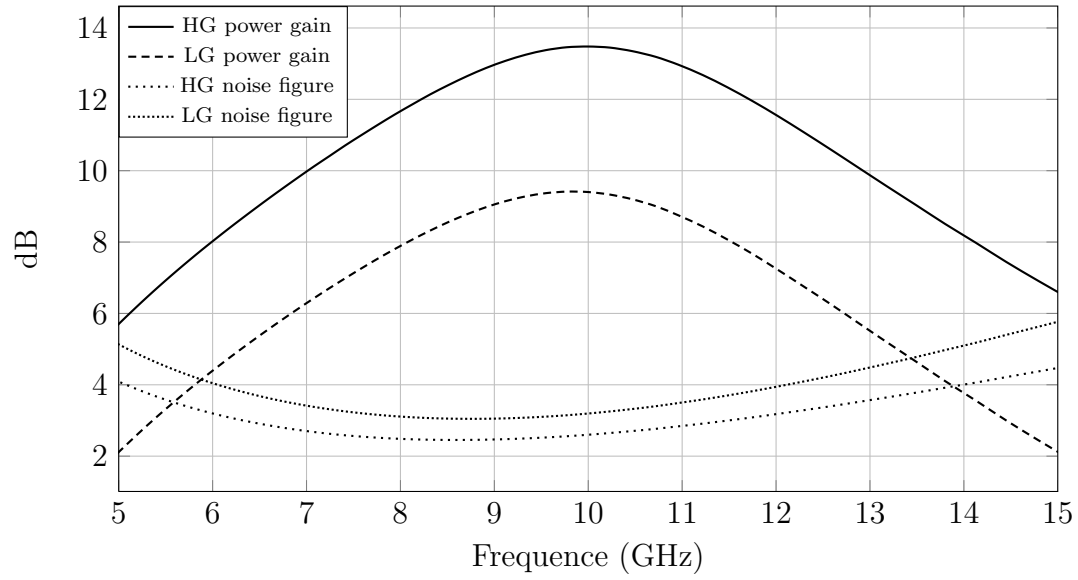


Figure 2.35: Power gain and noise figure versus frequency (enlarged version).

Input and output return loss versus frequency

Simulation condition: $T = 27\,℃$, $V_{CC} = 3.3\,V$.

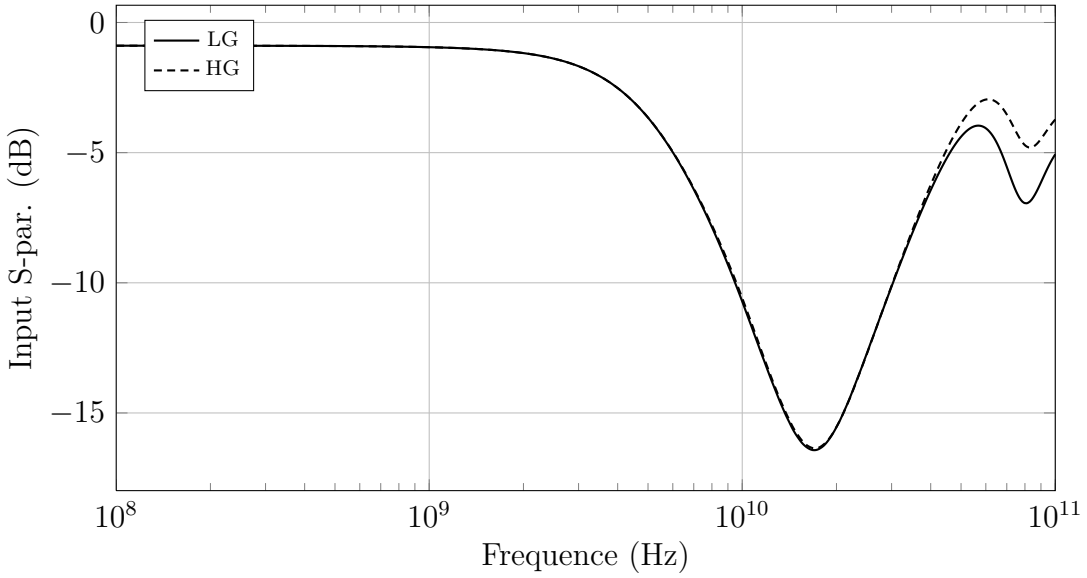


Figure 2.36: LNA input S-parameter versus frequency.

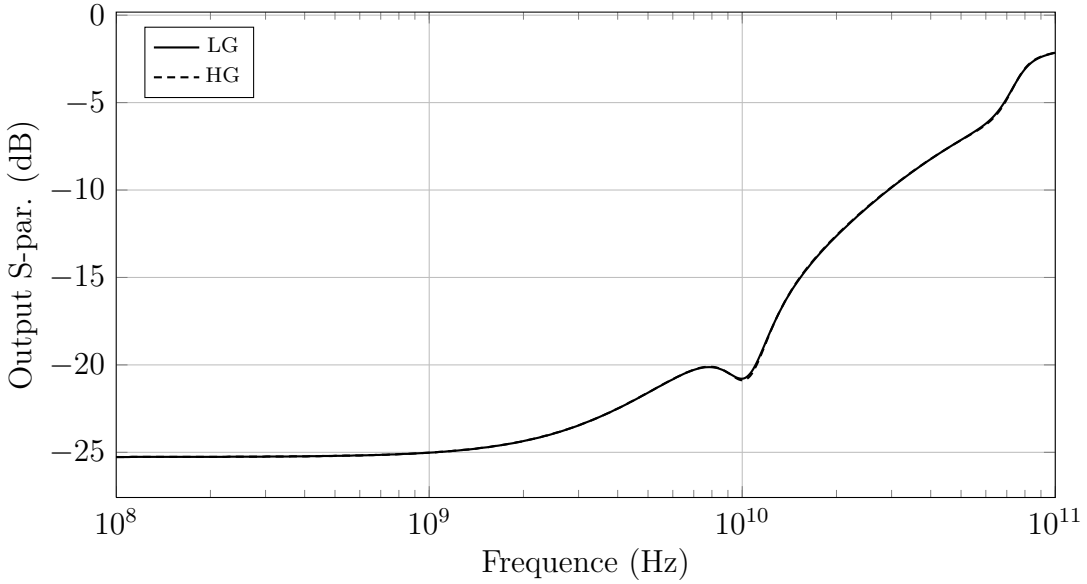


Figure 2.37: LNA output S-parameter versus frequency.

2.1.7 Stability

Stability check uses an SP analysis in the range 100 MHz ÷ 100 GHz. Temperature is set at -40 ℃ and supply voltage at 3.6 V, the worst case for stability. As source and load two PORTs are used in series with a big cap to not influence the biasing of the circuit. Their impedance is 100 Ω in case of differential input/output or 50 Ω in the other cases. Different configurations have been checked:

- differential input to differential output;
- singular input to in-phase output;
- singular input to opposite-phase output;
- two singular inputs with open circuit at the outputs;
- two singular outputs with open circuit at the inputs.

As seen in subsection 1.2.5, the stability is guaranteed using SPECTRE for each type of source and load if the following conditions are verified at all the frequencies of the band analysed;

$$K_f > 1 \qquad b_1, f > 0 \tag{2.23}$$

The two resistors R_F were already present in the original circuit to eliminate a stability problem produced by the EF buffer. First stability check has shown instability at 60-70 GHz. This problem is solved considering the parasitic inductive component introduced by the path that connect the differential pair collectors and the cascode stages emitters (∼50 pH), which reduce the gain at this frequencies. Considering these changes, the stability is checked again on the final circuit. Results are reported in Table 2.10.

	LG		**HG**	
	K_f	$\beta_{1,f}$	K_f	$\beta_{1,f}$
Differential input and output	ok	ok	ok	ok
Input + and output +	ok	ok	ok	ok
Input + and output -	ok	ok	ok	ok
Differential input and floating outputs	ok	ok	ok	ok
Floating inputs and differential output	ok	ok	ok	ok

Table 2.10: LNA design stability results.

2.2 Quadrature mixer

The starting point is a 3.3 V 4 GHz-IF mixer with a driver to amplify the LO signal and drive the switching pairs of a Gilbert double-balanced structure. The first target is to retune the circuit to 10 GHz. Before to decide to design separate test-chips for LNA and mixer, the second goal was to achieve also high linearity to fit the output signal characteristics of the LNA. A second request was a LNA+mixer gain of at least 20 dB. If the LNA as a gain of $13.5 \div 14.0$ dB mixer has to reach a minimum conversion gain of 6 dB. With a first block showing an OIP3 of 18 dBm is necessary a circuit with an IIP3 at least of 22 dB (see Equation 1.15. Last but not least, considering a NF of 2.8 dB for the LNA, a total noise figure of maximum 3.5 dB is reachable with a 10 dB DSB-NF mixer. Table 2.11 summarizes the targets described above. The decision to design a test-chip

parameter	**condition**	**min**	**typ**	**max**	**unit**
Center frequency	-	-	10	-	GHz
Power gain	T = 27 ℃, f_{RF} = 10.5 GHz	6	-	-	dB
DSB noise figure	T = 27 ℃	-	-	7	dB
Input IP3	T = 27 ℃	14	-	-	dBm
RF-port return loss	T = 27 ℃	10	-	-	dB
LO-port return loss	T = 27 ℃	10	-	-	dB
IF-port return loss	T = 27 ℃	10	-	-	dB
RF-input band	-	9	-	11	GHz
IF-output band (-1dB)	-	0.5	-	-	GHz
Op. temperature	-	-40	-	120	℃

Table 2.11: Quadrature mixer parameters guideline.

for each block has not changed these reference parameters. The analysis will start with the circuit core, Gilbert double balanced structure. All other parts of the mixer directly depend on it and will be discussed later in the section.

2.2.1 Gilbert double-balanced mixer

The structure used is derived from the one analysed in the first chapter (see Section 1.3.7). Figure 2.38 shows the circuit will be discussed. RF-input differential pair structure is similar to LNA's one. Only the inductors L_B have been replaced with two resistors R_B and there are not the capacitors C_{BE} to tune the input. It's therefore easy to rewrite equations.

$$Z'_{IN}(s) = r_b + g_m \frac{L_E}{C_\pi} + sL_E + \frac{1}{sC_\pi} \tag{2.24}$$

$$\begin{aligned} Z_{IN}(s) &= 2\left(R_B \parallel Z'_{IN}\right) \\ &= 2R_B \frac{1 + s\left(r_b C_\pi + g_m L_E\right) + s^2 L_E C_\pi}{1 + s\left[\left(r_b + R_B\right) C_\pi + g_m L_E\right] + s^2 L_E C_\pi} \end{aligned} \tag{2.25}$$

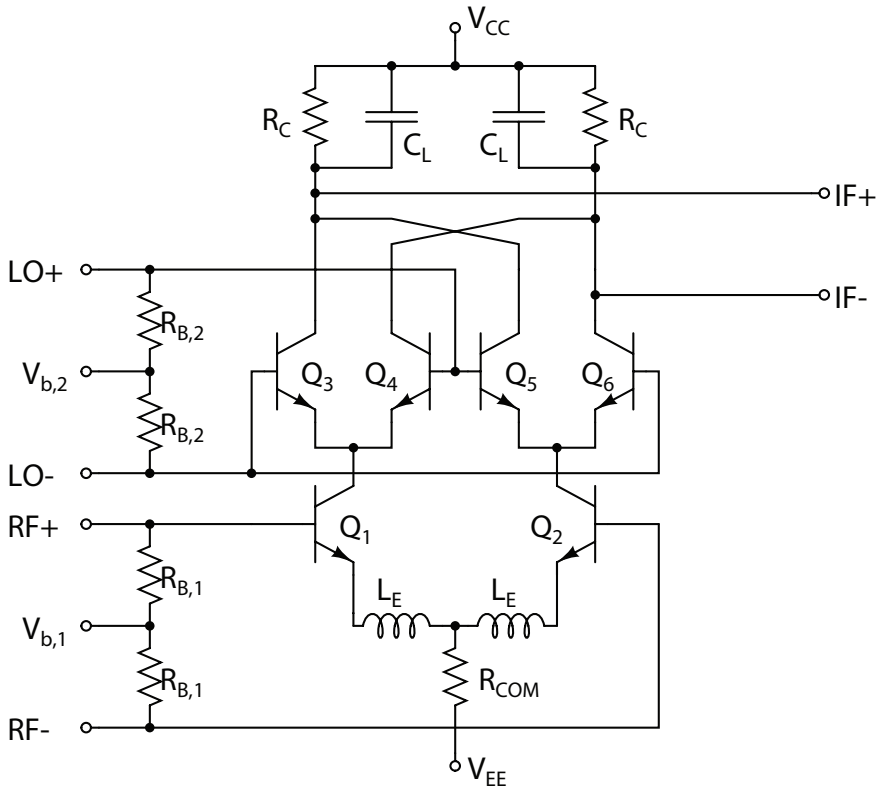


Figure 2.38: Mixer structure used in this work.

$$\frac{I_d}{V_s}(s) = g_m \cdot \frac{R_B}{R_S + R_B} \cdot \frac{1}{1 + s\left[(r_b + R_b \parallel R_s)\, C_\pi + g_m L_e\right] + s^2 L_e C_\pi} \tag{2.26}$$

Transfer function between the collector current and input voltage is characterized by low-pass behaviour with $f_C = \frac{1}{2\pi\sqrt{L_E C_\pi}}$. C_π depends on the size of the devices, which is also related to the linearity, as g_m. L_E influence also linearity and noise figure, because it is the degeneration inductor. Table 2.12 summarizes how the various components influences the performance of the differential pair.

parameter	**Gain**	**IIP3**	**NF**	f_C	Z_{in}
$L_E C_\pi \uparrow$	$\downarrow$	$\uparrow$	$\uparrow$	$\downarrow$	*
R_B	$\uparrow$	*	*	-	$\uparrow$
g_m	$\uparrow$	*	$\downarrow$	-	$\uparrow$

Table 2.12: Mixer parameters guideline.

The load of the mixer was initially composed by only the two resistors R_L, as needed for the baseband output signal. Two capacitors, C_L, have been added to cut high frequency and reduce the possible intermodulation between the output signal and spurious products of down-conversion. Providing a -3dB-bandwidth above 1 GHz for this filter it is possible to increase the linearity with a minimal reduction of in-band gain. The bandwidth depends not only on these two components; it is influenced also by the presence of the

load. This is also valid for all the other parameters of the mixer. Therefore load affects heavily the analysis of the circuit.

$$Z_L(s) = \frac{2R_C}{1 + s4R_CC_C} \parallel Z_{buf}(s) \tag{2.27}$$

Z_L is the differential load seen by the mixer, Z_{buf} is the differential input impedance of the external load. If a $100\,\Omega$ load is considered it's easy to understand that R_L resistors cannot be considered the only components which convert differential current into differential output voltage. A buffer with really high input impedance allows to reduce the influence of the load on mixer performance as for LNA. Considering now the presence of the buffer and a perfect square-wave LO signal, conversion gain is expressed by the Equation 2.28.

$$\begin{aligned} G_C(s) &= \frac{V_{od}}{V_{id}}(s) \\ &= g_m \cdot \frac{R_B}{R_S + R_B} \cdot \frac{1}{1 + s\left[g_mL_E + C_\pi\left(R_B \parallel R_S\right)\right] + s^2L_EC_\pi} \cdot \\ &\cdot \frac{2}{\pi} \cdot \left(\frac{2R_C}{1 + s4R_CC_C} \parallel Z_{buf}(s)\right) \end{aligned} \tag{2.28}$$

If the buffer has high impedance and the equation is considered at the input frequencies around 10 GHz, it becomes

$$G_C \approx \frac{2}{\pi} g_m(2R_L)\frac{kR_B}{R_B + R_B} \tag{2.29}$$

Parameter **k** represent the module of the frequency-dependent part of equation 2.26 and it's lower then 1. It depends on L_E and the size of the transistors used in the differential pair. The same parameters heavily influence linearity and noise figure as in the LNA. This means that, even in this case, the choice of input components is the result of a compromise between gain, linearity and noise figure.

As already said for the LNA, high speed transistors need a V_{CE} close to 1 V to achieve best linearity. This is particularly important for the differential pair that heavily influences this parameter. The two switching pairs can be considered as cascode stages. Their V_{CE} can be less then 1V but not as much as in the LNA because driven signal has a greater amplitude. Simulations return the range $0.8 \div 1.0\,\text{V}$ for V_{CE}. Considering a voltage for the common mode resistor of 0.2 V, the range of voltage for the load resistors is $1.3 \div 1.5\,\text{V}$ with a supply voltage of 3.3 V. If the supply voltage is increased to 5 V the range becomes $3.0 \div 3{,}2\,\text{V}$ and load resistors can be much bigger, as the gain achieved. Costumer decided to keep 3.3 V supply voltage for the LO driver circuit which implies the need for DC decoupling the two circuits by capacitors, in case of a 5 V-supplied mixer. Use of these caps will be discussed in subsection 2.2.7. After deciding on the type and size of the transistors of the differential pair, having set the current in order to bias

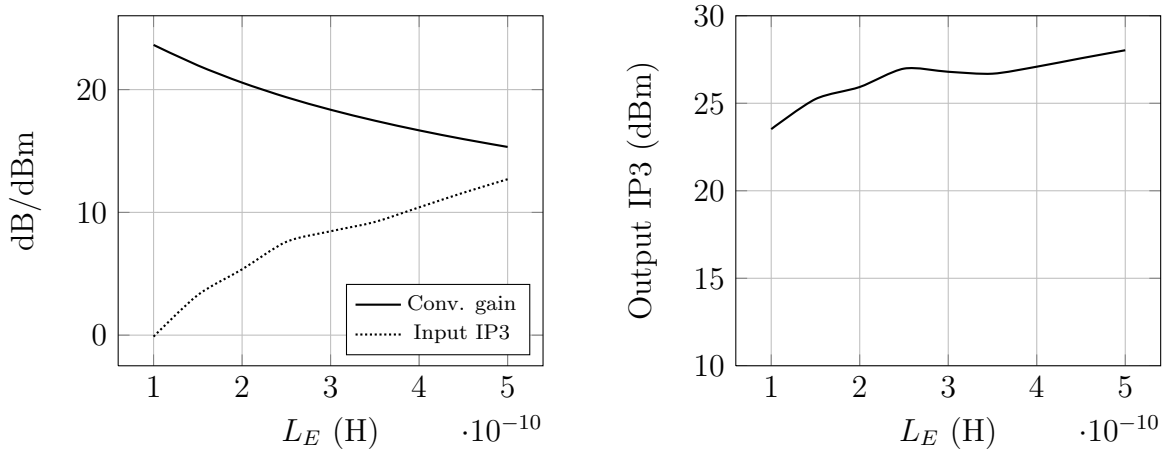


Figure 2.39: Single mixer conversion gain, input and output IP3 according to selected degeneration inductance value.

the devices properly, the component which sets the performance of the mixer and on which it's possible to work is L_E. An increase of the value of this inductance involves an improvement of linearity and a gain reduction, behaviour directly related to its use as feedback. A secondary effect is the increase in noise figure due to the resistive element of the real component. It was decided to consider first the noise, to see if it is possible to reach the performance required when LNA and mixer are connected together. It has already been said that, with the performance in terms of gain and noise figure of LNA, a mixer with a DSB noise figure of around 10 dB is needed. This is the starting point for the parametric simulations used to find component's values.

Following results come from simulation of a single Gilbert double-balanced mixer using ideal inductors with a resistive part proportional to the size of the component. Differential pair is biased with a 40 mA current and transistors used are sized to ensure maximum gain, without destroying linearity.

Figure 2.39 reports how conversion gain and linearity change according the variation of the degeneration inductors. To keep in mind a bigger coil means a higher noise figure. Figure 2.40 reports how conversion gain and linearity are affected by the value of the load resistor.

The analysis of these results crossed with the achieved noise figure returns the values for the two components: $L_E = 350 \div 400\,pH$ and $R_L = 140 \div 150\,\Omega$. This configuration return a conversion gain of $16 \div 17$ dB and an IIP3 of above 10 dBm. Finally the SSB-NF is close to 10 dB that mean a DSB-NF of 7 dB for each Gilbert mixer. Where two mixers are combined together, taking in account the presence of a transformer at the RF-input (see Section 2.2.6) with an insertion loss of 3 dB, the total DSB-NF is 10 dB has requested. To improve linearity is necessary to increase the value of L_E that mean a higher noise figure. The starting requests are no affordable all together.

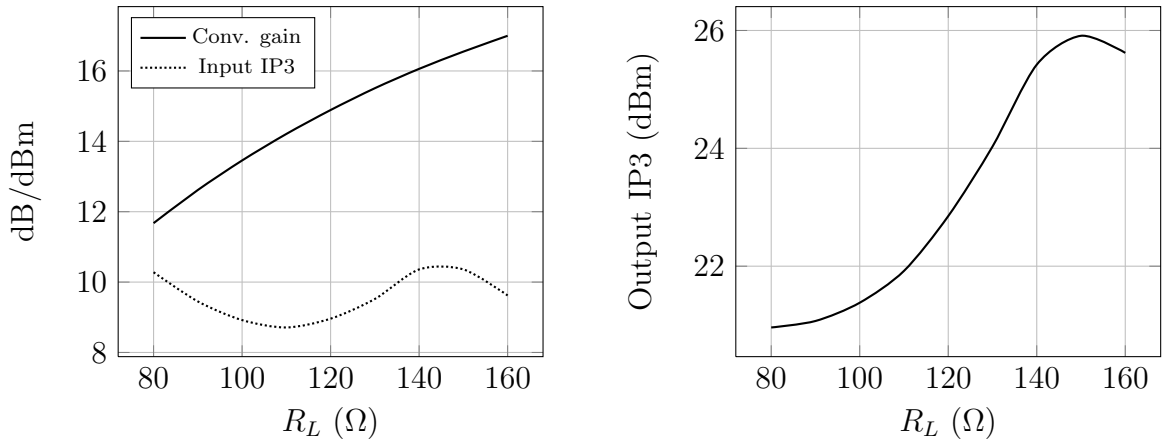


Figure 2.40: Single mixer conversion gain, input and output IP3 according to selected load resistance value.

2.2.2 Buffer

Figure 2.41 shows three topologies have been studied.
Before to start to discuss the various circuits, note all of them share the same input transistor configuration, a degenerated common emitter stage. Therefore following equation can used for all the versions of the buffer, considering an alternative model of the transistor, good at low frequencies (base-emitter impedance is represented by the parallel between r_π and C_π).

$$\frac{I_c}{I_b}(s) = \frac{g_m r_\pi}{1 + s r_\pi C_\pi} = \frac{\beta}{1 + \frac{s}{\omega_C}} \tag{2.30}$$

$$Z_{IN}(s) = \frac{r_\pi}{1 + s r_\pi C_\pi} + Z_E \left(1 + \frac{g_m r_\pi}{1 + s r_\pi C_\pi}\right) \tag{2.31}$$

$$\approx Z_E \frac{\beta}{1 + \frac{s}{\omega_C}} \tag{2.32}$$

$I_b(s)$ and $I_c(s)$ are respectively base and collector current Laplace transform, Z_{IN} the input impedance of the stage. As it's possible to see from the equation input impedance strongly depends on the size of the device. A bigger device means higher g_m but also bigger C_π, so ω_C is reduced. This has to be taken in account especially when choosing the type of transistor to use. Actually the circuit in Figure 2.41(b) is a variant of the circuit in Figure 2.41(a), which uses a common collector stage before R_F to limit the influence of the feedback path on the output of the buffer.
If, initially, it's ignored influence of the feedback between the collector and base, the two circuits have the same structure, a common emitter stage. The gain has the following

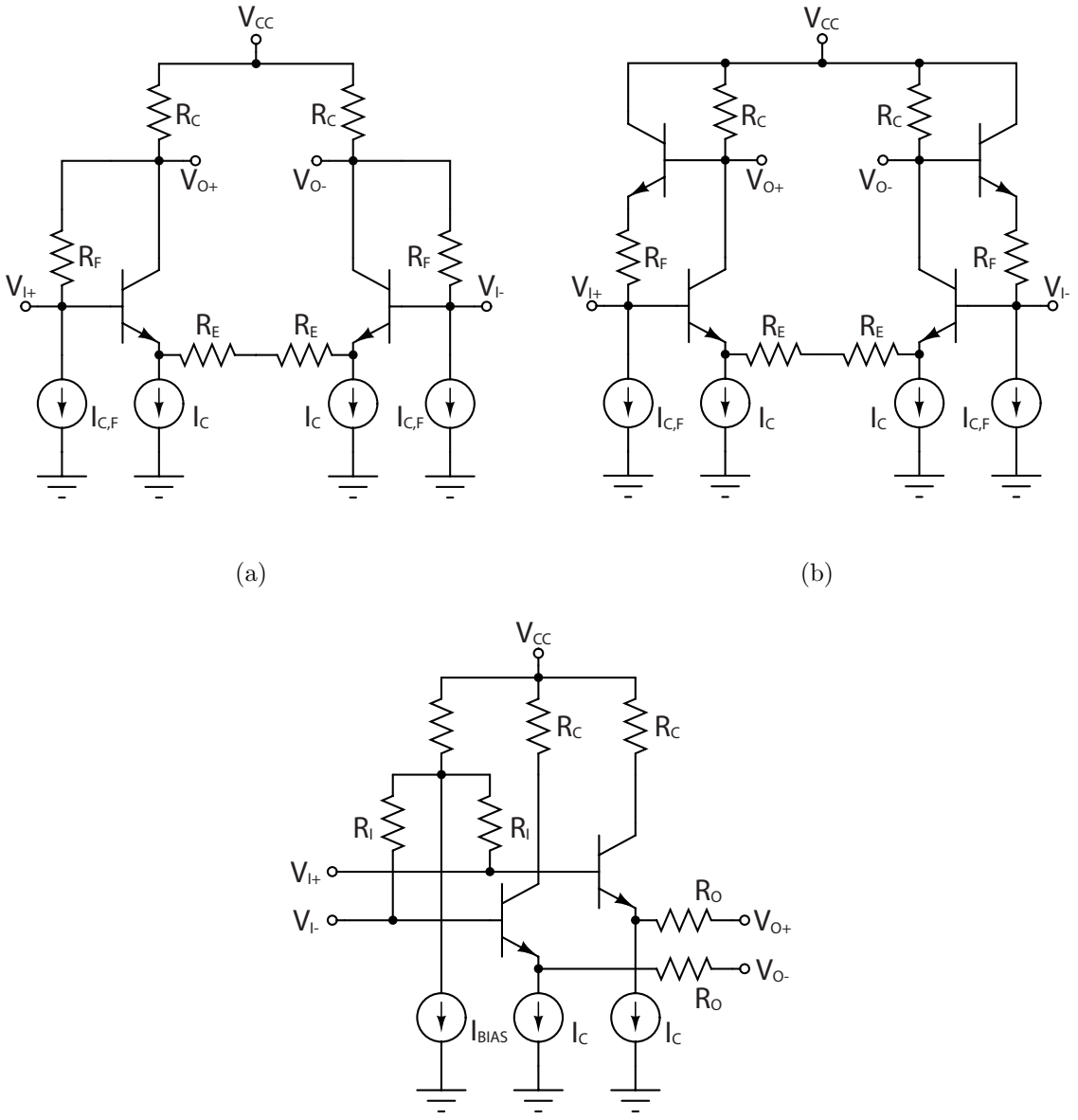


Figure 2.41: Studied topologies for mixer buffer.

equation,

$$\frac{V_{out}}{V_{in}}(s) = -\frac{1}{Z_{in}(s)} \cdot g_m r_\pi \cdot \frac{1}{1 + s r_\pi C_\pi} \cdot Z'_L \tag{2.33}$$

$$\approx -\frac{Z'_L}{Z_E} \tag{2.34}$$

where $Z'_L = Z_L \parallel Z_C$. Load impedances, in this case, is the characteristic impedance $Z_0 = 100\,\Omega$. $Z_C = 2R_C$ and it fixes also the matching with the load. As a first approximation, in fact, the output impedance of a single stage common emitter coincides impedance connected to the collector.

$$Z_{out,a} \approx Z_{out,b} \approx 2Z_C \tag{2.35}$$

This value has to be as close as possible to $100\,\Omega$, then $Z_C \approx 50\,\Omega$. Gain without load connected to the circuit decreases of 6 dB when connecting Z_L.
A buffer has to afford at least a gain equal to 1, to not reduce the performance of the mixer. If these conditions are combined with Equation 2.34 a maximum value for the degeneration resistors appears.

$$R_E < 50\,\Omega \tag{2.36}$$

As a matter of fact this limits the possibility of using the degeneration to linearize the circuit. The only way to do it is to work on the other feedback path.
Circuit (a) uses the resistors R_F in the C-B paths. Increasing the amount of signal taken from the output and reported to the input, IIP3 grows as increasing the value of the degeneration resistor R_E. Feedback helps to increase the linearity of the amplifier but it also influences the performance of the common emitter amplifier. Following equations shows what happen to the gain and to the input impedance in circuit (a).

$$A_a = -\frac{Z_C}{Z_E} \cdot \frac{1 - (1+\beta)\frac{Z_E}{Z_F}}{1 + (1+\beta)\frac{Z_C}{Z_F}} \tag{2.37}$$

$$Z_{in,a} = 2\left[Z_{in} \parallel \left(\frac{Z_F}{A-1}\right)\right] \tag{2.38}$$

The following instead refer to the circuit (b),

$$A_b = -\frac{Z_C}{Z_E} \cdot \frac{1 - \beta\frac{Z_E}{Z_F}}{1 + \beta\frac{Z_C}{Z_F}} \tag{2.39}$$

$$Z_{in,b} = 2\left[Z_{in} \parallel \left(\frac{Z_F}{A-1}\right)\right] \tag{2.40}$$

In both cases, both the gain that the input impedance inversely dependent on the impedance of feedback. Input impedance is in any case limited by the value of Z_E. To

summarize, small Z_F involves high linearity, low gain and low input impedance. These results, supported by the circuit simulation, suggest to exclude the use of these topologies for the buffer.
Now is time to analyse the simplest of the three topologies. Circuit (c) shown in Figure 2.41(c) has the same structure used for the LNA buffer. Emitter follower stage has an high input impedance which is expressed by the Equation 2.32. Then differential input impedance of the buffer is

$$Z_{in,c}(s) = 2Z_{in}(s) \approx \beta(s)Z_E \tag{2.41}$$

To note that Z_E depends on the load of the buffer, but this value is obviously higher then $100\,\Omega$, the characteristic load impedance. Also β as high value at low frequency, then the input impedance is very high.
The gain is

$$A_c = \frac{(1+\beta)\,Z_E}{(1+\beta)\,Z_E + Z_\pi} \approx 1 \tag{2.42}$$

Looks like a good buffer, but it has two problems:

- too low output impedance;
- possible instability of the stage.

Low impedance it's a problem for matching. This problem has been solved introducing as in the LNA the two resistors R_O. As already explained in section 2.1.4 this means an attenuation of the gain, that is comparable with the one of the other two buffer versions if return loss is close to the minimum of 10 dB (-4 dB with $R_O = 30\,\Omega$). The only way to see if the stability can be a problem is to check the buffer in all conditions and, at the end of the design, to check stability of the complete system. The circuit has the same supply voltage of the mixer, 5 V, but has been also necessary to introduce capacitors between the blocks. This buffer as initially been inserted to replace the first stage of the PGA block. The programmable gain amplifier is DC coupled at the input, so this caps allows to set the output DC voltage of the buffer to provide the biasing to the next stage. After the decision to produce separate test-chips, these components have not been removed. It's even possible to remove them re-biasing the circuit to the output voltage of the mixer core (2.3 V). These capacitors have to be big enough to not limit the desired signal at the output. To afford the necessary performance to match the output of the mixer, by simulation it has been chosen a biasing current of 20 mA each branch. That means a total current consumption 42 mA, considering also the biasing circuit, and a total power consumption 210 mW.

Simulations

All the three configurations are simulated with a 300 Ω differential impedance source, close to the output impedance of the mixer, and a 100 Ω differential impedance load. Current consumption is 40 mA and supply voltage is 5 V. The simulation temperature is 27 ℃. Results are shown in Figure 2.42

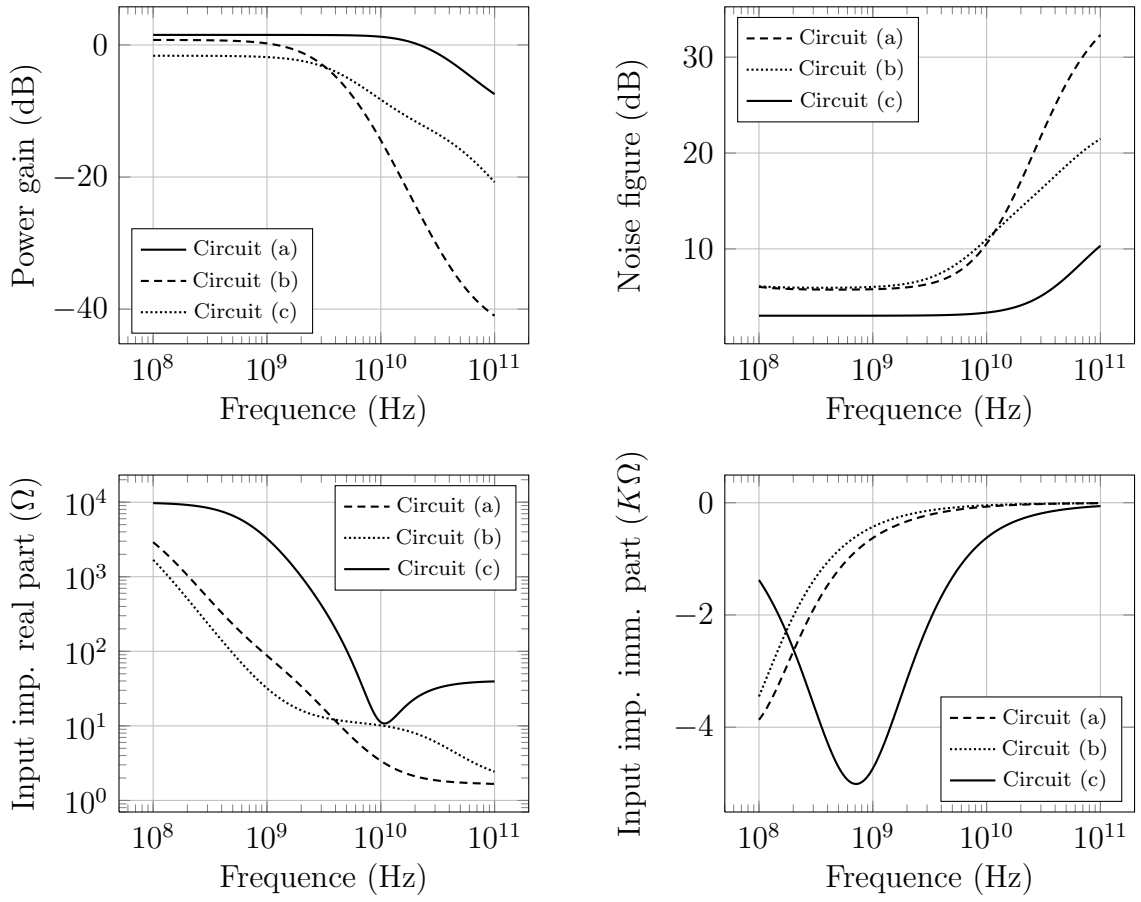


Figure 2.42: Power gain, noise figure and input impedance for each version for the buffer.

The different buffer configurations have been tested also using High Voltage transistors, because they have not the issue of the avalanche effect when V_{CE} exceed 1.5 V so they can afford higher linearity. Another advantage is the lower cut-off frequency, which is not a problem for the baseband, which reduces the risk of instability. Unfortunately this kind of transistor is much bigger then the High Speed considering the same biasing current. A big device means big parasitic capacitors which limits the input impedance and the band. It was therefore decided to discard this option due to the poor performance achieved in simulation.

2.2.3 LO driver

The original structure of this block is shown in Figure 2.43.

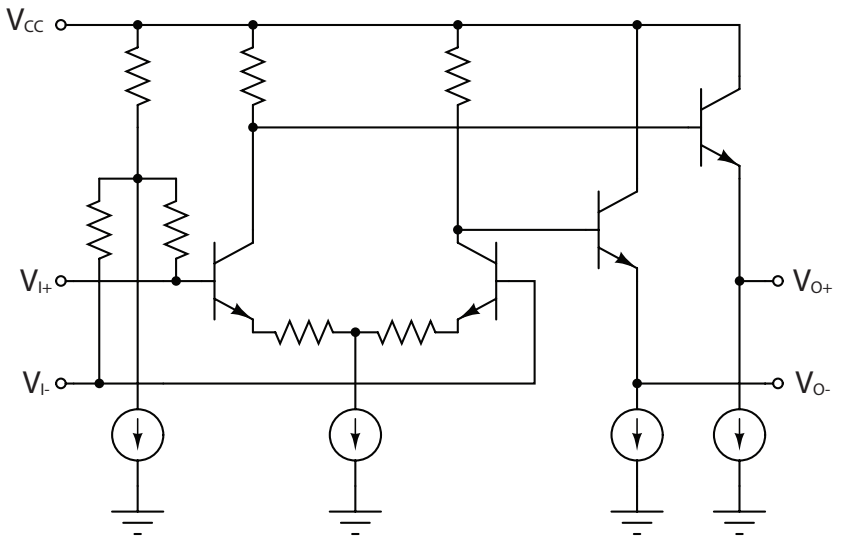


Figure 2.43: LO driver original scheme.

The first stage is composed by a differential pair with resistive degeneration, a circuit just analysed for the mixer buffer. Its task is to amplify the signal coming from the polyphase filter, reducing influence of the mixer switching stage on it. This means it has to show high input impedance. To note that in this case linearity is less important than in the buffer, so this structure looks to meet the requirements. A possible drawback is the high frequency of the signal treated, 10 GHz. As already seen the performance of this structure is strongly influenced by the parasitic components of the transistor. To keep the size of the active devices as small as possible helps to reduce this issue. Another way is too use an emitter follower stage as buffer before the amplification block. It increases also the input impedance at the cost of a higher power consumption.
Second stage is similar to mixer buffer. It has the function to drive big switching transistors without overcharging the previous stages. High biasing current and big transistors are here needed to provide enough power for the switching pairs. It's not necessary to repeat all the discussion, the formulas are the same used in Section 2.2.2.
Two different versions of the LO driver have been simulated,

- differential pair + EF buffer;
- EF buffer + differential pair + EF buffer.

To compare directly the two options, both have the same current consumption, 20 mA, and use same structure for the final EF buffer. As expected, the first circuit most influence the polyphase filter because of lower input impedance. The higher gain compensates the

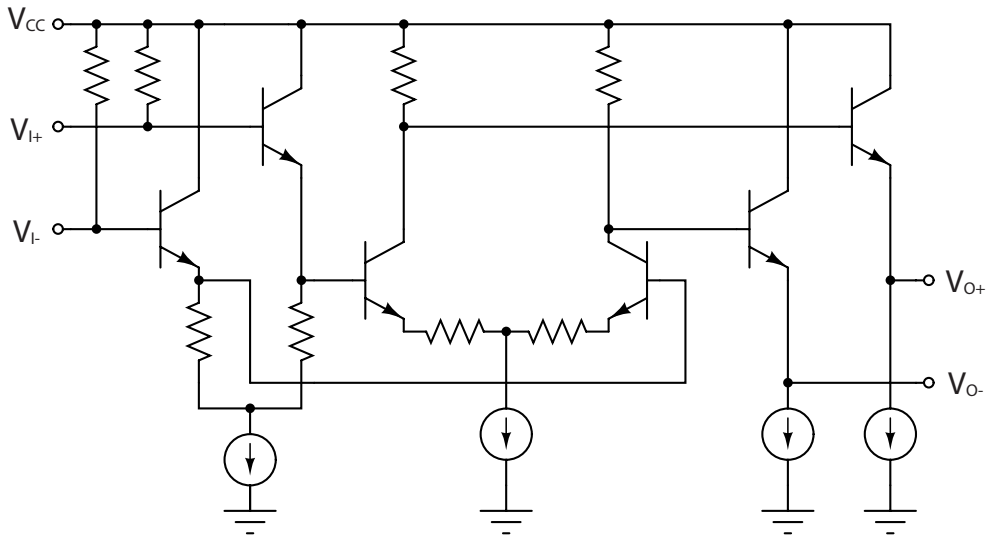


Figure 2.44: LO driver modified scheme.

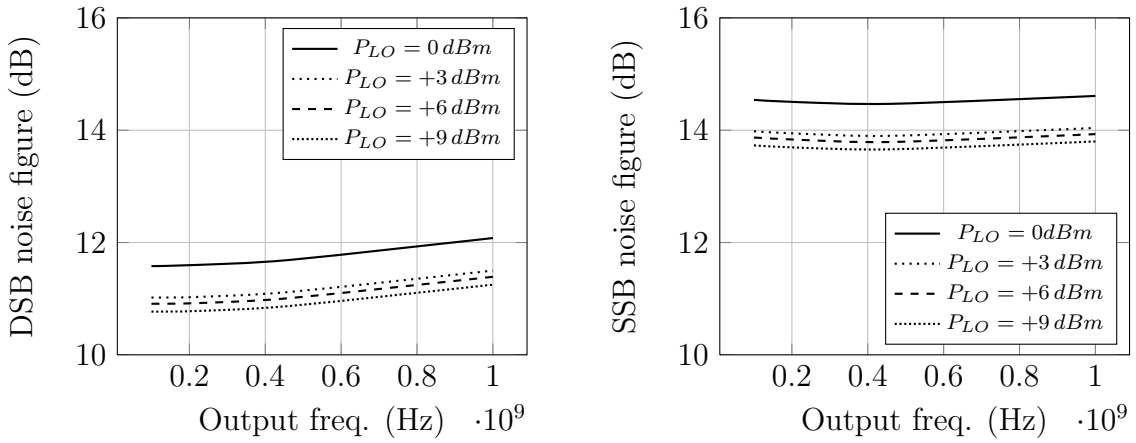


Figure 2.45: Noise figure according to the LO signal input power.

lost LO signal. Finally the second version obviously occupies a greater area in the layout of the circuit. Both the circuits have a current consumption of 21 mA ($\sim$ 70 mW). The amplitude of the sine signal has to be big enough to fast switch between the two transistor couples of the mixer switching stage. Steeper are the fronts of the pseudo square wave produced, the greater are the conversion gain and lower the noise figure. In contrast, if the amplitude of the Lo signal is too big it can produces unwanted peaks in the collector current of the switching pairs, as result of transistors parasitic components presence. These peaks reduce linearity of the system. The circuits have been designed to afford the possibility to drive the LO input with 0 dBm-signal. This is the minimum input power to reach good performance. Best results are available with an input power of +6 dBm (see Figure 2.52). Figure 2.45 shows how LO signal input power influence noise figure.

2.2.4 Polyphase filter

Original filter is replaced with a new one tuned to 10 GHz instead of 4 GHz. Furthermore it uses a 3 stages structure to reach an IMRR around 40 dB. To match a specific input source it is possible to inserts a resistor in parallel with the differential input. For a good return loss with a 100 Ω a resistor of 150-200 Ω is needed. In the final structure this component is not needed because of the presence of the transformer (see Section 2.2.6).

2.2.5 Degeneration coils

The only inductances to design in the mixer are the degeneration ones. The model used is the same the LNA's ones: two crossed coils, to reduce the sensibility to temperature and wafer characteristics gradients. In this case it is necessary to be careful with the width of the paths used because of the higher currents present in the differential pairs of the two mixers. If for the CU4 layer the minimum width is enough big to support the current flow, it' necessary to enlarge all the vias and the paths traced in the other connection layers.
Two version of this component have been designed. The first as an inductive value close to 375 pH, in the range previously indicated, to afford a 10 dB SSB-NF. The second as an inductive value above 500 pH and has been designed to obtain a higher IIP3. Obviously, the noise figure is much higher and therefore not useful for the project. Interestingly, this component, using overlapping windings and the same area of the first version, provides nearly twice the inductance with only one winding more. In the project will be used the first version.

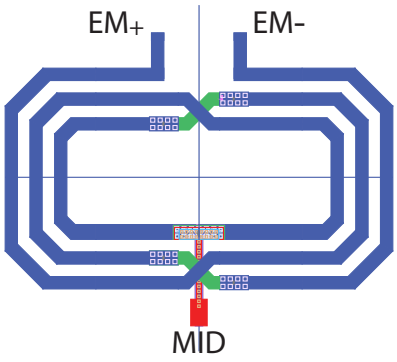


Figure 2.46: Layout of degeneration coils.

2.2.6 Input transformers

Having decided to study the blocks separately, at the two inputs of the mixer are placed decoupling transformers to simplify the measurement. Structure of these components is shown below. They are different in size because of the different characteristic of the input

and of the return loss needed.

The bigger one, the transformer at the RF input, has to drive the differential inputs

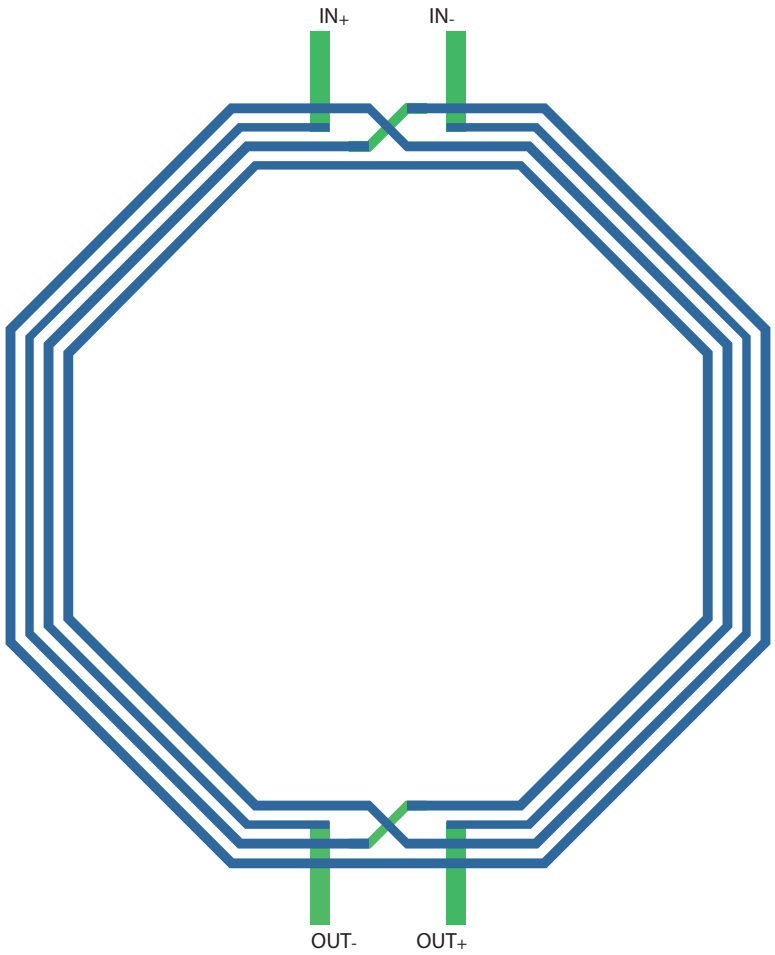


Figure 2.47: Layout of load inductances, second version with overlapped coils.

of the two mixers connected in parallel. A minimum return loss of 10 dB is required in the bandwidth $9 \div 11$ GHz. This means that the coils of the transformer have to be quite big to ensure a good inductance value. The simulation of a version of the transformer composed by discrete components, consisting of two inductors of equal value and quality factor comparable to the real case, coupling factor of 0.7, returns a value for primary and secondary coils of above 1.5 nH. LO-input transformer has also to achieve a good return loss but in a narrower band. It has been decided to use the same structure of the RF-transformer scaled to reduce the size of the component. Since these components are needed only for the test-chip they have not been optimized.

Both have to be tuned to 10 GHz. A cap is connected in parallel with the primary. The value of this component is the result of a parametric simulation to center the bell curve to this frequency. The real components will be considered for simulation only after the layout phase. For design simulations the system composed by two inductances coupled is used.

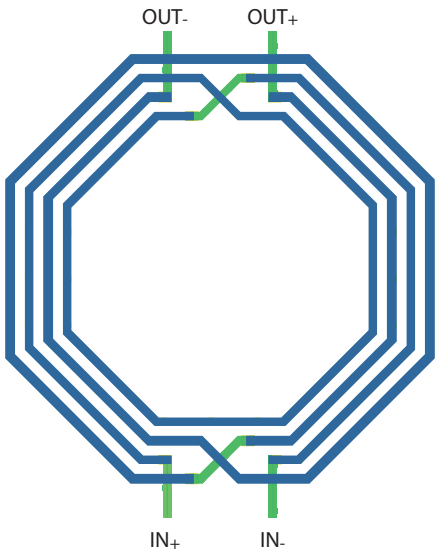


Figure 2.48: Layout of load inductances, second version with overlapped coils.

2.2.7 Design summary

Final structure of the mixer is presented in Figure 2.50. The circuit uses to different supply voltages, $V_{CC} = 5\,V$, to drive mixers and buffers, and $V_{CCA} = 3.3\,V$, to drive the LO-drivers. Two enable pins are present; EN_LO and EN_MX, to control, respectively, the 3.3 V and 5.0 V powered sections of the circuit. The section is enabled when the enable-pin is connected to the relative supply voltage.
The differential RF inputs of the two Gilbert double-balanced mixers are connected in parallel to share the RF signal coming from the tuned transformer. The other transformer is connected to the LO differential input and drives the polyphase filter directly. IN-quadrature differential signals at the output of the PPF control the inputs of the two LO-drivers. The internal structure of the Gilbert double-balanced mixer is shown in Figure 2.49. The total current consumption is of 46.9 mA for the 3.3 V section and

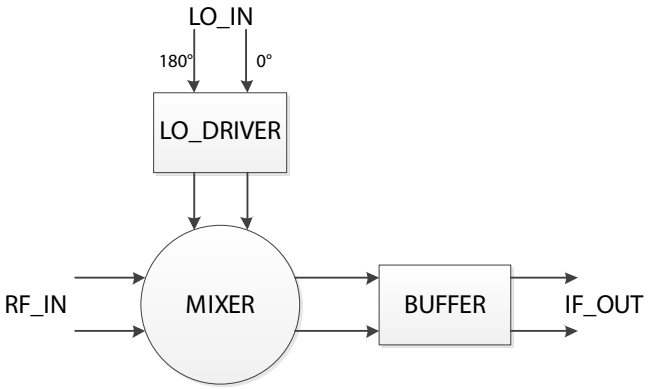


Figure 2.49: Gilbert double-balanced mixer complete block scheme with buffer and LO driver.

165.2 mA for the 5.0 V one.
Finally the outputs of the two mixer buffers return the baseband signal. Some capacitors are used to AC couple blocks. Most important are the capacitors between the LO-driver and the switching stage of the mixer. They are necessary because of the different supply voltages of the blocks. These components have to be big enough to not influence the signal. During next simulation a value of 20 pF is used. The same value is used to decouple the output of the mixer and input of the buffer.
The various parts of the mixer are design to achieve a good OIP3 keeping a DSB noise figure down the value of 10 dB. The same considerations made for LNA are valid. All the transistors are biased to return the best performance regarding linearity and gain. Also in this block are used High Speed transistor so in any situation V_{CE} has been set to be as close as possible to 1 V.
The results in the next Section refer to the circuit composed by:

- the Gilbert double-balanced mixer analysed in Section 2.2.1;
- the emitter follower buffer with $R_O = 30\,\Omega$;
- the 3-stage LO driver;
- the 3-stage 10 GHz-tuned polyphase filter;
- the two ideal transformers, composed by ideal inductance with resistive parasitic component and a coupling coefficient $k = 0.7$.

Considering the insertion loss of the transformers, the attenuation of the gain of 4 dB introduced by the buffer and considering input power is shared by two mixers instead of only one (-3 dB), the conversion gain measured considering the total input power and the output power of a single mixer is attenuate of about 10 dB. IIP3 increases of the same value, approximately. This means a gain above 6 dB and IIP3 close to 19 dB.

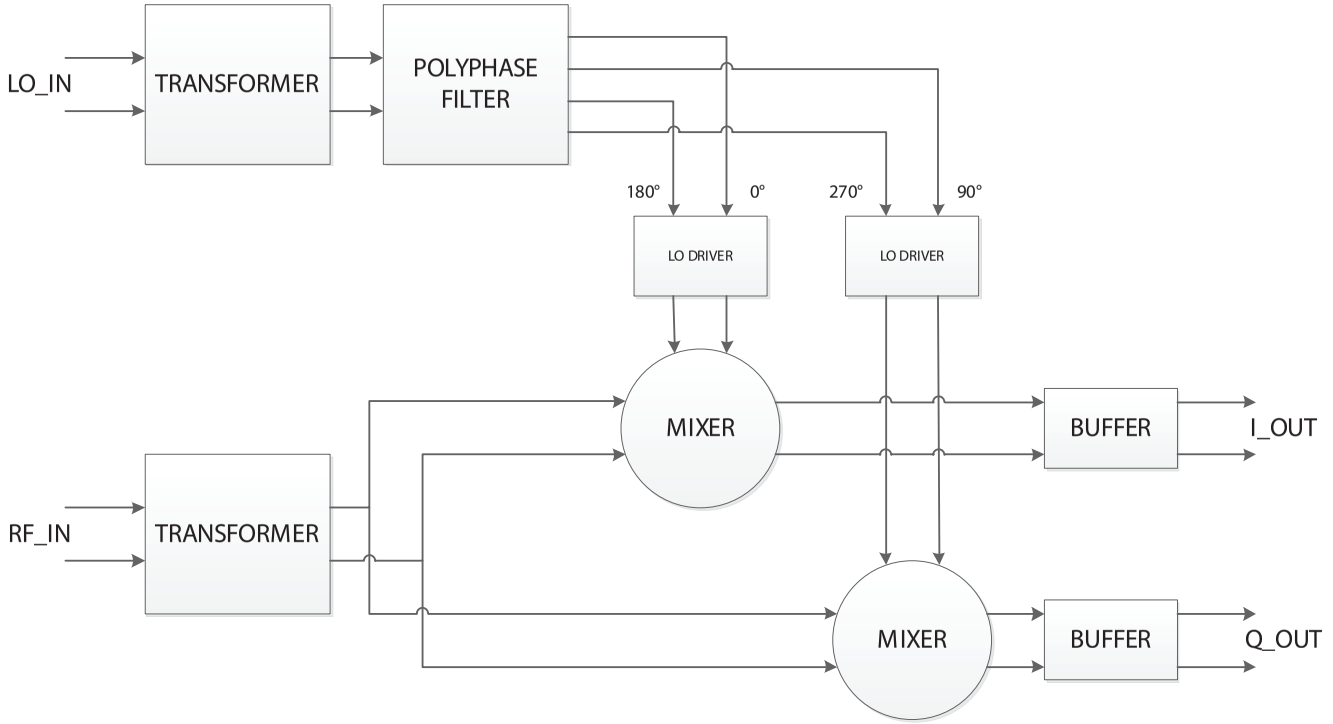


Figure 2.50: Quadrature mixer complete structure.

2.2.8 Design results

The circuit is tested using three 100 Ω PORTs, because two input are present, RF and LO, and an output. The simulations used in SPECTRE are:

- **DC analysis** to check DC biasing parameters.
- **SP analysis** to check S-paramters.
- **HB analysis** to check conversion gain, IIP3;
- **HBnoise analysis** to check SSB and DSB noise figures (RF-input signal disabled);
- **TRAN analysis** to check waveforms of the LO signals.

Tables summarize the results using two different values for the load capacitors of the mixer.

Output freq. MHz	**Conv. gain** dB	**IIP3** dBm	**SSB-NF** dB	f_{-1dB} MHz	f_{-3dB} MHz
250	6.97	18.31	∼13.5	∼400	∼ 800
500	6.03	18.81			
1000	3.28	20.60			

Table 2.13: Quadrature mixer results with $C_L = 1\,pF$ (T = 27℃, $V_{CCA} = 3.3\,\text{V}$, $V_{CC} = 5.0\,\text{V}$, P_{RF} = -40 dBm, $P_{LO} = 0\,\text{dBm}$).

Output freq. MHz	**Conv. gain** dB	**IIP3** dBm	**SSB-NF** dB	f_{-1dB} MHz	f_{-3dB} MHz
250	7.13	18.30	∼13.4	∼550	> 1000
500	6.56	18.65			
1000	4.74	20.40			

Table 2.14: Quadrature mixer results with $C_L = 0,5\,pF$ (T = 27℃, $V_{CCA} = 3.3\,\text{V}$, $V_{CC} = 5.0\,\text{V}$, P_{RF} = -40 dBm, $P_{LO} = 0\,\text{dBm}$).

RF-input and LO-input return loss

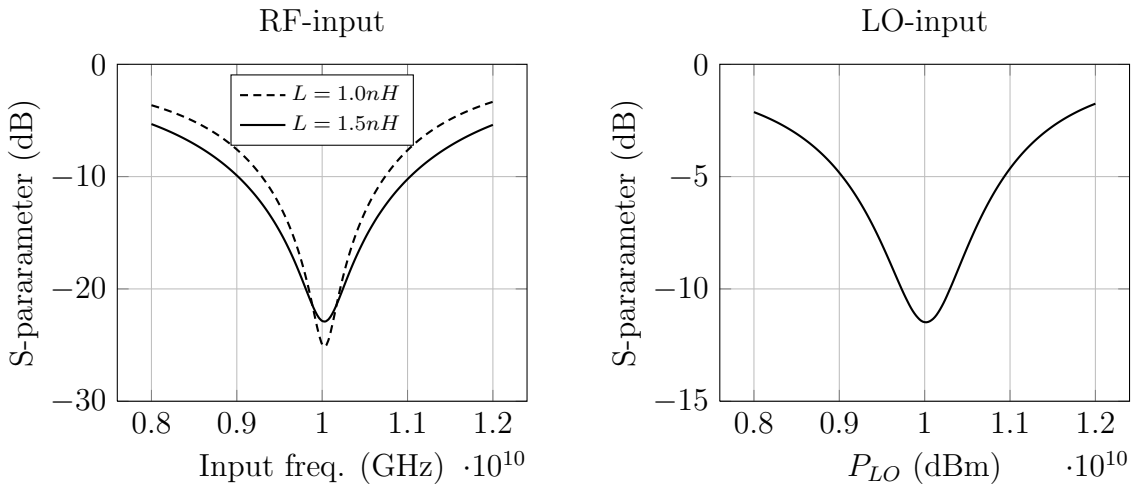


Figure 2.51: RF-input and LO-input S-parameters versus input frequency.

Two different choice was tested for C_L and the size of RF-input transformer inductors. Best results are achieved using, respectively, 500 fF and 1.5 nH instead of initially used 1 pF and 1 nH. The rest of the results shown below refer to the enhanced results version of the system.

Conversion gain versus LO signal power

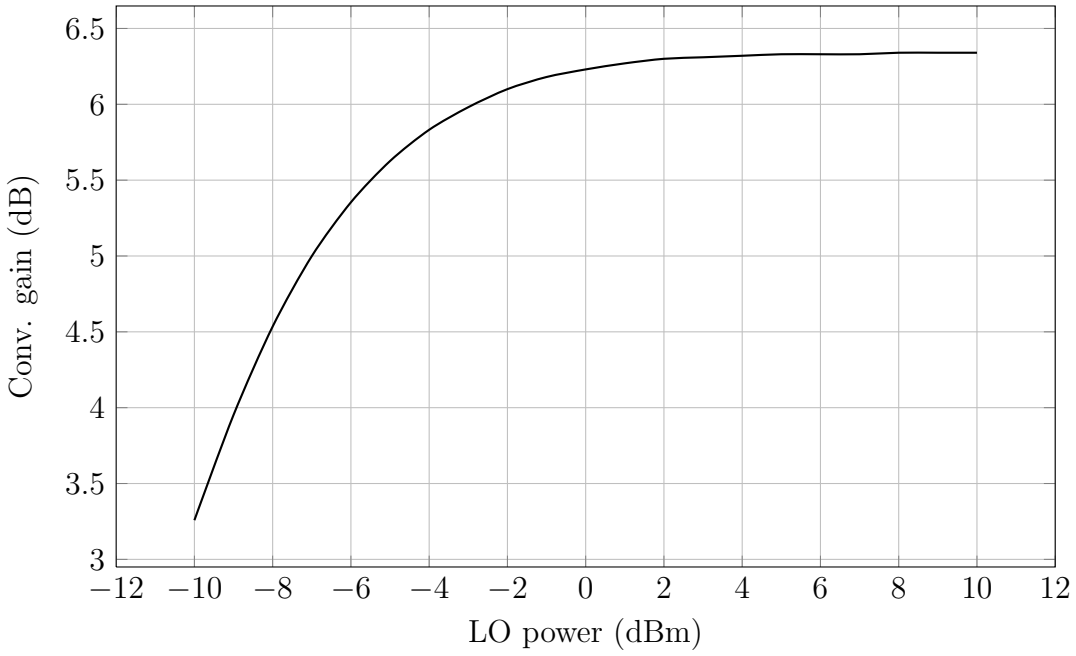


Figure 2.52: Conversion gain versus LO-input power (T = 27℃, V_{CCA} = 3.3 V, V_{CC} = 5.0 V, P_{RF} = -40 dBm).

Conversion gain, input IP3 and noise figure

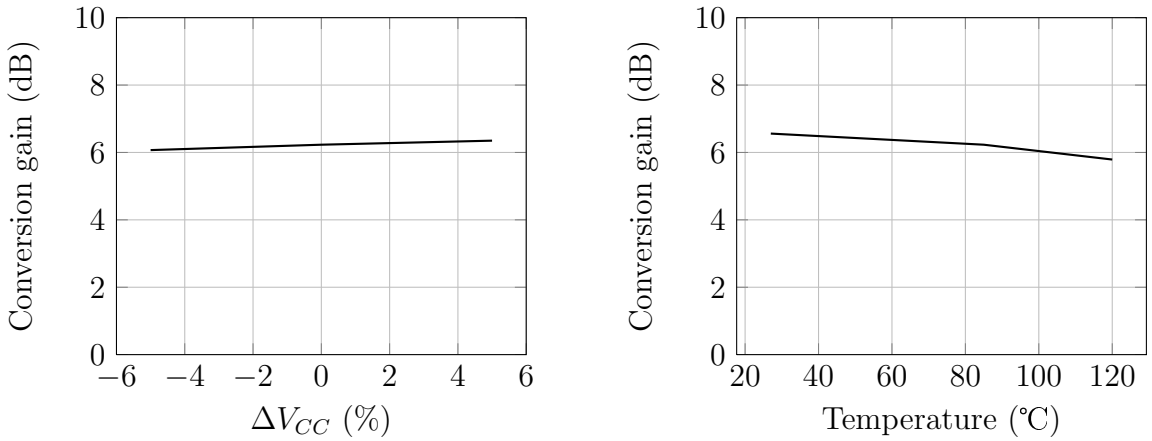


Figure 2.53: Conversion gain sensibility to supply voltage and temperature variations (respectively at $T = 85$°C and standard supply voltages).

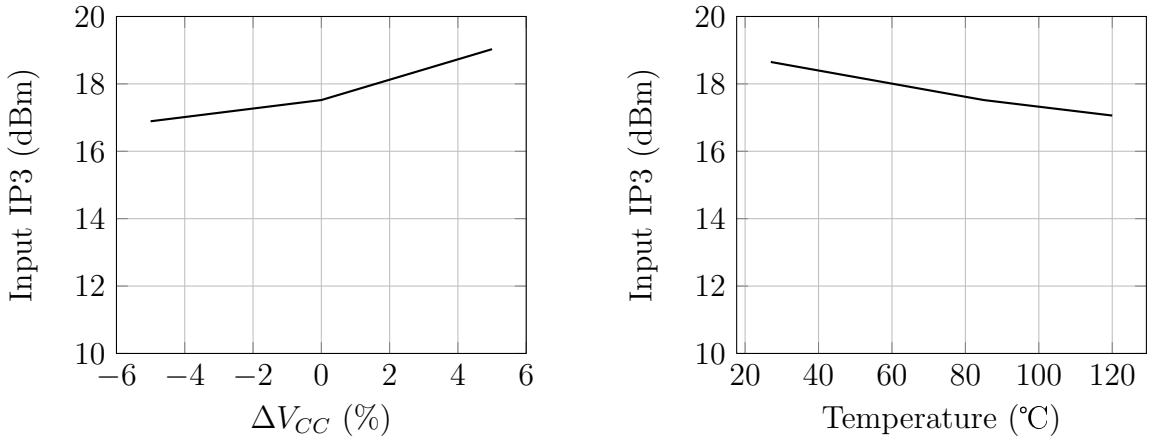


Figure 2.54: Input IP3 sensibility to supply voltage and temperature variations (respectively at $T = 85$°C and standard supply voltages).

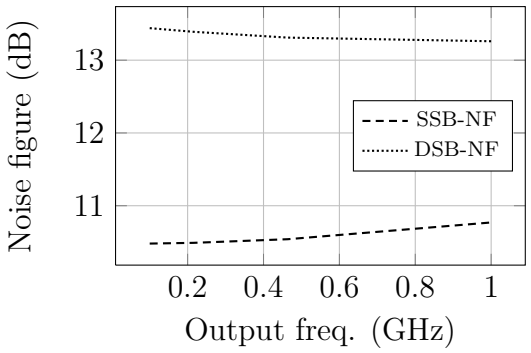


Figure 2.55: SSB and DSB noise figure according to output frequency.

Power consumption

Sup.	**-5%**	**0**	**-5%**
3.3 V	42.9 mA	46.8 mA	50.8 mA
5.0 V	149.3 mA	158.5 mA	167.7 mA

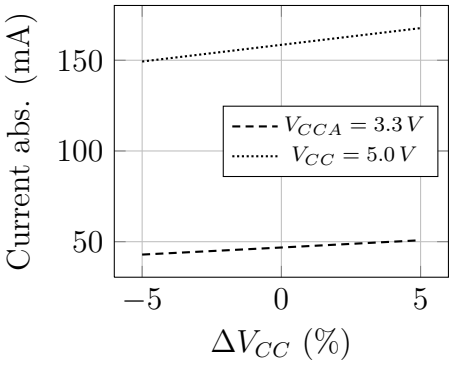


Figure 2.56: Current consumption sensibility to supply voltage variation.

Sup.	**27°C**	**85°C**	**120°C**
3.3 V	46.9 mA	46.8 mA	46.7 mA
5.0 V	165.2 mA	158.5 mA	151.5 mA

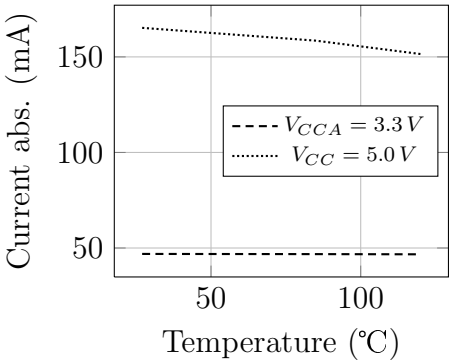


Figure 2.57: Current consumption sensibility to temperature variation.

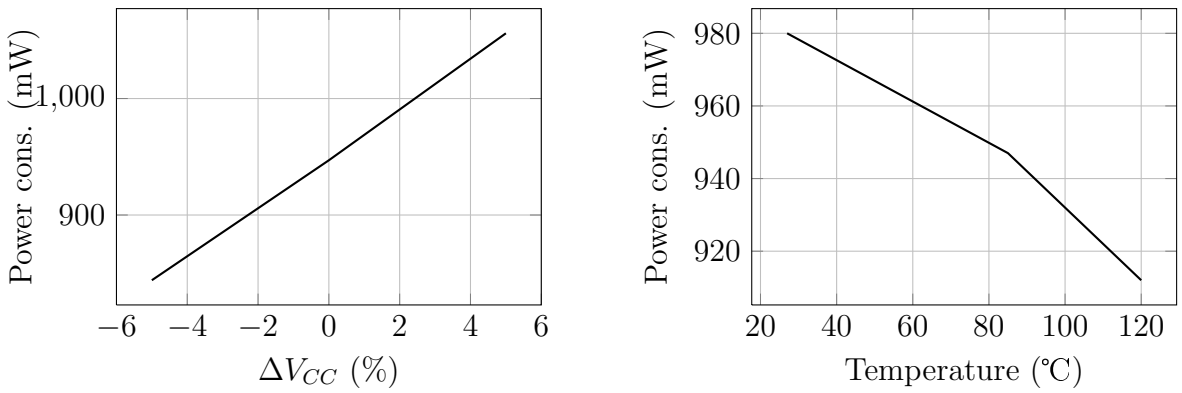


Figure 2.58: Power consumption sensibility to supply voltage and temperature variation.

2.2.9 Stability

Stability check uses an SP analysis in the range 100 MHz ÷ 100 GHz. Temperature is set at -40℃ and supply voltages at 3.6 V and 6 V, the worst case for stability. As source and load two PORTs are used in series with a big cap to not influence the biasing of the circuit. Their impedance is 100 Ω in case of differential input/output or 50 Ω in the other cases. To check the stability of the mixer is not easy because of the presence of three ports and its non-linear behaviour. The check has been done considering two ports at a time. The third port has been connected differently depending on the situation. Here are reported the cases:

- RF-port is connected to ground trough two big capacitors to not influence biasing point;
- LO-port is connected in two different ways, to check the mixer with both the switching pairs working, that happen when the LO differential sine signal has a value of 0V, and to check it with only one switching pair on, that happen when the LO signal has the maximum amplitude;
- IF-port is left open.

Different configurations are checked for each ports couple:

- differential input to differential output;
- singular input to in-phase output;
- singular input to opposite-phase output;
- two singular inputs with open circuit at the outputs;
- two singular outputs with open circuit at the inputs.

Only in the first case also the transformers are considered. In other cases they are removed to allow the simulations with single ended connections.
As seen in subsection 1.2.5, the stability is guaranteed for each type of source and load if the following conditions are verified at all the frequencies of the band analysed;

$$K, f > 1 \qquad b_{1,f} > 0 \tag{2.43}$$

Given the apparent increase of different configurations due to the complexity of the circuit are not reported all results as for the LNA. It's possible to summarize the work done saying that the circuit is stable in each condition.

2.3 Programmable gain amplifier

PGA has not been redesign like the previous blocks. It has been simulated in order to derive the characteristics of gain, noise figure, linearity and power consumption. Design choices will not be treated, not being questioned optimization of this circuit.

2.3.1 Block structure

The circuit is composed by the repetition of two blocks, an amplification stage and an AC-coupling circuit. All the blocks have a differential input and a differential output. The 2-blocks structure is repeated three times. Although the basic circuits are not perfectly identical, the structures used remain the same, which allows a generalized discussion of their functioning.
First block, here called PGA, generally presents three stages of signal amplification in parallel. Every stage has a different voltage gain value. Three signals are used to activate a singular stage at a time. Activation is made enabling or disabling biasing network of the stage.
Second block, here called AC3, acts as a buffer between the PGAs. It's necessary to afford AC coupling between PGAs, without reducing linearity and band.
Signal to enable PGA's stages is provided by a de-codification block. It converts the four input bits GS0-1-2-3 into 8 enable signals which directly control the biasing circuit of the stages.
Figure 2.59 shows the complete structure of the VGA18 circuit.
All buffer blocks are DC coupled so the input of the PGA has to be biased properly. The other buffers are biased by the output stage of each PGA.

2.3.2 Selection circuit: *vga_decoder4*

The circuit is a logical net that converts the input four bits in the signals to enable the stages. Transistors are used as electrical voltage controlled switches to set the voltage of the outputs to 0 V or V_{CC}.
The first value enables the stage, the second disable it.
GS4 directly controls PGA0 (see Table 2.15).

GS4	**PGA0 conf**	**ΔGain (dB)**
0	LG	+16
1	HG	+28

Table 2.15: PGA0 enabled stage according to GS4 bit configuration.

The other three bits are used to control PGA1 and PGA2 configuration. Table 2.16 shows the conversion.

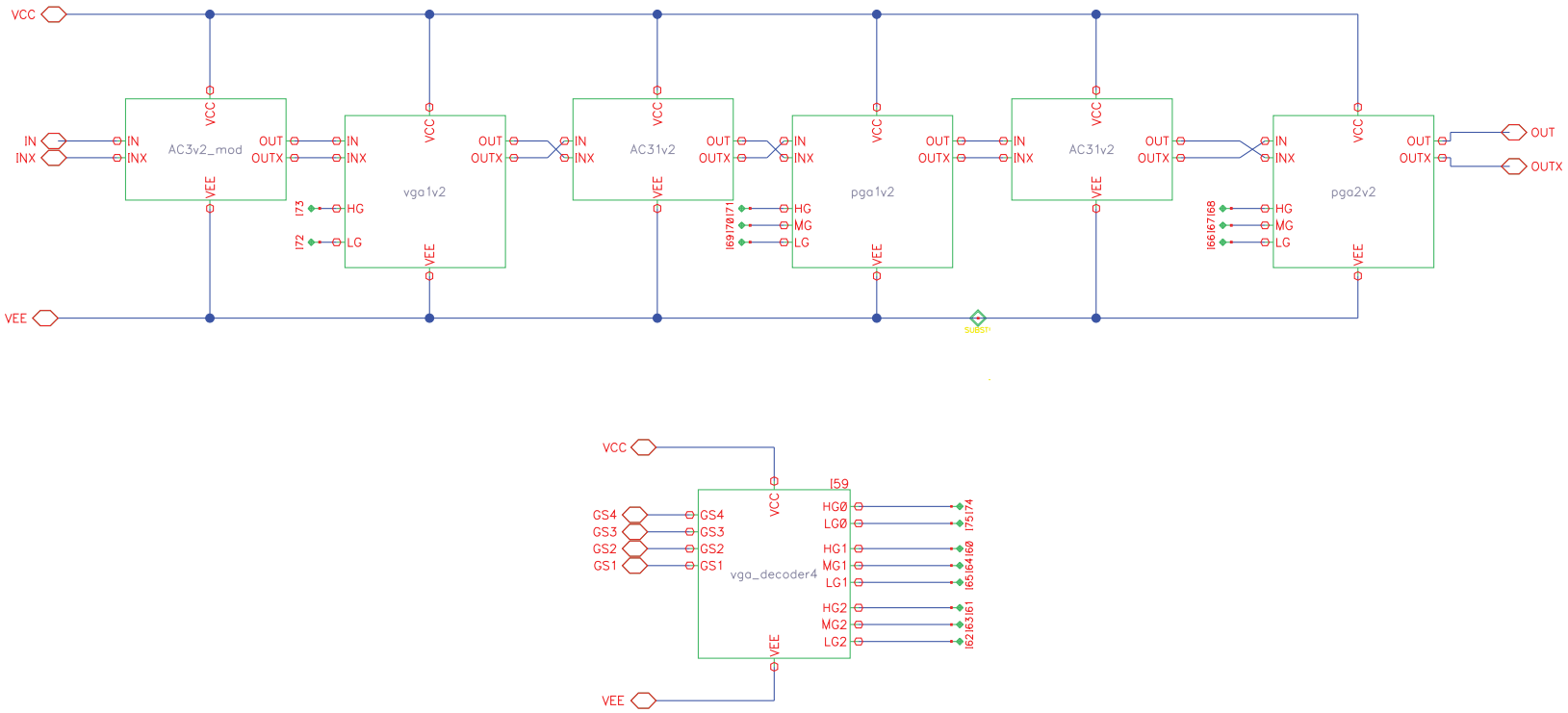


Figure 2.59: PGA block structure.

GS3	GS2	GS1	PGA1 conf.	PGA2 conf.	ΔGain (dB)
0	0	0	LG	MG	+0
0	0	1	LG	HG	+3
0	1	0	MG	LG	+6
0	1	1	MG	MG	+9
1	0	0	MG	HG	+12
1	0	1	HG	LG	+15
1	1	0	HG	MG	+18
1	1	1	HG	HG	+21

Table 2.16: PGAs' enabled stages according to GS3, GS2 and GS1 bit configuration.

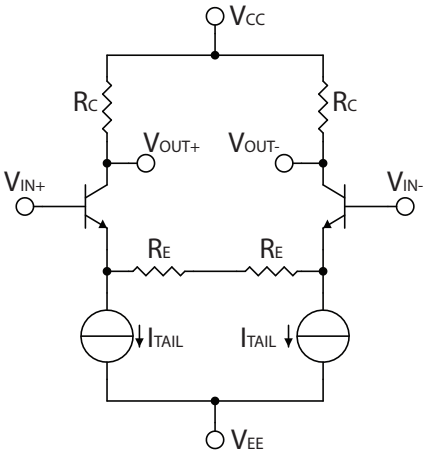
2.3.3 Amplification stage: *vga1v2*, *pga1v2*, *pga2v2*

The circuits will be called PGA0 (vga1v2), PGA1 (pga1v2) and PGA2 (pga2v2). They are slightly different but the base structure is the same:

- 2-3 amplification stages in parallel with different gain characteristic, differential input and output, sharing the same load;
- a biasing circuit for each stage, with the possibility to be enabled and disabled;
- two emitter followers as buffer for the differential output.

Basically between the circuits change the number of gain configurations and their gain.

Amplification stage Most important part to analyse is the single amplification stage topology. Voltage gain of the circuit is expressed by the following equation:



$$A_V = -\frac{\beta R_C}{r_\pi + (\beta + 1)R_E} \tag{2.44}$$

If the two conditions $r_\pi \ll (\beta + 1)R_E)$ and $\beta \gg 1$ are verified equation 2.44 becomes

$$A_V \approx -\frac{R_C}{R_E} \tag{2.45}$$

In first approximation, the gain of the stage only depends upon the values of resistors R_C and R_E. As already said the load (R_C) is shared by the stages, so the different gain values are fixed by the value of the R_E of each stage.

Emitter follower buffer

As in all the other circuit seen before, two emitter follower stages are used as buffer to reduce next-stage influence on the load of the amplification stage. The structure is exactly the same presents in mixer and LNA blocks.

2.3.4 Coupling circuit: *AC3v2*, *AC31v2*

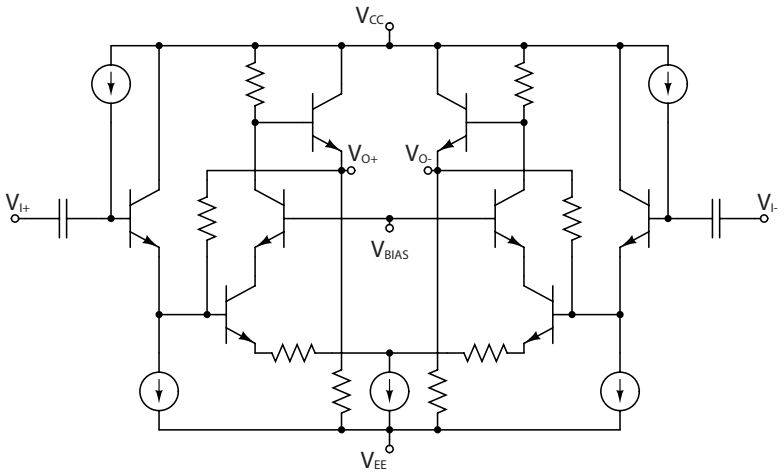


Figure 2.60: AC3v2 simplified structure.

The circuit has the task of DC decouple the PGA's stages because of the different biasing voltage. It's composed by a cap for DC decoupling, an emitter follower to not charge PGA's output stage and high linearity buffer that also provides the correct voltage for the next PGA's stage.

2.3.5 Results

The current absorbed by the circuit is quite the same for each configuration, 29.6 mA. So the power consumption is 98 mW. Band is different for each gain configuration. Only the -3 dB low pass cut frequencies for the most important configurations have been reported here. Presence of AC coupling stages introduces a high-pass filter and then the system

parameter	**unit**
LG0 - lowest gain	3.30
LG0 - highest gain	2.18
HG0 - lowest gain	2.38
HG0 - highest gain	1.70

Table 2.17: VGA18 low-pass cut frequency.

has a band-pass behaviour. The simulation band is 100 MHZ ÷ 100 GHz and the high-pass cut frequency is not visible, indicating it is at lower frequencies.
Below are reported the results obtained with regard to gain, linearity and noise figure. The circuit is simulated with a 3.3 V supply voltage, 100 Ω source and load, driving the gain selection pins with 0 V(to enable) or 3.3 V(to disable) voltage sources.

conf.	**cur. cons.**	**Power gain**	**Input IP3**	**Noise figure**
	mA	dB	dBm	dB
1	29.44	16.10	+0.13	21.01
2	29.49	19.09	-1.97	20.94
3	29.49	22.02	-5.85	19.49
4	29.54	25.01	-7.75	19.46
5	29.49	28.01	-10.31	19.45
6	29.54	30.94	-15.02	19.22
7	29.54	33.93	-16.87	19.21
8	29.59	36.93	-19.38	19.21

Table 2.18: PGA low-gain configuration results

conf.	**cur. cons.**	**Power gain**	**Input IP3**	**Noise figure**
	mA	dB	dBm	dB
1	29.49	28.07	-11.70	15.16
2	29.54	31.07	-13.88	15.14
3	29.55	34.00	-17.78	14.84
4	29.59	36.99	-19.71	14.83
5	29.54	39.99	-22.83	14.83
6	29.60	42.92	-27.05	14.79
7	29.59	45.91	-28.98	14.79
8	29.64	48.91	-31.68	14.79

Table 2.19: PGA high-gain configuration results

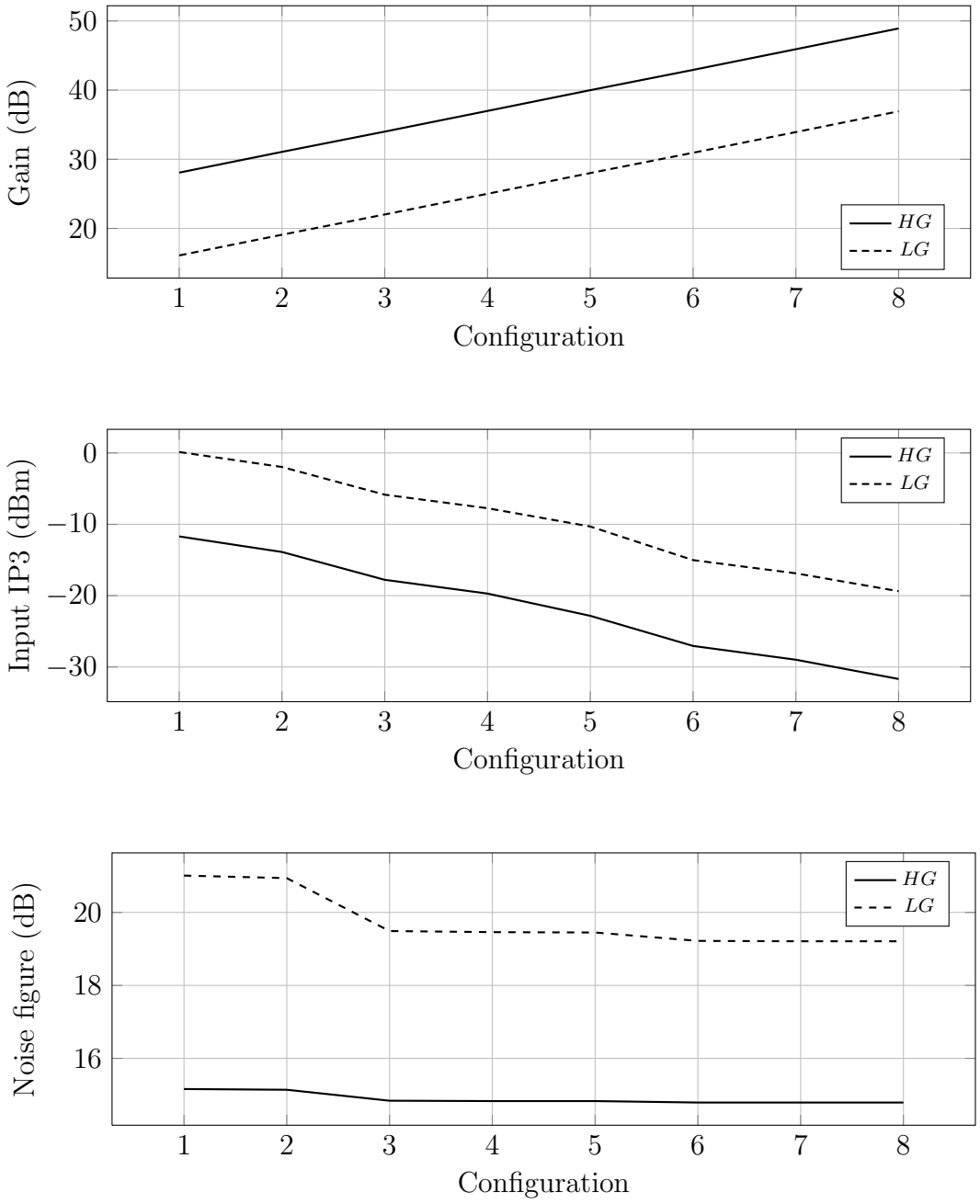


Figure 2.61: PGA gain, IIP3, noise figure at each bit configuration.

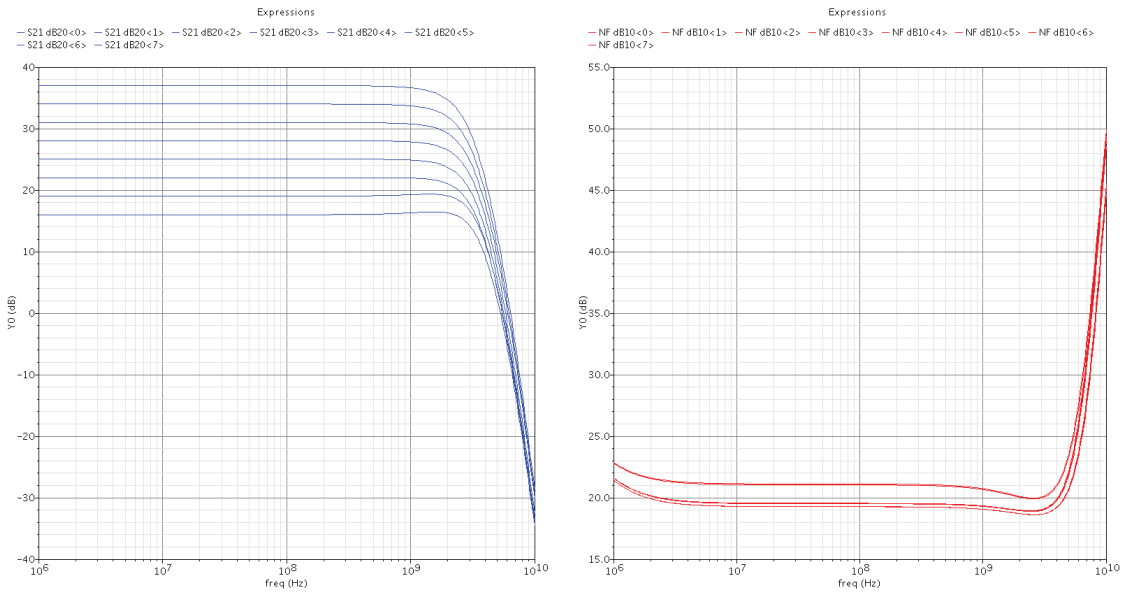


Figure 2.62: PGA LG0-enabled power gain and noise figure results.

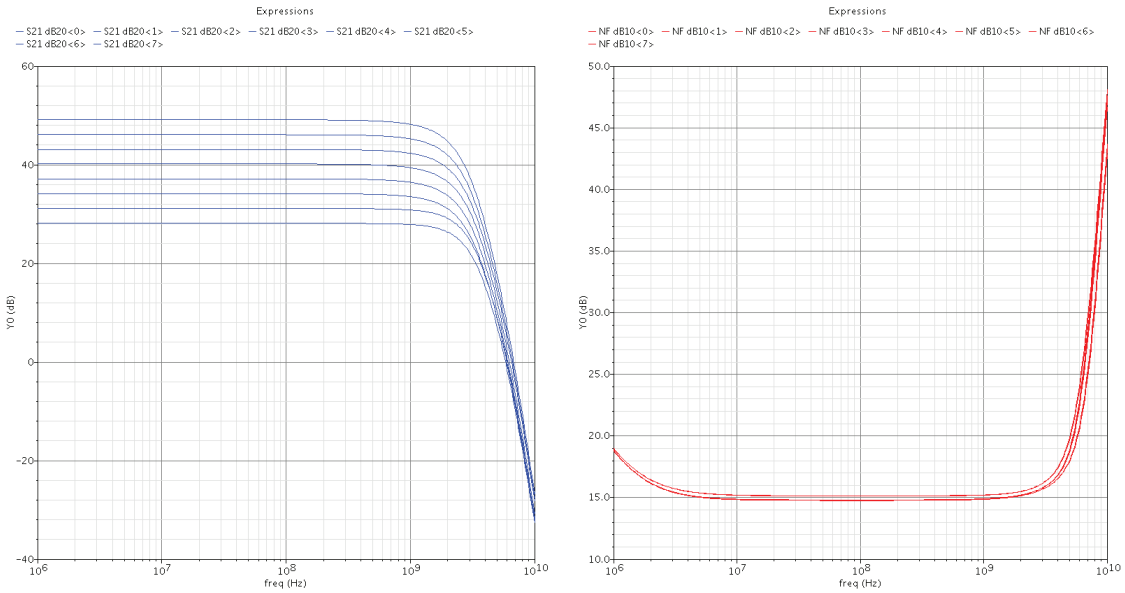


Figure 2.63: PGA HG0-enabled power gain and noise figure results.

2.4 Biasing circuit

Biasing circuit implements also enable circuit. Used structure is shown in Figure 2.64. It

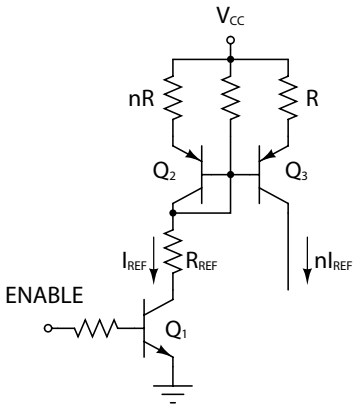
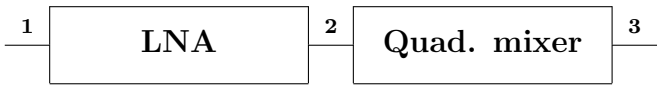


Figure 2.64: Biasing circuit structure.

provides a reference DC current to the circuit. This current depends basically only the value of R_{REF}. Usually this current is scaled, to reach wanted biasing current, through current mirrors that can be represented as DC current generators. In a differential pair or in a cascode stage transistors are directly used as generators of the biasing current inside the mirror. In this case it's necessary to introduce resistors of some KΩ in series to the point where them pick up the reference voltage of the mirror, in order to reduce the influence of the biasing circuit on the signal at the input of the transistor.

2.5 Cascoded stages

In this section are summarized the results of the combination of the three blocks using formulas indicated in Chapter 1. Table 2.5 reports results of LNA and quadrature mixer combination. Table 2.5 summarize results of the entire down-converter considering PGA

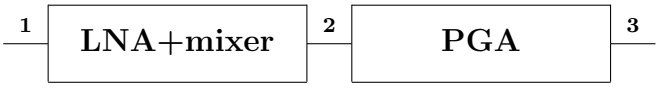


Stage parameters				
Gain (dB)		13.3		6.6
Noise figure (dB)		2.7		10.5
Input IP3 (dBm)		4.4		18.7

Cascoded parameters					**Total**
Gain (dB)		13.3		20.1	**20.1**
Noise figure (dB)		2.7		3.7	**3.7**
Input IP3 (dBm)		4.4		1.7	**1.7**

Table 2.20: LNA + quadrature mixer theoretical results ($T = 27$℃, typical supply voltages, $P_{RF} = -40\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$)

setted at the highest gain option.



Stage parameters				
Gain (dB)		20.1		48.9
Noise figure (dB)		3.7		14.8
Input IP3 (dBm)		1.7		-31.7

Cascoded parameters					**Target**
Gain (dB)		20.1		69.0	**70.0**
Noise figure (dB)		3.7		3.9	**3.5**
Input IP3 (dBm)		1.7		-51.8	**-**

Table 2.21: Downconverter theoretical results ($T = 27$℃, typical supply voltages, $P_{RF} = -40\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$)

Chapter 3

Layout

3.1 Low noise amplifier

The layout of the original LNA circuit is the starting point to develop this chip. Basically coils occupy the same area and have similar connections of the original ones.

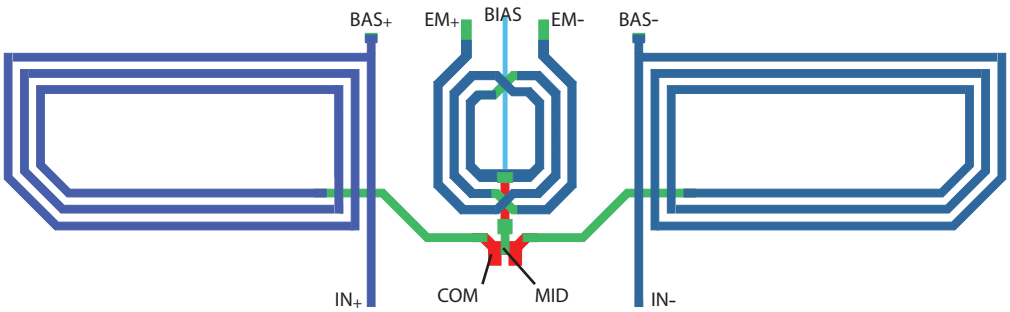


Figure 3.1: Final layout for matching and degeneration inductors.

Space between degeneration/matching coils and the load ones has been reorganized to introduce bigger transistors and the resistors of the low gain stage. TAN resistors are used in this case because of their precision and lower temperature sensibility. The drawback is the large area needed. It has been decided to put them orthogonally to the principal axis of the circuit to not increase RF paths length (see Figure 3.2).

The main difficulty encountered in the layout phase is represented by the introduction

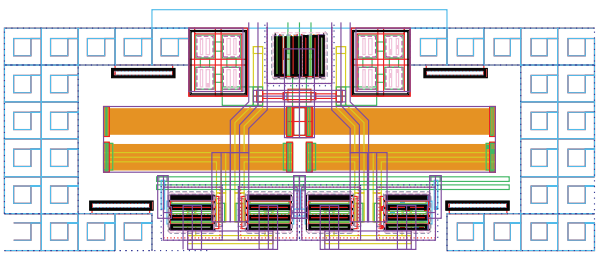


Figure 3.2: Gain selection circuit layout (TAN resistors are orange filled).

of ESD component on the line carrying the current for biasing the differential pair via the inductances of matching. This has prompted the redesign of the contacts of the component which contains these inductances and those of degeneration (see Figure 3.1). Output buffer has been redesign because of the increased biasing current. Structure is the same of the original, only resistors, caps and transformers have been enlarged to fit with the current requests (see Figure 3.3).

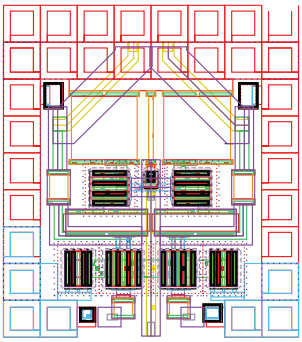


Figure 3.3: Output buffer layout.

Finally the two current mirrors to drive cascode stages have introduced in order to afford programmable gain (see Figure 3.4).

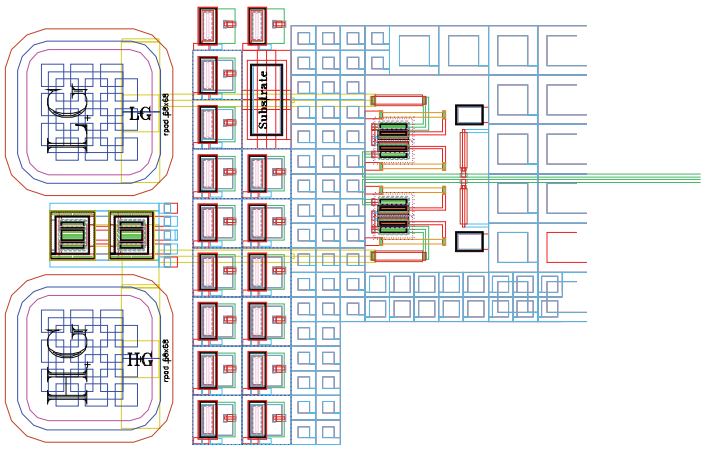


Figure 3.4: Gain selection enable circuit.

The complete layout is shown in Figure 3.5.

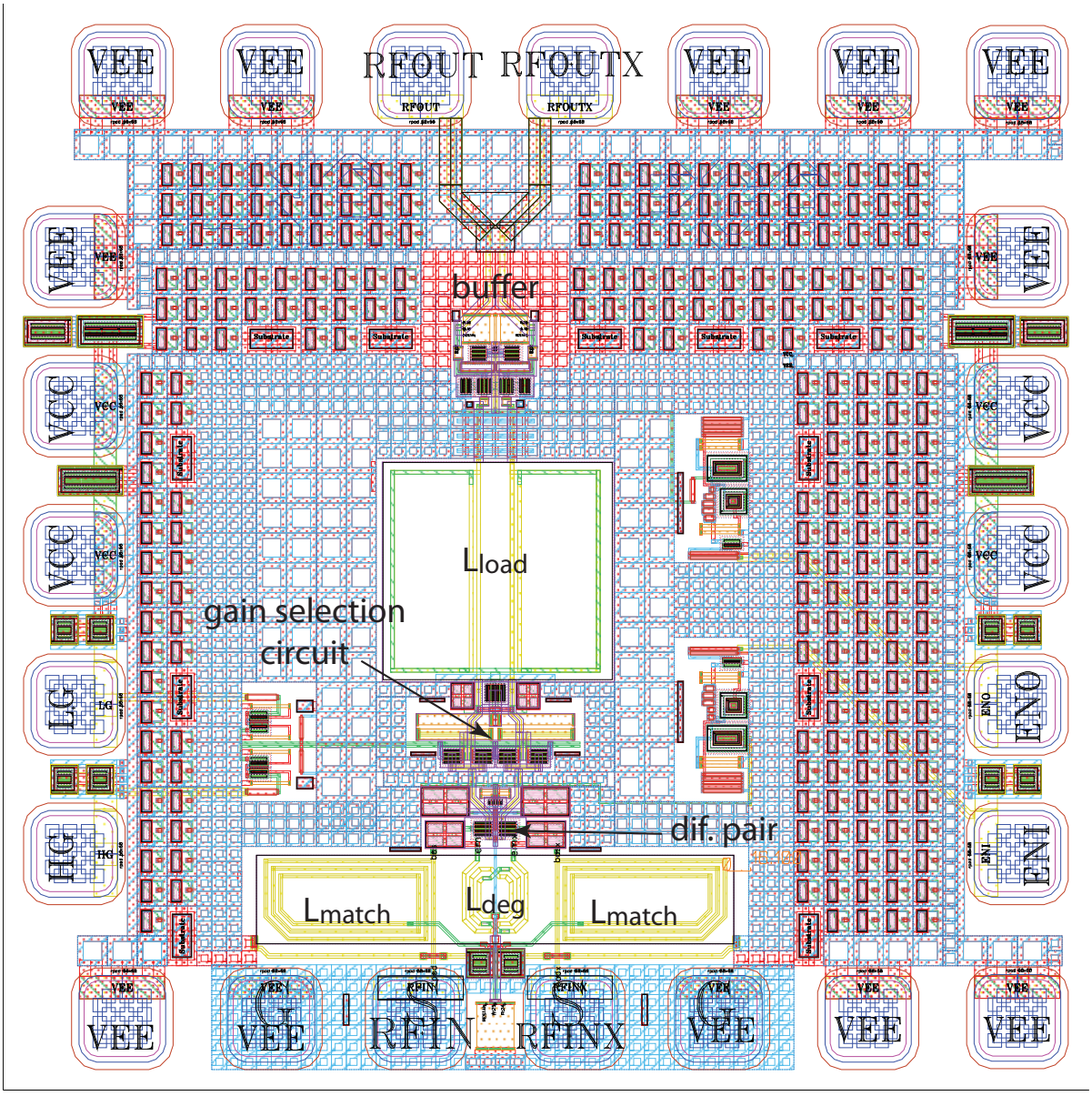


Figure 3.5: LNA chip layout.

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3.2 Quadrature mixer

Block layout design didn't start from a previous chip version as for the LNA. The parts to place are the following:

- the two Gilbert double-balanced mixers, connected in parallel at the RF-input;
- the LO-drivers to connect to the switching pairs of the mixers trough big capacitors because of the different supply voltage.
- the polyphase filter that gives the signal to the LO-divers.
- the output buffers of the mixers with AC-coupling capacitors;
- RF-input and LO-input transformers;

The first purpose is to reduce the length of the RF paths. Main axis of the chip divides the chip in the two sub-mixers I and Q. Layout is fully symmetric with respect to this axis.

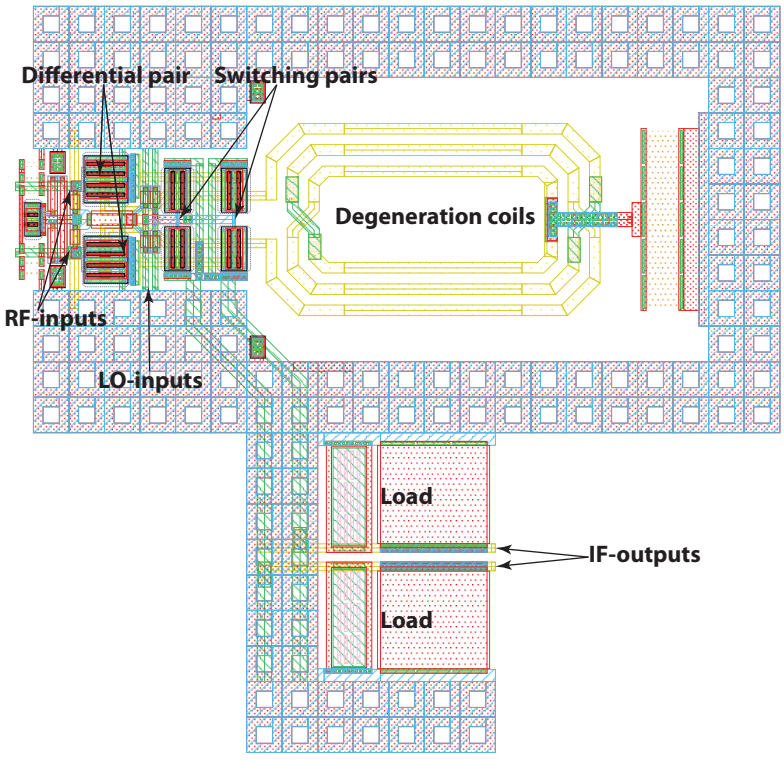


Figure 3.6: Gilbert double-balanced mixer layout

3.2.1 Gilbert double-balanced mixer

This block has been designed to connect together the RF-inputs of the two mixers reducing the length of paths. Also the LO-inputs are easily accessible. Both these inputs are close to the principal axis. To obtain this result the load and the degeneration inductances are moved closer to the pads, at the cost of longer connection paths. The signal managed by the load is at lower frequency (IF) so the length less influence the performance of the circuit. Degeneration inductors are partially redesigned turning the coils to reduce the height of the component. they have been also slightly reduced in size because of the high noise (10.4 dB) figure resulting from pre-layout simulations. The target, considering the +3 dB introduced by the RF-input transformer, is to achieve a maximum value of 7 dB (10 dB with the transformer).

3.2.2 LO-driver

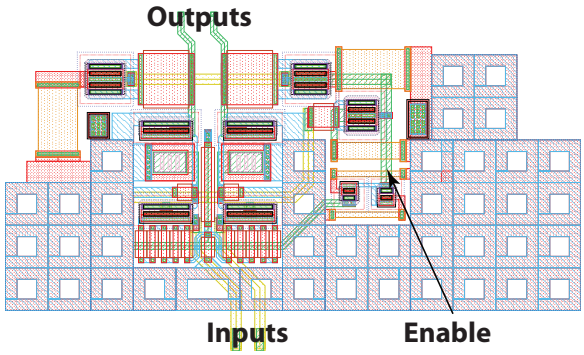


Figure 3.7: 2-stage LO-driver layout.

Initially in the layout of the block was present the 3-stage version of the circuit. It has been redesigned reducing the stage to original version ones, a differential pair and di EF buffer, to reduce the size of the component. The biasing circuit is designed to not increase the height of the circuit.

3.2.3 Output buffer

The buffer is connected at the output of the mixer. It is designed to keep the same height of the mixer load to obtain a rectangular form-factor, much easier to integrate in the final layout. Four connections path are provided to connect the AC-coupling capacitors will placed below this component. The output paths are on the opposite side with respect to the main axis to be directly connected with the chip pads.

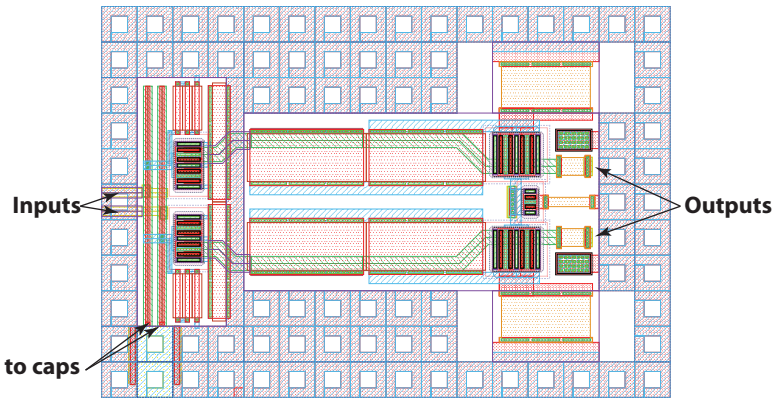


Figure 3.8: Mixer output buffer layout.

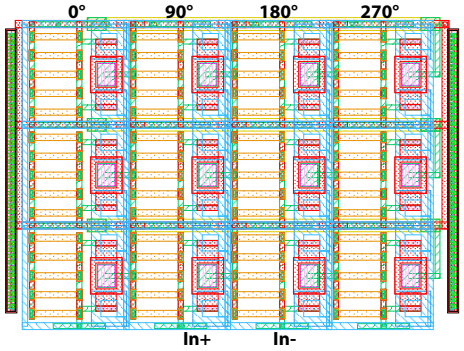


Figure 3.9: Polyphase filter original layout.

3.2.4 Polyphase filter

The original layout of this component has been slightly modified to adapt the contacts to the chip configuration.

3.2.5 Complete quadrature mixer chip layout

Coils, transformers and big capacitors are modified to fit the layout of the chip. Capacitors between LO-driver and mixer are smaller, 7 pF instead of 20 pF. This variation reduces a little the LO-signal at the input of the mixer, but it can be compensated increasing the incoming LO-signal power of some dB. Also the caps between mixer and buffer are smaller (17 pF). These components cannot be reduce too much because this affects the output band of the system. These caps are placed on the same line and have similar height to create an area that divides the chip in two parts. Upper part is the 5.0 V powered one, lower part contains the 3.3 V blocks. Four capacitors are now present between the polyphase filter outputs and the LO-drivers inputs. They reduce the low frequency disturbs coming from the mixer. This ensures to no introduce noise in the LO-signal that can affect other chips. Another advantage is the elimination of the DC component in the circuit of the filter. Finally transformers are adapted to the layout.

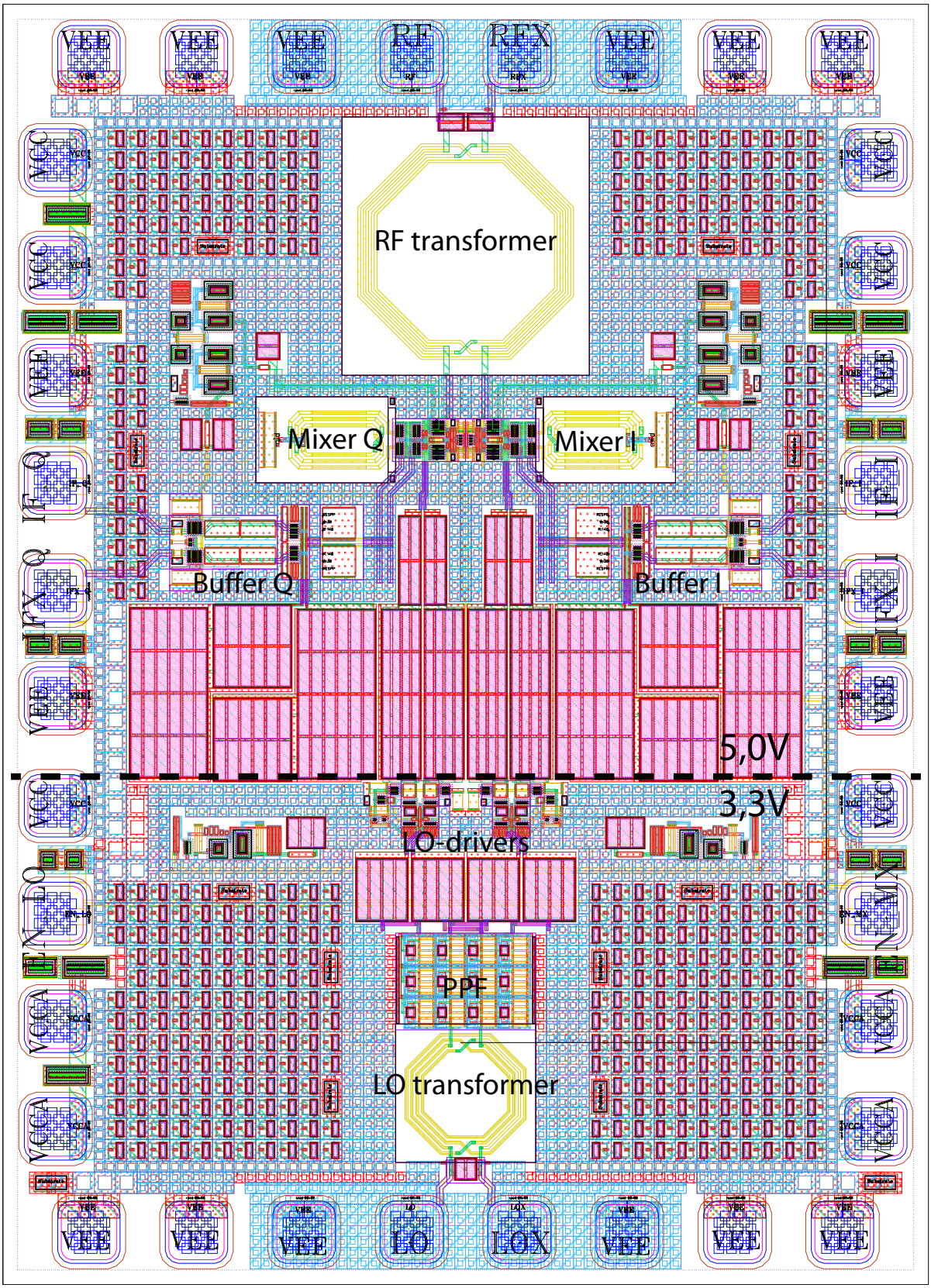


Figure 3.10: Quadrature mixer chip layout.

Chapter 4

Results

The chapter lists the results obtained by simulating the two blocks again considering parasitic components and the modifications made during the layout phase.
In the last section, after discussing the results of the individual blocks, are listed the main parameters obtained by combining LNA and quadrature mixer, comparing them with expected results.

4.1 Low noise amplifier

During the layout the circuit has been modified. Main changes are here summarized:

- Gain step between LG and HG configurations increased from 4 to 7 dB varying R_1 and R_2 values;
- Redesign of the input matching network inductors (L_B) to increase their value and enhance input return loss;
- Increased bias current from 10 mA to 12 mA in the output buffer, because of the insufficient linearity performance.

The circuit is simulated with the same configuration used during design phase. Monte Carlo simulation is added to test the sensitivity of the circuit to process spread and mismatches.
In these last simulations the currents used to drive gain selection circuit are different at each temperature to compensate resistors value variation and to keep the biasing point of cascode stages constant. Table 4.1 reports current values used during simulation.

	T = -40°C	**T = 27°C**	**T = 85°C**	**T = 120°C**
Enable current	0.55 mA	0.50 mA	0.43 mA	0.40 mA
Disable current	1.05 mA	1.00 mA	0.93 mA	0.90 mA

Table 4.1: HG and LG enabling/disabling currents.

4.1.1 Temperature and supply voltage sensibility

Simulation condition: $P_{RF} = -40\,dBm$.

Power gain

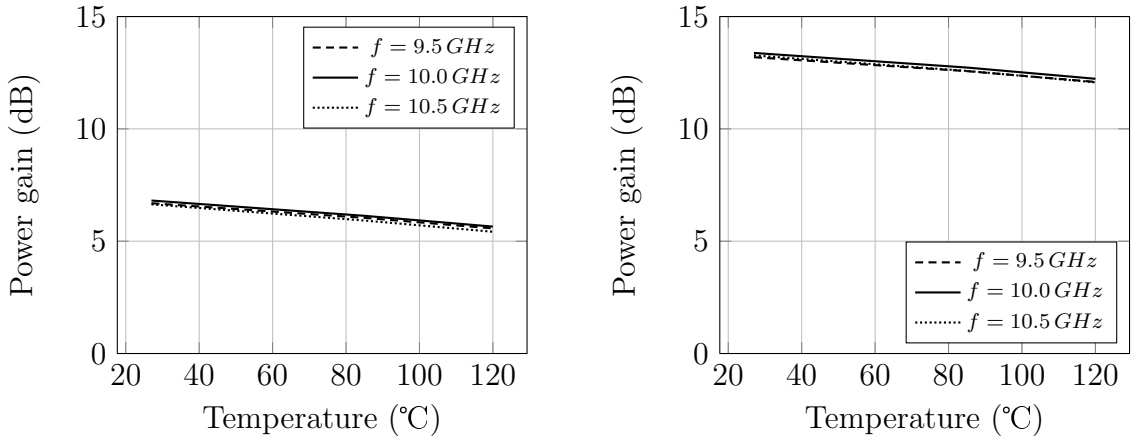


Figure 4.1: Power gain versus temperature ($V_{CC} = 3.3\,V$).

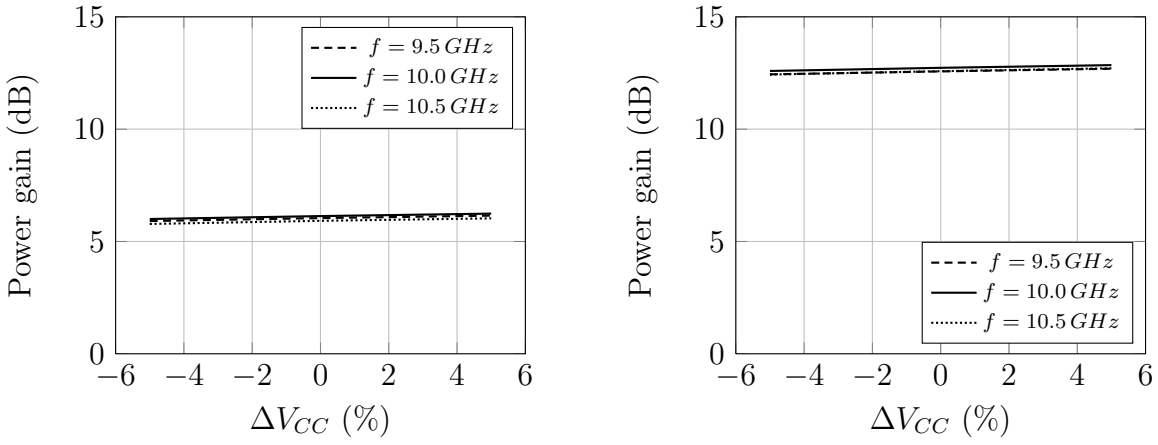


Figure 4.2: Power gain versus supply voltage variation (Temperature = 85℃).

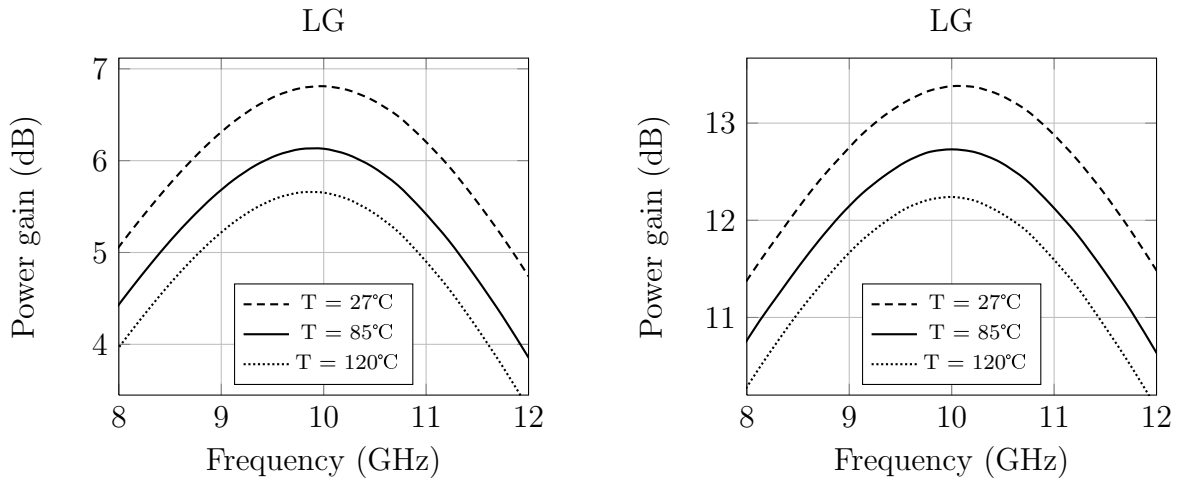


Figure 4.3: Power gain versus input frequency ($V_{CC} = 3.3\,V$).

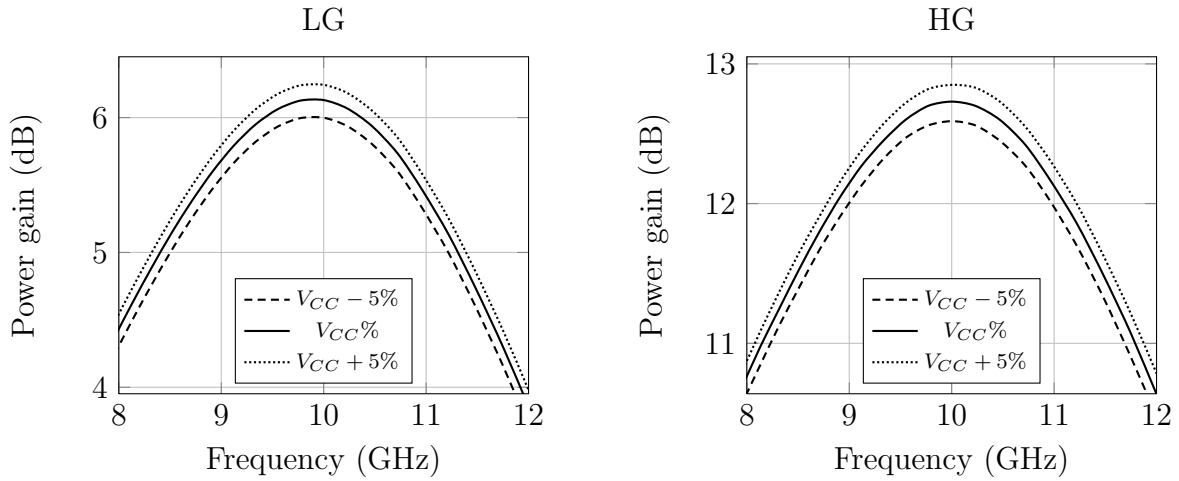


Figure 4.4: Power gain versus input frequency (T = 85℃).

Noise figure

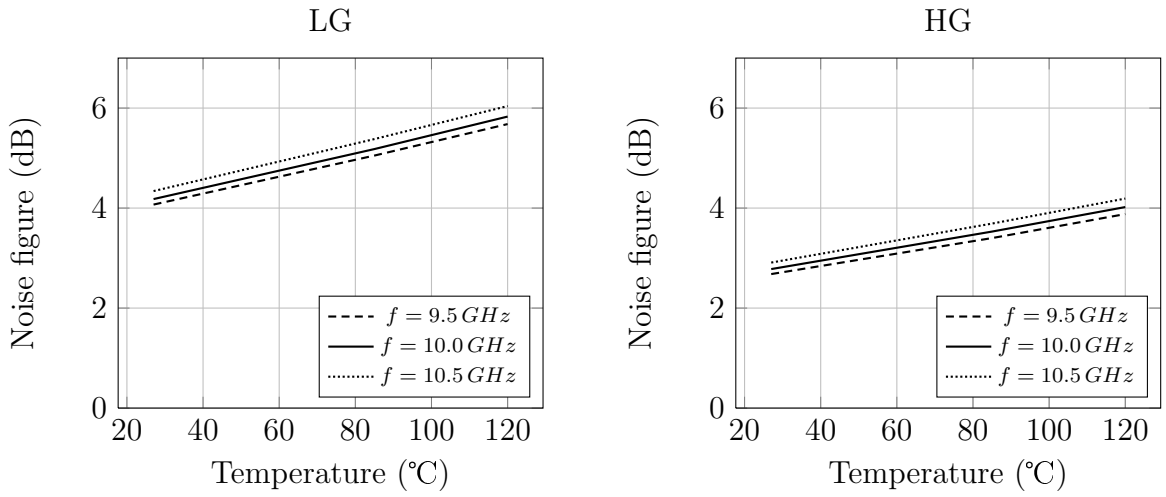


Figure 4.5: Noise figure versus temperature ($V_{CC} = 3.3\,V$).

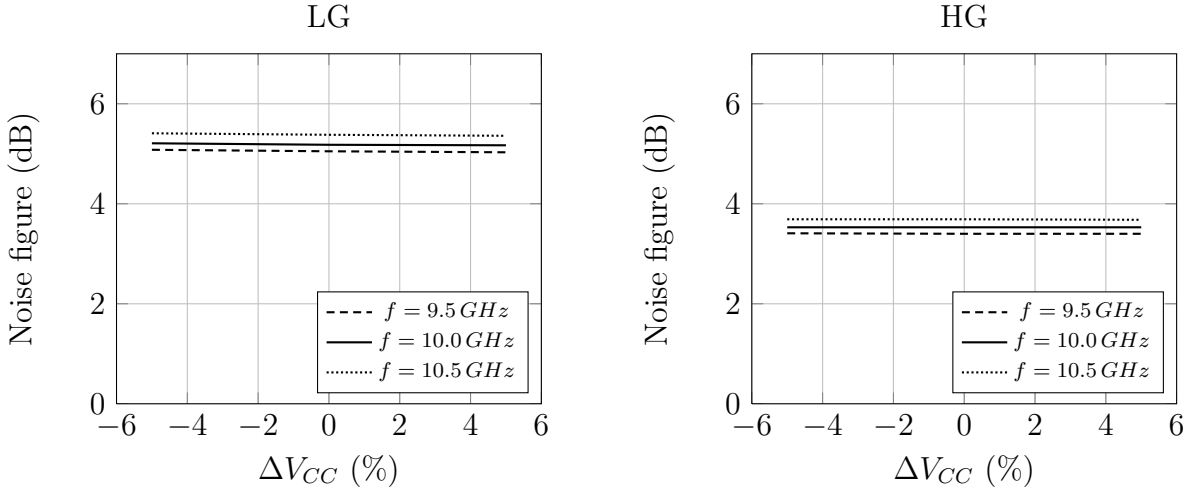


Figure 4.6: Noise figure versus supply voltage variation (Temperature = 85°C).

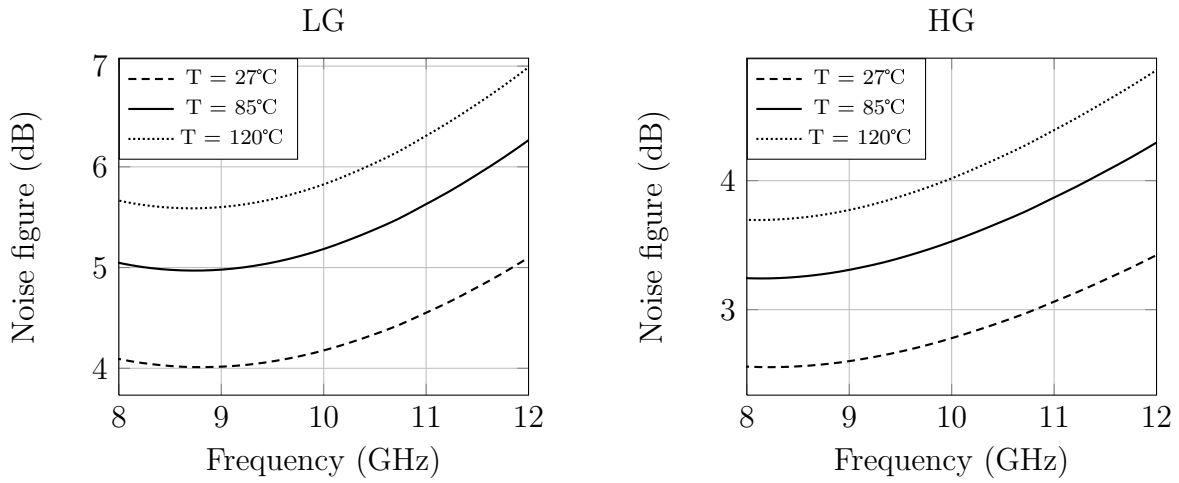


Figure 4.7: Noise figure versus input frequency ($V_{CC} = 3.3\,V$).

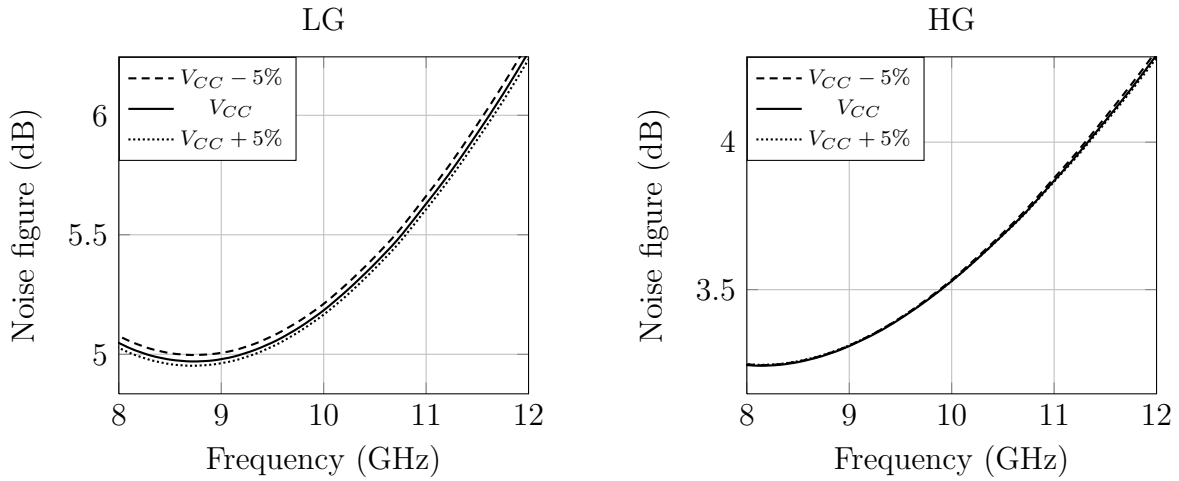


Figure 4.8: Noise figure versus input frequency (T = 85℃).

Input IP3

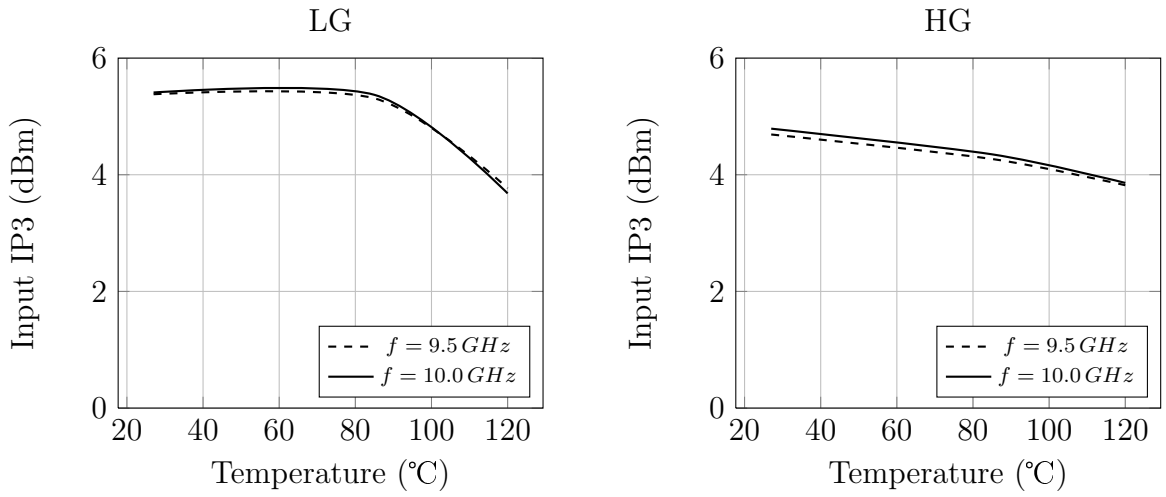


Figure 4.9: Input IP3 versus temperature ($V_{CC} = 3.3\,V$).

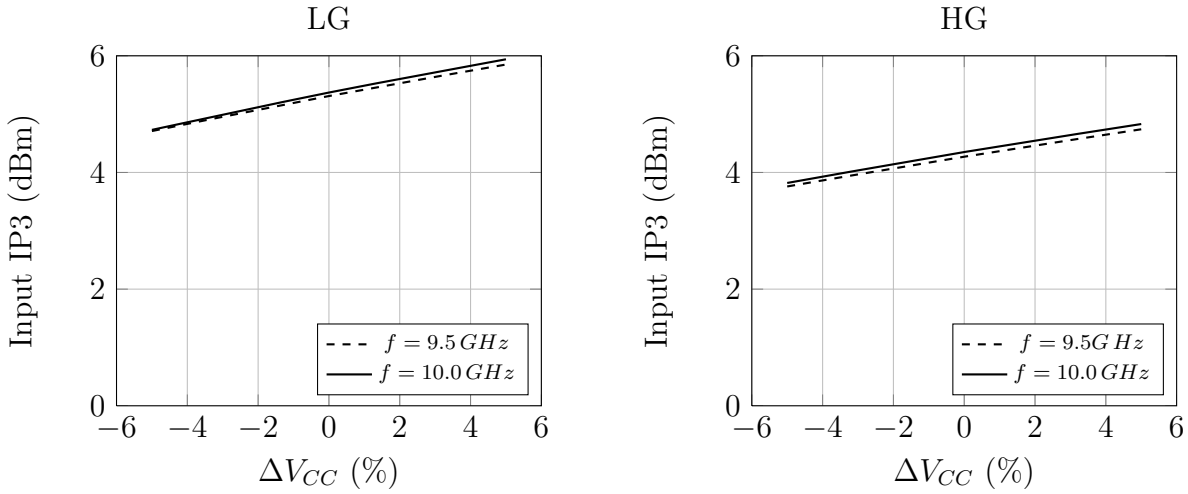


Figure 4.10: Input IP3 versus supply voltage variation (Temperature = 85℃).

Input return loss

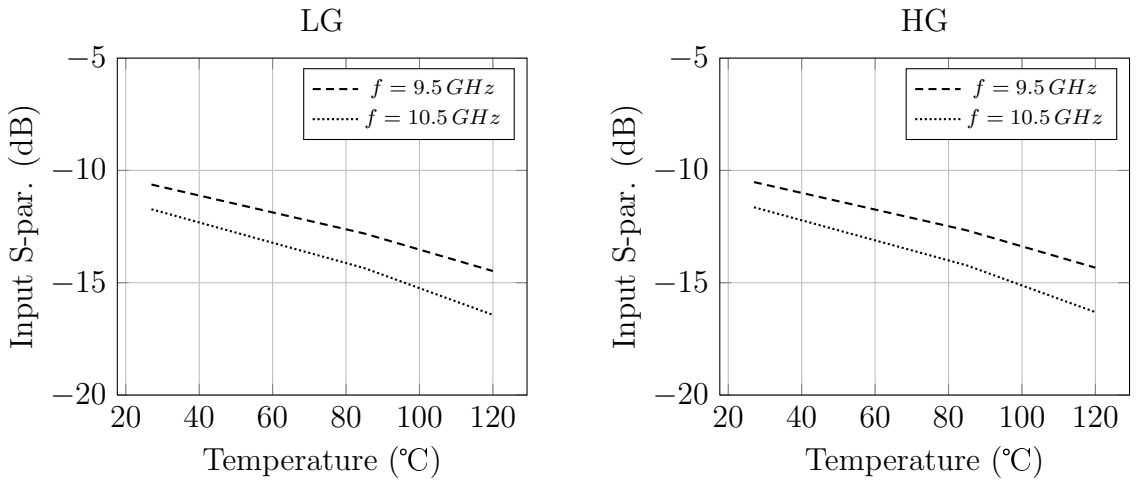


Figure 4.11: Input S-parameter versus temperature ($V_{CC} = 3.3\,V$).

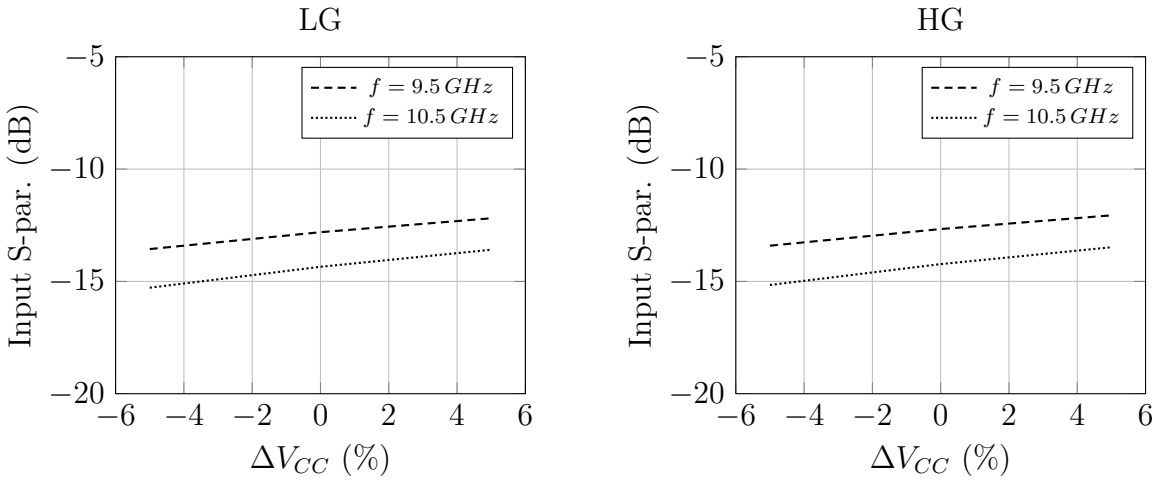


Figure 4.12: Input S-parameter versus supply voltage variation (Temperature = 85℃).

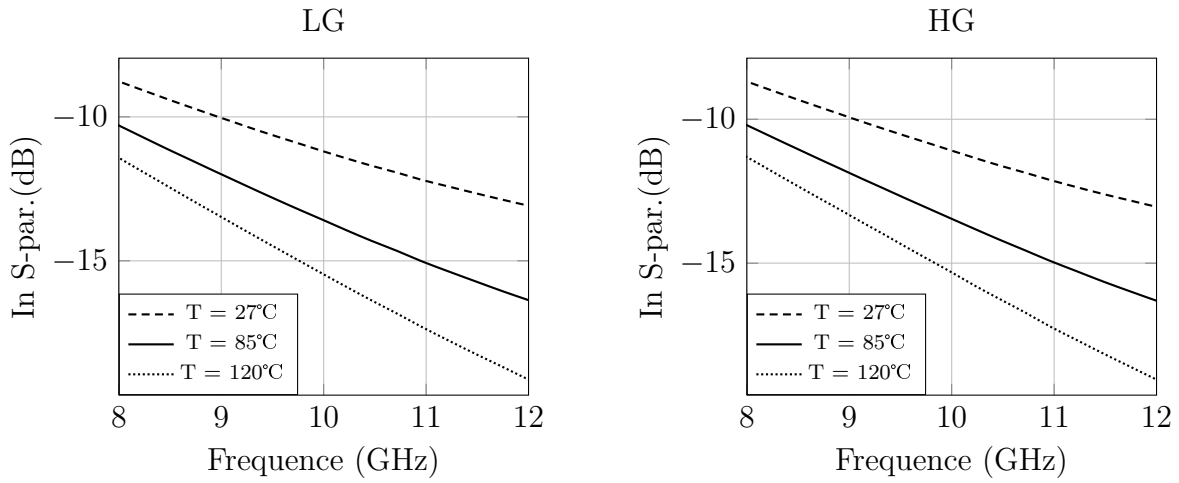


Figure 4.13: Input S-parameter versus input frequency ($V_{CC} = 3.3\,V$).

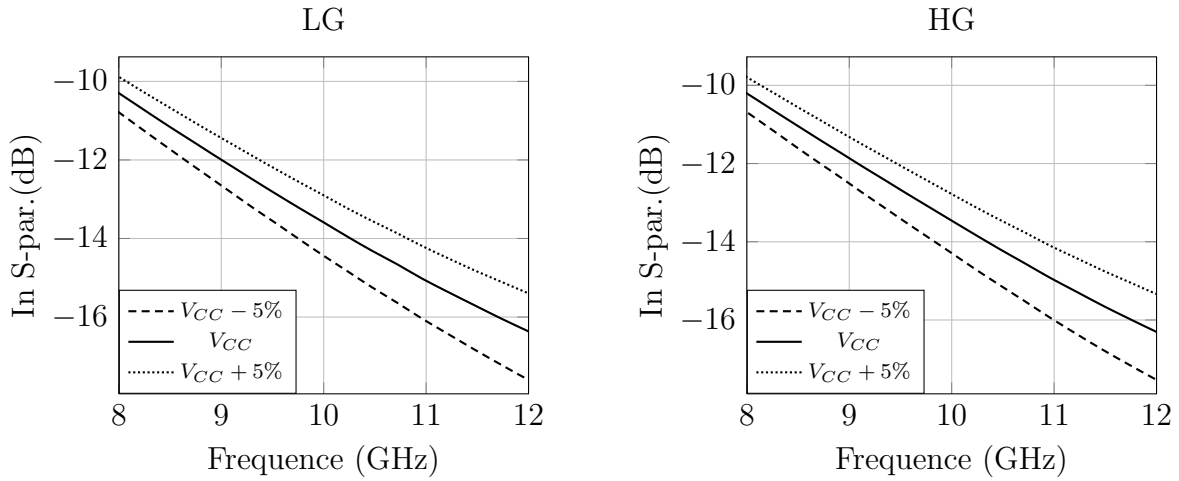


Figure 4.14: Input S-parameter versus input frequency (T = 85℃).

Output return loss

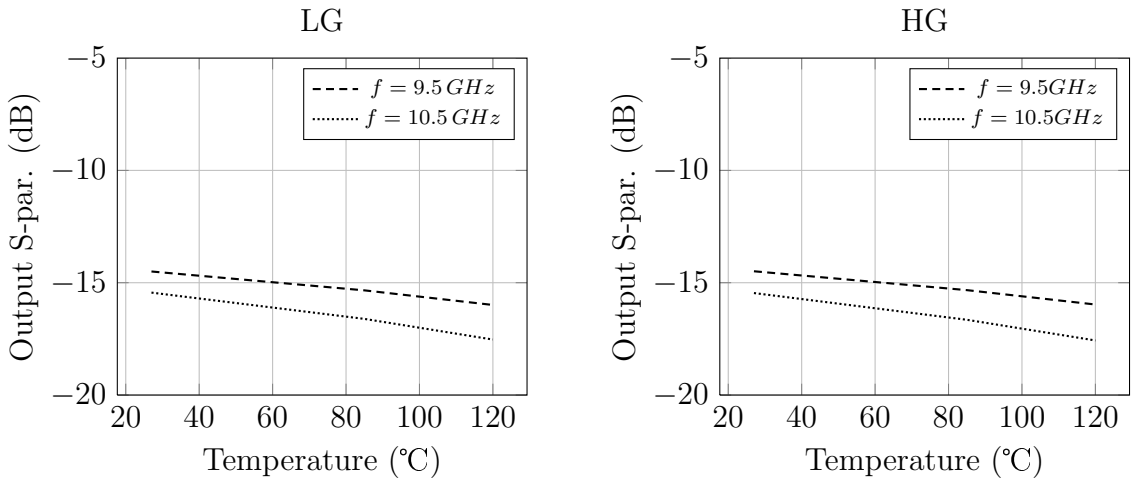


Figure 4.15: Output S-parameter versus temperature ($V_{CC} = 3.3\,V$).

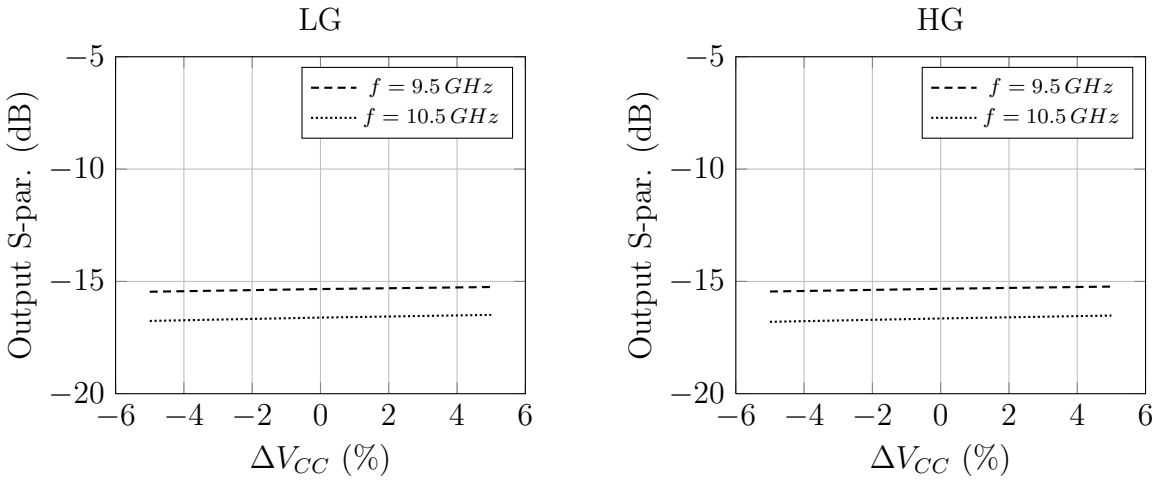


Figure 4.16: Output S-parameter versus supply voltage variation (Temperature = 85℃).

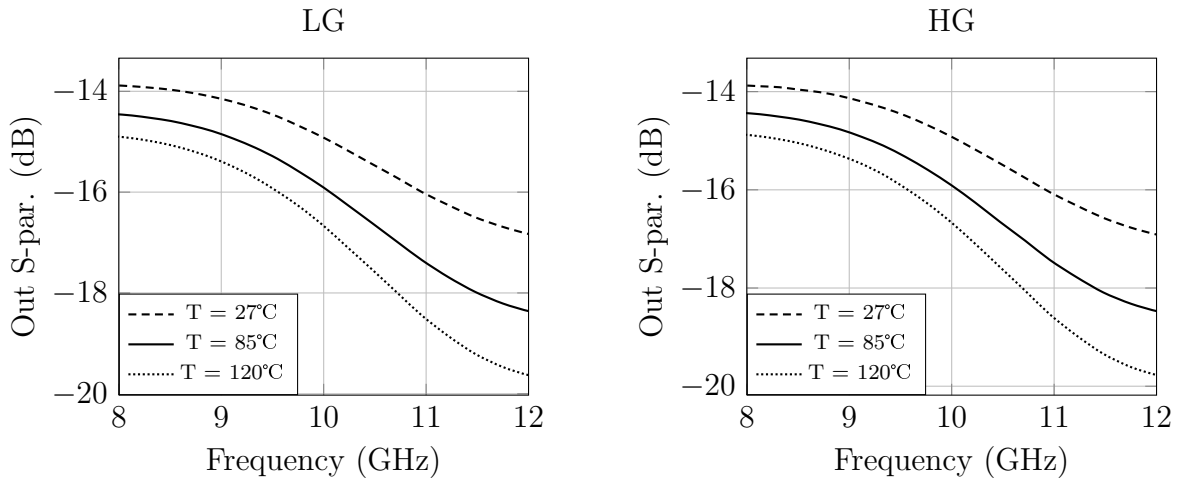


Figure 4.17: Output S-parameter versus input frequency ($V_{CC} = 3.3\,V$).

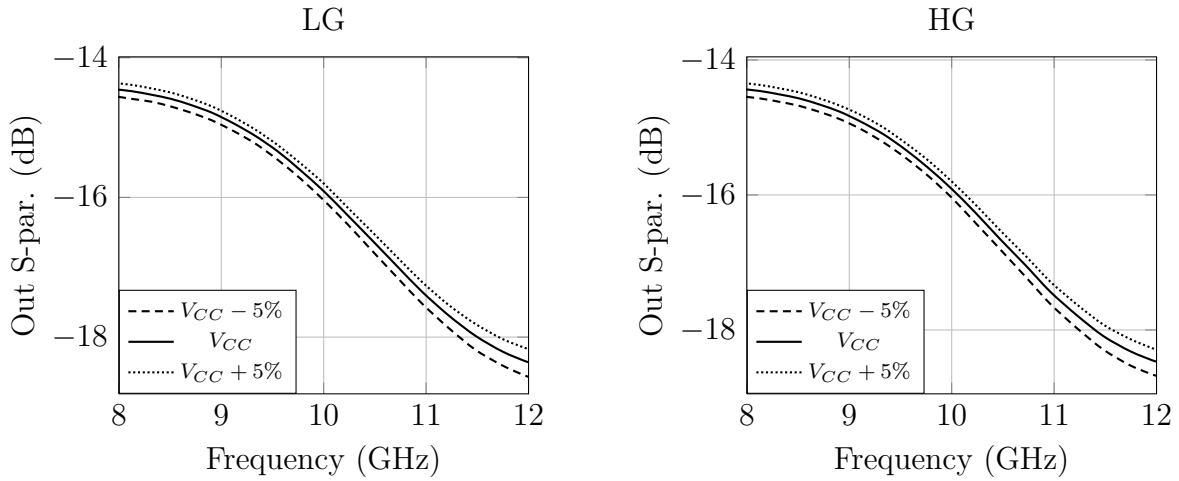


Figure 4.18: Output S-parameter versus input frequency (T = 85℃).

Center frequency

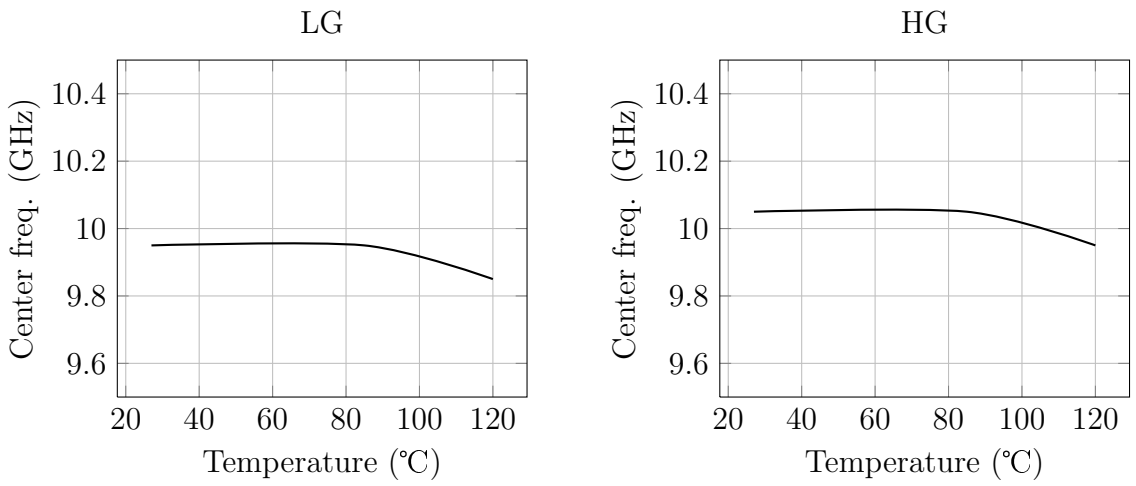


Figure 4.19: Center frequency versus temperature ($V_CC = 3.3\,V$).

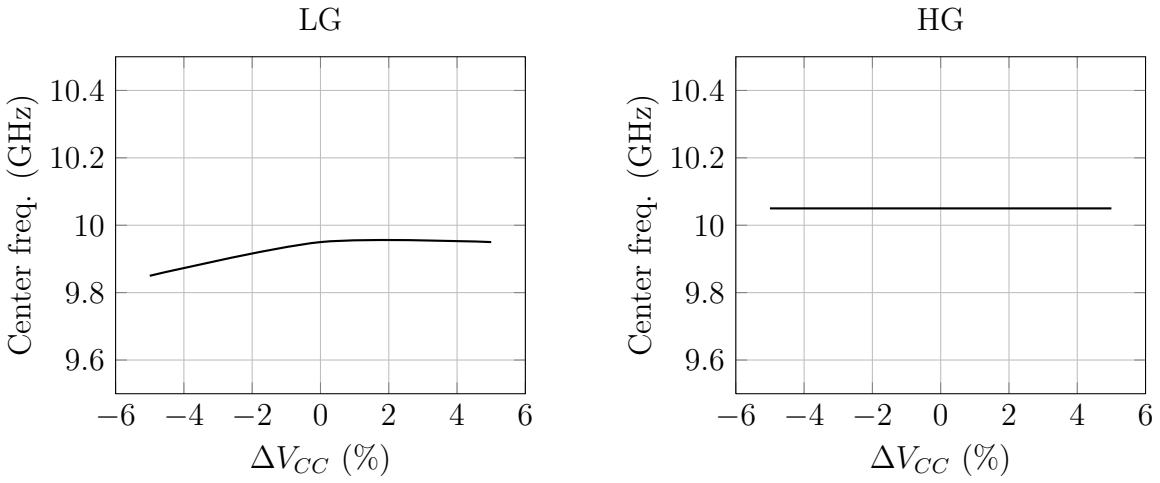


Figure 4.20: Center frequency versus supply voltage variation (Temperature = 85℃).

-2dB bandwidth

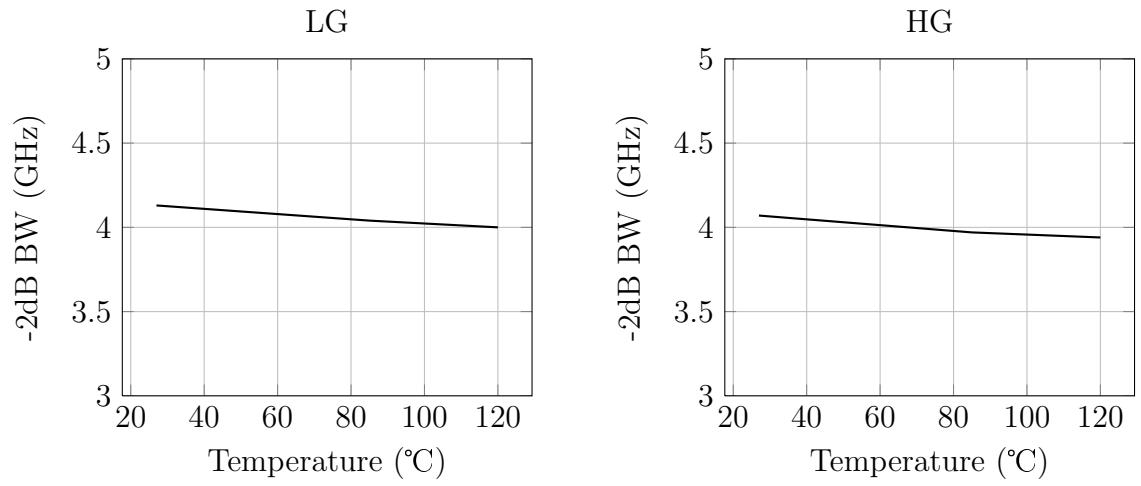


Figure 4.21: -2dB bandwidth versus temperature ($V_{CC} = 3.3\,V$).

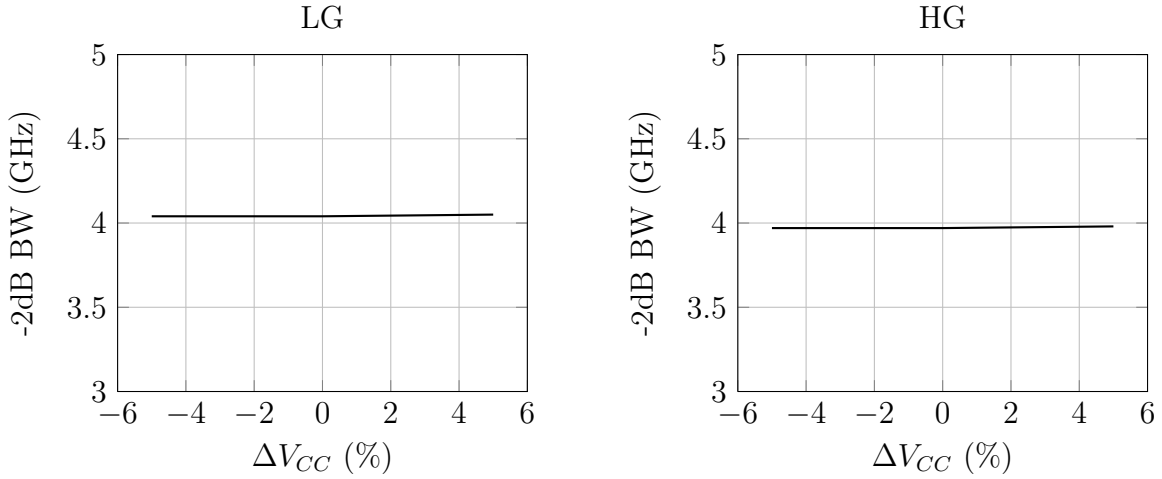


Figure 4.22: -2dB bandwidth versus supply voltage variation (Temperature = 85℃).

-3dB bandwidth

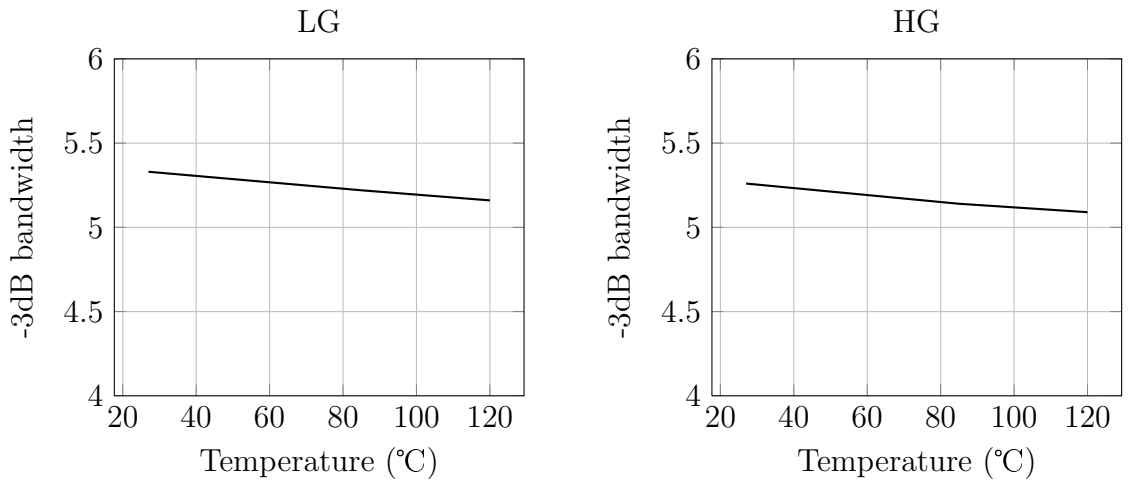


Figure 4.23: -3dB bandwidth versus temperature ($V_{CC} = 3.3\,V$).

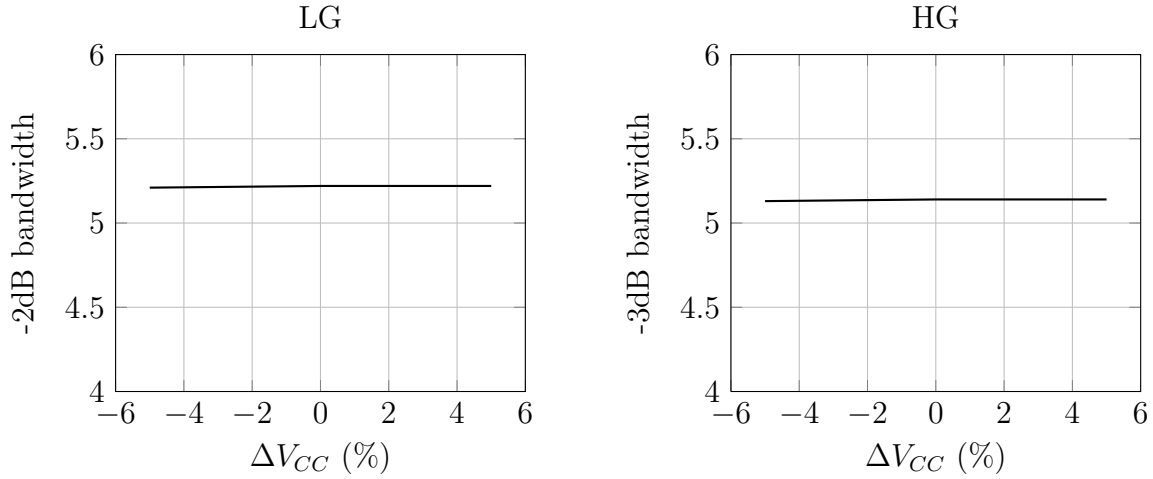


Figure 4.24: -3dB bandwidth versus supply voltage variation (Temperature = 85℃).

Power consumption

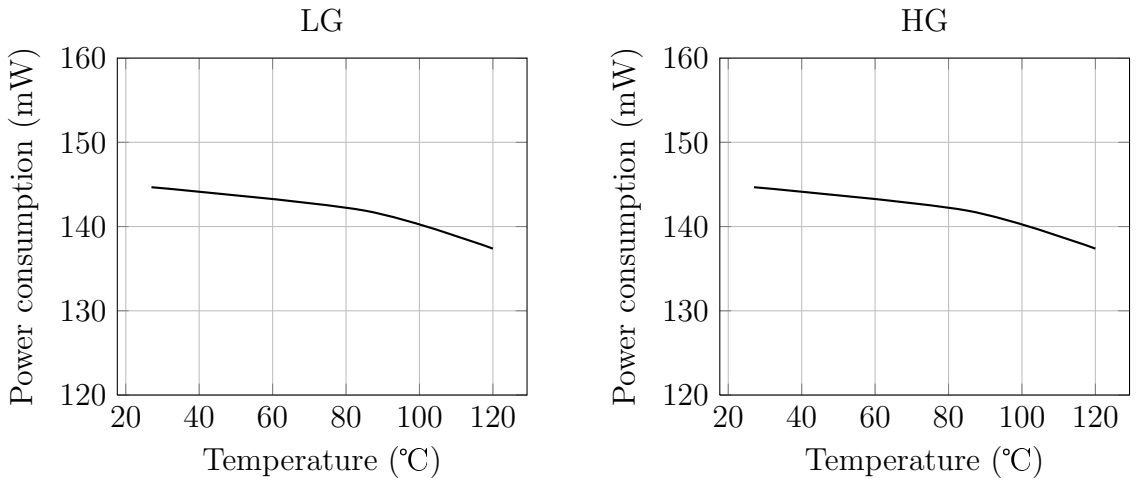


Figure 4.25: Power consumption versus temperature ($V_{CC} = 3.3\,V$).

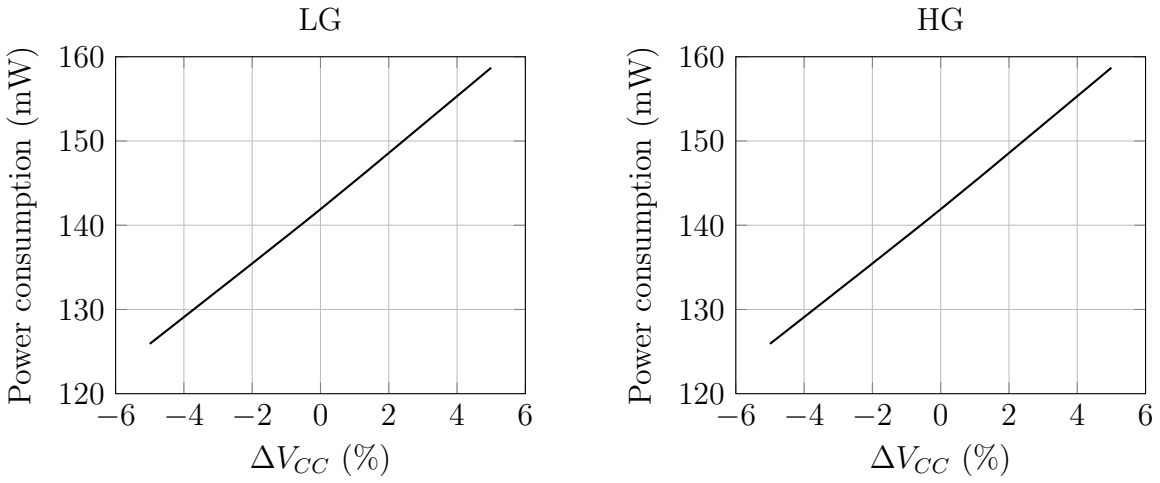
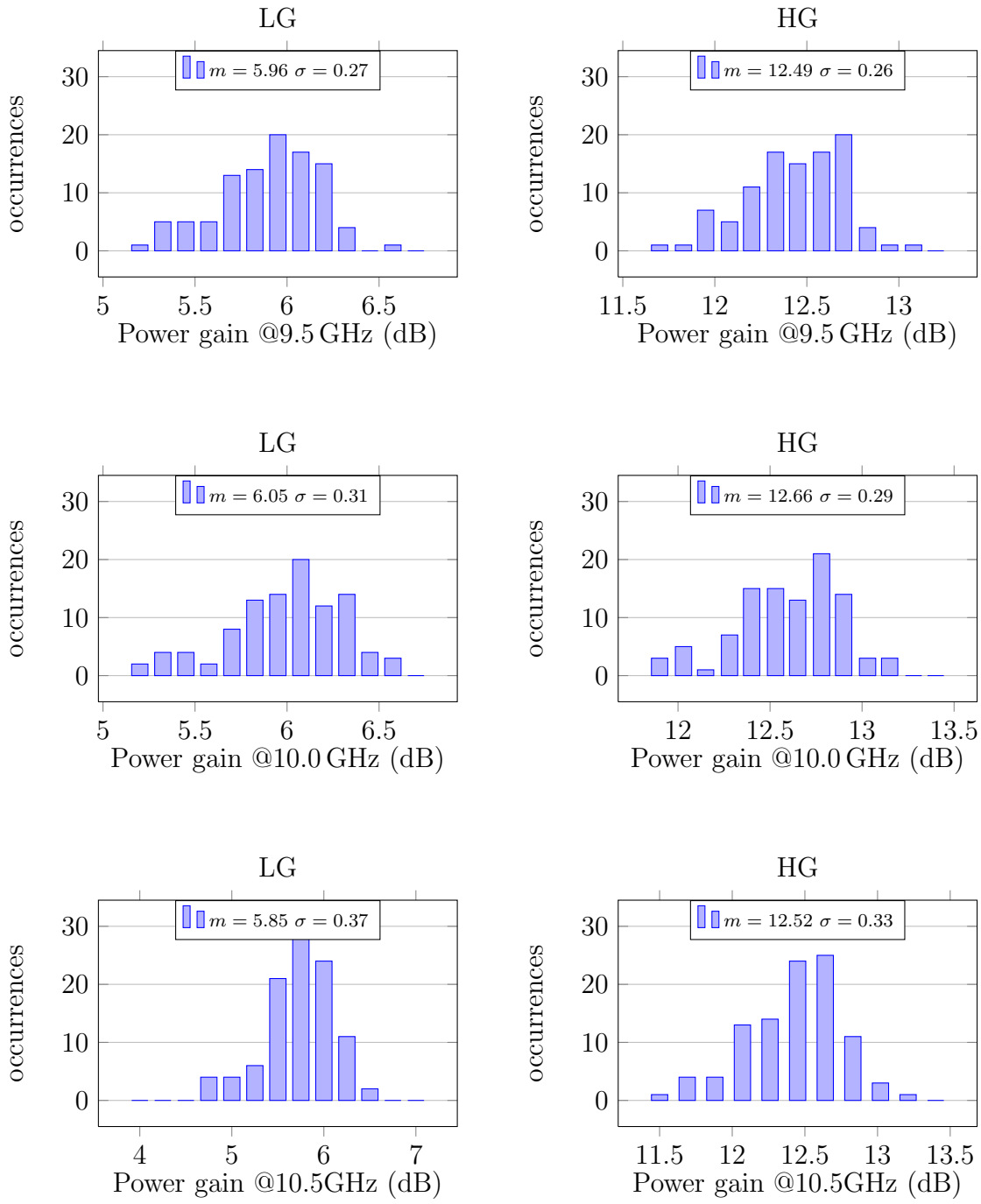


Figure 4.26: Power consumption versus supply voltage variation (Temperature = 85℃).

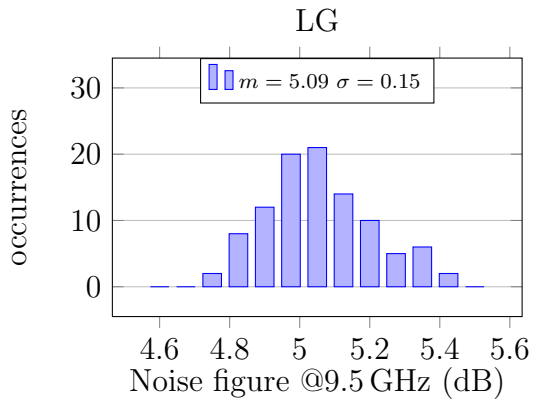
4.1.2 Monte Carlo simulation

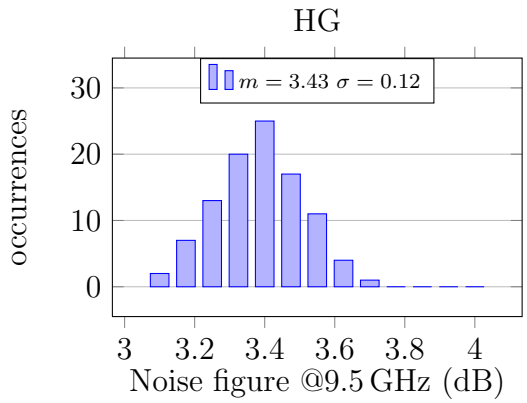
Simulation condition: $P_{RF} = -40\,dBm$, $f_{RF,1} = 10.50\,GHz$ (only for IIP3), $f_{RF,2} = 10.51\,GHz$ (only for IIP3), $V_{CC} = 3.3\,V$, $T = 85$℃.

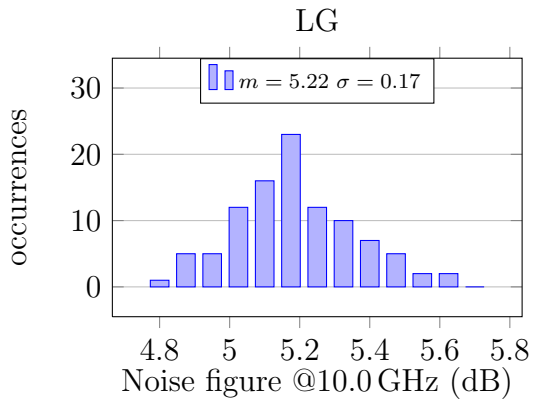
Power gain

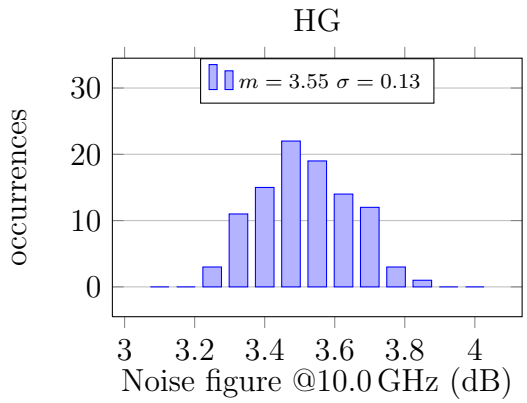


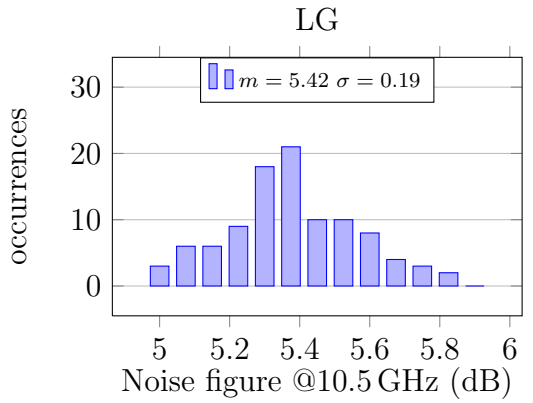
Noise figure

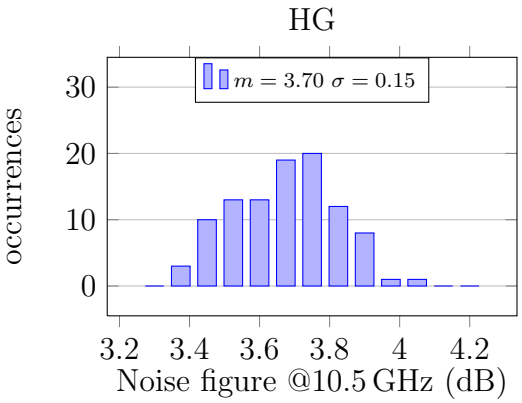




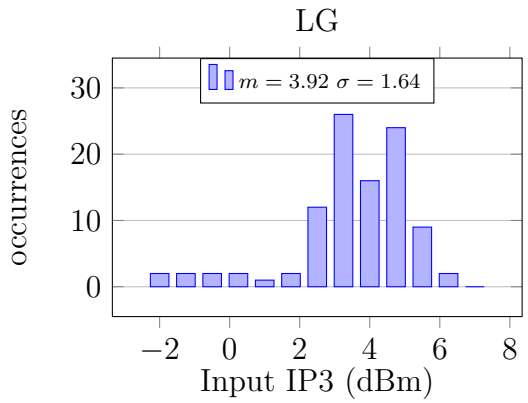


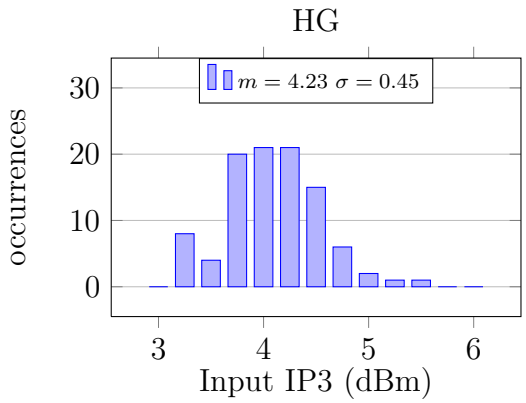


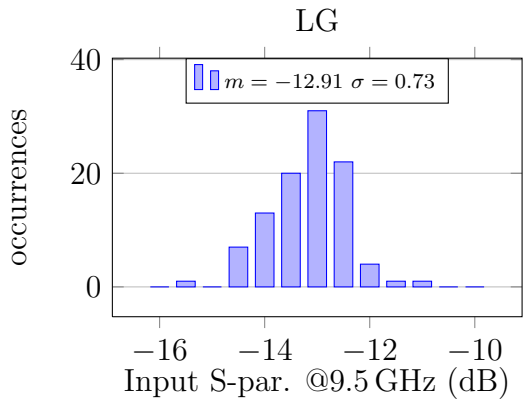


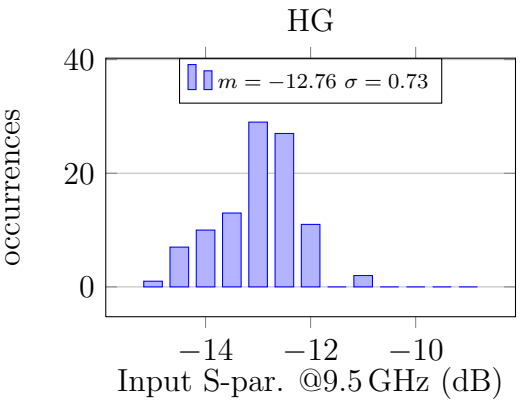


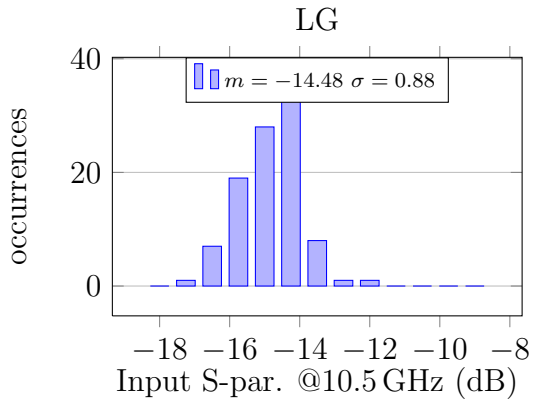
IIP3 and input matching

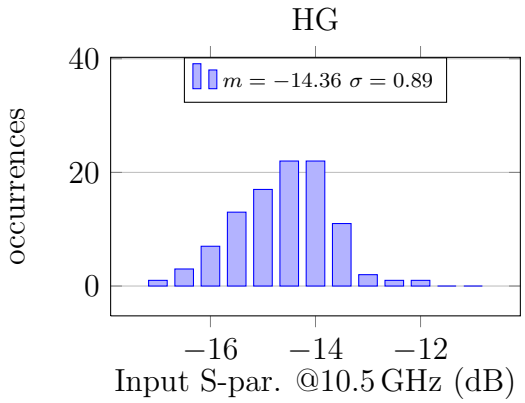




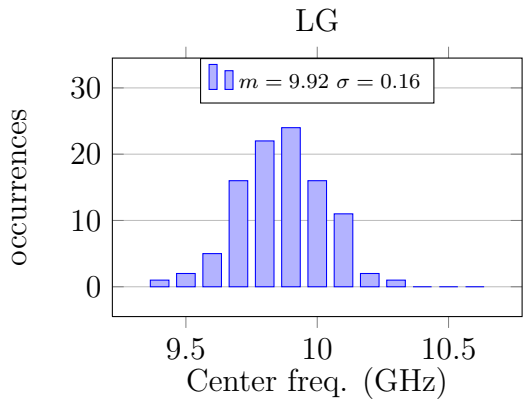


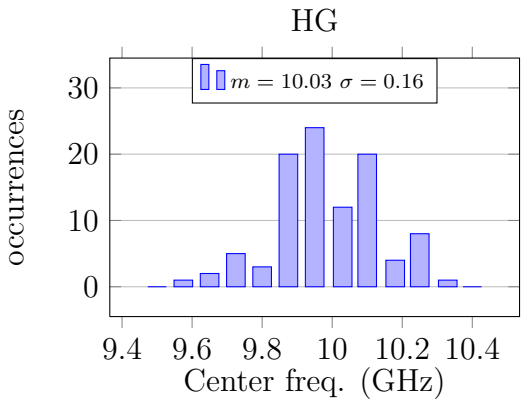


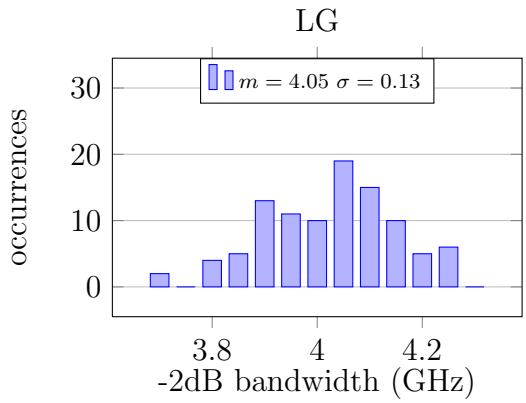


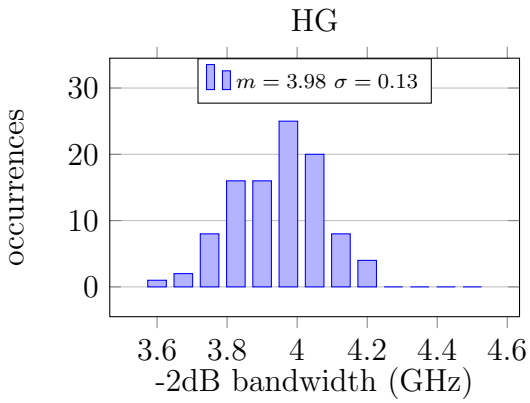


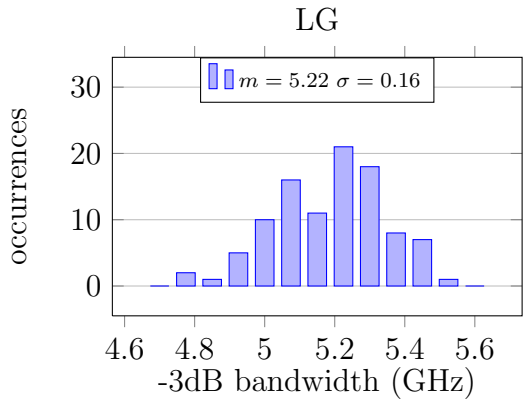
Center frequency and bandwidth

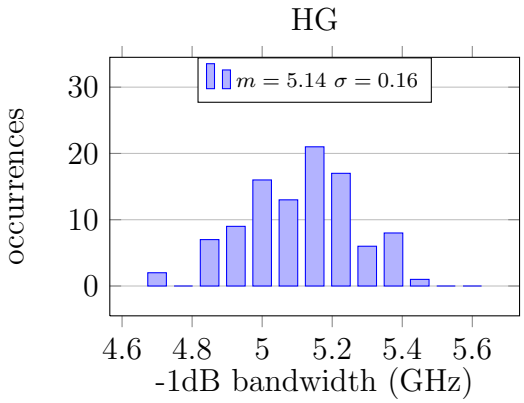












4.1.3 Stability

The setup of the simulation is the same used during design. The K_f and $b_{1,f}$ factors curves are quite similar and circuit is stable. It has also been verified the value of the inductive component introduced by the connection lines between the differential pair collectors and the cascode stages emitters. Its value is around 50pH, the value used during the design, which eliminated the instability (see Section 2.1.7). K-factor is still close to 1 at high frequencies, but it's necessary to consider that this happens when the system has no load connected, that is not the typical situation the circuit has been designed for. Figure 4.27 shows how the two stability parameters change according to input frequencies considering HG selected (HG is the worst case for stability check).

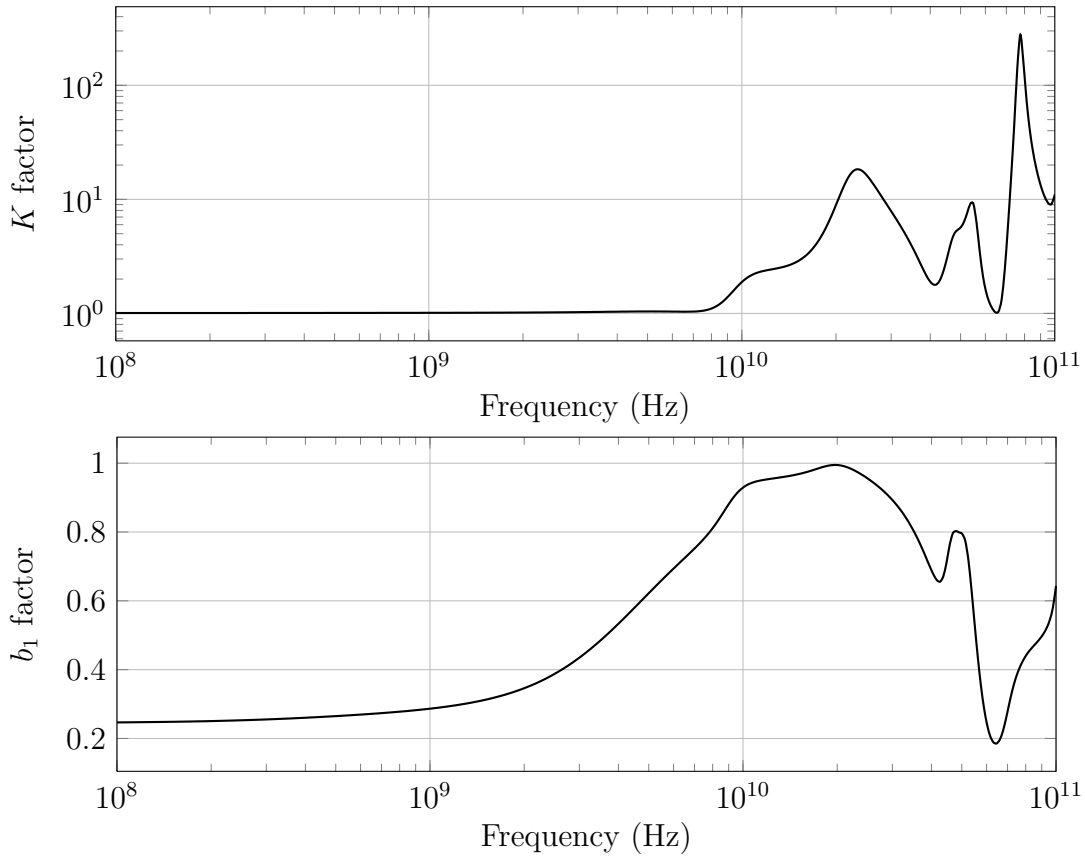


Figure 4.27: K and b_1. Conf.: two single-ended inputs, open outputs, HG selected.

4.1.4 Results summary

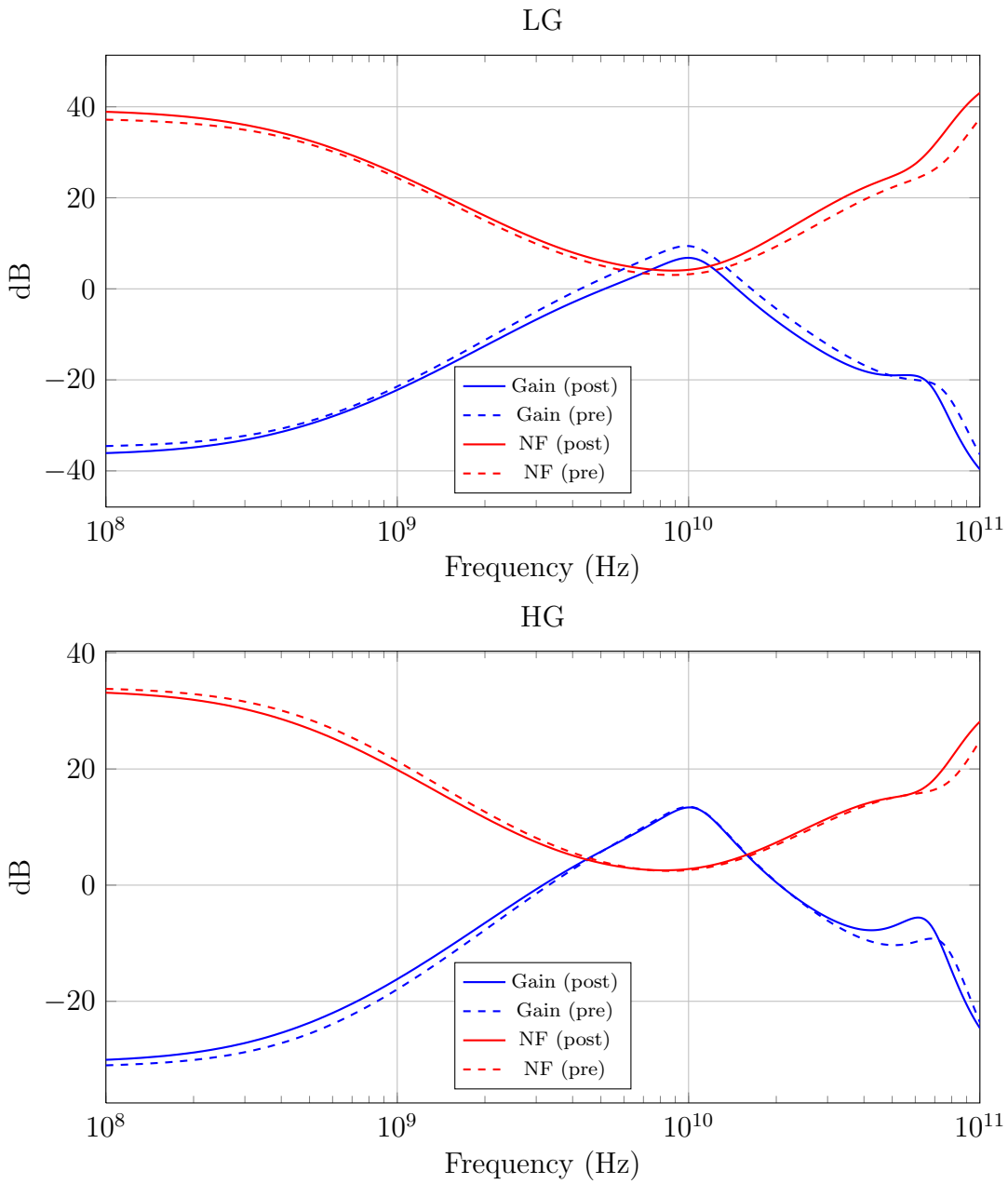


Figure 4.28: Pre- and post-layout power gain and noise figure results comparison ($T = 27℃$, $V_{CC} = 3.3\,V$).

Figure 4.28 compare the curves of gain and noise figure before and after the layout phase. LG configuration results are quite different due to the different value of R_1 and R_2 and are not directly comparable. HG configuration results overlapped exactly at the central frequency and in the bandwidth of the LNA. The pick at very high frequency (60-70GHz) is slightly increased and is the reason of the low K factor seen during stability check.

Tables 4.2 and 4.3 summarize post-layout results and compare them with pre-layout ones (indicated in brackets). Finally Table 4.4 compare current and power consumption of the circuit.

Freq. GHz	**Gain** dB	**NF** dB	**In-RL** dB	**Out-RL** dB	**IIP3** dBm	**f_0** GHz	**-3B BW** GHz	**-2B BW** GHz
9.5	6.69 (9.35)	4.07 (3.10)	10.63 (10)	-14.50 (20.7)	5.4	9.95	5.33	4.13
10,0	6.81 (9.40)	4.18 (3.20)	- (-)	- (-)				
10.5	6.65 (9.18)	4.34 (3.33)	11.73 (11.4)	-15.44 (20.6)	(5.5)	(9.8)	(5.41)	(4.23)

Table 4.2: Low gain configuration LNA results (T = 27℃, V_{CC} = 3.3 V, P_{IN} = -40 dBm).

Freq. GHz	**Gain** dB	**NF** dB	**In-RL** dB	**Out-RL** dB	**IIP3** dBm	**f_0** GHz	**-3B BW** GHz	**-2B BW** GHz
9.5	13.19 (13.35)	2.68 (2.52)	10.63 (9.9)	-14.50 (20.7)	4.7	10.05	5.26	4.07
10.0	13.38 (13.48)	2.78 (2.60)	- (-)	- (-)				
10.5	13.27 (13.33)	2.91 (2.71)	11.73 (11.3)	-15.44 (20.7)	(4.4)	(10.0)	(5.37)	(4.17)

Table 4.3: High gain configuration LNA results (T = 27℃, V_{CC} = 3.3 V, P_{IN} = -40 dBm).

Conf.	**Current cons.** mA	**Power cons.** mW
LG	43.8 (40.3)	144.5 (133.0)
HG	43.8 (40.3)	144.5 (133.0)

Table 4.4: Current and power consumption (T = 27℃, V_{CC} = 3.3 V, P_{IN} = -40 dBm).

4.2 Quadrature mixer

Before to show results it's good summarize changes made during layout phase:

- Redesign of degeneration inductors to fit the layout and reduce noise figure;
- introduction of real transformers tuned trough a capacitor connected in parallel with the primary;
- mixer load is placed far from the switching pair to keep RF paths as shot as possible;
- return to the 2-stage version for the LO driver;
- reduction in the size of the decoupling capacitors;
- introduction of decoupling capacitors between the PPF and the polyphase filter;
- removal of the capacitors of the load of the mixer.

The paths between differential pair collectors and switching stage emitters in the mixer core have been reduced in length as much as possible because of their strong influence on circuit linearity.
As the in the LNA the simulation setup is the same used during design phase. A Monte Carlo simulation returns the sensibility of the circuit to the process quality and mismatches.
Important to note: all the parameters refer to the RF and LO inputs and the I-output (the results of the Q output are almost identical thanks to the symmetry of the circuit).

4.2.1 Temperature and supply voltage sensibility

Conversion gain

Simulation condition (unless otherwise specified): T = 85℃, $V_{CC} = 5.0\,V$, $V_{CCA} = 3.3\,V$, $P_{RF} = -20dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$.

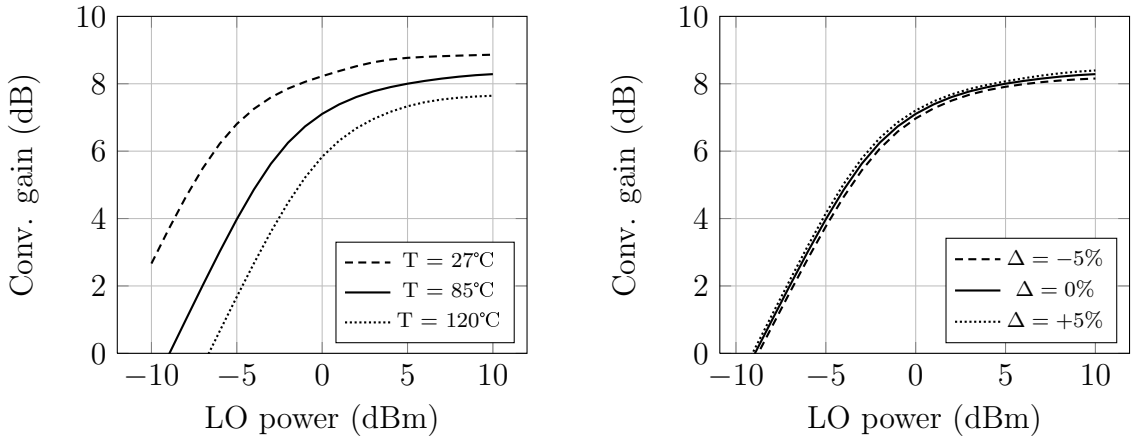


Figure 4.29: Conversion gain versus LO-input power.

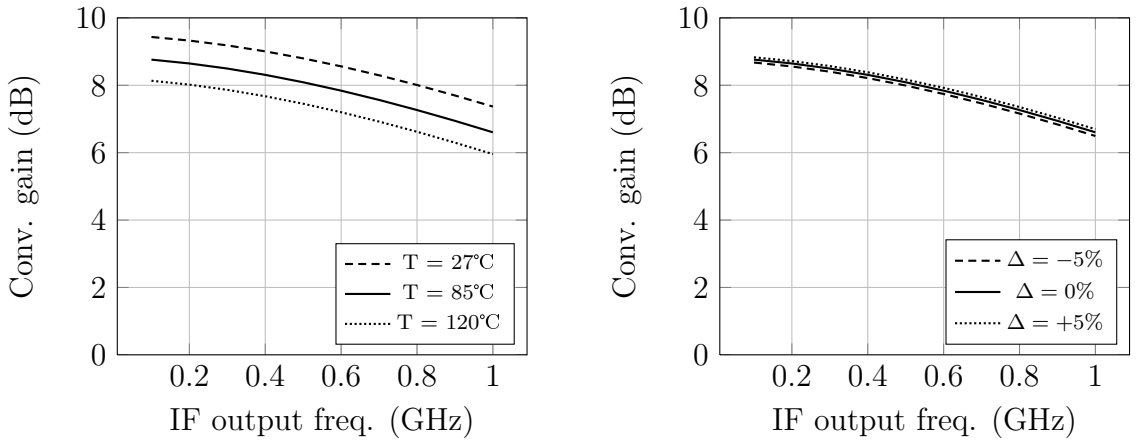


Figure 4.30: Conversion gain versus IF-output frequency.

Input IP3

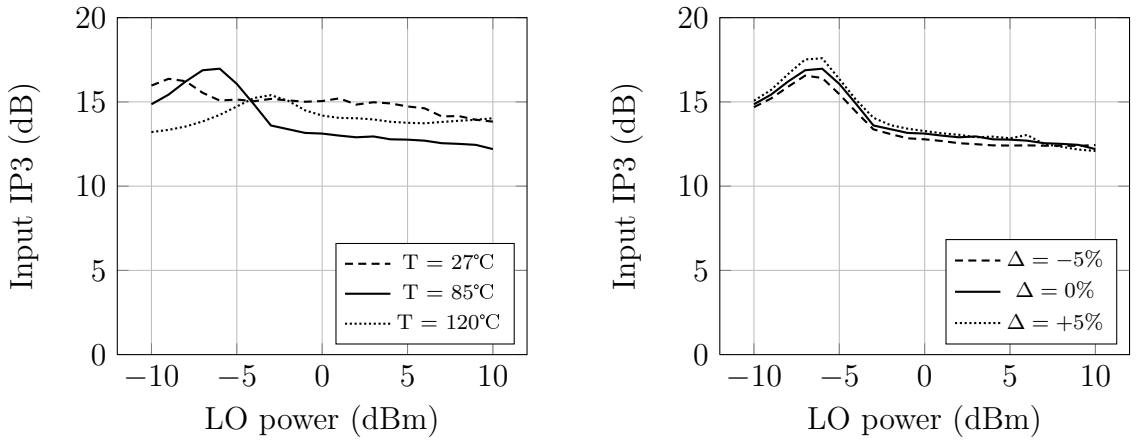


Figure 4.31: Input IP3 versus LO-input power.

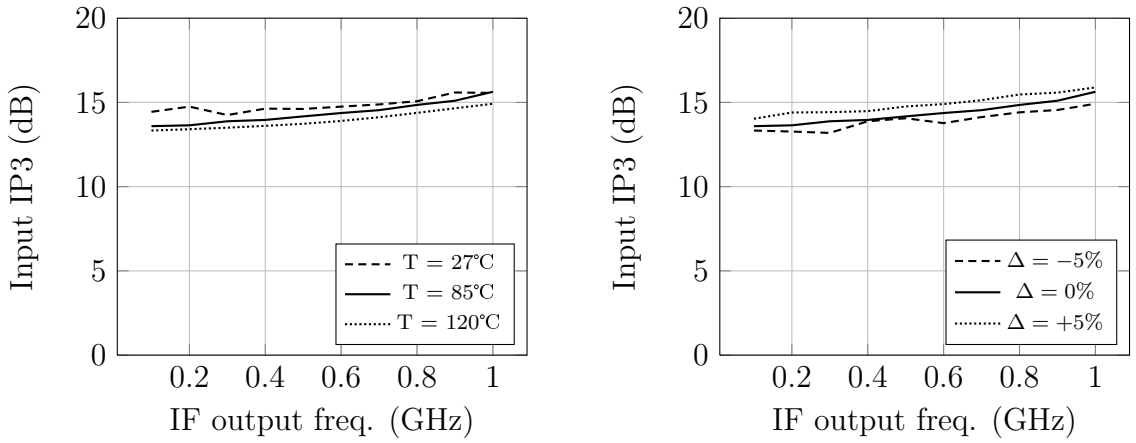


Figure 4.32: Input IP3 versus IF-output frequency.

SSB noise figure

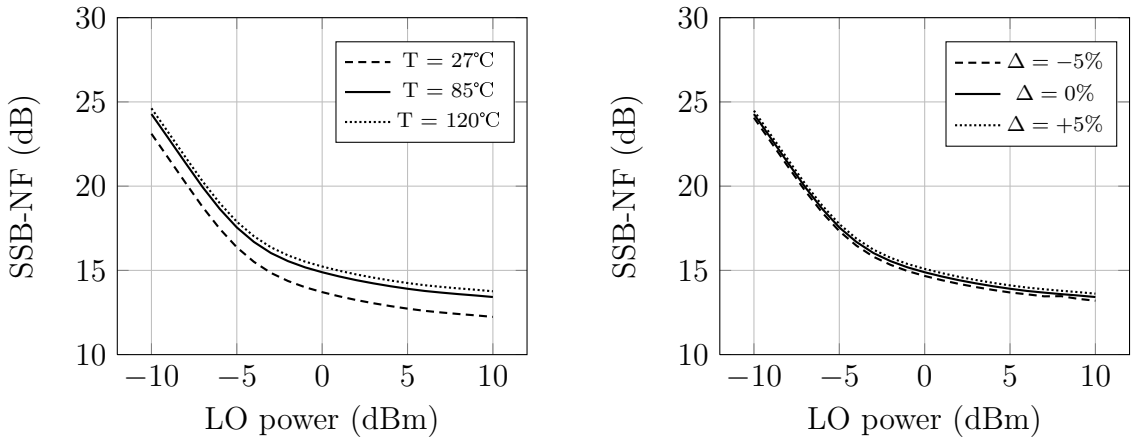


Figure 4.33: SSB noise figure versus LO-input power.

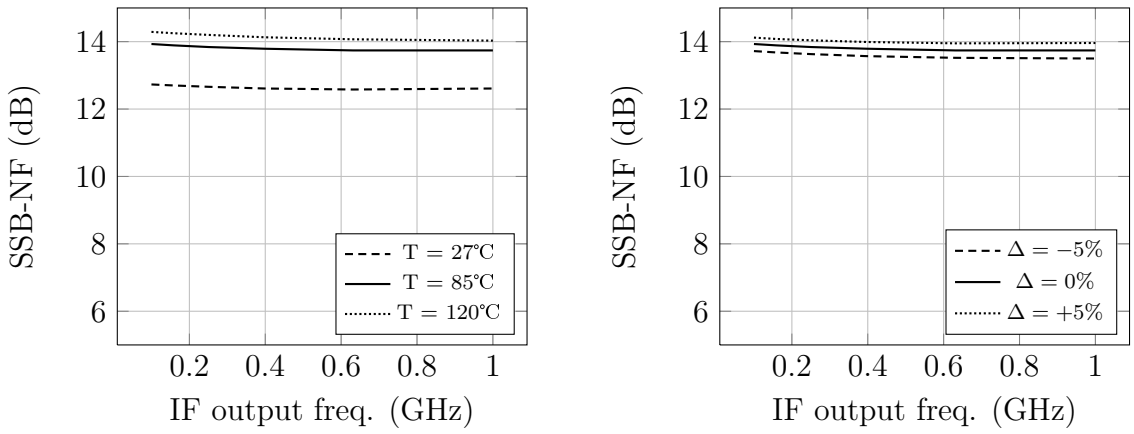


Figure 4.34: SSB noise figure versus IF-output frequency.

DSB noise figure

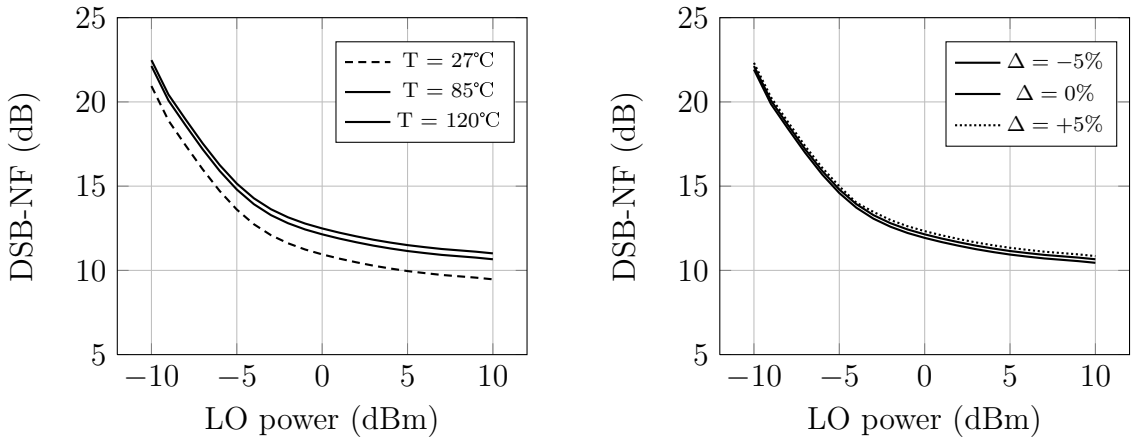


Figure 4.35: DSB noise figure versus LO-input power.

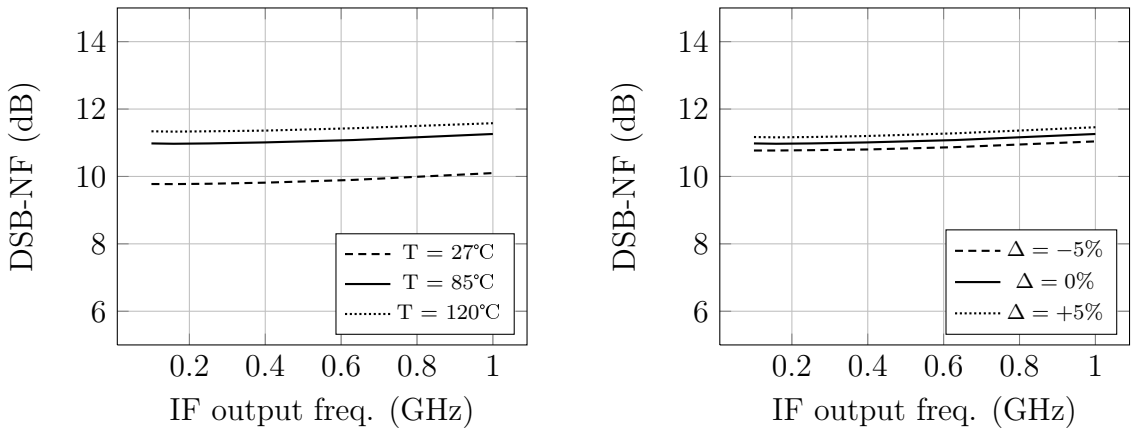


Figure 4.36: DSB noise figure versus IF-output frequency.

RF-input return loss

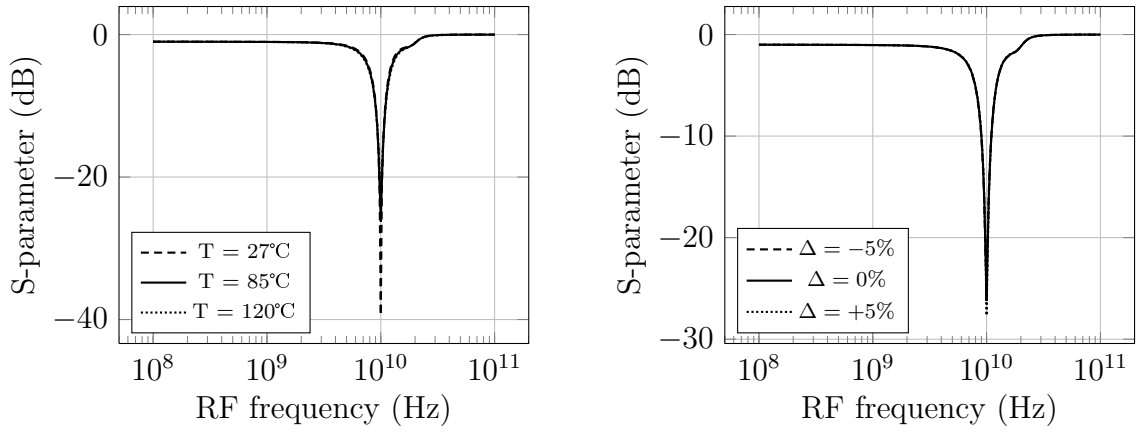


Figure 4.37: RF-input S-parameter versus IF-output frequency.

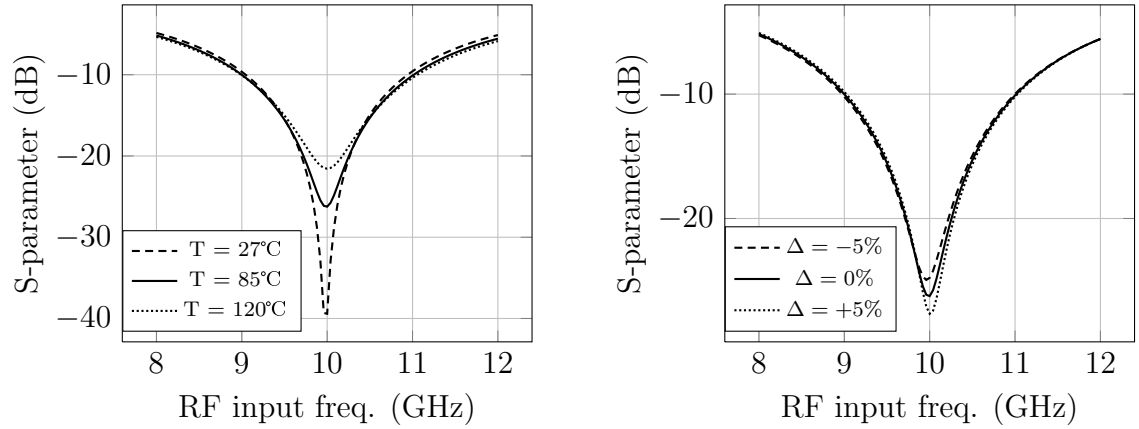


Figure 4.38: RF-input S-parameter versus IF-output frequency.

LO-input return loss

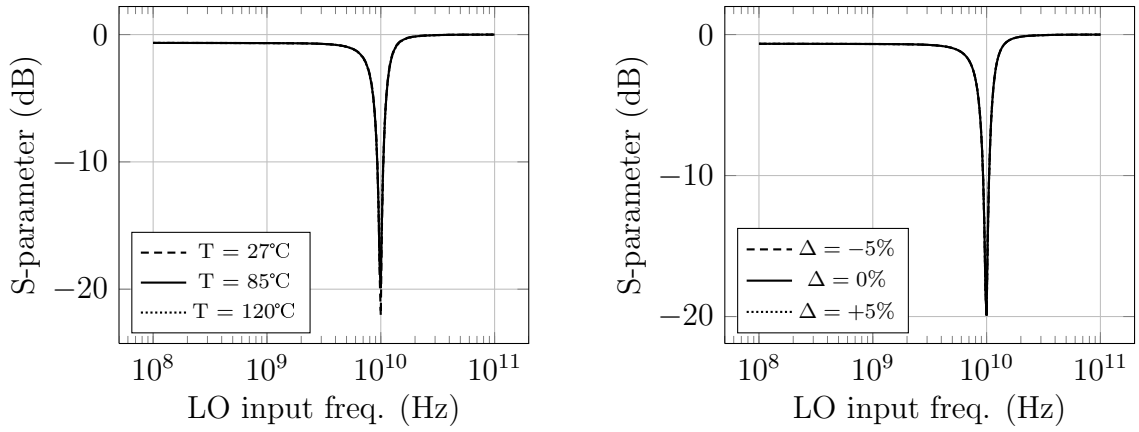


Figure 4.39: LO-input S-parameter versus IF-output frequency.

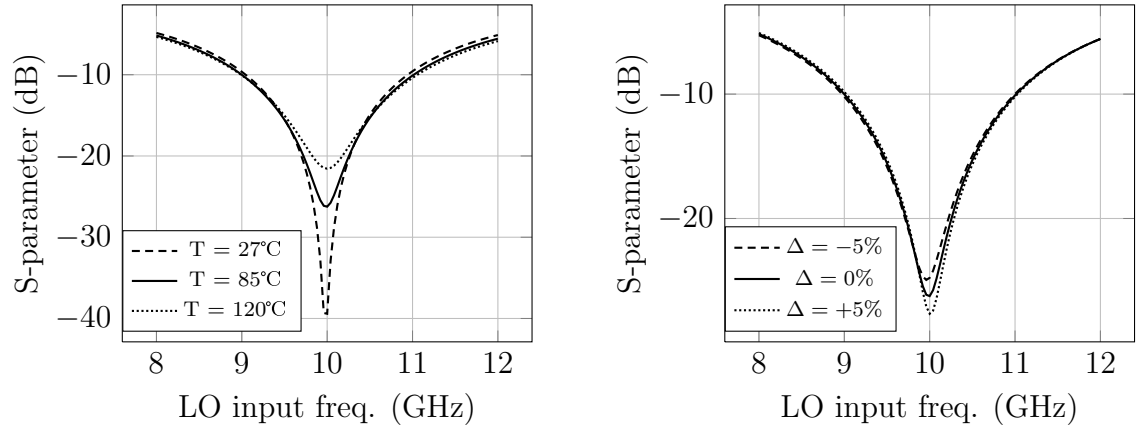


Figure 4.40: LO-input S-parameter versus IF-output frequency.

IF-output return loss

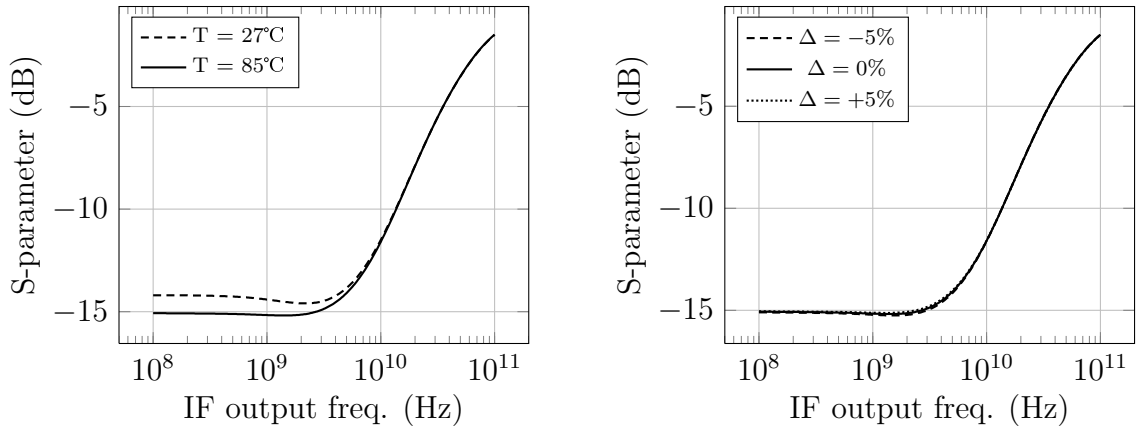
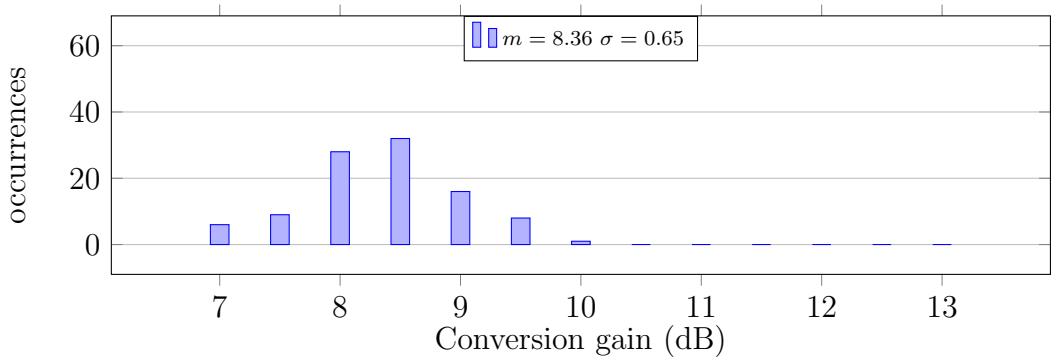
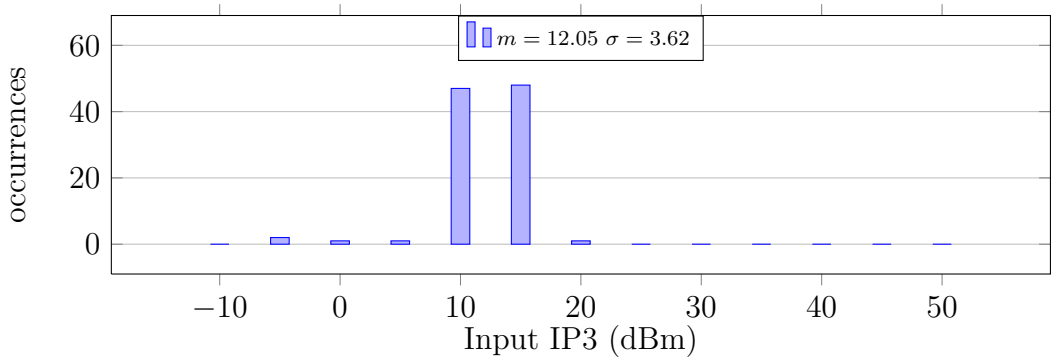


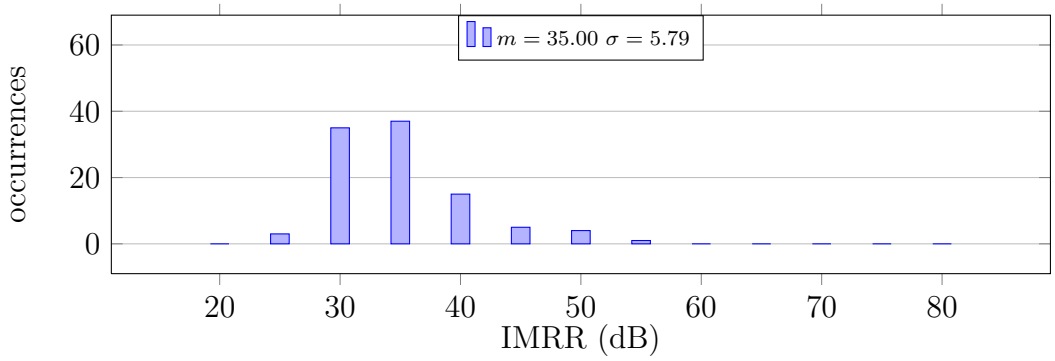
Figure 4.41: IF-output S-parameter versus IF-output frequency.

4.2.2 Monte Carlo simulation

Simulation condition (unless otherwise specified): T = 85℃, $V_{CC} = 5.0\,V$, $V_{CCA} = 3.3\,V$, $P_{RF} = -20dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$.







4.2.3 Stability

The same simulation setup reported in Section 2.2.9 is used. Only one configuration has a K factor below 1 at around 450 MHz. This is case when the outputs of the mixer are not connected to a load and there are two single-ended sources at the RF input.
In the biasing circuits have been added some resistors between the PNP collector and the node where the reference current is taken. Between this node and ground is also connected a cap to provide a low-impedance path to high-frequencies signals and protect the circuit from disturbs. Removing this cap in the Gilbert double-balanced mixers biasing circuit eliminates instability at low frequencies. Figure 4.42 reports stability factors for the unstable version of the circuit, showing the possible instability at 400-450 MHz.

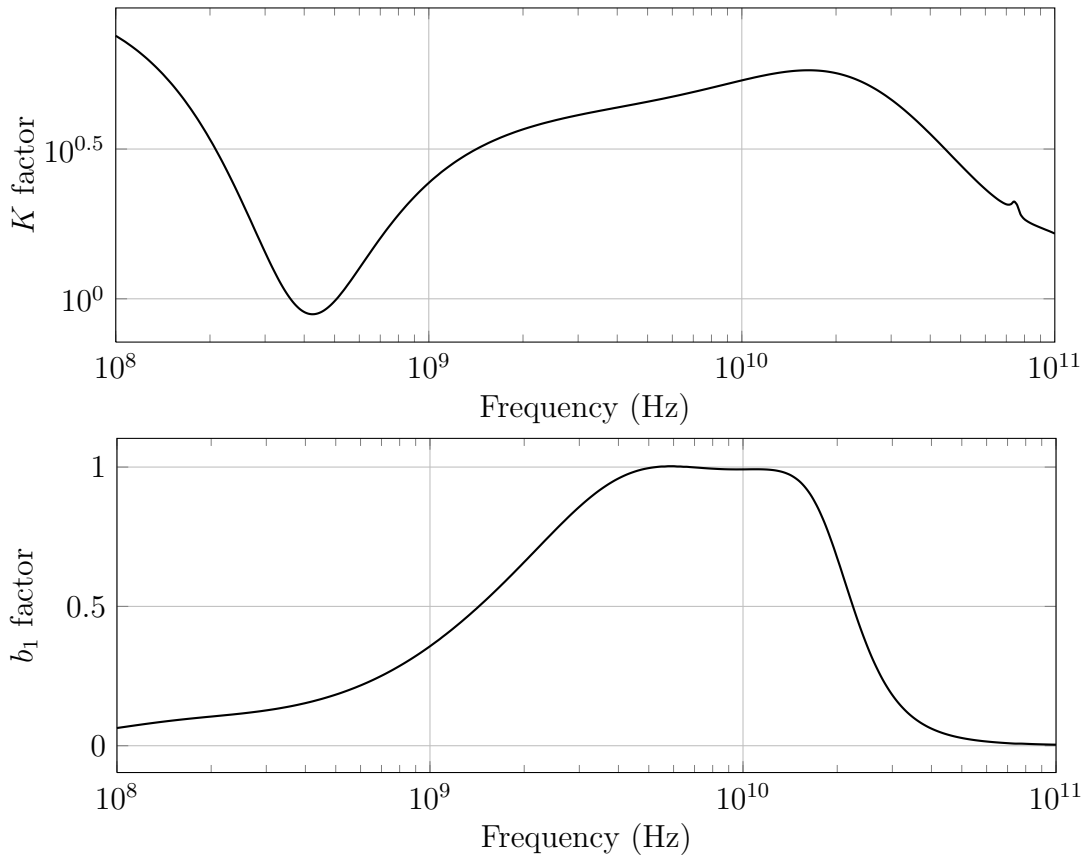


Figure 4.42: K_f and $b_{1,f}$. Conf.: two single-ended RF inputs, open outputs, LO signal set to 0 V (both switching pairs on)

4.2.4 Results summary

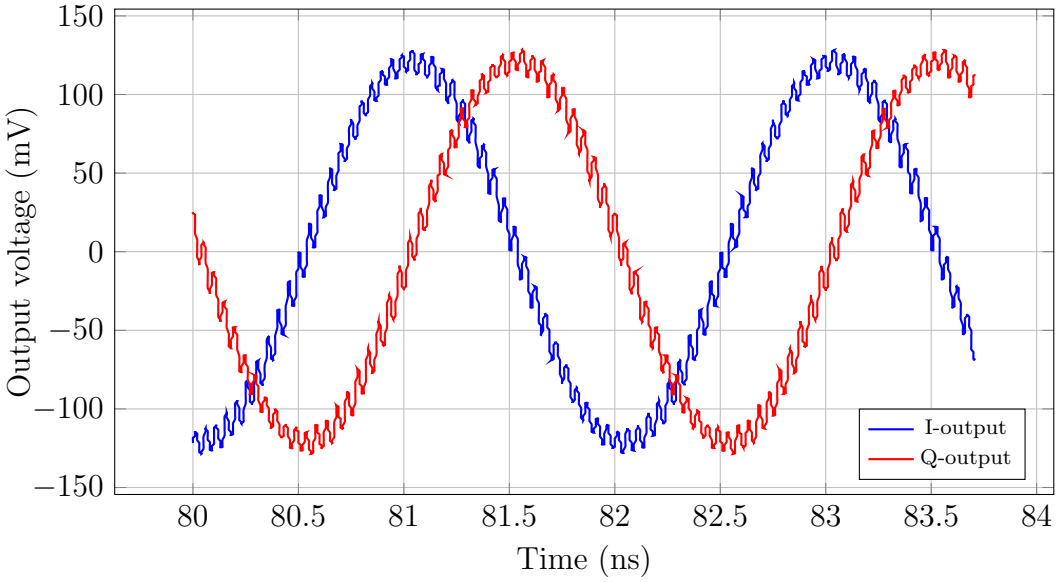


Figure 4.43: I and Q differential output signals from transient simulation ($T = 27$℃, $V_{CC} = 5\,V$, $V_{CCA} = 3.3\,V$, $P_{RF} = -20\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF} = 10.5\,GHz$, $f_{LO} = 10\,GHz$).

Figure 4.43 shows the two signals at the output of the quadrature mixer when at RF input there is a 10.5 GHz signal composed by in-phase and in-quadrature components with the same amplitude. The LO signal is a 10 GHz sinusoid. The resulting curves are two signals similar to a sine at the frequency of 500 MHz ($f_{RF} - fLO$) with phase difference of 90° as expected.
It's evident the presence of components at a frequency close to 20 GHz due to intermodulation products. They are not a problem if it's considered the limited bandwidth of the PGA, which can easily filter the signal reducing them.
Figures 4.44 and 4.45 represent the power spectrum of the I-differential output. In 4.44 it's possible to see the components at high frequencies found also in the transient simulation results. In 4.45 are visible the two fundamental tones at 500 MHz and 510 MHz, result of the down-conversion of the two tones at 10.5 GHz and 10.51 GHz. Are also present the two 3-order intermodulation products at 490 MHz and 520 MHz ($2f_1 - f_2$ and $2f_2 - f_1$). These four components are the ones needed for the extrapolation of IIP3. Tables 4.5, 4.6, 4.7 and 4.8 summarize the results of the quadrature mixer comparing them with the pre-layout ones (between brackets).

Output freq.	**Conv. gain** dB	**Input IP3** dBm	**IF-out RL** dB	**SSB-NF** dB	f_{-1dB} MHz	f_{-3dB} MHz
500 MHz	8.22 (6.56)	15.05 (18.65)	-14.26	∼13.7 (∼13.4)	∼670 (∼550)	>1000 (>1000)

Table 4.5: Quadrature mixer results (T = 27℃, V_{CCA} = 3.3V, V_{CC} = 5.0V, P_{RF} = -20 dBm, P_{LO} = 0 dBm).

Output freq.	**Conv. gain** dB	**Input IP3** dBm	**IF-out RL** dB	**SSB-NF** dB	f_{-1dB} MHz	f_{-3dB} MHz
250 MHz	9.23 (7.13)	14.40 (18.30)	-14.21	∼12.6	∼670	> 1000
500 MHz	8.80 (6.56)	14.61 (18.65)	-14.26			
1 GHz	7.37 (4.74)	15.56 (20.40)	-14.41	(∼13.4)	(∼550)	(>1000)

Table 4.6: Quadrature mixer results (T = 27℃, V_{CCA} = 3.3V, V_{CC} = 5.0V, P_{RF} = -20 dBm, P_{LO} = 6 dBm).

Input freq.	**RF-input RL** dB	**LO-input RL** dB
9 GHz	-15.47	-12.48
10 GHz	-39.42	-22.06
11 GHz	-14.93	-10.41

Table 4.7: Quadrature mixer RF and LO inputs return loss (T = 27℃, V_{CCA} = 3.3 V, V_{CC} = 5.0 V).

	current cons. mA	**power cons.** mW
$\mathbf{V_{CC}}$ **= 3.3 V**	162.6	813
$\mathbf{V_{CCA}}$ **= 5.0 V**	37.4	123
Total	-	936

Table 4.8: Quadrature mixer current and power consumption (T = 27℃, V_{CCA} = 3.3 V, V_{CC} = 5.0 V).

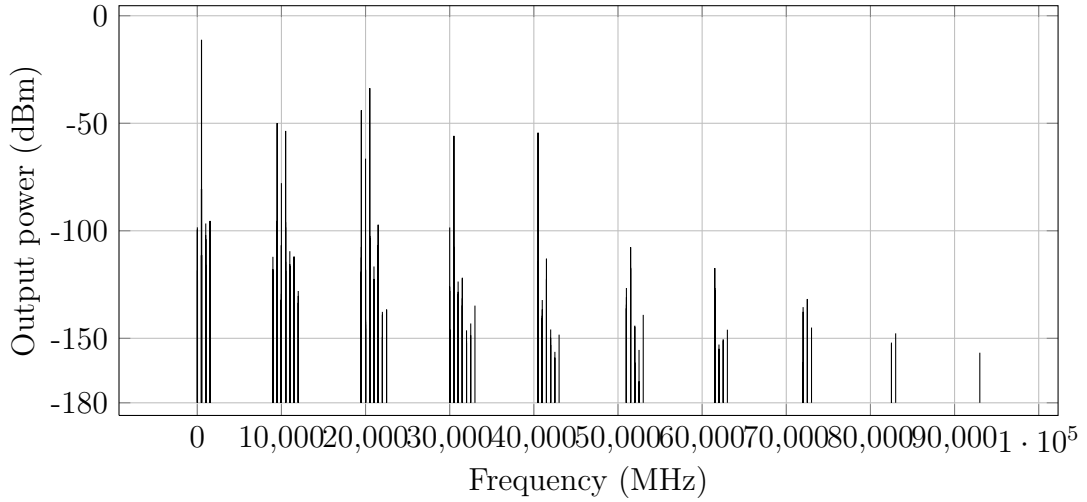


Figure 4.44: I-differential output power spectrum ($T = 27$℃, $P_{RF} = -20\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$).

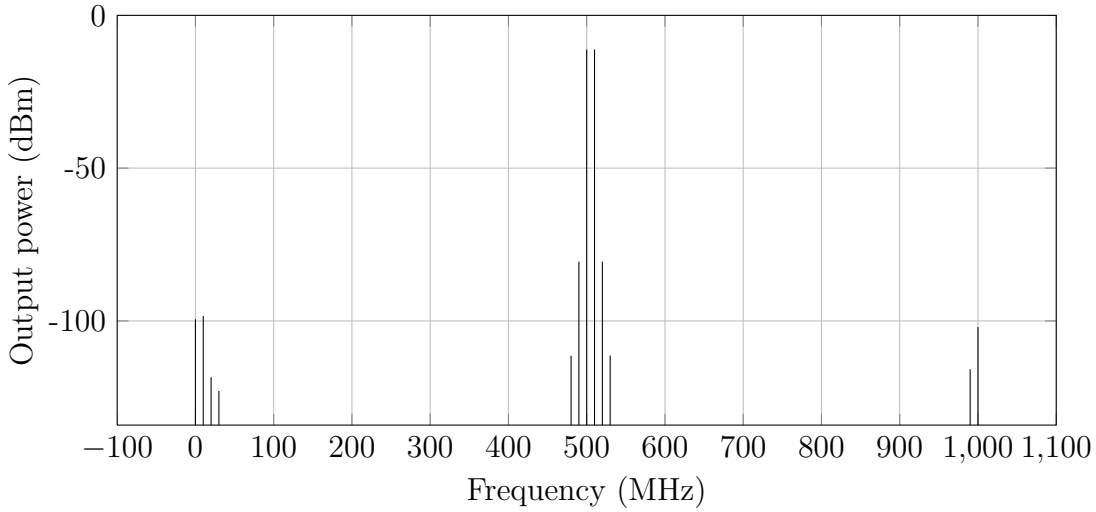


Figure 4.45: I-differential output power spectrum (zoomed graph)($T = 27$℃, $P_{RF} = -20\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$).

Mixers comparison

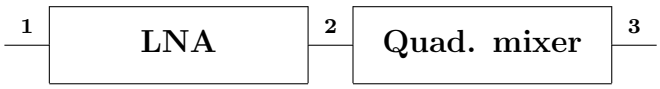
In this Section will be presented a comparison between this work and its results and some commercial products to understand which level of performance have been reached.

parameter	[31]	[32]	[33]	[34](2)	**this work**	**single mixer**	**unit**
mixer typology	single	single	single	single	quadrature	single	
RF frequency	1.2	1.95	3.9	5.8	10.5	10.5	GHz
LO frequency	1.6	1.75	3.4	5	10	10	GHz
IF frequency	0.4	0.2	0.5	0.8	0.5	0.5	GHz
Z_{IN} (RF/IF inputs)	50	50	50	50	100	200	Ω
RF port RL	10	15	24	12	15	21	dB
LO port RL	10	14	18	12	22	22	dB
IF port RL	(1)	15	(1)	(1)	14	14	dB
LO power	0	+3	0	+2	0	0	dBm
Conversion gain	4.5	8.5	8.4	6.4	8.2	14.1	dB
Input IP3	24	24	24.8	25.8	15.1	9.8	dBm
SSB noise figure	10.5	9.5	9.8	12.8	13.7	9.8	dB
Supply voltage	5	5	5	3.3	5/3.3	5/3.3	V
Current cons.	84	202	230	194	162.6/37.4	81.3/18.7	mA
Power cons.	420	1010	1150	640	936	468	mW

Table 4.9: Comparison between this work and some commercial mixers(T = 27℃, (1)- the mixer as not output buffer, output impedance correspond to the load of the mixer, (2) This product uses different technologies.).

4.3 LNA and quadrature mixer combination

LNA and quadrature mixer have been connected together to see if simulation results coincide with calculated ones. The DSB-NF is considered for the mixer. Table 4.3 summarizes and comparer the three most important parameters.



Stage parameters						
Gain (dB)		13.4		8.8		
Noise figure (dB)		2.9		9.9		
Input IP3 (dBm)		4.7		14.7		
Cascoded parameters						**Simulation**
Gain (dB)		13.4		22.2		**22.2**
Noise figure (dB)		2.9		3.7		**3,7**
Input IP3 (dBm)		4.7		-0.3		**-0.4**

Table 4.10: Comparison between calculated and simulated cascaded results ($T = 27$℃, typical supply voltages, $P_{RF} = -40\,dBm$, $P_{LO} = 6\,dBm$, $f_{RF,1} = 10.5\,GHz$, $f_{RF,2} = 10.51\,GHz$, $f_{LO} = 10\,GHz$)

Chapter 5

Conclusion

This work reports on the redesign of LNA and quadrature mixer circuits to be combined with a baseband PGA in order to obtain a 10GHz to baseband down-converting receiver presenting a high gain (70 dB), low noise figure (3.5 dB) and a good linearity (3dBm IIP3).
The LNA and quadrature mixer have completely been redesigned for performance and frequency of interest, the baseband PGA has not been modified, but only simulated to report its performance. First simulations with ideal components have clarified the impossibility to achieve the receiver characteristics required by the customer with a gain of 70 dB and high linearity. So separate test-chips for highly linear LNA and quadrature mixers have been designed and layouted to understand their capabilities.
Original LNA structure is modified by adding a gain selection circuit to introduce a programmable gain. The technique used to reduce gain shows a certain linearity sensibility to temperature variation (between 85℃ and between 120℃ IIP3 values there is a difference of 1.6 dB). The LNA has a gain of 13.4 dB, a high IIP3 (+4.7 dBm) and a noise figure of 2.8 dB with a current consumption of 44 mA from a supply voltage of 3.3 V (145 mW). The programmable gain circuit allows the possibility to select a gain of 13.4 or 6.8 dB.
A lot of design effort was invested in the complex RF mixer. The original structure has been extensively modified. The LO frequency has been modified from the 4 GHz to 10 GHz, through the replacement of the polyphase filter, involving the redesign of the LO driver. Finally a buffer is added at the output to match the PGA which needs DC coupling at the input. Considering the choice to design a measurable test-chip two transformers are added to LO and RF inputs for AC coupling. The obtained IQ mixer test-chip has a conversion gain of 8.2 dB and an IIP3 of 15.1 dBm, that means an output IP3 of 23.3 dBm. DSB noise figure is below 11 dB. The circuit uses two different supply voltages: 5.0 V for the mixer core and the output buffer, 3.3 V for the LO-signal driver. The total power consumption is 936 mW.
Considering the attenuation of 4 dB introduced by the output buffer, mixer core reach an OIP3 of 27.3 dBm. The RF-input transformer used in the test-chip has an insertion loss of 3.1 dB. Removed also this element, the quadrature mixer is able to provide a gain of

about 16 dB, 11.5 dBm of IIP3 and a DSB noise figure of 8 dB. These are the characteristics achievable when the mixer is integrated completely in the down-converter. To take advantage of the linearity achieved by the LNA it's necessary to increase the IIP3 of 9 dB with an equivalent reduction of gain. It can be done increasing degeneration inductors of sub-mixers' differential pairs, at the cost of a higher noise figure. This parameter is the bottleneck of the mixer. Finally the single Gilbert double-balanced mixer structure results are compared with commercial product in Table 4.9. Noise figure is one of the lowest and also power consumption is higher then only the AD8344. If the output buffer is not considered as for the other models the total gain is 18.1 dB achieving a total OIP3 of 28 dBm. This result is close to the one of the Analog Device product and around 5 dB lower then MAX9993 and MAX19998, which have more then two times the power consumption of the circuit described in this work. The only circuit that seems to show much better performance is the LTC5544, which, with only 200 mW more, achieves 32 dBm of OIP3. This result is obtained at the cost of noise figure greater than rivals of 2-3 dB.
Analyzing possible future developments of this project, it seems particularly necessary, in light of the comparison with other products already on the market, further study of the quadrature mixer in order to achieve greater linearity.

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