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A 24 GHz Synchronized Super-regenerative receiver in 65 nm CMOS

Tesi di

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A nonna Maria, e alla mia famiglia.

"A ogni passo del suo cammino Siddharta imparava qualcosa di nuovo, poichè il mondo era trasformato e il suo cuore ammaliato. Vedeva il sole sorgere sopra i monti boscosi e tramontare oltre le lontane spiagge popolate di palme. Di notte vedeva ordinarsi in cielo le stelle, e la falce della luna galleggiare come una nave nell'azzurro. Vedeva alberi, stelle, animali, nuvole, arcobaleni, rocce, erbe, fiori, ruscelli e fiumi; vedeva la rugiada luccicare nei cespugli al mattino, alti monti azzurri e diafani nella lontananza; gli uccelli cantavano e le api ronzavano, il vento vibrava argentino nelle risaie. Tutto questo era sempre esistito nei suoi mille aspetti variopinti, sempre erano sorti il sole e la luna, sempre avevano scrosciato i torrenti e ronzato le api, ma nel passato tutto ciò non era stato per Siddharta che un veleno effimero e menzognero calato davanti ai suoi occhi, considerato con diffidenza e destinato a essere trapassato e dissolto dal pensiero, poichè non era realtà: la realtà era al di la delle cose visibili. [...] Bello e piacevole andar così per il mondo e sentirsi così bambino, così risvegliato, così aperto all'immediatezza delle cose, così fiducioso. [...]"

Hermann Hesse, *Siddharta*

Sommario

Questo lavoro presenta il progetto di un ricevitore super-rigenerativo sincronizzato, sviluppato in tecnologia CMOS 65 nm. Il ricevitore adotta una frequenza operativa di 24 GHz ed è progettato per raggiungere una velocità massima di 2 $Gbps$, a partire da un minimo di 100 $Mbps$. La tecnica super-rigenerativa viene impiegata per realizzare un ricevitore a bassa potenza, da utilizzare nella comunicazione a breve distanza ($1 - 10\,m$), e la simulazione dimostra che, lavorando ad 1 $Gbps$, il ricevitore manifesta un rendimento energetico di 3.38 pJ/bit. Il diagramma a blocchi del circuito presenta tre blocchi principali: l'LNA (Low-Noise Amplifier), collegato all'antenna, che garantisce un S_{11} di $-19.62\,dB$ a 24 GHz; l'oscillatore super-rigenerativo (SRO), che è il cuore del circuito; e l'oscillatore ad anello che viene utilizzato per generare il segnale di quench che deve pilotare l'SRO. Teoria, metodi di progettazione e risultati ottenuti sono ampliamente illustrati all'interno della Tesi.

Abstract

This work presents the design of a synchronized super-regenerative receiver developed in 65 nm CMOS technology. The receiver is working with an operating frequency of 24 GHz and it is projected to achieve a maximum data bit rate of 2 $Gbps$, starting from a minimum of 100 $Mbps$. The super-regenerative technique is used to realize a low power receiver for short-range distance ($1-10\ m$), and the simulation shows that working at 1 $Gbps$ the receiver has an energy efficiency of 3.38 pJ/bit. The block diagram of the circuit presents three main blocks: the LNA (Low-Noise Amplifier), connected to the antenna, which guarantees an S_{11} of $-19.62\ dB$ at $24\ GHz$; the Super-Regenerative Oscillator (SRO), which is the heart of the circuit; and the Ring Oscillator which is used to generate the quench signal that has to drive the SRO. Theory, design methods and final results are fully explained inside the Thesis.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

At the beginning of April 2010, during my Education Abroad Program at the University of Santa Barbara, in California, I started to work on my Master Thesis under the supervision of Prof. Patrick Yue, of the ECE Department. During my Master in Electrical Engineering I got really interested about RF design. The first class that I took it was in Italy, at my own University of Padova, with my official supervisor for this Master Thesis, Prof. Andrea Bevilacqua. The class was called Analog-Integrated Circuit Design. Then, during my experience in the United States, I had the possibility to follow two classes in Communication Electronics, and in one of these I met Prof. Yue, who became my American supervisor for this Master Thesis. He proposed to me to work on a particular kind of receiver, using the super-regenerative technique. We are talking about a receiver which is designed to work in the short-range wireless area $(1 - 10\,m)$. The super-regenerative technique is a really nice method to increase the data bit rate, that is the number of bits received per second, still maintaining a really low power consumption. Prof. Yue, in particular, gives to me the possibility to work on it using the IBM10LP technology, which employs the $65\,nm$ CMOS process, working in the $24\,GHz$ frequency band. There was a belief that it would have been possible to realize a receiver capable to work at $1\,Gbps$, and dissipating less than $10\,pJ$ per bit (the energy per bit is a fundamental concept in the Communication area). Before me, already another student, Kung-Hao Liang, in collaboration with Luis Chein, had worked on this project [16]. They used the $60\,GHz$ frequency band, but the best obtained performance was around $200\,Mbps$, with an energy of $50\,pJ/bit$. Thus, for my work, I started considering their circuit configuration, adding then some changes. And, just to have a little anticipation in the introduction about my results, after five month of

work I was able to project a synchronized super-regenerative receiver with a maximum working frequency of 2 *Gbps*; and perfectly in agreement with the initial expectations, working at 1 *Gbps*, my circuit was dissipating just 3.4 pJ/bit.

The Thesis has been organized in this way:

- the introduction is dedicated to the description of possible marketing areas for this kind of receiver, and to focus the attention on some fundamental problems that are coming out using a short-channel device which works at really high frequency;
- in the second chapter I spent time to describe the theory that is important to read to comprehend:
  - what is the super-regenerative technique;
  - what is the difference between asynchronous and synchronous operating mode;
  - what are the different boxes which form the block diagram of the receiver and how they work.
- in the third chapter I illustrated how, each block of the circuit, has been projected starting from the theory;
- in the forth chapter I wrote down the results I got, and in particular I tried to focus the attention on the main problems that I found building my circuit;
- in the last chapter there is the conclusion.

1.1 Short-range wireless links

The kind of receiver that will be presented in this Master Thesis it is a low power receiver for short-range distance ($1 - 10\,m$) which works in the $24\,GHz$ frequency band. It has an energy efficiency of $3.38\,pJ/bit$, working with a bit-rate of 1 *Gbps*. It is a receiver able to capture and amplify a really fast AM (Amplitude-Modulated) signal that is coming from a pretty near source, that could be installed inside the same room or, if we talk about body area networks, on the human body. In these applications, where there is usually a device which is supplied by a battery, it is fundamental to dissipate a little power, increasing the battery lifetime.

For the marketing area, some important new application fields need to be cited, for example: WiGig short-range WiFi, wireless HDMI and, in the medical field, Wireless Body Area Network. [1][2][3]

In the WiGig area there are two associations that are working on the project: Wireless Gigabit Alliance and Wi-Fi Alliance; and there will be probably necessary at least a couple of years to have this technology available. WiGig will be able to become the new standard for the Wi-Fi connections, transferring data with a bit-rate in a range between 1 $Gbps$ until a maximum of 7 $Gbps$. This means that it will be possible to transfer an high definition video in streaming from a computer to a television without HDMI cable. To make it possible, this two associations are working in a new transmission band of 60 GHz. Nowaday the typical Wi-Fi speed is around 150 $Mbps$ using the standard 802.11n, so it means that with WiGig it will be possible to transmit the same data more than 6 times faster. The major companies that are working in this project are: Broadcom, Cisco, Dell, Intel, Microsoft, NEC, Nvidia, Nokia e Samsung.

Wireless HDMI (High Definition Multimedia Interface) technology is instead available since 2003. HDMI is a digital audio and video interface that is capable to transmit uncompressed streaming data. The wired counterpart connects two digital video and audio components, like DVD player and a High Definition television. Wireless HDMI is just the same thing but without wire. The transmitter is a little black box, the size of a laptop that will likely get smaller as the technology improves. Data are sent from the transmitter through the airwaves to the receiver where the video and audio are decompressed and then sent through the HDMI port to the displaying device. Wireless HDMI transmits data at 3 $Gbps$. The transmitter compresses data with an impression compression standard base on JPEG algorithm technology, which is used for compressing images for a wide variety of uses from medical images to personal pictures. The receiver and transmitter in the wireless HDMI system will not need a straight line of sight. In fact, they can be in different floors or different rooms and still capable of beaming data to each other. Both devices typically must be within 5 m. An UWB adapter can be used to widen that distance up to 31 m.

Finally, another important application for this kind or receiver could be the Wireless Body Area Network (WBAN). This is the application of wearable computing devices. A wireless communication between several miniaturized Body Sensor Units (BSU) and a single Body Central Unit (BCU) worn at the human body. The Body Area Network field is an interdisciplinary area which could allow inexpensive and continuous health monitoring with real-time updates of

medical records via Internet. Implanting very small bio-sensors inside the human body in order to monitor the patients' health status no matter their location. Information are transmitted wirelessly to an external processing unit and this device will instantly transmit all information in real time to the doctors throughout the world. If an emergency is detected, the physicians will immediately inform the patient through the computer system by sending appropriate messages or alarms. The main applications of BANs are expected to appear primarily in the healthcare domain, especially for continuous monitoring and logging vital parameters of patients suffering from chronic diseases such as diabetes, asthma and heart attacks.

1.2 IBM10LP 65 nm CMOS Technology

The technology that has been used to design the super-regenerative receiver is the IBM10LP 65 nm technology.

When a new technology has to be studied for the first time, you do not have a lot of information about its technological parameters, so, the first thing to do is to plot the figures of merit of the CMOS devices, which can give many useful information about the characterization of their performance. Usually, power consumption and band of an amplifier are the two most important items to take in account. Talking about CMOS devices that dissipate a little power and work at high speed, it is always related to the density current which is biasing them. The density current depends by the size of the device (and when the length L is constant, the width W becomes the parameter we need to consider) and by the bias current that is flowing through it. Because of the main task of a CMOS device is to amplify a signal, also what is its maximum transit frequency becomes fundamental. f_T, is the maximum operating frequency where the device can still amplify in current, and it is extrapolated putting the load shorted and finding the value of frequency where the current gain is one. Working at higher frequencies, in fact, the parasitic elements of the device, and in particular C_{gs} and C_{gd}, become relevant; their impedance goes down and this fact kills the gain of the transistor.

For the huge amount of problems that are coming out working at high frequency (24 GHz), and using device with a really short channel (65 nm), it is fundamental to write down a brief description of the equations which try to described these phenomena.

Two phenomena play a key role in the short-channel devices: mobility degradation and velocity saturation [4]. Fig.1.1 represents the motion of an electron inside the channel of a

transistor.

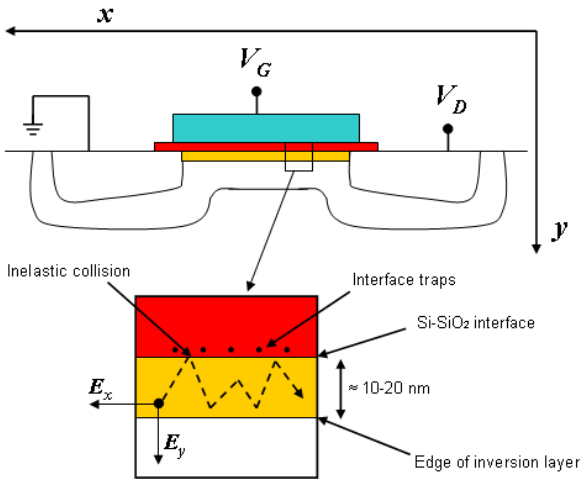


Figure 1.1: Motion of an electron under the influence of lateral field E_y and vertical field E_x.

Mobility Degradation

This effect affects also long-channel transistors, but it is a more serious limitation for short-channel devices. It is related to the x-directed gate oxide fields (the electric field that is orthogonal to the gate, E_x) which is higher in short-channel transistors because the power-supply voltage is not scaled as much as suggested by constant-field scaling when the gate-oxide thickness is reduced. The drain current in a MOSFET is carried by a mobile-charge density Q_n that is moving in a region near the surface under the influence of varying fields. The electrons are scattered by collision with the interface as well as with charged acceptor sites and thermal phonons. It is impossible to write down an exact theory to describe this phenomenon but some approximations have been done and the empirical equation that can represent the mobility degradation for the mosfet is

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^v} \tag{1.1}$$

where μ_0, E_0, and v are all fitting parameters. E_{eff} is, instead, the average x-directed field experienced by all the mobile carriers at the MOS surface. In Fig.1.2 there is the drain-current, I_D, due to the mobility degradation. The dotted line represents the ideal evolution of the current increasing V_G, while the thick line is the real one.

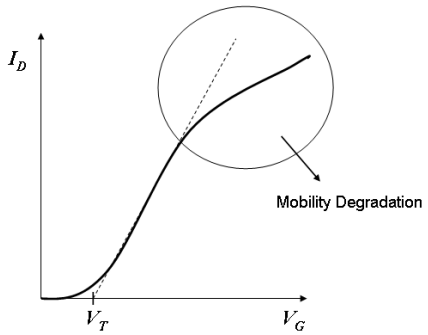


Figure 1.2: $I_D - V_G$ characteristics.

Velocity Saturation

This phenomenon is related to the applied field in the direction of carrier drift (the y-direction for the MOSFET channel, E_y). When high fields are applied, carrier velocities approach a limiting value. At lower fields, the velocity is fit by an equation of the form

$$v = \frac{\mu_{eff} E}{1 + E/E_{sat}} \qquad E < E_{sat} \tag{1.2}$$

while for fields greater than the saturation field E_{sat}, the velocity becomes constant

$$v = v_{sat} \qquad E > E_{sat} \tag{1.3}$$

The parameter E_{sat} is determined by solving for the field at which $v = v_{sat}$ and it becomes

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \tag{1.4}$$

E represents the y-direction field and and it can be also written as

$$E = \frac{V_{DS}}{L} = \frac{V_{GS} - V_T}{L} \tag{1.5}$$

So, taking $\theta = 1/(E_{sat}L)$ for the velocity (1.2) there is the following equation:

$$v = \frac{\mu_{eff} \dfrac{V_{DS}}{L}}{1 + \theta V_{DS}} \tag{1.6}$$

And using this kind of equation inside the common equation of the drain current of a MOSFET, in velocity saturation conditions, I_D can be written as:

$$I_D = \frac{\mu_{eff} C_{ox}}{2} \frac{\frac{V_{GS}-V_T}{L}}{1+\theta(V_{GS}-V_T)} W(V_{GS}-V_T) = \frac{\mu_{eff} C_{ox}}{2} \frac{1}{1+\theta(V_{GS}-V_T)} \frac{W}{L}(V_{GS}-V_T)^2 \quad (1.7)$$

And for the short-channel, where

$$\frac{V_{GS}-V_T}{L} \gg 1 \quad (1.8)$$

I_D becomes, using eq.(1.4) and (1.7)

$$I_D = \frac{\mu_{eff} C_{ox} W}{2}(V_{GS}-V_T)E_{sat} = C_{ox} W (V_{GS}-V_T) v_{sat} \quad (1.9)$$

In velocity saturation, the output current is

- independent of L
- a linear function of $(V_{GS}-V_T)$

In silicon, typical values for the velocity saturation are:

$$\mu_{eff} \sim 0.07 \frac{m^2}{Vs} \qquad E_{sat} \sim 10^6 \frac{V}{m} \qquad v_{sat} \sim 10^5 \frac{m}{s} \quad (1.10)$$

Fig.1.3 illustrates how the velocity saturates increasing the E_y.

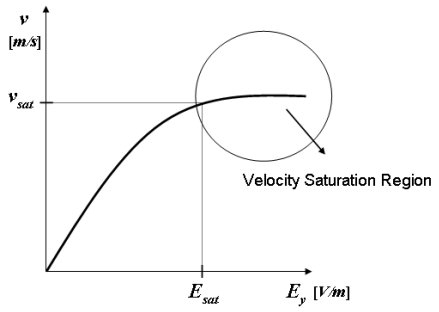


Figure 1.3: Electron velocity vs. E_y.

1.2.1 MOSFET Small-Signal AC Model

[5] To understand how complex a small-signal AC model for a MOSFET becomes, the operating frequency as to be increased, take a look to Fig.1.4 . This model can be considered valid

for frequencies that are below $1\,GHz$; at $24\,GHz$ the model should be even more complex. Comparing with the simplest small-signal AC model, where C_{gs} is the only considered parasitic capacitance, here there are many others that are playing an important role in the transistors performance, in particular: C_{gd}, C_{sb}, C_{gb}, and C_{db}. The last two, it is easy to see, can turn off the

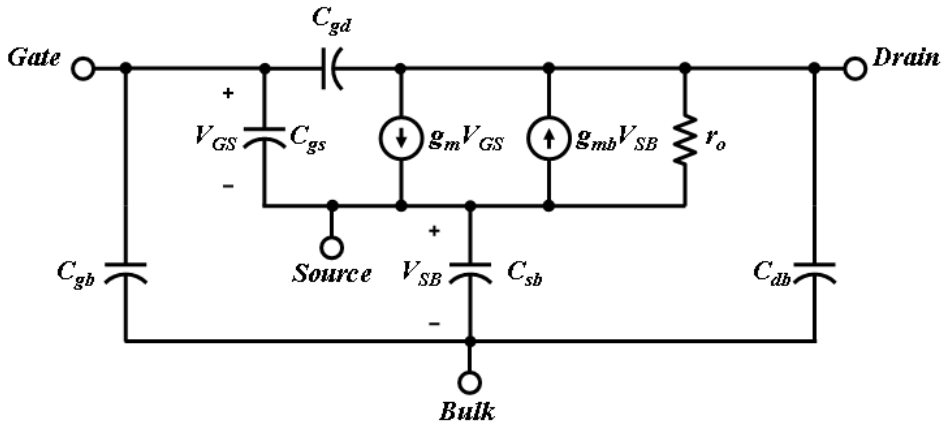


Figure 1.4: MOSFET Small-Signal AC Model below 1 GHz operating frequency.

transistor, taken the gate-voltage and the drain-voltage to zero. C_{sb}, instead, is responsible for the body effect. When $V_{SB} > 0$ the threshold voltage of the device increases and for the same applied V_{GS}, the transconductance g_m gets smaller. This fact is represented adding another transconductance g_{mb} which is opposite to g_m. C_{gd}, at the end, at high frequency, generates a feedback between the output and the input of the transistor. Because of the Miller effect, it can be represented in parallel with C_{gs} with a value equal to $C_{gd}(1 - A_v)$, where A_v in the inverting voltage gain of the transistor. Thus, it becomes responsible, at high frequency, of the increasing of the input capacitance of the transistor. Using the simplified model in Fig.1.5, we obtain for f_T the following expression:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad when \qquad \left|\frac{I_D}{I_{IN}}\right| = 1 \tag{1.11}$$

Starting from eq.(1.9), we know that the transconductance g_m can be calculated as

$$g_m = \frac{dI_D}{dV_{DS}} = WC_{ox}v_{sat} \tag{1.12}$$

Thus, using eq.(1.4) and (1.11) the transit frequency f_T, can be rewritten as

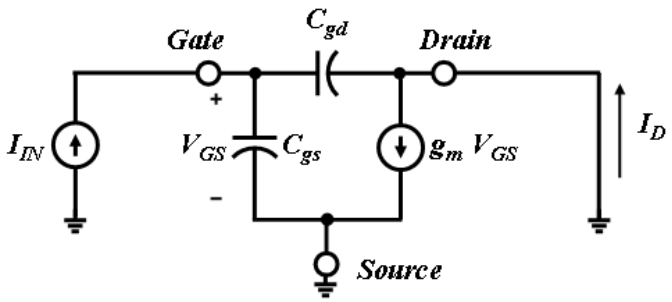


Figure 1.5: Unity Current Gain Frequency, f_T.

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{gs}} = \frac{WC_{ox}v_{sat}}{(2\pi)\left(\frac{2}{3}WLC_{ox}\right)} = \frac{1}{2\pi}\frac{3}{2}\frac{v_{sat}}{L} = \frac{1}{2\pi}\frac{3}{4}\frac{E_{sat}}{L} \tag{1.13}$$

Another important parameter to consider is f_{max} that, in presence of input and output matching for the device, represents the frequency at which the maximum power transfer, G_{max}, is equal to one. It can be shown in eq.(1.14) that:

$$|G_{max}| = 1 \quad \longrightarrow \quad f_{max} \approx \sqrt{\frac{f_T}{8\pi R_{gate} C_{gd}}} \tag{1.14}$$

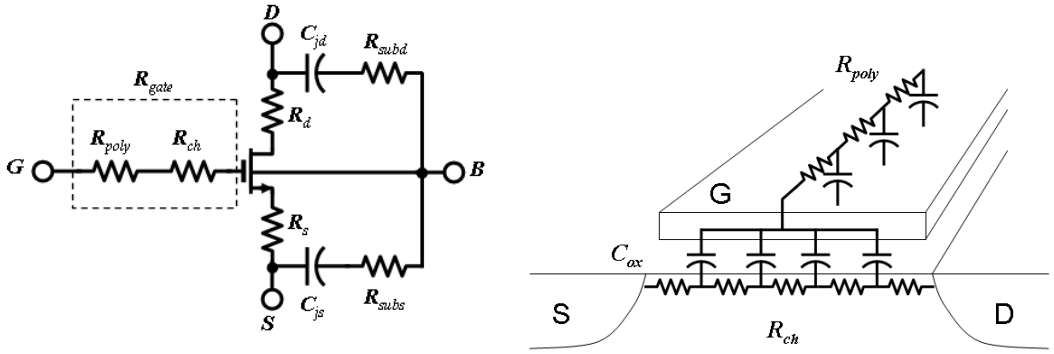
An important element appears inside eq.(1.14), the gate resistance R_{gate}. At low frequency it does not matter, because C_{gs} represents an open-circuit; but working in the RF design, where the parasitic capacitances start to have a fundamental role, also the parasitic resistances come out and have to be considered in the model. Thus, the RF model for the MOSFET becomes the one that is shown in Fig.1.6a. R_{gate} represents the effective gate resistance, and it can be split into two other parasitic resistances, R_{poly} and R_{ch}.

$$R_{gate} = R_{poly} + R_{ch} \tag{1.15}$$

Fig.1.6b shows where these two parasitic resistances come from. R_{poly} is the distributed gate electrode resistance and it can be estimated as

$$R_{poly} = \frac{1}{3}\rho_{poly}\frac{W}{n^2 L} \tag{1.16}$$

where ρ_{poly} is the resistivity of the gate electrode, W and L the dimensions of the device, and n the number of fingers. R_{ch}, instead, is the channel induced gate resistance, and it can be



(a) Model (b) Effective Gate Resistance

Figure 1.6: RF Model for MOSFET

calculated as

$$R_{ch} = \frac{1}{\delta}\left(\frac{V_{Dsat}}{I_{DS}} \parallel \frac{qL}{kT\mu_{eff}WC_{ox}}\right) \tag{1.17}$$

where δ is a fitting parameter which takes in account for distributed effects and it swings between 12 and 15. V_{Dsat} is the drain saturation voltage and it is related to E_{sat} in the following way

$$V_{Dsat} = \frac{E_{sat}L(V_{GS} - V_T)}{E_{sat}L + (V_{GS} - V_T)} \tag{1.18}$$

and it converges to $(V_{GS} - V_T)$ when E_{sat} becomes very large. q is the charge, $1.602 \times 10^{-19}\ C$; k is the Boltzmann's constant, $1.38 \times 10^{-23}\ J/K$, and T is the temperature in Kelvin.

R_s and R_d are, instead, the parasitic resistances of source and drain respectively. Finally, R_{subs} and R_{subd} represent the lumped substrate resistors.

Using the model to simulate the device in Cadence, R_s, R_d and the two R_{sub} are already included. The standard values for this resistances, for this CMOS technology, are usually: $R_s \sim 2\,\Omega$ and $R_{sub} \sim 100\,\Omega$. For the gate resistance instead, sometimes the model does not include it. For example in the IBM10LP technology R_g is not taken in account in the model, and in the simulation it is necessary to add an external resistance, of about $2 - 3\,\Omega$, to consider it. A smart method to verify the presence or the absence of it in the model, is to plot G_{max}. As it is shown in eq.(1.14), if $R_{gate} = 0$, f_{max} goes to infinity, so it means that G_{max} will be always above 1.

An important design rule, to minimize R_{gate} in RF MOSFETs, is to make a multi-finger layout, at the expense of more parasitic capacitance. Typical finger width for $0.25\ \mu m$ device ia about $5\ \mu m$, for $0.13\ \mu m$ device is $2.5\ \mu m$; so, in my project, for $65\ nm$ device I used fingers

1 μm wide. As it is shown in eq.(1.16), R_{poly} scales with $1/n^2$, instead, R_{ch} is independent on n.

Equivalent Circuit Parameters for MOSFET in Terms of Y-Parameters

As, in the previous section, the device is considered when is working in saturation region. Consider the model in Fig.1.4, taking also in account the parasitic resistances, and using the Y-parameters, a new model for the RF MOSFET can be extrapolated, which is shown in Fig.1.7. In the Tab.1.1 there is the list of the 6 equations that can be plotted in Cadence to have an idea of how the 6 device parameters change in the frequency domain.

Input Resistance: $R_{in} = \Re\left\{\frac{1}{Y_{11}}\right\}$	Input Capacitance: $C_{in} = \frac{\partial}{\partial\omega}\left[\frac{1}{\Im\left(\frac{-1}{Y_{11}}\right)}\right]$
Output Resistance: $R_{out} = \frac{1}{\Re(Y_{22})}$	Output Capacitance: $C_{out} = \frac{\partial}{\partial\omega}[\Im(Y_{22})]$
Transconductance: $g_m = \Re(Y_{21})$	Feedback Capacitance: $C_{fb} = \frac{\partial}{\partial\omega}[\Im(-Y_{12})]$

Table 1.1: Circuit Parameters for MOSFET in terms of Y-Parameters

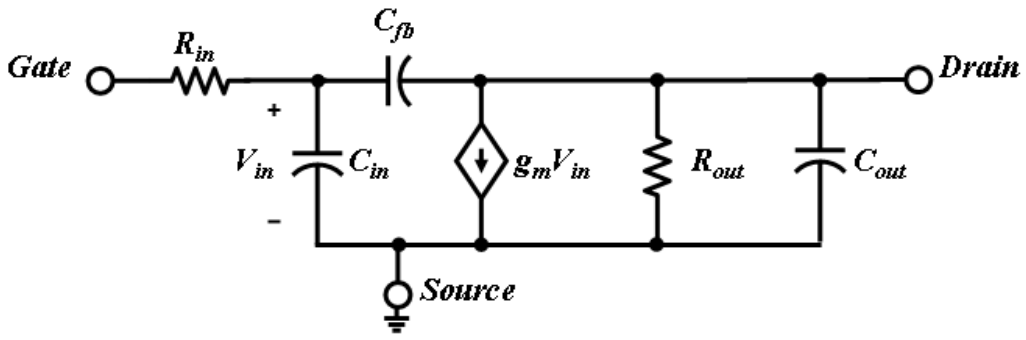


Figure 1.7: MOSFET model in terms of Y-Parameters.

1.2.2 Device characterization for the IBM10LP technology

After this introduction, there is an idea of the huge amount of problems that come out designing a circuit in the radio-frequency domain. At low frequency, in the kHz range, all the parasitic elements are hidden inside the device. They do not play any role in the operating behaviour of the device and so there are a lot of pretty useful formula that can be used. Instead, when the frequency goes up, formula start to have a marginal role, because there are too many phenomena and parasitic elements that come up. At this point it is still important to have some easy formula to relate with, but the simulator becomes fundamental. This is why it is so important to test a device alone, plot some graphs, and do a first characterization of it, before starting the actual project. The same analysis should be done for both N- and P-MOSTFET.

For all the plots that will be shown, a 1 finger device with $W = 1\,\mu m$ and $L = 60\,nm$ is used. With this technique, the current and the density current assume the same value, and so I could plot some important graphs in function of the density current which is the parameter which help to characterize a transistor, and not the current itself. The supply voltage for these testing simulation, and for the project in general it will be $1\,V$. The first plots to draw are I_D vs. V_{GS}, and I_D vs. V_{DS} (Fig.1.12 - 1.13). These plots can show the threshold voltage magnitude is about $V_{th} = 350\,mV$ for both the devices. Using then the circuit configuration in Fig.1.8, other plots are: g_m vs. I_{den} (Fig.1.9), and f_T vs. I_{den} (Fig.1.10), where the density current is $I_{den} = I_x/W$. These two plots help to understand what is the optimal bias current density to use. From Fig.1.9 it is possible to see that curves have a saturation point. There is a "limit" after that g_m becomes insensitive on the density current. It implies that the device is in velocity saturation, so, keeping increasing the drain current, maintaining W constant, g_m will remain constant the same and the device will dissipate more power for nothing (not power efficient). The goal is to work at an I_{den} where $\partial g_m/\partial I_{den} > 1$, and this happens when for the N-MOSFET $I_{den} < 216\,\mu A/\mu m$, and for the P-MOSFET $I_{den} < 123\,\mu A/\mu m$. In Fig.1.14, a zoom-in of g_m vs. I_{den} has been done in the interested region. These two plots has been the most useful for design of the circuit. They are fundamental to decide how much big devices have to be. The equation of g_m in Fig.1.14 can be simplified as

$$g_m = \sqrt{\frac{2\mu_{eff}C_{ox}W}{L}I_x} = W\sqrt{\frac{2\mu_{eff}C_{ox}W}{L}I_{den}} \tag{1.19}$$

i.e. if for a particular I_{den}, $W = 20\,\mu m$, just multiplying 20 times the value of g_m that is mapped

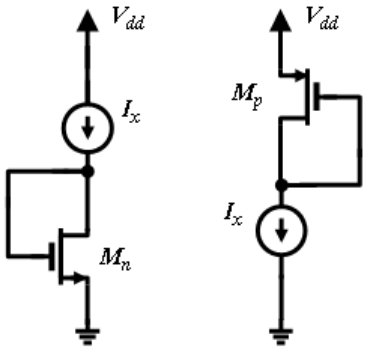


Figure 1.8: Circuit configuration to extrapolate the figures of merit.

in Fig.1.14 permits to obtain the new searched value.

From Fig.1.10, the transit frequency saturates at 175 GHz for the N.MOSFET, and to 125 GHz for the P-MOSFET.

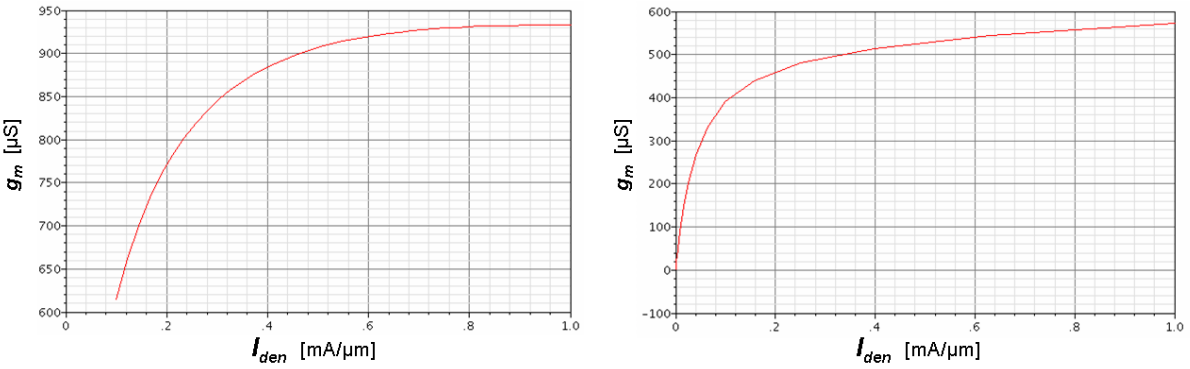
Moreover, knowing I_{den} and g_m, from Fig.1.15, the value of V_{gs} to apply can be extrapolated.

Finally, taking the same devices, and putting $V_{gs} = V_{ds} = 1\,V$, it can be calculated in Cadence the value of each equation, in Table 1.1, assumes at 24 GHz. R_{in} is 0 because, in the IBM10LP model, the gate resistance has not been included. In Table.1.2 there are the results.

Device	R_{out}	C_{in}	C_{fb}	C_{out}	g_m
N-MOSFET	5.94 $K\Omega$	0.88 fF	0.22 fF	0.51 fF	895.4 μS
P-MOSFET	8.31 $K\Omega$	0.84 fF	0.25 fF	0.56 fF	468.3 μS

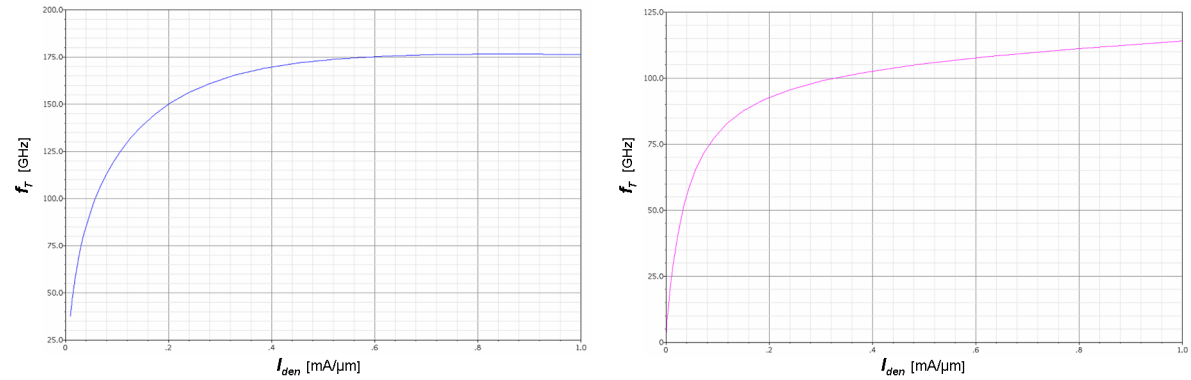
Table 1.2: Circuit Parameters to include in Fig.1.7 for IBM10LP technology, at 24 GHz

The last plot that is useful to see is plotted in Fig.1.11. It shows that when the frequency is smaller than 100 GHz, for both the devices, g_m maintains a constant value. So, during the design, the DC value for g_m, given by Cadence can be trusted, because it is pretty similar to the g_m value at 24 GHz.



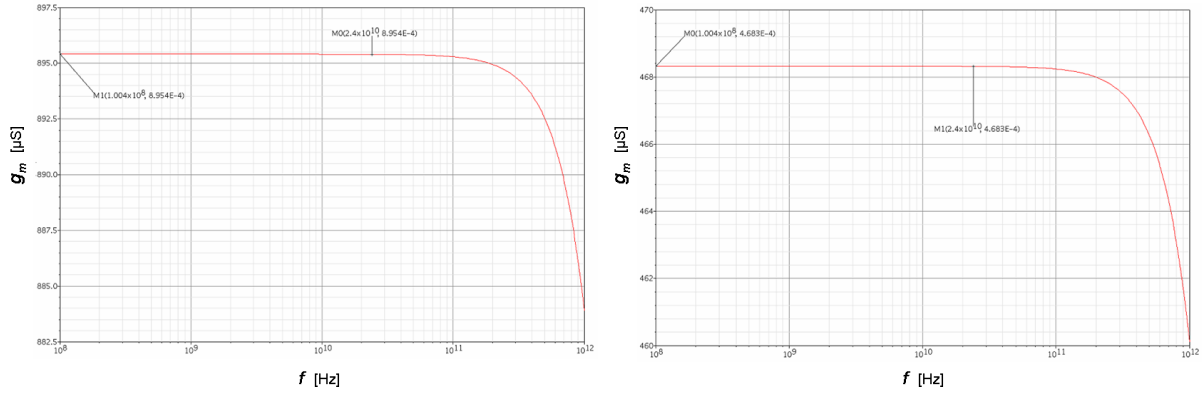
(a) N-MOSFET (b) P-MOSFET

Figure 1.9: g_m vs. I_{den}



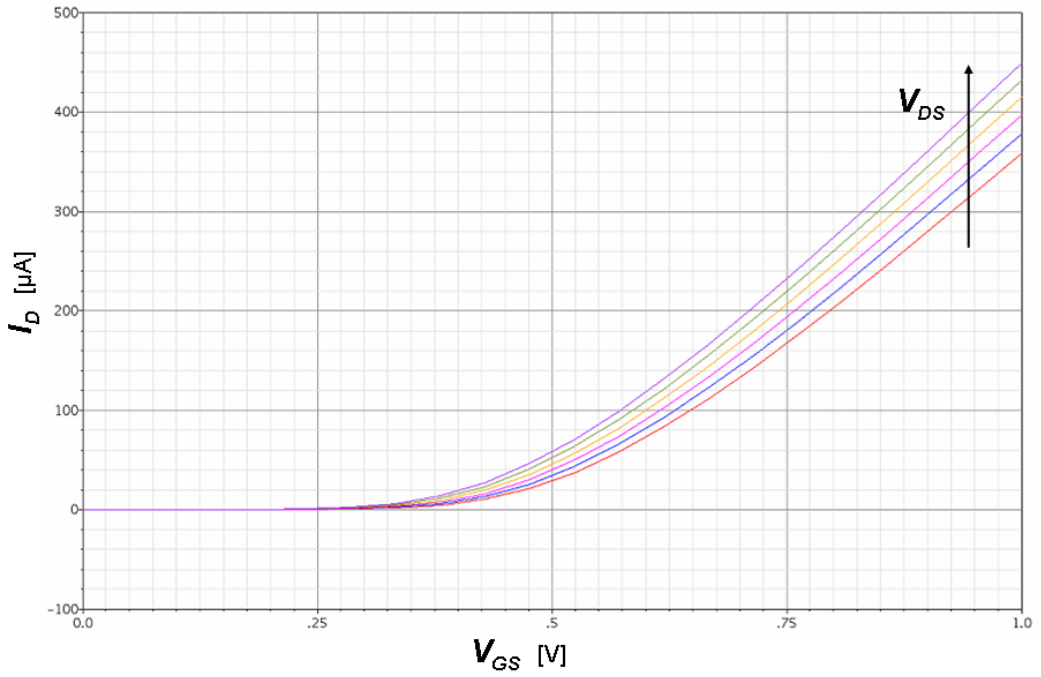
(a) N-MOSFET (b) P-MOSFET

Figure 1.10: f_T vs. I_{den}

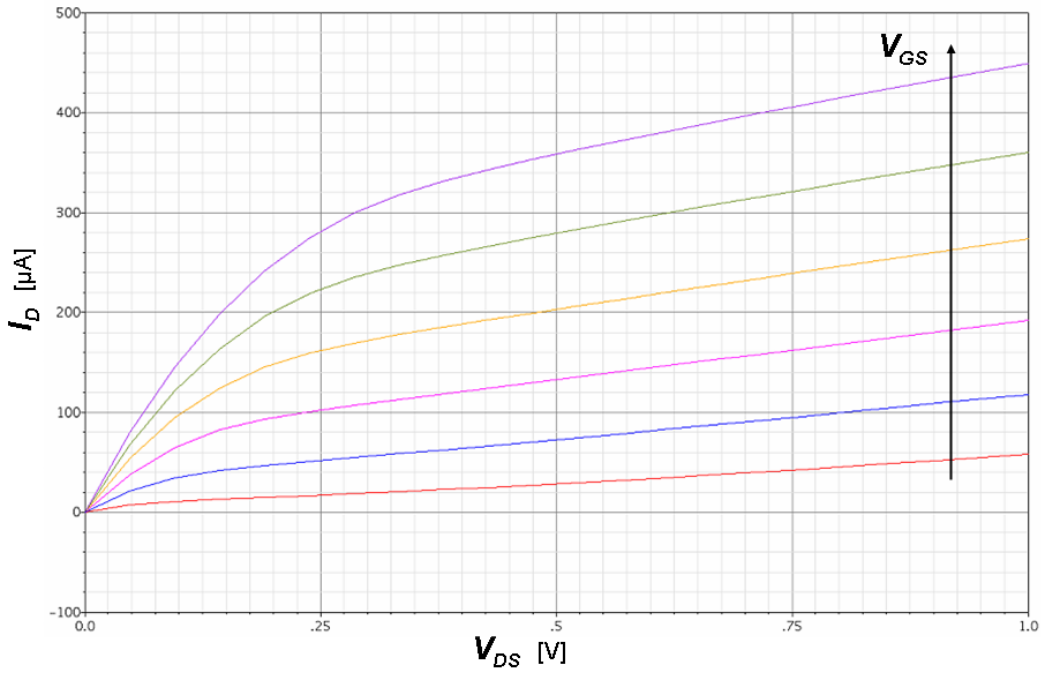


(a) N-MOSFET (b) P-MOSFET

Figure 1.11: g_m vs. Frequency, $V_{GS} = V_{DS} = 1V$

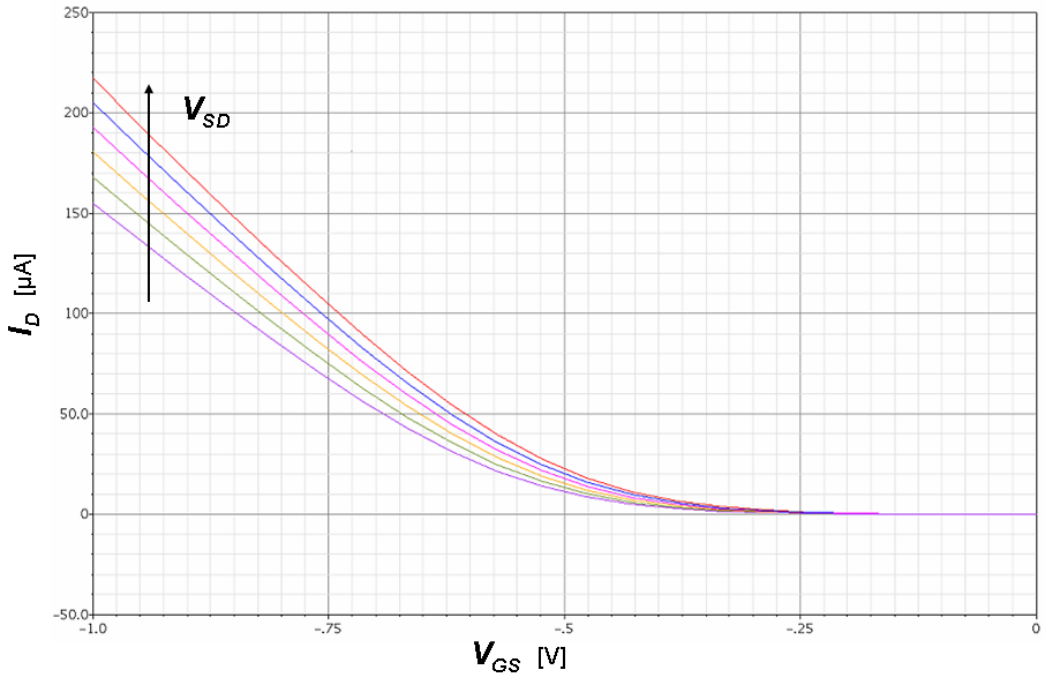


(a) I_D vs.V_{gs}

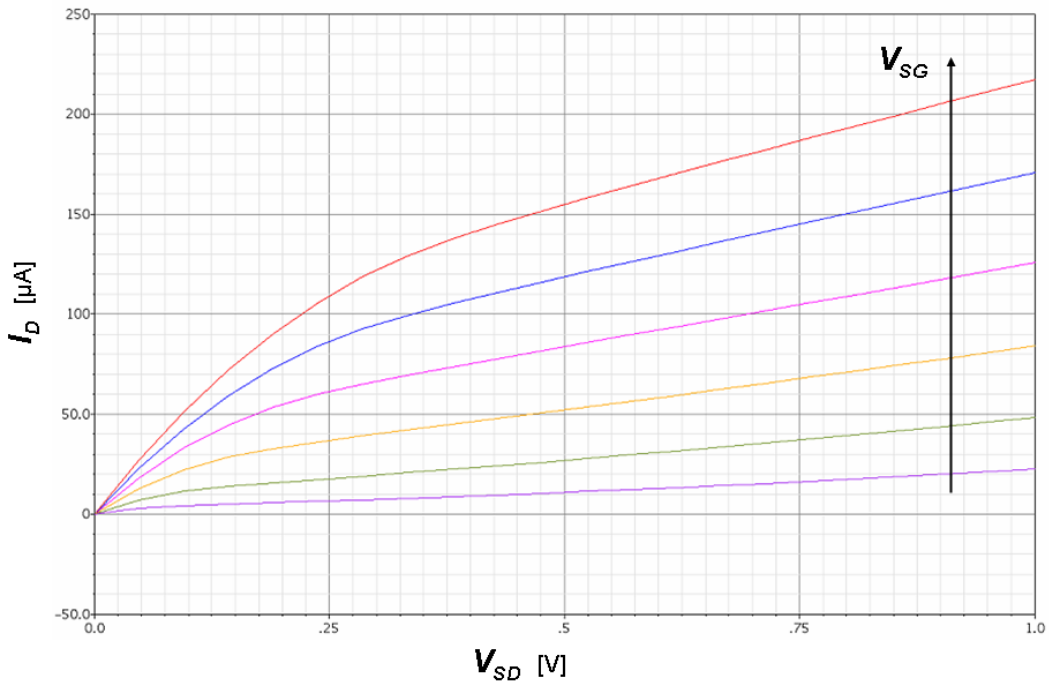


(b) I_D vs.V_{ds}

Figure 1.12: N-MOSFET: a) I_D vs. V_{GS} with $V_{DS} \in [0.5V,\ 1V]$ step $0.1V$; b) I_D vs. V_{DS} with $V_{GS} \in [0.5V,\ 1V]$ step $0.1V$.

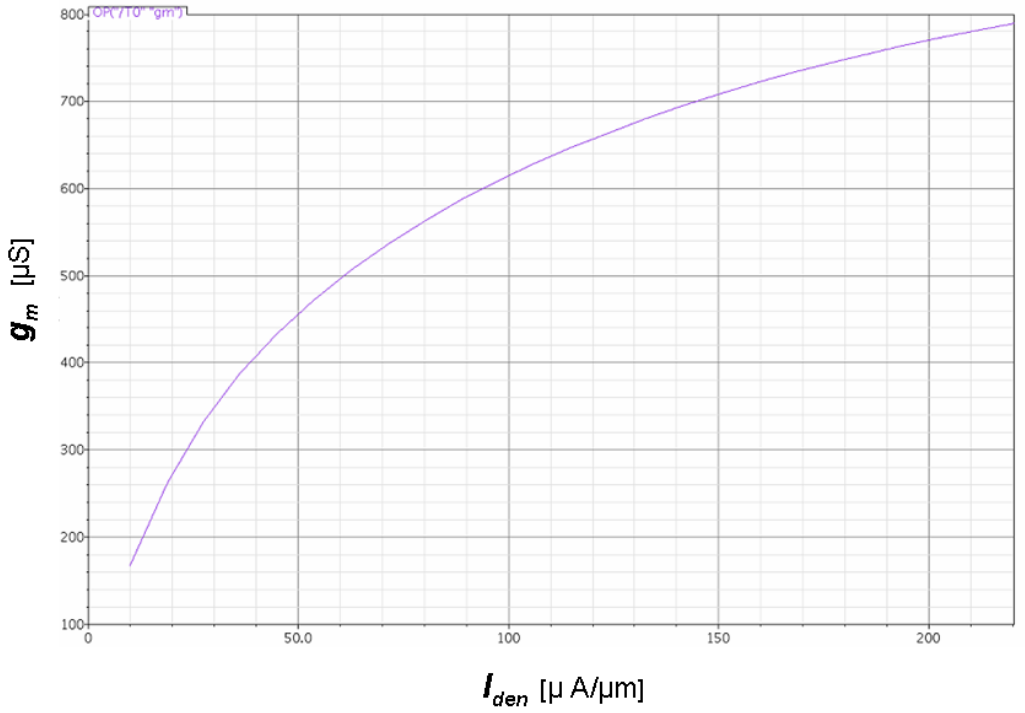


(a) I_D vs.V_{gs}

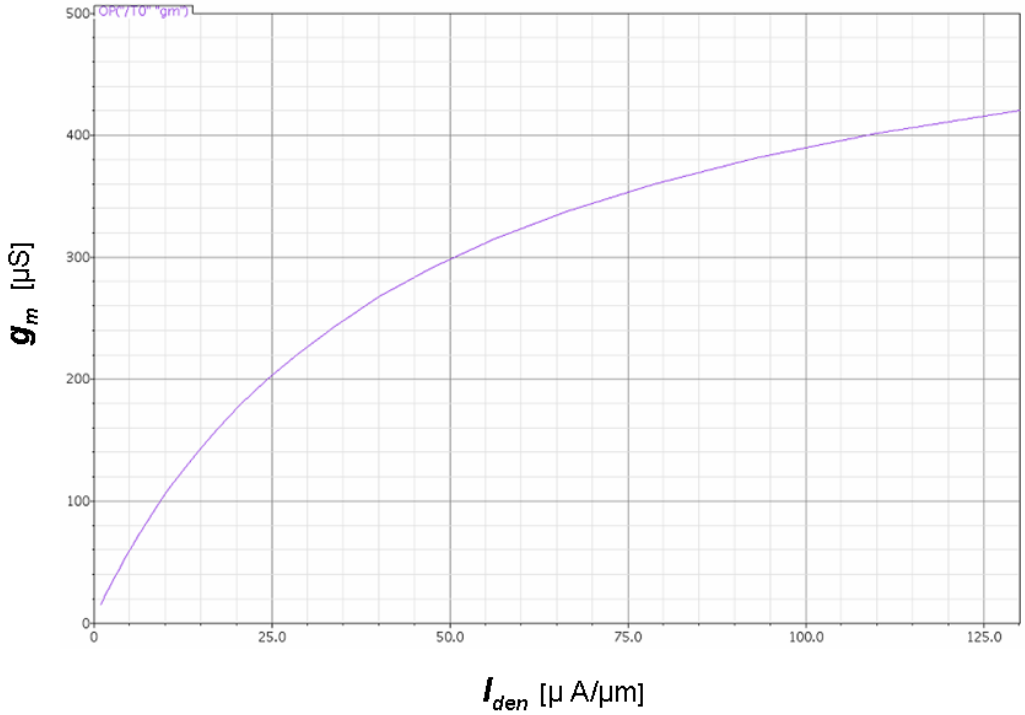


(b) I_D vs.V_{sd}

Figure 1.13: P-MOSFET: a) I_D vs. V_{GS} with $V_{SD} \in [0.5V,\ 1V]$ step $0.1V$; b) I_D vs. V_{SD} with $V_{SG} \in [0.5V,\ 1V]$ step $0.1V$.

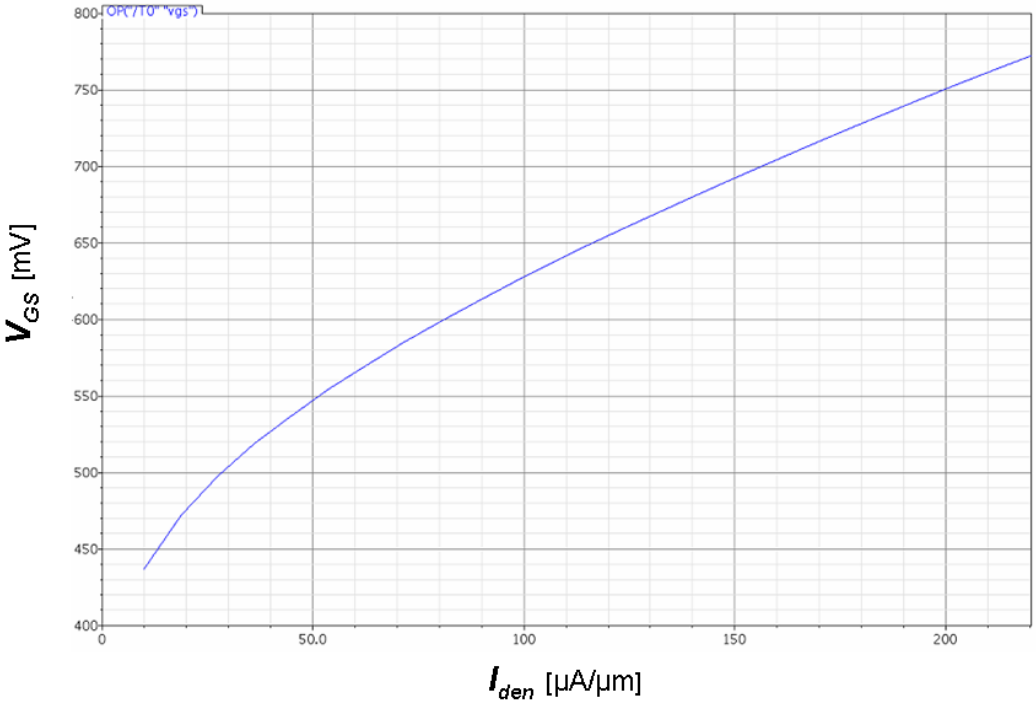


(a) N-MOSFET

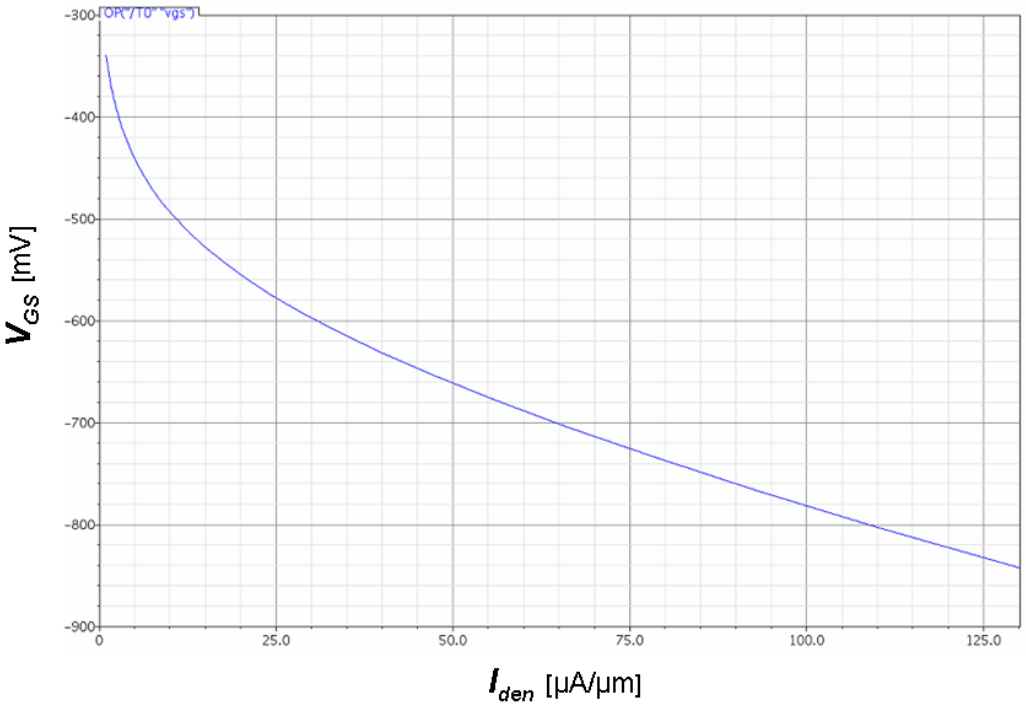


(b) P-MOSFET

Figure 1.14: g_m vs. I_{den} - zoom in



(a) N-MOSFET



(b) P-MOSFET

Figure 1.15: V_{gs} vs. I_{den}

Chapter 2

Theory and System Architecture Design

2.1 Super-regenerative receiver (SRR)

[9][13] Integrated Circuits (IC) designers are favoured by the fact that the incremental cost of a transistor is essentially zero. This has given liberty with a large number of devices that are prevailing today. Not a long time ago when the economics of circuit design were fundamentally based on the number of device counts, often the designer was restricted by the relatively expensive active device to try to get blood from a stone. It is amazing that in the early 1920s, Edwin Armstrong devised a super-regenerative receiver circuit using few components that trade lot of gain for bandwidth, contrary to the conventional wisdom that gain and bandwidth should trade off more or less the directly. The number reduction of device components is not only cost-effective, but also improves reliability.

The characteristics of the super-regenerative receiver to generate large-signal gain at very low bias currents and the ability to operate above the cut-off frequency (f_T) of the RF device make it attractive and the preferred architecture for integrated ultra-low power wireless receiver.

Fig.2.1 depicts a 1940's 500 MHz SRR, which is bulky and require manual calibration, but the circuit operates above the device ft, which was an astonishing accomplishments in those days.

The phenomenon of the super-regenerative detection has been the main focus research, and it is still an open issue despite significant gains in practical experience and modern CAD tools

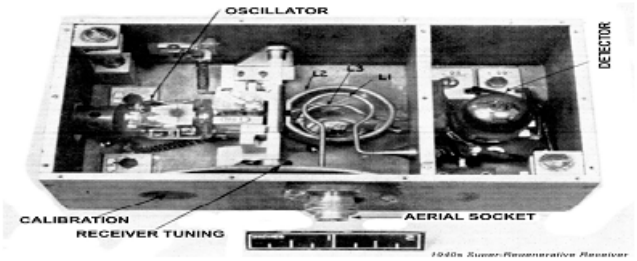


Figure 2.1: A 1940's 500-MHz Super-regenerative receiver

for design. The SRR circuits uses just a few components, and its basic design is simple, but detailed analysis is complex, due to the time varying and non-linear characteristics of the receiver circuit. Super-regenerative receivers have been used for many decades, and are still manufactured in large quantities for short-distance data exchange. Although an SRR has advantages of high gain, simplicity, low cost, low power consumption and constant demodulated output over a wide range of input signal levels, it has also drawbacks of inherent frequency instability.

Fig.2.2 shows the typical block diagram of a super-regenerative receiver, which consists of a matching network, an isolation amplifier, an amplifier with time varying loop gain and a bandpass feedback network forming a regenerative oscillator.

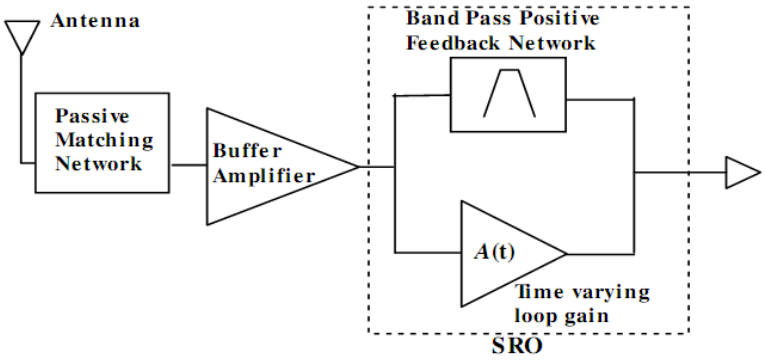


Figure 2.2: A typical block diagram of super-regenerative receiver (SRR).

The buffer amplifier between the antenna and the SRO (super-regenerative oscillator) performs the following functions: it reduces the RF leakage of the oscillation signal to the antenna, it provides an input match to the antenna via the passive matching network, and it injects the RF input signal current into the oscillator tank without adding significant loading to the SRO. The time varying nature of the loop gain is designed such that the SRO transconductance pe-

riodically exceeds the critical values of the transistor transconductance g_m necessary to induce instability. Consequently, the SRO periodically starts up and shuts off. The periodic shut down of the SRO is called "quenching".

The start-up time of a SRO (the time from enabling the oscillator until it reaches its saturation voltage Vsro) can be described by:

$$t_{rise} = \tau_{rise} \log \left[\frac{V_{sro}}{\sqrt{\overline{v_n^2}}} \right] \tag{2.1}$$

Where τ is the time constant of the exponentially increasing oscillation envelope, V_{sro} is the zero-peak RF voltage of the saturated oscillator, and v_n is the thermal noise generated due to the resonator tank and active device.

From (2.1), the start-up time of the SRO is dependent on the instantaneous noise in the resonator, when the SRO loop gain is unity (at the onset oscillation).

Fig.2.3 exhibits the start up of the SRO in presence of thermal noise. Observing that the start up time is very sensitive to low-level signals in the SRO tank, it becomes obvious that this mechanism can be used to amplify any RF input signal.

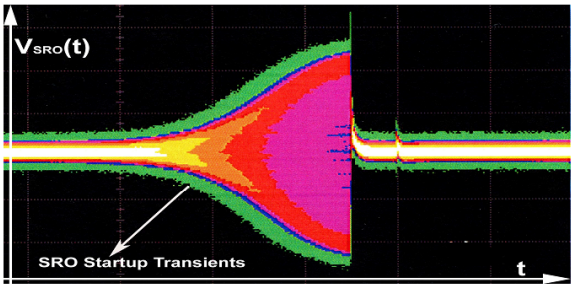


Figure 2.3: A typical start-up transient of SRO circuit in presence of thermal noise.

Although the conceptual block diagram of the SRR is of a compact size, power efficient and uses small device counts, the design methodology is not well defined, which leads to a "cut and try" approach, based on results obtained from the simplified model. Moreover, the compact size of the SRR implies a small antenna, with poor efficiency that degrades the sensitivity of the receiver. To achieve reasonably good performance, a high sensitivity is required that conflicts with the circuit design requirements for low power consumption.

Fig.2.4 shows a typical SRR circuit that consists of the following basic modules: antenna, LNA (low noise amplifier), SRO (super-regenerative oscillator), QO (Quench oscillator), ED

(envelope detector), and LPF (low-pass filter). The working principle is based on a repeated build up and decay of the self-oscillations in a SRO whose frequency is near or equal to the RF signal frequency intercepted by antenna. As illustrated, the RF signal is intercepted by

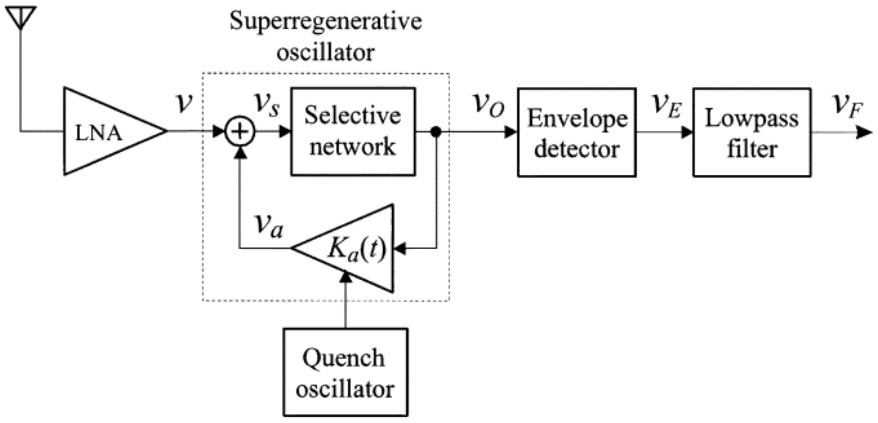


Figure 2.4: Detailed block diagram of the SRR.

the antenna and injected through the LNA into the SRO module. [10] The main objective of the LNA module is to facilitate the impedance matching with the antenna, guaranteeing the maximum power transfer into the SRO module. The LNA module optimize the noise figure, and in addiction, provides isolation, minimizing the power injected back into the antenna due to the building-up of the self-oscillations by SRO module. The gain of the SRO is periodically varied by QO signal (f_q) for sampling the RF signal at the point of maximum sensitivity. The start-up time of the SRO's self-oscillations is proportional to the amplitude and frequency of the RF signal received through the antenna. The $K_a(t)$ loop is used to stabilize the amplitude of the v_E by adjusting the bias current thereby enhancing the receiver's input dynamic range. Finally, the demodulation is performed by rectifying the self-oscillation voltage v_0 and then filtering the envelope voltage v_E by the BPF.

2.2 Low-Noise Amplifier (LNA)

2.2.1 Simplified analysis

[5][11][12] The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages. Hence, low noise figure and high gain are critical LNA performance parameters; in portable applications, low power dissipation is also essential. LNA design involves trade-off among linearity, input matching and power dissipation. The basic common-source LNA circuit is widely used in CMOS RF IC design and the CS-LNA configuration is currently popular because of its superior noise performance; i.e., the inductive degeneration is ideally noiseless and the RF input signal is pre-amplified by the input-matching series resonant network. The complete schematic of the 24-GHz LNA that I used in my project is depicted in Fig.2.5. The method employed here is the inductive

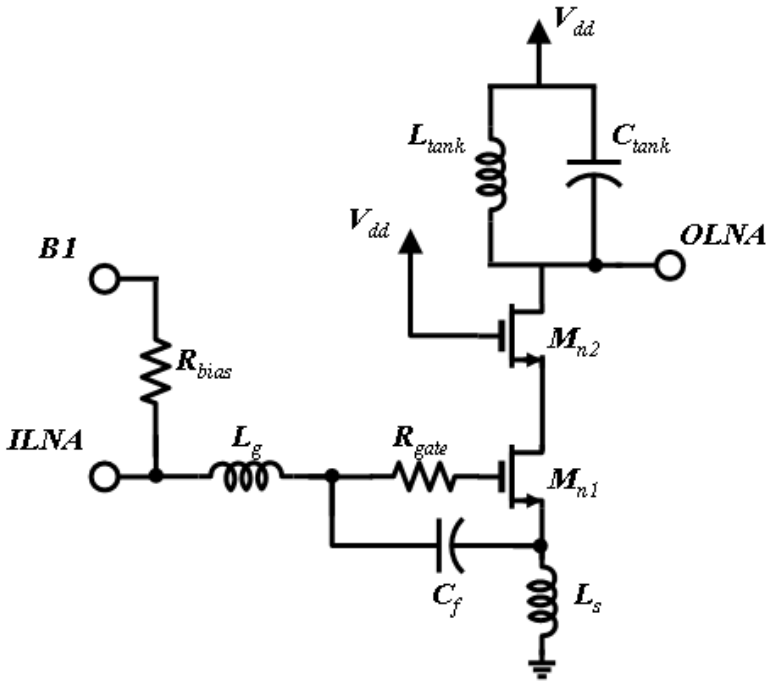


Figure 2.5: Complete schematic of the 24-GHz LNA.

source degeneration. L_g, L_s and L_{tank} are implemented with an internal series resistance which takes in account losses in the component. R_{gate} instead is a resistance that has been added during the simulation in Cadence to take in account losses in the gate of the mosfet M_{n1}, whose were not considered in the IBM model. Adding C_f in shunt to the parasitic C_{gs} of M_{n1} gives more degrees of freedom to design the LNA input matching network. C_{tank}, at the same time,

let me adjust the resonant frequency of the LNA without having to use a huge inductor L_{tank}. R_{bias} is a big resistance which has to make the output impedance of the bias circuit really high and neglectable in the LNA input matching network design. Cascoding M_{n2} is used to reduce the intersection of the tuned output with the tuned input, and to reduce the effect of the gate-drain capacitance of M_{n1}. L_g, L_s and C_{gs} are chosen to provide the desired input resistance. Obviously at the input and at the output of the LNA two blocking capacitances, C_{BL1} and C_{BL2}, will be added. Their value will be the maximum value available for the technology that will be used. In this way they will not influence the input matching network in the operating frequency.

Input Matching

The simplified version of the LNA small-signal model is shown in Fig.2.6. It will help to extrapolate some basic and useful formulas for input matching and noise. To simplify the analysis,

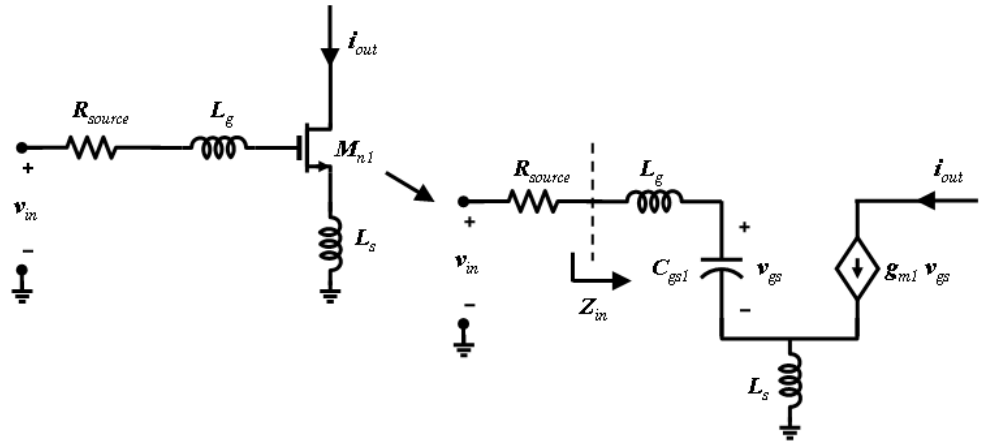


Figure 2.6: Narrowband LNA with inductive source degeneration.

we can consider a device model that includes only a transconductance and a gate-source capacitance, and where L_g and L_s do not contain any parasitic resistance. In this case, it is not hard to show that the input impedance can be written as:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs1}} + \frac{g_{m1}}{C_{gs1}}L_s \approx s(L_s + L_g) + \frac{1}{sC_{gs1}} + \omega_T L_s \tag{2.2}$$

Hence, the input impedance is that of a series RLC network, with a resistive term that is directly proportional to the inductance value. And in the context of low-noise amplifiers, we actually seek to enhance this effect, creating a resistive input impedance without the noise of

real resistors. However, this approach has the undesirable side effect of degrading high-frequency gain. Considering this model, Z_{in} is specified by choosing L_s and L_g to resonate with C_{gs1} at the operating frequency with $(g_{m1}/C_{gs1})L_s$ set to 50Ω. The associated quality factor is:

$$Q = \frac{1}{2\omega_0 C_{gs1} R_{source}} > 1 \tag{2.3}$$

Gain

The effective trasconductance of the LNA stage is:

$$G_m = g_{m1}Q = \frac{g_{m1}}{\omega_0 C_{gs1}(R_{source} + \omega_T L_s)} = \frac{\omega_T}{\omega_0 R_{source}\left(1 + \frac{\omega_T L_s}{R_s}\right)} \tag{2.4}$$

and when the input is matched to R_s, it becomes:

$$G_m = \frac{1}{2R_{source}}\left(\frac{\omega_T}{\omega_0}\right) = \frac{1}{2R_{source}}\left(\frac{f_T}{f_0}\right) \tag{2.5}$$

In RF systems R_{source} is usually equal to 50Ω. Note the G_m depends only on the ratio of f_T to f_0 and it is independent of the MOSFET small-signal trasconductance g_{m1}. The transit frequency f_T is usually $5 - 10$ times bigger than the signal frequency f_0, therefore, the common-source LNA provides high gain.
The final gain for the LNA results:

$$A_v \approx g_{m1} Q R_{tank} \tag{2.6}$$

Noise Figure

The major advantage of the common-source amplifier with inductive degeneration is that the resistive input impedance is noiseless, unlike other topologies where a noisy resistor is added in the signal path to create a 50Ω terminating impedance. The noise factor of this topology is:

$$F = \frac{\overline{i^2_{n,out}}}{\overline{i^2_{R_{source}}}} = 1 + \frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega_0}{\omega_T}\right)\left[1 + \frac{\delta\alpha^2}{5\gamma}(1+Q^2) + 2\left|c\right|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right] \tag{2.7}$$

With:

$$\overline{i^2_{R_{source}}} = \frac{4kT\Delta f}{R_{source}} \tag{2.8}$$

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \tag{2.9}$$

$$\overline{i_g^2} = 4kT\delta g_g\Delta f \tag{2.10}$$

$$Q = \frac{1}{\omega_0 C_{gs1} R_{source}} \tag{2.11}$$

$$\overline{i_g i_d^*} = c\sqrt{\overline{i_g^2}\,\overline{i_d^2}} \tag{2.12}$$

where $c = j0.395$, α, γ, and δ are bias-dependent parameters, and ω_0 and ω_T are the operating and unity current gain frequencies, respectively. From (2.7), noise in the LNA is formed by

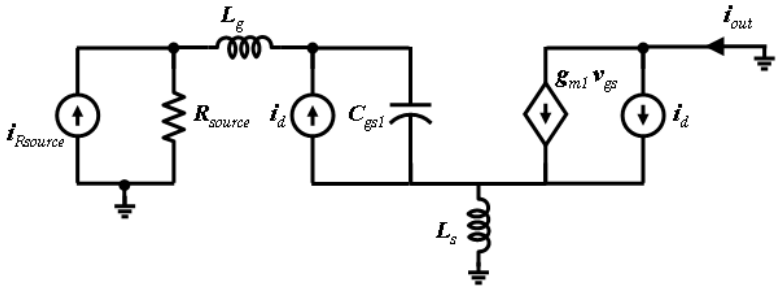


Figure 2.7: Small-signal circuit for noise figure analysis of CS-LNA.

three factors: channel noise, gate noise and correlated noise. Increasing Q of the input resonant circuit reduces the contribution of channel noise. In contrast, gate noise is enhanced by the Q factor. Hence, there exists an optimum Q that minimizes the noise figure. For a given overdrive and f_T, the optimum values are:

$$F_{min} = 1 + \frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right)\frac{2\delta\alpha^2}{5\gamma}Q_{opt} \tag{2.13}$$

$$Q_{opt} = \sqrt{1 + 2\,|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2}} \tag{2.14}$$

To achieve a high f_T, minimum channel length is used. Knowing the optimum Q value for minimum noise figure, the optimum width of the device is then easily determined.

2.2.2 Accurate analysis

If we consider Fig.2.5 and we also take in account the parasitic resistance of L_s and L_g the formula for the input matching becomes a little bit different. The following equation is the one

I used to design the LNA.

$$Z_{in} = s(L_s + L_g) + \frac{1}{s(C_{gs1} + C_f)}(1 + g_{m1}R_s) + \frac{g_{m1}}{C_{gs1} + C_f}L_s + R_s + R_g + R_{gate} \tag{2.15}$$

where R_s and R_g are the parasitic series resistances of L_s and L_g respectively.

2.3 Super-regenerative oscillator (SRO)

2.3.1 Super-regenerative Modes

[13] Fig.2.8 shows the two typical operation modes for the SRR: detector output in the linear mode, detector output in the logarithmic mode and RF input signal. The linear mode is

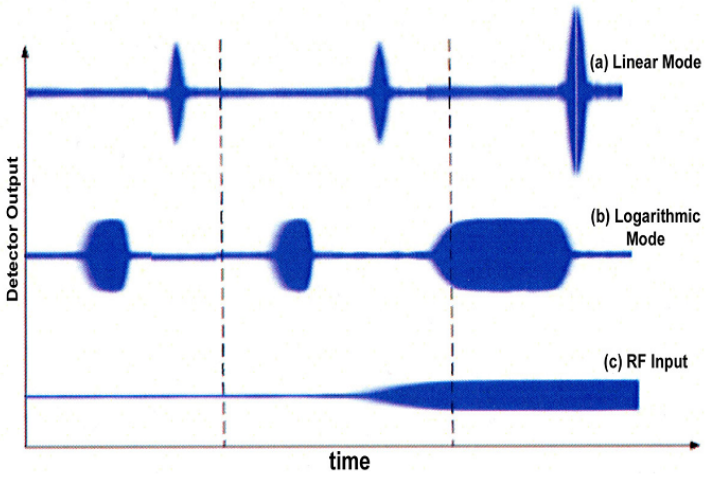


Figure 2.8: Super-regenerative Modes.

described by a linear relationship between the amplitude of the RF input signal and the amplitude of the demodulated output. In this mode, SRO does not reach its steady state during the quench period, due to a high quench frequency and/or a low start-up current. However, the typical operation is made of a combination of the both modes; hence, it is difficult o predict an exact mode of SRO operation. In the linear mode, the oscillation amplitude is measured before the oscillator reaches saturation providing a high independent gain.

As depicted in the linear mode, the samples envelope is much larger in the presence of the RF input signal. Notice that, in this mode, the oscillator is disable after the amplitude is measured. Thus, in the linear mode, the oscillator never reaches saturation.

A logarithmic mode is described by a logarithmic relationship between the amplitude of the RF input signal and the amplitude of the demodulated output characterizes the logarithmic mode. In this mode the SRO reaches its steady state amplitude at each quench cycle, due to a low frequency and/or a high start-up current; therefore, a reduction in the dynamic range of the demodulated output is due to the logarithmic compression of the signal. In the logarithmic mode, however, the oscillator is allowed to saturate during each cycle. The detector circuitry

senses the area under the oscillation envelope, providing a signal dependent gain. As shown for the logarithmic mode, the area under the saturated oscillation envelope is increased in the presence of an RF input, resulting from the decrease oscillator start-up time in this condition.

So one important difference between the two modes is that the logarithmic mode provides an inherent automatic gain control.

2.3.2 Analytical Model of the super-regenerative receiver for the Linear Mode

[9][10] Before starting with the detailed description of the theory, which will try to give a mathematical explanation of the super-regenerative phenomenon, it is convenient to anticipate the parameters that will be used (Fig.2.9 and 2.10 can help to visualize the shape of the functions that are going to be listed):

1. **Feedforward Gain**: Factor K_0 is the gain provided by the selective network at the resonance frequency. It represents the open-loop gain of the super-regenerative oscillator, i.e., the one provided when the feedback amplifier remains inactive.

2. **Sensitivity Curve**: $s(t)$ is a normalized function that, for $t = 0$, takes the maximum value of unity, and decreases toward zero as time separates from $t = 0$. The decrease of this curve is quite fast, due to its exponential dependence on t. In practical receivers, the value of this function becomes practically null in an environment relatively close to the origin, $t = 0$. The shape of $s(t)$ is determined mainly by the environment of the zero-crossing of $\varsigma(t)$. A slow transition will provide a wide sensitivity curve, whereas a fast one will generate a narrow curve.

   Both the regenerative gain and the frequency response depend on the product $p_c(t)s(t)$. In this way, the sensitivity curve acts as a function which weights the incoming envelope $p_c(t)$; the values of $p_c(t)$ near $t = 0$ will be taken into account, whereas those close to t_a t_b will be irrelevant. The instant $t = 0$ can be considered the instant of maximum sensitivity.

3. **Regenerative Gain**: K_r is also called the *slope* or *step factor* in the literature, depending on the type of quench applied. It takes in account the contribution of differential portions of the input signal envelope, each one weighted by the sensitivity curve. This gain depends on the product $p_c(t)s(t)$. If $p_c(t)$ or $s(t)$ is narrow, the regenerative gain will be small.

Instead, if both of those are wide, the regenerative gain will be large.

4. **Super-regenerative Gain**: K_s is related with the exponential growth of the oscillation and is the most significant amplification factor. It is determined by the area enclosed by the negative portion of the damping function.

5. **Frequency Response**: It is the normalized Fourier transform of $p_c(t)s(t)$ shifted toward the oscillation frequency ω_0. If both, $p_c(t)$ and $s(t)$, are wide, the bandwidth of the selectivity curve of the receiver will be small; if $p_c(t)$ or $s(t)$ is narrow, the bandwidth will be large.

6. **Normalized Oscillation Envelope**: Finally, the normalized oscillation envelope $p(t)$ is determined mainly by the evolution of the damping function close to t_b.

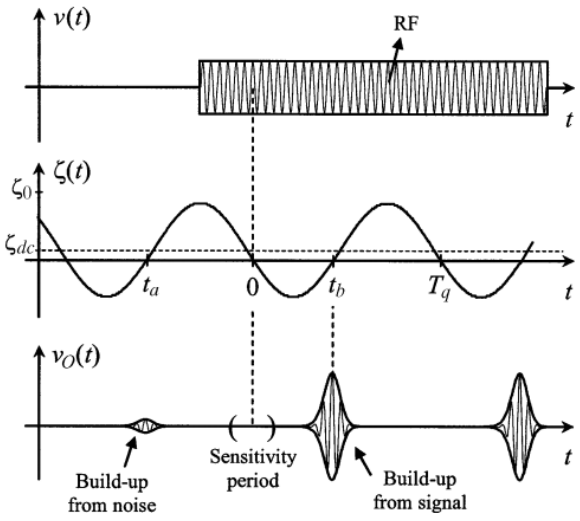


Figure 2.9: RF input signal, damping function, and SRO output.

The following analysis considers the block diagram previously presented in Fig.2.4. The feedback amplifier module shows a variable gain $K_a(t)$, which is controlled by the quench signal QO, that forces the system to be alternatively stable and unstable. The transfer function of the selective network (SN) can be described by

$$G(s) = K_0 \left[\frac{2\varsigma_0 \omega_0 s}{s^2 + 2\varsigma_0 \omega_0 s + \omega_0^2} \right] \tag{2.16}$$

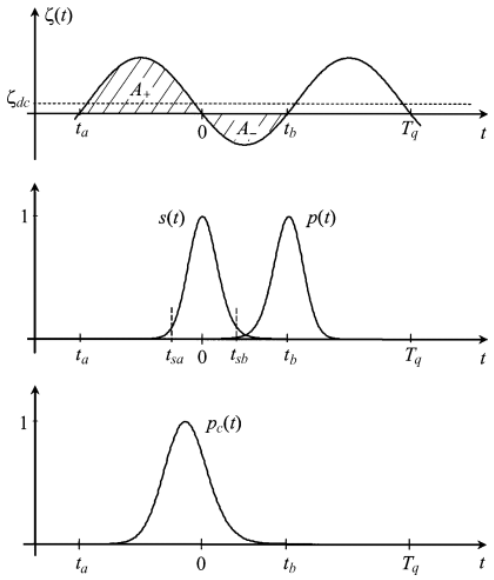


Figure 2.10: Damping function $\varsigma(t)$, sensitive curves $s(t)$, normalized envelope of the output pulse $p(t)$, and normalize envelope of the input signal $p_c(t)$.

From Equation (2.16), the characteristic differential equation of the SR can be given by

$$\frac{\partial^2 v_0(t)}{\partial t^2} + 2\varsigma_0\omega_0\frac{\partial v_0(t)}{\partial t} + \omega_0^2 v_0(t) = 2K_0\varsigma_0\omega_0\frac{\partial v_s(t)}{\partial t} \tag{2.17}$$

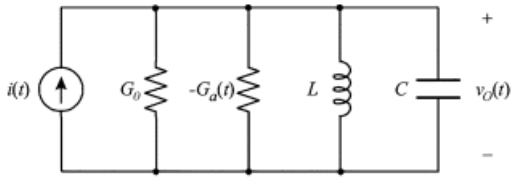
where ς_0 is the quiescent damping factor and K_0 is the maximum amplification. Fig.2.11 shows the typical parallel and series equivalent representation of the SRO. The feedback network can be described as $v_s(t) = v(t)K_a(t)v_0(t)$, which can be represented by the linear, time-variant, second-order differential equation

$$\frac{\partial^2 v_0(t)}{\partial t^2} + 2\varsigma_0\omega_0\frac{\partial v_0(t)}{\partial t} + \omega_0^2 v_0(t) = 2K_0\varsigma_0\omega_0\left[\frac{\partial v(t)}{\partial t} + K_a(t)\frac{\partial v_0(t)}{\partial t} + v_0(t)\frac{\partial K_a(t)}{\partial t}\right] \tag{2.18}$$

$$\frac{\partial^2 v_0(t)}{\partial t^2} + 2\varsigma_0\omega_0\frac{\partial v_0(t)}{\partial t} + \omega_0^2 v_0(t) = 2K_0\varsigma_0\omega_0\frac{\partial v(t)}{\partial t} \quad for \quad \frac{\partial K_a(t)}{\partial t} \to 0 \tag{2.19}$$

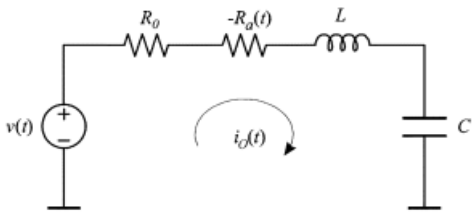
where $\varsigma(t)$ is the instantaneous damping factor of the closed-loop system that can be characterized as

$$\varsigma(t) = \varsigma_0\left[1 - K_0K_a(t)\right] \tag{2.20}$$



Block diagram	v	v_O	K_0	ζ_0	ω_0	$K_a(t)$
Circuit	i	v_O	$\frac{1}{G_0}$	$\frac{G_0}{2C\omega_0}$	$\frac{1}{\sqrt{LC}}$	$G_a(t)$

(a)



Block diagram	v	v_O	K_0	ζ_0	ω_0	$K_a(t)$
Circuit	v	i_O	$\frac{1}{R_0}$	$\frac{R_0}{2L\omega_0}$	$\frac{1}{\sqrt{LC}}$	$R_a(t)$

Figure 2.11: Parallel and Series RLC circuits.

The instantaneous quality factor $Q(t)$ is

$$Q(t) = \frac{1}{2\varsigma(t)} \tag{2.21}$$

The quench oscillator generates an instantaneous damping factor, or damping function, $\varsigma(t)$, that is periodic. This function is composed of successive quench cycles. A new quench cycle starts when the damping function changes to positive ($t = t_a$), which extinguishes any oscillation present in the oscillator. After it changes to negative ($t = 0$), the oscillation builds up from the injected signal $v(t)$ and achieves the maximum amplitude when $\varsigma(t)$ once again changes to positive ($t = t_b$). Citing results which have been obtained in the article [10], the receiver seems especially sensitive to the input signal in a certain environment at the instant $t = 0$. The behaviour of the receiver is mainly determined by the characteristics of the damping function (e.g., its shape, repetition frequency and mean value). Since $\varsigma(t)$ gives global information about

the system's performance, it is a better descriptor than just the feedback gain $K_a(t)$. In practice, $K_a(t)$ is adjusted in order to obtain the desired $\varsigma(t)$.

The general solution of (2.18) can be broken down into the sum of the general solution of the homogeneous equation plus a particular solution of the complete equation, according to

$$v_o(t) = v_{oh}(t) + v_{op}(t) \tag{2.22}$$

where $v_{oh}(t)$ is the free (or natural) response, which may exist even though no excitation is present, whereas $v_{op}(t)$ represents the forced response generated by the excitation.
Skipping the complex calculation and in order to obtain compact expressions that are easier to interpret, several parameters and functions that have been used in the literature to describe the operation of the receiver are introduced:

1. Super-regenerative gain:

$$K_s(t) = e^{-\omega_0 \int_0^{t_b} \varsigma(\lambda) d\lambda} \tag{2.23}$$

2. Normalized envelope of the SRO output:

$$p(t) = e^{-\omega_0 \int_{t_b}^{t} \varsigma(\lambda) d\lambda} \tag{2.24}$$

3. Sensitivity curve:

$$s(t) = e^{\omega_0 \int_0^{t} \varsigma(\lambda) d\lambda} \tag{2.25}$$

All of these functions exhibit an exponential dependence on the damping function $\varsigma(t)$.
The typical input signal $v(t)$ of the SRO can be given in a single quench interval as

$$v(t) = V_m p_c(t) \cos\left[\omega_0 t + \phi\right] + n(t) \tag{2.26}$$

where V_m is the peak amplitude, $p_c(t)$ is the normalized envelope of the SRO input signal, $n(t)$ is the additive Gaussian noise generated by the active devices of the receiver circuit (described by the autocorrelation function $R_n(\tau) = [\eta/2]\,\delta(t)$ with the power spectral density $G_n(f) = \eta/2$). The SRO output can be described by:

- the general solution of the homogeneous differential equation

$$v_{oh}(t) = V_h p_c(t) \cos(\omega_0 t + \phi_h) \tag{2.27}$$

  where V_h and ϕ_h are the magnitude and the phase, respectively;

- and the particular solution of the complete equation becomes

$$v_{op}(t) = 2\varsigma_0 K_0 K_s p_c(t) \int_{t_0}^{t} \dot{v}(\tau) s(\tau) \sin \omega_0 (t-\tau) d\tau \tag{2.28}$$

  where ς_0 is the quiescent damping factor, $s(t)$ is the sensitivity curve, K_0 is the maximum amplification and K_s is the super-regenerative gain. The above expression apply to any value of t, but we are interested in the values of $s(t)$ in the interval (t_a, t_b). Note that the maximum value of expression (2.25) within this interval equals unity and that this value is achieved when $t = 0$. Considering, instead, $p(t)$, expression (2.24) shows that the maximum value of unity is achieved when $t = t_b$. Fig.2.10 shows the typical shapes of $s(t)$ and $p(t)$ under sinusoidal quench.

The noise output n_0 can be given by

$$n_0(t) = 2\varsigma_0 K_0 K_s p_c(t) \int_{t_0}^{t} n(\tau) s(\tau) \sin \omega_0 (t-\tau) d\tau \tag{2.29}$$

From Equations (2.26) to (2.29) the signal to noise ratio (S/N) at the SRO output can be given as

$$[SNR]_0 = \left[\frac{S}{N}\right]_{output} = \frac{E_c}{\eta} \frac{\left[\int_{t_a}^{t_b} p_c(\tau) s(\tau) d\tau\right]^2}{\int_{t_a}^{t_b} p_c^2(\tau) \int_{t_a}^{t_b} s^2(\tau) d\tau} \tag{2.30}$$

where E_c is the average chip energy.
From Equation (2.30) the SNR of the SRO can be optimized using Schwarz's inequality as

$$\frac{\left[\int_{t_a}^{t_b} p_c(\tau) s(\tau) d\tau\right]^2}{\int_{t_a}^{t_b} p_c^2(\tau) \int_{t_a}^{t_b} s^2(\tau) d\tau} \leq 1 \tag{2.31}$$

From Equation (2.30) and (2.31), $[SNR]_{0,opt}$ can be given by

$$[SNR]_0 = \frac{E_c}{\eta} \quad for \quad p_c(t) = s(t) \tag{2.32}$$

Response to an RF Pulse

Next, the system response to a single RF pulse is going to be presented. For sake of simplicity, noise will be neglected in the study. Fig.2.10 helps to understand this section.

The RF pulse is applied within the limits of a single quench cycle, given by the interval (t_a, t_b), and expressed as

$$v(t) = V p_c(t) \cos(\omega t + \phi) \tag{2.33}$$

where p_c is the normalized pulse envelope and V its peak amplitude. p_c is assumed to be zero beyond the cycle limits defined by t_a and t_b. Furthermore, there is no free response coming from previous quench cycles when the current cycle starts, and so $v_{oh}(t) = 0$ and $v_o(t) = v_{op}(t)$, using expression (2.28), we obtain that the response $v_{op}(t)$ is determined by the derivative of the excitation, whose expression is

$$\dot{v}(t) = V \left[\dot{p}_c(t) \cos(\omega t + \phi) - p_c(t)\omega \sin(\omega t + \phi)\right] \tag{2.34}$$

This expression can be approximated by

$$\dot{v}(t) \approx -V p_c(t)\omega \sin(\omega t + \phi) \tag{2.35}$$

when $p_c(t)$ varies slowly in comparison with the RF oscillation ($|\dot{p}(t)| \ll p(t)\omega$).
Taking $v_{oh}(t) = 0$ and replacing (2.35) in (2.28) and making some consideration to simplify the expression, we can write that

$$v_o(t) \approx V K_0 K_s \varsigma_0 \omega p(t) \times \int_{t_a}^{t} p_c(\tau) s(\tau) \cos((\omega - \omega_0)\tau + \omega_0 t + \phi) d\tau \tag{2.36}$$

The sensitivity curves usually decreases rapidly as time separates from the origin, $t = 0$, reaching negligible values that fall outside the interval defined by (t_{sa}, t_{sb}), which can be defined as the sensitive period. This means that the influence of the input signal is small outside the specified interval. Assuming that $s(t)$ is small at the end of the quench period, it has an effect on both the initial values of the envelope and the super-regenerative gain. In particular

$$s(t_a) = p(0) = e^{\omega_0 \int_0^{t_b} \varsigma(\lambda) d\lambda} = \frac{1}{K_s} \ll 1 \tag{2.37}$$

Therefore, a small value for the sensitivity curve at the end of the quench cycle implies small values for the output envelope near the origin and large super-regenerative gains. Consider that the sensitive period ends for all practical purpose when the amplitude of the oscillation is still small, it is possible to replace t by t_b in the integration limits of (2.36), yielding

$$v_o(t) = VK_0K_s\varsigma_0\omega p(t)\int_{t_a}^{t_b} p_c(\tau)s(\tau)\cos((\omega-\omega_0)\tau+\omega_0 t+\phi)d\tau \tag{2.38}$$

And this equation is valid only after the practical end of the sensitivity period, when $t > t_{sb}$; otherwise, t must be kept instead of t_b. Expression (2.38) shows that, in the linear mode, the output of the oscillator is proportional to the peak amplitude of the input signal, and that the forced response has the form of the free response after the end of the sensitivity period.

Response to a Pulse when the carrier is Tuned to the Resonance Frequency

When the receiver is tuned to the receiver frequency, then the solution becomes

$$v_o(t) = VK_0K_s\varsigma_0\omega_0 p(t)\left[\int_{t_a}^{t_b} p_c(\tau)s(\tau)d\tau\right]\cos((\omega_0 t+\phi) \tag{2.39}$$

and it shows that in addiction to K_0 and K_s, a new amplification factor appears. This factor is the regenerative gain

$$K_r = \varsigma_0\omega_0\int_{t_a}^{t_b} p_c(\tau)s(\tau)d\tau \tag{2.40}$$

This gain takes into account the area of the envelope of the received pulse weighted by the sensitivity curve. A pulse the concentrates its energy around the peak of the sensitivity curve will have a regenerative gain greater than that of a more spread pulse. Thus, the new expression for the tuned input is

$$v_o(t) = VK_0K_rK_s p(t)\cos(\omega_0 t+\phi) \tag{2.41}$$

This expression allows the peak amplification K, defined as the ratio between the peak values of the input and the output oscillation, to be obtained. Thus

$$K = K_0K_rK_s \tag{2.42}$$

The output is then reduced to the simple expression

$$v_o(t) = VKp(t)\cos(\omega_0 t + \phi) \tag{2.43}$$

2.3.3 Synchronous Operation of the Receiver

[8] Taking always in account Fig.2.9 and keep working on equation (2.25), the sensitive curve $s(t)$ can be also write as

$$s(t) = e^{\omega_0 \int_0^t \varsigma(\lambda)d\lambda} \approx e^{-\frac{1}{2}\left(\frac{t}{\sigma_s}\right)^2} \tag{2.44}$$

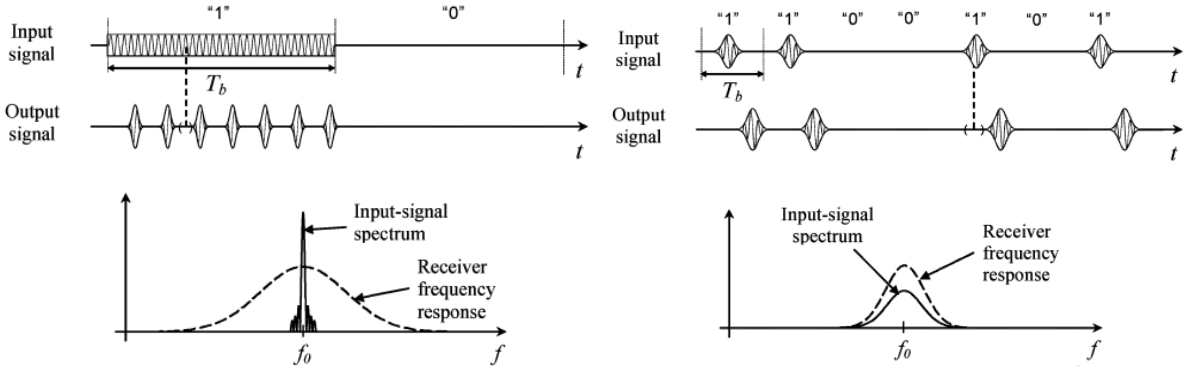
Indeed, when the slope of $\varsigma(t)$ is finite, $s(t)$ can be approximated by a Gaussian function, whose standard deviation σ_s is considerably smaller than the quench period (sinusoidal quench). Consequently, from eq.(2.40) and (2.42), we can see that the receiver is more sensitive to the input signal at $t = 0$, which is called sensitivity period. This point confirms the behaviour of the SRO as a sampling device. The RF bandwidth of the receiver is proven to be inversely proportional to σ_s, and it can be expresses as

$$\Delta f_{-3dB} = \frac{\sqrt{\ln 2}}{\pi}\frac{1}{\sigma_s}. \tag{2.45}$$

Fig.2.12a represents the conventional linear mode operation with a narrowband on-off keying (OOK) modulated input signal. This technique is adopted when the SRO is asynchronously quenched. Indeed, when input data and quench signal are not synchronized the quench samples several times during each bit period T_b to satisfy the Nyquist criterion so that the information can be retrieved by low-pass filtering the baseband bit samples. It means that if there is not any kind of synchronization between the received signal and the quench signal, we will need a quench able to detect more samples for each bit to observe the presence of a single bit. So, the quench frequency f_q should be more than 4 times bigger than the data-bit rate. In Fig.2.12a we can also observe that the sensitivity period is much shorter than the bit period, so the resulting RF bandwidth is much greater than the modulation bandwidth.

Another way to work is, instead, shown in Fig. 2.12b. When the SRO is quenched synchronously with the received signal, with a circuit configuration proposed in Fig. 2.13, we can get a single sample for each bit pulse. This means that the quench frequency equals the bit frequency. The duration of the sample bit is closer to that of the sensitivity period, and so the bandwidth of the modulated signal and that of the receiver become similar. The block diagram

of the receiver in Fig. 2.13 incorporated a PLL that controls the quench voltage-controlled oscillator (VCO) to ensure bit sampling is properly carried out. The output of the envelope detector gives the error signal, which is passed through a baseband amplifier (BBA) and a loop filter. Fig.2.14 shows the normalized envelope of the received bit pulse and the sensitivity curve of



(a) Asynchronous receiver: several samples per bit (b) Synchronous receiver: one sample per bit

Figure 2.12: SRO input and output signals with OOK modulation.

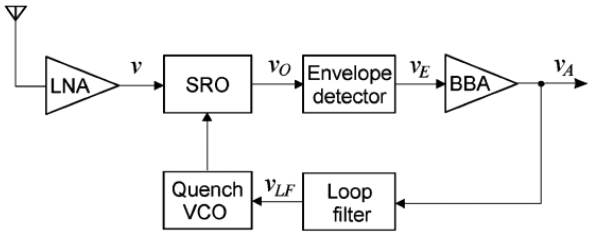


Figure 2.13: Block diagram of the synchronous super-regenerative receiver.

the SRO under normal operation. After the acquisition of the bit, the loop goes to center the sensitive period of the SRO on the ascending flanks of the received bit pulses. Thus, the phase variation of the received pulse results in an amplitude variation at the loop-filter output that tends to correct the error δ, that is shown in Fig.2.14.

2.4 Current-Reuse CMOS Differential LC-VCO

[6][16][17] Fig.2.15 shows a comparison between a conventional NMOS-based differential LC-VCO (2.15a) and the proposed current-reuse differential LC-VCO (2.15b). As compared to the complementary cross-coupled CMOS VCO, the circuit structure of the current-reused oscillator is asymmetrical. The negative conductances are provided by the cross connected pairs of

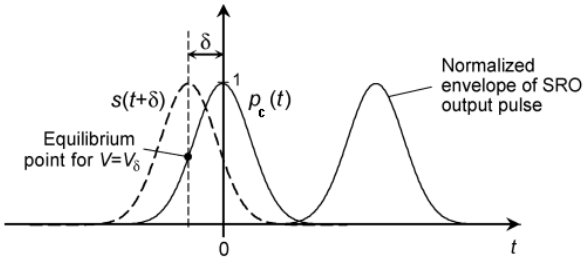
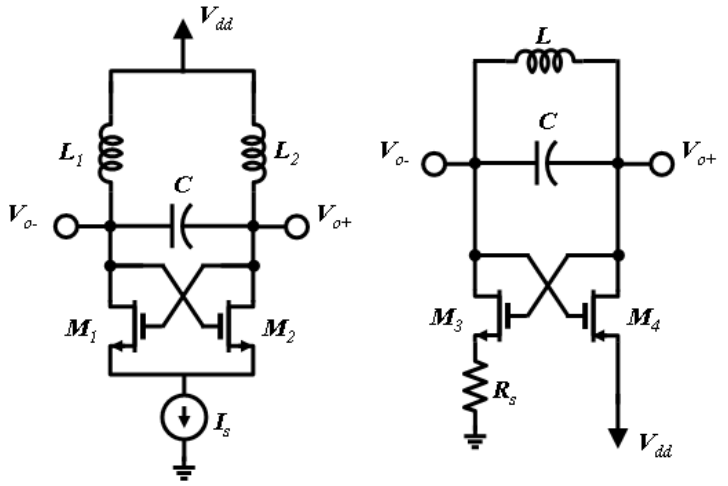


Figure 2.14: Normalized envelope of the input bit pulse $p_c(t)$, shifted sensitivity curve of the SRO $s(t+\delta)$, and normalized envelope of the SRO output oscillation.

transistors, M_1 and M_2 in the first case, and, M_3 and M_4 in the second case, to compensate the losses in the LC-tanks. In the conventional LC-VCO configuration, two N-MOSFETs or two P-MOSFETs can be used to form the cross-couple, and when the oscillation starts the two devices are alternatively ON and OFF. In the current-reuse oscillator, instead, the cross connected pair is formed by an N-MOSFET and P-MOSFET, and during the unstable phase they turn both ON and OFF at the same time. This configuration reduces power dissipation to half that of conventional topologies. In fact, in Fig.2.15a, for the whole oscillation period the bias current I_s is flowing alternatively in both branches; instead, Fig.2.16 shows that the bias current is going through the oscillator just in the first-half period. Thus, the series stacking of N- and P-MOSFET allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance.

To explain the operation of the current-reuse VCO for $R_s = 0$, Fig.2.16 shows the schematic and corresponding large-signal equivalent circuits during each half period of operation. In Fig.2.16, $C_x = C/2 + C_{px}$ and $C_y = C/2 + C_{py}$, where C_{px} and C_{py} represent the parasitic capacitances at nodes X and Y, respectively. As shown in the figure during the first half-period, the transistors M_3 and M_4 are ON and the current from V_{DD} to ground through the tuning inductor L. During the second half-period, the transistors are OFF and the current flows in the opposite direction through the capacitors C_x and C_y. During the first half-period of oscillation, the devices operate in the triode mode near the peak of the voltage swing. In this case, the voltage swing is limited by the supply voltage. Therefore, the oscillator can operate in a voltage-supply-limited mode. However, during the second half-period, the voltage swing across the inductor L is not limited and can lead to a voltage swing greater than the supply voltage. Due to the large amount of current during the first half period, the voltage-waveform results distorted. This is way it is important to add a resistor (R_s) in order to solves this problem. R_s controls the DC current as



(a) (b)

Figure 2.15: Differential LC-VCO: (a) conventional, (b) current-reuse.

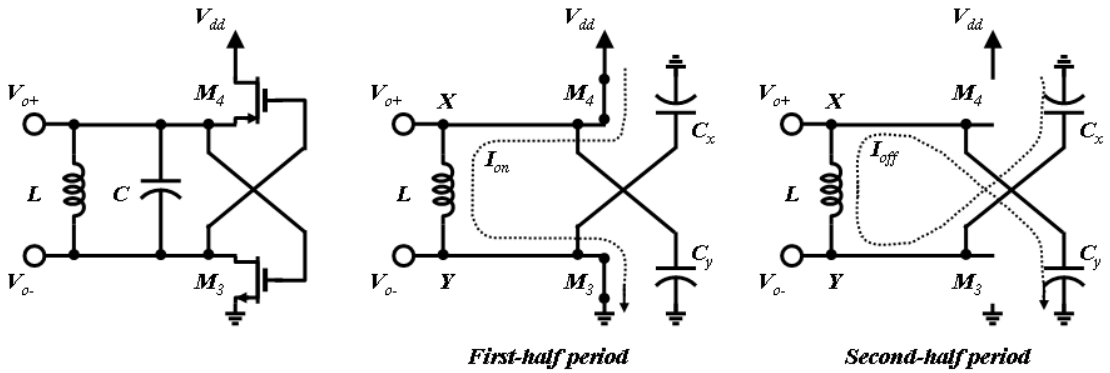


Figure 2.16: Proposed VCO operations with $R_s = 0$ during each half period.

well as the peak dynamic current of the proposed VCO. Therefore, using the correct value of R_s, the proposed VCO can operate in a current-limited mode, rather than the voltage-limited mode. In the current-limited mode, the voltage swing symmetric during the two half periods. In Fig.2.17, the output voltage swing of the two different operation modes is shown. Another advantage of the current-reuse configuration is that, there is not a common source node, and the transistors switch ON and OFF at the same time. Therefore, this VCO is inherently immune to the phase noise degradation caused by second harmonic terms at the common source node. In the convention differential VCO, instead, the phase noise can be degraded significantly by the noise near the second harmonic. Moreover, the P-MOS transistor M_4, in the cross connected pair helps to reduce the phase noise due to lower flicker noise and hot carrier effects.

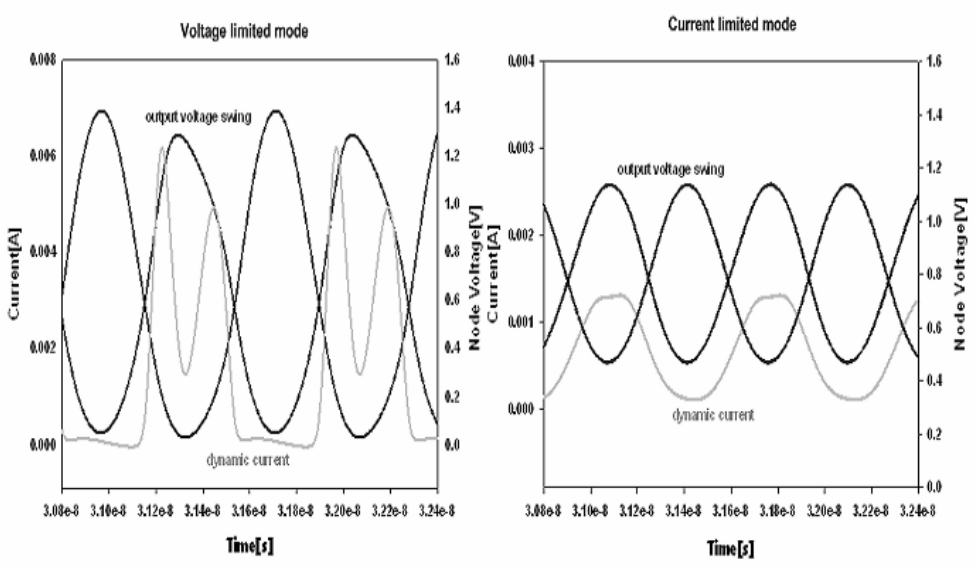


Figure 2.17: Differential output voltage and dynamic current waveforms: voltage limited mode ($R_s = 0$) and current limited mode ($R_s \neq 0$).

Obviously, R_s can be replaced by another active device, N-MOSFET or P-MOSFET, driven by the variable signal. In this way R_s could become a variable resistance.

2.4.1 Simplified Model of the Negative Resistance Oscillator

In Fig.2.18 there is the SRO that has been used in the project, and in Fig.2.19 there is a representation of the passive network, where real and parasitic elements are taken in account.

To design the SRO I decided to extrapolate a model for the cross-coupled differential pair in such a way to determine the right value of the components in the tank to synthesize the negative resistance. Two models will be presented: a simplified one, typical for a conventional differential LC-VCO, and a more accurate one, more appropriate for the current-reuse version, where there the devices are non symmetric.

In Fig.2.19, L_{sro} and C_{sro} represent the integrated inductance and capacitance of the tank. R_{SL_sro} is the parasitic series resistance of L_{sro}. C_{g_ns1} and C_{d_ns1} are the gate and the drain parasitic capacitance of M_{ns1}. C_{g_ps1} and C_{d_ps1} are, instead, the gate and the drain parasitic capacitance of M_{ps1}. r_{o_ps1} and r_{o_ns1} are the output resistances, while g_{m_ps1} and g_{m_ns1} are the two trasconductances of M_{ps1} and M_{ns1} respectively.

Making some calculation we find out that if we call

$$C_1 = C_{d\_ps1} + C_{g\_ns1} \qquad C_2 = C_{d\_ns1} + C_{g\_ps1} \tag{2.46}$$

then two admittances can be indentify

$$Y_1(s) = sC_1 + \frac{1}{r_{o\_ps1}} \qquad Y_2(s) = sC_2 + \frac{1}{r_{o\_ns1}} \tag{2.47}$$

So the current i_t can be written as

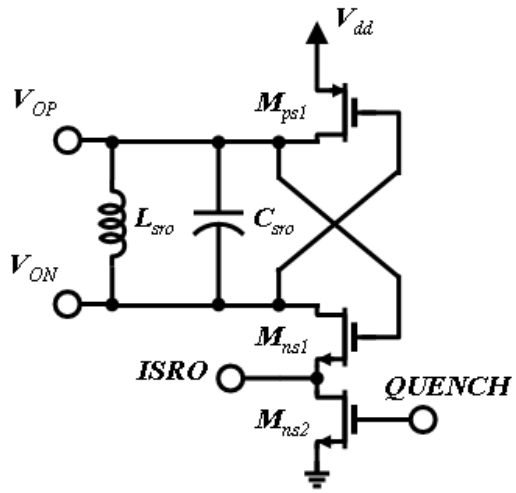


Figure 2.18: Super-regenerative oscillator.

$$i_t = g_{m\_ns1} v_{gs\_ns1} - Y_2(s) v_{gs\_ps1} = g_{m\_ps1} v_{gs\_ps1} - Y_1(s) v_{gs\_ns1} \tag{2.48}$$

and

$$v_t = -v_{gs\_ps1} - v_{gs\_ns1} \tag{2.49}$$

In presence of a cross-coupled differential pair where both the devices are equals, two N-

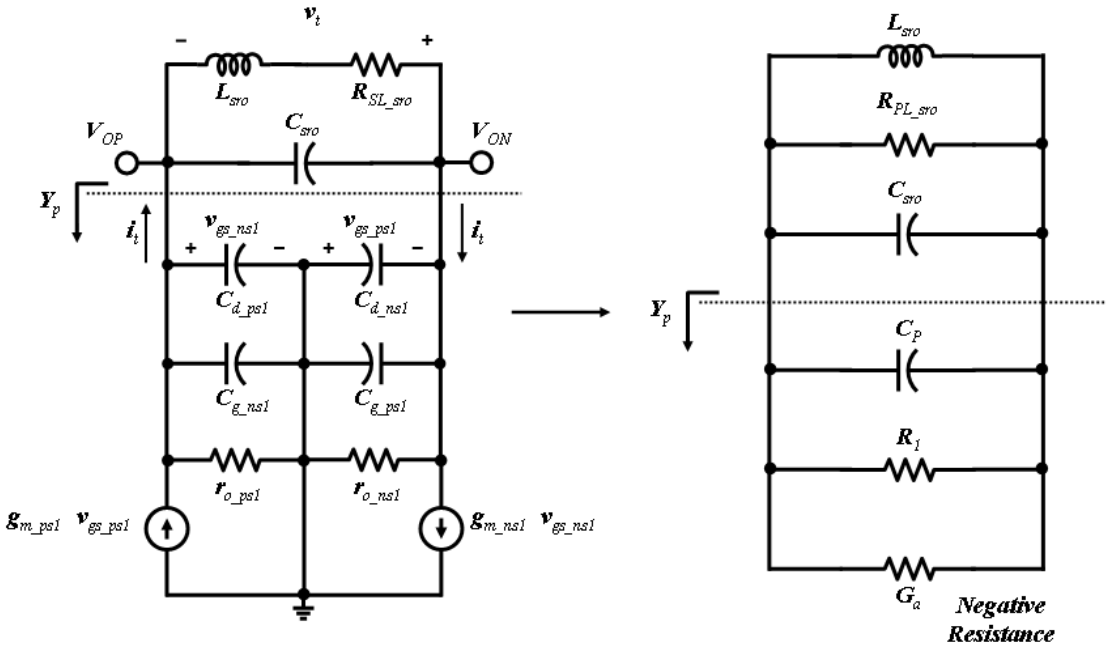


Figure 2.19: Total Network representation of the SRO.

MOSFETs or two P-MOSFETs, then

$$C_1 = C_2 = C \tag{2.50}$$

$$r_{o\_ns1} = r_{o\_ps1} = r_o \tag{2.51}$$

$$Y_1(s) = Y_2(s) = Y(s) \tag{2.52}$$

$$g_{m\_ns1} = g_{m\_ps1} = g_m \tag{2.53}$$

$$v_{gs\_ps1} = v_{gs\_ns1} = v_{gs} \tag{2.54}$$

From eq.(2.49)

$$v_{gs} = -\frac{v_t}{2} \tag{2.55}$$

and i_t becomes

$$i_t = v_{gs}(g_m - Y(s)) = -\frac{v_t}{2}(g_m - Y(s)) \tag{2.56}$$

From eq.(2.55), the admittance $Y_P(s)$ that is shown in Fig.2.19(a) results

$$Y_P(s) = \frac{i_t}{v_t} = -\frac{g_m}{2} + \frac{Y(s)}{2} = -\frac{g_m}{2} + \frac{sC}{2} + \frac{1}{2r_o} \tag{2.57}$$

From eq.2.57 the negative resistance is now visible, written as conductance $-g_m/2$

$$G_a = -\frac{g_m}{2} \qquad C_P = \frac{C}{2} \qquad \frac{1}{R_1} = \frac{1}{2r_o} \tag{2.58}$$

Now, if the Q factor of L_{sro} is available, the respective parasitic shunt capacitance can be extrapolated as

$$R_{PL\_sro} = (1 + Q^2)R_{SL\_sro} \tag{2.59}$$

With this value there are all the elements to build a model for the total network, that is shown in Fig.2.19(b).
The overall network has an impedance that can be written as

$$Z_{tot}(s) = \frac{sL_{sro}}{1 + sL_{sro}\left(\frac{1}{R_{PL\_sro}} + \frac{1}{R_1} - G_a\right) + s^2 L_{sro}C_{sro}} \tag{2.60}$$

And the final condition to have instability is

$$\frac{1}{R_{PL\_sro}} + \frac{1}{R_1} - G_a < 0 \quad \longrightarrow \quad g_m > \frac{1}{r_o} + \frac{2}{R_{PL\_sro}} \tag{2.61}$$

2.4.2 Accurate Model of the Negative Resistance Oscillator

In the current-reuse LC-VCO, the circuit is not symmetrical and so eq.2.50)-(2.51)-(2.52)-(2.53)-(2.54) are not valid anymore. From eq.(2.46) to eq.(2.49) the considerations are the same. After that, solving a system including eq.(2.48) and (2.49), generates the following admittance

$$Y_P(s) = \frac{i_t}{v_t} = \frac{Y_1(s)Y_2(s) - g_{m\_ns1}g_{m\_ps1}}{g_{m\_ns1} + g_{m\_ps1} + Y_1(s) + Y_2(s)} \tag{2.62}$$

which it is exactly

$$Y_P(s) = \frac{s^2 C_1 C_2 + s\left(\frac{C_1}{r_{o\_ns1}} + \frac{C_2}{r_{o\_ps1}}\right) + \left(\frac{1}{r_{o\_ns1}r_{o\_ps1}} - g_{m\_ns1}g_{m\_ps1}\right)}{s(C_1 + C_2) + \left(g_{m\_ns1} + g_{m\_ps1} + \frac{1}{r_{o\_ns1}} + \frac{1}{r_{o\_ps1}}\right)} \tag{2.63}$$

Introducing 5 new parameters

$$A = C_1 C_2 \tag{2.64}$$

$$B = \frac{C_1}{r_{o\_ns1}} + \frac{C_2}{r_{o\_ps1}} \tag{2.65}$$

$$C = \frac{1}{r_{o\_ns1} r_{o\_ps1}} - g_{m\_ns1} g_{m\_ps1} \tag{2.66}$$

$$D = C_1 + C_2 \tag{2.67}$$

$$E = g_{m\_ns1} + g_{m\_ps1} + \frac{1}{r_{o\_ns1}} + \frac{1}{r_{o\_ps1}} \tag{2.68}$$

eq.2.63 becomes

$$Y_P(s) = \frac{s^2 A + sB + C}{sD + E} \tag{2.69}$$

With some calculations the real and the imaginary part of $Y_P(s)$ result

$$Y_P(s) = \frac{\omega^2(BD - AE) + CE}{\omega^2 D^2 + E^2} + j\omega \frac{\omega^2 AD + BE - CD}{\omega^2 D^2 + E^2} \tag{2.70}$$

The first member represents the real part

$$Re\{Y_P(s)\} = \frac{\omega^2(BD - AE) + CE}{\omega^2 D^2 + E^2} = G_a + \frac{1}{R_1} \tag{2.71}$$

The second part instead is the imaginary part

$$Im\{Y_P(s)\} = \omega \frac{\omega^2 AD + BE - CD}{\omega^2 D^2 + E^2} = \omega C_P \tag{2.72}$$

Using Cadence and a spreadsheet it is easy to estimate the real and the imaginary part of $Y_P(s)$, and starting from that, extract the value of G_a and check if it is negative as i has to be. At the same time, the next step is to evaluate the value of C_{sro} that I have to add to the tank to tune the resonant frequency of the SRO at 24 GHz.

$$C_{sro} = \frac{1}{(2\pi f_q)^2 L_{sro}} - C_P \tag{2.73}$$

2.5 Tunable Differential Ring Oscillator (RO)

[14][18] To get the circuit more realistic I also implemented a tunable differential ring oscillator which had to generate a quench signal with a range of frequencies between 100 MHz to 2 GHz. In Fig.2.20 the final structure of the differential ring oscillator is shown. This is the engine of the ring oscillator and the fine-tuning is achieved through the control of the bias current in the 4 gates by changing the voltage at node V_{B1}. The output signal is taken from the two nodes V_{RP} and V_{RN} and it is sent to the differential buffer which is shown in Fig.2.21.

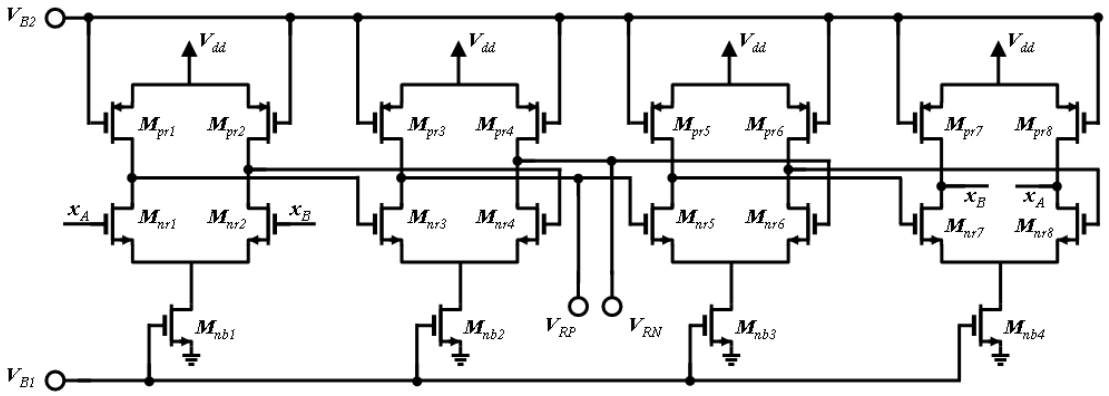


Figure 2.20: Tunable Differential Ring Oscillator.

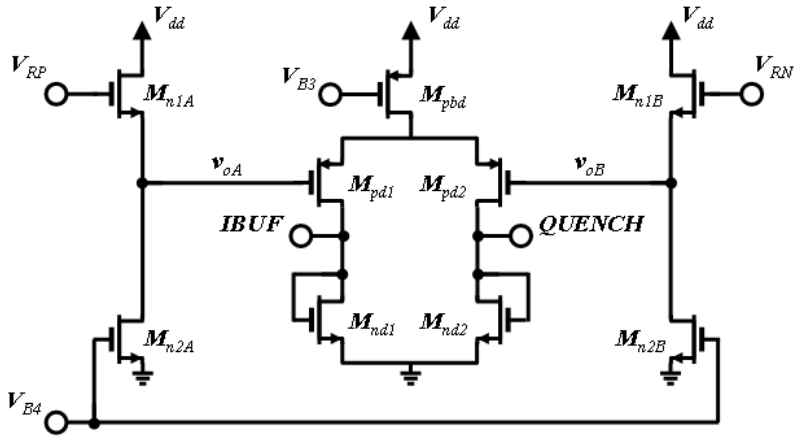


Figure 2.21: Buffer Stage of the Differential Ring Oscillator.

Step by step, let start to explain how the differential ring oscillator works, considering Fig.2.20. This circuit has been designed to generate a source for the quench signal that had to be tunable in a big range of frequencies, from 100 MHz to 2 GHz. Furthermore, the goal is to

reduce the power dissipation. The circuit is formed by 4 stages (gates) in series with a cross connection at the end of the forth stage with the first one. This cross connection guarantees a 180° phase shift in the Nyquist diagram. Pay attention at how the two nodes x_A and x_B connect the last with the first gate. Having 4 stages, at the output of each one there is a 45° phase shift.

Considering only one gate, the pull-up represents the load (r_{op}) and the two P-MOSFETs are two variable resistances which are driven by the voltage source V_{B2}. V_{B1}, instead, is driving the N-MOSFET at the bottom of the structure (M_{nb}) and this transistor is the one which decides the current that is flowing in the gate. The propagation delay of one stage can be described as:

$$t_{dg} \propto RC \propto \frac{\Delta V \times C}{I_{bias}} \tag{2.74}$$

where ΔV is the voltage change across the load resistor R of each gate ($R \approx r_{on} \parallel r_{op}$), C is the total output capacitance, and I_{bias} is the biasing current. Equation (2.74) shows that the propagation delay of one stage is proportional to the output voltage swing of the gate. In this design, instead, ΔV is roughly constant and only I_{bias} is changing. Increasing V_{B1} and decreasing V_{B2} at the same time, I_{bias} goes up and the output resistance of the two P-MOSFETs goes down, so the voltage drop in the load (ΔV) remains roughly the same. Increasing the bias current I_{bias}, t_{dg} goes down, and so the frequency of the differential output signal goes up. The number of the stages in series is also important and 4 is the minimum amount of stages. Using less then 4 stages with this technology, the total propagation delay, that is

$$T_d = 2 \times N \times t_{dg} \tag{2.75}$$

with N number of stages, becomes really small and it is impossible to achieve 100 MHz as minimum wanted frequency for the output signal. Furthermore, the amplitude of the oscillation, increasing the frequency, becomes little because the voltage gain of each gate goes down, and it would be necessary a huge value of R to maintain ΔV constant.

The buffer stage, that is shown in Fig.2.21, has been introduced to modify the shape of the signal coming from the ring oscillator, obtaining an output final quench signal with the wanted features. How we can see there is first a common-drain stage which has just to modify the bias voltage of the signal roughly maintaining the AC amplitude. The equation that we can use in

first approximation at low frequency, to decide the voltage gain of the common-drain stage, is:

$$a_{v0} = \frac{g_m}{g_m + \dfrac{1}{R'_L}} \quad , \qquad R'_L = R_L \parallel r_0 \parallel \frac{1}{g_{mb}} \tag{2.76}$$

where g_m is the transconductance of M_{n1A} and M_{n1B}, R_L is the output resistance of M_{n2A} and M_{n2B}, r_0 is the output resistance of M_{n1A} and M_{n1B}, and g_{mb} is the transconductance of M_{n1A} and M_{n1B} due to the body-effect ($V_{bs} \neq 0$). If R_L and r_0 remain high, the voltage gain can be written as:

$$a_{v0} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\chi} \quad , \qquad \chi = \frac{g_{mb}}{g_m} \tag{2.77}$$

So, when the body-effect is not so relevant the voltage gain of a common-drain stage is 1. Then, for both the common-drain stages, the transistor size and the bias current are designed in such a way to have the wanted DC value of the output voltage in v_{oA} and v_{oB}. V_{B4} is the voltage signal which has to drive M_{n2A} and M_{n2B}, deciding the bias current in both two branches.

At the end, there is the final differential buffer, which is designed to realize a current mirror with the tail transistor M_{ns2} of the SRO (see Fig.3.7), using the load transistor in diode configuration M_{nd2}. Also for the buffer, the bias current is decided by an external voltage signal V_{B3} which drives M_{pbd}. It is important to set the DC component of the two signals v_{oA} and v_{oB} in the perfect point because its AC component will have to turn the two P-MOSFETs, M_{pd1} and M_{pd2}, ON and OFF alternately. In this way the bias current coming from the supply will flow first in one branch and then in the other one, obtaining the maximum swing oscillation in the output. Transistors M_{nd1} and M_{nd2} will be chosen to generate a current mirror with transistor M_{ns2} of the SRO.

In the next chapter, it will be shown that both outputs, $QUENCH$ and $IBUF$, having opposite phase, will result useful. Anyway, it is important to notice how 4 external sources (V_{B1}, V_{B2}, V_{B3} and V_{B4}) are necessary to control the behaviour of the Ring Oscillator.

Chapter 3

Circuit Design

The main goal of this project was to design a super-regenerative receiver, for short-range distance applications, capable to achieve a maximum data-bit rate of 1 $Gbps$, working with a carrier frequency of 24 GHz. From the theory that has been reported in the second chapter, the actual design of an SRR should include a PLL that controls the quench voltage-controlled oscillator (VCO). The global circuit should be closed-loop, as it was shown in Fig.2.13, which guarantees the synchronous operation of the receiver. In this design, instead, there was not enough time to project the PLL, and so the receiver is an open-loop circuit, where the quench frequency has been chosen using a current-controlled ring-oscillator. In Fig.3.1 there is the global schematic design of the SRR. In the real testing part, the synchronization between quench signal and data coming from the antenna, should be done using the testing instruments. The purpose, right now, was just to show how the circuit behaves in the synchronous operating mode. The RF signal coming from the antenna was ideal and no sources of noise were included in the circuit. In this way all the obtained results are completely ideal and they just have to be read as a starting point for a better comprehension of the super-regenerative mechanism. The difficulty in modelling the regenerative behaviour forced to adopt a sort of "cut and try" method based on results obtained during the simulation of each block of the circuit. It has been verified that the design of the LNA and the SRO cannot be divided in two. In fact, with the SRO configuration that has been chosen, the output impedance of the LNA is strongly dependant to the input impedance of the SRO, which is changing in relation with the quench signal. This means that the gain of the LNA changes periodically with the quench frequency f_q. When the SRO works in the unstable region, the tank of the LNA goes in low-impedance, because the input impedance

of the SRO goes down. So, during this phase it looks like the LNA is amplifying in current and not in voltage. The size of the blocking capacitor C_{B2} becomes fundamental, because it has to guarantee the maximum transfer energy, realizing a sort of matching between LNA and SRO. The values of this capacitance has been chosen by simulation and it is 200 fF. So at the end, these two blocks, in the first step, have to be designed separately, but then, some modifications are necessary to get the correct behaviour of the receiver. The supply voltage for the project in general was 1 V.

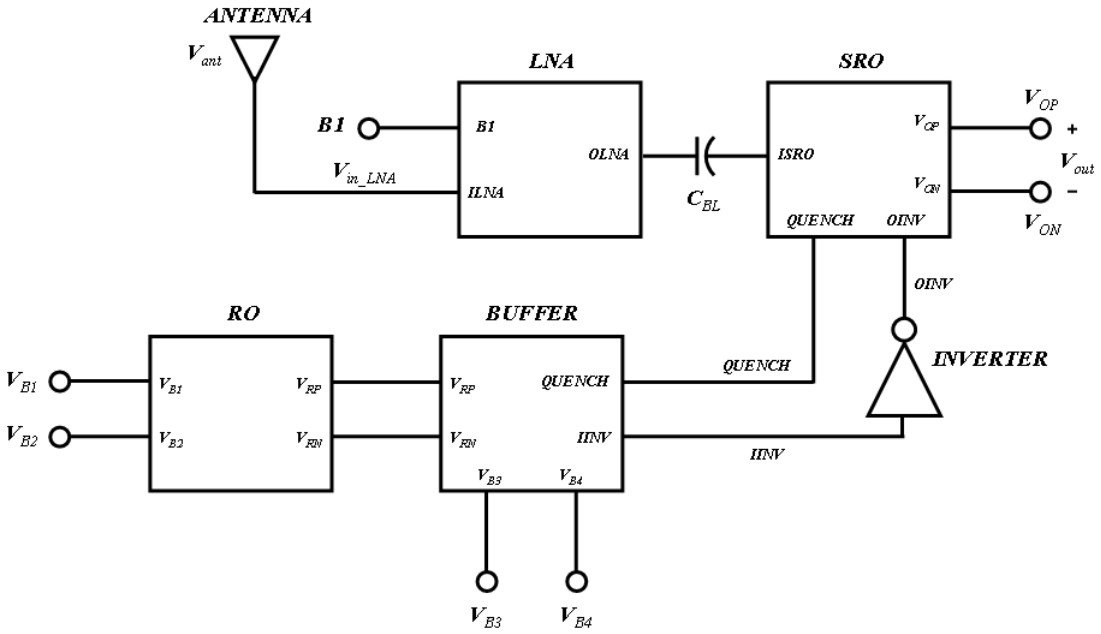


Figure 3.1: Global Circuit Design.

Component	Value
C_{BL}	200 fF

Table 3.1: Blocking Capacitors

First of all the AM (Amplitude-Modulated) signal comes from the Antenna and it is injected inside the LNA. For an AM signal the information is stored around the carrier frequency f_c, in the lower and in the upper sidebands. Thus, to have a circuit capable of achieving a maximum data-bit rate of 1 $Gbps$ ($f_m = 1\,GHz$), the LNA bandwidth ($-3\,dB$ band) should be bigger than 3 GHz and with a central frequency of 24 GHz. The LNA gain has to be about 10 dB. In fact not a lot of power has to be dissipated in the LNA. It just have to guarantee a good

input power matching with the antenna, affording a good noise figure and minimizing the power injected back into the antenna due to the building-up of oscillations by SRO module.

At the same time, the Ring-Oscillator (RO), which is current-controlled by V_{B1} and V_{B2}, has to generate a quench signal that can be setted in a range between 100 MHz and 2 GHz. This signal goes through the BUFFER stage, which contains inside a common-drain stage and a differential buffer. One of the two outputs of the differential buffer becomes the $QUENCH$ signal. The other one, that has opposite phase ($IBUF$), goes inside a static INVERTER which has to amplify the AC amplitude of the signal using the whole available voltage swing between 0 V to 1 V.

Using Cadence, in the simulation environment, the synchronism between the data-signal coming from the LNA ($ISRO$) and the $QUENCH$ coming from the BUFFER is easily obtained. In reality, instead, there is not this information, and so, for an automatic receiver, which does not need to be manually controlled, a PLL is necessary. So, in simulation, RF signal and $QUENCH$ signal goes into the SRO already synchronized. The gain of the SRO is periodically varied by the $QUENCH$, sampling the RF signal at the point of maximum sensitivity. The importance of the signal coming from the inverter ($OINV$) will be explained in the next section.

3.1 Low-Noise Amplifier (LNA)

Fig.3.2 shows the configuration that has been used to implement the LNA. First of all, the LNA has to guarantee a good impedance matching with the antenna; it means that S_{11} has to be smaller than $-10\,dB$. The second point is that the LNA should minimize the power

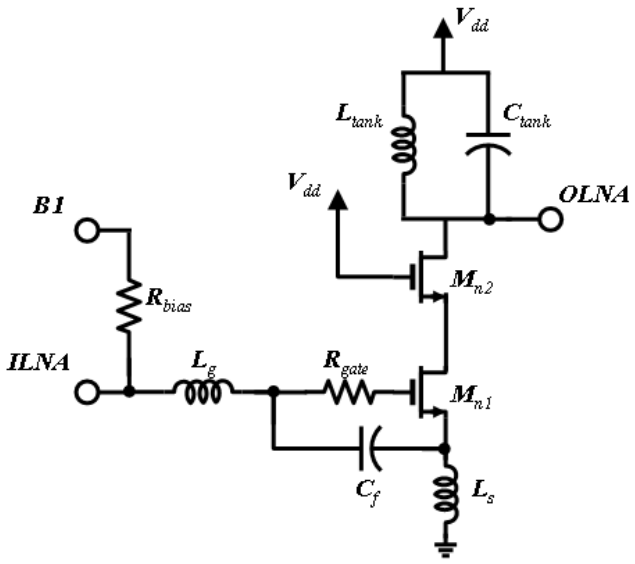


Figure 3.2: Low-Noise Amplifier.

Device	Type	Size W/L	# fingers	Bias
M_{n1}	N-MOSFET	$10\mu m/60nm$	10	$1.53\,mA$
M_{n2}	N-MOSFET	$10\mu m/60nm$	10	$1.53\,mA$

Table 3.2: Active devices (LNA)

Component	Value	Q_L factor	Parasitic Resistance
L_g	$840\,pH$	15	$8.44\,\Omega$
L_s	$220\,pH$	8	$4.15\,\Omega$
L_{tank}	$880\,pH$	15	$8.84\,\Omega$
C_f	$33.5\,fF$		
C_{tank}	$35\,fF$		
R_{gate}	$2\,\Omega$		
R_{bias}	$10\,K\Omega$		

Table 3.3: Passive Components (LNA)

injected back into the antenna due to the building-up of self-oscillations by the SRO block; and

it means that S_{12} has to be also as small as possible. S_{12} really small means that the amplifier is unidirectional. Then, this kind of LNA is an inductive source-degenerated low noise amplifier, which realizes an input matching without using any resistance, and so, without the addition of any further source of noise. It is the best candidate to achieve a good noise figure. For any receiver, in fact, the first stage is the most important for the noise. The biggest amount of noise usually is injected into the receiver by the antenna. The noise figure, if there are many circuital blocks connected in cascade, is calculated as

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \frac{F_4 - 1}{A_1^2 A_2^2 A_3^2} + \dots \tag{3.1}$$

where $F_{\#}$ is the noise figure in dB of each stage and $A_{\#}$ the voltage gain. It is clear that, if the first stage of the circuit has an F_1 small and the voltage gain A_1 is high, the total noise figure gets better. But in this case, the LNA has to be designed to improve the total noise figure, without dissipating a lot of power in the LNA, so maintaining a low voltage gain. There are two opposite conditions to guarantee, and so a design choice is inevitable. Moreover, if the LNA, during the unstable phase of the SRO is not amplifying in voltage but in current, the trasconductance of M_{n1}, g_1, becomes important and in order to achieve a good noise figure it should be taken high. In first approximation the voltage gain of the LNA, when the SRO is in the unstable phase, has been taken around 10 dB.
For the super-regenerative technique the gain has not to come from the LNA, but this job is assigned to the SRO, the heart of the circuit. The original principle, in fact, would be to have a simple buffer in the first stage of the receiver.

The design technique has been iteratively used and here it is explained:

- chose the values of the inductors, L_s and L_g (for the component values take a look at Tab. 3.3). Usually it is better to use a small inductor in the source because its parasitic series resistance is smaller, and in a common-source stage it is fundamental to have a small resistance in the source, because it causes the decrease of the common-source stage voltage gain. The quality factor of an inductor cannot be decided. It depends on the technology and during the first step of the design, using Cadence, it is necessary to use realistic values for it. To have some experience with a particular kind of technology, helps to take right decisions. For the LNA design two different quality factors have been used: 15 for values of inductance bigger than 400 pH, and 8 for values smaller than that. But it is just a

choice. In theory bigger the inductance and bigger the quality factor, but in reality, when these inductors are realized on chip, because of the parasitic effects, there could also be an opposite behaviour;

- after a possible estimation of Q, also R_s and R_g are evaluated;
- R_{gate} simulates the gate resistance, which is not present inside the model, and for this technology it can be chosen as 2 Ω;
- the operating point of the device M_{n1} is fundamental for the matching too; so, using the simulation, the transistor size and the voltage-bias, $B1$, have been chosen to obtain a good value of g_{m1}, which has to be used in eq. (2.15), and, has to guarantee enough gain for the LNA too;
- with information about size and trasconductance, the parasitic capacitance of M_{n1}, C_{gs1}, can be simulated ;
- the possibility to use C_f gives a new degree of freedom and I could use it to adjust the impedance matching at the end;
- finally, R_{bias} has to be big, because this branch of the circuit, has to be seen as an open-circuit, and it does not have to influence the impedance matching.

Obviously, it is an iterative method and before getting the final configuration many simulations are necessary.

For the calculation part, considering the values in Tab. 3.2 and 3.3 :

- $Z_{in} = s(L_s + L_g) + \dfrac{1}{s(C_{gs1} + C_f)}(1 + g_{m1}R_s) + \dfrac{g_{m1}}{C_{gs1} + C_f}L_s + R_s + R_g + R_{gate} = sL_{tot} + \dfrac{1}{sC_{tot}} + R_{tot}$
- $L_{tot} = (220 + 840) \times 10^{-12} = 1.06 \times 10^{-9} = 1.06\ nH$
- $C_{tot} = \dfrac{(8.57 + 33.5) \times 10^{-15}}{1 + (6.77 \times 10^{-3})(4.15)} = 40.92 \times 10^{-15} = 40.92\ fF$
- $f_0 = \dfrac{1}{2\pi\sqrt{L_{tot}C_{tot}}} = \dfrac{1}{2\pi\sqrt{(1.06 \times 10^{-9})(40.92 \times 10^{-15})}} = 24.16 \times 10^9 \approx 24\ GHz$
- $R_{tot} = \frac{6.77\times10^{-3}}{(8.57+33.5)\times10^{-15}} 220 \times 10^{-12} + 4.15 + 8.44 + 2 = 50\ \Omega$

- $Q = \dfrac{\omega_0 L_{tot}}{2R_{tot}} = \dfrac{(2\pi 24 \times 10^9)(1.06 \times 10^{-9})}{2 \times 50} = 1.6$

For the tank, a big inductance (L_{tank}) has been chosen, to have larger tank equivalent parallel resistance, increasing the gain. C_{tank}, instead, has been chosen at the end, after connecting LNA and SRO together, in order to have the peak of the gain at $24\,GHz$. In the final real circuit, with all the blocks together, in condition of maximum instability for the SRO, the voltage gain has the shape shown in Fig.3.5. At $24\,GHz$ the gain is $11.85\,dB$, but at higher frequencies I can also see something else, another kind of resonance, that is probably due to the instability of the SRO. C_{sro} was chosen equal to $35\,fF$, because with this value the global circuit was working better.

From Fig.3.3, we can see that S_{11}, at $24\,GHz$, is $-19.62\,dB$, and it is perfectly centred. From Fig.3.4, instead, we can observe that S_{12} is $-39.1\,dB$. Both this two S-parameters have been measured considering just the LNA block alone. The same has been done to estimate the noise figure, and it can be seen in Fig.3.6. Its value is $3.61\,dB$. No manual calculations have been done for the noise figure, because there were not any information about the fitting parameters of this technology which are shown in section 2.2.1.

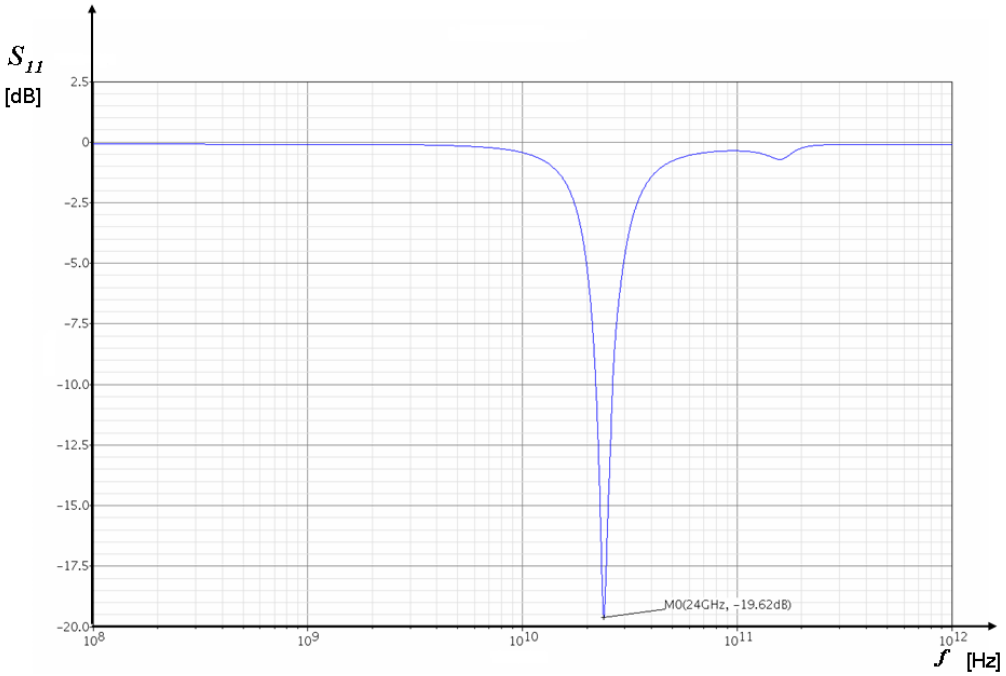


Figure 3.3: S_{11} of LNA

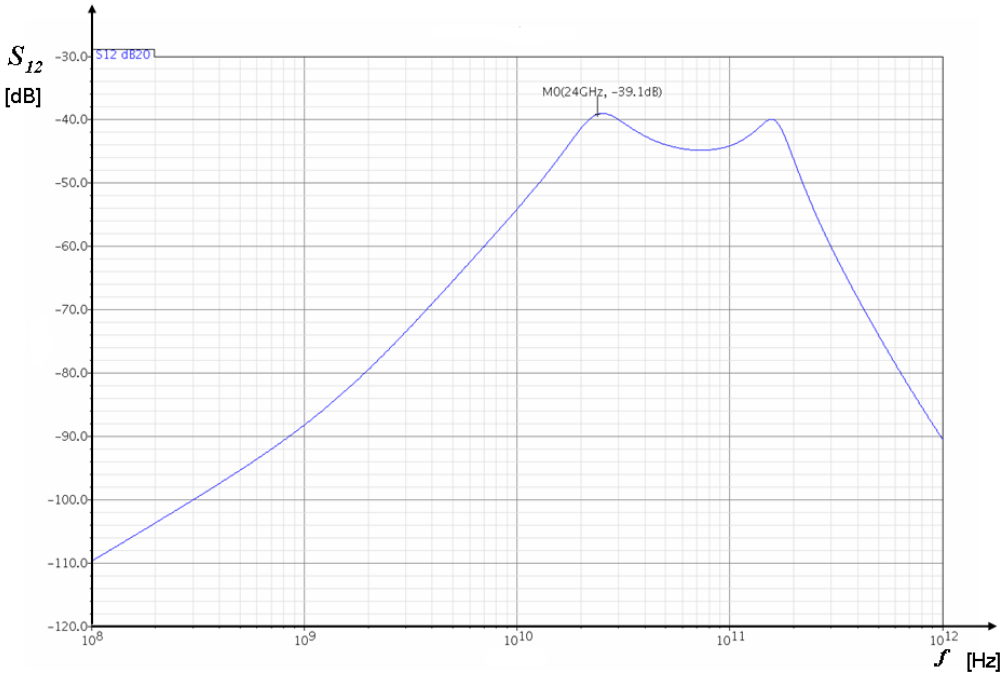


Figure 3.4: S_{12} of LNA

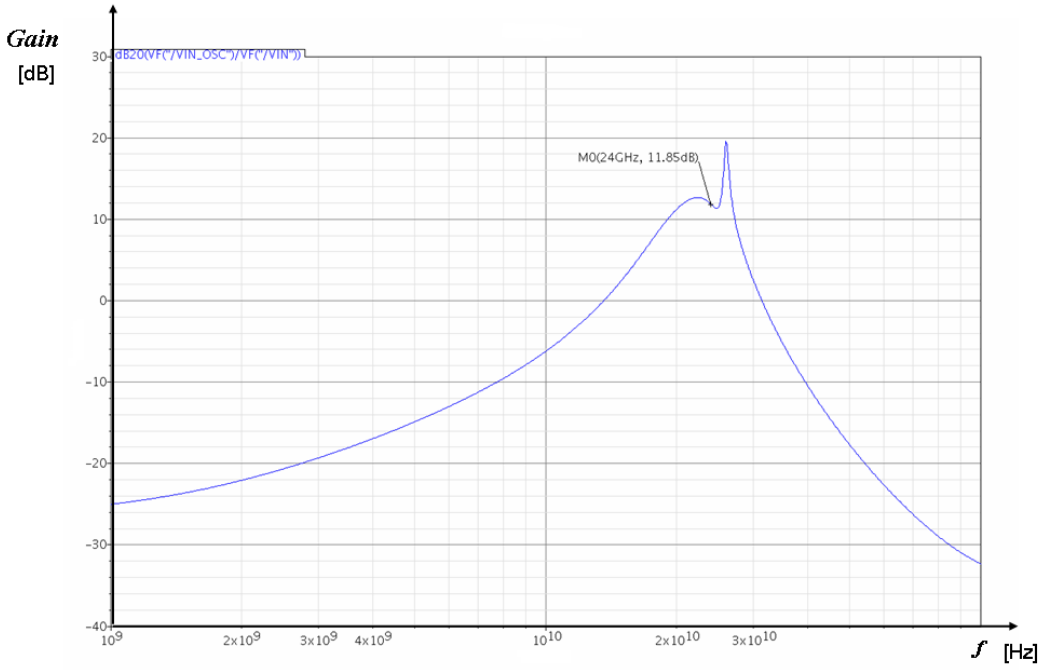


Figure 3.5: Voltage Gain of LNA.

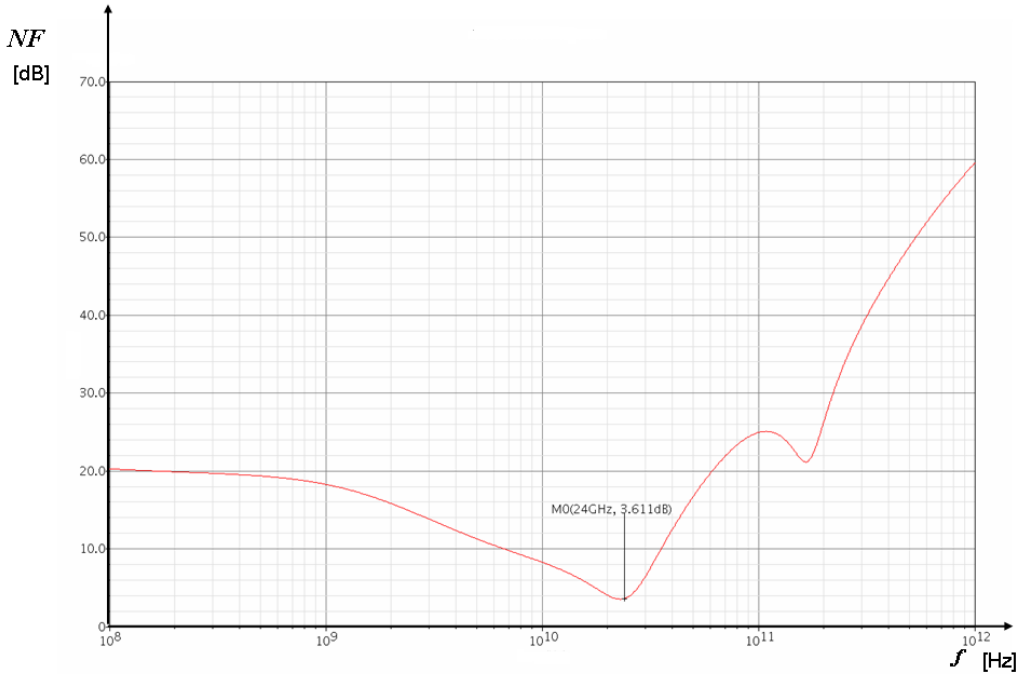


Figure 3.6: Noise Figure of LNA.

3.2 Super-regenerative oscillator (SR0)

Let start to explain the design of the SRO that is the heart of the circuit. Fig.3.7 shows the final configuration that has been implemented. As it has been written in section 2.4,

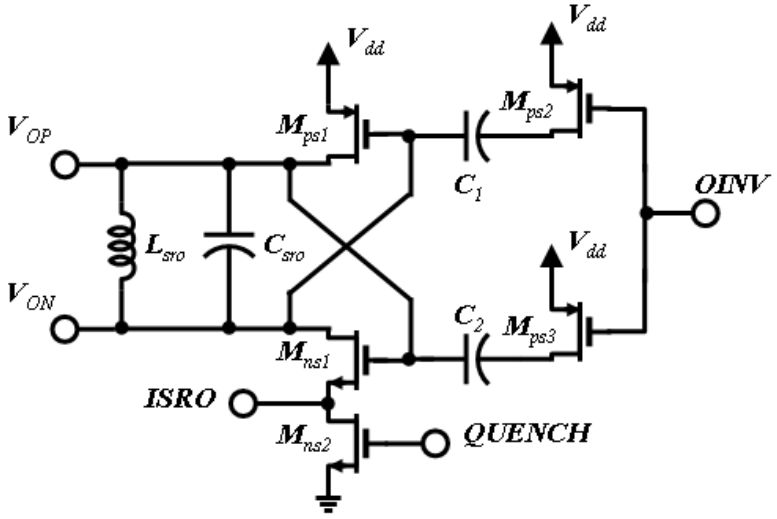


Figure 3.7: Final Version of SRO.

Device	Type	Size W/L	# fingers	Bias ($f_q = 1\ GHz$)
M_{ns1}	N-MOSFET	$20\mu m/60nm$	20	328 μA
M_{ns2}	N-MOSFET	$20\mu m/60nm$	20	328 μA
M_{ps1}	P-MOSFET	$60\mu m/60nm$	60	328 μA
M_{ps2}	P-MOSFET	$10\mu m/60nm$	10	0
M_{ps3}	P-MOSFET	$10\mu m/60nm$	10	0

Table 3.4: Active devices (SRO)

Component	Value	Q_L factor	Parasitic Resistance
L_{sro}	440 pH	15	4.42 Ω
C_{sro}	50 fF		
$C_1 - C_2$	500 fF		

Table 3.5: Passive Components (SRO)

this configuration reduces power dissipation to half that of conventional topologies. In this configuration, the RF signal coming from the LNA ($ISRO$) is injected between the source of M_{ns1} and the drain of M_{ns2}, as it shown in Fig. 3.7. Others injections points has been studied

(the gate of M_{ns2} was one possible option), but the version that is shown in Fig. 3.7 resulted the best one.

The first version of the SRO, that has been tested, was the one introduced in section 2.4 and reported again in Fig. 3.8.

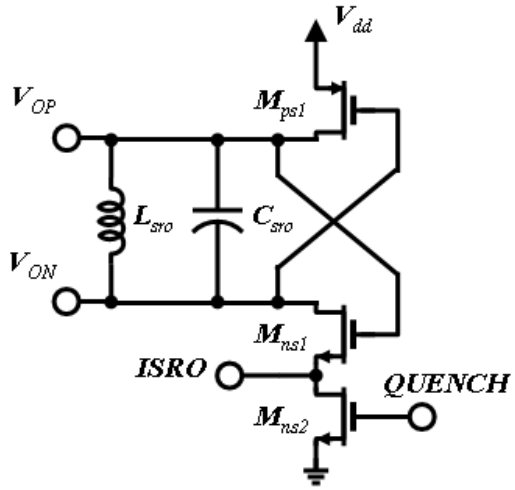


Figure 3.8: First version of the SRO.

Using simple words, this circuit works in this way (take a look at Fig. 3.9):

- the $QUENCH$ drives the gate of M_{ns2}, and in first approximation it can be seen as a sinusoidal signal;
- when the $QUENCH$ goes up, M_{ns2} turns ON and the bias current that is flowing through it increased. The tank of the circuit, which is formed by L_{sro}, C_{sro}, and the two active devices M_{ps1} and M_{ns1}, is designed to be stable until the bias current does not reach a particular value I_{limit}. After this limit the transconductance of M_{ps1} and M_{ns1} becomes big enough to overcome the losses in the tank. So when the current, which is decided by M_{ns2}, goes beyond this limit, the circuit becomes unstable (T_a);
- at this point, if an RF signal is coming from $ISRO$, it will generate a oscillation in the tank that will grow up exponentially;
- when the $QUENCH$ goes down, the current decreases and becomes smaller than I_{limit}. Now the circuit is stable again and it will have to be able to discharge the tank, shutting down the oscillation, in the other part of time available ($T_b = T_q - T_a$).

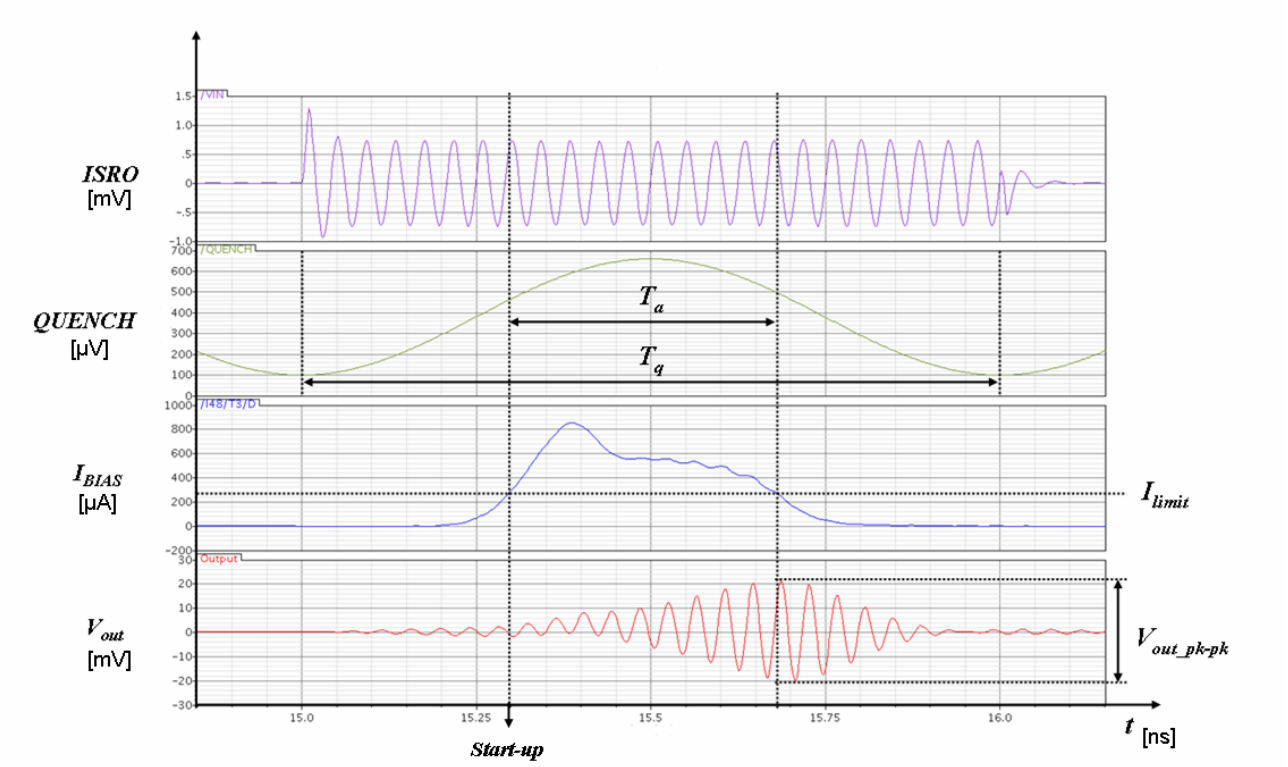


Figure 3.9: Example in Cadence simulation with $f_q = 1\,GHz$: RF signal $ISRO$ (it represents 1 bit), sinusoidal $QUENCH$ signal, bias current I_{BIAS}, and differential SRO output V_{out}.

The SRO has to be seen as a circuit with two sources of power. The first part of this power is coming from $ISRO$ by the RF signal, and we can call it P_{RF}; the other part, instead, is coming from the $QUENCH$ signal, which is going to turn ON and OFF the NMOSFET M_{ns2}, changing the bias current, and we can call it P_Q. These two source of power are related together and they both cause the oscillation in the output. As it will be shown in the last chapter, with the simulation results, these two amount of power are related in a different way, depending by the working frequency, and the relation is not linear. In this project, the quench frequency f_q and the data bit rate are the same, as in the synchronous mode shown in Fig.2.12b. Furthermore, the circuit works between 100 MHz and 2 GHz, and output differential pulse V_{out} needs to have a peak to peak value of about 40 mV.

$$P_{RF} + P_Q \longmapsto V_{out\_pk-pk} \approx 40\,mV$$

If the ratio T_a/T_q remains constant and the peak of the quench signal is maintained at the center of the received pulse, at low frequency, when T_a is big, the oscillation will have more time to

grow up and the main amount of power will be coming from P_Q. P_{RF} will just have to be big enough to make the oscillation star. At high frequency, instead, T_a becomes really small and so there is not a lot of time for the oscillation to grow up. It means that P_{RF} becomes fundamental, the bigger it is and better the output result will be. If the concept of power is substituted with the concept of energy the argument becomes opposite. At low frequency, a small P_{RF} for a long time can produce a bigger amount of energy compared to a big P_{RF} for a really brief time, when the circuit is working at high frequency. As it will be presented in the last chapter, the energy per bit decreases when the frequency goes up.

Before testing the SRO with a real $QUENCH$ signal coming from the RO, an ideal sinusoidal signal has been used. After many simulations, and working with the final version of LNA and SRO, the ideal quench signal has been setted with a DC component of 380 mV and an AC component of 280 mV. So, all the final tests, before adding the real ring oscillator, have been done using this signal.

3.2.1 Design Methodology

To design the SRO the circuit in Fig.3.8 has been considered, and equations in section 2.4.2 (the "Accurate Model of the Negative Resistance Oscillator") have been used. First of all, the value of the inductance[1] L_{sro} has been decided, using also in this time a quality factor of 15. The inductance has to be 440 pH, with a parasitic series resistance of 4.42 Ω. Then, M_{ps1} and M_{ns1}, have to be designed in such a way to have the same g_m. An iterative method, using equations (2.71) and (2.72), is inevitable in order to extrapolate the dimensions for the devices and the bias current. The capacitance to add in the tank, C_{sro}, is the result of eq.(2.73). For the tail transistor, M_{ns2}, the conclusion was to use the same size of M_{ns1}. As showed in the theory, in section 2.4, M_{ns2} will make the SRO work in the current limited mode.

Using a constant quench signal of 660 mV (V_{q_pk} = 380 mV+280 mV), which should simulate the point of maximum instability for the oscillator, with no data input; and solving the equations in section 2.4.2, the active devices in the negative resistance model have to be whit the dimensions that are shown in Tab.3.6:

[1] In the project, respecting the rules of the IBM10LP technology, I used:

- inductors with values bigger than 100 pH (and for my choice, smaller than 1 nH);
- capacitors with values bigger than 20 fF.

Thus,

$$C_1 = 29\ fF \qquad\qquad C_2 = 43.7\ fF$$

The 5 parameters, given in eq.(2.71) and (2.72), result:

- $A = C_1 C_2 = 1.26 \times 10^{-27} F^2$
- $B = \dfrac{C_1}{r_{o\_ns1}} + \dfrac{C_2}{r_{o\_ps1}} = 7.26 \times 10^{-17} FS$
- $C = \dfrac{1}{r_{o\_ns1} r_{o\_ps1}} - g_{m\_ns1} g_{m\_ps1} = -3.86 \times 10^{-5} S$
- $D = C_1 + C_2 = 7.26 \times 10^{-14} F$
- $E = g_{m\_ns1} + g_{m\_ps1} + \dfrac{1}{r_{o\_ns1}} + \dfrac{1}{r_{o\_ps1}} = 1.46 \times 10^{-2} S$

Device	Size W/L	# fingers	I_{BIAS}	C_g	C_d	g_m	r_o
M_{ns1}	$20\mu m/60nm$	20	546 μA	13.16 fF	4.74 fF	6.77 mS	1 $K\Omega$
M_{ps1}	$60\mu m/60nm$	60	546 μA	38.84 fF	15.8 fF	5.84 mS	1 $K\Omega$

Table 3.6: M_{ns1} and M_{ps1} in the SRO

And from eq.(2.71) and (2.72):

- $Re\{Y_P(s)\} = \dfrac{\omega^2(BD - AE) + CE}{\omega^2 D^2 + E^2} = G_a + \dfrac{1}{R_1} = -2.59\ mS$
- $Im\{Y_P(s)\} = \dfrac{\omega^2 AD + BE - CD}{\omega^2 D^2 + E^2} = C_P = 17.8\ fF$

Then, the parasitic series resistance of L_{sro} can be transformed in a parallel resistance using eq.(2.59):

$$R_{PL\_sro} = (1 + Q^2) R_{SL\_sro} = (1 + 15^2) 4.42 = 1\ K\Omega \ \longrightarrow\ G_{PL\_sro} = \frac{1}{R_{PL\_sro}} = 1\ mS$$

The condition form the instability is that $Re\{Y_P(s)\} + G_{PL\_sro} < 0$. From the calculations, in fact, it results that

$$Re\{Y_P(s)\} + G_{PL\_sro} = -1.59\ mS$$

and the circuit is unstable.

Thus, the capacitance to add to the tank, using eq.(2.73), results

$$C_{sro} = \frac{1}{(2\pi f_q)^2 L_{sro}} - C_P = \frac{1}{(2\pi(24 \times 10^9))^2 440 \times 10^{-12}} - 17.8 \times 10^{-15} = 82 \times 10^{-15} = 82\ fF$$

The final value of C_{sro} in simulation is 74 fF, that is really close to the calculated value.

3.2.2 Limits of this configuration and how to increase its performance

After the realization of SRO and LNA, the simulation of the circuit using an ideal quench signal showed that it was not possible to increase the operating frequency (data-bit rate) beyond 800 MHz. Working at bigger frequencies, with an input sequence of bits corresponding to "101010", "1" or "0" were indistinguishable. The output sequence of bits was just a bunch of pulses, also when a "0" (no pulse) had to compare. The main reason of it was that the tank SRO, increasing the frequency, had not enough time to discharge the charge that had been stored with the previous "1". When a "1" is injected into the SRO and the quench signal goes up, the oscillation starts and a lot of energy is stored in the tank. After this time, the quench signal goes down and the tank starts to lose its charge. If the discharging time is not long enough, and the next bit that is coming is a "0" (no RF-signal is going into the tank), the tank, which still contain some charge inside, will generate a new oscillation in the next time that the circuit becomes unstable. The result it will be "11" in the output, instead of "10". Because of the goal of this project was to get a maximum data bit rate of 1 *Gbps* and more, the invention of a new solution was fundamental to solve this problem, and the solution that came up is illustrated in Fig. 3.7.

The key point of this new configuration is the presence of two new P-MOSFETs, M_{ps2} and M_{ps3}. Each of these transistors connects the gate of the active devices, M_{ps1} and M_{ns1}, with the supply. Furthermore, two blocking capacitors, C_1 and C_2, are used to maintain the previous bias conditions of the SRO constant. Using simple words, this new configuration does not have to change the operative point of the already designed SRO, but it just have to create a new easier path to ground for the charge stored in the tank during the stable phase of the SRO. As we can see, in these new transistors there is not DC current that is going through, because drain and source have the same potential. However, changing their gate voltage, using the whole voltage window available from 0 V to 1 V, I can turn OFF and ON these devices and vary their output resistance r_o. Thus, at the end, these two transistor can change the Q factor of the tank, making much easier the discharge of the tank when the $QUENCH$ signal goes down and the circuit becomes stable. Now, it is possible to understand the importance of the signal $OINV$ coming from the inverter. It is a signal in phase with the $QUENCH$, just a bit translated ahead in time, due to the delay of the inverter, and it oscillates with frequency f_q between 0 V and 1 V.

When the $QUENCH$ goes up, $OINV$ goes up to $1\,V$, M_{ps2} and M_{ps3} are completely OFF (their are in the high-impedance region), and so their output resistance is huge. The circuit, in the unstable phase, works exactly as in the first configuration. When the $QUENCH$ goes down, instead, $OINV$ goes down to $0\,V$, M_{ps2} and M_{ps3} gets completely ON, and so their output resistance becomes small. In the stable phase, the total conductance of the tank increases and the Q factor gets smaller than in the first configuration. In the same time interval, now, the tank is capable to lose its charge much faster.
In the design, the value of C_{sro} has to be smaller, because now, connected to the tank, there are other parasitic capacitance coming from M_{ps2} and M_{ps3}. By simulation the new value of C_{sro} is $50\ fF$.
In the old version of the SRO, the quality factor had this form (take a look at Fig. 2.19):

$$Q = \frac{\omega C_{TOT}}{G_{TOT}} \quad \longmapsto \quad C_{TOT} = \frac{1}{(2\pi f)^2 L_{sro}} \quad and \quad G_{TOT} = \frac{1}{R_1} + \frac{1}{R_{PL\_sro}} \tag{3.2}$$

Now, instead, the total conductance changes.

$$G_{TOT} = \frac{1}{R_1} + \frac{1}{R_{PL\_sro}} + G_x \tag{3.3}$$

The contribute of G_x is insignificant during the unstable phase, but becomes considerable during the stable phase. To built a new analytical model for this circuit results complicated and would not give more information compared to the one shown in section 2.4.2, so, the parametric simulation in Cadence has been used to estimate the best size of the two transistors, M_{ps2} and M_{ps3}, the value for the two blocking capacitors, C_1 and C_2, and the final value of C_{sro}. In Tab.3.4 they are listed. The only annotation is that: C_1 and C_2 have to be big because at $24\,GHz$ they have to act as short-circuits; while the size of M_{ps2} and M_{ps3} has been chosen to have a working circuit with the minimum occupied area on chip.

Last considerations:

- two N-MOSFETs connected to ground could be used instead of two P-MOSFETs, but two inverters would be necessary, and not just one. The total circuit would dissipate more power because of it, but the performance would not improve;
- using just one device to discharge the tank, M_{ps2} or M_{ps3}, would get the SRO unbalanced, with bad output performance.

3.3 Ring Oscillator (RO)

Fig.3.10 shows the circuital configuration for the ring oscillator.

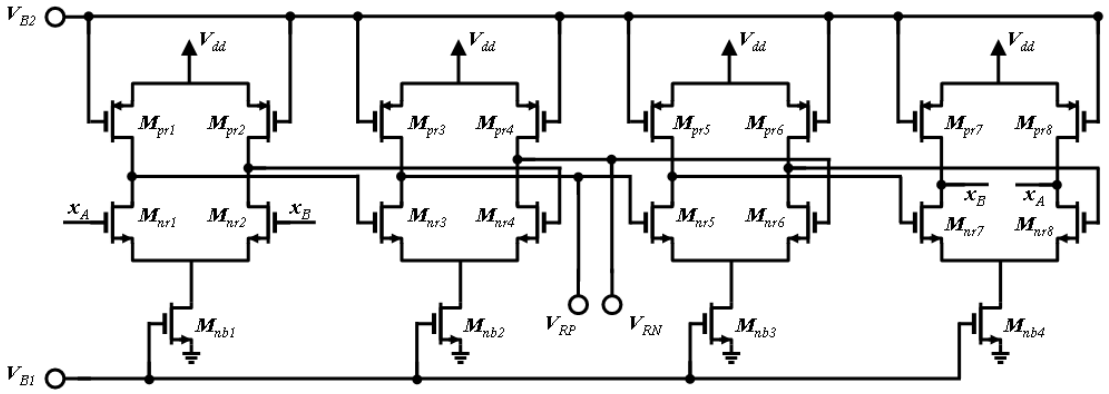


Figure 3.10: Ring-Oscillator.

Device	Type	Size W/L	# fingers	Bias ($f_q = 1\ GHz$)
$M_{nb1} - M_{nb4}$	N-MOSFETs	$40\mu m/500nm$	40	215 μA
$M_{nr1} - M_{nr8}$	N-MOSFETs	$50\mu m/60nm$	50	108 μA
$M_{pr1} - M_{pr8}$	P-MOSFETs	$40\mu m/60nm$	40	108 μA

Table 3.7: Active devices (RO)

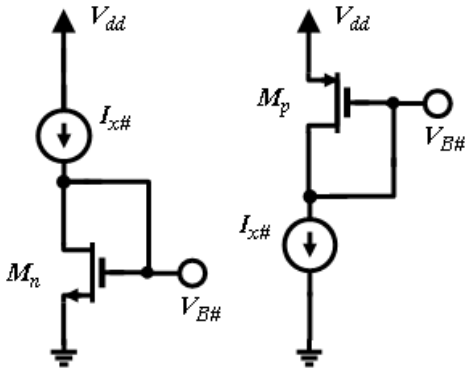
The whole design has been done using Cadence simulation. Indeed, to built a tunable ring oscillator, which is capable to work in a large range of frequencies (for this project, from 100 MHz to $2s\ GHz$), there are too many variables to take in account, and a manually calculation would not be so easy and helpful.

First of all, it is necessary to understand how many stages have to be used to get a circuit able to generate oscillations at 100 MHz. In fact, increasing the number of stages, maintaining constant the bias conditions, the total delay time gets bigger and bigger, and the oscillation frequency goes down. After different simulations, the minimum number of stages has been found to be 4. Using 4 stages, it means that after each one the phase of the oscillation is 45 degrees shifted. The output of the ring oscillator is withdrawn form the nodes V_{RP} and V_{RN}.

The size of the devices is shown in Tab.3.7.

After this step, as it has been shown in section 2.5, the circuit has been driven in current, using two external sources, connected to V_{B1} and V_{B2}, in current mirror configuration (see Fig. 3.11).

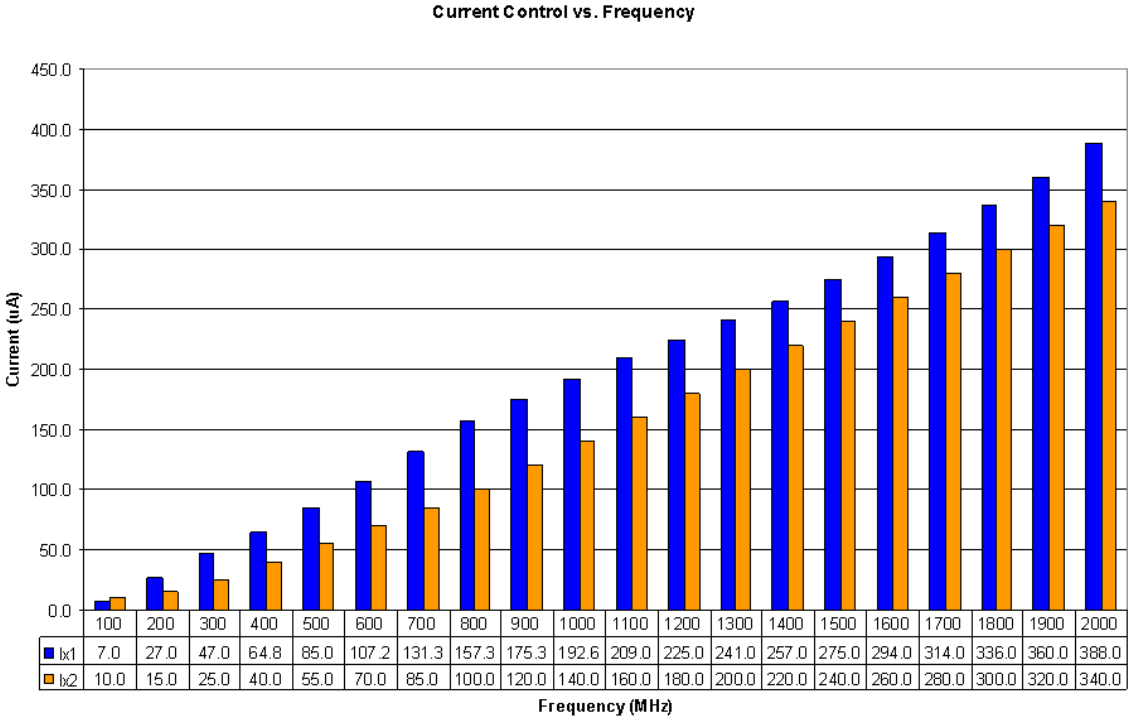
Using a mirror with an 1:1 ratio, for both the N-MOSFETs $M_{nb1} - M_{nb4}$, and the P-MOSFETs



(a) N-MOSFET (b) P-MOSFET

Figure 3.11: Current Mirror configuration for N-MOSFET and P-MOSFET, respectively.

$M_{pr1} - M_{pr4}$, in Fig.3.12, there is the plot with the current values that have to be used in the mirrors in order to make the ring oscillator work between 100 MHz to 2s GHz. I_{x1} drives $M_{nb1} - M_{nb4}$, while $M_{pr1} - M_{pr8}$ are driven by I_{x2}. Increasing I_{x1} the oscillation frequency goes up, and increasing I_{x2} the output resistance of the P-MOSFETs goes down, maintaining the



	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
Ix1	7.0	27.0	47.0	64.8	85.0	107.2	131.3	157.3	175.3	192.6	209.0	225.0	241.0	257.0	275.0	294.0	314.0	336.0	360.0	388.0
Ix2	10.0	15.0	25.0	40.0	55.0	70.0	85.0	100.0	120.0	140.0	160.0	180.0	200.0	220.0	240.0	260.0	280.0	300.0	320.0	340.0

Figure 3.12: Current Control in the Ring Oscillator.

output amplitude of the oscillation ($V_{RP} - V_{RN}$) pretty constant.
From Fig.3.12, it can be observed that both currents grows up almost linearly.

Next step is to transfer this signal from the nodes V_{RP} and V_{RN} to the SRO, but there is some problems:

- the DC voltage bias at these nodes is not optimum;
- the amplitude of the AC component is too small to be used as $QUENCH$ signal;
- moreover, the SRO, is a single ended circuit and a buffer which transforms the differential signal that is coming from the RO into a perfect $QUENCH$ signal with the right shape, is necessary.

3.3.1 Buffer stage

As it is shown in Fig.3.13, the buffer is formed by two stages, and both of these are current controlled by an external source, V_{B3} and V_{B4}. Also in this case, the same method to drive the transistors M_{pbd}, M_{n2A}, and M_{n2B}, has been used. Two current mirror with an 1:1 ratio have been implemented. The P-MOSFET M_{pbd} has been driven by a current I_{x3} (3.11b) equal to 600 μA, while the two N-MOSFETs M_{n2A} and M_{n2B}, with a current I_{x4} (3.11a) equal to 50 μA. The first stage of the buffer is a simple common-drain stage. The goal, here, is to change the DC voltage bias of the nodes V_{RP} and V_{RN}, maintaining the AC component of the signal coming from the ring oscillator, pretty identical. In this way, the second stage, which is a differential pair that works as a buffer, can receive a input signal with the desired DC voltage bias. I_{x4} is important, in the testing part, to set the DC component of the signals v_{oA} and v_{oB}, in the right position to make the next stage work in a better way.
The differential pair has to realize a current mirror with the N-MOSFET M_{ns2} of the SRO. In this way, it is possible to control the current that is flowing in the SRO simply changing I_{x3}. The problem is that M_{ns2} is working in the triode region, while M_{nd2} is in saturation; it means that the current mirror is not precise. Making M_{nd2} 4 times smaller than M_{ns2} (ratio 1:4), the average current in M_{ns2} is not 4 times bigger that the one in M_{nd2}, but about 1.4.

The main thing to know is that, the ring oscillator has been not designed to generate a sinusoidal $QUENCH$ signal with the same characteristic of the ideal one ($V_{DCq} = 380\ mV$ and $V_{ACq} = 280\ mV$), but buffer has been built to control the current in the SRO, making it similar

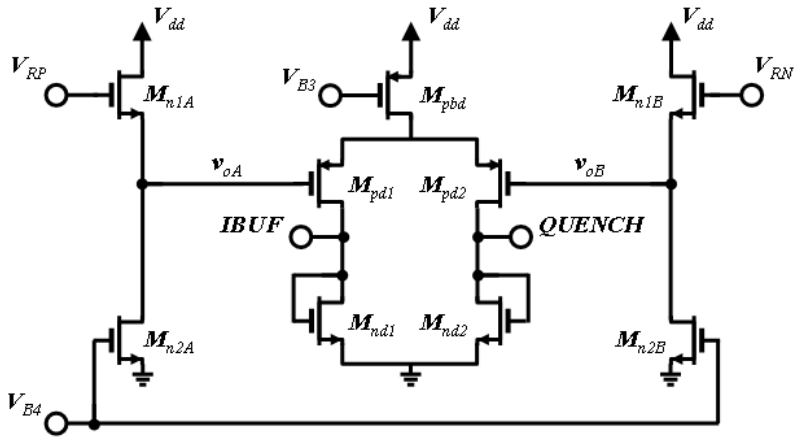


Figure 3.13: RO Buffer.

Device	Type	Size W/L	# fingers	Bias ($f_q = 1\,GHz$)
$M_{n1A} - M_{n1B}$	N-MOSFETs	$10\mu m/60nm$	10	51.4 μA
$M_{n2A} - M_{n2B}$	N-MOSFETs	$5\mu m/300nm$	5	51.4 μA
$M_{nd1} - M_{nd2}$	N-MOSFETs	$5\mu m/60nm$	5	236 μA
$M_{pd1} - M_{pd2}$	P-MOSFETs	$80\mu m/60nm$	80	236 μA
M_{pbd}	P-MOSFET	$80\mu m/500nm$	80	472 μA

Table 3.8: Active devices (RO Buffer)

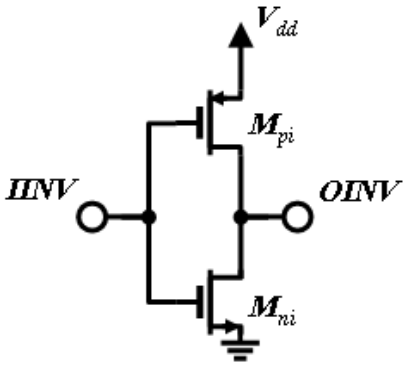


Figure 3.14: Inverter.

Device	Type	Size W/L	# fingers	Bias ($f_q = 1\,GHz$)
M_{ni}	N-MOSFET	$3\mu m/60nm$	3	86.1 μA
M_{pi}	P-MOSFET	$10\mu m/60nm$	10	86.1 μA

Table 3.9: Active devices (Inverter)

o the ideal case. Only the shape of the current in the SRO matters. So, the $QUENCH$ signal has not to be necessary sinusoidal.

Then, a static inverter (3.14) has been used to expand the AC component of the signal $IINV$, which is opposite in phase compared to the $QUENCH$, between $0\,V$ e $1\,V$. The size of M_{pi} and M_{ni} has been chosen to guarantee also at high frequency, when the time to charge and discharge the output capacitance of the inverter gets really small, to have the maximum output voltage swing.

Chapter 4

Simulation of the SRR and Discussion

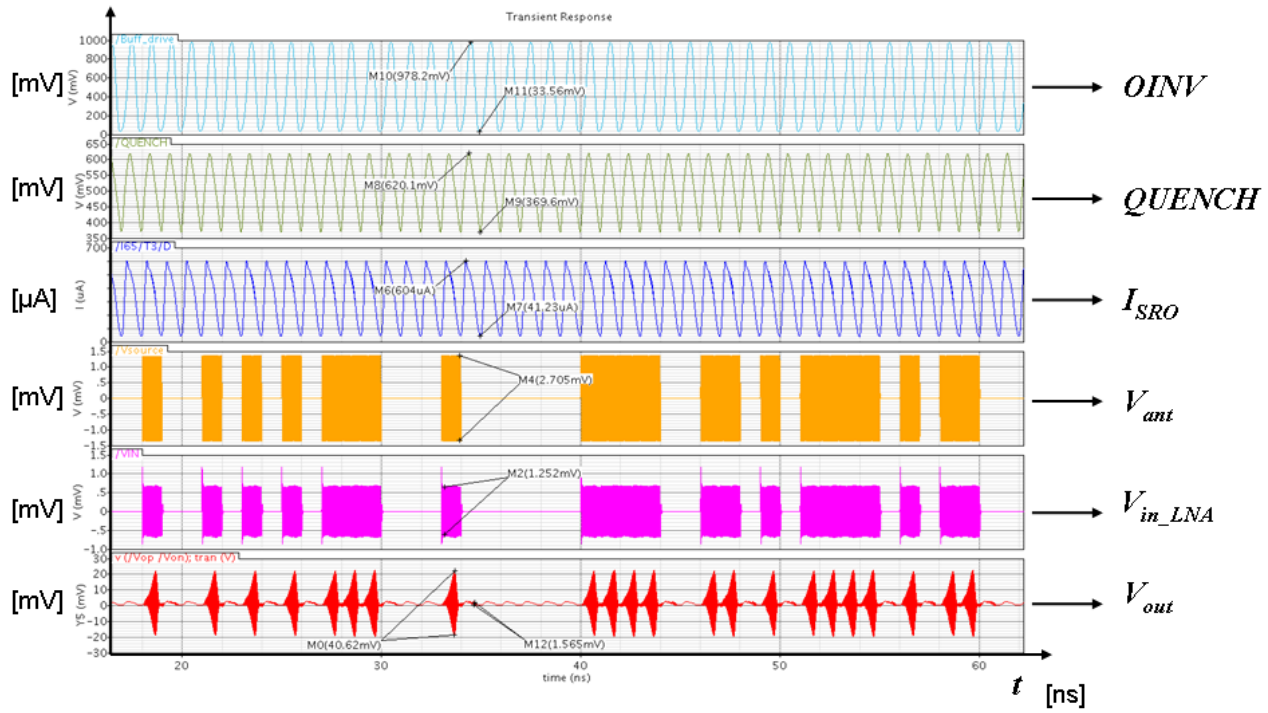


Figure 4.1: Waveforms of the Final SRR at 1 GHz.

In this chapter there will be a comparison between two circuits. The first that is just ideal and it is illustrated in Fig.4.1. It does not include the ring oscillator and in the SRO, $QUENCH$ and $OINV$ are driven using the same sinusoidal signal, having a DC component of

380 mV (V_{DCq}) and an AC component of 280 mV (V_{ACq}). The second one , instead, is the final version of my super-regenerative receiver, which has been introduced in the previous chapter (Fig. 3.1). In fact, during the design process, the ring oscillator has been the last block that

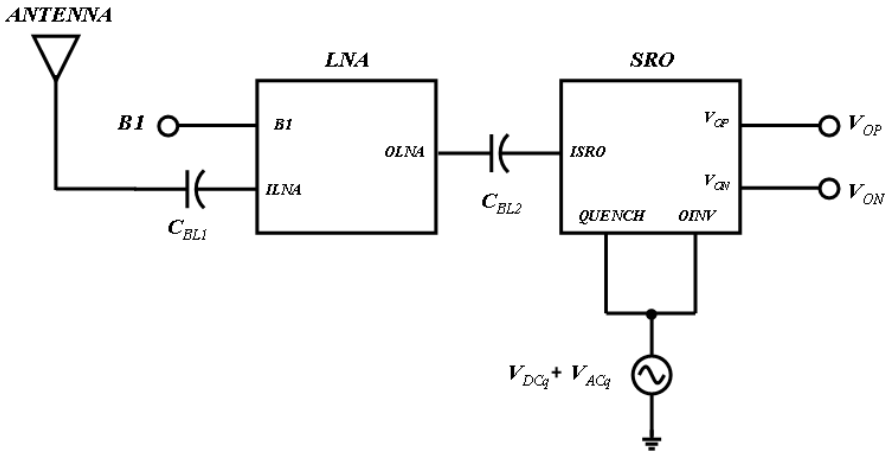


Figure 4.2: Ideal circuit without Ring Oscillator.

has been implemented, for the necessity to generate a real quench signal. Before of that, all the simulation have been done using an ideal sinusoidal $QUENCH$, that it could be easily changed.

4.1 Receiver Sensitivity and SNR

Another concept to introduce before starting with the illustration of the final results, is the receiver sensitivity. The receiver sensitivity indicates how faint an RF signal can be successfully received by the receiver. The lower the power level that the receiver can successfully process, the better the receiver sensitivity. For any given receiver, the higher the data rate, the less sensitive will be the receiver because more power is required to the receiver to support the higher data rate. The receiver sensitivity is expressed using the version of decibel employed in measurements of radio power, the dBm. In the dBm scale, 0 dBm equals 1 mW, and 30 dBm represents 1 W. In the measurements, to extrapolate the sensitivity of the receiver, four conditions have been fixed:

1. in the SRO, the bias current peak is synchronized with the center of the incoming bit (see Fig. 3.9);

2. the peak to peak variation of the differential output voltage ($(V_{OP}-V_{ON})_{pk-pk} = \Delta V_{out\_pk-pk}$)

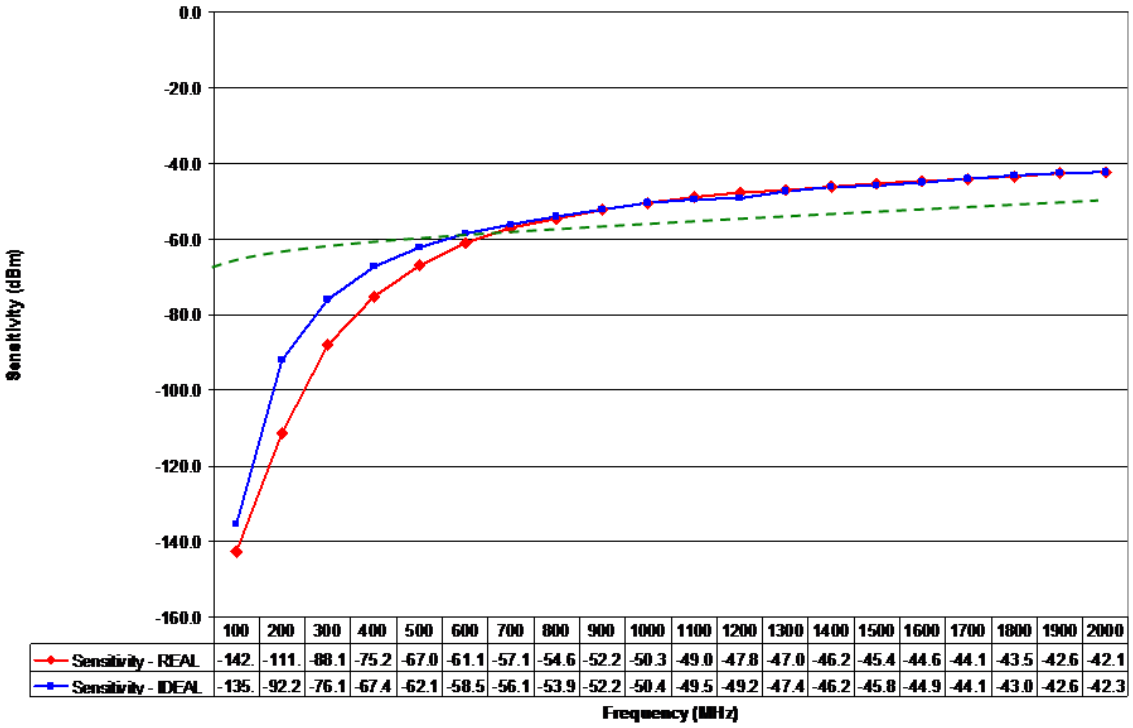
has to be 40 mV;

3. the ratio between the smallest output pulse which represents the bit "1", and the biggest output pulse which represent the bit "0", has to be greater than 10 dB (3.16).

Furthermore, results do not take in account any source of noise. Everything is ideal, and the receiver has been tested in these conditions to show the mechanism of the super-regenerative technique. The noise should be added in a second time, to understand how much the receiver performance could be gotten worse. But for now this part has not been studied yet. In presence of a "0", there could be present at the output a little pulse (see V_{out} in Fig. 4.1) that could be caused either by energy still stored in the tank after the stable phase of the SRO, or by energy coming from a too high value of the bias current peak during the unstable phase. Thus, the last condition represents a sort of output SNR (SNR_{out}).
The power to consider for the sensitivity is the amount of power that is going into the LNA. In presence of a perfect impedance matching at the input, half of the received power is dissipated into the antenna, which can be represented as an AC generator in series with a 50 Ω resistance. The other half goes inside the LNA. The rms (root-mean-square) value of a rectangular waveform is equal to its height, so, the sensitivity in a 50 Ω system is calculated as:

$$S = 10 \log \left(\frac{\left(\frac{V_{ant}}{2} \right)^2}{50} \times 1000 \right) \tag{4.1}$$

where V_{ant} is the rms value of the AM signal injected into the antenna, and 1000 is the number to multiply to have the dBm value (i.e., $1\,W = 1000\,mW$). In Fig.4.3 there is a comparison plot between the sensitivity using the ideal circuit, with the one using the final real circuit. The blue curve is for the ideal circuit, the red one for the real. The two cases are different just at low frequency. The real circuit is much more sensitive because, driving the ring oscillator, there is the possibility to generate a better $QUENCH$ signal for each frequency. In the ideal case, if fact, the $QUENCH$ is the same for the whole range of frequencies and it has been used to get good performance especially at high frequency. As it is shown in the picture, the same signal does not give the best performance at low frequency. Anyway, in both cases, at low frequency



	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
Sensitivity - REAL	-142.	-111.	-88.1	-75.2	-67.0	-61.1	-57.1	-54.6	-52.2	-50.3	-49.0	-47.8	-47.0	-46.2	-45.4	-44.6	-44.1	-43.5	-42.6	-42.1
Sensitivity - IDEAL	-135.	-92.2	-76.1	-67.4	-62.1	-58.5	-56.1	-53.9	-52.2	-50.4	-49.5	-49.2	-47.4	-46.2	-45.8	-44.9	-44.1	-43.0	-42.6	-42.3

Figure 4.3: Sensitivity vs. Frequency.

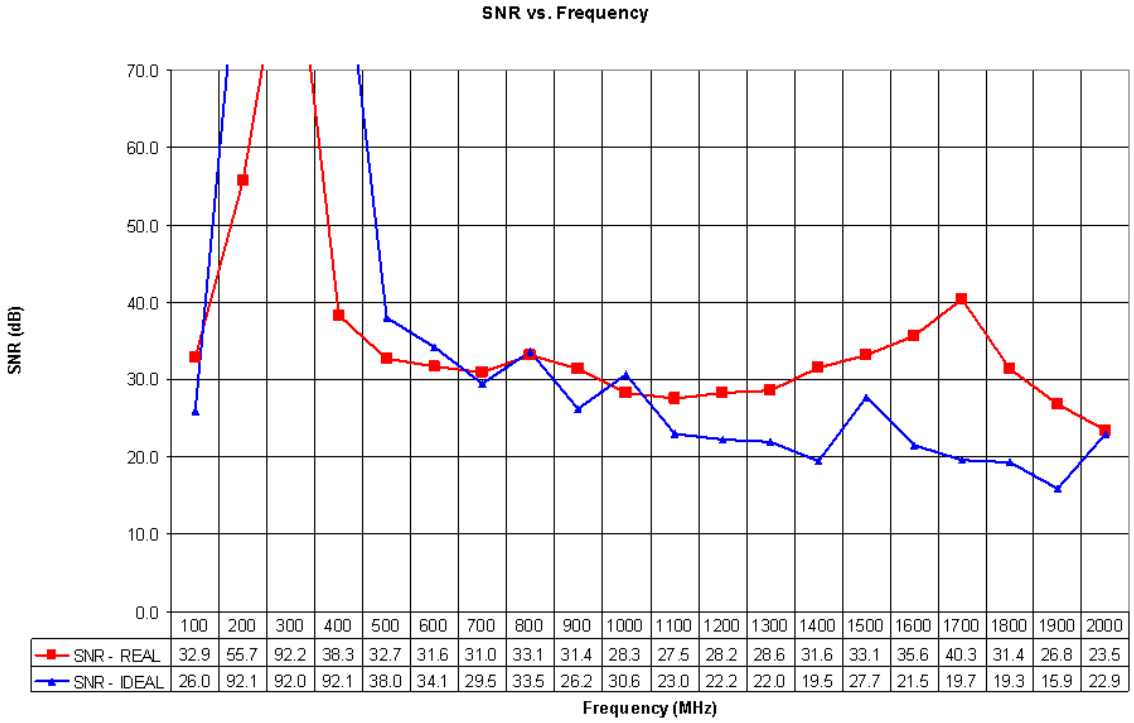
the circuit is really sensitive. Working at 100 MHz (or 100 $Mbps$) the sensitivity is

$$-142\ dBm = 6.31 \times 10^{-18} W = 6.31\ aW \qquad \longrightarrow \qquad V_{ant} = 32\ nV$$

This is the advantage of the super-regenerative receiver: starting from a signal in the antenna with a zero-peak amplitude of 32 nV, we get at the output of the SRO a pulse with a zero-peak amplitude of 20 mV. There is a total voltage gain of 625×10^3 or 115.9 dBV, with a power dissipation of just 2.51 mW. Taking a look at the output SNR[1], in Fig. 4.4, with the red curve we can see the results in real circuit, and with the blue one in the ideal. The first thing that we can observe is that at 300 MHz the SNR goes to infinity. In fact, in both cases, at this frequency the presence of a "0" bit in the output is represented as a perfect flat curve. It means that the SRO works perfectly. At higher frequencies, above 1 GHz, the real circuit works better.

So, at the end, working in the SRO with a bias current whom peak is synchronized with the center of incoming bit:

[1]To estimate the SNR_{out} I always considered a long series of random bits in output, and made the ratio between the smallest "1" and the biggest 0, as I already explained.



	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
SNR - REAL	32.9	55.7	92.2	38.3	32.7	31.6	31.0	33.1	31.4	28.3	27.5	28.2	28.6	31.6	33.1	35.6	40.3	31.4	26.8	23.5
SNR - IDEAL	26.0	92.1	92.0	92.1	38.0	34.1	29.5	33.5	26.2	30.6	23.0	22.2	22.0	19.5	27.7	21.5	19.7	19.3	15.9	22.9

Figure 4.4: SNR_{out} vs. Frequency.

- the real circuit has a better sensitivity below 1 GHz, and the same sensitivity above it;
- for the SNR, instead, the real circuit is working better below 1 GHz, and it is pretty simalr below it.

So, in general, the real synchronized super-regenerative receiver is working better.

If also the contribution of the thermal noise is considered

$$kT \longrightarrow -174\, dBm/Hz$$

where k is Boltzmann's constant and T the room temperature ($300\, K$), then I can estimate what is the minimum sensitivity that could be obtained in reality. The equation to use is

$$dBm(P_{in,min}) = -174 + 10\log(B) + dB(NF) + dB(SNR_{out_min}) \tag{4.2}$$

where B represents the band of the receiver. NF is the noise figure of the receiver and it can be estimates around 8 dBIn these systems, the SNR, is related to the BER (Bit-Error-Rate) which measures the ratio between errors and total number of bits. In this project SNR_{out_min} has to

be 10 dB, and we can suppose that with this value of SNR the BER is of 1×10^{-3} $err/bits$. The bandwidth of the receiver, as it has been explained in section 2.3.3, decreases when the quench frequency goes up. With a data bit rate of 100 MHz it could be of 1 GHz. Then,

$$dBm(P_{in,min}) = -174 + 90 + 8 + 10 = -66\, dBm$$

and this values should get worse increasing the quench frequency. Thus, in reality, just the presence in the system of the thermal noise will cause a big loss of sensibility at low frequency. An approximate dashed green line represents the realistic sensitivity of the receiver in Fig.4.3.

4.2 Voltage Gain and Energy Efficiency

Considering the ratio between the output zero-peak voltage and the input V_{ant}, a plot of the total voltage gain of the circuit can be drawn. From Fig.4.5 it is clear that at low frequency the gain is much much bigger, and it means that the super-regenerative technique is working pretty well. Considering that the gain coming from the LNA is about 10 dB, we can understand from this plot that the SRO is the heart of the circuit. It is the block which is dissipating less power (without considering the inverter), but in Fig.4.13 we can see how much it influence the total voltage gain of the circuit. Below 700 MHz , in fact, more than the 90 % of the voltage gain is coming from the LNA.

To estimate the total power dissipation of the circuit the average current of each block has been measured: LNA, SRO, RO, BUFFER and INVERTER. For the LNA the power consumption does not change working at different frequencies and it is equal to 1.53 mW. For all the other blocks, instead, the average current changes, increasing the working frequency (see Fig.4.7). The total power consumption is illustrated in Fig. 4.8.

From Fig.4.7, after the LNA, the biggest amount of power dissipation, above 700 MHz, is due to the ring oscillator. All the other block are dissipating almostly the same amount of power in the whole range of frequencies.

Another fundamental element that to consider communication, is the amount of energy used to receive (or transmit) one single bit. This energy is calculated with the following simple equation:

$$E_{bit} = \frac{Power}{Frequency} \tag{4.3}$$

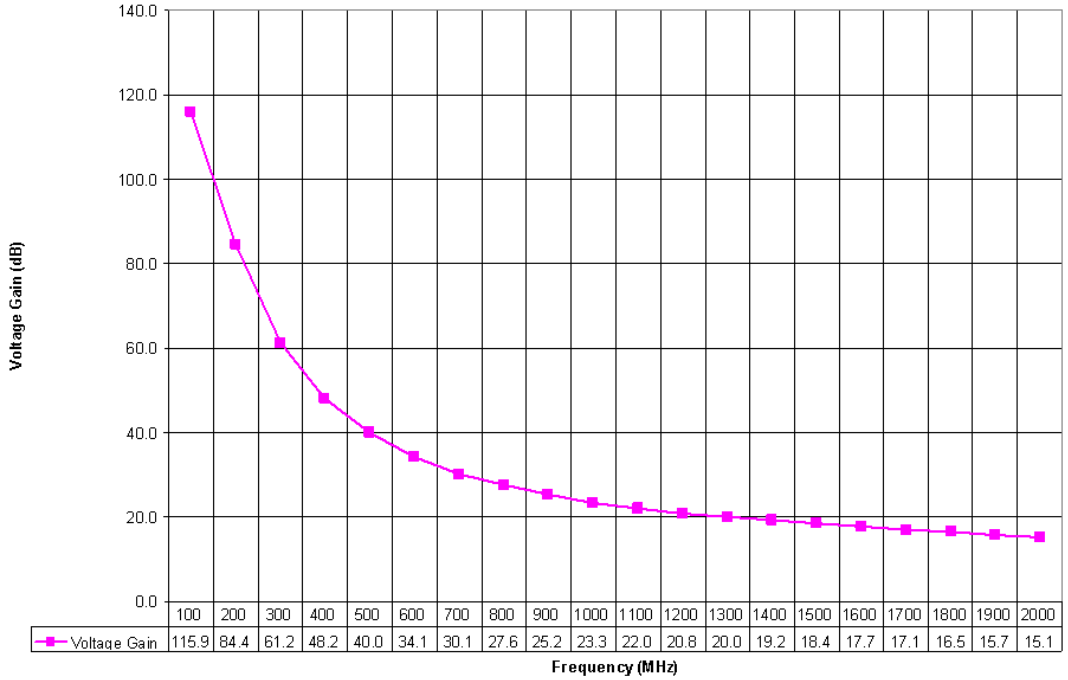


Figure 4.5: Voltage Gain vs. Frequency.

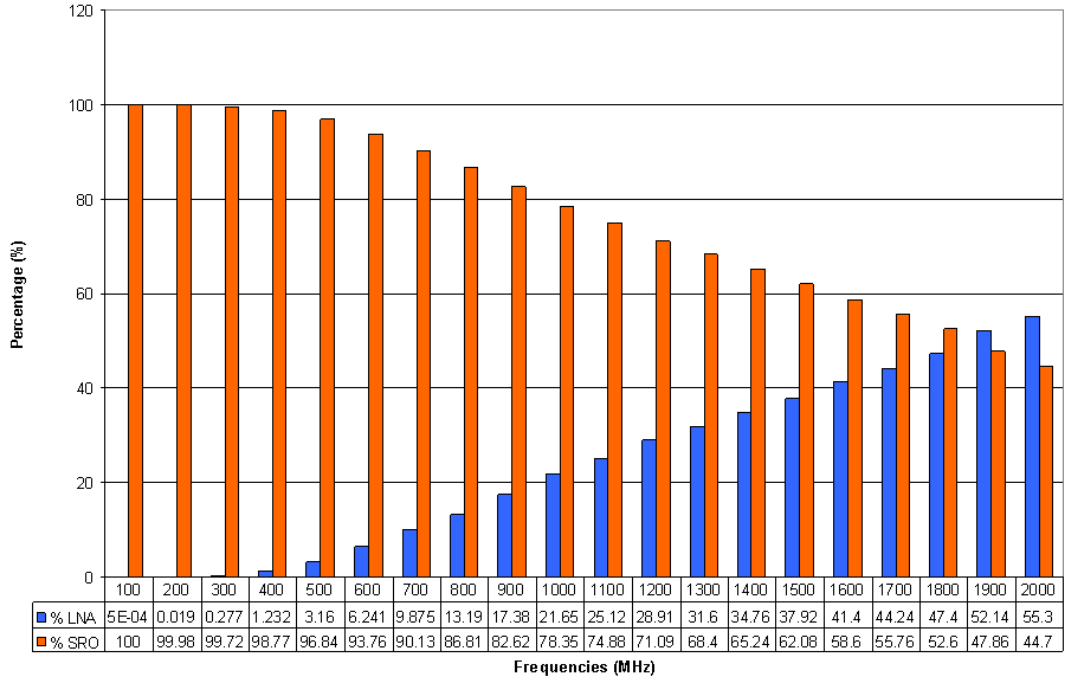
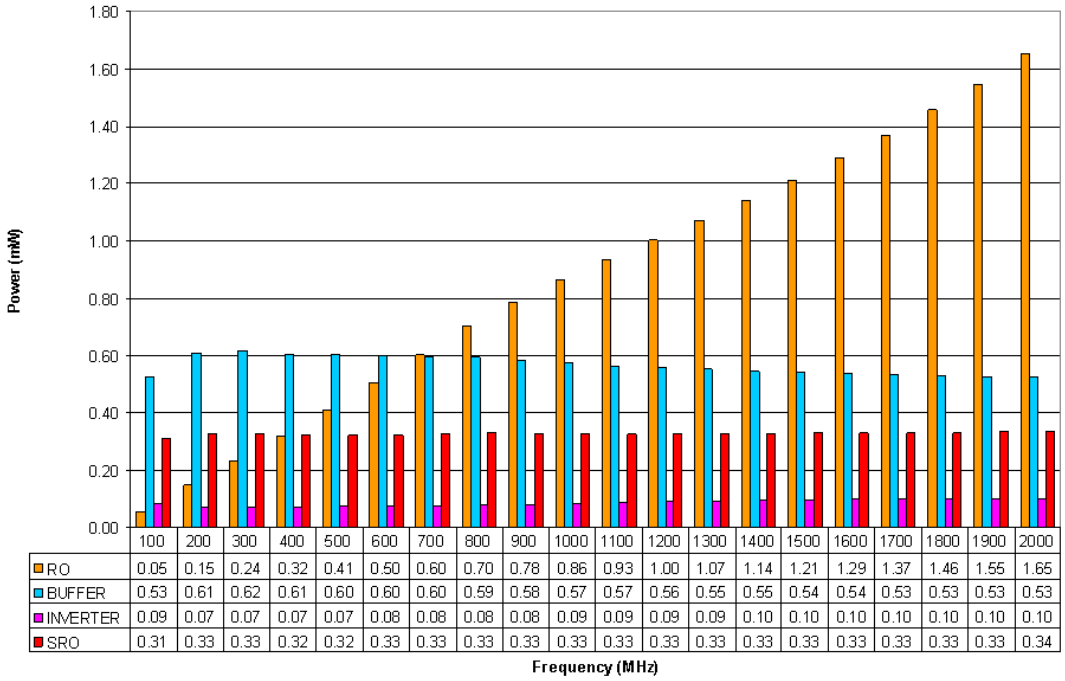
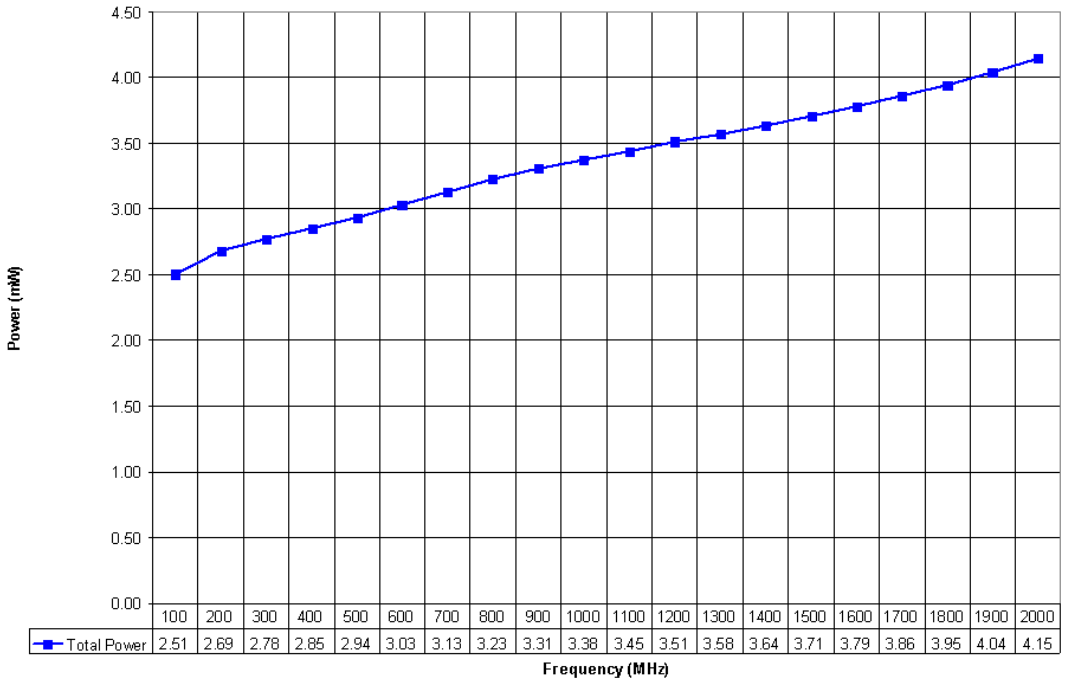


Figure 4.6: Percentage of Voltage Gain coming from the SRO and LNA vs. Frequency.



	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
RO	0.05	0.15	0.24	0.32	0.41	0.50	0.60	0.70	0.78	0.86	0.93	1.00	1.07	1.14	1.21	1.29	1.37	1.46	1.55	1.65
BUFFER	0.53	0.61	0.62	0.61	0.60	0.60	0.60	0.59	0.58	0.57	0.57	0.56	0.55	0.55	0.54	0.54	0.53	0.53	0.53	0.53
INVERTER	0.09	0.07	0.07	0.07	0.07	0.08	0.08	0.08	0.08	0.09	0.09	0.09	0.09	0.10	0.10	0.10	0.10	0.10	0.10	0.10
SRO	0.31	0.33	0.33	0.32	0.32	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.34

Figure 4.7: Power of each block vs. Frequency.



	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000
Total Power	2.51	2.69	2.78	2.85	2.94	3.03	3.13	3.23	3.31	3.38	3.45	3.51	3.58	3.64	3.71	3.79	3.86	3.95	4.04	4.15

Figure 4.8: Total Power vs. Frequency.

In Fig. 4.9 there is the plot which gives this information. The curve looks like a hyperbola.

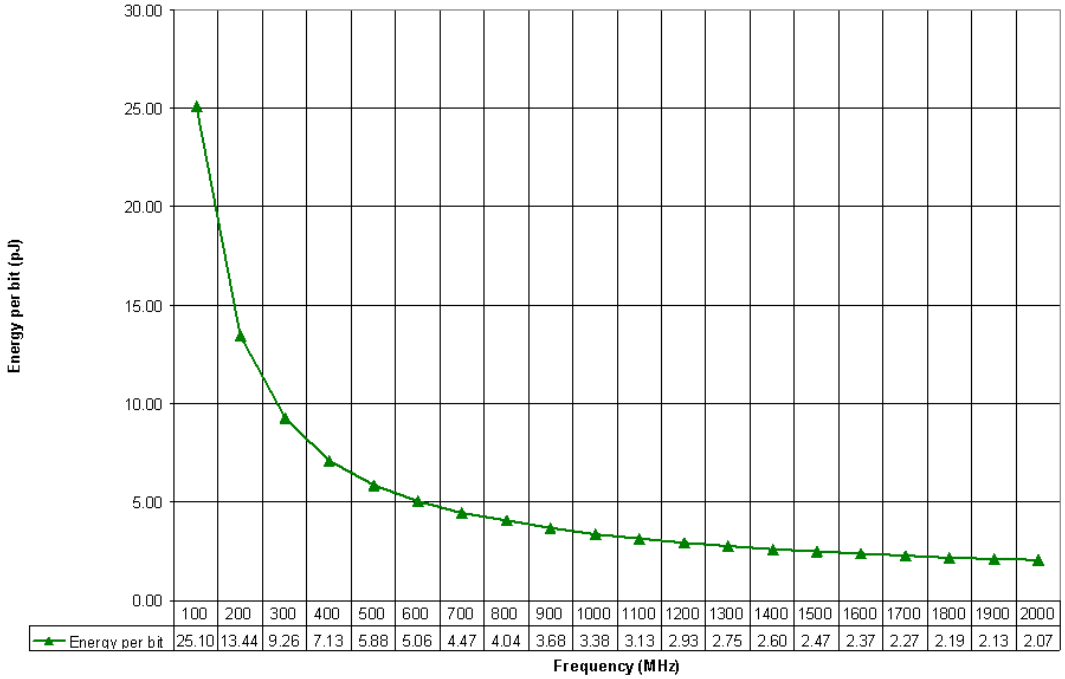


Figure 4.9: E_{bit} vs. Frequency.

The bigger the frequency, the smaller the energy per bit. For example, working at 100 MHz the power is really small, 2.51 mW, but the period of each bit is 10 times the period that the period at 1 GHz, and so, at the end, more energy is necessary just to send one bit. This is way this parameter is so important, because it shows how, in communication, the energy per bit is a more appropriate concept to use rather than power.

4.3 Why synchronization is so important in the SRO

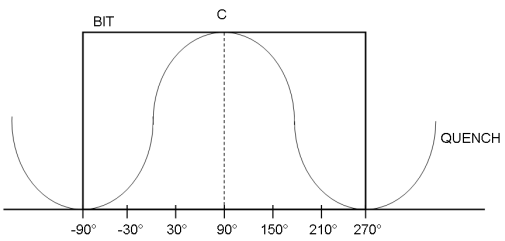
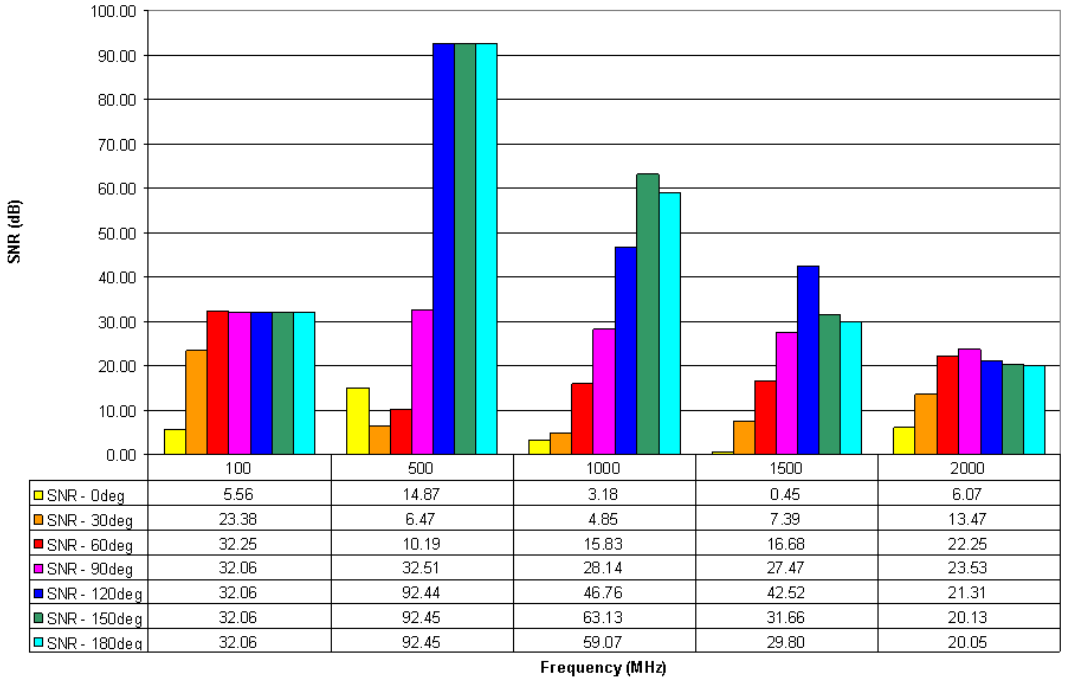


Figure 4.10: Synchronization of the $QUENCH$.



	100	500	1000	1500	2000
SNR - 0deg	5.56	14.87	3.18	0.45	6.07
SNR - 30deg	23.38	6.47	4.85	7.39	13.47
SNR - 60deg	32.25	10.19	15.83	16.68	22.25
SNR - 90deg	32.06	32.51	28.14	27.47	23.53
SNR - 120deg	32.06	92.44	46.76	42.52	21.31
SNR - 150deg	32.06	92.45	63.13	31.66	20.13
SNR - 180deg	32.06	92.45	59.07	29.80	20.05

Figure 4.11: How change the SNR synchronizing the quench signal in different ways.

As showed in section 2.3.3, to work in asynchronous mode, the quench signal should have a frequency that is a integer multiple of the data frequency. More than 4 four times bigger should be good. To get a maximum data frequency of 2 GHz, as it has been done in this project, the quench frequency should be 8 or 10 GHz, but at this point there would be two big problems:

- first of all, the operative frequency should increase. 24 GHz is too low, just 2-3 times the quench frequency. Furthermore, to change operative frequency is not achievable, because I should go up over 100 GHz, and with this technology it would not be possible;

- second problem is represented by the power dissipation. In the ring oscillator it goes up almost linearly with the frequency, so it means that the RO should dissipate 4-5 times more.

So, at the end, the only solution would be to decrease the maximum bit rate working below 500 $Mbps$.
Using the synchronization, instead, the circuit becomes much more complex, but higher frequencies can be reached. To show how much important is the perfect synchronization of the quench signal with data, a simple simulation has been run in Cadence. 5 frequencies have been

considered: $0.1 - 0.5 - 1 - 1.5 - 2\,GHz$; and the variation of the SNR_{out} changing the phase of the quench has been simulated. The graph in Fig.4.11 shows that:

- everytime the SNR is smaller than $10\,dB$ there is loss of information and the output sequence of pulses results wrong;
- 90^o phase-shift can be considered the average value, and using this synchronization good performance are always guaranteed;
- there is a window, between 90^o and 90^o, where the SNR gets better.

4.4 Output waveforms of the SRR

The following plots want to show how the SRR works at different frequencies. The only curiosity that needs a further explanation is referred to the Fig.4.12. When the bit rate is 100 MHz it is possible to observe at the input of the LNA some pulses. These peaks are to the output pulses of the SRO, which are going back through the LNA until the antenna. These pulses are visible just because the RF signal injected into the antenna is really small ($\approx 32\,nV$). In reality each pulse is about $62\,\mu V$, and considering that the output pulse is about $40\,mV$, it means that it has been attenuated of $56\,dB$. So the LNA is doing is job pretty well.

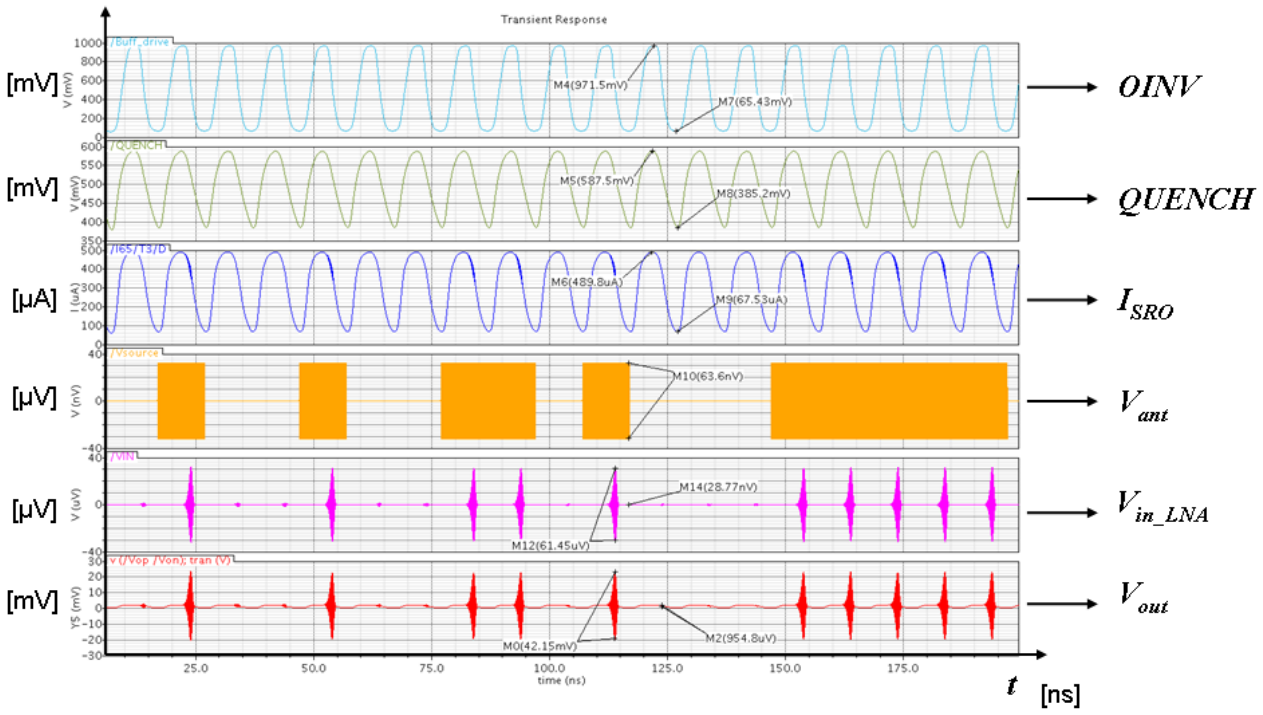


Figure 4.12: Output waveforms of the SRR at 100 MHz.

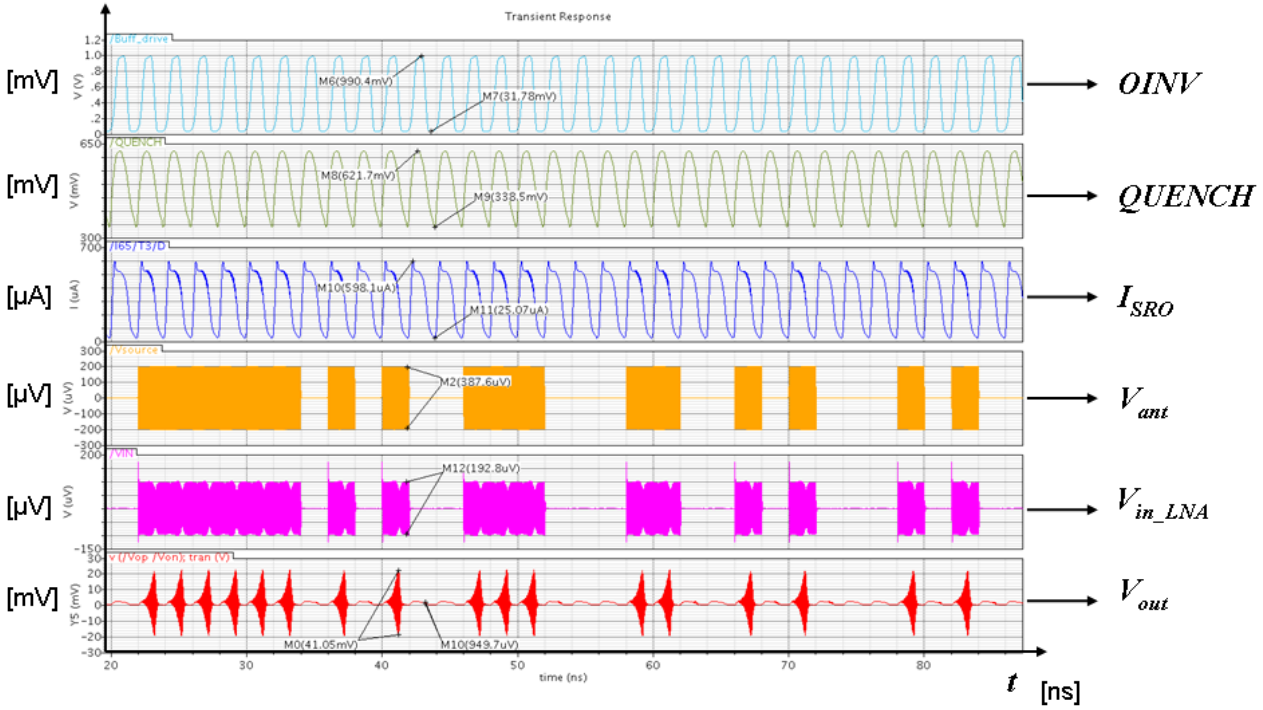


Figure 4.13: Output waveforms of the SRR at 500 MHz.

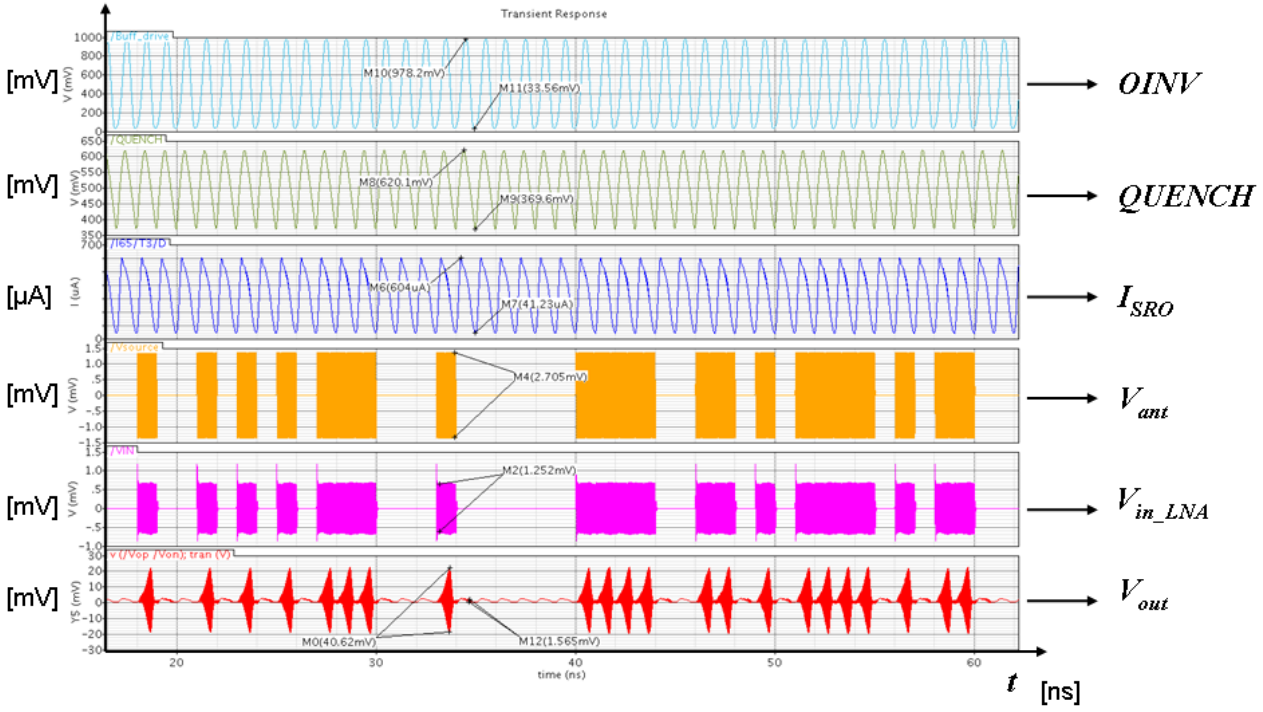


Figure 4.14: Output waveforms of the SRR at 1 GHz.

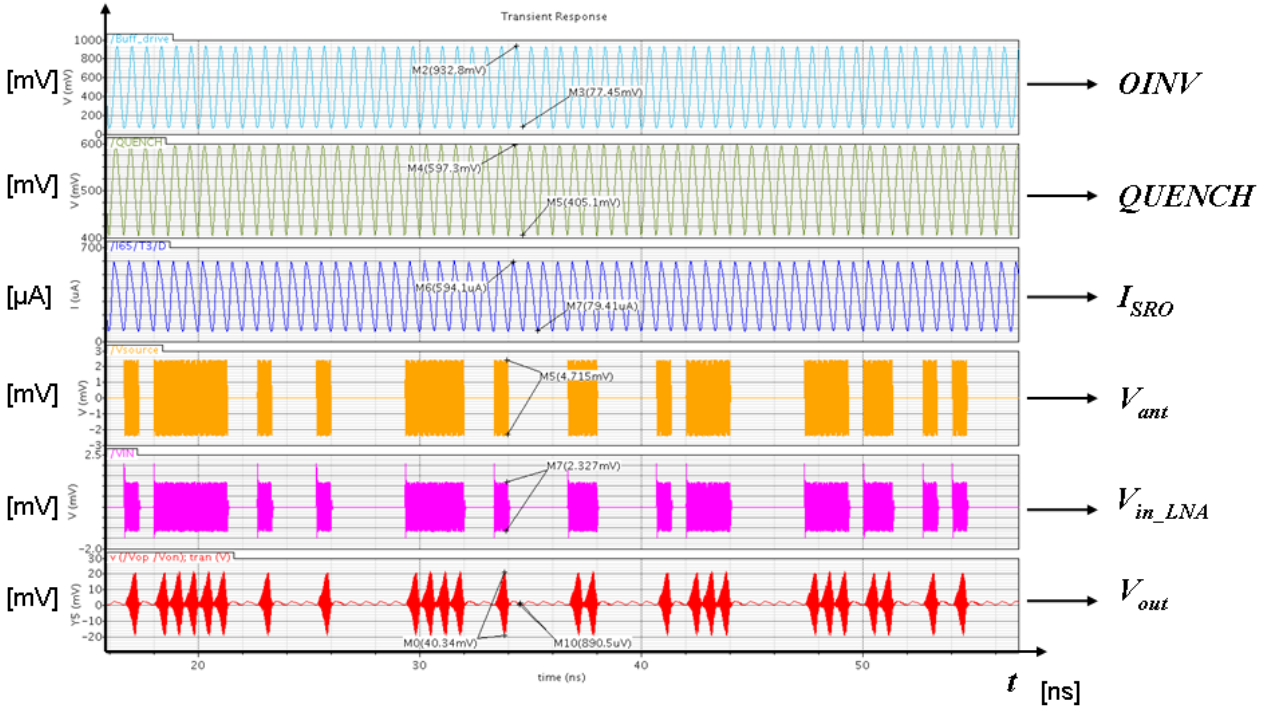


Figure 4.15: Output waveforms of the SRR at 1.5 GHz.

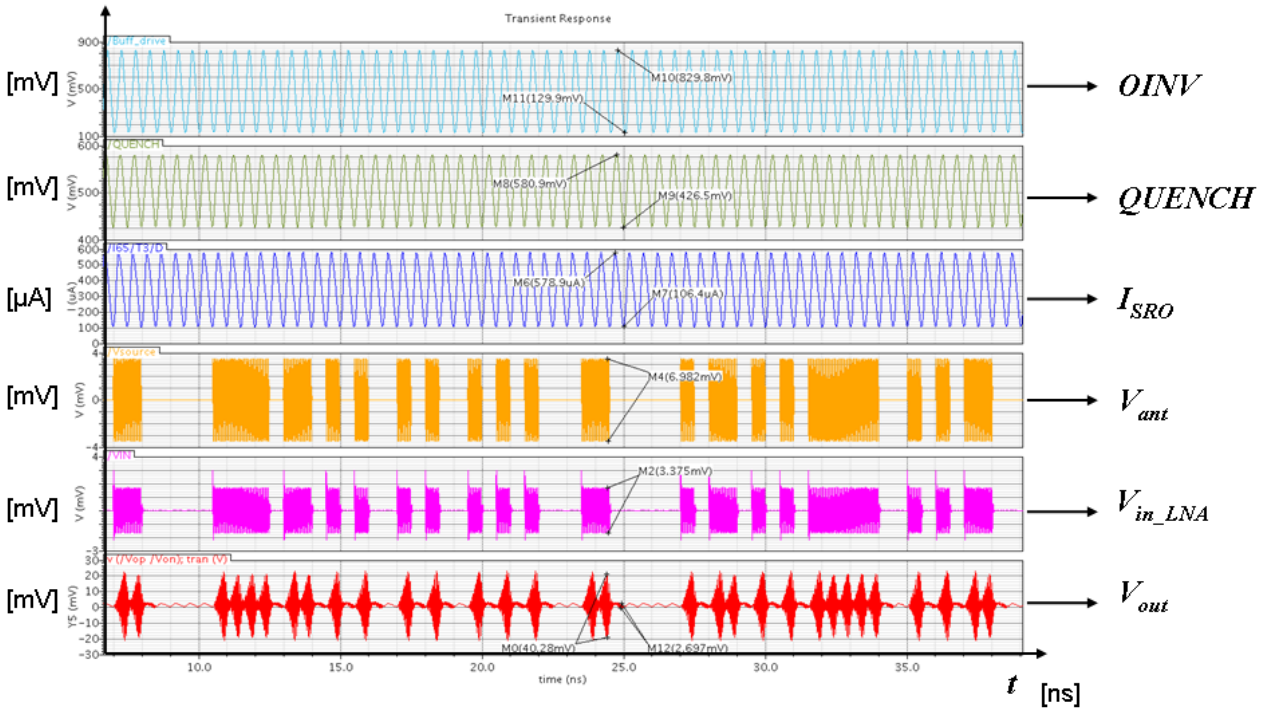


Figure 4.16: Output waveforms of the SRR at 2 GHz.

Chapter 5

Conclusions

At the beginning of this project the main goal it was to realize a super-regenerative receiver capable to work with a data bit rate of 1 $Gbps$, and an energy per bit smaller than 10 pJ/bit. The only way to get this performance it was using the synchronous version of the receiver. Indeed, with the asynchronous one, starting from the same circuit and the same technology, the maximum data rate can get four or five times worse. After this consideration, to get high performance, the closed-loop version of the SRR is the best circuit configuration to implement. Thus, the implementation of a PLL results fundamental to build a self-regulating circuit capable to synchronize incoming data with quench signal. Here, to design of the PLL has not been done, but using Cadence, it was possible to simulate the synchronous operating mode of the receiver the same. The implementation of the ring oscillator, which is driven by four current controllers, it gave the possibility to generate a real quench signal. A complete version of the super-regenerative receiver should also include an envelope detector after the SRO, to filter the information, deleting the carrier frequency from the output signal.

Then, another point is that, working at different frequencies, and without considering the noise, the sensitivity of the receiver drastically changes. Below 700 MHz it gets smaller than -60 dBm, so, if the input impedance of the receiver is perfectly matched with the antenna, it is sufficient to inject into the antenna a signal with a power smaller than 4 nW (450 μV), to obtain in the output a pulse with a zero-peak amplitude of 20 mV. With presence of thermal noise, instead, this performance cannot be reached, and the minimum value for the sensitivity can be estimated between -60 and -70 dBm. Thus, if the goal of the super-regenerative technique is to get a high voltage gain, maintaining a low power consumption, taking in consideration Fig.4.8 and

4.5, this goal is better achieved at low frequency, below 700 MHz, when the voltage gain starts to be bigger than 30 dB. Also the plot of the SRN in Fig.4.4, shows that the circuit is working pretty well between 200 MHz and 400 MHz. Increasing the frequency, instead, the receiver is still working well, and is still doing is job, but the voltage gain gets smaller and smaller below 30 dB. Thinking that, above 1 GHz more than one fifth of the gain is coming from the LNA, it means that the SRO is starting to lose is importance. This is principally due to the fact that, working at 1 GHz and more, each bit becomes shorter than 1 ns in time. It means that the period of the operating frequency (24 GHz) starts to be comparable with each bit, so when the oscillation starts in the SRO, during the unstable phase, it will have less and less time to grow up, and the only way to get an output pulse of 20 mV, it will be to have already a big RF signal at the input of the circuit (the sensitivity of the receiver becomes small). The main point is that, if the duration of the unstable phase of the SRR is much much bigger than the period of the operating frequency, the oscillation has much more time to grow up; and because of the fact that it grows up exponentially, the total voltage gain and the sensitivity of the circuit can improve a lot.

In conclusion, the final circuit works well and the obtained data bit rate is twice bigger than desired. At 1 GHz the sensitivity is -49 dBm, and considering also the power dissipated into the ring oscillator, the total energy per bit is 3.38 pJ/bit.

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