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Design of a low noise amplifier for a X-band phased array radar system in SiGe BiCMOS technology

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Alla mia famiglia,
con immensa gratitudine.

Contents

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ABSTRACT

Digital-processing systems require interfaces to the analog world. A Low Noise Amplifier (LNA) is the first active stage of a radio frequency receiver module, with the prevalent goal of minimizing the noise figure of the whole system. In fact, the key performance issue for a low noise amplifier is to deliver the undistorted but amplified signal to the signal-processing unit while adding a minimal amount of noise.
Firstly, this work presents a review of the figures of merit of a low noise amplifier and the design philosophy to give the reader some background into typical performance measures. A brief overview of different architectures is carried out: it investigates the best circuit solutions considering the specific field of application. Silicon-germanium (SiGe) technology is discussed, evaluating its physical characteristics and its potential. The main purpose of this work is the design of a linear low noise amplifier as the first stage of a X-band phased array radar system, using the SiGe BiCMOS technology of Infineon Technologies. The gain, noise figure, linearity, input matching, reverse isolation and stability of the amplifier operating at 10 GHz are investigated using Spectre, ADS and Sonnet simulators and the results are compared with the target specifications. Two slightly different topologies with inductive degeneration are implemented, in order to optimize the noise performance of the amplifier. The designed structures have a differential topology and they are linked to an output buffer, with a 3.3V supply voltage and an ESD protection system. At the operating frequency, the first low noise amplifier proposed has a S11 value of -19.5 dB, a gain of 18.6 dB, a noise figure NF=1.88 dB, and an IIP3=-2.1 dBm, with a power consumption of 60 mW for the core. Maintaining the same power consumption, the second inductive degeneration topology presents a S11=-15.6 dB, a gain of 18.8 dB, a noise figure NF=1.65 dB, and an IIP3=-1.2 dBm at the operating frequency.
In addition, a wide-band amplifier is analyzed and implemented, evaluating the differences between a narrow-band and broad-band low noise amplifier design. A transimpedance stage with ESD protection is considered. At the operating frequency of 10 GHz, it shows: S11=-12.1 dB, S21=11.3 dB, and NF=3.1 dB. Although at 10 GHz the noise performance of the wide-band amplifier is lower compared to the case of a narrow-band solution, with this structure the input matching (S11<-10 dB) is obtained within a frequency range from 2.8 GHz to 14 GHz.
The analysis and the optimization of the low noise amplifiers are examined and described in detail. The full-custom layout, including parasitic extraction, of each discussed circuit is also presented.

Chapter 1

Introduction

1 Presentation

1.1 Motivation

During last decades, an extraordinary development of radio frequency apparates has taken place and by now satellites, radars, mobile phones and many others electronic devices are part of our daily life. However, behind each of these wireless communication services there are circuits which have taken years of research and investments by many companies around the world. The growth of the telecommunications industry has been driven by continued demand for increasingly efficient products, and the result is their very stringent performance requirements. Hence, these transmission and reception systems have to be implemented optimizing the most important figures of merit for the specific field of application. A typical block diagram of a radio frequency transceiver structure used for wireless communication is shown in Fig. 1.1.

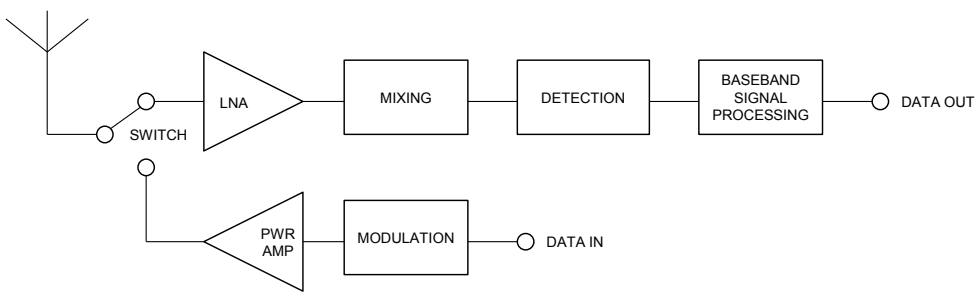

Figure 1.1: Radio frequency transceiver

Considering Fig. 1.1, the transmitter is made of the modulator and power amplifier blocks, while the low noise amplifier, mixing block, detection circuitry, and baseband signal processor make the receiver. The purpose of the receiver front-end, which consists of the low noise amplifier and the mixing system, is to amplify the weak signal received from the antenna and convert the carrier frequency down to a range that is more easily processed. Finally, detection and baseband signal processing techniques are dependent on the type of transmission modulation. The first stage of a receiver is typically a low noise amplifier, whose main function is to provide enough gain to overcome the noise of the subsequent stages, but, at the same time, low power consumption and high linearity are always the design targets.
The need to transmit high power to far distances in the desired direction, and to improve the receiver sensitivity, increases the number of antenna elements which are used in phased array antenna systems. A phased array antenna is composed of lots of radiating elements each connected to a phase shifter. Beams are formed by shifting the phase of the signal emitted from each radiating element, to provide constructive and destructive interference, steering the beams in the desired direction. Military systems require high power transmission, therefore these systems are highly expensive. However, phased array systems for civil applications are focused on reducing costs, improving the efficiency by implementing transceiver modules with affordable integrated circuit technology. In particular, phased array radar systems are playing an increasingly important role in every day life.
The elementary radar system consists of a transmitter unit, an antenna for emitting electromagnetic radiation and receiving the echo signal, an energy detecting receiver, and a processor. The following Fig. 1.2 illustrates this kind of system.

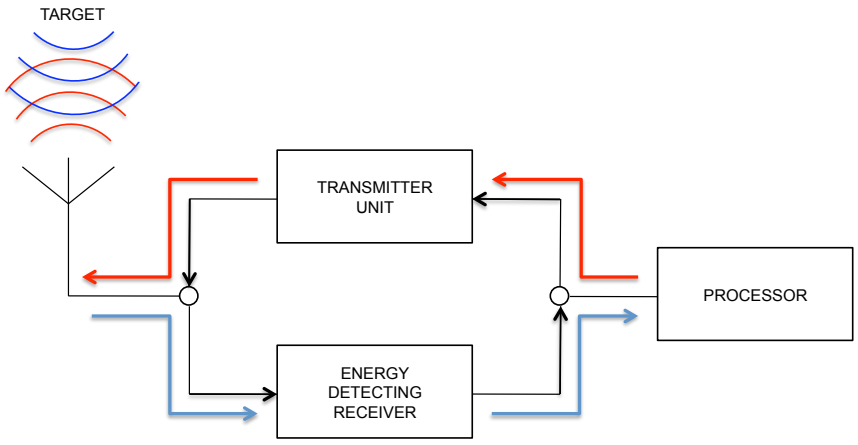

Figure 1.2: Radar system

A portion of the transmitted signal is intercepted by a reflecting object and it is reradiated in all directions. The antenna collects the returned energy in the backscatter direction and it delivers the signal to the receiver. The distance to the receiver is determined by measuring the time taken for the electromagnetic signal to travel to the target and back.
To understand the importance of developing a complete radar system, and implementing each functional block, the main fields of application are listed below.

- *Automotive*
  The applications of radar in the automotive area are manifold. They are concerned with security systems, adaptive cruise control, headway alert, collision warning, mitigation and brake support [1].

- *Air Traffic Control and Air Navigation*
  Radar is used to provide air traffic controllers with position and other information on aircraft flying within their area of responsibility. High resolution radars are used in airports to monitor aircrafts and ground vehicles. In addition, the weather avoidance radar is used on the aircrafts to detect and display areas of heavy precipitation and turbulence [2].

- *Ship Safety*
  It is one of the least expensive, most reliable and largest applications of radar. Radar is found on ships and boats for collision avoidance and to observe navigation buoys, especially when the visibility is poor [3].

- *Imaging*
  Imaging radar systems are attractive for a wide variety of commercial and scientific appliciations like nondestructive testing, material characterization, security scanning, and medical screening [4].

- *Space*
  The large ground radar bases are used for detection and tracking of satellites. Radars are also used for rendezvous and docking and they were used for the landing on the moon [5].

- *Military*
  Radar is an important part of air-defence systems. It performs the functions of surveillance and weapon control. Surveillance includes target detection, target recognition, and target tracking [6].

1.2 Objective

Considering the concepts presented in the previous paragraph, the aim of this thesis is to design a X-band ($8 \div 12\,\text{GHz}$) low noise amplifier intended for phased array radar systems, using the SiGe BiCMOS technology of Infineon Technologies.
The transceiver module is the heart of a modern phased array radar system. This module exists at each antenna element and it independentely controls the amplitude and the phase of the radar signal of each element in the array. The extreme level of control allows the antenna beam pattern to be changed dynamically and the resulting beam can be actively scanned. The transceiver module integrates an electronic phase shifter, a pre-amplifier and a power amplifier, a low noise amplifier, the limiter, and a circulator. All the components are assembled in one single module, typically realized using a monolithic microwave integrated circuit. In Fig. 1.3, the block diagram of a typical transceiver module of a phased array radar system is shown.

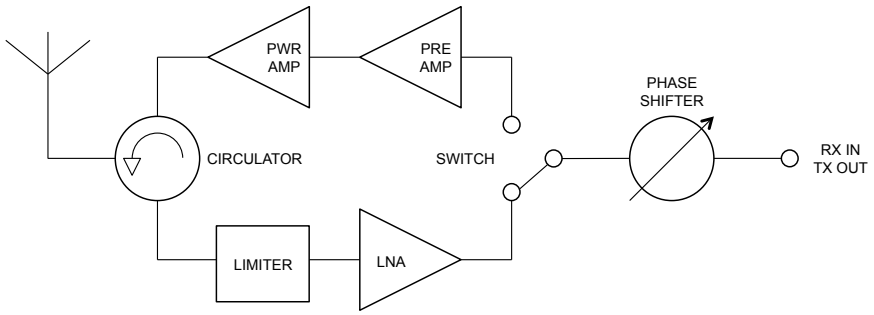

Figure 1.3: Radar transceiver module

The circulator is the element which allows the antenna to be shared between the transmitter and the receiver. A limiter is added between the antenna and the low noise amplifier, with the aim to reduce very strong incoming signals from jammers or large targets close to the radar and to protect the receiver against circulator failure. The low noise amplifier sets the noise figure of the system, but all losses between the antenna and this functional block add to the overall noise figure and they have to be minimized. In order to maximize the sensitivity of the transceiver module, every effort is made to locate the first low noise amplifier and the power amplifier as close as possible to the antenna to minimize attenuation of long transmission lines. The phase shifter supplies the incremental phases to each element. Since the phase shifting is required in both transmit and receive operations, the phase shifter is a passive reciprocal device. Finally, the pre-amplifier

and the high-power amplifier are often the biggest and most expensive parts of this module. The radar receiver is required to amplify the received signals without adding too much supplementary noise or introducing any form of distortion, to optimize the probability of detection of the signal, to provide a large dynamic range and to reject interfering signals, so that the required information can be optimally detected. Thus, the low noise amplifier becomes a critical block for the entire system.
In the design of a low noise amplifier, there are common goals that the designer should take care of. These are: minimizing the noise figure, obtaining the maximum possible gain with enough linearity, stability, impedance matching at the input and output terminals. All these design targets cannot be considered separately, so it is useful to specify the importance of each one to perform the best tradeoff between the figures of merit. Tab. 1.1 illustrates the tentative target specifications for the X-band phased array low noise amplifier discussed in this thesis.

f [GHz]	**S11 [dB20]**	**S21 [dB20]**	**NF [dB10]**	**IIP3[dBm]**
10	< -10	> 15	< 2	> -5

Table 1.1: Target specifications

Considering the targets summarized in Tab. 1.1, they are intended in a bandwidth of 2 GHz with a central frequency of 10 GHz, thus in the frequency band $9 \div 11$ GHz. Even if they are not explicitly specified, also the parameters S22, which is the output reflection coefficient, and S12, the reverse transmission coefficient, should assume sufficiently low values.
The SiGe BiCMOS technology is a silicon-based technology that takes advantage of the maturity of the silicon processing techniques and results into very low cost components, because it allows to improve the performance of the devices, while maintaining the conventional CMOS manufacturing process. Hence, SiGe HBT BiCMOS technology is chosen here for implementing the monolithic transceiver modules required for X-band phased array radar applications.

1.3 Literature review

Before evaluating the specific design of a low noise amplifier, the typical fields of application of a phased array radar system are taken into consideration, to understand the importance of these systems in everyday life. Some information on this kind of system are available in [1], [2], [3], [4], [5], and [6].
The design of an electronic system starts by defining target specifications and methods used to evaluate the performance. The first part of this work has the purpose to explain the main figures of merit to consider during the design of a low noise amplifier. In [7] an evaluation of the distortion in transistor circuits is presented and the parameters used to measure the linearity are introduced. In particular, the minimum value of the IIP3 is usually defined by the specification on the linearity of the desidered low noise amplifier. Another important figure of merit, especially for a low noise amplifier, is the noise figure, a concept introduced by H. T. Friis in [8], which is related to the signal noise ratio at input and at output of the system to analyze. Gain, noise and linearity are the most important features of a low noise amplifier, as its purpose is to feature high gain and low noise. However, there are tradeoffs between these parameters: optimizing one of them may worsen another feature. Hence, the design should focus on the most important specifications.
The significant interaction between devices and circuit determines the importance of the fabrication technology on the device characteristics and the final implemented system. For this reason, it is important to investigate the technology used to develop the low noise amplifiers presented in this work, the SiGe BiCMOS technology. In [9] the development of the bipolar transistor is discussed, from its invention to the most advanced versions. The SiGe technology is obtained by adding germanium to the base of the bipolar transistor. A brief review of the history of this technology is presented in [10] and a detailed review of SiGe epitaxial base technology can be found in [11] and [12]; in particular, in [11] the requirements and processes for high-quality SiGe film preparation are discussed, with an emphasis on fundamental principles, while [12] is focalized on process integration and on some device structures. The evaluation of the SiGe BiCMOS technology, the frequency behavior of the devices, and a study of their models gives some more insight to be used during the analysis of the circuits here presented. More details about the specific SiGe technology and the European $Dotfive$ project can be found in [13], [14], and [15].
The design of a low noise amplifier has to consider the purpose of the circuit and its application. In fact, there are several options and degrees of freedom, it can be either single-ended or differential, single-stage or multi-stage. For example, the

single-ended low noise amplifier architecture has at least one important shortcoming, the sensitivity to parasitic ground inductance. A differential topology can solve this problem, but for the same total power consumption the noise figure of a differential solution is usually higher than its single-ended counterpart. A multistage low noise amplifier may achieve a higher gain, but it is more difficult to guarantee its stability. The criteria for choosing between different options depends on the application and on the specific design requirements. From an architecture point of view, in the literature most of the low noise amplifiers intended for phased array radar systems are designed using an inductive emitter degeneration. A single-ended structure is often implemented. In accordance with the desired performances of the system, it is possible to design the circuit evaluating the appropriate frequency response, with a narrow-band or a wide-band topology. In particular, in the case of a narrow-band solution, it is important to understand the effect of the emitter degeneration, as explained in [16], where the effects of resistive, capacitive and inductive degeneration for single-ended and differential circuit topologies are analyzed. The operation frequency of the circuit affects the complexity of the system: at high frequencies parasitics become significant. Important references about the study of devices and amplifiers are reported in [17], [18] and [19].
Electrostatic discharge (ESD) has become one of the most important reliability issues in integrated circuit products and the design has to take it into consideration. A reference for the study of this topic is in [21], where the use of diodes and inductors is discussed to realize some ESD protection topologies. In particular, in this work the Human Body Model (HBM) is considered [20].
In the design of narrow-band low noise amplifiers, inductive degeneration solutions are pursued. The references used in this work are [22], [23], [24], [25], [26], [27], and [28]. In particular, references [23] and [24] study the optimal bias current and sizing of the devices in order to obtain the best noise performance and the impedance and noise matching at the input of the system. In [22], an ESD protection network based on inductors is introduced. This approach is used in this work to propose a low noise amplifier topology without any series base inductor, which is the primarily responsible of the degradation of the noise performance. In addition, some results to compare the proposed solutions can be found in [29], [30], [31], [32], [33], [34], [35], [36], [37], and [38].
Considering an electronic circuit, resistors are sources of thermal noise, hence their use has to be minimized. On the other side, inductors are commonly used in integrated circuits, but large chip areas are required, increasing the cost of fabrication. The quality factor Q is the most important parameter of an inductor and it speci-

fies the performance of the device [39]. Today's inductors are fabricated using the top metal level. The layout parameters, such as metal width, metal spacing, number of turns, and metallization thickness are the main features in the design and fabrication process of an inductor. A careful design of the inductors is necessary to minimize the amplifier noise; some references are available in [40] and [41].
Wide-band amplifiers are important functional blocks in wireless communication systems as well as in microwave communication systems and instrumentation. There are two main design approaches to obtain wide-band low noise amplifier realizing the input matching: using a bandpass filter concept or implementing a resistive feedback technique. Resistive feedback is generally considered inferior, because it degrades the gain and noise figure. However, a proper study of the shunt-shunt resistive feedback can minimize the noise contribution without affecting gain and matching. The main key advantage of a resistive feedback low noise amplifier is offered by the area savings, because there are not on-chip spiral inductors. In this thesis, the design of a transimpedance amplifier is presented, and also in this case a tradeoff between the figures of merit has to be considered. The references considered during the design of the wide-band low noise amplifier here presented are [42], [43], [44], [45], while [46], [47], [48], [49], [50], [51] are used to compare the obtained results.

2 Figures of merit

In a receiver, a low noise amplifier is used principally to overcome the noise of subsequent stages. The main specifications of a low noise amplifier are noise figure, gain, bandwidth, linearity, power consumption, input and output matching. It has already been noticed that it is not possible achieve highest gain, lowest noise figure and lower power consumption at the same time, but there are always tradeoffs between the specifications. The analysis of an electronic system has to consider the figures of merit which characterize each functional block, with the purpose to guarantee the respect of the given specifications. Hence, the following subsections have the purpose to remind the definitions of these parameters.

2.1 Gain

One of the most basic parameters for an amplifier is its gain. It is important to know which kind of gain is considered. In the radio frequency field, power gain is commonly used. It is defined as the ratio between the power delivered to the load and the available power from the source. Other times it is prefered to use the voltage gain, the ratio between the output and input voltage. Then, it is possible to consider the following expressions:

$$Power\ Gain \rightarrow G = \frac{P_{OUT}}{P_{IN}} \rightarrow G_{dB} = 10log(G) \tag{1.1}$$

$$Voltage\ Gain \rightarrow G = \frac{V_{OUT}}{V_{IN}} \rightarrow G_{dB} = 20log(G) \tag{1.2}$$

The power or voltage gain of a single block depends not only on the characteristics of the functional block, but also on the input and output impedances. If the matching conditions between cascaded blocks are guaranteed, the gain of the system formed by the cascade of the blocks is given by:

$$G_{tot} = G_1 * G_2 * ... * G_N \rightarrow G_{tot_{dB}} = G_{1,dB} + G_{2,dB} + ... + G_{N,dB} \tag{1.3}$$

2.2 Linearity

The distortion is a phenomenon related to the fact that the amplifiers contain non linearities, which origin spurious frequency contributions. Any difference in the shape of the input and the output waveforms versus time, not considering scaling factor, is called distortion. Complete and depth analitycal analysis about distortion for a single transistor, differential pairs and single stage amplifiers are available in [7]; in the following, the purpose is to briefly present the figures of merit to consider with the aim to measure the distortion in a generic system.
The spurious harmonics can be calculated using a Taylor series expansion around the operating point. Imposing $x(t) = Acos(\omega t)$ as the input of the amplifier, its output $y(t)$ can be expressed as function of $x(t)$ by the power series indicated in (1.4).

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ... \tag{1.4}$$

The coefficient α_0 represents the dc component of output signal, α_1 is the linear gain of the system, whereas α_2, α_3, ..., describe the distortion of the system. Remembering the trigonometric relations $cos^2x = \frac{1}{2}(1+cos2x)$ and $cos^3x = \frac{1}{4}(3cosx+cos3x)$, and replacing the definition of $x(t)$ in (1.4) truncated at the third order, the output signal $y(t)$ becomes:

$$\begin{aligned} y(t) &= \alpha_1 A cos(\omega t) + \alpha_2 A^2 cos^2(\omega t) + \alpha_3 A^3 cos^3(\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left[\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right] cos(\omega t) + \frac{\alpha_2 A^2}{2} cos^2(2\omega t) + \frac{\alpha_3 A^3}{4} cos(3\omega t) \end{aligned} \tag{1.5}$$

In (1.5), the terms with the same frequency of the input determine the fundamental tone, while the other terms are harmonics due to the non linearity of the system. From (1.5), the second order distortion causes a dc offset, while the third order distortion produces a gain variation. It is interesting to notice that at the fundamental frequency the term $\alpha_3 A^3$ can be neglected compared to $\alpha_1 A$, if the amplitude of the input is sufficiently small.

Harmonic Distortion

A figure of merit to evaluate the non linearity of a system is the harmonic distortion. The distortion is measured considering the ratio between the i-th harmonic power and the fundamental tone power. Thus, it is possible to introduce the second-order and third-order harmonic distortion parameters:

$$HD_2 = \frac{second\ harmonic\ amplitude}{fundamental\ amplitude} = \frac{1}{2}\frac{\alpha_2}{\alpha_1}A \tag{1.6}$$

$$HD_3 = \frac{third\ harmonic\ amplitude}{fundamental\ amplitude} = \frac{1}{4}\frac{\alpha_3}{\alpha_1}A^2 \tag{1.7}$$

It is also possible to evaluate the total harmonic distortion THD, considering the contribution of all harmonics, as indicated in (1.8):

$$THD = \frac{\sqrt{\Sigma_i (n-th\ harmonic\ amplitude)^2}}{fundamental\ amplitude} \tag{1.8}$$

Intermodulation

If the interest is to quantify the effects to the output of two input tones, with the amplitudes A_1 e A_2 (generally $A_1 = A_2$), at frequencies f_1 and f_2, respectively, the appropriate solution is a two-tone test. At the output, harmonic components arise at all combinations of $\omega_1 = 2\pi f_1$ and $\omega_2 = 2\pi f_2$, and their multiples. Imposing the input signal $x(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$ and replacing in (1.4), we get:

$$\begin{aligned} y(t) &= \alpha_1[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)] + \alpha_2[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)]^2 + \\ &= +\alpha_3[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)]^3 + \alpha_4[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)]^4 + ... \end{aligned} \tag{1.9}$$

Then, expanding the second term of (1.9), we obtain:

$$\begin{aligned} \alpha_2[A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)]^2 = \alpha_2 \frac{A_1^2}{2} [cos(2\omega_1 t) + 1] + \alpha_2 \frac{A_2^2}{2} [cos(2\omega_2 t) + 1] + \\ + \alpha_2 A_1 A_2 [cos[(\omega_1 + \omega_2)t] + cos[(\omega_1 - \omega_2)t]] \end{aligned} \tag{1.10}$$

The reader can observe the creation of second-order terms for each input, a dc offset and harmonics at sum and difference frequency. This is true for all even order distortion; for example, a fourth order intermodulation generates tones at $2\omega_1 + 2\omega_2$ and $2\omega_1 - 2\omega_2$. Hence, it is possible to evaluate the intermodulation products. The second-order intermodulation distortion (IM_2) is defined as the ratio between the component at frequency $\omega_1 \pm \omega_2$ and the one at ω_1 or ω_2, imposing $A_1 = A_2 = A$:

$$IM_2 = \frac{\alpha_2 A^2}{\alpha_1 A} = \frac{\alpha_2 A}{\alpha_1} = HD_2 + 6dB \tag{1.11}$$

In the same way, considering the third term in (1.9), the intermodulation products at frequencies $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ are obtained, defining IM_3:

$$IM_3 = \frac{\frac{3}{4}\alpha_3 A^3}{\alpha_1 A} = \frac{3}{4}\frac{\alpha_3}{\alpha_1} A^2 = HD_3 + 9.5dB \tag{1.12}$$

Clearly, to be able to measure the intermodulation tones, harmonics produced by the distortion have to fall in the frequency band of the system. Positioning the tones at the edge of this band, intermodulation tone at difference frequency, related to even distortion, is close to dc, while odd distortion components are close to the two test tones. Fig. 1.4 illustrates the harmonic components for a two tones test, with fundamentals at ω_1 and ω_2.

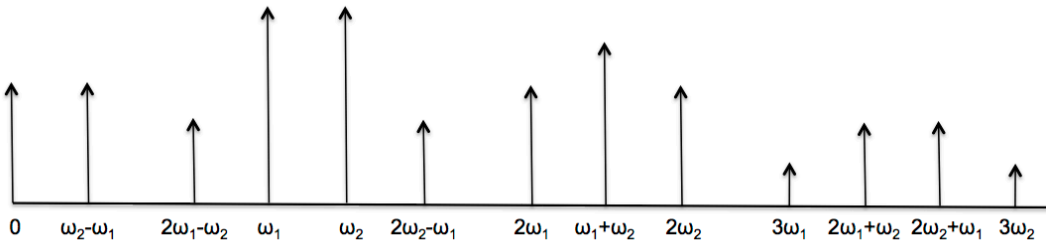

Figure 1.4: Two tones test

1dB compression point

The 1 dB compression point is defined as the input signal level which decreases by 1 dB the gain at the fundamental frequency. Considering the expression (1.5), with low amplitude levels the term $\alpha_1 A$ dominates, but as the input signal increases, the $\frac{3\alpha_3 A^3}{4}$ term becomes more significant and the amplifier begins to compress (α_3 is generally negative). When the sum of the two terms is 1 dB smaller than the first term alone, the 1 dB compression point is reached; in this analysis it is assumed that the effect of higher-order terms is not significant.

Intercept Points

The intercept points are another way to characterize the distortion. The intercept point is the signal level at which the intermodulation distortion is unity. In the third-order case:

$$\alpha_1 A = \frac{3}{4}\alpha_3 A^3 \rightarrow IIP3 = \sqrt{\frac{4}{3}\frac{\alpha_1}{\alpha_3}} = \frac{A}{\sqrt{IM_3}} \rightarrow IIP3_{dB} = A_{dB} - \frac{1}{2}IM_{3dB} \quad (1.13)$$

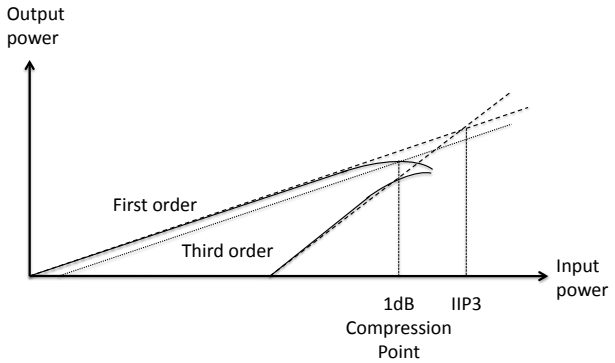

Figure 1.5: 1 dB compression point and IIP3

2.3 Noise figure

In electronic circuits, noise is represented by any random interference unrelated to the signal of interest. The main types of noise can be listed as follow:

- *Thermal Noise*
  The random thermal movement of electrons in resistive materials creates thermal noise, which is white noise and it can be minimized by keeping the temperature low and the bandwidth as smaller as possible.

- *Shot Noise*
  This is white noise generated by random release of electrons or by the random passage of electrons and holes across a potential barrier.

- *Burst Noise*
  This type of noise is related to the presence of heavy-metal ion contamination. It also can be caused by a monolithic impurity in a pn junction.

- *Flicker Noise*
  This is caused mainly by traps associated with contamination and crystal defects. Its effect decreases at high frequencies.

The most widely used parameter to quantify the noise performance of a system is its noise figure, which has been introduced by H. T. Friis in 1944 [8]. The noise figure is a measure of how much a device degrades the Signal to Noise Ratio (SNR). Considering the SNR at the input and the SNR at the output of a system, the noise figure NF is defined as indicated in (1.14):

$$NF = \frac{SNR_{input}}{SNR_{output}} = \frac{S_i/N_i}{S_o/N_o} \tag{1.14}$$

In (1.14), S_i is the input signal power, S_o is the output signal power, N_i is the noise power due to the source, and N_o is the total output noise power including the circuit noise contribution and noise transmitted from the source. For an ideal noiseless amplifier $S_0 = GS_i$ and $N_o = GN_i$, where G is the power gain of the system. Hence, it is possible to consider the noise contributions of an amplifier N_{iamp} at the input, as indicated in Fig. 1.6.

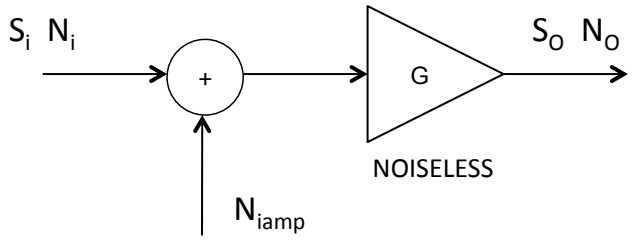

Figure 1.6: Equivalent noise circuit

Now, replacing the expression (1.14), it is possible to obtain the following result:

$$NF = \frac{S_i}{N_i}\frac{N_i + N_{iamp}}{S_i} = 1 + \frac{N_{iamp}}{N_i} \tag{1.15}$$

From (1.15), it is clear that the noise figure is more than one and it depends on the noise of the source and on the noise of the amplifier (referred to the input). Considering a cascaded system, the relationship between the overall noise figure and the noise figure of each stage, characterized by a power gain G_i, is given by:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + ... + \frac{NF_n - 1}{G_1 G_2 ... G_{n-1}} \tag{1.16}$$

An important consequence of this formula is that the overall noise figure of a radio receiver depends mainly on the noise figure of the first amplifier stage. Subsequent stages will have a relatively minor effect on the SNR of the whole system.

2.4 S-parameters

In order to realize the impedance matching between the antenna and the low noise amplifier, as well as between the low noise amplifier and the subsequent block, matching networks are generally implemented, using active and passive components. The S-parameters allow to evaluate the input and output matching. Considering the two-port network of Fig. 1.7, its scattering matrix, related to the incident and reflection waves a_i and b_i, is defined.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2=0} \qquad S_{12} = \frac{b_1}{a_2}\bigg|_{a_1=0} \qquad S_{21} = \frac{b_2}{a_1}\bigg|_{a_2=0} \qquad S_{22} = \frac{b_2}{a_2}\bigg|_{a_1=0}$$

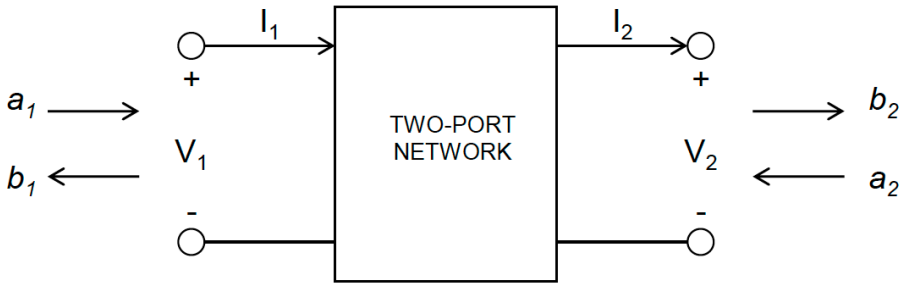

Figure 1.7: S-parameters

In particular, S11 and S22 are the reflection coefficients at port 1 and port 2, respectively, while S12 and S21 are the transfer coefficients between the two ports. Thus, if the interest is in the input and output matching of a block, the reflection coefficients, the ratio between reflected and incidented wave, have to be considered.

2.5 Stability

To check the stability of a functional block, several methods can be used. A common method considers the scattering matrix and two coefficients K_f and b_{1f}:

$$K_f = \frac{1 - |S11|^2 - |S22|^2 + \Delta^2}{2|S12S21|} \tag{1.17}$$

$$b_{1f} = 1 + |S11|^2 - |S22|^2 + \Delta^2 \tag{1.18}$$

$$\Delta = S11S22 - S12S21 \tag{1.19}$$

A specific block is unconditionally stable if $K_f > 1$ and $b_{1f} > 0$. These parameters indicate if the stability has been reached, but not if a functional block is more or less stable than another one or how to realize the stability condition. Finally, if the complete system is considered, it is not possible to say if it is stable or not only looking at the stability of each single block.

3 SiGe BiCMOS technology

A knowledge of the technology used to fabricate integrated circuits is important for several reasons. The advancement of the technology has become indispensable because it provides the advantage of the planar process to fabricate complex circuits at low cost. Since integrated circuit technology presents a completely different set of cost, the optimum choice to solve a given design problem and realize a specified function requires a knowledge of the factors influencing the cost.
Analog integrated circuits are designed in bipolar technology, CMOS technology, and technologies that combine both types of devices. The necessity to associate digital functions on the same integrated circuit with analog functions has resulted in an increasing use of CMOS technologies for analog integrated circuits. However, bipolar technology is now used, and it will continue to be used, in a wide range of applications requiring high-current drive capability and high levels of analog precision performance. Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) are becoming increasingly popular because of their advantages over conventional silicon and GaAs transistors, requiring less power and giving greater functions with fewer chips at higher frequencies. Finally, BiCMOS technology offers bipolar devices for radio frequency and analog functions and CMOS transistors for the ever-increasing digital interface requirements. Thus, by using SiGe BiCMOS technology, radio frequency front-end, baseband, and digital signal processing circuits for telecommunications systems can be integrated together on the same chip. In this section, a review of bipolar transistors and relatively recent technologies are presented, focusing on heterojunction bipolar transistors and BiCMOS technology. However, for obvious reasons related to the industrial know-how, it is not possible to analyze in detail the specific SiGe BiCMOS technology used in this work.

3.1 Bipolar transistor

Compared to CMOS devices, bipolar transistors exhibit higher transconductance per bias current, faster switching speeds, and excellent properties for many analog applications. At a basic level, the bipolar transistor consists of two pn junctions, with a base made as thin as possible. In fact, considering a npn bipolar transistor, if the base region is thin enough, the base current consists primarily of the back-injected hole current from base to emitter, while the electrons from the emitter do not have sufficient time to recombine in the base.
For small signal applications, the transconductance g_m is probably the most important parameter to consider of a bipolar transistor. It is defined as:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{\partial}{\partial V_{BE}} I_S e^{\frac{V_{BE}}{V_T}} = \frac{I_C}{V_T} \tag{1.20}$$

From (1.20), the transconductance depends linearly on the bias current. The transit frequency f_T is another parameter to consider in a bipolar transistor. It is defined as the frequency at which the small signal current gain (considering a shortcircuit load) drops to unity. Thus, it is a measure of the maximum useful frequency at which a transistor can be used as an amplifier. The small signal current gain $\beta(f)$ at high frequencies is defined in (1.21):

$$\beta(f) \simeq \frac{g_m}{j\omega(C_\pi + C_\mu)} \tag{1.21}$$

Therefore, from (1.21), considering $|\beta(j\omega)| = 1$, it is possible to derive the expression of the transit frequency f_T:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{1.22}$$

This transit frequency f_T can be expressed as a function of the transit time $\tau = \tau_b + \tau_c + \tau_e$, the average time taken by the minority carriers to cross the quasi-neutral region, as indicated in (1.23):

$$f_T = \frac{1}{2\pi\tau} = \frac{1}{2\pi(\tau_b + \tau_c + \tau_e)} \tag{1.23}$$

Another more important figure of merit is the maximum oscillation frequency f_{max}. It is the frequency at which power gain is 1, indicating the maximum frequency at which useful power gain can be expected from a device. The maximum oscillation frequency f_{max} is related to the transit frequency f_T and its definition is shown in (1.24), where R_b is the base resistance:

$$f_{max} = \sqrt{\frac{f_T}{2\pi R_b C_\mu}} \tag{1.24}$$

Equations (1.23) and (1.24) show that the frequency response of a bipolar transistor is determined by the intrinsic speed of the carriers through the device, as well as the parasitic resistances and capacitances of the transistor. So, the base width can be made very small to increase the intrinsic frequency response. Since the base

contact is physically removed from the active base region, a significant series ohmic resistance is observed between the contact and the active base. This resistance can have a significant effect on the high frequency gain and on the noise performance of the device. Transistors designed for low noise and high frequency applications, where low base resistance is important, have a double or triple base contact. Thus, considering the desidered noise performance for the low noise amplifiers described in this work, the signal transistors are designed with two or three base strips, with the aim to reduce the base resistance, and then the overall noise figure.

3.2 SiGe Heterojunction Bipolar Transistor

The heterojunction bipolar transistor differs from the traditional homojunction transistor because one of its two junctions is formed between different semiconductor materials. In particular, in SiGe HBTs germanium is added to the base of the bipolar device. In a homojunction bipolar transistor the emitter doping is selected to be much greater than the base doping, with the aim to obtain an emitter injection efficiency close to unity. Hence, the base is relatively lightly doped while the emitter is heavily doped. Considering (1.23), the transit frequency f_T of a device is also limited by τ_b, the time required for minority carriers to cross the base. In radio frequency applications, it is important to maximize the transit frequency to obtain excellent performance. Thus, to increase f_T, the base width has to be reduced. However, the base doping is fixed to maintain a constant emitter injection efficiency, with the result to increase the base resistance. In addition, this base resistance forms a time constant with base-emitter dynamic capacitance, limiting the speed of the device. Therefore, a tradeoff between high transit frequency and low base resistance has to be evaluated. One way to overcome this tradeoff is to add some germanium to the base of bipolar transistors to form heterojunction transistors. The key idea is that the different materials on the two sides of the junction have different band gaps. In particular, the band gap of silicon (1.12eV) is greater than for germanium (0.66eV), and, forming a SiGe compound in the base, the band gap is reduced in this region. The relatively large band gap in the emitter can be used to increase the potential barrier for holes, which can be injected from the base back to the emitter. Therefore, this structure does not require an emitter doping much greater than the base doping for a unity emitter injection efficiency. Then, the emitter doping can be decreased and the base doping can be increased, allowing to obtain low base resistance even when the base width is reduced to increase transit frequency. In addition, the width of the base-collector depletion region is reduced in the base when the transistor operates in the forward

active region, decreasing the effect of base width modulation and increasing the Early voltage of the device. Finally, decreasing the emitter doping, the width of the base-emitter depletion region in the emitter increases, reducing the junction capacitance between base and emitter and increasing the maximum speed of bipolar device. Hence, SiGe heterojunction transistors offer three key advantages over the conventional bipolar transistors:

- A reduction in base transit time resulting in higher frequency performance
- An increase in collector current density, allowing high current gain with low intrinsic base resistance
- An increase in Early voltage

On the other side, the advantages of heterojunction bipolar transistors over homojunction devices come at the price of an increased complexity of fabrication, which also increases the costs.

3.3 BiCMOS Technology

Until relatively recent years, it has been necessary to use many technologies to design a radio frequency transceiver. For example, GaAs technology for power amplifiers, low noise amplifiers and other radio frequency components, but CMOS devices for the baseband operations. Hence, combining high speed HBTs with CMOS devices into a SiGe BiCMOS technology higher performance can be achieved.
BiCMOS technology is a combination of bipolar and CMOS technologies together on a single process. Bipolar process gives high speed and low noise transistors. On the other hand, CMOS technology is more suited for digital circuits. The integration of bipolar and CMOS technologies is advantageous when it is used to optimize microelectronics circuits for different applications such as telecommunications, mixed-signal, and radio frequency apparates.
In conclusion, it is possible to summarize the advantages of BiCMOS technology:

1. *Good performance in analog applications*
   - High analog precision components
   - Well controlled device characteristics

2. *Good performance in digital applications*
   - Accurate digital control
   - Availability of small size devices

3. *High-speed performance*
   - Very low transit time
   - Parasitic resistances and capacitances minimized
   - Advanced processing to minimize the size

4. *Good power switching performance*
   - Low series resistance
   - High breakdown voltage
   - Good performance with high currents

In the light of the foregoing discussion on BiCMOS technology, all circuits described in this work are designed in a BiCMOS SiGe process of Infineon Technologies similar to that described in [13], [14], and [15], with a transit frequency f_T, a maximum oscillation frequency f_{max}, and a gate delay of approximately 250 GHz, 350 GHz, and 2 ps, respectively. In addition, six metal layers, MIM capacitors, two different polysilicon resistors, and precision tantalum nitride resistors are available.

Chapter 2

Design

The aim of this chapter is to analyze the design of a low noise amplifier that satisfies the design specifications previously discussed. In particular, an inductive degeneration topology with a cascode stage is the most suitable solution for the purpose. In addition, the Electrostatic Discharge (ESD) protection is also implemented, allowing the analysis and the design of two slightly different low noise amplifiers. Specifically, first of all a typical low noise amplifier topology is presented, with a structure often considered in the literature. Then, another solution is analyzed with the goal of improving the performance. Furthermore, the study and the design of a transimpedance low noise amplifier with a resistive feedback network is also discussed, in order to obtain a structure with a wider input matching and gain bandwidth. The latter goes beyond the desire of a structure that complies with the discussed specifications, but it allows to assess the difference between narrow-band and wide-band solutions, which are used in different applications.

1 Design topologies

Evaluating the three basic amplifier configurations, common emitter, common base, and common collector, the first one is the only which offers both current and voltage gain. This is advantageous for a low noise design. Common base configurations offer low input impedance, but high output impedance. Shunt feedback can be used to reduce the output impedance, but it has limited applicability at high frequencies, because a high open-loop gain is required to obtain an adequate loop gain; multiple stages may also be considered, but stability issues generally limit the number of stages. Finally, common collector configurations are used at low frequencies, but at high frequencies the output impedance becomes inductive and the configuration is

prone to parasitic oscillations. For these reasons, common emitter configuration is preferred to realize a low noise amplifier, especially for high frequency applications. The dominant noise contributors are thermal noise due to the resistors and shot noise through pn junctions. Ideal reactive elements do not generate noise, but they may affect the overall noise performance, while resistive feedback adds additional noise sources and it is often avoided in low noise amplifier design. However, resistive feedback may be used to increase the linearity of the system, to set the gain and the input and output impedance over wide-bandwidths. In this work, considering the specifications, it is necessary to use reactive networks, to realize the input and output matching, remembering that the use of real reactive components degrades the noise performance. Thus, an accurate design of the inductors becomes necessary.
Before evaluating the specific design solutions, we present the classical low noise amplifier topologies, considering advantages and disadvantages of narrow-band and wide-band structures, the differences between single-ended and differential solutions, the effect of emitter degeneration, and the necessity to implement an electrostatic discharge protection.

1.1 Wide-band and narrow-band low noise amplifiers

A low noise amplifier can be designed adopting a wide-band or narrow-band topology, depending on the application and on the desired frequency response. This choice determines the design of the input matching network and each type of specified design has his own advantages and disadvantages. A narrow-band solution has a tuned input and output matching network, and it can reach good noise performance using less dc power than a wide-band topology. The main disadvantage is the difficulty to achieve bandpass amplification and input matching with an accurate center frequency. On the other side, a wide-band solution needs a flat frequency response and a larger input matching is paid in terms of a higher power consumption. Considering the specific phased array radar system, a broad-band system is not required, so it is desiderable to use narrow-band techniques for the low noise amplifier. Thus, an emitter degeneration structure is designed to generate a real term in the input impedance and to obtain the possibility to tune the amplifier. This is the most prevalent method used for SiGe HBT amplifiers, allowing to achieve the best noise performance.

1.2 Single-ended and differential solutions

A single-ended amplifier architecture has at least one important shortcoming compared to a differential topology. It is sensitive to parasitic ground inductance. Considering a common emitter structure, the ground return of the signal is supposed to be at the same potential of the emitter. However, there is inevitably a difference in these potentials because there is always some impedance between the two points. Hence, small amounts of additional parasitic reactance between the two grounds can have a large effect on the amplifier performance. In addition, a single-ended structure can be inclined to signal dependent currents from other stages, forming a parasitic feedback loop that destabilizes the amplifier. Dedicated additional ground pins can mitigate these problems, but generally a differential solution is preferred. In this way, any parasitic reactances in series with the bias current source is largely irrelevant. Another important attribute of the differential topology is its characteristic to reject common mode disturbances. This is particularly important at chip level, where both the supply and substrate voltages are noisy. Hence, the symmetry of the circuit is critical and it is the first target to be pursued during the layout realization. Finally, the power consumption is twice compared to a single-ended amplifier to achieve the same noise performance, but the linearity is improved.

1.3 Inductive degeneration

In many radio frequency building blocks, the common emitter configuration and the differential pair stage are commonly used. To improve the linearity of the structure, using a feedback solution, it is possible to add a degeneration emitter impedance Z_E, as shown in Fig. 2.1, where a single-ended stage is presented, but the discussion is easily extended to the case of a differential pair. As analyzed in the next paragraphs, this solution also allows to set the input impedance of the stage. As explained in [16], emitter degeneration can be resistive, capacitive or inductive, and stages with reactive degeneration have lower noise figure than those with resistive degeneration. In [16], it is possible to evaluate the procedure to find the expression of IM_3, which uses the Volterra's series. Considering the results of the single-ended model, the expression of the third order intermodulation IM_3 is reported in (2.1), allowing to quantify the linearity:

$$|IM_3| \propto 1 + sC_{be}Z_B(s) + sC_{be}Z_E(s) \tag{2.1}$$

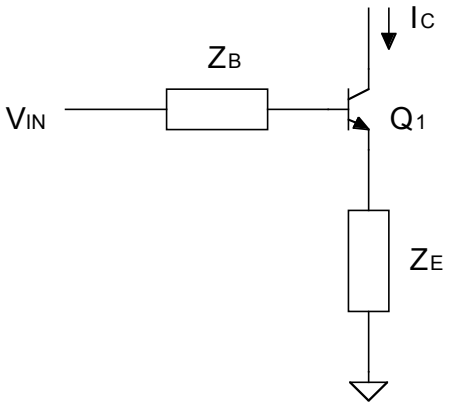

Figure 2.1: Emitter degeneration structure

Evaluating (2.1), where C_{be} is the base-emitter capacitance that includes also any external capacitance connected between the base and emitter terminals, with inductive degeneration the term $sC_{be}Z_E(s)$ is, for s=jω, real and negative, reducing the third order intermodulation. On the other side, capacitive degeneration would increase the intermodulation, because the term $sC_{be}Z_E(s)$ becomes a positive real number, for s=jω, which adds to the "1" term. It is also important to highlight that $|IM_3|$ directly depends on the base-emitter capacitance. Finally, in [16] it is also shown as the linearity depends on the third power of the ratio of the small signal transconductance to the bias current.

1.4 Electrostatic discharge protection

In the field of integrated circuits design there is a growing interest on the effects of Electrostatic Discharge (ESD) on chip performance. Electrostatic discharge problems are increasing in the electronics industry because of the trends toward higher speed and smaller device sizes, thus they have to be taken into consideration.
Static charge is an unbalanced electrical charge at rest. When this static charge moves from one surface to another, it becomes an electrostatic discharge, a miniature lightning bolt of charge that moves between two surfaces with different potentials. Thus, it becomes a current that can damage or destroy junctions, gate oxide, and metallizations in an integrated circuit. Only the HBM is considered here [20].
In the design of low noise amplifiers, the input pads are usually connected to the base terminals of the transistors, which leads to a very low electrostatic discharge robustness if no appropriate ESD protection is used. In the following, the goal is to introduce the reader to the main electrostatic discharge protection solutions for

integrated circuits, the same topologies adopted to prevent this kind of damage for the low noise amplifiers discussed in this thesis.
Diodes are commonly used for ESD protection. The conventional double-diode topology is shown in Fig. 2.2, where two diodes connected to the input pads are illustrated. If D_1 or D_2 are in the forward biased condition, they can provide efficient discharging paths from input pad to V_{DD} and from V_{SS} to input pad, respectively.

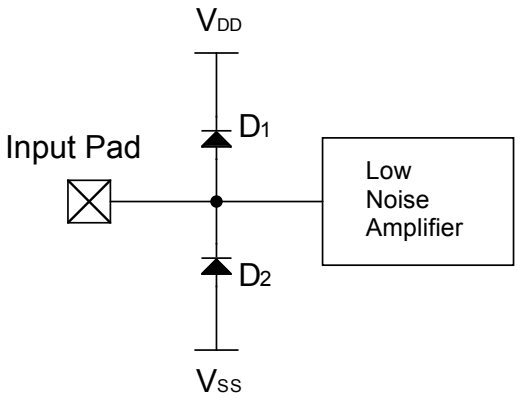

Figure 2.2: ESD protection diodes 1

The solution illustrated in Fig. 2.2 is adopted when the circuit has no internal ac coupling. Conversely, if the circuit is internally coupled, the solution generally adopted for electrostatic discharge protection is shown in Fig. 2.3.

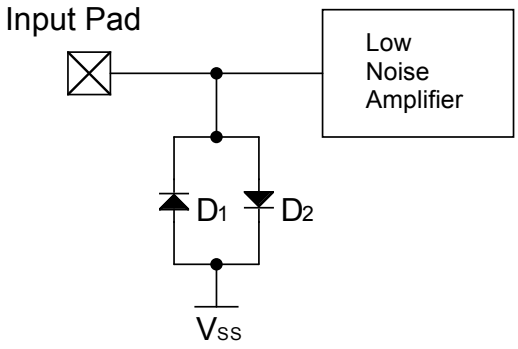

Figure 2.3: ESD protection diodes 2

The addition of the electrostatic discharge protection can degradate the circuit performance with several undesired effects. The parasitic capacitance of the ESD devices is one of the most important issues in radio frequency circuits. Hence, the dimensions of the ESD protection devices should be decreased to reduce this parasitic

capacitance. However, electrostatic discharge robustness needs to be maintained, so the minimum device dimensions cannot be decreased unlimitedly. One solution to reduce the parasitic capacitance is to use topologies with series ESD protection diodes: the overall equivalent capacitance is decreased compared to the previous circuits. However, this benefit is achieved at the price of increasing the number of the devices. Another way to mitigate the performance degradation caused by protection devices is offered by the possibility to tune the parasitic capacitance using inductors. References on these solutions are available in [21] and [22]. In particular, in [22] the possibility to use only one inductor as ESD protection is also presented. Inductors exhibits high impedance at high frequency, so this inductor can be placed between the input pad and V_{SS}: since the frequencies of ESD are much lower than that of the input signal, the inductor can act as a low impedance path for the electrostatic discharge current while it shows a high impedance path to the radio frequency signal. Implementing this circuit topology, a dc blocking capacitor is indispensable, with the aim to provide a separated bias for the low noise amplifier circuit. The solution described is illustrated in Fig. 2.4.

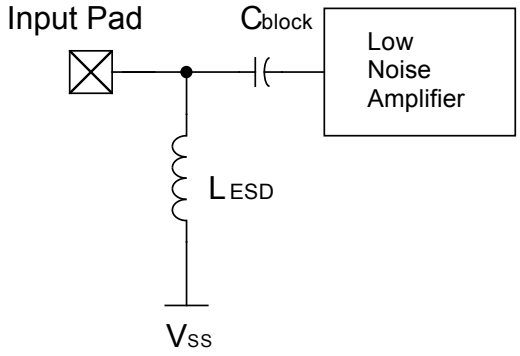

Figure 2.4: ESD protection inductor

However, considering each analyzed case, the insertion of devices with the purpose to realize the ESD protection, essential to avoid damage to the chip, has to be studied in conjunction with the development of the functional block. It is important to remember that more complex solutions require more area and they inevitably introduce additional parasitics, which may have consequences for the functionality of the circuit. In particular, in the design of a low noise amplifier the devices added for this purpose, diodes or inductors, modify the input impedance of the system with direct consequences also for the noise performance of the circuit.

2 Narrow-band low noise amplifier design

Considering the target design specifications, traditional low noise amplifiers for these purposes are implemented using reactive matching networks, to transform the input impedance to the signal source impedance and the optimum noise impedance of the amplifier to the source impedance. The real part of the optimum noise impedance, which is inversely proportional to frequency and transistor size, and the real part of the input impedance are usually quite different, so this approach compromises the input reflection coefficient of the amplifier with the goal of minimizing its noise figure. In fact, the real part of the optimum noise impedance and the real part of the input impedance of the amplifier can be independently tuned using transistor sizing and reactive feedback respectively, while the imaginary part of the input impedance and the imaginary part of the optimum noise impedance can be tuned using series inductors. After this considerations, we have to remember that geometry and optimum bias current of transistors are very important variables, while the passive matching networks determine the size and the cost of the chip.

Based on these properties, once set the optimum current density, the low noise amplifier design can be performed in two main steps: active matching, that is to set the transistor size to make the real part of the optimum noise impedance equal to the source impedance, and reactive feedback matching, to match the input impedance, resonating the imaginary part of the input impedance, and tune out the imaginary part of the optimum noise impedance.

The most used structures in these cases are the common emitter and cascode amplifier topologies with inductive emitter degeneration, shown in Fig. 2.5, which allow to achieve noise figure values close to the minimum noise figure of the single input transistor, at least over a narrow bandwidth. The topologies in Fig. 2.5 make use of a series-series feedback network, which consists of the emitter inductance. In addition, an external base-emitter capacitance can be used to increase the degrees of freedom in the design, improving the linearity of the stage. However, it is not always necessary, also because it degrades the noise performance of the structure. In addition, the cascode stage is inserted with the aim to reduce Miller effect, isolating the input network from the output, condition to be sought in the design of this kind of systems. For these reasons, an inductive degeneration differential topology, with a cascode stage and tuned input and output networks, is considered to implement the low noise amplifier discussed in this work.

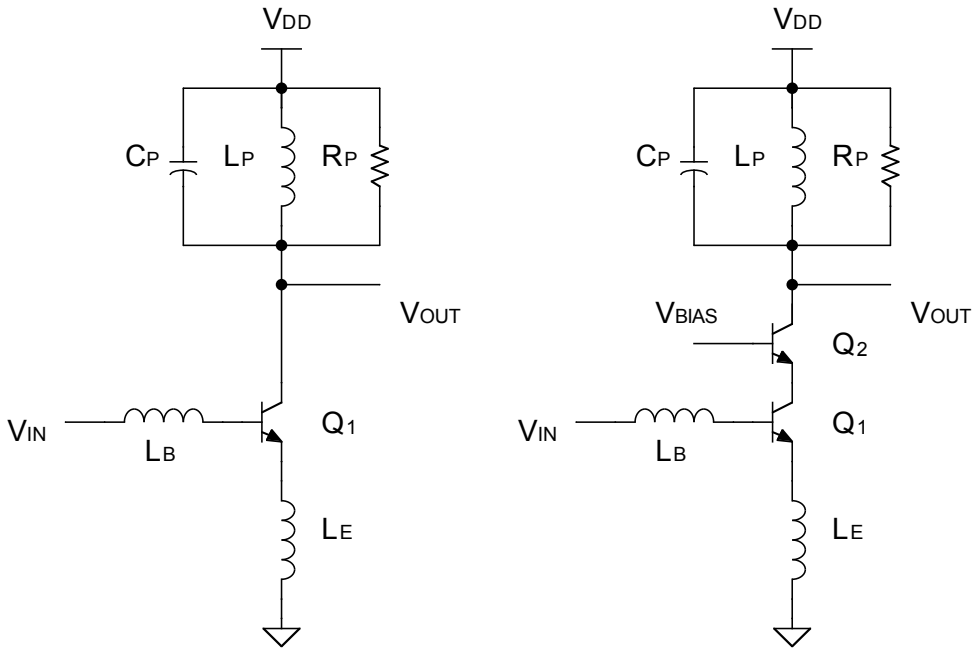

Figure 2.5: LNA1 - Topology

2.1 Active device matching

As discussed in [23], a low noise amplifier can be represented as a two-port network driven by a signal source with an admittance $Y_S = G_S + jB_S$. Following the noise formalism, the noise figure of this two-port network can be expressed as indicated in the following expression (2.2), using the IEEE noise parameters:

$$NF = NF_{MIN} + \frac{R_n}{G_S}|Y_S - Y_{Sopt}|^2 \tag{2.2}$$

In (2.2), NF_{MIN} is the minimum noise figure of the amplifier, ideally identical or close to the minimum noise figure of the signal transistor, and R_n is the noise resistance of the amplifier. The second term of NF is zero when the signal source admittance Y_S equals the optimum source admittance Y_{Sopt}. In this condition, the noise figure of the two-port becomes the minimum noise figure NF_{MIN}. Thus, it is necessary to take into consideration two design steps to minimize the noise figure of the low noise amplifier:

- The minimum noise figure NF_{MIN} has to be made as low as possible to reduce the contribution of the first term in (2.2); the lowest limit is the minimum noise figure of the transistor.
- The optimum source admittance Y_{Sopt} has to be equal to the signal source admittance Y_S to minimize the second term in (2.2).

With the purpose to obtain these two conditions, it is necessary to bias the transistors at the optimum current density for the minimum NF_{MIN} and to size the devices for the desidered optimum noise impedance.
Here, an analytical method used to minimize the noise figure of the system is introduced from a theoretical point of view, and a mathematical expression for the optimum current density J_{Copt} as a function of frequency is found.
Considering [24], it is possible to derive the expressions of NF_{MIN} and Y_{Sopt} for this HBTs amplifier topology:

$$NF_{MIN} = 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}} \tag{2.3}$$

$$Y_{Sopt} = \frac{f}{f_T R_n}\left(\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{4\beta_0 f^2}} - j\frac{n}{2}\right) \tag{2.4}$$

In (2.3) and (2.4), n is the collector current ideality factor, approximately equal to one, β_0 is the dc current gain, f is the operating frequency, f_T is the transit frequency, r_E and r_B the series emitter and base resistance, respectively, and V_T is the thermal voltage. These parameters are nonlinear functions of the emitter width w_E through the term $I_C(r_E + r_B)$. Hence, two parameters have to be determined to achieve the minimum value of NF_{MIN} and to obtain $Y_{Sopt} = Y_S$: they are the dc collector current I_C and the transistor size. It is clear that it is not so easy to determine the two parameters simultaneously, but for the integrated circuits process the minimum size of the device is fixed. In particular, the minimum emitter width can be adopted. In [24] it is discussed how NF_{MIN} remains invariant to changes in emitter length; therefore, the minimum noise figure NF_{MIN} is pratically independent on emitter length, which is adjusted only to modify the optimum noise resistance R_{Sopt}, making it equal to the source resistance R_S, at the minimum noise current density and at operating frequency. Thus, considering [25], it is possible to rewrite the NF_{MIN} as a function of the dc collector current density J_C, as indicated in (2.5), where $(r_E + r_B)_u$ is the sum of emitter and base resistances for a minimum size transistor:

$$NF_{MIN}(J_C) = 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2J_C}{V_T}(r_E + r_B)_u\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}} \tag{2.5}$$

To achieve the minimum value of the noise figure NF, it is necessary to minimize the minimum noise figure NF_{MIN} of the amplifier. By differentiating NF_{MIN} with respect to J_C, we get:

$$\frac{\partial NF_{MIN}}{\partial J_C} = 0 \rightarrow J_{Copt} \tag{2.6}$$

From [19], considering C_{jE} and C_{jC} the base-emitter and base-collector junction capacitances, $(C_{jE} + C_{jC})_u$ the sum of the aforementioned capacitances for a minimum size device, and τ_b the base transit time, the transit frequency f_T is given by (2.7):

$$f_T = \frac{1}{2\pi\left(\tau_b + \frac{C_{jE}+C_{jC}}{g_m}\right)} = \frac{1}{2\pi\left(\tau_b + \frac{(C_{jE}+C_{jC})_u}{J_C} nV_T\right)} \tag{2.7}$$

Considering (2.5) and substituting the parameter f_T with the expression indicated in (2.7), it is possible to take the first derivative of NF_{MIN} with respect to the current density J_C. Hence, setting the condition (2.6) to find the minimum of the function NF_{MIN}, the optimum current density J_{Copt} is obtained:

$$J_{Copt} = 2\pi(C_{jE} + C_{jC})_u nV_T \sqrt{\frac{\beta_0 f^2}{1 + 4\pi^2\beta_0\tau_b^2 f^2}} \tag{2.8}$$

Analyzing (2.8), for frequencies below f_T, the term $4\pi^2\beta_0\tau_b^2 f^2 << 1$. Thus, (2.8) can be approximated as:

$$J_{Copt} \simeq 2\pi f(C_{jE} + C_{jC})_u nV_T\sqrt{\beta_0} \tag{2.9}$$

Finally, substituting J_{Copt} into (2.5), the expression of NF_{opt} is obtained:

$$NF_{opt} = 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{4\pi f(C_{jE} + C_{jC})_u n\sqrt{\beta_0}(r_E + r_B)_u\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}} \tag{2.10}$$

Although the presented mathematical method gives the possibility to understand the influence of the technological parameters on J_{Copt} and NF_{opt}, it is not a very accurate design process because it is necessary to know perfectly the value of these parameters. Thus, it is useful to plot the simulated minimum noise figure NF_{MIN} versus collector current density J_C at the operating frequency of 10 GHz, as shown in the following Fig. 2.6.

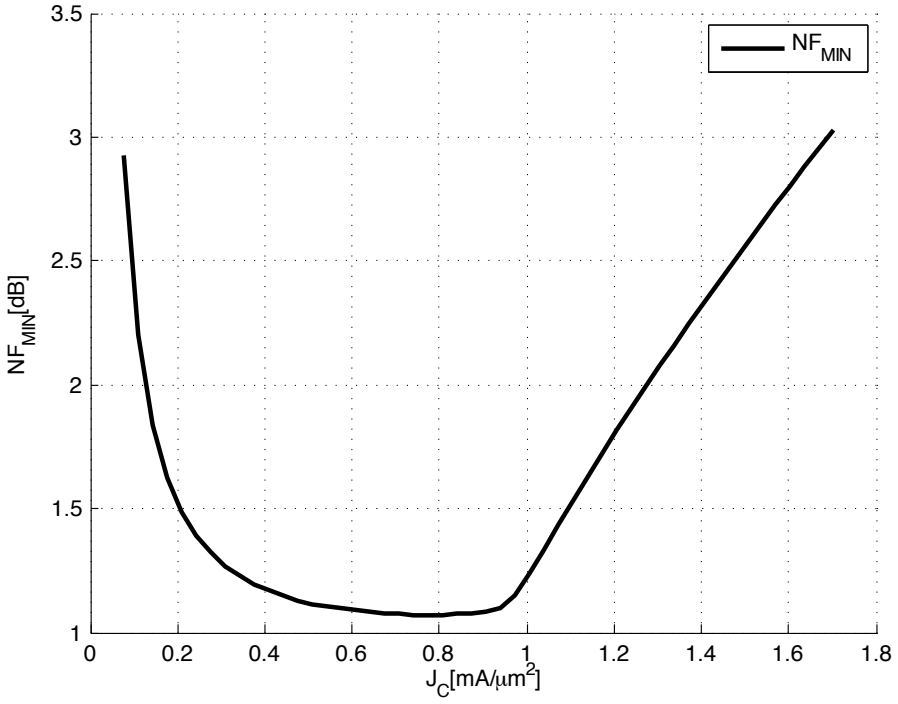

Figure 2.6: LNA1 - Optimum noise current density

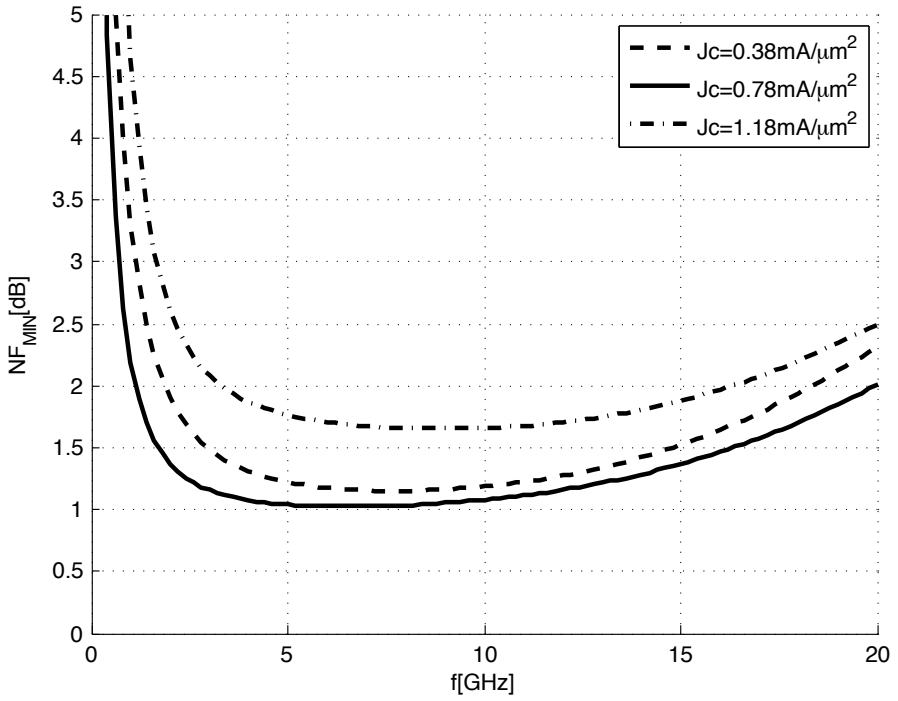

Figure 2.7: LNA1 - Minimum noise figure frequency response

Considering Fig. 2.6, the minimum noise figure has an absolute minimum $NF_{MIN} = NF_{opt} = 1.07\,\text{dB}$ for an optimum noise current density $J_C = J_{Copt} = 0.78\,\text{mA}/\mu\text{m}^2$. In addition, Fig. 2.7 illustrates the frequency response of NF_{MIN} for different values of J_C, to evaluate this parameter in a frequency range around 10 GHz.
For HBTs the optimum current density J_{Copt} increases with frequency, as it is possible to observe from the analytical expression (2.9). Moreover, it is dependent on the amplifier configuration; in fact, for a single transistor stage, it is typically smaller than the optimum current density of a cascode stage. In addition, J_{Copt} is always lower than the value corresponding to the f_T or f_{max} peak; thus biasing a transistor for low noise performance, a penalty in power gain is to be expected.
Once the optimum bias current density J_{Copt} has been selected, the next step is to size the transistor such that the optimum noise impedance of the low noise amplifier becomes equal to the signal source impedance. Analyzing [24], while the optimum noise resistance R_{Sopt} is different from the input resistance, the optimum noise reactance X_{Sopt} is equal to the complex conjugate of the input reactance of the system, and, as discussed in the next paragraph, a reactive matching network allows to cancel out the imaginary parts of the input and optimum noise impedance. As discussed in [23], this procedure is approximated, but it allows to achieve at the same time impedance matching and noise matching with an excellent degree of accuracy. Hence, it is possible only to consider the optimum noise resistance R_{Sopt} to calculate the appropriate size of the devices. An expression for R_{Sopt} to achieve NF_{MIN} of any bipolar device with arbitrary geometry in a common emitter configuration may be found in [25]; in particular, this expression highlights the R_{Sopt} dependency on the emitter stripe ratio of the device geometry relative to the unit device, indicated with N, and on the number of parallel devices M to increase the overall device size.

$$R_{Sopt}(N,M) = \frac{1}{NM}\left[\frac{f_T}{f}\left(\frac{n^2 V_T}{2J_C} + (r_E + r_B)_u\right)\left(\frac{\sqrt{\frac{J_C}{2V_T}(r_E+r_B)_u\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2 f_T^2}{4\beta_0 f^2}}}{\frac{J_C}{2V_T}(r_E+r_B)_u\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)}\right)\right] \tag{2.11}$$

From (2.11), the second term inside the square brackets is constant for a fixed J_C, thus the optimum noise resistance R_{Sopt} can vary with N and M. This means that by selecting these parameters, it is possible to set $R_{Sopt} = 50\,\Omega$ (in a single-ended amplifier). Note that the product NM gives the final device size relative to the unit device. In order not to change the value of NF_{opt} while varying N and M, the optimum current density J_{Copt} should be maintained, so, once the final device size is chosen, the bias current I_C is automatically determined.

The design method just analyzed allows to achieve the best noise performance assuming that the power consumption is flexible: the optimum device size, combined with the optimum current density, sets the power consumption of the low noise amplifier, fixing the bias current of the structure. Although there are not restrictions about the power consumption, the design of a low noise ampifier should try to get the best performance with the lowest power dissipation. Hence, considering both the linearity of the amplifier, which is proportional to the bias current, and the power consumption, it is possible to set the current I_C of each transistor and to calculate the size of the devices maintaining the optimum current density J_C. As discussed, for linearity and power consumption reasons, a current $I_C = 9\,\mathrm{mA}$ is set for the signal transistors of the amplifier.
Fixed the bias current, the theoretical approach to set the optimum size of the devices, as for the calculation of the optimum density current, is quite complex and not so accurate considered the uncertainty on the values of parameters which appear in (2.11). However, an alternative solution is offered by the possibility to use the simulator to determine the size of the transistors. Adopting the minimum emitter width of this technology for the best noise performance, considering transistors with two emitters, and imposing the bias current $I_C = 9\,\mathrm{mA}$, it is possible to evaluate the minimum noise figure NF_{MIN} and the current density J_C for different values of parallel devices M, and emitter stripe ratio N. In particular, N is a variable parameter with the length of emitter l_E; then, determining the size of the devices, maintaining the optimum current density J_{Copt}, it is possible to achieve a value of R_{Sopt} as close as possible to the source resistance. By simulation, the value of the parameter G_{MIN} may be obtained. Its expression is defined in (2.12). From (2.12), it is possible to evaluate the values of Y_{Sopt} and Z_{Sopt}, as shown in (2.13).

$$G_{MIN} = \frac{Y_S - Y_{Sopt}}{Y_S + Y_{Sopt}} \tag{2.12}$$

$$Y_{Sopt} = Y_S \frac{(1 - G_{MIN})}{1 + G_{MIN}} \rightarrow Z_{Sopt} = Z_S \frac{1 + G_{MIN}}{1 - G_{MIN}} \tag{2.13}$$

Therefore, the size which minimizes G_{MIN} to realize the condition $Z_{Sopt} \simeq Z_S$ has to be adopted for the best noise matching. The results about NF_{MIN}, current density J_C, and Z_{Sopt} obtained varying the value of the emitter length l_E and the number of parallel blocks M, are summarized in the following Tab. 2.1. A reference emitter length l_{REF} is considered in Tab. 2.1.

	$\mathbf{l_E}$[µm]	$\mathbf{NF_{MIN}}$[dB]	$\mathbf{J_C}$[mA/µm^2]	$\mathbf{Z_{Sopt}}$[Ω]
M=2	$4\,l_{\mathrm{REF}}$	1.38	2.56	167
	$5\,l_{\mathrm{REF}}$	1.29	2.05	156
	$6\,l_{\mathrm{REF}}$	1.23	1.70	149
	$7\,l_{\mathrm{REF}}$	1.18	1.46	145
	$8\,l_{\mathrm{REF}}$	1.15	1.28	142
	$9\,l_{\mathrm{REF}}$	1.13	1.14	141
	$10\,l_{\mathrm{REF}}$	1.11	1.02	142
M=3	$4\,l_{\mathrm{REF}}$	1.24	1.70	147
	$5\,l_{\mathrm{REF}}$	1.17	1.36	141
	$6\,l_{\mathrm{REF}}$	1.13	1.14	142
	$7\,l_{\mathrm{REF}}$	1.11	0.97	143
	$8\,l_{\mathrm{REF}}$	1.10	0.85	147
	$9\,l_{\mathrm{REF}}$	1.08	0.76	153
	$10\,l_{\mathrm{REF}}$	1.08	0.68	160
M=4	$4\,l_{\mathrm{REF}}$	1.17	1.28	140
	$5\,l_{\mathrm{REF}}$	1.12	1.02	142
	$6\,l_{\mathrm{REF}}$	1.10	0.85	148
	$7\,l_{\mathrm{REF}}$	1.09	0.73	157
	$8\,l_{\mathrm{REF}}$	1.08	0.64	166
	$9\,l_{\mathrm{REF}}$	1.08	0.57	173
	$10\,l_{\mathrm{REF}}$	1.09	0.51	187
M=5	$4\,l_{\mathrm{REF}}$	1.13	1.02	142
	$5\,l_{\mathrm{REF}}$	1.10	0.82	152
	$6\,l_{\mathrm{REF}}$	1.09	0.68	162
	$7\,l_{\mathrm{REF}}$	1.09	0.58	174
	$8\,l_{\mathrm{REF}}$	1.10	0.51	188
	$9\,l_{\mathrm{REF}}$	1.11	0.45	202
	$10\,l_{\mathrm{REF}}$	1.13	0.41	215

Table 2.1: LNA1 - Active device matching

Analyzing Tab. 2.1, the best size result that allows to observe the value of the optimum current density and to reach the value of NF_{opt} is $M = 3$ and an emitter length corresponding to the last but one line of the section related to three parallel devices. Anyway, it is clear that other pairs of values M and l_E allow to achieve similar results in terms of NF_{MIN} and J_C. For example, setting $M = 4$ or $M = 5$, with a suitable choice of the emitter length, it is possible to reach the minimum noise figure $NF_{MIN} = 1.09\,\text{dB}$ with a value of Z_{Sopt} close to $160\,\Omega$. However, considering the implementation of the reactive matching network, as discussed in the next paragraph, the parameters $M = 3$ and $l_E = 9\,l_{\text{REF}}$ allow to obtain a lower base inductance value to realize the impedance matching. In fact, taking the inductor non idealities into account a low value of base inductance generally limits the increase of the system noise figure. The optimal design is hence based on the parameters reported in Tab. 2.2.

	$\mathbf{l_E}$[µm]	$\mathbf{NF_{MIN}}$[dB]	$\mathbf{J_C}$[mA/µm^2]	$\mathbf{Z_{Sopt}}$[Ω]
M=3	$9\,l_{\text{REF}}$	1.08	0.76	153

Table 2.2: LNA1 - Optimum sizing

Finally, fixed the size of the devices, a transistor structure with three bases is chosen to limit the noise performance degradation.
After the active device matching, the design process considers the impedance matching, which depends on the topology implemented. Purely reactive components do not contribute noise and inductors do not dissipate dc power, so ideal inductors and capacitors are preferred as matching elements. These components occupy considerably more die area than transistors. Thus, using as few passive elements as possible is advisable. The design of the input network has to achieve the impedance matching and to tune out the imaginary part of the optimum noise impedance to obtain a minimum noise figure for the low noise amplifier. In addition, as analyzed in [24], a structure with the inductive degeneration does not modify the value of R_{Sopt}, but it affects the optimum source reactance X_{Sopt}. As already discussed, by connecting a base inductor L_B, simultaneous noise and input impedance matching is obtained. In the next subsections, the design procedure to realize the input matching of the low noise amplifier is presented.

2.2 Passive component matching

The second main step of the low noise amplifier design consists in the input impedance matching. Considering the cascode structure shown in Fig. 2.5, the expression of the input impedance Z_{IN} of the amplifier with inductive degeneration can be determined using the equivalent circuit of the signal transistor, as illustrated in Fig. 2.8.

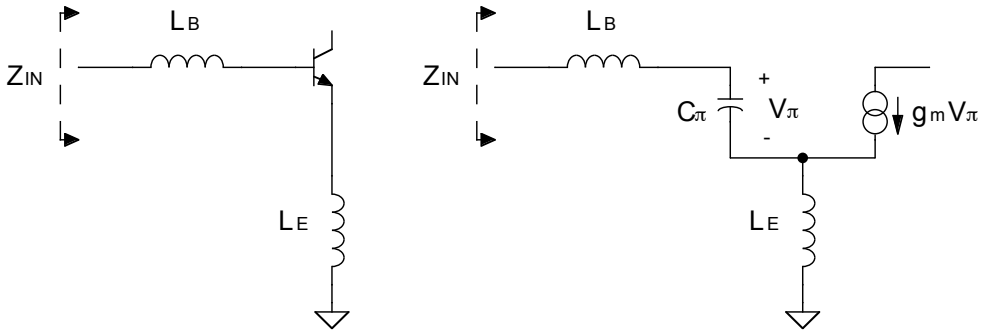

Figure 2.8: LNA1 - Equivalent input circuit

Ignoring the intrinsic base and emitter resistance of the transistor and considering ideal inductors as a first-order approximation, from the equivalent circuit shown in Fig. 2.8 it is possible to calculate the input impedance as indicated in (2.14):

$$Z_{IN}(s) = s(L_B + L_E) + \frac{1}{sC_\pi} + \frac{g_m L_E}{C_\pi} \tag{2.14}$$

Equation (2.14) shows that the input network of the low noise amplifier can be considered as a series resonant RLC network, as shown in Fig. 2.9.

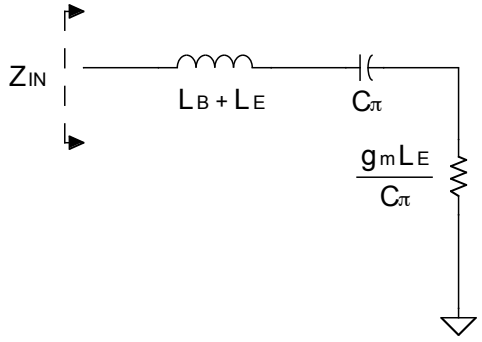

Figure 2.9: LNA1 - Input resonant network

Considering the source resistance R_S, the quality factor Q_{IN} of the input matching network is given by the following expression:

$$Q_{IN} = \frac{1}{\omega_0(g_m L_E + R_s C_\pi)} \tag{2.15}$$

From the equation (2.15), the reader can easily understand that the insertion of a capacitance in parallel to C_π decreases the quality factor of the input network and increases the input matching bandwith. However, this possibility is traded for a reduction of the noise performance of the system, even if an increase of this capacitance allows to reduce the base inductance L_B.
The input impedance Z_{IN} can be decomposed into real and imaginary part as shown in (2.16):

$$Z_{IN}(j\omega) = \frac{g_m L_E}{C_\pi} + j\left[\omega(L_B + L_E) - \frac{1}{\omega C_\pi}\right] \tag{2.16}$$

From (2.16) the real part of the input impedance is not dependent on frequency. Since the source impedance is purely resistive, $R_S = 50\,\Omega$, the real part of the input impedance should be designed to be equal to this value, while the imaginary part should be tuned out. It is clear that the purpose of L_B is precisely to cancel the imaginary part of the input impedance, but it is important to consider that its insertion has effects on noise performances, linearity and gain of the amplifier. In the analysis just presented the parasitic resistances of the inductors and the intrinsic base and emitter resistance are ignored, as the effect of coupling capacitance (adding in series to the input resonant circuit) used to separate the radio frequency signal path and the bias of the circuit. In most practical cases, the emitter inductance L_E is small and its associated series resistance can be ignored, while L_B is always large enough such that its series resistance cannot be neglected. However, these contributions are taken into consideration throught the simulation process.
Equation (2.16) illustrates the role of the degeneration inductor: by adding L_E the real part of the input impedance can be set to achieve the impedance match, and the amount of degeneration needed depends only on the value of $\omega_T = 2\pi f_T = g_m/C_\pi$. Thus, the value of the inductance L_E can be determined as follow:

$$L_E = \frac{R_S C_\pi}{g_m} = \frac{R_S}{2\pi f_T} \tag{2.17}$$

Considering (2.17), from the simulation it is possible to extrapolate the value of the capacitance C_π, which is related to the choice of the transistors used, while g_m is determined by the bias current. Therefore, considering the optimization process realized through the simulator, the value $L_E = 90\,\text{pH}$ is set.
Once the value of L_E is determined, it is possible to set the value of the series inductor L_B to tune out the imaginary term in (2.16) at the operating frequency $f_0 = 10\,\text{GHz}$. Its value is given by (2.18):

$$L_B = \frac{1}{\omega_0^2 C_\pi} - L_E = \frac{2\pi f_T}{(2\pi f_0)^2 g_m} - L_E = \frac{f_T}{2\pi f_0^2} - L_E \tag{2.18}$$

Considering also the effect of coupling capacitance, set to 1 pF, a suitable value of base inductor is $L_B = 1\,\text{nH}$. Then, the design process of the input matching network is complete. Fig. 2.10 and Fig. 2.11 illustrate the trend of the real and imaginary part of the input impedance Z_{IN}, R_{in} and X_{in}, respectively, and the $S11$ parameter, considering the implemented differential solution with a source resistance $R_S = 100\Omega$.

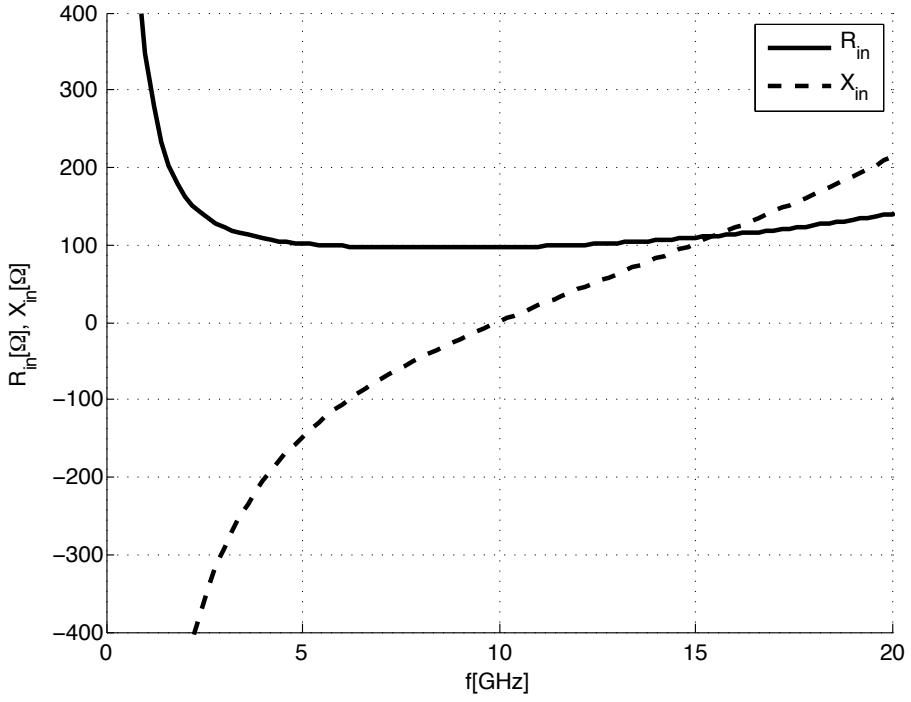

Figure 2.10: LNA1 - Input impedance

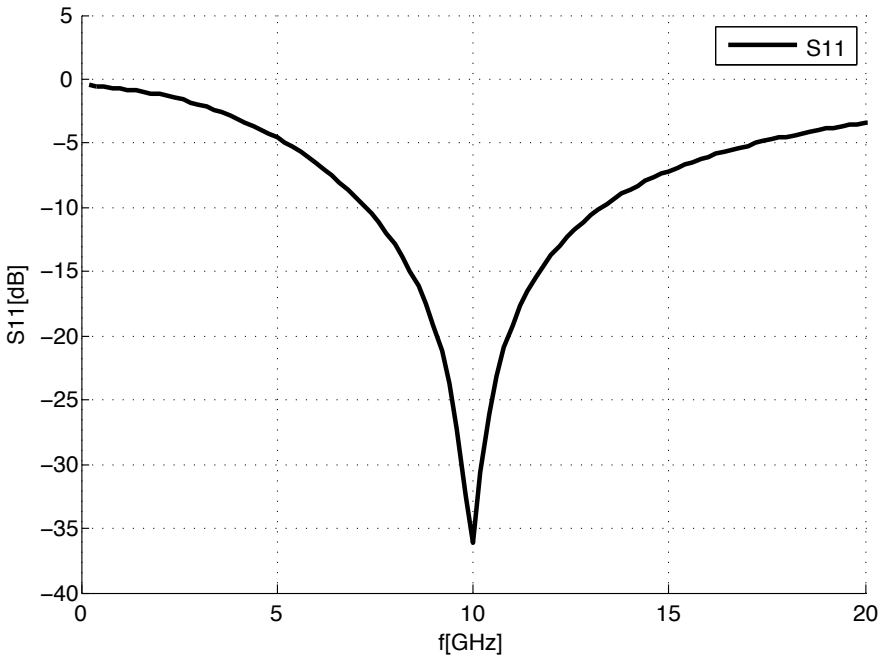

Figure 2.11: LNA1 - S11 parameter

At the operating frequency of 10 GHz, the real part of the input impedance is set to $R_{in} = 97\,\Omega$, while the imaginary term is $X_{in} = 0.72\,\Omega$. The input reflection coefficient is $S11 = -36$ dB at 10 GHz, and it is less than -10 dB in a bandwith of about 6 GHz, from 7.25 GHz to 13.25 GHz.

2.3 Load Tuning

A parallel resonant circuit tuned at the operating frequency of 10 GHz is used as load network. An additional benefit of using an inductor is offered by the possibility for the output voltage to swing above the supply rail, thus improving the linearity compared to the case where a resistive load is used.

The total load capacitance is determined by the overall capacitance connected to the output node, the output capacitance of the cascode transistor C_{CASC} and the input parasitic capacitance C_{EF} of an emitter follower connected to the output. In Fig. 2.12, the equivalent single-ended circuit of the output reactive network is shown.

Hence, considering the operating frequency, the results obtained by the simulator about C_{CASC} and C_{EF}, and setting $L_P = 1$ nH, the explicit output capacitance is fixed to the value $C_P = 80$ fF.

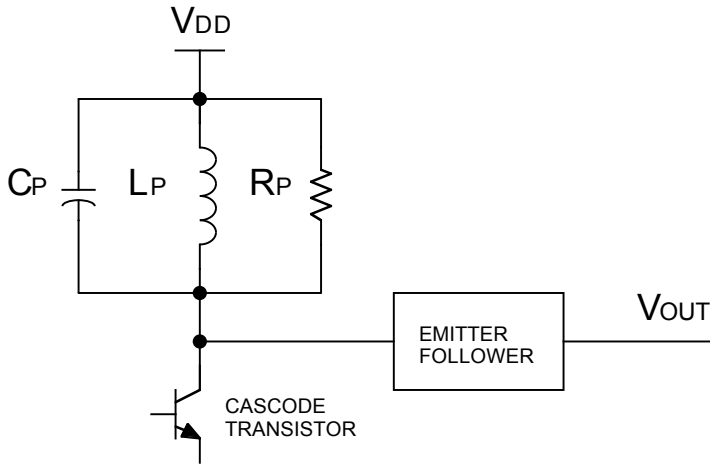

Figure 2.12: Output resonant network

At the resonance frequency f_0, the maximum power gain P_{MAX} expression of the low noise amplifier is given by (2.19):

$$P_{MAX} = \frac{1}{4}\left(\frac{f_T}{f_0}\right)^2\left(\frac{R_P}{R_S}\right) \tag{2.19}$$

If the purpose of the design is to maximize the power gain, only one variable to set is available, the load resistance R_P, once the transistors of the stage are fixed and f_T is determined; this means to design a high Q network. Therefore, considering $C_{TOT} = C_P + C_{CASC} + C_{EF}$, the following expressions determined the design of the output network, which allow to fix the resonance frequency and to evaluate the quality factor Q related to the bandwith:

$$\begin{cases} f_0 = \frac{1}{2\pi\sqrt{L_P C_{TOT}}} \\ Q = 2\pi f_0 C_{TOT} R_P \end{cases}$$

Finally, with the purpose to obtain a suitable gain, bandwidth and IIP3 the value of R_P has to be setted. In particular, observing the variations of IIP3 and $S21$ parameter when R_P changes, an appropriate value for this resistance is $R_P = 110\,\Omega$. Considering a differential topology, a more compact solution is shown in Fig. 2.13.

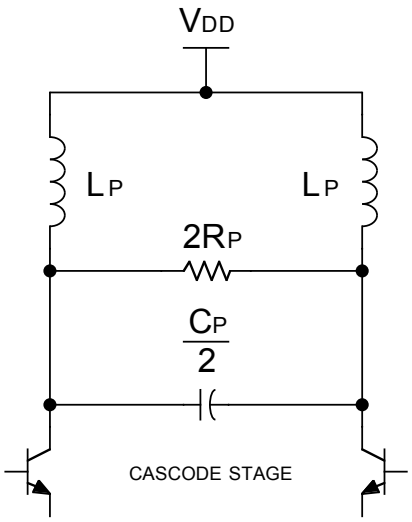

Figure 2.13: Differential output resonant network

Therefore, the capacitance of the output network is set to 40 fF and the resistance is 220 Ω. Finally, an IIP3=−2.6 dBm is obtained and the trend of the $S21$ parameter is shown in Fig. 2.14. At the operating frequency 10 GHz, observing the figure below, $S21 = 19.5$ dB and $BW_{-3dB} = 6.4$ GHz.

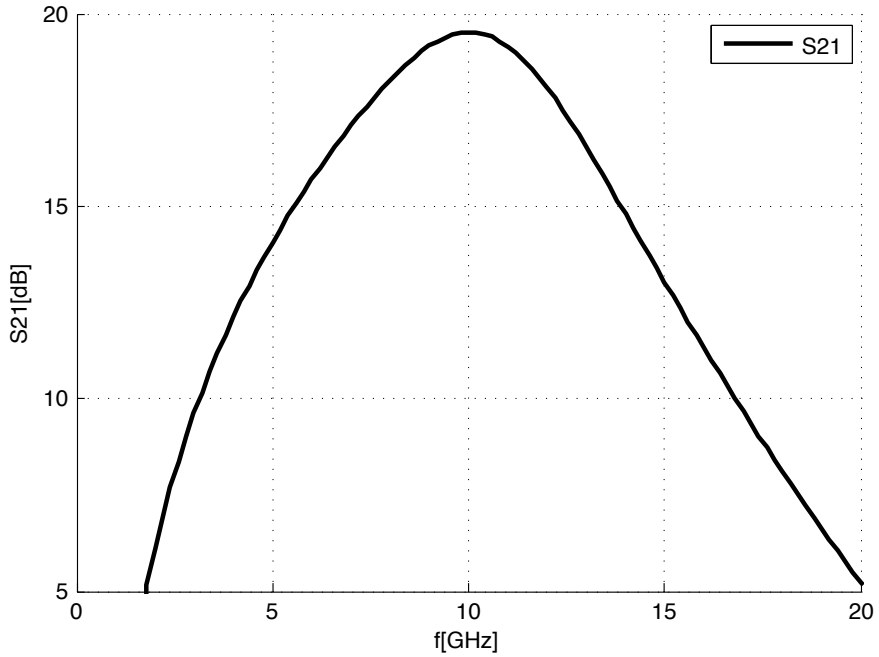

Figure 2.14: LNA1 - S21 parameter

2.4 Output buffer

The low noise amplifier has to be measured using standard 50 Ω equipment. Thus, it is necessary to add a buffer at the output. This buffer does not have to modify heavily the output network and it has the purpose to set the output impedance of the system to the value of 50 Ω, for the single-ended circuit. The implemented emitter follower is illustrated in Fig. 2.15. In this circuit Q_1 is the input transistor, while Q_2 is the transistor of the current mirror, which allows to set the current of the branch by modifying the value of R_{DEG}. In particular, transistors Q_1 and Q_2 are both designed with the minimum emitter width of this technology. The current of the branch is set to 7 mA. Finally, the condition $R_0 = 50\,\Omega$ is imposed to realize the output impedance matching.

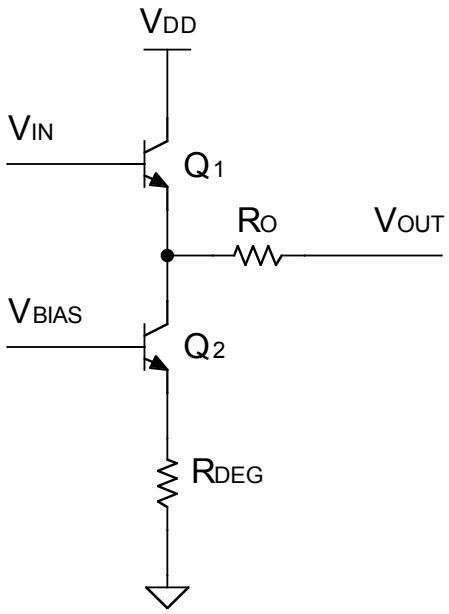

Figure 2.15: Output buffer

2.5 Noise performance

In the previous paragraphs, the study of the minimum noise figure and the evaluation of the optimum bias current for best noise performance has been presented, considering the analytical solution and the simulator results. Generally, high values of the intrinsic base and emitter resistance must be avoided, so transistors with more base strips are used. Thus, following the design analyzed procedure, it is possible to obtain the condition $NF = NF_{MIN}$ at the operating frequency. However, evaluating the expression of NF_{MIN} and the values in Tab. 2.1, further

contributions to the overall noise figures NF can be attributed to a non-optimum noise matching.

The purpose of this subsection is to report the results obtained regarding the noise performance. Fig. 2.16 shows NF_{MIN} and NF as a function of frequency for the designed low noise amplifier designed; in particular, at 10 GHz the value $NF = 1.16$ dB is achieved.

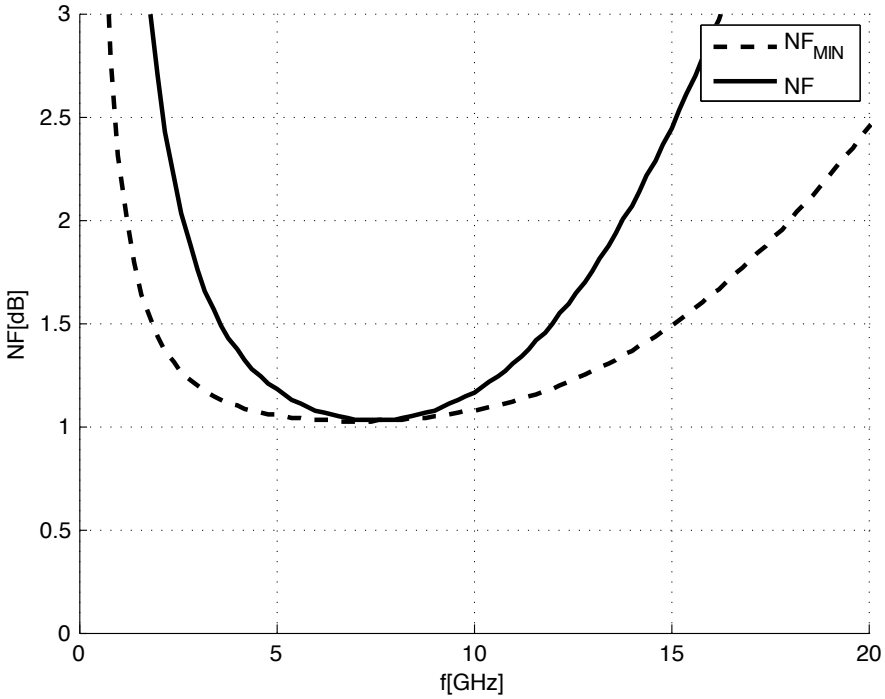

Figure 2.16: LNA1 - Noise performance

From Fig. 2.16, the reader can observe that the minimum value of the NF is centered at $f \simeq 8$ GHz. Through the simulator, it is possible to evaluate the optimum value of L_B for noise performance at 10 GHz, maintaining the value of L_E, and it results $L_B \simeq 700$ pH; in this case, the noise figure NF would be equal to the minimum noise figure $NF_{MIN} = 1.08$ dB. However, changing L_B the center frequency of the $S11$ dip is modified, and varying the values of the components of the input network, or adding an external capacitance between base and emitter of the transistor to center this peak at 10 GHz, worst noise performance is achieved. These results and considerations demonstrate that noise matching and impedance matching are not uncorrelated. In particular, an in-depth noise analysis shows the relation between the imaginary parts of the noise impedance and input impedance, as discussed in [23]. In addition, it can be demonstrated, using the theory of correlated noise sources in series-series feedback circuits, that if the degeneration inductor L_E is

a lossless inductor it will not change the value of the optimum noise resistance R_{Sopt}, but it will affect the optimum noise reactance X_{Sopt}; in particular, when the degeneration inductor L_E is added to the circuit the optimum noise reactance become $X'_{Sopt} = X_{Sopt} - 2\pi f L_E$, where X_{Sopt} can be derived from (2.4). However, the presented design procedure yields satisfactory results, considering that the noise figure at 10 GHz is 0.08 dB greater than the minimum noise figure NF_{MIN}.

2.6 Inductors design and electromagnetic model

Inductors are an essential part of many radio frequency systems. The electromagnetic behavior of these components can only be fully described through the numerical solution of Maxwell's equations. The main characteristics of an inductor to be taken into consideration during its design are the topology, the desired area, the inductance and the operating frequency. From this information, an integrated layout that lies within some tolerance of the desidered specifications and exhibits an optimal quality factor is produced. The purpose of this section is to explain the main concepts of a real inductor and to evaluate the effect on the low noise amplifier performance using the electromagnetic models obtained by Sonnet simulation. An inductor is a component that stores energy in the form of a magnetic field. Considering Maxwell's equations, as a current flows through an inductor, it creates a directional magnetic field surrounding the inductor, and its presence opposes any change to the current. Thus, energy is stored in the induced magnetic field which allows current to persist in the absence of electrical energy, and the inductance is a measure of how much energy can be stored in the magnetic field of a given device. The quality factor Q represents the ratio of the stored energy to the amount of energy dissipated in the inductor per cycle, providing an index of efficiency for the device, as defined in [39]:

$$Q = 2\pi \frac{E_{stored}}{E_{dissipated}} \tag{2.20}$$

An integrated inductor at high frequency exhibits significant capacitive effects with adjacent conductors and with the substrate, so it behaves like a second order system and there is a frequency at which the system resonates, called self resonance frequency f_0. Another method to define the Q factor for resonant system can be derived from its bandwidth. In fact, considering $\omega_0 = 2\pi f_0$ and the -3dB bandwidth, the quality factor of the system is defined in [39], as reported in (2.21):

$$Q = \frac{\omega_0}{\Delta\omega} \tag{2.21}$$

Considering series and parallel resonant networks, like in the design of input and output network of the low noise amplifier discussed in the previous paragraph, the quality factor Q is given by the following expressions:

$$\begin{cases} Q_{series} = \frac{\omega_0 L}{R} \\ Q_{parallel} = \omega_0 C R \end{cases}$$

The resulting definitions of Q for these systems agree with the intuition that a high quality resonator does not dissipate much energy at the resonance frequency.
Integrated inductors can be implemented as planar devices, and they are realized during metallization circuit process, which offers 6 metal layers in this technology. As discussed in [40], polygon spirals with more than four sides have higher Q than square spirals for the same area, and circular inductors allow to achieve the best performance. However, pratical CAD and fabrication problems limit mask preparation to allowed angles of 45° or 90°, hence octagonal and square inductors have to be used instead of circular structures.It is also possible to connect more metal layers as shunt connection to reduce the series resistance, and to improve the low frequency Q of the inductor. However, the parasitic capacitive coupling can reduce the self resonance frequency and the resistive contribution of vias used for the connection between different metal layers limit the benefits of this technique. Fig. 2.17 shows the shunt connection of an inductor using the two top available metal layers. For the reasons discussed, the inductors developed in this work have octagonal or square shapes, adopting a single layer for the spiral and adjacent layers for the underpass connections.

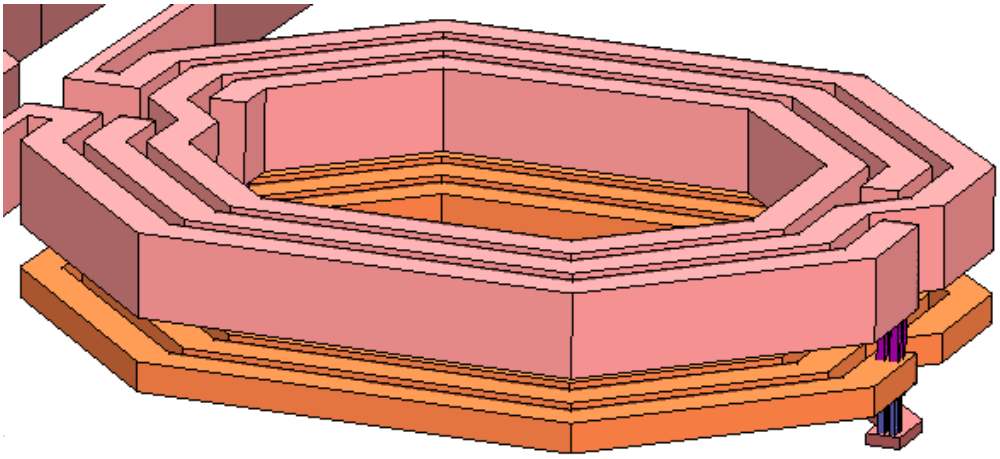

Figure 2.17: Shunt-connected inductor

The parasitic effects and the non-ideal behavior of an integrated inductor has to be considered during the design of the device, with the purpose to limit undesidered loss mechanisms. Thicker and higher conductivity metal layers improve the quality factor Q at low frequencies, whereas a higher resistivity substrate and thicker oxide help to isolate the device from the substrate at high frequencies. The optimization of the geometry of an inductor is quite difficult, because there are several parameters to take into consideration, including the area of the spiral, the metal width and spacing, and the number of turns. Much of the optimization process depends on the operating frequency: at low frequency, it is usually better to use the minimum space available to maximize the magnetic coupling, but at high frequency proximity effect requires a larger value of spacing. Similar consideration can be apply to the area of the spiral and to the number of turns; in fact, at lower frequencies wider metal width determines a low value of series resistance, but at higher frequencies the quality factor is dominated by the substrate losses and a smaller area is favorable.
In the following, the main undesidered effects are briefly analyzed, as eddy currents, skin effect and proximity effect.
A magnetic field created by a conductor can intersect a nearby conductor and it may induce small circular currents, called eddy currents. These currents generate a magnetic field which opposes the original field, dissipating energy in form of heat as they flow through the conductor, and decreasing the efficiency of the energy storage.
At high frequency, most of the current flows much more strongly near the surface of the conductor, causing the apparent cross-section area of the conductor to decrease, and consequentely causing the increase of the ac resistance. A measure of the skin effect is the skin depth δ, shown in (2.22), defined as the depth in the conductor at which the current density falls to $1/e$ of its value at the surface. In this expression μ is the permeability and σ the conductivity of the material, while f is the operating frequency.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{1}{\pi f\mu\sigma}} \tag{2.22}$$

If the skin depth is significantly larger than the conductor thickness at a given frequency, then the skin effect is negligible at that frequency. Thus, the rule of thumb is to design inductors with a conductor thickness smaller than the skin depth at operating frequency.

The proximity effect is another istance of eddy currents, in which nearby conductive material experiences induced eddy currents due to the magnetic field of a separate conductor. Therefore, also the distance between conductors in a spiral inductor has to be taken into consideration.
The main parameters to consider during the design of an inductor are the number of turns n, the conductor width w, the conductor thickness h, the spacing between conductors s, and the spacing to ground s_g. The following Tab. 2.3 summarizes the first approximation effects of these design parameters on the inductance L, series resistance R, self resonance frequency f_0 and substrate coupling capacitance C_{sub}.

	$\mathbf{L}$[H]	$\mathbf{R}$[Ω]	$\mathbf{C_{sub}}$[F]	$\mathbf{f_0}$[Hz]
n ↑	↑	↑	↑	↓
w ↑	↑	↓	↑	↓
h ↑	–	↓	↑	↓

Table 2.3: Inductor design rules of thumb

The rules of thumb analyzed in Tab. 2.3 have to be verified with the electromagnetic simulator. In fact, at high frequency increasing the width of conductors w may not yield a reduction of the resistance, considering the skin effect.
The spacing s between conductors dominates the self resonant frequency of a spiral and the determination of the smallest value that allows useful operation at a given frequency can be an important tool in the design.
Finally, considering the distance from the substrate s_g, the loss mechanism remains the same of proximity effect, so this distance can often be set large enough to avoid significant loss.
Following the discussed rules of thumb, using the electromagnetic simulator, more than one version for each inductor of the circuit is realized, trying to get the best performance. The topologies for the base and degeneration inductors are shown in Fig. 2.18, while Fig. 2.19 illustrates the load inductors structure. For the degeneration inductors, a differential structure is realized, as shown in Fig. 2.18;

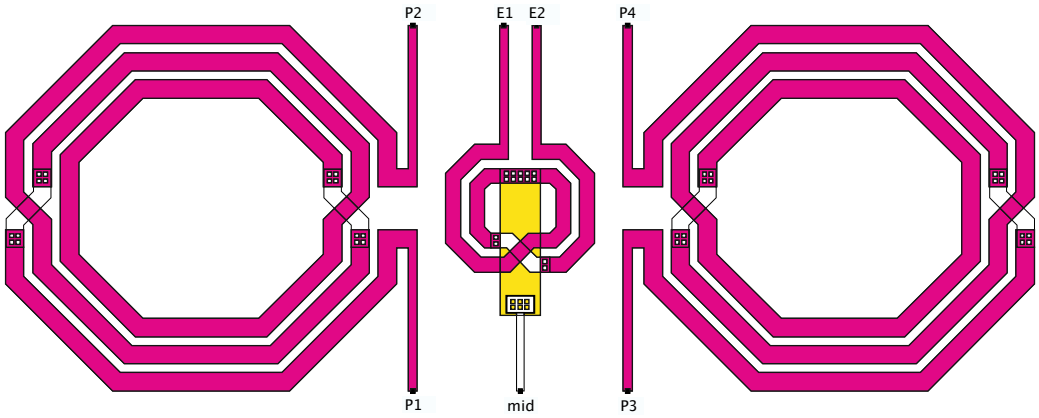

Figure 2.18: LNA1 - Base and degeneration inductors

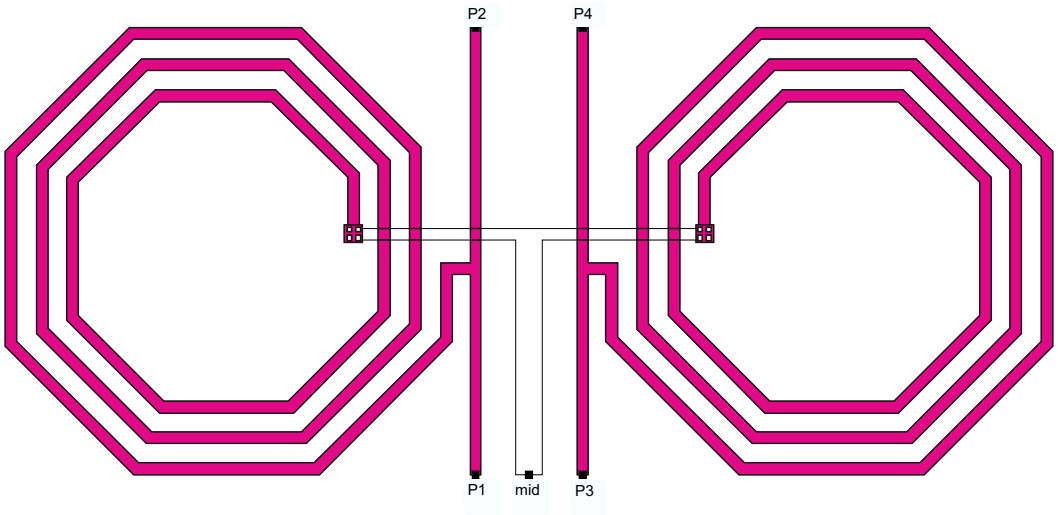

Figure 2.19: LNA1 - Load inductors

Through the electromagnetic simulator, it is possible to obtain a lumped parameter model, which characterizes the integrated inductor with the minimum number of discrete components. The resulting electrical structure is a $\pi - circuit$, as illustrated in Fig. 2.20. The series branch of this circuit corresponds to the winding of the inductor, and it is composed by the inductance L, the series resistance R_S and the lateral coupling capacitance C_L. In addition, the resistance R_{SUB} and capacitance C_{SUB} to the substrate and the oxide capacitance C_{OX} can be split into two equal parts to complete the equivalent circuit, as shown in the figure below.

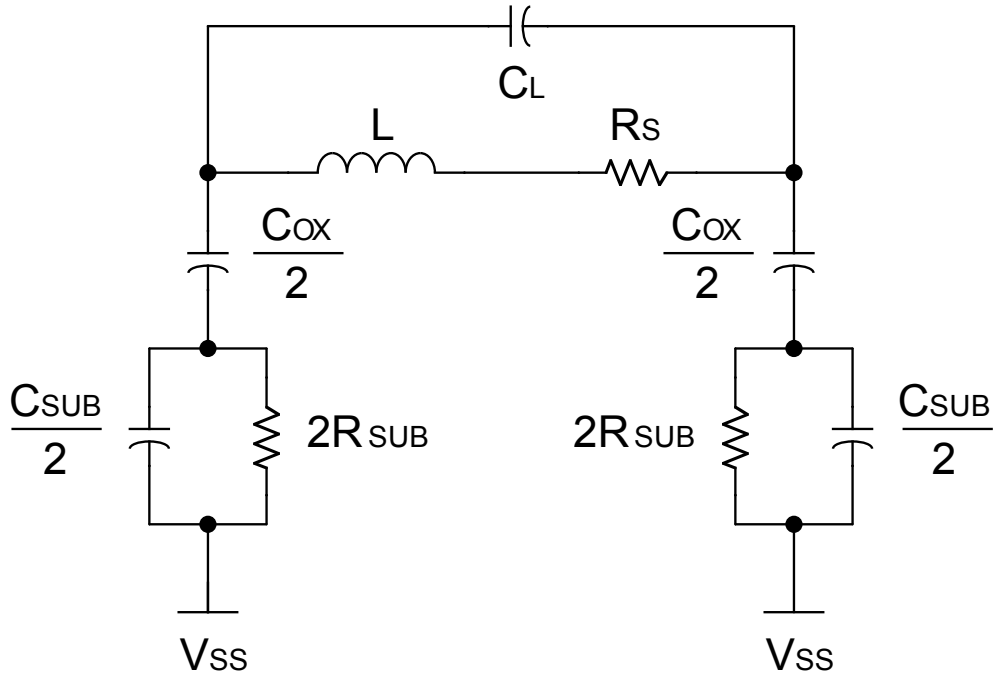

Figure 2.20: $\pi - circuit$ model of inductors

Considering the design of the input and output resonant networks of the low noise amplifier, the finite quality factor Q of inductors determines the necessity to slightly modify the value of the components that appear in these networks.
Tab. 2.4 summarizes the parameters of the base inductor, differential degeneration inductor and load inductor, obtained through the Sonnet electromagnetic simulator. In particular, this table illustrates the value of the inductance L at 10 GHz, the number of turns n, the width w used for metal layer 6, the self resonance frequency f_0, the quality factor Q, and the required area for each inductor.
The thickness of metal layer 4, 5, and 6 is fixed at 0.39 µm, 1 µm, and 2.8 µm respectively.
Finally, the input coupling capacitance is set to 1.5 pF, the load capacitance C_P is 120 fF, which becomes 60 fF with the differential structure shown in Fig. 2.13, and the load resistance is fixed at 250 Ω with the same differential topology.

	Base inductor	Degeneration inductor	Load inductor
L[nH]	0.990	0.170	1.110
n	3	2	3
w[μm]	5.0	4.0	2.4
f_0[GHz]	38	160	43
Q	15	7	11
area[μm^2]	100x100	60x60	100x90

Table 2.4: LNA1 - Inductors features

Finally, Fig. 2.21 and Fig. 2.22 illustrate the trend of the S-parameters $S11$ and $S21$, and of the noise figure NF and minimum noise figure NF_{MIN}. Evaluating Fig. 2.21, the dip of $S11$ at 10 GHz is -20.8 dB, and it is less than -10 dB in the range $7.3 \div 13.3$ GHz, while $S21 = 18.8$ dB at the operating frequency 10 GHz, with a -3dB bandwidth of 6.5 GHz.

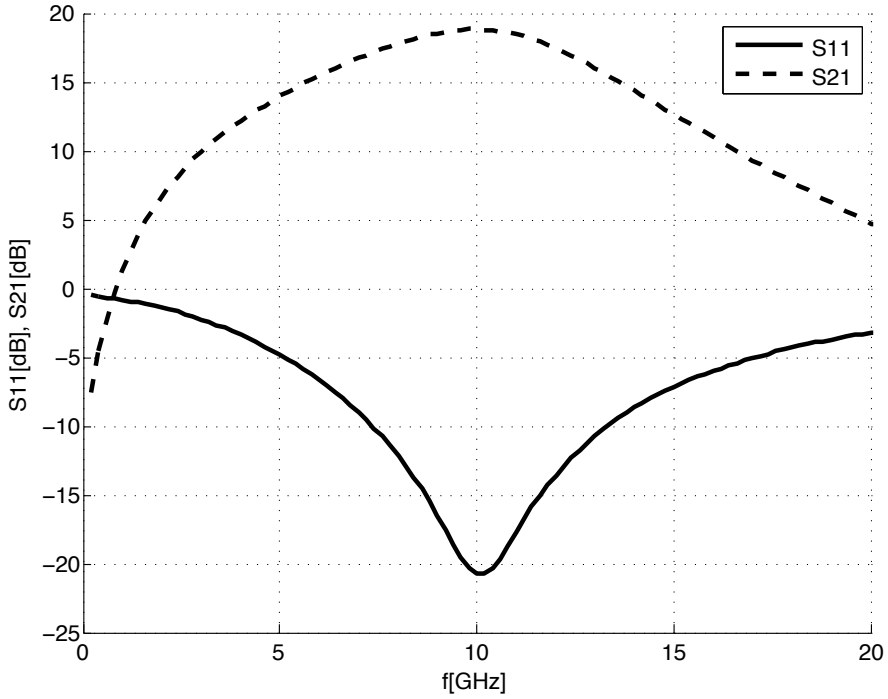

Figure 2.21: LNA1 - $S11$ and $S21$ parameters

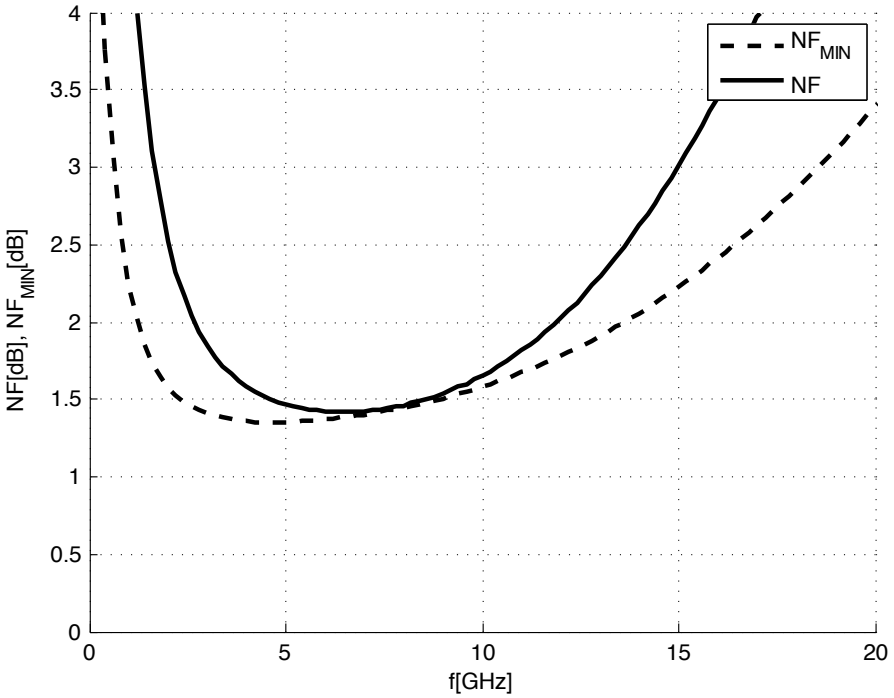

Figure 2.22: LNA1 - NF_{MIN} and NF

Considering Fig. 2.22, $NF = 1.65\,\text{dB}$ and $NF_{MIN} = 1.58\,\text{dB}$ at the operating frequency 10 GHz. Compared to the case of ideal inductors analyzed in the pevious paragraph, the noise figure is increased of 0.5 dB, and the main contribution is due to the base inductor L_B. In this context, only a more accurate design of the inductors can try to minimize this decreasing in noise performance. As evaluated in the following paragraphs, the alternative may be to change the low noise amplifier topology, avoiding the base inductor and searching for another solution to realize the input matching and the noise matching.

2.7 ESD protection

The electrostatic discharge protection system implemented for this low noise amplifier is based on the diodes structure shown in Fig 2.3. With this technology, three different sizes for the ESD protection diodes are available, contributing in a progressive manner to introduce parasitic capacitance to the input node of the system. To minimize the effects on the input network, the smaller devices are chosen. The implemented topology is illustrated in Fig. 2.23, where a series connection minimizes the total capacitance added. The insertion of ESD diodes imposes to adjust the parameters of the input network. Through the optimization process, the ac coupling capacitance is set to 1.3 pF.

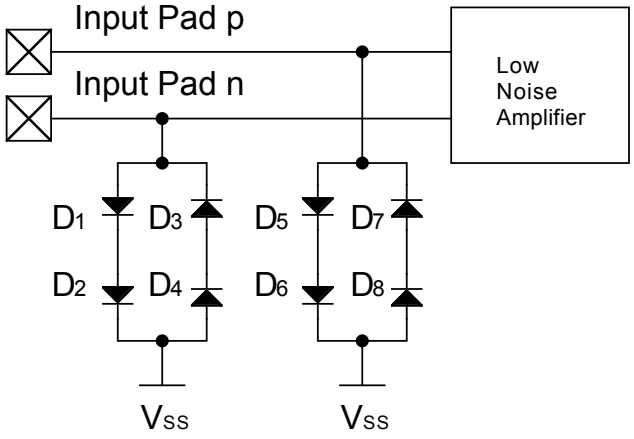

Figure 2.23: LNA1 - ESD protection

The cascode stage is simplified, fixing $M = 1$ and adopting the same structure with three bases, without observing a significant degradation. The plots of $S11$, $S21$, and the noise performance are shown in Fig. 2.24 and Fig. 2.25. The $S11$ dip at the operating frequency has a value of $-19.5\,\text{dB}$ and it is less than $-10\,\text{dB}$ in the range $7.4 \div 12.8\,\text{GHz}$; the $S21$ is equal to $18.6\,\text{dB}$ at $10\,\text{GHz}$, with a -3dB bandwidth of $7\,\text{GHz}$. Finally, $NF_{MIN} = 1.84\,\text{dB}$ and $NF = 1.88\,\text{dB}$, with an increment of $0.23\,\text{dB}$ in noise figure, compared to the case without ESD protection.

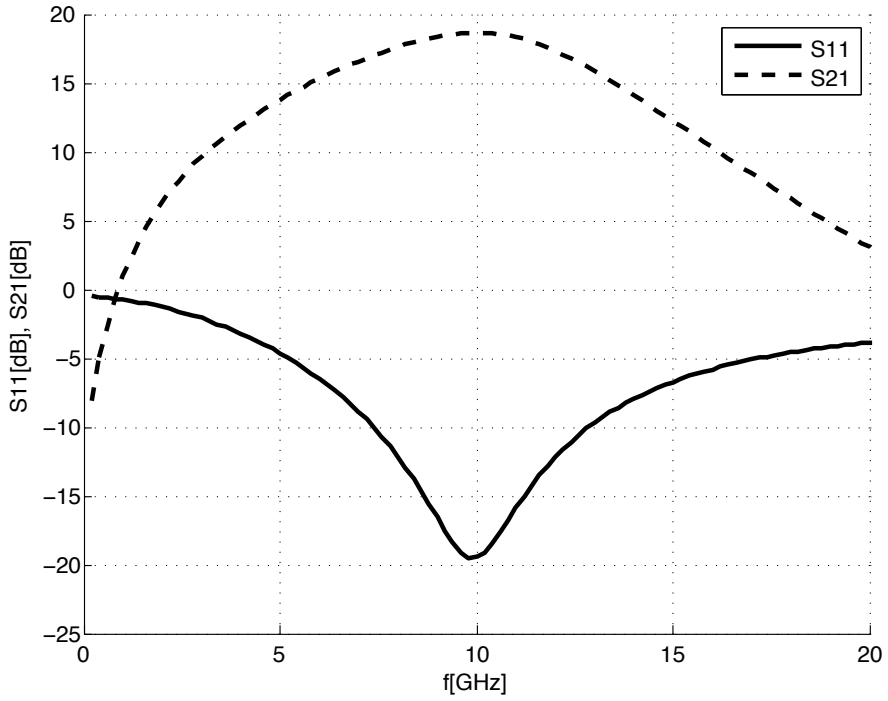

Figure 2.24: LNA1 - $S11$ and $S21$ with ESD protection

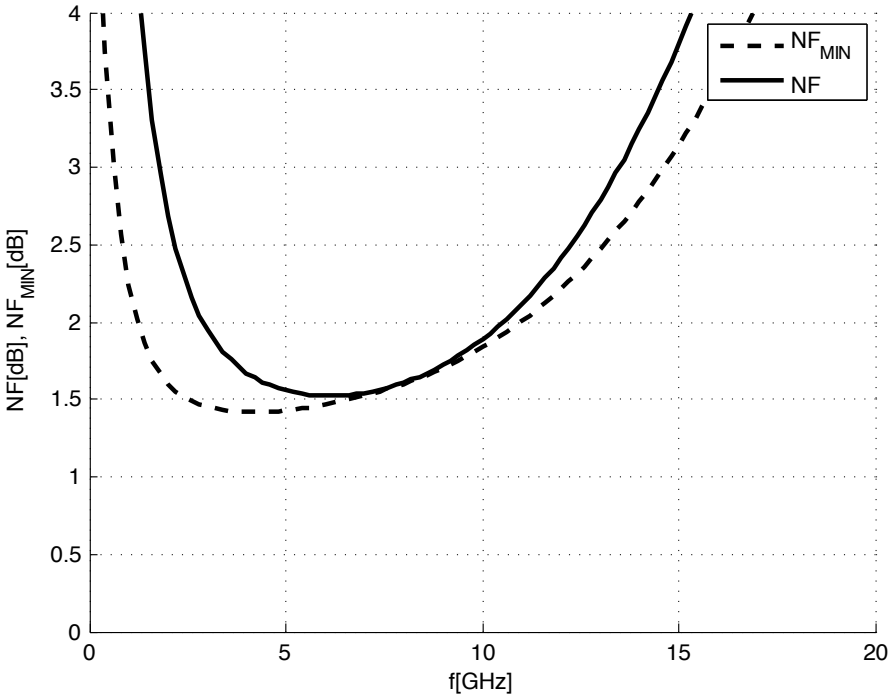

Figure 2.25: LNA1 - NF_{MIN} and NF with ESD protection

2.8 Biasing

The low noise amplifier presented in this work has a biasing realized by means of current mirror circuits, whose topology is illustrated in Fig. 2.26.

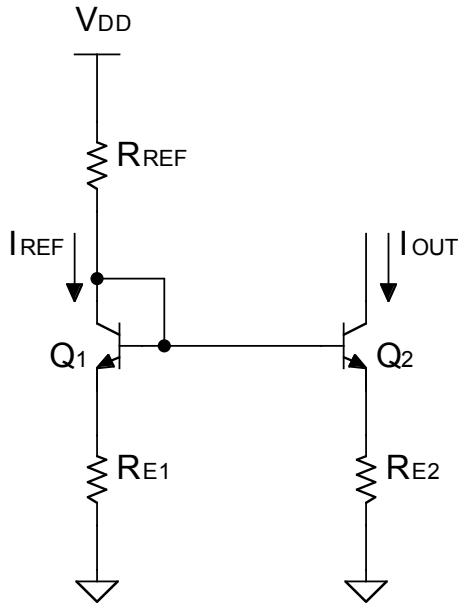

Figure 2.26: Current mirror

The performance of the simple current mirror can be improved by the addition of emitter degeneration: this solution permits to obtain a better matching between the current of the reference branch and that of the branch to biasing, and it boosts the output resistance of the system.
In a current mirror the emitter areas of transistors may be matched or ratioed. Considering Fig. 2.26, if the aim is to obtain $I_{OUT} = kI_{REF}$ the transistor Q_2 has to be k-times larger than Q_1, and $R_{E2} = R_{E1}/k$. In this way, all the dc voltage drops across R_{E1} and R_{E2} would be equal. In fact, using the Kirchhoff's voltage law around the loop including Q_1 and Q_2 and neglecting base currents:

$$I_{REF}R_{E1} + V_T ln\frac{I_{REF}}{I_{S1}} = I_{OUT}R_{E2} + V_T ln\frac{I_{OUT}}{I_{S2}} \tag{2.23}$$

From the equation (2.23), the expression for the current I_{OUT} can be derived:

$$I_{OUT} = \frac{1}{R_{E2}}\left(I_{REF}R_{E1} + V_T ln\frac{I_{REF}}{I_{OUT}}\frac{I_{S2}}{I_{S1}}\right) \tag{2.24}$$

Since $I_{OUT} = kI_{REF}$, and reminding that $I_{S1,2} \propto A_{E1,2}$ (where $A_{E1,2}$ is the emitter area of Q_1 and Q_2, respectively), the last term into brackets in (2.24) goes to zero:

$$I_{OUT} = \frac{R_{E1}}{R_{E2}}I_{REF} = kI_{REF} \tag{2.25}$$

From this analysis, if the voltage drops across R_{E1} and R_{E2} are much greater than V_T, the current gain is determined primarily by the ratio R_{E1}/R_{E2}, and only to a secondary extent by the emitter area ratio, because of the logarithmic term in (2.24).

2.9 Alternative topology

In the paragraph dedicated to the evalution of the noise performance, it has been noted as the resistance related to the base inductance is one of the main contribution to the noise figure of the low noise amplifier. Since a perfect input impedance matching is not required, the idea is to avoid this inductance, eliminating a degree of freedom of the design, but offering the possibility to improve the noise performance. This is the key idea of the design presented in this section. The low noise amplifier topology described in the following is illustrated in Fig. 2.27, where the ESD protection inductance is also reported, connected to the base of the input transistor, which has to be considered in the evaluation of the input matching network.

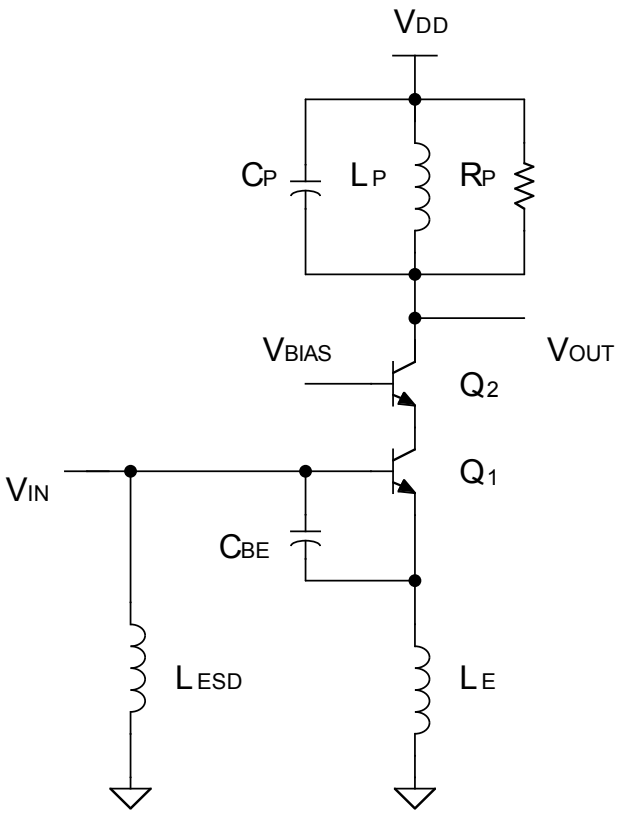

Figure 2.27: LNA2 - Topology

The design procedure is the same as presented in the previous paragraphs. However, with this structure the equivalent circuit of the input matching network is different, as the values of the reactive elements, compared to the previous case. In addition, if in the topology of Fig. 2.5 the capacitance C_{BE} can be added to increase the degrees of freedom in the design of the low noise amplifier, now it becomes necessary to realize the input impedance matching.

As a first step, it is important to implement the active device matching, choosing the optimum current density J_{Copt} with the purpose to obtain the best noise performance. Thus, in Fig. 2.28 the minimum noise figure NF_{MIN} at 10 GHz is plotted as a function of the collector current density J_C. Observing this graph, at the operating frequency, the minimum value $NF_{MIN} = 1.26\,\text{dB}$ is obtained for an optimum noise current density $J_{Copt} = 0.72\,\text{mA}/\mu\text{m}^2$. The optimum current density is approximately the same of the previous case, but the different topology determines a higher value of the NF_{opt}. Although this value is higher than that one obtained with the first topology, the absence of the base inductor may determine an advantage in terms of noise performance.

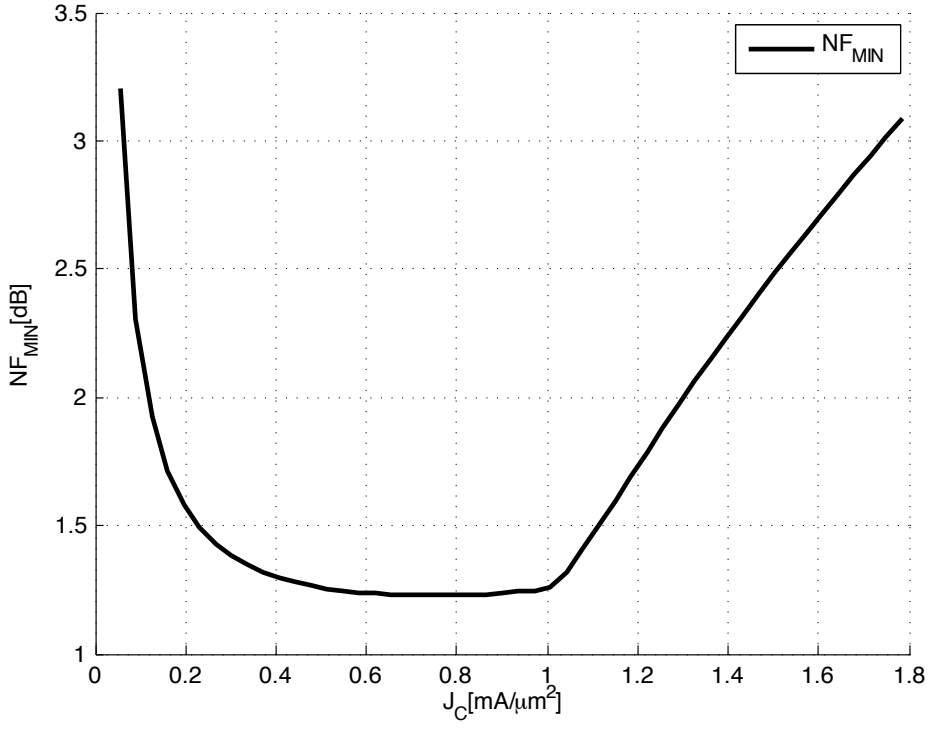

Figure 2.28: LNA2 - Optimum noise current density

Once the optimum bias current density J_{Copt} has been selected, the bias current is fixed as in the previous case $I_C = 9\,\text{mA}$ for each transistor considering the linearity and power consumption, and also in order to easily compare the performance of the two topologies of low noise amplifier.

The size of the devices, determined by the emitter length l_E and the number of parallel devices M, is chosen to achieve the value of J_{Copt} and to set the optimum noise impedance of the low noise amplifier equal to the signal source impedance. For this reason, using the simulator, it is possible to obtain the value of the minimum noise figure NF_{MIN}, current density J_C and optimum noise impedance Z_{Sopt} at the operating frequency 10 GHz, varying the number of parallel devices and the emitter length, as reported in the following Tab. 2.5. Analyzing this table, remembering that the emitter width is set to the minimum value for the best noise performance and each transistor has two emitters, the parameter M is fixed to 3 and a $10\,l_{\text{REF}}$ value of emitter length is adopted, where l_{REF} is a reference emitter length.

Also with this second topology of low noise amplifier there are some degrees of freedom in the choice of the parameters M and l_E. For example, consulting Tab. 2.5, also the choices $M = 4$ or $M = 5$, with a suitable emitter length, would be valid, obtaining NF_{MIN} and Z_{Sopt} values close to the best case just discussed.

	$\mathbf{l_E}$[µm]	$\mathbf{NF_{MIN}}$[dB]	$\mathbf{J_C}$[mA/µm^2]	$\mathbf{Z_{Sopt}}$[Ω]
M=2	$4\,l_{\mathrm{REF}}$	1.60	2.56	160
	$5\,l_{\mathrm{REF}}$	1.50	2.05	150
	$6\,l_{\mathrm{REF}}$	1.43	1.70	141
	$7\,l_{\mathrm{REF}}$	1.38	1.46	135
	$8\,l_{\mathrm{REF}}$	1.35	1.28	130
	$9\,l_{\mathrm{REF}}$	1.32	1.14	125
	$10\,l_{\mathrm{REF}}$	1.30	1.02	120
M=3	$4\,l_{\mathrm{REF}}$	1.44	1.70	141
	$5\,l_{\mathrm{REF}}$	1.37	1.36	130
	$6\,l_{\mathrm{REF}}$	1.33	1.14	125
	$7\,l_{\mathrm{REF}}$	1.30	0.97	120
	$8\,l_{\mathrm{REF}}$	1.28	0.85	115
	$9\,l_{\mathrm{REF}}$	1.27	0.76	113
	$10\,l_{\mathrm{REF}}$	1.26	0.68	108
M=4	$4\,l_{\mathrm{REF}}$	1.36	1.28	127
	$5\,l_{\mathrm{REF}}$	1.31	1.02	120
	$6\,l_{\mathrm{REF}}$	1.28	0.85	116
	$7\,l_{\mathrm{REF}}$	1.27	0.73	115
	$8\,l_{\mathrm{REF}}$	1.26	0.64	117
	$9\,l_{\mathrm{REF}}$	1.27	0.57	120
	$10\,l_{\mathrm{REF}}$	1.28	0.51	125
M=5	$4\,l_{\mathrm{REF}}$	1.32	1.02	120
	$5\,l_{\mathrm{REF}}$	1.28	0.82	115
	$6\,l_{\mathrm{REF}}$	1.27	0.68	117
	$7\,l_{\mathrm{REF}}$	1.27	0.58	120
	$8\,l_{\mathrm{REF}}$	1.28	0.51	125
	$9\,l_{\mathrm{REF}}$	1.30	0.45	130
	$10\,l_{\mathrm{REF}}$	1.32	0.41	135

Table 2.5: LNA2 - Active device matching

Tab. 2.6 summarizes the results obtained with the better choice for the number of parallel device M and the emitter length l_E.

	$\mathbf{l_E}$[µm]	$\mathbf{NF_{MIN}}$[dB]	$\mathbf{J_C}$[mA/µm^2]	$\mathbf{Z_{Sopt}}$[Ω]
M=3	$10\,l_{\mathrm{REF}}$	1.26	0.68	108

Table 2.6: LNA2 - Optimum sizing

The next step, as with the first topology of low noise amplifier, is to realize the input impedance matching. It is possible to consider the equivalent reactive input network shown in Fig. 2.29, to evaluate the input impedance of the system.

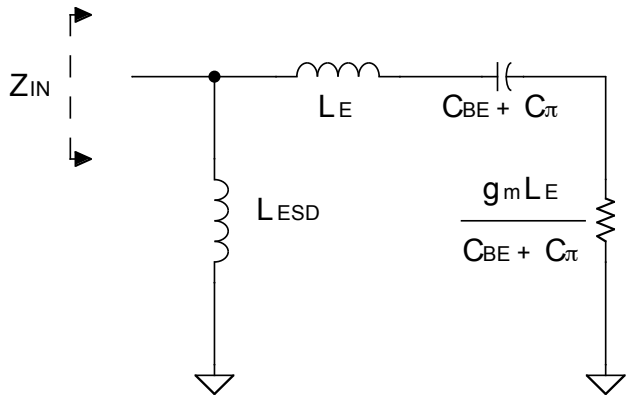

Figure 2.29: LNA2 - Input resonant network

From the equivalent circuit illustrated in Fig. 2.29, without considering the effect of the ESD protection inductor L_{ESD}, the two following equations have be satisfied, to realize the input impedance matching with the source resistance $R_S = 50\,\Omega$ at the operating frequency:

$$\begin{cases} \frac{g_m L_E}{C_{BE}+C_\pi} = R_S \\ \omega_0 L_E - \frac{1}{\omega_0 (C_{BE}+C_\pi)} = 0 \end{cases}$$

This analytical system has not a mathematical solution for appropriate values of the reactive components, so considering the specifications about the parameter $S11$ and the noise figure NF it is possible to set the values of C_{BE} and L_E through the simulator. However, since the ESD protection inductor L_{ESD} has a direct influence

on the input matching network, it is also appropriate to consider its effect in the operation of tuning just discussed. Considering Fig. 2.29, it is possible to calculate the input impedance as indicated in the following expression (2.26):

$$Z_{IN}(s) = sL_{ESD} // \left(sL_E + \frac{1}{s(C_{BE} + C_\pi)} + \frac{g_m L_E}{C_{BE} + C_\pi} \right) \tag{2.26}$$

Then, evaluating the frequency response of $Z_{IN}(s)$, the value of the components of input network are set in order to obtain an input resistance of about 50Ω, considering the single-ended model, and an imaginary part close to zero. Thus, from simulation, $C_{BE} = 150\,\text{fF}$ and $L_E = 100\,\text{pF}$, with a coupling capacitance of $3\,\text{pF}$ and $L_{ESD} = 1\,\text{nH}$. The design of the output resonant network is performed in a similar way as discussed for the first solution of low noise amplifier presented. Considering the effect of the same buffer discussed in the previous paragraphs linked to the output, referring to Fig. 2.27, it is setted $L_P = 1\,\text{nH}$, $C_P = 80\,\text{fF}$ and $R_P = 125\,\Omega$. The implemented circuit uses a differential topology, and the output network is illustrated in Fig. 2.13; thus, with this architecture the resistance value is doubled, while the value of the capacitance is halved. Finally, regarding the linearity performance, an IIP3$=-0.85\,\text{dBm}$ is obtained.
The real and imaginary part of the input impedance, $S11$ and $S21$ parameters, the trend of NF_{MIN} and NF are shown in figures Fig. 2.30, Fig. 2.31, and Fig. 2.32.

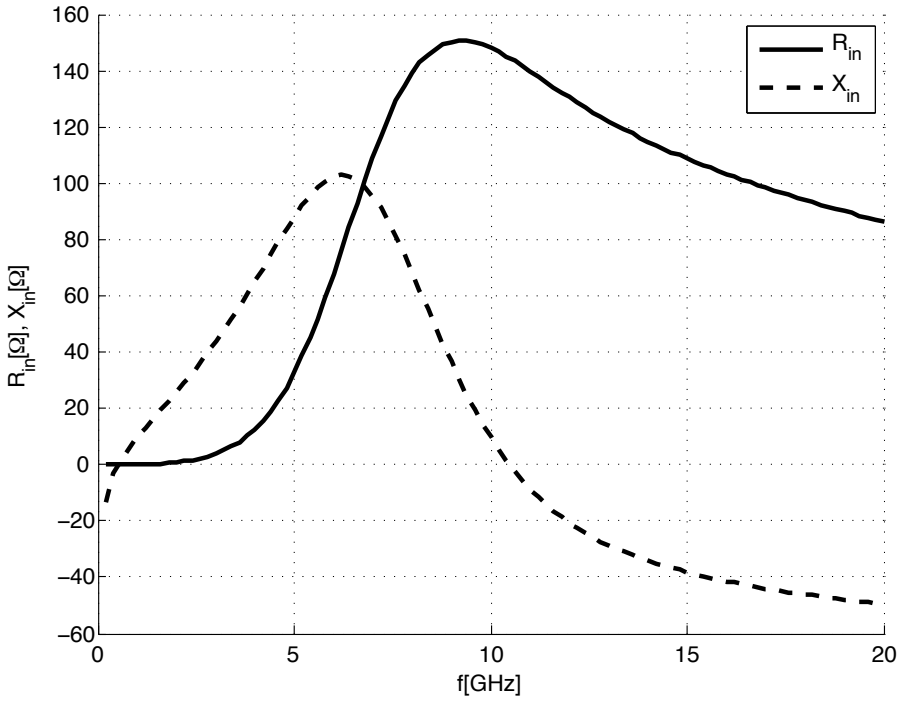

Figure 2.30: LNA2 - Input impedance

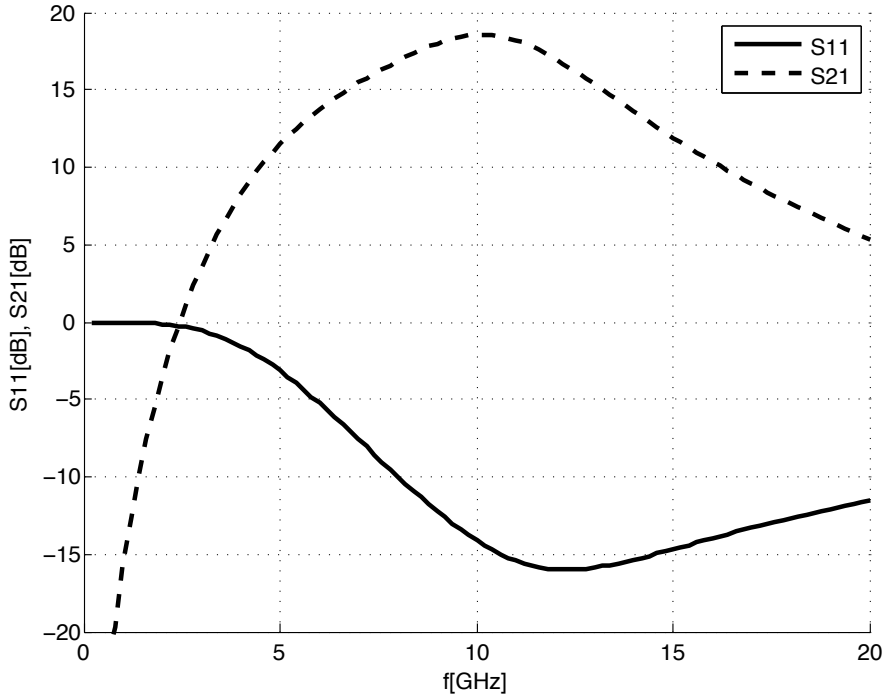

Figure 2.31: LNA2 - S-parameters

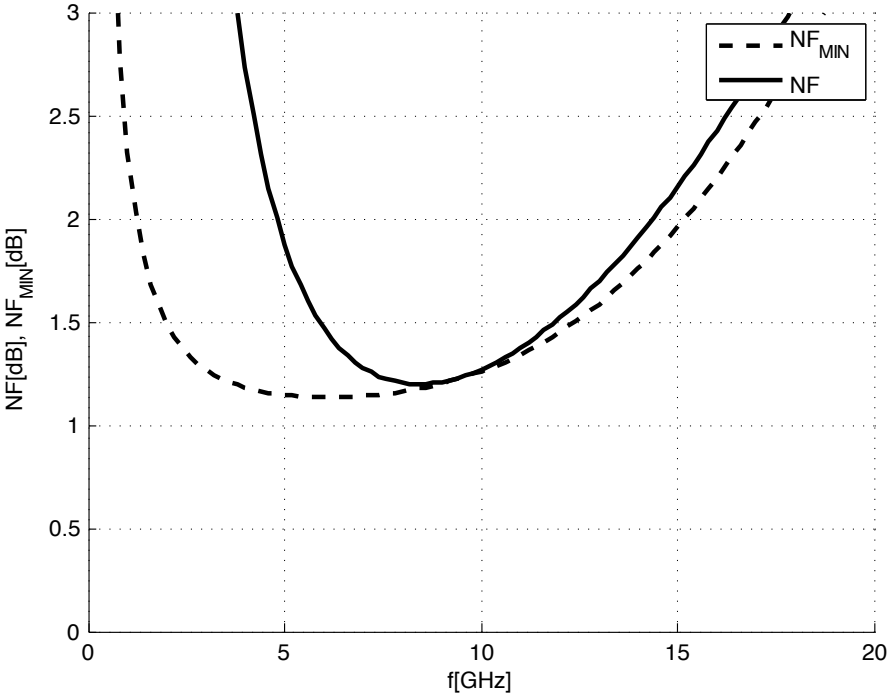

Figure 2.32: LNA2 - Noise performance

Considering the implemented differential topology, at 10 GHz the real part of the input impedance is equal to 148 Ω, while the imaginary term is 10 Ω. The parameter $S11$ has a value of −14.1 dB at 10 GHz and it is less than −10 dB in the frequency range $8 \div 23$ GHz. At the operating frequency, $S21 = 18.6$ dB, with a bandwidth $BW_{-3dB} = 5.7$ GHz. Finally, $NF_{MIN} = 1.26$ dB and $NF = 1.27$ dB at the operating frequency.
As discussed for the first structure of low noise amplifier, through the electromagnetic simulator, the inductors of the circuit are realized. The topolgy for the ESD protection and degeneration inductors is shown in Fig. 2.33, while Fig. 2.34 illustrates the load inductors structure.

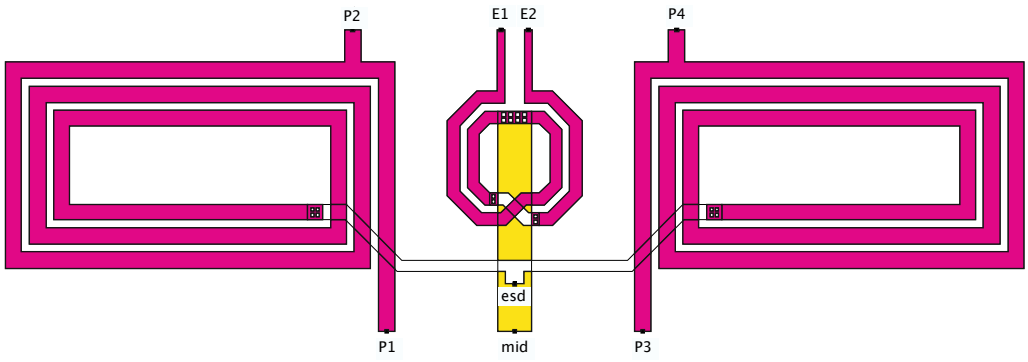

Figure 2.33: LNA2 - ESD protection and degeneration inductors

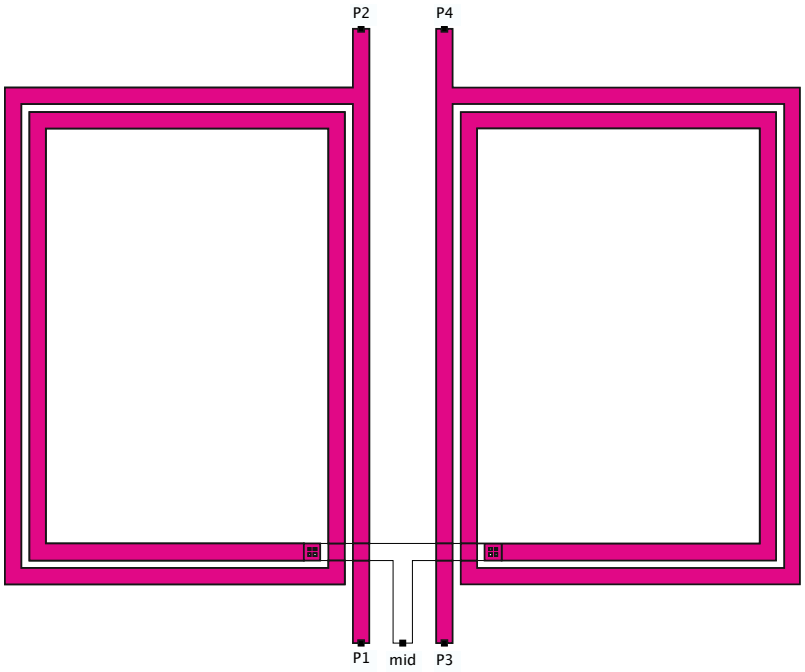

Figure 2.34: LNA2 - Load inductors

As in the previous case, the finite value of the quality factor Q of inductors determines the necessity to slightly modify the value of the components of the input and output resonant networks. In particular, the emitter degeneration inductor obtained is $L_E = 95\,\text{pH}$, so it is 190 pH considering the differential structure, and $L_{ESD} = 980\,\text{pH}$; also the cascode stage is simplified, using transistors with $M = 1$. For the output network, $L_P = 1.1\,\text{nH}$, $R_P = 165\,\Omega$, $C_P = 140\,\text{fF}$, which are respectively 1.1 nH, 330 Ω, and 70 fF in the differential topology of Fig.2.13. Tab. 2.7 summarizes the features of the ESD protection inductor, differential degeneration inductor, and load inductor designed with the electromagnetic simulator. In this table the values of the inductance L at 10 GHz, the number of turns n, the width w used for metal layer 6, the self resonance frequency f_0, the quality factor Q, and the required area for each inductor are reported. It is also important to remember that the thickness of metal layer 4, 5, and 6 is fixed at 0.39 µm, 1 µm, and 2.8 µm, respectively.

	ESD protection inductor	**Degeneration inductor**	**Load inductor**
L[nH]	0.980	0.190	1.110
n	3	2	2
w[μm]	5.3	4.0	5.3
f_0[GHz]	37	157	32
Q	16	8	16
area[μm^2]	125x90	60x60	190x130

Table 2.7: LNA2 - Inductors features

Finally, in Fig. 2.35 and Fig. 2.36 the frequency responses of the parameters $S11$ and $S21$, and of the noise figure NF and minimum noise figure NF_{MIN} are illustrated. The dip of $S11$ at the operating frequency 10 GHz is −15.6 dB, and it is less than −10 dB from 7.3 GHz to 18.1 GHz. The value of $S21$ at 10 GHz is 18.8 dB, with a -3dB bandwidth of 5 GHz. Regarding the noise performance, $NF = 1.65\,\text{dB}$ and $NF_{MIN} = 1.64\,\text{dB}$ at the operating frequency. Thus, compared to the case of ideal inductors, the noise figure is increased of 0.38 dB, but better noise results than the previous topology of low noise amplifier discussed are achieved, because with this structure the ESD protection is already implemented.

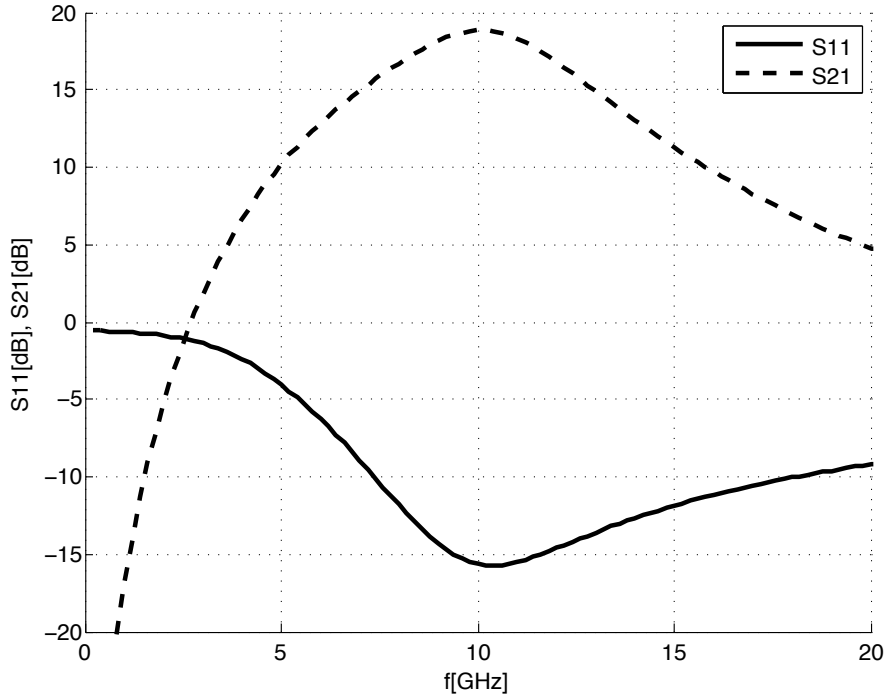

Figure 2.35: LNA2 - $S11$ and $S21$ parameters

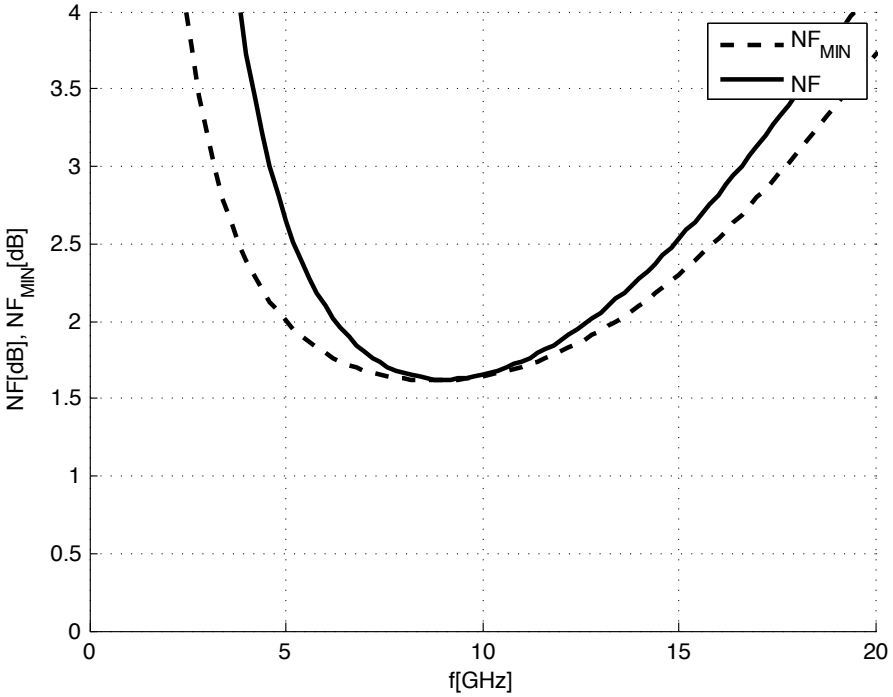

Figure 2.36: LNA2 - NF_{MIN} and NF

2.10 Design summary and results

The purpose of this paragraph is to summarize the design method and the obtained results, considering the initial target specifications, for the design of the X-band low noise amplifier, taking into consideraton both solutions discussed in the previous sections. In addition, the effects on the main figures of merit of a slight variations of the circuit parameters are also evaluated, observing that the behavior of the two low noise amplifier topologies presented is similar.
Here, it is briefly summarized the low noise amplifier design philosophy followed to implement the structures discussed:

- Select the topology with the lowest number of transistors and passive components, since each device will contribute noise.
- Bias the transistors at the minimum noise figure current density J_{Copt} of the topology to achieve the lowest value of minimum noise figure NF_{opt} at the operating frequency.
- Set the transistor size, emitter length l_E and number of parallel devices M, which corresponds to the desired optimum noise impedance R_{Sopt}, that is the source resistance value.
- Add reactive feedback to transform the real part of the input impedance to the desired value, at the operating frequency.
- Add reactive matching network to tune out the imaginary parts of the input impedance and optimum noise impedance X_{Sopt}.
- Add reactive matching network to tune the output at the operating frequency.

Following the design method just discussed, it is possible to achieve the results presented in this work. Although it may be considered a completely theoretical approach, the implementation of the system makes extensive use of the circuit simulator, considering the behavior of the components according to their analytical model. Fig. 2.37 and Fig. 2.38 illustrate the differential circuit of the low noise amplifiers implemented, including the ESD protection devices and the emitter follower connected to the output. The biasing is realized through current mirror circuits with mirror ratio of 1 : 10 and 1 : 5, as explained in section 2.8. Finally, the supply voltage V_{DD} is set to 3.3 V, while $V_{SS} = 0\,\mathrm{V}$.
In Fig. 2.37 the first analyzed low noise amplifier topology, with series base inductances, is illustrated, and the final values of the components are summarized in Tab. 2.8.

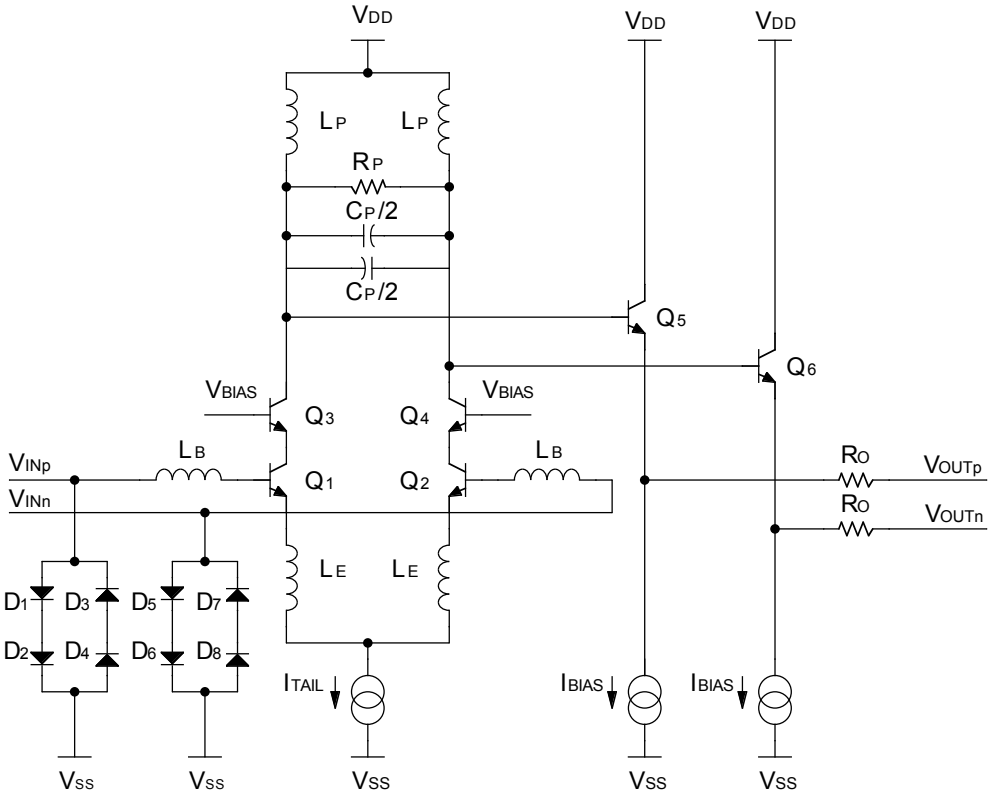

Figure 2.37: LNA1 - Schematic

L_B[pH]	L_E[pH]	R_P[Ω]	L_P[nH]	C_P[fF]	R_O[Ω]	I_{TAIL}[mA]	I_{BIAS}[mA]
990	85	250	1.11	60	50	18	7

Table 2.8: LNA1 - Components values

As shown in Fig.2.37, for a reason of symmetry the capacitance C_P is implementing using two capacitors $C_P/2$. In addition, while the emitter width is fixed for each device at the minimum value to obtain the best noise performance, the emitter length l_E for each transistor is set as explain in the previous paragraphs. The transistor Q_1, Q_2, Q_3, and Q_4 have a structure with three bases, while Q_5 and Q_6 have only two bases. The input differential pair (Q_1 and Q_2) is composed by $M = 3$ parallel devices. The ESD diodes are the smaller devices available with this technology.
In Tab. 2.9 the results about the main figures of merit of the system are shown.

f [GHz]	**S11 [dB20]**	**S21 [dB20]**	**NF [dB10]**	**IIP3[dBm]**
10	-19.5	18.6	1.88	-2.1

Table 2.9: LNA1 - Design results

The final value of each component is set following the design procedure described. It is also interesting to observe how the figures of merit change modifying the design parameters. Tab. 2.10 shows qualitatively the effect of changes in design parameters on the main figures of merit, where the "+" symbol implies an improvement, the "-" symbol indicates a worsening and the "/" symbol means that there is no variation.

Parameter	NF	$IIP3$	$S11$	$S21$
$L_E \uparrow$	-	+	-	-
$L_B \uparrow$	-	-	+	/
$R_P \uparrow$	+	-	/	+

Table 2.10: LNA1 - Parameters variations

The schematic of the second topology of low noise amplifier implemented, without the series base inductances, but with the ESD protection inductances, is shown in Fig. 2.38, and the values of the components are reported in the following Tab. 2.11. Compared to the previous design, the bias current of the core and of the emitter follower are the same, so also the power consumption remains the same, thus it is possible to evaluate the differences in performance of the two topologies.
Also in this case, two capacitances are used for the output resonant network, with the goal of maintaining the symmetry of the circuit.

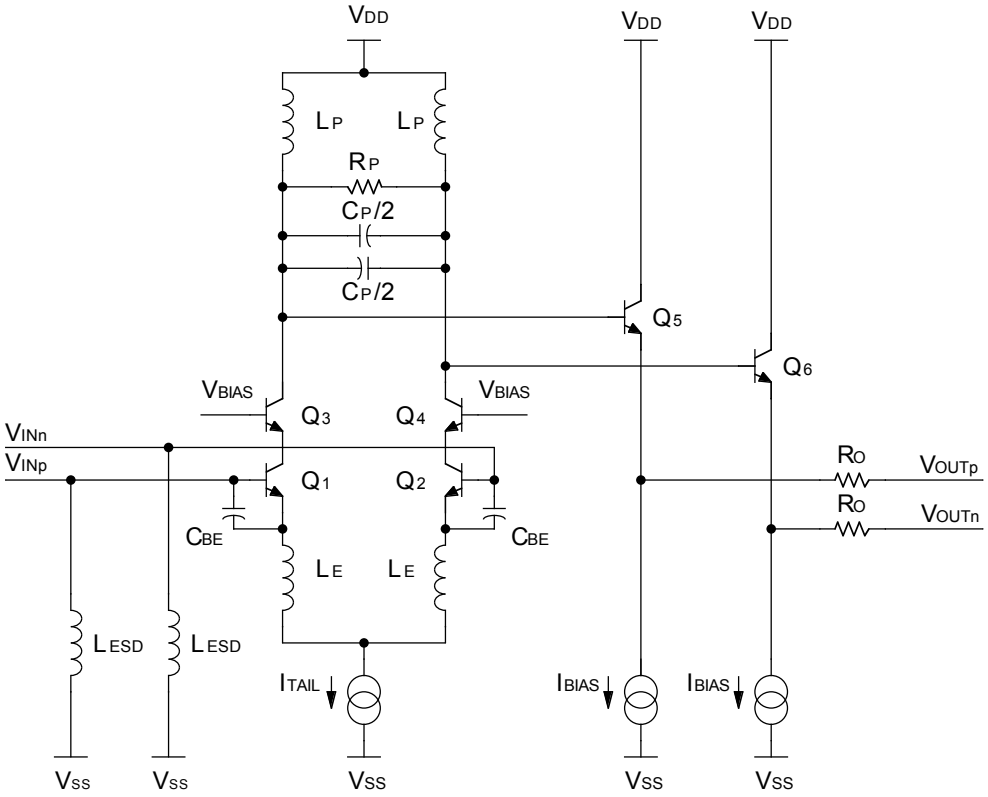

Figure 2.38: LNA2 - Schematic

L_{ESD}[pH]	L_E[pH]	R_P[Ω]	L_P[nH]	C_P[fF]	R_O[Ω]	I_{TAIL}[mA]	I_{BIAS}[mA]
980	95	330	1.11	70	50	18	7

Table 2.11: LNA2 - Components values

As for the previous design, fixing the emitter width of each transistor at the minimum value, the emitter length l_E for each device of Fig. 2.38 is set for the best noise performance. Transistors Q_1, Q_2, Q_3, and Q_4 have a structure with three bases, while Q_5 and Q_6 have two bases. Only the input differential pair has a topology with $M = 3$ parallel devices.

Tab. 2.12 illustrates the results regarding the main figures of merit of the low noise amplifier obtained with this second topology. In particular, it is clear that the noise performance is improved compared to the first low noise amplifier topology. This is due to the fact that the base inductances are deleted and the ESD protection devices are an integral part of the input matching network.

f [GHz]	**S11 [dB20]**	**S21 [dB20]**	**NF [dB10]**	**IIP3[dBm]**
10	-15.6	18.8	1.65	-1.2

Table 2.12: LNA2 - Design results

In Tab. 2.13 the effects of changes in design parameters on the main figures of merit are shown for this second structure, where the "+" symbol implies an improvement, the "-" symbol indicates a worsening and the "/" symbol means that there is no variation, due to the increasing of the specific circuit parameter.

Parameter	NF	$IIP3$	$S11$	$S21$
$L_E \uparrow$	-	+	-	-
$L_{ESD} \uparrow$	+	-	+	+
$C_{BE} \uparrow$	-	+	+	-
$R_P \uparrow$	+	-	/	+

Table 2.13: LNA2 - Parameters variations

3 Wide-band low noise amplifier design

Wide-band low noise amplifiers are functional blocks largely used in communication systems. In general, their noise performance is lower than narrow-band low noise amplifiers, but they allow to realize the input matching and gain on a wider bandwidth. In addition, one of the main benefit is the area savings, because, usually, there are no inductors. The two main design approaches for this type of low noise amplifier consist into realizing the input matching using a bandpass filter or to implement a resistive feedback technique. Although resistive feedback is generally considered inferior as far as the noise performance is concerned, an appropriate choice of the feedback resistor can minimize the noise contribution while realizing the input and output matching.

Considering the large field of application of wide-band amplifiers, in this section the purpose is to present the design of a transimpedance amplifier (TIA) using a shunt-shunt feedback resistor. The goal is to provide a low input impedance, ensuring also low noise and high gain. The typical topology of a transimpedance amplifier is the shunt-shunt feedback structure shown in Fig. 2.39, where an ideal inverting voltage amplifier is connected with a feedback resistance R_F, and C_{IN} is the input capacitance of the stage, which determines the bandwidth of the system. In this structure a negative feedback network senses the voltage at the output and returns a proportional current to the input. From the analysis of Fig.2.39, it is possible to obtain:

$$\begin{cases} Z_T = \frac{V_{OUT}}{I_{IN}} = -\frac{A}{A+1}\frac{R_F}{1+j\omega\frac{R_F C_{IN}}{A+1}} \\ BW_{-3dB} \simeq \frac{1}{2\pi}\frac{A}{R_F C_{IN}} \end{cases}$$

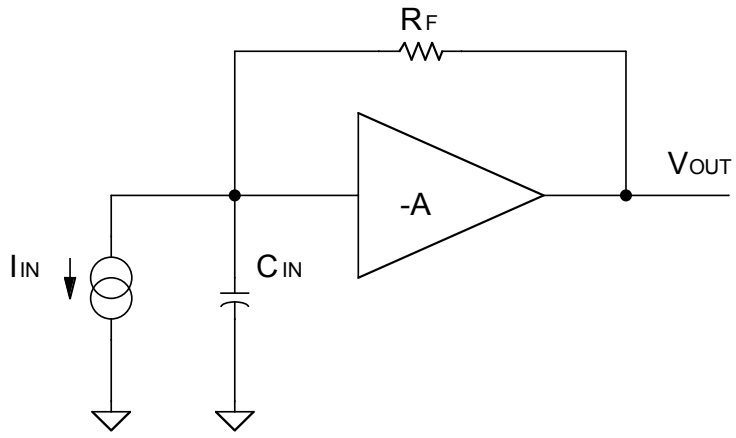

Figure 2.39: TIA - General structure

3.1 Transimpedance amplifier analysis

A common transistor implementation of the feedback transimpedance amplifier is shown in Fig. 2.40, where the single-ended circuit is presented. The source signal V_S and the source resistance R_S are also considered. The amplifier consists of a common emitter stage and an output buffer can be added to isolate the main stage from the load.

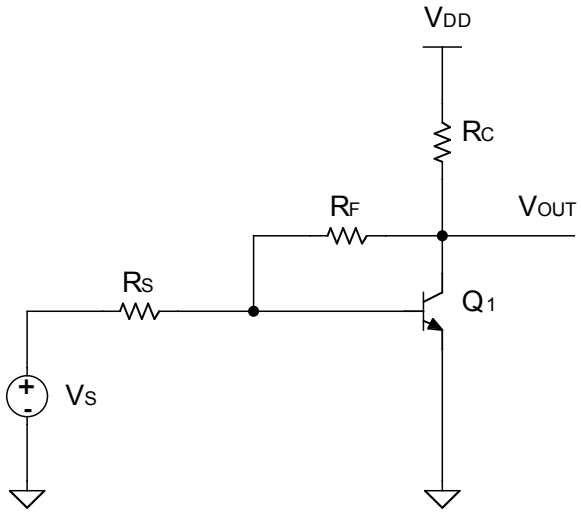

Figure 2.40: TIA - Topology

Starting from the small signal model, which is illustrated in Fig. 2.41, the block diagram shown in Fig. 2.42 is derived, where the characteristic parameters of a feedback structure are shown: W_S is the pre-processing block, A_{OL} is the open loop gain and β is the feedback factor. In addition, in this block diagram the currents at the comparison node at the input are the source current $I_S = V_S/R_S$ (Norton representation of the source), the feedback current I_F, and the error current I_E.

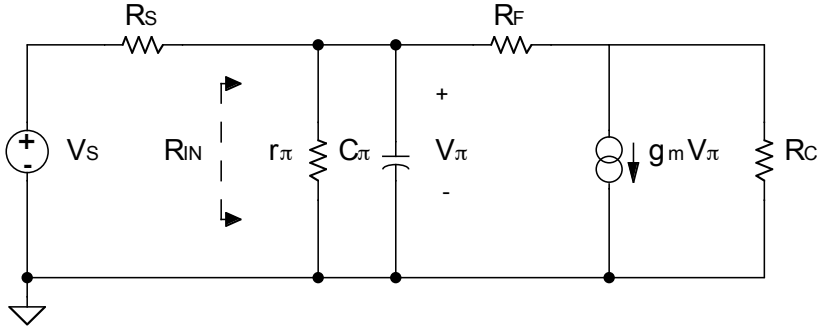

Figure 2.41: TIA - Small signal model

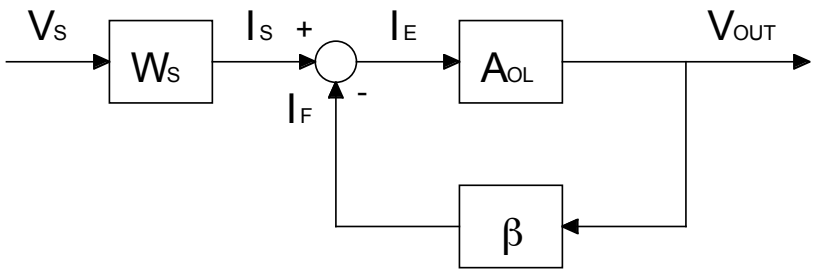

Figure 2.42: TIA - Block diagram

From the circuit analysis, it is possible to determine the parameters which appear in the block diagram shown in Fig. 2.42

$$\begin{cases} W_S = \frac{I_S}{V_S} = \frac{1}{R_S} \\ A_{OL} = -g_m(R_C//R_F)(R_S//R_F//r_\pi) \simeq -g_m(R_C//R_F)(R_S//R_F) \\ \beta = -\frac{1}{R_F} \end{cases}$$

Considering these expressions, the loop gain T of the system can be determined:

$$T = \beta A_{OL} = g_m \frac{R_C//R_F}{R_F}(R_S//R_F//r_\pi) \simeq g_m \frac{R_S}{R_S + R_F}(R_C//R_F) \tag{2.27}$$

Observing the block diagram in Fig. 2.42, it is possible to calculate the transimpedance gain A_F and the voltage gain A_V as shown in (2.28) and (2.29):

$$A_F = \frac{V_{OUT}}{I_S} = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{1}{\beta}\frac{T}{1+T} = -R_F\frac{T}{1+T} \tag{2.28}$$

$$A_V = \frac{V_{OUT}}{V_S} = W_S A_F = -\frac{R_F}{R_S}\frac{T}{1+T} \tag{2.29}$$

From (2.28), it is clear that if $T >> 1$, the transimpedance gain A_F is approximately equal to $-Rf$ and, under the same condition, $A_V \simeq -R_F/R_S$. However, as analyzed in the following, the desire to achieve the input matching does not allow to obtain high loop gain. Finally, considering the small signal circuit shown

in Fig. 2.41, it is also possible to estimate the input resistance R_{IN} of the system, as indicated in the following expression (2.30):

$$R_{IN} \simeq \frac{R_F + R_C}{1 + g_m R_C} \tag{2.30}$$

3.2 Specification and design

The purpose is to realize a low noise amplifier in the X-band ($9 \div 11\,\text{GHz}$). In particular, the interest is to implement an inductorless topology with the aim to save area on the chip. Firstly, we have to ensure the input matching of the system with the condition $S11 < -10\,\text{dB}$. Therefore, imposing the perfect matching condition $R_S = R_{IN}$:

$$R_S = \frac{R_F + R_C}{1 + g_m R_C} \Rightarrow g_m R_S R_C = R_C + R_F - R_S \tag{2.31}$$

Hence, considering the expression for the loop gain T presented in (2.27) and replacing the relation (2.31):

$$T = g_m \frac{R_S}{R_S + R_F} \frac{R_C R_F}{R_C + R_F} = \frac{R_F}{R_F + R_S} \frac{R_C + R_F - R_S}{R_C + R_F} < 1 \tag{2.32}$$

From the equation above, it is clear that it is not possible to realize a matching very close to the ideal case and, at the same time, to obtain a loop gain greater than one. However, the specification requires $|S11| < -10\,\text{dB}$, that is $25\,\Omega < R_{IN} < 97\,\Omega$. Thus, imposing $R_{IN} = kR_S$, with $k = 0.5 \div 1.9$, and evaluating again the expression for the loop gain T:

$$T = g_m \frac{R_S}{R_S + R_F} \frac{R_C R_F}{R_C + R_F} = \frac{g_m}{R_S + R_F} \frac{R_C R_F}{k(1 + g_m R_C)} = \frac{g_m R_C R_F}{k(R_S + R_F)(1 + g_m R_C)} \tag{2.33}$$

Then, setting the condition $T > 1$ with the purpose to obtain feedback benefits, from (2.33) it is possible to determine:

$$k < \frac{g_m R_C R_F}{(R_S + R_F)(1 + g_m R_C)} \tag{2.34}$$

Finally, if $g_m R_C >> 1$ is verified, the loop gain T can be approximated as indicated in the following expression (2.35):

$$T = \frac{g_m R_C R_F}{k(R_S + R_F)(1 + g_m R_C)} \simeq \frac{R_F/R_S}{k(R_F/R_S + 1)} \tag{2.35}$$

Hence, considering $R_F/R_S >> 1$, it is possible to define an upper limit for the loop gain T. In fact, from the expression (2.35):

$$T \simeq \frac{1}{k} < 2 \simeq 6dB \tag{2.36}$$

Taking into consideration only the significant noise contributions, the shot noise sources of the transistor $Q1$ and the thermal noise of the feedback resistor R_F as indicated in Fig. 2.40, the noise figure NF of the system is given by:

$$NF \simeq 1 + \frac{r_E + r_B}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_S}{2\beta_0} + \frac{R_S}{R_F} \tag{2.37}$$

In this expression, r_E and r_B are the intrinsic emitter and base resistances of the transistor $Q1$, and β_0 is its current gain. Evaluating the expression (2.37), it is clear that the noise figure depends on the ratio R_F/R_S and on the transistor parameters. From the analysis just presented, it is possible to observe that a high ratio R_F/R_S improves the loop gain T, noise performance and the voltage gain of the system. However, loop gains greater than $T = 6\,\text{dB}$ cannot be obtained, because of the condition on the input matching. Thus, feedback benefits may be reduced, including the linearity of the structure. Therefore, the specific target is to achieve the input matching ($S11 < -10\,\text{dB}$) over a frequency band greater than 10 GHz, to obtain good linearity (IIP3$>-5\,$dBm) and noise performance, not expecting for a high value of gain. The following figures represent the discussed procedure in a graphical way. From Fig. 2.43 it is possible to set the parameter k to obtain a certain value of $S11$, considering that high values of k for a good matching determine lower values of the loop gain T. Thus, the determination of the ratio R_F/R_S for gain or noise performance of the structure sets the loop gain T of the system, as shown in Fig. 2.44. Finally, in Fig. 2.45 the gain A_V is plotted as a function of R_F/R_S for different values of loop gain T. However, it is important to remember that this methodology is based on the assumption that the condition $I_C R_C >> V_T$ is verified, which leads to an increase in power consumption.

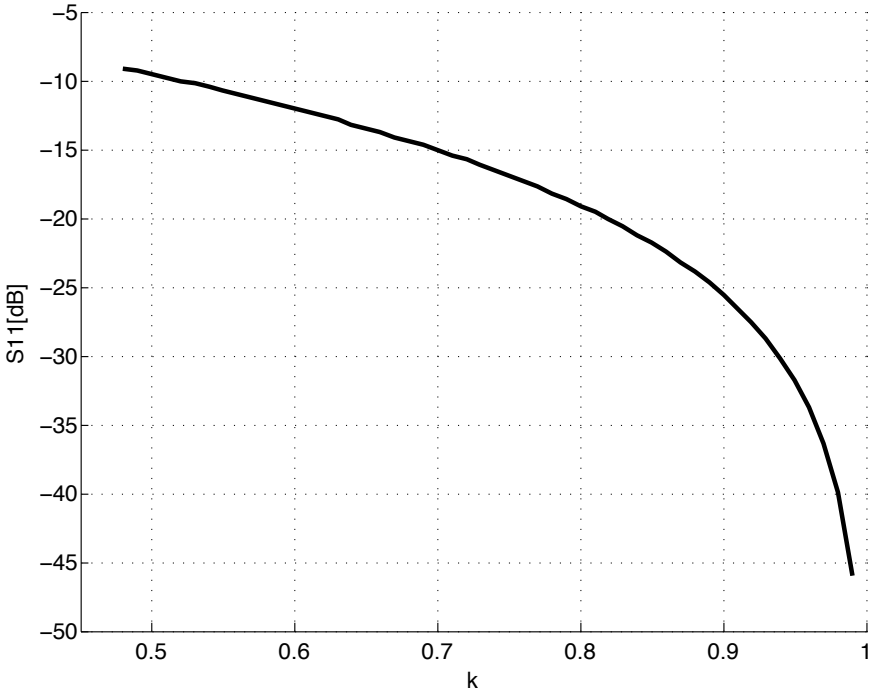

Figure 2.43: TIA - S11 design step

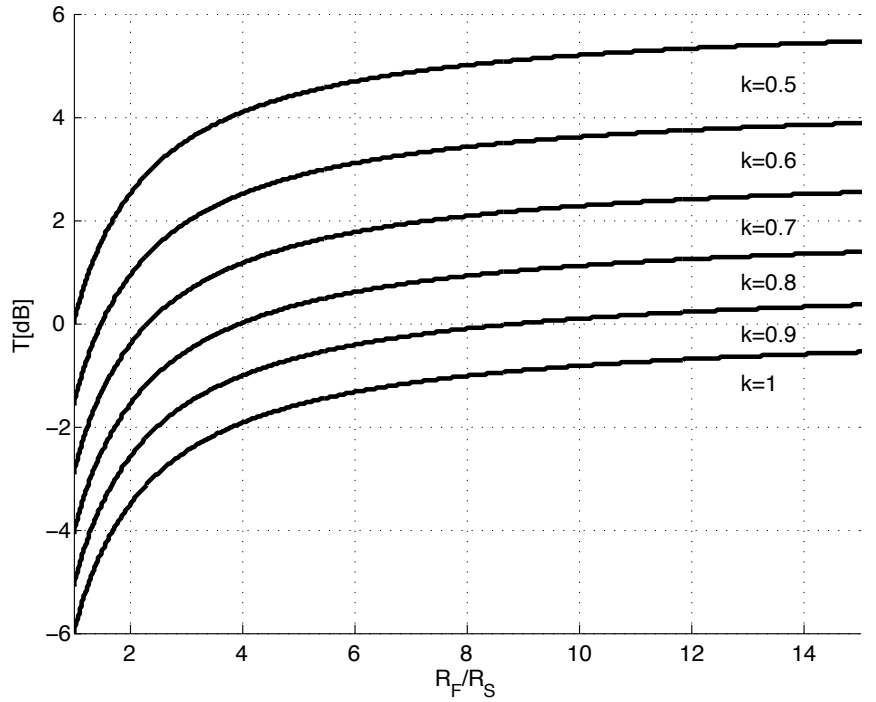

Figure 2.44: TIA - Loop gain design step

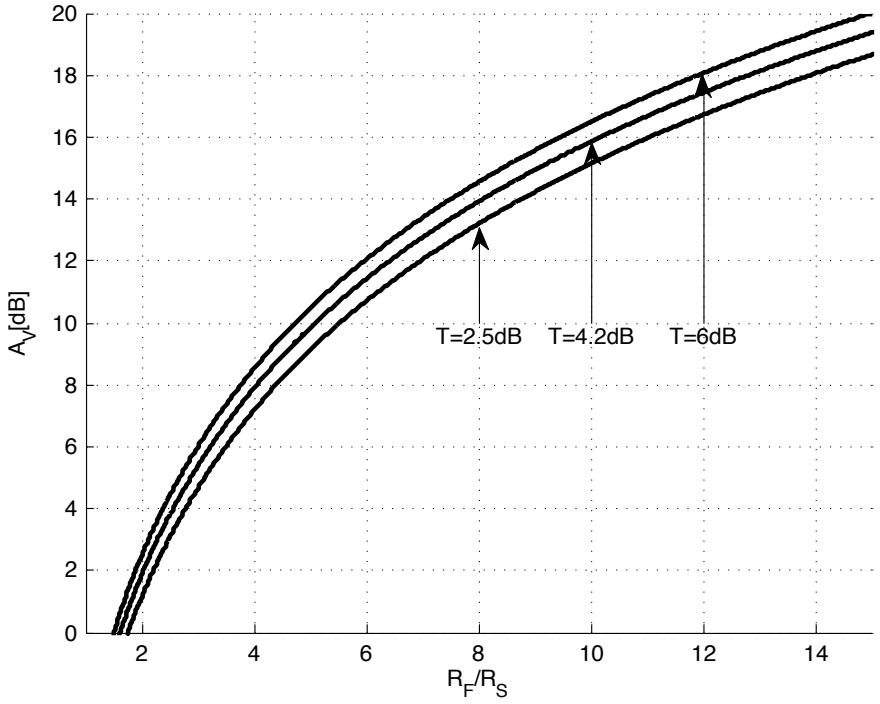

Figure 2.45: TIA - Gain design step

Tab. 2.14, shows the values chosen for the design parameters, set in accordance with the explained analysis.

g_m[mS]	$R_C[\Omega]$	$R_F[\Omega]$
150	100	400

Table 2.14: TIA - Design values

As analyzed, with the values indicated in the above table, the parameters which characterize the feedback system become:

$$\begin{cases} |A_{OL}| = 525.5 \simeq 54.4dB \\ T = 1.31 \simeq 2.37dB \\ |A_V| = 4.54 \simeq 13.1dB \\ R_{IN} = 30.9\Omega \end{cases}$$

The single-ended circuit of the amplifier considered is shown in Fig. 2.46, where a buffer is connected to the output of the transimpedance stage throught a capacitive coupling ($C_{AC} = 3pF$), with the purpose to avoid loading effects due to

the following stages. In this scheme, $R_O = 50\,\Omega$ has the task of setting the output resistance of the system. The bias currents of the two branches, I_{BIAS1} and I_{BIAS2}, are obtained by current mirrors, as discussed in section 2.8.

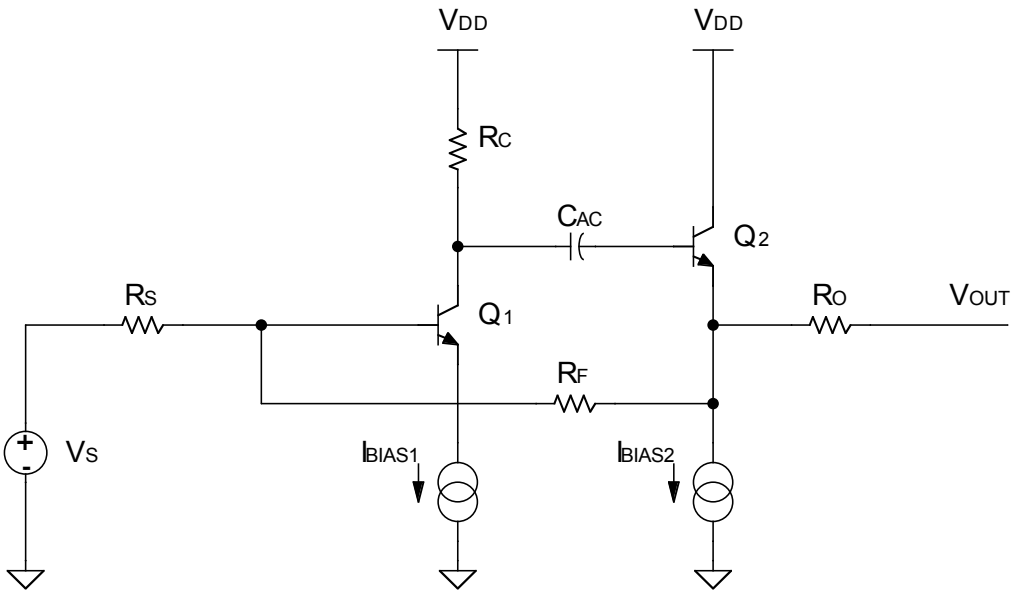

Figure 2.46: TIA - Single-ended circuit

Considerations about the value of R_F, and the compromise between input matching, loop gain and noise figure have been already presented. In addition, it is possible to use transistors with the smaller emitter width and adopting small values for the emitter length l_E, to minimize the parasitic capacitance. However, the effect of this choice on the noise figure NF of the amplifier has to be considered. Also the sizing of the transistors of the emitter follower is important, because it introduces a capacitance in the feedback loop, reducing the value of the loop gain at high frequency and worsening the overall system performance. So, the use of the simulator is very useful from this point of view, and it allow to set the transistors emitter length of the transimpedance stage and of the emitter follower.
The following figure, Fig. 2.47, Fig. 2.48, Fig. 2.49, and Fig. 2.50 illustrate, respectively, the results obtained for the magnitude and phase of the loop gain, the input impedance, the S-parameters $S11$ and $S21$ and the noise figure NF of the single-ended circuit.

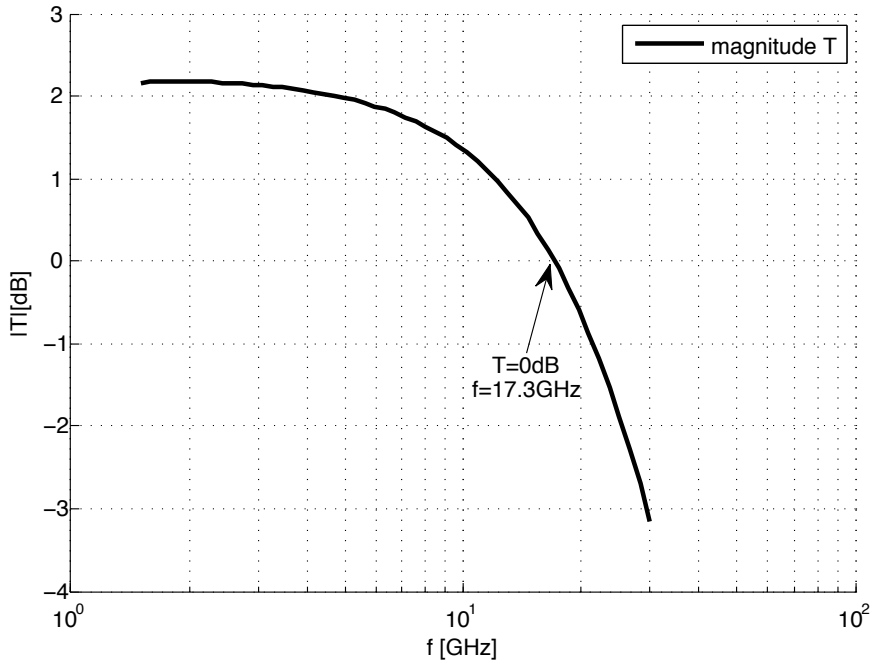

Figure 2.47: TIA - Loop gain magnitude

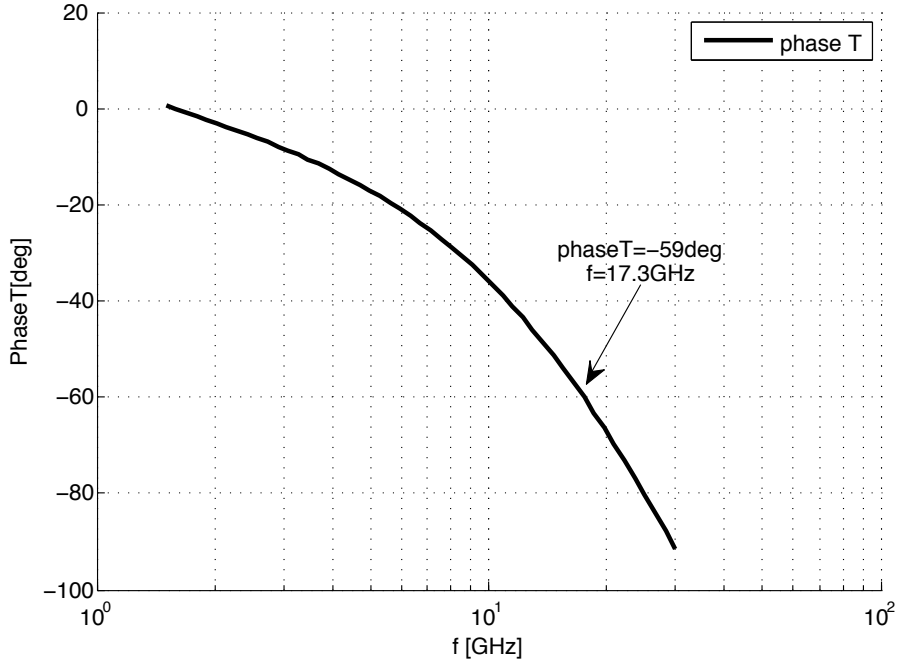

Figure 2.48: TIA - Loop gain phase

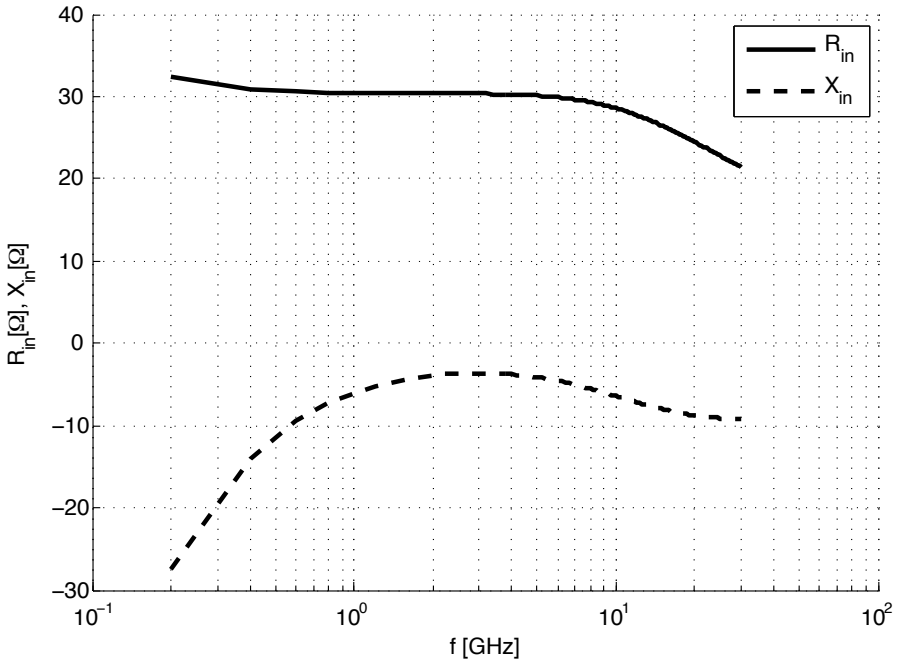

Figure 2.49: TIA - Input impedance single-ended circuit

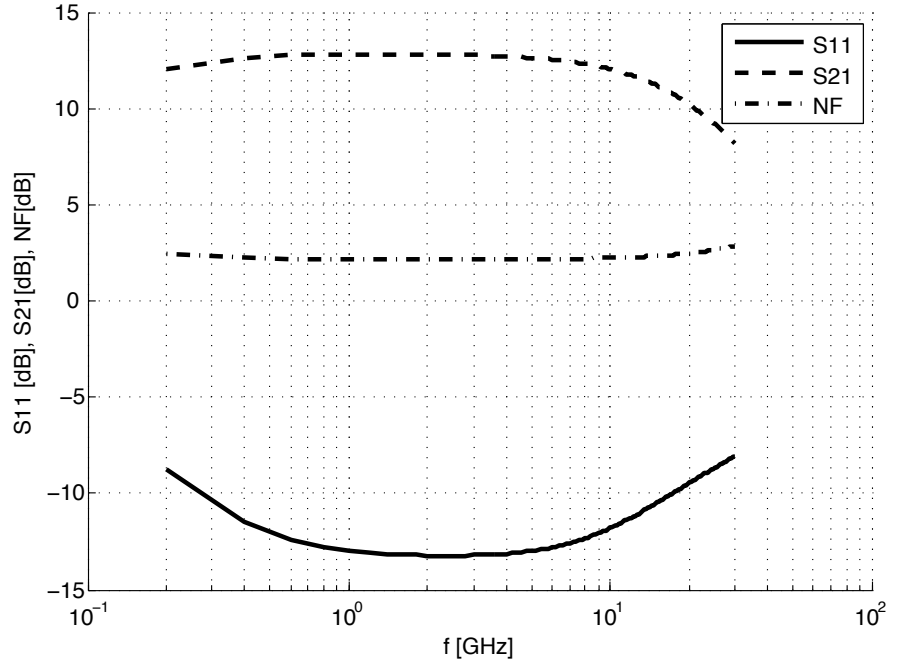

Figure 2.50: TIA - S-parameters and noise figure single-ended circuit

From Fig. 2.47 and Fig. 2.48, it is possible to observe a phase margin $PM \simeq 120°$, which ensures the stability of the system. The results of simulations related to the input impedance, the S-parameters and noise figure reflect the expected theoretical values, at least at low frequencies. In particular, a small value for the reactance X_{in} in the bandwidth $0 \div 10\,\text{GHz}$ is observed, so $Z_{in} = R_{in} + jX_{in}$ is dominated by the value of R_{in}. Considering Fig. 2.50, $S11$ remains less than $-10\,\text{dB}$ in the range $300\,\text{MHz} \div 17\,\text{GHz}$ with a minimum value of $-13.2\,\text{dB}$, the noise figure NF is approximately constant and equal to 2.1 dB in this band, and the $S21 = 12.8\,\text{dB}$, with $BW_{-3dB} \simeq 20\,\text{GHz}$. Finally, IIP3$=-3.2\,\text{dBm}$ is achieved.
The same system is implemented with a differential topology, and the results of the simulation of this circuit are presented below. In particular in Fig. 2.51 the input impedance is plotted, Fig. 2.52 shows the S-parameters $S11$, $S21$ and the noise figure NF. In the frequency range $1 \div 10\,\text{GHz}$ the input impedance of the system is approximately resistive, with a value between $75\,\Omega$ and $80\,\Omega$. This results in $S11 < -15\,\text{dB}$ in the band $300\,\text{MHz} \div 20\,\text{GHz}$, while the condition $S11 = -10\,\text{dB}$ is verified at 30 GHz. For the noise figure, the same value of the single ended simulation is obtained, $NF = 2.1\,\text{dB}$ in the band of interest, while $S21 = 12.1\,\text{dB}$ with $BW_{-3dB} \simeq 16.5\,\text{GHz}$. In this case, IIP3$=-2.7\,\text{dBm}$ is obtained.

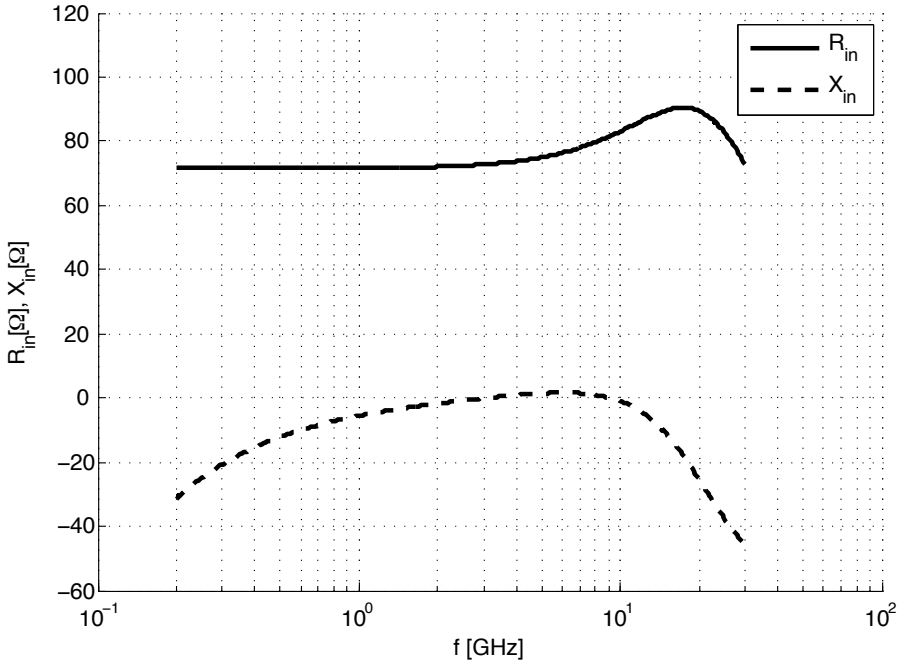

Figure 2.51: TIA - Input impedance differential circuit

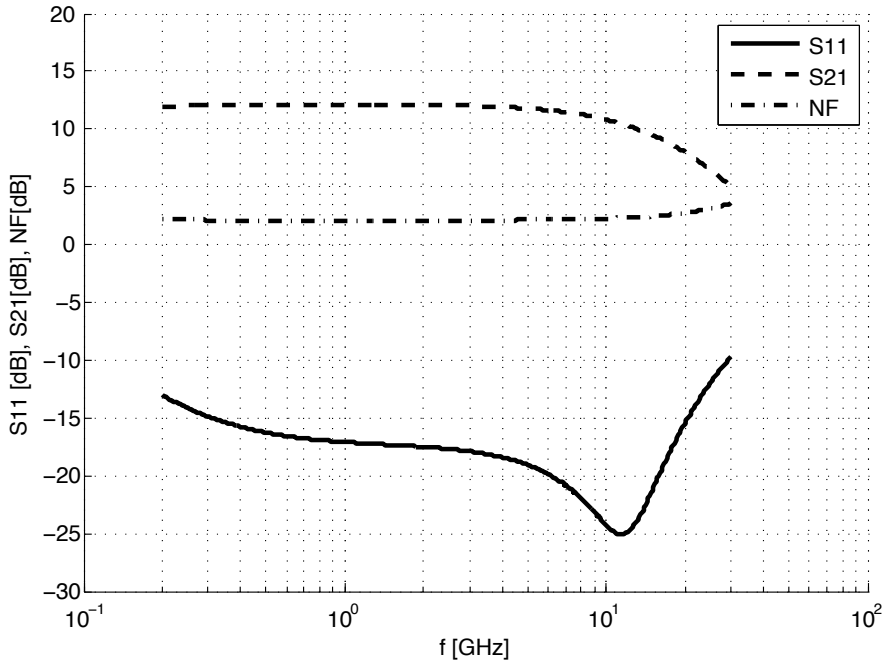

Figure 2.52: TIA - S-parameters and noise figure differential circuit

3.3 On-chip ac coupling implementation

The analyzed system requires to add external coupling capacitances to the chip, with the purpose to remove any dc components from the signal source. However, it may be more convenient for the user if the chip has already internal coupling capacitances. Therefore, with the inclusion of internal coupling capacitances to the chip, the input impedance presents an imaginary part which is not negligible. There would be the possibility to insert a series inductance to resonate the LC input network, but an inductorless solution is the target of this design. This solution increases the NF of the system, but a good compromise can be realized considering the advantage of having on-chip coupling. Thus, setting $C_{ACin} = 3\,\text{pF}$, the optimization of the parameters leads to consider a slight modification of the emitter length for the transistors, have a slight increase of the bias current resulting in $g_m = 170\,\text{mS}$, while it is possible to keep the value $R_C = 100\,\Omega$ and $R_F = 400\,\Omega$. The input impedance, $S11$, $S21$, and the noise figure are illustrated in Fig. 2.53 and Fig. 2.54. The real part of the input impedance is maintained close to $62\,\Omega$ up to 10 GHz, while the imaginary part becomes negligible only around this frequency. The $S11$ is less than $-10\,\text{dB}$ in the band $2.4 \div 22\,\text{GHz}$ and S11=$-16.88\,\text{dB}$ at 10 GHz. The noise figure is increased compared to the previous case, reaching a value of 2.6 dB, while $S21 = 12.25\,\text{dB}$ is obtained. Finally, IIP3=0.37 dBm.

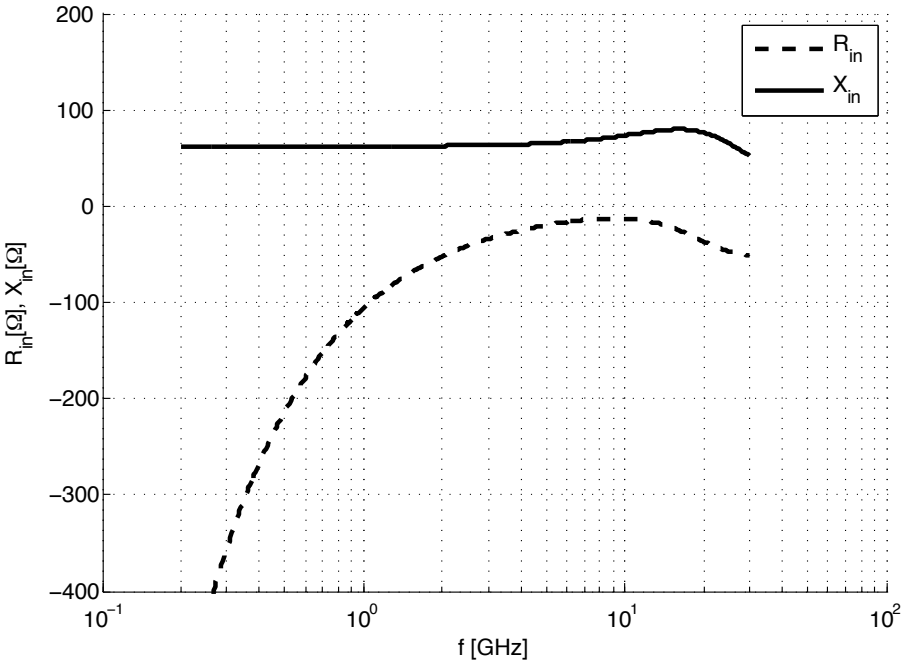

Figure 2.53: TIA - Input impedance with ac coupling

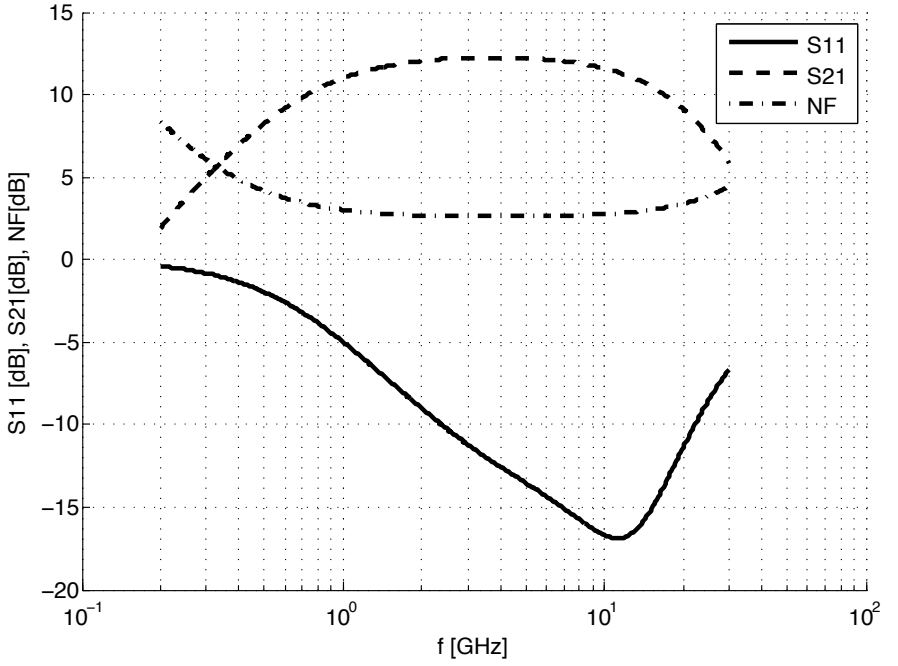

Figure 2.54: TIA - S-parameters and noise figure with ac coupling

3.4 ESD protection

The need to implement an ESD protection system, leads to consider a circuit based on diodes, whose basic version and its operation has been presented in the previous paragraphs. The designed amplifier exibits coupling capacitance, and the ESD protection circuit used is shown in Fig. 2.55, where series diodes limit the parasitic capacitance added on the input nodes. The effects of the on-chip pads are also considered.

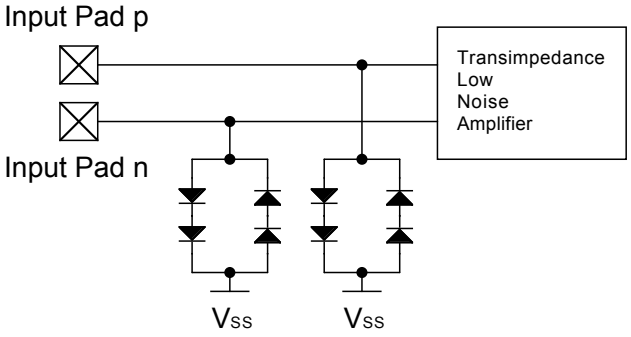

Figure 2.55: TIA - ESD protection

The introduction of the pads, ESD protection system and the ac coupling affects the performance of the amplifier. The input impedance of the system is shown in Fig. 2.56. From this plot, we can observe that the imaginary part of the input impedance cannot be neglected, while the real part is approximately equal to 60 Ω. In addition, from Fig. 2.57, it is possible to observe the bandwidth within which the input matching is guaranteed ($S11 < -10\,\text{dB}$): it becomes about 11 GHz ($2.8 \div 14\,\text{GHz}$), less than the case without the ESD protection and pads, where the same bandwidth was about 20 GHz. The reason is the increased capacitance at the input nodes of the amplifier. However, at 10 GHz, $S11 = -12.3\,\text{dB}$, complying with the initial specification. The noise figure and $S21$ in the bandwidth of interest are 2.7 dB and 12.1 dB, respectively. Since the system is changed compared to the first solution, the magnitude and the phase of the loop gain are plotted in Fig. 2.58 and Fig. 2.59. It is possible to observe a value for $|T|$ less than 2 dB in the band of interest and a phase margin $PM \simeq 140°$. Finally, the designed transimpedance amplifier is characterized by IIP3=0.38 dBm.

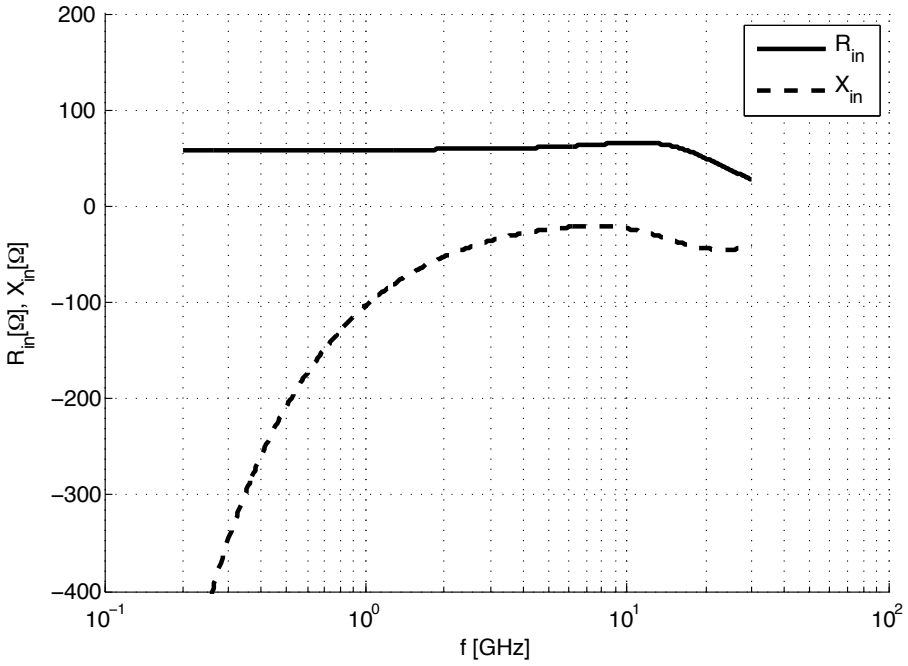

Figure 2.56: TIA - Input impedance with ESD protection

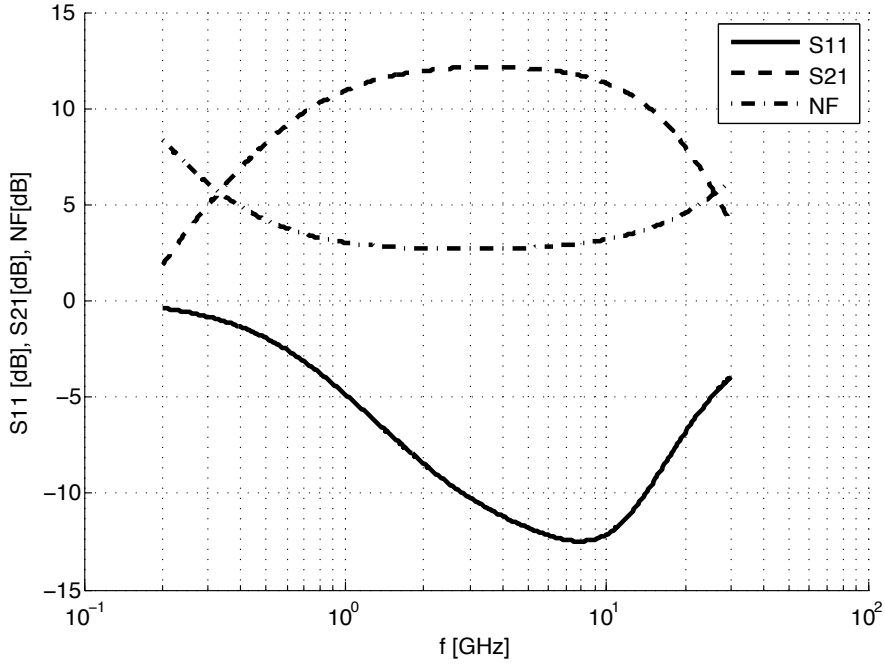

Figure 2.57: TIA - S-parameters and noise figure with ESD protection

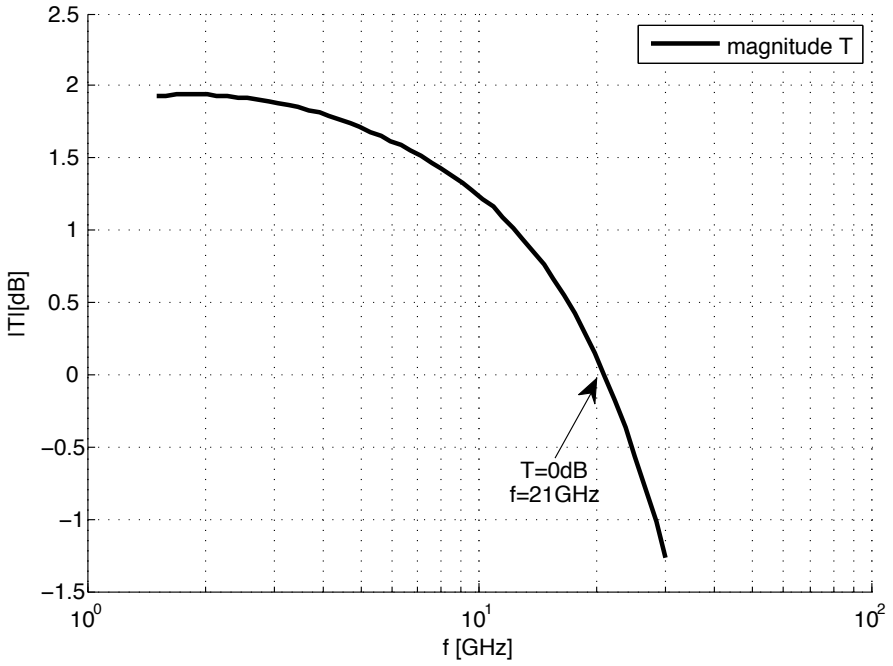

Figure 2.58: TIA - Final loop gain magnitude

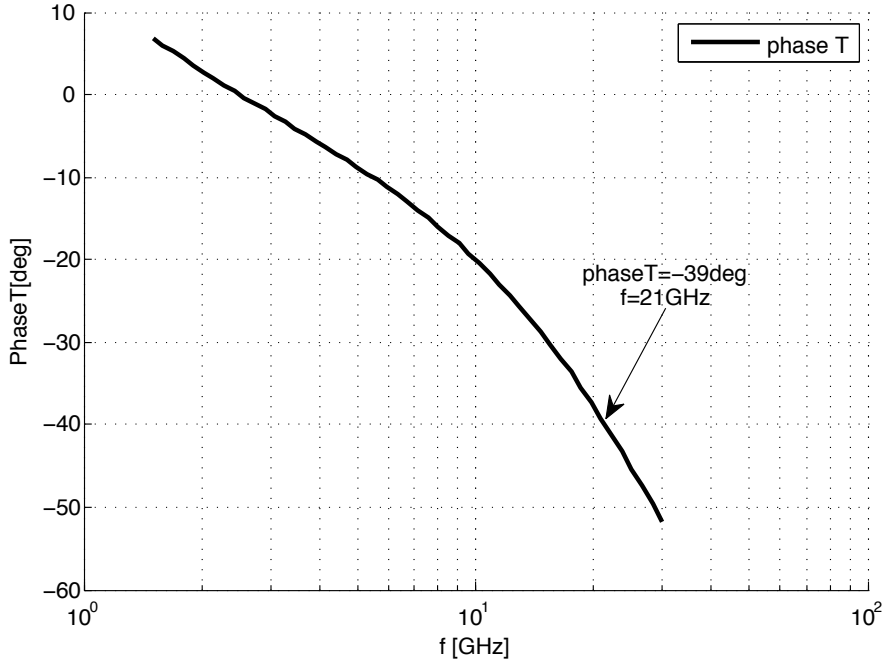

Figure 2.59: TIA - Final loop gain phase

3.5 Design summary and results

In this paragraph, a summary of the design parameters of the discussed wide-band amplifier is presented. In Fig. 2.60, the differential topology of the amplifier with the ESD protection system is illustrated. The biasing is obtained by current mirrors with mirror ratio 1:10, and it is set $I_{BIAS1} = 15\,\text{mA}$ and $I_{BIAS2} = 7.5\,\text{mA}$. Thus, the transimpedance stage and the emitter follower require 50 mW each, form a supply voltage of 3.3 V. As analyzed, the emitter width is fixed for all transistors to the minimum value, while the length of the emitters is setted with the same value for both the signal transistors and the emitter follower transistors. Compared with the analysis presented in the previous sections, in Fig. 2.60 a resistance R_{EF} is inserted to prevent high frequency oscillations. The values of the parameters are summarized in Tab. 2.15.

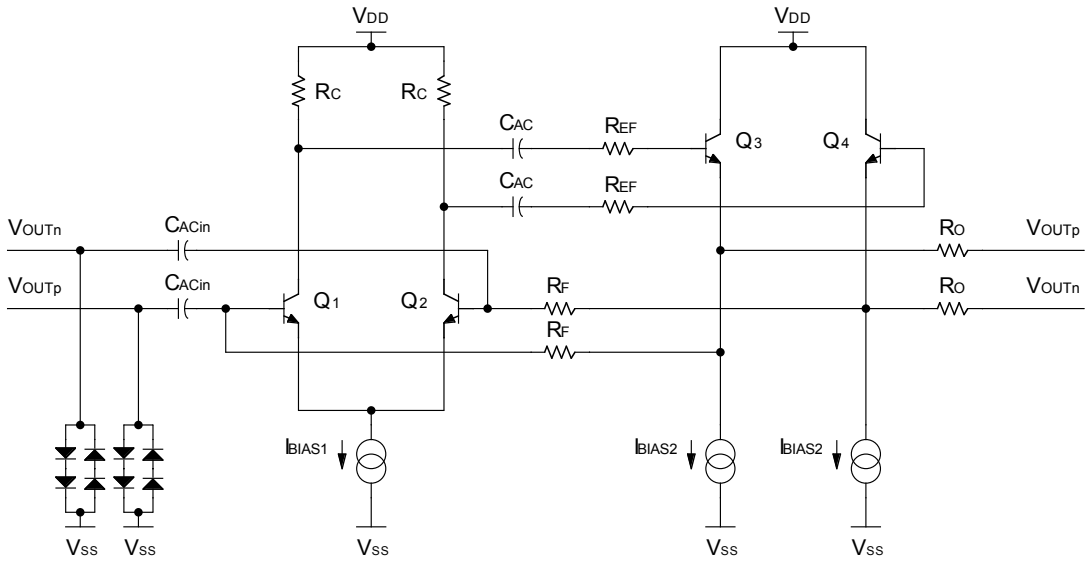

Figure 2.60: TIA - Schematic

$g_{m1,2}$[mS]	$R_C[\Omega]$	$R_F[\Omega]$	C_{ACin}[pF]	C_{AC}[pF]	$R_{EF}[\Omega]$	$R_O[\Omega]$
170	100	400	3	3	50	50

Table 2.15: TIA - Components values

The performance of the designed wide-band transimpedance amplifier is shown in Tab. 2.16.

f [GHz]	**S11 [dB20]**	**S21 [dB20]**	**NF [dB10]**	**IIP3[dBm]**
$2.8 \div 14$	-12.5	12.1	2.7	0.38

Table 2.16: TIA - Design results

The design of a broad-band amplifier leads to an extension of the input matching on a bandwidth of about 11 GHz, but also to a reduction of the gain of the amplifier. Furthermore, comparing the results with the narrow-band low noise amplifiers described, an increase of the noise figure is observed. However, it is an inductorless solution, which determines a reduction of the required area on the chip.
Focusing on the performance of the amplifier in the X-band, considering the range $9 \div 11$ GHz, the main figures of merit are reported in Tab. 2.17. In particular, at 10 GHz, $S11 = -12.1$ dB, $S21 = 11.3$ dB, and $NF = 3.1$ dB.

f [GHz]	**S11 [dB20]**	**S21 [dB20]**	**NF [dB10]**
$9 \div 11$	< -11.8	> 11.1	< 3.3

Table 2.17: TIA - X-band design results

Chapter 3

Layout

1 General rules

In the field of radio frequency design, the layout realization is a fundamental process. In fact, at the operating frequency, the parasitic elements play an important role, and their reduction is the fundamental target in this design phase. Three different kinds of parasitics may be considered at high operating frequency in the circuits analized in chapter 2. They are the resistive, inductive, and coupling capacitance contributions of the interconnections at the layout level. Then, a careful layout should be realized occupying the least possible area, making the connections between devices simple, and adopting a symmetrical solution.
In the low noise ampifiers with inductive degeneration, the realization of the inductors is the most important layout step, and it has already discussed in the section 2.6. Moreover, the cascode stage has to be close to the resonant output network to minimize the resistive component of the connection which may degrade the quality factor of the tank. In addition, in the emitter follower circuit, the collectors of the signal transistors have to be close to each other, minimizing the added inductive contribution and avoiding possible oscillations of the structure. Similar consideration apply for the transimpedance amplifier designed. In particular, in this structure the connection from the signal transistors to the load resistances determines an inductive contribution, that results in a peaking effect. Once realized the layout, and extracted the parasitics from the circuit with the simulator, it is possible to insert all the parasitic in the schematic and to proceed with the resimulation of the system performance. A new evaluation of the layout may be necessary if the parasitics affect too much the specification. Finally, it is strongly recommended to bring the V_{SS} metal layer evenly across the chip.

2 Layout views

2.1 Narrow-band LNA1

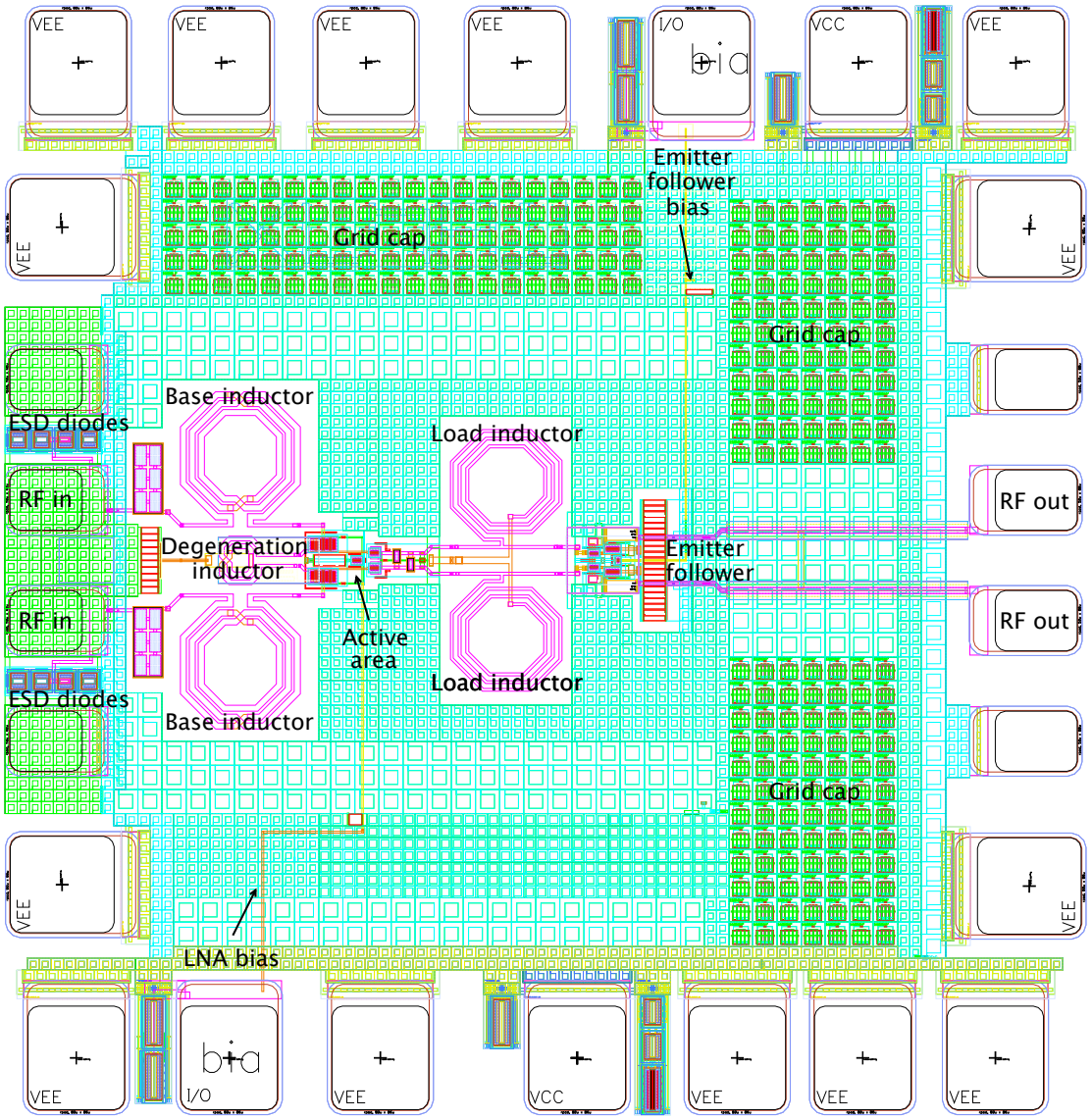

Figure 3.1: LNA1 - Layout view (930 µm × 930 µm)

Fig. 3.1 illustrates the layout of the first topology of narrow-band low noise amplifier discussed. A top level view is considered, including also the on-chip pads and the grid capacitances connected between the metal layer 1 (V_{DD}) and the metal layer 2 (V_{SS}). In addition, a signal for the activation of the emitter follower and one for the low noise amplifier stage are also implemented. Finally, a transmission line is adopted to connect the emitter follower to the output pads.

2.2 Narrow-band LNA2

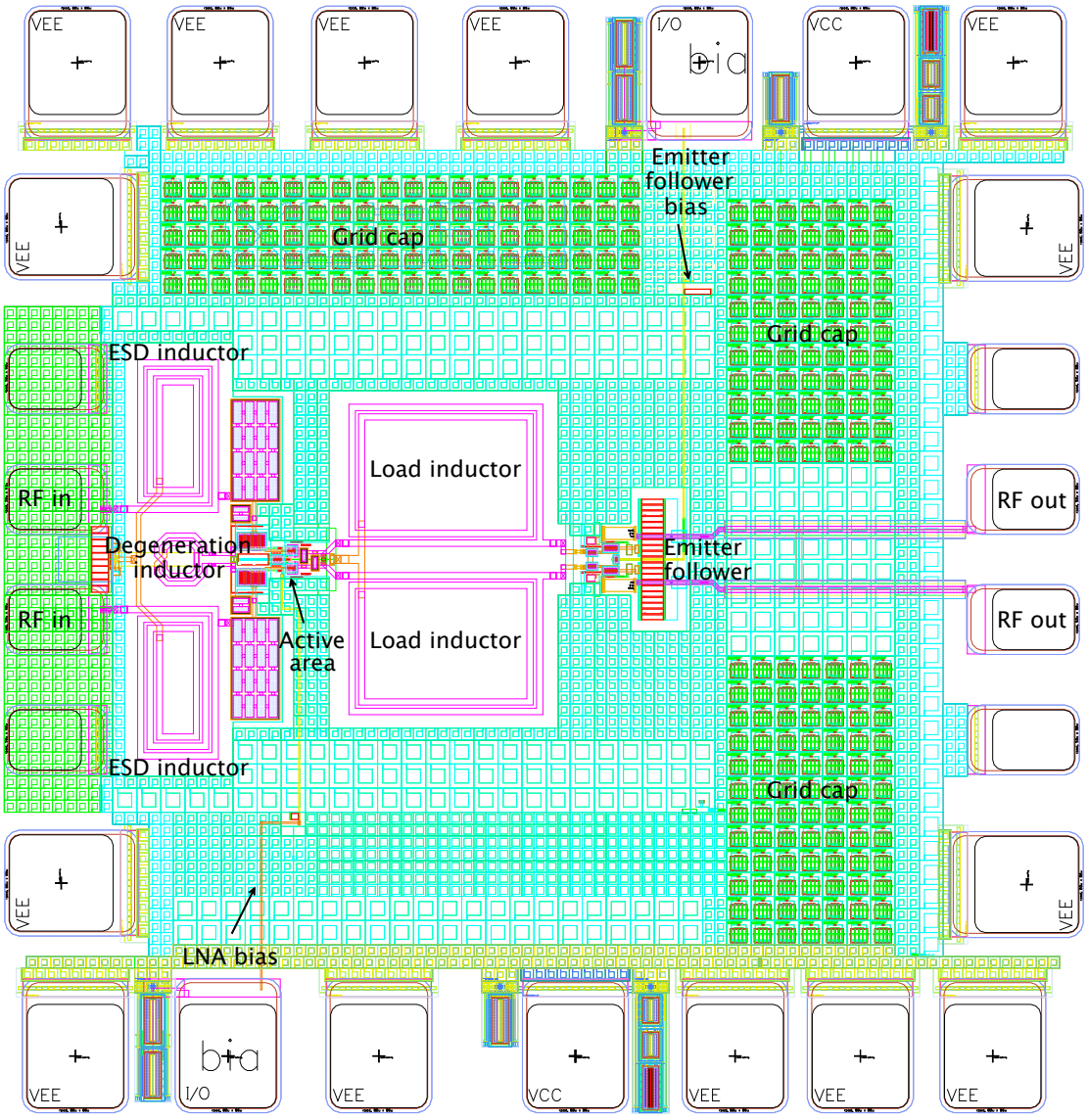

Figure 3.2: LNA2 - Layout view (930 µm × 930 µm)

The layout of the second topology of the inductive degeneration low noise amplifier designed is shown in Fig. 3.2. The on-chip pads, grid capacitances, and the bias signal for the amplifier stage and for the emitter follower are presented, as for the previous layout view. Compared to Fig. 3.1, in this case the ESD diodes at the input of the structure are not implemented. Also in this case, a transmission line connects the emitter follower to the output pads.

2.3 Wide-band LNA

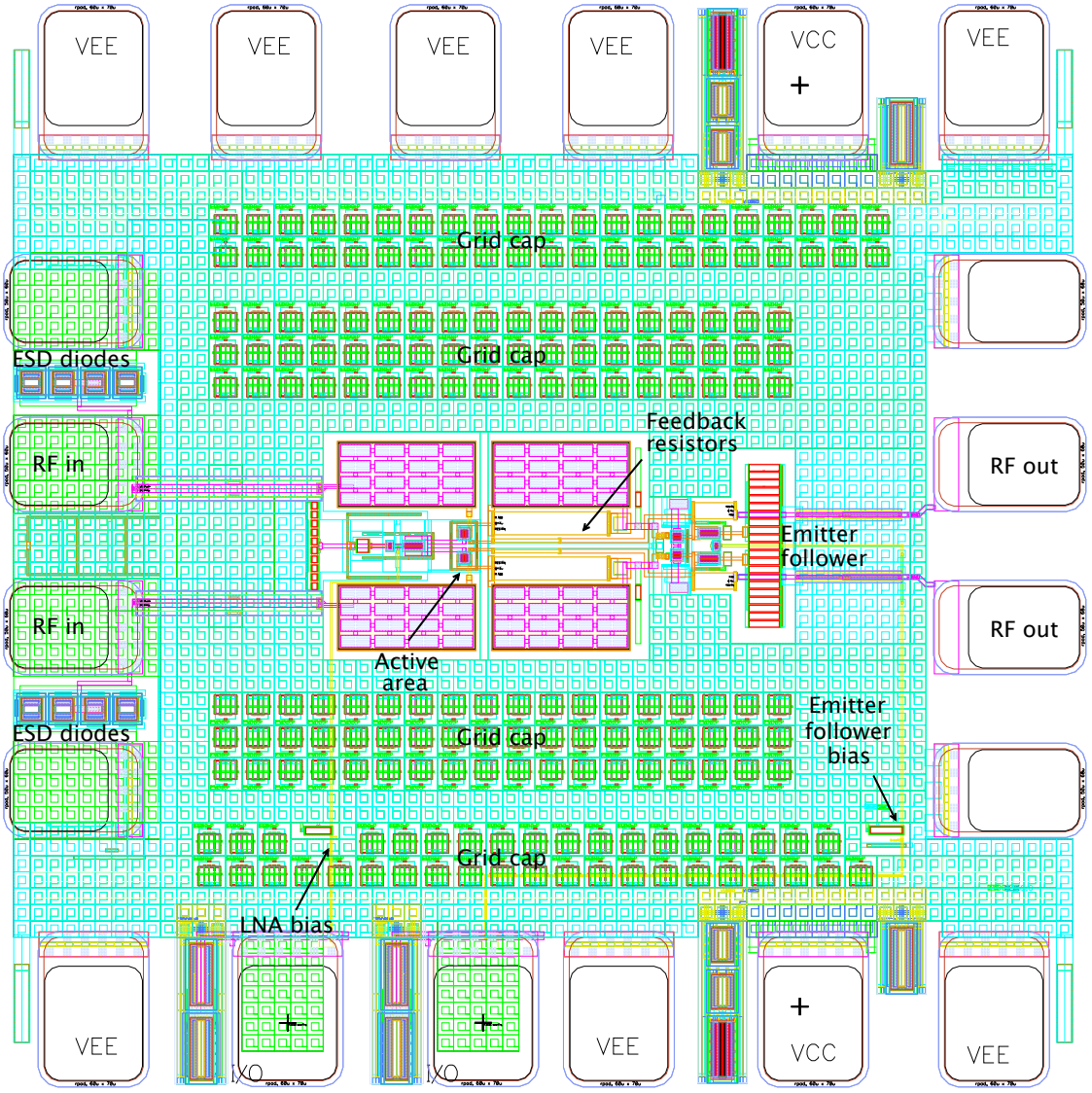

Figure 3.3: TIA - Layout view (672 µm × 672 µm)

Finally, the top level layout view of the designed transimpedance low noise amplifier is presented in Fig. 3.3. Compared to the layout of the two inductive degeneration amplifiers, it is a more compact solution, where the ac capacitances and the buffer coupling capacitances are the components which require the largest amount of area. Also in this case, the bias signal for the amplifier stage and for the emitter follower, the on-chip pads, the ESD diodes, and grid capacitances are illustrated. Two transmission lines are used to connect the on-chip pads to the input and output of the system.

Chapter 4

Results

In this chapter, a list of the simulation results obtained for the three topologies of designed low noise amplifier is reported. The goal is to illustrate an overview that summarizes the characteristics of the considered circuits, analyzing them one at a time. The presented results refer to simulations; however, they take into account the post-layout parasitic extraction.

The frequency trend of the S-parameters, the value of the S-parameters at the operating frequency 10 GHz, the noise figure, the value of the noise figure at 10 GHz, and the IIP3 are plotted considering a temperature range $25 \div 85\,^{\circ}\mathrm{C}$ and a variation $\pm 5\%$ of the supply voltage, assuming a possible variation of V_{DD} in the range $3.135 \div 3.465\,\mathrm{V}$.

Monte Carlo simulations are also analyzed, and the effects of mismatch and process variation of the S-parameters and the noise figure at the operating frequency and the IIP3 are plotted.

In addition, the stability of the amplifiers is verified plotting the parameters K_f and b_{1f}, as already discussed in the section related to the analysis of the stability through these two coefficients.

Finally, for the wide-band low noise amplifier, the variation of the main figures of merit is considered compared to the variation of the feedback resistor value, being able to assess the effect of this resistance on the characteristics of the feedback system.

1 Narrow-band LNA1

1.1 Temperature and supply voltage sensibility

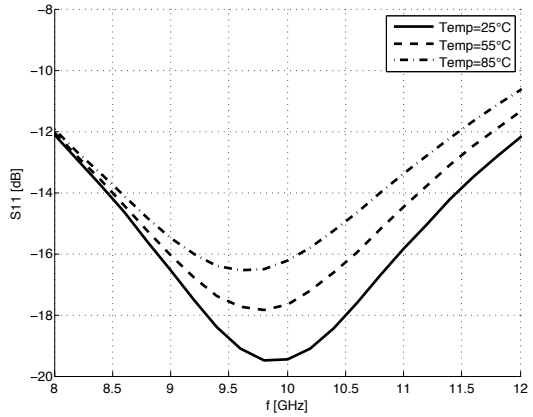

Figure 4.1: LNA1 - S11/Temp

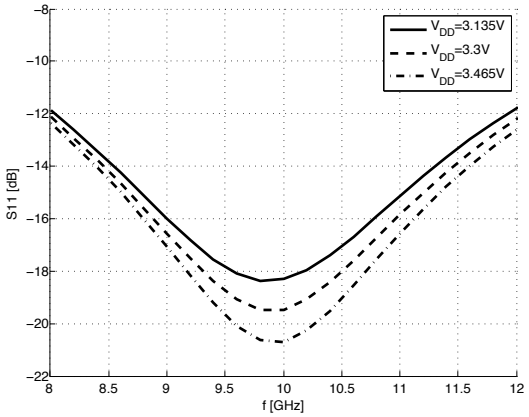

Figure 4.2: LNA1 - S11/V_{DD}

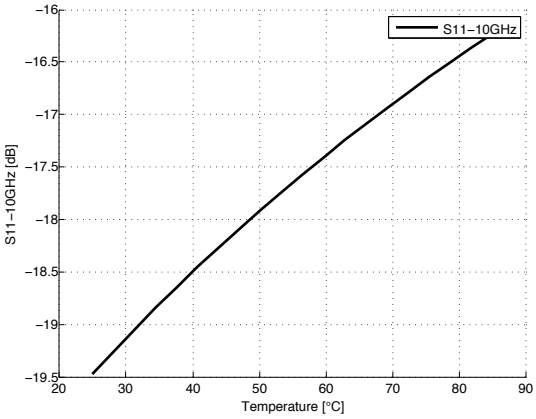

Figure 4.3: LNA1 - $S11_{10GHz}$/Temp

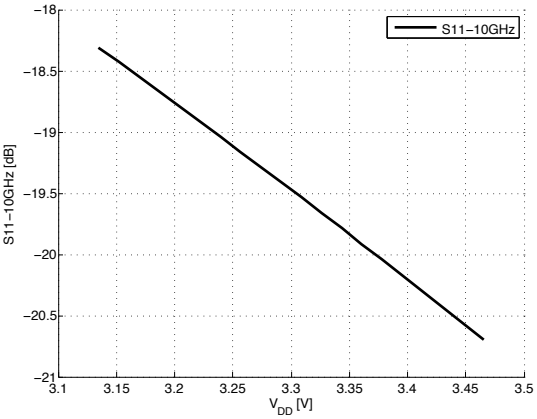

Figure 4.4: LNA1 - $S11_{10GHz}$/V_{DD}

From Fig. 4.1 and Fig. 4.2, it is possible to observe that a temperature increase degrades the minimum value of $S11$, while the supply voltage increase determines its improvement. For both the cases, a $S11$ variation of about 3 dB is determined. Finally, Fig. 4.3 and Fig. 4.4 show the trend of the value of $S11$ at 10 GHz considering a temperature and supply voltage variation, respectively.

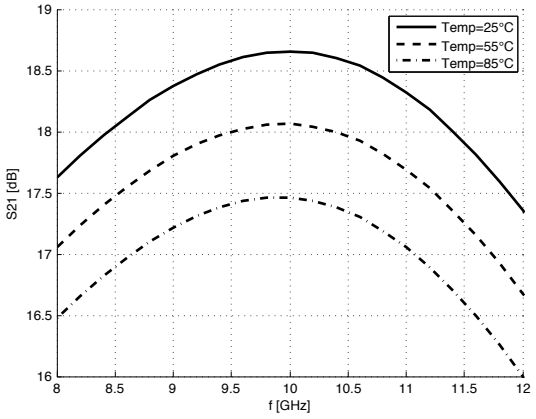

Figure 4.5: LNA1 - S21/Temp

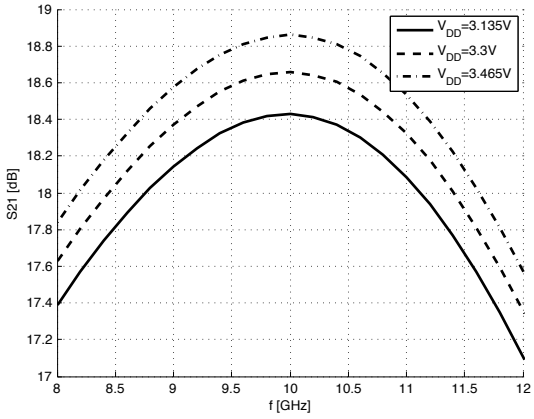

Figure 4.6: LNA1 - S21/V_{DD}

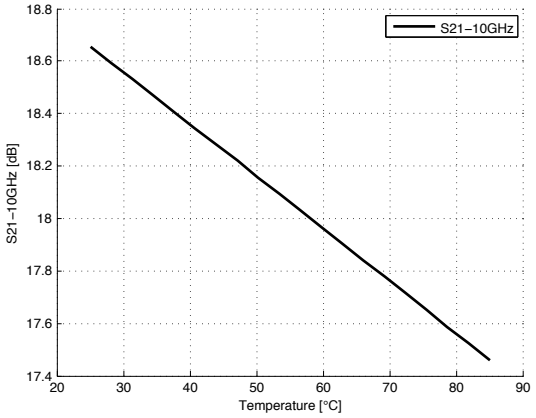

Figure 4.7: LNA1 - $S21_{10GHz}$/Temp

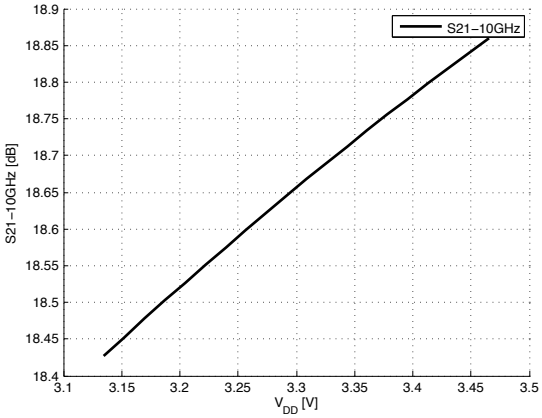

Figure 4.8: LNA1 - $S21_{10GHz}$/V_{DD}

Fig. 4.5 and Fig. 4.6 show the parameter $S21$ as a function of the temperature and supply voltage variations, respectively. It is possible to observe that a temperature and supply voltage increase determines different trends of this parameter. In particular, the $S21$ value at the operating frequency 10 GHz is shown in Fig. 4.7 and Fig. 4.8. These $S21$ variations are approximately 1 dB considering the temperature variations and 0.5 dB for the V_{DD} variations.

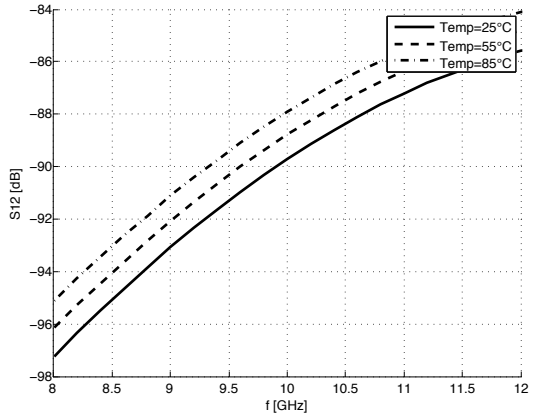

Figure 4.9: LNA1 - S12/Temp

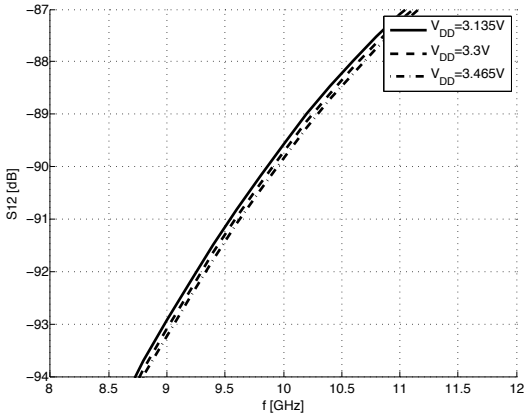

Figure 4.10: LNA1 - S12/V_{DD}

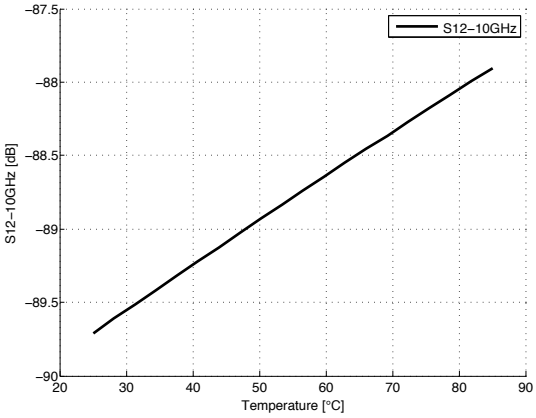

Figure 4.11: LNA1 - $S12_{10GHz}$/Temp

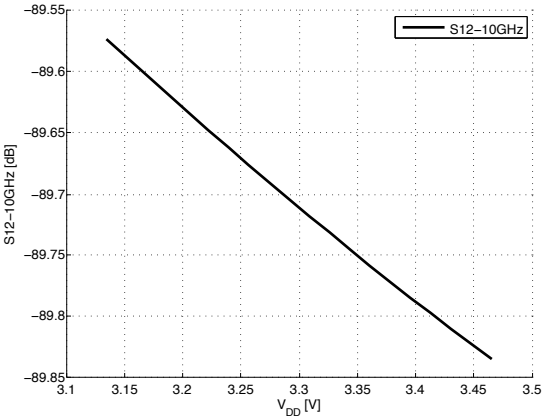

Figure 4.12: LNA1 - $S12_{10GHz}$/V_{DD}

In Fig. 4.9 and Fig. 4.10, the reader can observe the frequency trend of the inverse transmission coefficient $S12$, considering temperature and supply voltage variations. It is obtained a value $S12 \simeq -90\,\text{dB}$ and the reported variations are not so relevant. The trends of the value $S12$ at the operating frequency 10 GHz are shown in Fig. 4.11 and Fig. 4.12, for temperature and supply voltage variations.

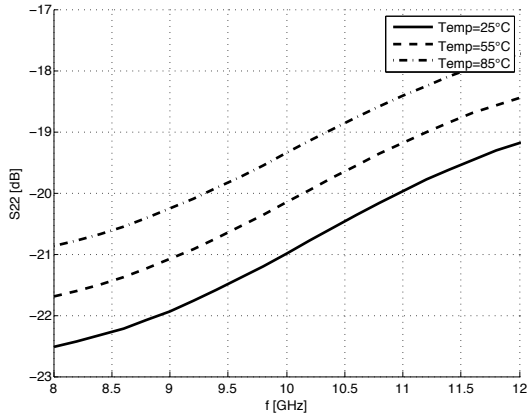

Figure 4.13: LNA1 - S22/Temp

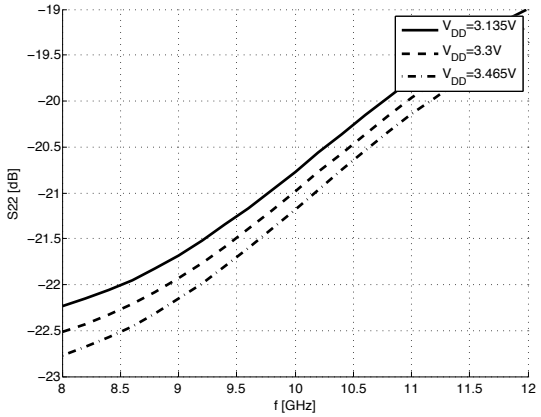

Figure 4.14: LNA1 - S22/V_{DD}

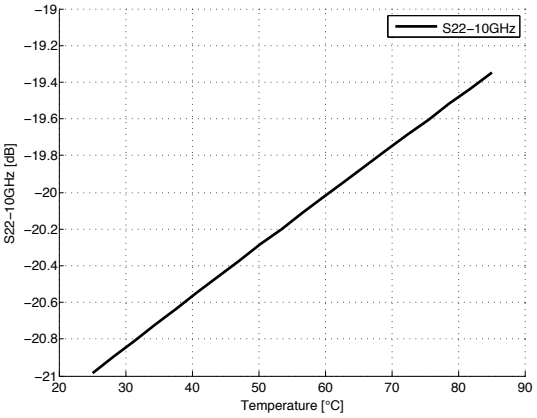

Figure 4.15: LNA1 - $S22_{10GHz}$/Temp

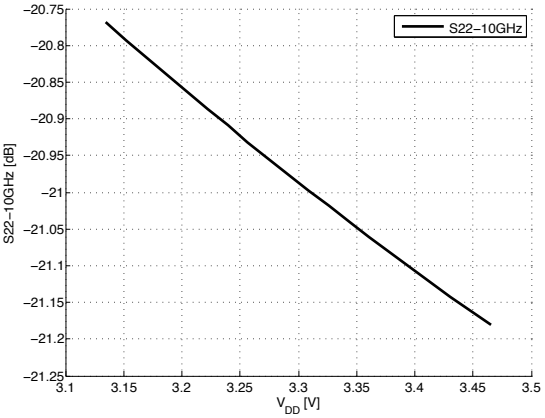

Figure 4.16: LNA1 - $S22_{10GHz}$/V_{DD}

From the simulation, $S22 \simeq -21\,\mathrm{dB}$ and the results of temperature and supply voltage variations are plotted in Fig. 4.13 and Fig. 4.14. The $S22$ value at the operating frequency 10 GHz is shown in Fig. 4.15 and Fig. 4.16. It is possible to note that the considered parameter variations have different effects on the reflection coefficient $S22$ at the output.

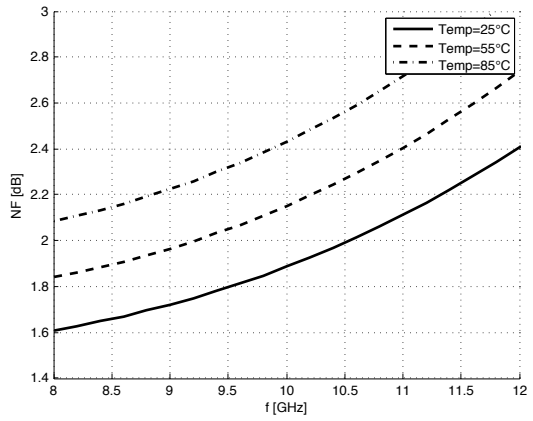

Figure 4.17: LNA1 - NF/Temp

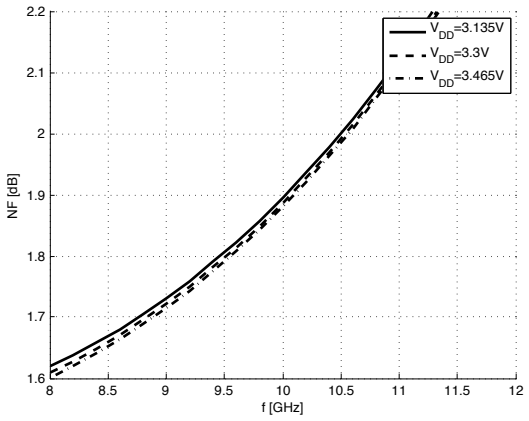

Figure 4.18: LNA1 - NF/V_{DD}

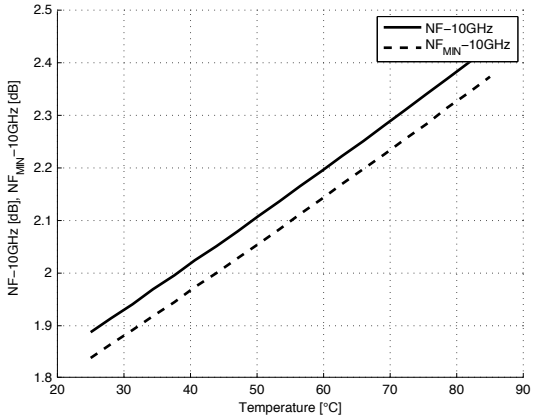

Figure 4.19: LNA1 - NF_{10GHz}/Temp

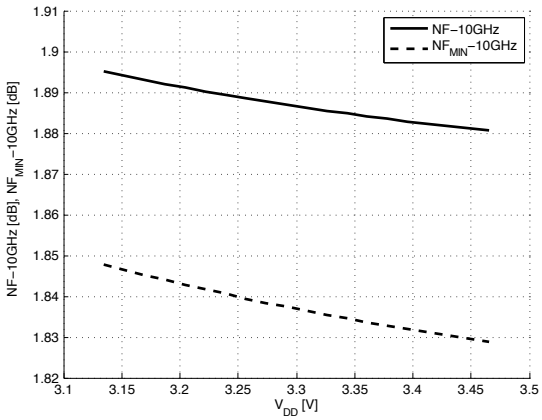

Figure 4.20: LNA1 - NF_{10GHz}/V_{DD}

Fig. 4.17 and Fig. 4.18 illustrate the trend of the noise figure of the circuit, considering temperature and supply voltage variations. The temperature increase determines a higher value of noise figure NF, while if V_{DD} increases a slightly lower value of noise figure is obtained. In addition, Fig. 4.19 and Fig. 4.20 show the NF_{MIN} and NF values at the operating frequency 10 GHz. It is clear that the temperature plays a dominant role with respect to the noise performance of the circuit.

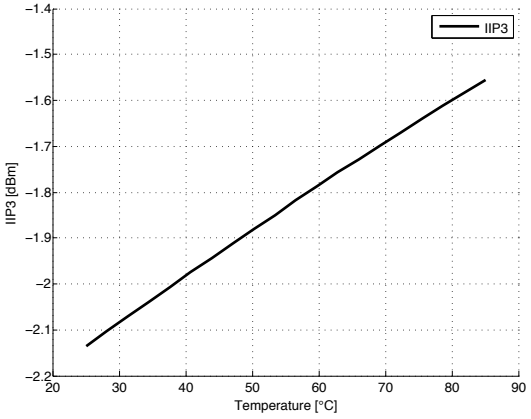

Figure 4.21: LNA1 - IIP3/Temp

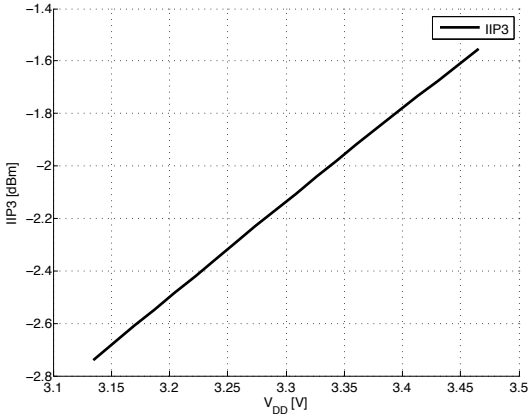

Figure 4.22: LNA1 - IIP3/V_{DD}

Finally, from Fig. 4.21 and Fig. 4.22, it is possible to observe the increase of IIP3 with temperature and supply voltage increase.

1.2 Monte Carlo analysis

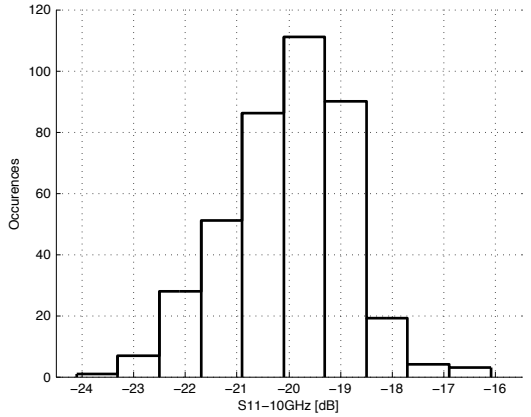

Figure 4.23: LNA1 - S11 MC simulation

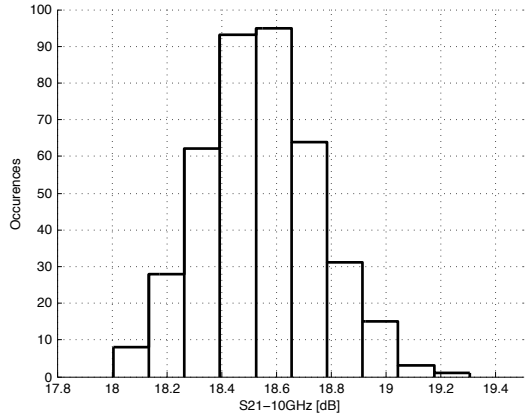

Figure 4.24: LNA1 - S21 MC simulation

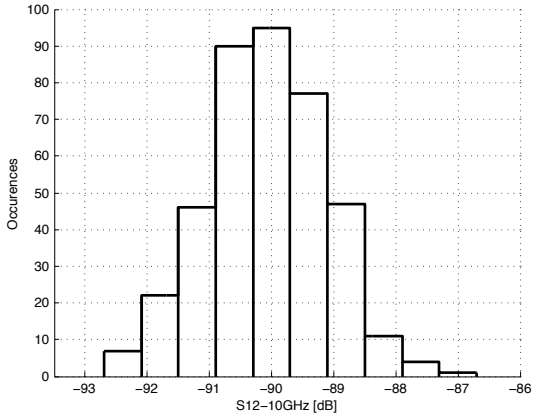

Figure 4.25: LNA1 - S12 MC simulation

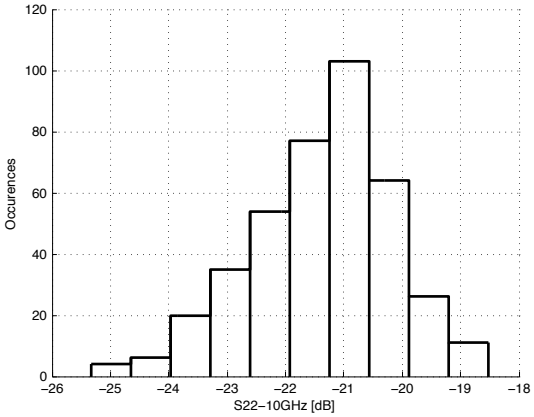

Figure 4.26: LNA1 - S22 MC simulation

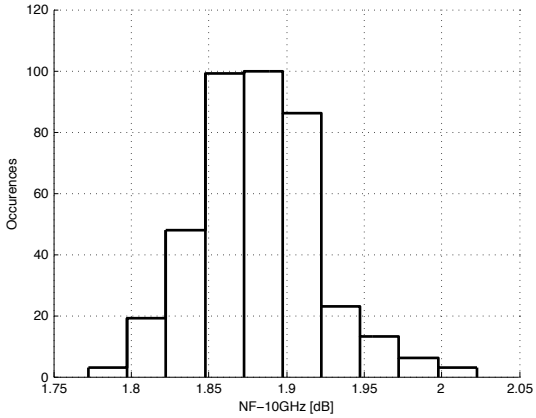

Figure 4.27: LNA1 - NF MC simulation

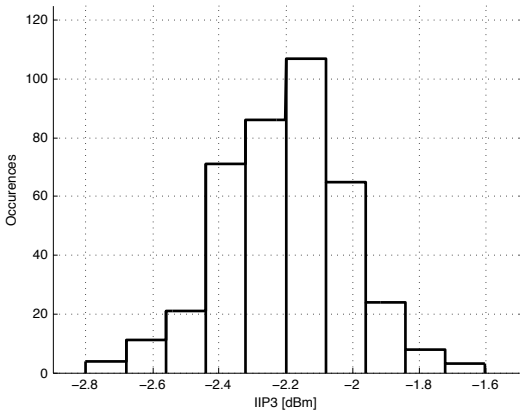

Figure 4.28: LNA1 - IIP3 MC simulation

Fig. 4.23-4.28 illustrate the results of the Monte Carlo analysis for the S-parameters (Fig. 4.23-4.26), noise figure (Fig. 4.27), and the parameter IIP3 (Fig. 4.28) at 10 GHz. A random sampling method with 400 points is considered for this kind of analysis.

1.3 Stability

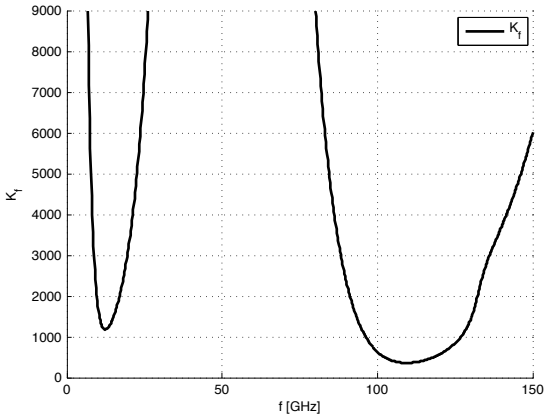

Figure 4.29: LNA1 - K_f factor

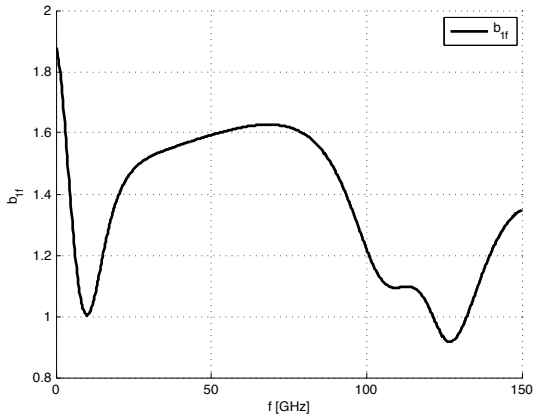

Figure 4.30: LNA1 - b_{1f} factor

Finally, for the first topology of narrow-band low noise amplifier designed, Fig. 4.29 and Fig. 4.30 illustrate the trends of the parameters K_f and b_{1f} in the frequency range $0 \div 150$ GHz. From these plots, it is possible to observe that the K_f parameter is always greater than 1 and b_{1f} is greater than 0, proving the stability of the discussed low noise amplifier.

2 Narrow-band LNA2

2.1 Temperature and supply voltage sensibility

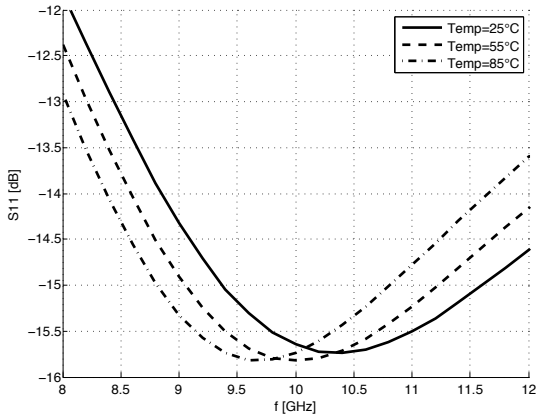

Figure 4.31: LNA2 - S11/Temp

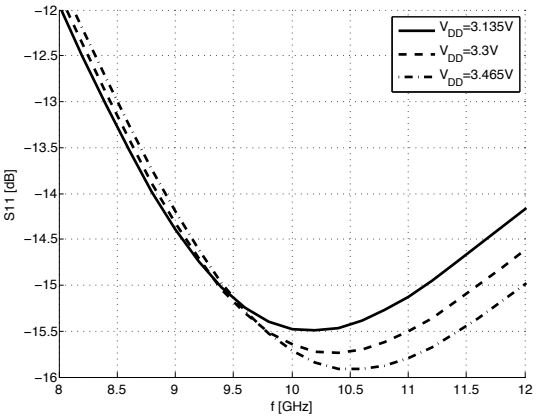

Figure 4.32: LNA2 - S11/V_{DD}

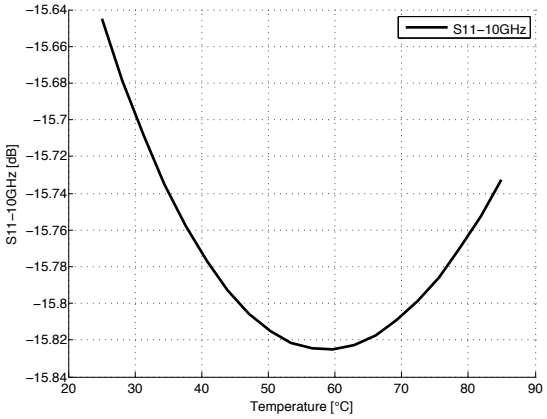

Figure 4.33: LNA2 - $S11_{10GHz}$/Temp

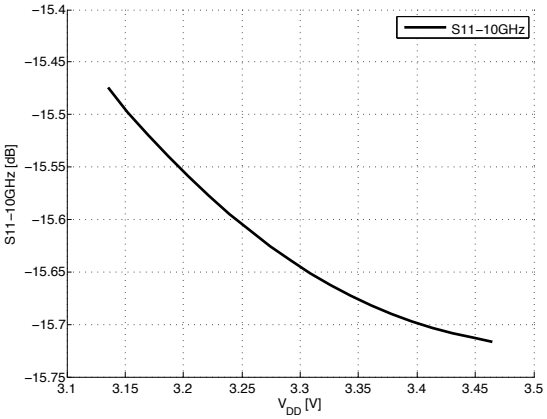

Figure 4.34: LNA2 - $S11_{10GHz}$/V_{DD}

Fig. 4.31 and Fig. 4.32 show the trend of $S11$ considering temperature and supply voltage variations. Compared to the case of the first designed low noise amplifier, it is possible to observe that a temperature increase moves the minimum of $S11$ at higher frequencies, while the V_{DD} increase determines its improvement and a slight increase of the frequency of the dip. However, these variations are not so relevant. Fig. 4.33 and Fig. 4.34 illustrate the value of $S11$ at 10 GHz considering a temperature and supply voltage variation, respectively. At the operating frequency, it is interesting to observe a minimum of $S11$ at the temperature of 57 °C.

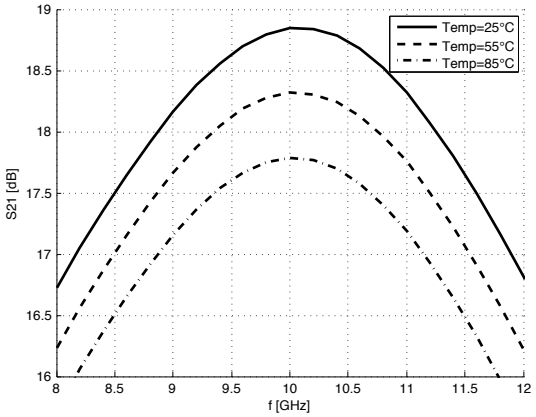

Figure 4.35: LNA2 - S21/Temp

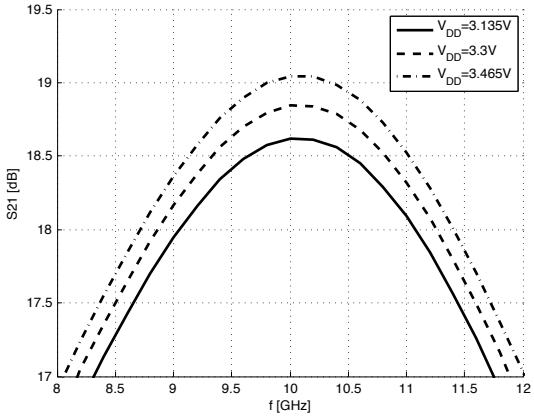

Figure 4.36: LNA2 - S21/V_{DD}

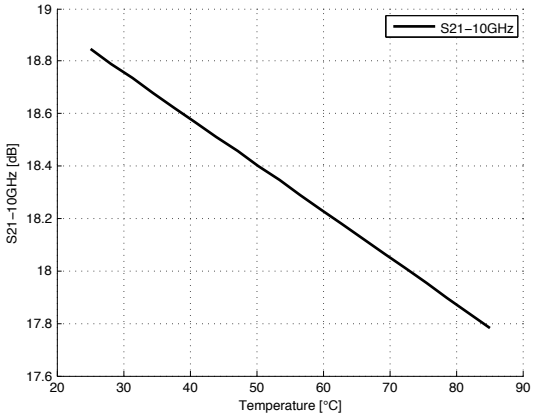

Figure 4.37: LNA2 - $S21_{10GHz}$/Temp

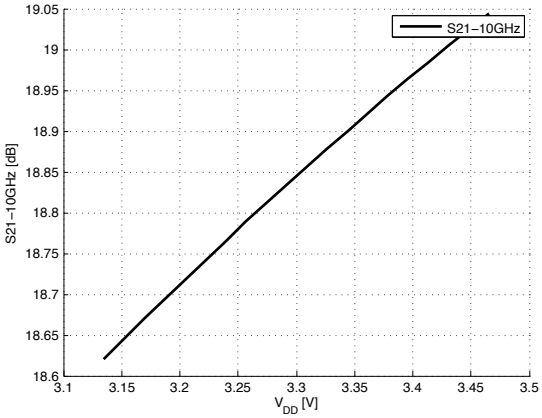

Figure 4.38: LNA2 - $S21_{10GHz}$/V_{DD}

As analyzed for the first proposed low noise amplifier, Fig. 4.35 and Fig. 4.36 illustrate the frequency trend of the $S21$ parameter considering the temperature and supply voltage variation. Also in this case, a temperature increase determines lower values of $S21$, while a supply voltage increase involves greater $S21$ values. Fig. 4.37 and Fig. 4.38 show the $S21$ parmeter at 10 GHz considering the temperature and supply voltage variations.

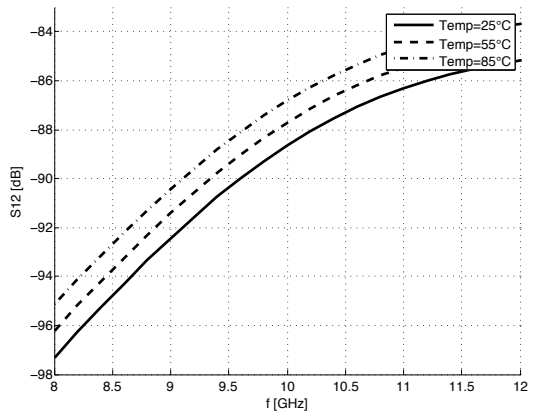

Figure 4.39: LNA2 - S12/Temp

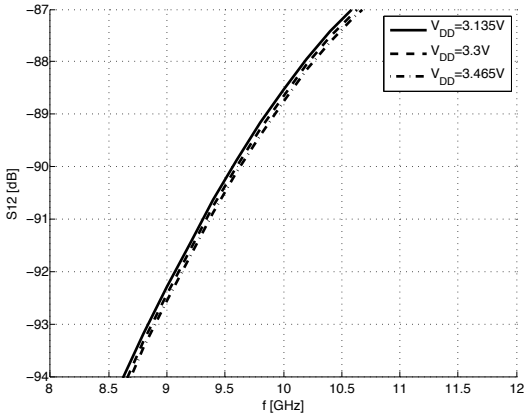

Figure 4.40: LNA2 - S12/V_{DD}

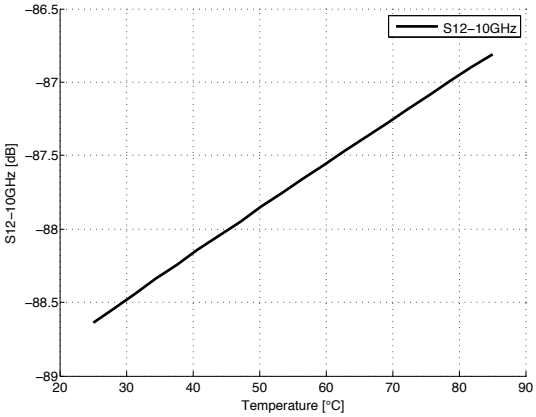

Figure 4.41: LNA2 - $S12_{10GHz}$/Temp

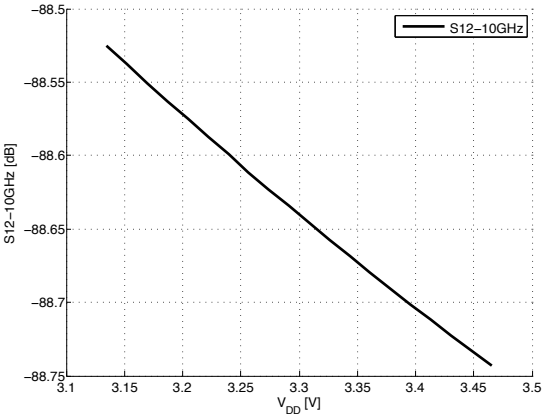

Figure 4.42: LNA2 - $S12_{10GHz}$/V_{DD}

Fig. 4.39 and Fig. 4.40 show the inverse transmission coefficient $S12$ considering temperature and supply voltage variations. The values obtained are very similar to the results in the previous case, with a $S12$ value between $-95\,\mathrm{dB}$ and $-85\,\mathrm{dB}$. The variations of the value of $S12$ at $10\,\mathrm{GHz}$ are shown in Fig. 4.41 and Fig. 4.42.

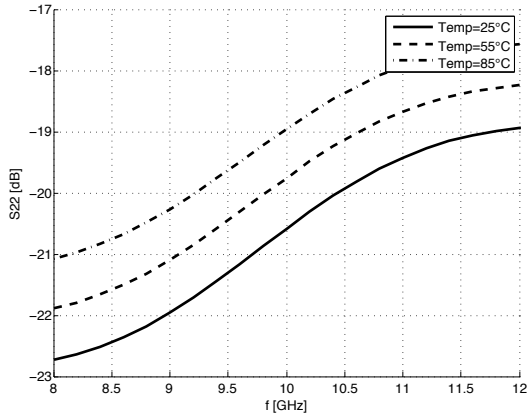

Figure 4.43: LNA2 - S22/Temp

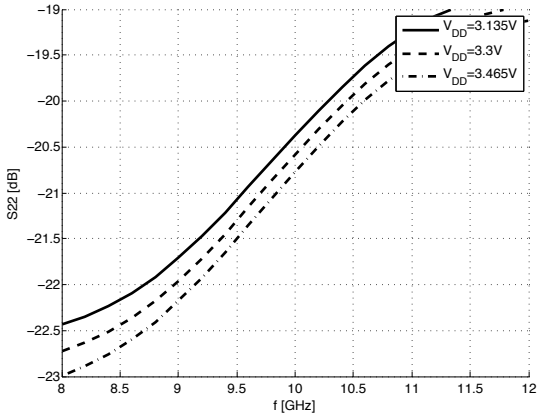

Figure 4.44: LNA2 - S22/V_{DD}

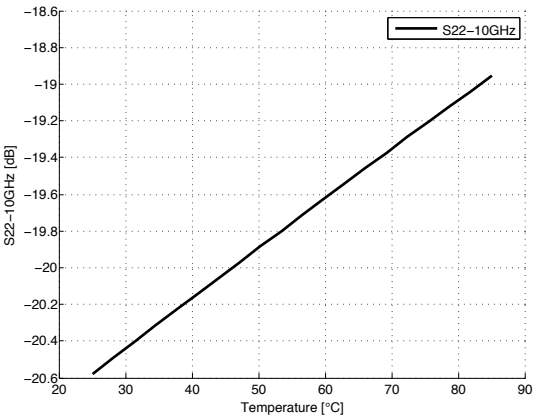

Figure 4.45: LNA2 - $S22_{10GHz}$/Temp

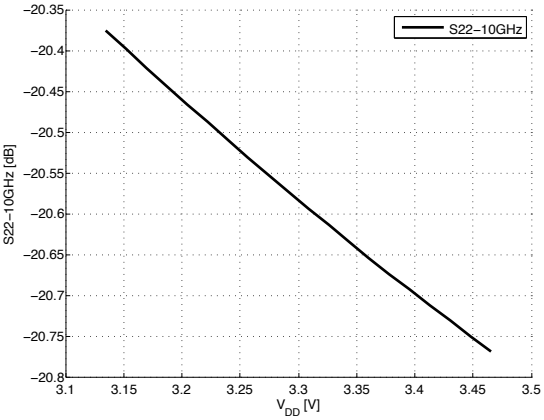

Figure 4.46: LNA2 - $S22_{10GHz}$/V_{DD}

The results obtained for the $S22$ parameter are plotted in Fig. 4.43 and Fig. 4.44. The $S22$ value at the 10 GHz operating frequency is shown in Fig. 4.45 and Fig. 4.46. The results show a value between −22 dB and −18 dB considering temperature and supply voltage variations.

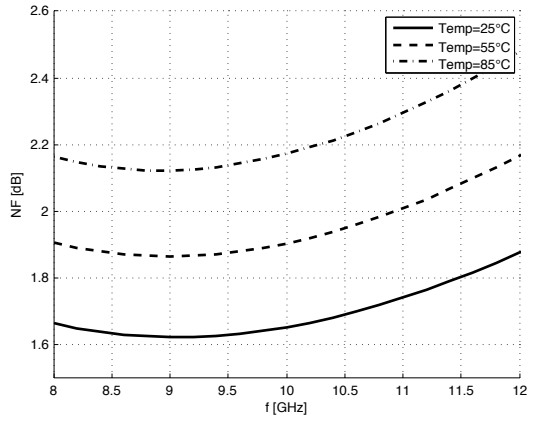

Figure 4.47: LNA2 - NF/Temp

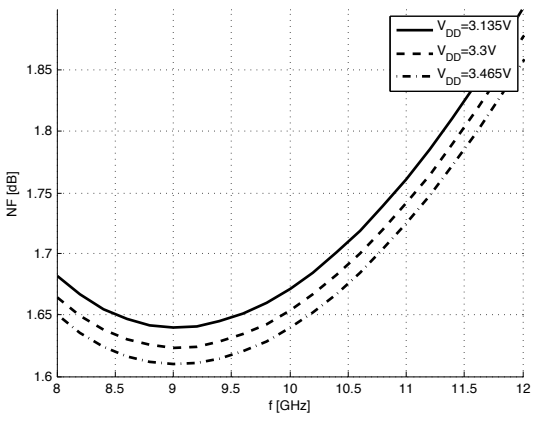

Figure 4.48: LNA2 - NF/V_{DD}

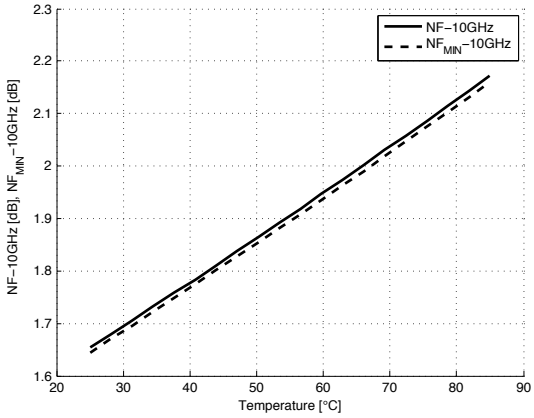

Figure 4.49: LNA2 - NF_{10GHz}/Temp

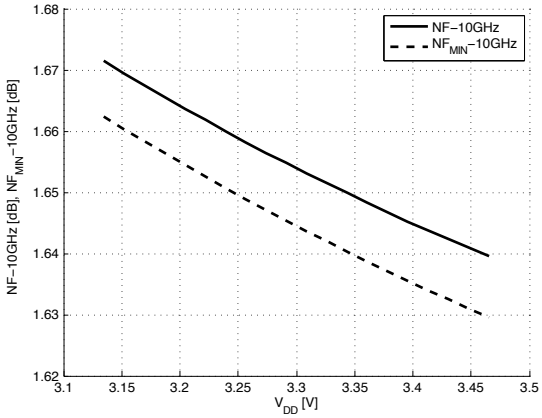

Figure 4.50: LNA2 - NF_{10GHz}/V_{DD}

The trend of the noise figure of the low noise amplifier is illustrated in Fig. 4.47 and Fig. 4.48, considering temperature and supply voltage variations. While the temperature increase determines an higher value of NF, if V_{DD} increases a slightly lower value of NF is obtained. The temperature is the dominant factor as in the previous case. Finally, Fig. 4.49 and Fig. 4.50 show the NF_{MIN} and NF values at the operating frequency.

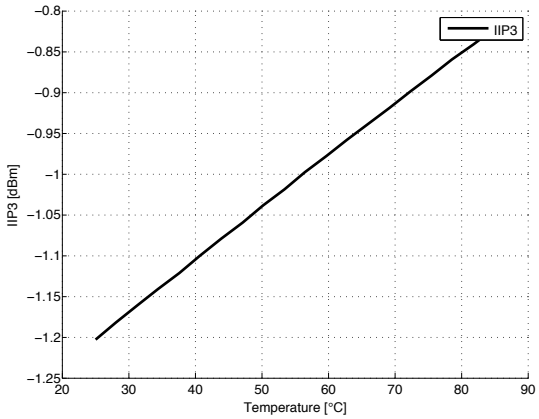

Figure 4.51: LNA2 - IIP3/Temp

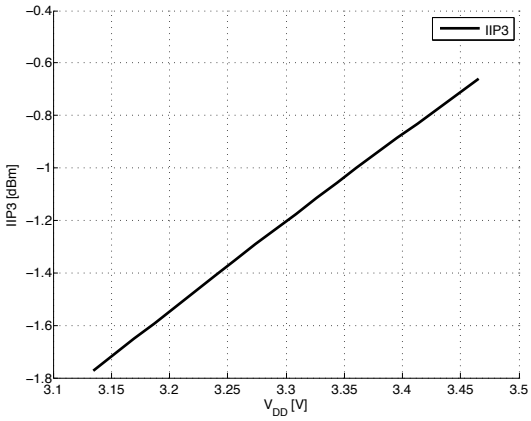

Figure 4.52: LNA2 - IIP3/V_{DD}

Fig. 4.51 and Fig. 4.52 illustrate the growth of the IIP3 parameter with the temperature and supply voltage increase.

2.2 Monte Carlo simulation

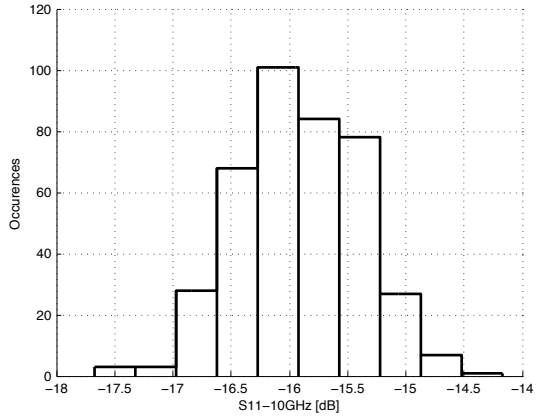

Figure 4.53: LNA2 - S11 MC simulation

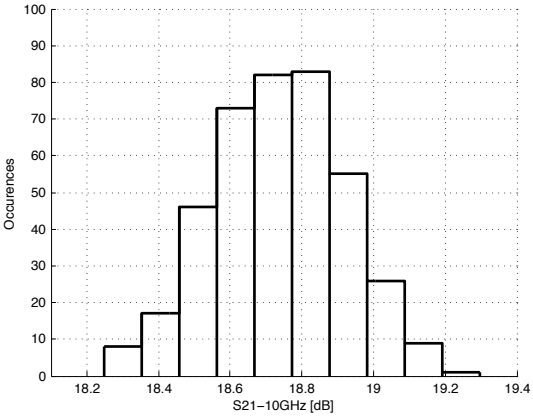

Figure 4.54: LNA2 - S21 MC simulation

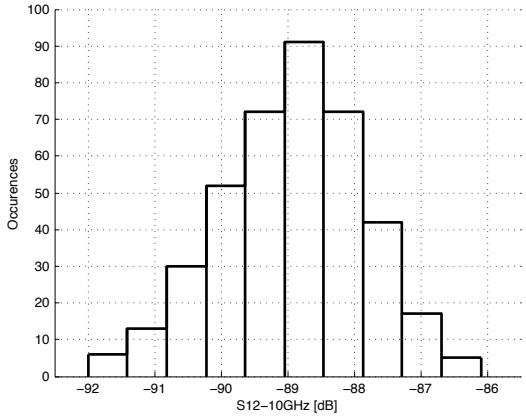

Figure 4.55: LNA2 - S12 MC simulation

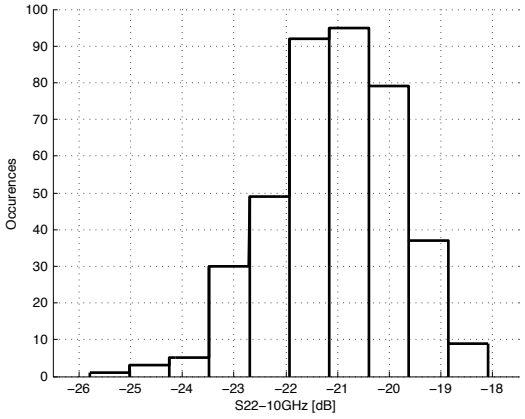

Figure 4.56: LNA2 - S22 MC simulation

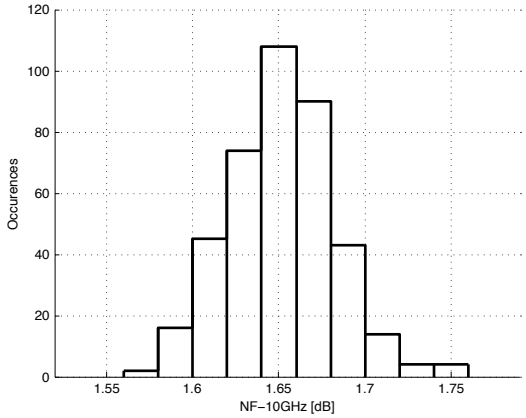

Figure 4.57: LNA2 - NF MC simulation

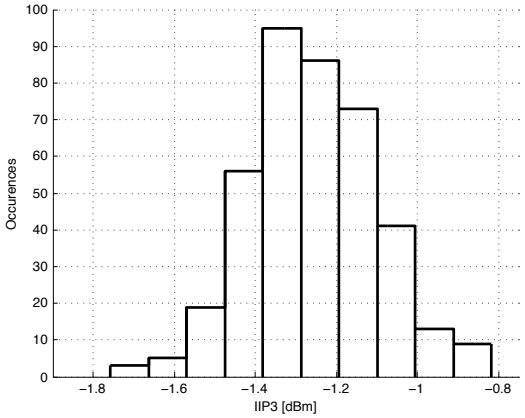

Figure 4.58: LNA2 - IIP3 MC simulation

Fig. 4.53, Fig. 4.54, Fig. 4.55, and Fig. 4.56 show the Monte Carlo analysis results for the S-parameters at 10 GHz, while the noise figure and IIP3 results of the same analysis are illustrated in Fig. 4.57 and Fig. 4.58, respectively. As for the first proposed solution of low noise amplifier, a random sampling method with 400 points is considered.

2.3 Stability

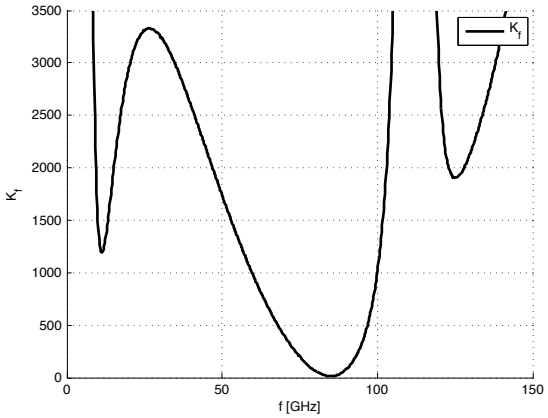

Figure 4.59: LNA2 - K_f factor

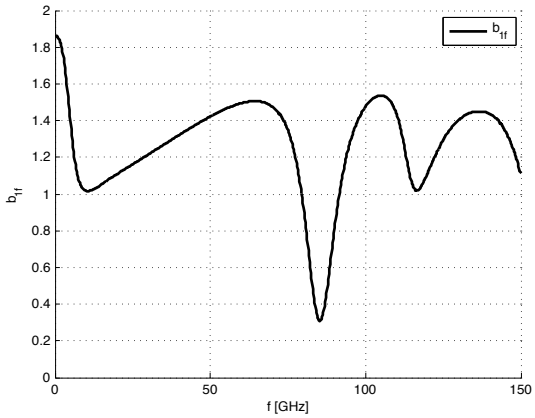

Figure 4.60: LNA2 - b_{1f} factor

The trends of the parameters K_f and b_{1f} are illustrated in Fig. 4.59 and Fig. 4.60, considering the frequency range $0 \div 150\,\text{GHz}$. The reader can observe how the K_f parameter is always greater than 1 and b_{1f} is greater than 0, proving the stability of this second topology of low noise amplifier proposed.

3 Wide-band LNA

3.1 Temperature and supply voltage sensibility

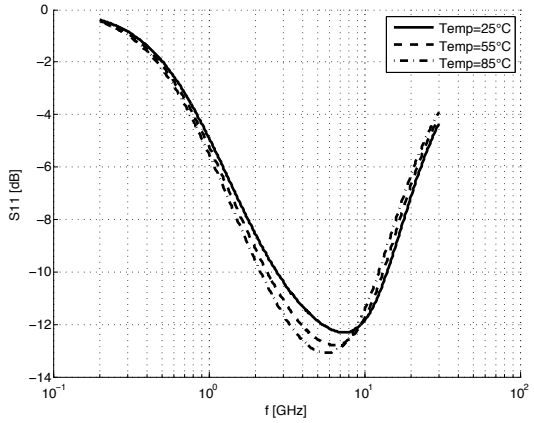

Figure 4.61: TIA - S11/Temp

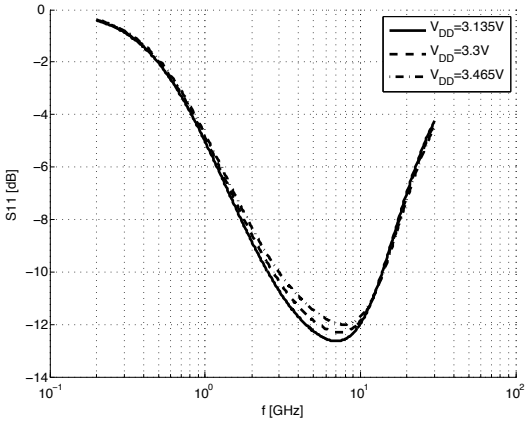

Figure 4.62: TIA - S11/V_{DD}

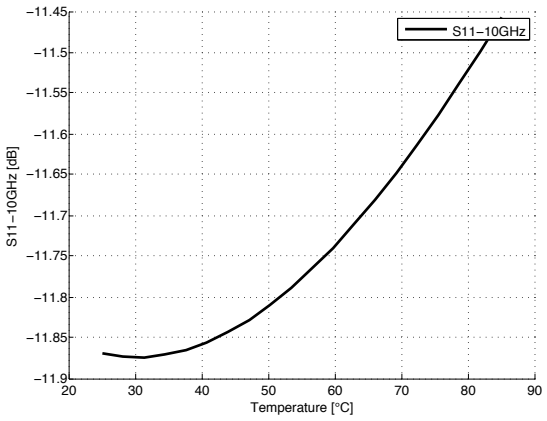

Figure 4.63: TIA - $S11_{10GHz}$/Temp

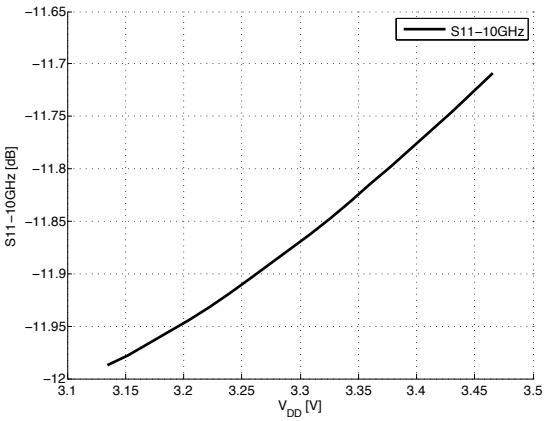

Figure 4.64: TIA - $S11_{10GHz}$/V_{DD}

From Fig. 4.61 and Fig. 4.62, it is possible to observe the $S11$ trend, considering temperature and supply voltage variations. Compared to the case of the inductive degeneration low noise amplifiers, with this solution a larger input matching bandwidth is obtained. Considering the value of $S11$ at 10 GHz, temperature and supply voltage increases determine a slight reduction of the matching performance, as shown in Fig. 4.63 and Fig. 4.64.

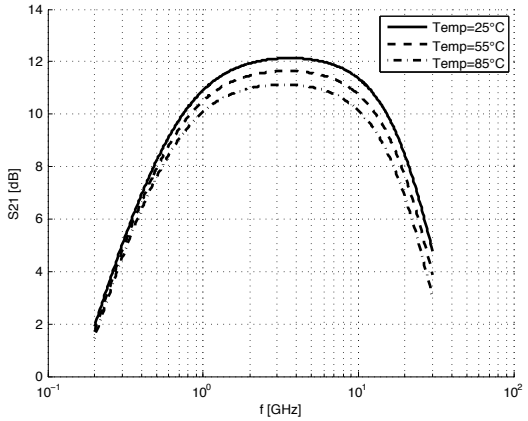

Figure 4.65: TIA - S21/Temp

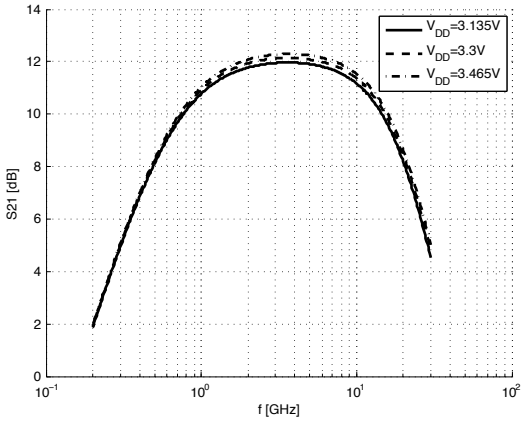

Figure 4.66: TIA - S21/V_{DD}

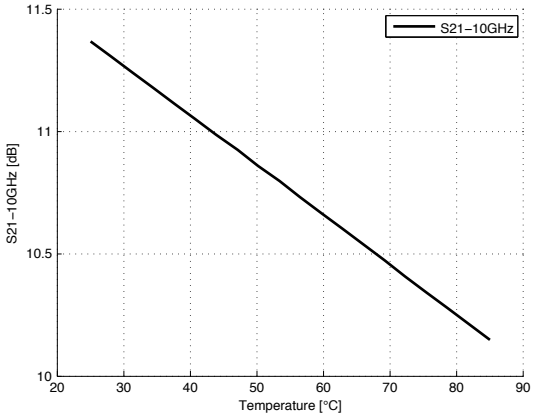

Figure 4.67: TIA - $S21_{10GHz}$/Temp

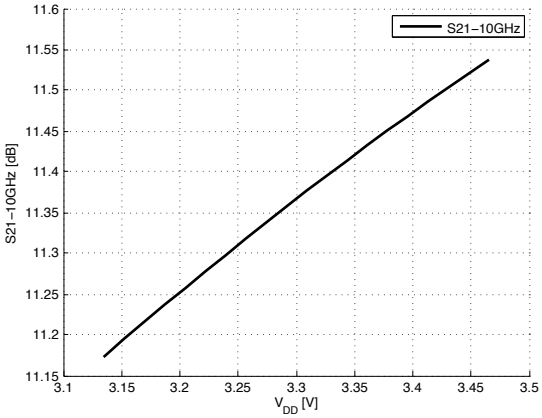

Figure 4.68: TIA - $S21_{10GHz}$/V_{DD}

Fig. 4.65 and Fig. 4.66 illustrate the frequency trend of the $S21$ parameter for the temperature and supply voltage variation. Considering Fig. 4.67 and Fig. 4.68, it is possible to evaluate the $S21$ parmeter at 10 GHz. Although the $S21$ variation is limited, the effect of temperature and supply voltage alteration is different from each other.

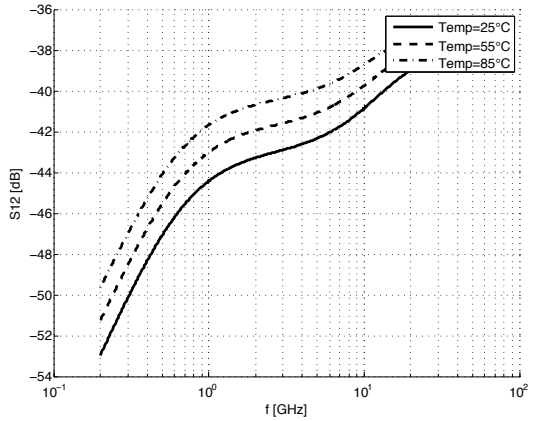

Figure 4.69: TIA - S12/Temp

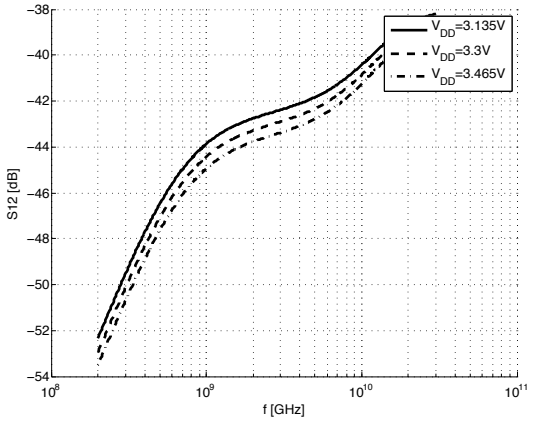

Figure 4.70: TIA - S12/V_{DD}

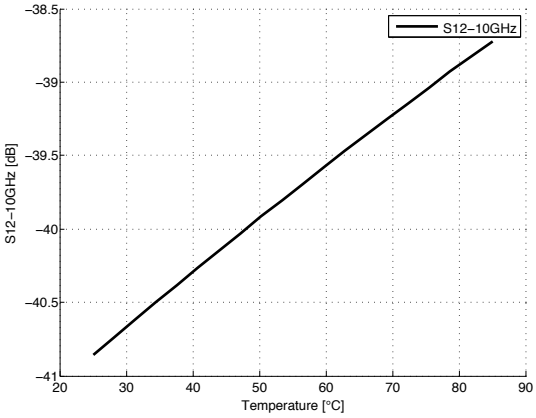

Figure 4.71: TIA - $S12_{10GHz}$/Temp

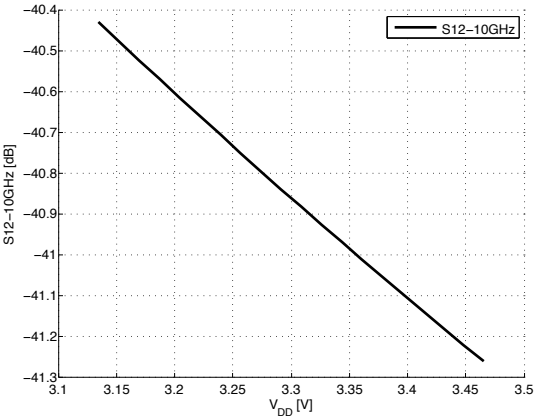

Figure 4.72: TIA - $S12_{10GHz}$/V_{DD}

Fig. 4.69 and Fig. 4.70 show the frequency trend of the inverse transmission coefficient $S12$, considering temperature and supply voltage variations. The value obtained is approximately $-43\,\mathrm{dB}$, less than the previous analyzed cases of narrowband low noise amplifiers. The variations of the value of $S12$ at $10\,\mathrm{GHz}$ are shown in Fig. 4.71 and Fig. 4.72.

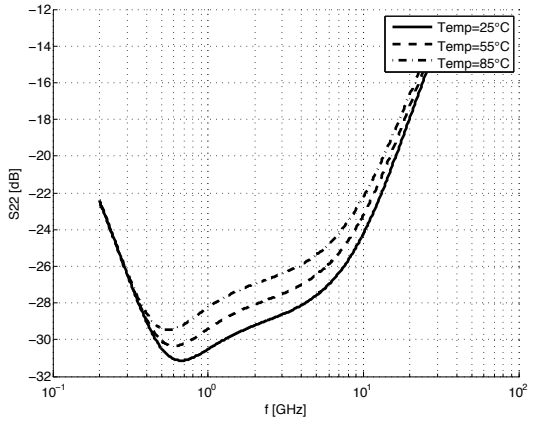

Figure 4.73: TIA - S22/Temp

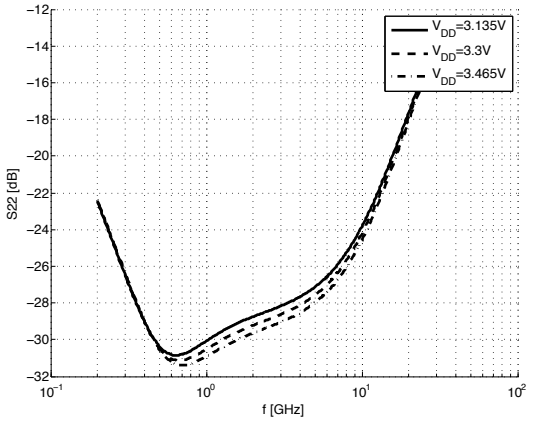

Figure 4.74: TIA - S22/V_{DD}

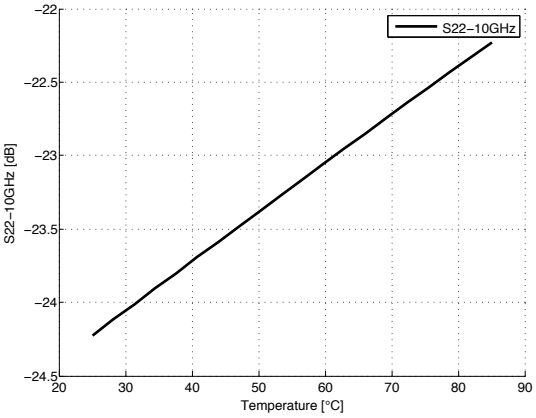

Figure 4.75: TIA - $S22_{10GHz}$/Temp

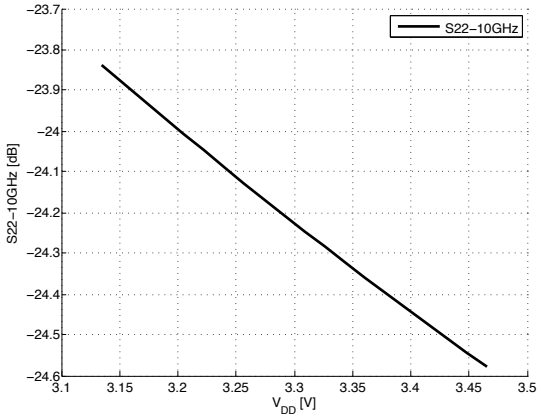

Figure 4.76: TIA - $S22_{10GHz}$/V_{DD}

The value of the $S22$ parameter obtained from the simulation is approximately $-30\,\mathrm{dB}$. Considering temperature and supply voltage variations, the results are plotted in Fig. 4.73 and Fig. 4.74. The $S22$ value at the operating frequency 10 GHz is shown in Fig. 4.75 and Fig. 4.76. It is possible to note that the temperature and supply voltage increases have different effects on the coefficient $S22$.

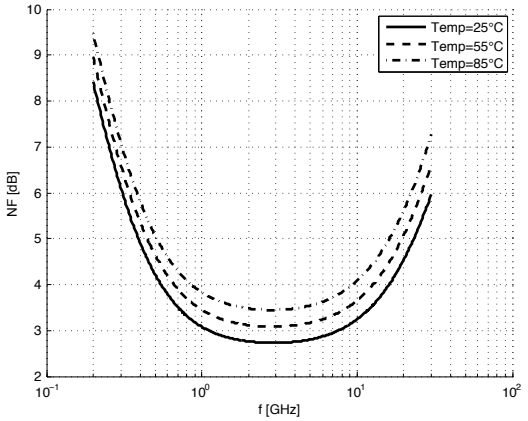

Figure 4.77: TIA - NF/Temp

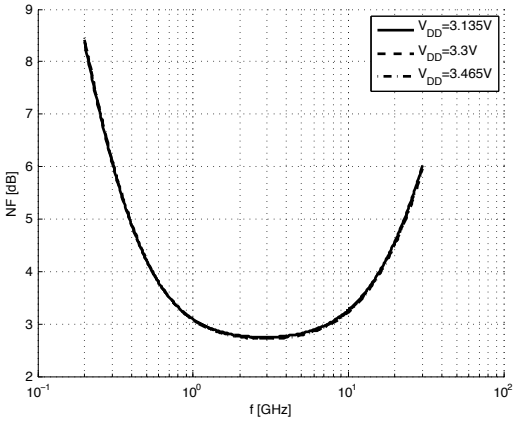

Figure 4.78: TIA - NF/V_{DD}

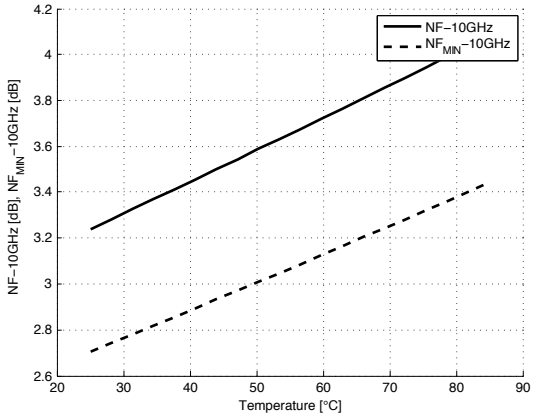

Figure 4.79: TIA - NF_{10GHz}/Temp

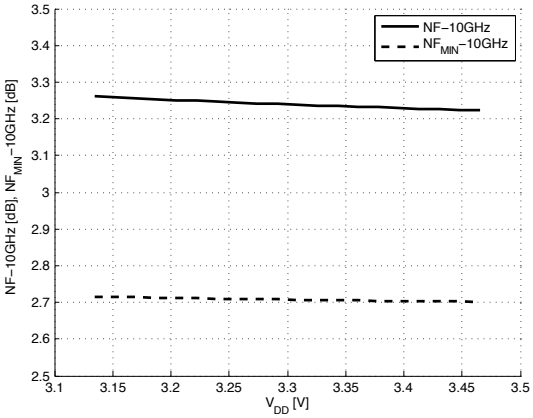

Figure 4.80: TIA - NF_{10GHz}/V_{DD}

The noise figure of the transimpedance amplifier is illustrated in Fig. 4.77 and Fig. 4.78, for the temperature and supply voltage variations. While the temperature increase determines an higher value of NF, as in the previous analyzed cases, a variation of V_{DD} has not a relevant effect on the noise figure. Fig. 4.79 and Fig. 4.80 show the NF_{MIN} and NF values at the operating frequency 10 GHz.

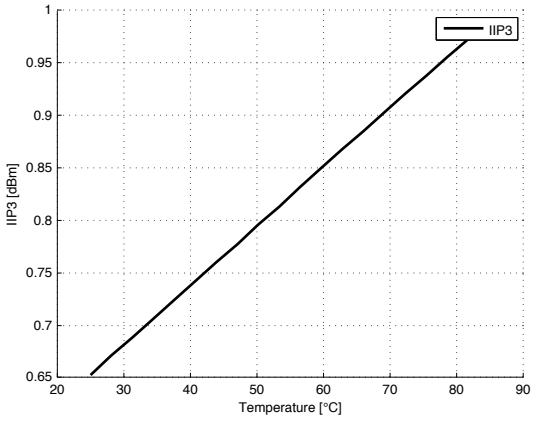

Figure 4.81: TIA - IIP3/Temp

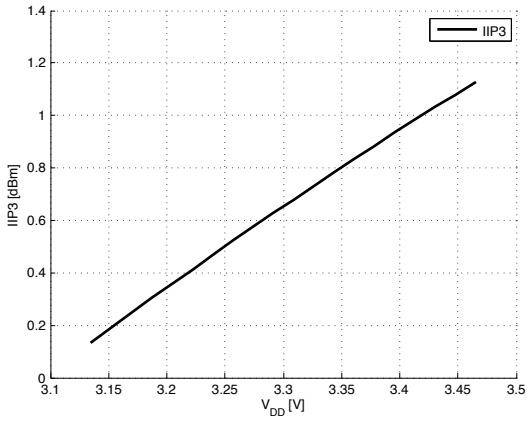

Figure 4.82: TIA - IIP3/V_{DD}

Fig. 4.81 and Fig. 4.82 show the dependence of the IIP3 parameter on the temperature and supply voltage values.

3.2 Monte Carlo simulation

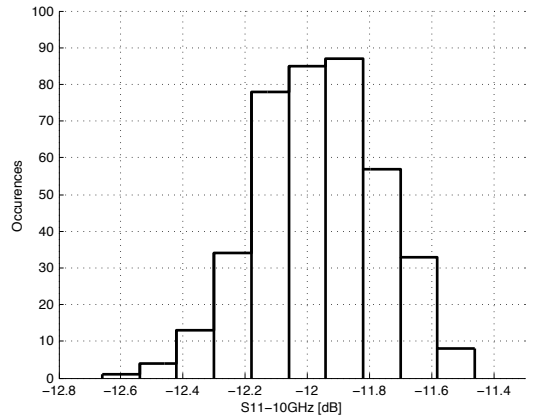

Figure 4.83: TIA - S11 MC simulation

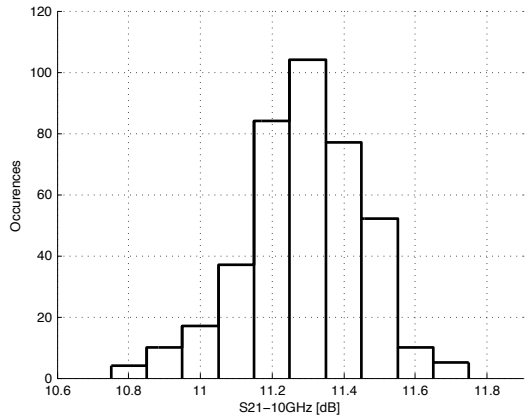

Figure 4.84: TIA - S21 MC simulation

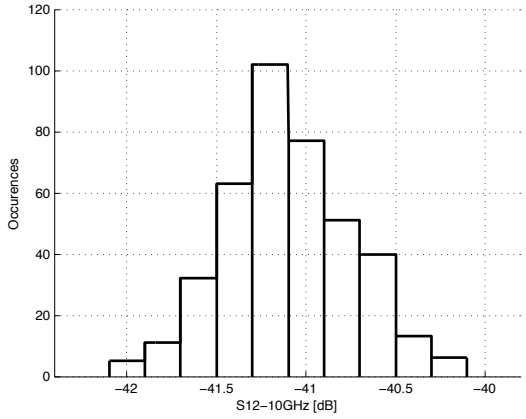

Figure 4.85: TIA - S12 MC simulation

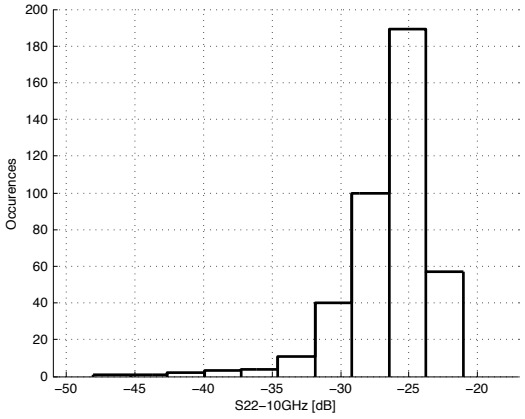

Figure 4.86: TIA - S22 MC simulation

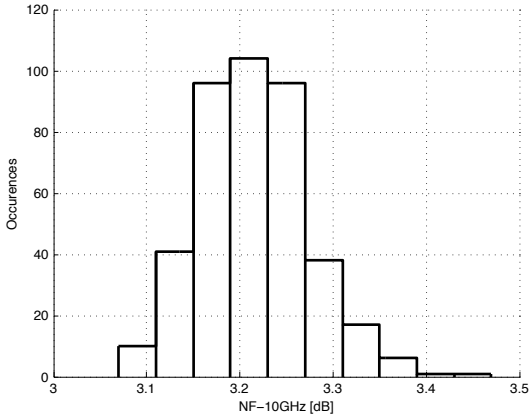

Figure 4.87: TIA - NF MC simulation

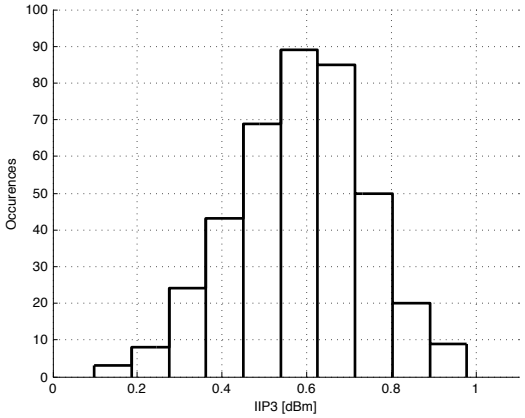

Figure 4.88: TIA - IIP3 MC simulation

Considering Fig. 4.83, Fig. 4.84, Fig. 4.85, Fig. 4.86, Fig. 4.87, and Fig. 4.88, it is possible to observe the results of the Monte Carlo analysis for the S-parameters, the noise figure, and the IIP3 parameter at 10 GHz. It is considered a random sampling method with 400 points, as for the previous low noise amplifiers discussed.

3.3 Stability

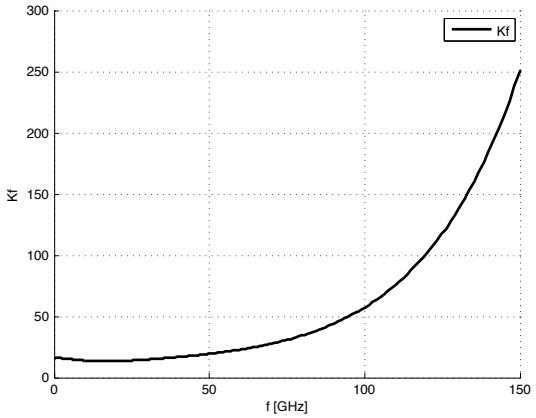

Figure 4.89: TIA - K_f factor

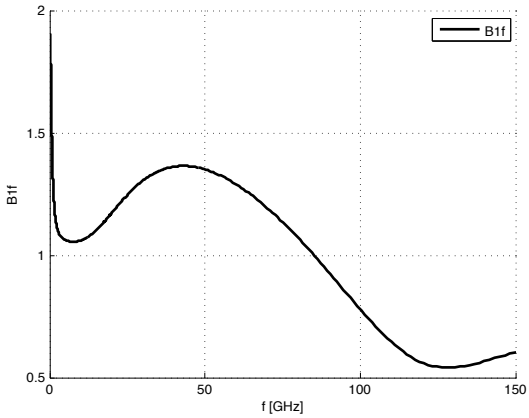

Figure 4.90: TIA - b_{1f} factor

Concerning the stability of the transimpedance amplifier, the parameter K_f and b_{1f} are shown in Fig. 4.89 and Fig. 4.90, considering the frequency range $0 \div 150\,\text{GHz}$. From these plots, the K_f parameter is always greater than 1 and b_{1f} is greater than 0, ensuring the stability of the wide-band low noise amplifier discussed.

3.4 Feedback resistor R_F variations

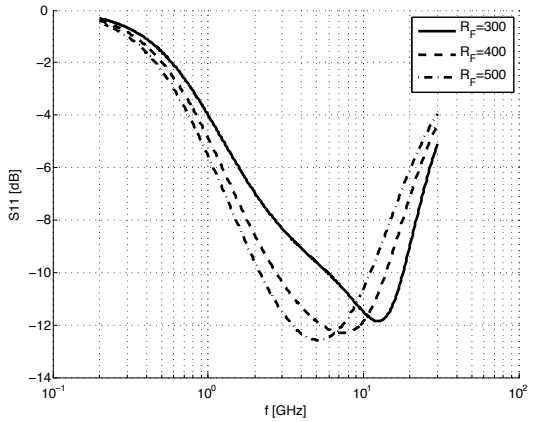

Figure 4.91: TIA - $S11/R_F$

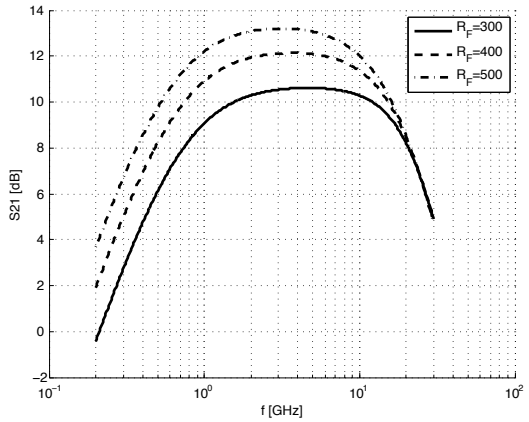

Figure 4.92: TIA - $S21/R_F$

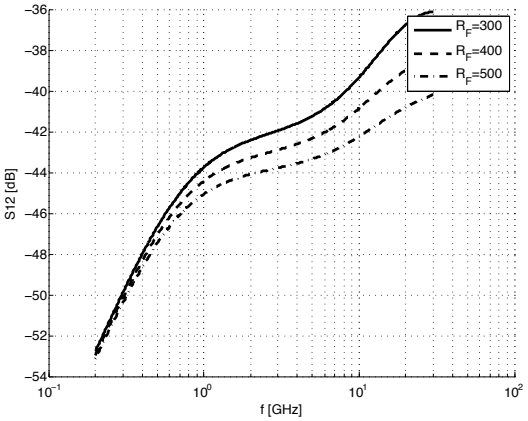

Figure 4.93: TIA - S12/R_F

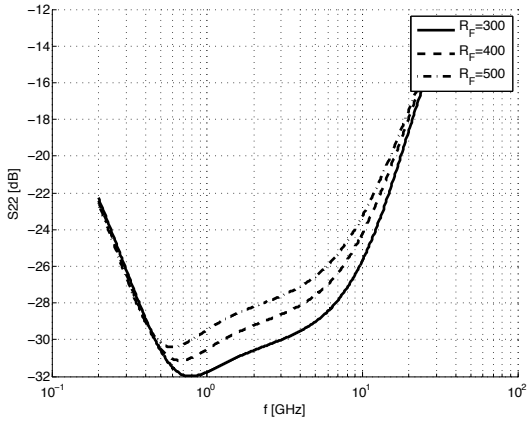

Figure 4.94: TIA - S22/R_F

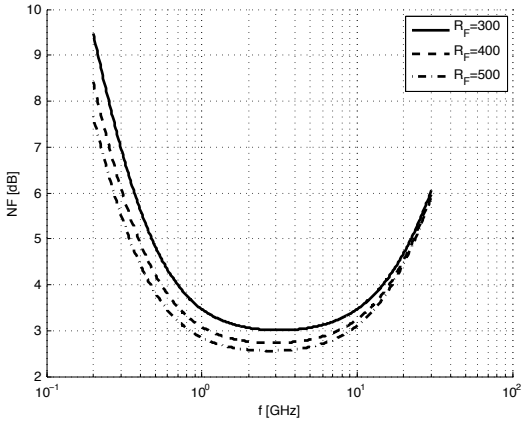

Figure 4.95: TIA - NF/R_F

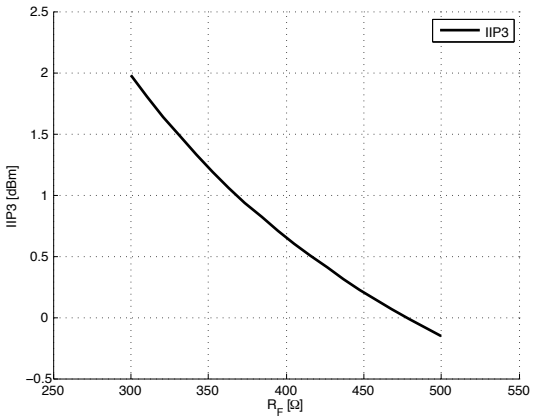

Figure 4.96: TIA - IIP3/R_F

In Fig. 4.91, Fig. 4.92, Fig. 4.93, Fig. 4.94, Fig. 4.95, and Fig. 4.96, it is possible to observe the effects of the R_F values on the S-parameters, noise figure and linearity of the designed transimpedance amplifier; in particular, increasing R_F, higher values of $S21$ and an improvement of noise performance are obtained, while the IIP3 parameter decreases as result of the decrement of the loop gain of the feedback system.

Chapter 5

Summary

This work has discussed the design of X-band low noise amplifiers for phased array radar systems. In the introduction chapter, the specifications have been discussed and the applications of this kind of amplifier are described, analyzing specifically the functional blocks of a transceiver module used for phased array radar system. An evaluation of the existing literature about the low noise amplifiers is also presented, together with the discussion of the SiGe technology and of the figures of merit to take into consideration. After that, the design of two narrow-band low noise amplifiers with inductive degeneration and a wide-band low noise amplifier is analyzed in detail. For the first two solutions, the noise analysis is discussed by an analytical point of view, and the classical approach which considers the current density and size of the devices to maximize the noise performance is described, evaluating also the inductors design and the effect of the ESD protection system. In particular, the first inductive degeneration topology is implemented with series base inductors, which degrade the noise figure of the amplifier. For this reason, the second low noise amplifier topology is proposed, removing these series inductors and implementing a different ESD protection. Tab. 5.1 summarizes the features of the two analyzed low noise amplifiers (LNA1 and LNA2), comparing them with other solutions proposed in the literature. In particular, the first half of the table reports the results for low noise amplifiers with a central frequency of 10 GHz, while the second one illustrates the results of proposed structures tuned at different frequencies. Generally, the cited references do not explain if the amplifiers discussed have an ESD protection and the emitter follower connected to the output, features presented by the solutions proposed in this work. Evaluating this table, it is possible to note that the single-ended (SE) topology can be implemented rather than using a differential (Diff) structure, considering also the single-ended output

of the antenna that precedes the low noise amplifier. While the results obtained for the gain, noise figure, and IIP3 are in accordance with the reported results in Tab. 5.1, the power consumption is slightly more than twice of that one of a single-ended structure at same frequency and realized with the same technology. This happens beacause the design has been implemented trying to get the best noise performance with this technology, not having a specification about the power consumption. However, halving the bias current the noise figure increases of about 0.2 dB, remaining in line with the results presented and obtaining an excellent power consumption. In addition, it would be possible to increase the gain of the proposed solutions, improving also the noise performance, but it is deliberately limited to avoid undesidered oscillations. Finally, the chip size is reported, where "*" means that the area including pads is considered.

Parameter	**LNA1**	**LNA2**	**[29]**	**[30]**	**[31]**	**[32]**
Tech	SiGe	SiGe	SiGe	SiGe	CMOS	SiGe
Topology	Diff	Diff	SE	SE	SE	SE
f[GHz]	10.0	10.0	10.0	10.0	10.0	10.0
Gain[dB]	18.6	18.8	22.0	19.5	15.8	24.2
NF[dB]	1.88	1.65	1.65	1.36	2.40	1.68
IIP3[dBm]	-2.1	-1.2	-8.0	0.8	-8.9	-6.7
$\mathbf{V_{supply}}$**[V]**	3.3	3.3	2.2	2.5	1.8	1.8
$\mathbf{P_{diss}}$**[mW]**	60.0	60.0	22.0	15.0	18.9	33.6
Size[µmxµm]	420x380	420x380	620x820	730x720*	/	2480x1380*
Year	2014	2014	2012	2006	2006	2005

Parameter	**[33]**	**[34]**	**[35]**	**[36]**	**[37]**	**[38]**
Tech	CMOS	CMOS	SiGe	CMOS	SiGe	SiGe
Topology	Diff	Diff	Diff	Diff	SE	Diff
f[GHz]	2.0	2.2	2.5	5.8	10.5	24.0
Gain[dB]	23.0	10.0	29.0	12.0	26.3	12.0
NF[dB]	2.85	1.87	1.32	1.7	2	3.1
IIP3[dBm]	-18.0	-2.1	-0.2	4.0	7.0	-1.8
$\mathbf{V_{supply}}$**[V]**	1.8	1.8	3.0	1.4	3.6	3.3
$\mathbf{P_{diss}}$**[mW]**	16.2	16.0	11.0	19.6	26.6	41.0
Size[µmxµm]	/	850x850	/	1200x1500*	450x550*	550x590*
Year	2013	2008	2009	2006	2000	2009

Table 5.1: Narrow-band low noise amplifiers comparison

Tab. 5.2 summarizes the results obtained for the proposed transimpedance amplifier (TIA) and it presents a literature performance overview with regards to wide-band amplifiers. Also in this case, in these references is not always so clear if the discussed solutions have an ESD protection and the emitter follower connected to the output. The proposed solution has an operating bandwidth comparable with [51], and larger than the other results listed below. Hence, the wider bandwidth and the technology used justify their higher power consumption, remembering that in [51] a single-ended (SE) solution is discussed. The CMOS solutions considered in this table present single-ended or differential topologies, and they exhibit a very low power consumption, even if [44] and [45] do not report the linearity results. The gain and the noise figure of this work are comparable with the references. Finally, the active area of the chip is reported, and "*" means that pads are included.

Parameter	**TIA**	**[44]**	**[45]**	**[46]**	**[47]**
Tech	SiGe	CMOS	SiGe	CMOS	SiGe
Topology	Diff	Diff	SE	SE	SE
f[GHz]	2.8÷14	4÷6	3.1÷10.6	2÷11	2÷10
Gain[dB]	12.1	17	14.2	12	13
NF[dB]	2.7÷3.3	<2.25	2.8÷3.8	5.5÷6	2.6÷3.3
IIP3[dBm]	0.38	/	/	-4	-7.5
V_{supply}[[V]	3.3	0.85	1.5	1.2	1.8
P_{diss}[mW]	50	12.1	5.4	17	9.6
Size[µmxµm]	300x150	970x840*	1380x970*	870x800*	/
Year	2014	2011	2007	2006	2005

Parameter	**[48]**	**[49]**	**[50]**	**[51]**
Tech	CMOS	CMOS	CMOS	SiGe
Topology	SE	SE	Diff	SE
f[GHz]	1.2÷11.9	2÷4.6	2.4÷6	2÷15
Gain[dB]	9.7	9.8	17.0	12.0
NF[dB]	4.5÷5.1	2.3÷4.0	2.4÷6.0	2.8÷4.0
IIP3[dBm]	-6.2	-7.0	-13	1.9
V_{supply}[V]	1.8	1.8	1.8	3.3
P_{diss}[mW]	20.0	12.6	40.0	24
Size[µmxµm]	900x650*	/	1090x1040*	550x450
Year	2005	2005	2005	2001

Table 5.2: Wide-band low noise amplifiers comparison

It is important to highlight that the results of this work are obtained by simulation. All the low noise amplifiers presented in this work will be produced as test-chip and they will be measured. If the specifications are fulfilled, especially for the second discussed narrow-band solution, the amplifier will be integrated in a phased array radar transceiver module.
Finally, the performance of the designed low noise amplifiers are summarized in Tab. 5.3.

Parameter	**LNA1**	**LNA2**	**TIA**
Tech	SiGe	SiGe	SiGe
Topology	Diff	Diff	Diff
f[GHz]	10.0	10.0	2.8÷14
Gain[dB]	18.6	18.8	12.1
NF[dB]	1.88	1.65	2.7
IIP3[dBm]	-2.1	-1.2	0.38
$\mathbf{V_{supply}}$**[V]**	3.3	3.3	3.3
$\mathbf{P_{diss}}$**[mW]**	60.0	60.0	50
Size[µmxµm]	420x380	420x380	300x150

Table 5.3: Performance of the designed low noise amplifiers

List of Figures

List of Tables

Bibliography

[1] M. Schneider, *"Automotive Radar - Status and Trends"*, Proceedings of the 2005 German Microwave Conference, pp. 144, 147, 5-7 April 2005

[2] T. Koga, X. Lu, *"Autonomous decentralized surveillance system and continuous target tracking technology for air traffic control applications"*, 2013 IEEE Eleventh International Symposium on Autonomous Decentralized Systems (ISADS), pp. 1, 8, 6-8 March 2013

[3] G. Margarit, J. Mallorqui, *"Operational approach for ship detection and classification"*, 2009 IEEE International Geoscience and Remote Sensing Symposium, IGARSS 2009, vol. 4, pp. IV-975, IV-978, 12-17 July 2009

[4] S. S. Ahmed, A. Schiessl, F. Gumbmann, M. Tiebout, S. Methfessel, L. Schmidt, *"Advanced Microwave Imaging"*, IEEE Microwave Magazine, vol. 13, no. 6, pp. 26, 43, September-October 2012

[5] M. Lucente, V. Dainelli, C. Dionisio, M. Noce, *"An innovative multimode millimeter wave radar for Moon remote sensing"*, 2009 IEEE Aerospace conference, pp. 1, 8, 7-14 March 2009

[6] P. M. Jeliazov, M. P. Jeliazov, M. S. Marinov, *"Influence of information technology on military radar systems"*, 2004 27th International Spring Seminar on Electronics Technology: Meeting the Challenges of Electronics Technology Progress, vol. 3, pp. 557, 563, 13-16 May 2004

[7] W. Sansen, *"Distortion in elementary transistor circuits"*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 3, pp. 315, 325, March 1999

[8] H. T. Friis, *"Noise Figures of Radio Receivers"*, Proceedings of the IRE, vol. 32, no. 7, pp. 419, 422, July 1944

[9] T. H. Ning, *"History and future perspective of the modern silicon bipolar transistor"*, IEEE Transactions on Electron Devices, vol. 48, no. 11, pp. 2485, 2491, November 2001

[10] D. L. Harame, B. S. Meyerson, *"The early history of IBM's SiGe mixed signal technology"*, IEEE Transactions on Electron Devices, vol. 48, no. 11, pp. 2555, 2567, November 2001

[11] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y. C. Sun, B. S. Meyerson, T. Tice, *"Si/SiGe epitaxial-base transistors. I. Materials, physics, and circuits"*, IEEE Transactions on Electron Devices, vol. 42, no. 3, pp. 455, 468, March 1995

[12] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y. C. Sun, B. S. Meyerson, T. Tice, *"Si/SiGe epitaxial-base transistors. II. Process integration and analog applications"*, IEEE Transactions on Electron Devices, vol. 42, no. 3, pp. 469, 482, March 1995

[13] B. Heinemann, R. Barth, D. Bolze, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, M. Lisker, S. Marschmeyer, H. Rucker, D. Schmidt, J. Schmidt, M. A. Schubert, B. Tillack, C. Wipf, D. Wolansky, Y. Yamamoto, *"SiGe HBT technology with f_T/f_{max} of 300GHz/500GHz and 2.0 ps CML gate delay"*, 2010 IEEE International Electron Devices Meeting (IEDM), pp. 30.5.1, 30.5.4, 6-8 December 2010

[14] R. K. Vytla, T. F. Meister, K. Aufinger, D. Lukashevich, S. Boguth, H. Knapp, J. Bdck, H. Schifer, R. Lachner1, *"Simultaneous Integration of SiGe High Speed Transistors and High Voltage Transistors"*, 2006 Bipolar/BiCMOS Circuits and Technology Meeting, pp. 1, 4, 8-10 October 2006

[15] M. Jahn, H. Knapp, A. Stelzer, *"A 122-GHz SiGe-Based Signal-Generation Chip Employing a Fundamental-Wave Oscillator With Capacitive Feedback Frequency-Enhancement"*, IEEE Journal of Solid-State Circuits, vol. 46, no. 9, pp. 2009, 2020, September 2011

[16] K. L. Fong, R. G. Meyer, *"High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages"*, IEEE Journal of Solid-State Circuits, vol. 33, no. 4, pp. 548, 555, April 1998

[17] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *"Analysis and Design of Analog Integrated Circuits"*, Fifth edition, Wiley, 2010

[18] T. H. Lee, *"The design of CMOS Radio-Frequency Integrated Circuits"*, Second edition, Cambridge University Press, 2004

[19] R. S. Muller, T. I. Kamins, *"Device Electronics for Integrated Circuits"*, Third edition, Wiley, 2003

[20] W. D. Greason, *"Constant charge and constant potential models for electrostatic discharge (ESD) and the human body"*, 1997 Thirty-Second IAS Annual Meeting Industry Applications Conference, vol. 3, pp. 1891, 1900, 5-9 October 1997

[21] M. D. Ker, C. Y. Lin, Y. W. Hsiao, *"Overview on ESD Protection Designs of Low-Parasitic Capacitance for RF ICs in CMOS Technologies"*, IEEE Transactions on Device and Materials Reliability, vol. 11, no. 2, pp. 207, 218, June 2011

[22] P. Leroux, M. Steyaert, *"A 5 GHz CMOS low-noise amplifier with inductive ESD protection exceeding 3 kV HBM"*, Proceeding of the 30th European Solid-State Circuits Conference, ESSCIRC 2004, pp. 295, 298, 21-23 September 2004

[23] S. P. Voinigescu, *"High-Frequency Integrated Circuits"*, First edition, Cambridge University Press, 2013

[24] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, D. L. Harame, *"A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design"*, IEEE Journal of Solid-State Circuits, vol. 32, no. 9, pp. 1430, 1439, September 1997

[25] O. Shana'a, I. Linscott, L. Tyler, *"Frequency-scalable SiGe bipolar RF front-end design"* IEEE Journal of Solid-State Circuits, vol. 36, no. 6, pp. 888, 895, June 2001

[26] G. Girlando, G. Palmisano, *"Noise figure and impedance matching in RF cascode amplifiers"* IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 11, pp. 1388, 1396, November 1999

[27] A. Bevilacqua, A. M. Niknejad, *"An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers"*, IEEE Journal of Solid-State Circuits, vol. 39, no. 12, pp. 2259, 2268, December 2004

[28] D. K. Shaeffer, T. H. Lee, *"A 1.5 V, 1.5 GHz CMOS low noise amplifier"*, 1996 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 32, 33, 13-15 June 1996

[29] T. Dinc, S. Zihir, I. Kalyoncu, Y. Gurbuz, *"X-band, high performance, SiGe-heterojunction bipolar transistors-low noise amplifier for phased array radar applications"*, IET Microwaves, Antennas & Propagation, vol. 6, no. 7, pp. 768, 772, May 2012

[30] W. L. Kuo, Q. Liang, J. D. Cressler, M. A. Mitchell, *"An X-band SiGe LNA with 1.36 dB mean noise figure for monolithic phased array transmit/receive radar modules"*, 2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 4, 501, 11-13 June 2006

[31] W. N. Chen, K. H. Cheng, T. D. Chang, *"A 10GHz With Low Power And Low Noise Figure Amplifier Using 0.18μm CMOS Technology"*, ICSICT '06. 8th International Conference on Solid-State and Integrated Circuit Technology, pp. 1556, 1558, 23-26 October 2006

[32] V. J. Patel, H. S. Axtell, C. L. Cerny, G. L. Creech, R. G. Drangmeister, M. A. Gouker, T. L. James, A. G. Mattamana, I. O. Mbuko, R. A. Neidhard, E. B. Nykiel, P. L. Orlando, D. L. Selke, J. M. Wiedemann, T. K. Quach, *"X-band low noise amplifier using SiGe BiCMOS technology"*, CSIC '05. IEEE Compound Semiconductor Integrated Circuit Symposium, pp. 4, 30 October - 2 November 2005

[33] M. NarayanaSwamy, D. P. Acharya, *"A power improvement technique for a differential LNA"* 2013 Students Conference on Engineering and Systems (SCES), pp. 1, 5, 12-14 April 2013

[34] X. Fan, H. Zhang, E. Sanchez-Sinencio, *"A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA"* IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 588, 599, March 2008

[35] H. B. Zhangl, H. Wu, M. Cai, H. L. Chen, *"A 2.5GHz BiCMOS low noise and high-gain differential LNA for WLAN receiver"* Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics, Prime Asia 2009, pp. 33, 36, 19-21 January 2009

[36] L. Aspemyr, H. Sjoland, H. Jacobsson, M. Bao, G. Carchon, *"A 5.8 GHz 1.7 dB NF fully integrated differential low noise amplifier in CMOS"* Asia-Pacific Microwave Conference, APMC 2006, pp. 309, 312, 12-15 December 2006

[37] D. Zoschg, W. Wilhelm, H. Knapp, M. Wurzer, T. F. Meister, J. Bock, H. D. Wohlmuth, K. Aufinger, L. Treitinger, *"Monolithic integrated LNAs in silicon-based bipolar technologies"* IEEE/AFCEA EUROCOMM 2000, Information Systems for Enhanced Public Safety and Security, pp. 400, 403, 2000

[38] V. Issakov, H. Knapp, M. Wojnowski, A. Thiede, W. Simburger, G. Haider, L. Maurer, *"ESD-Protected 24 GHz LNA for Radar Applications in SiGe:C Technology"* SiRF '09. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp.1, 4, 19-21 January 2009

[39] K. O, *"Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies"*, IEEE Journal of Solid-State Circuits, vol. 33, no. 8, pp. 1249, 1252, August 1998

[40] A. M. Niknejad, R. G. Meyer, *"Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs"*, IEEE Journal of Solid-State Circuits, vol. 33, no. 10, pp. 1470, 1481, October 1998

[41] K. Van Schuylenbergh, C.L. Chua, D.K. Fork, Jeng-Ping Lu, B. Griffiths, *"Self-assembled out-of-plane high-Q integrated inductors"*, IEDM '02 International Electron Devices Meeting, pp. 479, 482, 8-11 December 2002

[42] A. Bevilacqua, M. Camponeschi, M. Tiebout, A. Gerosa, A. Neviani, *"Design of broadband inductorless LNAs in ultra-scaled CMOS technologies"*, IEEE International Symposium on Circuits and Systems, ISCAS 2008, pp. 1300, 1303, 18-21 May 2008

[43] J. Lee, J. D. Cressler, *"Analysis and design of an ultra-wideband low-noise amplifier using resistive feedback in SiGe HBT technology"*, IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 3, pp. 1262, 1268, March 2006

[44] Y. Tu, C. Wang, *"A 4-6GHz current-mode differential transconductance wide band LNA"*, 2011 International Conference on Electrical and Control Engineering (ICECE), pp. 2821, 2824, 16-18 September 2011

[45] S. C. Chen, R. L. Wang, C. L. Tsai, J. H. Shang, C. H. Liu, *"A low power, good gain flatness SiGe low noise amplifier for 3.1-10.6GHz ultra wide band radio"*, 50th Midwest Symposium on Circuits and Systems, MWSCAS 2007, pp. 750, 753, 5-8 August 2007

[46] C. S. Wang, C. K. Wang, *"A 90nm CMOS Low Noise Amplifier Using Noise Neutralizing for 3.1-10.6GHz UWB System"*, Proceedings of the 32nd European Solid-State Circuits Conference, ESSCIRC 2006, pp. 251, 254, September 2006

[47] Y. Park, C. H. Lee, J. D. Cressler, J. Laskar, A. Joseph, *"A very low power SiGe LNA for UWB application"*, 2005 IEEE MTT-S International Microwave Symposium Digest, pp. 4, 12-17 June 2005

[48] C. F. Liao, S. I. Liu, *"A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receiver"*, Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, pp. 161, 164, 18-21 September 2005

[49] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, S. G. Lee, *"An ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB system"*, IEEE Journal of Solid-State Circuits, vol. 40, no. 2, pp. 544, 547, February 2005

[50] C. P. Chang, C. C. Yen, H. R. Chuang, *"A 2.4-6GHz CMOS Broadband High-Gain Differential LNA for UWB and WLAN Receiver"*, Asian Solid-State Circuits Conference, pp. 469, 472, 1-3 November 2005

[51] H. Knapp, D. Zoschg, T. Meister, K. Aufinger, S. Boguth, L. Treitinger, *"15 GHz wideband amplifier with 2.8 dB noise figure in SiGe bipolar technology"*, 2001 IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 591, 594, 20-24 May 2001