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Study of influence of bulk on breakdown and trapping phenomena in power AlGaN/GaN MIS-HEMTs grown on Si-substrate

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"Prima impara, poi chissà!"
Mago Merlino ne *"La spada nella roccia"*

A Laura,
Mamma, Papà e Sorellina.
E a tutti i miei amici.

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INTRODUCTION

Gallium-Nitride (GaN) is a III-V compound semiconductor, composed by Gallium (III group) and the Nitrogen (V group). The wide band gap (WBG) is the main characteristic of all III-V compound semiconductors.

GaN was firstly synthesized in 1932, however only in the middle of 1980s, the development of GaN-based devices was boosted by the production of new generation blue lasers and white and blue light-emitting-diodes (LEDs). In the early 1990s, GaN and its alloys were deemed ready for high power and frequency transistors beacause of its excellent parameters such as wide bandgap, high electron mobility, high sustainable breakdown field saturated electron velocity, thermal and mechanical stability and power density.

Therefore they are able to satisfy new needs in military, telecommunication and power fields, by significant high voltage, high power and high frequency capability. Their main applications are radar, electronic warfare, radio communications, solid state lightning, lasers, detectrors and high power amplifiers and switches.

In table 1 we can see that not all semiconductors can reach high performances, even if they are compound semiconductors such as Gallium-Arsenide (GaAs). In particular, Silicon which is the most common and basic material for many electronic applications, does not satisfy high operating frequency. To overcome this lack, GaAs-based devices can be employed. However the latter presents another problem: a limited breakdown voltage and power density, necessaries for high power devices. GaN and SiC present higher power density, even at higher frequencies. In figure 1 the pictorial comparison among GaN, SiC and Si is reported. We note that GaN is a very suitable material for high-voltage and high-frequency operations.

	Si	GaAs	SiC	GaN
Bandgap $[eV]$	1.1	1.42	3.25	3.49
Electron mobility $[cm^2/Vs]$	1500	8500	700	1000-2000
Saturated electron velocity $[\cdot 10^7 cm/s]$	1	1.3	2	2.5
Critical Breakdown Field $M[V/cm]$	0.3	0.4	3	3.3
Thermal Conductivity$[W/cm°K]$	1.5	0.5	4.5	>1.5
Relative Dielectric Constant ϵ_r	11.8	12.8	10	9
2DEG concentration$[cm^{-2}]$	NA	$4 \cdot 10^{12}$	NA	$1.2 \cdot 10^{13}$

Table 1: Comparison of main semiconductor material parameters.

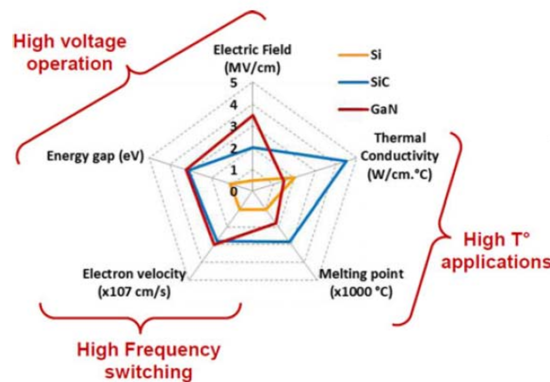


Figure 1: Si, SiC and GaN properties. Taken from [37].

The employment of GaN and its alloys is the key feature for improving performances, efficiency and reducing losses thanks to their electrical, thermal and switching-frequency properties.

0.1 POWER SWITCHING HEMTS

Power devices are mainly divided in rectifiers and switches employed in commutation mode. Diodes are an example of rectifier devices, instead MOSFETs, IGBTs and BJTs are the most important switches employed.

A good switch must satisfy the following requests:

- low resistance in on-state R_{on},

- high breakdown voltage,
- low leakage currents in off-state,
- high power density,
- high thermal conductivity.

Hence, an ideal power switch must behave as an oper circuit in off-state and as a short circuit in on-state. In real devices leakage currents flow, a non-zero voltage drops across it, parasitic capacitances reduce the high switching frequency. Because of that, the aim of research is to reduce these parasitic effects and a powerful instrument to improve technology is to study trapping phenomenac and parasitic effects.

Among the power switch devices, the High Electron Mobility Transistors (HEMTs) based on a heterostructures between two compound semiconductors is one of the most promising high-power devices. These devices are naturally normally-on devices. At the beginning, HEMTs were based on the AlGaAs/-GaAs heterostructures. However their limits are low heat conductivity and low breakdown field.

To overcome these problems and satisfy new market requests, AlGaN/GaN-based heterostructure devices began to be studied. They have a higher piezoelectric and spontaneous polarization at the interface between the two materials enhancing the two Dimensional Electronic Gas (2DEG) concentration[1]. The latter is the core of a HEMT and for AlGaN/GaN based HEMT is one order of magnitude higher than in AlGaAs/GaAs heterostructures. The AlGaN/GaN heterostructures can reach a $2x10^{13}cm^{-2}$ concentration[48] and have an excellent tradeoff between specific R_{on} and breakdown voltage. IN 1994 the first AlGaN/GaN HEMT was grown on sapphire substrate [20].

Concerning on GaN HEMTs on Silicon substrate the best breakdown performances was reached by IMEC team at 2.2kV [49].

Commercially normally-on and normally-off GaN HEMTs can substain voltage breakdown of $20-600V$[37].

This thesis work is based on the study of trapping phenomena in power HEMTs based on Gallium-Nitride (GaN).

In the following, the outline of the thesis is presented :

THE FIRST CHAPTER aims to show the structure and properties of AlGaN/GaN HEMTs and to explain how they work and their parasitic effects. A particular attention is paided on the features exhibited by Silicon-based substrates and Metal-Insulator-Semiconductor structure at gate contact.

THE SECOND CHAPTER describes the devices employed during the measurements.

THE THIRD CHAPTER is dedicated to the presentation of the system measurements and the aim of each one.

IN THE FOURTH CHAPTER the expherimental results are shown. Firstly, the preliminary characterizations are shown, then the role of bulk is investigated by means of breakdown and backgating measurements. The analysis of the R_{on} collapse and the buffer region is maken through backgating on-the-fly and transients measurements. Finally, the threshold voltage shift is investigated through transients and on-the-fly measurements which test the gate contact region.

THE FIFTH CHAPTER presents the measurement conclusions.

THE APPENDIX A is dedicated to a review of the articles which deal with the vertical breakdown from drain to substrate in AlGaN/GaN HEMTs.

1 GAN-BASED HEMTS

HEMTs is the acronym of High Electron Mobility Transistors.

A HEMT is a transistor that presents four contact terminals: gate, drain, source and bulk. Thanks to the presence of Two Dimensional Electronic Gas 2DEG at the AlGaN/GaN interface, that acts as a channel in conventional MOSFETs, electrons flow from source to drain, and the current is modulated by the gate voltage. The 2DEG is formed without applying any gate voltage so HEMTs are normally-on devices. The drain-source current I_{ds} flows if the channel is formes and a $V_{ds} > 0$ is applied.

The role of bulk substrate and its influence on the device behaviour will be discussed in the next chapters.

The aim of this chapter is to provide the physical bases to understand the behaviour of AlGaN/GaN HEMTs. We will discuss the intrinsic properties of the material, the relation among spontaneous polarization, piezoelectric polarization and the Two Dimensional Electronic Gas (2DEG) at the interface of an AlGaN/GaN heterojunction. This latter phenomenon is the core of HEMT behaviour and it is not present in a homojunction device. The substrate on which GaN-based devices are grown and the relations between them and the introduced parasitic effects will be also presented.

1.1 CRYSTAL LATTICE STRUCTURE AND PROPERTIES

To understand what happens in a GaN-based device, especially the 2DEG formation, it is very important to know the structure and the properties of the crystal lattice formed by Gallium and Nitride atoms and the Alluminium-based alloys.

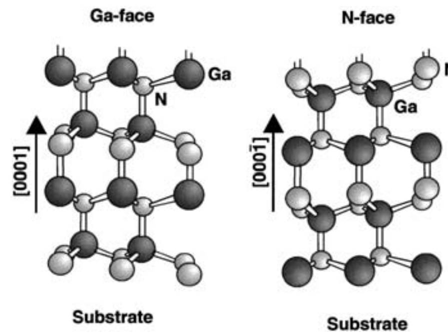


Figure 2: Drawings of the spontaneous and piezoelectric polarization induced sheet charge density for Ga-face and N-face and strained and relaxed AlGaN/GaN heterostructures[1]. We can see that both crystals are naturally distorted because of the strong ionicity of nitrogen and the consequent strong polarization [63].

There are two main crystalline structures for GaN lattice: the zincblende and the wurtzite, but only the latter one is thermodynamically stable [62]. The wurtzite lattice structure presents a hexaghonal simmetry, as can be seen in figure 2. The bond between Gallium and Nitride is ionic because of the large difference in electronegativity of Gallium and Nitride atoms[1]. The wurtzite can be Ga-face or N-face, depending on the growth condition which have different polarities. Because of its electrical transport properties and lower buffer resistivity, Ga-face devices are preferred.

Ga-face and N-face

In both Ga-face and N-face materials, GaN presents spontaneous polarization(P_{SP}) due to the strong ionicity of its molecules.

Spontaneous polarization

An example about how to strain a materials, is growing one material above another one with different lattice constants: this happens between AlN and GaN for example.

Generally devices are built by different layer material. If two adjacent materials have different lattice constants, there will be induced an extarnal strain polarization which is called piezoelectric polarization (P_{PE}) or strain-induced polarization. This polarization exerts a substantial influence on charge density and electric field distributions[1].

Piezoelectric polarization

1 Nitride is the most electronegative element in group V of the period table of the elements.

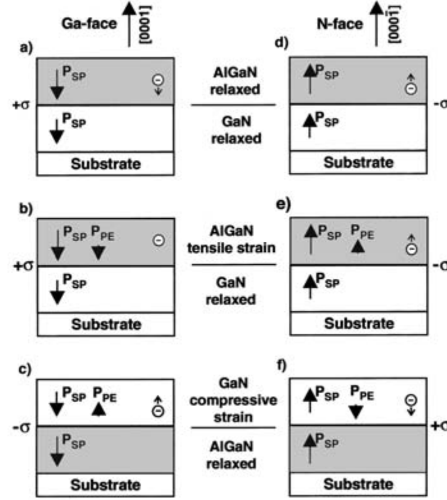


Figure 3: Crystal structure of GaN grown on Ga-face and N-face[1].

	AlN	GaN	$Al_xGa_{1-x}N$
Lattice constant [A]	3.11	3.19	-0.08x + 3.19
Relative Dielectric const.	9	9.5	-0.5x + 9.5
$P_{sp}[C/m^2]$	-0.081	-0.029	-0.052x -0.029
$e_{33}[C/m^2]$	1.46	0.73	0.73x + 0.73
$C_{13}[Gpa]$	108	103	5x + 103
$C_{33}[Gpa]$	373	405	-32x + 405

Table 2: Spontaneous polarization, piezoelectric and dielectric constants on III-N materials. The x stands for Al%.

Concerning on piezoelectric polarization, if the horizontal lattice constant a is varied from its natural value a_0 there will be non-zero along the vertical (c) axis:

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{1}$$

where the values of parameters are indicated in table 2. By this formula, we note that the value of piezoelectric polarization is always negative if $a > a_0$. For AlGaN, the piezoelectric polarization increases with the Al content.

Polarization at AlGaN/GaN interface

If the layers are not strained, both piezoelectric and spontaneous polarization are negative and parallel, otherwise they are opposite. In particular at the interface AlGaN/GaN, there is a

non-zero polarization charge induced by piezoelectric polarization, and the polarization sheet charge density is defined by:

$$\sigma_{pol} = \sigma_{\frac{AlGaN}{GaN}} = P_{SPAlGaN} + P_{PEAlGaN} - P_{SPGaN} > 0. \quad (2)$$

1.1.1 The formation of 2DEG

By the fact that σ_{pol} is positive, free electrons will tend to compensate the polarization induced charge. These electrons will form a carrier sheet named Two Dimensonal Electronic Gas (2DEG) at the AlGaN/GaN interface with a carrier density n_s. This negative sheet, in turn, causes a positive accumulation of charges at the interface metal/AlGaN. The electrons in 2DEG are free to move in this quantum well and typical values of n_s are in the order of $\sim 1-2 \cdot 10^{13} cm^{-2}$ as reported in [12].

According to [12] the source of electrons in 2DEG is the donor-like surface states[2] of AlGaN layer. This process can only occur if the AlGaN barrier thickness is grater than a critical thickness t_{cr} which will be calculated in the following.

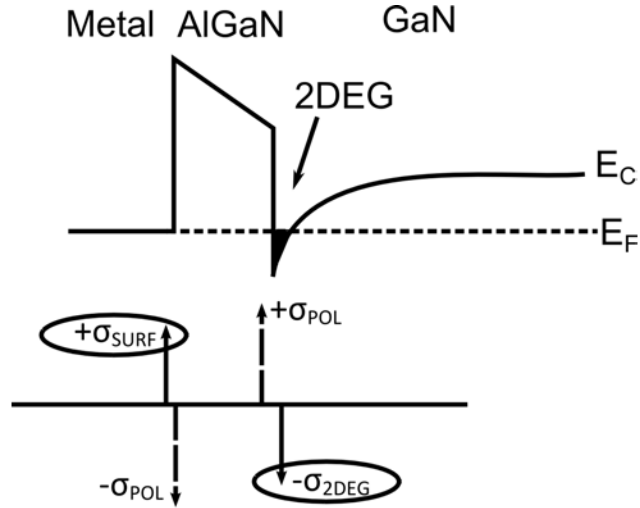


Figure 4: charge distribution in an AlGaN/GaN heterostructure.

If no external field is applied, the sum of the various space charge should be zero and compensated. Therefore also the total piezoeletric polarization should be.

2 A donor-like state is a state which is neutral when occupied by a carrier and positive when empty.

In presence of undoped AlGaN barrier layer, the neutrality of charge equation gives:

$$\sigma_{Surface} - \sigma_{PE} + \sigma_{PE} - qn_s = 0 \rightarrow qn_s = \sigma_{Surface} \quad (3)$$

thanks to the dipole origine of spontaneous, piezoelectric and polarization induced-charges.

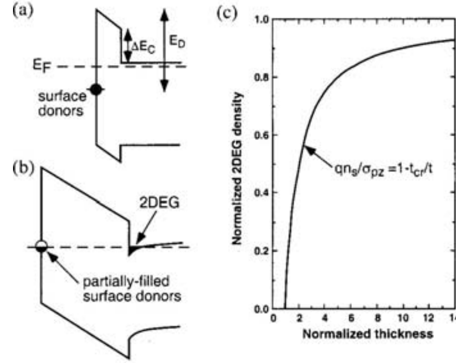


Figure 5: Surface donor model proposed by [12].

Surface donor-like state model

We consider now a deep surface state at an energy E_D below the conduction band and we see the influence of the AlGaN barrier thickness t on the effective 2DEG creation. If t is too much thin ($t < t_{cr}$), E_D lies below the Fermi level E_F so there is no formation of 2DEG because

$$\sigma_{Surface} = 0 \rightarrow qn_s = \sigma_{Surface} = 0. \quad (4)$$

As shown in figure 5, increasing the barrier thickness, the E_D energy reaches the E_F Fermi level and in this condition electrons are able to transfer from occupied surface state to empty conduction band states at the interface, giving rise to 2DEG and leaving behind positive surface charge. The critical thickness can be expressed by:

Critical AlGaN barrier thickness

$$t_{cr} = \frac{(E_D - \Delta E_C)\epsilon_{AlGaN}}{q\sigma_{PE}} \quad (5)$$

where $\epsilon_{AlGaN} = \epsilon_{AlGaN}(x) = -0.5x + 9.5$ in function of Al percentage and ΔE_C is the AlGaN conduction band offset. The

worst case is when E_D is in the middle of the AlGaN energy gap.

Finally, the 2DEG density concentration is calculated by:

$$n_s = \frac{\sigma_{PE}}{q}(1 - \frac{t_{cr}}{t}) \qquad (6)$$

By what said before, we obtain a good density of electron in the quantum well through a thick barrier and an high Al percentage.

1.1.2 High temperature properties

In the section before has been presented the basical role of the AlGaN/GaN heterostructure and its effects. In certain high power applications, the device temperature stability is extremely important and must be taken into account during the development of new devices.

Now we are going to present some useful concepts concerning on the dependence of temperature of 2DEG, energy gap, carrier concentration and mobility which are all temperature dependent parameters.

In [58] these parameters are studied by Hall measurements in a structure which present from the bottom a sapphire substrate, a nucleation gaN buffer layer, an unintentionally doped GaN (i-GaN), an unintentionally doped $Al_{0.18}Ga_{0.82}N$ (i-AlGaN) and ohmic contant stack of Ti/Al/Ni/Au at the top.

In figure 6a are reported the electron concentration and mobility in the i-GaN. We note that in the range 0°C 200°C the mobility highly decrease, instead the electron concentration grows. To explanation suggested of the mobility saturation at high temepratures is related to the longitudinal optical phonon scattering.

Concerning on the 2DEG, in figure 6b is shown the 2DEG mobility and density: until 200°C both parameter decrease. A possible explanation for the 2DEG density decrease is that decrease of the conduction band offset.

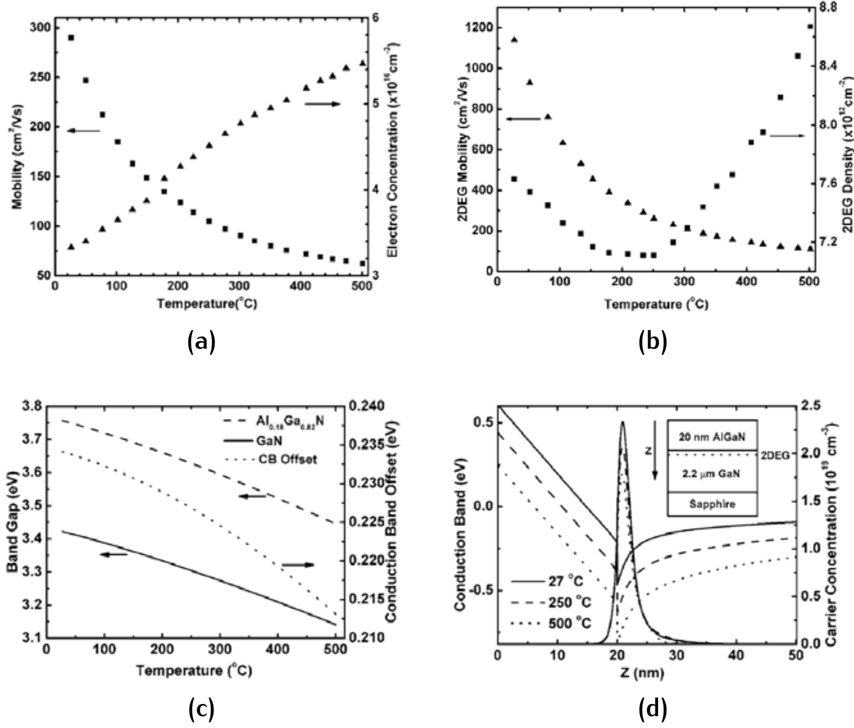


Figure 6: Effect of temperature on parameters in an AlGaN/GaN heterostructure. Taken from [58].

Even the energy gap E_g is not so insensitive to temperature, since it decreases with temperature by the formula:

$$E_g(T) = E_g(0°C) - \frac{\alpha T^2}{T + \beta} \quad (7)$$

where for GaN $E_g 0°C = 3.5eV$, $\alpha = 0.94meV/K$ and $\beta = 791K$; instead for AlN are $6.2eV$, $2.63meV/K$ and $2082K$ [58].

The bandgap of $Al_xGa_{1-x}N$ at a certain mole concentration x can be calculate by

$$E_g(x, T) = (1 - x)E_g(GaN)(T) + xE_g(AlN)(T) - bx(1 - x) \quad (8)$$

where b is about $1eV$.

The conduction band offset shown in figure 6c. We note that it decreases as well as the bandgap pf GaN and AlN. This might explain the decrease in the 2DEG density.

Finally in figure 6d is depicted the calculated band profile at the junction and the carrier distribution.

1.2 WORKING PRINCIPLES

Before analysing the power HEMT structure to deeply understand the role of which layer, how an HEMT works is reported.

In figure 7 is depicted the working principle of an HEMT. When $Vg < Vth$ is applied at gate contact (see figure 7a), the channel is interrupted under the gate because of the depletion region and the electrons of the 2DEG cannot flow from source to drain. In a simple AlGaN/GaN HEMT just like that in figure, the threshold voltage Vth is negative because of the natural presence of 2DEG: the device is normally-on.

As soon as $Vg > Vth$, the channel is formed and the electrons of 2DEG are free to move (see figure 7b).

As the Vds is increased, the electrons can flow from source to drain giving rise to a current.

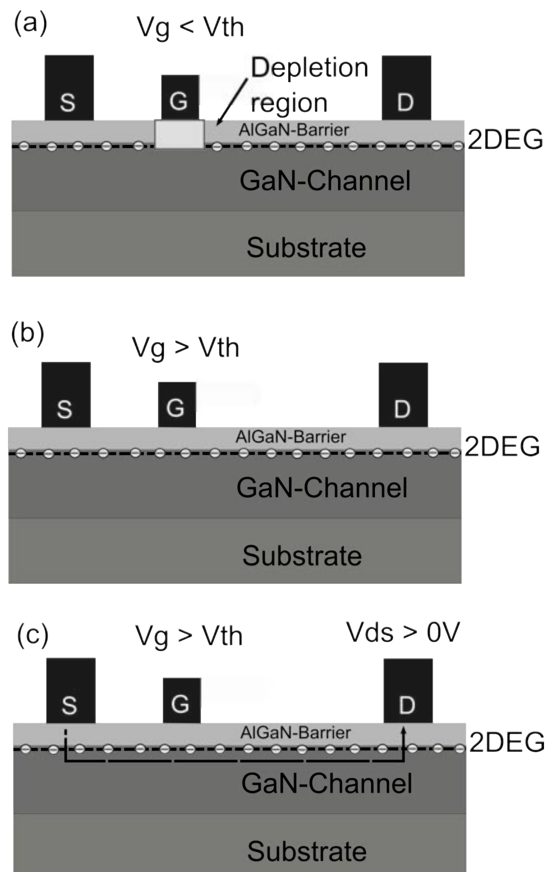


Figure 7: HEMT working principles.

In [21], a compact analytical model using charge control performance of AlGaN/GaN HEMT is presented. This model takes into account the dependency of trap concentration in the AlGaN, N_T, and the AlGaN barrier thickness d.

The total carrier concentration is given by th sum of the sheet charge concentration of the 2DEG formed $n_s(x)$ and the piezoelectric induced sheet charge concentration $n_{pz}(x)$. It can be expressed by:

$$n(x) = \frac{\epsilon_a}{qd}(Vgs - V_{offeff} - V_c(x)) \tag{9}$$

where

$$V_{offeff} = \Phi(m) - \Delta E_c(m) - \frac{q(N_d - N_T)d^2}{2\epsilon_a(m)} - \frac{\sigma_{pz}(m)d}{\epsilon_a(m)}3 \tag{10}$$

where m is the Al mole fraction, $\epsilon_a(m)$ is the AlGaN dielectric constant, $V_c(x)$ is the channel potential at x due to the drain voltage, d is the AlGaN thickness, Δd is the effective thickness of the 2DEG,$\sigma_{pz}(m)$ is the polarization induced sheet charge density, q and

Finally the drain to source punctual current I_{ds} is

$$I_{ds}(x) = zqv_d(x)n(x) \tag{11}$$

where z is the gate width. Integrating the latter from drain to source we obtain for the linear region [39] [50]:

$$I_{ds} = \frac{\mu z \epsilon_a}{Ld}\left[(v_{gs} - V_{offeff})V_{ds} - V_{ds}^2/2\right] \tag{12}$$

when the electric field in the channel reaches the critical saturation value, the velocity of carriers is saturated and the drain current is expressed by:

$$I_{ds} = qzv_{sat}n_s = \frac{\epsilon_a z v_{sat}}{d}(V_{gs} - V_{offeff} - V_{DSS}) \tag{13}$$

where V_{DSS} is the saturation drain velocity.

3 In modern devices, the employement of doping in AlGaN is not necessary because the charge induced by piezoelectric effect is still enough. Therefore the term with N_d is only dependent on N_T.

1.3 TECHNOLOGICAL FEATURES

A double heterostructure AlGaN/GaN HEMT is composed by:

- substrate and nucleation layer;
- AlGaN back-barrier;
- GaN channel;
- AlGaN barrier;
- ohmic and Schottky contacts;
- superficial passivation;
- Metal-Semiconductor or Metal-Insulator-Semiconductor structure below the gate contact.

In the following each section will be presented.

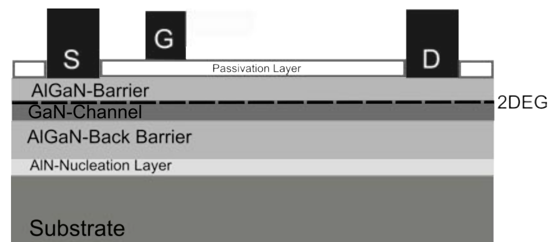


Figure 8: Section of a double heterostructure HEMT.

1.3.1 Substrates

If the active region of Si-based devices can be grown on Silicon bulk substrate, GaN-based devices require foreign substrate. Indeed, the growth of the active region on a GaN-substrate is unfauvorable due to the unacceptable costs and limited size (3-in).

Possible bulk substrates

Possible substrate materials are: sapphire (Al_2O_3), Silicon-Carbide (SiC) and Silicon (Si).

Historically, the first employed substrate was the sapphire, thanks to its mechanical and thermal stability and low cost fabrication. Unfortunately, it is not suitable for power devices because of its low thermal conductivity and defects.

SiC-substrates present the best characteristics in terms of low lattice and thermal mismatch with GaN, and high thermal conductivity. Nevertheless, small wafer size and very high production costs makes SiC unsuitable for mass-market[4].

Silicon substrate

A good compromise between costs and thermal and electrical properties is the choice of Si(111) substrate grown on large diameter wafer (up to 200mm)[36].

If GaN was grown directly on Si wafer, the interface would be full of defects due to the large crystal mismatch and different thermal expansion coefficient. This problem decreases the device breakdown voltage and facilitates vertical and horizontal leakage current because of active trapped carriers in leakage paths and defects[63] at the interface. Oxygen, Silicon and Carbon are the main impurities: the first two act like a n-type dopants, the latter as p-type dopant[5] [63]. Epilayer cracking and Si-wafer bowing are other results of this choice[32] [28].

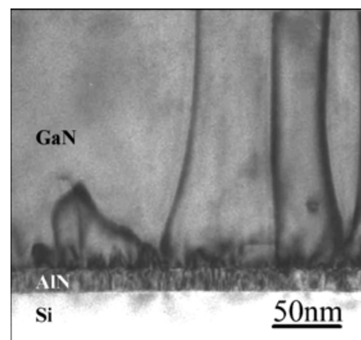


Figure 9: TEM image of GaN films grown on Si (111), where we notice the dislocations in the first layer above the AlN [28].

4 Sic substrate are largelly employed as microwave amplifier for space, defense and telecommunication applications.

5 Sometimes Carbon is intentionally introduced to compensate the unintentional shallow donors present in the GaN layer in order to render more insulating.

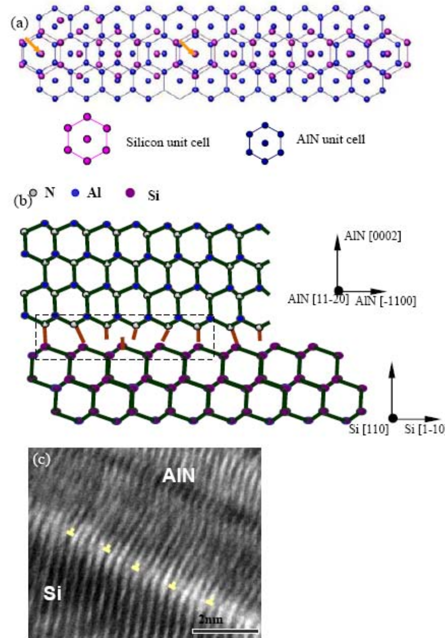


Figure 10: (a) Projection of the bulk basal plane of (111) where we can see silicon and the AlN dislocation positions for the observed epitaxial growth orientation. Arrows indicate the coincidence of the AlN atoms with silicon (111) atoms.
(b) A ball-and-stick-model of the atomic arrangement of AlN and silicon, viewed along the AlN [11$_2$0] and Si [110] directions. Corresponding to figure 10(a), misfit dislocations were introduced to relax the misfit strain between coincidence sites.
(c) Cross-sectional high resolution TEM at the interface AlN/Si. Misfit dislocations are indicated in the images.[18]

AlN nucleation layer

A solution is to grow an intermediate layer of Aluminium Nitride (AlN) between Silicon and GaN buffer. This lowers the vertical leakage current and allows a better GaN growth.

AlN is an alloy of GaN (such as AlGaN) and exhibits a wide band-gap ($E_g = 6.2eV$). Despite these improvements, the Si/AlN interface presents defects, and lots of dislocations starting from the nucleation layer and propagating through the HEMT structure [63].

This allows to create an horizontal and vertical current path. Figure 9 depicts that GaN layers close to the interface present a poor quality. Here, an amorphous SiN_X layer can form at the AlN-Si interface. This fact degrades further the quality of GaN films [18]. The solution of the formation of this parasitic layer,

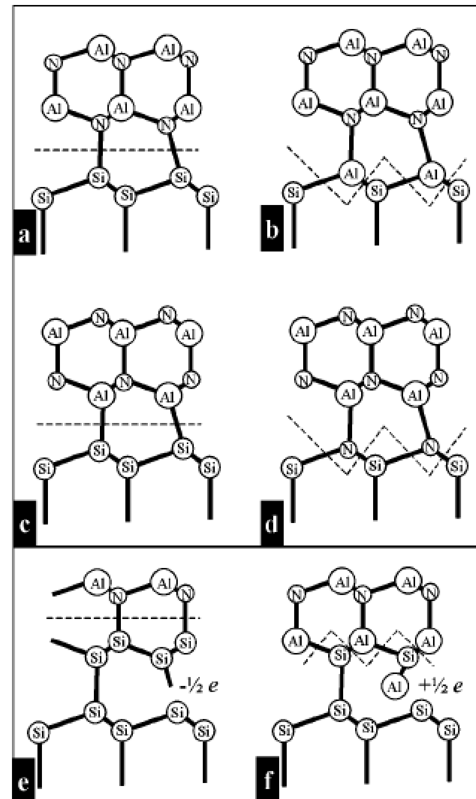


Figure 11: (a)-(d) Schematics of four possible bonding configurations at the Al/Si interface; (e) and (f) two models of the misfit dislocation structure for a charge-neutralized interface[28].

is to deposit an Al film on the Si surface before the deposition of AlN [28].

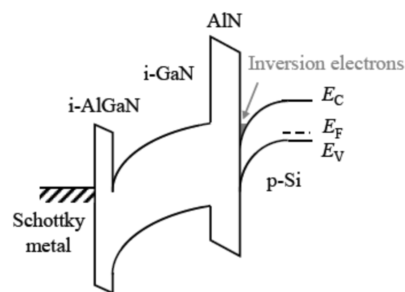


Figure 12: Band diagram from the Si-substrate to Schottky gate contact, where we can see the parasitic inversion electrons channel formed at AlN/Si interface. Taken from [53].

As shown in figure 12, there is a parasitic channel at the AlN/Si interface, therefore a possible leakage path. The solutiton

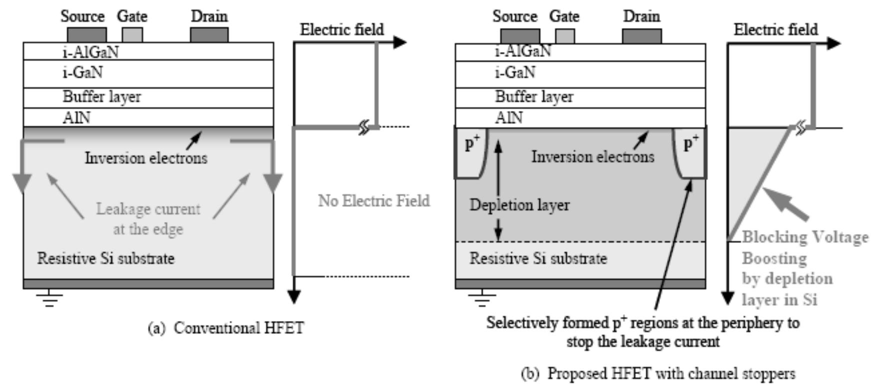


Figure 13: Section of a conventional HEMT in (a) and the new one proposed with channel stoppers. Taken from [53].

to this problem was proposed by Umeda et al. in [53] and it shown in 13: the addition of a ion implantation region at the peripheral area of the chip as channel stoppers to terminate the leakage current from the interfacial inversion layers at AlN/Si. A depletion layer widens in the substrate by the help of the channel stopper, which increases the blocking voltage of the HEMT.

1.3.2 Contacts

Ohmic and rectifying contacts

The metal-semiconductor junction is the base for HEMT contacts. There are two types of contacts: the ohmic contacts and the rectyfing contacts (also named Schottky contacts). Schottky contacts are employed at gate, instead ohmic contacts at source and drain. Indeed, source and drain request a low resistivity to reduce the voltage drop; on the other hand, the gate contact requires a barrier to control the flow of 2DEG electrons and to lower the reverse current.

1.3.3 Ohmic contacts

Typically, the material stack employed at ohmic contact is formed by: Ni/Au, Ti/Al/Ni/Au, W/Ti/Al or Ti/Al/Ti/Au.

These metals have a low work function Φ:$\Phi_{Ni} = 5.24eV$, $\Phi_{Ti} = 4.10eV$, $\Phi_{Au} = 5.10eV$, $\Phi_{Al} = 4.28eV$ and $\Phi_{W} = 4.55eV$.

An Au-free metalization process was developed at IMEC [54] on a $15mm$ GaN-on-Si substrate:

- to make GaN process compatible with a CMOS process,
- to avoid the Silicon contamination in GaN-on-Si technology.

This kind of process can be run in a standard CMOS factory, which reduces the cost.

1.3.4 Gate contact

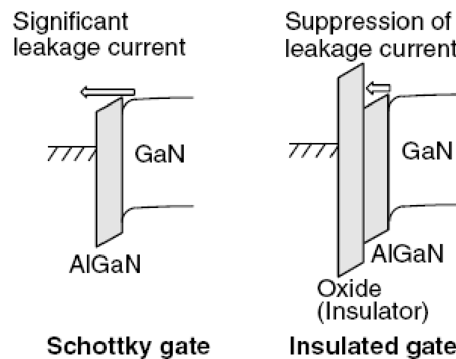


Figure 14: Band diagram of Schottky and Insulated gate in on-state[38].

The leakage current at gate contact is one of the most critical problem in Schottky gate HEMTs for power device applications. Despite of the potential barrier at junction, there is a reverse current that flows, as well as a power dissipation, which are possible sources of failure for devices.

We are going to present some conduction mechanism that explains the behaviour in forward and reverse bias. Such model mechanism is referred to a precise working condition and may or not take into account:

- gate voltage V,
- temperature T,

- potential barrier height Φ_B,
- potential trap height Φ_t.

Schottky gate

Thermionic field emission model

The forward Schottky gate behaviour in function of temperature and electric field is well described by thermionic field emission model (TFE) [50] :

$$J_{MSforward} = J_{sf} \left(\exp\left(\frac{qV}{n_f kT} \right) - 1 \right) \tag{14}$$

where

$$J_{sf} = A^* T^2 \left(-\exp\left(\frac{q\Phi_B}{kT} \right) \right) \tag{15}$$

$$n_f = \frac{E_{00}}{kT} \coth\left(\frac{E_{00}}{kT} \right) \tag{16}$$

$$E_{00} = \frac{h}{2} \sqrt{\frac{N_D}{m^* \varepsilon_S \varepsilon_0}} \tag{17}$$

and A^* is the Richarson constant, k is the Boltzmann constant m^* is the effective mass N_D is the donor density.

Electrons can pass through the barrier by means of thermal energy as well as tunneling[50].

To explain the reverse behavior of gate contact many models are employed and developed.

Thin surface barrier model

The first model considered is developed by Hashizume et al. in [10]. They proposed the thin surface barrier model (TSB) that previews an unitentional surface-defect donors that, in turn, enhances the tunneling transport processes. The surface-defect donors originates from Nitrogen vacancies V_N[10].

The TSB current density formula is more complex than the TFE because introduces the tunneling probability $T(E_x)$[6] for the normal component to the Schottky barrier:

$$T(E_x) = \exp\left(-2\frac{\sqrt{2m^*}}{\hbar} \int_{x_1}^{x_2} \sqrt{\Phi(x) - E_x}\, dx \right) \tag{18}$$

6 The tunneling probability was calculated by means of Wentzel-Kramers-Brillouin approximation.

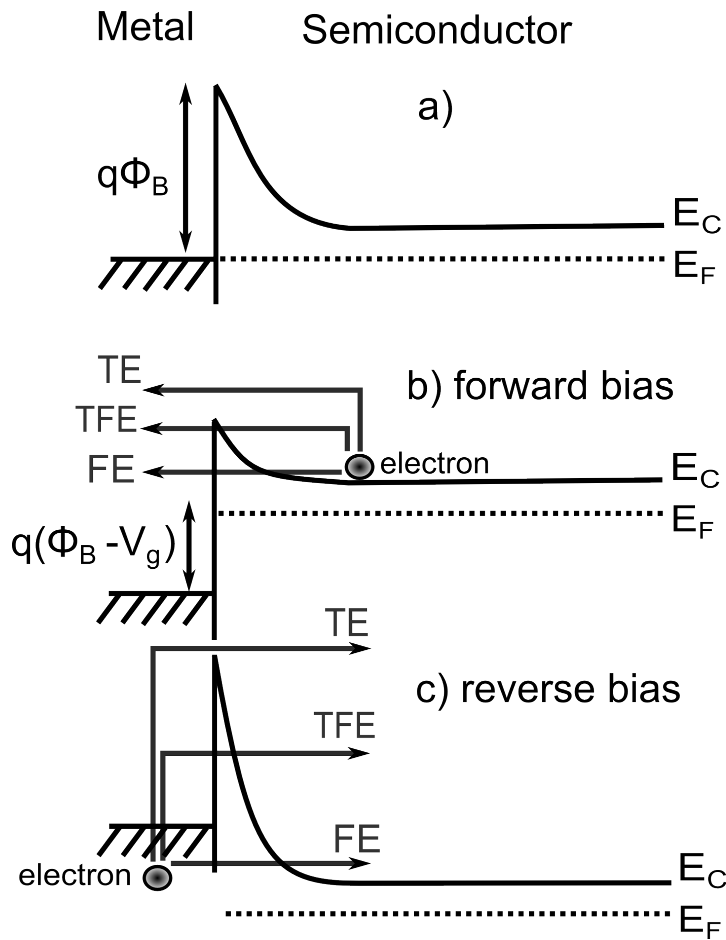


Figure 15: Thermionic field emission process[50]: a) at zero voltage applied, b) at forward bias, c)reverse bias. We can note that in reverse bias eletrons come from the metal.

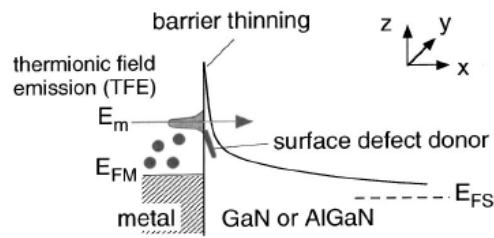


Figure 16: Thin surface model[10].

and the density of current from semiconductor to metal through the Schottky barrier:

$$J_{MSreverseTSB} = \frac{4\pi q m^*}{h^3} \int_0^\infty T(E_x) \int_0^\infty (f_s(E_p + E_x) - f_m(E_p + E_x))\, dE_p dE_x \tag{19}$$

where $f_s(E)$ and $f_m(E)$ are the Fermi-Dirac distribution function for semiconductor and metal. In figrure 16 a gaussian function E_m is presented. Since equation (18) is an exponentially increasing function and $f(E)$ are exponentially decreasing functions with E, the integrand in equation (19) forms a Gaussian peak for tunneling at E_m at a certain energy whose energy position is temperature dependent.

Trapped-assisted-tunneling and thermionic-trapped-assisted-tunneling

The trap-assisted-tunneling (TAT) model and the thermionic-trapped-assisted-tunneling (TTT or TTAT, see figure 17) involve tunneling through triangular barrier favoured by trap located in the semiconductor and consider also the image force lowering and quantum barrier lowering[7].

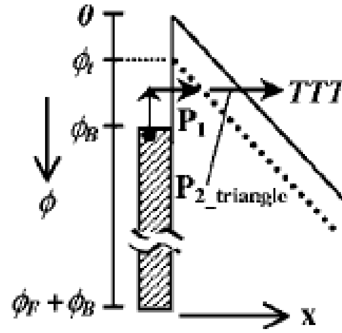


Figure 17: Thermionic trapped assisted tunneling[31].

Metal-Insulator-Semiconductor structure

The main reason to introduce a MIS structure at gate of power HEMTs is to reduce the reverse gate leakage current and power dissipation in off-state bias. The main disadvantages are the high defects located at the interfaces and inside the insulator. This is due to the non-crystalline structure of the insulators that can trap charge as well as the *ex situ* growth process[59].

7 The image-force lowering is the image-force-induced lowering of the barrier energy for charge carrier emission, in the presence of an electric field.

Between the gate metal contact and the AlGaN barrier, a thin insulating film is intentionally deposited. This insulator can be composed by different material layers, e.g. Si_3N_4 and Al_2O_3 to effectively reduce the gate leakage current. Generally, the insulator materials employed in MIS-HEMTs are : HfO_2, Al_2O_3, Si_3N_4, Ga_2O_3[38] (see figure 18). Al_2O_3, is a good comprmise between wide energy gap($E_g = 6-8eV$), high dielectric constant($\epsilon = 6-8$) and high breakdown field ($\geqslant 10MV/cm$)[38].

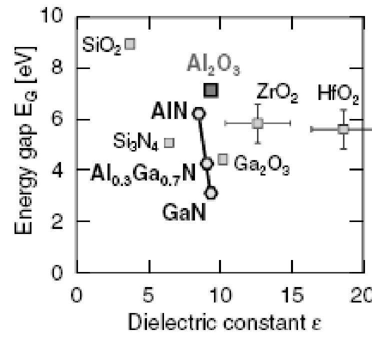


Figure 18: Dielectric constants and energy gaps of insulators and GaN compound. Taken from [38].

The first conduction mechanism presented is the Poole-Frenkel mechanism that takes into account the surface trapping paths and the vertical paths in insulator layers[8] to drain or source [7], [8], [50]. The process to free trapped charge overcoming the Φ_t trap potential well is favoured by thermal energy and high electric field. Since the high field applied bends the energy band diagram, the necessary thermal energy is lower.

Poole-Frenkel mechanism

The following formula expresses the Poole-Frenkel current:

$$J_{MISreversePF} = C\frac{V}{d} \exp\left(\frac{q}{kT}(2a\sqrt{V} - \Phi_B)\right) \tag{20}$$

$$a = \sqrt{\frac{q}{4\pi\varepsilon_i d}}$$

where C is a coefficient and d is the thickness of insulator[50].

Also tunneling is possible in the insulator material. As in

Tunneling

8 This mechanism is also suitable in AlGaN/GaN metal-semiconductor junction if the AlGaN barrier is considered as the insulator beacause of its wider band-gap.

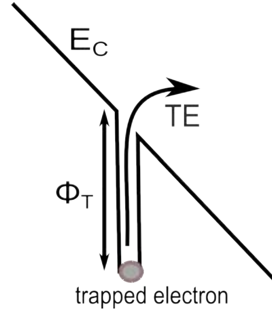


Figure 19: Poole-Frenkel emission model. The conduction energy band E_C is bended due to high electric field applied. This mechanism can occur in AlGaN barrier or at the interface between gate and AlGaN barrier.

metal-semiconductor junction, tunneling is strongly dependent on electric field that bends the energy bands [9]

Fowler-Nordheim Tunneling

Two possible situations can occur and are shown in figure 20. The Fowler-Nordheim tunneling is a particular case of tunneling, since carriers pass through the insulator triangular barrier because of the band bending. As in tunneling conduction, Fowler-Nordheim tunneling presents strong electric field dependece and weak temperature dependence:

$$J_{MISreverseFN} = \frac{q^2}{16\pi^2\hbar\phi_{ox}} E^2 \exp\left(\frac{-4\sqrt{2m^*}(q\phi_{ox})^{3/2}}{3\hbar q E}\right) \quad (21)$$

where $\phi_{ox} = Ed$ with d as the oxyde thickness and E electric field [50].

Hopping mechanism

At high temperature and low voltage, current can be generated by electrons, thermally excited, which hop from one isolated state to the next. This the hopping carrier transport that show a density current behaviour given by:

$$J_{Hopping} \propto V \exp\left(-\frac{c}{T}\right) \quad (22)$$

where c is a constant [50].

As reported in figure 21, in MIS structures at high temperatures and high electric fields the dominant current may be described by Poole-Frenkel mechanism; if there is no appre-

9 The energy gap E_g is sensitive to temperature, as can be calculated by 7.

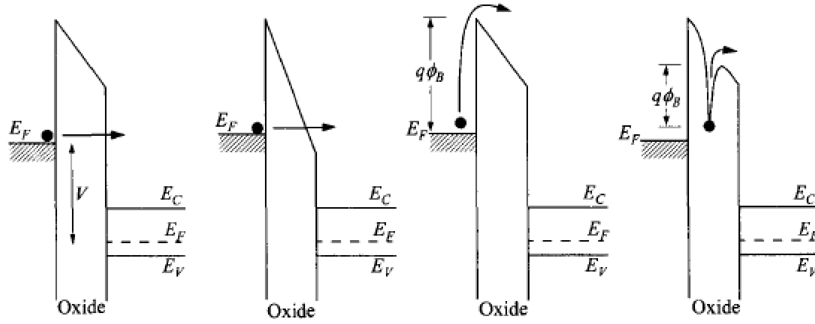


Figure 20: Energy band diagrams showing the conduction mechanism in a MIS structure. a) direct tunneling; b) Fowler-Nordheim tunneling through a triangle barrier; c) thermionic emission; d) Poole-Frenkel emission. Taken from [50].

ciable current variation in function of temperature a tunneling mechanism may be considered. At intermediate condition, the current may follow the Poole-Frenkel description.

1.3.5 Field plate

In power AlGaN/GaN HEMTs working conditions, drain contact could be at very high voltage, as in pinch-off condition, and induces a critical high electric field peak at the drain edge of the gate contact.

This can be avoided by the growth of a metal plate that covers a part of the gate-drain region and offers an additional edge for the electrical field lines to terminate at higher drain bias (see figure 22). The electric field peak extend both horizontally along the channel and vertically at the gate edge.

Some brief considerations can be done in order to better understand the field plate use and design choises of insulator or passivation thickness t_i and field plate length l_{FP}[10]. A too large l_{PF} reduces the device pulse performances because of the higher gate capacitance. On the hand, a too short l_{FP} nullify the benefits and does not spread the critical electric field. Concerning on the t_i, a too high t_i means a too far field plate, therefore

10 More detailed design tecniques are reported in [17] and [16].

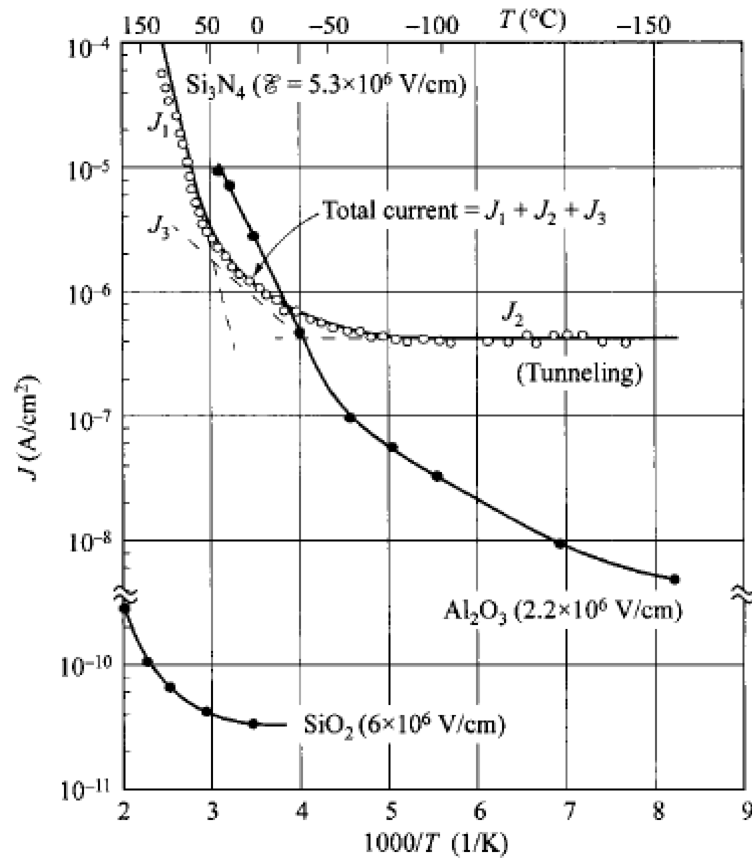


Figure 21: Current density comparison from insulator films: Si_3N_4, Al_2O_3 and SiO_2. In Si_3N_4 curve, J_1 indicates the Poole-Frenkel mechanisms, J_2 the tunneling mechanism and J_3 the hopping mechanism. Taken from [50].

there is no influence on the electric field a the surface. Instead too much close to the surface, it simply moves the electric peak because it seems a larger gate.

For the reasons explicated above, the employement of this technique leads to:

- reshape the maximum peak of electric field,
- increasing breakdown voltage,
- reducing current collapse,

and it is usually employed.

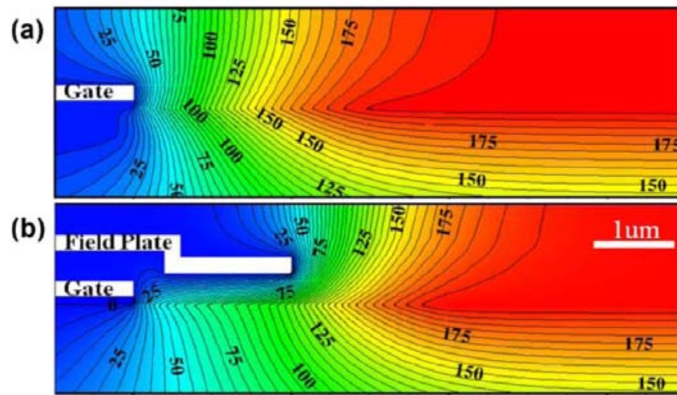


Figure 22: Simulation of electrostatic potential distribution (in [V]) (a) without and (b) with field plate at $V_g = 0V$ and $V_d = 200V$. Taken from [11].

1.3.6 In-situ passivation

We have just seen the critical role of the AlGaN surface charge in the 2DEG formation and its quality.

Recently, IMEC has developed a technique to passivate devices in order to preserve the surface charge and to avoid the virtual gate formation and strain relaxation.

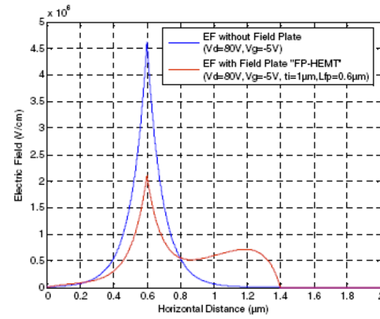
Without the in-situ passivation layer, the wafer surface is subject to air pollution and contaminants that affects the device performance because of the lower n_s.

A thin film of Si_3N_4 is deposited in-situ, that is, directly in the same molecular organic chemical vapour deposition reactor (MOCVD reactor) where is grown [55].

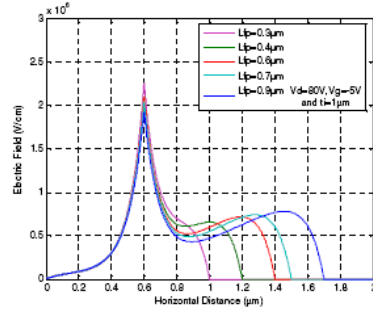
1.4 TRAPS AND PARASITIC EFFECTS

GaN HEMT technology is one pf the promising technology for the next future power switches but is still affected by performance losses related to the presence of traps. The study of these phenomena can improve the state-of-the-art processing and technology [6].

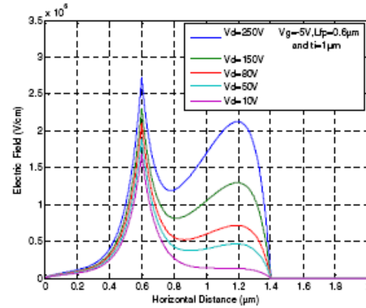
The next discussion will be focused on traps and parasitic effects of the AlGaN/GaN HEMTs in general, but a particular at-



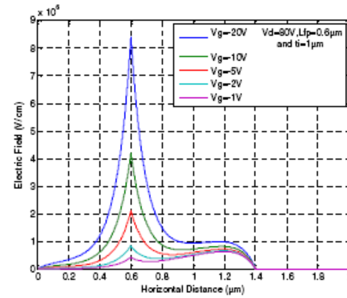
(a) Electric field distribution along the 2DEG with and without field plate.



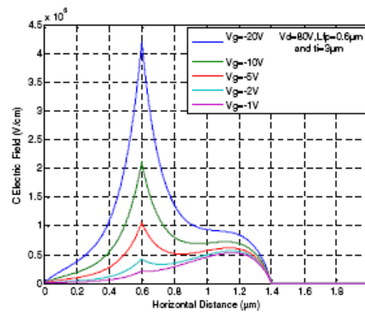
(b) Electric field along the 2DEG channel for various field plate lengths.



(c) Electric field along the 2DEG channel at different drain voltages.



(d) Electric field along the 2DEG channel for various gate voltage at insulator thickness $t_i = 1\mu m$.



(e) Electric field along the 2DEG channel for various gate voltage at insulator thickness $t_i = 3\mu m$.

Figure 23: Simulation taken from [15], which show the different electric field distribution in function of bias point and design parameters.

tention will be payed on the structure of the devices employed to develop this thesis work.

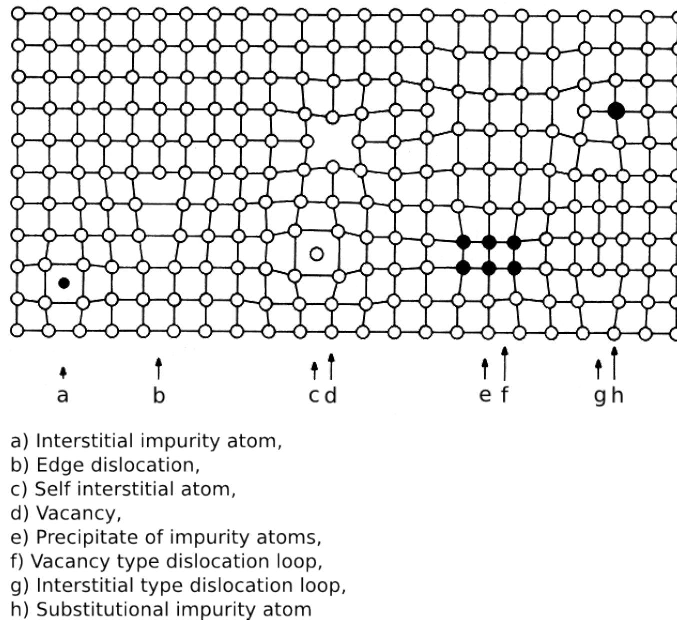


Figure 24: Pictorial view of defects in a semiconductor. Taken from [65].

To understand how a trap acts, it is useful to explain what are the generation and recombination mechanisms in a semiconductor.

A generation-recombination center is a state located in the bandgap of the semiconductor which simmetrically acts as generation and recombination center. Indeed it presents the capture cross section for electron σ_n equals to the capture cross section for hole σ_p[11].

A normal recombination process of a carrier considers a full transition between the conduction band to valence band, but this is not the unique.

A trap state is an unintentionally state that causes unwanted carrier captures and emissions. It is related to defects in the material such as dislocations, foreign interstitials, vacancies, foreign substitutionals, self interstitials, stacking faults, edge dislocations, volume defects and impurities (see figure 24).

Generation and recombination processes

The trapping phenomenon originates from the behaviour of a generation-recombination center which favours the capture of electrons or the capture of holes.

11 A deeper explanation of the topic can be found in [40] on the basis of [47].

Conversely, if a carrier is captured in a trap state, an external energy is required to emit it, this can be achieved applying a thermal energy or an exposion to light [56][12] with $\Delta E \geqslant E_a$.

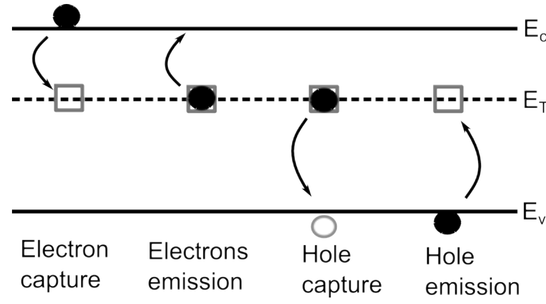


Figure 25: Pictorial view of Shockley-Read-Hall capture and emission of carriers through a trap level E_T in the semiconductor bandgap.

Through physical and Fermi-Dirac statistics considerations we can calculate the emission rate for electrons e_n and for holes e_p as:

$$e_n = \frac{1}{e_n} = N_C v_{th} \sigma_n \exp \frac{E_t - E_c}{kT} \tag{23}$$

$$e_p = \frac{1}{e_p} = N_V v_{th} \sigma_p \exp \frac{E_v - E_t}{kT} \tag{24}$$

here E_T, v_{th} and N_C are the state energy, the electron thermal velocity and the density of states at the conduction band. The strength of the SHR process depends on the position in the band gap ($E_c - E_t$ and $E_t - E_v$) and parameter of the trap state called capture cross section foe electrons σ_n and holes σ_p.

The lifetime constant of electron emission τ_n and holes emission τ_p from states is given by SHR statistics as:

$$\tau_n = \frac{1}{N_C v_{th} \sigma_n} \exp \left(\frac{E_T}{kT} \right) \tag{25}$$

$$\tau_p = \frac{1}{N_V v_{th} \sigma_p} \exp \left(\frac{E_T}{kT} \right); \tag{26}$$

12 The exposure to light is a very useful detrapping process employed during measurements to discharge traps and restores currents to the beginning values. It furnishes also a valuation of the energy associated to traps if the light energy is known.

the deeper is the trap, the longer could be the lifetime constant associated.

The model of a trap in the energy band diagram is shown in figure 26.

Therefore to characterise a trap is neccessary to know:

- charge state,
- activation or ionization energy E_a,
- capture cross section σ [6].

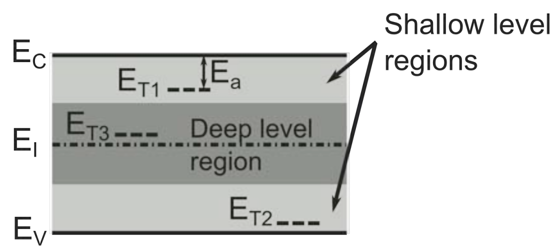


Figure 26: The band diagram shows how to model a trap level at different energies: E_{T3} is a trap level located in the deep level region, E_{T1} and E_{T2} are located in the shallow level region. We see also the activation energy E_a defined as $E_a = E - E_T$ where E is the closer band among the conduction band E_C or valence band E_V to E_T. It indicates the energy to supply to emit the carrier.

Trapping phenomena represent parasitic effects which affect the device performances. The main effects in power AlGaN/-GaN HEMTs are the R_{on} collapse (also named drain current I_d collapse or virtual gate) and the threshold voltage shift. Each effect is strictly related to the affected region as can be pictorially shown in figure 27.

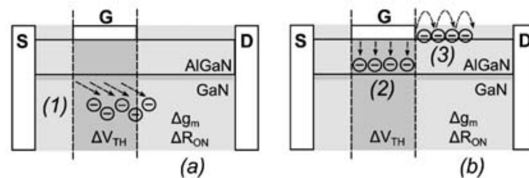


Figure 27: Pictorial view of trapping mechanisms in function of bias for the (a) semi on-state and the (b) off-state. Taken from [3].

Virtual gate, R_{on} *and* I_d *collpase*

The concept of virtual gate was developed by [56] to explain the drain current collapse due to surface trap states (see figures 28 and 29). Thanks to spontaneous and piezoelectric polarization and consequent 2DEG formation, a positive sheet charge of ionized states exists at the interface between gate and AlGaN barrier. Through measurements, it was noticed that the output current value was below the previewed. This lacking current might be due to negative charged trapped located in the surface region between drain and gate contacts. The negative charge acts like a negatively biased metal gate, its potential is not controlled directly by the applied gate bias. The potential at virtual gate is controlled by the total amount of trapped charge in the gate-drain surface region which in turn provokes the Ron collapse. A solution to prevent the virtual gate, is the superficial passivation by Silicon-Nitride SiN that buries the surface donor state and makes them inacessible to electron leaking from the gate metal[56]. This phenomenon does not allow to device to operate at high frequency gate voltage, and this impacts to device RF performances. Indeed at the gate signal commutation OFF-ON to close the channel and to allow the electrons to flow from source to drain, the charges in the depleted region do not follow the signal at gate because they are not directly controlled. The time to detrapping is longer and can be estimated by a transient measurement (see figure 30.

RF effects of virtual gate

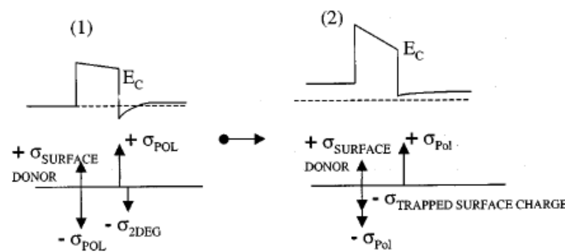


Figure 28: Band diagrams showing the impact of virtual gate. In situation(1), the 2DEG is formed and there is no virtual gate. In (2) we can see the absence of formation of 2DEG due to negative charge traps[56].

The R_{on} collapse can be monitored through transients measurements and Double-Pulse measurements[13]. The explication of this effect is reported in [36] and [3]. R_{on} collapse is due to the accumulation of electrons in the gate-drain region and increases with increasing L_{GD}. The trapped electrons in the gate-drain region may come from:

- the gate (in gate forward bias), so they are trapped in the passivation layer or in the surface defects during the hopping transport mechanism or
- from the channel to the AlGaN/GaN heterostructure (hot electrons).

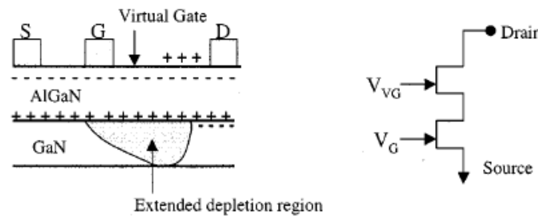


Figure 29: Effect of the virtual gate that induces a depleted region in the device[56]. If some electrons which originate the 2DEG are trapped at surface, the superface traps remain neutrally charged and the density of electrons in 2DEG is lower. An unwanted depletion region under the neutrally chaerged traps is formed. Because of the presence of the depletion region, the 2DEG is not connected, this causes a lower drain current and its difficulty to flow.

Threshold voltage shift

The other trapping phenomenon is the threshold voltage shift. This is due to the negative traps located under the gate region [3] which affect the threshold voltage and can lead to undesired effect to the device state. This phenomenon can be stimulated by applying a forward bias at gate contact in order to fill the traps as shown in figure 31. The choice of gate structure influences the extension of the trapped region under the gate: in a Schottky gate carrier may be trapped in the whole region under

13 The device is biased at certain quiescent bias point, usually with very negative gate voltage and high drain voltage, between a point and the consequent of the $I_D V_D$ curve. The measurement setup will be explained in the following chapters.

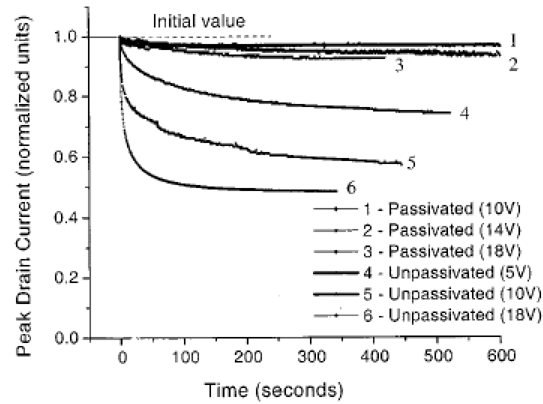


Figure 30: Effect of passivation layer on the transient measurments. A reduction of current collapse can be clearly noticed[56].

the gate, instead in MIS gate the region involved is smaller and may affects only the AlGaN barrier.

Location of traps in MIS-HEMT

In an AlGaN/GaN MIS-HEMTs, traps are located:

- at the interfaces between metal gate contact and insulator,
- at the interface between insulator and AlGaN barrier,
- at the interface between AlGaN barrier and GaN buffer,
- at the interface between AlGaN back-barrier and nucleation layer,
- at the interface between nucleation layer and Si-substrate,
- in GaN buffer layer and in the substrate.

We have to underline that the insulator under the gate contact and the AlN of nucleation layer are not crystalline materials so they have a high density of traps.

Therefore is very important to characterise these traps through specific measurements, such as: interface state density distribution D_{it} and concentration N_{it} employing a combination of standard and photo-assisted $C - V$ measurements [24], [38], [9]; I-DLTS in on-state bias [23], [24], [25]; conductance $G/\omega - V$ [59], [38].

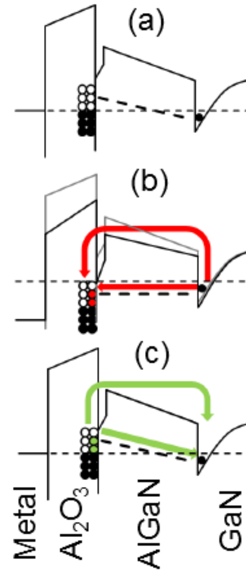


Figure 31: Traps at thermal equilibrium where all electrons below the Fermi level are filled (a), in forward bias during stress (b) and in reverse bias during recovery(c). The filled circles indicate the filled traps. Taken from [24].

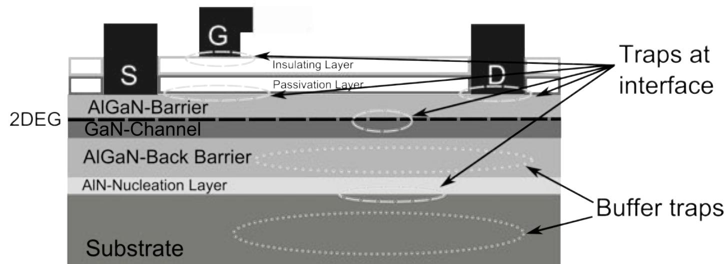
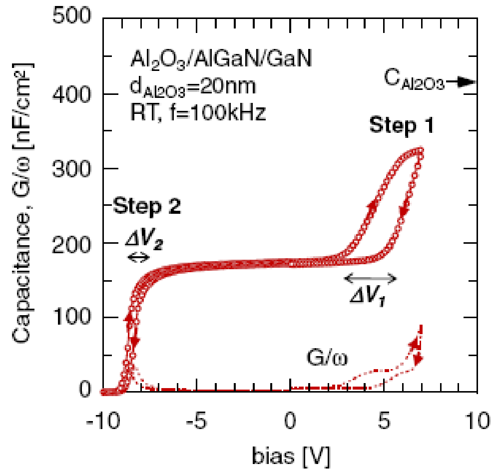


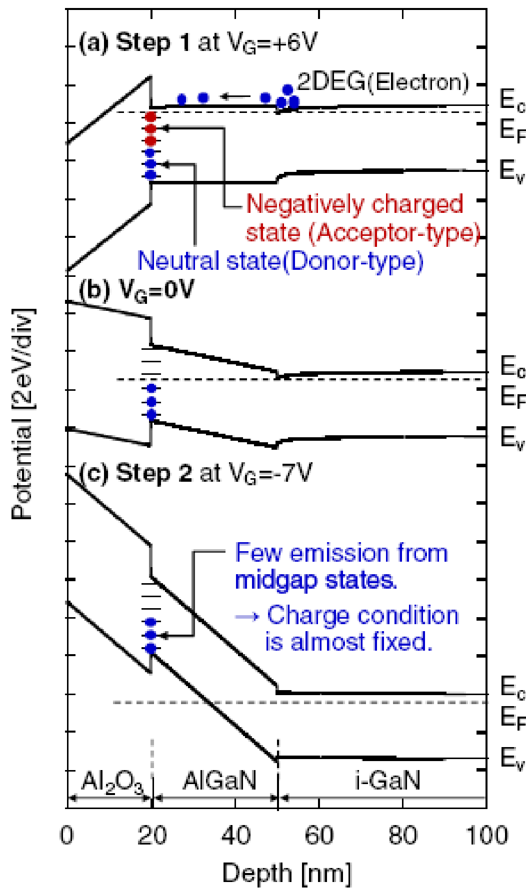
Figure 32: Possibly main location of traps in employed MIS-HEMTs.

Through a $C-V$ measurements, V_g sweep we can investigate the traps behaviour and estimate the emission time τ but not all traps can be uncharged as reported in [9].

In figure 33, the $C-V$ plot and the band diagrams at the main gate voltages are shown. In the $C-V$ measurement in the left side, between $-7V$ and $2V$ we note a constant capacitance corresponding to the series capacitance of Al_2O_3; at $-9V$ a step decrease is observed indicating the complete depletation of 2DEG; at $+3V$ instead, a steplike increase in capacitance occurs (step 1), here the electrons go to $Al_2O_3/AlGaN$ interface from 2DEG and there may be a high possibility of trapping



(a) $C - V$ and $G/\omega - V$ characteristics.



(b) Band diagram with $D_{it1}(E)$ corresponding to (a) step 1, (b) zero-bias applied, and (c) step 2.

Figure 33: Analysis of $C - V$ measurements of a $20nm - Al_2O_3/AlGaN/GaN$ diode. Taken from [38].

them at the interface. The hysteresis is consistent only in forward bias and it is due to the acceptor-type interface states (by the simulation shown in this article, there would not be the hysteresis without the introduction of interface states). As reported in the figure 33b at the top, thanks to the proximity of the Fermi level to conduction band at the $Al_2O_3/AlGaN$, the upper part of the acceptor-type interface states can be filled with electrons. The main consequence is to produce a high density of negatively charged interface states which can be estimated through the knowledge of Al_2O_3, the variation of energy (difference between two Fermi levels at the interface) and voltage of the hysteresis [38]:

$$D_{it}(E) = \frac{C_{Al_2O_3} \Delta V_1}{q \Delta E}. \quad (27)$$

The employement of a light source which detraps the carriers trapped, helps to estimate D_{it} in the step 2.

The study of traps through focused measurements is the base to improve electronic device performances and to suggest how to eliminate or to lower their effects. These effects are: drain current collapse, R_{on} collapse, leakage currents, aptitude to failure and so on.

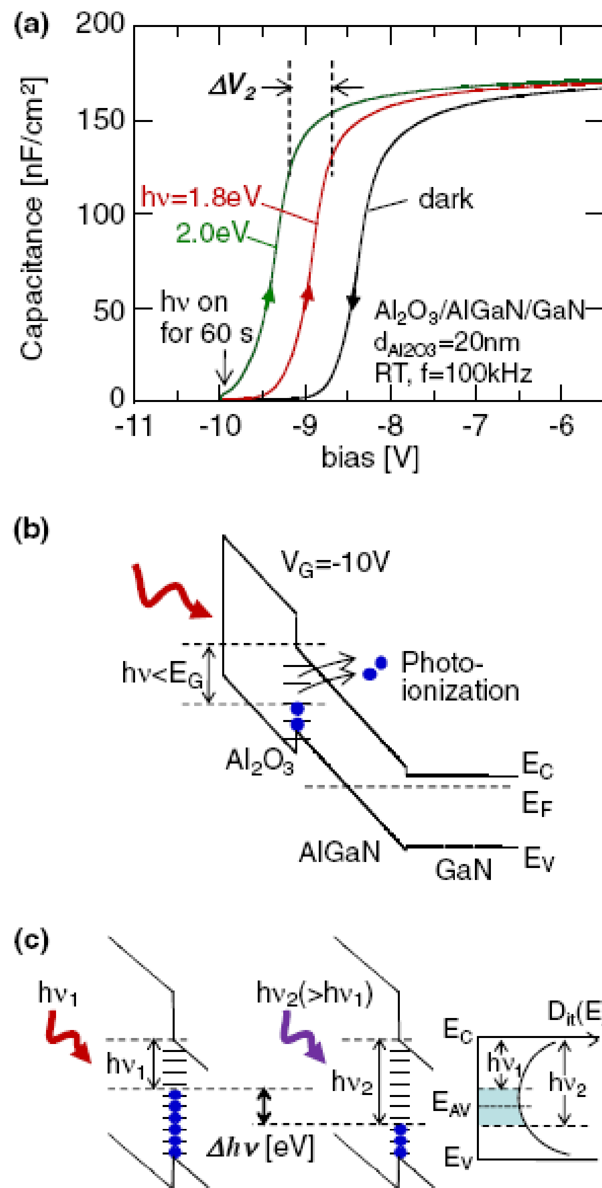


Figure 34: Photo-assisted C-V before and after illumination (a). In (b,c) it is shown the band diagrams of the photo-ionization of interface states under a monocromatic light with photon energy $h\nu$. Taken from [38].

2 CASE STUDY

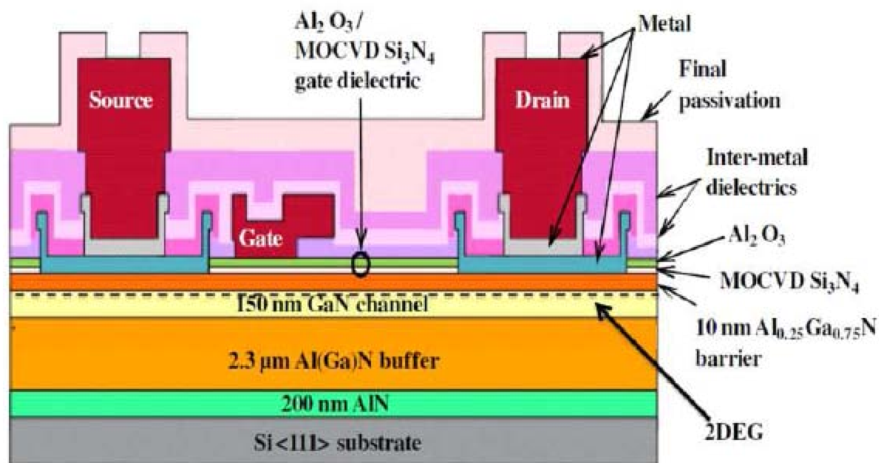


Figure 35: Section of IMEC device, where can be noticed the MIS superficial structure with two layer of Al_2O_3 and Si_3N_4, the passavation layers, the employement of field plate to lower the maximum electric field under the gate region, and the Si-substrate[36].

The devices employed was built by IMEC and the cross section is shown in figure 35.

The main properties of the employed devices are[36]:

- 150mm Si-substrate,
- double heterostructure AlGaN/GaN/AlGaN,
- Metal Insulator Semiconductor gate structure,
- 10nm in-situ grown passivation layer of Si_3N_4.

The double heterostructure is composed by:

- a 2.3μm $Al_{0.18}Ga_{0.82}N$ buffer layer,
- a 150nm GaN channel layer,
- a 10nm $Al_{0.25}Ga_{0.75}N$ barrier layer;

it allows the confinement of electrons in the channel and improve the sustainable maximum breakdown voltage.

The bilayer gate dielectric structure comprises:

- a $10nm$ of Al_2O_3 layer ($E_g = 6.2 - 9.0eV$),
- a $5 - 10nm$ Si_3N_4 layer ($E_g = 4.1 - 5.3eV$).

The metal gate contact consists of a W/Ti/Al stack and includes the field plate with an overhang of $1\mu m$ towards the drain side and $0.5\mu m$ towards the source side.

The geometry of tested devices is

- $L_{gd} = 10\mu m$ and $5\mu m$;
- $W = 200\mu m$;

gate-drain length L_{gd}, the $5\mu m$ and $10\mu m$ L_{gd} devices were employed.

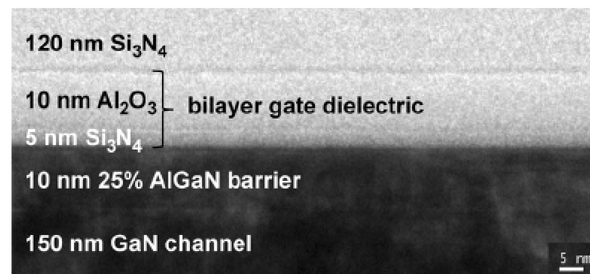


Figure 36: TEM image of bilayer gate dielectric[54].

2.1 DEVICE DESCRIPTION OF IMEC-MP1802 WAFER

The study was carried out at the Microelectronic Lab of the University of Padua on a wafer built on Si-substrate supplied by IMEC. The wafer includes five identical cells (named A, B, C, D, E), each cell is divided in rough and column and at each position there is a double-finger transistor. The study was limited to cells A,B,C,D to devices with $L_{gd} = 10\mu m$ or $5\mu m$ and

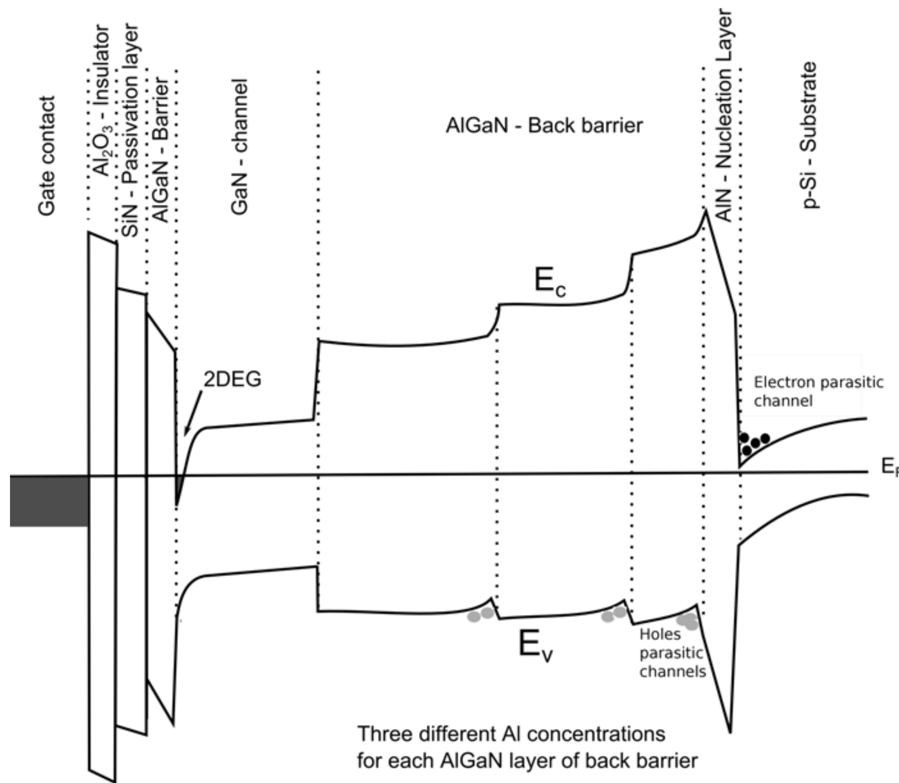


Figure 37: Pictorial band diagram from gate contact to p-Si substrate for an AlGaN/GaN MIS-HEMT with double heterostructure and MIS structure at gate.

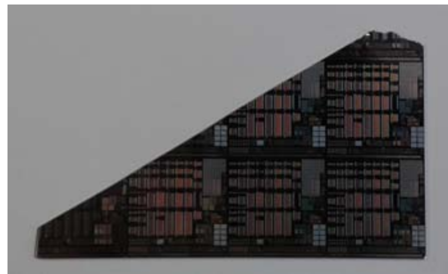


Figure 38: Photo of IMEC-MP1802.

the other parameters equals to those ones reported in table 3 and 4 in order to study the breakdown phenomena until 600V[1]. The employed devices will be indicated at the bottom of each plot and for each the identification codex is

IMEC _ MP1802 _ [cell]_[rough][column] - [notes].

1 A high reverse gate voltage allows to deplete the region under the gate, and raising the bands, it interrupts the channel. The depletion region extends towards the drain side of the gate. So the most important parameter linked to off-state breakdown is the L_{gd}.

Transistor parameters	Length [m]	Notes
L_g	1.5μ	gate width
L_{gg}	100μ	gate to gate spacing
L_{sg}	0.75μ	source to gate spacing
L_{gd}	10μ	gate to drain spacing
L_{fp}	1μ	field plate extension
w_a	100μ	transistor width

Table 3: Typical transistor parameters of IMEC-MP1802 wafer.

Interconnect parameters	Length [m]	Notes
Cell length	500μ	total length of the cell
Cell width	500μ	total width of the cell

Table 4: Interconnect parameters.

3 MEASUREMENT SYSTEMS

In this chapter we want to explain the adopted measurement systems which supply informations on the device behaviour and their relative trapping phenomena in function of bias point, stress conditions, temperature. The considerations extrapolated from data analysis can be employed to improve the device state-of-the-art and give feedback for the future improvements.

Each kind of measurement is necessary to enlight and focus on different aspects and behaviors of HEMTs.

3.1 DC MEASUREMENTS

The aim of DC characterisation is to view steady state device characteristics, which are:

- IdVd curves (also named OUT curves) in function of different V_{gs},
- IdVg curves in function of different V_{ds},
- Gate-Source or Gate-Drain DIODES (also named GS or GD DIODES),
- g_m curves in linear, knee and saturation region;

through these measurements we can extrapolate: the device threshold voltage V_{th}[1], the gate current leakage, transconductance g_m, R_{on} in the linear region of OUT measurements defined as

$$R_{on} = \frac{dI_{ds}}{dV_{ds}}$$

1 The threshold voltage is here defined as the voltage at which the current is $1mA/mm$.

. Furthermore we can compare the devices of the same wafer.

Another very important information, provided from DC characterisation, is the life status of the device or its degradation. Through a simple DIODES curve, for example, we can check the gate status or in addition the threshold shift in function of temperature or the R_{on}.

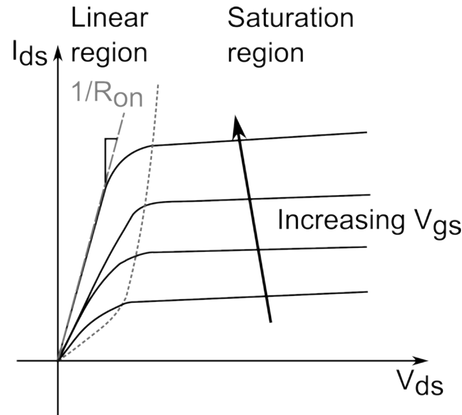


Figure 39: Ron measurements from OUT measurements.

The wafer is placed in a Kurl Suss probe station onto a thermal chuck that brings the device to high temperatures to carry out a study in function of several temperatures. The thermal chuck employment allows to view thermal activated mechanisms and their temperature dependence. They can cover a wide range of temperatures: from room temperature to 200°C.

To contact the device, the tips are mounted on a micrometric manual positioner that moves them in the three spatial directions. We have employed two kind of tips: RF and DC. A DC tip is a single tungsten needle, instead the RF tips are built with three needles and they are suited for RF layout devices. The needles at both sides are normally grounded connected, instead the central brings the signal[2].

Through an optical microscope, we can exactly contact the tips on the device pads and through BNC triaxial cable tips are contacted to the parameter analyzer. Usually only the Agilent Semiconductor Parameter Analyzer E5260A is employed

2 Sometimes DC tips suffer for noise and oscillations. This problem can avoided by mounting ferrite beads and connecting manipulators and thermal chuck to ground.

beacuase it has four *Source Monitor Unit* (SMU) to measure the gate, drain source and bulk voltages and currents, in particular two High Speed and High Power SMUs are reserved for gate and drain measurements and the other two High Speed and Medium Power SMUs for the source and bulk measurements. This is not the only employed parameter analyzer, there is also the B1505A and E5263A

As wrote above, an OUT measurements (from here indicated as OUT) is the measurements of I_{ds} in function of V_{ds} at different V_{gs} through the parameter analyzer. The ranges and voltages are setted through a LabView program which communicates with the instrumentation through a GPIB cable.

3.2 DOUBLE PULSE MEASUREMENTS

The aim of double pulse measurements is the investigation of drain current I_d and R_{on} collapse through voltage pulses applied at gate and drain, and bias stress periods.

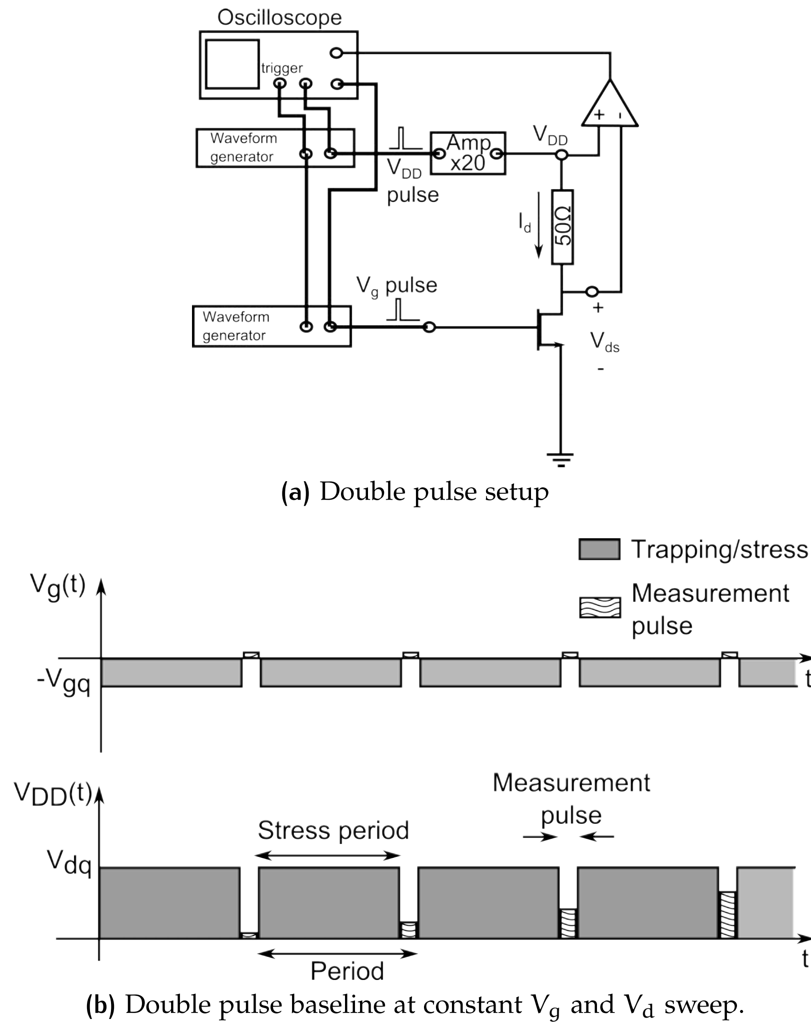
During a double pulse measurements (DP) [4], the device is biased at a certain quiescent bias point (also called baseline) for a setted stress period. After that, the gate voltage and the drain voltage are synchronously pulsed to a different bias value in order to measure the drain current because the HEMT drain is connected to $R_L = 50\Omega$ resistance, therefore the drain current I_d can be measured through:

$$I_d = \frac{V_{DD} - V_{ds}}{R_L} \tag{28}$$

where V_{DD} is the drain pulse width.

An example of quiescent bias point adopted in our DP measurements is $(V_{gq}; V_{dq}) = (-8V; 50V)$ because the channel is opened and electrons are trapped under gate where there is a depletion region, and high drain voltage favours trapping charge in the gate-drain region. During the pulse measurement interval, gate contact is usually forward biased (or $0V$ applied) instead growing voltage is applied at drain. We can say that this

kind of measurements is a sort of OUT but with a bias stress between an OUT point and the next[3]. The period was 100μs and the measurement period 1μs. In figure 40 is reported a schematic setup measurement and how DP is carried out.



(a) Double pulse setup

(b) Double pulse baseline at constant V_g and V_d sweep.

Figure 40: Double pulse measurement. Bulk contact can be both grounded and floating.

3 The DP measurement can be done also monitoring the IdVg curve; so that during the measurement pulse, a constant V_{DD} can be applied and the V_g is increased.

3.3 SUSTAINABLE BREAKDOWN MEASUREMENTS AT CONSTANT VOLTAGE

In these measurements the breakdown phenomena are investigated at a constant voltage at drain or at gate.

The four currents are monitored in order to see which activates the breakdown mechanism. The voltage at which there is a sudden increase of drain current is named breakdown voltage indicated as V_{BD}.

Breakdown voltage

3.4 CURRENT DEEP LEVELS TRANSIENT SPECTROSCOPY

The aim of Current Deep Levels Transient Spectroscopy measurements (I-DLTS) is to observe the dynamical evolution of drain current for a certain time period and the consequent identification of the corresponding deep level and capture rate through the analysis of the trap capture and emission evolution [3]. The choice of monitoring I_d is done because it is directly related to device performance [14].

I-DLTS

As said in [14], the change in the current results from the change in trapping status in the transistor.

Generally the transient measurement consists of two steps:

- a trap filling bias period and
- a drain current detrapping transient measurements.

Generally the trap filling bias period is chosen in order to fill the traps in the region that we want to see in the detrapping transient measurements [3]. For example if we want to evaluate the effects of traps located in the gate-drain region on the drain current in saturation region we will apply $(V_{gf}; V_{df}) = (-8V; 50V)$ during the trapping filling time, and $(V_{gm}; V_{dm}) = (0V; 5V)$ during the detrapping measurement. Instead,for ex-

Choice of detrapping bias

ample, the choice $(V_{gf}; V_{df}) = (-8V; 0V)$ focuses on the region under the gate.

Concerning on the width periods, it depends on the oscilloscope time resolution and/or the parameter analyzer time resolution; a good time window is from $1\mu s$ to 10^2 or $10^3 s$. A single measurement can be realized several times because of the limited time resolution window of the instrument. In this case for each time window, it is previewed the trap filling time and after the detrapping transient.

At different temperatures[4], it provides informations about the activation energy and cross section of the trap levels [35] through the Arrhenius plot.

Arrhenius law

The Arrhenius plot is based on the Arrhenius law which states that the electron emission rate in function of temperature is

$$e_n(T) = \gamma T^2 \sigma_a \exp\left(-\frac{E_a}{kT}\right) \tag{29}$$

and

$$\gamma = 2\sqrt{3} M_c (2\pi)^{\frac{3}{2}} k^2 m^* h^{-3} \tag{30}$$

where σ_a is the capture section[5], k is the Boltzmann's constant, M_c is the number of conduction band minima, h is the Planck's constant and m^* is the effective electron mass of an electron. Therefore to estimate the E_a we have to invert the equation 29 in function of the capture time constant τ_n:

$$\tau_n = \frac{1}{e_n} \tag{31}$$

.

The Arrhenius law can be employed in many other fields where the process is described by an exponential law in function of temperature and is in generally wrote as:

$$x = \sigma_a \exp\left(-\frac{E_a}{kT}\right) \tag{32}$$

4 Generally, by increasing temperature detrapping processes are faster because of the supplied external thermical energy [14].

5 The capture section can be related to the "width" of the trap.

where x is related to rate process and σ_a is the cross section.

To extrapolate the valus of E_a and σ_a we can make an analysis of Id transients at different temperatures and build the Arrhenius plot. Infact the slope of the Arrhenius plot is the activation energy E_a

Now it is very important dealing with the mathematical fitting analysis of the results because, through the latter, it is possible to extrapolate the time constant and the consequent activation energy E_a in the Arrhenius plot.

In [2], three different fitting methodes are presented:

1. a polynomial fitting,
2. sum of 100 exponential with fixed time constants and variable amplitude coefficients,
3. stretched multiexponential function.

In the first method [51], I_d is fitted using a polynomial function

$$I_d(x) = a_0 + a_1 x + ... + a_{n-1} x^{n-1} \tag{33}$$

with $n = 10$ and $x = \log(t)$. The second method based on [14], models the drain current as:

$$I_d(t) = I_\infty + \sum_{i=1}^{n} a_i \exp\left(-\frac{t}{\tau_i}\right) \tag{34}$$

where a_i are the fitting parameters and represents themagnitude trapping/detrapping processes, whereas τ_i are the predefined constants that are eqaully spaced logarithmically in time. The fitting method proposed in [3] is a multiexponential function

$$I_d(t) = I_\infty - \sum_{i=1}^{n} A_i \exp\left(-\frac{t}{\tau_i}\right)^{\beta_i} \tag{35}$$

where A_i[6] is the amplitude, β_i is the non-exponential stretching factor.

6 If $A_i < 0$ the process is the charge capture, else $A_i > 0$ is a emission capture.

3.5 CAPACITANCE DEEP LEVELS TRANSIENT SPECTROSCOPY

This technique was develop by Lang in 1974 [27] and to study the capacitance transient variation in function of temperature due to traps at the p-n junction. In view of the fact that in HEMTs there is no a unique junction, the gate-drain region or the gate-source region are chosen in order to study the traps under the gate with the HEMT control contact [35].

3.6 ON-THE-FLY MEASUREMENTS

This kind of measurements is a sort of transient measurements but at certain fixed period a pulsed probe bias voltage is applied in order to monitor the current collapse. Therefore in addition to the normal bias point $(V_{gb}; V_{db})$ employed to view the typical transient measurement, the probe bias point is set $(V_{gp}; V_{dp})$.

Bias point and probe point

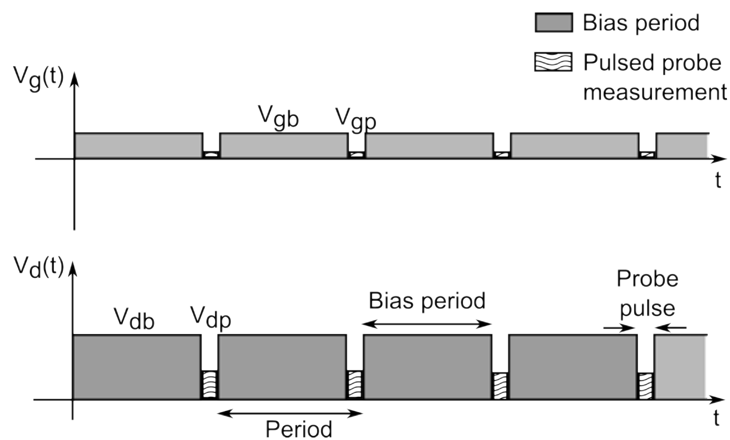


Figure 41: On-the-fly measurement.

A parameter analyzer is employed to perform this measurement with a minimum time resolution of $0.1s$ which is higher than the osciloscope one. The choice of the range of temperatures and device bias point must be taken precisely to obtain an useful measurement.

Through this measurements we can monitor the influence of the bias point on the drain current evolution at certain probe point. If the probe point is chosen in the linear working region we will see the R_{on} collapse, if in saturation region the threshold shift.

4 STUDY OF CURRENTS IN FUNCTION OF TEMPERATURE AND BIAS POINT

In this chapter we present the measurements performed on the devices under investigation. The role of temperature is extensively investigated. Temperature is important because it accelerates the processes and supplies external energy to device, as it will be clarified in the following. A good temperature stability of currents, Vth, $R - on$ must be guaranteed in power devices.

The main investigated feature of the devices is the parasitic leakage current and charge trapping effects introduced by Silicon-substrate and MIS-gate stack.

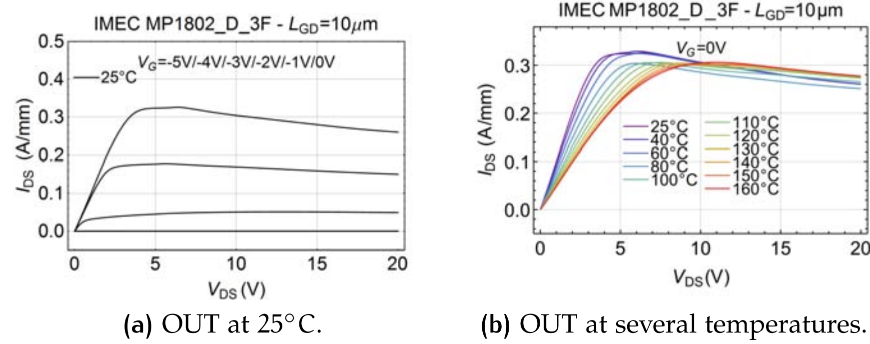
The role of substrate has been analysed through breakdown measurements in off-state, instead the second has been mainly investigated through on-the-fly and $I_d - DLTS$ measurements in on-state bias. At the beginning, DC measurements and double pulse measurements is shown. Then the study of breakdown and $I_d - DLTS$ will be presented.

4.1 PRELIMINARY STUDIES AND DC CHARACTERISATION

In this section we present the DC measurements at room temperature and at increasing thermal chuck temperatures.

First of all it is important to have a DC characterisation of a device in order to know the possible values of current or the order of magnitude at a certain bias points to not damage it.

In figure 42, 43 and 44 a complete DC characterisation of a device with $L_{gd} = 10\mu m$ at 25°C is reported[1].



(a) OUT at 25°C.

(b) OUT at several temperatures.

Figure 42: OUT characterisations. The device is the D_3F with $L_{gd} = 10\mu m$ and $W = 200\mu m$.

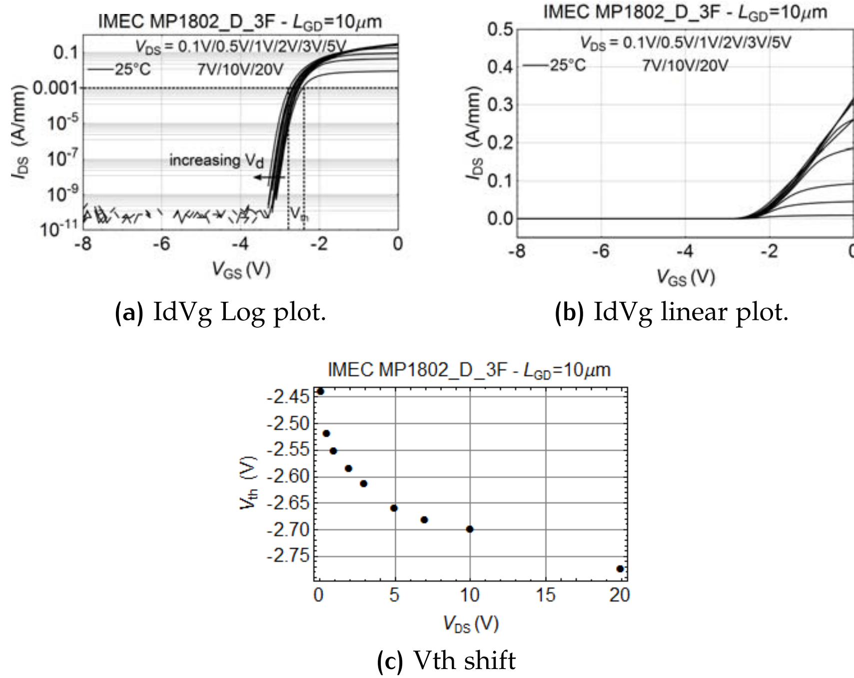
The OUT characterisation at $T = 25°C$ is reported in figure 42a and shows that there is a self-heating behaviour in the saturation region which decreases the Id as the Vd increases. Another consideration is that there is no appreciable Id when $Vg \leqslant -3V$. In figure 42b is reported an OUT plot at several temperatures at the same $Vg = 0V$. We observe the R_{on} collapse in the linear region and a growth of the saturation current if temperature is increased.

In figure 43, three IdVg are shown at increasing temperatures. Thanks to figure 43a we could estimate the pinch-off voltage in the Log-Log plot. The threshold voltage taken at $Id = 1mA/mm$ is Vd dependent (see figure 43c).

In figure $DCexampleIntemperature$, the IdVg at three different Vd are reported. As the temperature grows, a higher reverse gate voltage is required to open the channel because of the higher number of carriers when has been forming. The phenomenon is more evident as the Vd grows. This effect is named drain induced barrier lowering (DIBL) which lead to a IdVg shift.

However when channel is formed and at Vg close to 0V (saturation region) we note that the current decreases as the tem-

1 These measurements were performed through the Agilent Parameter Analyzer E5263 limits current resolution at $\sim 10^{-10}$A.

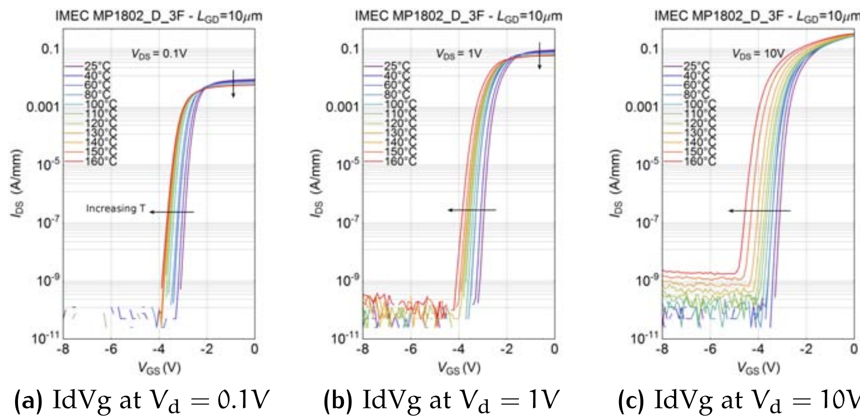


(a) IdVg Log plot.

(b) IdVg linear plot.

(c) Vth shift

Figure 43: IdVg characterisation examples. The device is the D_3F with $L_{gd} = 10\mu m$ and $W = 200\mu m$.



(a) IdVg at $V_d = 0.1V$ (b) IdVg at $V_d = 1V$ (c) IdVg at $V_d = 10V$

Figure 44: Log plots of IdVg curves at increasing V_d and at different chuck temperatures. They show the threshold voltage shift and the lowering of current in saturation region.

perature grows because of the low mobility of carriers [19], [58]. This phenomenon can be seen in 44b and 44c[2].

The study of currents vs temperature previews the knowledge of their order of magnitude and their limit conditions. The figure 45 represents a limit condition which may take place at

2 In 44c the phenomenon can not be observed because of the limited Vg range.

growing temperature conditions. At $Vg = -4V$ and at low temperatures, channel is still interrupted, consequently the drain current is lower than $1nA/mm$. At higher temperatures than $110°C$ the drain current overcomes $1nA/mm$ thanks to the threshold voltage shift.

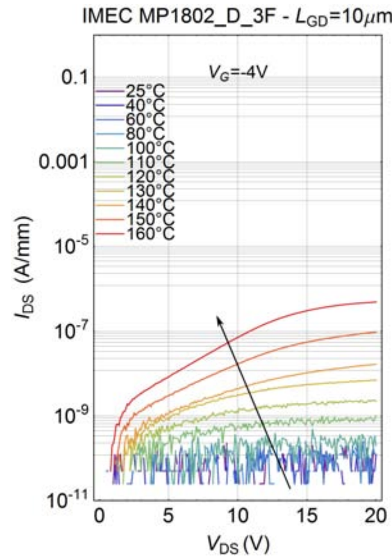


Figure 45: OUT measurement in a limit condition at $Vg = -4V$.

According to the Fermi-Dirac distribution, the temperature growth enhances the number of carrier: electrons at high temperature acquire thermal energy and could more easily overcome the energy barrier under the gate giving rise to parasitic currents.

4.2 EFFECTS OF GROUNDED AND FLOATING CONFIGURATION

Thanks to Si-substrate, we can choose to connect or not the device at ground potential[3].

This terminal could be another leakage path for current and can effectively play an important role during operations.

3 Devices grown on Al_2O_3 substrate do not have bulk contact because this material is an isolant, instead SiC-based devices are equipped with terminal.

In the following, comparisons between floating and grounded configuration will be shown for off-state to semi-on state breakdown measurements and DP measurements.

4.2.1 Breakdown at constant Vg from off-state to semi-on-state

The starting measurements which can be performed in this case is the breakdown measurements at constant Vg in off-state and semi-on state (see figure 46 a). Vg is increased from $-8V$ (off-state) to $-3.7V$ at different voltage steps. We can see from the IdVg figure, that when channel is formed the Id is higher in the grounded configuration because of the presence of more carriers involved. The four current contributions can be noticed in figure 46b and 46c.

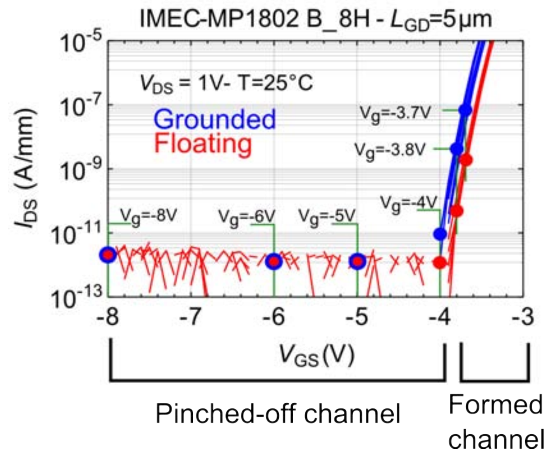
In grounded configuration when channel is formed, bulk current becomes the dominant contribution to breakdown, even higher than source current. At $Vd > 150V$ the bulk contribution is dominant and this gives rise to the vertical breakdown current originating from bulk and collected at drain. When channel is formed the drain current is the sum of bulk and source contribution.

Another remark can be done in the grounded measurement: the drain current starts always from a value lower than $10nA/mm$ and then goes in the same way of bulk.

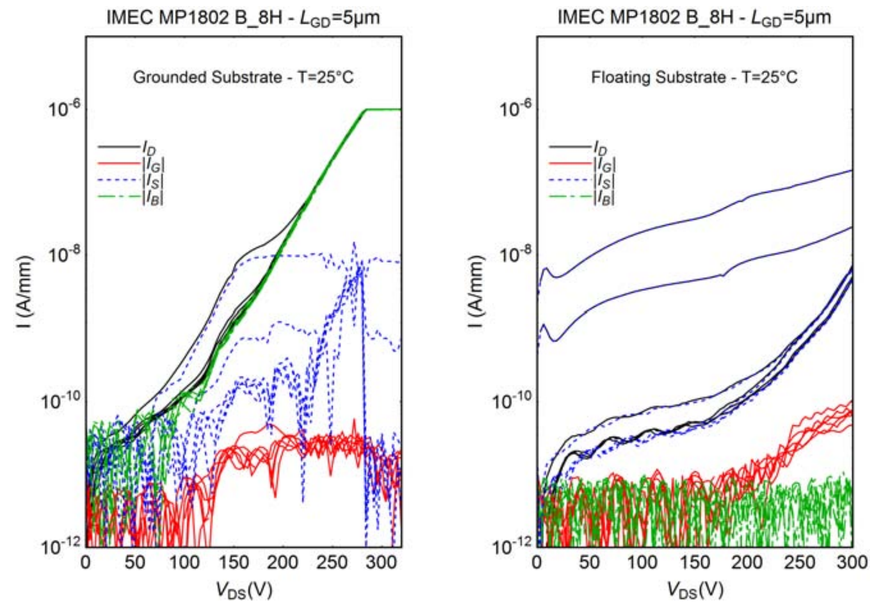
Instead in the floating configuration we can observe that drain current follows always the source current. Even at low Vg, when channel is interrupted. This can be explained by the presence of a leakage path in the GaN channel layer or in the AlGaN back-barrier because not involved in $Vg = -3.7V$ and $-3.8V$. The gate current does not contribute significantly to the process.

We can also notice the different slopes of the curves in the two different configurations: in floating configuration the drain current starts higher but it is more stable in function of Vd, instead in grounded configuration starts slower but grows faster

until the compliance. In floating configuration drain current is less sensitive in relation to Vd sweep.



(a) Comparison of the IdVg curves in floating and grounded configuration



(b) Grounded configuration. Source current not directly measured.

(c) Floating configuration

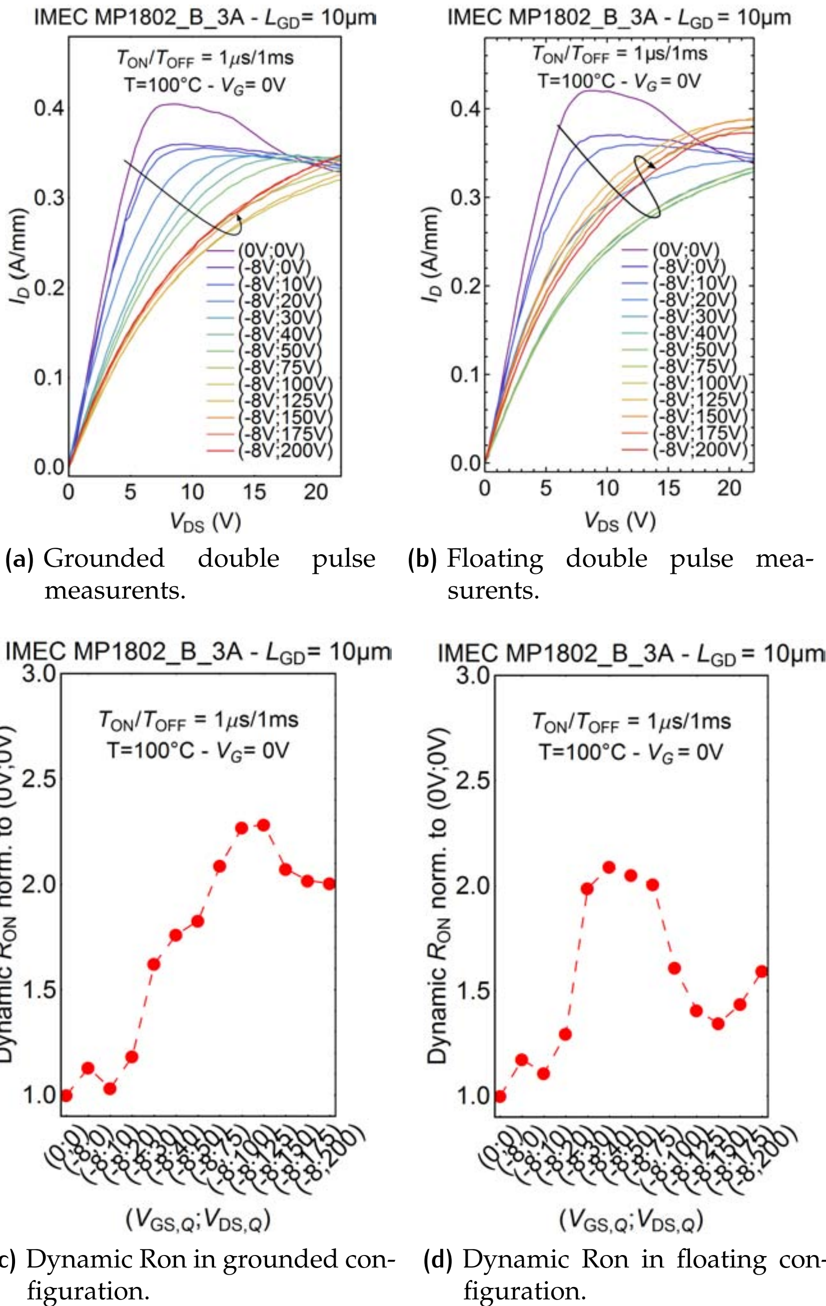
Figure 46: Breakdown measurements in floating and grounded configuration. A compliance at 1µA/mm is setted to not demege the device. Source current is not directly calculated.

Therefore through breakdown measurements from off-state to semi-on state, we note the critical role of bulk in power AlGaN/GaN HEMTs grown on Si-substrate at high Vd when a vertical breakdown occurs.

4.2.2 Double Pulse measurements

The critical role of Si-substrate can also be underlined by DP measurements at different quiescent bias points (see figure 47).

The quiescent bias points are chosen in order to trap in the whole gate-drain region in order to monitor the Ron collapse.



(a) Grounded double pulse measurents.

(b) Floating double pulse measurents.

(c) Dynamic Ron in grounded configuration.

(d) Dynamic Ron in floating configuration.

Figure 47: Comparison of DP in grounded and floating configuration.

If at low quiescent bias points the behaviour between the configurations is similar, after the quiescent bias point $(-8V, 30V)$ a significant changement is shown. Ron is growning for both of them but in two different ways. In floating configuration Ron remains quite constant until $(-8V, 75V)$ and then recovers, instead in grounded measurement the recovery is not so appreciable. The reason to explain the different recovery behaviours is still opened.

4.3 BREAKDOWN MEASUREMENTS AT CONSTANT VD

In figure 48 the sustainable breakdown measurements at constant $V_d = 50V$ are shown for each current contribution carried out on six devices of cell C of rough 3 with $L_{gd} = 10\mu m$.

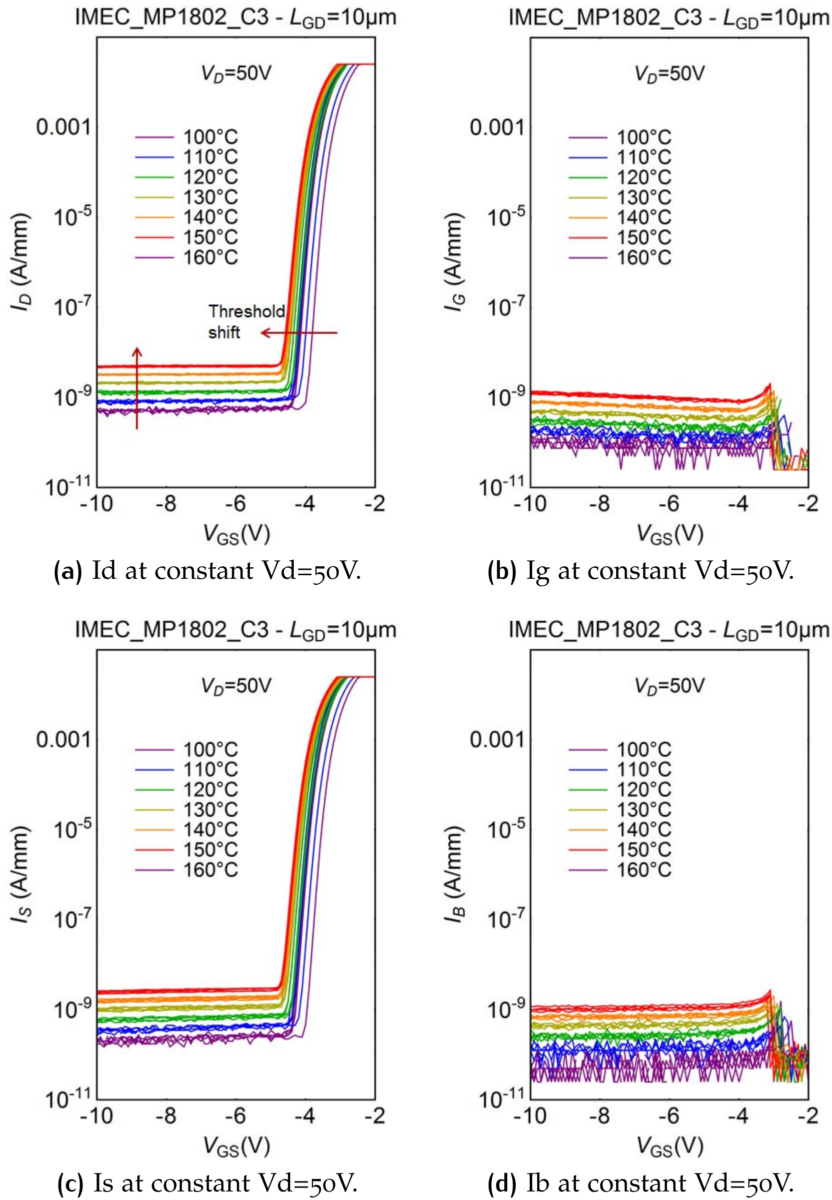
The aim of this measurement is to study the behaviour and the contribution of each current (I_d, I_g, I_s, I_b) at a relatevely high drain potential with bulk contact grounded.

These measurements allow to evaluate the growth of leakage currents and the threshold voltage shift at increasing temperatures and high voltage. They provide more information than a simple IdVg because they allow to see the different behaviour and growth of each current, which is not permitted through a IdVg.

We have chosen to plot only the curve in the range 100°C to 160°C because of the limited esolution of the parameter analyzer.

4.4 SUBSTRATE ROLE IN OFF-STATE BREAKDOWN

We focused our study on the breakdown phenomena at $V_g = -8V$ where the channel is interrupted and there is a depletion



(a) Id at constant Vd=50V.

(b) Ig at constant Vd=50V.

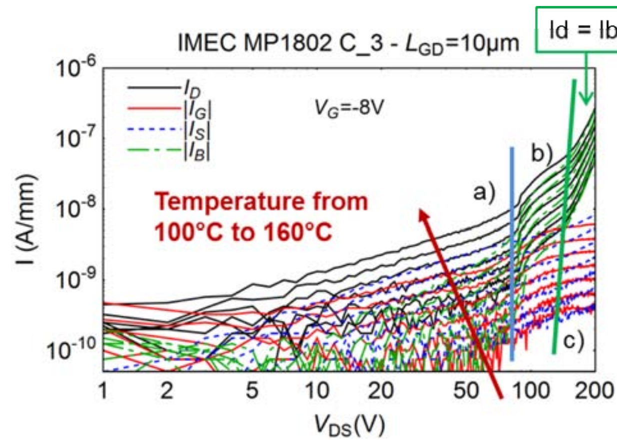
(c) Is at constant Vd=50V.

(d) Ib at constant Vd=50V.

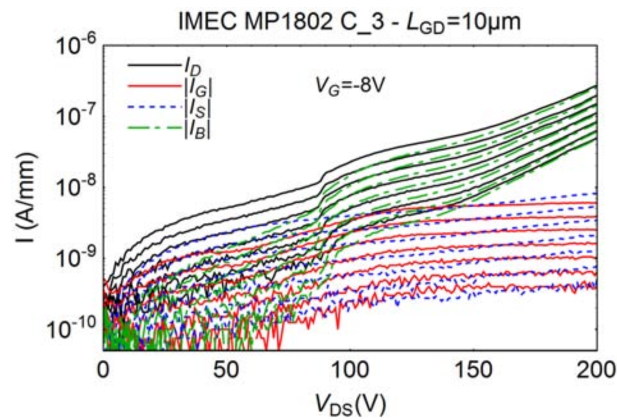
Figure 48: Breakdown at constant Vd=50V.

region under the gate in order to understand the contributions at the drain current which give rise to breakdown. We even present a case of failure during these measurements. Finally the backgating measurements are performed to see what happens by means of reverse bias at bulk contact.

In figure 49 are shown the Log–Log plot and Lin–Log plot. Three main different behaviours give rise to three region named a), b), c).



(a) Log-Log plot.



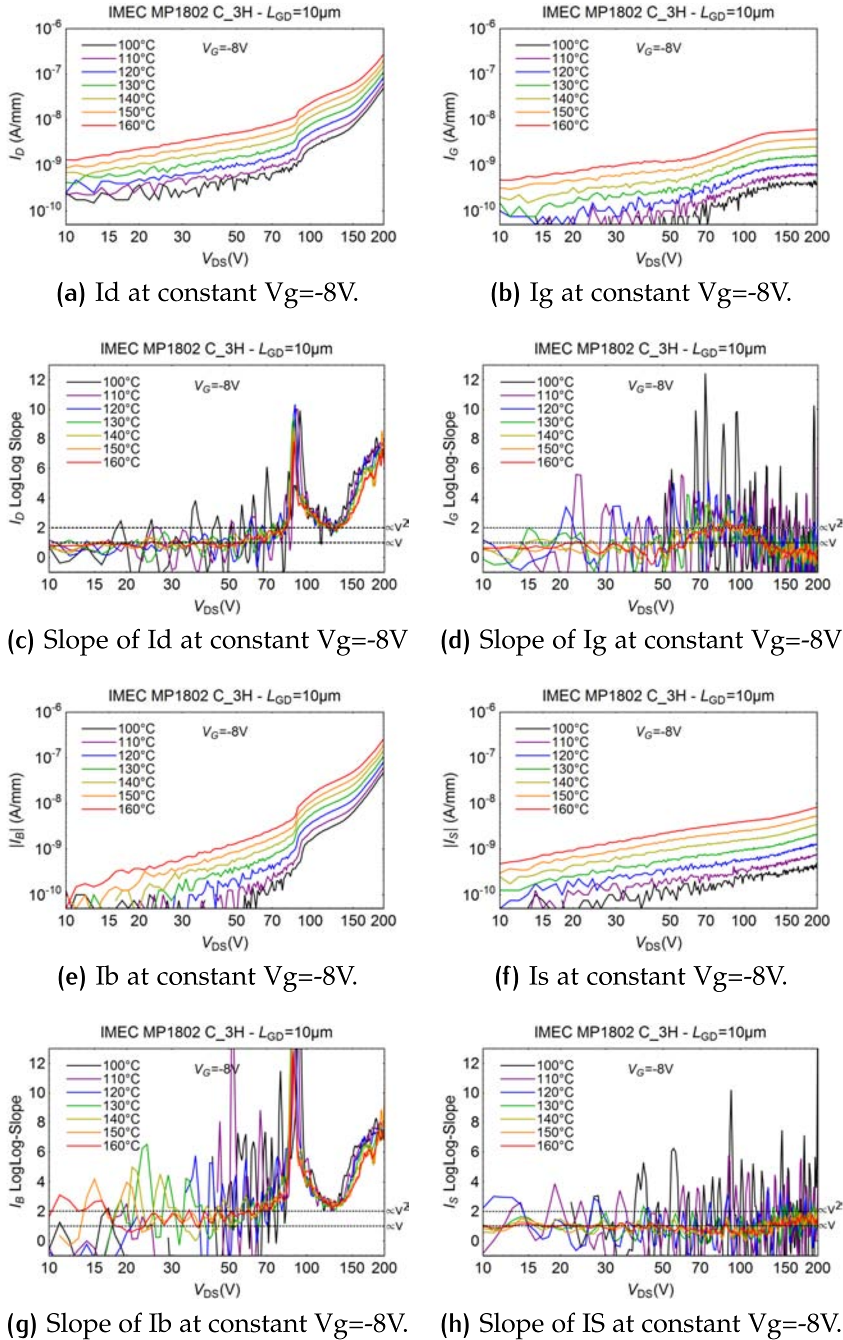
(b) Lin-Log plot.

Figure 49: Breakdown at constant $V_g = -8V$ at $T = 100°C$, 110°C, 120°C, 130°C, 140°C, 150°C and 160°C.

In the first one, the drain current follows the source and gate currents until ~ 85V where takes place the first sudden current increase given by the breakdown phenomenon.

To explain the phenomena we plotted the LogLog slope for each current (see figure 50). The drain current slope shows that until the first breakdown mechanism, the conduction could be ohmic (slope = 1), then it grows exponentially and then decrease until 2 which could mean a space-chare-limited-current[4] (SCLC) mechanism is involved. After that it exponentially grows.

4 This mechanism occurs in a bulk material region. It is due to the generation of charge in the region by means of high electric field which drops across it and ionizes/deionizes charges [26], [44]. The mechanism involves also trapped charges [43].



(a) Id at constant Vg=-8V.

(b) Ig at constant Vg=-8V.

(c) Slope of Id at constant Vg=-8V

(d) Slope of Ig at constant Vg=-8V

(e) Ib at constant Vg=-8V.

(f) Is at constant Vg=-8V.

(g) Slope of Ib at constant Vg=-8V.

(h) Slope of IS at constant Vg=-8V.

Figure 50: Breakdown at constant Vg=-8V at T = 100°C, 110°C, 120°C, 130°C, 140°C, 150°C and 160°C.

Gate current seems to be modeled by an ohmic current because the slope is 1 but at intermediate Vd, it is closer to a SCLC behaviour.

Source current remains ohmic during the whole Vd sweep.

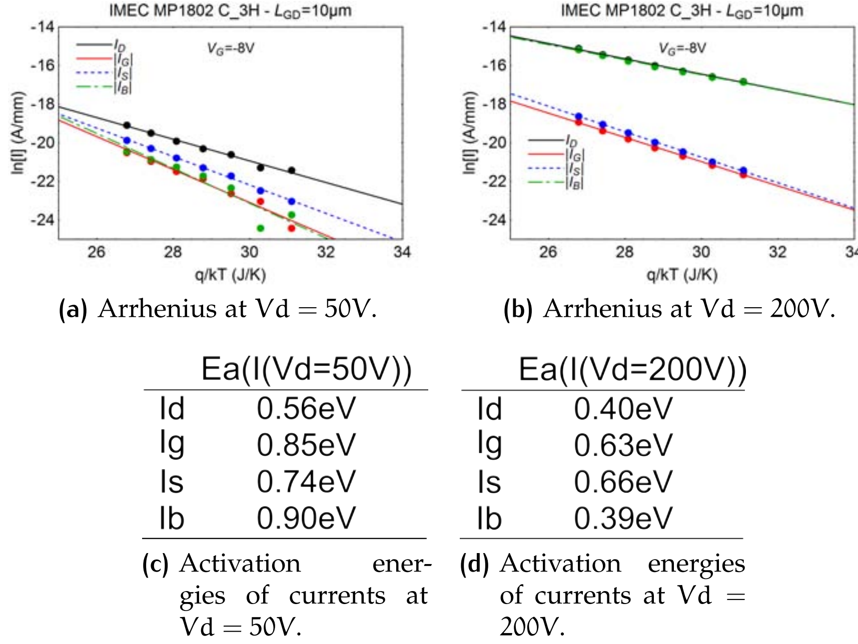
Concerning the bulk, it could be modeled by a SCLC before the exponential growth at the first breakdown phenomena.

We note that the sudden increase at drain is given by the bulk current. In fact if at low Vd the bulk contribution is negligible, it starts increasing with Vd and it becomes the main contribution to breakdown process. Like the drain current, it presents a SCLC slope after the exponential decrease. Then, another exponential growth occurs. We note also that the slope at the first breakdown phenomenon is higher for bulk current than for drain. A possible explanation is that the ohmic contact at drain lowers the effect of generated charge.

The origin of the first breakdown phenomena could be explained by the emission of the carriers trapped during the Vd sweep thanks to the combination of high electric field across the GaN buffer region and the bending of valence and conduction band. In fact, because of the increasing forward bias applied at drain, the band diagram is bended down at the drain side. The regions are bended one by one starting from GaN buffer at increasing Vd. Because of this, the carriers generated in the GaN buffer during the process should be the holes come from acceptor-like ionized traps (a possible demonstration of the fundamental role of holes is that the ohmic can not act as a reservoir of electrons because it is forward biased). Finally these generated holes go up to bulk contact giving rise to current.

The first drain current sudden increase occurs at the same drain voltage and it divides the a) region to the b). This fact could exclude the mechanisms activated by temperature and could be related to phenomena which involve a region which is completely bended. This region might be probably the GaN channel or the first AlGaN back barrier layer. After the first sudden increase, we note thaere is a extra current which might be associated to the emission of carriers (the latters might be trapped at lower Vd or can come from parasitic channels due to junctions such as GaN-channel/first-AlGaN back-barrier)

Finally in figure 51 the Arrhenius plots at $Vd = 50V$ and $Vd = 200V$ are presented with their currents activation energies.



(a) Arrhenius at Vd = 50V.

(b) Arrhenius at Vd = 200V.

	Ea(I(Vd=50V))
Id	0.56eV
Ig	0.85eV
Is	0.74eV
Ib	0.90eV

(c) Activation energies of currents at Vd = 50V.

	Ea(I(Vd=200V))
Id	0.40eV
Ig	0.63eV
Is	0.66eV
Ib	0.39eV

(d) Activation energies of currents at Vd = 200V.

Figure 51: Arrhenius plots and activation energies of currents in breakdown measurements at constant $V_g = -8V$.

First of all we observe that all currents are thermally activated because they present a non-zero activation energy.

Comparing the currents activation energies at these two different voltages, we observe the high decrease of bulk current from $0.90eV$ at $Vd = 50V$ to $0.39eV$ at $Vd = 200V$. Also other activation energies are lower at $Vd = 200V$ than at $Vd = 50V$. This means that other currents are more stable in temperature than the bulk one and consequently for the drain current.

4.4.1 Device failure case

We want to present now the failure of one device during the measurement. In figure 52 is reported the high-voltage breakdown at room temperature of a device with $L_{gd} = 10\mu m$[5].

We note that before the breakdown occurred at 693V the drai current follows always the bulk current. After the breakdown occured at $Vd = 693V$, the source current follows the gate current. This means that the breakdown is occured at gate contact,

5 An $L_{gd} = 10\mu m$ leads to a nominal breakdown voltage of 600V.

maybe in the drain side of it due to the critical electric field between the gate contact and the drain contact. Indeed the source current comes out from the broken gate contact and the drain. Finally we observe the snapback phenomena at drain contact caused by the device failure.

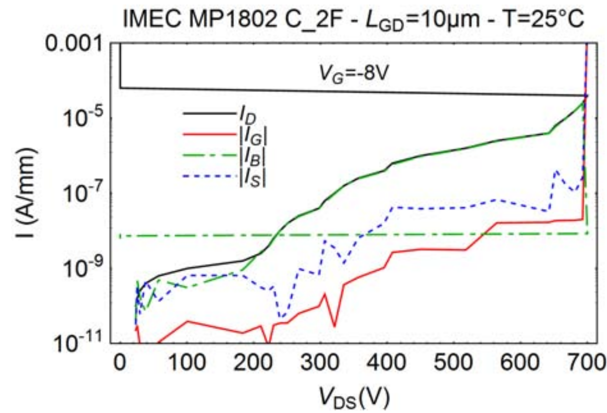


Figure 52: Device failure during breakdown at constant $Vg = -8V$ at $Vd = 693V$ due to the gate-drain breakdown. Source current is not directly measured.

To deeper understand and observe the bulk role, we performed backgating measurements of breakdown and transients at different temperatures and bias point.

This technique is well known in AlGaN/GaN HEMT since [33] and is also employed in [22] and in [60]. The name comes from the fact that the substrate/buffer junction creates a depletion region that controls the transistor channel in the back side [33].

As reported in [22] this kind of measurements is easier performed in HEMT grown on Silicon rather than ones grown on sapphire because of the backgate current is by 3-5 orders of magnitude lower.

4.4.2 Off-state back-gating measurements

Back-gating measurements

We performed off-state breakdown-backgating measurements sweeping drain voltage and applying each time a different reverse voltage at bulk contact from $0V$ to $-150V$ at constant $T = 100°C$.

If we would expect that the drain current will be lowered because of the extension of the depletion region because of the increasing reverse bias applied at bulk, it will not. Indeed we see that, as the forward drain and reverse bulk voltage grow, the drain leakage current grows. The reason is that the vertical bands between drain and bulk are more bended and, as the electrons at bulk recive energy they do not run into a blocking barrier and can flow to drain.

If we would expect that the drain current will be lowered because of the extension of the depletion region because of the increasing reverse bias applied at bulk, it will not. Indeed we see that, as the drain voltage grows, the drain current follows the bulk contribution which in turn grows. Until $Vd = 50V$ there is no appreciable current growth which means the good block of leakage current from substrate, then the leakage currents at drain and bulk grow and no breakdown mechanism is still involved until $Vd = 200V$.

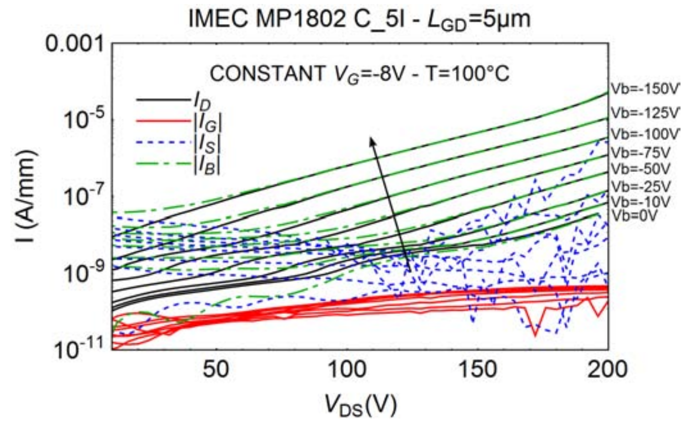
We conclude this section saying that the bias situation studied through off-state breakdown measurements can really occur: in off-state condition, the drain contact voltage is brought to high voltage because of the external circuit.

Therefore we can say that backgating measurements underline that reversing bias the bulk contact leads to higher leakage current.

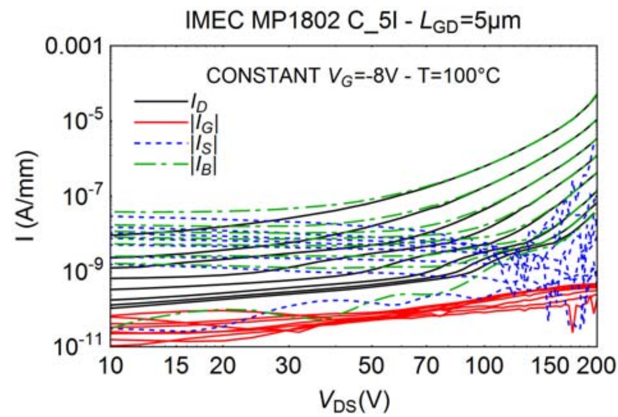
4.5 R_{on} INVESTIGATION THROUGH BACKGATING ON-THE-FLY AND TRANSIENT MEASUREMENTS

In power HEMTs, R_{on} is a key parameter which has to be as lower as possible and constant during the working conditions.

We have already presented the DP technique, however another techniques exist in order to monitor this parameter: the



(a) Lin-Log plot.



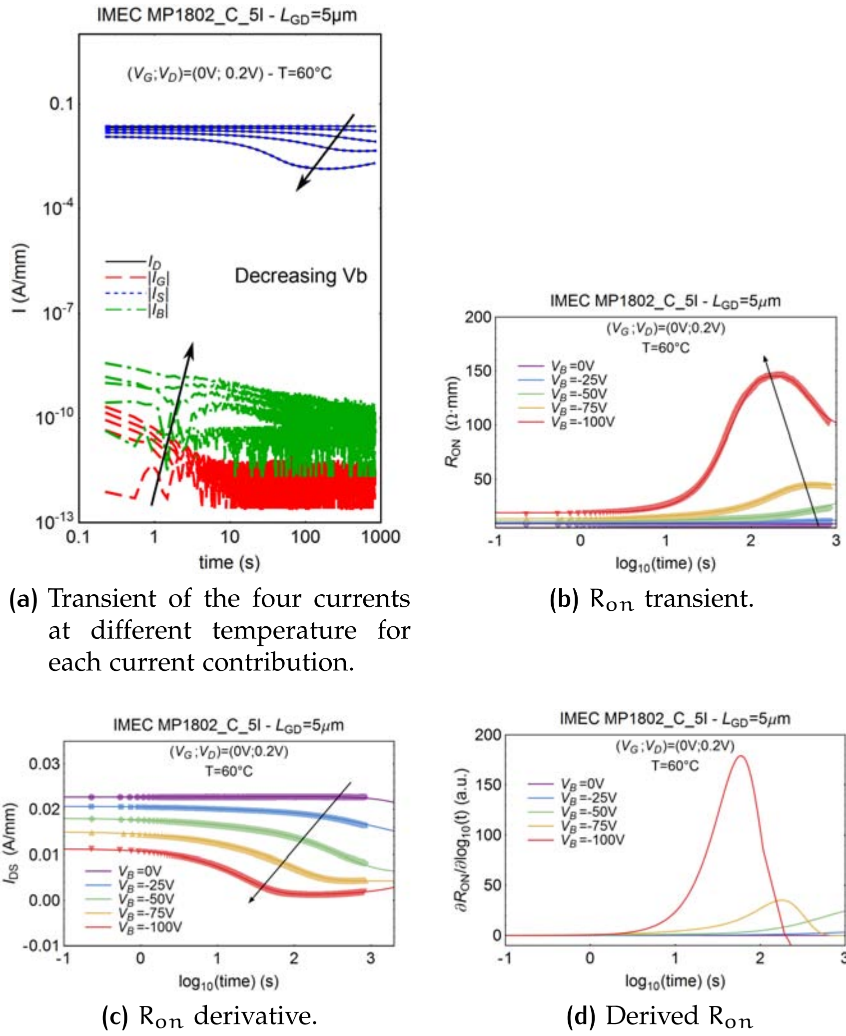
(b) Log-Log plot.

Figure 53: Backgating breakdown measurements at constant $V_g = -8V$ and $T = 100°C$. Source current is not directly measured.

transient measurements and the back-gating transient measurements.

Marso et al. in [33] performed the back-gating measurements with source and gate grounded, and $1V$ at drain contact (linear region). At the beginning they applied $0V$ at bulk, then they recorded the transient measurement at $Vb = -10V$. They performed this at several temperatures. They noted the decrease of the drain current at the bulk voltage switch and a large overshoot.

The explanation suggested for the first is that the depletion region was increased, the cause of the second can be related to thermal release of trapped majority carriers in the depletion region.



(a) Transient of the four currents at different temperature for each current contribution.

(b) R_{on} transient.

(c) R_{on} derivative.

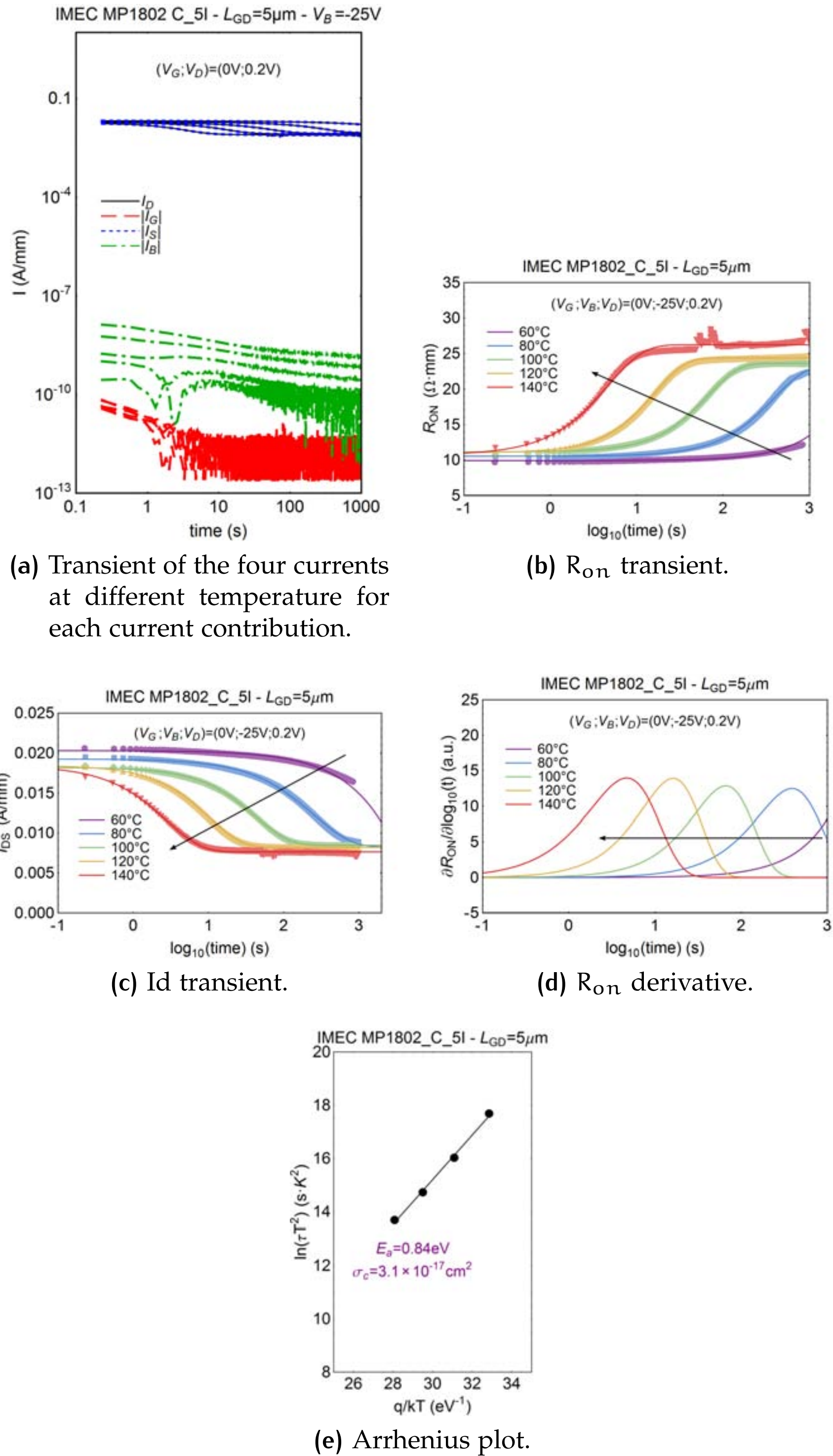
(d) Derived R_{on}

Figure 54: Backgating transient at constant temperature $T = 60°C$ at several $Vb = \{0V; -25V; -50V; -75V; -100V\}$.

Then we performed two transients in order to see the relation among Ron and reverse bias applied at bulk substrate and temperature:

- constant $Vg = -8V$ and $T = 60°C$ at different Vb (see figure 54),
- constant $Vg = -8V$ and $Vb = -25V$ at different temperatures (see figure 55).

The goal of the first one is to understand if there is a relation between the R_{on} and the reverse bias applied because of plots of figure 54.



(a) Transient of the four currents at different temperature for each current contribution.

(b) R_{on} transient.

(c) Id transient.

(d) R_{on} derivative.

(e) Arrhenius plot.

Figure 55: Backgating transient at constant bias point $(Vg, Vb, Vd) = (0V, -25V, 0.2V)$.

We note a big difference between the 0V applied at bulk curve and the $-150V$ curve. If in the first case there is no R_{on} collapse appreciable in a 1000s time interval, in the high-

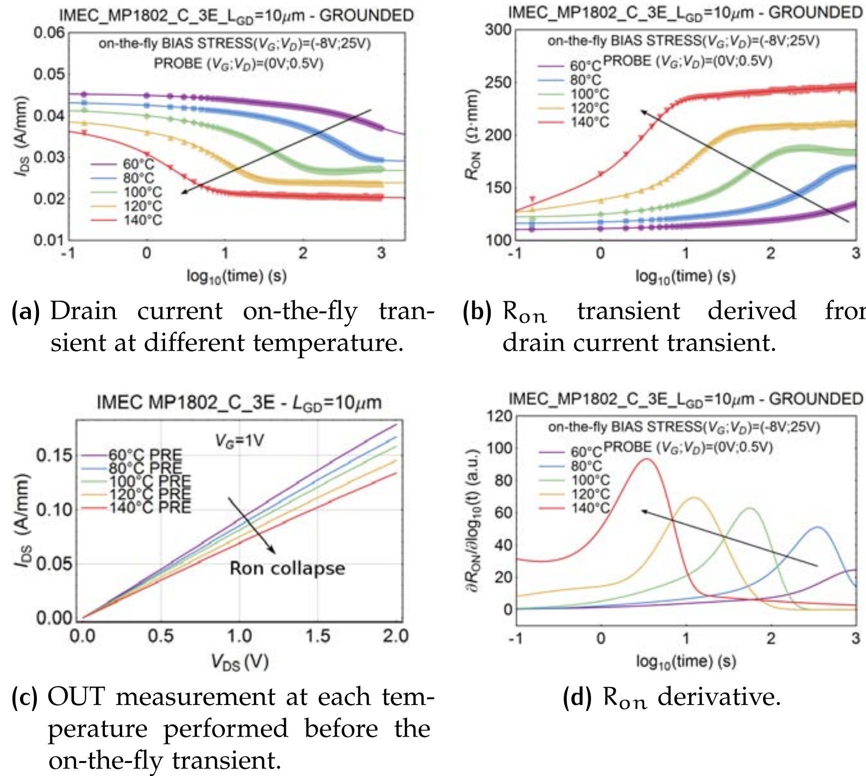
est reverse bias case there is a sensible collapse maybe due to the trapping phenomena in the substrate interface, back barrier and buffer regions due to the growing depletion region and carriers trapped there which lower the current. The R_{on} transient shows the critical R_{on} collapse at high reverse biases which accelerate the process (one time decade). We note also that in the most critical case (when the reverse bias is maximum), there is also a detrapping phase after 100s which gives rise to a recovery of the R_{on} and the emission of trapped carriers. This phenomenon is just seen at $Vb = -100V$.

In order to see if the backgating process of R_{on} collapse is also thermal activated, we have performed a transient measurement at several temperatures from $60°C$ to $140°C$ applying a constant $Vb = -25V$. The transient measurement and the subsequent extrapolated Arrhenius plot are shown in figure 55. Compared with the previous measurement, the process dynamic is faster thanks to the temperature growth. In 55c is shown the drain current transient: we note that the temperature speeds the process and causes a carrier trap. Even if the temperature grows we note that there is no recovery phase in this case. The energy activation E_a of the process is $0.84eV$ and a cross section $\sigma_c = 3.1x10^{-17}cm^{26}$.

The next step of the investigation is monitoring the R_{on} collapse during an on-the-fly stress measurement.

In order to trap in the gate-drain region which involves R_{on}, we applied during the bias stress $(Vg; Vd) = (-8V; 25V)$ and we recorded the probe transient in linear region at $(Vg; Vd) = (0V; 0.5V)$ (see figure 56). This measurement is carried out at different temperatures. At each temperature and before the on-the-fly measurement, we monitored the R_{on} collapse through an OUT measurement (see figure 56c). Comparing the drain current transient at 60°C and 140°C, we observe that there are two orders of magnitude between the end of the second and the beginning of the first.

6 These results are obtained considering the actual channel temperature with the thermal resistance $R_{th} = 15Kmm/W$ as reported in [6].



(a) Drain current on-the-fly transient at different temperature.

(b) R_{on} transient derived from drain current transient.

(c) OUT measurement at each temperature performed before the on-the-fly transient.

(d) R_{on} derivative.

Figure 56: On-the-fly transient measurements which monitors the R_{on} during a stress at $(Vg; Vd) = (-8V; 25V)$.

looking at the derivative plot of R_{on} we see that the process of capture of carriers [7] and a carrier emission [8] is speeded by the temperature.

Backgating and on-the-fly measurements both at constant and at growing temperature underline that the reverse bias applied at bulk contact leads to a higher leakage current coming from bulk and a consequent R_{on} collapse.

7 Which could be associated to a derivative increanse REFERNCE!!!
8 Which could be related to a decrease of derivative.

4.6 TRAPPING ON-THE-FLY TRANSIENTS AND DETRAPPING TRANSIENTS OF THE V_{th}

In this section we want to analyse the influence of traps located under the gate region to device performances. We did it by a combination of drain current transients and on-the-fly measurements.

The threshold voltage is the key parameter linked to this region. In fact the Vgs value affects the quantity of current which can flow in the channel. An unwanted threshold shift may cause critical and undesired operating situations.

As reported in the first chapter, our device are equipped with a MIS structure under the gate composed by a layer of Si_3N_4 and a layer of Al_2O_3. The effects of them is investigated in the following.

Firstly, we have performed an on-the-fly transient (see figure 57) applying a bias stress at $(Vg, Vd) = (2V, 0V)$ in order to fill the traps located under the gate without affecting the drain region (see figure 31), and applying a probe bias at $(Vg; Vd) = (-1V; 5V)$ in order to monitor the threshold voltage transition region during the stress.

By the transient figure we observe that the dynamic is different from the R_{on} presented in the section before. Infact it is not similar to an exponential, it looks like a line and it can be more appreciated in the normalized plot in figure 57b.

After that, we wanted to see the influence of the forward bias stress gate voltage in the trapping and detrapping transient of threshold voltage. It is shown in figure 58.

We note that as the gate bias stress voltage is increased, the trapping phenomena are more evident because of the current collapse[9]. In the first two bias points at $(Vg, Vd) = (0V, 0V)$ and $(1V, 0V)$ there is no appreciable Id decrease; on the other hand

9 Also the band diagram is changed: in fact as the voltage at gate grows, it is more bended and other traps located at the junctions between metal/insulator and insulator/AlGaN can be filled. See figure 31.

at $(Vg, Vd) = (2V, 0V)$ and $(3V, 0V)$ we obverse an higher collapse at drain due to the fact that these are critical bias points.

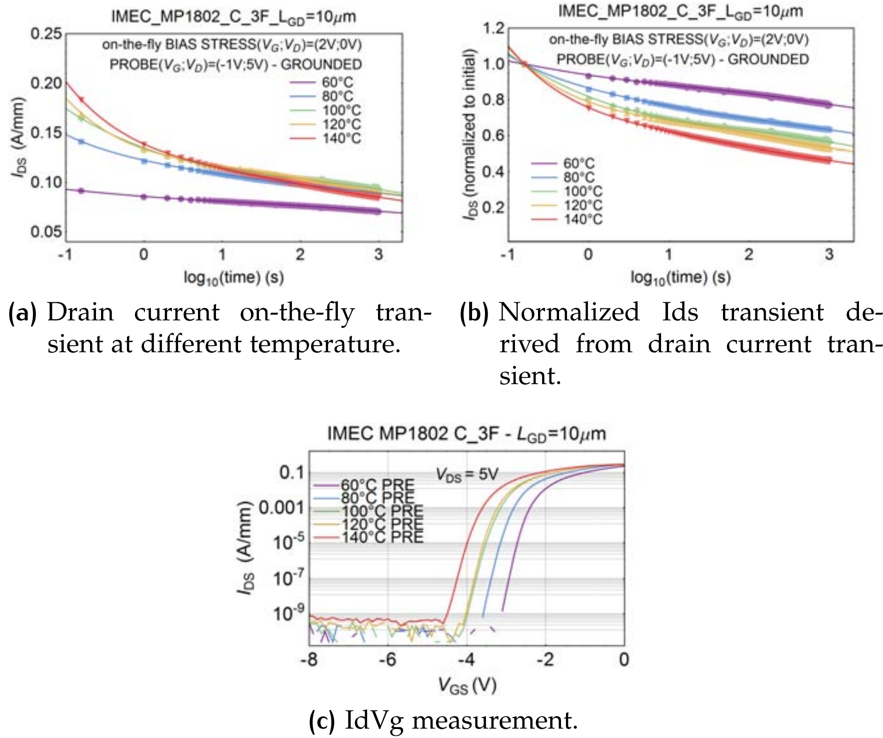
A possible explanation of this phenomenon is that electrons could be trapped in the interface states located at the $AlGaN/Al_2O_3$ interface or inside the insulators or at the $metal/Si_3N_4$. A non-exponential processing is occurring and it might be caused of the high number of traps located in this region which give rise to different exponential behaviours.

Another consideration is related to the time to recovery to the initial value of current. In the two case $1000s$ are not enough to restore the initial value of current, this means that the constant times associated to these trapping phenomena are long and the traps are deeply located.

Finally we performed the same kind of measurements but at several temperatures and at two forward bias stress points in order to see the relation between the phenomena involving the gate region and the temperature.

In figure 59 are reported the trapping on-the-fly transient and the detrapping transients: in the first rough are shown the measurements with on-the-fly bias stress at $(Vg, Vd) = (2V, 0V)$ instead in the second rough those related to the on-the-fly bias stress at $(Vg, Vd) = (3V, 0V)$.

In these figure we can compare the different start point of the on-the-fly stress measurements and that a recovery time of $1000s$ is not enough. During the stress measurement, the increasing temperature lowers the drain current. Due to the non-exponential behaviour we could not extrapolate the Arrhenius plot related to this measurements.

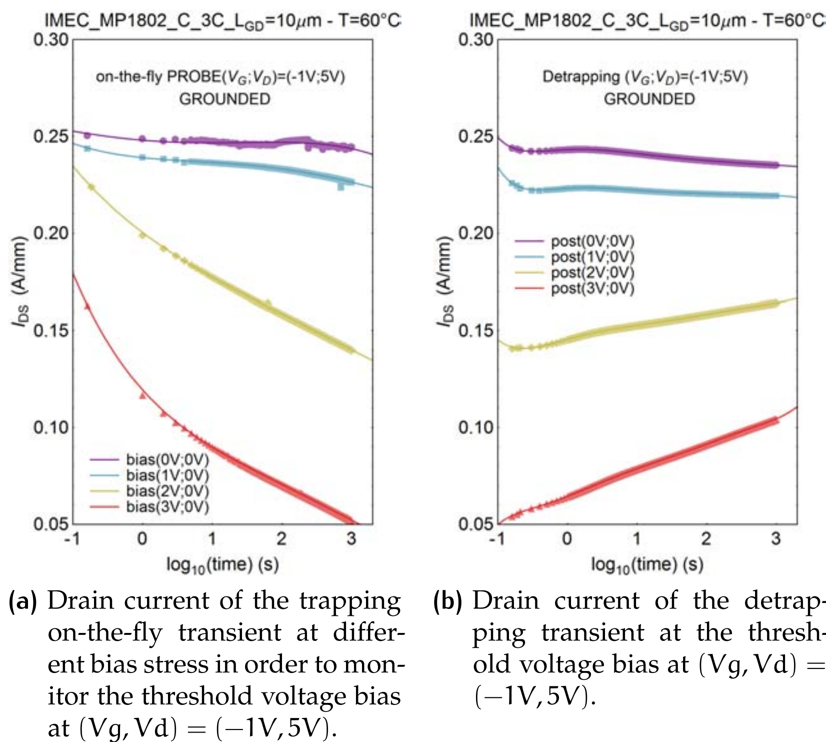


(a) Drain current on-the-fly transient at different temperature.

(b) Normalized Ids transient derived from drain current transient.

(c) IdVg measurement.

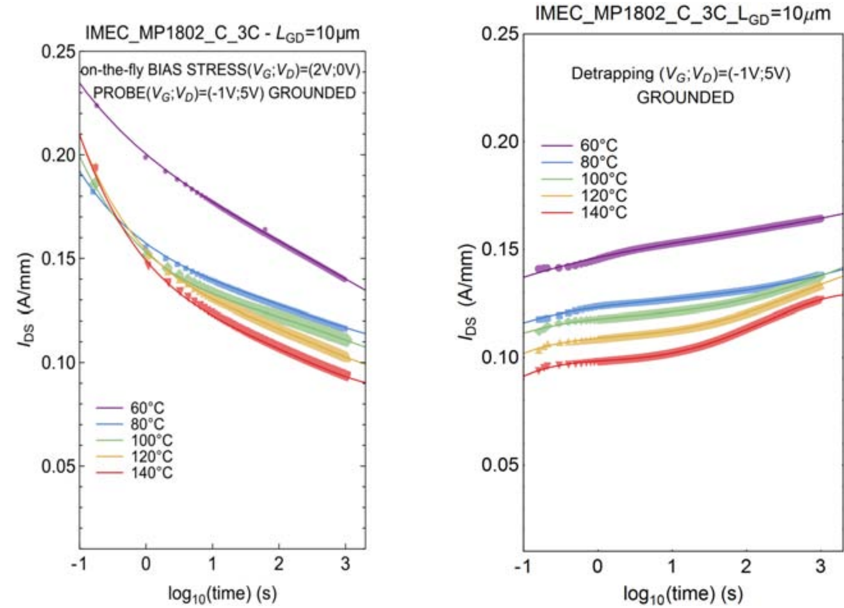
Figure 57: On-the-fly transient measurements which monitors the Vth during a stress at $(Vg; Vd) = (2V; 0V)$.



(a) Drain current of the trapping on-the-fly transient at different bias stress in order to monitor the threshold voltage bias at $(Vg, Vd) = (-1V, 5V)$.

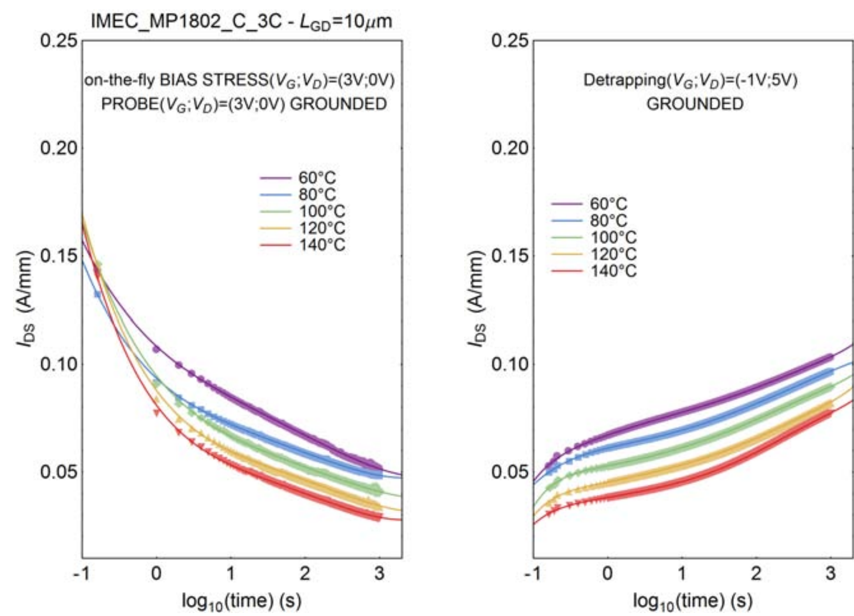
(b) Drain current of the detrapping transient at the threshold voltage bias at $(Vg, Vd) = (-1V, 5V)$.

Figure 58: Trapping on-the-fly measurements of threshold voltage followed by a detrapping transient.



(a) On-the-fly trapping probe measurement.

(b) Detrapping transient at $(Vg, Vd) = (-1V, 5V)$.



(c) On-the-fly trapping probe measurement.

(d) Detrapping transient at $(Vg, Vd) = (-1V, 5V)$.

Figure 59: On-the-fly trapping transient measurements and detrapping measurements which monitorthe Vth collapse during two different forwars bias stress conditions.

5 CONCLUSIONS

This thesis work is based on the experimentals on a double heterostructure AlGaN/GaN power MIS-HEMTs grown on Si-substrate produced by IMEC.

The aim was to study the influence of breakdown and trapping phenomena on possible operating situations: off-, semi-on- and on-state. The breakdown measurements were performed in off-state instead the trapping phenomena were monitored in the whole operating regions.

At the beginning, we performed the basical measurements to characterize the devices, i.e. DC and Double Pulse measurements. Due to the fact that power devices must guarantee good performances also at high temperatures, we employed a probe station provided by thermal chuck which supplies heat to device, then we observed the changement of curves and parameters.

We studied the role of the Si-substrate through off- and semi-on-state breakdown both in grounded and floating configuration. We observe that in off-state the role of bulk current is evident at high drain voltages, in fact a vertical breakdown occurs between drain and bulk contacts. We have also tried to explain the physical and electric origines of breakdown. A destructive breakdown was carried out on one device. It occurred at $Vd = 693V$. The failure has been originated at gate. The study of off-state vertical breakdown has requested a research of articles and sources to understand the phenomena. Thanks to this, in the appendix a review of the articles is presented.

A key parameter for power HEMT is the R_{on}. This parameter is investigated in linear region where the HEMT should work with the lowest R_{on} (ideally it should be a short circuit). Its stability in temperature and during and after device stress have been monitored through on-the-fly measurements and back-

gating transients measurements. By the obtained results we note that the temperature and high reverse Vb accelerate the collapse of R_{on}.

Finally the MIS gate contact has been investigated. The MIS structure reduces the reverse gate leakage current, requested feature in power devices. Until the off-state stress condition of $Vd \sim 600V$, the gate current is less than $100nA/mm$. However through the on-the-fly measurements performed in forward bias stress, we noted that there is a considerable shift voltage and Id collapse due to the trapping states present at the interfaces metal/insualtor and insulator/AlGaN. A non-exponential behaviour is shown. Forward stress on-the-fly and recovery transient measurements show high trapping at gate, drain current collapse and long time (more than $1000s$) to restore the initial value of current before the stress.

A A REVIEW OF VERTICAL BREAKDOWN IN ALGAN/GAN-BASED STRUCTURES

The vertical breakdown is a limiting phenomenon for power AlGaN/GaN HEMTs. The phenomenon occurs when the drain voltage is brought to high values during off-state operations.

The aim of this appendix chapter is to briefly present some useful works which deal with this topic and see the explations reported as also the suggested improvements.

This topic is investigated both on HEMT and on vertical dedicated structures to improve the device performances.

The first work was developed by Lu et al. in [29] on a vertical structure grown on Si-substrate with an AlGaN back-barrier layer. A GaN buffer layer and an ohmic contact on top of it are grown.

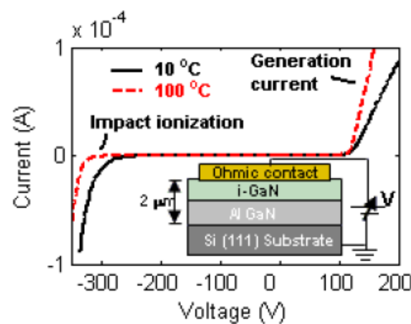


Figure 60: Forward and reverse vertical leakage current at T = 10°C and 100°C. Taken from [29].

In figure 60 we see the vertical leakage current in both forward and reverse bias. We note the asymmetry of the breakdown voltage (−290V and 100V) and the different behaviour vs temperature.

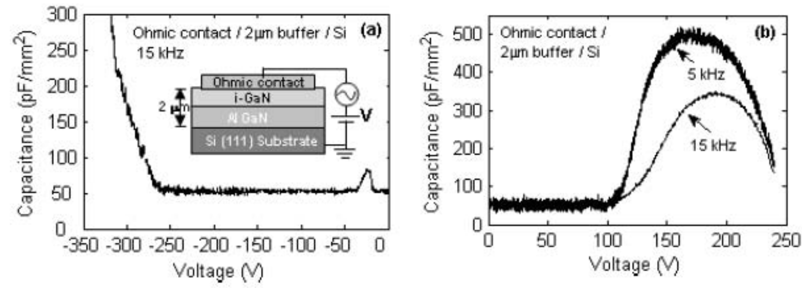


Figure 61: CV measurements in a) reverse bias and b) forward bias. Taken from [29].

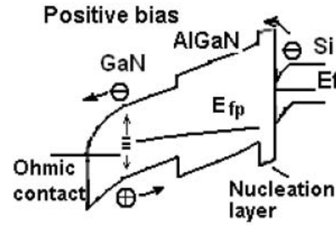


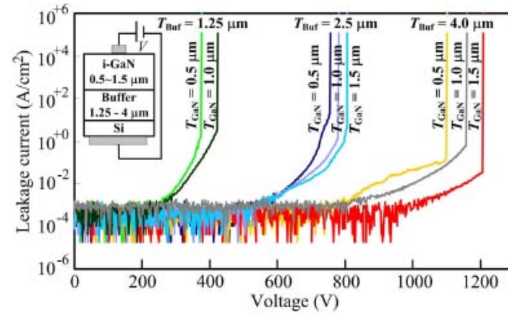
Figure 62: Band diagram in high forward bias. Taken from [29].

In figure 61 is reported the CV measurements in reverse and forward bias of the studied vertical structure. At high voltage both reverse and forward, the capacitance grows. In forward bias, electrons are injected from the substrate into the buffer. From $\sim 100V$ to $\sim 150V$ the capacitance grows, this means that the charge accumulated is positive, so holes are generated. As the voltage increases, electrons recombines with the holes reducing the capacitance (annihilation process). In reverse bias measurement as the reverse bias increases, electrons are injected from the source into the buffer giving rise to a space charge region[1].

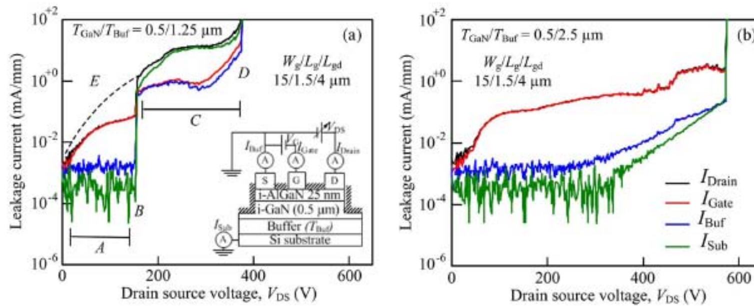
The problem of vertical breakdown is also studied by Rowena et al. in [45] in order to find the better buffer thickness T_{buffer} and i-GaN thickness T_{GaN} to increase the breakdown vertical voltage.

In figure 63a are reported the preliminary studies which underline that higher breakdown vertical voltage can be reached by a thicker T_{buffer}. Infact the role of the T_{GaN} is secondary. The

1 In the paper is also explained that this charge region creates a non uniform electric field distribution which could cause impact ionization in the buffer because of the positive temperature coefficient in figure 60.



(a) Vertical leakage current measured for the vertical structure dipcted at left.



(b) Off-state breakdown measurements with the comparison between a device with $T_{buffer} = 1.25\mu m$ and another with $T_{buffer} = 2.5\mu m$.

Figure 63: Study of the influence on buffer thickness on vertical breakdown. Taken from [45].

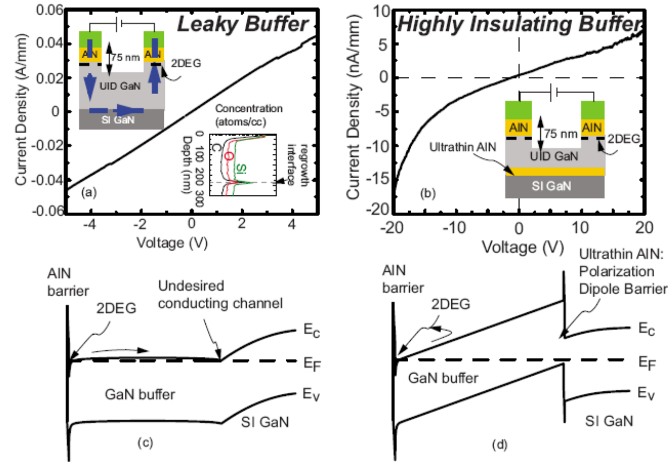
maximum breakdown voltage reached is 1207V with $T_{GaN} = 1.5\mu m$ and $T_{buffer} = 4\mu m$.

The off-state breakdown measurement was performed at $Vg = -5V$ on two HEMTs grown on Si-substrate with different T_{buffer}. The measurement is reported in figure 63b. It shows that the breakdown evolution is different in the devices: in the first we note two main steps, in the second only one. They reported that in the first case with thinner buffer, the behaviour is due to the larger dislocation driven by low resistive buffer. The second device with thick buffer is more stable and offers higher breakdown.

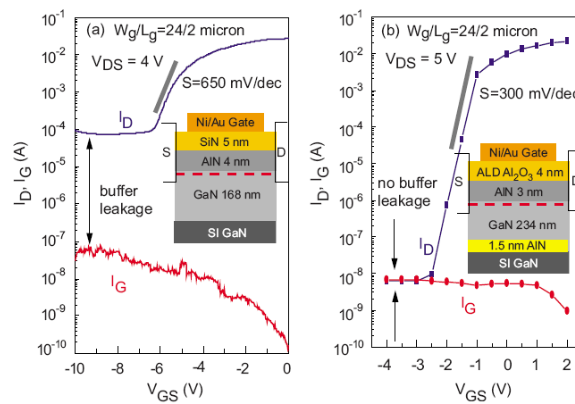
The problem of vertical breakdown is not also related to Si-based substrate.

Another article and solutions are proposed by Cao et al. in [5]. They investigated how to lower the buffer leakage in a

structure grown on semi-insulating GaN in order to improve HEMTs.



(a) Forward and reverse vertical leakage current for the two structures with their band diagrams.



(b) Compirason of the breakdown vertical leakage currents and band diagrams with and without the introduction of a nucleation layer.

Figure 64: AlN nucleation layer is adopted to lower the vertical leakage current. Taken from [5].

They proposed a solution to the problem of buffer leakage growing an AlN nucleation layer between the GaN buffer and the substrate. This solution introduces a polarization-induced charge dipole that bends the bands (see the band diagram in figure 64a.) and introduce a confinement barrier for 2DEG electrons to be trapped in the substrate. The nucleation layer effects can be appreciated in figure 64b where are shown the IdVg plots of gate and drain currents. We note that the presence of

the AlN layer reduces the leakage currents when the channel is not formed.

An extensive comparison among HEMTs grown on different substrates is performed in [42]. They tested devices grown sapphire, fre-standing GaN (FS-GaN) and Silicon substrate vs temperature.

In figure 68 are reported the Idb vs Vdb curves at varying temperatures for the three different based devices. We note that the sapphire based device presents the lowest current thanks its isolant substrate until $T = 250°C$; FS-GaN based device is quite stable at low voltages but presents the highest leakage current at high temperatures and Si-based device shows a leakage current growing with Vdb.

At $Vdb = 150V$ is calculated the Arrhenius plot for the three different based devices: Si-based device has two different E_a for low temperatures $\sim 0.1eV$, then $\sim 0.35eV$; the sapphire based HEMT shows an $E_a \sim 2.5eV$ only for $T > 250°C$ and for the FS-GaN based device it is $\sim 0.35eV$ with a linear behaviour.

These different behaviour suggests that the base mechanisms are different. The authors reproduced the current with a combination of resistive (hopping) and Poole-Frenkel mechanisms. They found out through simulations that the FS-gaN behaviour was well reproduced by the resistive-hopping mechanism, the Poole-Frenkel mechanism was well suited for the sapphire-based HEMT, instead for Si-based device was well fitted by a combination of the two.

The HV Idb vs Vdb has also been investigated (see figure 67) through simulations and experimental measurements according to their model mechanisms. They note that the Si-base device follows Poole-Frenkel mechanism uo to $\sim$ 250V and then seems a ohmic-like. In FS-GaN device occurred a destructive breakdown at 840V through an avalanche breakdown because of the dislocations and defects present in this substrate. The sapphire-based substrate present the largest non-destructive breakdown until 1100V (limit of measurements).

They performed even back-gating measurements and the results are shown in figure 68 where a non-simmetric forward/re-

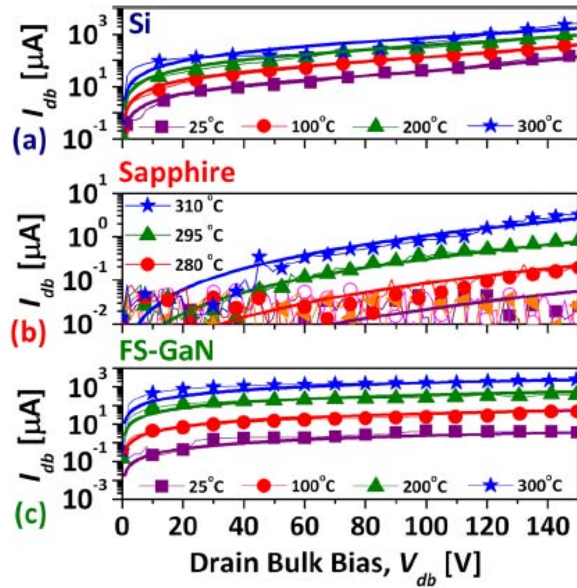


Figure 65: Comparison of the vertical drain-bulk currents at different temperatures for Si-substrate, sapphire and FS-GaN based devices. Taken from [42].

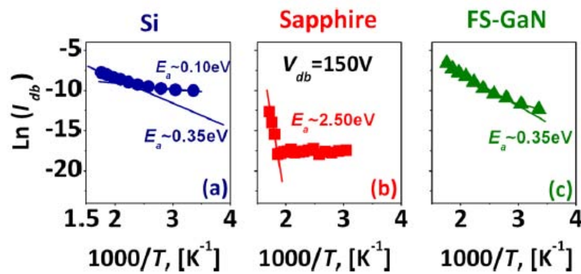


Figure 66: Arrhenius plot of the E_a of current at $Vdb = 150V$: measurements and simulations. Taken from [42].

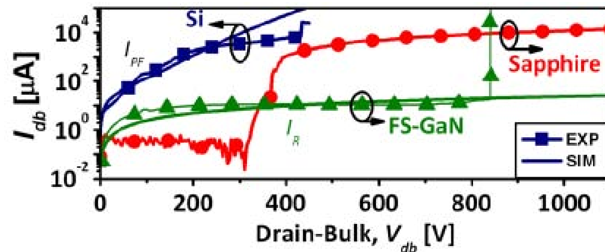


Figure 67: High voltage vertical drain-bulk currents for the three devices. Taken from [42].

verse bias behaviour is depicted for the Si-based device and sapphire-based device because of the different blocking band structures (they are shown in the figure on the right side).

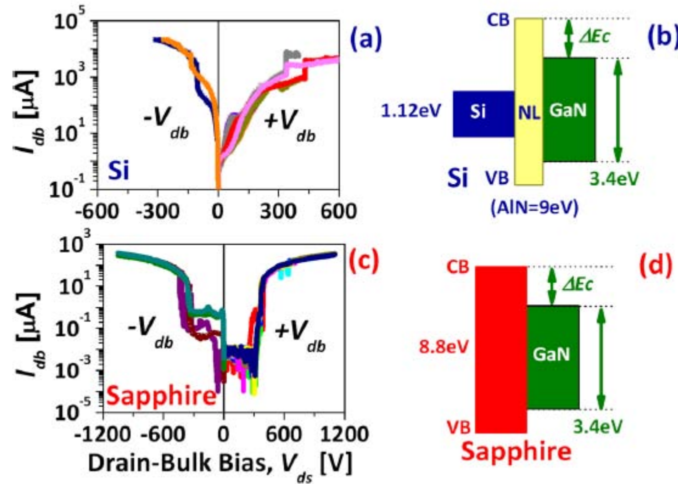


Figure 68: Comparison of the vertical drain-bulk currents vs forward and reverse Vdb applied for sapphire- and Si-based devices with they relative pictorial band diagrams. Taken from [42].

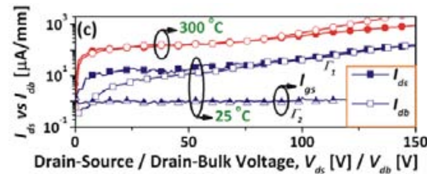


Figure 69: Off-state vertical breakdown measurement for Si-based device. Taken from [42].

Finally they performed an off-state breakdown measurement in Silicon-based substrate device (see figure 69). Because of the not-sufficient isolation of the GaN buffer from the substrate, there is a not negligible Ids leakage current which flows between the Silicon interface and bulk. They suggests that the Ids in the GaN buffer and the vertical Idb current are the main source of leakage. Other sources of leakage are electrons injected into GaN buffer and the tunneling leakage current at gate contact.

Finally we present two other articles about vertical breakdown phenomena [61], [60]. Both of them studied at the beginning the GaN buffer traps finding acceptor-like traps and donor-like traps. Then, they explain the breakdown behaviour through a space-charge-limited-current behaviour which involves

these buffer trap and high electric field in this region during vertical measurements.

The method employed in [60] to characterize the buffer traps is the thermally stimulated current spectroscopy (TSC): for this measurements they employed a test vertical structure (see figure 70). This method previews the device illumation for 20min through a white light at $T = 77K$ and biasing at $Vd = 1V$ in order to fill the buffer traps through photons (donor traps are filled with electrons photo-generated, acceptor traps are filled with holes photo-generated). Then the light is switched off and the traps are emptied by the temperature sweep (thermally emission of traps). When carriers are emitted, the TSC current signal (I_{TSC}) increases with temperature; on the other hand when the majority of traps are emptied I_{TSC} decreases. By this investigation they found three traps.

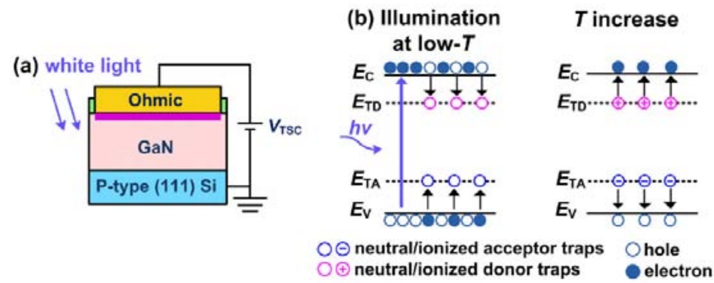


Figure 70: TSC setup measurement. Taken from [60].

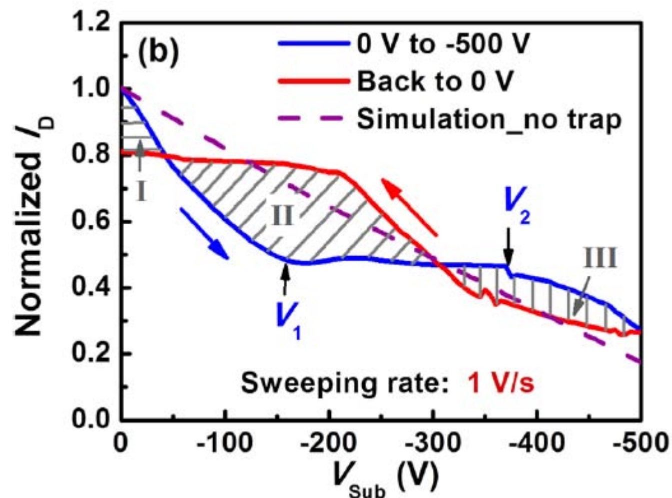


Figure 71: Back-gating measurement. Taken from [60].

In order to understand if donor-like or acceptor-like, they performed a backgating measurement applying $Vds = 1V$, $Vgs = 0V$, sweeping the bulk voltage $Vsub$ [2]. The result is reported in figure 71 with a simulation without considering the buffer traps (ideal case). The $Vsub$ sweep started from $Vsub = 0V$ to $Vsub = -500V$ (up sweep in blue line)and then back (red line).

By the plot, we note that the up sweep is faster than the ideal case because of the ionization of acceptor traps: they free holes hence they generate negative space charge. This partially deplate the 2DEG channel. After this first region, there is a flat one between V_1 and V_2, where the authors suggest that donor traps in the buffer are ionized (they emit electrons) generating positive space charge screening the increasingly negative $Vsub$ from depleting the 2DEG channel. In the third region of the up sweep, the Id decreases again.

In the back sweep the ionized acceptor and donor traps started to recover to neutral state (filling by the capture of holes or electrons). In region I and III the back Id is lower than in the up sweep. The motive might be that the deionization of the donor traps cannot follow $Vsub$.

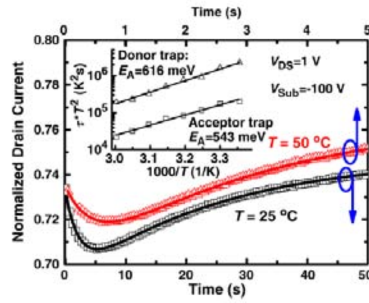
By this analysis they were able to say that one trap was donor-like and the other two are acceptor-like.

The last article presented in this section was made by Zhou et al. [61]: through a transient bakgating measurement they studied the traps located in the GaN buffer, later they performed a reverse and forward vertical breakdowm measurement in order to explain the mechanisms involved.

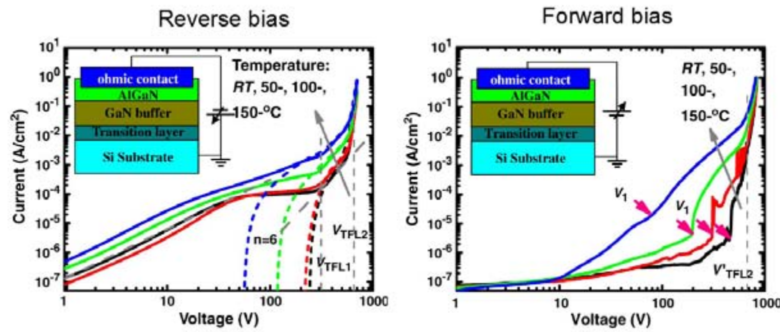
In figure 72a the Id transient measurement is reported. At the beginning they applied to an ungated AlGaN/GaN HEMT[3] a $Vd = 1V$, the source was grounded and the substrate bias switched from $0V$ to $-100V$. This measurement was performed at several temperatures. According to the authors, the decrease

2 The linear region bias is applied to eliminate the surface-states induced current-collapse and avoid device self-heating.

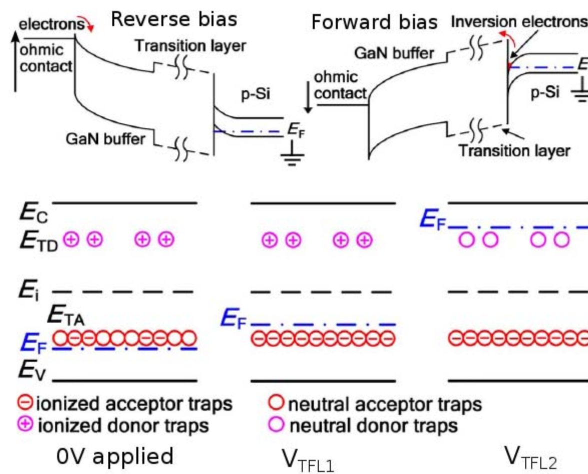
3 This was done to have a more uniform charge distribution along the 2DEG between the source and drain contacts.



(a) Transient backgating measurement and related Arrhenius plot.



(b) Reverse and forward vertical breakdowm measurement at varying temperatures.



(c) Physical explanation by means of band diagram at (a) 0V applied, at (b) V_{TFL1} when all the acceptor traps are ionized and at (c) V_{TFL2} when all the ionized donor traps become charge neutral by trapping electrons.

Figure 72: Measurements and physical explanation of the vertical breakdown in AlGaN/GaN vertical structure. Taken from [61].

of Id at the Vsub switch is due to the generation of negative space-charge in the GaN buffer by the ionization of the of acceptors traps, the emitted trapped holes deplete the 2DEG. The increase of the Id instead is related to the emission of electrons from the donor traps which give rise to a positive space charge region in the GaN buffer[4].

Later they performed a vertical breakdown in reverse and forward bias (see figure 72b). There are two temperature independent voltage at which there is a hump (V_{TFL1} and V_{TFL2}). According to the authors, at these voltage there is a trapped-filling-limit for acceptor-like and for donor-like traps respectively.

In the reverse bias curve, for $V < V_{TFL1}$ the logarithmic curve presents a slope of 1.8[5] and then decreases because at large bias electrons coming from the ohmic contact which acts as an electron reservoir, fill the acceptor traps reducing the current. At $V = V_{TFL1}$, the slope of the curve suddenly increases: a possible explenation is that at this voltage the acceptor traps are completely filled by electrons (see the band diagram in figure 72c). In the intermediate region, the slope is 6. In this region, the Fermi level is moved up and the donor-like traps are filled by electrons. At $V = V_{TFL2}$, the current increases with an higher slope because all of the donors traps are filled. Now the process is only driven by the drift.

In the forward bias, the electrons come from the parasitic channel between Si-substrate and the transition layer. We note that thermal energy is necessary to accelerate the process because they have to overcome the barrier (the first hump V_1 decrease as the temperature increases). Hence the leakage current in forward bias is lower than in the reverse. The second humps instead is temperature independent because it is related to SCLC mechanism which involve traps.

Therefore in this device, the SCLC model is the most suitable to explain the behaviour in reverse and forward bias because

4 Typically the number on acceptor-like traps N_A is greater than the number of donor-like traps [61].
5 The SCLC mechanism exibits a slope of 2.

of the presence of a donor-like and a acceptor-like trap in the GaN buffer.

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