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Corso di laurea in
ingegneria dell'informazione

Tesi di laurea

Transceiver for wireless communication at 60 GHz, prospects and realization

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Chapter 1

Introduction

The exchange of information has been very important in all human history. While in the past it was difficult, expensive and not instantaneous, from the invention of telegraph to now, thanks to information technology, the exchange of information has become very easy, instantaneous and definetely part of our life.
In the last decade, however, the way of exchanging information has been revolutionated by the increasing data rates available and the easiness of Internet connection thanks to wireless communication. Moreover the increasing popularity of portable devices and so the increasing consumer demand for high-definition media transfer, high data rates and the desire of untethered access to information have lead to a continous development of wireless communication devices.
The technological innovation has been also spurred by the allocation of new radio spectrum band by the FCC(Federal Communication Commission). In particular the unlicensed spectrum around 60 GHz "is of much interest since this is the band in wich a massive amount of spectral space has been allocated worldwide for dense wireless local communication"[16], as we can see from figure 1.1.

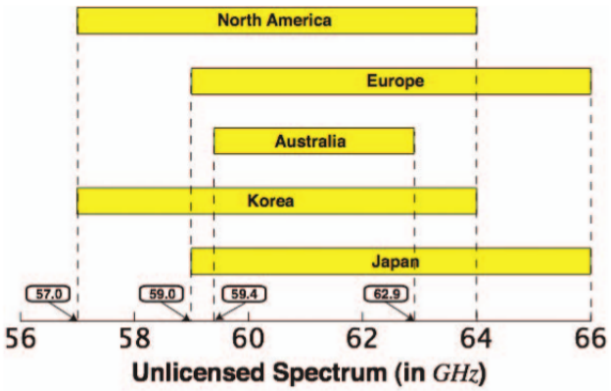

Figure 1.1: The international unlicensed spectrum

History teaches us which are the principal factors stimulating and allowing mass distribution of wireless communication devices. In fact when in 2001 the FCC allocated the band around 2.4 GHz the market of communication devices languished until semiconductor processes were ready for high-speed, low power components and the spectrum was regulated throughout the world creating a worldwide market. This fact resulted in the development of the wireless devices we are using nowadays.
Today the specrum around 60 GHz is more or less common worldwide and the semiconductor technology seems to be ready to support 60 GHz wireless communication devices(in fact the shrinking gate lenghts allows high integration and also the less expensive CMOS technology enable less costly devices) then it is possible to create a worldwide demanding market. Of course it is also essential to understand the applications that could be realized thanks to this new band.

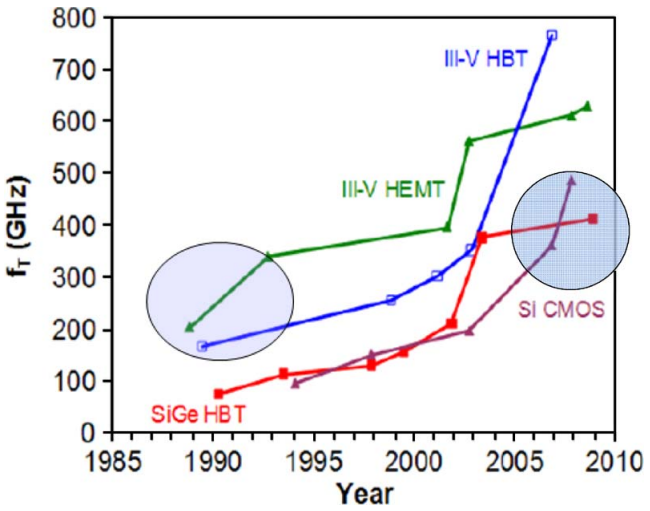

Figure 1.2: The last 20 years escalating frequency of semiconductors

First of all 60 GHz spectrum is so interesting because it will enable a WPAN(wirelss personal area network) capable of "massive data rates between portable devices, telecommunication infrastructure equipment and the cloud"[8]. In fact it is possible to forecast a future where informations will not be placed in the large hard disk drives of PCs but in the cloud or in other repositories thanks to the high data rates that 60 GHz wireless transceiver will be able to furnish. Another important and possible application is to use "low-power chip-to-chip communications"[8] to replace cables in the huge internet data centers in order to reduce power consumption. Moreover high definition video streaming, that is thought to be massively requested, will be a real possibility.
However many challenges have already to be solved or solution to these problems have to be improved. A difficulty for example is represented by the high attenuation that 60 GHz frequency propagation, but even other future higher band placed at 135,325 and 380 GHz, are affected. In particular

oxygen attenuation is very important and this fact will lead to short range wireless communication. Because of this problem the regulatory agency has designated 60 GHz band for future WPAN, with a range of about 10 meters. Wireless communication at 60 GHz is difficult to achieve for longer range since rain and fog attenuation becomes even more important than oxygen one. For this reason the research about 60 GHz propagation has been focused on short range communication, leading to a great number of information about indoor propagation and a lack of information about outdoor propagation. In order to make possible high data rates and long range wireless communication, it will be necessary to understand the outdoor propagation.

When the characteristics of propagation channel would have been understood, it will be possible to develop the fundamental device that enables 60 GHz communication: the wireless transceiver and all the devices that form it. Moreover it is very important to develop new strategies for "channel coding, data compression, interference mitigation, antenna beamforming, network addressing and spectral usage to take advantage of massive available bandwidths, lower power requirements of devices and the ever-present Internet"[8] in order to fulfill the expectations of "millions of 60 GHz communication devices produced and sold by 2015"[8].

This paper provides an overall overview about the state of the art of 60 GHz devices that form a wireless transceiver at this frequency.

At first it is shown a briefly description of 60 GHz propagation. After that it is simply described how a transceiver is composed and the various architectures that are employed at 60 GHz with the various differences between them.

Then all the most important devices that form the transceiver are described, explaining the challenges and the problems that the researchers have to face in order to obtain the most efficient components. Moreover the techniques developed and most employed at the moment for the solution of these issues are described.

Thus firstly it is described the power amplifier, the device that is maybe the more important and difficult one to design and that I deepened. There is an explaination of its role in the transceiver, a brief and simple theory of its peculiarity. After that the solutions that researchers have developed are described together with some examples of 60 GHz power amplifier realizations.

Finally all the other important components of a transceiver with their actual developments at mm-wave are depicted: antenna, trasmission lines, low-noise amplifier, VCO and mixer.

Chapter 2

60 GHz propagation

In order to obtain high data rates and utilize them for home applications such as video and audio transmission, one possibility is to use a large bandwidth like 60 GHz frequency is. In fact, according to Shannon's theorem, the channel capacity is proportional to the available bandwidth and so frequencies like 60 GHz are expected to achieve high data rates in the order of Gbps.
Anyway, according to Friis propagation rule, given a determined transmitted power, propagation attenuation is inversely proportional to the square of frequency, showing that 60 GHz radio is suitable for short range transmission.
In the following part a briefly explaination of 60 GHz propagation's main problems will take place, even if there is not the aim of going into deep details.
One of the main reason that determines the degradation of electromagnetic wave power is the absorption operated by the medium. Anyway, as said in [9], "various materials as papers, clothes, plastics, wood panels and leather are transparent to terahertz wave".
The real problems, instead, are carried by biological elements, since terahertz frequency range corresponds to the resonance frequency of various molecoles, making human body for example, an obstacle that absorbs very well subterahertz electromagnetic wave power. Also atmospheric gases have a great role on absorption, and so attenuation at these frequencies. In fact in [10], for example, it is said that "in frequency range of 57,5 GHz to 62,5 GHz in the lower part of the atmosphere the specific attenuation per Km due to oxygen is typically 14.7 dB/Km" making oxygen the main cause af attenuation at 60 GHz.
Another important factor of attenuation at mm-wave frequencies, especially in long range communication, is that due to rain/moisture. As it is possible to see in fig. 2.1 around 10^{10} Hz, so below 10 GHz circa, the attenuation due to oxygen and mostly to water is very low. With the increasing of the frequency, water attenuation becomes more important and at 60 GHz frequency has a great role since the attenuation due to absorption and scattering is high. This fact highly limits the coverage area of wireless transmissions

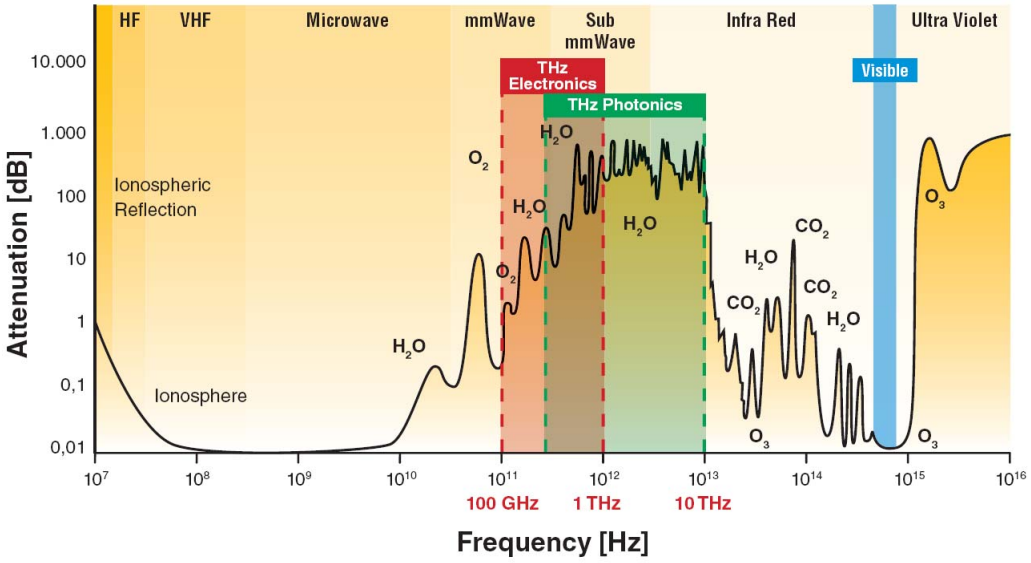

Figure 2.1: The signal attenuation at various frequencies and the corresponding attenuation main factor

at these frequencies.
Because of these problems in large scale propagation, researchers have been pushed to focus on inherently short range transmission in the 60 GHz band. This fact has lead to a detailed and numerous understanding of indoor propagation and attenuation at this band while outdoor propagation is not as much detailed.

Chapter 3

60 GHz transceiver module

As said before 60 GHz wireless communication and in particular 60 GHz WPAN are very close to be realized. The device that ensures wireless communication, sending and receiving informations, is the wireless transceiver. This one derives its name from the two parts it is composed of: the receiver(that is from the antenna to the ADC) and the transmitter(that is from the DAC to the antenna). As it is possible to see the ADC and the DAC are the two devices that divides the transceivers analog part from its digital part. Even though ADC and DAC are increasing their importance, because of their increasing sample rate(making this stage a difficult one to deal with), in this paper they will not be considered.

3.1 Superheterodyne architecture

In the realization of a transceiver it is alway necessary to cope with various problems and designers have always to make many choices. Nowadays wireless transceivers are widely utilized as the possibility and the need to access the Internet is increasingly important.
Therefore this need of continous connection to the web and exchange of informations is mainly done with portable devices thanks to the success of tools like the so-called "smartphones" and "tablet PCs"(like Apple iPad). Because of that, transceiver designers have to pay great attention to satisfy some essential specifics of transceivers: dimensions, power consumption and cost.
Considering all these characteristics, a designer has also to choose which architecture is the best to be utilized for the transceiver. In fact there are two architectures mainly employed for the realization of a wireless transceiver: *superheterodyne* and *homodyne*(also called *direct conversion*).
The former one is the most popular architecture utilized not only for the wireless transceiver we are talking about but for transceivers in general(it is employed for radios too). Although very old, heterodyne technique was first invented in 1902 and superheterodyne in 1918, it still offers the best performances of all different architectures.
Todays need of continously higher bit rate have lead to different ways of ex-

changing informations, from the low frequency of radio to optical fibers and WLAN. In particular this last technology uses radiofrequency to carry informations through different devices. However for actual WLAN the frequency employed is about 5 GHz and it can not be processed by any of actual processors. Therefore the idea that stands behind superheterodyne architecture is that of processing the signal in a fixed frequency, called IF(Intermediate Frequency), lower than RF in order to achieve the right gain, image rejection and bandwidth; finally the signal is demodulated and processed at a frequency called baseband, suitable for today processors. In figure 3.1 is possible to see a scheme of a wireless transceiver that shows the building blocks of this device.

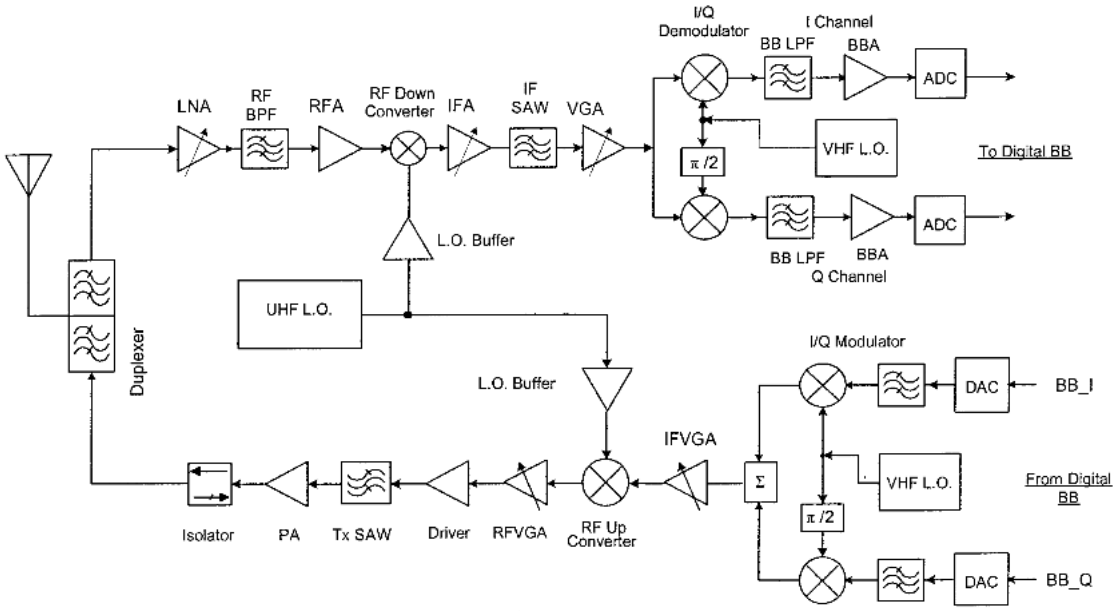

Figure 3.1: The scheme of a *superheterodyne* transceiver

The signal is first captured by the antenna and at this point its power is very low. For this reason after the antenna it is placed an important amplifier, called Low-Noise-Amplifier(LNA), that amplifies a bit the signal. Anyway besides this amplification,the great role of this device is that it does it "in the less noisy way" as it has a very low noise figure, and thanks to that it makes negligible the noise of the subsequent blocks. This last fact makes the LNA a fundamental device for a transceiver since a signal that has a low noise helps the correct decoding of the received informations.
After this stage the signal passes through some band pass filters, to reject the useless parts of it, and some other amplifiers. These are usually power amplifiers and they are other fundamental devices(even though the more important are the ones before the antenna in the transmitter part) because they have to amplify again the signal but more than what a LNA does. However it is necessary to make a distinction between the PAs at the receiver

and those of the transmitter since the amplification of the RF signal they perform at the receiver is not as high as the one of the transmitter due to different needs. In fact at the receiver the great part of signal amplification is done at intermediate frequency because at this frequency, lower than RF, is easier to highly amplify the signal and avoid great distortion doing that. On the other hand in the transmitter the signal sent by the antenna must have a great power(obtained through a meticolous link budget) in order to reach, in spite of the attenuation due to the propagation, other devices far from the transmitter.
The other fundamental devices after the amplifier are those that characterize the superheterodyne architecture: the mixer and the local oscillator. Indeed these two components are able to downconvert the signal from RF to IF and upconvert it from IF to RF. A mixer is usually a three port device capable of multiplying two signals and giving at its output the multiplication of the two inputs. In a transceiver the analog input signals are sinusoidal ones, the RF and that of the local oscillator, usually a VCO(Voltage Controlled Oscillator), that provides a sinusoidal signal at a stable frequency. The signal obtained is at a fixed frequency called IF, obtained by the difference of the two inputs signals(at the receiver).
In the IF stage(a transceiver could have even more than only one IF stage) the signal is filtered, so as to reject the image frequency, and of course amplified. However this amplification is done at a lower frequency than RF and so it is simpler. This is what makes superheterodyne a powerful architecture and the devices that perform the RF processes(antenna, LNA and PA) and those that perform the downconversion(mixer and local oscillator) are the fundamental transceiver devices.
The final receiver stage, after the IF one, is that of the signal demodulation and its shift to at baseband frequency, where at the end the signal is analog-to-digital converted by the ADC; finally it enters in the digital part of the device where it is processed.
Differently at the transmitter the digital signal is converted by the DAC(Digital-to-Analog Converter) then modulated and shifted to IF where it is first amplified. Finally the signal is upconverted to RF, amplified by the PA and sent to the antenna that performs the transmission.
Although superheterodyne architecture has many advantages, like the excellent selectivity and the high performances for example, it has some drawbacks too, as the high area that a superheterodyne transceiver occupies and its cost that is higher than other architectures since it employes various stages and devices for the up and down conversions.

3.2 Direct conversion architecture

A technique that is becoming "a very hot radio architecture"[11] being a serious alternative to superheterodyne, is homodyne or direct conversion architecture. Differently from superheterodyne in direct conversion the RF signal is directly downconverted to baseband and viceversa, without any

IF stage. For this reason this architecture is also called Zero-IF. Regarding superheterodyne direct conversion has some fundamental advantages: first of all it has less devices since there is not need of mixers and a LO for the IF stage. Moreover no expensive IF passive filters are needed as the signal is filtered in the analog baseband stage by active filters. these facts lead to another advantage of direct conversion architecture: its cost. Indeed it is less expensive than superheterodyne because of its need of less device to be implemented. Therefore this lack of complex circuitry leads also to a less area implementation, that is definetely an advantage as transceivers, as said before, are utilized in portable devices and their dimension has to be the smallest possible. Besides choosing homodyne architecture there is not need of managing the IF image frequency, the undesired frequency that derives from the downconversion and upconversion from RF to IF in superheterodyne devices. Finally in Zero-IF technique the transmitter has fewer issues than in superheterodyne and there are less spurious products, that are difficult to manage.
However direct conversion has some drawbacks too, that have made difficult its usage and they will have to be solved even at 60 GHz. In fact it has a strong susceptibility to the second order harmonics, it has a low isolation, so this leads to self-jamming, and RF filters are strictly needed for the rejection of adjacent channel.

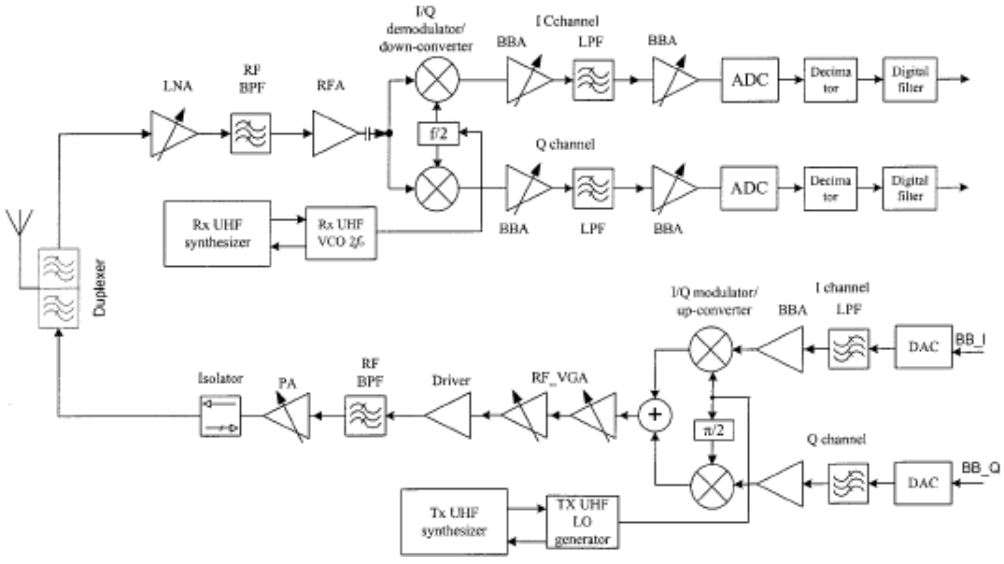

Figure 3.2: The scheme of a *direct conversion* transceiver

Direct conversion idea was first introduced in 1924 but because of its difficult implementation and challenges was not used until the '80s. In this architecture the receiver gain is achieved for the 75% in the baseband analog circuitry while in the transmitter it is obtained for 90% in the RF block, from the modulator to the PA. This fact leads to an important technical challenge that is the possibility of having a DC offset at the receiver, as the

signal is not always centered at zero value. Although both homodyne and superheterodyne suffer from this issue, in the latter it is easier to solve as the baseband gain is low. However the great issues proper of this architecture like the second order distortion, have made difficult the adoption of it for transceiver realizations.
Looking at what we said in the last paragraph it is clear that the choice of what kind of architecture is best for the RF transceiver is very important. In fact it is essential to choose the technique that better performs all the characteristics that we need for the transceiver. Therefore the designers usually have to evaluate the tradeoffs between simplicity and performances.

3.3 About 60 GHz transceiver

Concerning 60GHz there are some transceiver prototypes and most of them employ superheterodyne architecture because it is a technique more well-established. However, especially in the last 2-3 years, there are many prototypes that employ direct conversion, demonstrating how this architecture could be the future of RF transceivers.
In any case many are the challenges related to the devices that form the transceivers especially the ones that perform the most important actions in them.
Therefore it is clear what are the fundamental devices in a transceiver and these will be described in the next sections for 60 GHz realizations. Thus the **antenna** is essential for a correct reception and transmission of the signal, then another fundamental device is the **LNA** for the first signal amplification without the introduction of relevant noise. After that the other key devices, that represent the aim of the transceiver(thought as superheterodyne) with their up and down conversions, are the **mixer** and the **local oscillator**. Finally the other the other important device is the **power amplifier** that amplifies the signal before its transmission giving to it the correct power to satisfate the link budget analysis and reach the other receivers.
Apart from these key roles that these devices have for the correct functionalities of a wireless transceiver, they are also fundamental blocks since their issues regarding implementation, integration and research are essential for the realization of a transceiver particularly a an outstanding frequency as 60 GHz is.
For these reasons in the next chapters the speech will focus on these devices, with a more detailed attenction to the power amplifier.

Chapter 4

Power Amplifier

In the previous chapter we saw which are the main devices that forms a wireless transceiver and the specific role they play in transmission and reception. As these tranceivers are widely used in portable devices, their power consumtion is a really fundamental factor as it directly determines the battery life of the entire device. Indeed in a transceiver the power amplifier is the hungriest device in terms of power and so it has to be carefully realized considering the important power requirements.
Furthermore its importance derives also from the size it must have so as to keep as much compact as possible the transceiver; more important it has to satisfate the link budget analysis for an efficient implementation and function of the transceiver.
For all these reasons the PA is maybe the most important component for the realization of this device, even at 60 GHz where moreover challenges are enhanced by the high operating frequency.
In this chapter it will be first described what a PA is, its main factors, its component issues, its classification and finally some prototypes of 60 GHz PAs with the problems that affect these devices and some solutions that have been realized.

4.1 Power Amplifier description

An RF PA is a device that, given an input signal, amplifies its power level up to a desired value, taking the energy from the power supply. The purpose of the amplification is the achievement of the maximum output power.
The RF power amplifier is usually used to obtain a large output signal with a significant power from a low power input signal. Therefore it is utilized to drive antennas of transmitters and it is characterized by its high efficiency, good return loss and high gain.
Most of the transmitters have more than only one power amplifier and usually they are progressively larger in order to achieve the large power needed to amplify the low-power input signal. However this is only the simplest architecture(even though the most used) because sometimes it is necessary to disassemble and reassemble the signal in order to achieve linear

amplification.

4.2 RF PA properties

Linearity

The linearity is the most important paramenter of PAs as linear amplification is essential in order to give at the output the most accurate copy, even though amplificated, of the input signal.
As we will see a perfect linear amplification is quite difficult to achieve due to many issues related to the non-ideal components that forms the PAs and the need of satisfying other factors like good gain and stability. Sometimes a linear amplification could be obtained using a cascade combination either of linear and nonlinear PAs.
Because of linearity's importance it is necessary to be able of measuring it, with the result that many different ways of doing it were developed. Traditionally the measure of nonlinearity is achieved by C/I ratio(Carrier-to-intermodulation) that measures the difference between the amplitude of the third order harmonic and the one of the carrier signal. A typical C/I ratio value is about 30 dB.

Gain

The gain of an amplifier is a very important value since it determines, and it is, how the input signal is amplified. Indeed the gain is usually defined as the ratio between the output voltage(or in alternative power or current) and the corresponding output voltage(power or current).
Generally the gain of an RF PA is about 10-20 dB and it is strictly related to the transistor adopted for its implementation. In fact increasing the transistor sizes(the value $\frac{W}{L}$ for a MOSFET) the gain increases too. However this way of operating is most of the times inadvasible as the parasitic elements increase by the same value.
Finally it is necessary to say that the gain is also related to the class of amplification in which the PA operates.

Stability

Another fundamental property of a RF PA is its stability. In fact it is always necessary that unwanted and dangerous signals generated by instabilities affect and damage the device.
Instability could be produced in many ways, like cross-talk in the transmission lines or noise from the power supply. Moreover it can be very dangerous because at the frequency that could occur the instability, the gain could increase and reach such high values to saturate or even break the entire device. Therefore it is always important to careful design stabilization networks.

Efficiency

The efficiency in a RF power amplifier is defined as the percentage of DC power converted into RF power.
There are many different definitions for its evaluation, but maybe the most simply and direct is the so-called "drain efficiency", that is $\eta = \frac{P_{out}}{P_{in}}$. Anyway even though it is simply and useful this definition is not the most used because it is often necessary to take into account the RF power present at the input. Therefore it is defined the PAE(Power Added Efficiency) as $PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}}$(or equivalently by $PAE = \frac{P_{RFout} - PDR}{P_{in}}$ where P_{DR} is the power of the driver).
The efficiency of a RF PA is mainly determined by the class of amplification, as we will see later, and by the parasitic values that affect the device.
As the PA is the device that absorbs most of the power, it is important to obtain a high efficiency, so as to reduce the power absorbed by the biasing supplies, that means a reduction of the size of the power supply and a longer battery life. Moreover this fact leads to a less dissipated power and so lower temperature. Unfortunately, as we will see later in the description of the classes of amplification, a higher efficiency often results in a lower linearity and so higher distortion.

4.3 RF PA technology realization

In the realization of a RF power amplifier it is greatly important the choice of the technology that has to be utilized. First of all, as the amplifiers we are interested of are employed in portable devices, they have to be compact and small, making MMIC and RFIC the suitable technologies. Anyway the real important technology that with its choice makes a real difference is that about the transistor type that is utilized.
Historically RF devices have always been realized with compound III-V technologies, that are bipolar transistors like HEMT(High Electron Mobility Transistor), pHEMT and HBT(Heterojunction Bipolar Transistor).
However in the last years, the advances in silicon based technologies like BiCMOS, that combines CMOS and BJT technologies in the same IC exploiting the advantages of both applications, and CMOS are becoming the new more utilized components for the realization of radio frequency devices. This fact has occurred particularly for the incredible integration and cost reduction of silicon based technologies, but anyway we will analyse later the differences between bipolar and silicon transistors for RF applications. After that we will focus on CMOS technology and its employment in 60 GHz PAs.

4.3.1 III-V versus silicon technologies

When one has to design a PA he has to choose between various technologies of which III-V compound bipolar transistor and CMOS are the two more

important and utilized ones.
For this choice there are some values that better describe and help deciding which technology best fits in for our work.
These values are:

- the **transit frequency** f_T that is related to how fast the transistor can be operated. The f_T is defined in a MOSFET as the frequency at which the small-signal current gain of the device drops to unity while the source and the drain terminals are held at ground;
- the **breakdown voltage**(the minimum voltage that "breaks" the semiconductor, making it a conductor) that sets the power handling limits and affects linearity;
- the **thermal conductivity**. Indeed semiconductors change their properties with the increasing of the temperature, becoming more conductive. This fact affects the reliability of the device;
- the **cost** of the device;
- the level of **integration** of the device.

III-V compound technology devices are made employing mainly materials like Gallium-Arsenide(GaAs) and Indium-Phosphide(InP) as they offer high electron mobility and high transit frequencies. They have been the technology most used for RF power amplifiers since they were invented. Compared to silicon based technology, and in particular CMOS, III-V devices offer many advantages:

- higher transit frequency f_T that can be even about 200 GHz(for CMOS it is around 110-130 GHz);
- lower breakdown voltage that means lower power supply;
- better noise performances as they have higher current gain and f_T than CMOS;
- the current requires for a given f_T is lower than the one we would have employing a MOSFET;
- higher power gain than CMOS that results in higher PAE.

Anyway these devices have some fundamental disadvantages too. In fact their reliability is lower than Si devices as GaAs and InP substrates have lower thermal conductivity that directly affects the reliability as stated before.
In the last years it is increasing the adoption of CMOS technology for RF power amplifiers since III-V devices have higher costs and lower integration than CMOS. These two factors are really important nowadays because current portable devices need increasingly smaller and cheaper RF transceivers.

For these reasons, and so thanks to the progressively shrinking of Si transistors gate length(with the resulting increasing of f_T), Si devices have renewed their interest firstly for WLAN frequencies(2.4 GHz, 3.6 GHz and 5 GHz) and now they are thought to be the best choice for application at 60 GHz too.
So CMOS technology that is at the base of most of all the electronic devices and was not sufficiently considered in the past for RF implementations, it is now growing its popularity because of its high reliability, as it could directly integrate wit the baseband circuitry, and its low costs that allow the implementation for a broad consumer market.
Despite all these advantages, CMOS has some issues and challenges that become critical with the increasing of the operating frequency making their managment and resolution essential for 60 GHz applications too.

4.3.2 CMOS issues and challenges for mm-wave PAs

CMOS is the cheapest technology available not only for digital electronic, but in the last years for analog electronic too. Its continous scaling down dimensions, the related higher f_T and f_{MAX} and the gain high enough for 60 GHz, have made 130 nm technology and beyond available for 60 GHz transceiver implementation.
However many are the issues of CMOS technology regarding its employment for 60 GHz PAs implementation.
Firstly an important problem is CMOS low supply voltage since nowadays current CMOS supply voltage is 1 V and even below. Indeed we find that on one hand there is the important advantage of the higher operating frequencies and integration enabled by the continous transistors scaling dimensions, while on the other hand this reduction results in smaller channel lengths and thinner gate oxides that determine the breakdown voltage. This last fact results in a lower breakdown voltage and so in the necessity of using a lower supply voltage representing a great problem for the realization of CMOS power amplifiers. In fact a PA needs to have high voltage and high current in order to deliver high output power. Therefore if it is necessary to keep the transistor driving current high, the value $V_{GS} - V_{th}$(from which the drain current depends with V_{GS} the voltage between gate and source and V_{th} the threshold voltage) has to be kept high.
As the value of V_{GS} is decreasing due to the supply voltage reduction, a possible and adopted solution is to decrease V_{th}. Unfortunately the value of the threshold voltage could not be decreased too much because it is an intrinsic transistor value and more important its decreasing results in an increasing of the device's leakage current. This issue has not yet a proper solution but can only be "alleviated by performing an impedance transformation between the 50Ω load and the PA output"[22].

The most powerful and employed solution to this problem is that of increase the transistor width or the number of finger or both things. Anyway

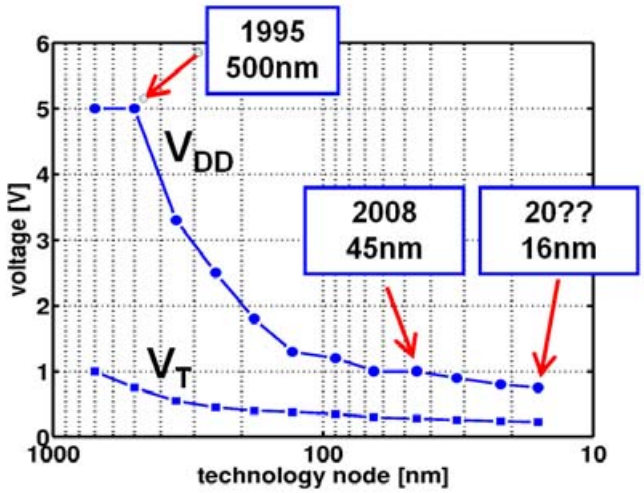

Figure 4.1: V_{DD} decreasing with CMOS scaling dimensions

the optimization of this solution results in a tradeoff between power gain and output power, representing another important challenge to face and solve in the realization of a 60 GHz PA.
Other problems that affect CMOS technology are its great process variability and some critical parasitic elements that are obviously enhanced while operating at such a high frequency as 60 GHz is.
An issue that has always a great relevance, and more important at 60 GHz is the exact knowledge of how active devices behave and how the parasitic elements are distributed at the frequency we want that our PA operates. Therefore it is becoming increasingly complex and important to develop transistor models at mm-wave frequencies so as to implement in the best way power amplifiers having accurate simulations.
In fact at 60 GHz the resistive losses are very high and active devices gain is quite low such that the specifications are barely fulfilled. Moreover at these high frequencies f_{MAX} factor is really important but it is directly determined by the transistor and the bias, but it highly depends on the parasitic values too. Actual CMOS are designed for operations around 10 GHz and all the accurate models developed for this frequency too. Anyway actual 90 nm CMOS devices can be used for 60 GHz operations but efforts for the development of accurate models have to be made. Indeed substantial differences between the real and the simulated performances result in circuit failure. Therefore models are needed because if we want to push the performance limits of active devices, and at 60 GHz it is compulsory for gain need, it is necessary to develop a careful design and layout.

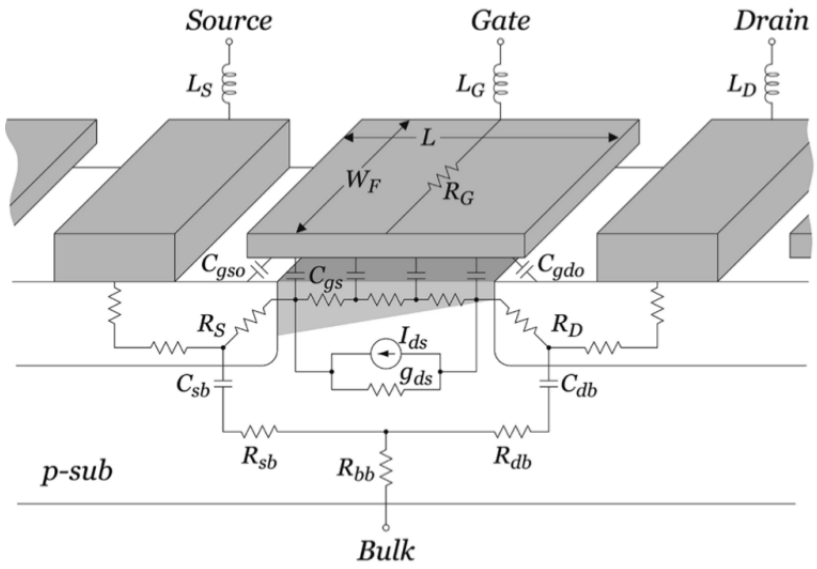

Figure 4.2: A simple model of a NMOS finger

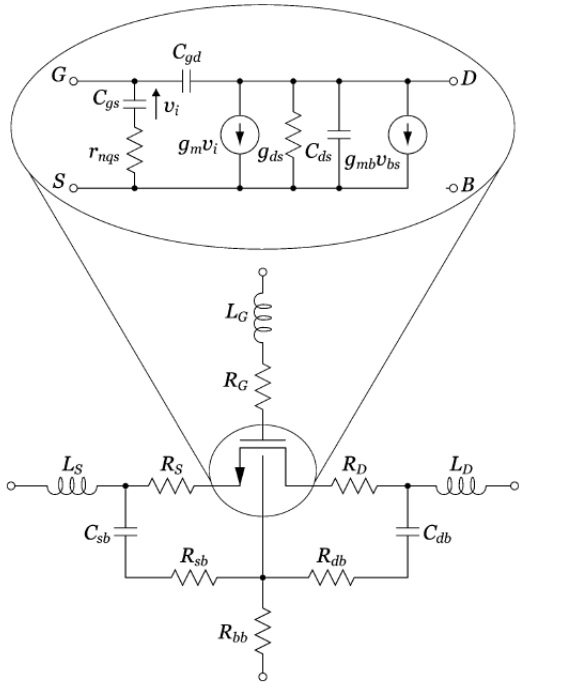

Figure 4.3: A CMOS small signal model at mm-wave frequencies

4.4 Classes of amplification

Before going into the description of the various problems of Power Amplifiers and the different architectures that can be used to face some PAs' problematic of 60 GHz transmission, it is advisable to see a bit of PAs theory.
Usually Power Amplifiers can mainly be subdivided in two types reflecting

their class of amplification:transconductor type amplifiers(Classes A, B, AB and C) and switching type amplifiers(Classes D, E and F). In the former amplifiers the transistor is used as a current generator, with the bias that determines the conduction angle, so linearity and efficiency. In the latter instead, the transistor is used as a switch, apart from class F amplifiers that despite being non linear amplifiers, they use a transistor as a current source as in transconductance classes.
All these classes differ from each other in method and even in their power output capability, that is define as the output power produced when the device has a peak collector voltage of 1 V and a peak collector current of 1 A. As power transistors are expenisve, designers have to use them as close as possible to their maximum voltage and current ratings; so the more higher is the power output capability, the less expensive is the practical implementation.
The type of bias applied to the RF Power Amplifier determines the class of amplification. So choosing the adeguate bias point of the PA can determine the level of possible performances that can be obtained with that device. Doing this it is possible to evaluate the tradeoffs between all the important parameters of the device: linearity, efficiency and gain.

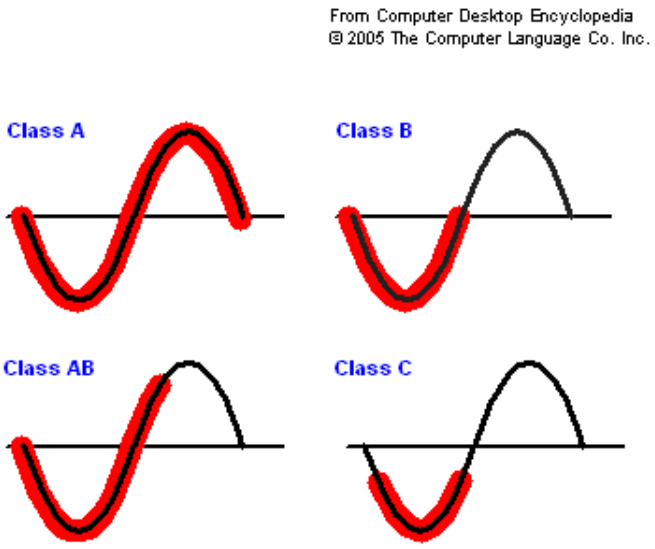

Figure 4.4: In this figure is possible to see the difference between the main classes related to the different conduction angles

4.4.1 Class A

In class A operations voltage and current are constant and large enough to ensure that transistors remain in the active region and act like a current

source.
The voltage is biased exactly in the middle between the cut-off voltage and the saturation voltage.
The theoretical efficiency of a class A power amplifier is 50% at PEP(Peak Envelope Power, that is the mean power measured at the crest of modulation during one RF cycle) and due to that the instantaneous efficiency is proportional to the power output while the average efficiency is inversely proportional to the peak-to-average ratio.
Class A amplifiers have the advantage of being very easy to implement, as they require only one transistor,
Class A PAs are inherently linear, have the advantage of being very easy to implement(as they require only one transistor), have the highest gain of any PA and can be used very close to the maximum operation frequency of the transistors. Unfortunately an amplifier biased in this class of amplification is very inefficient and is always conducting, resulting in a great waste of power and so a higher power consumption. Despite their low power, class A PAs are used for applications that need high linearity, high gain and high frequency.

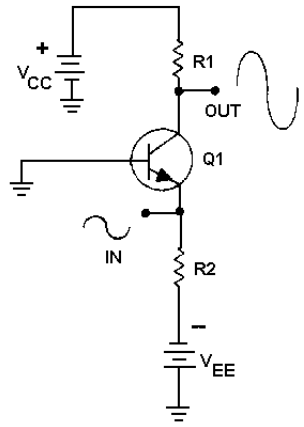

Figure 4.5: A simple class A amplifier

4.4.2 Class B

Class B Power Amplifiers are biased in such a way that they only amplify half of the input wave circle and this is achieved setting the gate bias at the threshold of conduction. A single stage class B amplifier would be non linear so the solution applied for this class of amplification is the adoption of push-pull transistors where one works for positive input signals and the other for negative input signals. So every transistor works for half period of the sine wave, that would be rebuilt at the output.
Differently from what happens in class AB PAs the quiescent current(that

is the current that flows in the circuit when no signal is applied) is ideally zero. This means that the istantaneous efficiency is 78,5% at PEP and for low level signals are higher than class A.
Since class B operation provides linear amplification it can be used for all RF power amplifiers without severe linearity requirements.

4.4.3 Class AB

In the previous two sections two linear classes were described with two different particularities:class A has a good gain but a poor efficiency while class B has a better efficiency but a poorer gain. A class of amplification that combines the advantages of both classes is class AB.
In class AB amplification the collector voltage is constant and the collector current, when the circuit is not amplifying or driving the load, increases with drive power. The AB amplifier conducts for more than a half period of the sine wave(that of class B), but less than 360 degrees(that of class A). Its maximum efficiency is 78.5% and the gain lays between the one of class A and the one of class B type of amplification.
This class of amplification gives an output signal more distorced than class A, but more linear than class B while its efficiency is between the one of these two classes. Because of that it is used for operations similar to class A that have less severe linear requirements.

4.4.4 Class C

In class C operation the amplifier allows conduction less than a half of the RF cycle and the transistor gate is biased below threshold.
In this way efficiency is increased compared with the precedent classes, but unfortunately distorsions are introduced. This fact makes class C amplifier non linear. RF transmitters operating at a single fixed carrier frequency is more common application for class C amplifiers distorsions can be controlled by a load that tunes the signal.
Ideally the efficiency of this class of amplification is 100% but to achieve this is necessary to have a conduction angle of zero degrees, that in practical is impossible since it causes the decreasing of the output power that becomes zero, and the increasing of the drive power to infinite. Moreover with a conduction angle next to zero degrees also the gain drops to zero. Proper class-C conduction angle is around 150 degrees that gives an efficiency of 85%.
Class C operation is not recommended for bipolar transistors as it shortens their life. However, in general, it is little used for solid-state power amplifiers at higher or microwave frequencies because in these devices the major problem is the large negative swing of the input voltage, which coincides with the collector/drain output voltage. For any transistor this is a very bad condition for reverse breakdown as even a small amount of leakage current really affects the device and the efficiency. As we have seen, for classes A/B/AB/C

the input waveform is kept sinusoidal so the amplitude is limited to $\frac{V_{dd}}{2}$. This fact is essential since efficiency can be improved only controlling the current and so large current is needed to deliver power. However class C amplifiers have a very poor gain and this fact limits their adoption in particular for frequencies higher than 1 GHz.

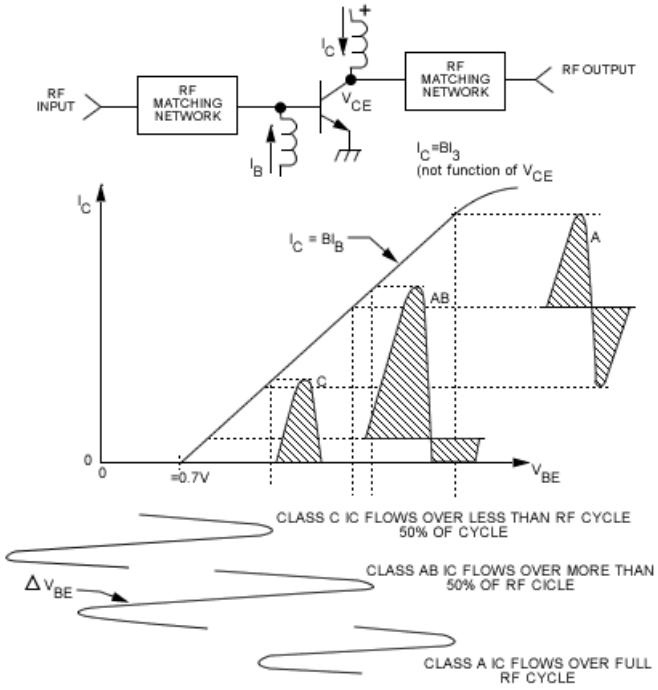

Figure 4.6: Current and voltage in different classes of amplification

4.4.5 Class D

A class D amplifier is a particular device called switching amplifier. This thing is due to the fact that two or more transistors are used as binary switches to generate square drain-voltage waveforms. A particularity of this class is that the modulation used is mainly pulse width modulation and due to the constant amplitude of the output signal, transistors are always completely on or off and so high power efficiency can be achieved. In fact its efficiency is ideally 100% since the current is drawn only through the transistors that are on.
However in practical usage of class D power amplifiers they are affected by losses due to drain capacitance, saturation and switching speed and these facts result in a efficiency less than 100%. Moreover it is decreased also by the series resistances of the switches. These resistances, anyway, could be reduced increasing the area of the switching transistors. Doing this unfortunately, increases the parasitics that affect the amplifier and limit the

operating bandwidth making class D amplifiers suitable for low frequencies and less utilized for high frequencies like 60 GHz is.

4.4.6 Class E

Class E amplifiers use a single transistor that acts like a perfect switch and an output network designed for the minimization of the power dissipations due to the non ideal transistors. In optimum class E devices the drain voltage goes to zero when the transistor turns on. A result of this fact is that the efficiency is ideally 100%. Moreover the problems of class D amplifiers are solved since, with a single transistor, the losses due to the charging of the drain capacitance are eliminated, the switching losses are reduced and there is a good tolerance of component varations(that are frequent in CMOS technology). Only a critical fact remain, that is the high drain voltage that the transistor has to face when the transistor turns off.
Because of the efficent operations that class E amplifier could afford even with the high parasitic drain capacitance, this device is used in high efficiency RF power amplifiers for switching.
Since the switching time at high frequencies becomes comparable to the duty time this type of PAs are largely used at these frequencies and we will see that at 60 GHz some research on class-E power amplifiers are made.

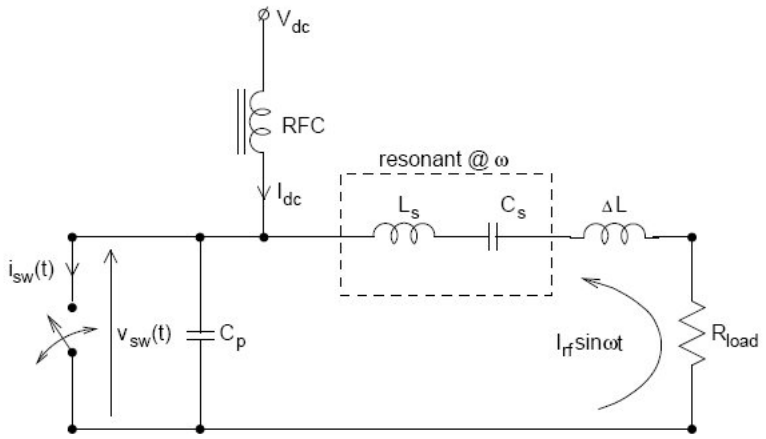

Figure 4.7: A simple class E amplifier

4.4.7 Class F

Class F amplifier is another type of switching amplifier that can improve both efficiency and output power. In fact the transistor is utilized as a current source, like in class A, and a output network placed between the drain

and the load. This network modifies the sine wave making it a square wave in order to reduce the dissipated power. This result is achieved adding a series of resonators in the output network to open-circuit the drain of the transistor at several odd-harmonics. So thanks to these resonators the output increasingly resemble a square waveform, since the odd voltage harmonics tends to flatten the top and the bottom of the input waveform. This flattening increase the efficiency since it decreases the voltage across the transistor during its conduction time. So, in the case of a perfect square output wave, the efficiency can reach 100%.
However, compared with class E amplifiers, class F have some disadvantages, as having a circuit implementation more complex and the operating switching frequency is limited by the limited number of harmonics, apart from the intrinsic switching speed of the active device.

4.5 60GHz PA realizations

In the last paragraphs we have seen the various classes and types of amplifiers and we analysed the advandages and drawbacks of each of them. In this one, instead, we will describe the problems, difficulties, solutions and choices that designers usually have to face in the realization of a RF power amplifier.After that we will see, together with some examples of realizations, all these problems related to 60 GHz PAs and all the other issues that have to be solved at this outstanding frequency.
Thus when it is necessary to realize a power amplifier for a transceiver, the designer has to choose between different configurations and has to decide which one is the most suitable for his device.
Obviously a power amplifier realization project results particularly difficult since the designer has to manage with different specifics. In fact a PA must have:

- high output power;
- high efficiency;
- high gain;
- low distortion;

while specifics like high efficiency are better fulfilled by nonlinear classes of amplification and other like low distortion by linear classes, simply explaining how the needs result in difficult choices.
Regarding the achievement of a high output power, it is very important, at first, to have an input output match at small signal. It is also important that the load lets the maximum excursion of drain voltage and current. Anyway there are also very important and utilized techniques that allow an increase of the output power, like:

- increase the breakdown voltage. Unfortunately this solution can not be taken seriously into account for our usage since the increasing of the breakdown voltage means an increase of the power supply too, thing that is highly unproposable as RF PA are needed for mobile devices transceiver in particular.
- increasing the output power it is very important not to introduce new parasitic effects and maintain good thermal properties that otherwise would affect the power amplifier role.
- increase, as said before, the maximum drain current.

This last technique is in particular the most utilized one, even in 60 GHz PAs prototypes that have been realized since now. Anyway in order to increase the maximum drain current, it is necessary to modify the gate area. This can be done in two ways, and each one carries a different result: increase the number of fingers(that is the number of different parallel transistor gates) or the gate length. Unfortunately adopting the former solution results also in an increase of the gate resistance and, beyond some values, it affects the gain and the PAE, decreasing them. Using the latter, instead, it is possible to obtain smaller gate resistance values and better thermal properties, while unfortunately parasitic values due to the link between the cells are introduced.
However the gate cannot be increased undefinetely, since beyond a certain value, the power reaches the saturation, so the gain sees a reduction.
Looking at the realizations of last years it is possible to notice how the values of the gate area, and so the number of fingers and the gate length value, are always carefully chosen and adapted to the architecture of the amplifier. Thus in [7] for example, the optimal device width is chosen to be $40\mu m$ with 40 fingers while in [6] we can see how the architecture influences the parameters choices. In fact the power amplifier is here realized with a cascode architecture(that will be described after in the paper) and for this reason the number of fingers is different in the two stages of the cascode because the second stage is larger than the first one in order to optimize the gain and the output power; for this reason the width is chosen as $1\mu m$ and the first stage has 63 fingers while the second has 150 fingers.
The other important factor that a designer has to cope with is the power amplifier efficiency. In fact as the PA is in the entire transceiver the device that absorbs the most quantity of energy from the power supply, there is the need of achieving the highest possible efficiency in order to keep low this power absorption. Therefore to a higher efficiency corresponds lower power supply dimensions, longer battery life and moreover a lower temperature, that means higher reliability. Summing up, all these specifics have to be satisfied in the development of a power amplifier and at 60 GHz it is even more difficult to do that since higher frequencies enhance the problems we talked about.
In this context the shape of the amplifier has to be carefully chosen and in the same closely way it must be done for its class of amplification. In

this choice it has to be taken into account also the type of modulation used for the transmission, but as it is possible to see from the articles we will mention, gain and efficiency play the most important role in this choice.
Therefore choosing one of the transconductance classes(A, B, AB, C) gives a good gain but on the other hand a poor efficiency. Instead using a switching class type(D, E, F), lets the achievement of a good efficiency but not a great gain. Moreover, differently from the other linear classes, nonlinearities are introduced, that means the generation of multiple harmonics and so a bigger distortion. The control of this distortion results in a tradeoff regarding the maximum achievable efficiency, but we will see some linearization technique utilized even at 60 GHz, next in this paragraph.
Firstly it is advisable to see some realization at 60 GHz with the technique employed for mm-wave power amplifiers. Although the research in the 60 GHz band is quite new and CMOS PA challenging, in the last years we can find a lot of research prototypes of 60 GHz PAs in CMOS technologies, BiCMOS and someone in bipolar too(employing HBT in general).
In order to show how CMOS is utilized and look how the problems we spoke about are solved, we will propose some interesting realizations.
Therefore if we try to understand what is the class of amplification preferred for 60 GHz PA we see that obviously there is not a unique solution. In fact in some realization, switching classes are utilized, priviledging the efficiency, and so the lower power consumption, with the result of a less linear amplification and the necessity of using specific techniques in order to decrease the distortions.
Thus looking for some 60 GHz prototypes, it is possible to find a class-E PA of 2006 using BiCMOS technology[1]. The usage of a class-E PA topology is very interesting for what concerns the efficiency of the device, as in fact it has ideally 100% efficiency. Anyway, as the researcher says in the article, "very efficient class-E operation demands that the active device operates as a switch with a turn-off time significantly smaller than the signal period as well as accurate termination of the harmonic components. Both of these requirements are difficult to meet as the operating frequency of the amplifier increases and approaches the f_T of the employed device"(with f_T that is the cutoff frequency).
For these reasons the adoption of a class-E amplifier is quite difficult at 60 GHz and so for the realization of the more recent years class-E doesn't have many space since there are employed more linear typologies as classes A,B and AB[2][3][23]. This fact is due to their linear behaviour that is thought to be more important than high efficiency as at such high frequencies as 60 GHz, distortions are frequent if not compensated. Obviously a lower power consumption(that derives from an high efficiency) doesn't have any utility if the signal is highly distorced and more power needs to be used to compensate these distortions.
Moreover most of these recent realizations in CMOS and BiCMOS(and even some realized in bipolar technology) employ more than only one stage. For example in [2] there are two stages of amplifiers, a main one operating in

class-A and an auxiliary one operating in class A, AB or B in order "to allow greater efficiency of the PA to be treated for better power handling capability".
Anyway the topology that is more employed with these linear classes is cascode. In fact there are a lot of realizations, most of them quite recent, that employ this topology. In [4], for example, a 3-stage power amplifier is employed, with two cascode stages, in order to achieve higher gain, and a final common source stage, for maintaining a good efficiency.
Also in [5] it is employed a four stage PA where the first and the second stages are in cascode topology, with the first stage, the common gate, used to obtain a better isolation and so higher stability in the entire band of utilization, while the second stage, the common source, is used to obtain high linearity, together with the third stage that is a common source too. In the final stage "two 40x2μm devices are connected in parallel and power combining is achieved [...] which ensures device output impedance loading to be in the maximum output power region".
Other examples of cascode utilization using CMOS are employed in [6], in [7] and in [8] but there are a lot of other application examples of this old architecture employed for the realization of 60 GHz power amplifiers.

Cascode topology

The classical cascode topology, that we spoke above, is made of two stages in cascade, one common source for FET(common emitter for bipolar transistors) and one common gate(common base for bipolar transistors). This configuration has a lot of advantages, most of all they are very interesting in the band that we are analysing.
Cascode was first invented for reducing and eliminating the Miller effect. Since the upper bound of the band is given by the base input total capacitance (base-emitter capacitance plus Miller base-collector capacitance), this configuration ensures a wide band of utilization. In fact the gain between base and collector(gate and drain) in the first stage is very small, because the emitter resistance of the second stage transistor is small. So the Miller terms are small too while with a single transistor it could be more than ten times bigger. Because the resistance seen from the input is mainly the same it results that the band upper limit is higher than a common emitter topology. More than this fact of the band, cascode ensures higher stability and especially high gain, due to the final common gate stage, and high input impedance, due to the initial common source stage.
Analysing cascode configuration, as we will see in [8], "at lower frequencies the main reason of using cascode is the higher gain". However increasing the frequency is possible to see that above 30 GHz the cascode device is unconditionally stable.

Returning to our problem, as we said before 60 GHz PAs have to be linear or near linear, and this fact depends also on the modulation employed, that, at the moment, are OFDM and SC-FDE(that requires a less linear PA compared with OFDM).
Anyway the efficiency of the PA is very important and, as said in [8], "there are many potential ways of improving the efficiency of linear or near linear PAs" and the best ones are Doherty architecture, envelope tracking, self biasing and power combining. These techniques are all efficiently used at low frequencies and have to be better investigated and developed at mm-wave frequencies.

4.5.1 Linearization and efficiency enhancing techniques

As we saw in the last paragraph a lot of prototypes are realized preferring the utilization of the so called linear classes, that provide a linear amplification obtaining unfortunately a poor efficiency. Efficient RF power amplifiers, however, are more adeguate for battery devices, since power amplifiers dominate the power consumption of portable devices. For this reason in modern mobile phones transceivers and WiFi tranceivers too, the use of nonlinear PAs(class E and F in particular) is obtaining more and more success. In fact these classes are able of assuring very good efficiencies(theorically 100%) but with the drawback of nonlinear amplification and distortions that we saw before. Therefore these nonlinear amplifiers could be a great choice for 60 GHz PAs too, but of course solutions for the nonlinear behaviour have to be developed or however some other existing techniques should be improved. On the other hand there are also other techniques that are used instead for the increase of the efficiency of power amplifiers that utilize linear classes of amplification(that as we saw have a good linearity but the drawback of a poor efficiency).

Doherty architecture

Doherty amplifier was realized for the first time in 1936 by W.H.Doherty. After many decades being dormant, this type of amplifier in the last ten years has become the "amplifier of choice" for wireless transmitters.
Classic and most used implementation consists of two amplifiers, a carrier amplifier, biased in class B or AB, and a peaking amplifier. The input signal is split so the difference between the two amplifiers' signal is 90 degrees.
For low voltage level the peaking amplifier is turned off while the carrier one reaches its peak and delivers maximum efficiency. As the voltage level increases the carrier amplifier continues operating at its peak while also the peaking amplifier turns on and reaches another peak point, increasing in this way the efficiency of the total amplifier.
At lower frequency Doherty technique is difficult to integrate due to the long transmission lines, while at mm-wave frequencies this problem increasingly reduces and so it is possible to see in this technique an efficient one

to apply at 60 GHz. In fact it is possible to find many realizations at lower frequencies(the ones used for actual WLANs). At 2.4 GHz for example with a Doherty amplifier is possible to reach 14% PAE while at 60 GHz could reach 3% PAE[8].
In conclusion it is possible to say that this technique has to be deeply investigated at 60 GHz, especially because it increases both efficiency and linearity, two fundamental characteristics of a PA.

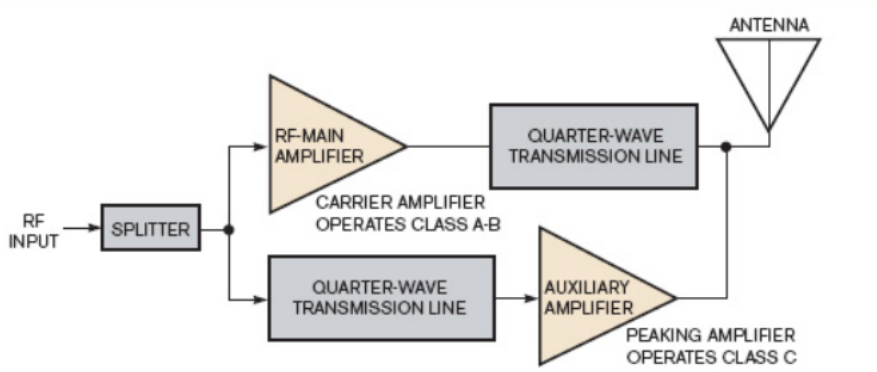

Figure 4.8: A simple scheme of Doherty amplifier architecture in which is possible to see the peaking amplifier and the carrier one with their usual classes of amplification

Envelope tracking

Envelope tracking technique(EER, envelope elimination and restoration) is used to increase the linearity of PAs. In fact as nonlinear devices are widely used for WLAN transceivers in order to achieve efficient amplification, then there is the need of linearize the operation so as to avoid distortions and mismatchs. At mm-wave frequencies too, there is the need of achieving power amplifiers with high efficiency is very important, and nonlinear classes of amplification are a possible successful solution. Anyway there is also the necessity of a linearization of the operation mode and EER is a possible technique that has to be deepened at 60 GHz.
As it is suggested by its name, envelope elimination and restoration technique consists in a first elimination of the RF input by a limiter, in order to generate a costant amplitude phase signal. More simply, the magnitude and the phase of the input RF signal are splitted, that is the magnitude is extracted by an envelope detector while the phase is obtained by the limiter. The two components of the input signal are then separately amplified and finally combined together, obtaining the amplified RF output as we can see from the block diagram in fig.4.8.
Another way of implementing EER is the use of a switching power supply and that is also the solution described in [8] for 60 GHz applications. It

consists of a supply modulator that acts varying the supply voltages of the amplifier in order to keep it near saturation. This is a very useful technique, especially if applied to non linear amplifiers in order to achieve linear amplification. In fact non linear amplifiers are more efficient when they operate near saturation, since they conduct current only for a fraction of time.
Moreover this technique could be used combined with Doherty architecture and this solution is very attractive as together they can perform linearization and efficiency enhancement. Anyway even this technique has to be more investigated at mm-wave frequencies since there are a few examples of application.

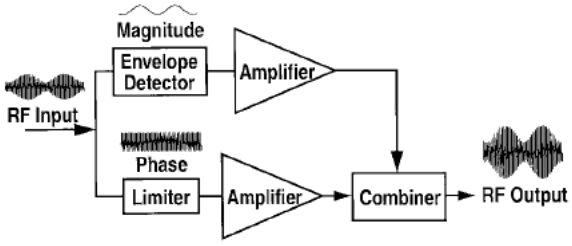

Figure 4.9: A simple scheme of envelope elimination and restoration technique

Power combining

Power combining the output of several power amplifiers is another technique that is used in the realization of PAs for wireless transceivers.
Realizing a PA it is obvious that important choices have to be made, especially if it is better to use a number of small PAs(that offer high gain, better phase linearity and lower cost, but they are hard to assembly) or one larger PA. In the case of using many small PAs power combining is a very important technique for the right combination of the outputs. Even this technique is sometimes used together with Doherty architecture and the combination of the Doherty PAs' outputs is achieved with power combining in order to have all the advantages of a Doherty amplifier.
Power combining is also used for antennas and "off-chip power combining is possible through correcly on-chip antennas"[8]. On-chip power combining is difficult at 60 GHz due to the limited output powers of indivifual components and so even this solution have to be improved.

Self-biasing

The last technique that "merits more investigation at mm-wave frequencies of 60 GHz and above"[8] is self-biasing. We saw before the EER technique for linearization enhancement and this type of techniques are more present

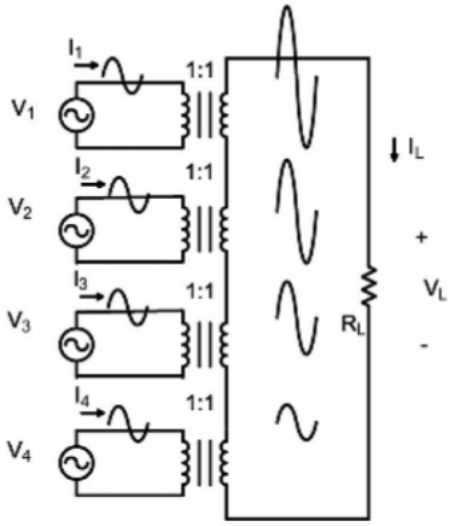

Figure 4.10: A simple explaination scheme of power combining technique

in the development of last years power amplifiers. Similarly to envelope tracking, self-biasing acts controlling the voltage supply and bias of the transistors and the components that forms the PA. Thus it is present a circuit that senses and corrects the bias, and so the voltage applied to the MOS, in order to achieve a more efficient operation mode. As an example in [23] self biasing technique is utilized in a cascode amplifier. In fact self-biasing is used in it to optimize the output power and the efficiency dividing in the most optimal way the voltage swing across the common source and the common gate stages. Since the output power and the efficiency are functions of the supply voltage, it is clear how this technique resembles EER. Obviously it can increase efficiency and furthermore reduces hot carrier effects.
Despite being a quite new technique even at low frequencies, self-biasing has shown good results in its applications. For these reasons it is a technique that could be useful at 60 GHz too, a frequency at which in any case its efficiency have to be verified.

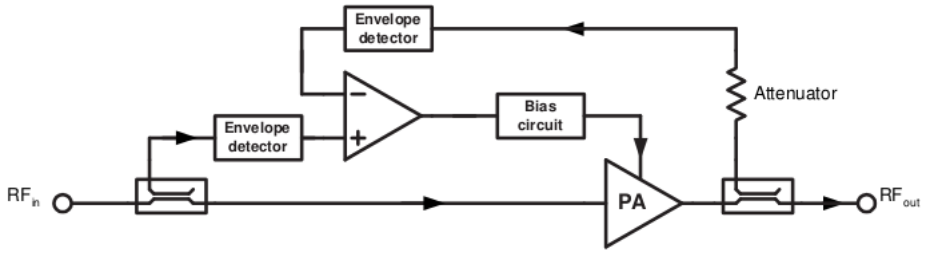

Figure 4.11: A scheme of self- biasing technique. As it is possible to see the architecture is similar to EER one

Chapter 5

Antenna

As it could be obvious the antenna plays a very important role in a wireless transceiver. In fact it has to convert, without significant distortion, the electromagnetic field that propagates in the air, into a suitable RF signal either in transmission and in reception.
Moreover in todays technology, filled of portable devices, power and space are more and more important and so also antennas should not consume too much power and occupy too much space.

60 GHz antenna trends

Thinking about modern transceivers we know that they operate at frequencies of 2.4/5 GHz. These operating frequencies mean that informations are carried by signals with wavelengths of some centimeters. At 60 GHz instead, the wavelengths are of some millimeters, resulting in the development possibility of smaller and more integrated antennas. Thus the antenna form factor at mm-wave frequencies is on the order of millimeter or less, and for this reason on chip or in-package antenna are becoming the new innovative architectures since "the possibility of integrating and combining antennas direcly on chip is one of the least explored areas for future subterahertz communication devices"[8]. Moreover innovative techniques like micromatching and proton implantation process are viable for the reduction of the silicon substrate losses and so for the increasing of the efficiency of the antenna. Anyway these techniques are quite expensive and so their utilization have to be carefully considered since they result in a more expensive final solution, that is a drawback as these transceivers are thought to be for mainstream diffusion.
Nowadays on-chip antennas are seldom utilized because of their low gain, low efficiency and high losses. However if would be possible to develop high directional on-chip antennas then these devices will have higher gain and efficiency but more important they will have lower costs and higher design flexibility than actual off-chip antennas.
Some available developments on on-chip antennas in order to increase their gains have been made thanks to "the placement of dielectric lenses below or above the antenna". These lenses act like resonators and push the radiation

intensity away from the substrate so that the losses decrease.
Another viable way is utilize in-package antennas, that consist in placing in the package that surrounds the chip all the elements that form the antenna. In-package antennas offer higher efficiency and higher gains than on-chip antennas but they show some important issues like their difficult reliability and high packaging costs that will have to be solved.

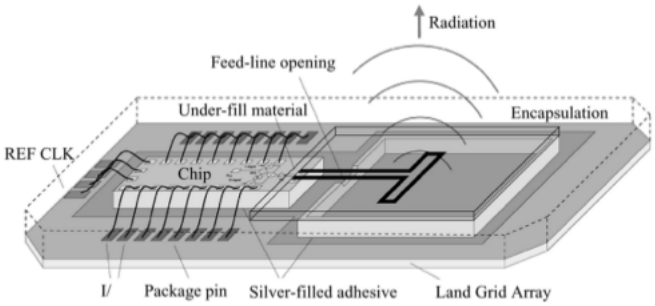

Figure 5.1: IBM conceptional drawing of in-package antenna

Apart from these types of antennas that have to be improved at 60 GHz, many examples that are described in [8] show that there is a large usage of antenna arrays, that is simply an antenna made by a bank of smaller antennas. In fact these antennas have the advantages of being directional, flexible for beam steering and have high gain and efficiency. The multiantenna techniques such as beam steering are very utilized and useful for the increase of the antenna radiation efficiency, of the transmission rate and furthermore for the increase of the reliability of wireless communication systems. This technique is also becoming a key technology for 60 GHz communication since it has many other advantages like increasing the gain of the whole antenna and "reduce the interference by steering the beam to the desired direction". Unfortunately antenna arrays occupy a bigger area and require more power since the antennas to be fed up are more.
Despite all the difficulties that the designers find implementing a key and difficult device like the antenna at 60 GHz, many are the solutions that have been proposed and that will result in continously integrated and more efficient antennas.

Chapter 6

Transmission lines

Transmission lines play an important role in wireless communication since they have to carry the RF signl power from one device to another in the transceiver and they have to do that in the most efficiency way, possibly without significant losses or distortion. Moreover they are employed as inductors or capacitors and utilized for performing very important impedance matching.
As the frequency of operation increases, long transmission lines like quarter wave become short enough to be directly integrated on chip since the wavelength decreases. There are many types of transmission lines but at 60 GHz the more appropiate for amplifier design and silicon integration are two: microstrip transmission lines and coplanar waveguide transmission lines.

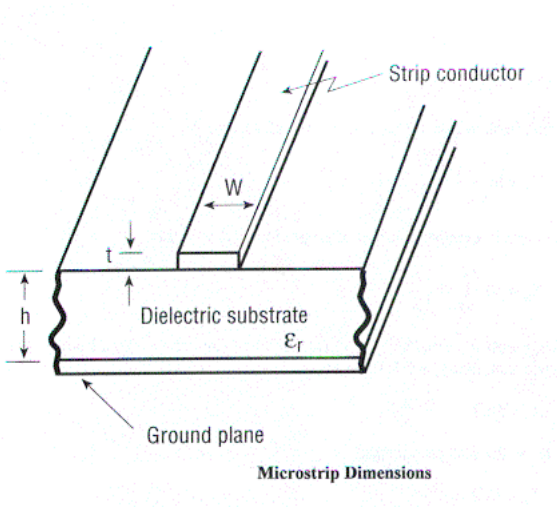

Figure 6.1: The section of a microstrip transmission line

The former, as we can see from figure 6.1, are transmission lines where there is a single conductor trace on one side of a dielectric substrate and a single ground plane on the other side. As is possible to see microstrip structure, a dielectric substrate between two traces, remind us in some way a capacitor and in fact microstrip transmission lines have higher capacitive

quality factors(that is the ratio between the electric enercy stored and the energy lost per cycle) than coplanar waveguide.

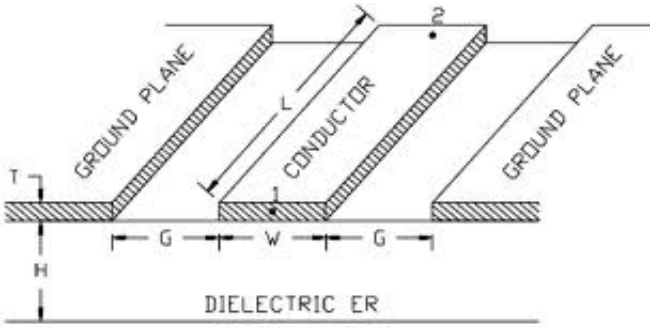

Figure 6.2: The section of a CPW(coplanar waveguide) transmission lines

On the other hand coplanar waveguide, as we can see from figure 6.2, are made of a single conductor strip deposited on a dielectric substrate placed in the middle of two ground electrodes that run adjacent and parallel to the conductor strip. Differently from the microstrip transmission lines, CPW have higher inductive quality factors(that is the ratio between the magnetic energy stored and the energy lost per cycle) than microstrip transmission lines. As said in [8] "the importance of inductive components(like in the design of LNAs for example) often make coplanar transmission lines preferable to microstrip transmission lines".
In the design of 60 GHz transceivers, however, transmission lines are increasingly important since they are utilized also for the development of capacitors and inductors but also because they have to be carefully realized. In fact designers have to take into account various phaenomena that transmission lines could produce at mm-wave frequencies like resonances but also impedances and so losses that could damage the operation of the other building devices.

Chapter 7

Low-Noise-Amplifier

The low-noise amplifier is the first device in any receiver chain. It has the important role of giving the first amplification to the low level signal that the antenna captures, but most important it has to make negligible the effect of noise from the subsequent blocks. Moreover it has to introduce the less possible of its own noise while performing input matching with the antenna at 50Ω.
All signals are affected by noise. When dealing with dc voltages or currents measured by a voltmeter for example, we always think of constant values. Indeed they are only the mean of noisy signals. In fact a current, for example, is continously constituted by electrons that are moving in a conductor. Their movement is not the same at every istant, but it varies resulting in small fluctuations around the dc value. The noise figure of a two-port network is a paramenter that measures how noisy is the device and it is defined as the input SNR divided by the output SNR. As said before the LNA is the first device in a receiver and so its noise figure is very important as it represents the most decisive factor in the total noise figure of the receiver, as we can see from the Friis equation

$$F(f) = F_1(f) + \frac{F_2(f) - 1}{g_1(f)} + ... + \frac{F_N(f) - 1}{g_1(f)...g_{N-1}(f)} \tag{7.1}$$

where $F_i(f)$ are the noise figure of the receiver devices(with $F_1(f)$ the one of the LNA) and $g_i(f)$ the gains of the various devices.
The other important characteristic of a LNA is its gain. The signal power that this device receives from the antenna is extremely low(even -110 dbm) and it has to give a power gain aroud 20 dB without increasing the noise of the signal. The other important characteristics that a LNA has to ensure are linearity and stability. Because of that the LNA has to be a linear device. For that reason usually a LNA is an amplifier that works in class A as biasing the circuit in this class of amplification ensures linearity, stability and high gain.

7.1 LNA design

As stated before a LNA needs a low noise figure, but also a high gain and obviously it has to be a linear device. The LNA design has to ensure also great stability and does not have to vary its linearity and overall performances even despite "semiconductor process, voltage and temperature variations"[8]. For these reasons a low noise amplifier is usually biased in class A. As we explained in chapter 4 analysing power amplifiers, class A amplifier is implemented with a single transistor that always conduct.
As we know, the signal that enters in a low noise amplifier comes directly from the antenna that has an output impedance value of 50Ω. Therefore, designing a LNA, it is important to perform an input matching through a input impedance of 50Ω. This input match is even more important when a pre-select filter is set before the LNA as these filters are sensitive to the quality of their terminating impedances.
Analysing the various stages of a LNA design the first important stage(of course after a careful biasing for low noise) is undoubtedly to perform an input impedance of 50Ω. There are various techniques to achieve this result. The first one is that of using a resistor at the input port of the transistor that provides the desired impedance value. The simplicity of this solution, however, has on the counterpart an important drawback as the resistor highly affects the noise figure of the entire device.
The second possible technique is that of using the source or emitter of a common-gate(or common-base) stage as the input termination of the transistor. However the main drawback of this architecture is its high noise figure.
The third technique is achieved through resistor and feedback. In fact it consists on using a shunt resistance and a feedback series capable of setting input and output matching. This solution provides higher power dissipation thanks to the resistors but unfortunately it requires on-chip resistors with high quality factors that usually are not available in CMOS technologies.
The fourth topology, also pursued in [21], employs inductive source or emitter degeneration in order to generate a real term in the input impedance. In fact considering a transistor with the two inductors placed as in figure 7.1(d) the input impedance can be simply derived as in the following equations.

We also have to develop a model of the MOS counting all the paramenters that give a contribute to the input impedance. Therefore, as in figure 7.2 the gate-source and gate-drain capacitances have to be considered for example. At the end we obtain

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right) L_s \tag{7.2}$$

and this impedance at resonance is $Z_{in} = \omega L_s$. We can see that this solution provides, at the resonance frequency of the input circuit, a real impedance

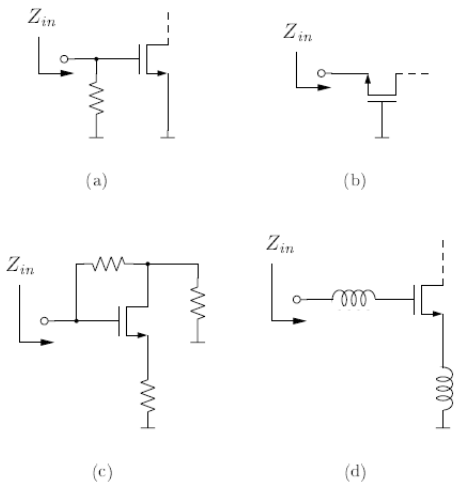

Figure 7.1: LNA architectures (a)Resistive termination, (b)$\frac{1}{g_m}$ termination, (c)Shunt-series feedback, (d)Inductive degeneration

proportional to the value of the source inductance. Moreover the use of inductances is preferable also for the noise figure, since there is a slight modification of the minimum noise figure differently from what happens using resistor termination architectures for example. At mm-wave frequencies these inductors could be implemented by the transmission lines, with an important space saving and more integration instead of using spiral inductors.
Another architecture that is used with success in the development of low-noise amplifiers is, as for PA, the cascode topology. In fact it provides high linearity and high gain, while at the same time it ensures a low noise figure. Looking at 60 GHz realizations it is possible to find some examples of cascode topology used for the implementation of mm-wave low noise amplifiers. In [23], for example, a first common base stage is chosen for the simple input matching, its higher gain compared to a common emitter and the higher reverse isolation. The second stage instead is a cascode common emitter amplifier in which great care is taken for the input and output matching in order to avoid the degeneration of the important properties of the LNA.
Looking at these realizations and also to the factors that the LNA has to assure(good gain, linearity and low noise figure) it is clear which are the main important values that the designer has to take care of realizing a LNA. Thus great efforts have to be made in order to have the best reverse isolation(this fact is made difficult from the low impedance exhibited by the silicon substrate), but also to achieve the most linear and stable amplification. Moreover the designer have to obtain these results combined with a good gain because as from the name, low noise amplifier, this device has to achieve the lowest possible noise figure together with a good amplification of the low signal that comes directly from the receiving antenna.
As we can see from figure 7.3 the last two architectures, cascode and inductive degeneration, can be used together combining the qualities of both

topologies.

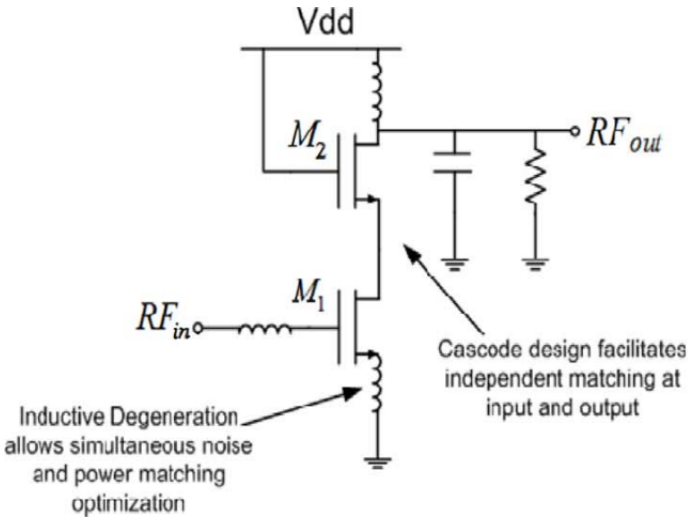

Figure 7.2: A typical LNA design with cascode architecture

Chapter 8

Oscillator

The local oscillator is a very important device in a wireless transceiver since it provides a stable frequency that multiplied with the radio frequency signal through the mixer, gives the important intermediate frequency signal that characterizes the superheterodyne architecture.
Anyway, as system operation frequency is continously increasing, so it has to do the frequency of the LO, without losing its important properties, that are the delivering of pure and sinusoidal waveforms at a stable frequency. This need results in a more difficult realization as at high frequency like 60 GHz, stability and not distorced signal are harder to obtain. This is a very difficult task for designers also because the oscillator has a nonlinear circuit that is incompletely described by linear system tools.
Moreover, especially at high frequencies, this difficulty is enhanced as the influence of parasitic elements is very pronunciated. This influence, combined with the resonance effects of passive elements, can lead to a wrong frequency of oscillation or even to the cease of oscillation.
For these reasons the oscillator have to be carefully designed.

8.1 Basic oscillator model

In every oscillator there is a particular thing that enables the oscillation:the positive feedback. In fact we can simplify the oscillator function by a block scheme as in figure 8.1 where it is shown the loop with the positive feedback.

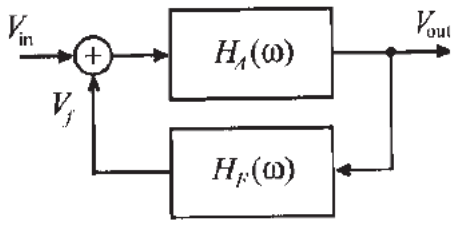

Figure 8.1: Circuit feedback model

Thus we can derive the transfer function of the whole block as in the equation:

$$\frac{V_{out}}{V_{in}} = \frac{H_A(\omega)}{1 - H_F(\omega)H_A(\omega)}$$

In an oscillator $V_{in} = 0$ because there is no input signal. Obviously we want a nonzero output signal and this can be achieved only if the denominator of the equation is equal to zero. This condition is also denominated Barkhausen criterion;

$$1 - H_F(\omega)H_A(\omega) = 0 \Rightarrow H_F(\omega)H_A(\omega) = 1$$

In order to increase the output voltage the loop gain $H_F(\omega)H_A(\omega)$ has to be greater than unity. Anyway after a while the voltage has to reach a steady state unless it will ideally increase to infinite. The solution used to stop this voltage increasing is the negative resistance that with its curve, a negative slope as we see from figure 8.2, ensures a decrease of the voltage gain.

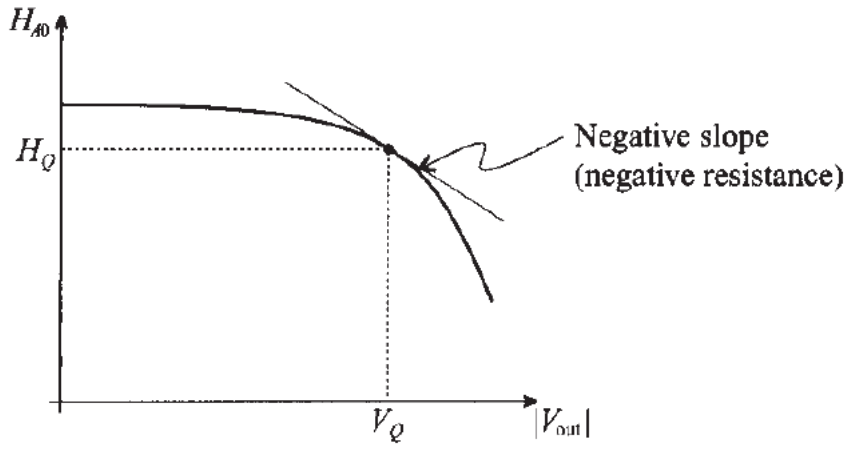

Figure 8.2: V_{out} versus gain characteristic with the negative slope shown

A simple oscillating circuit is the series of a resistor, a capacitor and an inductor, as in figure 8.3.

The equation that governs this circuit is a well-known differential equation

$$L\frac{d^2i(t)}{dt} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = -\frac{dv(t)}{dt} \tag{8.1}$$

that with the right side equal to zero has the solution $i(t) = e^{\alpha t}(I_1 e^{j\omega_Q t} + I_2 e^{-j\omega_Q t})$ where $\alpha = -\frac{R}{2L}$ and $\omega_Q = \sqrt{\frac{1}{LC} - (\frac{R}{2L})^2}$. In general, because of the negative value of α, the resonance circuit has a responce that tends to decrease and becomes zero as time passes. If ideally the resistance would become zero then a stable sinusoidal response would be obtained.
Thus adding a negative resistance to the circuit in order to obtain a total

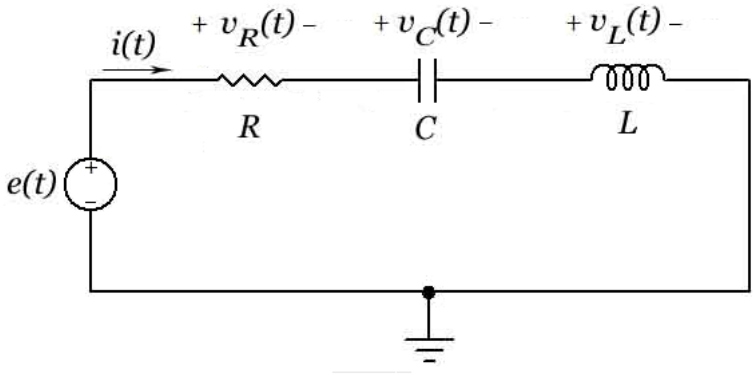

Figure 8.3: A simple RLC series circuit

resistance equal to zero is a solution that allows the achievement of the oscillation. A negative resistance is a nonlinear device with a voltage-current response that is in some way $v(i) = v_0 + R_1 i + R_2 i^2 ...$ and so the RLC differential equation becomes

$$L\frac{d^2i(t)}{dt} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = -R_1\frac{di(t)}{dt} \tag{8.2}$$

with $R + R_1 = 0 \rightarrow R_1 = -R$. A way of implementing a negative resistance is using a tunnel diode, a diode that is highly drogated at the point that the two junctions become two conductors. Thanks to that in its characteristic the tunnel diode shows a negative slope.

8.2 VCO

In the previous section we saw the main operating principles and characteristics of an oscillator. Anyway the local oscillator of a transceiver is usually implemented using a voltage-controlled oscillator(VCO).
The VCOs are feedback circuits with positive feedback such that they are designed to have an output signal even without an input one. Of course there are many different types of VCOs used at different frequencies, but the most suitable and used at 60 GHz are LC VCOs, subharmonic and distributed VCOs.
LC VCOs use an LC circuit, that is a resonance circuit, and a cross-couple transistors to generate the negative resistance that we have seen it is necessary for the oscillation. Varying the values of the capacitance and/or the inductuctance, it is possible to vary the oscillation frequency. One main advantage of LC VCO is the differential output as it ensures rejection from common-mode noise and less susceptibility to cross talk and noise.
Colpitts VCO instead, is similar to LC VCO since it employs an LC circuit too, but it does not have a differential output, so it employs only one transistor instead of the two of LC VCO. Moreover it offers low phase noise but it is "more susceptible to low-quality factor inductors and capacitors than

LC VCOs"[8].
Also VCO architectures based on push push and frequency doubling are interesting and efficient at 60 GHz even though they require additional circuits like filters and multipliers that occupy more space.
The thing that represents an important issue at 60 GHz, is that the high oscillation frequency required by the mm-wave transceiver is extremely sensitive to the layout parasitics and the design paramenters. Furthermore at mm-wave frequencies the LO leakage becomes a greater issue because of coupling through the silicon substrate.
Analysing some VCO prototypes used for mm-wave trasceivers it is possible to see that Colpitts VCOs are the ones mostly employed. Anyway, as it is possible to see from[25], in todays WLAN transceivers(and so at frequencies of 2.4-5 GHz) the most utilized VCO architecture in modern CMOS, is the complementary cross coupled structure. Generally this architecture gives better symmetry of the oscillation voltage, higher stability and lower hot carrier effects. For these reasons cross coupled VCOs are receiving some attenctions even for mm-wave realizations.
Despite these advantages at mm-wave frequencies the oscillator architecture mostly utilized is the colpitts VCO. In fact at high frequency this type of oscillator is able to provide better phase noise performances than cross coupled since it has a "higher power transferred efficiency and low impulse sensitivity". As an example Colpitts architecture is employed also in [23] in the transceiver LO, with two implementation, one oscillating at 20 GHz with a frequency tripler, and another at 60 GHz.
Anyway Colpitts oscillator presents also some disadvantages, as its high start-up conditions, that require a lot of power for the start of the oscillation. For this reason efforts are made in order to develop alternative solutions and find architectures that can offer at the same time good oscillation properties and low start-up conditions.
Obviously there are also many other types of oscillators that could be used at 60 GHz but what is essential to be taken into account in their development is that the oscillator at mm-wave frequencies requires large current for phase noise performances and it is really sensitive to parasitic elements. Therefore when a designer has to decide which VCO is best to use for his transceiver, it is really important to pay attention to all these particulars.

Chapter 9

Mixer

In chapter 3 we have described the superheterodyne transceiver, emphasizing on its peculiarity, that is the frequency shifting that takes place from an RF signal to an IF one. The mixer is the device that allows this up and down conversion since it is capable of taking two frequencies at its input and giving multiple frequencies components at his output, that is the multiplication of the two input signals.
We suppose of having two sinusoidal signals x_1 and x_2 at two different frequencies f_1 and f_2, for example

$$x_1 = A\cos(2\pi f_1 t)$$

$$x_2 = B\cos(2\pi f_2 t)$$

We apply these two signal at the input of a mixer that we know that multiplies its input signals so we obtain $y = AB\cos(2\pi f_1 t)\cos(2\pi f_2 t)$. Using the prosthaphaeresis identity $\cos(a)\cos(b) = \frac{1}{2}[\cos(a-b)+\cos(a+b)]$ finally we obtain

$$y = \frac{A+B}{2}[cos(2\pi(f_1+f_2)) + cos(2\pi(f_1-f_2))] \tag{9.1}$$

that is a sinusoidal signal with a component that depends on the difference of the two frequencies and one on the sum.
Thus using the mixer in a RF transceiver is possible to downconvert the RF input signal to an IF one employing a passband filter that selects the appropiate component.

9.1 Basic theory

It is clear that a linear system is unable to act like a mixer and multiply two inputs. Therefore it is necessery to use a nonlinear device, like a diode or a transistor, since it can generate multiple harmonics. In figure 9.1 there is a simple scheme of a mixer.

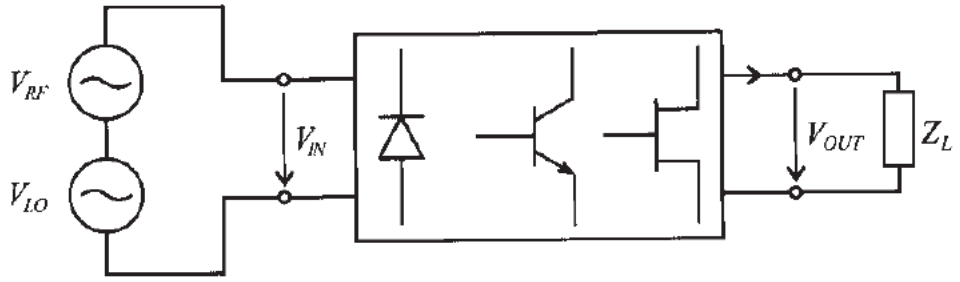

Figure 9.1: A scheme that simplify s mixer. We can see the two voltage inputs, the nonlinear device at the base of the mixer and the voltage output

Analysing the characteristics of diodes and transistors we can see that both diode and BJT have an exponential characteristic as $I = I_0(e^{\frac{V}{V_T}} - 1)$ where V_T is the thermal voltage. Differently a MOSFET has approximately a square behaviour as $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_{Th}})^2$.
From the figure we see two voltages $v_{RF} = V_{RF}\cos(\omega_{RF}t)$, that represents the RF signal, and $v_{LO} = V_{LO}\cos(\omega_{LO}t)$, that represents the local oscillator signal. The total input, that the nonlinear device(diode or transistor) has to operate, is the sum of the two signals hence

$$V = V_Q + V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t)$$

where V_Q is the bias voltage.
Applying the input voltage V to the diode or the transistor(that are nonlinear devices) we can obtain the linearized characteristic through a Taylor expansion that is

$$I = I_Q + V\left(\frac{dI}{dV}\right)|_{V_Q} + \frac{1}{2}V^2\left(\frac{d^2I}{dV^2}\right)|_{V_Q} + ... \tag{9.2}$$

Avoiding bias V_Q, I_Q, as they are constant, naming $A = (\frac{dI}{dV})\ |_{V_Q}$ and $B = (\frac{d^2I}{dV^2})\ |_{V_Q}$ and substituting the input voltage in equation (9.2) we obtain

$$\begin{aligned} I &= A[V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t)] \\ &+B[V_{RF}^2\cos^2(\omega_{RF}t) + V_{LO}^2\cos^2(\omega_{LO}t)] \\ &+2BV_{RF}V_{LO}\cos(\omega_{RF}t)\cos(\omega_{LO}t) + ... \end{aligned} \tag{9.3}$$

The terms containing $\cos^2(\omega t)$ depend only on the same frequency since $\cos^2(\omega t) = \frac{1}{2}[1 - \cos(2\omega t)]$. Instead the important term in (9.3) is the final one because it is the multiplication of two cosine functions and so(as from (9.1)) it results

$$I = ... + BV_{RF}V_{LO}[\cos((\omega_{RF} + \omega_{LO})t) + \cos((\omega_{RF} - \omega_{LO})t) \tag{9.4}$$

From (9.4) it is possible to see how a diode or a transistor gives new frequency terms of $\omega_{RF} \pm \omega_{LO}$ acting like a mixer. Anyway using the Taylor series we stopped it up to the third term $\frac{1}{2}V^2(\frac{d^2I}{dV^2}) \mid_{V_Q}$ neglecting the higher-order terms. However these higher-oder harmonic terms, employing diodes and BJTs are very important as they can compromise the performances of the mixer because they affect the signal interfering with it. Using a MOSFET with quadratic behaviour characteristic, instead, the harmonics higher than the second-order can survive with difficulty and so the performances of the mixer are less affected.
Another problem that afflicts the mixer is the one of the image frequency. In fact when for example a transceiver is receiving, it receives the frequency at the intermediate frequency that is obtained downconverting the RF signal through the mixer so it is $\omega_{IF} = \omega_{RF} - \omega_{LO}$. However if there is a signal at a frequency ω_{IM} such that $\omega_{LO} - \omega_{IM} = \omega_{IF}$, even this signal is received and can interfere with the other "right" signal. Thus it is necessary, when designing a transceiver, to place an image filter before the mixer circuit in order to avoid this issue.

9.2 Mixer types

There are two main types of mixers: active mixers and passive mixers. The former are characterized by the fact that some of the mixer transistors provide a small gain; instead in the latter all transistors act like switches. The decision of which mixer architecture it is best to use is very important since this choice influences the entire downconversion chain of the receiver circuitry.
In the realization of a mixer there are some fundamental parameters that have to be taken into account and have to be satisfied: conversion loss, linearity and power consumption. Thus researchers have to achieve the minimum conversion loss, together with a good linearity and the minimum power consumption.
For what concerns the devices utilized for the mixer implementation, SiGe and GaAs technologies are widely employed but their high costs and high power supply make these technologies not the optimal ones for actual max production. For these reasons CMOS is the best solution also for this device since it has lower power requirements, it offers better integration and it is cheaper.
Therefore once we have chosen CMOS technology for the realization, the other important decision is that of choosing between the use of active or passive mixer architecture.
Active mixers have the great advantage of achieving a low conversion loss since the active components used for the implementation provide a small gain and they are appreciated since they have a more compact layout and so they are more suitable for RF integrated circuits. Moreover they provide better isolation properties and moderately high performances. Unfortunately

active mixers show some important issues that are stressed at mm-wave frequencies. The most important issues are the linearity, that is accentuated by the low voltage supply, and the flicker noise.
On the other hand at 60 GHz passive mixers are easier to implement than active mixers and they have "a very good linearity, suitable for high dynamic range receiver design, and a very limited flicker noise effect, due to the absence of channel DC bias current"[26]. Therefore passive mixers have a zero power dissipation.
Anyway they suffer from a great disadvantage that is their conversion loss. In fact since there are not active devices capable of amplify a bit the signal, they result in a conversion loss in which some of the input power is lost.
A problem that affects both mixer architecture types, but more strongly passive ones, is the difficult achievement of a large LO power at 60 GHz. In fact in a passive mixer transistors operate like switches and a higher LO power is required in order to switch firmly. This fact results in a more pronunciated conversion loss.
Another important factor that have to be taken into account is the achievement of a good isolation of the mixer since a "low isolation results in increased distortion, self-jamming and dc offset errors"[8]. In conclusion we have seen all the problems that affect both active and passive mixer architectures at 60 GHz and the realizations that have been made since now do not show a marked preference between these two topologies. What is always really important in the realization of a mixer for a 60 GHz transceiver is that "researchers must balance gain, linearity and power consumption"[8] finding the best tradeoff between linearity, space occupation, isolation, conversion loss and power consumption.

Chapter 10

Conclusion

Recalling what we said in the introduction, 60 GHz wireless communication will lead to amazing data rates that will revolutionate the communication technology. Industry interest in this revolution is very high and so industries will support this new possibility.
Moreover the revolution will be a necessity for the developers too, where the state of the art of 60 GHz technology briefly described in this paper is only the base for future developments. "The availability of such massive bandwidths and subterahertz carrier frequencies will require communication engineers to rethink wireless approaches while learning how to fabricate devices in silicon, and circuit and antenna designers will need to become more aware of communication requirements"[8].
The developments on CMOS technology and the possibility to apply it to the mm-wave frequency devices will lead to low cost and small demensions devices. CMOS technology is going to be the future of devices development like RF PAs too. Therefore the research on design architecture based on CMOS and the optimization of the devices' efficiency maintaining low power consumption and low costs, will represent difficult challenges that researchers will always have to satisfy and to solve.
Concluding, 60 GHz wireless communication and high data rates are the future and a future quite near. Undoubtely mm-wave frequencies will change completely the way people will deal with information devices but also how wireless devices will be designed and developed.

Bibliography

[1] A. Valdes-Garcia, S. Reynolds and U. R. Pfeiffer *"A 60GHz Class-E Power Amplifier in SiGe"*, Solid-State Circuits Conference, 2006 IEEE Asian Page(s): 199 - 202

[2] T. Quémerais, L. Moquillon, S. Pruvost, J.M. Fournier, P. Benech, N. Corrao *"A CMOS Class-A 65nm Power Amplifier for 60 GHz Applications"*, Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2010 Topical Meeting on, Page(s): 120 - 123

[3] B. Wicks, C. M. Ta, E. Skafidas, R. J. Evans, and I. Mareels *"A 60-GHz power amplifier and transmit/receive switch for integrated CMOS wireless transceivers"*, Microwave and Millimeter Wave Technology, 2008. ICMMT 2008. International Conference on, Page(s): 155 - 158

[4] M. Khanpour, S. P. Voinigescu, M. T. Yang *"A High-Gain, Low-Noise, +6dBm PA in 90nm CMOS for 60-GHz Radio"*, Compound Semiconductor Integrated Circuit Symposium, 2007 IEEE, Page(s): 1-4

[5] D. Dawn, S. Sarkar, P. Sen, B. Perumana, M. Leung, N. Mallavarpu, S. Pinel, and J. Laskar *"60GHz CMOS Power Amplifier with 20-dB-Gain and 12dBm Psat"*, Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International, Page(s): 537 - 540

[6] A. Siligaris, Y. Hamada, C. Mounet, C. Raynaud, B. Martineau, N. Deparis, N. Rolland, M. Fukaishi, P. Vincent *"A 60 GHz Power Amplifier With 14.5 dBm Saturation Power and 25% Peak PAE in CMOS 65 nm SOI"*, Solid-State Circuits, IEEE Journal of Volume: 45 , Issue: 7, Page(s): 1286 - 1294

[7] D. Dawn, S. Sarkar, P. Sen, B. Perumana, D. Yeh, S. Pinel, and J. Laskar *"17-dB-Gain CMOS Power Amplifier at 60GHz"*, Microwave Symposium Digest, 2008 IEEE MTT-S International, Page(s): 859 - 862

[8] T. S. Rappaport, J. N. Murdock and F. Gutierrez *"State of the Art in 60-GHz Integrated Circuits and Systems for Wireless Communications"*, Proceedings of the IEEE | Vol. 99, No. 8, August 2011, Page(s): 1390-1436

[9] Jae-Sung Rieh and Dong-Hyun Kim *"An Overview of Semiconductor Technologies and Circuits for Terahertz Communication Applications"*,

GLOBECOM Workshops, 2009 IEEE Nov. 30 2009-Dec. 4 2009, Page(s): 1 - 6

[10] A. Deshmukh, S.K. Bodhe *"Characterization of radio propagation at 60 GHz channel"*, Internet, 2009. AH-ICI 2009. First Asian Himalayas International Conference on 3-5 Nov. 2009, Page(s): 1 - 8

[11] S. Aloui, E. Kerherve, D. Belot, R. Plana *"Design Techniques and Modeling for 60GHz Applications With a 65nm-CMOS-RF Technology"*, Millimeter Waves, 2008. GSMM 2008. Global Symposium on 21-24 April 2008, Page(s): 241 - 244

[12] C.H. Doan, S. Emami, A.M. Niknejad, R.W. Brodersen *"Design of CMOS for 60GHz applications"*, Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International 15-19 Feb. 2004, Page(s): 440 - 538 Vol.1

[13] Van-Hoang Do, V. Subramanian, W. Keusgen, G. Boeck *"A 60 GHz SiGe-HBT Power Amplifier With 20% PAE at 15 dBm Output Power"*, Microwave and Wireless Components Letters, IEEE March 2008 Vol. 18 , Issue 3, Page(s): 209 - 211

[14] M. Abbasi, T. Kjellberg, A. de Graauw, E. van der Heijden, R. Roovers, H. Zirath *"A Broadband Differential Cascode Power Amplifier in 45 nm CMOS for High-Speed 60 GHz System-on-Chip"*, Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE 23-25 May 2010, Page(s): 533 - 536

[15] B. Heydari, P. Reynaert, E. Adabi, M. Bohsali, B. Afshar, M.A. Arbabian, A.M. Niknejad *"A 60-GHz 90-nm CMOS Cascode Amplifier with Interstage Matching"*, Microwave Integrated Circuit Conference, 2007. EuMIC 2007. European 8-10 Oct. 2007, Page(s): 88 - 91

[16] W.J. Chang, J.W. Lim, H.K. Ahn, H. Kim, H.K. Yu "60 GHz Amplifier MMICs and Module for 60 GHz WPAN System" *Radio and Wireless Symposium, 2007 IEEE 9-11 Jan. 2007* Page(s): 377 - 380

[17] R. C. Daniels and R. W. Heath, Jr. *"60 GHz Wireless Communications: Emerging Requirements and Design Recommendations"*, Vehicular Technology Magazine, IEEE Vol. 2 , Issue 3 Sept. 2007, Page(s): 41 - 50

[18] Qizheng Gu *"RF System Design of Transceiver for Wireless Communications"* Springer, 1st edition (2005), USA Page(s): 113 - 171

[19] Steve C. Cripps *"RF Power Amplifiers for Wireless Communications"* Artech House, 2nd edition (2006), Norwood Page(s): 39 - 68 and 143 - 148

[20] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic and N.O. Sokal *"RF and Microwave Power Amplifier and Transmitter Technologies Part 1 to Part 4"*, from November 2003 High Frequency Electronics 2003 Summit Technical Media, LLC, Page(s): 22 - 49

[21] D.K. Shaeffer and T.H. Lee *"A 1.5 V, 1.5 GHz CMOS Low noise amplifier"*, VLSI Circuits, 1996. Digest of Technical Papers, 1996 Symposium on 13-15 Jun 1996, Page(s): 32 - 33

[22] P. Reynaert *"Design consideration for CMOS RF and mm-wave power amplifiers"*, Microwaves, Radar and Remote Sensing Symposium (MRRS), 25-27 Aug. 2011, Page(s): 47 - 50

[23] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T Zwick, T. Beukema, and B. Gaucher *"SiGe Bipolar Transceiver Circuits Operating at 60 GHz"*, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1, JANUARY 2005, Page(s): 156 - 167

[24] Ki-Jin Kim, Tae-Ho Lim, Hyun-Chul Park, Ahn K.H. *"mm-Wave CMOS Colpitts VCO & Frequency divider for the 60GHz WPAN"*, Communications (MICC), 2009 IEEE 9th Malaysia International Conference on 15-17 Dec. 2009, Page(s): 358 - 361

[25] M. Ercoli, M. Kraemer, D. Dragomirescu, R. Plana *"A Passive Mixer for 60 GHz Applications in CMOS 65nm Technology"*, German Microwave Conference 15-17 March 2010, Page(s): 20 - 23

[26] Y. P. Zhang, M. Sun, K. M. Chua, L. L. Wai, and Duixian Liu *"Antenna-in-Package Design for Wirebond Interconnection to Highly Integrated 60-GHz Radios"*, IEEE Transactions on antennas and propagation, vol. 57, no. 10, october 2009, Page(s): 2842 - 2852