Università degli Studi di Padova

Dipartimento di Ingegneria dell'Informazione

Università degli studi di Padova

Dipartimento di Ingegneria dell'Informazione DEI

Corso di Laurea Magistrale in Ingegneria Elettronica

Analysis and Design of a Low Noise Transconductance Amplifier for a Bluetooth Radio

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Anno Accademico 2021/2022

5 dicembre 2022

"Reste neutre. Observe sans juger. Obéis sans discuter. Apprends sans prendre position. Intéresse-toi sans t'attacher. Remplis ton devoir sans rien attendre en retour. C'est la seule façon de ne pas souffrir. Moins on souffre, plus on est efficace. Plus on est efficace, mieux on sert la cité."

[*from "Les Passe Miroir" by Christelle Dabos*]

"Se ho visto più lontano è perché stavo sulle spalle di giganti."

[*Isaac Newton*]

Alla mia Famiglia

SOMMARIO

Questa tesi raccoglie il lavoro svolto durante un periodo di tirocinio presso l'azienda Infineon Technologies AG a Villach, in Austria, tra marzo e ottobre 2022.

Gli argomenti esposti sono l'analisi di un amplificatore a basso rumore impiegato in una radio Bluetooth e il progetto di una versione dell'amplificatore stesso volta ad un minor consumo di potenza.

Gli amplificatori a basso rumore rivestono un ruolo fondamentale nei circuiti di ricezione a radiofrequenza in quanto costituiscono uno dei primi stadi della catena di elaborazione del segnale; da essi dipendono numerose caratteristiche dell'intero ricevitore come cifra di rumore, linearità e sensibilità. Risulta quindi di fondamentale importanza saper valutare le prestazioni necessarie ed impiegare criteri di progetto idonei affinché non solo l'amplificatore ma il sistema complessivo operi correttamente e secondo le specifiche.

L'elaborato racchiude una visione di insieme preliminare sullo standard Bluetooth atta a identificare il contesto di appartenenza dell'amplificatore a basso rumore, inclusa una breve discussione dello stato dell'arte di ricevitori a bassa potenza per BLE; successivamente espone i principali concetti teorici che permettono di comprendere la parte di analisi, progetto e simulazione racchiusi nei capitoli a seguire.
Un intero capitolo è dedicato alla descrizione del layout dell'amplificatore; in lingua italiana esso può essere tradotto come *disposizione* con il significato di *rappresentazione attraverso strati di metallo, ossido e semiconduttore di un circuito integrato*. In altre parole, si tratta di una versione fisicamente realizzabile dello stesso amplificatore che traduce in materia quello che viene astrattamente descritto a livello schematico. L'ultimo capitolo, infine, espone le conclusioni basate sui principali risultati ottenuti nelle simulazioni e apre scenari per futuri lavori nel ricevitore.

L'autore augura una buona lettura.

ABSTRACT

This dissertation deals with the internship work at Infineon Technologies AG in Villach, Austria, from march to october 2022.

The main topics are the analysis of a low noise amplifier for a Bluetooth radio and the design of a new lower power oriented version of it.

Low noise amplifiers assume a very important role in radio-frequency receivers: they are one of the first signal process system stages. Noise figure, sensitivity and linearity of the overall receiver strongly depend on them. A wise choice of requirements and good design criteria are essential to make both the amplifier and the receiver to work properly and according to project specifications.

This thesis starts introducing the Bluetooth standard in order to understand where and why a low noise amplifier is required; some state of art BLE receivers are described as well. To easily follow the main chapters regarding the analysis and the design of the amplifier, some theoretical aspects are firstly covered.
A whole chapter is spent discussing the layout design process of the amplifier; this step is needed to translate the schematic into a physical working device. The last chapter includes the conclusions based on the simulation results and proposes future investigations for the receiver.

The author wishes you an enjoyable reading.

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RINGRAZIAMENTI

Ringrazio tutti coloro che mi hanno sostenuto in questo periodo di formazione all'estero; ringrazio in particolare il professor A. Neviani, il Dr. Ing. M. Bassi e il Dr. Ing. Davide Ponton per avermi permesso di conoscere e lavorare in una grande azienda di semiconduttori quale è l'Infineon Technologies. Ringrazio tutti i membri del gruppo Wireless del DES per essere sempre stati disponibili a dissolvere qualsiasi dubbio e fornire consigli e suggerimenti, oltre che per avermi accolto in questi otto mesi di tirocinio.

Ringrazio la mia Famiglia che mi ha sempre sostenuto e ha appoggiato ogni mia scelta; ringrazio gli amici che mi sono sempre stati accanto.

L.G.

1 INTRODUCTION

In this chapter a brief and essential description of the Bluetooth standard is presented. First of all, a panoramic of the most common wireless communication technology standards is described as well as the position of the Bluetooth among them. The working principle and the simple block diagrams of the receiver and the transmitter circuits immediately follow. After that, the Bluetooth Low Energy standard is described. Eventually the structure of this thesis work is shown.

1.1 WIRELESS COMMUNICATION OVERVIEW

Since the radio invention, communication without the use of cables (that is, wire-less) has been knowing a huge growth, particularly accentuated nowadays.

The huge area of possible applications has risen the necessity of dividing the development in sub-areas. Each of them is responsible to cover a specific customer demand and can be distinguished from the others accordingly, for example, to the *distance* covered and/or to the amount of exchange data *speed*. *Power consumption* is another important keyword when one's talking about wireless communication due to its strictly dependence on the capability to work without power cables (battery operating devices).

This last index, which one can easily promote to figure of merit, is quite relevant in the field of *Internet of Things* devices (IoT devices); in a world where everything is connected, a decrease of the power consumptions is a primary goal in order to guarantee a fruitful and efficient communication among the aforementioned battery operating devices such as notebooks, smartphones, smartwatch, sensors and so on; this is particularly true when one is talking about wearable devices able to monitor the physiologic signals of an human body.

Application examples can be found in many different articles and papers, some of which the reader is indexed [4], [5]and [30].

Figure (1) shows some of the most important communication technologies used in the immense IoT field.

1.2 BLUETOOTH STANDARD

Bluetooth is a communication standard developed to work in the *Personal Area Network* (PAN) and to make user devices capable of interacting each other independently on the customer location [6]. It is described, according to its official site, as a low power radio, streaming data over 79 channels in the 2.4GHz unlicensed *Industrial, Scientific and Medical* (ISM) frequency band.

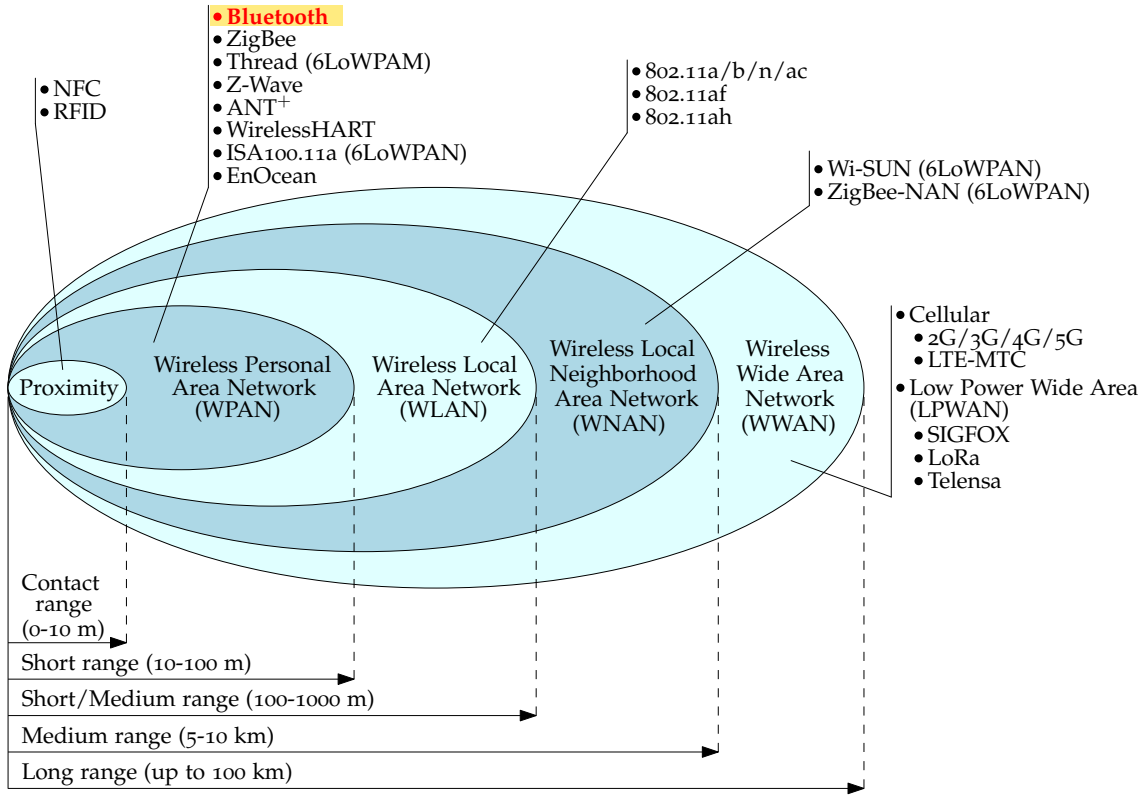


Figure 1: panoramic of the technologies used in IoT, source [19]

Bluetooth was first conceived with the purpose of reunifying short-range radio technologies and supporting different products and industries; since its birth, in 1996, more and more devices have adopted this communication standard. It has been estimated that a number of 7 billions Bluetooth enable devices will ship annually by 2026 [1].

Bluetooth is mainly used for point-to-point communications; an example of the latter concept is what happens between a smartphone and a car on board computer or between a headphones and a laptop. Unlike the WLAN standards, which purpose is to replace the older LAN cable maintaining and overtaking its speed, Bluetooth favours power saving and low costs. As a consequence, no more than 3Mb/s are achieved and shorter distances (<10m) are covered.

1.2.1 Working principle

A Bluetooth communication involves two entities, called master and slave: the former is the one that starts the data transfer. Every Bluetooth enable device comes with both the master and the slave hardware, hence every device is able to initiate the communication.

Data is transferred by means of sequence of *packets*: each packet occupies a *slot* and a *frame* consists of two slots: one transmit slot and one receive slot. In this way a *full-duplex* communication is provided between the master and the slave.

In order to guarantee a robust link against interference and noise, the data transfer hops to one of the 79 available channels of the Bluetooth standard (*Frequency Hopping*

Technique). The channel selection is algorithmically derived from the master ID and the previous channel number.

The main modulation format adopted by the standard is the *Gaussian Frequency Shift Keying* (GFSK) although other modulation scheme have been introduced along the years.

The data stream is firstly filtered by using a Gaussian filter; the resulting output is then used to modulate the carrier. The GFSK modulated signal can then be expressed as:

$$s(t) = \sin 2\pi \left[f_C + f_d \cdot g(t) \right] \tag{1}$$

where f_C is the carrier frequency, f_d the frequency deviation and $g(t)$ is given by:

$$g(t) = d(t) \cdot \exp \left[-\frac{1}{2} \left(\frac{\pi}{\sqrt{\ln 2}} \frac{t}{T_b} \right)^2 \right] \tag{2}$$

with $d(t)$ the data stream signal, T_b the bit period. The output $s(t)$ is the filtered by a band pass filter before being up-converted by the transmitter mixers: the power amplifier than send it to the antenna. From the receiver perspective, the signal is firstly

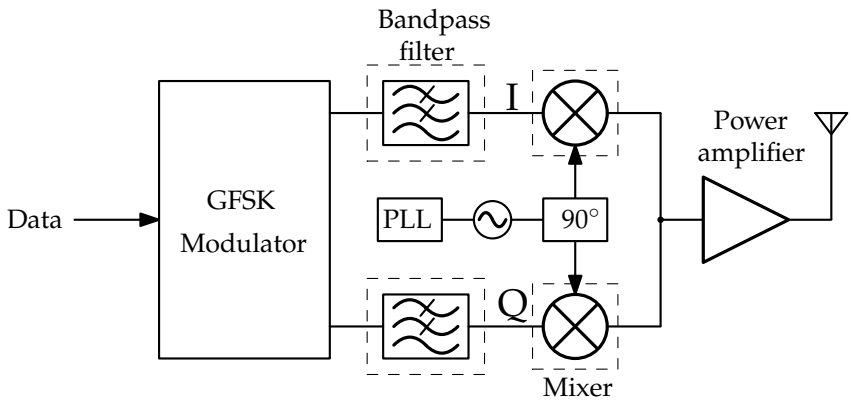


Figure 2: block diagram of a Bluetooth transmitter.

amplified by a low noise amplifier.

The reason behind the use of two quadrature signals, the *I* and the *Q signals*, is that the modulation scheme used is not symmetric around the carrier frequency; using a single mixer would cause corruption of the data due to the superimposition of the useful signal itself. Hence the use of two 90° phase shifted signals, being separated, allows to recover the original data signal.

The *I* and *Q* signals are then recovered by the use of I and Q mixers; a band pass filter is used to remove the DC and low pass noise components in addition to the higher frequency spectrum components. Bluetooth specifications have to be carefully followed in transceiver designs; these requirements are well defined in the correspondent sheet provided to the designer and deals with the sensitivity, the noise figure for a certain *Bit Error Rate* (BER) and so on.

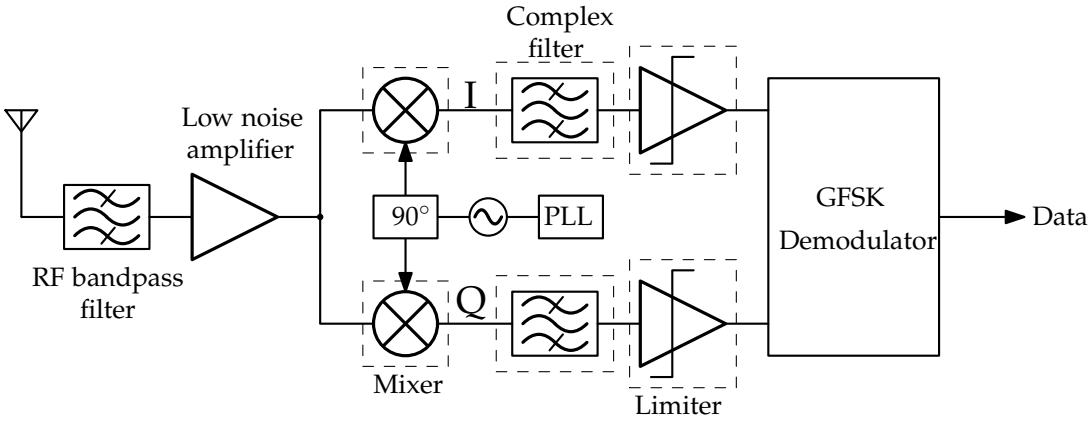


Figure 3: block diagram of a IF-based Bluetooth receiver.

1.2.2 Bluetooth Low Energy standard

Due to increasing demanding of ultra low power, ultra low cost IoT devices, an even more power performing standard has been required, given birth to the so called *Bluetooth Low Energy* (BLE) standard.

The main changes involve the quantity of data transfer, the number of available channels and the maximum output power while the radio structure remains mostly the same of the Bluetooth classic. Hence, previous considerations on the receiver/transmitter structures still hold true.

The two standards are intrinsically incompatible, which means a BLE vs BT classic communication is not possible due to the different ways of devices discovering and packets size [12]. To sustain compatibility both standards have to be adopted in the device.

Table (1) reassumes the main differences between the two. As can be seen, one the most important and crucial difference is about the channels arrangement along the operating bandwidth. In the BLE, 40 channels are used, 3 of which with the advertising scope, that is, dedicated channel used to show a BLE enable device presence. The reduced number of channels has enhanced the channel bandwidth, passing from 1 MHz of the Bluetooth classic to 2 MHz of the BLE.

The connection between BLE devices is established by using the advertising channels that allow them to find each other once a connection request is needed; each device periodically send non-connectable advertising packets which are received from anyone located nearby. In contrast a Bluetooth classic master device has to scan 32 different channels to discover the wanted slave and initiate the data swapping.

The amount of information exchanged in the two standards is different: the BLE is able to send essential data as position, date, environment measurements such temperature or humidity, while the Bluetooth standard is able to transfer even voice information. The reason relays on the different scenarios they are thought to work: the former is used essentially to make a constant interaction between very different devices possible while the latter is really indexed to realize an efficient interface with the user.

Many other differences do exist but, for the purpose of this work, are not considered.

Table 1: comparative table between the Bluetooth LE and the Bluetooth Classic.

	Bluetooth Low Energy (LE)	**Bluetooth Classic**
Frequency Band	2.4GHz ISM Band (2.402 – 2.480GHz Utilized)	2.4GHz ISM Band (2.402 – 2.480GHz Utilized)
Channels	40 channels with 2MHz spacing (3 advertising channels/37 data channels)	79 channels with 1MHz spacing
Channel Usage	Frequency-Hopping Spread Spectrum (FHSS)	Frequency-Hopping Spread Spectrum (FHSS)
Modulation	GFSK	GFSK, $\pi/4$ DQPSK, 8DPSK
Data Rate	LE 2M PHY: 2Mb/s LE 1M PHY: 2Mb/s LE Coded PHY (S=2): 500Kb/s LE Coded PHY (S=8): 125Kb/s	EDR PHY (8DPSK) 3Mb/s EDR PHY ($\pi/4$ DQPSK) 3Mb/s EDR PHY (GFSK) 1Mb/s
Tx Power [1]	$\leq$ 100mW (+20dBm)	$\leq$ 100mW (+20dBm)
Data Rate	LE 2M PHY: ≤ -70dBm LE 1M PHY: ≤ -70dBm LE Coded PHY (S=2): ≤ -75dBm LE Coded PHY (S=8): ≤ -82dBm	≤ -70dBm
Data Transports	Asynchronous Connection-oriented Isochronous Connection-oriented Asynchronous Connectionless Synchronous Connectionless Isochronous Connectionless	Asynchronous Connection-oriented Synchronous Connection-oriented
Communication Topologies	Point-to-Point (including piconet) Broadcast Mesh	Point-to-Point (including piconet)
Positioning Features	Presence: Advertising Direction: Direction Finding (AoA/AoD) Distance: RSSI, HADM (coming)	None

[1] Devices shall not exceed the maximum allowed transmit power levels set by the regulatory bodies that have jurisdiction over the locales in which the device is to be sold or intended to operate. Implementers should be aware that the maximum transmit power level permitted under a given set of regulations might not be the same for all modulation modes.

1.3 THESIS STRUCTURE

This thesis deals with the analysis and the design of an important block of the receiver structure used both by the Bluetooth Classic and the BLE (and not only): such block is called *Low Noise Amplifier* (LNA).

The main project where the work takes place is a *low power radio* currently (2022) under development at Infineon Technologies AG: a parallel study for the LNA has been made during the re-design and the porting (that is, the migration from one technology to another, mostly a more performing one) in order to investigate possible ways to lower the amount of power consumption.

The dissertation is structured as follows: after this brief introductory chapter, the second introduces some general concepts to help understanding each step and choice made in the work.

The third chapter reports a brief overview of the state of the art low power BLE receivers with a comparative table to show what is available in the recent literature; new targets can be set to make future works of the radio receiver part more competitive.

The fourth chapter is about the analysis of two different low noise amplifiers: the one used in a previous project and realized in an older technology and the one that is currently used in the radio receiver chain. Simulation results complete the chapter.

The fifth chapter deals with the design of a new version of the amplifier. Comparative results with the older designs are also presented to see advantages and disadvantages of the new architecture.

The sixth chapter contains some interesting insight about the layout realization, that is, the final step of the design where parasitic elements of the real circuit are taken into account and the amplifier assumes the shape of a real physical implementation.

A chapter of conclusion ends the work including space for future improvements and a summary of the results.

Because of Infineon Technologies copyrights, no technology parameters nor design dimension are shown, with few exceptions.

2 PRELIMINARY CONCEPTS

In this chapter, to make easier and more understandable the main contents of this thesis, some theoretical concepts are reviewed.

2.1 SCATTERING PARAMETERS (S-PARAMETERS)

Scatterings parameters are usually adopted to characterize high frequency circuits. Consider the generic n-port network depicted in figure (4). It is possible to define the normal-

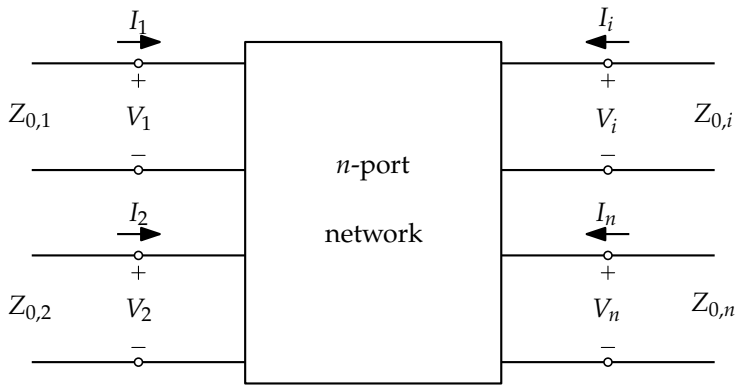


Figure 4: generic n-port network.

ized voltages and currents with respect to the correspondent characteristic impedance. The *forward waves* are expressed in the form:

$$a_i = \frac{V_i^+}{\sqrt{Z_{0,i}}} = I_i^+ \sqrt{Z_{0,i}} \tag{3}$$

while for the *backward waves* one has:

$$b_i = \frac{V_i^-}{\sqrt{Z_{0,i}}} = I_i^- \sqrt{Z_{0,i}} \tag{4}$$

The total voltage and the total current at one port can be written as:

$$V_i = V_i^+ + V_i^- \tag{5}$$

$$I_i = I_i^+ + I_i^- \tag{6}$$

The ratio between the forward and backward waves gives the definition of *reflective coefficient* associated to the port i:

$$\Gamma_i \triangleq \frac{V_i^-}{V_i^+} = \frac{b_i}{a_i} \tag{7}$$

The link between the normalized waves and the apparent power is expressed in the following way: for the forward wave it results:

$$P_i^+ = \frac{1}{2} V_i^+ \left(I_i^+\right)^* = \frac{1}{2} V_i^+ \left(\frac{V_i^+}{Z_{0,i}}\right)^* = \frac{1}{2} \frac{\left|V_i^+\right|^2}{Z_{0,i}} = \frac{1}{2}|a_i|^2 \tag{8}$$

and for the backward wave one has:

$$P_i^- = \frac{1}{2} \frac{\left|V_i^-\right|^2}{Z_{0,i}} = \frac{1}{2}|b_i|^2 \tag{9}$$

In order to compute the total active power entering the port one can write:

$$P = \Re\left\{\frac{1}{2} V_i I_i^*\right\} \tag{10}$$

and considering both (5) and (6) one has:

$$P = \Re\left\{\frac{1}{2}\left(V_i^+ + V_i^-\right)\left(I_i^+ + I_i^-\right)^*\right\}$$

which, after some manipulation, can be written as:

$$P = \frac{1}{2} \frac{\left|V_i^+\right|^2}{Z_{0,i}} - \frac{1}{2} \frac{\left|V_i^-\right|^2}{Z_{0,i}} = \frac{1}{2}|a_i|^2 - \frac{1}{2}|b_i|^2$$

that is the difference between the power flowing toward the port and the power reflected by the port. The *scattering matrix* allows to describe any linear system through the superposition of forward and backward waves by means of the following equation:

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_i \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & \dots & \dots & S_{1n} \\ S_{21} & S_{22} & \dots & \dots & \dots & S_{2n} \\ \vdots & \vdots & \ddots & & & \vdots \\ S_{i1} & S_{i2} & & \ddots & & S_{in} \\ \vdots & \vdots & & & \ddots & \vdots \\ S_{n1} & S_{2n} & \dots & \dots & \dots & S_{nn} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_i \\ \vdots \\ a_n \end{bmatrix} \tag{11}$$

where each *scattering parameter* is defined as:

$$S_{ij} = \left.\frac{b_i}{a_j}\right|_{a_k=0,\ \forall k \neq j} \tag{12}$$

when all other ports are connected to a matched load. Consider the two ports network depicted in figure 5: the reflective coefficient at port 1 can be written as:

$$\Gamma_1 = \frac{b_1}{a_1} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{13}$$

while the reflective coefficient at port 2, also called the *load*-port, can be written as:

$$\Gamma_2 = \Gamma_L = \frac{b_2}{a_2} = \frac{Z_2 - Z_0}{Z_2 + Z_0} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{14}$$

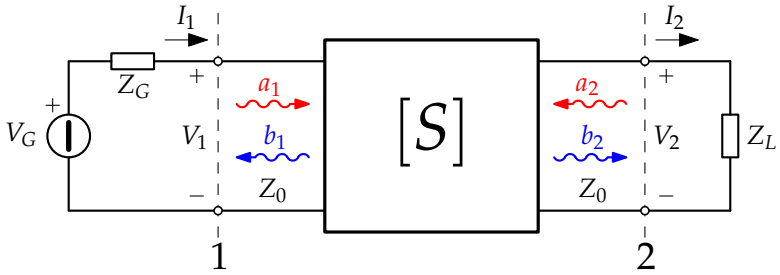


Figure 5: two ports network.

By exploiting the definition of scattering matrix one writes:

$$\begin{cases} b_1 = S_{11}\, a_1 + S_{12}\, a_2 \\ b_2 = S_{21}\, a_1 + S_{22}\, a_2 \end{cases} \tag{15}$$

and replacing (13) and (14) into (15) one obtains:

$$\Gamma_1 = S_{11} + \frac{S_{12}S_{21}}{1 - S_{22}}\Gamma_L \tag{16}$$

From such equation, one discovers that $S_{11} \equiv \Gamma_1$ only if $\Gamma_L = 0$, that is, the output port is actually connected to a matched load.

2.2 DIFFERENTIAL SCATTERING PARAMETERS

Considering the same generic two-port network of 5 in which input voltage and input current are denoted with v_1 and i_1, while output voltage and output current are denoted with v_2 and i_2, one can write the following system of equations:

$$\begin{cases} v_1 = Z_{11}\, i_1 + Z_{12}\, i_2 \\ v_2 = Z_{21}\, i_1 + Z_{22}\, i_2 \end{cases} \tag{17}$$

It is possible to define the *differential* and the *common mode voltages* as:

$$v_{\text{dm}} \triangleq v_1 - v_2 \tag{18}$$

$$v_{\text{cm}} \triangleq \frac{v_1 + v_2}{2} \tag{19}$$

and the *differential* and the *common mode currents* as:

$$i_{\text{dm}} \triangleq \frac{i_1 - i_2}{2} \tag{20}$$

$$i_{\text{cm}} \triangleq i_1 + i_2 \tag{21}$$

The *differential mode impedance* can be computed as:

$$z_{\text{dm}} \triangleq \frac{v_{\text{dm}}}{i_{\text{dm}}} = 2(Z_{11} - Z_{12}) \tag{22}$$

and the *common mode impedance* as:

$$z_{\text{cm}} \triangleq \frac{v_{\text{cm}}}{i_{\text{cm}}} = \frac{Z_{11} + Z_{12}}{2} \tag{23}$$

The single ended impedance can be derived by connecting one of the two differential terminals to ground giving:

$$z_{\text{se}} \triangleq \frac{v_1}{i_1} = Z_{11} + Z_{12} \tag{24}$$

2.3 DISTORTION

A system is said to be *linear* if its output depends on the applied input through the following relationship:

$$y(t) = \alpha \cdot x(t) \tag{25}$$

where α can be a function of time in case of a time-variant system. The meaning of such expression is that the output is directly proportional to the input or the output is a scaled copy of the input. For a non-linear system, however, one may write the input/output characteristic using a polynomial approximation:

$$y(t) = \alpha_0 + \alpha_1 \cdot x(t) + \alpha_2 \cdot x^2(t) + \alpha_3 \cdot x^3(t) + \dots \tag{26}$$

Now, clearly, the proportionality between input and output doesn't hold anymore since higher order terms of $x(t)$ are present. In practice the system is linearized in the sense a small signal model is derived and the (26) can be well approximated with (25). In other words, if the input remains confined into a certain interval, the output will follow quite accurately a straight line with a certain slope and it will lies on such line as the input moves inside the allowed region.

If the device is no more operating in the linear region, then it generates distortion which can be detected in the form of harmonics and intermodulation products.

2.3.1 Harmonic distortion

Consider a non linear system expressed by a third order polynomial of the form (26) to which a sinusoid is applied. Taking a look at the output of such system, one notes that, in addition to an amplified (or attenuated) tone centred at the input sinusoid frequency, the output shows other tones at integer multiples of the initial input frequency. In fact, given:

$$x(t) = A \cos \omega t \tag{27}$$

then:

$$\begin{aligned} y(t) &= \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t \\ &= \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2} (1 + \cos 2\omega t) + \frac{\alpha_3 A^3}{4} (3 \cos \omega t + \cos 3\, \omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3}{4} \alpha_3 A^3 \right) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\, \omega t \end{aligned} \tag{28}$$

where, besides the second term, which is the amplified input signal, called the *fundamental*, one has a dc component caused by the second order non linearity, a second order harmonic and a third order harmonic. In general, one can state that the even-order harmonics introduces dc components while odd-order harmonics influences the scale factor of the input signal as can be noticed in (28).

One may then focus on the output signal amplitude of the fundamental harmonic, that is $\alpha_1 A + \frac{3}{4}\alpha_3 A^3$. The input signal is thus multiplied by a factor equal to $\alpha_1 + \frac{3}{4}\alpha_3 A^2$ where the product $\alpha_1 \cdot \alpha_3$ may be negative, especially for RF circuits like the differential pair. If this is the case, the gain experiences a compression when the input signal overcomes a certain amount of power.

A practical way to characterize such phenomena for a particular circuit is the *1-dB compression point measurement*. In such a point, the amplitude of the signal applied to the input is such that it causes a 1-dB drop from the theoretical gain. The reasoning can be done both with voltage and power quantities.

In order to calculate the 1-dB intercept point, the following expression can be derived:

$$20 \log \left| \alpha_1 \frac{3}{4} \alpha_3 A^2_{\text{in, 1dB}} \right| = 20 \log |\alpha_1| - 1\text{dB}$$

from which:

$$A^2_{\text{in, 1dB}} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}$$

It is very important to notice that the 1-dB compression point represents a 10% reduction in the gain. The concept can be also understood considering figure (6) where the theoretical and the real behaviour of an amplifier gain are compared.

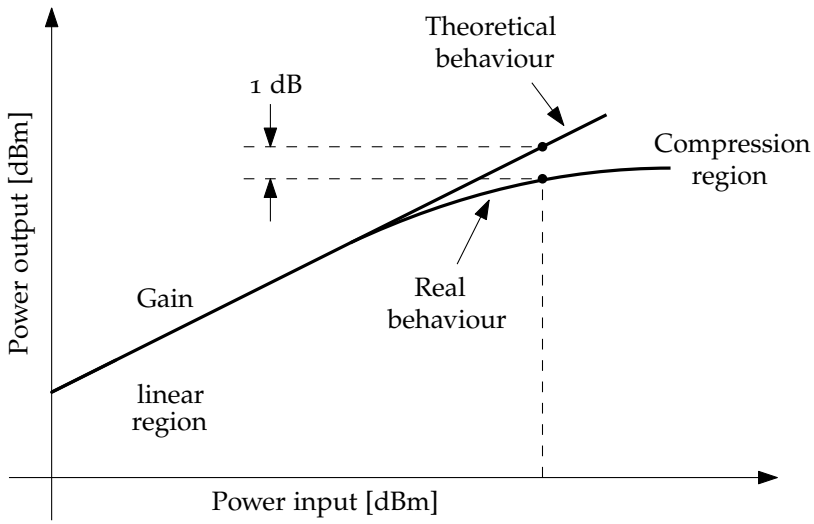


Figure 6: 1-dB compression point plot.

As can be noticed, input and output signals are well linearly related up to a certain input value, from which the gain starts decreasing, flattening the amplifier characteristic and entering the *compression region*.

2.3.2 Intermodulation distortion

Intermodulation appears when two or more signals are applied to a non linear system. The mixing of such signals produces new ones located at the sum and at the difference of the original frequencies of the input signals which can be called ω_1 and ω_2. Such tones can also mix with each others like $2\omega_1$ and $2\omega_2$, $3\omega_1$ and $3\omega_2$ etc. The extra products will be created at frequencies $2\omega_1 + \omega_2$, $2\omega_1 - \omega_2$, $2\omega_2 + \omega_1$, $2\omega_2 - \omega_1$ and so on and so forth. The order of harmonics and intermodulation is the sum of their coefficients without sign: $2\omega_1$ is called *second* order as well as $\omega_1 + \omega_2$, while $3\omega_1$, $2\omega_2 - \omega_1$ and $2\omega_2 - \omega_1$ are *third* order. The last two intermodulation products are very important in characterizing the linearity of an amplifier. In order to understand why, consider figure 8. In such plot, the 1st, the 2nd and the 3rd order products are depicted. As can

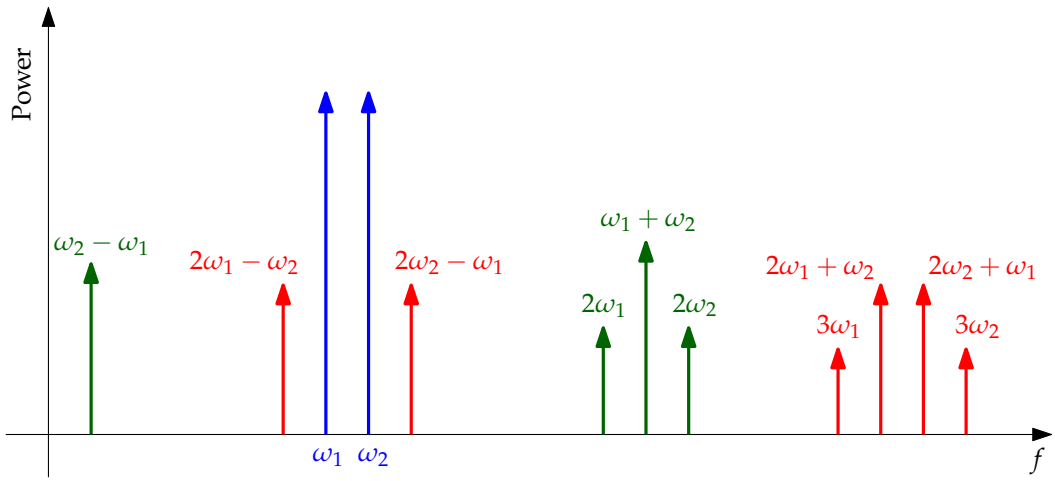


Figure 7: intermodulation distortion spectrum.

be noticed, the last product appears very close to the two input tones, likely causing leakage into the adjacent channels. Some of the intermodulation products are not so difficult to remove since higher order harmonics have very low amplitude and can be ignored and higher-frequency products typically fall outside the amplifier and/or the filter bandwidths. However, this is very hard to happen with the products highlighted before since they fall very close to the input signal amplified tones. The undesired intermodulation is usually referred to as *intermodulation distortion*. That's why they are most important tones to be concerned of.

Apart from the filtering problem, there's another important aspect related to the third-order intermodulation products to mention. Let's assume:

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{29}$$

If one is dealing with a third order polynomial system, the output can be written as:

$$\begin{aligned} y(t) =& \alpha_1 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2\right) + \alpha_2 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2\right)^2 \\ &+ \alpha_3 \left(A_1 \cos \omega_1 t + A_2 \cos \omega_2\right)^3 \end{aligned} \tag{30}$$

developing the left side of the expression, discarding the harmonics and the tone at $\omega_1 + \omega_2$, the following terms can be obtained:

$$\omega = 2\omega_1 \pm \omega_2 \ : \quad \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\omega_1 - \omega_2)t \tag{31}$$

$$\omega = 2\omega_2 \pm \omega_1 \ : \quad \frac{3}{4}\alpha_3 A_1 A_2^2 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}\alpha_3 A_1 A_2^2 \cos(2\omega_1 - \omega_2)t \tag{32}$$

as well as the following fundamental components:

$$\omega = \omega_1,\ \omega_2 \ : \quad \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos\omega_1 t + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_1^2 A_2\right)\cos\omega_2 t \tag{33}$$

It is important to note that the amplitude of the intermodulation products is proportional to A^3 hence, translating into a logarithmic scale, for every 1dB increase in the useful (fundamental) signal, the third order intermodulation product increases in level by 3dB, hence much more quickly. The concept is depicted in figure 8.

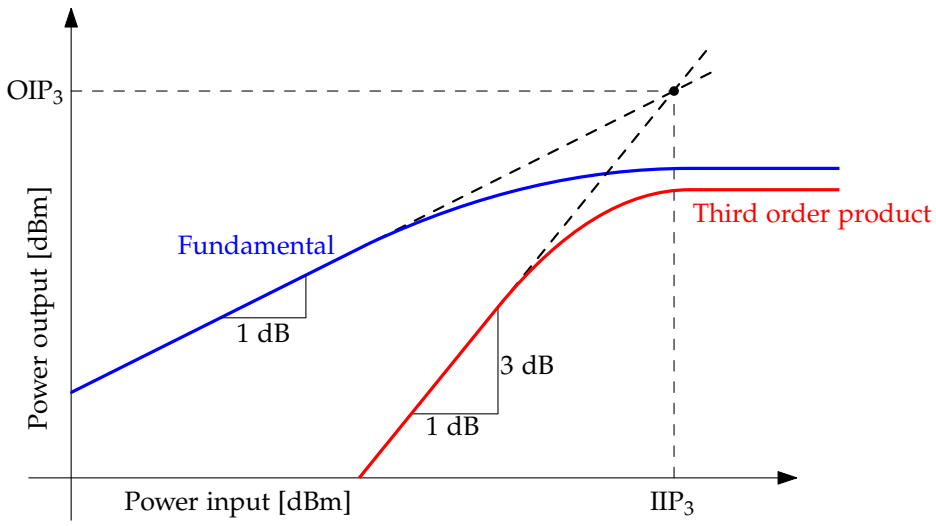


Figure 8: third order intercept point plot.

If one consider an ideal behaviour, the two gain lines are supposed to intercept each other at a certain point. Such a point is called the *third order intercept point*, *TOI* or *IP3* for short.

The higher the IP3, the better the linearity and the lower the level of intermodulation distortion of the device under test (DUT).

Remembering what discussed in the previous subsection, at a certain input power, the output power is no longer linearly increasing with the input power. Thus the third order intercept point is a *theoretical* value that can be *calculated* starting *from measured* values.

In practice, the IP3 is measured by sending two signals into the DUT; these tones are closely spaced and unmodulated signals with equal amplitude. The levels of these two fundamental signals and their adjacent third-order intermodulation products, called

P_{IM3}, are measured. The third order intercept is then computed from these level values by using (34).

$$\text{IIP3} = P_{\text{tone}} + \frac{P_\delta}{2} \tag{34}$$

where P_{tone} is the power of the applied input tone while P_δ is the power level difference between the TOI3 and the input signal.

2.4 NOISE IN ANALOGUE INTEGRATED CIRCUITS

Noise is a constant issue in electronics hence tools for analysing its impact are essential. Instantaneous value of noise in the time domain cannot be predicted hence a *statistical model* for the noise is used instead. However, in many cases, the average power of the noise can be predicted.

Noise is usually modelled as a random process, in particular an ergodic and stationary in strict sense process. One can then compute the average value for a voltage noise source $v_n(t)$ as:

$$\overline{v_n(t)} = \lim_{T\to\infty} \int_{-\frac{T}{2}}^{+\frac{T}{2}} v_n(t)\, dt = \langle v_n(t) \rangle = 0 \tag{35}$$

that is, the average value of the noise in the time domain is zero; the variance can be computed as well according to its definition:

$$\overline{v_n^2(t)} = \lim_{T\to\infty} \int_{-\frac{T}{2}}^{+\frac{T}{2}} \left(\langle v_n(t) \rangle - v_n(t)\right)^2 dt = \lim_{T\to\infty} \int_{-\frac{T}{2}}^{+\frac{T}{2}} v_n^2(t)\, dt = \langle v_n^2(t) \rangle = \sigma_{v_n}^2 \tag{36}$$

From basic circuit theory, the *average power* delivered by a periodic voltage $v(t)$ to a load resistance R_L is given by:

$$P_{\text{av}} = \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} \frac{|v(t)|^2}{R_L}\, dt \tag{37}$$

that can be visualized as the average heat produced by R_L and cause by the applied voltage $v(t)$. Since noise is aperiodic, the measurement must be carried out over a long time instead of a period T hence (37) becomes:

$$P_{\text{av}} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} \frac{|v_n(t)|^2}{R_L}\, dt \tag{38}$$

and it is practical to get rid of the resistance on which the power is computed. The idea is then to compute instead:

$$P_{\text{av, norm}} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} |x_n(t)|^2\, dt$$

which now clarifies from a practical point of view the definitions given in (35) and (36). In practice the *Power Spectral Density*, or PSD, is often defined in order to show how the power of the signal is distributed in the frequency spectrum. The PSD of a noisy waveform $x_n(t)$, $S_{x_n}(f)$, is defined as:

$$S_X(f) = \lim_{\Delta f\to 0} \frac{x_n^2(f)}{\Delta f} \tag{39}$$

and the power contained in the band $B = [f_1,\ f_2]$ can be computed as:

$$P_{\text{tot}} = \int_{f_1}^{f_2} S_X(f)\ df \tag{40}$$

Most of the noise sources of interest exhibit a predictable spectrum. Like the definition of P_{av} it is customary to eliminate R_L from $S_X(f)$, hence the unit of measure is expressed in V^2/Hz. An example of a common type of noise PSD is the white spectrum, also called the *white noise*. Such a PSD displays the same value at all frequency up to about 100THz.

If a signal with spectrum $S_X(f)$ is applied to a linear time-invariant system with transfer function $H(f)$, then the output spectrum is given by

$$S_Y(f) = S_X(f)|H(f)|^2$$

It's important to say that $S_X(f)$ is an even function of the function if $x(t)$ is a real signal, hence the total power carried by $x(t)$ in the frequency range $[f_1,\ f_2]$ is simply equal to:

$$P_{\text{tot}} = \int_{-f_2}^{-f_1} S_X(f)\ df + \int_{f_1}^{f_2} S_X(f)\ df = \int_{f_1}^{f_2} 2S_X(f)\ df$$

One can distinguish between two sided and one sided PSD. The spectrum shows the power carried in a small bandwidth at each frequency, revealing how fast the waveform is expected to vary in the time domain.

In order to compute the effect of several noise sources one has to consider the definition of power for two signals $x_1(t)$ and $x_2(t)$:

$$\begin{aligned}
P_{av} &= \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} [x_1(t) + x_2(t)]^2\ dt \\
&= \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} x_1^2(t)\ dt + \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} x_2^2(t)\ dt + \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} 2x_1(t)x_2(t)\ dt \\
&= P_{av_1} + P_{av_2} + \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} 2x_1(t)x_2(t)\ dt
\end{aligned}$$

which is the sum of the average power of $x_1(t)$ and $x_2(t)$ and a third term which tells how similar these two waveforms are.

If sources are uncorrelated, that is each of one is independent of each other, the superposition principle holds and the third terms is null.

2.4.1 Types of noise

In analogue circuits there are two main types of noise: noise generated by electronic devices themself and environmental noise that a circuit experiences through the supply or ground lines. Here some noise sources of the former type are presented:

- *resistor thermal noise* which spectral density can be written as:

$$S_v(f) = 4k_{\text{B}}TR \tag{41}$$

$$S_i(f) = \frac{4k_{\text{B}}T}{R} \tag{42}$$

where $k_B \simeq 1.38 \cdot 10^{-23}$J/K is the Boltzmann constant. Since $S_v(f)$ is expressed in V^2/Hz one can write $\overline{v_n^2}$ and define it as the average value per unit bandwidth ($\Delta f = 1$Hz).

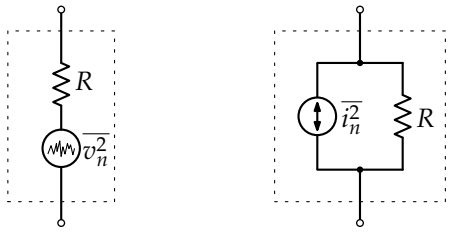


Figure 9: equivalent thermal noise models for a resistor.

- *MOS transistor thermal noise* is given by the following expression:

$$\left.\frac{\overline{i_{th}^2}}{\Delta f}\right|_{\Delta f=1} = \overline{i_{th}^2} = 4kT\frac{\gamma}{\alpha}g_m \tag{43}$$

where γ and α are device parameters that depends on the technology, g_m is the device transconductance under the hypothesis of strong saturation working region;

- *MOS transistor flicker noise* which is related to the extra energy states that appear at the end of the silicon crystal interface. This is called the *flicker noise* and it is usually modelled by a voltage source in series with the gate and it is given by:

$$\left.\frac{\overline{i_{1/f}^2}}{\Delta f}\right|_{\Delta f=1} = \overline{i_{1/f}^2} = \frac{K_f I_D}{C_{ox} L^2} \cdot \frac{1}{f} \tag{44}$$

where K_f is a process-dependent constant on the order of $10^{-25}V^2$ F. Hence, for the MOS transistor:

$$\overline{i_{d,n}^2} = \overline{i_{th}^2} + \overline{i_{1/f}^2} \tag{45}$$

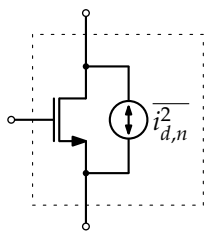


Figure 10: equivalent thermal noise model for a MOS transistor.

All the notation used in this section, as reported, assumes the use of a bandwidth equal to $\Delta f = 1$Hz. Other books and articles may used different notation though. For further investigation on this topic, see [24] and [11].

2.4.2 Noise Figure

Among the figures of merit the *noise figure* is one of the most important for a signal processing circuit. Considering a generic input-output system where the input signal is characterized by a Signal to Noise Ratio SNR_{in}, the output is characterized by a SNR_{out} which, in the ideal case, coincides with SNR_{in}; however, in practice, due to the system internal noise sources, such relation does not hold. The noise figure parameter quantifies the SNR degradation for a system both in the linear and in the logarithmic scale:

$$\mathrm{F} \triangleq \frac{\mathrm{SNR}_{in}}{\mathrm{SNR}_{out}} \tag{46}$$

$$\mathrm{NF} \triangleq 10 \log_{10} \mathrm{F} \tag{47}$$

Considering a cascade of electronic systems like the one reported in figure (11), the Friis equation states that:

$$\mathrm{F}_{\mathrm{casc}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3} + \cdots + \frac{F_n - 1}{G_1 \cdot G_2 \cdot \ldots G_{n-1}} \tag{48}$$

where F_k and G_k, $k = 1, 2, ; n$ are the noise figure and the power gain of each device in the chain. Because of this relationship, the first block, connected to the signal source,

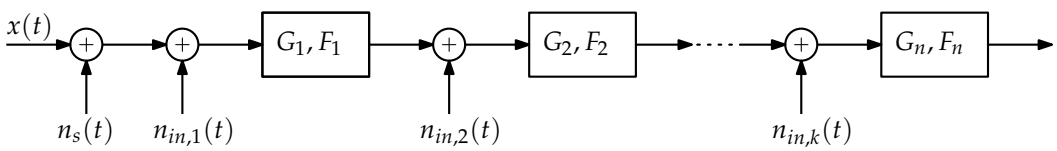


Figure 11: cascade connection of different gain blocks.

has to be carefully design and should be an active one in order that the following stage have a reduced noise figure.

2.4.3 Two-port noise figure derivation

Usually, to represent a noisy circuit an equivalent input noise voltage source and an input noise current source are used. Figure 12 shows the scheme used by the IEEE standard.

Let us consider the two types of noise sources being correlated each other, and taking the correlation with reference to the noise voltage source, v_n, in such a way that:

$$i_n = i_u + i_c = i_u + Y_{\mathrm{cor}} v_n \tag{49}$$

where Y_{cor} is the correlation admittance defined as follows:

$$Y_{\mathrm{cor}} \triangleq \frac{\overline{i_n \times v_n^*}}{\overline{v_n^2}} = G_{\mathrm{cor}} + jB_{\mathrm{cor}} \tag{50}$$

The noise resistance is defined as:

$$R_n \triangleq \frac{\overline{v_n^2}}{4k_B T} \tag{51}$$

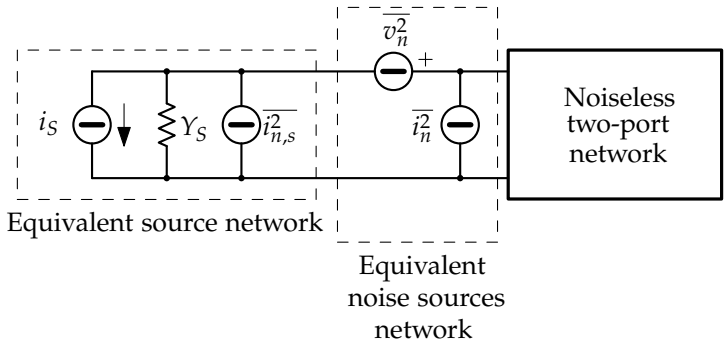


Figure 12: Equivalent schematic for representing a noisy network by means of an equivalent input noise voltage source and an equivalent input noise current source.

The noise conductance is defined as:

$$G_u \triangleq \frac{\overline{i_u^2}}{4k_B T} \tag{52}$$

Considering the short-circuit currents at the input of the network, one obtains the following expression:

$$i_{sc,tot} = i_{n,s} + i_n + Y_S v_n = i_{n,s} + i_u + (Y_S + Y_{\text{cor}})\, v_n \ , \quad i_{n,s} = 4k_B T \Delta f G_S$$

The noise figure can be computed by definition as:

$$F = \frac{i_{sc,tot}}{i_{n,S}} = 1 + \frac{\overline{i_u^2}}{\overline{i_{n,S}^2}} + \frac{\overline{v_n^2}\,|Y_{\text{cor}} + Y_S|^2}{\overline{i_{n,S}^2}} \tag{53}$$

which can be further written as:

$$F = 1 + \frac{R_n}{G_u}\,|Y_{\text{cor}} + Y_S|^2 + \frac{G_u}{G_S} \tag{54}$$

If one differentiates (54) with respect to G_S and B_S the minimum noise figure is:

$$F_{min} = 1 + 2R_n\left(G_{\text{cor}} + G_{opt}\right) \tag{55}$$

where the optimum noise admittance, G_{opt}, can be obtained computing:

$$G_{opt} = \sqrt{G_{\text{cor}}^2 + \frac{G_u}{R_n}} \ , \quad B_{opt} = 0 \ , \quad Y_{opt} = G_{opt} + jB_{opt} \tag{56}$$

The expression (53) can be rewritten as:

$$F = F_{min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 \tag{57}$$

If one makes he hypothesis of having uncorrelated noise sources, $\overline{v_n^2}$ and $\overline{i_n^2}$, then, by representing them as a single, equivalent noise source:

$$\overline{v_{eq}^2} = \overline{v_n^2} + \overline{i_n^2} R_s^2 \tag{58}$$

the noise figure is given by:

$$F = 1 + \frac{\overline{v_{eq}^2}}{\overline{v_s^2}} = 1 + \frac{R_n}{R_s} + G_n R_s \tag{59}$$

where:

$$\overline{v_n^2} = 4k_B T R_n \ , \quad \overline{i_n^2} = 4k_B T G_n \tag{60}$$

The optimum R_s can be found by finding the minimum for the noise figure expression:

$$\frac{\partial F}{\partial R_s} = 0 \quad \Leftrightarrow \quad G_n - \frac{R_n}{R_s^2} = 0 \tag{61}$$

Hence, in the case of uncorrelated voltage and current sources, one has:

$$R_{opt} = \sqrt{\frac{R_n}{G_n}} \tag{62}$$

while the minimum noise figure expression becomes:

$$F_{min} = 1 + 2\sqrt{R_n G_n} \tag{63}$$

To better understand how to deal with the noise figure in a practical case, consider a simple example of a passive network: let's compute the equivalent input referred noise sources for the pi-pad (pi network) depicted in figure 13. The procedure for the

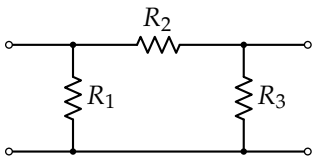


Figure 13: Pi-pad network schematic for the two-port noise figure example.

computation of $\overline{v_n^2}$ and $\overline{i_n^2}$ consists in two main steps:

1. in order to evaluate $\overline{v_n^2}$, consider figure 14 where the input and the output ports are shorted: one computes i_{sc} both for the circuit on the left and for the circuit on the right as function of the noise sources, for instance applying the superposition theorem. The two results are then compared in order to find the expression of v_n:

$$i_{sc,1,2,3} = \frac{v_{n,2}}{R_2} + \frac{v_{n,3}}{R_2} \ , \quad i_{sc,n} = \frac{v_n}{R_2}$$

   from which:

$$v_n = v_{n,2} + \frac{R_2}{R_3} v_{n,3} \tag{64}$$

2. in order to evaluate $\overline{i_n^2}$, consider figure 15 where the input and the output port are open: one computes v_{oc} both for the circuit on the left and for the circuit on the right. The two results are then compared in order to find the expression of i_n:

$$v_{oc,1,2,3} = \frac{R_3}{R_1 + R_2 + R_3} v_{n,1} + \frac{R_3}{R_1 + R_2 + R_3} v_{n,2} + \frac{R_1 + R_2}{R_1 + R_2 + R_3} v_{n,3} \ ,$$

$$v_{oc,n} = \frac{R_1 R_3}{R_1 + R_2 + R_3} i_n$$

from which:

$$i_n = \frac{v_{n,1}}{R_1} + \frac{v_{n,2}}{R_1} + \frac{R_1 + R_2}{R_1 R_3} v_{n,3} \tag{65}$$

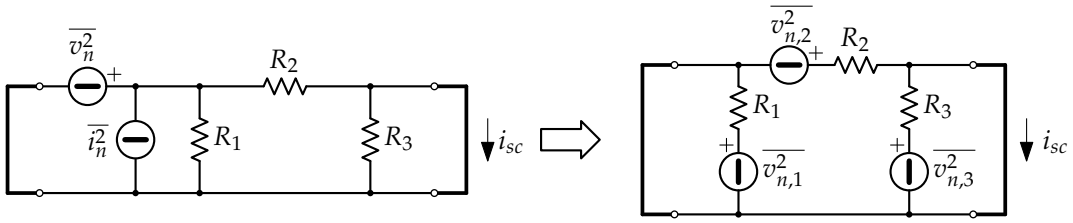


Figure 14: modified network for the input noise voltage source computation.

Once obtained the two expressions for i_n and v_n, one is able to compute all the useful quantities; starting from:

$$\begin{aligned}\overline{i_n \cdot v_n^*} &= \begin{pmatrix} f(v_{n1}) \\ f(v_{n2}) \\ f(v_{n3}) \end{pmatrix} \cdot \begin{pmatrix} g(v_{n1})^* \\ g(v_{n2})^* \\ g(v_{n3})^* \end{pmatrix} = \begin{pmatrix} \frac{v_{n,1}}{R_1} \\ \frac{v_{n,2}}{R_1} \\ \frac{R_1+R_2}{R_1 R_3} v_{n,3} \end{pmatrix} \cdot \begin{pmatrix} 0 \\ v_{n,2} \\ \frac{R_2}{R_3} v_{n,3} \end{pmatrix} \\ &= \frac{\overline{v_{n,2}^2}}{R_1} + \frac{R_2}{R_3} \cdot \frac{R_1 + R_2}{R_1 R_3} \cdot \overline{v_{n,3}^2}\end{aligned} \tag{66}$$

where the $\cdot$ (dot) symbol is used with the meaning of product between correspondent vector components. The noise resistance is evaluated as:

$$R_n = \frac{\overline{v_n^2}}{4k_B T} = \frac{1}{4k_B T}\left(\overline{v_{n2}^2} + \frac{R_2^2}{R_3^2}\overline{v_{n,3}^2}\right) = R_2\left(1 + \frac{R_2}{R_3}\right) \tag{67}$$

The correlation admittance is computed as:

$$Y_{\text{cor}} = \frac{\overline{i_n \cdot v_n^*}}{\overline{v_n^2}} = \frac{R_2}{R_1} \cdot \frac{1}{R_n} + \frac{R_2}{R_3}\left(1 + \frac{R_2}{R_1}\right) \cdot \frac{1}{R_n} = \frac{R_1 + R_2 + R_3}{R_1(R_1 + R_3)} \tag{68}$$

and the noise conductance is obtained considering that:

$$i_u = i_n - Y_{\text{cor}} \cdot v_n$$

and so, from its definition, it results:

$$G_u = \frac{\overline{i_u^2}}{4k_B T} = \frac{R_1 + R_2 + R_3}{R_1(R_1 + R_3)} \equiv Y_{\text{cor}} \tag{69}$$

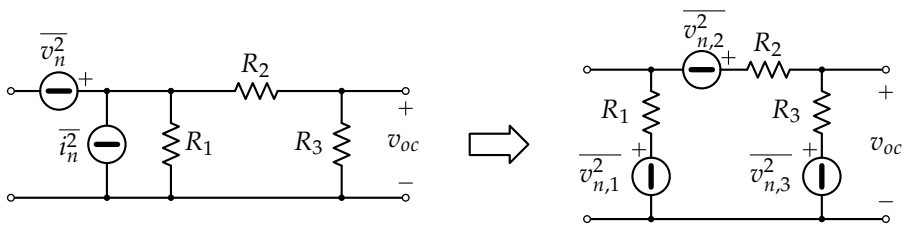


Figure 15: modified network for the input noise current source computation.

The correlation conductance is extracted from Y_{cor}:

$$G_{\text{cor}} = \Re\{Y_{\text{cor}}\} \equiv Y_{\text{cor}} = \frac{R_1 + R_2 + R_3}{R_1(R_1 + R_3)} = G_u \tag{70}$$

Finally is possible to compute Y_{OPT} for the pi-pad network:

$$Y_{OPT} = \frac{1}{Z_{OPT}} = \frac{1}{R_2 + R_3}\sqrt{\frac{(R_1 + R_2 + R_3)(R_1R_2 + R_2^2 + R_2R_3 + R_1R_3)}{R_1^2R_2}} \tag{71}$$

2.4.4 Cascade of two-port networks

Considering figure 16, according to Friis formula, the total noise figure for the cascade of two-port networks can be expressed as:

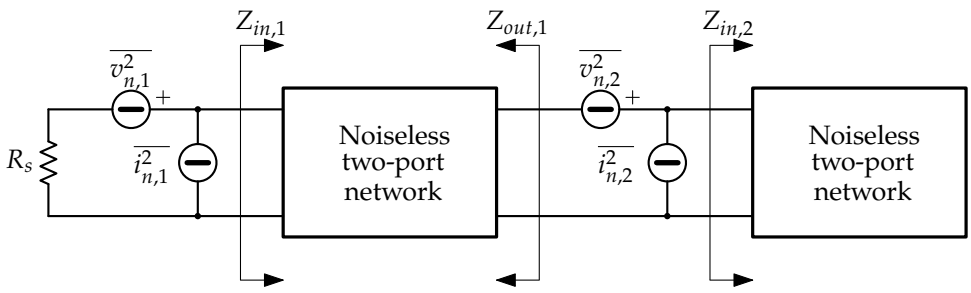


Figure 16: cascade of two noisy two-port networks.

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_1} \tag{72}$$

Each block features its one noise figure, in this case F_1 and F_2: the latter can be computed by using (53). Hence each block has its $R_{n,k}$, $G_{u,k}$, with k the associated block number, and so on and so forth. By substituting the two different noise figure expressions for the two two-port network into (72) under the hypothesis of having $\overline{v_n^2}$ and $\overline{i_n^2}$ uncorrelated, one obtains the following result:

$$F_{tot} = 1 + G_{n,1}R_s + \frac{G_{n,2}\,R_{out,1}}{A_{v_1}} + \frac{R_{n,1}}{R_s} + \frac{R_{n,2}}{R_{out,1}\,A_{v,1}} \tag{73}$$

where $R_{out,1}$ plays the same role of the source resistance R_s but for the second two-port network.

2.5 CASCODE AMPLIFIER

One of the most adopted amplifier configuration, also exploited in the LNTA of this thesis, is the *cascode amplifier*. Such configuration combines the advantages of common source and common gate amplifiers.

2.5.1 Small signal parameters

The structure of the Cascode amplifier as well as the correspondent two port model are reported in figure 17. At low frequency, the common gate stage behaves like a current

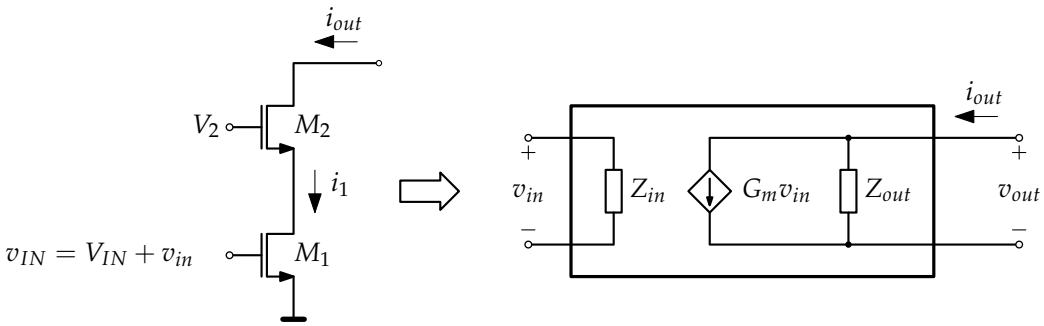


Figure 17: cascode amplifier configuration and equivalent two port model circuit.

buffer, that is $\beta_{CG} = i_{out}/i_o \simeq 1$. Thus, neglecting the channel length modulation, the transconductance gain is $G_m \simeq g_{m1}$. A small signal model representation of the cascode amplifier is shown in figure 18: the capacitances C_i and C_o are defined in the following way:

$$C_i = C_{gs_2} + C_{sb_2}\ , \quad C_o = C_{gd_2} + C_{db_2} \tag{74}$$

Notice the omnipresent of capacitance C_{gd} of the common source stage which effect

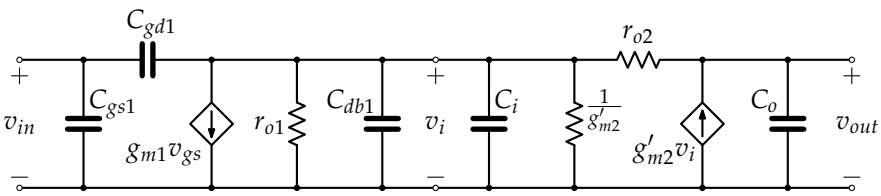


Figure 18: cascode amplifier small signal model.

is now mitigated by the low input impedance of the cascaded common gate amplifier. Because of that, the input impedance seen from the common source stage can be written as:

$$Z_{\text{in}} = R_g + \frac{1}{s\left[C_{\text{gs}} + \left(1 + \frac{g_{\text{m1}}}{g'_{\text{m2}}} C_{\text{gd1}}\right)\right]} \simeq \frac{1}{s\left[C_{\text{gs}} + \left(1 + \frac{g_{\text{m1}}}{g'_{m2}} C_{\text{gd1}}\right)\right]} \tag{75}$$

The Miller effect is mitigated because of the low input impedance of the current buffer and the gate resistance R_g can be neglected quite always. The output impedance is:

$$\begin{aligned} Z_{out} &= \frac{r_{0_1} + r_{0_2} + g'_{\text{m2}} r_{0_1} r_{0_2}}{1 + s(C_{\text{gd2}} + C_{db2})(r_{01} + r_{02} + g'_{m2} r_{01} r_{02})} \\ &\simeq \frac{g'_{m2} r_{01} r_{02}}{1 + s(C_{gd2} + C_{db2}) g'_{m2} r_{01} r_{02}} \end{aligned} \tag{76}$$

The voltage gain from input to output at dc is:

$$A_v\big|_{\omega=0} = G_m Z_{out}\big|_{\omega=0} = G_m \cdot R_{out} \simeq g_{m1} r_{01} \cdot g'_{m2} r_{02} \tag{77}$$

At high frequency, an additional pole due to the parasitic output capacitances is present:

$$G_m(s) = g_{m1} \cdot \beta_{CG}(s) \simeq \frac{g_{m1}}{1 + s\left(\frac{C_{gs2}+C_{sb2}+C_{db1}}{g'_{m2}}\right)} \tag{78}$$

2.5.2 Cascode noise parameters (IEEE noise parameters)

As reported in a previous section, the two port noise parameters of the cascode device can be computed. The equivalent input noise voltage source, from figure 19, is:

$$\overline{v_n^2} = \frac{\overline{i_{d,n}^2}}{g_m^2} + \overline{v_{n,g}^2} = \frac{4k_BT}{g_\mathrm{m}}\left(\frac{\gamma}{\alpha}\right) + 4k_BTR_\mathrm{g} \tag{79}$$

while the equivalent input noise current source, considering figure 19, is:

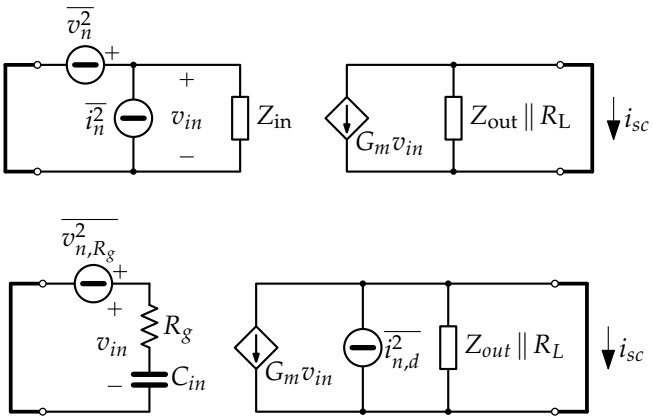


Figure 19: cascode model for the input referred voltage noise computation.

$$\overline{i_n^2} = \left|\frac{1}{R_g + \frac{1}{j\omega C_{in}}}\right|^2 \cdot \frac{\overline{i_{n,d}^2}}{g_m^2} = \frac{4k_BTg_\mathrm{m}}{1+\omega^2R_g^2C_\mathrm{in}^2}\left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 \tag{80}$$

where $\omega_{in} = \frac{1}{R_gC_{in}}$ in order to simplify the notation. The noise resistance is:

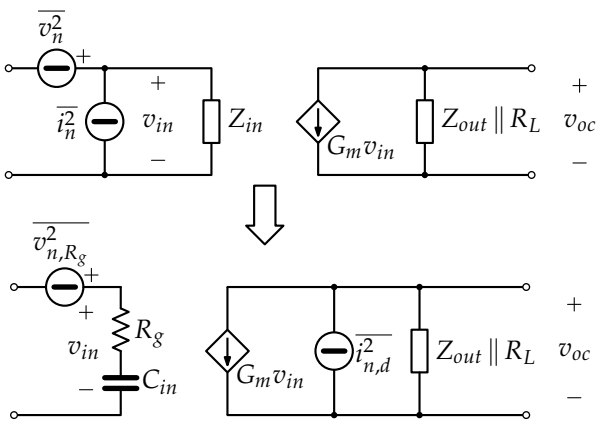


Figure 20: cascode model for the input referred current noise computation.

$$R_n = \frac{\overline{v_n^2}}{4k_BT} = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} + R_g \simeq \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{81}$$

while:

$$\overline{i_n \cdot v_n^*} = \frac{1}{g_m} \cdot \frac{j\omega C_{in}}{1 + j\omega R_g C_{in}} \cdot \overline{i_{n,d}^2} \tag{82}$$

The correlation admittance expression holds:

$$Y_{cor} = \frac{\overline{i_n \cdot v_n^*}}{\overline{v_n^2}} = \frac{1}{g_m} \cdot \frac{j\omega C_{in}}{1 + j\omega R_g C_{in}} \cdot \frac{1}{\frac{\gamma}{\alpha} \cdot \frac{1}{g_m} + R_g} = \frac{1}{g_m} \cdot \frac{j\omega C_{in}}{1 + j\omega R_g C_{in}} \cdot \frac{1}{g_m R_n} \tag{83}$$

and from that one can perform the computation of G_u which in turns leads to the estimation of the optimum input admittance for the amplifier:

$$G_u = \frac{\overline{i_u^2}}{4k_BT} = \left(\frac{H}{g_m}\right)^2 \left[\frac{1}{R_n} + \frac{\gamma}{\alpha} g_m - 2H\right] \tag{84}$$

And finally:

$$G_{opt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} \tag{85}$$

Considering the simpler approach of thinking $\overline{v_n^2}$ and $\overline{i_n^2}$ uncorrelated, computations are easier and give more understandable results:

$$F \simeq 1 + \frac{\overline{v_n^2} + \overline{i_n^2} R_s^2}{\overline{v_{n,R_s}^2}} \simeq 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right) g_m R_s \left(\frac{\omega}{\omega_T}\right)^2 \tag{86}$$

2.6 SUB-THRESHOLD OPERATING REGION

High speed circuits employ MOS transistors biased in the so called super-threshold region usually denoted as *saturation operating region*. However, when power consumption becomes an important aspect in the circuit design, one may consider to bias the transistors with very low currents and make them operating in the so called *sub-threshold* or *weak inversion region*.

The use of the MOS transistor in such region to perform very high-speed operations is not possible since the operating current is much lower than that in the triode or saturation (super-threshold) regions; this would require longer intervals of time to charge or discharge parasitic capacitance thus degrading the speed in digital circuits. Sub-threshold region is also cause of power leakage in such field of electronics since the not-nil current continues dissipating a considerable amount of power if one consider a nowadays processor can contain a billion and more of them.

In general, transistors designed to be operated in sub-threshold region can be made using the same fabrication process and with the same dimensions. Among the benefit of operating the MOS in such region, the transistor input capacitance is much less than that in the super-threshold hence, also for this reason, the power consumption will be much less than in other operating regions.

The demand of very low power, battery operated device has been rising over the year, forcing the scaling down of the power supply voltage. Scaling down the V_{DD} causes the threshold level of the device to be reduced to maintain the performance at an acceptable level; still, if this is the case, an increase of the sub-threshold leakage current and the associated rise in static power consumption.

2.6.1 MOS current behaviour in sub-threshold region

Considering the energy-band diagram of a MOS structure with a p-type substrate biased so that $\varphi_s < \varphi_{fp}$, the Fermi level is closer to the conduction band than to the valence band at the surface, hence the latter develops the characteristic of lightly doped n-type material. Thus, some conduction between the n-source and the n-drain contacts is expected at least in the form of minority carriers. The condition $\varphi_{fp} < \varphi_s < 2\varphi_{fp}$ is called *weak-inversion*. The drain current depends exponentially on the gate to source voltage of the MOS as stated in equation (87).

$$I_D = I_0 \cdot \exp\left(\frac{V_{GS} - V_{th0} - \gamma v_{sb} + \eta V_{DS}}{nV_T}\right) \cdot \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) , \tag{87}$$

where I_0, V_T and n are defined as:

$$I_0 \simeq \mu_0 C_{ox} \frac{W}{L} V_T^2 e^{1.8} , \quad V_T = \frac{k_B T}{q} , \quad n = \frac{C_{ox} + C_{depl}}{C_{ox}} \tag{88}$$

The parameter γ is the *linearized body-effect coefficient*, η represents the *drain-induced-barrier-lowering* or *DIBL* and V_{th0} is the *threshold voltage at zero source-to-substrate voltage*. Finally, n is the *sub-threshold swing factor*.

Neglecting the body-effect coefficient and the drain-induced barrier lowering coefficient, and considering $V_{DS} = 100\text{mV}$, then one can simplify the previous equation as:

$$I_D \simeq I_0 \cdot \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \tag{89}$$

2.6.2 Small signal analysis in sub-threshold region

In order to develop the ac small signal model for the sub-threshold operating region, let us assume the applied gate-to-source voltage is $v_{GS} = V_{GS} + v_{gs}$, considering (89), one can write:

$$i_D = I_0 \cdot \exp\left(\frac{V_{GS} + v_{gs} - V_{th}}{nV_T}\right) , \tag{90}$$

which can be split as follows:

$$i_D = I_0 \cdot \underbrace{\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)}_{\substack{\text{dc} \\ \text{components}}} \cdot \underbrace{\exp\left(\frac{v_{gs}}{nV_T}\right)}_{\substack{\text{ac} \\ \text{components}}} \tag{91}$$

The Taylor expansion can be used in order to extract the useful parameters for the small signal model:

$$\exp\left(\frac{v_{gs}}{nV_T}\right) = 1 + \frac{v_{gs}}{nV_T} + \left(\frac{v_{gs}}{nV_T}\right)^2 + \left(\frac{v_{gs}}{nV_T}\right)^3 + \dots ,$$

and, if $v_{gs} \ll nV_T$ one may neglect the higher order terms with respect to the first one, hence the total sub-threshold current can be written as the sum of a dc component, the biasing quantity, and an ac small-signal current of the first order:

$$i_D \simeq I_D + \frac{I_D}{nV_T} v_{gs} = I_D + g_m v_{gs} , \tag{92}$$

where:

$$g_m \triangleq \frac{I_D}{nV_T} \tag{93}$$

is the transconductance of the sub-threshold MOS.

The higher order terms in the Taylor expansion can be easily neglected only if the ac small signal voltage is less than one tenth the value of nV_T. That value os way less than its counterpart in the super-threshold device. It is possible to notice how the value of the transconductance parameter g_m is much less than that of the conventional MOS device since the current involved is much lower and also how similar it is to the BJT transistor.

The drain to source voltage is related to the sub-threshold current in the following way: considering equation (91), differentiating with respect to v_{ds} and considering the Taylor expansion up to the first order, then:

$$r_0 \triangleq \frac{v_{ds}}{i_D} \simeq \frac{nV_T}{\eta I_d} = \frac{1}{\eta g_m} . \tag{94}$$

Hence, depending on the value of η, it is possible to obtain a resistor controlled by v_{gs}, not possible if the transistor operates in super-threshold region.

The contribute of the body effect on the drain current can be studied with the same procedure: considering (87), differentiating with respect to v_{sb} and, as before, focusing on the Taylor expansion up to the first order, one can obtain:

$$g_{mb} = \frac{\gamma}{nV_T} I_D = \gamma g_m \tag{95}$$

Also the body-transconductance parameter is related to the main sub-threshold transconductance parameter. Now, one has all the parameters needed to build the small-signal equivalent model of the transistor, which is indeed the same of the super-threshold MOS except for the values of the single quantities. For further information, consider [25].

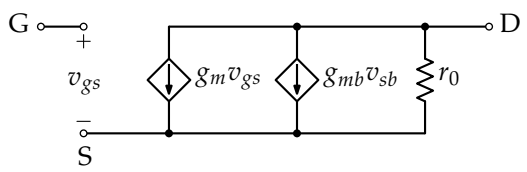


Figure 21: MOS sub-threshold region small signal model at low frequency.

2.6.3 High frequency model of the MOS in sub-threshold region

High frequency operation is not a well suited environment for operating MOS in sub-threshold for the reasons previously mentioned about the drain current. Very high speed circuits are in some way prohibited in such sense. However it is possible to reach, quite easily, up to few GHz, hence reaching the operating bandwidth of BT and BLE devices. For such reason, a look at the parasitic capacitances has to be done. Figure 22 shows the main important capacitances useful to consider at amplifier design stage. With respect

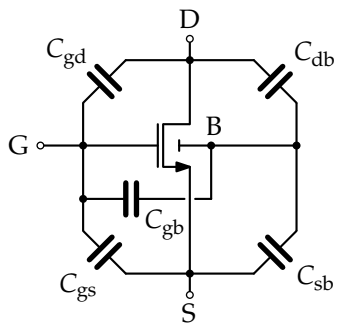


Figure 22: MOS sub-threshold parasitic capacitances.

to the super-threshold working region, the expressions for C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db} are reported in equation (96):

$$C_{gs} = C_{gd} = C_{ol} \ , \quad C_{gb} = \left(\frac{x_d}{WL\varepsilon_{Si}} + \frac{1}{WLC_{ox}} \right)^{-1} \ , \quad C_{sb} = C_{jsb} \ , \quad C_{db} = C_{jdb} \ , \tag{96}$$

where:

$$C_{ol} = C_{GS0} \cdot W + C_{GD0} \cdot W \tag{97}$$

$$C_{js(d)b} = \frac{A_{S(D)C_{j0}}}{\left(1 + \frac{V_{S(D),B}}{\psi_0}\right)^{m_j}} + \frac{P_{S(D)C_{jsw0}}}{\left(1 + \frac{V_{S(D),B}}{\psi_0}\right)^{m_{jsw}}} \tag{98}$$

which depends on the MOS layout.

2.6.4 MOS noise in sub-threshold

For what concern the noise contribution, let's write, for comparison, the expression which holds for the super-threshold working region:

$$\overline{i_{nd}^2} = 4k_B T \frac{\gamma}{\alpha} g_m \Delta f + \frac{K_f}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \tag{99}$$

For a MOS in sub-threshold region, one has:

$$\overline{i_{nd}^2} = 2k_B T n g_m \Delta f + \frac{K_f}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \tag{100}$$

2.7 A GENERAL TRANSCEIVER ARCHITECTURE

A basic structure representing a simple radio communication interface is reported in figure 23. This example is very close to what is currently being designed in the radio project topic of this dissertation.

Here, the antenna is connected to the radio via a three port device which assures a proper isolation between the power amplifier (PA) in the transmitter path and the low noise amplifier (LNA) in the receiver path.

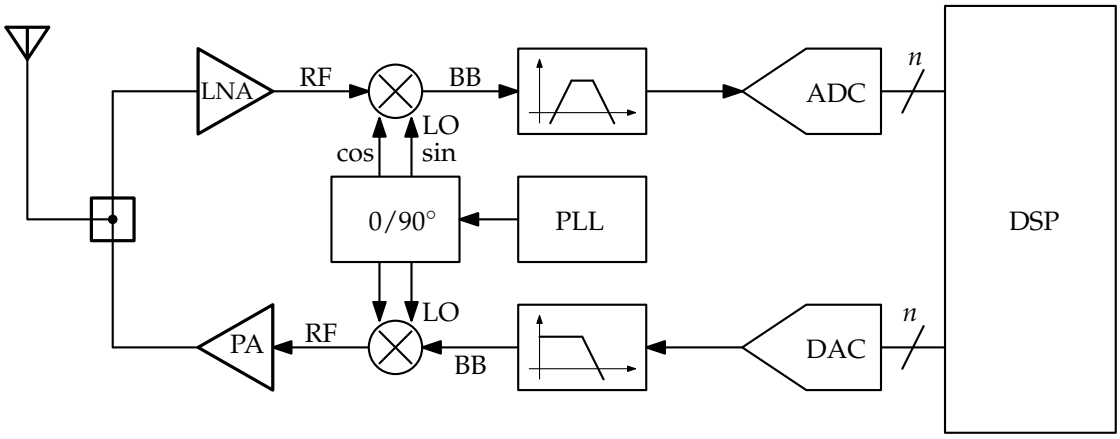


Figure 23: antenna to DPS interface with focus on the receiver and the transmitter paths.

Focusing on the receiver part, the LNA is responsible of the amplification of the signal coming from the antenna adding the less noise as possible. The mixer, which is responsible for translating the rf signal into a lower frequency range, can be very noisy reason of which its noise figure has to be lowered by a high gain low noise device before, as stated by the Friis equation (48). Hence, this amplifier is very important since it reduces the noise figure of the receiver chain a lot. This, in turn, helps in obtaining a high SNR ratio and so a high sensitivity, which is the capability of the system to distinguish the useful signal from the noise level. The mixer is followed by a band bass filter which removes both high and low frequency components; in this way, dc offset caused by even order harmonic distortion and flicker noise of active devices are well attenuated.

Mixers are usually divided in active and passive mixers; the former provide higher gain, low noise but suffer from poor linearity and consume more power. The latter, instead, are way more linear and less power hungry, but at cost of no gain and higher noise. In the case of this radio project, passive mixers are employed, partly because of the lower power consumptions. A passive mixer can be voltage or current driven. The first type is connected by a proper low noise voltage amplifier at the input and loaded by high impedance nodes at the output, usually an active filter. Because of the structure, if the signal voltage amplitude rises, then distortion gets more pronounced. On the other hand, a current driven passive mixer is connected to a low noise transconductance amplifier (LNTA) and loaded by a transimpedance amplifier which converts the current into a voltage for the ADC. Since current signals do not shows rising amplitudes similar to the voltage case, the structure becomes intrinsically more linear. Such considerations

have determined the receiver topology for this project, and lead to the design of a *low noise transconductance amplifier* instead of a low noise (voltage) amplifier.

2.7.1 The role of the LNA in the receiver path

As reported previously, the request of low power consumption wireless device has fixed design constraints which often lead to design challenges, especially in the analogue circuit field. Low power consumption, high gain, low noise figure are the most important requirements a LNA is called to satisfy. Since LNA determines the receiver performance, designing a LNA with consideration of all parameters within specified limits presents a demanding situation for all the researchers. Most of the LNAs are generally built in order to work at a single operating frequency because multiple bands LNA are quite complex even though they can be compatible for multi-standard communication protocols. This is generally paid in terms of increased power consumption and cost though [9].

2.8 LNA TOPOLOGIES

In order to achieve a reasonably low noise figure while maintaining a respectable gain value, the number of active components for a low noise amplifier has to be as small as possible. Hence, single stage architectures are usually adopted in practice. In this section two main LNA single stage configuration are described. Both of them make use of the cascode configuration to assure a proper insulation between input and output and uses a parallel tank as output load. Besides guaranteeing a good stability, the cascode configuration provides a high reverse isolation which is necessary to improve stability and make the LO feedthrough negligible.

2.8.1 Common Gate Low Noise Amplifier

This LNA configuration is reported in figure 24: this topology is one of the most used since its low input impedance make the source matching quite easy. The use of the cascode stage helps keeping the contribution of the channel length modulation of the first device low in the expression of the input impedance. Its in band small signal behaviour can be understood by considering the model depicted in figure 25. The main important aspect to consider for a low noise amplifier are the input impedance, the voltage gain and the noise figure.

Neglecting the channel length modulation effect, hence considering $r_0 \to +\infty$, it is easy to compute the input admittance of a common gate LNA as:

$$Y_{in} \simeq g_m + sC_i = g_m \left(1 + \frac{sC_i}{g_m}\right) \tag{101}$$

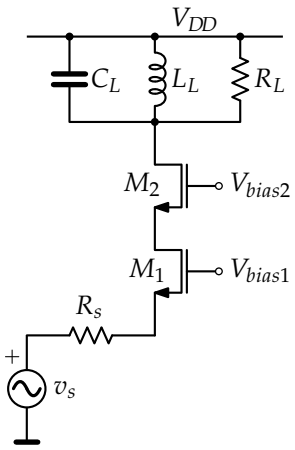


Figure 24: common gate LNA.

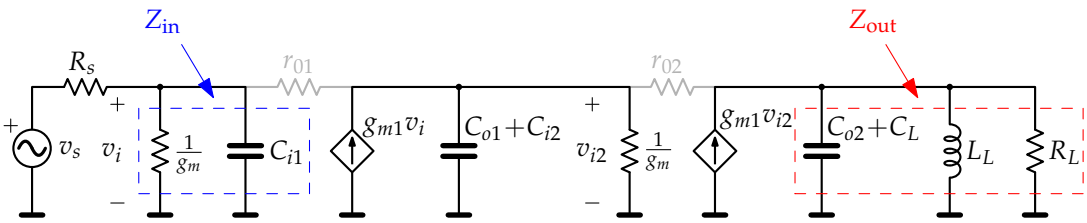


Figure 25: small signal model of the common gate LNA.

If the output inductor size, L_L is such that it resonates the output capacitance at the working angular frequency ω_0, the voltage gain can be computed as:

$$A_v \triangleq \frac{v_o}{v_i} \simeq \frac{g_m R_L}{1 + g_m R_S} \tag{102}$$

having assumed that, in band, the input capacitance as well as the output capacitances of the input common gate stage are negligible. However it is important to notice that this could not be well verified, in particular if g_m is quite consistent: in fact a big g_m usually implies that also the parasitic capacitance, especially C_{gs}, can achieve non negligible values and it must be verified in simulation design stage. Besides, a large g_m is needed for this configuration in order to obtain a proper matching. For instance, in the case of $R_s = 50\Omega$, a value of $g_m = 20\text{mS}$ is required.

Usually, the LNA is the first block to be connected to the input antenna, one may also have to consider the effect of a pad capacitance present at the LNA input mesh. The schematic of such situation is reported in figure 26. In such case, it is very common to put an inductor in such a way that it resonates the total amount of capacitance represented by the C_{pad}, C_{sb_1} and C_{gs_1}. A more realistic analysis should take into account also the effect of the output resistance of the devices, which are r_{01} and r_{02}. In such case the voltage gain computed from the input of the first stage is expressed as:

$$\frac{v_o}{v_i} = \frac{1 + g'_{m_1} r_{01}}{r_{01} + Z_X} \cdot \frac{1 + g'_{m_2} r_{02}}{r_{02} + R_L} \cdot Z_X \cdot R_L \tag{103}$$

where:

$$Z_X = \frac{R_L + r_{02}}{1 + g_{m'_2} r_{02}} \cdot \frac{1}{1 + sC_X \frac{R_L + r_{02}}{1 + g_{m'_2} r_{02}}} = \frac{R_X}{1 + sC_X R_X} \tag{104}$$

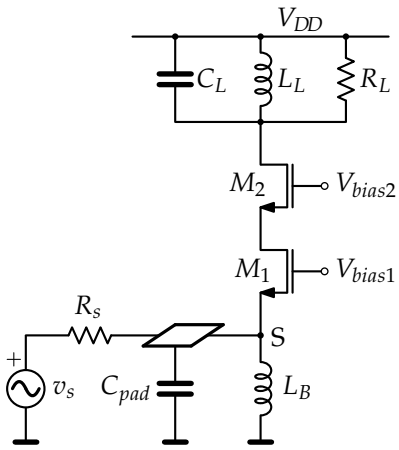


Figure 26: common gate LNA with the pad capacitance connected to the substrate and the degenerated inductor.

In case of small channel length, such expression is much more accurate since one's dealing with output resistances of few kilo-ohm, or even hundreds of ohms. Unfortunately, a more complex expression for the voltage gain can be unmanageable, even though all the important contributions are shown. The approximated noise figure can be computed, at the resonance frequency, as:

$$F = 1 + \left(\frac{\gamma}{\alpha}\right) \cdot \frac{1}{g_m R_S} + \frac{R_S}{R_L} \cdot \left(1 + \frac{1}{g_m R_S}\right)^2 \tag{105}$$

where the contribute of cascoded device is not shown because usually it shows itself at much higher frequencies with respect to the circuit working frequency. However, this is something that has to be verified. Compared to the common source amplifier, which will be described in the following subsection, the common gate LNA provides better input matching without the use of area consuming inductors while showing an higher noise figure.

2.8.2 Common Source Low Noise Amplifier

The schematic of such amplifier configuration, in its cascode version, is reported in figure 27. One of the possible biasing circuit which can be used are reported in figure 28: capacitance C_{BIG} and resistance R_{BIG} are used to realized a low-pass filter in order to insulate the low frequency circuit to the rf one. The small signal equivalent circuit is reported in figure 29, where C_{BIG} and R_{BIG} are not shown since their effect is negligible in the working band. In the case of the common source low noise amplifier, a different approach is used to match the input impedance to the source impedance. A degenerated inductor is connected to the source of the first MOS transistor: in this way, neglecting the gate to drain capacitance, the input impedance of the amplifier can be written as:

$$Z_{in}(j\omega) = j\omega(L_g + L_s) - \frac{j\omega}{C_{gs_1}} + \omega_T L_s \quad , \tag{106}$$

and, as can be seen, the inductor L_s can be used to set the real part of the LNA input impedance equal to the real part of the source impedance. Besides, along with inductor

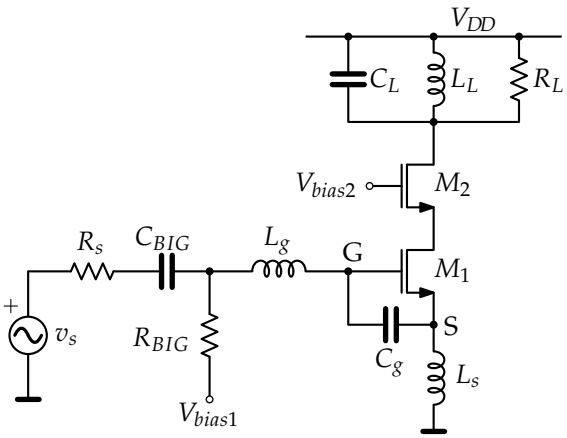


Figure 27: common source inductive degenerated LNA.

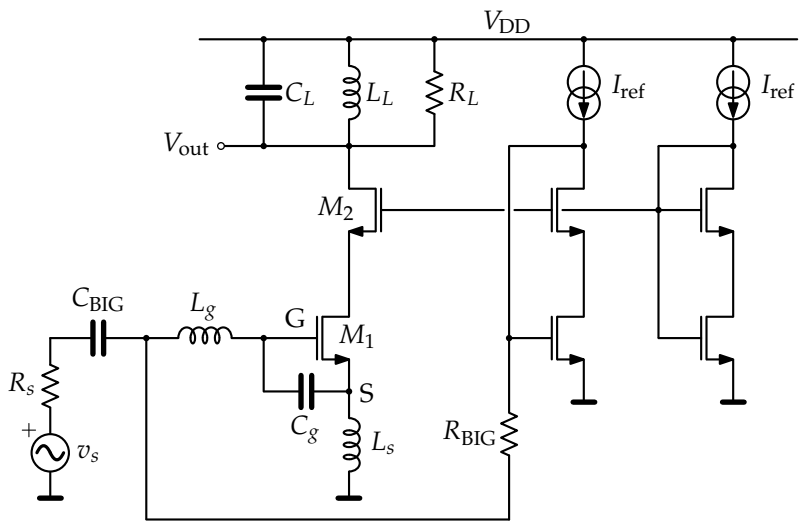


Figure 28: common source inductive degenerated LNA with a proper biasing circuit.

L_g, it resonates also the input capacitance of the stage in such a way that, at the working frequency, only a real impedance is seen looking at the low noise amplifier. The voltage gain of the amplifier can be computed considering the fact that, at the working angular frequency ω_0, it results:

$$v_o \simeq -\frac{g_{m_1}}{j\omega_0 C_{gs_1}} i_g R_L \tag{107}$$

hence the voltage gain from input to output is the following:

$$\left|\frac{v_o}{v_i}\right| \simeq \frac{\omega_T}{\omega_0} \cdot \frac{R_L}{R_S} \tag{108}$$

The third important expression is the noise figure which such structure can achieve. Ignoring the presence of the cascoded device as done for the common gate cascode low noise amplifier, the noise figure can be expressed in the following way:

$$NF = 1 + \left(\frac{\gamma}{\alpha}\right) \cdot \left(\frac{\omega_0}{\omega_T}\right)^2 g_m R_S + \frac{R_n}{R_S} \tag{109}$$

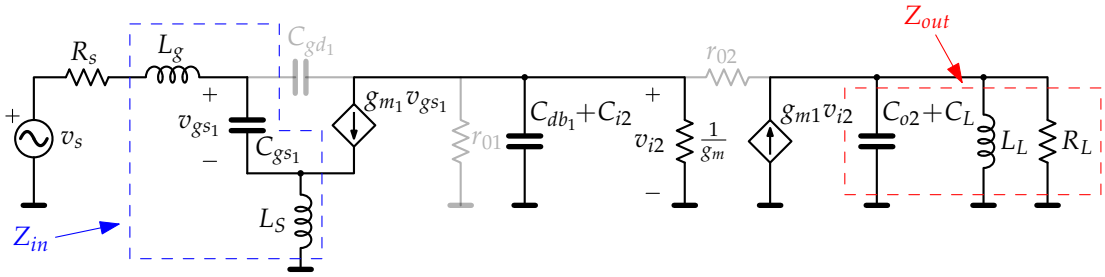


Figure 29: small signal equivalent circuit of the common source cascode LNA with degenerated inductor: the big capacitance and the big resistance are ignored since the circuit is considered to be operating at the rf working frequency.

where R_n takes into account the noise resistances of the input mesh of the amplifier due to the non ideal behaviour of L_g and L_s and to the gate resistance of the MOS. The design procedure usually starts considering the total amount of gain while R_s and R_L are usually constraints of the circuit. The gain is fixed by selecting a proper ω_T of common source device. The higher the gain and fastest should be the technology, which means the smaller the channel length of the active devices. Ones the transition frequency has been chosen, the following quantities can be fixed:

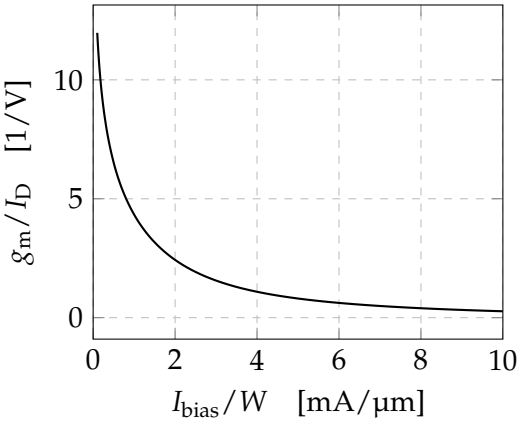
$$L_S = \frac{R_S}{\omega_T} \tag{110}$$

The higher is ω_T and the higher is the MOS transconductance g_{m_1} thus higher is the power consumption since $g_m \propto I_D$. High power consumption usually means low noise figure and higher gain according to (108) and (109). Another problem that may rise when dealing with the choice of the component value is the size of L_g which, especially when the devices are very small to achieve a high ω_T, can be very big. If this is the case, a capacitance in parallel to the gate and the source of the first active device can be place: in the figure such capacitance has been called C_g. However this has a strong impact on the transition frequency of the common source stage and some iterations are usually required in the design in order to obtain the desired performances.

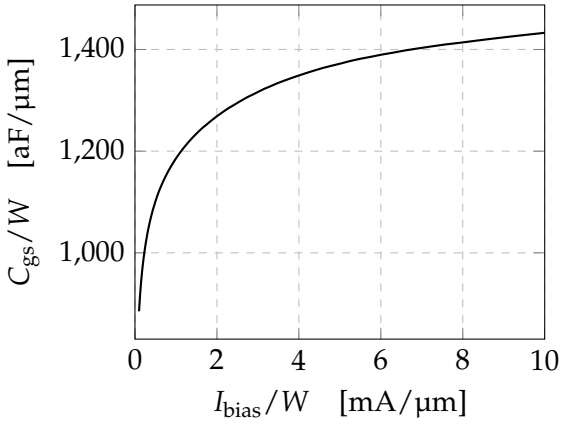
2.8.3 Design procedure example for the common source cascode LNA

Several design procedures can be followed according to what it is important from the designer's perspective. Here the most important parameter that has to be taken into account is the power consumption. The bias current is fixed. An initial value of V^* is chosen, and so $\frac{g_m}{I_D}$ is initially known. From the plot reported in figure 30a one can extract the device size by inverting the function, that is, $W = f^{-1}\left(\frac{g_m}{I_D}\right)$ finding a starting point for the simulator. From figure 30b and 30c it is possible to estimate the value of the initial input capacitance of the common source stage. These kind of plots can be obtained by simulations with the available devices in the technology to be used in the design. Plots obtained in figure 30 are only for demonstrative purpose and not associated to any technology.

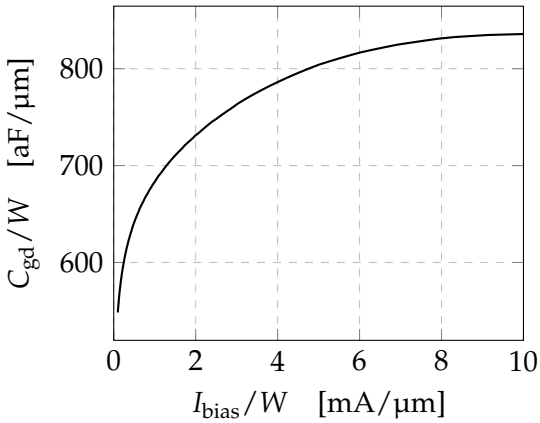
As stated before, if the device is particularly small, as can likely happen for rf applications, an explicit capacitance C_g can be put in parallel in order not to have a big inductor



(a) Transconductance over drain current.



(b) Normalized gate to source capacitance.



(c) Normalized gate to drain capacitance.

Figure 30: three MOS parameters which can be used for the design.

L_g. In this case it is very important to verify the new value for ω_T and hence expected voltage gain and noise figure. For instance one may set a minimum value for the former and correspondingly select a minimum value for ω_T. From that, L_s and L_g can be chosen. The MOS of the common gate stage can be sized like the one of the common source stage since the bias current is the same. The rest of the design is performed by the simulator: noise figure and voltage gain can be plotted as well as S_{11} parameter, verifying if the required performances have been achieved or if some changes are needed.

Other design procedures consider the lowest noise figure and the maximum gain achievement as the prior objectives. The one reported in [29] is based on the following steps:

1. set the drain to source voltage for maximum linearity;
2. find, by simulations, the optimum density current for the amplifier and be sure to keep the same density current throughout the rest of the design;
3. select the optimum finger width in order to obtain the minimum noise figure;
4. size the transistor such that $\Re\{Z_{opt}\} = Z_0$;

5. size the degeneration inductance L_s to set the real part of the input impedance equal to Z_0;
6. add the gate inductance L_g such that to cancel the imaginary parts ot Z_{IN} and Z_{SOPT} become equal to zero;
7. design the output matching network in order to maximize the power delivered to the load over the working bandwidth;
8. design the biasing circuit taking care of not degrading the noise.

The main issue of this procedure is that a quite complete characterization of the technology in use is required. However, the design is straightforward and allows to obtain the lowest noise figure at the expense of a greater current.

2.9 POWER SUPPLY REJECTION RATIO (PSRR)

Integrated circuits are powered by specialized power supplies which in a practical situation may no provide a clean and noiseless constant voltage: some residual ripples may still be present due, for instance, to the switching activities of DC-DC converters. A well designed amplifier should attenuate such residual ripples in order to avoid useless noise to be mixed with the output signal. In order to quantify such ability, the *Power Supply Rejection Ratio*, or *PSRR* for short, accordingly to [11] is defined as:

$$\mathrm{PSSR}^+ = \frac{A_{\mathrm{dm}}}{A^+} \tag{111}$$

$$\mathrm{PSSR}^- = \frac{A_{\mathrm{dm}}}{A^-} \tag{112}$$

having taken into account both the V_{DD} and the V_{SS} supplies. The gain A_{dm} is the differential mode voltage gain of the amplifier under test while A^+ and A^- are referred respectively to the the V_{DD} and the V_{SS} supplies voltage gain.

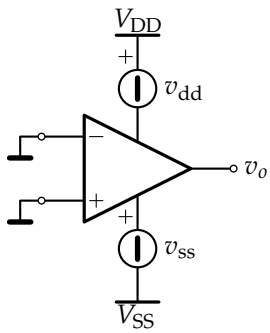


Figure 31: power supplies small signal noise.

In the case of a fully differential amplifier, the noise transferred from the supply lines should be, theoretically, zero since it is a common mode signal which is transferred to two identical branches: the output, being differential, rejects the common mode signals which are identically amplified (or attenuated) by the positive and the negative branches.

3 BLE RECEIVERS STATE OF THE ART

As already discussed in the first chapter, the increasing demand for cheap and low power IoT systems has risen the transceiver research field; ZigBee, Bluetooth Classic/Low Energy and Wi-Fi compatible architectures are the most attractive ones and a lot of publications can be found.

In this chapter, some of the most recent papers about BLE receivers are presented; the aim is to provide a comparison of the achievable performances and the technologies used to the company. This might help in the research and in the design of a new receiver architecture with particular attention to the low noise amplifiers which could meet the target for an industrial product.

It is important to clarify that not all the designs which can be found are practically implementable: a research design is, usually, aimed to prove that certain requirements and targets can be reach under some conditions. For an industrial product, however, targets and specifications might have to be met in various and very different working scenario: this is the case, for example, of the automotive field.

3.1 BLE RECEIVER SPECIFICATIONS

The Bluetooth Low Energy standard imposes some design specifications for what concern the receiver circuit.

A typical receiver design should start with establishing the global RX specification which are independent on the architecture choice; later, once the latter has been chosen, the specs can be distributed along the chain, thus fixing the requirements for the design of each block [22].

An example of initial specs are reported in table (2), based on [21].

3.2 BLE RECEIVERS

In this section, few papers regarding the state of art of the RX receivers for BLE are discussed; for each paper a brief explanation of the receiver working principle, the innovative solutions and the most important results reached are given.

A final comparative table highlighting pros and cons of the different papers ends the chapter.

The emphasis is especially put in the stages that, usually, immediately follows the RF input of the receiver, hence the input matching network, the low noise amplifier and the mixer.

Table 2: example of global specs for a BLE receiver.

Parameter	Specifications
Operating frequency	2.4 – 2.4835 GHz
Channel bandwidth	1 MHz
Channel spacing	2 MHz
Sensitivity with 1MSym/s uncoded data	< -70 dBm
Interference performance	
Co-channel interference, $C/I_{\text{co-channel}}$	21 dB
Adjacent (1MHz) interference, $C/I_{1\text{MHz}}$	15 dB
Adjacent (2MHz) interference, $C/I_{1\text{MHz}}$	-17 dB
Adjacent ($>$ 3MHz) interference, $C/I_{1\text{MHz}}$	-27 dB
Image frequency interference, C/I_{image}	-9 dB
Noise figure	< 30 dB
IIP3	> -31 dB
Image rejection ration	> 21 dB

An interesting site where more in terms of comparisons is [2] where a spreadsheet can be downloaded and analysed.

3.2.1 Thjissen and others, 2021

The title of this paper is *2.4GHz Highly Selective IoT Receiver Front End With Power Optimized LNTA, Frequency Divider and Baseband Analogue FIR Filter*, [28]. As the title suggests, the receiver is optimized in many aspects involving the power consumptions without, however, sacrificing important figures of merit, like the noise figure.

The chain transforms the RF input voltage coming from the antenna into a single ended current by means of a Low Noise Transconductance Amplifier (LNTA); the current is sent to a four-phase passive mixer and re-transformed into voltage by TIAs used as low pass filter. Then the channel selection is made by analogue Finite Impulse Response (FIR) filters.

The LNTA uses an inductive degenerated topology since the latter is able to make both low power consumption and low power possible. Here the authors were interested in obtaining the lowest transconductance but without rising too much the noise figure. For this topology, they have proved that, using ideal inductors, the noise figure is approximately independent on the transconductance, making sense to minimize up to certain estimated value. Of course, dealing with non-ideal inductors, required for the matching, degradation of the noise figure by means of the transconductance factor is unavoidable.

The chip of the receiver is realized in 22nm fully depleted silicon-on-insulator technology (FDSOI). It is powered by a supply voltage of 0.7V and, for the entire chip, a total power of 370µW is required.

The S_{11} parameter is below -10dB for the band between 2.2GHz and 2.9GHz while the overall noise figure in the band of interest is 5.5dB. The sensitivity reached for

the BLE is about −99dBm, the 1dB compression point is 5.0dB while the IIP3 reaches −7.5dBm for 4.01MHz offset at maximum gain of 61dB.

3.2.2 Kuo and others, 2016

This paper is about a complete BLE transceiver, that is, both the receiver and the transmitter are implemented. The original title is *A Bluetooth Low-Energy (BLE) Transceiver with TX/RX Switchable On-Chip Matching Network, 2.75mW High-IF Discrete-Time Receiver, and 3.6mW All-Digital Transmitter* [17].

The receiving and the transmitting paths share a matching network which interface the radio antenna to the chip. The insulation between the two paths is guaranteed by a Transmit/Receive (T/R) switch. Also in this case a low noise transconductance amplifier is adopted followed by a passive mixer and a band-pass filter. Gain controlled is provided by means of linear programmable inverter-based transconductance cells.

In receiver mode, the chip consume 2.75mW of power from a 1V voltage power supply at maximum gain; the low noise amplifier consumes 0.7mW. The RX maximum gain is 46dB showing a noise figure equal to 6.5dB and a IIP3 value equal to −19dB. Also the sensitivity is pretty good, reaching −95dBm. The scattering parameter S_{11} is well below −10dB both in the RX and in the TX in the band of interest for the BLE. The whole chip is realized in 28nm CMOS technology.

3.2.3 Tamura and others, 2020

Titled *A 0.5-V BLE Transceiver With a 1.9-mW RX Achieving -96.4-dBm Sensitivity and -27-dBm Tolerance for Intermodulation From Interferers at 6- and 12-MHz Offsets* [27], the article is about a BLE transceiver operating with a supply voltage of 0.5V.

The LNTA used in the receiver has the peculiarity of being able to change its topology according to the gain settings; this was needed to maintain a high linearity in different gain configurations and with different signal strengths. In high gain mode, it operates as a common-gate cascode amplifier; in the low gain mode, the topology changes into a common source amplifier. Finally, in the middle gain mode a hybrid common gate - common source topology is used. Fine gain is also provided by means of resistor arrays and an attenuator.

The chip is manufactured in 22nm FD-SOI process (WAS?); the measurements shows an average sensitivity equal to −96.4dBm at 1Mb/s. In the middle gain mode the IIP3 level reached is −3.5dBm and it improves as gain is reduced. The scattering parameter changes according to the gain settings and, in general, it is lower than −9.5dB.

For what concerns the power consumption, in RX mode, the transceiver is able to consume 1.0mW of power from 0.5V voltage supply.

3.2.4 Shirazi and others, 2021

The article's title is *An Ultralow-Power Current-Reused Direct-Conversion Bluetooth-Low-Energy Receiver Front-End in 40-nm CMOS* [26].

The paper is about a very low power receiver for BLE where current reuse techniques and subthreshold biased circuits are really employed.

Here the authors discuss the main problems of the latter techniques, which suffer from performance degradation over the Process, supply Voltage and Temperature (PVT) variations and are also dependent on the RX architecture choice. They propose then a low power fully differential direct conversion receiver with an integer N-PLL. The needs for a fully differential operation are found in a IIP2 improvement in order to keep the DC offset contribution low as well as I/Q mismatches issues.

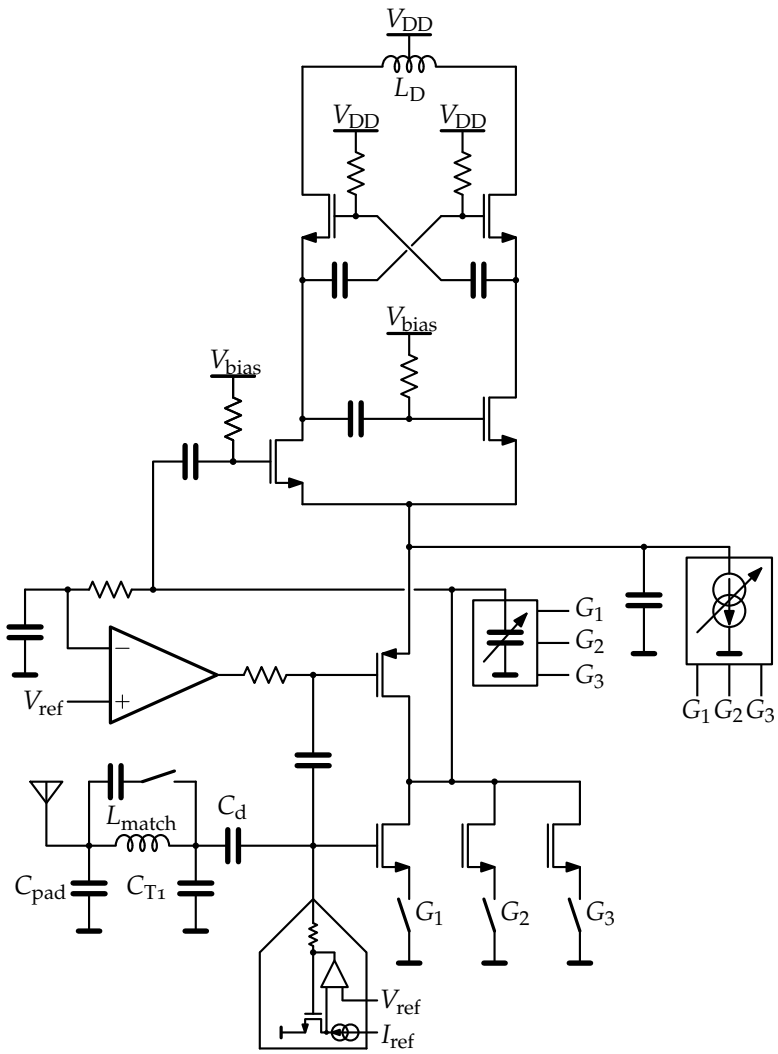


Figure 32: schematic of the proposed combination LNA and Single to Differential converter, as presented in [26].

The front end consists of a low noise amplifier followed by a single ended to differential converter (S2D). The LNA exploits a subthreshold current reuse push pull structure with a input matching network using only one inductor. The use of a push pull amplifier helps in linearity improvement; a dynamically biased feedback loop is used for PVT variations by setting the biasing point of the LNA transistors to a fixed value coming from a band-gap reference.

The single ended to differential conversion is made by two input common source buffers which output is sent to an active balun.

The mixer is a double balanced current driven passive mixer controlled by a 50% duty cycle which, although increasing conversion loss, noise figure and linearity, is able to consume less power.

The baseband filters are made of trans-impedance amplifiers followed by a programmable voltage amplifier.

The receiver is produced using the 40nm LP CMOS technology; the couple LNA plus S2D combines a 30dB of gain with a 3.2dB of noise figure while the $S_{11} < -15$dB at 2.4GHz. Consumptions is 400µW with 1V voltage power supply.

The overall receiver shows a sensitivity of −95.1dBm, a total noise figure of 5.2dB, a variable gain from 47dB to 72dB and a IIP3 of −19.7dB at lowest gain configuration while the 1dB compression point is −27.2dBm. The total power of the chip is 980µW from 1V voltage power supply however it doesn't take into account the external programmable clock and ADC, which would rise the total power consumption up to 3.5mW.

3.2.5 Jin and others, 2021

The one proposed in *A 400-µW IoT Low-IF Voltage-Mode Receiver Front-End With Charge-Sharing Complex Filter*, [14], [15], is about a low-intermediate frequency (IF) voltage-mode receiver for IoT applications and meeting, in particular, BLE requirements.

The point towards the authors are focusing is the fact that current-mode receivers demand low on resistance, which means bigger MOS and higher power consumption, an low input impedance of the baseband trans-impedance amplifier. Hence, voltage mode receiver might help in lowering power consumption. Furthermore, a low-IF receiver architecture requires power hungry complex base band filters. In this work, the latter exploit passive mixers charge sharing properties which should help in maintaining the power consumption sufficiently low for this application.

The front end of the receiver sees the use of a LNTA which, along with the mixer, produces parasitic capacitance. Because of charge sharing, a complex baseband impedance is really created. The idea is then to use such impedance to build a complex first order filter acting before the base-band circuits: the solution should relax the linearity specs of the following stages and avoid the flicker noise.

The LNTA uses a cross-couple common gate stage and a transformer to help a relatively low noise figure meanwhile keeping the biasing current at a low level. The LNTA is followed by a 4-phase 25% duty cycle passive mixers which, beside downconversion, implement also complex filtering. The baseband circuit consumes very little power, 50µV because of the wise use of the free and unavoidable parasitic capacitances.

The chip is realized in 28nm CMOS process and performances are good: it shows a total power consumption of 400µW from a 1V voltage power supply. The overall gain of the receiver is about 50dB while the noise figure of the entire chain is 6.8dB. The inband IIP3 is −14.7dBm and the 1dB compression points reaches −16dBm. The total power consumption is 400µW from a 1V voltage power supply.

3.2.6 Kargaran and others, 2019

This paper is titled *A Sub-0.6V, 330 μW, 0.15 mm² Receiver Front-End for Bluetooth Low Energy (BLE) in 22 nm FD-SOI with Zero External Components* [16].

The receiver front end employs a LNTA which converts the RF voltage into a current sending it to a single-balanced passive mixer and a TIA. The low noise amplifier adopts a common gate stage to match the input antenna and to guarantee a proper gain for the signal. Common gate amplifiers, however, consumes a lot of power to obtain a 50Ω input impedance from the transconductance value; this is why a 1:T step-up transformer is used. In such way, current consumption can be lowered by a factor of T^2. A source boosting technique is further used to lower the transconductance for input impedance matching. To improve even more the performance of the amplifier reusing the same biasing current, a stack configuration is also adopted.

Nothing is reported for the mixer; the baseband TIAs use self-biased inverter based amplifier to provide a good power efficiency and a low noise characteristic.

The RX chip is fabricated with a 22nm Fully Depleted Silicon-On-Insulator (FD-SOI) process and, from experimental measurements, the conversion gain is 32.3dB and the noise figure is 9.4dB. The S_{11} is lower than −10dB in the BLE band of interest; the in-band and out-of-band IIP3 are −30dBm and −8dBm respectively. The total power consumption is really 330μW and the supply voltage used is 0.55V.

3.2.7 Hu and others, 2021

This paper titled *A 0.7-V Sub-mW Type-II Phase-Tracking Bluetooth Low Energy Receiver in 28-nm CMOS* [13], proposes a new BLE receiver architecture that claims to break the 1mW of power.

Here an inductor free inverter based LNTA is used to obtain a gain of 60dB and a noise figure of 6dB for the entire chain. To realized the input matching the wire bounding inductance is used and the cut-off frequency of the transistor is taken to higher value. An off chip inductor to resonate the LNTA input capacitance is also used. An inverter based programmable gain transconductance cell is adopted for the TIAs.

From experimental results, the receiver manages to obtain a sensitivity of −93.2dBm at maximum gain (60dB) and a in-band/out of band IIP3 of −43dBm and −16dBm respectively. The power consumption is very low, 900μW with a voltage power supply of 0.7V, except for the DCO that runs at 0.22Vpower supply; 270μW of power are used by the LNTA and 400μW by the Digital Controlled Oscillator (DCO).

3.3 COMPARISON

Here a summary table is shown; the most important results, common to all the receivers listed in this chapter are collected. Measured IIP3 values are referred to the in-band behaviour of the receiver and, to put all the receivers on the same level, only performances related to the BLE standard are reported.

Table 3: summary of the state of art receivers.

Reference	[28]	[17]	[27]	[26]	[15]	[16]	[13]
Technology (nm)	22	28	22	40	28	22	28
Voltage supply [V]	0.7	1.0	0.5	1.0	1.0	0.55	0.7
Power [μW]	370	700	1000	980	400	330	900
Sensitivity [dBm]	-99	-95	-96.4	-95.1	NA	NA	-93.2
Gain [dB]	61	46	> 41	72	50	32.3	60
NF [dB]	5.5	6.5	NA	5.2	6.8	9.4	6.0
1dBCP [dBm]	5.0	NA	NA	-27.2	-16	NA	NA
IIP3 [dBm]	-7.5	-19	-3.5	-19.7	-14.7	-8.0	-16

From the papers, it is clear that a topology that exploits current driven mixers is usually preferred, making the choice of an LNTA mandatory.

4 FULLY DIFFERENTIAL VARIABLE GAIN LNTA

In this chapter the fully differential structures of the low noise transconductance amplifiers in 40nm and 22nm are presented. The former circuit is taken from an older project and in this thesis it will be the starting point before passing to the 22nm technology. In the following sections the structure and the main working equations are exposed.

4.1 RECEIVER STRUCTURE

The choice of the receiver architecture usually relies on different aspects as already discussed. Hhere a low IF receiver has been chosen instead of a zero IF to avoid the problem of the DC offset and the flicker noise due to the devices. The use of a fully differential architecture, besides attenuating the even order distortion, helps in maintaining a high SNR.

In this architecture the low noise amplifier, as well the transimpedance amplifiers, are equipped with a variable gain. The reason behind it is the necessity of avoiding that power signals which are detected by the receiver, saturates the stages along the chain with the consequence of introducing unwanted frequency lines in the baseband data due to distortion.

Figure 33 shows the receiver structure and highlights all the important blocks used to process the rf signal. The source signal is an antenna featured by an internal source

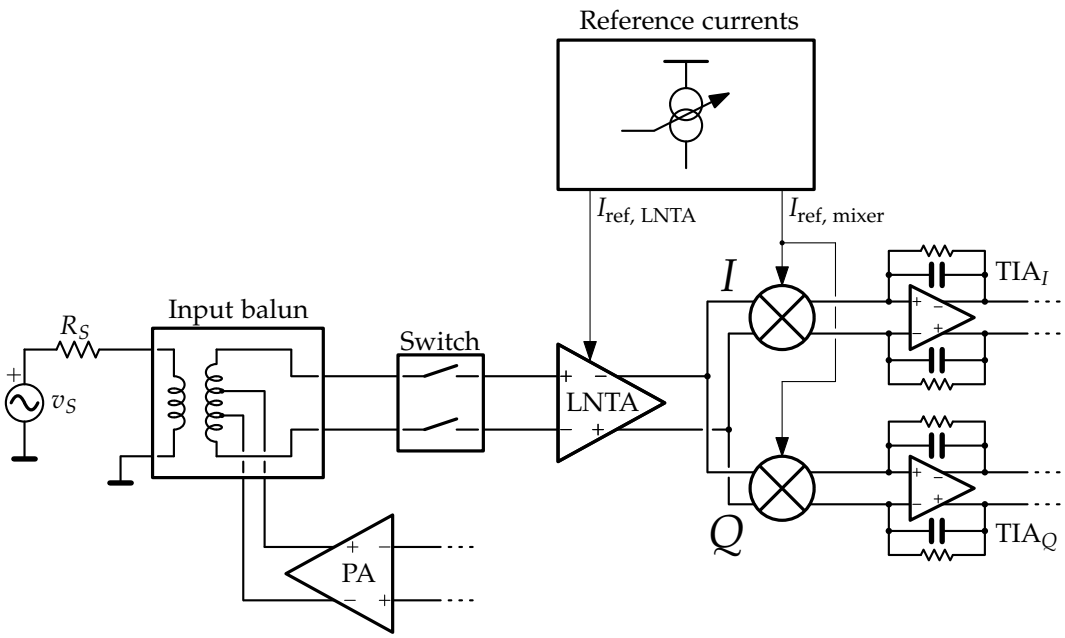


Figure 33: testbench for the simulation of the LNTA performances.

resistance equal to $R_{s,ant} = 50\Omega$ which is then connected to a *balanced-to-unbalanced* transformer, or *balun* for short. This passive device, besides converting the single ended signal coming from the antenna to a fully differential signal, connects both the receiver and the transmitter chain to the source. The communication is, in fact, of half duplex type: it is possible to send and to receive, but not simultaneously. When the transmitter mode is in use, a proper switch provides insulation for the receiver path from the balun to prevent the power amplifier to send the output signal directly to the receiver chain causing saturation of the devices (which needs time to recover from) and, worst, damaging the low noise amplifier itself. Since only the receiving working mode is used for the LNTA design, in the following, an equivalent load capacitance of has been considered in order to take into account the presence of the power amplifier when turned off.

The LNTA is required to drive the I-Q mixers each of them feeding a TIA that implements a band pass filter for the receiver path. A bandpass filter has been adopted to further filter out off DC components due to second order non linearity and flicker noise.

4.1.1 Input balun and switch considerations

The input balun, as said previously, is responsible for single ended to differential transformation for the LNTA in the receiver path and for differential to single ended in the case of the transmitter path. For further aspect on the topic, see [8] and [31]. Such passive device had been design to meet transmitter targets while the receiver chain had to be substantially adapted to what was obtained. This holds both for the 40nm and the 22nm project. The switch is made by two MOSFETs biased in triode region when in on state or in interdiction region when off and is partially responsible for the real part impedance which should match the equivalent source impedance seen from the output of the transformer.

4.1.2 Mixer and TIAs considerations

From the point of view of the output impedance seen by the LNTA, the two mixers, I and Q, basically up-convert the input impedance of the TIAs, centering it at the Local Oscillator (LO) frequency. For further details on this aspect, consider [7] and [20] as well as the mixer chapter of [23]. A double balanced passive mixer structure is very beneficial for the local oscillator feed-through problem; in fact, an unavoidable path made by parasitics capacitance is created from the mixer input up to the low noise amplifier and the antenna (*feed-through effect*). As a consequence, LO signal is sent back to the chain and transmitted by the receiver itself to the environment, causing possible interference for other devices working in the same area. A double balanced mixer topology creates two feed-through paths which cancel each other. Symmetry in the layout is mandatory to make an effective cancellation possible.

The mixers are decoupled from the LNTA outputs by means of decoupling capacitor C_{dec}. Both the Low Noise Transconductance amplifier and the two mixers for the I and Q paths are biased by proper digital controlled re-configurable current mirrors. Biasing and hence power consumption can be changed accordingly to the working conditions.

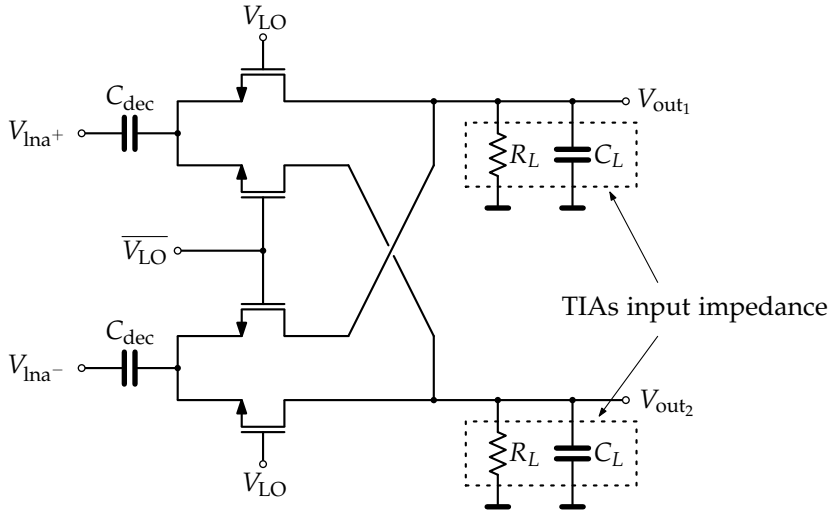


Figure 34: the double balanced passive mixer used for down-conversion of the I and the Q signals.

The TIAs are responsible to filter the signal by implementing band pass filtering stages and are connected to the ADC which then converts the analogue signals into digital and send them to the Digital Signal Processor (DSP) which is not shown in the schematic.

4.2 AMPLIFIER STRUCTURE IN 40NM

The structure of the amplifier is depicted in figure (35). It is a fully differential amplifier

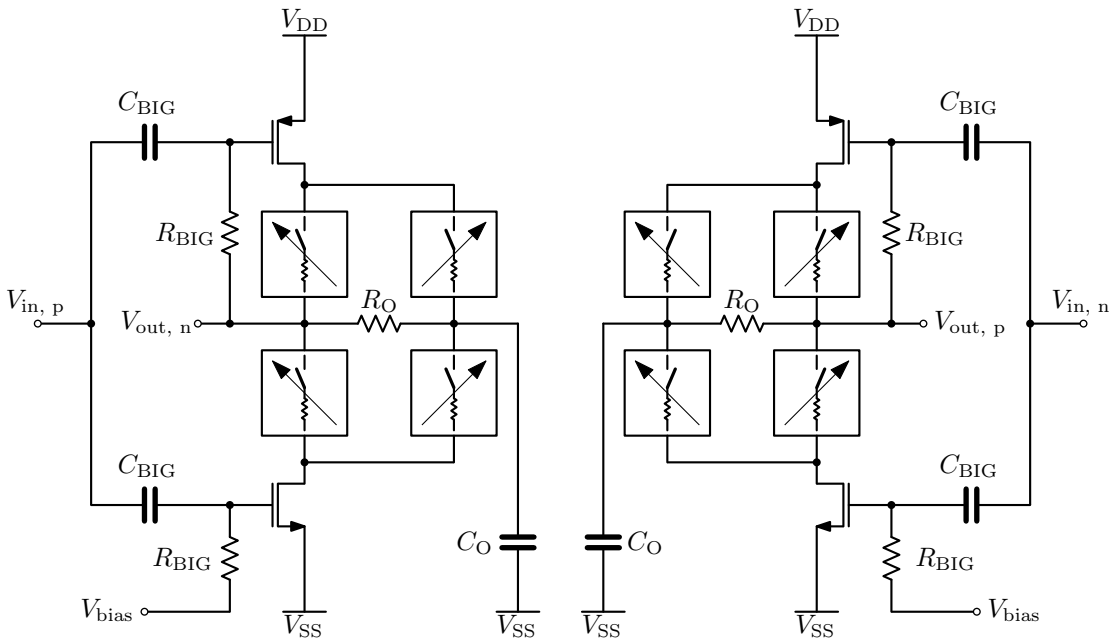


Figure 35: LNTA 40nm topology.

exploiting a complementary cascode structure for each branch. The gain tuning is possi-

ble due to the two different paths the signal can follow once passed the common source stage. This is done not to saturate the receiver chain when the available signal power coming from the antenna is not so weak. A high output resistance is needed because the amplifier has to behave as closed as possible to an ideal current source. The decoupling capacitance C_{BIG} are used to obtained a capacitive divider that, together with the switch and the balun, is used to provide a good match for the amplifier with the source.

4.2.1 Working principle

The working principle can be understood considering the equivalent ac model behaviour. If resistance R_O is quite big and if C_O can be considered as a short at the operating frequency, then, focusing for instance on the left branch, the MOSFETs opposite to the ones connected to the output node see an ac ground at their drain (source). The gate control of the two different blocks of common gates are complementary: if one transistor of a block is turned on and the others are turned off, in the opposite block, the correspondent transistor is off while the others are on and vice versa. In this way, a resistive (or conductance) divider is created and the signal can be all sent through the output, or partially, or nothing at all.

There are different ways to bias the common gate transistors of the LNTA; in this technology, by performing a dc operating point simulation, it has been possible to check the working regions of all the involved transistors. In particular, the common source are well biased in the super-threshold active region while the common base stages, responsible for the amplifier gain control, are biased in the triode region, meaning they all work as switching resistors, as also shown in the figures.

To sum up, the signal is firstly amplified by a common source stage amplifier and then sent to the output by using an adjustable signal path realized by MOSFETs biased in triode region (resistor like behaviour).

Before starting the mathematical analysis, it is very useful to understand how the common source and the following stages interact each others and give further insight on how to treat the amplifier. First of all, the gain control mechanism has to be defined, since it describes how the signal path is changed. The digital bus that sets the LNTA gain has four bits: hence the gain binary word can be written as $G_{\text{ctrl,bin}} = [b_3\ b_2\ b_1\ b_0]_2$; from the schematic available, one sees that the size of the four MOSFETs that realize a block is different. Figure 36 shows the internal structure realized in n-MOS (for the p-MOS is the same). The approximated expression for the equivalent resistance realized

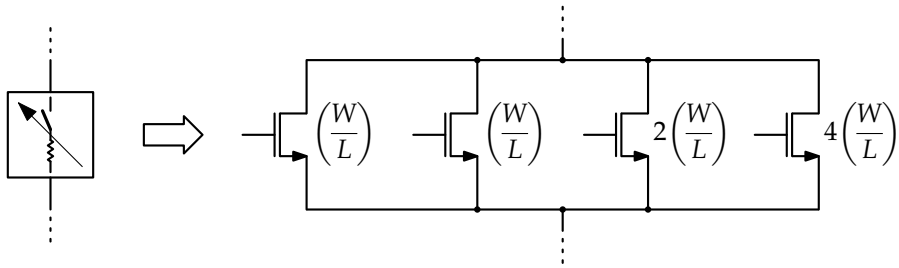


Figure 36: internal realization of one resistive path (to output or to ac ground).

by a MOS biased in triode region is given by equation (113).

$$R_{on} \simeq \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_{th} - V_{in})} = R_e \cdot \frac{1}{\left(\frac{W}{L}\right)} \tag{113}$$

Hence the block can be equivalently represented by figure 37, where an ideal switch is also depicted. Each bit is then associated to a weight. To convert the binary gain

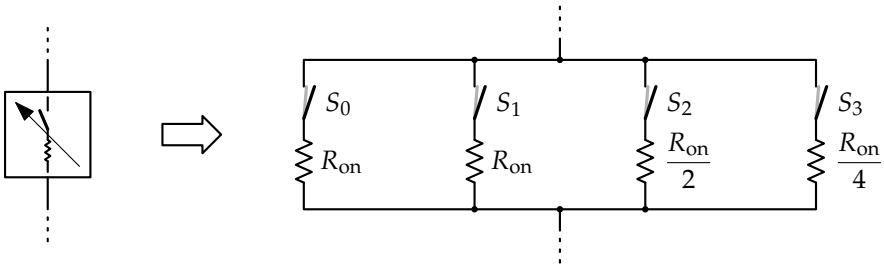


Figure 37: internal realization of one resistive path (to output or to ac ground) by means of equivalent on resistance and ideal switch.

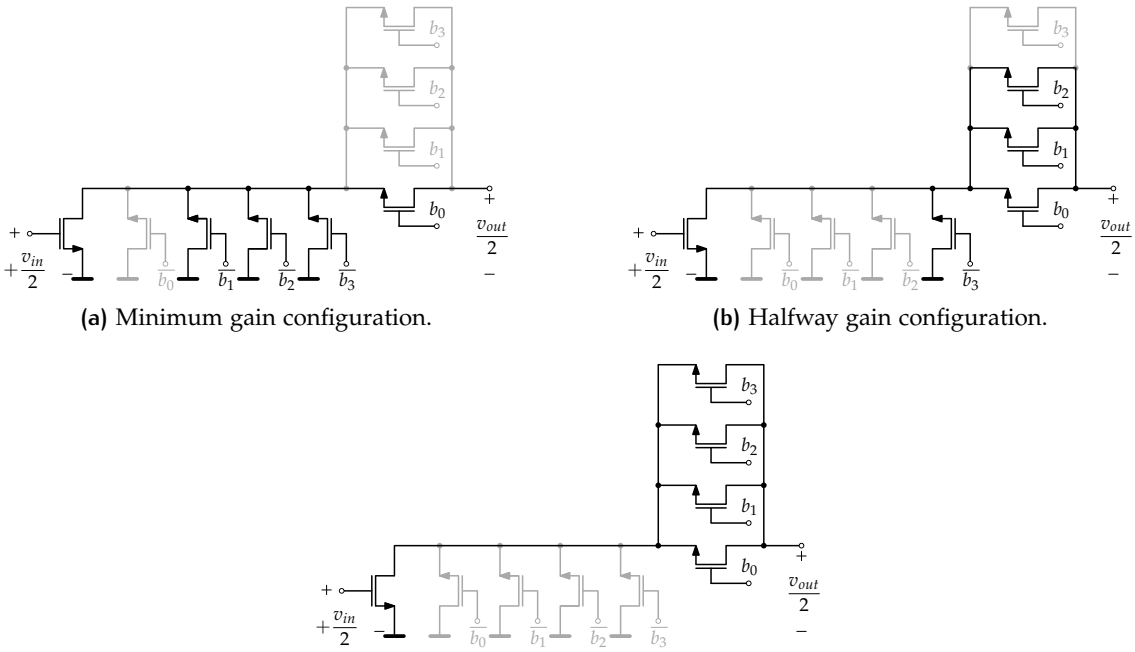
into a decimal number it is sufficient to multiply the former with a weight vector, $W = [w_3\ w_2\ w_1\ w_0] = [4\ 2\ 1\ 1]^T$.

$$\begin{aligned} G_{\text{ctrl, dec}} &= G_{\text{ctrl, bin}} \cdot W^T \\ &= w_3 \cdot b_3 + w_2 \cdot b_2 + w_1 \cdot b_1 + w_0 \cdot b_0 \end{aligned} \tag{114}$$

and it is easy to discover that $G_{\text{ctrl, dec}} \in [0, 8]$. The complementary binary gain word can be written as $\overline{G_{\text{ctrl,bin}}} = \left[\overline{b_3}\ \overline{b_2}\ \overline{b_1}\ \overline{b_0}\right]_2$ and the complementary gain control decimal number is:

$$\begin{aligned} \overline{G_{\text{ctrl, dec}}} &= \overline{G_{\text{ctrl,bin}}} \cdot W^T \\ &= w_3 \cdot \overline{b_3} + w_2 \cdot \overline{b_2} + w_1 \cdot \overline{b_1} + w_0 \cdot \overline{b_0} \\ &= 8 - G_{\text{ctrl, dec}} \end{aligned} \tag{115}$$

and also $\overline{G_{\text{ctrl, dec}}} \in [0, 8]$. Figure 38 shows three different gain scenarios, minimum, halfway and maximum gain, for one of the two n-MOS parts. In order to study the circuit, it is convenient to work in an equivalent single ended version of the amplifier to simplify notation. Focusing on the left branch of the LNTA, from a small signal point of view, the n-MOS part and the complementary p-MOS part are working in parallel sharing the same bias current: hence an equivalent, simpler representation can be the one depicted in figure 39. Here, the auto-biasing resistor R_{BIG} has been omitted to further simplify the analysis; also R_O has been considered as an open circuit while C_O has been considered as a short circuit at rf-working frequency. The transconductances of the common source stages, n and p, are summed while their output resistive paths, supposed equal for both of them, are halved. Since the common gate transistors are treated as switches, models depicted in figure 40 which includes the on/off-resistances and the involved high frequency capacitances can be used. Capacitance C_{on} and C_{off} are expressed differently depending on which transistor path they are associated with, the one that transfers the signal to the output and the one that transfer the signal to



(a) Minimum gain configuration.

(b) Halfway gain configuration.

(c) Maximum gain configuration.

Figure 38: three different MOS transistors configurations for the gain tuning.

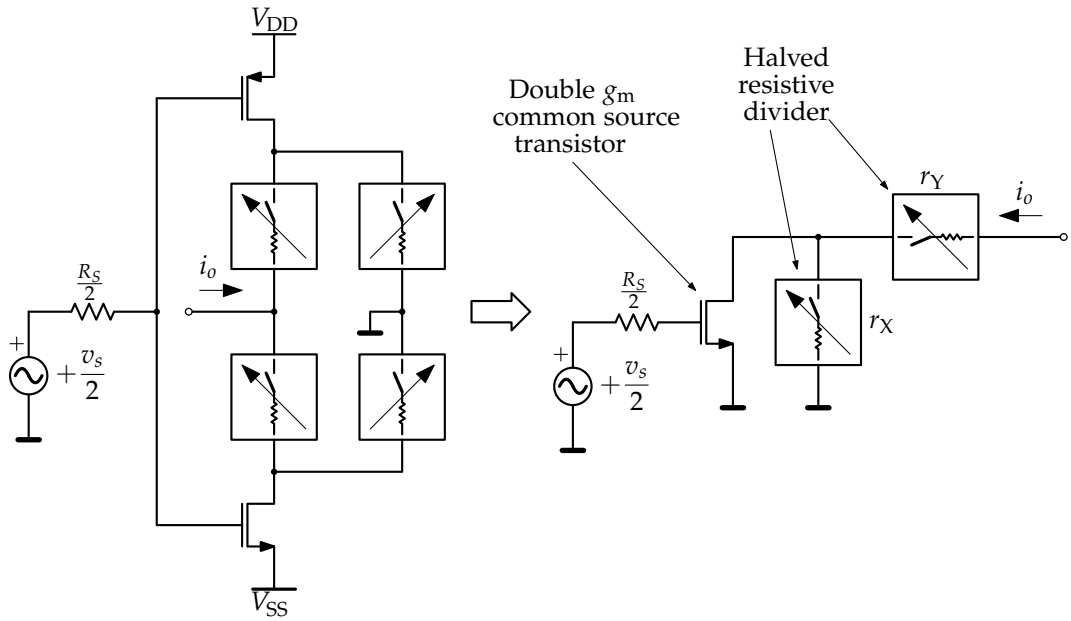


Figure 39: single ended 40nm LNTA convenient transformation.

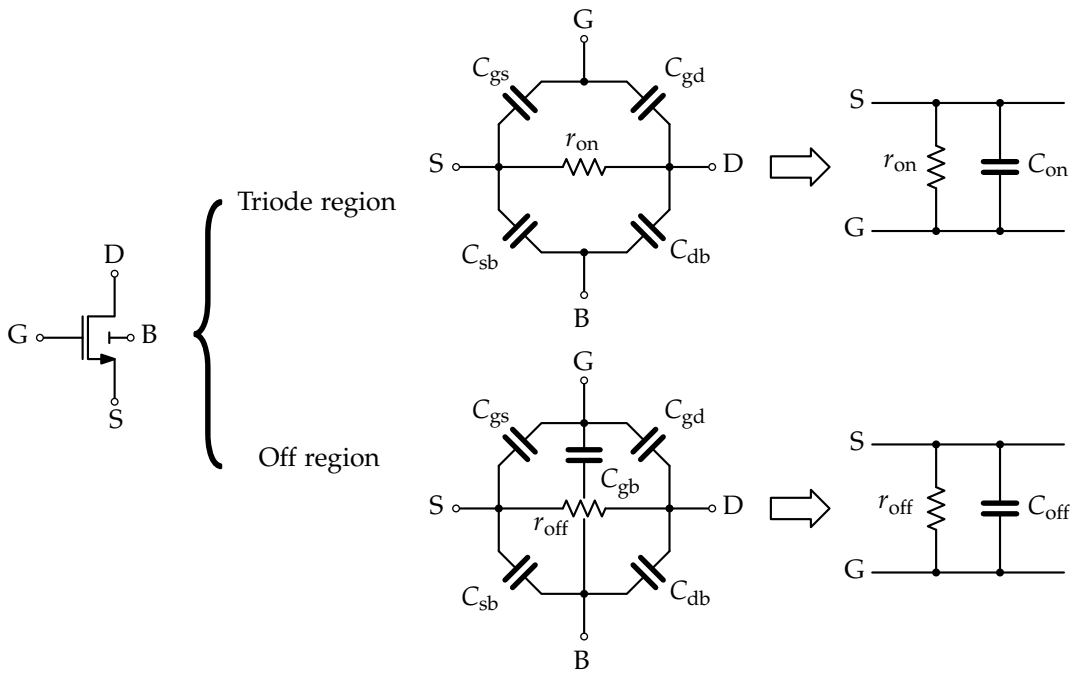


Figure 40: equivalent small signal model for the MOSFET working in triode and off regions.

the ac ground, because their input and output terminals are connected differently. The current divider realized by the structure is describe by equation (116), valid for in-band behaviour, that is, when the decoupling capacitors are considered as short circuits while the parasitic capacitance shows very high impedance.

$$i_{sc} \simeq -(g_{m,n} + g_{m,p}) \cdot \frac{r_X}{r_X + r_Y} \cdot v_{gs} \simeq -\cancel{2} g_m \cdot \frac{r_X}{r_X + r_Y} \cdot \frac{v_{id}}{\cancel{2}} \tag{116}$$

where $g_{m,n} \simeq g_{m,p} = g_m$ if one conveniently sizes the n-MOS and the p-MOS transistors. The overall amount of capacitance and resistance of each path depends on how many transistor are switched on and their size. The bigger the transistor, the bigger the capacitance and the smaller the on-resistance. When the MOS is turned off a small capacitance and a relatively high resistance are present, hence their presence and their affection to the circuit have to be taken into account as well. For the branch that send the signal to the ac ground, one can relate the resistance to the gain configuration by means of the following expressions:

$$r_{on_X} = \left(\frac{\overline{G_{ctrl}}}{r_{on}} \right)^{-1} = \frac{r_{on}}{\overline{G_{ctrl}}} \tag{117}$$

$$r_{off_X} = \left(\frac{G_{ctrl}}{r_{on}} \right)^{-1} = \frac{r_{off}}{G_{ctrl}} \tag{118}$$

as well as the total capacitance:

$$C_{on_X} = \overline{G_{ctrl}} \cdot C_{on} \tag{119}$$

$$C_{off_X} = G_{ctrl} \cdot C_{off} \tag{120}$$

while for the branch that send the signal to the output one has:

$$r_{\text{on_Y}} = \left(\frac{G_{\text{ctrl}}}{r_{\text{on}}}\right)^{-1} = \frac{r_{\text{on}}}{G_{\text{ctrl}}} \tag{121}$$

$$r_{\text{off_Y}} = \left(\frac{\overline{G_{\text{ctrl}}}}{r_{\text{off}}}\right)^{-1} = \frac{r_{\text{off}}}{\overline{G_{\text{ctrl}}}} \tag{122}$$

for the total resistance, while for the total capacitance one obtains:

$$C_{\text{on_Y}} = G_{\text{ctrl, dec}} \cdot C_{\text{on}} \tag{123}$$

$$C_{\text{off_Y}} = \overline{G_{\text{ctrl, dec}}} \cdot C'_{\text{off}} \tag{124}$$

Neglecting the channel length modulation of the common source stage ($r_{0_\text{cs}} \to \infty$), the equivalent resistances r_X and r_Y are given by:

$$r_X = r_{\text{on_X}} \parallel r_{\text{off_X}} \simeq r_{\text{on_X}}\,, \quad \overline{G_{\text{ctrl, dec}}} > 0 \tag{125}$$

$$r_Y = r_{\text{on_Y}} \parallel r_{\text{off_Y}} \simeq r_{\text{on_Y}}\,, \quad G_{\text{ctrl, dec}} > 0 \tag{126}$$

having assumed $r_{\text{off_X}} \gg r_{\text{on_X}}$ and $r_{\text{off_Y}} \gg r_{\text{on_Y}}$; equation (116) can then be rewritten as:

$$\begin{aligned} i_o &\simeq -g_m \cdot v_{\text{in}} \cdot \frac{r_{\text{on_X}}}{r_{\text{on_X}} + r_{\text{on_Y}}} \\ &= -g_m \cdot v_{\text{in}} \cdot \frac{\frac{r_{\text{on}}}{8-G_{\text{ctrl, dec}}}}{\frac{r_{\text{on}}}{8-G_{\text{ctrl, dec}}} + \frac{r_{\text{on}}}{G_{\text{ctrl, dec}}}} \\ &= -g_m \cdot v_{\text{in}} \cdot \frac{G_{\text{ctrl, dec}}}{8} \\ &= i_d \cdot \frac{G_{\text{ctrl, dec}}}{8} \end{aligned} \tag{127}$$

which is the effective output current as function of the gain, expressed in decimal number.

4.2.2 Analytical computations

In this section, expressions for the LNTA input and output impedance, transconductance gain and noise figure are derived, in order to build the model of figure 41. For the analytical computation, the single ended schematic depicted in figure 42 is considered; the models that describe the current paths are reported in figure 113 and are referred to a single branch. Capacitance C_Y can be estimated as:

$$C_Y \simeq C''_{\text{on}} \cdot G_{\text{ctrl, dec}} \tag{128}$$

under the hypothesis of having $C''_{\text{on}} \gg C''_{\text{off}}$. The value of C_{on} can be estimated once the technology parameters are known through equations summarized in table 4. The output load impedance, Z_{load} can be described as a parallel $R-C$ load:

$$Z_{\text{load}} = \frac{R_{\text{load}}}{1 + sR_{\text{load}}C_{\text{load}}} \tag{129}$$

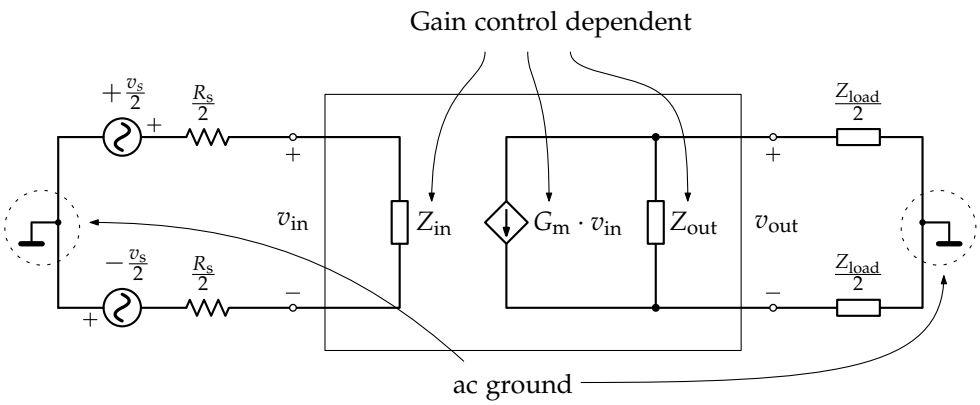


Figure 41: LNTA equivalent model.

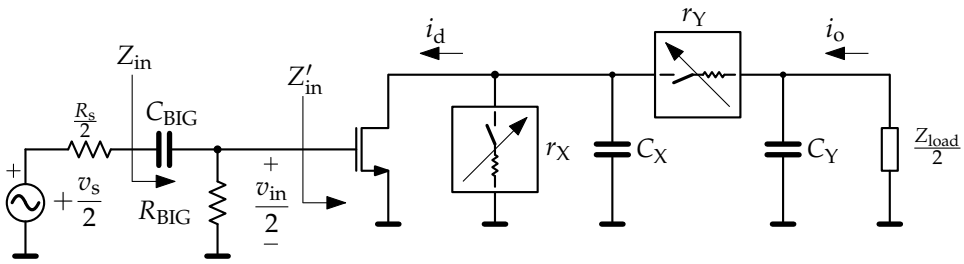


Figure 42: single ended n-MOS part for input impedance computation. For the sake of clarification, only the single ended version of the amplifier has been considered.

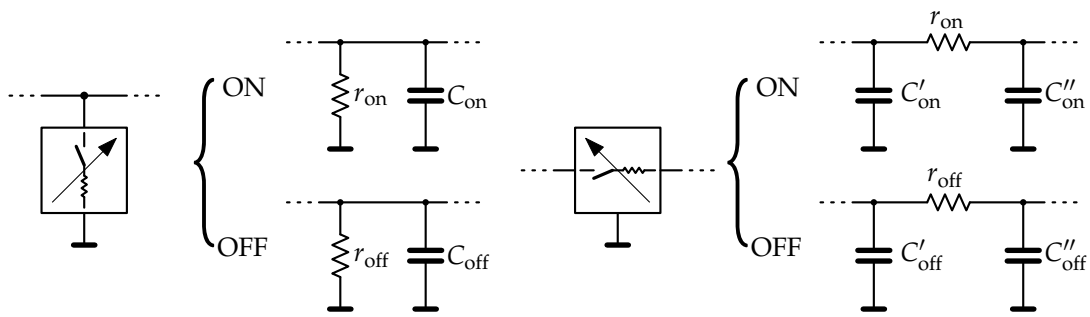


Figure 43: equivalent RC models for the MOS paths.

Table 4: summary MOS capacitance.

Capacitance	Subthreshold	Triode	Saturation
C_{gs}	C_{ov}	$\frac{1}{2}WLC_{ox} + C_{ov}$	$\frac{1}{3}WLC_{ox} + C_{ov}$
C_{gd}	C_{ov}	$\frac{1}{2}WLC_{ox} + C_{ov}$	C_{ov}
C_{gb}	$\left(\frac{x_d}{WL\varepsilon_{Si}} + \frac{1}{WLC_{ox}}\right)^{-1}$	0	0
C_{sb}	C_{jsb}	$C_{jsb} + \frac{1}{2}\frac{WL\varepsilon_{Si}}{x_d}$	$C_{jsb} + \frac{2}{3}\frac{WL\varepsilon_{Si}}{x_d}$
C_{db}	C_{jdb}	$C_{jdb} + \frac{1}{2}\frac{WL\varepsilon_{Si}}{x_d}$	C_{jdb}

4.2.2.1 Input impedance

The input impedance Z'_{in} is computed taking into account the Miller effect due to the C_{gd} capacitance of the common source stage: referring to the n-MOS

$$Z'_{in}(s) \simeq \frac{R_g}{2} + \frac{1}{s\left[2C_{gs_cs} + (1 + g_{m_cs}R_o)2C_{gd_cs}\right]} \simeq \frac{1}{sC_{eq}} \tag{130}$$

where R_o is the total output impedance of the common source stage, which is gain dependent, R_g is the gate resistance and $g_{m_cs} = g_{m,\,n} + g_{m,\,p} \simeq 2g_m$ is the total transconductance of the parallel combination of the active devices. The presence of parasitic capacitance in the Miller effect term has been neglected for simplicity. R_o can be then expressed as:

$$R_o \simeq \frac{r_0}{2} \parallel r_X \parallel \left(r_Y + R_{load}\right) = \frac{r_0}{2} \parallel r_{on_X} \parallel \left(r_{on_Y} + R_{load}\right) \tag{131}$$

with r_0 the intrinsic output resistance of a single n-MOS (p-MOS) common source stage, under the hypothesis of having identical electrical characteristics for the complementary devices. If the channel modulation effect is neglected, then one can simplify the expression as follows:

$$\begin{aligned} R_o &\simeq r_{on_X} \parallel \left(r_{on_Y} + R_{load}\right) \\ &= r_{on}\frac{r_{on} + R_{load}G_{ctrl,\,dec}}{8r_{on} + R_{load}} \\ &= r_{on}\frac{1 + \frac{R_{load}}{r_{on}}G_{ctrl,\,dec}}{8 + \frac{R_{load}}{r_{on}}} \end{aligned} \tag{132}$$

Such resistance can't be kept constant throughout all the gain interval hence both the input and the output impedances are clearly function of the gain. Back to the input impedance expression, if C_{BIG} is considered as a short and R_{BIG} an open circuit at the band of interest, then $Z_{in} \simeq Z'_{in}$. If their contribute is not neglected, the following expression can be considered instead:

$$\begin{aligned} Z_{in}(s) &\simeq \frac{1}{sC_{BIG}} + R_{BIG} \parallel Z'_{in}(s) \\ &= \frac{C_{BIG}C_{eq}R_{BIG}R_g s^2 + (C_{eq}R_g + C_{eq}R_{BIG} + C_{BIG}R_{BIG})s + 1}{C_{BIG}s\left[(C_{eq}R_g + C_{eq}R_{BIG})s + 1\right]} \end{aligned} \tag{133}$$

The behaviour described by such formula is reported in figure 44. As can be seen, the amount of capacitance contribute is quite relevant. The imaginary part impedance cancellation is carried out by the input balun. The real part of the input impedance is far from a "classic" 50Ω source impedance. However, because of the transformation of the input balun, a good S_{11} parameter can be obtained.

4.2.2.2 Transconductance gain

To determine the expression of the transconductance gain, one shorts the output of the LNTA in order to derive the short circuit current as function of the input voltage. The

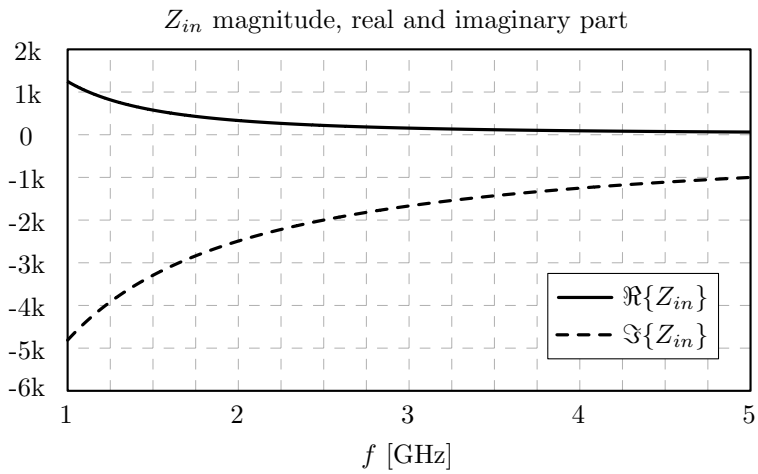


Figure 44: real and imaginary part of the LNTA differential input impedance in 40nm plotted starting from the expression reported in (133).

transconductance that can be obtained is a function of the gain decimal gain world, $G_m(G_{ctrl,\,dec})$ of the circuit in figure 42. Such current has already been found for mid-band working conditions. Taking into account the high frequency capacitance one has:

$$\begin{aligned} i_{sc} &\simeq -g_m \cdot \frac{r_X \parallel \frac{1}{sC_X}}{r_X \parallel \frac{1}{sC_X} + r_Y} \cdot \frac{\left(1 - s\frac{C_{gd}}{g_m}\right)}{1 + sC_{gd}\left(r_X \parallel r_Y \parallel \frac{1}{sC_X}\right)} \cdot v_{in} \\ &= -g_m \cdot \frac{G_{ctrl,\,dec}}{8} \cdot \frac{1 - s\frac{C_{gd}}{g_{m_n}}}{1 + s(C_{gd} + C_X)\frac{r_{on}}{8}} \cdot v_{in} \end{aligned} \tag{134}$$

The transconductance is then given by:

$$G_m = -g_m \cdot \frac{G_{ctrl,\,dec}}{8} \cdot \frac{1 - s\frac{C_{gd}}{g_{m_n}}}{1 + s(C_{gd} + C_X)\frac{r_{on}}{8}} \tag{135}$$

The positive real part zero can be neglected since it is relevant only after the transition frequency of the common source transistor. The dependence of the transconductance on the gain word is due to resistances r_X, r_Y and capacitance C_X.

4.2.2.3 *Output Impedance*

In order to complete the amplifier model, the output impedance has to be computed for the Norton equivalent circuit. Computations are performed exploiting figure 45.

$$\begin{aligned} Z_{out} &= (r_X + r_Y) \cdot \frac{1 + s\,(r_X \parallel r_Y)\,C_X}{1 + s\,[r_X(C_X + C_Y) + r_Y C_X] + s^2 r_X r_Y C_X C_Y} \\ &= \frac{8\,r_{on}}{(8 - G_{ctrl,\,dec})G_{ctrl,\,dec}} \cdot \frac{1 + s\frac{r_{on}}{8}C_X}{1 + s\left[\frac{8C_X + C_Y G_{ctrl,\,dec}}{(8 - G_{ctrl,\,dec})G_{ctrl,\,dec}}\right] r_{on} + s^2 \frac{r_{on}^2 C_X C_Y}{(8 - G_{ctrl,\,dec})G_{ctrl,\,dec}}} \end{aligned} \tag{136}$$

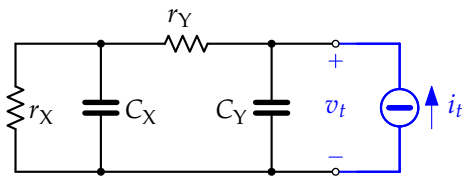


Figure 45: single ended n-MOS part for output impedance computation.

4.2.2.4 *Noise figure*

The noise produced by the low noise transconductance amplifier can be thought as the superposition of a noise voltage source, $\overline{v_n^2}$, and a noise current source, $\overline{i_n^2}$. The

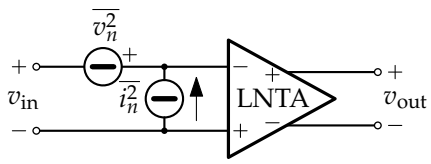


Figure 46: input referred noise sources of the Low Noise Transconductance Amplifier.

noise sources are input-referred, as shown in figure 46 and it is assumed $\overline{v_n^2}$ and $\overline{i_n^2}$ are uncorrelated; this allows to express the noise figure as:

$$F = 1 + \frac{\overline{v_n^2} + \overline{i_n^2} R_s^2}{\overline{v_s^2}}$$

Let:

$$\overline{v_{n,X}^2} = 4k_B T\, r_X \tag{137}$$

$$\overline{v_{n,Y}^2} = 4k_B T\, r_Y \tag{138}$$

be the equivalent noise voltage sources generated by r_X and r_Y; the noise source produced by the common source MOS devices are given by:

$$\overline{v_{n,g}^2} = 4k_B T R_g \tag{139}$$

$$\overline{i_{d,n}^2} = 4k_B T \left(\frac{\gamma}{\alpha}\right) g_m \tag{140}$$

while the source noise is given by:

$$\overline{v_s^2} = 4k_B T R_s \tag{141}$$

The noise voltage v_n is given by different noise sources hence it can be written as:

$$v_n = v_n\big|_{v_g} + v_n\big|_{i_{d,n}} + v_n\big|_{v_X} + v_n\big|_{v_Y} \tag{142}$$

The first two transfer functions are due to the first stage, the common source one, while the others are due to the output current steering stage; the noise sources of the latter are put in evidence by figure 47. Each transfer function reported by equation (142) can be computed by considering the second schematic of figure 48 where both the input

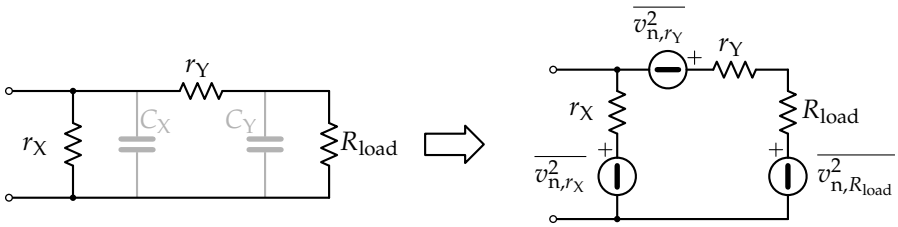


Figure 47: current steering and LNTA load noise sources.

and the output are shorted and by disabling all the generators except for the one the transfer function refers to (current source are opened, voltage source shorted, controlled generators are let operative). In such a way it can be found:

$$\overline{v^2_n} = \overline{v^2_g} + \overline{i^2_{d,n}}\left(\frac{\omega}{\omega_T}\right)^2 R^2_g + \left(\overline{v^2_{n,\,X}} + \overline{v^2_{n,\,Y}}\right)\left(\frac{R_g}{r_X}\right)^2\left(\frac{\omega}{\omega_T}\right)^2 \tag{143}$$

In the same way the noise current source can be expressed as:

$$i_n = i_n\big|_{v_g} + i_n\big|_{i_{d,n}} + i_n\big|_{v_X} + i_n\big|_{v_Y} \tag{144}$$

Considering the third and last schematic of figure 48, where both the input and the output are open circuit, and by doing similar computations as for $\overline{v^2_n}$, it can be found:

$$\overline{i^2_n} = +\overline{i^2_{d,n}}\left(\frac{\omega}{\omega_T}\right)^2 + \left(\overline{v^2_{n,\,X}} + \overline{v^2_{n,\,Y}}\right)\frac{1}{r^2_X}\left(\frac{\omega}{\omega_T}\right)^2 \tag{145}$$

Notice that the contribution of capacitance G_{gd} has been neglected for simplicity. The noise figure expression is hence given by:

$$F = 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s\left[1 + \left(\frac{R_g}{R_s}\right)^2\right] + \left(\frac{\omega}{\omega_T}\right)^2 \frac{1}{r_X}\left(1 + \frac{r_Y}{r_X}\right) R_s\left[1 + \left(\frac{R_g}{R_s}\right)^2\right] \tag{146}$$

where the role of the common source stage and the output load stage for the gain control are put in evidence. Now, in practice, the use of multifingers layout makes for sure $R_g \ll R_s$, thus equation (146) may be rewritten as:

$$F \simeq 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s + \left(\frac{\omega}{\omega_T}\right)^2 \frac{1}{r_X}\left(1 + \frac{r_Y}{r_X}\right) R_s \tag{147}$$

Since both r_X and r_Y are function of the gain, $G_{ctrl,\,dec}$, the noise figure may eventually be expressed as function of the latter as well.

$$F = 1 + \underbrace{\frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s}_{\text{Constant term}} + \underbrace{8\left(\frac{\omega}{\omega_T}\right)^2 \frac{R_s}{r_{on}} \cdot \frac{8 - G_{ctrl,\,dec}}{G_{ctrl,\,dec}}}_{\text{Variable term}} \tag{148}$$

which is a decreasing function of the gain. The characteristic noise figure of a common source amplifier is well recognisable, being the constant part of the whole expression (except the term "1").

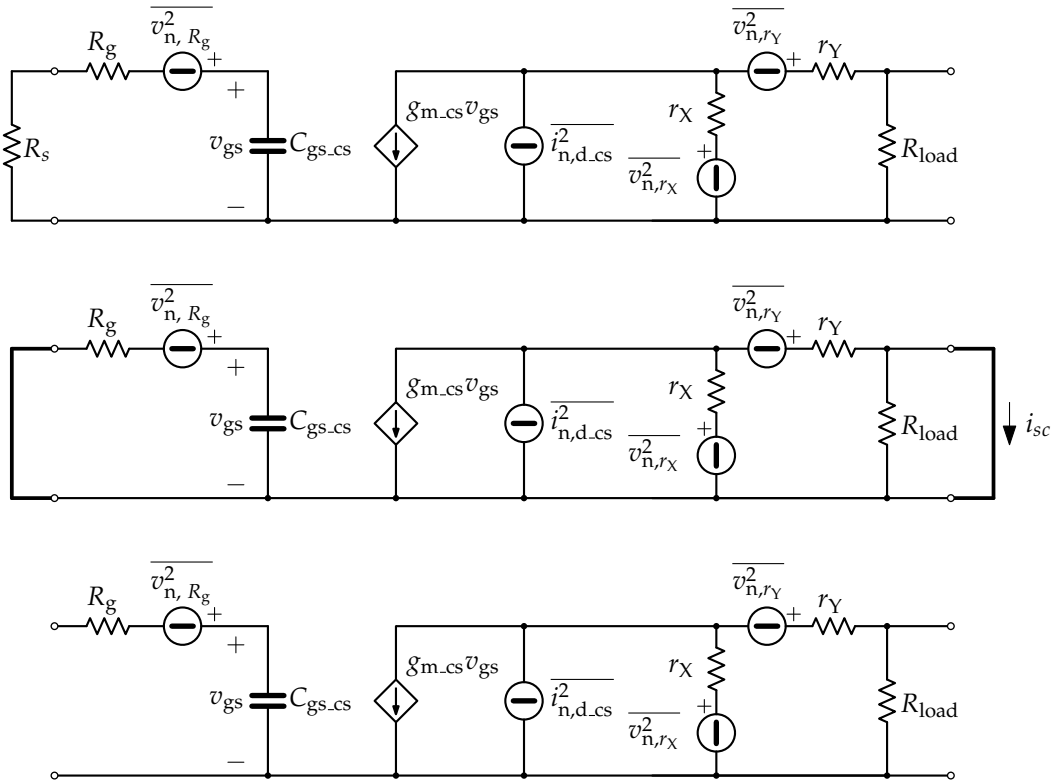


Figure 48: small signal common source equivalent circuit for noise figure computation.

4.2.3 Biasing circuitry

The biasing circuit of the 40nm version of the LNTA is reported in figure 49. The ref-

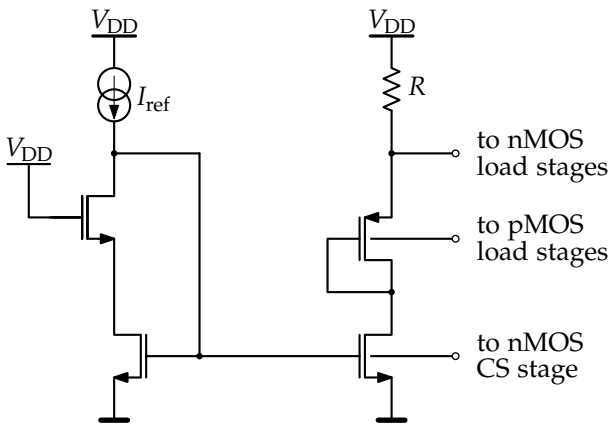


Figure 49: the main biasing circuit of the LNTA in 40nm.

erence current is mirrored to the right branch to generate the voltages for biasing the common source n-MOS stage, the n-MOS and the p-MOS devices of the resistor divider while the common source p-MOS stage is auto-biased by a resistor which senses the output dc common mode voltage. The device involved in the biasing circuit are not matched with the active device which can be a problem in case, for instance, of temperature variation: the devices may not follow the same trend, not resulting in a correct

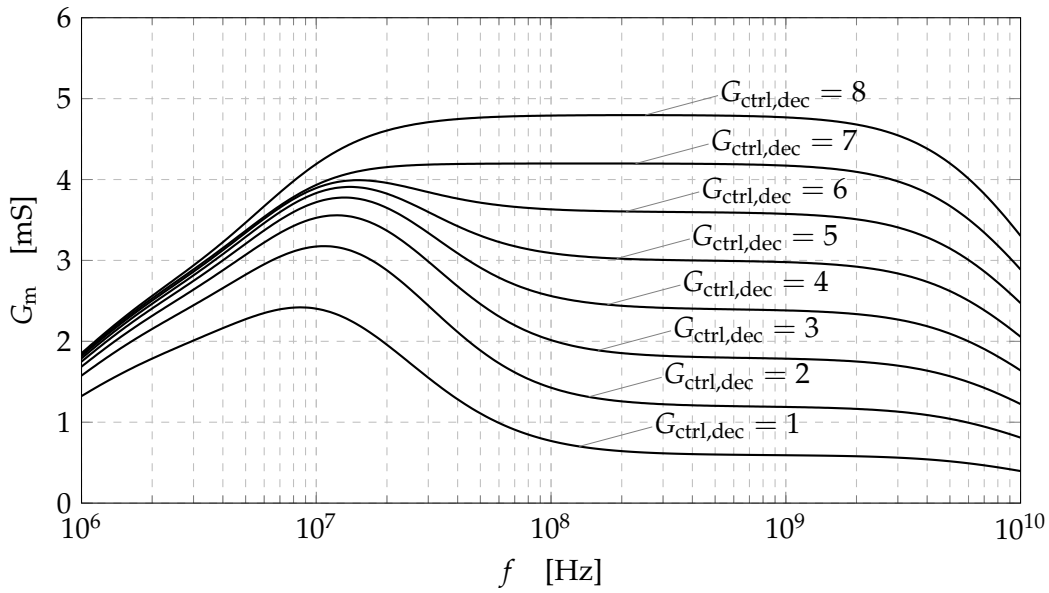


Figure 50: LNTA transconductance in the 40nm technology.

biasing region. The reference voltages created in this way are sent to a digital controlled buffer which, according to the gain settings, turns on and off the correspondent active devices.

4.2.4 Simulation results

The plot of the transconductance gain is reported in figure 50. The output resistance is plot instead in figure 51; the frequency dependence is due to the fact The low frequency behaviour is due mainly to the presence of the big capacitors C_O that connects the high frequency ac ground to the second branch of the current steering. At BLE frequency, the behaviour is well described by the equations. The reference current used for the simulations was fixed to 28µA. Figure 52 and table 5 summarizes all the performances obtained in the 40nm version of the LNTA at T = 27°C and for an input signal frequency tone of 2.45GHz, inside the BLE working band. The results are referred to the entire block chain, from the input balun to the LNTA output. This is due to the fact that the input balun has been designed taking into account the load effect of the power amplifier of the transmitter path and the input impedance of both the switch and the LNTA, which means it cannot be separated otherwise a proper match with the rest of the receiver chain would be lost. Table 6 shows the same results for an higher temperature of 55°C. As can be seen from the plot, the scattering parameter as well as the input impedance, varies along the gain because of the dependence on the load seen by the common source stage. A different choice of the operating region of the MOS that controls the signal path may mitigate the problem. Furthermore, the output impedance is not sufficiently high, and the in chain transconductance is influenced and lowered because of it.

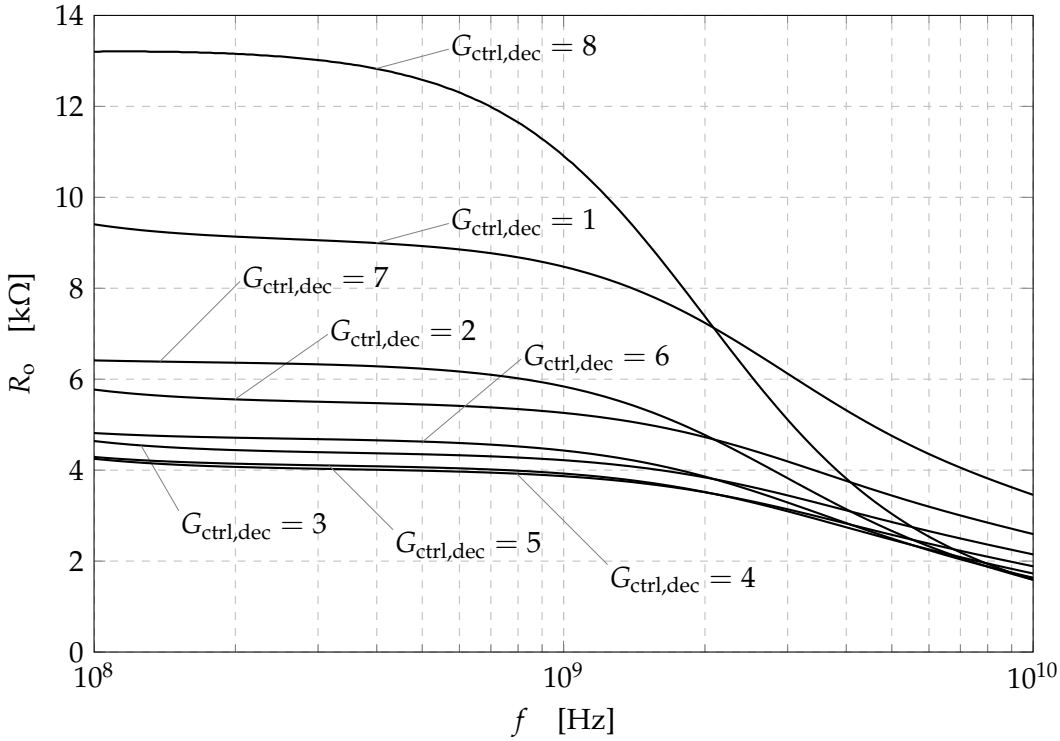


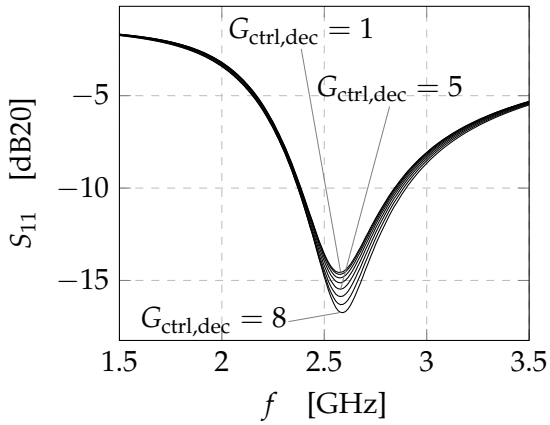
Figure 51: LNTA output resistance in the 40nm technology.

Table 5: main results for the new LNTA design at $T = 27°C$.

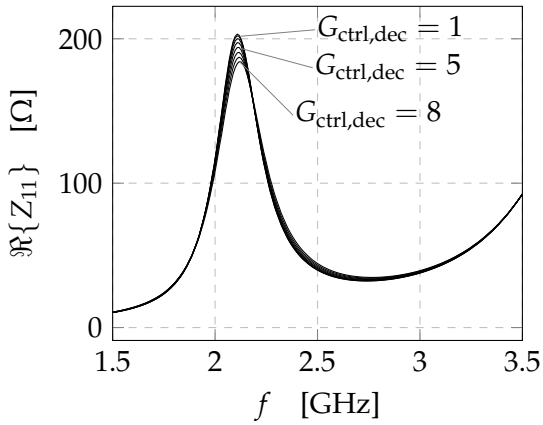
$G_{ctrl,\,dec}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF[dB10]	NF_{min}[dB10]
1	752	828	0,26	−11,8	15,7	15,4
2	752	828	0,51	−11,8	12,6	12,3
3	752	828	0,74	−11,9	10,8	10,6
4	752	828	0,94	−12,1	9,6	9,4
5	752	828	1,14	−12,2	8,7	8,5
6	752	828	1,34	−12,4	7,9	7,7
7	752	828	1,52	−12,5	7,3	7,1
8	752	828	1,69	−12,5	6,7	6,6

Table 6: main results for the new LNTA design at $T = 55°C$.

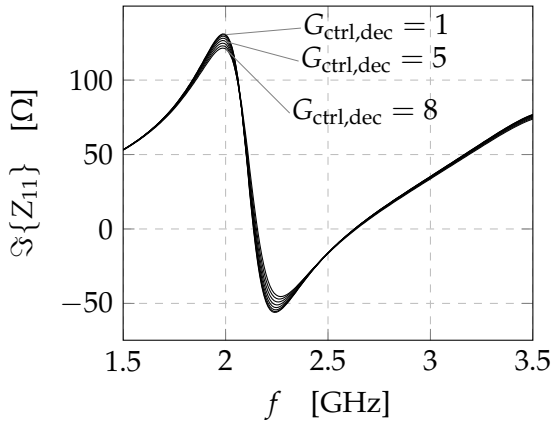
$G_{ctrl,\,dec}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF[dB10]	NF_{min}[dB10]
1	760	836	0,25	−11,8	16,3	16,0
2	760	836	0,48	−11,9	13,2	12,9
3	760	836	0,70	−11,9	11,4	11,2
4	760	836	0,89	−12,1	10,1	10,0
5	760	836	1,08	−12,2	9,2	9,0
6	760	836	1,26	−12,4	8,4	8,2
7	760	836	1,43	−12,5	7,8	7,6
8	760	836	1,59	−12,5	7,2	7,0



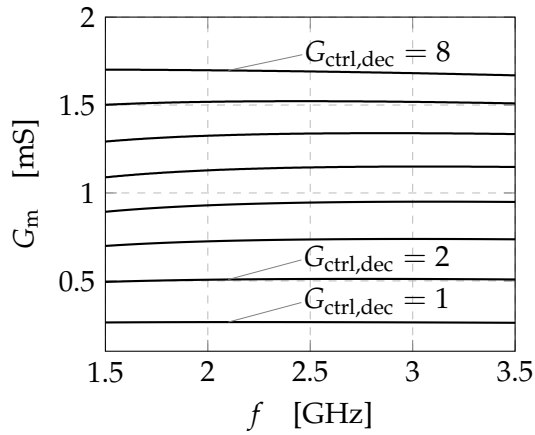
(a) Scattering parameter S_{11}



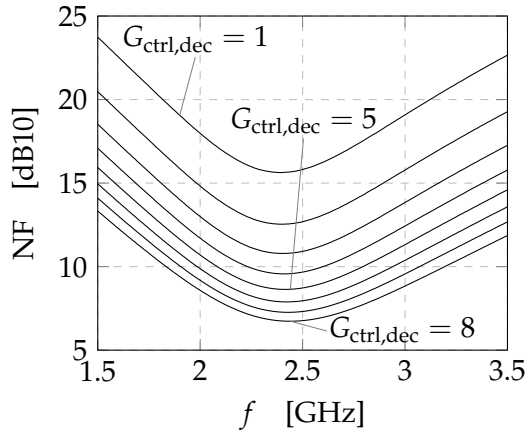
(b) Real part of the input impedance.



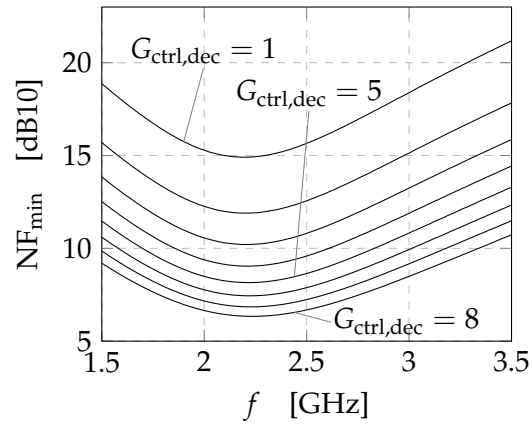
(c) Imaginary part of the input impedance.



(d) In chain transconductance of the LNTA.



(e) Noise figure



(f) Minimum noise figure

Figure 52: the most important results obtained for the starting point low noise transconductance amplifier.

4.3 AMPLIFIER STRUCTURE IN 22NM

The amplifier was ported into the 22nm technology with different changes: the schematic is shown in figure 53. The main variation with respect to before is a different operating

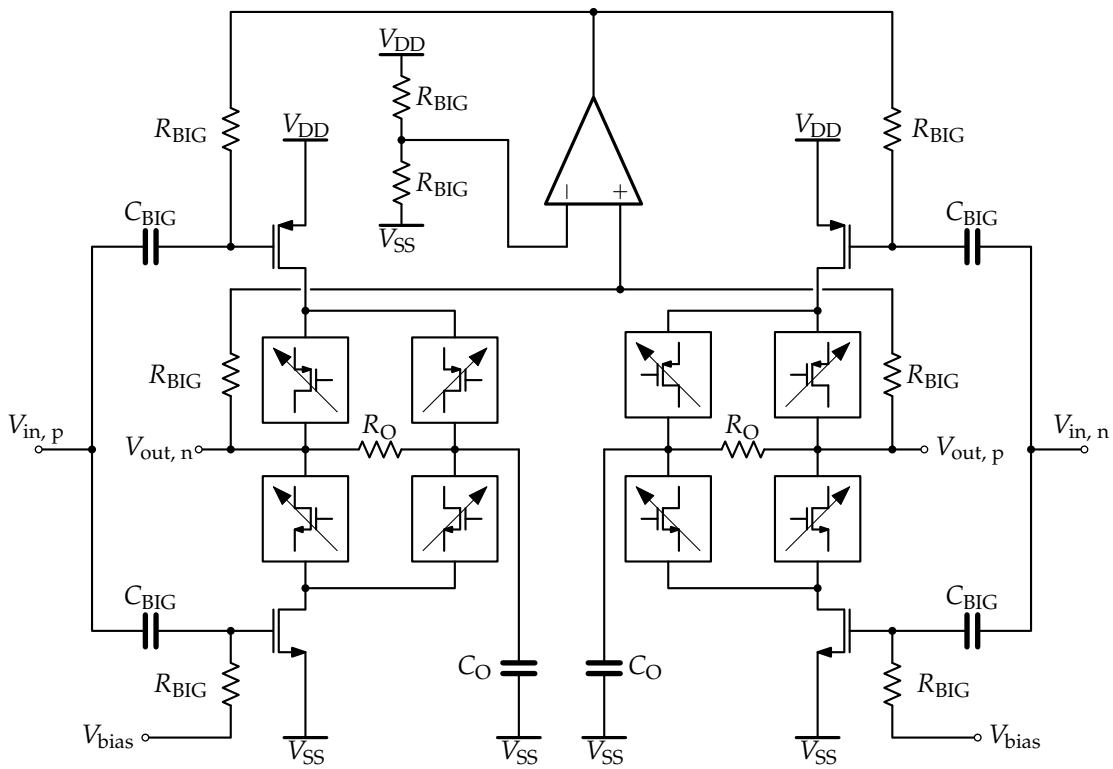


Figure 53: the Low Noise Transconductance Amplifier after the porting to the 22nm technology.

region of the devices. Due to the difficulty of maintaining them into strong inversion, it has been decided to bias all of them in the subthreshold working region. A different approach for the biasing circuit has been adopted: such approach makes use of a CMFB amplifier for auto biasing the pMOS common stages in such a way the common DC operating point at the output of the LNTA is maintained at half of the supply voltage. This should guarantee maximum room for the output voltage variation, avoiding that the active devices exit their operating region. The required performances for the receiver chain up to the LNTA output have to meet the targets reported in table 7.

Table 7: initial specifications for the LNTA in the 22nm BT radio project.

Parameter[1]	Minimum	Nominal	Maximum
G_m	5mS	-	-
S_{11}	-	-	−10dB
NF	-	-	5dB
I_{DC}	-	-	1mA

1 In chain at maximum gain at $T = 27°C$ and $T = 55°C$. The specs apply to the $2.4 - 2.48$GHz band.

4.3.1 Working principle

The new version of the LNTA in 22nm works really quite the same as the 40nm version: now, an equivalent current divider is realized by modifying the total driving signal sent to a current buffer, realized by a MOS common gate stage. The great advantage of the

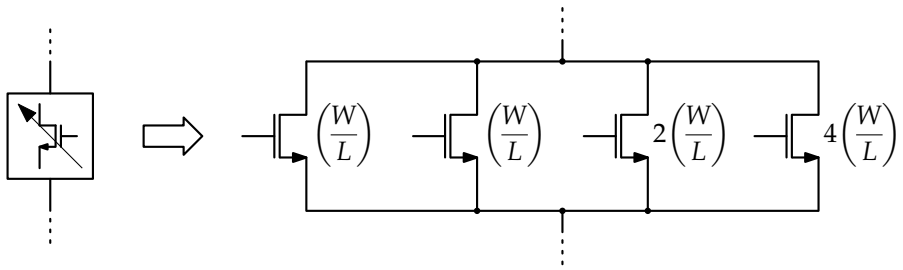


Figure 54: internal realization of one resistive path (to output or to ac ground).

new approach is that the output load seen by the common source stage can be kept almost constant along the gain configuration. The really same blocks are adopted for the 22nm structure, hence one may consider to adopt the same notation as done for the 40nm version. The number of MOS devices in active working region of the two

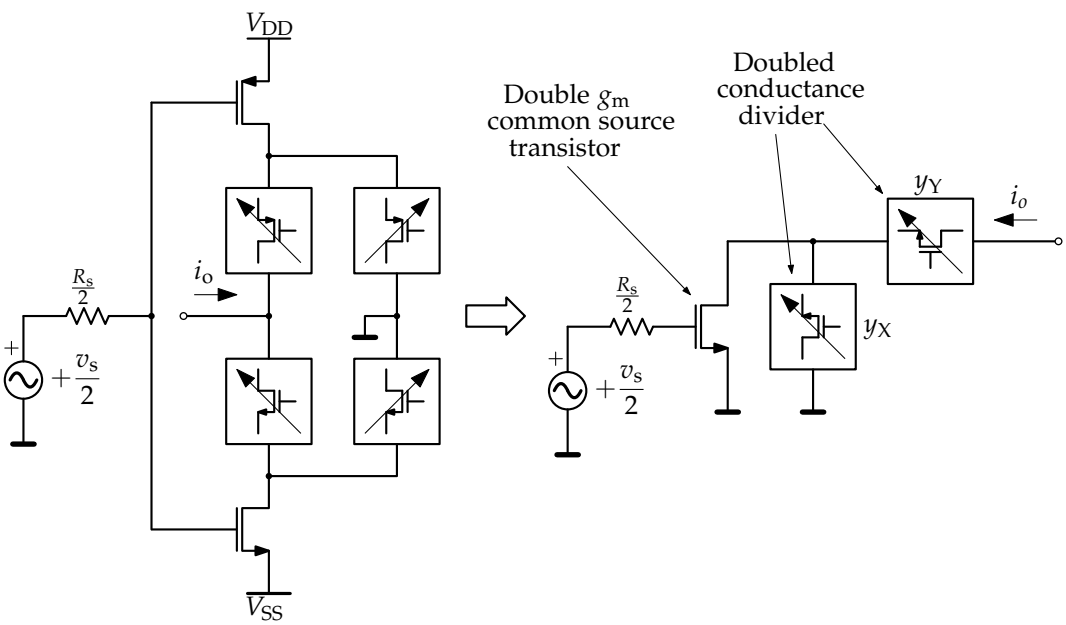


Figure 55: single ended 22nm LNTA convenient transformation.

subcircuits determines the overall transconductance gain as was done in previous 40nm version. The two different branches for the signal path can be modelled respectively by figure 56 and 57. The equivalent admittance y_X is given by both the contribute of the

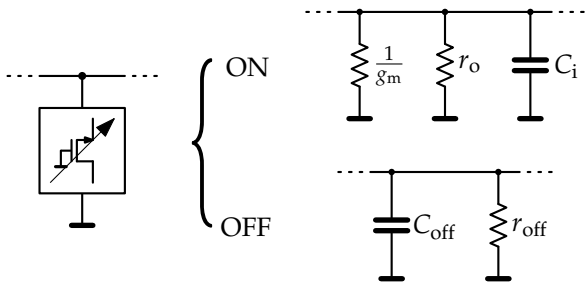


Figure 56: equivalent model of the MOSFETs which steer the signal current to ground.

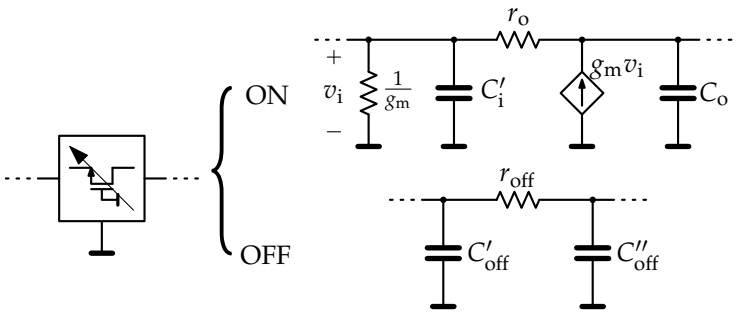


Figure 57: equivalent model of the MOSFETs which steer the signal current to the load.

MOS paths that send the signal to the ac ground and the one that send the signal to the output, hence:

$$y_{on_X} = g_{m_cg}\,\overline{G_{ctrl,dec}} + \frac{\overline{G_{ctrl,dec}}}{r_o} \simeq g_{m_cg} \cdot \overline{G_{ctrl,dec}} \tag{149}$$

$$y_{off_X} = \frac{G_{ctrl,dec}}{r_{off}} + g_{m_cg} G_{ctrl,dec} \simeq g_{m_cg} G_{ctrl,dec} \tag{150}$$

and, considering the parallel of the two, one obtains:

$$y_X = y_{on_X} + y_{off_X} = g_{m_cg}\left(\overline{G_{ctrl}} + G_{ctrl}\right) \simeq 8\, g_{m_cg} \tag{151}$$

which is independent of the gain. The on and off capacitances for the X node can be evaluated as:

$$C_{on_X} = C_i \cdot \overline{G_{ctrl,\,dec}} + C_{off}' \cdot \overline{G_{ctrl,\,dec}} \tag{152}$$

$$C_{off_X} = C_{off} \cdot G_{ctrl,\,dec} + C_i' \cdot G_{ctrl,\,dec} \tag{153}$$

while for the branch that send the signal to the output one has:

$$y_{on_Y} = \frac{\overline{G_{ctrl,\,dec}}}{r_o} \tag{154}$$

$$y_{off_Y} = \frac{\overline{G_{ctrl,\,dec}}}{r_{off}} \tag{155}$$

for the total conductance: hence, if r_o and r_{off} are high enough, then:

$$y_Y \simeq 0 \tag{156}$$

while for the on and off capacitances one obtains:

$$C_{on_Y} = C_o \cdot G_{ctrl,\,dec} \tag{157}$$
$$C_{off_Y} = C''_{off} \cdot \overline{G_{ctrl,\,dec}} \tag{158}$$

Capacitances C_X and C_Y are then given the by the parallel combination of the on and the off ones:

$$C_X = C_{on_X} + C_{off_X} \simeq C_i \cdot \overline{G_{ctrl,\,dec}} + C'_i \cdot G_{ctrl,\,dec} \tag{159}$$
$$C_Y = C_{on_Y} + C_{off_Y} \simeq C''_{off} \cdot \overline{G_{ctrl,\,dec}} \tag{160}$$

where the approximation is valid if one neglects the off contributing caps.

4.3.2 Analytical computations

Analytical computations follow the same order of the LNTA in the 40nm version: different changes have to be considered due to the fact the MOSFETs operate in a different working region and the adjustability of the gain is obtained in a similar but slightly different way.

Consider the equivalent model for the single ended nMOS part, which is depicted in figure 42. The small signal schematic is reported in figure 59.

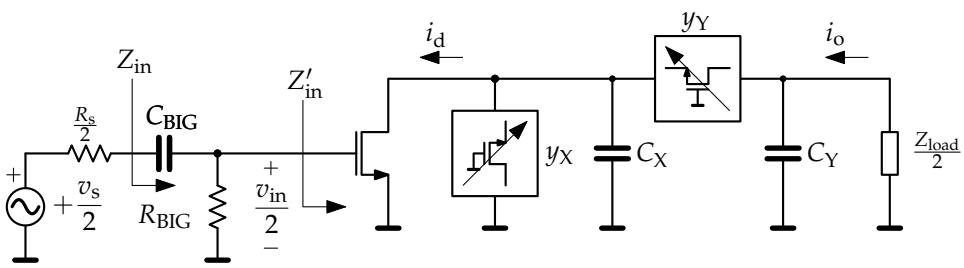


Figure 58: single ended n-MOS part for input impedance computation of the 22nm version.

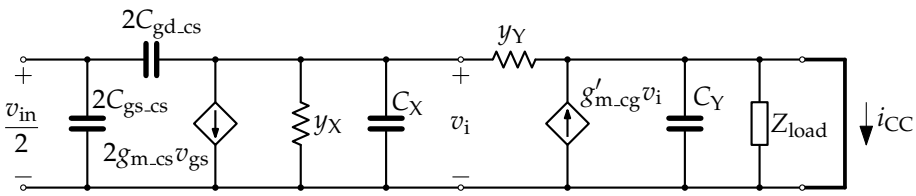


Figure 59: small signal analysis circuit for the single ended nMOS part of the 22nm LNTA.

4.3.2.1 Input impedance

The input impedance now coincides with the input impedance of a cascode amplifier: in particular one has:

$$Z'_{in}(s) \simeq \frac{R_g}{2} + \frac{1}{s\left[2C_{gs_cs} + \left(1 + \frac{g_{m_cs}}{g_{m_cg}}\right)2C_{gd_cs}\right]} \simeq \frac{1}{s2\left(C_{gs_cs} + 2C_{gd_cs}\right)} \tag{161}$$

since the load of the common source stage is approximately given by the inverse of the transconductance of the common gate stages: varying the gain, the load seen from the common source stage can be assumed constant since there is always a $\frac{1}{g_m}$ factor appearing.

4.3.2.2 Transconductance gain

The transconductance expression can be obtained in exactly in the same way it was done for the 40nm version: the only difference is the holding expression of r_X (y_X) and r_Y (y_Y). The short circuit current is:

$$\begin{aligned} i_{sc} &= \left(g'_{m_cg} G_{ctrl,\,dec} + y_Y\right) \cdot v_i \\ &\simeq g'_{m_cg} \cdot G_{ctrl,\,dec} \cdot v_i \end{aligned} \tag{162}$$

the common gate input voltage can be derived as:

$$v_i = \left(i_{gd_cs} - g_{m_cs} v_{gs_cs}\right) \left(y_X + y_Y + \frac{1}{sC_X}\right)^{-1} \tag{163}$$

which, substituted in (162) gives:

$$i_{CC} = \left(g'_{m_cg} + \frac{1}{r_Y}\right) \left(i_{gd} - g_{m_cs} v_{gs_cs}\right) \left(y_X + y_Y + \frac{1}{sC_X}\right)^{-1} \tag{164}$$

The current which is flowing through capacitance C_{gd} is given by:

$$i_{gd_cs} = \left(v_{gs_cs} - v_i\right) sC_{gd_cs} \tag{165}$$

hence the relationship between v_i and v_{in} can be written as:

$$\frac{v_i}{v_{in}} \simeq g_{m_cs} \cdot \frac{1}{8g_{m_cg}} \cdot \frac{\left(1 - s\frac{C_{gd_cs}}{g_{m_cs}}\right)}{1 + s\frac{C_{gd_cs}+C_X}{8g_{m_cg}}} \tag{166}$$

Eventually, the overall transconductance is given by:

$$G_m = g_{m_cs} \frac{G_{ctrl,\,dec}}{8} \cdot \frac{\left(1 - s\frac{C_{gd_cs}}{g_{m_cs}}\right)}{1 + s\frac{C_{gd_cs}+C_X}{8g_{m_cg}}} \tag{167}$$

If one neglects the C_{gd_cs} capacitance, one can obtain the transconductance expression of a cascode amplifier:

$$G_m(s) = g_{m_cs} \cdot \beta_{CG}(s) \simeq \frac{g_{m_cs}}{1 + s\frac{C_X}{g'_{m_eq}}} \tag{168}$$

4.3.2.3 Output impedance

The output impedance of the new version of the amplifier can be computed having in mind the one of a cascode amplifier:

$$Z_{out}(s) = \frac{r_X + r_Y + g_{m_cg} G_{ctrl,\,dec}\, r_X\, r_Y}{1 + sC_Y(r_X + r_Y + g'_{m_cg} G_{ctrl,\,dec}\, r_X\, r_Y)} \tag{169}$$

where r_X, R_Y, g_{m_eq}, C_X and C_Y depends on the selected gain configuration.

4.3.2.4 Noise figure

As previously done, with the help of figure 60 to find $\overline{v_n^2}$ and $\overline{i_n^2}$, one can compute the noise figure for a single branch as:

$$F = 1 + \frac{\overline{v_n^2} + \overline{i_n^2} R_s^2}{\overline{v_s^2}}$$

The noise source produced by the MOS devices are given by:

$$\overline{v_{n,\,g}^2} = 4k_B T R_g \tag{170}$$

$$\overline{i_{d_cs,\,n}^2} = 2k_B T n g_{m_cs} + 2k_B T n g_{m_cg}(8 - G_{ctrl,\,dec}) \tag{171}$$

$$\overline{i_{d_cs,\,n}^2} = 2k_B T n \; g_{m_cg} \; G_{ctrl,\,dec} \tag{172}$$

while the source noise is still given by (141). The input referred noise voltage source, as

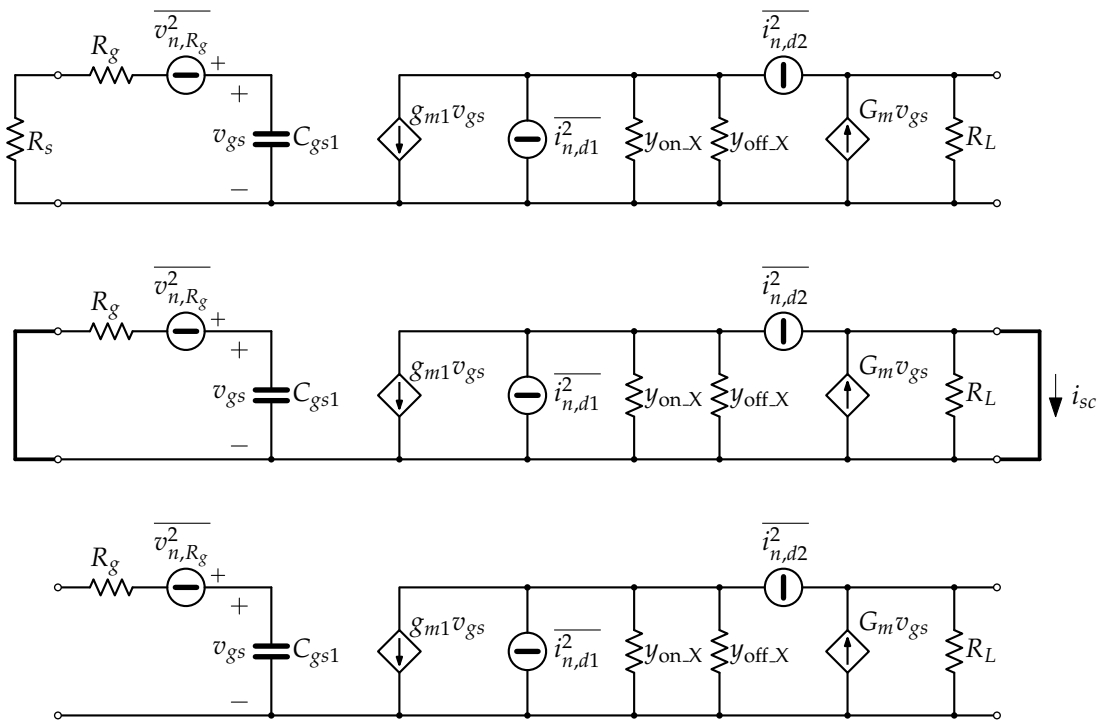


Figure 60: small signal models of the 22nm LNTA for the noise figure computation.

usual, is computed by shorting both the input and the output of the two-port device and finding the output short circuit current i_{sc} due to v_n and to the different noise sources that appear in the second schematic of figure 60.

$$\overline{v_n^2} = \overline{v_g^2} + \left|\frac{1 + j\omega R_g C_{gs_cs}}{g_{m_cs}}\right|^2 \overline{i_{d_cs,\,n}^2} + \left|\frac{1 + j\omega R_g C_{gs_cs}}{g_{m_cs}}\right|^2 \overline{i_{d_cg,\,n}^2} \left(\frac{y_X}{y_Y}\right)^2 \tag{173}$$

while for the noise current source:

$$\overline{i_n^2} = +\left(\frac{\omega}{\omega_T}\right)^2 \overline{i_{d_cs,\,n}^2} + \left(\frac{y_X}{y_Y}\right)^2 \left(\frac{\omega}{\omega_T}\right)^2 \overline{i_{d_cs,\,n}^2} \tag{174}$$

Let:

$$R_{\text{in}}(j\omega) = \frac{1 + j\omega R_g C_{\text{gs_cs}}}{g_{\text{cs}}} \tag{175}$$

The true noise figure is then:

$$\begin{aligned} F = 1 + \frac{R_g}{R_s} & \\ & + \frac{n}{2}\left[\frac{|R_{\text{in}}(j\omega)|^2}{R_s^2} + \left(\frac{\omega}{\omega_T}\right)^2\right]\left[g_{\text{m_cs}} + g_{\text{m_cg}}(8 - G_{\text{ctrl, dec}})\right] R_s \\ & + \frac{n}{2}\left[\frac{|R_{\text{in}}(j\omega)|^2}{R_s^2} + \left(\frac{\omega}{\omega_T}\right)^2\right]\frac{(8 - G_{\text{ctrl, dec}})^2}{G_{\text{ctrl, dec}}} g_{\text{m_cg}} R_s \end{aligned} \tag{176}$$

As can be seen, the effect of the common gate of the cascode device is relevant at low gain configuration. Because of the two paths for controlling the signal at the output of the common source stage, the noise of the latter is influenced by the group

4.3.3 Further considerations on the impedance matching

The impedance matching is quite difficult to obtain with the value of impedance given by the LNTA only. One has also to consider the contribute due to the switch and, most important, the role of the transformer input balun of the receiver chain.

4.3.4 Biasing circuitry

The re-designed biasing circuit of the new 22nm version of the LNTA is reported in figure 61. An additional resistance, R_1, made in poly-silicon, has been placed between the V_{SS} and the source of the right MOSFET. This was done to properly bias all the

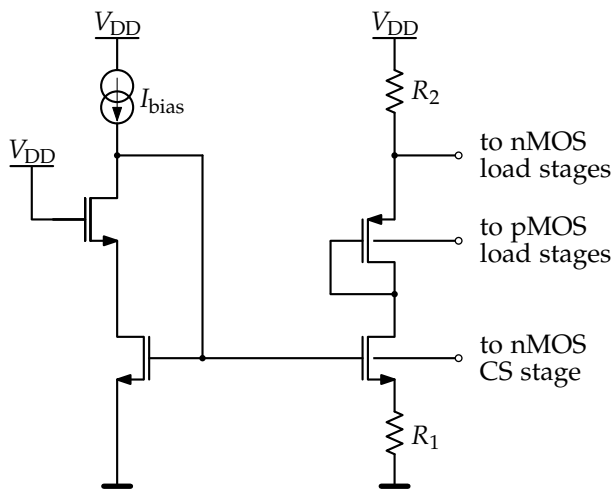


Figure 61: the main biasing circuit of the LNTA in 22nm, redesigned with respect to the previous technology.

MOSFETs of the LNTA in subthreshold region.

4.3.5 The Common Mode Feedback Amplifier

The Common Mode Feedback Amplifier, or CMFB for short, is used to automatically adjust the biasing point of the pMOS transistors used in the low noise transconductance amplifier. The use of feedback should make it more robust against the PVT (Process Voltage Temperature) variations with respect to the self-biasing resistors used in the 40nm version. The voltage gain realized by this structure, at low frequency, is equal to:

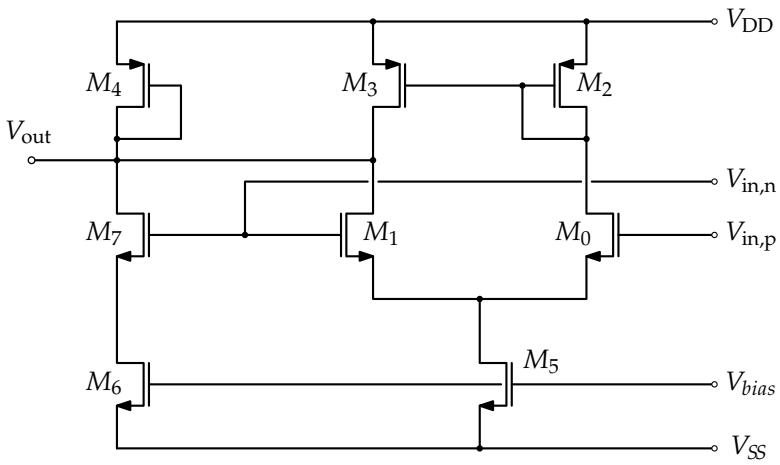


Figure 62: the structure of the CMFB amplifier used to bias the pMOS transistors of the LNTA.

$$A_v = g_{m_1} \cdot r_{0_1} \parallel r_{0_3} \parallel \frac{1}{g_{m_4}} \simeq 1 \tag{177}$$

having supposed $g_{m_1} \simeq g_{m_4}$. The amplifier is then used as a buffer for the realization of the self biasing of the common source pMOS. This low gain configuration is unusual for the common mode feedback loop but avoids the rise of instability problem since the open loop gain is low.

4.3.6 Simulation results

As done for the 40nm version, transconductance gain and output resistance of the low noise transconductance amplifier are reported in figures 63 and 64 and referred to a no load case; the in chain performance are plotted as well in figure 65. The output resistance, for higher frequencies, tends to higher value due to the frequency dependence of the real part of the output impedance. From the plots depicted in figure 65, one can appreciate the almost constant value of the scattering parameter S_{11} due to the new working region of the cascode devices, which now well insulate the common source stage from the load; gain labels are, for this reason, omitted. Table 8 summarizes all the performances obtained in the 22nm version of the LNTA.

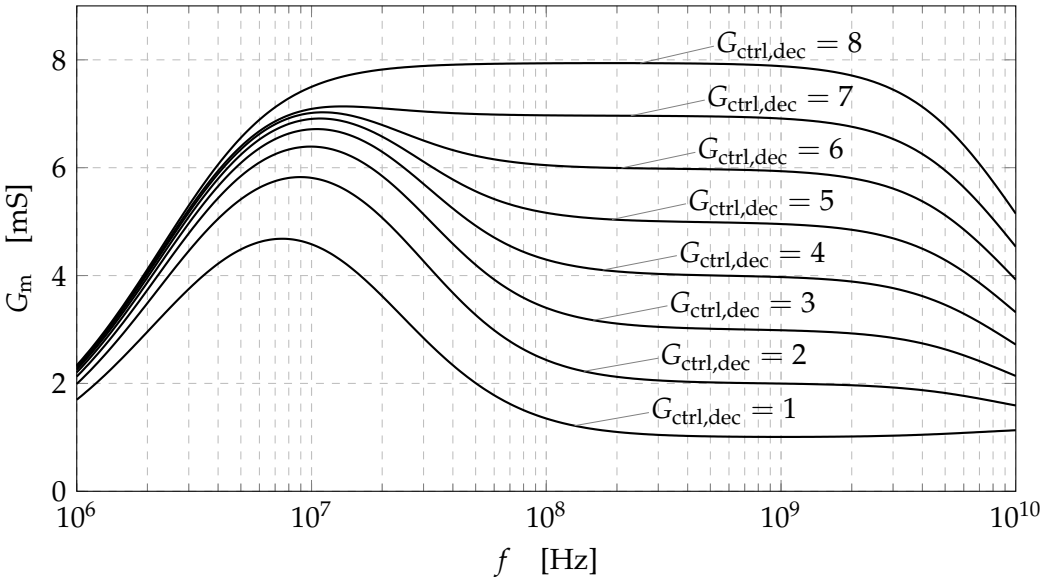


Figure 63: LNTA transconductance in the 22nm technology.

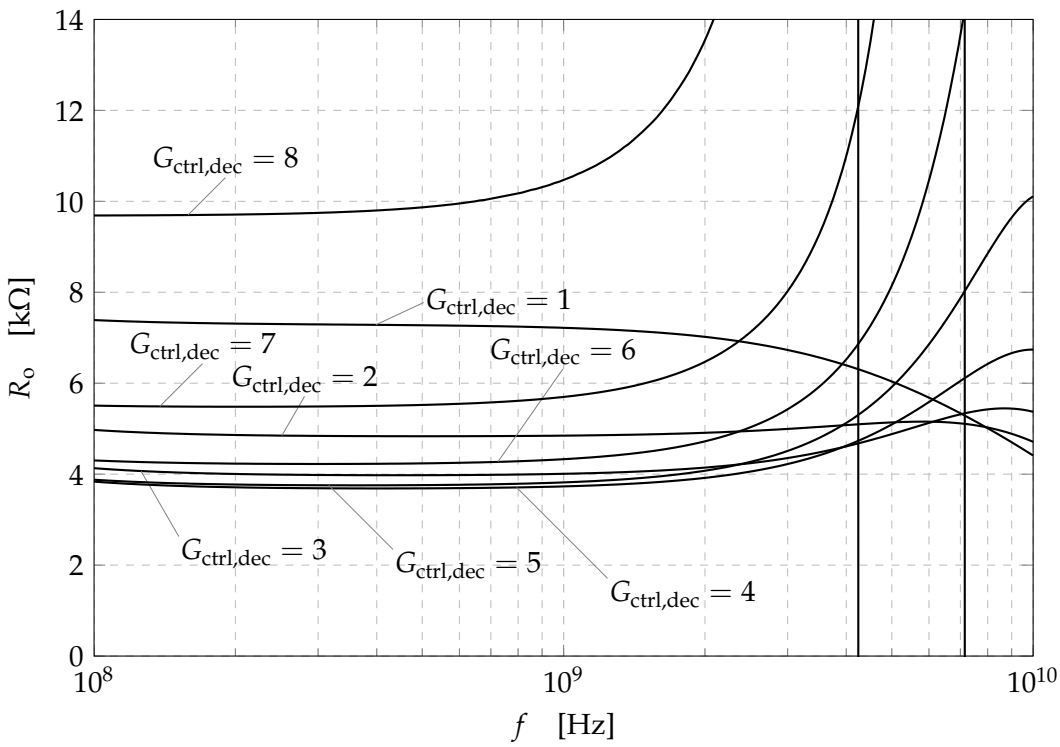


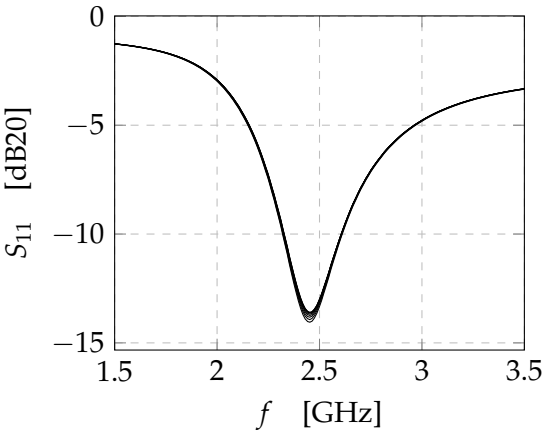
Figure 64: LNTA output resistance in the 22nm technology.

Table 8: main results for the new LNTA design at T = 27°C.

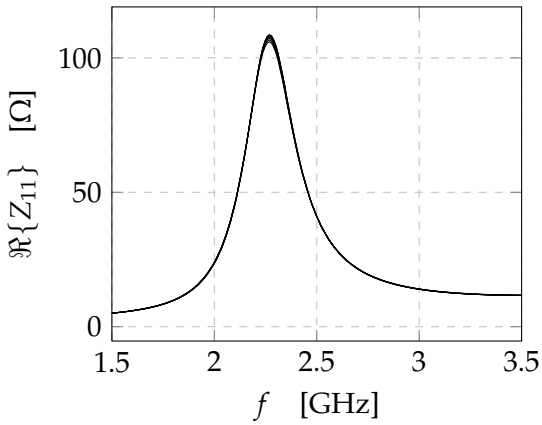
$G_{\text{ctrl, dec}}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF[dB10]	NF_{min}[dB10]
1	828	746	0,83	−13,6	9,46	9,41
2	828	746	1,57	−13,6	7,29	7,28
3	828	746	2,33	−13,6	6,16	6,14
4	828	746	3,01	−13,7	5,47	5,44
5	828	746	3,88	−13,7	5,01	4,95
6	828	746	4,67	−13,8	4,68	4,59
7	828	746	5,49	−13,9	4,42	4,30
8	828	746	6,32	−13,1	4,22	4,07

Table 9: main results for the new LNTA design at T = 55°C.

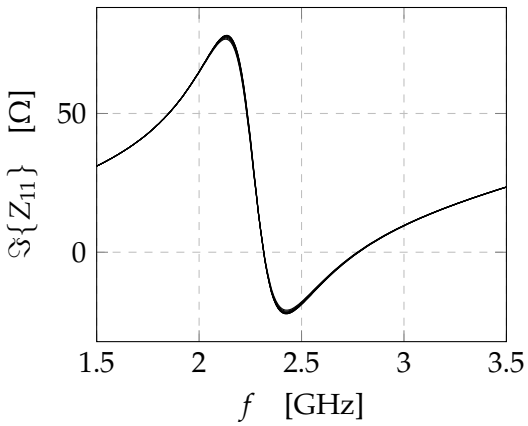
$G_{\text{ctrl, dec}}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF[dB10]	NF_{min}[dB10]
1	875	787	0,83	−13,8	9,94	9,90
2	875	787	1,56	−13,8	7,76	7,75
3	875	787	2,31	−13,9	6,60	6,59
4	875	787	3,01	−13,9	5,89	5,86
5	875	787	3,83	−14,0	5,40	5,35
6	875	787	4,61	−14,0	5,05	4,96
7	875	787	5,41	−14,2	4,78	4,66
8	875	787	6,22	−14,3	4,57	4,42



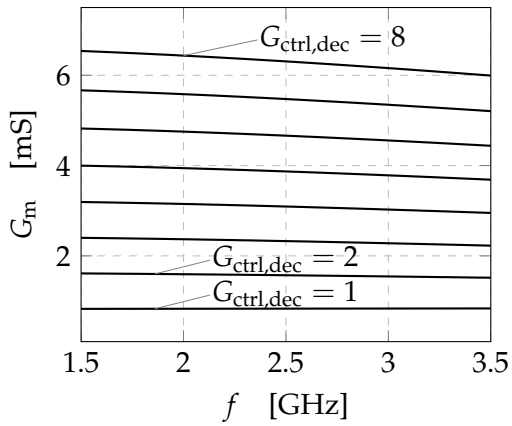
(a) Scattering parameter S_{11}



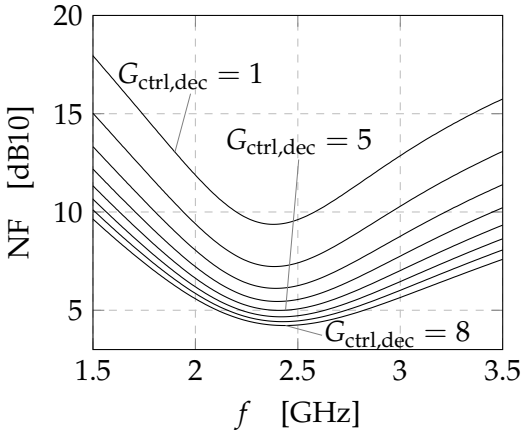
(b) Real part of the input impedance



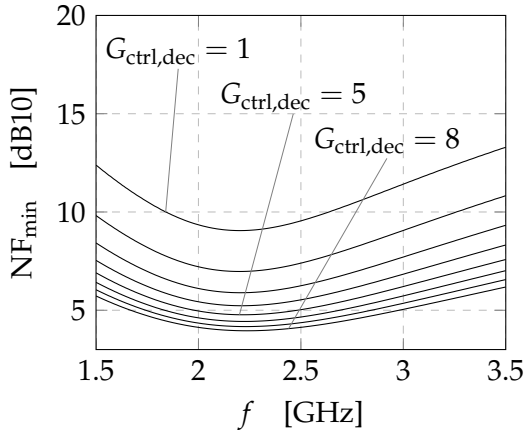
(c) Imaginary part of the input impedance



(d) Transconductance of the LNTA in chain



(e) Noise figure



(f) Minimum noise figure

Figure 65: the most important results obtained for the starting point low noise transconductance amplifier.

5 UPGRADED FULLY DIFFERENTIAL VARIABLE GAIN LNTA

In this chapter the design of a new version of the low noise transconductance amplifier is presented; the most important difference is the new approach for the gain tuning which helps saving power when the required gain for amplifying the signal is less than the maximum.

5.1 INTRODUCTION

The schematic of such new architecture is presented in figure 66. As can be immediately seen, only one signal path from input to output is present, and the common source stage has been split in different devices, forming basic cascode cells. The necessity of saving

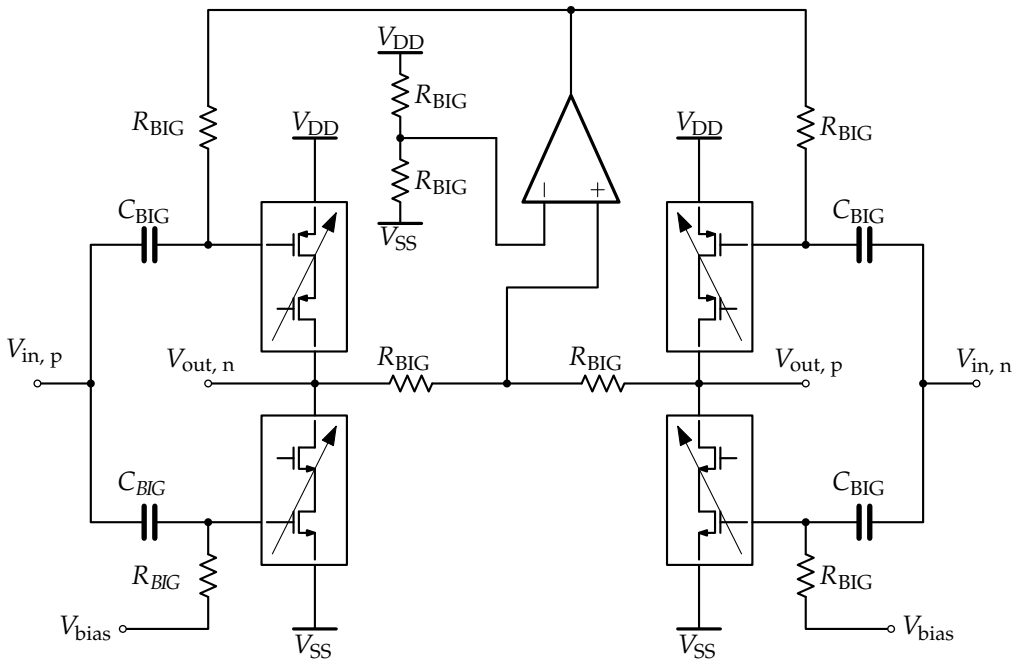


Figure 66: upgraded version of the LNTA in 22nm technology.

power has questioned the useless reason of sinking the same amount of current from the power supply even when the LNTA is operating at its lowest gain configuration. Compared to the earlier versions of the low noise amplifier discussed in this thesis, the new design has a different implementation for the core and, as a consequence, of the biasing circuit; the common mode feedback loop has been maintained since it has proved to be very robust compared to other solutions but with important changes in order to guarantee a more stable common mode dc operating point at the LNTA differential outputs.

5.2 WORKING PRINCIPLE

The new core of the low noise transconductance amplifier is made by four different sized complementary cascode amplifiers for each branch. Figures 67 and 68 depict the n-side and the p-side respectively. The common gate drain node is shared among the complementary structures and represents the output node of a single branch of the amplifier.

Each cascode amplifier is associated to one bit of the gain control word: the transconductance gain variation is then obtained by selecting the desired amount of active cascode devices, each of them contributing with their fixed transconductance value. The difference in terms of power consumptions with respect to the previous versions is straightforward: instead of changing the signal path of a common source MOS stage always consuming the same current value no matter the gain, here only the needed amplifiers are turned on. The current is thus directly proportional to the amount of transconductance gain the system requires: the lower the gain, the lower the power consumptions. A complementary structure allows to double the overall transconductance

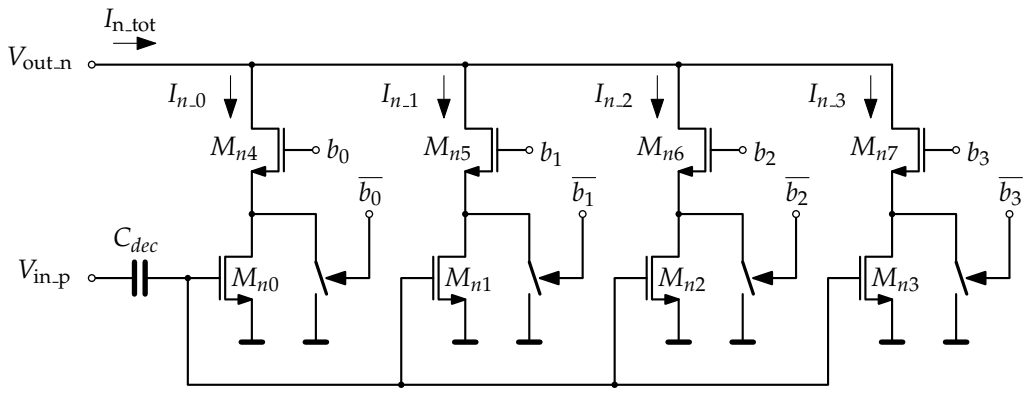


Figure 67: the nMOS cascode devices used in the new low power LNTA version.

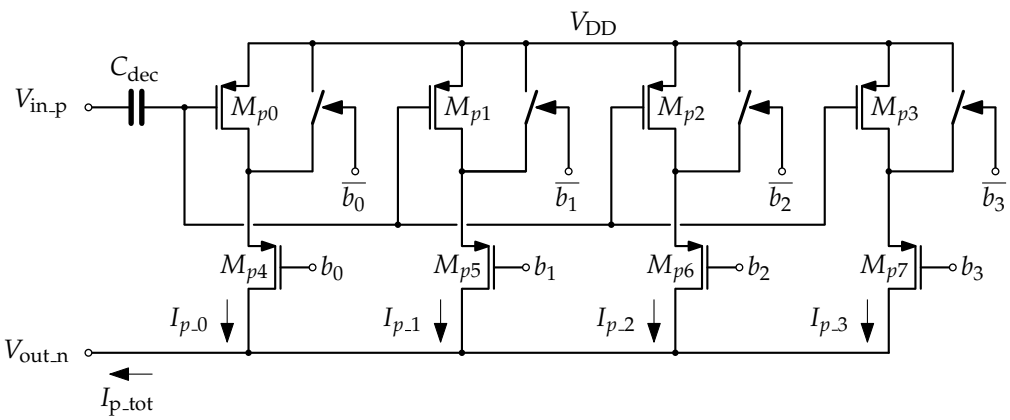


Figure 68: the pMOS cascode devices used in the new low power LNTA version.

sharing the same biasing current at the expense of a lower output voltage excursion: however, since only the output current matters, this problem does not exist, even though checks has to made to avoid unexpected behaviour in terms of biasing points.

For each complementary cascode, one can define the equivalent transconductance, $G_{m,eq}$, the equivalent input impedance, $Z_{in,eq}$ and the equivalent output impedance, $Z_{out,eq}$:

$$G_{m,eq} = g_{m,n} + g_{m,p} \simeq 2g_m \tag{178}$$

$$Z_{in,eq} = Z_{in,n} \parallel Z_{in,p} \simeq 2C_{in} \tag{179}$$

$$Z_{out,eq} = Z_{out,n} \parallel Z_{out,p} \simeq \frac{Z_{out,n}}{2} \tag{180}$$

Equations (178), (179) and (180) hold whenever the devices are biased into the correct operating region; if a branch is turned off, it features instead:

$$G_{m,eq} \simeq 0 \tag{181}$$

$$Z_{in,eq} \simeq 2C_{off} \tag{182}$$

$$Z_{out,eq} \to \infty \tag{183}$$

As can be seen from figures 67 and 68 the devices are turned on or off by enabling or disabling the common gate stages and opening or closing the switches in parallel to the common source stages. In this way it is assured that the node in between the two MOSFETs of the cascode device is kept at a known potential, avoiding any possible current leakage at high temperature when the correspondent cascode structure is off. It is possible to see that the MOSFET in common gate configuration is effectively turned off while the one in common stage configuration is actually not. Hence, being its gate at the same biasing potential, its input impedance is only slightly changed, allowing, theoretically, to obtain quite the same input impedance. For this reason, some considerations used in the device of the previous LNTA versions can be useful in the design process of the new one, especially for what concerns the decoupling capacitors, used to match the device with balun.

5.3 ANALYTICAL COMPUTATIONS

As done for the previous version of the amplifier, analytical analysis of the input impedance, the transconductance gain and the noise figure are performed. Figure 69 show the ac transformation applied to a single branch of the low noise amplifier. Here the pMOS branch of the single ended amplifier has been transformed in an equivalent nMOS branch, which doubles the transconductance of the equivalent two-port model of the cascode as well as the input capacitance and halving the output resistance, as discussed in the previous section. Because of the new structure reported in figures 67 and 68, one can assume the input capacitance C_{in}, mainly represented by C_{gs} is almost constant as the gain changes. In the practical case this hypothesis is correct only at first approximation and has to be verified by simulations. However, in order to get only some useful insights for the figure of merits, this hypothesis is here considered. This means that the two-port model of the single ended version of the LNTA is the one reported in figure 70.

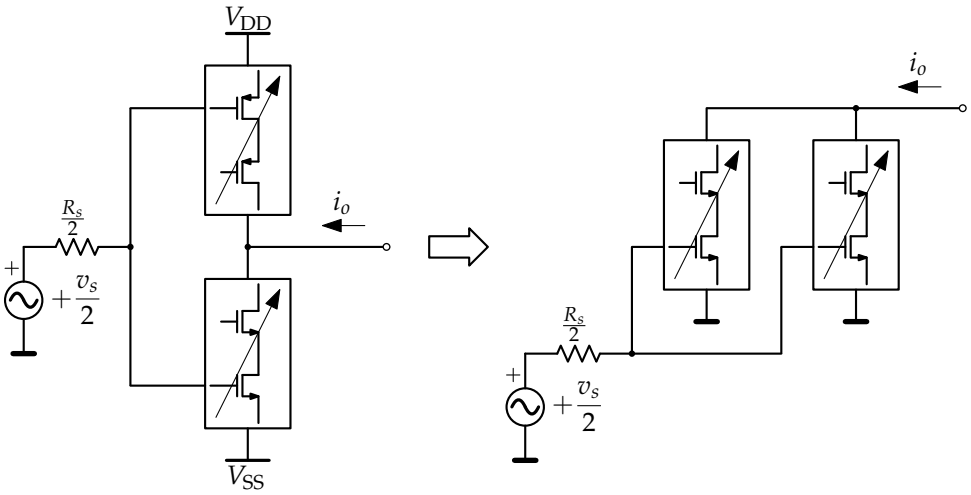


Figure 69: single ended complementary amplifier transformation: the pMOS branch is converted into nMOS for the small signal analysis. For the sake of simplicity nMOS and pMOS are assumed to be equivalent for the small signal point of view. Biasing circuit are not shown.

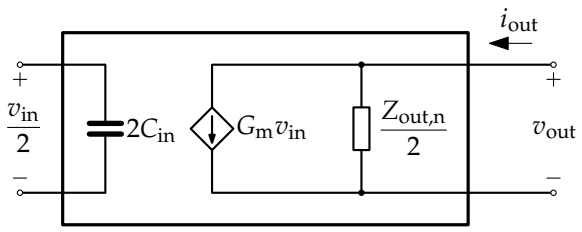


Figure 70: equivalent simplified two-ports model for the complementary cascode amplifier.

5.3.1 Input impedance

The input impedance can be computed considering the fact the MOSFETs of the common source stages are all operating in the sub-threshold region but do not have the same drain to source voltage. Because of this, the input impedance seen from the input balun will slightly change according to the gain variation. One can make the hypothesis these changes won't be excessive since the common source stages, when not used, are all still connected to the biasing circuit and thus correctly biased while their drain is shorted to their source by a parallel switch. Neglecting the contribution of the gate resistance, R_g, it is easier to consider the input admittance instead of the input impedance. Equation (184) already takes into account the number of parallel branch used in the schematic.

$$\begin{aligned} Y_{\text{in}} = \sum_{h=0}^{3} s \left[C_{\text{gs_}h} + \left(1 + \frac{g_{\text{m_}h}}{g_{\text{m_}h+4}}\right) C_{\text{gd_}h} \right] w_h \cdot b_h \\ + \sum_{h=0}^{3} s \left(C_{\text{gs_}h} + C_{\text{gd_}h} \right) w_h \cdot \overline{b_h} \end{aligned} \tag{184}$$

where it as been assumed the gate to source capacitance and the gate to drain capacitance do not change when the MOS drain to source voltage is shorted or not.

5.3.2 Transconductance gain

The transconductance gain can be computed considering the results of section 2.5. The short circuit current i_{sc} is given by:

$$i_{sc} = -G_{\text{m, eq}} \cdot \beta_{CG}(s) \frac{v_{\text{in}}}{2} = -2g_{\text{m}} \cdot \beta_{CG}(s) \frac{v_{\text{in}}}{2} = -g_{\text{m}} \beta_{CG}(s) \cdot v_{\text{in}} \tag{185}$$

For each branch, the transconductance of the CMOS cascode as function of the frequency is then given by equation (186):

$$G_{\text{m}}(s) = -g_{\text{m}} \cdot \beta_{\text{CG}}(s) \simeq -\frac{g_{\text{m}}}{1 + s\left(\frac{C_{\text{gs2}}+C_{\text{sb2}}+C_{\text{db1}}}{g'_{\text{m2}}}\right)} \tag{186}$$

Hence now, what changes in the transconductance gain is the amount of individual contribution each branch adds to the output node. If the only change for each branch is the MOS width size, then the expression for the variable transconductance gain of the amplifier is given by:

$$G_{\text{m,tot}}(s) \simeq \frac{g_{\text{m}}}{1 + s\left(\frac{C_{\text{gs2}}+C_{\text{sb2}}+C_{\text{db1}}}{g'_{\text{m2}}}\right)} \cdot G_{\text{ctrl}} \tag{187}$$

5.3.3 Output impedance

The output impedance of the upgraded version of the LNTA varies along the gain as well and it is given by the parallel of a cascode nMOS and a cascode pMOS: considering the frequency dependence as well, such impedance can be written as:

$$Z_{\text{out}} = Z_{\text{n,out}} \parallel Z_{\text{p,out}} \simeq \frac{1}{2} \cdot \frac{g'_{\text{m_cg}} r_{\text{0_cs}} r_{\text{0_cg}}}{1 + s(C_{\text{gd_cg}} + C_{\text{db_cg}}) g'_{\text{m_cg}} r_{\text{0_cs}} r_{\text{0_cg}}} \tag{188}$$

having assumed also in this case an identical small signal behaviour for the nMOS and the pMOS. Every branch that is used, besides increasing the overall transconductance, decreases the output impedance of the equivalent cascode amplifier, degrading the overall behaviour of the low noise transconductance amplifier. However, since the load is represented by a passive current controlled mixer, the amplifier sees a relatively low output impedance connected to its load when operating at the rf-frequencies, hence this problem becomes less important and can be forgotten (but, of course, simulations have to prove it).

5.3.4 Noise figure

The noise figure of this version can be derived from the case of the cascode device but taking into account the complementary part and the fact that parallel devices decrease the noise figure. The active devices are still biased in the sub-threshold working region, hence one has to take into account the equivalent noise model of that working region.

$$F \simeq 1 + \frac{R_g}{R_s} + \frac{n}{2}\frac{G_m R_s}{G_{ctrl}}\left[\frac{|R(j\omega)|^2}{R_s^2} + \left(\frac{\omega}{\omega_T}\right)^2\right] \tag{189}$$

where:

$$R(j\omega) = \frac{1 + j\omega R_g C_{in}}{G_{m_tot}}$$

Since R_g is usually very small especially with good layout techniques, then $\left(\frac{\omega}{\omega_T}\right)^2 \gg \frac{|R(j\omega)|^2}{R_s^2}$ and equation (189) can be further approximated as:

$$F \simeq 1 + \frac{R_g}{R_s} + \frac{n}{2}\frac{G_m R_s}{G_{ctrl}}\left(\frac{\omega}{\omega_T}\right)^2 \tag{190}$$

5.4 DESIGN STEPS

The leading idea of the design is to maintain the performances of the new LNTA as close as possible to the previous version of the design while lowering the power consumption for lower gain configurations.

The first step was to fix a maximum current consumption for the LNTA core; in order to maintain a binary weighted variable transconductance, four different size CMOS cascode amplifier branches have been used. By fixing a maximum current equal to $I_{D,max} = 400\mu A$, for each half of the differential amplifier, it freely comes that the first two branches, the less weighted ones, have to consume up to 50µA each, the third up to 100µA and the fourth up to 200µA. The remaining 200µA can be used for the biasing circuitry as well as the common feedback amplifier. The number of fingers, the width per finger and the channel length can be maintained from the previous design.

In order to make the layout easier, it has been decided to build eight equally sized complementary cascode devices per leg instead of different sized ones; the digital control will simply turn two identical CMOS cascodes instead of a double width single

cascode or four identical CMOS cascodes instead of four times sized one. Table 10 sums up the g_m/I_D methodology parameters.

Table 10: summary of small signal parameters for the nMOS common source: subscripts cs and cg refer to common source and common gate stages respectively.

Device	g_m[mS]	I_D[µA]	$\frac{g_m}{I_D}$[V^{-}1]	V^*[mV]
$M_{cs,\,n}$	1	50	20	100
$M_{cs,\,p}$	1	50	20	100
$M_{cg,\,n}$	1	50	20	100
$M_{cg,\,p}$	1	50	20	100

Once the width size per transistor has been graphically chosen, a good point is to find what width per finger ratio does give the minimum noise figure. For this purpose, by fixing the number of fingers, one can set, accordingly, the width per finger and perform a parametric simulation in order to understand the trend of noise figure and minimum noise figure. The optimal finger number that minimizes the latter has been found in this way.

5.5 BIASING CIRCUIT

The biasing circuit of the LNTA has been redesigned in order to be more robust against PVT variations: ideally, the circuit reported in figure 71 is a good and performant biasing circuit for the complementary cascode device. However such solution makes use of too

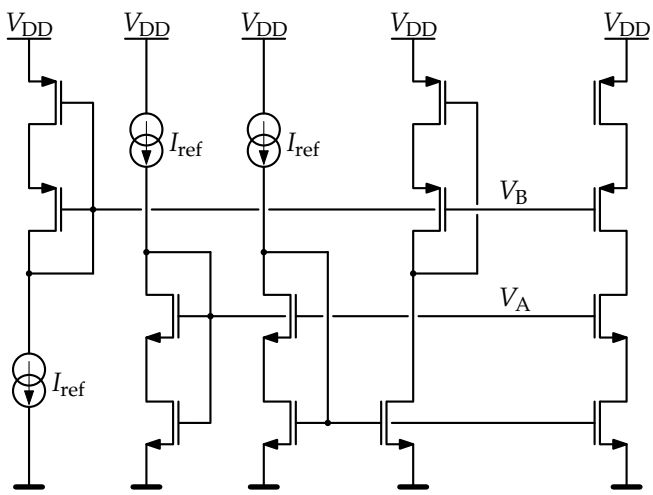


Figure 71: the proposed version of the main biasing circuit of the upgraded LNTA in 22nm.

many I_{ref} branches which are not available from the current reference generator. The simpler schematic reported in figure 72 overcome the issue by replacing the battery legs that produces voltages V_A and V_B with two resistors. The number of reference branches has been reduced to one, satisfying the requirements. The size of such resistor can be found by fixing the operating point of the MOSFETs involved for the cascode current

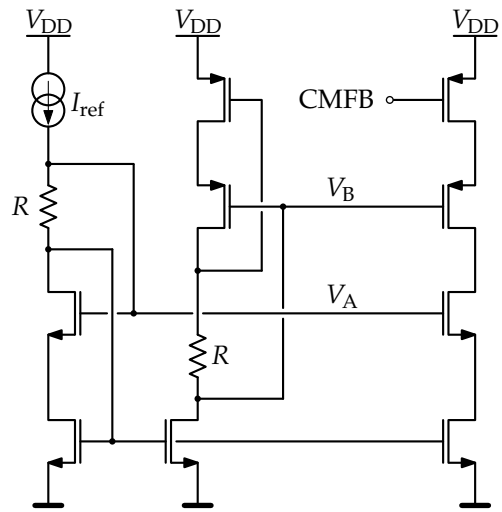


Figure 72: the implemented version of the main biasing circuit for the upgraded LNTA in 22nm.

mirrors. The reference current is known and the size of the active devices of the amplifier are identical to a single complementary cascode branch. In order not to let the biasing transistors to operate outside the subthreshold region, the resistor value can be fixed by consider a reasonable voltage drop which does not take too much headroom from the branch:

$$R = \frac{V_{max}}{I_{\text{ref}}} \tag{191}$$

As for the previous amplifier design, the biasing voltages obtained by the current mirror are sent to a digital circuit that turns on or off the devices required for a specific gain configuration.

5.6 THE COMMON MODE FEEDBACK LOOP

The Common Mode Feedback Amplifier has been maintained in the upgraded version of the LNTA because it proved to be robust and capable of obtaining a quite constant biasing point along temperature variation. In this case, a new version of the dedicated amplifier (OTA) has been derived from the current version of the library and used in the project. The differential pair has been maintained but the left branch has been removed being the cause of the low gain of the amplifier itself. In such case the DC open loop gain of the amplifier rises considerably, being given by expression (192).

$$A_v = g_{m_1} \cdot r_{0_1} \parallel r_{0_3} \tag{192}$$

Due to the absence of the diode connected p channel MOS, the differential pair now sees a very high output impedance and the simulated DC voltage gain rises up to almost 33dB or, in a linear scale, nearly 50V/V. Since the gain now is quite consistent, one has to check the impact on the new open loop gain and the new phase margin.

First of all one has to understand how the common mode feedback loop really works in the new schematic: one remembers that it allows to bias part of the LNTA circuit in

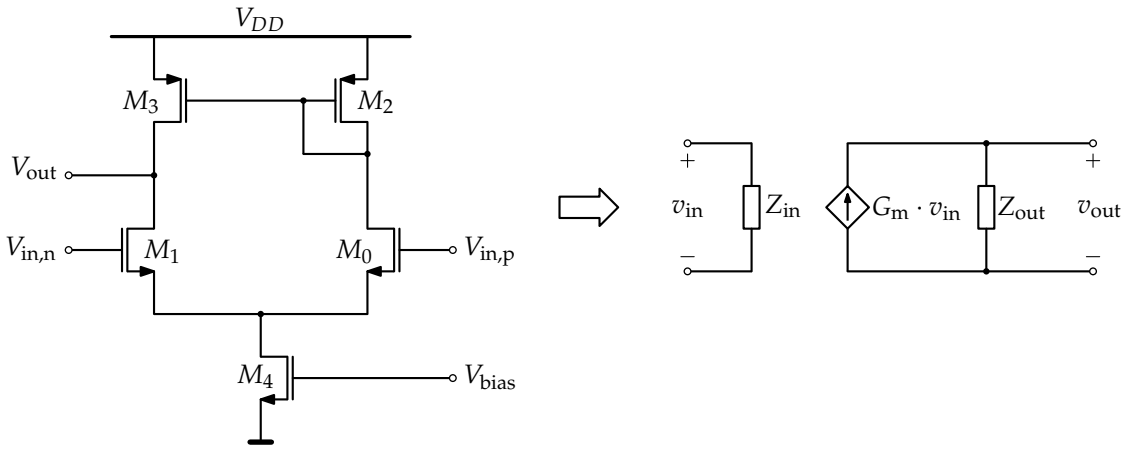


Figure 73: the new OTA version for the CMFB loop where only the differential pair has been maintained.

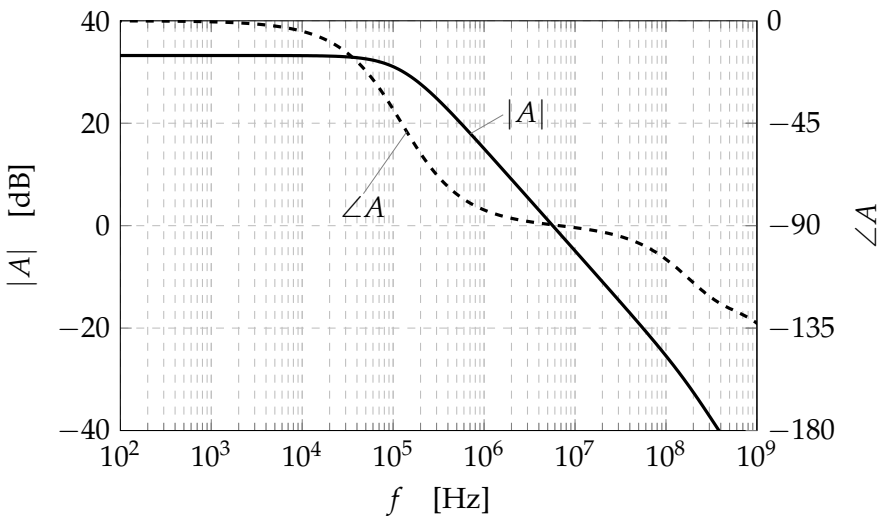


Figure 74: open loop gain and phase of the new OTA version load by 500fF capacitor.

order to fix the common mode DC operating point of the amplifier at a reference voltage level V_{ref} which, in this place, is exactly equal to $\frac{V_{DD}}{2}$, hence $V_{ref} = 450\text{mV}$.

It's clear, however, that the LNTA produces an amplified signal in terms of differential current and not voltage. As a consequence is not compulsory to obtain a very precise control on the common mode DC output voltage since we're not interested in guaranteeing the maximum output voltage variation. Nevertheless, the common mode feedback loop is still important because it assures the MOSFETs involved in the signal amplification remain in the proper operating region, defined in the design stage.

From the schematic of the upgraded LNTA depicted in figure (66), one can see the OTA is loaded not only by the p-MOS cascode devices of the LNTA, but also by the input circuit, i.e. the balun, the switch and the decoupling capacitors, i.e. the equivalent signal source. The decoupling capacitors insulate the useful rf input signal from the biasing signals interfere: for this reason, at low frequency, a very high impedance is seen across

it and a reasonable hypothesis for simplifying further computation is to treat them like open circuits. Such hypothesis has to be verified by simulations.

A similar approximation can be done for what concern the decoupling capacitors connecting the output of the LNTA to the passive down-conversion mixers: at low frequency, the mixer is decoupled from the amplifier output hence the pMOS cascodes are loaded only by their output resistance, that of the nMOS cascode and the input impedance of the CMFB OTA. The latter can be reasonably though as infinite for our purpose.

In order to investigate the overall stability of the CMFB loop, an *stb simulation* has been performed in the simulator environment. From the plot, it can be noticed that the changes applied to the CMFB amplifier structure produces a too high gain to achieve a satisfying phase margin at the crossing frequency. The phase margin of the LNTA is furthermore affected by the current gain selection: table 11 collects the simulation results. This can help finding what the worst case really is and provide an effective solution for all the other configurations. A compensation is likely needed. A block diagram of the overall biasing system may be useful to understand if and where a suitable compensation network can be placed without affecting the higher frequency performances of the LNTA. Such block diagram is depicted in figure 75. Different blocks

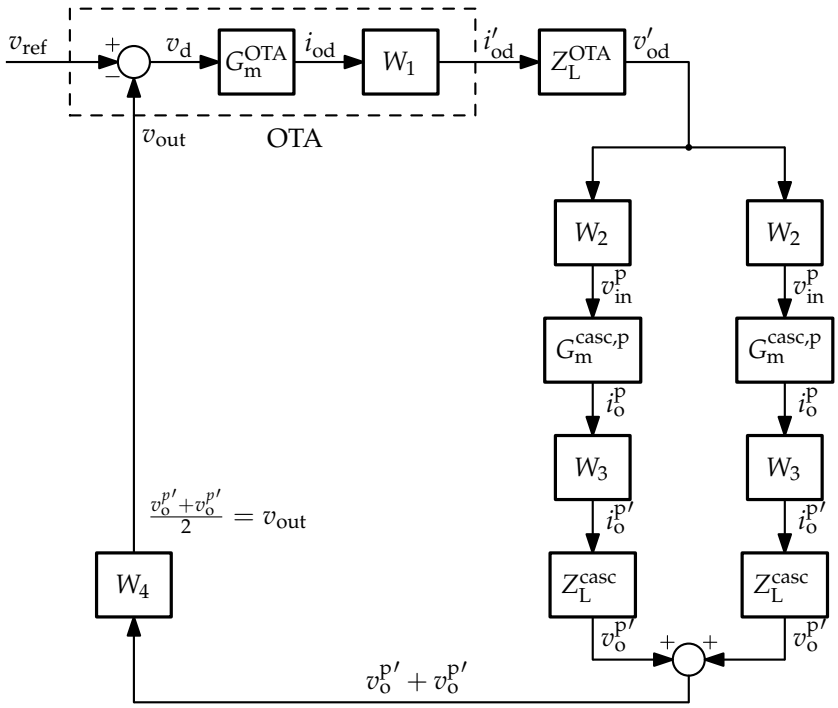


Figure 75: useful block diagram for the common mode feedback loop.

have been reported, each of them with a precise definition:

- OTA transconductance, G_m^{OTA} which converts the differential input voltage into a single ended current value;

- the interface transfer function W_1 defined as the current divider intrinsically present whenever the a load is present at the output of the OTA:

$$W_1 = \frac{Z_o^{OTA}}{Z_o^{OTA} + Z_L^{OTA}} \tag{193}$$

- the load impedance which is connected to the output port of the OTA, Z_L^{OTA}. Under the previous hypothesis, one has:

$$Z_L^{OTA} \simeq \frac{1 + sC_{\text{in}}^{\text{casc,p}} R_{\text{BIG}}}{sC_{\text{in}}^{\text{casc,p}}} \tag{194}$$

- the interface transfer function W_2 defined as the voltage divider:

$$W_2 = \frac{1}{1 + sC_{\text{in}}^{\text{casc,p}} R_{\text{BIG}}} \tag{195}$$

- the LNTA p-cascode transconductance, $G_{\text{m}}^{\text{casc,p}}$;
- the interface transfer function W_3 defined as the current divider:

$$W_3 = \frac{Z_o^{\text{casc,p}}}{Z_o^{\text{casc,p}} + Z_{\text{load}}^{\text{casc,p}}} \tag{196}$$

- the approximated load impedance connected to the output of the p-cascode amplifiers:

$$Z_{\text{load}}^{\text{casc,p}} \simeq Z_{\text{o}}^{\text{casc,n}} \tag{197}$$

- the last transfer function is $W_4 = \frac{1}{2}$ which computes the average of the common mode DC output voltage extracted from the two branches of the differential amplifier.

With the assumptions made so far, the new schematic is depicted in figure 76. and also one has:

$$Z_L^{\text{OTA}}(s) \simeq \frac{1 + sR_{big}C_{in}}{sC_{in}} \tag{198}$$

$$W_1(s) \simeq \frac{s2C_{in}R_o}{1 + s2C_{in}\left(R_o + \frac{R_{big}}{2}\right)} \tag{199}$$

$$W_2(s) \simeq \frac{1}{1 + sR_{big}C_{in}} \tag{200}$$

$$W_3(s) \simeq \frac{1}{2} \tag{201}$$

$$Z_L^{OTA}(s) \simeq Z_o^{casc,n} \tag{202}$$

The OTA, being realized with a single stage, doesn't introduce important poles nearby the loop gain crossing frequency, except the dominant one. One has to concentrate the effort in searching a general system compensation which also involves the pMOS cascode amplifier without affecting the internal structure of the OTA, i.e. lowering the

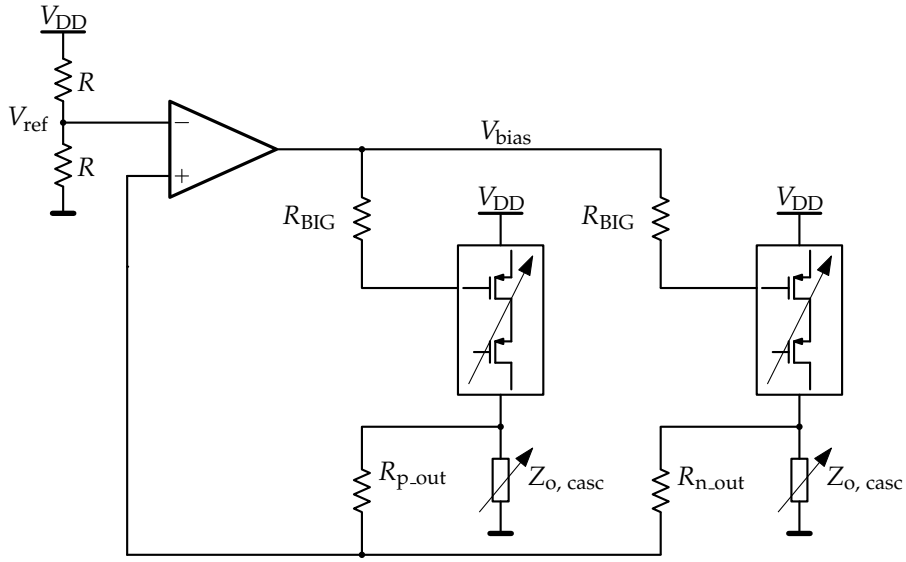


Figure 76: the simplified schematic of CMFB loop used for the auto-biasing of the pMOS common source stages.

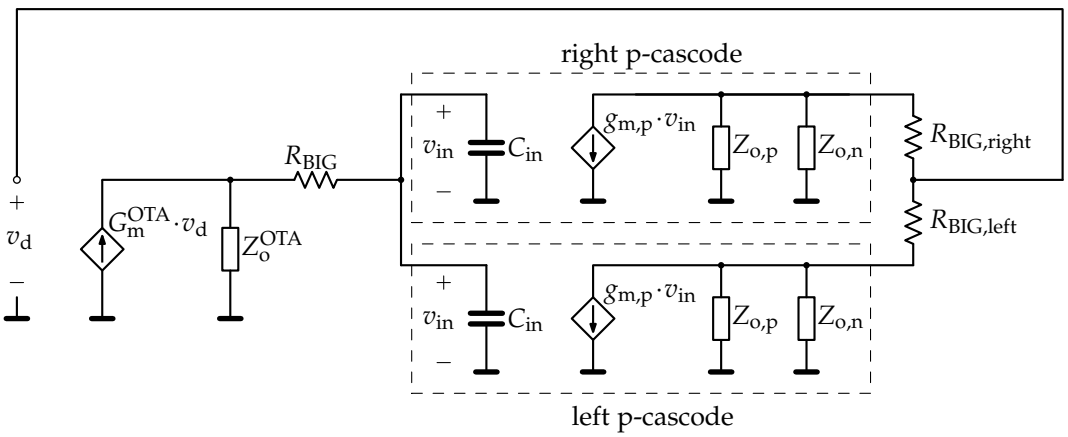


Figure 77: small signal for the simplified schematic of the common mode feedback loop.

gain. Furthermore, no changes are allowed for the decoupling capacitance and biasing resistances in order to avoid degradation of the high frequency performances of the LNTA. As can be seen in table 11, the higher the gain of the LNTA, the higher is the crossing frequency f_c and the lower is the phase margin. The worst case is then the one associated to the maximum gain operation condition. One may fix the required phase margin to be equal to at least 45° to avoid long term oscillations for the worst gain condition: the stability is then automatically solved for lower gain configurations.

In this frequency range, the equivalent balun output inductors represent a very low impedance hence Z_B is dominated by the decoupling capacitance. The dominant pole is thus represented by such capacitance in parallel to the pMOS cascode input capacitance. One may think the higher the input capacitance, the lower the frequency of the dominant pole hence higher the phase margin. This is partially true, however one has to consider that, in such case, the cascode reaches the maximum gain: since it appears in the overall CMFB loop gain, this would mean an higher low frequency gain as well.

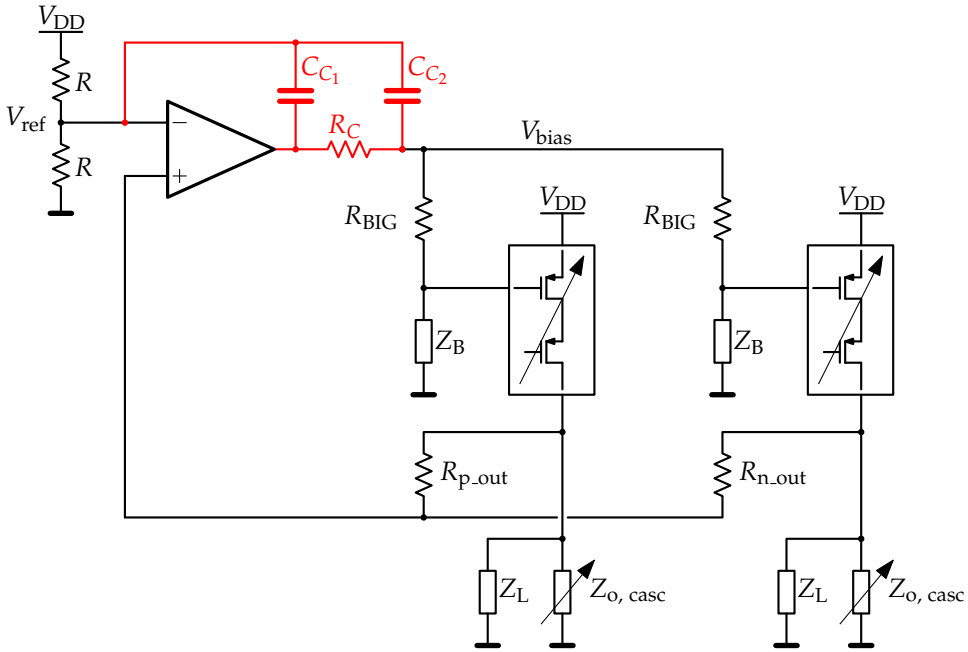


Figure 78: the compensated CMFB loop used for the auto-biasing of the pMOS common source stages.

The type of compensation that has been used to solve the problem is dominant pole plus a capacitive load compensation network. It makes use of two different value capacitances, C_{C_1} and C_{C_2} that operates at two different frequency range and resistor R_C helps in insulating the OTA amplifier from the load net. Results and theory aspects have been taken from [10], [3], [18]. As can bee seen in figure 80 and table 13, with proper values, the compensation network is able to boost the phase margin up to 45° even in the worst case scenario, represented by the highest working temperature condition.

5.7 SIMULATION RESULTS

The transconductance of the new version of the Low Noise Transconductance amplifier and the output resistance are shown in figures 81 and 82. As can be seen from the plots, both the transconductance and the output resistance show a flatter frequency response with respect to the previous versions. From 83 one can see that the input impedance variation is higher with respect to the current low noise amplifier design, but still satisfying the given specs. Table 14 summarizes all the performances obtained in the 22nm version of the LNTA and table 15 for 55°.

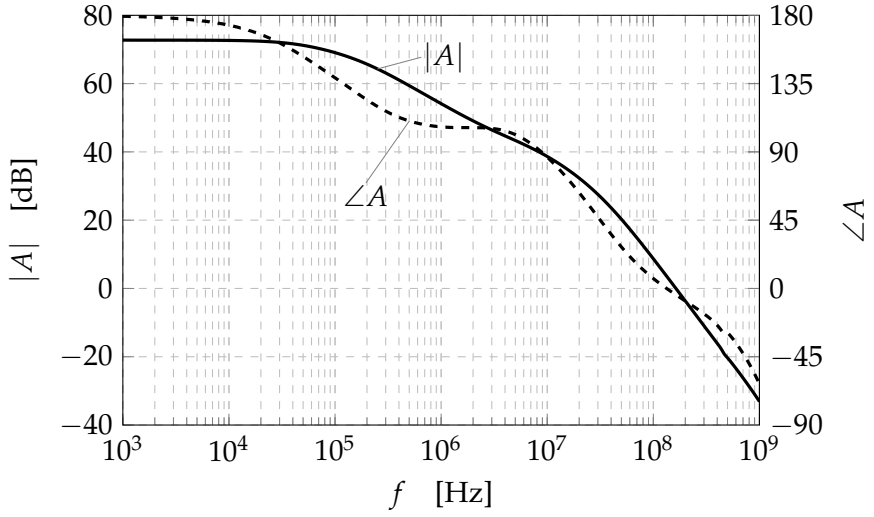


Figure 79: bode plot of the uncompensated common mode feedback loop for the maximum gain configuration.

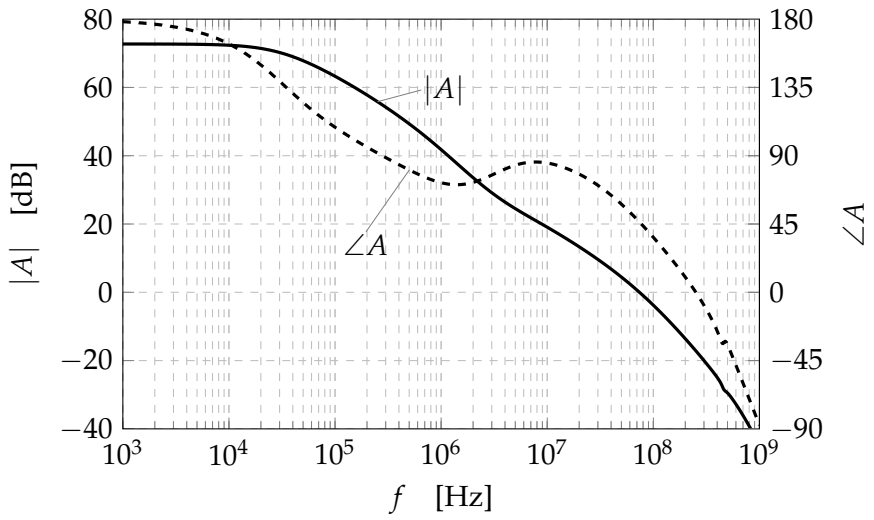


Figure 80: bode plot of the compensated common mode feedback loop for the maximum gain configuration.

Table 11: summary of the uncompensated CMFB loop stability performances for the upgraded LNTA.

$G_{\text{ctrl, dec}}$	I_{bias}[µA]	Phase Margin [°]	f_c [MHz]
1	168	1,3	74
2	263	<0	–
3	357	<0	–
4	451	<0	–
5	545	<0	–
6	639	<0	–
7	734	<0	–
8	828	<0	–

Table 12: summary of the compensated CMFB loop stability performances for the upgraded LNTA at $T = 27°C$.

$G_{\text{ctrl, dec}}$	I_{bias}[µA]	Phase Margin [°]	f_c [MHz]
1	168	45	23
2	263	47	38
3	357	47	50
4	451	46	58
5	545	46	63
6	639	46	68
7	734	46	72
8	828	46	74

Table 13: summary of the compensated CMFB loop stability performances for the upgraded LNTA at $T = 55°C$.

$G_{\text{ctrl, dec}}$	I_{bias}[µA]	Phase Margin [°]	f_c [MHz]
1	171	46	23
2	265	47	38
3	360	47	50
4	454	47	58
5	549	47	63
6	643	47	68
7	737	47	72
8	832	47	74

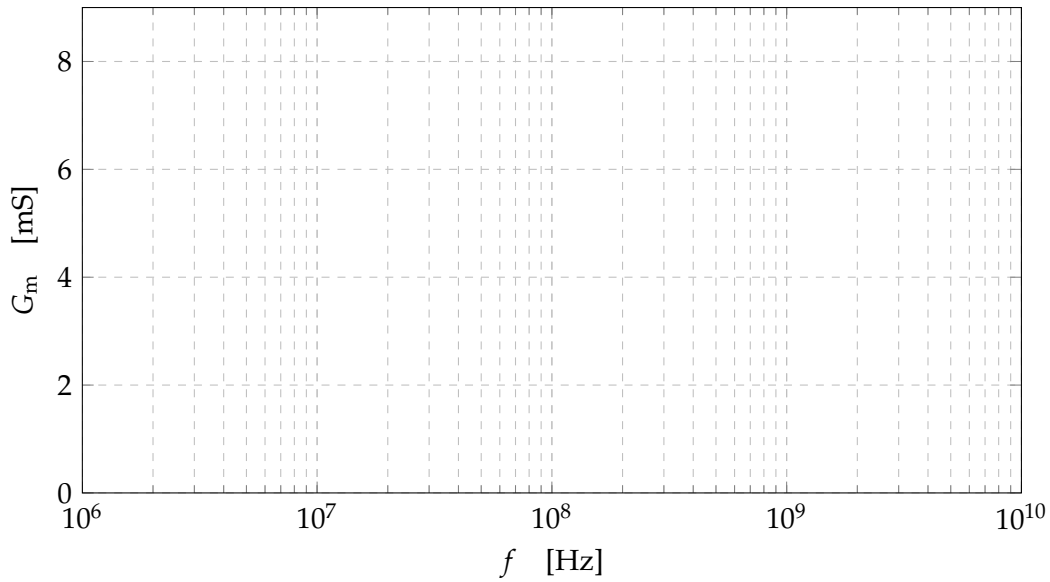


Figure 81: transconductance curves for different gain settings of the new amplifier.

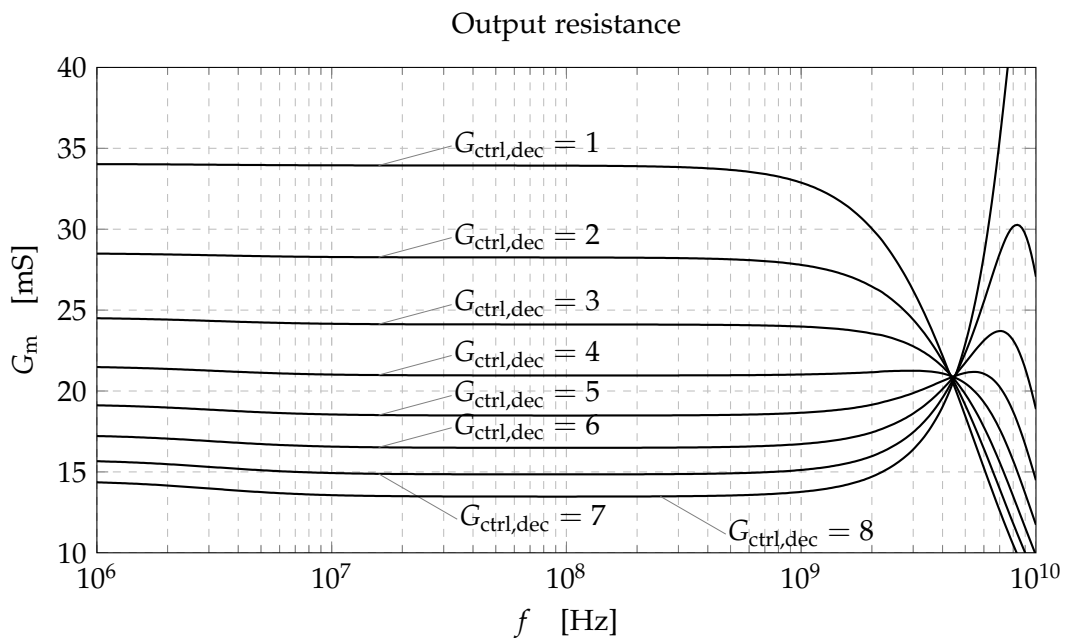


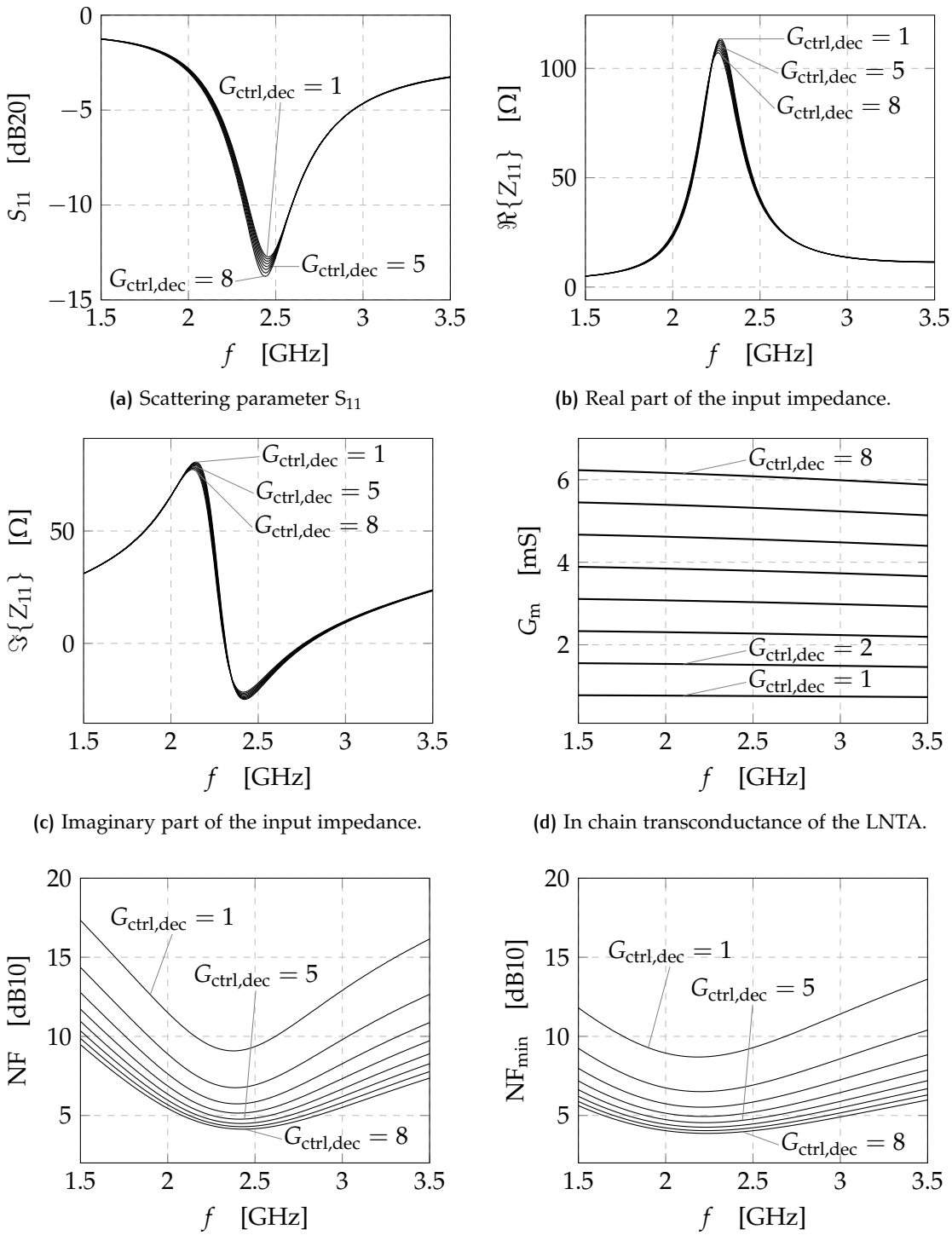
Figure 82: output resistance curves for different gain settings of the new amplifier.

Table 14: main results for the new LNTA design at T = 27°C.

$G_{\text{ctrl, dec}}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF_{11}[dB10]	NF_{min}[dB10]
1	168	152	0,76	−12,7	9,18	9,13
2	262	236	1,51	−12,8	6,81	6,80
3	357	321	2,28	−13,0	5,77	5,75
4	451	406	3,04	−13,1	5,17	5,13
5	545	491	3,80	−13,2	4,78	4,71
6	639	575	4,56	−13,4	4,50	4,40
7	734	660	5,33	−13,6	4,30	4,17
8	828	745	6,09	−13,7	4,14	3,98

Table 15: main results for the new LNTA design at $T = 55°C$.

$G_{\text{ctrl, dec}}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF_{11}[dB10]	NF_{min}[dB10]
1	170	154	0,72	−12,9	9,83	9,78
2	265	239	1,44	−13,0	7,38	7,38
3	360	324	2,15	−13,2	6,29	6,27
4	454	409	2,87	−13,3	5,65	5,61
5	549	494	3,59	−13,5	5,23	5,16
6	643	579	4,31	−13,6	4,93	4,83
7	737	664	5,04	−13,8	4,70	4,58
8	832	749	5,78	−13,9	4,53	4,38



(a) Scattering parameter S_{11}

(b) Real part of the input impedance.

(c) Imaginary part of the input impedance.

(d) In chain transconductance of the LNTA.

(e) Noise figure

(f) Minimum noise figure

Figure 83: the most important results obtained new low noise transconductance amplifier.

6 LAYOUT

The chapter shows how the amplifier previously designed is transposed into a integrated circuit representation; the layout process consists in taking the physical implementation of active and passive components and realized the connections according to the schematic.

6.1 INTRODUCTION

Each technology uses different layers both for components implementation and the nets. For the latter different metal layers are usually adopted; starting from the semiconductor material, metal thickness and conductivity increase moving towards the chip surface. Power connection are thus realized with the top or the more higher metal levels.

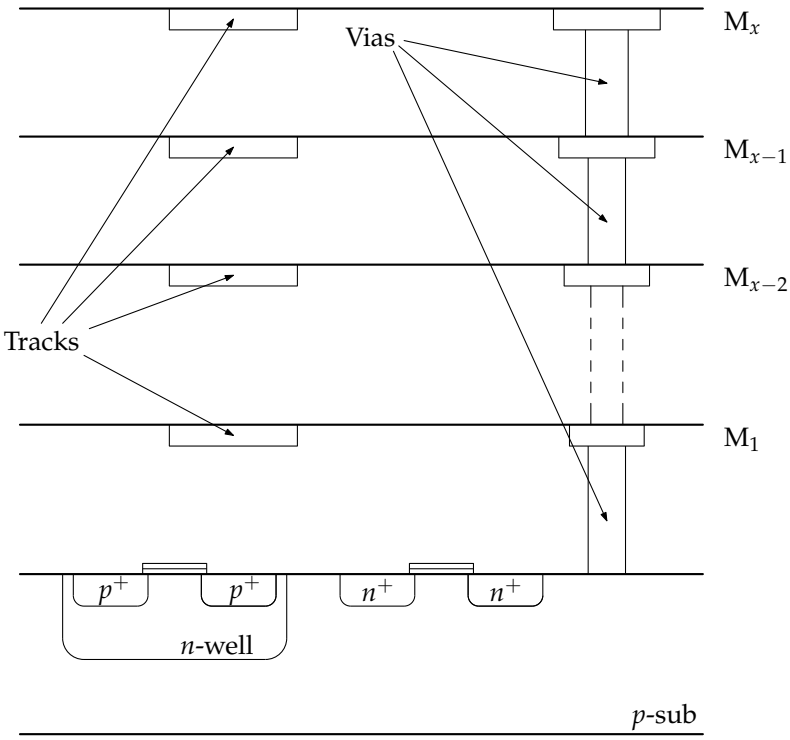


Figure 84: example of a layout stack for a generic technology.

An example of cross-section for a generic chip is the one depicted in figure 84. Vias are used to connect the metals and ensure a good contact among different levels. The active area is usually found on the lower layer and the others are made growing on it, realizing the connections.

6.2 LAYOUT DESIGN PROCESS

The layout process is developed can be split into four main steps:

1. the positioning inside the allowed active area of all the amplifier components is performed and the routing of all the traces that appear in the schematic level are drawn. Active and passive components layers are usually defined by the technology in use in such a way the designer has only to size them; however, some change might be necessary in particular cases. For instance, the shield that encircle a RF MOS device may be removed to make easier the grouping of multiple parts without sacrificing precious space. The ring can then be added to the entire group, being sure, by post simulations, that performance are not badly affected. One has to keep in mind that any change may not result in a pre and post layout exact conformity for the single component.

2. The second important process is to perform the *Design Rule Checking* (DRC) analysis. The layout rules depend on the technology which defines tracks width and clearance, distances between components, vias size as well as metal density and so on.

3. Once the DRC rules are all fulfilled, the *Layout Versus Schematic* (LVS) check is made. This check is carried on to ensure that each net on the schematic has the correspondent track in the layout and vice versa. Also, every component appearing in the layout has to match with the same features as in the schematic, both in its real presence and in its size.

4. The last step, if all the previous ones went well, is the *parasitic extraction* where the parasitics elements generated by the layout design are estimated. According to the level of accuracy one wants to achieve, different options are available. Here, since the circuit operation frequency is not extremely high (ISM band), it makes sense to use an RC extraction, neglecting the presence of possible inductance (L) or mutual inductance (KL). The extracted results are finally used to perform the same kind of simulation done with the schematic level but with a more realistic and accurate model which takes into account losses and parasitics element neglected in the designing process.

The layout process seems simple but in practice every track produces a parasitic resistance, capacitance and inductance, which might adversely affect the performance. This is really true for radio-frequency integrated circuits, especially when operating frequency is way beyond the giga-hertz threshold.

6.3 PREVIOUS LNTA DESIGNS IN 40NM AND 22NM TECHNOLOGIES

As a comparison with the layout made for the new low noise amplifier, the one of the previous versions in 40nm and 22nm are also reproduced; figure 85) is about the 40nm technology while figure 86 shows the current amplifier used in the Bluetooth radio.

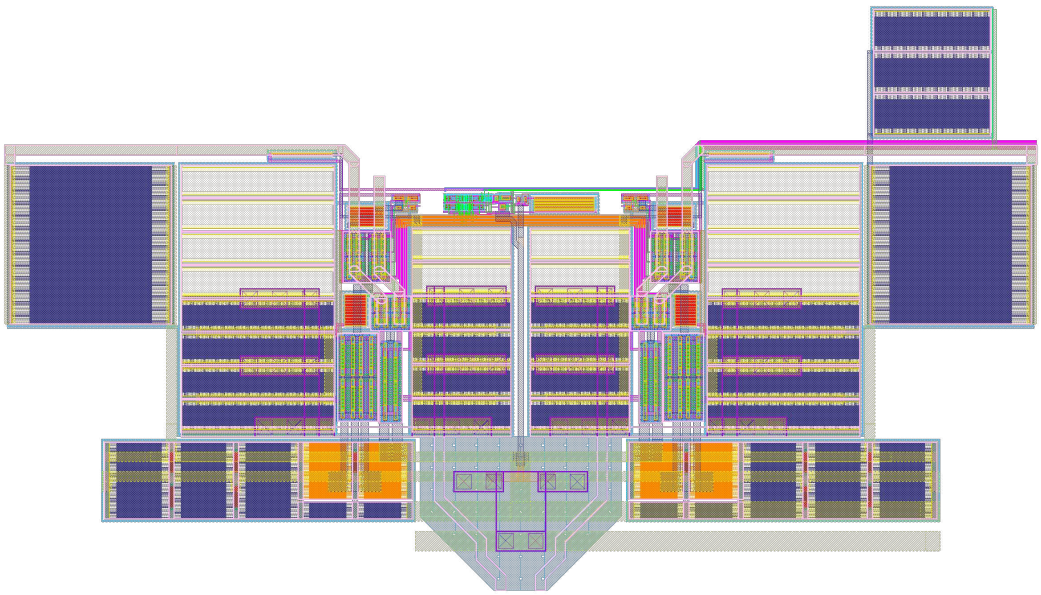


Figure 85: main layout of the 40nm version of the LNTA.

The shape of the two amplifiers is quite different since they come from two distinct projects; the main differences can be found in the arrangement of the matching and filtering capacitors while the signal path of the active cores is quite similar and confined in two arrays of pMOS and nMOS transistors.

For the new design a pattern similar to the 22nm version might be adopted, also to make sure it can fit the place it is supposed to be inserted for a future version of the radio.

6.4 LNTA UPGRADED IN 22NM

The layout designed started with the active core of the amplifier; to simplify the plan, the elementary cells of the nMOS and pMOS cascode amplifiers have been realized first. The idea was to increase the complexity in a progressive way to make the work easier and straightforward. The symmetry of the amplifier was also exploited for the same purposes.

Figure 87 shows the disposal of the elementary cells of one of the nMOS cascode branch. For the pMOS the arrangement is similar.

The digital circuitry is depicted in figure 88; the thin wires are used for the digital gain control. In this case, the track width is not a issue since the circuits works mainly in DC, excluding transients due to gain word changes and startups. In fact, MOS transistors show a huge input resistance at low frequency hence no DC current is actually flowing through them, meaning a big series resistance won't influence its behaviour.

This holds for the common source stages, but for the common gate a slightly different situation is obtained. In this case, even though the impedance between gate and source is very high at low frequency, at high frequency a couple zero-pole is created because of

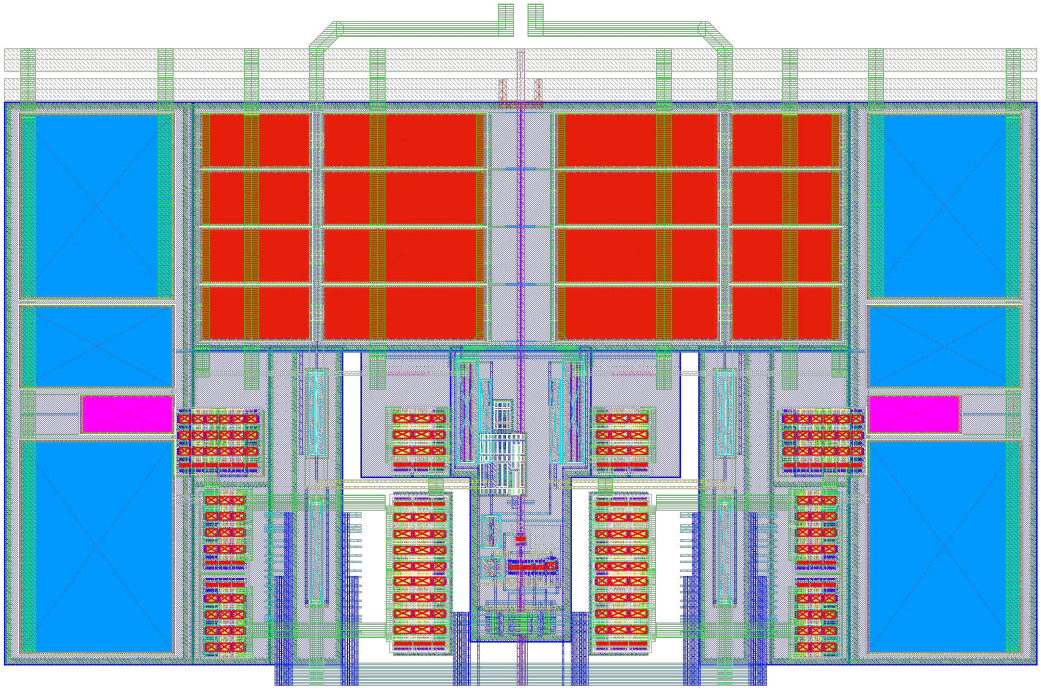


Figure 86: main layout of the 22nm version of the LNTA.

the series of capacitance C_{gs} and the resistance of the wire. The zero so created can kill the available signal coming the common source stage jeopardising the high frequency gain. For this reason, the common gate stages should be kept close to each other and long connection between their gates avoided. The common resistance, however, is not problematic since, because of the symmetry, both of its terminals are connected to an ac ground. Also, the source parasitic resistance of the common source stages might lower the amplifier gain because of degeneration; the nets involved in the connection should be kept as short as possible.

The complete layout of the low noise transconductance amplifier is shown in figure 91. The active core, visible in the middle, is still smaller compared to the capacitors used to provide the input matching and the filtering from the power supply fluctuations.

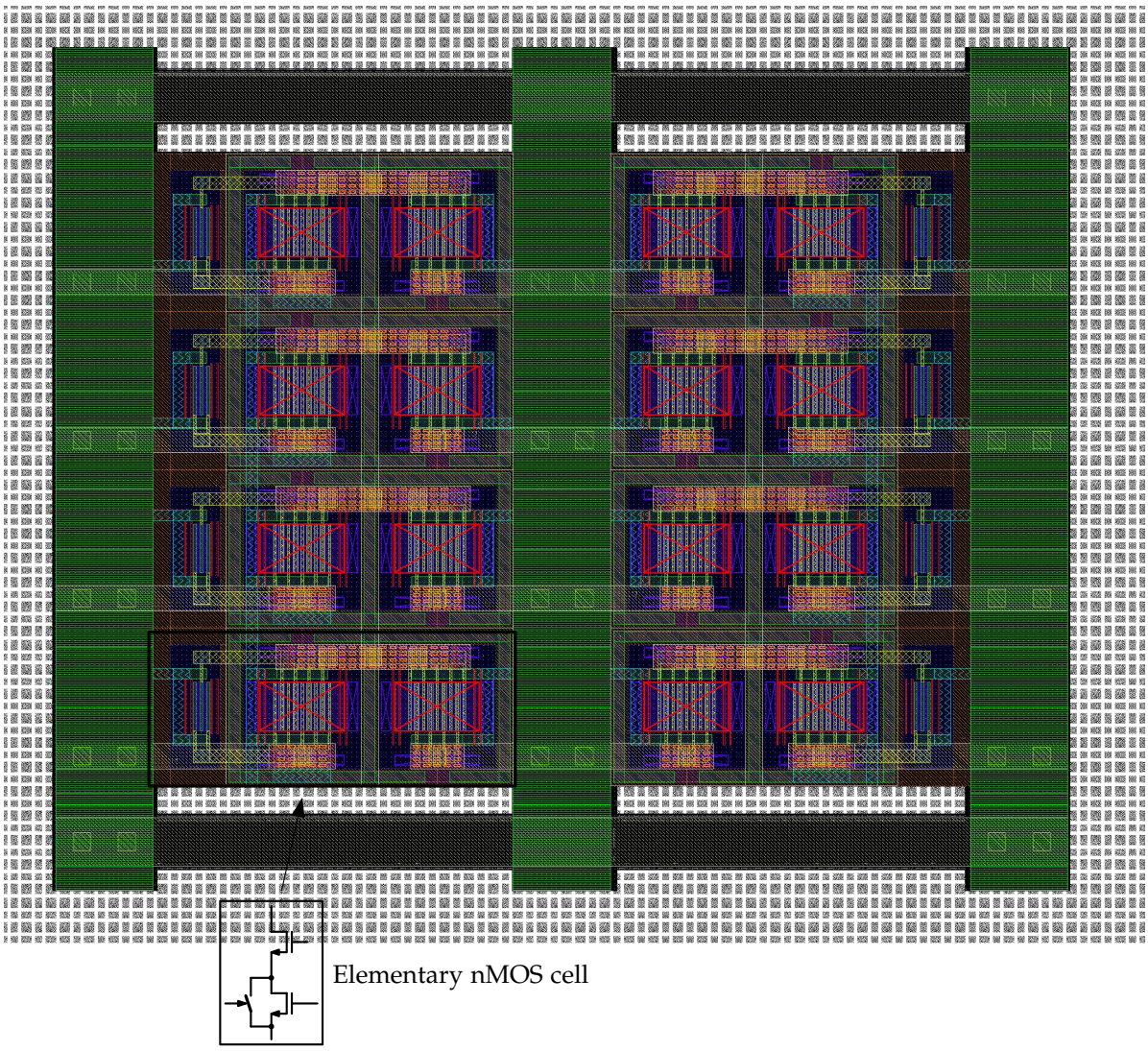


Figure 87: array of nMOS cells.

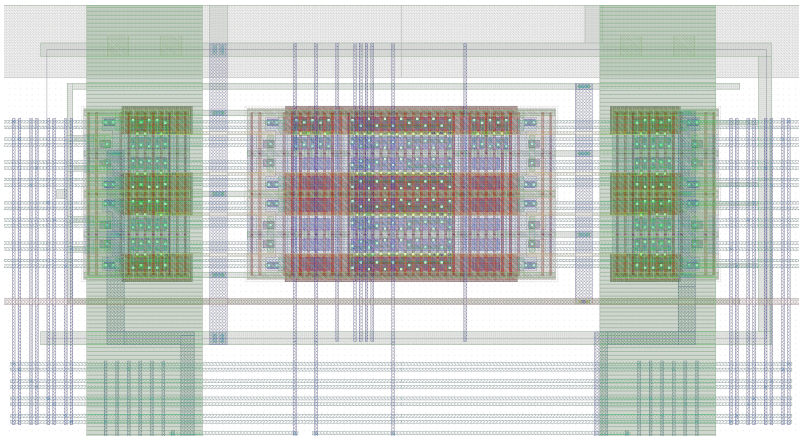


Figure 88: layout of the digital interface, responsible for the gain settings and the shutdown of the device.

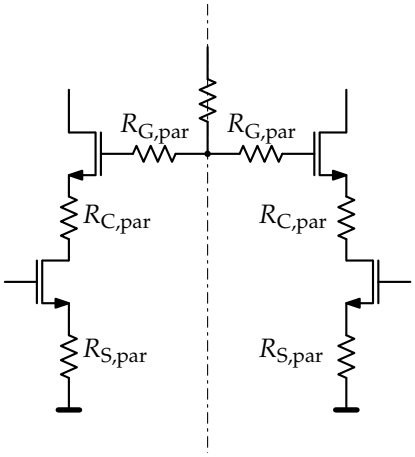


Figure 89: the layout parasitic resistances due to the connections; the common source stage is now degenerated for the presence of the non zero resistance between the source and the reference ground leading to a gain reduction.

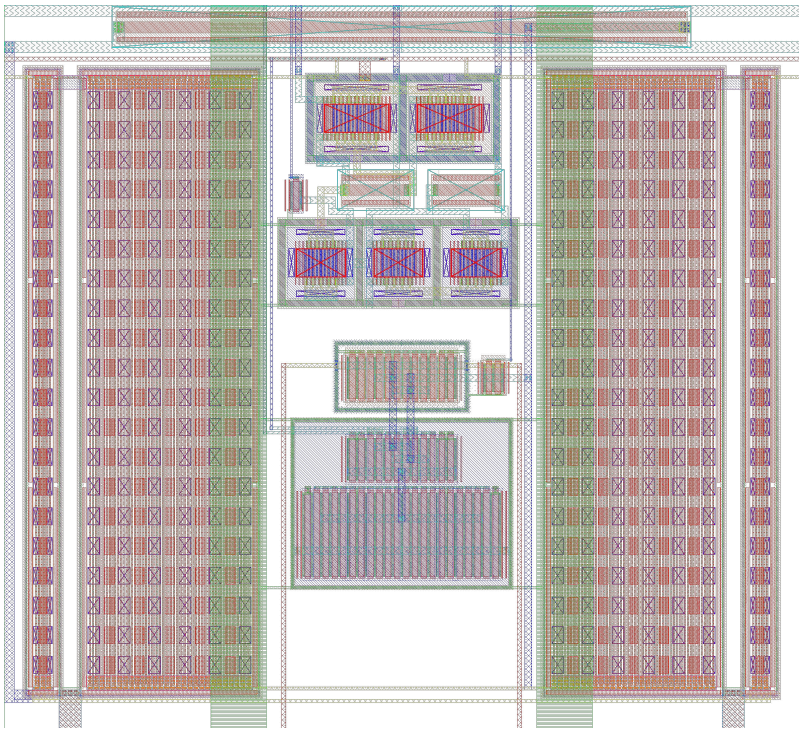


Figure 90: OTA and the common mode feedback loop circuit that, together with the biasing circuit, biases the low noise amplifier in the proper working region.

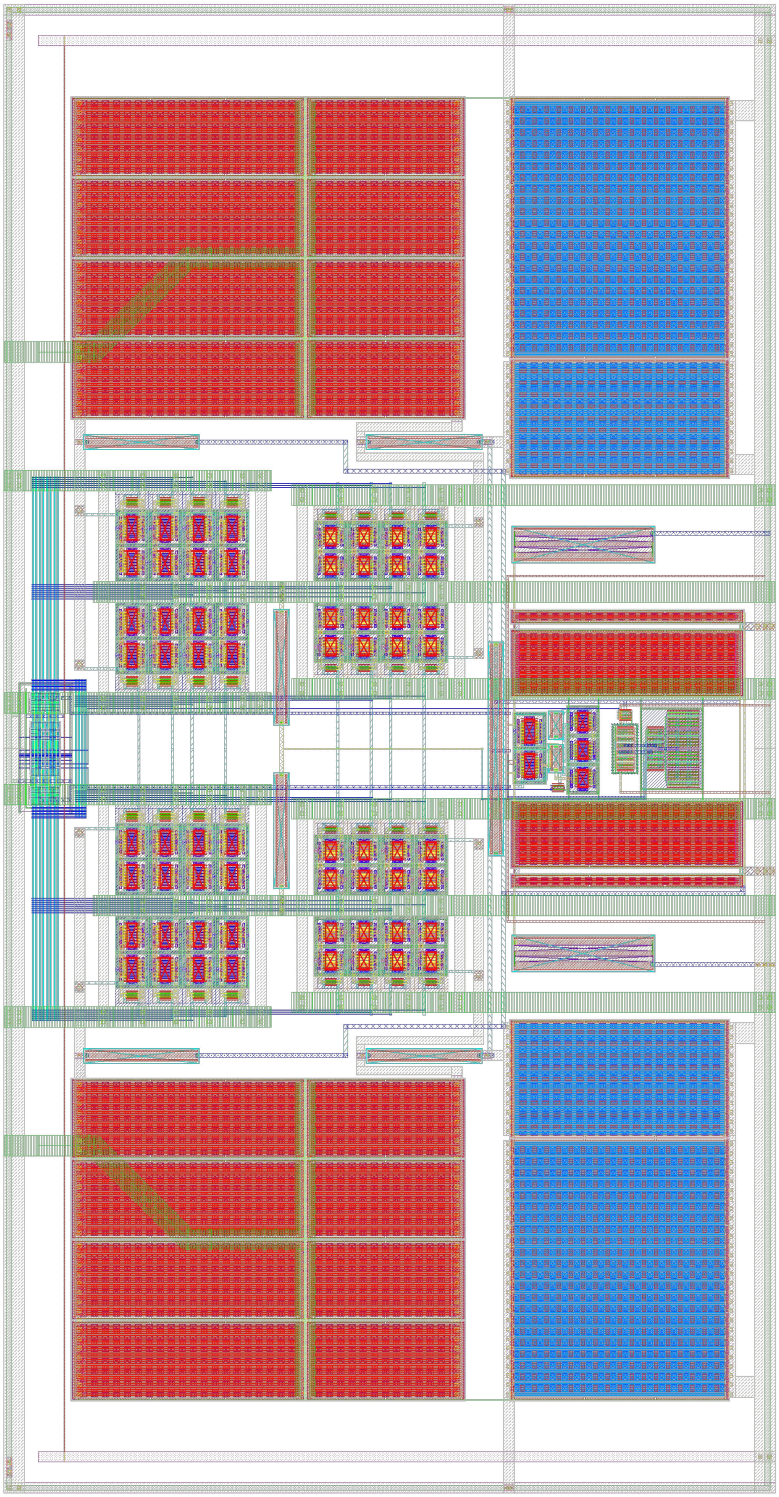


Figure 91: main layout of the new 22nm version of the LNTA.

7 CONCLUSIONS

The analysis and the design of a low noise transconductance amplifier has been here described. To implement a variable gain, multiple identical amplifier devices have been used to reduce the power consumption at low gain configurations. A new biasing circuit and a new common mode feedback loop has been designed and a preliminary version of layout for the entire amplifier has been carried on.

The simulations have shown that the amplifier has similar performances compared to the version really implemented in the Bluetooth radio and it is then, fully compatible for a use in a future version of the receiver.

Table 16 summarizes all the post layout performances, which really fulfil the targets of table 7.

Table 16: main results parameters for the new LNTA design after parasitics extraction at environment temperature.

$G_{\text{ctrl, dec}}$	I_{DC}[µA]	P_{DC}[µW]	G_{dm}[mS]	S_{11}[dB10]	NF_{11}[dB10]	NF_{min}[dB10]
1	167	151	0,72	−13,0	9,74	9,68
2	262	236	1,45	−13,1	7,14	7,14
3	358	322	2,18	−13,2	6,04	6,03
4	454	408	2,92	−13,3	5,39	5,37
5	549	493	3,66	−13,4	5,01	4,96
6	644	579	4,40	−13,6	4,71	4,63
7	739	665	5,15	−13,7	4,50	4,39
8	834	751	5,91	−13,9	4,32	4,19

Next improvements might involve the following topics:

- modify the main bias current generator used to provide the reference currents to the low noise amplifier and the mixer; such circuit is fully configurable hence different current values can be used. The goal is to further decrease the power consumption hence a new version of it is needed;
- optimize the layout for what concern the net traces; there are some discrepancies found between the pre-layout and post-layout simulations, thus a more careful arrangement is also needed.

The research work has shown that less power hungry receiver architectures do exist, hence it might worth for further investigations in a future projects.

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