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A study to improve the performance of an automotive LED current sense amplifier

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To everyone who thought all this was possible

I surely did not

Abstract

Although they're not a novelty, LEDs have become the standard for automotive lighting just in the last few years. In order to get consistent light intensity these devices need to be driven with a constant current, and in order to do so, an LED driver is used.

The accuracy and precision of LED drivers depend on the current measurement that closes the feedback loop and ensures the correct functioning of the system.

Process variation and environmental conditions might affect the measurement, and therefore ruin the driver performance.

Infineon uses various methods to ensure their chips are less and less affected by these factors, ensuring a stable and reliable product.

The scope of this thesis is to assess methods that can be viably used in order to improve performances, increase yield and possibly keep the production costs the same.

Thanks to Infineon, typical design steps are accompanied by laboratory testing in order to validate and troubleshoot various hypothesis on how to improve the current sensing performances.

Contents

Chapter 1

Introduction

The focus of this thesis is to improve performances of a current sense circuit in an integrated circuit used for automotive LED lighting while maintaining production costs contained.

The IC interfaces with a DC-DC converter controlling output current to get a constant output power and light intensity emitted by the load. With devices like LEDs current control is much more accurate than voltage control due to the exponential I/V curve that is typical of these components.

Moreover, a small variation between devices or variation of operating temperature could result in a drastically different light emitted by two of the same LEDs if the controlled quantity is voltage rather than current.

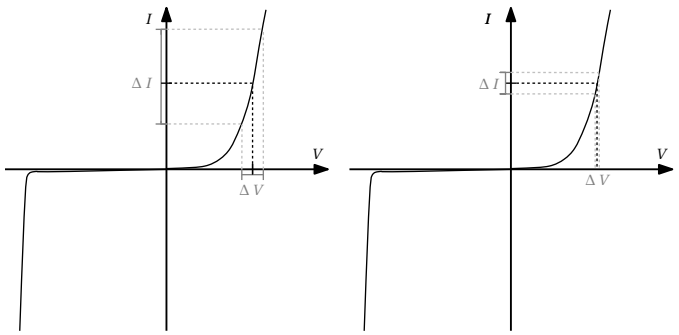


Figure 1.1: Possible effects of errors in voltage control of an LED (left) and of current control (right)

Nevertheless, current control must be precise, accurate and impervious to operating conditions variation (such as temperature) in order to ensure consistent lighting, especially in the very harsh environment in which these chips must function.

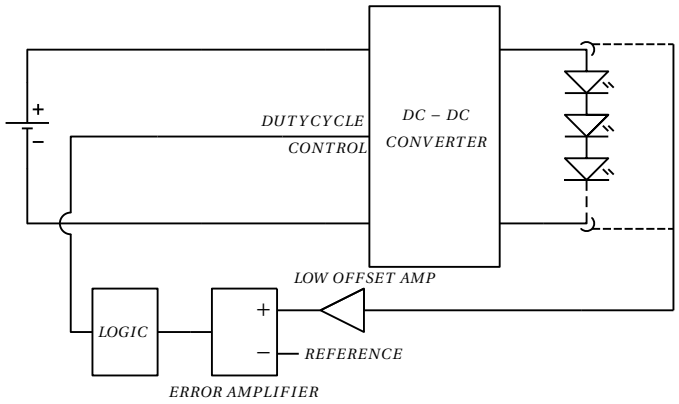


Figure 1.2: Block diagram of a generic LED driving circuit[2]

Automotive chips must sustain a wide range of operating temperatures to survive cold winters and the heat caused both by the weather and the vehicle operation, they also need to be very robust since they are subjected to a very electrically noisy environment that could compromise the correct operation.

1 Chip Overview

A block diagram of a dual channel version of the chip in analysis is reported below. The portion inside the square is the one relevant to this study and comprehends the current sense amplifier, the required circuitry to translate the voltage V_{SET} to the desired regulated output current and an error amplifier that compares the outputs of the two blocks.

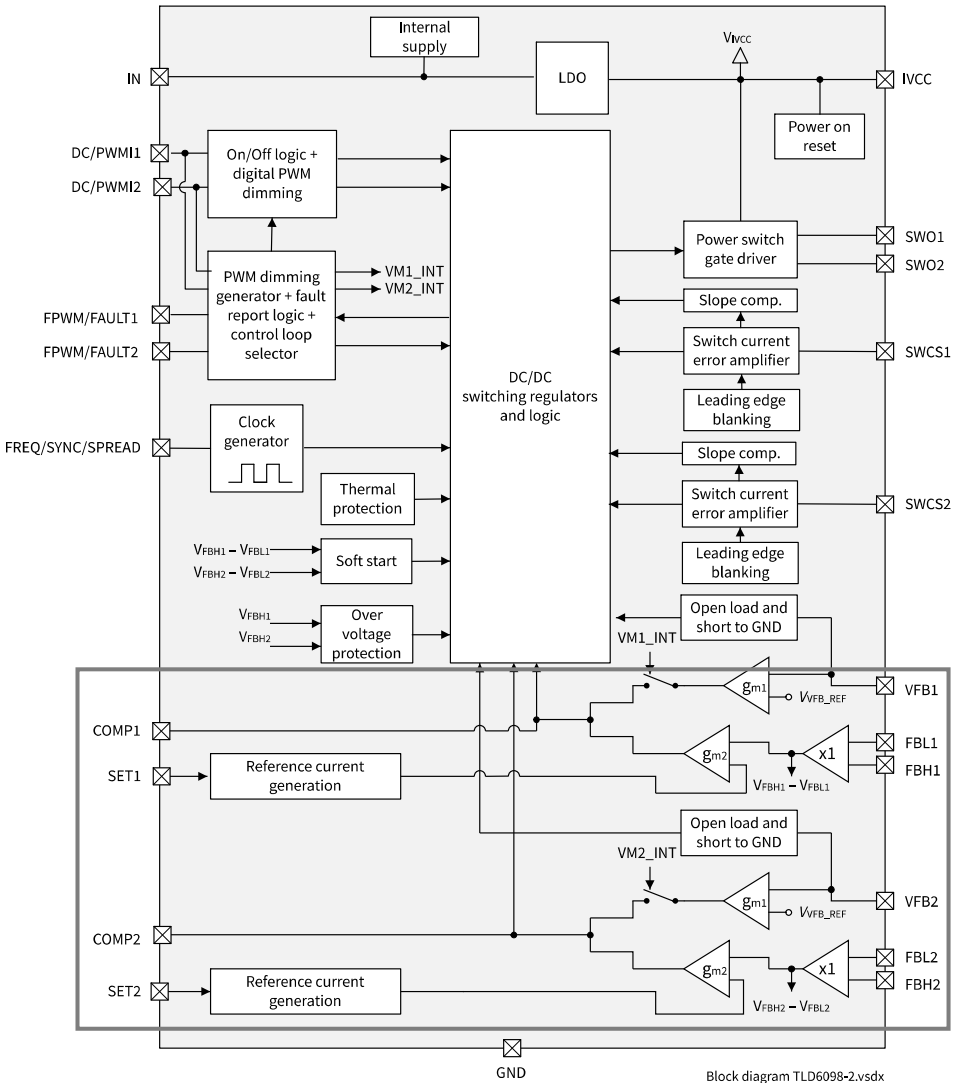


Figure 1.3: Block diagram of TLD 6098 dual channel

The current sensor circuit needs to satisfy the following requirements:

- Wide input voltage range (0-58V)
- Provide high accuracy of the LED current
- Sense reverse currents
- Measure and amplify consistently at temperatures ranging from -40°C to 150°C

These requirements highlight the necessity of a very accurate and precise differential amplifier that is impervious to high swings of common mode voltage.

The already existing amplifier consists in a cascode OTA which output current is fed back to two resistor at the input as in the schematic below. The same current is mirrored to an output resistor. The ratio between output and input resistors sets the voltage gain.

The circuit can function in two different operative modes:

- **Low Side operation:** when the voltage at the input pins FBH and FBL is lower than the internal supply voltage V_{DD}
- **High Side operation:** when the voltage at the input pins FBH and FBL is lower than the internal supply voltage V_{DD}

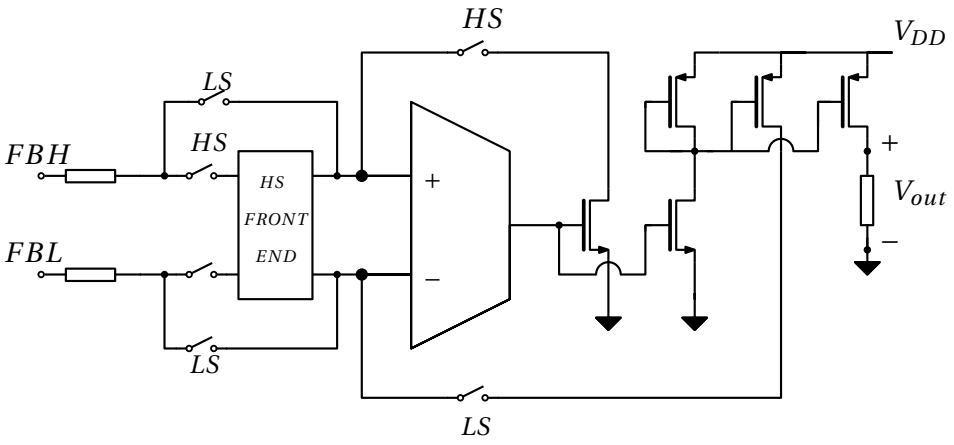


Figure 1.4: Conceptual diagram of the current sense amplifier.

If any of the input voltages are higher than the supply voltage (High Side conditions) the circuit is configured accordingly to shift the input voltage to a level that can be processed by the OTA via the High Side front end, and the feedback network is switched accordingly by sinking the feedback current instead of supplying it as in Low Side conditions.

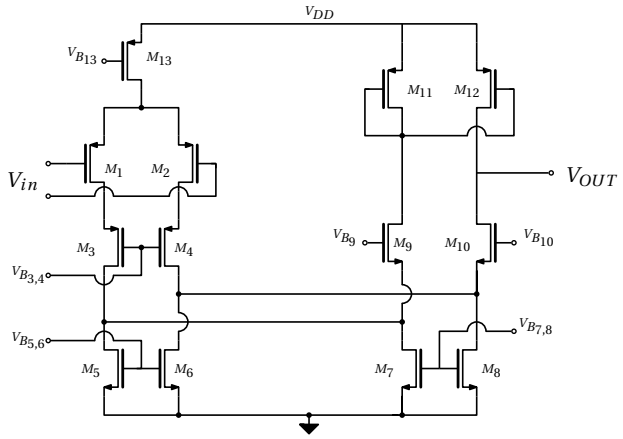


Figure 1.5: Conceptual schematic of the folded cascode OTA implemented in the circuit. This topology allows for high gain and high output voltage swing

2 Figures of merit

This study aims to improve the performances of an existing current sensing amplifier, where the targets are:

- Better accuracy
- Better precision
- Better temperature stability

Despite being used interchangeably colloquially, accuracy and precision have two different meanings.

Accuracy measures in average how close is the acquired data to the desired value, therefore measuring systematic errors, while precision measures how far apart are the single data points between each other, taking into account random errors.

In the case of this study, all the errors introduced throughout the circuit can be summarized by a single measurement: offset. In order to derive accuracy and precision a statistical analysis of multiple devices is required, distinguishing stochastic errors such as mismatch of components and overall process variations from systematic errors introduced by the design.

Since silicon properties can change at different temperatures, both precision and accuracy are temperature dependent and have to be analyzed across the whole operating range.

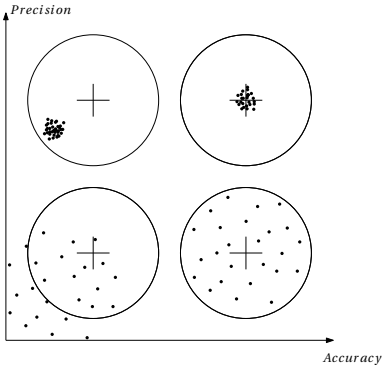


Figure 1.6: Difference between precision and accuracy

3 Offset

In applications where input signals are of the order of of millivolts and high precision amplification is required such as the current sensing amplifier subject of this study, a simple operational amplifier cannot suffice.

In low frequency applications, input referred offset has the most degrading impact on the amplifiers performances.

Offset is caused by errors that could occur throughout the amplifier but can be all traced back to the input of the amplifier. In generic operational amplifiers input referred offset can be of the order of millivolts or even tens of millivolts: much higher than required accuracy of the current sensing amplifier in analysis.

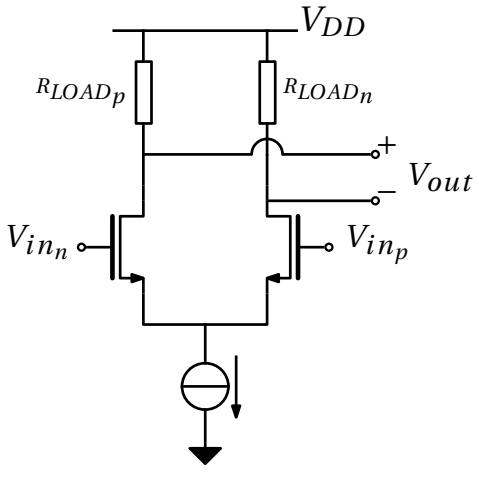


Figure 1.7: Generic schematic of a differential couple

In an operational amplifier the most common source of mismatch is the input differential pair. This structure requires matching of both the amplifier transistors and their relative loads.

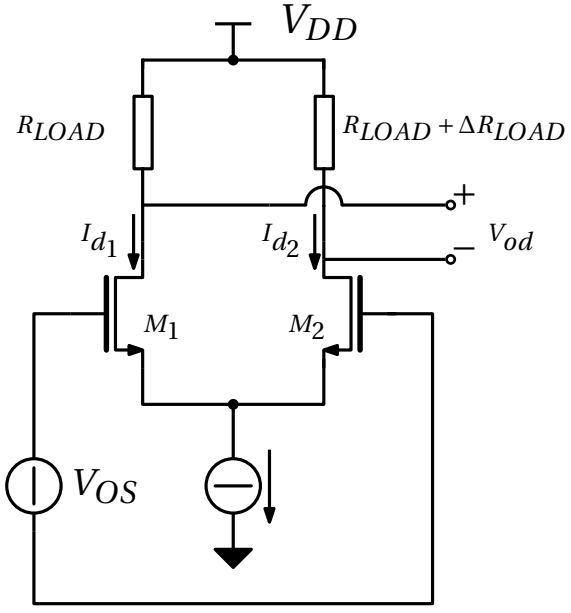
If these conditions are not matched, offset will be originated at the very start of the gain structure, with a very high probability of resulting in the most prominent error source.

In a differential couple the main sources of offset can be found in:

- Mismatch of load resistors R_{LOAD}
- Mismatch of current factor β
- mismatch in threshold voltage V_t

A mismatch between load resistors results in a variation of drain current where $\frac{I_{d_1}}{I_{d_2}} \approx 1 + \frac{\Delta I_D}{I_D}$. Since it is a small variation, ΔI_D can be approximated as $g_m V_{OS}$ relating the variation in resistance to input referred offset, obtaining

$$V_{OS} = \frac{\Delta R/R}{g_m/I_D} \tag{1.1}$$



A similar analysis can be carried out for β mismatch and V_t mismatch, obtaining the dependence of input referred offset V_{OS} from these factors.

$$V_{OS} = \Delta V_t + \Big(\frac{\Delta\beta}{\beta} + \frac{\Delta R}{R}\Big)\frac{I_D}{g_m} \tag{1.2}$$

This analysis highlights the fact that despite having origin all throughout the amplifier, offset can be input referred, and corresponds with the differential input voltage required to obtain a zero output voltage. It can be modeled as a series voltage generator in series with the input terminals of an offset free amplifier.

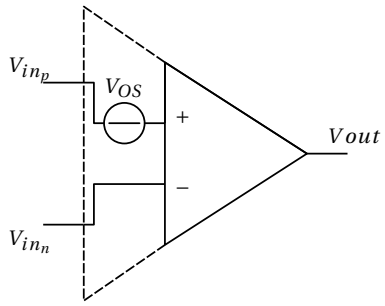


Figure 1.8: Model of an operational amplifier consisting in an offset free amplifier and a series input offset voltage generator

Chapter 2

Offset reduction methods

In an amplifier, offset is usually measured as input referred offset, consisting in the differential input voltage necessary to obtain a null output voltage.

With a statistical analysis on a large population it's possible to gauge the amount of input referred offset caused by systematic errors, found in the mean value of input referred offset, and stochastic errors, found in its standard variation.

Systematic offset should be removed by perfecting the design, but it's not always straight forward. For instance, systematic errors can be zero at a certain temperature, but as soon as this condition changes, temperature dependent properties of silicon will introduce errors that contribute to input referred offset. The errors introduced throughout the amplifier can be lowered by a more refined design. In an integrated circuit ultimately a balance between complexity, occupied area and performance has to be struck.

Stochastic offset is caused by random imperfections of the devices during the manufacturing process and therefore cannot be avoided. This doesn't mean that there's no way of reducing the effects of random offset.

There are methods that a designer can implement to reduce stochastic offset, such as:

- Improve matching
- Trimming
- Offset nulling topologies
- Reduce physical stresses

1 Matching

Offset is mainly caused by mismatches between transistors[1]. In some topologies, especially ones that have transfer functions that rely on ratios between two or more components in the circuit (differential couples, current mirrors etc..), minimizing the error between these component is a key factor.

In order to achieve so, two general methods can be used.

1.1 Layout methods

The first method acts on the layout of the chip. Since there might be a drift of the manufacturing process between different parts of a silicon wafer, matching can be improved by keeping critical components next to each other.

Layout symmetry can be used to reduce these effects as in the common centroid technique and inter digitization technique[5].

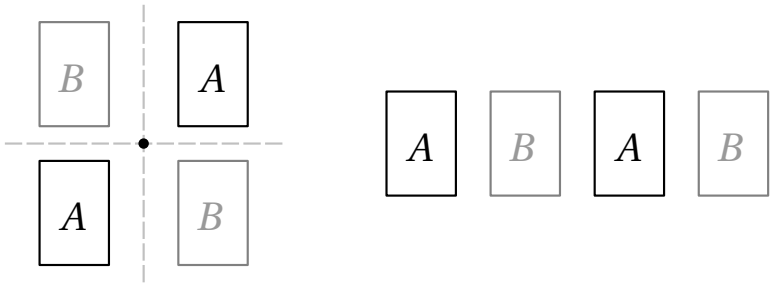


Figure 2.1: Example of a common centroid layout (left) and a inter digitization layout (right)

Furthermore, ratios between critical component can be better controlled by using multiple instances of the same device connected differently (e.g. connecting resistances in parallel) to obtain the desired values more accurately.

This not only minimizes the process variations, but also ensures that the various components undergo similar stresses[2] such that their ratios can be kept

[1] Mismatches include differences in components dimensions, doping concentrations, oxide thickness and other parameters used in the technology

[2] Temperature gradients during operation, physical stresses induced by bonding and packaging

1.2 Increasing dimensions

Each technology and production process has its own precision and accuracy. These property of the production process introduces mismatches in components dimensions, and therefore offset.

To reduce these effects it's possible to increase the dimensions of critical components that require matching, reducing the relative errors introduced by the production process with regards to the overall dimensions, and reduce the induced offset.

As in the previous chapter, the differential couple can be analyzed to gauge how random variations affect the input referred offset.

From equation 1.2 it's possible to calculate the input referred offset standard variation:

$$\sigma_{V_{OS}} = \sqrt{\sigma^2_{\Delta V_t} + \left(\sigma^2_{\frac{\Delta\beta}{\beta}} + \sigma^2_{\frac{\Delta R}{R}}\right)\left(\frac{I_D}{g_m}\right)^2} \tag{2.1}$$

In particular the parameter for transistors are

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}}, \quad \sigma_{\frac{\Delta\beta}{\beta}} = \frac{A_{\Delta\beta/\beta}}{\sqrt{WL}} \tag{2.2}$$

Where A_{V_t} and $A_{\Delta\beta/\beta}$ are technology parameters[3]. The equation above highlights the dependence of these parameters from the device area and the technology used.

2 Trimming

Trimming is a method that can be used in many part of a circuit to remove stochastic errors and bring parameters inside the required range.

The most simple trimming procedure consists in the actual cutting of resistors and capacitors with a laser beam, modifying their shape until the correct value is obtained.

Similar methods can be used to enable or disable modular structures (e.g. parallel current mirrors) implemented in the chip in order to bring the parameter controlled by them closer to the ideal value.

Usually the trimming procedure is performed on the wafer for each chip, and consists in the measurement of the sensitive parameters corresponding with each possible configuration of the modular structure affecting it, determining what combination is closer to the target.

[3]Usually measured in $mV/\mu m$ or $\%/\mu m$

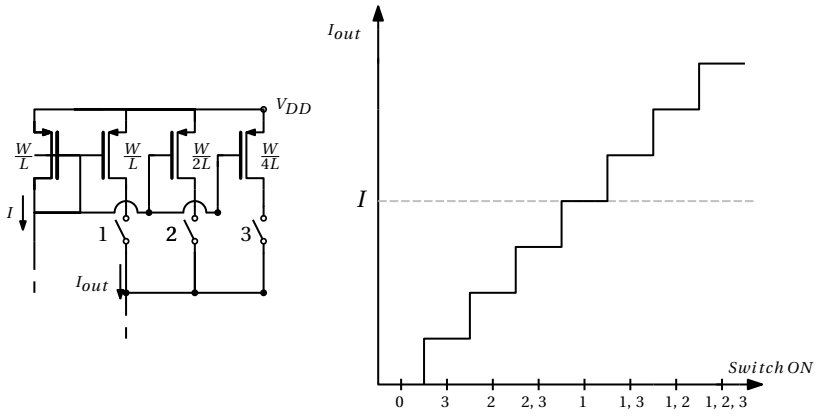


Figure 2.2: Structure of a trimmable current mirror (left), Achievable current values depending on the trimming configuration (right)

Due to the nature of this procedure, the conditions in which the trimming has been performed play a key role on how the chip will perform. Temperature and other factors such as packaging and bonding induced stresses could affect the trimmed values, degrading performances and potentially resulting in an out of spec chip. If these variations introduce a systematic error, it can be factored in the selection of the target value, improving the trimming performances.

Although the trimming procedure increases the yield making up for the increased costs of production and is a valuable step in the production of a chip, it requires a larger chip area for the modular structures, but most importantly it's quite costly because of the time spent to perform the procedure.

For this reason trimming should be used sparingly and designer should prefer other solutions if possible.

3 Offset nulling topologies

Offset nulling topologies are types of circuits that remove offset while the chip is running. Two of these have been analyzed for use in the current sensing amplifier because of their ability to reduce offset, but most importantly, their ability to do it without interrupting the amplifier operation.

3.1 Chopper amplifier

The first method is the chopper amplifier. The working principle of this topology is to modulate the input signal with a square wave, inverting the signal for half of its period at the amplifier input. The modulated signal gets amplified by the amplifier, adding its offset. At the output, the amplified signal and added offset get modulated again by the same input square wave, resulting in an demodulated signal with an added square wave which amplitude is the same of the amplified input referred offset, but the mean is null.

After the demodulator the signal can be filtered to reduce the contribution introduced by the modulation of the amplifier's offset.

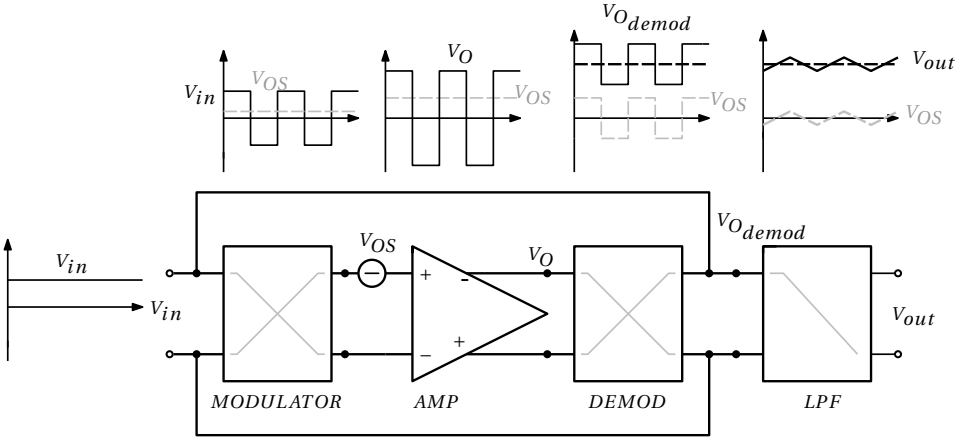


Figure 2.3: Block schematic of a Chopper amplifier

3.2 Ping Pong Auto Zero

An auto-zeroed amplifier consists in amplifier that works in two phases: a first phase, when the amplifier is disconnected from the input and measures its intrinsic offset, and a second phase, where the amplifier amplifies the input voltage, and removes the value previously measured in order to remove the offset. The working principle of a Ping Pong auto-zero amplifier is to use two Auto Zeroed amplifiers that work in opposite phases. This allows to have a continuous amplification of the input signal while using an auto-zeroed topology.

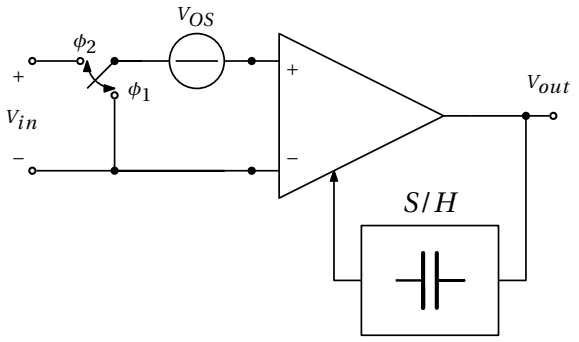


Figure 2.4: schematic of an auto zero amplifier

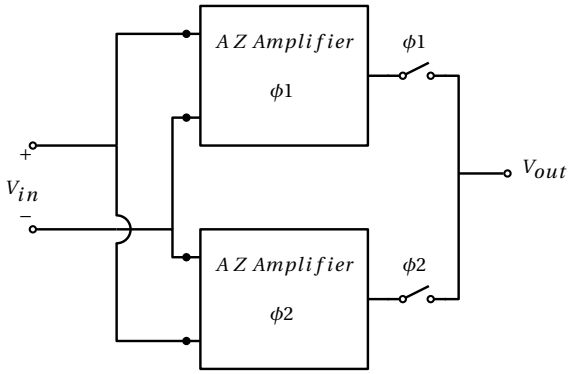


Figure 2.5: Block diagram of a Ping Pong Auto Zero amplifier

Whilst all the other methodologies have been implemented in the chip in analysis, the aforementioned nulling topologies need further investigation.

In particular, a chopper amplifier has already been designed, and its performances can be assessed in a testchip that has been manufactured.

The ping pong auto zero topology performances and footprint need to be evaluated in a simulation environment and compared with the results obtained with the chopper topology.

Chapter 3

Chopper Amplifier

As of the beginning of this thesis, Infineon had already implemented a chopper topology in the current sense [1] with the intent of improving the current sense circuit performances.

The aim of this chapter is to summarize the design choices and report the simulation results obtained in order to use them as a frame of reference for further analysis.

The results reported in this chapter are simulation results of the current sensing circuit isolated from the rest of the circuit. Some other known property of the circuit (e.g. temperature dependence of bandgap voltage reference) have been taken into account in the testbench used.

These result cannot be compared with on chip measurements reported in chapter 6, but should be compared with other simulation results that use a similar testbench.

1 Starting point

Before analyzing the the chopper amplifier it's necessary to establish a baseline of the already existing structure of the current sensing amplifier on which the chopper topology has been implemented.

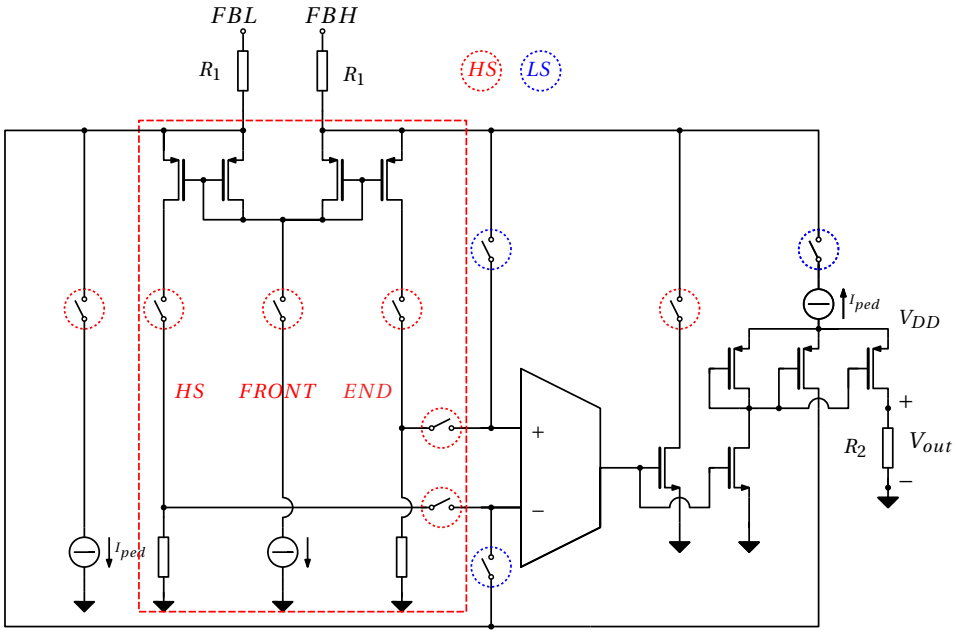


Figure 3.1: Current sensing amplifier

In figure 3.1 a more accurate schematic of the current sense amplifier, which output voltage can be determined as

$$V_{out} = \left(V_{FBH} - V_{FBL}\right)\frac{R_2}{R_1} + I_{ped}R_2 \tag{3.1}$$

The pedestal current I_{ped} is a constant current used to allow the amplifier to measure inverse currents. It is injected in the FBH node in LS configuration or absorbed from FBL in HS configuration and therefore mirrored on the output resistor R_2.

The HS front end plays a key factor in the circuit. It consists in a level shifter for the input signal that uses a common gate stage to buffer the input current, some high voltage switches and some resistors to convert the buffered current in input voltage for the OTA.

This structure has a high potential impact on the input referred offset of the amplifier since it's the first gain stage of the HS signal chain and requires matching in order to reduce it.

A Monte Carlo simulation of the original circuit has been performed, with the goal of assessing the input referred offset mean value and standard deviation across the required temperature range and both in HS and LS configurations.

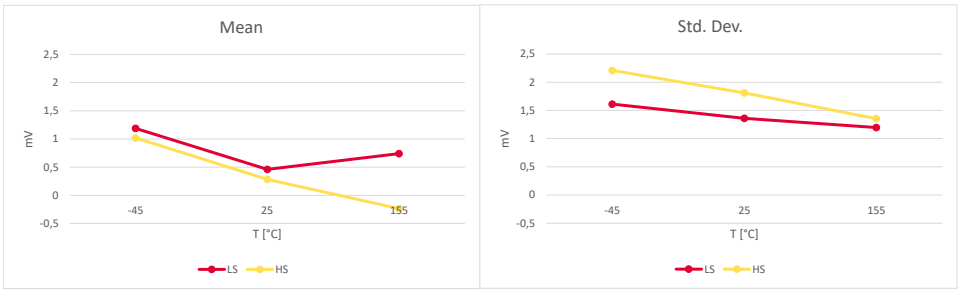


Figure 3.2: Results of a Monte Carlo simulation of the original circuit showing the mean value (mean) and standard deviation (sigma).

The simulation was performed on a sample size of 300 devices. The results obtained with this circuit configuration differ between HS and LS standard deviation, highlighting the importance of matching in the HS front end structure.

A non null mean could lead to think that a non stochastic error is present in the circuit, but since the standard deviation is significantly bigger than the mean, more effort should be directed at reducing the latter rather than the former.

Moreover, these results don't factor in any trimming procedure, errors introduced by packaging or layout method to reduce offset, and serve the purpose of gauging the performances of the amplifier itself, without much correlation with silicon performances.

2 Design

The purpose of this paragraph is not to explain the design of the chopper amplifier in detail as it has been already reported in another thesis[1] but rather to give an overview of how the chopper topology has been implemented and what options has been rendered available to test in the testchip analyzed in chapter 6.

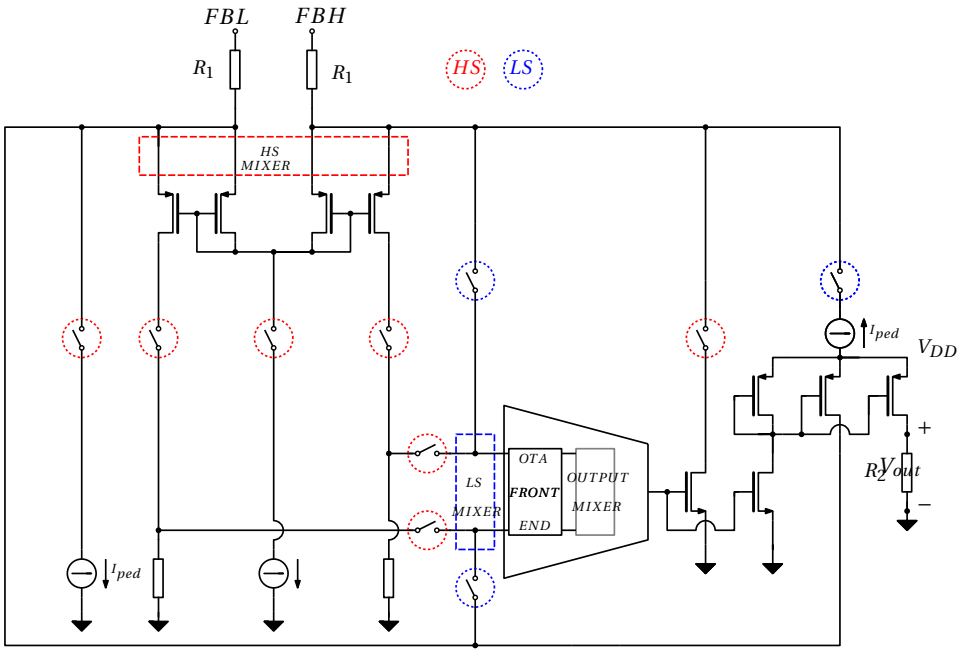


Figure 3.3: Current sensing amplifier with chopper implementation

In order to incorporate the HS front end in the chopped portion of the amplifier three mixers have been introduced. Two of them are dedicated to the inputs of each configuration as in figure 3.3, while the third is the output mixer and is shared between the two configurations placed after the input differential couple before the cascode stage of the OTA.

In order to drive the HS mixer, the non overlapping clock needs to pass through a high voltage level shifter has been implemented. This structure uses high voltage components that occupy a large area resulting in a possible lower yield.

3 Results

The same Monte Carlo simulation has been performed on the chopper amplifier giving the following results:

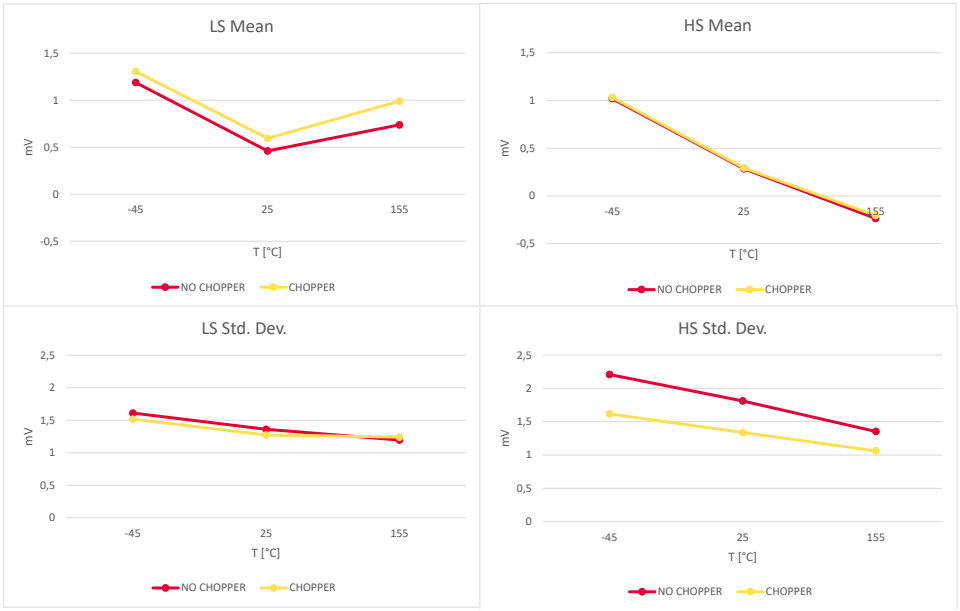


Figure 3.4: Results of a Monte Carlo simulation of the chopper amplifier circuit compared to results of the original circuit.

The most significant change introduced by the chopper amplifier can be seen in the HS standard deviation, while LS performances are very similar to the previous version of the circuit. It can also be noted that with the chopper amplifier HS standard deviation is brought to LS levels.

Since the difference between HS and LS is the inclusion of the HS front end in the chopped region, the previous supposition that the HS front end can be a major player in the amplifier's offset and mismatch finds evidence in this data.

Ideally a chopper amplifier should remove any offset in the chopped region, apart from some residual ripple and non idealities such as clock feed-through and charge injection. The residual standard deviation for both configurations of the circuit has to be found outside of the chopped area.

This investigation will be carried out in chapter 5 and 6.

Chapter 4

Auto Zero

Other offset nulling topologies are investigated to gauge whether it's possible to obtain better performances or lower area impact compared to the chopper amplifier.

Auto Zero amplifiers, as explained briefly in chapter 2, operate in 2 phases: the first where the offset is sampled, and a second one, when the input signal is amplified and the offset is removed.

This operation implies a period where the input is disconnected from the amplifier, interfering with the detection of faults.

Auto Zero amplifiers can be used to create continuous time amplifiers such as the Continuous Time Auto Zero (CTAZ) amplifier and the Ping Pong Auto Zero (PPAZ) amplifier. Both of these topologies are effective at reducing the input referred offset, but work in a different fashion.

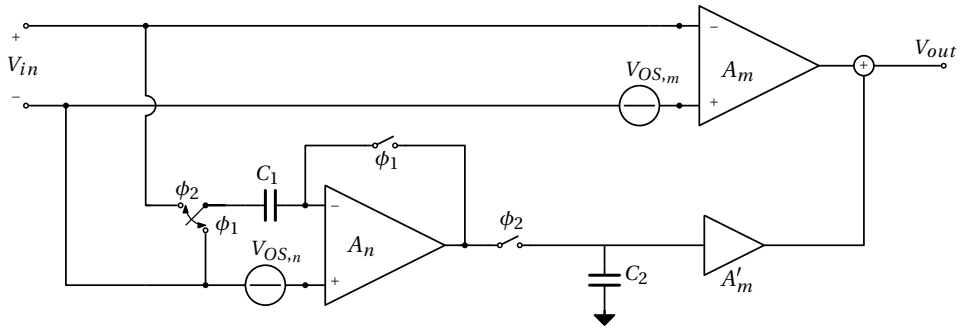


Figure 4.1: Schematic of a Continuous Time Auto Zero amplifier

CTAZ amplifiers use an auto zero amplifier as an auxiliary amplifier put in parallel with a continuous time amplifier. In the configuration illustrated in Figure 4.1 the residual offset $V_{os,res}$ can be calculated as:

$$V_{os,res} = -\frac{A_m V_{os,m}}{A'_m A_m} - \frac{V_{os,n}}{A_n} + \frac{q_{inj,1}}{C_1} + \delta \frac{A'_m}{A_n A'_m} \frac{q_{inj,2}}{C_2} \tag{4.1}$$

where $q_{inj,1,2}$ is the injected charge in capacitor $C_{1,2}$ by the switches connected to them, and δ is the duty cycle $\phi_1/(\phi_1 + \phi_2)$

Ignoring the non idealities in the circuit, the maximum theoretical input referred offset reduction granted by this topology is $A_{ol_{AZ}}/A_{ol_{CT}}$.

The existing amplifier has an open loop gain $A_{ol_{CT}} \approx 90dB$ and would require a very large gain (and occupied area) in order to significantly reduce the input referred offset.

1 Ping Pong Auto Zero

Ping Pong Auto Zero amplifiers instead use two identical Auto Zero amplifiers in parallel working in opposite phases. In this way, one can be in the offset cancelling phase while the other is amplifying the input signal and vice versa, ensuring continuous time amplification.

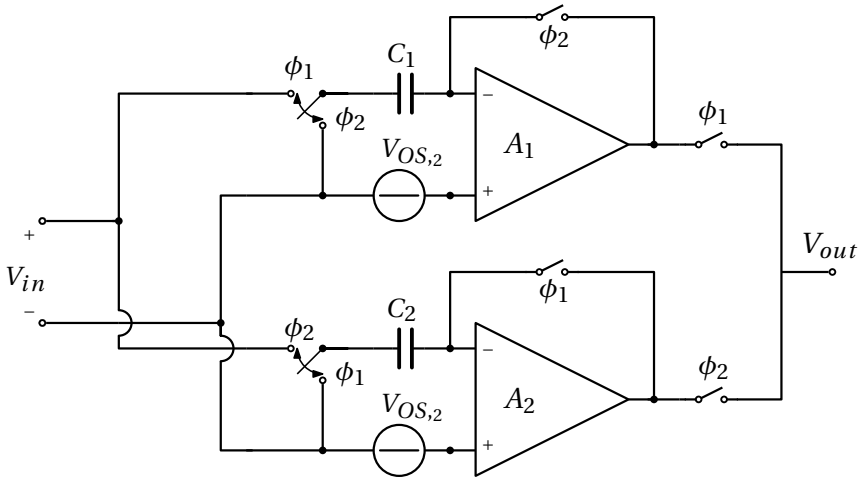


Figure 4.2: schematic of an auto zero amplifier

Ping Pong Auto Zero provide the same offset reduction of a single Auto Zero amplifier. An implementation that uses the unitary feedback configuration as illustrated in Figure 4.2 can achieve the residual offset

$$V_{os,res} = \frac{V_{os_{1,2}}}{A_{1,2}} \frac{q_{inj_{1,2}}}{C_{1,2}} \tag{4.2}$$

Given the results of the chopper amplifier simulations it's clear that the HS front end must be inside the auto zero unitary feedback loop. This requires the same high voltage level shifter required for the chopper HS mixer that will occupy a large area. Moreover, the Ping Pong Auto Zero requires a secondary amplifier which will occupy even more die area.

The use of this topology won't allow to incorporate the output mirrors and therefore it will not improve significantly the performances.

Because the Ping Pong Auto Zero topology cannot improve performances and require a larger area in this particular amplifier, the chopper solution seems the most advantageous of the offset nulling topologies.

These considerations cannot be generalised to other amplifiers since the prerequisite of this project is to keep intact most of the existing circuitry and adding something on top to mitigate the offset in order to limit the production costs.

If a new amplifier was to be designed from the ground up, any of the offset nulling topologies could be used and inserted in a suitable design.

Chapter 5

Investigating offset sources

The offset reduction methods proposed in previous chapters are effective, but leave some residual input referred offset.

More investigation is needed in order to understand the source of the residual offset and evaluate whether the chopper solution can be replaced with a better solution.

The identified improvement areas are:

- High Side front end
- Output pMOS and nMOS mirrors
- Pedestal current generator

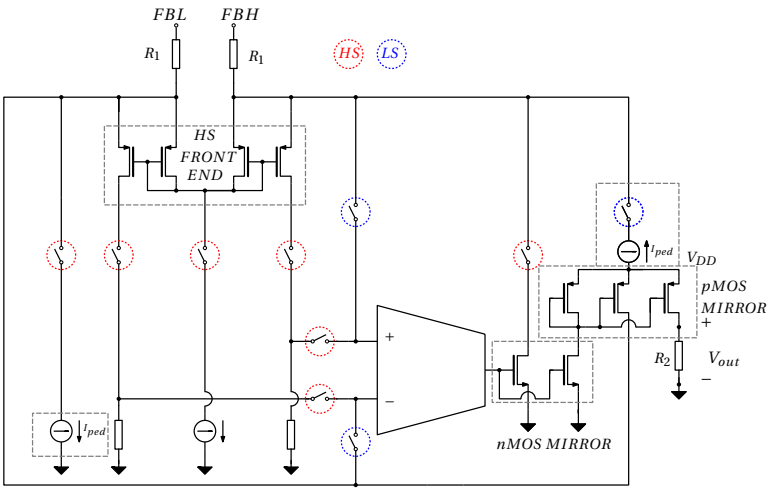


Figure 5.1: Current sense circuit portions identified for improvement

1 High Side front end

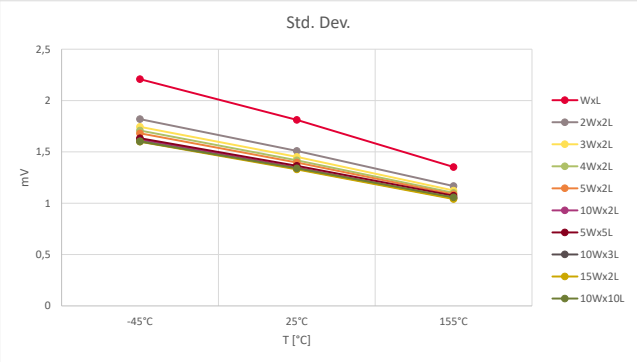
The results from the chopper amplifier highlight that one of the main sources of offset in HS configuration is the HS front end.

An investigation is needed to gauge whether offset can be significantly lowered by increasing the dimensions of the double pair of transistors that act as current buffers.

These modifications could result in a similar reduction of offset obtained with an offset nulling topology whilst occupying less area.

A Monte Carlo simulation has been carried out with various transistors dimensions monitoring the HS standard deviation. The original dimensions WxL were taken as a starting point, and each variation has been derived from WxL as a multiplication of each dimensions

	HS Std. Dev		
	-45°C	25°C	155°C
WxL	2,208	1,811	1,353
2Wx2L	1,819	1,51	1,167
3Wx2L	1,744	1,451	1,124
4Wx2L	1,708	1,418	1,101
5Wx2L	1,681	1,397	1,086
10Wx2L	1,622	1,348	1,053
5Wx5L	1,633	1,365	1,073
10Wx3L	1,605	1,336	1,047
15Wx2L	1,599	1,33	1,041
10Wx10L	1,601	1,34	1,057
CHOPPER	1,617	1,339	1,061



As expected, matching improves with the increase of area of the transistor, and even with an extreme increase of area ($10W$x$10L$) the measured input referred offset plateaus at the chopper amplifier's levels.

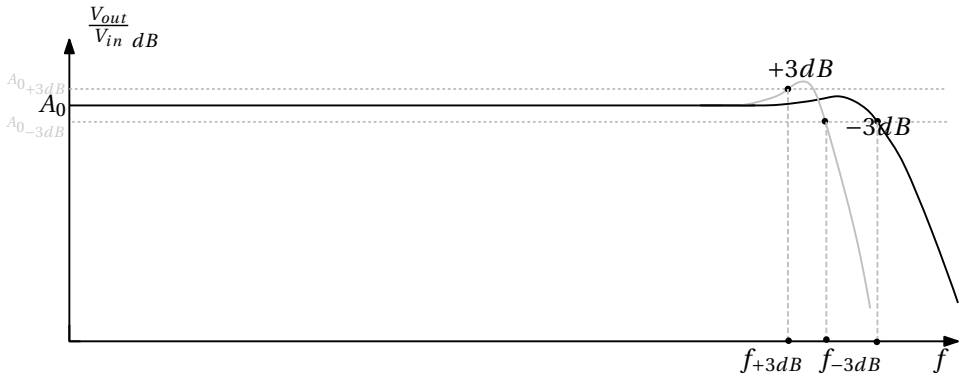
This is the confirmation that the transistors targeted with the increase of dimensions in the HS front end are responsible for the increase of offset observed in HS operation.

With a 10x ($5W$x$2L$) increase in transistor area, performances start to become indistinguishably similar to the chopper performances while occupying less area than the circuit required for the chopper implementation.

The increase of the transistors area imply an increase of their relative capacitances and a change in the amplifier's transfer function.

The increase in capacitance not only decreases the amplifiers bandwidth, but gives also rise to a resonant peak due to the interaction of poles and zeros in the transfer function.

In the following table, the f_{-3dB} and f_{+3dB} are reported along with the maximum peak amplitude of the transfer function.



	BW [MHz]		PEAK [dB]
	-3db	+3db	
WxL	18,62		14,14
2Wx2L	17,91		14,96
3Wx2L	18,3	5,24	16,1
4Wx2L	16,59	5,12	15,57
5Wx2L	17,37	4,073	17,65

Figure 5.2: Two typical behaviours of the amplifier's bandwidth, with $f_{-3_{dB}}$ and $f_{-3_{dB}}$ highlighted. If $+3dB$ bandwidth is not reported in the table the frequency response does not cross the $+3dB$ threshold (black), otherwise the frequency response crosses both thresholds (gray)

Such a large bandwidth is not necessary in order to perform the current regulation, but it's very important for fault detection. At high frequencies we're not concerned with gain accuracy, therefore if A_{peak} is reasonable, f_{-3dB} can be considered as the upper limit of the bandwidth.

The $5W$x$2L$ form factor allows for similar to chopper performances and a loss in bandwidth is $\approx 1.3MHz$ whilst the resonant peak is $+5.6dB$ from the DC gain value of $4(\approx 12dB)$. This value could be tamed by changing the value of some compensation capacitors in the design at the expenses of the amplifier's bandwidth. Since the slight overshoot is not a concern for the amplifier's stability no further changes are made.

2 Output mirrors and pedestal current generator

The current sensing circuit has an output nMOS mirror and an output pMOS mirror to close the feedback loop and drive the load that can be sources of mismatch.

An ideal current controlled current source is used to bypass these current mirror, and assess their weight on the overall sigma.

Three instances have been analyzed:

- nMOS mirror bypassed
- pMOS mirror bypassed
- Both mirror bypassed

All the analysis were made in HS and with HS front end transistors dimensions increased by 10 times (both width and length) to minimize the offset contribution by the HS front end.

	HS mean			HS Std Dev.		
	-45°C	25°C	155°C	-45°C	25°C	155°C
10Wx10L	1,022	0,2878	-0,2293	1,601	1,34	1,057
ideal nmos mirror	1,042	0,3061	-0,2148	1,451	1,221	0,9658
ideal pmos mirror	0,7536	-0,00642	-0,6102	1,323	1,112	0,8888
both ideal mirror	0,7965	0,03231	-0,5753	1,321	1,115	0,8928

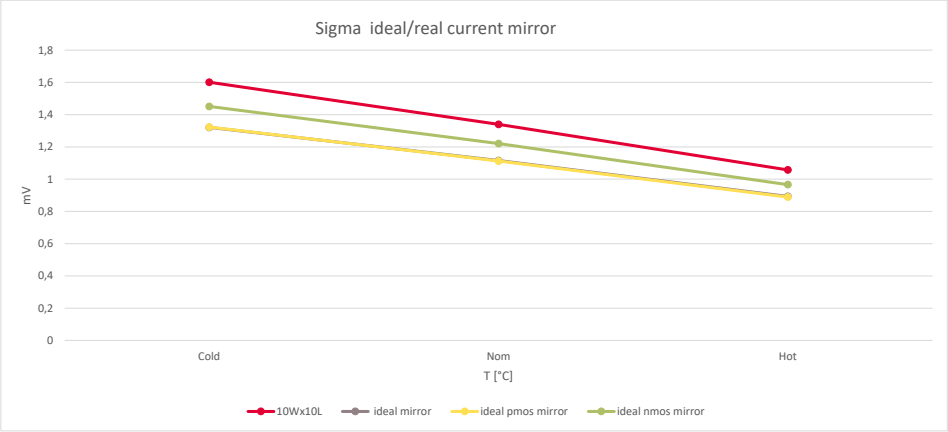


Figure 5.3: Standard deviation of the circuit with ideal output mirrors. HS front end transistor dimensions are $10W$x$10L$ for each test

The introduction of ideal output current mirrors results in a decrease of standard deviation, in particular the $pMOS$ mirror has much more impact in the standard deviation of the offset.

The $nMOS$ is much simpler than the $pMOS$ mirror, which, despite the simple representation in the conceptual schematic in Figure 5.1, is more complex to enable trimming.

The sheer amount of transistors used for the implementation of the current mirror might be the reason for the higher offset contribution.

Another possible culprit for offset generation is the pedestal current generator. This current is generated outside the amplifier, and copied on the output resistor via a cascode $pMOS$ mirror. As the previously mentioned current mirrors, this can introduce offset. Furthermore, the generator itself could be an offset source.

	HS mean			HS Std Dev.		
	-45°C	25°C	155°C	-45°C	25°C	155°C
10Wx10L	1,022	0,2878	-0,2293	1,601	1,34	1,057
ideal ped. real mirror	0,2151	0,2164	0,2421	0,8321	0,7239	0,5912
ideal ped. ideal nmos	0,256	0,2533	0,2753	0,8321	0,7329	0,5912
idedal ped. ideal pmos	-0,03282	-0,05925	-0,1201	0,793	0,6726	0,5358
ideal ped. ideal mirror	0,01008	-0,02051	-0,08519	0,6511	0,5837	0,4938

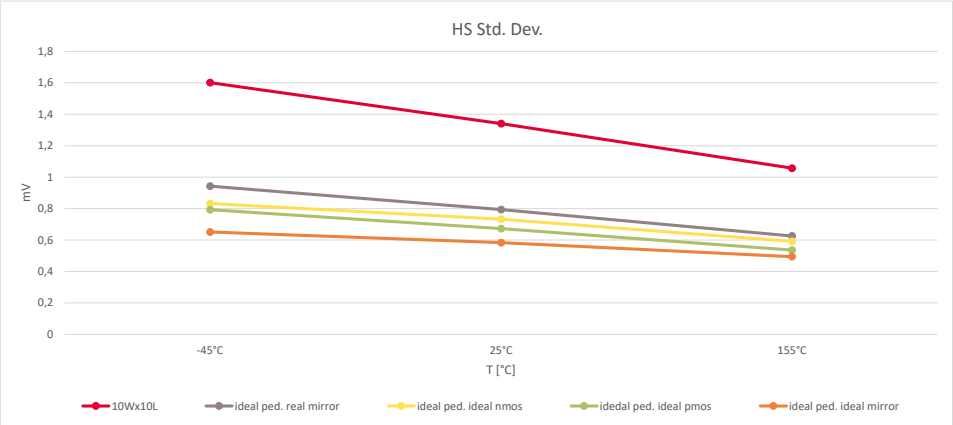


Figure 5.4: Mean value and standard deviation of the circuit with ideal output mirrors and pedestal current generator. HS front end transistor dimensions are $10W$x$10L$ for each test

The ideal current generator has a big effect on both stochastic and systematic errors. These results, although useful for finding the offset sources, are not achievable. Further design iterations should strive for less offset in these areas.

The redesign of these components are beyond the scope of this thesis. In the following chapter the focus will be shifted on experimental data and temperature dependence. This kind of investigation allows for the identification of offset sources that might not be taken into account in the simulations used.

Chapter 6

Laboratory Measurements

The current sensing circuit analyzed in this thesis is used in different versions of the chip where, for instance, the number of channels can vary (each channel has a dedicated current sensing amplifier), but at the same time the current sensing amplifier can be inserted in a different design with different features.

The design versions concerning this thesis are two, and will be referred as version A and B

A is an older design on which B was built. The main differences concerning this thesis between these designs is the introduction in design B of a temperature dependent current generator used to compensate the temperature behaviour of the amplifier.

Regardless of the design versions, every chip has an analog dimming feature that allows to regulate different load currents by changing an internal voltage reference V_{REF} depending on the voltage V_{SET} of the SET pin as in Figure 6.1. The control loop of the LED driver aims to render nil the difference between V_{REF} and V_{out}, the current sensing amplifier's output which coincides with

$$V_{out} = A_{CS}(V_{FBH} - V_{FBL}) = A_{CS}R_{sense}I_{load} \tag{6.1}$$

Where A_{CS} is the amplifier's gain, R_{sense} is the resistor across which flows the regulated current I_{load} and $V_{FBH} - V_{FBL}$ is measured.

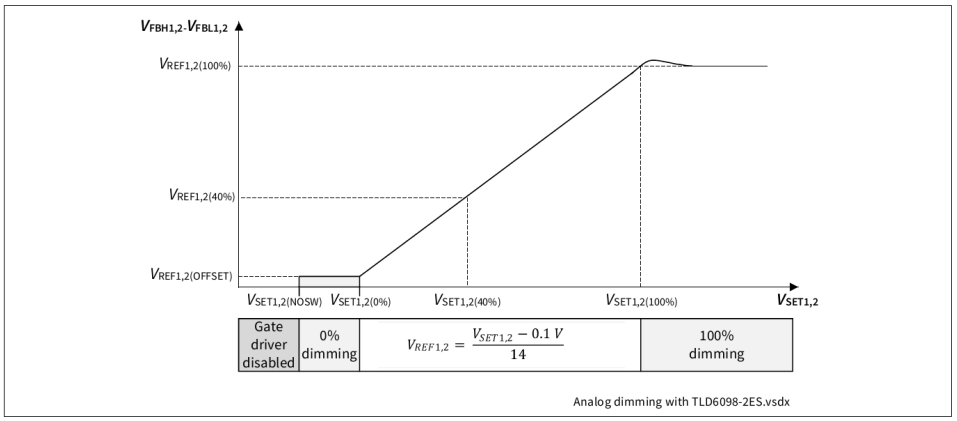


Figure 6.1: Relationship between V_{SET} and V_{REF}

This laboratory activity has three main purposes:

- Measure if the changes introduced in the testchips improve temperature behaviour.
- Find future improvement areas to reduce temperature depending offset.
- Measure potential degrading effect of a bonding pad overlaying the current sense amplifier.

1 Temperature dependent offset

Both designs are used for the analysis of temperature dependent behaviour: design A is used in the testchip with chopper implementation, whilst the testchip based on design B has no major differences from the original circuit other than the lack of the pad overlaying the current sensing circuitry.

1.1 Chopper Results

The testchip with chopper implementation is a dual channel chip based on the A design.

The main features of this testchip are

- Possibility of enabling/disabling the chopper
- Possibility of changing f_{CHP} between $312.5kHz$, $625kHz$, $1.25MHz$ and $2.5MHz$
- Possibility of bypassing the HS mixer, using the LS mixer whilst in HS conditions, leaving the HS front end out of the chopped region

The testchips in analysis skipped the front end trimming procedure during the manufacturing process. Despite this, it's possible to perform back end trimming (after packaging) in the laboratory.

On each device a trimming procedure is performed twice before testing: once with the chopper enabled and once with the chopper disabled. Every trimming procedure for this testchip is performed at ambient temperature ($25°C$).

The accuracy test consists in the evaluation of the required $V_{FBHL} = V_{FBH} - V_{FBL}$ to obtain the correct output of the error amplifier. A voltage ramp is performed at the input of the current sense amplifier, while the output current of the error amplifier is measured.

The monitored aspects in this analysis are the following:

- Effects caused by the introduction of the chopper amplifier
- Offset variation between temperatures within a single devices
- Effects caused by the variation of f_{chp}
- Effects caused by the variation of V_{FBL}
- Spread between samples at each temperature

In order to correctly analyse the parameters above, a wide array of tests are performed with these variations:

- $V_{IN} = 13.5V, 36V$
- $V_{FBL} = 0V(LS),\ 13.5V,\ 70V(HS)$
- $V_{SET} = 5V,\ 2.2V(100\%\ ADIM)\ 0.94V(40\%\ ADIM), 0.54V(20\%\ ADIM)$
- $T = \ -45°C, 25°C, 105°C, 155°C$
- $Chopper = OFF,\ ON,\ f_{CHP} = 312.5kHZ, 625kHz, 1.25MHz, 2.5MHz$
- $Chopper\ Override = OFF,\ ON$

The chopper override function allows to bypass the HS mixer and enables the LS mixer while in HS operation.

Each test is performed for both channel, and with the two aforementioned trimming conditions.

Due to the amount of data gathered it's necessary to rule out some of the conditions deemed not critical to the final results or with a constant effect on the output.

These are:

- V_{IN} does not affect the measurements since it represents the DC-DC converter input voltage and the measurements are performed in an open loop configuration (no converter attached). No other voltage inside the circuit depends from it.
- Chopper results are presented in the trimming with chopper on conditions, while non chopper results are presented in the trimming with chopper off conditions, in order to not introduce spread due to trimming favoring one configuration over the other.
- $V_{FBL} = 13.5V$-$70V$ introduces a constant shift across all temperatures in all devices and channels.
- f_{CHP} does not introduce any systematic effects, neither between devices or across temperatures.

The last two results are easily observable in Figures 6.2 and 6.3

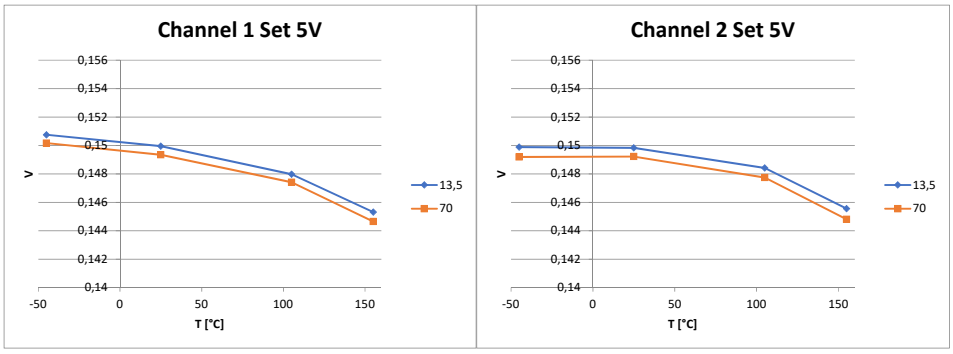


Figure 6.2: The change of V_{FBL} from $13.5V$ to $70V$ results in a rigid downward shift of the curves.

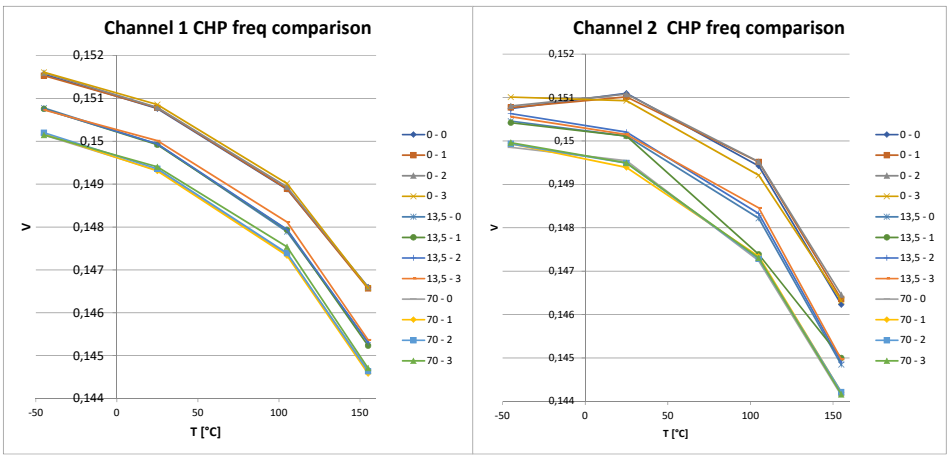


Figure 6.3: Mean temperature curves at different f_{CHP} both at the three values of V_{FBL}. In the legend, 1 corresponds to $f_{CHP} = 312.5KhZ$, 0 to $625kHz$, 2 to $1.25MHz$ and 3 to $2.5MHz$ Each value of V_{FBL} has similar curves for each chopping frequency

To better gauge the effects of the chopper amplifier on the temperature stability, it's possible to isolate the curves of a single device. The graphs in Figure 6.4 report the behaviour of a typical device.

It can be seen that channel 2 has a worse temperature behaviour with the chopper OFF. Once the chopper is turned ON, performances mimics the ones in Channel 1 This might be an effect of the overlaying pad, present in Channel 2, but not present in Channel 1.

Chopper Override is a shifted (due to trimming) version of the chopper OFF curve

Low Side curves do not have the same correction pattern as High Side ones since Chopper OFF performances don't seem to be affected as much at low temperatures. This might be sign that pad stresses affect mainly the HS front end circuitry as alluded previously. Further analysis on pad effects will be carried out in Section 3 of this Chapter.

Regardless of the input conditions, the $\Delta_{HOT-COLD}$ is a monotonically decreasing curve that in the worst case can reach values of $\approx 10mV$ with chopper disabled, $\approx 6mV$ with the chopper enabled and has the worse effects between $105 - 155°C$.

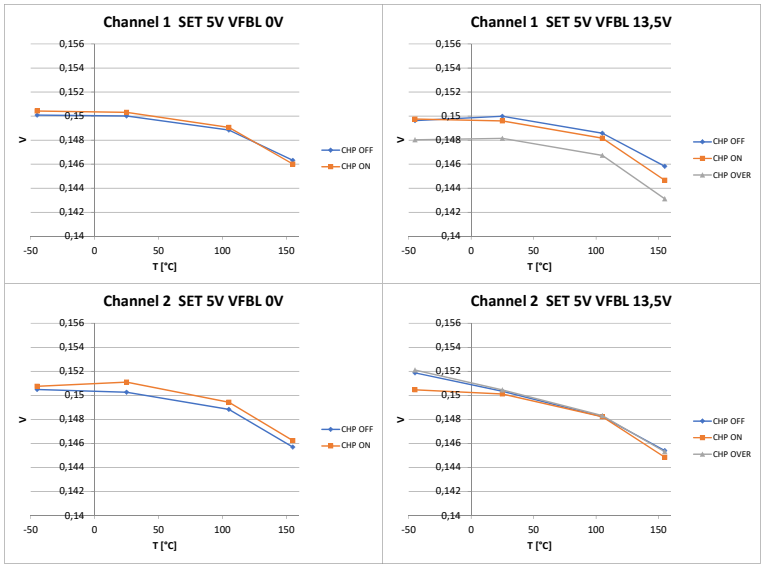


Figure 6.4: Accuracy results of DUT 14. Blue curves are chopper OFF curves, orange are chopper ON curves and grey are chopper ON with chopper override

It's possible to monitor the standard deviation of V_{REF} in order to gauge performances of the samples, and most importantly whether, even after trimming, the chopper amplifier improves it.

Due to the small number of tested devices these numbers have to be taken as a qualitative indication of what the circuit does. It can be seen that the sigma is almost always better with the chopper enabled even after trimming, therefore this topology cannot be used in place of trimming

As expected the lowest sigma is at 25°C, since its the temperature the trimming is performed at. The numbers obtained at this temperature is indicative of not only the topology performance but of the trimming performance too.

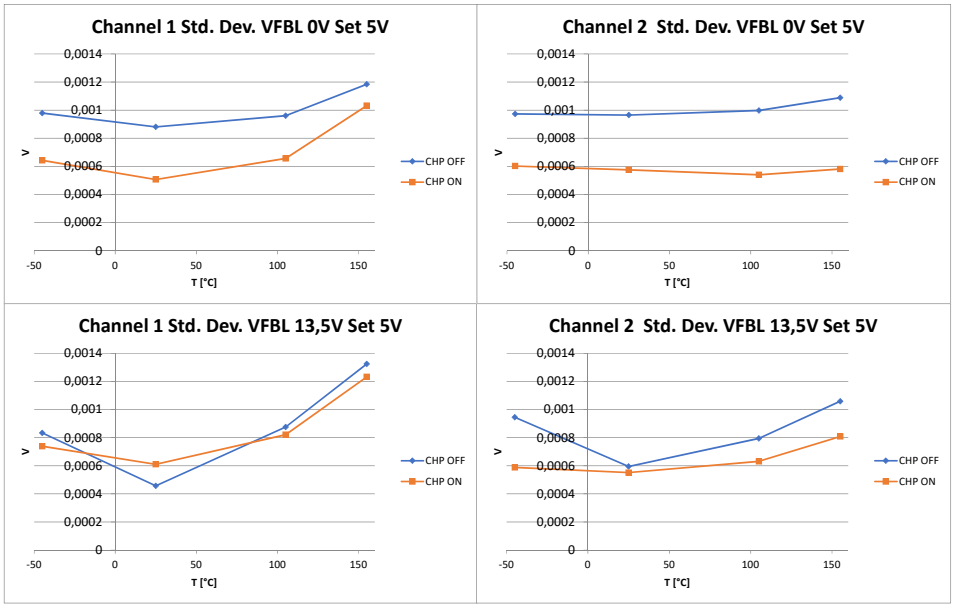


Figure 6.5: Comparison of the standard deviation of the devices analyzed with chopper enabled and disabled in Channel 1 Channel 2.

1.2 Introduction of temperature compensation

As seen in Figure 6.5, the curves are monotonically decreasing functions of temperature. This behaviour has been addressed in Design B with a temperature dependent current generator that compensates the average slope of the accuracy curves of design A.

The testchip analysed in this section is a single channel version based on design B with no pad overlaying the current sensing circuitry. Like the testchips based on design A, these chips were not trimmed during production, and will undergo back end trimming as the previous chips, with the difference that this time it will be performed at $155°C$ as it would in the fabrication process.

The trimming procedure is similar to the one used for the other testchip, but has different target values that take into account the temperature curves to obtain the correct values at ambient temperature despite performing the trimming at $155°C$.

In Figure 6.6 are reported the curves of one device representing the typical behaviour of the 20 tested. Comparing the behaviour of the curves with $ADIM$ 100% of these testchips with those obtained with version A of the design it's possible to observe the effects of the compensation current. $\Delta_{HOT-COLD} \approx 0$ and in both HS and LS configuration, the spread caused by temperature is $\approx 4mV$.

One side effect of the compensation introduced with this design is the behaviour at lower levels of $ADIM$. As can be seen in Figure 6.6, $ADIM$ 40% curves have a monotonically increasing trend with temperature after the compensation has been introduced.

The suspected reason for this behaviour is the voltage used as a reference as input for the error amplifier. The output of the current sense amplifier is compared with a voltage V_{REF} derived from the voltage at the set pin. When $V_{SET} \leq 2.2V$ corresponding to $ADIM < 100\%$,V_{REF} depends directly from V_{SET} while for $2.2V \leq V_{SET} \leq 5V$, which corresponds to $ADIM = 100\%$ V_{REF} is derived from the internal bandgap voltage reference.

This implies that for $ADIM = 100\%$ V_{SET} will vary with temperature, following the bandgap reference voltage curve. The current compensation has been calibrated to compensate the $ADIM = 100\%$ behaviour therefore factoring in the bandgap reference behaviour and resulting in an overcompensation at lower levels of $ADIM$.

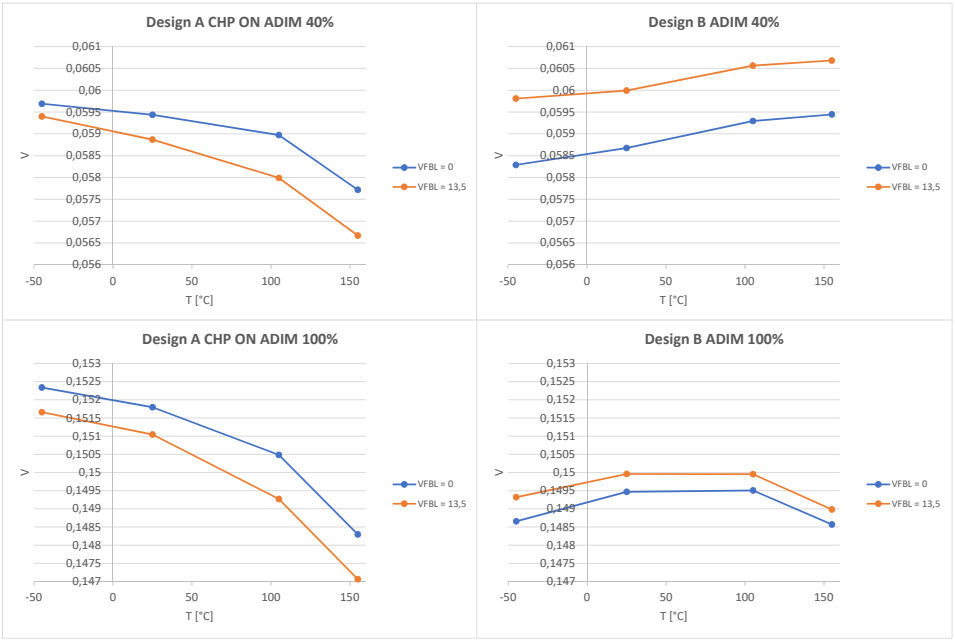


Figure 6.6: Accuracy results for $ADIM$ values of 40% and 100% with chopper enabled on design A. Both instances have no overlaying pad

In Figure 6.7 V_{REF} drops $\approx 6.5mV$ in the $105°C - 155°C$ interval with $ADIM = 100\%$, corresponding to a $\approx 1.65mV$ input referred drop. The measured input voltage drop at the same temperatures in design B is $\approx 1mV$, implying an input referred compensation of $\approx 0.65V$.

With $ADIM = 40\%$ the $105°C - 155°C$ is $\approx 2mV$, corresponding to a $0.5mV$ input referred drop. Taking into account the $0.65mV$ uplift given by the compensation, it's possible to explain the slight uplift observed in design B with $ADIM = 40\%$ in this temperature interval.

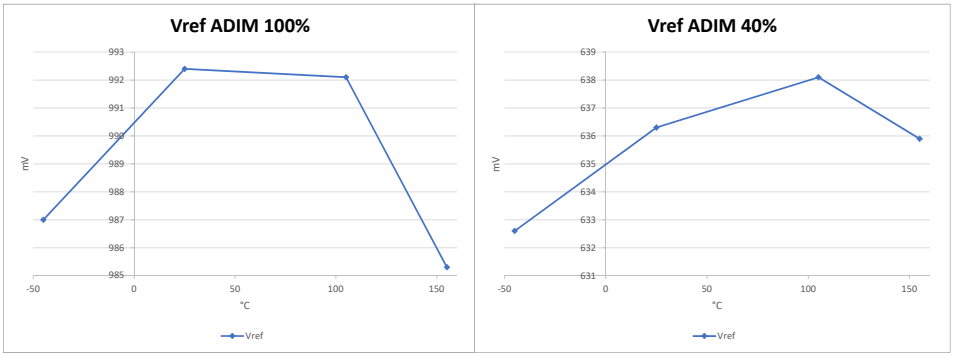


Figure 6.7: Comparison of V_{REF} with $ADIM = 100\%$ and 40%

1.3 Focused Ion Beam modifications

Further research is needed to improve temperature behaviour. The first observation is that all devices have a tendency of decreasing the regulated current between $105°C - 155°C$. This behaviour is more evident in design A due to the lack of compensation current, and exceeds the expected $\approx 1.65mV$ drop dictated by the behaviour of V_{REF} observed in Figure 6.7.

A potential cause for this behaviour could be the Electrostatic discharge (ESD) protection structure located at the $COMP$ pin since a potential leakage of this structure can affect the feedback loop of the error amplifier, resulting in a lower regulation.

A reason for the high temperature drop of V_{REF} observed in the previous paragraph is researched in the schematic, leading to the generating point of V_{REF}.

As in Figure 6.8, the $1V$ reference voltage is derived from the bandgap voltage reference via a resistor divider. At this node a low-pass RC filter was inserted to help with smoothing the transients that occur when the chip is turned on.

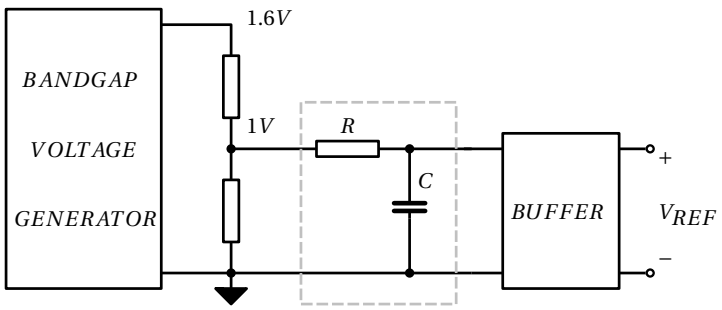


Figure 6.8: V_{REF} generation block diagram

The low-pass filter uses a $200k\Omega$ resistor, that could be the cause of a voltage drop if the following circuitry presents even a leakage current in the order of tens of nA at high temperature.

To investigate the effects of the ESD protection leakage and the low-pass filter resistor, chips based on design B have been subjected to a Focused Ion Beam (FIB) treatment. This procedure consists in de-lidding the chip with the aid of chemicals to access the die. Once the die is exposed the metal layers can be cut or bridged with the aid of an ion beam that can either remove or deposit some material. After the connection have been made, the die is passivated and the chip is covered, either with a metal lid or with a plastic material.

For a correct observation of the effects caused by these changes, the current compensation is disabled because it has been calibrated with results of chips that had the aforementioned components.

In summary, the following modifications have been made:

- Removal of ESD protection structure for $COMP$ pin,
- Removal of current compensation,
- Removal of resistor between $1V$ generation node and V_{REF} node.

The FIB modifications have been performed on several chips. After monitoring the behaviour of the chips while testing, only 2 devices could be considered stable in the whole temperature range, and their result are reported in Figure 6.9.

The instabilities could be due to the invasive nature of the process that can introduce defects. Most of the faulty behaviour consisted in a continuously changing regulated current, and appeared mostly at $-45°C$ or $155°C$, suggesting that the FIB procedure caused slight damages that became critical only in extreme conditions.

Disabling the current compensation result in a downward tilt of the curves that resembles the behaviour of design A. In HS conditions the compensation is much more present than in LS by design, and the tilt observed post FIB is proportional to it.

This highlights that the changes did not resolve the tilt issue, since both the ESD structure leakage and the $200k\Omega$ resistor removed from the circuit should affect the circuit only at high temperatures.

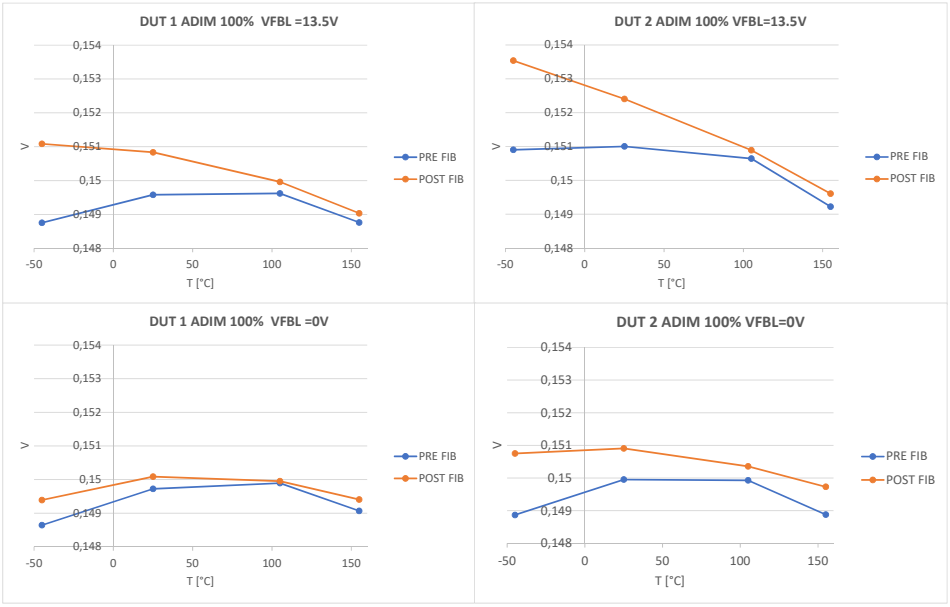


Figure 6.9: Accuracy results for the two devices that survived the FIB modifications. Results are shown pre and post FIB

Shifting the focus to the $105°C - 155°C$ interval, is possible to observe a similar drop between pre FIB and post FIB data of $\approx 1 - 1.5mV$ for HS and $\approx 1mV$ for LS. This is a sign of improvement, since post FIB data does not have the current compensation while pre FIB data has it.

To better visualize the difference, it's possible to mathematically add the effects that the compensation current would have added. The current was measured before the FIB procedure for each device. It's possible to input refer the voltage drop that the current variation causes when it flows across the output resistor as follows:

$$V_{T_{Comp}} = V_T + \frac{(I_{Comp_T} - I_{Comp_{155°C}})R_{out}}{A_{CS}} \tag{6.2}$$

Where V_T is the voltage at a certain temperature T and I_{Comp_T} is the compensation current measured at that same temperature.

Results are reported in Figure 6.10. After factoring in the current compensation, it's possible to observe flatter curves, especially in the $105°C - 155°C$ interval. With respect to pre FIB curves, the performance are better across the board, and reduce the overall delta from $1mV$ to $0.6mV$ for DUT 1 and $1.9mV$ to $1.5mV$ for DUT 2.

Due to the high amount of unstable chips, it's difficult to generalize data coming from only 2 samples. Figure 6.11 shows how the remaining chips have quite different behaviours, both before and after the modifications, especially in *HS* conditions, and it's possible to state that despite their differences, the changes did result in improvement in both cases, indicating that the lower temperature spread might not be due to a lucky couple of devices.

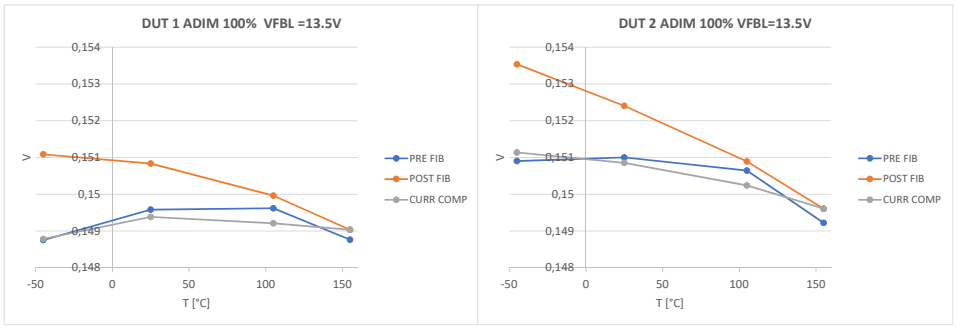


Figure 6.10: Comparison between accuracy result post FIB and the same results with the added compensation

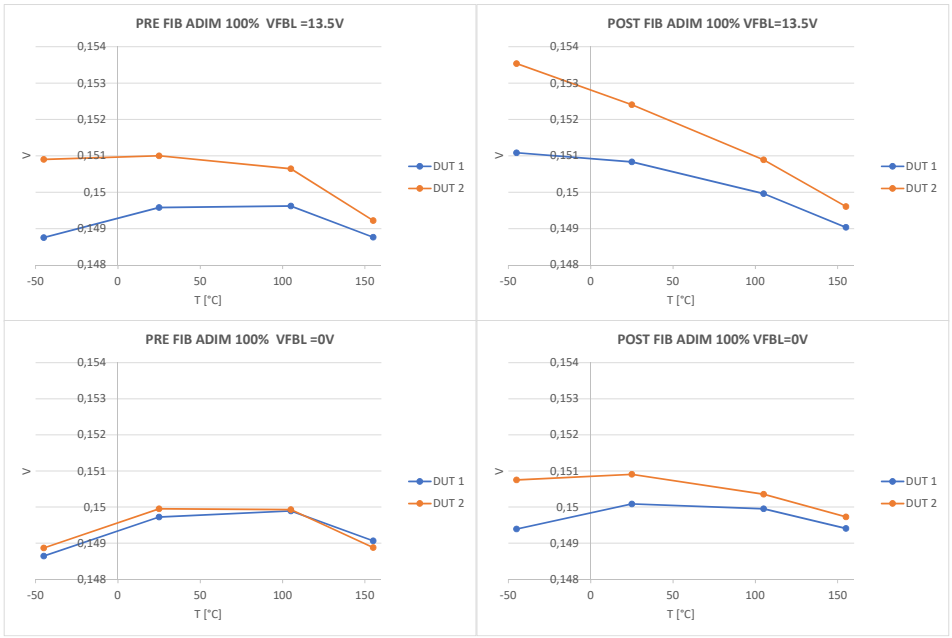


Figure 6.11: Comparison between the two DUTs before and after FIB highlights the variation between samples

Internal voltage references

The tilt observed in design A has been compensated in average with the current generator in design B, but as higlighted in DUT 2 data in Figure 6.10, not always the compensation eliminates the problem.

To investigate the source of this tilt, the following internal references are monitored:

- Bandgap Voltage V_{BG} from which all other internal voltage references are derived
- $V_{REF_{100}}$, an internal $1V$ reference used as V_{REF} when $ADIM = 100\%$
- V_{out}, the output of the current sense amplifier

By observing these references, it's possible also to assess if the removal of the $200k\Omega$ resistor identified in Figure 6.8 did affect the chip performances since measurement are taken before and after the FIB modifications.

To better understand all internal voltage references behaviour, the bandgap reference is monitored since they are all derived from it.

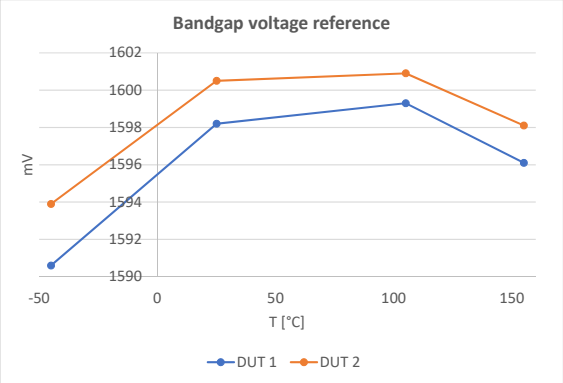


Figure 6.12: Bandgap voltage reference behaviour before FIB modifications in $DUT1$ and 2

In figure 6.12 the $1.6V$ bandgap voltage reference V_{BG} shows significant suffering at cold temperatures, with a drop of $\approx 7.5mV$ in the worst case, in the $105°C - 155°C$ interval a less significant $3mV$ drop is present.

In this voltage reference the slope observed in the accuracy test results without current compensation does not emerge, therefore V_{REF} and V_{out} are monitored to check if the origins of this behaviour can be found in these internal voltage references.

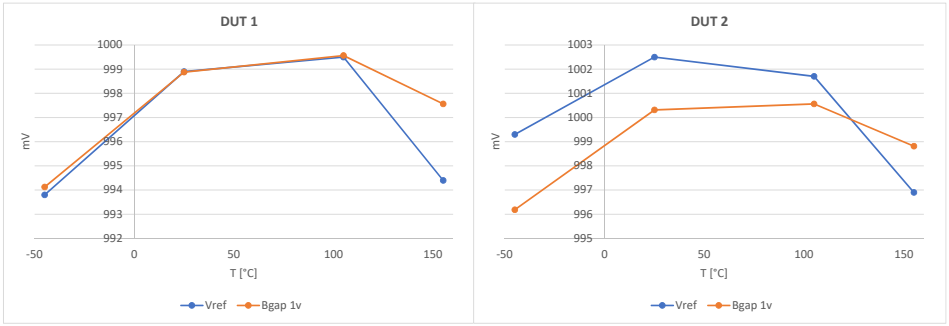


Figure 6.13: Comparison between V_{REF} and a version of the bandgap reference that has been resized to $1V$

In figure 6.13 V_{REF} is reported alongside with a scaled version of $V_{BG_{1V}} = \frac{V_{BG}}{1.6}$ is reported, to act as a reference point, and see how V_{REF} deviates from it.

Between $-45°C$ and $105°C$ it's possible to see once again how the two devices analyzed are different:V_{REF} in DUT 1 perfectly follows $V_{BG_{1V}}$, while in DUT 2 V_{REF} is a tilted and slightly offsetted version of $V_{BG_{1V}}$, confirming the diversity of the population of this analysis, despite its small size.

In the $105°C - 155°C$ interval there is a significant departure from $V_{BG_{1v}}$ in both devices, where V_{REF} drops an additional $\approx 2.5mV$ more than $V_{BG_{1V}}$.

This could be caused by the $200k\Omega$ resistor in Figure 6.8. The same data is gathered after FIB modifications, to confirm this hypothesis.

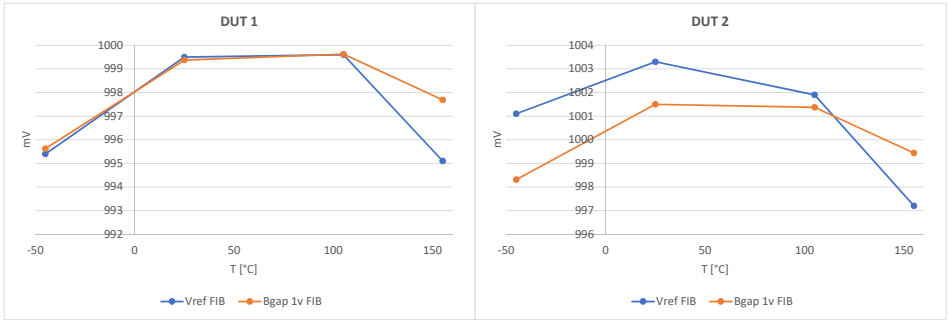


Figure 6.14: Comparison between V_{REF} and a version of the bandgap reference that has been scaled to $1V$

Data in Figure 6.14 shows that after FIB modifications, in the $105°C - 155°C$ interval DUT 1 the drop decreases of $\approx 0,7mV$, while for DUT 2 it decreases of only $0.2mV$. This indicates that the effects of removing of the $200k\Omega$ resistor can be very small, depending on the device.

V_{REF} measured with $ADIM = 40\%$ can be shifted to $1V$ by adding the residual voltage. Since $V_{REF_{40\%}}$ is centered around $640mV$ the formula used is $V_{REF_{40\%,1V}} = V_{REF_{40\%}} + 360mV$.

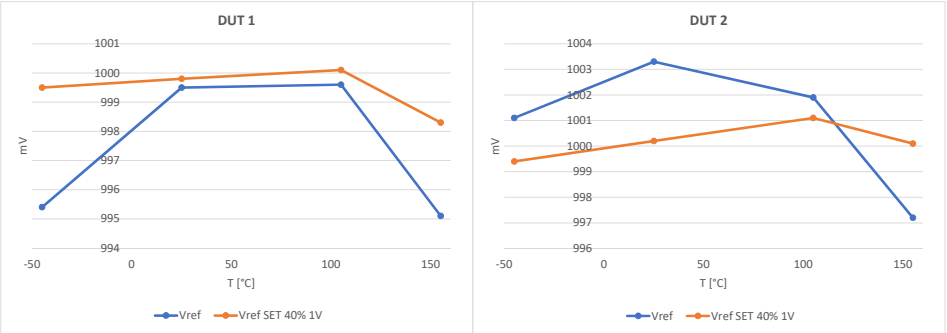


Figure 6.15: Comparison between V_{REF} with $ADIM = 100\%$ and a shifted version of V_{REF} with $ADIM = 40\%$ to $1V$

Figure 6.15 shows that when V_{REF} is derived from V_{SET} as it is for $ADIM < 100\%$ instead of V_{BG}, the variation with temperature is much less.

The residual temperature variation in $V_{REF_{40\%,1V}}$ highlights that the V_{REF} generation circuit used for $ADIM < 100\%$ contributes to the temperature variation observed in Figure 6.6. The generation of V_{REF} uses two different circuits for $ADIM < 100\%$ and $ADIM = 100\%$, therefore the temperature dependence in $V_{REF_{100\%}}$ cannot be derived by a superimposition of $V_{BG_{1V}}$ and $V_{REF_{40\%,1V}}$ temperature dependencies.

2 Future improvement

Overall, the FIB modifications highlighted that ESD leakage and $200k\Omega$ resistor have an effect on the temperature behaviour, and should be improved in the case of the ESD protection structure, or removed in the case of the resistor, since it does not affect the functionality of the circuit.

Despite the improvements obtained with these modifications, the temperature behaviour is still not ideal, and further research should be done to investigate the source.

The main area of research should be to find source of the temperature slope compensated with the current compensation I_{COMP} and the increase temperature stability of V_{BG}. Assessing the source of temperature dependence of V_{REF} is also important, especially at hot temperatures, where it has a worse behavior of $V_{BG_{1V}}$

3 Physical stresses: packaging and bonding

A source of offset that couldn't be taken into account in simulation is the physical stress introduced by packaging and bonding.

Both of these procedure can introduce stresses in the die that can affect the silicon properties and cause mismatch between critical structures for offset reduction.

These stresses become important if they are introduced after the trimming procedure. Trimming as mentioned in chapter 2 can occur at different stages of the chip manufacturing, and the later is introduced the less cost effective it is, therefore the stress introduced by bonding and packaging often can't be compensated.

Even if the trimming could be performed on all chips once packaged, the problems introduced by physical stress will still be present. Since trimming is a snapshot of the chip at a certain temperature and the different materials involved in bonding and packaging have different thermal expansion coefficients, the change in temperature will give rise to different physical stresses, potentially canceling the effects of trimming.

While the packaging stresses can't be removed, bonding stress, since it's more localised, can be avoided by removing it from sensitive parts of the circuit.

The original silicon happens to have a bonding pad above part of the current sensing amplifier. The pad in question is an additional connection taken as a precautionary measure during the design stages to avoid voltage drop caused by high current spikes that can occur at that pin. Bonding stresses can affect, although lightly, some properties of the silicon underneath [3] [4] and therefore laboratory measurements are needed to gauge if this is the case for the circuit in analysis.

3.1 Pad Effects

Experimental data for the effects of the overlaying pad are gathered from both versions of the circuit.

The analysis is carried out on a dual channel testchip with chopper implementation (based on the A version of the circuit) which has one of the channels with the pad removed, and a single channel testchip based on the B version which has no pad.

From the first with chopper implementation, a first analysis is carried out. It's possible to calculate the standard deviation of the current sense amplifier's input referred offset voltage from the gathered data, and formulate some hypothesis on the effects of the pad on the underlying circuitry.

Data is gathered with an accuracy test performed on the same devices with the chopper both enabled and disabled. For each configuration, a different trimming instance has been used: chopper ON data uses trimming obtained with the chopper amplifier enabled, whilst chopper OFF data uses trimmed obtained with the chopper disabled. Each trimming was performed at $25°C$

The accuracy test consists in the evaluation of the required $V_{FBHL} = V_{FBH} - V_{FBL}$ to obtain the correct output of the error amplifier. A voltage ramp is performed at the input of the current sense amplifier, while the output current of the error amplifier is measured.

The standard deviation of all the gathered data doesn't confirm the previously formulated hypothesis: for both HS and LS measurements the performances of channel 1 (without pad) are worse than channel 2 (with pad).

The suspected cause of this is trimming, since it's the main variable added between this test and the previous (at least at ambient temperature).

Further investigation has been carried out with chips based on the B architecture.

Using an accuracy test, 10 chips with the overlaying pad are tested and compared to 20 testchips based on the same architecture with no pad. The standard deviation of all the tested devices are compared in order to gauge the effects of the pad and check if the previous results obtained with this test .

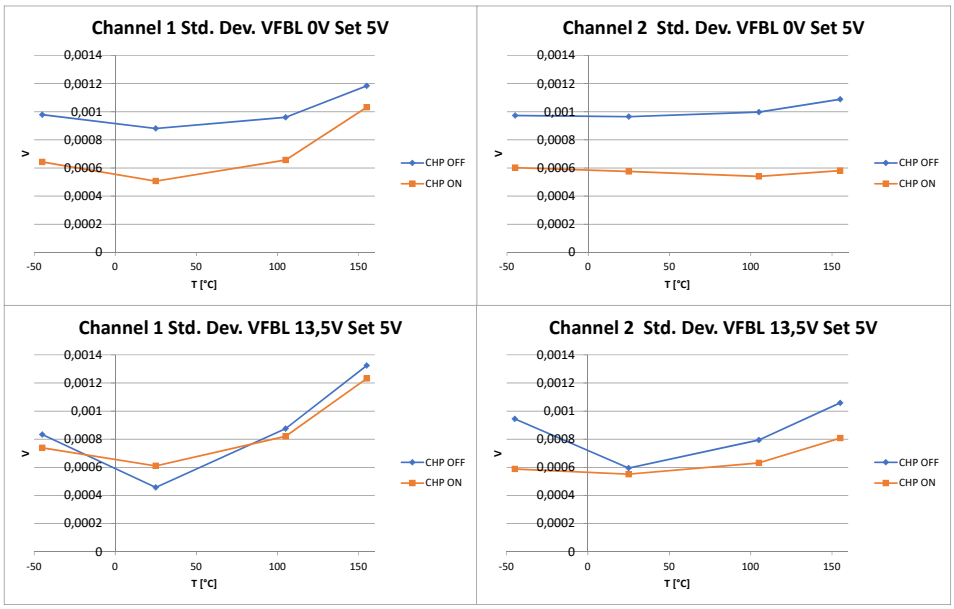


Figure 6.16: Comparison of the standard deviation of the devices analyzed with and without the overlaying pad in Channel 1 and with overlaying pad in Channel 2.

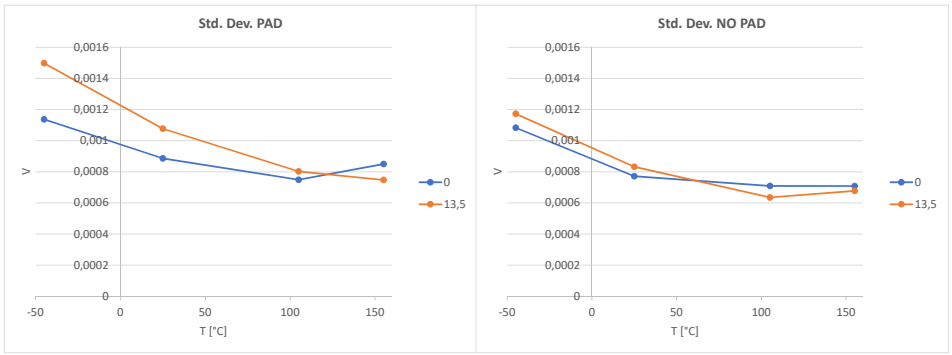


Figure 6.17: Comparison of the standard deviation of the devices analyzed with and without the overlaying pad in HS and LS conditions

From the data reported in the graphs of Figure 6.17 seems to emerge that the inclusion of the pad degrades the HS performance, whilst LS performance seems to be unaltered. Performances at $155°C$ are similar due to trimming, but at colder temperatures the effects of the physical stresses are more evident.

Despite not all the data gathered pointing towards the pad degrading the performances, the pad will be removed in the next iteration of the chip. The effects of the pad are muted by trimming since it is performed after packaging. The commercial product will not undergo the same procedure, and will be trimmed before packaging, therefore the effects might be more evident.

Due to chip availability at the time of testing, the sample sizes don't allow for a quantitative comparisons between standard deviations and therefore these results cannot be generalized, stating that the pad will have a degrading effect on the underlying circuitry. Moreover, the data wouldn't be representative of real world performance not only due to the small sample size but also because that all the testchips are from the same wafer and long term process variations that could happen in the manufacturing process are not represented in the study.

Chapter 7

Conclusions

The study conducted in this thesis had the aim of lowering the performances of the current sense amplifier in an LED driver IC.

The main focus were:

- Lowering the standard deviation of the input referred offset,
- Lowering the temperature variation of the input referred offset,
- Lowering production costs either by removing trimming steps or decreasing the area occupied by the amplifier.

The first improvement achieved is the smaller area impact obtained with the scaling of the transistors in the HS front end introduced in Chapter 5, where the standard deviation of the simulated population achieved similar results compared to those obtained with the chopper implementation, while not requiring less area than the level shifter used in the chopping amplifier.

This is an important result because in high volume production like in the case of this chip, increasing yield without sacrificing performances can be very beneficial, therefore future versions of the chip should prefer this solution to the chopper amplifier.

Other offset reduction methods such as Continuous Time Auto Zero and Ping Pong Auto Zero have been investigated, but then abandoned due to the area that these topology would require without a fundamental redesign of the current sense amplifier, since this was not the aim of the study.

Laboratory data indicates that despite the use f an offset nulling topology like the chopper amplifier, trimming is still a crucial resource and cannot be removed yet from the production process.

Slight improvements in temperature behaviour have been achieved by removing the pad overlaying the current sense circuitry, especially for HS conditions. The increase of HS front end transistor area could attenuate the effects caused by the pad, but this can only be confirmed by experimental data which are not available at the time of writing.

The pad in question is an additional connection taken as a precautionary measure during the design stages to avoid voltage drop caused by high current draws occurring at that pin.

Since the pad has no critical function and from the performed test it seems to degrade the chip performances, in later versions of this circuit the pad should removed.

To improve temperature performances, the modifications introduced with the Focused Ion Beam (FIB) procedure in Chapter 6 should be applied to a future version of the chip.

The removal of the $200k\Omega$ resistor is an easily achievable modification, but the the ESD protection removed from $COMP$ pin cannot be implemented. A redesign of the ESD protection with the aim of reducing the high temperature leakage is required for future versions of the chip.

Ultimately a balance between production costs, development costs and performances have been struck, achieving the proposed objectives of this study while highlighting areas of improvement for future versions.

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