

Differential read-out circuit for capacitive sensors

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Laurea Magistrale in Ingegneria Elettronica

Università degli Studi di Padova
Facoltà di Ingegneria

Supervisor:
Andrea Gerosa

in cooperation with:
Infineon Technologies Austria AG

Supervisor:
Andreas Wiesbauer

thanks to:
Wilfried Florian (Infineon Technologies Austria AG)
Michael Kropfisch (Infineon Technologies Austria AG)

Student:
Francesco Polo

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Chapter 1

Introduction

1.1 Motivation

Capacitive sensors market is growing every year with a constant annual rate, involving more and more interest in research and development. They have the capability to fit with a wide variety of sensing and measurement problems such as proximity detection, linear and rotary position encoding, fluid level detection, pressure measurements, acceleration detection and so on.

Capacitive sensors are very resistant to environmental factors, i.e. they can be unaffected by temperature and humidity. They also present a good robustness to mechanical misalignment. Another positive feature of this kind of sensors is their little power consume, especially important in portable device.

Accuracy and reliability reached by capacitive sensors are excellent. Furthermore, the technology can be easily integrated in a silicon substrate ensuring a good temperature stability of the sensor parameters. The main advantages of integration on silicon are [1]:

- Improved sensitivity
- Temperature compensation
- Easier Analog to Digital conversion
- Batch fabrication for lower cost

All these characteristics explain the success of capacitive sensors and their large presence in various consumer goods. However, the main limitation is represented by the design complexity of the sensor interface.

A capacitive sensor is a passive element which needs an active circuit to generate an output signal. The focus of this thesis is to study and design

such a circuit with differential read-out. Being an analog block, this circuit plays a fundamental role in the total system performances.

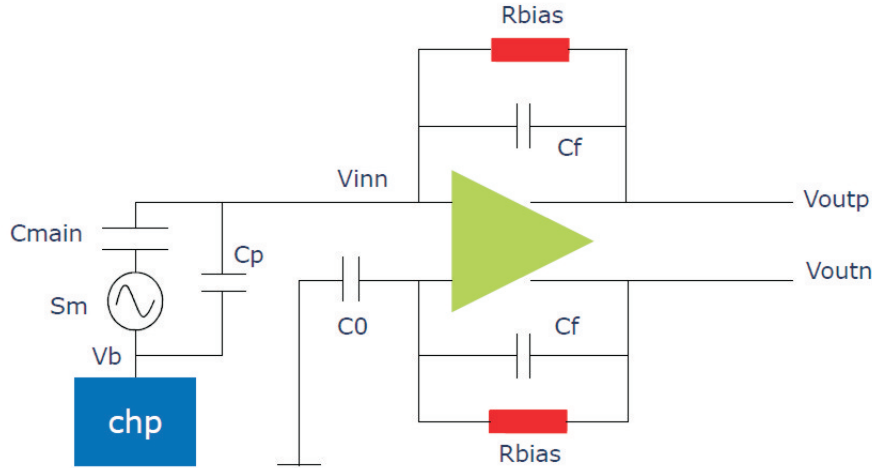


Figure 1.1: *The capacitive sensor model together with its differential read-out circuit*

Figure 1.1 reports the capacitive sensor electrical model, which consists of the sensor capacitance C_{main} with the signal generator S_m and the parasitic capacitance C_p in parallel, together with differential read-out circuit. The figure shows the system from a concept point of view. The illustrated solution includes an operational transconductance amplifier (OTA), which provides a current proportional to the differential input voltage, in a pseudo differential configuration. The single ended signal from the sensor is converted in a differential signal with all the benefits that this process provides.

First of all, the main goal for the system is to achieve the lowest overall noise with the highest linearity. Furthermore, low power consumption and high power supply rejection ratio (PSRR) are required.

This implementation has the potential to achieve all the requirements. In fact, the signal is output-limited in amplitude, since the amplifier input signal is relatively small. Hence, an high linearity can be achieved. Then, the amplifier consists of only one stage, this means low power consumption and less noise source. Furthermore, this implementation can work with high stimulus applied to the sensor due to the fact that the amplifier input signal is a current [9].

1.2 System structure

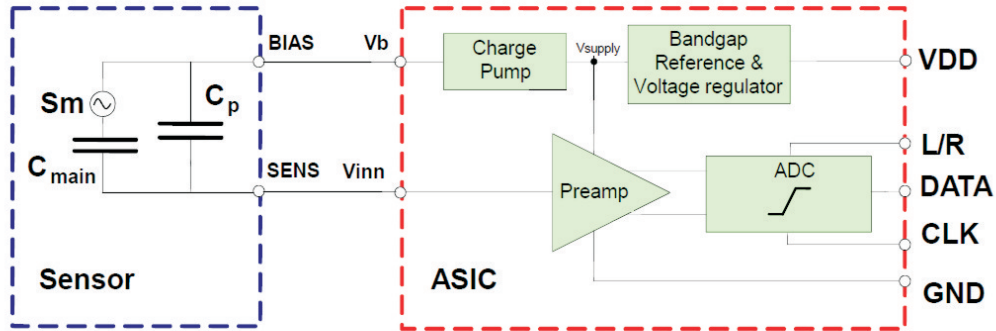


Figure 1.2: *The system architecture*

Figure 1.2 shows the block diagram of a typical sensor system, which includes an integrated capacitive sensor system-in-package (SiP) together with its amplifier, whose differential output signal feeds the analog to digital converter (ADC). Additional biasing blocks are present for the amplifier and the sensor.

The sensor operation can be divided into two parts: detection and output generation. Depending on the kind of measured physical quantity (temperature, pressure, gas composition, etc.), this detection interface can, for example, consist of a mechanical element, a chemical film, or a magnetic component, etc. In any case, the detection stage changes its properties as function of the input physical quantity to generate a related output signal. This signal is then process by analog blocks that usually provide amplification, filtering, etc. The use of analog signal processing is almost always required in situations where there is an interaction with the "real world", as in the case treated in this thesis. The analog part in the system is candidate to carry out a single-ended to differential conversion.

An analogic to digital conversion is then performed by means of a differential input ADC. It is well known that a digital circuit is less sensitive to noise and disturbs than an analog one, therefore, the analog part plays a very important role in the system performances. Hence, a transfer to digital domain should be performed as close as possible to the sensor to avoid the addition of undesirable signals in the analog path between sensor and ADC. In fact, solution that includes analog and digital conditioning together are

preferred.

Chapter 2

The capacitive sensor

2.1 Structure

Every capacitive sensor detects mechanical quantities by means of displacement measurements. A such sensor is realized when a mechanical quantity controls the movement of the flexible capacitor plate respect to a fixed one creates a capacitance variation of the sensor. This variation can be detected with opportune sensor interfaces.

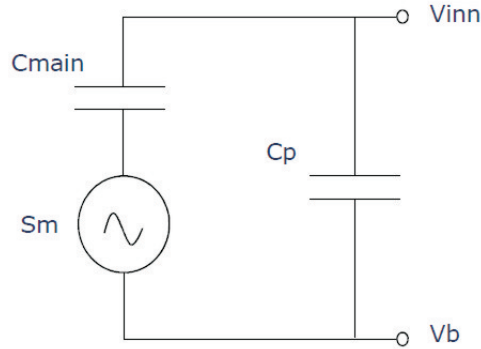
2.2 Model

A capacitive sensor model is needed to simulate the amplifier, focus of this thesis. In a first order modelling, figure 2.1, the sensor model includes the main capacitance C_{main} in series with the signal generator S_m . In parallel to this, a parasitic capacitor C_p is placed, which forms a voltage divider with C_{main} for the signal coming from S_m . If V_m is the peak amplitude of the signal generated by S_m , the peak amplitude of the microphone output signal V_{out} is:

$$V_{out} = V_m \frac{C_{main}}{C_{main} + C_p}$$

The sensor used in this project has $C_{main} = 2.5\text{pF}$ and $C_p = 0.83\text{pF}$.

It's important to underline that this model represents the sensor in a very optimistic way. In fact, it has no limitation regarding noise and linearity. The only non-ideality is represent by the parasitic capacitance C_p that attenuates the sensor output signal. Hence, the noise simulation detects only the noise generated by the amplifier. The same remark is also valid for the linearity.

Figure 2.1: *The capacitive sensor electrical model*

2.3 Parameters

A capacitive sensor is characterized by several parameters. In the following lines, the main parameters are mentioned.

- *Sensitivity*: Sensitivity is defined as the relation between the sensor output signal and the stimulus applied. It is measured in specific load condition. Sensitivity is expressed in $\frac{dBV_{rms}}{X_{rms}}$, where X is the unit with which the input stimulus is measured.
- *Frequency response*: Frequency response indicates Sensitivity variations over the input signal frequency. Bandwidth is the frequency where Sensitivity decreases of $-3dB$.
- *Output impedance*: In a first order model, Output impedance is simply formed by the parallel connection between C_{main} and C_p
- *Stimulus Level (SL)*: Stimulus Level is the logarithmic measure of the input rms voltage of S_m , V_{rms} , relative to a reference value of rms voltage, $V_{ref_{rms}}$. It is expressed in dBSL (dB Stimulus Level).

$$SL = 20 \log_{10} \frac{V_{rms}}{V_{ref_{rms}}}$$

A common value for the reference pressure rms is $V_{ref_{rms}} = 15.8mV_{rms}$, therefore a $V_{rms} = 316mV_{rms}$ give 26dBSL.

2.4 Biasing

The capacitive sensor need a biasing circuit, called charge pump, which provide a clean and stable DC voltage V_b .

The main sensor capacitance can be separated in two contributes, $C_{main} = C_{MAIN} + \Delta C_{main}$. Where C_{MAIN} is the static sensor capacitance, which can be measured when no stimulus is applied to the sensor, in this case $C_{main} = C_{MAIN}$. The second term in the sum, ΔC_{main} , represent the dynamic capacitance. In other words, it is the variation of the sensor capacitance related to the stimulus applied to the sensor. C_{MAIN} and C_p are usually much larger than the varying capacitance to be sensed ΔC_{main} . The static capacitance C_{MAIN} depends on the DC biasing voltage. Sensitivity also slightly depends on the biasing voltage, therefore, V_b must be constant in presence of temperature and voltage supply variations.

To avoid disturbs from the charge pump that can produce noise and non-linearity in the sensor, the biasing voltage V_b is filtered with a low pass filter, called charge pump filter, as it is shown in figure 2.2. Its cut-off frequency is in the order of hundreds of mHz.

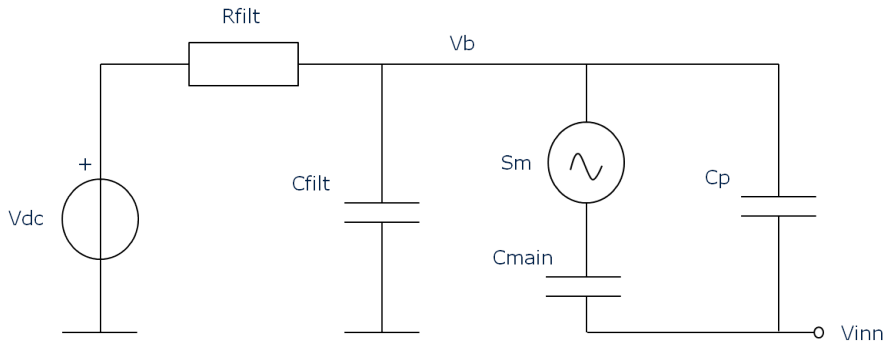


Figure 2.2: *The capacitive sensor with its biasing circuit*

Chapter 3

The operational amplifier

3.1 Concepts

Every passive sensor needs an active circuit to produce an output signal. As it was shown, the amplifier for the capacitive sensor is an operational transconductance amplifier (OTA), figure 3.1, in a pseudo fully differential configuration; in other words, one of its inputs is connected to ground. A feedback network connects the outputs with the inputs.

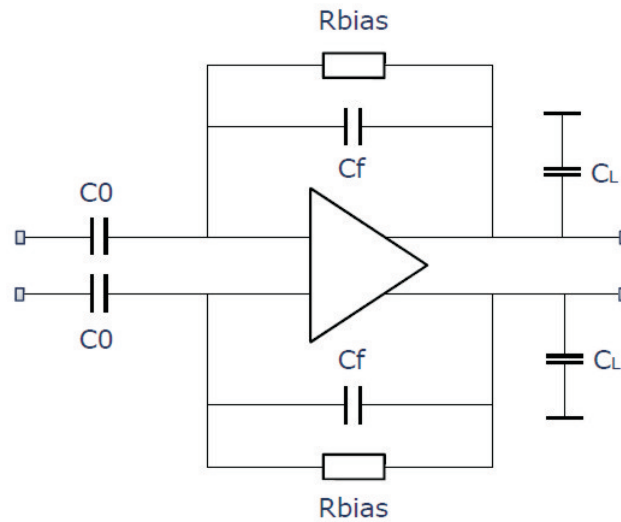


Figure 3.1: *The operational amplifier*

A fully differential structure comports several benefits respect to a single ended one, such as double output swing and rejection of the common mode

disturbs. An higher output swing means an higher signal to noise ratio (SNR). These benefits are achieved at the cost of an higher area and power consumption respect to a single ended configuration.

This amplifier plays a fundamental role in the system regarding its global performance in terms of noise, linearity, power consumption and power supply rejection ratio (PSRR). Therefore, its design is crucial for the whole system.

The amplifier is supplied through a LDO voltage regulator with $V_{DDLDO} = 1.64\text{V}$, whereas LDO voltage supply and the main system supply is $V_{DD} = 1.8\text{V}$. LDO ensures a good voltage stability and a good power supply rejection respect to V_{DD} . Figure 3.2 shows a typical frequency response for a capacitive sensor amplifier. Anyway, a low pass filter is present not only to avoid aliasing phenomena in the ADC, but also to reduce the noise at high frequencies.

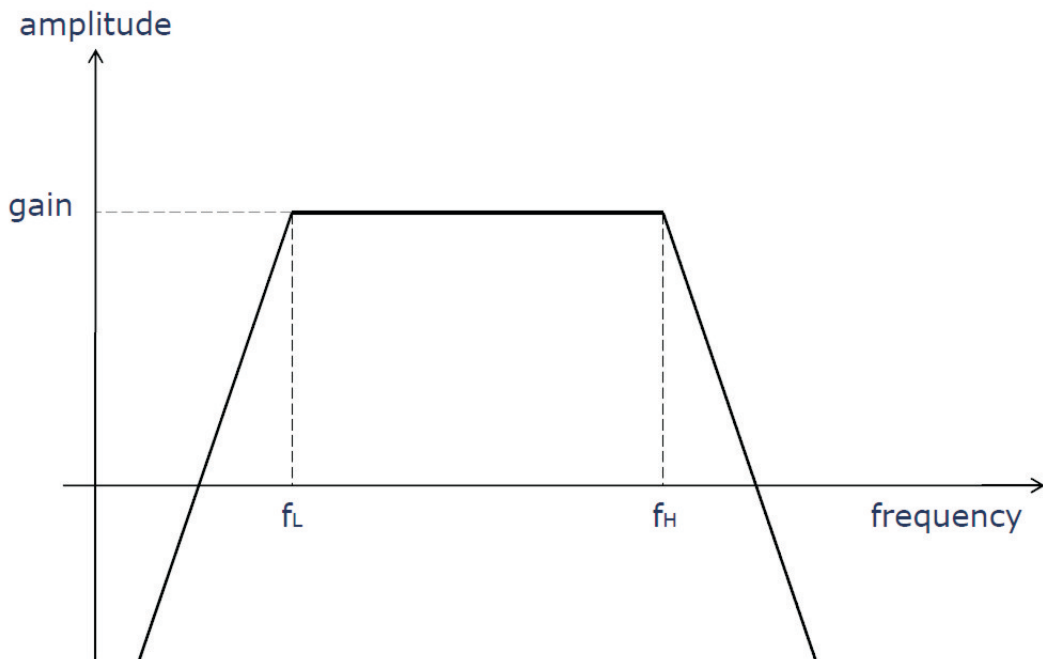


Figure 3.2: *A general amplifier frequency response*

To provide the DC path to the floating amplifier input nodes, two bias resistors R_{bias} are placed in the feedback loop [3][4]. These biasing resistors have a big influence in the output signal linearity and their noise contribution is not negligible. Furthermore, they set the low cut-off frequency of the amplifier.

Since the capacitive sensor is placed in one of the input branch, the gain depends on the sensor variable capacitance, whereas the input capacitance of the other branch, C_0 , is constant. Hence, in normal operative conditions, the amplifier branches will be not matched and it's well known that the differential amplifier performances depends on its matching. Mismatch introduces interaction between the differential mode and common mode signals. However, every real differential amplifier has mismatches due to imperfections introduced by the fabrication process. Nevertheless, in this case the mismatch depends on the sensor signal with a worse influence in the system than a normal process mismatch.

Now it is clear that without any calibration circuit this system won't work. Anyway a calibration system is not part of this thesis, in which the topic regards the amplifier itself and its design. Assuming $C_{main} = C_{MAIN} = const$ and relating the stimulus level directly to the signal amplitude from S_m is possible to study the amplifier without using a calibration system. Furthermore, the input capacitance of the input connected to ground, C_0 , should be matched with the sensor equivalent capacitance. In figure 3.1 the input capacitances are both equal to C_0 for commodity of representation.

The closed-loop mid band gain is fixed by the ratio between the input capacitance and the feedback capacitance.

$$|gain| = \frac{C_0}{C_f}$$

This expression is only theoretic because R_{bias} is large but finite and it introduces parasitic capacitances that change the equivalent capacitance in the feedback loop. Moreover, as it is shown in the following paragraphs, the value of C_0 that guarantees input matching is not immediately calculated. A gain of 9.5dB is required and this is obtained with $C_f = 720\text{fF}$.

The used technology is a CMOS process. The n-MOS are built directly in the p-doped substrate, while p-MOS are create inside an n-well. It is also possible to realize n-MOS in a triple well structure, allowing an arbitrary bulk connection.

3.2 Operational transconductance amplifier (OTA)

3.2.1 Design of a low noise low power OTA

The OTA is the core of the amplifier. It provides an output current proportional to the differential voltage between its inputs.

The current mirror OTA topology is implemented, figure 3.3. Thanks to its one-stage configuration, the chosen OTA has a good power efficiency. A differential pair is used as input stage to reject common mode disturbs and a cascode scheme realizes the output stage increasing both the output resistance and the gain.

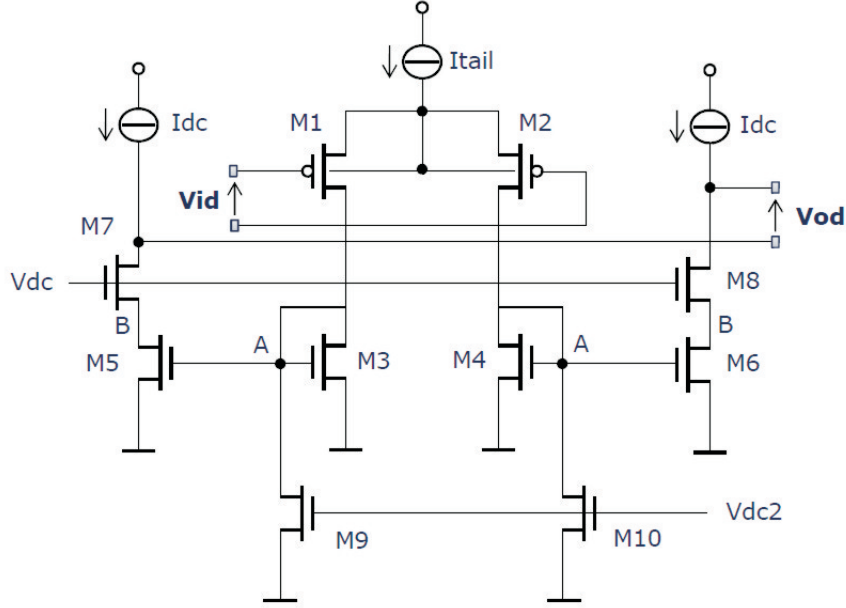


Figure 3.3: OTA schematic

The differential pair input transistors M_1 and M_2 are p-channel devices allowing a lower flicker noise. Another reason why a p-Mos input has better performance than a n-MOS input is that the p-MOS are built in a n-well which shields disturbs from the p-substrate. Besides, it is possible to avoid the Body effect connecting bulk with source.

The operational amplifier should achieve the lowest overall noise. This is the reason why a noise analysis is required to design a low noise OTA. In this analysis the current sources are considered as ideal, as well as, transistors $M_{9,10}$. The total input referred noise is calculated by adding all the input referred noise sources. In this way, the amplifier noise can be modelled as an input referred voltage noise source v_{geq} considering the equivalent single-ended half circuit, as can be observed in figure 3.4.

The analysis starts from the calculation of the input referred gate voltage noise v_{gcs} , generated by the cascode output of figure 3.5.

Considering the transistor M_5 and M_7 , the input referred power spectral density (PSD) S_{vgcs} , in V^2/Hz , is given by the sum of the PSD of the two

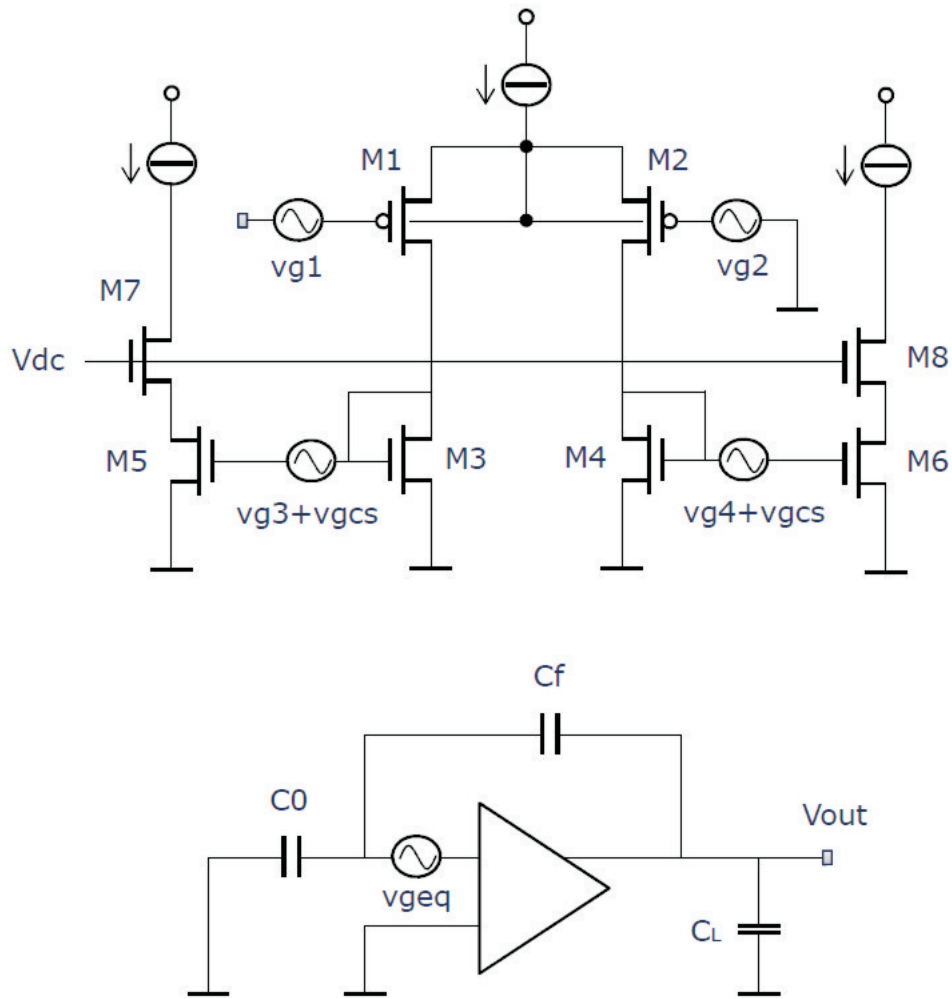
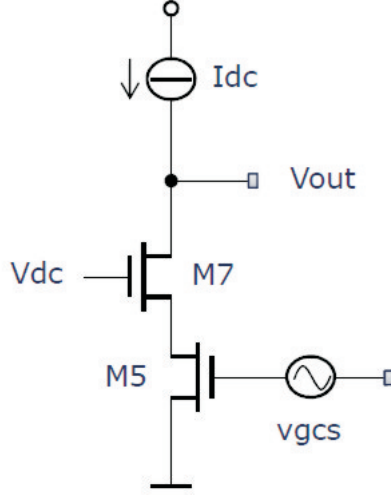


Figure 3.4: *The OTA with its voltage noise source*

Figure 3.5: *The cascode output and its input gate noise voltage*

transistors, S_{vg5} and S_{vg7} , referred to the cascode input. S_{vg5} is already referred at the input, the problem is to refer S_{vg7} . This is obtained multiplying S_{vg7} with the square of the transfer function between the gate of M_7 and the gate of M_5 . The transfer function between the gate of M_7 and the output is $-R_o/r_{o5}$, where R_o is the cascode output resistance and r_{o5} is the output resistance of M_5 . In fact, it is possible to see M_7 as a common source with source degeneration through M_5 . The cascode stage transfer function is $-g_{m5}R_o$ and calling S_{vgi} the gate voltage power spectral density (PSD) of the transistor M_i , the following result is obtained:

$$S_{vgcs} = S_{vg5} + \left(\frac{R_o}{g_{m5}r_{o5}R_o} \right)^2 S_{vg7} = S_{vg5} + \left(\frac{1}{g_{m5}r_{o5}} \right)^2 S_{vg7}$$

Therefore, assuming $g_{m5}r_{o5} \rightarrow \infty$ the contribution of the cascode transistor M_7 becomes negligible, hence, it can be neglected writing $S_{vgcs} = S_{vg5}$. S_{vgcs} is then added to S_{vg3} , the same is valid in the other matched branch where S_{vgcs} is added to S_{vg4} .

Now it remains the noise analysis of the differential pair. Assuming that M_1 and M_2 are matched, they have the same transconductance $g_{m1,2}$, a similar assumption is taken for M_3 and M_4 with transconductance $g_{m3,4}$, thus the amplifier input referred voltage noise source is given by:

$$S_{vgeq} = S_{vg1} + S_{vg2} + \left(\frac{g_{m3,4}}{g_{m1,2}} \right)^2 (S_{vg3} + S_{vg4} + S_{vg5} + S_{vg6})$$

where $S_{v_{gi}}$ is the sum between the thermal and flicker noise contribution $S_{v_{gi_thermal}}$ and $S_{v_{gi_flicker}}$ respectively.

It is useful to approximate the gate voltage PSD as function of the parameters that should be design [7], such as width W, length L and biasing current I_D :

$$S_{v_{gi_thermal}} \simeq \frac{K_{th}}{g_{mi}} \quad S_{v_{gi_flicker}} \simeq \frac{K_{fl}}{W_i L_i f}$$

Substituting these approximations for the PSD in the previous relation an important result is obtained:

$$\begin{aligned} S_{v_{geq}} &\simeq \underbrace{2 \frac{K_{th1,2}}{g_{m1,2}} + 2 \left(\frac{g_{m3,4}}{g_{m1,2}} \right)^2 \left(\frac{K_{th3,4}}{g_{m3,4}} + \frac{K_{th5,6}}{g_{m5,6}} \right)}_{thermal} + \\ &+ \underbrace{2 \frac{K_{fl1,2}}{W_{1,2} L_{1,2} f} + 2 \left(\frac{g_{m3,4}}{g_{m1,2}} \right)^2 \left(\frac{K_{fl3,4}}{W_{3,4} L_{3,4} f} + \frac{K_{fl5,6}}{W_{5,6} L_{5,6} f} \right)}_{flicker} \\ &\simeq \frac{2}{g_{m1,2}} \left[K_{th1,2} + \left(\frac{g_{m3,4}}{g_{m1,2}} \right) K_{th3,4} + \left(\frac{g_{m3,4}^2}{g_{m1,2} g_{m5,6}} \right) K_{th5,6} \right] + \\ &+ \frac{2}{f} \left[\frac{K_{fl1,2}}{W_{1,2} L_{1,2}} + \left(\frac{g_{m3,4}}{g_{m1,2}} \right)^2 \left(\frac{K_{fl3,4}}{W_{3,4} L_{3,4}} + \frac{K_{fl5,6}}{W_{5,6} L_{5,6}} \right) \right] \end{aligned}$$

For matching reasons, M_5 and M_6 are matched with M_3 and M_4 so a current mirror ratio 1:1 is created. Consequently, $g_{m3,4} = g_{m5,6}$ and $S_{v_{geq}}$ can be simplified:

$$\begin{aligned} S_{v_{geq}} &\simeq \frac{2}{g_{m1,2}} \left[K_{th1,2} + \left(\frac{g_{m3,4}}{g_{m1,2}} \right) (K_{th3,4} + K_{th5,6}) \right] + \\ &+ \frac{2}{f} \left[\frac{K_{fl1,2}}{W_{1,2} L_{1,2}} + \left(\frac{g_{m3,4}}{g_{m1,2}} \right)^2 \left(\frac{K_{fl3,4}}{W_{3,4} L_{3,4}} + \frac{K_{fl5,6}}{W_{5,6} L_{5,6}} \right) \right] \end{aligned}$$

The thermal noise parameter K_{th} can be considered almost constant in every operative region. Therefore the thermal noise contribution can be minimized choosing $g_{m1,2}$ large and $g_{m3,4}$ small.

To achieve this condition, it is necessary to investigate the g_m behavior as function of the transistor operative zone [7]. The studies start from the weak inversion or subthreshold operation.

The expression of large signal drain current and g_m in weak inversion are reported [8].

$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) (1 + \lambda v_{DS})$$

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q = \frac{I_D}{nV_t}$$

where I_t is the drain current for $v_{GS} = V_T$ and $v_{DS} = 0$, V_T is the threshold voltage, v_{GS} and v_{DS} are the gate source and drain source voltage, V_t is the thermal potential, λ is the channel length modulation coefficient and n is the slope factor.

The slope factor n is very important for a transistor in weak inversion and it is equal to the inverse of the capacitive divider that the oxide and depletion layer capacitances, C'_{ox} and C'_p respectively, form:

$$n = \frac{C'_{ox} + C'_p}{C'_{ox}}$$

Whereas the large signal drain current i_D and g_m expressions in strong inversion are:

$$i_D = \frac{1}{2} \frac{W}{L} \mu C'_{ox} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q = \sqrt{2I_D \mu C'_{ox} \frac{W}{L}}$$

where μ is the carrier mobility and C'_{ox} is the gate oxide capacitance per unit area. Figure 3.6 illustrates the behavior of i_D over v_{GS} in the two considered operative regions.

Afterwards it is possible to compare the analytic expression of the ratio g_m/I_D in weak and strong inversion:

$$\text{weak inversion : } \frac{g_m}{I_D} = \frac{1}{nV_t}$$

$$\text{strong inversion : } \frac{g_m}{I_D} = \sqrt{\frac{2\mu C'_{ox} (W/L)}{I_D}}$$

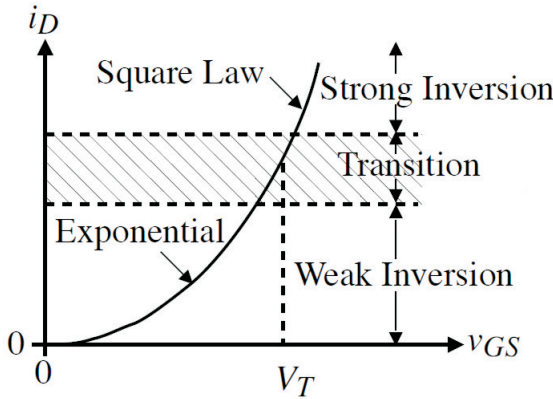


Figure 3.6: Different model for i_D as function of the operative region

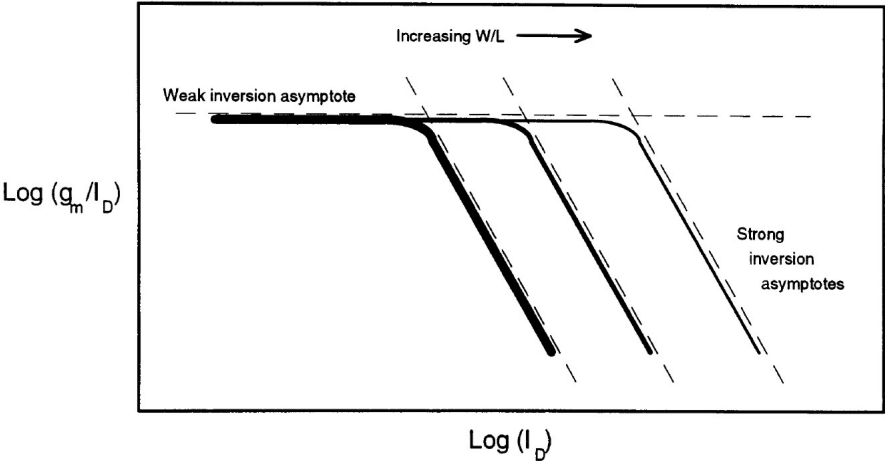


Figure 3.7: g_m/I_D ratio over I_D in logarithmic scale

Figure 3.7 shows the ratio g_m/I_D as function of I_D . This diagram suggests that in weak inversion the largest g_m is achieved for a given drain current I_D .

Having these results, a low thermal noise amplifier is obtained if the input transistor M_1 and M_2 are working in weak inversion, where they have a large $g_{m1,2}$, while M_3 and M_4 are operating in strong inversion with a small $g_{m3,4}$. This imposition will also reduce the flicker noise.

Furthermore, the parameter that sets the limit between weak inversion and strong inversion operation at a specified drain current is the W/L ratio. The following expression justifies this result, where i_T is the bound current between the two operative regions. To find i_T , $v_{GS} - V_T$ are compared in the two regions [8]

- *weak inversion* :

$$v_{GS} - V_T \simeq nV_t \ln \left(\frac{i_D}{I_t(W/L)} \right) \simeq nV_t \left(1 - \frac{I_t(W/L)}{i_D} \right) \quad \text{if } 0.5 < \frac{i_D}{I_t(W/L)}$$
- *strong inversion* :

$$v_{GS} - V_T \simeq \sqrt{\frac{2i_D}{\mu C'_{ox}(W/L)}}$$

Therefore:

$$\begin{aligned} nV_t \left(1 - \frac{I_t(W/L)}{i_T} \right) &= \sqrt{\frac{2i_T}{\mu C'_{ox}(W/L)}} \\ n^2 V_t^2 \left(1 - \frac{I_t(W/L)}{i_T} \right)^2 &= \frac{2i_T}{\mu C'_{ox}(W/L)} \\ n^2 V_t^2 \left(\frac{I_t^2(W/L)^2}{i_T^2} - \frac{2I_t(W/L)}{i_T} + 1 \right) &\simeq n^2 V_t^2 = \frac{2i_T}{\mu C'_{ox}(W/L)} \end{aligned}$$

where first order approximations are used. Rearranging the terms, the expression of i_T is obtained:

$$i_T = \frac{1}{2} \frac{W}{L} \mu C'_{ox} V_t^2 n^2$$

Thus, the operative region is set by the W/L ratio, and subthreshold operation can occur at large currents for large values of W/L.

Since M_1 and M_2 are operating in weak inversion, their biasing current $I_{D1,2}$ should be large to reduce their thermal noise, this means also a large transconductance. In fact, in subthreshold their PSD is equal to:

$$S_{vg1,2,thermal} \simeq \frac{K_{th1,2}}{g_{m1,2}} = \frac{K_{th1,2}nV_t}{I_D}$$

After choosing the transistor biasing current I_D , taking in account that the power consumption is proportional to this current, it is possible to make them work in subthreshold operation or strong inversion by setting an oportune W/L ratio. So, a large W/L ratio is needed for the input differential pair transistor, and this is achieved putting more transistor in parallel. On the other hand, a small W/L ratio is request to M_3 and M_4 . Afterwards it is possible to scale the area WL of each transistor in order to achieve the flicker noise contribution within the specifics.

Furthermore, to have a larger decrease on $g_{m3,4}$, a biasing current reduction is made up on transistors M_3 and M_4 . In fact, a significant part of the current in M_1 and M_2 flows through M_9 and M_{10} , that are also part of the common mode feedback circuit. This technique allows also a gain increase of the OTA as is explained in [5].

However, without current reduction, $I_{D1} = I_{D3} = I_{D5} = I_{D7}$ and the low frequency OTA voltage gain A_0 is given by:

$$\begin{aligned} A_0 &= g_{m1}R_0 = \frac{I_{D1} r_{07}(1 + g_{m7}r_{05})}{nV_t} \frac{1}{2} \simeq \frac{I_{D1} r_{07}g_{m7}r_{05}}{nV_t} \frac{1}{2} = \\ &= \frac{I_{D1}}{nV_t} \frac{1}{2\lambda_7 I_{D7}} \frac{1}{V_{GS7} - V_{T7}} \frac{1}{\lambda_5 I_{D5}} = \frac{I_{D1}}{nV_t \lambda_7 \lambda_5 (V_{GS7} - V_{T7})} \end{aligned}$$

where the transistor M_5 and M_7 are supposed to operate in strong inversion and all the current source are cascode mirror, hence, R_0 is multiplied with 1/2 to take in account the resistance of the current source I_{dc} . With a current reduction technique, a voltage gain improvement is possible. Setting $I_{D9} = kI_{D1}$, where $I_{D1} = I_{tail}/2$, $I_{D5} = I_{D5} = I_{dc} = I_{D3} = (1 - k)I_{D1}$ is obtained. Therefore:

$$\begin{aligned} A_{0,en} &= g_{m1}R_0 \simeq \frac{I_{D1} r_{07}g_{m7}r_{05}}{nV_t} \frac{1}{2} = \frac{I_{D1}}{nV_t} \frac{1}{\lambda_7 I_{D7}} \frac{I_{D7}}{V_{GS7} - V_{T7}} \frac{1}{\lambda_5 I_{D5}} = \\ &= \frac{I_{dc}}{nV_t(1 - k)} \frac{1}{\lambda_7 I_{dc}} \frac{1}{I_{dc}} \frac{1}{1} = \frac{A_0}{1 - k} \end{aligned}$$

As it is shown, the factor $1/(1 - k)$ improves the gain.

To reduce the thermal noise, I_{tail} is set to $90\mu A$, comorting $I_{D1} = I_{D2} = 45\mu A$. While setting the cascode biasing current I_{dc} , it's important to take in account that from this current will depend the differential slew rate (SR) of the amplifier:

$$SR = \frac{2I_{dc}}{C_L}$$

where C_L is the op amp load capacitance. This capacitance is usually quite large, therefore, I_{dc} cannot be so small if a good SR is needed.

Furthermore, the current reduction technique increases the impedance of the node A, shifting the pole associated to it. Hence, the factor k should be define taking in account also stability problems, as it is reported in the stability paragraph.

For these reasons, $I_{dc} = 8.5\mu A$. Thus, $k = 0.81$ and a gain improvement of 14.4dB is achieved.

With a load capacitance $C_L = 154pF$, an $SR = 110KV/s$ is obtained.

In order to keep the cascode transistor noiseless, the term $g_{m5,6}r_{o5,6}$ must be quite large. Since $g_{m5,6} = g_{m3,4}$ should be small, it is possible to satisfy the assumption making $r_{o5,6}$ large by setting a big $L_{5,6} = L_{3,4}$, due to the fact that $\lambda \propto 1/L$. This agrees with the previous results of choosing a small W/L ratio for the transistor M_3 and M_4 .

The cascode biasing voltage V_{dc} must be large enough to make M_7 and M_8 work in saturation.

3.2.2 Stability

Since the amplifier includes three poles, the study of its stability is not a trivial task. The starting point is the determination of the loopgain $T(s)$, then it is possible to apply the Bode method. From the theory $T(s) = \beta A(s)$, where $A(s)$ is the OTA voltage gain including the feedback load effects and β is the feedback factor.

A careful analysis shows that in the reality:

$$\beta = \beta(s) = \frac{1 + sR_{bias}C_f}{1 + R_{bias}(C_f + C_0 + C_x)}$$

where C_x includes the parasitics capacitances at the op amp input node. Due to the biasing resistor R_{bias} , the feedback factor is not constant over frequency. However, R_{bias} is a very high resistance in the order of tens $G\Omega$ and a simplification can be carried out. In fact, the pole-zero pair in $\beta(s)$ are very close each other, since C_f is more or less one third of C_0 and C_x is a parasitics capacitance, usually small. With the these design parameters, the zero-pole pair in $\beta(s)$ acts in the order of few Hz. Therefore, for frequencies high enough, it is possible to assume:

$$\beta(s) \simeq \beta(\infty) = \frac{C_f}{C_f + C_0 + C_x}$$

It is useful to separate the term $A(s)$ in a Bode form:

$$A(s) = \frac{g_{m1,2}R_0}{(1-k)(1+sR_AC_A)(1+sR_BC_B)(1+sR_0C_0)}$$

where R_A and C_A are the resistances and capacitance of the current mirror saw at the node A. R_B and C_B are the resistances and capacitance of the cascode saw at the node B. Analogous definitions are valid for R_0 and C_0 referred at the cascode output. Consequently, the system is a third order one with the poles:

$$\omega_A = \frac{1}{R_AC_A} \quad \omega_B = \frac{1}{R_BC_B} \quad \omega_0 = \frac{1}{R_0C_0}$$

To understand from which parameters depend the frequency of the poles, it is useful to rewrite ω_A , ω_B and ω_0 as function of the design parameters:

$$\begin{aligned} R_A &= \frac{1}{g_{m3,4}} & C_A &\simeq 2C_{gs3,4} + C_{db3,4} \\ R_B &= \frac{1}{g_{m7,8}} & C_B &\simeq C_{gs7,8} + C_{sb7,8} + C_{db5,6} \\ R_0 &= \frac{r_{o7,8}(1 + g_{m7,8}r_{o5,6})}{2} & C_0 &\simeq C_{db7,8} + C_{dg7,8} + (1 - \beta)C_f + C_L \end{aligned}$$

where C_{db} is the drain-bulk capacitance, C_{sb} is the source-bulk capacitance, C_{dg} is the drain-gate capacitance and C_{gsi} is the gate-source capacitance. A decreasing of $g_{m3,4}$ and $g_{m7,8}$, thus, an increasing of R_A and R_B respectively, is caused by the current reduction technique explained before.

It seems that $\omega_A \simeq \omega_B$. Since $M_{3,4}$ and $M_{7,8}$ have the same biasing current, $g_{m3,4} \simeq g_{m7,8}$. However, to make $M_{7,8}$ noiseless, it was set a large $L_{5,6} = L_{3,4}$. Thus, dimensioning:

$$W_{7,8}L_{7,8} \ll W_{3,4}L_{3,4} \quad \implies \quad C_{gs7,8} \ll C_{gs3,4}$$

The C_{gs} capacitance usually dominates C_A and C_B , therefore:

$$\omega_A \ll \omega_B$$

With this result and assuming that ω_c , where $|T(j\omega_c)| = 1$, is placed between ω_0 and ω_A , is possible to neglect ω_B in the study of the stability. Hence:

$$A(s) \simeq \frac{g_{m1,2}R_0}{(1-k)(1+sR_AC_A)(1+sR_0C_0)}$$

The system is stable with a good phase margin (PM) only if there is sufficient frequency separation between the two poles. In other words, the system must have a dominant pole ω_{pd} and, consequently, a non-dominant pole ω_{pnd} . Now, it is possible to write:

$$R_0 \gg R_A \quad \text{and} \quad C_0 \gg C_A$$

It's easy to prove these relations, since a cascode output resistance is much bigger than a diode connected transistor resistance. Then, the second relation is justified by the fact that the load capacitance C_L is larger than the transistor parasitics capacitance. Therefore:

$$\omega_0 = \omega_{pd} \quad \text{and} \quad \omega_A = \omega_{pnd}$$

A calculation of the phase margin (PM) is performed. From the theory:

$$\text{PM} = 180^\circ - \angle T(j\omega_c) \quad \text{where} \quad |T(j\omega_c)| = 1$$

Furthermore, it is possible to approximate ω_c with $\omega_c \simeq T_0\omega_{pd}$, where T_0 is the loopgain at low frequency, for the reason that the product gain-bandwidth is constant in a -20dB/dec slope. Thus, assuming a large enough T_0 , the dominant pole contributes for -90° at ω_c and the PM can be estimated in this way:

$$\text{PM} = 90^\circ - \arctan\left(\frac{\omega_c}{\omega_{pnd}}\right)$$

This means that the PM depends only on the ratio ω_c/ω_{pnd} . Having ω_c it is possible to estimate the PM.

The previous approximation allows the following expression:

$$\omega_c \simeq T_0\omega_{pd} = \beta \frac{g_{m1,2}R_0}{(1-k)R_0C_0} = \beta \frac{g_{m1,2}}{(1-k)C_0}$$

where

$$\beta = \frac{C_f}{C_f + C_0 + C_x} \quad \text{with} \quad C_x \simeq C_{gs1,2}$$

Hence:

$$\omega_c \simeq \beta \frac{g_{m1,2}}{(1-k)[C_{ab7,8} + C_{dg7,8} + (1-\beta)C_f + C_L]}$$

Finally, substituting the approximation of ω_c and ω_{pnd} in the formula calculated for the phase margin, an evaluation of it is obtained as function of the design parameter.

The table 3.1 reports the PM relative to a specific ω_{pnd}/ω_c ratio. In many case, a ratio ≥ 3 gives enough PM.

ω_{pmd}/ω_c	PM
1	45°
2	63°
3	72°
4	76°
5	79°

Table 3.1: The Phase Margin relative to a certain ω_{pmd}/ω_c ratio

3.2.3 Common mode feedback (CMFB)

A fully differential operational amplifier has larger output swing than a single-ended configuration. However, a common mode feedback is needed in a fully differential circuit to set the common mode output voltage V_{oc} , equal to a reference voltage V_{ref} , in order to maximize the output signal swing. In the design, $V_{ref} = V_{DDLDO}/2$ is set. This circuit works sensing V_{oc} at the op amp and, thanks to a negative feedback, forces this voltage to a value close to V_{ref} , with a certain error. Figure 3.8 shows the common mode feedback circuit.

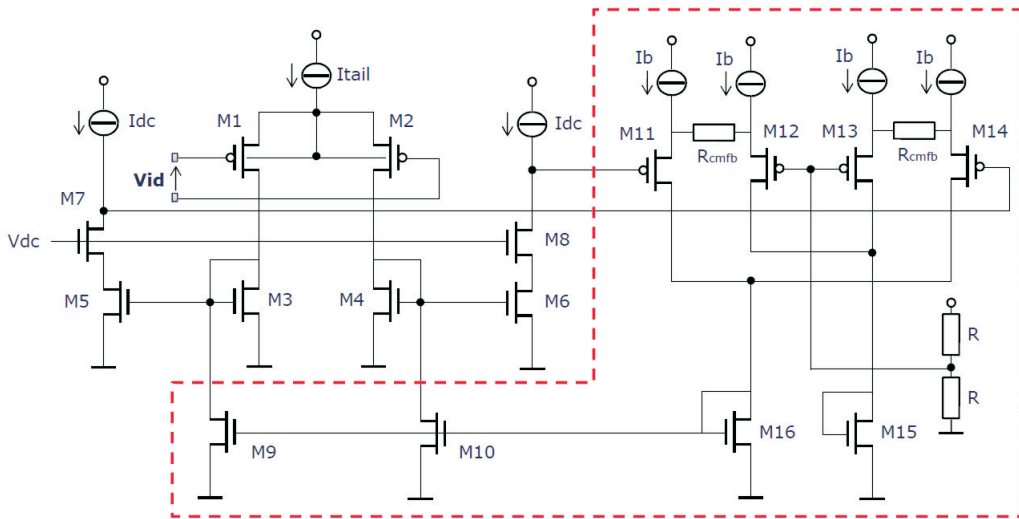


Figure 3.8: The common mode feedback circuit

The CMFB uses two matched differential pairs that sense and compare V_{oc} with V_{ref} . Then, the difference between them is kept small by adjusting the biasing current of the OTA transistors M_3 , M_4 and, hence, of the output cascode.

Non-idealities in the CMFB can affect the common mode and differential mode signals of the op amp [6]. Thus, to improve the linearity of the CMFB differential pairs, degeneration resistors R_{cmfb} are used. The same result can be obtained by using transistor M_{11-14} with a large channel length. However, the advantage of using degeneration resistors is to avoid an introduction of large capacitances, created by long channel devices.

A degeneration resistor also creates a g_m lowering of the transistor M_{11-14} , in fact:

$$g_{m11} \longrightarrow \frac{g_{m11}}{1 + g_{m11}(R_{cmfb}/2)}$$

The low frequency gain in the CMFB loop, $T_{0,cmfb}$, can be expressed in the following way [2] :

$$T_{0,cmfb} = A_{cmc}A_{cms}$$

where A_{cmc} is the part associated with the OTA and A_{cms} is related to the CMFB circuit. Therefore:

$$A_{cms} = \frac{g_{m11}}{1 + g_{m11}(R_{cmfb}/2)} \frac{1}{g_{m16}}$$

The result is that $T_{0,cmfb}$ depends on degeneration resistance R_{cmfb} .

The CMFB loopgain $T_{cmfb}(s)$ contains several poles, and the dominant pole is related to the part of the OTA. However, R_{cmfb} has no influence in these poles, but only in the low frequency loopgain. Hence, the unity-gain frequency and, consequently, the phase margin can be set by this resistor.

3.3 Frequency response

The closed-loop transfer function $H(s)$ is given by the following formula:

$$H(s) = \frac{V_{od}}{V_{id}} = \frac{A(s)}{1 + \beta(s)A(s)}$$

In order to find the high cut-off frequency, $\omega_H = 2\pi f_H$, $\beta(s) = \beta(\infty)$ is assumed. Furthermore, $A(s)$ is approximated by:

$$A(s) \simeq \frac{A_0}{1 + s/\omega_{pd}}$$

Hence, ω_H can be estimated with $\omega_H \simeq \omega_c$, where ω_c is calculated in the stability paragraph.

$$\omega_H = 2\pi f_H \simeq \omega_c \simeq \beta \frac{g_{m1,2}}{(1-k)[C_{db7,8} + C_{dg7,8} + (1-\beta)C_f + C_L]}$$

C_L is much bigger than the other capacitances, thus:

$$\omega_H \simeq \beta \frac{g_{m1,2}}{(1-k)C_L}$$

Now, the low cut-off frequency f_L remains to be calculated. This time it is not possible to consider $\beta(s)$ constant over frequency but its complete expression must be used:

$$\beta(s) = \frac{1 + sR_{bias}C_f}{1 + sR_{bias}(C_f + C_0 + C_x)}$$

At low frequency, where $f \ll f_H$, $A(s)$ can be considered constant and quite large, therefore, $H(s) \simeq 1/\beta(s)$. Afterwards, it's easy to prove that f_L is set by the feedback impedance:

$$\omega_L = 2\pi f_L = \frac{1}{R_{bias}C_f}$$

Figure 3.9 summarized the results.

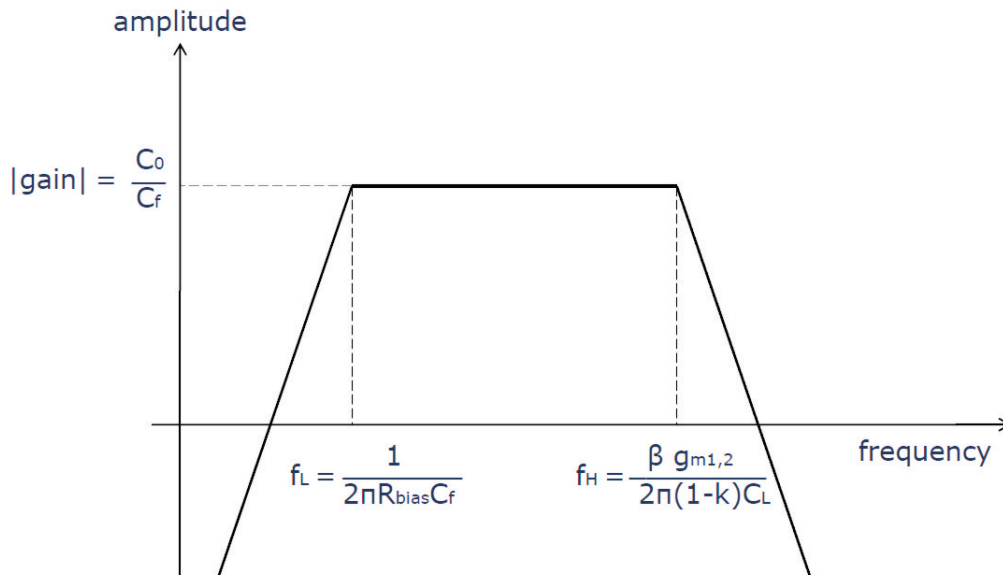


Figure 3.9: The amplifier closed-loop transfer function over frequency

3.4 Global noise analysis

In this paragraph, a global noise analysis is performed. The total output voltage noise power V_{no}^2 and the output voltage noise V_{no} are calculated. The total noise of the operational amplifier is generated by the OTA and the feedback resistors R_{bias} , as it is shown in figure 3.10.

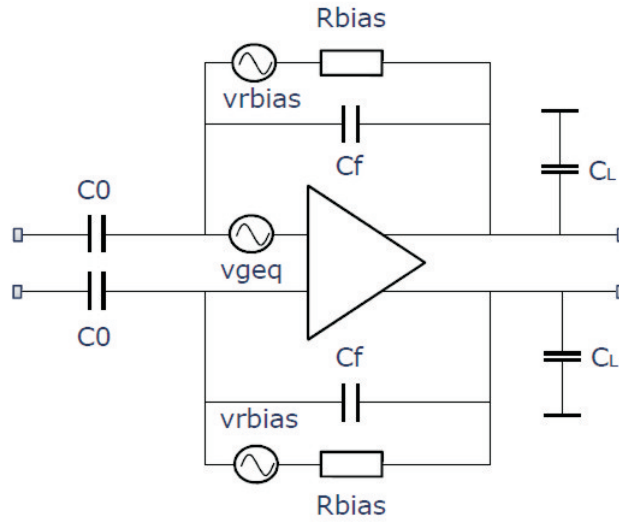


Figure 3.10: *The operational amplifier with its noise source*

A calculation of the OTA noise contribution is already performed. Its input referred voltage PSD, $S_{v_{geq}}$, was found. Writing as $S_{v_{o.OTA}}$ the output noise voltage PSD related to the OTA, the following result is obtained:

$$S_{v_{o.OTA}} = \left| \frac{A(j2\pi f)}{1 + \beta(j2\pi f)A(j2\pi f)} \right|^2 S_{v_{geq}}$$

As every resistor, R_{bias} introduces thermal noise. To evaluate its output noise contribution, a R_{bias} noise analysis is performed. Its voltage PSD is given by:

$$S_{v_{R_{bias}}} = 4KT R_{bias}$$

where K is the Boltzmann constant and T the absolute temperature. The problem now is to refer this contribution at the op amp output. This is obtained by writing:

$$S_{vo-Rbias} = \left| \frac{1}{(1 + jf/f_L)(1 + jf/f_H)} \right|^2 S_{vRbias}$$

Calling S_{vo} the total output PSD, it is possible to write:

$$S_{vo} = S_{vo-OTA} + S_{vo-Rbias}$$

The output noise voltage power V_{no}^2 is then calculated with an integration of the PSD, whereas, the output noise voltage V_{no} is its square root value:

$$\begin{aligned} V_{no}^2 &= \int_0^{+\infty} S_{vo} df = \int_{f_L}^{f_H} S_{vo} df \\ V_{no} &= \sqrt{V_{no}^2} = \sqrt{\int_{f_L}^{f_H} S_{vo} df} \end{aligned}$$

3.5 Biasing resistor R_{bias}

Biasing resistors R_{bias} are used to provide a DC path to the op amp input floating nodes. These are n-MOS pseudo resistors that create a very high ohmic impedance when the cross voltage is close to zero [3][4]. They are realized by a triple well n-MOS transistor with gate-drain and bulk-source connection. A series of three n-MOS pseudo resistor is used so that the output signal linearity can be improved.

Furthermore, a series of three n-MOS with gate-drain and bulk-drain is added in parallel to the previous series, in order to speed up the shock recovery transient, as it is illustrated in figure 3.11. A fast shock recovery is needed when an unwanted voltage impulse is applied to the input floating nodes of the op amp, to bring back the system in nominal operative conditions in short time.

Anyway, this will speed up the shock recovery transient but will decrease the global resistance R_{bias} .

To allow a bulk connection different from ground, triple-well devices are requested. The n-well is connected to the voltage supply in order to reduce the effects of parasitic diodes that are present in the bulk-well and substrate-well interface.

3.6 Input matching

As discussed before, the capacitive sensor is placed in one of the operational amplifier inputs, therefore, the other input must be matched to it. From a theoretical point of view, a matching condition is reached when there is no interaction between the differential mode and common mode signals.

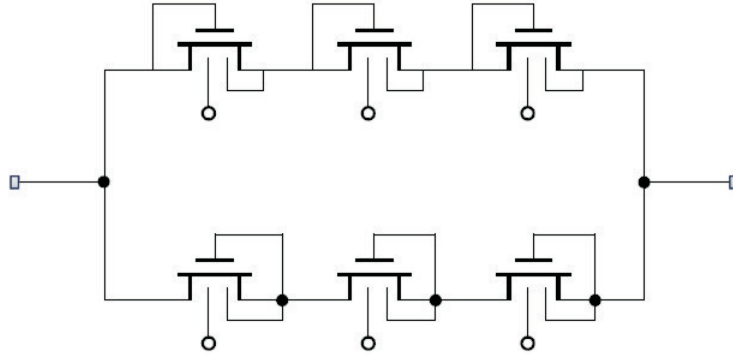


Figure 3.11: *The implementation of R_{bias}*

In the real design, an empirical rule is used to define a matching condition. In fact, when the design reaches this condition, the two branches of the amplifier are completely symmetrical. Thus, considering a disturb in the supply voltage, the amplifier branches produce the same single-ended output voltage. Consequently, the differential output voltage will be almost constant. In other words, the design is matched when it shows a large power supply rejection ratio (PSRR).

Since the sensor capacitance C_{main} and C_p are fixed for a given sensor model, a matching condition is obtained when the chosen value for C_0 guarantees a large PSRR. Besides, the amplifier noise performances are affected by the input matching, since a noise increase is registered when there is no matching. In addition to, the noise generated by the amplifier is proportional to the reached matching condition. So a good matching condition is very important for an high performance system. However, it is difficult to relate the output noise to the matching obtained by varying C_0 because the amplifier gain depends also on it.

As shown in figure 3.12, the PSRR near matching condition is very sharp, this means that the PSRR has a large sensitivity on C_0 variation.

Mismatch due to process variation are quite likely, hence the value of C_0 in matching condition is unknown. So, a trimming system is needed to change this value within an opportune range. However, the aforementioned system is create only for test-chip purpose. It creates a varying capacitance by adding capacitances connected in parallel.

Figure 3.13 shows the schematic of the trimming system, where C_{0min}

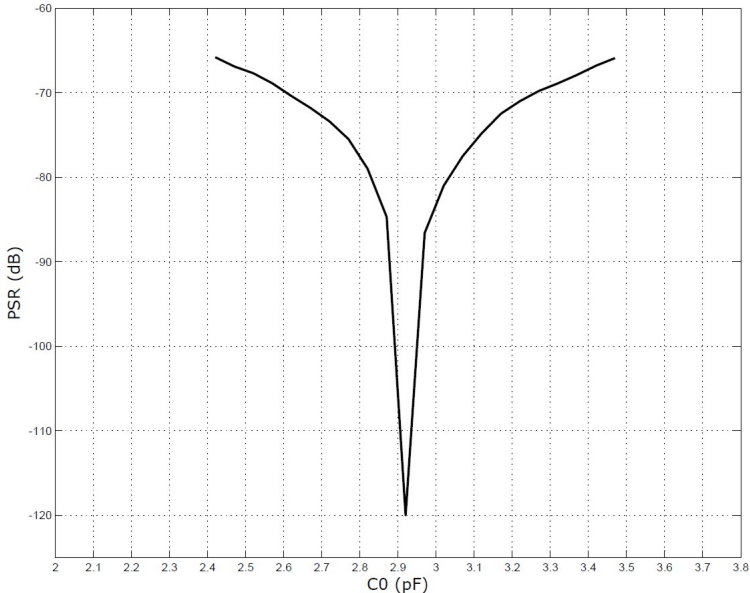


Figure 3.12: Differential Power Supply Rejection @ 217Hz over C₀

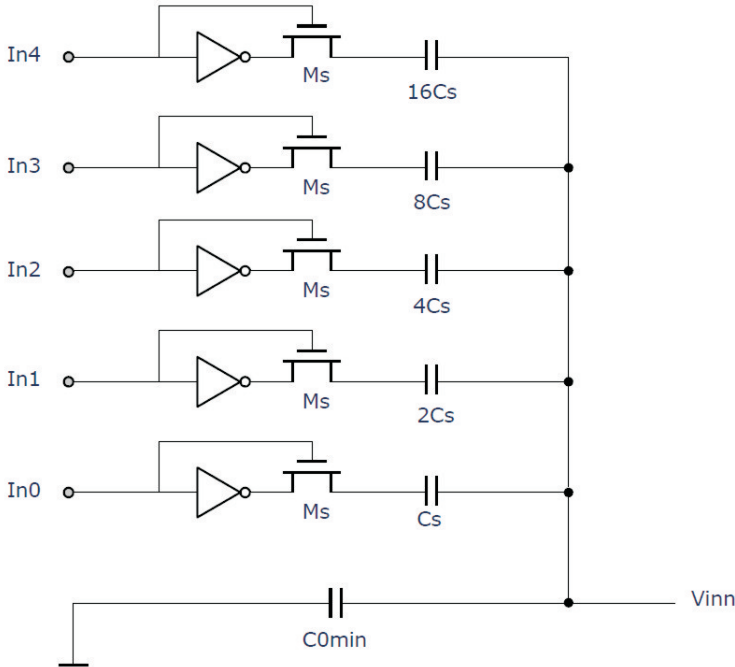


Figure 3.13: The input trimming system

is always connected to the input, therefore, it is the minimum achievable capacitance. Whereas, the maximum capacitance is given by:

$$C_{0max} = C_{0min} + \sum_{i=0}^4 2^i C_s = C_{0min} + C_s \sum_{i=0}^4 2^i = C_{0min} + 31C_s$$

that is obtained closing all the switches and consequently by summing all the capacitances present in the system.

Obviously, the step with which is possible to vary the capacitance is C_s and the range is equal to $31C_s$.

The sensor capacitances, C_{main} and C_p , are given with a 20% of tolerance. Whereas, the on-chip capacitances, such as C_{0min} and C_s , can vary for the 10% of their nominal values. Therefore, the matching depends on these variations.

Since the sensor capacitances are connected in parallel, the lower matching condition is obtained when both C_{main} and C_p have a -20% of variation from the nominal capacitances. Obviously, a variation of +20% in the sensor capacitances creates the upper matching condition. Figure 3.14 illustrates these cases. The values of C_0 that guarantee match in these two cases are C_{0min}^* and C_{0max}^* respectively.

The range of the trimming system must cover the upper and the lower matching also in presence of a variation on its capacitances C_s and C_{0min} . As a result, the trimming system parameter must satisfy these relations calculated in worst case (w.c.):

$$\begin{aligned} C_{0min}(w.c.) &= C_{0min} + 10\%C_{0min} = 1.1C_{0min} < C_{0min}^* \\ C_{0max}(w.c.) &= C_{0min} + 31C_s - 10\%(C_{0min} + 31C_s) = 0.9(C_{0min} + 31C_s) > C_{0max}^* \end{aligned}$$

Having a limited number of digital signals to control the trimming system, C_s is chosen as the minimum value that satisfies these relations and C_{0min} in order to center the range of variation.

From the figure 3.14:

$$\begin{aligned} C_{0min}^* &\simeq 2.4pF \quad \text{and} \quad C_{0max}^* \simeq 3.5pF \\ C_{0max}^* - C_{0min}^* &\simeq 1.1pF \end{aligned}$$

The worst case range of variation should be bigger than this value:

$$\begin{aligned} C_{0max}(w.c.) - C_{0min}(w.c.) &= 0.9(C_{0min} + 31C_s) - 1.1C_{0min} = \\ &0.9 * 31C_s - 0.2C_{0min} > 1.1pF \end{aligned}$$

A value of C_{0min} that satisfies the lower limit in worst case with a certain margin is 1.9pF, then $C_s = 75fF$ satisfies also the last relation, giving:

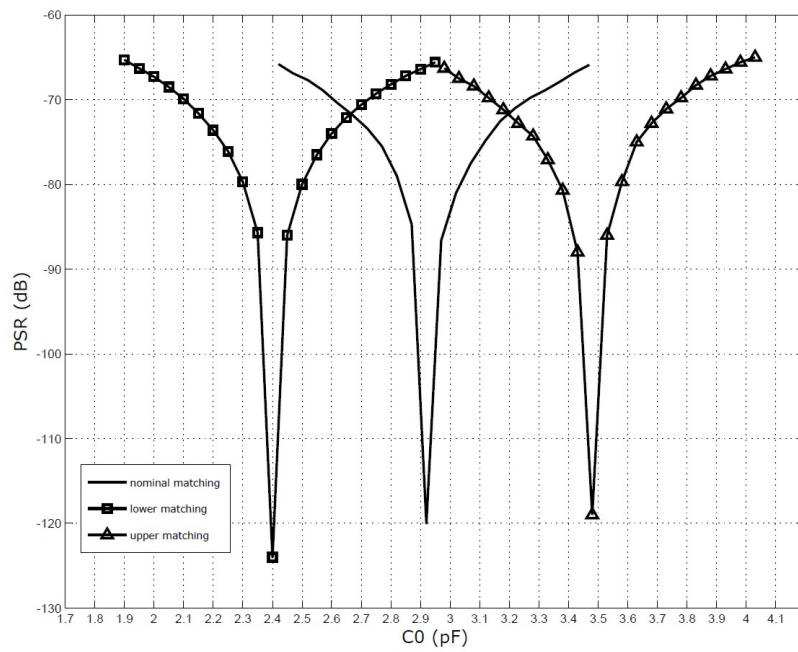


Figure 3.14: *The matching condition shifting as result of sensor parameters variation*

$$C_{0min}(w.c.) = 2.09pF \quad \text{and} \quad C_{0max}(w.c.) = 3.80pF$$

Hence, the trimming range is symmetric and it satisfies the requirements.

The gate of the switches M_s is directly driven by the control signal, whereas, the source is driven by the inverse of this signal. A source ground connection is also possible, but, in this case the trimming system introduces noise. In fact, when the switch M_s is open, its gate source voltage is equal to zero. The node V_{inn} has small fluctuation depending on the input signal and since the respective capacitance is connected to this node, a current has to flow across the branch where there is an open switch with a theoretic infinite resistance. Thus, M_s generates noise.

The solution presented avoids this problem because when M_s is open, its gate-source voltage is negative with amplitude equal to the supply voltage.

3.7 Start up behavior

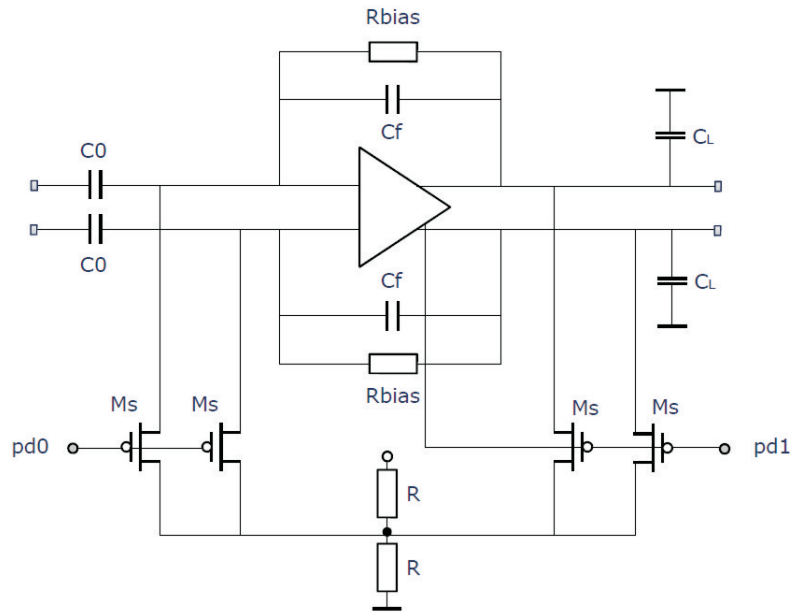
The amplifier includes high ohmic nodes that need to be charged at the correct operative point during an initial period of functioning, called start up. During this transient all the impedance are reduced in order to speed up the process. An adequate circuit creates the condition of lowering the circuit impedance.

Without start up circuit, the operative point is reached in a long time. Therefore, the start up circuit has to connect these high ohmic nodes to the biasing voltage throw a low ohmic path for a determinate period of time. Then the nodes must be released, starting the normal operation of the amplifier.

The input and the output nodes of the operational amplifier are high ohmic, hence, they must be charged during start up. The solution presented in figure 3.15 allows this result by closing the switches M_s and connecting the nodes to a biasing voltage, which is the same voltage used as reference for the common mode feedback circuit and equal to half of V_{DDLDO} . At the same time all the biasing current of the OTA are equal to zero by setting $V_{GS} = 0$ to every current mirror transistor. In this way, the charging process can start.

Two control signals pd0 and pd1 are required for the start up circuit, or equally one signal and a delay block. In fact, first the output nodes should be released together with the OTA biasing control and, then, after an appropriate delay, the switches that control the input nodes can be opened.

If all the nodes and the OTA biasing are released at the same moment, a voltage step occurs at the input nodes. Since they are charged when no

Figure 3.15: *The start up circuit*

current is flowing in the differential pair, a unique releasing comports a different voltage bias for the input nodes during start up, with no current in the OTA, and during normal operation with OTA biased.

During normal operation after the start up transient, the operative point is kept constant by the common mode feedback circuit. The output nodes are directly connected to this system, whereas the input nodes are connected to the output nodes via the biasing resistors R_{bias} .

Chapter 4

Simulation results

The simulations are run with $V_{DD} = 1.8\text{V}$, temperature of 27°C and with a nominal technological process.

4.1 AC simulations

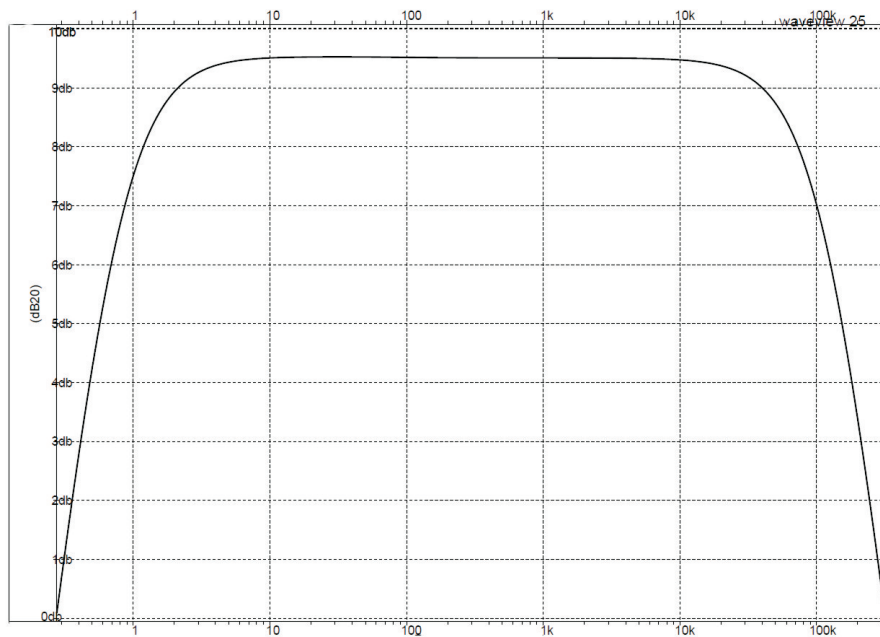


Figure 4.1: *The closed loop transfer function*

Figure 4.1 illustrates the transfer function $H(s)$ calculated in the previous chapter. The midband gain is correctly set to 9.5dB. The cut-off frequencies

at -3dB are:

$$f_L \simeq 0.7Hz \quad \text{and} \quad f_H \simeq 120KHz$$

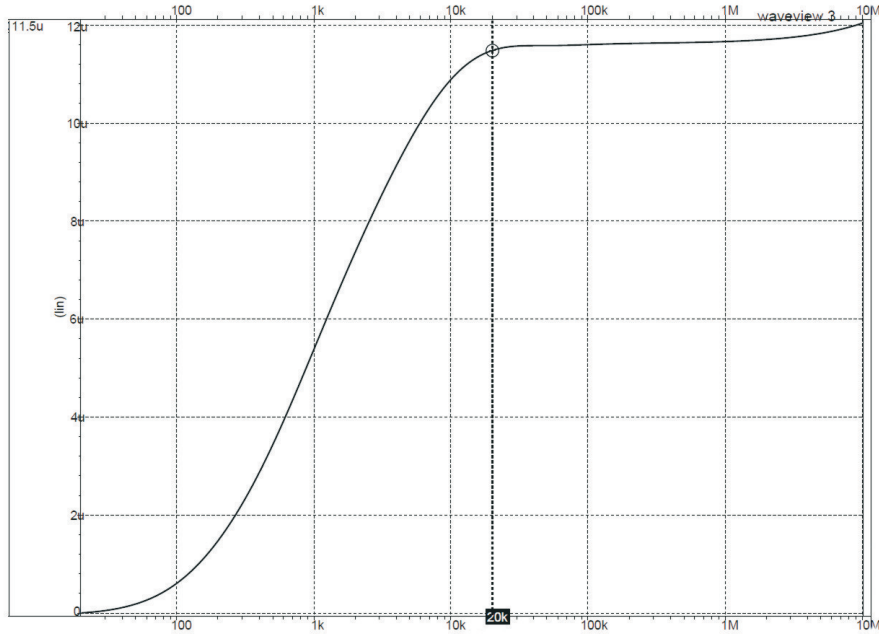


Figure 4.2: *A-weighted integrated output referred noise*

Figure 4.2 reports the A-weighted integrated noise output referred. In the audio band [20, 20000]Hz, a noise of $11.5\mu V_{rms}$ is obtained. Furthermore, the position of the high cut-off frequency comports a slight noise increment until 1MHz.

Stability issues of the operational amplifier are treated in paragraph 3.2.2. Here, figure 4.3, the Bode diagram of the amplifier loopgain is reported. It is possible to recognize a pole dominant behavior, with ω_{pd} placed around 10Hz. The non constancy registered before, it is due to the pole zero pair in $\beta(s)$, which confirms the approximations $\beta(s) \simeq \beta(\infty)$ for frequency $f \geq f_{pd}$ previously performed. A phase margin of 88° is achieved.

While setting the CMFB loopgain, two aspects are considered. First of all, the target is to obtain a large gain at low frequency. The second one is to achieve a good linearity, hence, degeneration resistors R_{cmfb} are introduced [6], even if this means a lower gain. Thus, the solution represents a compromise between the two aspects. From figure 4.4, a PM of 66° is obtained.

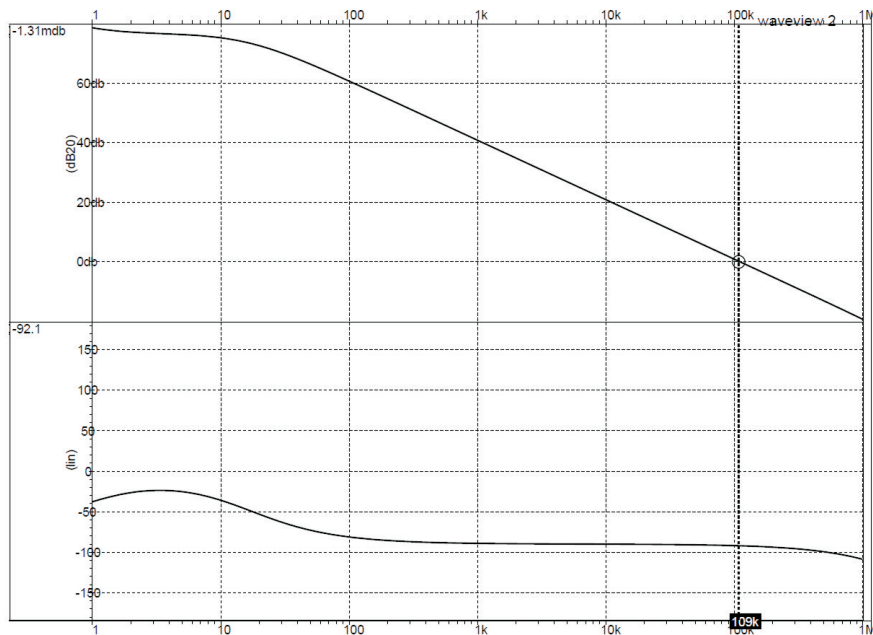


Figure 4.3: *Bode diagram of the amplifier loopgain*

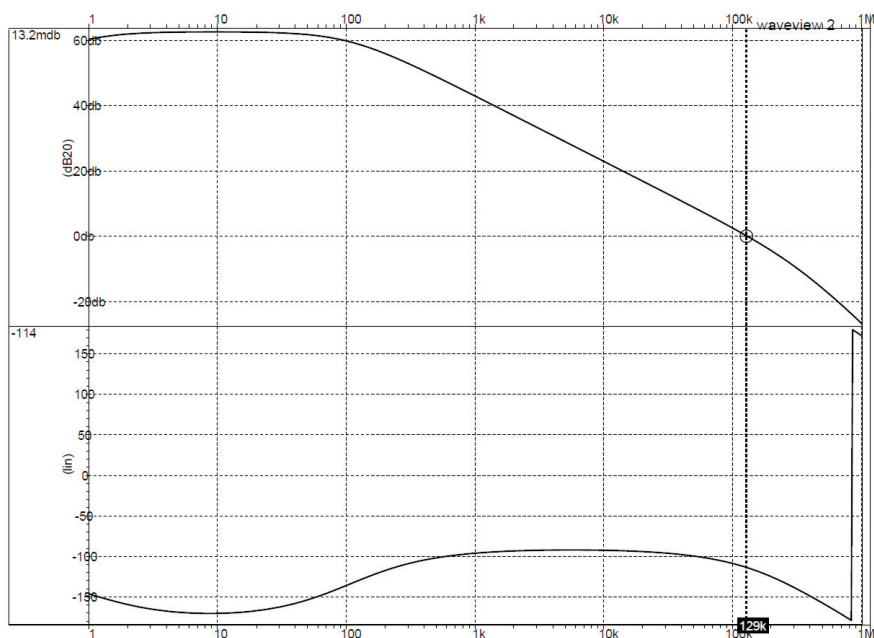


Figure 4.4: *Bode diagram of the CMFB loopgain*

4.2 Transient simulations

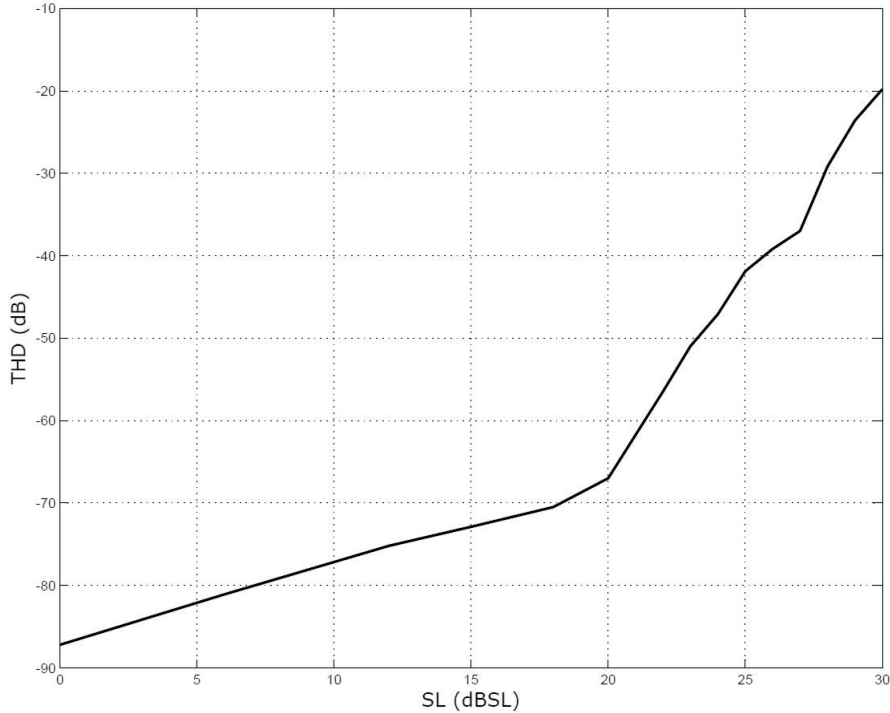


Figure 4.5: *Total Harmonic Distortion over Stimulus Level*

In figure 4.5 the THD as function of the Stimulus Level applied to the sensor is plotted. The slope is almost constant till 18dBSL, equal to an amplitude of 180mV_p in the S_m signal. After this, the THD starts to decrease in a faster way, due to the fact that the output transistors are moving out the saturation region.

4.3 Power consumption

The main power consumption is used for the input transistors M_1 and M_2 , in order to increase their $g_{m1,2}$ and to decrease their thermal noise. Considering only the operational amplifier, which is supply through the LDO, its power consumption is equal to:

$$P_{cons} = V_{DDLDO} I_{cons} = 1.64V \times 120\mu A \simeq 200\mu W$$

Chapter 5

Conclusion

In this Master Thesis, the study and design of an operational amplifier in a pseudo fully differential configuration suitable for capacitive sensors is performed. The designed interface provides a single-ended to differential conversion.

In the first part of the thesis, a general capacitive sensor is considered as input stage of the system. An electrical sensor model is then presented with the definition of its significant parameters. Furthermore, a sensor biasing technique is shown.

Starting from a concept point of view, the operational amplifier is then introduced, with the goals that it should achieve. The chosen OTA topology guarantees high power efficiency and, with a careful design, high noise performances. In fact, the biasing of the input transistors in weak inversion reduce the noise contribution of the other transistors. Their thermal noise is then decreased by setting a quite large biasing current and their flicker noise is minimized by choosing an opportune gate area WL. A current reduction technique also helps regarding this issue and increases the gain of the OTA [5]. The amplifier stability is analyzed in detail.

The CMFB circuit plays an important role in the linearity performances, hence, a linearized CMFB circuit is used. A global noise analysis is carried out, considering the noise contribution of the feedback resistors R_{bias} as well.

The problem of the input matching is treated and an input trimming solution for test-chip purpose is presented. Since the amplifier includes high ohmic nodes, a start up circuits is needed. A solution for this issue is reported.

The final part of the thesis includes simulation results, which reveal the performance of the introduced circuit.

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