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"WAVEFORM ENGINNERING IN INTEGRATED HARMONIC OSCILATORS: ANALYSIS AND EXAMPLES"

"INGEGNERIZZAZIONE DELLE FORME D'ONDA NEGLI OSCILLATORI ARMONICI INTEGRATI: ANALISI ED ESEMPI"

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Abstract

This thesis analyzes the effect of the presence of a second harmonic resonance in the differential LC oscillator, starting form the first intuitive idea that leads to the usage of it and going inside the different effects that it causes on waveform's shapes and phase noise improvement, considering different mechanisms. The analysis is carried out starting from the easiest topology of harmonic oscillator, giving general condition under which this technique has a practical advantage or not, even in other oscillator topologies. The thesis is closed with a practical example where all previously illustrated concepts are used.

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Introduction

Nowadays, most of communications systems are carried out using wireless technologies, which enable to exchange informations without complex infrastructures. However, wireless systems require a proper design of all the circuit that are part of the transmitter and receiver, taking into account all practical problems that are present. Most used radio communications technologies are nowadays digital, since this way to transmit information enables to reach higher speeds, and, since most of transmissions happen between digital systems (like computers), it's naturally to use such systems. Digital communication structures always require specific circuits, as briefly explained in the next chapter. One of the most critical component of every digital communication system is the oscillator, the circuit that provides to the other components a proper signal that is necessary for the functionality of the transmitter or the receiver. One of the most problems in designing wireless technologies is how to manage the presence of noise, which affects the signals present in the system, leading, in some cases, to limitation in the bitrate of the system or in the requirement, for it, to consume more energy. Noise sources are several: from electromagnetic interferences given by other analogous systems places in the neighborhood, to natural field always present, conditions of the medium (such as weather, ...) but also from the electronic noise sources present in all the circuits that are part of the transmitter and the receiver. Among all different types of noise sources in the system, this thesis will deeply study the effect that the noise has on the functionality of the oscillator, which is, as explained before, one of the most important block of all digital communication systems, concentrating on a way that can be used to reduce it and focusing on integrated solutions which are, nowadays, practically the only way used to realize wireless systems. The thesis is organized as follows: the first chapter shows, in general, how a digital communication system is realized, with a general review of most used digital protocols, focusing then on phase noise requirements of the local oscillator that must be satisfied for the proper working of the system. The second chapter introduces the well-known topology of the integrated class-B oscillator, including a brief review of other existing topologies developed to reach higher performances, with the full explanation of the most used theory on phase noise. In the third chapter the main idea of the thesis is presented, explaining how it's possible to use it an what are the advantages that it offers in term of phase noise, deriving all the conditions under which the ideas explained before are worth for a improvement of performances. Finally, the last chapter explains some practical problems and a complete example is shown.

Chapter 1

Preliminaries on Digital Communication Systems

In this section an introduction on digital communication systems is given. The following sections are not intended to be an exhaustive explanations of all details of digital communications, remanding to specialized books for further informations, but rather to be a small introduction to the Phase Noise problem that will be extensively discussed in the following chapters.

1.1 Digital modulation

A digital modulation is a way to transmit information in a different way with respect to analogue transmissions. When a digital modulation is used (in general not only in wireless systems), all informations are sent from the transmitter to the receiver in the form of a sequence of bit (called *bitstream*), that can, obviously, assume only two binary values (0/1). The principle of a digital modulation is to divide the input bitstream into groups of one ore more bit, choosing consecutive bits in the overall bitstream. For every of the different possible input sequence (called *symbol*) a different signal is associated via a biunivocal assignement, like the Example 1.1.1 clarifies.

Example 1.1.1 (4 symbols digital modulation)
Considering to take consecutive pairs of two bits in the input bitstream, the association between the four possible combinations and its corresponding signals could be, for istance, the one shown in Table 1.1, where $\omega = \frac{2\pi}{T}$, with T is a given *symbol period*

Input binary sequence	Associated signal
00	$s_1 = 2cos(\omega t)$
01	$s_2 = 3cos(\omega t)$
10	$s_3 = -2cos(\omega t)$
11	$s_4 = -3cos(\omega t)$

Table 1.1: *Example of digital modulation using 4 symbols*

In this example, all four signals are multiple of a reference signal, in this case $s_{ref} =$

$cos(\omega t)$. It's important to notice that the reference signal is not necessary part of the modulation's set of signals, but it might be. This is a general property of the modulation's set of signals. As in the case of the Example 1.1.1, in a digital modulation, all chosen signals must be obtained via a linear combination of one or more reference signals, which constitutes the *basis* of the modulation. In the Example 1.1.1, the basis consists of an unique signal, but usually the basis can have dimension greater than one (a typical case is two). When more than one reference signal is chosen, they all must be linearly independent, meaning that the only linear combination that gives the zero signal is the one with all coefficients equal to zero. In this way every signal of the modulation can be expressed as a vector whose components are the coefficients of the linear combination of the signal of the basis that gives rise to a certain signal. Still considering the Example 1.1.1, the signal associated to the sequence "00", can be simply expressed via the number 2, with respect to s_{ref}. The working principle of a digital communication system is to transmit, either wireless or via a cable the different signals representing all the bits that must be sent to the receiver. Than, the receiver must use an appropriate circuit to understand which was the original signal to have been sent, reconstructing, symbol by symbol, the original bitstream. In the receiver, the presence of noise (from different sources) must be taken into account. The presence of the noise is what actually causes the fact that, sometimes, the receiver miss a correct reception of the right symbol.

1.1.1 Digital Demodulator

To understand the working principle of the receiver it's necessary to represent the different possible receivable signals in a graphical representation, where every signal is represented with its vector components with respect to the different elements of the basis. Example 1.1.2 shows the graphical representation of the signals of Example 1.1.1. This type of representation is usually known as *constellation* of the digital modulation. Example 1.1.3, instead, shows another example of modulation's constellation, where, in this case, the basis has dimension two.

Example 1.1.2
Considering the example 1.1.1, the constellation is shown in Figure 1.1

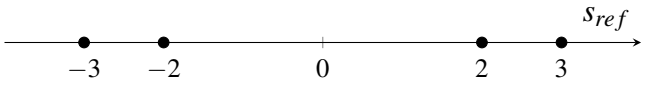

Figure 1.1: *Constellation of Example 1.1.1*

Example 1.1.3 (4-QAM)
Considering now a different modulation, constituted by the four signals of Table 1.2, which shows also the vector representation with respect to the basis (1.1), where, again, $\omega = \frac{2\pi}{T}$, with T being a given symbol period. This type of modulation is known as *quadrature amplitude*

modulation (QAM), and, since 4 symbols are used, it's frequently called 4-QAM

$$s_{ref1} = cos(\omega t); s_{ref2} = sin(\omega t) \tag{1.1}$$

Input binary sequence	Associated signal	Vectorial representation w.r.t (s_1, s_2)
00	$s_1 = cos(\omega t) + sin(\omega t)$	$(1,1)$
01	$s_2 = cos(\omega t) - sin(\omega t)$	$(1,-1)$
10	$s_3 = -cos(\omega t) + sin(\omega t)$	$(-1,1)$
11	$s_4 = -cos(\omega t) - sin(\omega t)$	$(-1,-1)$

Table 1.2: *Example of digital modulation using 4 symbols and two reference signals*

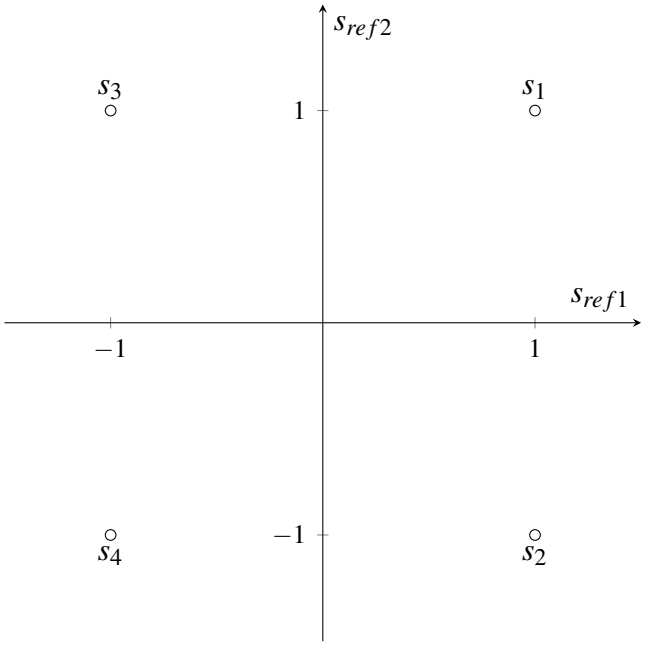

Figure 1.2: *Constellation of Example 1.1.3, axis divide the plane into 4 decision regions*

The goal of the demodulator is to understand, every symbol period, which was the original transmitted signal, given that the received signal is surely affected by **noise**, which is added to the received signal. The working principle of a digital demodulator is to divide the plane of the constellation in some regions, called *decision regions*. For istance, in the Figure 1.2, the axis divide the plane into 4 different decision regions (corresponding, in this case, to the four quadrants), each including one of the symbols. When a signal, which includes noise, is received, the components along the elements of the basis are calculated. Then, based on the position of the found point in the constellation, the demodulator understands what was the signal **probably** sent. The effect of noise (of any type) is to move the signal's point in the constellation from the original position to another one. If the other position is still contained in the decision region belonging to the transmitted symbol, the symbol is received correctly. In other cases, the receiver makes an *error*.

1.1.2 The minimum distance receiver

The way to associate the received signal to one of the symbols of the constellation are many, one of these is the *minimum distance* receiver. The way it works is dividing the constellation into decision regions in such a way that the symbol associated to a received signal (that includes noise) is the one which has the *minimum distance* (in sense of euclidean distance) in the constellation, like the Figure 1.2 already shows. To perform this analysis the receiver must, as first step, find the component of the received signal S_r along all the reference signals of the basis. The generic i-th component of the signal S_r along the reference signal s_i is:

$$S_i = \frac{1}{E_{s_i}} \int_0^{t=T} S_r(t)\, s_i(t) dt = \tag{1.2}$$

where E_{s_i} is the *energy* of the reference signal S_{ref}, namely the integral over a period of its square. So the receiver must include, for every element of the basis, at first a component, called *mixer*, that does the multiplication inside the integral in (1.2), then an integrator that integrates the result, followed by a sampler that samples the output of all integrators to find the values of the component at time $t = T$. A proper circuit calculates the distance of the signal from every symbol of the constellation outputting the right value that follows the minimum distance rule.

1.1.3 Effects of phase noise

As seen before, the presence of noise can move the point on the constellation and cause an error. Noise can come from different noise sources, but this thesis will concentrate only on phase noise, explaining, in an intuitive way, why its value is important in digital communication systems. Considering again the Example 1.1.3, the receiver must multiply the received signal by a cosine and a sine, in order to reconstruct the two components of the transmitted signal. To generate that reference signal, a *local oscillator* is used, which generates the reference signal s_{ref1}.

$$s_{ref1} = cos(\omega_0 t) \tag{1.3}$$

The signal s_{ref2} is always obtained by simply phase shifting s_{ref1} by 90° using an appropriate circuit. However, the oscillator, as all other electronic circuits, has some noise. For this reason, the signal generated by it is actually:

$$s^*_{ref1} = cos(\omega_0 t + \phi(t)) \tag{1.4}$$

where $\phi(t)$ is a random signal due to the presence of the noise. The reason why noise affects only the phase of (1.4) will be clear in the next Chapter. To understand what happens when s^*_{ref1} is used in place of s_{ref1}, the situation when there are no other noise sources is considered. The effect of the presence of a random phase disturbance is a movement of the point inside the constellation into a location different from the place where the received signal should be, along a circle centered in the origin and passing through the point itself, as Figure 1.3 clarifies. If, then, other noise sources are present, the effects sum up in the vector sense.

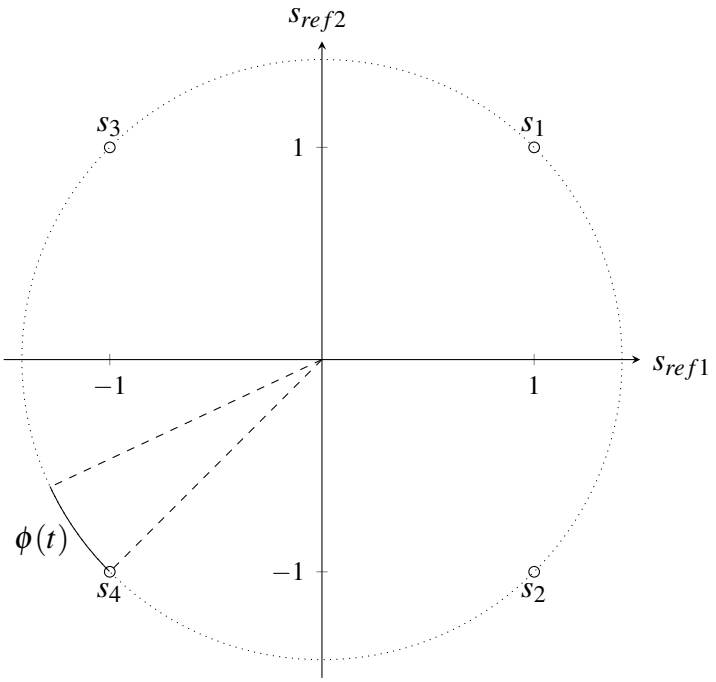

Figure 1.3: *Effect of phase noise in the case of a 4-QAM digital modulation, in this case the reception of s_4 is taken as example, while $\phi(t)$ is the effect of phase noise*

The amount of difference in point's position on the constellation depends on the statistical properties of $\phi(t)$, in particular its variance. If the variance is high, the point moves along the circle more, eventually causing a receiving error to happen more frequently.
When the requirements on bitrate become higher, usually more symbols are added to the constellation, to increase the number of bits sent for every period. For example, Figure 1.4 shows the constellation of a 16-QAM modulation. It's clear that, in this case, requirements on noise are more strict than 4-QAM. A 64-QAM will then require further strict specifications, and so on. Table 1.3 summarizes the phase noise requirements for some standardized wireless communication systems. It's evident the fact that, over the years, specifications are becoming more and more strict, requiring a research activity to develop oscillators capable to reach such values[1].

[1]Since, as extensively discussed in Chapter 2, the effect of the disturbance is to create nonzero frequency components at frequencies different from ω_0, phase noise is practically always expressed as the ratio between the power of the noise component at a given *offset frequency* from ω_0 and the power of the sinusoidal carrier. In this way specifications in Table 1.3 are given, too.

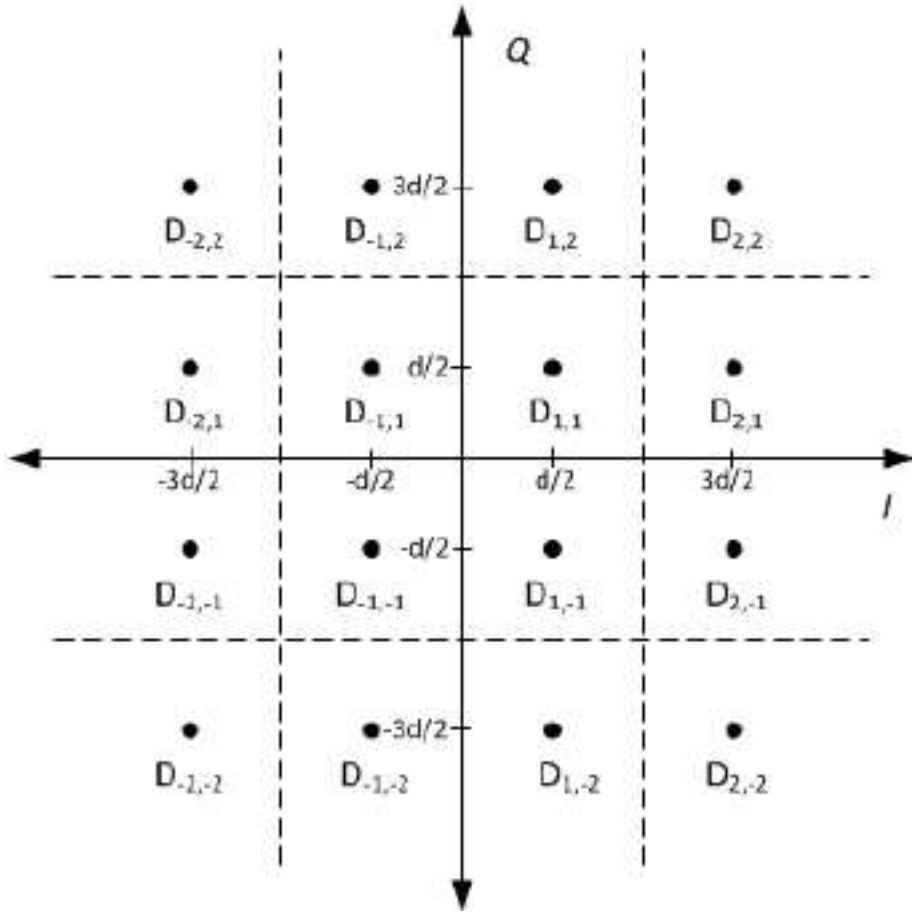

Figure 1.4: *Constellation of a 16-QAM, where dashed line separate the decision regions. It's clear that the system is more sensitive to phase noise, that must be lower*

Standard	Year	Oscillator's frequency	Phase Noise requirement	Corresponding offset frequency
Bluetooth 1.0 [1]	1999	$2.4GHz$	$-111dBc/Hz$	$3MHz$
E - GSM [2]	1999	$900MHz$	$-141dBc/Hz$	$3MHz$
RFID [3]	2007	$900MHz$	$-109dBc/Hz$	$80kHz$
5G [4]	2017	$20GHz$	$-117dBc/Hz$	$1MHz$

Table 1.3: *Phase Noise requirements for some wireless communication standards*

Chapter 2

Integrated LC Harmonic Oscillators

2.1 General structure of harmonic oscillators

An *harmonic oscillator* is a circuit capable to continuously provide a sinusoidal (from which "harmonic") waveform without any external input. The general structure of an oscillator is the one reported in Figure 2.1 [5]. It's important to notice that model explained in Figure 2.1 refers to the so called *negative resistance* structure. Harmonic oscillators can be also viewed as particular feedback circuits, however, for oscillators that will be discussed now on, the negative resistance approach is highly recommended and gives simpler analysis.

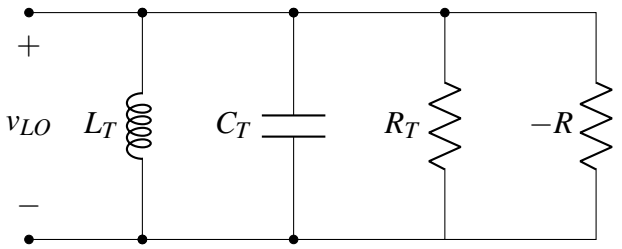

Figure 2.1: *General structure of harmonic oscillators*

The general working principle of an oscillator is the presence of a LC tank, which has some losses elements, represented, in Figure 2.1, by the equivalent parallel resistance R_T. A negative resistance, realized with active components, compensates the positive resistance of the tank in such a way to make the overall system unstable, letting an oscillation to start. Considering the circuit above, the impedance of the overall circuit is given by:

$$Z = \left(\frac{1}{sL_T} + sC_T + \frac{1}{R_T} - \frac{1}{R} \right)^{-1} = \frac{sL_T R_T R}{R_T R + s^2 L_T C_T R_T R + sL_T (R - R_T)} \tag{2.1}$$

As clear form (2.1), the system, if $R > R_T$, is unstable, since the poles have positive real part, and an oscillation at frequency $\omega_0 = \frac{1}{\sqrt{L_T C_T}}$ starts, as shown in Figure 2.2. From a linear point of view, oscillation should grow in amplitude indefinitely. Actually, in a real circuit, nonlinearities become more effective as the amplitude of the oscillation increases, limiting it to a certain value at the point where the oscillator reaches the so-called *Steady State*. However, to

properly understand the behaviour of the oscillator in steady state, the practical implementation of the principle schematic of Figure 2.1 must be analyzed, since different topologies lead to different steady state conditions.

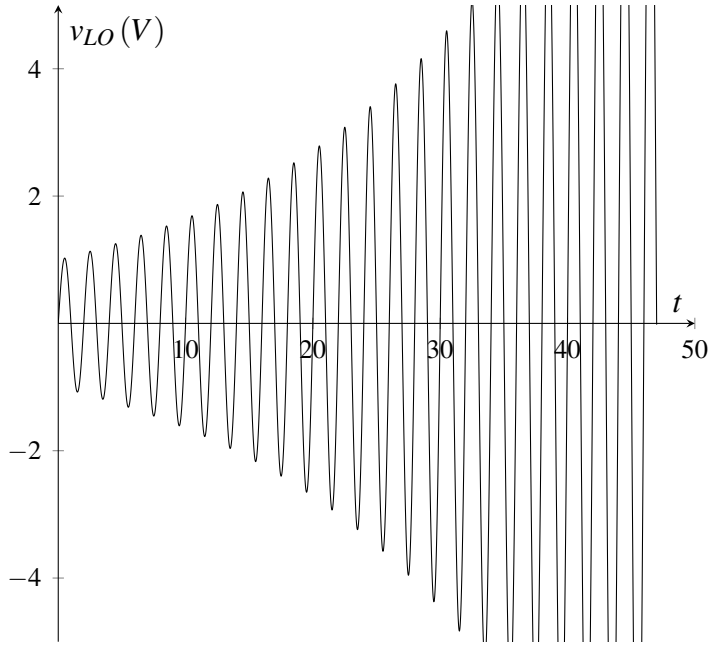

Figure 2.2: *Behaviour of v_{LO} when the system is unstable. Oscillations start with $\omega_0 \simeq 3.14\,rad/s$ (in this example). Notice that, theoretically, there's no limit in the amplitude of the oscillation.*

2.2 The Cross-Coupled Pair

The ways to implement the negative resistance are many different. However, in integrated harmonic oscillators most of the time it's implemented via two transistors (either MOS or bipolar), connected as shown in Figure 2.3, realizing the so-called *cross-coupled pair*. This type of circuit, where, of course, the bias current generator is realized with a proper current mirror, can easily implement a *differential* negative resistance, namely that the *differential* voltage v_d is proportional to the current i_d via a negative constant (at small signals). Since the bias current generator is an open circuit at small signals, the currents flowing into the drain of two devices are the same but with opposite direction.

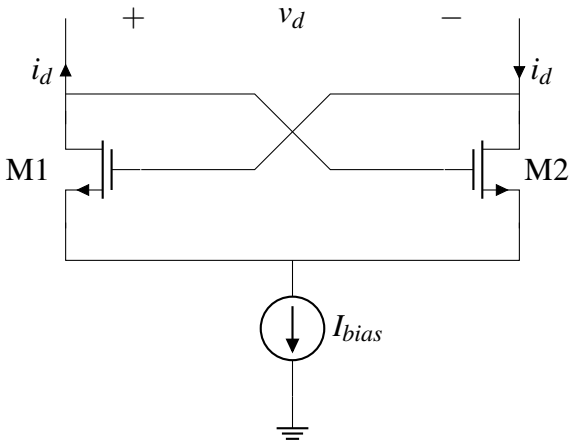

Figure 2.3: *General structure of the cross-coupled pair*

To analyze the cross-coupled pair and calculate the value of its negative resistance, it's necessary to move to its equivalent small signal circuit of Figure 2.4, where parasitic capacitances are not shown since they can be embedded in the tank capacitance C_T.

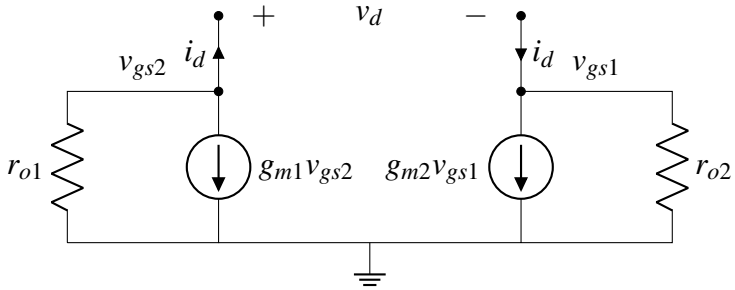

Figure 2.4: *Equivalent small signal circuit of the cross-coupled pair*

For the symmetry of the circuit and the voltages, the common source is an *ac ground*, for differential signals only. The gate to source voltages are:

$$v_{gs2} = -v_{gs1} = \frac{v_d}{2} \tag{2.2}$$

From which, considering, for istance, the left branch of Figure 2.4 :

$$i_d = -\left(\frac{v_d}{2r_{o1}} - g_{m1}\frac{v_d}{2}\right) = \frac{v_d}{2}\left(\frac{1}{r_{o1}} - g_{m1}\right) \tag{2.3}$$

The differential resistance seen at the port is then:

$$R_d = \frac{v_d}{i_d} \simeq -\frac{1}{g_m} \tag{2.4}$$

Since, in (2.3), $r_{o1} >> 1/g_{m1}$, and the two devices are supposed to have the same small signal transconductance $g_m = g_{m1} = g_{m2}$

2.3 The Class-B oscillator

Hence, it has been shown that the cross-coupled pair can provide a negative resistance, whose value depends on the transconductance of the device used to create it. With this structure, one can finally arrive to the general structure of the first oscillator topology, largely used especially in integrated oscillators, which is composed by a tank whose differential behaviour is equal to the one of Figure 2.1, and a cross-coupled pair used to realize the appropriate negative resistance. The so obtained oscillator is also known as *Class B oscillator*, and it's shown in Figure 2.5, where the current source has been replaced with a current mirror, the resistance R_T is actually created by the equivalent parallel of the inductance's series resistance, given by (2.5), and the inductor has been split into two halves, to let the bias current properly flow from the supply to the cross-coupled pair's devices.

$$R_T \simeq Q_L^2 * R_{sL} \simeq Q_L \omega_0 L_T \tag{2.5}$$

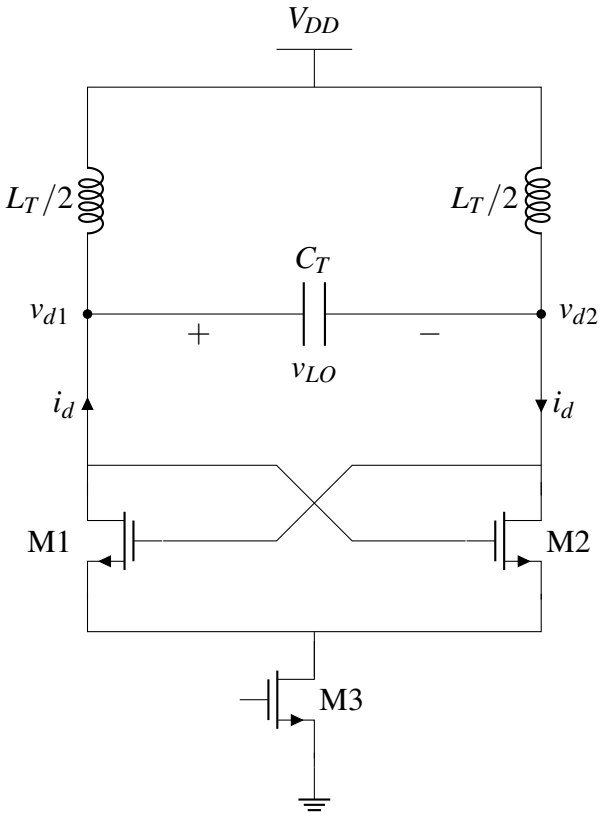

Figure 2.5: *Complete circuit of the class-B oscillator. The reference branch of the current mirror is not shown*

As explained before, there's no explicit resistor in the tank, but the resistive component shown in Figure 2.1 is created using the losses of the inductors. In fact, the more the inductor is ideal, the higher is the equivalent parallel resistance (since Q in (2.5) increases), leading to higher oscillation amplitudes, as explained in the next subsection.

2.3.1 Oscillator's Steady State

If the condition for the instability of the system whose general transfer function is the one in (2.1) is met, the oscillation starts, theoretically diverging to infinite amplitudes. In reality, nonlinearities of the devices limit the amplitude of the oscillation in such a way that, after a given amount of time, the oscillator reaches a *Steady State* condition, where the oscillation's amplitude is stable. This is mainly due to the behaviour of the devices forming the cross-coupled pair. When the amplitude of the gate to source voltages increases, that devices start to operate in the triode region, so decreasing the value of g_m, leading to a stable oscillation amplitude[1].

When the steady state condition is reached, both drain nodes oscillate with a given amplitude equal to $V_{LO}/2$ with respect to ground. $V_{LO}/2 = V_o$ is known as *single ended* amplitude, while v_{LO} is the differential voltage, oscillating with an amplitude equal to double the single ended one. Since the gate of a device is connected to the drain of the other one, waveforms at the drain and gate terminals of a device are reported in Figure 2.6. As clearly visible, when the oscillation's amplitude reaches steady state, the devices forming the cross-coupled pair operates with gate and drain voltages given by (2.6) and (2.7), where the mean value of the drains' voltages is V_{DD} and the single ended oscillation's amplitude is $V_{LO}/2$

$$v_g = V_{DD} - \frac{V_{LO}}{2} sin(\omega_0 t) \tag{2.6}$$

$$v_d = V_{DD} + \frac{V_{LO}}{2} sin(\omega_0 t) \tag{2.7}$$

In the steady state condition, the two transistors of the cross-coupled pair operate alternatively in triode region or in the OFF region. This behaviour is known as *Hard Switching* and the oscillator in steady state is properly modelled as shown in Figure 2.7, where switches and their parasitic resistance equivalently model the transistor in triode region. Moreover, if the capacitor is considered to be split in a series of two equal capacitors with double value, the point between them is a differential ac ground.

[1] In some topologies, different from the class-B, oscillation's amplitude might be, under some conditions, unstable

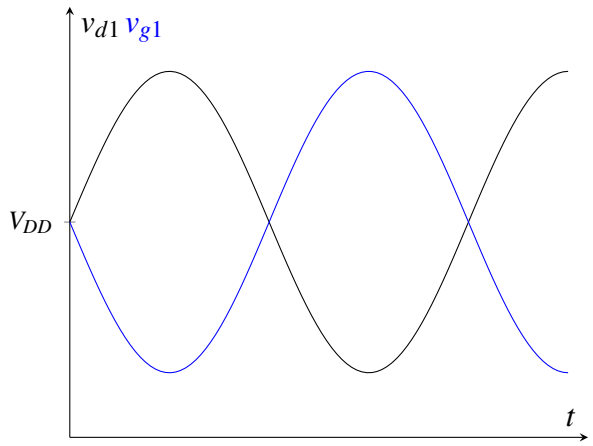

Figure 2.6: *Class-B Steady State waveform, with* $V_{DD} = 1V$

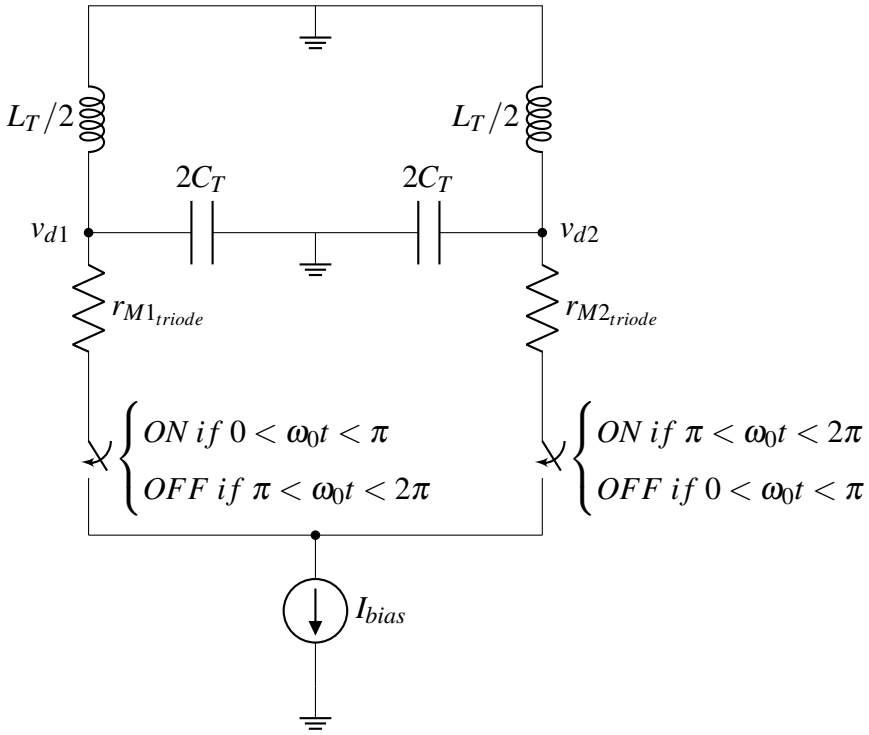

Figure 2.7: *Equivalent Steady State model of the class-B oscillator, where both the supply and the midpoint of the two capacitors representing* C_T *are AC grounds. Every half a period, one of the two switches (transistors) is ON while the other is OFF, and viceversa*

From Figure 2.7, it's clear that the current flowing into the two terminals of the tank is **ideally** (as clear later) a squarewave ranging from 0 to I_{bias}, with a period equal to the period of the oscillation. At ω_0, both the halves of the tank, redrawn as in Figure 2.7, operate in resonance, so they display an impedance equal to $R_T/2$, where R_T is the equivalent parallel resistance of (2.5), at the frequency $\omega = \omega_0$, and a low impedance for all other frequencies multiples of ω_0 (the out-of-resonance impedance is actually capacitive for $\omega > \omega_0$, but in this approximate analysis it's considered to be zero). Since the current is a periodic signal, it can be decomposed into its harmonic components. In particular, the amplitude of the first current

harmonic is:

$$I_1 = \frac{2}{\pi} I_{bias} \tag{2.8}$$

while further harmonics are irrelevant since they are multiplied by the impedance of the tank out of resonance, which results in a very low (ideally zero) voltage at the two drains. It's now easy to find the expression of $v_{d1} = -v_{d2}$:

$$v_{d1} = \frac{R_T}{2} I_1 sin(\omega_0 t) = \frac{2}{\pi} I_{bias} \frac{R_T}{2} sin(\omega_0 t) \tag{2.9}$$

where the fact that only half of the inductor is present at any of the two halves of the circuit has been used. From (2.9) the amplitude of the differential oscillation is:

$$V_{LO} = V_{d1} - V_{d2} = \frac{2}{\pi} R_T I_{bias} \tag{2.10}$$

2.3.2 Current and voltage efficiency

Analyzing the equation (2.10), it's possible to define some parameters used to characterize different oscillator topologies that are nowadays available, different from the traditional class-B. In any oscillator which contains a bias generator at the common source of the cross-coupled pair, the final oscillation's amplitude is always function of the first harmonic current's value I_1. The difference among various oscillator topologies is in the shape of the drain current of the devices at steady state, which can be different from the square wave of Class-B oscillator. For this reason, the *current efficiency* is defined by (2.11), quantifying how much the bias current is converted into first harmonic current (the only one that is further converted into a voltage).

$$\eta_I := \frac{I_1}{I_{bias}} \tag{2.11}$$

For the class-B, $\eta_I = \frac{2}{\pi} \simeq 0.64$, at least **theoretically**. For a real circuit, actually $\eta_I \sim 0.55$.

Another situation that limits the amplitude of the oscillation is the fact that the lower limit of v_{d1} and v_{d2} cannot be the ground voltage. In fact, as clear from Figure 2.6 there must be enough "space" between the minimum value of v_{d1} or v_{d2} to guarantee the operation in saturation of the current mirror and the presence of a voltage across the devices operating in triode. For this reason, the maximum single ended swing is lower than V_{DD}. Letting $V_{o_{max}}$ be the maximum single ended oscillation's swing, (2.12) defines the *voltage efficiency*.

$$\eta_V := \frac{V_{d_{max}}}{V_{DD}} \tag{2.12}$$

For the class-B, $\eta_V = (V_{DD} - r_{on} I_{bias} - V^*_{mirror})/V_{DD}$, V^*_{mirror} being the minimum voltage required by the mirror to keep itself in saturation.

With the above definitions V_{LO} can be expressed as:

$$V_{LO} = \eta_I R_T I_{bias} = 2\eta_V V_{dd} \tag{2.13}$$

It's important to notice that (2.13) is valid for any oscillator topology, given that η_I and η_V

have been properly defined. Table 2.3.2 shows the typical value of the above defined parameters for some typical oscillator topologies. The *class-F2* oscillator is the one which constitutes the main part of the following chapters.

Oscillator Topology	η_I	η_V
Class B	~ 0.55	$\sim 0.6 \div 0.8$
Class-C	~ 1	~ 0.9
Class-D	~ 1.5	~ 1.5
Class-F2	~ 0.6	$\sim 0.75 \div 0.8$

Table 2.1: *Typical values of voltage and current efficiency for different oscillator topologies. Values of voltage efficiency assume* V_{DD} *to be in the range* $0.8 \div 1.2V$

2.3.3 Current and Voltage Limited Regime

The behaviour of the oscillator modelled as in Figure 2.7 is valid if the tail's transistor operates in saturation for the entire period. This operation region is called *current limited regime*. If I_{bias} is increased, the amplitude of the oscillation is increased up to a point where the tail device enters the triode region for part of the cycle. If the current is further increased, that device is always in the triode region and the bias current cannot increase anymore, reaching the maximum possible value of it. This operating condition is called *voltage limited regime* and the tail generator could be also removed, leading to the class-D topology, where the value of the bias current cannot be controlled. Between these two regions, there exist a transition region where the tail's device enters triode only for part of the cycle. The dependence of the output amplitude on the average value of the tail's device current is shown in Figure 2.8, where the slope of the linear part of the graph should be in theory $(2/\pi)R_T$.

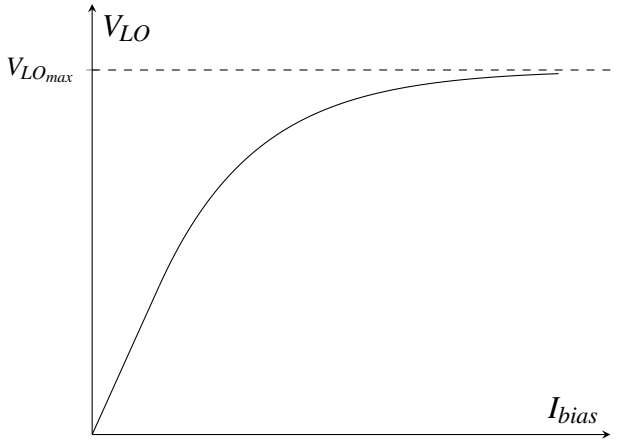

Figure 2.8: *Differential amplitude with respect to the bias current*

2.3.4 Real behaviour of Steady State drain current

In a real circuit, the waveform of the drain current of the cross-coupled pair's devices[2] is not a square wave anymore. In fact, the transition of that devices between the active and the triode region, together with the parasitic capacitance of the current mirror, shapes the drain current in a way that is different from a squarewave. Example 2.3.1 show a simulation of a real circuit where this fact is shown.

Example 2.3.1 (Class-B Drain Current)
Just as an example, a real circuit employing the 22-nm GlobalFoundries technology is simulated, using ideal components for the tank, with $L_T = 400pH$, $C_T = 2.53pF$ (this values gives $\omega_0 \simeq 5GHz$), $R_T = 1k\Omega$ and real transistors for the cross-coupled pair and the bias current generator. The bias current is fixed to $I_{bias} = 1.2mA$, resulting in a theoretical oscillation amplitude of $V_{LO} = 750mV$. The dimensions of the cross-coupled pair's devices are ($W = 8\mu m$, $L = 18nm$), allowing a ON voltage of $\simeq 50mV$, while the tail generator has ($W = 8\mu m$, $L = 300nm$) as dimensions, allowing it to always work in saturation. Figure 2.9 shows the simulated current which is not a squarewave at all. Moreover, the simulated oscillation amplitude is $711mV$, which gives $\eta_I = 0.59$, lower than the theoretical one.

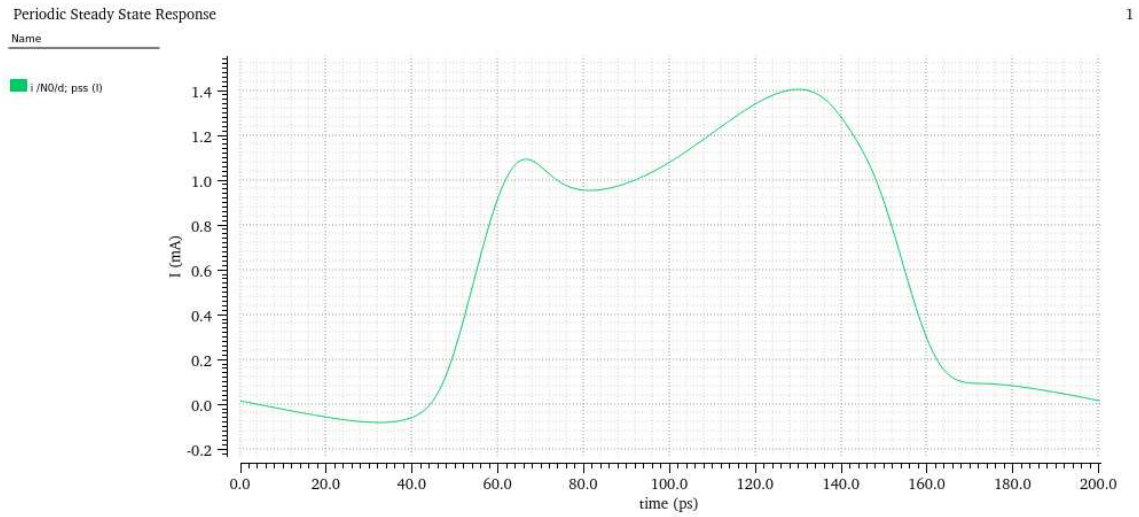

Figure 2.9: *Simulated current waveform of the oscillator of Example 2.3.1*

A detailed theoretical analysis of the waveform of Example 2.3.1 can be made only in an approximate way, which makes use of the long channel model for the transistor of the cross-coupled pair [6]. For more accurate models one should use the proper short channel model (especially if deep-scaled technologies are used). However, still with the long channel model calculations are quite complex and, at the end, it's still necessary to use numerical simulations to solve the final equation since, as it will be clear, it has not a closed form solution.

To analyze theoretically the current's waveform, at least in an approximate way, some hypothesis (not always perfectly true) are made:

- cross-coupled pair's transistors follow the long channel model;

[2] In many works, devices creating the cross-coupled pair are called *gm-devices*

- The parasitic drain-to-bulk capacitance of the tail generator is large enough to be assumed as a short circuit at ω_0.

The second point allows to consider the voltage of the common source V_S to be constant, **in general different from the bias point's value**. To study the circuit, it's convenient to move the reference point of voltages to the common source, studying the circuit of Figure 2.10, where, since the interest is on the drain current, the tank has been substituted with a sinusoidal voltage source with the right amplitude. Moreover, moving the reference to the common source will change V_{DD} to $V_{DD} - V_S$. Obviously, changing the reference doesn't change the values of currents.

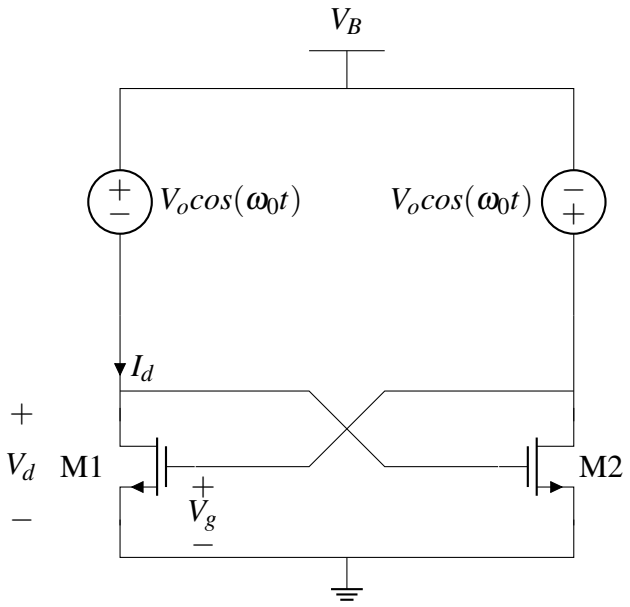

Figure 2.10: *Circuit used to calculate the drain current, with the reference on the common source*

With respect to Figure 2.10, and focusing only on one device (for istance $M1$), drain and gate voltages are, respectively:

$$V_d = V_{ds} = V_B - V_o cos(\omega_0 t) \tag{2.14}$$

$$V_g = V_{gs} = V_B + V_o cos(\omega_0 t) \tag{2.15}$$

defining $V_B := V_{DD} - V_S$.

The current waveform can be decomposed into some regions, as explained in Figure 2.11. In Figure 2.11, the three operating regions of the transistor are highlighted. Referring only to positive values of $\omega_0 t$, for angles between 0 and Ψ the transistor operates in triode region, between Ψ and ϕ it operates in saturation, for the remaining part of the period it's off. For the other transistor of the cross-coupled pair the situation is the same, with a π angle shift only in the angles axis. For this reason, considerations below always refers to one transistor. Using

long channel model, and defining $\beta = \mu C_{ox} W/L$, the steady state current of the transistor can be expressed as function of drain and gate voltages as:

$$\begin{cases} I_d = \beta (V_{gs} - V_T)^2 & \text{Saturation region} \\ I_d = \beta ((V_{gs} - V_T) V_{ds} - V_{ds}^2/2) & \text{Triode region} \\ I_d = 0 & \text{Off region} \end{cases} \tag{2.16}$$

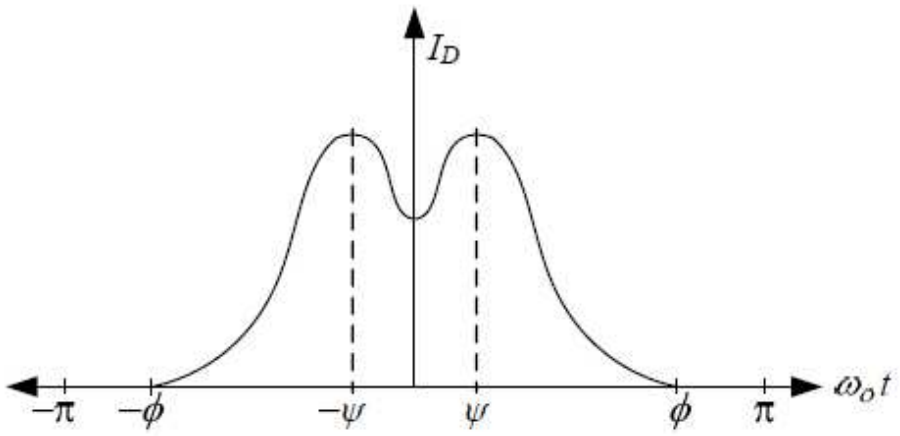

Figure 2.11: *Behaviour of the drain current according to the approximate model of [6]*

In any case, the average drain current I_D of the transistor is imposed by the tail generator to be $I_{bias}/2$.

$$I_D = I_{bias}/2 = \beta (V_{GS} - V_T)^2 \tag{2.17}$$

where V_T is the threshold voltage. From (2.17), the bias point gate-to-source voltage V_{GS} is:

$$V_{GS} = \sqrt{I_D/\beta} + V_T \tag{2.18}$$

Taking the ratio between the equation (2.16), in saturation region, and (2.17), and using the expression of V_{gs} given by (2.15), one gets:

$$\frac{I_d}{I_D} = \left(\frac{V_B}{V_{GS} - V_T} + \frac{V_o}{V_{GS} - V_T} cos(\omega_0 t) - \frac{V_T}{V_{GS} - V_T} \right)^2 \tag{2.19}$$

which is valid in **saturation** region. In triode region, with a similar reasoning, equation (2.19) becomes:

$$\frac{I_d}{I_D} = \frac{V_B + V_o cos(\omega_0 t) - V_T}{V_B - V_T} \frac{V_B - V_o cos(\omega_0 t)}{V_{GS} - V_T} - \frac{1}{2} \left(\frac{V_B - V_o cos(\omega_0 t)}{V_{GS} - V_T} \right)^2 \tag{2.20}$$

To find the limit angle between triode and saturation regions, it's necessary to consider that the device enters saturation from triode when $V_d = V_g - V_T$, which implies, using (2.14) and (2.15):

$$\psi = cos^{-1}\left(\frac{V_T}{2V_o}\right) \tag{2.21}$$

While imposing the drain current in saturation given by (2.19) to be zero, one gets:

$$V_B = V_T - V_o cos(\phi) \tag{2.22}$$

However, since V_B is not known, it's necessary to find a different way for the calculation of ϕ. In particular, the average drain current is found by piecewise integrating (2.16) and equating it with the average current value given by (2.17).

$$I_{bias}/2 = \int_0^{\psi} I_{d_{triode}} + \int_{\psi}^{\phi} I_{d_{sat}} \tag{2.23}$$

After some steps [6], an expression containing only ϕ as unknown is obtained:

$$\pi = \frac{V_o^2}{(V_{GS}-V_T)^2}\left[\frac{\phi}{2} - 2\psi - \frac{3}{2}sin(\phi)cos(\phi) + \phi cos^2(\phi) - 2cos(\psi)sin(\psi)\right] + 4\frac{V_o V_T}{(V_{GS}-V_T)^2}sin(\psi) + \\ - \frac{V_T^2}{(V_{GS}-V_T)^2}\psi \tag{2.24}$$

which can be solved numerically to find the value of ϕ.

Once ψ and ϕ has been obtained, V_B can be simply found using (2.22).

At this point, having all expressions of V_d, V_g and V_B, it's possible to explicit find the drain current in all three operating regions, by simply multiplying (2.19) and (2.20) by the average drain current I_D. Figure 2.12 shows the result of the calculation for Example 2.3.1, it's possible to notice the differences between simulation and theory.

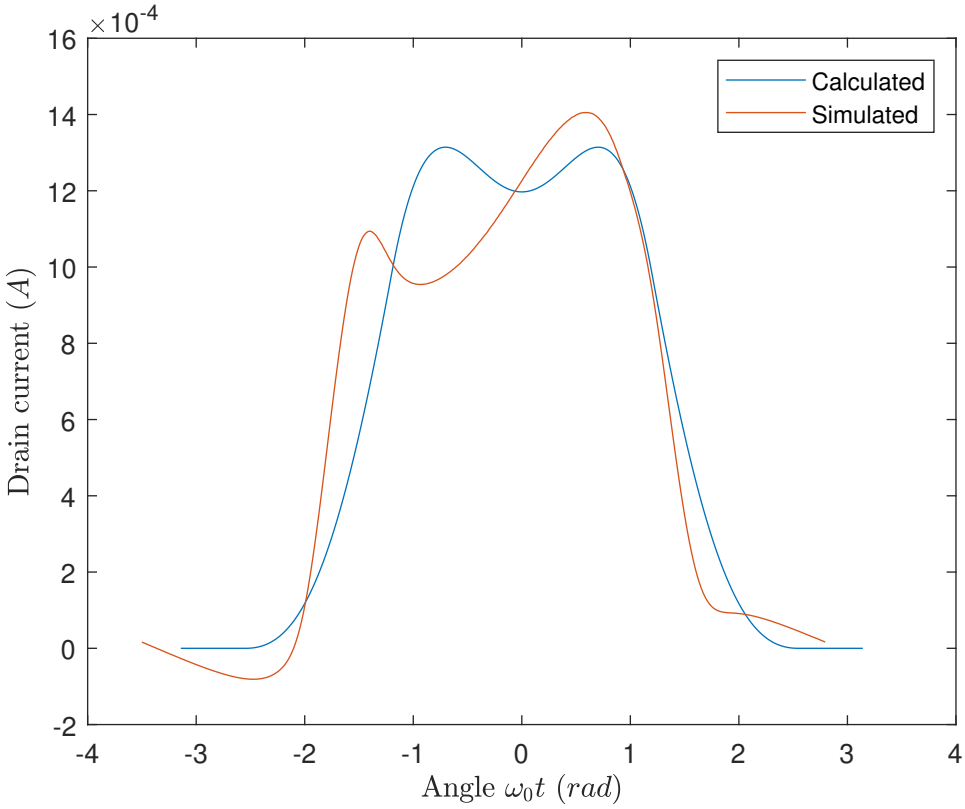

Figure 2.12: *Comparison of drain current's approximate analysis with the values of Example 2.3.1, compared with the result of the simulation*

It's clear that the theory is quite complex and it doesn't still provide enough accurate results. For this reason, in all practical design problems it's never used and simply some margin on η_I is considered, given that it's lower than $2/\pi$. However it can be useful to understand how the current's shape and spectrum depend on the shape of V_d and V_g. For istance, Figure 2.13 provides the current waveform for different values of V_o, while in Table 2.2 the corresponding Fourier coefficients are reported. It's noticeable that, the more the transistor enters the triode region, the higher is the value of the second harmonic, while the first slightly gets lower, since the waveform differs from the ideal squarewave more.

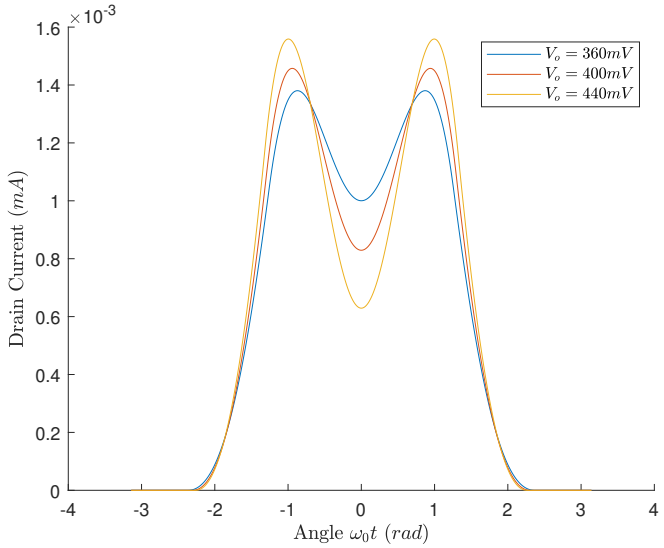

Figure 2.13: *Effect of the value of V_o on the shape of the drain current, whith $I_{bias} = 1.2mA$*

Amplitude V_o	First harmonic $\|I_1\|$	Second harmonic $\|I_2\|$
$360\,mV$	$729\,\mu A$	$28\,\mu A$
$400\,mV$	$702\,\mu A$	$99\,\mu A$
$440\,mV$	$669\,\mu A$	$184\,\mu A$

Table 2.2: *Effect on the first and the second harmonic of the drain's current, considering $I_{bias} = 1.2mA$, according to the approximate theory*

2.4 Phase Noise

In this section the effects on the oscillator of the noise generated by various noise sources present in the circuit is analyzed. Since, as it will be clear, the effect of the noise can be viewed as a perturbation in the phase of the oscillation, while it does not affect its amplitude, noise in electronic oscillators is referred as *Phase Noise*[3]. Main noise sources in an oscillator are:

- Lossy components of the tank (R_T);
- Noise generated by cross-coupled pair's devices;
- Noise generated by the bias circuit;

Different theories allowing the study of the phase noise have been developed since 90s, going from intuitive approaches to extremely rigorous approaches making use of the theory of Linear-Time-Variant systems. The theory it's going to be presented is the one by Hajmiri and Lee [7],[8], widely used to analyze oscillators in a decently rigorous way. Next, a more general theory, that considers also the harmonics of the output voltage different from the first, will be briefly presented, too.

[3] "PN" in the following

Considering a generic oscillator, it's easy to understand that noise may, in principle, change both the amplitude and the phase of the output sinewave. However, amplitude's variation are compensated by nonlinearities of the circuit, reaching a condition in which oscillation's amplitude is stable[4], so the relevant perturbation due to noise is the one on the phase. For this reason, the output voltage can be expressed as:

$$v_{LO} = V_{LO} cos(\omega_0 t + \phi(t)) \tag{2.25}$$

where $\phi(t)$ is a random phase perturbation caused by noise. Since ϕ is a random signal, the spectrum of v_{LO} is not a single line at ω_0 but it displays some nonzero components also at values close to ω_0 but different from it by an *offset frequency* $\Delta\omega$, operating as a phase modulation. For any offset frequency $\Delta\omega$, it's possible to find a value for the power spectral density of the output signal v_{LO}, $S_{v_{LO}}(\omega_0 + \Delta\omega)$. This is a value expressed in $[V^2/Hz]$, but it's usually expressed with respect to the power of the carrier defined as:

$$P_{carrier} = \frac{V_{LO}^2}{2} \ [V^2] \tag{2.26}$$

Furthermore, the ratio of the PSD of the noise with respect to the carrier's power is normally represented in a logarithmic scale, defining the noise, at $\Delta\omega$ from the carrier, as:

$$L(\Delta\omega) = 10 log_{10} \left(\frac{S_{v_{LO}}(\omega_0 + \Delta\omega)}{P_{carrier}} \right) \ [dBc/Hz] \tag{2.27}$$

Using dBc as unit of measurement, with the meaning of dB with respect to the power of the carrier (per unit frequency).

Any sinusoidal oscillator, regarding noise, can be represented with the block diagram shown in Figure 2.14, where it's possible to identify two main blocks:

- The first block converts the disturbance signal, represented with a noise current i_n, into the proper phase error.
- The second block converts the phase error into the output voltage, by simply calculating the value of the cosine function at the istantaneous phase properly accounting the phase error $\phi(t)$

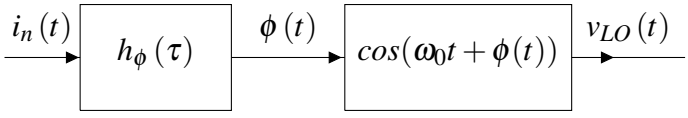

Figure 2.14: *Block diagram of a generic harmonic oscillator used to study the effect of the noise*

Focusing on the first block, the way the phase error is calculated is based on the so-called *ISF approach*, which is the main point of the Hajmiri and Lee theory [7]. The analysis of the

[4]In some cases, oscillation amplitude may be unstable [9], however, this phenomenon happens when large tail capacitors are used, which is not the case of circuits presented in this thesis

phase noise is first carried out considering the noise coming from the tank **only**. The effect of noise coming from other sources is discussed later. Noise coming from the tank is only due to the equivalent parallel resistance R_T. Referring to the circuit of Figure 2.7, tank's noise is generated from the equivalent resistance of $L_T/2$ inductor, namely $R_T/2 = Q^2 R_{s_L}/2$. Noise from a resistor can be modelled as a parallel current source injecting a noise current i_n with PSD:

$$S_{i_n} = \frac{4kT}{R_T/2} \tag{2.28}$$

where k is the Boltzmann constant and T is the absolute temperature. It's important to notice that the analysis is considering only the thermal noise. Furthermore, also flicker noise generated by active devices will be considered.

When a noise current is injected into a node of the circuit, the oscillation waveform is perturbed. First of all, an impulsive current's disturbance, injecting a charge q into a given node of the circuit is considered. The effect of perturbation depends on when the disturbance is injected with respect to the entire period of the oscillation. In fact, if an impulsive disturbance happens at the peak of the oscillation, it causes only an error in the amplitude of the waveform, not affecting the phase of it. On the contrary, a disturbance arriving when the oscillation crosses the mean value will cause the maximum possible phase error. Figure 2.15 clarifies this concept. For intermediate points the phase error caused by an impulse depends on when the impulse arrives. The function giving the phase error as a function of the time τ when the impulse current arrives is called *Impulse Sensitivity Function* (ISF). It's a dimensionless function, with 2π as period, giving the phase error with respect to the moment the impulse happens. The ISF' maximum value is equal to 1, namely that it's normalized to the maximum possible phase shift, no matter what it is. For a traditional class-B oscillator with cosinusoidal output waveform, the ISF of drain nodes is:

$$\Gamma(\tau) = sin(\omega_0 \tau) \tag{2.29}$$

As clear from (2.29), an impulse of charge q has no effect on phase if it's injected at $\omega_0\tau = 0, \pi$ (peak of oscillation), while the effect is maximum for $\omega_0\tau = \pi/2, 3\pi/2$. In general, the calculation of the ISF is not simple, the rigorous derivation of (2.29) can be find in [7].

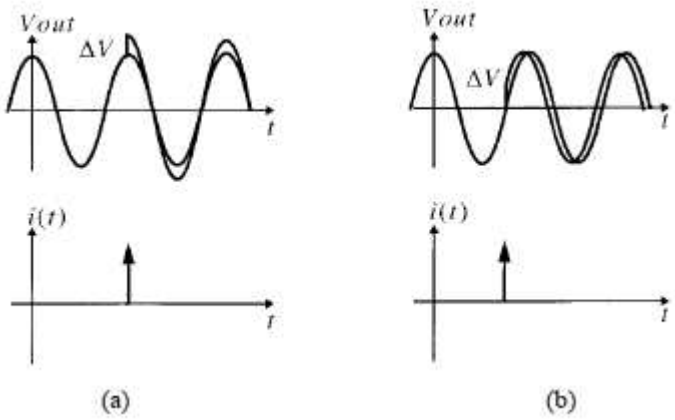

Figure 2.15: *Effect of the same impulsive current at different moments inside the period of the oscillation. In case (a) there's no phase error, while in case (b) there's a phase error lasting indefinitevely*

Referring to the block diagram of Figure 2.14, it's clear that the phase error $\phi(t)$ is given by the response of the first block to a generic input current i_n, and it can be obtained via the convolution with the impulse response of the block $h_\phi(t,\tau)$. The impulse response of the block is the response of it when an unitary impulsive current injecting a total charge $q = 1C$[5] is given as input. Since q is injected in a infinitesimal amount of time, it causes a voltage variation on the tank's capacitor *only*, equal to $\Delta V_{max} = q/2C_T$. Then, since the ISF is normalized to the maximum possible phase shift if a charge q is injected, it's necessary to compute the maximum phase shift $\Delta\phi_{max}$. Looking at the ISF, the maximum phase error occurs when the sinewave crosses the zero level. In that condition, if an instantaneous voltage change, equal to ΔV happens, the oscillation continues (with the phase error), reaching again the zero value after an amount of time which corresponds to the maximum phase error $\Delta\phi_{max}$, as clear from Figure 2.16. The phase error is:

$$\Delta V_{max} = -\frac{V_{LO}}{2} sin(\Delta\phi_{max}) \simeq \frac{V_{LO}\Delta\phi_{max}}{2} \tag{2.30}$$

[5]The impulse response is defined as the response to a unitary impulse, namely a current $i_n(t) = (1A)\delta(t)$, whose area, representing the total injected charge, is $1\,C$

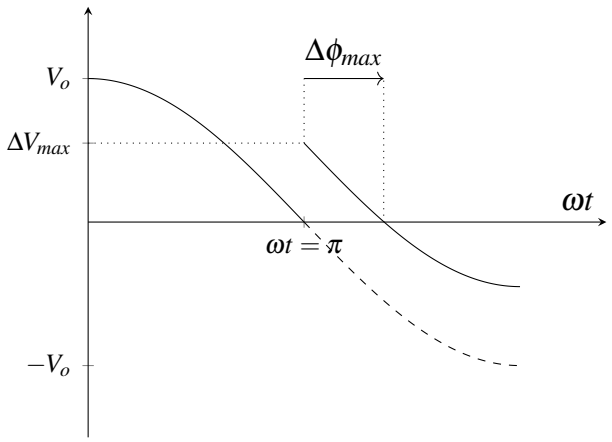

Figure 2.16: *Calculation of the maximum phase error*

where the last step uses a first order approximation of the sine function. This is called the *linearity* approximation, which is practically always true, as widely demonstrated in the literature [7].

From (2.30), by solving for $\Delta\phi_{max}$ and considering that $\Delta\phi = \Delta\phi_{max}\Gamma(\tau)$, the impulse response of the block converting the noise current into the phase error is:

$$h_\phi(t,\tau) = \frac{\Gamma(\tau)}{C_T V_{LO}} \delta_{-1}(t-\tau) \tag{2.31}$$

where δ_{-1} is the step function. The meaning of (2.31) is that, before the moment of injection, there's no phase error. After the q impulse arrives, the phase error suddenly steps to the value given by the ISF, considering the maximum possible phase error. Once the impulse response in known, the output phase error is given by the usual convolution (2.32). Notice that that's valid only in linearity condition, even if the system is not time-invariant.

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)\, i(\tau)\, d\tau = \frac{1}{C_T V_{LO}} \int_{-\infty}^{t} \Gamma(\tau) i(\tau) d\tau \tag{2.32}$$

To easily calculated the integral in (2.32), it's necessary to express the ISF with its Fourier series, since it's a periodic signal:

$$\Gamma(\tau) = \frac{c_0}{2} + \sum_{n=1}^{+\infty} c_n cos(\omega_0 t + \theta_n) \tag{2.33}$$

By inserting (2.33) into (2.32):

$$\phi(t) = \frac{1}{C_T V_{LO}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) + \sum_{n=1}^{+\infty} c_n \int_{\infty}^{t} i(\tau) cos(n\omega_0 \tau) d\tau \right] \tag{2.34}$$

Beside the computation of (2.34), it's important to analyze it to understand what's its practical meaning. To do this, the effect of a cosinusoidal disturbance $i(\tau) = I_k cos((k\omega_0 + \Delta\omega)\tau)$, of amplitude I_k and frequency $\Delta\omega + k\omega_0$, $k = 1,2,\ldots$, namely a frequency close to the (fixed) k-th multiple of ω_0, is analyzed. By inserting the expression of the current in (2.34):

$$\phi(t) = \frac{1}{C_T V_{LO}} \left[\frac{c_0}{2} \int_{-\infty}^{t} I_k cos((k\omega_0 + \Delta\omega)\tau) + \sum_{n=1}^{+\infty} c_n \int_{\infty}^{t} I_k cos((k\omega_0 + \Delta\omega)\tau) \cos(n\omega_0\tau) d\tau \right] \tag{2.35}$$

$$\phi(t) = \left(\frac{1}{C_T V_{LO}} \right) \frac{c_0}{2} \int_{-\infty}^{t} I_k cos(k(\omega_0 + \Delta\omega)\tau) + \sum_{n=1}^{+\infty} \frac{c_n}{2} \int_{\infty}^{t} I_k cos((n-k)\omega_0 t + \Delta\omega)\tau) d\tau + \\ + \sum_{n=1}^{+\infty} \frac{c_n}{2} \int_{\infty}^{t} I_k cos((n+k)\omega_0 t + \Delta\omega)\tau) d\tau \tag{2.36}$$

Moving to the frequency domain, the integral has a filtering effect. Since $\Delta\omega$ is much lower than ω_0 (and therefore all its positive or negative multiples), the only relevant term in (2.36) is the one coming from the second integral, when $n = k$. All other terms give rise to harmonic components that are strongly attenuated in frequency by integration. Hence, the phase error associated to the injection of a sinusoidal disturbance at frequency close to the k-th multiple of the oscillation frequency ω_0 can be well approximated by:

$$\phi(t) \simeq \frac{I_k c_k sin(\Delta\omega t)}{2 C_T V_{LO} \Delta\omega} \tag{2.37}$$

Since the noise is not constituted by a single spectral line but rather it looks like a continuous spectrum ranging the whole band of frequencies, the PSD of the noise error at frequency $\Delta\omega$ is given by the downconversion of all components located at a distance $\Delta\omega$ from **any** multiple of the oscillation frequency, as clarified from Figure 2.17

Moreover, if the PSD of the noise current is flat, the PSD of the phase error is proportional to $\frac{1}{f^2}$ (considering the the PSD is somehow the square of the Fourier transform and the integral is equivalent to a division by $j\omega$), while if the PSD of the noise is proportional to $\frac{1}{f}$ (flicker noise), the PSD of the phase error directly depends on $\frac{1}{f^3}$.

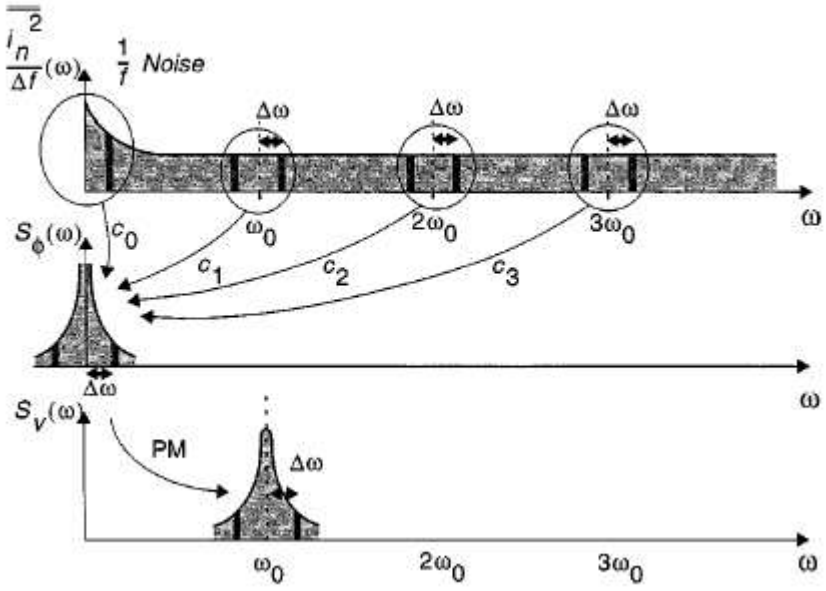

Figure 2.17: *Mechanism of conversion between the PSD of the noise into the PSD of the phase error (first two plots), the third plot represents the conversion of phase error into the output voltage, which will be explained later*

To calculate the total noise PSD at a given offset frequency, it's necessary to find the total noise power. Considering that (2.37) gives the phase error for a given k, it's necesssary to sum the power of (2.37), for all possible value of k. The power of a single value of k is given by (2.38), since the power of a sinewave is half the square of the amplitude.

$$|\Phi(\Delta\omega)|^2 = \frac{1}{8(C_T V_{LO})^2(\Delta\omega)^2} c_k^2 (I_k^2) \tag{2.38}$$

Summing the power of all sinewaves obtained for different value of k and dividing by a small frequency range Δf, to get the PSD of the phase error $S_\phi(\Delta\omega)$, one gets:

$$S_\phi(\Delta\omega) = \frac{1}{8(C_T V_{LO})^2(\Delta\omega)^2} \frac{4kT}{R_T/2} \sum_{k=0}^{+\infty} c_k^2 = \frac{kT/R_T}{(C_T V_{LO}^2)} 2\Gamma_{rms}^2 \tag{2.39}$$

where the fact that $I_k^2/\Delta f = \frac{4kT}{R_T/2}$, for every k has been exploited in (2.39), together with the Parseval's theorem, to substitute the sum of all c_k with $2\Gamma_{rms}^2$.

Finally, to understand the effect of the noise on the output voltage rather than the phase error, it's necessary to consider the effect of the second block of Figure (2.14). In the frequency domain, the multiplication by a cosine function simply upshifts the spectrum of the phase error centering it near ω_0. For this reason, (2.39) is the same when the PSD of the output voltage is considered instead of the one of the phase error, by simply remembering that, while $\Delta\omega$ used to represent the frequency offset with respect to the zero frequency, it represents now the offset with respect to the carrier frequency, as Figure 2.17 explains. By substituting Γ_{rms}^2 with the right value, in this case $1/2$, the final phase noise equation, in logarithmic scale, known as *Leeson*

Equation is:

$$S_v(\Delta\omega) = 10log_{10}\left(\frac{kT/R_T}{(C_T V_{LO})^2(\Delta\omega)^2}\right) \tag{2.40}$$

2.4.1 Effect of other noise sources

The above analysis considers only the effect of the noise generated by the tank. To consider also the effect of other noise sources, like the transistors of the cross-coupled pair or the bias generator, it's necessary to consider that the PSD of the noise current generated by the transitors vary along the period and it's not constant anymore. For istance, the PSD of the noise current generated by a transistor in the saturation region is:

$$S_{i_n} = 4kTg_m\gamma \tag{2.41}$$

where γ is a technological parameter which tends to be equal to $2/3$ in case of long channel MOS and it's higher for short channel devices (it can reach values up to 2). To manage with this noise sources (called *cyclostationary noise sources*) a generalization of the ISF is introduced. For each of these noise sources, the *effective ISF* is defined as:

$$\Gamma_{eff}(\tau) = \Gamma(\tau) * \alpha(\tau) \tag{2.42}$$

where $\Gamma(\tau)$ is the usual ISF of the tank, while $\alpha(\tau)$ is a function that takes into account the fact that the noise current PSD is not constant entire the whole cycle and/or it has not the same maximum value of the tank's one. In case of the cross-coupled pair, $\alpha(\tau) = g_m(\tau)\gamma/R_T$

With this remark, the analysis carried on previously is exactly the same, where Γ_{eff} must be used in place of Γ. For this reason, the final result differs from the one in (2.40) only by a proportionality constant, since $\Gamma^2_{eff_{rms}}$ can be different from Γ^2_{rms}. This reasoning is valid for all noise sources, so the total noise PSD differs from the one of the tank only by a proportionality constant, the *noise factor* F. With this consideration, the Leeson equation becomes:

$$S_v(\Delta\omega) = 10log_{10}\left(\frac{(kT/R_T)F}{(C_T V_{LO})^2(\Delta\omega)^2}\right) \tag{2.43}$$

The exact calculation of the noise factor can be find in literature, it involves the calculation (if possible) of the rms value of Γ_{eff}, comparing it with the rms value of Γ, for every noise source. A typical value for a class-B oscillator is around 5. The exact calculation of the noise factor for the tail generator is somehow shown in the next chapter. Instead, for the noise generated by the cross-coupled pair, it's possible to show that it's proportional to the one generated by the tank via γ, with no dependence on all other parameters of the circuit. The proof of this requires long calculations that are extensively presented in [10]. For this reason, the noise factor's increment due to the cross-coupled pair is simply $F_{cc} = \gamma$.

2.4.2 Flicker Noise and effect of the common mode resonance

Up to now, only white noise sources have been considered. However, devices different from the tank also display flicker noise, whose PSD can be modelled altogether with:

$$S_{i_{flick}} = \frac{A}{\Delta\omega} \tag{2.44}$$

where A is a constant that takes into account all the parameters determining the flicker noise that are not frequency dependent. With the same approach used before, flicker noise causes PN in the same way explained in Figure 2.17. However, in this case the PSD is not constant. Using (2.44) instead of (2.41), it's possible to neglect all terms different from c_0 in (2.39), obtaining, doing the next steps in the same way as before, the Leeson equation valid in presence of flicker noise only:

$$S_{v_{flick}}(\Delta\omega) = 10log_{10}\left(\frac{Ac_0^2}{8(C_T V_{LO})^2(\Delta\omega)^3}\right) \tag{2.45}$$

where the dependence on $1/f^3$ is clear. For this reason Phase Noise's plot contains a $-30dB/dec$ slope for low frequencies and the usual $-20dB/dec$ slope for higher frequencies. Of course, the transition between the two parts is not abrupt an there exist a region where both noise contributions are relevant, as Figure 2.18 clarifes. For low frequencies only the flicker noise is relevant. For high frequencies only the thermal noise is significant. Taking the tangent of the plot representing the phase noise for a relatively low value of offset frequency and a relatively high value, the crossing point is somehow an indication on the transition between the two regions. This frequency is called $1/f^3$ *corner frequency* and it can be find by equating (2.45) with (2.40), obtaining:

$$\omega_{1/f^3} = \frac{Ac_0^2}{4kT}R_T \tag{2.46}$$

The effect of the second harmonic resonance on flicker noise is outside the purpose of this thesis that mainly focuses on the thermal region. However, the improving effect of the common mode resonance on flicker noise is an extensively treated topic in literature [9].

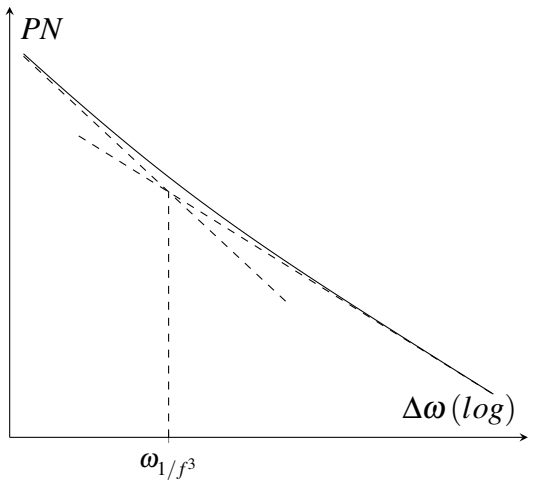

Figure 2.18: *Plot of the phase noise considering also flicker noise*

2.4.3 The figure of Merit (FoM)

Leeson's equation shown in (2.40) can be expressed in several different ways. One of this involves the replacement of the value of the capacitor C_T with $\frac{Q}{\omega_0 R_T}$, where Q is the quality factor of the tank, which is usually dominated by the one of the inductor Q_L.

$$S_v(\Delta\omega) = 10log_{10}\left(\frac{kT}{V_{LO}^2}\frac{R_T}{Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{2.47}$$

Looking at (2.47), it's clear that there's a square dependence of phase noise with respect to the ratio $\omega_0/\Delta\omega$. Moreover, the fact that the phase noise is inversely proportional to the square of the oscillation's amplitude means that it's also inversely proportional to the square of the bias current, namely that it's inversely proportional to the power consumption. For this reason, to compare different topologies of oscillator, working at possibly different frequencies, the *Figure of Merit* (FoM) is defined, normalizing the phase noise with respect to this two quantities [11].

$$FoM = S_v(\Delta\omega) - 20log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) + 10log_{10}\left(\frac{P_{dc}}{1\,mW}\right) \quad [dbC/Hz] \tag{2.48}$$

where P_{dc} is the DC power consumption of the oscillator.

2.5 Different oscillator topologies

To improve phase noise performances, a lot of different circuit topologies have been developed since 90s, trying to improve the phase noise with the same power consumption of the oscillator or the same chip area occupation. The main strategy used to achieve this goal is to increase the current and the voltage efficiency, to reach higher oscillation amplitudes which leads to better phase noise performances. In *Class-C* oscillators, cross-coupled pair devices are designed to operate always in saturation (using a proper bias circuit), and a big capacitor is added in parallel to the tail generator. In this way, the shape of the current is no longer the one reported in Figure 2.9, but it's composed by short pulses, with the current efficiency that is almost equal to 1,

giving an advantage in terms of phase noise. Another solution is the so-called *class-D*, where the tail generator is removed to let the oscillator work in the voltage limited regime. In this way, it's possible to reach higher amplitudes and there's no longer the noise contribution of the bias circuit (which, in a traditional class-B oscillator, can reach the 50 % of the total noise). A lot of other different topologies have been developed,the next chapter focuses on one possible solution to improve phase noise, which is the addition of the second harmonic resonance in the tank. As it'll be clear, there're some advantages that will be extensively discussed. The oscillator making use of the second harmonic resonance is called, in the literature, *class-F2* oscillator [12].

Chapter 3

The class F2 oscillator

3.1 The idea of introducing the second harmonic resonance

As seen in the previous chapter, the current's waveform differs from the theoretical square wave, displaying also even harmonics. Most of the time, the tank has a low impedance for all frequencies different form the resonance's one, giving rise to a sinusoidal oscillation at the drains. In reality, since the impedance of the tank is not zero for frequencies multiples of the oscillation's one, there are some higher order harmonics in the drain waveform, but they're usually negligible and the output waveform can be considered sinusoidal for all practical purposes. However, the presence of a non-zero second harmonic current must be useful to improve the performances of the oscillator, in a way that next subsections explains detailedly.

3.1.1 Class J waveform

This concept is outside the environment of oscillators, but it's the starting point of the entire idea of the thesis. In literature, there exist a type of power amplifier, called *Class-J*, which makes use of a particular voltage waveform at the load, which is shown in Figure 3.1. In power amplifiers, the purpose of the "clipping" in the low side of the sinewave is to prevent the transistor entering the triode region. Similarly, one can think that having that waveform at the drain of the transistor of a traditional class-B oscillator could increase the maximum possible voltage amplitude since the tail generator enters triode region for higher voltages.

To proper understand this concept it's necessary to know the expression of the waveform of Figure 3.1, which is:

$$v = Acos(\omega_0 t) + \frac{A}{2\sqrt{2}} cos(2\omega_0 t) \tag{3.1}$$

where A is a generic value of the amplitude.

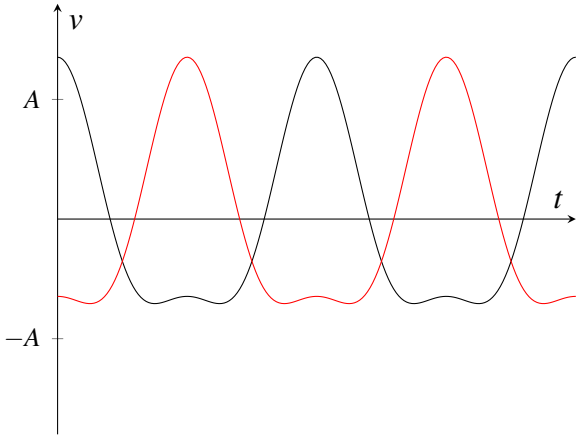

Figure 3.1: *Class-J waveforms, black and red ones have the first harmonic phase shifted by* π

As clear from (3.1), the waveform of Figure 3.1 is composed by two **in phase** sinewaves, with proper amplitude. It's important to notice that, if a time shift by t_0 is applied, waveform's expression becomes:

$$v = Acos(\omega_0(t-t_0)) + \frac{A}{\sqrt{2}}cos(2\omega_0(t-t_0)) = Acos(\omega_0 t - \omega_0 t_0) + \frac{A}{\sqrt{2}}cos(2\omega_0 t - 2\omega_0 t_0) \quad (3.2)$$

Hence, in general, the waveform in Figure 3.1 is represented by a sum of two sinewaves which must have zero phase shift or, if the first has a phase shift θ, the second must have a phase shift equal to 2θ, to have the same waveform, only shifted in time. A particular case is when $\theta = \pi$, in this case the expression becomes (3.3), and it's represented in red colour in Figure 3.1.

$$v = Acos(\omega_0 t + \pi) + \frac{A}{\sqrt{2}}cos(2\omega_0 t + 2\pi) = -Acos(\omega_0 t) + \frac{A}{\sqrt{2}}cos(2\omega_0 t) \quad (3.3)$$

so if the first harmonic is inverted in sign, to keep the same waveform the second one **must not** be inverted in sign. This concept will be crucial in next explanations. Another important thing to notice is that the minimum value of the waveform in (3.2) is actually higher than the minimum value of a sinewave with amplitude A.

3.1.2 Common mode resonance

A way to exploit the fact previously shown is to introduce in the tank the *common mode* resonance. In fact, since the waveforms at the two drains are opposite in sign, they actually have the even harmonics in phase each other, while odd harmonics are in opposition of phase between the two drains. For this reason, the tank may have also a common mode resonance, which can have a frequency different from the *differential mode* one. The usual differential mode impedance is defined as the impedance seen connecting a test generator like the Figure 3.2(a), while the common mode impedance is defined as the one seen with the configuration of Figure 3.2(b). Since the second harmonic is a common mode signal, the voltage at the drain of a device is.

$$v_d = -R_T I_1 cos(\omega_0 t) - R_{T2} I_2 cos(2\omega_0 t) \tag{3.4}$$

where R_T is the usual tank's resistance as defined up to now (differential mode), while R_{T2} is the resistance of the tank at common mode at $2\omega_0$, supposing to have a resonance at twice the oscillation frequency **for common mode signals**. It's important to notice that, in general, I_1 and I_2 can have a non-zero phase. By next expressing them as magnitude and phase, the voltage waveform at one of the drains becomes:

$$v_d = -R_T |I_1| cos(\omega_0 t + \phi_1) - R_{T2} |I_2| cos(2\omega_0 t + \phi_2) \tag{3.5}$$

where ϕ_1 and ϕ_2 are the phase of I_1 and I_2, respectively.

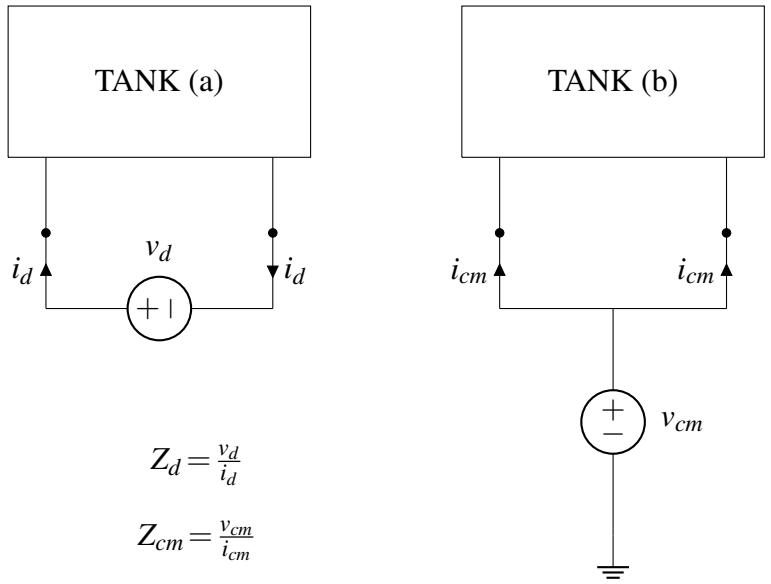

Figure 3.2: *Definition of differential (a) and common mode (b) impedances*

If $\phi_2 = 2\phi_1 + 180°$ the drains' waveform will be equal to the one of Figure 3.1. This is an advantage since the minimum value of the drain voltage is higher than a traditional class-B oscillator and, considering that the voltage drop across cross-coupled pair's devices is the same, it means that the tail generator works with an higher V_{ds}, delivering more current or, countersome, it's possible to have a tail generator with reduced area with the same current delivered by it[1]. However, to have the correct waveform at drains, it's necessary that $\phi_2 = 2\phi_1 + 180°$. If, arbitrarily, $\phi_1 = 0$, to have (3.5) equal to (3.3), it's necessary to have $\phi_2 = 180°$, which means that the second harmonic of the current must be in opposition of phase with the first. If the two are in phase, this technique is not applicable anymore.

To understand why, instead, this tecnicque can be used in traditional class-B oscillators, it's necessary to analyze the drain current's spectrum, in particular the phase of the second harmonic with respect to the first. Considering the example of the previous chapter, it's possible

[1]Drain-to-source saturation voltage is proportional to the square root of the form factor W/L of the transistor, according to short channel model [13]

to (numerically) calculate the first two Fourier coefficient I_1 and I_2 of the waveform of Figure 2.9, obtaining:

$$\begin{cases} \angle \underline{I_1} = 0^\circ \\ \angle \underline{I_2} = 180^\circ \end{cases} \tag{3.6}$$

The first remarkable point is that the theoretical analysis behind the calculation of (3.6) assumes the capacitance connected to the common source to be a short circuit at ω_0. If it's not true, the phase of the second harmonic with respect to the first changes. To retrieve a situation with the right phase shift between I_1 and I_2, adding an extra capacitance, in the order of fF at the source may be necessary. Figure 3.3 show the phase shift between I_1 and I_2 in Example 2.3.1, with respect to the value of an external tail capacitance. It's clear that, after a certain value, what is theoretically claimed by (3.6) is practically true, noticing that "class-J" waveforms are obviously achieved (with some minor differences) even if the phase shift is not exactly 180°, but still a value closer to it. However, in this particular Example, bias current is set to $1.2mA$, since the tank's resistance is fixed to $1k\Omega$. In practical oscillators, the equivalent parallel resistance of the tank is few hundreds of Ω, giving the need of higher bias current. This implies that the transistor creating the current source must be bigger and therefore its parasitic capacitance is already enough to guarantee (3.6) with no external capacitance. This is the reason why, in practical applications shown in the next chapter or in literature [12], this aspect is never considered.

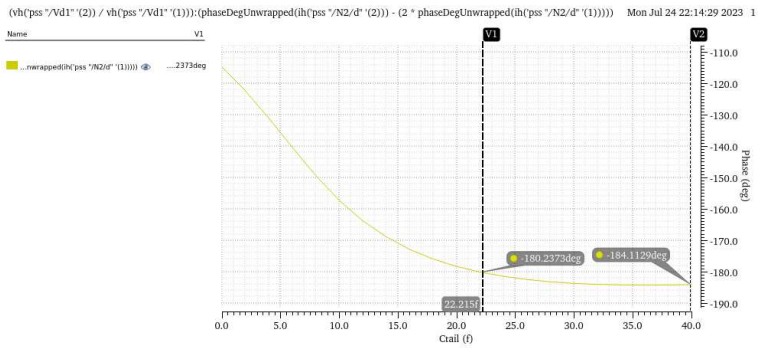

Figure 3.3: *Relative phase between I_1 and I_2 with respect to the external capacitance. After $C_{tail} = 22\,fF$, equation (3.6) is practically true*

Once the condition in (3.6) is verified, it's possible to exploit the presence of the second harmonic by modifying the tank adding the second harmonic resonance, as Figure 3.4 shows.

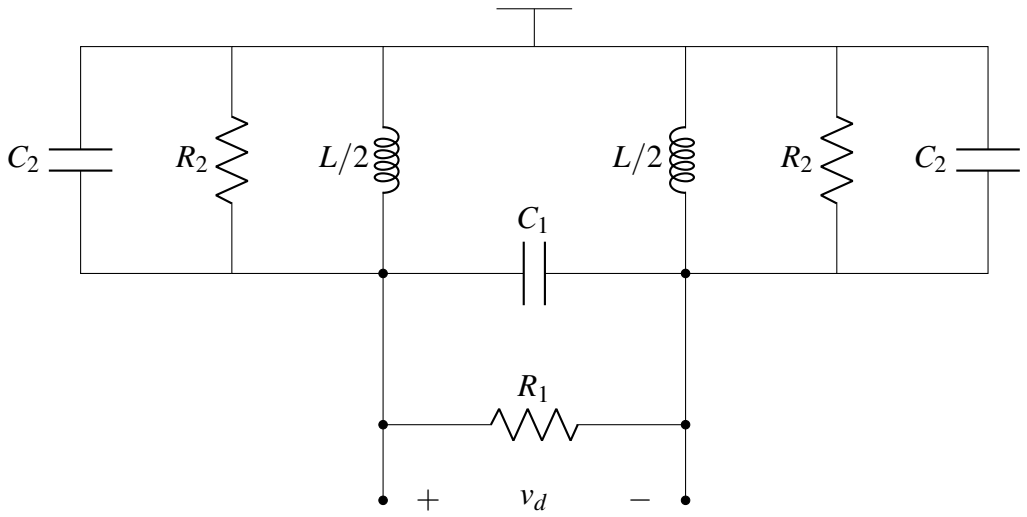

Figure 3.4: *Tank used to exploit the second harmonic resonance*

With a reasoning similar to the one shown before, the resonance frequency for differential signals is:

$$\omega_{dm} = \frac{1}{\sqrt{L(C_1 + C_2/2)}} \tag{3.7}$$

At ω_0, the impedance of the tank is $R_1//(2R_2)$.

From the common mode, instead, it's like C_1 and R_1 were not present. Hence, the circuit is composed by two identical halves that display a resonance at

$$\omega_{cm} = \frac{1}{\sqrt{\frac{C_2 L}{2}}} \tag{3.8}$$

at which the impedance of every half is R_2, that, multiplied by I_2, gives the second harmonic voltage. A class-B oscillator modified using this tank, or an equivalent one, is named in the literature *class-F2*. It gives several advantages in term of phase noise that will be discussed in next sections. It's important to notice that whatever follows is already present in literature but there's no "summary" work that show if, or if not, is possible to sum up all this advantages together.

3.2 Class F2 Waveform

In a class-F2 oscillator, waveform at the drain is no longer sinusoidal. In fact, the presence of the second harmonic resonance gives rise to a voltage at twice the oscillation frequency, which sums with the usual sinusoidal oscillation. For this reason, the drain voltage waveform looks like Figure 3.1. Of course, it depends on the relative amplitude between the first and the second harmonics. Figure 3.5 shows 3 examples of waveform where the amplitude of the second harmonic is changed among different values, keeping the phase shift at the right value, as explained before. Figure 3.6, instead, shows what happens when the phase of the second

harmonic has not the right value. As it's clear, there's no advantage in this case. Moreover, Figure 3.5 shows that the minimum value of the drain voltage is higher than the case of the simple class-B. This implies that, with the same first harmonic amplitude, namely the same differential output voltage, the drain voltage reaches an higher value. This further implies that the minimum voltage at the common source is higher than the class-B oscillator, with the same output amplitude, namely with the same phase noise. Hence, it's possible to increase the bias current entering the voltage limited regime for higher currents, meaning that it's possible to decrease the phase noise by increasing the oscillation amplitude without changing the size of the tail's transistor. On the contrary, it's possible to keep the bias current at the same value, in this case the form factor of the tail's device can be smaller. This further enables to have a less noisy bias' transistor, or simply a smaller one if the chip area is particularly relevant. Depending on the design's constraints, designers can choose between different views of the same concept.

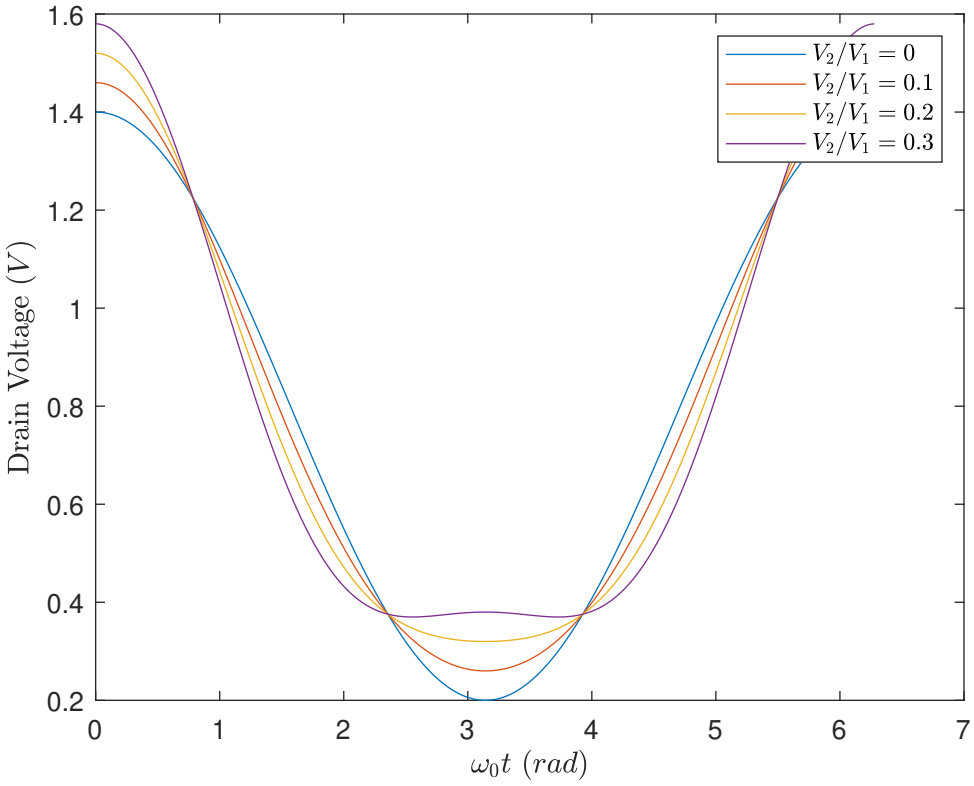

Figure 3.5: *Difference in the waveform changing the ratio between the first and the second harmonic. In this case* $V_{DD} = 0.8\,V$ *and* $V_1 = 600\,mV$

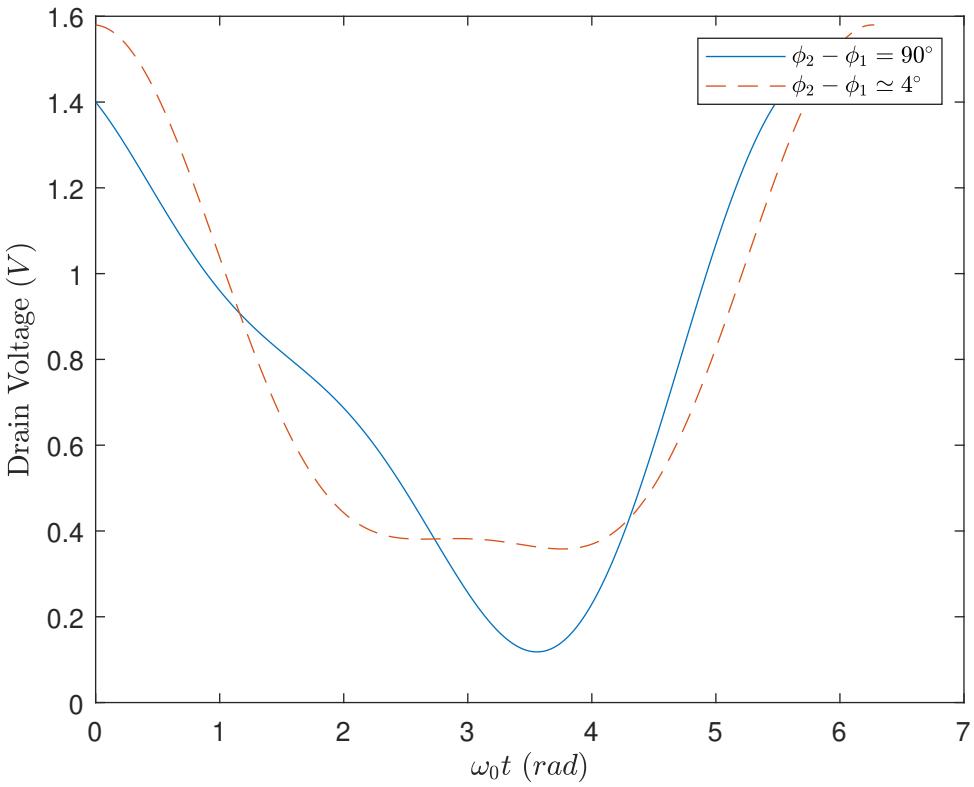

Figure 3.6: *Effects of a phase shift between the harmonics different from* 180°. *Dahsed line, instead, represent the effect of a small error in the phase shift, which causes no significant difference from the ideal case*

3.2.1 Effect on drain current

When the second harmonic resonance is applied, the voltage waveform at drains change. In particular, the minimum value of the drain voltage is higher and this makes the transistor to less enters triode, causing therefore the drain current to move to a more ideal squarewave. This therefore implies that the second harmonic current is lower as the second harmonic voltage is higher, giving rise to a sort of *negative feedback* effect. For this reason, if R_2, for istance, doubles, the second harmonic voltage increases but less than twice, and so on. Figure 3.7 shows what happens applying the tank of Figure 3.4 to the same oscillator of Example 2.3.1, and changing R_2 from $7k\Omega$ to $11.5k\Omega$. As it's clear, the increment in the voltage's value of the second harmonic with respect to the first is not proportional. Moreover, since the square wave is moved toward the ideal one, the ratio between the first harmonic of the current and its average value, namely the current efficiency η_I, increases, approaching the ideal value of $2/\pi$.

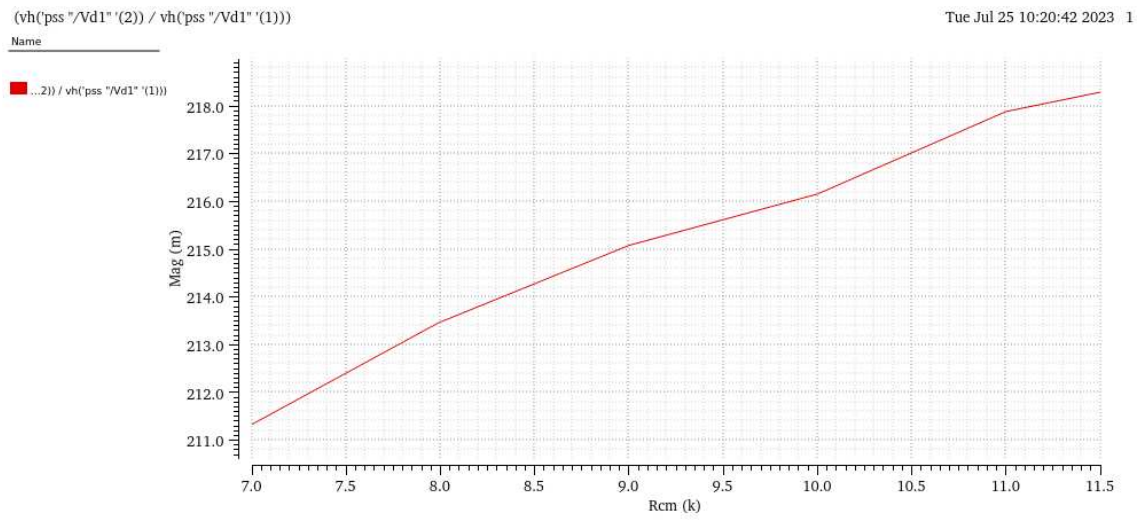

Figure 3.7: *Ratio between the second and the first harmonic of the drain voltage with respect to the value of R_2, keeping $R_1 = 1k\Omega$*

What explained previously suggests that the value of the second harmonic resistance R_2 is not critical, either because of what shown in Figure 3.7, or because the benefit of an higher value if the minimum drain current is obtained for a large range of the second harmonic voltage. Therefore, to get the advantage just shown in a practical design, the presence of the second harmonic resonance is required, not caring too much on the value of it, provided that the second harmonic voltage is at last 15-20 % of the fundamental. This is also what makes this technique to actually be feasible. In fact, in practise, the equivalent parallel resistance at the fundamental R_1, or at the second harmonic R_2, depend on the quality factor of the inductor at ω_0 and $2\omega_0$, respectively, and it's not fully controllable. Figure 3.8 shows a summary of this first advantage, considering again Example 2.3.1 with the modified tank. As it's clear, for the same value of bias current, it's possible to reach higher differential oscillation amplitudes (which implies an improvement in phase noise's performances) or, counterwise, an higher value of the minimum voltage of the common source for the same differential amplitude, which enables to use smaller tail transistor or, in any case, a lower g_m/I_d device (which reduces the noise from the tail generator).

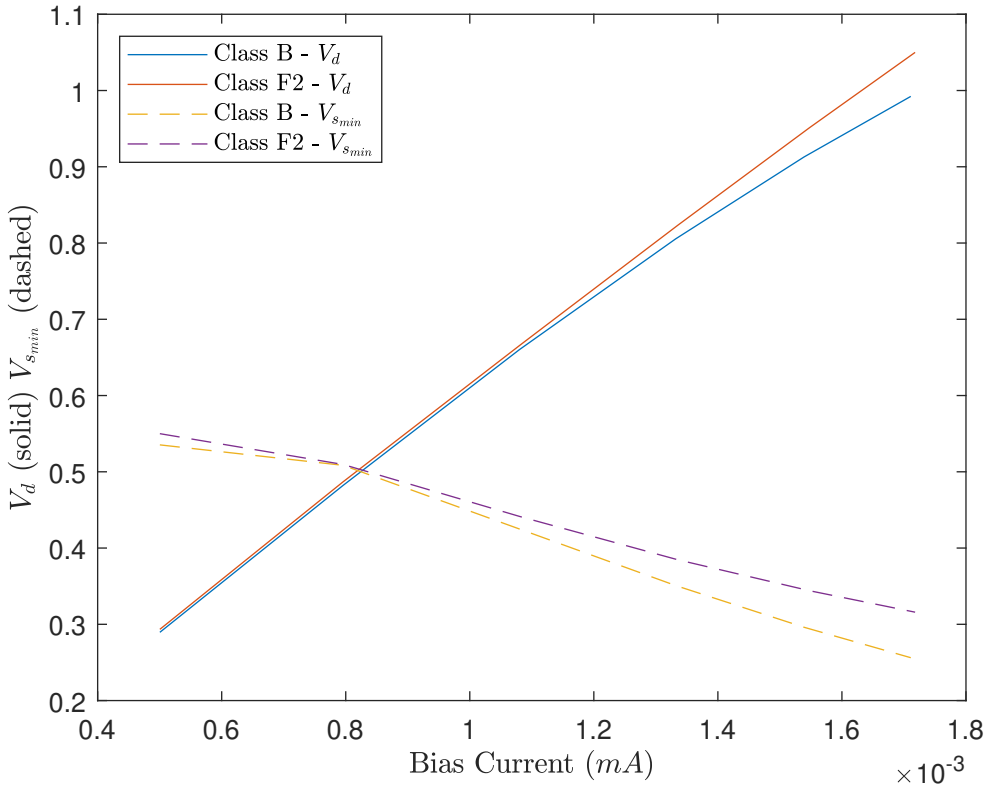

Figure 3.8: *Sweep of the bias current in the two cases. From* 1.2 *mA, current efficiency of class-F2 oscillator is higher than the standard class-B. Also, for the same bias current, the minimum voltage at the common source is higher in the case of the class-F2 oscillator*

However, the presence of the second harmonic has other two beneficial effects on phase noise, that will be explained in the next sections. An important remark is that the main effect of the common mode resonance, as widely discussed in literature [9], is to highly reduce the flicker noise upconversion, as also visible in the example of the last chapter. However, this thesis focuses on the effect of the second harmonic resonance on the thermal noise *only*, which is a topic not perfectly clarified by works dealing with the class-F2 oscillator, despite some numerical simulations without any rigorous proof [14].

3.3 Tail generator's noise reduction

3.3.1 Class-B - Noise from bias current's generator

As explained in the previous chapter, the value of the noise factor in a real oscillator is larger than one. Beyond the tank and the cross-coupled pair, a relevant noise contribution comes from the transitor that generates the bias current. The reason why it's usually relevant, up to the 50% of the total noise, is that normally the tail's transistor is the largest one in the circuit, given that it carries the whole bias current and that it's sometimes necessary to avoid it entering the triode region (which is not necessary at all for the crossed couple). In a traditional class-B oscillator, for an estimation of the effect of the tail generator with respect to the noise from the tank, noise

current from the biasing transistor is modelled as usual, with a parallel current source with power spectral density:

$$S_{i_n} = 4kT\gamma g_m \tag{3.9}$$

For the calculation of the contribution of the noise given by the current source, the simplest model of the oscillator of Figure 2.7 is used. With this model, the noise current coming from the tail generator enters, alternatively, one of the two devices creating the cross-coupled pair. By again reasoning on Figure 2.7, the effect of that noise current is totally equivalent to the current noise of the tank, except for the fact that it occours only for half the period. For this reason, the ISF of the tail generator is:

$$\begin{cases} sin(\omega_0\tau) \text{ if } 0 < \omega_0\tau < \pi \\ 0 \text{ if } \pi < \omega_0\tau < 2\pi \end{cases} \tag{3.10}$$

From which the RMS value of that ISF is:

$$\Gamma^2_{tail_{rms}} = \frac{1}{4}\Gamma^2_{tank} \tag{3.11}$$

From now, calculations are the same performed for the tank, with (3.9) as power spectral density and (3.10) as ISF. By a simple comparison, the noise factor associated to the tail generator is [15]:

$$F_{tail} = \frac{g_m\gamma R_T}{4} \tag{3.12}$$

In reality, devices creating the crossed couple do not operate as ideal switches but rather they have a nonzero series resistance when they are in triode and, moreover, they work in saturation for part of the cycle. For this reason, the ISF in (3.10) becomes much more complicated [10]:

$$\Gamma^2_{tail_{rms}} = \frac{1}{8}\eta(\Phi) \tag{3.13}$$

where $\eta(\Phi)$ is a function of half the commutation angle Φ, namely the angle during which both transistor are in saturation region since the commutation is happening[2]. The function $\eta(\Phi)$ is plotted in Figure 3.9.

Hence, the noise factor differs from the one in (3.12) and it's equal to:

$$F_{tail} = \eta(\Phi)\frac{g_m\gamma R_T}{4} \tag{3.14}$$

For istance, when the conduction's angle approximates 0, (3.12) is retrieved.

[2]Ideally, the commutation is instantaneous and $\Phi = 0$ with the simplified model of Figure 2.7

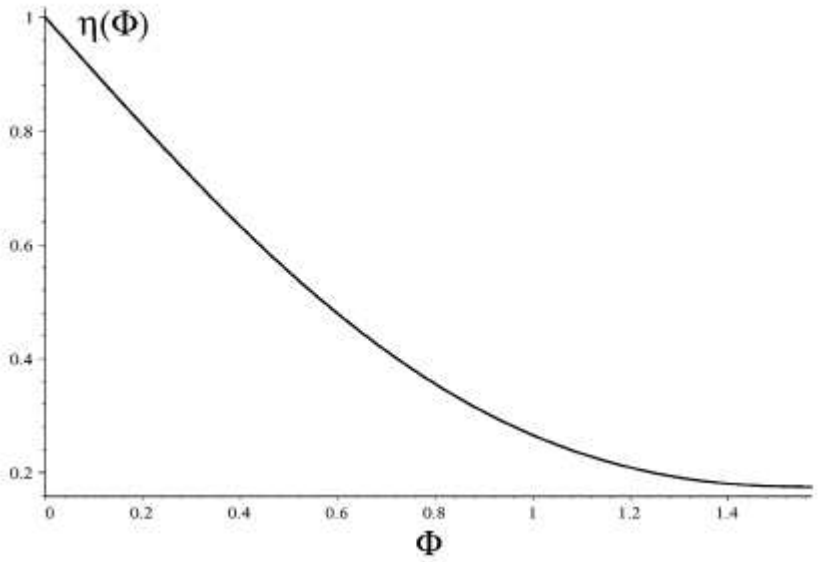

Figure 3.9: *Plot of the function* $\eta(\Phi)$ *[10]. When* Φ *approaches* 0*, the ideal formula is found again*

3.3.2 Tail's noise reduction with common mode resonance

Another phenomenon widely discussed in literature, still related to the presence of the common mode resonance, is the effect that it has on the reduction of the noise coming from the tail generator. To understand the working principle, it's necessary to consider that the current noise generated by the transistor is a common mode signal, since it's applied to the common source of the two transistors. Moreover, the path toward the tank is not the only one possible for the noise current, since the parasitic capacitance connected to the source node is present, too. For this reason, noise current divides into two parts. One flows into the parasitic capacitance and the other flows through the cross-coupled pair to the tank, generating phase noise. If the impedance of the tank at common mode is relevant, as in the case of an explicit second harmonic resonance (as shown before, $R_2 \simeq 10k\Omega$), most of the noise current flows into the parasitic capacitance and the phase noise generated by the tail's device becomes much lower than the case of a traditional class-B, where the relatively low common mode impedance (essentially given by the impedance of the inductor at $2\omega_0$) let all noise current to convert into phase noise. Example 3.3.1 shows the ISF of the tail current generator for a given oscillator with the common mode resonance. In this case, taken form [12], the tank is much more complex, but it can still be modelled as Figure 3.4. Obviously, the amount of noise that is converted into phase noise depends on the value of the second harmonic resistance of the tank R_2 and the impedance of the parasitic capacitance at the source at $2\omega_0$.

Example 3.3.1 (class F2 tail generator noise)
Considering the circuit of the Figure below, with the indicated sizes of devices, the simulated ISF is shown in Figure 3.10. It's clear that noise from current source is practically totally suppressed, with a RMS value of the ISF being equal to 0.04 [12] (while it's equal to $\simeq 1/8$ in the class-B (3.10))

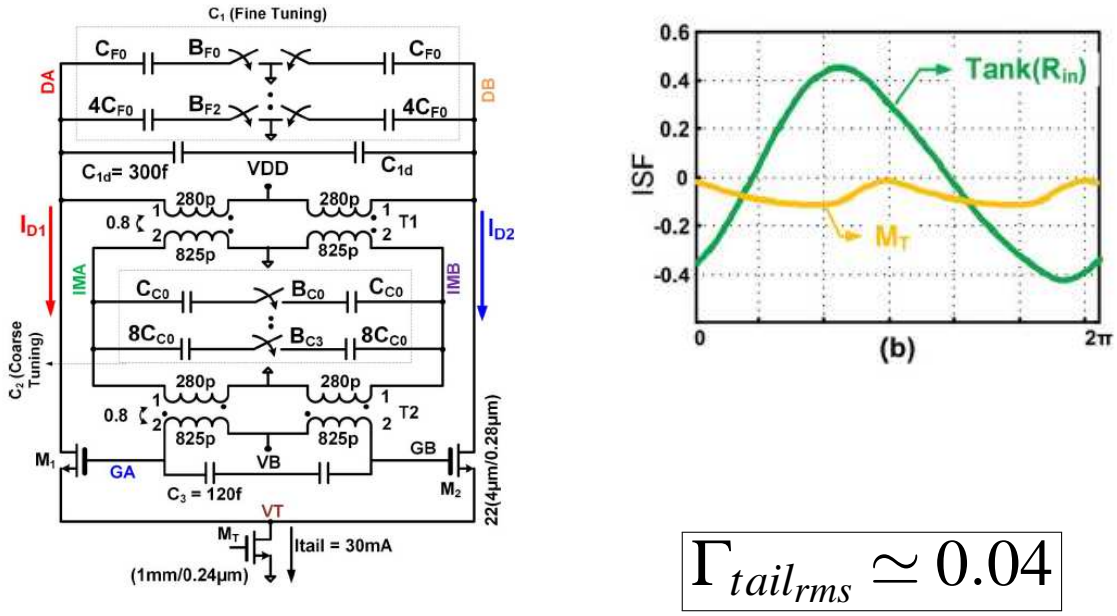

Figure 3.10: *Circuit of [12] (left) and the ISF of the tail generator (right, yellow curve)*

3.4 Effect of second harmonic on noise tank

The last effect of the introduction of the second harmonic is the reduction of the noise generated from the tank. Up to now, the result of the introduction of the second harmonic is to strongly reduce the effect of the tail generator, plus the possibility to increase the oscillation amplitude with the same size of transistors. The last effect that it has is a reduction of the noise from the tank itself. To analyze this counterintuitive effect it's necessary to rely on the complex and general analysis presented in [16], which is valid for any oscillator following the principle schematic of Figure 3.11.

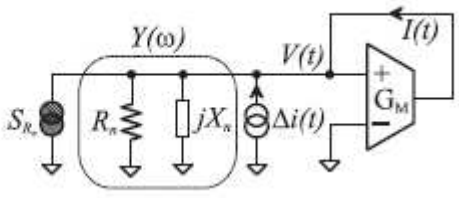

Figure 3.11: *General schematic of an oscillator according to [16]*

The class F2 oscillator actually meets this general structure, since G_m indicated in the Figure can vary freely and it can be either not constant over the period or even frequency-dependent.

The result of the analysis, which requires long and complex calculations that can be find in [16], aims that, in case of a tank with first harmonic resonance with resistance R_1, second harmonic resonance with resistance R_2[3] and the value of the impedance at all other harmonics to be zero, Phase Noise at an offset of $\Delta\omega$ from the carrier, normalized with respect to the **differential** oscillation amplitude and considering the effect of the tank *only*, is:

$$L(\Delta\omega) = 10log_{10}\left(\frac{kT}{\Delta\omega^2}\frac{A_1^2/R_1 + 4A_2^2/R_2}{(A_1^2C_1 + 4A_2^2C_2)^2}\right) \tag{3.15}$$

where A_1 is the first harmonic differential voltage amplitude, A_2 is the common mode second harmonic voltage amplitude, C_1 is the differential equivalent capacitor while C_2 is the common mode capacitance[4]. It's trivial to notice that, when $A_2 = 0$, (3.15) moves back to the usual Leeson equation (with the contribution of the tank only). Also in this case, if the contribution of the cross-coupled pair is considered, [16] proves that, again, the equation is equal to (3.15) simply multiplied by $(1+\gamma)$ (like in the usual class-B oscillator, as stated in the previous chapter). To show this agreement, the result of (3.15) is applied to the circuit of Example 2.3.1, with the modified tank of Figure 3.4, taking the value of the amplitude from the simulation results. Figure 3.12 shows an excellent agreement between theory and simulation, remembering that the contribution from the tail generator is highly reduced by the presence of the second harmonic resonance. Moreover, for the calculation of the phase noise, the value of γ must be known. To obtain this, a simulation testbench, contained in the Appendix, has been developed. One gets: $\gamma \simeq 1.4$[5]

[3] In this subsection *only*, R_2 is supposed to be the common mode resistance as seen at the input port of the tank applying a test generator between ground and the two terminals of the input port shorted together, to be consistent with [16]. Hence, the value is half the one intended up to now

[4] Again, with the same convention used for R_2

[5] The value is strongly higher than the ideal $2/3$. a further proof of the poor validity of the short channel model with deep-scaled technologies, like the 22 *nm* used for the examples of this thesis

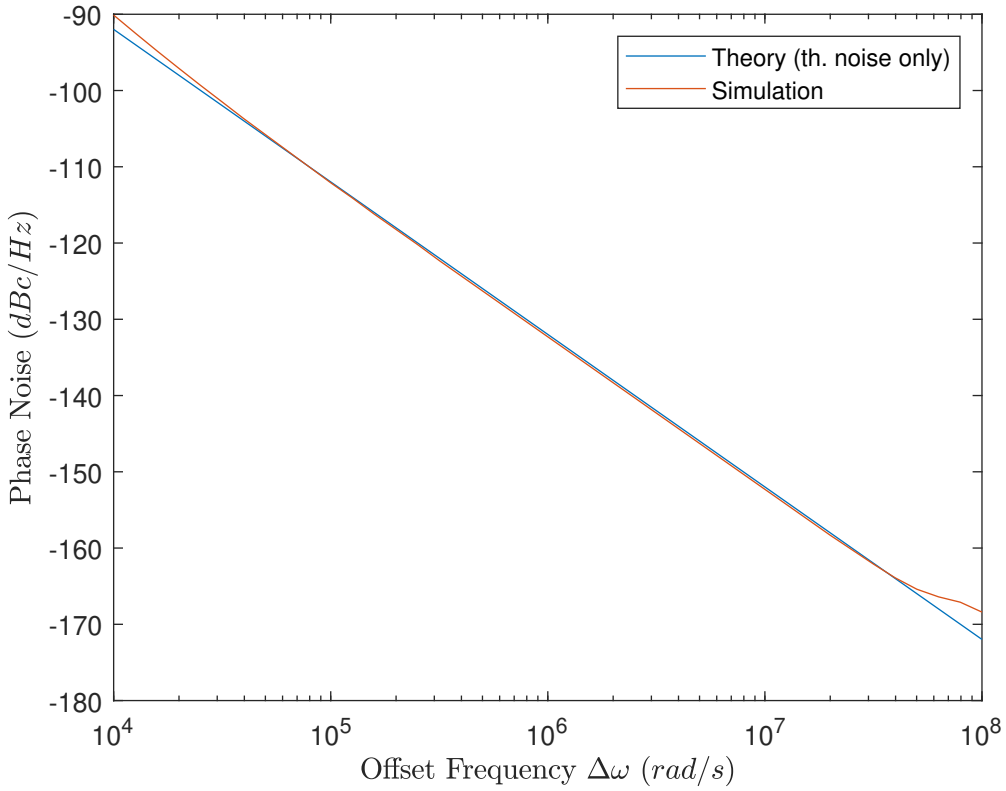

Figure 3.12: *Comparison between simulation and the value calculated using (3.15). The agreement is excellent (in the thermal region).*

To understand when the usage of the second harmonic is relevant or not from a phase noise improvement perspective, it's necessary to manipulate (3.15) to gain some design insight. To do this, let I_1 and I_2 being the first and second harmonic current, respectively, and let k be its ratio I_2/I_1. Let also r being the ratio R_2/R_1 and let q be the ratio between the quality factor of the tank at the second harmonic Q_2 and the same value at the first harmonic Q_1, namely $q = Q_2/Q_1$. With this assumptions, the ratio between capacitances turns out to be:

$$\frac{C_2}{C_1} = \frac{q}{2r} \tag{3.16}$$

By developing (3.15) rewriting the phase noise in terms of I_1, k, r, q and R_1, making use of (3.16), one gets:

$$L(\Delta\omega) = 10log_{10}\left(\frac{kT}{\Delta\omega^2}\frac{A_1^2/R_1}{(A_1^2C_1)^2}\frac{1+16rk^2}{(1+8rk^2q)^2}\right) \tag{3.17}$$

Next, it's necessary to consider that r, which is the ratio of the resistances, is not independent on q, since, in the case of the considered class-F2 oscillator, R_1 and R_2 represent the equivalent differential and common mode resistances of the tank at ω_0 and $2\omega_0$, respectively. For this reason:

$$r = \frac{R_2}{R_1} = \frac{2\omega_0 LQ_2}{2}\frac{1}{Q_1\omega_0 2L} = \frac{q}{2} \tag{3.18}$$

where (2.5) has been used. By substituting (3.18) into (3.17), (3.19) is finally obtained, where the phase noise is expressed as a function of I_1, R_1, k and r, beyond the usual parameters contained into the standard Leeson equation.

$$L(\Delta\omega) = 10log_{10}\left(\frac{kT}{\Delta\omega^2}\frac{A_1^2/R_1}{(A_1^2C_1)^2}\frac{1+8qk^2}{(1+4k^2q^2)^2}\right) \tag{3.19}$$

3.5 Phase noise advantages of class-F2

After the detailed analysis of the main different noise sources of the class-F2 oscillator, an overall summary is presented. Since the effect of the common mode resonance in the flicker noise upconversion is already known and outside the purpose of this thesis, the following analysis focuses only on the thermal region, summarizing what are the advantages in term of phase noise if a second harmonic resonance is used instead of a traditional class-B topology. The concept will be practically shown also in the design example of the next Chapter. As discussed in previous sections, a class F2 oscillator gives advantage in term of phase noise via three different mechanisms that happen when a second harmonic resonance is introduced in the tank:

1. Reduction of the noise coming from the tail device;
2. Reduction of the overall noise coming from the tank;
3. Higher minimum drain voltage that allows higher current efficiency;

3.5.1 Reduction of the noise from tail generator

The first effect of the presence of a common mode resonance is the reduction of the noise coming from the tail generator, as already explained previously. To quantify the improving in terms of PN, the total noise factor of a class-B oscillator must be considered:

$$F = 1+\gamma+\frac{g_m\gamma R_T}{4} \tag{3.20}$$

When the common mode resonance is applied, noise factor moves approximately to $1+\gamma$. For this reason, there exist a strong improvement in phase noise's performances of the oscillator, that depends on the parameters of the tail device. Example 3.5.1 shows a quantitative analysis of the improvement given by the second harmonic resonance, considering some typical range for the parameters in (3.20)

Example 3.5.1 (Effect of the tail generator)
For a typical submicron technology, the value of γ is in the order of 1.5. Since R_1 is determined by the quality factor of the inductor, it usually reaches value up to 300Ω. Values of g_m, instead, are determined by the "equivalent" overdrive voltage V^* and the bias current I_D:

$$g_m = \frac{2}{V^*}I_D \tag{3.21}$$

giving values in the order of $10-20mS$. With this values, the last term in (3.20) is in the order of 2. In general, the contribution of the tail generator can reach up to the 60% of the total. Removing this contribution is worth a phase noise's improvement of about $3dB$. The tail generator can be designed judiciously, avoiding unnecessary high values of g_m/I_D, namely high value of W/L, but its contribution is anyway at least 20% of the total, giving still around $1dB$ penalty in PN.

3.5.2 Reduction of the overall noise coming from the tank

Another effect, which cannot be explained in an intuitive way, despite from some numerical simulations, is the reduction of the noise coming from the tank when the second harmonic resonance is present. To explain this, (3.17) is used, comparing it with itself but in case of $A_2 = 0$, given by (3.22).

$$L(\Delta\omega) = 10log_{10}\left(\frac{kT}{\Delta\omega^2}\frac{A_1^2/R_1}{(A_1^2C_1)^2}\right) \tag{3.22}$$

The amount of phase noise's improvement is obtained dividing the full expression in (3.17) by (3.22), eventually expressing the result directly in dB;

$$PN_{improv_{dB}} = 10log_{10}\frac{1+16rk^2}{(1+8rk^2q)^2} \tag{3.23}$$

To better visualize (3.23) there are two possible representations. One makes use of the contour plot of (3.23), in which the phase noise's improvement (or eventually the phase noise's penalty) are plotted with respect to the value of r and q, for a given k. Figure 3.13 shows the result for $k = 0.2$, while Example 3.5.2 makes use of this result applying it to the Example 2.3.1.

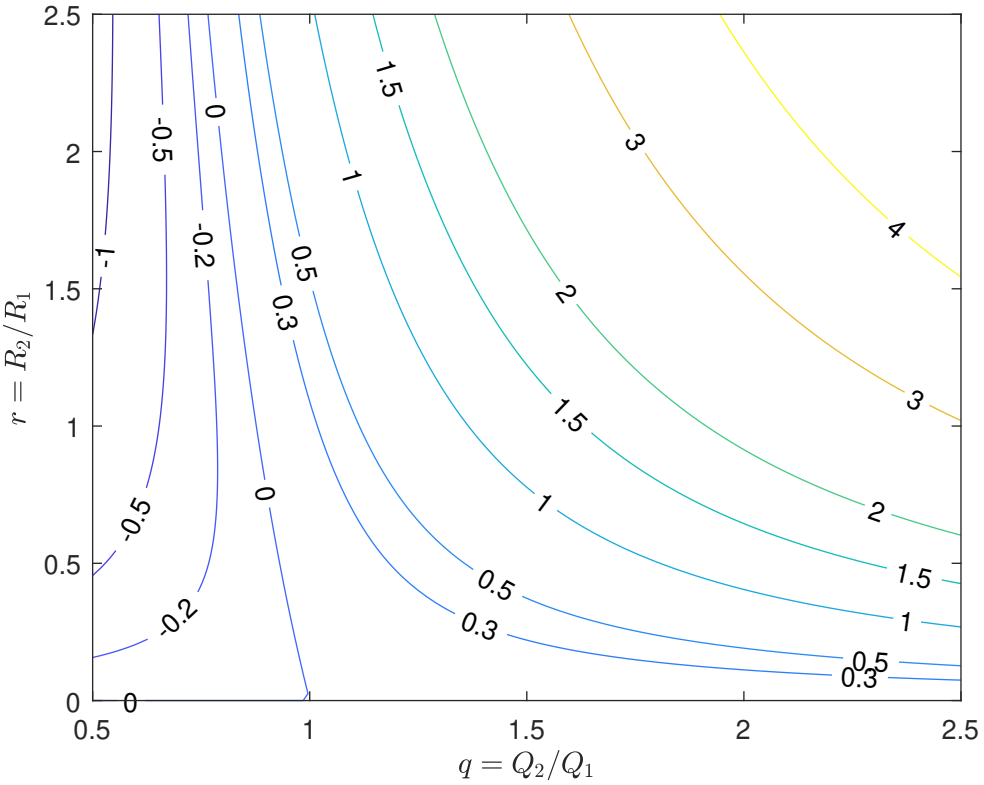

Figure 3.13: *Contour plot of (3.23), negative values accounts for Phase Noise's penalty. All values are expressed in dB and are referred to the case of* $k = 0.2$.

Example 3.5.2

Considering again Example 2.3.1, with the usual modified tank, from the simulation one gets $k = 0.025$. In this case, q and r are equal to:

$$\begin{cases} r = \frac{R_2}{R_1} = 5 \\ q = \frac{Q_2}{Q_1} = \frac{2\omega_0 R_2 C_2}{\omega_0 R_1 C_1} = 2r\frac{C_2}{C_1} \simeq 4.98 \end{cases} \tag{3.24}$$

(3.23) gives $\simeq 0.8\,dB$ as result, which corresponds, in linear scale, to $\simeq 0.83$. Actually, Figure 3.14, showing the noise summary, confirms it.

Device	Param	Noise Contribution	% Of Total
/R0	rn	6.43682e-17	37.71
/N2	therm_Rg	2.58862e-17	15.16
/N0	therm_Rg	2.58861e-17	15.16
/N2/slvtnfet_mmw_5t/rgres1	rn	1.15863e-17	6.79
/N0/slvtnfet_mmw_5t/rgres1	rn	1.15862e-17	6.79
/N7	therm_Rg	5.61701e-18	3.29
/R4	rn	3.28761e-18	1.93
/R3	rn	3.28759e-18	1.93
/R1	rn	2.8582e-18	1.67
/N2/slvtnfet_mmw_5t/rgres	rn	2.38621e-18	1.40

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.70706e-16
No input referred noise available
The above noise summary info is for pnoise_pm data

Device	Param	Noise Contribution	% Of Total
/R0	rn	7.83964e-17	29.23
/N7	therm_Rg	3.93615e-17	14.67
/N0	therm_Rg	3.13625e-17	11.69
/N2	therm_Rg	3.13625e-17	11.69
/R1	rn	2.09284e-17	7.80
/N2/slvtnfet_mmw_5t/rgres1	rn	1.48177e-17	5.52
/N0/slvtnfet_mmw_5t/rgres1	rn	1.48176e-17	5.52
/N2/slvtnfet_mmw_5t/rgres	rn	3.042e-18	1.13
/N0/slvtnfet_mmw_5t/rgres	rn	3.04198e-18	1.13
/N9	flicker	2.89949e-18	1.08

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 2.68239e-16
No input referred noise available
The above noise summary info is for pnoise_pm data

Figure 3.14: *Noise Summary of Example 3.5.2 (upper part), compared with a class-B oscillator with the same parameters (lower part). It's possible to notice the improvement in the phase noise from the tank (R_0), of about* 0.82*, in linear scale.*

However, as stated before, the value of r is dependent on the value of q in a tank realized with real components. For this reason, the phase noise's improvement can easily be understood by using (3.19), comparing again with the case in which $A_2 = 0$. After that, Phase Noise improvement can be plotted with respect to the single variable q, for different value of k, taken as parameter. The result is shown in Figure 3.15, where values of q spans from 1 to 1.5. This choice is not random: in an ideal inductor, the quality factor is proportional to the frequency, so the theoretical value of q should be equal to 2. However, nonidealities such as skin effect make Q to be sublinearly dependent on ω_0, giving rise to values of q less than 2[6]. Figure 3.15 shows that there always exist an improvement, especially when q is greater than around 1.3. This tells that the approach is worth of a relevant improving in PN only in the case that the inductor used in the design have the quality factor at $2\omega_0$ higher than the same value at ω_0. For this reason an analysis of the technology must be done before the design to understand if this method can be useful or not. In the last chapter, where a design example is given, the inductor used in the circuit effectively has this property.

[6]In practise, it's difficult to reach values larger than $\simeq 1.5$

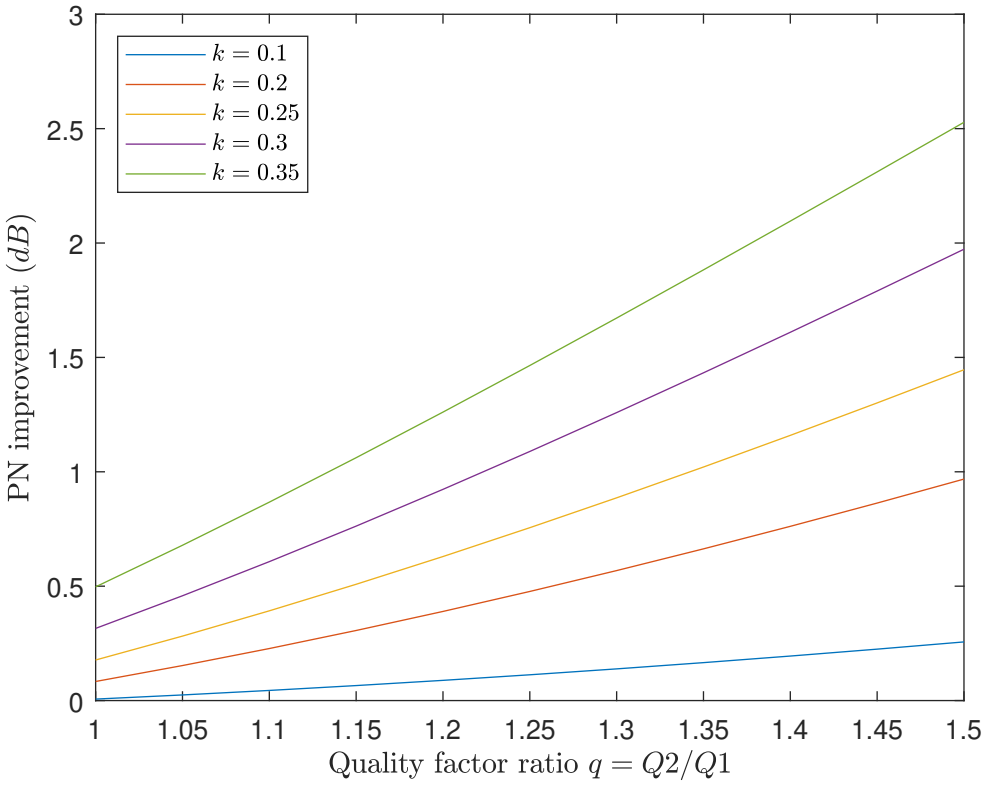

Figure 3.15: *Phase Noise improvement with respect to the quality factor ratio.*

3.5.3 Increasing in the current efficiency

The last advantage in terms of phase noise of the class-F2 oscillator is the increasing of the current efficiency due to the increasing of the minimum drain voltage with respect to a normal class-B oscillator. Figure 3.8 shows how the differential oscillation's amplitude varies with respect to the bias current, in the circuit of Example 3.5.2. It's possible to see that for low currents the two oscillators behave equally, but increasing the bias current the class-B oscillator starts entering the voltage limited regime **before** the class-F2, since the minimum drain voltage of the latter is higher (for the same current's value). Therefore, if the oscillator is used in that region, the oscillation's amplitude is higher, for the same value of the bias current, namely, for the same power consumption. This leads to a phase noise's improvement simply due to the increasing in the oscillation's amplitude[7], that can be visualized, still in case of Example 3.5.2, by plotting the phase noise with respect to the bias current, at an offset frequency of $\Delta\omega = 10MHz$[8]. The result is shown in Figure 3.16, where it's possible to see that, for lower value of I_{bias} the difference between the two oscillator is around $2dB$ (due to the other two mechanisms previously explained), while it enlarges for higher values of the bias current, exploiting this last mechanism.

By summarizing all this aspects, it's possible to aim, for a class-F2 oscillator, a phase noise improvement, with respect to the traditional class-B oscillator, from $2dB$ (if the noise from the

[7] Phase noise is proportional to the **square** of the oscillation amplitude

[8] This relatively high value of offset frequency guarantees that the flicker noise is highly negligible

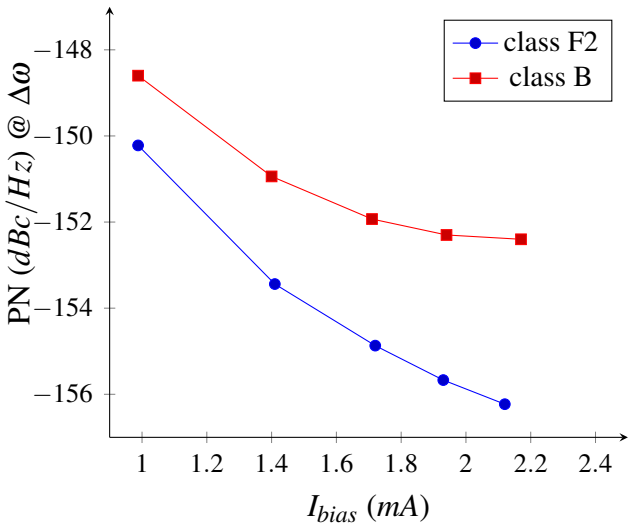

Figure 3.16: *Comparison of Phase Noise between class B and class F2 oscillators, both considering Example 2.3.1, with different tanks.*

tail generator is low) up to $5-6dB$, if the noise from the tail's device is relevant. Another point to be noticed is that all the concepts previously shown have already been studied in literature, but they've never been analyzed together or specifically for the class-F2 oscillator. In particular, the analysis about the quality factor ratio is nowhere present in literature.

3.6 Chip area saving of class-F2 oscillator

Another aspect not clearly discussed in literature is a quantification of the area saving from the usage of the second harmonic resonance. To exploit this fact, the quantification of the increment in the minimum value of the voltage waveform must be done priorly. Table 3.1 shows the minimum value of the voltage waveform, for different values of the second harmonic, expressed with respect to the first, for a fixed first harmonic amplitude of $600mV$ [9], measuring the minimum value from the average value of a pure sinewave with the same amplitude. As it's clear from the Table, there's always (even for small amplitudes of the second harmonic), an advantage in term of the minimum voltage, gaining extra "voltage headroom" for the cross-coupled pair's voltage (remembering that the minimum drain voltage is achieved when the corresponding transistor operates in triode), or the possibility to have an higher $V_{D_{sat}}$ for the tail generator. If the choice is to use this "free voltage headroom" to lower the W of the transistors forming the cross-coupled pair, the voltage across them in triode is inversely proportional to their W. For this reason, if there's the possibility to increase the voltage across the cross-coupled pair's transistors by a given amount, its dimension can also be reduced by the same amount. Table 3.1 shows, in the third column, the amount of W that can be reduced, making the hypothesis to start from a situation when the ON voltage is $100mV$ (when $V_2 = 0$). Fixing the gate length, that numbers directly corresponds to the area saving for the cross-coupled pair.

[9] This values corresponds to a differential amplitude of $1.2V$, which is a typical value for a technology with $V_{DD} = 0.8V$

V_2/V_1	Gaining V_{min} at drains	Relative W_{cc} saving (each device)	Relative W_{tail} saving
0.1	$60mV$	1.6	1.5
0.15	$90mV$	1.9	1.8
0.2	$120mV$	2.2	2.2
0.25	$150mV$	2.5	2.6
0.30	$170mV$	2.7	2.8
0.35	$176mV$	2.8	2.9

Table 3.1: *Area saving with respect to the amount of second harmonic voltage, for* $V_1 = 600mV$ *(single-ended)*

Another possibility is to keep the crossed couple fixed and reduce the size of the tail generator. Since the minimum voltage required by the transistor to operates in saturation $V_{D_{sat}}$ is, according to the short channel model [13], inversely proportional to $\sqrt{W}$, with a similar reasoning it's to possible to derive the last column of Table 1.2. However, in this case, a typical value for V_{dsat} is about $250mV$, so the area saving is different with respect to the previous case. Of course, the designer could also use a combination of this two techniques as his choice, to minimize the overall chip area of the particular design.

3.7 Application of the second harmonic resonance to other oscillator's topologies

As briefly seen at the beginning of this chapter, to get the correct waveform at drains the mandatory condition is that the phase shift between the first and the second harmonic of the drain current must be 180°. If this is not the case, the technique is no more advantageous. To detailedly explain this fact a different oscillator topology, in this case the class-C, is considered. In the class C topology, a big capacitance is added to the common source and a different bias voltage is applied to the gate of the devices (in a traditional class-B oscillator, the bias voltage of the gate is V_{DD}, like the one at drains). This two differences enable the cross-coupled pair to work always between saturation and OFF condition, without entering triode. The shape of the current of a class-C oscillator is no longer a squarewave, but it's composed of short and tall current pulses, as Figure 3.17 explains. However, if the phase of the second harmonic is calculated on the waveform of Figure 3.17, the result is that first and second harmonic are **in phase**. If, again, the tank displays a common mode second harmonic resonance, the drain voltage's expression will be equal to the one in (3.5), but, in this case, $\phi_1 = \phi_2 = 0°$, so the drain voltage is:

$$v_d = -R_T|I_1|cos(\omega_0 t) - R_{T2}|I_2|cos(2\omega_0 t) \tag{3.25}$$

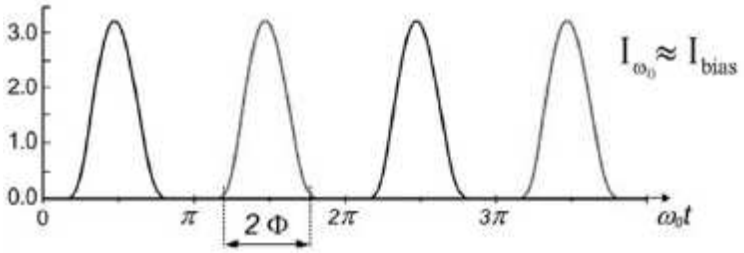

Figure 3.17: *Current shape in a class-C oscillator*

whose plot is represented in Figure 3.18. It's evident that, in this case, there's no advantage at all, but rather the minimum drain voltage is lower and this further makes the current efficiency to get worse and require bigger devices, a situation totally opposite to what happens in the class-F2.

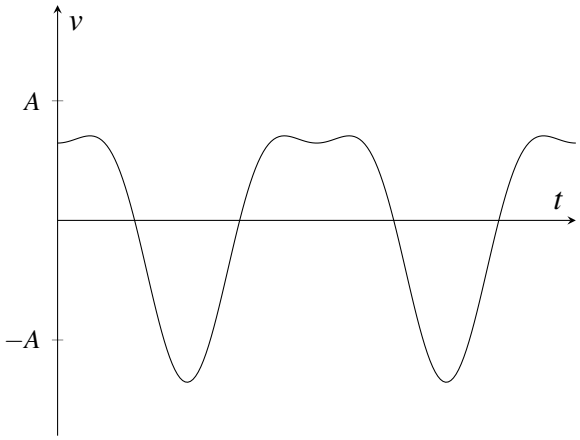

Figure 3.18: *Drain voltage of a class-C oscillator with second harmonic resonance, with A as amplitude of the first harmonic*

Chapter 4

Design Issues and an Example

Despite of the characteristic that the inductor must have in order to fully exploit the advantages shown in the previous chapter, there's one other main issue that must be taken into account in a design of a real class-F2 oscillator, which is related to the way that can be used to implement a tuning. In fact, in this case tuning is much more complicated than an oscillator without the second harmonic resonance, as discussed later. After the discussion on the problem of the tuning, a real example is provided, that reaches the state-of-the-art specifications. Since the purpose is to show a circuit with all real components, contrary on what have been shown up to now, and the purpose of the thesis is not to reach given specifications, the design procedure is slightly different from a typical design flow. In fact, the starting point will be the Example proposed up to now, where the sizing of the transistor have already been explained, scaling it according to an higher value of the bias current, considering that the inductor has not a value of Q such high as the case with ideal components, where the quality factor can be chosen freely.

4.1 The problem of tuning

If a class-F2 *Voltage Controlled Oscillator* must be designed, the usual tuning technique can be applied. However, the fact that there's a second harmonic resonance must be taken into account, considering that if the resonance at first harmonic is increased to modify the oscillation's frequency, the second harmonic resonance must be varied appropriately. In literature various types of tank are proposed such that they provide the second harmonic resonance. However, in the following a simple tank looking like the one shown before is used (Figure 3.4). Of course, resistances are removed and the resistive part is created by the equivalent parallel resistance of the inductor given by (2.5), obtaining the tank of Figure 4.1, where also parasitic capacitances, either differential or single-ended, are represented. By calculating the differential and common mode resonance frequency one gets:

$$\omega_{dm} = \frac{1}{\sqrt{L(C_1 + C_{pd} + C_2/2 + C_{pcm}/2)}} \tag{4.1}$$

$$\omega_{cm} = \frac{1}{\sqrt{(L/2)(C_2 + C_{pcm}/2)}} \tag{4.2}$$

from which the value of C_1 and C_2 giving the correct operation of the tank are:

$$C_2 = \frac{2}{L}\frac{1}{\omega_{cm}^2} - C_{pcm}/2 \tag{4.3}$$

$$C_1 = \frac{1}{L}\frac{1}{\omega_{cm}^2} - C_{pcm}/2 - C_2/2 - C_{pd} \tag{4.4}$$

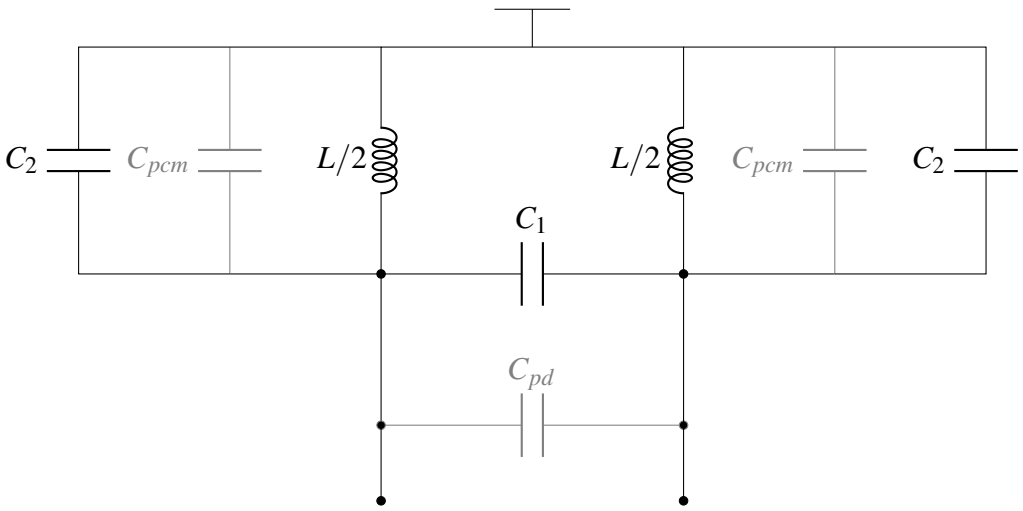

Figure 4.1: *Tank used in the design example, where also parasitics are represented in light colour*

Despite of the presence of the parasitics, values of C_1 and C_2 can be varied appropriately to reach the exact oscillation frequency at ω_0 and the common mode resonance at $2\omega_0$. When this situation is achieved, the oscillator is perfectly tuned. If now the frequency needs to be varied, C_1 and C_2 must be moved to C_1' and C_2', in such a way that, if ω_0' is the new oscillation frequency, the common mode must resonate at $2\omega_0'$. With the new values, (4.4) and (4.3) becomes:

$$C_1' = \frac{1}{L}\frac{1}{\omega_{dm}'^2} - C_{pcm}/2 - C_2'/2 - C_{pd} \tag{4.5}$$

$$C_2' = \frac{2}{L}\frac{1}{\omega_{cm}'^2} - C_{pcm}/2 \tag{4.6}$$

Calculating the difference $\Delta C_2 = C_2' - C_2$ one gets:

$$\Delta C_2 = \frac{2}{L}\left(\frac{1}{\omega_{cm}'^2} - \frac{1}{\omega_{cm}^2}\right) \tag{4.7}$$

With the same procedure for ΔC_1, (4.8) is obtained:

$$\Delta C_1 = \frac{1}{L}\left(\frac{1}{\omega_{dm}'^2} - \frac{1}{\omega_{dm}^2}\right) - \frac{\Delta C_2}{2} = \frac{3}{2}\Delta C_2 \tag{4.8}$$

Observing the equation, it's clear that the frequency variation is not dependent on parasitics, provided that they remain the same. Moreover, whatever are ΔC_1 and ΔC_2, the former must be $3/2$ the latter. Hence, to design a tuning circuit that sweeps the frequency from f_{min} to f_{max}, the following procedure must be used:

1. Starting from a circuit tuned at f_{max}, the amount of the maximum "extra" C_1 needed is calculated using (4.7).

2. The value of C_2 must be properly increased with the correct proportionality to keep the common mode resonance at the correct value.

4.1.1 Discrete tuning

Typically, in all oscillators the tuning is performed adding capacitors to the tank, to lower the oscillation frequency. This is done dividing the total capacitance that must be added to move from f_{max} to f_{min} in a binary way, with a given number of bits N, that provide a minimum addable capacitance of $C_{min} = \Delta C/2^N$. The circuit typically used is shown in Figure 4.2, where capacitors are scaled in a binary way (C_{min},$2C_{min}$,$4C_{min}$,...). In this way, sweeping the binary number from 0 to $2^N - 1$, the full range is covered, with a minimum step given by C_{min}.
Circuit in Figure 4.2 is a single ended version. However, tuning capacitors can also be added in a differential way, by using the circuit of Figure 4.3.

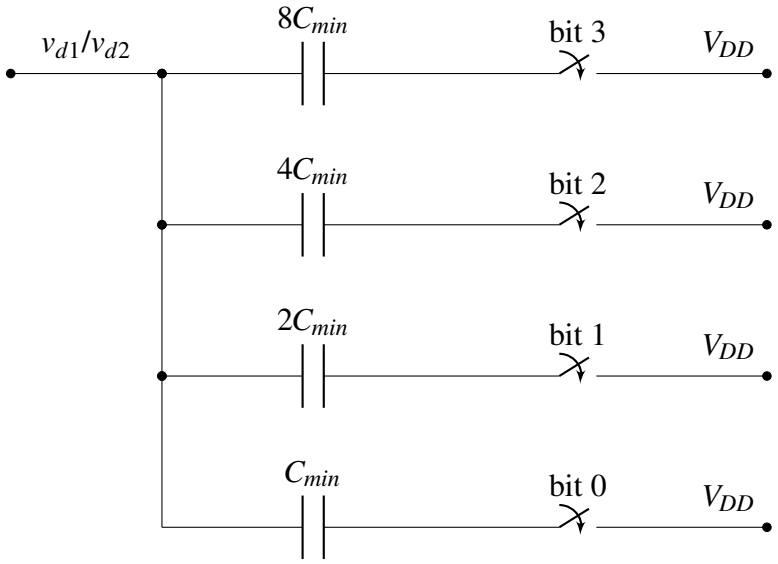

Figure 4.2: *Circuit for single-ended discrete tuning, with, just as an example, $N = 4$*

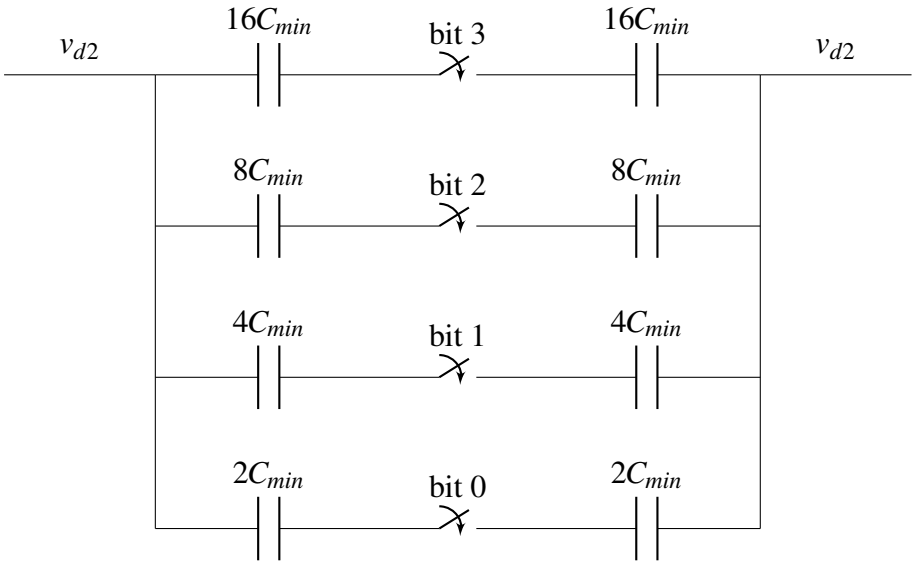

Figure 4.3: *Circuit for differential discrete tuning, with, just as an example,* $N = 4$

In both cases, switches are implemented using transistors working in triode. The size of the transistors must be chosen such that they're not too small to introduce too high series resistance, that lowers the quality factor of the tank, but not too big such that the parasitic capacitance introduced by them when they're off is relevant. Normally, if the tuning capacitors are scaled in a binary way, also transistors are, since lower capacitance value involves less current in a proportional way. In a class-F2, both differential and tuning capacitor are used, with a fixed ratio of $3/2$. Obviously, both differential and common mode tuning banks must be use the same number of bits.

4.1.2 Fine tuning

On the top of the discrete (or *Coarse*) tuning, a fine tuning is applied to modify the frequency for values lower than the one covered by a bit. For this purpose, typically a varactor is used, in a circuit like the one in Figure 4.4. The size of varactors is such that, changing the control voltage V_{tune} from 0 to V_{DD}, the capacitance changes more than C_{min}, so covering all the frequencies continuously. However, Figure 4.4 shows immediately that the structure is intrinsically single ended, since the tuning voltage is an ac ground at the oscillation frequency, and it's not possible to add differential tuning varactors. In a typical harmonic oscillator this is not a problem, but in a class-F2 it can be, since the rule derived before is violated, adding a single ended capacitance with no corresponding differential one. For this reason, the number of bits N, in a class-F2 structure must be at least 4 or 5, such that the range covered by the varactor is so small that this detuning is negligible. To better quantify the minimum number of bits, the bandwidth of the tank at the second harmonic must be considered. Since the bandwidth over the which the impedance can be considered equal to R_2 is $\frac{2\omega_0}{Q_2}$, the range covered by varactors must be well below that number. In the following design example the explicit calculation is included, too.

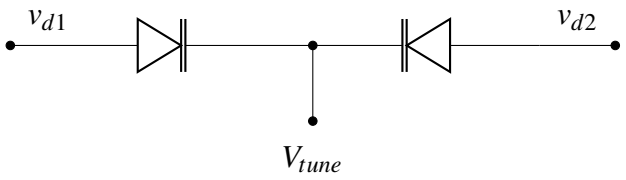

Figure 4.4: *Circuit for fine tuning*

4.2 Design Example

4.2.1 Design procedure

To design the oscillator, the starting point is the choice of the inductor. The technology used is a 22-nm FDSOI technology, manufactured by GlobalFoundries, which includes some passive elements together with the cadence model. The operating frequency is chosen to be $5GHz$, in such a way that parasitic components are not extremely relevant. At this frequency, a $800pH$ inductor exhibits a quality factor of $Q_1 = 15$, while, at $10GHz$, it is $Q_2 \simeq 17$. According to the discussion of the previous chapter, this gives a tank's Phase Noise improvement, which depends on k. Since, in the Example 2.3.1, cross-coupled pair is already composed of real devices, as well as the tail generator, values indicated there are considered as a starting point. However, in the aformentioned example the resistance of the tank at the oscillation frequency is $1k\Omega$, while in the real case is about 370Ω[1]. For this reason, the bias current is increased to $6mA$, reaching a value actually more inline with a typical real oscillator. Of course, the output voltage amplitude will be larger than the previous case. The increasing of the current must be followed by an appropriate scaling in the size of transistors. Therefore, the width of the cross-coupled pair is set to $W_{cc} = 40\mu m$ as well as the tail generator, $W_{tail} = 40\mu m$. Lengths are kept at the same value[2]. For capacitors, models of real MOM capacitors are used, in place of ideal ones. Since class-F2 operation highly reduce not only the noise coming from tail's device, but also the one generated by the reference branch of the current mirror, there's no need to add a proper bias' filter, as it's usually done in other oscillator topologies [9]. The width of the reference transistor is chosen to be equal to $W_{ref} = 8\mu m$, with a mirror ratio of 5. The tuning range, defined as:

$$TR = \frac{f_{max} - f_{min}}{f_0} \tag{4.9}$$

is chosen, taking some margin, to be 20%. For this reason, $f_{max} = 5.5GHz$,$f_{min} = 4.5GHz$. Hence, value of fixed capacitors *should* be calculated using (4.4) and (4.3), tuning the oscillator at f_{max}. Since parasitics are not known exactly, it's easier to use that values as a starting point and fine tune the oscillator relying on simulations, obtaining:

$$C_1 = 347.9fF \tag{4.10}$$

[1] Value calculated using (2.5)
[2] $L_{cc} = 18nm$, $L_{tail} = 50nm$

$$C_2 = 111.9fF \tag{4.11}$$

After that, ΔC_1 and ΔC_2 are calculated, obtaining:

$$\Delta C_1 = 182.25fF \tag{4.12}$$

$$\Delta C_2 = 121.5fF \tag{4.13}$$

The number of bits for the coarse tuning is $N = 4$ and so the minimum values of tuning capacitors are:

$$C_{1_{min}} = \frac{\Delta C_1}{2^N - 1} = 12.3fF \tag{4.14}$$

$$C_{2min} = \frac{\Delta C_2}{2^N - 1} = 8.1fF \tag{4.15}$$

The width of the transistors realizing the switches must be chosen to prevent Q's degradation and, at the same time, to avoid introducing extra parasitics that reduces the tuning range. With a value of $W_{single-ended} = 300nm$ and $W_{diff} = 1.2\mu m$ (for the smallest transistors of tuning banks), scaled then as previously explained, the final oscillator achieves a tuning range of 16%, which typical is a good value for a wide range of applications. Since a tuning range must be centered around the nominal frequency, the last design step is to move again the maximum frequency to

$$f_{max} \simeq f_0 + \frac{TRf_0}{2} = 5.4GHz \tag{4.16}$$

In this way:

$$f_{min} \simeq 4.6GHz \tag{4.17}$$

Finally, the fine tuning must cover the range of the least significant bit. Two varactors, with $L = 600nm$ and $W = 3\mu m$, configured as Figure 4.4, covers the range with a safety overlap when V_{tune} is swept from 0 to V_{DD}. The final schematic is reported in Figure 4.5, with a magnification of tuning elements in Figure 4.6. Finally, the frequency range swept by the varactor only is equal to $61MHz$, well inside the $-3dB$ bandwidth of the tank at $2\omega_0$ which is approximately $2\omega_0/Q_2 \simeq 500MHz$. For this reason, even if varactors don't follow the right proportionality between the added single ended and differential capacitances, the second harmonic resonance is, practically, still present.

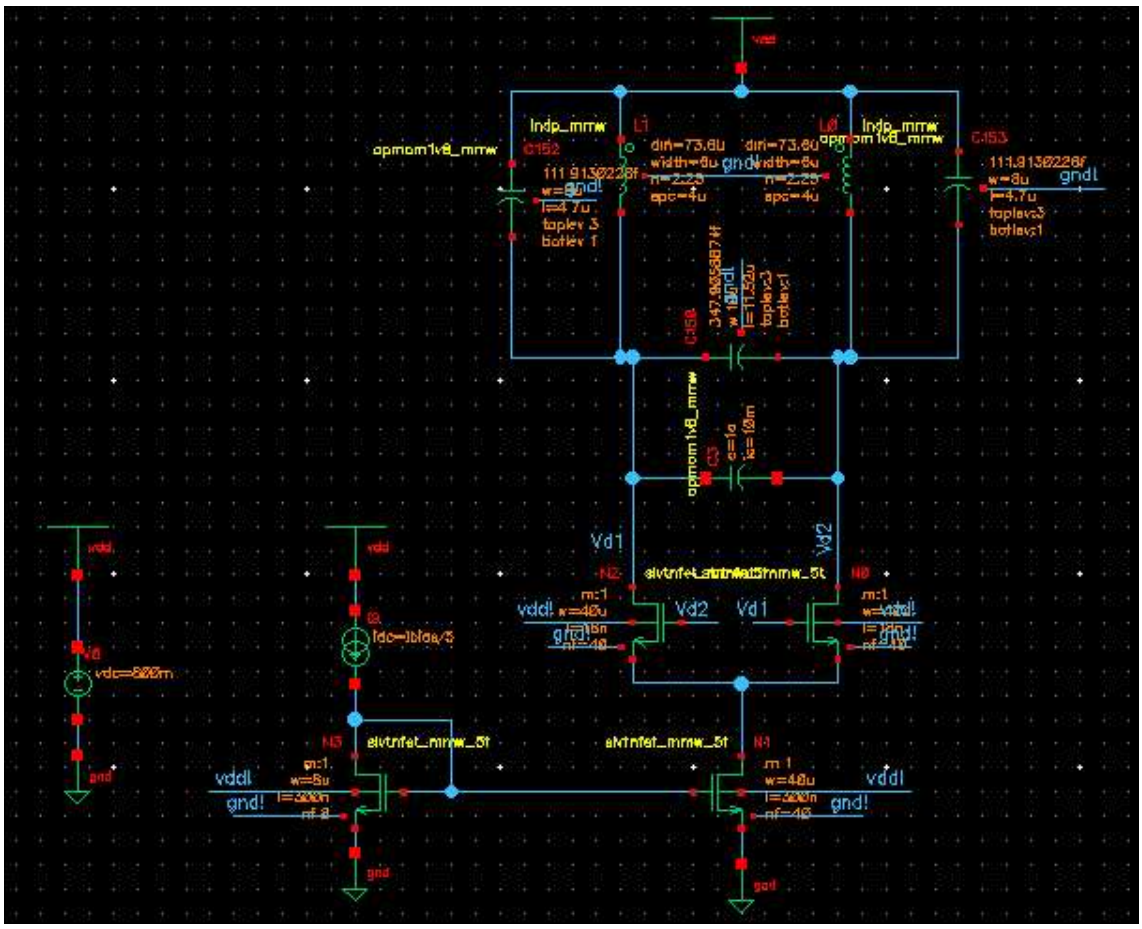

Figure 4.5: *Final schematic of the designed oscillator*

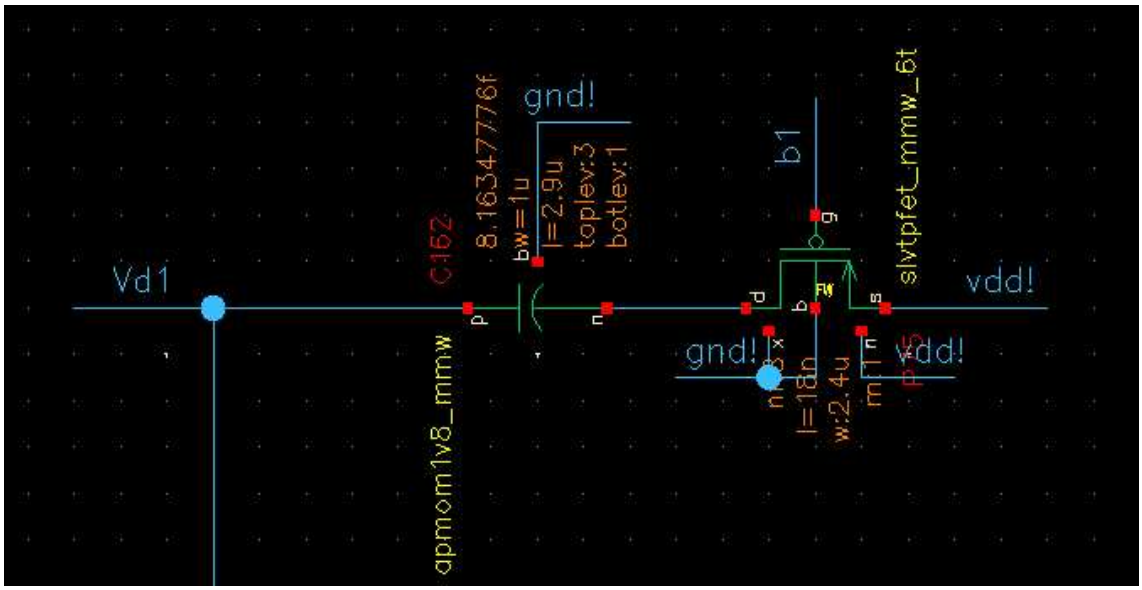

Figure 4.6: *Final schematic of the designed oscillator - Magnification of 1 bit of the single ended tuning bank*

4.2.2 Simulation Results

The first simulation performed is the sweep of the whole tuning range to see if all frequencies are covered and to calculate the actual tuning range. Oscillator sweeps from $f_{max} \simeq 4.6GHz$ to $f_{max} \simeq 5.4GHz$, with a tuning range of 16%, as already said before. Figure 4.7 shows the whole sweep of it.

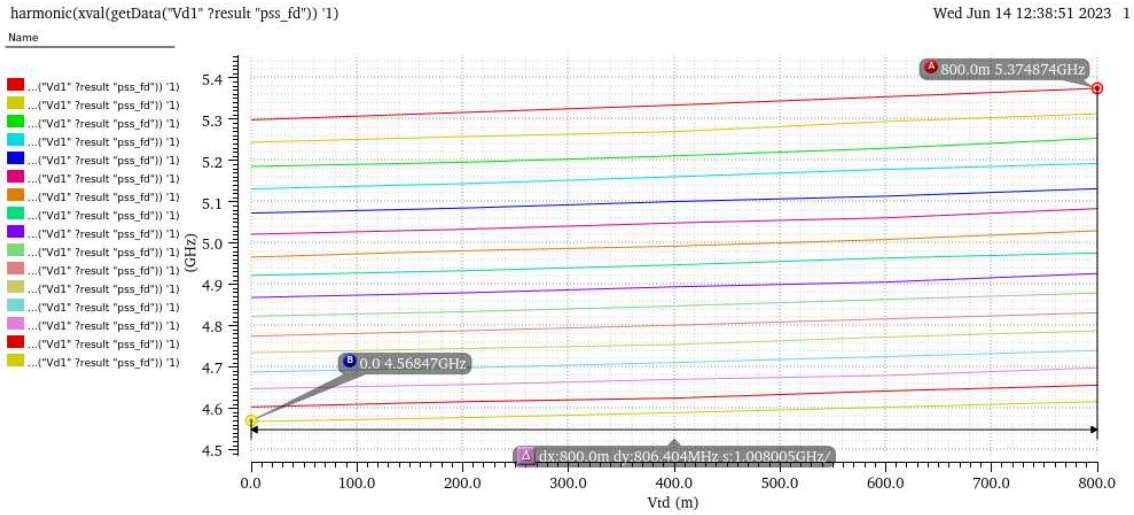

Figure 4.7: *Sweep of the frequency range. Each line is obtained with a different digital combination, while the sweep of V_{tune} exploits the fine tuning.*

At the operating frequency, waveforms are the one reported in Figure 4.8, where the effect of the second harmonic is clearly visible. Analyzing the spectrum of that voltage, the ratio between the first and the second harmonic turns out to be 0.25. Finally, phase noise is plotted in Figure 4.9, and the oscillator achieves $-122.3dBc/Hz$ at an offset of $\Delta\omega = 1MHz$, and $-142.9dBc/Hz$ at $\Delta\omega = 10MHz$ frequency offset, as Figure 4.9 shows. For a good comparison, Leeson equation in (2.40) for the same circuit's parameters, at $\Delta\omega = 10MHz$ gives $-147dBc/Hz$, **if only the tank is considered**. Therefore, the noise factor is $F \simeq 2.6$, about half of a typical noise factor of a class B oscillator. The power consumption of the oscillator is $P \simeq 5mW$[3], achieving a FoM of $-190dBc/Hz$[4]. Table 4.1 compares the specifications with some other recent works, noticing that in this thesis only simulations are provided and usually a real chip is manufactured.

[3]This value is higher than $I_{bias} * V_{DD}$, since the reference branch is considered, too
[4]Value calculated at $\Delta\omega = 10MHz$, well inside the thermal region

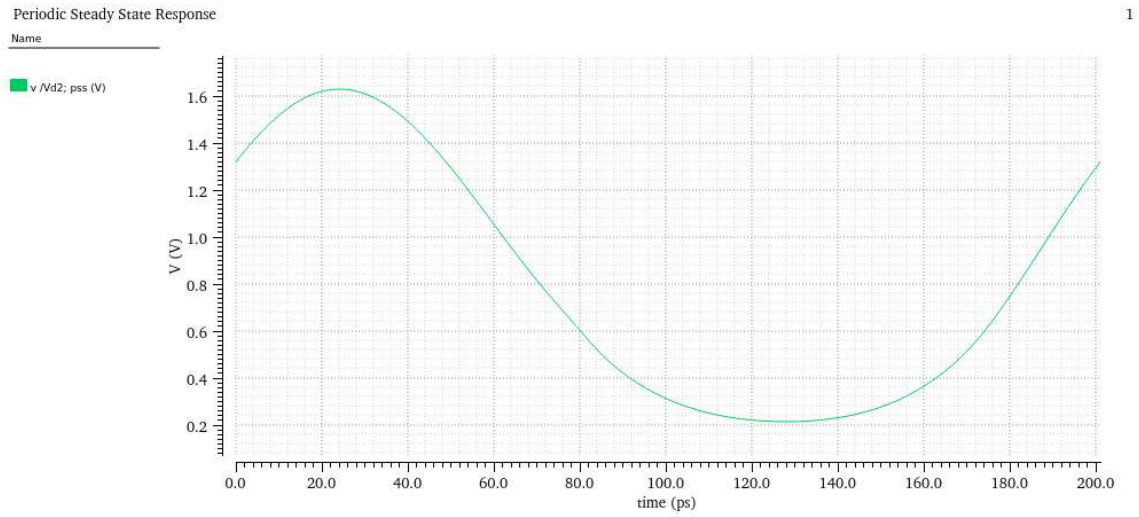

Figure 4.8: *Drain voltage waveform of the designed oscillator*

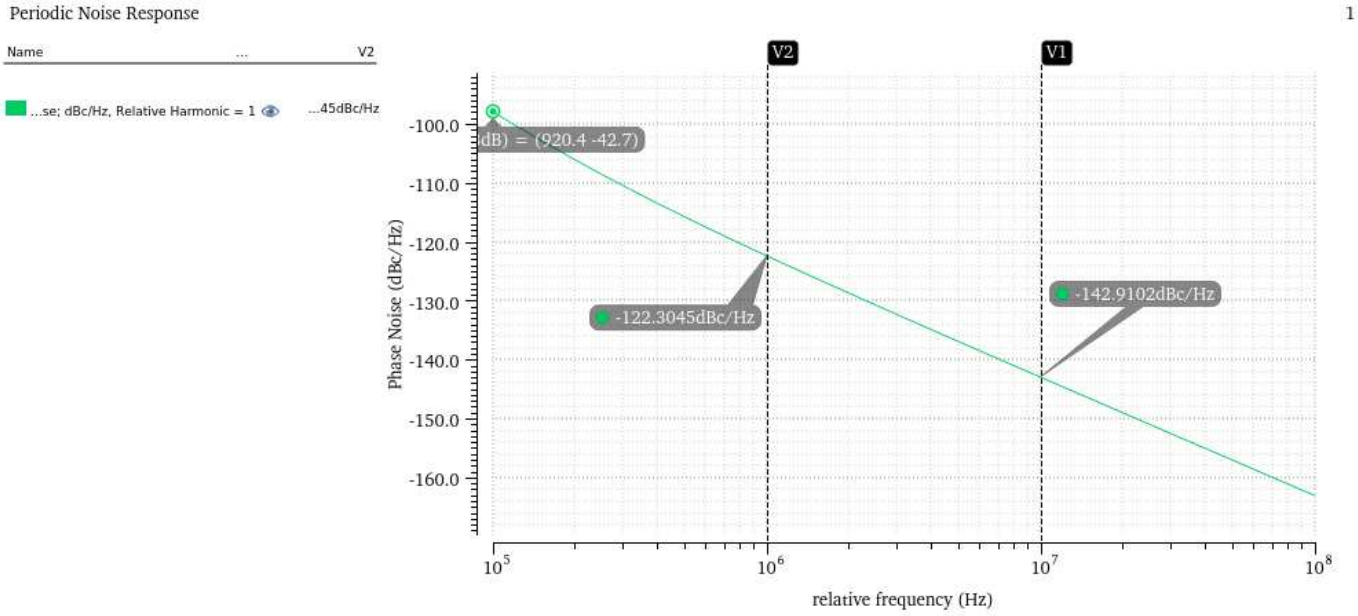

Figure 4.9: *Simulated Phase Noise of the designed oscillator*

	This Thesis	[14]	[17]	[18]	[19]	[15]
Technology	$22\,nm$	$28\,nm$	$40\,nm$	$28\,nm$	28 nm	$28nm$
Frequency $[GHz]$	5	27.3	57.8	19.5	25.2	3.3
Tuning Range	16%	14%	25%	12%	22%	27%
Power $[mW]$	5	12	24	20.7	14.4	6.8
PN norm. w.r.t $\omega_0 = 5GHz$ @ $1MHz$ offset $[dBc/Hz]$	-121.5	-120.7	-121.2	-123.8	-125.6	-124.7
FoM $[dBc/Hz]$	-190	-184	-181	-185	-184	-192
Core Area $[mm^2]$	0.04	0.15	0.13	0.07	0.02	0.19

Table 4.1: *Comparison between other recent works and this thesis*

For a final comparison, common mode capacitors are connected in a diffferential way, creating a standard class-B oscillator, and new phase noise is compared. Tuning again the oscillator to operate at $5GHz$, the phase noise is reported in Figure 4.10, where a difference of around $4dB$ in the thermal region is shown. To deeply analyze the effect of the common mode resonance, noise summaries at an offset of $\Delta\omega = 10MHz$ are compared in Figure 4.11, where the noise of the tail generator is highly reduced, and reduction of the noise coming from the tank by 0.83 is present, consistent with 3.19[5]. This two aspects account for a $2.7dB$ improvement of the phase noise, while other $1.3dB$ difference is explained by the difference in the current efficiency and, as a consequence, in the voltage amplitude. Cadence's noise summary shows the values of noise **without** normalizing it with respect to the carrier (in Figure 3.14, values are in V^2), so this aspect is not visible there.

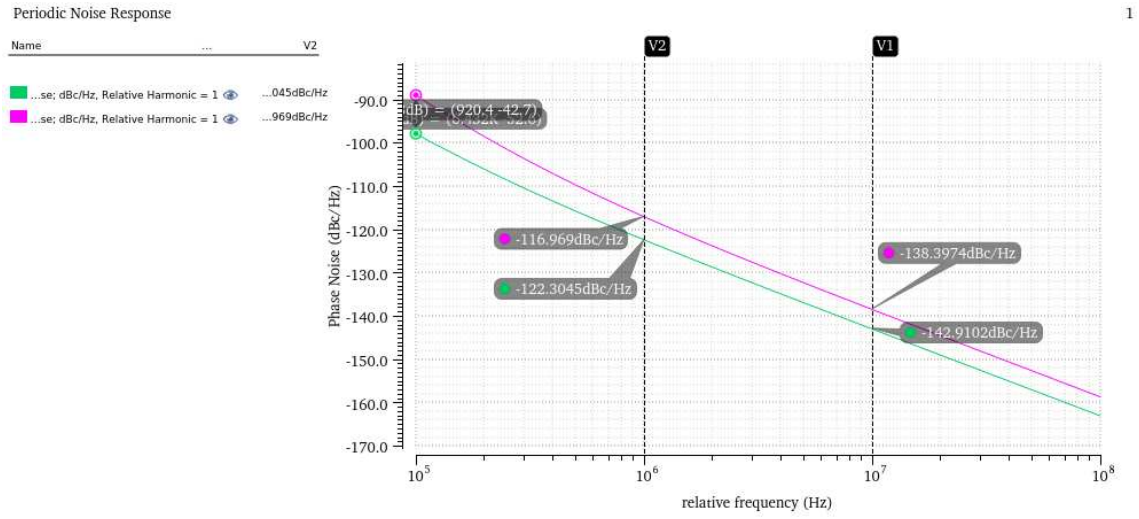

Figure 4.10: *Simulated Phase Noise of the designed oscillator, removing the second harmonic resonance, compared with the previous case*

[5]In this case, $k = 0.3$

Device	Param	Noise Contribution	% Of Total
/N2	therm_Rg	1.23298e-15	16.58
/N0	therm_Rg	1.22765e-15	16.51
/N1	therm_Rg	4.83082e-16	6.50
/N2/slvtnfet_mmw_5t/rgres1	rn	4.37825e-16	5.89
/N0/slvtnfet_mmw_5t/rgres1	rn	4.37046e-16	5.88
/L0/XIND/XIND/rs1_3	rn	3.63807e-16	4.89
/L1/XIND/XIND/rs1_3	rn	3.63435e-16	4.89
/N2/slvtnfet_mmw_5t/rgres	rn	2.40511e-16	3.24
/N0/slvtnfet_mmw_5t/rgres	rn	2.40106e-16	3.23
/L0/XIND/XIND/rs1_1	rn	1.64281e-16	2.21

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 7.43431e-15
No input referred noise available
The above noise summary info is for pnoise_pm data

Device	Param	Noise Contribution	% Of Total
/N1	therm_Rg	3.35138e-15	23.82
/N0	therm_Rg	1.50428e-15	10.69
/N2	therm_Rg	1.5036e-15	10.69
/N1/slvtnfet_mmw_5t/rgres	rn	1.44008e-15	10.24
/N0/slvtnfet_mmw_5t/rgres1	rn	5.84539e-16	4.15
/N2/slvtnfet_mmw_5t/rgres1	rn	5.84337e-16	4.15
/L1/XIND/XIND/rs1_3	rn	4.43876e-16	3.16
/L0/XIND/XIND/rs1_3	rn	4.43675e-16	3.15
/N1	flicker	3.78049e-16	2.69
/N0/slvtnfet_mmw_5t/rgres	rn	3.2184e-16	2.29

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.40687e-14
No input referred noise available
The above noise summary info is for pnoise_pm data

Figure 4.11: *Comparison of noise summaries of the two aformentioned oscillators, where upper part describes the class-F2 oscillator while the lower one refers to the class-B. Reduction of both tank (L_0,L_1) an tail generator ($N1$) noise contribution are visible*

Conclusions

The thesis has deeply analyzed all the effects of the presence of the second harmonic in the usual cross-coupled pair oscillator, which is the a common topology used in integrated solution, even if nowadays a lot of variants have been developed. The effect of that resonance is to improve the phase noise of the oscillator not only in the flicker noise region, as extensively know in literature, but also in the thermal region. This concept is present in literature only partially, and there's no work where all the effects discussed in this thesis are treated properly, especially about the conditions under which the presence of the second harmonic is effectively useful for a phase noise improvement. In fact, all the mechanisms previously illustrated give advantages only under certain conditions, that the designer must verify before counting on the benefit of class-F2 topology, which are not always present. The thesis also shows what is the general condition that a known oscillator topology must have in order to let the usage of the second harmonic resonance to be possible and, unfortunately, some topologies which have noise performances better than the traditional class-B oscillator (such as the class-C) cannot be improved more by using the methods explained in the thesis. Finally, the Example proves that all the mentioned facts are applicable in practise.

Appendix A

Simulation of the noise factor

To find the noise factor of the transistor whose phase noise is simulated in Figure 3.12, the test circuit of Figure A.1 is used, where the size of the transistor is set to be the same of the circuit used to simulate phase noise in Figure 3.12. The current generator provides the same bias current of $1.2mA$ used in the simulated oscillator.

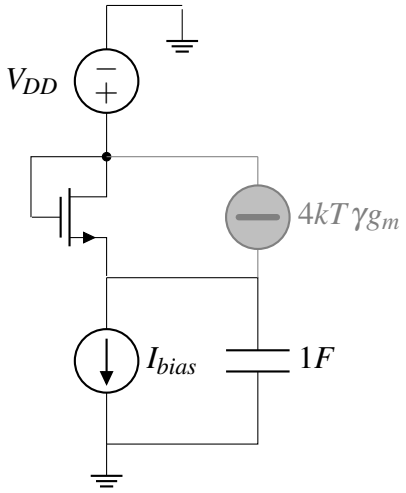

Figure A.1: *Circuit used for the simulation of the noise factor γ, with the equivalent parallel noise current source*

From the noise point of view, the current noise, modelled with a parallel current generator between drain and source, flows into the supply voltage only, since it's an ac ground from a small signal point of view. To create a path for the noise current to/from ground, a really big capacitor, that can be assumed as a short circuit for all nonzero frequencies, is added in parallel to the ideal current source that is an open circuit for the noise. Simulating the value of the noise current's PSD flowing into the supply generator, the noise factor γ is simply found by using:

$$\gamma = \frac{S_{i_n}}{4kT g_m} \tag{A.1}$$

where the value of g_m is taken from the simulation, looking at DC parameters. The simulation must be performed at frequencies above $100GHz$ where the effect of the flicker noise is

negligible[1]. In the particular case of this thesis, (A.1) gives $\gamma \simeq 1.4$.

[1]To check if the flicker noise is negligible, it's possible to print the *noise summary*

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