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"A 10GHz integrated LC-DCO underneath a single-turn inductor in 28-nm CMOS"

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Contents

Abstract

A possible design choice, to satisfy the need of low power RF LC-based oscillators in PLL for IoT applications, is to dimension the inductor without size limitations obtaining big coil with high quaity factor. To overcome the problem of large area consumption, the tank capacitance and the other components of the entire PLL, including digital blocks, could be implemented as structures underneath the inductor. Such a decision introduces problems linked to cross talking which degrades the oscillator performances. So, the use of pattern metallic shields, to electrically isolate the coil from the beneath circuitry, is analyzed showing that the best choice to avoid cross-talking is to use a patterned ground shield (PGS). In this thesis is presented a 10GHz LC-based Class-B DCO in 28-nm CMOS underneath a single-turn shielded inductor, with $FOM = -192.9dBc/Hz$ and $FOM_T = -199.1dBc/Hz$. Its simulated phase noise at $27°C$ is equal to -112.5dBc/Hz, at the offset frequency of 1MHz, with a power consumption $P_{dc} = 0.9mW$.

Abstract in italiano

Una possibile scelta progettuale, per soddisfare l'esigenza di oscillatori RF LC-based a bassa potenza in PLL per applicazioni IoT, è quella di dimensionare l'induttore senza limiti di spazio occupato, ottenendo spirali di grandi dimensioni con un elevato fattore di qualità. Per ovviare al problema del grande consumo areale, la capacità del tank e gli altri componenti dell'intero PLL, compresi blocchi digitali, potrebbero essere implementati come strutture al di sotto dell'induttore. Questa scelta introduce problemi legati al cross talking che degradano le prestazioni dell'oscillatore. È stato quindi analizzato l'uso di schermature metalliche discontinue, per isolare elettricamente le spire dell'induttore dalla circuiteria sottostante, dimostrando che la scelta migliore per evitare il cross-talking è quella di utilizzare una schermatura discontinua connessa a massa (PGS). In questa tesi viene presentato un DCO LC-based in Classe B a 10GHz, in tecnologia CMOS a 28-nm sotto un induttore schermato, formato da un unica spira, con una $FOM = -192.9 dBc/Hz$ e una $FOM_T = -199.1 dBc/Hz$. Il rumore di fase simulato alla temperatura di $27°C$ è pari a -112.5dBc/Hz, alla frequenza di offset di 1MHz, con un consumo di potenza $P_{dc} = 0.9 mW$.

1 INTRODUCTION

The demand for more competitive price, low dimensions and low power devices are moving the oscillator design to fully on-chip solutions. Power consumption is reduced since less discrete component are driven and so external connection losses are in this way avoided. On the other hand fully on-chip passive structures, like inductors, soffer of low quality factor: the VCO output phase noise could be strongly degraded [1]. Using simple solutions without inductors, like in a ring oscillator, could solve the problem of area consumption paying in terms of poor phase noise performances [2], [3]. LC-VCOs/DCOs present lower phase noise at lower power consumption: a deeper study on them is important to achieve the needed results. The main problem of this oscillator topology is its area occupation: passives, and in particular inductors, size doesn't reduce proportionally with active components process geometry scaling. That's why, even using very scaled technologies, the majority of the circuit area is occupied by the inductor structure. To find a good trade-off between occupied space, low noise and low power consumption, a studied solution is to implement the inductor as a big one and build the VCO/DCO, or even the whole PLL circuitry, below the inductor.

But new problems are introduced in this way, like parasitic coupling and cross-talk effects between the inductor and the underneath structures: conductive shields and careful layout to avoid ground loops are studied in this thesis. Without a proper isolation, a big area occupying inductor could be source and receptor of noise coupling decreasing its quality factor and so the overall performance of the DCO.

In order to minimize the total area occupation, the DCO digital loop, that controls the switched capacitor bank switching activities, could be implemented underneath the inductor: digital currents have a completely different frequency spectrum in respect with the one of the current flowing through the inductor and so they can cause a non negligible phase noise degradation.
Different shield topologies are studied in order to quantify the variations introduced by them, in terms of inductor's quality factor, DCO's output phase noise and magnetic/electrical coupling between the inductor and its underneath structures.

Since the main use of this DCO will be in IoT and automotive, the chosen output frequency is 10GHz. At this frequency the inductor's quality factor reaches its maximum for N28 technology, if the inductor's self resonance frequency is sufficently high [4], reducing the oscillator's power consumption, making possible to use this circuit for USB purpose and, adding frequency dividers and multipliers, for Wi-Fi, BLE and radar applications.

2 Theory

2.1 LC cross-coupled oscillators

Cross-coupled pair (CCP) based topologies are studied to implement this circuit. They are the dominant choices in RF applications due to their low achievable output phase noise and limited power consumption. On the other hand, the presence of one or more inductors makes their dimensions big in respect with the ones of different topologies, based on the feedback theory without L or C components. However, the trend is to use LC-VCO to implement high performace PLLs based frequency synthesizers.

Initially the needed inductance and the tank quality factor at 10GHz are found looking at the well known theory around cross-coupled oscillators [5]. Equations are rewritten as a function of the tank's capacitance and inductance ratio. In this way, considering the phase noise and current specifications, needed circuit's quantities are found. Inductor's area occupation is initially not considered, since it should cover a big space, in which underneath circuit's structures are built [6].

The circuit modeling starts considering the bias current as the one provided by a generic current mirror: it corresponds to the reference current I_{ref} multiplied by the mirror factor M:

$$I_{bias} = MI_{ref} \tag{1}$$

2.1.1 Phase noise Leeson's equation and tank quality factor

Starting from the phase noise specification at the offset Δf Hz, the Leeson's equation is used to predict the phase noise beahavior in the $\frac{1}{f^2}$ region, in sake of semplicity:

$$\mathscr{L}(\Delta f) = 10log_{10}\left\{ R^3 \left(\frac{C}{L}\right)^2 \frac{k_B \pi^2 T F}{8 I_{bias}^2} \left(\frac{f_0}{\Delta f}\right)^2 \right\} \tag{2}$$

In addition to the temperature T in K, the Boltzmann constant k_B, the noise excess factor F, which is used to take into account the white noise contribution of the cross-coupled pair and depends mostly on the oscillator topology [4], it's possible to recognize the tank single ended equivalent series resistance R. It is used to model the losses linked to capacitor's and inductor's parasitic resistances. They are responsible of the non-infinite overall tank quality factor Q, which is defined as:

$$Q = \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)^{-1} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{3}$$

where:

$$Q_L = \frac{L_S \omega_0}{R_{S_L}} \qquad Q_C = \frac{1}{R_{S_C} \omega_0 C_S} \tag{4}$$

In first approximation, the losses are considered dominated by the inductor ones and so $R_{S_L} = R$ and $R_{S_C} = 0$.

This quantity is the main limit to power consumption: lower it is, higher is the current needed to achieve the specification output phase noise value and so the needed output oscillation voltage amplitude. It's possible to obtain an estimation of the zero-peak oscillation amplitude analzying the circuit with the mixers' theory.

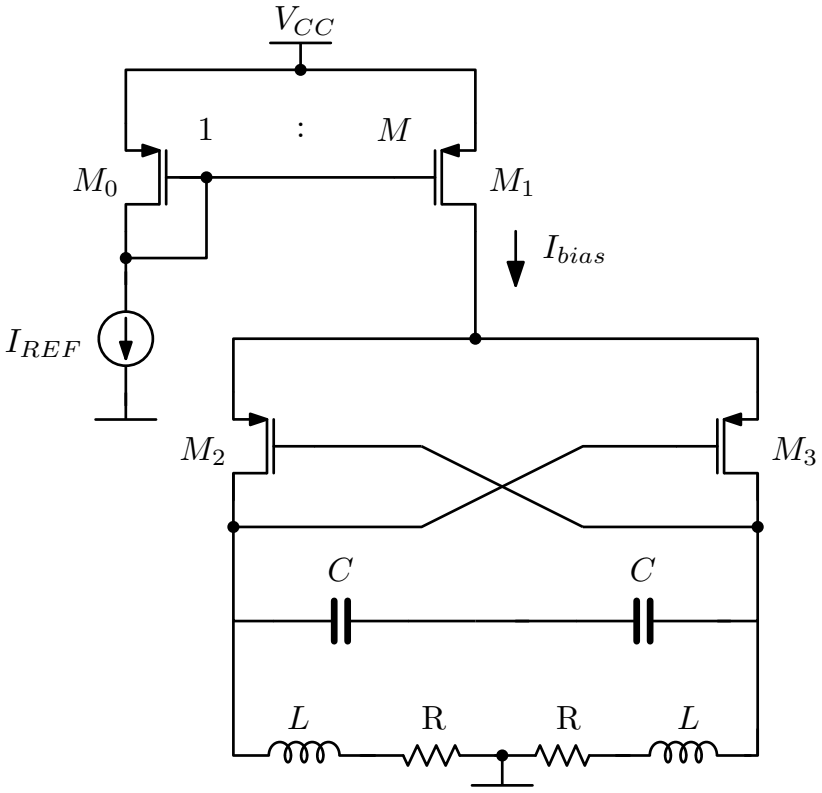

Figure 1: ideal pMOS cross-coupled pair oscillator schematic with a current mirror as a bias circuit

2.1.2 Oscillation amplitude

Starting from the series to parallel transformations and considering the tank capacitor's and inductor's quality factors very bigger than one, the following approximations could be done:

$$L_P = L(1 + Q_L^{-2}) \approx L \qquad C_P = \frac{C}{1 + Q_C^{-2}} \approx C \qquad R_P \approx RQ^2 \quad (5)$$

Now, is possible to analyze the circuit in Fig.2, in which the CCP pair pMOSFETs are considered working in hard switching mode.

Each transistor conducts the current I_{bias} for half period of the output signal $v_{LO}(t)$ that could be written as:

$$v_{LO}(t) = I_{bias} \sum_{k=-\infty}^{\infty} Z_L(jk\omega_0) M_k e^{jk\omega_0 t} \quad (6)$$

where ω_0 is the angular frequency of the fundamental harmonic of

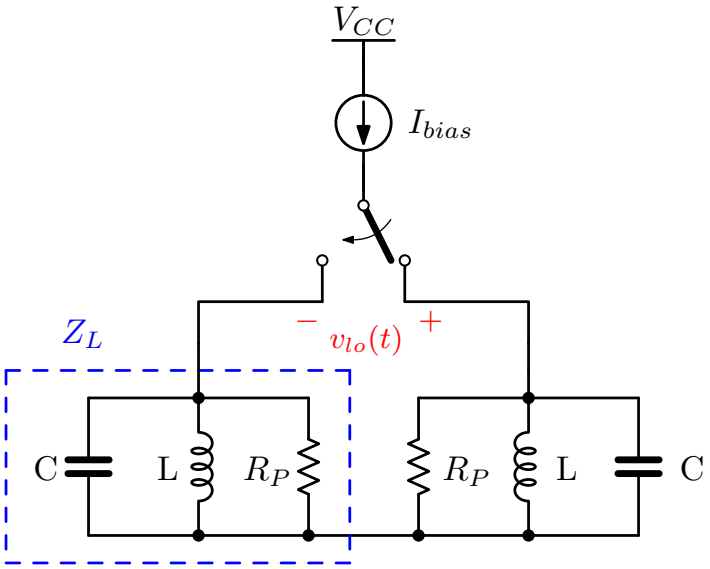

Figure 2: oscillator model considering the cross-coupled pair MOSFETs operating in hard switching

the current square wave $i_y(t) = \sum_{k=-\infty}^{\infty} M_k e^{jk\omega_0 t}$ flowing through the transistors and throught the tanks, each one with an impedance equal to $Z_L(jk\omega_0)$.

Assuming a high tank quality factor, which makes very selective the LC network, it's possible to semplify calculations. Considering:

$Z_L(\pm j\omega_0) = R_P$ and $Z_L(\pm kj\omega_0) \approx 0$ for $k \neq \pm 1$

the following result is obtained:

$$v_{LO}(t) = I_{bias}\frac{2}{\pi}R_P\left(e^{j\omega_0 t} + e^{-j\omega_0 t}\right) = \frac{4}{\pi}R_P I_{bias} cos(\omega_0 t) \tag{7}$$

and so the differential oscillation amplitude (zero-peak voltage) $V_{LO,0p}$ is:

$$V_{LO,0p} = \frac{4}{\pi}R_P I_{bias} \approx \frac{4}{\pi}I_{bias}\frac{1}{R}\frac{L}{C} \tag{8}$$

2.1.3 MOS' transconductance and start up condition

The parasitic tank resistance R causes a power loss and so the attenuation of output sine amplitude: after some time oscillations are estin-

guished. In other words, the Barkhausen conditions are no more met and the circuit becomes stable killing the oscillations. In order to balance this parasitic resistance effect, the CCP has to be carefully designed. Its MOSFETs transconductances g_{m1} and g_{m2} are considered both equal to g_m in next calculations.

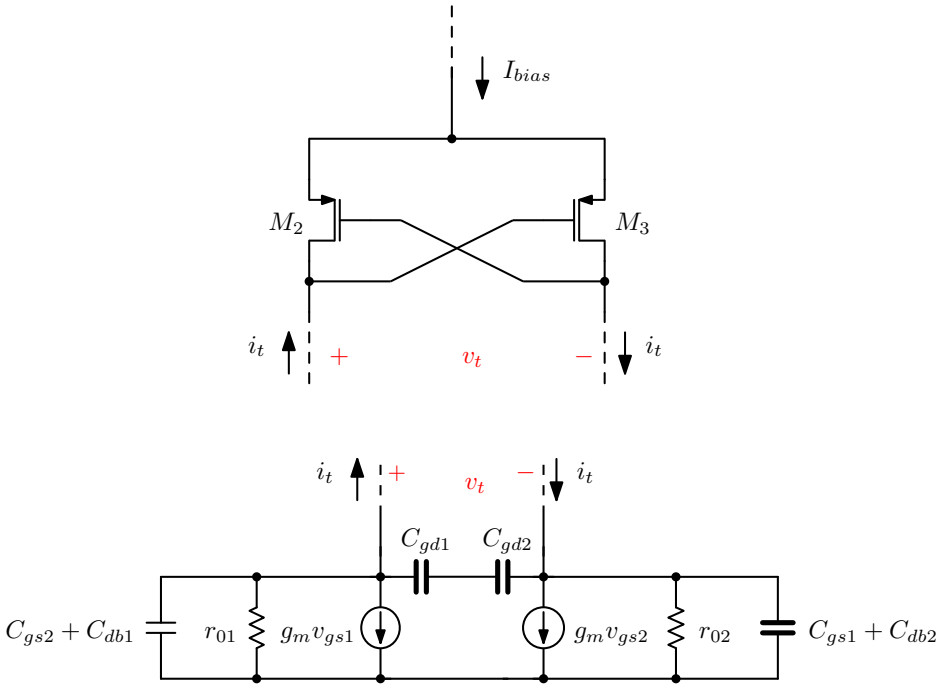

Figure 3: ideal ccp schematic (top) and ccp small signal model (bottom)

Looking at the CCP small signal model in Fig. 3, and considering two identical MOSFETS, the lossy tank sees in parallel with itself:

- a negative transconductance equal to $G_a = -\frac{g_m}{2}$, since $v_{gs1} = -v_{gs2} = -\frac{v_t}{2}$, $i_t = -\frac{g_m}{2} v_t$;
- the two CCP's MOSFET output conductances $\frac{1}{r_{01}} // \frac{1}{r_{02}} = \frac{1}{2r_0}$;
- a parasitic capacitance $C_{par} = \frac{C_{gs}}{2} + 2C_{gd} + \frac{C_{db}}{2}$

Considering the total tank losses equal to $G_T = \frac{1}{2r_0} + \frac{1}{2R_P}$, oscillation

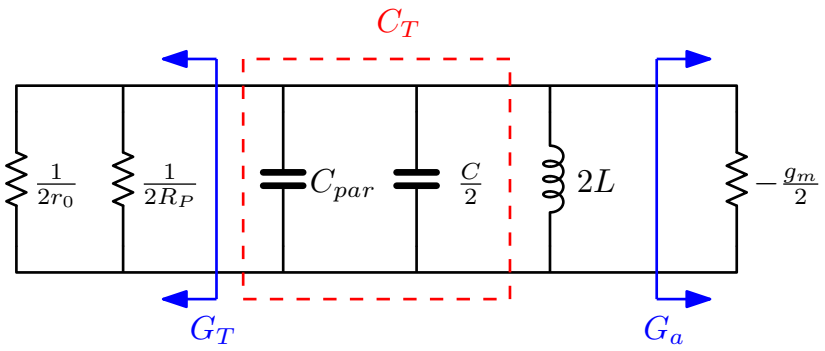

Figure 4: ideal oscillator schematic with the ccp modeled as a negative transconductance in parallel to the tank

can start and substain only if they are equal to zero:

$$|G_a| = G_T \tag{9}$$

Barkhausen conditions are met, the circuit resonates.

The new total tank capacitance across the oscillator output C_T is no more equal to $\frac{C}{2}$. In particular, considering the two MOSFETs identical, a new contributor C_{par} is added:

$$C_T = \frac{C}{2} + C_{par} \tag{10}$$

Since r_0 is usually very bigger in respect to R_P, in next calculation its effect is neglected:

$$R_T = \frac{1}{G_T} = 2r_0//2R_P \approx 2R_P \tag{11}$$

So it's true that the equation (9), ideally, ensures the oscillation substain, but it doesn't ensure its start and substain considering the presence of parasitics. A more relaxed condition should be chosen, which lets the oscillation begin:

$$|G_a| > G_T \rightarrow g_m > \frac{1}{R_T} \tag{12}$$

This is called the start up condition.

Initially the current is low, the total resistance seen by the tank is negative: the circuit is unstable. The rise of the oscillations increases the MOSFETs' transconductance making the total tank resistance positive: the circuit is stable. This process repeats periodically letting the circuit respect in mean the Barkhausen conditions.

In order to make more useful the disequation (12), it could be rewritten in the following way:

$$g_m = \alpha_{min} R \frac{C}{L} \tag{13}$$

where $\alpha_{min} > 1$ is called the transconductance safety factor.

A trade of is needed in order to find the optimal α_{min} since, if on one hand, lower g_m means higher oscillation amplitude and so lower phase noise, on the other hand, a bigger output swing results in larger mirror dimension since a lower mirror V^* is needed.

2.1.4 CCP MOSFETs design

As said, a constraint to CCP MOS' dimension is given by the transconductance value needed to respect the start up condition.

Considering the transistors working in saturation region [7], their width W is obtained starting from g_m transconductance espression:

$$g_m = k_p \frac{W}{L_{ch} V_{ov}} \quad \longrightarrow \quad W = \frac{g_m L_{ch}}{k_p V_{ov}} \tag{14}$$

Where the channel length L_{ch} is a fixed technological parameter equal to 28nm and V_{ov} the transistors' overdrive voltage. In modern transistor CMOS processes, the trend is to choose overdrive voltages in the order of $0.3 \div 0.5V$. Its value is critical since, if on the one hand a big V_{ov} degrades g_m due to mobility degradation and saturation velocity effects for channel carriers, on the other hand a low V_{ov} requires large MOSFETs' dimensions.

2.1.5 Oscillation angular frequency

The oscillation angular frequency is:

$$\omega_0 = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{LC}} \sqrt{\frac{1 + {Q_C}^{-2}}{1 + {Q_L}^{-2}}} \tag{15}$$

Considering an inductor and capacitor quality factors very bigger than 1, and so using the approximations shown in (5), the oscillation angular frequency could be approximated to:

$$\omega_0 \approx \frac{1}{\sqrt{LC}} \tag{16}$$

2.1.6 Oscillator topology choice

The design equations reported until now reffer to a single nMOS/pMOS cross-coupled pair LC oscillator. Since the phase noise specification is one of the most challenging to be satisfied, all topologies, in class-B operation, are taken into account.

The nMOS one shows the worst performances in terms of phase noise: the center tap of the differential tank inductor is directly connected to the power supply letting the low frequency noise enter directly into the circuit.

Even if pMOS are bigger structures in respect with nMOS – at equal channel resistance, transconductance and channel length – they present less output noise making them optimal for controlled oscillator circuits. This feature of pMOS is given by their structure. nMOSFETs present a surface channel, pMOSFETs a buried one: channel carriers in the former are closer to the silicon/silicon oxide interface presenting a higher probability of trapping and detrapping by oxide traps, which are considered responsibles of the most of the $\frac{1}{f}$ noise [8]. It means that the phase noise performance is strongly increased if all n-type transistors are substituted by pMOSFETs, including the ones in the biasing circuit.

Another solution, that lets achieve a higher efficiency and lower phase noise values, at the same power consumption, is the cMOS topology. Two cross-coupled pairs are used: one composed by nMOSFETs, one by pMOSFETs. Intuitevely, adding two transistors should mean introducing two new noise sources. This thought is wrong.
Considering the gains of pMOS $g_{m,p}$ and nMOS $g_{m,n}$ equal, the overall cMOS oscillator transconductance $g_m = g_{m,p} + g_{m,n}$ results doubled in respect to a single CCP oscillator topology and it causes two effects:

- the cross-coupled pairs commutation time is halved, dividing by two the noise injected by the RF transistors;
- the output oscillation amplitude $V_{LO,0p}$ is doubled.

The main consequence is a 6dBc/Hz reduction in the output phase noise [5]. This theoretical result has been confirmed by a simulation of a simple oscillator schematic, using ideal passive components to implement the LC tank with losses (Fig.5).

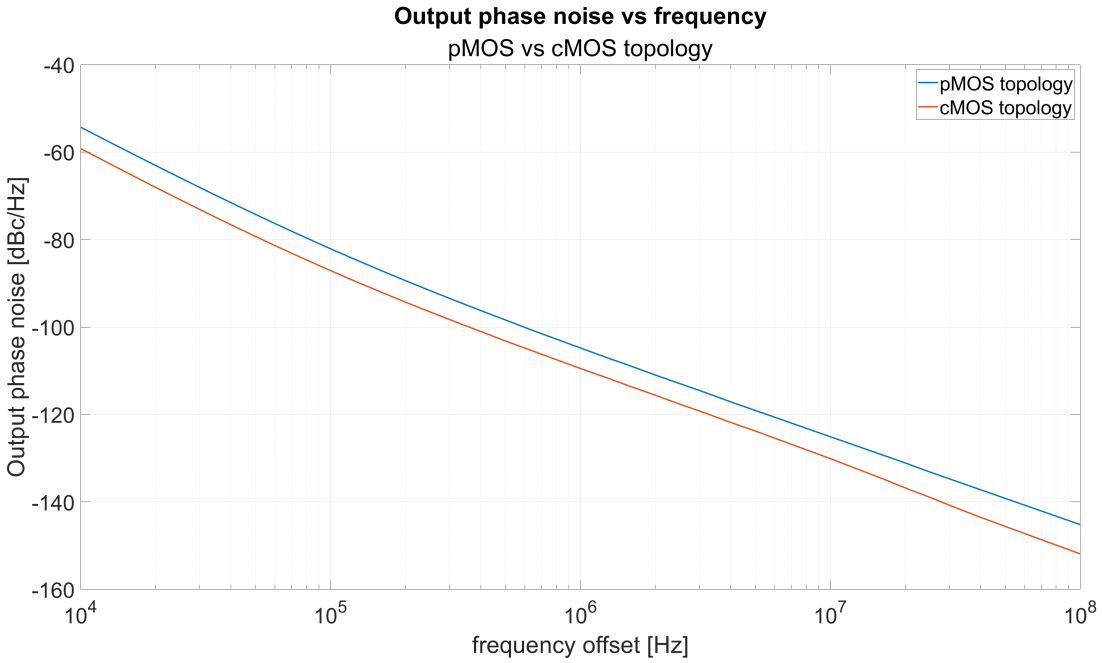

Figure 5: Phase noise comparison: pMOS based oscillator (blue) and cMOS based oscillator (red)

2.1.7 Figures of merit

$$FOM = \mathscr{L}(\Delta f) - 20log\left(\frac{f_0}{\Delta f}\right) + 10log\left(\frac{P_{dc}}{1mW}\right) \tag{17}$$

$$FOM_T = FOM - 20log\left(\frac{TR\%}{10}\right) \tag{18}$$

where $P_{dc} = V_{dd} * I_{bias}$

where TR% is equal to the sum of the fine and coarse tuning ranges in percentage.

2.2 Capacitor bank theory

Looking at equation (16), the output oscillation frequency adjustment is possible changing tank capacitance, tank inductance or both of these quantities. Since it is simpler and it lets to achieve a more linear behavior, the capacitance is the most common varied quantity to tune an oscillator.

In a DCO, the capacitance variation is discrete and controlled by a digital signal: that's why switched-capacitor cells are studied in this thesis. Implement one or more banks of switched-capacitor cells lets achieve a wider tuning range (necessary in IoT applications) and less control voltage noise sensibility in respect of continuous tuning techniques based on varactors use.

2.2.1 Switched-capacitor cell

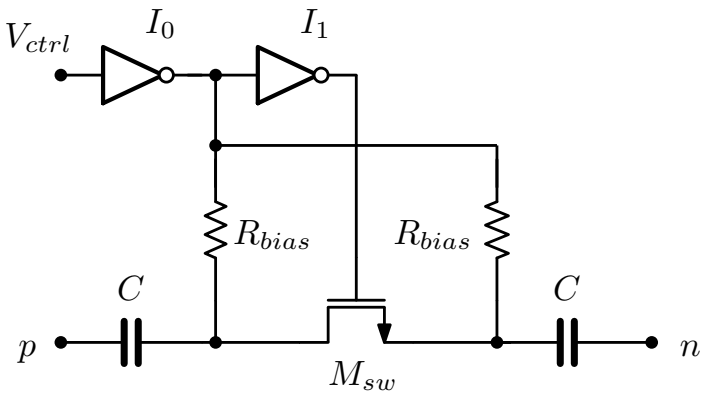

Figure 6: switched-capacitor cell with bias circuit

The voltage V_{ctrl} turns ON and OFF the MOSFET M_{sw}, used as a switch, that controls the current flow through the cell.

The two bias resistors R_{bias} are used to fix the DC voltage in between the series of the two explicit caps C.

In Fig. 7 is shown the small signal model of a switched cap cell. The

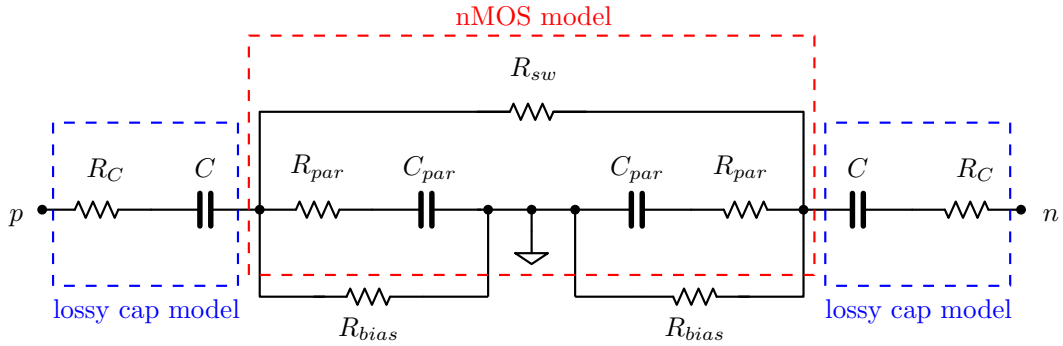

Figure 7: switched capacitor cell small signal model

capacitor's losses are model with series resistances R, for the two explicit capacitances C, and with the series resitances R_{par} for the nMOS' parasitic capacitances $C_{par} = C_{gd} + C_{db} = C_{gs} + C_{sb}$.

The role of the digital signal V_{ctrl} is to change the resistance R_{sw}, turning ON or OFF the nMOS M_{sw}, varying the total capacitance seen at the nodes p and n.

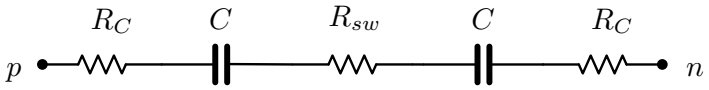

Figure 8: simplified switched capacitor cell small signal model: ON state

When the gate voltage is equal to $V_{ctrl} = V_{dd}$, the cell is ON.
Since the nMOS equivalent resistance R_{sw} is very small, it's possible to assume that a negliglible current flows through the parasitic capacitances C_{par}. So, the ON state cell schematic could be approximated as shown in Fig. 8.
Considering also that the parasitic reistances R_C of the exlicit caps are smaller than the nMOS one, an estimate of the cell's resistance R_{on} and capacitance C_{on} is found as follow:

$$R_{on} = 2R_C + R_{sw} \approx R_{sw} \qquad C_{on} \approx \frac{C}{2} \tag{19}$$

In effort with (4), the on state cell's quality factor is:

$$Q_{on} \approx \frac{1}{\omega_0 R_{sw} \frac{C}{2}} \tag{20}$$

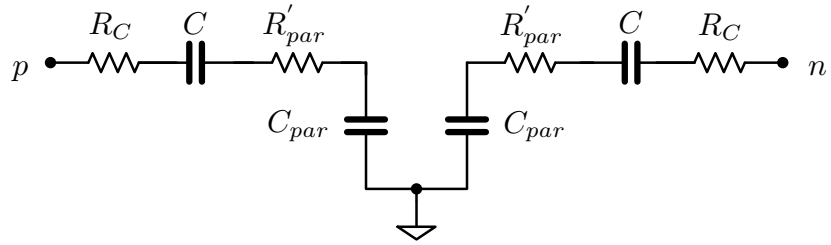

Figure 9: simplified switched capacitor cell small signal model: OFF state

When the gate voltage is equal to $V_{ctrl} = 0V$, the cell is OFF. The nMOS isn't conducting: its equivalent resistance R_{sw} is very big and all the current flows through parasitic capacitances C_{par}. Since they are small, the presence of the two bias reisistors R_{bias} must be considered in the OFF state cell quality factor Q_{off} calculation. As shown in Fig. 9, a new equivalent resistance R'_{par} is considered in series with parasitic caps:

$$R'_{par} \approx R_{par} \left(1 + \frac{R_{par}}{R_{bias}} Q^2_{C,par}\right) \tag{21}$$

Where $Q_{C,par}$ is the quality factor of the parasitic capacitances calculated using (4).

That being said, is finally possible to obtain an estimate of the OFF state cell's resistance R_{off} and capacitance:

$$R_{off} = 2R_C + 2R'_{par} \qquad C_{off} \approx \frac{1}{2} \frac{CC_{par}}{C + C_{par}} \tag{22}$$

and the OFF state quality factor Q_{off}:

$$Q_{off} \approx \frac{1}{\omega_0 \left(R_C + R'_{par}\right) \frac{CC_{par}}{C+C_{par}}} \tag{23}$$

2.2.2 Capacitor bank and tuning range equations

The final capacitor bank is composed by N single cells: N_{on} cells in ON state and N_{off} in OFF state. An estimate of the overall bank quality factor Q_{CB}, at the oscillation frequency f_0, has been done considering the following equations, deeply explained in [9]:

$$Q_{CB} = Q_{off} \frac{N + N_{on}(\beta - 1)}{N + N_{on}(\beta\gamma - 1)} \tag{24}$$

where $\beta = \frac{C_{on}}{C_{off}}$ and $\gamma = \frac{Q_{off}}{Q_{on}}$.

Even if achieving a very high bank quality factor Q_{CB} is the best choice in power consumption minimization, a trade-off between it and the needed DCO tuning range TR specification value must be found.

A possible way to increase Q_{on} could be to enlarge the nMOS size: if on one hand R_{sw} goes down increasing the ON state cell quality factor, on the other hand, parasitic capacitances C_{par} increase enlarging the minimum bank capacitance C_{min}, affecting the tuning range value. Another possible way to increase the ON state cell quality factor could be use smaller explicit capacitances C: in effort with (4), smaller caps have bigger quality factors. Again this choice has to be done carefully since the nMOS fixed parasitic capacitance becomes comparable with C, letting $C_{on} \approx C_{off}$. The final result is a degradation of the achievable tuning range value.

A possible way to increase Q_{off} could be to increase the bias resistance R_{bias}: in effort with (21), it's clear that higher this resistance is, lower the series OFF state cell losses are. But it is not always possible to

choose very high bias resistance values, since they are responsible of the charge and discharge of parasitic nMOS' capacitances. Too large bias resistances introduce non negligible time constants that can limit the switching time of the single cells: if the oscillator is used in dynamic tuning application (e.g. radio applications, where frequency modulation is needed) particular care must be taken in R_{bias} design.

The oscillator's tuning range TR is defined as:

$$TR = \frac{\omega_{0,max} - \omega_{0,min}}{\frac{\omega_{0,max}+\omega_{0,min}}{2}} = \frac{\Delta\omega}{\omega_0} \tag{25}$$

where $\omega_{0,max}$ is the maximum output angular frequency, achievable with all the capacitor bank cells in OFF state and so with a tank capacitance equal to the minimum value C_{min}. In a complementary way, $\omega_{0,min}$ is the minimum output angular frequency, achievable with all the capacitor bank cells in ON state and so with a tank capacitance equal to the maximum value C_{max}.

Taking into account these last considerations it's possible to rewrite equation (25) in the following manner:

$$\omega_{0,max} = \frac{1}{\sqrt{LC_{min}}};\quad \omega_{0,min} = \frac{1}{\sqrt{LC_{max}}} \quad \rightarrow \quad TR = 2\frac{\sqrt{\frac{C_{max}}{C_{min}}} - 1}{\sqrt{\frac{C_{max}}{C_{min}}} + 1} \tag{26}$$

And so, the equation used to start the capacitor banks design is:

$$\frac{C_{max}}{C_{min}} = \left(\frac{1 + \frac{TR}{2}}{1 - \frac{TR}{2}}\right)^2 \tag{27}$$

This equation holds also in single cell design since it's linked to the

ratio between the maximum and minimum capacitance which is independent on the bank cells number:

$$C_{min} = NC_{off} \qquad C_{max} = NC_{on} \tag{28}$$

Another useful equation, which links the angular frequency variation $\Delta\omega = \omega_{0,max} - \omega_{0,min}$ around $\omega_0 = \frac{1}{\sqrt{LC}}$ to the capacitance variation $\Delta C = C_{max} - C_{min}$ around C is the following:

$$\Delta C = \frac{1}{{\omega_{0,min}}^2 L} - \frac{1}{{\omega_{0,max}}^2 L} = 32C\frac{{\omega_0}^3\Delta\omega}{\left(4{\omega_0}^2 - \Delta\omega^2\right)^2} \tag{29}$$

Since, usually, $\Delta\omega << \omega_0$ and so $\Delta C << C$, is possible to simplify the previous equation as follow [10]:

$$\Delta C \approx 2C\frac{\Delta\omega}{\omega_0} \tag{30}$$

2.3 Inductor design equations

The needed inductance could be obtained starting from the phase noise constraint, using the Leeson's equation (2).

2.3.1 Integrated inductor model

In order to understand the real behavior of an integrated inductor of inductance L, parasitic effects must be taken into account.

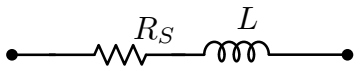

Figure 10: RF inductor lumped model

Until now, the inductor has been modeled as shown in Fig. 10: the metal inductor's routings ohmic losses are modeled with the series resistance R_S. In a real integrated inductor used in RF application, R_S is a frequency dependent parameter. At high frequencies, due to the so called "skin effect", the current which flows in the inductor is no more uniformely distributed through the inductor's routing and it causes an increase of the series resistance with the frequency.
Big inductors also suffer by other high frequency unwanted effects like capacitive and magnetic coupling with the substrate.

To represent frequency dependent losses in a real integrated inductor, it's possible to use the semplified lumped elements schematic reported in Fig. 11. The inductor series resistance R_S is considered constant, capacitive coupling and substrate losses effects are modeled respectevely through: the oxide capacitance between the inductor and the substrate C_{ox}, the silicon substrate capacitance C_{Si} and resistance R_{Si}. The capacitance C_S is used to model parasitics linked to inductor's routings

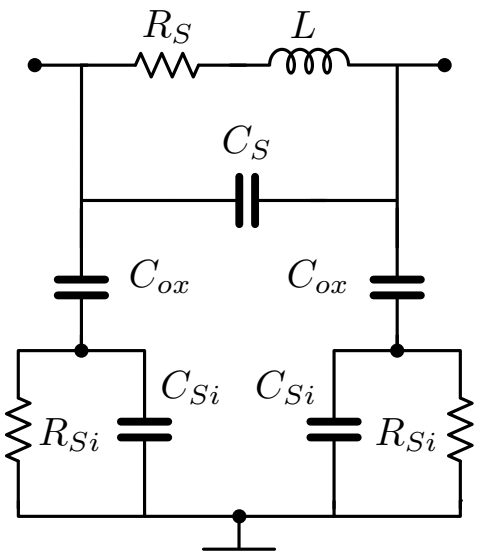

Figure 11: RF lumped model of an integrated spiral inductor

fringe capacitance and routings overlap capacitance.

In the schematic shown in Fig. 11, magnetic coupling effects are neglected.

A more accurate model could be obtained considering the inductor series resistance R_S as a frequency dependent quantity [11]:

$$R_S(f) = R_{DC} + R_{RF}\frac{(f/f_O)^2}{1+(f/f_O)^2} \tag{31}$$

where R_{DC} models the metal ohmic losses and R_{RF} the magnetically and electrically induced losses. The parameter f_O is a factor which controls the transition between the low and high frequencies and it is proportional to the square metal resistance R_{sq} and inversely proportional to the product between the skin depth δ and the magnetic permeability μ.

In sake of simplicity, magnetic coupling effects with the substrate are neglected and the inductor's series resistance R_S is considered equal to R_{DC}.

2.3.2 Inductor's self-resonance angular frequency

In addition to taking into account non ohmic losses parasitic effects, particular care must be taken also to the self-resonance angular frequency ω_{sr}. In the more realistic inductor model shown in Fig. 11, the presence of parasitic capacitances in parallel with the ideal inductance L creates a LC tank which resonates at:

$$\omega_{sr} = \frac{1}{\sqrt{L\left(C_S + C_{par}\right)}} \tag{32}$$

At that frequency the inductor has no impedance, then starts behaving like a capacitor: to be sure that calculations fit with real inductor's behavior, the output oscillation angular frequency ω_0 must be lower than ω_{sr} [4], [12].
C_{par} is the equivalent parallel capacitance of the shunt branch composed by R_{Si}, C_{ox} and C_{Si}. Its calculation is fully justified in [13].

2.3.3 Inductor's geometrical equation

Different equations are proposed in literature to predict the inductance L, in base on inductor's geometrical property. The one adopted in this thesis is the following:

$$L = k_1 \mu_0 \frac{N^2 d_{avg}}{1 + k_2 \rho_d} \tag{33}$$

where:

- $d_{avg} = \frac{d_{in}+d_{out}}{2}$ is the average coil's diameter;
- d_{in} and d_{out} are the inner and outer coil diameter;

- N is the number of turns;
- $rho_d = \frac{d_{out}-d_{in}}{d_{out}+d_{in}}$ is called the "fill factor";
- μ_0 is the vacuum magnetic permeability.

k_1 and k_2 are constants linked to the inductor's shape:

- for a square coil, $k_1 = 2.34$ and $k_2 = 2.75$;
- for an octagonal coil, $k_1 = 2.25$ and $k_2 = 3.55$.

Rewriting the equation (33) as a function of d_{in} and d_{out} it's possible to obtain:

$$L = \frac{k_1 \mu_0}{2} \frac{N^2 \left(d_{out} + d_{in}\right)^2}{d_{out}\left(1 + k_2\right) + d_{in}\left(1 - k_2\right)} \tag{34}$$

Since the denominator second addend is always negative, is clear that increasing d_{in} and fixing d_{out} increases the numerator and decreases the denumerator, enlarging the inductance. But this choice affects the quality factor: the metal used to implement the coil is less wide and so parasitic series resistance is bigger.

2.4 Inductor's shield theory

Looking at inductor lumped model reported in Fig. 11, it's clear that a possible way to reduce inductor losses is to avoid current flow through substrate. It can be done in two ways:

- setting $R_{Si} \approx \infty$ by the addition of a non conductive layer over the substrate to limit the current flow. This solution is not very simple: materials which are less conductive than the already present oxide are not so common;
- setting $R_{Si} \approx 0$ with the use of a metal shield which can short this resistance. It can be ground connected or floating.

2.4.1 Ground connected metal shield

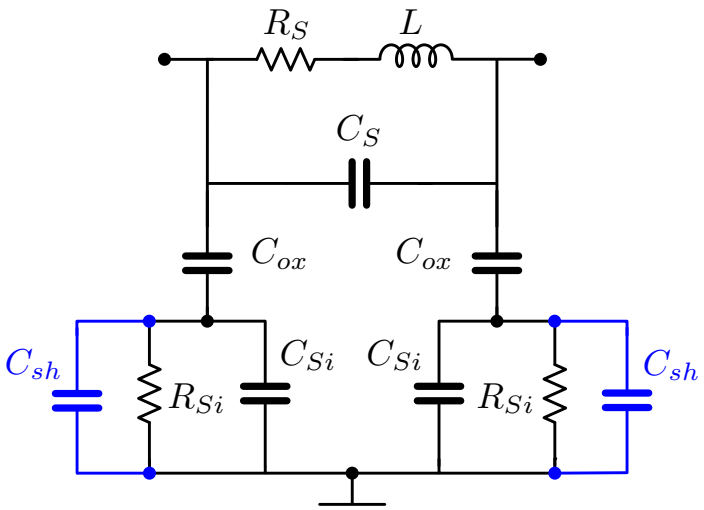

Figure 12: RF lumped model of an integrated inductor with a ground connected shield . Shield's parasitic capacitances are in blue.

To avoid the ac current flow in the shunt branch composed by R_{Si} and C_{Si}, a metal plate over the substrate could create a very low impedance path toward ground. In particular, the shield's capacitance C_{sh} helps C_{Si} in shunting the current from R_{Si}, decreasing the losses as shown in

Fig. 12. So, adding a ground connected metallic shield closest as possible to the substrate could short the substrate equaivalent resistance, but introduces new losses: in a large metal area, Eddy currents can flow in low resistive loops, strongly affecting coil's inductance and its quality factor [12]. In order to avoid these unwanted magnetic coupling effects, the shield should be patterned i.e. composed by single metal strips, in order to increase the loops' resistance. In addition, if these strips are orthogonal to the inductor's routings, parasitic currents are minimized. If the shield's pattern is well done, any significant difference in the inductance can be noticed.

This shield topology requires on-chip connections and since the RF ground is not usually exactly equal to 0V, some disturbances can be injected in the circuit through shield's capacitances.

2.4.2 Floating metal shield

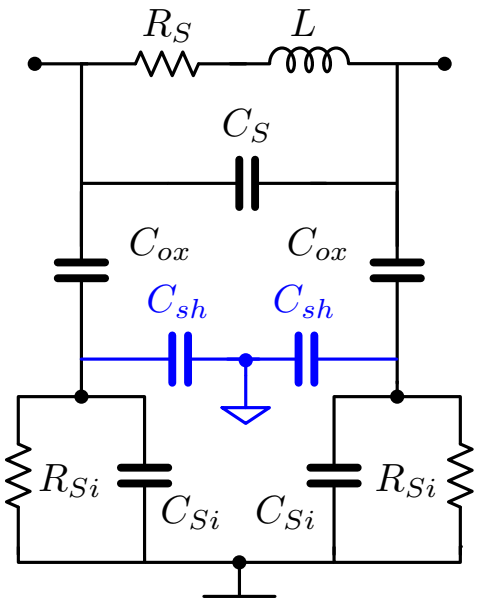

Figure 13: RF lumped model of an integrated shielded spiral inductor. Floating shield's parasitic capacitances are in blue.

Comparing Fig. 12 and Fig. 13, it's possible to see the main difference between the ground connected and the floating shields electrical models. If the metal strips are superimposed side-to-side with the inductor, it's possible to assume that the floating shield's parasitic capacitances C_{sh} are ac-ground referred.
This effect is caused by the fact that the shield is "differentially driven" [14]: the current induced in the strips by an inductor side has opposite direction to the one induced in the other side in the same strips. The total ac induced current in the shield is null [15].

So, using a floating shield with side-to-side metal strips makes not only simpler the connections (no ground connections are needed) but also minimize the coupling with the RF ground.
With this shield topology implemented in low metal layers, close to the substrate, it's possible to achieve the best inductor's quality factor Q_L.

2.4.3 Study of the state-of-the-art

After these significant results, is important to not forget the objective of this thesis: build an entire LC-based DCO underneath the inductor.
Until now, under the inductor is considered only the substrate and an oxide layer. The metal shield has been taken into account only to understand how to increase Q_L. Nothing has been said about the use of metal shields to electrical isolate the inductor from the beneath circuitry.

In Fig. 14 is reported the cross-section view of a patterned ground shielded (PGS) inductor. The befenits, in terms of inductor's quality factor, are linked to the distance D between the inductor and the shield:

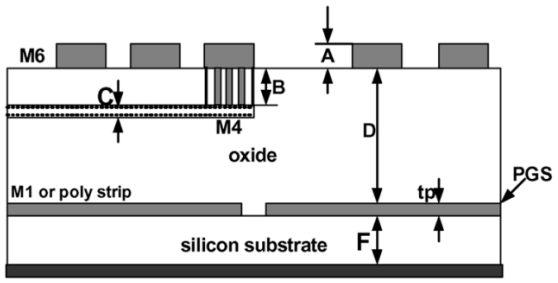

Figure 14: Cross-sectional view of an on-chip spiral PGS inductor in 0.18μm CMOS

larger it is, better is Q_L [16].

So, a careful analysis has to be done before putting a metal shield in proximity to the inductor in order not to degrade too much its quality factor.

In literature, few examples of voltage controlled oscillator underneath the inductor are reported.

In [6] Jha et al. show two different VCOs, both underneath a multi-turns inductor. This choice is led by the fact that their main target is to minimize area consumption.

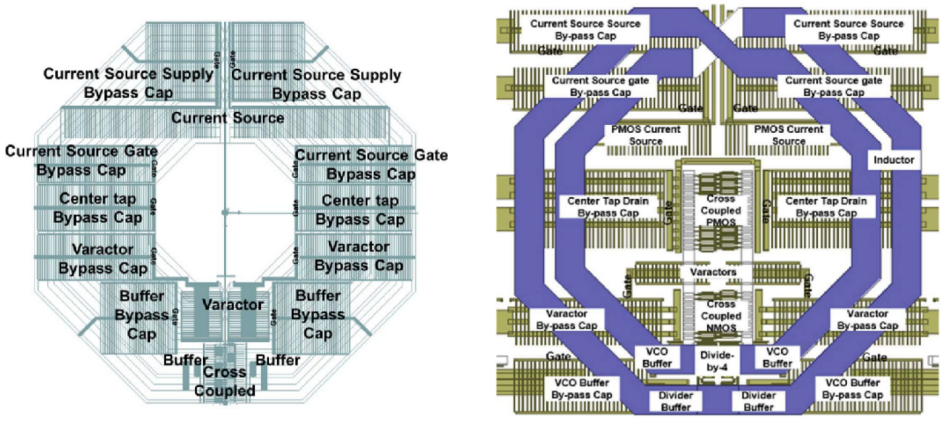

Figure 15: 4.3-5.6GHz first pMOS VCO (left) and 16-19GHz second cMOS VCO (right)

Since the inductor and underneath analog circuitry currents are very

similar, they avoid magnetic coupling and electrical losses with careful layout choices:

- multi-finger structures, perpendicular to the inductor's routings, are used;
- if possible, the underneath circuitry should be position far from the inductor's center (where the EM field is maximum);
- ac-loops are avoided positioning in a symmetrical way all the underneath blocks;
- metal-1 ground connections are used to create a PGS.

This last layout choice is also used in other underneath inductor's VCOs, like the one reported in [17].

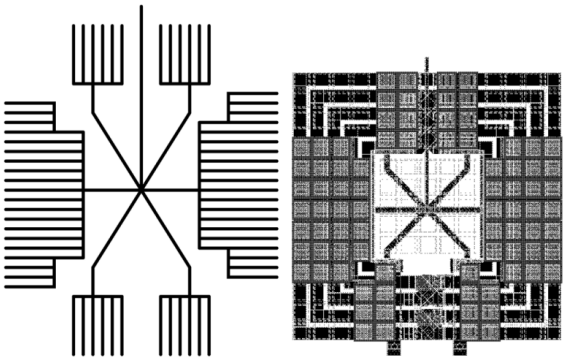

Figure 16: tuning signal path (left); inductor and varactors layout view (right)

As shown in Fig. 16, the varactors occupy the area under the inductor routings, and the tuning signal path is built in order to create a PGS close to the substrate, which increases inductor quality factor. In this two last publications, only VCO with varactor-based continuous tuning are considered. As already said, the authors didn't consider the use of

a metal shield immediately under the inductor because proper layout could minimize the magnetic coupling and the electrical losses. The coupling between inductor and underneath circuitry is minimal, since their currents are similar. A proof of that is the absence of significant differences in the oscillator output voltage spectrum and in the oscillator output phase noise with or without structures beneath the coil.

Following what said until now, if the inductor and underneath structures currents are very different, coupling effects become more evident. So, for example, deciding to put digital circuitry beneath the inductor could arise the final circuits' phase noise: the presence of clock signals, which have a lower frequency than the oscillation one introduce spurious harmonics which can degrade Q_L and the output phase noise. Other sources of additional noise could be the capacitor bank's switching activity and the supply ripple caused by the power switching converters.. Careful layout choice are no more sufficient to preserve overall circuits' performances and the use of a shield directly under the inductor is needed, as reported in [18].

Sharkia et al. propose a beneath the inductor complete frequency synthesizer (made by a 5GHz DCO, sub-sampling PLL, frequency divider and a reference buffer). In order to avoid coupling effects they use a patterned ground shield (PGS) to electrically isolate the inductor from the circuitry. It is composed by metal 7 long strips, perpendicular to inductor current direction, of width which matches the maximum linewidth used in synthesizer routings (1.5μm).
To overcome magnetic coupling linked problems, they also avoid at all

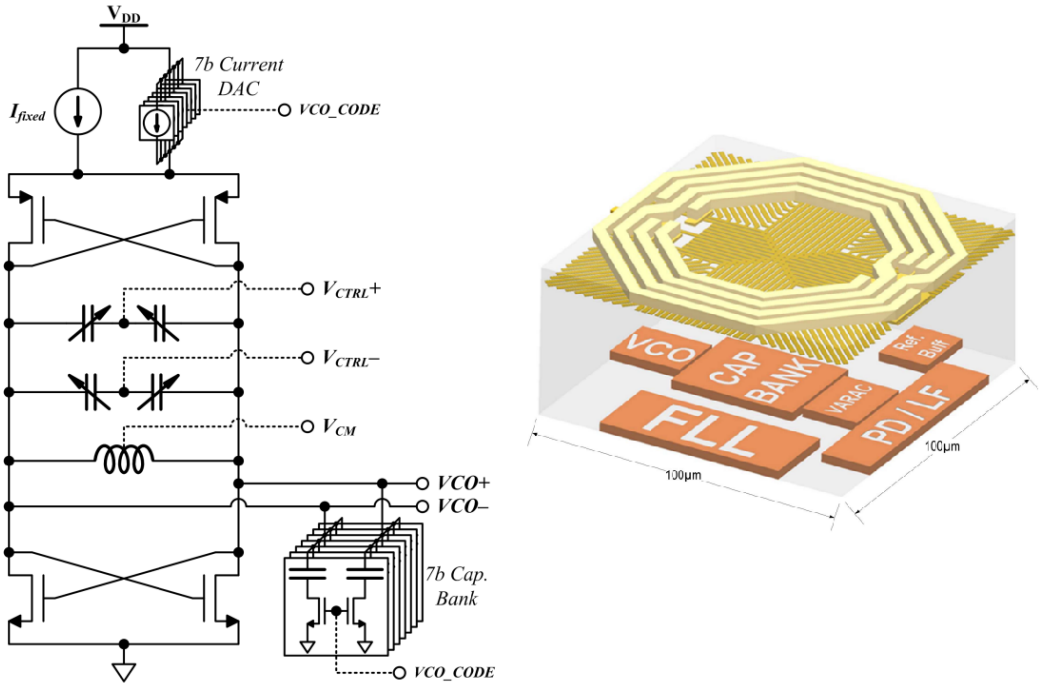

Figure 17: proposed DCO schematic (left) and complete frequency synthesizer image (right)

cost closed metal loops and they use multifinger MOM capacitors instead of MIM, made of large plates. Measurements show that addition of the patterned ground shield causes:

- a small degradation in the inductor's quality factor at frequency of interest;
- a left shift in the inductor's quality factor peak;
- a shift of the inductor's self resonance frequency to a lower frequency.

2.4.4 Electrical model

Since the shield addition arises the total parallel capacitance seen by the inductor, attention must be paid to the self-resonance frequency which assumes a lower value. A too small frequency is dangerous for the reasons

discussed in section 3.2 of this chapter.

In order to evaluate this effect, electrical models (very similar to the one shown in sections 4.1 and 4.2) are obtained:

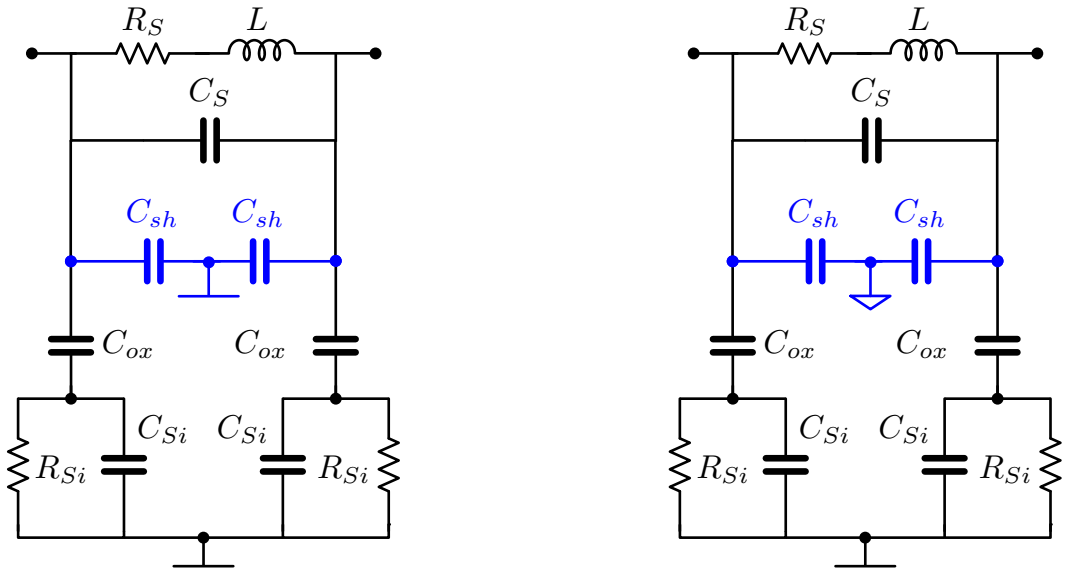

Figure 18: patterned ground connected shielded inductor model (left) and floating shielded inductor model (right)

In Fig. 18 the shield under the inductor equivalent electrical model is highlighted in blue.

Making the assumption that the shields electrically insulate the inductor and so negligible leakage currents flow through the oxide capacitances C_{ox}, the inductor's self resonance angular frequency ω_{sr} becomes in both cases:

$$\omega_{sr} \approx \frac{1}{\sqrt{L\left(C_S + \frac{C_{sh}}{2}\right)}} \tag{35}$$

The coupling capacitance C_{sh} between the inductor and the shield is directly linked to these two structures superimposed metal area: strips' width and spacing have to be properly size to find a trade off in terms of inductor electrical isolation and self resonance angular frequency.

Another made assumption, in sake of semplicity, is to neglect strips inductance since it is very smaller in respect with the inductor's one equal to L.

For completeness, supposing that shield's metal layer should be employed to implement some circuit's connections, the use of a shield with a central hole is also considered.
The floating shield with an inner hole is called by Long et al., in [15] and in [14], "ladder" and presents the worst performances, in terms of the inductor quality factor, since the strips with the same orientation are no more side-to-side connected and so the shield results no more "differentially driven".

3 Design

3.1 Specifications

- Oscillation frequency: $f_0 = 10\text{GHz}$
- Maximum current consumption: $I_{bias,max} = 2mA$
- Phase noise $\mathscr{L}(\Delta\text{f}=1\text{MHz}) \leq$-110dBc/Hz
- Coarse tuning 1.8GHz

  The first guess was 1.5GHz but, to lock the oscillation frequency over process, it has been chosen equal to 1.8GHz
- Fine tuning 200MHz, LSB 1.6MHz

3.2 Inductor design

After topology choice, three assumptions are done:

- transconductance safety factor α_{min} is set equal to 2;
- output phase noise, at $\Delta f = 1MHz$ and $T = 300K$, is fixed equal to -112dBc/Hz: some margin is taken on given specification value;
- tank quality factor at $f_0 = 10GHz$ is initially fixed equal to 12: since the inductor will be very big, considering a tank quality factor in the order of 10-15 is a good assumption.

Is now possible to start the design looking at the previously described equations and, finally, to plot the obtained main oscillator's quantities as a function of the ratio between the tank's single ended capacitance C and inductance L:

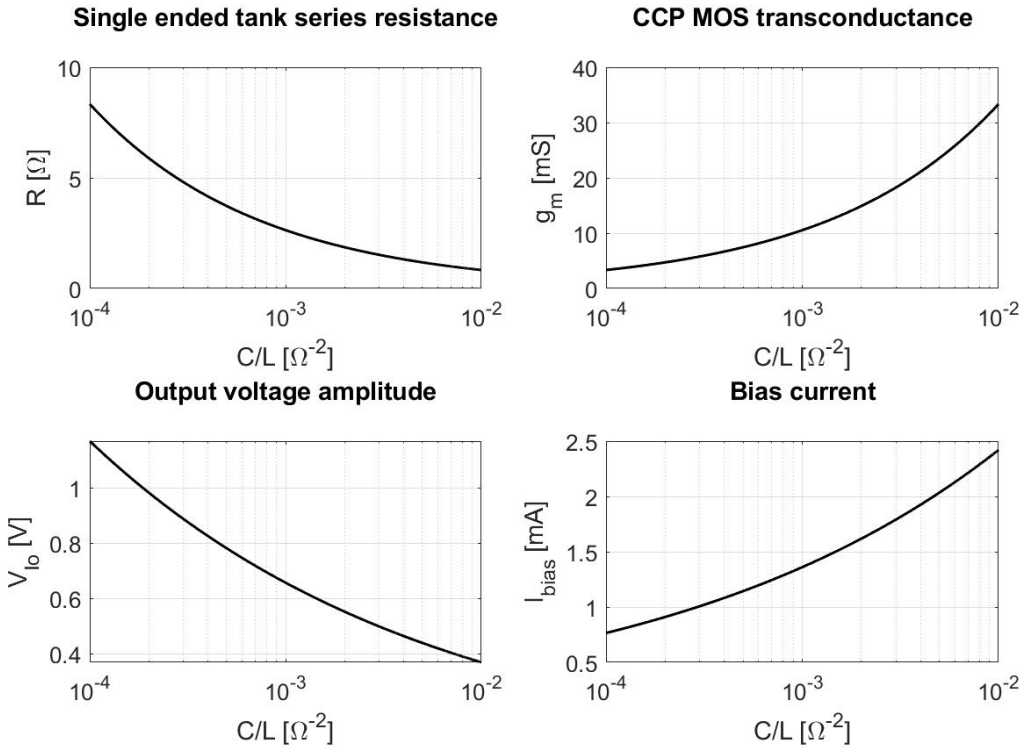

Figure 19: Design quantities as functions of the ratio C/L

The main constraint in the choice of L and C is the voltage power supply. It's true that to small C/L values correspond high $V_{LO,0p}$ and low bias currents I_{bias} values, but the voltage power supply equal to 0.9V in 28nm technology limits the maximum oscillator's swing. Having said that, simulations are performed and finally $C/L = 2.5m\Omega^{-2}$ is chosen. Needed differential tank inductance results $L_T = 320pH$, so $L = 160pH$.

To satisfy the low power consumption specification, without consuming silicon area, the chosen inductor's shape is the octagonal one: for the same occupied area, an octagonal inductor presents a higher quality factor in respect with a square spirals one. Moreover, the quality factor is enhanced by the fact that the inductor is implemented with a single spiral in metal 8, which is the metal layer with the lowest resistance per

sheet (since it is the top one).

In effort with equation (34), the estimated inductor's inner and outer diameter are $d_{in} = 155\mu m$ and $d_{out} = 180\mu m$ respectively. Surely, a bigger inner diameter is needed, since around the inductor is placed a ground connected metal guardring. This structure consists in a metal square-shape ring with inner diameter which is around half the inductor's outer diameter. Even if it degrades a little the inductor's properties, it is necessary to isolate the inductor from external circuitry which can couple with it, changing inductance and quality factor in a non predictable way. In addition, to be sure that coarse and fine banks fit inside inductor area, minimizing their distance with coil pins, the final choice is a non symmetric inductor with dimensions reported in Fig. 20. The achieved differential inductance is $L_T = 308pH$, a self resonance frequency $f_{sr} = \frac{\omega_{sr}}{2\pi} = 74GHz$ and a quality factor $Q_{L_T}(f_0) = 33.5$ (Fig. 21). Since the oscillation frequency f_0 is more than 7 times lower than the self resonance frequency, $Q_{L_T}(f_0)$ has been calculated as the ratio between the imaginary part and the real part of the inductor's impedance Z_{L_T}:

$$Q_{L_T}(f_0) = \frac{\Im\{Z_{L_T}(f_0)\}}{\Re\{Z_{L_T}(f_0)\}} \tag{36}$$

The choice of the single turn width equal to $d_{out} - d_{in} = 25\mu m$ is led by the need to maximize the quality factor and so to reduce the metal ohmic losses. Such a wide metal turn could present a non negligible capacitive coupling with underneath structures which could drastically degrade the inductor's self resonance frequency.

Simulations were performed with $17\mu m$ and $21\mu m$ wide spiral: in the next section dedicated to shield design, will be clear how it degrades

inductor's quantities and why a rouitng width equal to $25\mu m$ is adopted.

In order to connect the inner structures with the inductor, two metal 8 strips are needed as shown in Fig. 20. Their length is linked to the inner structures dimensions, their width is chosen finding a good trade off between achieved quality factor and inductance variation through the strips length. $15\mu m$ width metal connections permit to have an inductive variation among the entire metal length lower then 10% in respect with the previous inductance L_T obtained by EM and SP simulations, with a negligible degradation of the quality factor.

Figure 20: Inductor momentum 3D view (metal 8 layer)

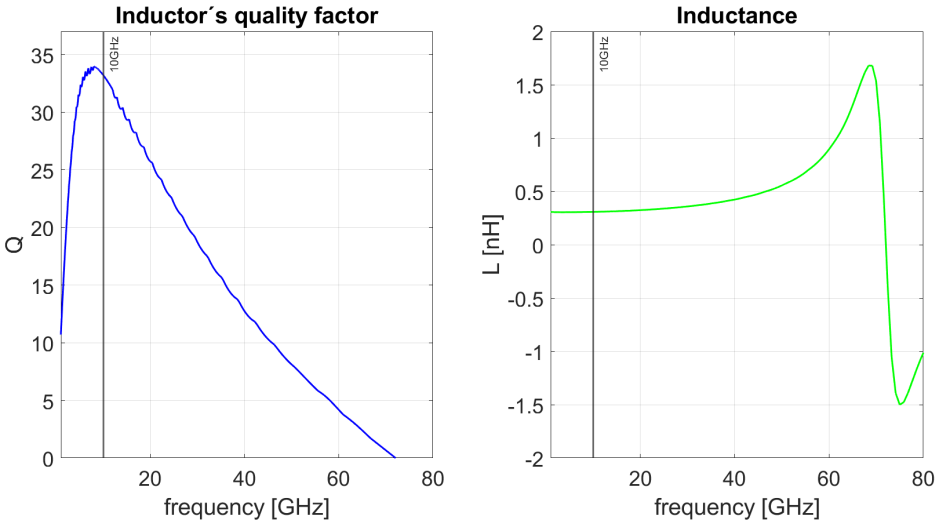

Figure 21: Inductor layout view (metal 8 layer)

3.3 Capacitor banks layout

Two thermometric banks made of switched caps cells are used in this project: one for the coarse tuning and one for the fine tuning. In both of them, MOM capacitors are used to minimize the magnetic coupling with the inductor.
Two separate sections are dedicated to their design.

3.3.1 Coarse bank design

Starting from specifications, a coarse tuning of 1.8GHz is needed. Since controlling a number of cells equal to a power of two is simpler, a 16 cells bank is implemented for coarse tuning.
Each cell presents the following characteristics:

- $C_{on} = 28.0fF$
- $C_{off} = 9.1fF$
- $R_{bias} = 46k\Omega$
- $Q_{on} = 26.4$
- $Q_{off} = 49.9$

Knowing that the inductance is equal to 308pH, the total tank capacitance variation needed to achieve the specification tunig value is estimated using equation (29) which gives $\Delta C_T = 301fF$. Even if the coarse tuning range specification is 18%, also equation (30) could be used and it gives a very close result: $\Delta C_T = 296fF$.
So the needed per cell capacitance variation has been obtained simply dividing ΔC_T by sixteen, $\Delta C_C = 18.8fF/cell$. As shown in Fig.23,

each capacitor C is implemented by two parallel squared capacitors: this choice lets to achieve higher quality factors both in ON and OFF cell's states, in respect of using a single big rectangle capacitor.
The two bias resistors R_{bias} are set equal to $46k\Omega$ since for this value a trade off in between achieved off quality factor and space occupation is found. Such a big resistance is justified by the fact that this bank will be used to lock the frequency, in static operations, so the switching time between OFF and ON states is not critical.

The final coarse bank is a 2 rows by 8 columns mosaic. All the cells output pins are connected in parallel via metal 7 strips, as shown in Fig.22.

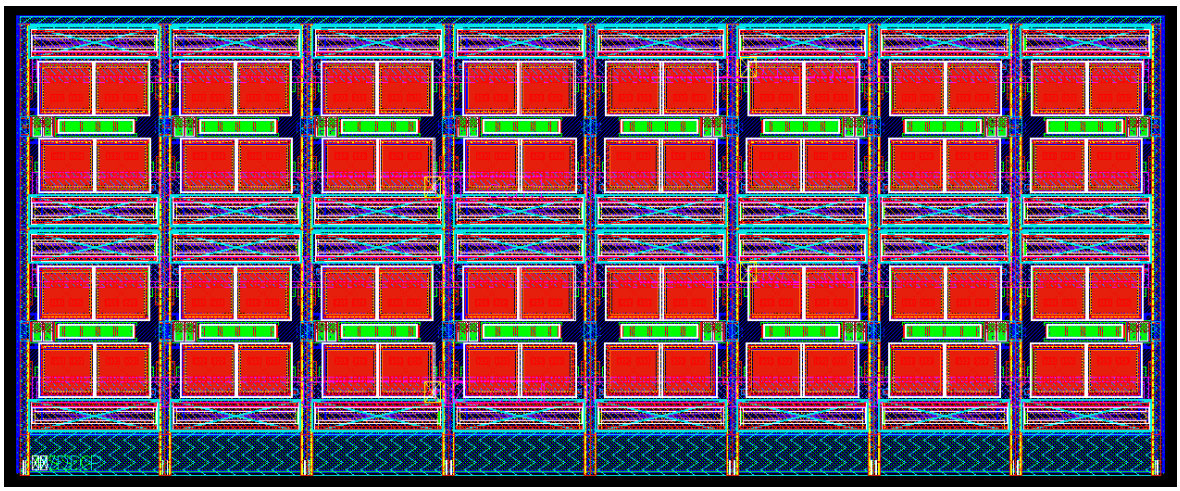

Figure 22: Coarse bank layout view

3.3.2 Fine bank design

Starting from specifications, a fine tuning range of 200MHz is needed. A 128 cells bank is implemented for fine tuning operations.
Each cell presents the following characteristics:

- $C_{on} = 1.785fF$
- $C_{off} = 1.475fF$
- $R_{bias} = 11k\Omega$
- $Q_{on} = 88.4$
- $Q_{off} = 41.3$

The needed tank capacitance variation is again found using equation (30): $\Delta C_T = 33fF$. Dividing this number by 128, the single per cell capacitance variation results equal to $\Delta C_C = 0.26fF/cell$. In order to achieve such a low capacitance variation, very little capacitors are used, which present high quality factor.
The small bias resistance value $R_{bias} = 11k\Omega$ strongly affects the OFF quality factor, but is needed in order to reduce the time transition between OFF and ON state, since these cells are used in dynamic operations.

The final fine bank consists in a 8 rows by 16 columns mosaic. Around it a frame made of dummy switched capacitor cells is added in order to allow all cells to see the same environment around them, as shown in Fig.23. Also in this case all the cells are connected in parallalel via metal 7 strips.

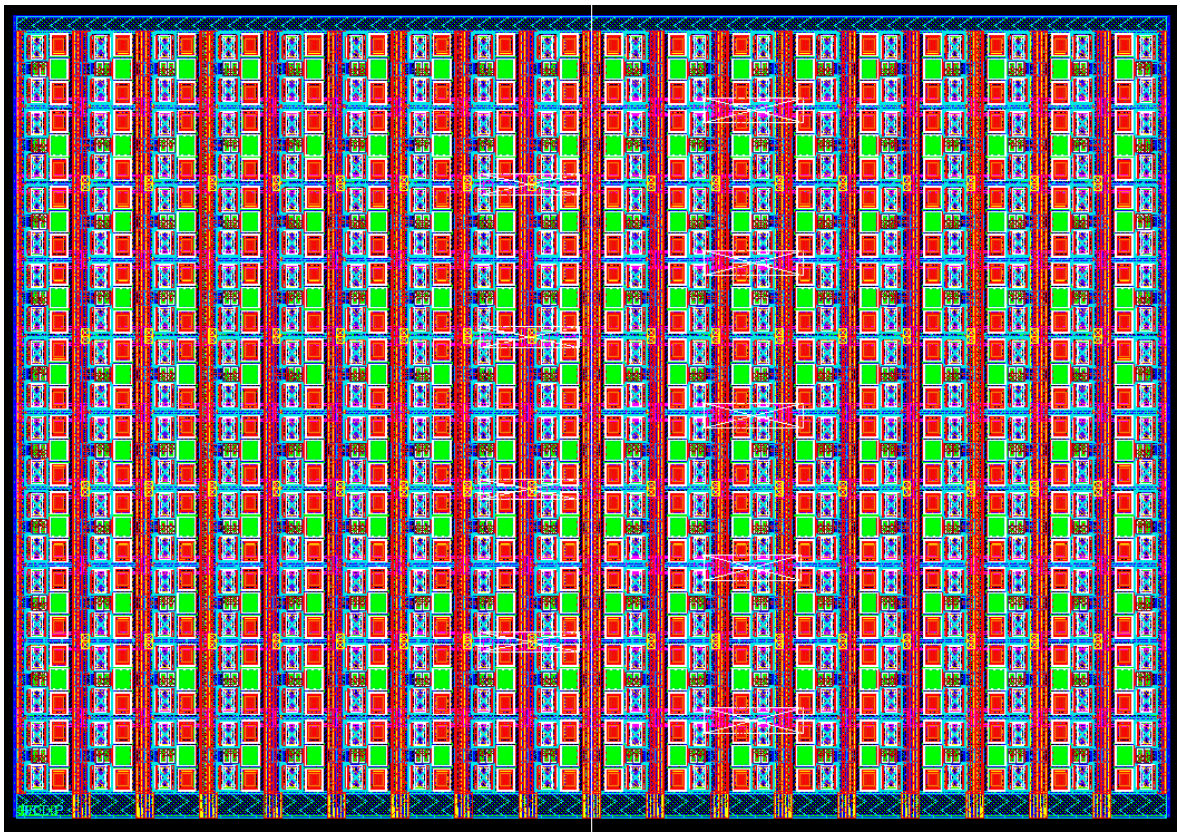

Figure 23: Fine bank layout view

3.4 Cross coupled pairs design

Since the cMOS topology presents the advantage of lower phase noise at the same power consumption, two cross-coupled pairs are designed. The start up condition (13) is at first considered. As said at the beginning of this Chapter, the transconductance safety factor is fixed arbitrarily, making some considerations.

The proper value of the transconductance safety factor α_{min} is chosen finding a trade off between the mirror's headroom, power consumption and noise specifications.
The phase noise injection happens when all transistors are conducting at the same time. To reduce this CCP's commutation time, cMOS are sized with the same transconductance as explained by Jha et al. in [6]. Equal MOSFETs' transconductances permit to have better rise time and fall time simmetry which reduces the upconversion of transistors' flicker noise.
In this sense, a big g_m could be chosen to achieve better results, but more current should be used to sustain oscillations, affecting the power consumption. Moreover, higher current means bigger bias circuit's dimensions needed to achieve the chosen bias MOSFET's V^*. Too big g_m also causes the arise of the parasitic capacitances of the cross-coupled pairs, affecting the achievable tuning range.
Considering all these particulars, a good trade off is found choosing the transconductance safety factor α_{min} approximately equal to 2.

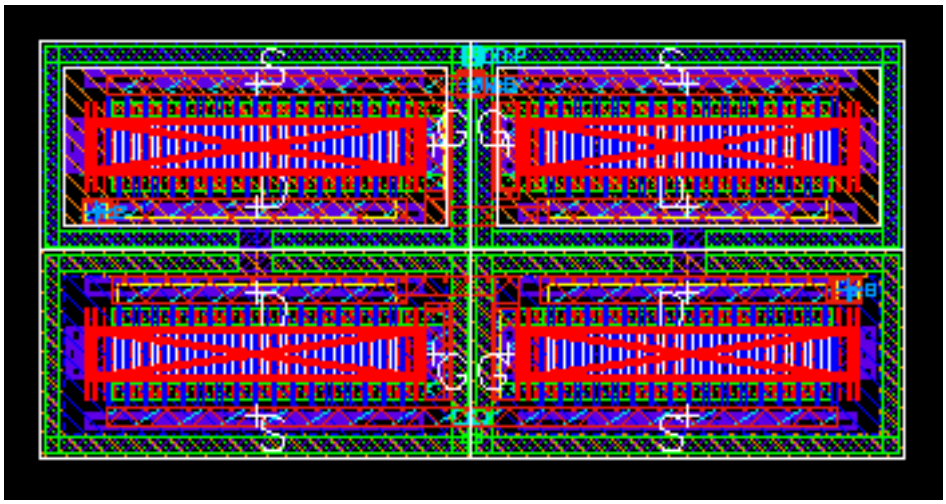

Figure 24: Two cross-coupled layout view

3.5 Biasing circuit design

In order to properly bias the circuit, two solutions are considered at the beginning: a passive one and an active one.

A simple resistor between the power supply and the oscillator's common mode node could be used to fix the current flowing into the oscillator. If on one hand it is a flicker noise free (resistances are only affected by white nosie) and space saving solution, on the other lets the current to be dependent on power supply variations.

This is why the chosen biasing circuit is a pMOS based current mirror: it fixes the oscillator DC operating point, ensuring a good robustness in respect to PVT variations. Moreover, the topology is the simplest one composed by two transistors, due to the low voltage power supply. It doesn't allow to cascode lots of transistors which have non negligible V^*. Long channel pMOSFETs (e.g. 1μm) are used in order to increase the mirror output resistance, which reduces the amount of injected flicker noise.

3.6 Phase noise reduction techniques

3.6.1 Mirror's RC filter

To reduce the overall power consumption, high mirror ratio M are used. In this way the reference current I_{ref} can be very small compared to the bias one I_{bias}. But very high mirror ratios cause also an increase of the injected noise by the reference branch in which the diode connected transistor is conducting.
Two solutions are found: use a not so high mirror ratio M and add an RC passive filter.

Since the bias current maximum value is equal to 2mA, M is then set to 20: the reference current is very small in respect with the bias one and doesn't degrade so much the overall power consumption.
The addition of a passive RC filter in between mirror's transistors gates needs negligible leakage currents through them. To be sure that this condition is met, 1.8V pMOSFETs are used to implement the bias circuit: these transistors present a thicker gate oxide and so practically zero leakage currents. The resistance is chosen equal to $R_f = 2.2M\Omega$ and the capacitance equal to $C_f = 20pF$.
In order to size R_f and C_f, some simulations were performed: for very high resistances the phase noise at $\Delta f = 1MHz$ is practically the same as using an ideal current source, but the low offset noise arises. It isn't always a problem. Infact, if the oscillator will be used to implement a PLL, the flicker noise willl be strongly attenuated.

3.6.2 Tail capacitance

In order to suppress unwanted higher order harmonics, which degrade the output phase noise, a tail capacitor is added between the common mode node and VDD. Its value is chosen equal to $C_{tail} = 2pF$.

The final circuit's schematic, which considers the fine and coarse banks, is the one reported in Fig. 25

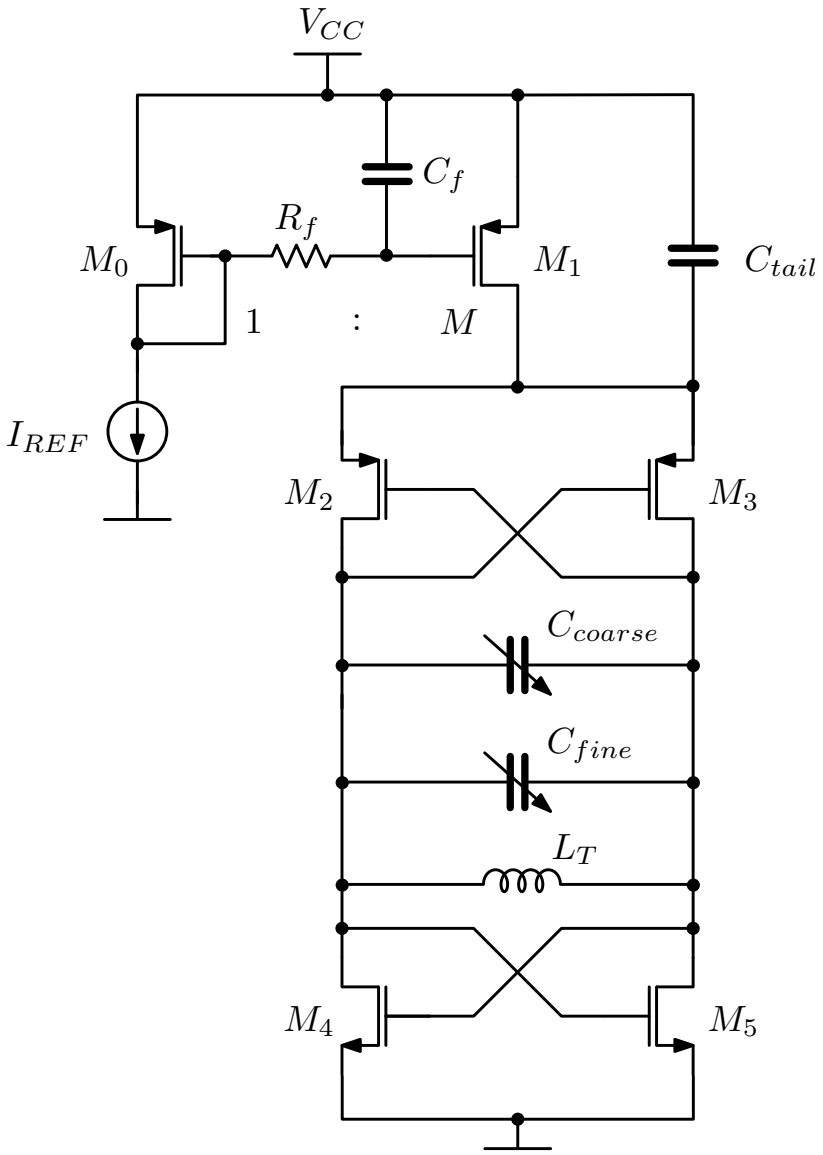

Figure 25: DCO final schematic

3.7 Inductor's shield design

The inductor's shield design was the most challenging part of this DCO design. Looking at the already used metal layers the only one left in between the inductor and the underneath circuitry is metal 7.

Considering theory and inductor layout, some customize shields are designed. The technique used in layout view is to draw eight sets of parallel fingers, each one of width W_f distant S_f from the closest one, perpendicular to the inductor's sides. Going toward the inductor's center, these sets intersect. Their fingers are carefully cut and merged in order to avoid loops. The line in between two different merged sets coincides with half inductor's diagonal: this geometrical choice should minimize the magnetic coupling between inductor and shield through all the inductor's area.
Finally, three different shields are taken into account. Arbitrarily, they are called:

- double-cross connected shield: it is a patterned shield, connected to ground. All the eight finger sets are ground connected, since they are attached to the guardring;
- single-cross connected shield: it is a patterned shield, connected to ground. Only four finger sets are connected to the guardring;
- floating shield: it isn't connected to the guarding and all the finger sets cover the full inductor's area, plus a rectangle over each side of height W (the inductor's routing width) and base approximately equal to the outer inductor's side length.

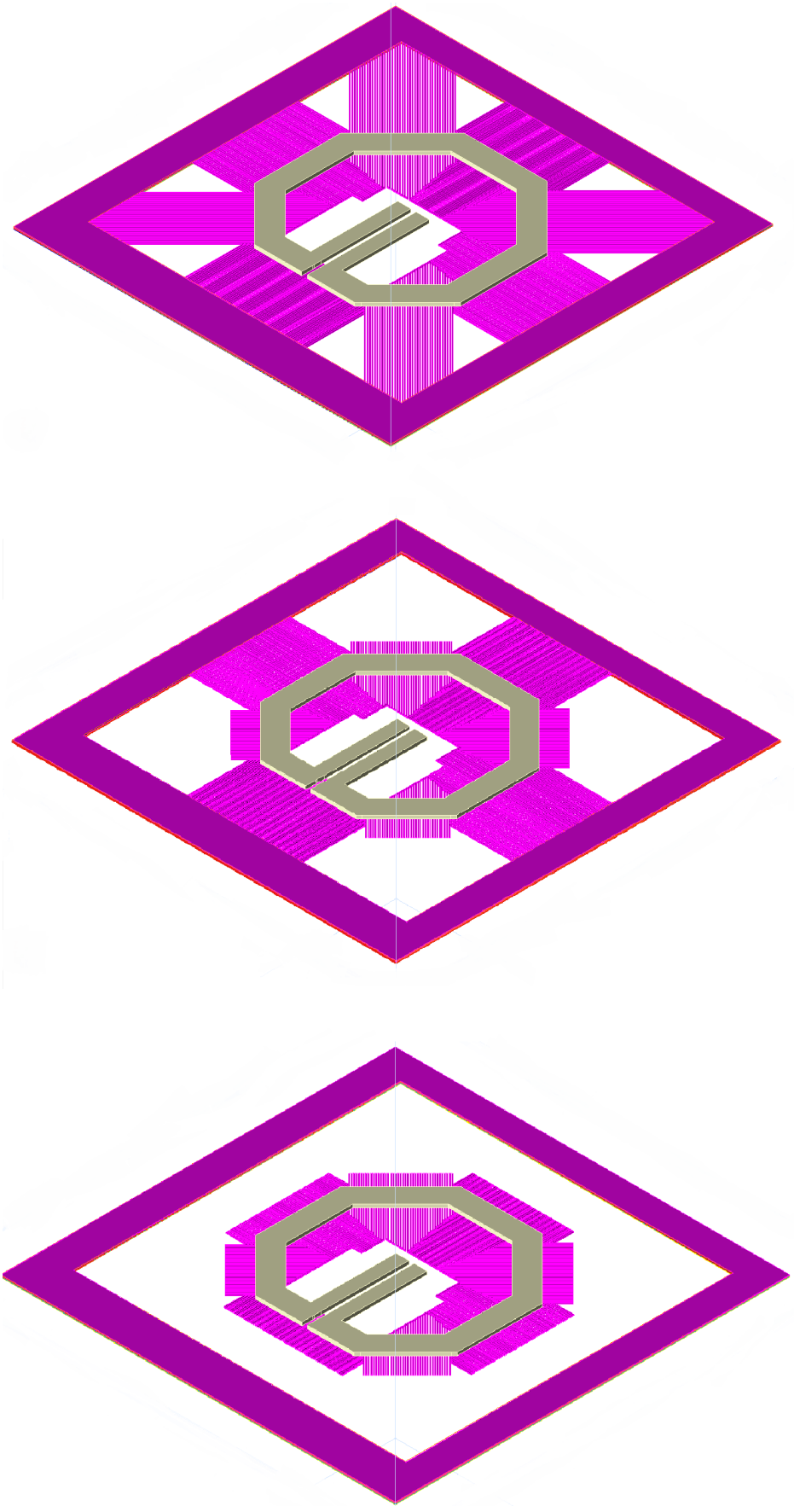

Figure 26: Inductor shielded with: double cross connected shield (top); single cross connected shield (middle); floating shield (bottom)

The choice of W_f and S_f is the result of a trade off in between the inductor's self resonance frequency and quality factor. The electrical isolation is proportional to the shield's metal density. But a too much metal increases the overlap capacitance between the shield and the inductor decreasing the self resonance frequency.
That being said, the three previously described shields are implemented with strips of width $W_f = 1\mu m$, equally spaced by a distance $S_f = 1\mu m$. Considering also the banks footprint, a hole is cut through the shield.

3.7.1 Studied shield topologies

By electro-magnetic and S-parameters simulations, the following shielded inductor's quantities are obtained:

Shield type	$\boldsymbol{Q_{L_T}(f_0)}$	$\boldsymbol{f_{sr}}$	$\boldsymbol{L_T(f_0)}$
Double cross	19.76	31GHz	305pH
Single cross	25.76	26GHz	317pH
Floating	28.19	47GHz	310p
No shield	33.50	74GHz	308pH

Table 1: Simulations results with different shields

To estimate shielded inductor's quality factor, (36) is used at the beginning. Since the inductor's resonance frequency isn't very bigger than f_0 in all cases, a better estimate of $Q_{L_T}(10GHz)$ (reported in Table 1) is done looking at the derivative in respect with the frequency of the impedance Z_T imaginary part phase of a tank resonating at f_0, made of the inductor L_T and a loss-less capacitor. In this way the inductor's quality factor coincides with the tank's one, which is:

$$Q_{L_T}(f_0) = \left| \frac{d\angle Z_T}{df} \frac{f}{2} \right|_{f=f_0} \tag{37}$$

To estimate the inductance at the oscillator output frequency f_0, the impedance Z_T imaginary part is again considered:

$$L_T(f_0) = \frac{\Im\{Z_T(f_0)\}}{2\pi f_0} \tag{38}$$

3.7.2 Final inductor's routing width choice

As mentioned in section 3.3, the inductor's routing width is set equal to $25\mu m$. This choice is led by the need of a sufficiently high quality factor to respect the bias current and phase noise specifications.

Looking at Table 1, the inductor's self resonance frequency, with $W = 25\mu m$ wide routing, is just 3 times f_0 for ground connected shields and 5 times f_0 for floating shield, a possible way to enlarge f_{sr} is reducing W. In addition, thicker metal means less area consumption to achieve the same inductance L_T.

Three different W values are analyzed:

Shield type	**$17\mu m$**	**$21\mu m$**	**$25\mu m$**
Double cross	38GHz	35GHz	31GHz
Single cross	37GHz	34GHz	26GHz
Floating	54GHz	52GHz	47GHz
No shield	75GHz	75GHz	74GHz

Table 2: Self-resonance frequency f_{sr} for different routing widths

From Table 2 is clear that the inductor's self-resonance frequency is

strongly dependent on the underneath shield topology. Moreover, since the inductance is the same for all routing width, the inductor sees more parallel capacitance if ground connected shields are used.
Inductor's quality factor is checked: small W means higher f_{sr} but it also increases the inductor ohmic losses.

Shield type	**17μm**	**21μm**	**25μm**
Double cross	12.06	16.01	19.76
Single cross	11.16	16.31	25.76
Floating	23.76	26.48	28.19
No shield	31.56	32.62	33.50

Table 3: Quality factor Q_{L_T} for different routing widths

Looking at the obtained quality factors in Table 3, it's clear that the smaller is W, the lower is the quality factor. The final simulations, which makes clearer why the chosen routing width is $25\mu m$, are the ones linked to the oscillator's output phase noise. The oscillator with the floating

Shield type	**17μm**	**21μm**	**25μm**
Double cross	-108.0dBc/Hz	-111.1dBc/Hz	-112.5dBc/Hz
Single cross	-107.2dBc/Hz	-111.3dBc/Hz	-112.7dBc/Hz
Floating	-112.6dBc/Hz	-112.7dBc/Hz	-113.0dBc/Hz
No shield	-112.6dBc/Hz	-112.7dBc/Hz	-113.0dBc/Hz

Table 4: Oscillator's phase noise at $\Delta f = 1MHz$ for different routing widths

shielded inductor is the one which is less affected by the routing width change. On the contrary, the inductors with the two ground connected shields cause a strong degradation of the DCO's phase noise if W is too

small. Moreover, since is needed to take some margin in the simulated phase noise results, $W = 25\mu m$ seems a good choice: for smaller values, the use of ground connected shields is no more possible, in terms of phase noise (Table 4).
Data collected until now are not sufficient to discard two of the three studied shield topologies.

3.7.3 Shields' insulation properties

Until now, the only two quantities taken into account to evaluate shields' goodness are the inductor's quality factor and the achieved oscillator pahse noise at the offset of 1MHz. Anything is said about the behavior of the DCO if some noise sources are located beneath the shield.
Infact, the main feature of these shields is to avoid the coupling between the inductor and the underneath circuitry. In order to quantify how much the different shield topologies avoid coupling, some metal structures are drawn in metal layers lower than M7 and different signals are injected trough them. Then the transfer function between the oscillator output voltage and the input noisy signal is considered.
In order to have a more complete view about the behavior of the oscillator with a shielded inductor and underneath circuitry, the transfer functions are calculated as a function of the frequency offsets referred to $f = 0Hz$ (DC) and to $f_0 = 10GHz$ (DC-to-RF) to let understand better how the noisy signals affect the low frequency output voltage spectrum, and, most importantly, how the noisy signals affect the spectrum around the output oscillation frequency.

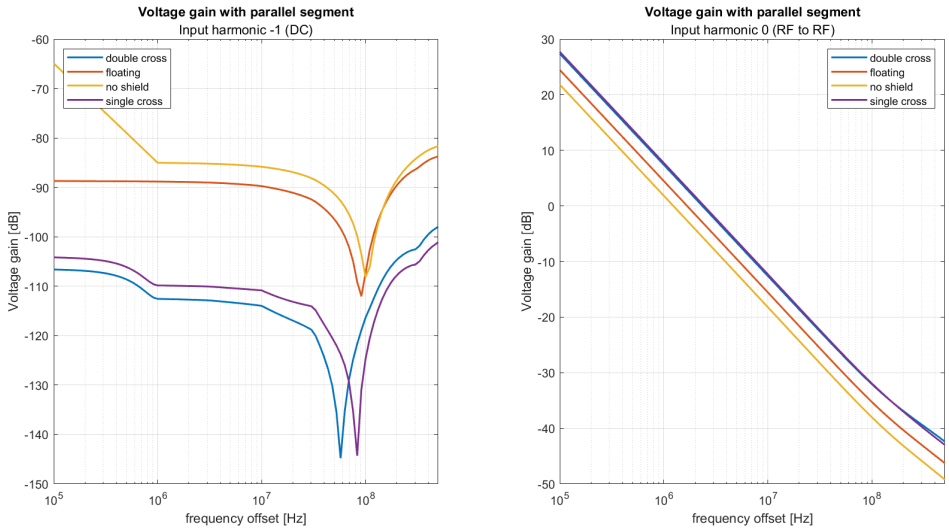

Figure 27: Voltage gain: metal strip, parallel to the inductor's routing

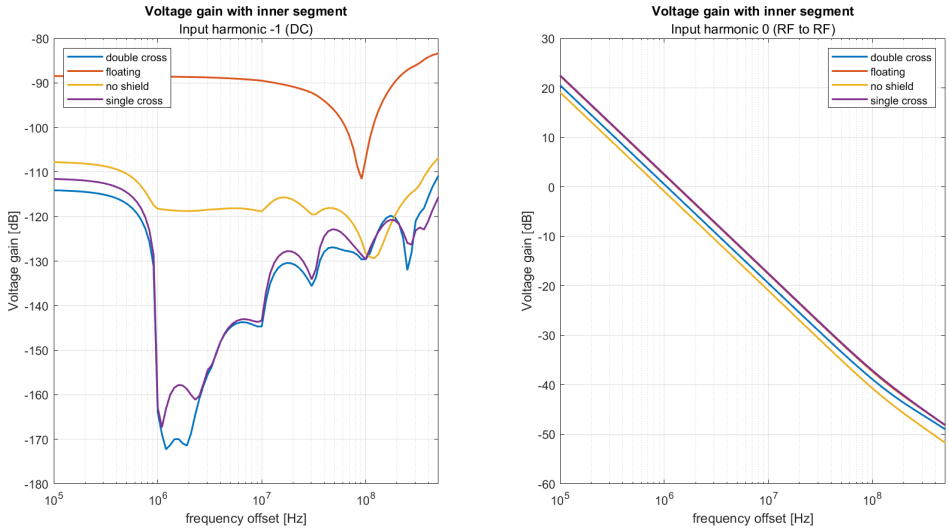

Figure 28: Voltage gain: metal segment, inside the inductor

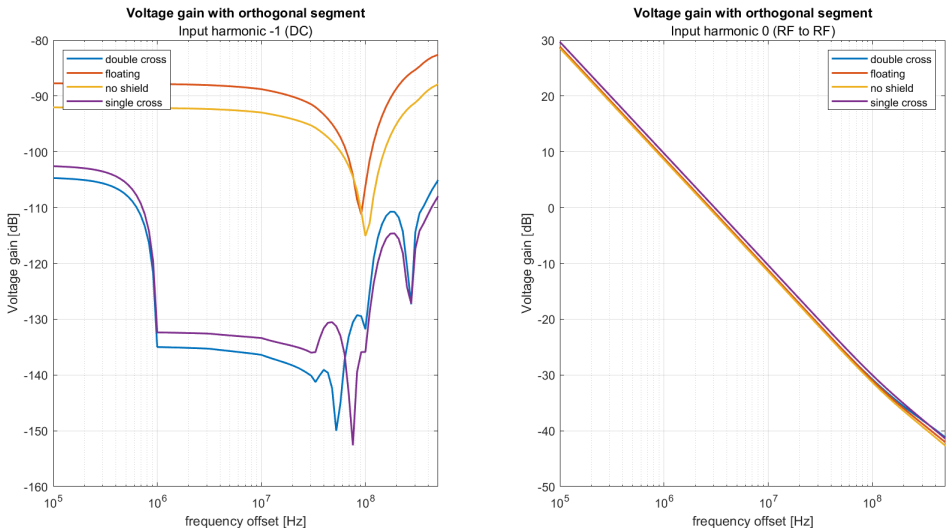

Figure 29: Voltage gain: metal strip, orthogonal to the inductor's routing

In the three figures (Fig. 27, 28, 29), three voltage gains are reported. They refer to simulations done considering as input noisy signals, three voltages across a segment in metal 5, which has a length comparable with an inductor side. In the top plot the segment is parallel to an inductor side. In the middle one the segment is in the inside the inductor covered area. The bottom one is orthogonal to an inductor's side.
Even if the floating shield makes the coupling effects indipendent in respect with the segment position (the gain is the sam ein all plots), the use of a ground connected shield is the best choice in terms of isolation at low frequencies: the gain is at least 20dB lower than the one without shield in the range $[100kHz - 100MHz]$.
In the DC-to-RF plot, the lowest gain, for the oscillator with a shielded inductor, is achieved with the floating one but, since the disturbance is in the order of mV and the output zero-peak differential voltage will be in the order of hundreds of mV, grounded shields could be used without any problems.
These results are also confirmed by the simulation of a bigger structure like a grid (Fig. 30).
Simulating a bigger structure, the difference noticed in transfer function gains between the non shielded inductor and the ground connected ones decreases but still remain at least equal to 13dB.

So, looking at all collected data, the chosen shield is the single cross connected one. In terms of coupling it is very similar to the double cross connected one, ensuring a good isolation between the inductor and the underneath structures. It also lets the inductor to achieve a higher

quality factor than the single cross one (Table 3). In terms of achieved phase noise, there isn't a significant difference with the ones obtained with the other two topologies, since it is dominated by the white noise of the two cross-coupled pairs (Table 4).

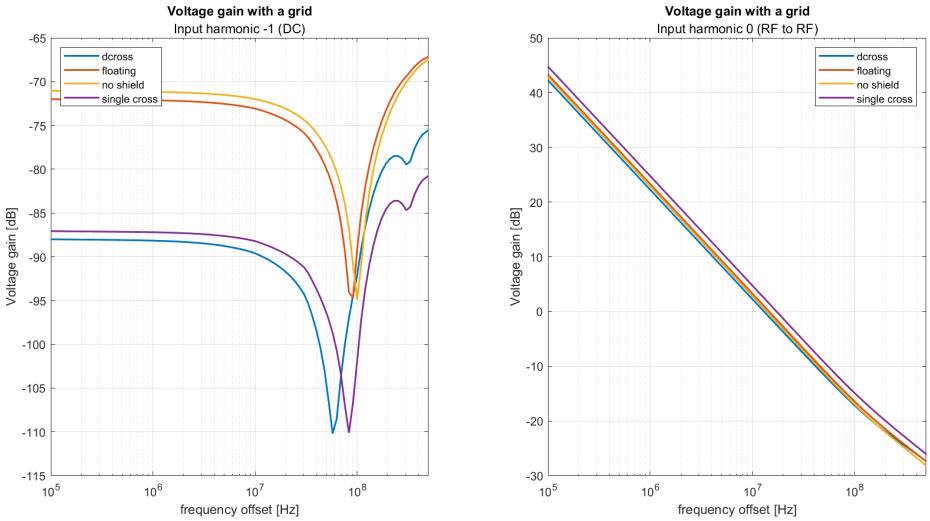

Figure 30: Voltage gain: metal grid under an inductor side

3.8 RF circuitry floorplan

After the design of all the active RF components, an analysis is done in order to understand how to organize them under the inductor's area. Simulations' results show that if the two cross-coupled pairs see the best inductor's quality factor, at least 1dBc/Hz better phase noise value (at 1MHz) is achieved at the oscillator's output pins. It means that the cross-coupled pairs have to see the shortest length of the two $15\mu m$ wider connections used to link the active RF circuits to the inductor.
So the final floorplan is composed by the two cross-coupled pairs close as possible to the output inductor's pin (which are also the circuit's output pin), then are connected the fine bank and finally the coarse bank, which is the most inner structure in the inductor's area.

Looking at Fig. 31 is now possible to visualize why the inductor is not symmetric: making the lowest horizontal inductor's side a little longer, the fine bank can fit better decreasing the empty space close to the inductor's routing, minimizing the length of the two $15m$ wide strips.

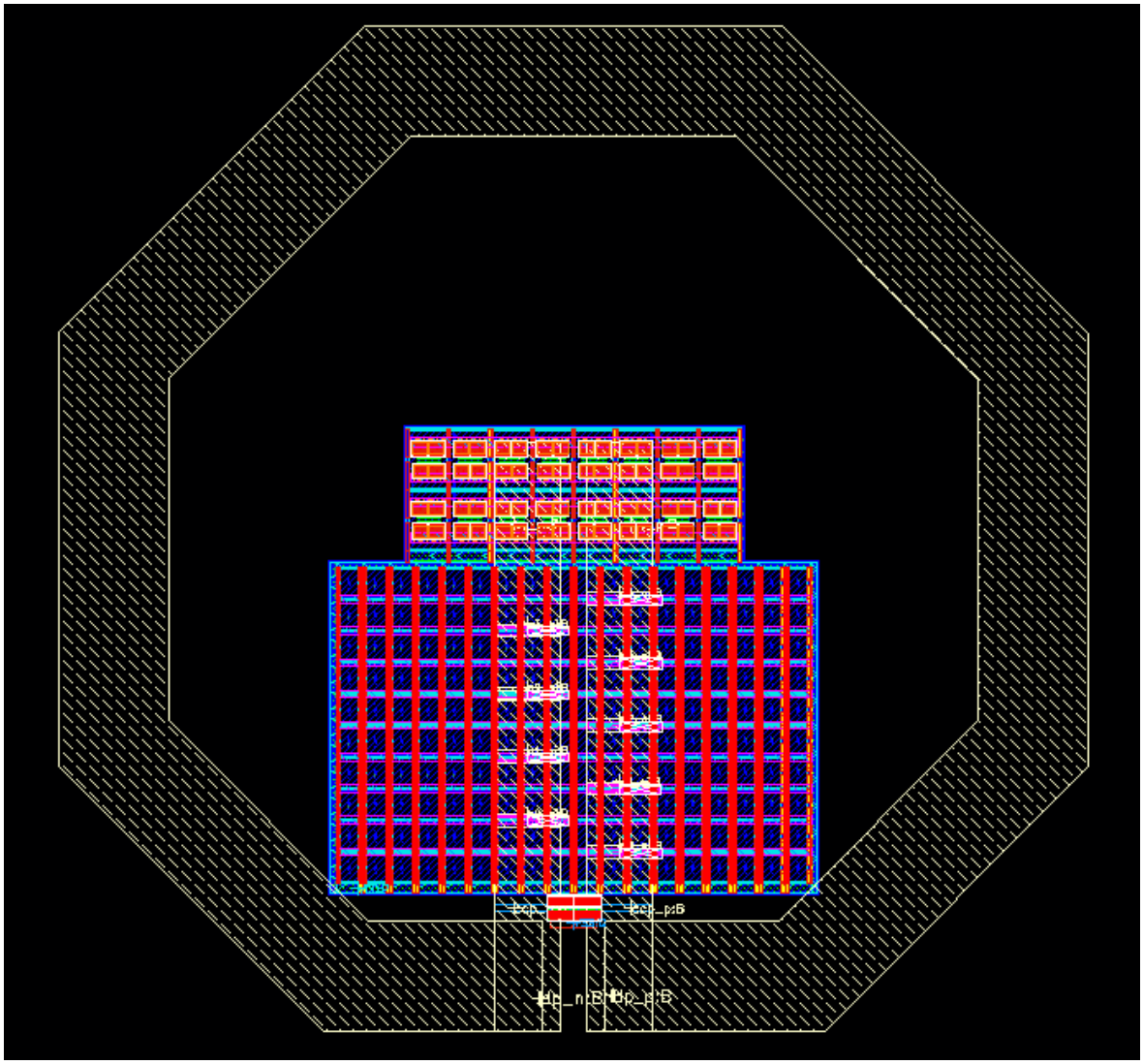

Figure 31: Floorplan layout view

4 Results

The final DCO version results about phase noise, tuning range and figures of merit are reported in this chapter.

4.1 Tuning range

After tanks design, the fine and coarse tuning ranges are checked.

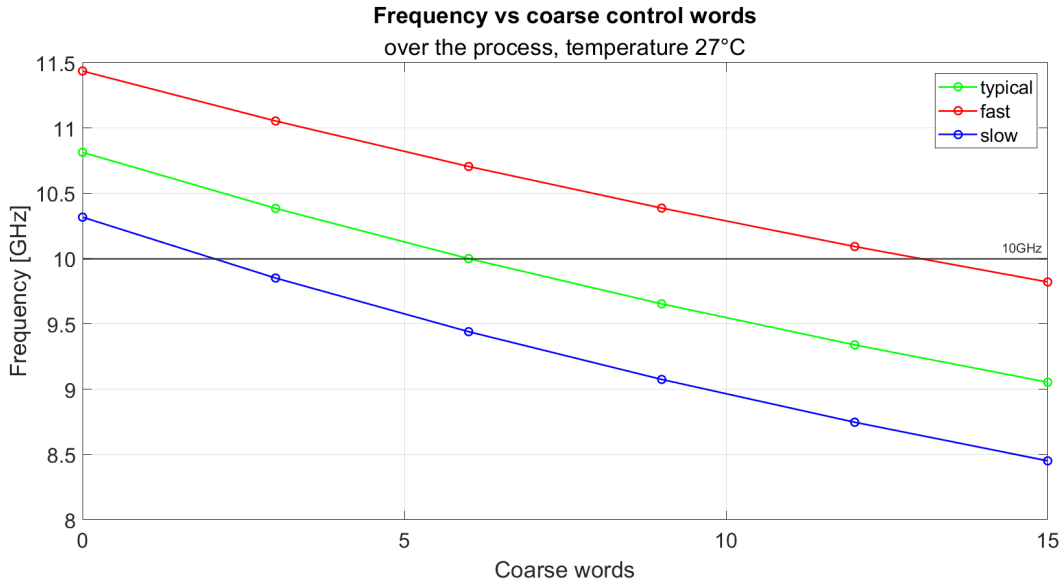

Figure 32: Coarse tuning range over process vs control words

Coarse tuning ranges at $27°C$ are equal to:

- 1.760GHz for typical process. Coarse control word= 6;
- 1.865GHz for slow process. Coarse control word= 2;
- 1.615GHz for fast process. Coarse control word= 13.

Looking at typical process, the tuning range is in specification.

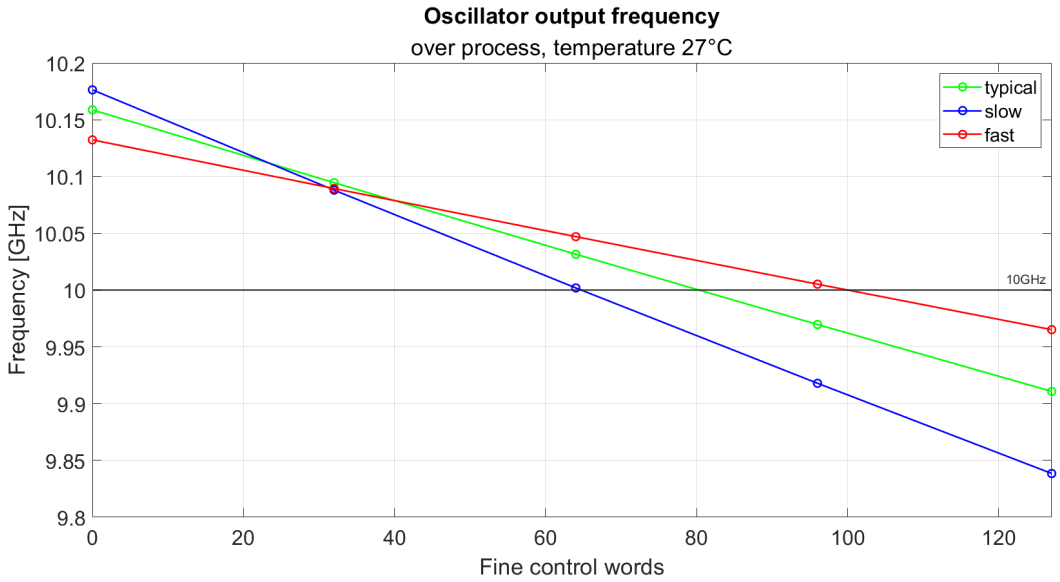

Figure 33: Fine tuning range over process vs control words

Fine tuning ranges at $27°C$ are equal to:

- 237MHz for typical process. Fine control word= 77;
- 338MHz for slow process. Fine control word= 63;
- 167MHz for fast process. Fine control word= 95.

Fine tuning range is overdesigned: for typical process at $27°C$ is equal to $237MHz$. It is 20% bigger than specification value. One of the next steps will be to redesign fine single cells to respect the LSB specification.

Simulations results show that frequency f_0 is correctly locked over process.

4.2 DC power consumption and phase noise

From theory, as shown in Fig. 19, choosing the ratio $C/L = 2.5m\Omega^{-2}$, the bias current is $I_{bias} = 1.5mA$. Until now, all the above results were obtained using this value as the biasing current. Looking at previous results reguarding the banks' and inductor's quality factors, the assumption done in theoretical calculations of a tank quality factor equal to 12 seems to be good.
Starting from:

- inductor's quality factor, considered at the cross-coupled pairs pins Q_{L_T};
- ON and OFF quality factors of the single coarse and fine banks' cells

The tank quality factor was estimated as:

$$Q_T\left(10GHz\right) = \left(\frac{1}{Q_{L_T}(10GHz)} + \frac{1}{Q_{CB,tot}(10GHz)}\right)^{-1}$$

where $Q_{CB,tot}\left(10GHz\right)$ is the quality factor of the two parallel coarse and fine banks quality factors $Q_{CB,coarse}\left(10GHz\right)$ and $Q_{CB,fine}\left(10GHz\right)$, both calculated with equation (24), when the banks are set to resonate the inductor at the output frequency f_0.

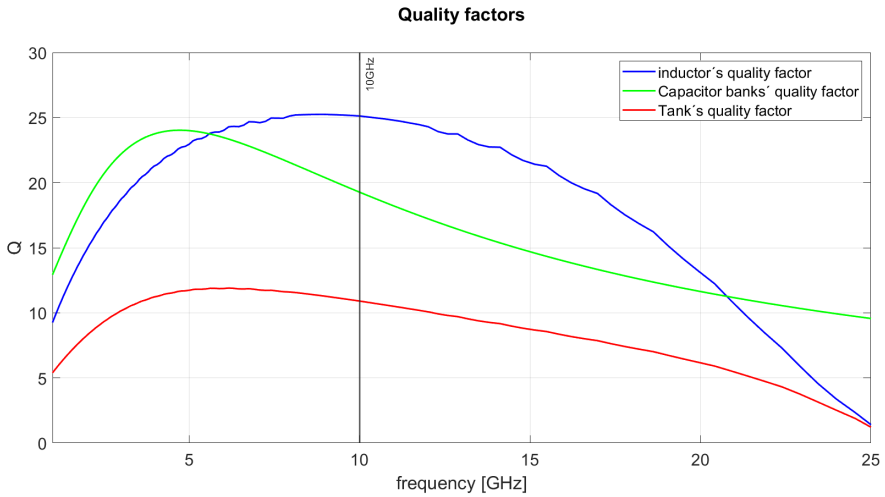

Figure 34: Inductor's quality factor (blue), equivalent tank capacitor's quality factor (green) and tank quality factor (red)

But, theoretical results in Fig. 34 have been obtained without considering that the connection between tank capacitor and inductor is not in a single point. Moreover, the DCO has to respect phase noise specification over process and over temperature. New simulations are needed to better understand how to properly bias the oscillator. The plots $\mathscr{L}(\Delta\text{f=1MHz})$ versus I_{bias} vs temperature over process are reported.

The current reference will be produced by a PTAT (proportional to absolute temperature) current source: it will ensure circuit's operations in specification for all automotive temperature range $[-50; 150]°C$ over process.

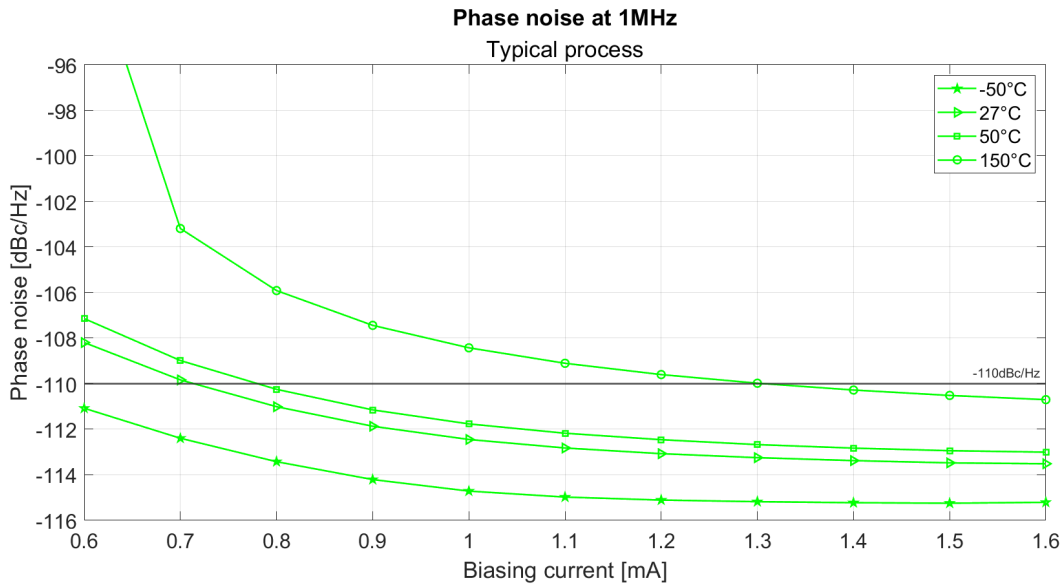

Figure 35: Phase noise at 1MHz in typical process vs biasing current

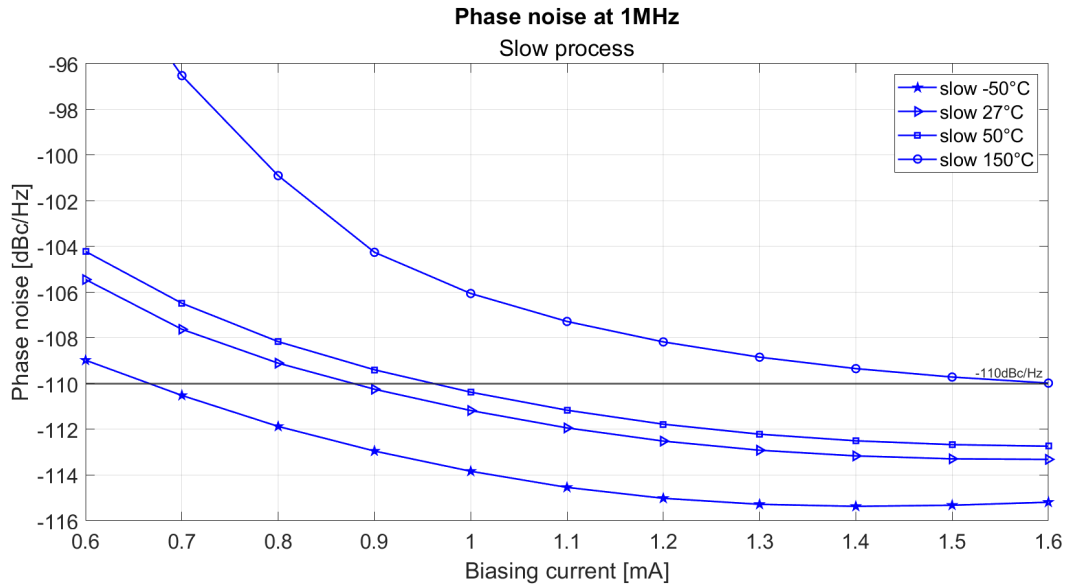

Figure 36: Phase noise at 1MHz in slow process vs biasing current

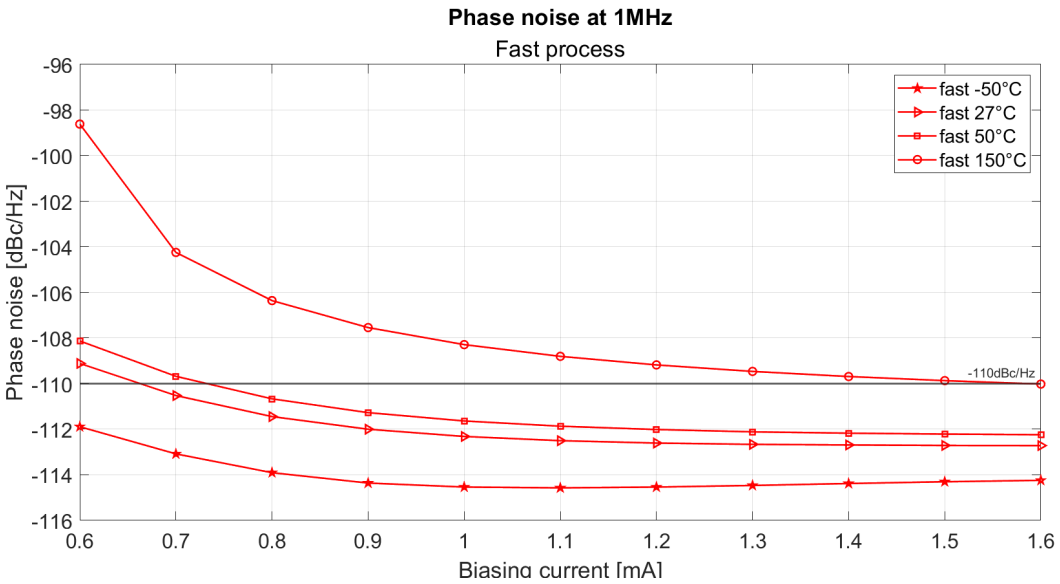

Figure 37: Phase noise at 1MHz in fast process vs biasing current

Previous plots (Fig. 35, 36, 37) show that the maximum needed current to ensure phase noise specification at 1MHz over process at $150°C$ is $I_{bias} = 1.5mA$. Moreover, this is the maximum current for which the mirror works correctly in saturation region.

The value for which the noise specification at 1MHz is respected at $27°C$ over process, with some margin, has been fixed equal to $I_{bias} = 1mA$.

4.3 Phase noise over tuning range

Phase noise, simulated at the two different frequency offsets of 100kHz and at 1MHz, versus fine control words plots are reported. In case of frequency modulation, phase noise specification has to be guaranteed all over the around the oscillation frequency $f_0 = 10GHz$.
The choice of $I_{bias} = 1mA$ is well justified by the fact that it is the minimum current value for which phase noise specification is met over process at the room temperature, $27°C$ (Fig. 39).

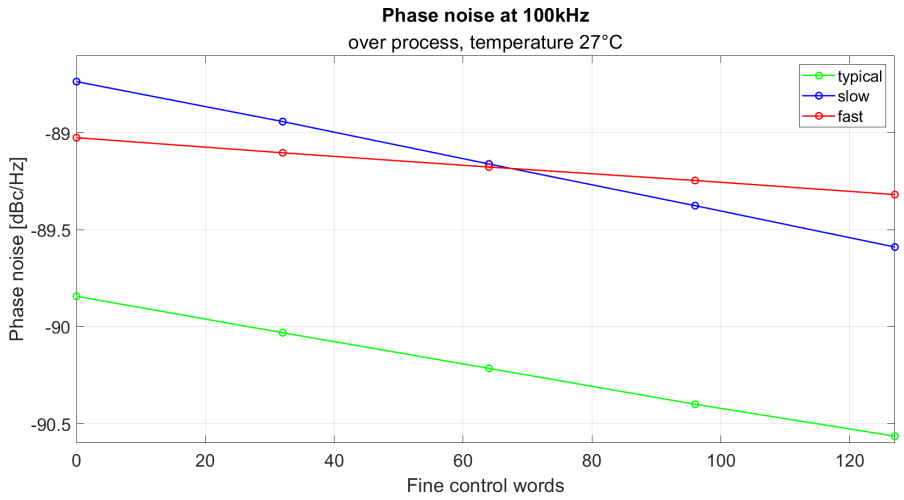

Figure 38: Phase noise at 100kHz over process vs fine control words

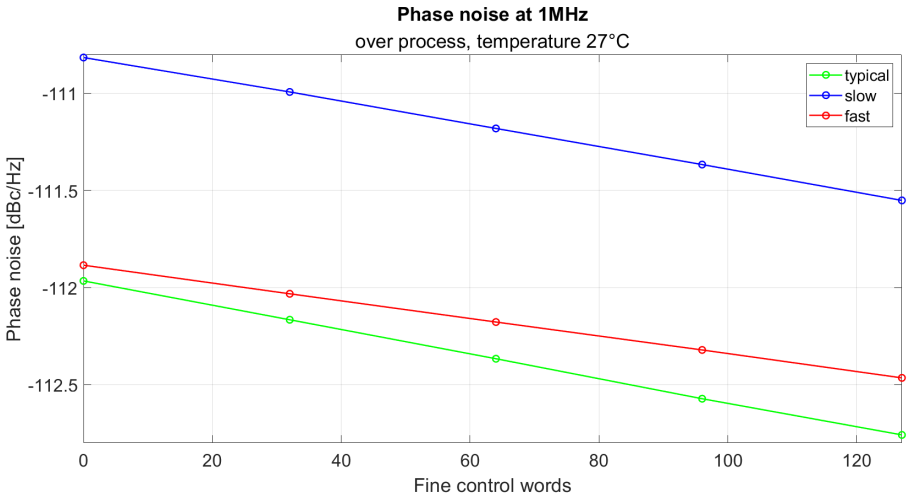

Figure 39: Phase noise at 1MHz over process vs fine control words

4.4 Figures of merit

In order to have general metrics which characterize the performance of the designed DCO, two figures of merit are then reported using data obtained in typical process at room temperature $27°C$.
The used equations are the one reported in Chapter 2 for the FOM eq.(17) and for the FOM_T eq.(18).

Metrics used for figures of merit calculations:

Oscillation frequency	$f_0 = 10GHz$
Offset frequency	$\Delta f = 1MHz$
Phase noise	$\mathscr{L}(\Delta f)$=-112.5dBc/Hz
DC power consumption	$P_{dc} = 0.9mW$
Tuning range	$TR\% = 20.4\%$

Table 5: DCO's metrics

where the tuning range is equal to the sum of the coarse and fine normalized tuning ranges $TR\% = TR_{coarse}\% + TR_{fine}\%$.

Figures of merit:

- $FOM = -192.9dBc/Hz$
- $FOM_T = -199.1dBc/Hz$

5 Conclusions and future works

A big challenge in integrated LC-based oscillators design is to realize fully-on-chip inductors with high quality factors. Reducing the number of coil turns surely decreases losses but, if the frequency is not sufficently high, the poor achieved inductance could be not sufficient to implement the tank. Another simple solution might be to enlarge the inductor size but this would cause a huge increment in the total circuit's area occupation.

This work shows that it's possible to find a trade-off in between the inductor's quality factor and the circuit's total footprint, implementing the oscillator or the entire PLL underneath a single-turn inductor. To further reduce space occupation, is also possible to add digital blocks beneath the coil, as long as a patterned shield is used to electrically isolate the inductor from other circuits: the strong uncorrelation between digital signals and oscillator's ones causes the introduction, via unwanted coupling effects, of new spectral components which are converted in additional output phase noise.

Since the previously mentioned effects have an EM nature, it's convenient to adopt solutions also to minimize magnetic coupling effects between the inductor and the underneath circuitry. That's why shield's fingers are drawn orthogonally to the inductor's sides.

A significant result is that, in terms of electrical insulation, using a patterned ground connected shield (PGS) is a better choice in respect with using pattern floating shield: PGS avoids in a more effective way unwanted coupling effects. But attention must be payed to the reduction of the inductor self-resonance frequency. If it's too low, it can degrade

significantly the inductor's quality factor and so the DCO power consumption and phase noise.

Future works

To complete this project, a full PLL will be implemented under the inductor. New simulations will be performed to estimate the ON/OFF transition time of the fine bank's cells in order to determine how fast the control block can switch them. Moreover, the fine bank's cells will be revised to fully respect the specification on the LSB, without degrading too much the ON and OFF quality factors.

Due to lack of time, the biasing circuit design was not completed: the layout will be finished ensuring its correct operation. Moreover, particular attention will be given to shield's ground connections: it's not possible to use a low resistive continuous grounded metal plate since the magnetic coupling will cause a drop in the inductor's quality factor and inductance.

Since simulations' results are only indicative and don't give complete informations on the real effectiveness of the patterned ground shield, two test chips should be carried out, comparing the circuits metrics with and without shield.

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