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Impact of Short-circuit events on Lifetime Expectancy of SiC MOSFETs

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Dedicata ai miei nonni.

Dedicated to my grandparents.

Acknowlegments

English My initial thanks I would like to dedicate to my beautiful family, who have always given me the opportunity to choose my future, make my own choices and define my own path. Thanks to mum Maria, dad Stefano and sister Eleonora. Also the present grandparents, Countess Franca, Ceciliano and the past ones, Zaira and Igino.

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Padova, 23rd April 2024 Giovanni Martello

Contents

Abstract

The following thesis is based on the ISLE project (impact of short-circuit event on lifetime expectancyof SiC Mosfet), it is born by the collaboration between the Aalborg university and the IRT Saint-Exupery.
The Silicon Carbide (SiC) is a "new" material that offers very high performance, but the lifetime of components (in this case SiC MOSFET) are not sufficient and is shorter than the Silicon (Si) counterparts. The power cycling test is the best and the main way to extract the lifetime of a component. It can be performed in AC or DC mode, in this project the focus is on the DC mode. For the components made with Silicon Carbide (SiC) the expected lifetime is not reaching the theoretical value, due to problems during the manufacturing procedure and to the not clear failure mechanisms. This project aims to find if the lifetime of a SiC MOSFET, at which a no destructive stress has been performed (in this case the stress is a short-circuit with energy below the critical value), lays between the life time of a no damage component and a damage component. The power cycling are performed in a AC machine, adapted to work in DC mode, to do that a load adaptor has been developed.

Chapter 1

Introduction

The world electric demand is continuing to grow over time. In the past 20 years the electric requests markedly increased, for they are set to slightly grow by than 2% this year (2023) [16]. Nowadays, compared to the past, there is more awareness about the source of electric energy. In fig.1.1, the renewable energies (yellow bar) markedly increased during the years, furthermore, after COVID-19 (which started in 2020 and finished in 2022), they became the most important sources of electricity in Europe, while the coal (light blue bar), gas (dark blue bar), nuclear (light green) and other non-renewable (dark green) significantly dipped. [16] The

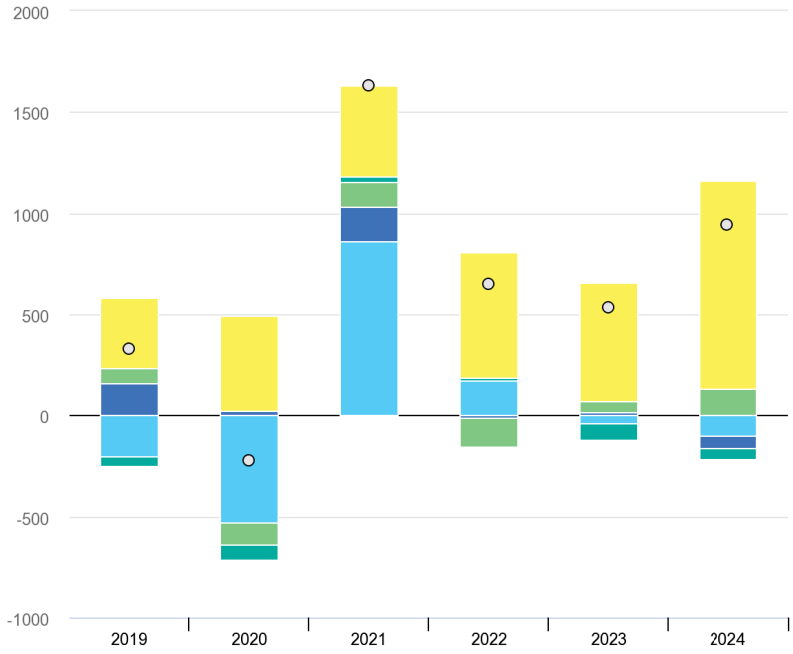


Figure 1.1: Year-on-year global change in electricity generation by source, 2019-2024. Legend: the renewable energies (yellow bar), coal (light blue bar), gas (dark blue bar), nuclear (light green) and other non-renewable (dark green). [16]

graph 1.1 of the article [16] shows that the global trend is moving into a more eco-friendly position, and here the task of power electronics starts; new power devices will lead not only to enormous energy savings but also to conservation of

fossil fuels and reduced environmental pollution. Eco-friendly means also to not waste energy, thus to be more efficient. Electric energy is regulated and converted, so that the power can be supplied to the loads in the best form; in general, the efficiency of power electronics is limited by the performance of semiconductor devices, capacitors, inductors and packaging. The power electronics (PE) is based on a material that could be considered "the father of the modern electronic": the Silicon. However, nowadays new materials that have even better characteristics than the Silicon have been studied.
The new studied materials for PE are: SiC (Silicon Carbide) and GaN (Gallium nitride).
The initial studies for this types of material have stared in the twentieth century [21], and are still continuing nowadays; compound semiconductors have established unique positions in PE applications where Si devices cannot exhibit good performance because of the inherent material properties. These devices will also find applications in efficient high-voltage DC power transmission lines, while for automotive applications the use of new materials will considerably reduce electricity loss during vehicle operation.
The first electronics components created with SiC have been released in the early 1990s [21] and then the first commercial diode based on this new material has been commercialised in 2001 [13]. A very intuitive graph that allows to understand the developing of the SiC over the years is reported in fig. 1.2. Before 2006 the

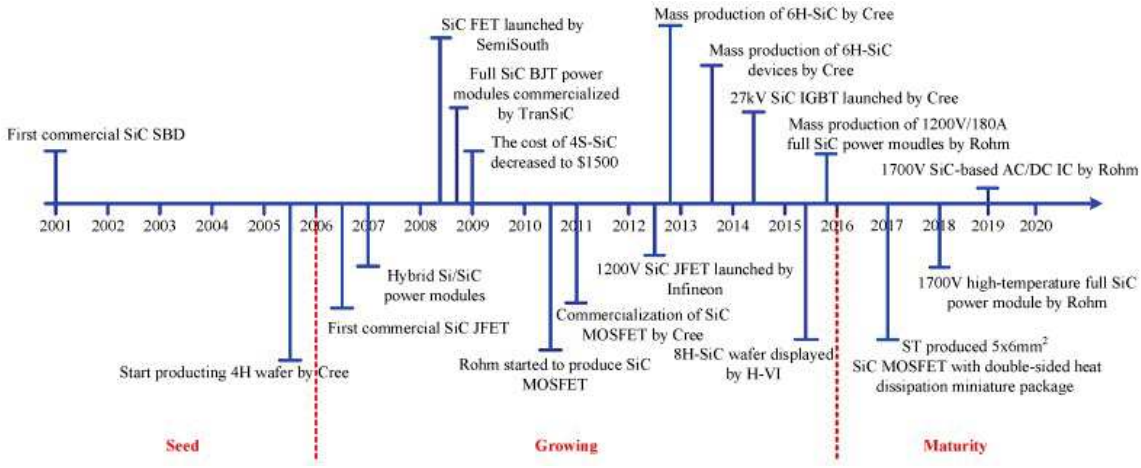


Figure 1.2: The milestones of the development process of SiC power electronic devices. [13].

technology wasn't ready to provide a very reliable and functional component made of SiC, but throughout the years the quality and the study increased to allow a good development of new components.Between 2006 and 2016, SiC technology started to grow significantly and successful results were obtained. After 2016, SiC technology was considered ready and mature [13]. The market value of SiC in 2022 was equal to 843.9 USD millions [17] and it is expected to continue growing in the next years, with a exponential trend, as shown in fig. 1.3. Furthermore, in 1.3 are reported two different categories of SiC: the green and the black SiC;

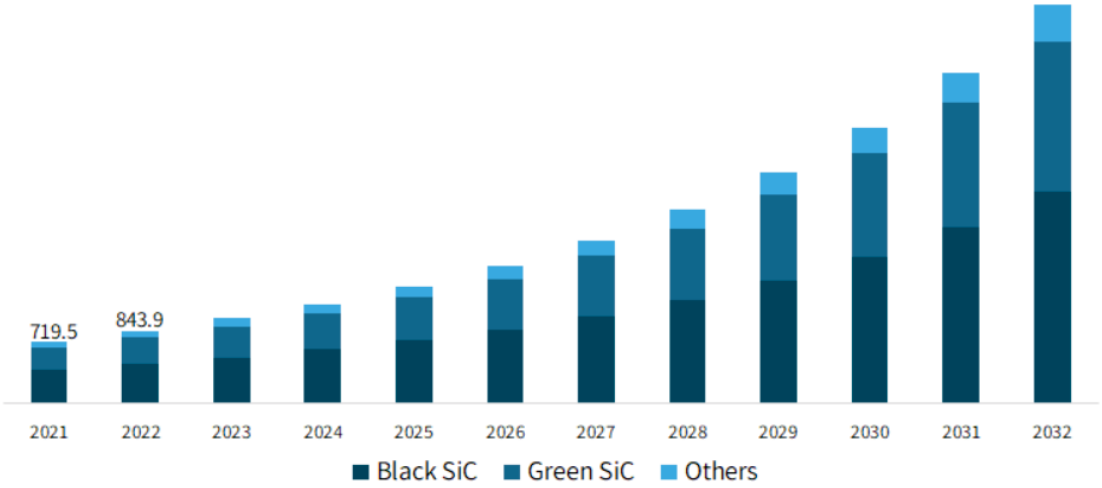


Figure 1.3: Global silicon carbide market size [Millions of USD] and its forecasted . [17].

green silicon carbide is basically the same as black silicon carbide, only the raw material and manufacturing process are different, the green product is translucent, hardness and purity is better than black silicon carbide [17].

To allow a better interpretation about the quality and differences between Si and SiC, in fig.1.4 are reported few of the most important parameters that show those differences. As can be seen all the characteristics are much higher in SiC compared to Si, an important aspect that deserves a small focus is the thermal conductivity ($\frac{W}{cmC^{\circ}}$); the high value of this parameter (even more than GaN thermal conductivity [24]) indicates that the SiC devices are the perfect subjects to handle high power because they are able to conduce in most efficient way the heat power; in addition, a related parameter is the junction temperature, which will be lower and therefore less subject to thermal stress. [11].

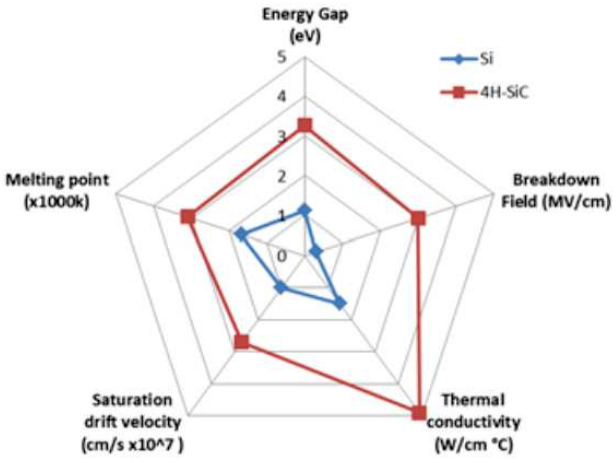


Figure 1.4: Comparison between Si and SiC material, based on their characteristic [28].

The future of electronics will be based on new materials (SiC and GaN), which, as it has been said, they have better characteristics compared to the "old" material (Si). Taking into account the world trend that is moving towards being more eco-friendly, the life-time of the components has a crucial role into this aspect, just think of how many electronic components are present in every devices and a component failure can lead to the device being discarded. Thus developing a more reliable electronics allow to produce less wastes, therefore important aspect that has to be taken into account is the reliability of these new components made with compound materials. The devices made by Si are well-known and their failure mechanisms as well, thus the knowledge of them also in the SiC and GaN devices, must to be examined in depth to guarantee the expected performance and their theoretical life-time[2] .
The goal of the electronics of the future is to be able to unleash the enormous potential that new materials hold for the world.

1.1 Purpose of the ISLE Project

The purpose of this project is investigate the impact of Short-circuit events on Lifetime Expectancy of SiC MOSFETs, it is a ECPE (European Center for Power Electronics) project. The AAU University will collaborate with IRT Saint Exupéry, Technological Research Institute (Toulouse University). The project aim to investigate the effect of SC on the SiC Mosfet life-time. From previous studies has been seen [6] that there is a so-called critical energy (E_{CRIT}) where the device under test is irreversibly damaged. In the past many other tests at reduced durations (Design-of-experiment approach) has been performed to investigate at which percentage of E_{CRIT} there is an observable drift of measurable parameters. Some results found by IRT are:

- V_{TH} does not change up 50%E_{CRIT}.
- I_{gss} does not change up to 90%E_{CRIT}.

However, some aspects of SiC Mosfet behaviour have lacks of knowledge about

1. Whether a device subject to a short-circuit event below 100%E_{CRIT}, i.e., damaged but still complaining with specs, reaches anyway up to the same expected life.
2. Whether a device subject to a short-circuit event below50%E_{CRIT}, i.e., with no detectable damage on any of the measurable device parameters, reaches anyway up to the same expected life.

The selected components are provided by *STmicroelectronics*, and the component is a 1200 V, 30 A SiC Mosfet, having a static typical drain-source on-resistance equal to 64 mΩ: **SCT070W120G3AG**.
Initially, the SC time-to-failure ($t_{SC_{Failure}}$) is investigated and the critical energy (E_{CRIT}) identified for the given part number. Tests is performed in the range of

50% to 70% blocking voltage. Afterward, three batches will be prepared. The samples belonging to the first one will not be subject to short circuit. The samples belonging to the second one will be subject to repetitive short circuit at damaged conditions (point 1 above) and, finally, the ones belonging to the third one will be subject to repetitive short circuit at no detectable damage conditions (point 2 above).

Next step will be to power-cycle the samples belonging to the three batches above. Although a Coffin-Manson relationship would be nice to have, we are aware that this would take a non-reasonable amount of time to be achieved. For this reason, we hereby propose to use only one temperature-swing point ΔT, which could be representative of the expected trend (see figure 1.5). Thereby, we will likely use 80 K as the temperature swing and $T_J^{MAX} = 150\,°C$ maximum junction temperature.

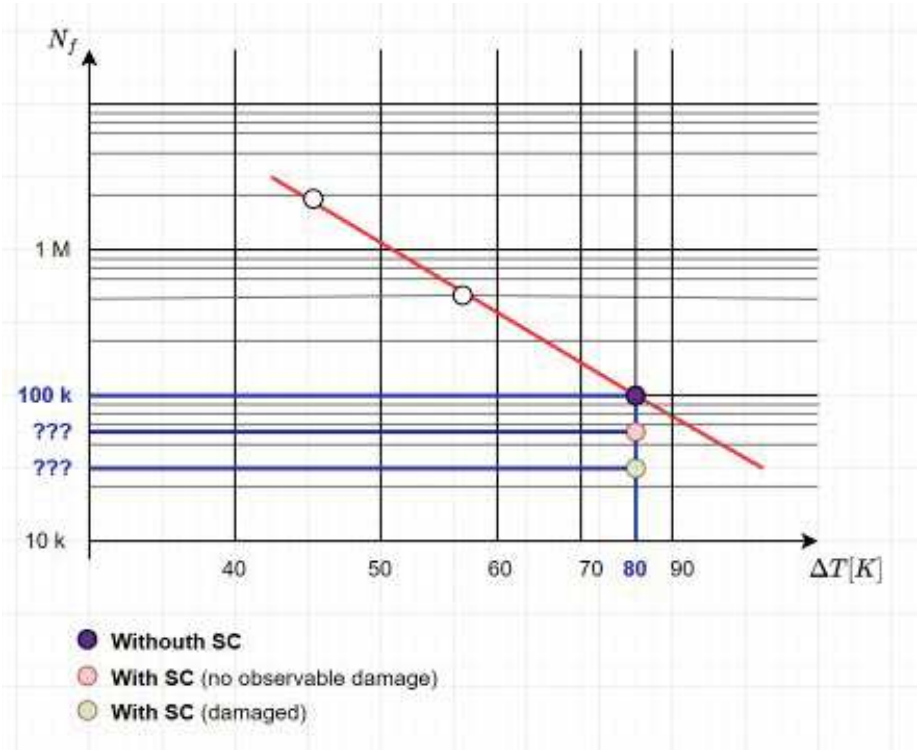


Figure 1.5: Expected results of the study case expressed in number of failure over temperature difference.

In fig. 1.6 is showed the expected results. in terms of $V_{DS_{ON}}$ degradation during power-cycling tests.

The procedure tasks of this project are the following: 1)IRT Saint-Exupery is in charge of the short-circuit tests and post-failure analyses; 2) AAU is in charge of the power-cycling testing [22]; 3) Electrical characterizations are considered by both research units.

Final step is extrapolate a law to correlate the number of cycles and the SC energy.

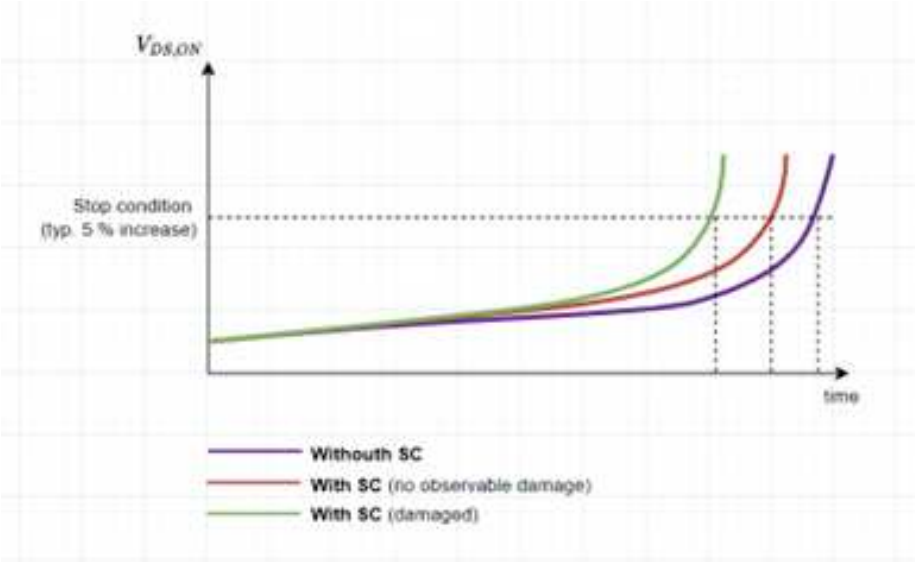


Figure 1.6: Expected results in terms of $V_{DS_{ON}}$ degradation during power-cycling.

1.2 Limitations

The power cycling (PC) test takes a lot of time to be performed; the expected time for the culmination of the ISLE project, in the case there are no issues or delays due to the availability of both universities, is almost 1 year. Therefore in the following thesis has been addressed just some parts of it and as reported in the previous point, Aalborg University is in charge to perform the power cycling step. Furthermore, during the analysis particular attention should be paid to distinguishing between the effects of V_{th} increase and the one related to metallization degradation; then the stress tests will be conducted on a substantial number of samples for each family, this due the mismatching of the component parameters introduced during the manufacturer process. Another aspect that should be taken into account is the lack of availability of the equipment used to perform the power cycling, the dedicated machines used for it in AAU are the Mentor Graphics. This has led some delays in the developing of the project and to overcome this problem a pre-existing AC power cycling machine has been adapted to work in DC mode. For that reason, the final result of the thesis does not present any results on power cycling.

1.3 Thesis Outline

To summarize, the points addressed in this master thesis work follow. The thesis consist in four parts:

1. An overview about SiC's Technology and about the physical parameters of the material and of components created with it. Furthermore, a focus about some of the parameters that characterise the components is needed to figure out who are more interesting for our analysis.

2. The characterisation procedure to extrapolate the parameters responses of the components, to do that a dedicated equipment will be used, it is the Keysight B1505A.

3. Explanation about Power Cycling, which are the parameters sampled and how.

4. Final consideration regarding the results.

Chapter 2

SiC Technology

Silicon is used and it has been used in very wide number of applications, but due its characteristics has a quite important limitations, thus in past new materials have been studied. The component made with new material, like SiC and GaN, are defined as high electron mobility transistors (HEMT) due to their capability to allow a higher velocity for electrons that pass through them. To give an simple example of the incredible advantages that these new materials can bring into the electronic world, is reported in [30] an example of application. As reported in article [30], if a withstand voltage of 5000V is to be obtained, the Si power device with a substrate material doped with $2.5 \times 10^{13}\,\mathrm{cm}^{-}3$ requires a drift layer thickness of 0.5 mm and an area resistance of $10\,\frac{\Omega}{\mathrm{cm}^2}$, while the SiC MOSFET with a drift layer doped with a concentration of $2 \times 10^{15}\,\mathrm{cm}^{-}3$ only requires a thickness of 0.05 mm and an area resistance of $0.02\,\frac{\Omega}{\mathrm{cm}^2}$. SiC power devices allow the use of thinner drift regions to maintain higher blocking voltages, significantly reducing forward voltage drop and conduction losses.

To figure-out which material between Si and SiC is the best for the power application in table 2.1 are listed some physical & electric parameters, with a carrier density equal to $10 \times 10^{16}\,\mathrm{cm}^{-3}$ at room temperature. Since the saturated drift velocity of electrons in 4H-SiC is twice the value of Si, SiC devices are able to reach higher switching speeds with lower power dissipated. One more aspect to takes into account is the internal breakdown field, in tab 2.1 can be seen that

Physical characteristic	Si	4H-SiC
Bandgap energy (eV)	1.12	3.26
Breakdown field parallel to *c-axis* (MV/cm)	0.3	2.8
Electron mobility parallel to *c-axis* at 300 K ($cm^2/V \times$ sec)	1000	1200
Relative dielectric constant	11.8	10
Thermal conductivity ($W/cm \times K$)	1.4–1.5	3.3–4.9
Electron Saturated Drift Velocity ($10 \times 10^7\,\mathrm{cm/s}$)	1	2.2

Table 2.1: Overview of the material properties of Si and 4H-SiC.[21] [7]

the breakdown field in 4H-SiC is three times higher than Si, that means the dimension of the chip could be smaller and it allows to operate at higher voltages. A correlated aspect to high breakdown electric field inside the SiC components is the reliability of the oxide. SiC based devices have a native insulator, as well as the Si components, the silicon dioxide (SiO_2). It is an amorphous material used in microsystems as a dielectric to isolate various electronic elements. Thin films of oxide are easily grown or deposited on silicon wafers using a variety of techniques[23].
Up to now a quick overview about the relevant parameters have been accounted, now a brief focus on what are the real qualities that bring SiC to the top of the market is needed. SiC is an exceptional wide bandgap semiconductor, in the sense that control of both n- and p-type doping over a wide range is relatively easy. As is listed in tab. 2.1 4H-SiC has a very high bandgap value, just to be precise the band gap is the distance expressed in eV from the conduction band to valance band, the effective densities of states in the conduction band N_C and valence band N_V can be calculated and for this material at room temperature they are $1.8 \times 10^{19}\,\mathrm{cm}^{-3}$ and $2.1 \times 10^{19}\,\mathrm{cm}^{-3}$, respectively. These two values are important as they allow to estimate whether the material will be degenerate when heavy impurity doping is performed. Knowing these two parameter the intrinsic carrier concentration can be extracted by eq. 2.1.

$$ni = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \tag{2.1}$$

At room temperature its value is $5 \times 10^{-9}\,\mathrm{cm}^{-3}$ (for the silicon the intrinsic concentration is $1 \times 10^{10}\,\mathrm{cm}^{-3}$), this result is due the larger band gap. This is the main reason why SiC electronic devices can operate at high temperatures with low leakage current [21].
Another important parameter is the *mobility*, the formulas used to calculate the values for electrons and holes mobility in 4H-SiC is reported in eq. 2.2 and 2.3.

$$\mu_{e^-} = \frac{1020}{1 + \left(\frac{N_A + N_D}{1.8E17}\right)^{0.6}} \tag{2.2}$$

$$\mu_{h^+} = \frac{118}{1 + \left(\frac{N_A + N_D}{2.2E18}\right)^{0.7}} \tag{2.3}$$

Along the c-axis in the crystallographic structure of the 4H-SiC, the mobility for electrons is approximately $1200\,\frac{\mathrm{cm}^2}{\mathrm{V}\times\mathrm{sec}}$ and for the holes is $120\,\frac{\mathrm{cm}^2}{\mathrm{V}\times\mathrm{sec}}$ at room temperature, this is one of the major reasons why 4H-SiC is the most attractive polytype for vertical power devices fabricated on SiC[0001] wafers. At high temperature, the doping dependence of mobility becomes small, because the influence of impurity scattering decreases. In general, the temperature dependence of mobility is discussed by using a relationship of $\mu \sim T^{-n}$ [21].
A further parameter that markedly bring SiC as the most suitable compound material to produce power electronic components is the *Breakdown electric field*.

At the moment when a very high electric field is applied to a p-n junction or Schottky barrier in the reverse-bias, the leakage current increases generating electron–hole pairs and the junction ultimately breaks down. Exist two different braking mechanism and they occur in two distinct situations, one is the *avalanche breakdown* and the second is the *tunnelling breakdown*. The breakdown field for 4H-SiC is 2.8 MV/cm which is approximately nine times bigger than the breakdown field of Si 0.3 MV/cm, at the same value of doping. Into a junction with a lightly-doped region, avalanche breakdown is predominant, this is the case for most power devices[1]. In his case the carriers can gain enough energy to excite electron hole pairs and the generation of e/h pairs is multiplied inside the space charge region of a junction, this condition can lead to breakdown. The critical voltage that cause the breakdown in a Schottky barrier diodes or a one side p-n junction is expressed by eq.2.4.

$$V_B = \frac{E_B X_{BD}}{2} = \frac{\epsilon_{sic} E_B^2}{2qN_D} \tag{2.4}$$

Where E_B is the critical electric filed straight, ϵ_s is the dielectric constant of the material, q is the charge of electron in free space and the N_D is the concentration of the impurities (donor concentration) introduced into the semiconductor. Moreover, for a given V_B, SiC power devices could be made thinner than the Si devices. The minimum width of the Drift (W) region is in general limited by the need to contain the entire depletion region which extends with the applied blocking voltage[1]. When the doping density is increased, the width of the space-charge region becomes small and the distance for carriers to be accelerated becomes short. Furthermore, the mobility is reduced in highly doped materials because of enhanced impurity scattering. These are the reasons why the critical electric field strength apparently increases with increasing doping. From the literature can be seen that this characteristic of hexagonal SiC polytypes is the main reason why SiC is very attractive for power device applications [21].
Owing to the high critical field strength and high electron mobility along the c-axis, 4H-SiC exhibits a significantly higher qualities and properties than other SiC polytypes. This is a another reason why 4H-SiC has been almost exclusively employed for power device applications.
A parameter that is sure to be reported is the *Thermal Conductivity*, that indicates how fast is the rate of transfer of heat generated inside the component. This parameter in 4H-SiC is almost three times larger than Si, so for power components it is so relevant and it's understandable why SiC is used to produce power devices, because having higher thermal conductivity value enables a reduction of the thermal resistance of the semiconductor device, that means a larger capability to handle with high current and high voltage without entering dangerous operating zones. Just to clarify the role of this parameter a graph that describes the relation between the thermal conductivity and the temperature of the component is reported in figure 2.1.

The thermal conductivity has a inverse correlation with the temperature, then when the junction temperature increases the rate of transfer of heat generated

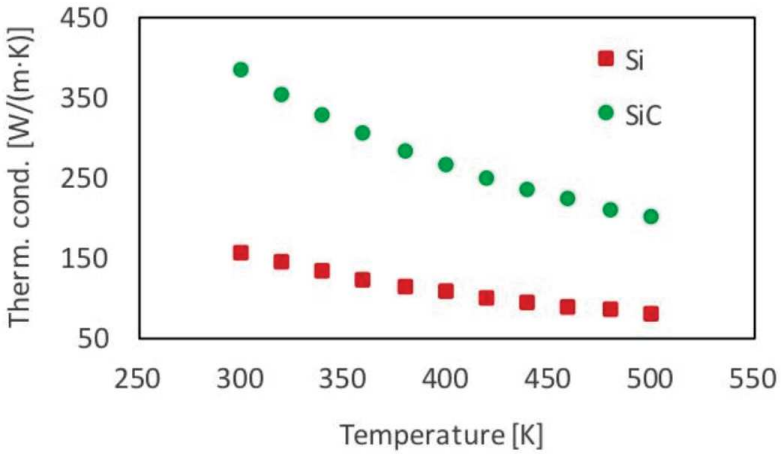


Figure 2.1: Thermal dependence between the thermal conductivity and the temperature of the MOSFET. The graph has been taken by [30].

inside the component dips. Then the MOSFET are not longer able to cool down as when the temperature is low.

Another important parameter that can be addressed to describe better the silicon carbide as new material, or better, as better material compared to silicon, is the on-resistance. The value of the specific R_{DS} in the drift region is expressed from the equation 2.5 and it has been taken from the literature [21].

$$R_{ON,SP} = \frac{4V_B^2}{\mu_N \epsilon_{sic} E_C^3} \tag{2.5}$$

The equation explain very well that the specific on-resistance increases as the square of the desired blocking voltage V_B, and is inversely proportional to the cube of the critical field E_C. Since the critical field in 4H-SiC is almost an order-of-magnitude higher than in silicon, the on-resistance for a given blocking voltage will be almost 1000 times lower. This accounts for the great interest in developing power devices in this material [30]. Then to show in more clear way a graph that describes the relation between the on-resistance $R_{ON,SP}$ and the blocking voltage V_B is reported in figure 2.2 .

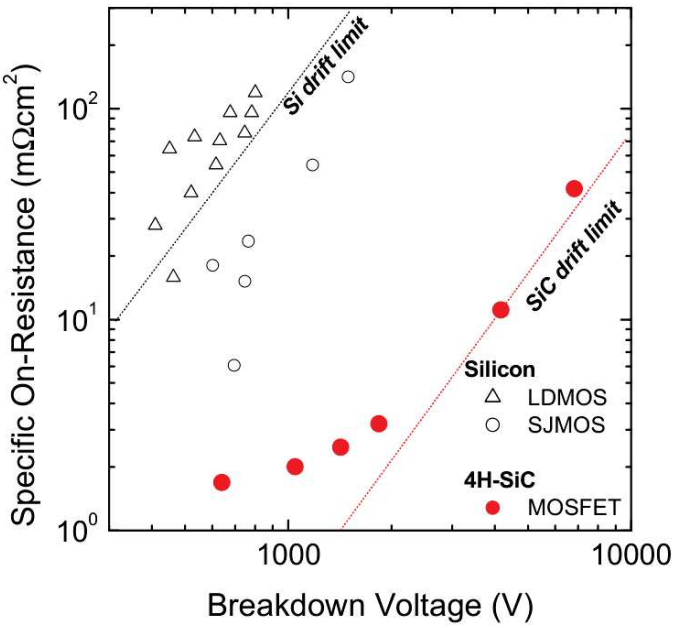


Figure 2.2: Comparison of specific on-resistance in the drift region as a function of the breakdown voltage breakdown voltage (V_B) for Si and 4H-SiC power MOSFET. The solid lines are the theoretical unipolar limit [10].

2.1 Structure of MOSFET and developing

During the years even more typologies of MOSFET have been developed, in fig. 2.4 is shown the base structure of a n-MOSFET based on SiC (to be precise, the base structure of a Si mosfet is the same). The entire structure is grounded on a SiC substrate layer which has been doped by elements belonging to the third group, they have just three valence electrons (Silicon and silicon carbide atoms have 4 valence electrons), thus the introduction of these elements into the crystal reticle of SiC creates free spaces, they are called holes, in which electrons can go and stand there. Instead the parts indicated with n are created introducing into the SiC crystals elements belonging to the fifth group, they have 5 valence electrons. To resume, the conduction of a current in p doped area is related to the movement of the holes, instead in a n doped area the current is created from the movement of electrons (electrons in this type of mosfet are the majority carriers). The majority carriers are the most relevant causes for the current in a mosfet components [21]. The base structure of a planar MOSFET is reported in fig.2.4, as can be seen three terminals are present (plus one that is put equal to reference ground): Gate, Source and Drain. Appling well-known levels of voltage between these terminals a current is allowed to pass through the component, or better a depletion region is formed and after that an inversion layer can be created between the drain and source, it allows a current to flow.

In this chapter and in this work the goal is not to address the differences between the structures of different mosfet typologies and their functionality but a

small overview is needed to show the advantaged and the differences between the normal structure of the mosfet and the power mosfet. As said above, applying the correct value of voltage between the pins, the component can be controlled to perform and behave in different mode. Exist three district main working area for the mosfet, the linear, saturation and off region. They are extractable and capable from the characteristic curve that link I_D over V_{DS}, un example for that is reported in fig.2.3.

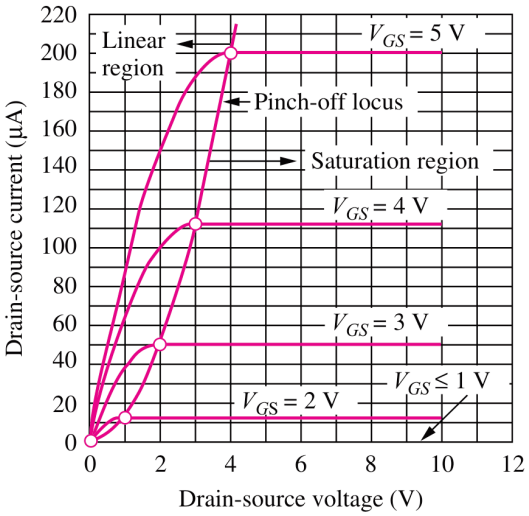


Figure 2.3: I_D over V_{DS} characteristic of a generic ideal Mosfet, in which are reported the interesting areas. [3]

During the year companies developed new structure of for the MOSFET to achieve even better characteristics than before; for the SiC power mosfet, as it has been reported above, the preferable conduction direction is along the c-axis, so the configuration of the components are changed. The n+ drainage area is no longer on the upper surface and the current exits the inversion channel and flows first horizontally and then vertically through the lightly doped n-drainage region to the n+ substrate, which acts as the drain terminal. As shown in fig.2.5 two main structure has been developed, the planar one and trench one, but they are known as DMOSFET and UMOSFET, respectively. DMOSFET because the n+ source and p base regions are formed by diffusion of n-type and p-type impurities through the same mask opening, whereas the UMOSFET derives from the U-shaped geometry. The power mosfet incorporates the basic mosfet structure on a thick, lightly-doped n-type epilayer on an n+ substrate. And as can be seen in figure 2.5, the blocking voltage in the off state of the MOSFET is supported by the reverse biased junction between the MOS capacitor formed by the gate and the drift region, but it is also supported by the base and the drift region. Then, taking in consideration the structure of the DMOSFET in figure 2.5a, the electric field along vertical cross-sections taken through the pn junction and the MOS capacitor.

Considering the electric field in the semiconductor, since the silicon carbide has a bigger dielectric constant compared to the silicon (not that bigger), the electric

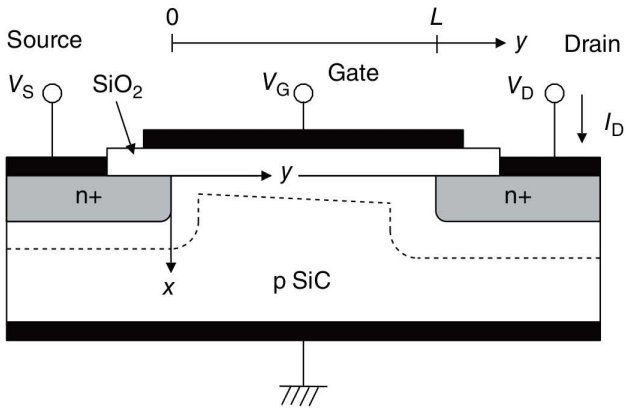
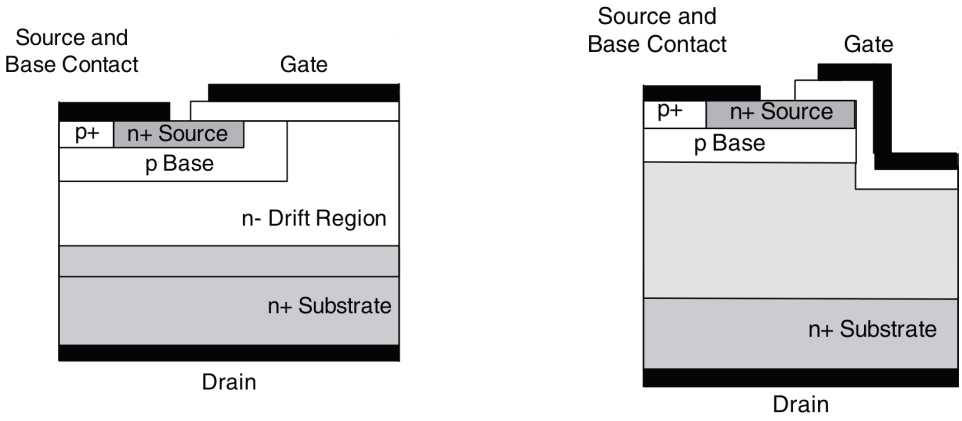


Figure 2.4: Planar SiC MOSFET with n-channel. [21]



(a) Double-diffused SiC MOSFET structure.

(b) Trench SiC MOSFET structure.

Figure 2.5: Two different structure of a power SiC mosfet [21].

filed inside the dioxide of silicon, the insulator, can be calculated by the equation 2.6.

$$E_{OX}\epsilon_{OX} = E_{SiC}\epsilon_{SiC} \tag{2.6}$$

Doing the calculation the electric field inside the insulator can be ~ 2.5 times larger than the field in the semiconductor. Furthermore, analysing the critical electric field in the oxide, its maximum value is $10\,\mathrm{MVcm}^{-1}$ [21], but to ensure a longer lifetime for a component it is limited to $4\,\mathrm{MVcm}^{-1}$; taking in mind that the electric field in the semiconductor is right below the limits. To do an example, if the electric file on the interface with the oxide is around $0.3\,\mathrm{MVcm}^{-1}$, the filed inside the dielectric material is equal to $0.75\,\mathrm{MVcm}^{-1}$, then right below the limits reported before.

As can be seen in the figure 2.5, the necessity to find another structure for a MOSFET is linked to research a component which has maximized performance and this can be done involving trade-offs between parameters. To simplify the

approach, researchers have developed figures of merit (FOMs) that define the theoretical envelope of maximum performance and quantify the degree to which actual devices approach these theoretical limits. In a power component, to be precise in a unipolar power component a useful figure of merit is the product between the blocking voltage and the current during the on-state, the starting point is reported in the equation 2.7.

$$FOM = V_B \times I_{ON} \tag{2.7}$$

The maximum allowable power dissipation is determined by the thermal capability of the package, the maximum allowable junction temperature of the device and other parameter [21], then the figure of merit reported above can be rewritten in the equation 2.8

$$FOM = A\sqrt{P_{MAX}\left(\frac{V_B^2}{R_{ON_{SP}}}\right)} \tag{2.8}$$

Where A is the area of the device and it is limited by material quality and the technological level of manufacturing. Moreover, using a package with a lower thermal resistance would increase the FOM, this is due the maximum power limitation that comes from the thermal capability fo the package. Furthermore, the final argument on 2.8 is the ration $\frac{V_B^2}{R_{ON_{SP}}}$ that is called unipolar device FOM and the goal is to maximize that ratio. Then reduce the drift resistance and increase the blocking voltage [21]. But it is important to bear in mind that the blocking voltage V_B may be limited by an oxide field that exceeds the limit for satisfactory oxide reliability. Then to reduce the resistance some innovation have been adopted in the new structure of DMOSFET, figure 2.5a, but this is not the case to explain them. But for example the new structure called UMOSFET, figure 2.5b, present opportunities such as the possibility to create the same component in a smaller chip and to form a short-channel [21].

2.2 Physical & Electric Parameters of a SiC Mosfet

A focus to the most important parameters of SiC Mosfet is needed to figure out better which are the most significant for this study cases and also in a general one, because the pertinent physical and electric quantities analysed during the characterization, or during a study case, of a component are basically the same; however sometimes some parameters are more important than other.
To understand the quality of a component exist a very wide range of parameters, that, as been said above, allow to extrapolate the functionality characteristic: below a list of electrical and physic parameters are reported:

- R_{DS}: The resistance seen between the Drain and the source.
- V_{TH}: The threshold voltage correspond to the gate-source voltage at which a significant drain current starts to flow.

- $V_{DS_{ON}}$&$V_{DS_{OFF}}$: The drain-source voltage is the potential difference measured between the drain and the source pins.
- S_iC/S_iO_2 *Defects*: The interface between the semiconductor and the insulator can have some defects that modify the functionality of the component.
- *Junction Temperature*: The T_J is the junction temperature of the SiC die.
- *Gate oxide Reliability*: The reliability of the gate oxide is related the manufactured quality of the insulator layer inside the component.

In order to provide a broader overview of the effects that each of these parameters can have during the operation of a SiC Mosfet, a brief description of each is needed. Thus below has been reported, for each item cited above, a description about its behaviour in a SiC Mosfet.

R_{DS} : The resistance seen between the drain and the source in a MOSFET is the union of few small resistance that are present inside the semiconductor chip and also the resistance of the connection from the chip to the case (in some cases this resistances are neglected because very small). The n+ drain is no longer at the surface and instead the current exits the inversion channel and flows vertically through the lightly-doped n-drift region to the n+ substrate, which acts as the drain terminal. Consequently, the on-resistance of the power MOSFET is the sum of the on resistance of the fet channel plus the on-resistance of the drain drift region and the substrate. As reported before exist two main topologies of power MOSFET, the planar (or double diffusion) and the trench configuration. This difference implies that there will be some differences between the R_{DS} of them. Below in fig.2.6 and fig.2.7 are shown the main contribution of each layer on the total resistance in the two difference structure.

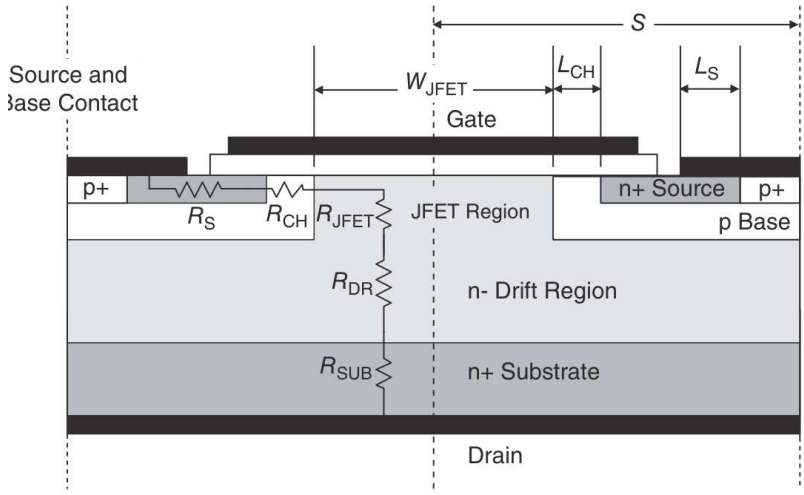


Figure 2.6: Internal resistance inside a power DMOSFET [21].

For the planar power mosfet the resistance seen between drain and source is defined by the equation 2.9, follow [21]:

$$R_{ON,SP} = R_{CH,SP} + R_{DR,SP} + W \times S \times (R_S + R_{JFET} + R_{SUB}) \tag{2.9}$$

Here R_S represents the resistance of the source contact and the n+ source region, R_{JFET} is the resistance of the vertical JFET gated by the grounded p base regions, and R_{SUB} is the resistance of the substrate and its ohmic contact. And W and S are the width and half-pitch of the cell. The DMOSFET introduced some innovations to achieve the desired features, and as can be seen form the literature [21], they could be: (I) a self-aligned submicron MOS channel, (II) a more heavily doped JFET region, (III) a current spreading layer (CSL), (IV) source ohmic contacts that are self-aligned to the polysilicon gate, and (V) p base contacts that are segmentented along the length of the fingers. For instance, a focus about one of them is the description of self-aligned source contacts, it allows the source ohmic metal and top metal to be deposited directly over the polysilicon gate, isolated from the gate by a thick oxide. This reduces cell area by eliminating an alignment tolerance, reduces the source resistance by shortening the n+ source region, and reduces the resistance of the top metal[21].
For the trench power MOSFET the new structure figure 2.7, present opportunities such as the possibility to create the same component in a smaller chip and to form a short-channel [21]. The effect of the JFET region has been deleted, so it is reasonable thinking that the total resistance in lower than planar one [21].

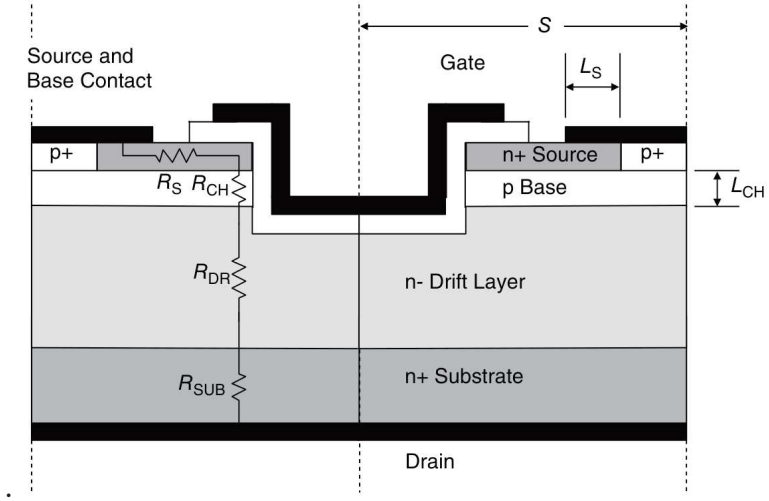


Figure 2.7: Internal resistance inside a power UMOSFET [21].

V_{TH} : The threshold voltage of the mosfet is the lowest level of tension that up to that the current starts to flow through the drain and source. Another way to define it as the a voltage applied to the metal electrode to enter in

strong inversion and when the surface of a semiconductor enters in strong inversion condition, the surface potential is equal to twice the bulk potential. The V_{TH} in a SiC mosfet is affected by trapping phenomenon [15] and when the junction temperature of the component increase the intrinsic carrier density rise and this bring a decreasing of the V_{TH} in relation with the temperature. If the temperature stress is continuing during the time, the SiC mosfet degrades due the accumulated electrons trapped in the gate oxide and the V_{TH} increases [33].

V_{DS} : The voltage across the drain and the source in a Mosfet is called V_{DS} and it can be distinguished in two: $V_{DS_{ON}}$&$V_{DS_{OFF}}$ during the t_{on} and t_{off} time respectively. The value of the voltage indicated as $V_{DS_{ON}}$ is defined by the current that pass through the channel and the relative resistance during that interval of time, $R_{DS_{ON}}$. The value of those resistance has been defined above and it has a strongly dependence by the controlling voltage (V_{GS}) and the threshold voltage V_{TH}. The value of the voltage indicated as $V_{DS_{OFF}}$ is affected by some parameters, as V_{GS} and from the conduction of the body diode. Because in the SiC mosfet the channel is not completely closed with $V_{GS} = 0V$ [33] and this bring some changes in the behaviour of its. This aspect is well addressed in chapter 4.

S_iC/S_iO_2 ***Defects*** : The defects in the gate oxide and in the interface between the semiconductor and the insulator are basically: mobile ionic charges, oxide trapped charges, fixed oxide charges, S_iC/S_iO_2 interface traps and near interface oxide traps. To have a better interpretation, in fig. 2.8 is reported a small image found in an article of literature [31] that show the differences between the different defects. The fixed charge is correlated with the oxidation process. The oxide trapped charges can be induced by ionising radiation and avalanche injection. The interface traps and near interface oxide traps can be attributed to structural defects. [31] The threshold voltage are mainly affected by the interface and near interface oxide traps and that bring a faster degradation of the SiC mosfet.

Junction Temperature : The theoretical working junction temperature in the SiC mosfet is quite higher than the Si mosfet counterpart. Furthermore, the higher thermal conductivity enables a reduction of the thermal resistance of the semiconductor device, that means a larger capability to handle with high current and high voltage without entering dangerous operating zones; but due to the structural defects and the problem during the manufacturing, the theoretical working temperature is not reached yet.

Gate oxide Reliability : High level of temperature can induce broking mechanism of the silicon dioxide. This bring a creating of a conductive path between the gate and source. The I_G increases and the V_{GS} dips to zero [8]. The reliability of the gate oxide in a SiC component is affected by different factors:
the density of interface traps is very high because of the presence of carbon

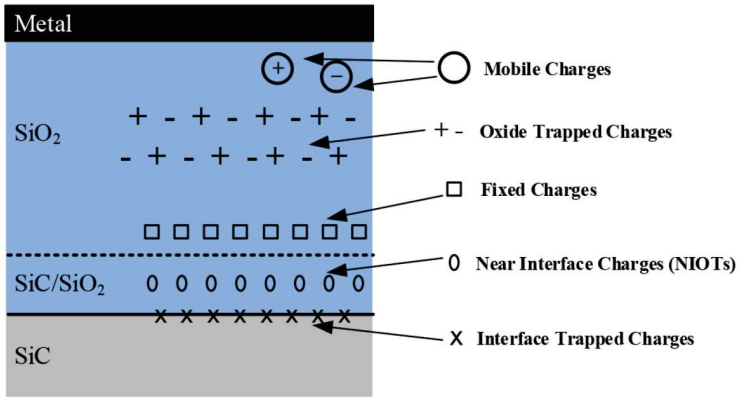


Figure 2.8: Simplified schematic diagram with reported main defects in the SiC mosfet [31].

atoms during the thermal oxidation of SiC and defects formed during the process. The density of charged interface defects and interface states in S_iC/S_iO_2 structures is still quite high and these are the possible root reason for the reliability and ruggedness of SiC mosfet.
The tunnelling effects are more present in the S_iC/S_iO_2 than in the S_i/S_iO_2, due to the small energy band offset between the semiconductor and the oxide. Furthermore, the SiC components have a higher tunnelling current with the same value of electric field; when the temperature increase the effective barrier height in the interface between the S_iC/S_iO_2 dips.
At the end the higher critical electric field allowed by SiC material, may cause failures inside the gate oxide [31].

To resume wide bandgap materials power electronic components are faster, smaller, more efficient and more reliable than their Si-based counterparts; furthermore, they permit the operation of devices at higher voltages, temperatures, and frequencies, making it possible to reduce volume and weight in a wide range of applications. SiC has highest thermal conductivity compared than Si, indicating that SiC devices can operate at higher power densities, that means SiC components produce much lower heat and thus the temperature will rise much more slowly. Wide bandgap devices can operate at a voltage 10 times higher than Si-based power devices, because of their higher maximum electric field and operating temperatures of well over 300°C, twice the maximum operating temperature of Si-based devices. [11] Thus the components manufactured with SiC look like the best compromise to handle high power.

2.3 Expected SC effects

According to the reported literature, discrete SiC mosfet devices can withstand an SC event for a shorter time than the Si components counterparts [31] and this can be see from the fig.2.9 . The main reason is that their much smaller chip size and

larger power density than Si components. Thus, the SC issues of SiC mosfet needs to be addressed for further performance improvement and to do that the failure mechanism has to be studied. Self-heating of the mosfet due to the short-circuit event is the most influential parameter, this processes is related to the increase of the device temperature, since temperature influences a multitude of physical quantities of any semiconductor [8]. When a SC events occur the drain current first rise up and then dips as the device temperature increases, due to the negative thermal coefficient. Furthermore, the threshold voltage of the MOSFET decreases. The level of the drain current is strictly related to the applied gate voltage from the relation [21]:

$$I_D = \mu_N C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{2.10}$$

Thus, higher is the gate voltage higher is the current peak during the SC event.

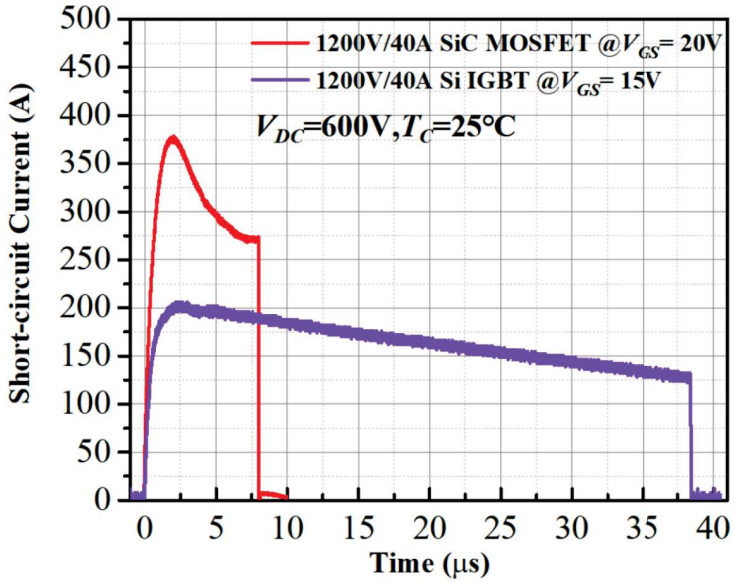


Figure 2.9: SC current comparison of the $1200V$ / $40A$ SiC MOSFET and $1200V$ / $40A$ Si IGBT under $V_{DS} = 600V$ and $T_C = 25C^{\circ}$[31]

However from the literature [31] can be distinguished two different failure mode for the SiC mosfet due to short circuit:

- Gate terminal shorted with the source and the PN junction is the remains blocking capability. The main key factor for this type of failure is the V_{GS} value.
- All three terminals of the component are shorted, this case is recognized as thermal runaway. The main key factor for this failure is the bus voltage value.

Therefore, when a SC event is applied to a SiC MOSFET, great care must be taken not to break the component under test.

Chapter 3

Device Characterization

The characterisation of a component consists in extracting its parameters. A SiC MOSFET or every electronic component has an enormous number of physical quantities that can be measured; as reported in chapter 2, section2.2 some parameters are linked with others, furthermore it exists a very close connection between them; obviously there will be some parameters more affected than others and some that will be independent. Thus, one of the first step in a project is to figure out which of them are relevant, fortunately in chapter 2 they are already pointed. It is important to bear in mind that, when talking about an integrated semiconductor component, one expects its parameters to be strongly interrelated, considering that the device is constructed into a single piece of semiconductor. This last sentence has been largely discussed and analysed considering the effect using a new semiconductor material that allows the construction of new components using even smaller quantities of semiconductor, see chapter 2.
However, the choice of the important parameters has been taken in advance, as reported in 2.2. In this chapter the focus is to report the measurement evaluated before the stressing procedure (stressing means DC power cycling); in chapter 1 all the three different study cases have been expounded; a small recall of them is mandatory, thus the three families of components that will be evaluated are:

No Short circuit : This family is the one that did not get stressed, it means the components belonging to it have characterised directly out from the manufacturer. Thus, they did not receive any stressing procedure (like SC and PC), the expected behaviour should match with the data provided by manufacturer on the data-sheet; it is important to bear in mind that due to the mismatch and variation of the parameters, there will probably be some variations, but this fact has been taken into account previously. For that reason, several components will be characterized.

Short circuited with damage : SiC mosfet are especially susceptible to damage as a result of short-circuiting events due to their fast switching speeds and very low on-state resistance. As reported in [25], the current passing through a SiC mosfet during a short circuit event can exceed 10x the nominal rating with 10-20 microseconds after turn-on. In this case the parameters extracted by the analyser after short-circuit event will not match with those extracted

by the components at which the SC haven't been performed.

Short circuited without visible damage : In this batch the SC has been performed but below the critic energy (E_C), that value has been extracted in in a step before. Thus, the curves expected behaviour should be the same, or better, should be in the range of the variation found in the first case, for the component at which the SC was not performed.

The equipment used for the study and for extrapolation and derivation of the parameters and curves is a dedicated analyser, the owner company of the project and the seller is the Keysight; the device is the Keysight B1505A. It is a single-box solution with the capability to characterize high-power devices from the pico-ampere level up to several hundred ampere, as well as for the voltage. All the features are available and reported in [19]. The components have been characterized are SCT070W120G3AG from STMicroelectronics, since they are power components is reasonable thinking the package is also made to handle for high power level of voltage and current; since they are designed to have a blocking voltage equal to $1200V$ and constant current entering thought the drain equal to $30A$ at $25°$, it's understandable that the construction of the container in which the DIE are arranged, has to be consistent with the power level. The following components are provided in two different power packages: TO-247 *3 pins* and TO-247 *4 pins*. The main difference between them is the number of pins, to be precise in the *4 pins* the source contact is divided in two, or better, the source contact has two pins, one used for the power connection, so current flows out of this pin and in from the drain, and the another one is the sense connection, as known as kelvin source, this pin is used to have a very clean and precise measure of the source potential because the kelvin source is arranged closer to the DIE than the power source pin. Furthermore, the *4 pins* introduces a higher efficiency in the switching losses, as reported in [27], due the gate voltage relevant effects, because the gate voltage affects also the R_{ON}. In fig. 3.1 it can be seen the structural difference between the two configurations, the increasing of the efficiency in the *4 pins* can be explained looking at the right-hand figure and observing that using the kelvin source as reference to control and to apply the gate signal, the parasitic inductance coming from the source power pin has been neglected, so that the V_{GS} needed to turn-on (or better, to enter in the inversion layer) the component is lower because the voltage across the stray inductance is not present.

The Keysight B1505A Power Device Analyzer has a very well defined measurement procedure and also the connections are pre-set, but to be able to measure a real component another equipment is needed, that creates the connection between the B1505A and the DUT (device under test). The mid component is the N1265A Ultra high current expander/fixture which contains the current expander to enable $500A$ output and measurement, and contains the selector to switch the measurement resource connected to the DUT.
The measurement chain is reported in the graph 3.2 and as can be seen, between the DUT and the N1265A there is an adaptor, which is needed just to create a well-done connection between the DUT and the cable coming out from the

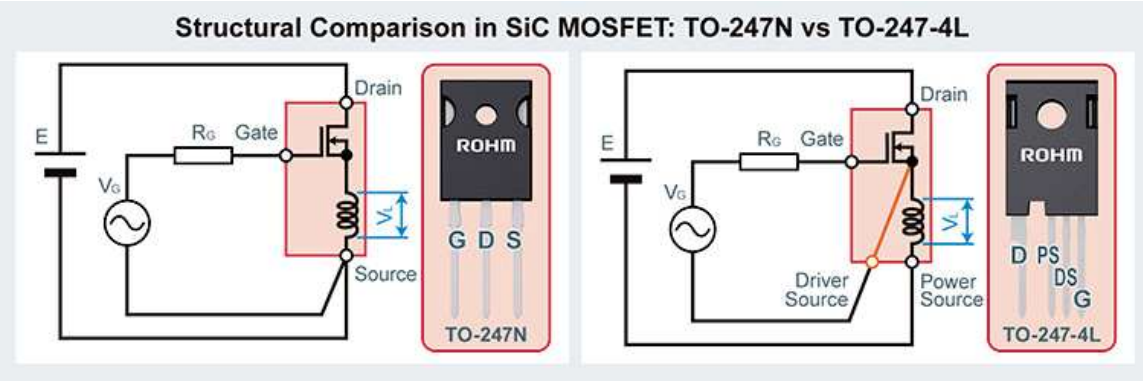


Figure 3.1: Structural differences between TO-247 *3 pins* and TO-247 *4 pins* [27] .

expander. The final data come out from the B1505A and they can be used in several different ways, in our case the interest measurements are: I_D/V_D, I_D/V_G, $I_{G_{SS}}$ and $I_{D_{SS}}$. However, the N1256A was designed in such a way as to separate the power and sensing connections. As can be see in fig.3.3, every pin of the DUT has two possible connections, one for the force and one for the sense (except the gate, it still have two cable, this for apply a gate signal with a modifiable reference point). In this case is reported a n-mosfet in a TO-247/4 package, where the sense pin for the source is the kelvin source, so at the end in total, to perform the measurements that we need, 6 connections are needed; it is important to bear in mind that the same number of connections is required also with TO247/3 package.

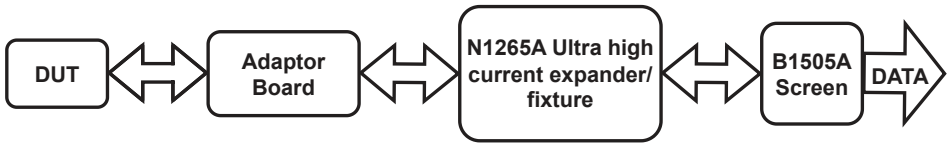


Figure 3.2: Flow chart of measurement chain using Keysight products.

An additional difficulty introduced in this project was the lack of an adaptor board for the TO247/4, therefore a new adaptor board has been designed following the guideline provided by Keysight in [20]. The crucial step was to create a board that fit with the required packages (TO247/3 and TO247/4) and that allowed to perform correctly the measurements, thus creating, as mentioned above, the connection for the force and sense cable. To address the problem about the two different packages a new footprint has been developed, it was to be allowed to install in the same adaptor two different components (not at the same time) with mounting structure markedly different, thus a 5 pins foot print has been extrapolated through superposition of the pins. The following footprint is reported in fig. 3.4 and the in the upper side are indicated the enumeration of the pins for

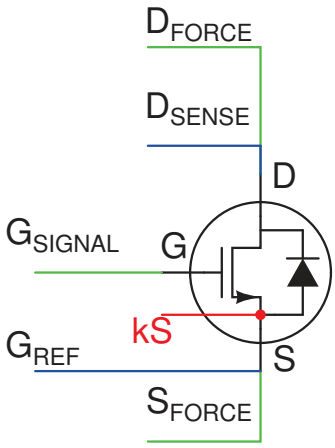


Figure 3.3: Division of power and sense connection in a mosfet with package TO247 4 pins.

the package TO247/3 and in the lower side for the TO247/4.

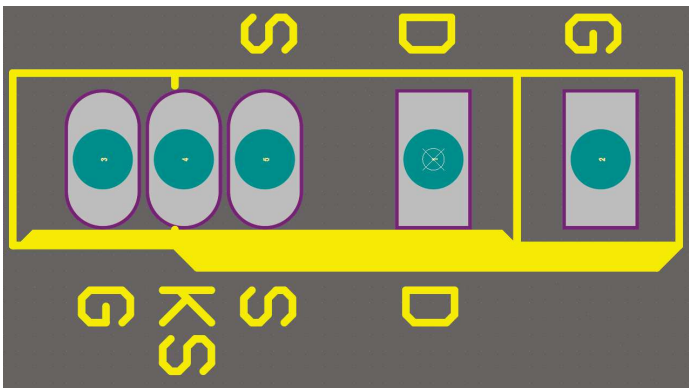


Figure 3.4: Footprint for installation of TO247/3 an TO247/4.

This approach was also adopted for the next phase, the DC power cycle, but this is better detailed in the chapter.4. The hole and the pads are oversized to make installation and disassembly easier, but in the final project it is added also the dedicated socket, that allows an easier installation without the use of solder. The final project and a picture in which are reported all the connections and the DUT in a real case are reported in fig.3.5 and fig.3.6, respectively. In fig. 3.5 the 5 pins footprint can be pointed and it is on the right-hand side of the board, instead in the center there is the socket adaptor. One thing can be highlighted and it's that for the gate, there is just one connector, this because the gate in the mosfet should absorb a very small current, so the force and the sense connections has been merged.

In figure 3.6 the DUT can be seen on the left-hand side of the board and the connections, the red connector are used to indicated the high side, that means the drain, the black for the low side, so the source, and the last one, the yellow is used for the gate control.

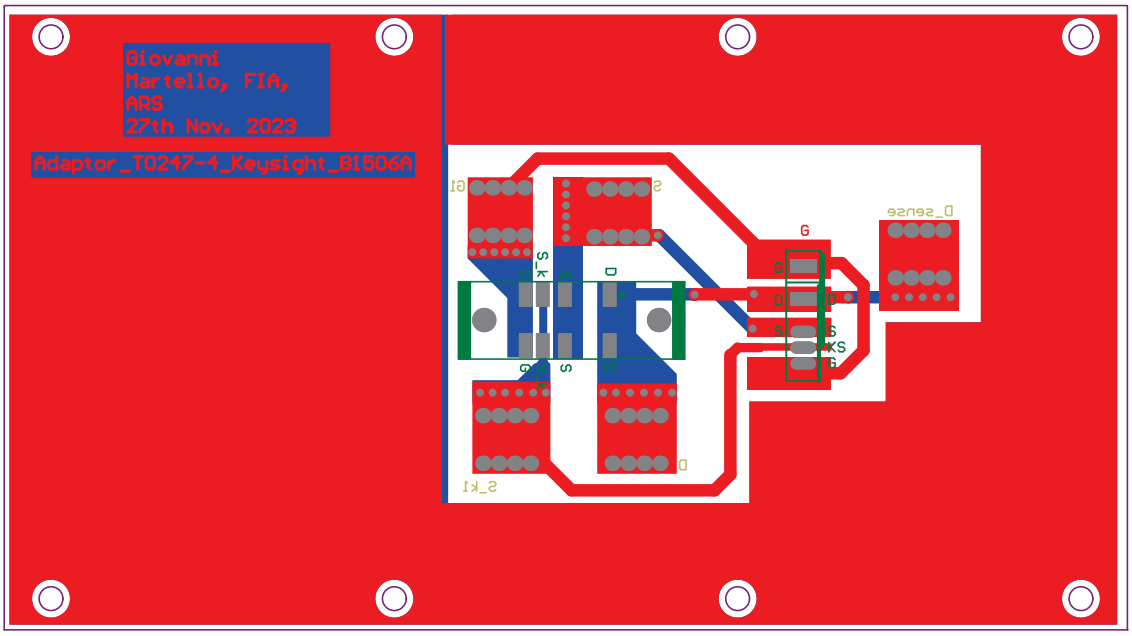


Figure 3.5: PCB board of adaptor, here is highlighted the top layer.

3.1 Measurements of interest

During the characterization of components several measurements can be performed. The measurement chain using the Keysight's product are able to extract a lot of information from a DUT, but in this project just of them are needed and relevant. The curves of interest are: I_D/V_{DS}, I_D/V_{GS}, $I_{D_{SS}}$ and $I_{G_{SS}}$. A short explanation about the circuit connection used to extract the correct curve in each measurements is useful to understand how the measurement has been performed. Below are reported a short description of each different circuit used:

I_D/V_{DS} During the extrapolation of the following curve, the focus is to check the behaviour of the component under different values of gate voltage, the measurement circuit carried out by Keysight B1505A is reported in fig. 3.7. As reported in blue, the gate and the drain voltage are steeped up and down during the measurement. To address in a complete way this quantification of the component, the working procedure is explained: the voltage V_{DS} is setted to start from an well defined value up to the maximum set value, this sweep has been performed for every prearranged gate voltage, because also the V_{GS} is changed and as can be see in fig. A.1 the curve I_D/V_{DS} has been plotted at 8 different gate voltages. Thus for every value of gate voltage, the drain voltage is swept, from the minimum up to the maximum value and at the meantime time the current of the drain is sampled. The reason for

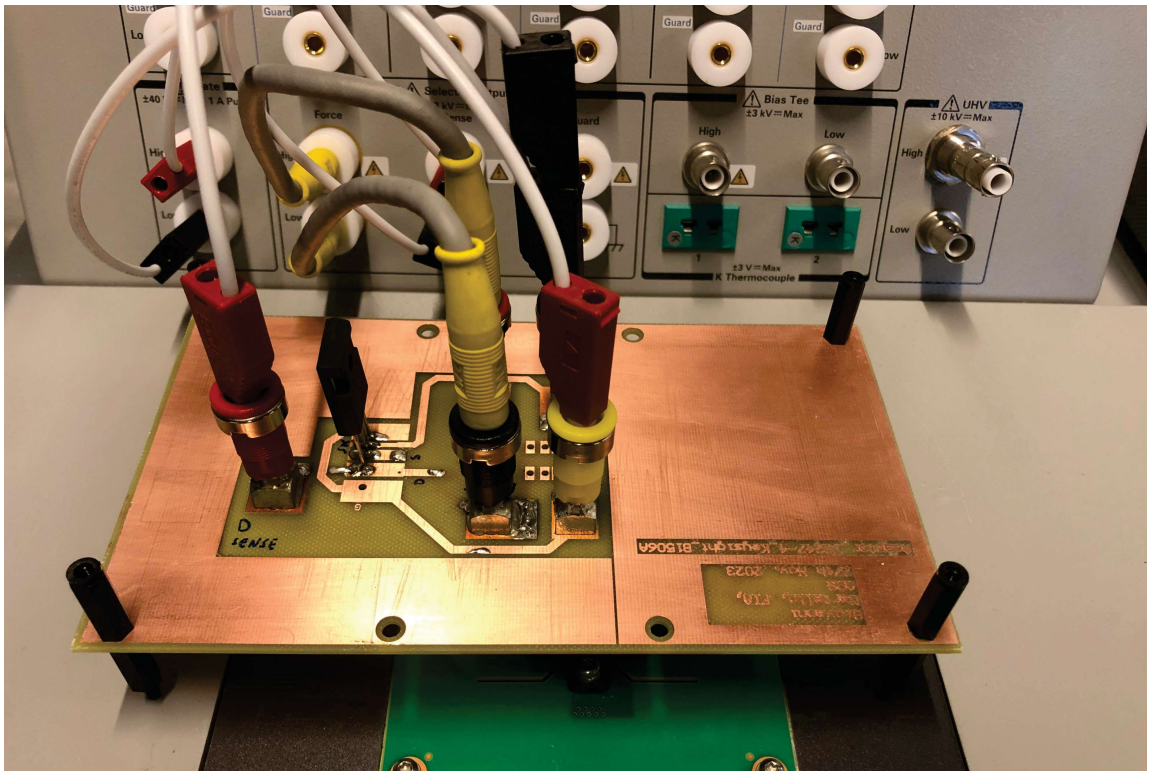


Figure 3.6: Picture of DUT and adaptor board connected to the analyser.

changing the gate voltage is to extract a graph to recognise the saturation and linear working region of the mosfet. Furthermore, it is interesting to analyse the behaviour of the mosfet in the presence of a high current at different gate voltage.

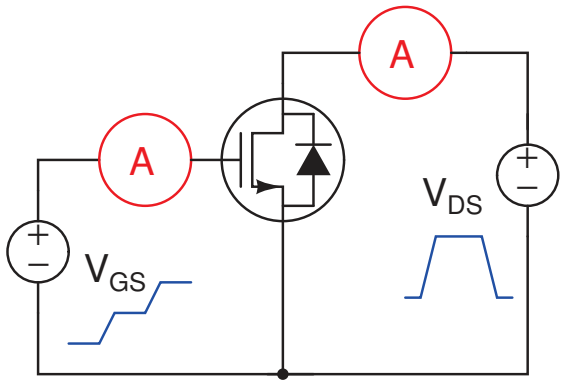


Figure 3.7: Conceptual electric schematic to measure the value of interest, for I_D/V_{DS} graph.

I_D/V_{GS} This curve in the most part of the cases is plotted to extract the threshold voltage of the mosfet. It is the value of the voltage at which significant current starts to flow through channel, or it is the voltage applied to the metal electrode to enter in strong inversion and when the surface of a semiconductor enters in strong inversion condition, the surface potential is equal to twice the bulk potential. The tipical way to measure the V_{TH} is short together the gate and drain, but in this case Keysight decided to perform in a different way, so that a new connections weren't needed, as reported in [19], both gate and drain voltage sweep at the same potential by synchronizing two SMUs. Then in order to decide what the V_{TH} is, it is sufficient to decide for which drain current the threshold voltage is considered to have been reached. To compare the results extracted by measurements with the data obtained from the data-sheet of manufacturer the same drain current should be taken into account, however this aspect is addressed in the section 3.2. The simplified schematic measurements chain used to extrapolate the V_{TH} is reported in fig.3.8, the dotted line indicates the hide connection created internally in the B1505A [19].

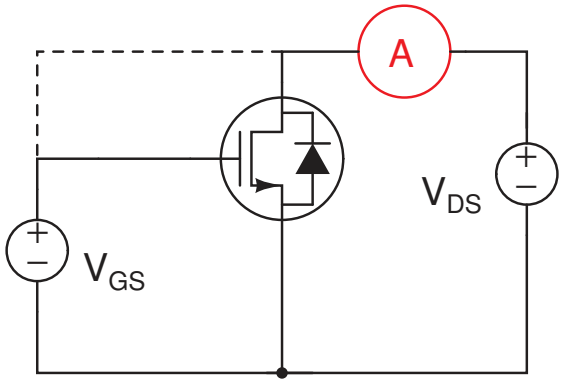


Figure 3.8: Conceptual electric schematic to measure the value of interest, for I_D/V_{GS} graph.

$I_{D_{SS}}$ The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited is defined as $I_{D_{SS}}$. As in the previous points a simplified electric measurement is displayed below, it can be see in fig.3.9. The ideally value of leakage current in a mosfet should be equal to zero ampere, but every real component has non-idealities characteristic and one of these is the gate leakage current. Considering that the voltage applied on the gate is markedly below the threshold voltage, the channel is not formed, so no electrons should be able to pass through the channel, because the transistor is in sub-threshold region, or weak-inversion region.

$I_{G_{SS}}$ The leakage current that occurs when the specified voltage is applied across gate and source with drain and source short-circuited is defined as $I_{G_{SS}}$. Low oxide thickness with high electric fields results in electrons tunnelling from

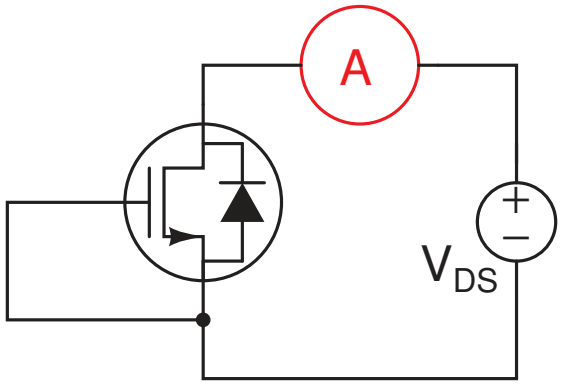


Figure 3.9: Conceptual electric schematic to measure the value of interest, for $I_{D_{SS}}$ graph.

the substrate to the gate and from the gate to the substrate through the gate oxide, resulting in gate oxide tunnelling current.

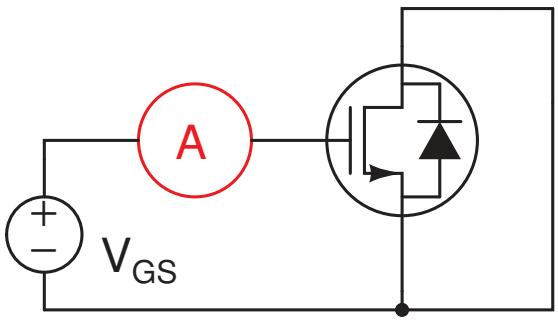


Figure 3.10: Conceptual electric schematic to measure the value of interest, for $I_{G_{SS}}$ graph.

Above have been reported the typical measurement that can be performed to characterize a MOSFET, but at some point of the ISLE project development, those data were not enough and the university partner with the AAU reference professor decided to develop a measurement list dedicated. This list of measurement is reported in the table 3.1. It has been arranged bearing in mind that the tests have to be performed on a large number of sample, for each family. Thus, the list of measurement has been formed by the parameters of interest that, from the point of view the project's supervisors, indicate the similarity between the samples.

The list of tests starts with the measurement of the reverse leakage current that comes from the gate of the MOSFET in a particular condition, in reverse state, that means the drain and the source are still shorted and the potential on the gate is set negative, then the point is to extract some current from the gate. The second one is the contrary, the forward gate leakage current, then the same condition as before with $V_{DS} = 0\,\text{V}$, but the gate is polarized positively, then the test wants to see which is the amount of the current that can be adsorbed by the gate. It important to bear in mind that an ideal MOSFET doesn't absorb any current on the gate, but as can be seen by the values of the leakage current on a real

Parameter	Description	Condition
$I_{G_{SS}Rev}$	Gate-Body Leakage Current Reverse	$V_{DS} = 0\,\text{V}, V_{GS} = -10\,\text{V}$
$I_{G_{SS}}$	Gate-Body Leakage Current Forward	$V_{DS} = 0\,\text{V}, V_{GS} = 22\,\text{V}$
V_{TH}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\,\text{mA}$
$I_{D_{SS}}$	Drain leakage current	$V_{GS} = 0\,\text{V}, V_{DS} = 1200\,\text{V}$
Delay		100 ms
$R_{DS_{ON1}}$	Static Drain-Source On-Voltage	$V_{GS} = 15\,\text{V}, I_D = 15\,\text{A}$
Delay		100 ms
$R_{DS_{ON2}}$	Static Drain-Source On-Voltage	$V_{GS} = 18\,\text{V}, I_D = 15\,\text{A}$
Delay		100 ms
BV_{SS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\,\text{V}, I_D = 1\,\text{mA}$
$I_{D_{ON1}}$	Drain On Current	$V_{GS} = 10\,\text{V}, V_{DS} = 10.5\,\text{V}, t_P = 300\,\mu\text{s}$
Delay		200 ms
$I_{D_{ON2}}$	Drain On Current	$V_{GS} = 10\,\text{V}, V_{DS} = 15\,\text{V}, t_P = 300\,\mu\text{s}$
Delay		200 ms
$I_{D_{ON3}}$	Drain On Current	$V_{GS} = 10\,\text{V}, V_{DS} = 20\,\text{V}, t_P = 300\,\mu\text{s}$

Table 3.1: Test list of ISLE/ECPE project 2024, all the measurements has been performed by Alter Technology France.

component has a small value. As third measured parameter has been selected the threshold voltage that as well explained in the chapter 2.2, the threshold voltage correspond to the gate-source voltage at which a significant drain current starts to flow. And the measurement condition are the same reported above; the important in this case is to decide a drain current at which the V_{TH} is defined. The forth parameter is the drain leakage current; it has the kind same purpose of the first two, find the current that flows into the drain of the MOSFET, when the channel is open and the drain voltage is very high. Then a delay period is introduced. After that the resistance of the MOSFET during the on-state is measured twice, one with the gate voltage equal to 15 V, then a small delay and the last time with the gate-source voltage equal to 18 V (the suggested working gate voltage). The resistance during the on-state are affected by multiple factors, as said in the chapter 2.2, and it value is determinated also by the choice of the gate voltage, see equation 4.1; larger is the V_{GS} lower is the value of the $R_{DS_{ON}}$. This parameter is

very important for the power cycling test, since the MOSFET increases its own temperature during the PC test, due to the value of the resistance, thanks to the Joule effect. Thus, the value of the on-resistance to find similarity between the components is so interesting. All the on-resistance measurement are performed with the same current level. Then another delay occurs and the drain to source blocking voltage is measured, that is the drain to source voltage with the gate ideally shorted with the source and the drain to source potential is increased since the current on the drain is equal a defined value, in this case is 1 mA. The last parameter measured for three times is the drain current in three different condition, imposing the gate and the drain voltage and measuring the drain that flows through the drain. The only thing that that changes is controlling voltage, that starts from 10.5 V, then 15 V and the last is equal to 20 V.

3.2 Parameter of three different batches

3.2.1 Not short circuited

Considering that the following project is in collaboration with another university the timing of proceeding can be slow and has some delays due to the distance and the several appointment of the supervisors. For that reason up to now has been analysed just the virgin sample, those one that no stresses have been applied. The simple results, as discussed above, are extracted with the analyser provided by Keysight, in each graph are reported two different curve and each of those correspond to one sample, instead several data can be see in the graphs related to the list adopted and decided during the developing of the project, reported in the table 3.1; those data has been extracted by **Alter Technology France**.
Now a short description of the graph extracted using the Keysight follows. The trans-characteristic of the two MOSFET are showed in fig. A.1, and as can be seen increasing the gate voltage, the drain current markedly surges for the same value of the drain voltage, this can be explained by the equation of the current of the mosfet, that it has a linear dependency from V_{TH} and V_{GS}. In the fig.3.11 are reported the curves that allow to extract the value of V_{TH} and the two threshold voltage have a slightly difference between them, but this is normal, because their values are between the range indicated by the manufacturer. The values of the threshold voltage in the two different cases are reported in tab.3.2, the range of the V_{TH} can be sees in [29]. It is important to bear in mind that the value of V_{TH} has been measured at one specified drain current, thus to be consistent with the comparison between the manufacturer data and the extrapolated one, the drain current has been set equal to that one indicated in the data-sheet, so $I_D = 1\,\text{mA}$. It exists way more different typologies to measure the threshold voltage in a MOSFET, but to be still consistent with the specification of the manufacturer, during the test (PC) the drain and source are shorted together and the current at which the threshold voltage is reached is $I_D = 1\,\text{mA}$. Then, the two remaining graphs extracted by two test samples are reported in figure A.3 and A.2. They are reporting the behave of the gate and drain leakage current, respectively.

	Threshold voltage
Sample 1	2.7330 V
Sample 2	2.7179 V

Table 3.2: Values of threshold voltage of the two virgin samples reported in fig3.11, the reference current is $I_D = 1\,\text{mA}$.

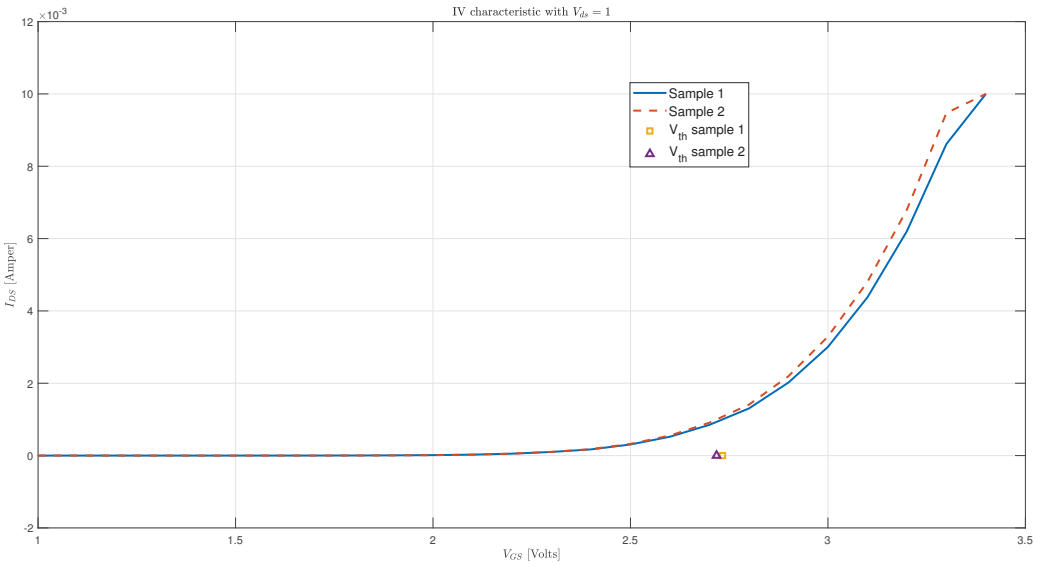


Figure 3.11: I_D/V_{GS} curves in which the V_{TH} are reported curve.

The graph 3.11 has been reported as an example, but the interesting things now is figure out what are the results of the measuring list reported above. The entire characterization has been performed on 140 different samples, then a data base of informations formed. The high number of sampled analysed is due the fact of the variation of the electrical parameter of each component has, then a large number of samples is used to increase the probability of finding components with similar parameter values. From the 140 samples just a well defined number of components can be selected and the way, to select them, is described by the characterization list reported on the table 3.1; comparing the values of some parameters the more similar component can be extracted. From 140 just 45 samples have been selected to be used on the project. The 45 samples include all the components that form the three families, they are reported here because the characterization done up to now are performed on new components, not to stressed ones, thus the results can be incorporated together. Not all the graphs are reported here, but just the more relevant for the scope to show the similarity between them. The samples have been selected by the university partner of the project, the IRT with the help

of Alter. The figure 3.12 report the reverse leakage current of the gate with the drain and source shorted, and the voltage on the gate is equal to $-10\,\mathrm{V}$. The average value of the gate reverse leakage current, considering all the 140 samples, is $-1.771\,06 \times 10^{-9}\,\mathrm{A}$.

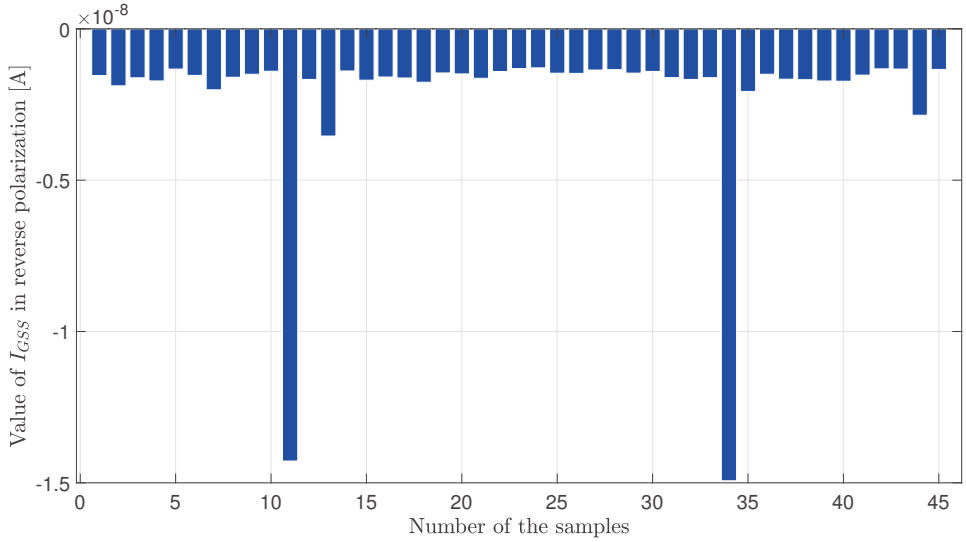


Figure 3.12: Bar graph of the selected samples that reports the reverse gate leakage current. Measure performed by Alter Technology France.

The figure 3.13 report the direct leakage current of the gate with the drain and source shorted, and the voltage on the gate is equal to $22\,\mathrm{V}$. The average value of the gate direct leakage current, considering all the 140 samples, is $4.617\,27 \times 10^{-9}\,\mathrm{A}$.

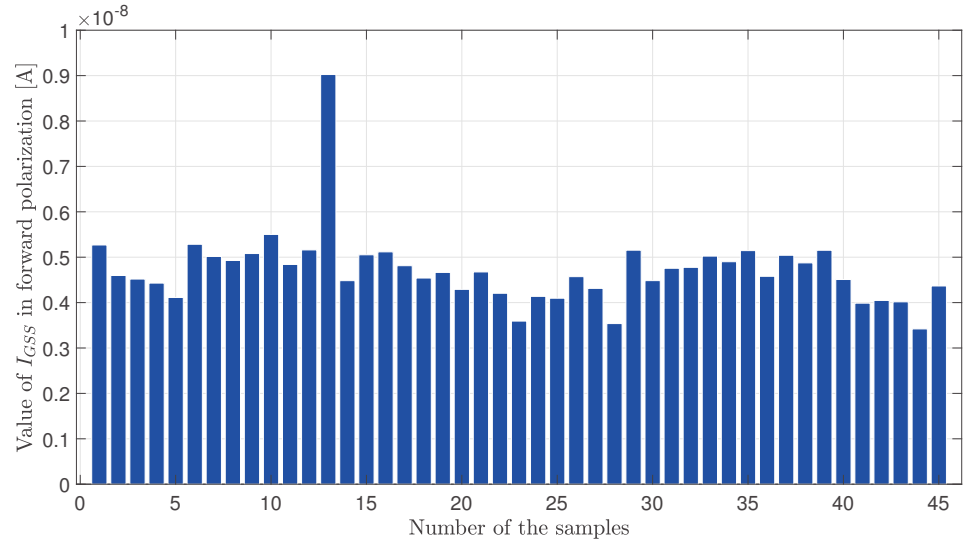


Figure 3.13: Bar graph of the selected samples that reports the direct gate leakage current. Measure performed by Alter Technology France.

The figure 3.14 report the threshold voltage extracted shorting the gate and the drain together and pushing a current equal at 1 mA into the drain. The average value of the threshold voltage, considering all the 140 samples, is 2.9146 V.

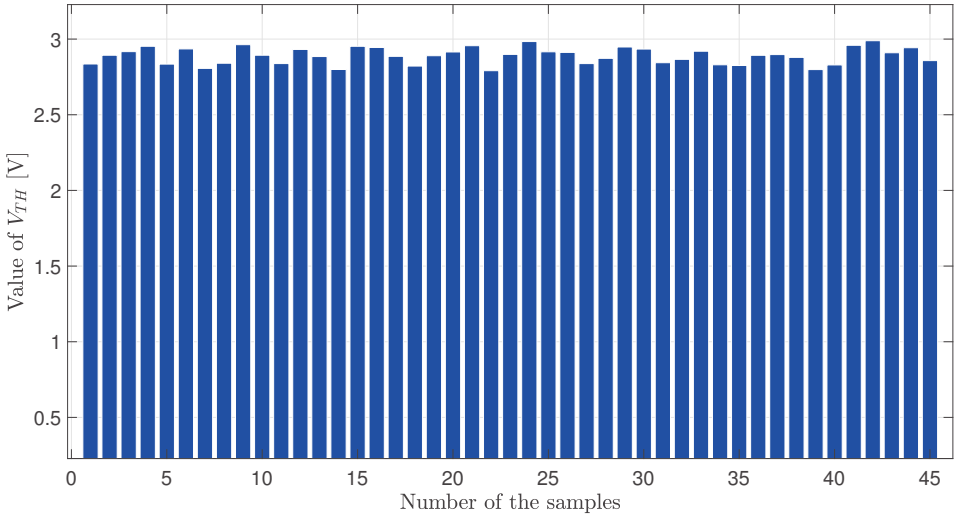


Figure 3.14: Bar graph of the selected samples that reports the Threshold voltage. Measure performed by Alter Technology France.

The figure 3.15 report the drain leakage current with the gate and source shorted, and the voltage on the drain is equal to 1200 V. The average value of the drain leakage current, considering all the 140 samples, is $1.944\,33 \times 10^{-7}$ A.

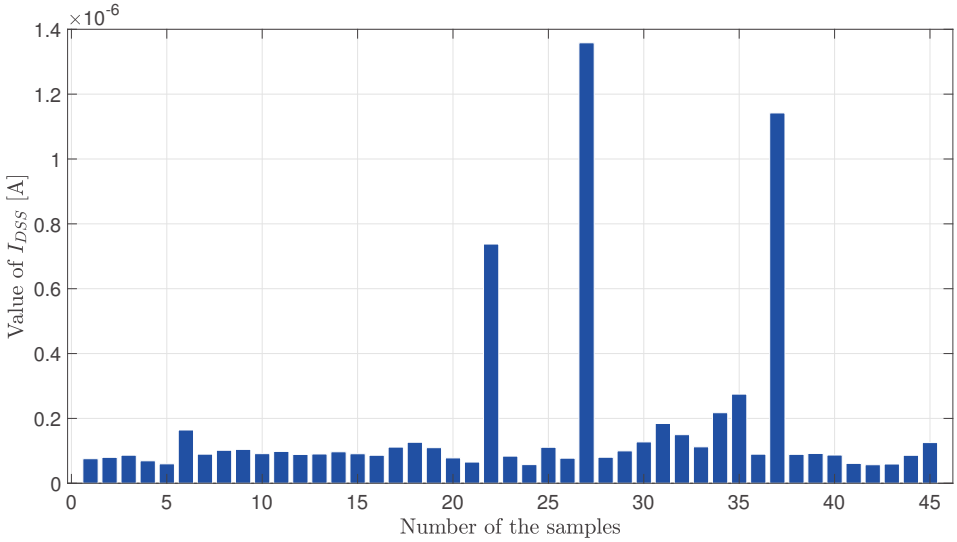


Figure 3.15: Bar graph of the selected samples that reports the drain leakage current. Measure performed by Alter Technology France.

The figure 3.16 report the on-resistance in the first case, with the gate voltage equal to 15 V and the drain current equal to 15 A. The average value of the

on-resistance, considering all the 140 samples, is 80.31 mΩ.

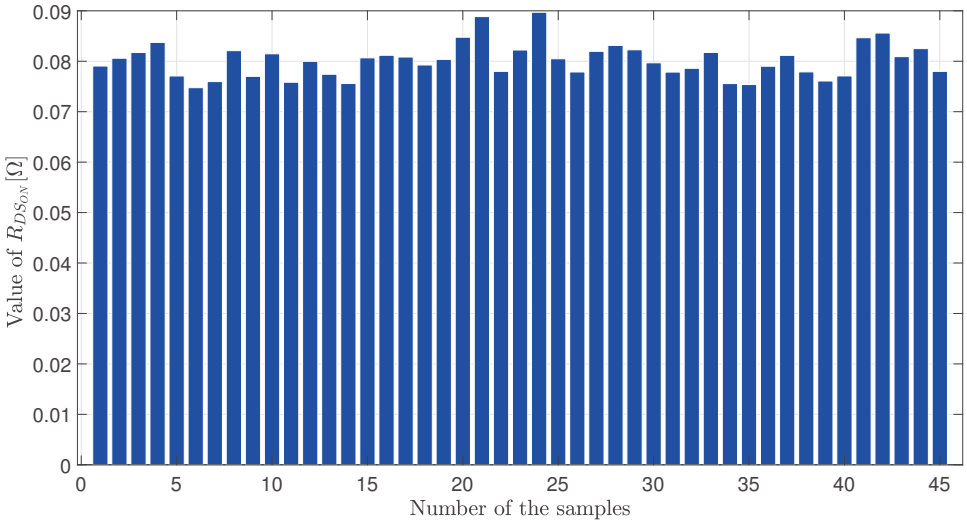


Figure 3.16: Bar graph of the selected samples that reports the on-resistance in the first case. Measure performed by Alter Technology France.

The figure 3.17 report the on-resistance in the first case, with the gate voltage equal to 18 V and the drain current equal to 15 A. The average value of the on-resistance, considering all the 140 samples, is 66.88 mΩ.

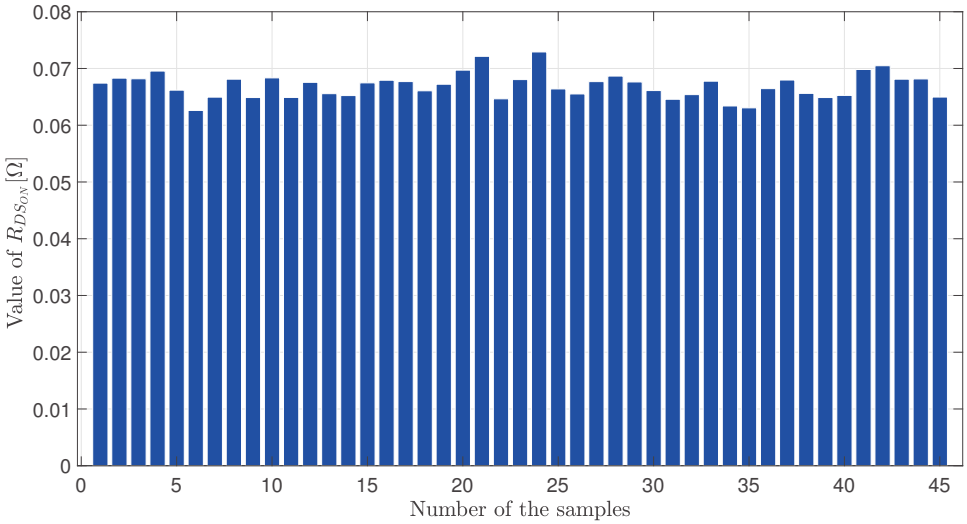


Figure 3.17: Bar graph of the selected samples that reports the on-resistance in the second case. Measure performed by Alter Technology France.

Obviously the average of the on-resistance values is lower when the gate voltage is higher, as can be seen comparing the two figures 3.16 and 3.17, and this can be explained by the formula 4.2. The figure 3.18 report the drain current in the first

case, with the gate voltage equal to 10 V and the drain voltage equal to 10.5 V. The average value of the drain current, considering all the 140 samples, is 23.879 A.

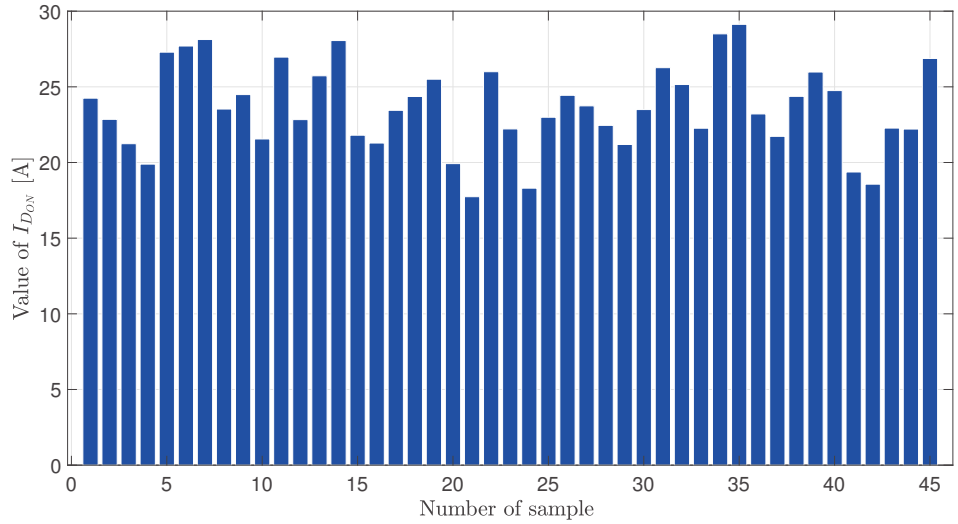


Figure 3.18: Bar graph of the selected samples that reports the drain current in the first case. Measure performed by Alter Technology France.

As last figure 3.19, is reported the voltage of the inner body diode, measured imposing the inverse current equal to 15 A and the gate voltage equal to the source potential, then to 0 V. It was not included in the list of measurement but it has been performed as well, just to have a reference of each V_{SD} value in the next steps. The average value of the body diode voltage, considering all the 140 samples, is 2.412 V.

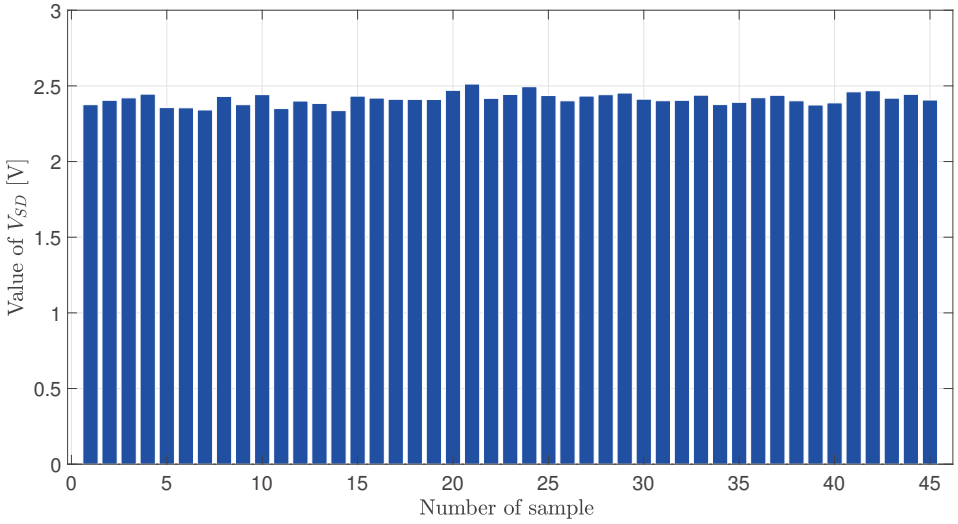


Figure 3.19: Bar graph of the selected samples that reports the body diode voltage. Measure performed by Alter Technology France.

After all this figure, can be understandable the 40 samples have been selected properly and the proves are shown above, the variation of the selected parameters is acceptable to assert that they are similar and their behaviour could be satisfying during the next step.

3.2.2 Short circuited with damages

Data not available at this moment of the project.

3.2.3 Short circuited without visible damages

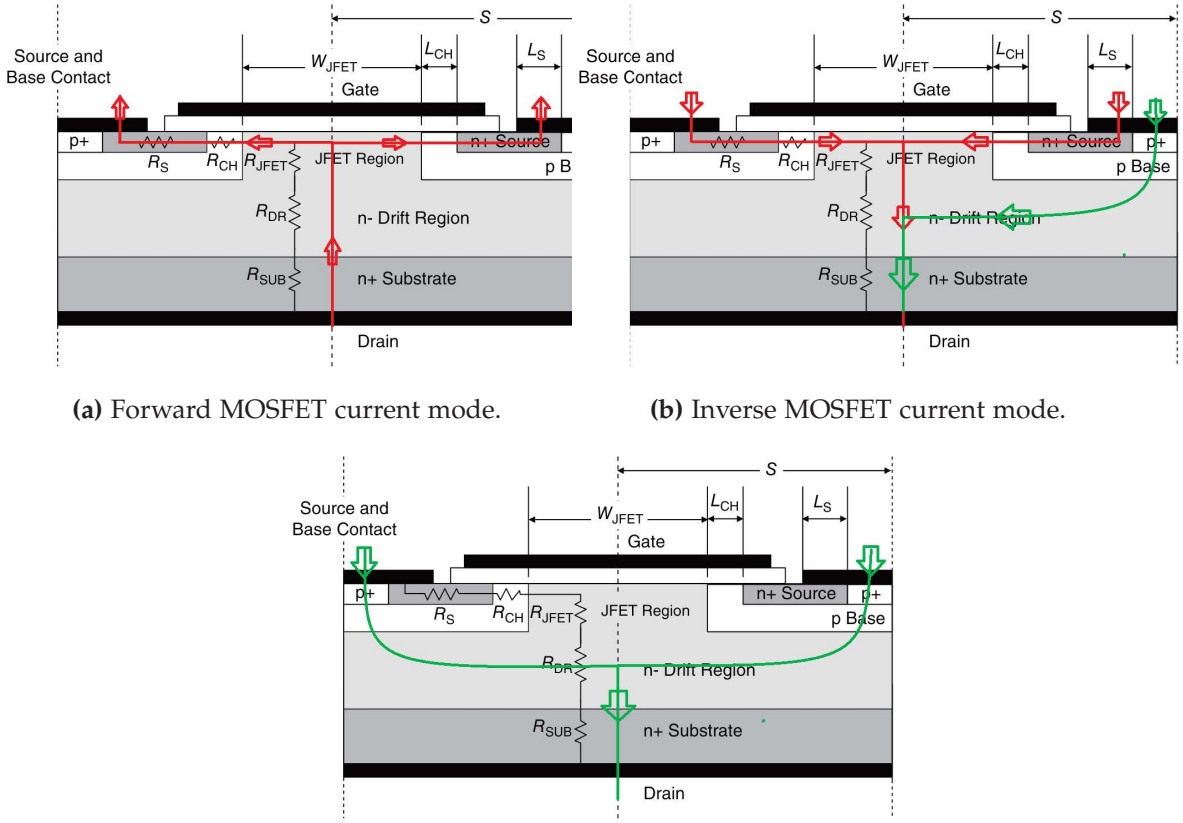
Data not available at this moment of the project.

Chapter 4

DC Power Cycling

According to a recent survey, the power semiconductor failures account for more than half of the total failures in DC-DC converters in industry [33]. As mentioned in the previous chapters, the reliability of power semiconductor devices is important as the device failures can lead to power converter malfunctions or power interruptions, which are not desirable in industry because of the penalties of maintenance cost, operation cost, and safety concerns. Thus a way to evaluate the reliability of them is so important. The classic way to extrapolate the life time of a power device is perform the Power Cycling test, that is the most important reliability test in of power electronics, normally with DC injection in conduction mode [4]. For the power device with a single conduction mode (single conduction mode means that the current has a single path in which flows, instead into the mosfet exist more than one current paths and they depend in which state the component is; furthermore the presence of body diode add a further path for the current), as IGBT, diode, the knowledge about the procedure of the test is well know. Whereas due to the unique characteristics of the MOSFET cell structure, there are three conduction modes, namely forward MOSFET mode, reverse MOSFET mode and body diode mode [4]. The different characteristics under different conduction modes lead to different PC methods, and the failure mechanisms and lifespans may vary. However, the standard of PC method for mosfet is not clearly defined, and it is mentioned that the body diode mode can be used to simplify the test process. Therefore, a precise and accurate study about the reliability of the power semiconductor device is needed, especially for the emerging silicon carbide SiC MOSFET since limited field data are available regarding its reliability [33].

As reported in literature [4] three different working zone exist for power MOSFET, the forward mode, the inverse mode and the body diode mode. In the fig. 4.1 are reported the three cases mentioned above, taking into account them, it is reasonable to think that the current passing through the mosfet has different behave in those three cases, so the conduction paths changes. In the most of the cases, in the direct conduction of the mosfet is in the forward voltage, thus the current flows from the drain to the source through the formed channel that can be see in fig4.1a where is present the R_{CH}. When the mosfet is turned off, that means $V_{DS} < V_{GS} - V_{TH}$ and $V_{GS} < V_{TH}$, the only possible way for the current to pass



(a) Forward MOSFET current mode.

(b) Inverse MOSFET current mode.

(c) Body diode MOSFET current mode.

Figure 4.1: Three different path of the current during working modes.

through the mosfet is from the body diode an parasitic structure of the power mosfet, which can be used as a freewheeling during switching; so the current can flow just if enter from the source and go out from the drain. This case is reported in fig.4.1c. When power MOSFET is working in the reverse mode, that means the mosfet is kept turn-on, or better the channel is still present, thus the conventional current path for the current is formed, furthermore the current may also flow from the source through the PN junction to the drain, as shown by the dashed line in fig.4.1b. At this time, the mosfet device works in a combination mode of forward mode (for the presence of the channel) and body diode mode.

The most important factor affecting the power cycling capability is the junction temperature T_J swing and the maximum junction temperature T_J^{MAX}, because higher is the temperature of the component, higher is the degradation rate [4], thus the lifetime is affected and, with good approximation, reduced. Since the power cycling test has been performed on components with the TO-247 package Thus, the temperature of the MOSFET has to be measured in the best and more precise possible way; the best solution would be to have the possibility to measure directly the junction temperature through a temperature sensor (PTC, custom optical fiber, laser, infrared camera, etc...), as it is used in the power module in which using a thermal optical fiber the junction temperature is sampled directly. Instead, in the ISLE project as mentioned before, the component are discrete, thus

the DIE of silicon carbide is surrounded by epoxy resin and all the structure forms the TO-247 package, hence the junction cannot be reached. This means that the junction temperature has to be extracted applying a different approach, an indirect procedure, this can be done finding a measurable electrical parameter that has a close correlation with the temperature, or better that its value can has changes with the variation of the temperature of the junction. Exist plenty of these possible parameters and they are known as TSEP. In some research, as reported in [15] [9], it has been observed how is difficult to find a temperature sensitive electrical parameter (TSEP), that it is independent of both device aging and package related degradation. Taking into account that, the selected TSEP must be as independent as possible by all the previous possible problems that are out of the scientist's control.
An overview about which is the best indirect way to measure the junction temperature, is needed, to do that in the tab.4.1 are listed the possible parameters used for this goal. Each electrical values reported needs and has its own approach to extract the junction temperature and in every different case are present one or more possible issues linked with it.

Parameters	Possible issues
$R_{DS_{ON}}$	Trapping e^- in gate-channel, degradation met. chip, lift-off bonding wires.
V_{TH}	Trapping e^- inside the gate-channel and oxide defects
V_{SD}	Channel not completely close (a calibration is needed)

Table 4.1: Principal issues about a reliable TSEP parameter.

$R_{DS_{ON}}$ can not be the TSEP for the PC, because its value has a strong dependence with the temperature and it is not stable, due the trapping into the gate-channel and the degradation of the metallization. This instability can be see on the graph 4.2 and it's can also be explained through the equation 4.1, where R_{ch} is the resistance of the channel, R_d is the resistance of the drift region and the R_{sub} is the resistance of the substrate. And as reported in [9] the channel and the substrate resistances are both directly linked with the temperature from the mobility.

$$R_{DS_{ON}} \simeq R_{ch} + R_d + R_{sub} \tag{4.1}$$

And as reported in [9] the channel and the substrate resistances are both directly linked with the temperature from the value of the mobility and their values are expressed by 4.2 and 4.3.

$$R_{ch} = \frac{L_{ch}}{W_{ch}\mu_{ch}C_{OX}\left(V_{gs} - V_{th}\right)} \tag{4.2}$$

$$R_{sub} = \frac{L_d}{q\mu_{nd}N_D A_d} \tag{4.3}$$

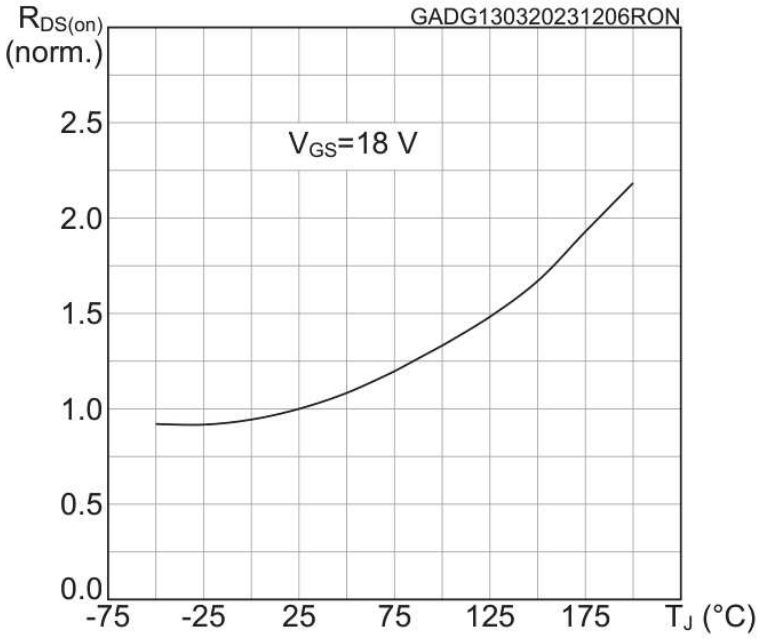


Figure 4.2: Relation between the $R_{DS_{ON}}$ and temperature. This graph has been taken from the data-sheet of the component adopted for this study case: **SCT070W120G3AG**.

Where L_{ch} andW_{ch} are the channel length and width of the channel region, same for the drift region where L_d andA_d are the length and area. The mobility of the channel is indicated by μ_{ch}, whereas μ_{nd} is the mobility of the drift region; and N_D is the doping concentration of the n^- drift layer. As the junction temperature increases, the channel mobility increases while the drift region mobility decreases. Furthermore it can be seen that at high drain current the differences between the resistance values at different temperature are markedly larger, that is attributable to the conditions where the effect of package-related degradation becomes more significant.

Same of the previous reasons can be addressed for use the threshold voltage V_{TH}; the trapping phenomenon is strong enough to make the V_{TH} unstable and unreliable, furthermore one of the main problem on the SiC MOSFET is the instability of the threshold voltage, thus it can not be used as TSEP. The formula [9] that describes the value of V_{TH} of a nMOSFET is reported in 4.4; where ϵ_{sic} is the dielectric constant, k is Boltzmann's constant, T_J is the junction temperature, N_A is the doping concentration in the p-type well, n_i is the intrinsic carrier concentration, C_{OX} is the specific gate oxide capacitance, q is the electric charge, Q_{ot} is the oxide trapped charge, and N_{it} is the interface trap density.

$$V_{TH} = \frac{\sqrt{4\epsilon_{sic} k N_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ot}}{C_{OX}} - \frac{qN_{it}}{C_{OX}} \tag{4.4}$$

This instability can be addressed as the following line of reasoning: when

the junction temperature T_J reaches high levels, the intrinsic carries density n_i drastically increases [21]: and in this condition, as shown in [9], the threshold voltage decrease as the temperature of the junction increases. The graph that shows this relation is the number 4.3, here is reported informations just for one sample, or better the average value, but in the reality the value of the threshold voltage has a large variation between the various samples. Furthermore, the value of V_{TH} is strongly linked with the ageing, due the degradation of the component; the accumulated electrons trapped in the gate oxide interface increases, thus the threshold voltage grows up too [4]. In addition, threshold voltage drift causes changes in the on-state resistance $R_{DS_{ON}}$ of the chip, which affects the on-state voltage drop $V_{DS_{ON}}$ and junction temperature T_J measurement.

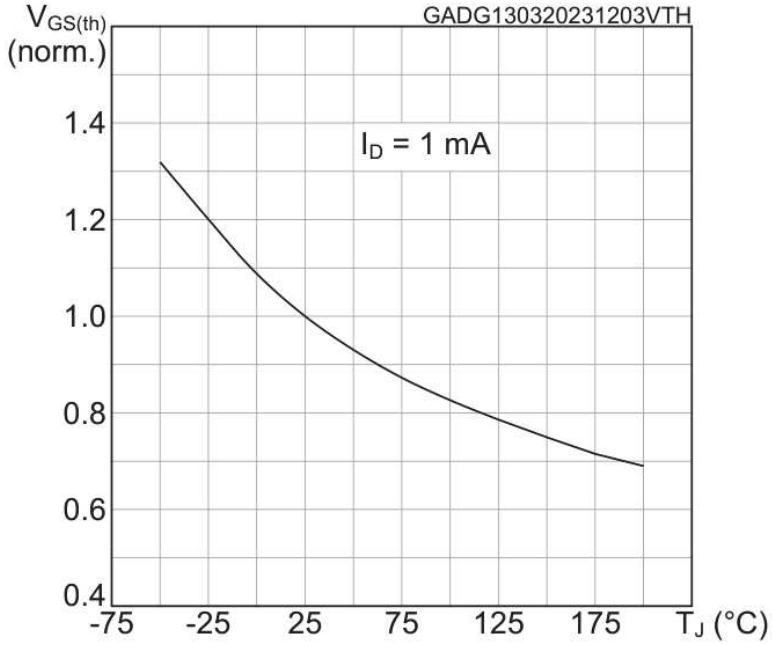
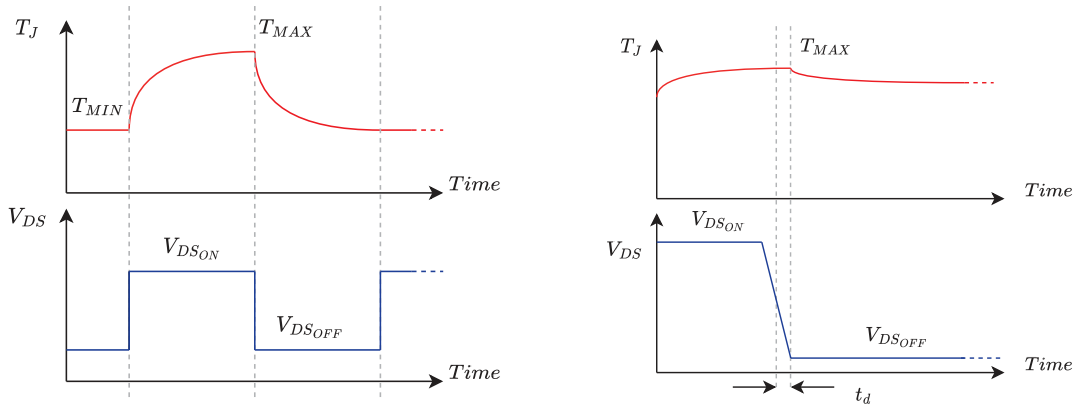


Figure 4.3: Relation between the V_{TH} and temperature. This graph has been taken from the data-sheet of the component adopted for this study case: **SCT070W120G3AG**.

The last possibility is use the inner body diode that is present inside the structure of the MOSFET, one example of its is reported in fig.4.1c, but in the contrary to a Si MOSFET, the SiC MOSFET gate-channel at $V_{GS} = 0\,\text{V}$ is not completely close, thus some part of the current can pass through the channel [15]; but this inconvenience can be solved applying a negative voltage to the gate to be sure that the channel is completely close; the negative value can be found extracting the calibration curve of the body diode, applying a negative voltage in the gate and forcing a small current pass through the inner diode, all of that is made during a sweep of temperature; this procedure have to be performed at different negative value of gate voltage, as long as the curve doesn't change anymore (same crossing point and slope). A good example of that can be see in [15] and in the next subchapter is which have been reported experimental results



(a) Diagram of different phases of the thermal characterization.

(b) Zoom in the commutation moment for the V_{DS} and junction temperature.

Figure 4.4: Waveforms of the drain to source voltage and the junction temperature.

found in the laboratory activities. The calibration curve is used also to extract the thermal coefficient of the body diode inside the SiC MOSFET, it is needed to calculate the temperature of the junction, that can be calculated starting from the V_{SD} which is sampled in very precise moments during the course of power cycling, to be precise the voltage of the body diode can be divided in two different parts, the V_{SD} *hot* and the V_{SD} *cold*, these nomenclatures are defined in this way to recall the status of the junction, or better, the temperature of its. As shown in fig.4.4a the junction has a maximum and minimum value, indicated as T_J^{MAX} and T_J^{MIN}, respectively; these two values are in correspondence with the V_{DS} (or V_{SD}) and as can be seen at the end of on-state of the MOSFET (when a high current level pass through the MOSFET and then the temperature rises due the Joule effect), the maximum temperature is reached and then it start to decrease. The temperature trend is exponential due the thermal impedance of the junction, that can be schematized in a equivalent RC (Resistance-Capacitance) electric model. The T_J^{MIN} can be any desirable value, it can be the ambient temperature, the temperature of a cooling plate set before the experiment, to have an appropriate temperature swing (as in this case study) or any different value that the junction reaches during the cooling. The sampling of T_J^{MAX} occur when the MOSFET is entering in the off state, because here in that point the load current stops to flow, so that the maximum temperature is reached; thus using the body diode to measure the temperature, the off state of the MOSFET is the only possible way to perform the measurement; the current that pass through the MOSFET is just a small current which creates a voltage drop that turn on the body diode and this happens just during the $V_{DS_{OFF}}$ as said, then the voltage in the *hot* point is sampled after a way short delay time after that the MOSFET starts to enter in the off state.

In the fig.4.4b the following approach is clearly illustrated. The same procedure of sampling the temperature can be applied for the T_J^{MIN}, in this case the

procedure is easier, because the MOSFET is in the off state and the body diode is still turn on, thus a very accurate timing as on the T_J^{MAX} is not needed, the sufficient thing is measure the voltage slightly before the MOSFET is turned on, so to be sure that the temperature of the junction has reached the minimum level. Once the two temperature have been sampled the temperature of the junction can be calculated using the formula 4.5 extracted from the calibration curve and an example of that is also reported on [5]. It is a first order line equation and the extrapolation of the junction temperature is very quick and easy.

$$-(V_{DS}^{hot} - V_{DS}^{cold}) = k \times (T_J^{hot} - T_J^{cold}) \tag{4.5}$$

It's important to bear in mind that the figure 4.4 reports just ad ideal behaviour of the V_{DS} because in the real world, the drain voltage is different, it is not constant during the cooling, it has a slope and the voltage across the body diode when the junction is hot is different than the voltage when the junction is cold, otherwise the temperature measurement would not be possible. Just to fix this aspect, since the thermal coefficient of the diode has negative value, the expected value of the V_{DS} when the junction is *hot* is smaller than the value when the junction is *cold*. Furthermore the PC test aims to find the life time of a component, the criterion used for assessing the end of lifetime of the component is the increase in the forward voltage drop V_{DS} by 5% measured at load current. Once the drain to source voltage goes above this value the component is considered damaged and the test stops. [14]. The most important parameter that has to be taken into account during the power cycling test is the junction temperature [12], as said before, this is because the degradation rate is faster when the temperature of the junction is higher and this is the reason of the breakdown of the components. Thus the temperature swing of the junction has to be carefully detected, in this study case the first power cycling test has been performed with a $\Delta T = 80\,\mathrm{K}$; and it is intuitively clear that decreasing the temperature swing, the number of cycles before the breakdown of the component rises. Further studies can be done with a smaller thermal swing, for instance with $\Delta T = 70\,\mathrm{K}$ or $\Delta T = 60\,\mathrm{K}$ but the number of cycles before failure could be large, that means a very long period could be necessary to perform the test [22]; and sometimes it is not worth it. Therefore, the power cycling test has been set to have temperature swing and it is set imposing a current load on the DUTs equal to a desired value and it is modulated to have a $t_{ON} = 2\,\mathrm{sec}$ and $t_{OFF} = 2\,\mathrm{sec}$, thus a square wave current load with a duty cycle equal to $\delta = 0.5$ [22].

Schematic The circuit deigned for the developing of this project is reported in fig.4.5 and as can be seen the circuit presents 6 MOSFET, 4 low power DC current source and one high power DC current source. The schematic circuit has been manufactured on a PCB board, but this aspect has precisely discussed below in the following next paragraph.

First of all, can be seen that the circuit is composed by two different legs, in this case we can call them differently to distinguish them, the left leg are defined as *phase A* instead the right leg is the *phase B*. Each leg is made up of three MOSFET,

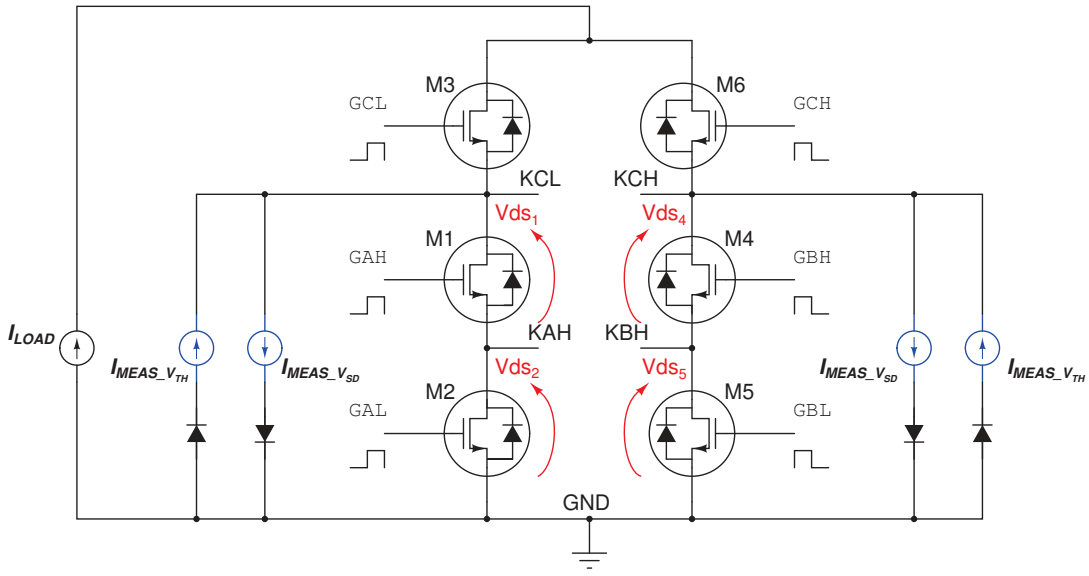


Figure 4.5: Electrical scheme of the entire measurement system adopted for the power cycling test.

for the the *phase A* the MOSFET are $M_{1,2,3}$ and for the *phase B* are $M_{4,5,6}$; the upper one is the control MOSFET, or better, is the MOSFET that is used to allow or to stop the flow of the DC load current, its task is to open the circuit to stops the high level of the load current in a well defined instant and to close it, to recreate a path for the current; the M_3 and M_6 are not DUT, they are not involved in the PC because the goal of this project is not perform PC also on M_3 and M_6, so they must have a current range a quite larger then the other 4 MOSFET ($M_{1,2.4,5}$), but this aspect are addressed in a more specific way later. To resume briefly the roles of each component: the DUT (device under test) in this project are, as could be guessed, $M_{1,2.4,5}$, they have a current ranking lower than the external switching ($M_{3,6}$).
The left leg and the right leg to allow a good functionality and to extract good results, have to be controlled in a very precise way; when the *phase A* turn on the *phase B* should turn off, thus they have to be controlled in phase opposition, that means the signals that controls the components on the *phase A* are shifted by 180° from the other signal on the *phase B* and this can be appreciated also in the fig. 4.5. On the gate pins of each MOSFET are reported the control signals and in the left leg when the gate signals are low, the gate signals in the right leg are high, but this feature has a point ot make, since the power load of this circuit is a DC current load, care must be paid to the timing that is applied to gate signals; because the current load, that is a current generator, it needs lo have always a close circuit to works properly, thus throughout the control of the two phases

particular attention must be taken that the current generator never sees an open circuit. A way to overcome this possible problem is to temporize the gate signal of each legs to have a overlapping, in fig.4.6 is reported the theoretical behaviour of the gate signals and as can be see the overlapping between the two signals are set equal to 50 µ sec, in this way the current load finds always a close circuit, so that its functionality is ensured.

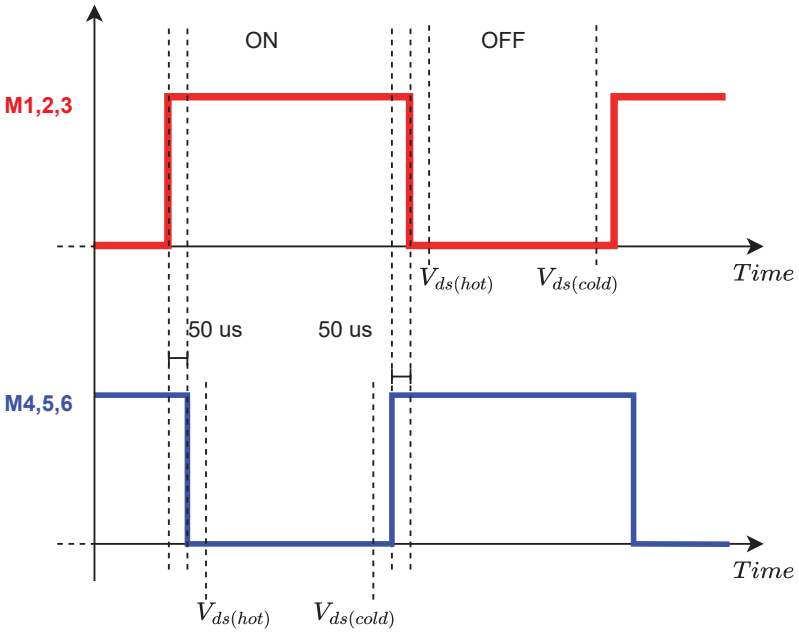


Figure 4.6: Gate signals with current overlapping.

However this waveforms are theoretical, then when the physical circuit are explained and this timing is accounted; furthermore in fig,4.6 are indicated the instant at which the V_{DS} are sampled to extrapolate the junction temperature. As reported in the graphs in fig.4.4, the junction temperature has two levels, T_J^{MAX} and T_J^{MIN}, but there's a proper moment to measure the the V_{DS} across the body diode and it is when the load current is interrupted and through the MOSFET just flows the small inverse current, named $I_{MEAS_{V_{SD}}}$, but this aspect of the functionality is well addressed after this chapter.
As is highlighted in the schematic in fig.4.5, the values that are sampled are the V_{DS}, during the functioning of the entire system the values across the drain to source are sampled by an ADC located in the main board (the role of the main board is well explained after). These sample points are fixed in the board and they can not be changed during the functioning of the circuit. They also have another purpose, during the measuring of the threshold voltage they don't need any change because thanks to the configuration adopted in the board, the same sample points are used to measure V_{DS} and V_{TH}, but this particular aspect are described later. Now can be just addressed the presence of the small DC current generator named $I_{MEAS_{V_{TH}}}$, it is present on the board just to allow the measuring of the threshold voltage; however the V_{TH} can not be measured using the sampling

connections indicated in the fig. 4.5, the gate and the drain must be connected together and a small current has to be pushed into the drain [14], as reported in fig.4.15, but this aspect is well addressed in the next part.
To resume the *principle of operation* of the DC-PC, a short overview of the main board functionality is needed, this can be easier of interpretation looking the waveforms in fig.4.6. The two legs are controlled in a complementary way, when the *phase A* is high, the *phase B*B is low, but a short overlapping is needed to ensure a path for the current provided by the load, because the DC-PC test has a load constant DC power current generator that push a high level current into the DUT ("high level" is relative to the DUTs, the current has to be higher enough to stress the component, so that to rise up its junction temperature). For now let's focus just to one phase: let's assume that the circuit is on steady state, when the MOSFET M_3 (M_1 and M_2 as well) turn-on the current load starts to flow also through the the *phase A*, because before was flowing in phase B, but just for a small time interval the load current is divided and it is flowing in the two legs; this is due the overlapping introduced in the control signals. After this small interval of time in which the two legs are conducting in the same moment, the M_6 (M_4 and M_5 as well) opens, thus the entire amount of the the load current flows thought the phase A and from this moment due to the high level of the current the junction temperature T_J of the DUTs start to rise. In the meantime, the small current generator $I_{MEAS_{V_{SD}}}$ is still working (the $I_{MEAS_{V_{TH}}}$ are used in a different situation). Once the signal gate on *phase A* changes from high to low, the highest junction temperature has been reached and the load current are not present anymore, the only possible current that flow through the DUT is the inverse current provided by $I_{MEAS_{V_{SD}}}$ that can exist due the presence of the body diode inside the MOSFET. In that precise moment the V_{DS} is sampled (that is negative). In this instant the drain to source voltage is referred to maximum temperature of the junction T_J^{MAX}. The small current is the only current that flows in the phase A during the t_{OFF} time and at the end of this time the sampled voltage V_{DS} is referred to the minimum junction temperature T_J^{MIN}; furthermore at the end of this span the *phase B* is turned on and after a short overlapping time the *phase A* is turned off and the cycle repeats.

The flowchart that explains the experimental chain of the DC power cycling is reported in fig.4.7, the entire system is controlled by PC which enable the control and sensing program inside a FPGA (field gate programmable array), then the main board is supplied by an external voltage source that gives the needed power to turn on all the components on it. All the control signal signal are delivered from the FPGA to the main board and its task is transform the control signals into a consistent signals to govern the adaptor, furthermore it is important to take in mind that the main board has two different tasks, one is delivers the control signal and the second one is to transform the signal extracted by the DUT and send them to the FPGA. After the main board there is the adaptor board, that its task is provide the connections to control the DUTs and the external switches, moreover it is used to sample the electrical informations coming from them. The adaptor board, since the system has been changed to works in DC mode, has

a direct connection with a DC current supply, that provide the needed current to stress the DUTs and it has 4 small current generators that produce the small current used during the t_{OFF} time, as explained above. All the DUTs and the external switches are placed on a cooling plate to control the minimum operating temperature of the devices.

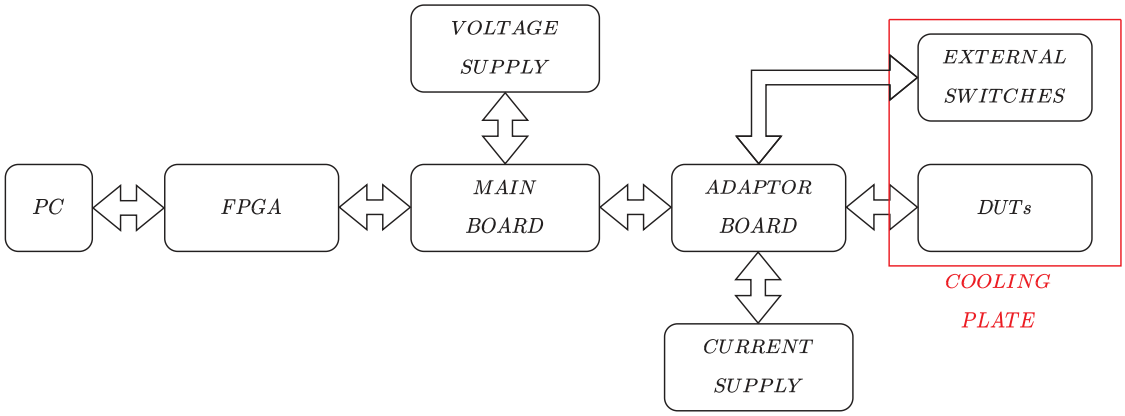


Figure 4.7: Flowchart of the entire DC power cycling system.

4.1 Measurements and parameters of interest

During this PC test the load current is always turn-on and the DUT is in on/off control mode to generate a certain junction temperature swing. An milliampere-level current is constantly flowing through the device and is used to determine the maximum junction temperature when the high load current is removed from the DUT by interdiction of it and to extract the calibration curve of the body diode. The temperature of the junction is a way interesting because high temperature within the material has a degrading effect on it and this leads to premature failure of the component. In this test, and in general power cycling test, the relevant and interesting value that have to taken under control are the junction temperature T_J, the drain voltage in each component V_{DS}, the gate signal or better the applied gate voltage V_{GS} and the drain current that pass through the DUT I_D.
The circuit configuration for measure the V_{DS} in the reported in fig.4.8, this circuit is the same for the *phase A*, *phase B* and this is the configuration during the t_{OFF} time. As reported in fig.4.4 and equation 4.5, the junction temperature is extracted from the value of the drain to source voltage. But before to be able to extract the junction temperature of the component one step before is needed and as said briefly above, the extraction of the calibration curve of the body diode is the key step. The calibration curve is a graph that has in the y-axis there is the body diode voltage of the MOSFET in a well defined condition, hence the current that is flowing through the body diode must to be constant and not variable. Its value

should be larger enough to create a voltage drop on the component, but not that much large otherwise the diode can be damaged. In the x-axis is present the temperature, to be precise the temperature of the junction T_J of the component. The span of it, usually goes from the room temperature, up to 140/150 °C; the shape of the curve extracted is a straight line and the equation that describes the curve is a normal first order equation: $y = mx + y_0$.

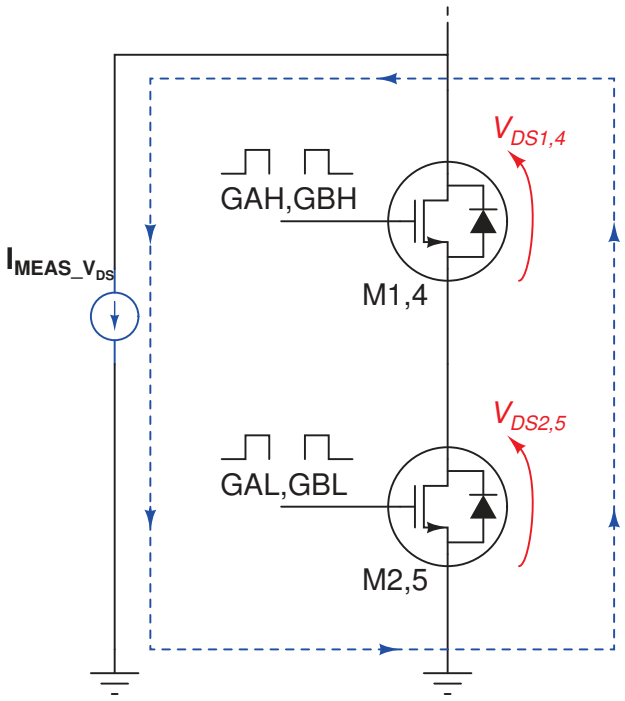


Figure 4.8: Circuit configuration for the measure of the diode forward voltage. The current direction is indicated with the blue arrows.

An example of calibration curve is reported in the figure 4.9, in which for simplicity are shown two different calibration curves and the only difference between them is the gate voltage V_{GS} applied during the extraction procedure. And as said in the previous chapter, the channel of the SiC MOSFET is not completely close at $V_{GS} = 0\,\text{V}$, instead this happens for the Si counterparts [9]; for that reason the value of the gate voltage, in both the cases, is lower than zero. But for now the interesting curve is blue dotted one, with the value of the gate voltage equal to $V_{GS} = -5\,\text{V}$. Furthermore, the equation that describes the curve is reported next to it and it can be used to calculate the temperature on every single moment during the t_{OFF} timespan, when the small inverse current, in this case is equal to 20 mA, is flowing. For instance, if the voltage measured on the body diode is equal to $V_{SD} = 2.4\,\text{V}$ and putting this value inside the equation of the curve reported in 4.6, the temperature of the junction can be extracted.

$$V_{SD} = -0.001578 \times T + 2.498 \tag{4.6}$$

$$T = \frac{2.4 - 2.498}{-0.001578} \simeq 62\,^{\circ}\text{C} \tag{4.7}$$

It is important to bear in mind, that in this case the temperature reported on the calibration curve is the temperature of the cooling plate on which the components are fixed, as can be seen in figure A.4; and to be sure that the junction temperature reached the same level of the cooling plate, the voltage of each MOSFET has been measured after a transitory time equal to 15 min. This aspect can bring some approximation in the final result extracted, as well as the temperature read of the cooling plate, because it was indicated on the screen of the cooler (Julabo Presto A40) was calculated by the software of it. Thus, the final temperature can be affected from approximations introduced during the calibration proceed.

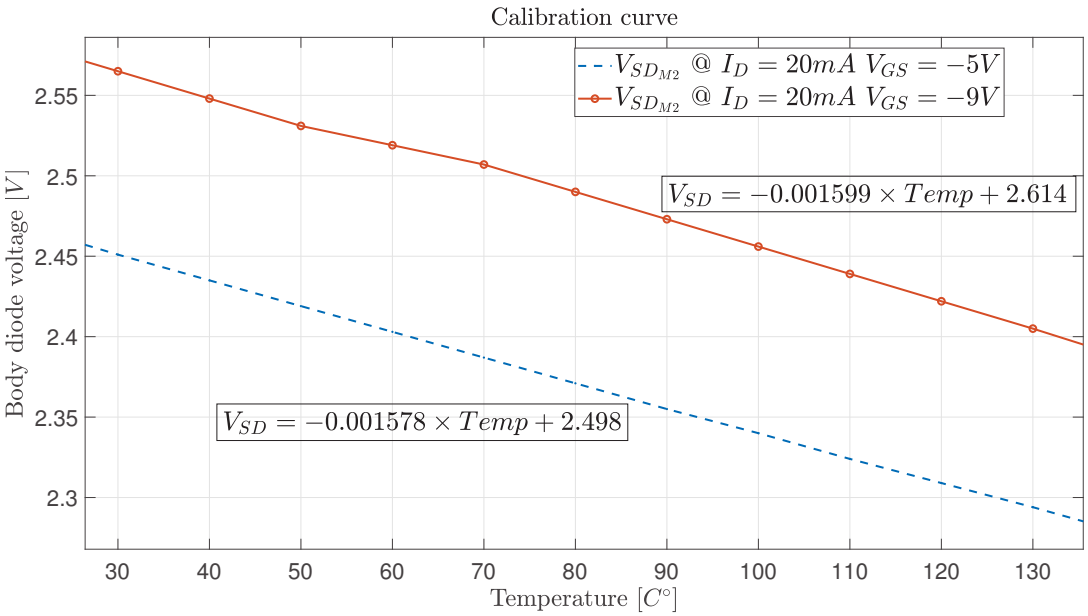


Figure 4.9: Calibration curve of body diode (component code SCT070W120G3AG) using as temperature reference the temperature indicated on the cooler (Julabo Presto A40) screen. There are the equation of the curves extracted by a fitting tool.

As has been addressed before, in the figure 4.9 is present another curve, the red one, that curve is the answer because the calibration is necessary in this type of experiments to use to body diode voltage as indirect thermal meter. The red curve is the calibration curve of the same component but with one crucial difference, the gate voltage in this case has been increased negatively, from $V_{GS} = -5\,\text{V}$ up to $V_{GS} = -9\,\text{V}$. That value has been selected taking into account the maximum negative voltage allowed by the component, that is $-10\,\text{V}$, then to have a safety margin the voltage selected was $-9\,\text{V}$, even though the recommanded negative controlling voltage is $-5\,\text{V}$. The temperature span is the same as before but, as can be seen the voltage measured on the body diode has markedly changed and this is the example of the problem addressed above in the beginning of the chapter, that the channel of the SiC MOSFET is not completely open at $V_{GS} = 0\,\text{V}$. This results bring on the light a possible issue, during the operation in body diode mode (see fig. 4.1c) not all the inverse current passes through the body diode,

but part of its goes through the channel and this happens if the channel is not completely open, so that the MOSFET is no longer working in body diode mode, but in inverse mode. *Thus, for the component under testing (SCT070W120G3AG) the recommanded negative working voltage is not enough to ensure the complete opening of the channel*. As for the previous case, an example how to extract the temperature from using the equation 4.5 in useful. Taking the same voltage measured across the body diode ($V_{SD} = 2.4\,\text{V}$), the temperature extracted of the junction is:

$$V_{SD} = -0.001599 \times T + 2.614 \tag{4.8}$$

$$T = \frac{2.4 - 2.614}{-0.001599} \simeq 134\,^{\circ}\text{C} \tag{4.9}$$

The results obtained from the calculation in 4.9 is in line with the graph 4.9 information.
Since the entire system and its accuracy is based on the temperature reached by the cooling plate, then the junction temperature, a good attention has to be put on the sampling of the real temperature of the junction. As said before the calibration curve needs to be as precise as possible, thus to overcome the uncertainty introduced by the thermal indicator of the cooler, two approaches has been adopted and the result compared. In both has been used an optical fiber customized to sample the temperature, the system is from the company OpSens Solution and the product is the OTG-PM. Furthermore, for this stage test the gate voltages have been set equal to $-5\,\text{V}$. Even though at that gate voltage, the previous experiment has shown the channel was not completely open, but it was compulsory to use $V_{GS} = -5\,\text{V}$ because the main board had not the possibility to goes lower level. The small sensing current was the same of previous experiment: $I_{MEAS_{V_{SD}}} = 20\,\text{mA}$. It is important to bear in mind that some issues emerged during this stage and between the first and second approach, the samples has been substituted. In the first one the samples were on TO247-*4 pins*, instead in the second approach the samples were on TO247-*3 pins*.

First approach Since, in normal condition, the DIE of SiC is surrounded by epoxy the temperature cannot be directly sampled by the thermal optical fiber, but if one component is dug, the DIE become more available to be touched by an thermal sensor. Thus in this first approach, one component has been dug using a dedicated equipment in Aalborg University, with a power laser, the epoxy that was on the front side of the component has been excavated. The laser has been stopped when the first connector pad, at which the bonding wires are soldered, was visible and this particular aspect can be see in the figure 4.10; one interesting thing that can be observed is that the two thick bonding wires on the left, in which the thermal optical fiber is posed, are the source bonding wires that connect the pins of the MOSFET to the DIE. Instead, the two thin bonding wires on the right of the picture are the connection for the kelvin source pin and the source pin. In the figure 4.11 are reported the calibration curves on each single component. Each MOSFET due the manufacturing procedure has its own response of the body diode,

and in the graph 4.11 this aspect can be seen very well. Looking always the component number M2 analysed above, fitting the curve measured and extracting the values of the mathematics equation that describes its behaviour, the calibration results have a small variation compared with reported on figure 4.9; the new result for M2 is $V_{SD} = -0.001812 + 2.502$.

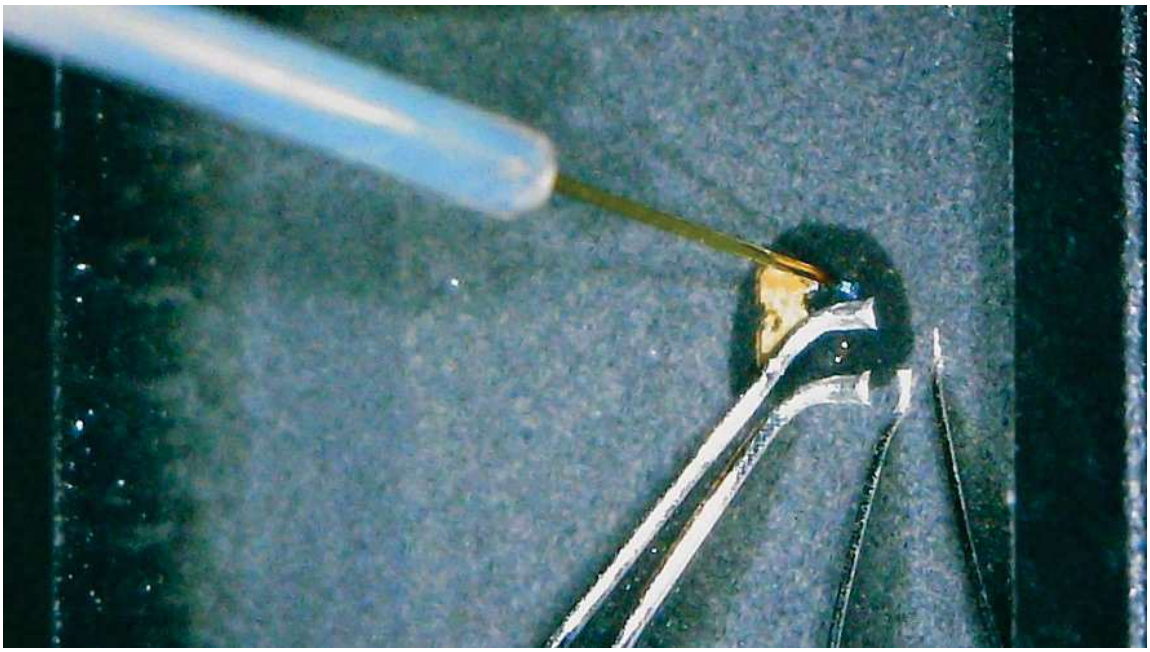


Figure 4.10: Zoom of the thermal optical fiber used to sample the temperature of a MOSFET in which a hole had dug by using a power laser.

Furthermore, all other components have been subjected of small variations of them previous values. This effect can be traced back to the different temperature measurement methodology.

Second approach In the previous approach, the basis was the excavated box and the available pad, in order to get as close as possible to the DIE; but that approach is too invasive and it involved the destruction of the component, or better, if the component was used just one time the extract the characterization curve of the body diode, that approach was reliable, but since all the components of this project are installed, moved and shipped plenty times throughout the duration of the tests, create a dig in the components was not reliable and doable. Therefore, a less invasive way to sample the temperature of the component then, of the junction, has been adopted and the second approach is still based on the revelation of the temperature by the thermal optical fiber. Furthermore, as said above in the summary before the description of the two cases, the samples used with this second approach has been substituted, and the component now have the TO247-*3 pins*, then the calibration curve that are reported below are different from those one shown on the first approach. Therefore, the connection and the sampling setup of the thermal optical fiber are reported

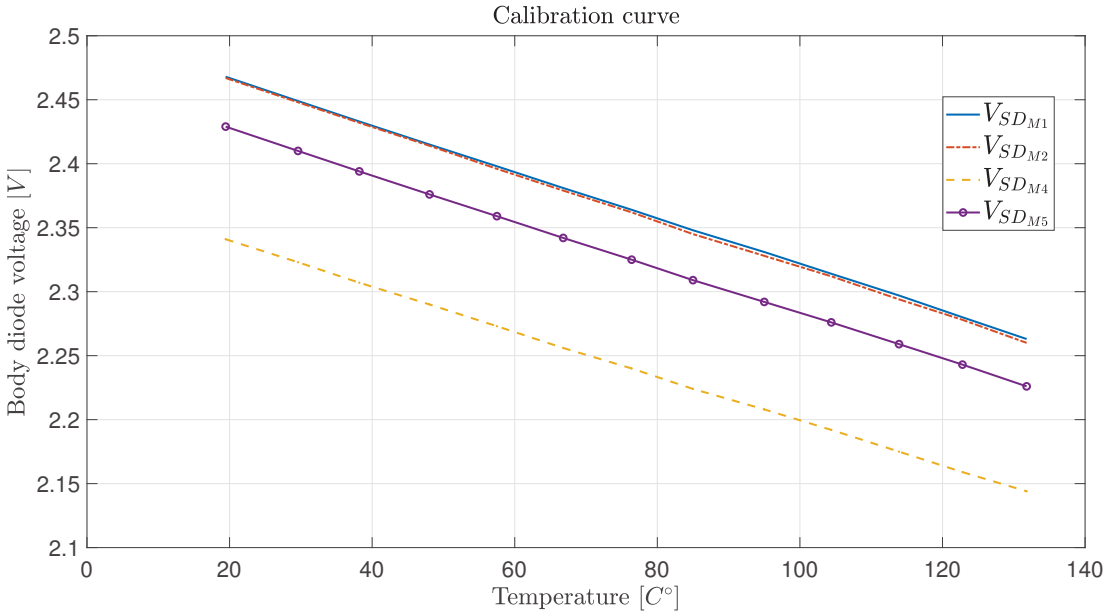


Figure 4.11: Calibration curves of 4 DUTs extracted using a thermal optical fibre touching the source pad of the excavated component as a temperature gauge. All the curves have the same measurement thermal condition and samll current that pass through them.

in the figure 4.13. Here the sensor are posed in a dig filled by thermal paste and it is created on the cooling plate. The position of the hole is central compared to the 4 DUT, this to take into account the possible thermal distribution of the heat. The thermal material helps the heat conduction between the sensor and the cooling plate, it has been done to ensure the best coupling, because the air is not the best means of thermal conduction and it has a higher impedance compared to the thermal paste. The results of those calibration curves is reported in figure 4.12, and can be seen that the values on the y-axis are way more different compared to the *4 pins* components. The equation of the new curves are slightly different, as values, and they are M1: $V_{SD} = -0.001591 + 2.391$, M2: $V_{SD} = -0.001533 + 2.304$, M4: $V_{SD} = -0.001528 + 2.292$, M5: $V_{SD} = -0.001506 + 2.291$.

In this case a further analysis has been done and it was based to the fact that the gate signal, during the normal functional working, is not constant as during the calibration procedure, then the entire system has been controlled to work as in a normal condition ($t_{ON} \simeq t_{OFF} = 2\,\text{s}$), then the main board provided (the gate drivers are the part of th board that send the signals to the gate of the MOSFET) the maximum possible voltage level on the gate pins. The maximum voltages available on the output of the gate driver are $V_{GS_{MIN}} = -5\,\text{V}$ and $V_{GS_{MAX}} = 18\,\text{V}$. This experiment has been performed taking into account the gate-channel trapping procedure and the defects present on oxide, the that occurs during the functional working time. The results found are not reliable and not usable to extract any possible data

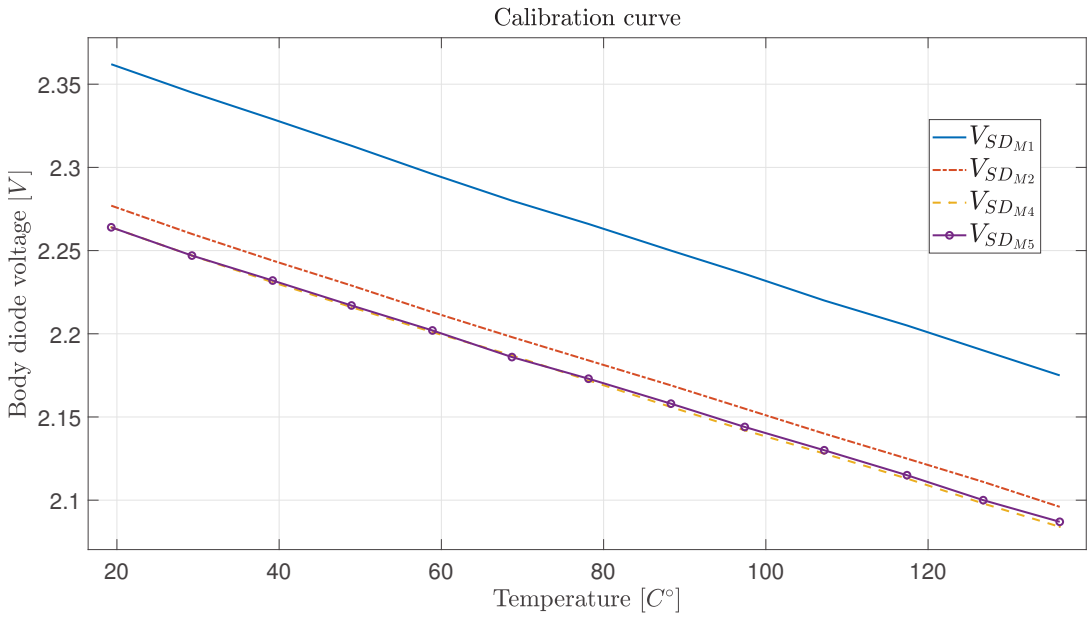


Figure 4.12: Calibration curves of the *3 pins* components. The sensing current is still equal to 20 mA and in this case the thermal sensor has been put in a dig next to the central component.

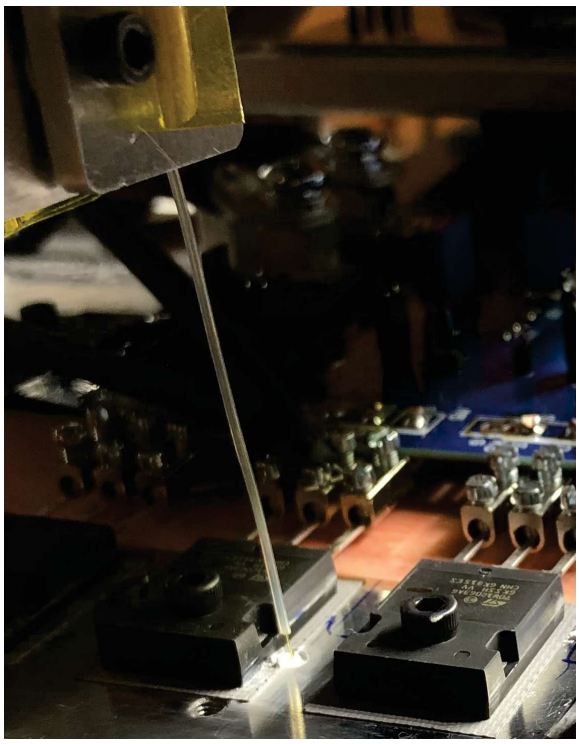


Figure 4.13: Connection of the thermal optical fiber in the second approach, in which can be seen that the components have *3 pins* and the sensor is posed next to the central one.

or calibration curve, the graph can be see on figure 4.14. Thus, during the calibration curve extraction the only possible way to have good results is to use a negative constant voltage on the gate.

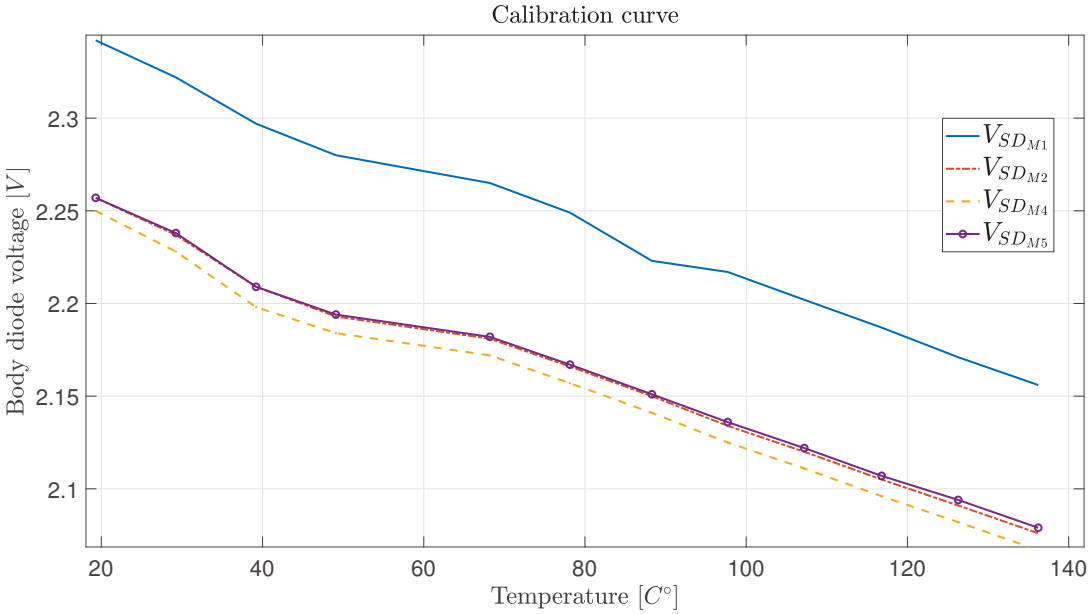


Figure 4.14: Calibration curve extracted with the gate signal not constant equal to a negative voltage, but variable between the maximum and minimum available values provided by the gate driver for a time equal on the same level.

Another important parameter in the SiC MOSFET is the threshold voltage, its value is unstable due to the trapping of electrons in the channel and in the oxide, as reported in literature [18], [21], [31], [32], [26]. The circuit configuration that allows to measure the V_TH is reported in fig.4.15. As can be seen, the drain and the gate are at the same potential and a small DC current $I_{MEAS_{V_{TH}}}$ is pushed into the drain pins of the MOSFET, because they are connected in series, then the current is the same in both the components. It is important to bear in mind that the following measure can be performed just when the power cycling test is not running, because the configuration of the circuit has to be changed and the dedicated current source has be turned on. The necessary modifications to the circuit are discussed in the next subsection. The configuration of the measuring circuit has been selected to be consistent with that one reported in the data-sheet published by the manufacturer [29]. The producer shows that the standard to measure the threshold voltage is to short the gate and the drain together, then a small current is allowed to flow through the MOSFET. This measuring system has been adopted too in this study case, it has been done to compare the results with that one found in the data-sheet. Furthermore, the standard to measure the threshold voltage is well defined as can be see in [32]. Moreover, looking the figure 4.15 the gate and the drain are shorted together, then the problem that seems to emerge is the the sample point, to measure the voltage. But, bearing in mind that

the sample points before were connected on the drain and the source, now the gate is shorted with the drain and the source is still there, thus the connections didn't need to be changed and with the same measuring equipment present on the main board, the V_{TH} can be sampled. In the data-sheet [29] of the component, the threshold voltage is the voltage that is measured between the gate and the source pins when the current flows into the drain is equal to 1 mA. This extraction method is also reported on [18].

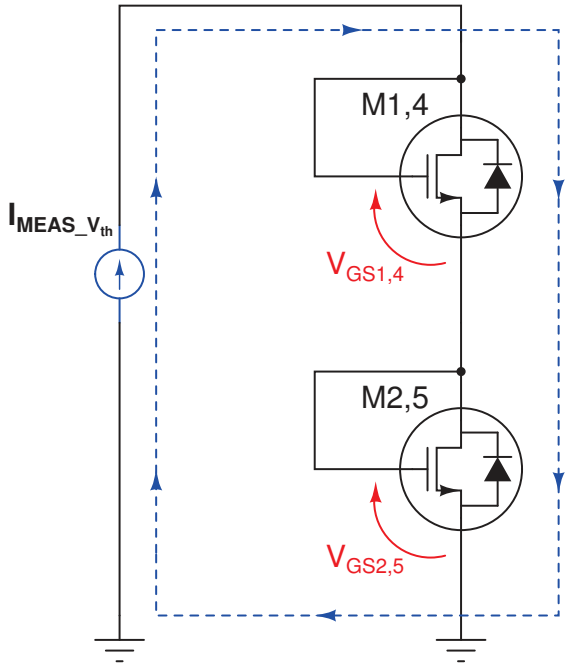


Figure 4.15: Circuit configuration for the threshold voltage measurement. The current direction is indicated with the blue arrows.

As reported in the chapter 3 the threshold voltage is one of the most interesting parameter during the characterization step. And in the histogram 4.16 is reported the the distribution of threshold voltage of the selected 45 samples. The data has been extracted during **ISLE/ECPE project 2024, measurements performed by Alter Technology France**. The distribution of the values follow a semi bell distribution and as it can be seen, their values are still inside the range reported from the manufacturer on the data-sheet. The ranges of the data-sheet are quite large to incorporate the maximum possible variation of the values, during the manufacturing process.

4.2 Adaptations of equipment

In the market exist a lot of DC power cycle machines, in which all the needed features are embedded inside them, one of those machine are present in Aalborg university and the brand of its is Mentor Graphics and it is a expensive commercial equipment. For this project the commercial DC power cycling equipment has not

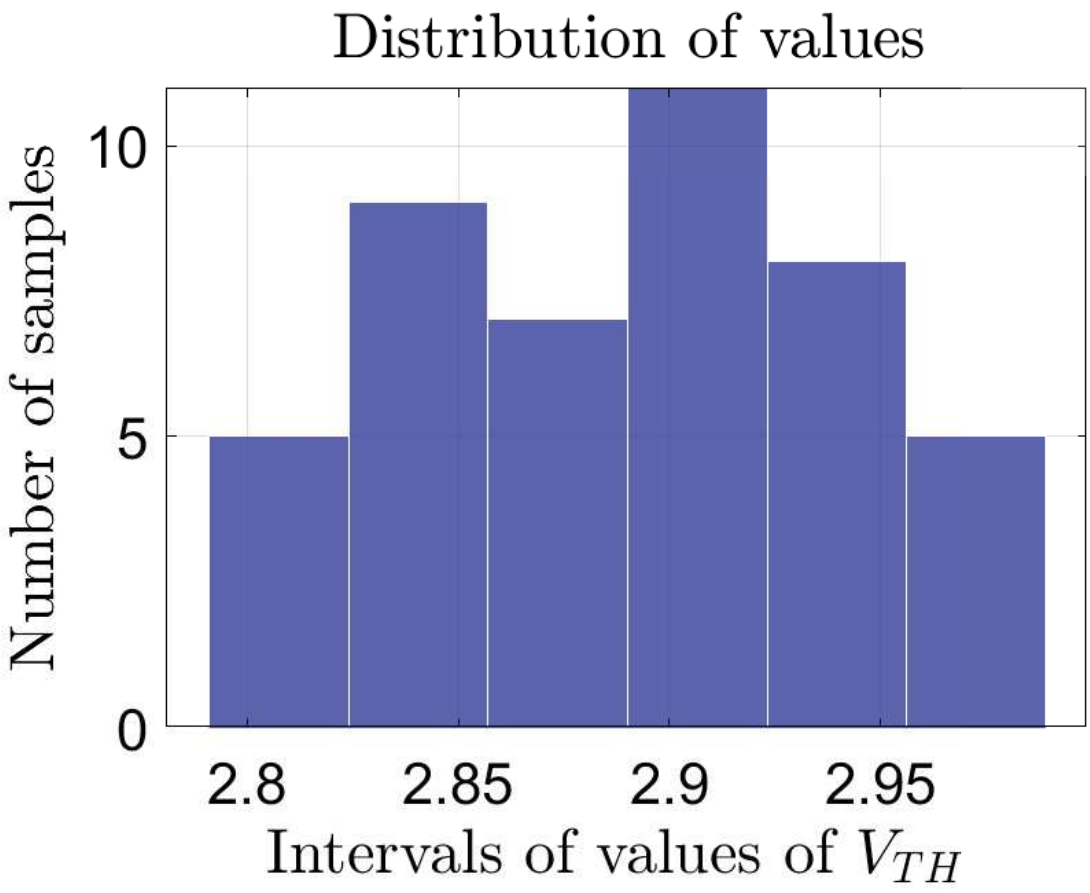


Figure 4.16: V_{TH} values extracted from the selected samples. The sampling conditions are well reported in the subchapter 4.1.

been used due to the luck of its availability, because in AAU are present just two machines and the availability are strictly reduced and the waiting list for use them is pretty long; thus to overcome this problem, also for a future necessity, a solution has been found: adapt an AC power machine to work in DC mode. Saying it in words may seem easier than doing it. This choice brought some troubles and delays in the project developing, but the main point that deserves attention is the needed to adapt the main board to work as a DC power cycling board with DUTs that use the TO247 package, to be precise the TO247 *3 pins* and TO247 *4 pins*. Therefore, the main characteristics required for the adaptor are:

A Possibilities to perform DC power cycling in to different packages of TO247: TO247 *3 pins* and TO247 *4 pins*.

B Embed a DC current source in the board to measure the V_{DS}, so to use an indirect temperature measurement: the body diode inside the SiC MOSFET.

C Embed a DC current source to measure the V_{TH} during well defined moments throughout DC power cycling, to do that physical changes in the circuit was needed.

D Allows parameters of interest during the DC power cycle to be measured intelligently: measuring qualities with the lowest possible noise and highest possible accuracy.

A short explanation follows for each point addressed above:

A To overcome this particular request a new footprint has been developed, as reported in chapter 3 a 5 pins footprint is explained, in fig.3.4 it is reported. This footprint allows to install in the adaptor devices that has different TO247 packages: TO247 *3 pins* and TO247 *4 pins*.

B The DC current source to measure the V_{DS} is developed and placed in the adaptor board is reported in fig.4.17. The upper component **LT3092** is used to create the current that is needed to measure the voltage across the MOSFET during the t_{OFF} and from that, calculates the temperature, as described by the eq.4.5. The following component has been selected for its good linearity with the temperature, since the adaptor board is arranged above the cooling plate and for its output current (maximum 200 mA but minimum 300 µA). The current was set equal to 20 mA to be sure that the voltage across the was as high as possible to be measured. Furthermore the diode D2 in the left-hand side of the schematic has been positioned so that the current can only flow in one direction, as reported in fig.4.8. To allow the correct operation of the current source, a minimum voltage across its has to be ensured, for that reason a voltage equal to −12 V is applied; taking into account that the current must flow out from the DUTs and the point at which the current source is connected can arrive around 4 V. The complete circuit can be see in the appendix A in fig.A.6.

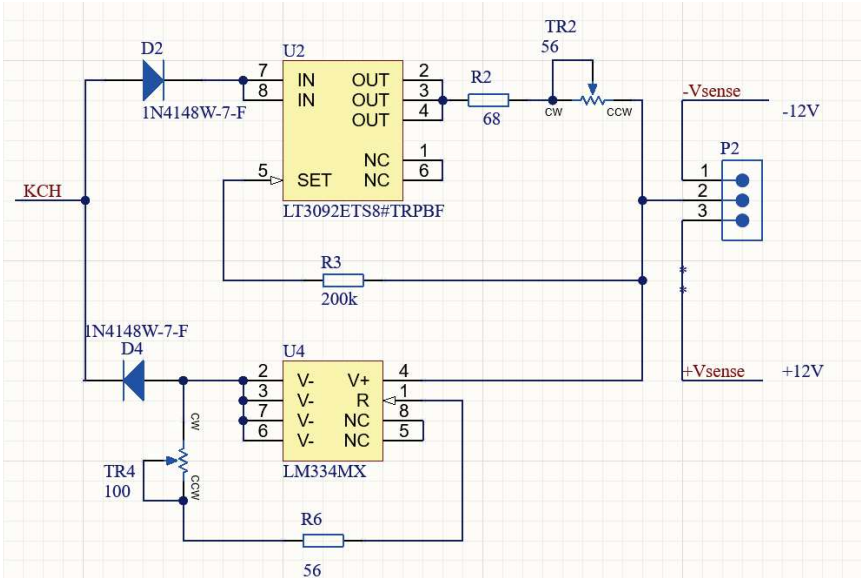


Figure 4.17: Real electric schematic configuration adopter for the current sources.

C For the DC current source used to measure the V_{TH} a dedicated chip has been used, the **LM334**, it can be see in the bottom side on fig.4.17. It was chose because it has a programmable range (from 1 µA up to 10 mA) that fits with the needed current. Changing the passive component that are connected to the LM334 the output current can be changed; in the first step the current was set equal to 10 µA but to be consistent with the data-sheet of the producer [29] it should be rose up to 1 mA. Here the diode D4 has been placed for the same reason of before, so that the current can only flow in the desired direction; in this case the current must flow in the circuit, as reported in fig.4.15. Here since the current must flow in the circuit the voltage across the regulator must be applied in a different way, now the voltage is 12 V, and as can be see in the schematic in fig.4.17 a jumper is present and trough its the desired voltage can be changed; changing the jumper position the required DC current source is activated.

D The aspect concerning the measuring and the transport of the information of interest is quite important. Since the frequency of working for the system is not high ($t_{ON} = t_{OFF} = 2\,\text{sec}$ then $f_{DC-test} = 0.25\,\text{Hz}$) the problem of the stray inductance and capacitance is not largely predominant, but still the circuit rooting presents some attentions about that. Looking the fig.4.5 in which are indicated the names of the nodes of interest in the circuit, they are present on the upper side of the DUTs (KCH and KCL)component, on the central point (KAH and KBH) and on the lower side (GND). Taking in mind them and looking the fig.4.18, the same name are reported to highlight the routs reported in the image 4.5. This has been made to show which was the approach to ensure a very precise measurement mode and to minimize the stray inductance of the circuit, then to be able to extract, in the best possible way the relevant informations from the circuit. An anticipation of the adaptor board design is that it is composed by 4 layers, the two external layers are made to conduct the high current (they are the thickest on the board) and the inner are used for the signals (they are the thinnest on the board); but as can be see in fig. 4.18, the measuring routs has been developed in the two closer layer, to be precise, using the top (first) and the second layer, so that the distance between the copper routs is smaller. Then to improve the robustness against noise the routing has been carried out in this way, knowing that the left leg has at the upper side KCL, the center is KAH and the low side is GND, a good approach is to route the upper and lower side as closer as possible and them should be surrounded by the central node, this should be done for all the length of the routs and split them as closer the starting and final point as possible, so that the voltage drop is the same along the length of the tracks; and in case of interferences all the routes would be involved by that, then the differences measured from each sample points could be unchanged.

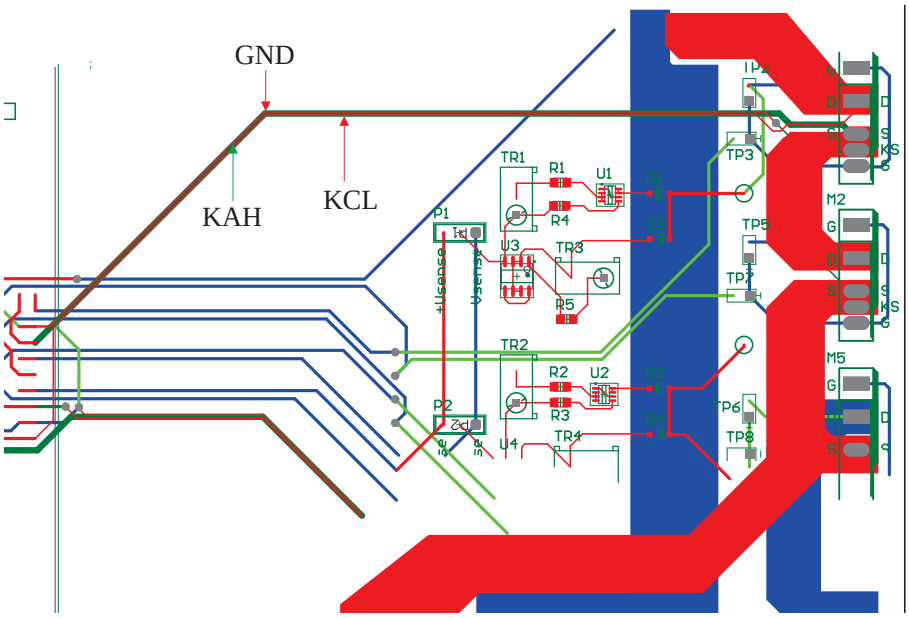


Figure 4.18: Enlargement of PCB board with tracks of interest highlighted.

4.2.1 Adaptor

The adaptor board, as reported above, must have some features that have to take into account during the developing. In fig.4.20 is reported the final version of the adaptor and a simplified diagram is shows in fig.4.19, it is used to figure out better which are the interesting parts and the locations of them on the board. The board can be resumed in small subspaces, the central part has been used to allocate the embedded current sources, instead the edges were developed to allocate the connectors or the external parts. But a better zoom of each part is crucial. In the left-hand side of the board can be found the SAMTEC® connector which has been adopted to be consistent with the type connectors used in the main board, it has 40 pins dedicated for the low power connections (located in the central part of the connector) and 8 pins for the high power connections (located in the lateral part of the connector, in this case are not used because the external current load is provided by an external generator and it is independent from the main board). The low power pins are used for the gate signals of the gate control of the devices, for the sample connections (test points) and to supply the current source.
In the central part are present the 2 symmetrical circuit, the current sources: the upper one provide the current for the left leg (*phase A*) and the lower one for the right leg (*phase B*) and in the left-hand side of the both current source circuit are present 3 linear pins header connectors, that as mentioned before they are used to select which current generator has be to be used. The resistor trimmers (blue components) are used to precisely set the current value of each source, this procedure has been done during the debugging of the board and it must to be

done as accurately as possible because the values read on the body diode are directly linked with the values of these current.
The power line, in the bottom side of the figure, is the connectors used to connect the external DC current load to the circuit, they are two large pads on which the power cable are secured through a dedicated clips. They have a crucial aspect also for the safety, because through them a high current flows and they must to be able to withstand at very high current levels.
The external switches are in the outer parts of the board, in the top and in the bottom side; they are the M_3 and M_6 MOSFET reported in fig.4.5. The position of them are not casual, they are located there to be not much far away from the DUT, otherwise the distance between them and the DUT could be a problem for the parasitic factor.
Last but not least, in the right-hand side of the board are located the DUT, the SiC MOSFET under test. As mentioned before it has been used the 5 pins footprint developed during the case study, which it allows to connect two different packages, TO247 *3 pins* and TO247 *4 pins*, and perform the DC power cycling on them without any changes on the circuit, furthermore the devices under test can have different packages also during the same test, then the board can be used in a very flexible way.

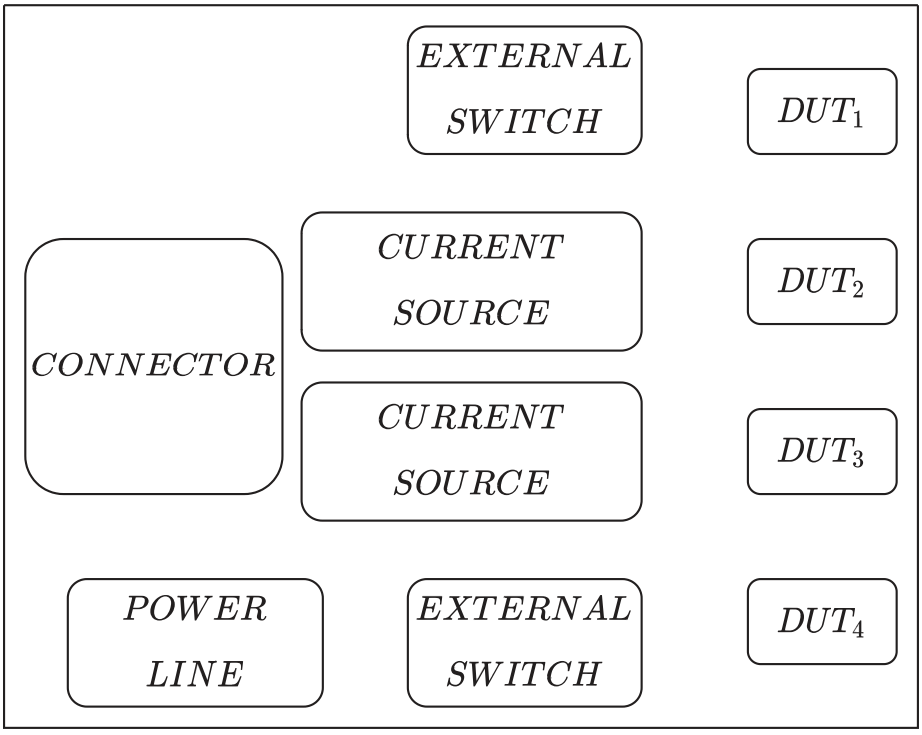


Figure 4.19: Schematic of the PCB adaptor board.

The holes of the dedicated footprint have a larger size compared with the normal dimensions indicated on the mechanical part of the datasheet that are

reported from the manufacturer. This feature was done to allow a easier change of components, since the board is designing to work for long time, this involves that the power cycling test can be performed in a very high number of samples and since they are soldered on the board, the larger holes are useful for easy soldering and desoldering of the components.
As reported above the layers of the entire board are not commonly two, but it has been designed to have 4 layers. The introduction of 4 layers bring quality into the board as the capability to divide the power layers from the signal layers and the facility to route the connections. A precise description of the layers is reported here:

- The two external layers, the bottom and the top layer are primary used to conduct the high power current, thus their thickness are higher than the internal ones, and they are equal to 105 µm (or expressed with quantity of copper on a surface 3 $ounces/foot^2$). It is the maximum commercial thickness that normally can be found on the board. Obviously, different and thicker layers can be made but for most of the board on the market this thickness is sufficient.

- The inner layers are primary used for the control signal, thus for the signal connections and they have thickness equal to 35 µm (or expressed with quantity of copper on a surface 1 $ounces/foot^2$). To be precise, some of the signal route pass also in the external and thicker layer, but just for a small part.

The power paths have been made larger enough to support the high DC level current provided by the external DC current supply. The board reported on figure 4.20 is the adaptor and all the components mentioned above can be seen; but the external switches, in the reality, are not positioned in that way and the real position can be seen on figure A.5.

Furthermore, on the figure A.5 can be seen the way of connection between the DUT and the adaptor board. Before has been said that the holes of the new footprint have a larger size than the normal footprint, this to allow easily the soldering and the de-soldering of the components on the board, but since the power cycling test has to be performed on a large number of components throughout its working time and that after the stressing test the DUT has to be characterised one more time by the partner university, a further implementation has been done. Instead of holes, clamps have been placed on the board, so that the components don't need to be soldered and they are less damaged during the tests. The main reason is because the IRT SAINT EXUPERY (the partner university) during the short-circuit test they use a particular connector composed by two plates, in which the component is positioned in the middle and the pins of its pressed against the flat surfaces of the plate; that connection between the DUT and the plates has to be as perfect as possible, to ensure the repeatability of the test and its reliability.

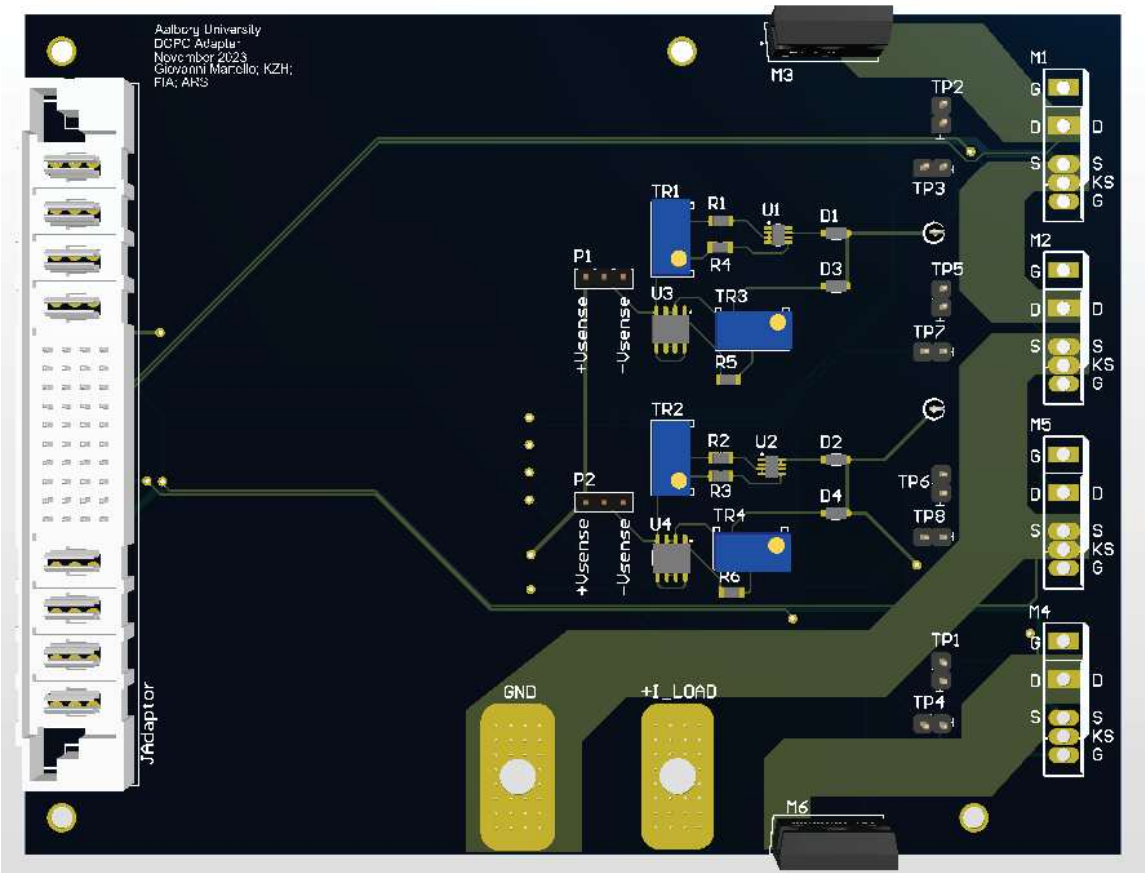


Figure 4.20: PCB adaptor board.

4.3 Results and waveforms

The entire board is controlled by an FPGA which it communicates with a PC. The controlling program is based on a National Instruments ^{TM} system and the functionality of the program is not businesses on this thesis work, then the goal for now is to analyse the functionality of the board, all the timings of the signals that are delivered from the main to the adaptor board and the sampled signal measured on the adaptor. The first step of the project was the debugging of the board and it takes a very important place in the entire project progress. First of all, the entire number of connections has been checked using a tester, this to guarantee that all the electric tracks were made in the correct way and there were no issues and errors during the manufacturing process of the board (the boards were made in China from a specialized company: XNJPCB). After that the embedded current sources have been tested and some issues rose up. The calibration of the sources was tricky, then the values of the component (resistance) have been modified. Then the calibration was more easy and all the embedded current source has been calibrated to have the desired value. To remind it, the current source for the extraction of the body diode voltage is equal to 20 mA and the values for that one used for the threshold voltage is 1 mA. Then the board has been populated with the DUT and the external switches and mounted to the

cooling plate with a silpad to isolate the iron plate with the back of the DUT (see fig.A.4), because in those type of package the back of the component has a small plate surrounded by the epoxy of the component and it is connected to the drain, then to be able to dissipate the heat created from the component it has to be posed on a cooling plate and said above to avoid catastrophic short-circuit the silpads have been adopted. In this step for each legs (they are the *phase A* and *phase B*) just the current source dedicated for the V_{DS} measurements are turned on and the jumper to short-circuit drain and gate disconnected. Then the situation is similar to that one reported by the circuit reported on figure 4.8. The gate signal coming from the control program and transformed into a physical value from by the main board, is sampled by a oscilloscope are reported in figure4.21, as can be see the gate voltage are between $-5\,\mathrm{V}$ and $19\,\mathrm{V}$ and they are consistent with the set values, as expected. Furthermore, the overlapping of the gate signal is checked, to be sure that the timing was correctly set and this still can be seen on figure 4.21. From the initial condition of the test the overlapping time must to be equal to $50\,\mu\mathrm{sec}$, this was chose to ensure a close circuit for the current load generator; as can be seen from the cursors it is correct and it is perfectly equal to $50\,\mu\mathrm{sec}$.

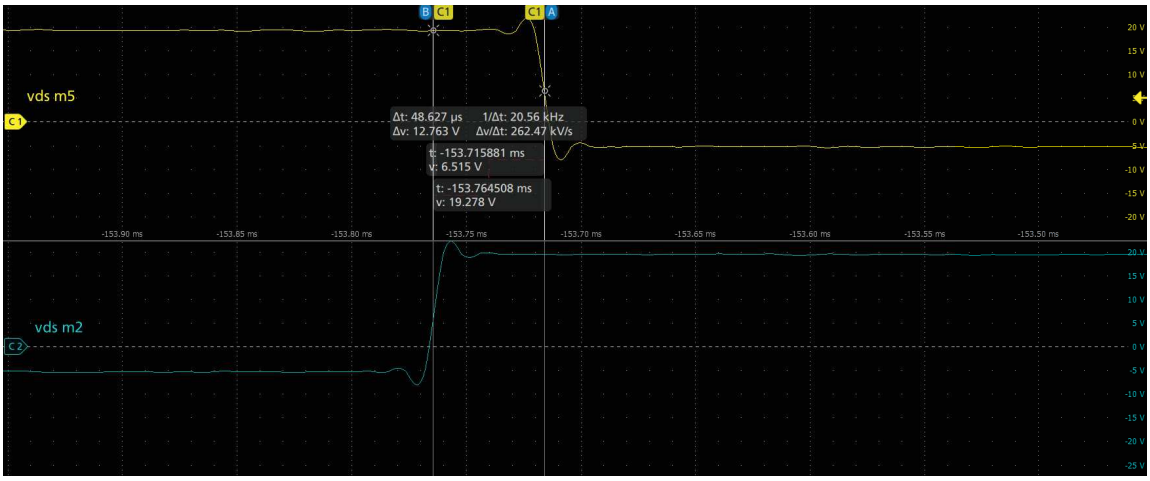


Figure 4.21: Gate signal sampled on the PCB board with an oscilloscope. The BH signal is coming from the right leg and AH from the left leg of the circuit

Once controlled that the gate signals and the current source had the right values, the first low current power cycling test has been performed, with load current equal to 10 A. The graph of this is try is reported in figure 4.22. At first glance this graph does not tell much, but analysing it closer it is full of answers. Firstly the component M4 is on the right leg and it is controlled in anti-phase with the left leg; during the t_{OFF} time the only possible current that flows through the right leg is the $I_{MEAS_{V_{SD}}}$, then the voltage measured can be only conductible to the intrinsic body diode and as it can be seen on the graph the voltage during the t_{OFF} time is almost equal to $V_{DS} = 2.4\,\mathrm{V}$. The result is completely consistent with the values found during the extraction of the calibration curve and the informations provided by the manufacturer on the datasheet. Moreover, the value during the t_{ON} is important as well, because the value of the voltage drop, during that

portion of time, is conductible to the product between the value of the on-state resistance and the current that are flowing. Since the current is known and the nominal resistance as well, the counter-calculation can be done.

$$V_{DS}\Big|_{t_{ON}} = I_{Load} \times R_{DS_{ON}} \tag{4.10}$$

$$V_{DS}\Big|_{t_{ON}} = 10 \times 64e^{-3} \simeq 0.64\,\text{V} \tag{4.11}$$

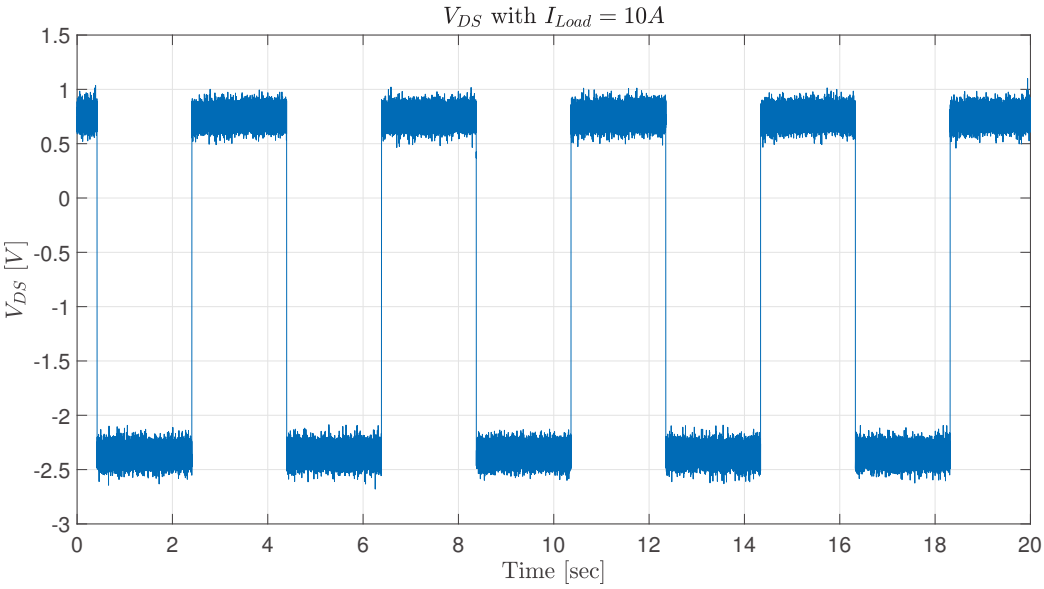


Figure 4.22: Drain to source voltage of the component in position M4, with a current load equal to 10 A. From this graph can be seen that the small current source during the t_{OFF} works properly.

The calculation is consistent with value measured on the DUT. The average value on the figure 4.22 is around 0.65 V With the current load the overlapping is still important, then a check is necessary. The graph that shows the overlapping also in this condition is reported in figure 4.23 and as it can be seen during the overlapping period the voltage drop across the MOSFET is almost the half than the normal condition; because during the overlapping time the current that are flowing into the leg is the half than the normal and then the voltage drop is divided by two. Furthermore, looking the data tips reported in the figure, the overlapping period is almost equal to 50 µs that is consistent with the project data.

Increasing the load current, the expectation is pretty clear; taking the gate voltage at the same level and the temperature of the environment sill constant, the voltage across the MOSFET V_{DS} obviously rises. But since the current and the voltage are increased, also the power dissipated must rise due the Joule effect, then the junction temperature changes and increases its value. It start from the ambient temperature when the MOSFET is in the off condition (during the t_{OFF}) then when turn in the on-condition (during the t_{ON}), its temperature arrives at

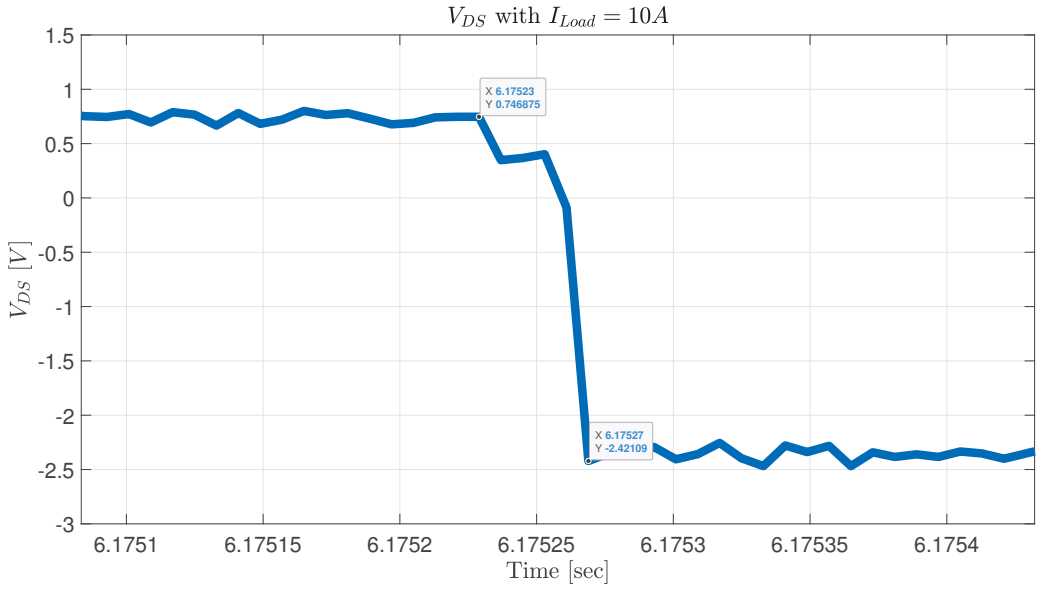


Figure 4.23: Zoom of a commutation instant of the previous graph 4.22, in which is highlighted the overlapping time.

some values, that is directly linked with the dissipation parameter (V_{DS} and I_D). The growth of the temperature has a second effect; looking the figure 4.2, in which are reported the relation between the on-resistance ($R_{DS_{ON}}$) versus the junction temperature (T_J), it is clear to see that at the increase of the junction temperature, the on-resistance rises; then what can be aspected is that during the t_{ON} with a high current that are flowing into the MOSFET, the initial V_{DS} is obviously higher then the case with lower current, but right after the initial value, it begins to grow. Instead, during time t_{OFF}, as the temperature of the junction is increased until the end of the switch-on time, the first value of the body diode voltage is different than the last value that can be read at the end of the t_{OFF} time. As reported before and in the previous sub-chapter, the thermal coefficient of the inner body diode of the MOSFET has a negative values, that means when the temperature increase, the value of the voltage across the body diode decrease, it became smaller. This effect can also be observed in the figure 4.24, in which the waveform has a negative slope during the t_{OFF} time. And to resume: at the end of the t_{ON} time the junction temperature is higher, that the ambient temperature, then the voltage across the body diode is smaller compared to the value sampled at the end of the t_{OFF} time. All the aspect described in the last sentences are refereed to the figure 4.24, in which is reported the behaviour of one sample with a current load equal to 15 A.

Increasing even more the load current the effects described before became stronger. Imposing the current load equal to 20 A, the temperature of the junction strongly increases and the slope of the waveform during the t_{ON} becomes more inclined, due to the increases of the resistance during the ON state, $R_{DS_{ON}}$. Furthermore, the voltage of the body diode becomes smaller, due to the negative thermal coefficient of the inner body diode of the MOSFET; this aspect can be appreciated looking the waveform during t_{OFF}; the slope of the waveform is

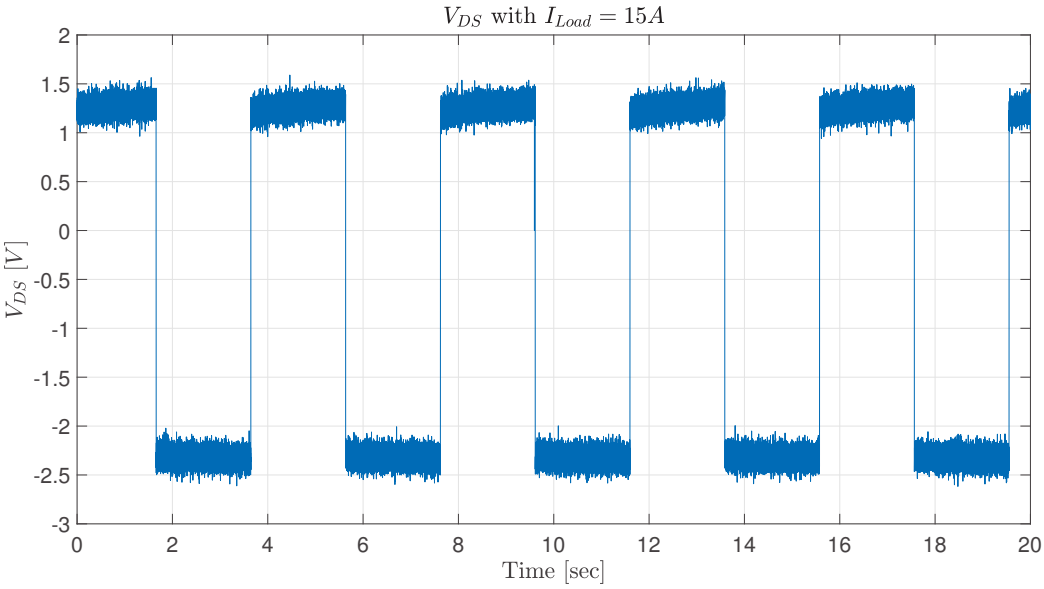


Figure 4.24: Drain to source voltage of the component in position M4, with a current load equal to 15 A. From this graph can be seen the slope of the wave form imputable to the junction temperature variation.

slightly negative. All these aspect can be appreciated on the figure 4.25. It is important to bear in mind that during the power cycling test the goal is to stress the component until the variation of some parameter, that indicate the failure. The parameter, that makes the degradation of the component faster, is the high temperature of the junction, thus T_J is the parameter to be checked. Before has been explained that since the junction is not available due the structure of the package of this type of MOSFET, the only possible way is to extract the temperature is using a temperature sensitive electrical parameter (TSEP), the selected one is the voltage of the body diode. Thus, once selected the component, extract the calibration curve of each of them, the junction temperature can be calculated during the power cycling test.

Therefore, the temperature of the junction during the test at 20 A is calculated. The calibration results of the sample used in the figure 4.25 is the following one:

$$V_{SD}\Big|_{t_{OFF}} = -0.001591 \times T_J + 2.391 \tag{4.12}$$

$$T_J = \frac{V_{SD} - 2.391}{-0.001591} \tag{4.13}$$

But the junction reaches two temperatures during the t_{OFF} time, a maximum and a minimum value. To be precise a zoom of the graph reported in 4.25 is shown in figure 4.26, in which the temperature extracted using 4.13 are indicated. The value of the voltage across the body diode is not clear, or better, during the measurement some interferences and noise were present, thus to overcome the possible problem in the final result, the values of the voltage, in a well defined

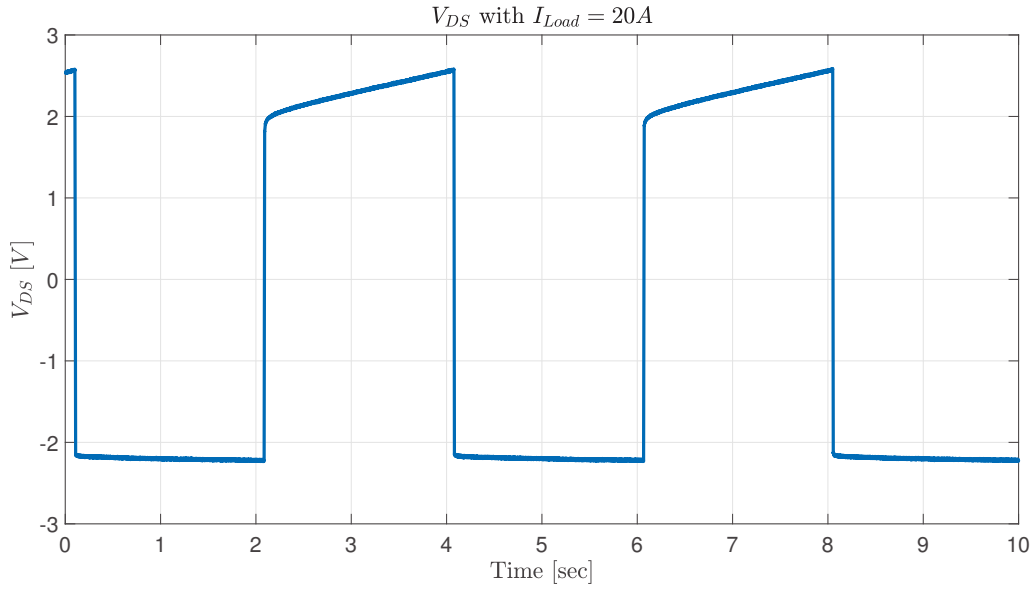


Figure 4.25: Drain to source voltage of the component in position M4, with a current load equal to 20 A, sampled with high resolution mode.

position, have been extracted doing the average between 50 sample points. The values of the voltage used to extract the junction temperature and relative results are reported in the table 4.2.

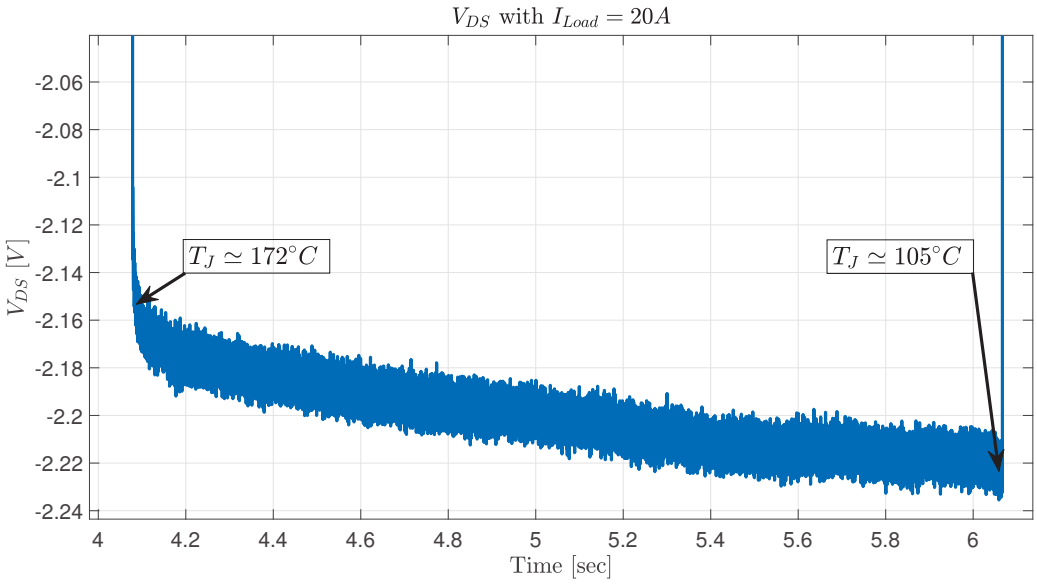


Figure 4.26: Drain to source voltage of the component in position M4, during the t_{OFF} time, with a current load equal to 20 A, sampled with high resolution mode.

As can be seen in the figure 4.26 and in the table 4.2, the values of the estimated junction temperature are pretty high, close to 200 °C, that can be assumed as maximum boundary. Thus the temperature level looks strange, since the recommanded

and maximum values for the gate voltage are 18 V and 22 V, respectively. Then the current is not even close to the high nominal value, that is 30 A. Furthermore, the maximum temperature indicated by project data is around 150 °C, thus this data assert that in this condition the test cannot be performed.

Point	Voltage measured	Temperature calculated
Hot point	2.1171 V	172 °C
Cold point	2.2234 V	105 °C

Table 4.2: Measured and calculated values of the point indicated in figure 4.26.

The difference between the high and the low temperature has been set equal to 80 K (ISLE project). But in this condition both the temperatures are too high. Analysing these results, a possible problem could be the thermal impedance between the samples and the cooling plate, then the thermal resistance has been calculated to avoid any possible issues about that. A qualitative image that shows the conformation of the system is report in figure 4.27.

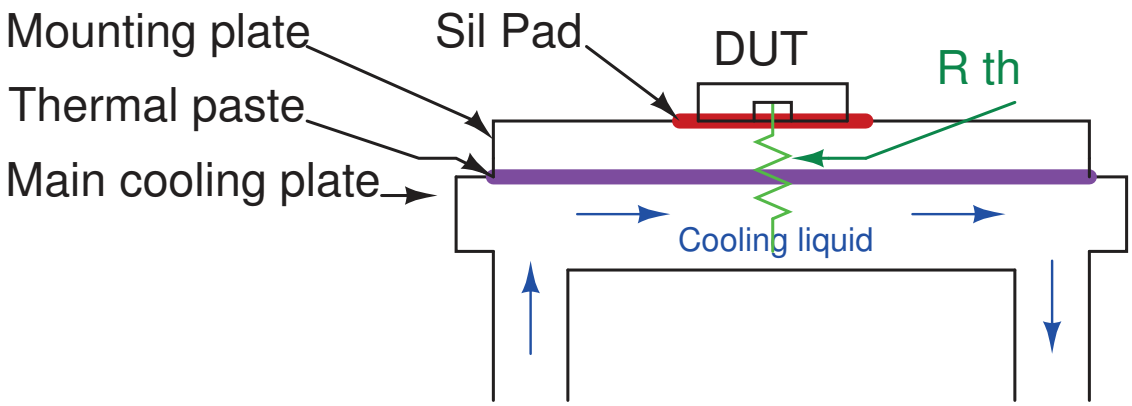


Figure 4.27: Schematic in which is indicated the theoretical total thermal resistance and all the parts that creates the system.

To estimate the thermal resistance a constant current has been run through just one leg of the circuit, the components present on that leg has been kept close, so that the temperature could rise up. The component used to perform this test was that one reported in figure 4.10 that has been dug and the temperature of the junction measured by using a thermal optical fiber. The current has been left for a amount of time needed to have the temperature of the junction constant. Once arrive at the steady state, the temperature of the junction and the temperature of the cooling plate have been recorded. The last information needed to extract the R_{TH} is the drain to source voltage, V_{DS} and it has been measured with an high resolution oscilloscope. Once the entire system arrived at the steady state, the

data has been recorded and the current load turned-off. The formula on the base of this calculation is the equation number 4.14.

$$P_{LOSS} \times R_{TH} = \Delta T = T_J - T_{AMB} \tag{4.14}$$

To be sure about the results, the calculation has been done with two different current level, with 10 A and 15 A. The results are more or less the same and them are reported in the table 4.3. The cooling plate temperature was constant equal to 20 °C and it has been checked using another available thermal optical fiber present in the system equipment.

I_D	V_{DS}	Junction temperature	R_{TH}
10 A	0.6627 V	45.2 °C	3.8 $\frac{°C}{W}$
15 A	1.2216 V	86 °C	3.6 $\frac{°C}{W}$

Table 4.3: Values measured and calculated to calculate the thermal resistance of the entire system.

The value of the thermal resistance, in both the cases, can be considered reasonable good and satisfying for the experiment requirement. Comparing these values with those one found in other similar system they are on the same magnitude, therefore the thermal aspect of the system can be considered irrelevant for the issue had with too high temperature of the junction at not limit current level (the current was at 66 % of the maximum level and the gate voltage was even higher than the recommanded value). To figure out which is the behaviour of the system at higher current load the system has been pushed up in current and more experiments have been performed since the protection present on the main board and in the external current load supply activated.
The behaviour of the system with a load current equal to 22 A is reported in figure 4.28 and as can be seen at some point the voltage V_{DS} of the sample suddenly skyrockets, starting from almost 2.5 V up to 5 V; then the protection of the external load current supply activates because in one leg there are three components, two DUT and one external switch; looking the trans-characteristic of each component the maximum voltage drop of the entire leg should be equal around 6 V, but taking in account the figure 4.28, the total voltage drop was pretty larger that 6 V and the maximum allowed voltage drop in the external load supply has been set equal to 12 V, then once the total voltage went behind the limits the current generator shut-down. The same story was for the protection from the main board, because the system adopted to sample the voltage uses an ADC for each channel and it has a maximum allowed voltage that can read, when it goes behind the limits a protection intervenes, turning-off the gate driver. At this point the entire system is frozen and an human action is needed to turn-on everything again. The external switch has a smaller voltage drop, compared with the DUT, since

it has a lager current capability and then a smaller on-resistance, thus they are not relevant and not taken into account in this aspect. Therefore, the figure 4.28 describes perfectly the protection of the system and its working procedure. But even more important is that the DUT should not arrive at that level of V_{DS} voltage, imposing a current equal to 22 A and a gate-source voltage 19 V. One possible explanation is the rising of the junction temperature and a correlated effect is the increasing of the on-resistance, that could explain the enormous voltage drop seen on the figure 4.28.

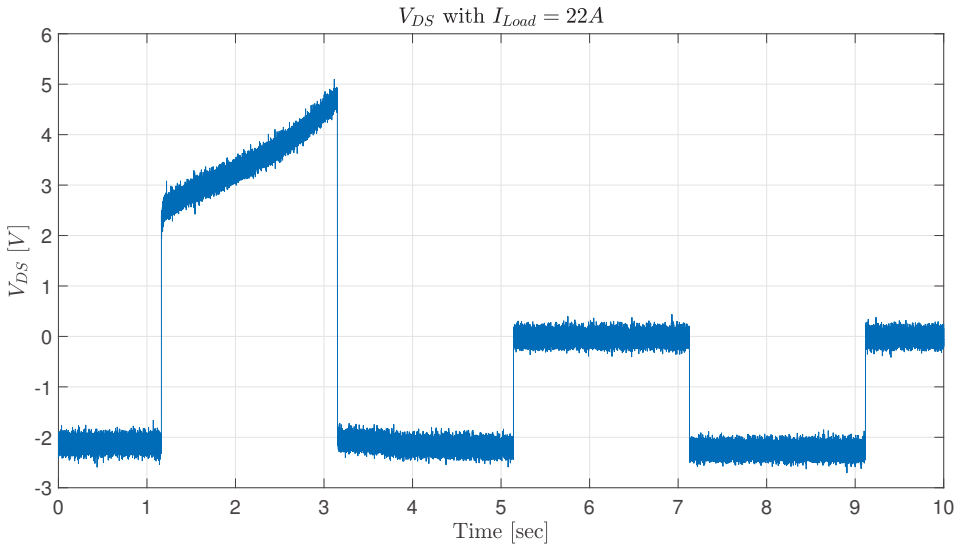


Figure 4.28: Drain to source voltage of the component in position M4, with a current load equal to 22 A.

Point	Voltage measured	Temperature calculated
Hot point	2.2134 V	282 °C
Cold point	1.9408 V	112 °C

Table 4.4: Measured and calculated values of the point indicated in figure 4.29.

Thus the junction temperature has been extracted using the same procedure as before; also the equation has been kept the same because the component analysed is the same. The formula adopted is reported above an it is the equation 4.13 and the data are repoted in the table 4.4. Furthermore, the zoom during the t_{OFF} time right after the saturation of the system is reported in figure 4.29 and the temperatures of junction are indicated.

The working junction temperature is to high to work in this condition and the ΔT is quite larger than the 80 K defined at the beginning; then to work properly

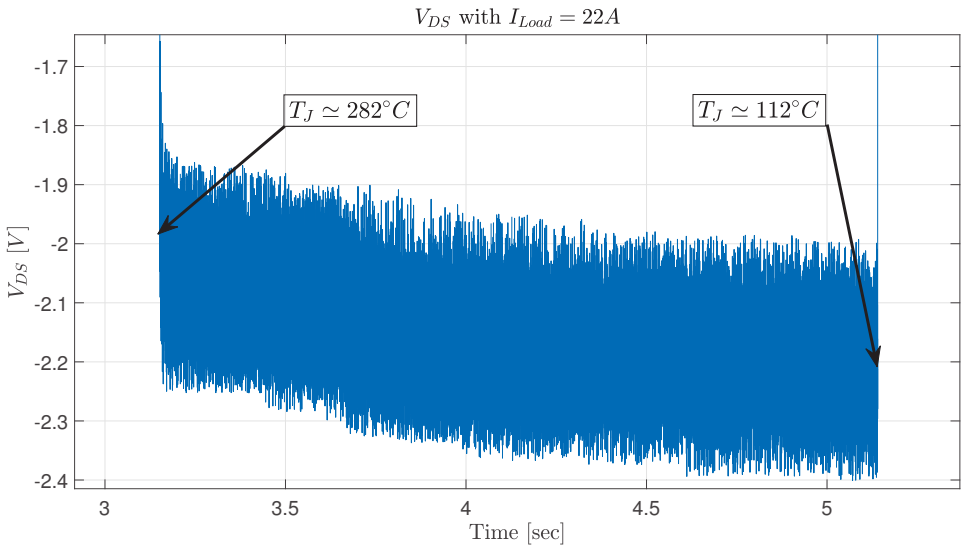


Figure 4.29: Drain to source voltage of the component in position M4, during the t_{OFF} time, with a current load equal to 22 A.

and meet process specifications with this gate voltage the load current can not pushed to high.

4.4 Possible implementation

Further possible implementations for the project can be:

Change the gate control Controlling the gate with a defined voltage can affect the threshold voltage and induce a drift in the on-state resistance of the chip, which affect the on-state voltage drop and junction temperature measurement of the DUT. Furthermore, the threshold voltage drift changes almost linearly with time, and the linear change rate is proportional to the applied bias voltage [4]. Then the [4] indicates that the threshold voltage drift is related to the polarity, magnitude and duration of the voltage applied on the gate. Then to minimize the threshold voltage drift the relation 4.15 can be adopted.

$$\Delta t_+ \times V_{G_+} = \Delta t_- \times V_{G_-} \tag{4.15}$$

The following approach, with relative results, is reported in the research paper [4].

Better thermal coupling Finding a better silpad to couple the thermal pad of the MOSFET with the cooling plate could be useful to improve the thermal ability to easily handle the junction temperature, then it means reduce the thermal resistance of the system.

Chapter 5

Conclusions

The present project (ISLE) is a part of a larger project funded by ECPE, in which Aalborg University (AAU) aims to implement power cycling. The objective of this project is to try to find the lifetime of a SiC MOSFET component that has been stressed with a short circuit having energy below the critical energy E_C. It is expected that this component has no change in its parameters, but that its lifetime lies between the lifetime of a component to which no stress test has been carried out and a component which has been stressed to the point of changing parameters (i.e. damaged). The expected duration of the study is around one year, so this report shows up to the initial step of that. Furthermore, the lack of availability of the equipments brings one more difficulty in the project, to overcome the problem a AC power cycling machine has been adapted to work in DC mode. To do that, a new adapter has been developed, which allows to measure the V_{DS} during the t_{OFF} and the V_{TH} thanks to a current sources embedded in the board; furthermore, it allows to mount two different types of TO247 packaging (*TO*247 *3 pins* and *TO*247 *4 pins*). To be sure that the result were consistent, from a 140 test samples, just 40 samples have been selected for the project and they are chose taking into account common parameters that could ensure the same behaviour during the tests, the parameters have been chose by the supervisor of the project. The preliminary power cycling test shows that the defined component can not work at nominal current, but this is not necessary an issue for the project, because the power cycling needs to have a ΔT with a well defined maximum temperature. Then to reach the good condition for the test the gate voltage and the current load, that allow to work in well defined condition, have to be found. Therefore, up to now the new configuration of the system works properly and the first long power cycling tests, until the variation of the parameter that indicate the failure, have to be done. The ISLE project needs one year to be completed, then the following thesis document aims to address just a part of its. The final consideration is that the adaptor developed to adapt the system to work in DC mode, instead AC mode, works properly and it can be use per the project, furthermore, to be able to use the following system with all the existing components the DC/DC converter that supply the gate driver have to be changed to provide a wider voltage range for the control of the DUTs.

Appendix A

Appendix

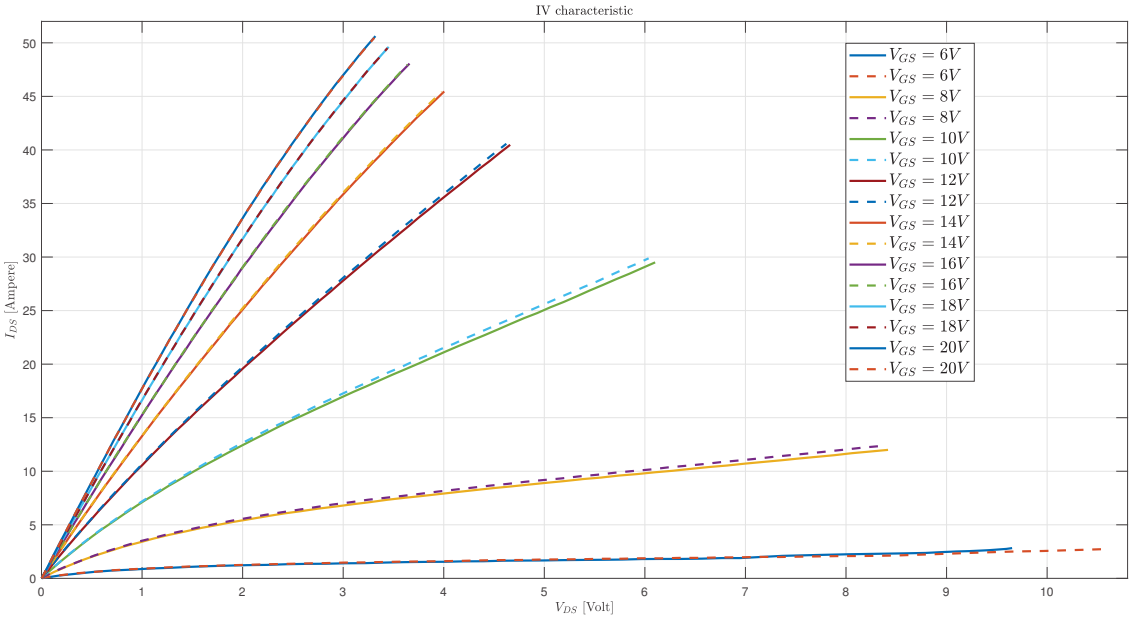


Figure A.1: I_D over V_{DS} characteristic of DUT. Continous line is for sample one and dotted line for sample two.

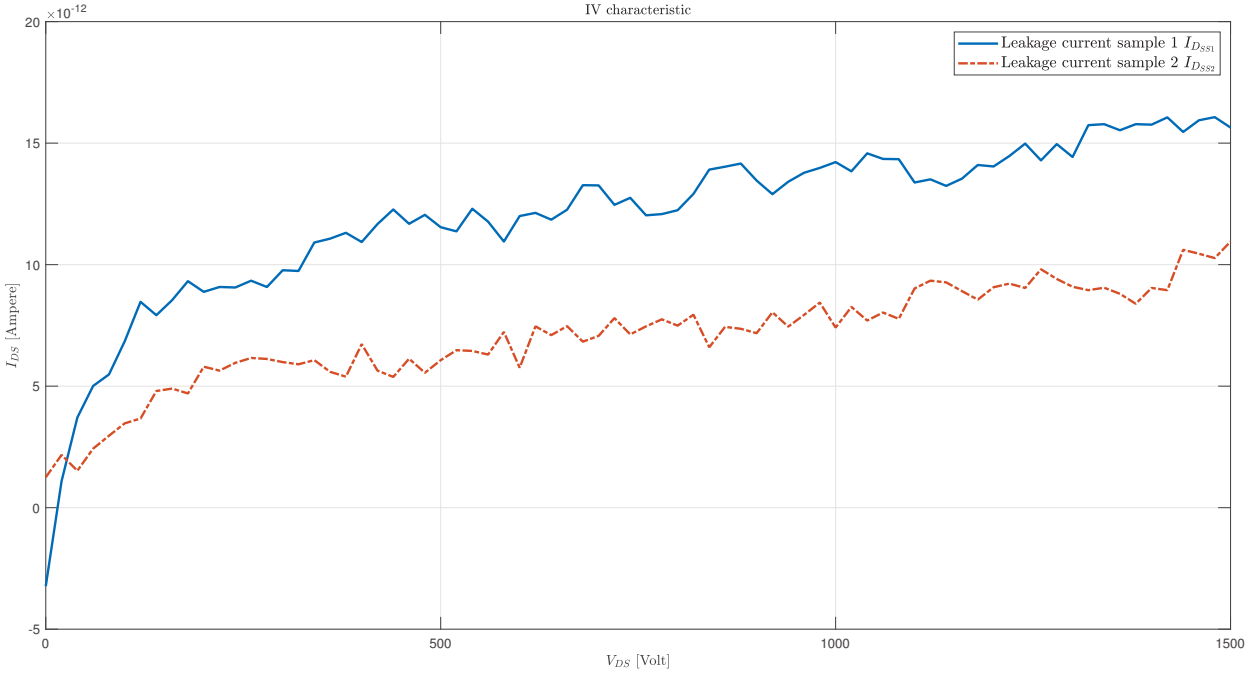


Figure A.2: Leakage current curves on the drain.

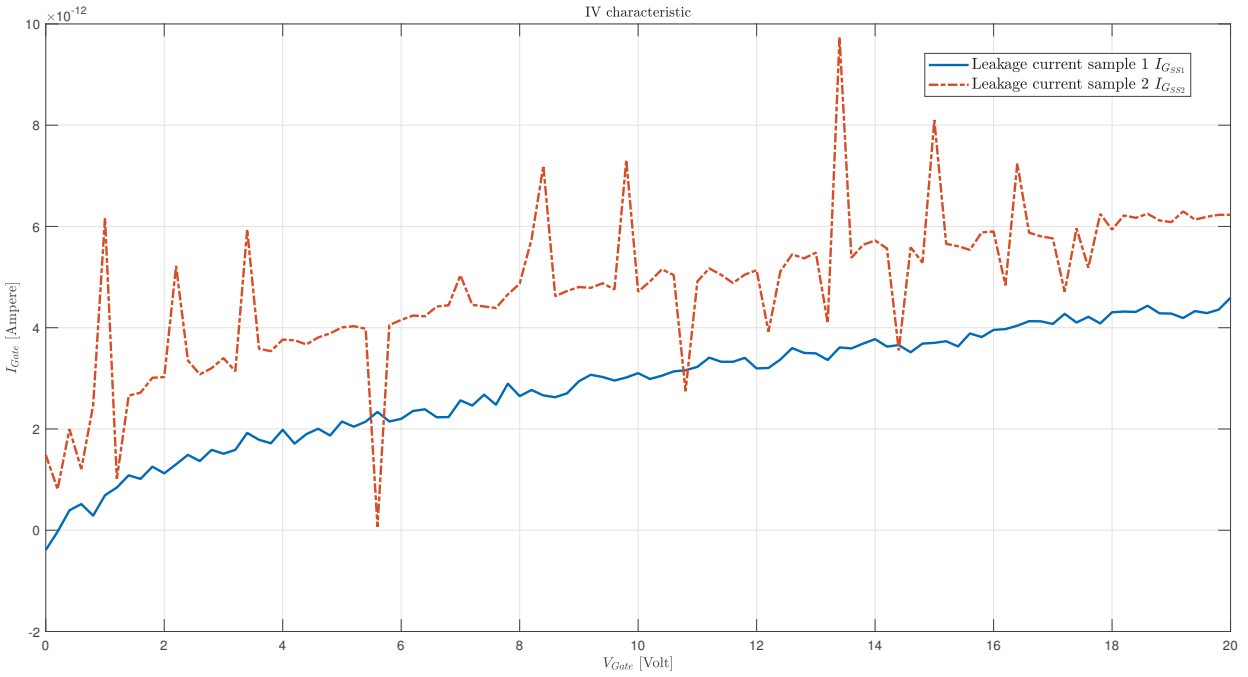


Figure A.3: Leakage current curves on the gate.

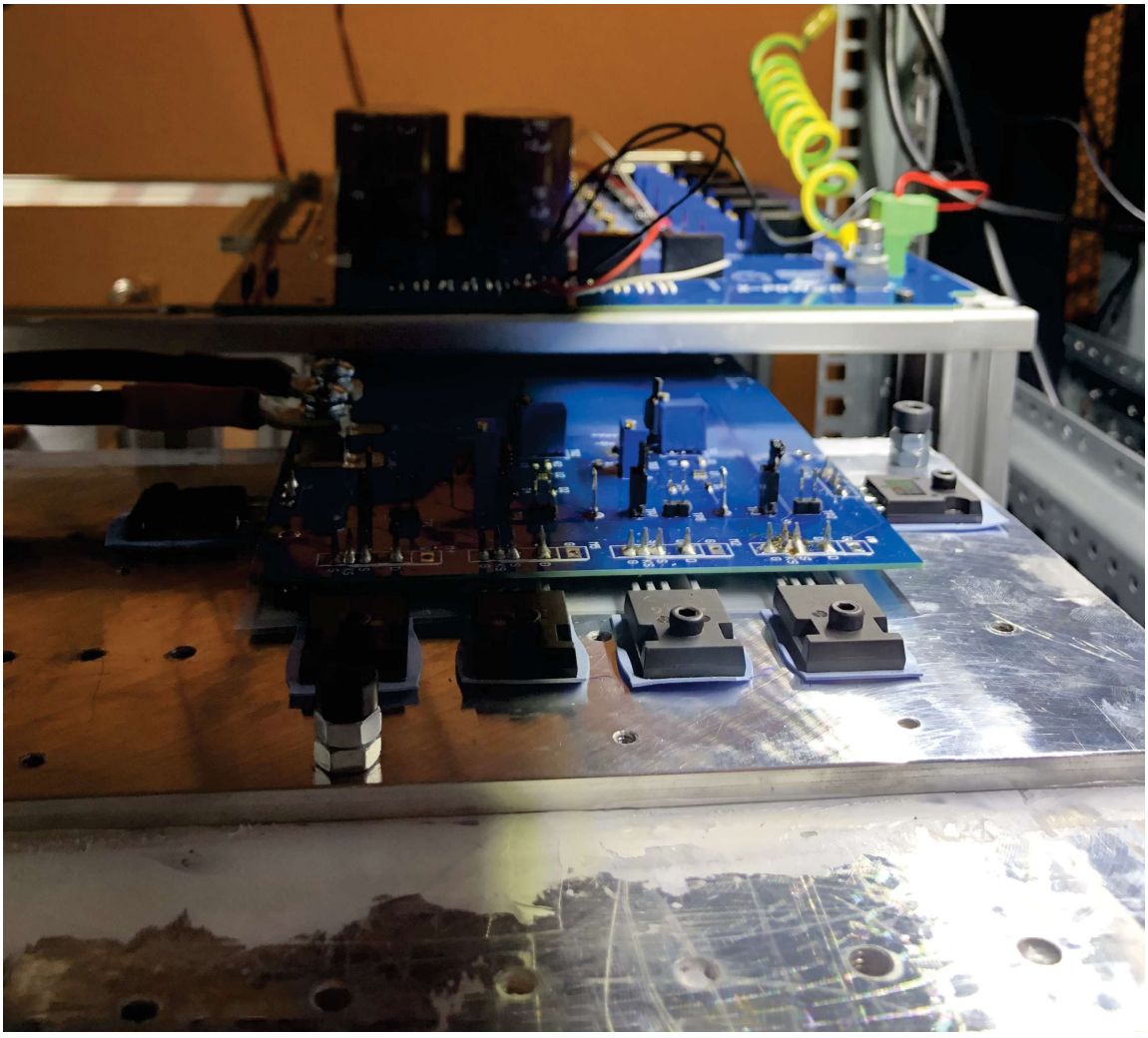


Figure A.4: Picture of the real setup.

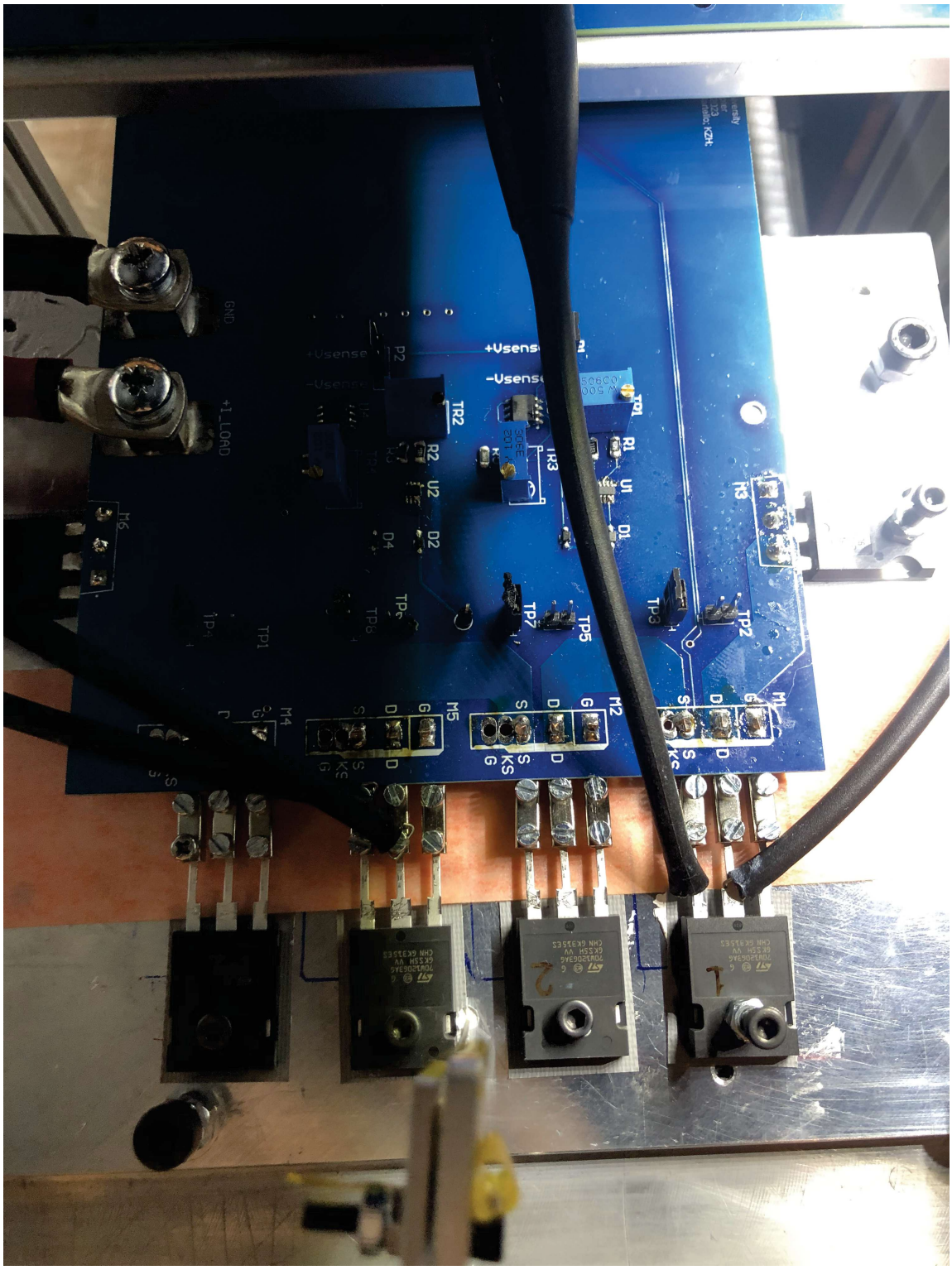


Figure A.5: Picture of the real setup in which can be seen the 3 pins components and the clamps positioned on the footprint.

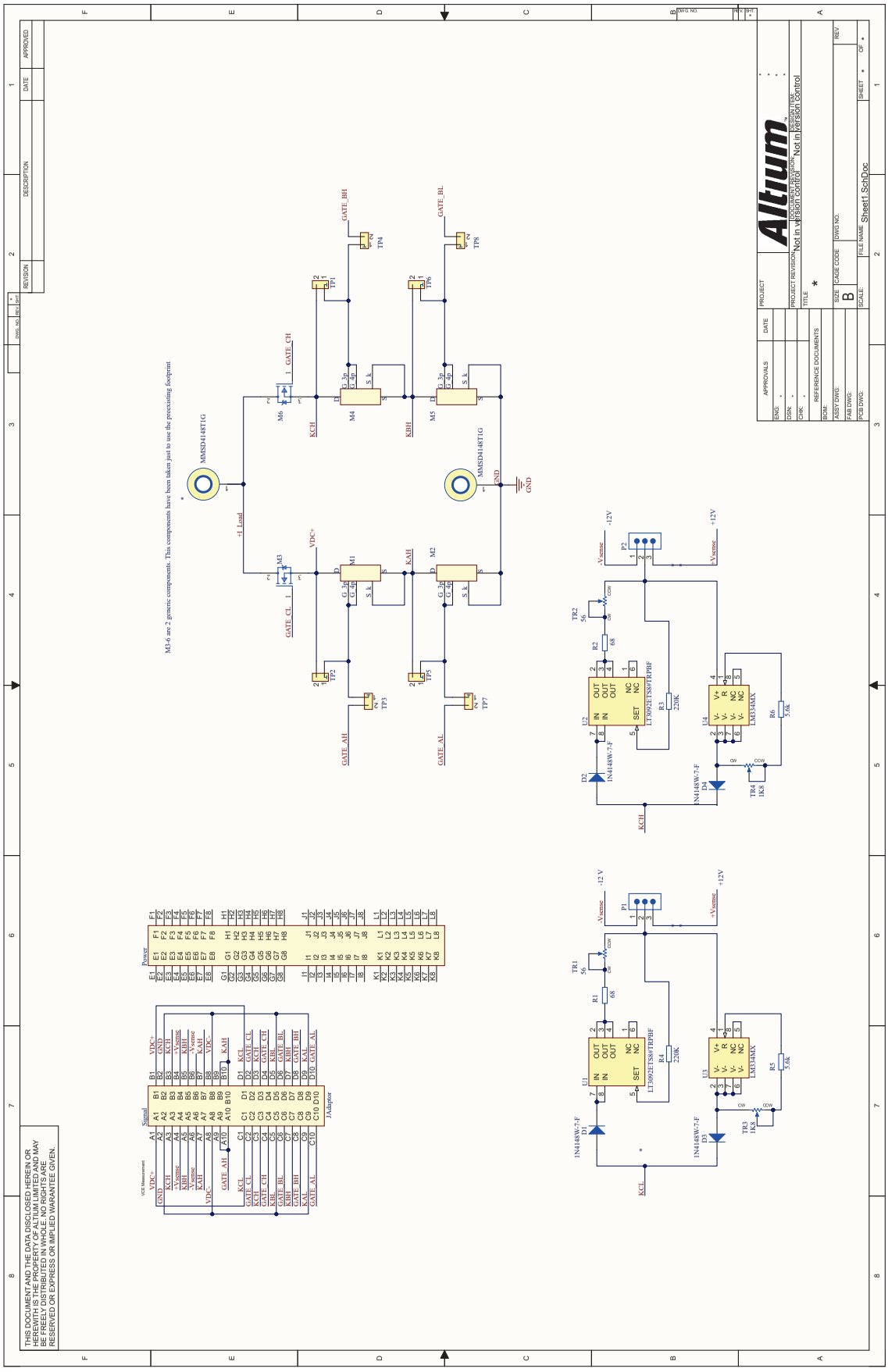


Figure A.6: Total schematic circuit of the PCB adaptor board.

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