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Investigation of Total Ionizing Dose Effects on Semiconductor Power Devices under Static and Dynamic Conditions

Studio degli Effetti della Dose Totale delle Radiazioni Ionizzanti sui Dispositivi di Potenza a Semiconduttore in Condizioni Statiche e Dinamiche

Laureando:

Eugenio Valente

1082511

Relatore:

Simone Gerardin

Alla mia famiglia e ai miei amici
per il supporto, e non solo, in tutti questi anni.

Abstract

The present thesis is aimed to show the results achieved during a five months internship period at the European Space Agency-European Space Research and Technology Centre (ESA-ESTEC) in the Component Space Evaluation & Radiation Effects Section and a period at the Department of Information Engineering at the University of Padova. The purpose of this work is to investigate Total Ionizing Dose (TID) Effects on semiconductor power devices under static and dynamic bias with particular attention to power MOSFETs.

The space environment has a strong influence as far as satellite performances are concerned. In fact several sources of radiation can degrade the electronic devices inside the spacecraft. Power MOSFETs are one of the most important electronic devices. The main degradation effect in power MOSFETs is TID. So the success of a space mission relies on the correct functionality of these electronic devices.

Thus, TID testing is essential to characterize the performance of power MOSFETs in this environment. TID tests are usually performed with static bias for a worst-case evaluation. However, in the real world, these devices do not work in this condition all the time, maybe they never work in the worst-case. Hence, to simulate a real usage it is better to use a dynamic bias during TID tests.

What is the degradation under dynamic conditions? How does it compare with static ones?

The main goal of this thesis is to answer these two questions.

The thesis activities were divided in three parts:

- a TID test campaign followed by annealing and ageing on power devices;
- design of a boost converter;
- analysis and physical modeling of test results under static and dynamic bias.

In this thesis there is also a study of the Enhanced Low Dose Rate Sensitivity (ELDRS) effect on bipolar transistors.

All the tested devices are prototypes from STMicroelectronics.

This work is organized in five chapters:

Chapter1 covers the basic concepts of TID in semiconductor devices.
Chapter2 shows the test results performed at ESTEC on power MOSFETs in static bias condition.
Chapter3 shows the test results of power MOSFETs with dynamic bias condition and the comparison with the static bias condition.
Chapter4 shows the test results performed at ESTEC on bipolar transistors in static bias condition.
Chapter5 summarize of the results of this thesis.

Sommario

La presente tesi ha lo scopo di mostrare i risultati raggiunti durante cinque mesi di tirocinio all'European Space Agency-European Space Research and Technology Centre (ESA-ESTEC) nella Component Space Evaluation & Radiation Effects Section e un periodo al Dipartimento di Ingegneria dell'Informazione all'Università di Padova. Lo scopo di questo lavoro è di analizzare gli effetti da dose totale delle radiazioni ionizzanti (TID) sui dispositivi di potenza a semiconduttore in polarizzazione statica e dinamica, con particolare attenzione riservata ai MOSFET di potenza.

L'ambiente spaziale ha una forte influenza per quanto riguarda le performance di un satellite. Infatti diverse sorgenti di radiazioni possono degradare i dispositivi elettronici che si trovano all'interno di un apparato spaziale. Uno dei più importanti dispositivi di potenza è il MOSFET di potenza. Il principale effetto che induce degradazione nei MOSFET di potenza è il TID. Quindi il successo di una missione spaziale si basa sulla corretta funzionalità di questi dispositivi elettronici.

Perciò, il test TID è essenziale per caratterizzare la performance dei MOSFET di potenza in questo ambiente. Questi test sono spesso eseguiti con polarizzazione statica per la valutazione del caso peggiore. Tuttavia, nel mondo reale, questi dispositivi non lavorano in questa condizione tutto il tempo e forse non si trovano mai nella situazione di lavorare nella condizione peggiore. Perciò, per simulare un utilizzo reale è meglio usare la polarizzazione dinamica durante i test TID.

Cos'è la degradazione in condizione dinamica? Come può essere con-

frontata con la condizione statica?

Il principale obiettivo di questa tesi è di rispondere a queste due domande.

L'attività di tesi è stata divisa in tre parti:

- campagna di test TID seguita da annealing e ageing sui dispostivi di potenza;
- progetto di un convertitore boost;
- analisi modellizzazione fisica dei risultati dei test in polarizzazione statica e dinamica.

In questa tesi è presente lo studio dell'effetto *Enhanced Low Dose Rate Sensitivity* (ELDRS) sui transistor bipolari.
Tutti i dispositivi testati sono prototipi di STMicroelctronics.
Questo lavoro è organizzato in cinque capitoli.
Capitolo1 riguarda i concetti base degli effetti TID nei semiconduttori.
Capitolo2 mostra i risultati dei test eseguiti in ESTEC sui MOSFET di potenza in condizione di polarizzazione statica.
Capitolo3 mostra i risultati dei test dei MOSFET di potenza in condizione di polarizzazione dinamica ed il confronto con la condizione di polarizzazione statica.
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Chapter 1

Basic Concepts of TID in Semiconductor Devices

The space is a very challenging environment. Electronic devices have to withstand a large amount of ionizing radiation.
There are three main sources of radiation:

- Radiation Belts: protons(keV-500MeV) and electrons(eV-10MeV)
- Solar Flares: protons(keV-500MeV) and ions(1-few 10MeV/n)
- Galactic Cosmic Ray(GCR): protons and ions(max 300MeV/n)

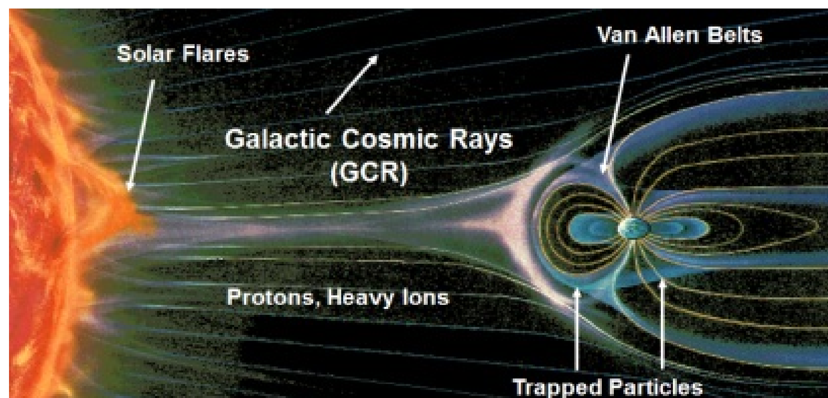

Figure 1.1: Principal radiation sources [Cortesy of NASA].

The main effects that the ionizing radiation causes in power devices are:

- Total Ionizing Dose(TID)
- Single Event Effects (SEE)

This chapter will cover concepts about basic mechanisms of the interactions of ionizing radiation with MOS and bipolar devices.

1.1 Ionizing Dose Effects on Power MOSFETs

All the spacecrafts have at least one power MOSFET. Accordingly we can claim that power MOSFETs are one of the most important electronic devices in space.
There are several types of power MOSFETS:

- vertical double-diffused MOSFETs (VDMOS), figure 1.2(A);
- vertical trench-gate style MOSFETs, figure 1.2(B);
- superjunction MOSFETs, figure 1.2(C);
- lateral double-diffused MOSFETs (LDMOS), figure 1.2(D)

Ionizing radiation often causes damaging effects on the characteristic of MOS devices and circuits. The main parameters that are affected include the threshold voltage, leakage drain current and leakage gate current. Changes in these parameters depend on a number of factors: the total dose of radiation received and its energy, the bias applied during the irradiation, the geometry, type and the method of fabrication of the transistor; the dose rate at which the radiation is delivered; the temperature during the irradiation and the bias, time and temperature after the irradiation is completed. Usually the transistor is the primary element in an integrated circuit and all these changes in its properties lead to an alteration of the behavior of the whole circuit,

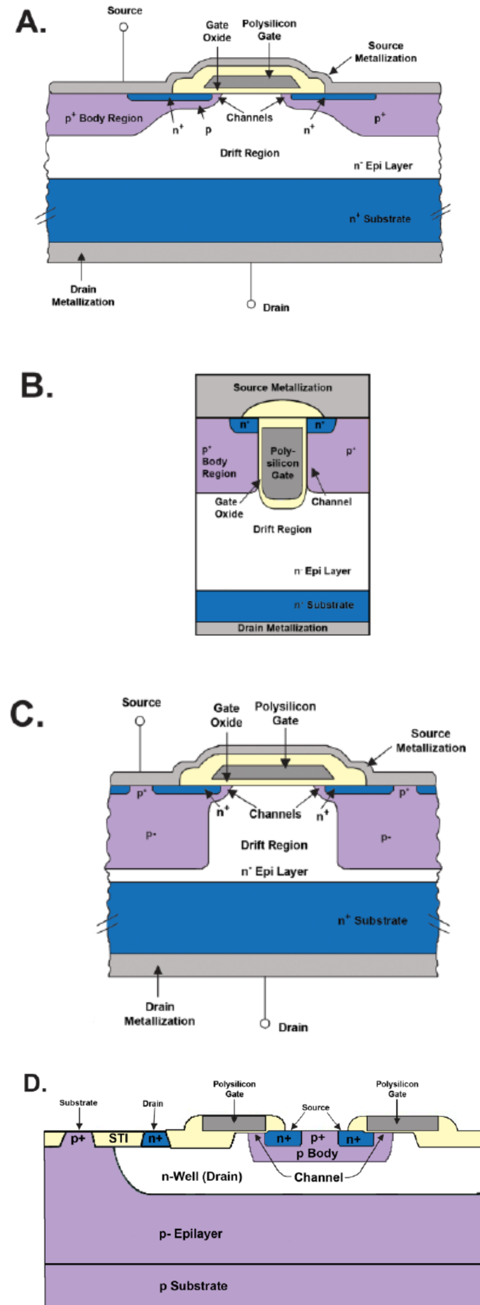

Figure 1.2: Illustrations of n-type power MOSFETs: A) VDMOS, B) trench-gate, C) superjunction and D) LDMOS. [1]

for example in its functionality, leakage currents, timing, input and output switching levels, output drives and operating voltage and frequency [2].

In Figure 1.3 it is possible to see a schematic energy band diagram of a MOS structure, where a positive bias is applied to the gate causing radiation-induced electrons to flow toward the gate and holes to move to the Si substrate. Furthermore, in this figure the four major physical processes are shown which contribute to the degradation of the parameter of a MOS device. The gate oxide insulator is the most sensitive part of a MOS system [3].

The first process takes place when a gate oxide is struck by a ionizing particle and electron/hole pairs are created by the deposited energy. In SiO_2 the electrons are much more mobile than the holes, and they are swept out of the oxide, typically in a picoseconds or less. However, in those first picoseconds, a large number of the electrons and holes will recombine depending on the electric field. The fraction of electron/hole pairs, which escape the initial recombination, is called **charge yield**. Surviving holes hop slowly through shallow defects and release hydrogen and get trapped close the interface. Electron/hole pair generation and recombination is the first process in Figure 1.3. The maximum initial threshold voltage shift due to this process is shown in Figure 1.4 [3].

The second process in Figure 1.3 is rappresented by the holes that move to the Si/SiO_2 interface, which causes the recovery of the threshold voltage as shown in Figure 1.4. This process takes many decades in time in the space, and it is very dependent on the applied field, temperature, oxide thickness, and oxide processing history. This process can take less than a second at high temperature, but it can be slower at low temperature[3].

The third process in Figure 1.3 and in Figure 1.4 occurs when the Si interface is reached by the holes. A fraction of the transporting holes that escape the initial recombination can fall into relatively deep trap states. So negative voltage shift is caused by these trapped holes, which can persist for hours or even for years. In any case, also these trapped holes, after a lot of

time, are released thanks the effect of the annealing as shown in Figure 1.4 [3].

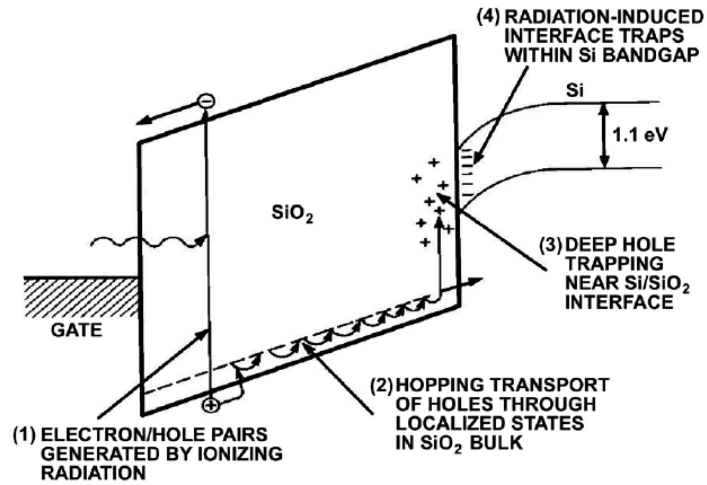

Figure 1.3: Schematic energy band diagram for MOS structure [3].

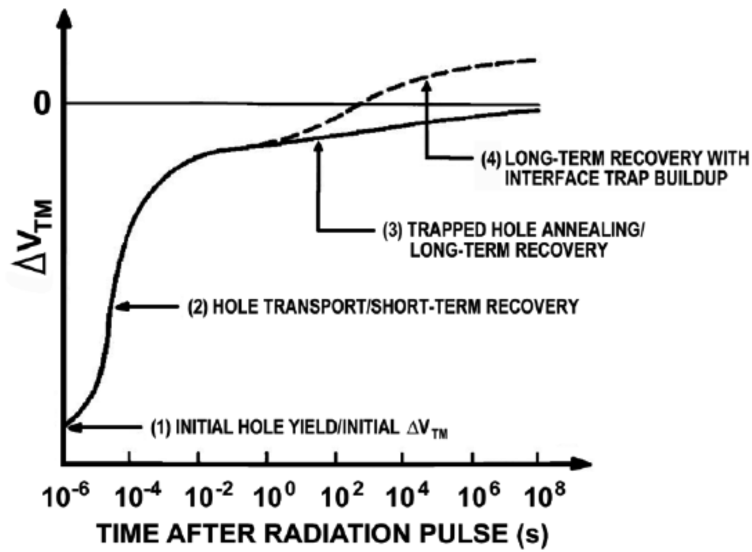

Figure 1.4: Schematic time-dependent post-irradiation threshold voltage recovery of N-channel MOSFET [3].

The fourth process of MOS radiation response is represented by the radiation-induced buildup of interface traps right at the Si/SiO_2 interface. The charge state of these interface states is determined by the Fermi level, and as shown in figure 1.4 this process causes another voltage threshold shift [3].

Figure 1.4 is taken from [3] and there does not show real data, but it reasonably represents the main characteristics of the radiation response of a hardened N-channel MOS transistor.

1.1.1 Charge Yield

Taking in consideration the first process in figure 1.3, the fraction of holes that escape at the initial recombination is called **charge yield**. In fact due to the presence of an electric field in the oxide, once generated, electrons and holes are transported in opposite directions and a fraction of electrons, due to their high mobility, swept out of the silicon dioxide in very shortly time (picoseconds). Anyway the other fraction of electrons recombine with the holes in the oxide. Thus, the initial recombination is strongly dependent on the electric field and the type of incident particle too [2] [4]. In fact if the particle has a large ionizing power, a dense group of charge gets formed and in this case there is a high probability of recombination. On the contrary, if the particle has low ionizing power, it generates isolated charge pairs and the probability of recombination is very low. Figure 1.5 illustrates the dependence of initial recombination on the electric field strength in the oxide for different particles: protons, alpha, gamma and x rays. On the other hands this figure shows the fraction of unrecombined holes (charge yield) versus electric field in the oxide[4].

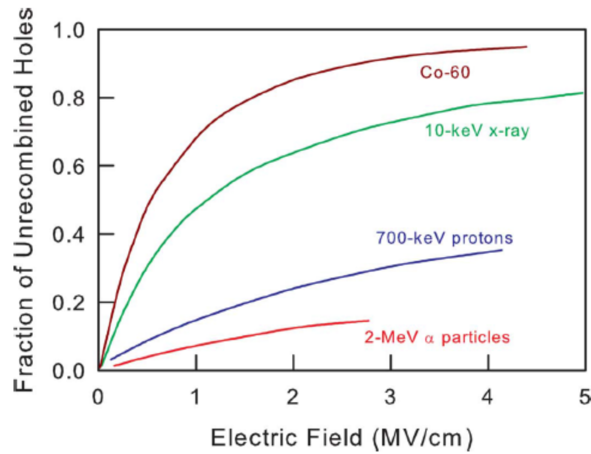

Figure 1.5: Charge yield as a function of electric field for different particles[4].

1.1.2 Oxide Traps

As described in the previous sections, holes in the oxide are slower than electrons and their direction depends on the bias applied, in fact if the bias is negative holes move towards the $gate/SiO_2$ interface, instead if the bias is positive, holes move towards the Si/SiO_2 interface. The transport of holes in the oxide occurs by hopping through localized states and, due to their positive charge, holes causes a distortion in the electric field. This distortion slows down holes transport and makes it dispersive because this local distortion increases the trap depth at the localized site where holes tend to trap themselves. The combination of the charged carrier (hole) and its strain field is known as a **polaron** [4].

As said before, with the application of a positive gate bias, holes are transported to the Si/SiO_2 interface and close to the interface they meet a large number of oxygen vacancies which can act as trapping centers. The out-diffusion of oxygen in the oxide during manufacture and lattice mismatch at the surface causes these oxygen vacancies. Thus when the holes arrive close to the interface, some fraction of them will become trapped. The capture cross-section depends on both the applied field and the device fabrication; in

fact in hardened oxides there is only a few percent of the holes being trapped and in a soft oxide the percentage can arrive till 100%. The positive charge associated with trapped holes causes a negative threshold-voltage shift in both N-channel and P-channel MOS transistors[4].

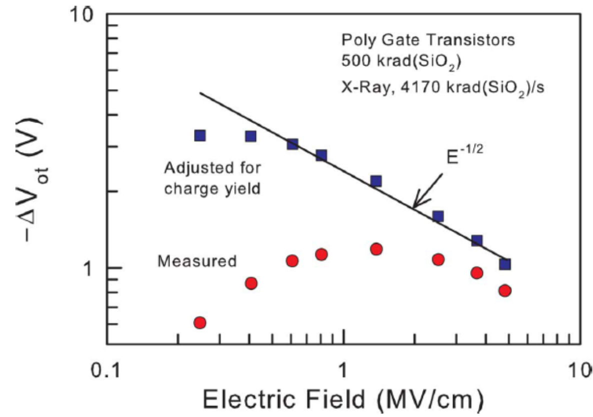

Figure 1.6: Electric field dependence of ΔV_{ot} versus electric field[4].

Figure 1.6 is a plot of the threshold-voltage shift due to oxide-trap charge, ΔV_{ot}, versus oxide electric field. The curve with red circles represents the measured data, the curve with squares, instead, is the measured data adjusted for charge yield. As shown, for electric fields greater than 0.5 V/cm, ΔV_{ot} adjusted for charge yield follows approximately an $E^{-1/2}$ electric field dependence [4]. The curve with red circles consider both the effects of charge yield and trap cross-section, and it is possible to conclude that the worst bias condition is at an intermediate value. In fact, these two effects balance themselves: charge yield increases with electric field and trap cross-section decreases with electric field. Trapped charge decreases over time, so there is a time-dependent effect and the neutralization of holes trapped is accelerated at high temperature.

1.1.3 Interface Traps

As holes are trapped close to the Si/SiO_2 interface or during hopping polaron process, hydrogen ions are likely released and when these hydrogen ions arrive at the interface, they can generate interface traps. Interface traps are amphoteric, that means they are of donor or acceptor type depending on their position with respect to the intrinsic Fermi level. So the interface traps are negatively charged in an inverted N-MOSFET and positively charged in an inverted P-MOSFET. Anyway the effects of the interface states are not immediately visible because their generation occurs over time due to the slow transport of holes and hydrogen in the oxide and the saturation can arrive after thousand of seconds, as it is possible to see in Figure 1.7.

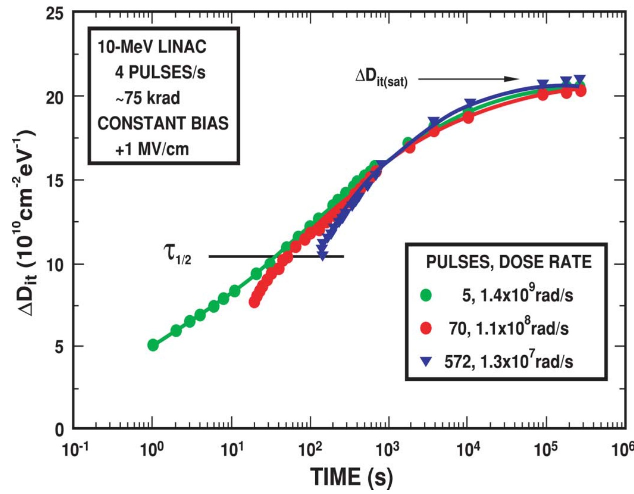

Figure 1.7: Amount of interface traps as a function of time after irradiation[4].

To conclude in N-MOSFETs there is a compensation effect between the positively trapped charge and the negatively interface traps and after annealing this can lead to rebound effects. Instead in P-MOSFETs there is no compensation effect but there is an additive effect that can explain why a P-MOSFET degrades more than a N-MOSFET. The neutralization of interface state occurs only a temperature higher than 400°C.

1.2 Ionizing Dose Effects on Bipolar Transistor

As power MOSFETs also bipolar transistors are affected by TID. The most radiation-sensitive parameter is the current gain.
There are several types of bipolar transistors: vertical, lateral, substrate, etc. For a NPN device, the base current at a given base-emitter voltage increases with irradiation; on the contrary the collector current does not change. So the device gain decreases (See fig. 1.8)

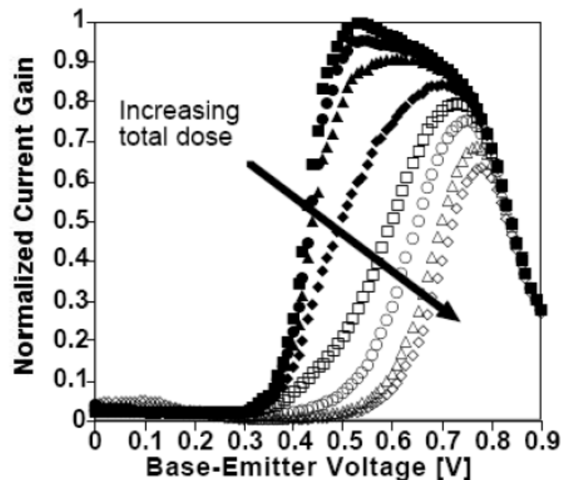

Figure 1.8: Gain degradation in BJT vs total Dose [11].

The base current is the sum of three contributions: Holes injected from the base into the emitter, Recombination in the emitter-base depletion region, Recombination with electrons traversing the neutral active base. Usually the second contribution is affected by TID. Indeed, in the depletion region two effects are generated: increased surface recombination velocity and an increase of the emitter-base depletion region width at the surface.
The cause of this increase of recombination, as shown in figure 1.8, is related to the interface traps that are generated at the surface of the depletion region of the forward-biased base-emitter junction. The other effect is that the presence of charge in the oxide increases the area over which recombination

can be effective [8].

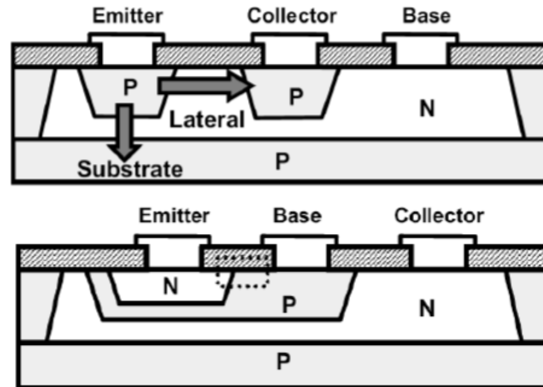

Figure 1.9: pnp and pnp bipolar transistors. the dashed line represent the most sensitive area [11].

1.2.1 Enhanced Low Dose Rate Sensitivity (ELDRS)

The dose rate in BJTs has an important role in the degradation. In fact, in many BJTs is possible to see that the degradation at low dose rate is higher than at high dose rate. The name of this particular phenomenon is *Enhanced Low Dose Rate Sensitivity*(**ELDRS**) and it may be interpreted as a reduced sensitivity at high dose rate rather than the opposite. Hence, in BJTs there is a different behavior compare to MOSFETs, in fact in MOSFETs the radiation effects are time-dependent, but not dose rate dependent.
There are a lot of models that can explain ELDRS. The most intuitive one is the space charge model that attributes the lower degradation at high dose rate to the large amount of positive charge generated at high-dose rate which acts as a barrier for the transport of holes and hydrogen to the interface thus reducing the degradation rate [9] [8]. Another model for this phenomenom is based on the competition between trapping and recombination of radiation-induced carriers due to electron traps [10]

Chapter 2

Static Bias Test on Power MOSFETs

This chapter shows the results of the tests in static conditions performed at ESA-ESTEC on power MOSFETs.

2.1 Low dose rate Co60 TID Tests of 100 krad, 250V, 10A Power MOSFET N-channel prototype

2.1.1 Introduction

A total dose characterization test of 250V Power MOSFET N-channel prototype was performed at the ESTEC Co-60 Facility. The transistors have been exposed to a total accumulated dose of 100 krad(Si), using a constant low dose rate of 360 rad(Si)/h (6 rad(Si)/min). The purpose of this test is to evaluate the TID tolerance of the MOSFET. The tests have been performed in accordance with the ESCC Basic Specification No. 22900 [6].

2.1.2 Experimental Conditions

Facility and Dosimetry

The ESTEC Co-60 facility comprises of a Nordion Gamma beam 150°C irradiator containing a nominal 85.2 TBq (2300 Ci) Co-60 source at the last reload date in October 2011. The irradiation room is monitored for temperature, relative humidity and pressure. The dosimetry system is based on a Farmer type 2571A 0.6 cc air ionization chambers linked to a Farmer 2670 electrometer. The dosimetry system is compensated against temperature and pressure environmental fluctuations. All irradiations and measurements have been performed at room temperature (22.5 ± 3 °C).

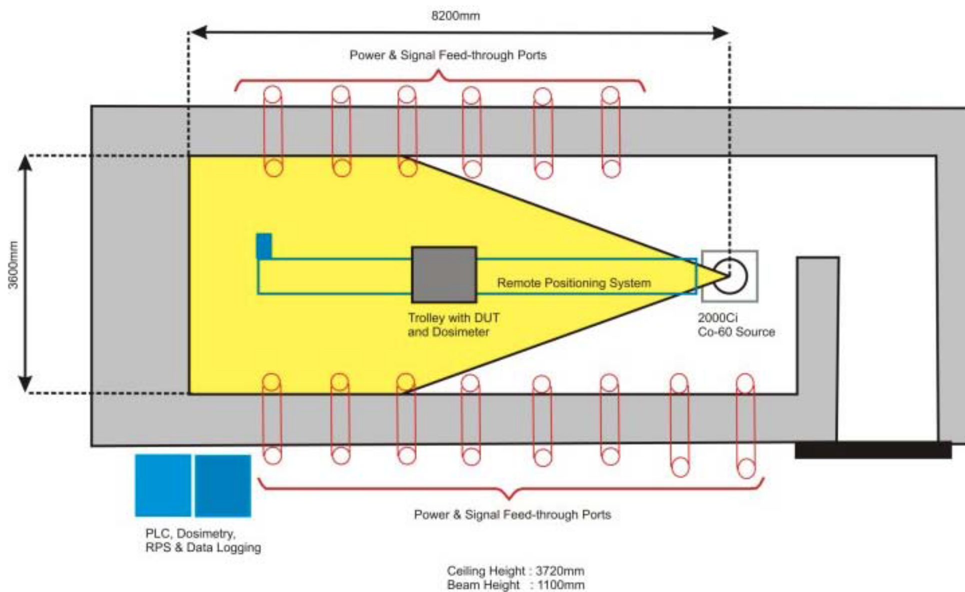

Figure 2.1: Co-60 ESA-ESTEC, radiation cell. [7]

Tested Devices

Part type	Prototype
Manufacturer	STMicroelectronics
Function	250V, 10A N-channel MOSFET
Family	Transistor
Group	-
Package	TO3

Table 2.1: Information Power MOSFET N-channel

Irradiation Test Conditions

For the needed dose rate of 360 rad/h, the dose rate to distance calculator provided by the web page of the facilities has been used [7], giving a required distance of 199 cm between the device and the source and a uniform irradiation area of 92×92 cm. The irradiation has been performed at room temperature.

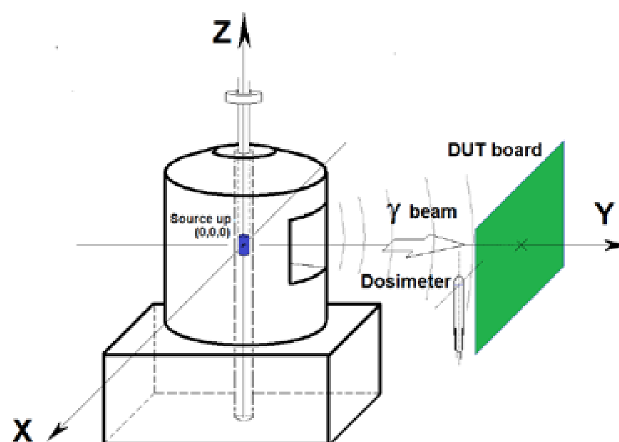

Figure 2.2: Co-60 irradiator head and board positioning sketch. [7]

The radiation test steps, for the two biased conditions, are reported in the following tables (table 2.2, table 2.3):

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(Si)	krad(Si)	rad(Si)/min	hours	°C
1	3.000	0	6		Room
2	5.927	3.000	6		Room
3	8.084	8.927	6		Room
4	8.900	17.011	6		Room
5	10.156	25.911	6		Room
6	24.758	36.067	6		Room
7	18.679	60.825	6		Room
8	15.972	79.504	6		Room
9	26.094	95.476	6		Room
10		121.570	6		Room
11		121.570	-	24	Room
12		121.570	-	168	100

Table 2.2: The Radiation test steps on Power MOSFETs with bias $V_{GS} = +15V$

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(Si)	krad(Si)	rad(Si)/min	hours	°C
1	2,535	0	6		Room
2	6.481	2.535	6		Room
3	8.074	9.016	6		Room
4	9.579	17.090	6		Room
5	6.861	26.669	6		Room
6	25.861	33.530	6		Room
7	15.593	59.391	6		Room
8	17.914	74.984	6		Room
9	23.986	92.898	6		Room
10		116.884	6		Room
11		116.884	-	24	Room
12		116.884	-	168	100

Table 2.3: The Radiation test steps on Power MOSFETs with bias $V_{GS} = +8V$

At the completion of each irradiation step, intermediate electrical measurements have been carried out according to the electrical measurement parameters (Table. 2.4). Following the ESCC 22900 recommendations, the time interval from the completion of the exposure to the start of the mea-

surements have been of 1 hour max and the next exposure has started after a maximum of 2 hours.

Bias Condition During Irradiation

In total 7 samples were tested:

- 4 samples with $V_{GS} = +15V$ and $V_{DS} = 0$ (S/N N01,N02,N03,N04);
- 3 samples with $V_{GS} = +8V$ and $V_{DS} = 0$ and VDS=0V (S/N N05,N06,N07);
- 1 sample as reference device (not irradiated).

2.1.3 Measurements Setup

No in-situ measurements were performed during irradiation. In the following table 2.4 there are the measured electrical parameters:

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	V_{DS}= 200V			10	mA
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	V_{DS}= 150V			10	mA
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	V_{DS}= 100V			10	mA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}= 20V V_{GS}= -20V			100	nA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}= 10V V_{GS}= -10V			100	nA
$V_{GS(th)}$	Gate threshold voltage	I_D=1mA	0.5		2	V

Table 2.4: Measured Parameters, Min-Max Limits and Test conditions (Ta=25°C)

The electrical measurements have been performed at room temperature using an Agilent 4156C *Precision Semiconductor Parameter Analyzer* with an Agilent 41501B *SMU and Pulse Generator Expander* and an Agilent 16442A *text Fixture*.
For the electrical measurements two configurations have been used for the measurement of the threshold voltage: in the first configuration $V_{DS} = 2.5V$

and V_{GS} is variable from -2.0V to 2V (Fig. 2.3a), in the second configuration $V_{DS} = V_{GS}$ are both variables from 0V to 2V (Fig. 2.3b). The other two configurations are for the measurement of gate current and drain current. For the gate current measurement $V_{DS} = 0$ and V_{GS} is variable @ -20V, -10V, 0V, 10V, 20V (Fig. 2.3c). For the drain current measurement $V_{GS} = 0$ and V_{DS} is variable @ 100V, 150V, 200V (Fig. 2.3d).

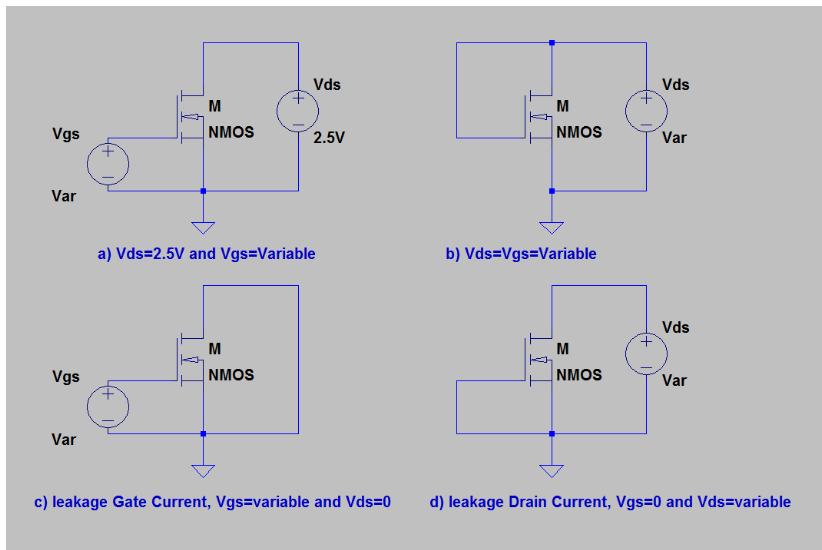

Figure 2.3: Configuration for the electrical measurement.

2.1.4 Test Results

In this section the results of the electrical measurements are shown with plots. These results include:

- Threshold voltage(for each configuration there are measurements @ 250μA and 1mA);
- Gate leakage Current;
- Drain leakage Current;
- $I_d - V_{GS}$ Characteristics.

Threshold Voltage ($V_{GS} = +15V$)

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.3a)

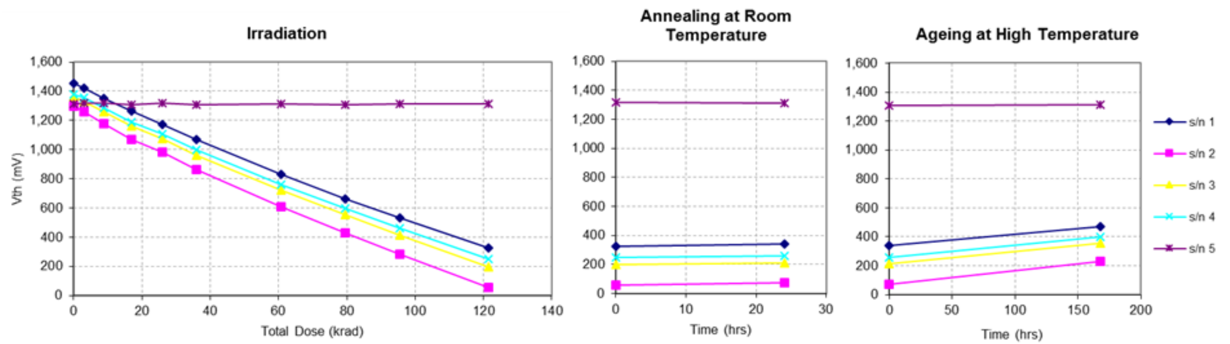

Figure 2.4: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) ($V_{GS} = +15V$) (configuration Fig. 2.3a)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.3a)

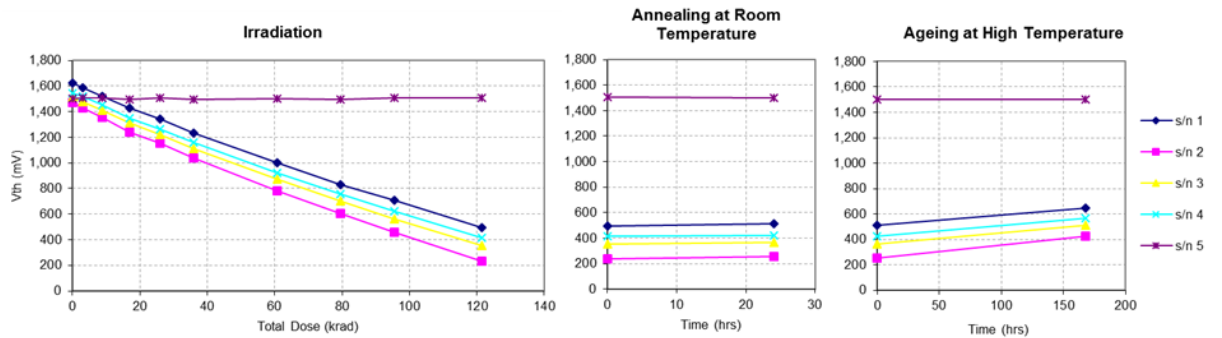

Figure 2.5: Irradiation [rad (Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) ($V_{GS} = +15V$) (configuration Fig. 2.3a)

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.3b)

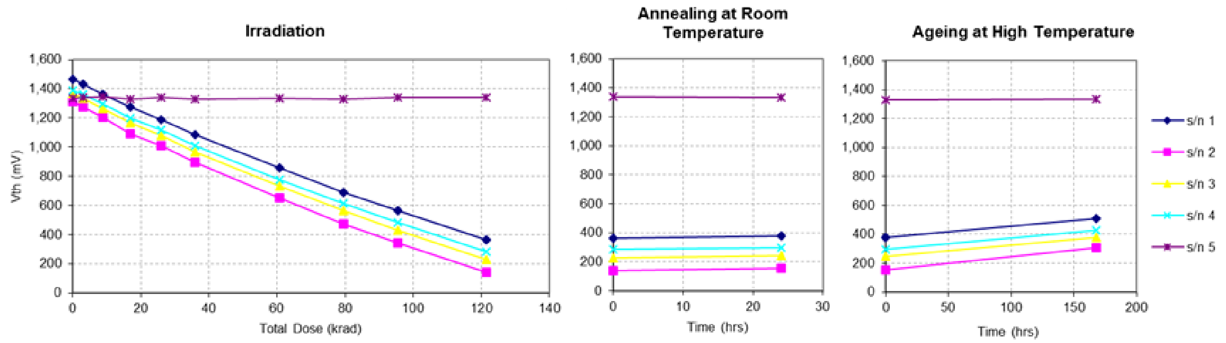

Figure 2.6: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) ($V_{GS} = +15V$) (configuration Fig. 2.3b)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.3b)

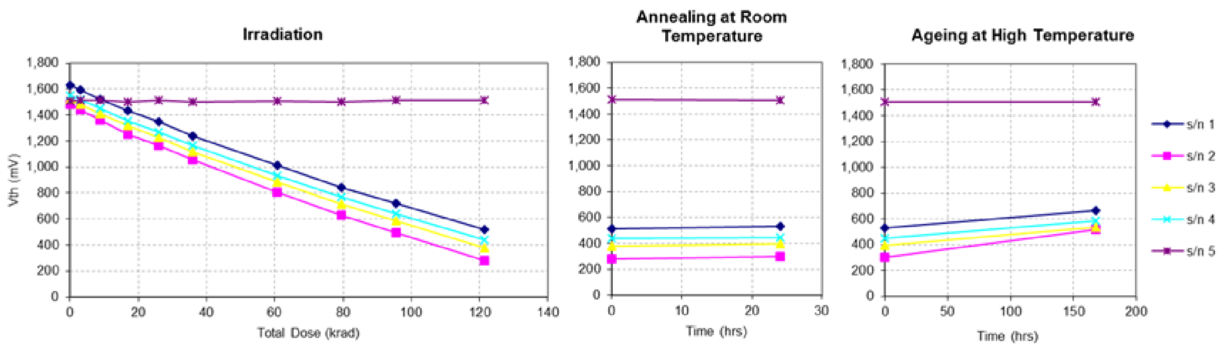

Figure 2.7: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) ($V_{GS} = +15V$) (configuration Fig. 2.3b)

Gate Leakage Current I_{GSS} $(V_{GS} = +15V)$

- I_{GSS}[nA] @ $V_{GS} = -20V$ (configuration Fig. 2.3c)

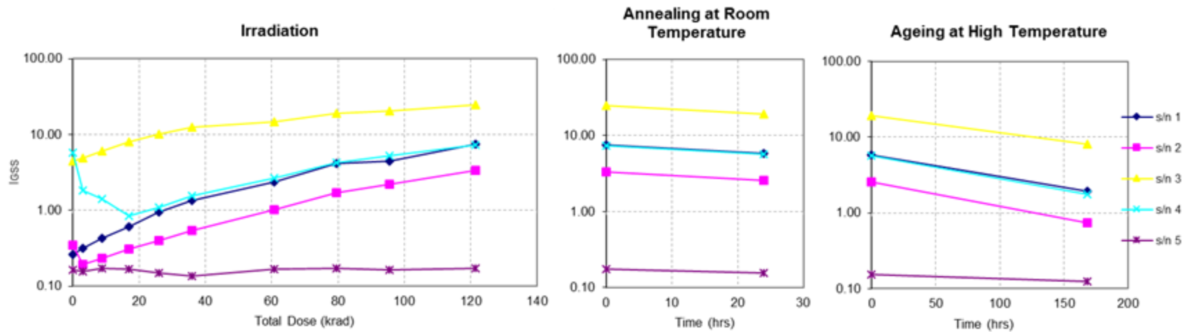

Figure 2.8: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = -20V$) $(V_{GS} = +15V)$ (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = -10V$ (configuration Fig. 2.3c)

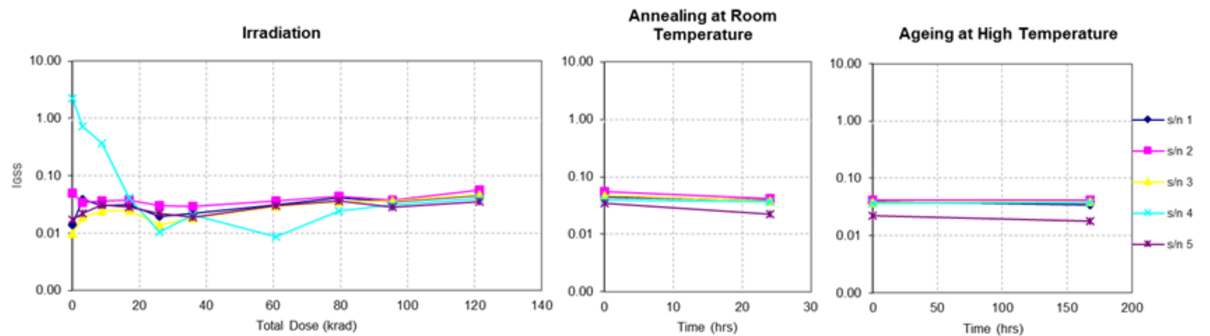

Figure 2.9: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = -10V$) $(V_{GS} = +15V)$ (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = 10V$ (configuration Fig. 2.3c)

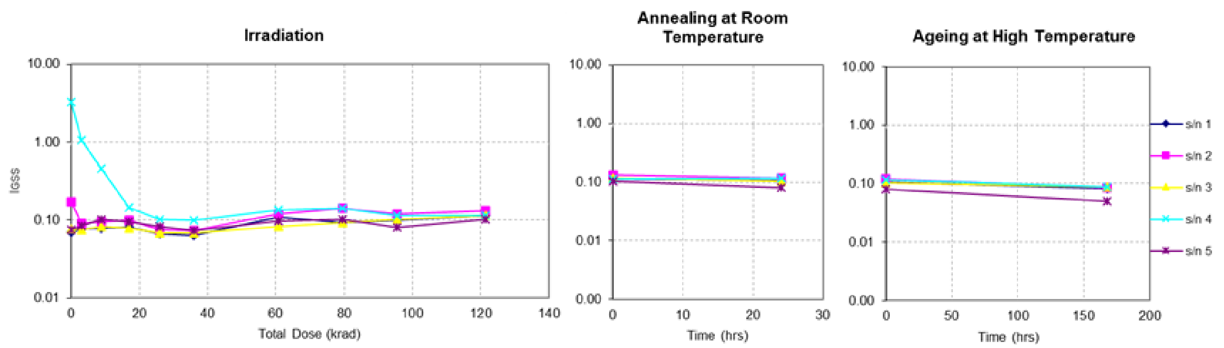

Figure 2.10: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = 10V$) ($V_{GS} = +15V$) (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = 20V$ (configuration Fig. 2.3c)

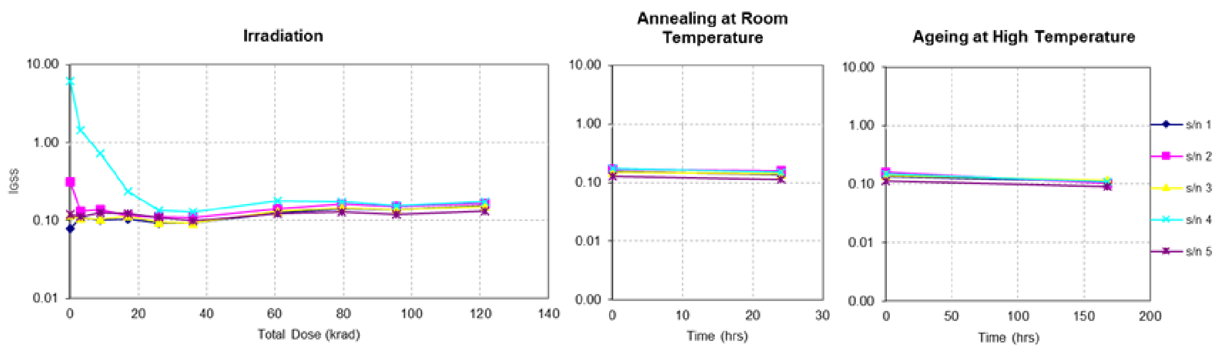

Figure 2.11: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = 20V$) ($V_{GS} = +15V$) (configuration Fig. 2.3c)

Drain Leakage Current I_{DSS} ($V_{GS} = +15V$)

- I_{DSS}[mA] @ $V_{DS} = 100V$ (configuration Fig. 2.3d)

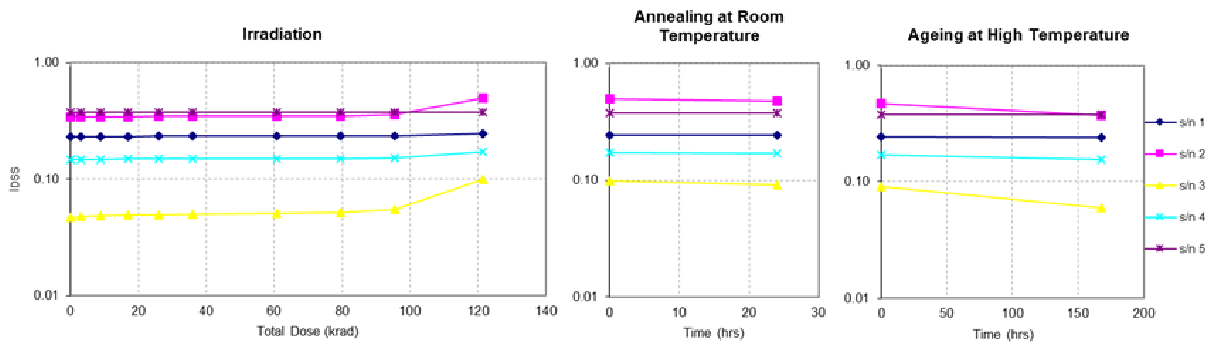

Figure 2.12: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 100V$) ($V_{GS} = +15V$) (configuration Fig. 2.3d)

- I_{DSS}[mA] @ $V_{DS} = 150V$ (configuration Fig. 2.3d)

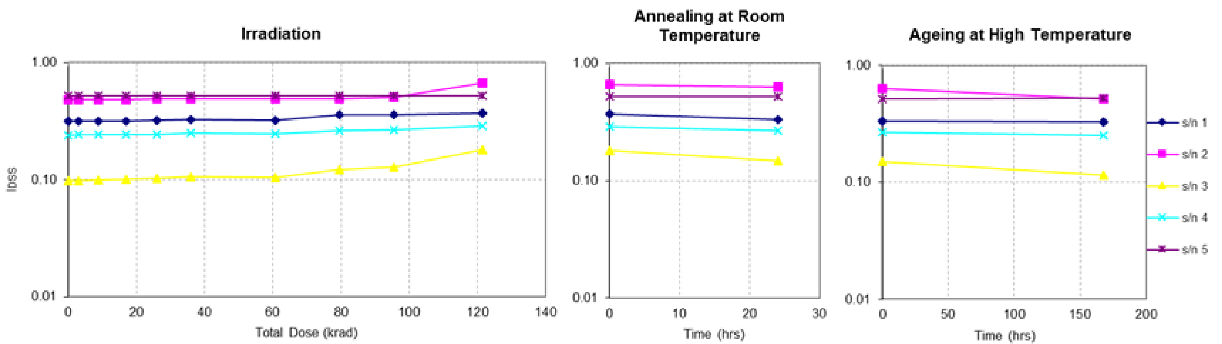

Figure 2.13: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 150V$) ($V_{GS} = +15V$) (configuration Fig. 2.3d)

- I_{DSS}[mA] @ $V_{DS} = 200V$ (configuration Fig. 2.3d)

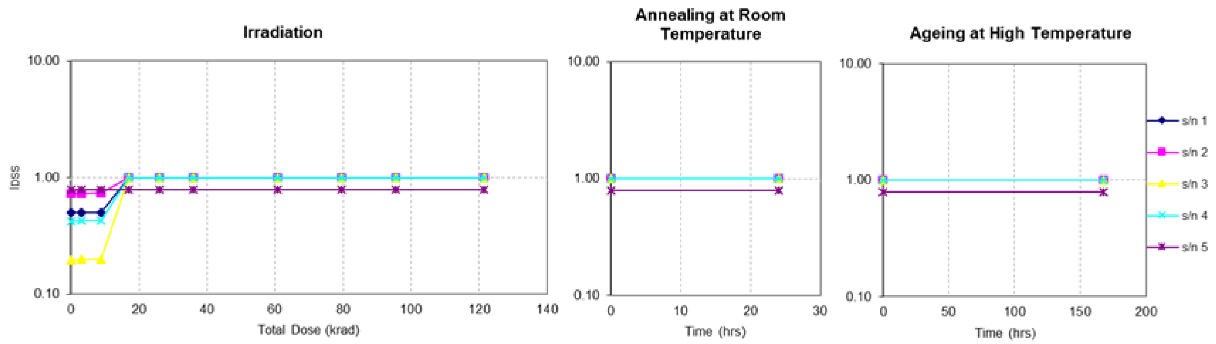

Figure 2.14: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 200V$) ($V_{GS} = +15V$) (configuration Fig. 2.3d)

In this plot the last values shown are at the 8.9krad step because after the 17 krad step the curves have reached the compliance that has been set at 1mA.

- $I_D - V_{GS}$ Characteristics ($V_{GS} = +15V$)

In the following plots (Fig. 2.15): Run00 is the first measurement before the irradiation, from Run01 to Run09 are the measurements during irradiation, Run10 is the measurement after annealing and Run11 is the measurement after ageing.

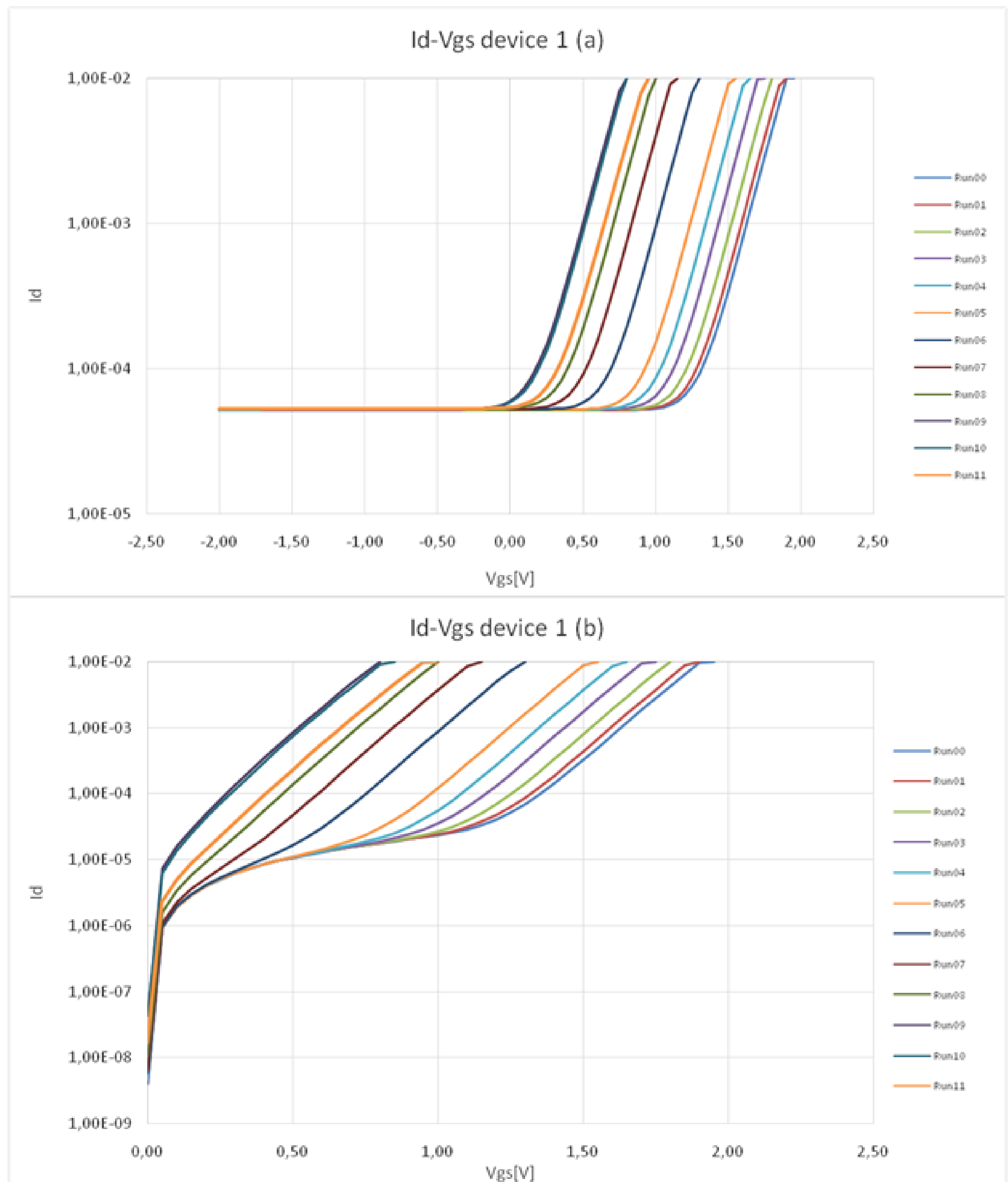

Figure 2.15: $I_D - V_{GS}$ Characteristics ($V_{GS} = +15V$): a) Configuration Fig. 2.3a, b) Configuration Fig. 2.3b

Threshold Voltage ($V_{GS} = +8V$)

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.3a)

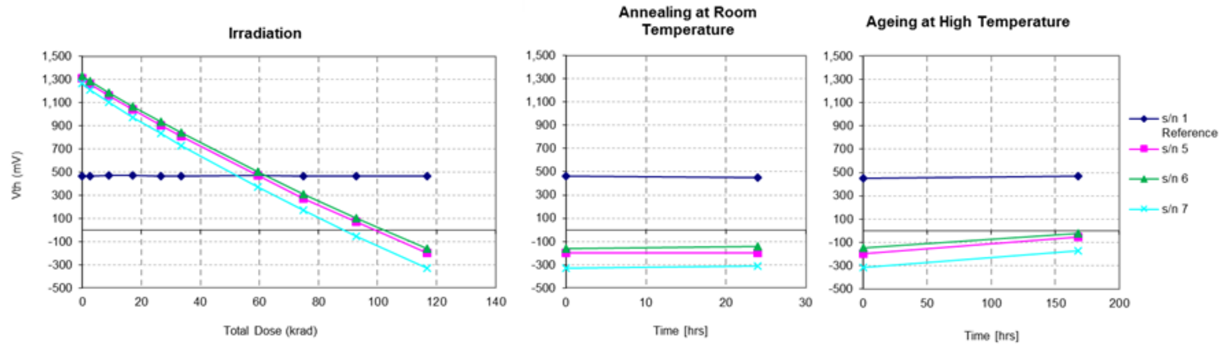

Figure 2.16: Irradiation [rad (Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) ($V_{GS} = +8V$) (configuration Fig. 2.3a)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.3a)

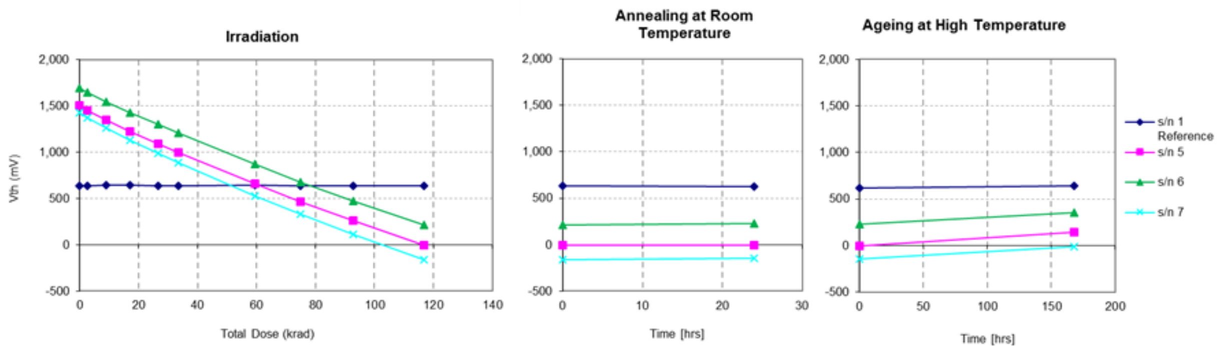

Figure 2.17: Irradiation [rad (Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) ($V_{GS} = +8V$) (configuration Fig. 2.3a)

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.3b)

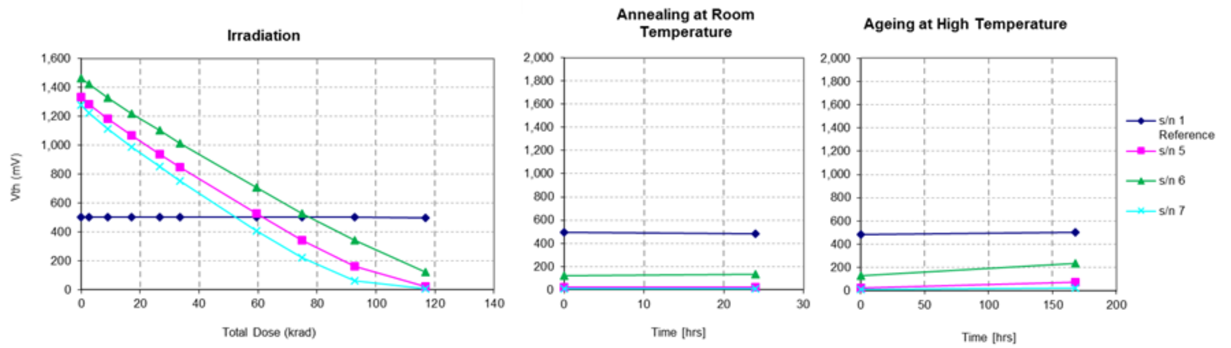

Figure 2.18: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) ($V_{GS} = +8V$) (configuration Fig. 2.3b)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.3b)

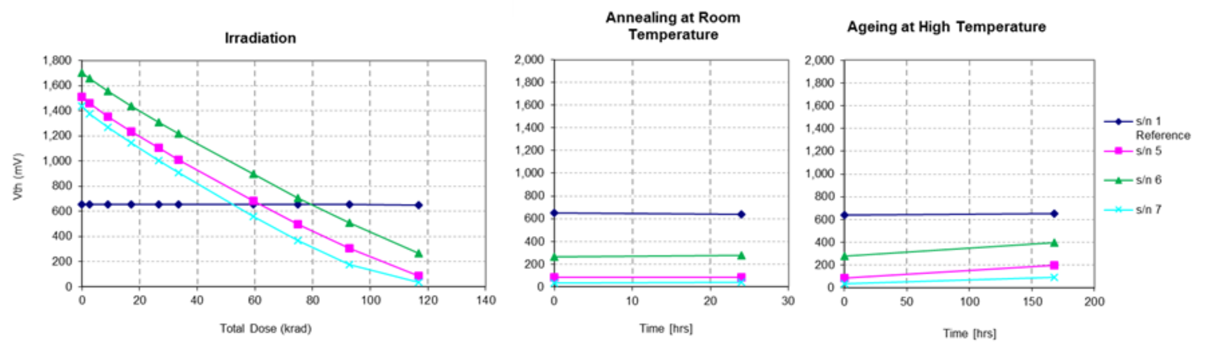

Figure 2.19: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) ($V_{GS} = +8V$) (configuration Fig. 2.3b)

Gate Leakage Current I_{GSS} ($V_{GS} = +8V$)

- I_{GSS}[nA] @ $V_{GS} = -20V$ (configuration Fig. 2.3c)

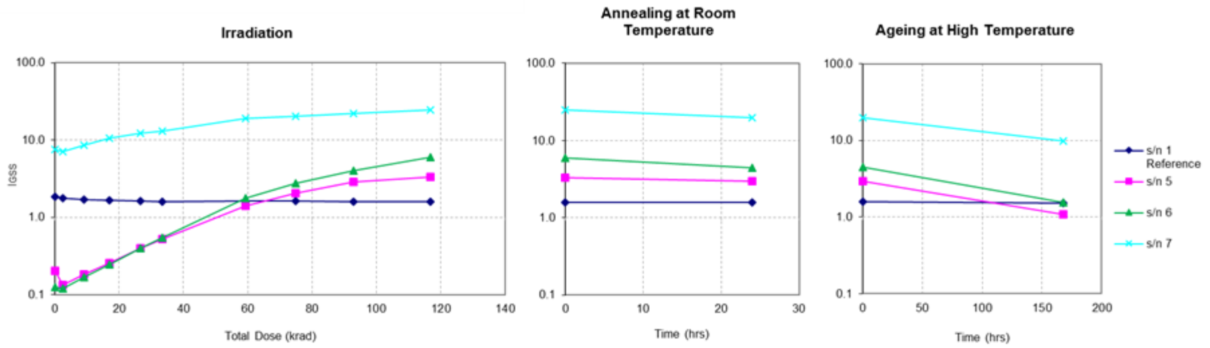

Figure 2.20: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = -20V$) ($V_{GS} = +8V$) (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = -10V$ (configuration Fig. 2.3c)

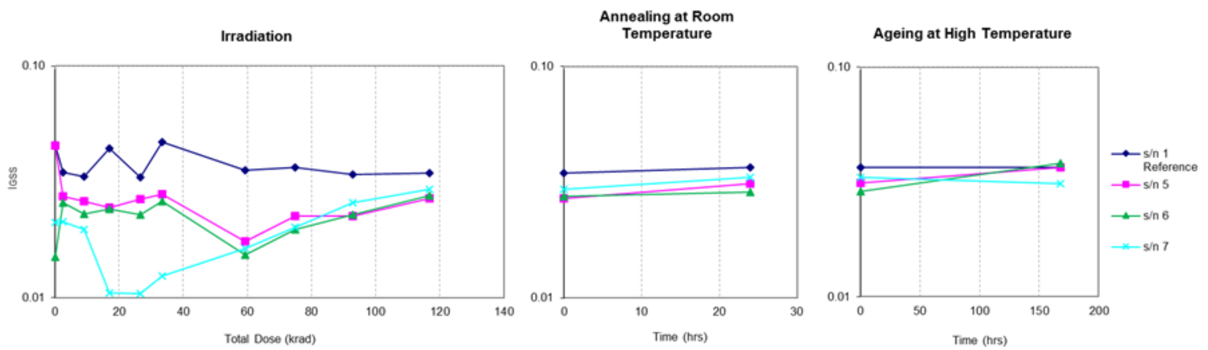

Figure 2.21: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = -10V$) ($V_{GS} = +8V$) (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = 10V$ (configuration Fig. 2.3c)

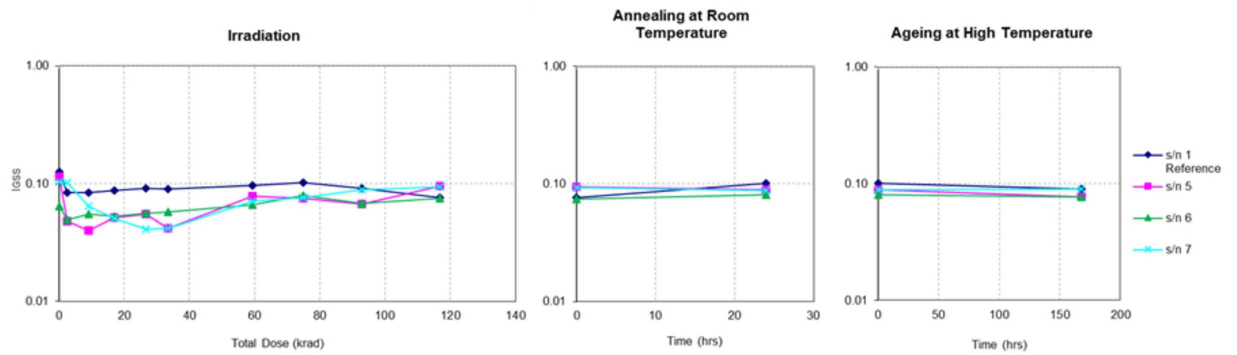

Figure 2.22: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = 10V$) ($V_{GS} = +8V$) (configuration Fig. 2.3c)

- I_{GSS}[nA] @ $V_{GS} = 20V$ (configuration Fig. 2.3c)

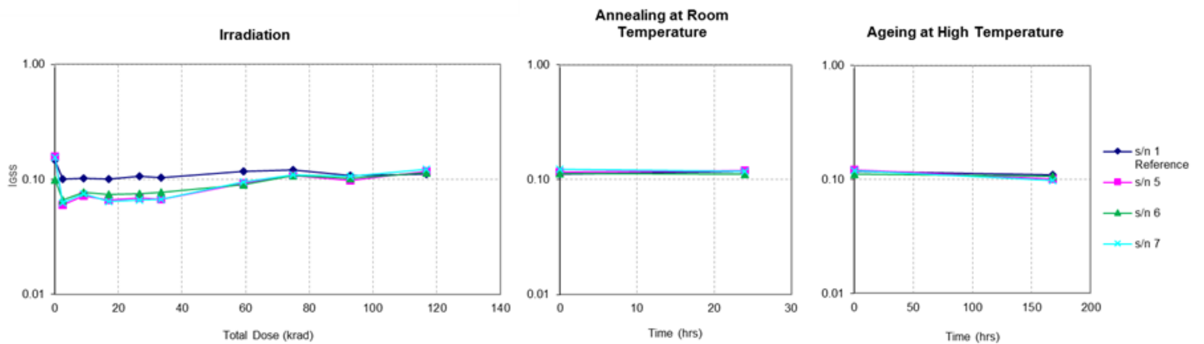

Figure 2.23: Irradiation [rad(Si)], annealing and ageing (I_{GSS}[nA] @ $V_{GS} = 20V$) ($V_{GS} = +8V$) (configuration Fig. 2.3c)

Drain Leakage Current I_{DSS} ($V_{GS} = +8V$)

- I_{DSS}[mA] @ $V_{DS} = 100V$ (configuration Fig. 2.3d)

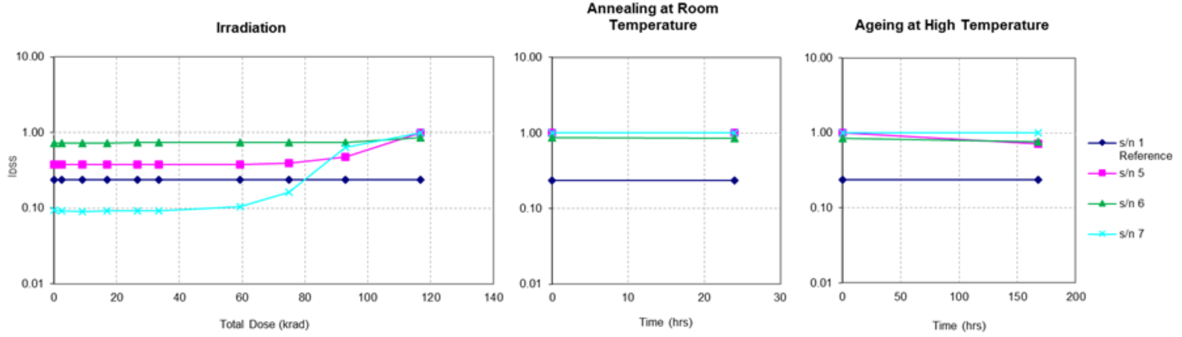

Figure 2.24: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 100V$) ($V_{GS} = +8V$) (configuration Fig. 2.3d)

- I_{DSS}[mA] @ $V_{DS} = 150V$ (configuration Fig. 2.3d)

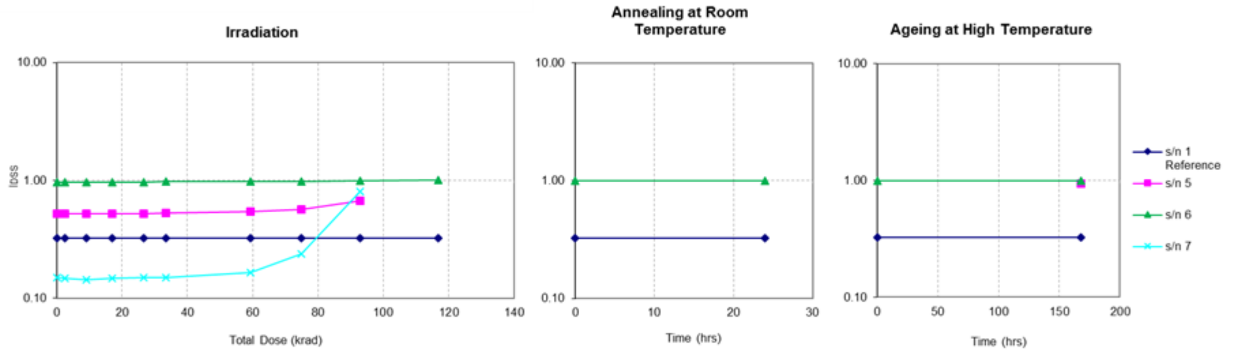

Figure 2.25: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 150V$) ($V_{GS} = +8V$) (configuration Fig. 2.3d)

In this plot the values are considered until the compliance that it has been set at 1mA.

- I_{DSS}[mA] @ $V_{DS} = 200V$ (configuration Fig. 2.3d)

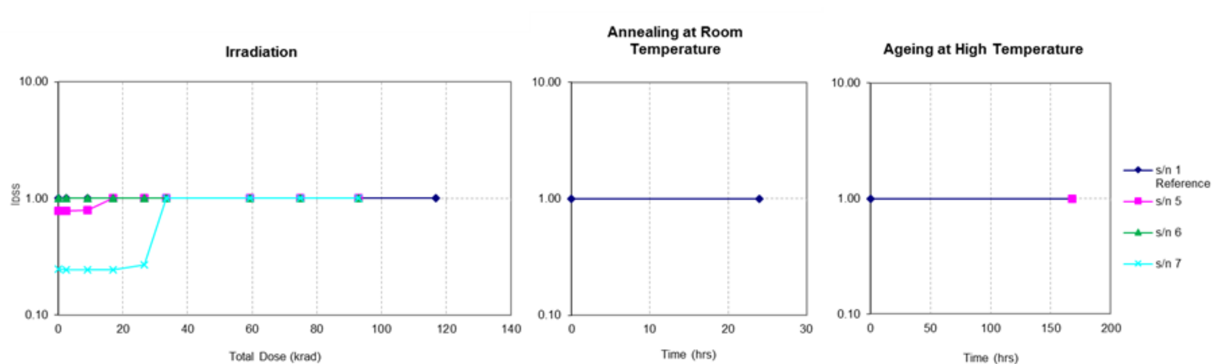

Figure 2.26: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = 200V$) ($V_{GS} = +8V$) (configuration Fig. 2.3d)

In this plot the values are considered until the compliance that has been set at 1mA.

- $I_D - V_{GS}$ Characteristics ($V_{GS} = +8V$)

In the following plots (Fig. 2.27: Run00 is the first measurement before the irradiation, Run01 to Run09 are the measurements during irradiation, Run10 is the measurement after annealing and Run11 is the measurement after ageing.

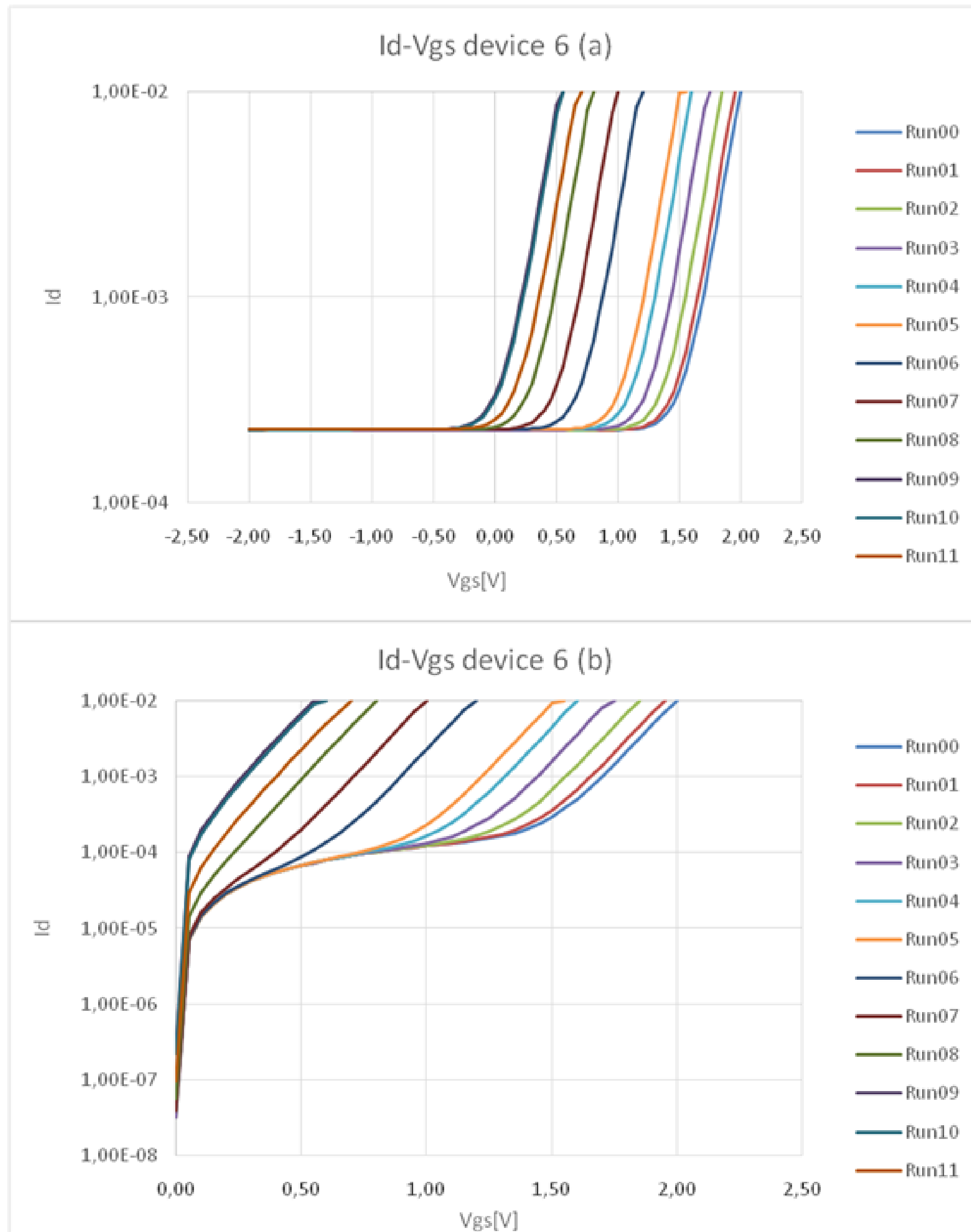

Figure 2.27: $I_D - V_{GS}$ Characteristics ($V_{GS} = +8V$): a) Configuration Fig. 2.3a, b) Configuration Fig. 2.3b

2.1.5 Discussion

Based on the electrical results summarized above for the tested device with bias $V_{GS} = +15V$:

- Device N01 $\Delta V_{th} = 1.11V$ @ 121.57krad
- Device N02 $\Delta V_{th} = 1.19V$ @ 121.57krad
- Device N03 $\Delta V_{th} = 1.14V$ @ 121.57krad
- Device N04 $\Delta V_{th} = 1.11V$ @ 121.57krad

Instead for the tested device with bias $V_{GS} = +8V$:

- Device N05 $\Delta V_{th} = 1.42V$ @ 116.88krad
- Device N06 $\Delta V_{th} = 1.43V$ @ 116.88krad
- Device N07 $\Delta V_{th} = 1.40V$ @ 116.88krad

The following table shows the comparison, in percentage, of the degradation of the threshold voltage between the two different bias conditions $V_{GS} = +15V$ and $V_{GS} = +8V$:

Bias	Min	Max	Average	Std.Dev.
Vgs = +8V	84.49%	97.63%	92.17%	6.85%
Vgs = +15V	68.3%	81.0%	74.0%	5.4%

Table 2.5: Table: Comparison between $V_{GS} = +15V$ and $V_{GS} = +8V$

N-channel power MOSFETs @ $V_{GS} = +8V$ failed after 75 krad and N-channel power MOSFETs @ $V_{GS} = +15V$ failed after 100 krad. So the bias condition with $V_{GS} = +8V$ is the worst-case. It is possible to explain this fact, with the observation that the charge yield and the cross-section in the oxide depend on the electric field. Observing figure 1.6 it is possible to note that the worst-case is with an intermediate bias condition.

After annealing and ageing there was no rebound effect in both conditions.

From the analysis of the $I_D - V_{GS}$ characteristics of the samples, it is possible to note that: the curves have shown only a drift of the threshold voltage, instead the sub-threshold slope has not had important changes. This drift of the threshold voltage can be explained with the trapping of positive charge in the oxide due to the effect of TID. Instead, the lack of changes in the slope means that there has not been interface state generation.

2.2 Low dose rate Co60 TID Tests of 100 krad, 150V, 10A Power MOSFET P-channel prototype

2.2.1 Introduction

A total dose characterization test of 150V, 10A Power MOSFET P-channel prototype was performed at the ESTEC Co60 Facility. The transistors have been exposed to a total accumulated dose of 100 krad(Si), using a constant low dose rate of 360 rad(Si)/h (6 rad(Si)/min). The purpose of this test is to evaluate the TID tolerance of the MOSFET. The tests have been performed in accordance with the ESCC Basic Specification No. 22900 [6].

2.2.2 Experimental Conditions

Tested Devices

Part type	Prototype
Manufacturer	STMicroelectronics
Function	150V, 10A P-channel MOSFET
Family	Transistor
Group	-
Package	TO3

Table 2.6: Information Power MOSFET P-channel

Irradiation Test Conditions

For the needed dose rate of 360 rad/h, the Dose Rate to Distance calculator provided by the web page of the facilities has been used [7], giving a required distance of 199 cm between the device and the source and a uniform irradiation area of 92×92 cm. The irradiation has been performed at room temperature (see fig. 2.2). The radiation test steps, for the two biased conditions, are reported in the following table 2.7:

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(Si)	krad(Si)	rad(Si)/min	hours	°C
1	3.000	0	6		Room
2	5.927	3.000	6		Room
3	8.084	8.927	6		Room
4	8.900	17.011	6		Room
5	10.156	25.911	6		Room
6	24.758	36.067	6		Room
7	18.679	60.825	6		Room
8	15.972	79.504	6		Room
9	26.094	95.476	6		Room
10		121.570	6		Room
11		121.570	-	24	Room
12		121.570	-	168	100

Table 2.7: The Radiation test steps on Power MOSFETs with biased $V_{GS} = -15V$ and $V_{GS} = -12V$

At the completion of each irradiation step, intermediate electrical measurements have been carried out according to the electrical measurement parameters (Fig. 2.4). Following the ESCC 22900 recommendations, the time interval from the completion of the exposure to the start of the measurements have been of 1 hour max and the next exposure has started after a maximum of 2 hours.

Bias Condition During Irradiation

In total 8 samples were tested:

- 4 Samples with $V_{GS} = -12V$ and $V_{DS} = 0$ (S/N P01,P02,P03,P04);

- 4 Samples with $V_{GS} = -15V$ and $V_{DS} = 0$ (S/N P05,P06,P07,P08);
- 1 sample as Reference device (Not irradiated, S/N P09).

2.2.3 Measurements Setup

No in-situ measurements were performed during irradiation. In the following table 2.8 there are the measured electrical parameters:

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	Vds=-120V			10	mA
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	Vds=-75V			10	mA
I_{DSS}	Zero gate voltage drain current(V_{GS} = 0)	Vds=-30V			10	mA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}=10V V_{GS}=-10V			10	uA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}=20V V_{GS}=-20V			10	uA
$V_{GS(th)}$	Gate threshold voltage	I_D=1mA	-6		-3.5	V

Table 2.8: Measured Parameters, Min-Max Limits and Test conditions (Ta=25°C)

The electrical measurements have been performed at room temperature using an Agilent 4156C *Precision Semiconductor Parameter Analyzer* with an Agilent 41501B *SMU and Pulse Generator Expander* and an Agilent 16442A *text Fixture*.
For the electrical measurements two configurations have been used for the measurement of the threshold voltage: in the first configuration $V_DS = 2.5V$ and V_{GS} is variable from -6.0V to 2V (Fig. 2.28a), in the second configuration $V_{DS} = V_{GS}$ are both variables from -6V to 0V (Fig. 2.28b). The other two configurations are for the measurement of gate current and drain current. For the gate current measurement $V_{DS} = 0$ and V_{GS} is variable @ -20V, -10V, 0V, 10V, 20V (Fig. 2.28c). For the drain current measurement $V_{GS} = 0$ and V_{DS} is variable @ -30V, -75V, -120V (Fig. 2.28d).

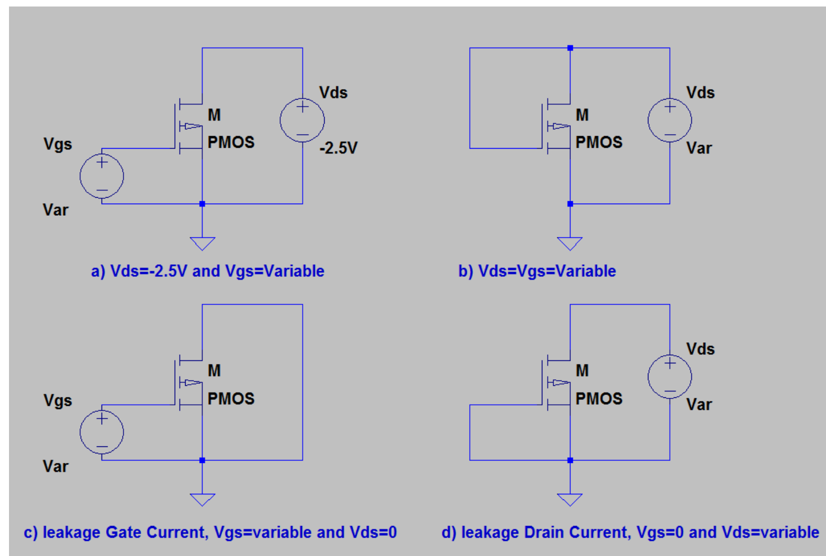

Figure 2.28: Configuration for the electrical measurement for p-Channel.

2.2.4 Test Results

In this section the results of the electrical measurements are shown with plots. These results include:

- Threshold voltage(for each configuration there are measurements @ 250μA and 1mA);
- Gate leakage Current;
- Drain leakage Current;
- $I_d - V_{GS}$ Characteristics .

Threshold Voltage

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.28a)

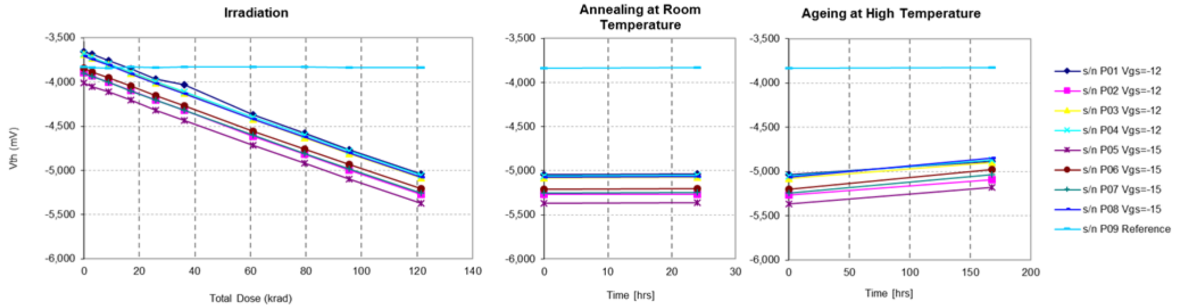

Figure 2.29: Irradiation [rad (Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) (configuration Fig. 2.28a)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.28a)

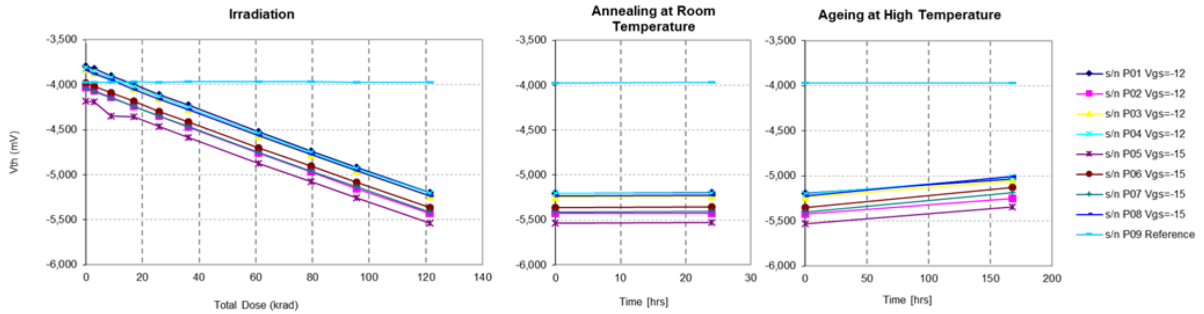

Figure 2.30: Irradiation [rad (Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) (configuration Fig. 2.28a)

- $V_{GS_{th}}$[mV] @ $I_d = 250\mu A$ (configuration Fig. 2.28b)

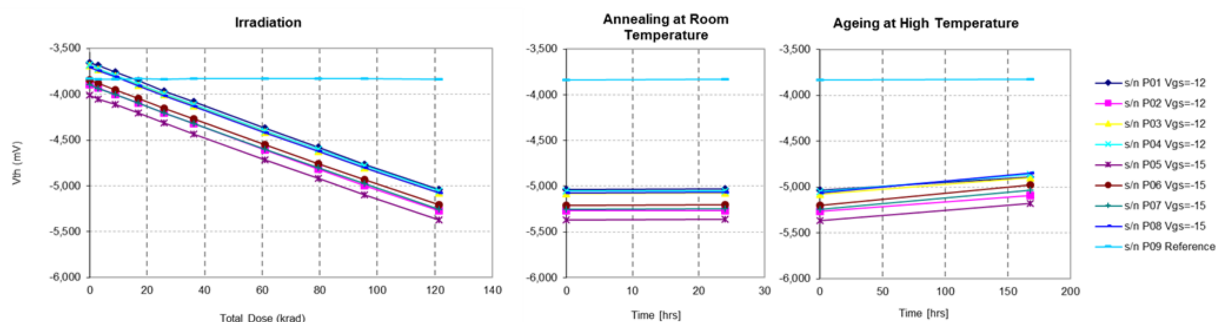

Figure 2.31: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 250\mu A$) (configuration Fig. 2.28b)

- $V_{GS_{th}}$[mV] @ $I_d = 1mA$ (configuration Fig. 2.28b)

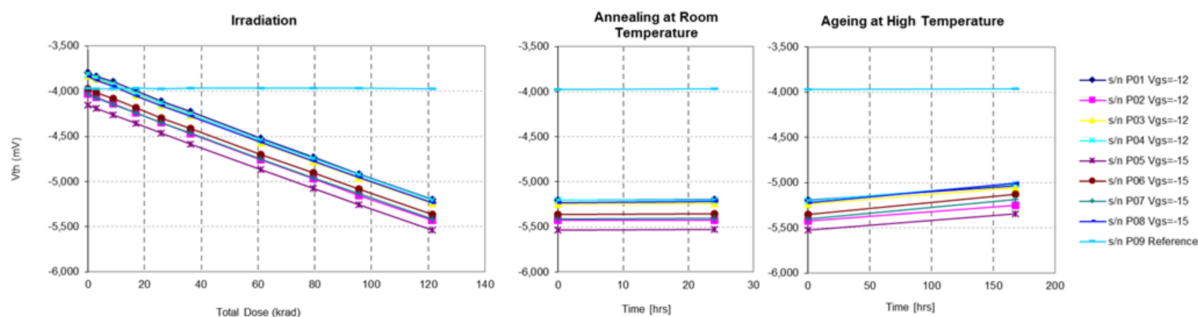

Figure 2.32: Irradiation [rad(Si)], annealing and ageing ($V_{GS_{th}}$[mV]@ $I_d = 1mA$) (configuration Fig. 2.28b)

Gate Leakage Current I_{GSS}

- $I_{GSS}[\mu A]$ @ $V_{GS} = -20V$ (configuration Fig. 2.28c)

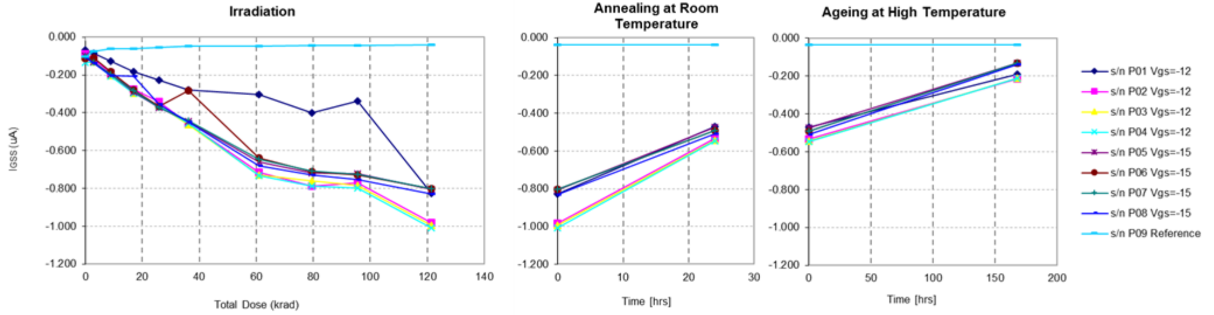

Figure 2.33: Irradiation [rad(Si)], annealing and ageing ($I_{GSS}[\mu A]$ @ $V_{GS} = -20V$) (configuration Fig. 2.28c)

- $I_{GSS}[\mu A]$ @ $V_{GS} = -10V$ (configuration Fig. 2.28c)

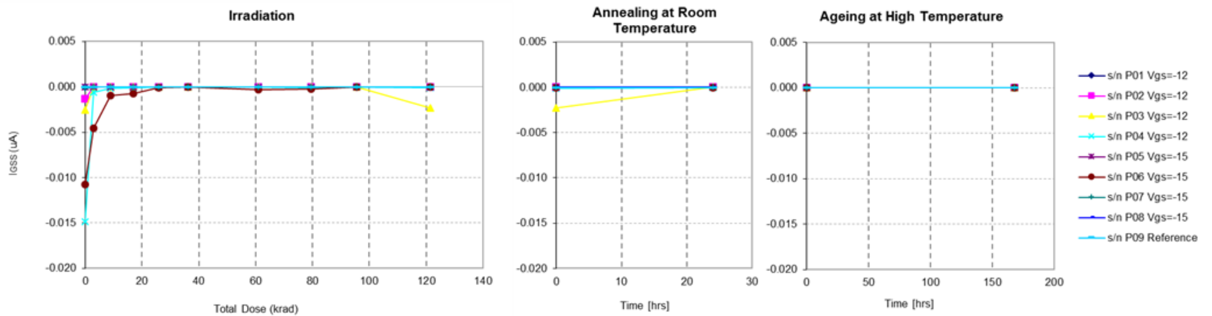

Figure 2.34: Irradiation [rad(Si)], annealing and ageing ($I_{GSS}[\mu A]$ @ $V_{GS} = -10V$) (configuration Fig. 2.28c)

- $I_{GSS}[\mu A]$ @ $V_{GS} = 10V$ (configuration Fig. 2.28c)

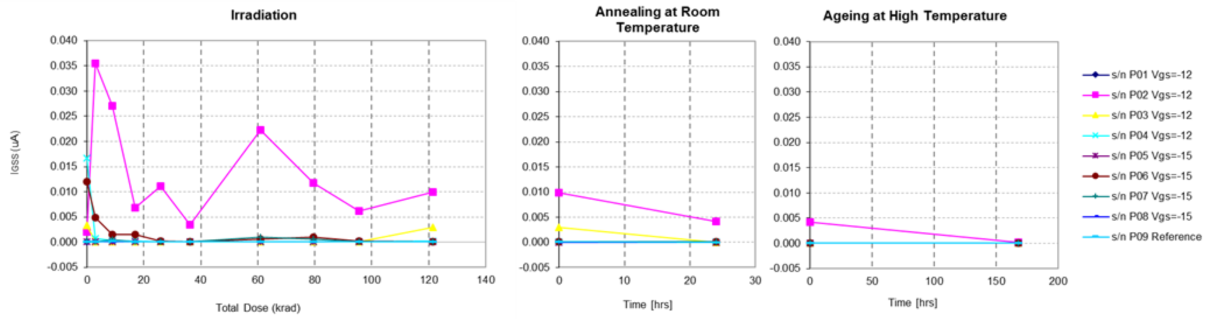

Figure 2.35: Irradiation [rad(Si)], annealing and ageing ($I_{GSS}[\mu A]$ @ $V_{GS} = 10V$) (configuration Fig. 2.28c)

- $I_{GSS}[\mu A]$ @ $V_{GS} = 20V$ (configuration Fig. 2.28c)

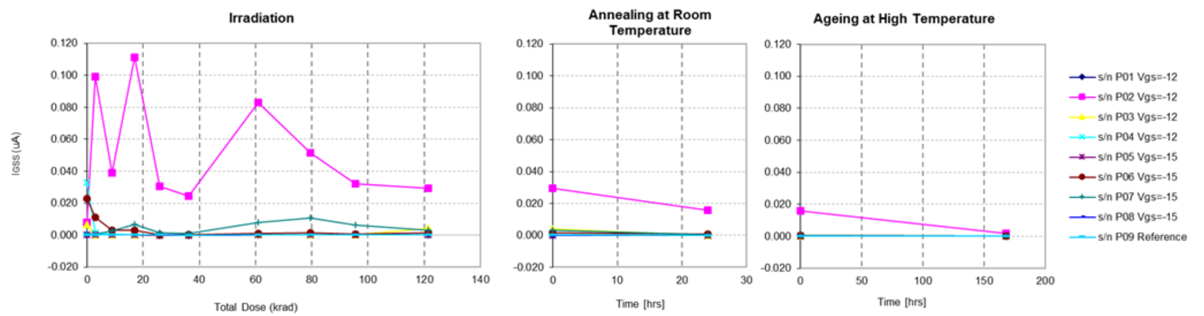

Figure 2.36: Irradiation [rad(Si)], annealing and ageing ($I_{GSS}[\mu A]$ @ $V_{GS} = 20V$) (configuration Fig. 2.28c)

Drain Leakage Current I_{DSS}

- I_{DSS}[mA] @ $V_{DS} = -30V$ (configuration Fig. 2.28d)

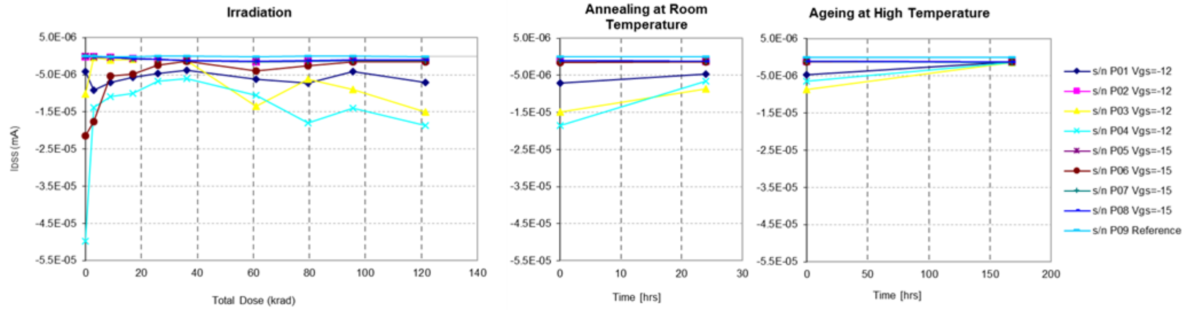

Figure 2.37: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = -30V$) (configuration Fig. 2.28d)

- I_{DSS}[mA] @ $V_{DS} = -75V$ (configuration Fig. 2.28d)

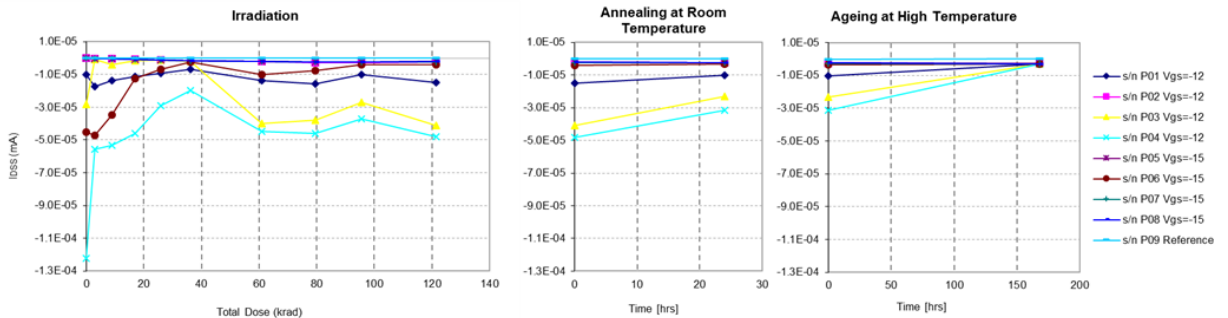

Figure 2.38: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = -75V$) (configuration Fig. 2.28d)

- I_{DSS}[mA] @ $V_{DS} = -120V$ (configuration Fig. 2.28d)

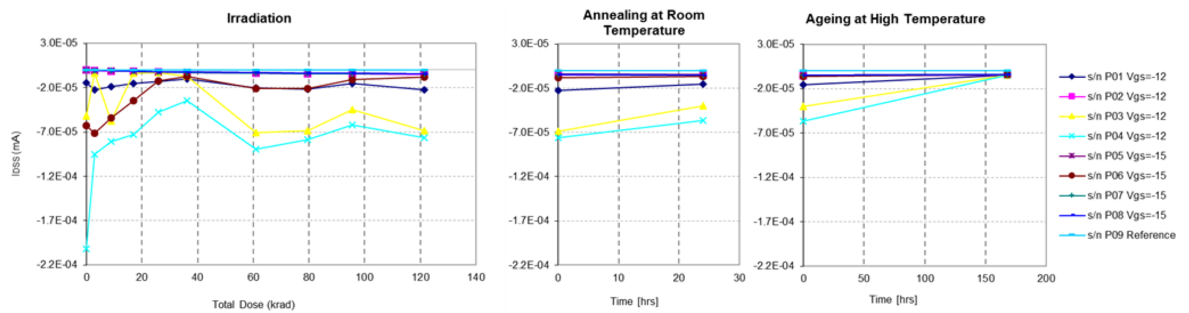

Figure 2.39: Irradiation [rad(Si)], annealing and ageing (I_{DSS}[mA] @ $V_{DS} = -120V$) (configuration Fig. 2.28d)

- $I_D - V_{GS}$ Characteristic

The following plots show the I-V characteristics of one device for $V_{GS} = -12V$ (Fig. 2.40) and $V_{GS} = -15V$ (Fig. 2.41) respectively: Run00 is the first measurement before the irradiation, Run01 to Run09 are the measurements during irradiation, Run10 is the measurement after annealing and Run11 is the measurement after ageing.

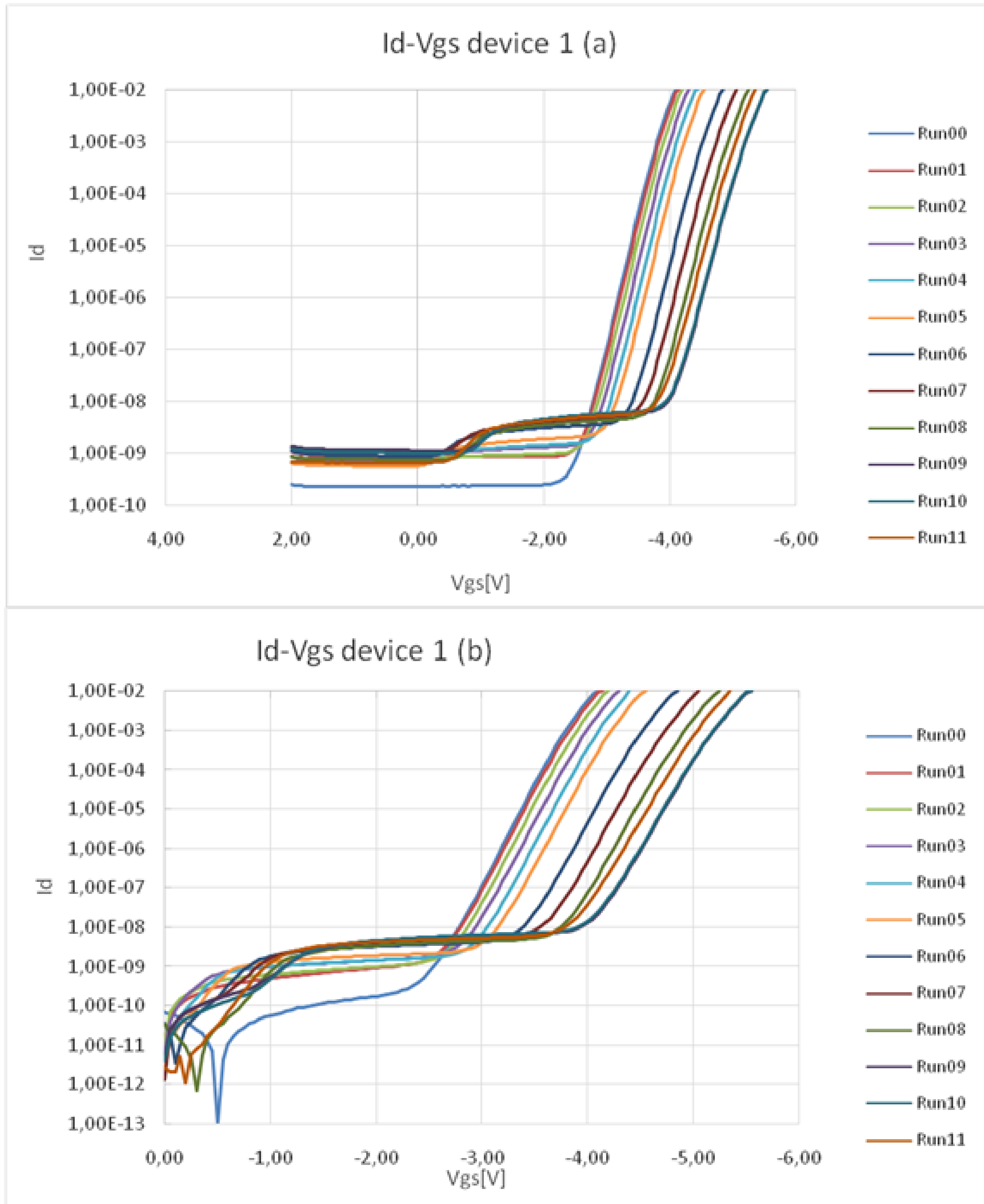

Figure 2.40: $I_D - V_{GS}$ Characteristics ($V_{GS} = -12V$): a) Configuration Fig. 2.28a, b) Configuration Fig. 2.28b

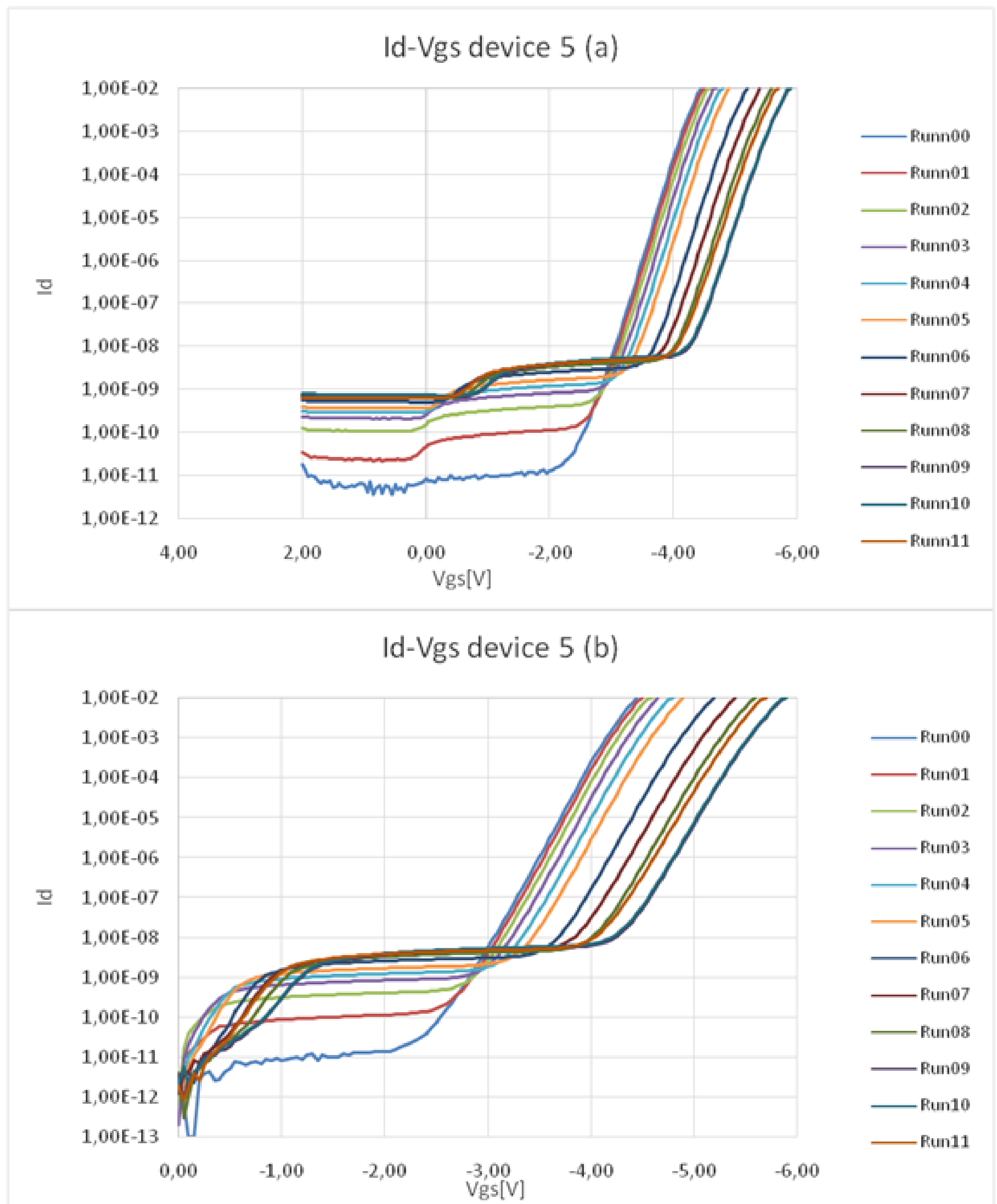

Figure 2.41: $I_D - V_{GS}$ Characteristics ($V_{GS} = -15V$): a) Configuration Fig. 2.28a, b) Configuration Fig. 2.28b

2.2.5 Discussion

Based on the electrical results summarized above:

- Device P01 $\Delta V_{th} = 1.41V$ @ 121.57krad ($V_{GS} = -12V$)
- Device P02 $\Delta V_{th} = 1.40V$ @ 121.57krad ($V_{GS} = -12V$)
- Device P03 $\Delta V_{th} = 1.42V$ @ 121.57krad ($V_{GS} = -12V$)
- Device P04 $\Delta V_{th} = 1.39V$ @ 121.57krad ($V_{GS} = -12V$)
- Device P05 $\Delta V_{th} = 1.38V$ @ 121.57krad ($V_{GS} = -15V$)
- Device P06 $\Delta V_{th} = 1.38V$ @ 121.57krad ($V_{GS} = -15V$)
- Device P07 $\Delta V_{th} = 1.38V$ @ 121.57krad ($V_{GS} = -15V$)
- Device P08 $\Delta V_{th} = 1.39V$ @ 121.57krad ($V_{GS} = -15V$)

The following table shows the comparison, in percentage, of the degradation of threshold voltage between the two different bias condition $V_{GS} = -15V$ and $V_{GS} = -12V$:

Bias	Min	Max	Average	Std.Dev.
Vgs = -12V	34.7%	37.2%	36.4%	1.1%
Vgs = -15V	33.4%	36.3%	34.7%	1.2%

Table 2.9: Table: Comparison between $V_{GS} = -15V$ and $V_{GS} = -12V$

P-channel power MOSFETs did not fail after 121.57 krad. Also in this case the worst-case is with the lower value of bias in absolute value as for N-channel.

After annealing and ageing there was no rebound effect in both conditions.

From the analysis of the $I_D - V_{GS}$ characteristics of the samples, it is possible to note that: the curves have shown only a drift of the threshold voltage, instead the sub-threshold slope has not had important changes. This drift of the threshold voltage can be explained with the trapping of positive

charge in the oxide due to the effect of TID. Instead, the lack of changes in the slope means that there has not been interface state generation.

Chapter 3

Dynamic Bias Test on Power MOSFETs

This chapter shows a different method of TID test. The purpose of this technique is to better simulate the real life of the electronic device, a power MOSFETs, and to compare the dynamic bias conditions with the static bias condition test results. To do this test a boost converter was designed, developed and assembled. During the irradiation test, only the power MOSFET was irradiated operating inside the boost converter.

3.1 Introduction

A total dose characterization test of 60V, 40A N-channel Power MOSFET , was performed at the University of Padova X-Ray Facility. The transistors have been exposed to a total accumulated dose of 75 krad(SiO_2), using a constant high dose rate of 36 krad(SiO_2)/h. The purpose of this test is to compare the degradation in dynamic and static bias conditions. The results are shown in the section 3.1.5 with plots.

3.2 Experimental Conditions

3.2.1 Facility

The main characteristics of the X-Ray generator are:

- X-ray tube using a Tungsten target
- power supply voltage: 50 kV
- Current: 5 mA
- Distance tube from the DUT 222 mm
- Laser pointer allows experimenter to align the DUT with the X-ray beam center

All irradiations and measurements have been performed at room temperature (22 ± 3 °C).

3.2.2 Tested Devices

Part type	Prototype
Manufacturer	STMicroelectronics
Function	60V, 40A N-channel MOSFET
Family	Transistor
Group	-
Package	TO3

Table 3.1: Information Power MOSFET N-channel

3.2.3 Irradiation Test Conditions

The radiation test steps are reported in the following table 3.2:

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(SiO_2)	krad(SiO_2)	rad(SiO_2)/min	hours	°C
1	25	0	600		Room
2	25	25	600		Room
3	25	50	600		Room
4		75	600		Room
5		75	-	24	Room
6		75	-	168	100

Table 3.2: The Radiation test steps

At the completion of each irradiating step, intermediate electrical measurements have been carried out to extract the electrical measurement parameters. The time interval from the completion of the exposure to the next exposure, after measurement, is less than of 2 hours.

3.2.4 Bias Condition During Irradiation

In total 3 samples were tested:

- 1 sample with $V_{GS} = +15V$ and $V_{DS} = 0$
- 1 sample with $V_{GS} = 0V$ and $V_{DS} = 0$
- 1 sample in dynamic conditions
- 1 sample as reference device (not irradiated).

For the tested sample in dynamic conditions, only the device was irradiated operating inside the boost converter. The temperature of the device during this test reached 30°C only 5°C more the devices tested in static condition. So the effect of the temperature was not important for the degradation of the device.

3.3 Measurements Setup and Condition

No in-situ measurements were performed during irradiation. In the following table 3.3 there are the measured electrical parameters:

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current($V_{GS}=0$)	$V_{DS}=48V$			10	µA
I_{GSS}	Gate body leakage current ($V_{DS}=0$)	$V_{GS}=20V$ $V_{GS}=-20V$	 -100		100	nA nA
$V_{GS(th)}$	Gate threshold voltage	I_D=1mA	2		4.5	V

Table 3.3: Measured Parameters, Min-Max Limits and Test conditions (Ta=25°C)

The electrical measurements have been performed at room temperature using an **Agilent 4156C** *Precision Semiconductor Parameter Analyzer* and an **Agilent 16442A** *text Fixture*. For the electrical measurements two configurations have been used for the measurement of the threshold voltage: in the first configuration $V_{DS} = 2.5V$ and V_{GS} is variable from -2.0V to 6V (Fig. 3.1a), in the second configuration $V_{DS} = V_{GS}$ are both variables from 0V to 6V (Fig. 3.1b). The other two configurations are for the measurement of gate current and drain current. For the gate current measurement $V_{DS} = 0V$ and V_{GS} is variable @ -20V,-10V, 0V, 10V, 20V (Fig. 3.1c). For the drain current measurement $V_{GS} = 0V$ and V_{DS} is variable @ 24V, 36V, 48V (Fig. 3.1d).

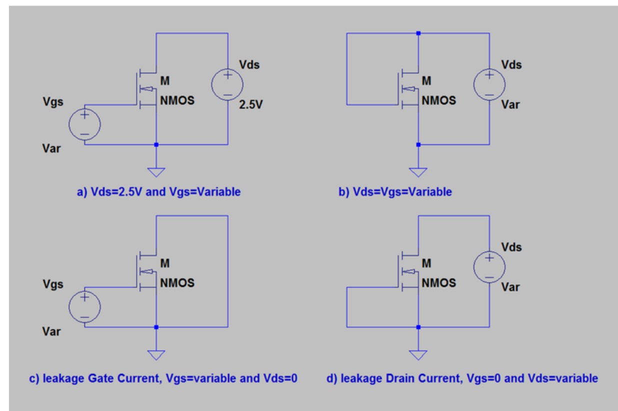

Figure 3.1: Configuration for the electrical measurement.

The measurements after each step were divided in three parts: after the exposure the first electrical measurements have been taken, then with the

oscilloscope the waveforms of the boost converter have been observed and finally other electrical measurements have been taken.

3.4 Boost Converter

This section gives a rapidly explanation on the **boost converter** design.

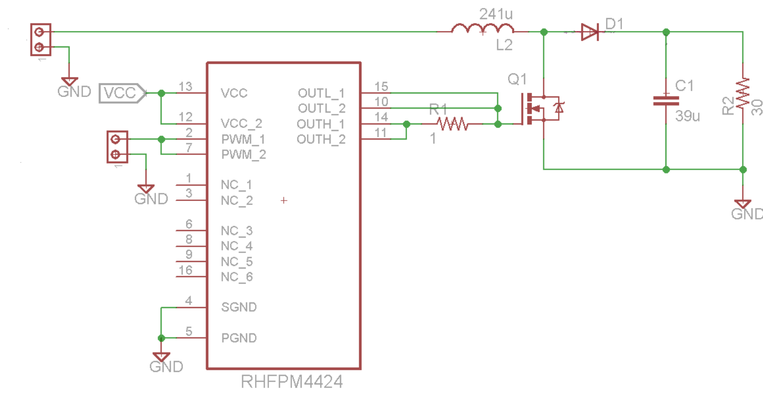

Figure 3.2: Boost Converter

Figure 3.2 shows the basic schematic of the boost converter that consists, in particular, of a power MOSFET that is the device under testing and a driver that pilots the gate of the power MOSFET with a square wave with high level +15V and low level 0V. The ***duty-cycle*** was imposed at $D = 50\%$ and the ***frequency*** of the circuit at $f_s = 100kHz$ (**period** $T_s = 10\mu s$). The other conditions are: ***input voltage*** $V_{in} = 18V$ and ***output current*** $I_{out} = 1.2A$. The others parameters were calculated.

Conversion Factor M

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} = 2 \Rightarrow \textbf{output voltage} V_{out} = 36V \qquad (3.1)$$

Load Resistence R_0

$$R_0 = \frac{V_{out}}{I_{out}} = 30\Omega \qquad (3.2)$$

DC inductor current I_L

$$I_L = \frac{V_{out}}{(1-D)R_0} = 2,4A \tag{3.3}$$

Inductor L

$$L = 241\mu H \tag{3.4}$$

This was a design choice of project and the inductor was built following the indications in [5]

Ripple inductor current Δi_L

$$\Delta i_L = \frac{V_{in}}{2LF_s} D = 0.187A \tag{3.5}$$

Load capacitance C and ripple output voltage Δv_{out}

$$C = 39\mu F \Rightarrow \Delta v_{out} = \frac{V_{out}}{2CR_0 f_s} D = 0.08V \tag{3.6}$$

DC switch current I_S

$$I_S = I_L D = 1.2A \tag{3.7}$$

DC diode current I_D

$$I_D = I_L(1-D) = 1.2A \tag{3.8}$$

Switch rms current I_{Srms}

$$I_{Srms} = I_L\sqrt{D} = 1.69A \tag{3.9}$$

Diode rms current: I_{Drms}

$$I_{Drms} = I_L\sqrt{1-D} = 1.69A \tag{3.10}$$

3.5 Test Results

In this section the results of the electrical measurements are shown. These results include:

- Threshold voltage shift (for each configuration there are measurements @ 1mA);

- Leakage Gate Current;

- Leakage Drain Current;

- $I_d - V_{GS}$ Characteristics.

3.5.1 Threshold Voltage shift

- ΔV_{th}[mV] @ $I_d = 1mA$ (configuration Fig. 3.1a)

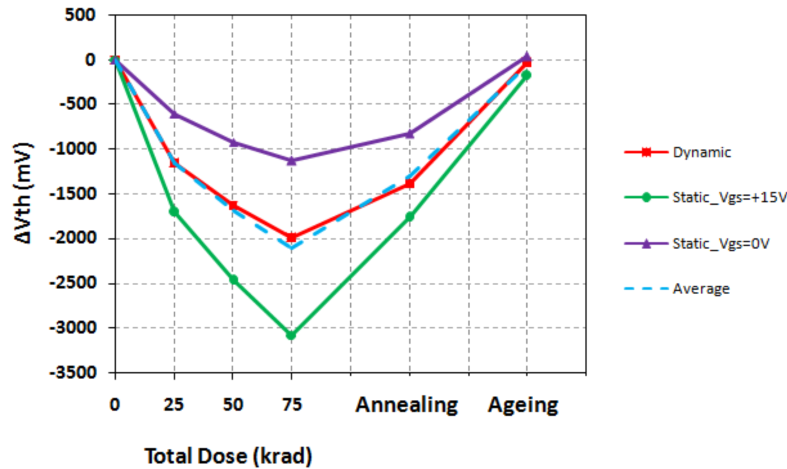

Figure 3.3: Irradiation [rad(Si)], Annealing and Ageing (ΔV_{th}[mV]@ $I_d = 1mA$) for dynamic test. (configuration Fig. 3.1a)

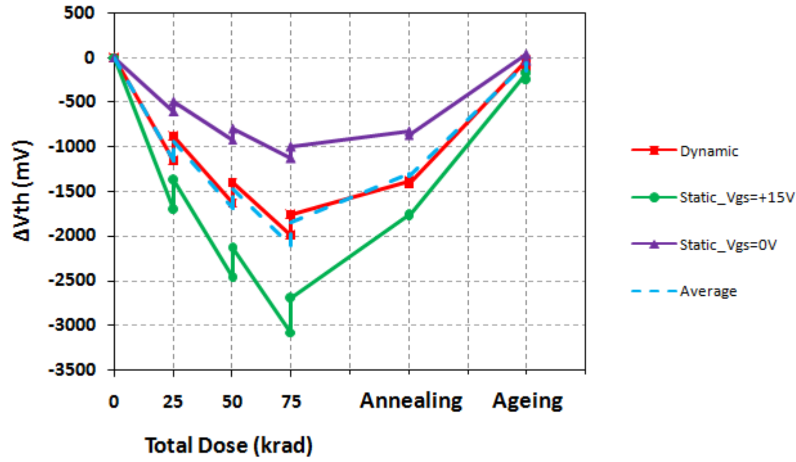

Figure 3.4: Irradiation [rad(Si)], Annealing and Ageing (ΔV_{th}[mV]@ $I_d = 1mA$) for dynamic test with measurement after oscilloscope. (configuration Fig. 3.1a)

- ΔV_{th}[mV] @ $I_d = 1mA$ (configuration Fig. 3.1b)

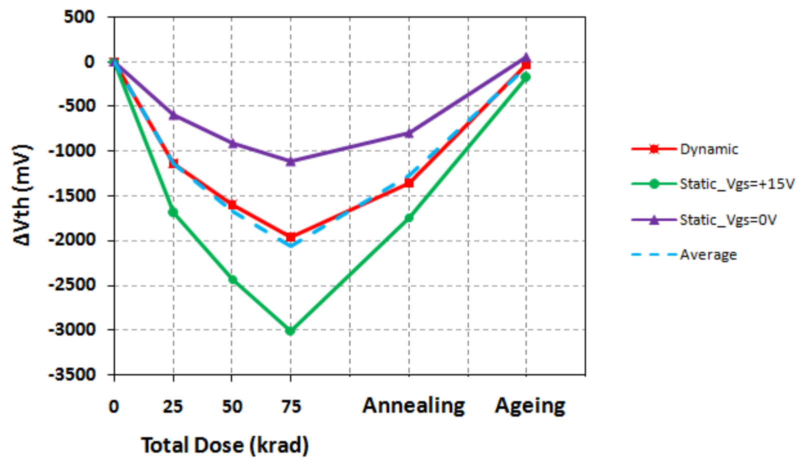

Figure 3.5: Irradiation [rad(Si)], Annealing and Ageing (ΔV_{th}[mV]@ $I_d = 1mA$) for dynamic test. (configuration Fig. 3.1b)

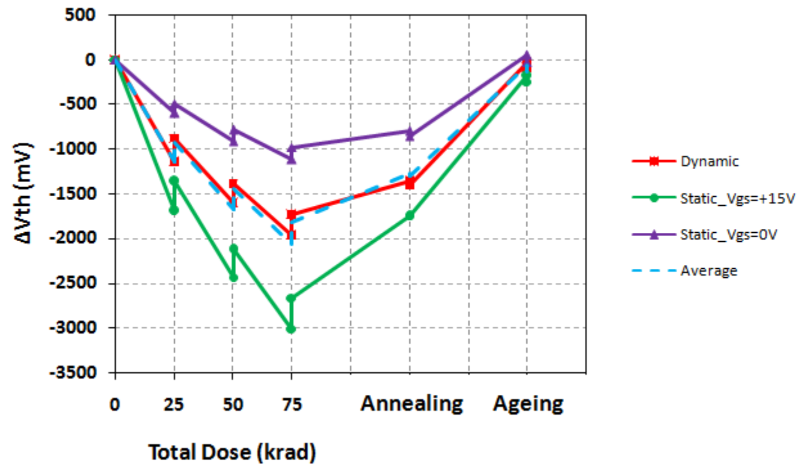

Figure 3.6: Irradiation [rad(Si)], Annealing and Ageing (ΔV_{th}[mV]@ $I_d = 1mA$) for dynamic test with measurement after oscilloscope. (configuration Fig. 3.1a)

3.5.2 Gate Leakage Current

- I_{GSS}[nA] @ $V_{GS} = -20V$ (configuration Fig. 3.1c)

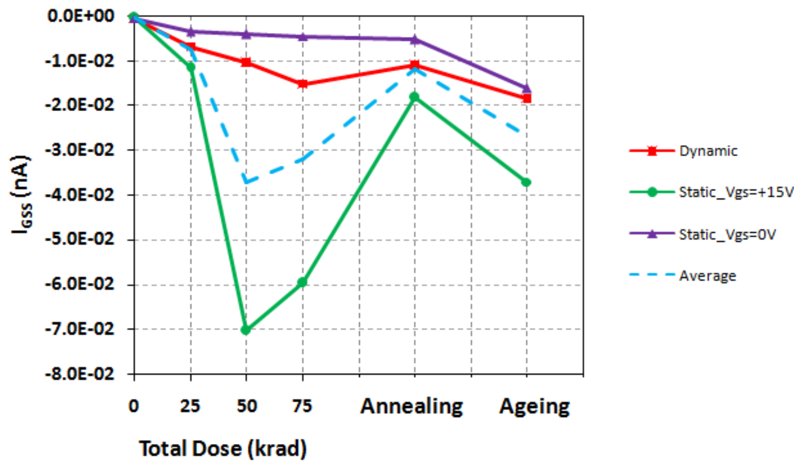

Figure 3.7: Irradiation [rad(Si)], Annealing and Ageing (I_{GSS}[nA] @ $V_{GS} = -20V$) for dynamic test. (configuration Fig. 3.1c)

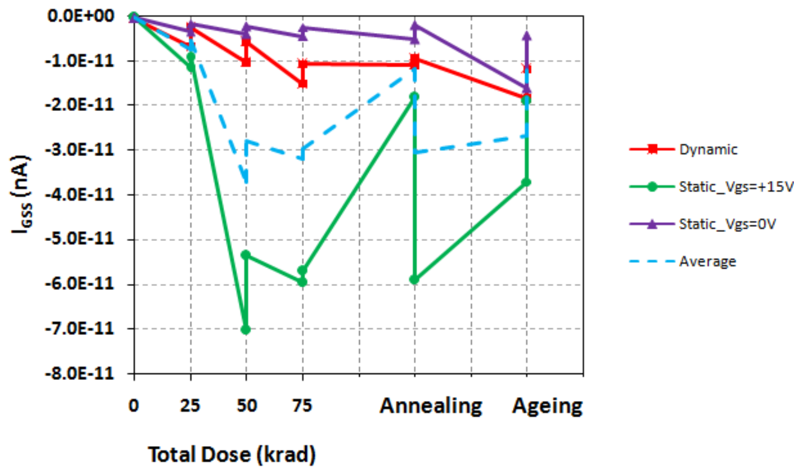

Figure 3.8: Irradiation [rad(Si)], Annealing and Ageing (I_{GSS}[nA] @ $V_{GS} = -20V$) for dynamic test with measurement after oscilloscope. (configuration Fig. 3.1c)

- I_{GSS}[nA] @ $V_{GS} = 20V$ (configuration Fig. 3.1c)

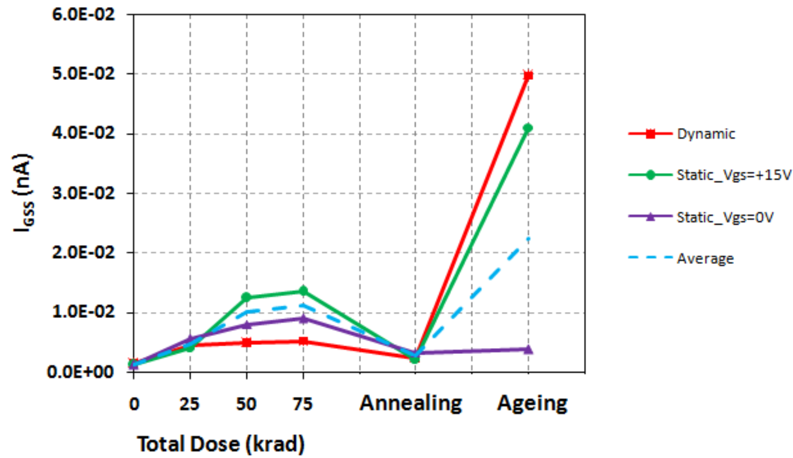

Figure 3.9: Irradiation [rad(Si)], Annealing and Ageing (I_{GSS}[nA] @ $V_{GS} = 20V$) for dynamic test. (configuration Fig. 3.1c)

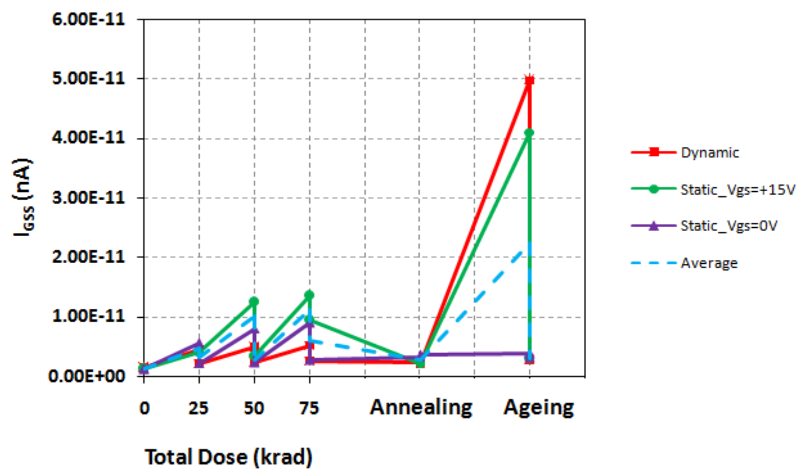

Figure 3.10: Irradiation [rad(Si)], Annealing and Ageing (I_{GSS}[nA] @ $V_{GS} = 20V$) for dynamic test with measurement after oscilloscope. (configuration Fig. 3.1c)

3.5.3 Drain Leakage Current

- $I_{DSS}[\mu A]$ @ $V_{DS} = 150V$ (configuration Fig. 3.1d)

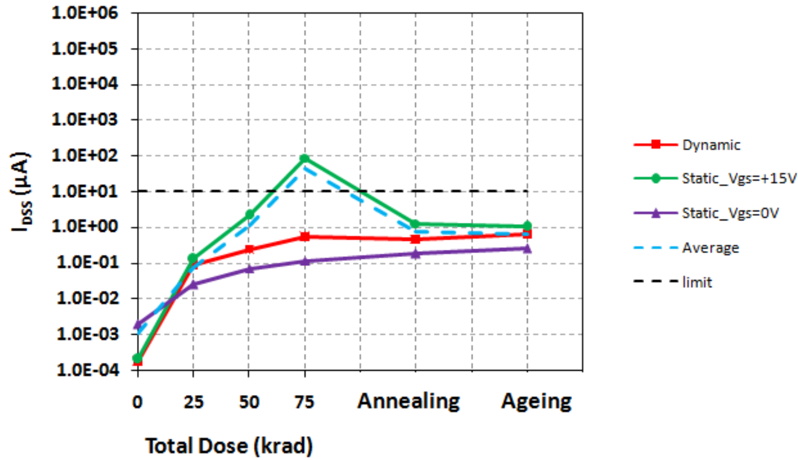

Figure 3.11: Irradiation [rad(Si)], Annealing and Ageing (I_{DSS}[mA] @ $V_{DS} = 48V$) for dynamic test. (configuration Fig. 3.1d)

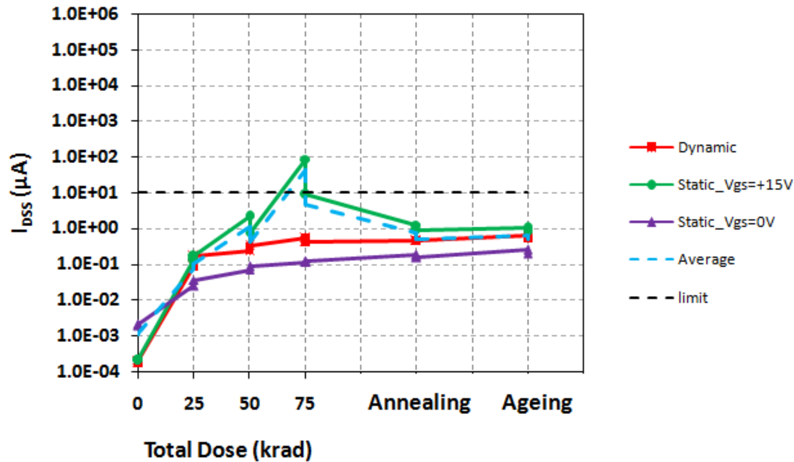

Figure 3.12: Irradiation [rad(Si)], Annealing and Ageing (I_{DSS}[mA] @ $V_{DS} = 48V$) for dynamic test with measurement after oscilloscope. (configuration Fig. 3.1d)

- $I_D - V_{GS}$ Characteristics

Static Bias Condition $V_{GS} = 0V$

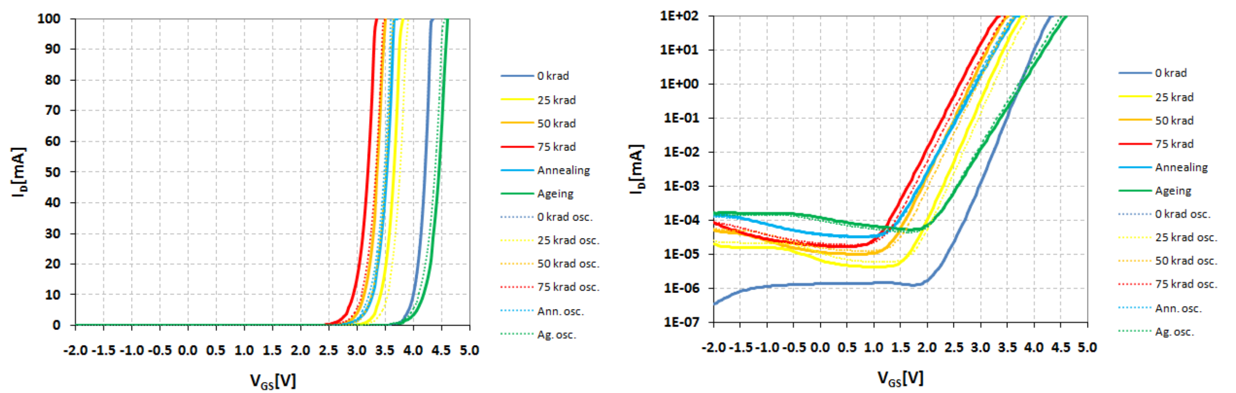

Figure 3.13: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1a): at the left linear scale and at the right semilog scale.

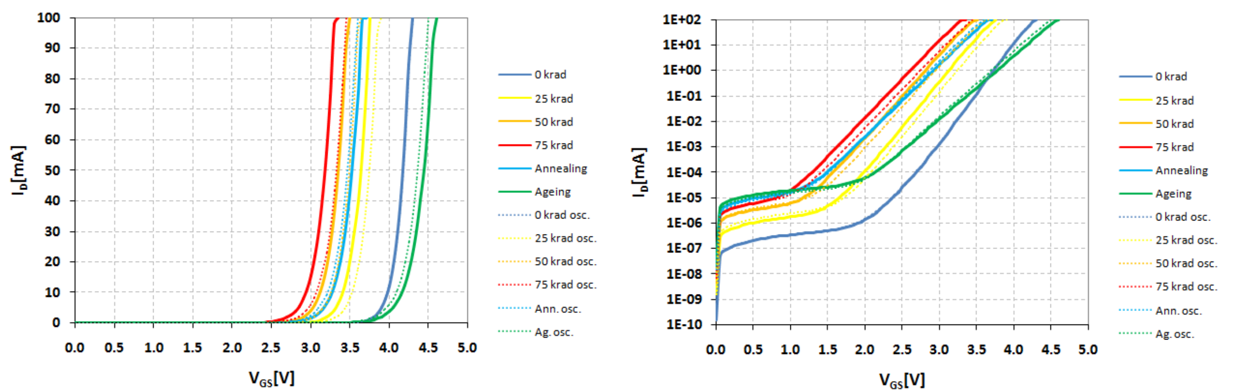

Figure 3.14: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1b): at the left linear scale and at the right semilog scale.

Static Bias Condition $V_{GS} = +15V$

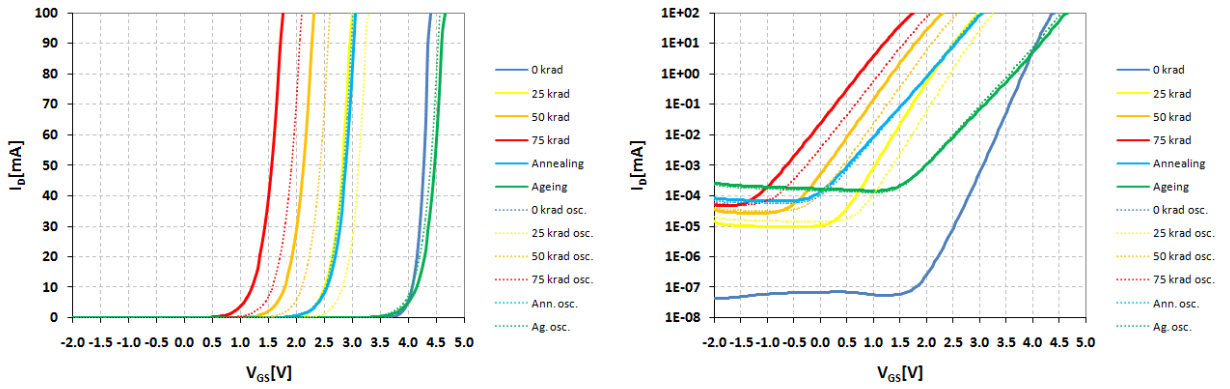

Figure 3.15: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1a): at the left linear scale and at the right semilog scale.

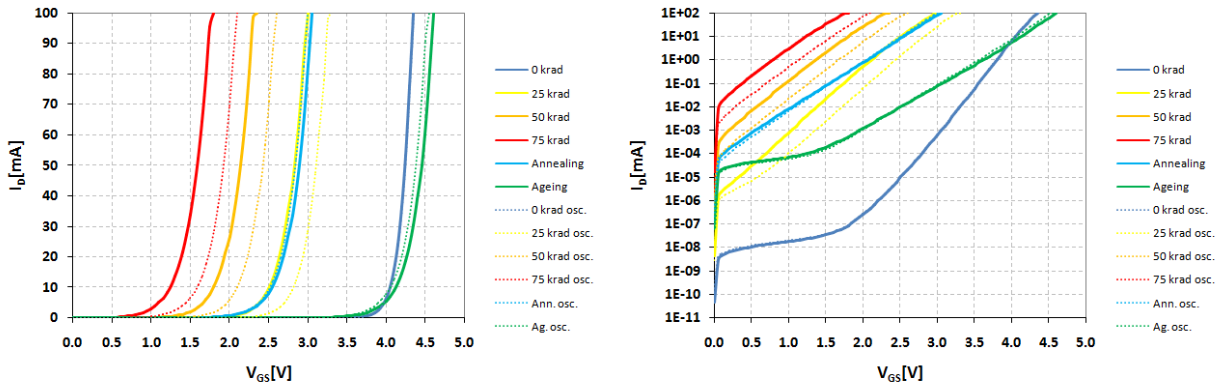

Figure 3.16: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1b): at the left linear scale and at the right semilog scale.

Dynamic Bias Condition

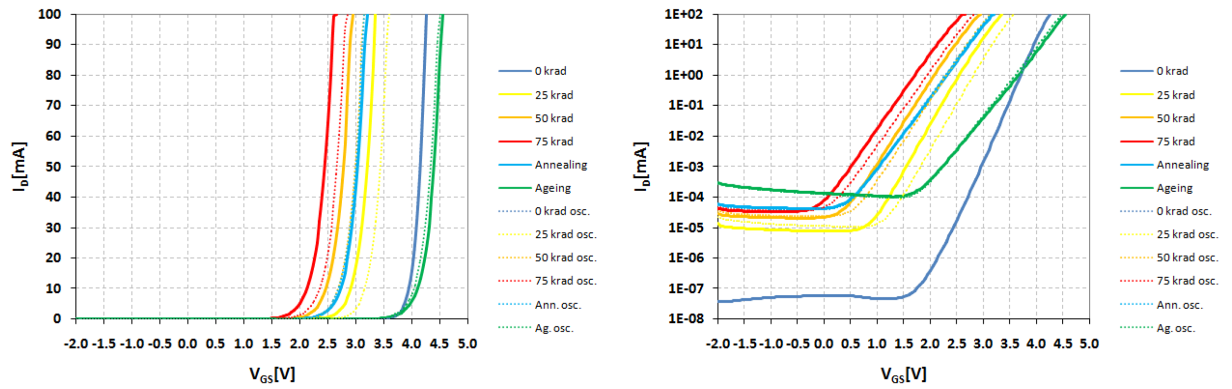

Figure 3.17: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1a): at the left linear scale and at the right semilog scale.

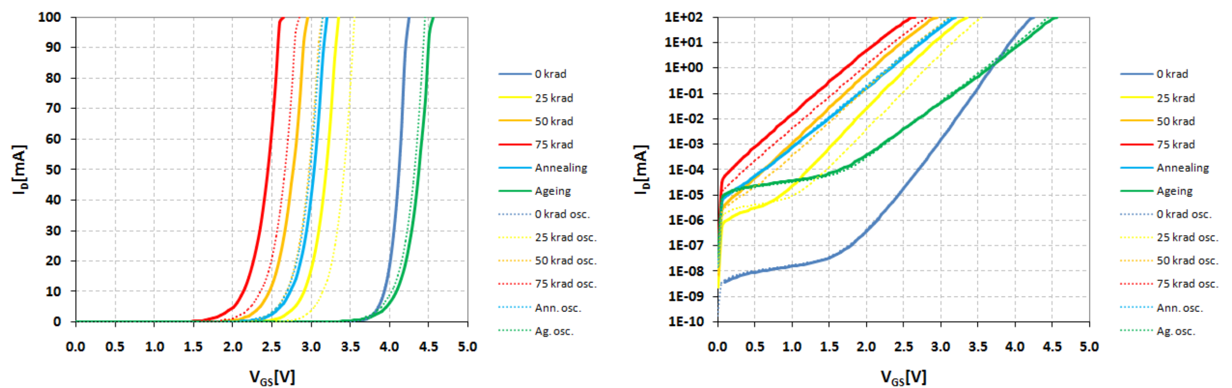

Figure 3.18: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1b): at the left linear scale and at the right semilog scale.

Comparison

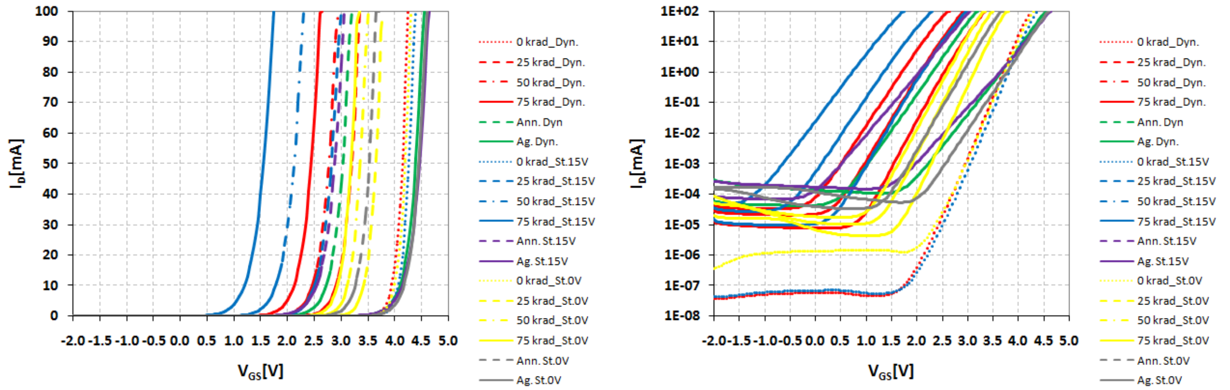

Figure 3.19: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1a): at the left linear scale and at the right semilog scale.

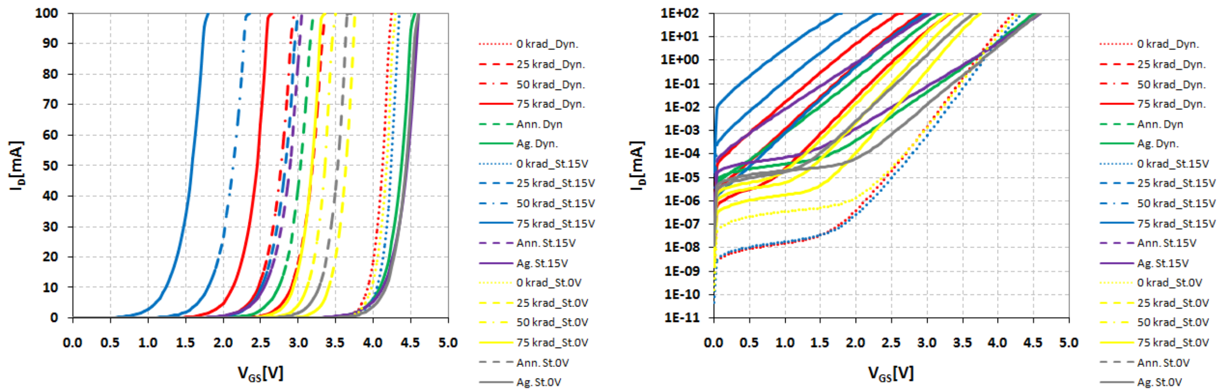

Figure 3.20: $I_D - V_{GS}$ Characteristics (Configuration Fig. 3.1b): at the left linear scale and at the right semilog scale.

3.6 Waveforms

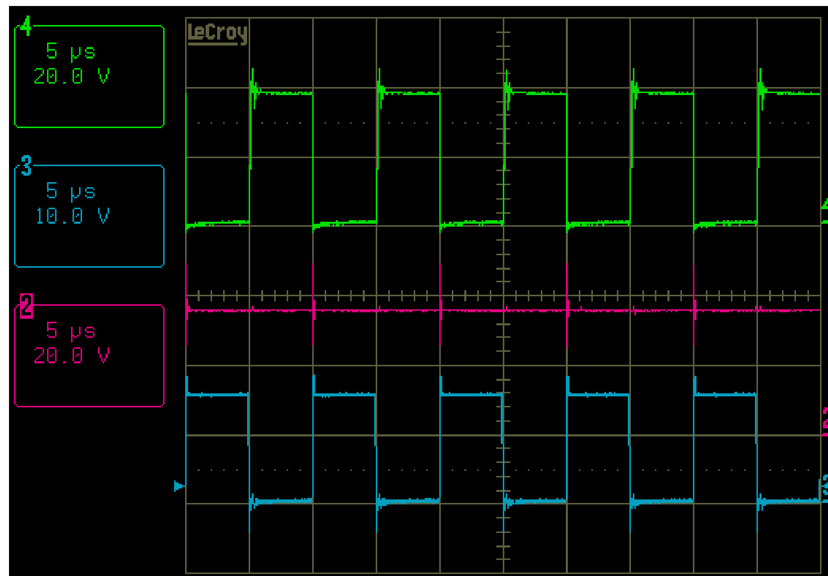

Figure 3.21: Wafe forms: Drain(green), Gate(blue), Output Voltage(violet)

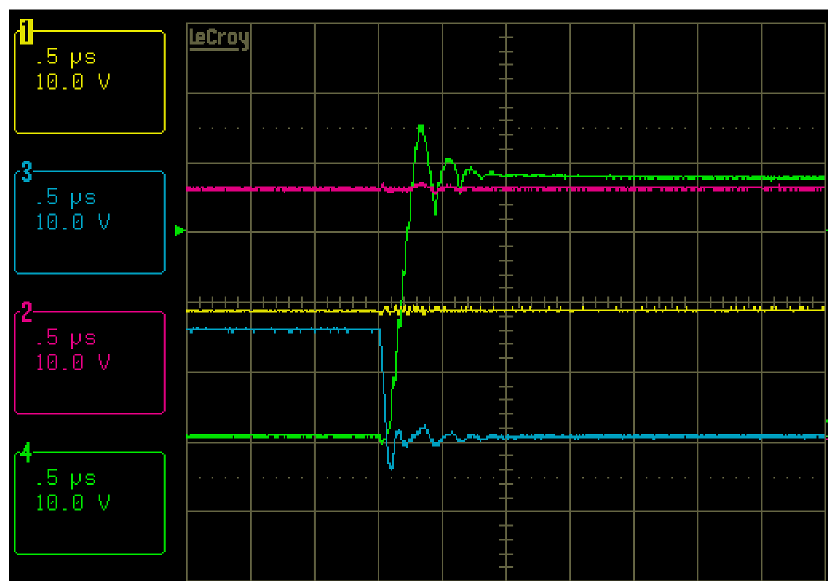

Figure 3.22: Waveforms: Drain(green), Gate(blue), Input Voltage(yellow), Output Voltage(violet)

The picture 3.22 is an extension of the figure 3.21

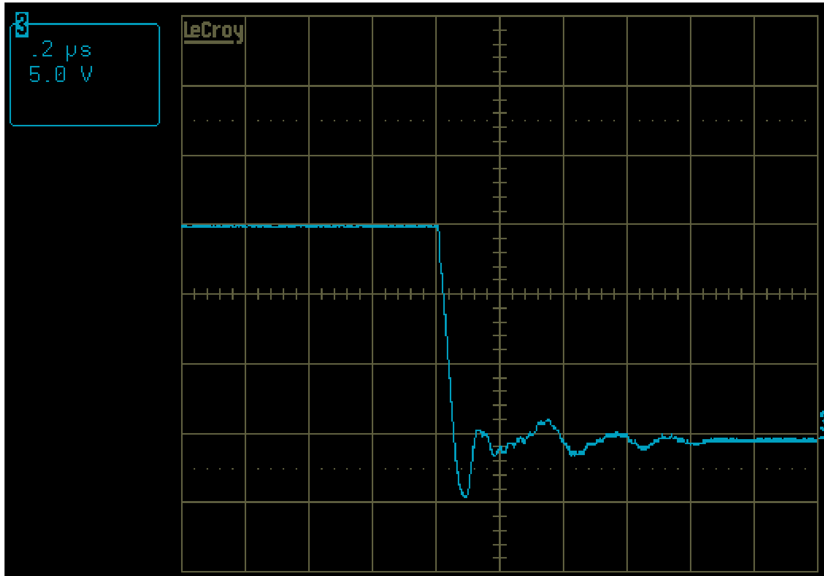

Figure 3.23: Waveforms: switch off gate

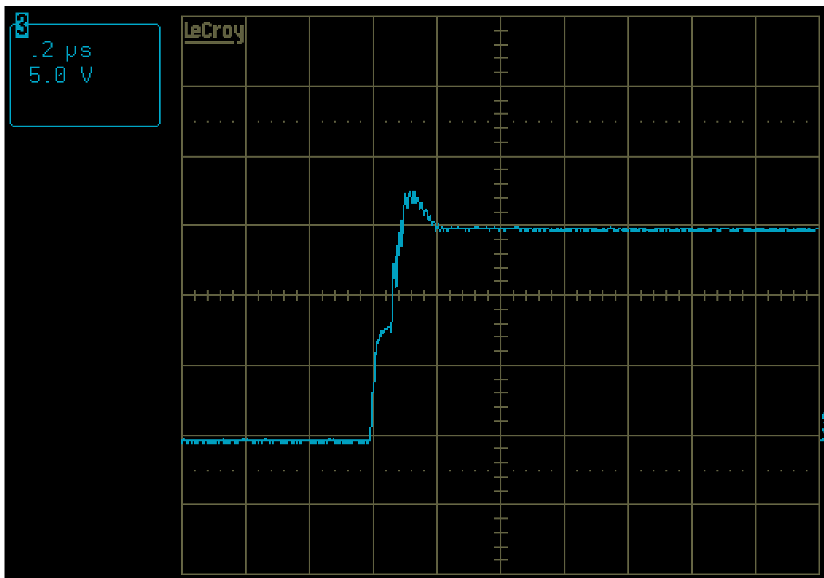

Figure 3.24: Waveforms: switch on gate

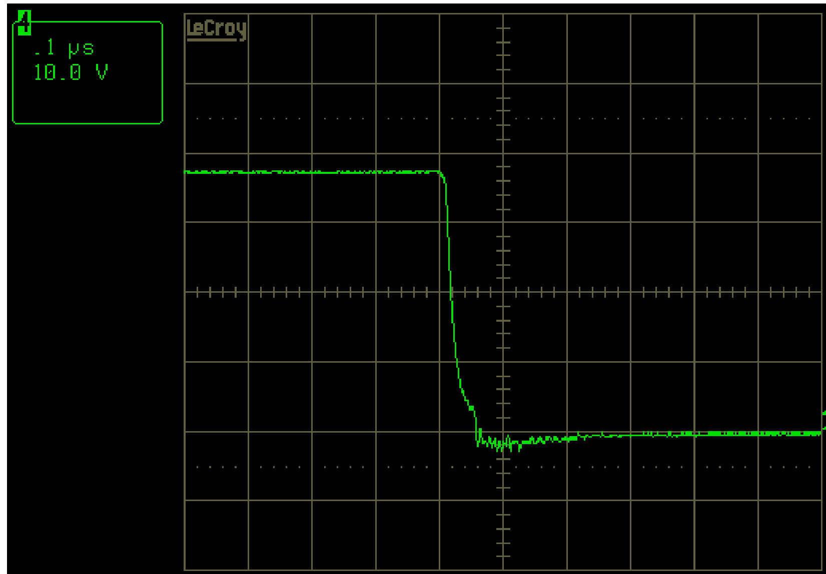

Figure 3.25: Waveforms: switch off drain

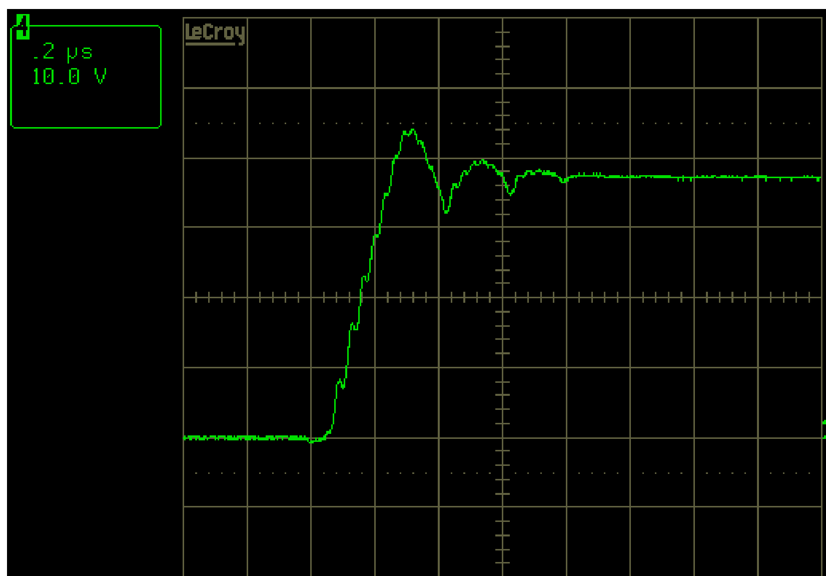

Figure 3.26: Waveforms: switch on drain

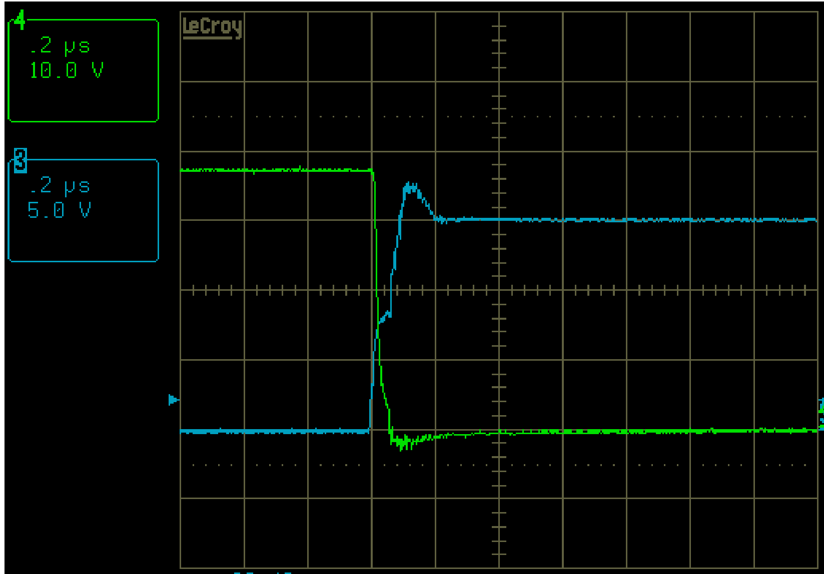

Figure 3.27: Waveforms: switch off drain(green) and switch on gate(blue)

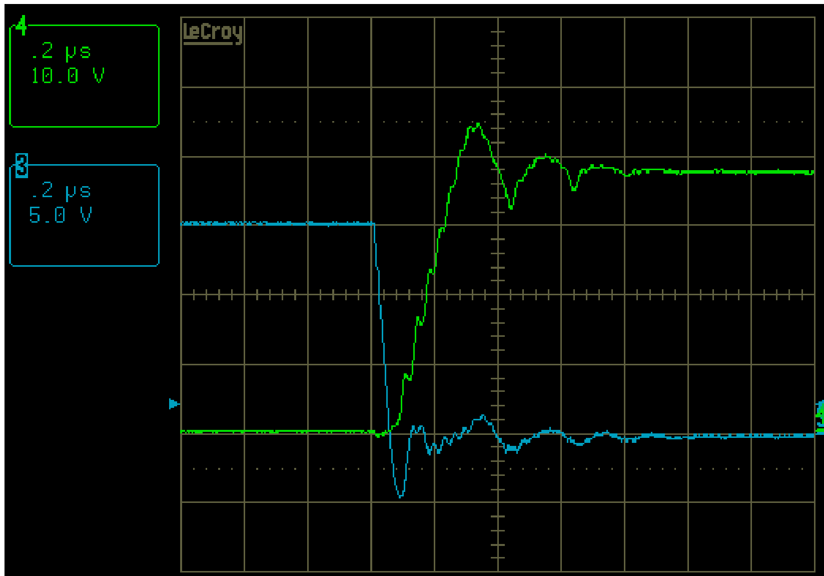

Figure 3.28: Waveforms: switch on drain(green) and switch off gate(blue)

3.7 Discussion

In the previous section it is possible to observe all the degradation of the considered electrical parameters.

From Figure 3.3 to Figure 3.6 it is possible to see the threshold shift (ΔV_{th}) about the two different configurations(configuration in Fig. 3.1a is to see better the sub-threshold current and configuration in Fig. 3.1b the one that STMicroelectronics uses for this type of the test). The worst-case is with the static bias $V_{GS} = +15V$ so the degradation with static bias $V_{GS} = 0V$ is smaller then with $V_{GS} = +15V$. It is important to note that the degradation of the power MOSFET with dynamic bias is approximately equal to the average between the degradation of the power MOSFET with static bias $V_{GS} = +15V$ and the power MOSFET with static bias $V_{GS} = 0V$:

$$Dynamic \cong \frac{static@V_{GS} = +15V + static@V_{GS} = 0V}{2} \tag{3.11}$$

As shown in the section of the boost converter, the whole circuit works with a frequency $f_s = 100kHz$, a period $T_s = 10\mu s$ and with a duty-cycle D=50% so during the irradiation in dynamic condition the power MOSFET was on for $5\mu s$ and stayed off for $5\mu s$. Observing the formula written above and the work conditions of the boost converter it is possible to assert that a rapidly switching bias does not impact degradation and does not alter the dynamics of charge trapping also because during the irradiation the power MOSFET reached only 30°C some degree more than the temperature of the device in static bias (room temperature 25°C), so the temperature has no an important effects on the degradation. The recovery after annealing follows the same rule.

From Figure 3.13 to Figure 3.18 it is possible to note the shift of the $I_D - V_{GS}$ characteristics during the irradiation caused by the generation of charge trapping and there is no significant change in the sub-threshold slope of the curves but after annealing and ageing, beyond the recovery of the shift, these slopes have an important change so during the irradiation there is no the generation of interface traps, but after long time these interface traps

were created.

The leakage gate current remains very small even after the exposure. Instead for the leakage drain current only the values for the device in static bias with $V_{GS} = +15V$ go beyond the limit that the manufacturer imposed after 60 krad.

Regarding the boost converter waveforms, after every step of measurement, in all three power MOSFETs, there were no noticeable changes in each waveform (gate, drain, output). In spite of the degradation, these tested devices continue to work well in the boost converter.

Chapter 4

Static Bias Test on Bipolar Transistors

This chapter shows the test results in static conditions, performed at ESA-ESTEC, on NPN bipolar transistor .

4.1 Co60 TID Tests of 100 krad, 600V, 0.5A NPN Bipolar Transistor

4.1.1 Introduction

A total dose characterization test of STMicroelectronics 600V, 0.5A NPN high voltage bipolar transistor prototype was performed at the ESTEC Co-60 Facility. The transistors have been exposed to a total accumulated dose of 100 krad(Si), using two different constant low dose rate of 360 rad(Si)/h (6 rad(Si)/min) and 36 rad(Si)/h (0.6 rad(Si)/min). The purpose of this test is to evaluate the TID tolerance of the bipolar transistor and to see if there is Enhanced Low Dose Rate Effects (ELDRS). The tests have been performed in accordance with the ESCC Basic Specification No. 22900.

4.1.2 Experimental Conditions

Tested Devices

Part type	Prototype
Manufacturer	STMicroelectronics
Function	600V, 0.5A npn bipolar transistor
Family	Transistor
Group	-
Package	TO39

Table 4.1: Information npn bipolar transistor

Irradiation Test Conditions

The radiation test steps, for the two different dose rate, are reported in the following tables (table 4.2, table 4.3):

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(Si)	krad(Si)	rad(Si)/min	hours	°C
0	2.535	0			
1	6.481	2.535	6	-	Room
2	8.074	9.016	6	-	Room
3	9.579	17.090	6	-	Room
4	6.861	26.669	6	-	Room
5	25.861	33.530	6	-	Room
6	15.593	59.391	6	-	Room
7	17.914	74.984	6	-	Room
8	23.986	92.898	6	-	Room
9	-	116.884	6		
10	-	116.884		24	Room
11	-	116.884		168	100

Table 4.2: The Radiation test steps with 360 rad/h

Run	Irradiation Steps	Cum. Rad.	Dose rate	Annealing steps	Temperature
	krad(Si)	krad(Si)	rad(Si)/min	hours	°C
0	1.571	0			
1	2.504	1.571	0.6	-	Room
2	6.048	4.075	0.6	-	Room
3	5.877	10.123	0.6	-	Room
4	8.254	16.000	0.6	-	Room
5	4.118	24.254	0.6	-	Room
6	24.200	28.372	0.6	-	Room
7	-	52.572	0.6		
8	-	52.572		24	Room
9	-	52.572		168	100

Table 4.3: The Radiation test steps with 36 rad/h

At the completion of each irradiation step, intermediate electrical measurements have been carried out according to the electrical measurement parameters. Following the ESCC 22900 recommendations, the time interval from the completion of the exposure to the start of the measurements have been of 1 hour max and the next exposure has started after a maximum of 2 hours.

Bias Condition During Irradiation

In total 18 samples of the NPN high voltage bipolar transistor were used for testing. After the exposure, the samples have been annealed for 24 hours and subsequently aged at 100 °C for 168 hours maintaining the same biasing conditions as during the exposure. The following table summarizes the bias conditions of the components:

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{CBO}	Collector cut-off current(I_E =0)	V_{CB}=950 V		1	µA
I_{CES}	Collector-emitter cut-off current (I_B =0)	V_{CE}=950 V		1	µA
I_{EBO}	Emitter cut-off current(I_C =0)	V_{EB}=5 V		1	µA
$V_{(BR)CBO}$	Collector-base breakdown voltage (I_E =0)	I_C=1 µA	950		V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage(I_B =0)	I_C=500 µA	600		V
$V_{(BR)EBO}$	Emitter-base breakdown voltage (I_C =0)	I_E=1 mA	7		V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C=10 mA, I_B=2 mA I_C=50 mA, I_B=10 mA		0.4 0.5	V V
$V_{BE(sat)}$	Base-emitter saturation voltage	I_C=50 mA, I_B=10 mA		1.0	V
h_{FE}	DC current gain	I_C=100 µA, V_{CE}=5 V I_C=1 mA, V_{CE}=5 V I_C=10 mA, V_{CE}=5 V I_C=50 mA, V_{CE}=5 V	20 23.3 18 5		

Table 4.5: Measured Parameters, Min-Max Limits and Test conditions (Ta=25°C)

DUT S/N	Usage
1-4	Unbiased during Co60 irradiation with 360rad/h(Si), anneal and ageing
5-8	Biased during Co60 irradiation with 360rad/h(Si), anneal and ageing
9-12	Unbiased during Co60 irradiation with 36rad/h(Si), anneal and ageing
13-16	Biased during Co60 irradiation with 36rad/h(Si), anneal and ageing
17-18	Reference device (Not irradiated) - Electrically tested before and after each intermediate measurement run.

Table 4.4: Sample usage

4.1.3 Measurements Setup

No in-situ measurements were performed during irradiation. In table 4.5 there are the measured electrical parameter.

The electrical measurements have been performed at room temperature using a M3000 universal test system with a TA07B transistor test adapter set in a Faraday cage at the ESTEC facilities. SCADUS software has been used to control and automatize the electrical measurements with the instru-

mentation. Furthermore an Agilent B1505A *Power Device Analyzer/Curve Tracer* and an Agilent B1265A *Ultra high Current Expander/Fixture* have been used to evaluate the breakdown voltage $V_{(BR)CBO}$ and $V_{(BR)CBO}$.

The figure 4.1 shows an example of the two different electrical circuit about the biased and unbiased condition (in the left side biased an in the right side unbiased):

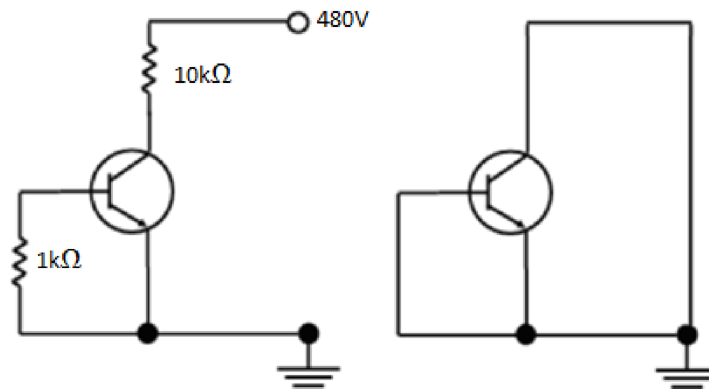

Figure 4.1: Configuration for the electrical measurement.

4.1.4 Test Results

In this section the results of the electrical measurements are shown with plots. These results include all the electrical parameters in table 4.5. In the charts there are the average curves for each conditions to see if there is ELDRS effect.

- Collector cut-off current ($I_E = 0$), I_{CBO}[nA]

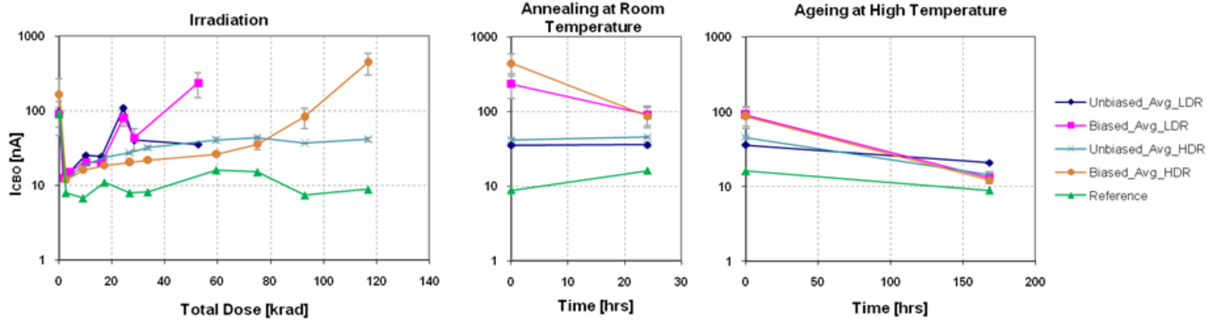

Figure 4.2: Irradiation [rad (Si)], annealing and ageing (Collector cut-off current, I_{CBO}[nA]). Average values and standard deviation (unbiased and biased samples)

- Collector-Emitter cut-off current ($I_B = 0$), I_{CES}[nA]

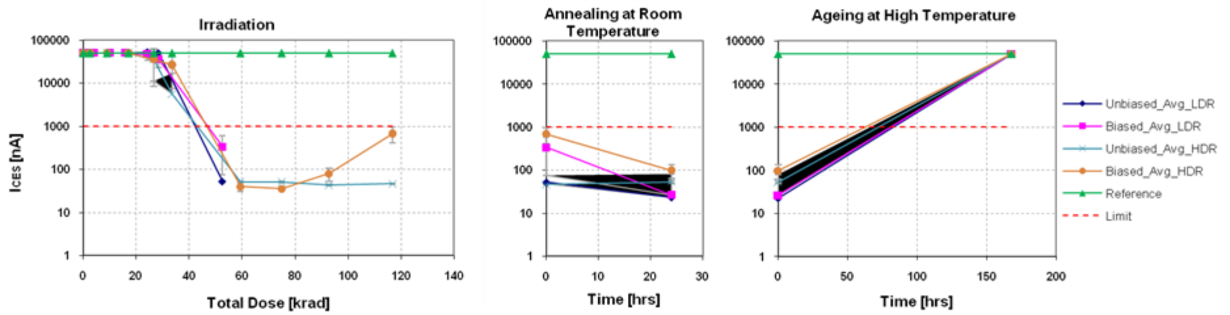

Figure 4.3: Irradiation [rad (Si)], annealing and ageing (Collector-Emitter cut-off current, I_{CES}[nA]). Average values and standard deviation (unbiased and biased samples)

- Emitter cut-off current ($I_B = 0$), I_{EBO}[nA]

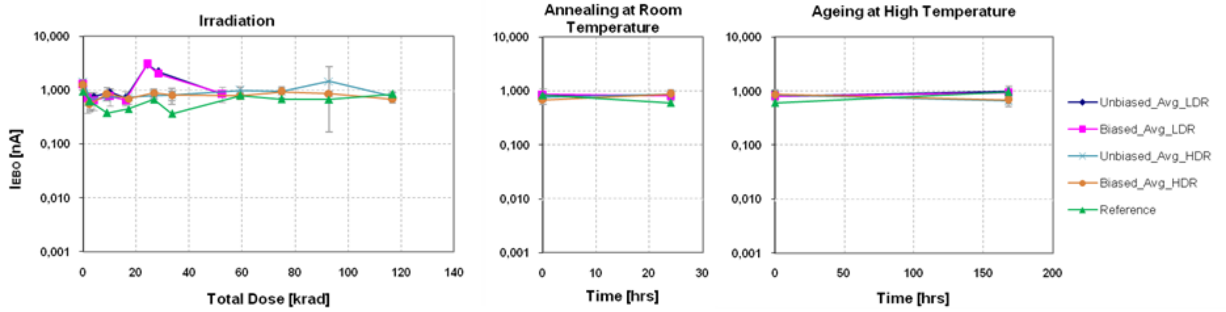

Figure 4.4: Irradiation [rad (Si)], annealing and ageing (Emitter cut-off current, I_{EBO}[nA]). Average values and standard deviation (unbiased and biased samples)

- Collector-Base breakdown voltage ($I_E = 0$), $V_{(BR)CBO}$[V]

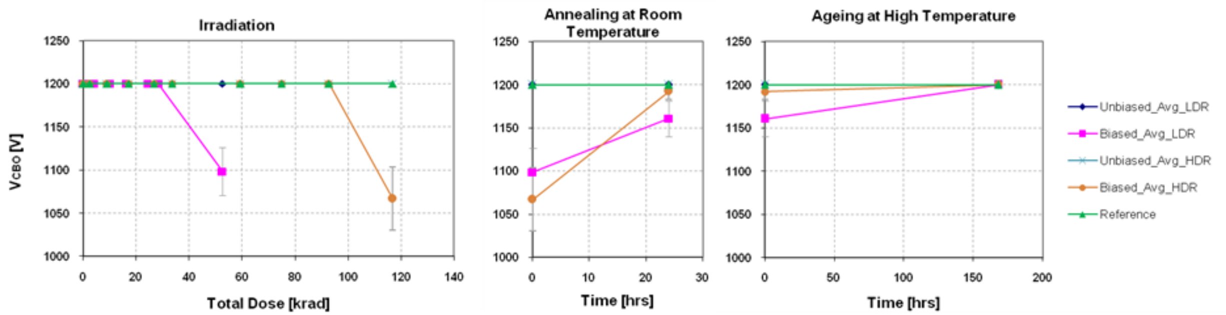

Figure 4.5: Irradiation [rad (Si)], annealing and ageing (Collector-Base breakdown voltage, $V_{(BR)CBO}$[V]). Average values and standard deviation (unbiased and biased samples)

- Collector-Emitter breakdown voltage ($I_B = 0$), $V_{(BR)CEO}$[V]

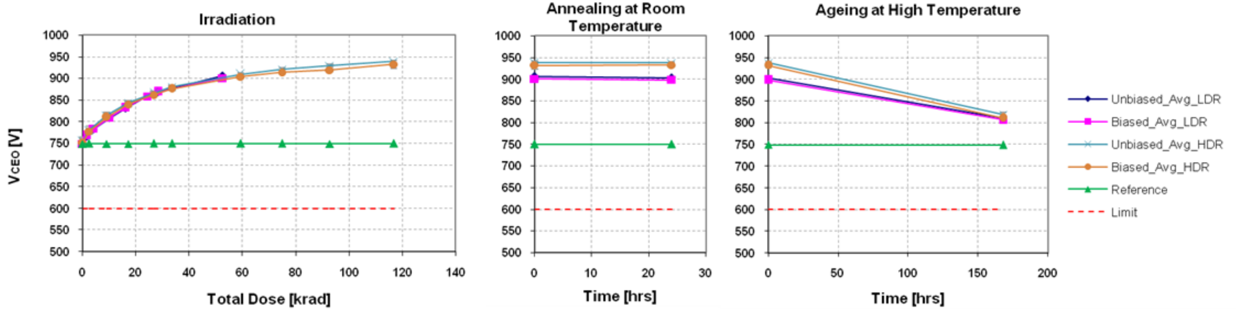

Figure 4.6: Irradiation [rad (Si)], annealing and ageing (Collector-Emitter breakdown voltage, $V_{(BR)CEO}$[V]). Average values and standard deviation (unbiased and biased samples)

- Emitter-Base breakdown voltage ($I_C = 0$), $V_{(BR)EBO}$[mV]

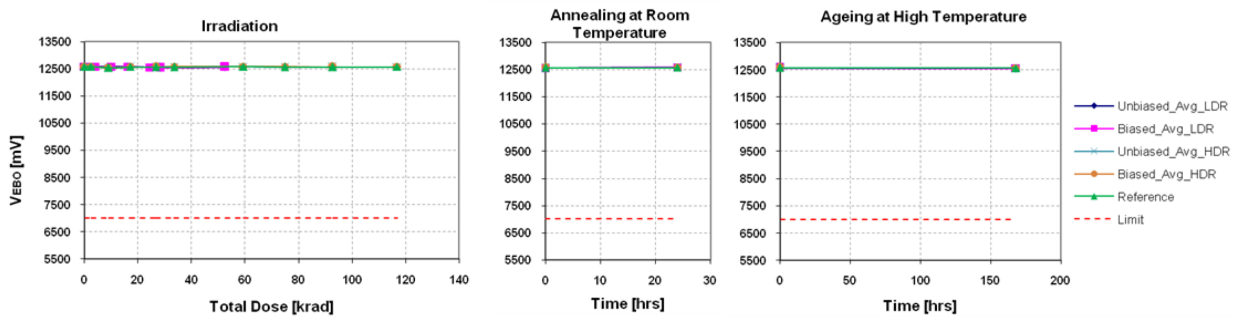

Figure 4.7: Irradiation [rad (Si)], annealing and ageing (Emitter-Base breakdown voltage, $V_{(BR)EBO}$[mV]). Average values and standard deviation (unbiased and biased samples)

- Collector-Emitter saturation voltage, $V_{CE(SAT)}$[mV] ($I_C = 10mA$, $I_B = 2mA$)

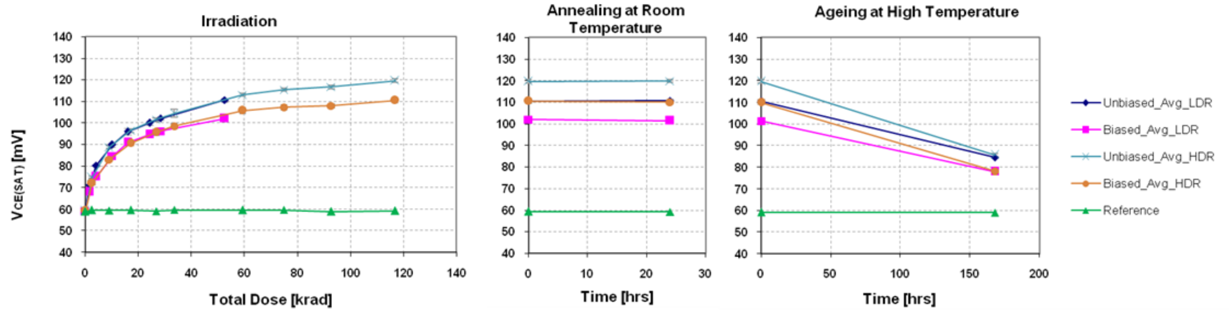

Figure 4.8: Irradiation [rad (Si)], annealing and ageing (Collector-Emitter saturation voltage, $V_{CE(SAT)}$[mV] with $I_C = 10mA$, $I_B = 2mA$). Average values and standard deviation (unbiased and biased samples)

- Collector-Emitter saturation voltage, $V_{CE(SAT)}$[mV] ($I_C = 50mA$, $I_B = 10mA$)

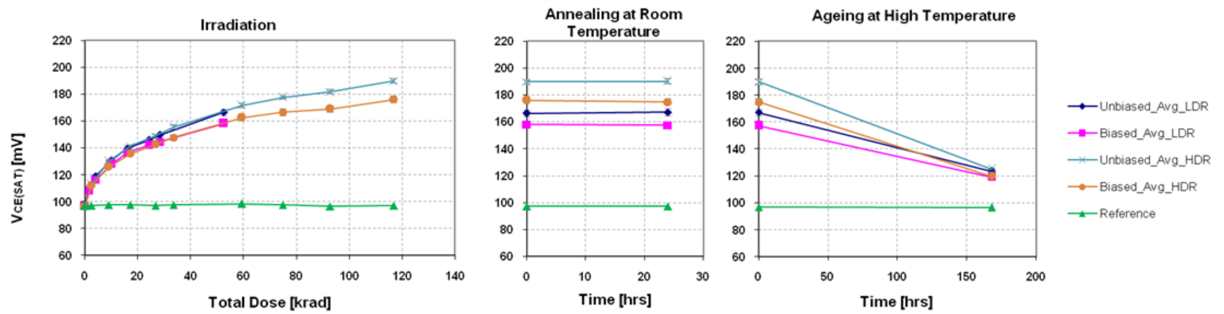

Figure 4.9: Irradiation [rad (Si)], annealing and ageing (Collector-Emitter saturation voltage, $V_{CE(SAT)}$[mV] with $I_C = 50mA$, $I_B = 10mA$). Average values and standard deviation (unbiased and biased samples)

- Base-Emitter saturation voltage, $V_{BE(SAT)}$[mV] ($I_C = 50mA$, $I_B = 10mA$)

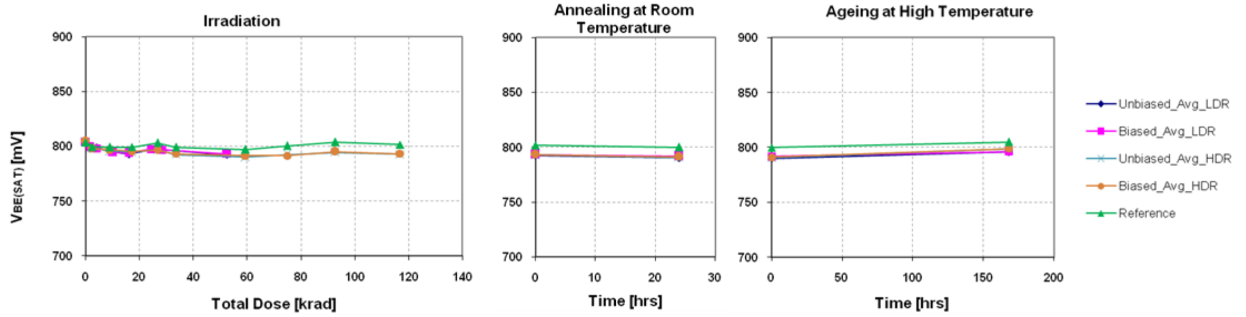

Figure 4.10: Irradiation [rad (Si)], annealing and ageing (Base-Emitter saturation voltage, $V_{BE(SAT)}$[mV] with $I_C = 50mA$, $I_B = 10mA$). Average values and standard deviation (unbiased and biased samples)

- DC Current Gain, $h_{FE}(I_C = 100\mu A, V_{CE} = 5V)$

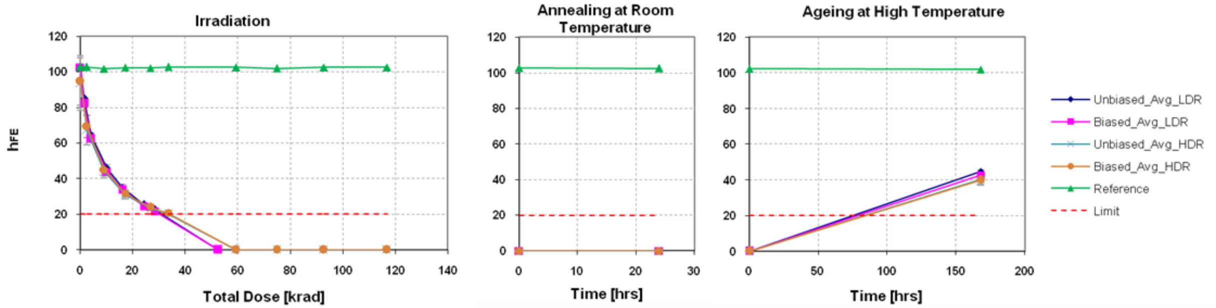

Figure 4.11: Irradiation [rad (Si)], annealing and ageing (DC Current Gain, h_{FE} with $I_C = 100\mu A$, $V_{CE} = 5V$). Average values and standard deviation (unbiased and biased samples)

- DC Current Gain, $h_{FE}(I_C = 1mA, V_{CE} = 5V)$

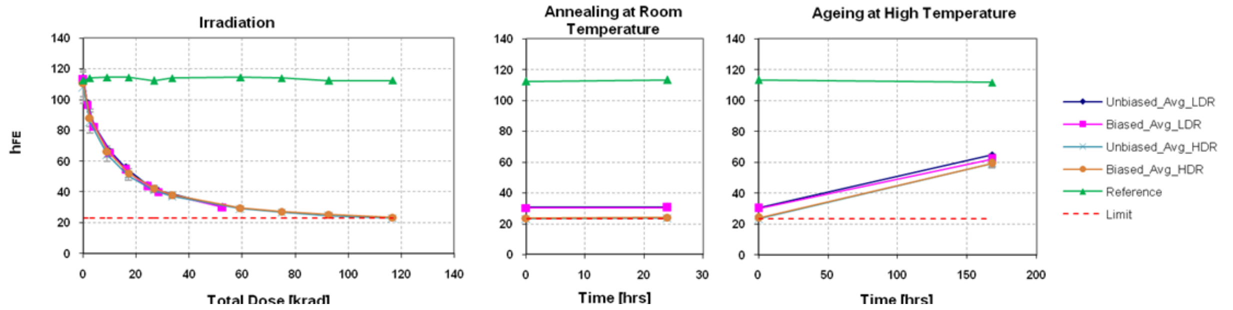

Figure 4.12: Irradiation [rad (Si)], annealing and ageing (DC Current Gain, h_{FE} with $I_C = 1mA$, $V_{CE} = 5V$). Average values and standard deviation (unbiased and biased samples)

- DC Current Gain, $h_{FE}(I_C = 10mA, V_{CE} = 5V)$

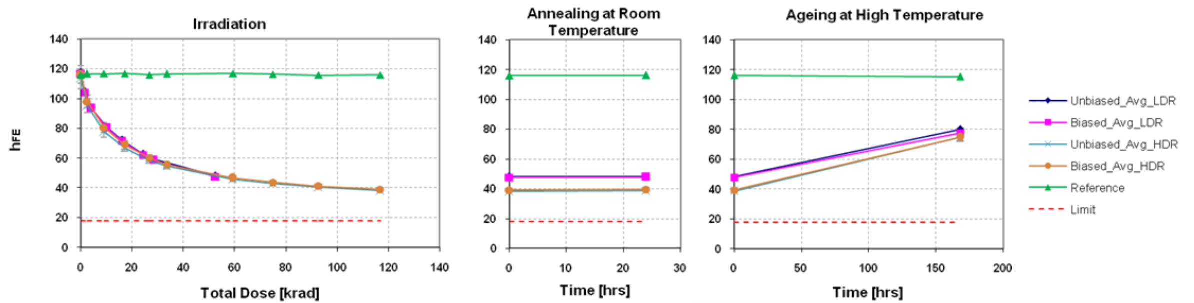

Figure 4.13: Irradiation [rad (Si)], annealing and ageing (DC Current Gain, h_{FE} with $I_C = 10mA$, $V_{CE} = 5V$). Average values and standard deviation (unbiased and biased samples)

- DC Current Gain, $h_{FE}(I_C = 50mA, V_{CE} = 5V)$

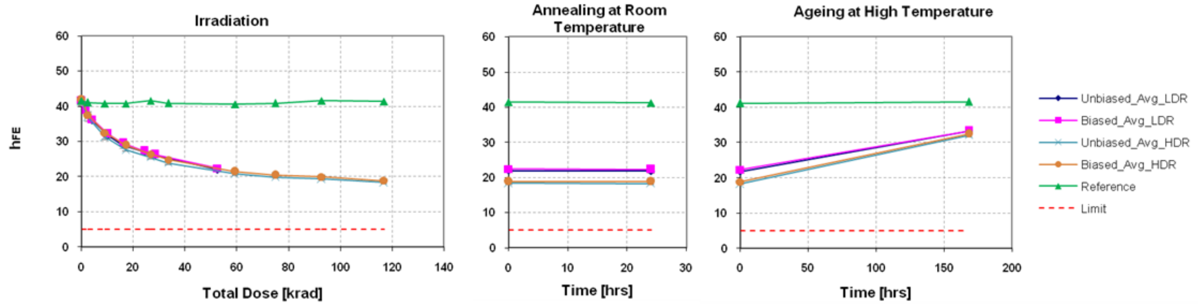

Figure 4.14: Irradiation [rad (Si)], annealing and ageing (DC Current Gain, h_{FE} with $I_C = 50mA$, $V_{CE} = 5V$). Average values and standard deviation (unbiased and biased samples)

4.1.5 Discussion

Based on the electrical results summarized above, it is possible note that after the radiation, for the devices that were irradiated at high dose rate (360 rad/h) till 116.8 krad of total dose, the electrical parameters (biased and unbiased samples) are inside the margins of the manufacturer except for the gain h_{FE} ($I_C = 100\mu A$, $V_{CE} = 5V$) where the devices failed at 33 krad. After annealing at room and high temperature there was a recovery for each electrical parameter. For the devices that were irradiated at low dose rate (36 rad/h) till 52.6 krad of total dose, the electrical parameters (biased and unbiased samples) are inside the margins of the manufacturer except for the gain h_{FE} ($I_C = 100\mu A$, $V_{CE} = 5V$) where the devices failed at 33 krad. After annealing at room and high temperature there was a recovery for each electrical parameter.

It is possible note the ELDRS effect in Collector-Base breakdown voltage, $V_{(BR)CBO}$[V], between biased samples at high dose rate and biased samples at low dose rate close 30 krad. For the other electrical parameters it is not possible note ELDRS effects.

Conclusions

The work of this thesis was focused on the analysis of the Total Ionizing Dose effects on power MOSFETs. In particular the study investigated the degradation of the threshold voltage that is one of the electrical parameters more sensitive to irradiation effects, but also other electrical parameters as drain leakage current and gate leakage current have been taken in consideration.

From the TID tests in static bias condition, we noted that the bias applied on power MOSFETs has an important role in the degradation and especially that the worst-case is not necessarily the bias with the highest value but with an intermediate value. This result is possible to explain with the dynamics of the charge yield and the cross-section in the oxide due to their dependence on the electric field.

Furthermore, we observed that the degradation in static bias condition of P-channel power MOSFETs is worse than that of the N-channel power MOSFETs due to the additive effects of trapped charge in the oxide and interface state.

From the TID tests in dynamic bias conditions on power MOSFETs, we saw that the degradation of the threshold voltage, for the tested device in dynamic condition, is the average of the degradation of the threshold voltage between the two static bias conditions: $V_{GS} = +15V$ and $V_{GS} = 0V$. This result is caused by the dominant contribution of the charge trapping in pre-existing oxide traps. In fact, during the irradiation the power MOSFET reached a temperature of 30°C that it is only 5°C higher than the temperature of the

two power MOSFETs in static condition reached during the irradiation so the temperature do not alter the process of degradation in this case. In the future it is possible to test the devices in dynamic bias conditions in order to allow power MOSFETs to reach higher junction temperature during the irradiation. Hence, we can see the effects in the same time of the annealing that is caused by high temperature in the device and the degradation of the threshold voltage of the power MOSFETs that is caused by irradiation. Moreover, we observed that the degradation of the threshold voltage of these devices has no effects on the boost converter functionality: the waveforms have no degradations.

To conclude we observed in the bipolar transistors there is the ELDRS effect only in the base breakdown voltage ($V_{(BR)CBO}$).

Bibliography

[1] J.-M. Lauenstein, A. Topper, M. Casey, E. Wilcox, A. Phan, H. Kim, and K. LaBel, “Recent radiation test results for power mosfets” in Radiation Effects Data Workshop (REDW), 2013 IEEE, pp. 1–6, July 2013.

[2] T. P. Ma and P. V. Dressendorfer, “Ionizing Radiation Effects in MOS Devices and Circuits” Eds. New York: Wiley, 1989.

[3] T. R. Oldham, “Basic Mechanisms of TID and DDD Response in MOS and Bipolar Microelectronics”, NSREC 2011 Short Course.

[4] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, “Radiation Effects in MOS Oxides” IEEE Trans. Nucl. Sci., Vol.55, No.4, pp 1833-1853, Aug. 2008

[5] http://www.mag-inc.com/, "Magnetics New Powder Core Catalog", 2011. [Online]. Available: http://www.mag-inc.com/design technical-documents/request-magnetics-new-powder-core-catalog. [Accessed: 10-Now-2015].

[6] ESCC Basic Specification No. 22900: Total Dose Steady State Irradiation Test Method.

[7] A. Costantino, “Basic information about the Estec Co-60 facility” https://escies.org/webdocument/, December 2013.

[8] A. Paccagnella, S. Gerardin, “Basics of Radiation Effects” RADECS 2009 Short Course.

[9] R.L. Pease, D.G. Platteter, G.W. Dunham, J.E. Seiler, H.J. Barnaby, R.D. Schrimpf, M.R. Shaneyfelt, M.C. Maher and R.N. Nowlin, “Characterization of enhanced low dose rate sensitivity (ELDRS) effects using Gated Lateral PNP transistor structures”, IEEE Transactions on Nuclear Science, Vol. 51(6), pp. 3773-3780, 2004

[10] J. Boch, F. Saigne, R. D. Schrimpf, J. -. Vaille, L. Dusseau and E. Lorfevre, “Physical model for the low-dose-rate effect in bipolar devices”, IEEE Trans.Nucl.Sci., vol. 53, pp. 3655-3660, 2006.

[11] R.D. Schrimpf, “Physics and Hardness Assurance for Bipolar Technologies”, 2001 IEEE NSREC Short Course Notes

[12] “Basic calculation of a Boost Converter’s Power Stage”, Application Note, Texas Instruments (SLVA372C)

[13] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, K. L. Hughes and F. W. Sexton, “FIELD DEPENDENCE OF INTERFACE-TRAP BUILDUP IN POLYSILICON AND METAL GATE MOS DEVICES”, IEEE Transaction on Nuclear Science, Vol. 37, NO. 6, Dec. 1990.

[14] T. R. Oldham and F. B. McLean, “Total Ionizing Dose Effects in MOS Oxides and Devices” IEEE Transaction on Nuclear Science, Vol. 50, NO. 3, June 2003.

[15] D. V. Boychenko, L. N. Kessarinkiy, A. Y. Nikiforov, “Investigation of Low dose rate effects in DC/DC Converters”, Proc. RADECS 2013 DW-15 1/3.

[16] S. Dhombres, A.Michez, J.Boch, F. Saigné, Senior Member, IEEE, S. Beauvivre, D. Kraehenbuehl, J.-R. Vaillé, P. C. Adell, E. Lorfèvre, R. Ecoffet and F. Roig, “Study of a Thermal Annealing Approach for Very High Total Dose Environments” IEEE Transaction on Nuclear Science, Vol. 61, NO. 6, pp. 2923-2929, Dec. 2014.

[17] D. Bisello, A. Candelori, A. Kaminski, A. Litovchenko, E. Noah and L. Stefanutti, "X-ray radiation source for total dose radiation studies", Rad. Phys. Chem., vol. 71, pp. 713-715, October-November 2004.

[18] M. Wind, J. V. Bagalkote, P. Beck, M. Latocha, M. Poizat, "TID and SEGR Radiation Characterisation of European COTS Power MOSFETS with respect to Space Application Electronics" IEEE.

[19] D. M. Fleetwood, "Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices", IEEE Transaction on Nuclear Science, Vol. 60, NO. 3, pp. 1706-1730, June 2013.