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TESI DI LAUREA

ELECTRICAL CHARACTERIZATION OF THIN FILM PASSIVATION LAYERS FOR P-TYPE SILICON SOLAR CELLS

Caratterizzazione elettrica di strati di passivazione a film sottile per celle solari in Silicio di tipo-p

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Abstract

This work characterizes p-type Silicon surface passivation using a high-k material (Al_2O_3 or HfO_2) combining capacitance voltage (CV) and lifetime measurements. For Al_2O_3 samples, the Silicon substrate bulk and surface quality is equivalent to CZ Silicon used in industrial solar cell processing. While Al_2O_3 has been proven to provide high quality surface passivation on p-type doped Silicon surfaces, the influence of the growth conditions and the post-deposition annealing is not yet completely understood. The dielectric thin film has been deposited by common techniques (ALD, PECVD) on H-/OH- terminated Silicon surfaces (hydrophobic and hydrophilic, respectively). The impact of the roughness of the surface prior to the deposition has been also considered. Then, the passivation of each layer has been investigated as a function of different Al_2O_3 thicknesses (5 to 30 nm) and post-deposition annealing temperatures (300 to 800 °C). CV measurements have been used to characterize *chemical passivation* (= interface trap density, D_{it}) and *field effect passivation* (= fixed charge density, Q_f). Lifetime measurements have been used to assess the effective surface passivation. The results of both types of electrical characterization fit well together. (i) Prior post-deposition anneal, only either chemical passivation (ALD) or field effect passivation (PECVD) is adequate, resulting in lower effective lifetimes. (ii) At higher annealing temperatures, a negative net charge in the Al_2O_3 and a low D_{it} at the interface are measured, ideal for p-type CZ Silicon passivation and causing maximal effective lifetimes. (iii) At too high annealing temperatures, chemical passivation is destroyed resulting in decreasing effective lifetimes even though negative field effect remains in many cases. Another candidate as passivation layer on Silicon is HfO_2. Being a new material in photovoltaics, it has been studied on high quality substrates (FZ Silicon) and its electrical characterization has demonstrated interesting passivation properties at low anneal temperatures, also as-deposited.

Sommario

Questo lavoro tratta la caratterizzazione della passivazione superficiale del Silicio di tipo-p ottenuta tramite materiali ad elevata costante dielettrica (Al_2O_3 e HfO_2), combinando misure di capacità-tensione (CV) e di tempo di vita. Per quanto riguarda i campioni di Al_2O_3, la qualità del substrato di Silicio e della superficie è equivalente al Silicio CZ utilizzato nella produzione industriale di celle solari. Se da un lato è stato dimostrato come Al_2O_3 possa fornire una passivazione superficiale di alta qualità su superfici di Silicio di tipo-p, l'influenza delle condizioni di crescita del materiale dielettrico e il contributo dell'annealing dopo la deposizione, non sono ancora stati del tutto compresi. Il sottile strato di dielettrico è stato depositato tramite tecniche comuni (ALD, PECVD) su superfici di Silicio con terminazioni H-/OH- (rispettivamente, idrofobiche ed idrofile). Anche l'influenza della rugosità della superficie, prima della deposizione del dielettrico, è stata considerata. La passivazione di ciascuno strato è stata analizzata in funzione di differenti spessori di Al_2O_3 (da 5 a 30 nm) e delle temperature degli annealing successivi alla deposizione (da 300 a 800 °C). Le misure CV sono state impiegate per caratterizzare la cosiddetta *passivazione chimica* (correlata alla densità di trappole all'interfaccia, D_{it}) e la *passivazione per effetto di campo* (legata alla densità di carica fissa, Q_f). Le misure di tempo di vita sono state utilizzate per valutare l'effettiva passivazione di superficie. I risultati di entrambi i tipi di caratterizzazione elettrica concordano fra loro. (i) Prima dell'annealing, soltanto la passivazione chimica (ALD) o la passivazione per effetto di campo (PECVD) è adeguata, comportando bassi tempi di vita per i portatori. (ii) A temperature di annealing maggiori, la presenza di una carica netta negativa all'interno di Al_2O_3 ed un basso livello di D_{it} all'interfaccia sono misurati, ideali per la passivazione del Silicio CZ di tipo-p, fornendo i maggiori tempi di vita. (iii) A temperature di annealing

troppo elevate, la passivazione chimica viene compromessa comportando una diminuzione dei tempi di vita, nonostante in molti casi un opportuno effetto di campo rimanga presente.
Un altro candidato come strato di passivazione su Silicio è HfO_2. Trattandosi di un materiale nuovo nell'ambito del fotovoltaico, è stato studiato su substrati di alta qualità (Silicio FZ) e la sua caratterizzazione elettrica ha dimostrato interessanti proprietà di passivazione a basse temperature di annealing, anche solo una volta depositato.

Preface

The present thesis is submitted as fulfillment of the prerequisites for obtaining the M.Sc. in Electrical Engineering at the University of Padova, Italy (Università degli Studi di Padova). The duration of this 21 ECTS credits project is a 8 months internship from September 2011 to May 2012. The work has been carried out at IMEC (Interuniversity Microelectronics Centre), Leuven (Belgium) in the "PV-Platform" group headed by Dr. Joachim John and with the supervision of Prof. Gaudenzio Meneghesso, professor of Microelectronics at the Department of Electrical Engineering at the University of Padova. From this work an article has been presented at last "IEEE – Photovoltaic Specialists Conference" in Austin (TX, USA) and the results obtained have been also used in other publications (Appendix A). I wish to thank Prof. Meneghesso and Dr. John to give me the opportunity to prepare this thesis abroad, permitting me to work in a real high-technology research group . I wish to thank everyone who helped me during this amazing experience, in particular my daily supervisor Dr. Bart Vermang. I also want to acknowledge Hans Goverde, Dennis Lin and Anne Lorenz for their precious help answering my questions.

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Chapter 1
Introduction

1.1 Energy Market:

In the beginning of the twenty-first century, our society is faced with an energy challenge: as highly populous, developing countries (Brazil, Russia, India and China over all) become more affluent and as the developed nations continue to increase their energy consumption (Fig. 1.1) [1], the energy demand in the entire world has reached levels that cannot be sustained in the future. At the same time, fossil fuels, which are currently providing more than 80% of the total global energy supply (Fig. 1.2) [1], are limited (according the most pessimistic previsions we have already reached the petroleum extraction peak [2]) and, in addition, their widespread use has significant adverse environmental consequences. The combustion of fossil fuels produces carbon dioxide, which is one of the causes of global warming as well as of other environmental effects, such as acid rain, higher ozone concentration in urban areas, particulates and aerosols that are detrimental to air quality. The limited supply of the fossil fuels and their effects on the global environment indicate the only long term solution of the energy challenge: a significant increase in the use of renewable energy sources for the production of electricity as well as for meeting other energy needs of the industrial and post-industrial human society.

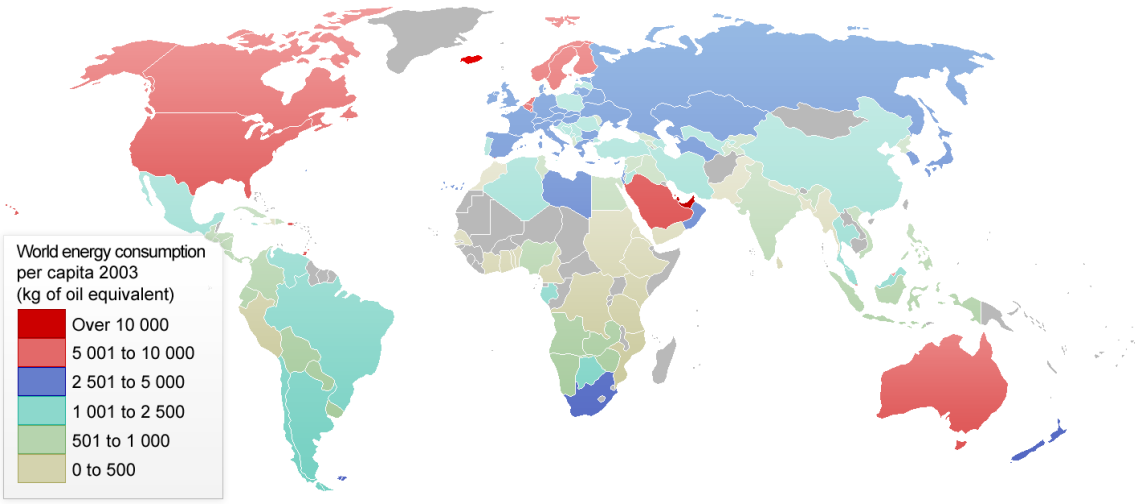


Figure 1.1: Map depicting world energy consumption per capita based on 2003 data [1]

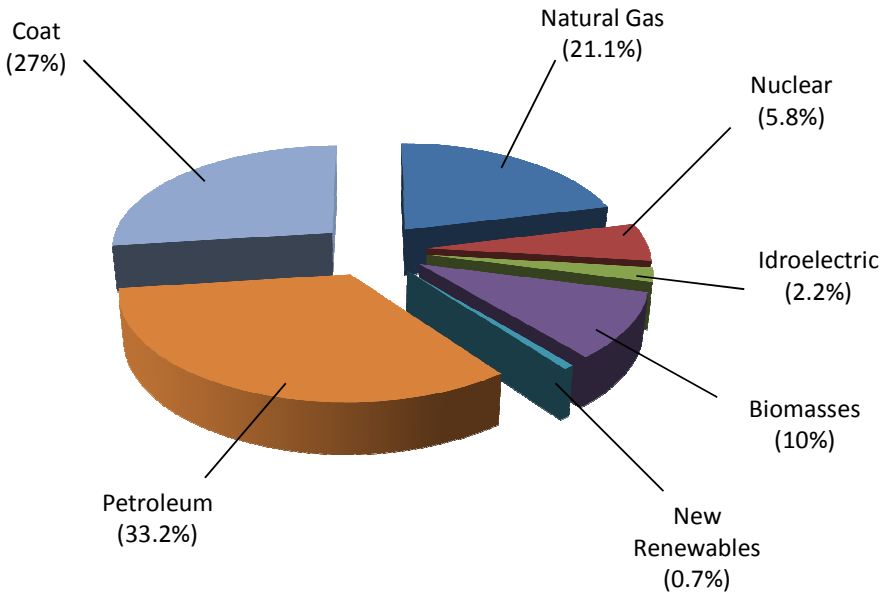
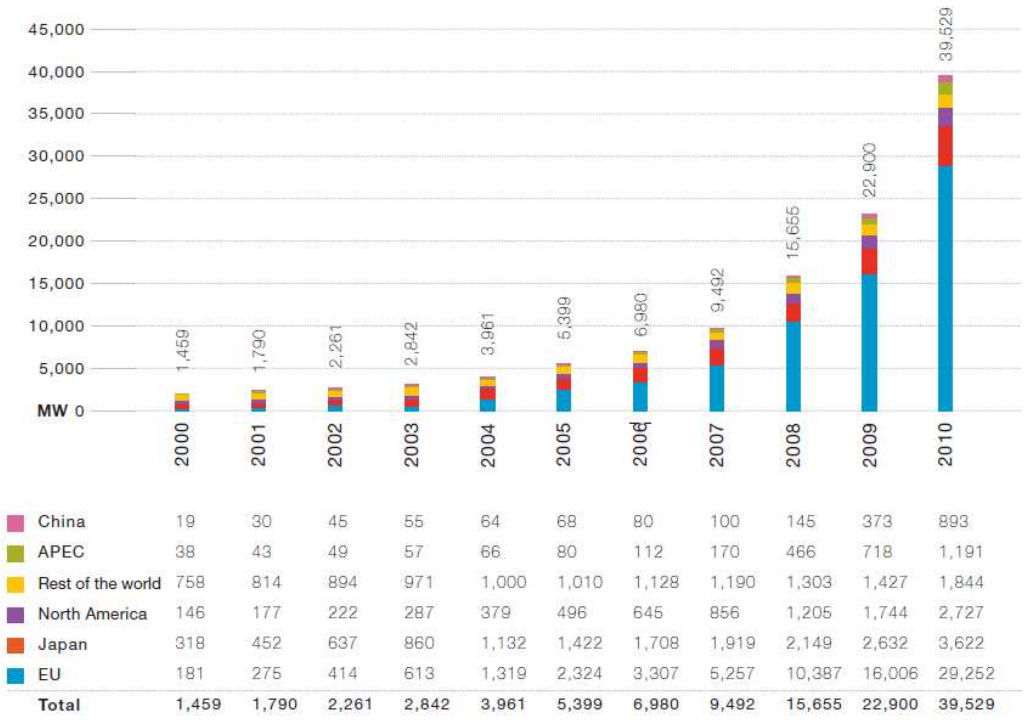


Figure 1.2: Primary energies in the world [1]

1.2 Photovoltaic Technologies

In 1839 Becquerel discovered the photovoltaic (PV) effect by demonstrating that electrons could interact with electromagnetic radiation with an electrolytic cell made from a Platinum electrode coated by Silver [4]. One century later (1954), Gerald Pearson, Daryl Chapin and Calvin Fuller were the first ones to build a PV device based on mono-crystalline Silicon with an energy conversion efficiency of ~ 6 % and an estimated cost of 200 $/W [5]. Nowadays, great strides have been made, leading to more and more efficient devices: the current record for commercial monocrystalline-Silicon based solar cell is ≈ 25% [6].



	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
China	19	30	45	55	64	68	80	100	145	373	893
APEC	38	43	49	57	66	80	112	170	466	718	1,191
Rest of the world	758	814	894	971	1,000	1,010	1,128	1,190	1,303	1,427	1,844
North America	146	177	222	287	379	496	645	856	1,205	1,744	2,727
Japan	318	452	637	860	1,132	1,422	1,708	1,919	2,149	2,632	3,622
EU	181	275	414	613	1,319	2,324	3,307	5,257	10,387	16,006	29,252
Total	**1,459**	**1,790**	**2,261**	**2,842**	**3,961**	**5,399**	**6,980**	**9,492**	**15,655**	**22,900**	**39,529**

Figure 1.3: Evolution of global cumulative installed PV capacity (2000-2010) [3]

Photovoltaics, among other forms of renewable energies (e.g. wind, hydro, biomass, and geothermal) can be considered a credible candidate to face the global climate change and energy crisis. Compared to conventional energy production by burning fossil fuels, PV has

several advantages ranging from offsetting greenhouse gas emissions, to meeting government renewable energy targets, to providing a cost-competitive and self-sufficient energy option for rural and remote communities. However, in order for PV to be widely accepted as an economically viable means of electricity generation and to be used on a larger scale across the world, the levelized cost of PV electricity must be reduced to values that are competitive with conventional electricity.

The progress of PV market over the last 10 years has been impressive: the total installed PV capacity in the world has multiplied by a factor of 27, from 1.5 GW in 2000 to 39.5 GW in 2010 with a yearly growth rate of 40% (Fig. 1.3) [3]. That growth has proved to be sustainable, allowing the industry to develop at a stable rate and governments to finance further research.

1.3 Silicon Solar Cells

PV market is expected to be dominated by crystalline Silicon solar cells for at least the next decade [3]: Silicon dominance will last at least until 2020. In order to maintain this market share of Silicon in PV technology and obtain grid parity, production costs require a significant reduction. At present, the Silicon wafer cost constitutes about 70% of the cell cost [7], driving the PV industry to ever thinner wafers.

PV industry uses solar grade Czochalski (CZ) Silicon (less pure and less expensive) for the production of solar cell. The typical thickness of a mono-crystalline solar cell is 200 μm: Silicon solar cells costs can be reduced by decreasing the Silicon substrate thickness. The continuous decrease of the substrate thickness yields an increased surface-to-volume ratio that makes *surface passivation* a crucial point. Passivation means the deposition on the Silicon substrate of a *passivating surface layer* such as Silicon nitride, Silicon dioxide or

Titanium dioxide, which can reduce surface recombination and increase the efficiency of the solar cell.

1.4 Silicon Surface Passivation

As described in the above paragraph, the passivation of the Silicon surface is one of the most relevant technological challenges to reduce thickness of the Silicon substrate. The effective recombination can be used to express the level of surface passivation. As it will be widely explained in Chap. 2, the surface is an abrupt interrupt of the Silicon crystal lattice resulting in a high density of dangling bonds on top of the wafer. The dangling bonds create interface traps, which are active recombination centers of excited electron/hole pairs. The interface trap density can be reduced by synthesizing a thin functional film (passivation layer) on the Silicon surface to reduce the effects of dangling Silicon bonds. Furthermore, an electrical field can be created at the Silicon/deposited film interface, by forming a fixed charge density with the adequate polarity within the passivation layer. When this electrical field has the right polarity, it can repel the free electrons at the surface reducing the carrier concentration at the surface. Both effects lead to reduction of the effective surface recombination velocity and therefore to an increase of conversion efficiency. They are indicated as "*chemical passivation*" and "*field effect passivation*" respectively. They are considered the most common passivation techniques and this work provides a characterization of the Silicon surface passivation by analyzing these two aspects.

1.5 Outline of the Thesis

This thesis wants to provide a description of the Silicon surface passivation (in terms of chemical passivation and field effect passivation) by electrical measurements. Various passivation layers have been investigated (varying the material used, the deposition

technique, the post-deposition annealing temperature). The work is developed in the following chapters:

- *Chap.2* provides an exhaustive dissertation about the carrier recombination theory. The main recombination mechanisms are discussed.

- *Chap. 3* illustrates the most common techniques to deposit passivation layers. Also the followed steps to prepare the samples investigated are here explained.

- *Chap.4* provides a theoretical explanation of the electrical measurement techniques used to characterize the passivation properties. The results of the first passivation layer (ALD Al_2O_3) are here collected.

- *Chap.5* presents a different deposition technique for Al_2O_3: PECVD.

- *Chap.6* discusses the characterization of a novel material for Silicon surface passivation: HfO_2.

Chapter 1 References

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Chapter 2

Recombination in Crystalline Silicon

This chapter explains in detail the theory of generation and recombination in Silicon: the theoretical approach is mostly based on [1, 2]. Generation in semiconductors is the process whereby electron-hole pairs are created and recombination is its opposite: a loss of electron-hole pairs, with the excess energy released as either *photons* or *phonons*. Recombination therefore reduces the performance of solar cells, particularly the open circuit voltage (V_{oc}). Experimentally, it is the recombination lifetime that is measured. The recombination lifetime (τ) of a material can be defined as the average time for an electron – hole pair to recombine following generation. It can be determined from the recombination rate (U) as shown in Equation 2.1:

$$\tau = \frac{\Delta n}{U} \tag{2.1}$$

where Δn (Δp) is the excess carrier density of electrons (holes) and $\Delta n = \Delta p$ in the absence of trapping effects. Interpreting this recombination lifetime can be difficult, as it represents a number of specific recombination mechanisms occurring simultaneously within the bulk and at the surfaces. For this reason, the recombination lifetime is sometimes referred to as an *effective lifetime.*

2.1 Recombination Mechanisms

Three fundamental recombination mechanisms that occur in semiconductors are (i) *radiative recombination*, (ii) *Auger recombination*, and (iii) recombination through defects in the bandgap (as known as *Shockley – Hall – Read recombination*). Other recombination processes within solar cells can generally be viewed as a combination of these three fundamental mechanisms: (a) The surface of a semiconductor represents an abrupt discontinuity in its otherwise uniform crystal structure. The high number of dangling bonds creates a large density of defects throughout the bandgap. Therefore, *surface recombination* is a particular case of process (iii) above. (b) Similarly, in the heavily doped emitter regions of a solar cell, the high doping results in Auger recombination limiting the lifetime within the emitter, in conjunction with surface recombination at the emitter surface. *Emitter recombination* is therefore a particular case of processes (ii) and (iii) above.

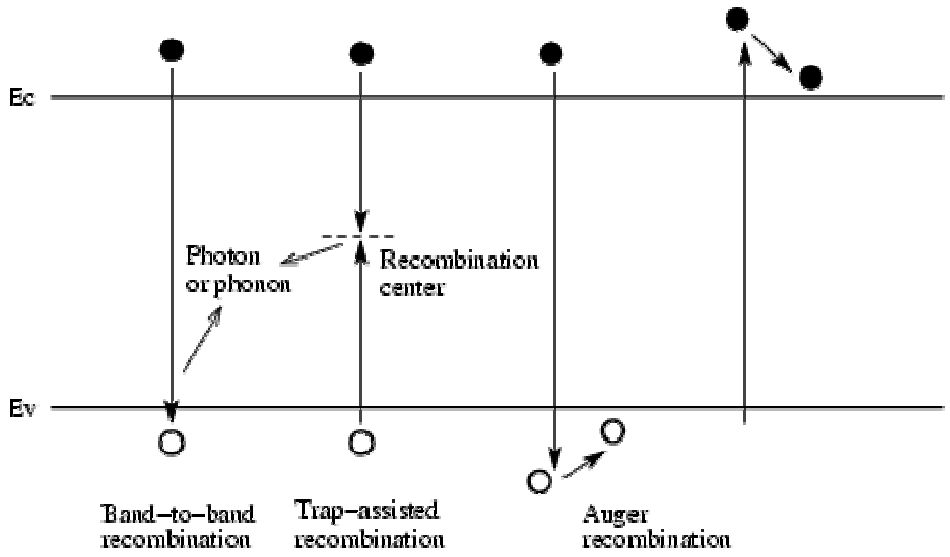

Figure 2.1: The main recombination mechanisms are depicted: (a) radiative recombination, (b) recombination through defects in the bandgap, (c) Auger recombination with the excess energy transferred to a valence band hole or to a conduction band electron.

2.1.1 Radiative Recombination

Radiative recombination is simply the direct destruction of an electron - hole pair as depicted in Figure 2.1 (a): it is the inverse process to optical generation, the excess energy being released mainly as a photon with an energy close to that of the bandgap. It involves a conduction band electron falling from an allowed conduction band state into a vacant valence band state (a hole). Therefore, as seen in Equation 2.2, the radiative recombination rate (U_{rad}) depends on the concentration of free electrons (n) and free holes (p), while B is the coefficient of radiative recombination.

$$U_{rad} = Bnp \tag{2.2}$$

From Equation 2.2, the common relationships for the radiative lifetime in n-type and p-type material under low injection ($\tau_{rad,li}$) and high injection conditions ($\tau_{rad,hi}$) can be determined as shown in Equation 2.3, where N_{dop} is respectively the density of donor (N_D) or acceptor atoms (N_A). It can be seen that the radiative lifetime depends on the inverse of the majority carrier density ($\tau_{rad} \propto 1/n$). Therefore, τ_{rad} is constant at low injection, but then decreases and continues to decrease as the injection level increases. In general, the rate of radiative recombination in Silicon is considered negligible compared to other recombination processes, since Silicon is an *indirect-bandgap* semiconductor and must simultaneously emit a photon and a phonon to conserve both energy and momentum (improbable, according to quantum mechanics).

$$\tau_{rad,li} = \frac{1}{BN_{dop}} \qquad and \qquad \tau_{rad,hi} = \frac{1}{B\Delta_n} \tag{2.3}$$

2.1.2 Auger Recombination

Traditionally, Auger recombination is viewed as a three-particle interaction where a conduction band electron and a valence band hole recombine, with the excess energy being transferred to a third free electron or hole, as depicted in Figure 2.1 (c). The charge carriers involved are assumed to be non-interacting quasi-free particles. Therefore, the *eeh* process denotes when the excess energy is transferred to another electron, with the recombination rate given by $U_{eeh} = C_n n^2 p$. Similarly, the *ehh* process denotes when the excess energy is transferred to another hole, with recombination rate $U_{ehh} = C_p n p^2$, where C_n and C_p are Auger coefficients. The total Auger recombination rate (U_{Auger}) is then given by Equation 2.4, from which the common relationships for the Auger lifetime in n-type and p-type material under low injection ($\tau_{Auger,li}$) and high injection conditions ($\tau_{Auger,hi}$) can be determined. Both are shown for p-type Silicon in Equation 2.5, where $C_a = C_n + C_p$ is the ambipolar Auger coefficient.

$$U_{Auger} = C_n n^2 p + C_p n p^2 \tag{2.4}$$

$$\tau_{Auger,li} = \frac{1}{C_p N_A^2} \quad and \quad \tau_{Auger,hi} = \frac{1}{(C_n + C_p)\Delta n^2} \tag{2.5}$$

From Equation 2.5, it can be seen that the Auger lifetime ideally depends on the inverse of the carrier density squared ($\tau_{Auger} \propto 1/n^2$). It shows a stronger dependence with the injection level than τ_{rad}, and therefore, Auger recombination will become the dominant mode of recombination in Silicon for high injection levels, as might occur in concentrator solar cells, or for high doping densities, as occurs in heavily doped emitter regions. However, Auger recombination is more complicated. Band-to-band Auger processes can occur with phonon participation (*phonon-assisted Auger recombination - PAAR*) and without phonon participation (*direct Auger recombination - DAR*) to conserve momentum. Furthermore, a third Auger recombination mechanism, *termed trap-assisted Auger recombination* (*TAAR*)

has been also proposed. Finally, additional processes that have not yet been accounted for may impact the Auger lifetime. One such possibility is the Coulombic interactions between mobile charged carriers and fixed charges (ionized dopant atoms). A general parameterization of Auger recombination has been proposed by Kerr and can be found in Equation 2.6 [1]. The parameterization is intended to provide the simplest functional form for the experimental observations of Auger recombination in Silicon and demonstrates that Auger recombination is increased above the ideal rate, and that the increase is a function of both the doping density and the injection level.

$$U_{Auger} = np(1.8 \times 10^{-24} n_o^{0.65} + 6 \times 10^{-25} p_o^{0.65} + 3 \times 10^{-27} \Delta n^{0.8}) \quad (2.6)$$

2.1.3 Bulk Recombination Through Defects

The presence of defects within a semiconductor crystal, coming from impurities or crystallographic imperfections such as dislocations, produces discrete energy levels within the bandgap. As shown in Figure 2.1 (b), these defect levels, also known as *traps*, greatly facilitate recombination through a two step process : a free electron from the conduction band first relaxes to the defect level and then relaxes to the valence band where it annihilates a hole. The dynamics of this recombination process were first analyzed by Shockley and Read [3] and Hall [4], with the recombination rate (U_{SRH}) for a single defect level given by Equation 2.7. Where n_i is the intrinsic carrier concentration and τ_{p0} and τ_{n0} are the fundamental hole and electron lifetimes which are related to the thermal velocity of charge carriers (v_{th}). The density of recombination defects (N_t), and the capture cross-sections (σ_p and σ_n) for the specific defect as shown in Equation 2.8. n_1 and p_1 are statistical factors defined as in Equation 2.9, where N_C and N_V *are the effective density of states* at the conduction and valence band edges, E_C and E_G are the conduction band and bandgap energies and E_t is the energy level of the defect. k is the Boltzmann's constant.

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{2.7}$$

$$\tau_{p0} = \frac{1}{\sigma_p v_{th} N_t} \qquad and \qquad \tau_{n0} = \frac{1}{\sigma_n v_{th} N_t} \tag{2.8}$$

$$n_1 = N_C \, exp \frac{E_t - E_C}{kT} \qquad and \qquad p_1 = N_V \, exp \frac{E_C - E_G - E_t}{kT} \tag{2.9}$$

It follows from Equation 2.1 that the SRH lifetime (τ_{SRH}) can be expressed as in Equation 2.10. It can be seen that the SRH lifetime is a function of the carrier injection level and the dopant density (through n_0 and p_0), as well as defect specific properties such as the concentration of traps, their energy level and their capture cross-sections. An important result that follows is that traps with energies close to the centre of the bandgap (deep defects) are the most effective recombination centers. Furthermore, for such deep defects in p-type Silicon, the SRH lifetime can be simplified for low injection ($\tau_{SRH,li}$) and high injection ($\tau_{SRH,hi}$) conditions as in Equation 2.11.

$$\tau_{SRH} = \frac{\tau_{n0}(p_0 + p_1 + \Delta_n) + \tau_{p0}(n_0 + n_1 + \Delta_n)}{n_0 + p_0 + \Delta n} \tag{2.10}$$

$$\tau_{SRH,li} = \tau_{n0} \qquad and \qquad \tau_{SRH,hi} = \tau_{n0} + \tau_{p0} \tag{2.11}$$

Figure 2.2 shows lifetime curves for a 1 Ω·cm p-type Silicon wafer for SRH recombination (deep defect, τ_{n0} = 1 ms and τ_{p0} = 20 ms), radiative recombination and free-particle Auger recombination. It can be seen that recombination through deep defects results in a distinctly different injection level dependence than the intrinsic recombination processes (radiative and Auger), and that SRH recombination normally dominates at low injection levels, eventually being surpassed by the rate of Auger recombination at sufficiently high injection levels.

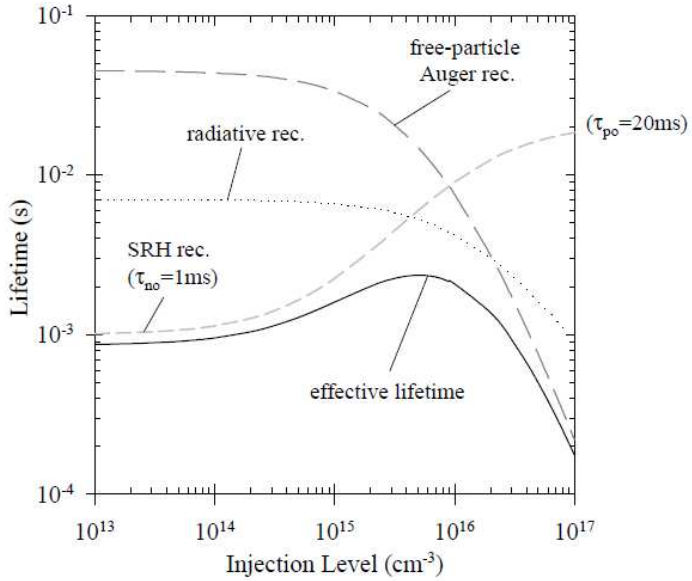

Figure 2.2: Lifetime curves for a 1 Ω·cm p-type Silicon wafer for *SRH recombination* (deep defect, τ_{n0} = 1 ms and τ_{p0} = 20 ms), *radiative recombination* and *free-particle Auger recombination*, taken from [1].

2.1.4 Surface Recombination Through Defects

Since the surfaces or interfaces of a Silicon substrate represent an abrupt discontinuity in its crystalline structure, the SRH bulk recombination discussion above serves as a useful starting point for the analysis of defects originating at the surfaces of semiconductors. The large numbers of partially bonded Silicon atoms give rise to many *dangling bonds*, and therefore a large density of defect levels are found within the bandgap near the semiconductor surface. Even if the Silicon surface is not bare (due to a native oxide on top) the presence of Silicon-oxygen bonds can stress the crystal structure at the surface, which again introduces many defect states. The SRH analysis of Section 2.1.3 can be again applied, although it has to be reformulated in terms of recombination events per unit surface area, rather than per unit volume. For a single defect at the surface, the rate of surface recombination ($U_{surface}$) is given by Equation 2.12, where n_s and p_s are the

concentrations of electrons and holes at the surface, and S_{no} and S_{po} are related to the density of surface states per unit area (N_{ts}), and the capture cross-sections (σ_p and σ_n) for the specific defect as shown in Equation 2.13.

$$U_{surface} = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2.12}$$

$$S_{n0} = \sigma_n v_{th} N_{ts} \qquad and \qquad S_{p0} = \sigma_p v_{th} N_{ts} \tag{2.13}$$

In reality, defect levels are so numerous that they can be considered to be continuously distributed throughout the bandgap, and both their density and capture cross-sections will be dependent on their energy level. Using $D_{it}(E)$ for the density of interface traps at a given energy (rather than N_{ts} for a specific energy level) and integrating over the entire bandgap (from valence band energy E_V to conduction band energy E_C), Equation 2.14 follows for a continuum of noninteracting surface states E_{it}. Similar to the definition of the recombination lifetime, the effective surface recombination velocity (S_{eff}) is defined as in Equation 2.15 and so the surface recombination velocity can be related to the fundamental properties of the surface defects through Equations 2.12 and 2.14.

$$U_{surface} = \int_{E_V}^{E_C} \frac{v_{th}(n_s p_s - n_i^2)}{\frac{n_s + n_1}{\sigma_p(E_{it})} + \frac{p_s + p_1}{\sigma_n(E_{it})}} D_{it}(E_{it}) dE_{it} \tag{2.14}$$

$$U_{surface} = S_{eff} \Delta n \tag{2.15}$$

What can be concluded from Equation 2.14 is that there are two fundamental mechanisms for reducing the surface recombination rate at a semiconductor surface. (1) Reducing the density of the interface states and the magnitude of the capture cross-sections. By growing an appropriate dielectric layer such as Silicon oxide, many of the dangling Silicon bonds

are passivated with oxygen or hydrogen atoms and the D_{it} is reduced. (2) Minimizing the concentration of minority carriers also reduces the surface recombination rate. (2a) This can be achieved by doping the semiconductor surface to repel the minority carries such as in an emitter region or a BSF. (2b) Alternatively, fixed charges in an overlying dielectric layer can be used to either repel the minority carriers (for a p-type wafer one would use negative charges to repel the free electrons), or in the extreme case invert the surface (large amounts of fixed positive charges would invert the surface of a p-type Silicon wafer). This is also known as *field effect passivation*, as an electric field is essentially established near the surface.

2.1.5 Emitter Recombination

Modeling the recombination occurring within an emitter region from first principles is relatively complicated. Doping profiles are not normally uniform and so the spatial variation in the dopant concentration needs to be considered, as does the possibility of a dead layer from the diffusion process. Heavy doping effects including the degeneracy of the semiconductor, bandgap narrowing and free-carrier absorption need to be included, along with intrinsic recombination processes and the normal SRH recombination processes related to defects, both within the emitter and at the emitter's surface.

Because the emitter regions are heavily doped, two simplifications follow. Firstly, the minority carrier concentration in the emitter region normally remains low and secondly, Auger recombination is likely to be the dominant bulk recombination mechanism. It follows that the recombination lifetime in the emitter region is constant with injection level, and the recombination current into the emitter (J_{rec}) can be expressed as in Equation 2.16, where J_{0E} is defined to be the emitter saturation current density, and n and p refer to the electron and hole concentrations on the base side of the space-charge region.

$$J_{rec} = J_{0E} \frac{np}{n_i^2} \tag{2.16}$$

Emitter recombination can be viewed as a special case of surface recombination. A virtual surface can be defined just at the base side of the space-charge region. Hence, combining Equations 2.15 and 2.16 reduces for p-type Silicon to the quasistatic emitter approximation (Equation 2.17), with q the elementary charge. It is important to differentiate such a virtual surface from the actual surface of an emitter. The S_{eff} at the virtual surface is merely another way of representing the J_{0E}.

$$S_{eff} = J_{0E} \frac{N_A + \Delta n}{q n_i^2} \tag{2.17}$$

2.2 The Effective Lifetime (τ_{eff})

The five recombination mechanisms discussed in Section 2.1 may occur simultaneously within a semiconductor. In many situations, some of the recombination processes will contribute negligibly to the overall recombination rate (e.g. radiative recombination in Silicon). Indeed, in many experimental situations the aim is to minimize the other recombination mechanisms to facilitate the exploration of one particular recombination process. In the study of surface recombination processes for example, high quality float-zone (FZ) Silicon wafers can be used to minimize bulk recombination. In other situations, the contributions from different recombination processes will be unknown or even unavoidable. It is therefore necessary to consider how the different recombination mechanisms combine to give an overall effective recombination rate or an effective lifetime. In general, the recombination processes can be considered to occur independently and the effective recombination rate (U_{eff}) is simply the sum of the individual rates, as expressed in Equation 2.18, where the first three terms refer to bulk recombination processes and are often grouped as in Equation 2.19.

$$U_{eff} = U_{rad} + U_{Auger} + U_{SHR} + U_{surface} + U_{emitter} \quad (2.18)$$

$$U_{bulk} = U_{rad} + U_{Auger} + U_{SHR} \quad (2.19)$$

Test structures used for examining recombination at the interface of Silicon and a passivating film are briefly discussed.

The test structure is a Silicon wafer which has been passivated on both sides with an identical dielectric film. The recombination rate can be expressed as in Equation 2.20 and simplifies to Equation 2.21 if the carrier profiles are relatively uniform throughout the wafer with a thickness W.

$$U_{eff} = U_{bulk} + 2U_{surface} \quad (2.20)$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \quad (2.21)$$

2.3 Measuring the Effective Lifetime

2.3.1 Lifetime Measurement

As an accurate determination of recombination lifetime is a fundamental prerequisite for lifetime spectroscopy. The measurement of carrier lifetimes is based on the recombination dynamics of excess carriers which are normally generated optically. The different techniques may be classified in terms of the time dependence of the illumination and the technique used to measure the excess carrier density. Concerning the time dependence of

the illumination, three operating regimes can be distinguished. (i) The first regime involves a sharp pulse of illumination that is rapidly turned off and a subsequent determination of the excess carrier density without illumination. This is the traditional *transient technique*, used especially to measure high carrier lifetimes. (ii) The second regime is the *steady-state illumination*, which is of minor importance due to the problem that the samples will quickly suffer from heating and a changing lifetime in true steady state. (iii) Such effects are avoided in the third regime, where the illumination intensity is slowly reduced to zero over several milliseconds, the decay being long enough to ensure that the sample remains in steady state in terms of the recombination processes. This is the basis of the *quasi-steady-state method* first introduced by Sinton and Cuevas [7].

The major advantage of a slowly decaying illumination is that a large range of operating points can be conveniently explored. Note that the covered range of carrier densities is typically about one order of magnitude (in this work typically ~ 10^{14} - 10^{15}). Obviously the first two regimes are special cases of the third, which therefore represents the general case.

The detailed analysis of the recombination dynamics in all three cases is based on the continuity equation for the excess minority carriers (Equation 2.22).

$$\frac{\partial \Delta n}{\partial t} = G_{bulk}(t,x) - U_{bulk}(t,x) + \frac{1}{q}\frac{dJ_n}{dx} \qquad (2.22)$$

where G_{bulk} and U_{bulk} are the photogeneration rate and the recombination rate in the bulk, Δn the excess minority carrier density (usually ≈ 10^{15} cm^{-3} in this work) and J_n the electron current density. The transport term reduces to surface recombination terms when Equation 2.22 is integrated over the sample width, because the sample is in open-circuit conditions. A generalized analysis procedure has been proposed by Nagel et al. [8]. In order to define an effective lifetime regardless of the decay time of the illumination source, they combined the bulk and surface recombination rates into an effective recombination rate *Ueff* and

found, considering all the terms in Equation 2.22, the following Equation 2.23 for the effective carrier lifetime.

$$\tau_{eff} = \frac{\Delta n_{av}}{G_{av}(t) - \frac{\partial \Delta n_{av}(t)}{\partial t}} \qquad (general\ case) \qquad (2.23)$$

where n_{av} is the average excess carrier density and G_{av} the average generation rate, both calculated over the whole wafer thickness. In the extreme operating regimes, simplified τeff expressions follow directly from Equation 2.23.

In the first regime with $G = 0$:

$$\tau_{eff} = \frac{\Delta n_{av}}{\frac{\partial \Delta n_{av}(t)}{\partial t}} \qquad (quasi - transient\ case) \qquad (2.24)$$

which is only valid when carrier lifetime is significantly higher than the decay time of the illumination source.

In the second regime with $\partial \Delta n/\partial t = 0$:

$$\tau_{eff} = \frac{\Delta n_{av}}{G_{av}(t)} \qquad (quasi - steady - state\ case) \qquad (2.25)$$

which is only valid when the carrier lifetime is significantly lower than the decay time of the illumination source.

Thus, to determine the effective lifetime it is necessary to measure the time dependence of the excess carrier density and the generation rate within the test samples (except for the transient case). The excess carrier density can be directly monitored via the photoconductance, which can be measured inductively (*Quasi-Steady-State*

Photoconductance technique, QSSPC) or by means of the reflectivity of microwaves (*Microwave-Detected Photoconductance Decay technique, MW-PCD*). Only the first one has been used in this work and it will be widely described.

A common feature of both techniques is that they are non-contacting, which makes them ideally suited for lifetime spectroscopic purposes, as partially finished devices that are free of metal contacts can be investigated, including the starting material itself, as in the present work.

2.3.2 Quasi-Steady-State Photoconductance Technique (QSSPC)

The experimental apparatus used in the present work for QSSPC measurements was fabricated by *Sinton Consulting* [9] and is shown in Fig. 2.3a(Appendix B). A photographic flash lamp (Fig. 2.3b) is used as the generation source. The sample is inductively coupled by a coil to a radio-frequency bridge, which senses changes in the permeability of the sample and therefore its conductance. A reference solar cell and an oscilloscope are used to determine the time dependence of both the excess photoconductance of the test sample $\Delta\sigma(t)$ and its illumination $I(t)$ by using appropriate calibration functions. The average excess carrier density $\Delta n_{av} = \Delta p_{av}$ in the test sample can be determined by Equation 2.26.

$$\Delta n_{av}(t) = \frac{\Delta\sigma(t)}{q(\mu_n + \mu_p)W} \tag{2.26}$$

where W is the sample thickness and μ_n and μ_p are the electron and hole mobilities. As μ_n and μ_p are themselves functions of the carrier density, the determination of Δn_{av} requires an iterative procedure on the basis of a carrier-density-dependent mobility model [10].

The illumination intensity I_{av}, measured from the calibrated reference solar cell and normally quoted in suns (1 sun = 1000 W/m^2), is a measure of the number of photons

incident on the sample surface. As any real sample will only absorb a fraction f_{abs} of these available photons, the remainder being lost by reflection and transmission, the generation rate within the sample can be determined as Equation 2.27.

$$G_{av}(t) = \frac{I_{av}(t)\, f_{abs}\, N_{ph}^{1sun}}{W} \tag{2.27}$$

where ${N_{ph}}^{1sun}$ is the flux of photons in solar light with an irradiance of 1 sun, which generate electron-hole pairs in the sample. As the required quantities in the general Equation 2.23 can thus be experimentally measured, a determination of the effective lifetime is possible.

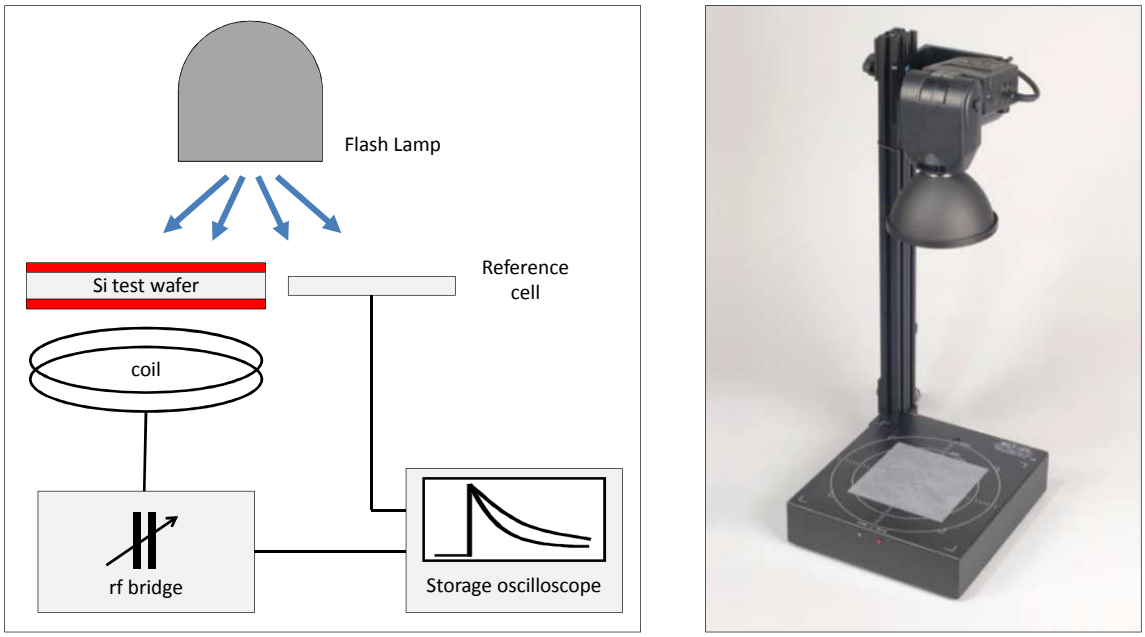

Figure 2.3: (a) Schematic of the inductively coupled photoconductance apparatus used for measuring the effective lifetime. The picture also illustrate the particular sample under test: the Silicon wafer investigated has been coated on both sides with an identical dielectric film. (b) The Xenon photo flash lamp WCT-120 here used for QSSPC, fabricated by *Sinton Consulting* [9].

As the decay time of the flash lamp may be varied by two orders of magnitude, the QSSPC setup allows measurements in the *transient mode* (PCD) and in the *quasi-steady-state mode* (QSSPC). The typical PCD and QSSPC traces are displayed in Fig. 2.4a and 2.4b, respectively. In conjunction with the simplified analyses given in Equations 2.24 and 2.25, both modes are restricted to certain lifetime ranges. Being well suited for high lifetimes, the PCD mode is less accurate for low lifetimes (< 200 µs) due to the poor cutoff time of the flash lamp. The QSSPC mode, on the contrary, is well suited for low lifetimes, but becomes increasingly invalid for high lifetimes (> 200 µs), as the steady-state assumption starts to break down.

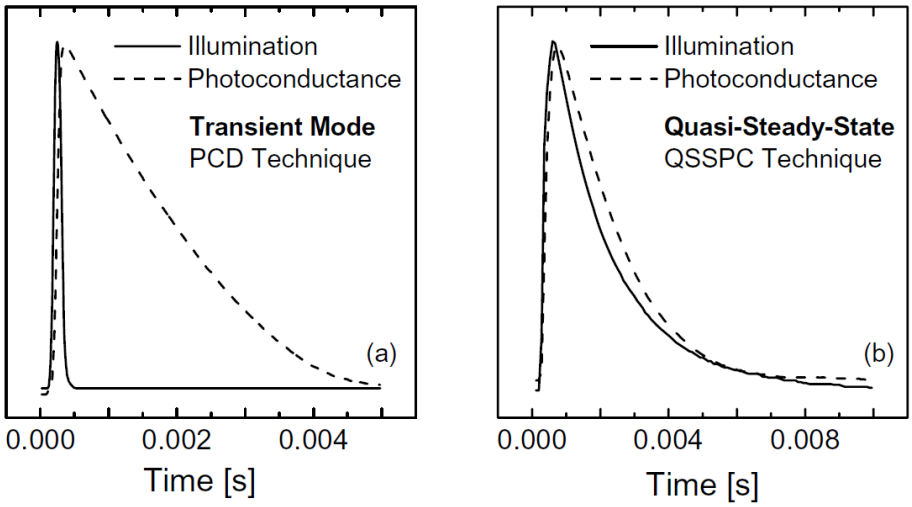

Figure 2.4: Typical traces measured by means of the inductively-coupled QSSPC system. (a) Traces in the transient mode showing the sharp illumination peak (*solid line*) and the ensuing photoconductance decay (*dashed line*). (b) Traces in the quasi-steady-state mode, showing the uniform decay of both signals.

However, using the QSSPC mode in conjunction with the generalized analysis given in Equation 2.23, it constitutes an excellent method for measuring a large range of carrier lifetimes (from 0.1 µs to several ms) over a large range of carrier densities (10^{12}–10^{17} cm^{-3}, depending on the lifetime level). Thus, this technique is ideally suited for injection-

dependent lifetime measurements and has been used throughout this work. Details about the calibration of the coil and the reference solar cell may be found in [11].

An example of one lifetime QSSPC measurement as a function of carrier density can be founded in Fig. 2.5. As mentioned in the presentation of this work, all the investigated samples have been made of solar grade material (CZ Silicon): this point is widely developed in Chap. 4. This means that the investigated samples may have a low level of uniformity: this can be seen in Fig. 2.5. Different curves (red dots) have been obtained only changing the stimulated area of the sample, indicating not uniform properties on the investigated area because of the low quality material used. Fig. 2.5 also indicates a clear lifetime degradation over time: the back dots correspond to measurements done ~ 2 months later than the red dots.

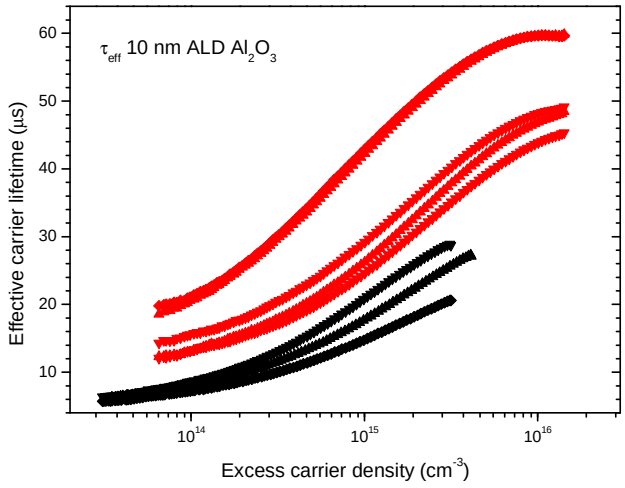

Figure 2.5: Example of injection-level-dependent effective lifetime measurements using QSSPC technique. The Silicon substrate was coated by 10 nm ALD Al_2O_3. (i) Red dots have been measured stimulating different points on the passivated surface: the dispersion indicate the not perfect uniformity of the sample. (ii) The black dots have been measured on the same saple after ~ 2 months: the degradation is evident.

Chapter 2 References

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Chapter 3
High-k Material Deposition Techniques

In this work, high-k materials are characterized as negatively charged passivation layer for p-type Silicon. Therefore, in this chapter some relevant deposition techniques are discussed first. (i) *Atomic Layer Deposition* (ALD) presents (a) excellent uniformity and growth control, and (b) high trimethylaluminum (TMA, $Al(CH_3)_3$) efficiency. Other deposition techniques here discussed are (ii) *Plasma-Enhanced* (PE) *or Plasma-Assisted* (PA) *ALD*, (iii) *Chemical Vapor Deposition* (CVD) and (iv) *Plasma Enhanced Chemical Vapor Deposition* (PECVD).

3.1 Wafer Cleaning

Prior to starting with any deposition of the passivation layer, advanced cleaning treatment of Silicon surface is required in order to decrease the level of impurities and obtain a sufficient cleanliness of the surface. This chemical process can leave an oxidized Silicon OH- surface (*Hydrophilic surface*) or an HF last Silicon H- surface (*Hydrophobic surface*). The wafer investigated have been cleaned using a technique similar to the *RCA clean standard*, the procedure developed in 1965 by Werner Kern while working for *Radio Corporation of America* [1, 2].

Passivation layers investigated have been deposited on p-type Czochralski (CZ) Silicon substrates with a resistivity of 1 - 1.5 Ω·cm and a thickness of 180 µm. They first endure a *Saw Damage Removal* (SDR) to reduce damages after the sawing of an ingot. This etching process has two steps: (i) a dip in NaOH : H_2O (5 minutes at 85 °C) and (ii) neutralization in HCl : H_2O (10 minutes at 85 °C). Between SDR and cleaning, the wafers are then dipped into a *Hydrofluoric acid* (HF) and water solution for 10 seconds (the HF concentration is about 2%) to remove mostly the organic impurities on the surface. This HF dip is a characteristic step of IMEC process and is not mentioned in the *standard procedure* (RCA). Afterwards, the samples are soaked in a *Sulfuric Peroxide Mixture* (SPM), H_2O_2:H_2SO_4 1:4, for 10 minutes at 85°C. This treatment results in the formation of a thin Silicon dioxide layer on the Silicon surface that traps metallic contaminants on the wafers' surface. Finally, this dioxide layer is removed with a final dip in HF water solution (2%) and HCl water solution (5%). Now the surface of each wafer is H- terminated and presents a lower level of roughness and contamination. OH- terminations on the surface require an additional step: *Ammonium Peroxide Mixture* (APM, NH_4OH:H_2O_2:H_2O 1:1:5) allows the formation of these OH groups on the wafer.

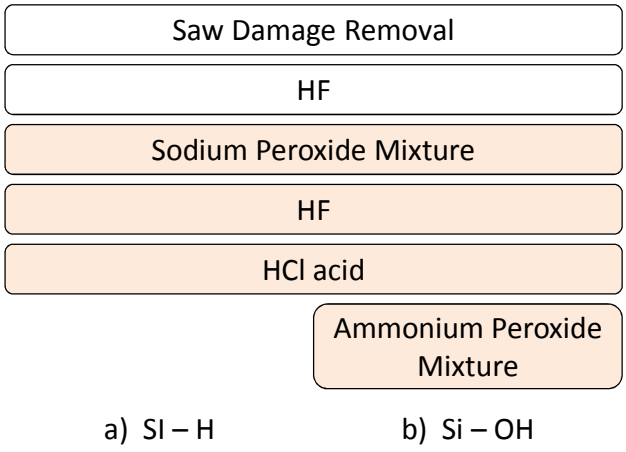

Figure 3.1: Surface cleaning sequences of p-Silicon wafers. Prior the as-known *standard cleaning* (red cells), a polishing process and an additional HF dip have been done (white cells). After the last dip in Hydrochloric acid, the surface is H- terminated (a). An additional cleaning step (APM) is required to have OH- terminations on the surface (b).

3.2 Drying Techniques

After the cleaning, a drying process of the surface is needed. There are several techniques available: the samples here investigated have been dried using a *Marangoni dryer*. This is an expensive and time consuming technique (compared to others, e.g. *hot-air*) but it has been used since a low level of impurities on the surface is required.

The substrates are introduced in a tank filled with water. An alcohol vapor (*Isopropyl alcohol*, IPA) is vaporized using heated H_2 through nozzles over the wet wafer surface. The Marangoni effect is introduced by a surface-tension gradient in the wetting film (IPA:H_2O) on the substrate, causing the water film quickly drain backwards into the rinse bath. As a result, a completely dry substrate emerges from the bath [3]. For a schematic representation, see Figure 3.2.

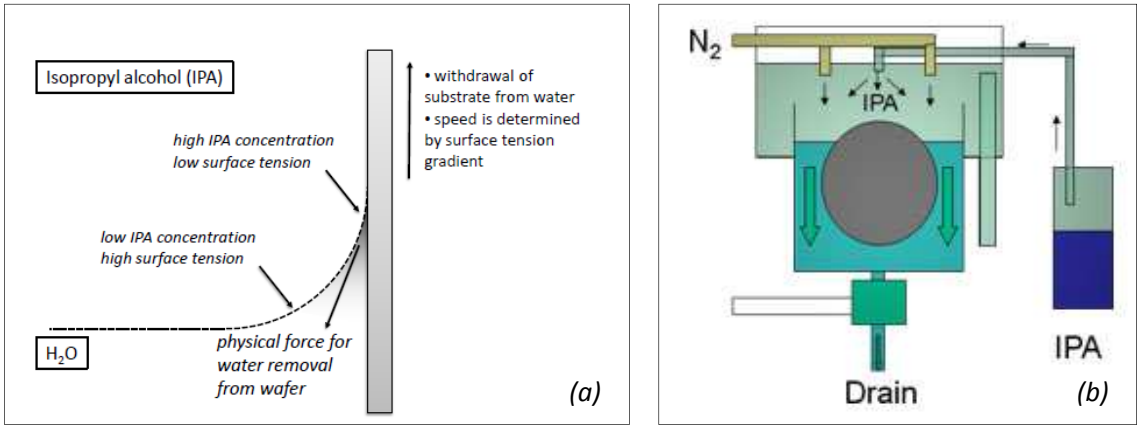

Figure 3.2: The Marangoni Effect as drying technique (a): It is based on surface tension gradient forces after the deposition of IPA on the wet surface. (b) Cross section of a dryer tool (*Accudry* by IMTEC, [4] and Appendix C). All the mentioned parts are well visible: IPA tank and the noozles to create the N_2 - alcoholic vapor inside the chamber, the water tank containing the wafers and the drain system to decrease the water level. The tension gradient forces make the surface out of water dry: the process ends when the water tank is empty.

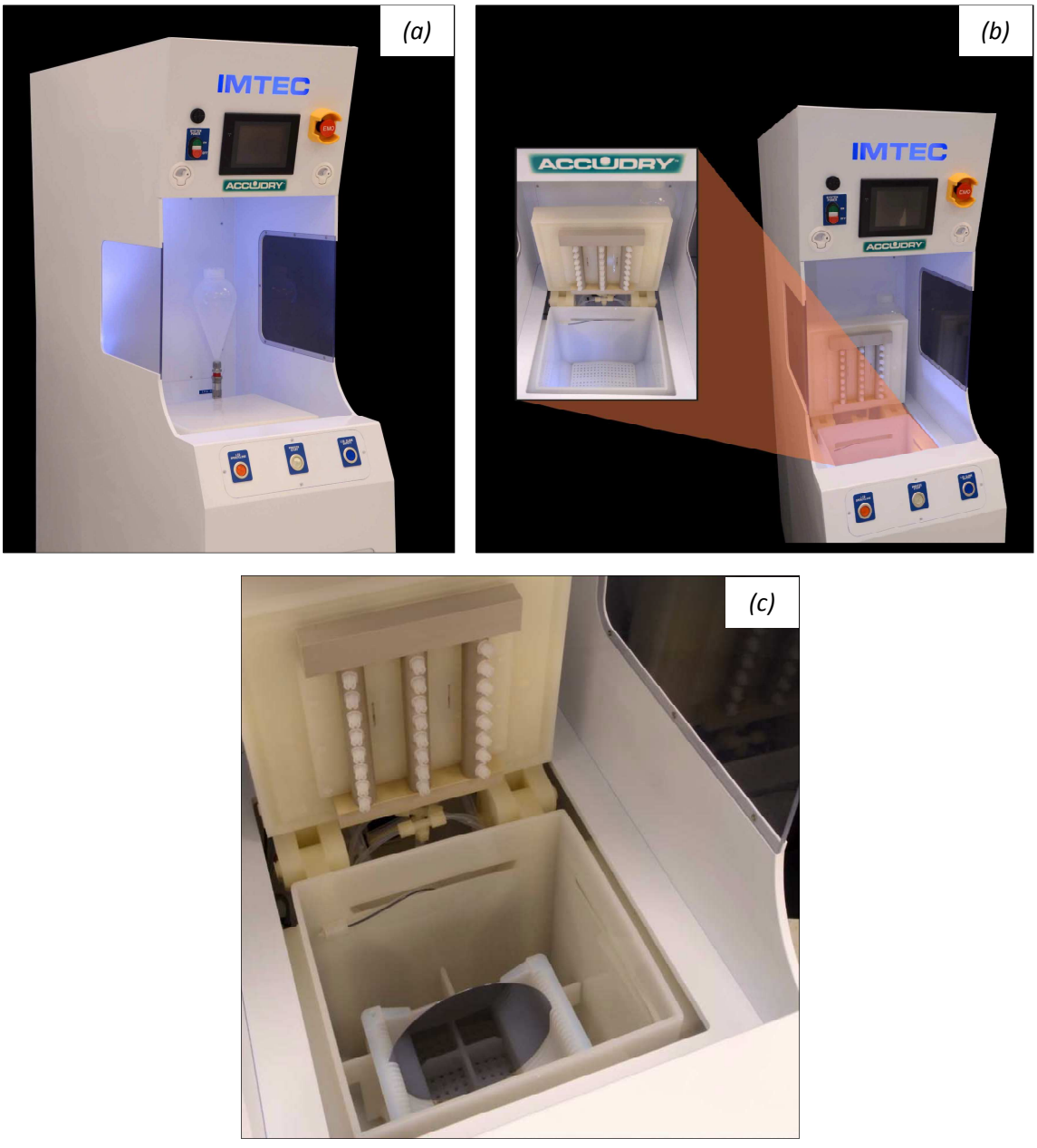

Figure 3.3: *Accudry*, dryer tool based on Marangoni effect, by *IMTEC* [4] (a). This tool can rapidly displace water from the wafer surface (inside the process chamber, (b)) until it is completely dry. This yields substrates that are watermark-free with extremely lowparticle counts and zero feature damage. The drying process is controlled by the level of water in the tank (c): it signifies no moving parts or mechanical stress on the wafers, meaning no costly breakage or damage.

3.3 Deposition Techniques

The deposition of dielectric layer is a crucial point: the quality of the material deposited and the interface region on the wafer play a fundamental role. Some of the most common deposition techniques are discussed below, focusing on the ones used in the samples preparation (Thermal ALD and PECVD).

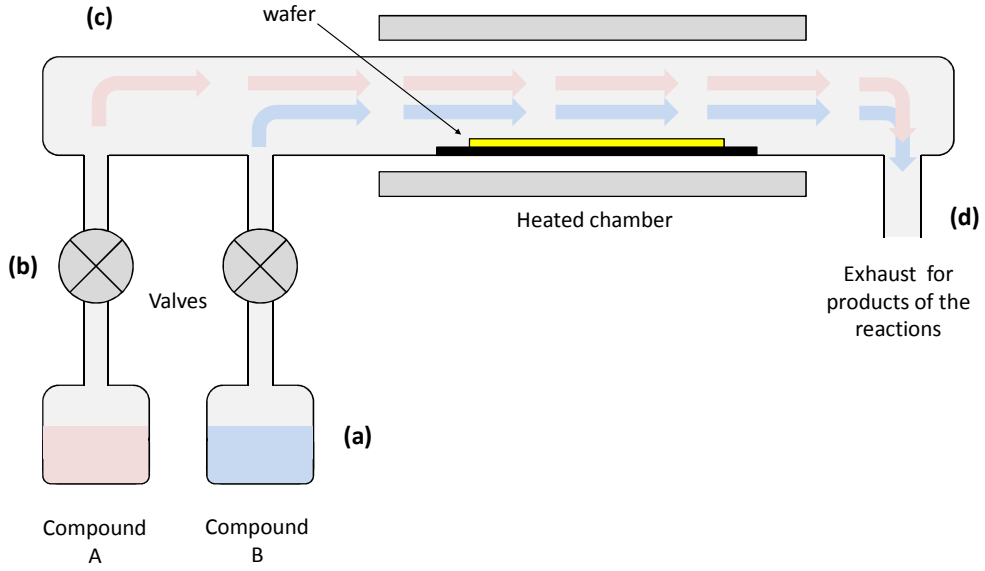

Figure 3.4: Cross section of a typical ALD reactor. The picture illustrates and distinguishes the main components of this deposition tool.

3.3.1 Thermal ALD

Thermal ALD is an accurate technique, because of its excellent uniformity and growth control allowing conformal films to be deposited on very high aspect ratio structures. ALD is based on sequential, self-limiting surface chemical reactions involving two vapor phase reactive chemical species, typically a metal-organic precursor and a co-reactant.

During the process, the wafer to coat is inside a high-vacuum chamber, where the reactants are injected continuously at pressure and temperature controlled. The film grows at a rate determined by the velocity of the reactions involved and by the time needed to bring reactants at the surface: both these parameters are linked to the pressure and the temperature. This means the desired thickness depends mostly on the velocity and on the time of the deposition. However, controlling the velocity of the reactions is not easy and limitations in resolution of the thickness can occur.
Very thin layers can be grown by Thermal ALD, depositing one single atomic layer per time: this signifies the thickness of the film can be determined by the number of cycles performed.

3.3.1.1 ALD Reactor

Fig. 3.4 depicts the typical cross section of an ALD reactor:

a) Two separated chambers contain liquid state precursors at controlled temperature.

b) Both chambers are separated from the reaction chamber by high pressure valves. The valves have also to guarantee high velocity opening/closing and they are controlled electronically.

c) The wafer to coat is set at the center of the deposition chamber on a support sometimes heated. The volume of the chamber is as small as possible in order to reduce the time to make the vacuum and the gas quantity needed.

d) Gases are injected and expelled through a pump system to maximize the velocity and the efficiency of the process. To maintain a steady pressure during the process it is necessary that the pumps injecting gases and pumps expelling this work at the same rate: an automatic control system is needed to keep constant the gas flow.

The samples investigated in this work have been built from wafers coated by *Savannah S200*, ALD reactor of Nanotech Cambridge ([5], Appendix D), Fig. 3.5.

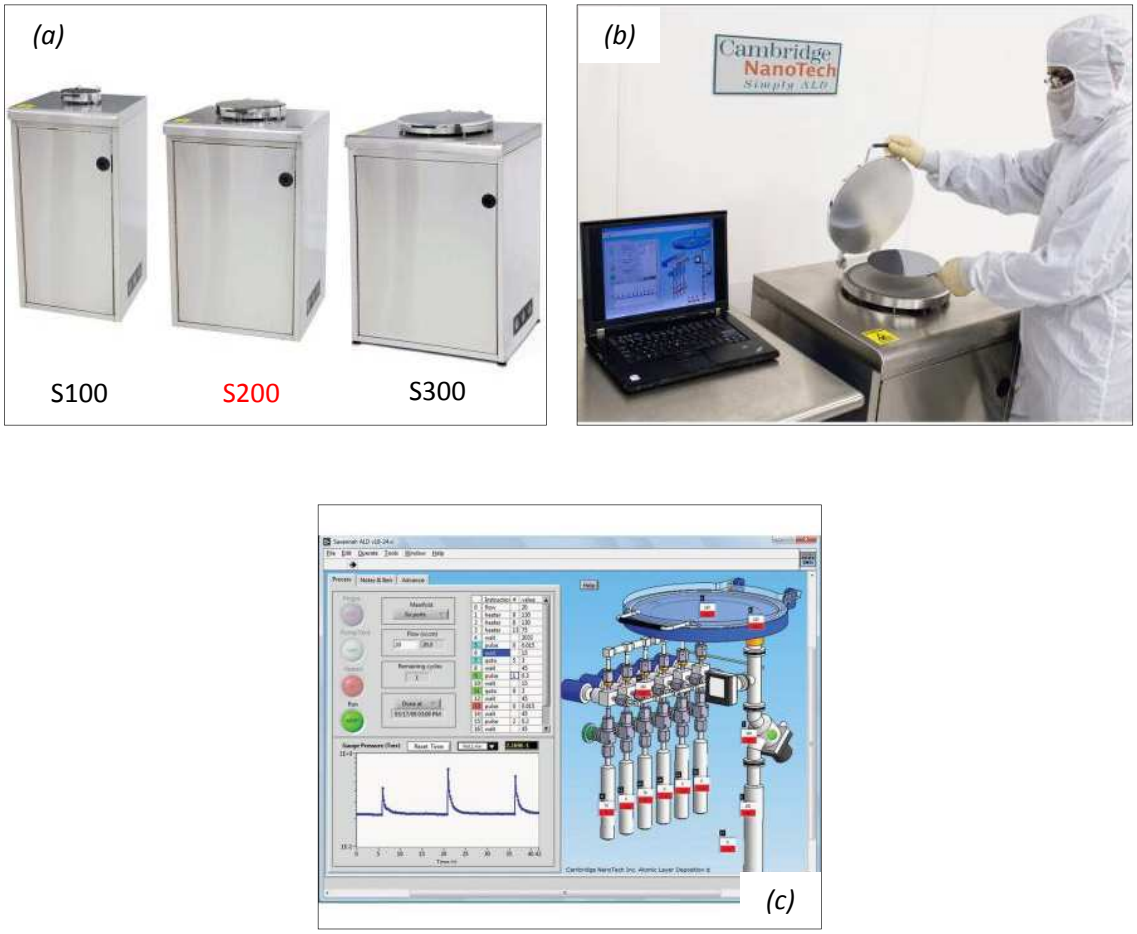

Figure 3.5: *Cambridge NanoTech* is considered one of the leading providers of ALD solutions for research and industry worldwide [5]. The tool used comes from the *Savannah Series* (a): S200 allows the deposition on wafers with a a diameter up to 200 mm. The tool is compact (b) and the complete control of all key system parameters is easily achievable through the dedicated Graphical User Interface (c).

After describing the ALD reactor, the chemical reactions involved during the deposition of Aluminum Oxide (Al_2O_3) are here illustrated. The process takes place over a p-type Silicon substrate, with OH- groups on its surface after the cleaning process (*Hydrophilic* surface). Each deposition cycle can be divided into four different steps (Fig. 3.6) [6].

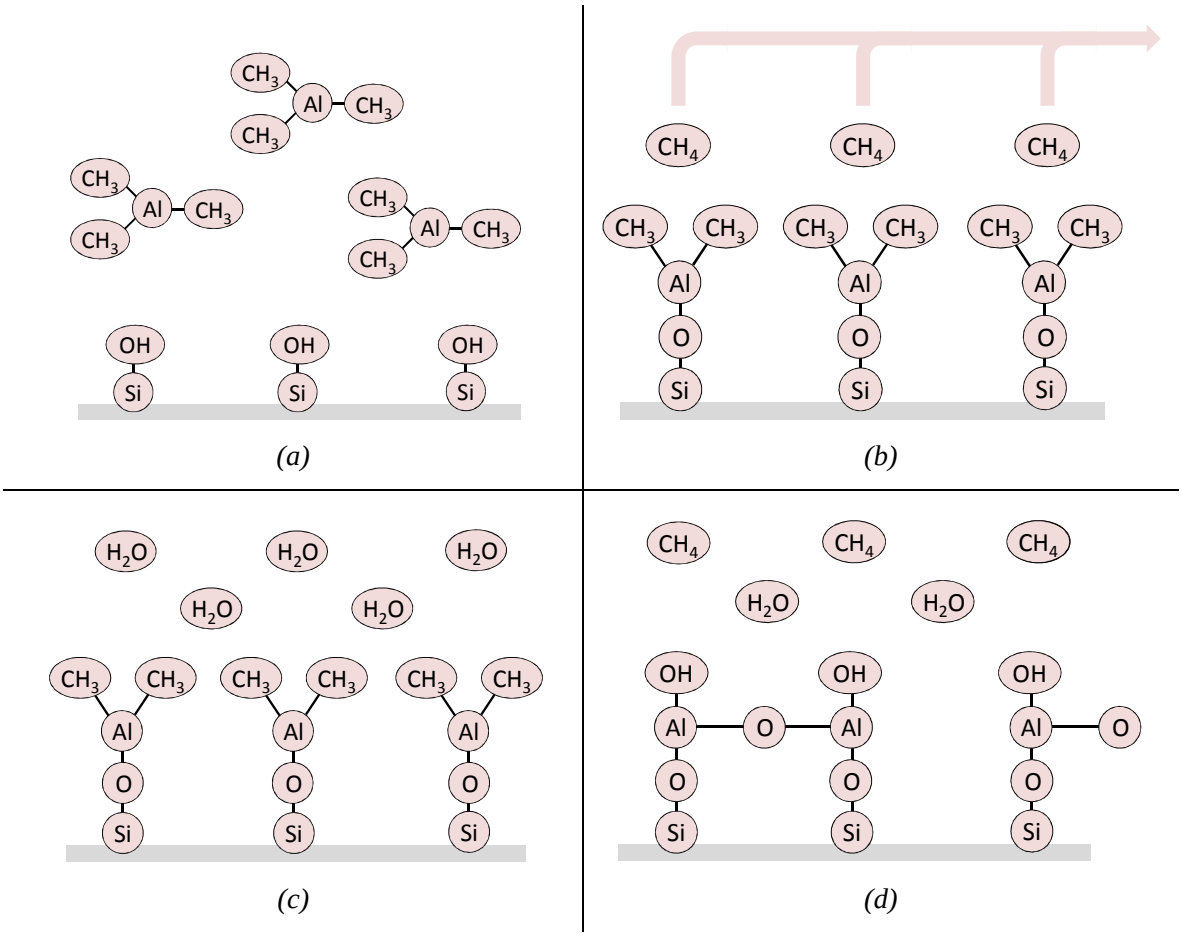

Figure 3.6: (a) to (d) Schematic diagram of one cycle of atomic layer deposition of Al_2O_3 using sequential saturation exposures of TMA and H_2O, separated by inert gas purging steps. After the full cycle, the starting hydroxylated surface is reproduced, allowing the cycle to be repeated to build up a coating with near monolayer precision.

a) Injection of TrimethylAluminum, $Al(CH_3)_3$, in the reaction chamber.

b) A reaction involving TrimethylAluminum and the surface of the wafer takes place: the precursor chemically reacts and bonds to the surface without fully decomposing. The precursor also changes the dominant surface termination, leaving the surface ready to react with the co-reactant.

$$AlOH + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2 + CH_4$$

The reaction is self-limited by the disponibility of free OH- groups on the surface: when all the OH- groups have been saturated, the reaction stops, also if there is still exceeding gas inside the chamber. The remaining vapor products are pumped or pushed out of the deposition zone using inert gas flow.

c) Water vapor (H_2O) is injected in the reactor. A reaction with CH_3-groups starts:

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$$

Also in this step the reaction is self limited by the presence of CH_3-groups.

d) The vapor products are flushed out. The starting hydroxylated surface is reproduced and the “ALD cycle” can start over again.

The characteristic feature of an ALD process is that the half-reactions are self-limiting. Once the precursor has reacted with sites prepared during the previous co-reactant exposure, the surface reaction stops: that is, the surface sites prepared by the precursor reaction are reactive to the co-reactant, but not the precursor itself. This means that during steady-state growth, the precursor will typically deposit at most only one monolayer during each half-reaction cycle, even when the surface is exposed to the reactant species for long periods of time. One must ensure that enough precursor is delivered to achieve full

saturation, otherwise, growth will be non-ideal and non-uniform [7]. Therefore, each reaction Al_2O_3 cycle adds a given amount of material to the surface, referred to as the growth per cycle (GPC), which depends on the deposition temperature. Figure 3.7 shows the Al_2O_3 layer thickness on hydroxylated Silicon as a function of the amount of ALD cycles for deposition temperatures of 150, 200 or 250 °C. This graph clearly shows the self-limiting facet of ALD: for hydroxylated Silicon samples a GPC of 1.1 to 1.4 Å per cycle, depending on the deposition temperature, is calculated. In this work, ALD Al_2O_3 films have been deposited at 200 °C.

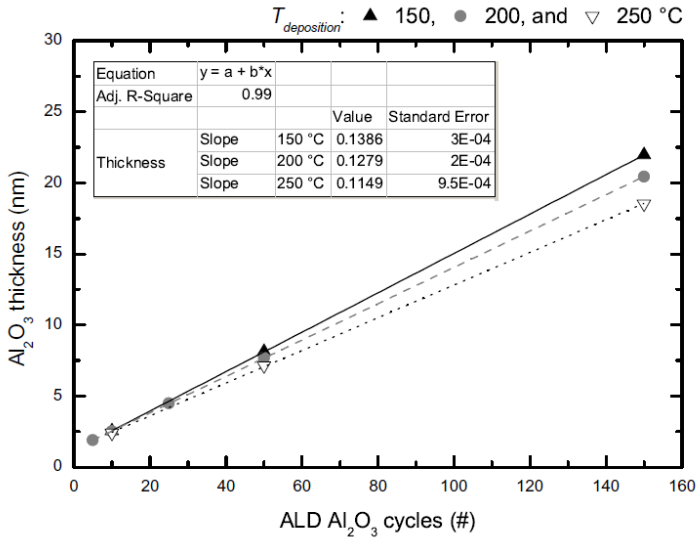

Figure 3.7: Thickness of Al_2O_3 layers deposited as described above on hydroxylated Silicon wafers as a function of the number of ALD cycles for deposition temperatures of 150, 200 or 250 °C. Also the linear fits are shown. From its slope the growth per cycle can be calculated.

The process described above is a typical temporal ALD cycle since the samples are placed in a reaction chamber and the half cycles are separated by purge steps. Uniform ultrathin layers can be manufactured using temporal ALD, however, conventional time-resolved ALD is limited by a low deposition rate (~ 0.2 nm min^{-1}).

Instead of temporal separation, the ultra-fast ALD concept is based on the spatial separation of the half-reaction: such reactor has separate zones exposing the precursor one by one to a

substrate that floats underneath the reactor [8]. Fig. 3.8 displays a schematic overview of a reactor for the spatial resolved ALD deposition of Al_2O_3 [9].

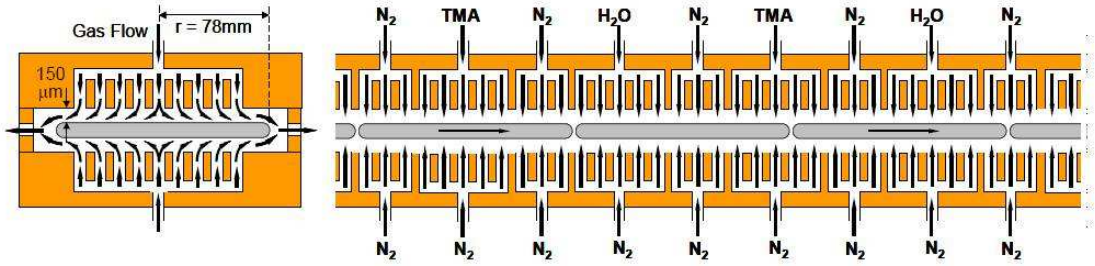

Figure 3.8: Schematic overview of the Levitrack® ALD system [10] for ultra-fast deposition of Al_2O_3 passivation layers (Appendix E).

It can be seen that the wafers pass regions in which the front of the wafer surface is successively exposed to $Al(CH_3)_3$ (TMA), N_2, H_2O and N_2. In this arrangement the flow of precursors is constant in time, being the wafer the only object in the track that moves. In this way very high deposition rates are achieved, while maintaining the required high film quality. This concept allows (i) single side, (ii) in-line, and (iii) atmospheric pressure deposition, and (iv) a deposition speed well above 1 nm/s. Commercial ultra-fast setups with a throughput of 1 wafer min^{-1} (10 nm) are available, meeting the cost-efficiency and throughput demands of the PV market [10, 11].

3.3.1.2 Temperature and Pressure choice

The pressure inside the reactor has to be chose carefully in order to keep the precursors steady and volatile at the deposition temperature. To achieve ALD growth, the temperature must be held within 200-400 ˚C: out of this *ALD window* the reaction doesn't work properly (Fig. 3.9).

a) If the temperature is too low (< 200 ˚C), condensation of the gas on the substrate could be observed, and more than one layer per cycle will be grown (1). In this

temperature condition it is also possible an incomplete reaction, because of its slowness (2): less than one layer per cycle will be obtained in this way.

b) If the temperature is too high (> 400 ˚C), it is possible that the bonding ready formed will be broken: this means the evaporation of the deposed layer. In this way (3), the grown layer looks uncompleted (less than 1 layer per cycle). Another unexpected effect can occur at too high temperatures (4): the gas molecules are broken starting off undesirable reactions with the substrate (more than one layer grown per cycle).

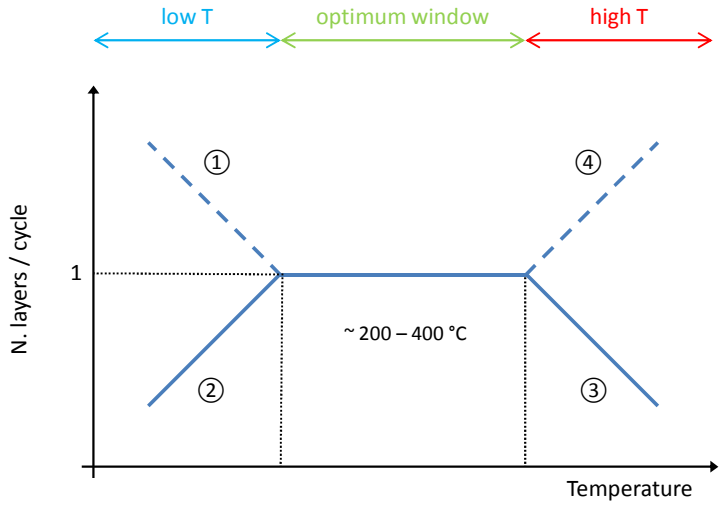

Figure 3.9: Schematic representation of the *ALD window*. To achieve ALD growth, the temperature must be held low enough so that the precursor does not decompose during surface adsorption, but the temperature must be high enough to thermally activate the reaction and/or avoid surface condensation.

3.3.2 PEALD

In the Plasma-Enhanced ALD (PEALD) process, an oxygen plasma is ignited above the substrate, generating oxygen radicals which effectively react with the methyl groups and

the Aluminium at the surface, as illustrated in Fig. 3.9. All the considerations below have been obtained by a *remote* approach: an inductively coupled plasma (ICP) source is used, which means that the oxygen plasma is not in direct contact with the Silicon wafer during Al_2O_3 deposition. This type of remote-plasma deposition technique is known to create almost no plasma damage at the surface, and is hence well suited for an excellent Silicon surface passivation [12].

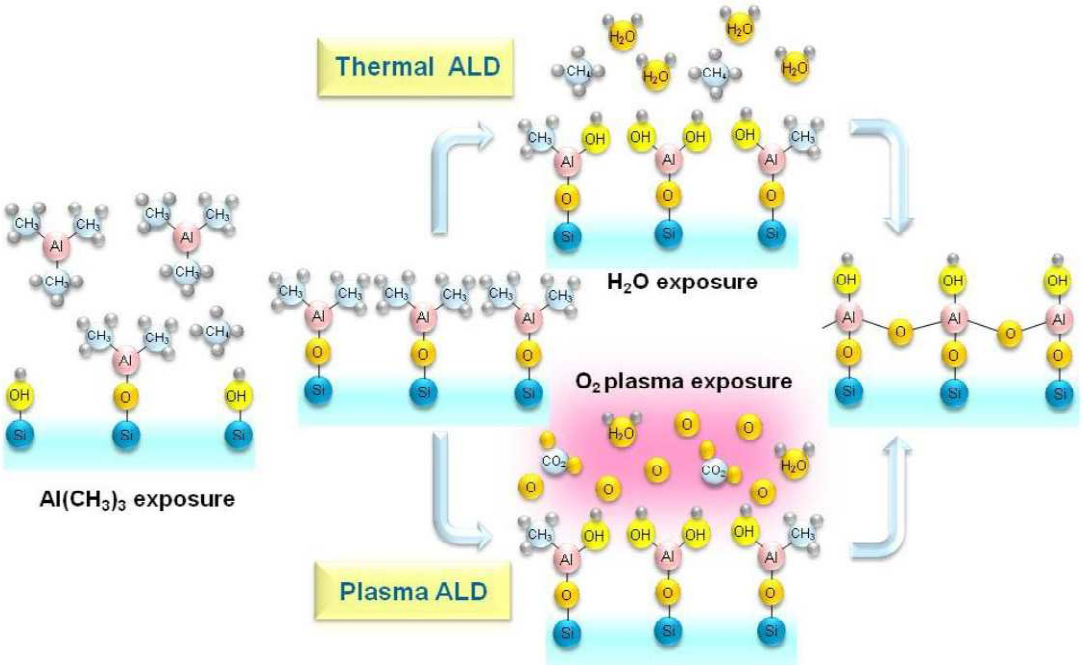

Figure 3.10: Schematic of one cycle of a thermal and a plasma-assisted ALD process. Each cycle consists of two half-steps: first, the TrimethylAluminum (TMA) molecules attach to the hydroxyl groups attached to the Silicon surface; second, the molecules are oxidized by H_2O (thermal ALD) or an O_2 plasma (plasma ALD).

As expected, the thickness increases linearly with the number of completed cycles also for the remote plasma ALD process. J. L. Hemmel et al. have observed (using the *Oxford Instruments FlexAL* reactor, Fig. 3.11.a and Appendix F) from in situ thickness measurements, that the growth per cycle is higher for remote plasma ALD than for thermal

ALD (in the same Pressure/Temperature conditions): i.e., 1.2 Å/cycle for remote plasma ALD and 1.0 Å/cycle for thermal ALD (Fig. 3.11.b) [13]. Thus, the mass densities of the remote plasma ALD films are slightly higher than those of the thermally deposited films. Also, plasma ALD yields fair material properties at low deposition temperatures (substrate heated at a temperature below 100°C) at a relatively high growth per cycle and short cycle times [13].

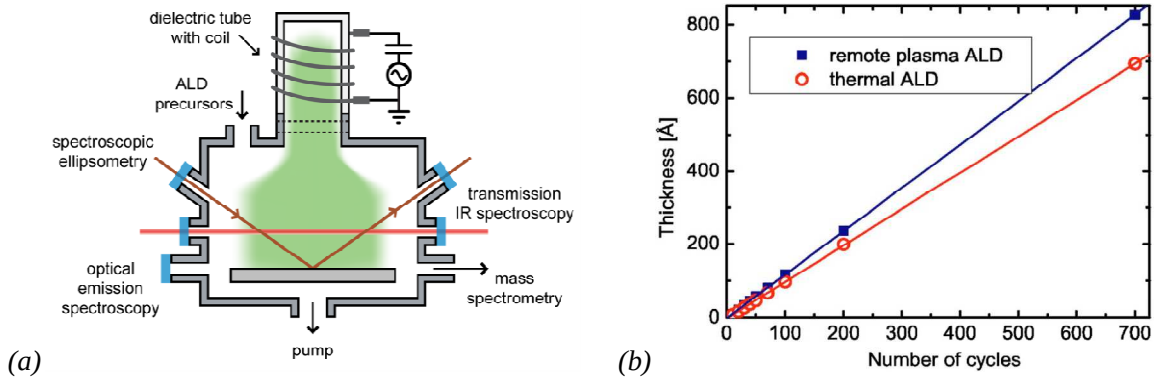

Figure 3.11: (a) Schematic cross section of a (remote) Plasma Enhanced ALD reactor (*Oxford Instruments FlexAL* reactor) [14]. The picture also depicts the different diagnostics implemented in situ (ellipsometer, spectroscopy) to obtain fundamental understanding of the reaction mechanism of plasma-assisted ALD. (b) Al_2O_3 film thickness as a function of the number of cycles for both remote plasma ALD and thermal ALD [13]. The thickness has been determined by in situ spectroscopic ellipsometry and the growth per cycle was obtained from the linear fits shown in the figure. The substrate temperature was 200°C.

3.3.3 CVD

Chemical Vapor Deposition (CVD) is a deposition technique allowing the formation of a high quality/purity film through the reaction on one or more gas species on the surface of a substrate. Usually the material to coat is kept on a base inside the deposition chamber and it is exposed to one or more gases containing the material to deposit. Precursors react with the

surface forming a solid layer and some volatile products later on are expelled from the chamber. Depending on the material grown and the reactions involved, typical process temperatures are within 300-900 °C.

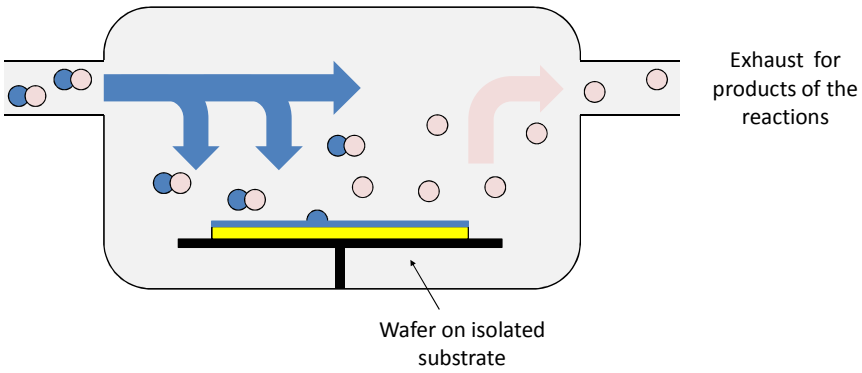

Figure 3.12: Cross section of a typical CVD tool. The picture depicts the most relevant phases during the deposition process.

CVD follows three main steps (Fig 3.11):

- The material to be deposited is put inside the reactor throw one or two gaseous compounds.
- Precursors react with the surface forming a thin and uniform film, plus eventual volatile residuals.
- Residual materials are expelled out from the reactor, otherwise a residual layer would form blocking the reaction.

The growth rate depends on two factors: the *velocity of the reaction* and the *concentration of precursor gases* near the surface. Optimizing the process, the temperature is a fundamental parameter. In general it can be observed (Fig. 3.13) that increasing this parameter (1), an higher level of thermal agitation of the molecules is obtained and the transport of the reactants is improved. However, if the temperature is too low (2), a new limitation linked to the reaction efficiency occurs. In general, depending on the

temperature, the bottle neck will be the slowest process: the deposition takes place at high temperatures, a good draining system for unreacted products is required.

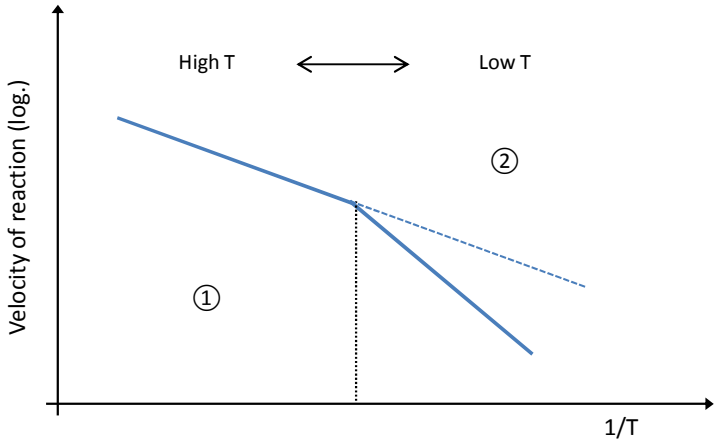

Figure 3.13: The graph illustrates the limit of the velocity of reaction (logarithmic scale) as function of the temperature. The growth process depends on two factors: (1) the transport of the reactants, more relevant at high temperatures and (2) the surface velocity of reaction, significant at low temperatures.

3.3.4 PECVD

Plasma Enhanced CVD is a variant of CVD using a ionized gas (plasma) in order to improve the reactivity of the precursors and then the efficiency of the process. The plasma is typically generated with a RF electromagnetic field (order of MHz) between two plan electrodes. The substrate (typically OH- terminated) is set on the lower electrode and heated at relatively low temperatures (100-400 °C).

The reagent gases are injected from the top and the reagent species are activated by the plasma between the electrodes. The residual gases and the products of the reactions are removed from the bottom. The pressure in the chamber can vary from few microbar up to few millibar (Fig. 3.13).

Since the electric field is orthogonal to the wafer, the surface of the substrate is subjected to an intense ionic bombardment. Ions can be either *reactive* (interacting with the substrate

forming the film) or *inert*. If the second case occurs, the bombardment with inert ions will increase the temperature at the surface making the reaction more efficient. In both cases, the growth of the film occurs mostly on the horizontal surfaces of the wafer, rather than on the vertical ones.

PECVD is already frequently used in industrial Silicon PV to deposit a front surface antireflection coating of PECVD hydrogenated amorphous Silicon Nitride (a-SiNx:H). Hence, PECVD has already been demonstrated as a low-cost and industrially relevant technique. The most frequently used in-line PECVD Al_2O_3 layer has been developed by *Roth&Rau* (Appendix G). The microwave-remote plasma is created by 2.45 GHz microwave pulses, which are introduced to the reaction chamber via a linear antenna. The chamber pressure and deposition temperature are in the range of respectively 0.15 mbar and 300 °C. As reactants, a mixture of nitrous oxide (N_2O), TMA and argon (Ar) is applied [15, 16].

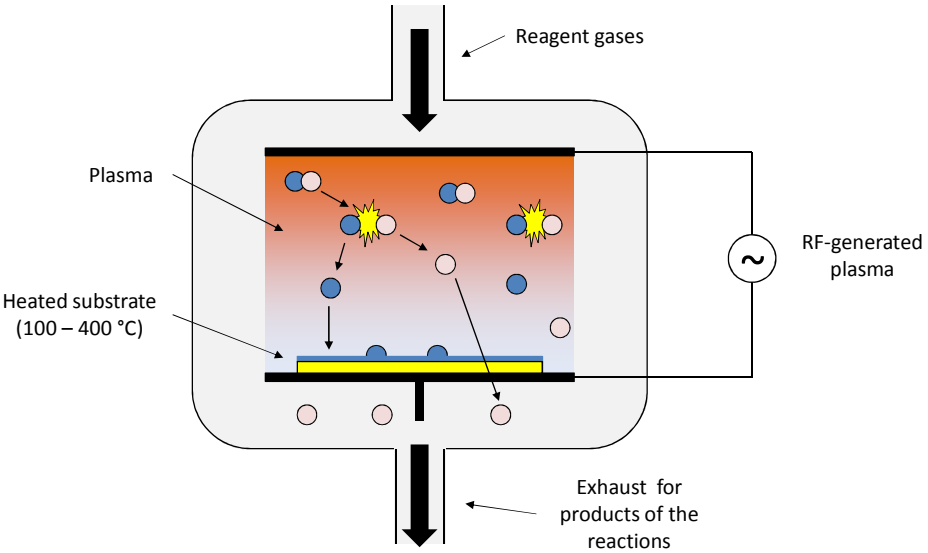

Figure 3.13: Cross section of a typical PECVD tool. The picture depicts the most relevant phases during the deposition process.

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Chapter 4

Silicon Surface Passivation by ALD Al_2O_3

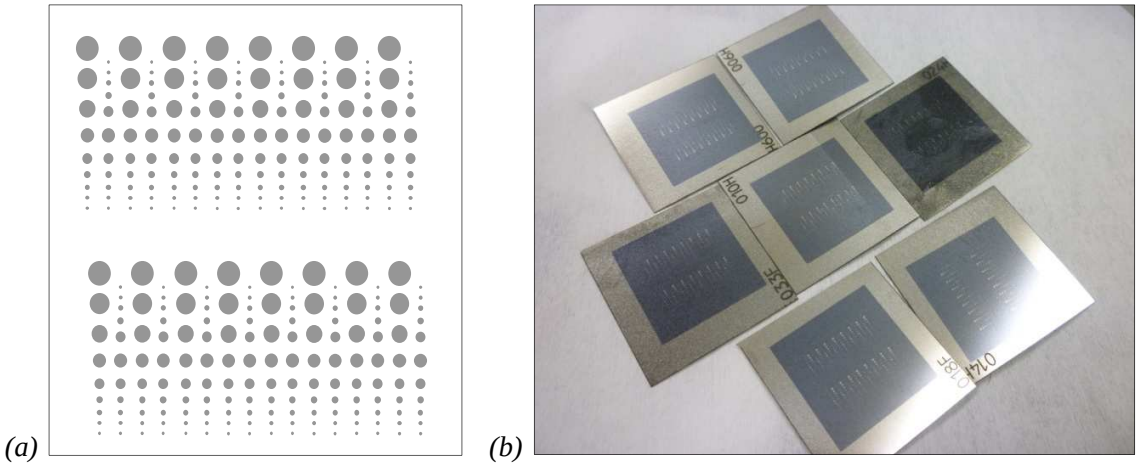
Last chapters have to be considered as a presentation of the concept of Silicon surface passivation and of the most common techniques to deposit a passivation layer. The aim of this chapter is to describe and investigate in detail the mechanisms behind passivation, focusing their correlation with the post-deposition annealing. Passivation is mostly based on *chemical passivation*, related to the defect density at the Silicon/dielectric interface and *field effect passivatio*n, which deals with the formation of a negative fixed charge density within the dielectric.

4.1 Electrical Characterization

In general, three main methods can be used to analyze passivation effects: (i) corona charging (CC) [1,2], (ii) second harmonic generation (SHG) [3] and (iii) capacitance-voltage (CV) measurements. CV measurements show an advantage compared with respect to the others methods mentioned above: they provide also an estimation of D_{it} (beyond fixed charge) and they are performed on metalized surfaces. CV method looks therefore better suited for studying complex structures where passivating dielectric is covered by a metal layer (e.g Passivated Emitter and Rear Cell, PERC). In addition CV measurements

are quite simple to be taken compared with other methods and seem perfect for a quick control of cells under test or in a real production line. However, this choice has to consider that the presence of a metallization on a dielectric layer affects its electrical properties [4], and hence influences both the field effect and chemical passivation estimated [5].

4.1.1 Samples Preparation



(a) *(b)*

Figure 4.1: (a) Shadow mask used during Platinum deposition. Dots from 35 µm up to 500 µ. The size of these dots has been found quite irregular: because of the technique itself, not a perfect contact between the mask and the layer below is possible yielding not the dot sizes expected (variations up to 25 % than the expected value have been observed). (b) Samples after all the preparation steps, ready for electrical measurements.

Al_2O_3 (5, 10, 15, 20 nm) is deposited on one side on SDR p-type CZ Silicon using ALD (T_{dep} = 200 °C). Prior to deposition, Silicon surfaces were H- or OH- terminated. On the rear side, Aluminum has been deposited by sputtering PVD with a thickness of about ± 2 µm. After Aluminium deposition, the samples have been annealed at T_{ann} = 300, 500, 800 ˚C in N_2 environment for a time interval of 20 min, to investigate the effect of the temperature on the passivation properties. On the side coated with high-k material,

Platinum has been evaporated through a shadow mask (Fig. 4.1) by e-beam evaporation in order to define dot-shaped Schottky contacts with a diameter of 35-500 µm.

The Platinum contacts deposited can have not a regular, round and precise shape: since the shadow-mask sputtering technique is not the most precise, the shape of the metallization can be irregular and also well different compared to the expected dimension (variations also of 25% than the nominal value have been observed). Dot area is a crucial parameter, being used to convert the results per unit area and affecting the C_{ox} value in CV curves.
In order to get an estimation of these areas, a Java-based image processing program has been used: *ImageJ* [6].

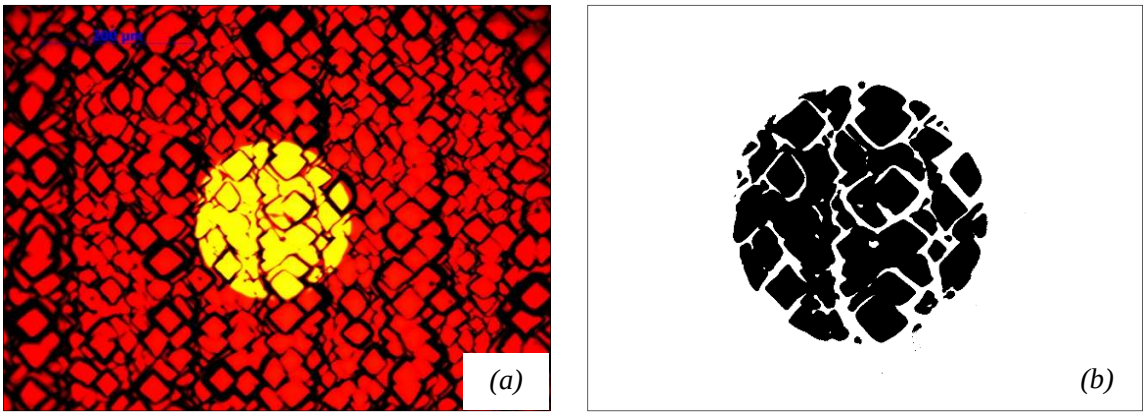


Figure 4.2: 200 µm diameter metal dot seen by optical microscope. (a) represents the picture taken by microscope after modifying its contrast. (b) The binary image of the observed dot.

An adequate number of dots in a sample has been observed by optical microscopy. Each picture have been modified to get an high contrast between the metal dot and the surrounding area (Fig. 4.2a). Finally, this has been converted to a binary image, representing the shape of the considered dot (Fig. 4.2b). This procedure have been repeated five times for each sample: the dot area used is the average of these five values.
Fig. 4.2 refers to the Silicon sample (hydrophobic) coated by 10 nm of ALD Al_2O_3. The diameter is close to the nominal value 200 µm, but the shape of the dot looks irregular and also damaged by the measuring needle. The analysis of Fig. 4.2 by ImageJ has provided an area of $\approx 26{,}2 \times 10^3$ µm^2 (~ 16% lower than the nominal value $31{,}4 \times 10^3$ µm^2).

4.1.2 Electrical Measurement Setup

Figure 4.3: Setup for electrical measurements. All the main parts are well visible: (a) the *PA300* electrical probe-station, (b) the *HP4284A* precision LCR-meter and (c) the computer workspace to control the measure operations.

Electrical measurements have been taken using an electric *Probe-Station* (PA300, Fig.4.3a and Appendix H) and a precision *LCR-meter* (HP4284A, Fig.4.3b and Appendix I), both remote controlled by a computer workspace, Fig. 4.3c. The measurements have been taken at high frequency (100 kHz) at room temperature (≈ 26˚C). This setup allows to have at the same time CV and GV measurements.

All the capacitances and the conductances here mentioned are considered divided for the surface area of the MOS interface.

4.1.3 Solar Grade Material and Related Issues

This work aims to provide an electrical characterization of samples made of solar grade material, to obtain results relevant also for the real industrial production. This not ideality brings along various issues, mainly the *scattering properties* and the *leakage effect*.

4.1.3.1 Scattering Properties

Being made of not ideal material, the samples investigated have shown different CV curves just changing the contact dot measured. This means a limited level of uniformity of the dielectric layer and a great effort has been put in trying to understand the "global" characteristics of each layer.

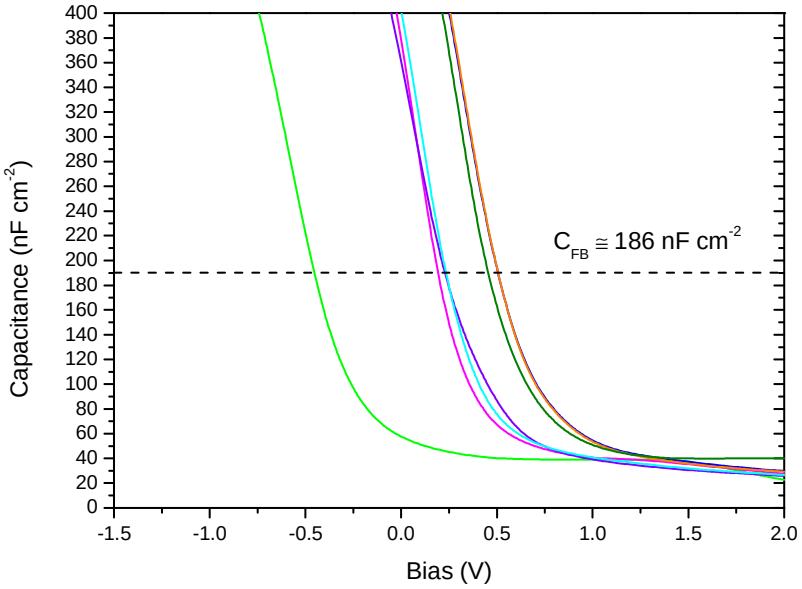


Figure 4.4: CV (per unit area, cm^{-2}) curves taken from different dots (formally 200 µm diameter) on 10 nm Al_2O_3 (deposited on hydrophobic Silicon surface) sample annealed at 500 ˚C. The black dashed line corresponds to the flat band capacitance. V_{FB} differences of also 1 V can be observed preventing us to consider just one random curve. An average approach has been followed: V_{FB} considered comes from the average of extracted values.

Several CV curves (and GV as well) have been obtained measuring the same sample from different dots: the parameter of interest has then been obtained from an average evaluation of the values extracted from the curves. E.g. Fig. 4.4 depicts an average evaluation of flat band voltages (V_{FB}). As it will be explained in paragraph 4.1.5, V_{FB} is the key parameter in the extraction of the fixed charge density in the dielectric. The picture clearly illustrates how these differences can be also not negligible and the average approach has been considered the only way to estimate reasonable V_{FB} values.
The average approach is not the only way to face the scattering issue: one can also analyse the samples considering the best cases or the worst cases. However, this approach has been considered less adequate for this work.

A trustworthy average approach needs several measurements. Each sample has been measured (from different random dots) five times at least. For each measured CV curve, V_{FB} has been calculated and finally an average value has been estimated. Because of the great number of V_{FB} calculations required, an automatic tool to extract them has been used (Fig. 4.5), *Hauser's Cvc software* [7]. V_{FB} voltages extracted come from the forward direction (inversion to accumulation) at 100 kHz of each capacitance curve.

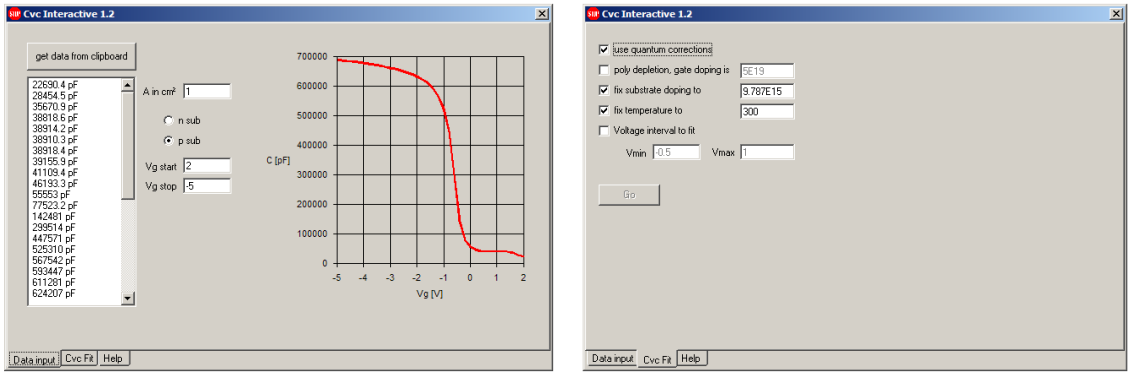


Figure 4.5: Because of the high number of curves to analyze, an automatic software has been used, *Hauser's Cvc software.* It provides an automatic and quick evaluation of all the parameters extractable from a capacitance curve (among which V_{FB}). Some parameters have to be set (e.g. the type of substrate and its doping level).

4.1.3.2 Loss Angle

Beyond the above mentioned scattering effect, another relevant issue to face has been the *leakage effect*: many measurements performed looked trustworthy, but actually they weren't because of high electrical dissipation inside the dielectric material. Leakage effects have been faced using a *Loss Angle* approach.

The loss angle (δ) is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy when an AC signal is applied [8]. The MOS stack measured is considered as a not ideal capacitor, with a loss component (G_p) as depicted in Fig. 4.6a.

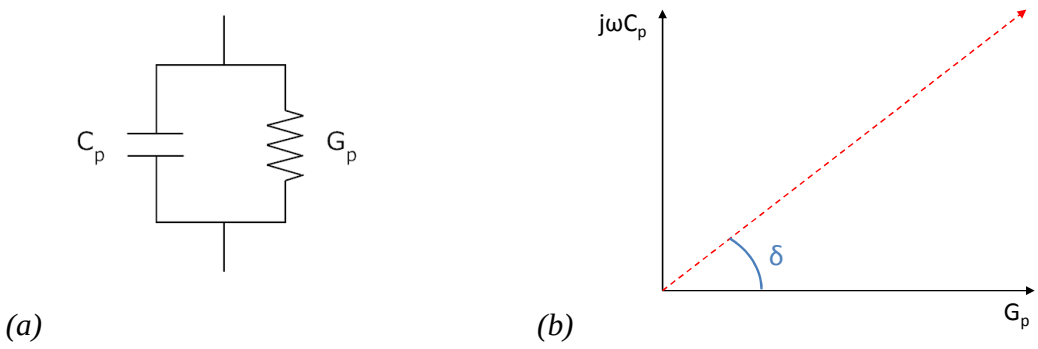


Figure 4.6: MOS systems investigated have been modeled as real capacitors (a), with a resistive loss contribute. The admittance can be represented on the complex plane (b), highlighting the resistive (loss) and reactive contributions. Loss angle (δ) is comprised between the conductance axis and the admittance vector (red vector): the higher δ is (up to 90°), the lower G_p is and loss mechanism can be considered negligible, making the measurement trustworthy.

The admittance of this parallel contains also a loss contribute: the lower G_p is, the lower the loss mechanism is and δ is close to 90°. Considering Fig. 4.6a, the ideal condition corresponds to a pure capacity yielding to the maximum δ value (90°). Since electrical CV and GV measurements performed provide both C_p and G_p, δ can be always estimated and its value quantifies how much leakage affects the measurement.

Observing Fig. 4.6a, loss angle has been defined as in Equation 4.1 [8].

$$Loss\ Angle\ \delta = \left[arctan\left(\frac{2\pi f C_m}{G_m}\right)\right]\frac{180}{\pi} \tag{4.1}$$

considering values above 80° as reliable (especially in depletion region).

4.2 Field Effect Passivation

Thin film solar cells have a relevant drawback: the carrier surface recombination. A way to reduce this disadvantage is the as known *field effect passivation*: an electric field is formed through the dielectric layer, with a polarity adequate to reduce the effective recombination velocity of the free electrons on the Silicon surface [9].
After the deposition of a dielectric layer on the Silicon surface, it has been observed the formation of a SiO_2 thin layer between Silicon and dielectric. Several works in literature reports the growth of this layer [10] and it has been demonstrated that a positive charge density is trapped at the Silicon/SiO_2 interface (e.g. Rothschild et al. measured a positive fixed charge density close to 5×10^{10} cm^{-2} [11]). This means that an adequate electric field can be achieved with a negative fixed charge density within the dielectric material deposited and at the dielectric/SiO_2 interface (typically ~10^{12} cm^{-2} [9]). Hence, it is evident how the SiO_2 layer plays a central role in surface passivation: in paragraph 4.2 it will be explained how important it is also for the *chemical passivation*.

4.2.1 Distribution of the Charges

An effective technique and methodology for the estimation of fixed charge components in high-k (as Al_2O_3) films by varying both the interfacial SiO_2 and high-k dielectric

thicknesses is well explained in [11,12]. The schematic of the gate stack, with its constituent charge layers in a simple model, is shown in Fig. 4.7. Oxide charge at the metal gate (electrode) / high-k interface is assumed to be included in the work function as a constant contribution that therefore cannot be estimated in thickness-series experiments. As a first order approximation, the areal charge densities (at the Silicon / SiO_2 and SiO_2 / hi-k interfaces, $Q_{Si/SiO2}$ or $Q_{SiO2/hi-k}$, respectively) are assumed to be located on a plane of infinitesimal thickness at the interface in question, whereas the bulk or volumetric charge density ρ_{hi-k} is assumed to be uniformly distributed throughout the entire layer. The volumetric bulk charge in the SiO_2 layer is negligible, consistent with the fact that thermally grown SiO_2 typically contains a significantly small amount of positive charges [13,14,15].

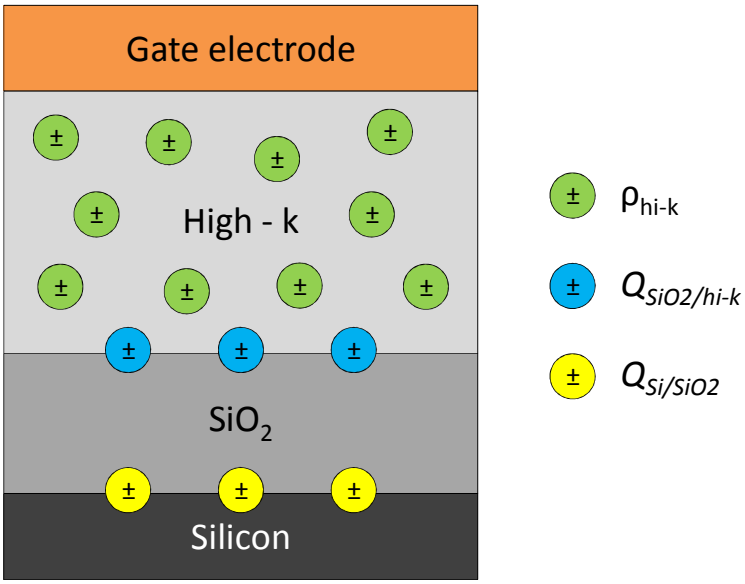


Figure 4.7: Schematic model of the charge locations used in the extraction of fixed charge. The charge at the gate (electrode)/high-k interface is assumed to be included in the work function and to be constant in a thickness-series experiment. Also he volumetric bulk charge in the SiO_2 layer is negligible.

4.2.2 Fixed Charge Density Investigation

4.2.2.1 Extraction of the Necessary Parameters

The fixed charge density present in the Al_2O_3 layer (deposited at 200 ˚C on hydrophobic Silicon surface) has been calculated comparing similar samples with different passivation layer thicknesses (5, 10, 15 and 20 nm) and plotting V_{FB} as a function of the *equivalent oxide thickness* (*EOT*) value [11]. Thicker layers (15, 20 nm) are expected to be more problematic to characterize due to their typical blistering problems, as widely explained in literature, e.g. [16]. However, they are necessary, providing an adequate number of points to extract a reasonable workfunction value for the MOS stack.
The dielectric charge has been calculated according to Equation 4.2.

$$Q_{ox} = C_{ox}\,(\varphi_{ms} - V_{FB}) \tag{4.2}$$

with C_{ox} the oxide capacitance and φ_{ms} the difference between Silicon and metal (Platinum, on the samples under test) workfunctions [17].

The evaluation of φ_{ms} is a crucial point (it will affect both the sign and the value of the estimated charges) and it has been calculated by plotting V_{FB} as a function of respective thicknesses. The intercept with ordinate axis is φ_{ms} according to Equation 4.3 [17].

$$V_{FB} = \varphi_{ms} - \frac{Q_f t_{ox}}{k_{ox} - \varepsilon_0} \tag{4.3}$$

with the oxide thickness $t_{ox} = 0$ and $k_{ox} \approx 8$. The value of the oxide dielectric costant (Al_2O_3 in this case) is explained and calculated below, being a quite variable parameter. In literature, it has not a fixed value but a range: its precise value has to be determined case by case.

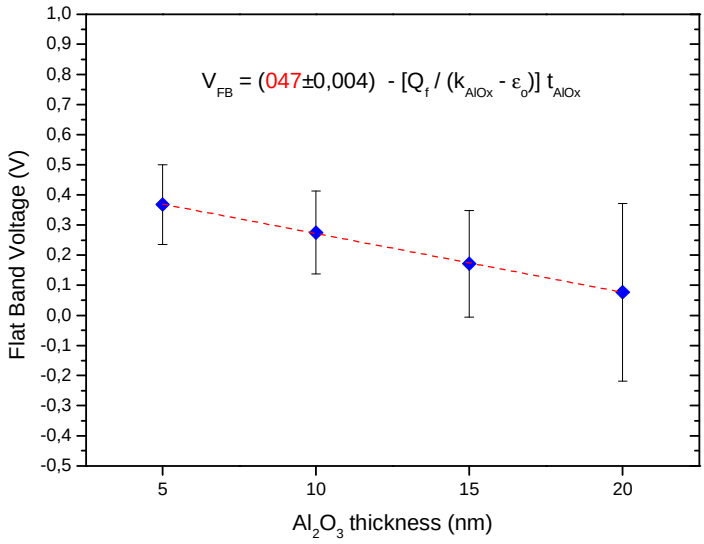


Figure 4.8: Average V_{FB} in function of their corresponding Al_2O_3 passivation layer thicknesses (200 ˚C ALD on hydrophobic Silicon surfaces). The four points show a good alignment and the intercepts with ordinate axis provides a reasonable estimation of the workfunction of the system (0.47± 0.004 eV in this case).

The workfunction value of the system has been extracted from as-deposited samples. The above mentioned blistering effect affecting the thicker layers (15, 20 nm) is even more relevant increasing the anneal temperature [16]: this means that the different layers can be hardly comparable after annealing.

This way, for as-deposited Al_2O_3 samples, a φ_{ms} of about 0.47 ± 0.004 eV has been estimated. This value is coherent with the involved workfunctions: (i) Silicon within 4.6-4.85 eV, (ii) Platinum within 5.12-5.93 eV [18].

k_{ox} above mentioned has been considered of ≈ 8. This is a typical value for Al_2O_3, within the expected range (7-11, from literature [19]). However, because of its variability it has been verified from the investigated samples. *EOT* has been plotted in function of Al_2O_3 thicknesses: the slope of the line obtained is the value of k_{ox}. In fact *EOT* can be defined as in Equation 4.4[19]. k_{SiO_2} and $k_{Al_2O_3}$ are constants and the last one (*EOT*) can be obtained from Equation 4.5 [19].

$$EOT = \left(\frac{k_{SiO_2}}{k_{Al_2O_3}}\right) t_{Al_2O_3} \tag{4.4}$$

$$EOT = \frac{(k_{SiO_2}\ \varepsilon_0)}{C_{ox}} \tag{4.5}$$

Each Al_2O_3 thickness has its own C_{ox} value that provides a corresponding *EOT*. Then k_{AlOx} has been calculated after putting *EOT* values in a graph and observing the slope of the line (Fig. 4.9).

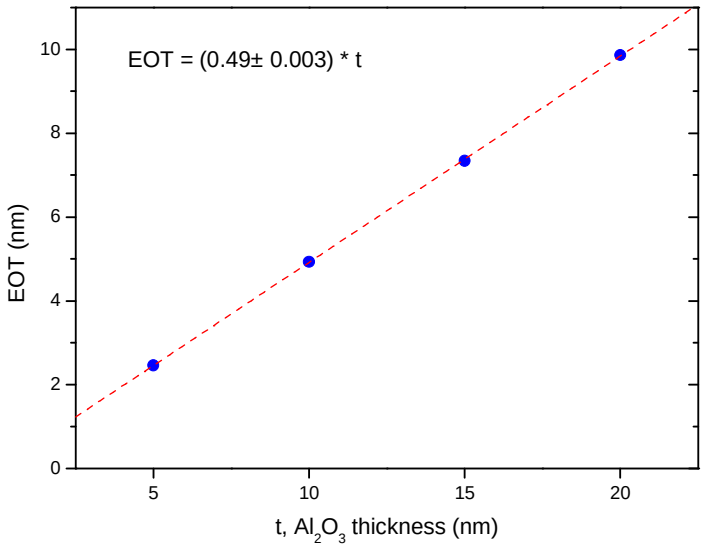


Figure 4.9: k_{ox} has been estimated moving from the samples under test. Its value comes from the slope of the red-dashed tendency line.

The considered value of k_{SiO_2} constant is 3.9 from literature [18]. After few calculations the value estimated is:

$$k_{SiO_2} \approx 8$$

The value looks reasonable being within the expected range (7-11, from literature: e.g. [19]).

4.2.2.2 Fixed Charge Density Calculation

In a CV curve, φ_{ms} is equal to V_{FB} when no fixed charge is in the system under investigation, therefore every shifting of V_{FB} with respect to φ_{ms} gives an estimation of Q_f. Fig. 4.10 below, depicts this shifting of the capacitance curves increasing the post-deposition annealing temperature: the plots move more and more to the positive voltages meaning the formation of a negative charge.

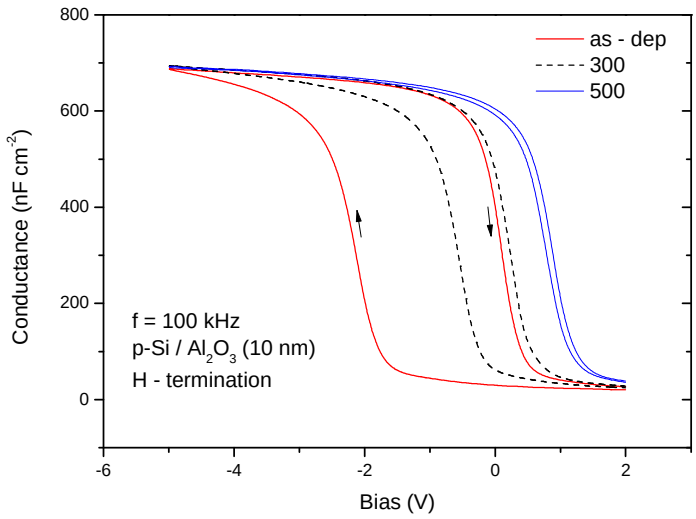
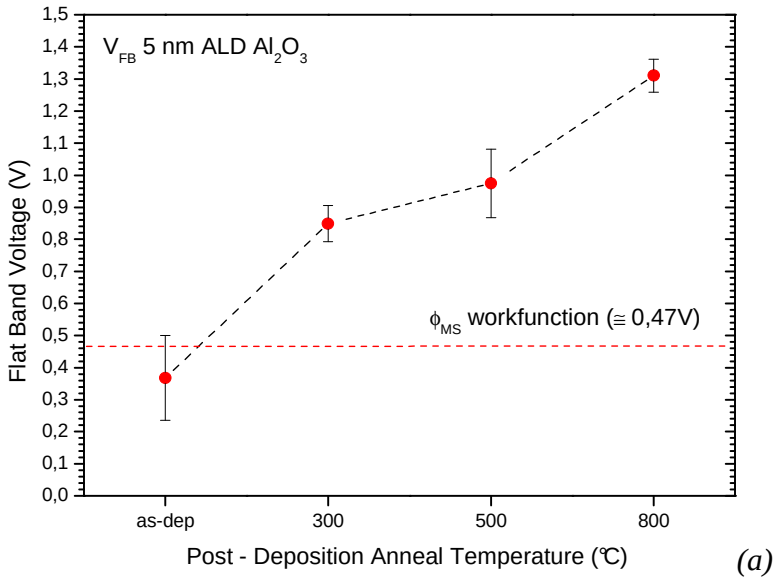
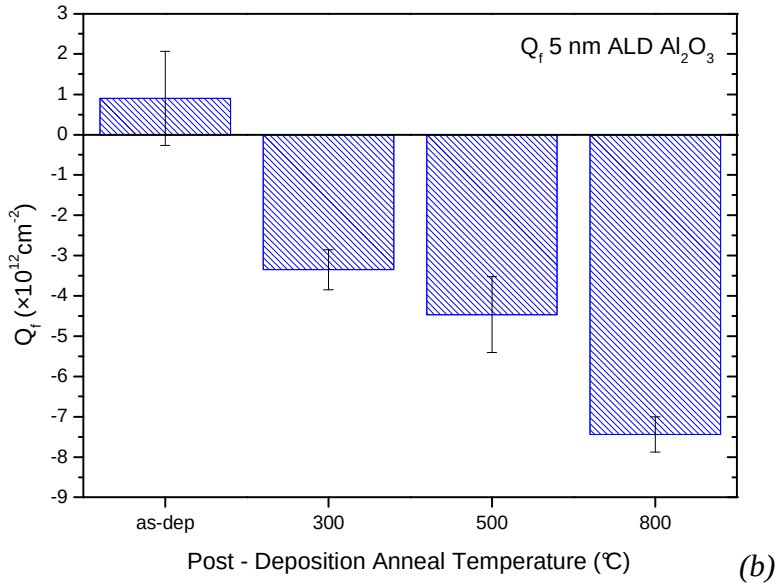


Figure 4.10: CV curves corresponding to 10 nm Al_2O_3 passivated hydrophobic surface. Each curve corresponds to a different post-deposition thermal treatment (as-dep, 300 ˚C and 500 ˚C). The picture clearly depicts a shift of the curves toward positive voltages (meaning the formation of a negative Q_f), increasing anneal temperature. Each shift corresponds to a variation of Q_f in high-k material and can be used to get an estimation of this charge. The wide voltage range chosen (from -5V up to +2V) has allowed also an estimation of mobile charges, as illustrated in paragraph 4.1.3.4.

Fig. 4.11, 4.12, 4.13, 4.14 clearly explain this point, showing the average V_{FB} values as a function of post-deposition annealing temperature for p-type CZ Silicon surfaces (hydrophobic) passivated by 5 to 20 nm of ALD Al_2O_3. The value of estimated φ_{ms} is indicated by a red dashed reference line. The shifting of V_{FB} corresponds to the formation of a fixed charge density in the dielectric: all the values are collected in Tab. 4.1.



(a)



(b)

Figure 4.11: The graphs refer to 5 nm ALD Al_2O_3 on hydrophobic Silicon surface. Average V_{FB} values as a function of anneal temperature (a): each shift with respect of workfunction level corresponds to formation of charge density (b). Data points above reference red dashed line correspond to negative fixed charge density present in the Al_2O_3 layer.

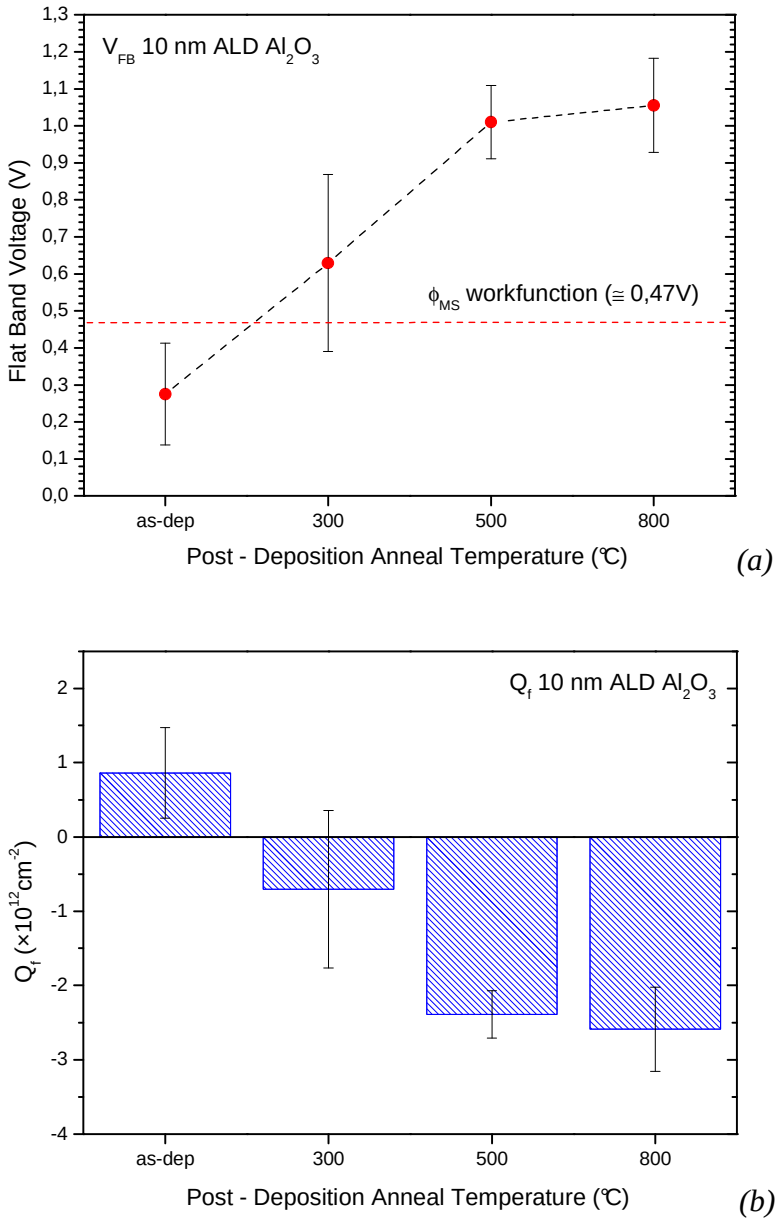
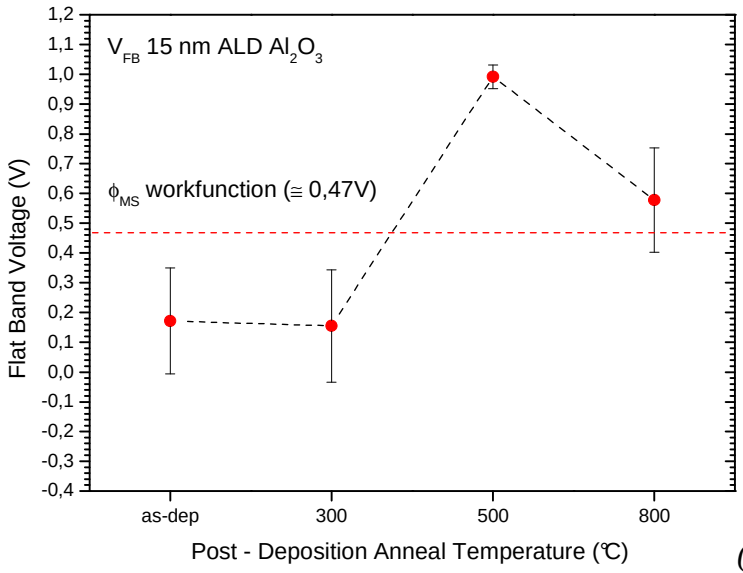
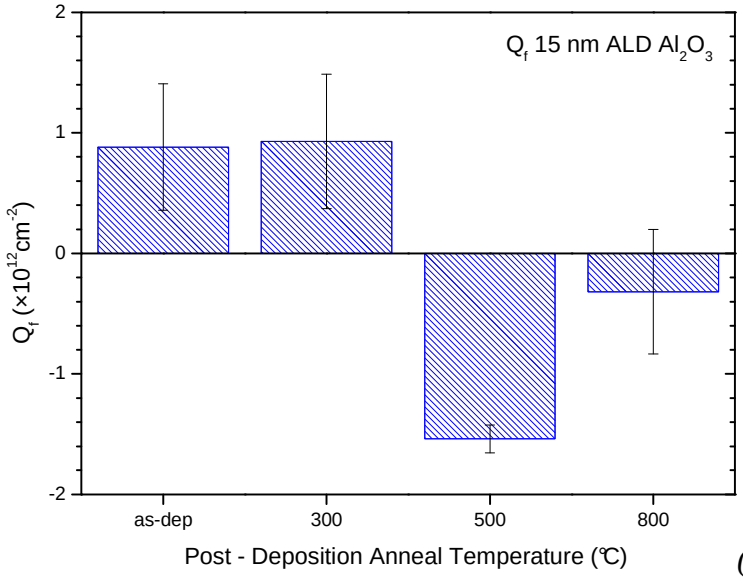


Figure 4.12: The graphs refer to 10 nm ALD Al_2O_3 on hydrophobic Silicon surface. Average V_{FB} values as a function of anneal temperature (a): each shift with respect of workfunction level corresponds to formation of charge density (b). Data points above reference red dashed line correspond to negative fixed charge density present in the Al_2O_3 layer.



(a)



(b)

Figure 4.13: The graphs refer to 15 nm ALD Al_2O_3 on hydrophobic Silicon surface. Average V_{FB} values as a function of anneal temperature (a): each shift with respect of workfunction level corresponds to formation of charge density (b). Data points above reference red dashed line correspond to negative fixed charge density present in the Al_2O_3 layer.

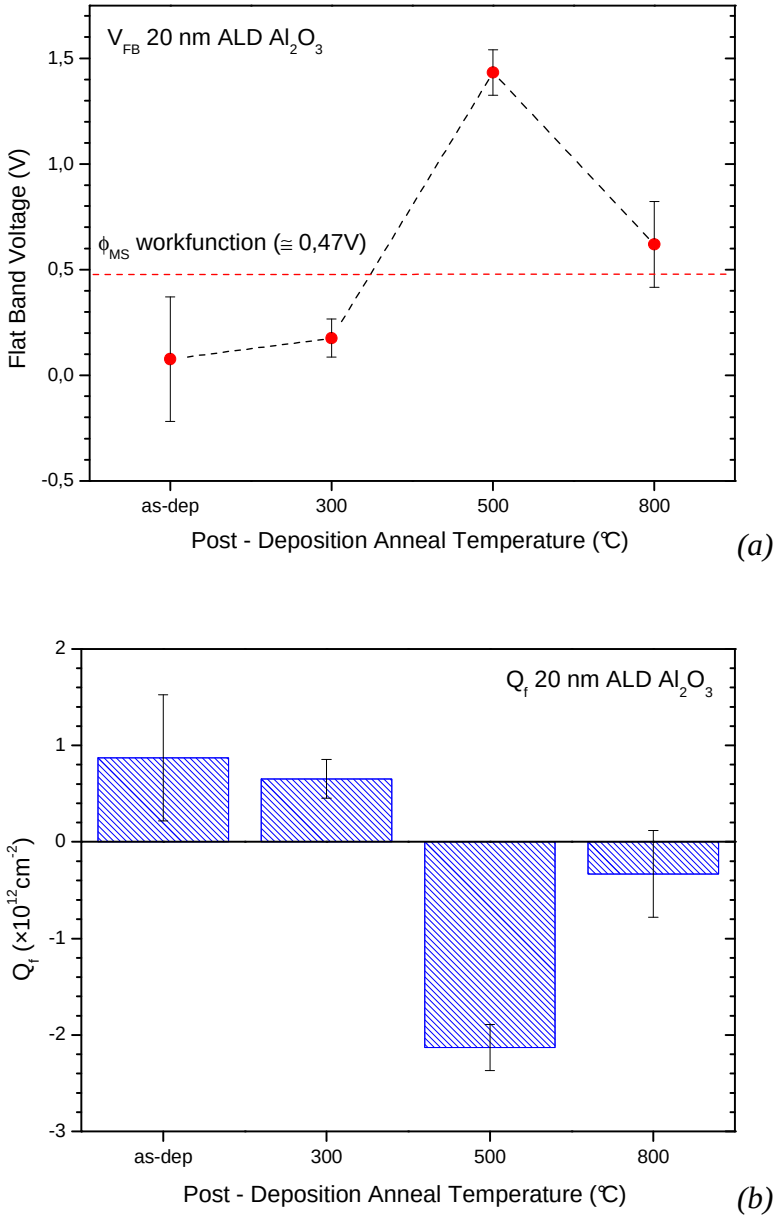


Figure 4.14: The graphs refer to 20 nm ALD Al_2O_3 on hydrophobic Silicon surface. Average V_{FB} values as a function of anneal temperature (a): each shift with respect of workfunction level corresponds to formation of charge density (b). Data points above reference red dashed line correspond to negative fixed charge density present in the Al_2O_3 layer.

This pictures clearly show a shift in V_{FB} as a function of annealing temperature. Even more, at higher annealing temperatures the V_{FB} becomes > φ_{ms}, which signifies the formation of a fixed negative charge density in the Al_2O_3 film. This negative fixed charge density inside the dielectric yields the creation of an electrical field at the Silicon surface preventing free carrier surface recombination.

Table 4.1: Fixed charge density (Q_f) for p-type CZ Silicon samples (hydrophobic) coated by 5, 10, 15, 20 nm of ALD Al_2O_3.

	Q_f ($\times 10^{12}$ cm^{-2})			
T_{ann} (˚C)	*5 (nm)*	*10 (nm)*	*15 (nm)*	*20 (nm)*
as-dep	0.903	0.863	0.881	0.870
300	-3.352	-0.705	0.929	0.651
500	-4.464	-2.390	-1.539	-2.129
800	-7.441	-2.590	-0.317	-0.332

Referring to 10 nm sample as example, a positive fixed charge density of $Q_f = (8.63 \pm 6.08) \times 10^{11}$ cm^{-2} is reported for as-deposited Al_2O_3. After a post-deposition annealing at T_{ann} = 300 and 500 ˚C, negative fixed charge densities of respectively $Q_f = (-0.70 \pm 1.06) \times 10^{12}$ cm^{-2} and $(-2.39 \pm 0.32) \times 10^{12}$ cm^{-2} have been reported. After highest anneal temperature (800 ˚C), a negative fixed charge is still present: $(-2.59 \pm 0.56) \times 10^{12}$ cm^{-2}. It has been supposed the fixed negative charges are formed after the release of hydrogen, creating oxygen intestinal in the bulk Al_2O_3 [20].

4.2.2.3 Mobile Charge Density Calculation

Since CV curves have been performed considering a wide voltage range (from -5V up to +3V), the calculation of the mobile charge density (Q_m) is also possible. Mobile charge density estimation comes from CV curve observation: an enough wide bias range allows the formation of clearly visible counterclockwise hysteresis during the bias voltage sweep,

indicating the presence of mobile charge density in the dielectric [21]. Mobile charge density is not related to any passivation mechanism: it is provided to illustrate another information extractable from CV curves. Q_m is due primarily by the presence of ionic impurities like K^+, Na^+, Li^+ and H^+. In the case of Al_2O_3, H^+ is responsible for the mobile charge density, since K^+, Na^+ and Li^+ are not used during substrate cleaning or Al_2O_3 deposition. Q_m is quantified using Equation 4.6 [21].

$$Q_m = -\Delta V_{FB} C_{ox} \tag{4.6}$$

With ΔV_{FB} the difference in flat band voltage between the forward and the backward bias voltage sweep (hysteresis width) and C_{ox} the oxide capacity.

Table 4.2: Mobile charge density (Q_m) for p-type CZ Silicon samples (hydrophilic / hydrophobic) coated by 5, 10 nm of ALD Al_2O_3.

	Q_m ($\times 10^{12}$ cm^{-2})			
	hydrophobic		hydrophilic	
T_{ann} (˚C)	*5 (nm)*	*10 (nm)*	*5 (nm)*	*10 (nm)*
as-dep	15.985	10.135	9.688	1.929
300	9.782	4.191	7.558	0.767
500	7.657	0.531	2.666	0.116
800	3.558	0.839	1.787	0.300

The high Q_m for as-deposited Al_2O_3 on hydrophobic Silicon surfaces indicates the presence of a higher amount of H^+ compared to Al_2O_3 deposited on hydrophilic surfaces. It should be noted that the hydrophilic and hydrophobic sample were not measured simultaneously, and affected by degradation: the mobile charge density decreases over time. However, the difference is significant large to conclude that a higher amount of mobile charge density is reported for Al_2O_3 deposited on hydrophobic Silicon surfaces. During the thermal anneal, hydrogen is released from the dielectric, resulting in a decrease of mobile charge density. However, at T_{ann} = 800 ˚C, Q_m can increase, most probably due to the effusion of H from

the Silicon substrate. As reported by Beyer, a high effusion rate of H is observed at ≈ 625 ˚C, indicating a high breakage rate of Silicon-H bonds break, resulting in an increase of H^+ radicals, and therefore an increase of the mobile charge density in the Al_2O_3 layer [22] At higher annealing temperatures, the H^+ is outgassed from the Al_2O_3 and Q_m decreases again.

4.3 Chemical Passivation

Chemical passivation deals with the quality of the Silicon/insulator interface: a low interface trap density (D_{it}) means few recombination centers preventing free carriers from surface recombination. Low levels of D_{it} are essential for benefiting from the strong field effect induced by the high density of negative charges of the Al_2O_3 (field effect passivation), to have high lifetime values. The correlation with annealing temperature has been widely investigated.

4.3.1 D_{it} Theoretical Estimation (*Conductance Method*)

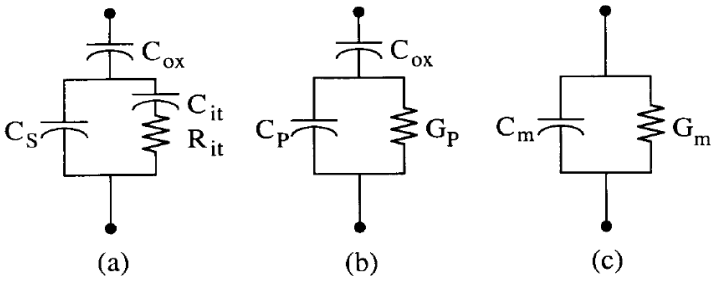


Figure 4.15: Equivalent electrical circuits of the MOS capacitors under test. Circuit (a) represents the most accurate model, including the main capacitances and loss contributions of the system: C_{ox} (Oxide capacitance), C_s (Semiconductor capacitance), C_{it} (Silicon/insulator interface capacitance) and the loss contribution R_{it}, representing the electrical loss at the interface. Models (b) and (c) are simplifications of the first one: their parameters come from the resolution of the equivalent circuits by solving series / parallel impedances.

D_{it} density in the MOS samples under test has been investigated following a technique similar to the well-known *Conductance Method* [24], proposed by Nicollian and Goetzberger in 1967. This is generally considered to be the most sensitive method to determine D_{it}. It is based on the measurement of the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. This conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of D_{it}. As mentioned before, all the capacitances and the conductances here mentioned are considered divided for the surface area of the interface.

The simplified equivalent circuit of an MOS capacitor is shown in Fig. 4.15a. It consists of the *oxide capacitance* (C_{ox}), the *semiconductor capacitance* (C_s) and the *interface trap capacitance* (C_{it}). The capture-emission of carriers by interface traps is a lossy process, represented by the resistance R_{it}. For D_{it} analysis, it is convenient to replace the circuit of Fig. 4.15a by that in Fig.4.15b, where C_p and G_p are given by Equations 4.7, 4.8 [24]:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{4.7}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \tag{4.8}$$

where $C_{it} = qD_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$ (the interface trap time constant) given by $\tau_{it} = [\upsilon_{th}\ \sigma_p\ N_A\ exp(-q\varphi_s / KT]^{-1}$. G_p is divided by ω to make Equation 4.8 symmetrical in $\omega\tau_{it}$. The interface trap capacitance is the parameter related to D_{it}: however, it is not possible a direct access to this capacitance value.

The conductance G_p is measured as a function of frequency and plotted as G_p/ω versus ω (at a fixed gate voltage). G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$ [25]. Hence we determine D_{it} from the maximum G_p/ω, and τ_{it} from ω at the peak conductance location on the ω-axis. Equation 4.9 reports this relevant result.

$$D_{it} = 2\frac{G_p}{q\omega} \tag{4.9}$$

LCR meters generally assume the device under test as a parallel C_m // G_m. A comparison between circuits of Fig. 4.15b and Fig. 4.15c gives G_p/ω in terms of the measured capacitance C_m, the Oxide capacitance C_{ox} and the measured conductance G_m (assuming series resistance negligible), as in Equation 4.10 [24, 25].

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox} - C_m)^2} \tag{4.10}$$

Equation 4.10 finally brings after some calculations to Equation 4.11 which can provide a D_{it} estimation by using the measured electrical parameters (C_m, G_m).

$$D_{it} = \frac{2}{qA}\frac{G_{m\,max}/\omega}{[(G_{m\,max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]} \tag{4.11}$$

4.3.2 Features and Disadvantages of Conductance Method

Every electrical measure has to be performed sweeping both frequency and voltage over a wide range obtaining several CV and GV measurement. Fig. 4.16 depicts a typical electric measure sweeping the gate voltage (-3V, +3V) at a fixed frequency value (100 kHz).

From Fig. 4.16, it is then possible to fix the gate voltage, find the corresponding G_p/ω and plot this as a function of the frequency, like Fig. 4.17 (the investigated sample is described in the caption). This picture clearly illustrate how these measures are also frequency depending: G_p/ω as a function of the frequency provides a peak at a frequency f_{peak}. This has been observed to vary changing the gate bias: Fig. 4.17 depicts $f_{peak} \approx 10^3$-10^4 Hz with a gate voltage = 1 V; f_{peak} shifts to ≈ 100 kHz with a bias = 1.5-2 V.

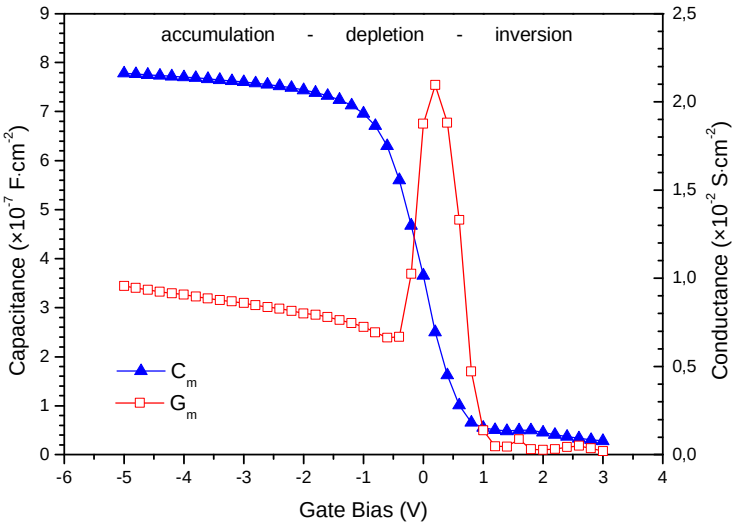


Figure 4.16: CV (blue dots) and GV (red dots) curves measured at 100 kHz on 10 nm ALD Al_2O_3 passivated Silicon (hydrophobic) substrate (after a post deposition annealing at 700 °C).

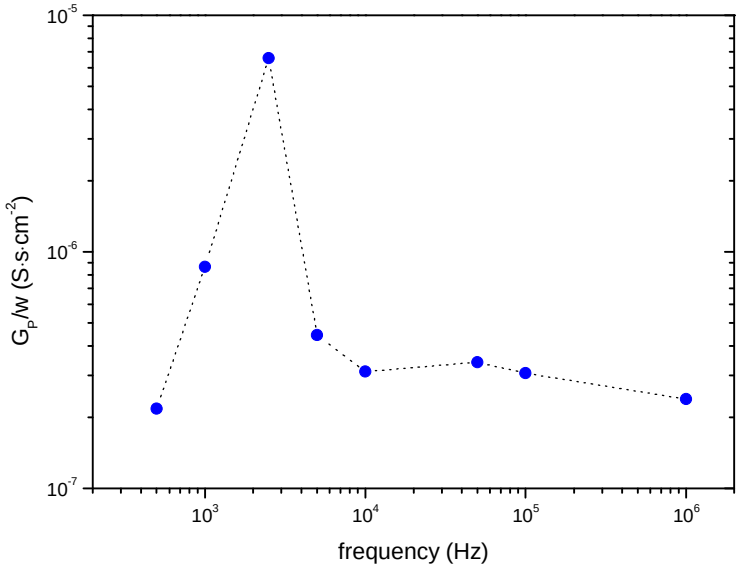


Figure 4.17: Multi-frequency analysis of a 10 nm Al_2O_3 (deposited by PECVD at 350 °C and after 500 °C post-deposition annealing) passivated Silicon substrate at a fixed gate voltage (1 V). Voltage value chosen has been estimated at boundary of depletion region. The peak obtained sweeping gate voltage frequency provides an estimation of D_{it} in the bandgap at the energy level corresponding to the gate bias applied. D_{it} value here estimated is 4.12×10^{13} eV^{-1} cm^{-2}.

The gate bias is an important parameter, being related to an energy level within the bandgap: it is then possible to get an estimation of D_{it} for every energy level. That is really interesting because D_{it} is not uniform within the bandgap, as shown in Fig. 4.18 [25].
This can be also observed in Fig. 4.17: at the edge of depletion region (gate voltage ≈ 1 V) $D_{it} \approx 4 \times 10^{13}$ eV^{-1} cm^{-2} has been calculated, two order of magnitude higher than the one estimated for the mid-gap, $D_{it} \approx 8 \times 10^{11}$ eV^{-1} cm^{-2} (this sample is well explained and investigated in the Chap. 5).

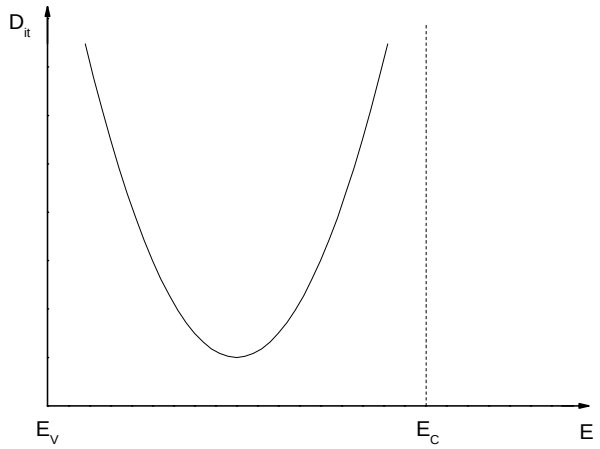


Figure 4.18: D_{it} is not uniform within the bandgap. At the boundaries of depletion region, D_{it} can reach values one or two orders of magnitude higher compared to mid-bandgap [26].

That is the complete and classical method known in literature as *Conductance Method*. However, it shows a main disadvantage: it needs several measurements to provide a D_{it} description. The interface trap description obtained is precise and trustworthy but it requires a lengthy analyze that may not fit with the quick testing process of many devices.

Since the aim of this work is not to provide an accurate method to measure of the passivation parameters, a slightly different method has been followed. Capacitance and conductance measurements have been obtained varying only the gate voltage at a fixed frequency value (100 kHz). This method is really close to the *one frequency method* developed in 1979 by W.A. Hill and C.C. Coleman [25].

4.3.3 One Frequency Conductance Method

From only one frequency measurement, a complete picture of the D_{it} across the entire bandgap cannot be obtained and formulas provided before have been slightly changed following the approach of Nicollian and Brews [27]: the D_{it} investigation is focused at the centre of the bandgap.

Equation 4.7 is still applicable but the conductance expressed by the Equation 4.8 is valid only for interface traps with a single energy level in the bandgap. Interface traps at the Al_2O_3/Silicon interface have been considered continuously distributed in energy throughout the semiconductor bandgap. Capture and emission occur primarily by traps located within a few kT/q above and below the Fermi level for such a continuum of interface traps. This results in a time constant dispersion and gives the normalized conductance as in Equation 4.12 [24]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \qquad (4.12)$$

The conductance is measured as a function of frequency and plotted as G_p/ω versus ω. This has a maximum at $\omega \approx 2 / \tau_{it}$ and $D_{it} = 2.5\ G_p / q\omega$ at that maximum.
Equation 4.13 describes the expression used in this work to find the interface trap density in terms of the measured maximum conductance [23]: Gp/ω can be substituted with Equation 4.10.

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \qquad (4.13)$$

Each sample has been characterized in this way. (i) A fixed frequency and a voltage range are chosen, then (ii) CV and GV curves are taken: being both electrical measurements, they can be kept with one step. (iii) The GV curve should present a peak as Fig. 4.13 (unless

leakage problems occur) and this value is considered in Equations 4.10 and 4.9, together with the corresponding capacitance: this provides a D_{it} estimation of the sample under test. Hence the frequency dependency has been neglected and the D_{it} estimated has to be referred to an energy level close to the middle of the bandgap, also because the voltage associated to the peak (within depletion region) corresponds to an energy value near the mid gap.

The general Equations 4.7, 4.8 presented in the opening of the chapter allow us to find interface traps density wherever inside the bandgap. The last ones (4.7, 4.12) are focused in the mid gap and look more suitable for a single frequency estimation. The frequency value chosen (100 kHz) approximately corresponds to the conductance peak in depletion region. Also, this frequency has permitted fast measures (being a high frequency) and clear CV and GV curves.

One more consideration about the value of G_p. As stated above, the MOS measured is seen by the tool like Fig. 4.15c and the conductance measured is G_m. Equation 4.9 has to be applied and the value of G_p can be calculated. At this point a question could arise because this method considers crucial the value of G_p peak but G_m is measured: it has been demonstrated that the peak conditions of G_m are really close to the ones of G_m [25].

In conclusion, the complete method remains the best one and it is really interesting trying to estimate how far this fast method than the classic one is. The values estimated following the general method can be also one or two orders of magnitude higher than the ones estimated in this way but this is reasonable according to Hill and Coleman [25]. This is because the complete method can scan the entire bandgap: at the boundaries of the energy region investigated traps concentration can increase of also one order of magnitude and this explains why the fast method can underestimate D_{it} values (see Fig. 4.4). However, the aim of this work is not providing an advanced technique to find precise values for D_{it}. The goal is finding a general trend of D_{it} in the material under test and a general underestimation can be accepted.

4.3.4 Interface Trap Density Investigation

The techniques explained in the previous paragraph have been followed to investigate the annealing temperature dependency of D_{it}. As mentioned before, CV and GV measurements have been done at 100 kHz, sweeping the gate voltage from -5V up to +3V.

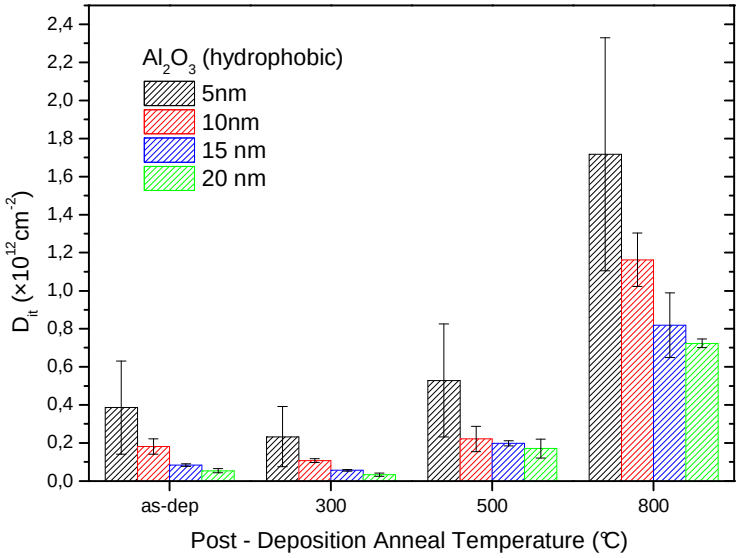


Figure 4.19: Estimated average D_{it} as a function of annealing temperature for p-type CZ Silicon samples (hydrophobic surface) coated by 5, 10, 15, 20 nm of Al_2O_3.

D_{it} calculated for different Al_2O_3 thicknesses (from 5 nm to 20 nm) are illustrated in Fig. 4.19 and reported in Tab. 4.3. The picture clearly depicts a dramatic increase of the D_{it} value after high temperature annealing (above 500 °C), up to one order of magnitude higher than lower annealing: e.g. from 5.28×10^{11} cm^{-2} eV^{-1} (500 °C) to 1.72×10^{12} cm^{-2} eV^{-1} (800 °C) for 5 nm passivated layer and from 2.21×10^{11} cm^{-2} eV^{-1} (500 °C) to 1.36×10^{12} cm^{-2} eV^{-1} (800 °C) for 10 nm. Low temperature annealing provides D_{it} values relatively close to each other (compared to high temperature D_{it})reaching the lowest values at 300 °C. The mentioned drop of chemical passivation (strong increase of D_{it}) at the highest annealing temperatures (above 500 °C), has been caused by the dehydrogenation of dangling bonds at the Silicon surface [22].

It has been also observed that D_{it} increases with thicker Al_2O_3 layers.

Table 4.3: Interface trap density (D_{it}) for p-type CZ Silicon samples (hydrophobic) coated by 5, 10, 15, 20 nm of ALD Al_2O_3.

	D_{it} (× 10^{12} cm^{-2})			
T_{ann} (˚C)	5 (nm)	10 (nm)	15 (nm)	20 (nm)
as-dep	0.387	0.181	0.0838	0.0541
300	0.233	0.107	0.0565	0.0329
500	0.528	0,221	0.198	0.17
800	1,717	1,163	0.819	0.723

4.3.4.1 Impact of Surface Finishing on Chemical Passivation

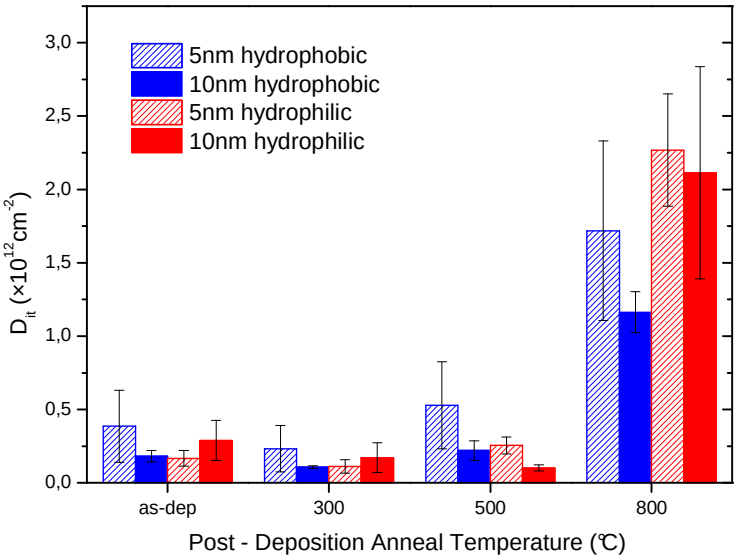


Figure 4.20: Estimated average D_{it} as a function of annealing temperature for p-type CZ Silicon samples (H- terminated, blue bars; OH-terminated, red bars) coated by 5, 10 nm of Al_2O_3.

The effects of Silicon surface termination on chemical passivation have been also investigated. Al_2O_3 passivation layer has been deposited on Silicon surfaces both hydrophobic or hydrophilic to understand if the cleaning process is relevant for chemical passivation. Hydrophilic surfaces have pointed up a tendency similar to the hydrophobic one, showing a drop of chemical passivation at high anneal temperatures (above 500 °C), as depicted in Fig. 4.20.

The D_{it} values estimated for hydrophilic samples have been collected in Table 4.4.

Table 4.4: Interface trap density (D_{it}) for p-type CZ Silicon samples (hydrophilic) coated by 5, 10 nm of ALD Al_2O_3.

	D_{it} ($\times 10^{12}$ cm^{-2})	
T_{ann} (°C)	*5 (nm)*	*10 (nm)*
as-dep	0.168	0.29
300	0.112	0.171
500	0.255	0.102
800	2,279	2,113

After low temperature annealing (300, 500 °C), the hydrophilic samples have in general showed lower D_{it} values than hydrophobic surfaces. This have been considered due to the formation of a thicker SiO_2 layer on the hydrophilic Silicon surfaces [28].

The interfacial SiO_2 layer is supposed to play a central role with respect to the Al_2O_3 surface passivation, being a key factor both for field effect passivation (as observed before) and chemical passivation. Since SiO_2 is known to effectively reduce the D_{it} at the SiO_2/Silicon interface, this thin interfacial SiO_2 layer might be effectively responsible for the low D_{it} values above mentioned [10].

The hypothesis has been verified by *X-ray Photoelectron Spectroscopy* (XPS). XPS has been used to determine the atomic concentrations of Al_2O_3 deposited on Silicon with hydrophobic or hydrophilic surface finishing, after different post-deposition annealing. 3

nm thick Al_2O_3 (XPS requires a thin dielectric layer) has been deposited on both sides of mirror polished p-type CZ Silicon with a resistivity of 1.5 Ω·cm and a thickness of 700 μm using ALD at 200 ˚C. Prior to deposition, Silicon surfaces have been H- or OH- terminated by the final cleaning step, as reported in section 3.1. XPS measurements have been performed in a *Thermo Science Theta300*.

The atomic concentrations of as-deposited or Forming Gas Annealed (FGA) (H_2) Al_2O_3 with a thickness of 3 nm, deposited on H- / OH- terminated Silicon surfaces are listed in Tab. 4.5.

Table 4.5: Atomic concentration (%) of 3 nm thick Al_2O_3 deposited on Silicon with hydrophobic/hydrophilic surfaces.

	Atomic concentration (%)							
T_{ann}	Hydrophobic				Hydrophilic			
(˚C)	*Al*	*O*	*SiO_2*	*Si sub*	*Al*	*O*	*SiO_2*	*Si sub*
as-deposited	30.3	44.1	< DL	16.4	27.8	40.1	11.9	2.7
FGA (350 °C, 20 min)	29.5	43.4	0.8	16.1	29.2	44.8	13.2	2.8

Table 4.5 displays the atomic percentage of Aluminum, Oxygen, SiO_2 and Silicon both in hydrophobic and hydrophilic surface. The typical penetration depth of the beam is 5 nm leading to contribution of the Silicon substrate.
Regarding the formation of a Silicon oxide layer, no SiO_2 interface has been observed for as-deposited hydrophobic sample. After FGA, the SiO_2 concentration increased up to 0.8%. Differently, a SiO_2 interface layer is present in as-deposited Al_2O_3 films deposited on hydrophilic Silicon surfaces. The SiO_2 interface increases after the annealing. It can be observed that the Silicon substrate contribution is significant lower compared with the result coming from hydrophobic substrate.

The difference in SiO_2 intensity is displayed in Fig. 4.21a. The SiO_2 and Al_2O_3 thickness are calculated by using the signal of Fig. 4.21a and the results are displayed in Fig. 4.21b.

In Fig. 4.21a, one can see that the spectrum of as-deposited Al_2O_3 on hydrophobic Silicon surfaces shows no peak associated with SiO_2 (102 eV). The intensity of the peak depends on the thermal treatment: the maximum is after annealing. The peak at 98 eV corresponds to the Silicon and therefore independent on the Silicon surface termination and annealing. The spectrum of Fig. 4.21a shows a SiO_2 peak for as-deposited Al_2O_3 on Silicon with hydrophilic surface, indicating the presence of an interface layer. Fig. 4.21b shows the thickness calculated from the signal displayed in Fig. 4.21a. No detectable SiO_2 interface is present between as-deposited Al_2O_3 and hydrophobic Silicon surface. A SiO_2 interface layer is formed during the forming gas anneal. The as-deposited SiO_2 interface of Al_2O_3 deposited on hydrophilic Silicon surface has a thickness of 1.01 nm. The interface increased slightly to a thickness of 1.06 nm after annealing.

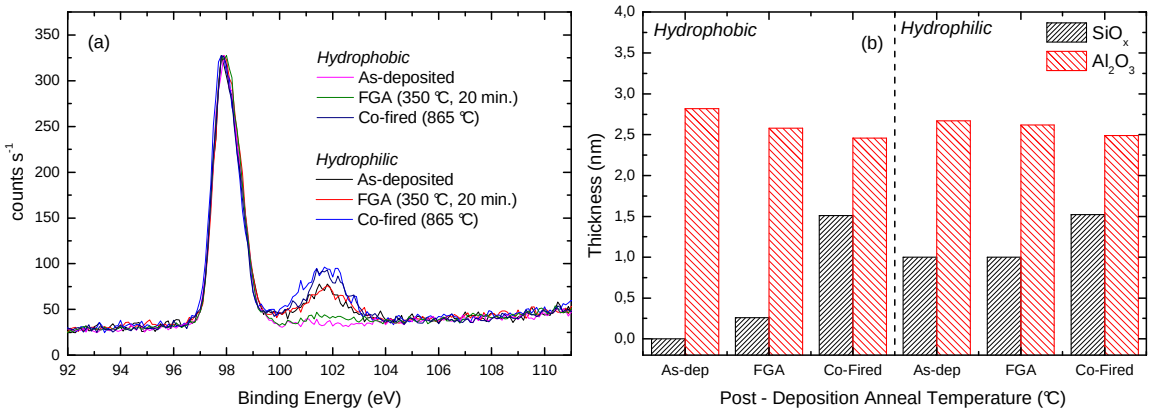


Figure 4.21: SiO_2 and Al_2O_3 thickness of as-deposited and FGA (350 ˚C, 20 min.) samples deposited on Silicon with hydrophobic and hydrophilic surfaces. An additional co-firing treatment (865 °C) has been considered to make more clear the graphs.

4.4 Relating Electrical Results to Effective Carrier Lifetime

Carrier lifetime is commonly used as a parameter to characterize passivation quality.

Effective carrier lifetimes of the double side passivated samples (p-type CZ) have been measured by QSSPC measurements at 1×10^{15} cm^{-3} injection level and are shown (normalized) in Fig. 4.22 as a function of annealing temperature.

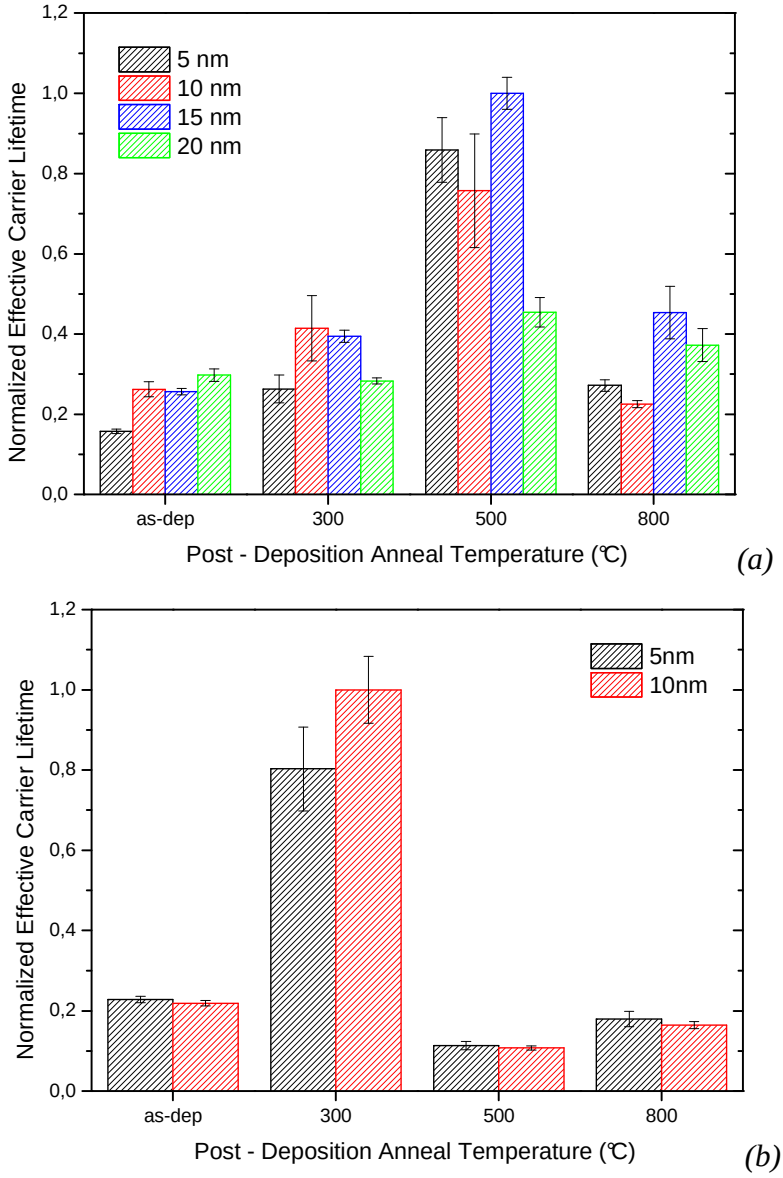


Figure 4.22: Effective carrier lifetime at $\Delta n = 1\times10^{15}$ eV^{-1} cm^{-2} of (a) hydrophobic and (b) hydrophilic Al_2O_3 passivated layers as a function of the annealing temperature. All lifetimes have been normalized to the highest value.

Both graphs of Fig. 4.22 depict a general improvement after a certain post-deposition thermal treatment: (a) the hydrophobic surfaces reach a relevant improvement at 500 °C, (b) the hydrophilic surfaces at a lower annealing temperature (300 °C).

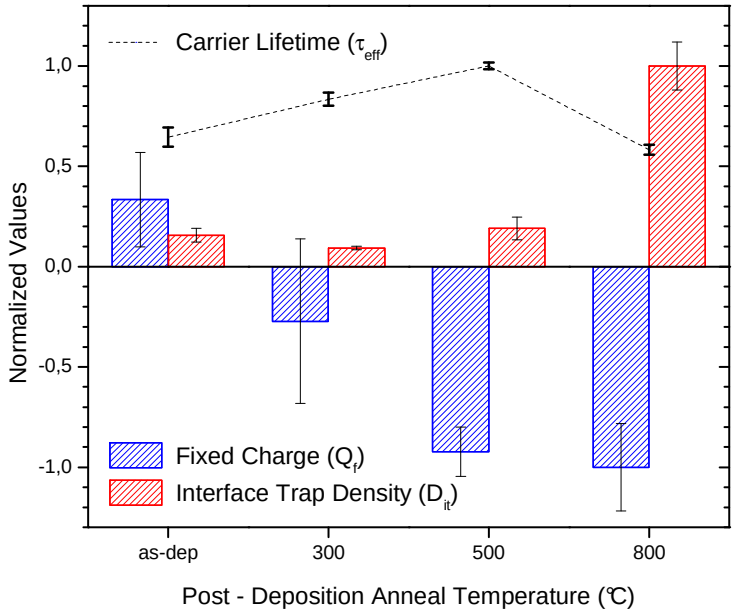


Figure 4.23: Normalized effective carrier lifetimes, Q_f (*field effect passivation*) and D_{it} (*chemical passivation*) for p-type CZ Silicon (hydrophobic surface) passivated by 10 nm of Al_2O_3 as a function of annealing temperature.

The electrical characterization described in the previous paragraphs fits well with the QSSPC results above illustrated. Fig. 4.23 provides a correlation between the lifetime measurements and the parameters estimated trough the electrical characterization (Q_f, D_{it}) for a Silicon hydrophobic surface passivated by a 10nm ALD Al_2O_3 layer (all the values have been normalized).

A clear improvement of τ_{eff} as a function of annealing temperature can be observed, reaching an optimum at 500 °C and decreasing after an annealing at 800 °C. The electrical characterization results coherent. (i) At low anneal temperatures, chemical passivation is adequate (low D_{it} values) but the charges in the Al_2O_3 have the wrong polarity resulting in low effective lifetimes. (ii) At higher annealing temperatures (500°C), chemical passivation remains sufficient and due to negative charges in Al_2O_3 a field effect is formed, ideal for p-type CZ Silicon passivation and causing maximal effective lifetimes. (iii) At too high annealing temperatures, chemical passivation is destroyed resulting in decreasing effective lifetimes while keeping a similar field effect as in (ii).

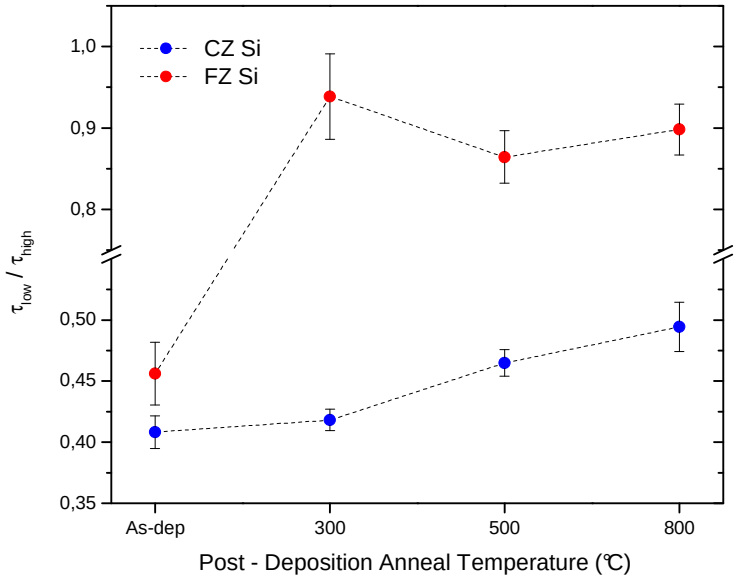


Figure 4.24: Ratio between effective lifetime at injection level of 1x10^{14} cm^{-3} (τ_{low}) and 1x10^{15} cm^{-3} (τ_{high}) as a function of annealing temperature for 10 nm of ALD Al_2O_3 deposited on p-type CZ Silicon (blue dots) or FZ Silicon (red dots) of comparable resistivity and thickness.

The graphs above make clear how important is D_{it} parameter. Field Effect (negative fixed charge formation inside Al_2O_3) is fundamental to reach a good level of passivation, however its benefit can be obtained only with a low level of interface defect density, meaning few recombination centers near the surface. Fig. 4.23 depicts a relevant amount of negative fixed charge also after an high temperature (800 °C) annealing: however, the high interface trap density annuls any benefit coming from field effect passivation.

There is also a direct relation between measurements of *lifetime* and Q_f. Fig. 4.24 shows the ratio between τ_{eff} at *low injection level* (τ_{low}, n = 1 × 10^{14} cm^{-3}) and τ_{eff} at *high injection level* (τ_{high}, n = 1 × 10^{15} cm^{-3}) as a function of annealing temperature for 10 nm of ALD Al_2O_3 deposited on p-type CZ or FZ Silicon. In case of a $Q_f < 0$ for p-type Silicon passivation layers, illumination or injection independency is expected. For 10 nm of Al_2O_3 (200 °C ALD on hydrophobic Silicon surface) and a post-deposition anneal 300 °C, a negative Q_f has been measured as shown above, which is also clear from Fig. 4.24: for the FZ Silicon samples, τ_{low} / τ_{high} values very close to 1 have been measured for annealing temperatures

above 300 °C, clearly proving the illumination independency. Unfortunately, this relation is less visible for the low quality CZ samples, which are known to have a strong decrease in effective lifetime for lower injection levels because of enhanced Shockley-Read-Hall recombination caused by the low quality bulk material.

4.5 Silicon Surface Texturing Influence

The influence of Silicon surface polishing prior to ALD Al_2O_3 (10 nm) passivation has also been investigated since it will affect the final surface passivation.
The samples analyzed have been made of CZ Silicon, similar to the one analyzed in the previous paragraphs. Various surface roughnesses have been obtained by varying the amount of Silicon removal during polishing (5, 10, 15 and 20 μm) [29]. Thereafter these surfaces have been passivated by using 10 nm of Al_2O_3 and a subsequent annealing at 350 °C in FG.

Being these samples similar to the previous ones, it has been considered reasonable to keep the metal-Silicon workfunction estimated before in Paragraph 4.2.2.1 (≈ 0.47 V) and a Q_f evaluation has been possible (Fig. 4.25 and Table 4.6).

Table 4.6: Fixed charge density (Q_f) for p-type CZ Silicon samples (hydrophobic) coated by 10 nm of ALD Al_2O_3. The Silicon surfaces have different polishing treatments.

	Q_f ($\times 10^{12}$ cm^{-2})				
T_{ann} (°C)	*FT*	*5 (nm)*	*10 (nm)*	*15 (nm)*	*20 (nm)*
350 °C	-0.973	-0.863	-0.823	-0.752	-0.699

The field effect depends on the surface roughness: an increase of the negative fixed charge density from the most polished surface (-7 × 10^{11} cm^{-2}) to the fully textured surface (-1 × 10^{12} cm^{-2}) has been observed (Fig. 4.25b). As expected, the fixed charge density value

obtained on the more polished surface is equivalent to the one calculated in the previous paragraph for a 300 °C annealing.

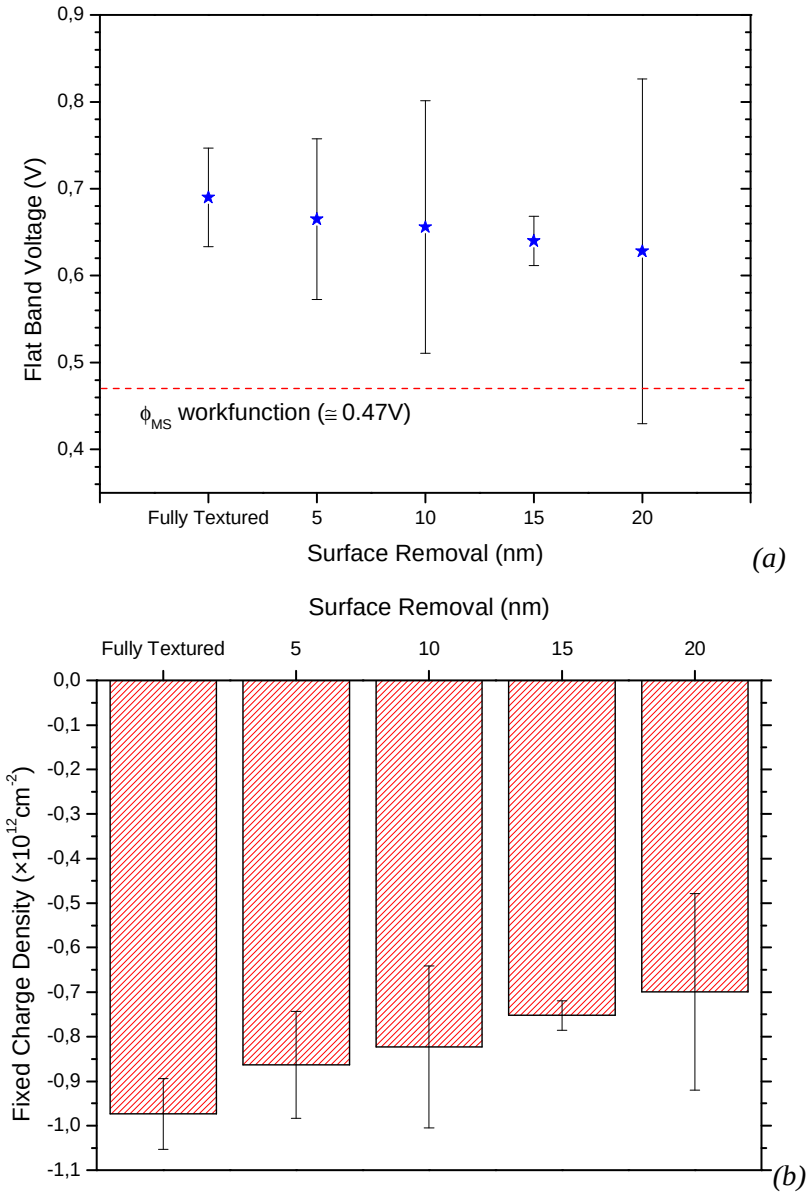


Figure 4.25: V_{FB} values in function of their corresponding surface removals. The values look close each other depicting a smooth improvement with less polished surfaces: highest flat band value (meaning highest negative Q_f) has been observed in fully textured surface (FT).

Fig. 4.26 depicts D_{it} and τ_{eff} (normalized) as a function of the Silicon removed during the polishing. It can be seen a dramatic reduction of D_{it} and an increase of τ_{eff} after any polishing.

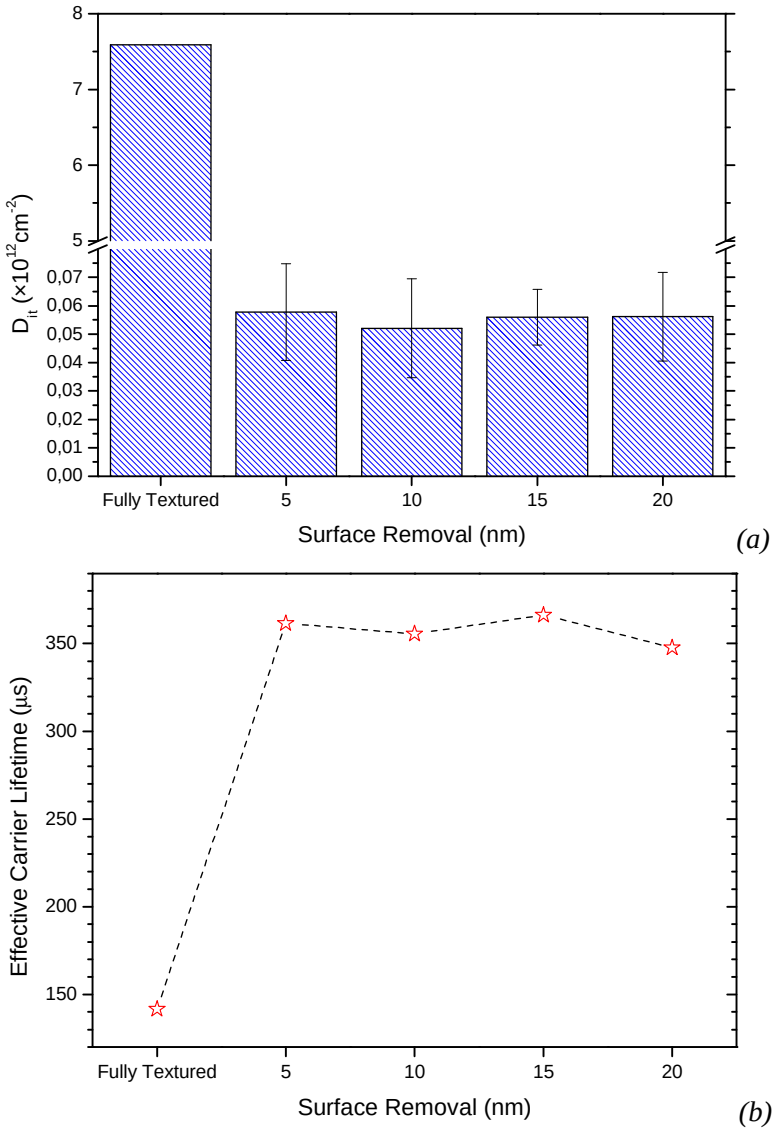


Figure 4.26: (a) D_{it} and (b) effective carrier lifetime (τ_{eff}, $\Delta n = 1 \times 10^{15}$ cm^{-3}) as function of the surface polishing (Fully Textured and 5, 10, 15, 20 µm of Silicon removed).

All the removals provide values close each others, meaning a limited influence of the texturing on this parameter. However, the fully textured surface presents a D_{it} value two

orders of magnitude higher than the others. It means that any polishing treatment of the surface (also limited, e.g. 5nm) is necessary to avoid a high D_{it} level. D_{it} estimation fits well with measured lifetimes: lifetime and D_{it} graphs have the same shape. It proves how texturing affects mostly D_{it}, influencing less the fixed charge.

In conclusion, it has been observed that a polishing treatment of the surface prior Al_2O_3 deposition is required: (i) Fully Textured surface presents the highest negative Q_f but also a not sufficient level of chemical passivation (high D_{it}); (ii) after every polishing step, field effect passivation is still adequate but also D_{it} is sufficiently low to provide high τ_{eff} values.

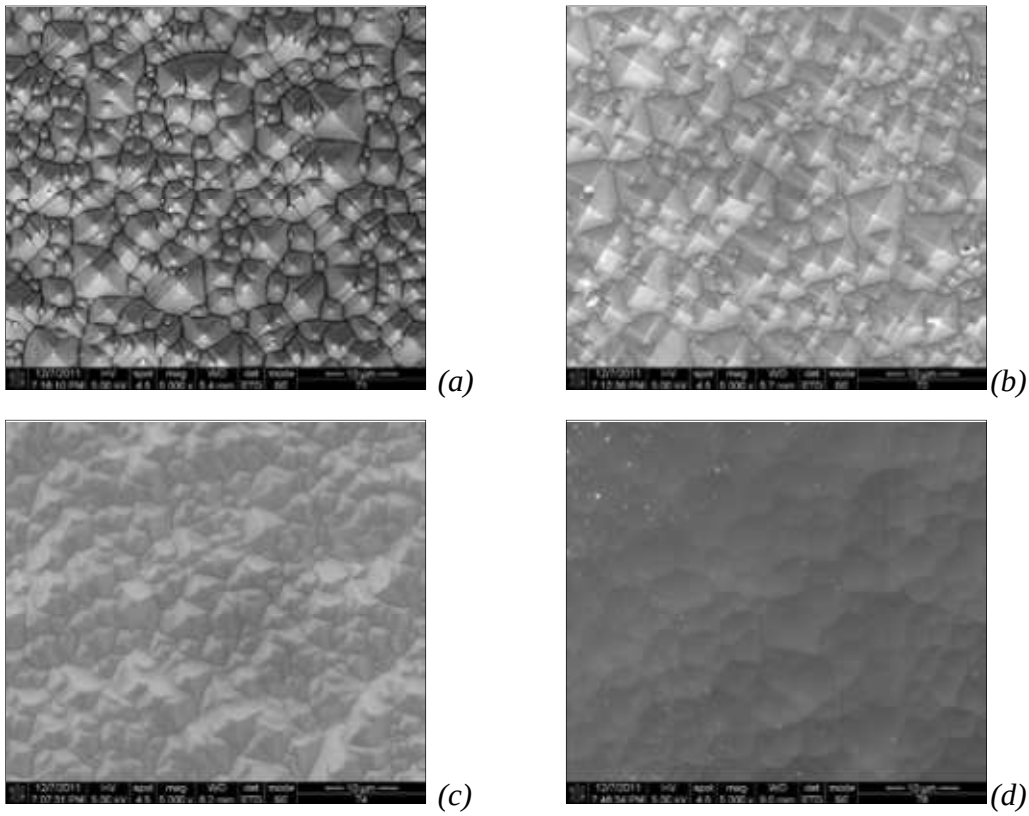


Figure 4.27: Top view SEM image of Silicon surface for textured (a), 4 µm (b), 7 µm (c) and 15 µm (d) removal [29].

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Chapter 5

Silicon Surface Passivation by PECVD Al_2O_3

The benefits of a passivation layer deposited by ALD have been investigated in the last chapter. ALD allows the deposition of high quality and uniform dielectric layers. However, it is also an expensive and time consuming technique, hardly applicable to a real industrial process, making PECVD interesting for the PV production.
PECVD Al_2O_3 films have been investigated in this chapter as Silicon surface passivation layers. Different deposition conditions (temperature and pressure, T_{dep} and P_{dep}) have been considered: the samples investigated are collected in Tab. 5.1. Every slot contains the corresponding dielectric film deposited.

5.1 Electrical Characterization

5.1.1 Fixed Charge Density Investigation

Even though the materials involved in these samples are formally similar to the ones of the previous chapter, PECVD samples have to be analyzed independently. PECVD is a process less accurate than ALD, giving structures less ideal (D_{it} much higher than ALD is expected)

and also the parameters of the MOS stack investigated can be different with respect to the ALD samples.

As seen in Chap. 4, a key parameter is the metal-semiconductor workfunction of the system (φ_{ms}). As mentioned before, an exact value of φ_{ms} has been calculated plotting V_{FB} voltages of different passivation layer thicknesses (10, 20, 30nm) and finding the intercepts on the ordinate-axis (Fig. 5.1).

Table 5.1: PECVD Al_2O_3 films investigated.

P_{dep} *(mBar)*	T_{dep} *(°C)*	
	350	*400*
0.15	10, 20, 30 nm	20, 30 nm
0.2	20, 30 nm	-

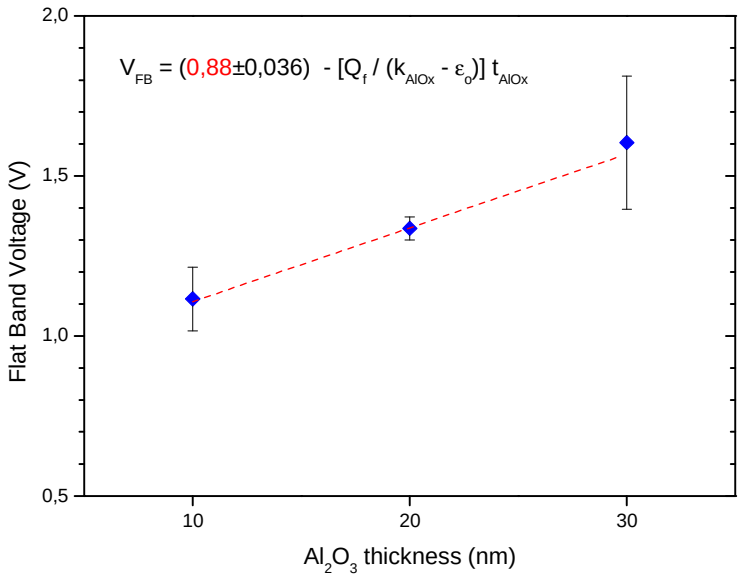


Figure 5.1: Average V_{FB} in function of their corresponding PECVD Al_2O_3 passivation layer thicknesses (T_{dep}=350 ˚C / P_{dep}=0.15 mBar on hydrophilic Silicon surfaces). The three points show a good alignment and the intercepts with ordinate axis provides a reasonable estimation of the workfunction of the system (0.88 ± 0.04 eV).

As expected, φ_{ms} here estimated (0.88 eV) is not the value early obtained (0.47 eV): it is not meaningless and confirms how a different system this is. Nevertheless, also this new value can be considered reasonable, within the expected range 0.27 – 1.33 eV [1].

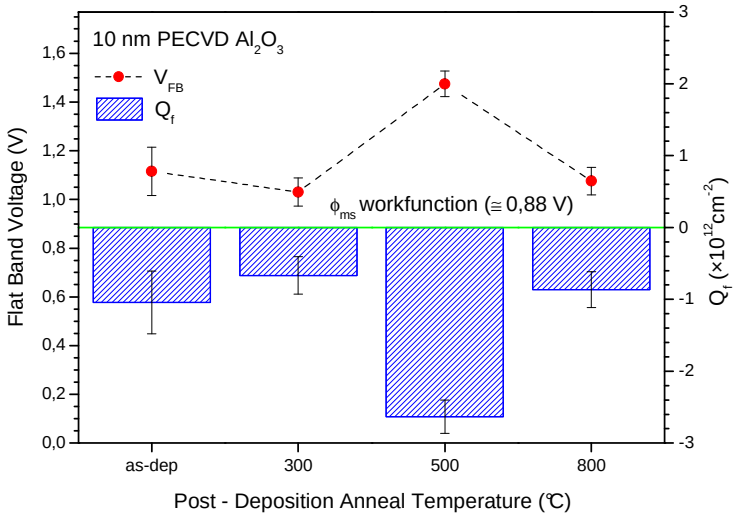
The evaluation of φ_{ms} for PECVD samples has been more problematic with respect to ALD samples. The ALD V_{FB} in function of the corresponding thicknesses (5, 10, 15, 20 nm) have provided aligned points and a relatively easy estimation of the intercepts with the ordinate axis (= φ_{ms} value). This has been less easy with PECVD films: it has been supposed to be due to the thicknesses chosen. ALD thicknesses are quite thin (5 nm up to 20 nm) compared to PECVD ones (10 nm up to 30 nm): the thickest layers (30 nm) have been considered affected by a relevant blistering, preventing well aligned V_{FB} plots.

CV curves for 10 and 20 nm PECVD films have showed realistic V_{FB} values: not 30 nm films, providing V_{FB} not aligned with the 10-20 nm ones, except with T_{dep}=350 °C / P_{dep}=0.15 mBar as-deposited films. This has been considered a further proof for blistering effect: in fact, it has been observed how blister formation in a thick dielectric film becomes more and more relevant increasing anneal temperature, e.g. [2]. However, the evaluation of the as-deposited 30 nm film has not been possible for T_{dep}=400 °C / P_{dep}=0.15 mBar and T_{dep}=350 °C / P_{dep}=0.2 mBar: this has not been completely understood and a further research is required.

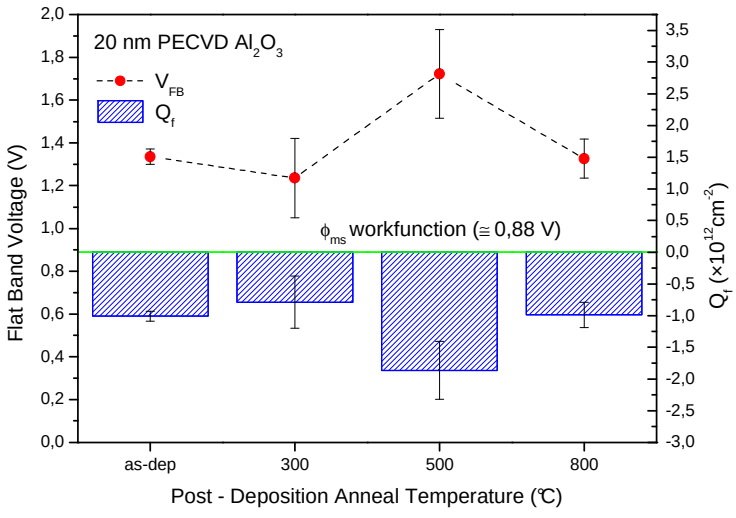
Considering these relevant issues, the choose of such thick layers comes from PECVD technique itself: ALD is really accurate and suitable also for really thin layers, PECVD is less precise and only quite thick layers can be distinguished.
Because of this, fixed charge density have been calculated always moving from T_{dep}=350 °C / P_{dep}=0.15 mBar workfunction. This is not the most accurate way to characterize T_{dep}=400 °C / P_{dep}=0.15 mBar and T_{dep}=350 °C / P_{dep}=0.2 mBar samples, being different systems. However, such assumption can provide a general tendency showing the temperature dependency of the samples investigated, even though with not really precise

fixed charge density values. This assumption is similar to what stated in the previous chapter about the general underestimation of D_{it}.

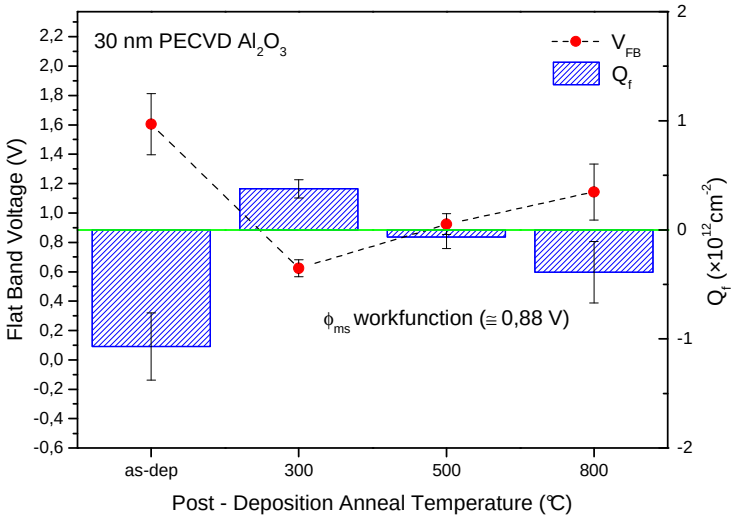
Fixed charge density evaluation above described brings the results illustrated in Fig. 5.2 and listed in Tab. 5.2.



(a)



(b)



(c)

Figure 5.2: Average V_{FB} values shifting with respect of workfunction level of the system (≈ 0.88 V): points above reference line mean the formation of a negative fixed charge density. (a) and (b) depict 10 and 20 nm PECVD (T_{dep}=350 °C / P_{dep}=0.15 mBar) Al_2O_3 samples, respectively. (c) refers to the sample coated by 30 nm of Al_2O_3: it has been considered less trustworthy than (a) and (b) because of blistering.

Table 5.2: Fixed charge density (Q_f) for p-type CZ Silicon samples (hydrophilic) coated by 10, 20, 30 nm of PECVD Al_2O_3 (T_{dep} = 350 °C / P_{dep} = 0.15 mBar).

	Q_f ($\times 10^{12}$ cm^{-2})		
T_{ann} (°C)	*10 (nm)*	*20 (nm)*	*30 (nm)*
-	-1.042	-1.009	-1.068
300	-0.667	-0.788	0.378
500	-2.633	-1.864	-0.0649
800	-0.864	-0.988	-0.387

Fig. 5.2 illustrates that the fixed charge density inside 10 and 20 nm PECVD dielectric films remains (i) almost constant and (ii) negative in polarity for all anneal temperatures (from as-dep up to 800 °C). Only after the 500 °C anneal, a significant decrease of Q_f is noticed. It means an adequate level of field effect passivation after every thermal treatment,

also prior annealing: unlike ALD Al_2O_3 passivated samples from previous chapter, a negative Q_f is also measured for as-deposited samples.

PECVD negative fixed charge density after 500 °C anneal is expected higher than the corresponding ALD one, as reported previously (e.g.) by Dingemans et al. [3]. Here, this value is comparable to the ALD counterpart (e.g. 10 nm Al_2O_3 deposited film): -(2.58 ± 0.6) x 10^{12} cm^{-2} for ALD and -(2.63 ± 0.23) x 10^{12} cm^{-2} for PECVD.
Even though Veith et al. have recently found similar results [4], it is probably due to the technique used to extract fixed charge density in the dielectric. To get precise values, other methods should be followed: e.g. Corona Charging [5,6] or Second Harmonic Generation [7].

Other relevant issues have been revealed measuring PECVD samples: less uniform film thickness than ALD samples and a not insignificant metal dot size variability. Since ALD layers have showed a less variable dot area, it has been supposed that this two problems are related, due to the deposition technique used. As stated before, PECVD is a process less accurate than ALD, yielding less regular layers. It means that PECVD films have more rough surfaces and dot area can be higher than expected (Fig. 5.3).

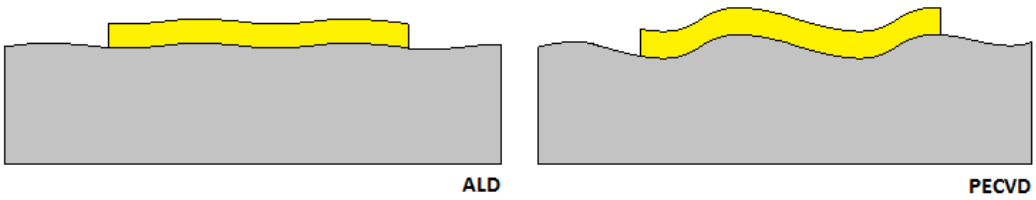


Figure 5.3: The deposition technique used (ALD or PECVD) can affect not only the thickness uniformity of the layer grown but also the effective area of the metallization.

As mentioned above, a fixed charge evaluation for T_{dep}=400 °C / P_{dep}=0.15 mBar and T_{dep}=350 °C / P_{dep}=0.2 mBar PECVD films is more problematic, probably because of blistering effect, since only thick films (20, 30 nm) have been available. Nevertheless, a

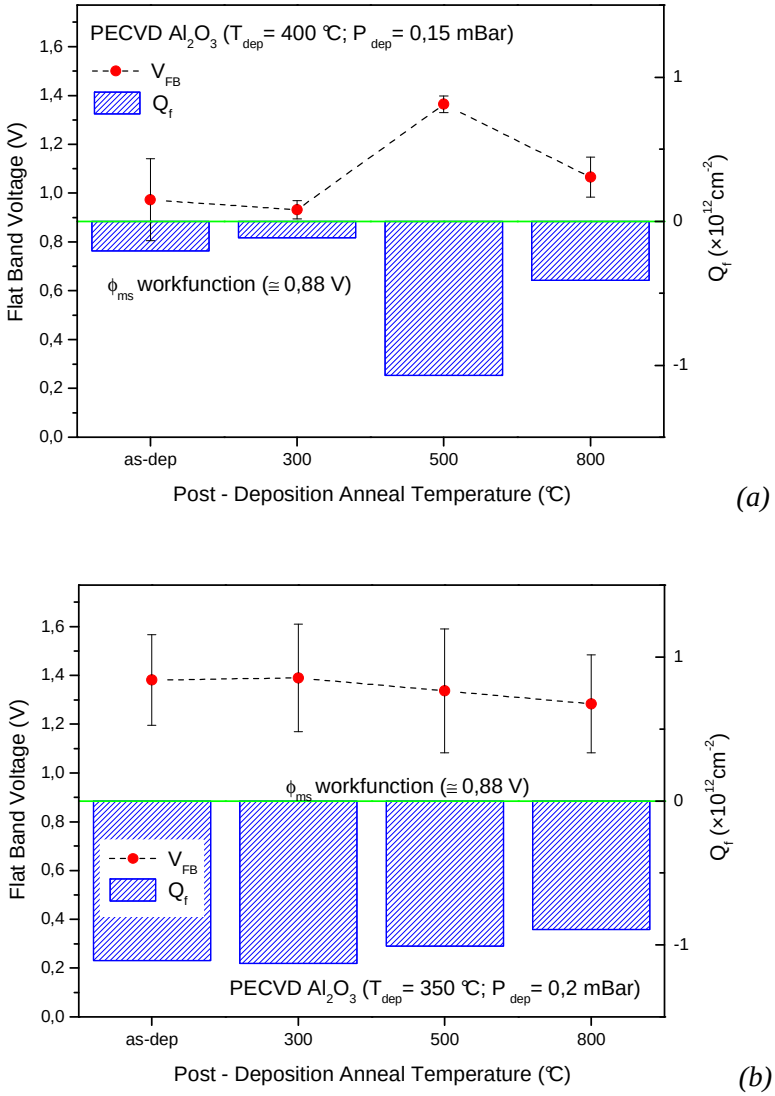


Figure 5.4: Average V_{FB} values shifting with respect of workfunction level of the system (≈ 0.88 V): points above reference line mean the formation of a negative fixed charge. Graphs refer to (a) T_{dep}=400 °C / P_{dep}=0.15 mBar and (b) T_{dep}=350 °C / P_{dep}=0.2 mBar 20 nm PECVD Al_2O_3 films. The reference level (workfunction) comes from T_{dep}=350 °C / P_{dep}=0.15 mBar films.

charge investigation has been done from workfunction estimated for the first group of PECVD samples (T_{dep}=350 °C / P_{dep}=0.15 mBar) and the corresponding graphs and values are showed in Fig. 5.4 and Tab. 5.3. The graphs refer only to 20 nm PECVD layers: the results coming from 30 nm films have been considered not trustworthy. Even though the systems are dissimilar (different deposition conditions), the assumed workfunction value (0.88 eV) can be considered more reasonable than the one coming from ALD samples, being different also the deposition process.

These calculations depend on a parameter coming from a different system and the values of their results have been considered not trustworthy. They have to be considered just to understand the general temperature dependency of the systems investigated.

Table 5.3: Fixed charge density (Q_f) for p-type CZ Silicon samples (hydrophilic) coated by 20 nm of PECVD Al_2O_3 (T_{dep}=400 °C / P_{dep}=0.15 mBar and T_{dep}=350 °C / P_{dep}=0.2 mBar).

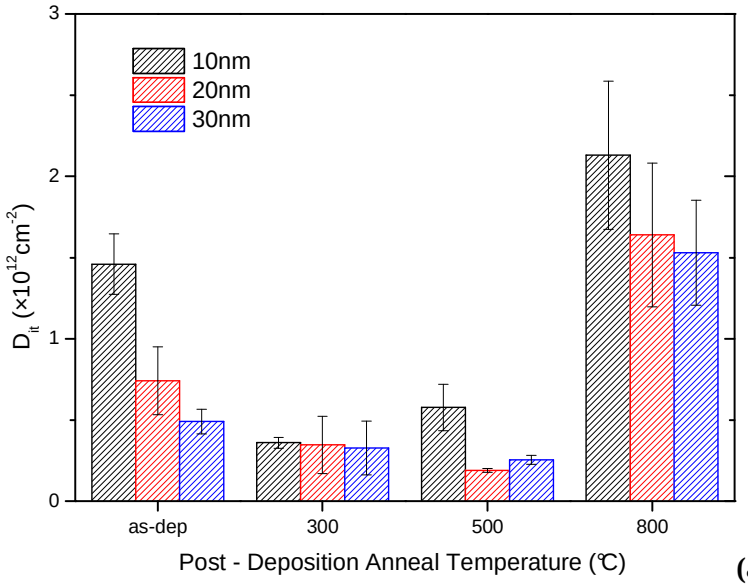
	Q_f ($\times 10^{12}$ cm^{-2})	
	T_{dep}=400 °C / P_{dep}=0.15 mBar	T_{dep}=350 °C / P_{dep}=0.2 mBar
-	-0.205	-1,109
300	-0.115	-1,128
500	-1,071	-1,009
800	-0.41	-0.893

5.1.2 Interface Trap Density Investigation

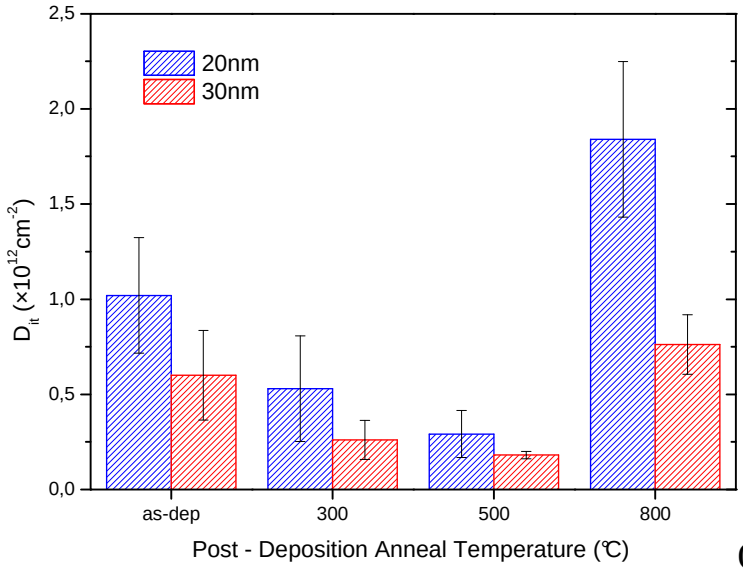
D_{it} evaluation of PECVD samples has been estimated as described in Chap. 4. Fig. 5.5 illustrates D_{it} for the PECVD samples here analyzed.

The dependency of D_{it} with respect of anneal temperature in PECVD samples, is similar to what has been observed in ALD films early investigated. After a low temperature

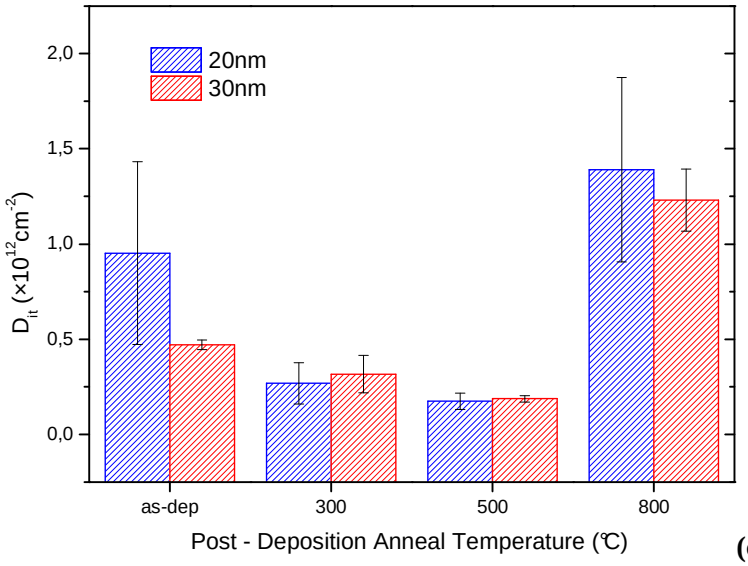
annealing, a decrease of D_{it} can be observed, meaning an improvement of the quality of chemical passivation: Fig. 5.5 illustrates the lowest D_{it} value by annealing at 500 °C (unlike ALD films, more close to 300 °C). After an high temperature annealing (800 °C), a dramatic growth of D_{it} occurs (like ALD films).



(a)



(b)



(c)

Figure 5.5: Average D_{it} as a function of annealing temperature for p-type CZ Silicon samples passivated by: (a) 10-20-30 nm of PECVD Al_2O_3, T_{dep}=350 °C / P_{dep}=0.15 mBar, (b) 20-30 nm of PECVD Al_2O_3, T_{dep}=400 °C / P_{dep}=0.15 mBar, (c) 20-30 nm of PECVD Al_2O_3, T_{dep}=350 °C / P_{dep}=0.2 mBar. All the surfaces above mentioned are hydrophilic.

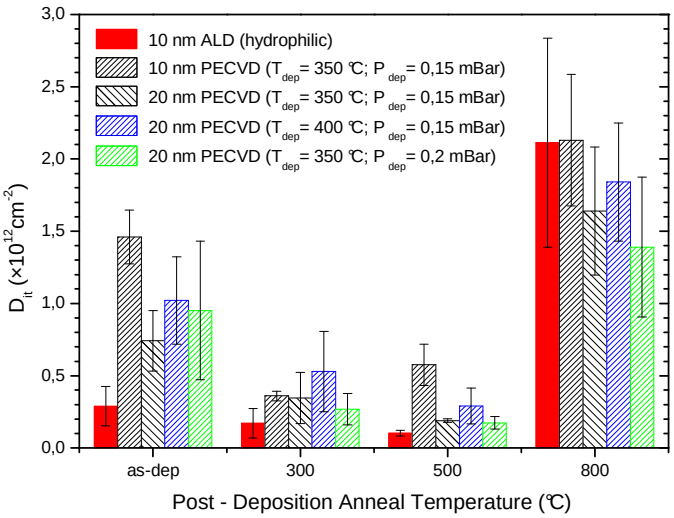


Figure 5.6: Average D_{it} as a function of annealing temperature for p-type CZ Silicon samples passivated by: (i) 10 nm of ALD Al_2O_3 (hydrophilic surface), red bars; (ii) 10, 20 nm of PECVD Al_2O_3 (in different deposition conditions), patterned bars.

Beyond a similar temperature dependency between ALD and PECVD samples, it can be also seen in Fig. 5.6 how as-dep D_{it} values of PECVD samples are up to one order of magnitude higher than ALD hydrophilic ones, as reported previously in other works [3,4]. E.g. (i) as-dep 10 nm ALD Al_2O_3 film (hydrophilic surface) has D_{it} = (1.81 ± 0.39) × 10^{11} cm^{-2}, (ii) as-dep 10 nm PECVD Al_2O_3 (T_{dep}=350 °C / P_{dep}=0.15 mBar) has D_{it} = (1.46 ± 0.19) × 10^{12} cm^{-2}. This difference is significant at low temperatures: after thermal treatments it becomes less relevant. This means that (i) PECVD is a deposition technique that provides less surface control than ALD and it needs post-deposition anneal treatments to improve D_{it}; (ii) after annealing, D_{it} values from ALD and PECVD become closer [3]. Hence, the implementation of efficient PECVD passivation layers is possible and it has been recently proved also by manufacturing PECVD-PERC cells with efficiencies similar to ALD ones [4].

Table 5.4: Interface trap density (D_{it}) for p-type CZ Silicon samples (hydrophilic) coated by 10, 20, 30 nm of PECVD Al_2O_3 (T_{dep}=350 °C / P_{dep}=0.15 mBar).

	D_{it} ($\times 10^{12}$ cm^{-2})		
T_{ann} (˚C)	*10 (nm)*	*20 (nm)*	*30 (nm)*
-	1.46	0.74	0.49
300	0.36	0.35	0.33
500	0.58	0.19	0.25
800	2.13	1.64	1.53

Table 5.5: Interface trap density (D_{it}) for p-type CZ Silicon samples (hydrophilic) coated by 20, 30 nm of PECVD Al_2O_3 (T_{dep}=400 °C / P_{dep}=0.15 mBar).

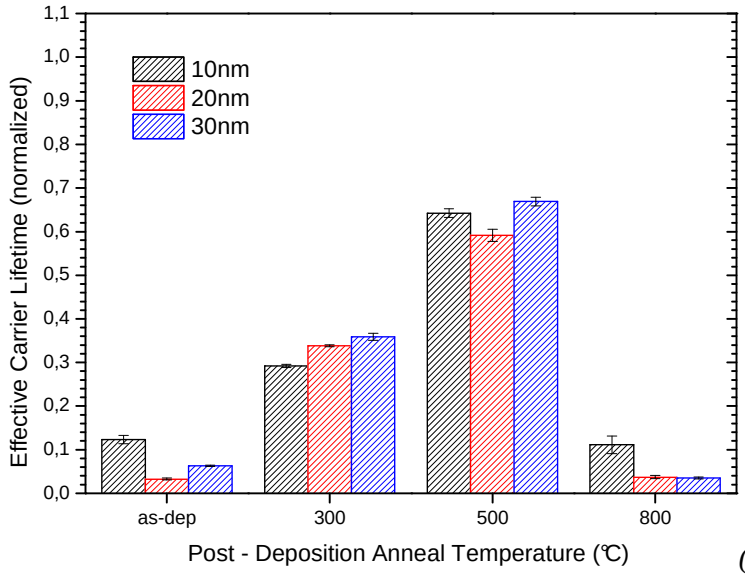
	D_{it} ($\times 10^{12}$ cm^{-2})	
T_{ann}	*20 (nm)*	*30 (nm)*
-	1.02	0.6
300	0.53	0.26
500	0.29	0.18
800	1.84	0.76

Table 5.6: Interface trap density (D_{it}) for p-type CZ Silicon samples (hydrophilic) coated by 20, 30 nm of PECVD Al_2O_3 (T_{dep}=350 °C / P_{dep}=0.2 mBar).

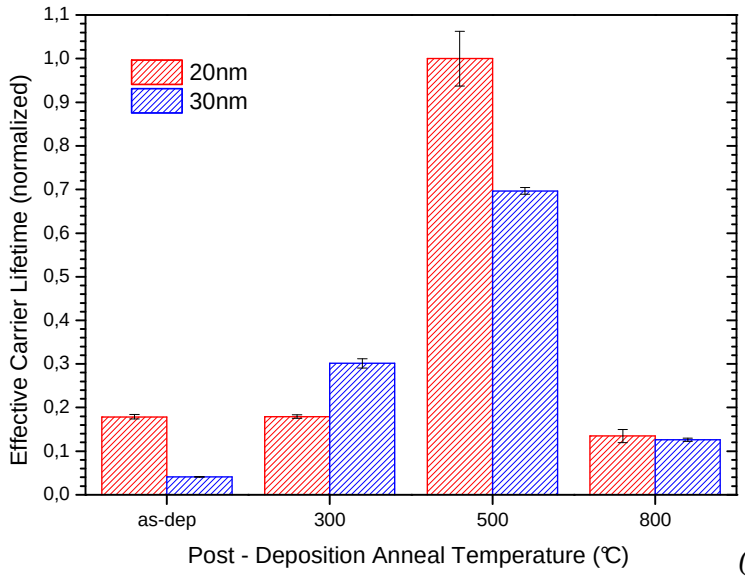
	D_{it} ($\times 10^{12}$ cm^{-2})	
T_{ann}	*20 (nm)*	*30 (nm)*
-	0.95	0.47
300	0.27	0.32
500	0.17	0.19
800	1.39	1.23

5.2 Relating Electrical Results to Effective Carrier Lifetime

Lifetime measurements have been used (like in Chap. 4) to access the effective surface passivation and to correlate the electrical results, obtained in the previous paragraphs, to the carrier lifetimes.



(a)



(b)

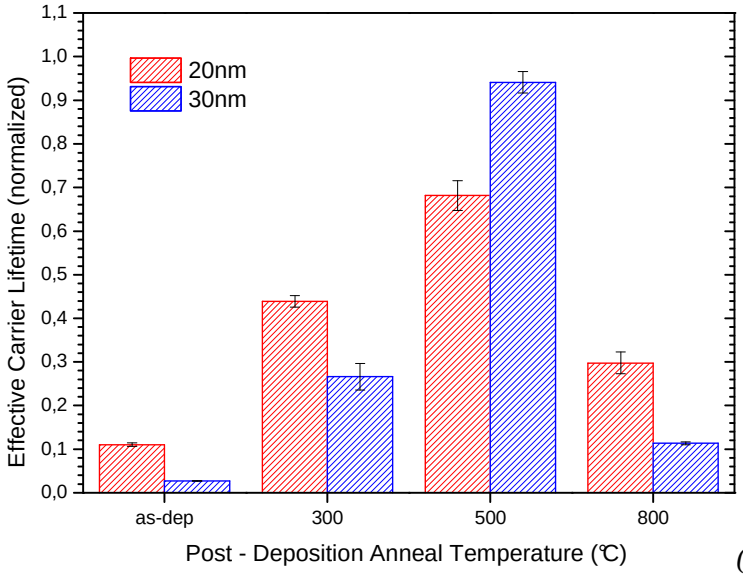


Figure 5.7: Normalized effective carrier lifetimes at $\Delta n = 1 \times 10^{15}$ cm^{-3} for p-type CZ Silicon surfaces coated by: (a) 10-20-30 nm of PECVD Al_2O_3, T_{dep}=350 °C / P_{dep}=0.15 mBar, (b) 20-30 nm of PECVD Al_2O_3, T_{dep}=400 °C / P_{dep}=0.15 mBar, (c) 20-30 nm of PECVD Al_2O_3, T_{dep}=350 °C / P_{dep}=0.2 mBar. All the surfaces above mentioned are hydrophilic.

Effective carrier lifetimes (τ_{eff}) of the p-type CZ Silicon samples passivated by PECVD Al_2O_3 have been measured by QSSPC at 1×10^{15} cm^{-3} injection level. Results are shown (normalized) in Fig. 5.7 for all the PECVD samples investigated (on OH- terminated surfaces) as a function of annealing temperature.

Fig. 5.8 compares the electrical results (Q_f and D_{it}) with the lifetime measurements in one of the films analyzed. Q_f, D_{it} and τ_{eff} depicted refer to 10 nm PECVD Al_2O_3 (T_{dep}=350 °C / P_{dep}=0.15 mBar) samples. There is a clear improvement of τ_{eff} as a function of annealing temperature, reaching an optimum around 500 °C and decreasing after an annealing at 800 °C. The electrical characterization and QSSPC results fit well together. (i) As-deposited PECVD samples show a low level of chemical passivation (high D_{it} values, unlike ALD samples early investigated), even though (ii) field effect passivation is observable: a fixed charge density negative in polarity is already formed and is present after every annealing. This results in low effective lifetimes. (iii) At higher annealing temperatures (500 °C), field

effect passivation remains sufficient but also an adequate chemical passivation is obtained (low D_{it} values, comparable to the ALD ones), ideal for p-type CZ Silicon passivation and causing maximal effective lifetimes. (iv) At too high annealing temperatures (800 °C), chemical passivation is destroyed resulting in decreasing effective lifetimes while keeping a similar field effect as in the previous points.

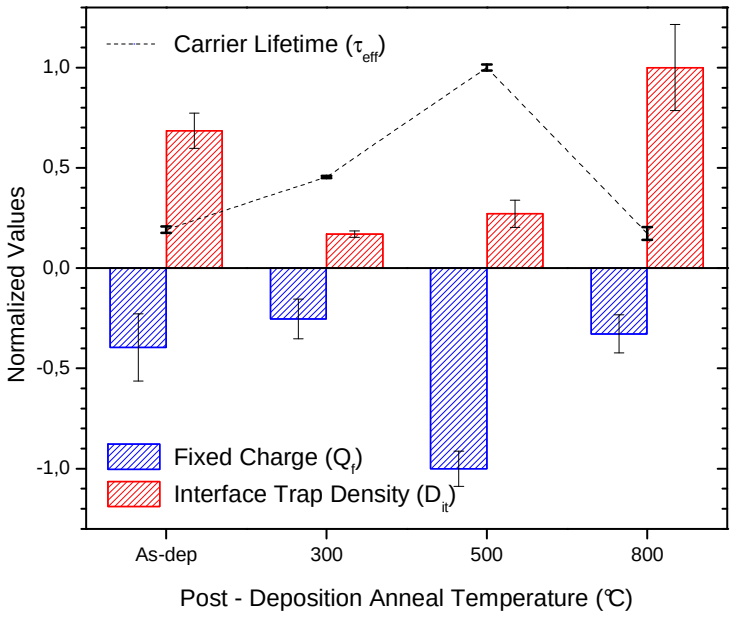


Figure 5.7: Normalized effective carrier lifetimes at $\Delta n = 1 \times 10^{15}$ cm^{-3}, Q_f (corresponds to field effect passivation) and D_{it} (corresponds to chemical passivation) for p-type CZ Silicon passivated by 10 nm of PECVD Al_2O_3 (T_{dep} = 350 °C / P_{dep} = 0.15 mBar) as a function of annealing temperature.

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Chapter 6

Silicon Surface Passivation by HfO_2

Al_2O_3 is a widely used and analyzed material in thin- film solar cells research. Another candidate for the employment as thin function layer in Silicon solar cells is HfO_2. This dielectric has been intensively studied by the C-MOS industry because of the high k-value and the low interface trap density (D_{it}) [1]. In this chapter, HfO_2 layers have been studied for the application as passivation layer in Silicon solar cells.
Given the novelty of this material as passivation layer, high quality substrates (FZ Silicon) have been used.

The passivated Silicon layers have been provided by the *University of Tartu* (Estonia). The deposition of HfO_2 by ALD, using $HfCl_4$ and H_2O is reported by K. Kukli *et al.* and J. Aarik *et al*. [2,3]. The optimized deposition cycle demonstrated a growth rate of 0.18 – 0.29 nm cycle^{-1}, which is significantly higher than the typical growth rate of Al_2O_3 using TMA + H_2O (0.125 nm cycle^{-1}). The growth has been performed at T_{dep} = 300 °C on polished 2.72 Ω·cm p-type FZ Silicon wafers (≈ 280 μm thickness), unlike Al_2O_3 samples investigated in the previous chapters (CZ Silicon). Annealing steps have been done in FG (N_2, 10% H_2) at 300 and 500 °C for 20 minutes
K. Kukli *et al.* and J. Aarik *et al*. have deeply studied this material from a physical point of view: the aim of this chapter is to provide a reasonable characterization as passivation material by electrical measurements.

Several CV measurements have been performed on the layers and an estimation of dielectric constant of HfO_2 layer has been calculated (≈ 13), being well known how this value varies changing deposition conditions of dielectric layer [3]. The value estimated looks reasonable and consistent with Aarik's work [3].

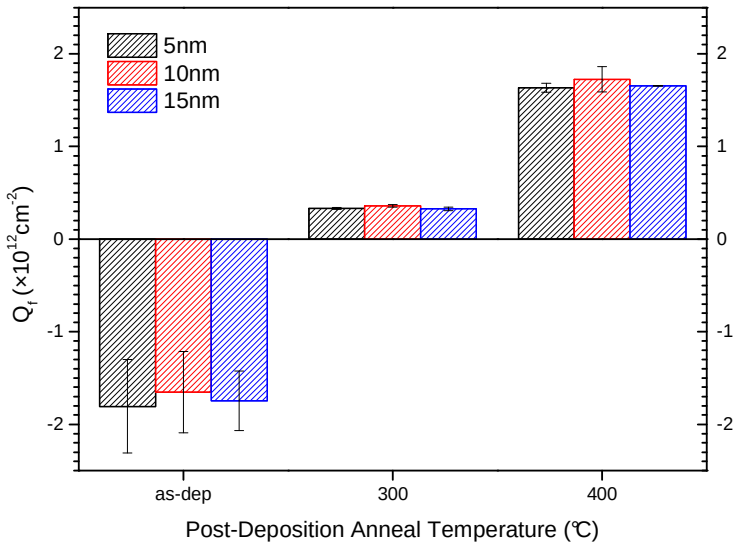

Figure 6.1: Average Q_f as a function of annealing temperature for 5, 10, 15 nm of HfO_2 deposited on p-type FZ Silicon.

Table 6.1: Fixed charge density (Q_f) for p-type FZ Silicon samples (hydrophilic) coated by 5, 10, 15 nm of ALD HfO_2.

	Q_f (× 10^{12} cm^{-2})		
T_{ann} (˚C)	*5 (nm)*	*10 (nm)*	*15 (nm)*
-	-1,806	-1,654	-1,746
300	0.331	0.359	0.327
500	1,635	1,726	1,656

The electrical characterization of these samples is analog to what has been done in the previous chapters (Chap. 4 and 5). The fixed charge density estimation comes from three

different film thicknesses (5, 10 and 15 nm). The usual V_{FB} investigation has given $\varphi_{ms} \approx$ 0.61 ± 0.029 eV (considered reasonable [4]) : the average Q_f values as a function of annealing temperature are depicted in Fig. 6.1 and collected in Tab. 6.1.

Average D_{it} values as a function of annealing temperature are depicted in Fig. 6.2 and the calculated values are in Tab. 6.2.

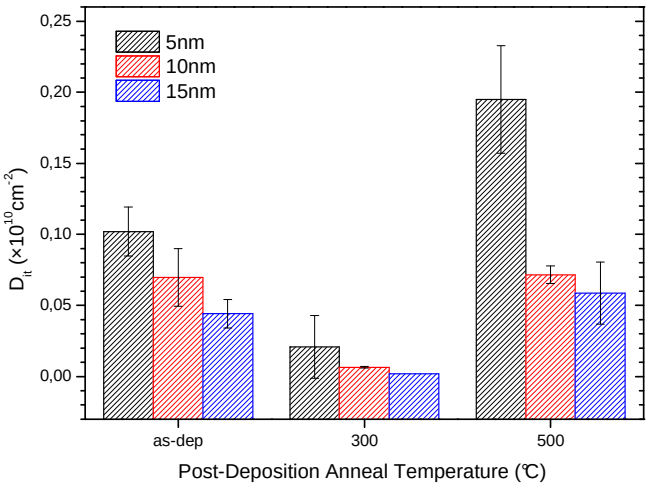

Figure 6.2: Average D_{it} as a function of annealing temperature for 5, 10, 15 nm of HfO_2 deposited on p-type FZ Silicon.

Table 6.2: Interface trap density (D_{it}) for p-type FZ Silicon samples (hydrophilic) coated by 5, 10, 15 nm of ALD HfO_2.

	D_{it} ($\times 10^{10}$ cm^{-2})		
T_{ann} ($^{\circ}C$)	*5 (nm)*	*10 (nm)*	*15 (nm)*
-	10.201	6.966	4.414
300	2.077	0.647	0.206
500	19.49	7.153	5.865

Fig. 6.1 and Fig. 6.2 show a different tendency compared to Al_2O_3: as-deposited, a negative fixed charge density is already present. After an anneal at 300 °C, the polarity changes and the positive fixed charge density increases with the temperature. The negative fixed charge density has been considered a consequence of the presence of negative charge Cl^{-1} residuals from the precursor in the thin film [3].The Cl atoms are effused during a post deposition thermal treatment, therefore decreasing the negative fixed charge density level. It has been also supposed that the positive charge after annealing is the result of oxygen vacancies. Furthermore, hydrogen from H_2O is released during the annealing, leading to a decrease of interface trap density.

The D_{it} as a function of annealing temperature is similar to what observed for Al_2O_3: an anneal treatment can improve the quality of Silicon/HfO_2 interface, decreasing D_{it}. Nevertheless, D_{it} values estimated above are much lower than the corresponding densities of Al_2O_3 layers, meaning that an adequate interface quality is always present. However, it has to be considered that HfO_2 has been deposited on FZ Silicon substrates (FZ-Silicon): these low values could depend only on the high-quality substrate.

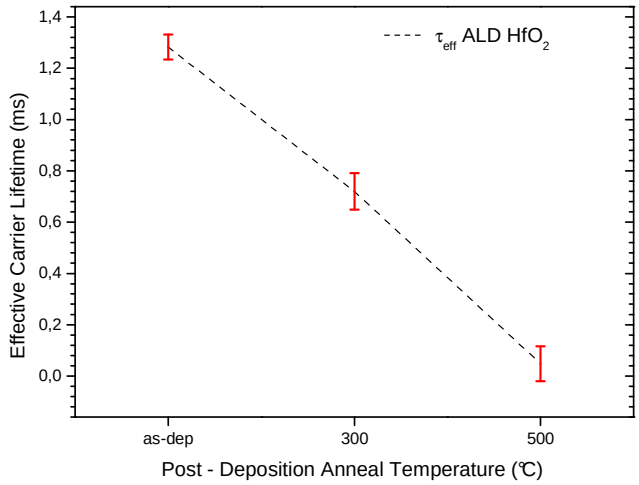

Figure 6.3: Effective carrier lifetimes at $\Delta n = 1 \times 10^{15}$ cm^{-3} for p-type FZ Silicon passivated by 10 nm of ALD HfO_2 as function of annealing temperature.

Fig. 6.3 represents the effective carrier lifetime of 10 nm ALD HfO_2 in function of anneal temperature. The figure depicts the highest lifetime value prior to anneal treatments (as-dep), after which a drop can be observed.
The data collected in Fig. 6.1 and Fig. 6.2 fit with the lifetime data depicted in Fig. 6.3. The only anneal condition providing a sufficient passivation level is as-deposit (Fig. 6.3): (i) this is the only case with a relevant negative Q_f value, $(-1.65 \pm 0.76) \times 10^{12}$ cm-2; (ii) D_{it} is low in any thermal condition, meaning passivation depends mostly on Q_f. Fig. 6.3 shows the same tendency: the highest lifetime value measured corresponds to the as-dep layer then, the Silicon passivation is degraded after any temperature treatment.

HfO_2 has been demonstrated as a good candidate for Silicon surface passivation, especially at low annealing temperatures. Also, the high refractive index of 2.12 or higher is favorable for the use of the layer as anti-reflection coating.

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Chapter 7
Conclusions

It has been shown that a thermal post-deposition treatment is required to reduce the interface trap density (D_{it}) level for all investigated passivation layer deposition methods. The annealing temperature dependency of D_{it} does not depend on the deposition technique. (i) ALD samples as-deposited have a D_{it} value higher than PECVD samples, (ii) after thermal treatments at temperatures below 500 °C D_{it} is reduced, (iii) after annealing temperatures of more than 500 °C D_{it} strongly increase, causing a degrading chemical passivation. The surface roughness investigation shows that after removing 5μm from an alkaline textured surface, the D_{it} of the passivated surface saturates at values of $5\times10^{11}cm^{-2}$. The different deposition techniques and the deposited dielectrics show an effect on the fixed charge density. (a) ALD Al_2O_3 requires a thermal treatment to become negatively charged, (b) PECVD Al_2O_3 shows a negative charge density value at every post-deposition temperature. (c) ALD HfO_2 has a negative fixed charge density only as deposited: all post deposition thermal treatments provide a change towards positive charges. Fixed charge density (Q_f) and Interface trap density (D_{it}) have been investigated as key parameters for surface passivation. It has been shown that determining their values, the effective carrier lifetime (τ_{eff}, the main parameter to characterize surface passivation) can be predicted. In every sample, the highest τ_{eff} occurs only with adequate values of Q_f and D_{it}. (i) ALD and PECVD Al_2O_3 show the best lifetime values after a low temperature thermal annealing (300, 500 °C); (ii) ALD HfO_2 samples have their optimum after the deposition.

Appendix

A Manuscript and poster presented at 38th IEEE-PVSC, Austin (TX, USA)

B *WCT-120*, Silicon wafer lifetime tester, Sinton Consulting Inc.

C *Accudry*, IPA vapor dryers, IMTEC

D *Savannah Series*, ALD systems, Cambridge NanoTech

E *Levitrack Tool*, Spatial ALD system, Levitech

F *FlexAl*, PEALD systems, Oxford Instruments

G *DEP_X 2000*, PECVD system, Roth&Rau

H *PA300PS*, semi-automatic probing system, Cascade Microtech Inc.

I *Agilent 4284A* (ex HP4284A), precision LCR meter, Agilent Tech.

Electrical characterization of ALD Al_2O_3 – HfO_2 and PECVD Al_2O_3 passivation layers for p-type CZ-Silicon PERC solar cells

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[3]Katholieke Universiteit Leuven (K.U.Leuven), Oude Markt 13 Bus 5005, 3000 Leuven, Belgium
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***Abstract* — This work characterizes p-type Silicon surface passivation using a high-k material (Al_2O_3 or HfO_2) combining capacitance voltage (CV) and lifetime measurements.**

For Al_2O_3 samples, the Silicon substrate bulk and surface quality is equivalent to CZ Silicon used in industrial solar cell processing. While Al_2O_3 has been proven to provide high quality surface passivation on p-type doped Silicon surfaces, the influence of the growth conditions and the post-deposition annealing is not yet completely understood. The dielectric thin film has been deposited by common techniques (ALD, PECVD) on H-/OH- terminated Silicon surfaces (hydrophobic and hydrophilic, respectively). The impact of the roughness of the surface prior to the deposition has been also considered. Then, the passivation of each layer has been investigated as a function of different Al_2O_3 thicknesses (5 to 20 nm) and post-deposition annealing temperatures (300 to 800 °C). CV measurements have been used to characterize *chemical passivation* (= interface trap density, D_{it}) and *field effect passivation* (= fixed charge density, Q_f). Lifetime measurements have been used to assess the effective surface passivation. The results of both types of electrical characterization fit well together. (i) Prior post-deposition anneal, only either chemical passivation (ALD) or field effect passivation (PECVD) is adequate, resulting in lower effective lifetimes. (ii) At higher annealing temperatures, a negative net charge in the Al_2O_3 and a low D_{it} at the interface are measured, ideal for p-type CZ Silicon passivation and causing maximal effective lifetimes. (iii) At too high annealing temperatures, chemical passivation is destroyed resulting in decreasing effective lifetimes even though negative field effect remains in many cases.

Another candidate as passivation layer on Silicon is HfO_2. Being a new material in photovoltaics, it has been studied on FZ Silicon substrates and its electrical characterization has demonstrated interesting passivation properties at low anneal temperatures (also without thermal treatment).

***Index Terms* — silicon surface passivation, Al_2O_3, HfO_2, conductance method, crystalline silicon solar cells, silicon.**

I. INTRODUCTION

At present, the photovoltaic (PV) market is dominated by crystalline Silicon solar cells, which is expected to continue for at least the next decade [1]. In addition, the Silicon wafer cost constitutes about 70% of the cell cost [2], driving the PV industry to ever thinner wafers. Therefore, striving for higher cell efficiencies, excellent surface passivation is required.

Al_2O_3 leads to outstanding rear surface passivation of p-type Silicon PERC (as is shown by cell efficiencies above 19 %), its industrially relevant deposition techniques being thermal ALD and Plasma-Enhanced Chemical Vapor Deposition (PECVD) [3,4,5]. However, the mechanisms behind passivation have not been completely understood yet.

This work aims to provide an electrical characterization (combining CV and lifetime measurements) of p-type CZ Silicon surface passivation. All the samples have been made of solar grade material and they have been investigated: (i) comparing different deposition techniques for Al_2O_3 (ALD, PECVD); analyzing the impact of the (ii) post-deposition temperature and (iii) the surface polishing on the substrate passivation. Finally, (iv) a novel material (HfO_2) has been also presented and compared with Al_2O_3.

II. EXPERIMENTAL

P-type Czochralski Silicon substrates with a resistivity of 1-1.5 Ω · cm and a thickness of 180 µm first endure a wet chemical Saw Damage Removal in NaOH:H_2O and neutralization in HCl:H_2O. Their surfaces are randomly textured and then polished in the HF/HNO_3 based solution varying the amount of Silicon removal, starting from a fully textured surface up to 20 µm removed [6]. After which the samples are cleaned in H_2O_2:H_2SO_4, followed by an HF dip, H_2O rinse and drying prior to deposition of the dielectric layer (H- terminated surfaces). An additional step with NH_4OH:H_2O_2:H_2O is required for OH- terminated surfaces. Al_2O_3 passivation layers are manufactured using thermal ALD with $Al(CH_3)_3$ and H_2O as precursors at a deposition temperature (T_{dep}) of 200 °C; the thickness of high-k layer is determinated controlling the number of cycles of the ALD process (40 cycles = 5 nm). HfO_2 layers are grown similarly using $HfCl_4$ and H_2O; the optimized deposition cycle demonstrates a growth rate of 0.18 – 0.29 nm per cycle [7,8]. Al_2O_3 passivation films are also made with PECVD at T_{dep} = 350 °C and P_{dep} = 0.15 mBar.

Post-deposition, Al_2O_3 samples are kept as-deposited or are annealed in N_2 at a temperature of 300, 500 or 800°C. HfO_2 samples to be annealed are submitted to thermal treatment in FG (10% H_2) at a temperature of 300 or 500 °C.

Double side passivated samples are used to characterize surface passivation by Quasi Steady State Photo Conductance measurements (QSSPC) using a Sinton WCT-120 instrument. Single side passivated samples are used for electrical

characterization: CV and conductance - voltage (GV) measurements. On one side coated with high-k material, Platinum is evaporated through a shadow mask by e-beam evaporation in order to define dot-shaped Schottky contacts with a diameter of 35-500 μm, while the other side is fully coated with Aluminium by Sputtering-PVD with a thickness of about ±2 μm.

The samples measured are not ideal, causing a significant fluctuation in the CV data. Therefore, on each sample a number of dots have been measured leading to an average effect. Also, to face leakage effects, all CV and GV data (C_m, G_m measured) have been evaluated using a *Loss Angle* approach: Loss Angle $\delta = [\arctan(2\pi f \cdot C_m/G_m)] \cdot (180/\pi)$, considering values above 80° as reliable (especially in depletion region).

III. RESULTS AND DISCUSSION

A. Aluminum Oxide as Silicon surface passivation

A1. Electrical characterization of ALD Al_2O_3 passivation layers

Al_2O_3 films deposited on polished (20 nm Silicon removed) hydrophobic surfaces have been first investigated.

Fixed charge density present in the Al_2O_3 layer has been calculated comparing similar samples with different passivation layer thicknesses (5, 10, 15 and 20 nm) and plotting the flat band voltage (V_{FB}) as a function of the equivalent oxide thickness (EOT) value [9]. For each sample, V_{FB} values have been extracted with *Hauser's Cvc software* [10] for the forward direction (inversion to accumulation) at 100 kHz. The dielectric charge has been calculated according to $Q_{ox} = C_{ox}(\varphi_{ms} - V_{FB})$, with C_{ox} the oxide capacitance and φ_{ms} the difference between Silicon and metal work functions [11]. This φ_{ms} is calculated by plotting V_{FB} as a function of respective thicknesses: the intercept with ordinate axis is φ_{ms} according to $V_{FB} = \varphi_{ms} - (Q_f \cdot t_{ox}) / (k_{ox} - \varepsilon_o)$ with $t_{ox} = 0$ and $k_{ox} \approx 8$ [11]. This way, for as-deposited Al_2O_3 samples a φ_{ms} of about 0.47 ± 0.004 eV has been calculated, as expected within the range of 0.27 to 1.33 eV [12]. φ_{ms} is equal to V_{FB} when no fixed charge density is in the system under investigation, therefore every shifting of V_{FB} with respect to φ_{ms} gives an estimation of Q_f. Fig. 1 shows the average V_{FB} values as a function of post-deposition anneal temperature for p-type CZ Silicon samples passivated by 5 or 10 nm of ALD Al_2O_3 and also the value of estimated φ_{ms} is indicated by a dashed reference line. This figure clearly shows a shift in V_{FB} as a function of annealing temperature. Even more, at higher annealing temperatures the V_{FB} becomes > φ_{ms}, which signifies the formation of a fixed negative charge density in the Al_2O_3 film. This negative fixed charge density formation inside the dielectric yields the creation of an electrical field at the Silicon surface preventing carrier recombination at the surface. The charge might be related with the formation of a SiO_2 layer on the Silicon surface after anneal treatments [13][14].

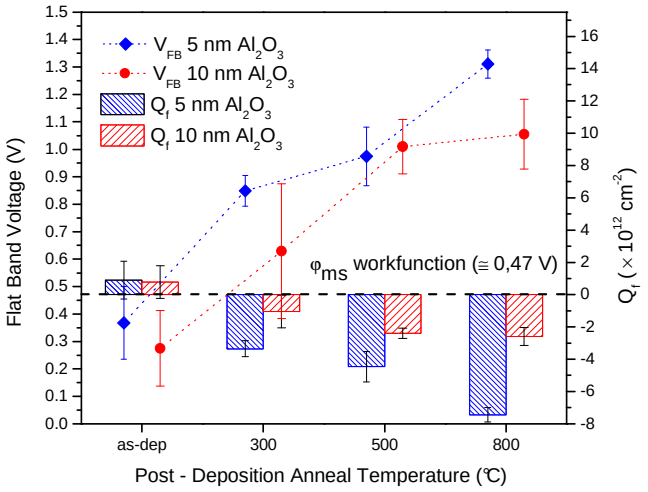

Fig. 1: Average flat band voltage as a function of anneal temperature for 5 and 10 nm of ALD Al_2O_3 on p-type CZ Silicon. Each shift corresponds to formation of charge density (below in the graph): data points above the reference line (aligned to φ_{ms}) correspond to negative fixed charge density present in the Al_2O_3 layer.

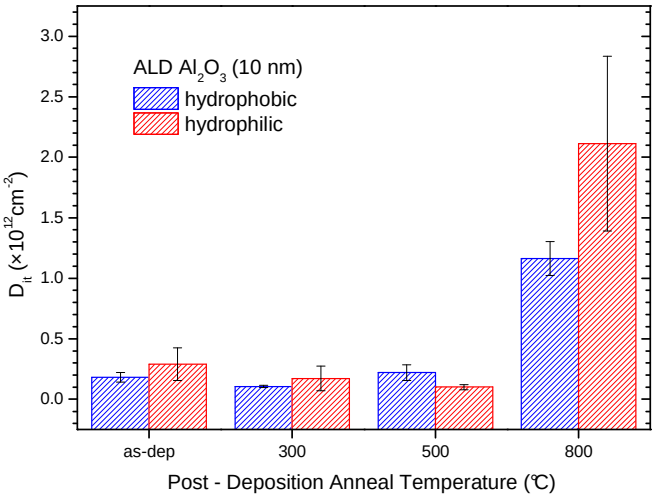

Fig. 2: Estimated average D_{it} as a function of annealing temperature for p-type CZ Silicon samples (H- terminated, blue bars, or OH-terminated, red bars) coated by 10 nm of Al_2O_3.

A number of methods are available for extracting the density of interface traps at dielectric-Silicon interface. In literature *Conductance Method* is considered the most accurate way to get an estimation of D_{it} [11]. However, it is quite lengthy being both time and frequency depending. Therefore, a simplified approach has been followed [15]. Conductance measurements have been taken at a fixed

frequency (100 MHz) sweeping only the voltage: leakage not affected measurements show a conductance peak in depletion area. For each sample, the conductance peak value measured (G_m) has been converted to corresponding *Substrate Conductance* (G_p), related to interface trap density according to $D_{it} = 2.5\ G_p/(q\omega)$ [11], where q is the elementary charge and ω the measurement angular frequency. D_{it} calculated for the 5 and 10 nm (hydrophobic and hydrophilic surface) Al_2O_3 samples are reported and compared in Fig. 2.

This figure depicts a general drop of chemical passivation (strong increase of D_{it}) at the highest annealing temperatures, caused by the dehydrogenation of dangling bonds at the Silicon surface [16].

The D_{it} values reported are reasonably low: according to Hill and Coleman [15] it is realistic since the method used is focused around mid Energy Gap.

Fig. 2 illustrates that the measured D_{it} values are well below 5×10^{11} cm^{-2} for both hydrophobic and hydrophilic surfaces for annealing temperatures up to 500 °C.

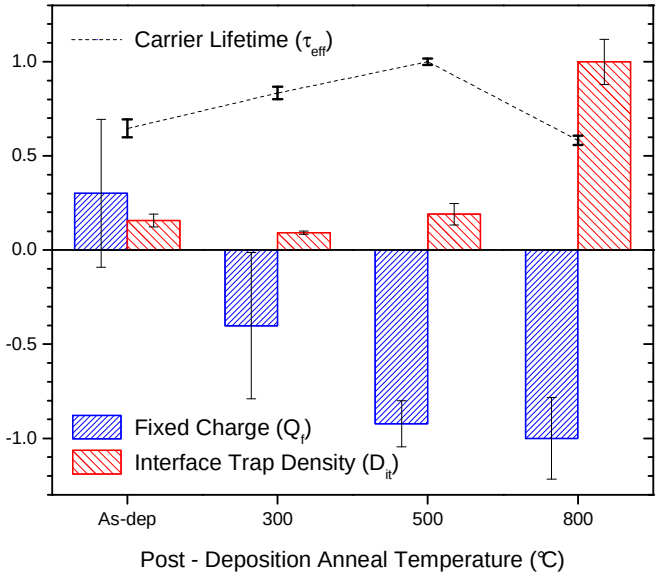

Fig. 3: Normalized effective carrier lifetimes at $\Delta n = 1 \times 10^{15}$ cm^{-3}, Q_f (corresponds to *Field Effect Passivation*) and D_{it} (corresponds to *Chemical Passivation*) for p-type CZ Silicon passivated by 10 nm of ALD Al_2O_3 as a function of annealing temperature.

Minority carrier lifetime is commonly used as a parameter to characterize passivation quality. Effective carrier lifetimes (τ_{eff}) of the p-type CZ Silicon samples passivated by ALD Al_2O_3 have been measured by Quasi Steady State Photo Conductance (QSSPC) at 1×10^{15} cm^{-3} injection level. Results are shown (normalized) in Fig. 3 for a 10 nm ALD Al_2O_3 passivation layer (on H- terminated surface) as a function of annealing temperature. Also Q_f and D_{it} are shown (normalized) for this 10 nm ALD Al_2O_3 passivation layer.

There is a clear improvement of τ_{eff} as a function of annealing temperature, reaching an optimum around 500 °C and decreasing after an annealing at 800 °C. The electrical characterization and QSSPC results fit well together. (i) At lower annealing temperatures, chemical passivation is adequate (low D_{it} values) but the charges in the Al_2O_3 have the wrong polarity resulting in lower effective lifetimes. (ii) At higher annealing temperatures (≈ 500 °C), chemical passivation remains sufficient and due to negative charges in Al_2O_3 a field effect is formed, ideal for p-type CZ Silicon passivation and causing maximal effective lifetimes. (iii) At too high annealing temperatures, chemical passivation is destroyed resulting in decreasing effective lifetimes while keeping a similar field effect as in (ii).

A2. Impact of the Silicon surface roughness on passivation properties

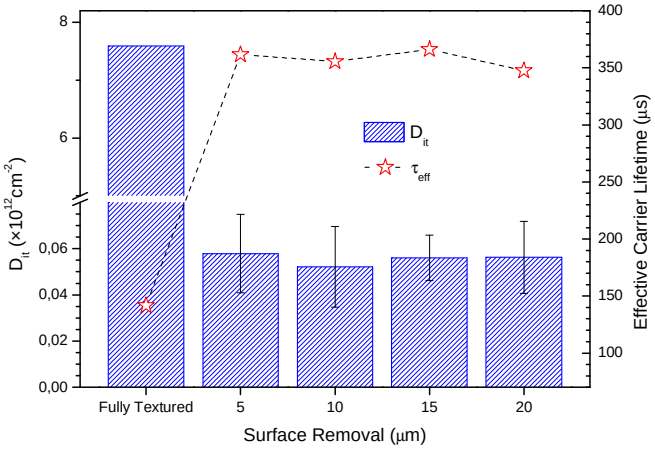

Fig. 4: D_{it} and effective carrier lifetime (τ_{eff}, $\Delta n = 1 \times 10^{15}$ cm^{-3}) as function of the surface polishing (Fully Textured and 5, 10, 15, 20 µm of Silicon removed).

The influence of Silicon surface polishing prior to ALD Al_2O_3 (10 nm) passivation has also been investigated since it will affect the final surface passivation.

Various surface roughnesses have been obtained by varying the amount of Silicon removal during polishing (5, 10, 15 and 20 µm) [6]. Thereafter these surfaces have been passivated using Al_2O_3 and a subsequent annealing at 350 °C in FG.

The field effect depends on the surface roughness: an increase of the negative fixed charge density from the most polished surface (-7×10^{11} cm^{-2}) to the fully textured surface (-1×10^{12} cm^{-2}) has been observed. As expected, the charge density value obtained on the more polished surface is equivalent to the fixed charge density calculated in section *A1* for a 300 °C annealing.

Fig. 4 depicts D_{it} and τ_{eff} (normalized) as a function of the Silicon removed during the polishing. It can be seen a dramatic reduction of D_{it} and an increase of τ_{eff} for all polished surfaces. It means that a polishing treatment of the surface prior Al_2O_3 deposition is required: (i) Fully Textured surface presents the highest negative Q_f but also a not sufficient level

of chemical passivation (high D_{it}); (ii) after every polishing step, field effect passivation is still adequate but also D_{it} is sufficiently low to provide high τ_{eff} values.

A3. Electrical characterization of PECVD Al_2O_3 passivation layers

Next to ALD Al_2O_3, also PECVD Al_2O_3 films have been investigated as Silicon surface passivation layers.

As above, the fixed charge density has been estimated from different passivation layer thicknesses: 10, 20 and 30 nm. Flat band voltages (V_{FB}) as a function of the equivalent oxide thickness (EOT) values have given $\varphi_{ms} \approx 0.88 \pm 0.036$ eV (within the expected range [12]). Fig. 5 depicts the average V_{FB} values as a function of post-deposition annealing temperature for p-type CZ Silicon sample passivated by 10 nm of PECVD Al_2O_3; the value of φ_{ms} is indicated by a red reference line.

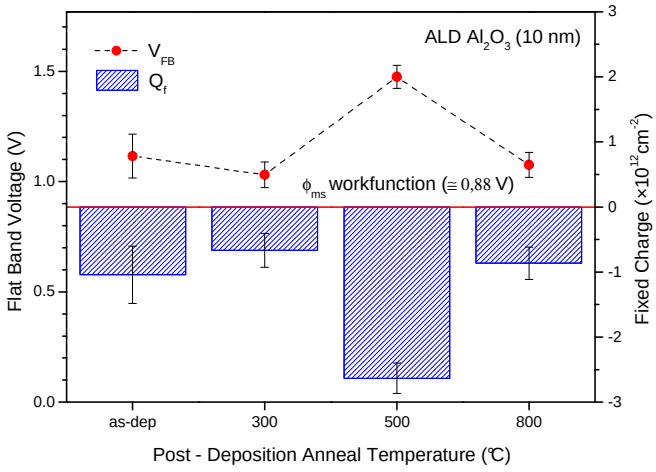

Fig. 5: Average V_{FB} as a function of annealing temperature for 10 nm of PECVD Al_2O_3 deposited on p-type CZ Silicon. Q_f formation in function of anneal temperature is also shown: data points above the reference line (aligned to φ_{ms}) correspond to negative fixed charge density present in the Al_2O_3 layer.

Fig. 5 illustrates that the fixed charge density of these PECVD dielectric films remains (i) almost constant and (ii) negative in polarity for all anneal temperatures. Only after the 500 °C anneal a significant different Q_f is noticed. Unlike ALD Al_2O_3 passivated samples, a negative Q_f is also measured for as-deposited samples (Field Effect passivation present).

PECVD fixed charge density after 500 °C anneal is expected higher than the corresponding ALD one, as reported previously (e.g.) by Dingemans and others [17]. Here, this value is comparable to the ALD counterpart. Even though B. Veith et al. have recently found similar results [18], it is probably due to the technique used to extract fixed charge density in the dielectric. To get precise values, other methods should be followed: e.g. *Corona Charging* [19, 20] or *Second Harmonic Generation* [21].

D_{it} has been estimated for PECVD Al_2O_3 samples, as early described (*A1*). Fig. 6 illustrates D_{it} for 10 – 20 nm PECVD Al_2O_3 samples and compares them with 10 nm ALD (on hydrophilic surface) Al_2O_3. The bar graph depicts a decrease of D_{it} after low temperature treatments (300-500 °C) and a dramatic growth at high temperatures (above 500 °C). Beyond a similar temperature dependency between ALD and PECVD samples, it can be also seen how as-dep D_{it} values of PECVD samples are up to one order of magnitude higher than ALD hydrophilic ones, as reported previously in other works [17][18]. E.g. (i) as-dep 10 nm ALD Al_2O_3 film (hydrophilic surface) has $D_{it} = (1.81 \pm 0.39) \times 10^{11}$ cm^{-2}, (ii) as-dep 10 nm PECVD Al_2O_3 has $D_{it} = (1.46 \pm 0.19) \times 10^{12}$ cm^{-2}. This difference is significant at low temperatures: after thermal treatments it becomes less relevant. This means that (i) PECVD is a deposition technique that provides less surface control than ALD and it needs post deposition anneal treatments to improve D_{it}; (ii) after annealing, D_{it} values from ALD and PECVD become closer [17]. Hence, the implementation of efficient PECVD passivation layers is possible and it has been recently proved also by manufacturing PECVD-PERC cells with efficiencies similar to ALD ones [18].

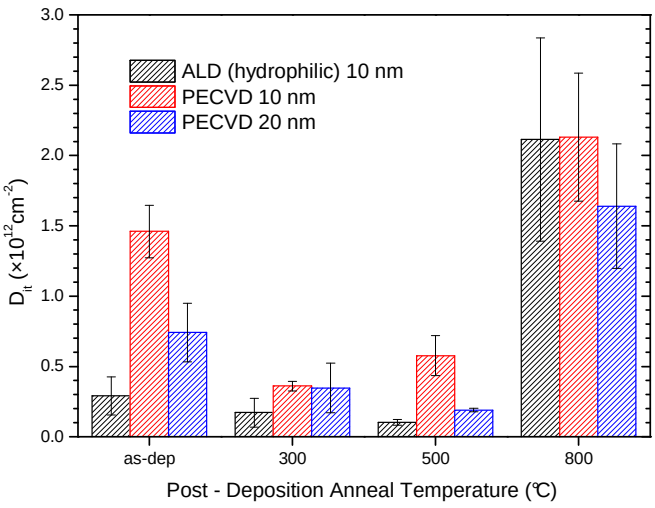

Fig. 6: Average D_{it} as a function of annealing temperature for p-type CZ Silicon samples passivated by 10 nm of ALD Al_2O_3 (hydrophilic surface) and 10 or 20 nm PECVD.

B. Hafnium Oxide as Silicon surface passivation

As a novel candidate for Silicon surface passivation, ALD HfO_2 has been investigated. Given the novelty of this passivation layer, FZ Silicon substrates have been used.

The fixed charge density estimation comes from three different film thicknesses (5, 10 and 15 nm). The flat band

voltage investigation described above has given $\varphi_{ms} \approx 0.61 + 0.029$ eV (considered reasonable [12]). Fig. 7 illustrates the average Q_f and D_{it} for a 10 nm HfO_2 layer as a function of the annealing temperature.

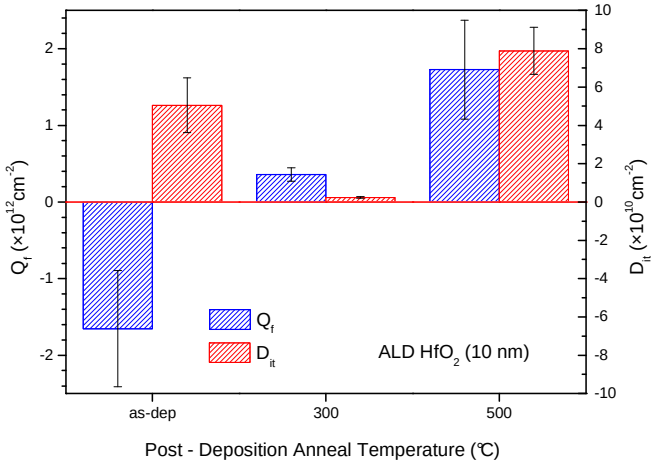

Fig. 7: Q_f and D_{it} as a function of annealing temperature for 10 nm of ALD HfO2 deposited on p-type FZ Silicon.

Fig. 7 shows a different tendency compared to Al_2O_3: as-deposited, a negative fixed charge density is already present. After an anneal at 300 °C, the polarity changes and the positive fixed charge density increases with the temperature.

The D_{it} as a function of annealing temperature is similar to what observed for Al_2O_3: an anneal treatment can improve the quality of Silicon/HfO_2 interface, decreasing D_{it}. Nevertheless, D_{it} values estimated above are much lower than the corresponding densities of Al_2O_3 layers, meaning that an adequate interface quality is always present. However, it has to be considered that HfO_2 has been deposited on FZ Silicon substrates (FZ-Silicon).

Fig. 8 represents the effective carrier lifetime of 10 nm ALD HfO_2 in function of anneal temperature. The figure depicts the highest lifetime value prior to anneal treatments (as-dep), after which a drop can be observed.

The data collected in Fig. 7 fit with the lifetime data depicted in Fig. 8. The only anneal condition providing a sufficient passivation level is as deposit (Fig. 7): (i) this is the only case with a relevant Q_f value, $(-1.65 \pm 0.76) \times 10^{12}$ cm^{-2}; (ii) D_{it} is low in any thermal condition, meaning passivation depends mostly on Q_f. Fig. 8 shows the same tendency: the highest lifetime value measured corresponds to the as-dep layer then, the Silicon passivation is degraded after any temperature treatment

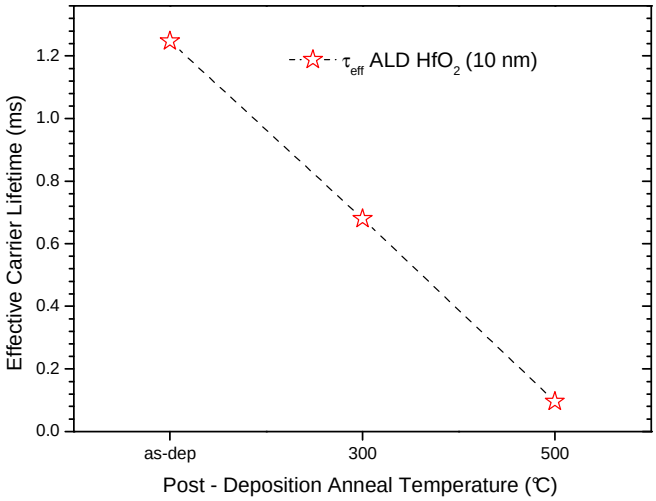

Fig. 8: Effective carrier lifetime at $\Delta n = 1 \times 10^{15}$ cm^{-3} for 10 nm of ALD HfO_2 deposited on p-type FZ Silicon as a function of Anneal Temperature.

VI. Conclusion

It has been shown that a thermal post-deposition treatment is required to reduce the interface trap density (D_{it}) level for all investigated passivation layer deposition methods. The annealing temperature dependency of D_{it} does not depend on the deposition technique. (i) PECVD samples as-deposited have a D_{it} value higher than ALD samples, (ii) after thermal treatments at temperatures below 500 °C D_{it} is reduced, (iii) after annealing temperatures of more than 500 °C D_{it} strongly increase, causing a degrading chemical passivation. The surface roughness investigation shows that after removing 5µm from an alkaline textured surface, the D_{it} of the passivated surface saturates at values of 5×10^{11} cm-2.

The different deposition techniques and the deposited dielectrics show an effect on the fixed charge density. (a) ALD Al_2O_3 requires a thermal treatment to get negatively charged, (b) PECVD Al_2O_3 shows a negative charge density value at every post-deposition temperature. (c) ALD HfO_2 has a negative fixed charge density only as deposited: all post deposition thermal treatments provide a change towards positive charges. Fixed charge density (Q_f) and Interface trap density (D_{it}) have been investigated as key parameters for surface passivation. It has been shown that determining their values, the effective carrier lifetime (τ_{eff}, the main parameter to characterize surface passivation) can be predicted. In every sample, the highest τ_{eff} occurs only with adequate values of Q_f and D_{it}. (i) ALD and PECVD Al_2O_3 show the best lifetime values after a low temperature thermal annealing (300 – 500 °C); (ii) ALD HfO_2 samples have their optimum after the deposition.

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ELECTRICAL CHARACTERIZATION OF ALD Al_2O_3 – HfO_2 AND PECVD Al_2O_3 PASSIVATION LAYERS FOR P-TYPE CZ-SILICON PERC SOLAR CELLS

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(*) Presenting author

This work characterizes p-type Silicon surface passivation using high-k material (Al_2O_3 or HfO_2) combining capacitance - voltage (CV) and lifetime measurements. The samples are based on solar grade materials, close to the real industrially used ones. CV measurements have been used to characterize chemical passivation (= interface trap density, D_{it}) and field effect passivation (= fixed charge density, Q_f). Lifetime measurements have been used to assess the effective surface passivation and to understand the impact of the above mentioned passivation mechanisms on carrier recombination.

Samples investigated
- MOS systems made by Silicon, 10 nm of dielectric (passivation layer) and Platinum metallization.
- Post-deposition anneal temperature dependency analyzed.

Fixed Charge Density (Q_f)
related to Field Effect Passivation

Interface Trap Density (D_{it})
related to Chemical Passivation

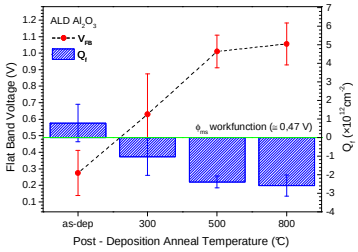
Effective Carrier Lifetime (τ_{eff})
Main Passivation parameter

ALD Al_2O_3

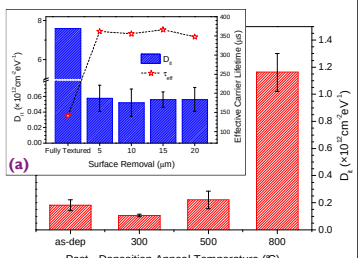
CZ-Si H- terminated

Thermal annealing (in N_2) at 300, 500 and 800 °C

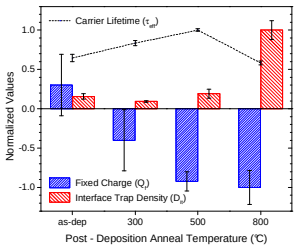
Impact of surface polishing on carrier recombination also considered



Average flat band voltage as a function of anneal temperature. Each shift corresponds to formation of charge density (below in the graph): data points above the reference line (aligned to φ_{ms}) correspond to negative fixed charge density present in the Al_2O_3 layer. ***Thermal annealing is necessary for negative Q_f.***



Estimated average D_{it} as a function of anneal temperature: ***low D_{it} values after annealing ≤ 500 °C.*** Beyond anneal temperature dependency, also polishing impact has been considered (a): ***drop of D_{it} after any polishing process*** ($\Delta n = 1 \times 10^{15}$ cm^{-3}, in picture).

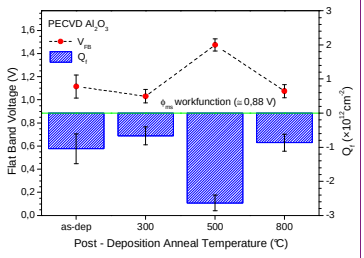


Normalized effective carrier lifetimes (at $\Delta n = 1 \times 10^{15}$ cm^{-3} injection level), Q_f and D_{it}. ***The highest value of τ_{eff} occurs after ≈ 500 °C annealing, with a low level of D_{it} and an adequate negative Q_f.***

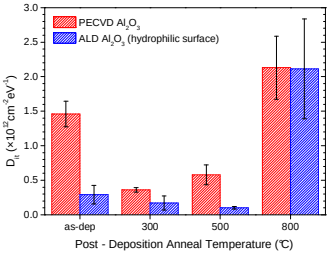
PECVD Al_2O_3

CZ-Si OH- terminated

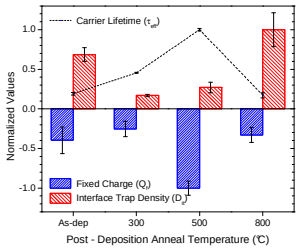
Thermal annealing (in N_2) at 300, 500 and 800 °C



Average V_{FB} as a function of annealing temperature. Data points above the reference line (aligned to φ_{ms}) correspond to negative fixed charge density present in the Al_2O_3 layer. ***Negative Q_f is present also as-deposited. After thermal annealing Q_f is still negative.***



Average D_{it} as a function of annealing temperature (red bars): the values are much higher than the corresponding by ALD (blue bars), especially for as-deposited layers. ***Thermal annealing (≤ 500 °C) is required for low D_{it} values.***



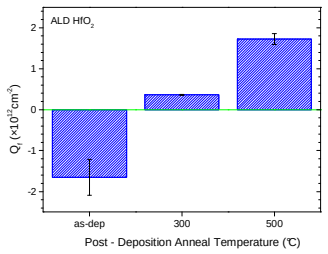
Normalized effective carrier lifetimes (at $\Delta n = 1 \times 10^{15}$ cm^{-3} injection level) Q_f and D_{it}. ***Best τ_{eff} after ≈ 500 °C annealing: high negative Q_f and sufficient low level of D_{it}.***

ALD HfO_2

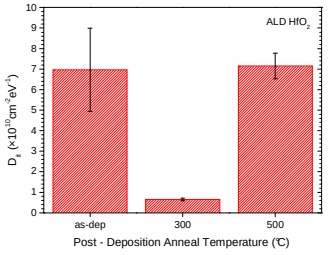
FZ-Si(*) OH- terminated

(*) Being a new material in Si passivation, it has been studied on high quality substrate

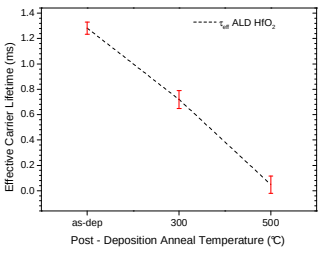
Thermal annealing (in FG, 10% H_2) at 300 and 500 °C.



Average Q_f as a function of anneal temperature: ***negative Q_f is present only in as-deposited layer. Thermal annealing increases Q_f*** also after a low temperature process (≤ 300 °C) Q_f is close to zero.



Average D_{it} as a function of anneal temperature. ***Low levels of D_{it} have been measured in any temperature condition*** (probably, also because of the high quality FZ-Si substrate).



Effective carrier lifetimes (at $\Delta n = 1 \times 10^{15}$ cm^{-3} injection level). ***Best τ_{eff} prior thermal annealing: relevant negative Q_f and sufficient low level of D_{it}.***

Conclusions – Post-deposition anneal treatments can improve both Q_f and D_{it}. (A) A thermal treatment (below 500 °C) is required to reduce D_{it} for all presented passivation layers. (B) The deposition technique and the high-k material affect Q_f: (i) ALD Al_2O_3 shows a negative Q_f after annealing, (ii) PECVD Al_2O_3 has a negative Q_f already as-deposited, (iii) ALD HfO_2 presents a negative Q_f only as-deposited. The influence of Q_f and D_{it} on carrier lifetime has been proved: in every sample the highest τ_{eff} occurs with adequate values of Q_f (negative polarity for p-type Si, ~ - 2 × 10^{12} cm^{-2}) and D_{it} (as low as possible, ~ 2 × 10^{11} cm^{-2}eV^{-1}).

UNIVERSITÀ DEGLI STUDI DI PADOVA

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imec

WCT-120
Silicon Wafer Lifetime Tester

Sinton Consulting, Inc.

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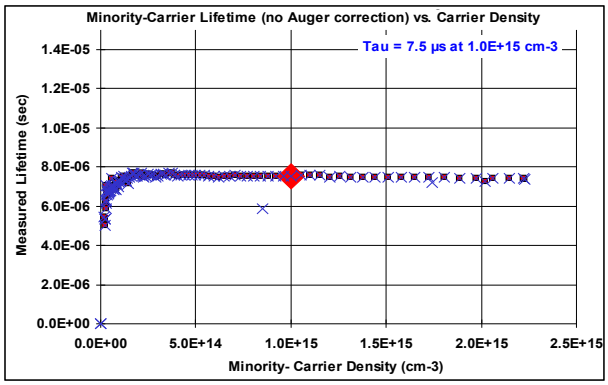
+1.303.945.2199 (fax)
www.sintonconsulting.com

Applications

- Monitoring initial material quality
- Detecting heavy metals contamination during wafer processing
- Evaluating surface passivation and emitter dopant diffusion
- Step-by-step monitoring and optimization of fabrication process
- Providing a contactless, implied IV curve at any stage of solar cell processing

Key Features

- Single-click identification of key characteristics of silicon wafers:
  - Sheet resistance: 3 to 1000 (undoped) Ω/sq
  - Lifetime: 10ns to greater than 10ms
  - Trap density
  - Emitter saturation current density
  - Implied voltage
- Calibrated minority carrier lifetime vs. injection level, independent of carrier profile
- Suitable for single or multicrystalline wafers
- Instantaneous, high-resolution measurement
- Simple, software-controlled sensor tuning



Sinton Consulting's analysis yields a calibrated carrier injection level for each wafer, so you can interpret lifetime data in a physically precise way.

The WCT-120 is an affordable, tabletop silicon lifetime and wafer metrology system, suitable for both device research and industrial process control.

System Components

- WCT-120 instrument, signal connector box, signal cables
- Programmable flashlamp with bandpass filter
- Computer with installed, configured software:
  - Windows OS
  - MS Office
  - Antivirus software
- Sinton Consulting data acquisition and analysis software package
- 12-bit DAQ card with 2-channel simultaneous sampling and common-mode rejection
- Optional: Suns-Voc accessory

WCT-120
Silicon Wafer Lifetime Tester

Sinton Consulting, Inc.

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Product Overview

WCT testers showcase our unique measurement and analysis techniques, including the Quasi-Steady-State photoconductance (QSSPC) lifetime measurement method. This technique is ideal for monitoring multicrystalline wafers, heavy diffusions, or low lifetime samples, and makes the WCT a highly regarded research and process tool.

The QSSPC lifetime measurement also yields the implied open-circuit voltage (vs. illumination) curve, which is comparable to the final I-V curve at each stage of a solar cell process.

The WCT-120 with Suns-Voc accessory stage: the ideal process control setup.

Product Specifications

Wafer size, standard configuration	38-210 cm diameter std. Other sizes possible with user calibration.
Wafer thickness range	10 - 2000 µm (calibrated) Other thicknesses may be measured.
Measurement modes, standard configuration	QSS, Transient, Generalized lifetime analysis
Other standard modes	Bias light hardware and analysis
	White-light and IR illumination
	Emitter saturation current analysis
	Resistivity measurement
Typical calibrated injection range	10^{12}-10^{16} cm^{-3}
A/D converter resolution	12-bit, up to 5MS/s
Ambient operating temperature	20°C - 25°C
Power requirements	WCT-120: 40W Computer with monitor: 200W Light source: 60W
Dimensions	22.5 cm W x 28 cm D x 57 cm H
Universal mains voltage	100-230VAC 50/60Hz
Warranty	One year limited warranty on all parts and software.

CE

Purchase

For a quote, please contact quotes@sintonconsulting.com or fax a request to the number above.

We are happy to accommodate custom requirements, please inquire about a quote for your specific needs.

For our full product line, please visit: www.sintonconsulting.com/products.htm

Quotes are valid for 60 days. Please allow 8-10 weeks for delivery from the purchase order date.

ACCUDRY™

IPA Vapor Dryers

Damage and watermark free substrate drying

Wafer Drying, Engineered Right

As any process engineer can tell you, wafers are only as clean as their last process. That's why the Accudry utilizes the latest in alcohol vapor drying technology to ensure that the last step of your critical process results in clean, damage-free substrates. Using the Accudry after any wet process can improve the performance of ICs, solar cells, fuel cells, MEMS, disk drives, and many more.

How Does the Accudry Work?

The Accudry uses room-temperature IPA vapor to rapidly displace water from the wafer surface until it is completely dry. This technique yields substrates that are watermark-free with extremely low particle counts and zero feature damage.

No Spinning, No Moving Parts

Alcohol vapor drying is ideal for today's thinner substrates. No moving parts or mechanical stress on the wafers means no costly breakage or damage.

Ease of Use

The Accudry has been designed for ease of use and real world functionality. With program-mable recipes and semi automation, operators require minimal training. Operating the Accudry is as simple as load, set, run.

Highly Configurable

The Accudry can process a batch of 25 or 50 wafers depending on configuration. The dryers are configurable to accept one or two cassettes from 150mm to 300mm and can be produced as stand-alone units or integrated into wet processing stations for OEMs.

All Accudry units are backed by Imtec's 40 Years of process module expertise and ISO 9001 quality certification.

ISO 9001
10002862

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IMTEC®

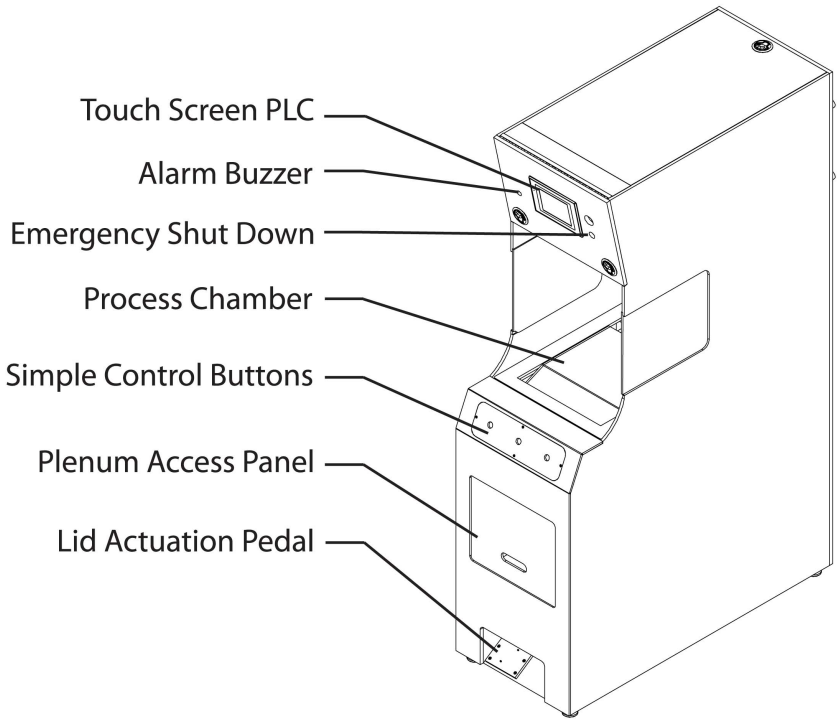
ACCUDRY™

Engineered for Spotless Substrate Rinsing & Drying

IMTEC®

The Advantage

- No watermarks
- Molecular level drying
- No substrate breakage/feature damage
- Effectively dries high aspect ratio structures
- IPA is safely maintained at room temperature
- Extremely low chemical consumption
- Fits in the same footprint as a spin rinser dryer
- Capital cost savings:
  - -Shorter process times
  - -Reduced maintenance
  - -Extremely price competitive



Features

- Automatic, high volume, single or dual cassette configurations
- Adaptable to virtually any substrate material and/or shape
- Available as a stand alone unit or integrated into a wet station
- Programmable recipes including precise control of vapors and gasses
- User-friendly software with touch screen interface

Options

- Quartz in-line water heater
- Integrated megasonic clean unit
- Fire suppression system
- Resistivity probe
- Connection for external IPA bulk fill module
- Custom options available upon request

Available Sizes

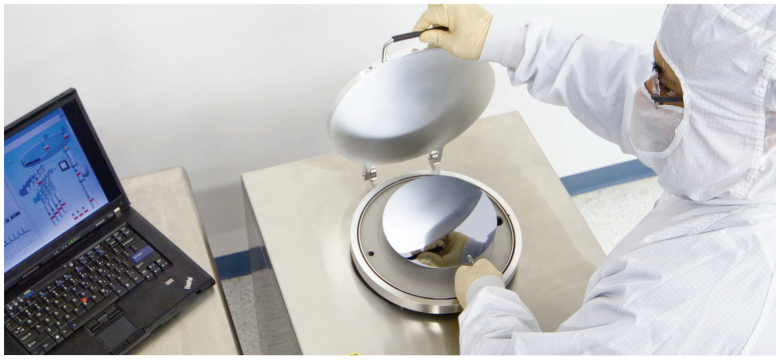
Single / Dual 150mm Cassette
Single / Dual 200mm Cassette
Single / Dual 300mm Cassette
Custom Sizes Upon Request

CambridgeNanoTech
Simply ALD

Savannah™ Series

Product Data

Cambridge NanoTech is the leading provider of atomic layer deposition (ALD) solutions for research and industry worldwide, delivering expert services and versatile, turnkey systems that are accessible, affordable, and accurate to the atomic scale. All Savannah™ ALD systems exemplify these core competencies, making it the platform of choice for those doing ALD research and development.



Accessible

With more than 200 systems shipped worldwide, the Savannah makes ALD accessible to everyone, from experts to those just entering the field. The Savannah system is a flexible and simple system to configure and to operate. It comes with numerous standard recipes and expert support from our team of highly experienced ALD scientists and technologists.

- Each Savannah is designed for maximum experimental flexibility with configurations of up to 6 precursor lines, compact ozone generator, and optional ALD Booster™ low vapor pressure precursor delivery system.
- Savannah systems are in stock and typically ship within seven days. Average time from uncrating to depositing perfect films is just a few short hours.
- Our easy to understand and flexible user interface, combined with readily available recipes and pre-packaged precursors from our partner, Sigma-Aldrich, gets you up and running quickly.

Savannah S100

Affordable

The low cost of entry and reduced operating expense combined with expert advice when you need it, makes the Savannah the best value for those doing serious ALD research, development and production.

- Low Cost of Ownership. Our ALD Shield™ protects expensive pumps and pump lines from deposits, greatly extending the lifetime of your pump.
- Lowest consumption of precursors saves you money compared to similar systems.
- Smallest footprint saves you valuable lab and cleanroom space.
- Cambridge NanoTech's expert team provides first-year system and process support at no additional charge. We are your ALD resource center.

Accurate

ALD offers precise control of depositions down to the atomic scale. Savannah ALD systems are recognized for superior film quality. Such precise control is the result of meticulous design and experience that can only come from knowledgable ALD experts.

Savannah S200

- Savannah systems provide digital control of your thin films which grow one layer at a time and can be controlled to accurate thicknesses.
- Two deposition modes allow precise control of your films from the nano scale to the micro scale. Our unique Exposure Mode™, combined with our proprietary precursor delivery system and precise temperature control, enables conformal film growth on ultra-high aspect ratio features (greater than 2000:1), found in materials such as porous foams, fibers and nanogels.
- Our Continuous Mode™ enables the rapid growth of perfectly dense, uniform, and conformal films.
- Individually precise control of precursor line temperature gives the flexibility to use solid, liquid, or gaseous precursors.

Savannah S300

System Specifications	
Substrate size	Savannah S100: up to 100 mm Savannah S200: up to 200 mm Savannah S300: up to 300 mm
Dimensions (w x d x h)	Savannah S100: 485 x 560 x 965 mm Savannah S200: 585 x 560 x 965 mm Savannah S300: 686 x 560 x 965mm
Cabinet	Stainless steel, built in cooling, removable panels, adjustable feet
Operational Modes	Continuous Mode™ (high speed) or Exposure Mode™ (ultra-high aspect ratio)
Power	115 VAC or 220 VAC,1200 W (excluding pump)
Control	LabVIEW™, USB, Windows™ PC
Substrate Temperature	S100: RT - 450 ˚C; ±1 ˚C (heat zone optionally higher) S200: RT - 400 ˚C; ±1 ˚C (heat zone optionally higher) S300: RT - 400 ˚C; ±1 ˚C (heat zone optionally higher)
Deposition Uniformity (Al_2O_3)	<1% (1σ)
Vacuum Pump	Integrated, minimum 3.5 CFM required
Compatibility	Cleanroom class 100 compatible
Compliance	CE, CSA
Options	Dome lid with wafer cassette, custom reactors, glovebox interface, ALD Shield™ vapor trap
Precursor Specifications	
Precursor Delivery System	2 lines standard, up to 6 lines available. Each line accommodates solid, liquid and gas precursors and is independently heated up to 200 ˚C (higher temperature optionally available.) Metal VCR seals.
Valves	Industry standard high speed ALD valves with 10 msec response time
Precursor Cylinders	Individually heated 50 ml stainless steel cylinders (up to 315 ˚C), optional larger cylinders available
Carrier/Venting Gas	N_2 or Ar mass flow controlled,100 SCCM
Options	ALD Booster™ for low vapor pressure precursors, ozone generator, liquid injection, higher-temperature ALD valves (>200 ˚C), up to 3 gas MFCs

ALD Films

At the forefront of ALD precursor and ALD thin film research, Cambridge NanoTech scientists continuously add to the list of standard ALD recipes:

- Oxides: Al_2O_3, HfO_2, La_2O_3, SiO_2, TiO_2, ZnO, ZrO_2, Ta_2O_5, In_2O_3, SnO_2, ITO, Fe_2O_3, MnO_x, Nb_2O_5, MgO, Er_2O_3, WO_x
- Nitrides: WN, Hf_3N_4, Zr_3N_4, AlN, TiN, NbN_x
- Metals: Ru, Pt, W, Ni, Fe, Co

These films, their nanolaminates, and many more materials and their recipes are available from Cambridge NanoTech's own staff, its partnerships, and its 200+ customer base.

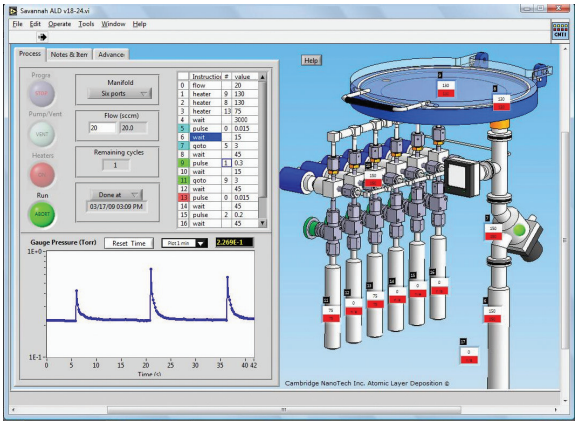
ALD Shield™

Cambridge NanoTech's ALD Shield allows excess reactive vapors to form a film before they reach the pumping system, thus preventing build-up of deposits on the plumbing and in the pump. This saves money in maintenance costs and prevents excess gases from being exhausted to the environment.

The ALD Shield's high conductance, hot foil design causes gases to deposit until depleted. The vapor shield is easily removable for periodic cleaning.

Complete Control

Complete control of all key system parameters is easily achievable through our intuitive Graphical User Interface (GUI). Precise films come from precise control. The Savannah system allows you to control all key system parameters programmatically from substrate temperature to precursor dose with a simple LabVIEW™-based GUI that is powerful, yet simple to use. The LabVIEW program is easily expandable and Cambridge NanoTech provides the LabVIEW source code for complete programmatic flexibility.



Glovebox Integration

The Savannah is readily integrated with MBraun™ gloveboxes for handling thin film samples in an advanced inert atmosphere system that is free of oxygen and moisture.

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High-Throughput, In-line ALD Al_2O_3 System

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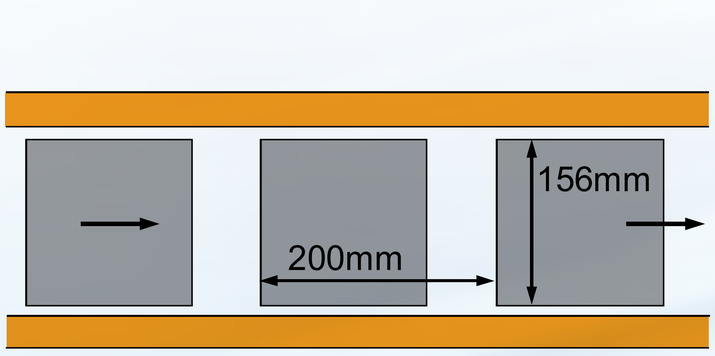
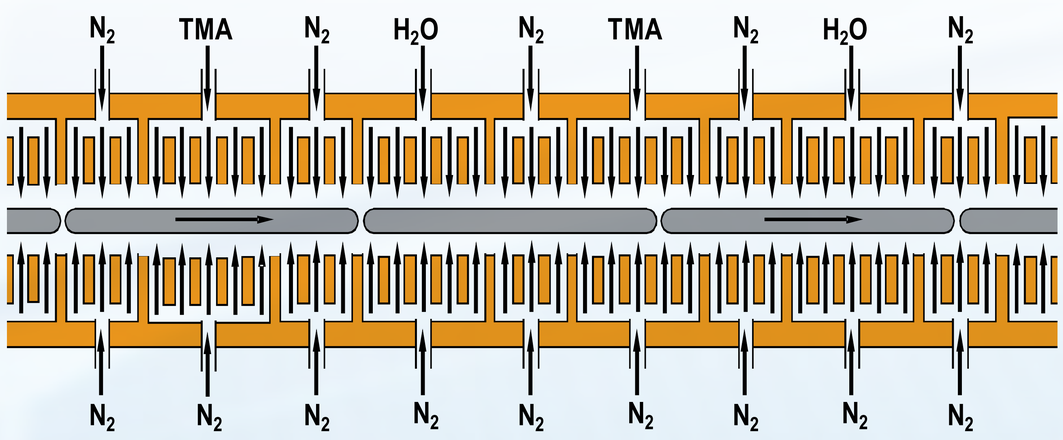
For details visit us at booth: H4/L2/D40

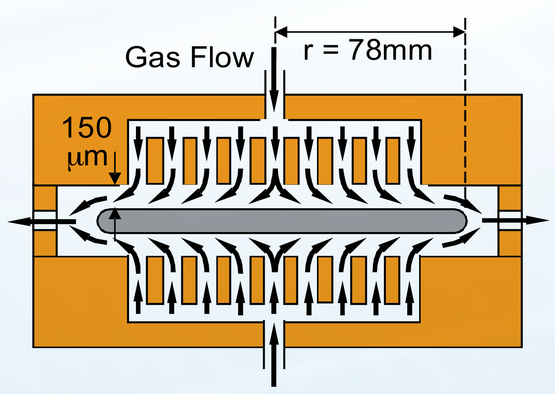
LEVITECH

Levitrack Tool Principles

The ALD process is based on wafers moving in a linear track, floating on gas, passing successive regions of TMA, N_2, H_2O and N_2
After passing a complete ALD cell, a Al_2O_3 layer with a thickness of 0.09-0.12nm is deposited (depending on the temperature)

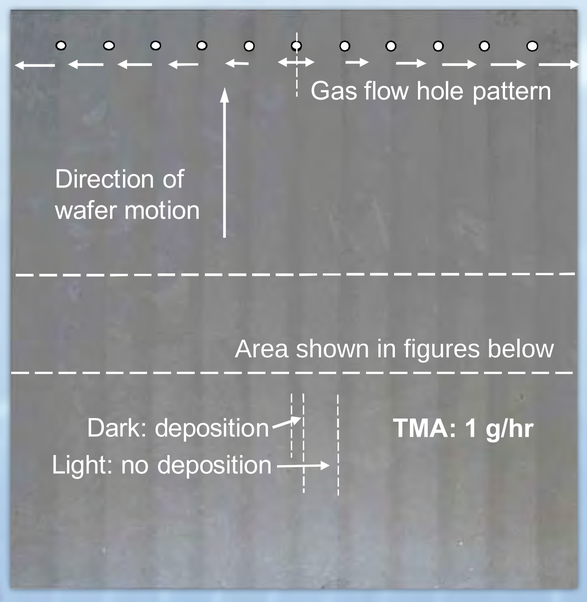


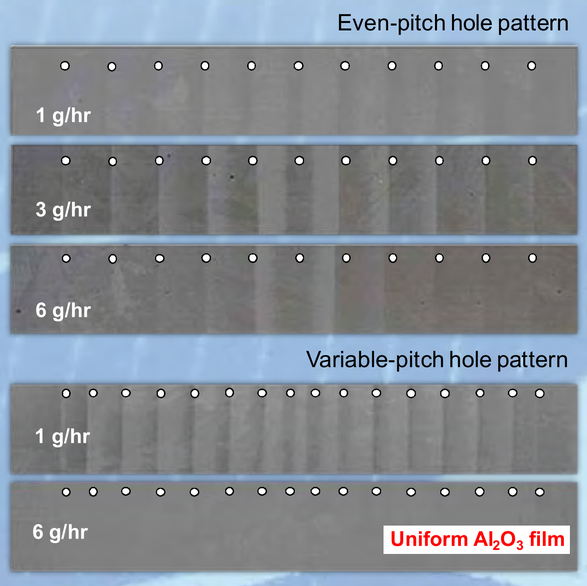




- 10nm is deposited in a system with an (active ALD) length of 10m
- Deposition takes place on one side of the wafer only
- Wafer transport velocity ~ 0.2m/s ≈ **Throughput 3600 wfrs/hr**
- Wafer heats up in ~ 2s ≈ 60cm track length
- No valves to overcome pressure differential with outside world
- System has no moving parts (except the wafers)
- Operation under atmospheric conditions; no vacuum pumps
- No deposition on walls of the system

Characterization Al_2O_3 ALD Process





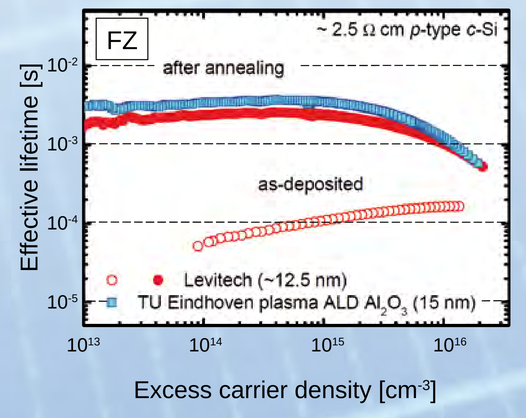
The experiments were done in a 4m system with 2m of ALD cells, each cell 12cm.
· This results in a deposition rate of ~ 1nm/m
· Theoretically, saturation occurs with 100% efficiency at 1.4g/hr TMA, 0.5g/hr H_2O

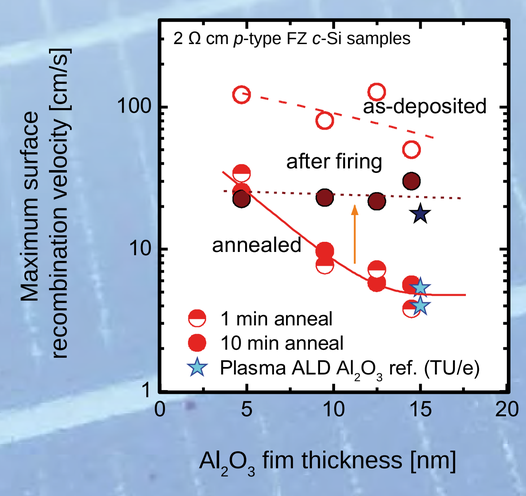
The deposition patterns are consistent with the characteristics of ALD processes:
· At TMA flows of 1g/hr (and saturated H_2O flow), there is insufficient TMA to saturate the are between adjacent injection points
· This results in stripes in the direction of the wafer transport

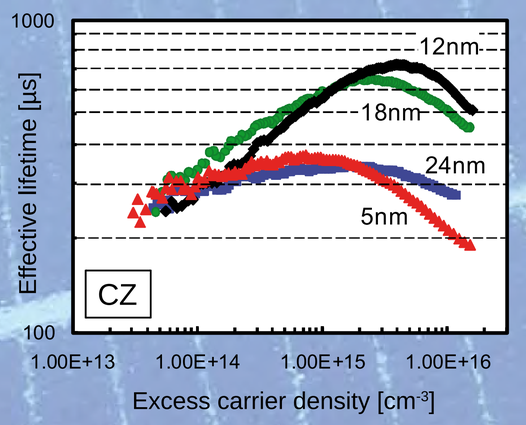
With increasing TMA flow, the area between adjacent stripes is gradually filled
· Note that in case of CVD, the patterns would remain the same, with thicker films growing at the position of the stripes
· In case of ALD, the film thickness remains constant, but the stripes become wider

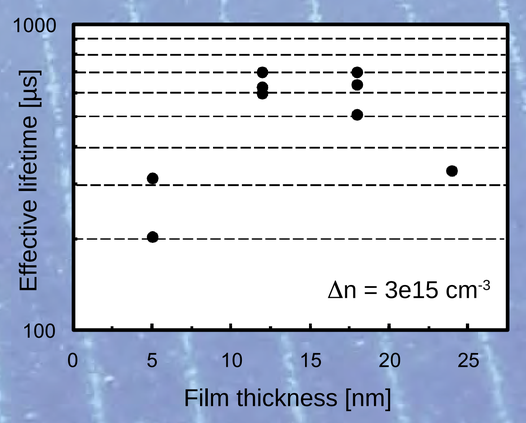
Various hole patterns were investigated
· When the holes are spaced at equal distance (even-pitch pattern), the center hole is not able to provide sufficient TMA to fill the area between its two neighbors
· In a more optimized hole pattern (variable-pitch) the complete wafer area is covered with **a uniform ALD film**

Passivation Performance









ALD Al_2O_3 films were also deposited on 200µm CZ wafers, and analyzed by the **Technical University Eindhoven** (Kessels, Dingemans, published at this conference, paper 2DP.2.1)
The Levitrack Al_2O_3 films were compared with reference PEALD films deposited at the Technical University
· The as-deposited ALD films have lifetimes in the range ~ 100µs
· Upon annealing at 400°C for 10min. the lifetime increases to values > 2ms
· This is comparable with the reference PEALD samples of the TU Eindhoven

Various further testing was done with the samples
· A variation of the annealing time at 400°C has little or no influence
· Upon firing at ~800°C the lifetime decreases with a factor of 4-5; the resulting **recombination velocity is well within spec for advanced passivation applications**
· All results are comparable with the reference PEALD samples
· There appears to be an optimum Al_2O_3 thickness in the range 12-15nm
- **A film thickness of 10nm provides adequate passivation**

ALD Al_2O_3 films were also deposited on 200µm CZ wafers, and analyzed by **ECN**, The Netherlands (results earlier published by Cesar et al, 35th IEEE Photovoltaic Specialist Conference, June, 2010,Hawaii)
· The lifetime is measured after a firing anneal at ~800°C are in the range of 300-700ms; this is relatively high for CZ material
· The stability of these films will be monitored over time

The lifetime was measured as a function of film thickness
· The optimum thickness is similar to that found above, i.e. in the range 12 -18nm
· Overall, it appears that a **film of 10nm will be sufficient**

Cell data with the Levitrack ALD Al_2O_3 films are published by **ECN** at this conference Romijn et al, paper 2DO.1.5

Atomic Layer Deposition Systems

ALD Process Solutions using **FlexAL**® and **OpAL**®

OXFORD INSTRUMENTS

The Business of Science®

Introduction to ALD

Self limiting digital growth

Atomic Layer Deposition (ALD) offers the opportunity to create precisely controlled ultra-thin films for advanced applications on nanometre and sub-nanometre scales, with conformal coating into high aspect ratio structures.

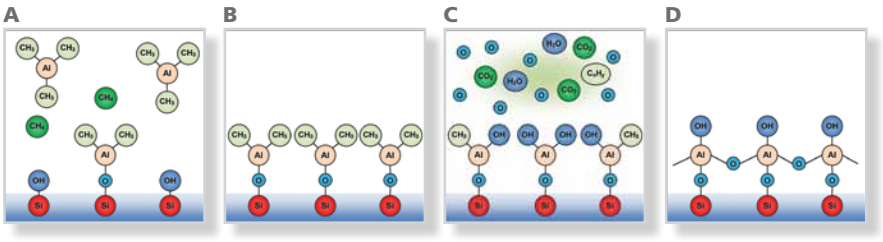
Oxford Instruments' ALD product family offers a unique new range of flexibility and capability in the engineering of nanoscale structures and devices by combining remote plasma ALD processes with thermal ALD.

Exploit the benefits of plasma ALD

The remote plasma option allows for the widest possible choice of precursor chemistry with enhanced film quality:

- Plasma enables low-temperature ALD processes and the remote source maintains low plasma damage[5]
- Effective metal chemistry through use of hydrogen plasma rather than complex thermal precursors
- Eliminates the need for water as a precursor, reducing purge times between ALD cycles
- Higher quality films through improved removal of impurities, leading to lower resistivity, higher density, etc.

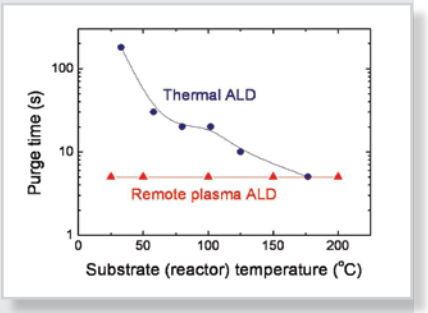
ALD cycle for Al_2O_3 deposited using TMA and O_2 plasma[6]. Only step C varies between H_2O for the thermal process or O_2 plasma.



A. TMA chemisorbtion
B. TMA purge
C. O_2 plasma
D. Short post plasma purge

Example applications of ALD

- Nano-electronics
- High-k gate oxides[1]
- Storage capacitor dielectrics[2]
- High aspect ratio diffusion barriers for Cu interconnects
- Pinhole-free passivation layers for OLEDs and polymers[3]
- Passivation of crystal silicon solar cells[4]
- Highly conformal coatings for microfluidic and MEMS applications
- Coating of nanoporous structures
- Bio MEMS
- Fuel cells



Purge time for thermal ALD of Al_2O_3 (H_2O) and remote plasma ALD of Al_2O_3 (O_2).
Data courtesy of Eindhoven University of Technology

FlexAL and OpAL

Remote plasma and thermal ALD in one tool

FlexAL

A family of tools to meet your needs

The ALD product family encompasses a range of tools to meet the varied demands of academia, corporate R&D and small scale production.

FlexAL tool

- Remote plasma & thermal ALD in one flexible tool
- Automated 200mm load lock for process flexibility
- Clusterable for vacuum transfer of substrates
- Cassette to cassette handling increases throughput suitable for production

OpAL tool

- Open loaded thermal ALD tool with plasma option
- Field upgrade available for plasma option
- Small wafer pieces up to full 200mm wafers – equally suitable for academic and industry R&D

OpAL

FlexAL and OpAL Precursor Delivery

- Multiple liquid or solid precursor delivery systems
- Vapour draw or bubbling up to 200°C source temperature
- Rapid gas delivery

Designed for safe handling of hazardous precursors by enclosing them in a stainless steel extracted cabinet with attachable glove box for use during precursor exchange

ALD Process Benefits

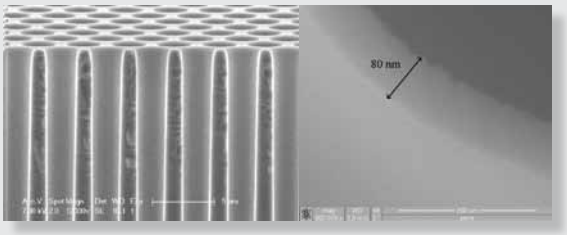
Conformal, controlled, low pin-hole nano-scale growth

General ALD process benefits

- Excellent process control with wafer to wafer repeatability <±1%
- Up to 200mm wafer with typical uniformity <±2%
- Excellent step coverage even inside high aspect ratio structures
- Virtually pin-hole free films
- Low film impurities; particularly with plasma ALD
- Growth at room temperature 25°C possible with plasma ALD

Specific material properties by ALD

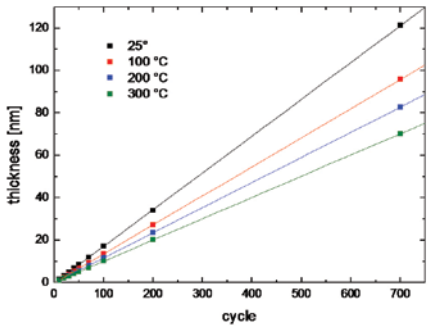
- High k
- High breakdown voltage
- Low resistivity for conductive nitride and metal films by plasma ALD
- Superb thin film barrier properties



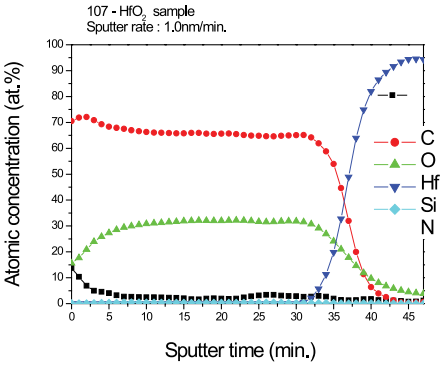
Plasma ALD of 80 nm Al_2O_3 from TMA and O_2 plasma in a 10:1 aspect ratio deep trench capacitor structure. Courtesy of Eindhoven University of Technology and NXP

Parameter	Al_2O_3	HfO_2
Dielectric Contstant	8	18
Breakdown voltage	~9 MV/cm	~3 MV/cm

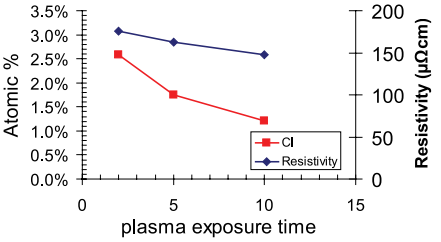
High breakdown voltage[2] of Al_2O_3 and high dielectric constant[1] of HfO_2. HfAlO can provide an average k value, but high breakdown voltage.



Excellent repeatability due to linear self-limiting growth. Example shown of Al_2O_3 by plasma ALD measured by in-situ spectroscopic ellipsometry at deposition temperatures down to room temperature (25°C). Data courtesy of Eindhoven University of Technology[2]

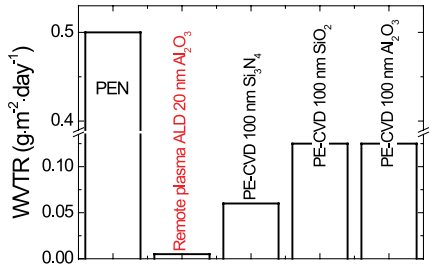


*HfO_2 from TEMAH and O_2 plasma – Auger analysis showing low carbon content of <2% obtained by **FlexAL** remote plasma ALD*



Chlorine impurities of TiN by RBS and resistivity by FPP deposited at 350°C.

Resistivity <200µΩcm possible with plasma ALD even at low temperatures. (350°C plasma = 550°C thermal)



Al_2O_3 barrier deposition at room temperature. Graph shows excellent single layer moisture and oxygen diffusion barrier (20 nm Al_2O_3 with WVTR = 5.0.10.3 g.m-2.day-1).

Data courtesy of Eindhoven University of Technology[4]

Process Library

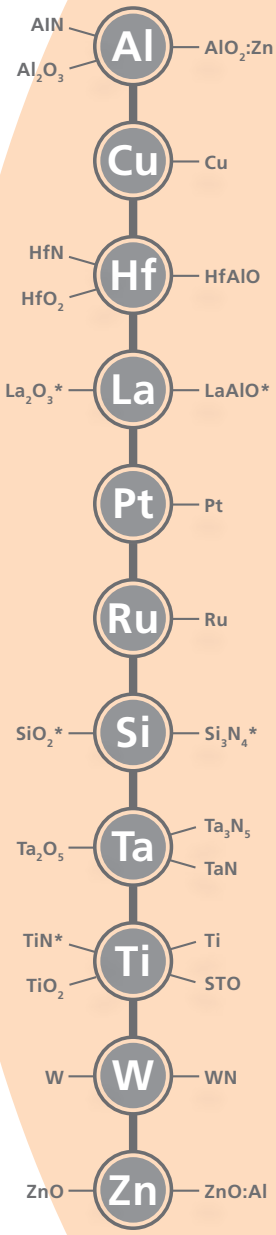
Rapidly populating the periodic table

Oxford Instruments has an extensive process library, and new processes are continually being developed.

Process Development

The list of developed processes is continually expanding; please contact your Oxford Instruments sales representative for the latest information; alternative chemistries may also be available for certain materials. Oxford Instruments provides free on-going process support for the lifetime of any ALD tool offering advice on developing new materials and continued access to our latest ALD process developments including new process recipes.

Global Applications Support - As a global company, processes developed in the UK Applications Laboratory and with collaboration partners are delivered to customers via local front-line support. Oxford Instruments' network of process support engineers is based in the USA, Asia and Europe.



*Requires or strongly benefits from plasma

Precursors

Metal Precursors

Liquid or solid precursors vapours can be delivered to the reaction chamber by heating up to 200°C.

Delivery modes:

- Vapour under own vapour pressure
- Vapour draw with carrier gas assist
- Bubbling with carrier gas

Non-metal Precursors

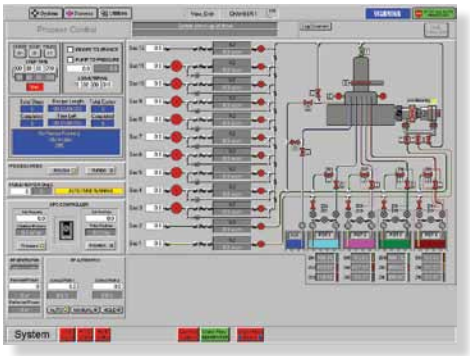
H_2O	Thermal Oxides
Ozone	Thermal Oxides
O_2	Plasma oxides, plasma metals, thermal metals
N_2	Plasma nitrides
H_2	Plasma metals, plasma nitrides, some thermal metals
NH_3	Thermal nitrides and some plasma nitrides

Product Overview

Flexible, configurable, powerful tools

Both **FlexAL** and **OpAL** can be fitted with the Oxford Instruments Plasma Technology remote Inductively Coupled Plasma (ICP) ALD source. This source is close coupled to an Oxford Instruments matching unit with dedicated control systems to enable rapid plasma striking.

Feature	OpAL	FlexAL
Substrates	Up to 200mm wafers and pieces directly on stage	Up to 200mm wafers handling and pieces on carrier plate
Bubbled liquid and solid precursors	Up to 4	Up to 8
Max precursor source temperature	200°C (jacket)	200°C (oven and jacket)
Additional precursors	Water + ozone	Water + ozone
Mfc controlled gas lines with rapid delivery system; 1) thermal gas precursors (e.g. NH_3, O_2) 2) plasma gases (e.g. O_2, N_2, H_2)	2 internally. Up to 8 in externally mounted gas pod	Up to 10 in externally mounted gas pod
Plasma	Option / field upgrade	Option
Loading	Open load	Loadlock or cassette
In situ diagnostic ports	Ellipsometry, QCM, OES, QMS (on foreline)	Ellipsometry, QCM, OES, QMS
Swagelok 10ms rapid pulsing ALD valves	Yes	Yes
Removable inner chamber	Yes	Yes
PC2000 rapid control software	Yes	Yes
Clusterable to other process modules	No	Yes - including third party MESC modules as special option
Wafer stage temperature range	25°C – 400°C (500°C option)	25°C – 400°C (550°C option)



*Powerful **PC**2000 Software*

Power ahead with intuitive software

Easy to use, multi-user level, **PC**2000™ cross platform control software is tailored for rapid cycle ALD.

Be reassured with global support

Local engineers based worldwide.

Save time with process guarantees

Developed in our applications laboratory and backed by on-site process acceptance and support.

Configuration Options

Systems easily configured for cutting edge research or production

FlexAL

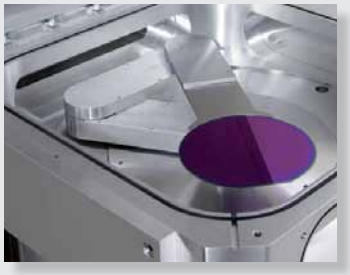
Research Solutions

Single wafer loadlock

Entry handler clustered to other process modules

Production Solutions

All configurations can be located entirely within the cleanroom or through-the-wall



Handler with robot and 25 wafer cassette for 4", 6" or 8" wafers

OpAL

*A nitrogen purged glove box can surround the **OpAL** chamber for dry loading of samples, giving lower oxygen contamination in nitride and metal films.*

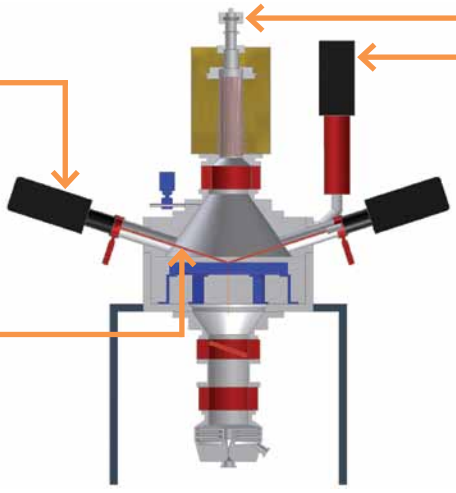
In situ options

Ellipsometer

- Nucleation delay
- In situ resistivity
- Linear growth
- Saturation growth

Quartz Crystal Microbalance (QCM)

- Saturation growth
- Linear growth
- Reaction mechanism



Optical emission spectroscopy (OES)

- Saturation growth
- Reaction mechanism

Mass Spectrometer (QMS)

- Reaction mechanisms
- Background chamber condition
- Precursor condition

■ Plasma Etch & Deposition ■ Atomic Layer Deposition ■ Ion Beam Etch & Deposition ■ Nanoscale Growth Systems ■ HVPE

Global Service and Support

For more information about our ALD tools, please contact your local Oxford Instruments office

Worldwide Service and Support

Oxford Instruments is committed to supporting our customers' success. We recognise that this requires world class products complemented by world class support. Our global service force is backed by regional offices, offering rapid support wherever you are in the world.

We can provide:

- Tailored service agreements to meet your needs
- Comprehensive range of structured training courses
- Immediate access to genuine spare parts and accessories
- System upgrades and refurbishments

REFERENCES

[1] Deposition of TiN and HfO_2 in a commercial 200 mm remote plasma atomic layer deposition reactor. S.B.S. Heil, J.L. van Hemmen, C.J. Hodson, N. Singh, J.H. Klootwijk, F. Roozeboom, M.C.M. van de Sanden and W.M.M. Kessels, J. *Vac. Sci. Technol.* A, 1357, (**2007**).

[2] Plasma and thermal ALD of Al_2O_3 in a commercial 200 mm ALD reactor J.L. van Hemmen, S.B.S. Heil, J.H. Klootwijk, F. Roozeboom, C.J. Hodson, M.C.M. van de Sanden and W.M.M. Kessels, J. *Electrochem. Soc.* 154, G165 (*2007*).

[3] Plasma-assisted atomic layer deposition of Al_2O_3 moisture permeation barriers on polymers . E. Langereis, M. Creatore, S.B.S. Heil, M.C.M. van de Sanden, and W.M.M. Kessels, *Appl. Phys.* Lett. 89, 081915 (**2006**).

[4] Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al_2O_3. J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M.C.M. van de Sanden and W.M.M. Kessels, *Prog. Photovolt: Res. Appl.* (**2008**)

[5] Remote Plasma Atomic Layer Deposition of Hafnium Oxide, Hyeongtag Jeon, AVS 5th International Conference on Atomic Layer Deposition 2005.

[6] Reaction mechanisms during plasma-assisted atomic layer deposition of metal oxides: A case study for Al_2O_3. S.B.S. Heil, J.L. van Hemmen, M.C.M. van de Sanden and W.M.M. Kessels, J. *Appl. Phys.* 103 (**2008**) 103302

www.oxford-instruments.com/plasma for more information

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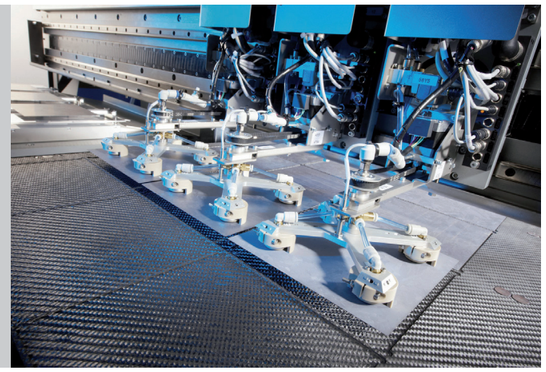
PECVD coating equipment

Integrated automation solutions

- Inline and batch operation
- Contact and contact-less grippers
- Link to wet chemistry (variable number of lanes)
- Cassette loading and unloading
- Coin unloading
- All major cassette and coin types available
- Transfer, buffer, and flip modules enable multi-layer applications



DEP$_X$ 2000 series – The low cost cell manufacturing solution

- Lowest cost of ownership
- High uptime
- Easy to operate and maintain
- Highest deposition rate
- Small footprint
- Automation included
- Integrated electrical cabinet
- Modular design
- Scalable to 70 MWp
- SiNx and SiOx capability
- High process uniformity
- Single and multi-layer capable
- Inline metrology (optional)

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The world's highest speed PECVD system

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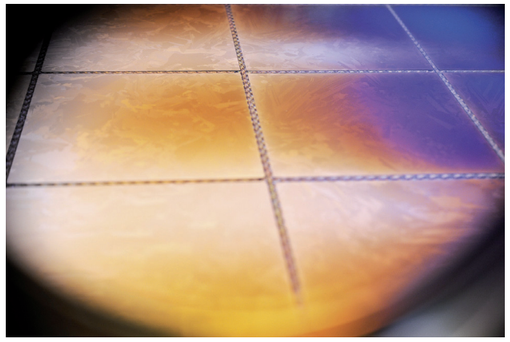
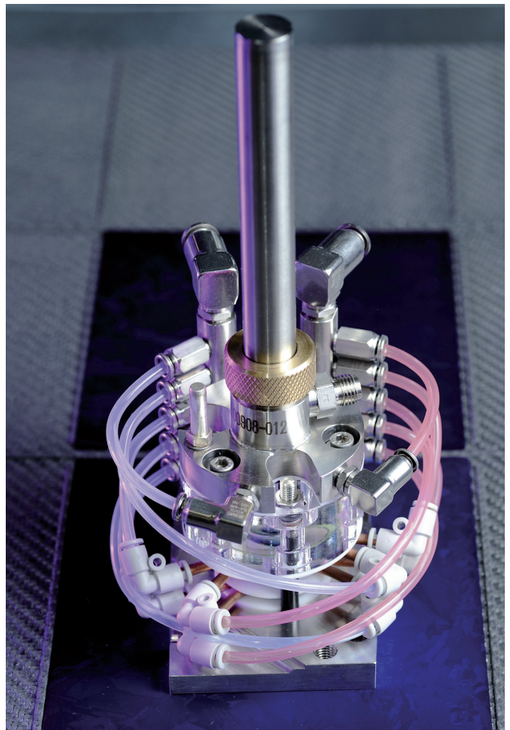




OTB Solar – Roth & Rau has developed a new generation of PECVD equipment for the deposition of antireflective coatings and passivating layers on crystalline solar cells. The DEP_X 2000 is a further evolution of the DEP_X 1000 series, which has a proven track record in high efficiency solar cell production. The DEP_X 2000 series provides an improved throughput, higher uptime, and a lower cost of ownership.

The equipment has a modular design which allows for easy configurability. The DEP_X 2000 series combines an innovative linear motion system (LMS) and the proprietary Expanding Thermal Plasma (ETP) technologies to provide the highest process speed and superior reliability.

Expanding Thermal Plasma

The PECVD process is based on the proprietary ETP source technology, which is a dc Ar plasma discharge.

The low voltage high pressure Ar plasma expands at supersonic speed through a narrow channel into the deposition chamber. At the exit nozzle a second gas is injected into the plasma stream. A third gas is injected just above the substrates. By choosing the right combination of precursor gasses the system can deposit amorphous hydrogenated silicon nitride (SiNx) as well as silicon oxide (SiOx). Other layers are currently under development.

The ETP source is a remote plasma, which means that plasma production, transport, and deposition are geometrically separated. The substrate does not play a role in plasma production and ion bombardment of high-energy particles on the substrate is virtually absent.

LMS technology

The system works with a Linear Motor System (LMS), a patented technology. The carriers are transported on a rail system in vacuum without any feed-through to the outside. The motion of the carriers is achieved by a magnetic system placed outside the vacuum. Therefore the transport system is almost maintenance free and reduces the risk of a vacuum leak to a minimum.

Specifications

Configurations & Options

Throughput	1600 - 2400 wafer/h
Process capability	3 – 5 ETP sources
Process	SiNx, SiOx
Software	MES Lite, SECS-GEM, RFID, wafer tracking

Equipment*

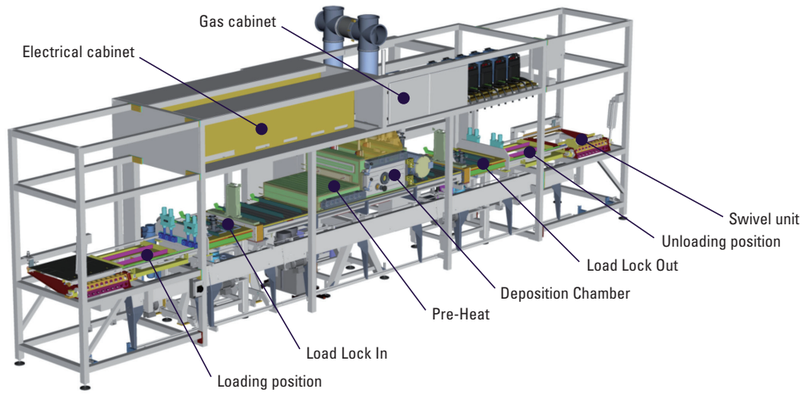
Footprint	10.0 m x 2.3 m
Weight	9950 kg
Yield	> 99%
Breakage	< 0.3%
Uptime	> 90%

*Process equipment including automation

Process

Capability	SiNx, SiOx
Deposition rate	up to 10 nm/s
Thickness	60 nm – 90 nm
Thickness Uniformity	± 2.5%
Refractive index uniformity	± 1%
Process temperature	< 500°C

Overview of DEP_X 2000 system modules from the front side



Cascade Microtech, Inc.

SPECIFICATION SHEET

The ultimate tool for 300 mm device characterization and reliability test

PA300PS

300 mm Semi-automatic Probing System

The PA300PS is the world's best device characterization tool, combining excellent positioning accuracy with excellent measurement accuracy for device modeling and wafer level reliability (WLR) tests.

The unique design of the PA300PS is enhanced with ProbeShield® technology, providing a fully electromagnetically shielded, ultra low-noise, light-tight environment. This means your measurements are more accurate, resulting in more efficient model extraction, faster model turnaround and less design iterations, faster time to market and ultimately a higher return on investment on your devices. In order to fully implement a sound EMI/RFI shield, all high-precision DC servos are shielded by ProtecDrive™ and augmented automatically with QuietMode™, which safely removes all power to servos, motorized ProbeHeads™ and the motorized microscope movement to prevent any degradation of the spectral noise floor.

Since the PA300PS has been designed to provide best-in-class measurements, it is easy to integrate the sensitive measurement equipment inside the shielded environment of the ProbeShield system. This significantly reduces cable lengths, which increases measurement dynamic, and eliminates the need for an additional, expensive shielded room for measurements such as low-frequency flicker (1/f) noise.

Handling fragile and expensive wafers is easy with the patented PA300PS loading mechanism. While the chuck and integrated CeramPlate™ stay inside the system, a loading plate smoothly glides out to comfortably load substrates and/or wafers. By using a small opening for loading and unloading, we minimize the pollution of the test environment with warm, moist air. Reconditioning after wafer change starts immediately without requiring additional time for purging the system with dry air. Since the sensitive CeramPlate stays in the system, damage or contamination is minimized, significantly reducing repair and maintenance costs.

FEATURES AND BENEFITS

Efficient model extraction with highly accurate parameter measurements	Low-noise test environment with advanced EMI-shielding concept and CeramPlate, which eliminates thermal chuck's interference
	AccuraCV™ and SussCal® control of 4294A provide accurate high-k, thin oxide C-V characterization
	Unique measurement equipment integration with shortest cable lengths for best measurement dynamic and accuracy
	1/f set-up with ProPlus NoisePro eliminates need for additional shielding room and provides best-in-class measurement accuracy
	LRM+™ and RRMT+™ for accurate wafer-level calibration
Automated generation of modeling and reliability data	Unattendend test at different temperatures (-60°C to +300°C) with Automated Thermal Management™ and optional ReAlign™ for thermal shift compensation
	Automated calibration substrate alignment
	Interfaces with all leading data acquisition and modeling software
	Extended microscope movement and multi-site, high-temperature probe cards for reliability parallelization
Fine-pitch probing on small pads	Best-in-class mechanical precision for accurate positioning
	Highest Z accuracy for reducing skating of probe needles on pads
Easy and safe operation	Unique handling of probe cards and ProbeHeads: Patented ContactView™ and ProbeHorizon™ options for easy and safe contact setting Integrated probe card holder - no mechanical change over Simultaneous use in EMI-shielded environment

SPECIFICATIONS*

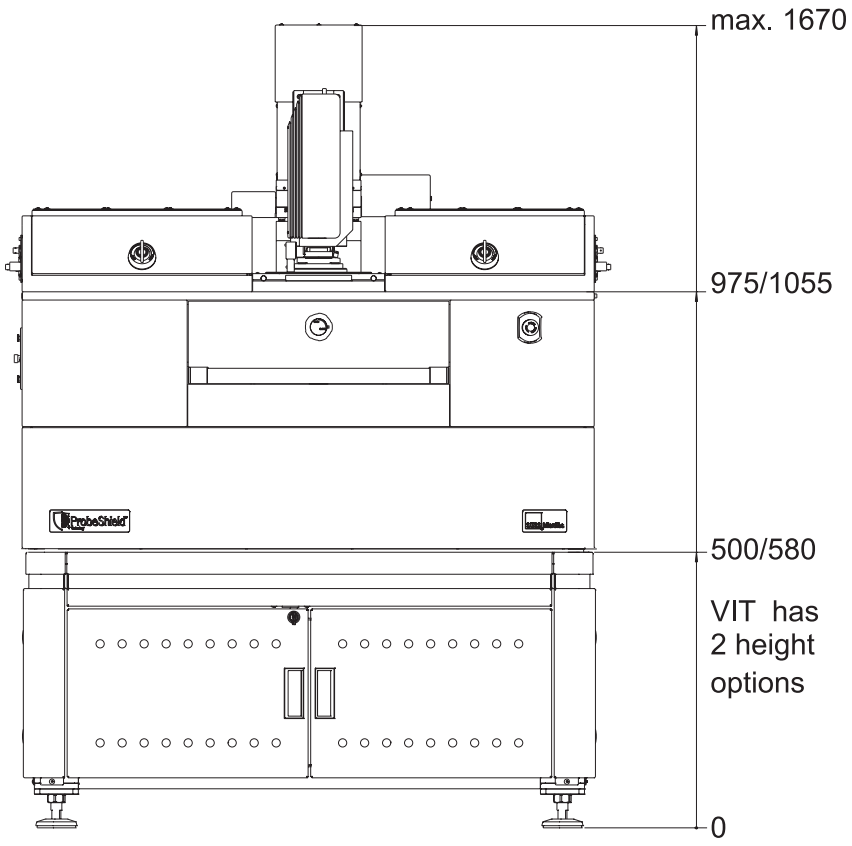
General Features		
	Substrate sizes	Single chips to 300 mm wafers
	Temperature range	-60°C to 300°C
	Automated temperature test	ReAlign (optional), Automated Thermal Management
Chuck Stage		
	X-Y Movement	Closed-loop, DC servo with linear encoder feedback
	Travel / Resolution	305 mm x 305 mm / 0.5 µm
	Repeatability	± 1 µm
	Accuarcy	± 2 µm
	Planarity	± 15 µm
	Maximum speed	50 mm/sec
	Z Movement	DC servo with rotary encoder feedback
	Travel / Resolution	12 mm / 0.25 µm
	Repeatability	± 1 µm
	Theta Movement	DC servo with rotary encoder feedback
	Travel / Resolution	7.5° / 0.0001°
Programmable Microscope Movement		Closed-loop, DC servo with rotary encoder feedback
	Travel / Resolution	50 mm x 80 mm (iVista™, A-Zoom) / 0.25 µm
	Access lift	130 mm motorized
Utilities		
	Vacuum	Less than 200 mbar abs
	Dry air	6^{-10} bar; dewpoint lower than - 65° C; maximum flow rate 180 liters/min at SATP
		(depending on system configuration)
	Power	100/240 V, 50/60 Hz, maximum 1500 VA (depending on system configuration)

*Data, design and specification depend on individual process conditions and can vary according to equipment configurations.
Not all specifications may be valid simultaneously.

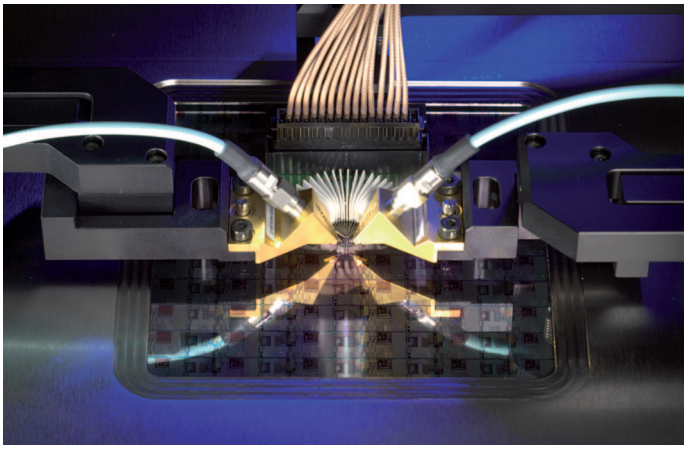
PHYSICAL DIMENSIONS

Weight	Maximum 1000 kg (depending on system configuration)

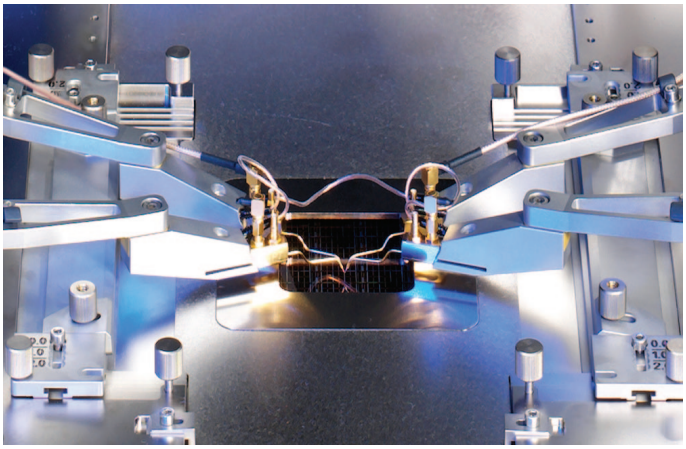
Dimensions (mm)



APPLICATIONS



Device characterization in an EMI-/RFI-shielded environment using the |**Z**| Probe® and ProbeWedge™.



Setting up complex measurements such as pulsed I-V is no challenge with the advanced ergonomic design of the PA300PS.

PA300PS-SS-0310

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Agilent 4284A
Precision LCR Meter

Data Sheet

Specifications

The complete Agilent Technologies 4284A specifications are listed in this data sheet. These specifications are the performance standards or limits against which the instrument is tested. When shipped from the factory, the Agilent 4284A meets the specifications listed here.

Measurement Functions

Measurement parameters

|Z| = Absolute value of impedance
|Y| = Absolute value of admittance
L = Inductance
C = Capacitance
R = Resistance
G = Conductance
D = Dissipation factor
Q = Quality factor
R_s = Equivalent series resistance
R_p = Parallel resistance
X = Reactance
B = Susceptance
θ = Phase angle

Combinations of measurement parameters

|Z|, |Y|	L, C	R	G
θ (deg), θ (rad)	D, Q, R_s, R_p, G	X	B

Mathematical functions

The deviation and the percent of deviation of measurement values from a programmable reference value.

Equivalent measurement circuit

Parallel and series

Ranging

Auto and manual (hold/up/down)

Trigger

Internal, external, BUS (GPIB), and manual

Delay time

Programmable delay from the trigger command to the start of the measurement, 0 to 60.000 s in 1 ms steps.

Measurement terminals

Four-terminal pair

Test cable length

Standard 0 m and 1 m selectable
With Option 4284A-006 0 m, 1 m, 2 m, and 4 m selectable

Integration time

Short, medium, and long (see *Supplemental Performance Characteristics* for the measurement time)

Averaging

1 to 256, programmable

Agilent Technologies

Test Signal

Frequency

20 Hz to 1 MHz, 8610 selectable frequencies

Accuracy

±0.01%

Signal modes

Normal (non-constant) – Program selected voltage or current at the measurement terminals when they are opened or shorted, respectively.

Constant – Maintains selected voltage or current at the device under test (DUT) independent of changes in the device's impedance.

Signal level

	Mode	Range	Setting accuracy
Voltage	Non-constant	5 mV_{rms} to 2 V_{rms}	±(10% + 1 mV_{rms})
	Constant[1]	10 mV_{rms} to 1 V_{rms}	±(6% + 1 mV_{rms})
Current	Non-constant	50 μA_{rms} to 20 mA_{rms}	±(10% + 10 μA_{rms})
	Constant[1]	100 μA_{rms} to 10 mA_{rms}	±(6 % + 10 μA_{rms})

1. Automatic Level Control Function is set to ON.

Output impedance

100 Ω, ±3%

Test signal level monitor

Mode	Range	Accuracy
Voltage[1]	5 mV_{rms} to 2 V_{rms}	±(3% of reading + 0.5 mV_{rms})
	0.01 mV_{rms} to 5 mV_{rms}	±(11% of reading + 0.1 mV_{rms})
Current[2]	50 μA_{rms} to 20 mA_{rms}	±(3% of reading + 5 μA_{rms})
	0.001 μA_{rms} to 50 μA_{rms}	±(11% of reading) + 1 μA_{rms})

1. Add the impedance measurement accuracy [%] to the voltage level monitor accuracy when the DUT's impedance is < 100 Ω.
2. Add the impedance measurement accuracy [%] to the current level monitor accuracy when the DUT's impedance is ≥ 100 Ω.

Accuracies apply when test cable length is 0 m or 1 m. The additional error when test cable length is 2 m or 4 m is given as

$$fm \times \frac{L}{2} \ [\%]$$

where:

fm = Test frequency [MHz]

L = Test cable length [m]

For example,

DUT's impedance:	50 Ω
Test signal level:	0.1 V_{rms}
Measurement accuracy:	0.1%
Cable length:	0 m

Then, voltage level monitor accuracy is

±(3.1% of reading + 0.5 mV_{rms})

Display Range

Parameter	Range
|Z|, R, X	0.01 mΩ to 99.9999 MΩ
|Y|, G, B	0.01 nS to 99.9999 S
C	0.01 fF to 9.99999 F
L	0.01 nH to 99.9999 kH
D	0.000001 to 9.99999
Q	0.01 to 99999.9
θ	–180.000° to 180.000°
Δ	–999.999% to 999.999%

Absolute Accuracy

Absolute accuracy is given as the sum of the relative accuracy plus the calibration accuracy.

|Z|, |Y|, L, C, R, X, G, and B accuracy

|Z|, |Y|, L, C, R, X, G, and B accuracy is given as

$A_e + A_{cal}$ [%]

where:

A_e = Relative accuracy
A_{cal} = Calibration accuracy

L, C, X, and B accuracies apply when D_x (measured D value) ≤ 0.1. R and G accuracies apply when Q_x (measured Q value) ≤ 0.1. G accuracy described in this paragraph applies to the G-B combination only.

D accuracy

D accuracy is given as

$D_e + \theta_{cal}$

where:

D_e is the relative D accuracy
θ_{cal} is the calibration accuracy [radian]

Accuracy applies when D_x (measured D value) ≤ 0.1.

Q accuracy

Q accuracy Q_e is given as

$$Q_e = \pm \frac{Q_x^2 \times D_a}{1 \mp Q_x \times D_a}$$

where:

Q_x = Measured Q value
D_a = D accuracy

Q accuracy applies when $Q_x \times D_a < 1$.

θ accuracy

θ accuracy is given as

$\theta_e + \theta_{cal}$ *[deg]*

where:

θ_e = Relative θ accuracy [deg]
θ_{cal} = Calibration accuracy [deg]

G accuracy

When D_x (measured D value) ≤ 0.1

G accuracy is given as

$$B_x \times D_a \quad [S]$$

$$B_x = 2\pi f C_x = \frac{1}{2\pi f L_x}$$

where:

B_x = Measured B value [S]
C_x = Measured C value [F]
L_x = Measured L value [H]
D_a = Absolute D accuracy
f = Test frequency [Hz]

G accuracy described in this paragraph applies to the C_p-G and L_p-G combinations only.

R_p accuracy

When D_x (measured D value) ≤ 0.1

R_p accuracy is given as

$$R_p = \pm \frac{R_{px} \times D_a}{D_x \mp D_a} \quad [\Omega]$$

where:

R_{px} = Measured R_p value [Ω]
D_x = Measured D value
D_a = Absolute D accuracy

R_s accuracy
When D_x (measured D value) ≤ 0.1

R_s accuracy is given as

$$X_x \times D_a \quad [\Omega]$$

$$X_x = 2\,\pi f L_x = \frac{1}{2\,\pi f C_x}$$

where:

X_x = Measured X value [Ω]
C_x = Measured C value [F]
L_x = Measured L value [H]
D_a = Absolute D accuracy
f = Test frequency [Hz]

Relative Accuracy

Relative accuracy includes stability, temperature coefficient, linearity, repeatability, and calibration interpolation error. Relative accuracy is specified when all of the following conditions are satisfied:

1. Warm-up time: ≥ 30 minutes

2. Test cable length: 0 m, 1 m, 2 m, or 4 m (Agilent 16048 A/B/D/E)

For 2 m or 4 m cable length operation, test signal voltage and test frequency are set according to Figure 1-1. (2 m and 4 m cable can only be used when Option 4284A-006 is installed.)

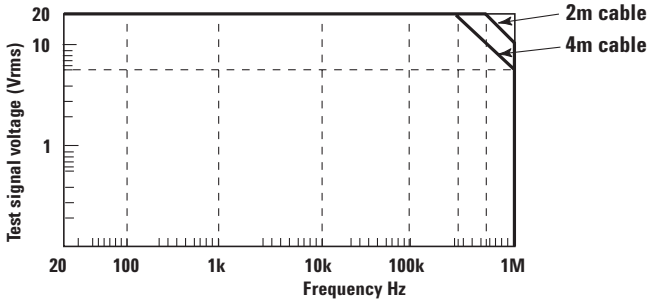


Figure 1-1. Test signal voltage and test frequency upper limits to apply relative accuracy to 2 m and 4 m cable length operation

3. OPEN and SHORT corrections have been performed.

4. Bias current isolation: Off

(For accuracy with bias current isolation, refer to supplemental performance characteristics.)

5. Test signal voltage and DC bias voltage are set according to Figure 1-2.

6. The optimum measurement range is selected by matching the DUT's impedance to the effective measuring range. (For example, if the DUT's impedance is 50 kΩ, the optimum range is the 30 kΩ range.)

Range 1: Relative accuracy can apply.

Range 2: The limits applied for relative accuracy differ according to the DUT's DC resistance. Three dotted lines show the upper limits when the DC resistance is 10 Ω, 100 Ω and 1 kΩ.

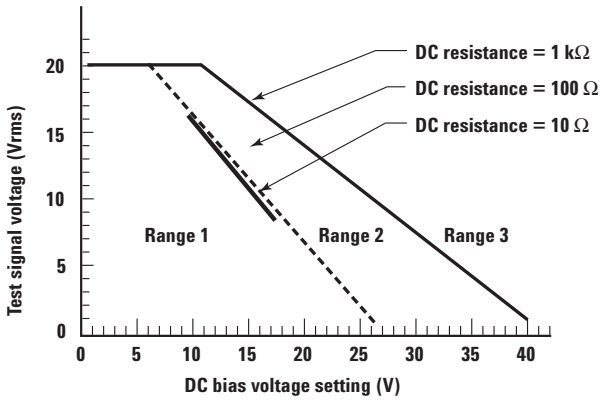


Figure 1-2. Test signal voltage and DC bias voltage upper limits apply for relative accuracy

|Z|, |Y|, L, C, R, X, G, and B accuracy

|Z|, |Y|, L, C, R, X, G, and B accuracy A_e is given as

$$A_e = \pm [A + (K_a + K_{aa} + K_b \times K_{bb} + K_c) \times 100 + K_d] \times K_e \ [\%]$$

A = Basic accuracy (refer to Figure 1-3 and 1-4)
K_a = Impedance proportional factor (refer to Table 1-1)
K_{aa} = Cable length factor (refer to Table 1-2)
K_b = Impedance proportional factor (refer to Table 1-1)
K_{bb} = Cable length factor (refer to Table 1-3)
K_c = Calibration interpolation factor (refer to Table 1-4)
K_d = Cable length factor (refer to Table 1-6)
K_e = Temperature factor (refer to Figure 1-5)

L, C, X, and B accuracies apply when D_x (measured D value) ≤ 0.1.

R and G accuracies apply when Q_x (measured Q value) ≤ 0.1.

When $D_x \geq 0.1$, multiply A_e by $\sqrt{1 + D_x^2}$ for L, C, X, and B accuracies

When $Q_x \geq 0.1$, multiply A_e by $\sqrt{1 + Q_x^2}$ for R and G accuracies.

G accuracy described in this paragraph applies to the G-B combination only.

D accuracy

D accuracy D_e is given as

$$D_e = \pm \frac{A_e}{100}$$

Accuracy applies when D_x (measured D value) ≤ 0.1.

When $D_x > 0.1$, multiply D_e by $(1 + D_x)$.

Q accuracy

Q accuracy is given as

$$\pm \frac{Q_x^2 \times D_e}{1 \mp Q_x \times D_e}$$

where:

Q_x = Measured Q value
D_e = Relative D accuracy

Accuracy applies when $Q_x \times D_e < 1$.

θ accuracy

θ accuracy is given as

$$\frac{180 \times A_e}{\pi \times 100} \ [deg]$$

G accuracy

When D_x (measured D value) ≤ 0.1

G accuracy is given as

$$B_x \times D_e \ [S]$$

$$B_x = 2 \pi f C_x = \frac{1}{2 \pi f L_x}$$

where:

B_x = Measured B value [S]
C_x = Measured C value [F]
L_x = Measured L value [H]
D_e = Relative D accuracy
f = Test frequency [Hz]

G accuracy described in this paragraph applies to the C_p-G and L_p-G combinations only.

R_p accuracy
When D_x (measured D value) ≤ 0.1

R_p accuracy is given as

$$\pm \frac{R_{px} \times D_e}{D_x \mp D_e} \quad [\Omega]$$

where:

R_{px} = Measured R_p value [Ω]
D_x = Measured D value
D_e = Relative D accuracy

R_s accuracy
When D_x (measured D value) ≤ 0.1

R_s accuracy is given as

$$X_x \times D_a \quad [\Omega]$$

$$X_x = 2\pi f L_x = \frac{1}{2\pi f C_x}$$

where:

X_x = Measured X value [Ω]
C_x = Measured C value [F]
L_x = Measured L value [H]
D_e = Relative D accuracy
f = Test frequency [Hz]

Example of C-D Accuracy Calculation

Measurement conditions

Frequency:	1 kHz
C measured:	100 nF
Test signal voltage:	1 V_{rms}
Integration time:	MEDIUM
Cable length:	0 m

Then:

A = 0.05

$$|Z_m| = \frac{1}{2\pi \times 1 \times 10^3 \times 100 \times 10^{-9}}$$
$$= 1590\ [\Omega]$$

$$K_a = \frac{1 \times 10^{-3}}{1590}\left(1 + \frac{200}{1000}\right)$$
$$= 7.5 \times 10^{-7}$$

$$K_b = 1590 \times 1 \times 10^{-9}\left(1 + \frac{70}{1000}\right)$$
$$= 1.70 \times 10^{-6}$$

$$K_c = 0$$

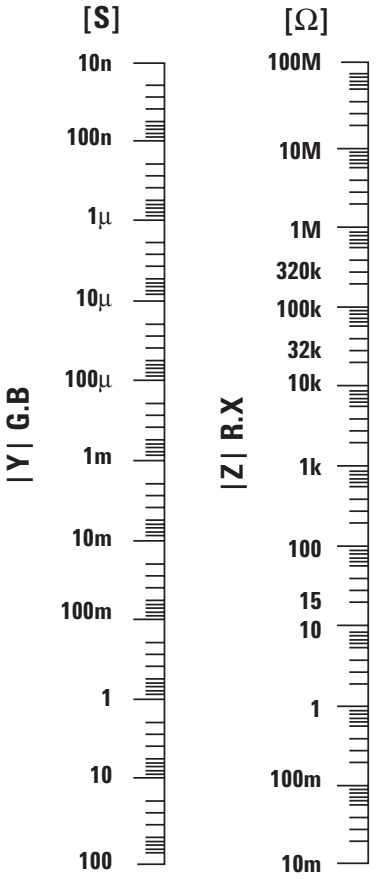
Therefore,

$$C_{accuracy} = \pm[0.05 + (7.5 \times 10^{-7} + 1.70 \times 10^{-6}) \times 100]$$
$$\approx \pm 0.05\ [\%]$$

$$D_{accuracy} = \pm \frac{0.05}{100}$$

$$= \pm 0.0005$$

Specification Charts and Tables



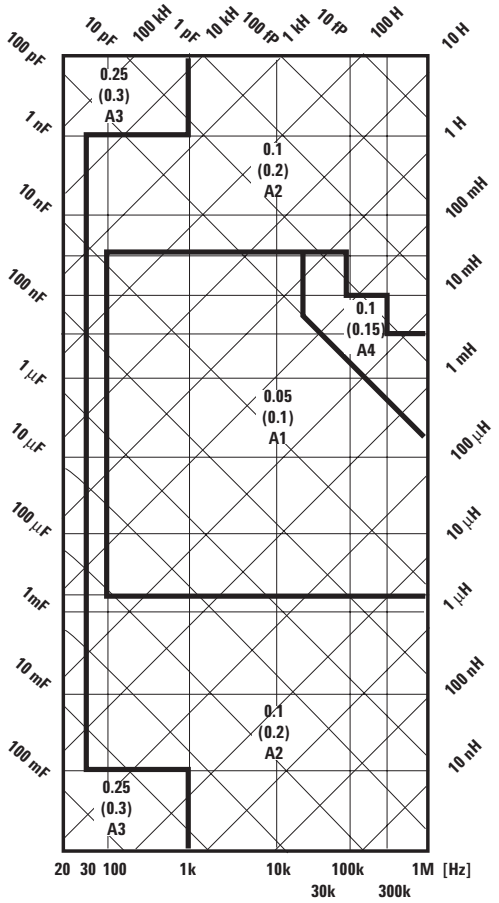


Figure 1-3. Basic accuracy A (1 of 2)

On boundary line apply the better value.

Example of how to find the A value:

0.05 = A value when 0.3 $V_{rms} \leq V_s \leq 1\ V_{rms}$ and integration time is MEDIUM and LONG.
(0.1) = A value when 0.3 $V_{rms} \leq V_s \leq 1\ V_{rms}$ and integration time is SHORT.
A_1 = A value when $V_s < 0.3\ V_{rms}$ or $V_s > 1\ V_{rms}$. To find the value of A_1, A_2, A_3, and A_4 refer to the following table.

where:

V_s = Test signal voltage

The following table lists the value of A_1, A_2, A_3, and A_4. When Atl is indicated find the Atl value using Figure 1-4.

Test signal voltage

	5m	12m	0.1	0.15	0.3	1	2	5	20 [Vrms]
Medium/ long	A_1 = Atl A_2 = Atl * A_3 = Atl A_4 = Atl	A_1 = Atl A_2 = Atl * A_3 = 0.25 A_4 = Atl	A_1 = Atl A_2 = Atl A_3 = 0.25 A_4 = Atl	A_1 = Atl A_2 = 0.1 A_3 = 0.25 A_4 = 0.1			A_1 = Atl A_2 = Atl A_3 = 0.25 A_4 = Atl	A_1 = Atl A_2 = Atl A_3 = 0.25 A_4 = Atl **	
Short	A_1 = Atl A_2 = Atl A_3 = Atl A_4 = Atl		A_1 = Atl A_2 = Atl A_3 = 0.3 A_4 = Atl	A_1 = Atl A_2 = 0.2 A_3 = 0.3 A_4 = 0.5 X Alt+0.1			A_1 = Atl A_2 = Atl A_3 = 0.3 A_4 = Atl	A_1 = Atl A_2 = Atl A_3 = 0.3 A_4 = Atl **	
	5m	33m	0.15			1	2	5	20 [Vrms]

* Multiply the A values as follows, when the test frequency is less than 300 Hz.

100 Hz ≤ f_m <300 Hz: Multiply the A values by 2.
f_m < 100 Hz: Multiply the A values by 2.5.

** Add 0.15 to the A values when all of the following measurement conditions are satisfied.

Test frequency: 300 kHz < f_m ≤ 1 MHz
Test signal voltage: 5 V_{rms} < V_s ≤ 20 V_{rms}
DUT: Inductor, $|Z_m|$ <200 Ω ($|Z_m|$: impedance of DUT)

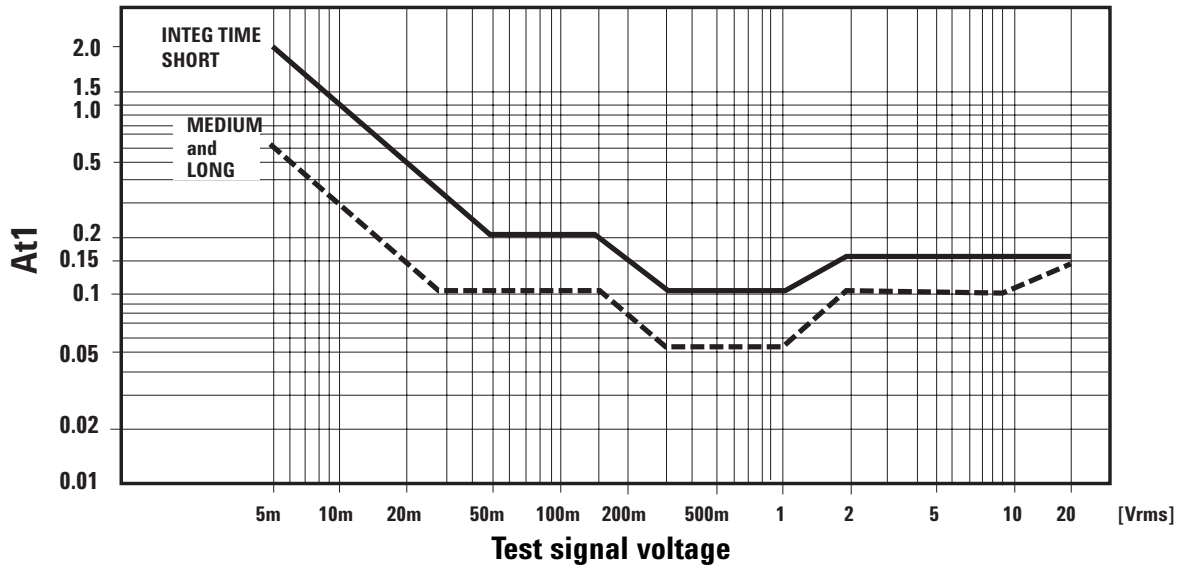


Figure 1-4. Basic accuracy A (2 of 2)

K_a and K_b values are the incremental factors in low impedance and high impedance measurements, respectively. K_a is practically negligible for impedances above 500 Ω, and K_b is negligible for impedances below 500 Ω.

Table 1-1. Impedance proportional factors K_a and K_b

Integ-time	Frequency	K_a	K_b
MEDIUM LONG	$f_m < 100$ Hz	$\left(\frac{1\times10^{-3}}{\lvert Z_m\rvert}\right)\left(1+\frac{200}{V_s}\right)\left(1+\sqrt{\frac{100}{f_m}}\right)$	$\lvert Z_m\rvert\left(1\times10^{-9}\right)\left(1+\frac{70}{V_s}\right)\left(1+\sqrt{\frac{100}{f_m}}\right)$
	100 Hz $\leq f_m \leq$ 100 kHz	$\left(\frac{1\times10^{-3}}{\lvert Z_m\rvert}\right)\left(1+\frac{200}{V_s}\right)$	$\lvert Z_m\rvert\left(1\times10^{-9}\right)\left(1+\frac{70}{V_s}\right)$
	100 kHz $< f_m \leq$ 300 kHz	$\left(\frac{1\times10^{-3}}{\lvert Z_m\rvert}\right)\left(2+\frac{200}{V_s}\right)$	$\lvert Z_m\rvert\left(3\times10^{-9}\right)\left(1+\frac{70}{V_s}\right)$
	300 kHz $< f_m \leq$ 1 MHz	$\left(\frac{1\times10^{-3}}{\lvert Z_m\rvert}\right)\left(3+\frac{200}{V_s}+\frac{V_s^2}{10^8}\right)$	$\lvert Z_m\rvert\left(10\times10^{-9}\right)\left(1+\frac{70}{V_s}\right)$
SHORT	$f_m < 100$ Hz	$\left(\frac{2.5\times10^{-3}}{\lvert Z_m\rvert}\right)\left(1+\frac{400}{V_s}\right)\left(1+\sqrt{\frac{100}{f_m}}\right)$	$\lvert Z_m\rvert\left(2\times10^{-9}\right)\left(1+\frac{100}{V_s}\right)\left(1+\sqrt{\frac{100}{f_m}}\right)$
	100 Hz $\leq f_m \leq$ 100 kHz	$\left(\frac{2.5\times10^{-3}}{\lvert Z_m\rvert}\right)\left(1+\frac{400}{V_s}\right)$	$\lvert Z_m\rvert\left(2\times10^{-9}\right)\left(1+\frac{100}{V_s}\right)$
	100 kHz $< f_m \leq$ 300 kHz	$\left(\frac{2.5\times10^{-3}}{\lvert Z_m\rvert}\right)\left(2+\frac{400}{V_s}\right)$	$\lvert Z_m\rvert\left(6\times10^{-9}\right)\left(1+\frac{100}{V_s}\right)$
	300 kHz $< f_m \leq$ 1 MHz	$\left(\frac{2.5\times10^{-3}}{\lvert Z_m\rvert}\right)\left(3+\frac{400}{V_s}+\frac{V_s^2}{10^8}\right)$	$\lvert Z_m\rvert\left(20\times10^{-9}\right)\left(1+\frac{100}{V_s}\right)$
f_m : Test frequency [Hz] $\lvert Z_m\rvert$: Impedance of DUT [Ω] V_s : Test signal voltage [mV_{rms}]			

K_{aa} is practically negligible for impedances above 500 Ω.

Table 1-2. Cable length factor K_{aa}

Test signal voltage	Cable length			
	0 m	1 m	2 m	4 m
≤ 2 V_{rms}	0	0	$\frac{K_a}{2}$	K_a
> 2 V_{rms}	0	$\frac{2\times10^{-3}\times f_m^2}{\lvert Z_m\rvert}$	$\frac{(1+5\times f_m^2)\times10^{-3}}{\lvert Z_m\rvert}$	$\frac{(2+10\times f_m^2)\times10^{-3}}{\lvert Z_m\rvert}$
f_m : Test frequency [MHz] $\lvert Z_m\rvert$: Impedance of DUT [Ω] K_a : Impedance proportional factor				

Table 1-3. Cable length factor K_{bb}

Frequency	Cable length 0 m	1 m	2 m	4 m
$f_m \leq 100$ kHz	1	$1 + 5 \times f_m$	$1 + 10 \times f_m$	$1 + 20 \times f_m$
100 kHz < $f_m \leq 300$ kHz	1	$1 + 2 \times f_m$	$1 + 4 \times f_m$	$1 + 8 \times f_m$
300 kHz < $f_m \leq 1$ MHz	1	$1 + 0.5 \times f_m$	$1 + 1 \times f_m$	$1 + 2 \times f_m$

f_m: Test Frequency [MHz]

Table 1-4. Calibration interpolation factor K_c

Test frequency	K_c
Direct calibration frequencies	0
Other frequencies	0.0003

Direct calibration frequencies are the following forty-eight frequencies.

Table 1-5. Preset calibration frequencies

			20	25	30	40	50	60	80	[Hz]
100	120	150	200	250	300	400	500	600	800	[Hz]
1	1.2	1.5	2	2.5	3	4	5	6	8	[kHz]
10	12	15	20	25	30	40	50	60	80	[kHz]
100	120	150	200	250	300	400	500	600	800	[kHz]
1	[MHz]									

Table 1-6. Cable length factor K_d

Test signal level	Cable length 1 m	2 m	4 m
$\leq 2\ V_{rms}$	$2.5 \times 10^{-4}(1 + 50 \times f_m)$	$5 \times 10^{-4}(1 + 50 \times f_m)$	$1 \times 10^{-3}(1 + 50 \times f_m)$
$> 2\ V_{rms}$	$2.5 \times 10^{-3}(1 + 16 \times f_m)$	$5 \times 10^{-3}(1 + 16 \times f_m)$	$1 \times 10^{-2}(1 + 16 \times f_m)$

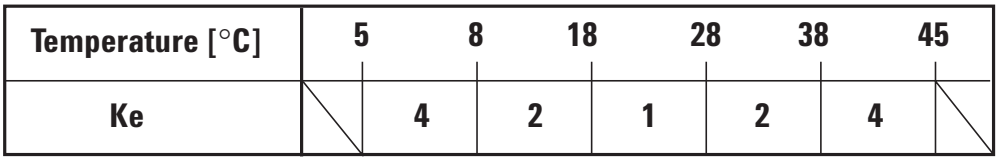
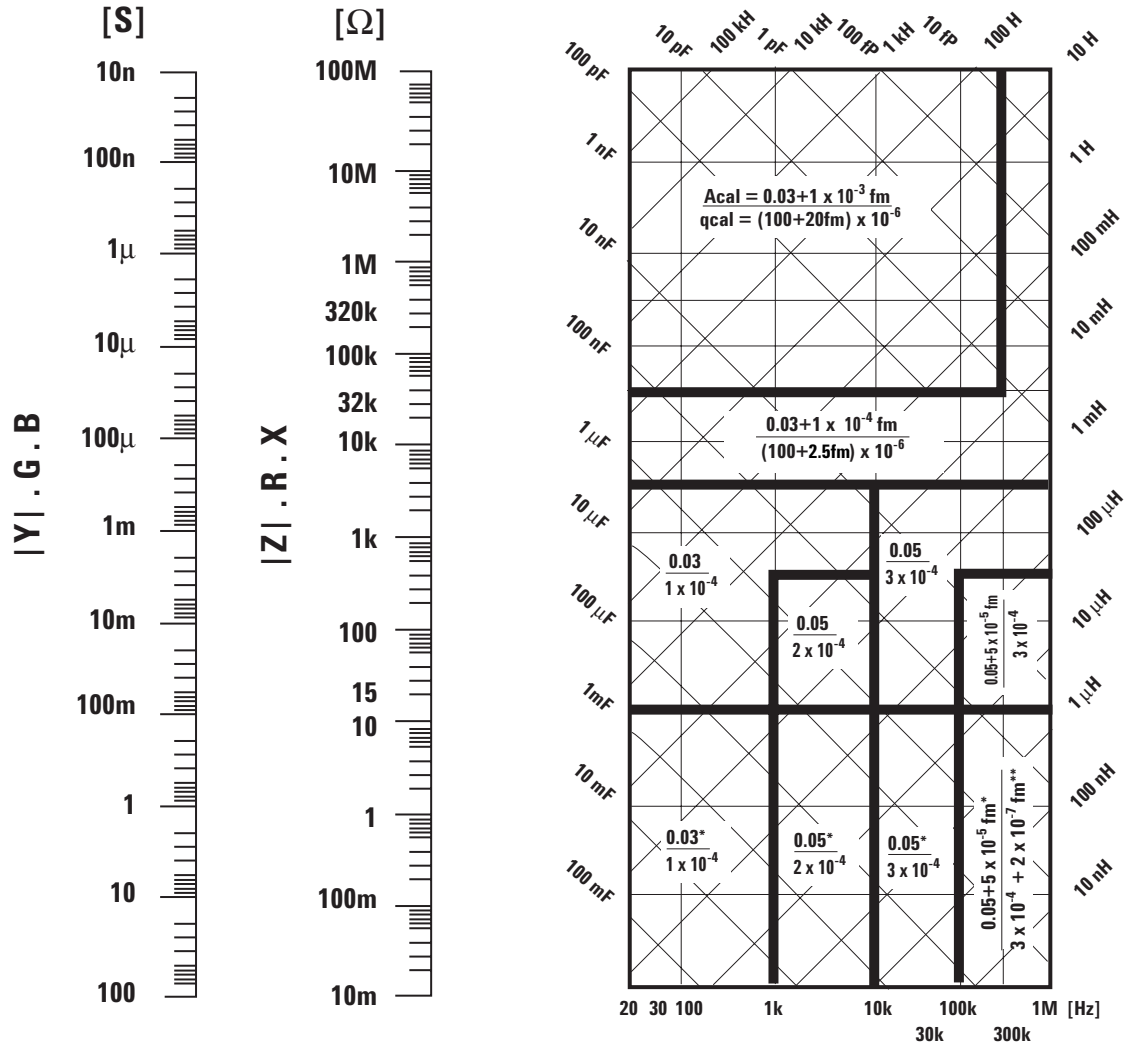


Figure 1-5. Temperature factor K_e

Agilent 4284A Calibration Accuracy

Calibration accuracy is shown in the following figure:



Test frequency

f_m = test frequency [kHz]

On boundary line apply the better value:

Upper value (A_{cal}) is |Z|,|Y|, L, C, R, X, G, and B calibration accuracy [%]

Lower value (θ_{cal}) is phase calibration accuracy in radians.

* A_{cal} = 0.1% when Hi-PW mode is on.

** A_{cal} = (300 + fm) x 10^{-6} [rad] when Hi-PW mode is on.

Phase calibration accuracy in degree, θ_{cal} [deg] is given as,

$$\theta_{cal}\,[deg] = \frac{180}{\pi \times \theta_{cal}}\,[rad]$$

Additional Specifications

When measured value < 10 mΩ, |Z|, R, and X accuracy A_e, which is described on page 5, is given as following equation.

|Z|, R, and X accuracy:

$A_e = \pm[(K_a + K_{aa} + K_c) \times 100 + K_d] \times K_e \quad (\%)$

Where

- K_a: Impedance proportional factor (refer to Table 1-1)
- K_{aa}: Cable length factor (refer to Table 1-2)
- K_c: Calibration interpolation factor (refer to Tables 1-4 and 1-5)
- K_d: Cable length factor (refer to Table 1-6)
- K_e: Temperature factor (refer to Figure 1-5)
  - X accuracy apply when D_x (measured D value) ≤ 0.1
  - R accuracy apply when Q_x (measured Q value) ≤ 0.1
  - When D_x > 0.1, multiply A_e by $\sqrt{(1 + D_x^2)}$ for X accuracy.
  - When Q_x > 0.1, multiply A_e by $\sqrt{(1 + Q_x^2)}$ for R accuracy.

When measured value < 10 mΩ, calibration accuracy A_{cal}, which is described on page 11, is given as follows.

Calibration accuracy:

- When 20 Hz ≤ fm ≤ 1 kHz, calibration accuracy is 0.03 [%]*.
- When 1 kHz < fm ≤ 100 kHz, calibration accuracy is 0.05 [%]*.
- When 100 kHz < fm ≤ 1 MHz, calibration accuracy is $0.05 + 5 \times 10^{-5}$ fm [%]*.
  - fm: test frequency [kHz]
  - *A_{cal} = 0.1% when Hi-PW mode is on.

Correction Functions

Zero open

Eliminates measurement errors due to parasitic stray impedances of the test fixture.

Zero short

Eliminates measurement errors due to parasitic residual impedances of the test fixture.

Load

Improves the measurement accuracy by using a working standard (calibrated device) as a reference.

List Sweep

A maximum of 10 frequencies or test signal levels can be programmed. Single or sequential test can be performed. When Option 4284A-001 is installed, DC bias voltages can also be programmed.

Comparator Function

Ten bin sorting for the primary measurement parameter, and IN/OUT decision output for the secondary measurement parameter.

Sorting modes

Sequential mode. Sorting into unnested bins with absolute upper and lower limits

Tolerance mode. Sorting into nested bins with absolute or percent limits

Bin count

0 to 999,999

List sweep comparator

HIGH/IN/LOW decision output for each point in the list sweep table.

DC Bias

0 V, 1.5 V, and 2 V selectable

Setting accuracy

±5% (1.5 V, 2 V)

Other Functions

Store/load

Ten instrument control settings, including comparator limits and list sweep programs, can be stored and loaded from and into the internal non-volatile memory. Ten additional settings can also be stored and loaded from each removable memory card.

GPIB

All control settings, measured values, comparator limits, list sweep program. ASCII and 64-bit binary format. GPIB buffer memory can store measured values for a maximum of 128 measurements and output packed data over the GPIB bus. Complies with IEEE-488.1 and 488.2. The programming language is SCPI.

Interface functions

SH1, AH1, T5, L4, SR1, RL1, DC1, DT1, C0, E1

Self test

Softkey controllable. Provides a means to confirm proper operation.

Options

Option 4284A-001 (power amp/DC bias)

Increases test signal level and adds the variable DC bias voltage function.

Test signal level

	Mode	Range	Setting accuracy
Voltage	Non-constant	5 mV to 20 Vrms	±(10% + 1 mV)
	Constant[1]	10 mV to 10 Vrms	±(10% + 1 mV)
Current	Non-constant	50 μA to 200 mArms	±(10% + 10 μA)
	Constant[1]	100 μA to 100 mArms	±(10% + 10 μA)

1. Automatic level control function is set to on.

Output impedance

100 Ω, ±6%

Test signal level monitor

Mode	Range	Accuracy
Voltage[1]	> 2 V_{rms}	±(3% of reading + 5 mV)
	5 mV to 2 V_{rms}	±(3% of reading + 0.5 mV)
	0.01 mV to 5 mV_{rms}	±(11% of reading + 0.1 mV)
Current[2]	> 20 mArms	±(3% of reading + 50 μA)
	50 μA to 20 mArms	±(3% of reading + 5 μA)
	0.001 μA to 50 μArms	±(11% of reading + 1 μA)

1. Add the impedance measurement accuracy [%] to the voltage level monitor accuracy when the DUT's impedance is < 100 Ω
2. Add the impedance measurement accuracy [%] to the current level monitor accuracy when the DUT's impedance is ≥ 100 Ω.

Accuracies apply when test cable length is 0 m or 1 m. Additional error for 2 m or 4 m test cable length is given as:

$$f_m \times \frac{L}{2} [\%]$$

where:

f_m is test frequency [MHz]
L is test cable length [m]

DC bias level

The following DC bias level accuracy is specified for an ambient temperature range of 23 °C ±5 °C. Multiply the temperature induced setting error listed in Figure 1-5 for the temperature range of O °C to 55 °C.

Test signal level ≤ 2 V_{rms}

Voltage range	Resolution	Setting accuracy
±(0.000 to 4.000) V	1 mV	±(0.1% of setting + 1 mV)
±(4.002 to 8.000) V	2 mV	±(0.1% of setting + 2 mV)
±(8.005 to 20.000) V	5 mV	±(0.1% of setting + 5 mV)
±(20.01 to 40.00) V	10 mV	±(0.1% of setting + 10 mV)

Test signal level > 2 V_{rms}

Voltage range	Resolution	Setting accuracy
±(0.000 to 4.000) V	1 mV	±(0.1% of setting + 3 mV)
±(4.002 to 8.000) V	2 mV	±(0.1% of setting + 4 mV)
±(8.005 to 20.000) V	5 mV	±(0.1% of setting + 7 mV)
±(20.01 to 40.00) V	10 mV	±(0.1% of setting + 12 mV)

Setting accuracies apply when the bias current isolation function is set to OFF. When the bias current isolation function is set to on, add ±20 mV to each accuracy value (DC bias current ≤ 1 μA).

Bias current isolation function
A maximum DC bias current of 100 mA (typical value) can be applied to the DUT.

DC bias monitor terminal
Rear panel BNC connector

Other Options

Option 4284A-700	Standard power (2 V, 20 mA, 2 V DC bias)
Option 4284A-001	Power amplifier/DC bias
Option 4284A-002	Bias current interface Allows the 4284A to control the 42841A bias current source.
Option 4284A-004	Memory card
Option 4284A-006	2 m/4 m cable length operation
Option 4284A-201	Handler interface
Option 4284A-202	Handler interface
Option 4284A-301	Scanner interface
Option 4284A-710	Blank panel
Option 4284A-907	Front handle kit
Option 4284A-908	Rack mount kit
Option 4284A-909	Rack flange and handle kit
Option 4284A-915	Add service manual
Option 4284A-ABJ	Add Japanese manual
Option 4284A-ABA	Add English manual

Furnished Accessories

Power cable	Depends on the country where the 4284A is being used.
Fuse	Only for Option 4284A-201, Part number 2110-0046, 2 each

Power Requirements

Line voltage
100, 120, 220 Vac ±10%, 240 Vac +5% – 10%

Line frequency
47 to 66 Hz

Power consumption
200 VA max

Operating Environment

Temperature
0 °C to 55 °C

Humidity
≤ 95% R.H. at 40 °C

Dimensions

426 (W) by 177 (H) by 498 (D) (mm)

Weight

Approximately 15 kg (33 lb., standard)

Display

LCD dot-matrix display

Capable of displaying
Measured values
Control settings
Comparator limits and decisions
List sweep tables
Self test message and annunciations

Number of display digits
6 digits, maximum display count 999,999

Supplemental Performance Characteristics

The 4284A supplemental performance characteristics are not specifications but are typical characteristics included as supplemental information for the operator.

Stability

MEDIUM integration time and operating temperature at 23 °C ±5 °C

|Z|, |Y| L, C, R, < 0.01%/day

D < 0.0001/day

Temperature Coefficient

MEDIUM integration time and operating temperature at 23 °C ±5 °C

Test signal level	|Z|, |Y|, L, C, R	D
≥ 20 mV_{rms}	< 0.0025%/°C	< 0.000025/°C
< 20 mV_{rms}	< 0.0075%/°C	< 0.000075/°C

Settling Time

Frequency (f_m)

< 70 ms ($f_m \geq 1$ kHz)
< 120 ms (100 Hz ≤ f_m < 1 kHz)
< 160 ms (f_m < 100 Hz)

Test signal level

< 120 ms

Measurement range

< 50 ms/range shift ($f_m \geq 1$ kHz)

Input Protection

Internal circuit protection, when a charged capacitor is connected to the UNKNOWN terminals.

The maximum capacitor voltage is:

$$V_{max} = \sqrt{\frac{1}{C}} \quad [V]$$

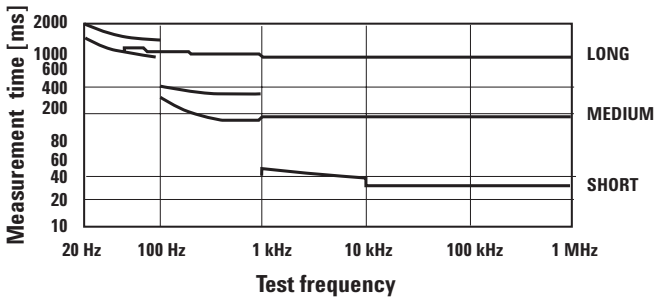
where:

$V_{max} \leq 200$ V,
C is in Farads

Measurement Time

Typical measurement times from the trigger to the output of EOM at the handler interface. (EOM: end of measurement)

Integration time	Test frequency 100 Hz	1 kHz	10 kHz	1 MHz
SHORT	270 ms	40 ms	30 ms	30 ms
MEDIUM	400 ms	190 ms	180 ms	180 ms
LONG	1040 ms	830 ms	820 ms	820 ms



Display time

Display time for each display format is given as

MEAS DISPLAY page	Approx. 8 ms
BIN No. DISPLAY page	Approx. 5 ms
BIN COUNT DISPLAY page	Approx. 0.5 ms

GPIB data output time

Internal GPIB data processing time from EOM output to measurement data output on GPIB lines (excluding display time).

Approx. 10 ms

DC Bias (1.5 V/2 V)

Output current.: 20 mA max.

Option 4284A-001 (Power Amp/DC Bias)

DC bias voltage

DC bias voltage applied to DUT (V_{dut}) is given as

$$V_{dut} = V_b - 100 \times I_b \quad [V]$$

Where, V_b is DC bias setting voltage [V]
I_b is DC bias current [A]

DC bias current

DC bias current applied to DUT (I_{dut}) is given as

$$I_{dut} = \frac{V_b}{100 + R_{dc}} \quad [A]$$

where: V_b is DC bias setting voltage [V]
R_{dc} is the DUT's DC resistance [Ω]

Maximum DC bias current when the normal measurement can be performed is as follows.

Measurement range		10 Ω	100 Ω	300 Ω	1 kΩ	3 kΩ	10 kΩ	30 kΩ	100 kΩ
Bias current isolation	On	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA	100 mA
	Off	2 mA	2 mA	2 mA	1 mA	300 µA	100 µA	30 µA	10 µA

Relative accuracy with bias current isolation

When the bias current isolation function is set to on, add the display fluctuation (N) given in the following equation to the A_e of relative accuracy. (Refer to "relative accuracy" of specification.)

The following equation is specified when all of the following conditions are satisfied.

DUT impedance ≥ 100 Ω
Test signal level setting ≤ 1 V_{rms}
DC bias current ≥ 1 mA
Integration time : MEDIUM

$$N = P \times \frac{DUT_{impedance}\,[\Omega]}{Measurement\ range\,[\Omega]} \times \frac{DC_{bias\ current}\,[mA]}{Test\ signal\ level\,[V_{rms}]} \times \frac{1}{\sqrt{n}} \times 10^{-4} \quad [\%]$$

where:

P is the coefficient listed on Table 1-7.
n is the number of averaging.

When the DC bias current is less than 1 mA, apply N value at 1 mA. When integration time is set to SHORT, multiply N value by 5. When integration time is set to LONG, multiply N value by 0.5.

Table 1-7. Coefficient related to test frequency and measurement range

Meas. range	Test frequency f_m [Hz] $20 \le f_m < 100$	$100 \le f_m < 1$ k	1 k $\le f_m < 10$ k	10 k $\le f_m \le 1$ M
100 Ω	0.75	0.225	0.045	0.015
300 Ω	2.5	0.75	0.15	0.05
1 kΩ	7.5	2.25	0.45	0.15
3 kΩ	25	7.5	1.5	0.5
10 kΩ	75	22.5	4.5	1.5
30 kΩ	250	75	15	5
100 kΩ	750	225	45	15

Calculation Example

Measurement conditions

DUT: 100 pF
Test signal level: 20 mVrms
Test frequency: 10 kHz
Integration time: MEDIUM

Then:

DUT's impedance = $1/(2\pi \times 10^4 \times 100 \times 10^{-12}) = 159$ kΩ
Measurement range is 100 kΩ
DC bias current << 1 mA
P = 15 (according to Table 1-7)

A_e of relative accuracy without bias current isolation is ±0.22 [%]. (Refer to "relative accuracy" of specification.)

Then, $N = 15 \times (159 \times 10^3)/(100 \times 10^3) \times 1/(20 \times 10^{-3}) \times 10^{-4} = 0.12$ [%]

Therefore, relative capacitance accuracy is:

±(0.22 + 0.12) = ±0.34 [%]

DC Bias Settling Time

When DC bias is set to on, add the settling time listed in the following table to the measurement time. This settling time does not include the DUT charge time.

Test frequency (f_m)	Bias current isolation On	Off
20 Hz ≤ f_m < 1 kHz	210 ms	20 ms
1 kHz ≤ f_m < 10 kHz	70 ms	20 ms
10 kHz ≤ f_m ≤ 1 MHz	30 ms	20 ms

Sum of DC bias settling time plus DUT (capacitor) charge time is shown in the following figure.

Bias source	Bias current isolation	Test frequency (f_m)
(1) Standard	On/Off	20 Hz ≤ f_m ≤ 1 MHz
(2) Option 4284A-001	Off	20 Hz ≤ f_m ≤ 1 MHz
(3)	On	10 kHz ≤ f_m ≤ 1 MHz
(4)	On	1 kHz ≤ f_m < 10 kHz
(5)	On	20 Hz ≤ f_m < 1 kHz

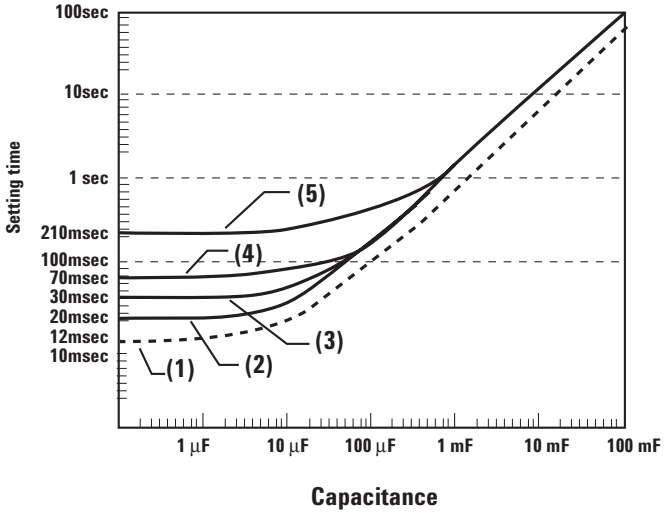


Figure 1-6. Measurement time

Rack/Handle Installation

The Agilent 4284A can be rack mounted and used as a component of a measurement system. The following figure shows how to rack mount the 4284A.

Table 1-8. Rack mount kits

Option	Description	Kit part number
4284A-907	Handle kit	5061-9690
4284A-908	Rack flange kit	5061-9678
4284A-909	Rack flange and handle kit	5061-9684

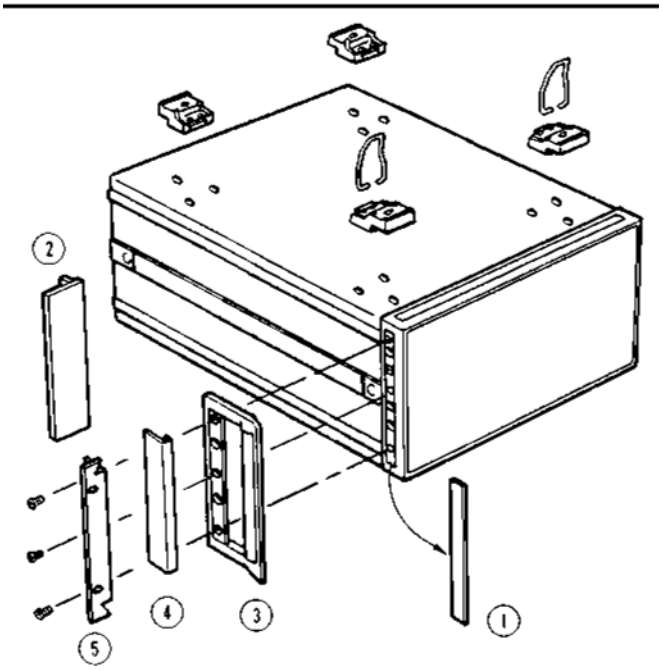


Figure 1-7. Rack mount kits installation

1. Remove the adhesive-backed trim strips (1) from the left and right front sides of the 4284A.

2. HANDLE INSTALLATION: Attach the front handles (3) to the sides using the screws provided and attach the trim strip (4) to the handle.

3. RACK MOUNTING: Attach the rack mount flange (2) to the left and right front sides of the 4284A using the screws provided.

4. HANDLE AND RACK MOUNTING: Attach the front handle (3) and the rack mount flange (5) together on the left and right front sides of the 4284A using the screws provided.

5. When rack mounting the 4284A (3 and 4 above), remove all four feet (lift bar on the inner side of the foot and slide the foot toward the bar).

Storage and repacking

This section describes the environment for storing or shipping the Agilent 4284A, and how to repackage the 4284A far shipment when necessary.

Environment

The 4284A should be stored in a clean, dry environment. The following environmental limitations apply for both storage and shipment

Temperature: –20 °C to 60 °C
Humidity: ≤ 95% RH (at 40 °C)

To prevent condensation from taking place on the inside of the 4284A, protect the instrument against temperature extremes.

Original packaging

Containers and packing materials identical to those used in factory packaging are available through your closest Agilent sales office. If the instrument is being returned to Agilent for servicing, attach a tag indicating the service required, the return address, the model number, and the full serial number. Mark the container FRAGILE to help ensure careful handling. In any correspondence, refer to the instrument by model number and its full serial number.

Other packaging

The following general instructions should be used when repacking with commercially available materials:

1. Wrap the 4284A in heavy paper or plastic. When shipping to an Agilent sales office or service center, attach a tag indicating the service required, return address, model number, and the full serial number.
2. Use a strong shipping container. A double-walled carton made of at least 350 pound test material is adequate.
3. Use enough shock absorbing material (3- to 4-inch layer) around all sides of the instrument to provide a firm cushion and to prevent movement inside the container. Use cardboard to protect the front panel.
4. Securely seal the shipping container.
5. Mark the shipping container *FRAGILE* to help ensure careful handling.
6. In any correspondence, refer to the 4284A by model number and by its full serial number.

Caution

The memory card should be removed before packing the 4284A.

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