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Analog and Digital Signal Processing Strategies for a Six-Port based Direction Of Arrival Detector

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Introduction

What does DOA measurements mean?

The Direction of Arrival (DOA) measurement is a method for the determination of the direction of propagation of a radio-frequency wave incident with respect to an antenna array.
For tracking system, defence purpose, security applications as well as industrial monitoring and tracking system is an important piece of information.
To obtain this, it is common to determine the DOA direction by measuring the

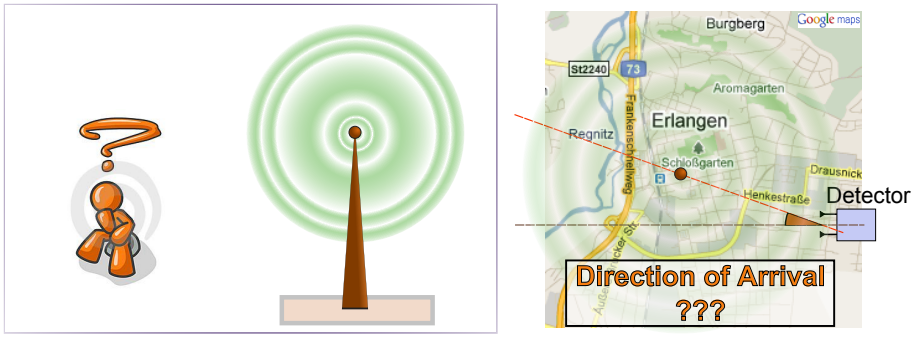

Figure 1: An antenna is emitting an electromagnetic signal. We want to detect from where it is coming the signal, in particular to measure the angle of incidence of the signal to a detector.

Time Difference of Arrival (TDOA) at individual elements of an antenna array. From the measure of delays the DOA angle can be calculated. Generally the TDOA measurement is made by measuring the difference in received phase at each element in the antenna array. This can be obtained with a beam forming technique [1] in reverse mode. In beam forming, the signals from each elements of the antenna array is delayed by some weight technique to "steer" the gain of the antenna. For the DOA measurements, the delay of arrival at each element is measured directly and converted into a DOA angle.
By considering, for example, a two element antenna array L spaced as shown in Fig. 2, where a wave is propagating with an angle α with respect to the antenna array x axis, the electromagnetic wave propagates through space at a speed ν:

$$\nu = f\lambda = \frac{1}{\sqrt{\mu\epsilon}} \ , \tag{1}$$

where f is the frequency of the wave and λ the wavelength in all the space. The two antennas measure the absolute time of arrivals: t_1 at the antenna 1 and at t_2 at the antenna 2. These two time values are enough to calculate the direction of arrival angle of the wave with the following formula:

$$\alpha = asin\left\{\frac{\nu(t_2 - t_1)}{L}\right\} \ . \tag{2}$$

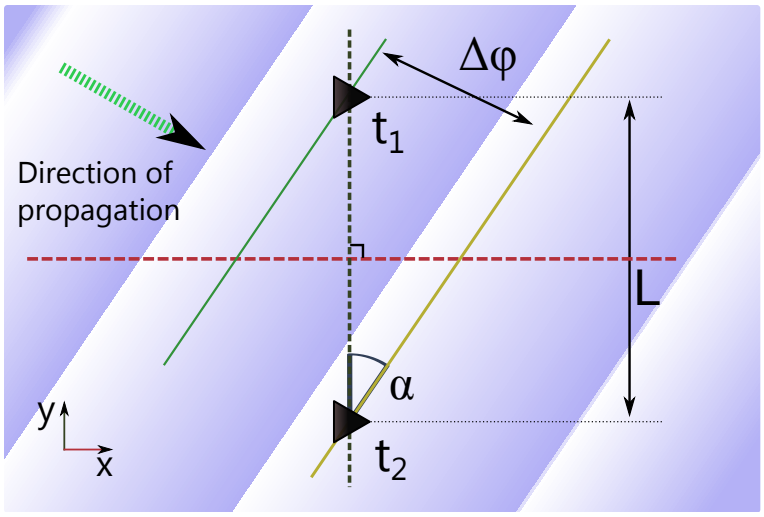

Figure 2: Dual antenna array for the TDOA measurements with an incoming wave. The wave arrives at time t_1 at the antenna 1 and at time t_2 at the antenna 2.

This is the canonical method to measure the Direction of Arrival angle since the first year of the '50. The TDOA has a lot of problems in terms of stability and accuracy and the hardware are expensive and sophisticated. In particular, oscillators are critical components for the system stability, they are used to down-mixing the incoming electromagnetic signals. Unfortunately, they have to work in ambient temperature-stabilized and don't allows to measure broadband signals.
A new approach has then been introduced for the DOA measurements as explained in the following.

The goal of the project

The result expected in this project is the implementation of a new approach for the Direction Of Arrival measurement based on the wave phase measurement. This new approach is based on the use of a Six-Port component for the measuring of the phase shift. This offers the advantage that the oscillator is no-more needed and the signals are automatically down-mixed from the Six-Port network. This is very important, because without oscillators the measurement system does not need to be thermal stabilized or also in particular situations where the detection system does not have to emit radiations (for example in stealth airplain).
This measurements architecture then allows to create a robust, low-cost board able to measure the direction of arrival angle with high accuracy.

In this thesis technical solutions for the signal acquisition from Six-Port inter-

ferometers and the digital samples processing of the samples to obtain the DOA angle have been discussed on the base of the development and the test of an acquisition prototype board (A/D module) with the support of a FPGA-based developing board (DSP module). Different acquisition architecture and different computational approaches have been tested.
The radio-frequency circuits have been designed to work with 24 GHz signals in MCW (modulated continuous wave) mode. This frequency is commonly used for automotive radars. The result of this project, for example, allows to solve the calibration in the car radar devices and thus to avoid misalignment.
Desired accuracy of the DOA detection is $1 \cdot 10^{-}4$ DEG with a range approaching of 180 DEG.

Chapter 1

Analog and Digital domains

Signals are the objects we need to work with to receive and send informations. It is possible to define two main groups based on theirs domains: Analog or Digital signals.
The Analog signals are continuous in the time-domain, whereas the Digital are discrete time-domain (with discrete amplitude values).
With this chapter we want to introduce the conversion process between this two domains, the problems which have to be solved for this operation and a little section about architectures for the digital processing.

1.1 Analog - Digital conversion

Analog-to-digital (A/D) conversion is the hybrid transformation in which a (continuously variable) analog signal (a continuous domain signal) is changed, without altering its essential content, into a multi-level digital signal (a discrete domain signal). Instead, the Digital-to-Analog (D/A) conversion is the hybrid transformation in which a multi-level digital signal is changed in a continuously variable analog signal.
These transformations in modern applications offer a set of advantages, the most important are that digital signals propagate more efficiently than analog signals, and digital impulses are easy to be distinguished from noise, allowing to transmit more informations. This is the main advantage of the digital domain in communications.
Moreover, computers "talk" and "think" in terms of digital data: while a microprocessor can analyse analog data, the signal must be converted into digital form for the computer.
The A-D conversion is a loss free information if it satisfies some rules mainly the Sampling Theorem and the Heaviside conditions. In this case it is possible, from the digital data, to correctly reproduce the original analog one, and vice-versa.

Sampling

The sampling is a instantaneous, LTI (Linear and Time Invariant) transformation, used in A/D Conversion, that produces a discrete signal y_n from a continuous signal $x(t)$ [2]. The produced discrete signal has a domain at instants multiples of a *sampling period* (T_s) [3]:

$$y_n = x(n \cdot T_s), \ \text{n} \in \mathbb{Z}. \tag{1.1}$$

Where $\mathbb{Z}$ is the discrete numbers domain. The sampling transformation can be viewed as a system (Fig. 1.1) in which the input signal is continuous and the output is discrete. The inverse of the sampling period is called *sampling frequency* (or *sampling rate*) $F_s = 1/T_s$. This value represents the number of samples per unit time and is expressed in Hz unit.

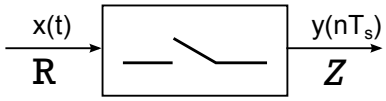

Figure 1.1: Representation of a sampling system of a continuous time signal x(t).

The sampling in the time domain creates repetitions in the frequency domain $Y(f)$:

$$Y(f) = rep_{F_s} X(f) = \sum_{n=-\infty}^{+\infty} X(f - nF_s), \ \text{n}\in \mathbb{N}. \tag{1.2}$$

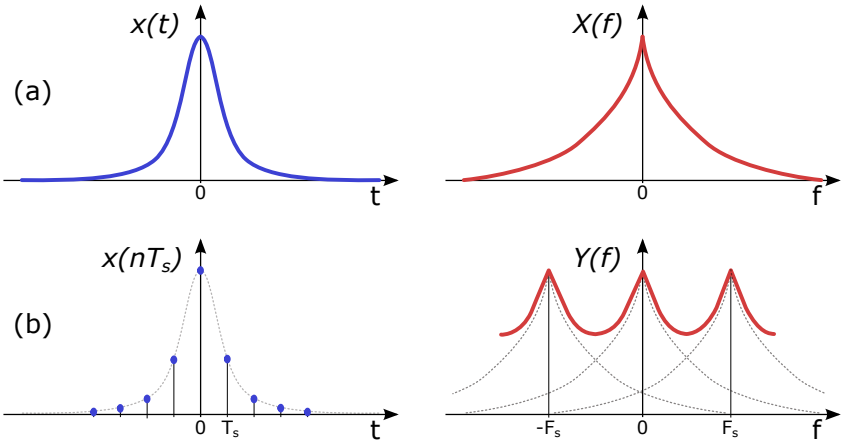

Figure 1.2: Fourier Transform of a continuous time signal(a) and the Transform of the sampled signal (b).

The relation between x and y is illustrated in Fig. 1.2 both in time and frequency domains. This repetitions of the spectrum of the input signal (X) could produce superposition of the output spectrum (Y). The overlapping of the spectrum may cause a distortion of the discrete signal y in the frequency domain that does not allow to reproduce correctly the original signal from the sample data.

Bandwidth

Very important for the A/D conversion is the bandwidth of the analog signals. This term can be extended also to the digital signals.
The *full band* $\overline{B}_x$ of a continuous time signal x is defined as the support of its Fourier Transform (FT), that is the set of frequencies where its FT is not zero:

$$\overline{B}_x = \{f \in \mathbb{R} \ : \ X(f) \neq 0\}.$$

For Real-value signals the full band is symmetric with respect to the origin. In this case, it is usual to use the definition of *band* B_x as the subset of not negative

frequencies for which its FT is not zero.
A signal can be classified with respect to their band [4] (Fig. 1.3) as:

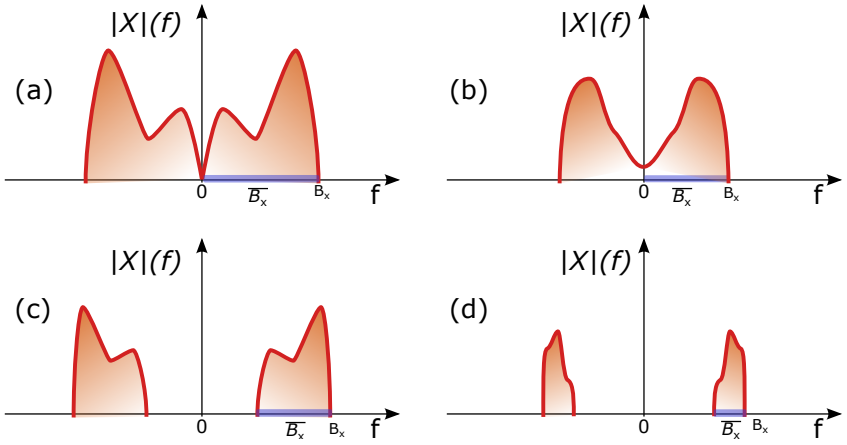

Figure 1.3: Example of frequency-domain representation of Real-value signals: bandlimited (a), baseband (b), passband (d) and narrowband (e).

- band limited (a), *if its band is a limited set*;
- baseband (b), *if its band is limited, around the origin and includes the origin*;
- passband (c), *if its band is limited and does not includes the origin*;
- narrowband (d), *if it is passband and his bandwidth $\overline{B}_x$ is smaller than its maximum frequency.*

Filters

A filter is a linear time-invariant transformation. Its input-output relationship can be written as the convolution of a signal x with the *impulse response* of the transformation (g). The Haar integral of a LTI filter is defined such [3]:

$$y(t) = \int_D du\ g(t-u)x(u) = (g * x)(t). \tag{1.3}$$

In the frequency domain the input-output relationship 1.3 becomes:

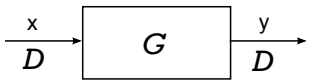

Figure 1.4: Representation of a filter system.

$$Y(f) = G(f) \cdot X(f). \tag{1.4}$$

This means that the Fourier Transform of the output can be obtained just by multiplying the Fourier Transforms of the input signal by the impulse response of the filter at any frequency f.
If the impulse response is band limited, the filter applies a window function to the incoming signal spectrum. This operation in the frequency domain allows to reduce (shape) the bandwidth B_x of the input signal x(t).
A filter with response g can be:

- low pass (LPF), *if its band is limited, around the origin and includes the origin*;
- high pass (HPF),*if its band excludes the origin and it is infinity*;
- band pass (BPF), *if its band is limited but not include the origin*;
- narrowband (NBF), *if its band is limited and more smaller than its maximum frequency*;
- notch (NTF), *if its band is the complement of the narrowband filter*;
- all pass, *if its band does not have zero values in the $|G(f)|$ function.*

Interpolation

The interpolation is a transformation which generates a continuous time signal $y(t)$ from a discrete time signal $x(nT_s)$ with quantum T_s.
To generate the output signal, the incoming discrete sample passes through

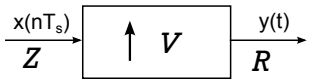

Figure 1.5: Representation of a interpolation system.

a continuous time-domain filter with impulse response v. The input-output relationship is:

$$y(t) = \sum_{n=-\infty}^{+\infty} T_s \; v(t - nT_s)x(nT_s). \tag{1.5}$$

This transformation is called also *interpolate filter* for his structure. In the frequency domain the interpolation works as a filter, in fact it applies a window to the input signal spectrum.

$$Y(f) = V(f)X(f). \tag{1.6}$$

From the same input samples it is possible to obtain different output signals using different functions v. For the interpolation the most common functions used are:

- holding interpolation: $v(t) = rect(\frac{t-T_s/2}{T_s})$;
- linear interpolation: $v(t) = triang(\frac{t}{T_s})$;
- raised cosine interpolation (with roll-off factor $\rho \in [0,1]$):

$$v(t) = sinc\left(\frac{t}{T_s}\right)\frac{\cos\left(\frac{\pi\rho t}{T_s}\right)}{1-\frac{4\rho^2t^2}{T_s^2}} \ .$$

Sampling theorem

The Shannon-Wittaker sampling theorem gives the bases of how to create a system that allows to convert an analog signal to a digital signal and then from the sample how to reconstruct the original loss free signal.
Let's consider the system in Fig. 1.6, where the input $x(t)$ is a real continuous

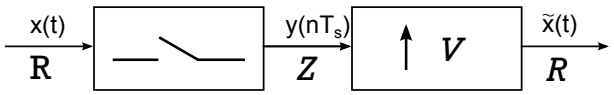

Figure 1.6: Sampling of a continuous time signal and reconstruction of its values through interpolation.

time signal. If:

1. the input signal $x(t)$ is with limited bandwidth ($\overline{B}_x \subset [0, B_x)$);
2. the sampling rate is $F_c \geq 2B_x$ (Nyquist frequency);
3. the interpolate filter v has frequency response

$$V(f) = \begin{cases} T_s, & |f| < B_x; \\ arbitrary, & B_x < |f| < F_c - B_c; \\ 0, & |f| > F_c - B_x; \end{cases} \tag{1.7}$$

the theorem says that the input signal is perfectly reconstructed at the output ($\widetilde{x}(t)$), that is

$$\tilde{x}(t) = x(t) \ , t \in \mathbb{R}. \tag{1.8}$$

If the incoming signal has a wide bandwidth, it is possible anyway to verify condition (1) by using a filter which reduce the signal bandwidth (information).

Heaviside conditions

The Heaviside conditions provide outlines for the no-distortion conditions.
Let's consider a signal x passing through a communication channel given by cascade of some transformations. The output signal of this large transformation is y. The aim of this communication channel is to guarantee a correct transmission of the x signal which allows to be reconstruct from the output signal y. To do this, the output signal can be maximum attenuated and/or shifted version of the input:

$$y(t) = A_0 \cdot x(t - t_0) \ , \tag{1.9}$$

where A_0 defines the attenuation (or amplification) of the original signal and t_0 the time shift.
The Eq. (1.9) required the complete transformation to be LTI and its impulse response h has to be:

$$h(t) = A_0 \cdot \delta(t - t_0) \ . \tag{1.10}$$

In the frequency domain, the Eq. 1.10 becomes:

$$H(f) = A_0 \cdot e^{j2\pi f t_0} \ . \tag{1.11}$$

This condition in the frequency domain creates a filter with constant amplitude ($|H| = A_0$), with a linear phase proportional to the frequency and with a constant group delay (also called envelope delay, t_0).
The Heaviside conditions define that if a input signal pass through a filter like Eq. (1.10) it is possible to have an output signal free of distortion. If the input signal is band limited ($\overline{B}_x$) it is possible to shrink the Heaviside conditions only in the band of interest.

1.2 Analog Digital Devices

To perform the Analog-To-Digital and the Digital-To-Analog transformations are commercially available different devices. The Analog Digital Converters (ADCs) are designed to perform the sampling transformation instead the Digital Analog Converters (DACs) are designed to perform the interpolation.

Analog Digital Converters (ADCs)

An Analog Digital Converter (ADC) is an electronic device which makes a sampling transformation. From an analog signal it produces a digital binary vector which is proportional to the magnitude of the input voltage.
ADCs can be divided in groups based on: voltage input, resolution, sampling rate, structures and channels.
The voltage input determines the voltage range that the ADC can measure. The resolution indicates the number of discrete values that can produce over the

analog values. Usually resolution is indicated with the number of bits used to encode the discrete values. An ADC with 8 bit resolution for example can represent $2^8 = 256$ different values which means a dynamic range of $10 \cdot log_{10}(256) = 24$ dB. The sampling rate defines the sampling frequency $F_s = 1/T_s$ expressed in Hz. A complete sample is delivered every T_s time. For the Sampling Theorem, this value determines the sampling frequency which has to be at least two times higher than the target signal bandwidth.
The ADCs internal structures allow to determine how the ADC works, the most common are pipelines, Wilkinson, successive-approximation types. The ADC implementation determines the performance and the accuracy of the measurements.
The channels defines the number of analog inputs has the ADC. The most common multi-channel ADCs connect the inputs, multiplexed to a single ADC, or an ADC array, to reduce the production costs. There are some others which have an ADC for each channel. Anyway the last expensive structure allows to create a system with simultaneous sampling necessary in some measurements.

Digital Analog Converters (DACs)

Digital to Analog Converting (DAC) allow the reverse operation performed by ADC. Digital to Analog Converters (DACs) provide the interpolation transformation, allowing to generate an analog signal from digital samples.
DACs can be divided into groups based on: resolution, maximum sampling frequency, THD+N and dynamic range.
The resolution number, expressed in bits, describes the maximum output values the DAC is able to reproduce.
The maximum sampling frequency is the maximum refresh speed at which the DAC is able to transform the digital number into an analog signal correctly. For the Nyquist-Shannon sampling theorem this frequency has to be at least two times higher than the target signal bandwidth. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DAC's that operate with a sampling frequency more than 40 kHz
The THD+N is a measurement of the distortion and noise introduced to the signal by the DAC. This value is expressed as a percentage of the total power of unwanted harmonic distortion and noise affecting the desired signal.
The dynamic range represents the difference between the largest and smallest signals the DAC can reproduce expressed in decibels unit.

1.3 Digital Processing approach

After the Analog to Digital conversion, the acquired signals processed before to be stored or converted back into an analog signal.
The processing of the digitalized input signals is normally performed by an integrated circuit (IC). The Architectures to implement an integrated circuit are two: application-specific integrated circuit or field-programmable gate array.
In the following, the characteristics of these two architectures are presented and discussed for the use in digital processing. A final comment for the use of these two architectures has been made for the IC developing.

Application-specific integrated circuit (ASIC)

The application-specific integrated circuit (ASIC) is a semiconductor device with inside an IC customized for a particular use. The ASIC is normally used to produce VLSI (Very Large Scale Integration) chips for dedicated functions. The ASIC chip are generated normally with a CMOS fabrication which is a lithographic process. This means that to develop an ASIC chip has to define a layout design that provides dimension and geometry of all the elements necessary to generate transistors and the interconnections.
It is not possible to modify the functions of the chip. To implement another function a new design has to be made. The ASIC contain a power grid (that provides the power to the circuits), a core, a pad ring (for input-output connections) and a clock tree. The core implements the IC and can be designed to manage analog and/or digital signals, it can be designed with a Full-Custom, Semi-Custom or Cell-Based approaches. An Full-Custom ASIC is made with a manual layout of the IC (obtained with a CAD software). This method is used for critical circuit of the system: it allows to design a optimized speed and consumption chip, with an small area occupation. Disadvantage of this architecture are long design, very difficult for complex circuit and low possibility to reuse the design for other design. A faster approach is based on the Semi-Custom or Cell-Based based on a design with standard or proprietary libraries. This method allows a more rapid development of the circuit at detriment of more space occupied and chip power consumption.
An important note is that the ASIC chips can have inside the core an analog circuit that allows to create high frequency circuits (for instances at 70 GHz) or to implement an ADC directly on-chip.
The ASIC being the basis for processors (such as Intel i5® or AMD Phenom® processors), allows to create a programmable chip programmed by software to performs more tasks.

Field-programmable gate array (FPGA)

Within respect to ASIC, the field-programmable gate array (FPGA) is a semiconductor device made to be programmable after manufacturing by using a hardware description language (HDL, like VHDL). Instead of being restricted to any predetermined hardware function, an FPGA allows to program features and functions for the product, to adapt to new standards, and reconfigure hardware for specific applications even after the product has been installed in the field-hence the name "field-programmable".
The FPGA can be used to implement any logical function that an ASIC could perform, but the ability to update the functionality after shipping offers advantages for many applications.
FPGAs consist of various mixes of configurable embedded SRAM, high-speed transceivers, high-speed I/O, logic blocks, and routing.
Specifically, an FPGA contains programmable logic components called logic elements (LE's) and a hierarchy of reconfigurable interconnects that allow the LE's to be physically connected. It is possible to configure LE's to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

ASIC versus FPGA, different approaches in the Digital Processing

In digital processing the architectures available are the ASIC and the FPGA which have different targets [5]. The operations implementable inside this two architectures are almost the same. The main differences are the production and developing costs and the performances required to the chips.
It is to be noted that the ASIC chips normally needs an external system of RAM and flash memory to work (if not implemented inside the chip), instead, the FPGA needs only an external chip where to store the logic configuration.
Table 1.1 compares the advantages of these two architectures.

Let's make final comments for the use of these two architectures to develop an IC.
FPGA used for prototype of digital signals processing is the best architecture for a fast developing cost-effective. In particular, the new FPGA architectures, fabricated with 22 μm CMOS technology [6], are covering the distance from the ASIC's in therms of power consumption and speed. Moreover a FPGA architecture is able to implement any logical function that an ASIC could perform. In fact, inside a FPGA with an FPAA (field-programmable analog array) it is also possible to implement the analog side working with low frequency signals (some GHz). The ASIC's chip it is the best solution for a final release (and large productions) with fix functions, high speed and low power consumption, and

ASIC Architecture Advantages	FPGA Architecture Advantages
- Full custom capability: *for design since device is manufactured to design specs;*	- Faster time-to-market: *no layout, masks or other manufacturing steps are needed;*
- Lower unit costs: *for very high volume designs;*	- No upfront NRE (non recurring expenses): *costs typically associated with an ASIC design;*
- Smaller form factor: *since device is manufactured to design specs.;*	- Simpler design cycle: *due to software that handles much of the routing, placement, and timing;*
- Higher raw internal clock speeds;	- More predictable project cycle: *due to elimination of potential re-spins, wafer capacities, etc.;*
- Analog side: it is possible to implement inside also high frequency analog components;	- Field reprogramability: *a new bit stream can be uploaded remotely;*
- Programmable in C-code: *easy code*;	- Programmable in HDL code: *it is possible to program the single AND/OR gates.*

Table 1.1: FPGA and ASIC Architecture Advantages

for Very Large Scale Integration (VLSI) integrated circuit. Disadvantages are that the ASIC design requires design experience for good results and the chip productions are schedule with waiting pre-production time of about 6 months.

Chapter 2

Digital signal processing for the DOA measurements

The scope of this chapter is to give the theoretical principles undergoing the detection of the DOA angle of an electro-magnetic (EMC) signal and a possible software architecture that can be used to calculate the DOA from the measurements obtained by the new type of detector based on the phase difference of the waves received from an antennas array.
With the introduction of a particular component introduced as "Black-Box" (the Six-Port component for the phase-measurements, present in the next Chapter) we want to present the mathematics and the software problems beyond the project.
In a first section, the principles of the DOA detection with a single black-box will be explained. In the second section, the expansion of the measurements to a dual black-boxes system will be considered. In the last paragraph, mathematical tools have been introduced to manipulate the data to reduce errors in the real measurements.

2.1 Single DOA detection

Let's suppose to have two receiving antennas (A1 and A2) at distance $d/2$ from a references axis as shown in Fig. 2.1. Moreover, let's suppose to have a black-box circuit with two inputs (I_1 and I_2) connected to the antennas which generates four outputs (P_1, P_2, P_3 and P_4) obtained as superposition of the

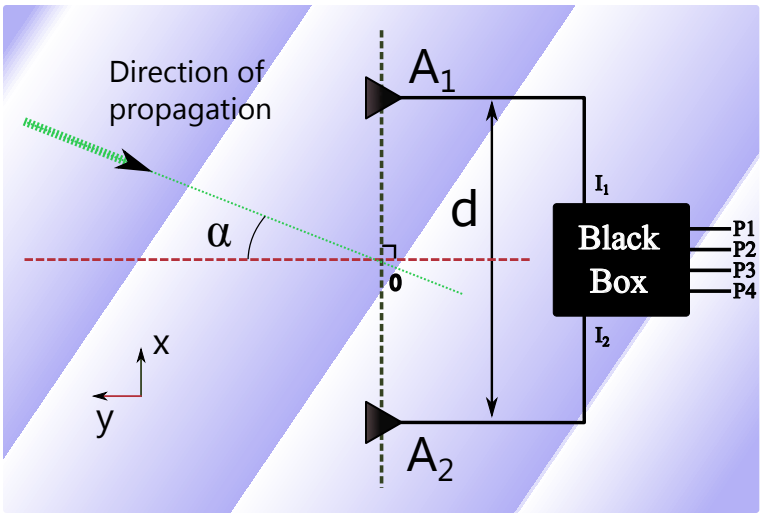

Figure 2.1: The antennas collect the EMC wave and the signals collected fed the received inputs into a black-box.

incoming signals with different relative phase:

$$P_1 = \quad I_1 + jI_2 \ ; \tag{2.1}$$
$$P_2 = \quad jI_1 + I_2 \ ; \tag{2.2}$$
$$P_3 = \quad jI_1 + jI_2 \ ; \tag{2.3}$$
$$P_4 = \quad I_1 - I_2 \ , \tag{2.4}$$

and down converted into baseband signals.
An electromagnetic wave at frequency f is incoming with angle α (see Fig. 2.1), the waves received from the two antennas have a phase difference of:

$$\Delta\phi = \phi_2 - \phi_1 = \frac{2\pi}{\lambda} \cdot d \cdot \sin(\alpha) \ , \tag{2.5}$$

see also Fig. 2. In the formula, λ represents the wavelength of the EMC wave.
If the signals amplitude collected from the two antennas are equal, it is possible to shows [7] [8] that the phase difference of the two signals collected from the antennas is given by:

$$\Delta\phi = \phi_1 - \phi_2 = arctan\left(\frac{P_1 - P_2}{P_3 - P_4}\right) \ . \tag{2.6}$$

By replacing the phase difference into equation (2.5), it is also possible to combine the two equations to obtain the DOA angle detected θ by the baseband outputs as:

$$\theta = \alpha_{detected} = asin\left[arctan\left(\frac{P_1 - P_2}{P_3 - P_4}\right) \cdot \frac{\lambda}{2\pi d}\right] \ . \tag{2.7}$$

The DOA angle detected has to be equal to α.
The Eq. (2.7) is the fundamental equation used to calculate the direction of arrival based on phase difference measurements.
The detection of the angle of incidence (α) is therefore bound to a non-linear function dependent on the four output values delivered by the system and on the distance d between the two receiving antennas. The arc tangent function delivers a linear phase difference which range from $-\pi$ to $+\pi$ as a result of the black-box output equations. The parameter d on the other hand determines the form factor of the arc sine function. By decreasing the distance between the antennas (d small in comparison with λ), via the arc tangent has a predominant role in the arc sine function thus delivering a complete sweep range of the angle θ within the function boundaries depending on the phase difference deriving from the arc tangent. By increasing d which depends the arc sine function stretches delivering a limited sweep range for the outcome of θ upon a complete phase sweep. Therefore, by increasing the distance d between the antennas a higher accuracy can be achieved within a narrower angle of incidence, since the complete phase difference is mapped through the arc sine function within a smaller range of θ. Although

the angle of incidence is non-linearly dependent on the phase difference $\Delta\phi$ it is possible to state that, within a small range around $\Delta\phi = 0$, the function can be assumed to be linear (small signal approximation of a sinusoidal function) [9].

Two simulations of angle detection with $|\alpha| < 5$ DEG, a signal at 24 GHz and with antennas $d = 20$ cm (a) and $d = 5$ cm (b) have been produced in Matlab. A different efficiency of the black-box outputs have been taken into account to simulate a real black-box.
The simulations are presented in Fig. 2.2. In the image, the red line represents

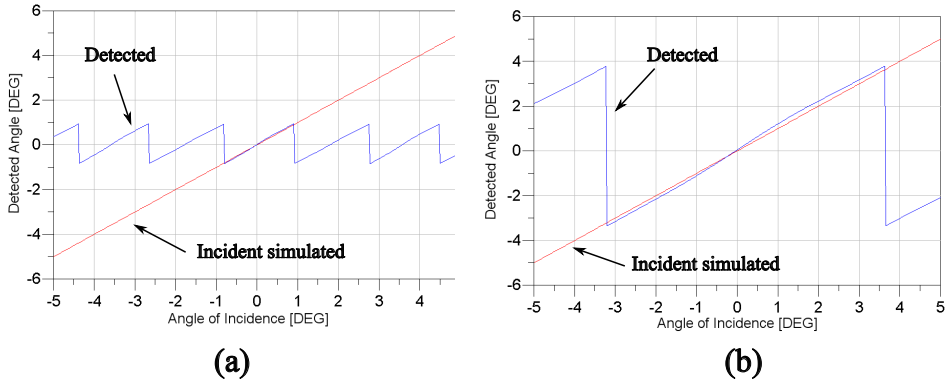

Figure 2.2: Simulation of the detected (blue) vs incident (red) angle for a wave at 24 GHz and a) with antennas at $d = 20$ cm and b) with antennas at $d = 5$ cm.

the simulated angle of incidence α and with blue line the θ angle calculated with the Eq. (2.7). It is also possible to see the DOA angle detection generated with α in the range [-5,+5] DEG. It is straight to observe that the detection of the DOA angle delivers no ambiguity only if $|\alpha| \widetilde{<} 0.75$ DEG for $d = 20$ cm and $|\alpha| < 3.75$ DEG for $d = 5$ cm where the angle detected θ is equal to the simulated angle α. Within a small range around an incident angle of zero, the detected angle has a quasi-linear periodicity shown in Fig. 2.2. It is possible to calculate the periodicity of the angle detected as:

$$P[\theta] = f(d) = \frac{\lambda \cdot 360 \text{ DEG}}{2\pi \cdot d} \ . \tag{2.8}$$

The formula shows that the periodicity of the detection is inversely proportional to the distance. The connection between resolution and detectable range does not allows to have at the same time a wide angle detection and good resolution.

Two errors are possible to see in the simulation: a geometrical distortion and a detection error. For large incident angles the detected value θ become highly non-linear by changing the periodicity ratio (see further). The non-linear behaviour

derives from a trigonometric dependency of the detected phase difference to the DOA angle (sinusoidal dependency). A post-production mapping of the detected angle can solve the geometric distortion. The simulations show that a small error is present also in the narrow angle measurement when different efficiency of the black-box outputs are present. In the last paragraph of the chapter a mathematical data treatment to compensate this problem will be presented.

Software strategies for the angle calculation

The aim of the paragraph is the presentation and a simple evaluation (in terms of programming complexity) of the possible software strategies usable for the α angle measurement, starting from the digitalized P values.
To develop a software for the DOA measurements we have first examined the conversion of the analog signals into digital samples. In fact, a series of ADCs have to be placed after the black-box to digitalize the P values. Very important is the definition of the digital resolution (aka number of bits) of the samples that determines the software requirements in therms of size and performances.
For the project the reference value for the resolution were $\pm 2 \cdot 10^{-4}$ DEG for the angle in a range between -90 and +90 DEG; then a 20 bit sign variable has been chosen to be used for angle representation and 12 bit unsigned values for the P inputs to guarantee a good dynamic input range.
For a fast project development, commercial available IC have been considered, whereas the software has been developed. Regarding the software, two possible approaches can be used, and two possible architectures (ASIC and FPGA) are available to implement the software. For each architecture, a board which includes memory and some communication interfaces, need to be used. Both software development can been performed for the two architectures.
The program developing in VHDL for the FPGA architecture and in C-code for an ASIC programmable processor have been compared. The software approaches to calculate the Eq. (2.7) are direct computation (DC) or direct digital synthesis (DDS).
In next paragraphs, θ and α will be used for the measured angles (or detected) and for the simulated angle respectively.

For the direct computation approach all the required operations have to be implemented, in fact, to compute the Eq. (2.7), the digital input samples (P1, P2, P3, P4) undergo all the operations presented in Fig. 2.3, where the constant ($const$) equals the value $const = \lambda/2\pi d$: a division, an $atan$ function, a multiplication and finally an $asin$ function.
This approach has a easy implementation in the ASIC processors thanks to the libraries available in the compiler. The possible C-code function to calculate the Eq. (2.7) is:

```
#include <math.h>
```

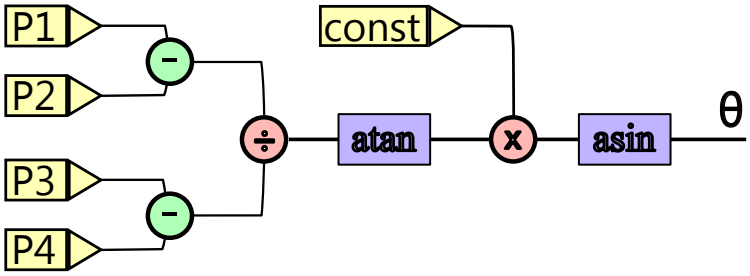

Figure 2.3: Computational flow-chart for the calculation of θ with the Eq. (2.7) from the P values.

```
#include <stdio.h>
float CONST= 79.57747155e-3;    //labda/(2pi*d), f=24GHz d=25mm
short s1, s2;
float deltaphi, division, theta;

float ThetaCalc(short p1, short p2, short p3, short p4){
  s1 = p1-p2;
  s2 = p3-p4;
  division = (float)s1 / (float)s2;
  deltaphi = atan(division)*CONST;
  theta = asin(deltaphi)*57.295779; // return as DEG
  return theta;
}
```

The FPGA code developing is more difficult, two Cordic cores for the trigonometric functions and all the others operations have to be implemented. The synchronization of all this components can be very hard and has to be designed with high accuracy. Furthermore, the VHDL code length and the code complexity is proportional to the internal variable's bit length, a good resolution required a lot of code lines. Anyway, for the nature of the FPGA chip this architecture allows to create an operational pipeline (if there are enough LEs available) that allows to increase the calculation throughput, where, for example, a single core ASIC can execute only one operation for time (one task). To develop the VHDL software faster IP libraries can be used for the single operations.
The drawback of the DC approach, independently on the architecture, is the needs of a high computational power.

For the DDS approach, using a lookup-table LUT, the output values of the computation are pre-calculated, with simulated inputs, and saved into a memory, by using a indexing function ϕ.
Before to be used, the Lookup-Table has to be created with all the possible input values. Then, with a simple software implementation inside the hardware,

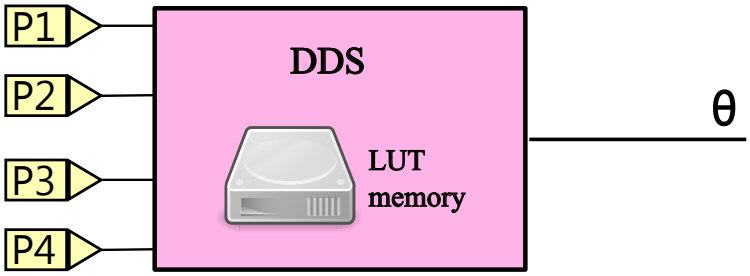

Figure 2.4: Flow-Chart for calculation of the the Eq. (2.7) by Lookup-Table.

any desired value can be addressed. A function ϕ can be used to manage the input values P1, P2, P3, P4 to give the memory references where to store the pre-calculated θ value.
This strategy decreases dramatically the computational requirements for the angle detection but increases the required memory space, more than the direct computation. Anyway, a new big matrix has to be calculated every time the constants change (the frequency f or the antenna distance d) whereas in the DC case it is enough to change the *const* value.

The LUT approach by using a bi-dimensional matrix implementation has been evaluated. Two 13 bit signed values calculated as $S_1 = (P_1 - P_2)$ and $S_2 = (P_3 - P_4)$ have been used for the matrix row and column selections (the ϕ function). The memory space occupied from the LUT is $M = 2^{13} \cdot 2^{13} \cdot 20 \approx 2$ Gbit. This LUT memory M determines the maximum memory space required for the DDS approach.
A possible C-code function to implement the DDS into an ASIC can be:

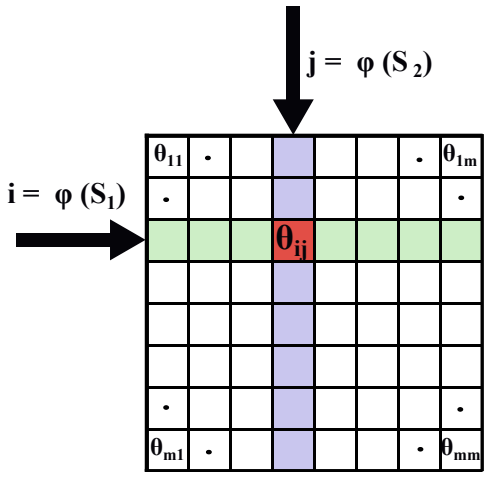

Figure 2.5: Search in the Lookup-Table the correct angle.

```
#include <stdio.h>
short s1, s2;
int index;
float LUT[8192][8192]; // The LUT memory

float ThetaDDS(short p1, short p2, short p3, short p4){
  s1 = p1-p2;
  s2 = p3-p4;
  theta = LUT[s1][s2]*57.295779; // return as DEG
  return theta;
}
```

The dependences of the P values help to reduce the LUT memory size M. The P values, along the angles of incidence, are sinusoidal waves with a 90 DEG offset between P1 and P2, P2 and P3, P3 and P4, P4 and P1. This dependences make S_1 and S_2 to be also sinusoidals with a 90 DEG offset.
In the ideal case, for the matrix indexing's construction (S_1 and S_2), it will be used only few values, representable as a vector, inside the matrix as shown in Fig. 2.6. From the complete matrix it is possible to extract this values and it is possible to obtains a vector with $2 \cdot 2^{13}$ values. The memory necessary to store this vector is $D = 2 \cdot 2^{13} \cdot 20 \approx 400$ kbit.
Keep in mind that, the LUT memory size is important. In fact, a small LUT

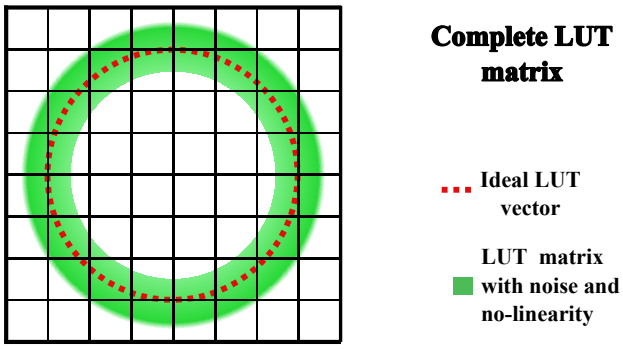

Figure 2.6: The matrix-values necessary for a Lookup-Table (LUT) in theory and in presence of noise.

can be obtain faster because require less computational power.

This ideal solution is not stable for a real case because, it does not consider noise or non-linearity in the input signals. The ideal LUT vector used in presence of noise or non-linearity produces as output unknown or wrong values.
To avoid this problem, the complete LUT matrix of size M has to be used for the detection. In fact, inside the LUT are presented all the possible values.
Anyway, it is possible to shrink the memory occupied from the matrix using a

statistical approach. In fact, only some cells will be selected during the measurements due to input noise.
Let's suppose to have a White Gaussian Noise (WGN) in the input signals, it is possible to define a Signal to Noise Ratio (SNR). With this SNR value it is possible to define the selectable LUT values around the ideal LUT vector (see Fig. 2.6 in green) and then to save only this values into the DDS memory.
With the Eq. (2.9) it is possible to define the width of the ring along the ideal LUT vector, where N is the SNR value and b the bit resolution of the incoming values.

$$c = \frac{2^b}{10^{N/20}} \ . \tag{2.9}$$

For the our evaluation we have been considered a SNR of 66 dB for the S_1 and S_2 values (2^{13} bit) and with the formula (2.9) 4 cells have been obtained. This means, all the cells with distance below 2 cells to the ideal LUT vector have to be stored in the LUT memory.
To store all this values we need to save, the ideal vector and all the cells far less than 2 from the vector. We need a memory of about $D \approx 2^{13} \cdot 2^5 \cdot 20 = 6$ Mbit to store all the cells.

From the evaluations done in this paragraph, the best hardware and software implementation for the angle detection has been resulted the complete computation implemented in a programmable processor ASIC. The easy code to program the processor and the simple code update (to change the *CONST* value), mixed to the computational power of the ASIC chips, produce a good system. Some ASIC processors moreover have inside a multi-core system, that allows to simulate a pipeline structure (run more tasks in the same time), and dedicate functions on hardware that increase the computational power.
The second choice it is still the ASIC architecture but with implemented the DDS technique. In this case it is possible to use a low-cost ASIC chip with a large memory. Anyway in this case it is necessary to compute a LUT matrix if the distance of the antennas or the frequency changes.
The FPGA system to implement a DDS can be used with good performances but the upgrading of the system could be more difficult than for an ASIC (in particular for the memory update). Instead, use a FPGA to calculate the Eq. (2.7) appear to be not convenient in therms of software develop time. Anyway, using the commercial IP library it is the fast approach but can be expensive.

2.2 Double instantaneous DOA measurements

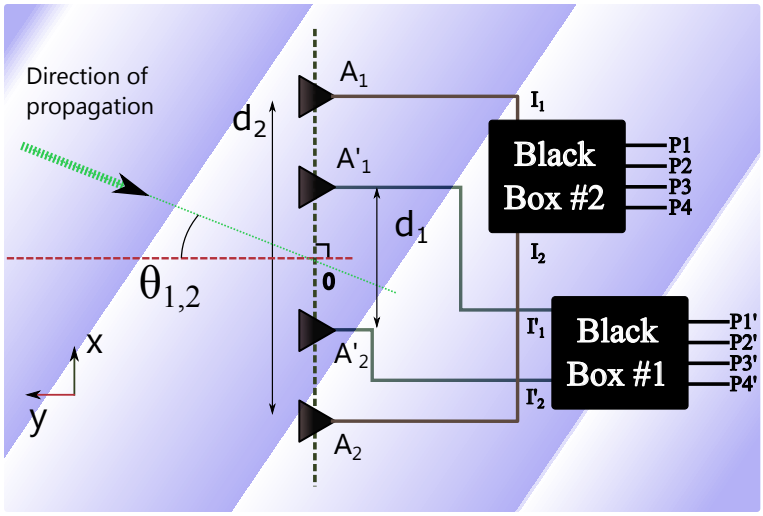

Figure 2.7: The parallel of two DOA system with antennas a different distance d_1 and d_2.

In the previous paragraph it has been shown that a two antennas array and a black-box can be used for the DOA measurement but that it is not possible to measure a wide angle with high accuracy.
These problems are overcome, with the introduction of a dual measurement of DOA (θ_1 and θ_2) from two different antenna arrays having different antennas distance.
As shown in Fig. 2.7 two black boxes are present working in parallel; a black-box (#2) with wide distance d_2 of the antennas is used to calculate with good accuracy the DOA angle θ_2. The second black-box (#1) with short antennas distance d_1 and wide detectable range is used to compensate the ambiguity of the first measurement [10].
Each back-box provides the system to calculate a DOA angle (θ_1 and θ_2) with the Eq. (2.7). The angles θ_1 and θ_2 are affected by the periodicity problem (see Eq. 2.8), with different periods due to the different antenna distances d_1 and d_2. The subtraction of these two angles (see Fig. 2.9) produces a step periodic function $\Delta\theta$, where the periodicity of this last function $P[\Delta\theta]$ depends on the ratio between d_1 and d_2. A wide periodicity of this subtraction ($P[\Delta\theta]$) allows to use the $\Delta\theta$ function to map the desired angle of incidence range that needs to be detected without ambiguity. With an appropriate factor $q = d_2/d_1$ it is possible to obtain this periodicity larger than the detection range.
A simulation of a 24 GHz EMC signal received from antennas with $d_1 = 18$ mm and $d_2 = 60$ mm (ratio $q = 3.33$) for instance, allows to detect an angle from -80 DEG to $+80$ DEG with no-ambiguity.

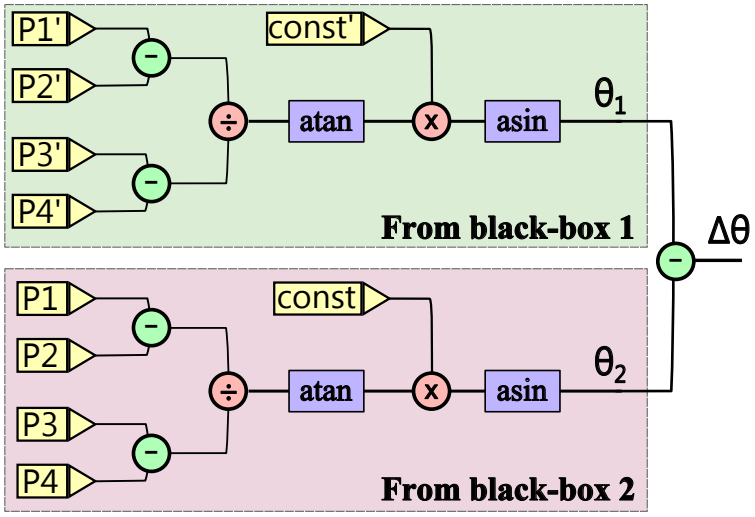

Figure 2.8: Computational flow-chart for the calculation of α with the Eq. (2.7) from the P values with a dual black-box.

The simulation is presented in Fig. 2.9. The P values of two black-boxes, considering the geometry and different efficiency of the channels, have been mathematically generated. With the subtraction of the simulated θ_1 and θ_2 angles of incidence has been produced the $\Delta\theta$ graph which has 13 different amplitude

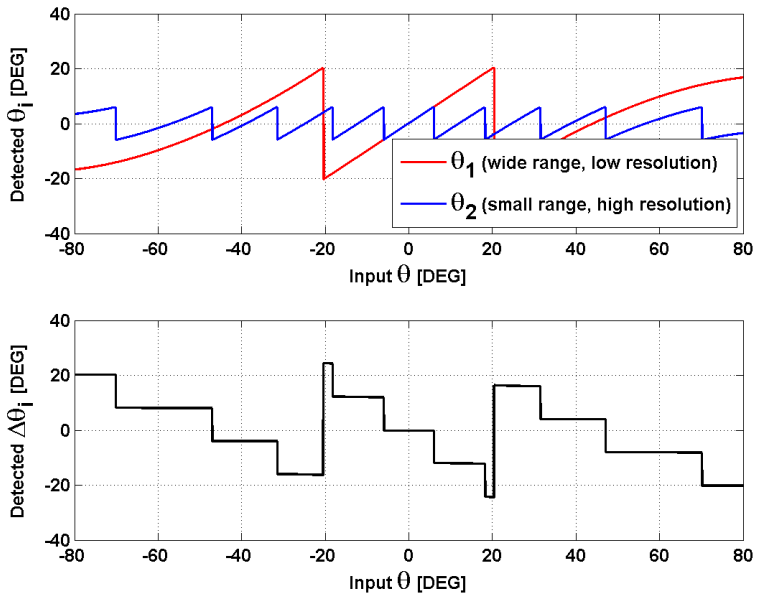

Figure 2.9: Simulation of dual DOA measurements with two pairs of antennas $d_1 = 18$ mm and $d_2 = 60$ mm and $\Delta\theta$ graph of the angle measured differences.

steps.
Once the detected θ_1, θ_2 angles and the $\Delta\theta$ graph have been obtained, it is possible to produce the correct DOA angle $\widetilde{\alpha}$ without ambiguity.

2.3 Measurements compensation

The simulation presented in the last paragraphs are affected by non-linearity in the angle detection. The distortion at large angles of detection (see Fig. 2.9) is caused by the geometry of the simulated system and by the trigonometric functions used in the equation (Eq. (2.7)) to calculate the angle. This distortion can be compensated with a calibration after production.
Local distortion of the angle detected are caused by different efficiency of the real black-box outputs, this different efficiency have been considered in the simulations.
This paragraph explains how to compensate the different outputs efficiency of the black-box to obtain a correct $\widetilde{\alpha}$ angle detected from the the θ detected angle .

In the first simulation, of a single black-box with the antennas at $d = 5$ cm (see Fig. 2.2, b), the subtraction of the simulated detection with the ideal angle provides the angle detection error, represented in Fig. 2.10. We would to compensate the measurements to reduce the detection error ideally to zero [10].

A polynomial compensation function can not be used, without big errors,

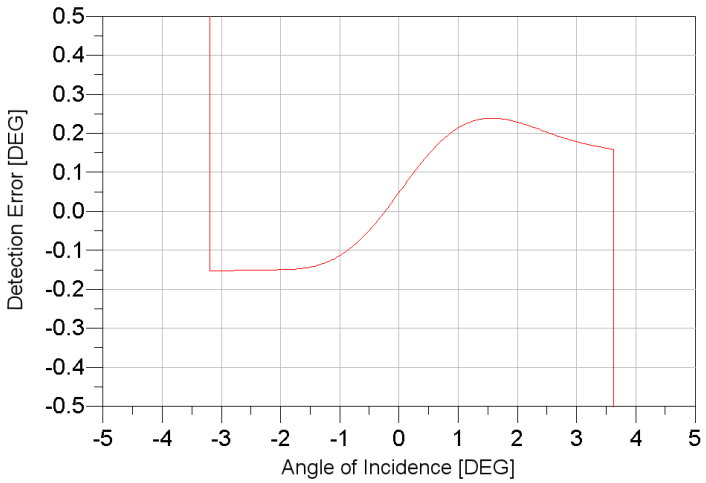

Figure 2.10: Angle detection error between measured (θ) and incident (α) angles with a single black-box, antennas at $d = 5$ cm and wave at 24 GHz (simulated).

due the angle detected periodicity which have a spot angle errors (Fig. 2.9).
It is possible to compensate the angle with a polynomial compensation function defined into angle domains. Using, for instance, the $\Delta\theta$ graph, it is possible to split the detectable angles into regions and to produce the compensation function with a polynomial fitting of the errors. Different function orders, number representation and resolutions have been evaluated. A 5th order polynomial function with coefficients quantized to fix point (9 bits integer and 11 bits decimal) has been a good solution in terms of fast computation and low memory requirements. To compensate the Fig. 2.9 which has 13 angle domains with 5th order functions it is necessary a memory of $C = 13 \cdot 6 \cdot 20 = 1560$ bit.
Also a DDS system can be used for the measurements compensation. For each angle detected it is possible to store the detection error and then to save this value inside a LUT. Supposed to have a correction error of 20 bit, it is necessary a LUT memory space of $M = 2^{20} \cdot 20 \approx 21$ Mbit.
A DDS and domains polynomial compensation have been compared in terms of error after the compensation ($\widetilde{\alpha}$ error) in a observing range -80 DEG to 80 DEG. A 20 bit format, with 9 bit signed integer and 11 bit decimal, have been used for the measured angle, for the coefficients of the 5th order functions and for the LUT matrix values.
The compensation of the simulation of a dual DOA measurement (see Fig. 2.9) using $d_1 = 18$ mm and $d_2 = 60$ mm has been processed. The domain polynomial compensation and the DDS as explain before have been used to compensate the angle detected (without geometrical compensation).
The result of the subtraction of the compensated value with the ideal angle is presented in Fig. 2.11.
From the figure it is possible to see a good compensation of the DDS system in all the observing range. The angle detected $\widetilde{\alpha}$ after the compensation has an error lower than $0.5 \cdot 10^{-3}$ DEG. The positive error is due the quantization errors of the LUT values. Instead, the polynomial compensation presents 13 peak with high values in the borders between different angle domains.
From this comparison, the DDS system has been resulted the best solution to compensate the angle detected from the non-linear response of the black-box outputs.

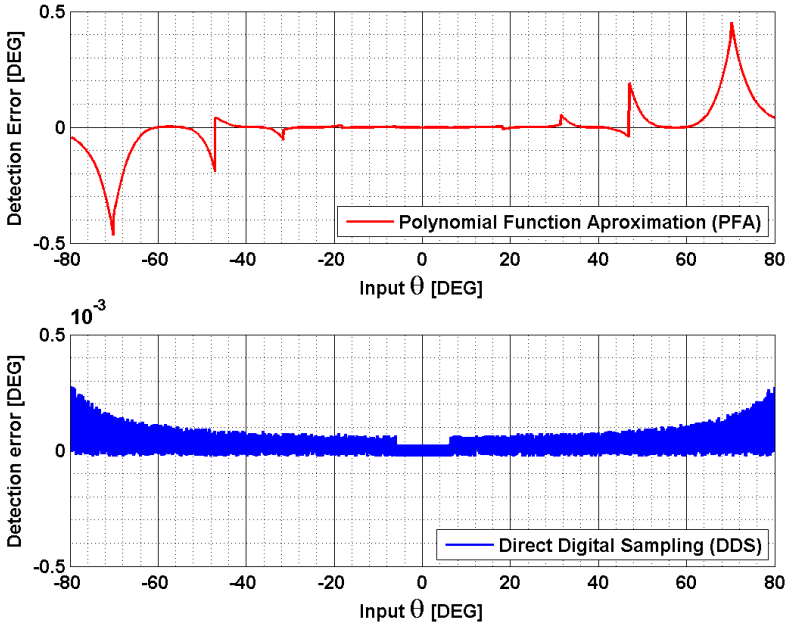

Figure 2.11: Angle error which affect $\widetilde{\alpha}$ using a polynomial function or a DDS system to compensate the different channels efficiency of the black-box's outputs.

Chapter 3

Wide Angle, Dual Six-Port Based High Resolution DOA Detector

The dual Six-Port DOA detector is an innovative small and portable all-in-one stand-alone device capable to detect the angle of arrival of a RF wave with high accuracy and wide angle detection.
The simultaneous high accuracy and wide angle detections of the DOA detector has been obtained by using a parallel of two Six-Port DOA detectors, as foreseen in previous chapter. In fact, by using two parallel DOA systems with different distance of the antennas (d_1 and d_2) [11], it is possible to increase the measurable angle range with no-ambiguity, moreover a better accuracy is obtained.
The project has been carried out in collaboration with the Lehrstuhl für Technische Elektronik (LTE) Department (with the group of Dipl. Ing. Gabor Vinci, PhD) of the Friedrich-Alexander University, Erlangen-Nürnberg, that set up the project, and that developed the RF site. The system development has been organized in blocks to execute specific tasks: acquisition, radio-frequency processing, digital conversion, digital processing and auxiliary.
For each blocks, a module has been developed to execute the assigned task; a prototype has been produced and then tested.
This chapter presents the concepts and gives some details for the final design (v.2) of the dual DOA detector. This version has been sent to manufacture.
The thesis work consisted in the development of the digital conversion and feed-

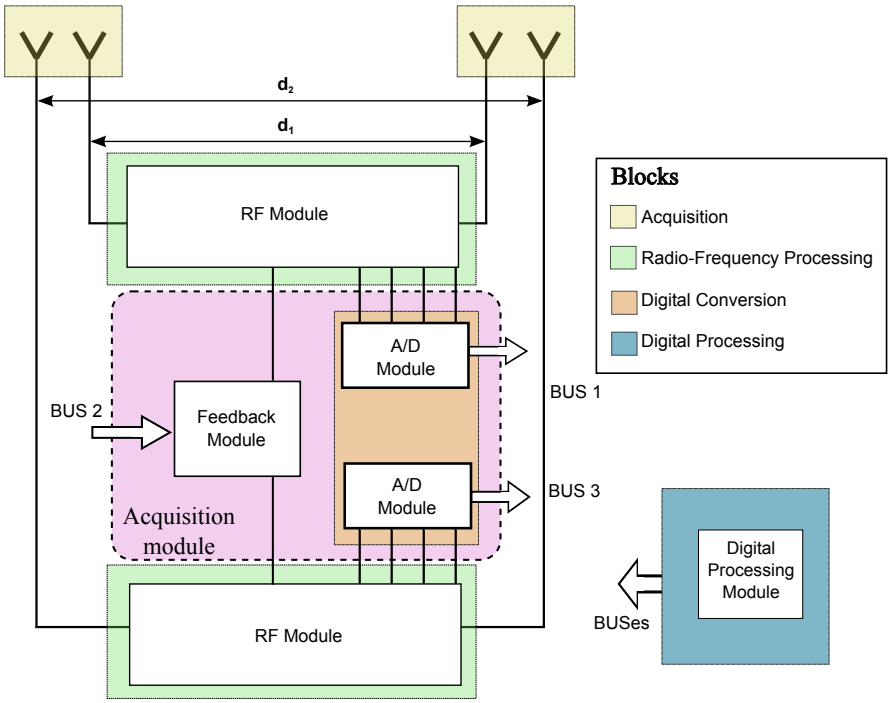

Figure 3.1: Blocks and modules scheme of the Dual DOA detector.

back blocks that will be presented in the following. The experimental work, conducted on prototypes, are presented in the next chapter (4).

Project organization

The blocks are organized in such a way that the acquisition block receives the electromagnetic signals with an antennas array, the radio-frequency block process the RF signals with a six-port based interferometer network and converts them into analog baseband signals. The digital conversion block, provides the A/D conversion of the baseband signals. The digital processing block provides the digital signal processing to calculate the Direction Of Arrival angle. Moreover, a auxiliary block has been developed to control the RF components to have the best analog baseband signals and avoid saturation of the RF components.
The creation of prototypes has been fundamental for the design of the final board (v.2), as it allowed to find and solve problems for the final version.

Antenna block

This block is used to receive the radio signal waves and feed the signals to the RF inputs channels of the radio-frequency processing block.
The antenna module, implementing the antenna block, consists of two patch antenna pairs built into a PCB board. Each antenna of each pair is equidistant from a common point used as origin, moreover the antennas are located along a common axis. As presented in the previous chapter, the ratio of (q=3.33) between the distances $d_1 = 18$ mm and $d_2 = 60$ mm allows to measure with non-ambiguity an angle range of $|\alpha| < 90$ DEG.

Radio-frequency processing block

The radio-frequency processing block is the core for the dual DOA measurement, which provides the linear combinations of the inputs as required by Eq. (2.2-4). The calculation of the DOA angle is performed in the digital processing block.
The signal process has been realized with two Six-Port interferometers, each for one pair of antennas. The two Six-Ports are included into two identical branches (see Fig. 3.2) forming the RF module. The four output channels (P_1, P_2, P_3 and P_4) are the linear combination of the two inputs (P_{a1} and P_{a2}) according to Eq. (2.2-4). The two incoming signals undergo a dual stage amplification prior to enter the Six-Port network.
The four output channels of the Six-Port and down converted by RF Detectors; these convert RF power into amplitude modulated voltage signals. The signals are then amplified to reach the specification of the input stages of the Acquisition (A/D) module using Baseband (BB) Amplifiers.

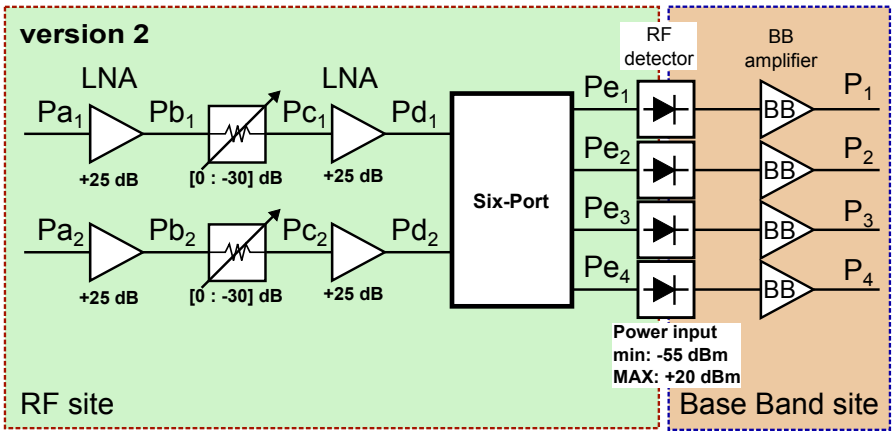

Figure 3.2: Scheme of one Phase Measurement Detector inside the RF module v.2.

In this module two Hittite HMC751LC4 LOW NOISE AMPLIFIER, 17-27 GHz (LNA) have been used, with a fix gain of +25 dB and a maximum input power of -5 dBm with, in between, an Hittite GaAs MMIC VOLTAGE-VARIABLE ATTENUATOR, 5-30 GHz with gain between 0 and -30 dB.

The Six-Port used is a passive interferometer, hybrid couplers based, with two input ports and four output ports [9] designed with for 24 GHz EMC signals.
The inner transmission line structure of this passive component consists of three $\pi/2$ hybrid couplers and one Wilkinson power divider (Fig. 3.3).
The input signals ($I_1 = Pd_1$ and $I_2 = Pd_2$) crossing the component are sent to the four output gates ($O_1 = Pe_1$, $O_2 = Pe_2$, $O_3 = Pe_3$ and $O_4 = Pe_4$) with fixed different phase shifts of 0, $\pi/2$, π and $3/2\pi$.
The four outputs related to the input signals according to:

$$O_1 = \frac{1}{2}(I_1 + jI_2); \tag{3.1}$$

$$O_2 = \frac{1}{2}(jI_1 + I_2); \tag{3.2}$$

$$O_3 = \frac{1}{2}(jI_1 + jI_2); \tag{3.3}$$

$$O_4 = \frac{1}{2}(I_1 - I_2); \tag{3.4}$$

Radio-Frequency (RF) Detectors are passive transducers used to convert power-modulated microwave signals into voltage-modulated baseband signals. Each Six-Port output channel is terminated with a RF detector. Schottky diode, also known as *hot carrier diode*, is the most common used device for his low drop

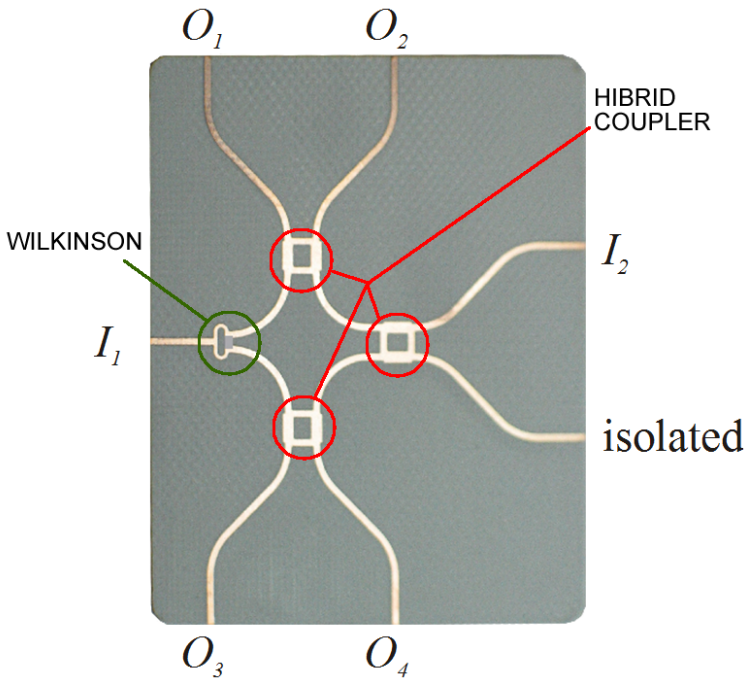

Figure 3.3: The Six-Port component.

voltage and for the quadratic relation between voltage and current.
To create a RF Detector diode based, three components are needed: a filter (F), a diode (D) and a capacitor (C) as shown in Fig. 3.4.
The filter allows to shape the input signals frequency spectrum. A RF choke,

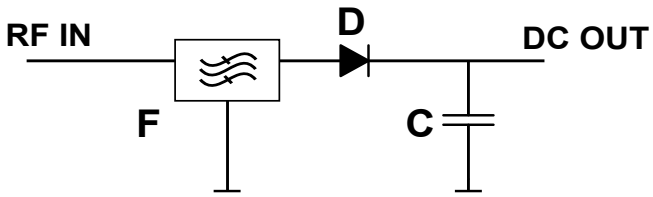

Figure 3.4: Scheme of a diode microwave detector.

typically a stunt inductor, is placed across the detector diode to avoid DC component passing over the diode. This creates a high-/band- pass filter and the DC component of the RF signal is dropped to ground. The diode makes the detection of the power using his quadratic relation between voltage and current; the current charges the capacitor C, with a charge related to the input power level.
In the literatures several schemes for diode detector are available. By changing topology and components it is possible to change the transducer dynamic range. Two topologies with a resistance stub (for best network match) and with a LC

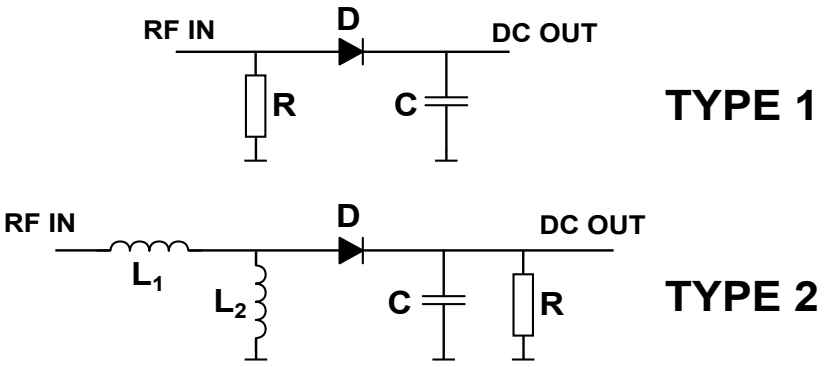

Figure 3.5: Different RF Detector topology.

stub (for best filtering) have been chosen to be compared.
The two topologies compared for this project are shown in Fig. 3.5, where the RF power detector Type 2 has obtained the best performance in therms of power detected range (see next chapter).

Digital conversion block

The digital conversion block provides the conversion of the eight analog signals that underwent the phase shift in the previous block.
The task of this block has been realized with the A/D module which consists in a parallel of eight ADCs, one for each analog channel coming from the RF module (P1-P4 per branch). The simultaneous sampling of the eight channels is critical for this module. In fact, with a simultaneous sampling it is possible to reconstruct the phase of the signal received from the antenna module. ADCs system with 8 input simultaneous sampling channels with good resolution are

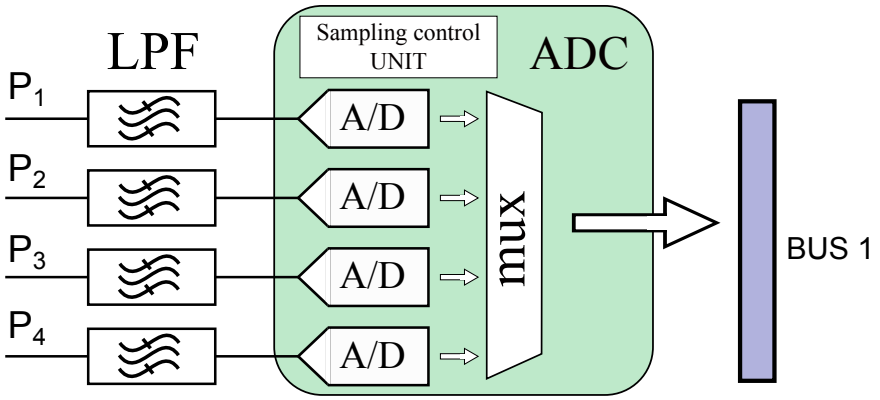

Figure 3.6: Scheme of a A/D module branch implementing the digital conversion block.

expensive and not so common in the market. The module has been developed with two branches within a single ADC 4 input simultaneous sampling channels each. This solution is considered the best trade-off between performance and costs.
The signal is then converted into digital domain for the digital processing block. In Fig. 3.6 a A/D module branch is presented. A 8th order Butterworth low pass filter (LPF) obtained with a Linear LTC1562-2 is placed before the ADC to avoid the Aliasing (see Sampling Theorem). Then, the ADC is a TI TLV5626 with four 12bit input channels, simultaneous-sampling, 680 ksps with parallel interface. Internal to the TLV5626 (ADC) the four A/D samples are multiplexed externally and directly connected to the DSP module via BUS 1.

Digital processing block

The digital processing block provides the digital processing of the sampled data and some controls. This task is deputed to a stand-alone external board able to control the sample acquisition, to process the data and to send the computation results to another external device (a computer).
The module must provides the value of the DOA angle θ according to Eq. (2.7) two times (one for each Six-Port). The calculation has to be performed within the period of the sampling frequency.
The module provides the control of the amplification stages in the RF module to guarantee a good measurement and to avoid component saturation. To do this, it has some digital and analog lines to the controls (provided by auxiliary block).
To implement the digital processing block an Altera DE2 board is uses.

Auxiliary block

The auxiliary block provides interconnections of the digital control signals for the RF module.
The Feedback module, which implements the auxiliary block, is based on variable resistances and DACs. A branch of the Feedback module is shown in Fig. 3.7, where the BUS 2 receives the control signals from the DSP module. The variable resistances are used to adjust the gain of the BB amplifiers (via the connections CHA-CHD) whereas, the DACs provide analog voltages (Attenuator_A and Attenuator_B) for the attenuator in the dual stage amplification.
For the DAC a TI TLV5626 8bit is used and for the variable resistances is used a Microchip MCP42100.

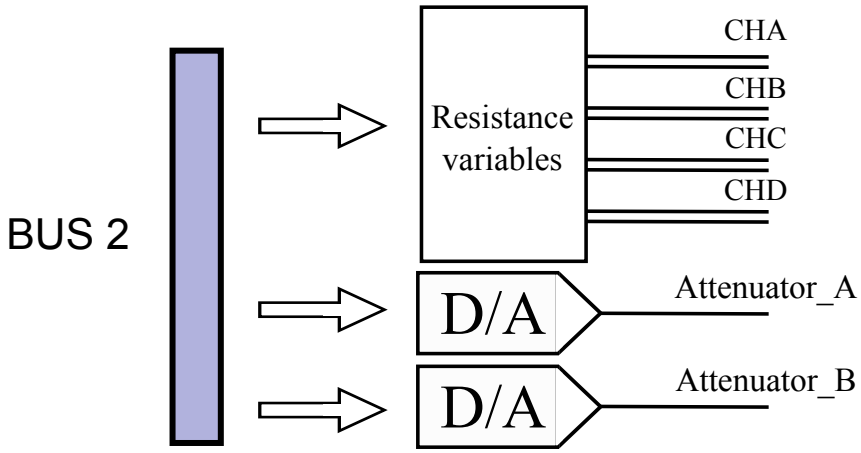

Figure 3.7: Scheme of the Feedback module branch implementing the auxiliary block.

Chapter 4

Development of a system for DOA measurements

This chapter collects and presents the experimental work that has been used for the development of the final version of the dual DOA detector Six-Port based. The work consisted in the :

- measurements of the RF module prototype;
- the design and the test of the A/D module prototype;
- the test on a DSP module;
- the design and the test of the Feedback module prototype;
- the design of the final A/D and Feedback module version assembled into the final board.

4.1 Tests on the RF module prototype

The development of the A/D module required test measurements on the output channels of the RF module prototype. The RF module Prototype with a singles Six-Port receiver front-end module used for the measurements is shown in Fig. 4.1. The board consists of a high-frequency Rogers 4003C Substrate laminated on an FR4 0.5 mm material for mechanical stability.
There are two input lines (Pa) with a amplifier stage (a LNA and a RF variable attenuator). Then, the Six-Port network which have four output lines (Pd) fed to pass-band filters (BP filter). Then, RF detectors are placed to convert the RF into baseband signals.
In the final stage, baseband amplifiers, with gain x100, amplify the baseband signals to reach a a minimum voltage output of 0.004 V.
The photo and the block-scheme of the RF module prototype is shown in Fig.

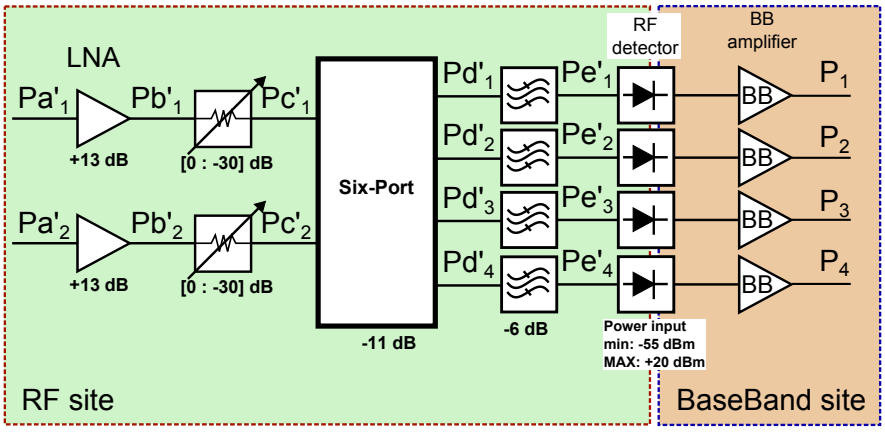

Figure 4.1: Scheme of the RF module prototype.

4.2.
In the front-end of the RF module, an LNA: Hittite HMC341LC3B LOW NOISE AMPLIFIER, 21-29 GHz, with a fix gain of +13 dB and a maximum input power of +5 dBm has been used. Following, there is an Hittite HMC812lC4 GaAs MMIC VOLTAGE-VARIABLE ATTENUATOR [0 30] dB, 5-30 GHz to adjust the power going to the Six-Port. *Signals passing through the Six-Port undergo to an attenuation of about 11 dB.* The filter is a pass-band filter based on a three stage coupled line filters with 24 GHz center frequency and a bandwidth of 2 GHz. Finally there is a diode power detector with a baseband amplifier (BB). The diode mounted is a *MZBD-9161* from Aeroflex Metelics (GaAs beam lead Schottky diode). The presence of the attenuator prevents the saturation of the detector for incoming high power signals.
The two inputs of the RF module are provided through two edge-mount k-

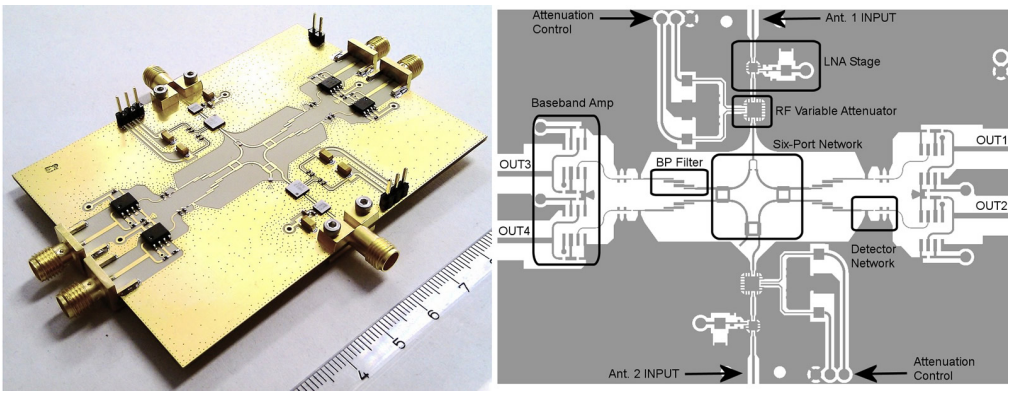

Figure 4.2: The RF module prototype.

connectors (2.92 mm, *antenna input connector*) while the four outputs are routed on SMA connectors (*base band output connector*).
To properly use this RF module a set of measurements have been carried out. A correct sampling of a signals out coming from this module required the knowledge of the response of the RF diode detector.
Measurements on the diode power detector module provided the voltage output when RF power signals are fed in input. Fig. 4.3 shows the scheme of the connections used during the measure. An Agilent E8267 power generator and a Keithley 2612A were used. The system was controlled via Ethernet network from a computer with a Matlab script (*diode_sweep.m*). Ten amplitude sweeps in the frequency range between 23 and 25 GHz were programmed in the power generator and then the data were acquired from the Keithley multimeter.
The voltage output at the diode detector with a power amplitude sweep input signal at 24 GHz is reported in Fig. 4.4. From this measure it was possible to see that the diode power detector starts to measure form a power of about -55 dBm. With the data collected form the measure and the specifications of the

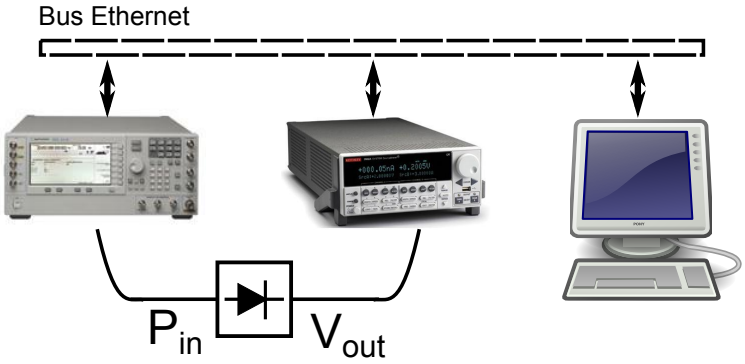

Figure 4.3: Scheme for the connections used to measure the power at the diode detector used in the RF module prototype.

RF module components, it has been produced the Table 4.1 with the power level working range of this module.
The maximum power level incoming in the RF module (Pa') is limited by the

Table 4.1: Power level working range of the RF module prototype (Fig. 4.1) determined from the test measurement and components specifications.

Power	Pa'	Pb'	Pc'	Pd'	Pe'
Maximum	+5 dBm *	+18 dBm	+18 dBm	+7 dBm	+2 dBm
Minimum	-51 dBm	-38 dBm	-38 dBm	-50 dBm	-55 dBm **

* maximum input power level for the LNA component.
** sensitivity level of the RF GaAs diode detector.

maximum power input of the LNA (fix to +5 dBm). Instead, the minimum power level (-51 dBm) is estimated as the minimum power that is detectable at the RF diode detector (minimum Pe'=-55 dBm). The RF module prototype has so a dynamic range of 56 dB to the antenna input connector, and 57 dB of dynamic range to the SMA output connectors.
This value is important for the ADCs choosing in the A/D module.

4.2 A/D module prototype developing

The A/D module is used to bridge the analog part (RF module) to the digital one (DSP module). An A/D module prototype has been developed and created, based on a small board for the RF board prototype. The A/D prototype has been designed with a filtering stage and a A/D converter stage. The board has four input connectors to be connected to the analog signal outputs of the RF module. A dedicated connector is used to transmit data (Fig. 4.5) to an external

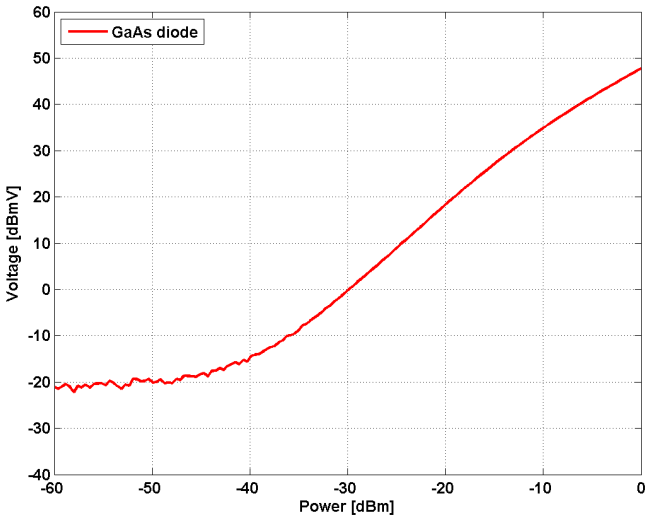

Figure 4.4: Voltage output of the RF detector module with a power amplitude sweep input at 24 GHz

board used as DSP module. The same connector was used to receives controls. The requirements for the A/D converter stage have been extracted from table 4.1. The A/D converter stage needs at least 10 bits per channel to acquire correctly the four analog signals (which they have a detected dynamic of 57 dB) coming from RF module outputs.

The A/D module developing started with the Texas Instrument TLC3541 ADC's. The TLC3541 has been allowed to create a real prototype. These converters are single channel 14 bit ADC, 200 ksps, rail-to-rail, with serial interface. The chip is powered by a single 5 V line.
With the TLC3541 chips, a simple four channel A/D module able to measure positive baseband signals with analog bandwidth of about 50 ksps, maximum amplitude of 4.95 V and an accuracy of 0.3 mV has been developed.
Before each ADC a first order filter has been inserted. This component allows to reduce the incoming analog bandwidth to prevent aliasing effects (to satisfy point 1 of the Sampling theorem). To keep the prototype simple, a single R-C filter was placed. The filters were designed with a cut frequency (-3 dB) at 2300 Hz. The chosen values of R = 1 kΩ and C = 68 nF were able to guarantee an attenuation of -37 dB at 100 ksps (the minimum Nyquist's frequency).
This value was the best trade-off between a good filtering and best pass band, but, the attenuation of 37 dB at 100 ksps does not allow to use all the 14 bit of the samples. In fact, a 14 bit sample allows to measure a dynamic of 84 dB, to measure 37 dB only 7 bits are needed. Anyway, all the available bits have been

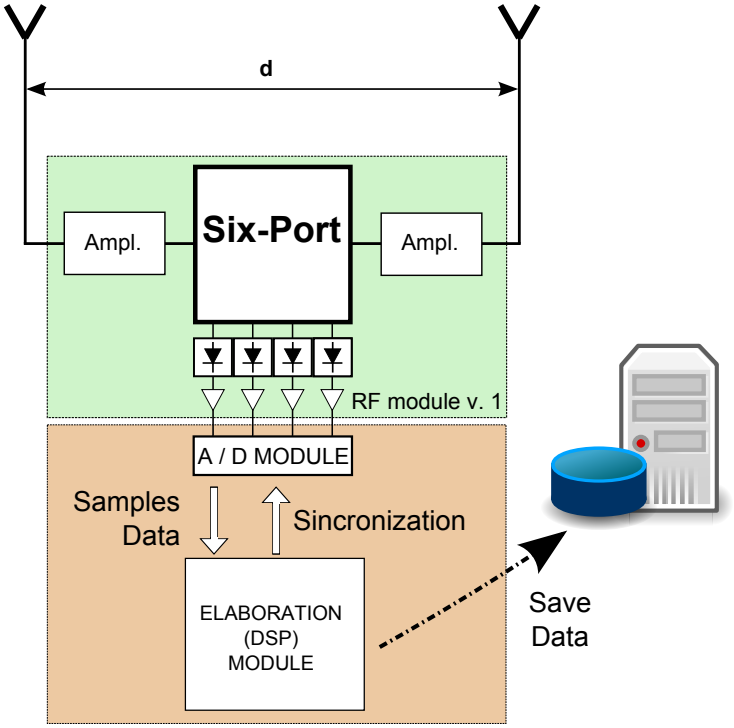

Figure 4.5: Scheme of the prototype system.

chosen to use, significant and insignificant, to keep the computational requirements closer to the final version of the DSP module.

An *Altera DE2* board (Fig. 4.6) has been used as DSP module to process the acquired digital signals and control of the A/D module. The Altera DE2 is a Development and Education board for the Altera's University Program, based on a FPGA chip: *Altera Cyclone II EP2C35F672C6* with EPCS16 16-Mbit serial configuration device.
The FPGA chip allows a parallel execution of tasks and to create clock signals. A FPGA board has been chosen to be used, in particular the Altera DE2, for the flexibility of his architecture and because it can implements internally a soft-core microprocessor called *Nios Core II* (a programmable ASIC processor).
The Altera DE2 board has a lot of interfaces, in particular: two 40-pin GPIO expansion headers (General Purpose I/O), an Ethernet interface and a serial RS-232 port [12]. We has been chosen to use one GPIO header to connect the DE2 board to the acquisition module prototype. The DE2 provides through this header 36 GPIO lines (CMOS 3.3 V), and can transmit and receive digital signals from the A/D module. From the same interface the DE2 board provides two power lines (+5 V and +3.3 V) with grounds. From these power lines, it has been possible to power the components on the acquisition prototype.

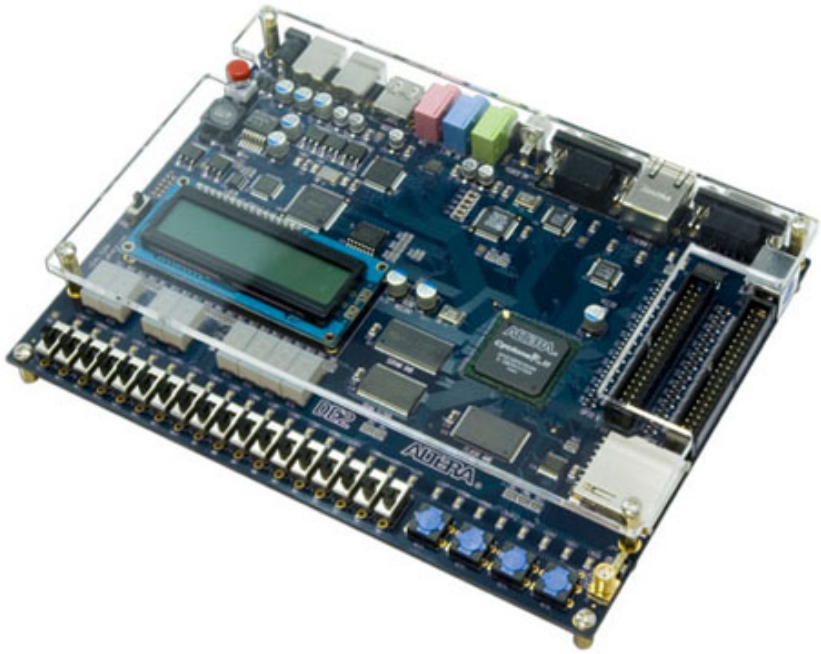

Figure 4.6: The Altera DE2 board.

A/D board prototype development

The A/D module has been implemented in hardware with a prototype PCB designed with Altium Designer Winter ed. 09.
This is a professional CAD software for scheme and PCB design. The requirement for the board were: small area, space for filters and ADCs, connectors for the analog signals and space for a 40-pin input male connector for the digital data and the power supply.
A sheet has been created of the electric (analog, digital and power) lines inside an Altium project. With the internal components library, each component has been inserted in the sheet with reference to his footprint. A new entry has been created in an external library file when the component's footprint was not available.
The internal blocks of the PCB are shown in Fig. 4.7. A single power line (*+5 V*) is provided from the 40-pin connector (*P1*) and from an external connector (*P0*) as backup. To use the power line coming from the Altera Board, the R0 resistance (0 Ω value) has to be insert. To receive the four analog data from the SMA output connector of the RF module, four MCX connectors (*P11, P22, P33, P44*) have been included. Between each MCX connector and the ADC input pin a R-C filter has been inserted. The ADC's reference pin have been connected to the +5 V line to measure an analog input voltage between 0 to

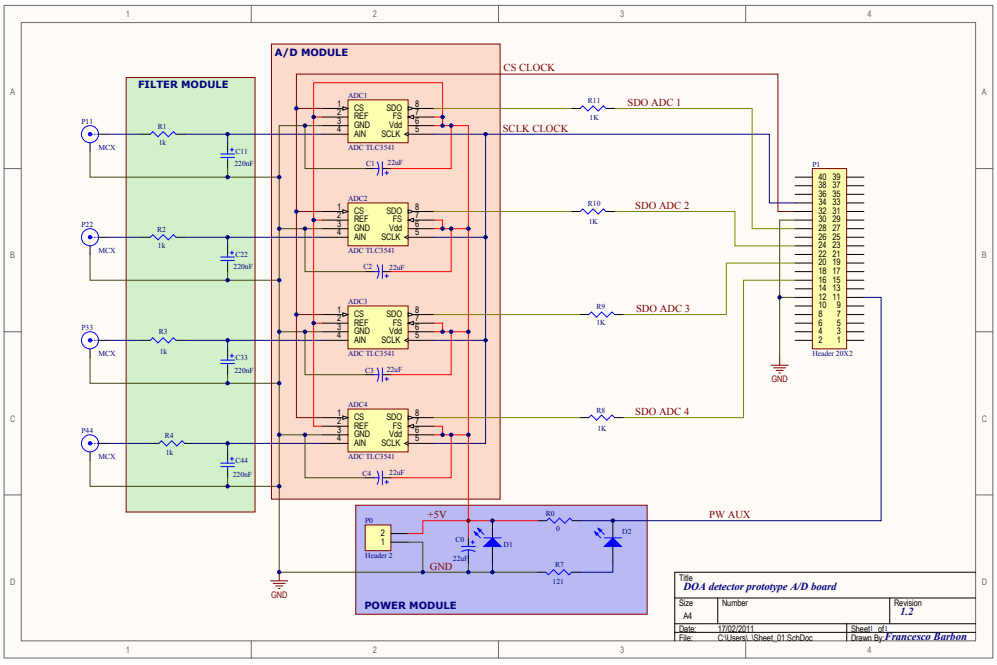

Figure 4.7: Scheme sheet of the DOA acquisition system prototype in Altium.

4.95 V.
There was a problem of voltages compatibility between the ADC's digital line and the Altera GPIO lines. It has been solved with a 1 kΩ resistance inserted in series to the lines. In fact, the DE2 GPIO lines works with digital signals at 3.3 V, instead the ADC's have the digital site at the same voltage of the power line (5 V). For the ADC's voltage tolerance they can receive, clock and sync signals from the Altera board, but the DE2 can't receive 5 V as input. Indeed, each GPIO line on the DE2 expansion headers is connected to two diodes and a resistor that provide protection from high and low voltages. If it is set in input a voltage more than 4 V, these components burns out. The resistor of 1 kΩ with the cooperation of the DE2 GPIO voltage protection system allows to "adapt" the 5 V to the 3.3 V, DE2 voltage standard.
Correlate with the GPIO position to reduce the size and the complexity of the line routing we have been chosen the position of the digital pin and the power supply lines.

Also the PCB layout has been designed with Altium Designer.
Following with the Altium project it has been possible to import the sheet, before made, into the PCB layout. By means, footprint of the component and the interconnections reference between the pins have been imported into a PCB layout sheet. The placing and routing of the components and of the networks have been made by hand.
The PCB designed is a dual layer board, 46 mm width and 55 mm height. In

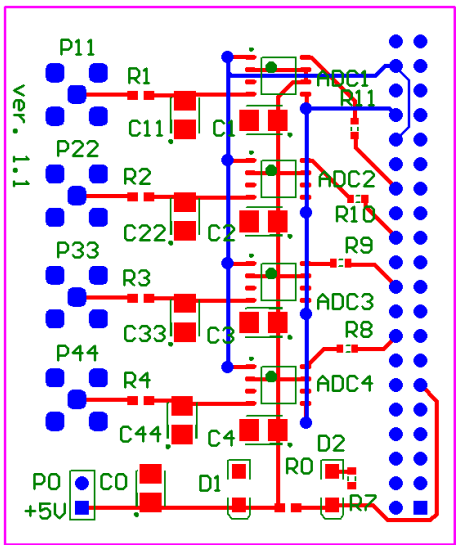

Figure 4.8: Prototype PCB Layout: Top Layer (red) and Bottom Layer (blue).

this area, a 40-pin connector, four ADC's, four MCX connectors with a R-C filters network have been placed. In Fig. 4.8 is possible to see the top (red) and

bottom (blue) layers, the green color is the top overlay.
Each ADC needs a 12.5 MHz serial communications clock (SCLK). This signal with the chip select (CS) have been router in the bottom layer, instead the analog and digital serial lines in the top layer to avoid electromagnetic problems. It has been chosen a Daisy-Chains topology of the digital clocks to reduce the routing complexity. Although the system needs a simultaneous sampling, with a low routing path and a high speed serial frequency this topology would not be a problem. To prevent electromagnetic interferences the PCB layout has 62 ground via.
The PCB rendering of the A/D module is shown in Fig. 4.9.

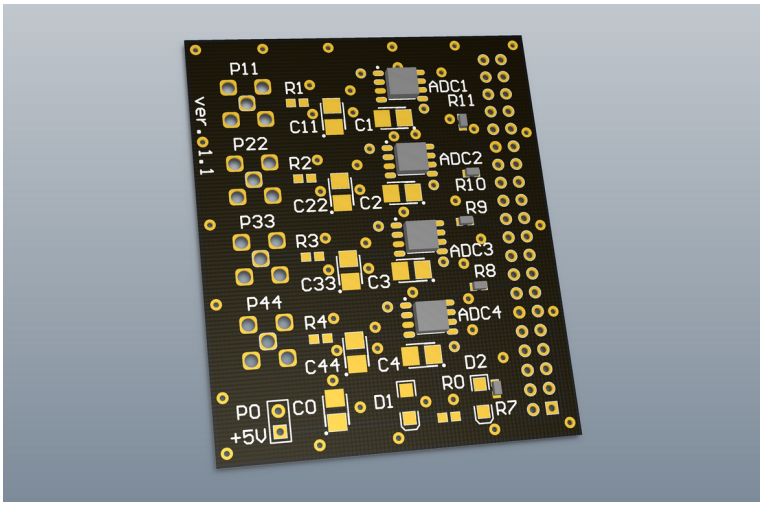

Figure 4.9: Prototype PCB rendered Layout.

This board has been produced, in FR4 substrate with gold plated soldering pad, by a manufacturer in Germany.

4.3 Software prototypes for the A/D board

The software for the Altera DE2 board and the computer had to be implemented to test the A/D module prototype and for test of the equation (2.7) calculation. Two software versions working with the A/D module prototype have been created for calculate the measured angle θ (the compensation has not been implemented). The first version, programmed in VHDL only, makes the DE2 board to send the four sampling data in raw mode (*Acquisition P*). In the second version the Nios Core, implemented inside the FPGA, calculates and sends the measured angle θ (*Acquisition Theta*). The last software has been programmed in VHDL for the FPGA and C-code for the Nios Core II. For each version a Matlab script for the computer has been developed.
To connect the DE2 board to the computer the serial port of the DE2 board

has been used. The Ethernet connection was not considered. because it needs a serial programming to be programmed (worst in VHDL) and for the Nios Core II drivers were not available for the suite used.
A standard, to transmit correctly the data through the serial port, was necessary to be developed. In fact, the transmitted data are longer than 8 bit (the biggest packet for the serial port). The DE2 board for example in raw mode acquires in the same moment four 14 bit values from the ADC (P1, P2, P3, P4). These values are totally 56 bit (a DOA sample) and they have to been transmitted through the serial port, it means to create least 7 packets.
The maximum speed of the serial port is 115200 bps (Bit per second) in 8-N-1 mode, the maximum transmission bandwidth of the system sending raw data (slower than the ADC sampling rate) is about 2000 sps. The Ethernet port would be the best solution, because a datagram can be 1500 byte long and the speed is more faster (100 Mbps), it would be able transmits about 1.5 Msps.
Header and frame packets have been necessary to be introduced for the serial transmission. The header has been used to keep the frame synchronization while the frames to transport the data samples. We have been chosen to send the 14 bit samples expanded to 16 bit adding zeros for padding. This force the DE2 board to send 8 serial packets instead of 7. Anyway, this allowed to use only 2 serial packets with value 0xFF as header, with absence of collision. In facts, if an ADC measures the maximum value (0x3FFF equivalent to a voltage of 4.95 V), in the serial port will be sent the packets: 0xFF and 0x3F in the first and second packet respectively. The synchronization is made with the check of the header pattern, looking for the first two sequential packets with the value 0xFF. With this standard we have been able to develop Matlab scripts working with both software versions in the Altera board.
In the Acquisition P version, this standard reduces the theoretical transmission bandwidth to 1440 sps (-28% from the raw data sending).
In the Acquisition Theta software, the DE2 board has to compute the DOA angle and send it through the serial port. We chosen to send an angle of 16 bit (two serial packet) with a two-packet headers. In this case the theoretical transmission bandwidth is 3600 sps (-50% from the maximum 7200 sps).
With an angle resolution of 16 bit the software is able to measure an angle range of 180 DEG with resolution of 0.0027 DEG.

In Altera Quartus II 10 x64 with Altera University Program (AUP) IP Core the software for the Altera DE2 board have been developed in VHDL code, and with Altera Nios II Embedded Design Suite (EDS) 10 x64, in C-code.
The VHDL code compiled has been stored in the EPCS16 chip. On the DE2 boot this chip configure the FPGA's logic cells automatically.
The *Acquisition P version* is a group of VHDL modules implemented and compiled for the FPGA Cyclone II with Quartus II. The core module is the *acd_ control* which manages the connection between the DE2 and the acquisition boards. In

facts, it provides to the acquisition board the synchronization clocks (SCLK and CS), it receives from the four ADC's the serial samples and provides the de-serialized samples to the other internal modules (P1, P2, P3, P4). A modules system have been developed and implemented inside the FPGA, working with the *adc_ control module*, that provides moreover the transmission of the samples through the serial port.
The clocks have been generated from an internal signal in the DE2 board at 50 MHz, with counters.
The Acquisition P modules and the main digital interconnections implemented

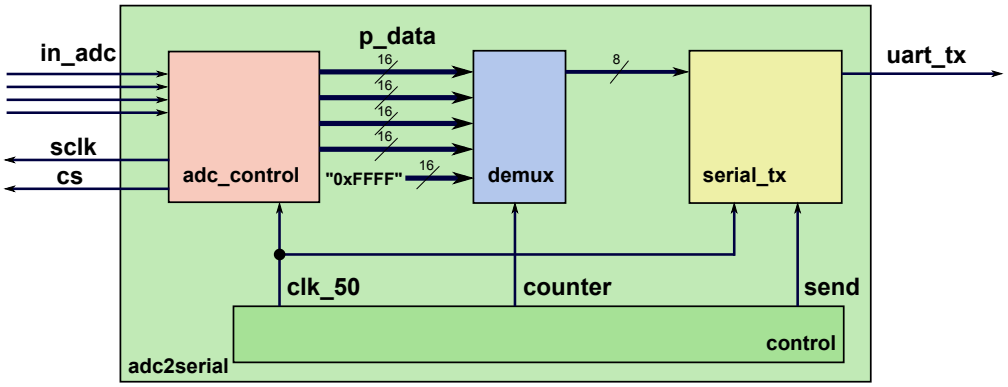

Figure 4.10: Module interconnection in Acquisition P version.

inside the FPGA are shown in Fig. 4.10.
The results of the compilation in Quartus were:

```
Analysis & Synthesis Status : Successful
[...]
Top-level Entity Name : adc2serial
Total logic elements : 553 / 33,216 ( 2 % )
Total combinational functions : 545 / 33,216 ( 2 % )
Dedicated logic registers : 303 / 33,216 ( < 1 % )
Total registers : 303
```

A correct compiling makes to use only 2% of the internal LEs inside the FPGA. This mean, it is posible to implements other operations inside the Cyclone II (for example the operations needed in the Acquisition Theta software).

The *Acquisition Theta version* needs some critical operations: division, multiplication and trigonometric functions.
The generation of the source code in VHDL, without IP library, it is a cumbersome. A multiplication is possible to be used also for the division: the dividend has to be multiply by the inverse of the divisor. The multiplications are easy to implement, for example with the RAG strategy [13][14], but it works only if there

is a fix therm. In the Theta formula, the first operation has each time a different dividend and divisor (P1-P2)/(P3-P4) so it is not possible to implement a RAG system. It is possible to implement a programmable multiplication in VHDL, but the program needs a lot of logic elements (if dedicated logics are not available) and it has a long computational delay. Also the trigonometric functions are implementable with a Cordic algorithm [15]. This solution unfortunately required a sophisticated control and synchronization units that increases the complexity of the complete VHDL code.
To simplify the program developing we have been chosen to use a high level language programming, as is the C-code, for an ASIC programmable processor to compute the Eq. (2.7). A Nios Core II processor has been implemented inside the Cyclone II FPGA as SoPC (System on Programmable Chip) [16]. The Nios II processor family is a user-configurable embedded general-purpose 32-bit RISC soft-core processor set. This embedded soft-core processor includes three version: fast, standard and economy, where the differences are the computational power and the logic elements occupied. In this project the Nios Core II/F (fast version) was implemented. This processor is handling capacity of more than 200 MIPS and need to occupy about 1,800 logic cells. This processor allows to use easily the 35 embedded multipliers and 4 PLL internal in the Cyclone II with a C program.
The *acd_ control* module has been used also in this version to provide the deserialized data from the ADC's to the Nios Core. The processor calculates the angle of incidence using the Eq. (2.7) and send the results through the serial port to a computer.
The conceptual interconnections of the modules implemented in the FPGA are shown in Fig. 4.11.
The SoPC and the interconnections between the VHDL modules have been de-

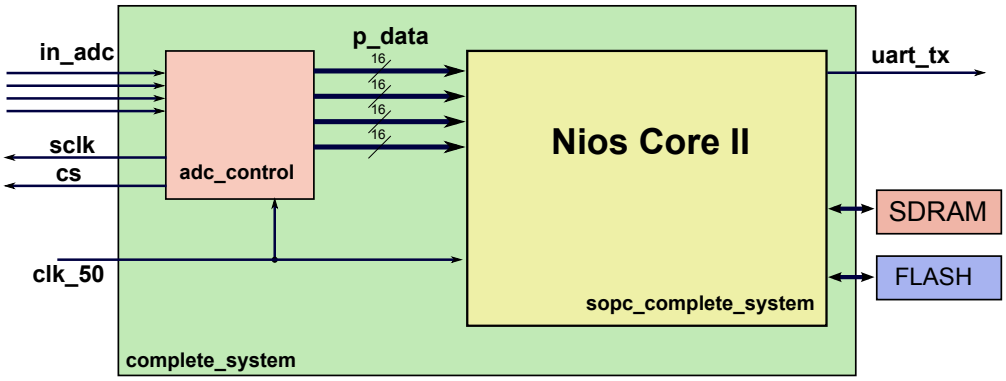

Figure 4.11: Module interconnection in Acquisition Theta version.

veloped in Quartus II, instead the C code for the Nios II have been developed in Nios II EDS.

The Nios Core II has a clock frequency of 140 MHz (generated with a PLL from 50 MHz), is connected to the ram chip (available on the DE2 board) clocked at 100 MHz and a dedicated core in the SOPC, for calculation with floating point, have been included. In this version, the VHDL compiled code and the SoPC configuration has been still saved in the EPCS16 instead the C compiled code has been stored in the flash memory. The Nios Core II has been configured to boot up reading from the flash memory.
The compilation results of the VHDL code in Quartus were:

```
Analysis & Synthesis Status : Successful
[...]
Top-level Entity Name : complete_system
Total logic elements : 15,450 / 33,216 ( 47 % )
Total combinational functions : 12,918 / 33,216 ( 39 % )
Dedicated logic registers : 9,011 / 33,216 ( 27 % )
Total registers : 9128
Total pins : 267 / 475 ( 56 % )
Embedded Multiplier 9-bit elements : 11 / 70 ( 16 % )
Total PLLs : 1 / 4 ( 25 % )
```

From the compilation result it is possible to see that there are available enough LEs to use the Cyclone II FPGA for the Dual Six-Port Based DOA Detector which needs two Nios Core II working in parallel.

Acquisition prototypes communication test

The acquisition system needed a functionality and communication tests, in which the hardware (the A/D module) and the software produced with some demo-signals are tested for the response. The A/D module produced has been connected to the DE2 board through the 40-pin connector number 0 with no signals in the board inputs.
The Acquisition P software has been loaded into the DSP module, then static voltages have been fed to the MCX A/D module; the acquired data were transferred and stored in the computer.
The ramp has been obtained with an Agilent E3646A Dual Output Power Supply. Via GPIB with an Agilent E5810A LAN/GPIB Gateway the E3646A has been controlled. The computer has been linked with the serial port to the DE2 board and then the Matlab script *ADC_ Test_ sweep_ 04.m* has been executed. The Matlab script controlled the power generator through the Agilent Gateway and the voltage measured via the serial connection.
For increasing values of the applied voltages, it is expected a linearity in the system response.
The results of this measurement is presented in Fig. 4.13. For channels 1-3 the acquisition is linear, whereas the channel 4 has some transmission errors.
This problem was caused for a wrong synchronization between the ADC 4 and

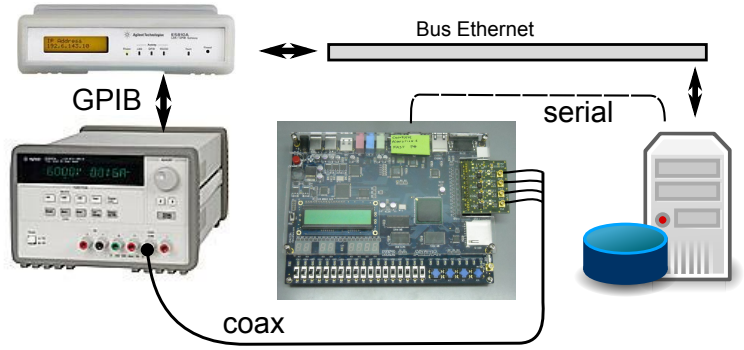

Figure 4.12: Setup for the sweep test.

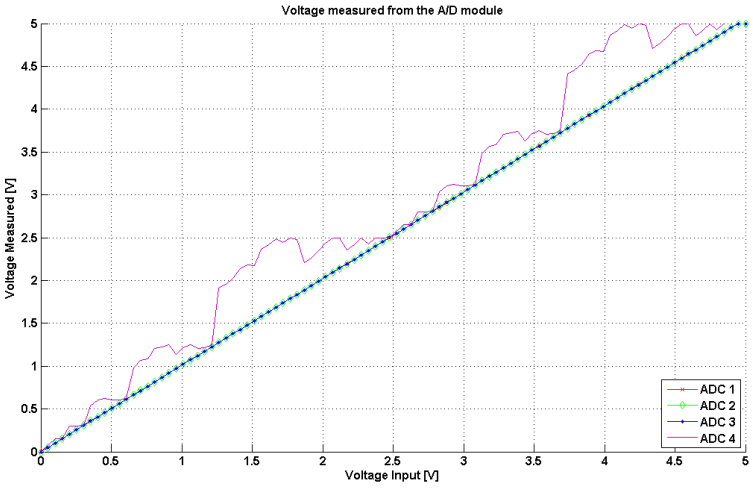

Figure 4.13: A/D module linearity measurement, SCLK @ 12.5 MHz.

the *acd_ control* module inside the FPGA. In fact, the Daisy-Chain topology of the clock path does not allow to send the clock signals with the same delay to all the four ADCs. The measurement in particular shows one bit loss in the transmission. Both, a high speed buffer or a tree topology, applied to the SCLK and the CS lines, can solve this synchronization problem.
A correct linear response of the system also for channel 4 has been obtained with a slower SCLK clock, from the original 12.5 MHz to 5 MHz, as shown in the Fig. 4.14. To reduce the clocks SCLK and CS, the *acd_ control* module has been modified using in the counter (SCLK_GEN) set to the configuration to (10,5) instead of (4,2).
A reduction of the clock frequency does not deteriorate the performances because the bottleneck of the process is the serial communication between the DE2 and the computer. The SCLK clock reduction make the ADCs sampling rate fall

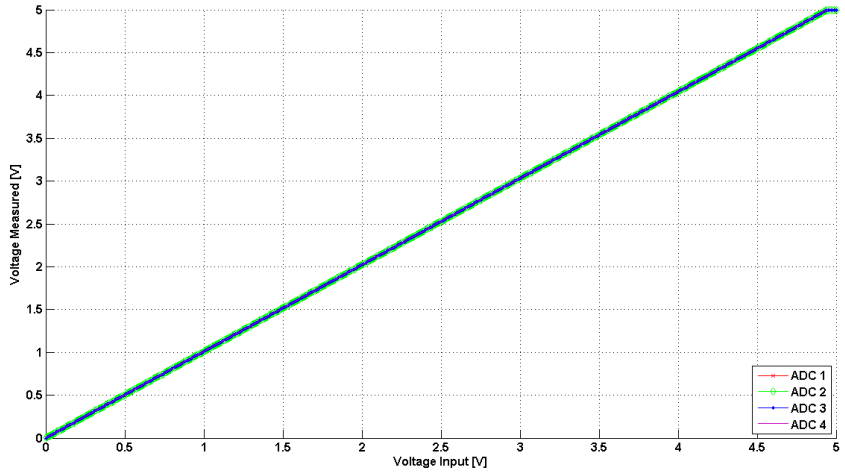

Figure 4.14: A/D module linearity measurement, SCLK @ 5 MHz.

down from 200 ksps to about 80 ksps (-60%).
The transmission throughput obtained has been 503 sps (one sample data contains four words: [P1, P2, P3 and P4]), very distant from the prototype's design (50 ksps). This value is -65% less than the serial port trasmission capability. Half speed reduction is caused from the receiving algorithm. A stream reading can improve the throughput over the packet reading. In fact, the current version reads 160 bits (20 pck) from the serial port and then extracts 56 sample bits (8 pck, the P1, P2, P3 and P4 words).
The last 15% is caused to the particular Matlab version running under Windows 7, with limitated support for the serial port. An ad-hoc Matlab driver would be able to increase the serial port throughput.

Sine waves with frequency up to 250 Hz have been used to test the A/D module and the Acquisition P software in the frequency domain.
Different sine waves, with 4.50 V amplitude and 2.25 offset, have been fed to

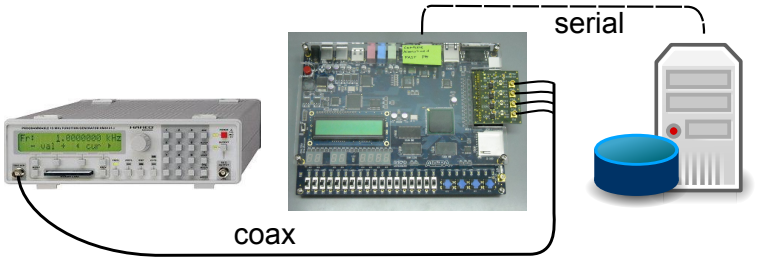

Figure 4.15: Setup for the frequency test.

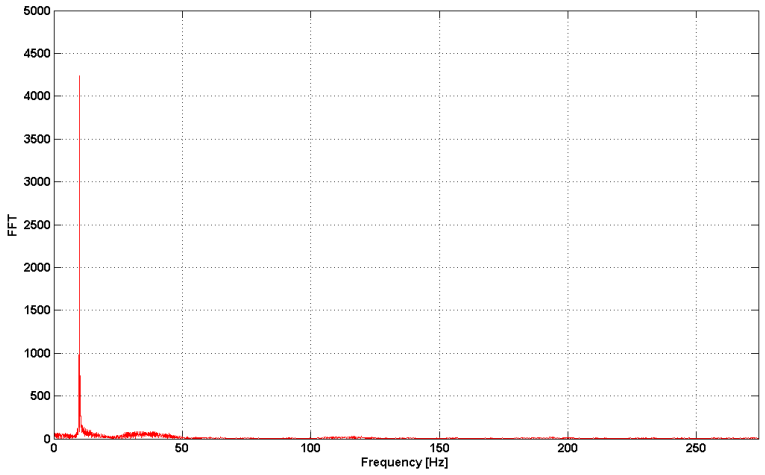

Figure 4.16: FFT of a 10 Hz sine wave acquired with the A/D module.

the A/D module inputs, produced with a Hameg HM8131-2. 8192 sample per channel have been collected from the computer, and then calculated the FFT function. Result of the FFT with a 10 Hz sine wave is shown in Fig. 4.16.
From the measurement it has been possible to see that the acquisition in the time domain has a low jitter because the FFT transforms presents negligible contributions other than the pure sine spectrum. The acquisition keeps a good definition, with sine waves up to 200 Hz. This frequency it is possible to define the maximum analog bandwidth measurable.
From this frequency value, the A/D module designed works with below the design specifications.

Having tested the system for the linearity response, it is possible then to test the Acquisition Theta version which performs the computation for the DOA detection.
The response of the RF module to an EMC wave arriving with α angle has been simulated with a set of four E3646A power generators. The four signals have been acquired with the A-D module having the Acquisition Theta software running in the DE2 board. The Altera board provided the θ angle measured directly to the computer; the values have been compared with the α angle simulated. The system provided a correct detection for 20 different α angles over 20 trials with a tolerance of 0.0027 DEG. The throughput measurement of the DOA angle has been of 500 sps.
These measurements verified the correct function of the Acquisition Theta software.

A carefully analysis of the computing process show that such a low throughput value is obtained because of the serial connection.
The clock ticks necessary to compute the single operations have been evaluated by using breakpoints and timestamps. To compute Eq. (2.7) by using the approach in Fig. 2.3 the processor uses:

- 6000 ticks for the subtraction $p1p2 = (P1 - P2)$ and $p3p4 = (P3 - P4)$;
- 260 ticks for the division $division = p1p2/p3p4$;
- 140,000 ticks for the atan function;
- 500 ticks for the multiplication with const;
- 120,000 ticks for the asin function.

The Nios Core II processor has 140,000,000 ticks per second.
Without the transmission of the θ angle from the tick required for the operations, the Nios II can calculate 500 Ksps. Due the serial connection and the Matlab acquisition script, the throughput of the computation is reduced to 500 sps (-99%).

From the measurements, it has been possible to determine that for the Dual DOA measurement a Cyclone 2 FPGA can be used to acquire the sample from the ADCs and to calculate two angles in parallel. In fact, it has enough LEs and calculation power to guarantee a good throughput. The interconnection between the DE2 board is the bottleneck of the system. It can be solved writing a Nios SOPC driver for the Ethernet interface. Anyway the DE2 board is too big to be used for the final hardware release. A less-feature board with a Cyclone 2 FPGA chip, ram, flash memory and Ethernet chip could be a good solution for the Dual DOA Measurement.

4.4 DOA measurements on the prototypes

The second test step has been the verification of the DOA measurements with two tests: a DOA detection test and a high accuracy DOA measurements. The first test has been performed to verify the theory of the DOA detection Six-Port based, instead the second to check the sensibility of the system. For these tests, a mechanical system has been required.
The setup consists of a dummy transmitter sending a continuous wave at 24 GHz, and a test receiver both built on high-precision mechanical translation and rotation stages. The distance between the two systems is fixed to 2.2 m. The receiver is based on a two-constraints system, that allows to rotate two receiving antennas about an axis perpendicular to the reference axis, and to adjust the distance between the receiving antennas. The dummy transmitter is also based on a two-constraints system. The first degree of freedom is the rotation of the

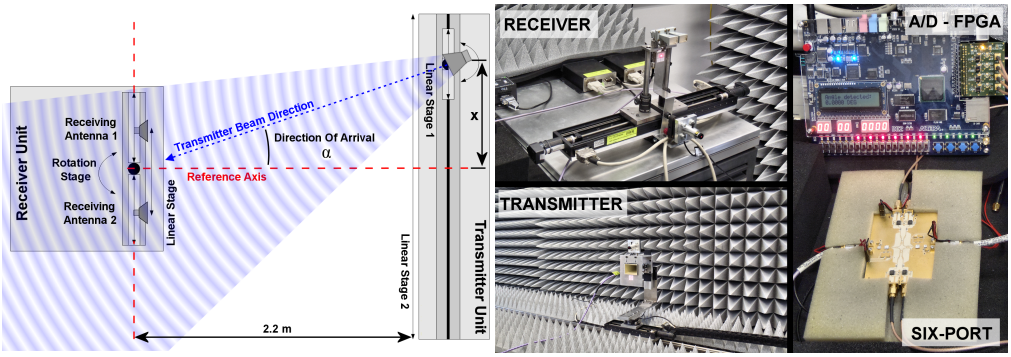

Figure 4.17: Overview of the prototype system for the DOA measurement.

transmitting antenna and the second constraint is the linear translation of the dummy transmitter with two linear stages: a large stage (Linear Stage 2) for long translations with moderate accuracy and a small stage (Linear Stage 1) for short but accurate translations.

The Direction Of Arrival angle α is described by:

$$\alpha = atan\left(\frac{x}{2200}\right) \ , \tag{4.1}$$

where x is the distance in [mm] of the transmitting antenna from the reference axis introduced by the linear stages.
The transmit antenna has been connected to the Agilent E8267 set to MCW mode, 24 GHz, 0 dBm. The two RF module prototype inputs have been connected to the two receiving antennas and the four outputs to the A/D module. The A/D module has been then plugged into the GPIO header 0 of the Altera DE2 board. The linear stages and the angle detected logging have been controlled by a computer, running Matlab scripts.
The first acquisition to verify the DOA detection has been performed with the antennas at $d = 17$ cm and a transmitter translation of of $\Delta x = 640$ mm with the long linear stage (tolerance of ± 0.3 mm), equivalent to an angle sweep from 0 to 6 DEG. The measurements offset and compensation have not been considered. With the Altera DE2 running the acquisition_p program has been possible to acquire the single P voltages and to calculate the angle detected in the computer. The acquisition is presented in Fig. 4.18. The theory anticipated in Chapter (3) for a single Six-Port has been obtained, in particular, it is possible to note the different amplitudes of the four Six-Port channels and the ambiguities in the calculation of the angle of incidence are evident and delimit the detection range. With this test, the connections between the A/D module, the DSP module with the software have been verified.
By increasing the antenna distance to $d = 20$ cm and introduced an measurement offset has been possible to obtain a more comparable measure. In this case

the acquisition_theta program has been used. In Fig. 4.19 the measured angle of incidence is compared to the incident angle within a narrow detection range. A good linearity can be noticed when comparing the curve to an ideal linear function. This measure shows that the software inside the DSP module which calculates the Eq. (2.7) works correctly.
An accurate measure of the DOA detection has been performed with the setup in high accuracy, by using the antennas at $d = 30$ cm (the maximum possible with the receiver linear stage) and by using the short linear stage of the transmitter (which has tolerance of ± 5 μm).
In Fig. 4.20 is presented the DOA detection with a translation of the transmitter of $\Delta x = 55$ mm equivalent to a set an angle within 0.025 DEG. The linear stage has been moved with 10 steps equivalent to 0.0027 DEG.
The plot presented are based on raw acquisition data without compensation. The excellent linearity of the results demonstrate the high accuracy of the acquisition system.
This measurement has been reached the higher resolution capable for the detection system due the 16 bit angle resolution variables used. Probably by increasing this value it is possible to reach a more accurate measurement.
The correct work of the A/D, the DSP modules and of the software prototypes have been verified.

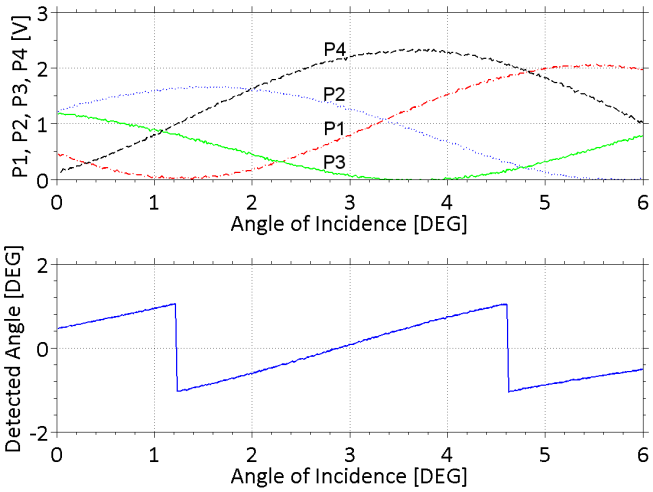

Figure 4.18: P voltages measurement and detected angle vs incident angle with $d = 17$cm.

4.5 Feedback module prototype developing

Also for the Feedback module a prototype has been produced. The Feedback module consist in two system: the first it is used to adjust the gain of the baseband amplifier with a variable resistor, and the second it is used to manage the variable attenuator with a DAC system. Both system are used to manage the components in the RF module.
Small component with SPI interface and capable to work with a shared clock line have been chosen to use for this module. These components allow to reduce the complexity of the final version of the Dual DOA acquisition system. Moreover, it has been used a low clock to avoid a-priori synchronizations problems (like in the A/D module).
The Microchip MCP42100 have been chosen to be used for the variable resistances. This component is a two independent channels 8 bit digital potentiometers. The two adjustable resistances have 256 positions available, between 0 to 100 kΩ. This component accept a maximum clock frequency of 10 MHz. For each Six-Port, the module needs two of this components. The MCP42100 components control a gain factor between 0.3 to 100 of the baseband amplifiers.
Two analog voltages input in the RF PCB module control the two stage attenuators features by Hittite variable attenuator (HMC812lC4). It has been possible to adjust linearly the attenuation between 0 and 30 dB of the HMC812lC4 with a voltage moved linearly between -3 V to 0 V in the two voltage inputs. To obtain two independent voltages between 0 and -3 V a Texas Instrument LTV5626 connected to an operational amplifier, with inverting configuration, has been used.

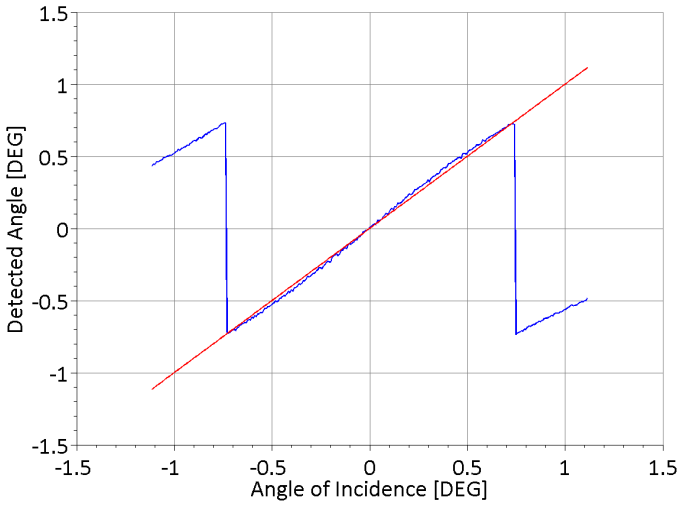

Figure 4.19: Measured vs incident angle from -1.5 to 1.5 DEG, receiving antennas at $d = 20$cm.

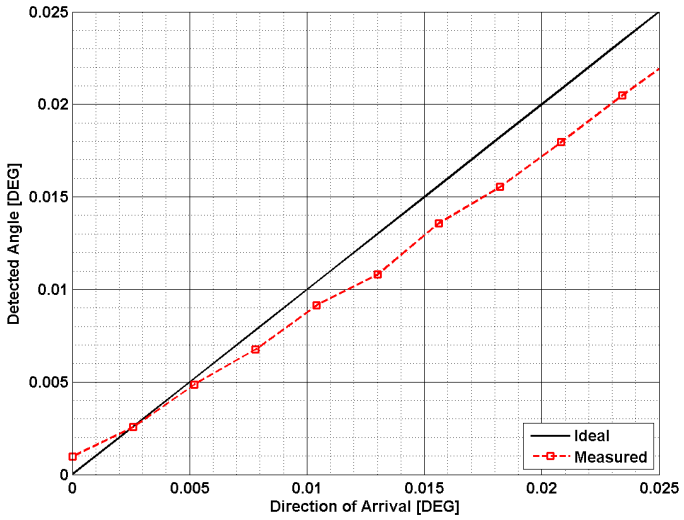

Figure 4.20: DOA detection in high accuracy mode, incident angle from 0 to 0.025 DEG, receiving antennas at $d = 30$cm.

The LTV5626 is a dual channel, 8 bit DAC with SPI interface. The DAC outputs provide a positive voltage between 0 to 5 V and with the inverting configuration of the op-amp, with gain 3:5, it was possible to have the correct voltage. The DAC works with a maximum clock frequency of 20 MHz.
To provide the negative voltage, a stable negative power supply has been necessary to be implemented. Two power supply modules on board have been inserted to produce a -5 V and a +5 V stable lines. A Maxim MAX889 for the negative voltage (-5 V) have been used. The MAX889 is an inverting charge pump that delivers a regulated negative output voltage at loads of up to 200 mA.
A National Semiconductor LP3878-ADJ has been used to stabilize the positive voltage. This component is an 800 mA adjustable output voltage regulator, designed to provide high performance and low noise. It produces, with a resistance configuration, a stable voltage between 1 and 5.5 V.
A demonstration board has been developed and produced with these two system and a power supply implemented. The power supply modules have been used to power the components on board.
The scheme of the two systems are presented in Fig. 4.21.
The digital lines of the components have been connected to the 40-pin GPIO of the Altera DE2 board with wires. With two VHDL programs (*MCP42100_control* and *TLV5626_control*) programmed inside the Cyclone II have been possible to control these components. For the serial communications (SCLK) a 1 MHz clock has been used.
Both systems and the power supply have been tested with positive result.

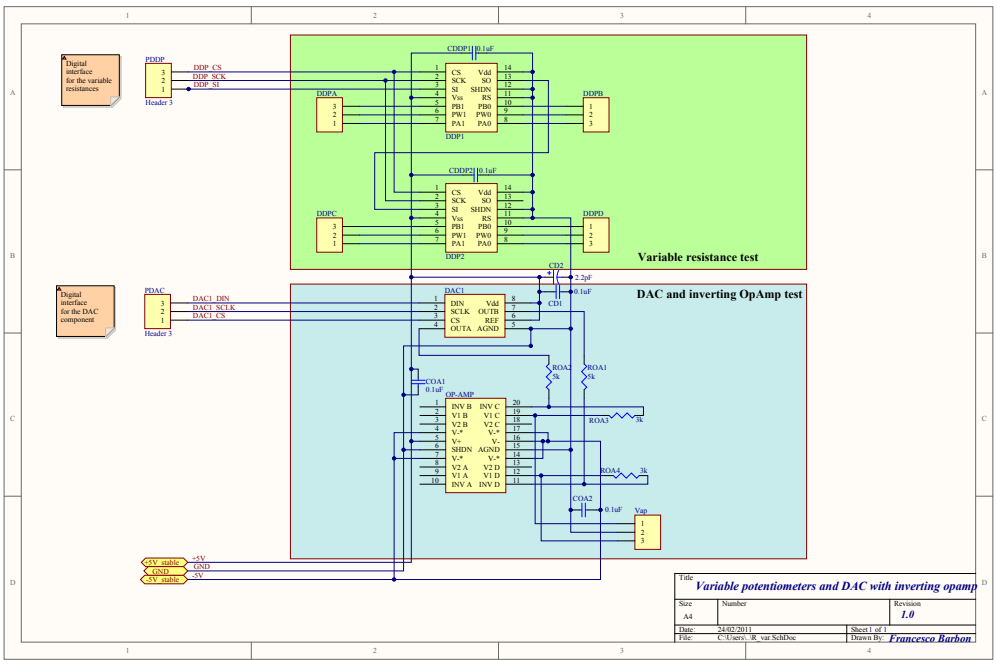

Figure 4.21: Scheme of the Feedback module prototype.

4.6 Final version developing

All the modules developed before into a single board have been included in the final release for the Dual DOA board. A 5 layers stack PCB board with SMD components have been chosen to be developed in order to overcome the complexity of the system and to separate the high/low frequency networks.
The layer stack is represented in Fig. 4.22 where the first layer L1 is the RF

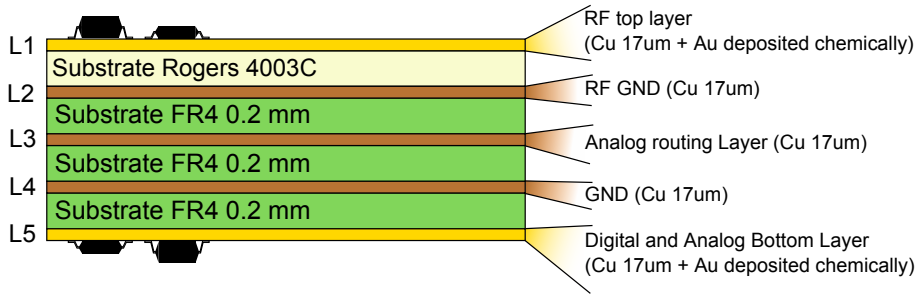

Figure 4.22: Diagram of the 5 layer substrates in the Final version.

Top Layer which integrates the RF module. Below this layer there is the ground reference (RF GND) layer L2 for the RF top layer. Then, layer L3 contains the analog lines routing networks. Layer L3 is separated from L5 by a common analog and digital ground plane (GND) layer L4. Finally the Bottom Layer L5 contains the digital and analog lines routing networks. Moreover, the Bottom Layer contains the digital and analog components of the A/D, and the Feedback modules.
Physical separation of the layers are realized by using different dielectrics: the Top Layer (L1) and the first ground plane (L2) are separated by a Rogers 4003C substrate 0.2 mm thin, whereas the other three layers are separated by a FR4 0.2 mm substrate.
The Rogers substrate has been placed below the layer L1 for the RF networks and components because the parasitics of the FR4 material are too high to ensure a good signal transmission at higher frequencies. Therefore a special hydrocarbon ceramic substrate (Rogers 4003C) has been used. Although, it is possible to use this ceramic component also for all the other substrates, due the high production costs and the fragility of the resulting board, FR4 material is more suitable.

The design started from the development of the first two layers L1 and L2, by taking into account the fact that below analog and digital layers required constrained geometries.
This version has been designed with two independent RF modules working in parallel in the layer L1. The RF module v.2 layout has been tested in CST Microwave Studio 2011. The L1 rendering is shown in Fig. 4.23.
The two layers designed occupied an area 80 mm wide and 70 mm height.

In order to reduce the occupied area from the RF module, Six-Port network has

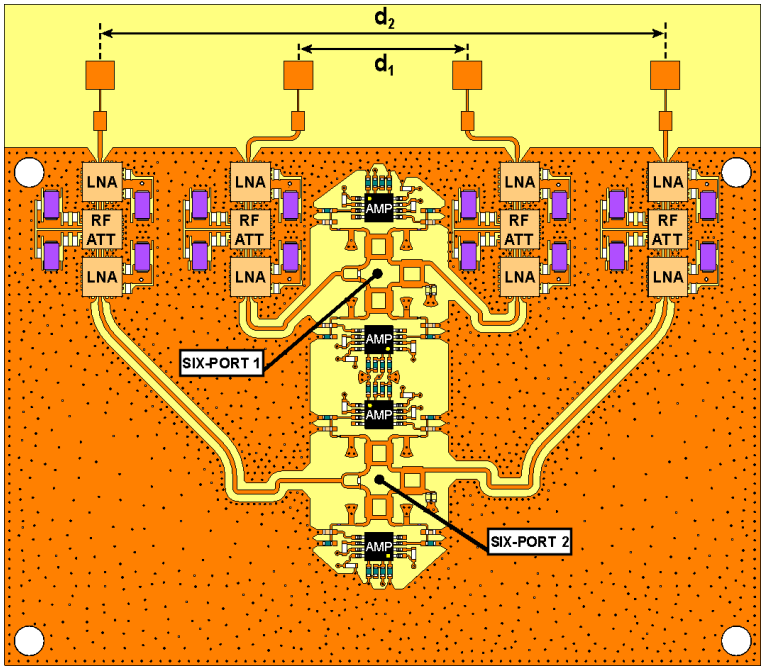

Figure 4.23: CST MWS rendering of the RF module v.2.

been compacted. The pass-band filters have been removed because unnecessary, and the front-end amplifier stages updated in a dual-stage amplifier to guarantee a better gain and to extend the working power range.
From Fig. 4.23, it is possible to identify the two new Six-Port networks in the middle with the two-stage amplifiers (LNA, RF ATT, LNA) for the input lines. The baseband amplifier (AMP) just after the RF power detector network are also marked.

In this new version the external antenna connectors have been replaced by four patch antennas. This modification is important because it reduces the costs of the board and also increases the mechanical stability. In fact, the board needs no more the antenna connectors (that means less holes in the PCB) and the external antennas. Moreover, the integration of the antennas allows to control the distance d_1 and d_2 between the antennas with a excellent precision (the production accuracy is about 25 μm).
The integrated patch antennas have been designed with a center frequency of 24 GHz and matched with the LNA input impedance (50 Ω).
The area below the patch antennas has been designed with flood of a big reference ground plane. The RF module v.2 has been developed to be coverable with a metallic shield to avoid parasitic coupling of external signals with the networks. With four holes in the PCB, the shield has been designed to be fixed.

The power lines and the voltages for the RF variable attenuators have been connected to the layer L3 through via. Also the analog signals, output of the two RF modules, have been provided to the layer L3 through via, and then routed to the acquisition module placed in the Bottom Layer L5.

A/D module design

The measurement of the detector (Fig. 4.3) shows that the acquisition system needs at least 10 bit to guarantee a correct sampling. The A/D module has been upgraded using a 12 bit ADC system to guarantee flexibility and future upgrade of the board. In particular it has been updated because this final version 8 acquisition channels are needed.
In order to limit the complexity of the system, the number of components have been reduced by using two chips with more input channels and with a fast refresh rate instead of eight TLC3541.
The commercially available ADC systems on chip (*DAS, data-acquisition system*) with fast sampling rate and 12 bit per sample have 8 or 16 analog input, unfortunately no-one guarantees the simultaneous sampling, in facts most of them have the input channels multiplexed into a single fast converter. Two Maxim MAX1305ECM (12 bit with four independent input channels) in parallel have been chosen to be used to sample the analog signals. With the respect to the 8 or 16 input channels, this chip has a track-and-hold (T/H) system that provides simultaneous sampling for each channel. A 20 MHz, 12-bit, bidirectional parallel data bus provides the conversion results with a throughput of 680 ksps and accepts digital inputs for the chip programming.
The standard datasheet scheme for the ADCs has been used and not reported.

A new filter network has been implemented to guarantee a correct sampling. It has been chosen to use a Butterworth Low-Pass Filter (LPF). This filter guarantee a flat frequency response in the passband.
The new filters have been designed to allow passing the maximum analog bandwidth available, cutting all the components above the Nyquist frequency (340 kHz).
An active 8th order LPF has been developed with a Linear LTC1562-2. This chip is a low noise, low distortion continuous time filter with rail-to-rail inputs and outputs, optimized for a center frequency of 20 kHz to 300 kHz. Four independent 2nd order filter blocks configurable with three resistor are available inside the chip. With the software Linear FilterCAD it has been possible to obtain the filter network design, the best resistance values for the circuit and the simulation of the filter response. A 8th order Butterworth LPF has been designed with a pass-band of 80 kHz and an attenuation of 91 dB at 300 kHz to allow the ADCs a correct sampling. The simulation responds of the filter and the best resistor configuration for the LTC1562-2 have been provided from

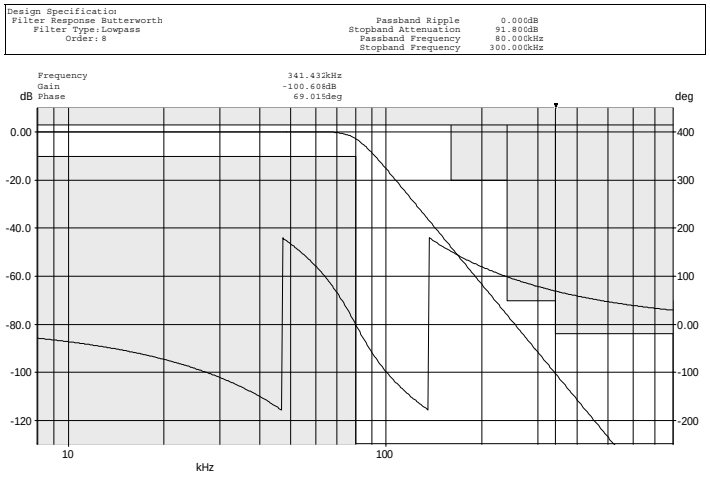

Figure 4.24: Bode diagram and phase graph of the 8th order Butterworth LPF.

FilterCAD (Fig. 4.25).
This configuration uses three filter blocks of one chip, it means that the new acquisition module needs eight chips in total.
In order to shrink the routing complexity the scheme of the filters have been modified in an Altium sheet; only two chip's filter blocks have been used for each channel, instead of four as shown in the Fig. 4.26. The 3th and 4th filter

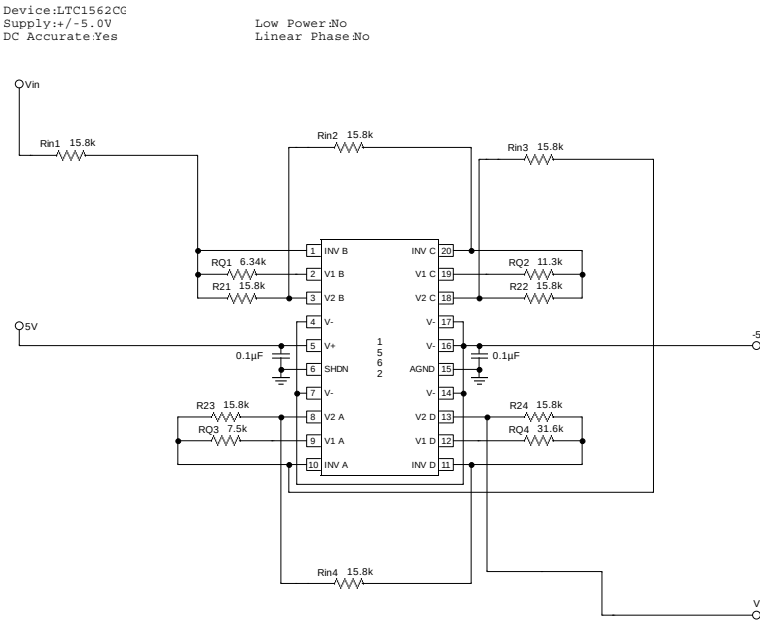

Figure 4.25: LPF circuit for the LTC1562-2 chip.

blocks, in fact, have been moved to a second chip. In this configuration two chips are used shared for filtering two channels. The total filter are based on four branches like those shown in Fig. 4.26.
This structure allows a symmetric structure with a site grouping the inputs and one site grouping the outputs. The new filter network allows more over to reduce the area occupied from the components.

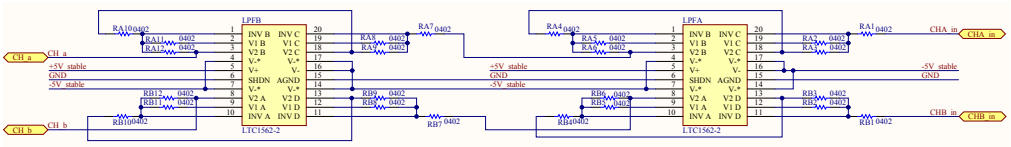

Figure 4.26: Scheme of the new 8th order filter for two channels.

Feedback module

The Feedback module has been designed cloning the Feedback prototype scheme. The Final version needs eight variable resistance. The variable resistance scheme, with the MCP42100 chips used to adjust the gain of the baseband amplifiers on the RF modules, was developed from the prototype scheme. The final design has been obtain using two times the old scheme and shrinking the redundancy lines. The result of these operations is presented in Fig. 4.27.
The four chips have a shared clocks RV_SCLK and RV_CS signals. Two serial lines are used to provide the controls of the variable resistors. These two lines produce two branches with two MCP42100 chips connected in Daisy-Chain.
A low number of lines to be routed for the controls have been obtained with this configuration. Otherwise, the chips, due the Daisy-Chain connection, needs to be configured two times to receive the complete configuration.

The Final version of the DAC block, inside the Feedback module, has been produced also starting from the prototype scheme.
Four independent channels (two four each Six-Port) were needed for the final release. Two TLV5626 DAC connected to a Linear LTC1562-2 chip (the same used for the filters) used as operational amplifier have been used to control the HMC812lC4's. In facts inside a filter block there is an operational amplifier in inverting configuration.
The scheme of the design is shown in Fig. 4.28.

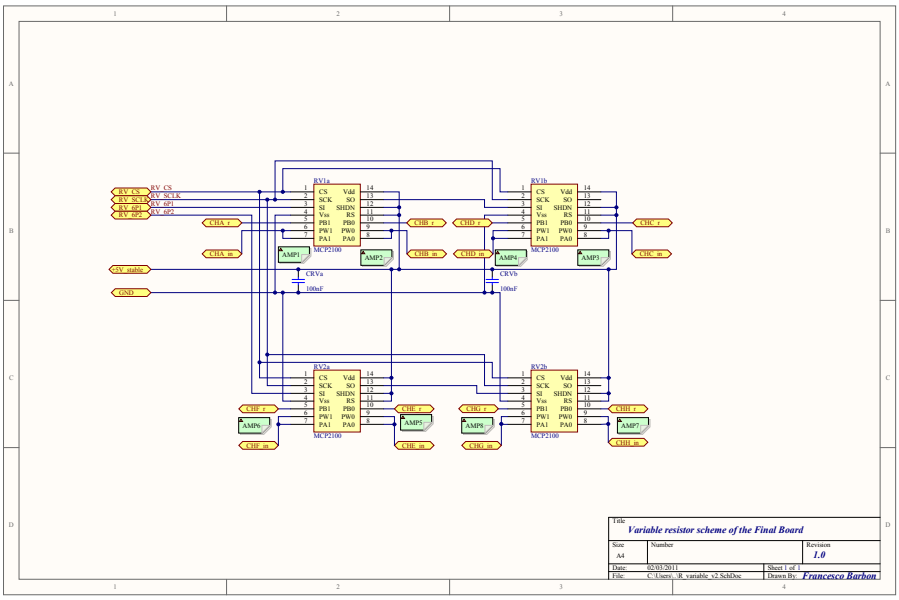

Figure 4.27: Scheme of the variable resistances block in the Feedback module of the Final version.

Board power supply development

The power supply system used in the Feedback Module prototype has been retained to feed power to all the components of the board. It required a single 6 V line from which it can produce all the voltages and power needed from the board's components. Different voltage lines have been generated with different components. The +5 V, +4 V and the +3 V lines are provided stable with a NS LP3878-ADJ chip from the +6 V input line. The -5 V line are produced with a Maxim MAX889 chip from the +5 V stable line. All the power lines were routed in the Analog routing layer.
The scheme of this system is presented in Fig. 4.29. The figure reports the components used and the connections of the power supply to the different components, together with the voltages.

It is to be noted that the -0.1 V line is produced in a very unconventional way by using an operational amplifier (MAX410).
With a resistance network, a positive voltage of 0.1 V has been applied to the negative input of the operational amplifier while the positive connector has been connected to ground as shown in Fig. 4.30. This forces the op-amp to produce a voltage of -0.1 V. This scheme is much simpler and cheap than using a conventional power stabilizer chip, but it can be used only to power low consumption loads.

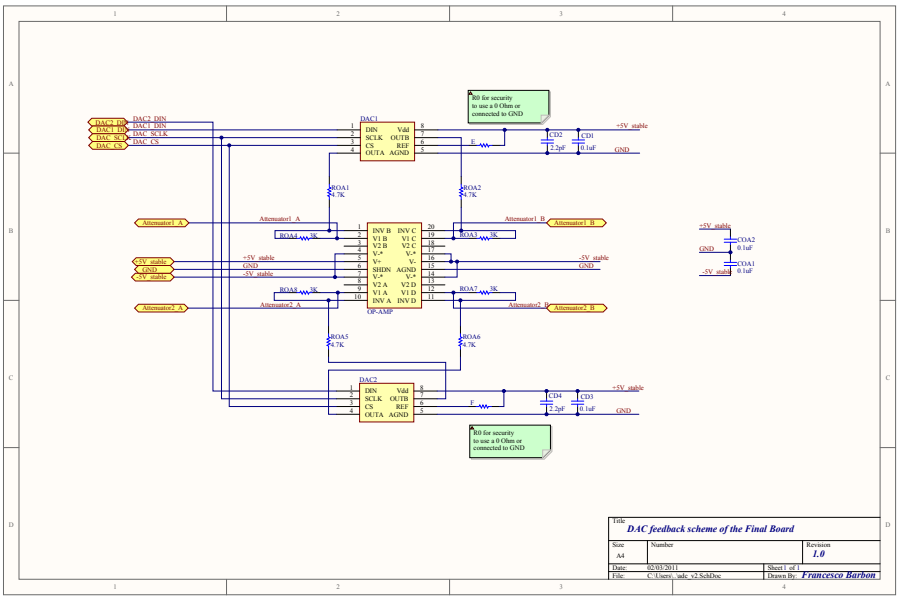

Figure 4.28: Scheme of the DAC block in the Feedback module of the Final version.

It is possible to use this configuration for the power supply of the baseband amplifier because the components have an evaluated absorption lower than 35 mA in total.

PCB design

To design the PCB layout of the last three layers (L3, L4 and L5), in an Altium PCB document a three layer PCB with the same size of the RF module in the layer L1 has been generated. Then, the scheme of the A/D, Feedback and Power Supply modules have been imported into this document. The placing and routing by hand of the components and of the networks, produced the Final version Board. The Altium rendering of the board is shown in Fig. 4.31.
The components have been located according to the position of the via presents in the layer L3. In fact, the interconnections of the layer L1 with the layer L3 are placed in a cross structure where in the vertical line the output signals of the baseband amplifiers are placed instead in the horizontal line the power lines for the LNAs and the voltages for the RF attenuators are located.
The presence of variable resistances, filters and ADCs forced the board design to be asymmetrical. Moreover, the central position of the signals coming from the RF module forced to route the analog signals to the variable resistors (R_V). This route of the baseband signals have been located in the layer L3 together

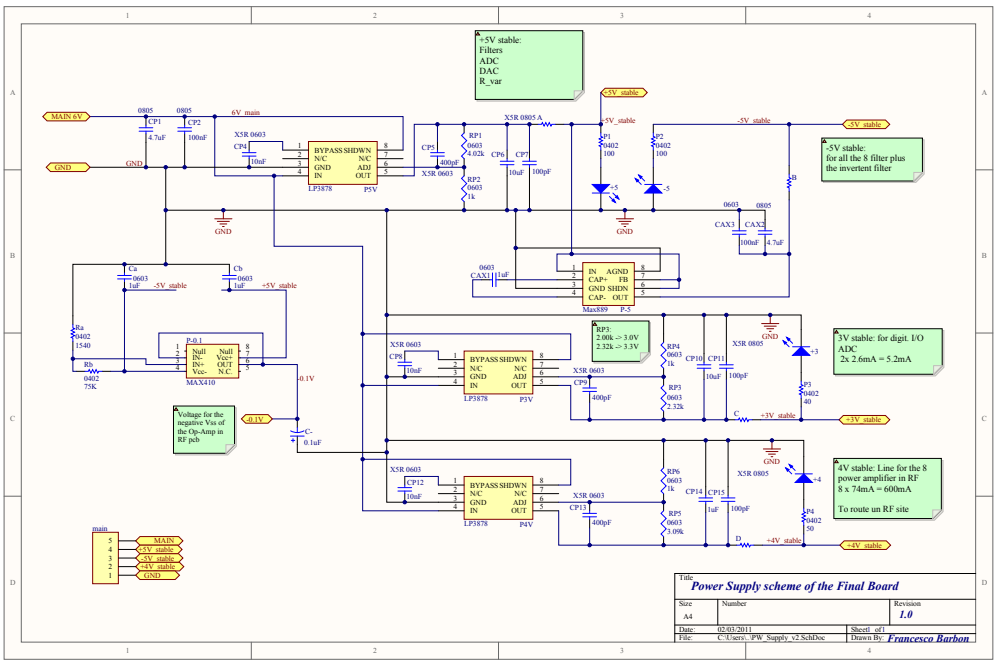

Figure 4.29: The power supply module of the Final Version.

with both the routing of the outputs of the DAC block (to the variable resistors) or the +4 V output of the power supply module (to the power input of the LNAs in the RF module).
The design rules were the routing of the analog lines with priority in the layer L3 and of the the digital lines in the layer L5.
Two 80-pin headers J0 and J1 have been included in the PCB to connect the board with an external DSP module. In the J0 connector all the pins of the two ADCs (ADC1 and ADC2) have been connected, instead in the connector J1 the power supply and the controls for the Feedback modules have been connected. A

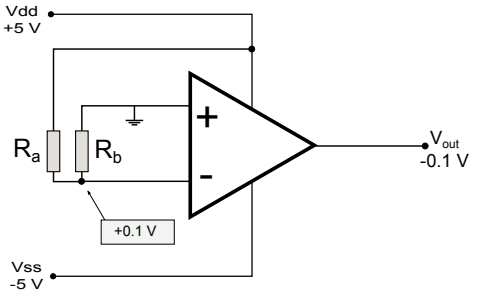

Figure 4.30: The generation of the -0.1 V line with an operational amplifier.

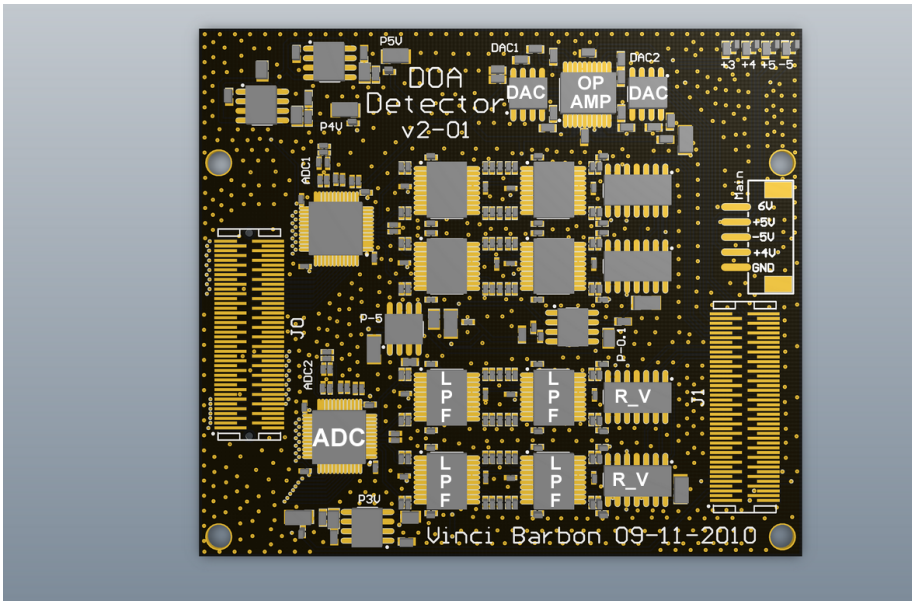

Figure 4.31: Altium rendering of the Final version board.

4-pin connector, Main, has been inserted to bypass the power supply. Through this connector with an external multiple voltage power supply it is possible to power all the components on board.

A cheap test board with some modules of the Final version design have been designed to test networks and some components in the L3, L4 and L5 layers.
As shown in Fig. 4.32, in the board the RF module has been removed to keep the board a three layer PCB in FR4 substrate. Also the power supply for the +4 V stable and the DAC blocks have been removed.
The board presents sixteen MCX connectors footprints that allow to test the filtering stages and to inject signals to the ADC's input pins.
With a 40-pin header (J12) an external DSP module can controls the ADC's, instead with two separate 4-pin connectors J14 and J15 it is possible to set-up the two variable resistors branch.

No-one of these two boards have been able to be tested because still in productions.

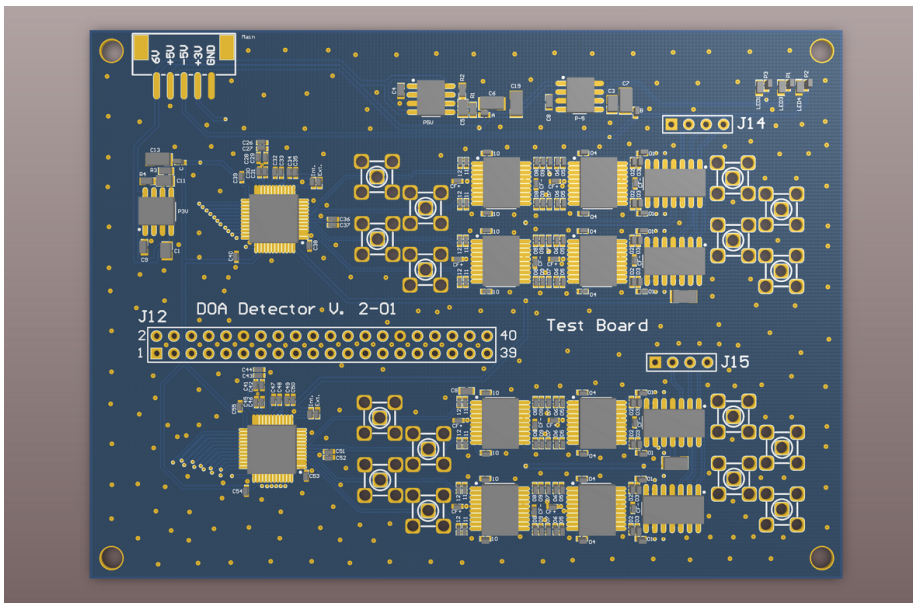

Figure 4.32: Altium rendering of the test board for the A/D, filters and feedback modules insert in the Final version board.

Conclusions

This thesis is part of the project aimed to the development of a board for the DOA detection based on the a phase measurements concept, which is a new approach with in respect to the conventional DOA detection based on the TDOA measurements. To perform the phase measurements, a Six-Port interferometer pair has been used. The architecture developed allows to create a robust and low-cost board able to measure the DOA angle at 24 GHz with high accuracy and in a wide-angle.
The board developed resulted to be a 5 layers PCB 80mm wide and 70 mm height, where in the Top Layer the radio-frequency components, and in the Bottom Layer all the digital and low frequency components have been placed. In the Top Layer, in fact, there are the four antennas, the two Six-Ports, the eight RF detectors and baseband amplifiers. In the Bottom Layer, instead, are present the eight filters, the two ADCs and the Feedback system to control the Top Layer's components.
This board has two header for the power supply and for the interconnections to an external digital signal processing module. This board anyway is in production by manufactures.

The development of the PCB has been based on measurements and tests realized on prototypes for the digital conversion and the auxiliary blocks. The prototypes have been assembled to create a full working DOA detector based on a single Six-Port, and then it has been performed DOA measurements. To control the acquisition and to calculate the DOA angle, an Altera DE2 FPGA board has been used as DSP module, with a soft-processor Nios Core II implemented. The assembled prototype has been able to transmit 500 sps with a maximum resolution of 0.0027 DEG in a detecting range of ± 3 DEG. The measurements performed allowed moreover to verify the mathematical model for the system response in a range of ± 90 DEG.
A software prototype has been created to test the hardware performances of an acquisition system prototype with a single Six-Port.
A program study has been made to detect the best architecture and source code for a fast development. An ASIC programmable processor programmed in C-code resulted to be the best choice.
Future prospectives:
A planned hardware upgrade comprises a stacked system on the back of the existing board that delivers the digital signal processing, at the moment done by the external FPGA. The new DSP unit will be based on a fast System on Chip (SOC) ARM Cortex-A9 Dual-Core Processor to improve the refresh of the detected angle. To improve the data transmission Ethernet, ad-hoc 802.11n (MIMO) or Thunderbolt links have to be considered.

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