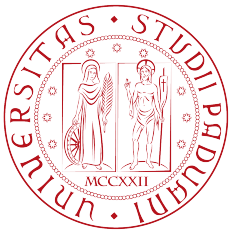

Università degli studi di Padova
Tesi di laurea specialistica in
ingegneria elettronica

MODELLING OF A P-MOS LOW DROP-OUT VOLTAGE REGULATOR WITH FAST TRANSIENT RESPONSE AND ITS FEASIBILITY IN LOW COST TECHNOLOGY

by
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To my family for their encouragement, love and support.

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Sommario

I regolatori di tensione lineari sono dei componenti molto utili in campo elettronico. Questi componenti garantiscono una tensione costante in uscita a fronte di una tensione variabile in ingresso. Gli alimentatori di ultima generazione, sfruttano la serie di un convertitore tipo switching e di un regolatore lineare. Nelle applicazioni che funzionano tramite batterie, il regolatore lineare è assi diffuso. Per esempio, in campo automobilistico, i regolatori lineari sono ampiamente utilizzati in quanto ad ogni sistema elettrico è garantito una tensione costante.

In questa tesi si è analizzato nel dettaglio i principali tipi di regolatori lineari, focalizzandosi su quelli a basse cadute "low drop-out". Ci si è inoltre focalizzati su una tecnica di compensazione multi retroazione. Per far questo si è realizzato una interfaccia grafica tramite Matlab chiamata `LDO behavior`, che riuscisse a spiegare, almeno in prima approssimazione, l'effetto dei feedback sul sistema totale. La fase di progettazione è stata realizzata sfruttando le informazioni fornite da questa interfaccia grafica. Infine si è realizzato un test-chip che è stato caratterizzato in laboratorio.

Acknowledgements

I would like to thank my supervisor Marco Piselli, for his many suggestions and constant support during this research. I am also thankful to Simone Massaro and Massimo Rossetto for their guidance.

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Padova, Giovanni Bisson

July 6, 2010.

Introduction

This thesis work, which was developed in collaboration with Infineon Technologies s.r.l., focuses on the realization of a voltage regulator with current efficiency, low voltage and low drop-out. These characteristics are driven by portable and battery operated products requiring compactness and low power. In particular, the increasing demand for portable battery operated products has driven power supply design towards low voltage and low quiescent current, for example in cellular phones, camera recorders, laptops, etc.

On the other hand, nearly all electronic circuits, from simple transistor and operational amplifier circuits to elaborate digital and microprocessor systems, require one or more sources of stable dc voltage. Regulators are an essential part of any electrically powered system, which also includes the growing family of portable battery-operated products. Regulators are also required to reduce the large voltage variation of battery cells to lower and more acceptable levels. The absence of these power supplies can be catastrophic in many high frequency and high performance circuit designs. As a result, low drop-out regulators and other power supply circuits are always on great demand. Indeed, the increasing drive towards total chip integration (single chip solution or full on chip) requires power supply circuits to be included in every chip. This is a consequence of the public need for smaller and less expansive portable products.

The current trend goes towards reducing the number of battery cells, in order to decrease cost and size, while minimizing quiescent current to increase battery life. Current efficiency is particularly important, because at low load current conditions, the life of the battery is adversely affected by low current efficiency, i.e., high quiescent current flow. On the other hands, at high load currents, current efficiency is typically high because the load current is significantly larger than the quiescent one. In this low voltage regime, a low drop-out

voltage regulator is the most appropriate form of linear regulator.

This research work develops techniques that enable circuit realizations of low drop-out voltage regulators at low input voltages and low quiescent current flow without sacrificing performance. As a result of high battery voltage variation, these regulators are required by almost all battery operated applications. Furthermore, most of all designs require to include such voltage regulators and other power supply circuits directly on chip to maximize the portability and minimize the costs. Low drop-out voltage regulators are appropriate for many circuit applications, namely, automotive, portable, industrial, and medical applications. In the automotive industry, the low drop-out voltage is necessary during cold crank conditions, where the battery voltage can drop below $6[V]$. The increasing demand, however, is more clear in mobile battery operated products. The portable electronics market requires low voltage and low quiescent current flow to increase the battery efficiency and longevity. As a result, high current efficiency is necessary to maximize battery life. Low voltage operation is also consequence of the trend of the technology process towards higher packing densities. In particular, isolation barriers decrease as the component densities per unit area are increased thereby manifesting lower breakdown voltages. Minimization of drop-out voltages in low voltage environment is also necessary to maximize the dynamic range while the noise remains typically constant. Consequently, low power and finer lithography drive regulators to operate at lower voltages, produce precise output voltages and require low quiescent current flow.

The Italian offices of Infineon Technologies s.r.l., located in Padova, are involved in the automotive sector. Historically, this industrial branch was born as a craftsmanship activity linked to the vehicle diffusion. Now this industry improves the concept of vehicle and the automotive industry provides technical and stylistic input that contributes to define the final product. Automotive design is a specialized category in industrial design which includes many disciplines such us ergonomics, mechanics, electronics and aerodynamics.

In this work we are interested on the electronic aspect of the automotive sector. In fact, automotive instrumentation includes the equipment and devices that measure engine and other vehicle variables and display their status to the driver. From about the late 1920s until the late 1950s, the standard automotive instrumentation included the speedometer, oil pressure gauge, coolant temperature gauge, battery charging rate gauge and fuel quantity.

Strictly speaking, only the latter two are electrical instruments. Indeed, this electrical instrumentation was generally regarded as a minor part of the automotive electrical system. By the late 1950s, however, the gauges for oil pressure, coolant temperature and battery charging rate were replaced by warning lights that were turned on only if specified limits were exceeded. This was done primarily to reduce vehicle cost and because of the presumption that many people did not regularly monitor these instruments.

Automotive instrumentation was not really electronic until the 1970s. At that time, the availability of relatively low cost solid state electronics brought a major change in automotive instrumentation; the use of low cost electronics has increased with time. In addition to providing measurements for display, modern automotive instrumentation performs limited diagnosis of problems with various subsystems. Whenever a problem is detected, a warning indicator alerts the driver and indicates the appropriate subsystem.

Electronics have recently been incorporated on new automotive subsystems and have become the standard implementation on many others. Features such as anti-lock braking system, ABS and air bags could only be introduced through the use of electronics. These features are rapidly becoming a standard, thanks to strong pressure due to the high market competition.

Chapter 1

Linear voltage regulators

This chapter will allow to understand the operation of linear voltage regulators. The most commonly used regulators are the Standard, Low Drop-out, and Quasi Low Drop-out regulators.

The linear regulator is the basic building block of nearly every power supply used in electronics. The IC linear regulator is so easy to use that it is virtually foolproof, and so inexpensive that it is usually one of the cheapest components in an electronic assembly [6].

Every electronic circuit is designed to operate off of some supply voltage, which is usually assumed to be constant. A voltage regulator provides this constant DC output voltage and contains circuitry that continuously holds the output voltage at the design value regardless of changes in load current or input voltage (this assumes that the load current and input voltage are within the specified operating range for the regulator).

A linear regulator operates by using a voltage-controlled current source to force a fixed voltage to appear at the regulator output terminal as shown in figure 1.1.

The control circuitry must monitor the output voltage, and adjust the current source, as required by the load, to hold the output voltage at the desired value. The design limit of the current source defines the maximum load current the regulator can provide while maintaining regulation.

The output voltage is controlled using a feedback loop, which requires some type of compensation to assure loop stability. Most linear regulators have built-in compensation, and are completely stable without any external components. Some regulators, like Low

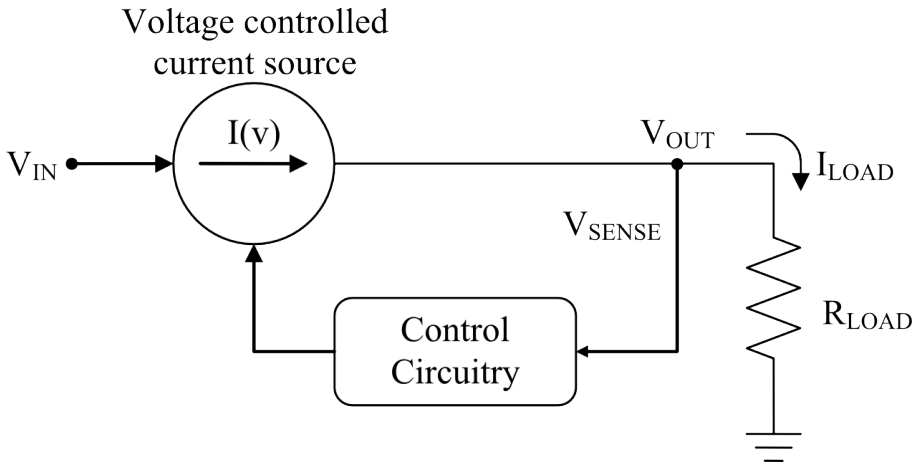


Figure 1.1: Linear regulator functional diagram.

Drop-out ones, may require some external capacitor connected from the output lead to the ground to assure regulator stability.

Another characteristic of any linear regulator is that it requires a finite amount of time to correct the output voltage after a change in the load current demand. This time lag defines the characteristic called **transient response**, which is a measure of how fast the regulator returns to steady-state condition after a load change.

1.1 Conventional linear regulator

In figure 1.2 is illustrated the block diagram of a generic series regulator. The circuit consists of:

- an error amplifier,
- a pass device,
- a feedback network

that are the principal blocks, then it is common to find:

- an internal supply,
- the voltage reference and his start-up circuit (if necessary),

- some protection circuits.

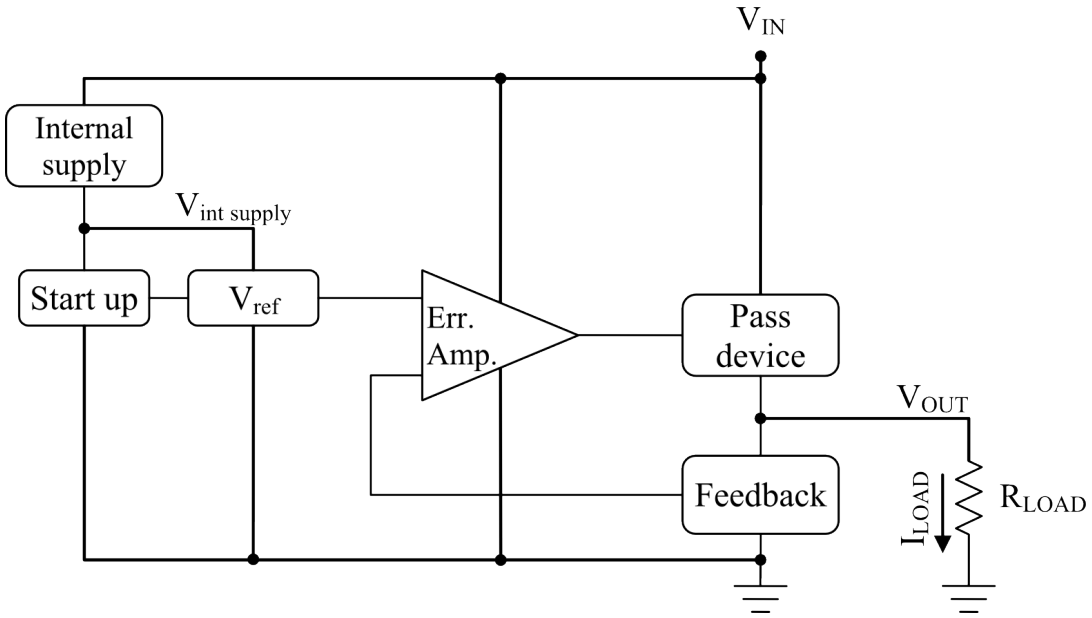


Figure 1.2: Generic linear regulator architecture.

The error amplifier makes possible to decrease the output error, by comparing the output voltage fed to the feedback network that (generally a resistor divider), with the voltage reference. The pass device implements the control of the error amplifier and, as we shall see, sets the minimum drop-out from the input to the output voltage. The internal supply pre-regulates the voltage for the voltage reference block, to increase the power supply rejection ratio or PSRR of the regulator. The reference provides a stable dc bias voltage with limited current driving capabilities. This is obtained using a zener diode, however, a band-gap reference is usually better suited for low voltage and high accuracy applications.

The error amplifier, the pass device, and the feedback network constitute the **regulation loop**. The function of the control loop is similar in all of the linear regulator types. The temperature dependence of the voltage reference and the error amplifier's input offset voltage define the overall temperature coefficient of the regulator; hence, low drift references and low input offset voltage amplifiers are preferred [5].

1.2 Analysis of a generic linear regulator

In figure 1.3 is displayed the regulation loop. We can note that the pass device is loaded with a real impedance that consists of four fundamental elements:

- the resistance part R_{LOAD},
- the load of the feedback network,
- the output capacitor C_{LOAD},
- the equivalent series resistance ESR of output capacitor.

On the next subsection we will analyse the steady-state behaviour and ac stability. Note that g_{mP} is a non-inverting block because the sign of loop gain must be negative. On the next pages we will handle a circuits topology that use a negative transconductance then to realise a negative feedback the error amplifier input will be flipped.

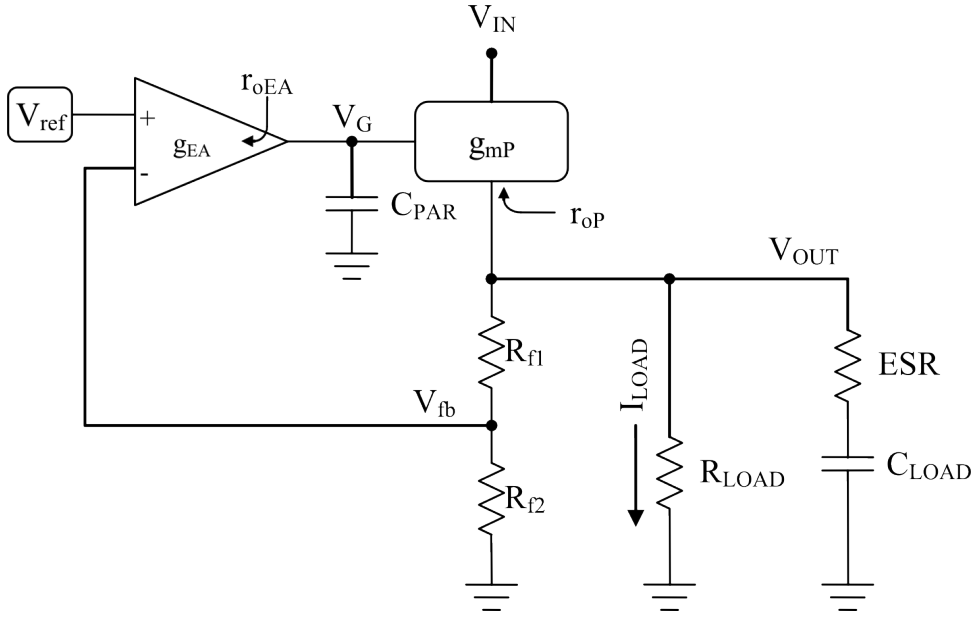


Figure 1.3: Regulation loop of a generic linear regulator with a real load.

1.2.1 Steady-state

The regulation loop will be faster as the bandwidth of loop gain T increases. When the loop has finished adjusting, the system reaches the steady-state. Ideally, in this state, we arrive at the condition that $V_{fb} = V_{ref}$ and $V_{id} \triangleq V_{ref} - V_{fb} = 0$. This condition is reached because the error amplifier feeds the correct voltage at the input of the pass device, so that the correct current causes $V_{fb} = V_{ref}$. For this reason we find at the output:

$$V_{out} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) V_{fb} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) V_{ref}.$$

In a real implementation of this circuit at the steady-state we define a static error gain ϵ_0 that depends to the DC loop gain T_0:

$$\epsilon_0 = \frac{1}{1 + T_0} \approx \frac{1}{T_0} \qquad \text{where } T_0 \text{ is} \qquad T_0 \triangleq \lim_{\omega \to 0} T(j\omega) \tag{1.1}$$

1.2.2 AC analysis and stability

The loop gain T is very important to understand if the entire system is stable or not. To calculate the loop gain T, we apply the return ratio analysis[1]. If we consider figure 1.4, we can first calculate the real impedance (equation 1.2)

$$\begin{aligned} Z_{out} &\triangleq R_x \Big/\!\Big/ \frac{1}{s\,C_b} \Big/\!\Big/ \frac{1 + s\,\mathrm{ESR}\,C_{LOAD}}{s\,C_{LOAD}} \\ &= \frac{R_x \cdot (1 + s\,\mathrm{ESR}\,C_{LOAD})}{1 + (\mathrm{ESR}\,C_{LOAD} + R_x\,C_{LOAD} + R_x\,C_b)\ s + (\mathrm{ESR}\,R_x\,C_{LOAD}\,C_b)\ s^2} \end{aligned} \tag{1.2}$$

where R_x is defined as the ac parallel resistance see at the output node.

$$R_x \triangleq r_{oP} /\!/ (R_{f1} + R_{f2}) /\!/ R_{LOAD} \tag{1.3}$$

Generally r_{oP} can be neglected, and for this reason we can approximate R_x as shown in equation 1.4.

$$R_x \approx (R_{f1} + R_{f2}) /\!/ R_{LOAD} \tag{1.4}$$

[1] See the appendix A for calculating steps.

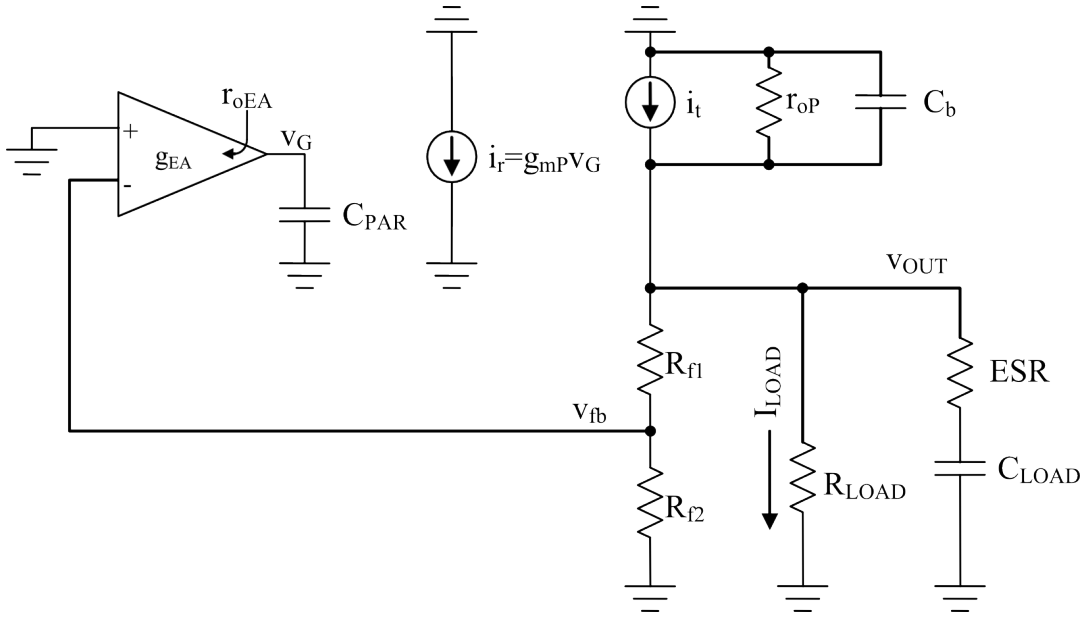


Figure 1.4: Hybrid small-signal circuit.

If C_{LOAD} is assumed to be reasonably larger than C_b, that is the typical condition, then it's possible approximate Z_{out} to:

$$Z_{out} \approx R_x \cdot \frac{1 + s\,\mathrm{ESR}\,C_{LOAD}}{(1 + s\,(\mathrm{ESR} + R_x)\,C_{LOAD}) \cdot (1 + s\,(\mathrm{ESR}//R_x)\,C_b)}. \tag{1.5}$$

At this point we can proceed as follows applying return ratio analysis:

$$\begin{aligned} v_{out} &= i_t\, Z_{out} \\ v_{fb} &= \tfrac{R_{f2}}{R_{f1}+R_{f2}} \cdot v_{out} = \tfrac{R_{f2}}{R_{f1}+R_{f2}}\, i_t\, Z_{out} \\ v_G &= (0 - v_{fb}) \cdot g_{EA} \left(r_{oEA} \Big/\!\Big/ \tfrac{1}{s\,C_{PAR}} \right) \\ &= -i_t\, Z_{out} \cdot \tfrac{R_{f2}}{R_{f1}+R_{f2}} \cdot \tfrac{g_{EA}\, r_{oEA}}{1+s\, r_{oEA}\, C_{PAR}} \\ i_r &= g_{mP}\, v_G \end{aligned} \tag{1.6}$$

$$\Rightarrow \mathcal{R}(s) = -\frac{i_r}{i_t} = g_{mP}\, Z_{out} \cdot \frac{R_{f2}}{R_{f1} + R_{f2}} \cdot \frac{g_{EA}\, r_{oEA}}{1 + s\, r_{oEA}\, C_{PAR}} \tag{1.7}$$

Now we have the return ratio $\mathcal{R}(s)$ that, under the hypothesis discussed in appendix A, satisfies $\mathcal{R}(s) \to T(s)$; where $T(s)$ is the loop gain.

It can be observed, from equation 1.7, that the system's loop gain consists of three poles and one zero: this is a potentially unstable system. The left-hand plane (LHP) poles and the zero can thus be approximated to be the following:

$$\begin{aligned} P_1 &= \frac{1}{2\,\pi\, r_{oEA}\, C_{PAR}} \\ P_2 &\approx \frac{1}{2\,\pi\,(\mathrm{ESR}+R_x)\, C_{LOAD}} \\ P_3 &\approx \frac{1}{2\,\pi\,(\mathrm{ESR}//R_x)\, C_b} \\ Z_1 &= \frac{1}{2\,\pi\,\mathrm{ESR}\, C_{LOAD}}. \end{aligned} \tag{1.8}$$

It is important to note that the order of the poles, depends on the architecture; in fact in the capacitor-less regulator we find first the pole between the output of the error amplifier and the pass device and then the output pole. In a classic linear regulator, we find a larger output capacitor, in order to assure the stability, and therefore the external pole is the first one. In figure 1.5 is illustrated the typical frequency response of the system assuming that the dominant-pole is at the output of the error amplifier and the output capacitor C_{LOAD} is larger than the capacitor C_b.

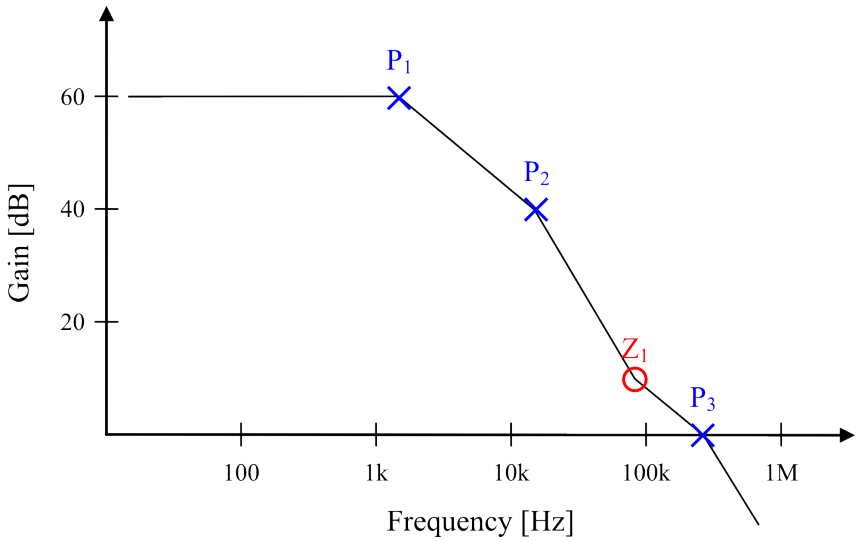


Figure 1.5: Asymptotic loop gain of a general linear regulator.

We can implement the circuit using an LDO architecture with ideal blocks as shown in figure 1.6. Here we find the three important blocks that constitute the regulation loop. The power MOS is the only real component; the feedback network, that is implemented with a

voltage controlled voltage source $E1$ and the error amplifier are ideal blocks. We can also note that a real modelling of a capacitor considers the equivalent series resistance ESR that generates a zero in the loop gain[2]. In DC analysis, V_2 gives the reference voltage but in AC analysis it is a virtual ground.

To study the loop gain in *Cadence*, we use STB analysis algorithm. V_3 is the point where the double insertion method or commonly called Middlebrook's Method is to be applied.

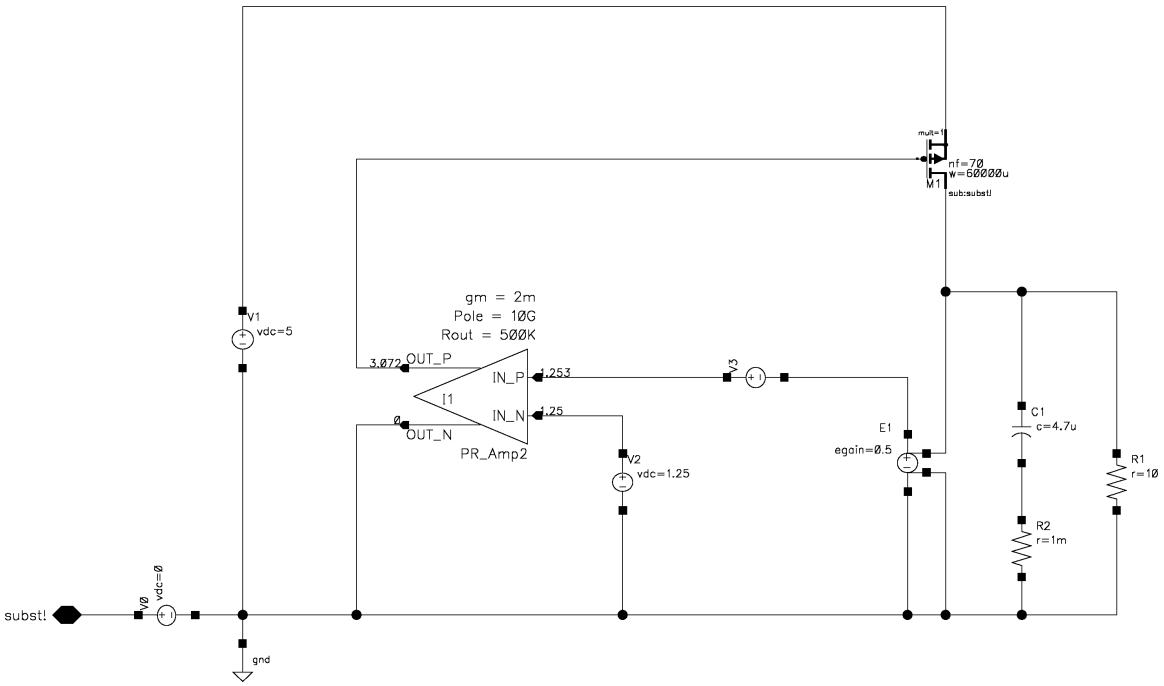


Figure 1.6: Quasi-ideal circuit of a LDO regulator, STB analysis.

The error amplifier is implemented by the circuit of figure 1.7, that depends on three parameters:

- the transconductance g_m,
- the internal pole Pole, that for simplicity is set at $10[GHz]$,

[2]There is a second zero that usually is not considered but depends on the architecture of the pass device. In figure 1.6 we consider an LDO architecture that exploits a common source configuration for realizing the pass device. This configuration has a right-hand plane (RHP) zero, generated by the C_{gd} of the power MOS and is called Miller's zero.

- the output resistance R_{out}.

We have implemented the error amplifier with two stages. The first stage amplifies the difference $v_{id} = IN_P - IN_N$ by a factor $A = g_m R_{out}$ equal to the DC gain, and also sets the internal pole at the frequency desired by changing the value of $C0$ by the following equation.

$$C0 = \frac{1}{2\,\pi\,R_{out}\,\mathrm{Pole}}.$$

The last stage is useful because we want an error amplifier that has a DC gain and two poles: one internal and the second one at the output (created with the gate capacitor of the power MOS and the error amplifier output resistance R_{out}). For this reason, the second stage is a voltage buffer that allows to set the output resistance and to separate the internal pole.

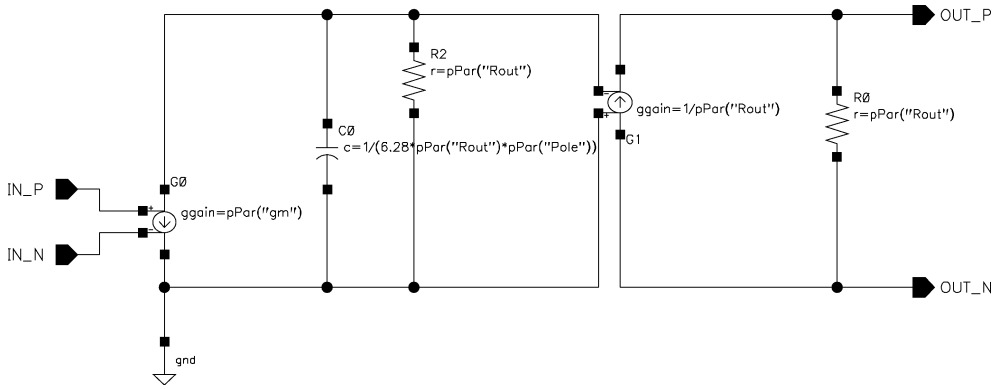


Figure 1.7: Quasi-ideal error amplifier.

In figure 1.8 we can see the loop gain magnitude and phase of the quasi-ideal regulator reported to the circuit of figure 1.6. We can note the near poles situated on the gate of the power MOS and to the output of regulator that represent P_1 and P_2. The left-hand plane (LHP) zero is situated at high frequency and corresponds to Z_1. The third pole P_3, is at high frequency and we can observe on the plot phase, in figure 1.8, the pole effect after the zero. The stability of the system is very low, indeed the phase margin is approximately $4[deg]$. This system has an oscillatory time response with a slow damping. On section 2, we will see how to improve the stability and increase the phase margin.

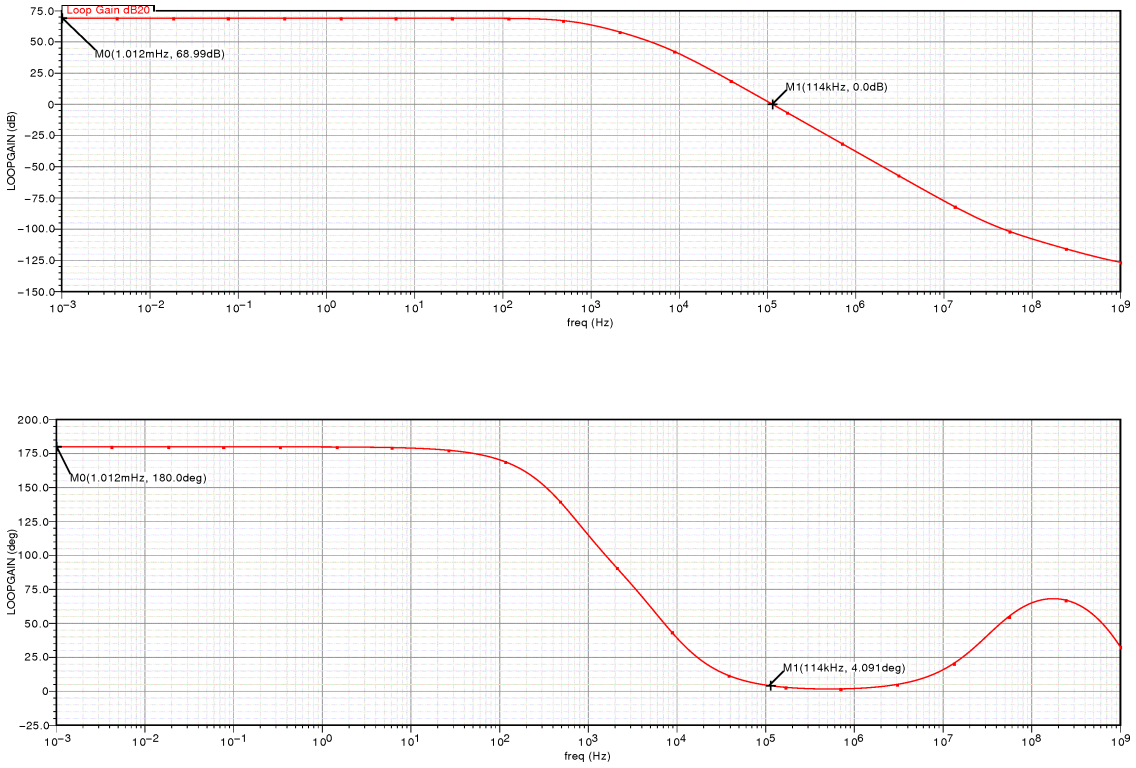


Figure 1.8: Typical loop gain of a quasi-ideal LDO regulator.

1.3 Linear regulator architectures

There are three basic types of linear regulator designs which will be shows [6]:

- Standard (NPN Darlington) Regulator,
- Low Drop-out (or LDO) Regulator,
- Quasi LDO Regulator.

The first most important difference between these three types is the **drop-out voltage**, which is defined as the minimum voltage drop required across the regulator to maintain output voltage regulation. A critical point to be considered is that the linear regulator that operates with the smallest voltage across it dissipates the least internal power and has the highest efficiency, in particular, the power dissipation resulting from the load current multiplied by the input-output voltage differential. The LDO requires the least voltage across it, while the Standard regulator requires the most.

The second important difference between regulator types is the **ground pin current** required by regulator when driving rated load current. Increased ground pin current is undesirable since it is wasted current, in that it must be supplied by the source but does not power the load.

1.3.1 Standard NPN Regulator

The first IC voltage regulators produced were using the NPN Darlington configuration as the pass device Q_1 and are now designated as the *standard regulator* (figure 1.9).

An important consideration of the *standard regulator* is that to maintain output regulation, the pass transistor requires a minimum voltage across it given by:

$$V_{DROP\ min} = 2V_{BE} + V_{CE}.$$

Allowing for the $-55[C]$ to $150[C]$ temperature range, this minimum voltage requirement is usually satisfied for about $2.5 - 3[V]$.

The voltage where the output actually falls out of regulation, called the drop-out voltage, will be probably between $1.5[V]$ and $2.2[V]$ for a *standard regulator* and will be dependent

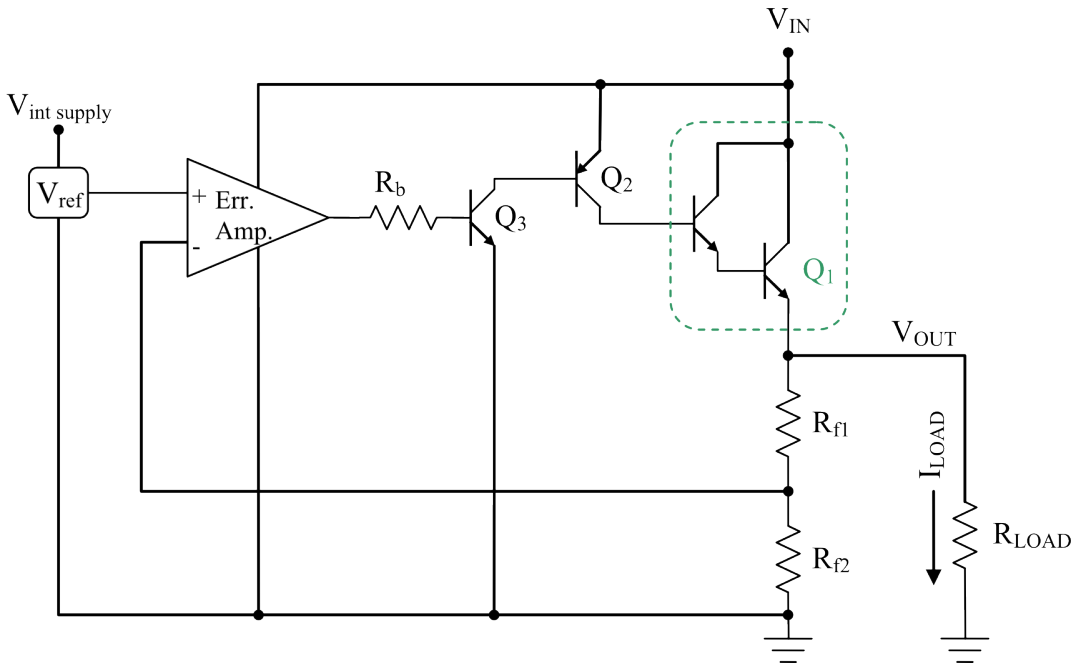


Figure 1.9: Standard NPN Regulator.

on both load current and temperature. Since the drop-out voltage of the *standard regulator* is the highest, this configuration is the worst of the three types.

The ground pin current of the *standard regulator* is very low. The reason for this is that the base drive current to the pass transistor, which flows out the ground pin, is equal to the load current divided by the gain of the pass device. In the *standard regulator*, the pass device is a network composed of one PNP Q_2 and two NPN transistors Q_1, which means the total current gain is extremely high (> 300).

The result of using a pass device with such a high current gain is that very little current is needed to drive the base of the pass transistor, which results in less ground pin current. Since the ground pin current of the *standard regulator* is the lowest, this configuration is the best of the three regulator types.

1.3.2 Low Drop-out or LDO Regulator

The low drop-out, or LDO, regulator differs from the *standard regulator* in that the pass device of the LDO is made up of only a single PNP transistor Q_1 as shown in figure 1.10.

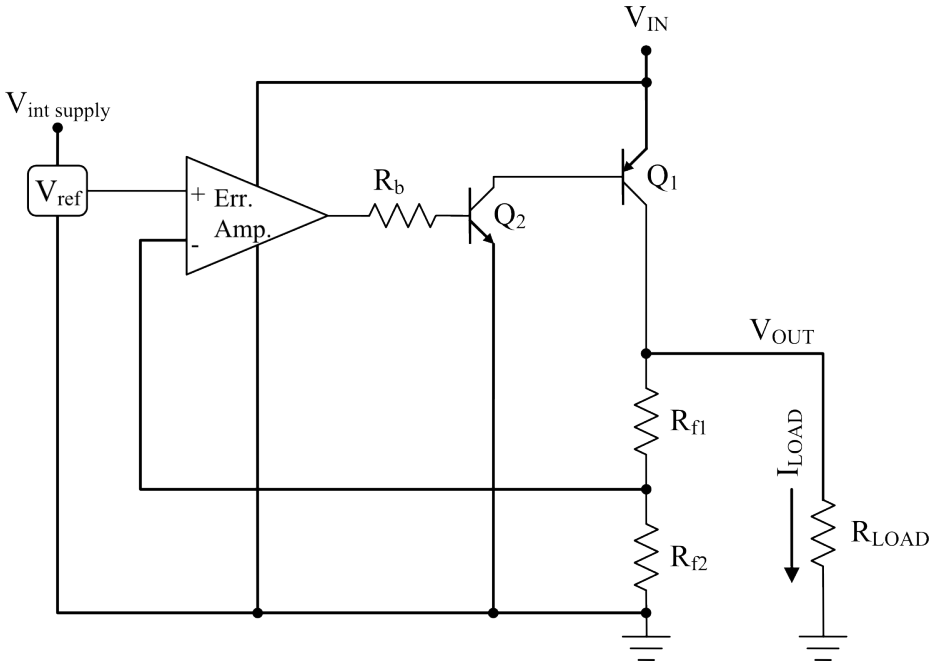


Figure 1.10: Low Drop-out or LDO Regulator.

The minimum voltage drop required across the LDO regulator to maintain regulation is just the voltage across the PNP transistor Q_1:

$$V_{DROP\ min} = V_{CE}.$$

The maximum specified drop-out voltage of an *LDO regulator* is usually about $0.7[V]$ to $0.8[V]$ at full current, with typical values around $0.6[V]$. The drop-out voltage is directly related to the load current, which means that at very low values of the load current, the drop-out voltage may be as little as $50[mV]$. The *LDO regulator* has the lowest drop-out voltage, and for this reason is the best of the three regulator types.

The lower drop-out voltage is the reason why *LDO regulators* dominate battery-powered applications, since they maximize the utilization of the available input voltage and can operate with higher efficiency. The explosive growth of battery-powered consumer products in the recent years has driven the development in the LDO regulator product line.

The ground pin current in an *LDO regulator* is approximately equal to the load current

divided by the gain of the single PNP transistor Q_1. Consequently, the ground pin current of an LDO is the highest of the three types.

1.3.3 Quasi Low Drop-out Regulator

A variation of the *standard regulator* is the *quasi low drop-out regulator*, more briefly called *Quasi LDO regulator*, which uses an NPN Q_1 and PNP Q_2 transistor as the pass device (figure 1.11):

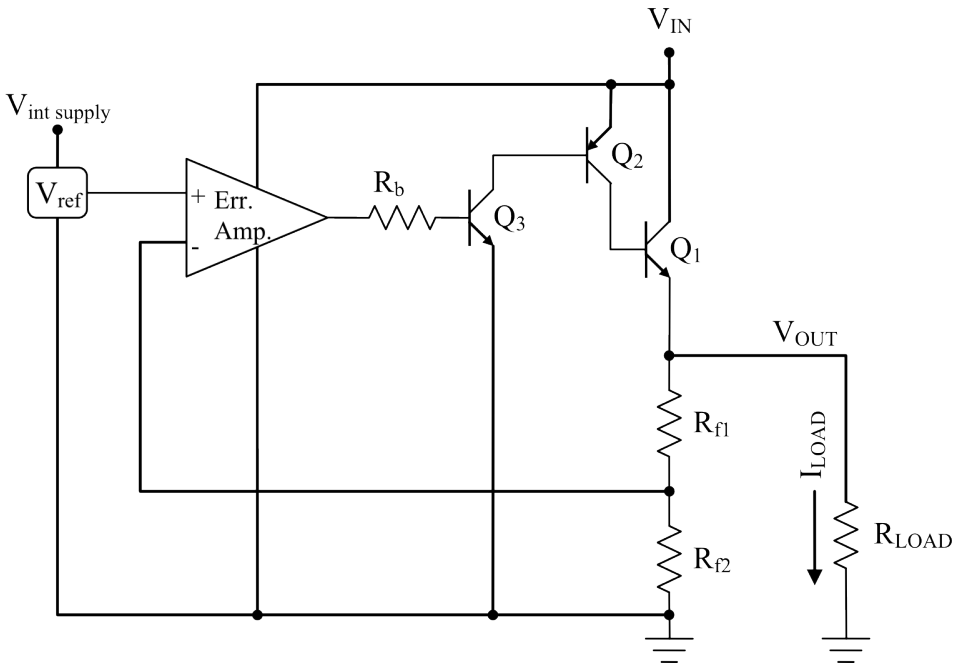


Figure 1.11: Quasi Low Drop-out Regulator.

The minimum voltage drop required across the *Quasi LDO regulator* to maintain regulation is given by:

$$V_{DROP\ min} = V_{BE} + V_{CE}.$$

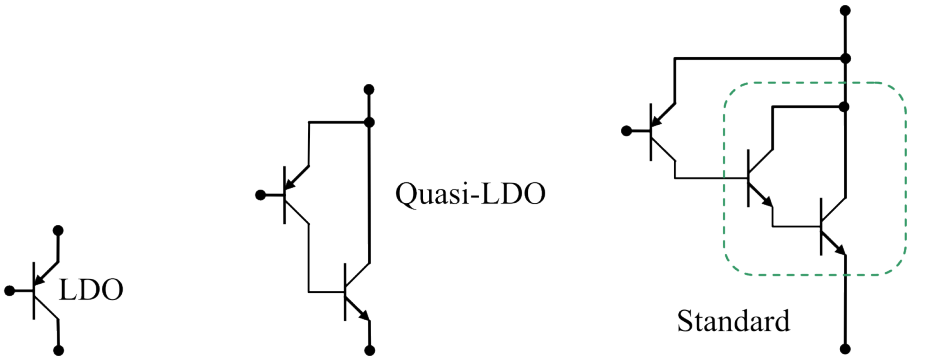
The drop-out voltage for a *quasi-LDO regulator* is usually specified at about $1.5[V]$ maximum. The actual drop-out voltage is temperature and load current dependent, but could never be expected to go lower than about $0.9[V]$ at $25[C]$ at even the lightest load.

The drop-out voltage for the quasi-LDO is higher than for the *LDO Regulator*, but lower than for the *standard regulator*.

The ground pin current of the *quasi-LDO* is fairly low which is as good as the *standard regulator*.

1.3.4 Summary

A comparison of the three regulator types [6] is shown in table 1.1. The *standard regulator*



$V_{DROP\ min} = V_{CE}$	$V_{DROP\ min} = V_{BE} + V_{CE}$	$V_{DROP\ min} = 2V_{BE} + V_{CE}$
$\sim 0.1[V]$ to $0.7[V]$	$\sim 0.9[V]$ to $1.5[V]$	$\sim 1.7[V]$ to $2.5[V]$
$I_{ground} \leq 20 \sim 40[mA]$	$I_{ground} \leq 10[mA]$	$I_{ground} \leq 10[mA]$
$I_{LOADmax} \approx 1[A]$	$I_{LOADmax} \approx 7.5[A]$	$I_{LOADmax} \approx 10[A]$

Table 1.1: Regulator type comparison.

is usually best for AC-powered applications, where the low cost and high load current make it the ideal choice. In AC-powered applications, the voltage across the regulator is usually at least $3[V]$ or more, so the drop-out voltage is not critical.

Interestingly, in this type of application (where the voltage drop across the regulator is $> 3[V]$) *standard regulators* are actually more efficient than LDO types, because they have less internal power dissipation due to ground pin current.

The *LDO regulator* is best suited for battery-powered applications, because the lower drop-out voltage translates directly into cost savings by reducing the number of battery cells required to provide a regulated output voltage. If the input-output differential voltage is low, like $1[V]$ to $2[V]$ the *LDO* is more efficient than a *standard regulator*, because of the

reduced power dissipation resulting from the load current multiplied by the input-output differential voltage.

1.4 Linear regulator characterization

All linear voltage regulators have constant output voltage regardless the supply voltage or load current variations. Voltage regulator specifications generally fall into three categories:

- steady-state specifications,
- dynamic-state specifications,
- high-frequency specifications [4].

All the equations presented consider only CMOS LDO voltage regulators, but the same basic principles relate to most other linear voltage regulators.

1.4.1 Steady-state specifications

The steady-state parameters include the line regulation, the load regulation, and the temperature coefficient effects.

The line and load regulation specifications are usually defined for a given LDO regulator, and measure the ability to regulate the steady-state output voltage for given line and load steady-state values. The temperature coefficient defines the combined performance of the voltage reference and the error amplifier offset voltage.

With reference to figure 1.12, we can define the block H with the following equation:

$$H \triangleq \frac{v_{fb}}{v_{out}} = \frac{R_{f2}}{R_{f1} + R_{f2}}. \tag{1.9}$$

It is also useful to model the path from the input of the internal supply to the output of the band gap as in equation 1.10.

$$K \triangleq \frac{v_{ref}}{v_{in}} \tag{1.10}$$

In particular, the block C is the transfer function from the source to the drain of pass transistor or power-mos. At first approximations the power-mos is in common gate

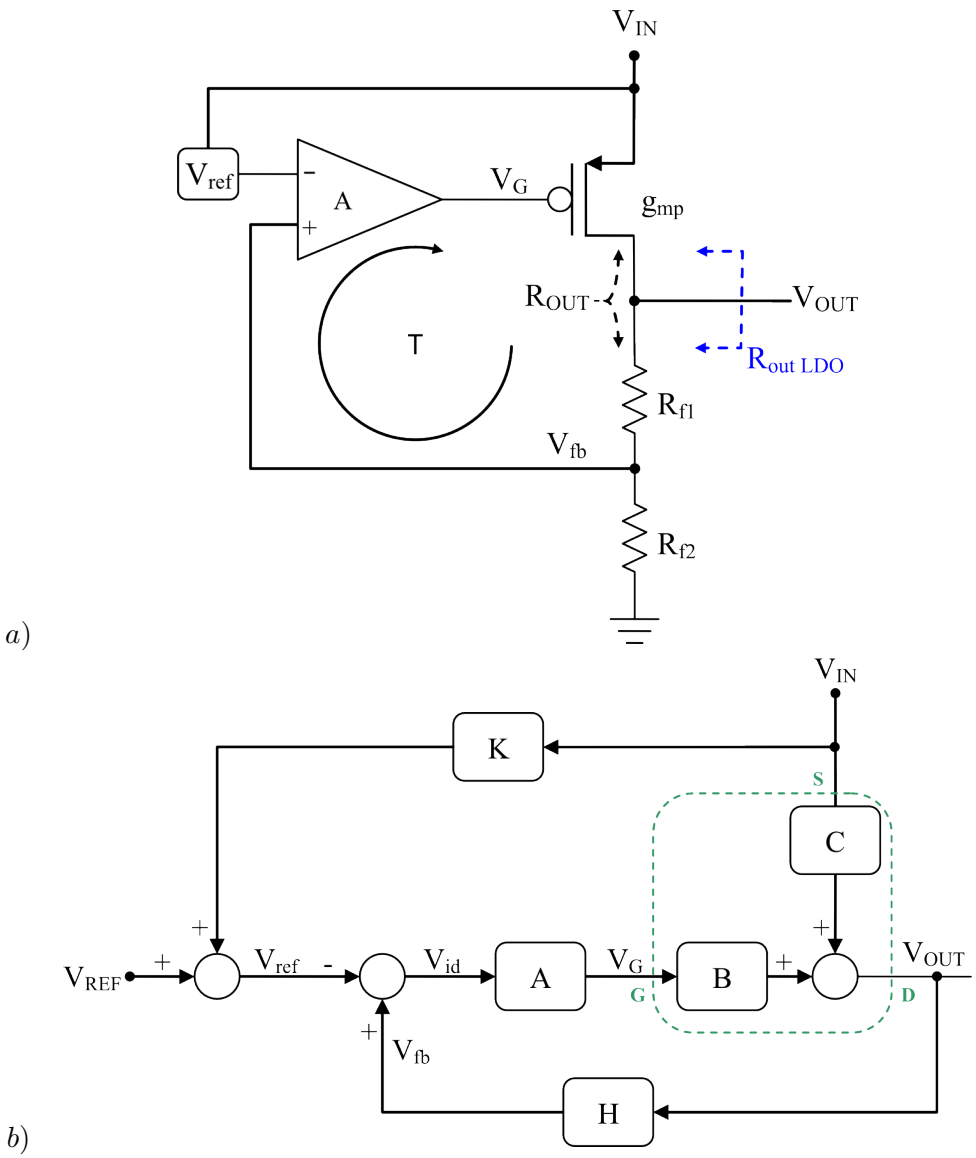


Figure 1.12: LDO regulator: *a*) ideal circuit diagram, *b*) relative block diagram.

configuration, and for this reason C is approximately:

$$C \triangleq \frac{v_{out}}{v_{in}} \approx g_{mp} R_{out}. \tag{1.11}$$

We can also note in figure 1.12a, the pass transistor transconductance g_{mp}, the pass transistor output impedance $R_{out} = r_{op}//(R_{f1} + R_{f2})$ and the loop gain $T = A\,B\,H$.

Line regulation defines the ratio of the output voltage deviation to a given change in the input voltage. This quantity reflects the deviation after which the regulator has reached steady-state. A general line regulation relationship is given in equation 1.12 [5]. Smaller output voltage deviation, for a given dc change in input voltage, corresponds to a better voltage regulator. To increase the line regulation, the LDO regulator must have a sufficiently large loop gain.

$$\frac{v_{out}}{v_{in}} = \frac{C}{1+T} + \frac{g_{mp} R_{out} A}{1+T} \cdot K \approx \frac{1}{AH} + \frac{K}{H} \tag{1.12}$$

Load regulation is a measure of output voltage deviation during no-load and full-load current conditions. The load regulation is related to the loop gain T, and the pass transistor output impedance, R_o. This relation is given in equation 1.13 [5].

$$R_{out\ LDO} = \frac{R_o}{1+T} \tag{1.13}$$

Temperature coefficient defines the output voltage variation due to temperature drift of the reference and the input offset voltage of the error amplifier. The temperature coefficient is given in equation 1.14 [5],

$$\begin{aligned} TC &\triangleq \frac{1}{V_{out}} \cdot \frac{\partial V_{out}}{\partial Temp} \\ &\approx \frac{1}{V_{out}} \cdot \frac{\Delta V_{TC}}{\Delta Temp} = \frac{\left(\Delta V_{TC\ ref} + \Delta V_{TC\ Voff}\right)\frac{V_{out}}{V_{ref}}}{V_{out} \cdot \Delta Temp} \end{aligned} \tag{1.14}$$

where TC is the temperature coefficient, ΔV_{TC} is the output voltage variation over the temperature range $\Delta Temp$, $\Delta V_{TC\ ref}$ and $\Delta V_{TC\ Voff}$ are the voltage variations of the reference and input offset voltage of the error amplifier, respectively. The output voltage accuracy improves as the error amplifier offset voltage is reduced and the reference voltage temperature dependence is minimized.

Drop-out voltage: the LDO regulator's drop-out voltage determines the maximum allowable current and the minimum supply voltage. These specifications - drop-out voltage, maximum load current, and minimum supply voltage - depend all on the pass transistor parameters. A particular LDO design typically specifies the maximum load current and the minimum supply voltage it can tolerate while maintaining pass transistor saturation. Equation 1.15 relates the LDO drop-out voltage to device parameters where I_{LOAD} is the maximum sustainable output current.

$$V_{drop-out} = I_{LOAD}\, R_{ON} = V_{DSAT\ \ PMOS} \tag{1.15}$$

The pass transistor dimensions are designed to obtain the desired V_{DSAT} at the maximum load current, I_{LOAD}.

1.4.2 Dynamic state specifications

The LDO regulator dynamic-state specifications specify the LDO regulator's ability to regulate the output voltage during load and line transient conditions. The LDO regulator must respond quickly to transients to reduce variations in the output voltage. Dynamic-state specifications, unlike steady-state specifications, depend also on the large signal LDO regulator capabilities. The most significant capabilities are the charging and discharging of parasitic capacitor and the parasitic capacitor feed-through.

Load transients define the LDO regulator's ability to regulate the output voltage during fast load transients. The largest variations in output voltage occur when the load-current steps from zero to the maximum specified value. The ability of the LDO to regulate the output voltage during a large current transient depends on the closed-loop bandwidth, the output capacitor, and the load-current. The output voltage variation is modelled in equation 1.16.

$$\Delta V_{out} = \frac{I_{max} \cdot \Delta t}{C_{LOAD}} \tag{1.16}$$

I_{max} is the maximum specified output current, Δt is the LDO response time, and C_{LOAD} is the LDO output capacitor. Δt is approximately the reciprocal of the LDO closed-loop bandwidth. A large output capacitor and a large closed-loop bandwidth improve the

load regulation. Conventional LDO regulators inherently have large output capacitors and therefore will have better load regulation compared to capacitor-less LDO regulators.

Parasitic capacitors also cause slewing effects that degrade the LDO regulator's load transient response. The gate capacitor of the pass transistor can be significant and places strain on the error amplifier. If the slew rate at the gate of the pass transistor is much slower than the gain-bandwidth product, significant transient voltage spikes appear at the output voltage node during fast load transients. This effect becomes more pronounced with capacitor-less LDO regulators.

Ripple-rejection-ratio specifies the ability for the regulator to reject the input signals from the output node. This parameter measures the small-signal gain from the input voltage to the output voltage. The ripple rejection ratio is given in equation 1.17.

$$Ripple\ \ rejection = 20 \cdot \log_{10} \frac{output\ \ ripple\ \ voltage}{input\ \ ripple} \tag{1.17}$$

The ripple-rejection-ratio is typically determined for lower frequencies within the gain-bandwidth product. Large input voltage transient spikes can cause larger output voltage variations than predicted by the ripple-rejection-ratio. The deviation is due to large signal effects, mainly capacitor slewing.

Power-supply-rejection-ratio, or PSRR, and regulator output noise can be categorized as high-frequency specifications. Both parameters are small signal parameters and are plotted versus frequency. Most LDO regulators specify PSRR at certain frequencies as well as spot noise at a particular frequency greater than the gain-bandwidth product.

PSRR defines the LDO regulator's ability to reject high-frequency noise on the input line. In figure 1.13 is shown the power-supply-rejection-ratio reference to LDO regulator of figure 1.6.

With reference to figure 1.12b, we can calculate the PSRR as:

$$\begin{aligned} v_{out} &= v_{in}\, C + A\, B\ (v_{in}\, K - v_{out}\, H) \\ v_{out}\, (1 + A\, B\, H) &= v_{in}(\, C + A\, B\, K) \end{aligned} \tag{1.18}$$

Where PSRR is:

$$\Rightarrow \text{PSRR} \triangleq \frac{v_{in}}{v_{out}} = \frac{1 + A\, B\, H}{C + A\, B\, K}. \tag{1.19}$$

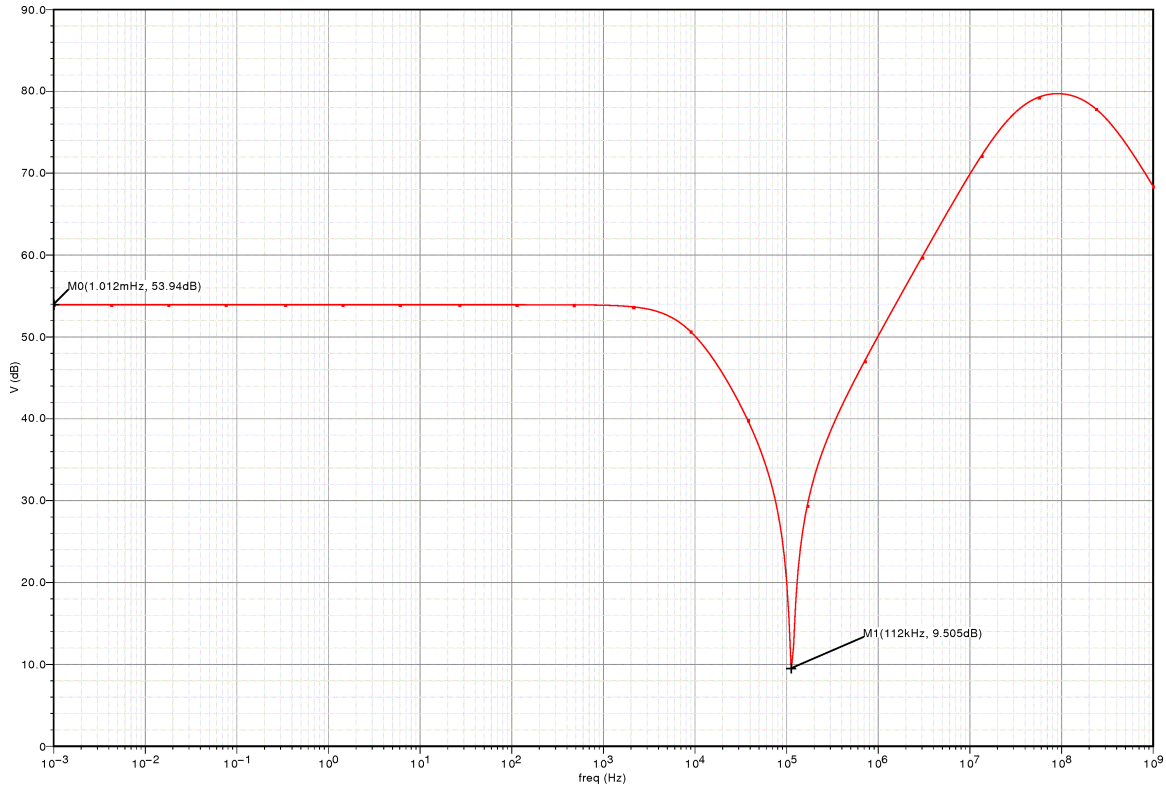


Figure 1.13: PSRR of a LDO regulator.

If we assume that the path from the input of the internal supply to the output of the band gap is negligible or $K \approx 0$, we obtain equation 1.20.

$$\text{PSRR} \approx \frac{1 + A\,B\,H}{C}. \tag{1.20}$$

As shown in equation 1.20, PSRR is a function of pass transistor parasitic capacitor, error amplifier and feedback network. On low frequencies, PSRR is dominated by the loop gain over C, while at high frequencies depends on the reciprocal of the block C. In table 1.2 are summarized all these concepts.

Asymptote at low frequency	Asymptote at high frequency
$\text{PSRR} \approx \frac{A\,B\,H}{C}$	$\text{PSRR} \approx \frac{1}{C}$

Table 1.2: Summary of asymptote of PSRR.

The error amplifier plays a major role in improving PSRR [2]. The combined individual error amplifier PSRR and the individual pass transistor PSRR are desired to sum to zero at the output voltage node.

Output noise is primarily defined by the input stage transconductance. The subsequent stages do not add significant noise to the output. Maximizing the input transistors' size lowers the output noise. The optimal noise figure is dependent on each particular design and a general analysis lacks sufficient information.

1.4.3 LDO Regulator Efficiency

The LDO regulator efficiency is determined by three parameters: ground current, load current, and pass transistor voltage drop. The total no-load quiescent current consumption for the entire LDO regulator circuitry is defined as the ground current. Equation 1.21 relates the LDO regulator power efficiency.

$$Eff = \frac{V_{out} \cdot I_{LOAD}}{V_{in} \cdot (I_{GND} + I_{LOAD})} \tag{1.21}$$

There are two cases for power efficiency, one for small load currents and one for large load currents. If is assume that $V_{out} \approx V_{in}$, the relation reduces to equation 1.22 for small load currents.

$$Eff \approx \frac{I_{LOAD}}{I_{GND} + I_{LOAD}} \tag{1.22}$$

Thus, the ground current affects the LDO regulator efficiency much more at very low load currents. The longevity of the battery life for low current applications can be significantly increased by reducing the quiescent ground current. On the other hand, for very large load currents, the power efficiency is solely dependent on the pass transistor voltage drop, shown in equation 1.23.

$$Eff \approx \frac{V_{out}}{V_{in}} \tag{1.23}$$

The efficiency of the linear regulator approaches 100% as the output voltage approaches the input voltage. This scenario, however, requires an infinitely large pass transistor and would result in an infinite gate capacitor. Clearly, there is a trade-off between efficiency and the speed of the LDO regulator.

1.5 Power Management Unit - PMU

In mobile devices, the battery management is very important since it is the good use of the battery energy that allows the devices to become more and more durable. In the most modern PMUs, the LDOs are used as post regulators. The DC-DC converters or switching regulators are used to convert one voltage level into a lower[3] one because of their high efficiency. The main problem of not using only the DC-DC converter is the ripple in the output voltage. So, in order to remove this ripple and load variations, a LDO is used after the DC-DC converter. The DC-DC regulator is designed to minimize the voltage drop across the linear regulator during loading conditions, as shown in figure 1.14.

[3]It is possible to convert one voltage level into a lower one with a buck or buck-boost configuration. Generally the DC-DC converters have the ability to generate larger or lower output voltages than the input and they can yield efficiencies between 85 and 98 %.

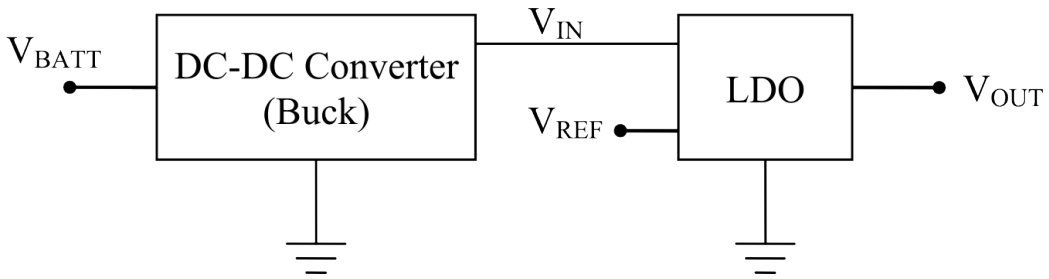


Figure 1.14: High efficiency linear regulation.

Chapter 2

LDO compensation

This chapter will enable to understand the techniques to compensate a Low Drop-out regulator. Two techniques will be described: the former, named standard, is the classic solution adopted in many linear regulator topologies that exploits the dominant-pole compensation, the latter one exploits pole splitting.

2.1 Standard compensation

In figure 2.1 is displayed a LDO regulator that exploits the dominant-pole compensation.

One of the most significant side effects in LDOs is the stability degradation due to the several poles embedded in the loop. The loop presents the following pole and zero frequencies[1]:

$$\begin{aligned} f_{P_G} &= \frac{1}{2\,\pi\,R_{outEA}\left(C_{gs}+C_{gd}(1+g_{mp}\,R_x)\right)} \\ f_{P_{out}} &= \frac{1}{2\,\pi\,R_x\,C_{LOAD}} \\ f_{Z_1} &= \frac{g_{mp}}{2\,\pi\,C_{gd}} \end{aligned} \tag{2.1}$$

where g_{mp}, C_{gs} and C_{gd} are the equivalent transconductance and capacitances of the ac model of the power MOS, R_x is defined in equation 1.3 while C_{LOAD} is the output capacitance. Note that Z_1 is a right-hand plane (RHP) zero and therefore reduces loop phase margin.

[1]For simplicity the equivalent series resistance effect has been neglected.

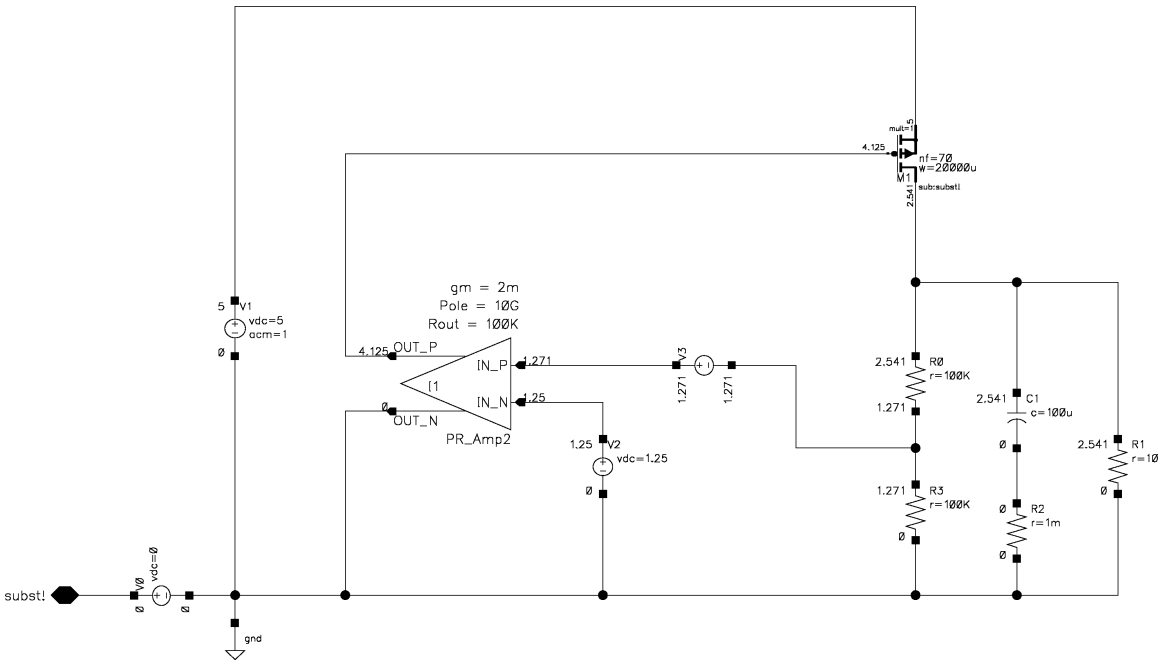


Figure 2.1: LDO regulator circuits with the dominant-pole compensation.

Usually, the standalone error amplifier has at least one internal pole located at relatively high frequency. In the circuit of figure 2.1 this internal pole is at very high frequency ($10[GHz]$); in a real realization of this circuit, the loop is affected by this internal pole and the circuit is probably unstable.

The output pole is inversely proportional to R_{LOAD}. The parameters used in the circuit of figure 2.1 are the following:

I_{LOAD}	R_{LOAD}	R_x	C_{LOAD}	$f_{P_{out}}$
$12.7[\mu A]$	not connected	$190[k\Omega]$	$100[\mu F]$	$8[mHz]$
$250[mA]$	$10[\Omega]$	$9.3[\Omega]$	$100[\mu F]$	$170[Hz]$

Table 2.1: Variation of the output pole.

In table 2.1 is also shown the large variation of the output pole frequency, $f_{P_{out}}$: more than four orders of magnitude; this effect requires to find a trade-off between of the stability and the quiescent current. In fact, in order to have a low variation of the output pole, while

keeping constant the other parameters of the circuit, one should decrease the R_x value. This translates in a decrease of $R_{f1}+R_{f2}$ and therefore,an increase of the quiescent current I_{GND}. On the other hand, decreasing I_{GND}, decreases the phase margin of the loop gain $T(s)$. These aspects allow to understand why the change in R_{LOAD} varies the stability of the circuit (figure 2.2). Note that the phase margin PM changes from 35 to 90 degrees.

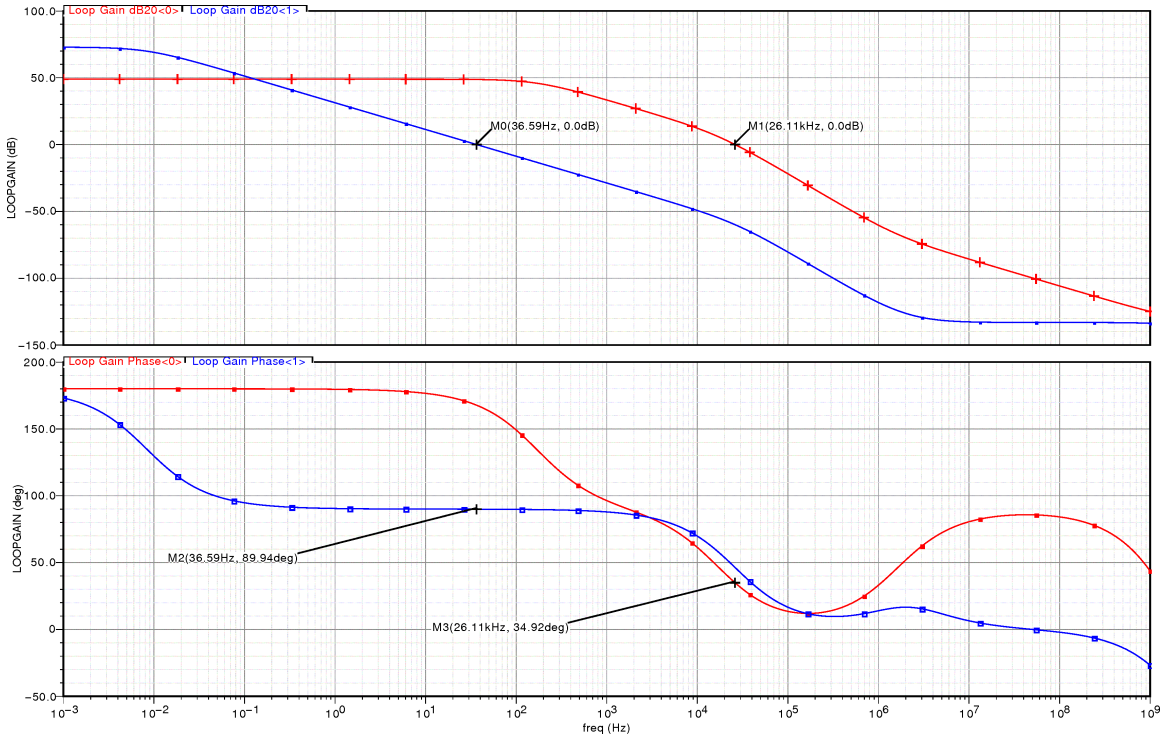


Figure 2.2: Loop gain $T(s)$ of the circuit of figure 2.1. In red $I_{ds} = 250[mA]$, while in blue $I_{ds} = 12.7[\mu A]$ (equal to the current that flows only through the resistor divider).

Some options to increase the distance between the poles at the gate and at the output of regulator, do exist. To change the time constant at the gate of the power MOS, it is possible to:

- decrease the output resistance of the error amplifier. This in turn decreases the DC loop gain T_0 and increases the static error gain ϵ_0, while lowering the low frequency,
- decrease C_{gs} of the power MOS. Most likely, this implies to decrease the product $W\,L$, which consequently increases the drop-out voltage that usually is not allowed

to change, due to design requirements.

To change the time constant at the output of the regulator, it is possible to increase the resistance R_x defined in equation 1.3, working on $R_{f1} + R_{f2}$ or R_{LOAD}.

Increasing $R_{f1} + R_{f2}$, decreases the quiescent current but when $R_{LOAD} \to \infty$, the power MOS works in sub-threshold zone and it has a very small g_{mp}[2]. For this reason to ensure the regulation $R_{f1} + R_{f2}$ can not increase too much.

Increasing the minimum R_{LOAD} decreases the maximum load current but is exploits only a part of the available current from the power MOS that it results oversized.

For these reasons to reach the stability usually the best choice is to increase the C_{LOAD} capacitance.

The DC gain of the power MOS is equal to $-g_{mp} R_x$. Increasing g_{mp} increases the loop gain while the phase margin decreases because it begins to be influenced by the pole at the gate of the power MOS.

This analysis shows the difficulties to compensate the regulator when increasing the current load. Alternative solutions that allow to increase the regulator's current, required to change the type of compensation.

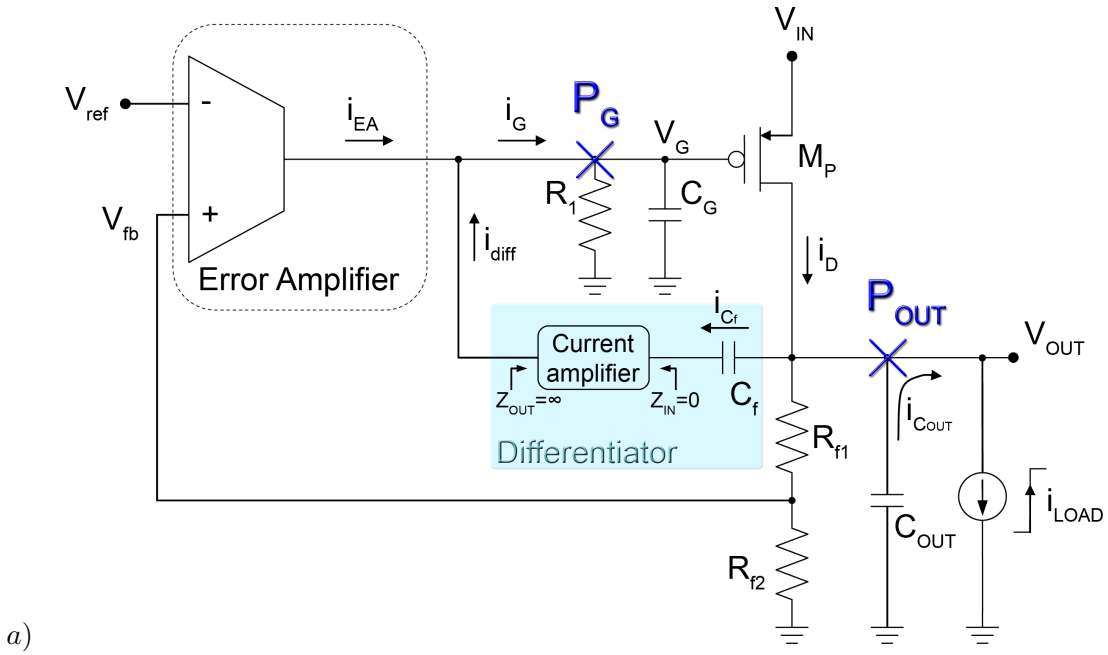
2.2 Proposed LDO compensation

To compensate the LDO regulator while keeping acceptable the load transient response and the stability at low load currents, a new structure was needed. The basic concept is shown in figure 2.3a.

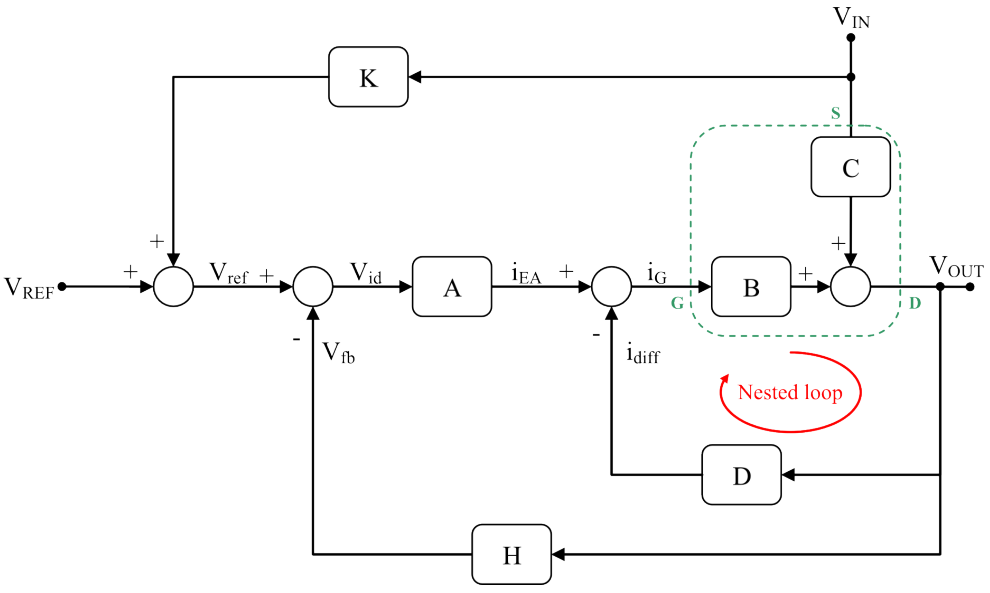
2.2.1 Steady-state

At steady-state, the fast path, that is realised with a differentiator block, is as an open circuit; this means that the regulator works as a classic LDO. Indeed, when the transient has faded, the output voltage is regulated by the external loop. At high frequencies, where the external loop gain is low, the fast path is able to control the load variation, acting on the gate of the power MOS. The main feedback loop determines the LDO's gain-bandwidth

[2]When $R_{LOAD} \to \infty$, $I_{DS} \to \frac{V_{out}}{R_{f1}+R_{f2}}$ but $V_{DS} = V_{out} - V_{in}$ remains constant whereby V_{GS} decreases. If the voltage headroom of the error amplifier is small, it is likely that V_G cannot reach the correct value, thus making it impossible to regulate the output.



a)



b)

Figure 2.3: Proposed LDO compensation: *a)* basic concept, *b)* blocks level description.

product and is the main mechanism that replenishes the energy in the output capacitor, restoring the output voltage to the correct steady-state level. The fast path is an internal negative feedback loop with very high bandwidth: much greater than the overall gain-bandwidth product, that senses any load current variation mirroring and amplifying the signal directly into the gate of the pass transistor.

2.2.2 Ac analysis - blocks level description

The ac analysis of the circuit of figure 2.3a, can be made by first defining some transfer functions.

- The block B represents the transfer function from the current at the gate of the power MOS $i_G \triangleq i_{EA} + i_{diff}$ (the sum of the output current of the error amplifier i_{EA} and the differentiator current i_{diff}) to the regulator output voltage v_{out} where the ac variations at the input voltage v_{in} are assumed to be zero:

$$B \triangleq -\left.\frac{v_{out}}{i_G}\right|_{v_{in}=0} \approx \frac{R_1\, g_{mp}\, R_x\, \left(1 - s\,\frac{C_{gd}}{g_{mp}}\right)}{(1 + s\, R_1\, C_G)\,(1 + s\, R_x\, C_{LOAD})} \tag{2.2}$$

  where $C_G \triangleq C_{gs} + C_{gd}\,(1 + g_{mp}\, R_x)$.

  On first approximation, the block B consists of the pole at the gate of the power MOS, the output pole and the Miller's zero (equation 2.2). The power MOS is in common source configuration; the DC gain of this stage is inverting. For this reason the sign of block B is positive: because it is useful to move back the sign to highlight the two negative loops: the nested one and the external one.

- The block D, that represents the differentiator transfer function, is defined as the ratio of the differentiator output current i_{diff} to the output voltage of the regulator v_{out}:

$$D \triangleq \frac{i_{diff}}{v_{out}} = A_i\, s\, C_f \tag{2.3}$$

  where $A_i \triangleq \frac{i_{diff}}{i_{c_f}}$ is the current gain. This block realises the split of the poles in block B; such operation is called **pole splitting**.

It is possible to define the nested loop gain as:

$$T_{nest} \triangleq B\, D \approx \frac{R_1\, R_x\, g_{mp}\, A_i\, C_f\, s\, \left(1 - s\,\frac{C_{gd}}{g_{mp}}\right)}{(1 + s\, R_1\, C_G)\,(1 + s\, R_x\, C_{LOAD})}. \tag{2.4}$$

The transfer function from i_{EA} to v_{out} at closed loop is:

$$B' = \frac{B}{1 + B\,D} = \frac{R_1\,R_x\,g_{mp}\,\left(1 - s\,\frac{C_{gd}}{g_{mp}}\right)}{a\,s^2 + b\,s + c} \tag{2.5}$$

because a negative feedback is considered. The coefficients of the denominator are:

$$\begin{aligned} a &= C_G\,C_{LOAD}\,R_1\,R_x - A_i\,C_f\,C_{g_d}\,R_1\,R_x \\ b &= C_G\,R_1 + C_{LOAD}\,R_x + A_i\,C_f\,R_1\,R_x\,g_{mp} \\ c &= 1 \end{aligned} \tag{2.6}$$

that can be approximated because:

$$\begin{aligned} &C_G\,C_{LOAD}\,R_1\,R_x >> A_i\,C_f\,C_{g_d}\,R_1\,R_x \\ &C_G\,R_1 + C_{LOAD}\,R_x << A_i\,C_f\,R_1\,R_x\,g_{mp}. \end{aligned} \tag{2.7}$$

Thus, we obtain:

$$B' \approx \frac{R_1\,R_x\,g_{mp}\,\left(1 - s\,\frac{C_{gd}}{g_{mp}}\right)}{1 + A_i\,C_f\,R_1\,R_x\,g_{mp}\,s + C_G\,C_{LOAD}\,R_1\,R_x\,s^2}. \tag{2.8}$$

Assuming the dominant-pole condition, we obtain the following pole frequencies:

$$\begin{aligned} f_1 &\approx \frac{1}{2\,\pi\,R_1\,C_f\,(A_i\,g_{mp}\,R_x)} \\ f_2 &\approx \frac{g_{mp}\,A_i\,C_f}{2\,\pi\,C_G\,C_{LOAD}}. \end{aligned} \tag{2.9}$$

This technique is named pole splitting compensation. In the next table we can appreciate the splitting of the poles with or without differentiator.

	$D = 0 \rightarrow T_{nest} = 0$	$D >> 0 \rightarrow T_{nest} >> 1$
Dominant-pole	$\frac{1}{R_1\,C_G}$	$\frac{1}{R_1\,C_f\,(A_i\,g_{mp}\,R_x)}$
Second pole	$\frac{1}{R_x\,C_{LOAD}}$	$\frac{g_{mp}\,A_i\,C_f}{C_G\,C_{LOAD}}$

Table 2.2: Pole splitting.

In figure 2.4 is shown how the equivalent transfer function of the block B changes if we increase the nested loop gain T_{nest}. The graphical analysis is an easy way to understand how the feedback acts with respect to mathematical treatment.

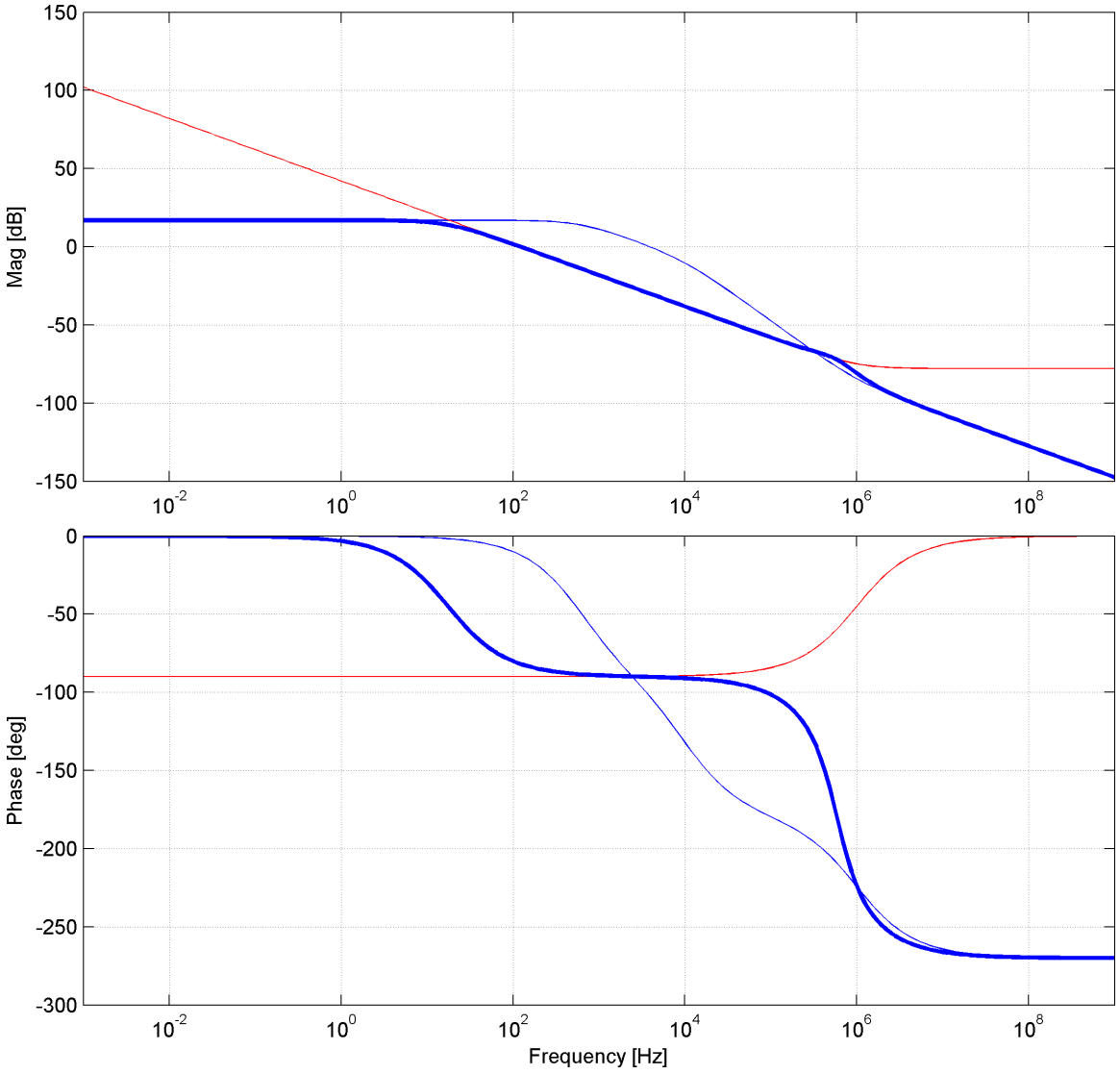


Figure 2.4: Action of the nested loop; graphical analysis. The thin blue line is the block B, the red line is $\frac{1}{D}$ while the thick blue line is the transfer function that the error amplifier sees (with the closed nested loop).

From the circuits of figure 2.3a it is possible to obtain the block-level description of all the regulator (figure 2.3b). The analysis with the block diagram is useful for understanding how the fast loop or nested loop compensates the voltage regulator[3].

On the next list, the transfer functions of the remaining blocks of figure 2.3b are defined.

- The block A represents the error amplifier transfer function, defined by the ratio of the output current of the error amplifier i_{EA} to the difference $v_{id} \triangleq v_{ref} - v_{fb}$.

  $$A \triangleq \frac{i_{EA}}{v_{ref} - v_{fb}} = \frac{i_{EA}}{v_{id}} \tag{2.10}$$

  The block A is a transconductance with an internal pole, because generally the error amplifier is realized with two stages.

- The block C represents the transfer function from the input voltage to the output voltage, where the variations at the gate current i_G are assumed to be zero.

  $$C \triangleq \frac{v_{out}}{v_{in}}\bigg|_{i_G=0} \tag{2.11}$$

  On first approximation, it is possible to note that the power MOS is in common gate configuration.

- The block H represents the resistor divider transfer function, defined by:

  $$H \triangleq \frac{v_{fb}}{v_{out}} = \frac{R_{f2}}{R_{f1} + R_{f2}}. \tag{2.12}$$

- The block K represents the band-gap transfer function. It is important to model it, to improve the precision of the PSRR.

The total loop gain or external loop gain is defined by:

$$T_{total} \triangleq A \frac{B}{1 + B\,D} H. \tag{2.13}$$

The bandwidth of the system is defined as the frequency where the loop gain $T(s)$ is unitary. If is designed a dominant-pole system where i.e, the effect of the second pole can be neglected, then it is possible to write that:

$$\text{GBW} \approx \frac{A_{DC}\,B_{DC}\,H_{DC}}{2\,\pi\,R_1\,C_f\,\left(A_i\,g_{mp}\,R_x\right)} \tag{2.14}$$

[3]It is possible to use the `LDO behavior`, a graphical user interfaces - GUI, that I personally create, to better understand how the nested loop works in the LDO voltage regulators. See appendix B for more information about `LDO behavior`.

where A_{DC}, B_{DC} and H_{DC} are the DC gain of the respective blocks.

Now we can recalculate the PSRR including the new branch:

$$\begin{aligned} v_{out} &= v_{in}\, C + [A\ (v_{in}\, K - v_{out}\, H) - v_{out}\, D]\ B \\ v_{out}\,(1 + A\, B\, H + B\, D) &= v_{in}(\, C + A\, B\, K) \end{aligned} \tag{2.15}$$

And the PSRR is:

$$\Rightarrow \text{PSRR} \triangleq \frac{v_{in}}{v_{out}} = \frac{1 + B\,(A\, H + D)}{C + A\, B\, K}. \tag{2.16}$$

2.2.3 Transient response

The transient response is dependent on the speed of the pass transistor and not on the output capacitor [4]; however, using the fast path, it is possible to improve it. For example, a quick change in the current load i_{LOAD}, causes a quick transient current flowing from C_{out} and another one from C_f, since the power MOS current is supposed to be constant. The current amplifier stage copies and amplifies the current i_{C_f} and causes a decrease of the gate voltage V_G. For this reason the fast loop feedback turns increasingly on the power MOS, which in turn increases the current i_D. When the current i_D increases, the current from C_f decrease and shut down the differentiator. After this fast regulation the external loop decreases the difference between V_{ref} and V_{fb}, while V_{out} returns to the desired DC voltage. On the other hand a slow variation in i_{LOAD} induced a consequent reaction in the external loop (that includes the power MOS), and a no appreciable contribution from the other loops.

The concept in figure 2.3 sets the basis of the research and design for the LDO voltage regulator study proposed in this thesis work.

2.2.4 Target design

The LDO regulator design targets are shown in table 2.3.

Parameter	Value
Gain Bandwidth	$0.5 \sim 1[MHz]$
Loop Gain	$80[dB]$ @ maximum load current
PSRR[4]	$> 70[dB]$ @ $10[kHz]$ $> 40[dB]$ @ $100[kHz]$
GND Current	$\approx 100[\mu A]$
Output Current	$0 \sim 1[A]$
Output Voltage	$\approx 1.2[V]$
Reference Voltage	$\approx 0.8[V]$
Minimum C_{load}[5]	$1[uF]$
Maximum C_{load}	$4.7[uF]$
Technology	$2[\mu m]$ CMOS

Table 2.3: LDO specification.

[4]High Ripple Rejection over full current range with $C_{load} = 1[\mu F]$.

[5]The minimum capacity that ensures the stability.

Chapter 3

Modelling of blocks

In this chapter the circuit previously proposed will be presented and analysed. Moreover, it will be shown how to obtain the transfer function of all the blocks that constitute the regulator described in figure 2.3b.

The proposed circuit, shown in figure 3.1, was developed with *Cadence* and highlights the nested loop, composed by the power MOS and differentiator blocks, and the external loop composed by the error amplifier, power MOS (with its compensation) and feedback network blocks.

3.1 Error amplifier

The proposed error amplifier is shown in figure 3.2. In the literature [1] this circuit consists of a basic single-ended two-stage Bi-CMOS operational transconductance amplifier or more briefly two-stage single-ended OTA. A differential input stage drives an active load followed by a second gain stage. The first stage in figure 3.2, consists of a p-channel differential pair realized by M_1 and M_2, with an n-channel current mirror load M_3 and M_4. The tail current source, is provided by a bipolar PNP transistor T_1 with an emitter resistive degeneration. The second stage consists of a n-channel common-source amplifier M_5 with the current source load T_2.

This circuit configuration was chosen because it provides a good voltage gain, output swing, common-mode range and common mode rejection ratio CMRR [1].

The steady-state of this circuit has the output OUT that hits V_I or GND like a

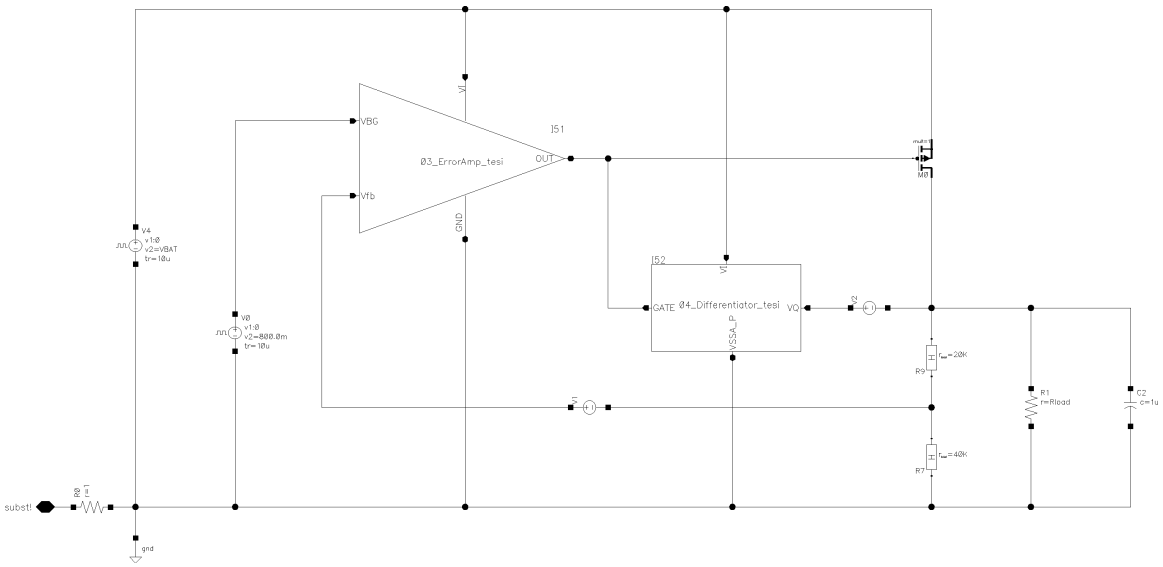


Figure 3.1: Main circuit.

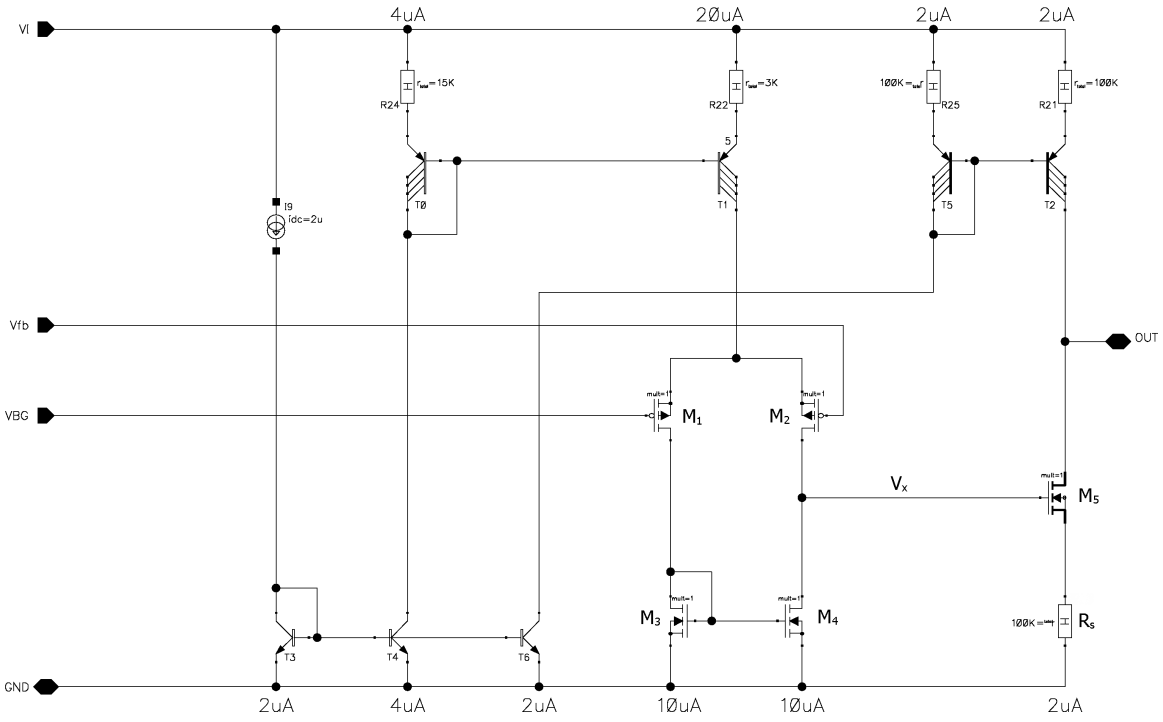


Figure 3.2: Proposed error amplifier.

comparator. Near these two limit zones, this circuit does not work like an error amplifier. On the other hand, when this circuit is closed in a negative feedback, the steady-state is reached and the output of the error amplifier is between $2[\mu A]\,100[k\Omega] + V_{ov5}$ and $V_I - 2[\mu A]\,100[k\Omega] - V_{EC}$.

When this state is reached, i.e where all MOSFET work in the saturation zone, the ac analysis can be done.

The ac gain of the first stage is:

$$A_1 = \frac{v_x}{v_{fb}} = \frac{-g_{m2}\,(r_{o2}//r_{o4})}{1 + s\;(r_{o2}//r_{o4})\;C_x} \tag{3.1}$$

where $r_{o2}//r_{o4}$ and C_x are respectively the equivalent resistance and capacitance at the output node of the first stage. Generally the natural frequency of this internal pole is near the unity gain frequency of the loop gain $T(s)$.

In the previous analysis the effect of the pole-zero doublet created by the active load M_3 M_4 is neglected. Generally the dominant pole of the first stage is given by the output time constant that is at much lower frequencies than the pole-zero doublet; for this reason is negligible.

The transconductance of the second stage is affected by the source resistance degeneration R_s. For this reason the equivalent transconductance G_{m2} is:

$$G_{m2} = \frac{i_{outEA}}{v_x} = \frac{-g_{m5}}{1 + g_{m5}\,R_s}. \tag{3.2}$$

The complete transfer function of block A is:

$$A = \frac{i_{outEA}}{v_{fb}} = A_1 \cdot G_{m2} = \frac{g_{m2}\,(r_{o2}//r_{o4}) \cdot g_{m5}}{(1 + g_{m5}\,R_s) \cdot (1 + s\;(r_{o2}//r_{o4})\;C_x)}. \tag{3.3}$$

The natural frequency of the pole of this block is:

$$f_{P_{int}} = \frac{1}{2\,\pi\;(r_{o2}//r_{o4})\;C_x}. \tag{3.4}$$

3.2 Power MOS

Generally, in LDO regulators, the power MOS represents the biggest component, as it can be seen in the layout images (figures 4.5a and 4.5b). For this reason, it is important to regard the principal ac parameters, C_{gs} and C_{gd}, that can reach values of few hundreds

of pico Farads. Usually the aspect ratio, $\frac{W}{L}$, is greater than some tens of thousands and generally the minimum length channel is used, to achieve the drop-out specification that requires a large aspect ratio.

The power MOS operates in strong inversion mode for a wide range of load currents, but at the minimum load current it works in sub-threshold areas. The relations of the basic parameters in these two zones are shown on the next table.

Strong inversion	Sub-threshold
$I_{ds} = \frac{\mu_p C_{ox}}{2} \frac{W}{L} V_{ov}^2$	$I_{ds} \approx I_{D0} \frac{W}{L} e^{\frac{V_{gs}}{n V_T}}$
$g_m = \sqrt{2 \mu_p C_{ox} \frac{W}{L} I_{ds}} = \frac{2 I_{ds}}{V_{ov}}$	$g_m = \frac{I_{ds}}{n V_T}$

Table 3.1: Basic parameter versus the working areas of the power MOS.

All the parameters of the power MOS ac model change accordingly to the bias voltage. The formulas in table 3.1 are a good approximation, but usually it is better to catch this parameters from the "`DC Operating Points`", in *Cadence*.

Different technologies can improve some of the parameters (for example the capacitance of the ac model at all nodes or the product $\mu_p C_{ox}$) but the purpose of this work thesis is to use a cheap technology.

On the following subsections, we will model the transfer functions from the gate to the drain and from the source to the drain of the power MOS (corresponding to the blocks B and C).

3.2.1 Block B

In figures 3.3a and b it is shown the equivalent model of the power MOS that generally remains valid for the working areas of the power MOS. This block is useful in the analysis of the two loops.

Using the Kirchhoff's current law (KCL) at the node A and B of figure 3.3b, it is possible to obtain the first two equations while, using the superposition theorem, it is possible to

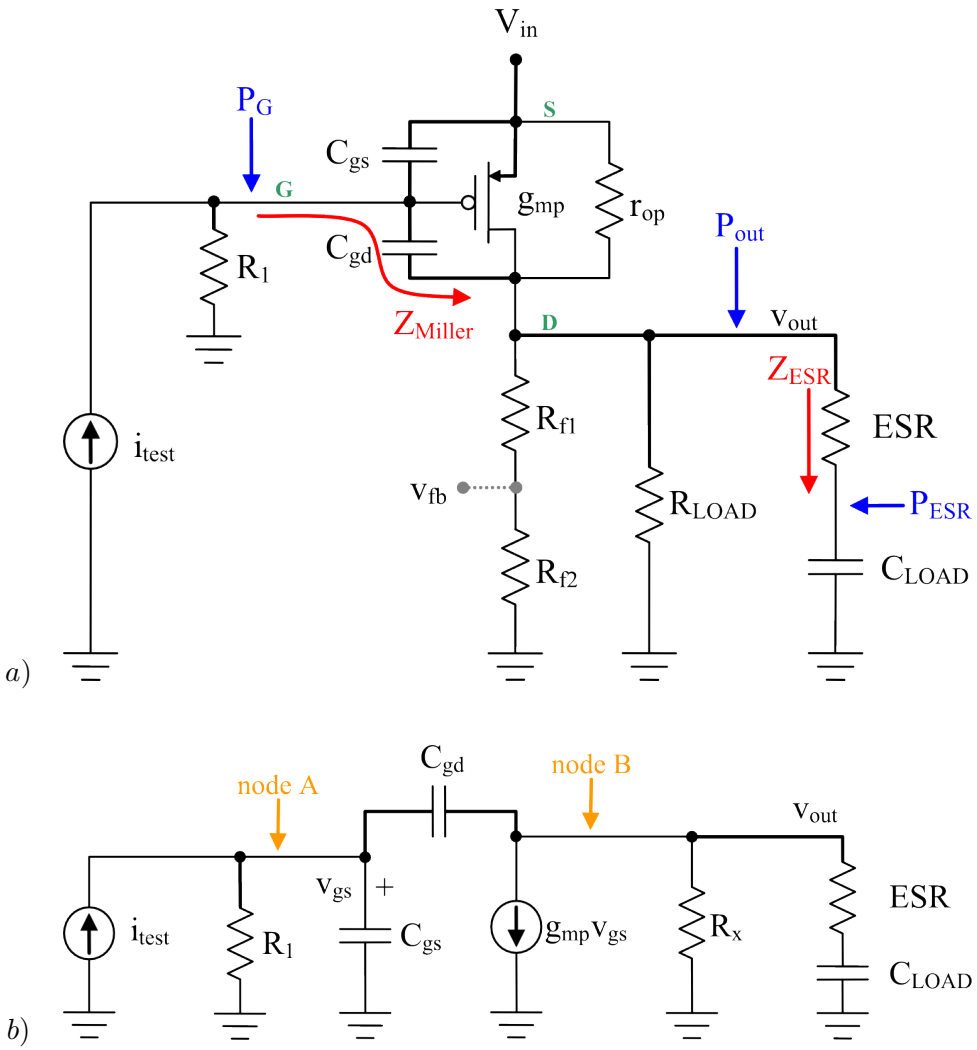


Figure 3.3: Power MOS, modelling of the block B: *a*) quasi ac model, *b*) equivalent ac model.

obtain the third one.

$$y_1 := \begin{cases} i_{test} - v_{gs}\,\frac{1}{Z_{in}} + i_{C_{gd}} = 0 \\ i_{C_{gd}} + g_{mp}\,v_{gs} + v_{out}\,\frac{1}{Z_{out}} = 0 \\ v_{gs} = R_1\,\frac{i_{in}+v_{out}\,s\,C_{gd}}{1+s\,R_1\,(C_{gs}+C_{gd})} \end{cases} \tag{3.5}$$

where

$$\begin{aligned} R_x &\triangleq R_{load}//\,(R_{f1}+R_{f2})\,//r_{op} \\ Z_{in} &\triangleq R_1//\tfrac{1}{s\,C_{gs}} = \tfrac{R_1}{1+s\,R_1\,C_{gs}} \\ Z_{out} &\triangleq R_x//\left(\mathrm{ESR}+\tfrac{1}{C_{load}}\right) = R_x\,\tfrac{1+s\,\mathrm{ESR}\,C_{load}}{1+s\,(R_x+\mathrm{ESR})\,C_{load}} \end{aligned} \tag{3.6}$$

After some steps, the system of linear equations y_1 gives:

$$\frac{v_{out}}{i_{test}} = \frac{-g_{mp}\,R_x\,R_1\,\left(1-s\frac{C_{gd}}{g_{mp}}\right)\,(1+s\,\mathrm{ESR}\,C_{load})}{a\,s^3+b\,s^2+c\,s+d} \tag{3.7}$$

where

$$\begin{aligned} a &= C_{gd}\,C_{gs}\,C_{load}\,\mathrm{ESR}\,R_1\,R_x \\ b &= C_{gs}\,C_{load}\,\mathrm{ESR}\,R_1 + C_{gd}\,C_{load}\,\mathrm{ESR}\,R_x + C_{gd}\,C_{gs}\,R_1\,R_x + C_{gd}\,C_{load}\,R_1\,R_x + \\ &\quad + C_{gs}\,C_{load}\,R_1\,R_x + C_{gd}\,C_{load}\,\mathrm{ESR}\,R_1\,(1+g_{mp}\,R_x) \\ c &= C_{load}\,\mathrm{ESR} + C_{gs}\,R_1 + C_{gd}\,R_x + C_{load}\,R_x + R_1\,C_{gd}\,(1+g_{mp}\,R_x) \\ d &= 1. \end{aligned} \tag{3.8}$$

It is possible to write the dominant pole approximation of equation 3.7 to highlight the three poles of the block B[1].

$$B \triangleq -\frac{v_{out}}{i_{test}} \approx \frac{g_{mp}\,R_x\,R_1\,\left(1-s\frac{C_{gd}}{g_{mp}}\right)\,(1+s\,\mathrm{ESR}\,C_{load})}{(1+s\,R_1\,C_G)\,(1+s\,(\mathrm{ESR}+R_x)\,C_{load})\,(1+s\,(\mathrm{ESR}//R_x)\,C_{load})} \tag{3.9}$$

where $C_G \triangleq C_{gs} + C_{gd}\,(1+g_{mp}\,R_x)$. Moreover, on the last equation is highlighted the typical DC gain of a common source configuration and the two zeros: the first one is created in the path through the C_{gd} and it is called Miller's zero, while the second one, is created from the equivalent series resistance ESR.

[1] As defined in equation 2.2, the block B is not an inverting stage.

From the preview equation, you can see that the Miller's zero is placed in the right hand plane, whereby it has a phase shift of $-90[deg]$. The insertion of a positive real part zero in a loop is the worse condition for the stability because it increases the bandwidth of the loop gain and shifts the phase of $-90[deg]$. Generally, a MOSFET in this configuration, with a low transconductance and little W, is not affected by this zero and for this reason it is usually neglected. In the literature this approximation is called *Miller approximation.* Unfortunately the big channel width W and transconductance g_{mp} increase the effect of this zero.

The zero created from the equivalent series resistance is located on the left hand complex-plane and generally has an natural frequency situated near the unity gain frequency of the total loop gain.

The natural frequencies of the poles and zeros of this block are:

$$\begin{aligned} f_{P_G} &= \tfrac{1}{2\,\pi\,R_1\,C_G} \\ f_{P_{out}} &= \tfrac{1}{2\,\pi\,(\mathrm{ESR}+R_x)\,C_{load}} \\ f_{P_{ESR}} &= \tfrac{1}{2\,\pi\,(\mathrm{ESR}//R_x)\,C_{load}} \\ f_{Z_{Miller}} &= \tfrac{g_{mp}}{2\,\pi\,C_{gd}} \\ f_{Z_{ESR}} &= \tfrac{1}{2\,\pi\,\mathrm{ESR}\,C_{load}}. \end{aligned} \tag{3.10}$$

In the figure 3.4 is shown the transfer function displayed by `LDO behavior`[2] that highlights the three poles and the two zeros just treated. The third pole P_{ESR} is at very high frequencies, in fact in this figure is out of scale.

3.2.2 Block C

In the figures 3.5a and b are shown the equivalent model of the power MOS that is useful in the characterization of the PSRR specification.

Using the Kirchhoff's current law (KCL) at the node A and B of the figure 3.5b, it is possible to obtain:

$$y_2 := \begin{cases} -\frac{v_g}{R_1} + (v_{test} - v_g)\; s\,C_{gs} + (v_{out} - v_g)\; s\,C_{gd} = 0 \\ (v_{out} - v_g)\; s\,C_{gd} + g_{mp}\,(v_g - v_{test}) + \frac{v_{out}-v_{test}}{r_{op}} + \frac{v_{out}}{Z_{out}} = 0 \end{cases} \tag{3.11}$$

[2]See the appendix B for more information about `LDO behavior` GUI.

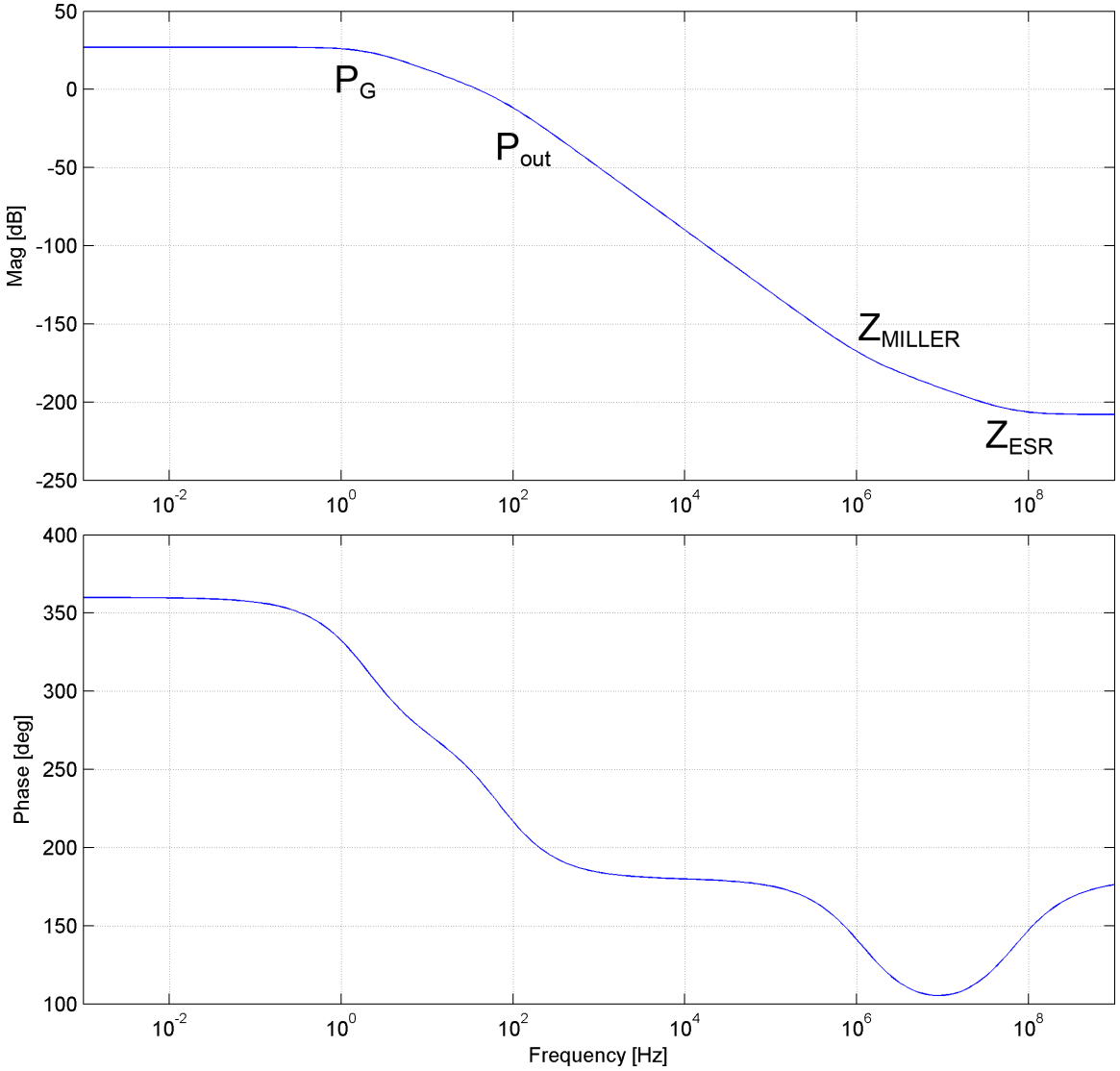


Figure 3.4: `LDO behavior` simulation: transfer function of the block B.

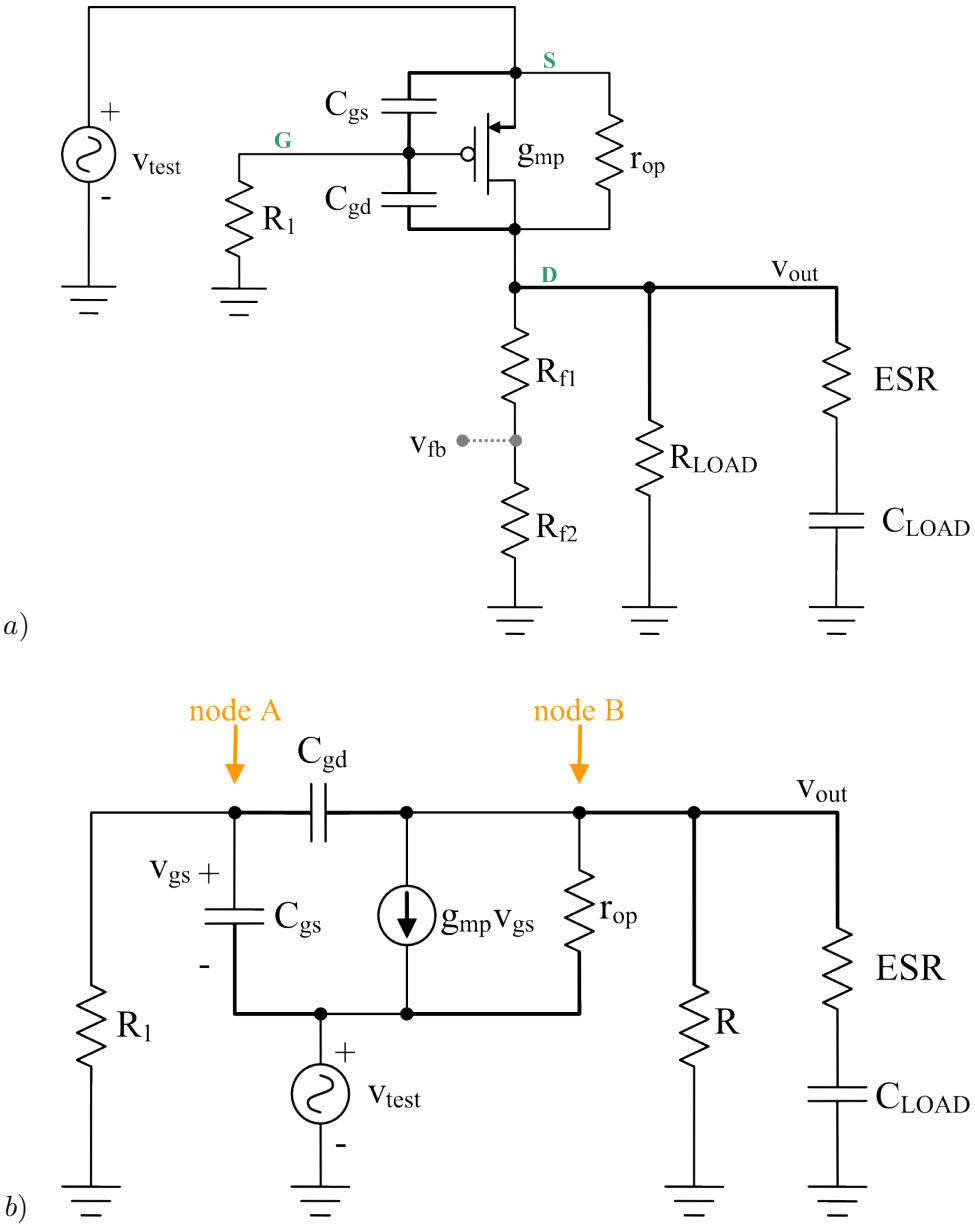


Figure 3.5: Power MOS, modelling of the block C: *a*) quasi ac model, *b*) equivalent ac model.

where

$$\begin{aligned} R &\triangleq R_{load} // (R_{f1} + R_{f2}) \\ R_x &\triangleq R // r_{op} \\ Z_{out} &\triangleq \left(\mathrm{ESR} + \tfrac{1}{s\,C_{load}}\right) // R = R \tfrac{1+s\,\mathrm{ESR}\,C_{load}}{1+s\,(R+\mathrm{ESR})\,C_{load}} \end{aligned} \tag{3.12}$$

Note that the linear system y_2 has two equations with three variables but we are interested on the ratio of these two. In fact the block C is defined as the ratio of v_{out} to v_{test}.

After some steps, the system of linear equations y_2 gives the following approximate result:

$$C \triangleq \frac{v_{out}}{v_{test}} \approx g_{mp}\,R_x \frac{(1+s\,\tau_{Z_1})\,(1+s\,\tau_{Z_2})\,(1+s\,\tau_{Z_{ESR}})}{(1+s\,\tau_{P_1})\,(1+s\,\tau_{P_2})\,(1+s\,\tau_{P_{ESR}})} \tag{3.13}$$

where the time constants of the poles and zeros are

$$\begin{aligned} \tau_{Z_1} &= \tfrac{R_1\left(C_{gs}+C_{gd}(1+g_{mp}\,r_{op})\right)}{1+g_{mp}\,r_{op}} \\ \tau_{Z_2} &= \tfrac{R_1\,r_{op}\,C_{gs}\,C_{gd}}{R_1\left(C_{gs}+C_{gd}(1+g_{mp}\,r_{op})\right)} \\ \tau_{Z_{ESR}} &= \mathrm{ESR}\,C_{load} \\ \tau_{P_1} &= R_1\,(C_{gs}+C_{gd}) + R_x\,(C_{load}+C_{gd}\,(1+g_{mp}\,R_1)) \\ \tau_{P_2} &= \tfrac{R_1\,R_x\,C_{load}\left(C_{gs}+C_{gd}\right)}{R_1\left(C_{gs}+C_{gd}\right)+R_x\left(C_{load}+C_{gd}\,(1+g_{mp}\,R_1)\right)} \\ \tau_{P_{ESR}} &= (\mathrm{ESR}//R_x)\;C_{load}. \end{aligned} \tag{3.14}$$

We assume that:

$$\begin{aligned} &C_{gs} << C_{gd}\,(1+g_{mp}\,r_{op}) \approx C_{gd}\,g_{mp}\,r_{op} \\ &R_1\,(C_{gs}+C_{gd}) >> R_x\,(C_{load}+C_{gd}\,(1+g_{mp}\,R_1)) \end{aligned} \tag{3.15}$$

then, the block C can be further approximated as follows:

$$C \approx g_{mp}\,R_x \frac{(1+s\,R_1\,C_{gd})\,\left(1+s\,\frac{C_{gs}}{g_{mp}}\right)\,(1+s\,\mathrm{ESR}\,C_{load})}{(1+s\,R_1\,(C_{gs}+C_{gd}))\,(1+s\,R_x\,C_{load})\,(1+s\,(\mathrm{ESR}//R_x)\,C_{load})}. \tag{3.16}$$

In figure 3.6 is shown the transfer function displayed by `LDO behavior` that highlights the three poles and zeros just treated. The third pole P_{ESR} is at very high frequencies, in fact in this figure is out of scale.

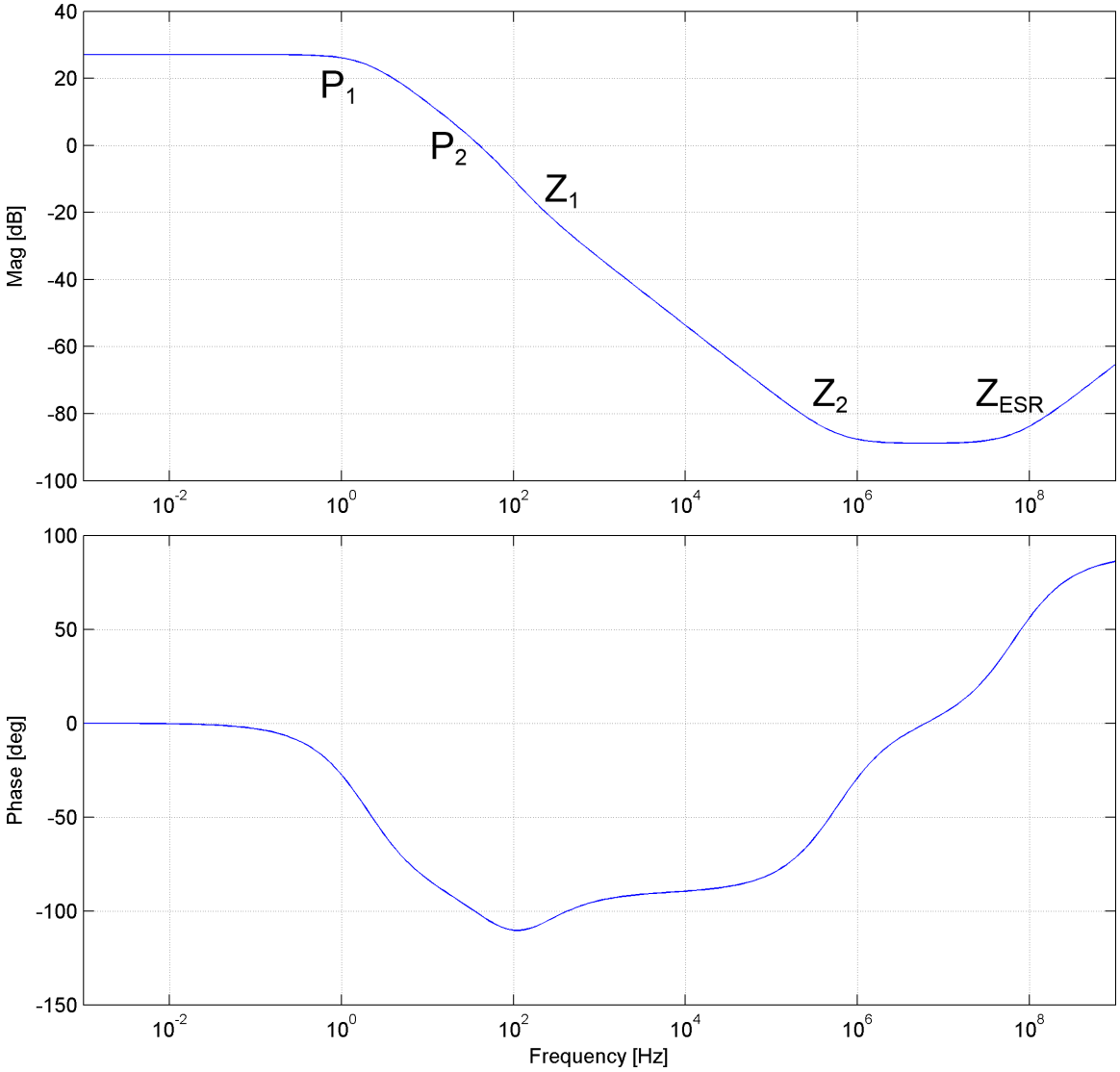


Figure 3.6: `LDO behavior`: transfer function of the block C.

3.3 Feedback network

The feedback network allows to sense the output voltage and provides a proportional signal of this voltage, at the input of the error amplifier. This block, previously called block H, is part of the main feedback. For modelling this block it is possible to consider the circuit of figure 3.7.

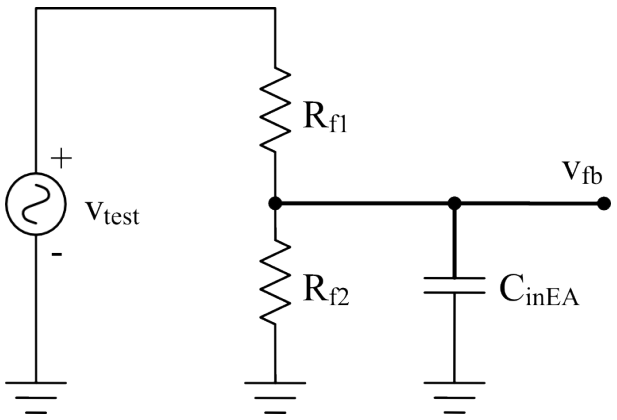


Figure 3.7: Ac model of the main feedback network of the regulator.

The transfer function that model this block is:

$$H = \frac{v_{fb}}{v_{test}} = \frac{R_{f2}}{R_{f1} + R_{f2}} \cdot \frac{1}{1 + s\ (R_{f1}//R_{f2})\ C_{inEA}} \tag{3.17}$$

where C_{inEA} is the equivalent capacitance that loads the output of the feedback network. Generally this capacitance creates a pole at high frequency that usually is neglected; therefore the block H is approximated as follows:

$$H \approx \frac{R_{f2}}{R_{f1} + R_{f2}}. \tag{3.18}$$

3.4 Differentiator

The differentiator is a block that can be realized in many ways; in this section two architectures are shown.

Ideally, the differentiator senses the output voltage of the regulator, and reacts with a proportional current. In the ideal realization of the figure 3.8, it is possible to obtain that

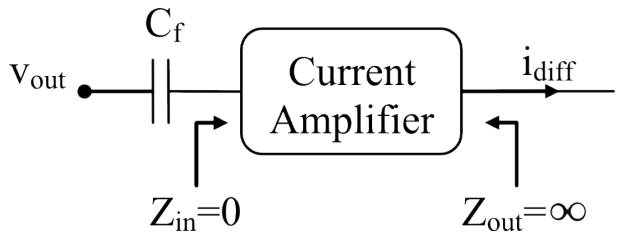


Figure 3.8: Ideal differentiator.

$i_{C_f} = v_{out}\, s\, C_f$ and $i_{diff} \triangleq A_i\, i_{C_f}$, whence it is possible to calculate the transfer function of this block as follows.

$$D_1 = \frac{i_{diff}}{v_{out}} = s\, A_i\, C_f. \tag{3.19}$$

To achieve a good compensation, with the pole splitting method, it is possible to use a big product $A_i\, C_f$. Generally if the current amplifier is realized with $A_i \approx 1$ i.e. is a current buffer, a big capacitance C_f should be required (on the order of nano Farads); this capacitor usually requires a big area that cannot be integrated on a chip. On the other hand it is difficult to realise a current amplifier with high gain for decreasing the capacitance.

It is important to note that the current amplifier realizes an unidirectional path from the output of the regulator to the gate of the power MOS. In fact the pole splitting compensation is realized by making the feedback network unidirectional to erase the effect of the real part zero, i.e the feed-forward path[3].

3.4.1 Passive differentiator

A possible realization of the differentiator is shown in figure 3.9, where it is used the cascade of a passive high pass filter and a transconductor[4]. This realization has this transfer

[3] In the literature [1] there are two solutions for erasing this effect:

- by making the feedback unidirectional
- by modifying the transfer function of the feedback network, moving the right hand zero to infinity (which means a null resistor).

The last solution uses a big capacitance C_f to achieve the stability.

[4] In figure 3.9b is highlighted the normalization of the sizes to realize the conversion into the logarithmic space. The notation adopted is the result of the fact that the argument of the logarithm is a pure number and for this reason a transconductance has to be normalised to 1 Siemens.

function:

$$D_2 = \frac{i_{diff}}{v_{out}} = g_D \frac{s\, R_f\, C_f}{1 + s\, R_f\, C_f}, \tag{3.20}$$

where g_D is a transconductance loaded on the equivalent resistance at the gate of the power MOS R_1. From equation 3.20 it emerges that increasing the product $R_f\, C_f$ the natural frequency of the pole decreases while the effect of the pole splitting increases. As explained

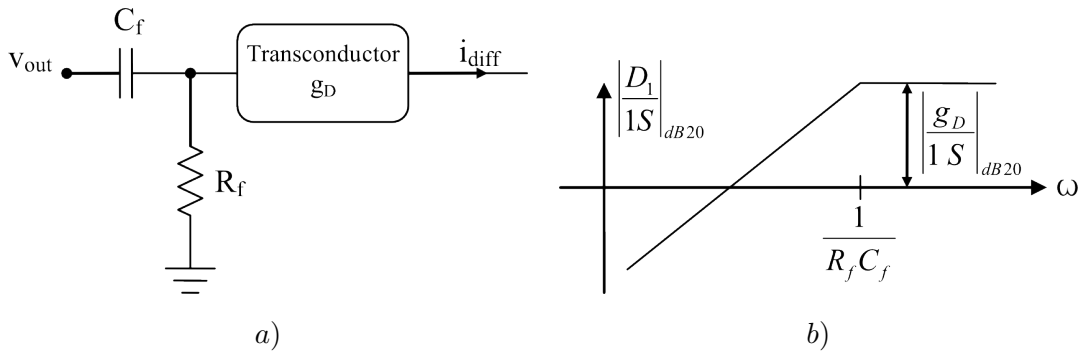


Figure 3.9: Passive differentiator: *a*) ideal circuit, *b*) transfer function.

in section 2, to achieve the stability of the regulator, it is required a high gain for this block, to realize a good pole splitting.

Generally, to hold the pole of the passive filter at high frequencies and realize a good pole splitting, it is required a high voltage gain $g_D R_1$. R_1 is not a parameter which can be manipulated while the transconductance depends on the square root of the bias current, which cannot increase so much. For these reasons, this type of differentiator can be only used in systems that require a low pole splitting to achieve the stability.

3.4.2 Active differentiator

The proposed differentiator is based on the circuit of the figure 3.10.

Using the Kirchhoff's current law (KCL) at the node A and B of figure 3.10b, it is possible to obtain the first two equations while, using the superposition theorem, it is possible to

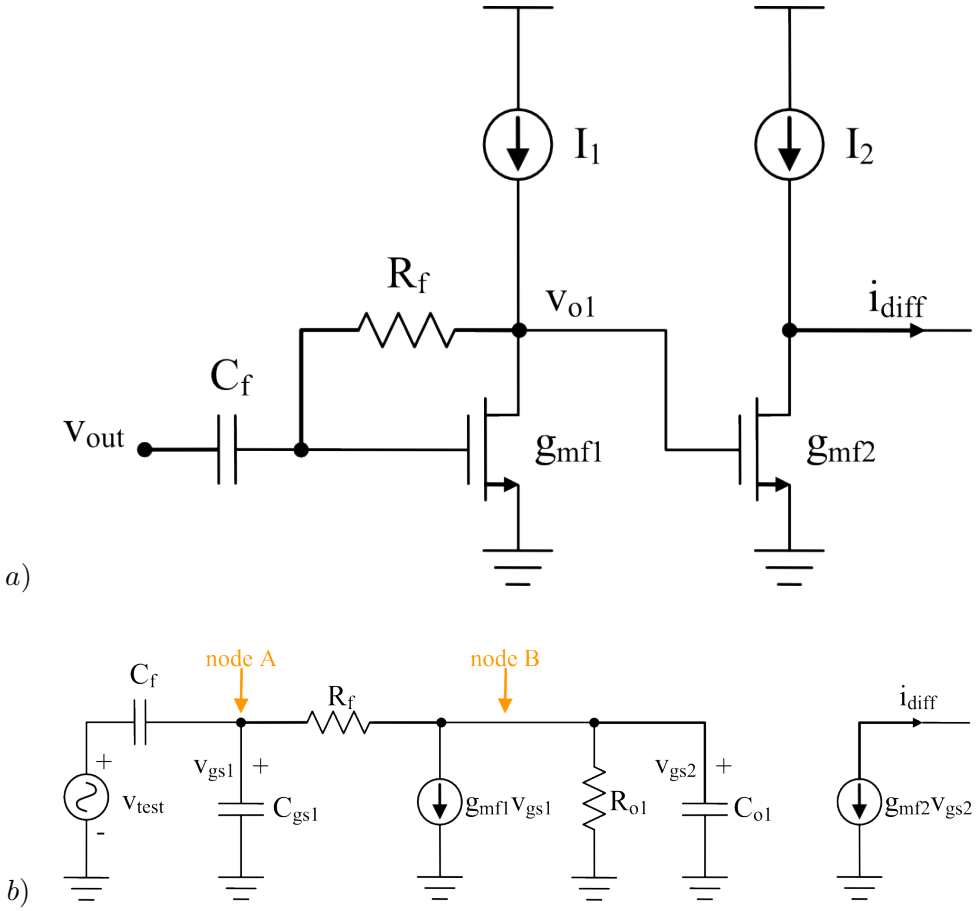


Figure 3.10: Active differentiator: *a*) base circuit, *b*) equivalent ac model.

obtain the third one.

$$y_3 := \begin{cases} (v_{test} - v_{gs1})\ s\,C_f - v_{gs1}\,s\,C_{gs1} + \frac{v_{gs2}-v_{gs1}}{R_f} = 0 \\ \frac{v_{gs2}-v_{gs1}}{R_f} + g_{mf1}\,v_{gs1} + \frac{v_{gs2}}{Z_o} = 0 \\ v_{gs1} = R_f\,\frac{v_{test}\,s\,C_f + \frac{v_{gs2}}{R_f}}{1+s\,R_f\,(C_f+C_{gs1})} \end{cases} \tag{3.21}$$

where

$$Z_o \triangleq R_o // \frac{1}{s\,C_o} = \frac{R_{o1}}{1 + s\,R_{o1}\,C_{o1}}. \tag{3.22}$$

As you can see, to not complicate the analysis of this block, the effect of C_{gd1} is neglected. After some steps, the system of linear equations y_3 gives:

$$D_3 = \frac{i_{diff}}{v_{test}} = \frac{s\,g_{mf2}\,R_{o1}\,C_f\ (R_f\,g_{mf1} - 1)}{a\,s^2 + b\,s + c} \tag{3.23}$$

where

$$\begin{aligned} a &= R_{o1}\,R_f\,C_{o1}\ (C_f + C_{gs1}) \\ b &= R_f\ (C_f + C_{gs1}) + R_{o1}\ (C_f + C_{gs1} + C_{o1}) \\ c &= g_{mf1}\,R_{o1} + 1. \end{aligned} \tag{3.24}$$

If the hypothesis of the dominant pole is assumed it is possible to obtain:

$$D_3 \approx \frac{s\,g_{mf2}\,R_{o1}\,C_f\ (R_f\,g_{mf1} - 1)}{\left(1 + s\frac{R_f\,(C_f+C_{gs1}) + R_{o1}\,(C_f+C_{gs1}+C_{o1})}{1+g_{mf1}\,R_{o1}}\right)\left(1 + s\frac{R_{o1}\,R_f\,C_{o1}(C_f+C_{gs1})}{R_f\,(C_f+C_{gs1}) + R_{o1}\,(C_f+C_{gs1}+C_{o1})}\right)} \tag{3.25}$$

Furthermore, if we assume that:

$$\begin{aligned} &g_{mf1}\,R_{o1} >> 1 \\ &C_f + C_{gs1} >> C_{o1} \end{aligned} \tag{3.26}$$

it is possible to write another approximation of equation 3.23 where the two poles of the block D are highlighted.

$$D_3 \approx \frac{s\,g_{mf2}\,g_{mf1}\,R_{o1}\,R_f\,C_f}{\left(1 + s\frac{(R_f+R_{o1})\,(C_f+C_{gs1})}{g_{mf1}\,R_{o1}}\right)\,(1 + s\,(R_f // R_{o1})\,C_{o1})} \tag{3.27}$$

The natural frequencies of the poles of this block are:

$$\begin{aligned} f_{P_1} &= \frac{g_{mf1}\, R_{o1}}{2\,\pi\left(R_f + R_{o1}\right)\left(C_f + C_{gs1}\right)} \\ f_{P_2} &= \frac{1}{2\,\pi\left(R_f // R_{o1}\right) C_{o1}}. \end{aligned} \tag{3.28}$$

In figure 3.11 is shown the proposed differentiator that is realized with two parallel paths; one of these with a p-MOS path while the other with a n-MOS path. This realization increases the circuit complexity but improves by a factor of 2 the DC gain (of the equations 3.25 and subsequent) and moreover allows to control the gate of the power MOS with a push-pull output.

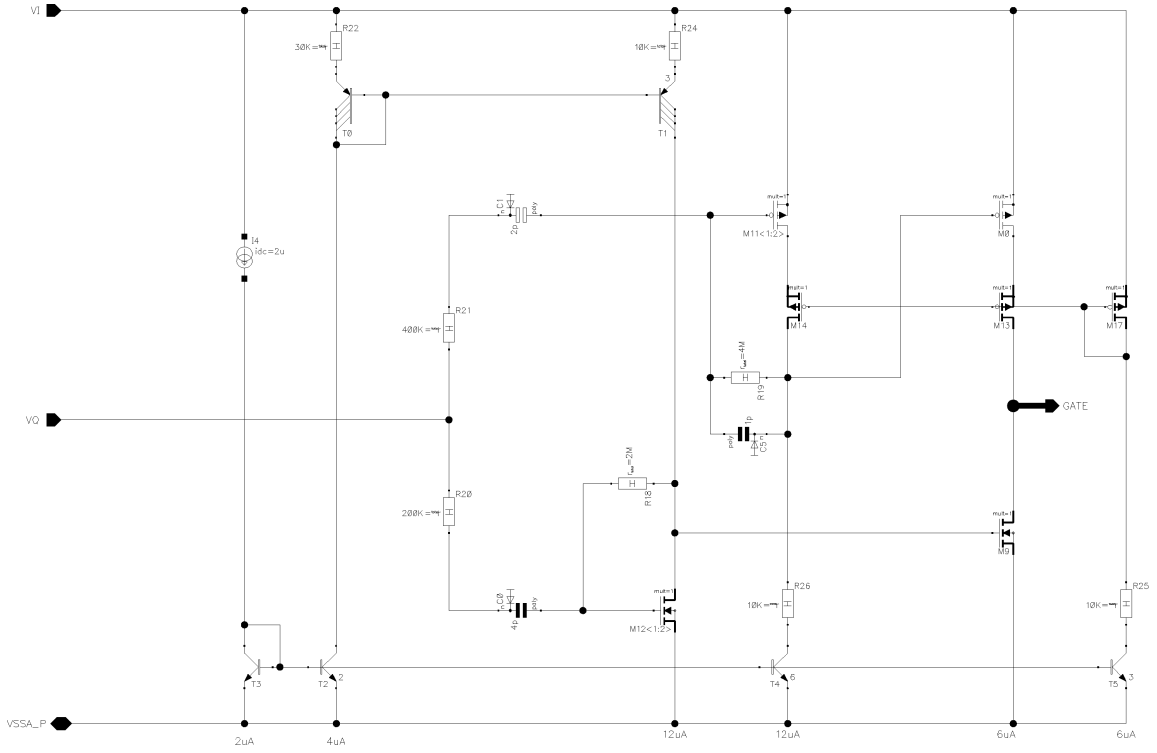


Figure 3.11: Proposed differentiator.

Chapter 4

Proposed LDO transistor-level design

In this chapter are explained the design criteria for the transistors of the realized LDO regulator and in the final part the simulations done with *Cadence* are shown.

4.1 Transistors Parameters

The essential parameters for the design of the transistors are V_{tn} $\mu_n C_{ox}$ for the n-MOS and V_{tp} $\mu_p C_{ox}$ for the p-MOS. These parameters were obtained by simulation of the circuit presented in figure 4.1, created for this purpose. The transistors MOS operate in the saturation region: in fact they are in diode configuration with a DC current source bias.

The parameters values cannot be presented for industrial security; the only information which is possible to report is that the components belong to Infineon Technologies.

4.2 Schematic Design

In this subsection are presented the design criteria for the sizing of all the regulator blocks. As a first step, the circuit has been realized with *Cadence* using the proposed technology; then, when the steady-state is reached (i.e. when the DC output voltage is that expected), it is possible to catch from the simulation results all the parameters of the power MOS ac model.

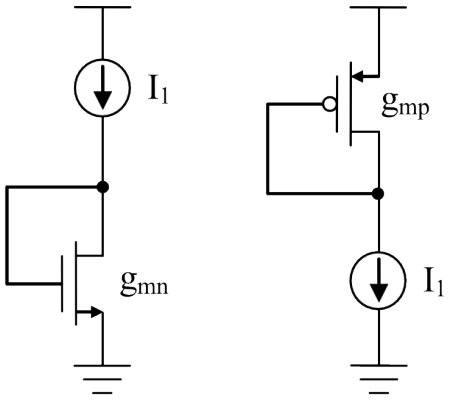


Figure 4.1: Circuit used to obtain the transistor parameters.

After this, the design of the regulator can be done using the `LDO behavior` GUI that has a good match between its results and those obtained with *Cadence*. Therefore, it is possible to know how the ideal performance can be reached with the power MOS used. For this reason the sizing of the four blocks described in chapter 3 begins from the characteristic parameters: the transconductance, the over-drive voltage or the bias current of the transistor MOS.

Generally if the gain of the differentiator is not high, i.e. the differentiator gain is not able to realize a good pole splitting, then the less stable case of the external loop is at the minimum current load. On the other hand, the worst case of the nested loop stability generally does not correspond to the previous condition. For these reasons it is better to design (with `LDO behavior`) firstly the nested loop, to ensure a minimum phase margin at its worst case (for example $> 45[deg]$) and then the external loop when the regulator is at the minimum current load.

As shown in table 2.3, the maximum ground current is a design target. For this reason it was decided in advance how much current had to be devoted to each block (table 4.1). With this budget is thought to reach a good DC gain in the error amplifier, to ensure that the power MOS does not work in sub-threshold zone and finally to ensure the bandwidth at the differentiator.

Block	Current devoted
Error Amplifier	$30[\mu A]$
Power MOS	$20[\mu A]$
Differentiator	$40[\mu A]$

Table 4.1: LDO current specification.

4.2.1 Error Amplifier

In figure 3.2 is shown the proposed error amplifier that can be sized starting from the placing of the internal pole and then, from the achievement of the total transconductance (defined on the equation 3.3).

The first stage is designed by sizing the tail current source of the differential pair. In fact with the increase of this current the equivalent resistance at the output of this stage decreases, as shown in equation 4.1.

$$r_o = \frac{\eta_{n(p)}\, L}{I_{ds}} \tag{4.1}$$

This causes the internal pole of the error amplifier to increase (equation 4.2). The purpose of this sizing is to put this pole at a bigger frequency than the bandwidth of the system GBW.

$$\omega_{P_{int}} = \frac{\frac{I_{tail}}{2}}{\left[(\eta_n\, L_4)\,//\,(\eta_p\, L_2)\right]\, C_x} \tag{4.2}$$

The second stage can be sized starting from the DC total transconductance A_{DC} set in `LDO behavior` as shown in the following equation:

$$g_{m5} = \frac{A_{DC}}{g_{m2}\,(r_{o2}//r_{o4}) - R_s\, A_{DC}}. \tag{4.3}$$

Now it is possible to find the aspect ratio of M_5 imposing the bias current provided by the transistor T_2 as follows:

$$g_{m5} = \sqrt{2\,\mu_n\, C_{ox}\, \frac{W_5}{L_5}\, I_{T_2}}. \tag{4.4}$$

This current is chosen by finding the trade-off between the output resistance, that should be big, and the charge-time of the power MOS capacitance C_G, that should be small.

The output resistance is very important because it is a part that composes the equivalent resistance at the gate of the power MOS $R_1 \triangleq R_{outEA}//R_{outDIFF}$. R_{outEA} is defined as follows:

$$R_{outEA} \approx [r_{o5}\,(1 + g_{m5}\,R_s)]\,//\,[r_{oT2}\,(1 + g_{mT2}\,R_{21})]\,. \tag{4.5}$$

To increase R_{outEA}, it is possible to act in two ways:

- using the source (emitter) degeneration resistances R_s and R_{21},
- minimising the bias current.

Using the first way, it is important ensure that the voltage headroom of the error amplifier output includes the voltage V_{gs} swept by the change of the load current.

Using the second way, it is important not to minimize the bias current that flows through the output stage of the error amplifier because it limits the maximum ac current that could charge the gate capacitance C_G; this effect could be seen at the switch-on of the regulator when the error amplifier charges the gate capacitance with a constant current. With the next equation it is possible to find the required time Δt to realize a linear variation of the voltage ΔV with a constant current I_{EA}.

$$i_{EA}(t) = C_G \frac{dv_t}{dt} \qquad \Rightarrow \qquad \Delta t = \frac{C_G\,\Delta V}{I_{EA}}. \tag{4.6}$$

4.2.2 Power MOS

For the sizing of the power MOS the specifications from which it is possible to start are the maximum current and the drop-out voltage.

It is possible to put the power MOS as shown in figure 4.2 and provide the gate voltage V_G that allows to reach the required drop-out voltage. The variables μ_p (hole mobility), and C_{ox} (gate capacitance per unit area), are device technology parameters and are obtained by simulation of the circuit 4.1 while, the threshold voltage can be catch from the "`DC Operating Points`", in *Cadence*. Using equations 4.7 and 4.8 it is possible to size the power MOS:

$$I_{DMAX} = \frac{\mu_p\,C_{ox}}{2}\,\frac{W}{L}\,(V_{gs} - V_{tp})^2 \qquad \Rightarrow \qquad W = \frac{I_{DMAX}\,L}{\frac{\mu_p\,C_{ox}}{2}\,(V_{gs} - V_{tp})^2} \tag{4.7}$$

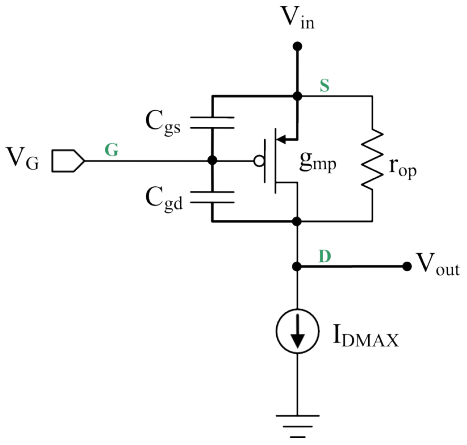


Figure 4.2: Pass transistor design.

$$V_{drop-out}\big|_{min} = V_{ov} = V_{gs} - V_{tp} \tag{4.8}$$

where I_{DMAX} is the maximum output current. Generally the minimum channel length available to minimise the channel weight is used.

To get the r_{op} resistance we can use the definition:

$$r_{op} \triangleq \frac{dV_{ds}}{dI_{ds}}. \tag{4.9}$$

If the power MOS works in saturation zone [1] it is possible rewrite it as:

$$r_{op} = \frac{\eta_p L}{I_{ds}}. \tag{4.10}$$

There are some ways to obtain the value of this parameter:

- from the current voltage characteristic V_{ds}/I_{ds} (with the gate voltage fixed), using the definition of equation 4.9,
- by testing the circuit of figure 4.3. In fact the DC point is equal to the circuit without the switch and the current source, but the ac analysis highlights the r_{op} parameter using the equation 4.11.

$$r_{op} = \frac{v_{test}}{i_{ac}} \tag{4.11}$$

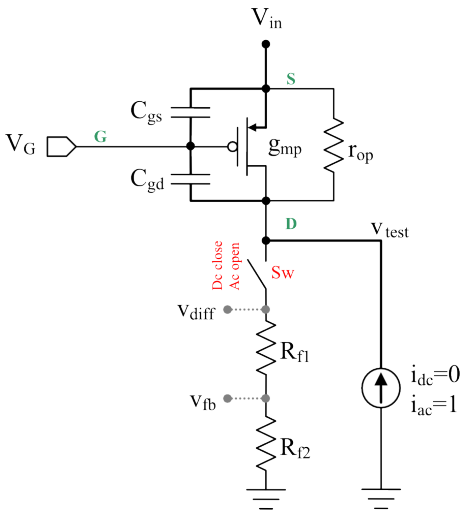


Figure 4.3: Circuit used for obtain the r_{op} parameter.

The effective pass transistor gate capacitance C_G is mainly composed by three addends (see figure 2.3):

- C_{gs},
- the contribution of the Miller effect on C_{gd} (varying with load conditions),
- the contribution of the nested loop contributes on C_f (varying with load conditions).

On the next equation is shown this three addends.

$$\begin{aligned} C_G &= C_{gs} + C_{gd}\,(1 + g_{mp}\,R_x) + C_f\,(A_i\,g_{mp}\,R_x) \\ &\approx C_f\,(A_i\,g_{mp}\,R_x) \end{aligned} \tag{4.12}$$

Generally, for the regulator, there are two types of load (as shown in the figure 4.4a and b) that affect the external pole:

- resistive,
- active realized with a current source.

The pass transistor output resistance is formed from the parallel combination of the feedback resistors $(R_{f1} + R_{f2})$, the transistor output resistance r_{op} and the load resistance. The

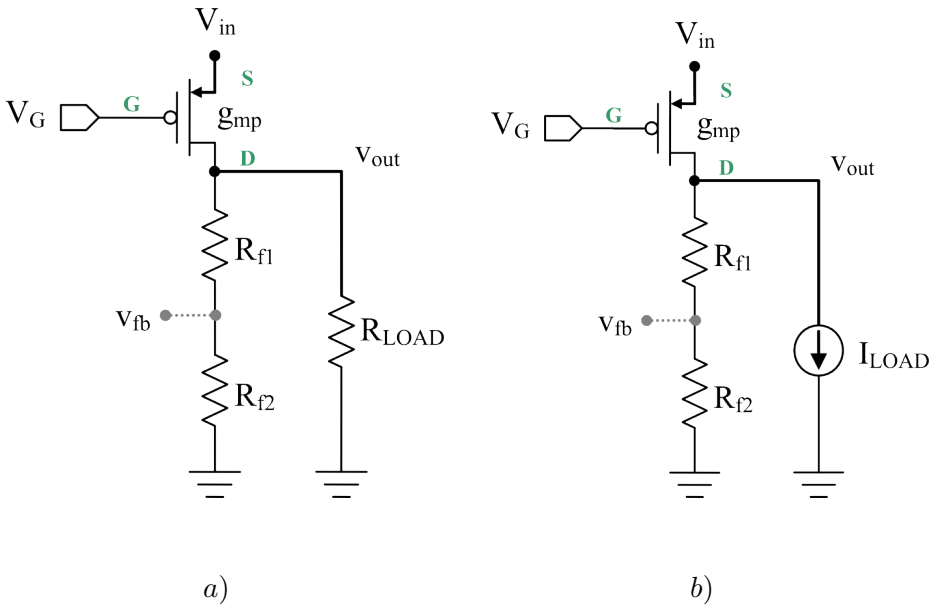


Figure 4.4: The types of load: *a*) resistive, *b*) active.

output resistance of a current source generator is infinite. For this reason, the resistive-load decreases the output impedance with respect to the active-load, and pushes the output pole to higher frequencies. Usually it is recommended to use the resistive-load in the ac analysis and the active-load in the transient one.

Pass transistor sub-threshold operation is another major concern. For the large variations of the load current, the p-MOS transistor will undergo a transition from the saturation region to the sub-threshold region. The pass transistor exhibits an exponential relationship while operating in sub-threshold in contrast to the nominal square law relationship. The relationship is shown in the equation 4.13.

$$I_{ds} \approx I_{D0} \frac{W}{L} e^{\frac{V_{gs}}{n V_T}} \tag{4.13}$$

Sub-threshold operation produces a significantly slower response [1]. This may cause a significant degradation in the voltage regulation for applications where the load current drops to low current levels in a short span of time. This degradation in load regulation can only be counteracted by providing more current to the LDO, improving the speed of the circuit. This is especially true during sub-threshold operation.

The pass transistor constitutes the only fixed predetermined regulator component. The

other components, i.e. the error amplifier, feedback network and the differentiator compensation network, are modelled around the fixed pass transistor.

4.2.3 Feedback network

The feedback network can be sized by starting from the quiescent current[1] of the power MOS $I_{Q,pass}$, the voltage reference of the band-gap V_{ref} and the output voltage of the regulator V_{out}. In equation 4.14 is shown the relationship of the resistance R_{f1} and R_{f2}.

$$\begin{aligned} R_{f1} &= \frac{V_{out}-V_{ref}}{I_{Q,pass}} \\ R_{f2} &= \frac{V_{ref}}{I_{Q,pass}} \end{aligned} \tag{4.14}$$

4.2.4 Differentiator

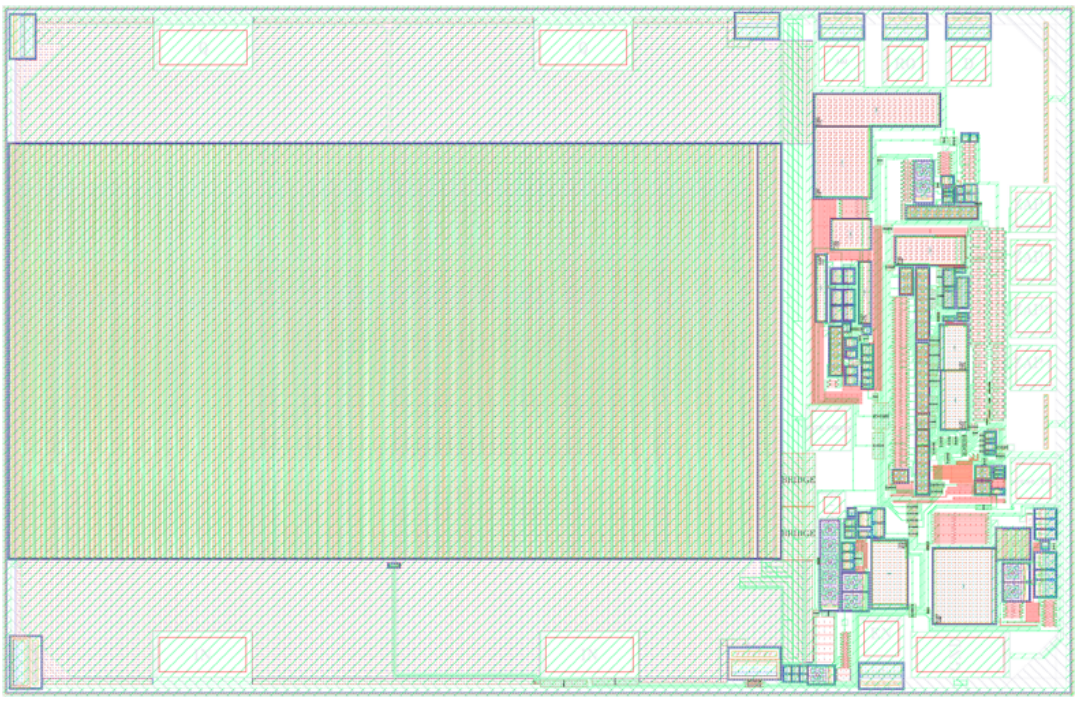
In figure 3.11 is shown the proposed differentiator that can be sized starting from the transconductance of the first stage and the second stage provided with the `LDO behavior` analysis. This block is the most important for the stability; in fact, as shown in the previous chapters, it could have a good gain and bandwidth. `LDO behavior` is an easy way to understand where the poles are located.

4.3 Layout

The layout of the realised circuit is shown in figure 4.5a while in figure 4.5b are highlighted the blocks analysed and designed in this work thesis. The total area of the chip is about $1.1[mm^2]$, where the 75% of it is taken by the power MOS.

[1] The quiescent current of the power MOS $I_{Q,pass}$ is defined as the minimum current that flows through the power MOS when the pass device is loaded with the resistor divider $R_{f1} + R_{f2}$.

a)



b)

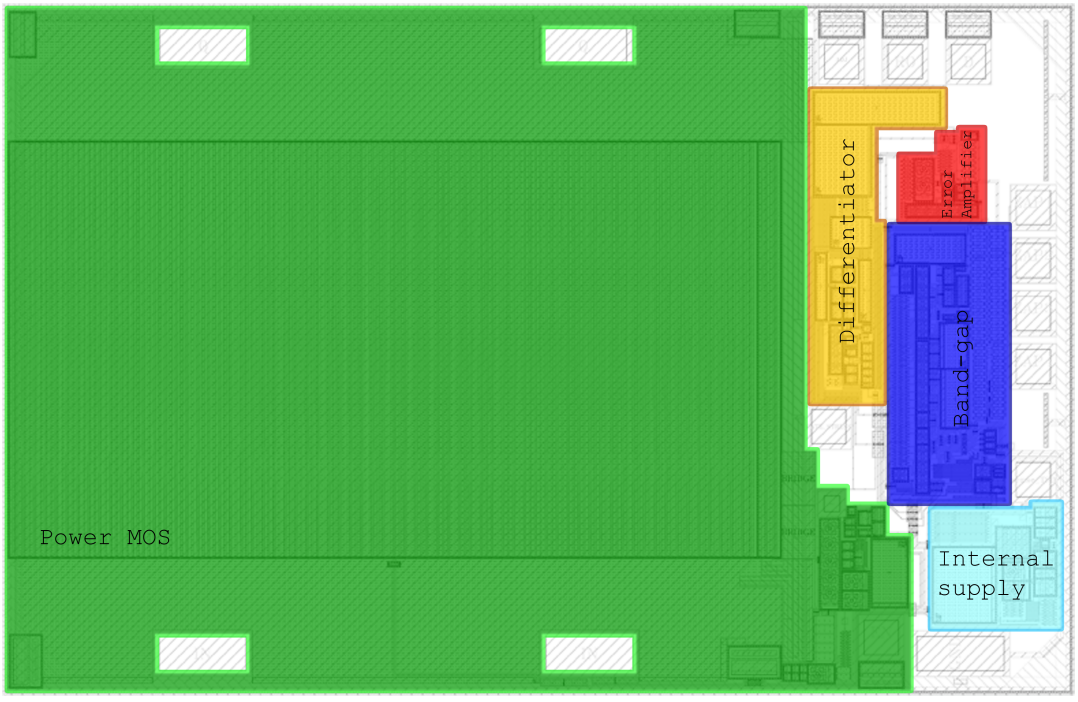


Figure 4.5: The layout-level of the proposed circuit *a)* and the highlighted blocks *b)*.

4.4 Transistor-level simulations

The design of the LDO voltage regulator aims to meet several initial parameters. The simulations are divided by type of parameter, namely loop gains ac response, steady-state parameters, dynamic state parameters, and high frequency parameters.

4.4.1 Loops gains ac response

The loop gains of the LDO voltage regulator at the transistor-level are shown in figure 4.6 for the total loop gain and in figure 4.7 for the nested loop gain.

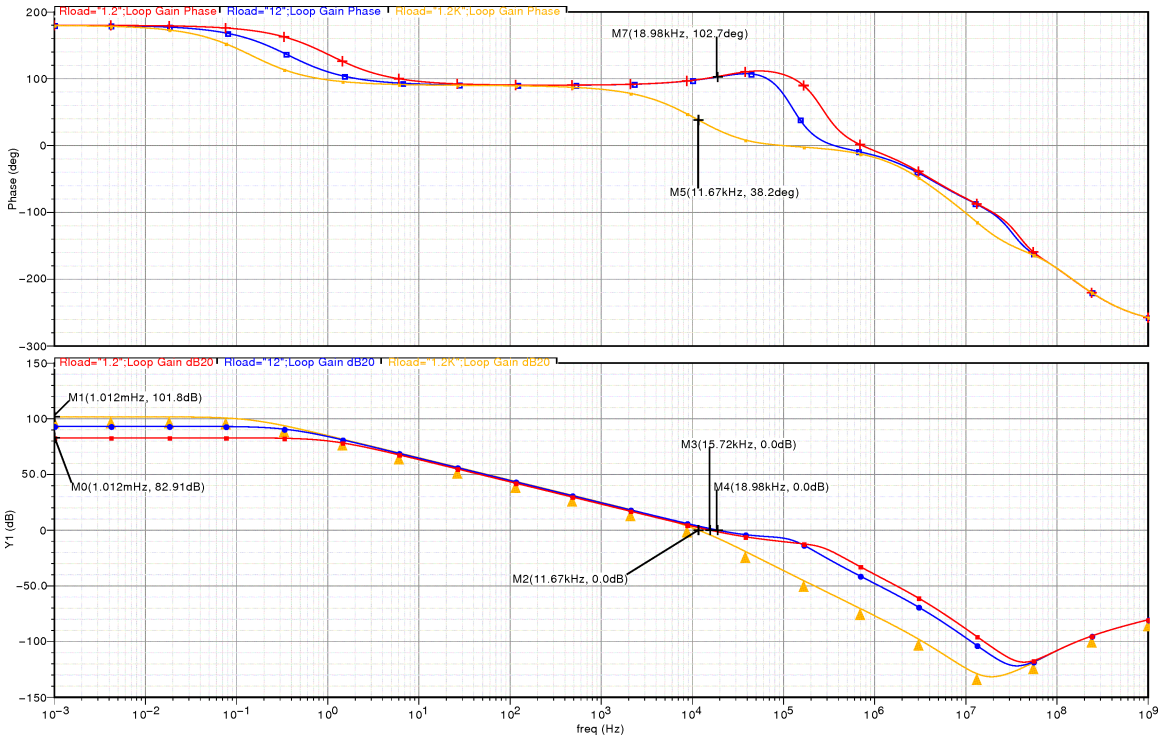


Figure 4.6: *Cadence* simulation: total loop gain versus R_{load}; the red line is with the maximum current ($1[A]$), the blue line is with $100[mA]$ and the yellow line is with $1[mA]$.

The DC gain of the total loop resides at roughly $82.91[dB]$ at high output currents while at roughly $101.8[dB]$ at low output currents. As shown in figure 4.6, the phase margin with the values of the current load between $1[A]$ to $1[mA]$ varies from $102.7[deg]$ to $38.2[deg]$

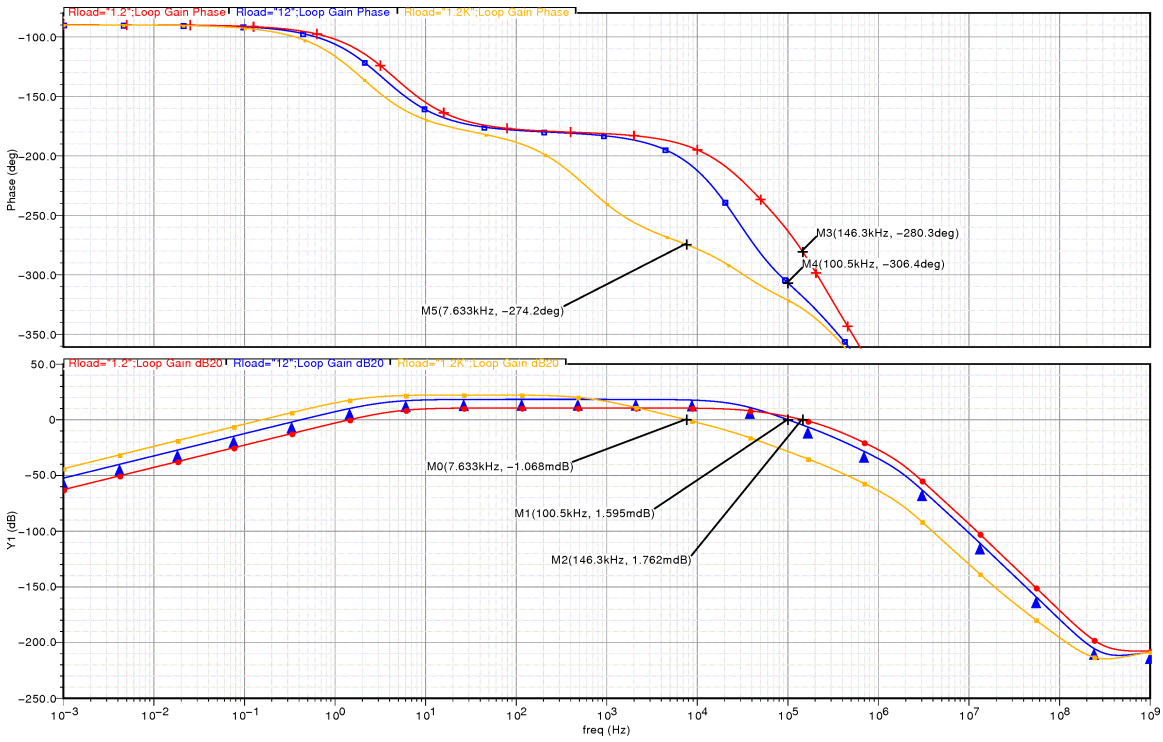


Figure 4.7: *Cadence* simulation: nested loop gain versus R_{load}; the red line is with the maximum current ($1[A]$), the blue line is with $100[mA]$ and the yellow line is with $1[mA]$.

respectively. When the current load decreases under $1[mA]$, the phase margin drops near $7[deg]$.

As shown in figure 4.7 the minimum phase margin of the nested loop does not correspond to the worst current load case of the total loop.

4.4.2 Steady-state Parameters

The steady-state parameters define the LDO's static state conditions. As explained in section 1.4.1, there are two important characteristics that define the steady-state LDO parameters, the **line regulation** and the **load regulation**.

The **line regulation** is the measurement of the steady-state output voltage and it was simulated with the change of the input voltage from $2[V]$ to $5[V]$ at the minimum output current. The results is shown in figure 4.8.

Like the line regulation, the **load regulation** measures the steady-state output voltage. This time, however, the input voltage is fixed to $5[V]$ and the output current was varied from $0[A]$ to the full load condition $1[A]$. The figure 4.9 shows the simulation results.

A higher DC voltage gain at the zero load condition improves the line and load regulation but at the expense of AC stability [4].

The **drop-out voltage** of the regulator is the difference between the battery and the output voltages and it was measured providing a fixed $V_{gs} = 2.7[V]$[2] in two load current conditions, at the maximum and 80% current load. In figure 4.10 it is possible to see the linear variation of the battery voltage (blue line), the output voltages (red line) and the current that throwing in the power MOS.

The **quiescent current** I_{GND} plotted as a function of the load current is almost constant (figure 4.11).

[2]This DC voltage is the maximum V_{gs} that the output of the error amplifier can achieve; with this polarization the power MOS is in drop-out condition.

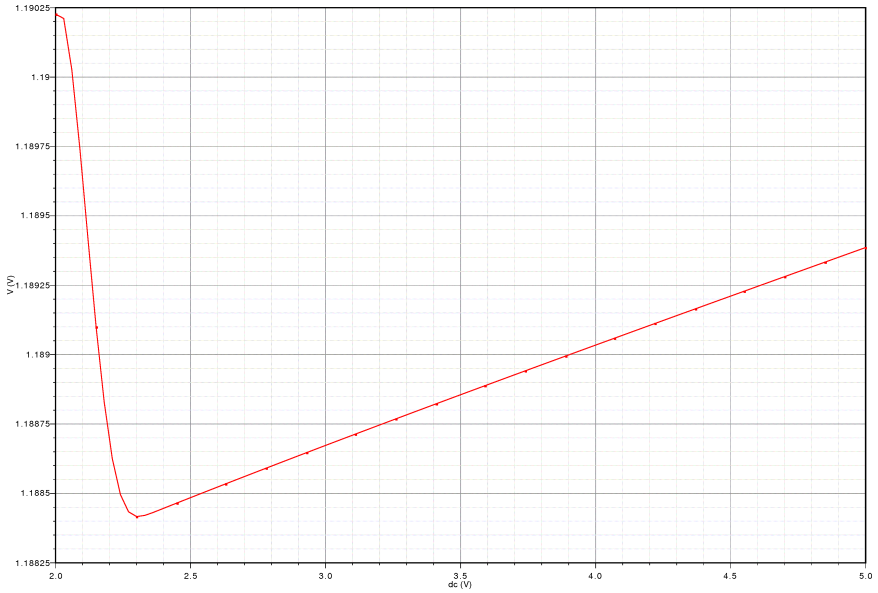


Figure 4.8: *Cadence* simulation: line regulation.

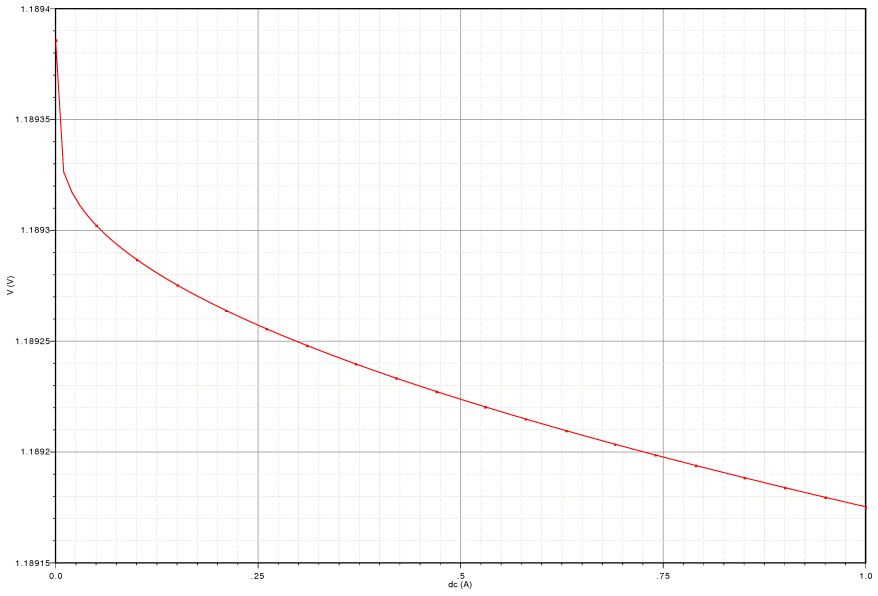


Figure 4.9: *Cadence* simulation: load regulation.

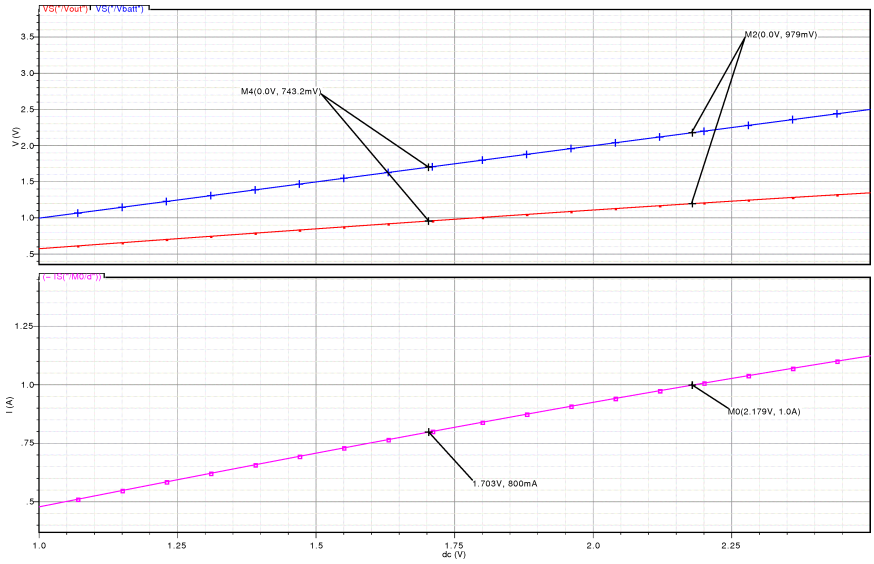


Figure 4.10: *Cadence* simulation: drop-out voltage at two load current conditions.

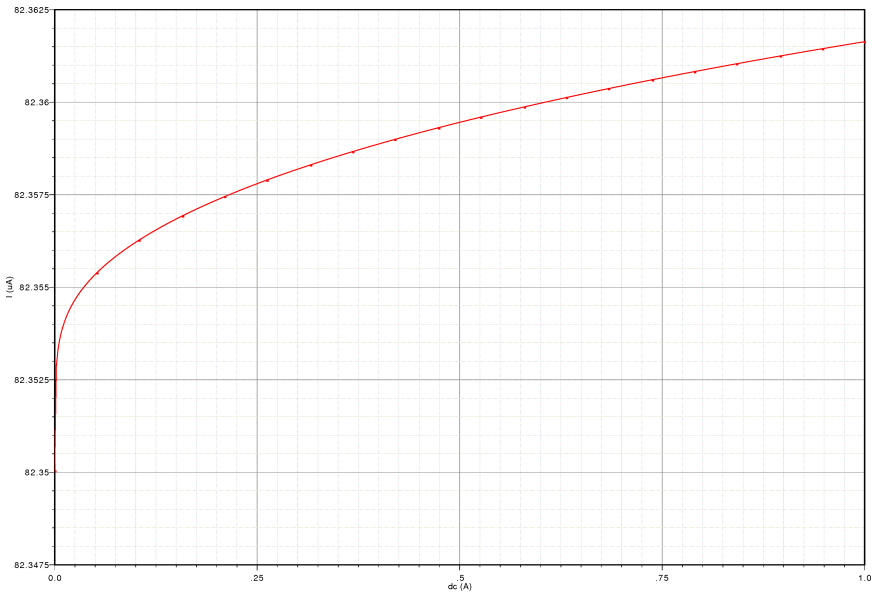


Figure 4.11: *Cadence* simulation: quiescent current plotted as a function of the load current.

4.4.3 Dynamic-state Parameters

The LDO regulator dynamic response was simulated for both load regulation and line regulation as well as the turn-on settling time.

The **line regulation dynamic response** was simulated at different load conditions: $R_{load} = 1.2[\Omega]$ and $R_{load} = 1.2[k\Omega]$, are shown in figures 4.12a and b respectively. The blue line is the battery voltage v_{in} while the yellow and red lines are the output voltage of the regulator with and without differentiator respectively. As it can be seen, in both figures 4.12a and b, the first part of the response is affected by the charge of the gate capacitance. In fact this capacitance is charged with constant current $i_G \triangleq i_{EA} + i_{diff}$ that generally, if there is not a quick variation at the output of the regulator, can be approximated as $i_G \approx i_{EA}$.

On the second part of the response the regulator reaches the DC steady-state in a different way. In fact using the differentiator increases the response speed and provides a convergence with minor fluctuations, i.e. increases the phase margin at a lower load current, as shown in figure 4.12b.

The **load regulation dynamic response** is shown in figure 4.13 where the blue line is the load current while the magenta and red lines are the output voltage of the regulator with and without differentiator, respectively.

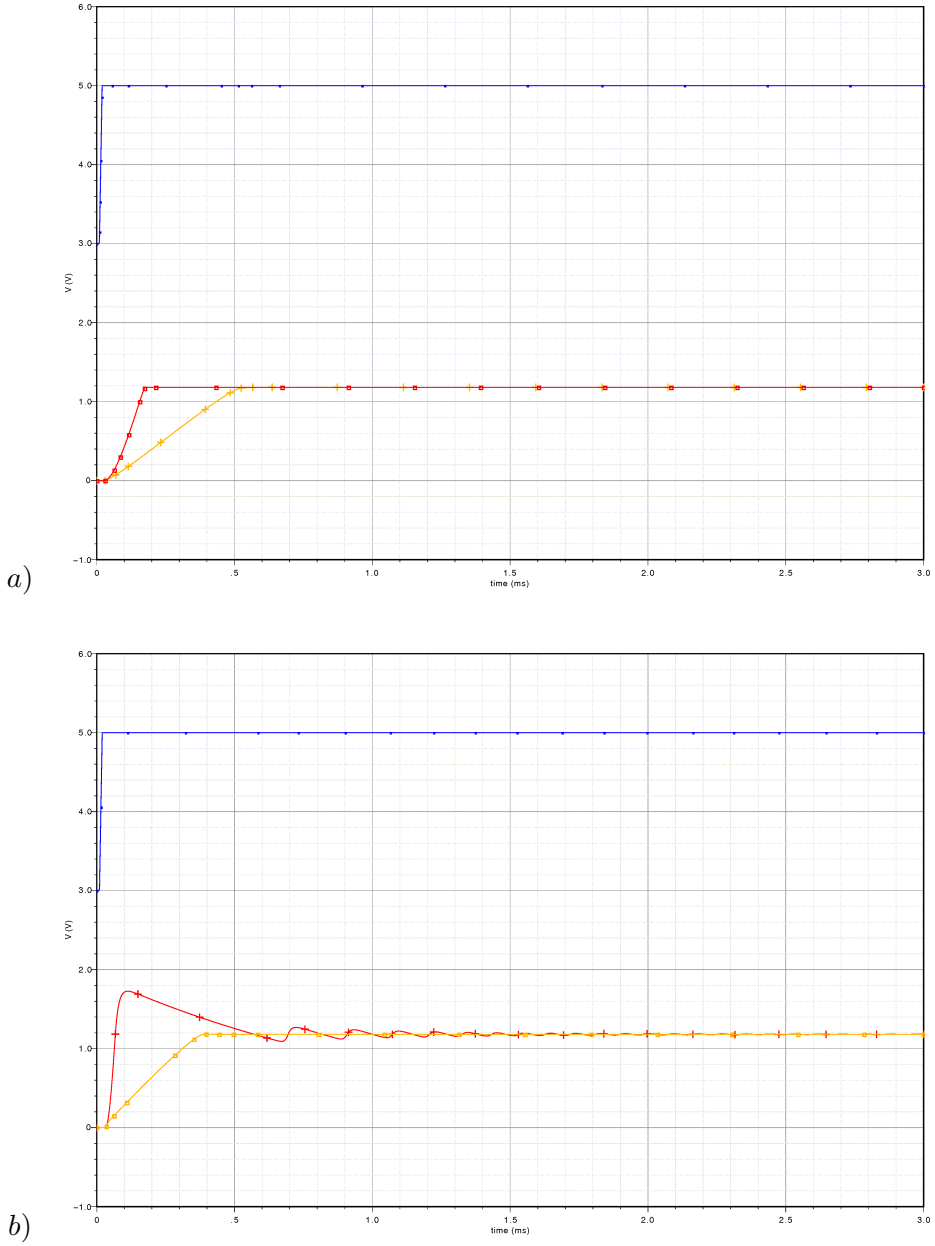


Figure 4.12: *Cadence* simulation: line regulation dynamic response with $a)$ $R_{load} = 1.2[\Omega]$ and $b)$ $R_{load} = 1.2[k\Omega]$. The blue line is the battery voltage V_{in} while the yellow and red lines are the output voltage of the regulator with and without differentiator respectively.

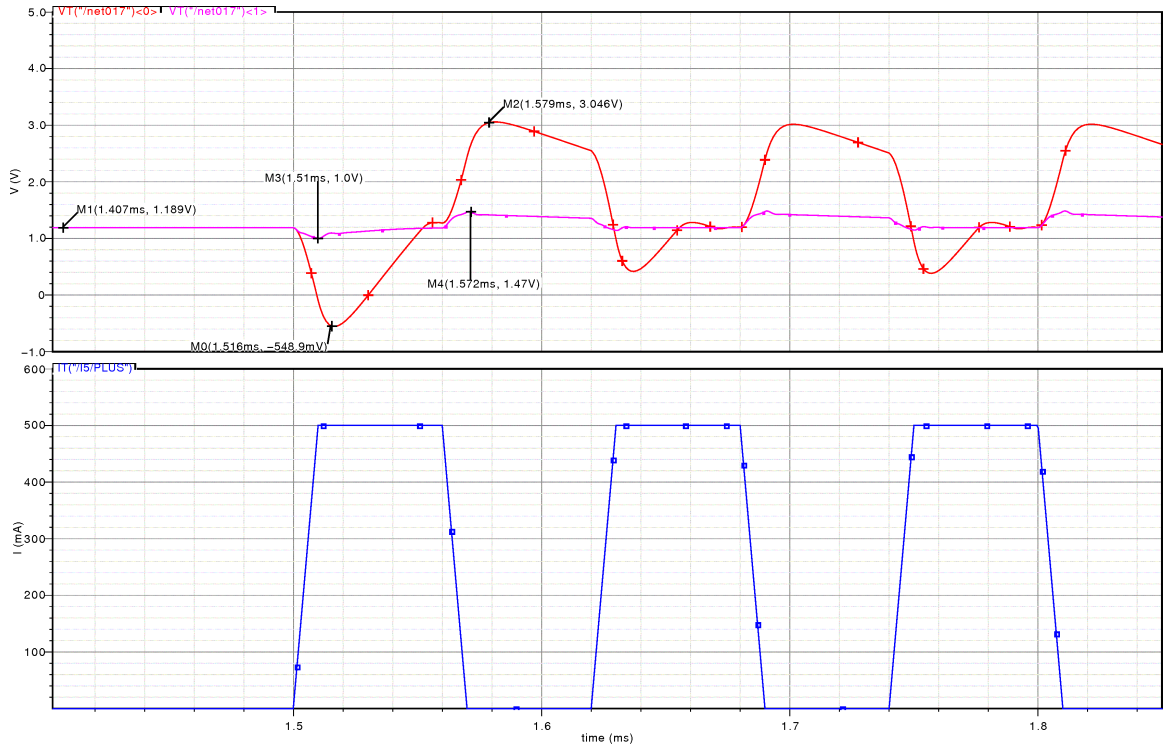


Figure 4.13: *Cadence* simulation: load regulation dynamic response. The blue line is the load current while the magenta and red lines are the output voltage of the regulator with and without differentiator, respectively.

4.4.4 High Frequency Parameters

The final set of measurements are the **equivalent output-regulator noise** and the **PSRR**.

The **equivalent output noise** was measured in closed-loop for different static output load conditions as shown in figure 4.14. The low-frequency noise component is influenced

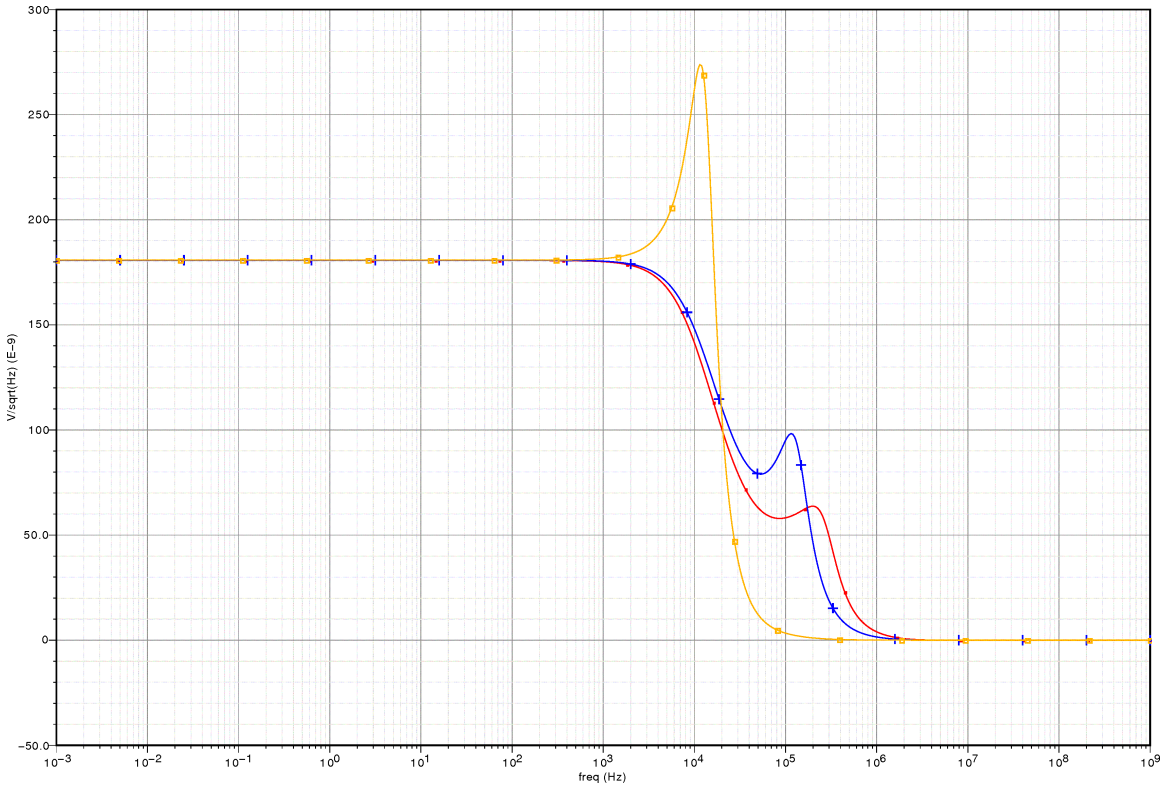


Figure 4.14: *Cadence* simulation: the equivalent output-regulator noise for the different load resistance conditions; $R_{load} = 1.2[k\Omega]$ yellow line, $R_{load} = 12[\Omega]$ blue line, $R_{load} = 1.2[\Omega]$ red line.

by the DC loop gain and the output impedance [4]. When the output impedance decreases, the output equivalent noise is reduced. The noise is then filtered at high frequencies by the output pole.

Power-supply-rejection-ratio (PSRR) defines the regulator ability to reject small-signal, high-frequency noise from the input line to the output voltage node. The voltage regulator's PSRR was measured in closed-loop for various static state current conditions (figure 4.15). The PSRR is a parameter that differs in the `LDO behavior` model. This is

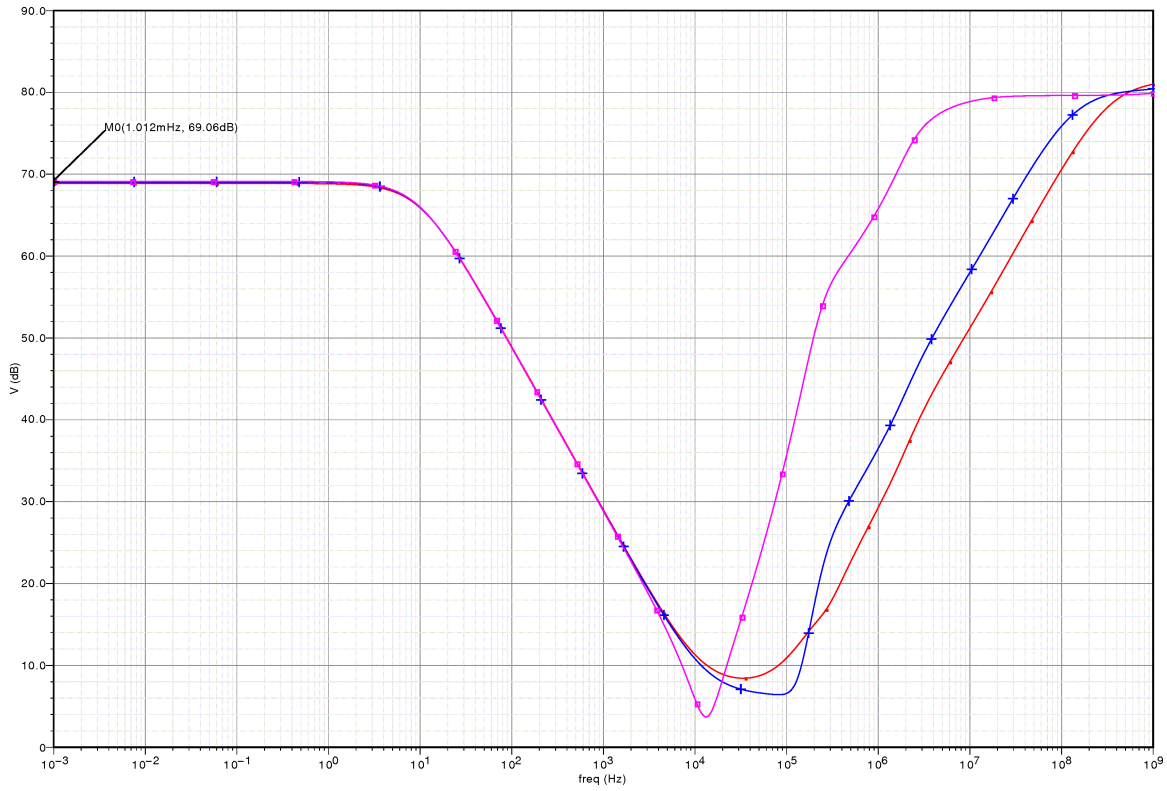


Figure 4.15: *Cadence* simulation: power-supply-rejection-ratio. The red, blue and magenta lines are the PSRR with R_{load} equal to $1.2[\Omega]$, $12[\Omega]$ and $1.2[k\Omega]$ respectively.

caused by the output stage of the error amplifier and differentiator, that unfortunately provide two additional paths that vary this parameters. Generally, the considered path through the band-gap, called block K, does not affect the PSRR as much as the last mentioned paths (figure 4.16), because it is small.

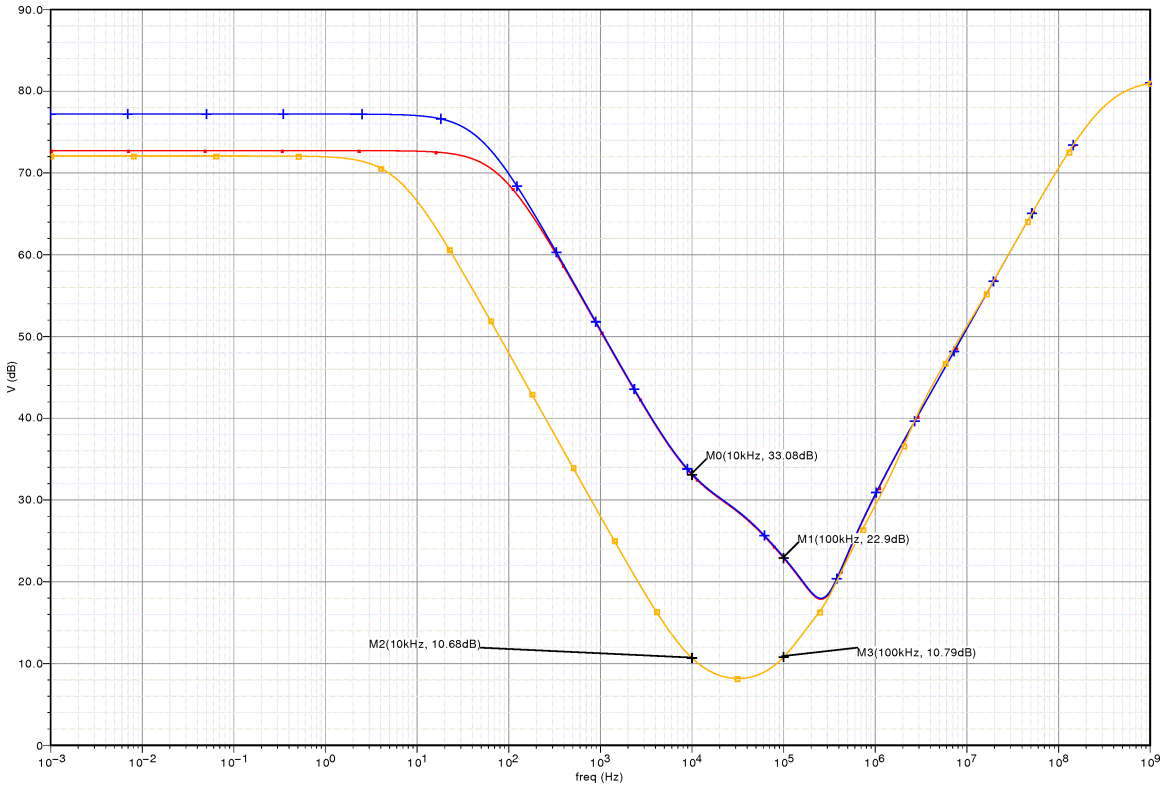


Figure 4.16: *Cadence* simulation: PSRR with different paths with R_{load} equal to $1.2[\Omega]$. The red line consider only the power MOS path, the blue line the error amplifier output stage and the power MOS paths while the yellow line consider also the differentiator path.

4.5 Statistical Analysis

In the integrated circuits production, the random variations of the electrical parameters are caused by the manufacturing processes:

- between different lots,
- between different wafers,
- in the same wafer, between different chips (or dies),
- in the same chip, between the components.

On the last case we talk about **local effect** and the difference is the effect between the devices.

Monte Carlo analysis is performed to study the regulator sensitivity to process variation such as carrier mobility and MOSFET threshold voltage (N=200). All the Monte Carlo simulations use the set-up of the Infineon manufacturing processes.

The DC steady-state output voltage was simulated for the process variation effects. The variation was verified for four different load resistance conditions, not connected, $1.2[k\Omega]$, $12[\Omega]$, and $5[\Omega]$. The results are shown in figure 4.17.

The bandwidth of the system GBW was simulated for the process variation effects. The variation was verified for four different load resistance conditions, not connected, $1.2[k\Omega]$, $12[\Omega]$, and $5[\Omega]$. The results are shown in figure 4.18.

The phase margin of the total loop was simulated for the process variation effects. The variation was verified for four different load resistance conditions, not connected, $1.2[k\Omega]$, $12[\Omega]$, and $5[\Omega]$. The results are shown in figure 4.19.

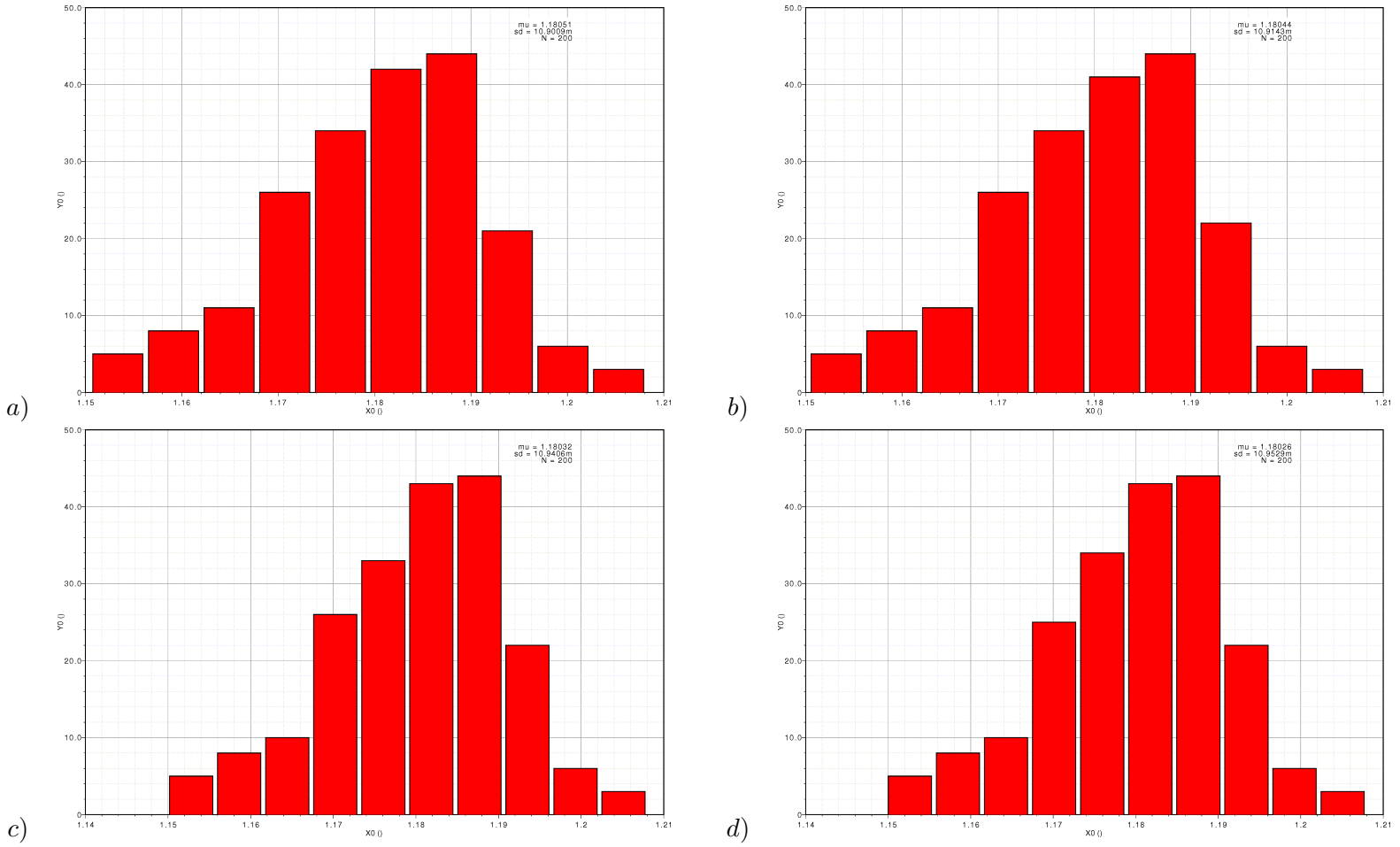


Figure 4.17: *Cadence* Monte Carlo simulation: DC steady-state output voltage with load resistance conditions, not connected $a)$, $1.2[k\Omega]$ $b)$, $12[\Omega]$ $c)$, and $5[\Omega]$ $d)$.

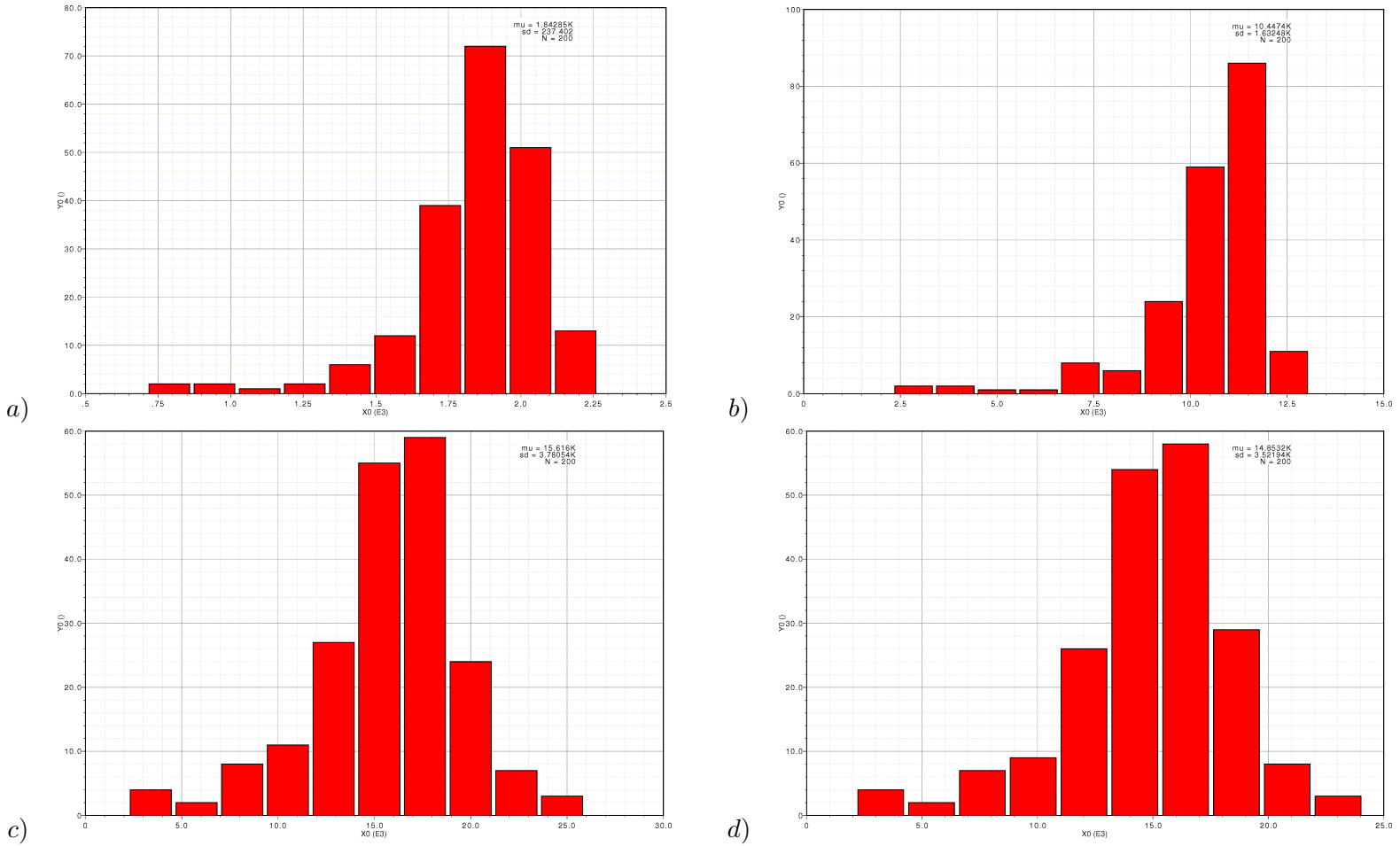


Figure 4.18: *Cadence* Monte Carlo simulation: bandwidth of the system GBW with load resistance conditions, not connected $a)$, $1.2[k\Omega]$ $b)$, $12[\Omega]$ $c)$, and $5[\Omega]$ $d)$.

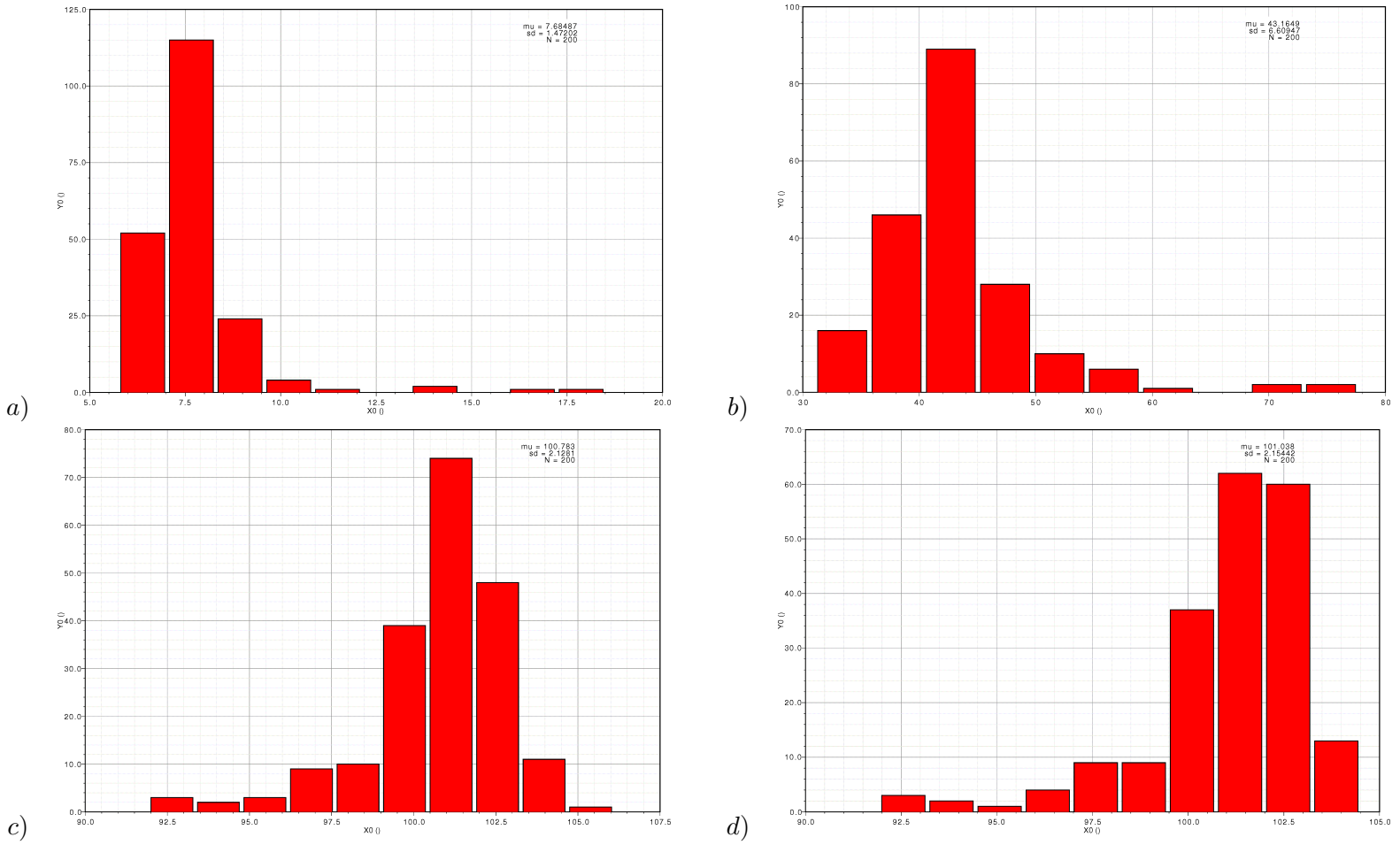


Figure 4.19: *Cadence* Monte Carlo simulation: phase margin of the total loop with load resistance conditions, not connected $a)$, $1.2[k\Omega]$ $b)$, $12[\Omega]$ $c)$, and $5[\Omega]$ $d)$.

Conclusions

In this work thesis a linear voltage regulator with low drop-out voltage has been studied. The compensation technique used highlights the potential to the future developments. The pole splitting compensation allows to improve the stability and also creates a new fast path that decreases the transient time response.

Some design targets of the proposed realization, like the full stability at all load currents (a minimum phase margin $> 45[deg]$), the bandwidth of the system and finally the PSRR specification are not achieved for the physical limits; for this reasons we focused on the achievement of other major targets like the stability. The change of the power MOS changing the maximum load current, improves the stability because the external pole variation is decreased. This work thesis shows the limits of the proposed low cost technology which is reflected in poor performance of the differentiator.

The solution to reach the stability is to change the technology with a higher performance one. Milliken's thesis [4] and his following article [3] realises a voltage regulator with a $0.35[\mu m]$ CMOS technology. The technology scaling, in fact, allows to:

- integrate more devices in the same chip,
- decrease the parasitic capacitances,
- increase the transconductance,
- operate with lower voltages.

The result of the technology scaling is the increase of the frequency response [1]. In fact using the `LDO behavior`, it is possible to understand that the decrease of the parasitics capacitance allows to reach higher gain and bandwidth in the differentiator block.

The change of the power MOS or the increase of the differentiator gain and bandwidth (using a better technology), can improve the stability at all load currents. The large working range of the load shown in figure 4.20a (dotted blue lines) requires a strong compensation that in this work thesis cannot be reached because of the technology limits.

On the proposed regulator there were other two solutions to reach the stability: the ground current increase and/or the error amplifier DC gain decrease; however, these are usually not acceptable.

The bandwidth specification of the system can be hardly reached. In fact to increase the bandwidth the differentiator gain and the total loop gain should be increased. The increasing of the differentiator gain enhances the pole splitting effect while the total loop gain increase can be realised acting (for example) on the error amplifier.

The PSRR specifications can be reached by discriminating the two cases reported in table 2.3 (page 39). The first specification on the PSRR is $> 70[dB]$ @ $10[kHz]$. Generally at this frequency the PSRR is not affected from the differentiator path but the main contribution comes from the outer loop as shown in the equation 1.20. This target can be reached by increasing the main loop gain. The second specification on the PSRR is $> 40[dB]$ @ $100[kHz]$. At this frequency the PSRR is affected by the differentiator gain as shown in the equation 2.16 that in the proposed regulator was maximized.

Future work

Unfortunately the test chip realised in this work thesis has not been analysed yet in laboratory, because it was not produced in time. The future works will focus on two objectives:

- the analysis of the test chip realised,
- the achievement of the targets using a higher performance technology.

The guideline that has been chosen in this work thesis and will be used in the next re-design can be summarized as follows:

- to update all the parameters that change with the technology in the `LDO behavior` GUI,

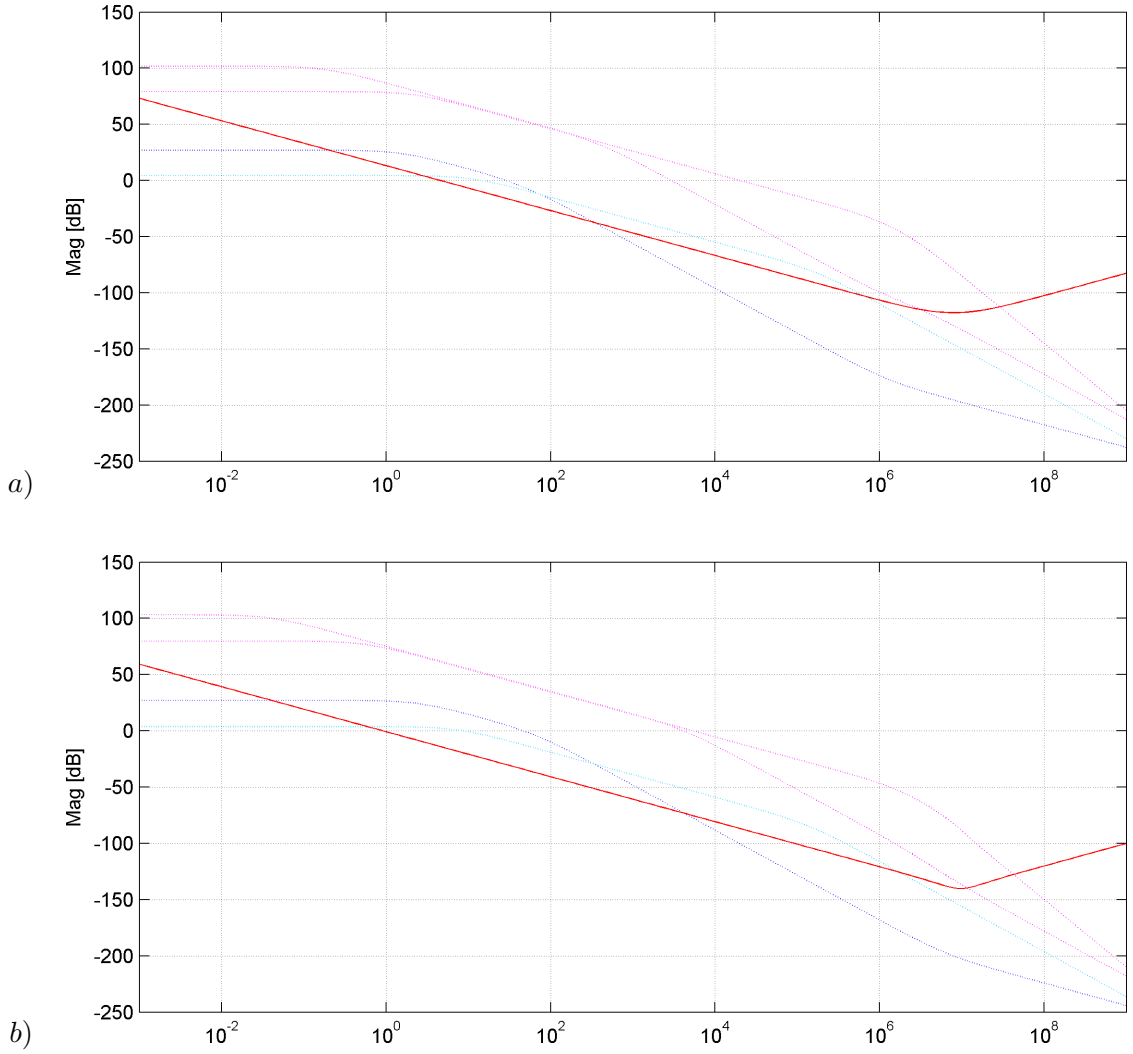


Figure 4.20: `LDO behavior` simulation: proposed realization a) and future realization b). The two dotted blue lines represent the large working range of the block B, the red line is $\frac{1}{D}$ and the dotted magenta lines are the total loop gain in the previous working range of the load.

- to understand the performance that is required for the error amplifier and the differentiator to reach firstly the stability with all load and then the PSRR,
- to design the error amplifier and the differentiator with the parameters provided by `LDO behavior`,
- to understand the limits and the potentials of the used technology aiming to the most important target specifics,
- to simulate the circuit realised and check the result with those that are provided by `LDO behavior`,
- to create a test chip to characterise and compare it with the previous simulations,
- to understand if it is possible to improve this circuit.

The first two points have been done and the results of the `LDO behavior` are showed in figure 4.20b and in table 4.2.

Error Amplifier		Differentiator		Main feedback network	
G_{m1}	$240[\mu S]$	G_{mf1}	$10[mS]$	R_{f1}	$20[k\Omega]$
R_1	$> 39[M\Omega]$	R_f	$200[k\Omega]$	R_{f2}	$40[k\Omega]$
f_{Pint}	$> 3.1[MHz]$	C_f	$11[pF]$		
		G_{mf2}	$2[mS]$		

Table 4.2: Future target realization using a new and higher performance technology: performance provided by `LDO behavior` of the error amplifier, differentiator and main feedback network.

There are good chances that these future works will be performed personally at the Infineon design centre of Padova.

Appendix A

Return ratio analysis

The classic feedback analysis uses the two-ports method to manipulate a feedback circuit into a unilateral forward amplifier and a feedback network.

Here is reported an alternative analysis that does not use two-ports [1]. This analysis, which is often easier than the two-port analysis, is called return-ratio analysis. Here, the closed-loop properties of a feedback circuit are described in terms of the return ratio for a dependent source in the small-signal model of an active device. The return ratio for a dependent source in a feedback loop is found with the following procedure:

1. Set all independent sources to zero.

2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the feedback loop.

3. On the side of the break that is not connected to the dependent source, connect an independent test source s_t, of the same sign and type as the dependent source.

4. Find the return signal s_r, generated by the dependent source.

Then the return ratio $\mathcal{R}(s)$ for the dependent source is:

$$\mathcal{R}(s) = -\frac{s_r}{s_t},$$

where the variable s represents either a current or a voltage.

Closed-Loop Gain Using Return Ratio

A formula for the closed-loop gain of a feedback amplifier in terms of the return ratio will now be derived. Consider a feedback amplifier as shown in figure A.1. The feedback

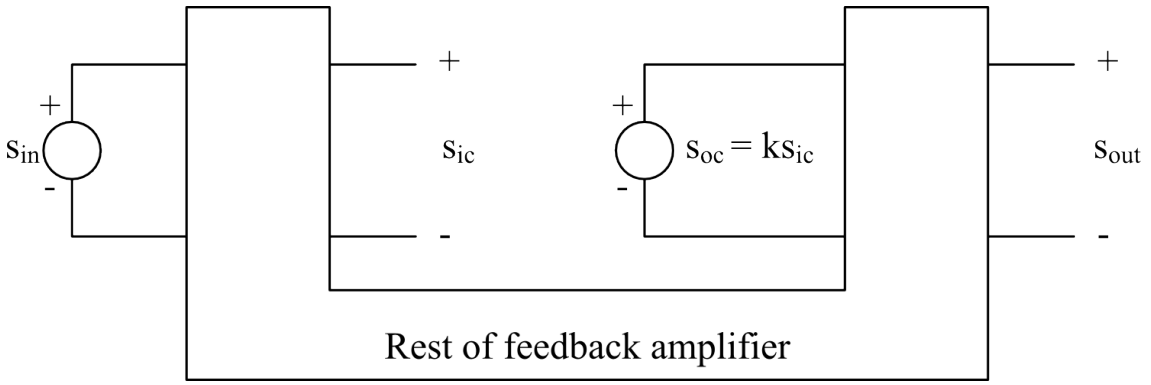


Figure A.1: Linear feedback amplifier used to derive the closed-loop gain formula.

amplifier consists of linear elements: passive components, controlled sources, and small-signal transistor models. A controlled source with value k that is part of the small-signal model of an active device is shown explicitly. The output of the controlled source is s_{oc} and the controlling signal is s_{ic}. The equation that describes the controlled source is:

$$s_{oc} = k\, s_{ic} \tag{A.1}$$

Each signal s in the figure is labelled as if it is a voltage, but each signal could be either a current or a voltage. Because the feedback amplifier is linear, signals s_{ic} and s_{out} can be expressed as linear functions of the outputs of the two sources, s_{oc} and s_{in},

$$s_{ic} = B_1\, s_{in} - H\, s_{oc} \tag{A.2}$$

$$s_{out} = d\, s_{in} - B_2\, s_{oc} \tag{A.3}$$

The terms B_1, B_2, and H in A.2 and A.3 are defined by:

$$B_1 = \left.\frac{s_{ic}}{s_{in}}\right|_{s_{oc}=0} = \left.\frac{s_{ic}}{s_{in}}\right|_{k=0} \tag{A.4}$$

$$B_2 = \frac{s_{out}}{s_{oc}}\Big|_{s_{in}=0} \tag{A.5}$$

$$H = -\frac{s_{ic}}{s_{oc}}\Big|_{s_{in}=0} \tag{A.6}$$

So B_1 is the transfer function from the input to the controlling signal evaluated with $k = 0$, B_2 is the transfer function from the dependent source to the output evaluated with the input source set to zero, and H is the transfer function from the output of the dependent source to the controlling signal evaluated with the input source set to zero, times -1.

Also, the direct feed-through d is given by:

$$d = \frac{s_{out}}{s_{in}}\bigg|_{s_{oc}=0} = \frac{s_{out}}{s_{in}}\bigg|_{k=0} \tag{A.7}$$

which is the transfer function from the input to the output evaluated with $k = 0$. The calculation of d usually involves signal transfer through passive components that provide a signal path directly from the input to output, a path that goes around rather than through the controlled source k.

Equations A.1, A.2 and A.3 can be solved for the closed-loop gain. Substituting A.1 in A.2 and rearranging gives:

$$s_{ic} = \frac{B_1}{1 + k\,H} s_{in} \tag{A.8}$$

Substituting A.1 in A.3 and then substituting A.8 in the resulting equation and rearranging terms gives the closed-loop gain A:

$$A = \frac{s_{out}}{s_{in}} = \frac{B_1\,k\,B_2}{1 + k\,H} + d \tag{A.9}$$

The term kH in the denominator is equal to the return ratio, as will be shown next. The return ratio is found by setting $s_{in} = 0$, disconnecting the dependent source from the circuit, and connecting a test source s_t where the dependent source was connected. After these changes, $s_{oc} = s_t$ and A.2 becomes:

$$s_{ic} = -H\,s_t \tag{A.10}$$

Then the output of the dependent source is the return signal $s_r = k\, s_{ic} = -k\, H\, s_t$. Therefore:

$$\mathcal{R} = -\frac{s_r}{s_t} = k\, H \tag{A.11}$$

So the closed-loop gain in A.9 can be rewritten as:

$$A = \frac{s_{out}}{s_{in}} = \frac{B_1\, k\, B_2}{1+\mathcal{R}} + d \tag{A.12}$$

or

$$A = \frac{s_{out}}{s_{in}} = \frac{g}{1+\mathcal{R}} + d \tag{A.13}$$

where

$$g = B_1\, k\, B_2. \tag{A.14}$$

Here g is the gain from s_{in} to s_{out} if $H = 0$ and $d = 0$, and d is the direct signal feed-through, which is the value of A when the controlled source is set to zero $(k = 0)$.

The closed-loop gain formula in A.12 requires calculations of four terms: B_1, B_2, d, and $\mathcal{R}$. This equation can be manipulated into a more convenient form with only three terms. Combining terms in A.13 using a common denominator $1+\mathcal{R}$ gives:

$$A = \frac{g + d\,(1+\mathcal{R})}{1+\mathcal{R}} = \frac{g + d\mathcal{R}}{1+\mathcal{R}} + \frac{d}{1+\mathcal{R}} = \frac{\left(\frac{g}{\mathcal{R}} + d\right)\mathcal{R}}{1+\mathcal{R}} + \frac{d}{1+\mathcal{R}} \tag{A.15}$$

Defining

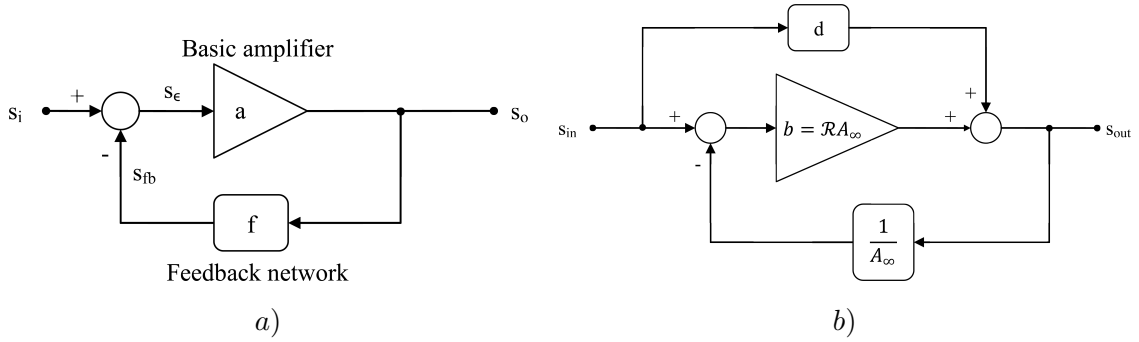
$$A_\infty = \frac{g}{\mathcal{R}} + d, \tag{A.16}$$

allows A.15 to be rewritten as:

$$A = A_\infty \frac{\mathcal{R}}{1+\mathcal{R}} + \frac{d}{1+\mathcal{R}} \tag{A.17}$$

This is a useful expression for the closed-loop gain. Here, if $\mathcal{R} \to \infty$, then $A = A_\infty$ because $\frac{\mathcal{R}}{1+\mathcal{R}} \to 1$ and $\frac{d}{1+\mathcal{R}} \to 0$. So A_∞ is the closed-loop gain when the feedback circuit is ideal (that is, when $\mathcal{R} \to \infty$).

A block-diagram representation of A.17 is shown in figure A.2b. The gain around the feedback loop is $\mathcal{R}$, and the effective forward gain in the loop is $\mathcal{R}\, A_\infty$. A key difference



a) *b)*

Figure A.2: Difference between the two-port a) and return-ratio b) analyses.

between the two-port and the return-ratio analyses can be seen by comparing figures A.2a and A.2b.

In the two-port analysis, all the forward signal transfer through the amplifier and the feedback network is lumped into a. In the return-ratio analysis, there are two forward signal paths: one path d for the feed-forward through the feedback network and another path $\mathcal{R}\,A_\infty$ for the effective forward gain.

Typically, A_∞, is determined by a passive feedback network and is equal to $\frac{1}{f}$ from two-port analysis. The value of A_∞, can be found readily since $A_\infty = A$ when $k \to \infty$. Letting $k \to \infty$ causes $\mathcal{R} = k\,H \to \infty$. (Here we assumed $k > 0$. If $k < 0$ in a negative feedback circuit, then $\mathcal{R} \to \infty$ when $k \to -\infty$.) When $k \to \infty$, the controlling signal s_{ic} for the dependent source must be zero if the output of the dependent source is finite. The controlled source output will be finite if the feedback is negative.

Appendix B

LDO behavior

`LDO behavior` is a Matlab GUI or Graphical User Interface that was created for analysing the stability and the time domain response of a multi-feedback regulator like the one presented in this thesis. The aim was not to replace *Cadence* or another simulation software but to make easier to understand the effect of any change in the parameters value. In figure B.1 the GUI is presented.

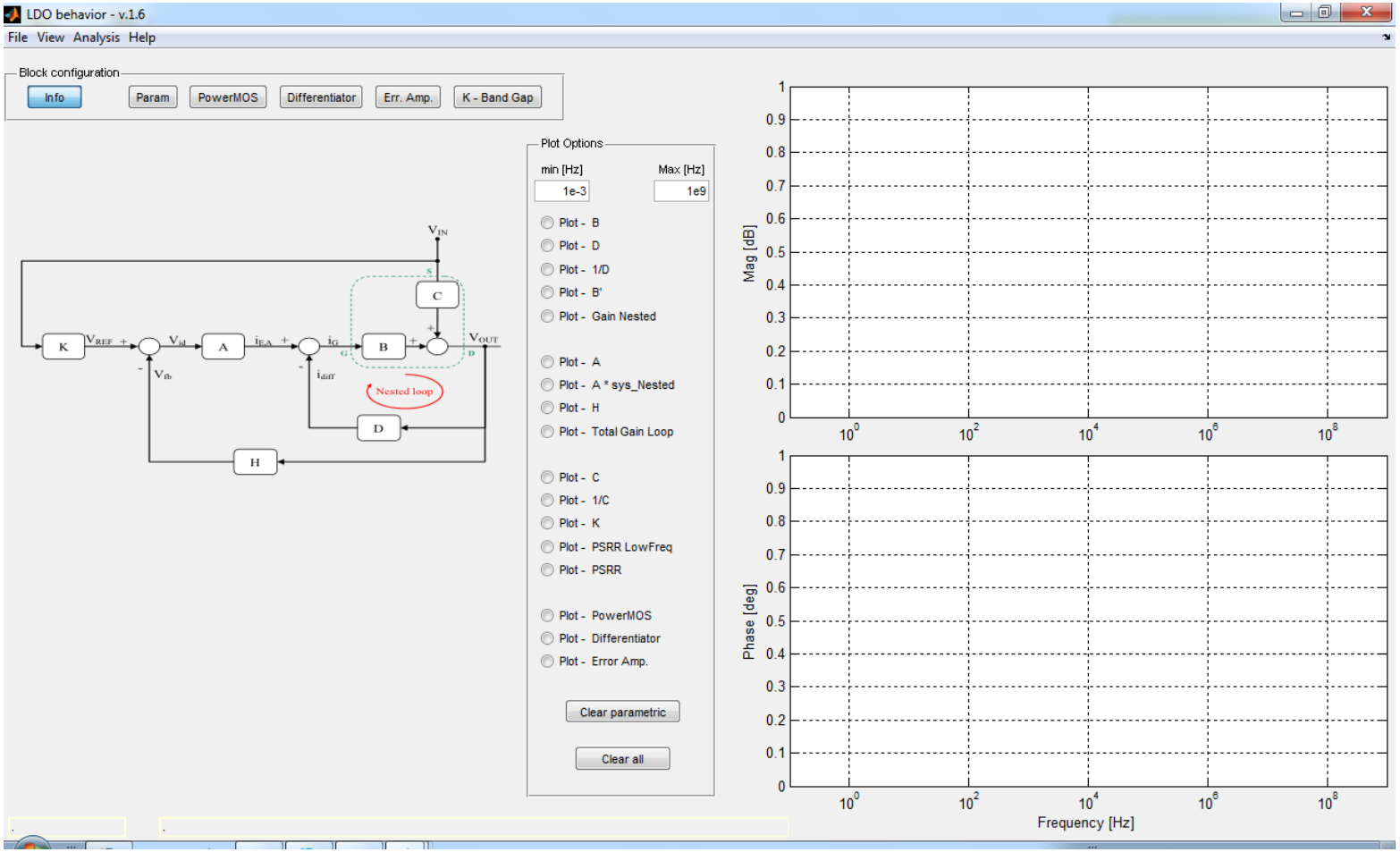


Figure B.1: `LDO behavior - v.1.6`.

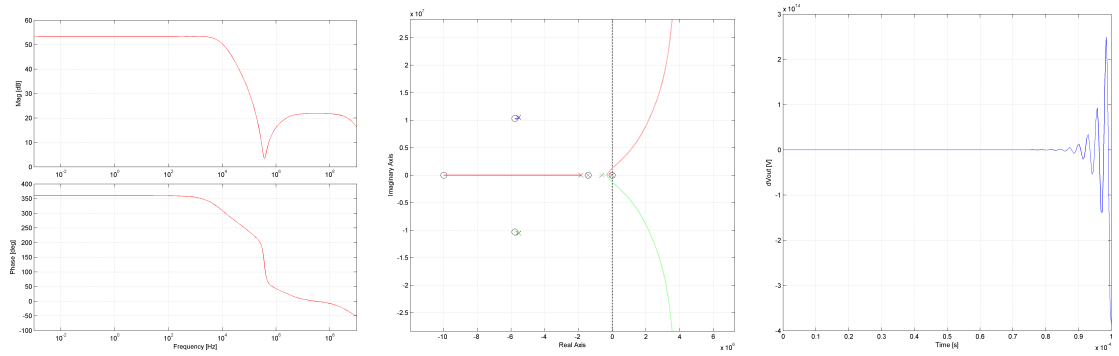
Menu bar

The menu bar of `LDO behavior - v.1.6` has four entries:

File: here there are the options to export or import the parameter data or save an image of the graphic area. The open and save section is capable of importing and exporting an Excel version of the data.

View: here it is possible to select the ideal blocks section or the parameters section. The ideal blocks section allows to define all the blocks as transfer functions where it is possible to set the poles and the zeros by means of a slider. The parameters section allows to set the parameter values for the ac model like resistance, transconductance and capacitance. In the latter section, it is possible to choose the type of the differentiator between a passive and an active realization.

Analysis: here is possible choose between three analysis like Bode, root locus and time domain response.



a) *b)* *c)*

Figure B.2: Analysis available: *a)* Bode, *b)* root locus and *c)* time domain response.

Help: here information about the program and the creator can be found.

Workspace

The workspace of `LDO behavior - v.1.6` consists of four areas (figure B.3).

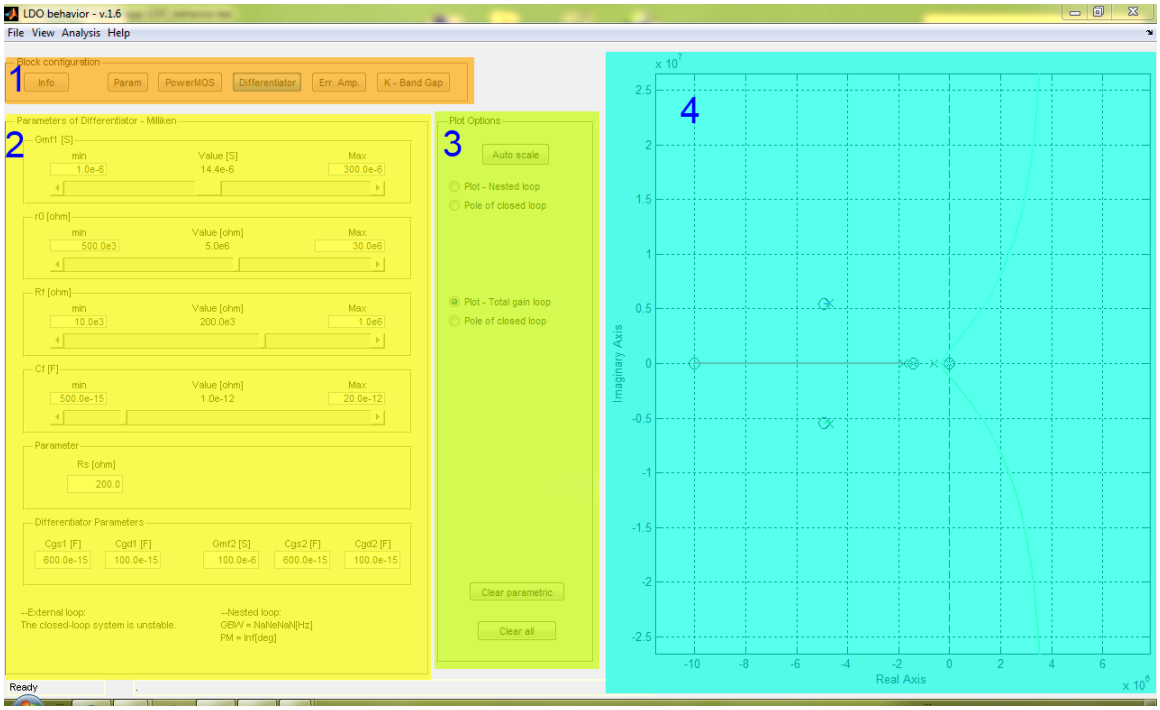


Figure B.3: `LDO behavior - v.1.6` workspace.

Block configuration is the first area shown in figure B.3 where a block can selected. This area changes accordingly to the View menu bar.

Parameters of LDO is the second area shown in figure B.3 where it is possible to change the parameters with a slider or by setting a fixed value (figure B.4).

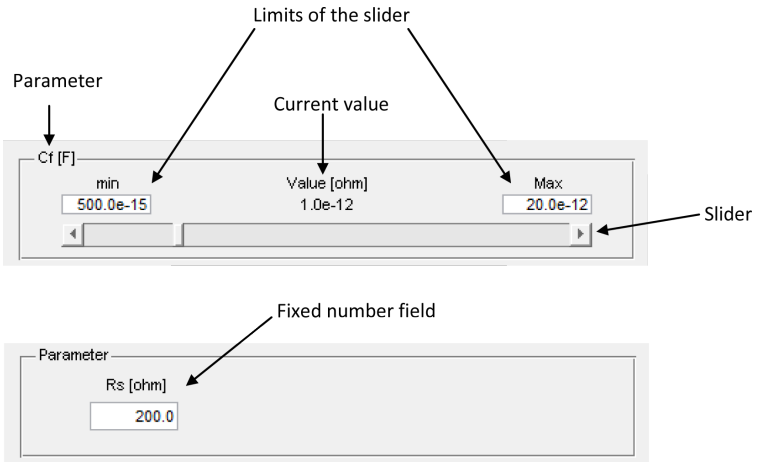


Figure B.4: `LDO behavior` slider and fixed number field.

Plot options is the third area shown in figure B.3 that allows to choose the functions to be plotted. This area changes accordingly to the Analysis menu bar.

Graphic area is the forth area shown in figure B.3 where the chosen functions are plotted. This area changes accordingly to the Analysis menu bar.

The code

I consider useless to publish all the source code of `LDO behavior - v.1.6` which consists of about 3500 lines. Instead, it is useful to comment the functions that I wrote.

Graphics_update manages the graphic update of the workspace accordingly to the **View** item in the menu bar.

TpannelBlock_SelectionChangeFcn manages the graphic update of the **Parameters of LDO** area by using a tabbed visualization.

update that when invoked saves the value of the last changed parameter in the database *handles.DATA(xx,xx)*.

personal_plot that when invoked calculates all the transfer functions useful for the analysis selected. Then plots the curves selected in **Plot Options** and in the end invokes the Matlab command *margin* to calculate the phase margin of the two loops.

drawRLocus is able to pre-analyse the system (given as input). Then plots in the axes (given as input) the root locus and the root required.

personal_check checks the parameters entered through the keyboard. If this parameter is not set correctly, the default value is placed and the function *err* is called.

personal_conv manages the strings of numbers displaying them with powers of ten multiples of three. This displaying function is usually called *engineering notation*.

err manages all the error dialogue windows.

amended_file is a useful function that understands if the parameters used are changed from those of the loaded file.

TGuiLDO_CloseRequestFcn asks if it necessary to save the current dataset.

releaser provides some information about the creator of `LDO behavior`.

The comparison with Cadence

In figures B.5 and B.6 are showed the simulations of the total loop gain with two load conditions, provided to `LDO behavior - v.1.6` and *Cadence*. As can be seen between $1[mHz]$ to $1[MHz]$ the results of the `LDO behavior - v.1.6` are similar to *Cadence*.

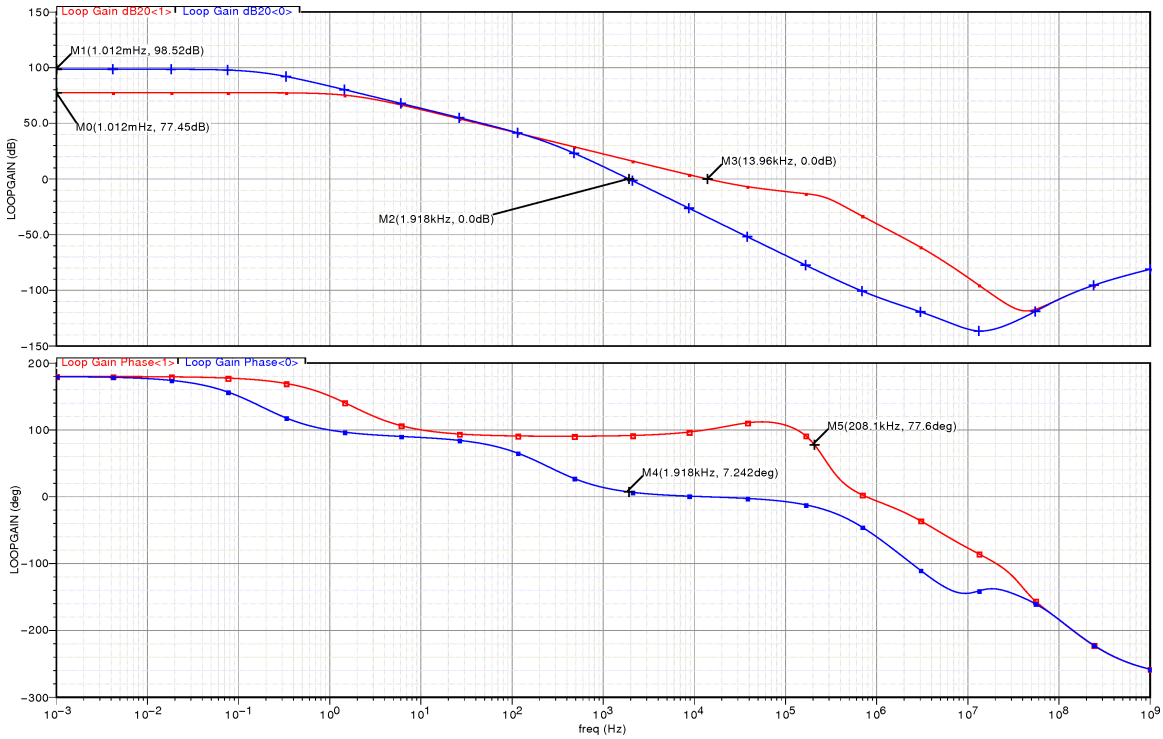


Figure B.5: Total loop gain with $R_{load} = 1.2[\Omega]$ red line and without load blue line: *Cadence* simulation.

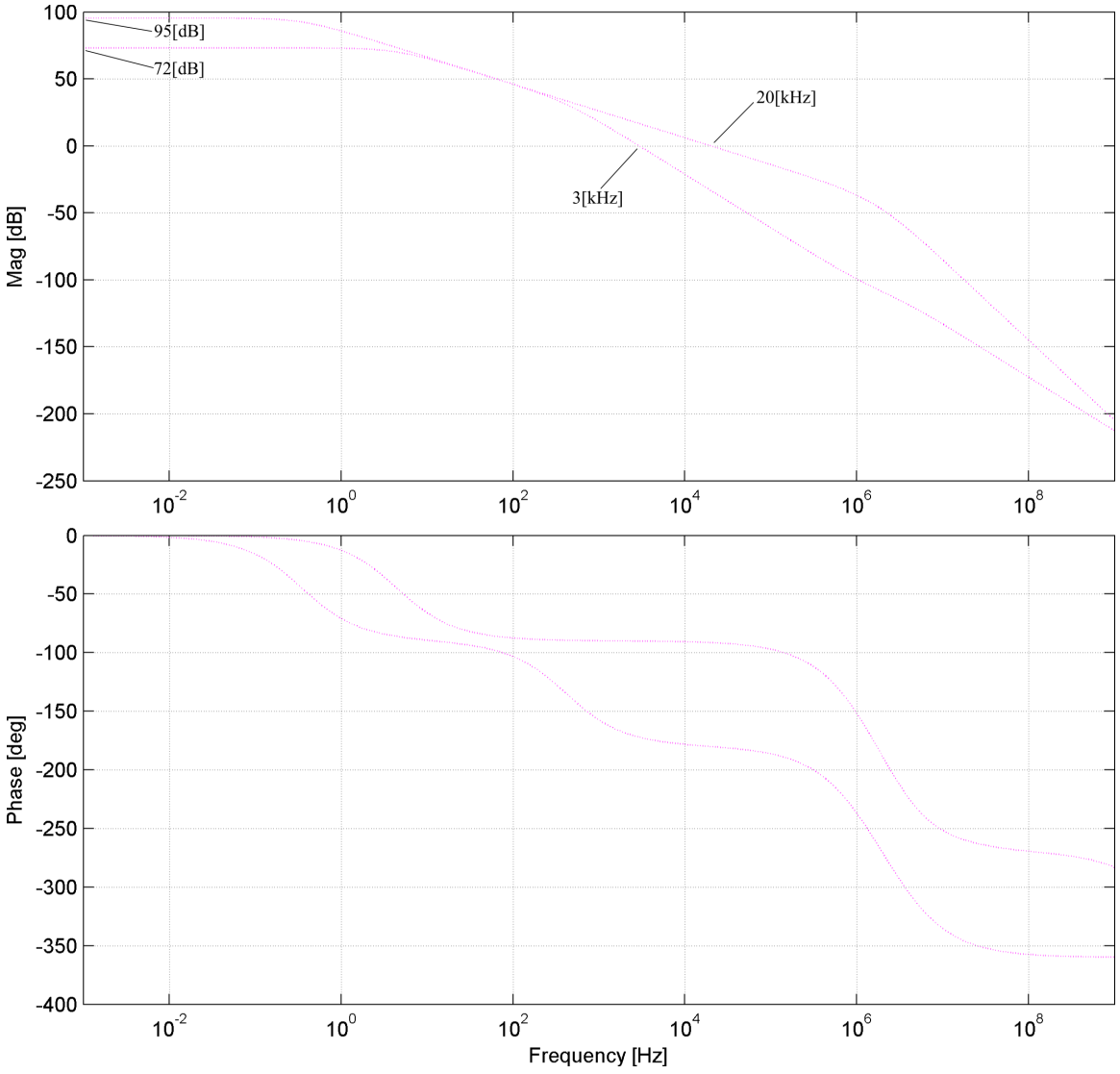


Figure B.6: Total loop gain with the same load conditions of figure B.5: `LDO behavior - v.1.6` simulation.

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