Università degli Studi di Padova

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GaN-Based Three-Phase Inverter for Electric Bicycles

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Abstract

This thesis reports the design of a GaN-based three-phase inverter for the motors of an electric bicycle under test at the Electric Drives laboratory at the University of Padova. The thesis opens with a review of the current literature, highlighting the main challenges of the project. The second chapter describes the selection and sizing of the inverter components. The third chapter describes the developed design of the printed circuit board, discussing the main key choices for fulfilling the desired functionalities and specifications. Chapter four draws the conclusions of the work and contemplates future developments.

Acknowledgement

Firstly, I would like to express my gratitude to my supervisor professor Tommaso Caldognetto for always kindly providing his tireless assistance, even late at night and during weekends. Without his dedication, this thesis work would not have been possible.

Special thanks also go to my parents and family who patiently endured my crankiness and mental breakdowns during my university studies. It is with a feeling of immense accomplishment that I dedicate this thesis to them.

Finally, my girlfriend Anna deserves an honorable mention for her constant encouragement during the final phases of this work. I would like to thank her for her sweet, heartwarming smiles and kind words.

Contents

1 Critical aspects and solutions shown by literature

Before considering the design of the pursued inverter using GaN power devices, it is worth highlighting their characteristics and the challenges that typically accompany a project based on such technology. A review of the most recent literature was conducted in order to investigate the feasibility of a 3-phase inverter prototype for e-Bike motors based on GaN transistors and the subsequent problems that need to be addressed in order to obtain a successful design that fully exploits the advantages offered by this new technology.

This chapter aims to provide a summary on the most critical aspects and solutions which will be considered in the design of the prototype based on the results found in literature.

1.1 Motivations for a GaN-based conversion circuit

Ever since their inception in the commercial market in 2010 [19][10], GaN power devices have proved to be attractive to electronic converters designers due to their high switching speeds which enable pushing the switching frequencies up of 2 orders of magnitude at most, from the tens of kHz typical of Si to the 100 kHz ÷ 1 MHz range. This helps cutting down losses caused by harmonic distortion (as the higher frequency components do not contribute to the transfer of active power to the load and are dissipated by the parasitic resistances) and, most importantly, allows reducing the size of filtering components; a feature which is greatly desirable in an e-Bike application where space is a constraint, since these are usually the bulkiest parts of a converter.

1.2 Parasitic impedances

With switching speeds typically lower than 10 V/ns, GaN devices are capable of running at very high switching frequencies but, due to the extremely steep current and voltage transients, they are also much more sensitive to the impact of parasitic impedances.

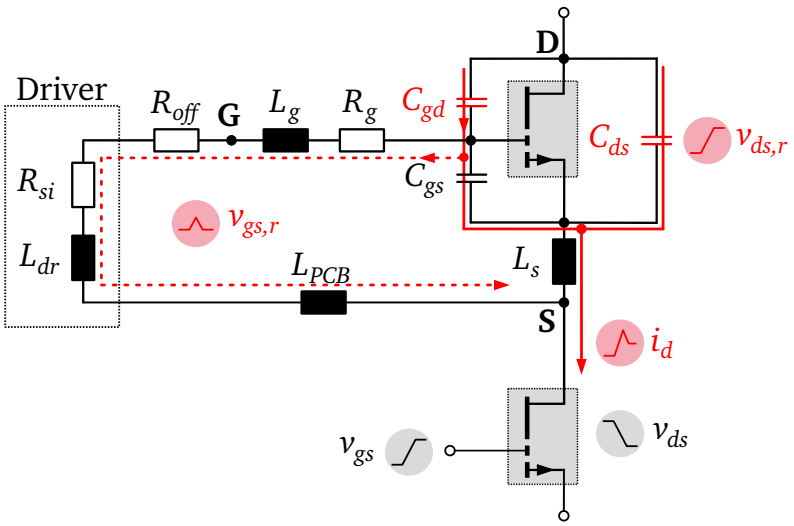


Fig. 1.1: Mechanism causing $C\,\mathrm{d}v/\mathrm{d}t$ induced effects and displacement currents in a phase-leg configuration during turn-on of the low-side device (image adapted from [7]).

These parasitic elements can cause unexpected behavior and unintended consequences, circuit malfunction, electromagnetic interferences (EMI), oscillations, and, in extreme cases, cross-conduction or "shoot-through" that can lead to transistor failures. The parasitic effects on the switching transients can be divided into $C\,\mathrm{d}v/\mathrm{d}t$ induced and $L\,\mathrm{d}i/\mathrm{d}t$ induced effects.

1.2.1 Impact of parasitic capacitances

The main cause of $C\,\mathrm{d}v/\mathrm{d}t$ induced effects in a phase-leg configuration, such as the one shown in Fig. 1.1), are the parasitic capacitances of the GaN HEMTs, in particular the output capacitance $C_{oss} = C_{ds} + C_{gd}$ of the high-side transistor. Double pulse tests conducted in [7] show that when fast voltage swings appear across the output capacitance, an overcurrent phenomenon, similar to a reverse recovery, occurs. This displacement current is distributed between the drain-source capacitance C_{ds} and the miller capacitance C_{gd}, according to the C_{gd}/C_{ds} ratio of the device. The current induced at the miller capacitance is itself split between the gate-source capacitance C_{gs} and the gate driver path, leading to voltage drops across the parasitic resistances and inductances of the gate loop which may increase the gate-source voltage over the threshold voltage and spuriously turn on the device. Reducing the speed of the switching transitions can mitigate this issue, however it would also nullify the advantages offered by the GaN technology. It is all but impossible to make the gate-drive loop low enough impedance with separately-packaged transistor and driver. This is primarily why negative gate-bias

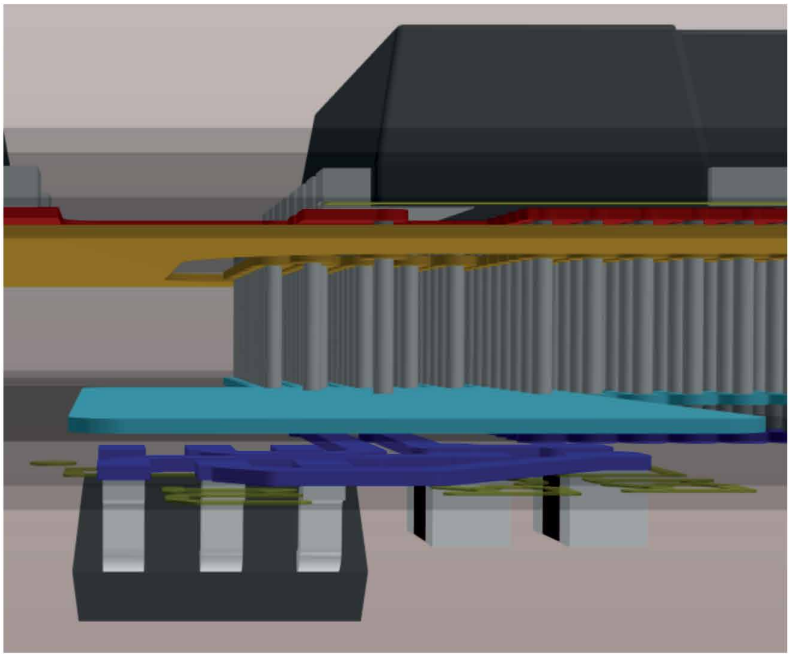


Fig. 1.2: Faraday shield to mitigate the common-mode capacitance problem. The light blue plane shields the gate drive circuit (bottom) from the ground plane (yellow).

is used in discrete designs: to provide sufficient margin so that gate bounce voltage does not exceed the threshold during switching transients [20].

On the other hand, the parasitic capacitance between the gate return path and the ground plane can and should be minimized by carefully designing the PCB layout. In particular, as suggested in [14], the gate drive return current should be routed on a plane-layer directly below the gate drive circuit and connected to the Kelvin source pin. This layer works as a sort of Faraday shield (illustrated in Fig. 1.2) which keeps the DC bus ground-referenced circuits away from the high-side gate-drive circuit. Thus, the gate-drive circuit only "sees" the small capacitance to its own local common, not to the bus ground plane. The current necessary to charge and discharge the capacitance between the Faraday shield and the DC ground plane therefore comes directly from the low-impedance switch-node, completely bypassing the gate-drive circuit.

Another solution to solve the problems described above, thanks to the recent developments in integration of components, comes from the new power stage ICs which integrate the driver circuit with the power transistor on the same die. This way the parasitic components are minimized already from the factory and the PCB layout design is greatly simplified.

1.2.2 Impact of parasitic inductances

The concepts of parasitic resistance and capacitance are quite straightforward to grasp: the first can be minimized by simply using more copper (increase the total current-carrying cross-section) while the second one is easy to see in a structure like a PCB, where copper layers act as parallel plates with a thin dielectric layer in between. Both of them can also be thought as discrete elements that sum together when put in series or parallel respectively.

Parasitic inductance is different: basic magnetics teaches that inductors interact with each other through mutual inductance, which can either increase or decrease the total inductance, depending on the geometry and direction of the current flow. Also, a good estimate of the layout inductance is often not available without experimental measurements carried out on a test prototype.

These issues are not new to power electronics design, but they become even more impacting as GaN transistors, with low gate charge and no reverse-recovery, make switching transitions even faster. Voltage overshoot in the power-loop can increase EMI issues and create higher voltage stress on the transistors, while an $L\,\mathrm{d}i/\mathrm{d}t$ reaction voltage in the gate loop will reduce the switching speed by opposing the applied gate voltage V_{gs} and can also lead to ringing and overshoot.

The newest GaN HEMTs in passivated die form can reduce the package parasitic inductance to almost negligible values. This is especially true for the power stage ICs of recent development, where integration helps reducing stray inductances. In this scenario, the stray inductance is mainly caused by the PCB layout.

It is of course impossible to minimize all interconnect inductance, and simultaneously eliminate all node-to-node capacitance on a PCB. The key to successful PCB layout is therefore to understand where the impedances really matter in switch-mode power electronics,and how to mitigate any undesired consequences of this inevitable impedance. For example, in a phase-leg configuration, the output side, which acts as a steady DC current port, won't be affected by the effects of parasitic inductance as much as the DC bus side, which should act like a steady DC voltage port despite current transients. As suggested in [14], the fundamental design principle is to route the outbound and return currents along the same path in order to exploit the subtracting interaction of inductances on adjacent parallel layers. It is crucial to avoid any lateral loops that will introduce additional inductance. Using topside-cooled transistor packages greatly helps in this regard as it removes the need for thermal vias by allowing to independently optimize the electrical and thermal paths while incidentally reducing drilling costs.

1.3 Reverse conduction losses

With the merit of advanced WBG material and wafer processing technologies, the body diode is eliminated in the GaN HEMT, which leads to no reverse recovery charge. This is one of the key features that gives GaN transistors a fast switching capability, along with a significant reduction of switching losses [8].

However, these advantages come at a cost, since the absence of the body diode also means that there is no diffusion of charge and reverse conduction has to take place exclusively due to drift currents. These can generate higher losses during the freewheeling period. In a three-phase motor drive (such as an e-Bike inverter) where space vector PWM is used, the reverse conduction period is generally limited to the length of the dead time and the effect of reverse conduction loss becomes marginal. Nevertheless, when regenerative braking is utilized or when the inverter is used to drive DC or single phase BLDC motors (done by disabling one leg and using the remaining two as a full-bridge), the reverse conduction period is significantly increased. [11] and [9] discuss some driving techniques aimed at reducing the reverse conduction and switching losses, which should be considered when designing a control algorithm for use with DC motors. Motor drive simulation results from both papers show that synchronous rectification (unipolar PWM with active freewheeling) can improve the efficiency of converters most effectively by suppressing the reverse conduction time.

1.4 Are GaN devices feasible for e-Bike driver applications?

While the harmonic distortion and filter size reduction cited at the beginning of this chapter are surely interesting advantages for an e-Bike inverter, they are not enough to justify the use of one type of devices just by themselves. The device's behavior in the specific operating conditions of such application must be considered too.

As demonstrated in [2], the semiconductor operating temperature and the converter switching frequency strongly affect the results of a comparison between different transistors and manufacturers, showing that different technologies may outperform each other depending on their operating conditions and specifications constraints. For example, two comparative performance assessments among the two most promising technologies in the near future of converters, SiC and GaN, were conducted; a first one using the easier to calculate $R_{ds,on}Q_{oss}$ figure of merit to provide a broad overview of the commercially available power switch technologies, and a second, more accurate one carried out

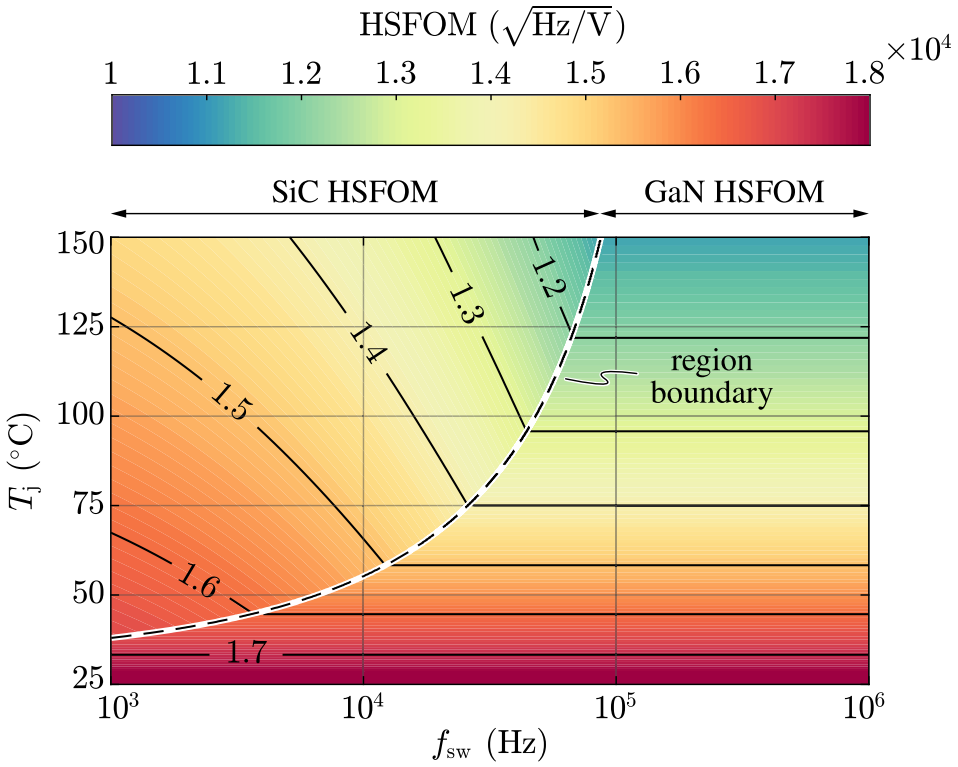


Fig. 1.3: HSFOM contour plot of the best performing semiconductor devices between Wolfspeed 650 V SiC MOSFETs and GaN Systems 650 V GaN e-mode HEMTs considering Vsw = 400 V, 1 kHz fsw 1 MHz and 25 °C Tj 150 °C. The region-delimiting boundary, indicating the intersection between the two HSFOM surfaces, is highlighted. Image taken from [2].

leveraging the newly introduced hard-switching figure of merit (HSFOM). It is worth noting that both figures can be easily evaluated with available datasheet information.

Even though $R_{ds,on}Q_{oss}$ does not fully characterize the semiconductor performance in hard-switching applications, as it does not account for the operating frequency of the converter, this preliminary comparison already highlights that GaN HEMTs outperform SiC MOSFETs at 25 °C. On the contrary, at temperatures around 150 °C, SiC devices appear to outperform the majority of GaN devices. This is due to the $R_{ds,on}$ resistance in GaN transistors, which strongly increases with temperature.

An even clearer distinction appears when the operating frequency is taken into account using the HSFOM. The contour plot in Fig. 1.3 highlights the presence of two distinct regions where SiC MOSFETs outperform GaN HEMTs and vice versa. While GaN HEMTs appear to perform best in low-temperature high-frequency applications, where they can fully leverage their superior switching performance, SiC MOSFETs still prove to be unmatched for lower frequency high-temperature operation due to their limited $R_{ds,on}$ dependence on temperature.

The new frontier for medium-small motor drivers (such as those for e-Bikes or vacuum cleaners) is to support PWM switching frequencies up to 250 kHz. This falls right in the high-frequency region of Fig. 1.3 where GaN devices perform better than SiC, at least up to temperatures of 150 °C, which makes them ideal for the kind of project that will be described in the following chapters.

Components selection and circuit design

2

2.1 Design requirements

An electric bike system is usually powered by a 24 V, 36 V, or 48 V lithium-ion battery, while its maximum power is set by EU regulations to be 250 W.* This means that an inverter designed for such a system has to be able to handle currents in the order of several amperes that are needed to transfer the necessary power. Given that the prototype will be used in a laboratory setting where motors are often pushed to their limits and beyond, the actual power could be much higher. Thus, the requirements set for this project, in order to maintain a good safety margin under the worst case stressing conditions, are the following:

- Supply voltage $V_{IN} = 18\,\text{V} \div 75\,\text{V}$. Even if the nominal voltage of an e-Bike battery is 48 V at most, when fully charged a higher voltage could be reached. Thus, the 75 V maximum value accounts for a 30% safety margin plus the possibility of using regenerative braking, which can raise the DC voltage over the 48 V limit.
- Steady state output current $I_{Phase} = 20\,\text{A}_{\text{RMS}}$.
- PWM switching frequencies up to 250 kHz thanks to the use of GaN power devices. The operating frequency is a variable that can be optimized during testing, however this aspect was not considered during this work as its impact on the overall design is small and can be eventually adjusted later by resizing the filters.

During usage, the inverter will be connected to a control system development platform such as the MicroLabBox by dSPACE and the PXI-7854R by National Instruments. These are expensive appliances which should be protected from costly damage that may occur during testing. Therefore, the circuit must provide total isolation for all the low voltage devices that will be in contact with the controller boards. This means that an isolated auxiliary power supply as well as isolated ICs will have to be chosen in order to allow perfect separation between high-side and low-side grounds. The resulting isolated power stage also eases the testing phases and helps managing EMI.

*European Union directive 2002/24/EC and Regulation No. 168/2013 of the European Parliament.

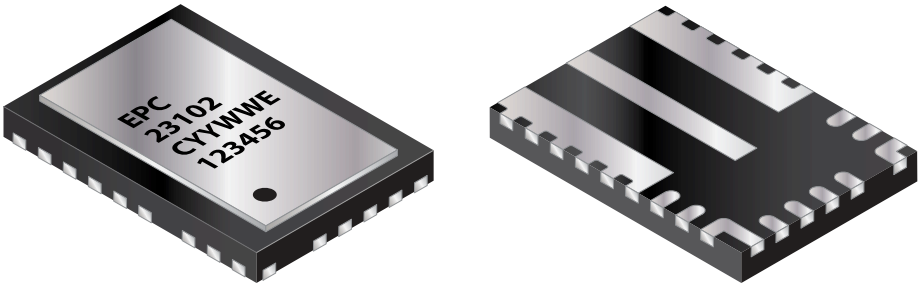
Ultimately, one last goal that was kept in mind during the development of this project is to try to keep the board size relatively compact. This is of particular importance since a compact layout of the switching converter is critical to avoid as much as possible the effects of parasitic components, noise and EMI. Approximately, the board should not exceed the size of typical commercially available products, which is around 10 cm × 10 cm.

2.2 Power stage ICs

The switching devices are the heart of any power conversion circuit and are therefore the most crucial component of the inverter. A crucial aspect to consider when looking for a candidate is that these components generate heat due to the high currents flowing through them. GaN devices help in this regard thanks to the absence of the reverse recovery charge which reduces the switching losses as discussed in section 1.3, offering high power-density capabilities in a compact form factor. Nevertheless, thermal management still requires particular care, because the achievable power levels can be limited by thermal overheating due to the extreme heat flux densities. Most of the GaN transistors currently on the market are packaged with a large conductive area underneath, referred to as "thermal pad", which provides low thermal resistance to the board. The area underneath the pad should be filled with copper vias in order to efficiently transfer the heat generated by the GaN HEMT to large copper areas in the PCB [17]. The problem with this kind of approach is that it can make the layout of the routes on the board more cumbersome, especially if stray inductances need to be minimized and space is a constraint, as in this case.

The optimal solution was found in the Quad Flat No-lead (QFN) package by EPC, which uses a flip chip on lead-frame technique [6]. This packaging structure, illustrated in Fig. 2.1, exposes the backside of the GaN die on the top side of the package, favoring the use of top-side mounted thermal management solutions by lowering the thermal resistance path from the die junction to an attached heatsink. Another important benefit is given by the very low parasitic inductance from the power terminals to the underlying PCB solder pads due to the small size of the package which doesn't exceed 5 mm in length.

The choice of device landed on the EPC23102 power stage IC by EPC. It can handle input and output voltages up to 100 V and steady state load currents up to 35 A. As shown by Fig. 2.2, these devices integrate input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with eGaN output transistors, providing a



(a) Top (b) Bottom

Fig. 2.1: EPC23102 QFN package outline and exposed backside of the GaN IC die.

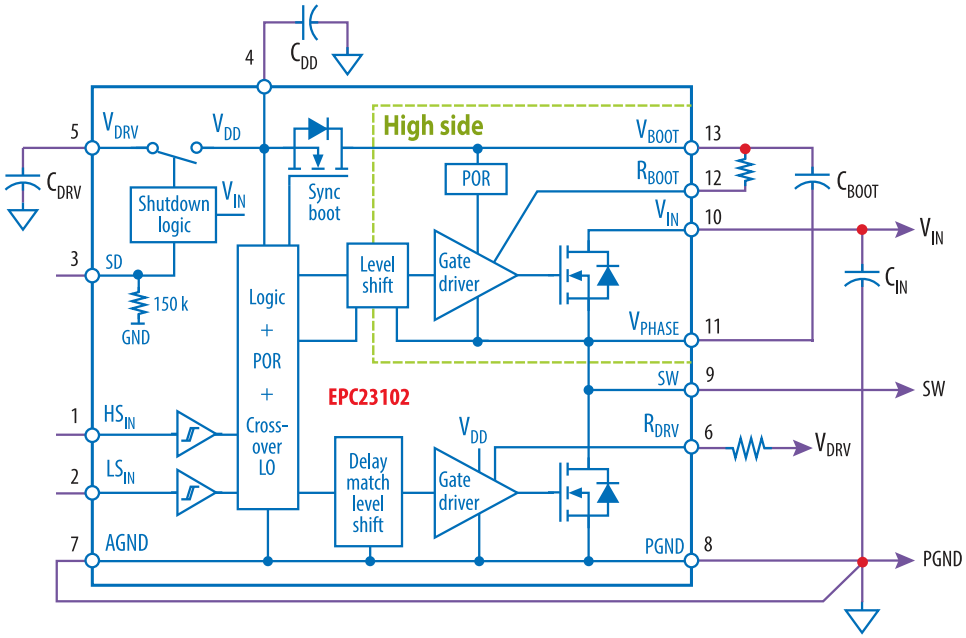


Fig. 2.2: Functional block diagram of the EPC23102 eGaN power stage.

fully functioning half-bridge leg on a single chip. This ensures high performance and also simplifies the circuit layout, as the gate drive and power loops come already optimized from the factory, reducing the parasitic impedances and the space occupied on the board to the absolute minimum, which makes these devices ideal for this application.

Due to their high level of integration, the EPC23102s require few external components to operate. In particular, according to [6], two resistors need to be connected to the R_{DRV} and R_{BOOT} terminals to tune the switching times and obtain a switching rate of 10 to 50 V/ns spanning zero to full load current. The design of optimal layout techniques to achieve minimized power loop inductance together with switching rate tuning by R_{DRV} and R_{BOOT}, allows to control the overvoltage spikes to less than +10 V above rail and -10 V below ground during hard switching transitions. Following the guidelines provided

by the EPC9176 Evaluation Board [4], 10 Ω resistors were chosen. The remaining passive components (bypass and decoupling capacitors) were also selected as recommended by the guidelines given by EPC, along with a 1 kΩ @ 100 MHz ferrite bead to protect the 5 V inputs from EM interference.

2.3 Current sensing

The measurement of the current produced by the phases is vital in various applications, as well as for implementing protection logic. Considering the final application, the current measurement will be used for the implementation of Field Oriented Control (FOC) algorithms, which require the current signal of each phase to be fed back to the controller, one essential feature it must provide is current sensing capability. Usually this is done by placing shunt resistors between the output node and the load and measuring the voltage across them. This mode of sensing current can give accurate measurements but, on the other side, it has some drawbacks since it relies on extra components which take up space on the board and have a higher power dissipation with respect to alternative solutions.

Instead, for this project, an integrated solution using Hall effect current sensors was chosen. The GO 20-SME transducers by LEM are excellent for this application as they can measure up to 50 A and provide galvanic separation between the input and output circuits, meeting the isolation requirements specified in section 2.1. Also, these ICs don't need any external components to function, except for the decoupling capacitors which were sized according to the recommendations found in [3].

2.4 Voltage sensing

Voltage sensing is another important feature to have on a motor drive inverter that, while not strictly required as the current sensing, can be very useful especially if sensorless control algorithms are going to be used.[†] The most common way to implement it is to use a resistive divider to scale the phase voltage from tens or hundreds of volts down to 1 V ÷ 5 V, which can then be fed directly to the microcontroller or to an amplifier.

As galvanic isolation of the controller must be guaranteed in this application, the chosen devices for this task are the AMC1350 isolated amplifiers by Texas Instruments, which

[†]Sensorless FOC uses voltage and current sensing to estimate the rotor position instead of measuring it directly with an encoder. It doesn't mean there are no sensors whatsoever.

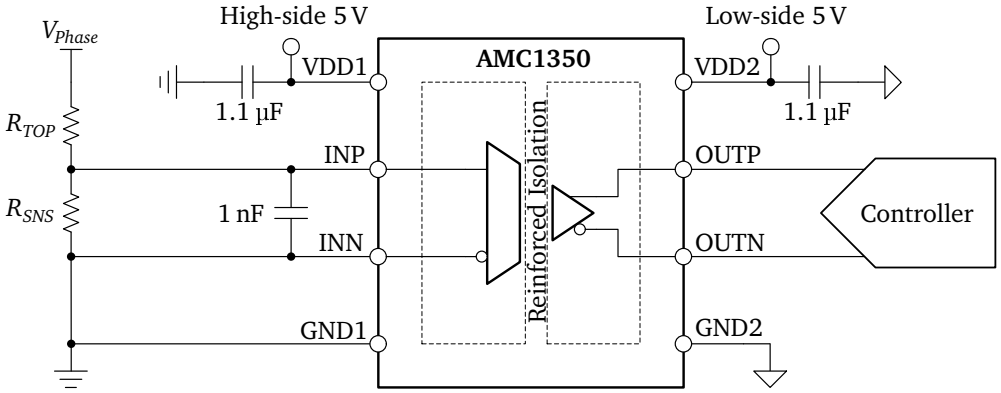


Fig. 2.3: Typical application of the AMC1350 isolated amplifier for phase voltage sensing.

are optimized for accurate voltage sensing in power converters and motor drives. The recommended design procedure [1] for the resistive divider is described below.

First of all, the maximum allowed current through the resistive divider, I_{CROSS}, is imposed. This value should be of at least 100 µA in order to minimize any measurement offset due to the input bias current of the amplifier. In this case, it was chosen so that $I_{CROSS} \leq 1\,\text{mA}$ when the phase output voltage is at its peak, namely when $V_{Phase} = V_{Peak} = 112.9\,\text{V}$. This determines that the total impedance of the resistive divider must be of at least 112.9 kΩ. Considering that the impedance of the divider is dominated by the top resistor (shown as R_{TOP} in Fig. 2.3), the voltage drop across R_{SNS} can be neglected for a short time. R_{TOP} can then be calculated as

$$R_{TOP} = \frac{V_{Peak}}{I_{CROSS}} = 112.9\,\text{k}\Omega \tag{2.1}$$

and the next closest value from the E96 series is $R_{TOP} = 113\,\text{k}\Omega$.

The effective sense resistor value $R_{SNS,eff}$ is the parallel combination of the external resistor R_{SNS} and the input impedance of the AMC1350, R_{IN}. $R_{SNS,eff}$ is sized such that the voltage drop across the impedance at maximum input voltage (112.9 V) equals the linear full-scale input voltage (V_{FSR}) of the AMC1350 (that is, +5 V). By applying the Kirchhoff voltage law, $R_{SNS,eff}$ is calculated as

$$R_{SNS,eff} = V_{FSR}\frac{R_{TOP}}{V_{Peak} - V_{FSR}} = 5.236\,\text{k}\Omega \tag{2.2}$$

In a final step, R_{SNS} is calculated as

$$R_{SNS} = \frac{R_{IN}R_{SNS,eff}}{R_{IN} - R_{SNS,eff}} \tag{2.3}$$

With $R_{IN} = 1.25\,\text{M}\Omega$ (typical value from datasheet), $R_{SNS} = 5.258\,\text{k}\Omega$ and the next closest value from the E96 series is 5.23 kΩ. Ultimately, a 1 nF capacitor is placed across the

input pins of the isolated amplifier to filter the input signals while a parallel combination of 1 µF and 100 nF bypass capacitors is used to filter the voltage at the high-side and low side supply pins (V_{DD1} and V_{DD2} respectively).

2.5 Digital isolators

While the Hall current transducers and the isolated amplifiers take care of the isolation of the analog feedback signals coming from the board, the PWM control signals need to be isolated by the means of a digital isolator. The requirements for such a device in this specific application are quite lax, as almost all digital isolators on the market are capable of at least 1 Mb/s while the PWM input signals are never expected to reach frequencies higher than 250 kHz. The only important aspects to take into account are the compatibility with 5 V logic levels and the number of available channels. In this case, there are seven signals that need to reach the power stages: six PWM inputs (one for the low side and one for the high side for each of the three legs) and one overcurrent detection signal coming from the protection circuits which will be examined in section 2.6.

The devices selected for this task are the ADuM1300 and ADuM1400 by Analog Devices, which combined provide a total of exactly seven isolated digital channels. The only external components required by these ICs are two 100 nF bypass capacitors connected between the supply and ground pins on both the high and low sides of the device as recommended by the datasheets [16, 18].

2.6 Over-current protection

The overcurrent detect circuit included with the EPC9176 [4] was modified to make the intervention threshold adjustable by tuning three multiturn trimmers (one for each phase). This can be useful in a laboratory setting when some particular equipment needs to be protected with a high safety margin (by lowering the threshold) or stress tested (by increasing the threshold).

A simplified schematic of the over-current protection circuit is illustrated in Fig. 2.4. The current measurement signals coming from the LEM transducers are fed to three LMV7235 open-drain comparators that trigger if any of the three phases current measurement exceeds the threshold set by its trimmer. To avoid output bounces due to noise, the

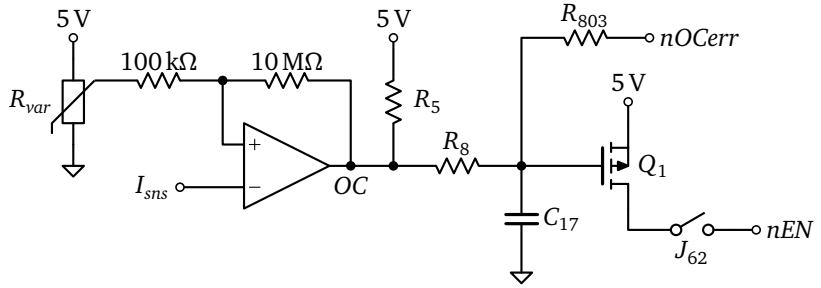


Fig. 2.4: Simplified schematic of the over-current protection circuit (filtering capacitors have been omitted).

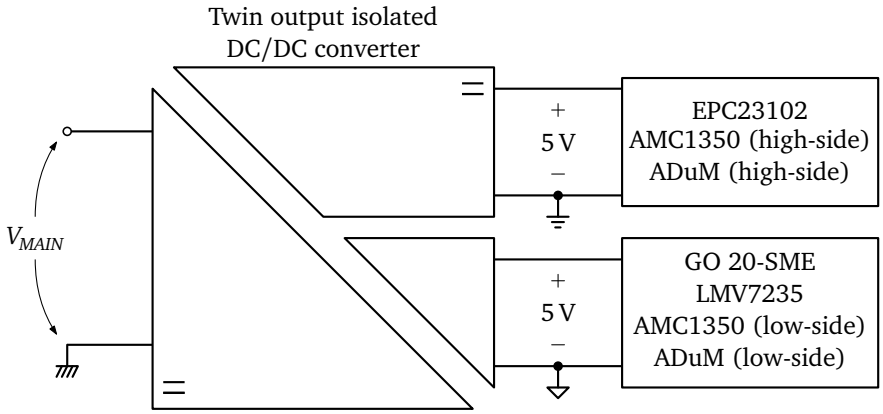


Fig. 2.5: Simplified diagram of the isolated power supply scheme. Bypass capacitors have been omitted for the sake of clarity.

comparators were configured with a 50 mV hysteresis band. All the resistors were sized following the procedures shown in [12].

Once an over-current is triggered, the active low *OC* signal will remain low for a short period of time, determined by the *RC* time constant (10 ms) of $R_5 + R_8$ and C_{17}, and all PWM signals will be disconnected from the eGaN ICs if jumper J_{62} is installed. The *OC* detect signal can be passed on to the controller as *nOCerr* through R_{803}.

2.7 Auxiliary isolated DC/DC converter

All the integrated circuits analyzed in the previous sections have to be powered by a 5 V auxiliary supply in order to function properly. However, to respect the galvanic isolation requirements set in section 2.1, not all the devices can be connected to the same 5 V and ground rails. In particular, the current sensors, the comparators and the low side supply pins of the analog and digital isolators all need to be powered separately from the the power stages and the high side supply pins of the isolated ICs. The relative

ground return paths should be isolated as well. This corresponds to the configuration illustrated by Fig. 2.5.

To this end, a twin output, fully isolated DC/DC converter such as the PRQ3W-Q48-D55-S by CUI comes in handy. This converter provides two separate 5 V rails, each with its own isolated ground pin, and can output power up to 3 W in total, which is more than enough to feed all the low voltage circuits on the board. As usual, bypass capacitors had to be put at the input and output pins following the sizing recommendations found in [15].

Printed circuit board design

3

The layout of the prototype was realized using the EAGLE PCB design software and submitted to Eurocircuits (a PCB manufacturing service) for verification before production. This means that a design with multiple layers is possible, allowing for more flexibility in the routing process. Relying on a service for production also allows for the use of small size component packages (such as the 0603 and 0402 standards) which help keeping the design compact. The final board layout measures 81 × 75 mm, well within the requirements given in section 2.1. The following paragraphs will present some fundamental concepts, which were considered when routing the PCB, and will then analyze the layout procedure in detail, highlighting the most critical aspects of the design. Finally, the last section describes the accessory hardware needed to complete the board, such as the heatsink, standoffs and connectors.

3.1 PCB layout considerations

PCB layout and routing represent the last fundamental steps in the design of electronic devices, which is often iterated further times after the experimental verification of the implemented design, to obtain an optimized final product. It requires knowledge about many aspects that are not at all included in the circuit design part. The most obvious ones, of course, are the parasitic components, but many others are to be kept in mind such as the assembly process and the cooling strategy.

The golden rule to follow when designing PCBs is to replicate as close as possible the layouts suggested by the manufacturers' guidelines for each of the core components on the board, which, for a power converter, are typically the power transistors and other accessory ICs. For the design to be developed, this ensures a reliable starting point, typically accurately devised and tested by the manufacturer of the component (i.e., the most authorative source of information for the use of the component itself). With this in mind, a correct workflow implies doing a preliminary analysis which can be outlined as follows:

1. Identify the various functional blocks of the circuit, such as the switching cells, voltage or current sensing, protection circuits, etc. Usually, these are built around

a specific IC along with the passive components it needs to function. Refer to the application notes and datasheets published by the manufacturers for guidelines when laying out the design of each block.

2. Identify high $\mathrm{d}i/\mathrm{d}t$ current loops and minimize their impact by reducing their size and exploiting the mutual inductance effects [14]. Multi-layer PCB technologies help in this regard by allowing to place the DC bus ground planes directly below the devices on the surface, maximizing the cancellation of stray inductances.

3. Identify high current traces and give each one a proper width, using more stacked layers connected by vias if necessary.

4. Identify high $\mathrm{d}v/\mathrm{d}t$ nodes (such as the switching nodes) and minimize their areas. This is important in order to reduce capacitive coupling and therefore minimize the related undesired effects.

5. Place all bypass capacitors as close as possible to their relative ICs to ensure a low impedance power supply to the ICs and to filter potential EMI coupled to the supply rails.

6. Finally, connect all the finished blocks together with copper traces, placing vias where necessary, considering both electrical and thermal needs.

3.2 Analysis of critical areas

As the final prototype will be produced by a specialized service, the board was designed to be etched on a 4 layer layout. This allows for more room when routing the copper traces and guarantees optimal soldering of even the smallest components. Nevertheless, some components not available for automated assembly by the service will have to be hand-soldered using a heat gun.

The next paragraphs describe in detail the layout and placement of each functional block of the circuit, together with the design choices made along the way.

3.2.1 Switching cells and current sensors

Knowing that the switching cells contain the devices which dissipate the greatest power on the board, it was decided that they should be placed first on the layout, so as to leave enough room around them to accommodate a cooling solution (which will be discussed later in section 3.3). Once the area that will be covered by the heatsink was delimited,

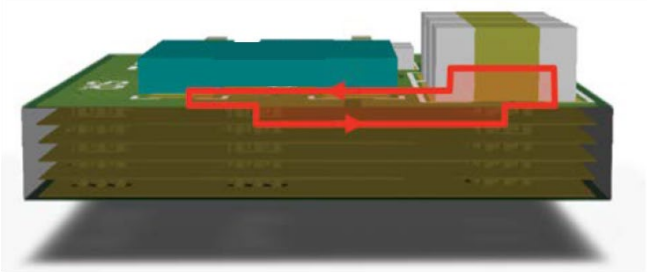


Fig. 3.1: Recommended layout technique to minimize power loop inductance. The eGaN devices are highlighted in blue. Image taken from [5].

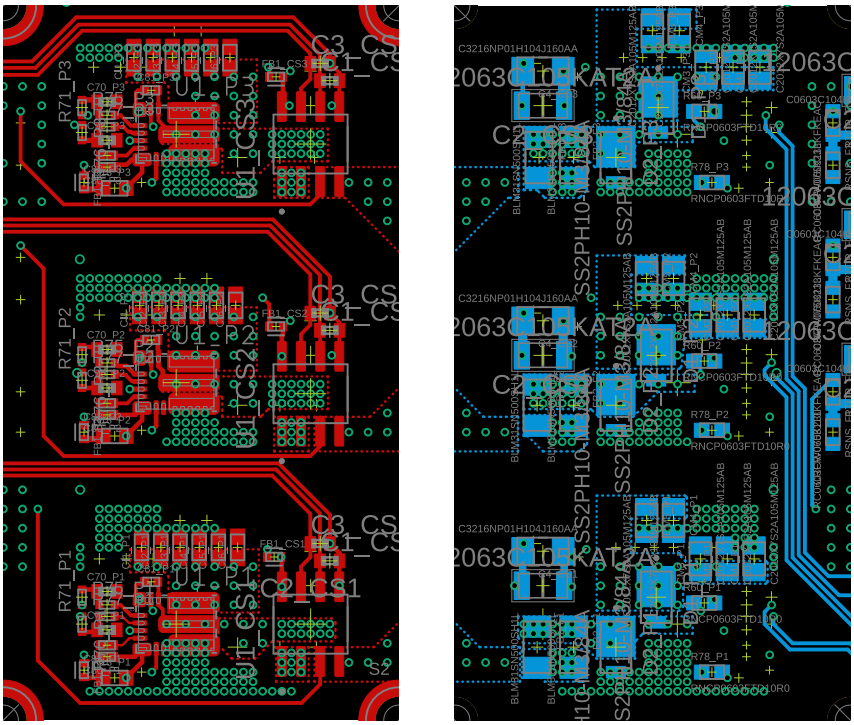
it became possible to arrange the switching cells' layout, making sure that they would sit perfectly within the boundaries of the said area.

Monolithic integration of the half-bridge output HEMTs together with their associated gate drivers significantly reduces parasitic common source inductance and gate drive loop inductance. The only thing left to be optimized by the designer is the high frequency power loop inductance that is determined by the PCB layout of the DC input capacitors in relationship to the current flow direction through the half-bridge power stage.

The layout technique recommended by EPC [5] was closely replicated in the design and is shown in Fig. 3.1.

This PCB layout uses the concept of creating a low-profile magnetic field cancellation loop in a multilayer PCB. The design utilizes the first inner layer connected to the GNDP plane as a power loop return path. Separated only by a thin substrate, the top layer power loop and the first inner layer current return path directly underneath generate opposing magnetic fields with induced currents that have opposite direction. The result is a cancellation of magnetic fields which translates into a reduction in parasitic inductance.

As can be seen from Fig. 3.2a, the switching cell assembly also includes the current sensors. These are placed close to the output pins of the eGaN stages in order to reduce the switching node area, which can introduce $C\,\mathrm{d}v/\mathrm{d}t$ parasitic effects as discussed in paragraph 1.2.1. This is also beneficial from a thermal management standpoint, since the whole phase current has to flow through the transducers which may warm up significantly as a consequence. Placing them close to the switching devices means that they will also be covered by the heat-spreader, which can improve their cooling performance.



(a) Top view **(b)** Bottom view

Fig. 3.2: Switching cells layout. The current sensors can be seen on the left of the top view (a).

3.2.2 Overcurrent protection circuit

Once the switching cells layout and the area covered by the heatsink were defined, the remaining space on the top side of the board was dedicated to the overcurrent protection circuits. This was done to make the potentiometers easily accessible, since they will need to be manually tuned using a screwdriver to adjust the intervention thresholds of the comparators.

3.2.3 Ground planes splitting and isolation

Since one of the key requirements for this design was complete isolation of the controller side of the board, special attention was put in shaping and dividing the different ground and power planes. In fact, the isolated ICs need some empty space to be left between the traces connected to their low-side and high-side pins in order to ensure proper isolation. The dual output isolated DC/DC converter used in this project defines three different ground nodes:

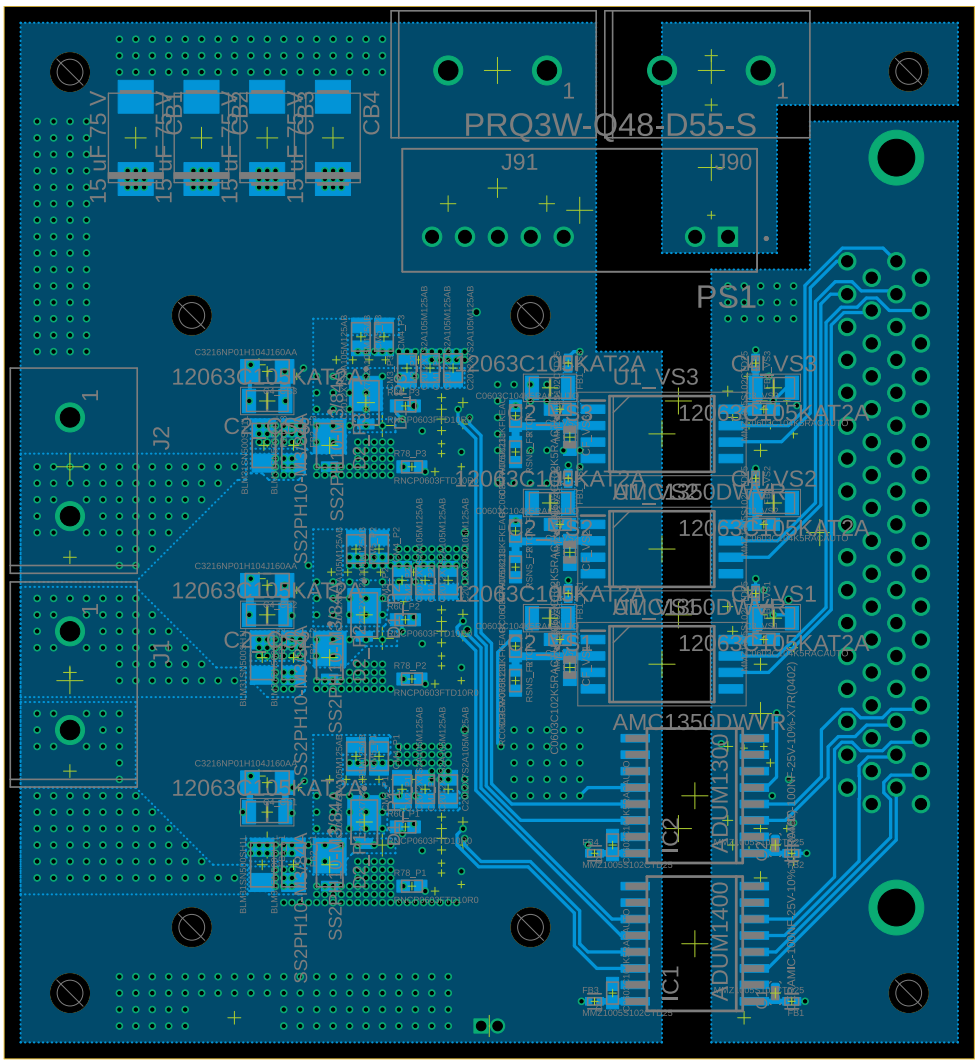


Fig. 3.3: Ground planes layout as seen from the bottom side of the board. Notice the insulation gaps on the right and the isolated devices placed across them. The same layout is replicated on all of the four layers.

- the first one is connected to the main power supply (VMAIN) and is denoted as EARTH in the schematic (see Fig. A.5 for reference);
- the second one, denoted as GND, serves as the reference point for the signals going from the control board to the digital isolators and from the sensing ICs to the controller;
- the third one, denoted as GNDP, is the DC bus ground and also acts as the reference point for the logic signals between the digital isolators and the power stages.

The ground planes corresponding to these reference nodes were shaped so as to define the three regions highlighted in Fig. 3.3. These are insulated by gaps with a thickness

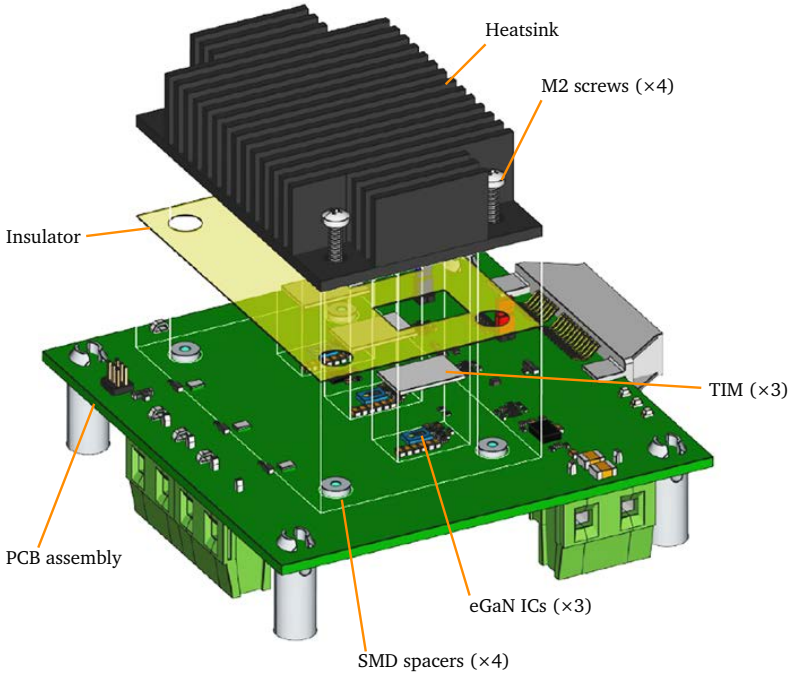


Fig. 3.4: Details for attaching a heatsink to the board.

never less than 1.27 mm on the narrowest sides and around 4-6 mm wide along most of their perimeter.

Given that there was no more space left on top of the board, all the isolated amplifiers, digital isolators and the DC/DC converter had to be placed on the bottom side. These devices are positioned so that they sit across the insulation gaps.

3.3 Thermal management

To improve the heat dissipation from the eGaN ICs and exploit the nominal current capacity of the devices, the cooling solution suggested by the EPC9176 evaluation board [4] was retained for this project.

The board is equipped with four mechanical spacers (S1, S2, S3, S4) that can be used to easily attach a cooler as shown in Fig. 3.4, and only a thermal interface material (TIM), a heatsink, and screws are required.

The heatsink is held in place using screws that fasten to the mechanical spacers which will accept 6 mm long M2 × 0.4 mm thread screws such as McMasterCarr 95836A109.

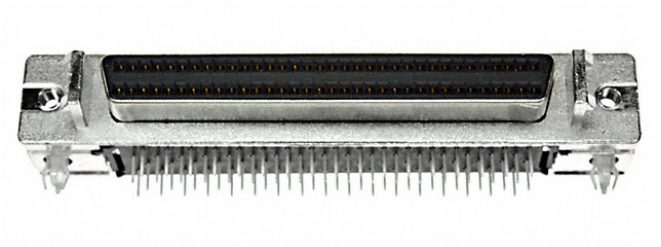


Fig. 3.5: HD-68 female plug used for connection with the control platform.

When assembling the heatsink, it is necessary to add a thin insulating layer to prevent the heat-spreader (which is connected to GNDP) from short circuiting with components that have exposed conductors such as capacitors and resistors. The insulator must provide rectangular openings to allow the TIM to be placed over the ICs to be cooled. An insulator sheet material suitable for this purpose is made by Laird with part number A14692-30 Tgard K52 and a thickness of 0.051 mm.

The TIM suggested by the EPC guidelines is made by t-Global Technology, measures $20 \times 20 \times 0.5$ mm thick with part number TG-A6200-20-20-0.5.

The natural convection cooling heatsink used for this board is a Wakefield-Vette, model 547-95AB.

3.4 Test points and connectors

The board comprises a total of eight Keystone 5015 hookup SMD test points for added convenience when using oscilloscope probes during experiments and set-up. The reference nodes GND and GNDP are exposed through TP4 and TP8 respectively. TP1, TP2 and TP3 should be used to check the overcurrent protection thresholds set by the trimmers. The output phase voltages can also be measured by hooking up probes to TP5, TP6 and TP7.

Connections for the power supplies and to the motor phases are provided by four screw type terminal blocks (J90, J91 and J1, J2 respectively).

A 68 pin high-density D-Subminiature plug is provided to interface the board with a controller. It was cabled according to the pinout indicated by the user manual for the PXI-7854R [13], but it can also be used with a dSPACE MicroLabBox by means of a custom built connection cable.

Conclusions

4

This thesis explored all the critical steps involved in the realization of a three phase inverter for e-Bike motors using GaN power devices. A prototype based on the design examined in the previous chapters will be produced and will be available for testing at the Power Electronics and Electric Drives laboratories at the university of Padova.

Further possible developments on this project following the production phase include a preliminary testing phase, a selection of the optimal drive currents and dead times and the deployment of field control algorithms to drive motors employing the on-board voltage and current sensing.

The design could also be expanded by including a microcontroller and an encoder interface on the board to make it a completely stand-alone solution which could be installed on an actual bicycle. It could also be adapted to work with an Arduino (or some other cheap microcontroller) to be used in a teaching environment thanks to its small dimensions and reinforced design.

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List of Figures

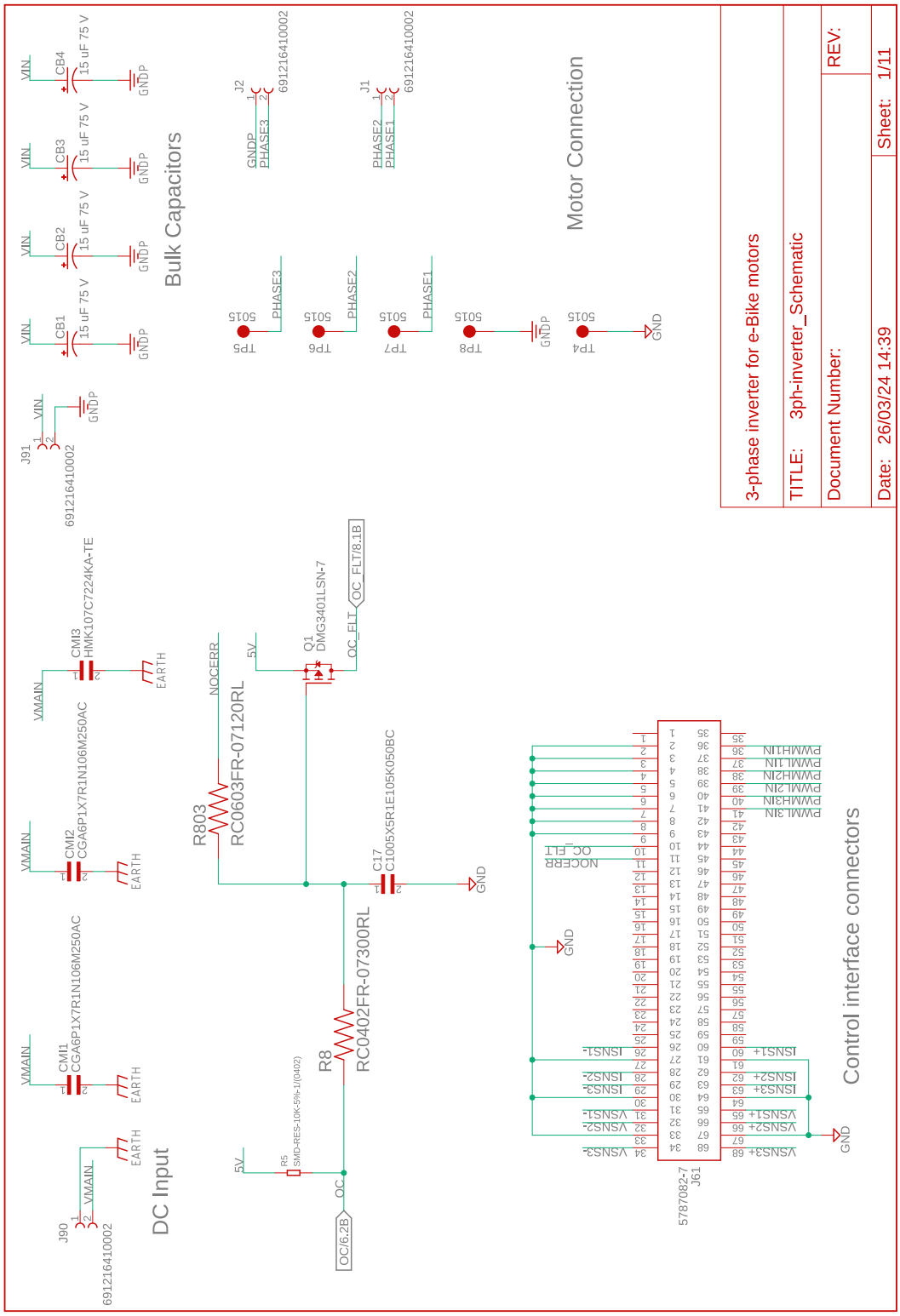

Fig. A.1: Main test points, bulk capacitors and connectors for power supplies, motor phases and controller boards.

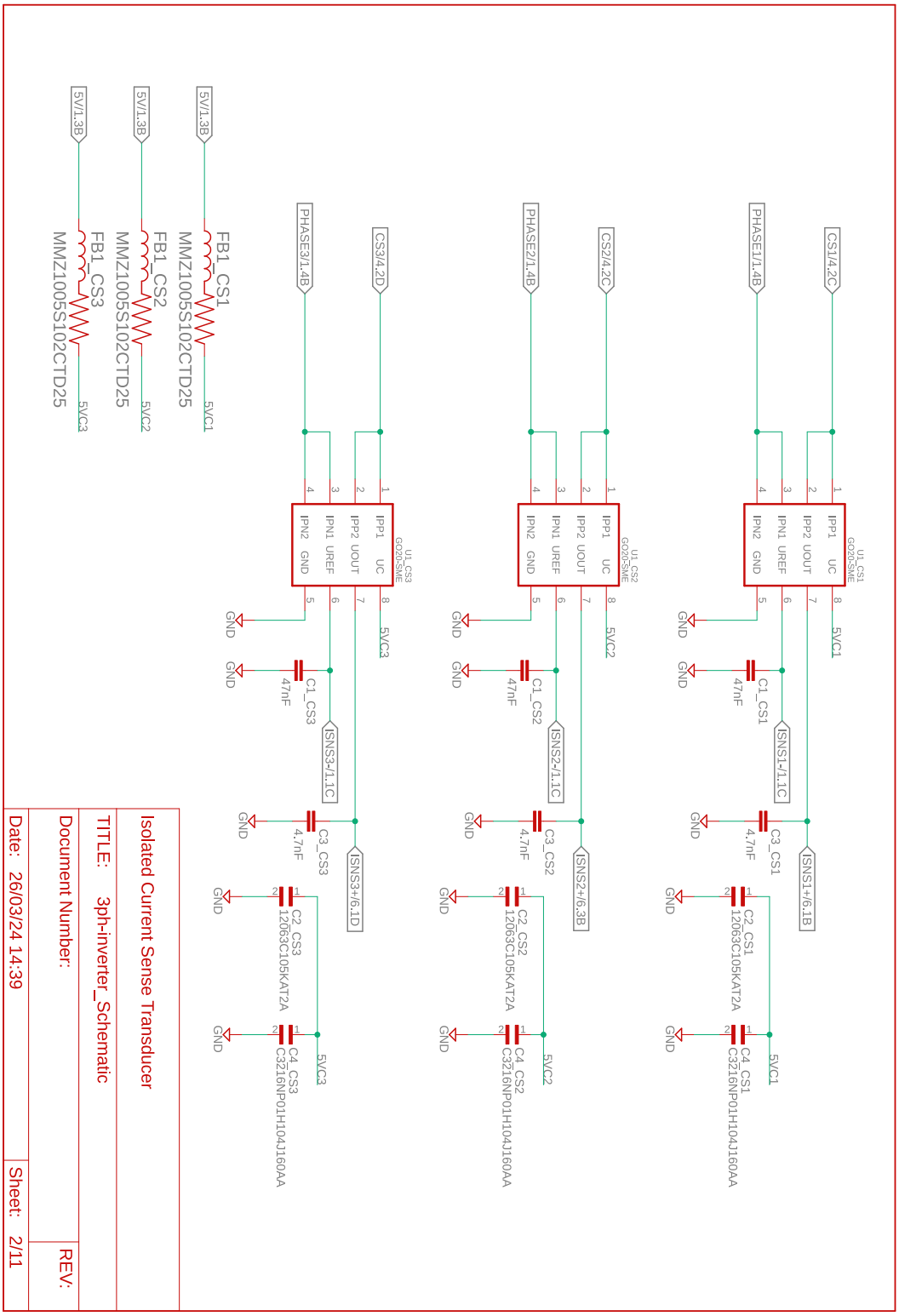

Fig. A.2: Current sensing circuit using Hall effect transducers.

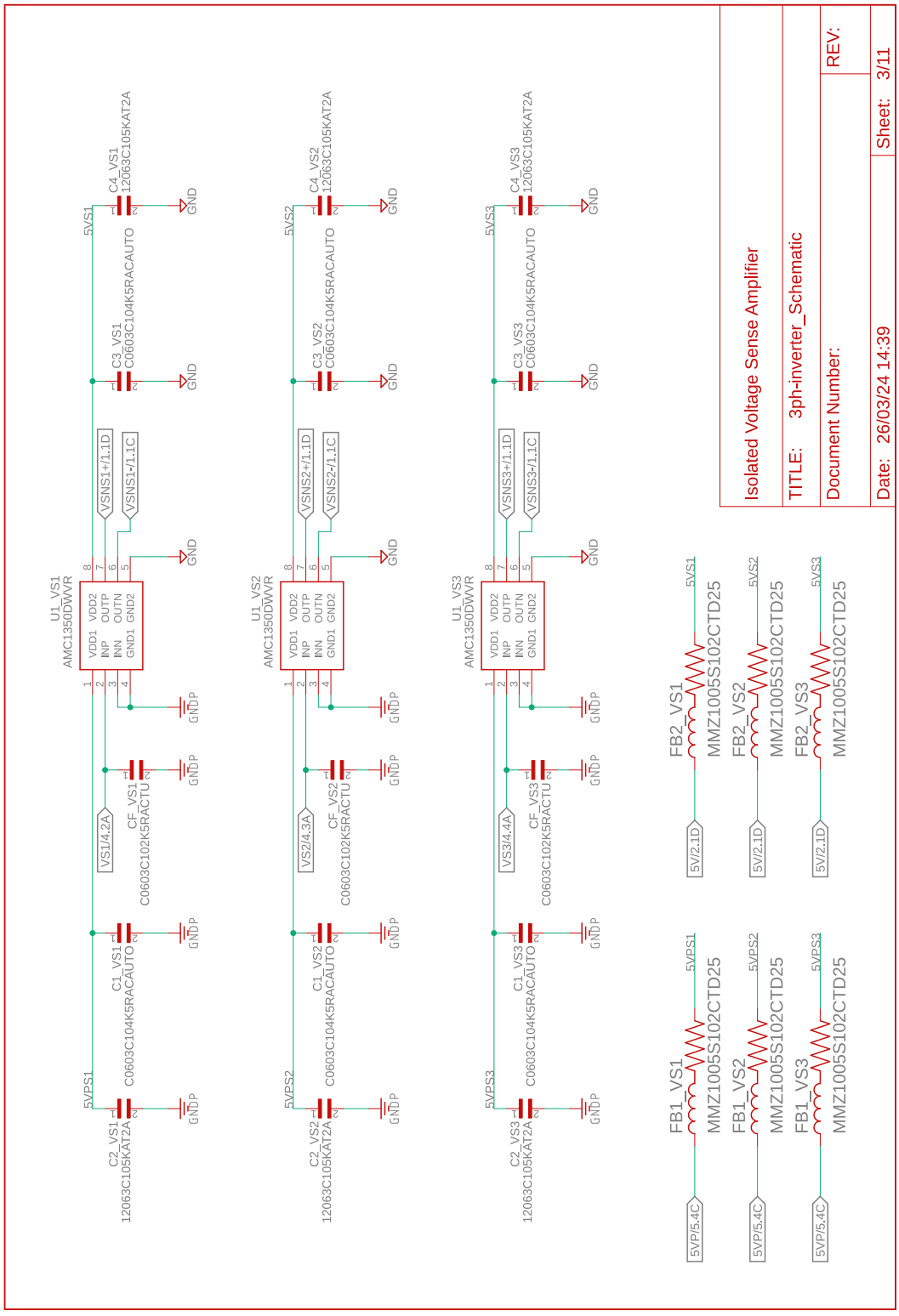

Fig. A.3: Isolated voltage sensing circuit.

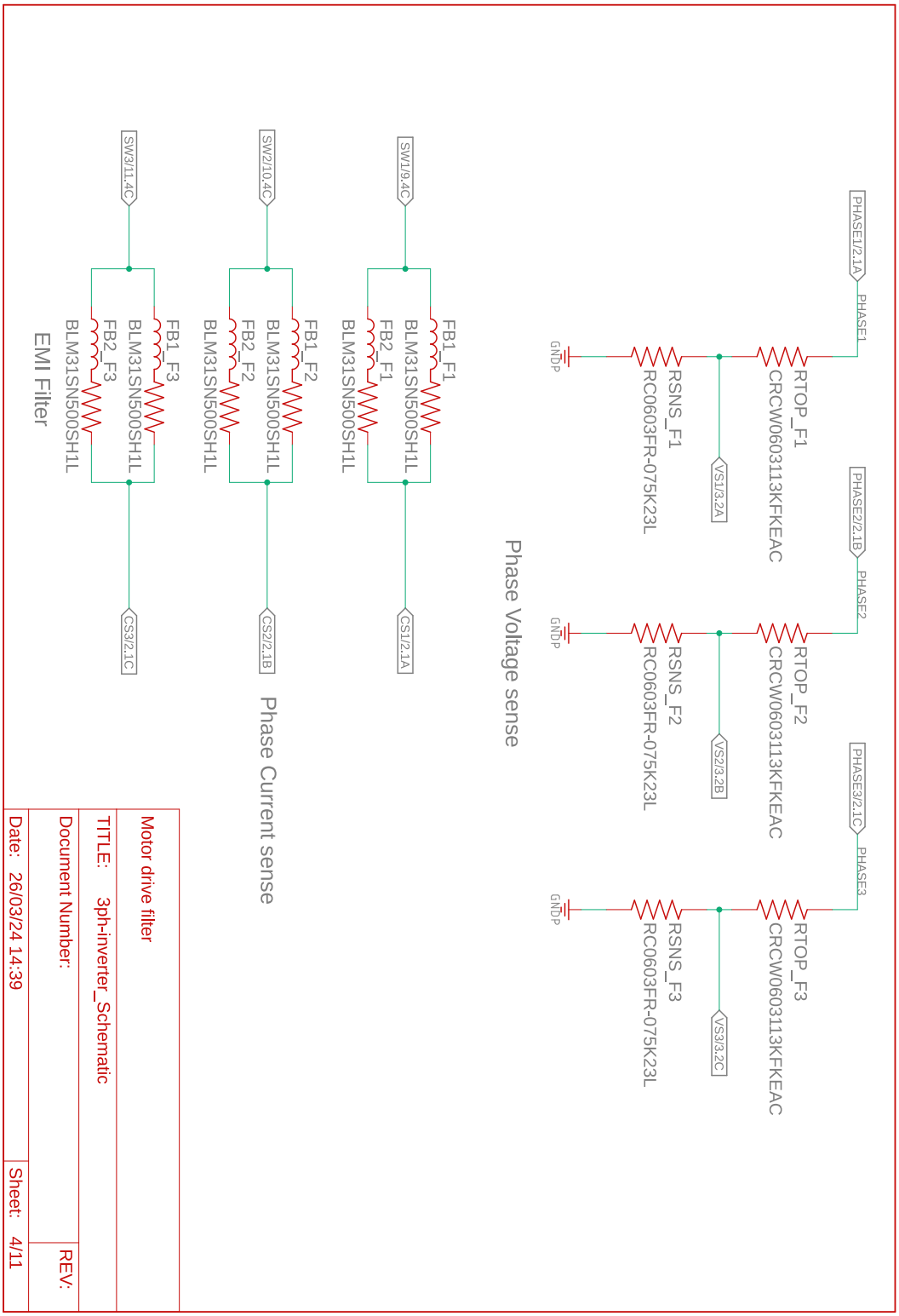

Fig. A.4: Output current filters and phase voltage sensing resistive dividers.

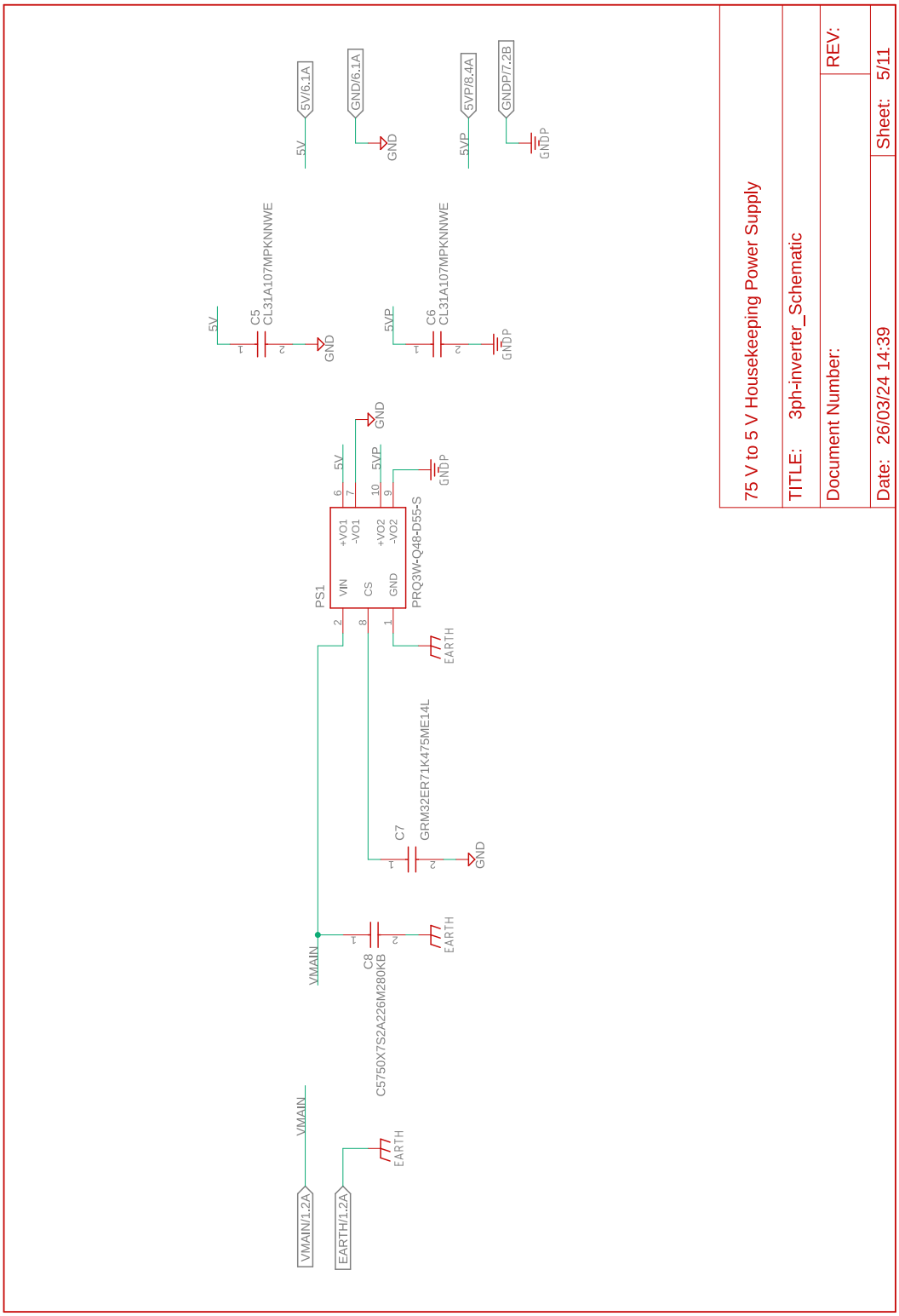

Fig. A.5: Twin output auxiliary isolated DC/DC converter.

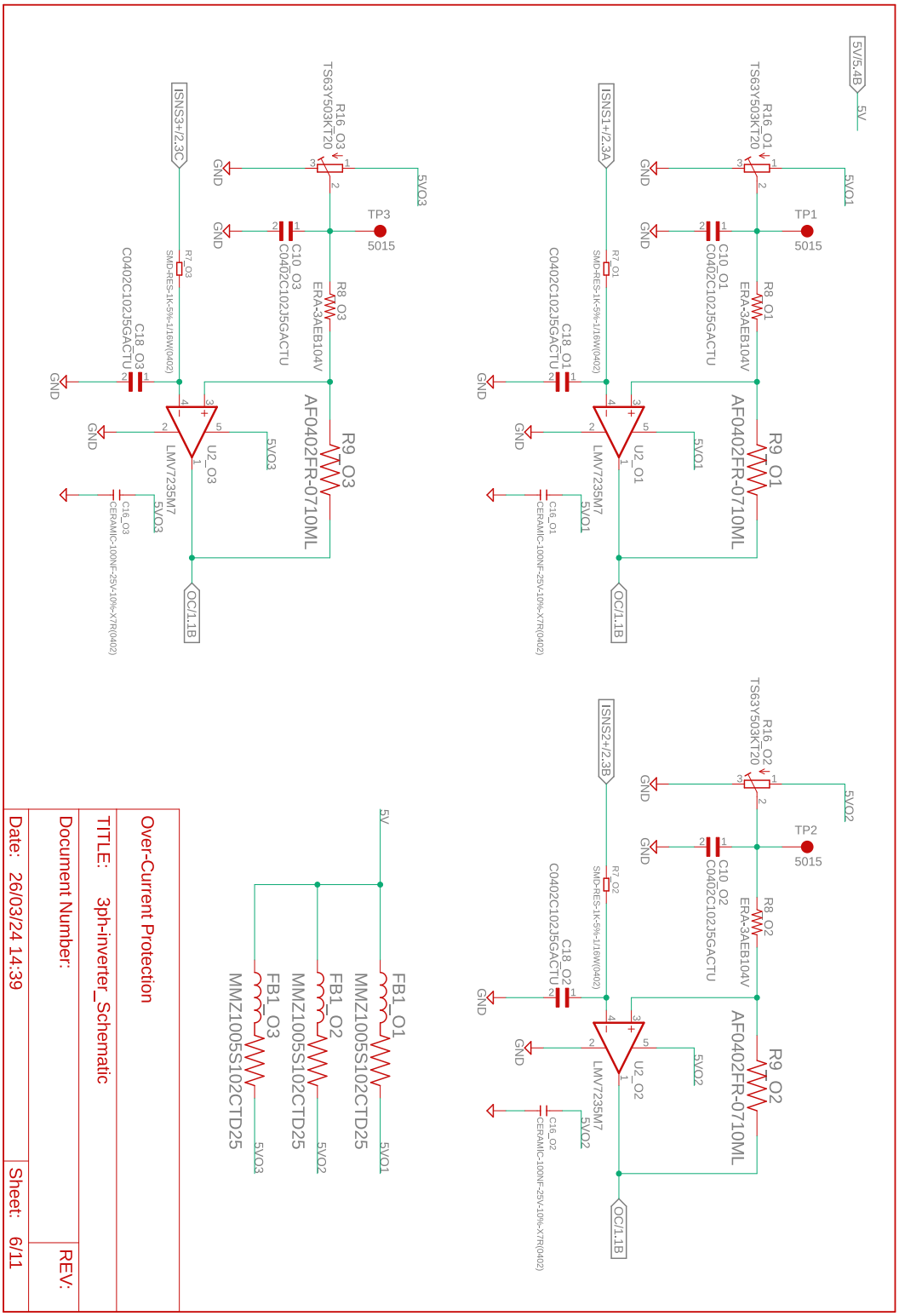

Fig. A.6: Adjustable overcurrent protection circuit.

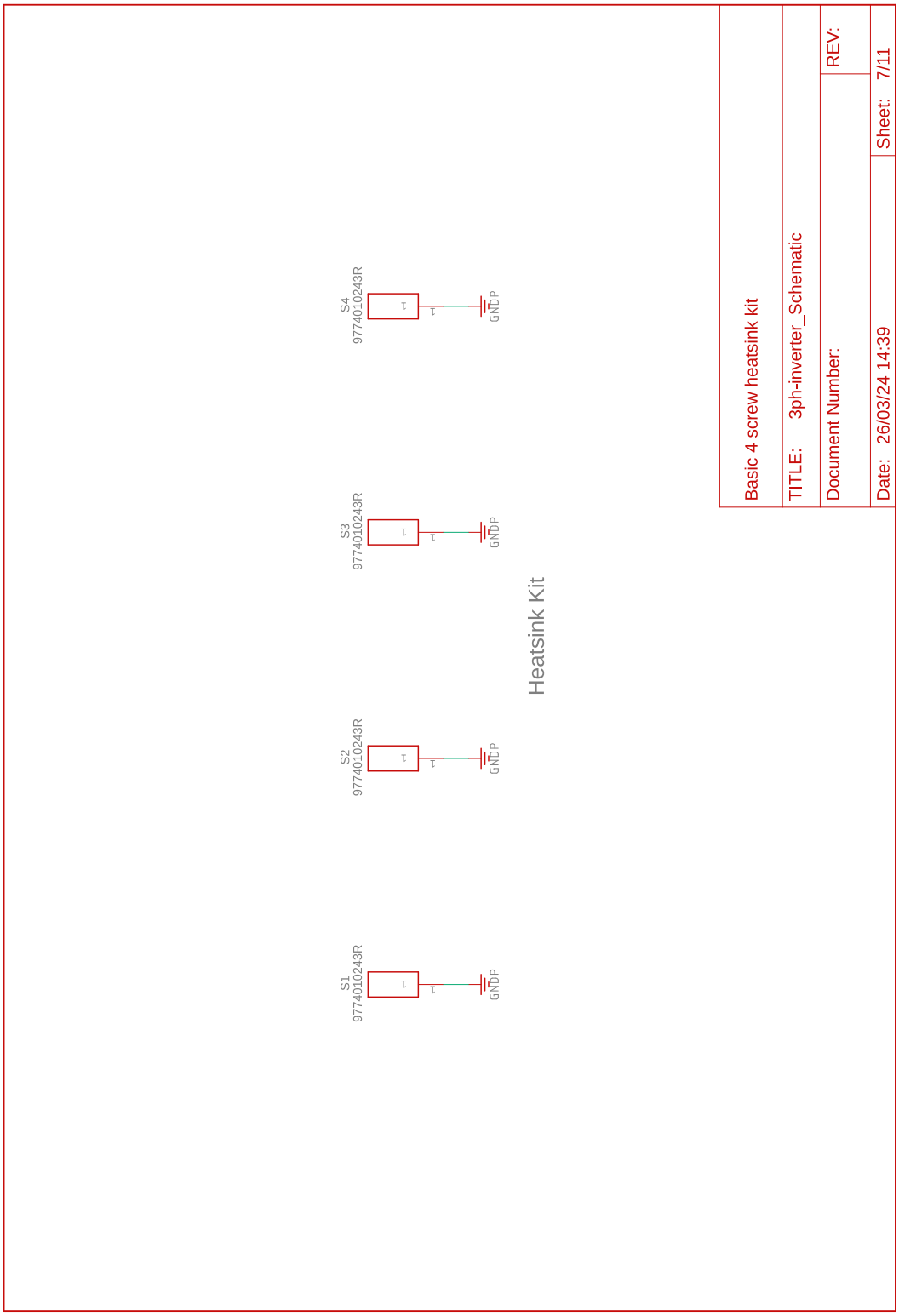

Fig. A.7: Heatsink mounting standoffs.

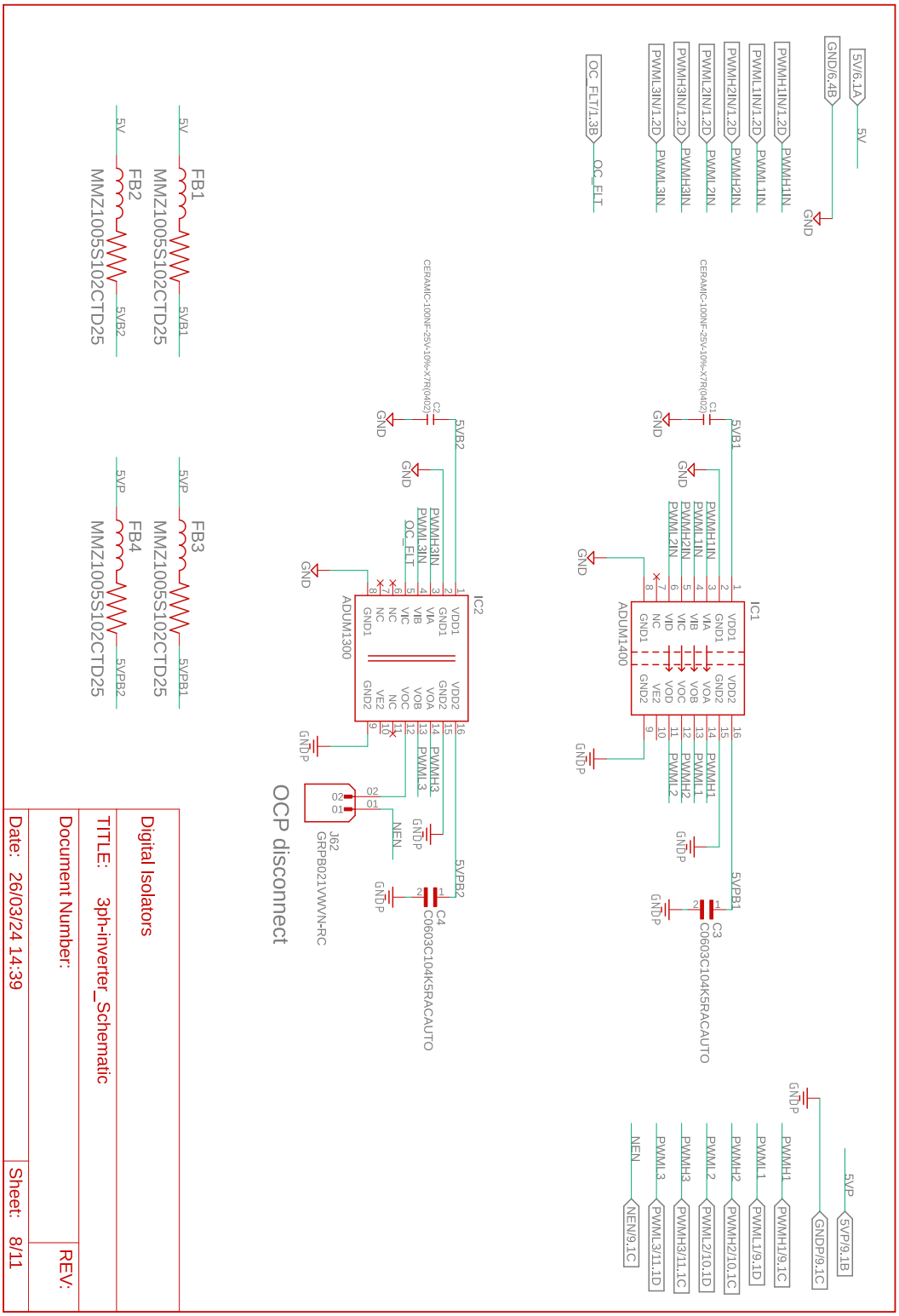

Fig. A.8: Digital isolators with OCP disconnect jumper.

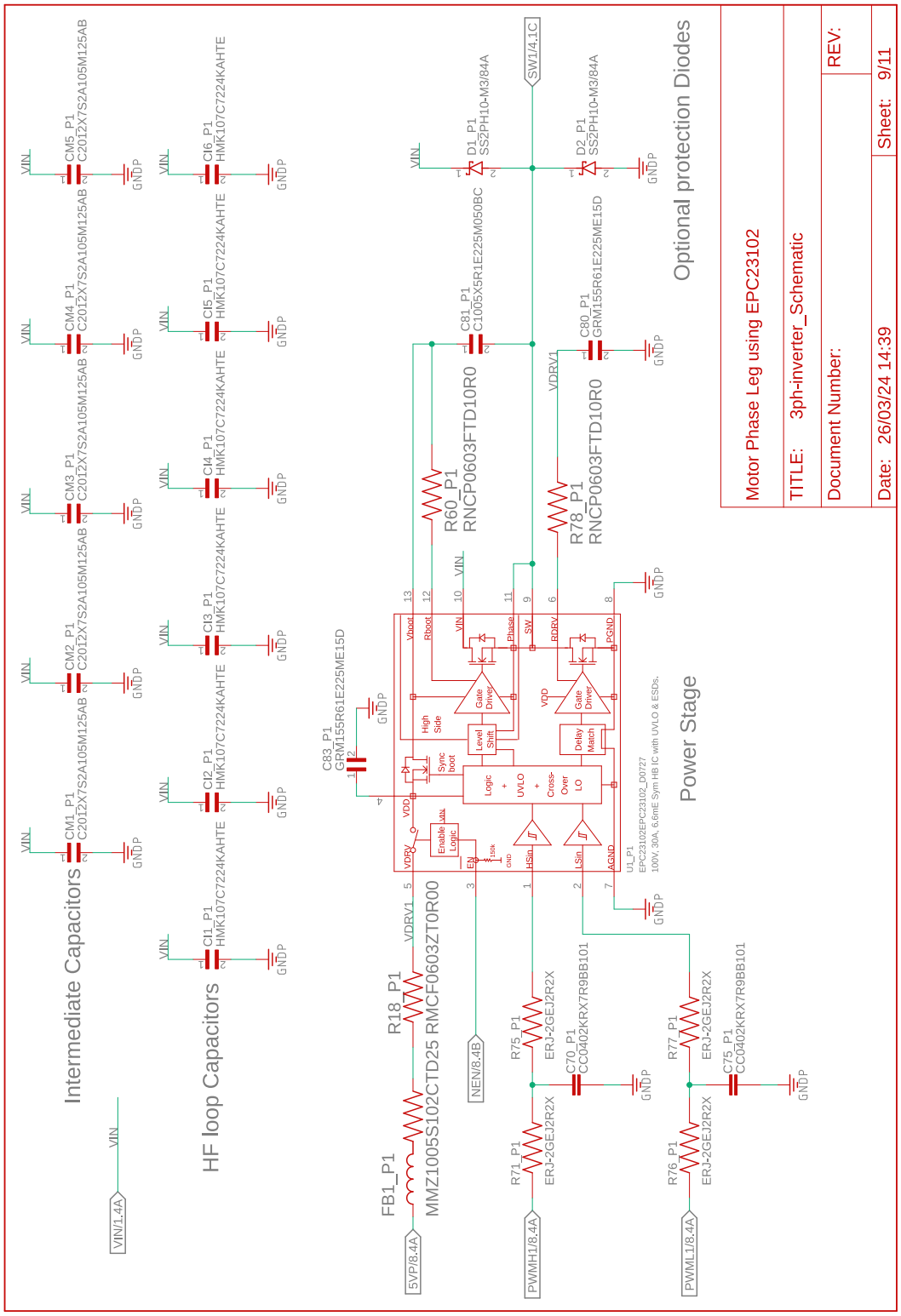

Fig. A.9: Motor phase leg 1 using EPC23102 eGaN power stage.

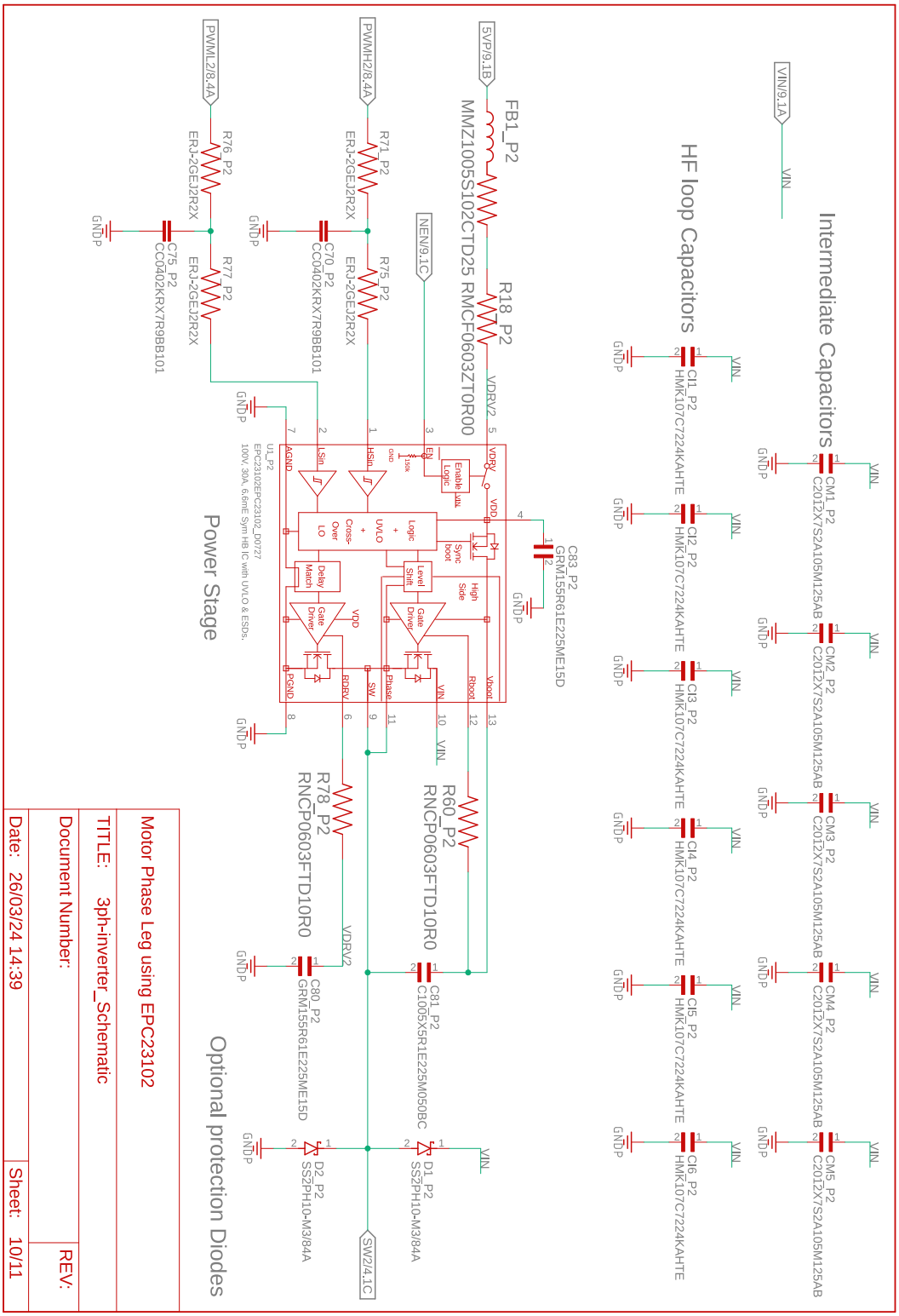

Fig. A.10: Motor phase leg 2 using EPC23102 eGaN power stage.

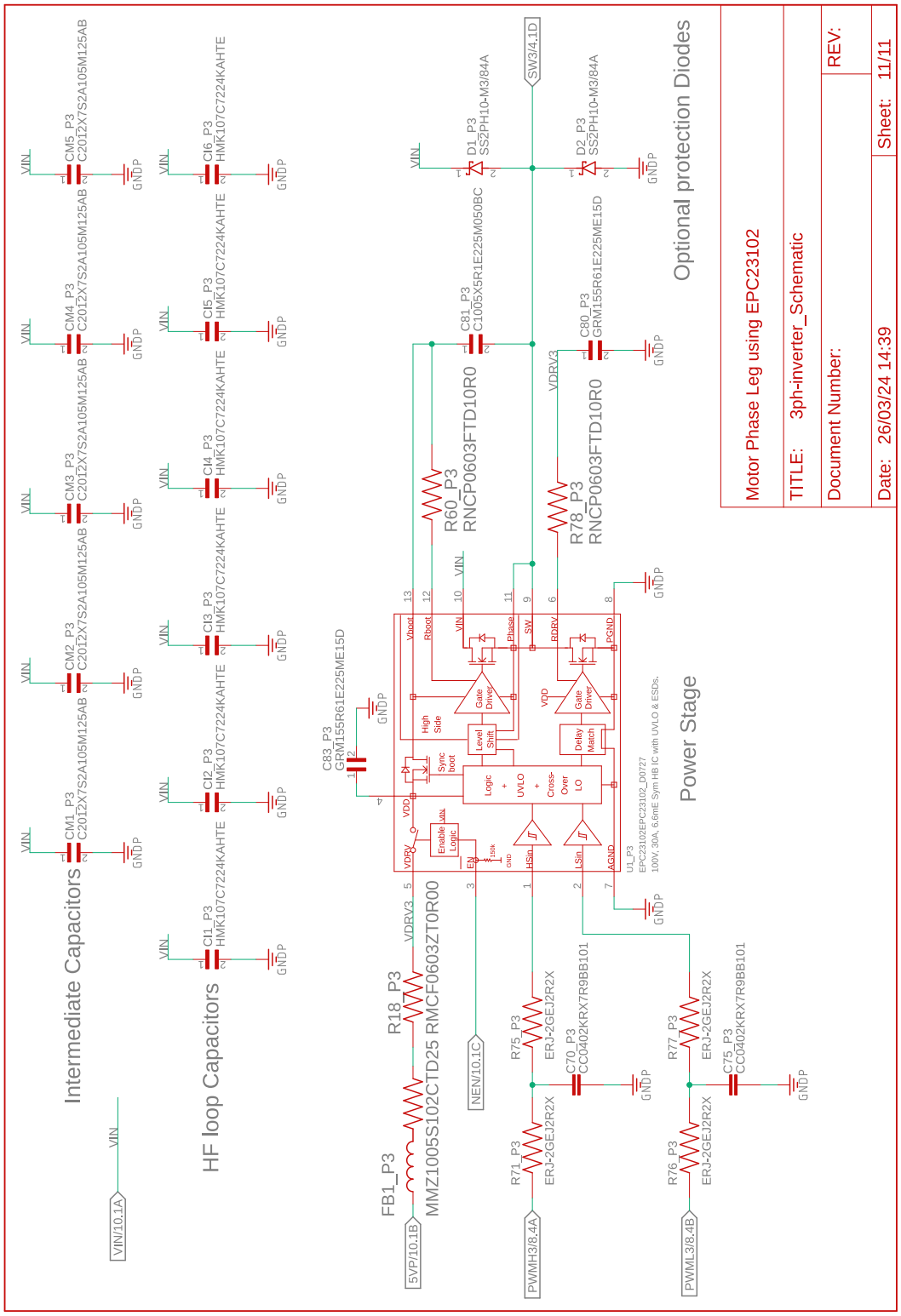

Fig. A.11: Motor phase leg 3 using EPC23102 eGaN power stage.

Layout

B

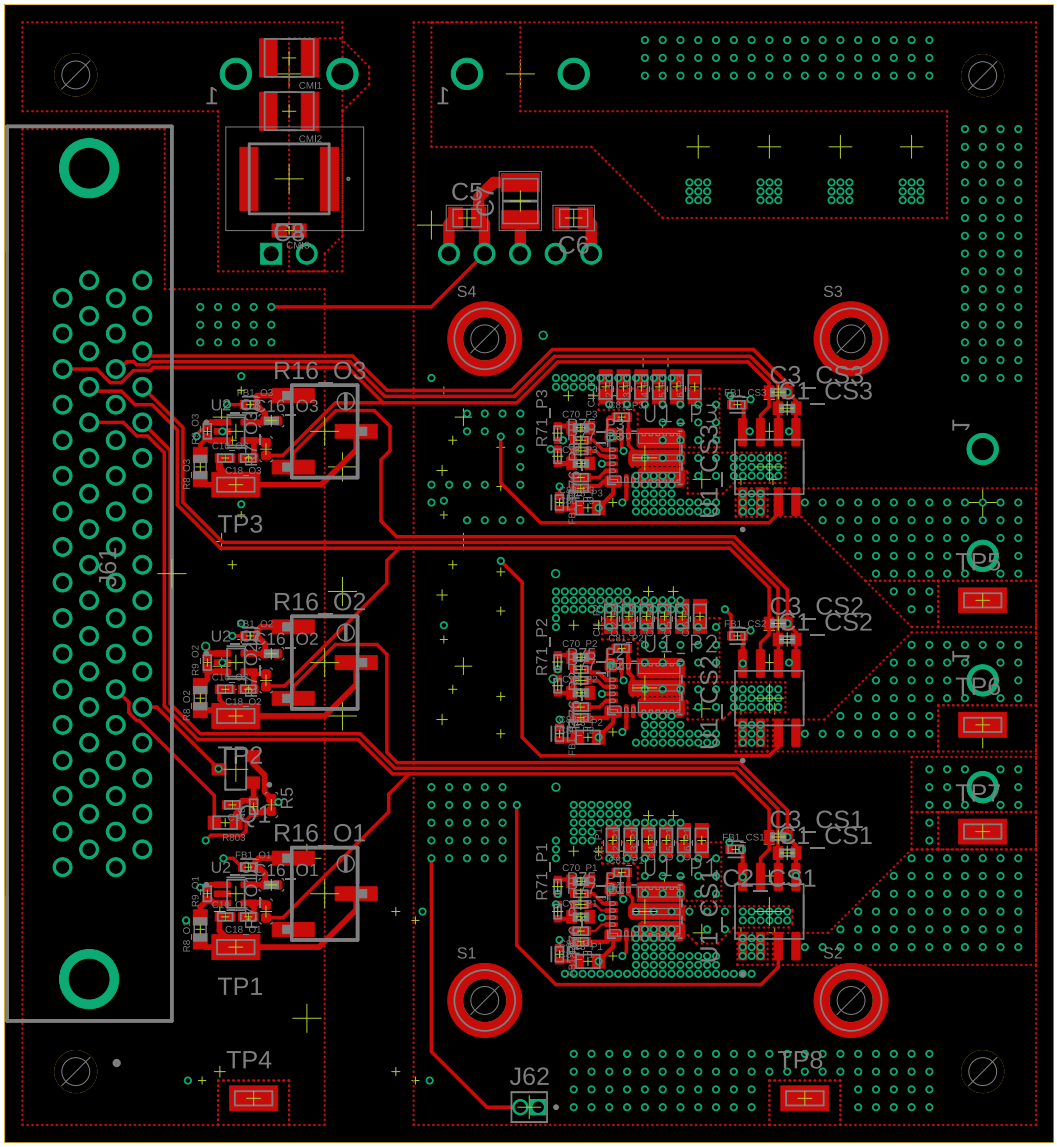

Fig. B.1: Top layer of the PCB hosting the power stage ICs, the OCP circuits and the HD-68 connector.

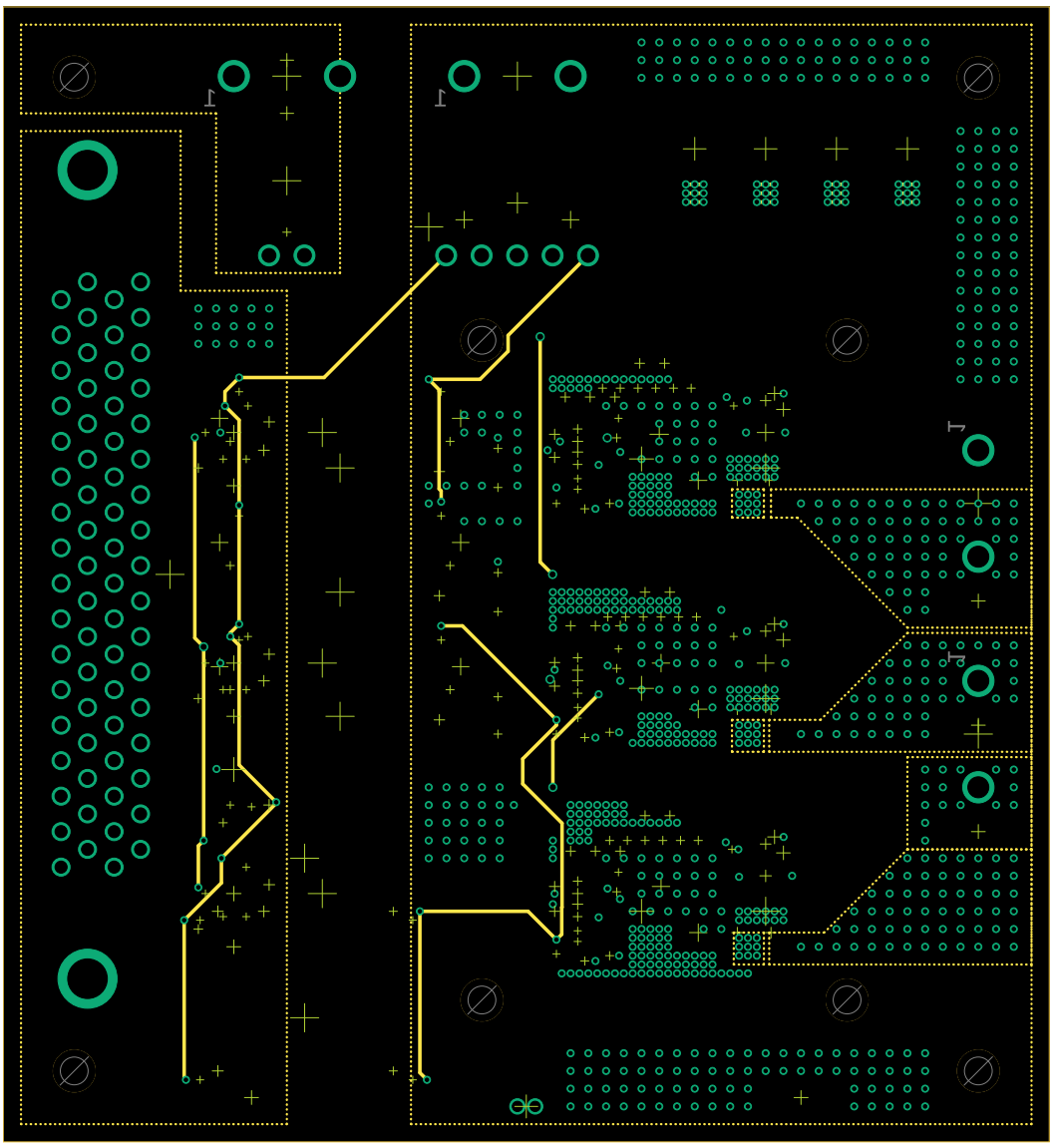

Fig. B.2: Second layer hosting the DC bus ground return plane.

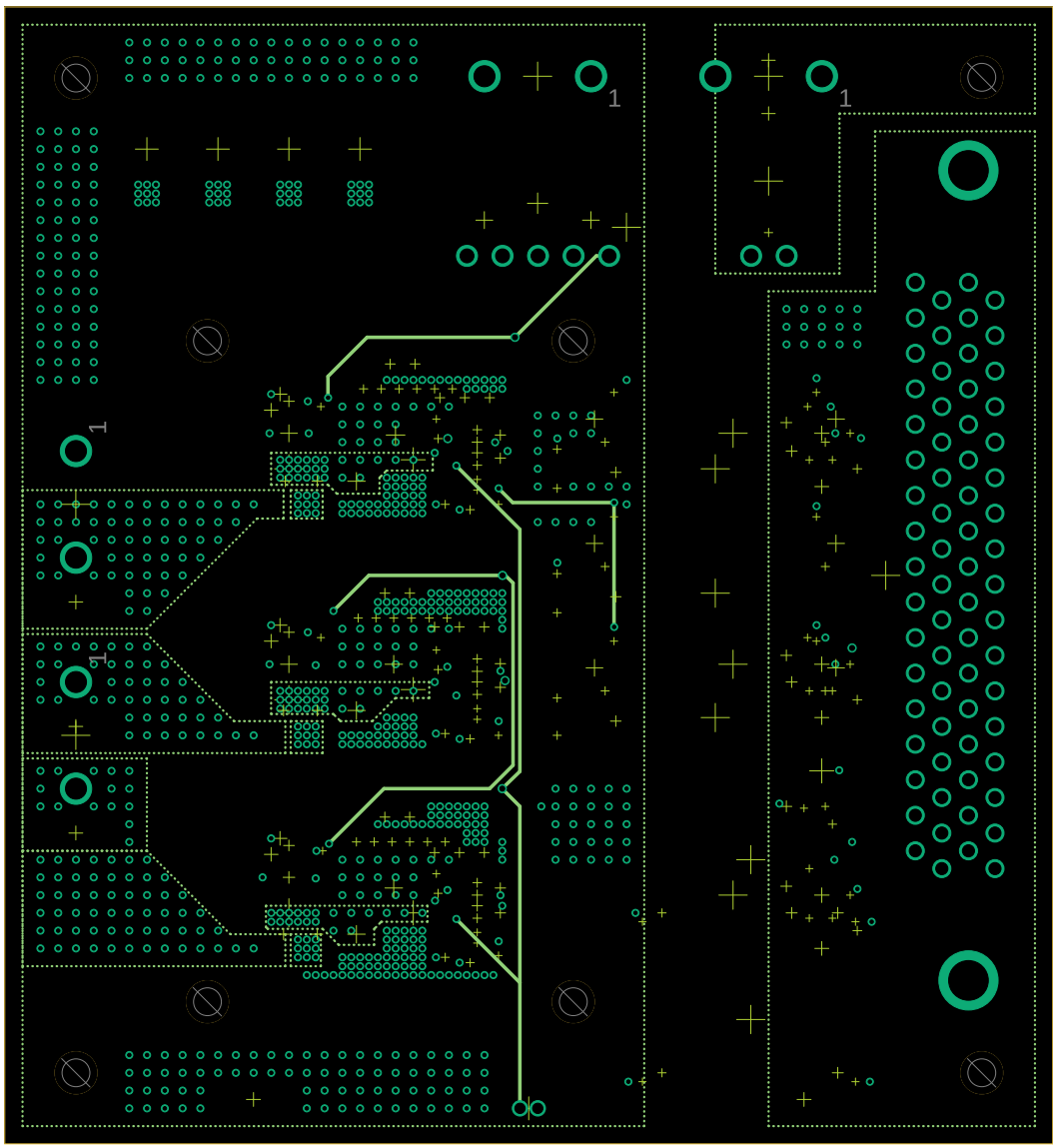

Fig. B.3: Third layer hosting the DC bus power plane.

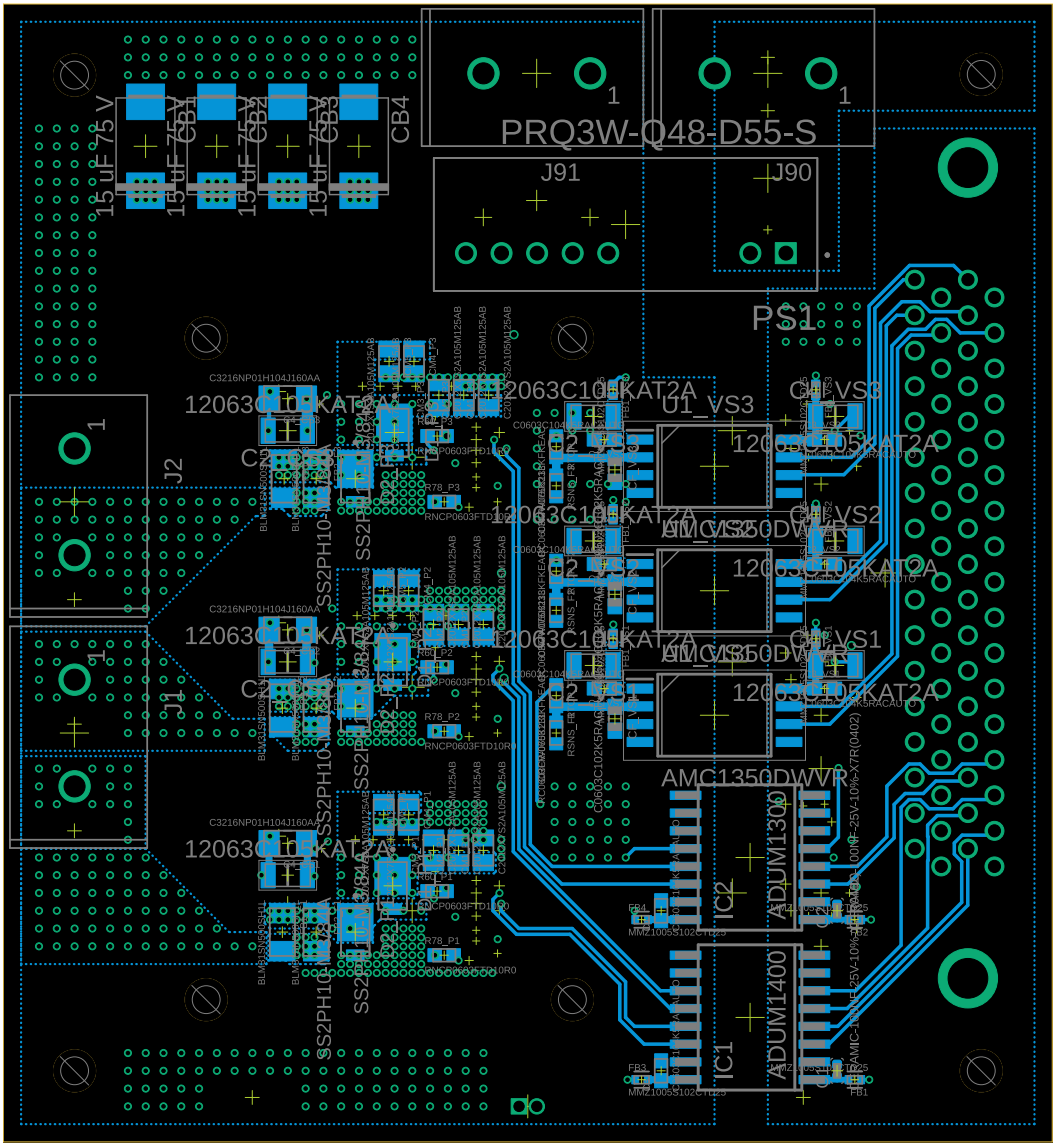

Fig. B.4: Bottom layer of the PCB hosting the screw type terminal blocks, bulk capacitors, isolated ICs and twin isolated DC/DC converter.

Bill of materials

C

Comment	Designator	Footprint
4.7 nF	C3_CS1 C3_CS2 C3_CS3	C0402
15 uF 75 V	CB1 CB2 CB3 CB4	D/7343-31R
47 nF	C1_CS1 C1_CS2 C1_CS3	C0402
5015	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	KEYSTONE_5015
12063C105KAT2A	C2_CS1 C2_CS2 C2_CS3 C2_VS1 C2_VS2 C2_VS3 C4_VS1 C4_VS2 C4_VS3	CAPC3216X178N
5787082-7	J61	5787082-7_1
691216410002	J1 J2 J90 J91	691216410002
9774010243R	S1 S2 S3 S4	WE_9774010243R
ADUM1300	IC2	SO-16W
ADUM1400	IC1	SO16W
AF0402FR-0710ML	R9_O1 R9_O2 R9_O3	RESC1005X37N
AMC1350DWVR	U1_VS1 U1_VS2 U1_VS3	SOIC127P1150X280-8N
BLM31SN500SH1L	FB1_F1 FB1_F2 FB1_F3 FB2_F1 FB2_F2 FB2_F3	BEADC3216X130N
C0402C102J5GACTU	C10_O1 C10_O2 C10_O3 C18_O1 C18_O2 C18_O3	CAPC1005X55N
C0603C102K5RACTU	CF_VS1 CF_VS2 CF_VS3	CAPC1608X90

Comment	Designator	Footprint
C0603C104K5RACAUTO	C1_VS1 C1_VS2 C1_VS3 C3 C3_VS1 C3_VS2 C3_VS3 C4	CAPC1608X90N
C1005X5R1E105K050BC	C17	CAPC1005X55N
C1005X5R1E225M050BC	C81_P1 C81_P2 C81_P3	CAPC1005X60N
C2012X7S2A105M125AB	CM1_P1 CM1_P2 CM1_P3 CM2_P1 CM2_P2 CM2_P3 CM3_P1 CM3_P2 CM3_P3 CM4_P1 CM4_P2 CM4_P3 CM5_P1 CM5_P2 CM5_P3	CAPC2012X145N
C3216NP01H104J160AA	C4_CS1 C4_CS2 C4_CS3	CAPC3216X180N
C5750X7S2A226M280KB	C8	C5750_COMMERCIAL
CC0402KRX7R8BB104	C1 C2 C16_O1 C16_O2 C16_O3	C0402
CC0402KRX7R9BB101	C70_P1 C70_P2 C70_P3 C75_P1 C75_P2 C75_P3	CAPC1005X60
CGA6P1X7R1N106M250AC	CMI1 CMI2	CAPC3225X280N
CL31A107MPKNNWE	C5 C6	CAPC2012X150N
CRCW0603113KFKEAC	RTOP_F1 RTOP_F2 RTOP_F3	RESC1608X55N
DMG3401LSN-7	Q1	TRANS_SSM3J325F LF
EPC23102	U1_P1 U1_P2 U1_P3	D0727
ERA-3AEB104V	R8_O1 R8_O2 R8_O3	RESC1608X55
ERJ-2GEJ2R2X	R71_P1 R71_P2 R71_P3 R75_P1 R75_P2 R75_P3 R76_P1 R76_P2 R76_P3 R77_P1 R77_P2 R77_P3	RES_ERJ-2GEJ2R2X

Comment	Designator	Footprint
GO20-SME	U1_CS1 U1_CS2 U1_CS3	SOIC127P600X175-8N
GRM32ER71K475ME14L	C7	CAPC3225X270N
GRM155R61E225ME15D	C80_P1 C80_P2 C80_P3 C83_P1 C83_P2 C83_P3	CAPC1005X55N
GRPB021VWVN-RC	J62	SULLINS_GRPB021VWVN-RC
HMK107C7224KA-TE	CMI3	CAPC1608X90N
HMK107C7224KAHTE	CI1_P1 CI1_P2 CI1_P3 CI2_P1 CI2_P2 CI2_P3 CI3_P1 CI3_P2 CI3_P3 CI4_P1 CI4_P2 CI4_P3 CI5_P1 CI5_P2 CI5_P3 CI6_P1 CI6_P2 CI6_P3	CAPC1608X90N
LMV7235M7	U2_O1 U2_O2 U2_O3	SOT65P210X110-5N
MMZ1005S102CTD25	FB1 FB1_CS1 FB1_CS2 FB1_CS3 FB1_O1 FB1_O2 FB1_O3 FB1_P1 FB1_P2 FB1_P3 FB1_VS1 FB1_VS2 FB1_VS3 FB2 FB2_VS1 FB2_VS2 FB2_VS3 FB3 FB4	BEADC1005X50N
PRQ3W-Q48-D55-S	PS1	CONV_PRQ3W-Q48-D55-S
RC0402FR-07300RL	R8	RESC1005X40N
RC0402JR-071KL	R7_O1 R7_O2 R7_O3	R0402
RC0402JR-0710KL	R5	R0402
RC0603FR-075K23L	RSNS_F1 RSNS_F2 RSNS_F3	RESC1608X55N
RC0603FR-07120RL	R803	RESC1608X55N

Comment	Designator	Footprint
RMCF0603ZT0R00	R18_P1 R18_P2 R18_P3	RESC1508X55N
RNCP0603FTD10R0	R60_P1 R60_P2 R60_P3 R78_P1 R78_P2 R78_P3	RESC1508X50N
SS2PH10-M3/84A	D1_P1 D1_P2 D1_P3 D2_P1 D2_P2 D2_P3	DIO_SS2PH10-M3/84A
TS63Y503KT20	R16_O1 R16_O2 R16_O3	RTRIMTS63Y

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