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Degradation and Dose-Rate Dependence  
in Decanometer MOSFETs Exposed to  
Ultra-High Levels of Total Ionizing Dose

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# Degradation and Dose-Rate Dependence in Decananometer MOSFETs Exposed to Ultra-High Levels of Total Ionizing Dose

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## Abstract

The main experiment performed in this thesis is called “Low Dose-Rate Sensitivity”, an analysis conducted on 65-nm technology node, intended to be implemented in most of the circuitry for CERN HL-LHC (High Luminosity - Large Hadron Collider) upgrade. The dose-rate (DR) is the dose absorbed per unit of time. If the DR is integrated over the irradiation time, then the Total Ionizing Dose (TID) deposited is obtained. The electronic components mostly affected by ionizing radiation, belonging to CMS and ATLAS detectors, are expected to reach TIDs up to 1 Grad(SiO<sub>2</sub>) in 10 years. The relative dose-rate is therefore around 0.01 Mrad(SiO<sub>2</sub>)/h. In the standard radiation assurance procedures, the devices are irradiated with dose-rates in the order of 10 Mrad(SiO<sub>2</sub>)/h, which are 1000 times higher than the real faced one. BJT are strongly sensitive to the changes in the DR, in what is called Extremely Low Dose Rate Sensitivity (ELDRS). In practice, for the same level of TID, low dose-rate experiments provoke a much more severe degradation than a high DR irradiation. Up to now, MOSFETs are supposed to be insensitive to changes in the dose-rate. We demonstrated with a set of experiments that this dose-rate dependency is found also in the modern transistors. We obtained interesting results regarding the bias and temperature dependencies. In addition, we used both an experimental and modeling approach, developing a coherent model that takes in account the differences between high and low dose-rates mechanisms. The results obtained will be the starting point for future studies and will be used for scientific publications.

We conducted experiments on the 28 nm technology node, which can represent a good alternative for CERN applications. In fact, as previously mentioned in other recent papers, this technology is particularly strong against ionizing dose. We irradiated up to 1 Grad(SiO<sub>2</sub>) a set of devices, and we encountered output current percentage degradation of nearly 10%. This is an encouraging result since, compared to previous technology nodes like the 130 nm or even the 65 nm, the same parameter was reduced by approximately 70%. As a notable draw-back, this new technology is strongly affected by drastic increases in the leakage current. These rises provoke enhancement in the static power dissipation of the circuits, which is intolerable in most of modern applications.

# Degradazione e Dipendenza dal Dose-Rate in MOSFET Decananometrici Esposti a Livelli Ultra-alti di Dose Totale Ionizzante

Sebastiano Costanzo

## Abstract

L'esperimento principale di questa tesi si chiama "Low Dose-Rate Sensitivity", un'analisi condotta per il nodo tecnologico a 65 nm, destinato ad essere implementato nella maggior parte dei circuiti per l'aggiornamento del CERN HL-LHC (High Luminosity - Large Hadron Collider). Il dose-rate (DR) è la dose assorbita per unità di tempo. Se il DR viene integrato nel tempo di irraggiamento, si ottiene la dose ionizzante totale (TID) depositata. I componenti elettronici maggiormente colpiti da radiazioni ionizzanti, implementati nei rivelatori CMS e ATLAS, dovrebbero raggiungere livelli di TID fino a 1Grad(SiO<sub>2</sub>) in 10 anni. Il relativo dose-rate è quindi circa 0.01 Mrad(SiO<sub>2</sub>)/h. Nelle procedure standard di irraggiamento, i dispositivi sono irradiati con dose-rates nell'ordine di 10 Mrad(SiO<sub>2</sub>)/h, che sono 1000 volte superiori a quello che realmente incontreranno. I BJT sono fortemente sensibili ai cambiamenti nel DR, in quella che viene chiamata Extremely Low Dose Rate Sensitivity (ELDRS). In pratica, a parità di TID, gli esperimenti a basso dose-rate provocano una degradazione molto più evidente rispetto ad un irraggiamento condotto a alto DR. Finora, i MOSFET vengono ritenuti essere insensibili ai cambiamenti del dose-rate. Abbiamo dimostrato con una serie di esperimenti che questa dipendenza rispetto al dose-rate si trova anche nei moderni transistor. Abbiamo ottenuto risultati interessanti per quanto riguarda le dipendenze da diverse tipologie di bias e temperatura. Inoltre, abbiamo usato sia un approccio sperimentale che modellistico, sviluppando un modello coerente che tiene conto delle differenze tra meccanismi ad alto e basso DR. I risultati ottenuti saranno il punto di partenza per studi futuri e saranno utilizzati per pubblicazioni scientifiche.

Abbiamo condotto esperimenti sul nodo tecnologico a 28 nm, che può rappresentare una buona alternativa per le applicazioni del CERN. Infatti, come già accennato in altre recenti pubblicazioni, questa tecnologia è particolarmente forte contro le dosi ionizzanti. Abbiamo irraggiato fino a 1 Grad(SiO<sub>2</sub>) una serie di dispositivi, e abbiamo incontrato una degradazione percentuale della corrente erogata di quasi il 10%. Questo è un risultato incoraggiante in quanto, rispetto ai precedenti nodi tecnologici come i 130 nm o addirittura i 65 nm, lo stesso parametro degrada di circa il 70%. Un notevole svantaggio per questa nuova tecnologia è un drastico aumento della corrente di leakage, ovvero la corrente erogata quando il dispositivo è spento. Tali aumenti provocano un incremento della potenza statica dissipata dei circuiti, che è intollerabile nella maggior parte delle applicazioni moderne.

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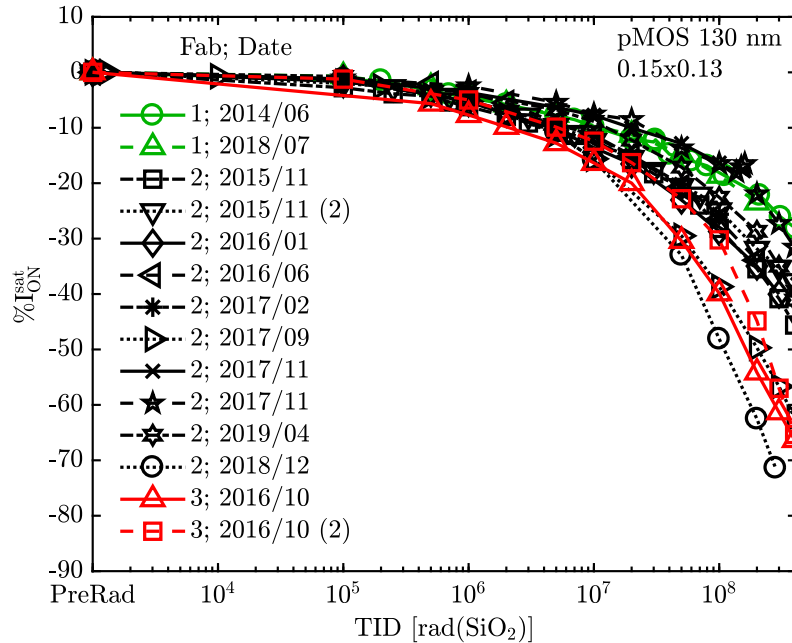
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# Chapter 1

## Introduction

The discovery of the radiation is dated back at the end of 17<sup>th</sup> century, thanks to the studies of Wilhelm Röntgen, Marie Curie and Henri Becquerel. Citing the first of the three listed researchers: *“It seemed at first a new kind of invisible light. It was clearly something new, something unrecorded...”* [1]. At first radiation sources were not considered an health hazard. Also Marie Curie died of problems mainly related to exposure to ionizing sources [2]. One of the classical example that highlighted the dangers of ionizing radiation was the case of the “Radium Girls”, workers whose job was painting watch dials with radium. After five of the workers sued the company (United States Radium), and also thanks to the ensuing publicity, the health risks of radiation exposure were brought to the public attention [3]. Radiation compromises also electronics standard operation. Generally, radiation-related degradation in electronics occurs due to the interaction between an impinging particle (proton, photon, heavy ion, electron, pion etc.) and the materials building the device. The type of damages are directly related to the energy of the particle and their relative ionizing proprieties. Radiation damages can be divided into two categories: non-ionizing (e.g. displacement damages) or ionizing. This thesis focus only on ionizing radiation effects on MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor). The integrated energy deposited by ionizing particles, called Total Ionizing Dose (TID), causes a cumulative build-up of charge in the oxides present in MOS transistors. The effect of multiple interactions can cause substantial changes in the nominal behaviour of the devices, therefore electronics intended to operate in harsh environments, i.e. with high radiation level, must be developed taking into account the effects of their interaction with particles. A well-known example of radioactive environment is the outer space. Satellites are in fact exposed to solar winds, cosmic rays and they orbits through Van Allen belts [4]. An updated analysis of radiation induced degradation on satellites in space application can be found in [5]. Among all the environments in which radiation is a threat to electronics systems, the Large Hadron Collider (LHC) running at CERN [6] and especially its future upgrade, High-Luminosity LHC (HL-LHC), that will be operative from 2025 [7], is the harshest environment in term of ionizing dose. In detail, CERN main experiments, such as ATLAS (A Toroidal LHC Apparatus), CMS (Compact Muon Solenoid), LHCb (Large Hadron Collider beauty) and ALICE (A Large Ion Collider Experiments) have to withstand the highest radiation level. In perspective, while TID usually reaches fractions of Mrad(SiO<sub>2</sub>) in space applications [8], the electronics designed for the inner layer of the particle detectors for the future HL-LHC experiments will



**Figure 1.1:** Ion percentage degradation for pMOS with  $W = 150$  nm and  $L = 130$  nm produced in different fabs, irradiated up to  $400\text{Mrad}(\text{SiO}_2)$  in diode configuration and with  $T = 25^\circ\text{C}$ .

experience up to one thousand Mrad(SiO<sub>2</sub>) [7]. The electronic components currently installed in LHC apparatus are mostly based on 250 nm technology node, while for the future upgrade the technologies will be scaled down to 130 and 65 nm transistors. In addition to the greater computational power allowed by the use of shorter channel devices, technology scaling naturally improves radiation-hardness [9]. As a drawback, the aggressive scaling enhances the device-to-device variability, which is nowadays one of the crucial issues encountered in radiation qualification processes [10]. As reported in [11], in each generation of devices, fewer atoms are employed in the fabrication processes, hence the presence of the absence of a single dopant atom can produce significant changes in the threshold voltage of a MOSFET. This high sensitivity requires extremely precise production processes to obtain robust chips. Radiation assurance analysis is becoming economically heavier at each technology scaling down step [12], since multiple tests are often required in order to obtain enough statistic to margin the variability unavoidably present in the fabrication processes. In addition, TID enhance the mentioned variability, as deeply analysed in [11]. As an example, Figure 1.1 reports the drive current percentage degradation variability in function of TID for nominal identical devices of the 130 nm technology node, produced by the same manufacturer but in three different fabrication plants, namely Fab. 1 (green), 2 (black) and 3 (red). Figure 1.1 is a clear representation of lot-to-lot variability. All the devices were irradiated up to  $400\text{Mrad}(\text{SiO}_2)$ , at room temperature and in diode configuration. The percentage variations at the end of the exposure are almost unpredictable, with some devices decreasing their output current of -70% and other just of -30%, even if produced in the same fab but in different years. The wide range in which the results fall shows how difficult it is to extrapolate models that can faithfully reproduce the behavior of devices exposed to different TID. Consequently, the objective of the radiation assurance experiments

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is the identification of mechanisms which greatly contribute to the degradation of the devices, independently from the inevitably present variability. Our job consists in determine which effects are enhanced or mitigated by particular auxiliary oxide structures, commonly implemented in modern MOSFETs. Our goal is hence to provide qualitative knowledge on the mechanisms that most occur during the ionization of oxides, rather than solid predictions on the final percentage of degradation of the device taken individually and irradiated at any level of TID.

This thesis presents two nuclei: The Dose-Rate (DR) effect on 65 nm technology node and a comparison between two 28 nm structures, produced by two different manufacturers. The analysis of true DR effects is based on extremely time-requiring tests and lasted in total multiple months. The DR effect on this technology has been already briefly reported in [13]. We gained further knowledge on this phenomenon, and we will propose some comments on the causes of the enhanced damage at low dose-rates. We were able to perform multiple tests, in which we covered different combinations of biases, temperatures and, of course, of DRs. In addition, the devices irradiated at the highest DR have been kept under bias for additional time, in order to exclude the possibility that the enhanced degradation at low dose-rates was caused by time-related effects.

We performed studies on the 28 nm technology node exposed to ultra-high level of ionizing dose. While several parameters of this devices are only slightly affected by TID even at ultra-high doses, the leakage current rises of multiple orders of magnitude. This technology can represent anyway a valuable choice for future electronic developments at CERN. We analysed the main parameter variations as a function of TID for two different manufacturer technologies, named Manufacturer A and B.

The thesis outline is here reported.

Chapter 2, *TID-Induced Traps Formation* will briefly discuss the basic mechanisms occurring in MOSFET oxides exposed to irradiation, focusing on charge generation, transport and relative trap centers formation. It is the preliminary chapter that allows to understand the mechanisms presented in Chapter 4, 5 and 6.

Chapter 3, *CERN X-Ray Setup* will describe the experimental setup used to obtain all the results reported in this thesis.

Chapter 4, *TID Effect On Modern CMOS Technologies* briefly summarize the most common degradation phenomena occurring in STI and spacer oxides for modern technologies, exposed to ultra-high levels of radiation. We will mostly focus on Radiation-Induced Narrow Channel Effect (RINCE) and Radiation-Induced Short Channel Effect (RISCE), and on the radiation induced drain to source leakage current path creation.

Chapter 5, *Low Dose Rate Effect on 65 nm node MOSFET* will contain a detailed analysis on the true DR effect measured in the 65 nm technology node.

Chapter 6, *A Prospective To CERN Future: 28 nm* will show the robustness of the 28 nm technology node exposed to ultra high level of radiation. We will compare two different manufacturers, proposing comments on the cause of the differences in the parameters evolution in function of TID.





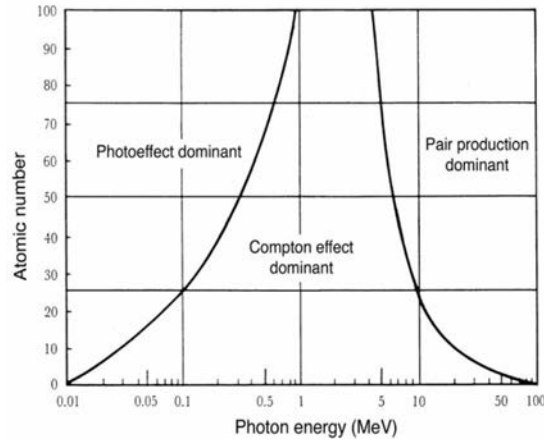
# Chapter 2

## TID-Induced Degradation

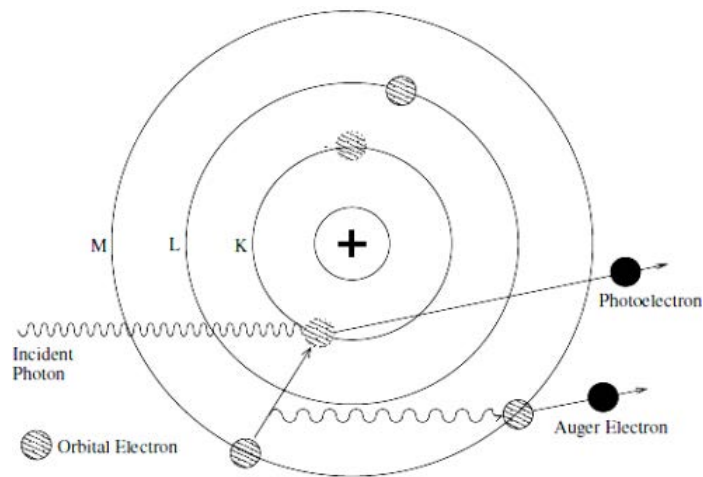
This chapter summarizes the processes that provoke the formation of trap centers, located either in the bulk of oxides or at the Si/SiO<sub>2</sub> interface. In Section 2.1 is reported a brief introduction on the photoelectric effect, that will allow us to understand under which conditions ionization in the oxides can occur. Section 2.2 covers the typical transport mechanisms of holes through the oxides that culminate with charge built-up in the depth of the oxides (generation of the oxide traps) and in the insulator region closer to the silicon bulk (creation of border traps). Section 2.3 analyzes the complex processes that result in the creation of Si/SiO<sub>2</sub> interface traps. We will compare the main differences between these traps and the one located in oxide bulk.

### 2.1 Interaction Between Radiation and Matter

The interaction of radiation with solid-state devices depends mainly on the mass, charge state and kinetic energy of the impinging particles, and on the atomic mass, atomic number and density of the target [14]. This thesis will refer to the interaction between photons and typical materials that compose the classical MOSFET, silicon (Si) and silicon dioxide (SiO<sub>2</sub>). There are three type of interactions between photons and targets material, each of them produces energetic free electrons [14]. In the experiments conducted, the photoelectric effect is mainly involved in the interactions, as it possible to see from Figure 2.1, taken from [15]. In fact, the atomic numbers of silicon and oxygen are respectively  $Z_{\text{Si}} = 14$  and  $Z_{\text{O}} = 8$ , while the X-Ray source spectrum used in the experiments conducted has a maximum of intensity at the energy of 10 keV. In the photoelectric effect, if the incoming photon has an energy high enough to excite an electron of the target atom from the K-shell, i.e. the closest shell to the nucleus, to an higher energy level, for example the L-shell (which is further from the nucleus, compared to the K-shell), then around 80 % of the collisions happen with K-shell electrons [14]. Photoelectric effect takes place predominantly in the K atomic shell and therefore it is possible to use its cross-section to estimate the total photoelectric cross-section [16]. The emitted electron completely absorbs the photon, and can be called photoelectron, even if its charge and mass are the same as a classical electron. Another electron, coming from the L-shell will fulfill the vacancy left from the photoelectron. Since the electron loses energy, there will be an emission of a low-energy photon (or so called fluorescence photon), with an energetic level equal to the difference of the energy level of the two shell, i.e. L and



**Figure 2.1:** Importance of three photon interactions as a function of atomic number and photon energy. Solid lines correspond to equal cross sections for neighbouring effects. Taken from [15]

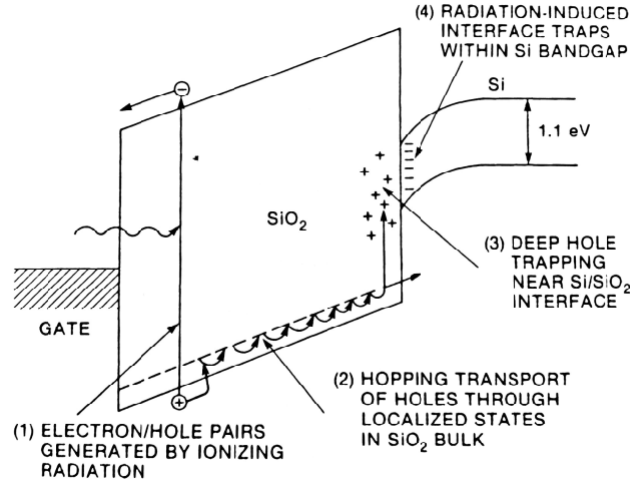


**Figure 2.2:** Description of photoelectric effect in a free atom. Taken from [16]

K. It is possible that the fluorescence photon emitted ejects another orbital electron, called Auger electron. Figure 2.2 provides a good representation of the photoelectric effect. Therefore, from the interaction of a photon with the insulating layer of the device, there are the generations of an electron-hole (e-h) pair, a low-energy photon and sometimes an Auger electron. The freed photoelectron, passing through the material, deposit a portion of its energy as ionization and the remaining as atomic lattice displacement. For charged particles, such as electrons, most of the loss of energy occurs via ionization, even if a small amount of atomic displacement can happen, while for neutrons is the opposite [14].

## 2.2 Holes Transport And Oxide-Traps Formation

Ionizing radiation effects are a concern for both the silicon bulk and the oxides of a MOSFET structure. When the ionization processes take place within a part of the MOS capable of retaining charges, such as layers of silicon dioxide, the effect of multiple interactions can accumulate over time. Figure 2.3 shows the ionizing

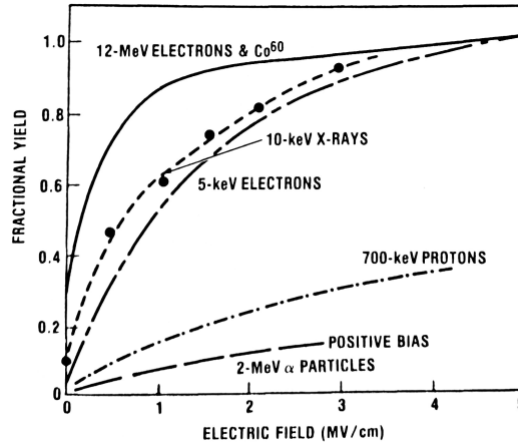


**Figure 2.3:** Schematic of ionizing radiation induced effects in MOS structures, with positive gate applied to n-channel MOSFET. Taken from [9]

radiation effects in a generic nMOSFET structure, with a positive bias applied to the gate. Multiple stages succeed one another in the process of charge trapping in the oxide layers. In particular:

1. Creation of electron-hole pairs by ionizing radiation
2. Transport of holes via polaron hopping through localized states in SiO<sub>2</sub> bulk
3. Deep hole trapping in the SiO<sub>2</sub> bulk, and near Si/SiO<sub>2</sub> interface
4. Interface traps depassivation at the Si/SiO<sub>2</sub> interface

As previously reported in Section 2.1, the photoelectron can, along his trace, ionize other particles, generating e-h pairs. Previous studies proved that the average energy required to create an e-h pair in SiO<sub>2</sub> is approximately  $17 \pm 1$  eV [17, 18]. As soon as the e-h pairs are generated, some of them are instantaneously recombined. The electrons are much more mobile than the holes, and can be considered negligible in the charge trapping processes in MOS oxides. From [19], the mobility of electrons in SiO<sub>2</sub> varies from  $\sim 20$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, measured at room temperature ( $T = 300$  K), to  $\sim 40$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> measured at low temperature ( $T < 150$  K). For high electric field in the oxides,  $E_{OX} \geq 5 \times 10^5$  V cm<sup>-1</sup>, the electron drift velocity saturates quite sharply to  $1 \pm 0.1 \times 10^7$  cm s<sup>-1</sup> [20]. Nowadays, since the thickness of the gate oxide is in the order of some nm, the magnitude of electric field crossing them is high enough to give at the electrons the possibility to reach the saturation drift velocity. This implies a transit time of the electrons in the oxides of the order of some picoseconds. Essentially, for all the temperatures and the electric fields, electrons transport can be considered instantaneous. Regarding holes, their mobility is dependent on both temperature and electric field, and in any case is smaller than the same parameters of the electrons. In fact, their mobility varies from  $10^{-4} \div 10^{-11}$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> [21]. Therefore holes are considered immobile compared to electrons, and for this reason the radiation induced effects are attributed exclusively at their presence.



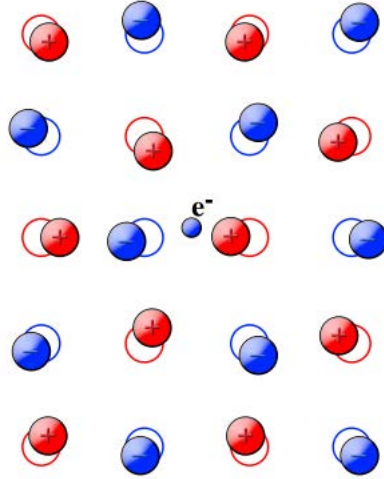
**Figure 2.4:** Fractional yield as a function of applied electric field for several different kinds of radiation incident particles on  $\text{SiO}_2$ . Taken from [9].

### 2.2.1 Recombination Models

Two basic models have been developed in order to describe the recombination of e-h pairs from an analytic point of view: the columnar model and the geminate model [9]. They differ between each other for two parameters:  $r_t$ , which is the initial distance of separation between the hole and its corresponding electron, and  $\lambda$ , which is the mean distance of separation between different e-h pairs. The columnar model proposes that the generation of e-h pairs happens in very narrow and dense columns, therefore for this model  $r_t \ll \lambda$ . On the other side, the geminate model proposes that one hole and its electron are further from each other than from another e-h pair couple, imposing  $r_t \gg \lambda$ . In most of the real cases, the actual recombination process is a combination of the two models.

### 2.2.2 Holes Transport in $\text{SiO}_2$

The charge generation and recombination processes are completed in few picoseconds after the impact of the radiation source. After this small amount of time, the fraction of holes that escaped recombination process – which is called charge yield – undergoes transport in  $\text{SiO}_2$ , optionally promoted by the presence of an electric field. As it is possible to notice from Figure 2.4, for a 10 keV X-Ray source the fractional yield rate approaches the unity for high electric fields, therefore it is clear that holes transport is a big concern for ionizing radiation effects. Over a certain amount of time, holes start to move toward the negative electrode, i.e. the silicon substrate, since, in this example, the gate has a positive bias imposed. The holes are then collected in the silicon substrate or captured in deep trapping sites. A large set of experiments, conducted since 1971, demonstrated the dependence of the hole transport mechanism by time, temperature and electric field [22, 23, 24]. It has become clear that the hole transport in  $\text{SiO}_2$  is rather anomalous in nature, since it lasts over decades of time, therefore is an highly time-dispersive process [25]. The holes that did not move through the oxide cause a negative flatband voltage shift, and therefore a negative threshold voltage shift [14]. From the set of experiments conducted in [22] and in [23], it emerged that the recovery time of the flatband voltage can be speeded from high temperatures and high electric fields, reaching a



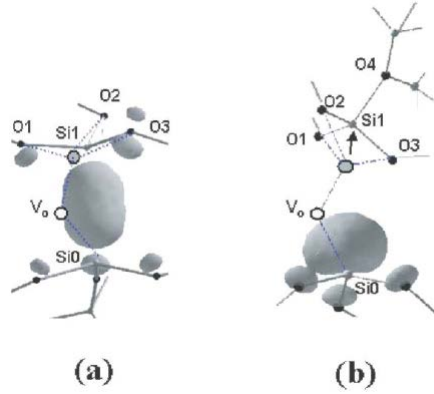
**Figure 2.5:** Representative image of a polaron. The conduction of one electron in a ionic crystal repels the negative ions and attracts the positive ones. Taken from [27]

reestablishment on the parameter in short time ( $t \ll 1$  s).

Holes transport in silicon dioxide through a complex mechanism, called polaron hopping. A polaron is a quasi-particle, proposed by Lev Landau in 1933 [26], formed by the coupling of a charge and the defects that surround it, which result in a localized distortion of the lattice. This combination of charge and distorted defects moves with decrease velocity, since the effective mass is higher than the mass of the single charge. In Figure 2.5 is reported a visual representation of a polaron structure, taken from [27]. The time-dispersive movement is non-Gaussian. In a Gaussian transport process, the mean displacement of a carrier package,  $\bar{x}$ , increases linearly with time, while its dispersion,  $\bar{\sigma} = \sqrt{(x - \bar{x})^2}$ , increases with the square root of the time. In a time dispersive transport, the time dependence of  $\bar{\sigma}$  is the same as  $\bar{x}$ , therefore their ratio is independent from time. This implies an asymmetric change in the carrier distribution over time [9]. In practice, there will be some fast charges that move rapidly deep in the oxide bulk, while most of the carriers will be left behind, since the dispersion increases faster in a time-dispersive process [25]. Many studies, for example [25], showed that hole transport is precisely described from Continuous-Time Random Walk (CTRW) model. This model describe a walker hopping randomly on a periodic lattice, with the steps occurring at random time intervals [28].

### 2.2.3 Hole Trapping in SiO<sub>2</sub>

Once the radiation-generated holes completed their transport through the SiO<sub>2</sub>, MOS structure presents a negative voltage shift in its electrical characteristics, for example in the threshold voltage ( $V_{TH}$ ), that can persist for years [9]. This long-term effect is attributed to the positive charge trapped in the oxide layer [9]. The term “hole trap” refers to a normally neutral oxide defect that can capture holes and retain them for long time period. Those defects are mostly formed by vacancies in the SiO<sub>2</sub> structure [29]. The silicon atoms are bonded with four oxygen atoms, and, if one of them is missing, two silicon atoms will be weakly bonded together, in a



**Figure 2.6:** Schematic of the  $E'_{\delta}$  center (a) and  $E'_{\gamma}$  center (b), taken from [31]. IEEE © 2002

structure generally called  $E'$  center [30]. The two silicon atoms share two electrons. The holes, moving along the oxide, can easily break this bond, recombining with one of the two electrons shared between the Si-Si structure. If this happens, the two silicon atoms are bonded with just a single electron. From [31], there are two different type of defects in the  $\text{SiO}_2$  structure. The first, (which represent around 80 % of the total defects), is called  $E'_{\delta}$  center and is the only stable configuration. In this case, the electron is equally shared between the two Si-Si atoms, making the configuration neutral, with a shallow electron containing energy level (around 1 eV). In the second structure (which represent the other 20% of all the defects), one of the two silicon atom relaxes back past the plane defined by its three oxygen neighbors and bonds with another network of oxygen atoms, forming an asymmetrical positive charge structure, which is called  $E'_{\gamma}$  center and has a much higher electron containing energy level (around 4.5 eV). In Figure 2.6 there is a visual representation of the centers, taken from [31].

The charge trapped in the oxide undergoes through annealing processes, caused for example from tunneling effects in the silicon substrate, e-h recombination or electron injection from silicon [9]. It is clear that, the nearest is the charge trapped in the oxide, the easiest it can be neutralized by electrons coming from the silicon substrate. As an implication, oxide traps collocated far from Si/ $\text{SiO}_2$  interface are, statistically, harder to neutralize. In case the trap is located near enough to the silicon substrate, it can react to any change of bias, switching back and forth from a positive charge state to a neutral state. This kind of traps have been formalized and defined as border traps, in [32], where all the oxide traps collocated at 3 nm or less from the Si/ $\text{SiO}_2$  interface can be considered part of this category. From analysis conducted in [9], it is possible to express overall charge buildup process in the following incremental form:

$$\Delta n_{\text{th}}(x, \Delta D) = F_{\text{h}}(x)\sigma_{\text{ht}}(E_{\text{ox}}(x))[N_{\text{ht}}(x) - n_{\text{ht}}(x)] - F_{\text{e}}(x)\sigma_{\text{r}}(E_{\text{ox}}(x))n_{\text{ht}}(x) \quad (2.1)$$

Where,  $F_{\text{h}}(x)$  and  $F_{\text{e}}(x)$  are the local fluences per unit of dose for radiation-generated holes and electrons;  $n_{\text{ht}}(x)$  is the local density of trapped holes;  $N_{\text{ht}}(x)$  is the local density of hole traps;  $\sigma_{\text{ht}}(x)$  is the local oxide field-dependent cross-section of the holes traps for capturing holes;  $\sigma_{\text{r}}(x)$  is the local oxide filed-dependent cross-section for recombination of an electron with a trapped hole. The first part of the equation

suggests that, starting from initial fluences per unit of dose of generate holes, some of them will be captured – therefore the presence of the field-dependent cross section term. The difference  $N_{ht}(x) - n_{ht}(x)$  are basically the empty traps state, that are effectively participating in the charge build-up process. The second part of the equation is subtracted to the first, since electron have a negative impact (due to recombination process) in the charge build-up. The charge density per unit of area is obtained integrating  $n_{ht}(x)$  over the oxide area, generally called  $d_{ox}(x)$ :

$$\Delta N_{ot} = \frac{1}{d_{ox}} \int_0^{d_{ox}} n_{ht}(x) x \, dx \quad (2.2)$$

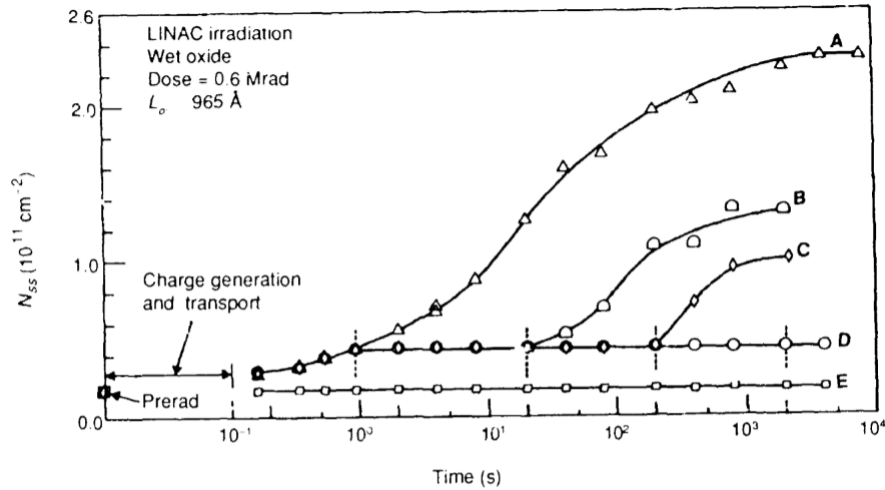
Finally, the flatband voltage shift is:

$$\Delta V_{ot} = -\frac{q}{\epsilon_{ox}} d_{ox} \delta N_{ot} \quad (2.3)$$

From the previous equation it is possible to notice the linear dependence of the flatband voltage shifts from the oxide thickness. If the oxide thickness decreases, the shift of the flatband voltage follows the same trend. This linear dependence has led to a reduced sensitivity of the gate oxide in modern technologies, e.g. 130 and 65 nm, which has been proved to be capable of withstand ultra-high level of total dose [33]. In these technologies, the gate oxide is few nanometers thick (around 2 nm in the 65 nm technology node) and entirely composed of silicon dioxide. As we will see, the radiation response is dominated by the presence of auxiliary oxides, like the STI (Shallow Trance Isolation) and spacers.

## 2.3 Si/SiO<sub>2</sub> Interface Traps Depassivation

The interface between silicon and silicon dioxide is generally deficient of oxygen, therefore there is a good amount of strained or “dangling” silicon bonds. These dangling bonds act as interface traps with energy within the energy gap of the silicon [9]. More in the detail, Winkour and colleagues developed between 1977 and 1979 a model in which is sustained that the formation of interface traps occurs in a two-stage process [34]. The first stage is associated with the transport of radiation-generated holes through the oxide. The hopping transport, described in Section 2.2, releases energy (evaluated around 5 eV). This energy breaks relatively weak H bonds with trivalent Si or with strained Si-O bonds formed during fabrication process. A released H<sup>+</sup> ion, in case of positive bias, drift through Si/SiO<sub>2</sub> interface, where it interacts with the dangling bonds and depassivate an interface traps. The activation of interface traps strongly depends on the electric field applied to the devices [35]. In fact, as it is possible to understand from Figure 2.7, extracted from [35], high electric fields enhance the formation and the trapping of charge in the Si/SiO<sub>2</sub> trap centers. In that experiment, multiple samples were tested, each of them having different electric field applied. Sample E had negative electric field of -4 MV cm<sup>-1</sup> applied to the gate, and no increase from the pre-irradiation interface state value was observed. Sample A, had a positive and extremely high field applied, 4 MV cm<sup>-1</sup>, imposed for almost 10000 seconds. As regards samples B, C and D, the electric field was positive and equal to the one imposed on sample A, but after 1 second it was switched to the negative value of -4 MV cm<sup>-1</sup> and the charge trapping an the



**Figure 2.7:** Field experiments showing importance of positive field during second stage of Winkour model [34]

interface stopped. For sample B the electric field was switched positive again after a total time of 10 seconds, while for sample C it was switched back after 100 seconds. For sample D is kept at  $-4 \text{ MV cm}^{-1}$  until the end of the experiment. The results showed the extremely dependence from the electric field applied to the gate of the structure in the interface traps depassivation mechanisms.

As stated in [9], interface traps must be collocated within one or two atomic bond distances (about 0.5 nm) from the silicon lattice, so that electrons and holes can easily tunnel from valence band to conduction band and vice versa. It has been shown that high temperature strongly enhance the transitions rate – the number of transitions per unit of time – between the two energetic bands [36]. At  $T = 300 \text{ K}$  the transitions rate for trap centers collocated close to the interface is about 100 transitions per second, while for further traps is 0.01 transitions per second. At  $T = 100 \text{ K}$ , for the first type of traps centers the transitions rate drastically drops to  $10^{-8}$  transitions per second, while the latter one are essentially frozen, with a transition rate of  $10^{-18}$  transitions per second. Another extremely important propriety of the interface traps is their amphoteric nature. In fact, the polarity of the net charge residing in them can be positive, neutral or negative, with the respect of their position in the energy gap of the silicon, compared to the Fermi Level ( $E_F$ ) and the Mid-Gap Level ( $E_M$ ). The defects in the bottom part of the band diagram are usually donor, which means that are neutral under  $E_F$  and when they are situated above  $E_F$  they free one electron, becoming positive charged. From the other side, defects collocated in the top part of the band diagram are acceptor, which means they are negative when above  $E_F$  and neutral once under it. As implication, if the voltage imposed on the gate is equal to the difference  $E_F - E_M$ , all the interface traps will have a neutral sign [9, 37].

## 2.4 ELDRS in Bipolar Devices

The discovery of the presence of a DR effect in microcircuit transistors can be dated back in 1991 [38] and in bipolar circuits in 1994 [39]. Following these first papers, several articles on Enhanced Low Dose Rate Sensitivity (ELDRS) have been pro-



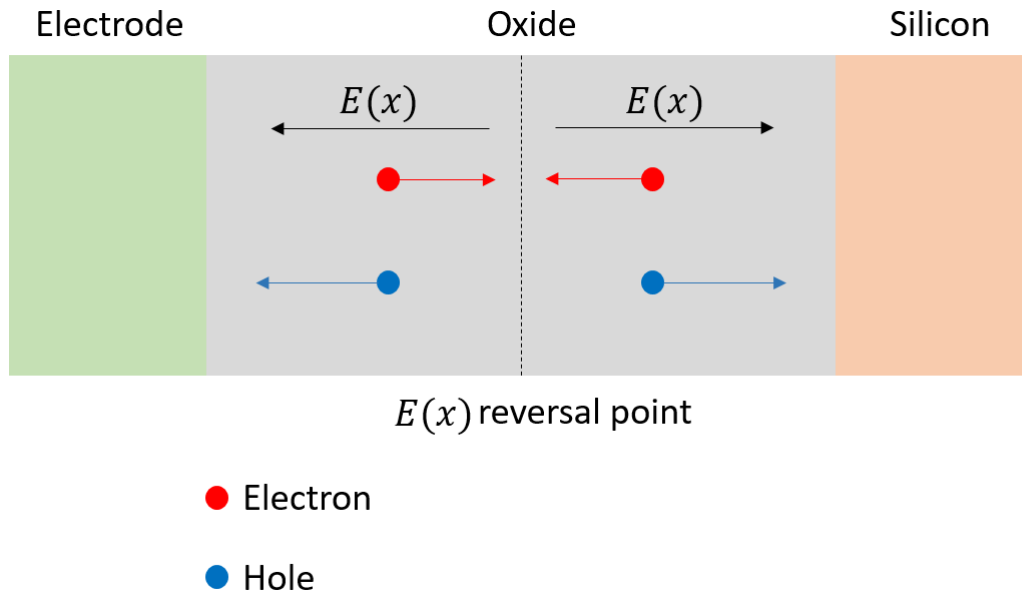
duced, for example [40] and [41]. Most of those concepts have been summarized and further investigated by Pease and co-workers in [42]. The acronym of ELDRS was introduced before a real understating of the mechanisms. Further studies showed that the mechanism was more a reduced degradation for High-DRs, rather than an enhanced degradation for Low-DRs. A more accurate name would be therefore Reduced High Dose Rate Sensitivity (RHDRS). However, the acronym ELDRS remained and it is still used to refer to a DR sensitivity of the radiation response. A true low dose-rate effect is not always easy to distinguish, and may be confused with a time dependent effect. In particular, quoting [42]: “to distinguish real dose rate effects it is necessary to anneal the device irradiated at high dose rate maintaining constant the temperature for a period of time at least as long as the irradiation time at low dose rate”. Many models have been proposed in order to explain and understand true dose rate effects in bipolar transistors. These models can be grouped into three main categories:

- Space Charge Models, see e.g. [43, 44, 45, 46]
- Bimolecular Process Models, see e.g. [47, 48]
- Binary Reaction Rate Model, see e.g. [49]

In the following sections a brief explanation of these three models will be proposed. The three models discuss the mechanisms differently and no agreement has yet been reached on which one is actually more consistent with the real processes. In any case, the effect of the dose-rate on the devices is extremely complex and it is difficult for a single model to explain with total correctness what phenomena occur.

### 2.4.1 Space Charge Models

Space charge model has been first developed by Fleetwood et. al., in the 1994 [43] and then further developed in other papers [44, 50]. In the first version, [43], it was reported how high dose-rates produce a space charge accumulation inside the BJT oxides. The accumulation of space charge was attributed to mechanisms that slows hole transport. In fact, the density of  $E'_{\delta}$  trap centers in parasitic oxide is usually high and they trap the radiation-generated holes, causing a decrease in the holes mobility. As high dose-rate irradiation proceeds, more and more holes are trapped inside the centers, forming a “wall” of potential that prevents additional holes to get trapped in deep trap centers. The space charge generated at high dose-rates produces a local reversion of the potential, therefore part of the holes are trapped closely to the interface (instead of in the bulk of the oxide) where they are easily annealed, as reported in Figure 2.8. From the other hand, if the radiation is performed with a low dose-rate, the flux of generated holes is not high enough to keep constantly filled the big majority of the  $E'_{\delta}$  trap centers. Therefore the process proceeds without any slowdown and there is not formation of space charge in the oxide. In [44], an improved second version of the model proposed that also the radiation-generated electrons participate to a reduction in the overall damages as the DR increases. In fact, these electrons can recombine with a hole which is part of the space charge and create a stable neutral dipole, reducing the positive overall charge in the oxide,  $N_{ot}$ . The first two versions of the model took in account the differences that low or high dose-rates cause to the charge trapped in the oxide,



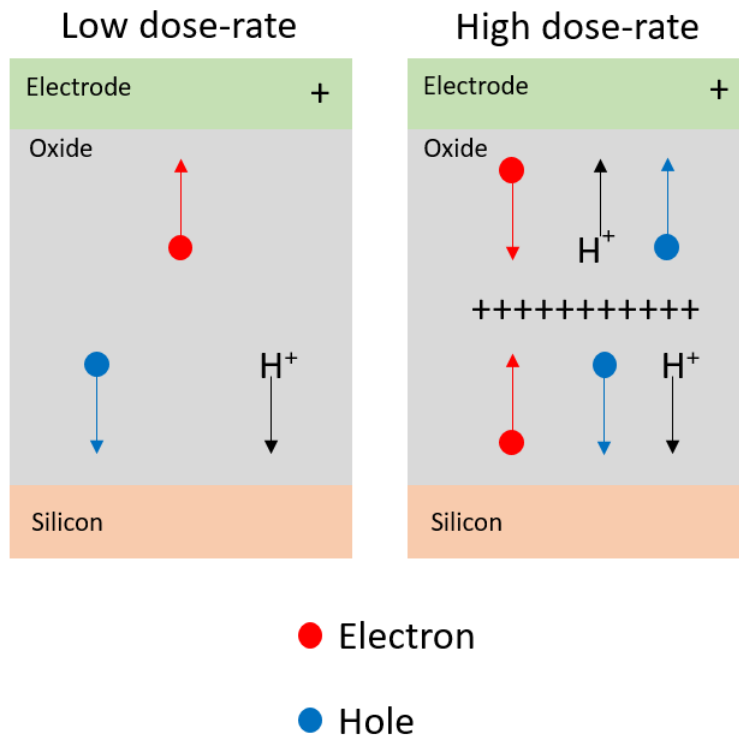
**Figure 2.8:** At high dose-rates holes and protons generated close to the gate side drift toward the gate, rather than toward the Si/SiO<sub>2</sub> interface, due to local reverse in the electric field caused by the space charge. After [46] IEEE © 1998

but they did not explain the influence of the DR on the depassivation of interface traps ( $N_{it}$ ). This was introduced in 1998, with the last version of the space charge model [50]. The space charge formed at high DRs reduces the effective number of  $H^+$  able to reach the interface and then react with the Si-H bonds, reducing  $N_{it}$ .

In conclusion, space charge model states that high dose-rates generate a space charge in the oxide (supposed in [50] to be uniformly distributed, as reported also in Figure 2.9) that reduce the net positive charge trapped in the oxide,  $N_{ot}$  thanks to trapping of holes close to the interface (hence easily annealed) due to local electric field reversal [43] and thanks to radiation-generated electrons/holes recombination mechanisms [44], that lead to the formation of neutral stable dipoles. In addition, the number of interface traps is reduced since a less hydrogen ions are able to reach the interface [50].

## 2.4.2 Bimolecular Process Models

Bimolecular process models are based on the interaction between two particles. Some studies suggested the presence of processes involving hydrogen reaction [51], trapped electron – free hole recombination [52], free electron – free hole recombination [51], molecular hydrogen formation [47], or a combination of hydrogen cracking and free electron recombination with trapped or transporting holes [48]. In general, each of these processes leads to a true dose rate effect by producing a sublinear total dose response at high dose rates [42]. In each of the studies proposed, authors carefully calculated the critical dose and dose rate (often respectively called  $N_c$  and  $g_c$ ) values which must be exceeded before ELDRS effect is tangible. The most recent ELDRS models attempt to explain the effects of hydrogen on the ELDRS response of  $N_{it}$  [48]. The reduced effects at High-DR can be related to a competition between defect reactions involving holes. The main reaction observed involves  $E'_s$  centers.

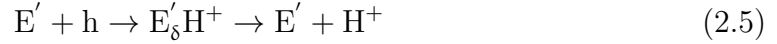


**Figure 2.9:** A uniform space charge distribution causes local inversion of the electric field in the bulk the oxide. As it is possible to notice, holes generated close to the Si interface drift toward the silicon bulk and can create interface traps. From the other side, holes generated closer to the gate electrode tend to drift toward it and get collected, reducing the net charge in the oxide. After [50] IEEE © 1998

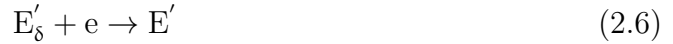
Molecular hydrogen (two H atoms sharing their two electrons) is cracked at these sites and in the process, protons are released:



From the previous interaction there is the formation of a trapped neutral hydrogen at the source site, which can in turn react with another hole to release an additional proton:



Where  $E'$  are neutral traps site. The protons migrate to the interface and depassivate the hydrogen, forming interface traps. At high dose rates, the net positive charge of the free holes, trapped holes and protons tends to confine the electron in the oxide [42]. The confined electron tends to recombine with the positively charged species, primarily the holes trapped at cracking sites:



Consequently, fewer protons will be released by these sites at high dose rates, and less damage will occur.

### 2.4.3 Binary Reaction Rate Model

One last model that is worth to be discussed is the one developed by Freitag et. al. in [49] in which it is assumed that the built up of  $N_{it}$  is a results of two defects interacting according to binary reaction rate theory. Radiation generated holes reacts with pre-existing quantity of hydrogen, causing an initial buildup of  $N_{it}$ , with a rate that initially increases and the decreases as the quantity of hydrogen is used up. Later, a new “supply” of hydrogen (radiation generated) reaches the interface, increasing the rate of  $N_{it}$  build up. In [49], it is shown that the amount of degradation that occurs when the delayed cargo of hydrogen reaches the interface is much greater if the device is under irradiation. This mean that in low dose rate experiments – more time requiring than High-DR ones – the degradation will be enhanced.

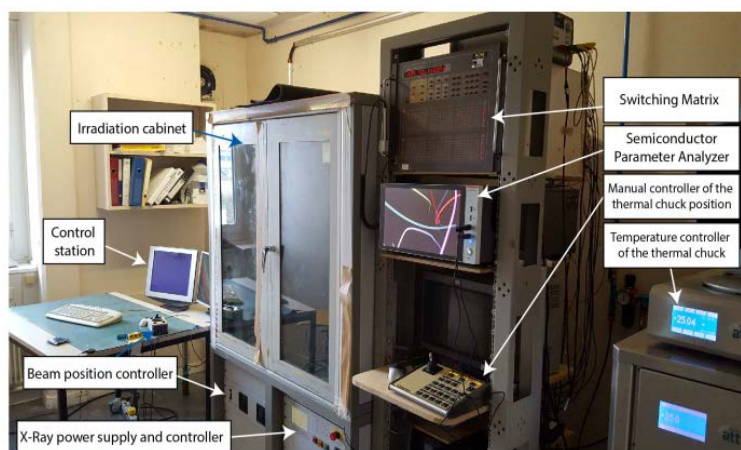
# Chapter 3

## CERN X-Ray Setup

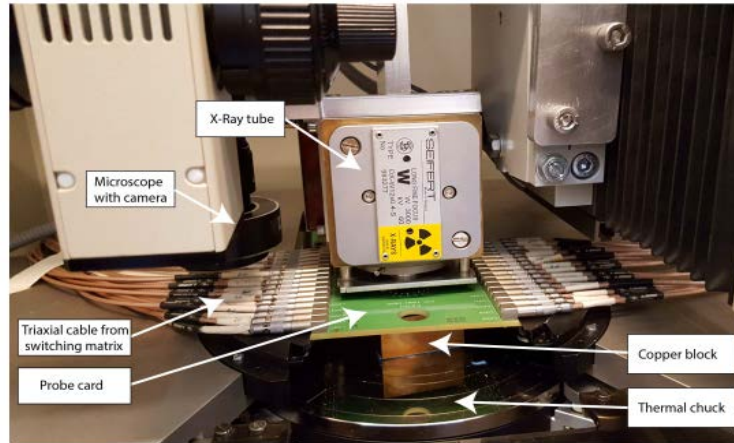
In this chapter we will briefly explain the whole measurement system used by the experiments reported in this thesis. It is a complex system that requires continuous maintenance. The implemented software is periodically updated, in order to have a good organization of the data obtained from the experiments.

### 3.1 CERN X-Ray Setup

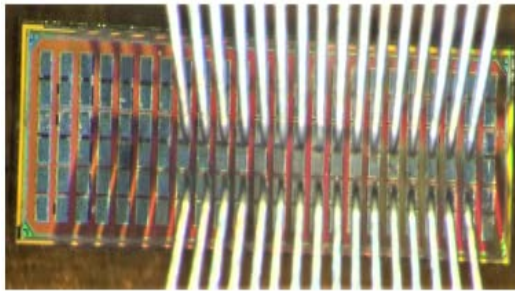
All the irradiation experiments reported in this thesis are conducted inside the CERN X-Ray Seifer RP149 cabinet, pictured in Figure 3.1. Inside the cabinet, the X-Ray beam is located above a probe card, which is connected to the switching matrix (showed in 3.1) via Lemo cables. The device under test is placed on a copper block and the thermal chuck is moved manually to reach contact with the DUT, while monitoring through the microscope incorporating a camera, as reported in Figure 3.2. The temperature is controlled by a thermal chuck, whose temperature can vary from  $-50\text{ }^{\circ}\text{C}$  up to  $200\text{ }^{\circ}\text{C}$ . Its position can be controlled with a pad, connected via a serial port interface. The thermal control assure a stable temperature for the whole experiment, which is mandatory in qualification processes, since most of the radiation related processes are thermally activated at different temperatures. The measurements are performed with a semiconductor parameter analyzer, nomi-



**Figure 3.1:** CERN EP-ESE group X-Ray irradiation facility, with all the related instruments used to perform accurate irradiation experiments.



**Figure 3.2:** Inner view of the CERN X-Ray cabinet.



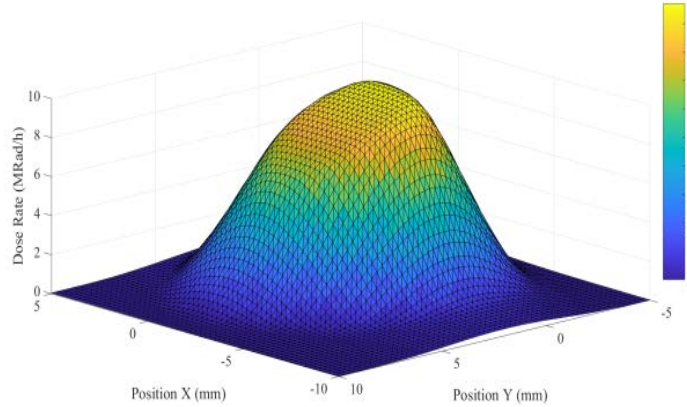
**Figure 3.3:** Probe card needles contacting a generic array.

nally Keithley 4200A-SCS, reported in Figure 3.1. The version used implements six Source Measure Units (SMUs) and one Capacitance Voltage Unit (CVU). SMU are a powerful resource in qualification processes, since it is possible to impose a voltage and, at the same time, to read a current at his node. The Keithley 4200A-SCS parameter analyzed is connected to a switching matrix, which allows to route each SMU through 32 triaxial outputs wired to the probe card, by commuting the contact inside the matrix. The chips analyzed are mounted on a thick layer of silicon substrate. In each chip there is a certain number of arrays (usually varying from 3 up to 7). Each array is divided into two adjacent columns of pads, which are connected to the terminals of the pMOS and the nMOS transistors. The above mentioned probe card has 32 needles, with the which is possibly to contact the whole array, as pictured in Figure 3.3.

The ionizing radiation source used to irradiate the ASICs is generated using a Crookes tube. The dose rate reached by these tubes can be high, even around 10 Mrad/h. It is possible to vary the dose rate changing the distance between the DUT and the beam, or changing the power at which the X-Ray machine operates. Each time a new experiment starts, we calibrate the dose rate, using a PIN photodiode [53]. The current flowing through the diode is proportional to the deposited energy by photons that contribute to the irradiation and a linear relationship can give information on the DR once the current is acquired:

$$DR = \alpha (I_{\text{READ}} - I_{\text{DARK}}) \quad (3.1)$$

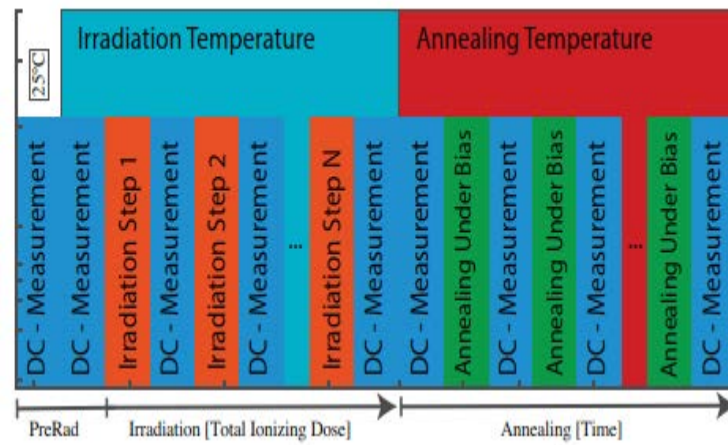
$\alpha$  is the conversion coefficient, which is known. The PIN current,  $I_{\text{READ}}$  include some



**Figure 3.4:** 3D calibration of the beam used to carry out the experiments.

unwanted current, called  $I_{\text{DARK}}$ , which is present even if the X-Ray machine is not irradiating and may be caused by other source of photons. This extra contribute has to be taken into account, especially when the experiments require low dose rates, since the two currents may become comparable. In Figure 3.4 is reported an accurate calibration process, conducted by Koch in 2018 [54].

Most of the qualification processes follows this procedure. A first measure is acquired at room temperature. Then the temperature is optionally changed to the target one, and in that case a second pre-irradiation characterization is required. After these measurements, the irradiation starts and is divided into several steps. The DUT is fully characterized after each step. Once the last irradiation step and the relative measured are finished, and if the temperature differs from 25 °C, an additional post-irradiation measurement is performed at room temperature. Optionally after that, annealing process start and the temperature is shifted to the wanted value. During annealing, the devices are kept under bias and usually at high temperature, to accelerate time-dependent mechanisms. The structure are measured every 2 to 5 hours for a period that can vary from some hours up to weeks. A visual representation of the process is reported in Figure 3.5.



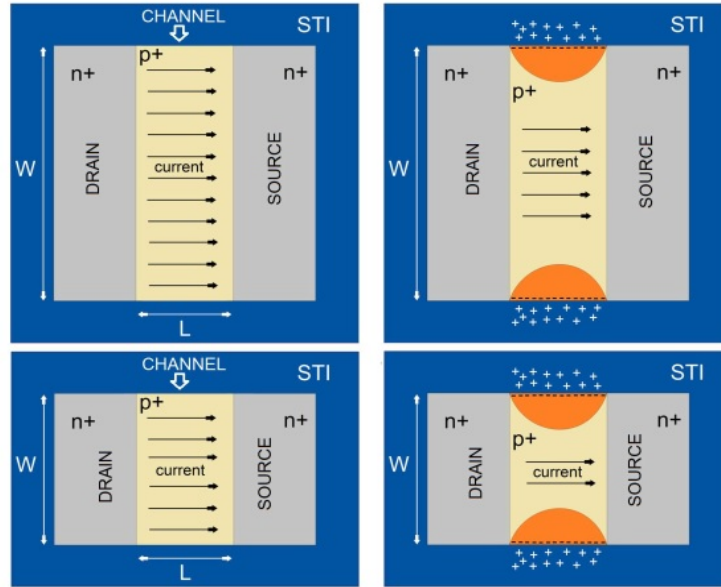
**Figure 3.5:** Typical qualification procedure used during TID experiments. Transistors are irradiated to a specific TID level and the irradiation is stopped to measure the device characteristic. Once the irradiation reaches the wanted TID, the annealing part starts.



# Chapter 4

## TID Effect on Modern CMOS Technologies

As briefly reported in Chapter 2, charge built-up processes affect oxides exposed to ionizing radiation. From Equation 2.3, flatband voltages are directly influenced by dielectric thickness. Gate insulators used to be much thicker [55] compared to modern structures [56], therefore these insulators were extremely sensitive to TID effects. Most of the studies on TID-induced traps formation processes are dated back between '80s and '90s, hence were conducted on gate oxides, such as extensively reported in books (e.g. [9, 57]) and summarized in scientific papers, e.g. [58]. Nowadays, gates are almost immune against ionizing process [59], since their thickness is less than 3 nm, consequently charge trapping is highly improbable, also due to tunnel effect [60]. In fact, studies on the 130 nm technology node, which gate thickness is around 3 nm, conducted by Faccio and co-workers in [33], demonstrated the insensitivity to TID for thin gate dielectrics. Modern technologies are however still strongly affected by total ionizing dose damages, since thick auxiliary oxides, such as Shallow Trench Isolation [61] and spacers [62], are present. These oxides can still be sensitive to TID effects, and the charge trapped therein can lead to substantial variations in the performance of MOS transistors [33, 63, 64]. The two dielectric structures are responsible for different types of damages. STI oxides, used to isolate adjacent MOSFETs, are responsible for the generation of a radiation-induced drain to source leakage current path [65, 66] and the radiation-induced narrow channel effects (RINCE) [33]. The spacers, located along the sides of the polysilicon gate to allow the implantation of Lightly Doped Drain (LDD) extensions [62], are responsible for the radiation-induced short channel effects (RISCE) [33]. Spacers have also a key role in the dose-rate effect. The aim of this chapter is to briefly describe the different type of radiation damages. Deeper explanations are provided by Borghello in [67]. Since the thickness of both STI and spacer oxides is comparable with the thickness of old technology node [55] it is possible to apply the theoretical knowledge on trapped charge disposition inside the gate dielectric and the relative effects on MOSFET parameters, previously acquired. For example [33, 59] still assume that the trapped charge distribution in the STI and spacer oxides does not vary from the extensively analysed for the gate insulator. It has to be mentioned that the electric field crossing the auxiliary oxides is different from that present in the gate oxides, therefore both the transport and the charge trapping mechanisms may be different from those analyzed in gate oxides.



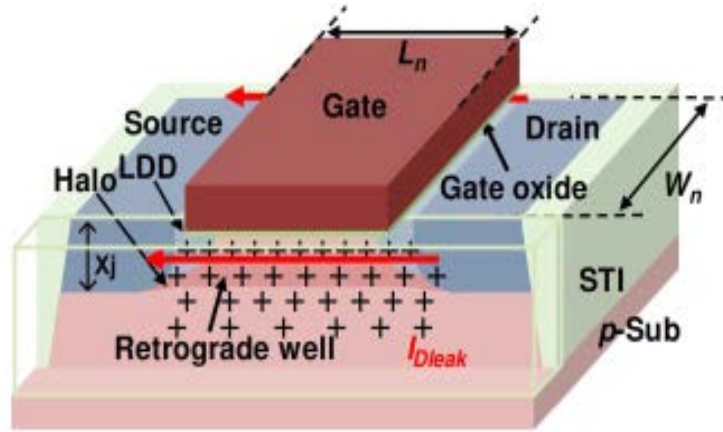
**Figure 4.1:** Graphical representation of the radiation induced narrow channel effect (RINCE). In narrow transistors the electric field generated by the charge trapped in the STI influences a larger percentage of the channel, limiting the current flowing between source and drain. Courtesy of G. Borghello, taken from [67].

## 4.1 STI-Related Effects

The effects of the presence of the STI have been studied for more than 20 years. In [65], radiation effects on STI irradiated up to 300 krad( $\text{SiO}_2$ ) have been studied. A deep understanding on extremely high TID levels effect on the fore mentioned structures have been acquired and reported in [33]. In this section, two phenomena that can significantly affect the radiation hardness of nano-scale MOSFET exposed to ultra-high TID levels will be described: the radiation induced narrow channel effects (RINCE) in Section 4.1.1 and radiation induced drain to source leakage current in Section 4.1.2.

### 4.1.1 RINCE Effects

The acronym RINCE has been coined by Faccio and co-workers in [33], to describe an unexpected channel width dependence of the radiation response of MOS transistors. RINCE effect is present in all modern technology nodes and has common characteristics in all the devices studied. Faccio and co-workers irradiated up to 500 Mrad( $\text{SiO}_2$ ) a 65 nm technology node chip, which contained devices with a significant channel length,  $L = 1 \mu\text{m}$ , and different channel widths, ranging from 120 nm to  $1 \mu\text{m}$ . The devices were irradiated at  $25^\circ\text{C}$  in diode configuration ( $|V_{\text{GS}}| = |V_{\text{DS}}| = 1.2 \text{V}$ ). The structures showed a smaller percentage degradation in the drive current,  $I_{\text{ON}}$ , as the channel length increased. RINCE can be understood referring to Figure 4.1. The electric field generated by the positive charge trapped in the STI region close to the interface reduces the effective width of the channel, resulting in a reduced current output. For larger channels, the mentioned electric field is not a concern, since a smaller percentage of the channel is affected by the trapped charge.



**Figure 4.2:** Parasitic path between source and drain, due to charge trapped in the STI. After [69] IEEE © 2017.

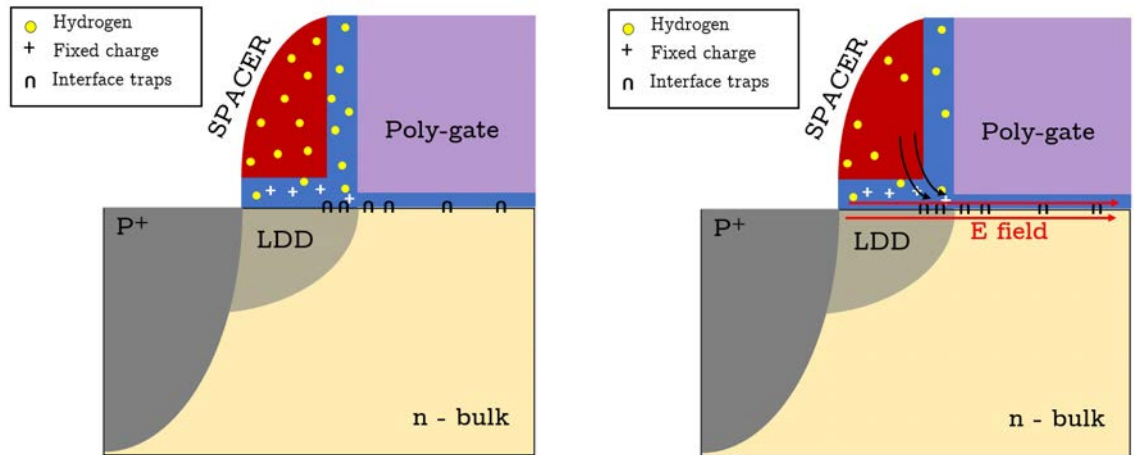
### 4.1.2 Radiation-Induced Drain to Source Leakage Current

The increase in the leakage current ( $I_{\text{OFF}}$ ), defined as the drain-to-source current flowing when  $V_{\text{GS}} = V_{\text{DS}} = 0 \text{ V}$ , is one of the major problems in CMOS technology exposed to TID, as it can cause considerable increases in the static power dissipation [68]. It is a well known phenomenon, reported, as an example, in [66] and [65]. More recent studies, e.g. [69] or those reported in Chapter 6, discovered that the increase in the leakage current is a serious issue even for the 28 nm technology node. The cause of increase in the leakage current is the activation of a parasitic transistors along the STI, as reported in Figure 4.2. The positive charge trapped in the STI can attract a considerable amount of electrons from the silicon bulk, forming a conductive path between source and drain. PMOS transistors are intrinsically immune to an increase in the leakage current, since their carrier are positively signed, as the charge trapped in the oxide [9]. As reported in [67],  $I_{\text{OFF}}$  cannot be controlled through variations in the gate voltage. This behaviour suggests that the charge responsible for the opening of this parasitic path is trapped relatively far from the STI-gate corner. The increase in the leakage current is not present in devices exposed to ionizing radiation if the gate bias is absent during irradiation. It means that, thanks to the imposition of positive gate voltages, the positive charge trapped close to the STI-gate corner is repelled further in the STI structure. The observation just proposed is in accordance with [70] in which they modeled the radiation-induced charge distribution in STI structures. They noticed that the charge inside the STI are repelled by the vertical electric field generated by the positive gate bias, hence less ionizing-induced charge is trapped close to the top of trench.

## 4.2 Spacers-Related Effects

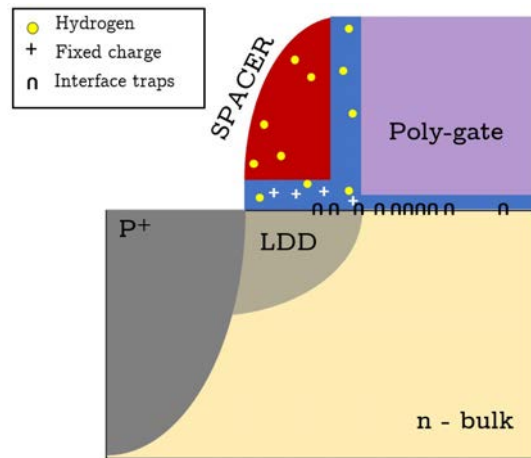
Spacers are heterogeneous insulator layers used during manufacturing process in advanced CMOS technologies, located along sides of the polysilicon gate. The presence of these oxides allows the implantation of Lightly-Doped Drain (or LDD) extensions. The first layer, close to the silicon interface, is composed by  $\text{SiO}_2$ . Then, a thick layer of  $\text{Si}_3\text{N}_4$  surmount the silicon dioxide [71]. The studies on spacer-related effects

on radiation response of MOS transistors begun just some years ago. In addition, the influence of oxide traps located in the spacer appears only at extremely high total ionizing dose (much higher than 1 Mrad(SiO<sub>2</sub>)), so these dielectrics are not a concern for the vast majority of spatial applications. Large part of the discoveries are reported in [33]. In the cited paper, Faccio and co-workers noticed a channel length dependence in the evolution of the drain current in irradiated devices. They coined the definition Radiation-Induced Short Channel Effect, or RISCE [33]. In the experiments, they irradiated, in diode configuration and at 25 °C up to 400 Mrad(SiO<sub>2</sub>) transistors with a considerable channel width ( $W = 20 \mu\text{m}$ ), and a channel lengths varying between 60 nm and 10  $\mu\text{m}$ . The channel width assures that the presence of the STI can be totally neglected. They saw, both for nMOS and pMOS, a more severe degradation in the output current for shorter devices. In addition, a 100 hours long annealing at 100 °C produced an additional dramatic deterioration in pMOS, while nMOS did not faced any drastic change in the output current, just a light recover. Radiation effect related to the presence of the spacers is a multiple stages process. In the first stage, the radiation-generated holes are trapped in fixed charges in the bulk of the dielectrics (Figure 4.3a) and free H<sup>+</sup>, which depassivate the interface traps mostly located at the spacer/drain interface. The drain-to-source resistance,  $R_{SD}$  rises for pMOS since positive oxide- and interface-trapped charges repel holes in the LDD extensions, causing a rise in the series resistance, while, for nMOS, the net evolution of this parameter is determined by the balance between the positive charges trapped in the oxide and the negative interface traps. In the second stage, the presence of bias pushes the hydrogen ions into the gate oxide, where they depassivate the Si-H bonds and create interface traps (Figure 4.3b and 4.3c). These interface traps located along the gate Si/SiO<sub>2</sub> interface and produce a threshold voltage shift that can reach hundreds of mV [63]. This stage is influenced by temperature. In fact, for nMOS devices, both the increase in series resistance and the threshold voltage shifts take place at room temperature, while for pMOS the second mechanism is thermally activated by high temperature. In addition, the devices become asymmetric, which means that drain and source are electrically different, because during irradiation and/or annealing  $V_{DS} \neq 1.2 \text{ V}$ .



(a) Holes trapping in the oxide and depassivation of interface traps due to  $H^+$

(b)  $V_{DS}$  helps the drift of  $H^+$  and promotes the depassivation of Si-H bonds.



(c) Generation of interface traps under the gate, due to the drift of  $H^+$  ions.

**Figure 4.3:** Multiple stage ionizing process in the spacer oxides. The hydrogen ions are reported in yellow, while the positive fixed charge is represented by a + sign. The interface traps are represented with a  $\square$ .



# Chapter 5

## Low Dose Rate Effect on 65 nm Node MOSFET

### 5.1 Introduction

The absence or the presence of a possible enhancement in the radiation-induced degradation for MOSFETs as the dose-rate decreases has been a point of discussion for the researcher interested in ionizing radiation effects since the discovery of the ELDRS in BJT structures [38, 39, 72, 73]. Traditionally, the DR effect on MOSFET oxides is considered absent [9]. In the past, the charge trapped in the gate oxide was the the main cause of radiation-related damages. As reported in [74], gate oxide strongly differs from the parasitic insulator used in the BJT, e.g. extremely high levels of purity are required for the gate oxide [75]. The parasitic oxides, which are the main cause of radiation-induced degradation in more recent technologies, contain generally many defects, are much thicker than the gate oxide and are crossed by small electric fields. They are hence more similar to BJT insulators, in which the DR dependence is measured. During this year of experiments, many analysis on the dose-rate effect have been carried out. This phenomenon, previously observed in [13] for the 65 nm technology node, has been further analyzed and understood. It will be shown that the main cause of the enhanced dose-rate sensitivity measured in the studied devices has been traced in the presence of the spacer oxides. This unexpected result shows how these oxides, despite only recently studied [33, 63, 76], contribute fundamentally to the radiation response at ultra-high doses. On the other hand, the effects related to the presence of the STI seem to be only slightly influenced by the dose-rate, except for a recent and not yet clearly understood effect called Ultra-high-dose Drain Current Increase (UDCI) [67]. In this chapter we will also present a study about the impact of the applied bias on the dose-rate effects in CMOS technologies exposed at ultra-high doses. To the best of our knowledge, this is the first time that such a study has been carried out. In addition, the set of experiments reported in Section 5.3.5 covers the radiation response at  $-30\text{ }^{\circ}\text{C}$  and different DRs. This is a crucial study for CERN applications, because the electronic parts of the HL-LHC subjected to the highest ionizing doses will be constantly kept at this temperature [77]. The results will be shown first for n-type devices, in which this DR effect is more evident. A brief discussion for the pMOS will follow.

	nSOURCE	VSS	
	pSOURCE	VDD	
	pGATE1	nGATE1	
	pGATE2	nGATE2	
	pGATE3	nGATE3	
	pGATE4	nGATE4	
Diode	nDRAIN1 ELT 1.32 $\mu\text{m}$ x 60 nm	nDRAIN1 ELT 1.32 $\mu\text{m}$ x 60 nm	Diode
Diode	nDRAIN1 120 nm x 10 $\mu\text{m}$	nDRAIN1 120 nm x 10 $\mu\text{m}$	Diode
Diode	nDRAIN1 1.32 $\mu\text{m}$ x 60 n	nDRAIN1 1.32 $\mu\text{m}$ x 60 n	Diode
Diode	nDRAIN2 ELT 1.32 $\mu\text{m}$ x 60 nm	nDRAIN2 ELT 1.32 $\mu\text{m}$ x 60 nm	Diode
Diode	nDRAIN2 120 nm x 10 $\mu\text{m}$	nDRAIN2 120 nm x 10 $\mu\text{m}$	Diode
Diode	nDRAIN2 1.32 $\mu\text{m}$ x 60 n	nDRAIN2 1.32 $\mu\text{m}$ x 60 n	Diode
Only $V_{DS}$	nDRAIN3 1.32 $\mu\text{m}$ x 60 n	nDRAIN3 1.32 $\mu\text{m}$ x 60 n	Only $V_{DS}$
Only $V_{DS}$	nDRAIN3 120 nm x 10 $\mu\text{m}$	nDRAIN3 120 nm x 10 $\mu\text{m}$	Only $V_{DS}$
Only $V_{GS}$	nDRAIN4 1.32 $\mu\text{m}$ x 60 n	nDRAIN4 1.32 $\mu\text{m}$ x 60 n	Only $V_{GS}$
Only $V_{GS}$	nDRAIN4 120 nm x 10 $\mu\text{m}$	nDRAIN4 120 nm x 10 $\mu\text{m}$	Only $V_{GS}$

**Figure 5.1:** Test structure used to carry out LDR experiment. The 6 separated gates, 3 for nMOS and 3 for pMOS, allow the possibility to apply different biases to different transistors.

## 5.2 Experiment Details

Figure 5.1 depicts a schematic representation of the test structure used to carry out this experiment. In the proposed structure, there are three different types of devices:

- ELTs with  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$ , used to completely exclude the STI-related effects.
- $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$ . Their radiation response is dominated by the STI while spacer-related effects are strongly mitigated.
- $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$ , are useful to evaluate the impact of both STI and spacers in the same device. Moreover, their  $W/L$  ratio is the same of the ELTs, giving us the possibility to easily compare their radiation response.

The diode configuration - known to be the worst-case condition during irradiation for high doses experiments for this technology node [33] - has been used for two devices of all  $W/L$  ratios, to have a "backup" in case one of the two diode-connected MOSFETs encounters malfunctions during the experiment. The presence of devices biased with only  $|V_{GS}| = 1.2 \text{ V}$  or  $|V_{DS}| = 1.2 \text{ V}$  allows us to recognize if one of the two biases has a major contribution in the results. The chips were irradiated up to 50 Mrad( $\text{SiO}_2$ ) with different dose-rates, namely 0.1 Mrad( $\text{SiO}_2$ )/h which is considered a low dose-rate, 0.5 Mrad( $\text{SiO}_2$ )/h which is a medium dose-rate, 1 Mrad( $\text{SiO}_2$ )/h and 10 Mrad( $\text{SiO}_2$ )/h that correspond to high dose-rate. It has to be mentioned that electronic components for CERN HL-LHC upgrade detectors can accumulate TID of up 1 Grad( $\text{SiO}_2$ ) in 10 years, with a dose-rate around 0.01 Mrad( $\text{SiO}_2$ )/h [77], which is 10 times lower of the lowest dose-rate used in this analysis<sup>1</sup>. Unfortunately,

<sup>1</sup>Not that not all the electronics components are placed closely to the interaction point. Electronics collocated far from the interaction point will never reach 1 Grad( $\text{SiO}_2$ ) over 10 years, but the expected TID is around hundreds of Mrad( $\text{SiO}_2$ ). Note that for this devices the dose-rate would be even smaller than the 0.01m Mrad( $\text{SiO}_2$ )/h expected, which is surely a worst-condition for the DR effect.



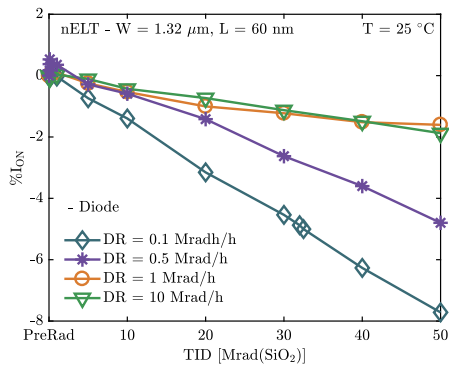
it was not possible to conduct experiment with dose-rates lower than the used one, since they would have been too time requiring.

### 5.3 Results for the n-Channel MOSFETs

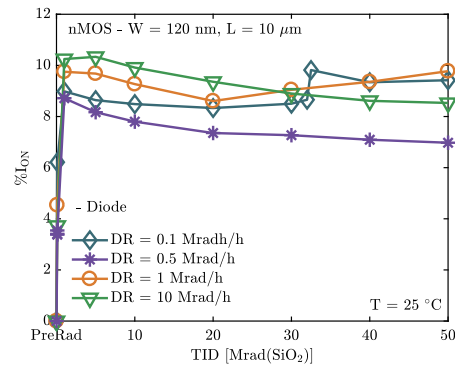
The drive current,  $I_{ON}$ , is a parameter often useful to summarize the degradation of the electrical characteristics that occurs in a MOSFET during irradiation. Deviations from its pre-irradiation value can be in fact the result of changes in several parameters, such as, e.g., threshold voltage, transconductance and sub-threshold swing. In addition, having the knowledge on the maximum current provided by the device is fundamental in any application. For this reasons, the analysis on n-channel devices starts showing the percentage variation of the drive current (Figure 5.2) in function of TID for the whole set of DRs used in these experiments, biased in diode configuration and exposed at  $T = 25^\circ\text{C}$ . The pre-irradiation measurements for the  $0.5 \text{ Mrad}(\text{SiO}_2)/\text{h}$  experiment are not completely reliable, due to problems with the probing of the chip. In any case, they still provide results that are qualitatively correct. The short channel devices ( $L = 60 \text{ nm}$ ) represented in Figure 5.2a and 5.2c undergo more significant damages as DR decreases. At  $\text{TID} = 50 \text{ Mrad}(\text{SiO}_2)$ , the drive current of the ELT structure shows a  $-8 \%$  variation (Figure 5.2a) and the standard MOSFET device reduces its output current of  $-12 \%$  (5.2c). The larger degradation in the not-enclosed device with respect to ELTs is caused by the charge trapped in the STI. It is interesting to observe that the drive current rises at the very begin of the irradiation ( $\text{TID} < 2 \text{ Mrad}(\text{SiO}_2)$ ), while it rapidly decreases for higher TID levels. Oxide traps, which are positively signed, are the responsible for this rise in the drive current. As the TID approaches higher levels, interface traps tend to limit the effect and then prevail over the oxide traps, producing this constant decreases in the  $I_{ON}$ . On the other hand, the long/narrow channel device ( $W/L = 120 \text{ nm}/10 \mu\text{m}$ ) does not present any significant dose-rate effect (Figure 5.2b). Figure 5.3 shows the evolution of the drive current in function of the TID for different bias configurations, for the highest and lowest dose-rates. The ELTs are not reported since they were polarized only in diode configuration. From this figure, it is clear that the absence of one between the drain bias or the gate bias strongly decreases the DR sensitivity of the devices. For narrow and long transistors, a particular phenomenon, called in [67] Ultra-high dose Drain Current Increase (UDCI), is clearly visible. Narrow/long devices irradiated with  $V_{GS} = 0 \text{ V}$  and  $V_{DS} = 1.2 \text{ V}$  show a constant increase in the drain current, even at ultra-high doses. This effect, related to the presence of the STI and not yet clearly understood, seems to be dependent on the dose-rate, with a larger evolution at lower DRs.

The  $I_D$  vs  $V_{GS}$  characteristics of the measured devices are reported in Figure 5.4. The solid lines correspond to the pre-irradiation curves, while the dashed are related to the post-irradiation condition. Drive current degradation is more severe for short channel devices (Figures 5.4a, 5.4b, 5.4e and 5.4f) than for long channel MOSFETs. In addition, the TID does not affect sub-threshold region (e.g. no radiation-induced drain to source leakage current), independently from channel width and/or length.

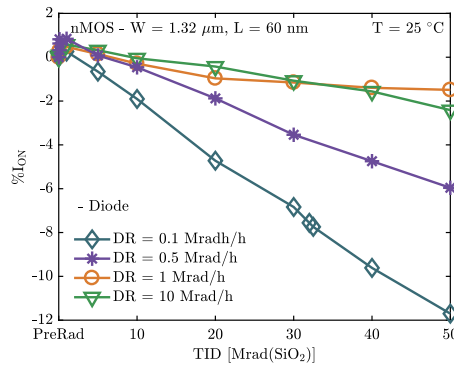
The solely observation that the experiment conducted with  $0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$  provoke more severe degradation, does not allow us do draw a definitive conclusion about an eventual true dose-rate dependence. In fact, the HDR experiment is 100 times faster than the LDR one, therefore the time-scales are different. Previous



(a) nELT  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$

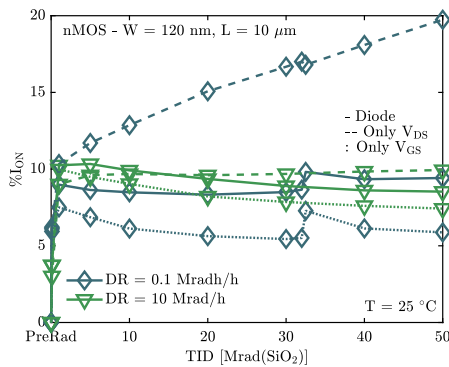


(b) nMOS  $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$

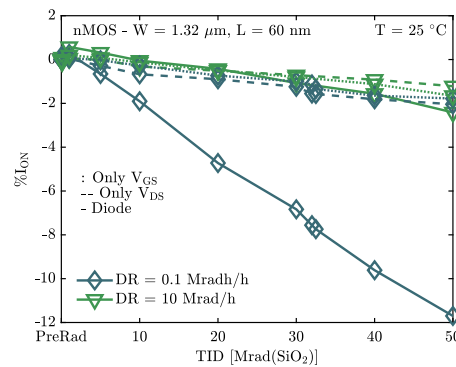


(c) nMOS  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$

**Figure 5.2:**  $I_{ON}$  percentage variations in function of TID for the n-MOS transistors, irradiated with different DRs up to  $50\text{Mrad}(\text{SiO}_2)$ . The devices are biased in diode configuration. A lower DR provokes a higher degradation in short-channel devices. (5.2a - 5.2c)



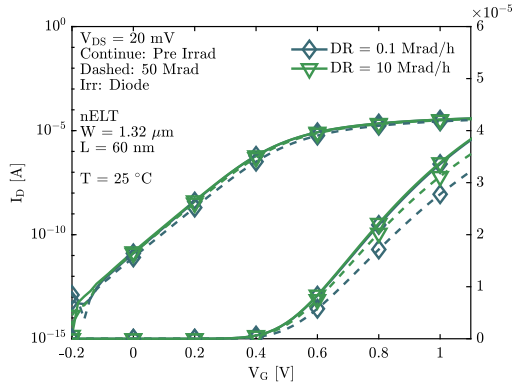
(a) nMOS  $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$



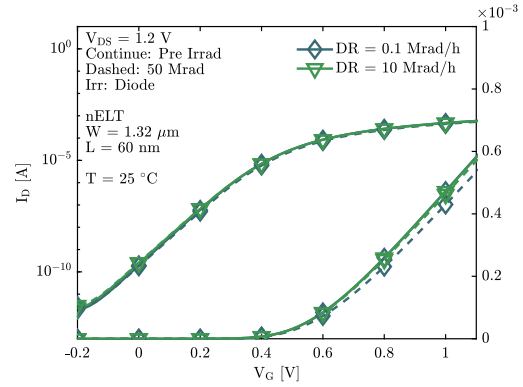
(b) nMOS  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$

**Figure 5.3:**  $I_{ON}$  percentage variations in function of TID for n-MOS transistors irradiated at 10 and 0.1  $\text{Mrad}(\text{SiO}_2)/\text{h}$  with different bias configurations.

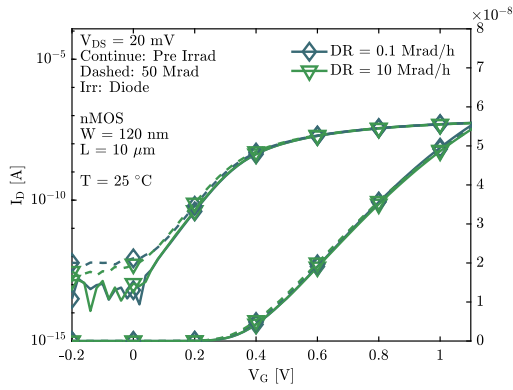
### 5.3. Results for the n-Channel MOSFETs



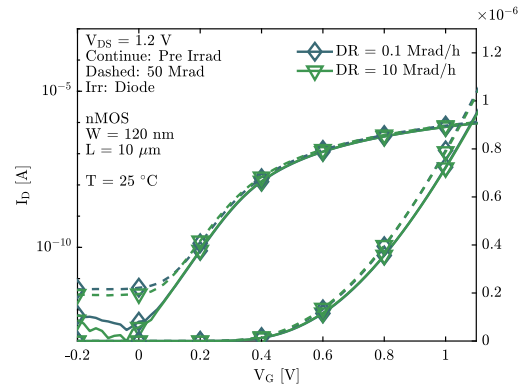
(a) Linear - nELT  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$



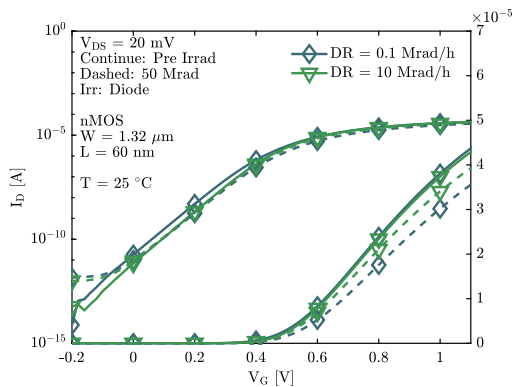
(b) Saturation - nELT  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$



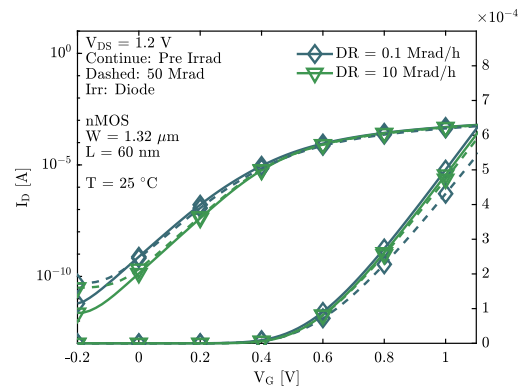
(c) Linear - nMOS  $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$



(d) Saturation - nMOS  $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$

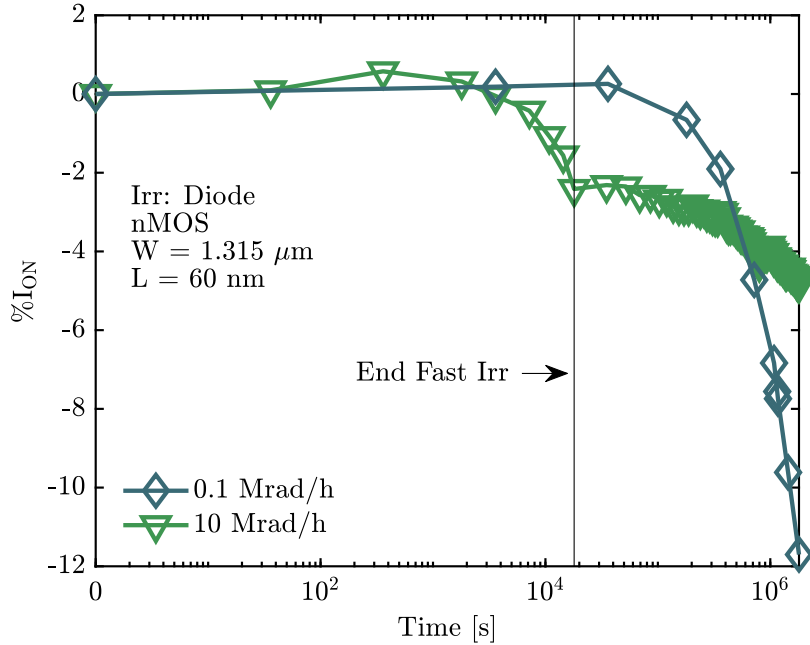


(e) Linear - nMOS  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$



(f) Saturation -  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$

**Figure 5.4:**  $I_D$  vs  $V_{GS}$  curves in linear (left) and saturation (right) region for all nMOS devices, irradiated with the highest and lowest dose-rates (10 Mrad( $\text{SiO}_2$ )/h and 0.1 Mrad( $\text{SiO}_2$ )/h) in diode configuration.



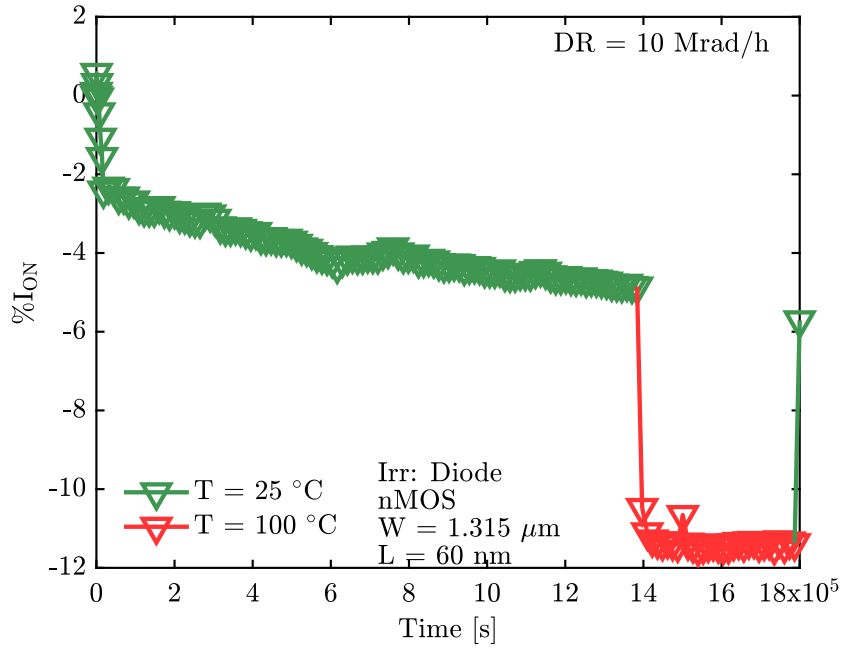
**Figure 5.5:** Drive current degradation for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  devices, irradiated with the highest (green) and lowest DRs (blue). The time is reported on the horizontal scale. After the end of 10 Mrad( $\text{SiO}_2$ )/h irradiation, the MOSFET underwent a long room temperature annealing, which allowed us to exclude times dependent effects.

studies [78, 79] suggested that, in order to exclude time-dependent annealing effects, it is necessary to keep under the same bias condition and at the same temperature the chip irradiated at HDR, until it is possible to compare LDR and HDR experiments over the same time scale. The LDR experiments took approximately 21 days of irradiation, while the HDR experiments took just 5 hours of irradiation. The devices irradiated with a HDR were kept under annealing for almost 3 weeks and measured every 5 hours. In Figure 5.5 is reported what we observed. Despite the  $I_{\text{ON}}$  evolves during annealing, the chip irradiated at LDR still presents greater degradation – almost the double of the HDR one. As previously observed in other experiments conducted on the same technology node, e.g. [33, 63], high temperature accelerates the time-dependent processes. To observe if this is the case, the chip annealed at room temperature, has been additionally annealed at  $T = 100^\circ\text{C}$  and kept in this condition for almost 5 days. From Figure 5.6 it is possible to notice that there is only an almost negligible evolution (around 1%).

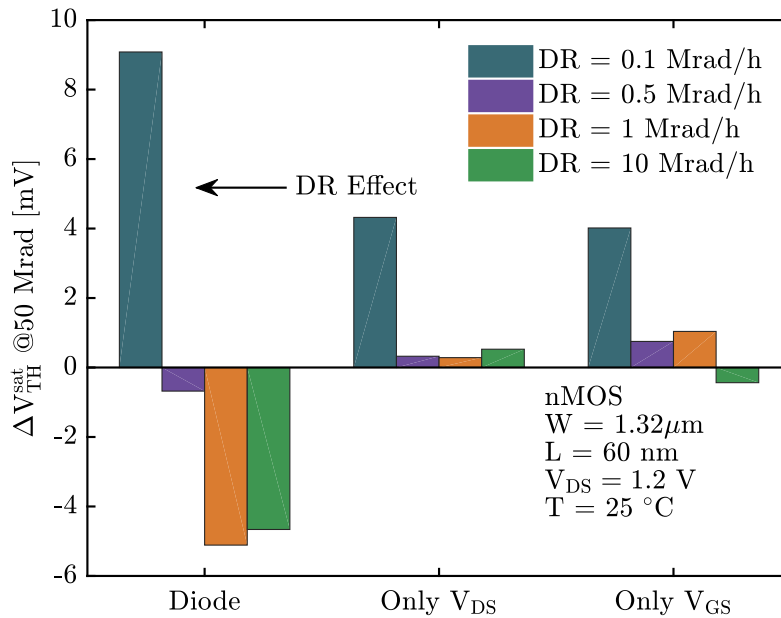
In the next subsections we will study how threshold voltage, transconductance and subthreshold swing change in function of the dose-rate.

### 5.3.1 Threshold Voltage

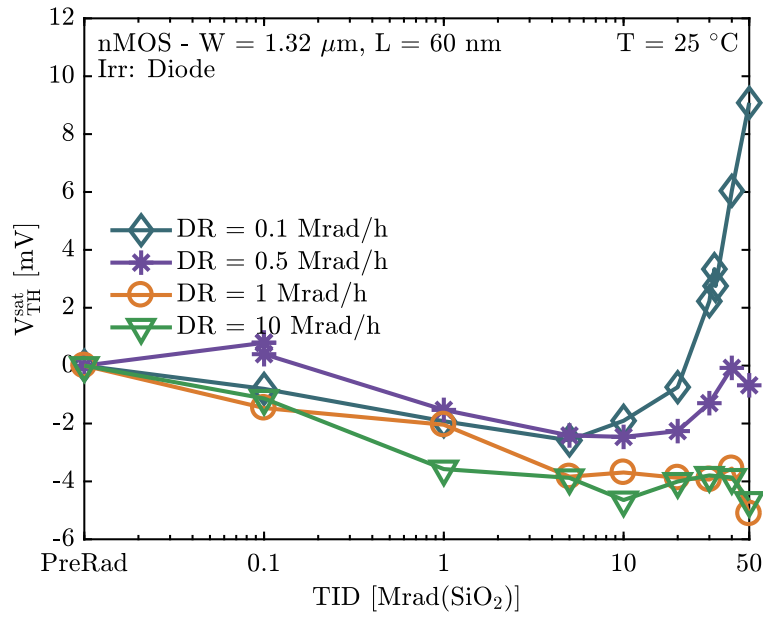
Figure 5.7 shows the threshold voltage shift (calculated with the device operating in saturation zone, with  $V_{\text{DS}} = 1.2 \text{ V}$ ) measured at  $\text{TID} = 50 \text{ Mrad}(\text{SiO}_2)$ , for the large and short n-channel devices. The pre-irradiation average value of this parameter, calculated using all the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  n-MOSFETs, is 337 mV, with a standard deviation of 16 mV. The radiation-induced variations of  $V_{\text{TH}}$  are smaller



**Figure 5.6:** High temperature annealing for the devices reported in Figure 5.5. The high temperature does not produce any substantial evolution in the I<sub>ON</sub>.



**Figure 5.7:** Threshold voltage variations for the W = 1.32 μm and L = 60 nm n-MOSFET, irradiated up to 50 Mrad(SiO<sub>2</sub>).

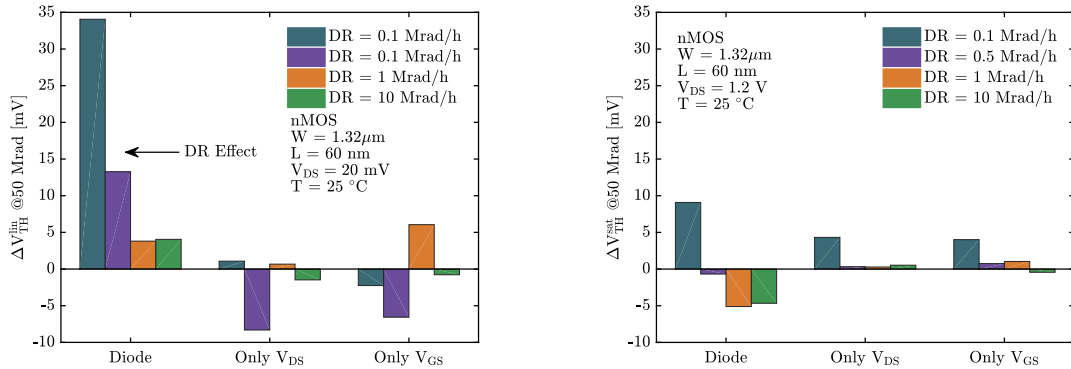


**Figure 5.8:** Threshold Voltage analysis for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  n-MOSFET. The Figure contains only the devices irradiated with a diode bias, for the all DRs.

than the pre-rad standard deviation. It is also interesting to observe a not monotonic behavior in the shift of the  $V_{\text{TH}}$  in function of the DR in the devices biased in diode configuration. The  $0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$  experiment produces a change of  $9 \text{ mV}$ , while all the other diode-biased devices undergo a small negative change. From Figure 5.8, it is possible to notice that the positive shift in the threshold voltage occurs only at low DR, and only above  $100 \text{ h}$  of irradiation. The positive threshold voltage shift in the device exposed to the lowest DR could indicate a more significant contribution of the negative charge trapped at the interface. Therefore, HDR irradiations seem to reduce charge trapping at the interface, which is in accordance with the models developed for the low dose-rate sensitivity in BJT structure, reported in Section 2.4.

Sometimes it may be worth to gain knowledge on the behavior of the threshold voltage calculated in linear operation mode ( $V_{\text{DS}} = 20 \text{ mV}$ ). In Figure 5.9a the shifts of  $V_{\text{TH}}^{\text{lin}}$  are hence reported, while in 5.9b the variations for the threshold voltage in saturation zone ( $V_{\text{TH}}^{\text{sat}}$ ) are recalled. It is interesting to observe that  $\Delta V_{\text{TH}}^{\text{lin}}$  is greater than  $\Delta V_{\text{TH}}^{\text{sat}}$ .

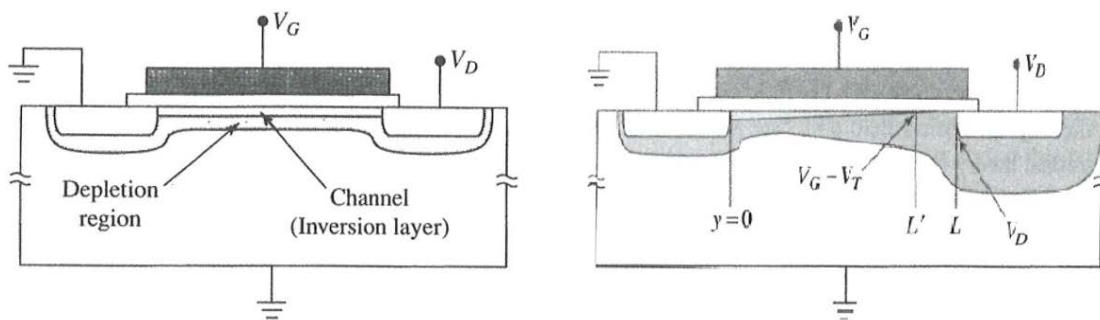
A possible first explanation of the difference in the behavior of  $V_{\text{TH}}$  measured in linear and saturation region is related to the variation of the spatial distribution of the carriers in the channel, in function of drain to source voltage. When the MOS is operating in linear zone, its channel directly connects source and drain terminals, as reported in the left part of Figure 5.10. On the other side, increments in the drain-to-source voltage, reduce the effective channel length, causing the pinch-off of the channel itself, as reported in the right section of Figure 5.10. When the channel is pinched-off, less interaction between the carriers and the charges trapped in the STI may occurs. However, the results measured for the ELTs allow reject this explanation. Since the channel does not interact with the STI oxides in this



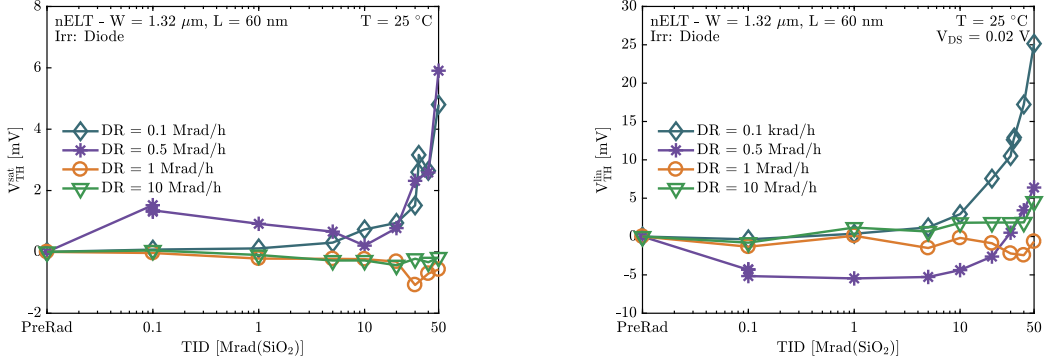
(a)  $V_{TH}^{lin}$  analysis for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  n-MOSFET

(b)  $V_{TH}^{sat}$  analysis for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  n-MOSFET

**Figure 5.9:** Comparison of the evolution of the threshold voltages for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  structure, both in linear (5.9a) and in pinch-off condition (5.9b).



**Figure 5.10:** MOSFET basic structure representation. The left image refers to the the MOS in linear operation, with the channel completely extending between source and drain terminals. The right part of the figure capture the pinch-off working point o a MOSFET, in which the channel length is reduced from  $L$  to  $L'$ . Taken from [80].



(a)  $V_{TH}^{\text{sat}}$  analysis for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  ELT n-MOSFET      (b)  $V_{TH}^{\text{lin}}$  analysis for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  ELT n-MOSFET

**Figure 5.11:** Comparison of the evolution of the threshold voltages for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  ELT structure, both in linear (5.11a) and in pinch-off condition (5.11b)

type of structure, then the changes in the threshold voltage calculated both in linear condition and in pinch-off operation mode should be mostly equal. As it is possible to notice in Figure 5.11, there is still a remarkable difference in the variations of the  $V_{TH}^{\text{sat}}$  and  $V_{TH}^{\text{lin}}$  for the ELT. Therefore, the interaction between the channel and the STI is not a valid explanation for the difference in the evolution encountered up to now. As it will be discussed later in 5.3.4, the different evolution of  $V_{TH}^{\text{sat}}$  and  $V_{TH}^{\text{lin}}$  may actually be related to the Drain Induced Barrier Lowering (DIBL) effect.

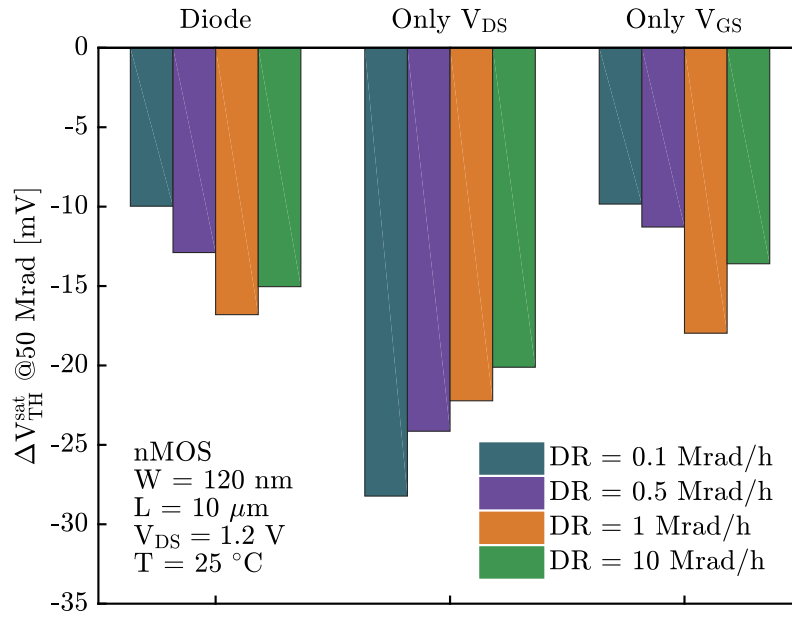
Figure 5.12 reports the variations of the threshold voltage, for the  $W = 120 \text{ nm}$  and  $L = 10 \mu\text{m}$  n-channel MOSFET. For these devices, there is no direct correlation between dose-rate and parameter variations, as already observed for the  $I_{ON}$ .

### 5.3.2 Transconductance

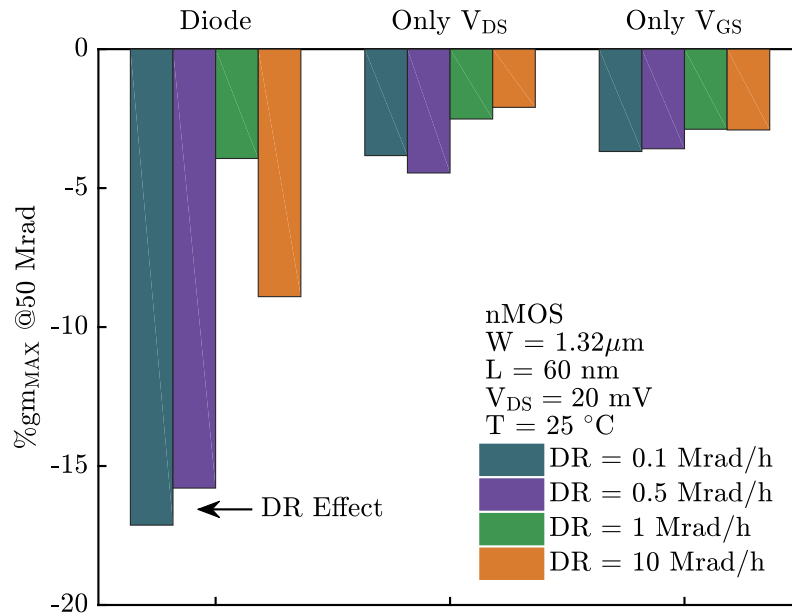
As for the threshold voltage, also the radiation-induced variation of the transconductance is dependent on the DR. It will be shown that the changes of this parameter have a stronger impact in the overall response. It has previously recognized that the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  device is sensitive to the DR, in both ELT and normal layout devices. Most of the comments on the transconductance will be proposed on the not-ELT MOSFET, since the DR effect is more easily distinguishable. Figure 5.13 shows the final percentage value reached by the peak of the transconductance ( $g_{m\text{MAX}}$ ) at the end of the irradiation, for the above mentioned device. The graph covers all the combinations of DRs and biases imposed in the set of experiments. In particular, for the device irradiated at  $0.1 \text{ Mrad(SiO}_2\text{)/h}$  in diode connection, the final value reached by  $g_{m\text{MAX}}$  is around -17%. As before, the device connected in diode configuration and exposed at the lowest dose-rate shows the largest degradation. Still from Figure 5.13, it is interesting to observe that Only- $V_{DS}$  and Only- $V_{GS}$  bias configurations strongly reduce the DR effect, as already observed for  $V_{TH}^{\text{sat}}$ .

Previous studies suggested that the degradation of the transconductance could

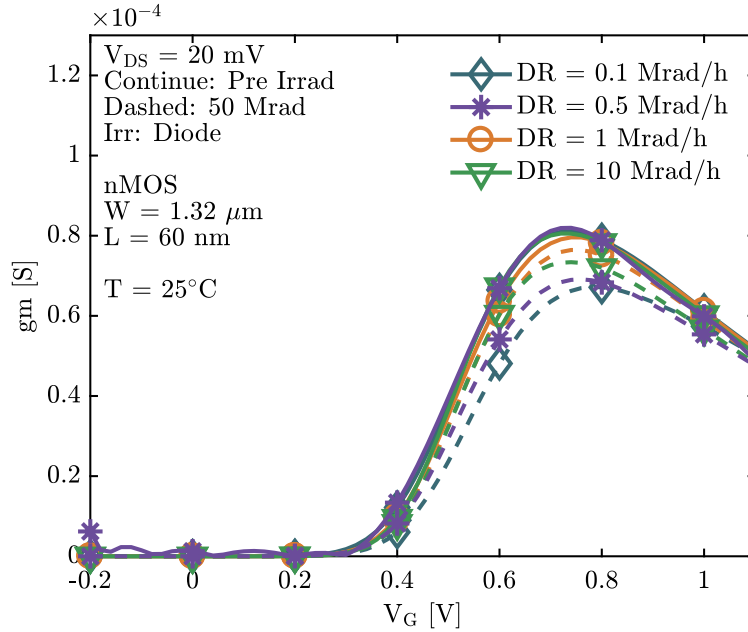




**Figure 5.12:** Threshold Voltage variations for the  $W = 120$  nm and  $L = 10$   $\mu$ m n-MOSFET, irradiated up to 50 Mrad( $\text{SiO}_2$ ). All the bias and DR are considered in the Figure.



**Figure 5.13:** Transconductance variation at 50 Mrad( $\text{SiO}_2$ ) for the  $W = 1.32$   $\mu$ m and  $L = 60$  nm nMOS.

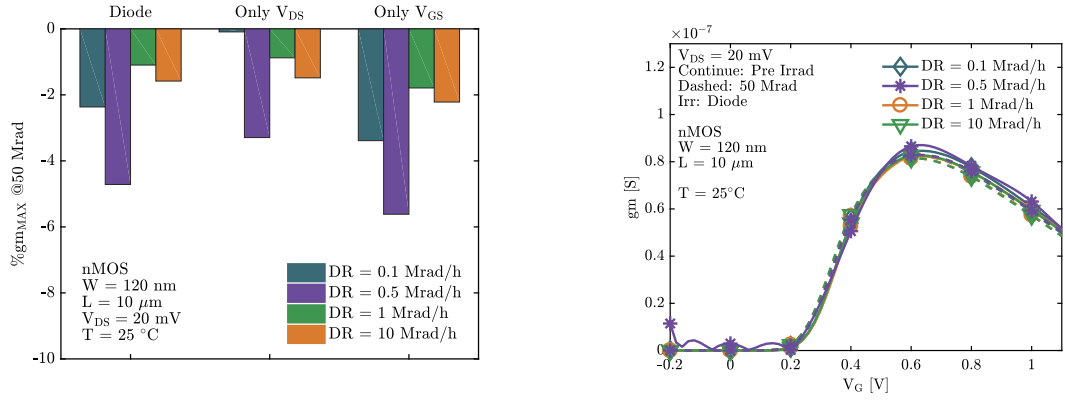


**Figure 5.14:** Transconductance comparison pre-post irradiation for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  nMOS.

be related to a rise in the series resistance [63, 76]. To state if our experiments agree with the observation proposed in those papers, it is worth to analyze the pre-irradiation and post-irradiation  $gm(V_{GS})$  curves. The changes of the transconductance in function of the TID are hence reported in Figure 5.14.

In [63], the transconductance undergoes a vertical translation when exposed to TID. This behavior was traced in an increase in the series resistance<sup>2</sup>  $R_{SD}$ , as also later confirmed with TCAD simulations by Bonaldo et al. in [76]. Moreover, vertical decreases in the peak of the transconductance were related to an increase in the series resistance also in [82]. However, in the curves reported in Figure 5.14, the degradation of the transconductance is not entirely caused by a vertical translation but is more evident close to the peak of the  $gm(V_{GS})$  curve while is reduced at higher  $V_{GS}$ . In other words, the pre- and post-irradiation characteristics tend to converge at  $V_{GS} = 1.2 \text{ V}$ . Note that the test chip used in the DR experiments comes from the same wafer that Faccio and co-workers used in their work [63], therefore we expect to see very similar behavior. To understand the different radiation-response of our samples with respect to those reported in [63, 76], we need first to notice that the model proposed in [63] was mainly developed from observation conducted on p-channel devices, because the transconductance of nMOS underwent a negligible degradation. In our tests, the dose-rate effect is more noticeable in n-channel transistors, and the transconductance degradation of these devices is not negligible, especially at low dose-rate. The differences between the behavior of nMOS and pMOS could indicate that different mechanisms dominate their radiation response. Note also that the same vertical translation measured in [63] can be seen in our pMOS, reported in Section 5.4.

<sup>2</sup>In [63], the series resistance was extracted with the method proposed by Fleury et al. in [81], which will be briefly reported in Appendix A.



(a) Percentage shifts of  $g_{m,MAX}$  calculated at 50 Mrad ( $\text{SiO}_2$ ) for the  $W = 120$  nm and  $L = 10$   $\mu$ m devices.

(b) Pre- and Post-irradiation  $g_m$  curves for the  $W = 120$  nm and  $L = 10$   $\mu$ m devices.

**Figure 5.15:** Complete analysis for the transconductance for the narrow and long device. No DR effect observed.

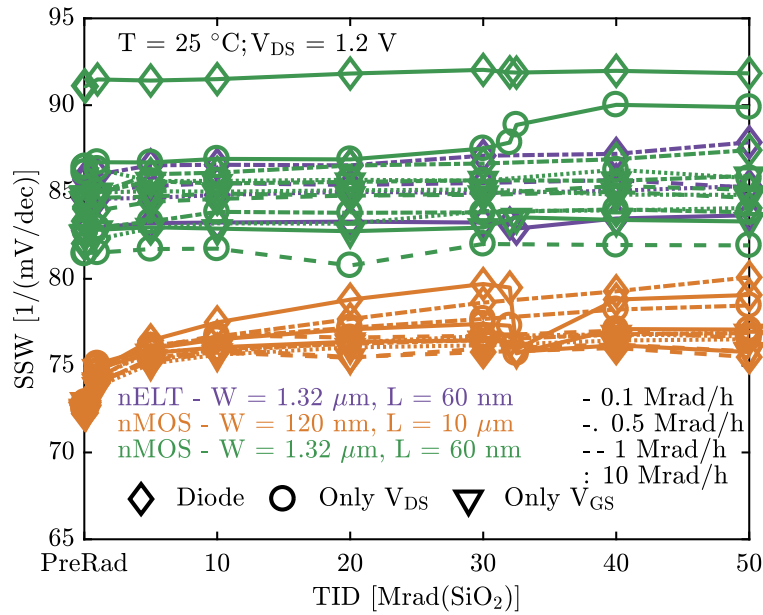
The vertical decrease that is present in the peak of the transconductance of our devices could still be related to rises in the  $R_{SD}$ , caused by an enhanced spacer/drain and/or spacer/source interface traps formation, encouraged at low DRs. However, the behavior of  $g_m(V_{GS})$  at high  $V_{GS}$  indicates that, rather than the series resistance, other not radiation-induced mechanisms dominate the reduction of the transconductance with the gate voltage. Moreover, the differences between nMOS and pMOS could also be related to the different effect of the charge trapped in the spacers oxides. While in pMOS they repel the carriers and increase the  $R_{SD}$  [63, 76], in nMOS they tend to accumulate charge close to the Si/SiO<sub>2</sub> interface. The effect of this accumulation is difficult to assess, but it certainly counterbalances the effect of negatively-charged interface traps. This complex picture and interaction of different phenomena requires more detailed studies to be clearly understood and safely used in a complete model of the degradation of nMOS devices. However, the simple model that we developed to explain the dose-rate effect (reported in Section 5.3.6) matches well with rises in the  $R_{SD}$ . This may indicate that, as for the pMOS, the degradation of the transconductance in nMOS devices is also mostly caused by a radiation-induced increase in the  $R_{SD}$ .

Not evident changes in the transconductance are observed for the narrow/long devices (Figure 5.15). In particular, since the charge trapping in the oxides of long channel devices occurs mostly in STI oxides, this curves is an additional confirmation that the dose-rate effect does not affect these insulators.

### 5.3.3 Sub-Threshold Swing

A parameter that can provide additional information about the impact of interface traps is the Sub-threshold Swing,  $S_{SW}$ , commonly measured in [mV/decade], and calculated as follows:

$$S_{SW} = \left[ \frac{\partial}{\partial V_G} \log_{10}(I_{DS}) \right]^{-1} \quad (5.1)$$

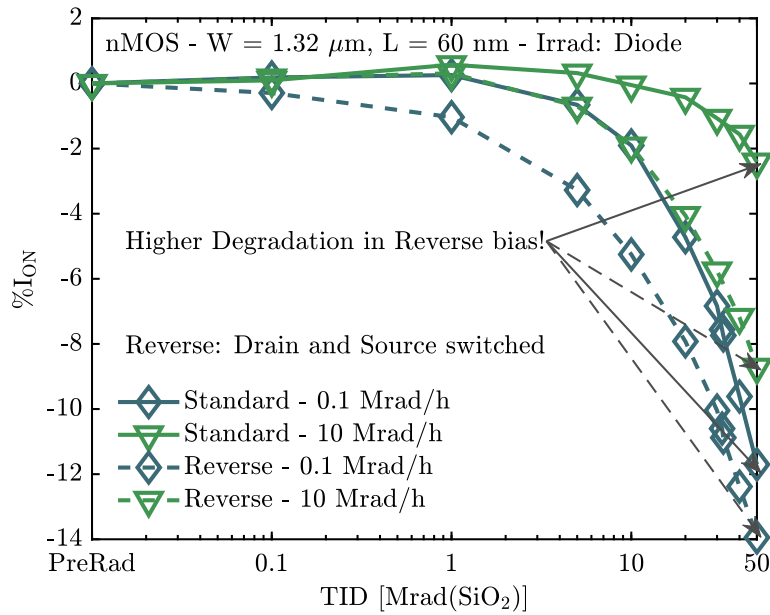


**Figure 5.16:** Sub-threshold swing evolution in function of TID for all the n-channel devices analyzed.

A strong presence of interface traps would cause a substantial increase in the  $S_{SW}$ , because the slope of the drain current in the sub-threshold region would reduce. The analysis of the  $S_{SW}$  may lead to the knowledge of the density of interface traps, see e.g. [83], and, in turn, to a possible correlation between dose-rate and the charge trapping at Si/SiO<sub>2</sub> interface. In Figure 5.16 the  $S_{SW}$  is therefore shown. It is clear that the changes in the  $S_{SW}$  are totally negligible since the parameter could be considered almost constant for the short channel devices and the small changes are not influenced by the DR. This means that the depassivation of the interface traps located along the channel is not DR dependent. The larger degradation encountered in short channel devices as the dose-rate decreases, may be hence caused by more charge trapped in the oxide and/or more depassivated interface traps between spacer oxide and drain/source terminals. From [76], in fact, interface traps which are not collocated along the channel have no influences in the sub-threshold zone, therefore their depassivation is not reflected as changes in the sub-threshold swing.

### 5.3.4 Interchangeability of Source and Drain

In the pre-irradiation condition, source and drain are simply determined by the bias applied. It is possible to interchange their roles, and the  $I_D$  vs  $V_{GS}$  curves would not change. If both the gate-to-source and drain-to-source biases applied during irradiation are not zero, the drain and the source in the post-irradiation behavior become two different electrical structures, because of asymmetric charge built up. This radiation-induced asymmetry is especially noticeable in short channel devices [63, 76]. In this case, interchanging the role of the terminals produces different  $I_D$  vs  $V_{GS}$  curves. In particular, after irradiation, the drain side of nMOS is more populated by charges trapped at the interface than the source, due to the drift of hydrogen ions from the spacers into the gate oxide. To analyze a possible



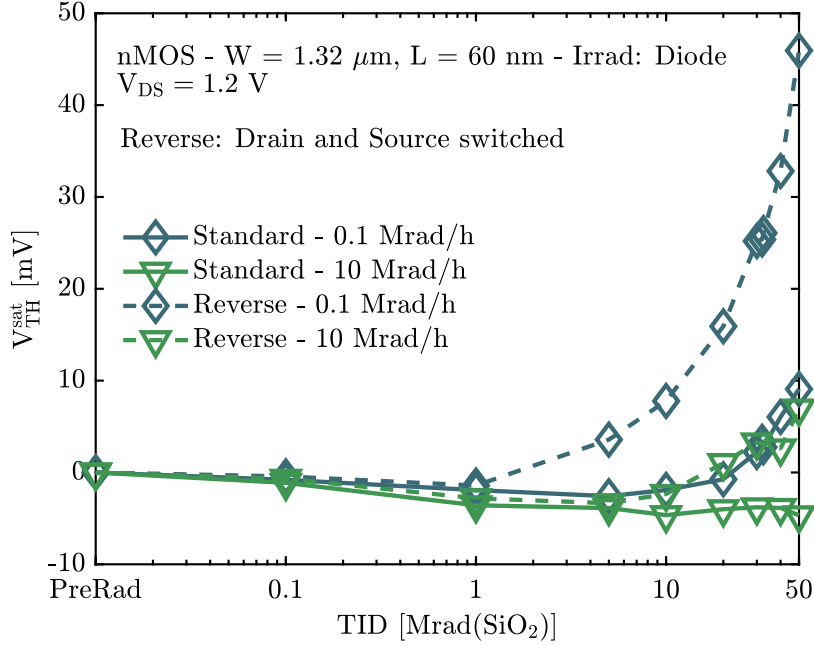
**Figure 5.17:** Standard (blue) and reverse (green) drive current degradation comparison for n-Channel MOSFET with  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$ .

**Table 5.1:** Standard and reverse drive current degradation comparison for n-Channel MOSFET with  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  irradiated at  $50 \text{ Mrad}(\text{SiO}_2)$  in diode configuration for lowest DR ( $0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$ ) and highest DR ( $10 \text{ Mrad}(\text{SiO}_2)/\text{h}$ ) experiments.

DR $\text{Mrad}(\text{SiO}_2)/\text{h}$	$I_{\text{ON}}$ std. %	$I_{\text{ON}}$ rev. %
0.1	-12	-14
10	-2	-9

correlation between changes in the DR and the enhancement in this asymmetric behaviour, the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  nMOS devices have been measured both in standard and in reverse configuration (with the drain and source switched between each other) for each step of irradiation. In Figure 5.17, the lowest and the highest DRs used in these experiments are compared for the structures irradiated in diode configuration. Dashed lines correspond to reverse configuration, while solid lines are related to standard use. It is possible to notice that, for both dose-rates considered, when devices are measured in reverse configuration they show a larger degradation with the respect to standard operation mode, as also reported in [63, 76]. In addition, the difference between the changes of the drive current  $I_{\text{ON}}$  among standard and reverse connected MOS is greater for the High-DR experiments, as also reported in Table 5.1.

Figure 5.18 shows the evolution of the threshold voltage of the devices irradiated with the lowest and highest DRs, measured both in standard (solid lines) and reverse (dashed lines) configuration. It is possible to notice that a lower dose-rate enhances the difference between the threshold voltages measured in standard and



**Figure 5.18:** Threshold voltage evolution during irradiation for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  n-MOS device. Presence of the reverse configuration analysis (dashed lines) for highest DR (green) and lowest one (blue).

reverse configuration. Previous studies conducted on the 65 nm technology node have linked this radiation-induced asymmetry to the Drain Induced Barrier Lowering (DIBL) [63]. DIBL is the threshold voltage shifts induced by a large drain voltage change  $\Delta V_{\text{DS}}$ , measured in  $\text{mV/V}$  [84]. This figure of merit is calculated in [67] with the following equation:

$$V_{\text{DIBL}} = -\frac{V_{\text{TH}}^{\text{sat}} - V_{\text{TH}}^{\text{lin}}}{V_{\text{DS}}^{\text{sat}} - V_{\text{DS}}^{\text{lin}}} \quad (5.2)$$

In particular, Faccio et. al. noticed an increase in the DIBL at the end of irradiation for the standard measured devices and a decrease for the inverse measured MOSFET [63]. We wanted to understand how DR may influences the evolution of the DIBL. Using Equation 5.2 we calculated the differences in the DIBL between the pre- and post-irradiation condition, both in standard and reverse configuration for different DRs. The results are reported in Table 5.2. We noticed that the experiment conducted with a low DR simply enhances the results obtained in the high DR tests.

In the remainder of this subsection we will describe how the DIBL evolves in function of the TID. This explanation is derived from what is reported in [63]. During irradiation, the bias imposed on these devices is  $V_{\text{GS}} = V_{\text{DS}} = 1.2 \text{ V}$ , hence the positive charged hydrogen ions produced in the spacers are continuously pushed from the drain side to the gate oxide, where they depassivate interface traps. On the other hand, the voltage applied on the source is always equal to 0 V and the applied  $V_{\text{GS}}$  tends to push the  $\text{H}^+$  far from the source-side of gate oxide. In Figure 5.19 a detailed explanation based on the surface potential lines allows to further explain the DIBL figure of merit. The physical source and drain are determined by the bias imposed during irradiation. The terminal used as drain is called  $D_p$

**Table 5.2:** Evolution of the DIBL for both standard and reverse structures. The lowest and highest DR are reported. Low dose-rates enhance what already discovered in [63].

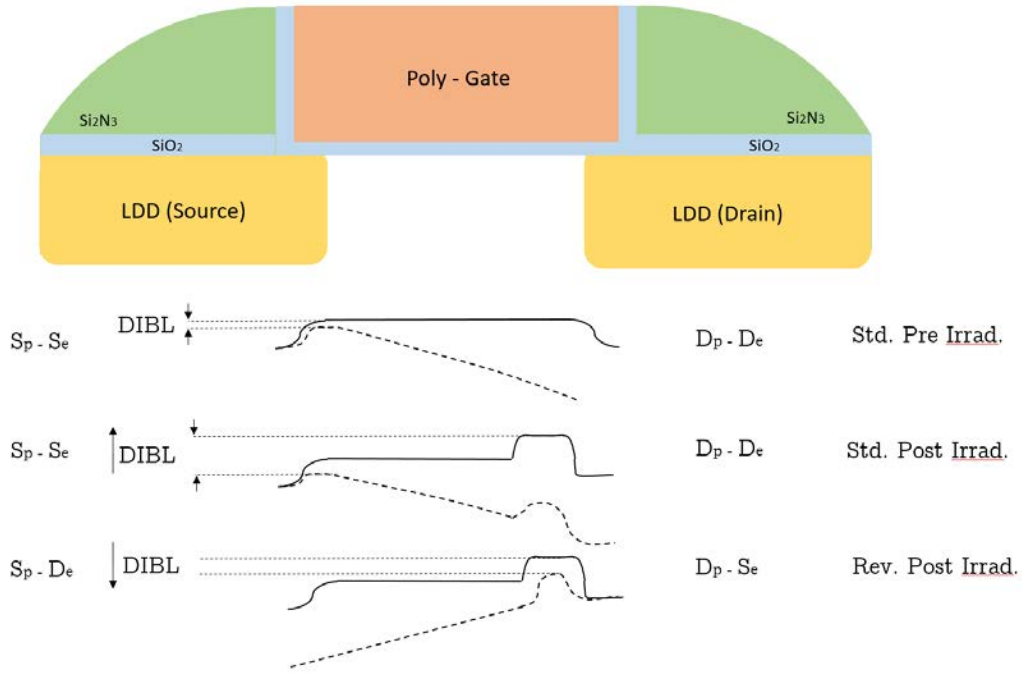
Operation	DR (Mrad/h)	DIBL <sup>pre</sup> (mV/V)	DIBL <sup>post</sup> (mV/V)	$\Delta$ DIBL (mV/V)
STD.	0.1	139.5	160.6	21.1
INV.	0.1	139.5	125.6	-13.9
STD.	10	125.7	133.1	7.4
INV.	10	125.7	123.4	-2.3

while the terminal used as source is called  $S_p$ . Once the irradiation starts, the asymmetric charge build-up process creates a strong distinction in the electrical behavior of the two terminals. To distinguish the two terminals during  $I_D$  vs  $V_{GS}$  measurements, it is necessary to define the electrical source and drain (respectively  $S_e$  and  $D_e$ ). When the device is measured in standard configuration, physical and electrical terminals coincide. When the device is measured in inverse configuration, the electrical drain and source swap roles, hence  $S_e = D_p$  and  $D_e = S_p$ . In the post-irradiation behavior, the asymmetric charge built-up process causes difference in the  $I_D$  vs  $V_{GS}$  curves between the standard and reverse configuration. In other words,  $I_{D_e}(V_{GS_e}) = I_{D_p}(V_{GS_p})$  in standard configuration, but  $I_{D_e}(V_{GS_e}) \neq I_{D_p}(V_{GS_p})$  in reverse. In Figure 5.19 the solid lines are referred to a transistor measured in linear region, in which  $V_{DS} = 20$  mV, so the drain potential is almost at the same level as the source. The dashed lines are related to the saturation condition, in which  $V_{DS} = 1.2$  V, therefore the potential line of the drain is notably lower than the source one. DIBL is related to the variation of the maximum of the potential barrier due to the voltage applied at the drain. During irradiation, the asymmetric charge built-up process rises the local potential, creating a “bump” of charge located close to drain side, which is visible in the post irradiation potential lines (second of three sets in Figure 5.19). It is possible to notice that, from the pre-irradiation condition, the DIBL raised, which can be seen as a rise in the difference between  $V_{TH}^{sat}$  and  $V_{TH}^{lin}$ . If the device is now measured in reverse configuration (third of three sets of lines), the potential of electrical source (which correspond to the physical drain) is the one determining  $V_{TH}^{sat}$ . In addition, from the second and the third sets of lines, it is clear that this asymmetry only appears for measurements in saturation, while in the linear regime of operation the transistor remains symmetric.

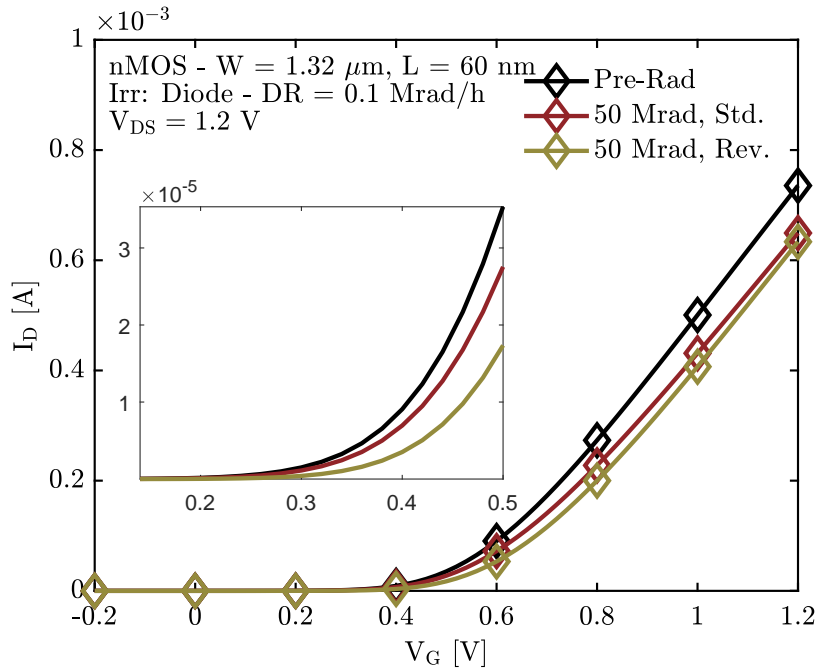
In conclusion, the pre- and post-irradiation  $I_D$  vs  $V_{GS}$  curves are reported in Figure 5.20. From the zoom part collocated inside the figure, it is possible to notice in detail the radiation-enhanced rises in the threshold voltage for the device operating in reverse condition.

### 5.3.5 Impact of Temperature

The temperature not only changes the behaviour of the devices, but also influences their response to radiation. In LHC applications, the electronic components that are mostly affected by TID damages are those closer to the interaction point. These devices are constantly maintained at a temperature around  $-30$  °C [77], which re-

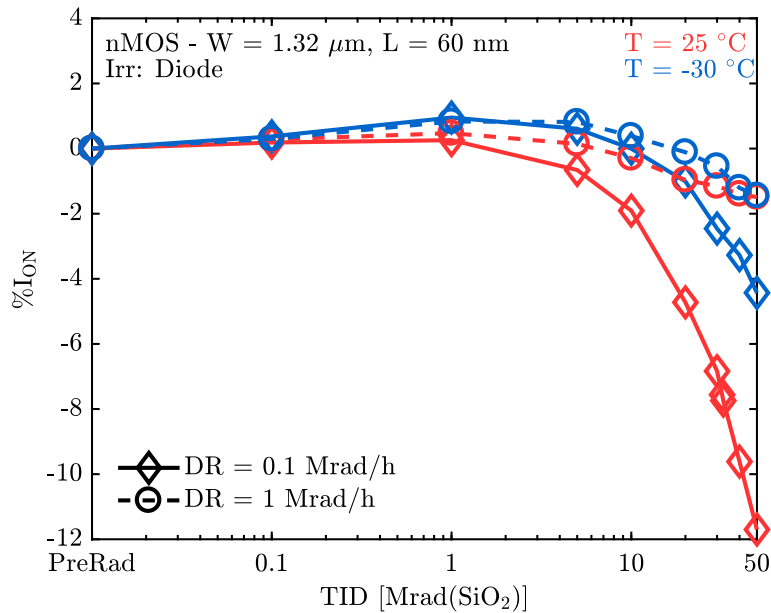


**Figure 5.19:** Representation of a generic MOSFET structure. The drain and source region and the relative LDD extensions are represented in yellow. The SiO<sub>2</sub> oxide part, used to create the gate and the inner part of spacers oxide is light-blue colored, while the outer part of the spacer, formed of Si<sub>2</sub>N<sub>3</sub> is shown in green. The poly-gate region is represented in orange.



**Figure 5.20:**  $I_D$  vs  $V_{GS}$  curves for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  device, plotted for  $V_{DS} = 1.2 \text{ V}$ . The solid black line correspond to the pre-irradiation case, the red one to the post-irradiation standard configuration and the yellow one to the post-irradiation reverse configuration. A visible  $V_{TH}^{sat}$  shift is present, while the slope of the curve is almost constant.





**Figure 5.21:** Drive current variation for n-MOS device with  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  in function of the TID both for high temperature and low temperature experiments.

duces the impact of TID in modern technologies as the 65 nm channel length node analyzed here [33, 63, 67]. However, the combined effect of temperature and dose-rate has never been evaluated for ultra-high doses. In this brief section we report the results of tests performed at  $T = -30^\circ\text{C}$  and different dose-rates.

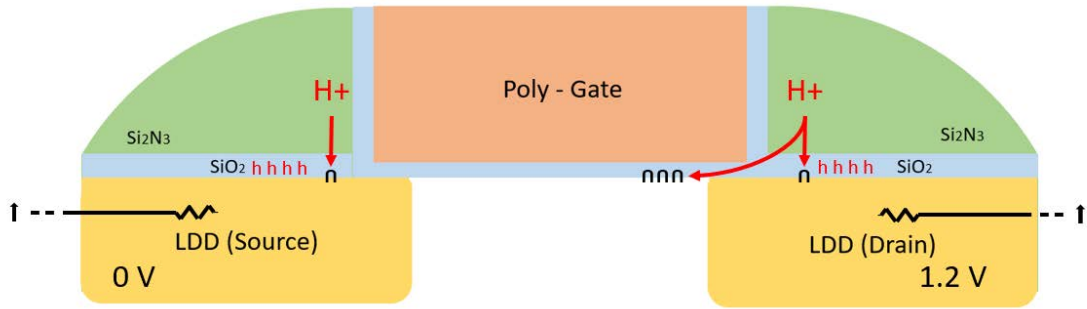
The 0.1 Mrad(SiO<sub>2</sub>)/h experiment (LDR) and the 1 Mrad(SiO<sub>2</sub>)/h experiment (HDR) were conducted both at 25 °C and at -30 °C. As can be seen in Figure 5.21, the differences between low and high dose-rate are significantly reduced for low temperatures, compared to those irradiated at  $T=25^\circ\text{C}$ . For CERN application this is a very encouraging result, due to the reason explained earlier.

This behavior is similar to the one that occurs in BJT, in which the higher the temperature, the weaker the oxide to the DR effect. In fact, as already reported in [85], lower temperature (actually much lower than the one used in this experiment, e.g. 125 K) reduces the ELDRS typical of BJT, exactly as for our devices.

### 5.3.6 Model for LDR effects in nMOS

In this subsection we will introduce a possible model, useful to understand how dose-rate may impact charge trapping in the spacer oxide. This model is based on what has been studied for the ELDRS mechanisms on BJT devices, e.g. [43, 44, 45, 46], and in particular the space charge model reported in Subsection 2.4.1. It is worth to remark why it is possible to base our analysis on the models developed for BJT oxide: BJT parasitic dielectrics have a high density of defects, are thick and are crossed by small electric fields. The same characteristics are encountered also in the spacers, which therefore could be affected by the same phenomena.

The processes that take place in the space charge model can be listed as follows:

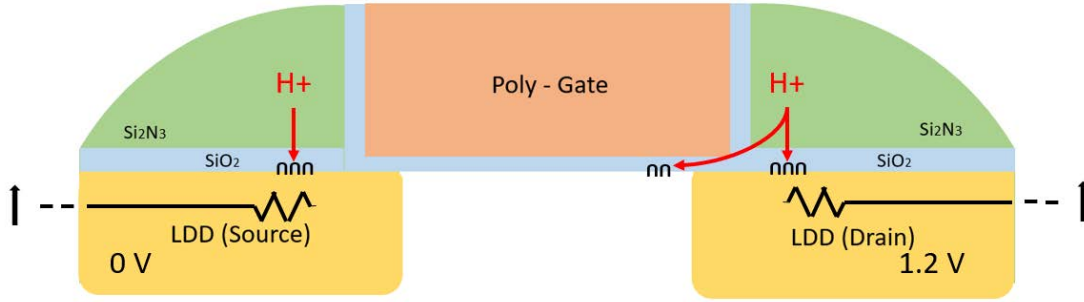


**Figure 5.22:** Proposed model for the High-DR experiments

- Trapping of holes closer to the interface where they are more easily compensated or annealed [43]
- Free electrons/trapped holes recombination which forms stable neutral dipoles and reduce  $N_{ot}$  [44]
- Reversing the electric field locally inside the oxide, so that holes near the gate drift to the gate rather than the Si [46]
- Holes forming an electrostatic barrier (due to local field reversal) to cause a fraction of hydrogen ions to drift toward the gate rather than the silicon bulk [46, 50]

The presence or the absence of a positive space charge inside spacer oxides plays a key role in our model. Figure 5.22 reports a possible representation for the holes movement and the interface traps depassivation for a high dose-rate experiment. This model is derived from what was proposed by Faccio in [63], where devices were exposed at similar high DRs. The above mentioned positive space charge is represented in Figure 5.22 with a series of letter “h” and it is supposed to be uniformly distributed inside the oxide<sup>3</sup> [46]. These charges can locally reverse the electric field and inhibit the depassivation of the traps collocated at the interface between the spacer silicon dioxide and the underlying n-well. In addition, the holes trapped in centers collocated close to the interface can recombine with electrons coming from the heavily doped silicon of the drain and source regions, reducing  $N_{ot}$ . The curved part of the red arrow, which points from the spacers to the gate oxide/bulk interface, indicates the path followed by a fraction of the  $H^+$  ions located in the spacers [63]. As detailed in 5.3.4, when a drain-to-source voltage is applied, the transport of  $H^+$  is promoted on the drain side and discouraged on the source side. In this case, since the depassivation of these interface traps occurs only on the drain side, the device become asymmetric [63, 76]. From the other hand, the straight part of the arrow represents the drift of a fraction of  $H^+$  that depassivates the spacer/silicon interface traps, which are indicated with the  $\cap$  symbol. The fraction of  $H^+$  who reaches the spacer/drain and spacer/source interfaces affects the carrier distributions under the spacers, provoking an increase in the series resistance  $R_{SD}$ , as reported in [63] and detailed in [76]. Since the charges trapped in the spacers

<sup>3</sup>Note that the charges may be not confined just inside the  $SiO_2$  oxide region of the spacers, but may be also present even in the  $Si_2N_3$  region.



**Figure 5.23:** Proposed model for the Low-DR experiments

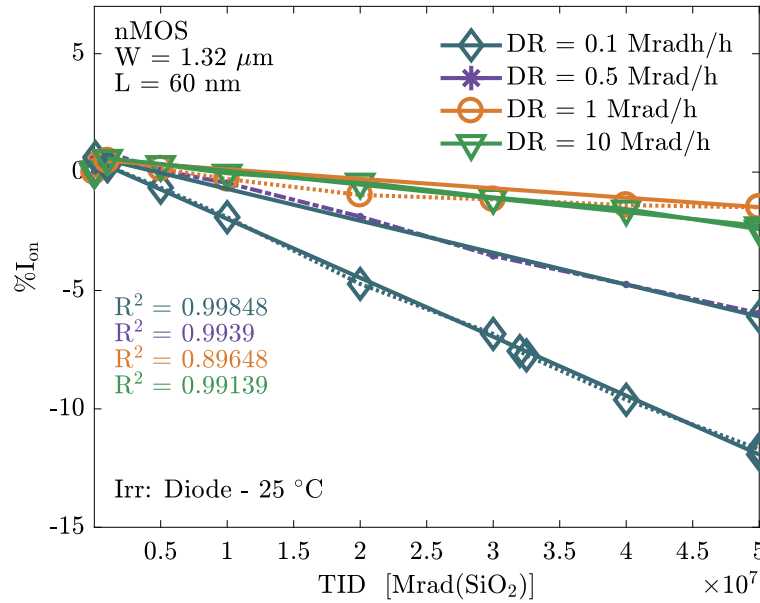
are positively signed, they do not produce rises in the series resistance for nMOS devices.

At low dose-rate, the space charge inside the spacer oxides is not formed, therefore  $H^+$  movement is not obstructed by its presence (see Figure 5.23). The drift of the hydrogen ions leads to an incremented rate of depassivation of both interface traps collocated between the spacer oxide and the drain and source n-wells and traps located at the gate/channel interface. The first mechanism could entail rises in the  $R_{SD}$ , while the second mechanisms increases the threshold voltage shift and the asymmetry. In addition, even if more holes are trapped in deep trap centers and their presence may obstacles to the rise of the drain-to-source resistance [76], the depassivation of interface traps located above the drain region dominates the over-all response.

Therefore, in the model we propose, high dose-rates reduce the three mechanisms taking place at lower dose-rates:

- Depassivation of interface traps located between the gate oxide and the silicon, that leads to asymmetrical changes in the device and mostly produces changes in the threshold voltage
- Depassivation of interface traps collocated between the spacer oxide and the LDD part of drain and source terminals, that entails rises in the  $R_{SD}$
- Domination of interface traps over oxide traps in the over-all radiation response, reflected as rises in the  $R_{SD}$

Figure 5.18 can help to strengthen the comments proposed so far. The filling of gate/silicon interface traps produces a strong asymmetry in the device [63, 76] as previously reported in Section 5.3.4. High dose-rates limit the depassivation of the interface traps collocated at gate/silicon interface, therefore less differences between the threshold voltage calculated in standard and reverse configurations as the dose-rate increases are expected. High dose-rates reduce also the filling of spacer/silicon interface traps. These filled trap centers entail rises in the  $R_{SD}$  [63, 76], as can be seen in Figure 5.14, where lower DRs provoke a larger degradation in the peak of the transconductance. From Figure 5.17 we can notice that the difference in the degradation of the output current between standard and reverse configuration are reduced by low dose-rate. This means that rises in the  $R_{SD}$  are more important in the overall response, than both gate/silicon interface traps depassivation (which causes the asymmetric charge build-up) and charge trapping in the spacer oxides.

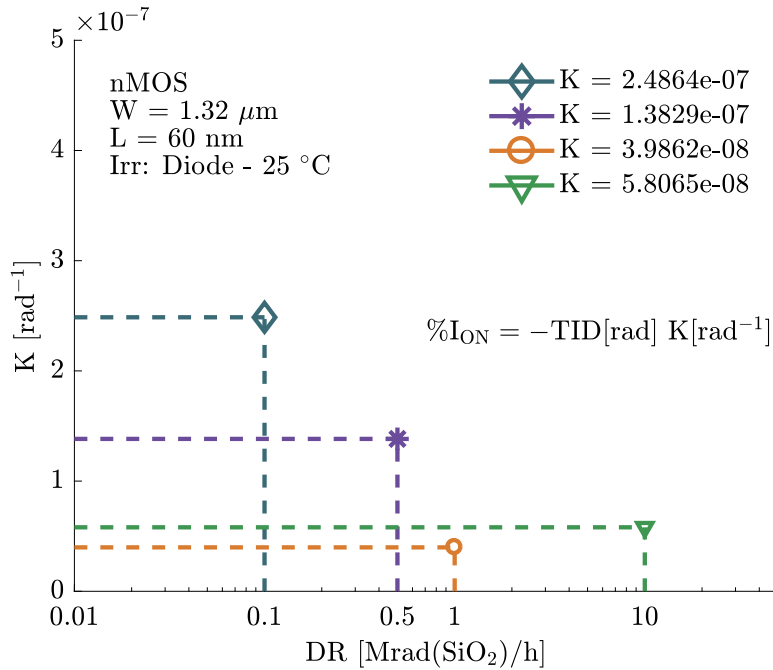


**Figure 5.24:** Fitting of the drive current variation curves.

In fact, even if for low dose-rates the difference between the standard and reverse threshold voltage are spread compared to the high DR experiment, the source-to-drain resistance rises still impact more in the degradation of the device.

### 5.3.7 A dose-rate Sensitivity Coefficient

It may be worth to extrapolate a coefficient which can state the effective sensitivity of our devices to the DR. The aim of this coefficient, here called  $K$ , is to provide a qualitative idea on the damage that a low dose-rate experiment would have produced on a n-channel MOSFET which has been irradiated with a high DR. As it has been shown in Figure 5.2, the percentage degradation of the drive current evolves almost linearly with TID. The first idea to obtain a coefficient is to extract the slope of the percentage variation of the  $I_{ON}$  in function of the TID for different dose-rates. To do so, the data have been fitted with a linear function. In Figure 5.24 it is reported the fitting procedure, with the additional presence of the  $R^2$  parameter, in order to state the preciseness of the extraction method. Since the  $R^2$  coefficient are close to 1, the fitting proposed is a good representation of the experiments. The slope of the fitting line will be used as the mentioned DR sensitivity coefficient  $K$ . Figure 5.25 reports the value of  $K$  for different dose-rates, where higher values of the coefficient  $K$  correspond to a heavier impact of the DR. As can be seen from the figure,  $K$  has a similar value at 1 and 10 Mrad(SiO<sub>2</sub>)/h, meaning that the high dose-rate-reduced degradation has reached a sort of saturation. For  $DR < 1$  Mrad(SiO<sub>2</sub>)/h,  $K$  increases rapidly, almost of a factor 6 at 0.1 Mrad(SiO<sub>2</sub>)/h the value reached at high-DRs. It is clear that we cannot extract any information on what happens at even lower dose-rates. The enhanced degradation could saturate just below 0.1 Mrad(SiO<sub>2</sub>)/h or could increase further. This is of course worrisome for CERN applications, where the actual dose-rate can be substantially lower than 0.1 Mrad(SiO<sub>2</sub>)/h. However, the reduction of the ELDRS at low temperature and for other biases than the diode

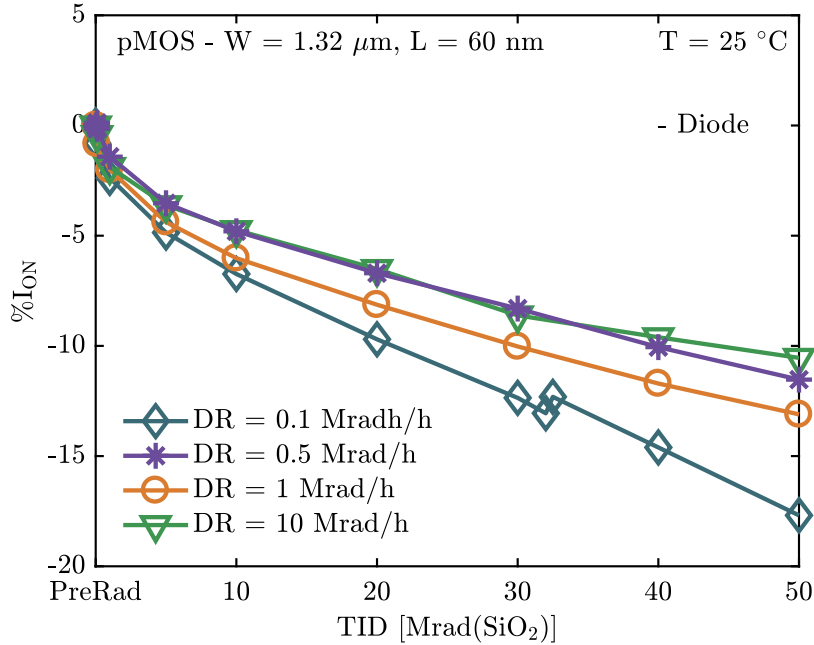


**Figure 5.25:** K coefficient for the different DRs analyzed.

goes in the direction of a smaller impact of the DR in the real application. The question of whether this consideration is sufficient to overlook the effect of DR in the design of devices for the HL-LHC is certainly a very complicated one, and more experiments at lower dose-rates are needed. Moreover, the experiments conducted reached a TID of 50Mrad(SiO<sub>2</sub>), and it is not possible to predict the degradation of the n-channel devices at higher levels of TID. It may be that the degradation changes slope for higher level and, in that case, the K coefficient would not be able anymore to predict the changes.

## 5.4 Results for the p-Channel MOSFETs

The DR dependence manifests itself also in p-channel devices, similarly to the n-MOS structure. For this reason, the results will be briefly shown just for the transistor irradiated in diode configuration with  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$ . As for the n-MOSFET devices, the analysis of the p-channel structure begins with considerations on the drive current evolution. In Figure 5.26, the percentage variations of the  $I_{\text{ON}}$  in function of the TID is reported. Compared to the nMOS structures, during the whole irradiation process the drive current degradation of the pMOS devices is higher, as already reported for example in [33]. As an example, at 50 Mrad(SiO<sub>2</sub>), pMOS transistors degrade their output current from -10% down to -17.5%. However, the DR effect is reduced in p channel devices, since the difference in the damages between low and high dose-rate experiments is smaller. The enhanced degradation of pMOS transistors is a well known phenomenon, commonly found in recent technology nodes [33], and it is caused by the equality of charge sign for oxide and interface traps. Since both trap centers are positively signed, they work together to repel the positive carriers, which form the channel, resulting in a elevated TID sensitivity. As already stated in Section 5.1, the DR effect is less evident in pMOS

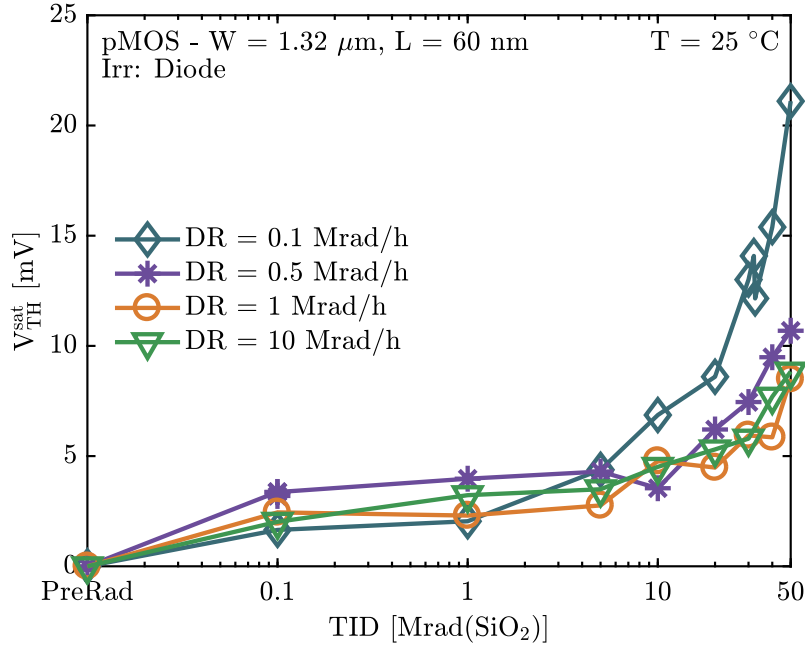


**Figure 5.26:**  $I_{ON}$  percentage variations in function of TID for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  pMOS transistor, irradiated with different DRs up to  $50 \text{ Mrad}(\text{SiO}_2)$ . The devices are biased in diode configuration. A lower DR provokes a higher degradation for these type of structure, as previously encountered also in the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  nMOS (5.2c)

transistors. In Figure 5.26, the Low-DR experiment produces a degradation in the drive current which is 1.75 times higher than the one caused by the High-DR experiment. For nMOS structure, this ratio of the same figure of merit is almost 6. More in detail, we can see that at low dose-rate the damage of pMOS is comparable with the damage of nMOS (17.5 % vs 12.5 %). On the other hand, at high dose-rate, the degradation of pMOS is around 10 %, while in nMOS it is around 2 %. That is, the difference between the degradation of nMOS and pMOS is greater at high dose-rate. Consequently it is possible to think of differences on how the high dose-rate impacts between nMOS and pMOS. A solid demonstration of these differences has not yet been found. We assume that the cause may be the difference in electric fields between nMOS and pMOS. In fact, in pMOS the direction of the electric field goes from source to gate/drain. However, this hypothesis needs further studies to be confirmed.

It is possible to observe, from Figure 5.26, that the slope of the drive current percentage degradation changes in function of the TID reached. For TID levels lower than  $10 \text{ Mrad}(\text{SiO}_2)$  the slope is definitely not constant, while it tends to be constant as the ionizing dose rises above  $10 \text{ Mrad}(\text{SiO}_2)$ .

In Figure 5.27 the  $V_{TH}^{\text{sat}}$  evolution in function of the TID for the large and short device is reported. As for the n-channel structure, the differences between the pre- and post-irradiation values are bounded in a small interval, and are probably harmless for most of the applications. In particular, the worst deviation from the pre-irradiation value occurs in the Low-DR experiment, as expected from [13]. The difference from the pre-irradiation value is around 20 mV. The presence of Only  $V_{DS}$  or Only  $V_{GS}$  biases influence the overall response, reducing the DR effect, as



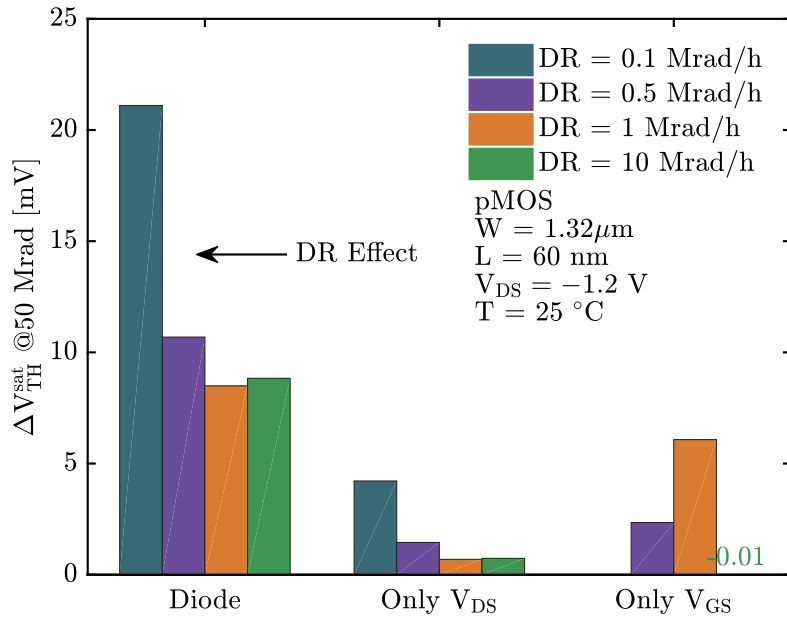
**Figure 5.27:** Threshold voltage variations for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  p-MOSFET.

it is possible to notice from Figure 5.28.

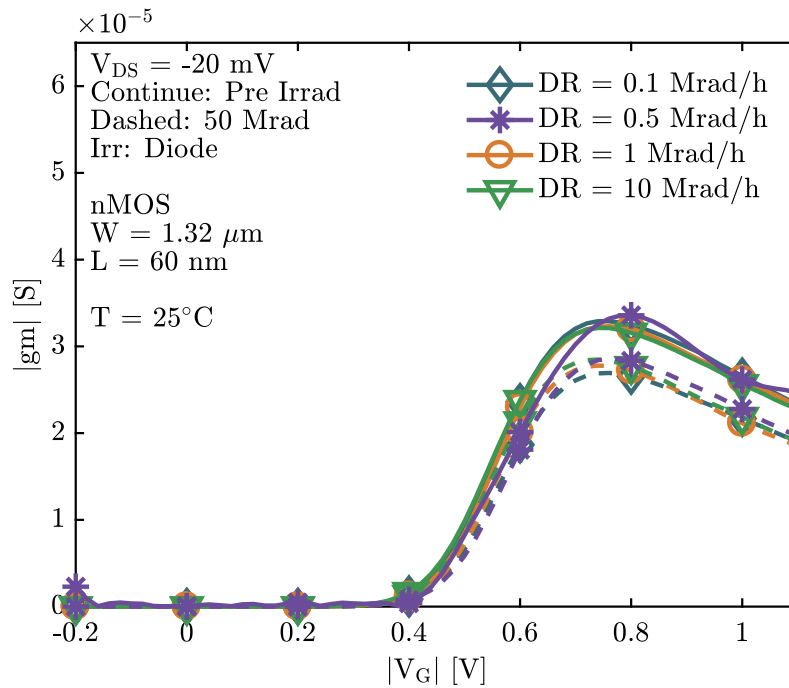
The pre- and post-irradiation curves for the transconductance of the large and short devices are reported in Figure 5.29. The major contribution to the degradation of the transconductance comes from a vertical decrease, which is related to a rise in the series resistance between source and drain [63, 76]. For the sake of completeness, it is possible to notice that for higher voltages, the pre- and post-irradiation curves does not converge to the same  $g_m$  value, as was instead noticed for nMOS structure. Therefore is possible to exclude degradation in the mobility for these devices [63]. The degradation of  $g_{m\text{MAX}}$  can reach almost -20% at the end of irradiation, as reported in Figure 5.30. However, also higher DRs, as  $1 \text{ Mrad}(\text{SiO}_2)/\text{h}$  and  $10 \text{ Mrad}(\text{SiO}_2)/\text{h}$ , produce a not negligible reduction.

Also for the pMOS structures, the sub-threshold swing is not influenced by the dose-rate, and remains almost constant during the irradiation processes, as Figure 5.31 shows.

Similarly to nMOS, lower temperatures reduce the output current degradation. In Figure 5.32 is reported the dependence on the temperature for the above mentioned device. The difference in the degradation percentage between low and high DR experiments is reduced as the temperature decreases, as previously observed for the nMOS structures.

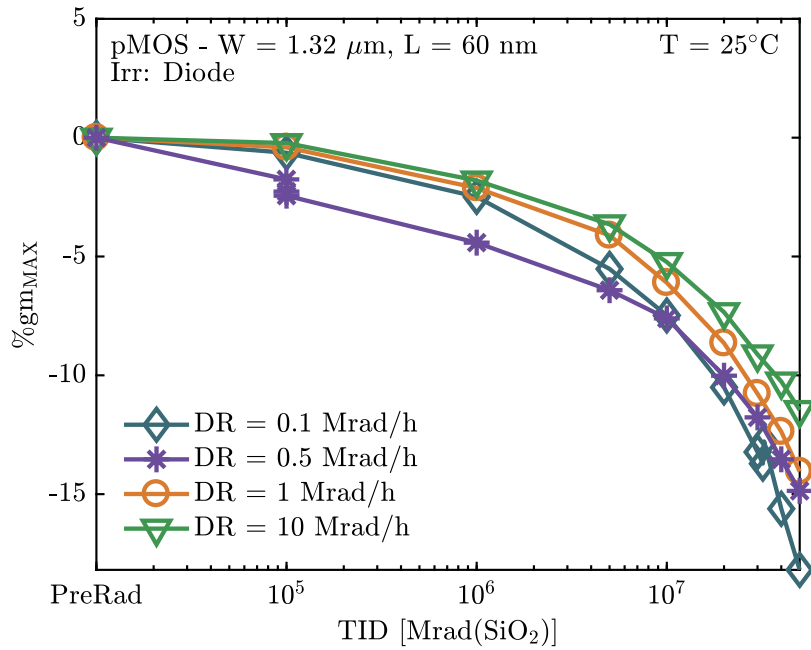


**Figure 5.28:** Threshold voltage shifts after 50 Mrad( $\text{SiO}_2$ ) for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  p-MOSFET

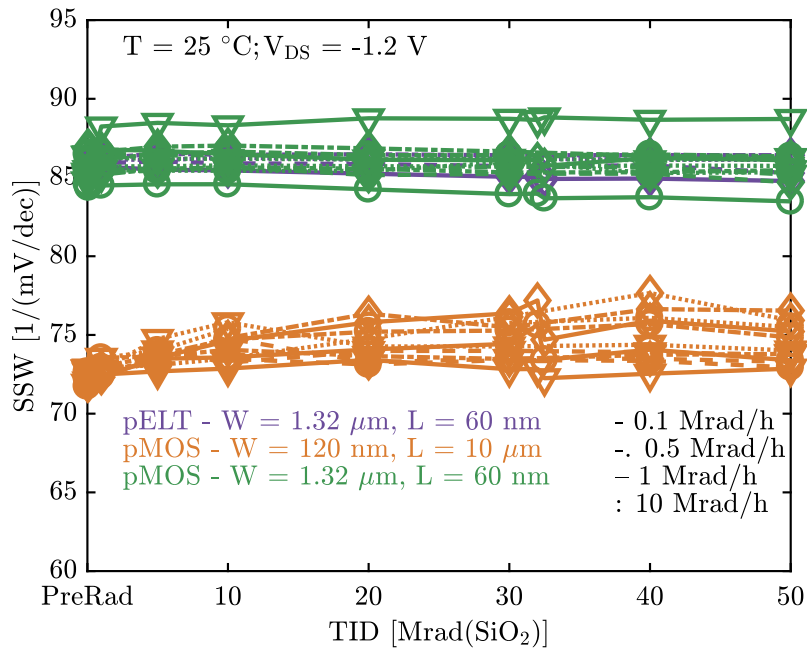


**Figure 5.29:** Pre- and post-irradiation transconductance curves for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  p-MOSFET

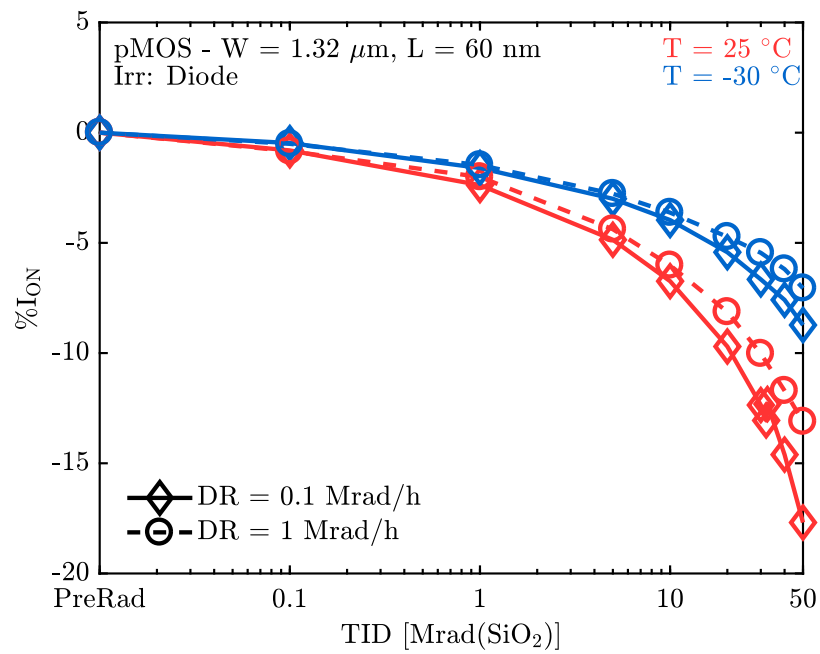




**Figure 5.30:** Evolution of the peak of the transconductance for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  p-MOSFET



**Figure 5.31:** Evolution of the Sub-Threshold Swing for the  $W = 1.32 \mu\text{m}$  and  $L = 60 \text{ nm}$  p-MOSFET



**Figure 5.32:** Temperature effect on the drive current for the W = 1.32  $\mu\text{m}$  and L = 60 nm p-MOSFET

## 5.5 Conclusions on the dose-rate effect

We irradiated up to 50 Mrad(SiO<sub>2</sub>) and at different dose-rates devices belonging to the 65 nm technology node. We noticed that the combination of a low DR and the diode connection applied during irradiation produces remarkably higher degradation in short channel devices ( $L = 60$  nm), while long channel devices (which damages is more caused by charge trapped in the STI [33]) are not sensitive to changes in the DR, independently from the bias applied. The ELT devices underwent a radiation-induced evolution very similar to the short channel MOSFETs. The presence of a ELT structure gave us additional confirmations on the nature of the DR effect, since these structure are immune by design from charge trapping in the STI. We came to the first conclusion that the DR effect is caused by complex phenomena taking place in the spacer oxides, while charge trapping in the STI is not sensitive to changes in the DR.

It is already known since 1994 that BJT are sensitive to low dose-rates . This dependence is called ELDRS and has been reported in a vast number of studies, such as [43, 44, 50] and summarized in [42]. The models, developed in order to explain the ELDRS in BJT oxides can be applied to our MOSFETs, since the previously mentioned similarities between the parasitic BJT oxides and the spacers. In particular, following the idea initially presented in [43] and then further developed, the space charge accumulation is the result of a delayed transport of holes at the Si/SiO<sub>2</sub> interface.  $E'_{\delta}$  centers act as traps for holes, and if the flux of radiation-induced charges is high, the filled centers are constantly filled by holes. This space charge produces local rises the electric potential. The wall of potential can encourage the drift of holes and hydrogen ions toward the gate electrode, as reported in Figure 2.9, instead of the classical bulk drift. In addition, as reported in [44], the positive net charge trapped at high dose-rates in the oxide,  $N_{ot}$ , decreases due to radiation-generated electron/trapped holes recombination mechanisms (consequent creation of stable dipoles). From [50] it has been demonstrated that the space charge creates a wall of potential that partially prevents the depassivation of traps at the gate/silicon, spacers/drain and spacer/source interfaces, inhibiting the effective density of active interface traps,  $N_{it}$ .

From the analysis of the radiation-induced evolution of the main parameters, such as  $I_{ON}$ ,  $V_{TH}$ , gm and  $S_{SW}$  we understood that the DR sensitivity was caused by a set of complex phenomena taking place in the spacer oxides. We attributed the main responsibility for the low DR enhanced drops in the output current to the changes in the transconductance. It is difficult to fully interpret the evolution of this parameter. In fact, in addition to a vertical decrease (observed also in [63, 76] and traced in rises of the  $R_{SD}$ ) the values of gm tend to converge to the pre-irradiation conditions at high electric fields, independently from the DR. This behaviour may suggest a possible mobility limitation, already present before irradiation. For the sake of completeness, the evolution of the threshold voltage takes place in a very well confined interval, equal or smaller than the uncertainty unavoidably presents in device production processes. The sub-threshold swing, which is the last figure of merit here analyzed, is constant in good approximation during all the irradiation process, therefore is not surely a concern for our applications. We focused also on the reverse configuration, extensively analyzed in Subsection 5.3.4. In fact, we understood that lowdose-rates enhance the positive  $\Delta DIBL$  (21.2 mV/V at 0.1Mrad(SiO<sub>2</sub>)/h vs 7.4

mV/V at 10Mrad(SiO<sub>2</sub>)/h) evolution for the standard device and the negative one (-13.9 mV/V at 0.1 Mrad(SiO<sub>2</sub>)/h vs -2.3 mV/V at 10 Mrad(SiO<sub>2</sub>)/h) for the inverse structure. We performed one high DR and one low DR experiment both at room temperature and at -30 °C, and observed that lower temperatures produce less severe degradation, but, more in detail, the difference in the drive current reduction between High- and Low-DR experiment is reduced. It is possible to state the DR effect is partially contained by low temperature, which is extremely helpful for most of CERN applications [77].

In addition, we proposed a model for the DR sensitivity, which can be seen as an extension of the one previously developed for the generic charge accumulation in the spacer oxides and at the relative Si/SiO<sub>2</sub> interfaces, developed in [63]. At high dose-rates the wall of charge (introduced in [43]) limits the depassivation of the traps located along the gate/bulk interface and the spacer/drain or spacer/source interfaces, limiting the threshold voltage shift caused by the first ones and the asymmetric charge built up and the rises in the R<sub>SD</sub> caused by the second and third ones. At low DR these phenomena are not limited, therefore we saw a more evident threshold voltage shift, an asymmetric charge build up and a promoted rise in the source-to-drain-resistance.

The analysis on the dependence of the DR is not completed, future studies should cover lower dose-rates both at room temperature and at -30 °C. It still has to be understood if for extremely low dose-rates, inferior to the 0.05 Mrad(SiO<sub>2</sub>)/h here reported, the charge depassivation rate at the interface saturates, creating an upper limit to the DR sensitivity coefficient, introduced in Section 5.3.7. In addition, TCAD simulations will help to resolve the present doubts on the possible degradation of the mobility in the channel and to confirm the effective presence of rises in the series resistance.

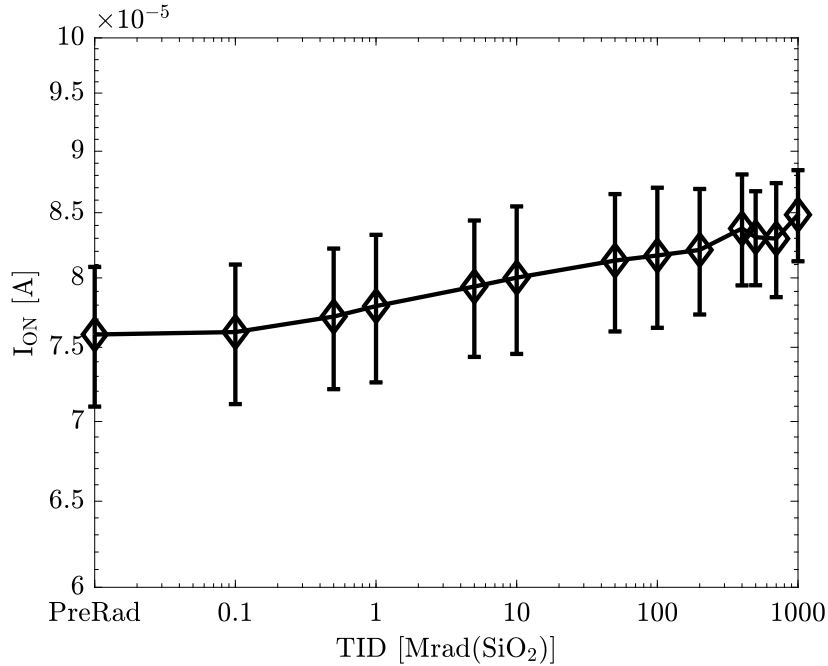
# Chapter 6

## Next Technology Step for CERN Applications: 28 nm

Circuitry in the new detectors for the HL-LHC is mostly designed in 130 and 65 nm technology nodes, but the transition to the 28 nm technology node could be an attractive solution for possible future applications. However, while an acceptable knowledge on the ionizing radiation-induced effects has been achieved for the 130 and 65 nm technology nodes, in newer and smaller technologies, like the 28 nm node, the investigation of the radiation response at ultra-high doses begun just recently. The scaling down requires different fabrication processes, resulting in a different radiation response. As it will be explained in this chapter, the 28 nm technology shows a reduced radiation-induced degradation in the output current compared to 130 and 65 nm. As a notable drawback, a dramatic increase in the leakage current is present. Three different types of threshold voltage flavour devices are considered, and some comments on how different concentration of doping may influence the overall radiation response are derived. In addition, a comparison between two different manufacturers will show an example of the already mentioned process-dependency on radiation-induced degradation.

Before starting to analyze the radiation response of the 28 nm technology node it is important to observe one main difference in the gate oxide, compared to older nodes. As the thickness of the insulator decreases, tunnelling of carriers through dielectric is facilitated. Therefore, in order to reduce this unwanted behaviour, the gate oxide in 28 nm CMOS technology is composed by a relatively thick layer of  $\text{HfO}_2$ , deposited over a very thin layer of  $\text{Si}/\text{SiO}_2$ . These types of gate are called High- $\kappa$  structures. Several gate oxide deposition techniques have been proposed [86]. The most used ones are Physical Vapor Deposition (PVD), Deposition by Electron Beam Evaporation and Atomic Layer Deposition (ALD) – which is the preferred one – since it gives the possibility to grow the thinnest films of any other method [86]. The thin layer of  $\text{Si}/\text{SiO}_2$  is inserted in order to reduce the presence of traps at the interface between the gate oxide and the silicon channel, improving the overall quality of the silicon-oxide interface [86]. Since the density of traps in the  $\text{HfO}_2$  layer and at its interface between the underlying  $\text{Si}/\text{SiO}_2$  could be higher than the one expected in a gate-oxide entirely made in  $\text{Si}/\text{SiO}_2$ , the impact of the gate oxide in this technology should be carefully evaluated in future studies.

In addition to the main experiment, which will be discussed in the following sections, we conducted analysis on the 28-nm technology node variability. In partic-

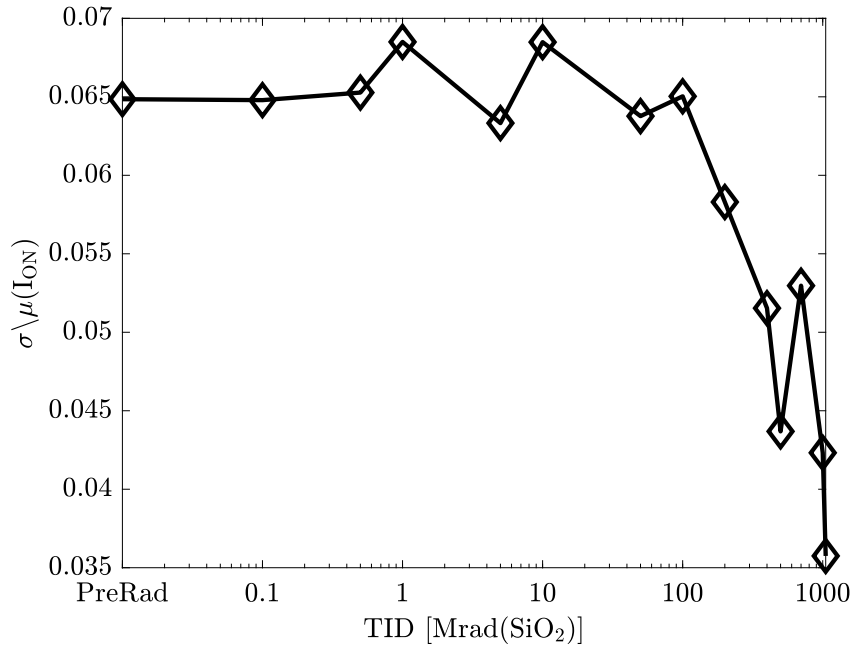


**Figure 6.1:** Ion variations for nMOS with  $W = 80$  nm and  $L = 30$  nm, irradiated up to 1 Grad. Sigma variation bars are considered

ular, we analysed the device-to-device variability of ten 80 nm x 30 nm nMOS and pMOS. In Figure 6.1 the evolution of the drive current in function of TID for the just mentioned device are reported. As we will see, variations of the drive current are not a big concern for the technology node, hence even if the TID level is outstanding, the evolution of the drive current is quite bounded in a narrow interval. Already in the pre-irradiation condition the drive current values spread in a wide interval. The values of  $\sigma$  are linked to the average of the drive current, hence one crucial parameter, used to understand if the standard deviation effectively increases due to irradiation is the ratio  $\sigma/I_{ON}$ , which provide an a-dimensional coefficient. This coefficient is reported in Figure 6.2. As we can see, opposite to the 65 nm technology node, previously analysed in [11], the TID does not enhance the variation in the drive current, but slightly narrows the interval in which the values are spread. A similar behavior is observed also in the leakage current changes. We will see that the evolution of the leakage current is the main concern for this technology node, but at least the irradiation does not enhance the differences.

## 6.1 Experiment Details

The devices have been irradiated up to 400 Mrad(SiO<sub>2</sub>), with a DR of 5.5 Mrad/h. The irradiation has been performed at room temperature ( $T = 25$  °C) and the transistors were biased in diode configuration ( $V_{GS} = V_{DS} = 0.9$  V). In order to characterize the evolution of devices as a function of the TID, the  $I_D$  vs  $V_{GS}$  curves and the some of the most relevant parameters of the MOS structure are presented. There will be, in Section 6.5, a brief comparison with another 28 nm CMOS technology. For this reason, the manufacturer of the chip irradiated in this experiment will be referred as "Manufacturer A". Figure 6.3 shows the layout of the test chip. Thanks



**Figure 6.2:**  $\sigma$  over mean ratio, for the drive current, in function of TID

Man. B vs Man. A	
VDD	VSS
pSOURCE	nSOURCE
gateP 1	gateN 1
gateP 2	gateN 2
pMOS 100nx30n	nMOS 100nx30n
pMOS 3ux30n	nMOS 3ux30n
pMOS 100nx1u	nMOS 100nx1u
<b>pMOS LVth 100nx30n</b>	<b>nMOS LVth 100nx30n</b>
<b>pMOS LVth 3ux30n</b>	<b>nMOS LVth 3ux30n</b>
<b>pMOS LVth 100nx1u</b>	<b>nMOS LVth 100nx1u</b>
<i>pMOS HVth 100nx30n</i>	<i>nMOS HVth 100nx30n</i>
<i>pMOS HVth 3ux30n</i>	<i>nMOS HVth 3ux30n</i>
<i>pMOS HVth 100nx1u</i>	<i>nMOS HVth 100nx1u</i>

**Figure 6.3:** Array of the chip analysed in the 28 nm technology node studies. Note the presence of different  $V_{TH}$  flavours.

to the presence of Low- $V_{TH}$  and High- $V_{TH}$  devices, it is possible to draw conclusions on the influence of doping, as the threshold voltages are usually modified by changing doping profiles. Moreover, the channel dimensions have also been chosen in order to separate the effects caused by the presence of STI oxides - that have a strong impact on MOSFETs with narrow channels - and those caused from spacer insulators - that have a strong repercussion on MOSFETs with short channels, at least in the 65 nm channel length node. It will be shown that, as regards the 28 nm technology node, the effect produced from charge trapping in the spacers is not as problematic as for the 65 nm channel length node.

## 6.2 Results: nMOS

The pre- and post-irradiation  $I_D$  vs  $V_{GS}$  characteristics are shown in Figure 6.4. The analysis has been divided into groups, each of which has a different W/L ratio.

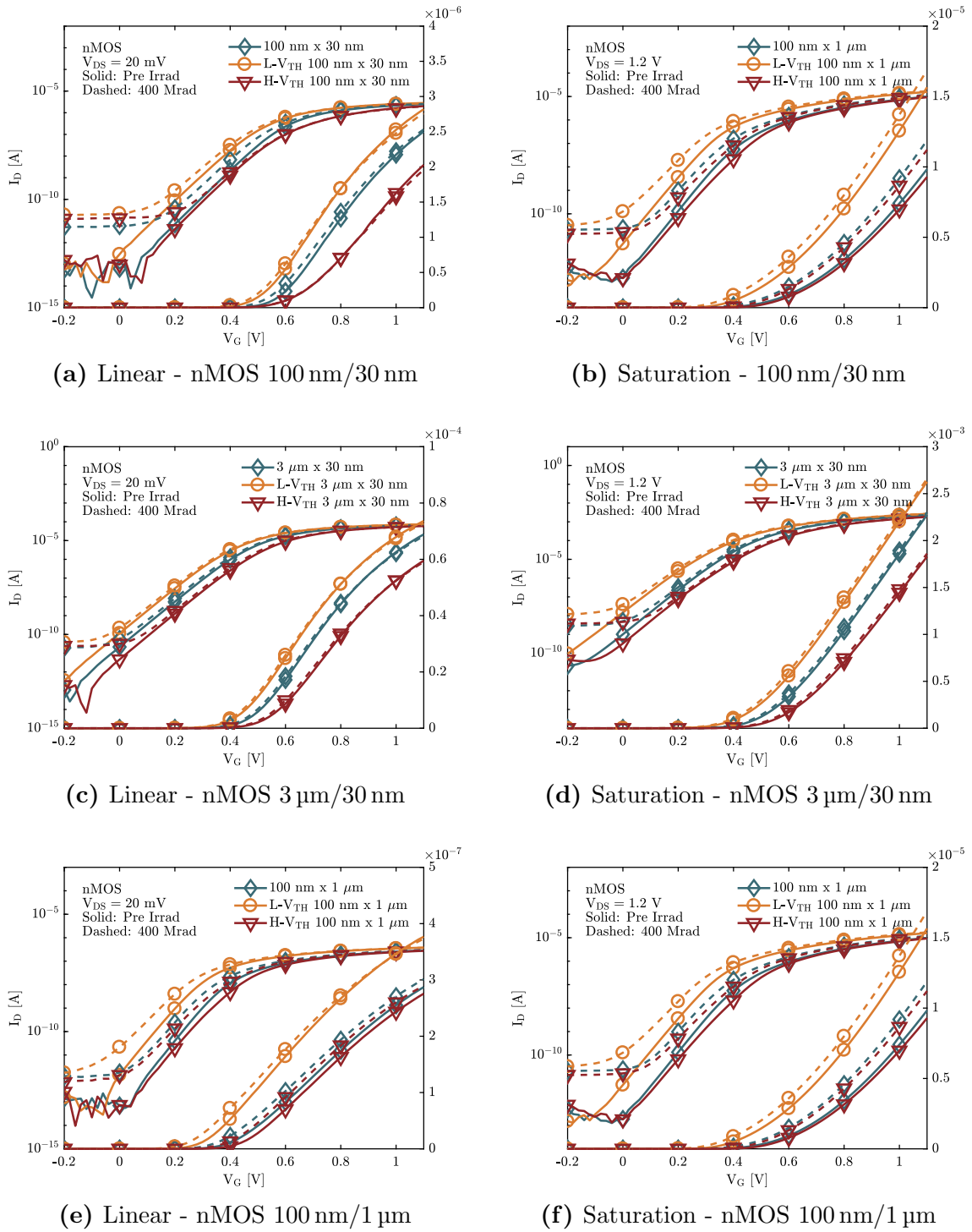
- Group 1 - W/L=100 nm/30 nm
- Group 2 - W/L=3  $\mu$ m/30 nm
- Group 3 - W/L=100 nm/1  $\mu$ m

The left column reports the curves measured in linear region ( $V_{DS} = 10$  mV) while the right column shows the results obtained in saturation region ( $V_{DS} = 0.9$  V). As mentioned in the at the begin of this chapter, the drive current degradation is bounded in a narrow interval, even if the TID reached is surely important.

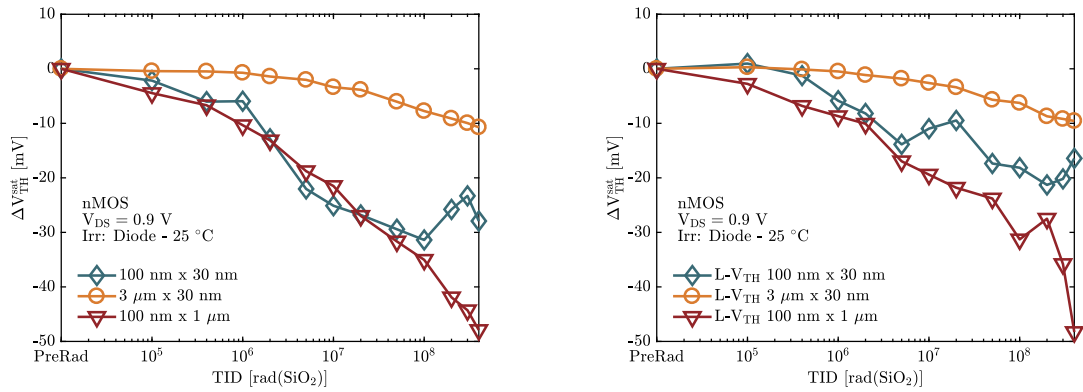
### 6.2.1 Threshold Voltage

In the 28 nm technology node, the variation of  $V_{TH}$  is most mainly caused by the presence of radiation-induced charges trapped in auxiliary oxides, such as STI and spacers, and at the interface between these oxides and the silicon. However, as stated in the brief analysis on the gate oxide composition made in the introduction, a presence of charges in the gate cannot be excluded. The oxide-trapped charge is positive, tending to decrease  $V_{TH}$ , while the interface traps are either empty or negatively charged, depending on the bias imposed at the gate [36]. Consequently, interface traps can produce an increase in the threshold voltage. As the charge trapping is less time-requiring for the oxide trap centers than for those located at the Si/SiO<sub>2</sub> interface, there will initially be a net decrease in threshold voltage [87]. Then, the impact of the charge trapped at interface becomes more relevant, compensating the effect of the oxide-trapped charge, and eventually increase the threshold voltage. Figures 6.5a (Standard- $V_{TH}$  devices), 6.5b (Low- $V_{TH}$  devices) and 6.5c (High- $V_{TH}$  devices) show the variation of the threshold voltage versus TID for the measured devices. It is interesting to note that, for all the devices, the threshold voltage shift is relatively small, less than 60 mV. Similar to what observed in other technologies, the behavior of the curves strongly depends on the size of the device [69, 83, 88, 89]. For devices having W=3  $\mu$ m and L = 30 nm or W = 100 nm and L = 1  $\mu$ m, oxide traps are dominant throughout the whole process. This results in a monotonic decrease in threshold voltage. On the other hand, for transistors with W = 100 nm and L = 30 nm, the negative charge trapped in the interface traps start, at a certain

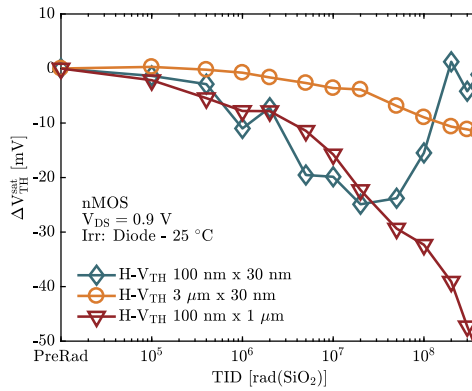




**Figure 6.4:**  $I_D$  vs  $V_G$  curves for all nMOS devices, irradiated up to 400 Mrad in diode configuration. In the left column the curves for linear zone are presented, while the right contains the curves for the saturation zone. The MOS are divided in group in function of their W and L dimensions.



(a) Threshold voltage evolution in function of TID for the standard  $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V. (b) Threshold voltage evolution in function of TID for the Low- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.



(c) Threshold voltage evolution in function of TID for the High- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

**Figure 6.5:** Evolution of the threshold voltages for the whole set of devices analysed for the 28 nm technology node.

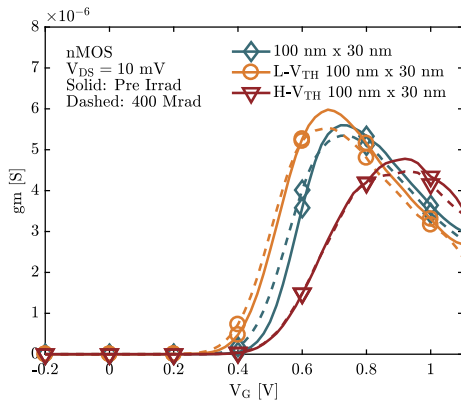
TID, to compensate and then prevail over the positive charge trapped in the oxide traps, thus balancing the negative threshold voltage shift. It is worth to observe that narrow and long devices show the maximum degradation in the drive current, compare to the pre-irradiation value, as already seen for 28 nm technology produced by Manufacturer B [88].

### 6.2.2 Transconductance

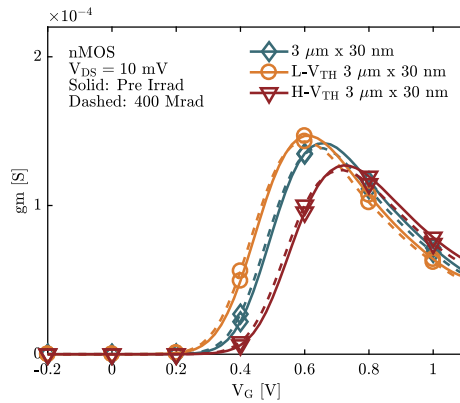
Figures 6.6a, 6.6b and 6.6c show the effects of the TID on the  $gm(V_{GS})$  characteristics, respectively for devices having  $W = 100$  nm and  $L = 30$  nm,  $W=3$   $\mu$ m and  $L = 30$  nm,  $W = 100$  nm and  $L = 1$   $\mu$ m. The degradation of the transconductance can be related to an increase in the series resistance  $R_{SD}$  or is possibly correlated to changes in the mobility of the carriers [63]. Even if the TID reached is certainly important, there are, compared to previous technology nodes – e.g. 65 nm, no significant shifts in the curves. In Figures 6.7a the percentage variation of the peak of  $gm$  ( $gm_{MAX}$ ) in function of the TID is presented. The peak of  $gm$  has a maximum degradation of -6 %, which is a very moderate variation, if compared to the 65 nm (Section 5.3.2 of this thesis) and 130-nm technological, reported in [33].

### 6.2.3 Drive Current

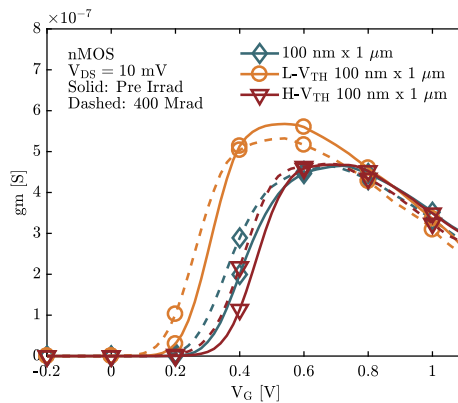
Figure 6.8 shows the radiation response of the  $I_{ON}$ , i.e. the drain current measured at  $V_{GS} = V_{DS} = 0.9$  V, for transistors of different sizes and different flavours of threshold voltage, exposed to a TID of 400Mrad( $SiO_2$ ). In nMOS transistors, oxide traps (positively charged) tend to increase the drive current, thanks to a negative variation in the threshold voltage, while interface traps (negatively charged) tend to decrease it, for the opposite reason. In the studied samples, the effect of interface traps starts to be relevant only at very high doses (TID > 10 Mrad( $SiO_2$ )) and for Standard- and High- $V_{TH}$  narrow/long devices the  $I_{ON}$  monotonically increases until the end of the exposure, up to +20 % at the end of irradiation. Similar results were found in [69] for the 28 nm technology produced by Manufacturer B. The wide current variation in narrow/long transistors shows that STI oxides play a key role in the radiation response of these devices. The charges trapped in these oxides tend to reduce the threshold voltage, as already reported in [69, 83, 88, 89] for devices produced by Manufacturer B, and as can be seen from the Sub-figures contained in Figure 6.5. The monotonic growth of the drive current of some of these transistors may indicate that the interface charges contribute negligibly to the trend of the  $I_{ON}(TID)$ . Since the actual impact of the charge trapped at the interface between the STI and the channel depends on doping concentration in the channel itself, the lower variation measured in the  $W = 100$  nm and  $L = 1$   $\mu$ m Low- $V_{TH}$  transistor can be explained by a variation in the doping levels, modified in order to control the threshold voltage. The relevance of the doping level in the channel may also explain the lower variation of  $I_{ON}$  in the minimum size transistors compared to the narrow/long ones. In fact, as explained in [89] for 28 nm transistors produced by Man. B, the reduction in channel length causes a variation in channel doping due to the overlap of regions, known as Halo.



(a) Transconductance evolution in function of TID for the  $W = 100 \text{ nm}$  and  $L = 30 \text{ nm}$  devices, calculated with  $V_{DS} = 10 \text{ mV}$ .

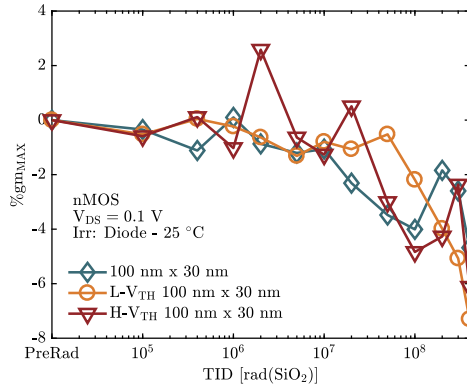


(b) Transconductance evolution in function of TID for the  $W = 3 \mu\text{m}$  and  $L = 30 \text{ nm}$  devices, calculated with  $V_{DS} = 1.2 \text{ V}$ .

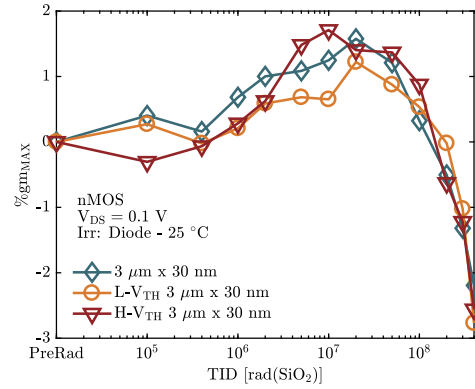


(c) Transconductance evolution in function of TID for the  $W = 100 \text{ nm}$  and  $L = 1 \mu\text{m}$  devices, calculated with  $V_{DS} = 1.2 \text{ V}$ .

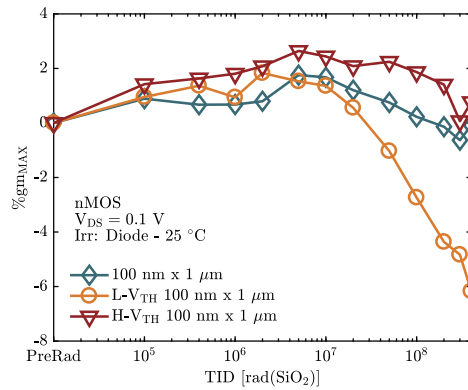
**Figure 6.6:** Comparison between pre- and post-irradiation transconductance curves for the devices analysed. The structure are divided into group in function of their channel length and width.



(a) Transconductance peak evolution in function of TID for the  $W = 100$  nm and  $L = 30$  nm devices, calculated with  $V_{DS} = 10$  mV.

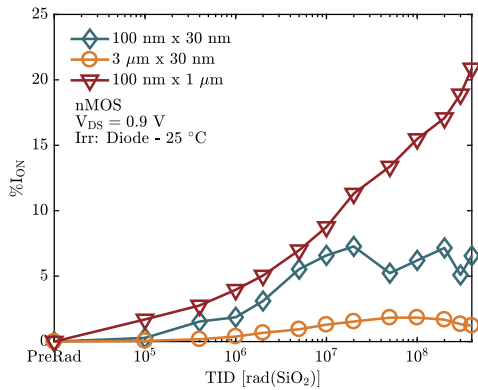


(b) Transconductance peak evolution in function of TID for the  $W=3\mu\text{m}$  and  $L = 30$  nm devices, calculated with  $V_{DS} = 10$  mV.

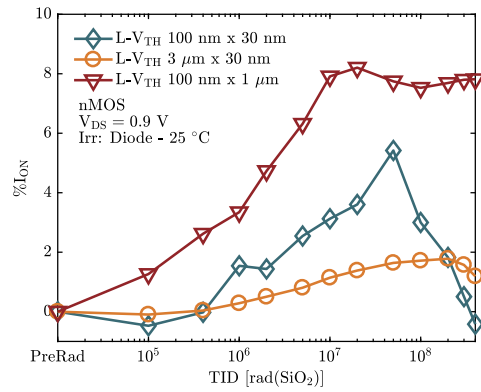


(c) Transconductance peak evolution in function of TID for the  $W = 100$  nm and  $L = 1\mu\text{m}$  devices, calculated with  $V_{DS} = 10$  mV.

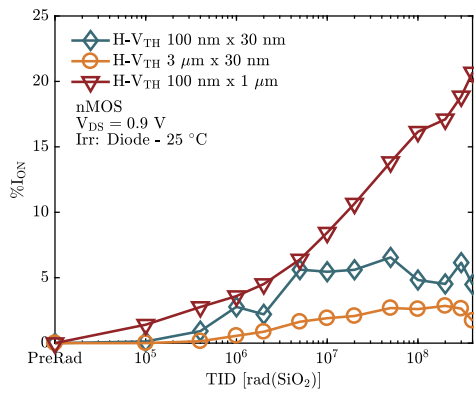
**Figure 6.7:** Evolution of the peak of the transconductance for the analysed devices. The structure are divided into group in function of their channel length and width.



(a) Drive current evolution in function of TID for the standard flavour devices.



(b) Drive current evolution in function of TID for the low threshold voltage devices.



(c) Drive current evolution in function of TID for the high threshold voltage devices.

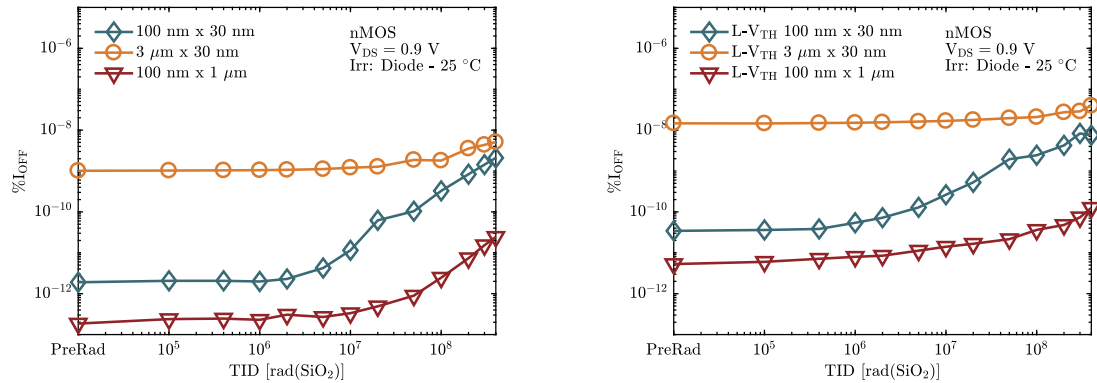
**Figure 6.8:** Drive current evolution in function of TID for the analysed devices. The structure are divided into group in function of their threshold voltage flavour.

### 6.2.4 Leakage Current

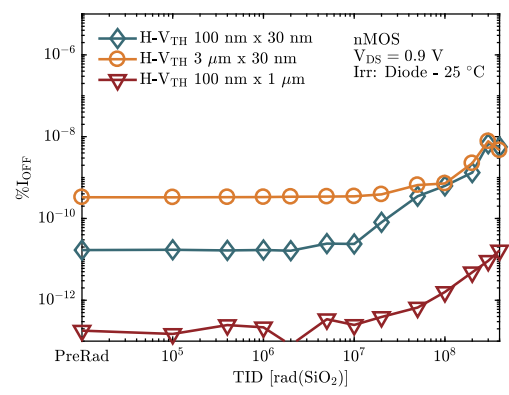
From previous experiments in 28 nm technology ([83] - [69] - [88] and [89]), it was observed that the leakage current ( $I_{\text{OFF}}$ ) is the parameter most affected in the 28 nm CMOS technology exposed to TID. The radiation-induced increase on the leakage current is almost independent from the  $V_{\text{DS}}$  imposed during irradiation, while the presence of an imposed  $V_{\text{GS}}$  during irradiation, strongly enhance the rise of the parameter, as previously reported in [70]. In addition, the presence of a positive gate voltage also rises the fractional yield, or the holes that escaped recombination processes. The influence of the gate voltage is mainly due to repulsive effect on the positive charge, which pushes the charge trapped in the STI in the depth of the same. The main cause of the increase encountered in the leakage current, is due to the creation of a parasitic MOSFET along the STI. The positive charge trapped in the insulator oxide can invert the parasitic lateral Drain-to-Source channels. As observed in [90], the charge is not trapped close to the gate, but in a deeper portion of the STI, where the gate voltage has no influence. In fact, the modulation of  $V_{\text{G}}$  does not implies changes in the measured leakage current. Figures 6.9a (Standard- $V_{\text{TH}}$  devices), 6.9b (Low- $V_{\text{TH}}$  devices) and 6.9c (High- $V_{\text{TH}}$  devices) show the evolution of the leakage Drain-to-Source current, measured at different levels of TID. It is possible to notice an increase in the  $I_{\text{OFF}}$  value, compared to the pre-irradiation conditions, by a factor strongly related to the channel length of the devices under test. Previous studies, stated an independence from the channel width and a dependence from the inverse of the channel length [83]. Those two dependencies appear because the leakage current flows in a parasitic path, which has a channel width dependent only on the distribution of the positive charge trapped in the STI, while it has a channel length which is the same of the main MOSFET. Since the pre-radiation leak current depends on the size of the device, MOSFETs with equal  $L$  but different  $W$  have different initial levels. The current flowing in the parasitic transistors always rises, but its contribution becomes visible only when its value is higher than the parasitic current flowing in the main transistor.

It is interesting to study the radiation-response of the leakage current in different flavors of the same technology, i.e. Standard-, Low- and High- $V_{\text{TH}}$ . The method mainly used by manufacturers to change the threshold voltage, consists in manipulating the doping, increasing its level to reduce  $V_{\text{TH}}$ . The manufacturers do not specify the doping profile, but it is possible to draw some considerations on the trends. From the literature [90], it is known that low doping levels reduce the effect of the total ionizing dose on the leakage current. Therefore, devices with lower threshold voltages (higher doping level) will be more sensitive to an increase in the TID-induced leakage current (if the threshold voltage has been actually modified changing the doping profiles). Figures 6.10a, 6.10b and 6.10c show the variation of the leakage current for different flavors of threshold voltage of same size MOSFETs. It was expected to have a higher leakage current for Standard- $V_{\text{TH}}$  than for High- $V_{\text{TH}}$  devices in the pre-irradiation condition. This only happens for Group 2 ( $W = 3 \mu\text{m}$  and  $L = 30 \text{ nm}$ ), while for the other two groups the hypothesis is not verified.

In fact, already in the pre-irradiation condition (Figure 11) the leakage current for High- $V_{\text{TH}}$  devices already major the Standard- $V_{\text{TH}}$  leakage current. From voltages varying between -0.2 V and 0 V, the values of  $I_{\text{OFF}}$  for High- $V_{\text{TH}}$  and Standard- $V_{\text{TH}}$  devices does do not present a monotonous decreasing trend, as it



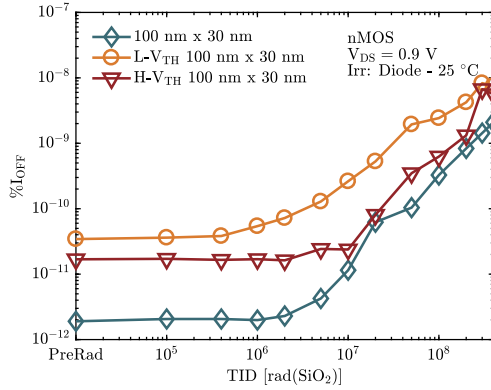
(a) Leakage current evolution for the normal  $V_{TH}$  devices. (b) Leakage current evolution for the low  $V_{TH}$  devices.



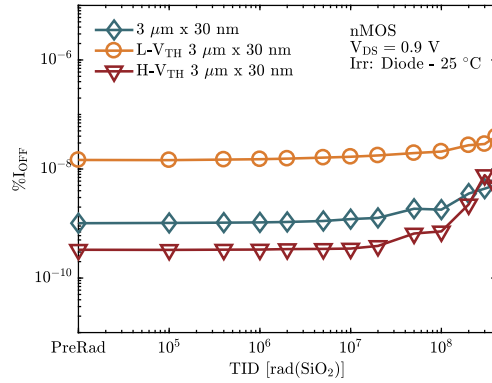
(c) Leakage current evolution for the high  $V_{TH}$  devices.

**Figure 6.9:** Leakage current evolution in function of TID for the analysed devices. The structure are divided into group in function of their threshold voltage flavour.

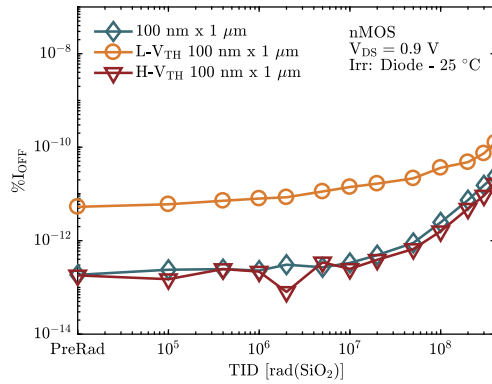




(a) Leakage current evolution for the  $W = 100$  nm and  $L = 30$  nm devices.



(b) Leakage current evolution for the  $W = 3 \mu\text{m}$  and  $L = 30$  nm devices.



(c) Leakage current evolution for the  $W = 100$  nm and  $L = 1 \mu\text{m}$   $V_{\text{TH}}$  devices.

**Figure 6.10:** Leakage current evolution in function of TID for the analysed devices. The structure are divided into group in function of their  $W$  and  $L$ .

should be in pre-irradiation conditions. The elevated pre-irradiation leakage current in the High-V<sub>TH</sub> and Standard-V<sub>TH</sub> minimum size MOSFET may be an example of Gate Induce Barrier Lowering (GIDL), which is a phenomenon that occurs when gate voltage is low, i.e. from -0.2 V to 0 V, and the drain voltage is high, i.e. 0.9 V. Under such conditions, the PN junction, intrinsically present in the MOSFETs structure undergoes reverse bias, which is strong enough to bend the conduction band and the valence band of the PN diode at a point in which the tunnel effect of electrons from the valence band to the conduction band (and of holes from conduction band to valence band) is highly probable. This movement of charge from a band with lower energy to one with higher energy level, promotes a leakage current through the gate oxide.

## 6.3 Results: pMOS

As for the nMOS, pMOS are also divided into groups, with the same rule applied for nMOS. I<sub>D</sub> vs V<sub>G</sub> curves for pre- and post-irradiation are shown in Figure 6.11.

### 6.3.1 Threshold Voltage

From Figures 6.12a 6.12b 6.12c, the variations on V<sub>TH</sub> for pMOS are smaller than in the relative nMOS devices. A step of 20 mV is used in the sweep of V<sub>G</sub>, so the variation on V<sub>TH</sub> is comparable with the granularity of the measure. For pMOSFETs, the charges trapped in both oxide and interface traps have positive sign. Therefore, both of them add up negative threshold voltage shifts. Since charge trapping at the Si/SiO<sub>2</sub> interfaces occurs slowly, oxide trapped charges are dominant in the first steps of irradiation. When the impact of the charges trapped at Si/SiO<sub>2</sub> interface also becomes significant, it results in a further decrease in threshold voltage.

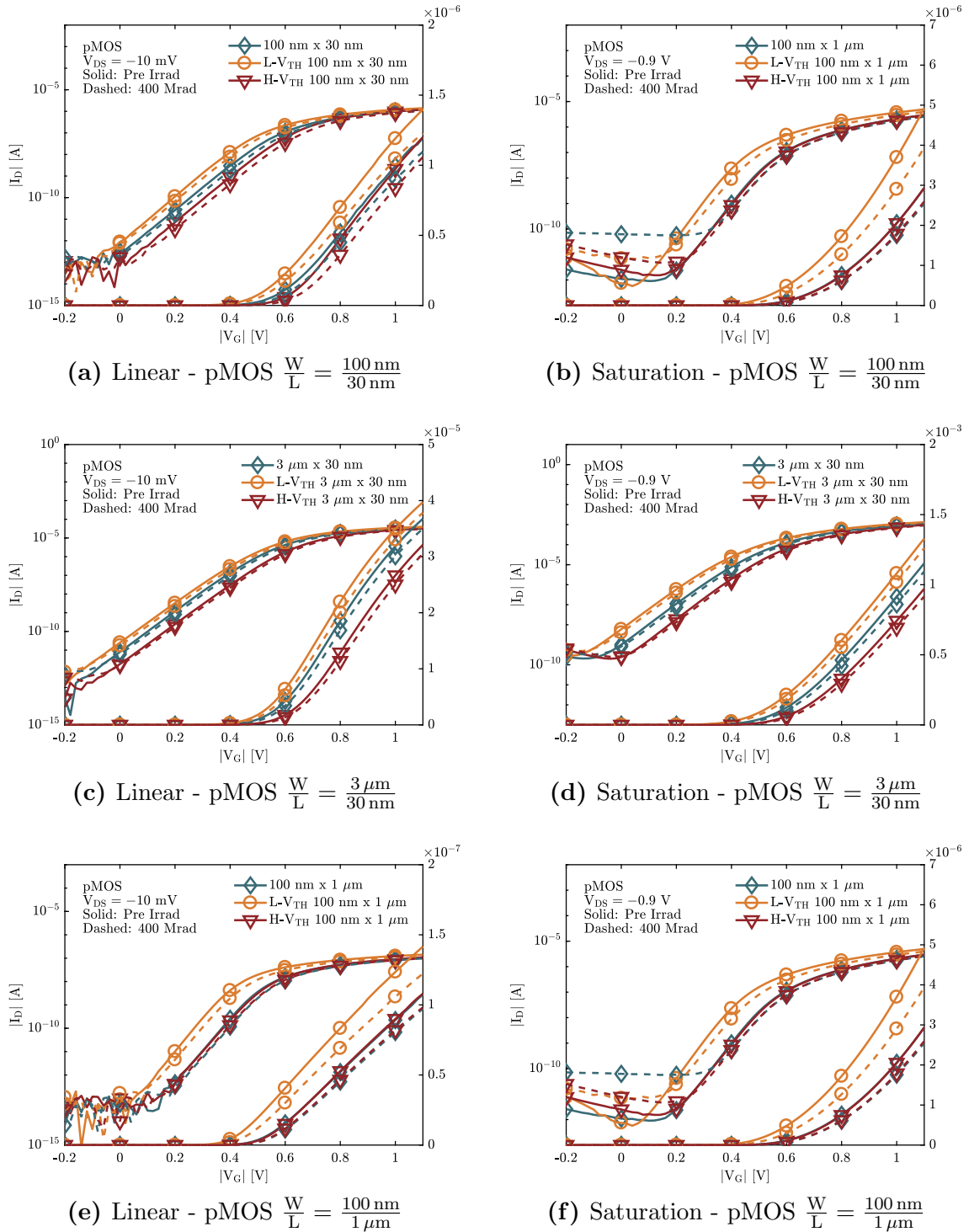
### 6.3.2 Transconductance

As for nMOSFETs, also pMOSFETs do not present relevant shift in the curve of the transconductance, as it is possible to notice in Figure 6.13 (a, b, c).

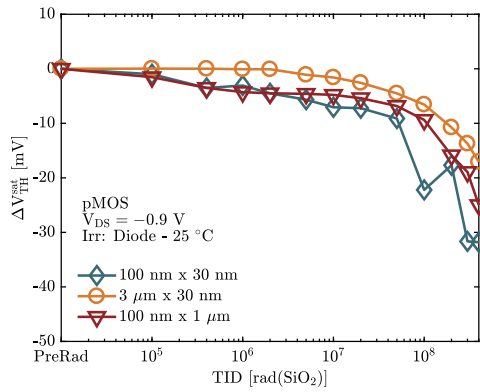
Moreover, looking at Figures 6.14 (a, b, c) it is possible to see a variation in the gm<sub>MAX</sub>, in function of TID, within the range of -10% with respect to pre irradiation conditions.

### 6.3.3 Drive Current

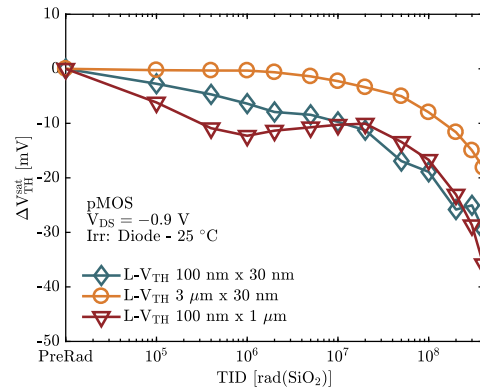
Figures 6.15 (a, b, c) show the radiation response of the I<sub>ON</sub>. Devices with narrow channel (100 nm) have a lower tolerance to TID compared to large channel pMOSFETs. In this experiment, devices with W equal to 100 nm show a degradation from 11 to 13.5 % at 400 Mrad(SiO<sub>2</sub>), while the large channel pMOSFETs, with W equal to 3 μm show a degradation of just 5 % at 400 Mrad(SiO<sub>2</sub>). The dependence of the radiation response on the W, called RINCE, has already been encountered also in other technology nodes, like 65 nm [33]. From previous studies [89], for small W, longer devices tend to degrade more at higher TID. This effect is caused by the presence of Halo, in which doping levels are lower compared to the one of the substrate. When L decreases, the two Halo regions start to overlap, lowering the



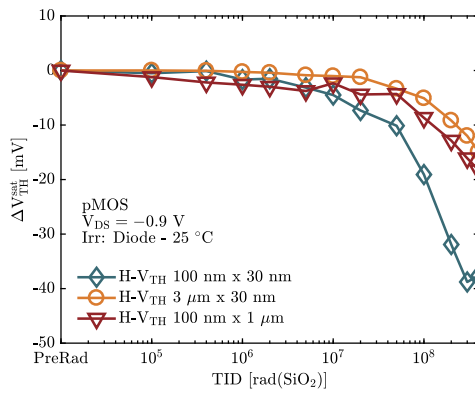
**Figure 6.11:**  $I_D$  vs  $V_{GS}$  curves for all pMOS devices, irradiated up to 400 Mrad in diode configuration. In the left column the curves for linear zone are presented, while the right contains the curves for the saturation zone. The MOS are divided in group in function of their W and L dimensions.



(a) Threshold voltage evolution in function of TID for the standard  $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

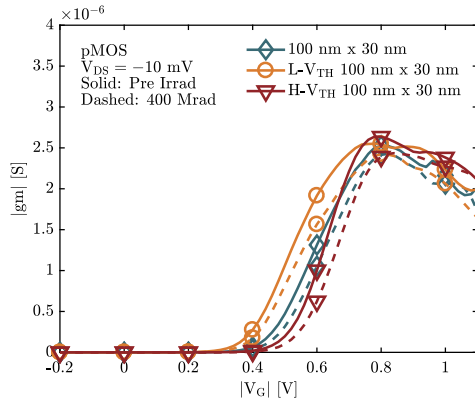


(b) Threshold voltage evolution in function of TID for the Low- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

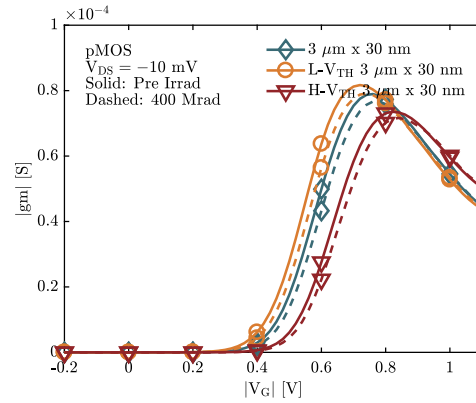


(c) Threshold voltage evolution in function of TID for the High- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

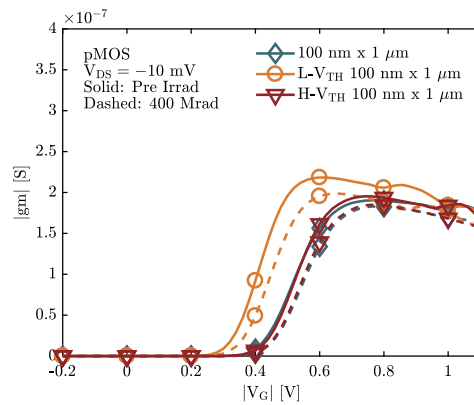
**Figure 6.12:** Evolution of the threshold voltages for the whole set of devices analysed for the 28 nm technology node.



(a) Transconductance evolution in function of TID for the 100 nm x 30 nm devices, calculated with  $V_{DS} = 10$  mV.

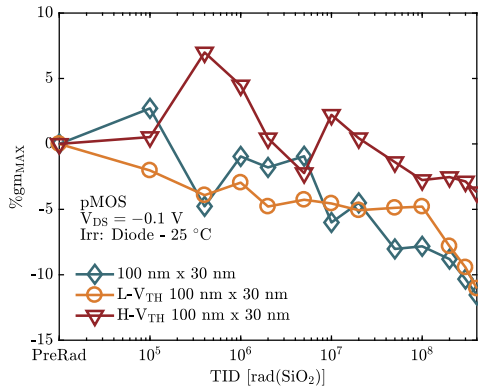


(b) Threshold voltage evolution in function of TID for the Low- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

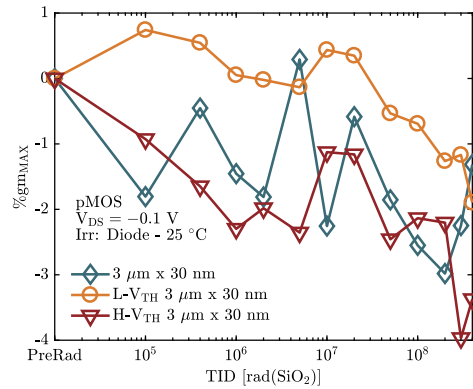


(c) Threshold voltage evolution in function of TID for the High- $V_{TH}$  devices, calculated with  $V_{DS} = 1.2$  V.

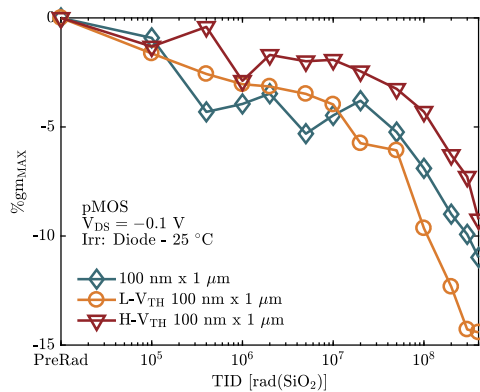
**Figure 6.13:** Comparison between pre- and post-irradiation transconductance curves for the devices analysed. The structure are divided into group in function of their threshold voltage flavour.



(a) Transconductance peak evolution in function of TID for the standard threshold voltage flavour, calculated with  $V_{DS} = 10$  mV.

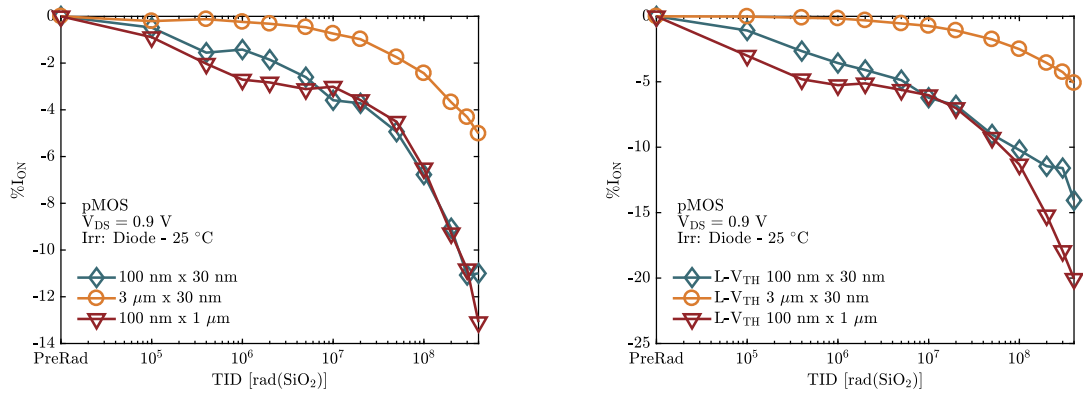


(b) Transconductance peak evolution in function of TID for the low threshold voltage flavour, calculated with  $V_{DS} = 10$  mV.



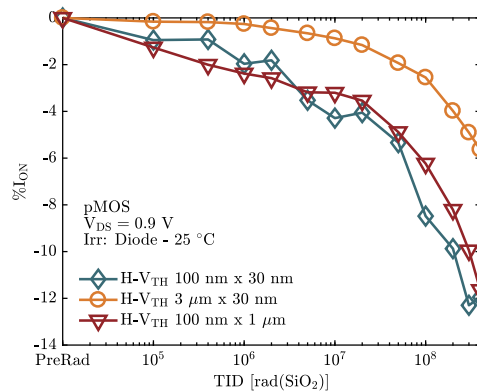
(c) Transconductance peak evolution in function of TID for the high threshold voltage flavour, calculated with  $V_{DS} = 10$  mV.

**Figure 6.14:** Evolution of the peak of the transconductance for the analysed devices. The structure are divided into group in function of their threshold voltage flavour.



(a) Drive current evolution in function of TID for the standard flavour devices.

(b) Drive current evolution in function of TID for the low flavour devices.



(c) Drive current evolution in function of TID for the high flavour devices.

**Figure 6.15:** Drive current evolution in function of TID for the analysed devices. The structure are divided into group in function of their threshold voltage flavour.

doping in the channel [89]. This trend is valid for channel lengths up to about 200 nm, after which the degradation is no longer dependent on channel length [89]. In the array used to analyze Man. A 28 nm CMOS technology, there were no devices with  $W = 100$  nm and  $L$  varying between 30 nm and 200 nm, except for the one having minimum dimensions. Therefore, it is not possible to state how strong is the effect generated from the overlap between Halo for MOSFETs produced by Man. A.

## 6.4 Final Comments on Manufacturer A 28 nm

The  $I_D$  vs  $V_G$  curves of nMOS and pMOS have been presented in both linear and saturation region. An increase in the drive current in saturation has been reported for all nMOS, while all pMOS shown a degradation in the drive current.  $V_{TH}$ , calculated for a TID of 400 Mrad(SiO<sub>2</sub>), varies less than 60 mV for all the devices, both nMOSFETs and pMOSFETs. The transconductance shows a variation of maximum -9 % for a TID of 400 Mrad(SiO<sub>2</sub>). Analyzing the variation of  $V_{TH}$  and  $g_m$ , no big changes on  $I_{ON}$  were expected. In fact, it is possible to see a variation in the drive current contained in the +20 % range with respect to pre-irradiation conditions for nMOS and -20 % for pMOS. Additionally, the variation in the drive current for minimum size MOS is remarkably small, compared to the changes of the same parameter for the minimum size MOS in 65 nm technology [69]. The variation of the leakage current as a function of the TID has no dependence on channel width but increases as  $1/L$ . The observed variation of the  $I_{OFF}$  can be attributed to the positive charge trapping in the STI oxide, which is able to invert the adjacent p-type silicon layer along the STI side of the channel, forming parasitic conductive paths ([83] - [69] - [89]). From these results, it is possible to state the main contributors to the radiation response of this technology are the STI oxides.

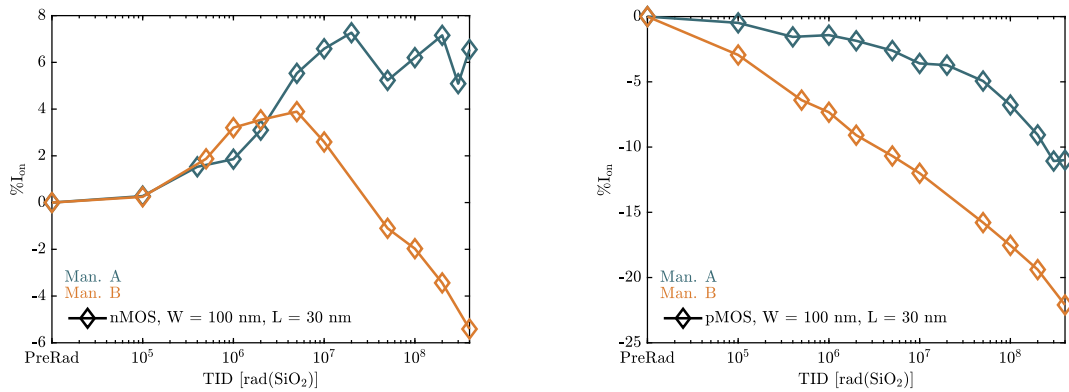
## 6.5 Manufacturer A vs Manufacturer B

This section presents a comparison between Man. A and Man. B 28 nm minimum dimensions and standard flavour transistors. The only two parameters that will be discussed are the drive and leakage currents.

Figures 6.16 (a, b) compare percentage variations of  $I_{ON}$  as a function of TID for Man. A and Man. B 28 nm CMOS technology node for MOSFETs with Standard- $V_{TH}$ . For Man. B devices, when a certain TID is reached, the initial increase caused by the faster charge trapping in the oxide is balanced by the charge trapping at the Si/SiO<sub>2</sub> interface. Therefore a net decrease occurs, bringing the drive current almost at its initial level or even lower. It is not straightforward to determine if there is a smaller number of traps in the oxide for Man. B devices, or if the interface charge trapping is faster for these MOSFETs.

As it is possible to notice in Figure 6.17, also the device produced by Man. B shows a considerable radiation-induced variation in the  $I_{OFF}$ . It is evident that the same hypothesis on channel width independence and channel length dependence are also valid for the Man. B device. The initial values of leakage current for same size devices are different within the two companies, probably stating a difference in the doping levels and in the general manufacturing process. The pre-irradiation value of

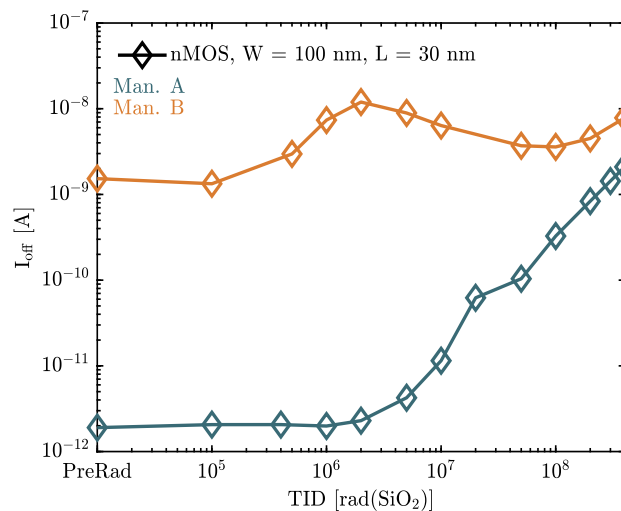




(a) Percentage variation of  $I_{ON}$  for nMOS  $W = 100$  nm,  $L = 30$  nm, irradiated up to 400 Mrad.

(b) Percentage variation of  $I_{ON}$  for pMOS  $W = 100$  nm,  $L = 30$  nm, irradiated up to 400 Mrad.

**Figure 6.16:** Drive current comparison between two different manufacturers minimum size, standard flavour nMOs and pMOS. Devices produced by Man. A are represented in blue, while the one created by Man. B are shown in orange.



**Figure 6.17:** Leakage current evolution comparison between minimum size, standard flavour nMOSETs produced by Man. A (blue) and Man. B (orange).

the leakage current is around three order of magnitude higher in the Man. B device.

# Chapter 7

## Conclusions

The 65 nm technology is used in the design of most of the circuitry developed for CERN applications. It is also subject to very high ionizing doses, in the order of 1 Grad(SiO<sub>2</sub>) in 10 years. This means that the dose-rate is approximately in the order of 0.01 Mrad/h. Starting from the first observations carried out by Borghello in [13], we have continued the analysis of dose-rate dependence in this technology. We have confirmed that lower dose-rates result in higher degradation in both nMOS and pMOS. We therefore focused more on nMOS, as the difference between the degradation encountered at high and low dose-rates is greater than in pMOS. We observed a dependence on the channel length. In fact, only short-channel devices (60 nm), have increased degradation at low dose-rates. On the other hand, long channel devices (10  $\mu$ m), have proved to be completely unaffected by changes in the dose-rates. Then we focused on bias. We noticed that the diode connection is the only condition in which increased degradation occurs at low dose-rate. It is already known that this configuration is the worst-case for 65 nm technology [33]. The fact that the dependence on the dose-rate occurs only in diode connection is positive, as the devices are not always continuously connected to diode, so in our studies this effect is certainly accentuated. We have also analyzed how temperature affects dose-rate dependence. Low temperatures ( $T = -30^\circ\text{C}$ ) mitigate the dependence on DR. Again, this result is extremely encouraging for CERN applications. In fact, the circuitry implemented at the collision points is consistently maintained at  $-30^\circ\text{C}$  [77]. Thanks to the above mentioned short channel length dependence, we also observed that charge trapping processes that are dependent from the dose-rates occur in only one of the two auxiliary oxides: the spacers. Spacers are similar to BJT oxides, already known to be susceptible to ELDRS [43, 44, 50]. To describe the dose-rate dependence, we have therefore applied to our MOSFETs one of the most widely accepted model, proposed for the BJTs [43]. We have proposed a low dose-rate model which is the extension of the model developed for high DRs proposed by Faccio in [63]. Finally, we created a coefficient that could estimate the degradation of a device. Usually the devices are irradiated at high dose-rates, so the degradation they encounter is certainly less than the real one. With the proposed coefficient it is possible to estimate the damage encountered at low dose-rates without carrying out the relative radiation at low DR.

We have seen how 28 nm technology can be a solid choice in future CERN applications. The current drive of this technology degrades much less than older technology nodes, even at ultra-high levels of TID. On the other hand, the increase

in leakage current is a major constraint for this technology. It will be necessary to assess whether such an increase could represent a problem of power consuming for future applications and, in this case, such technology may not be easily usable, despite the great robustness of the current drive.

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# Appendix A

## Source-to-drain resistance extrapolation

The total resistance of a MOSFET is indicated with  $R_{TOT}$  and is the sum of two components:  $R_{CH}$  and  $R_{SD}$ . The first one is the intrinsic resistance of the channel, while the latter one is the source-to-drain resistance. As the values of  $R_{SD}$  can be affected by radiation-induced changes, we want to extract its values. The linear extrapolation of the total resistance seen between source and drain,  $R_{SD}$ , is obtained measuring an array containing MOSFET with different channel lengths and constant channel width. This method is based on the BSIM3v3 model, in which it is possible to extrapolate the effective channel length  $L_{eff}$ , useful to determine the  $\beta$  coefficient, which will be necessary to extrapolate  $R_{SD}$ . The current flowing in the drain terminal is expressed as follows:

$$I_D = \beta V_{OV} \frac{V_{DS} - R_{SD}I_D}{1 + \theta_1 V_{OV} + \theta_2 V_{OV}^2} \quad (A.1)$$

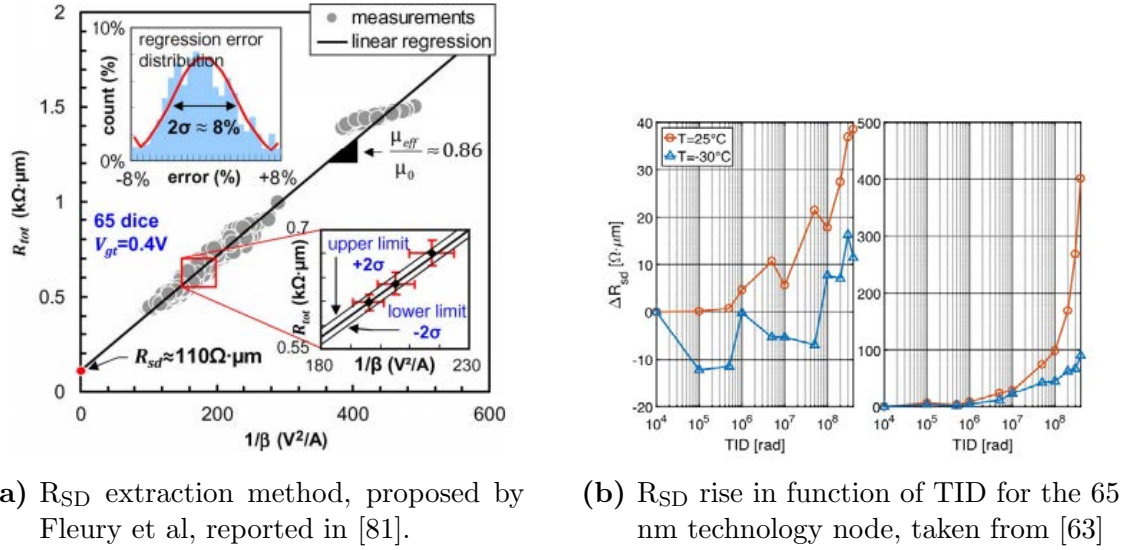
Where:

- $V_{OV}$  is the overdrive voltage  $V_{GS} - V_{TH}$
- $V_{DS}$  is the drain to source voltage
- $R_{SD}$  is the source to drain resistance, to be extrapolated
- $I_D$  is the drain current
- $\theta_1$  and  $\theta_2$  are fitting parameters which account for the mobility decrease, and are assumed constant for a given technology
- $\beta$  is the transconductance gain, defined as  $\beta = \mu_0 C_{eff} \frac{W}{L_{eff}}$  and  $C_{eff}$  is the effective gate oxide capacitance in strong inversion

Once the overdrive voltage is fixed for a set of devices with several lengths, the equation provides a useful relation that links  $R_{TOT}$  to  $\beta$  and allows to extract  $R_{SD}$ .

$$R_{TOT} = \frac{V_{DS}}{I_D} = \frac{1}{\beta} \times \frac{1 + \theta_1 V_{OV} + \theta_2 V_{OV}^2}{V_{OV}} + R_{SD} \quad (A.2)$$

It is possible to extract  $R_{SD}$  as the intercept of the least mean squares linear regression performed on  $R_{TOT}$  versus  $\frac{1}{\beta}$ . The procedure is graphically reported in Figure A.1a. In particular, in their experiment, Faccio et al., used an array of nMOS and



**Figure A.1:**  $R_{SD}$  extraction method proposed by Felury [81] and results obtained by Faccio in [63].

one of pMOS with L varying from 60 nm to 4  $\mu\text{m}$ , with W fixed at 20  $\mu\text{m}$ , big enough to make RINC-effect negligible [33]. They irradiated up to 400 Mrad( $\text{SiO}_2$ ) the 65 nm technology node array at two different temperature and measured  $R_{SD}$ . The results are shown in Figure A.1b.