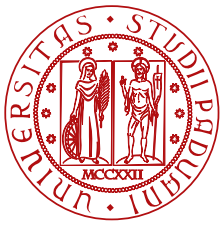

UNIVERSITÀ DEGLI STUDI DI PADOVA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

CORSO DI LAUREA IN INGEGNERIA ELETTRONICA

Design and Development of a DC/DC Converter for High-Voltage Pulsed Electrical Stimulation

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Data di laurea 23/09/2024

to those who
give their all

Contents

Introduction

The objective of this thesis is to design, simulate and fully assemble a very compact, portable, and optionally wearable voltage conversion device to be used for electrical stimulation purposes.
Most electrical stimulation techniques involve the generation of a repetitive waveform, arbitrarily spaced, with an amplitude that depends on the application. These electrical pulses are applied via two or more electrodes on the skin of the area of the human body interested by the treatment. A typical example of such signal could be a train of triangular pulses (duration 10us), equally spaced (frequency 100 Hz), with an amplitude of 300V.

The most common used electrical stimulation techniques are the following:

- Transcutaneous Electrical Neuromuscular Stimulation (TENS)
- Neuromuscular Electrical Stimulation (NMES)
- Interferential Current (IFC)
- High-Voltage Galvanic Current (HVGC)
- Electrical muscle stimulation (EMS)

Each one of these techniques is characterized by its own waveform, frequency, amplitude range, and most importantly, desired therapeutic effects.
An in-depth analysis of these kind of treatments is beyond the purpose of this thesis, but among the reasons a patient may need one of these therapies are:

- Short and long term pain management in physical therapy
- Forcing contraction of some muscle groups, stimulating blood flow to the area of interest
- Muscular relaxation and relief
- Wounds repairing process improvement

Several electro-stimulators capable of performing some of the previously mentioned therapies are already commercially available. For instance, a TENS device can be observed in the following picture.

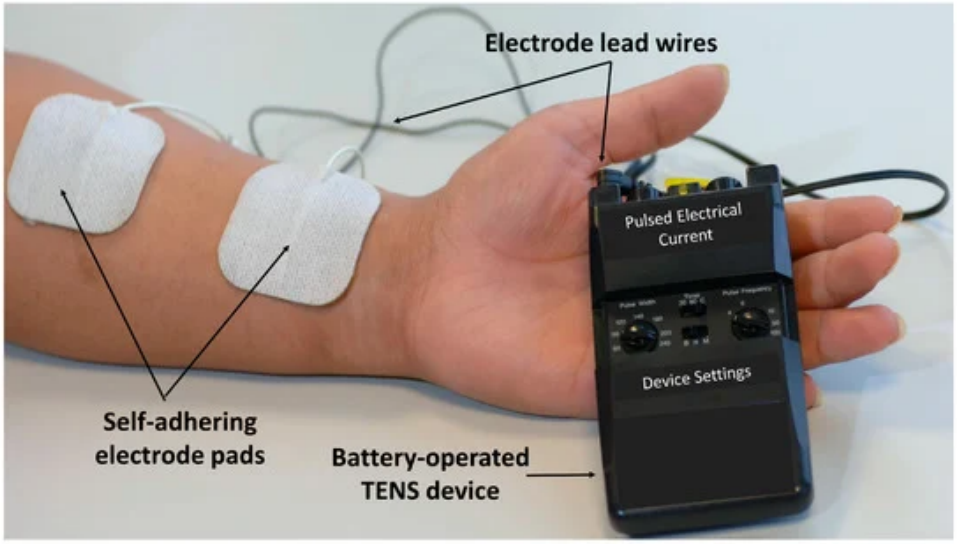


Figure 2: COMMERCIAL TENS device: forearm application. LEFT knob regulates pulse width; RIGHT knob regulates frequency; amplitude: 50-100V range

The main challenges of this project will be to drastically reduce the size of this kind of device and fit it into a very small form factor, lipo-battery powered device, such as a smartwatch. This requirement comes from the main potential application that this device is intended to have. Generally speaking, electro-stimulation therapies are performed in a static way: the electrodes are applied on the area of interest and the therapy starts. Other experimental approaches consist on carrying out conventional physiotherapy in conjunction with treatments using an electro-stimulation device. In order to achieve this, the physiotherapist should wear a portable device interfaced with a special isolated glove covered by electrodes.

This device will be able to generate a monophasic waveform, consisting of a series of high voltage pulses of fixed duration (approximately 5 -10 us). The interval between these pulses will be adjustable and programmable through two on-board touchscreens and a user interface available on the device display. Despite the fixed duration, these short pulses may be generated consecutively (back to back) to create the effect of a longer one.
Even though the commercially available electro-stimulators are able to reach, in the case of HVGC, voltages up to around 500V maximum, another ambitious goal for this project is to design a device capable to generate a widely adjustable voltage amplitude signal, ranging from 50 V to 15 kV, starting from a 3.7V lipo-battery.

The effects of high voltage (>1 Kv) treatments are highly dangerous and great care must be

taken when dealing with this kind of signals. The reason why this feature will be implemented for this device is due to the lack of experimental work and literature concerning the application of such short duration, very high voltage pulses, resulting in a small output power absorbed by the patient's body. As a final point, this device aims to allow medical experts and physical therapists to research and test some experimental and potentially promising electro-stimulation treatments in uncharted territory.

Chapter 1

General Configuration

In this chapter the hardware configuration and structure of the device will be discussed. The device consists of a stack-up of two PCBs and several auxiliary interface boards:

POWER PCB

- Battery management system
- LC filter
- High-voltage pulse generator

LOGIC AND CONTROL PCB

- Microcontroller
- User interface : Display, Touch buttons
- Peak-current mode control circuit
- Power management circuit

Interface boards

- High-voltage path guide with connector
- Output demonstration board

1.1 POWER PCB Configuration

The POWER PCB contains all the power electronics circuitry, and handles the high current path flowing from the battery to the switching circuit. A micro-USB port used for charging and/or programming the microcontroller is also included and accessible from this board. More specifically, it includes:

- **Battery management system and LC filter**: The BMS [Battery Management System] is composed of the charging circuit (5V micro-USB port) and the overcurrent/overvoltage battery protection. The current drawn by the switching circuit can result in considerably high current peaks; therefore, a LC filter is required to avoid unnecessary electrical stress on the battery and filter-out higher current harmonics.
- **High-voltage pulse generator**: The heart of the POWER PCB is the High-Voltage pulse generator: this is a switching circuit which exploits the very fundamental Faraday's law of induction to produce a voltage pulse on the primary winding of a high turn-ratio isolated transformer, resulting in a much greater voltage peak at the secondary winding. Two independent snubber circuits can be activated to provide some flexibility and accuracy in the output voltage level.

1.2 LOGIC & CONTROL PCB Configuration

The LOGIC & CONTROL PCB is an electronic board built around the microcontroller, which drives the display user interface, monitors the touch buttons and activates the input to the switching circuit according to the peak current mode control algorithm. This board contains all the low voltage sensing conditioning circuits to be fed into the microcontroller ADC, as well as a discrete component circuit that handles the different power modes that will be presented in next chapters. More specifically, it includes:

- **Microcontroller and user interface**: The R7FA4M1AB3CFM from Renesas is A 32-bit, 48 MHz Arm Cortex-M4 high performance microcontroller, with 14 bit ADC and a 12-bit DAC, USB 2.0 native compatibility and other features that particularly suited to the design of this device. The user interface is displayed on a 240x240 IPS screen, while the interaction with the device is facilitated by two touch buttons on the lower part of the front panel.
- **Battery SoC and Peak current mode control circuitry**: The battery state of charge is solely determined based on the battery voltage level (after a proper V/I characterization), but future versions of the device will include a battery current sensor allowing for precise

integration of the battery current over time. The peak current mode control circuit allows the microcontroller to set a current threshold via the DAC, when the primary winding current exceeds the threshold, an interrupt is generated.

- **Selective power shutdown circuit**: This circuit handles the power-on and power-off of the various sections of the device (i.e., the display, the sensing circuitry...). By combining software and hardware solutions, the maximum theoretical battery life of this device can reach ∼12 days.

1.3 Mechanical case structure and Constraints

A critical requirement for this design lies in the limited size and dimensions of the device case, and , considering that it should be wearable, its form factor falls into the realm of smartwatches. As a reference for general dimensions, a commercial smartwatch was considered:

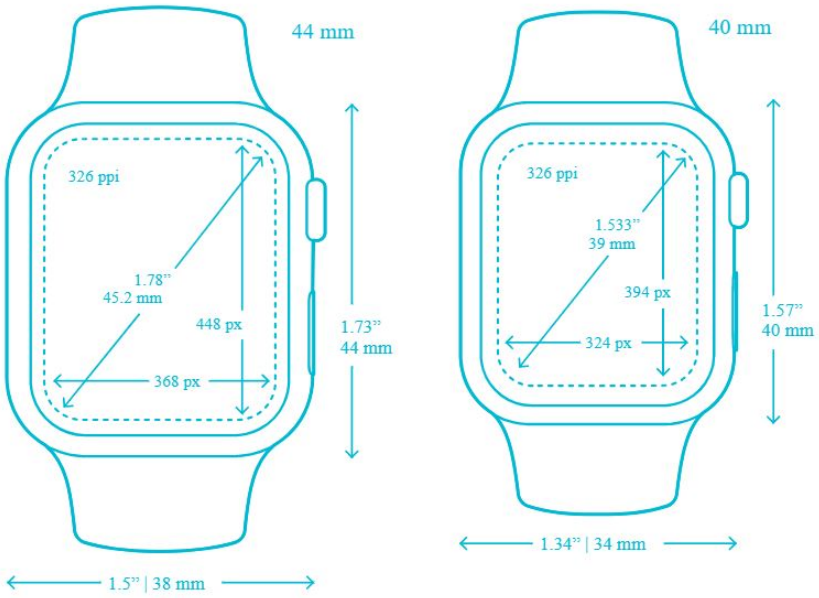


Figure 1.1: Dimensions of APPLE watch series 6

Before designing the final device enclosure, it's essential to identify the major constraints and build the rest of the structure around them, drawing inspiration from the size and shape of a typical smartwatch such as the one presented above.
The following are the most significant constraints to be considered:

- Battery

- High Voltage Transformers
- Display size and Touch buttons

Other factors, such as the connectors accessibility, are a bit premature to consider and will be addressed when the PCB design is complete. The important thing for the moment is to have an initial PCB board shape to work with. The picture below and the document after that, illustrate the CAD model assembly of the device, without including all the electronics, that will be custom designed inside this enclosure. The final expected size is aligned with the desired mechanical profile: [33mm x 41 mm x 12 mm] which can be commonly found in a variety of commercial smartwatches.

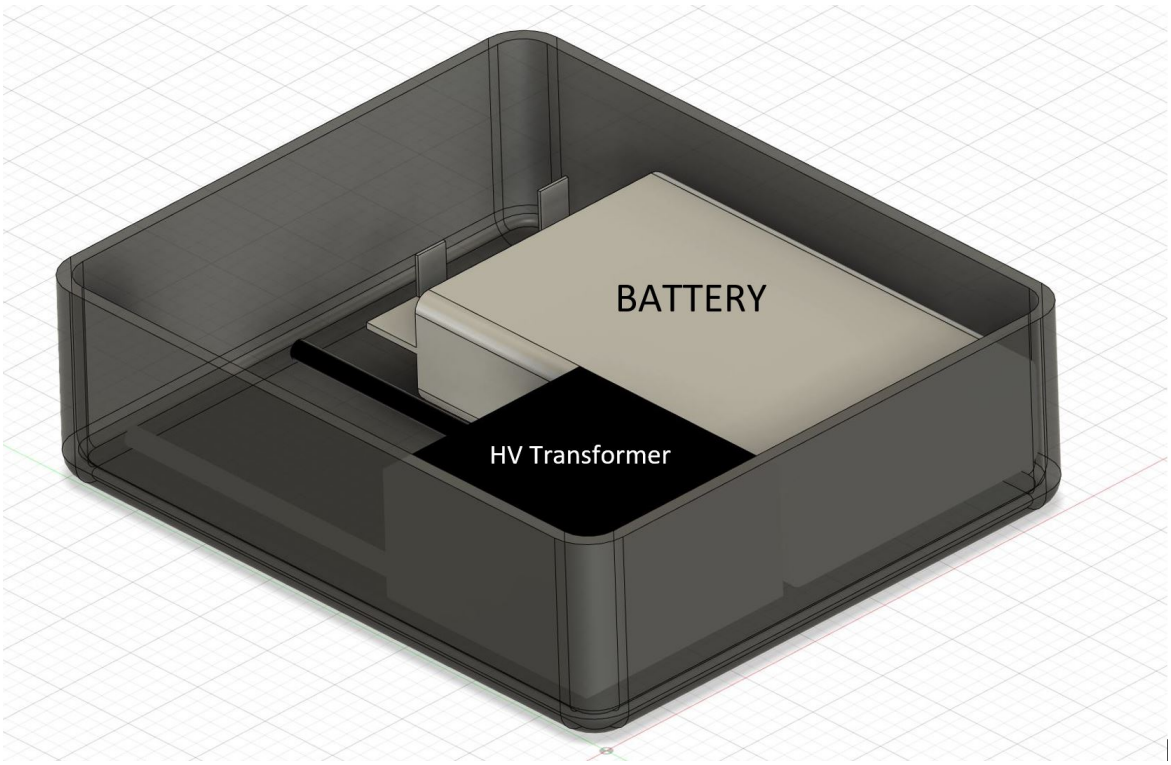
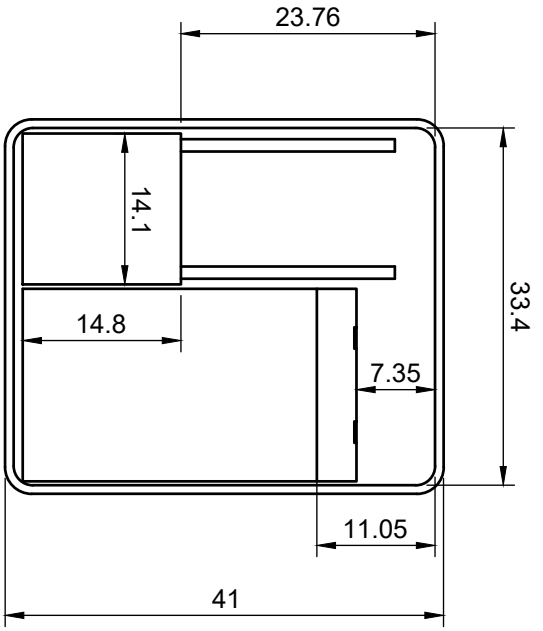
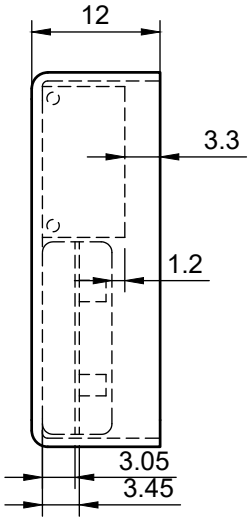
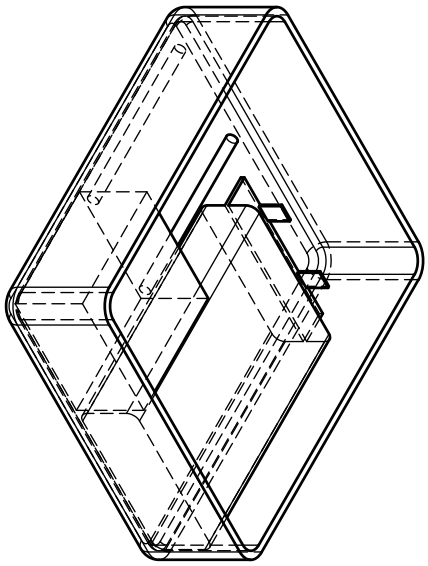
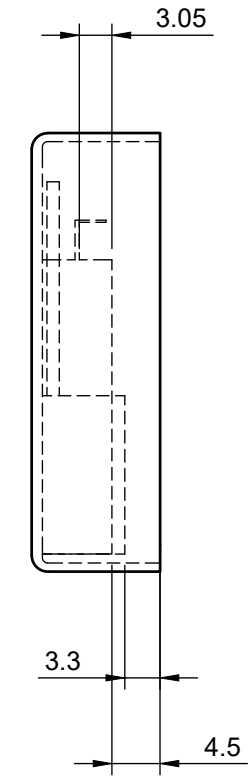


Figure 1.2: 3D view of the initial case configuration









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	Technical reference		
	Created by	Francesco Soppera	
	Document type		
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Rev.	Date of issue	DWG No.	Document status
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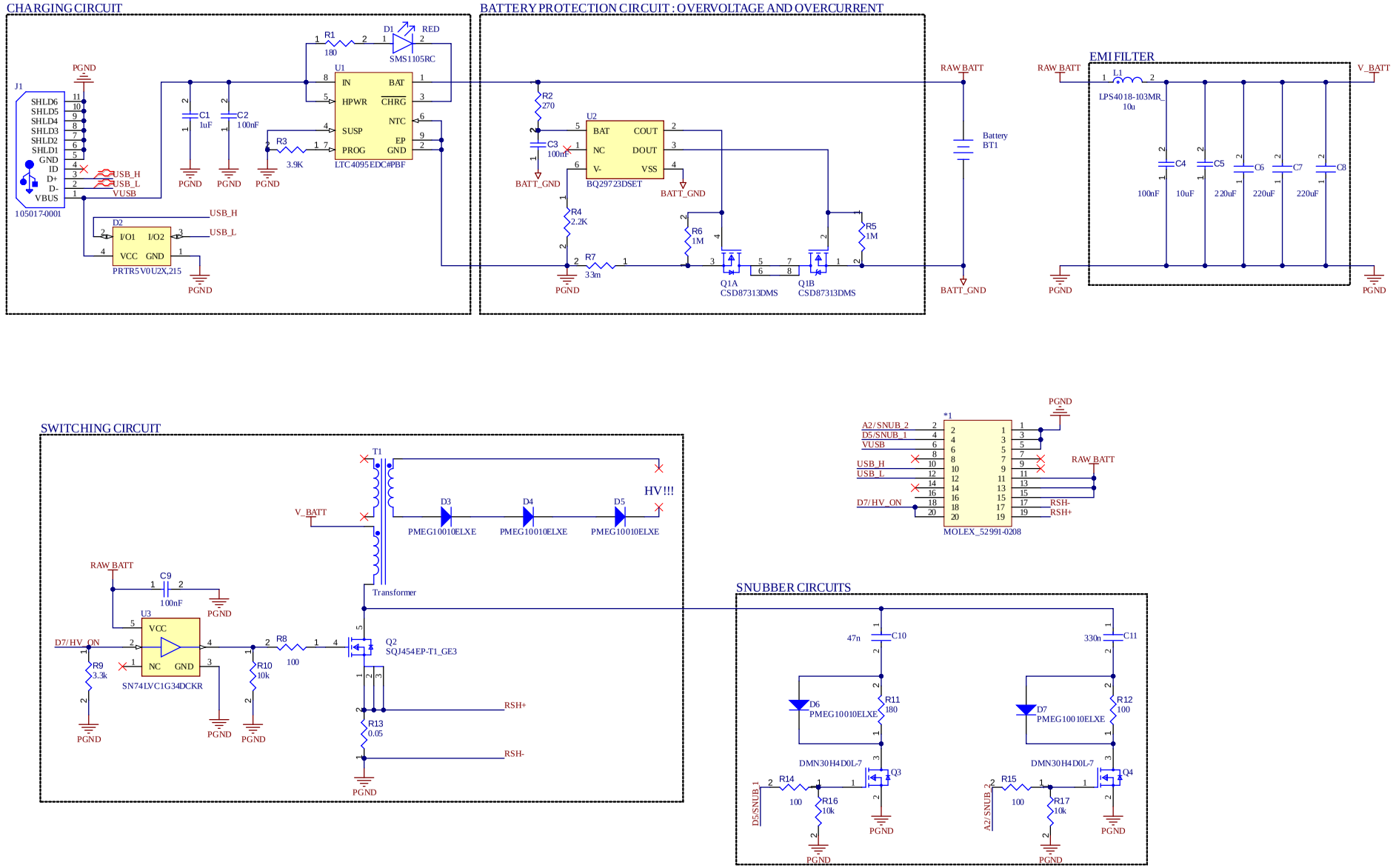
CHARGING CIRCUIT
BATTERY PROTECTION CIRCUIT : OVERVOLTAGE AND OVERCURRENT
EMI FILTER
SWITCHING CIRCUIT
SNUBBER CIRCUITS
J1
105017-0001
U1
LTC4095EDC#PBF
U2
BQ29723DSET
D1
SMS1105RC
D2
PRTR5V0U2X,215
T1
Transformer
U3
SN74LVC1G34DCKR
Q1A
CSD87313DMS
Q1B
CSD87313DMS
Q2
SQJ454EP-T1_GE3
Q3
Q4
D3
PMEG10010ELXE
D4
PMEG10010ELXE
D5
PMEG10010ELXE
D6
PMEG10010ELXE
D7
PMEG10010ELXE
MOLEX_52991-0208
LPS4018-103MR_
10u
Battery
BT1
PGND
RAW_BATT
V_BATT
BATT_GND
USB_H
USB_L
VUSB
D7/HV_ON
HV!!!
RSH+
RSH-
A2/SNUB_2
D5/SNUB_1
DMN30H4D0L-7
Title
POWER_PCB SCHEMATIC
Size
A3
Number
Revision
Date: 9/05/2024
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File: C:\Users\..\Sheet1.SchDoc
Drawn By: Francesco Soppera

Chapter 2

POWER PCB

In this chapter the schematic of the POWER PCB will be described, along with the corresponding SPICE simulation results. The full schematic is available in the previous page.

2.1 Battery characterization

The choice of the battery was driven by space and dimensional requirements. Lithium-polymer batteries usually represents the best choice in terms of energy capacity per unit volume, moreover they are generally capable of withstanding higher electrical stress, such as higher currents. The price to be paid for these favorable points resides in the measures required to guarantee safe operation, in fact, unlike other battery types, Li-Po batteries tend to be more susceptible to overheating and fire hazards if not used or handled properly.
In light of the previous considerations, the battery chosen for this design is a 260mAh, 10C, 3.7 V, 601730 Li-Po battery. (6 mm x 17mm x 30 mm).

In order to provide a state of charge estimation based only on the battery voltage, a discharge curve characterization was performed on two similar batteries: BAT1 [601730]: (6x17x30[mm]) [260mAh] and BAT2 [602030]:(6x20x30 [mm]) [300mAh]. BAT2 curves will be illustrated, but as previously mentioned, BAT1 was chosen for this project. The characterization was accomplished by applying an initial load of 30 Ω, while measuring the battery voltage and current at regular intervals. When the battery voltage dropped below 3V, the load was swapped with a lighter one (220 Ω), allowing for complete battery draining.

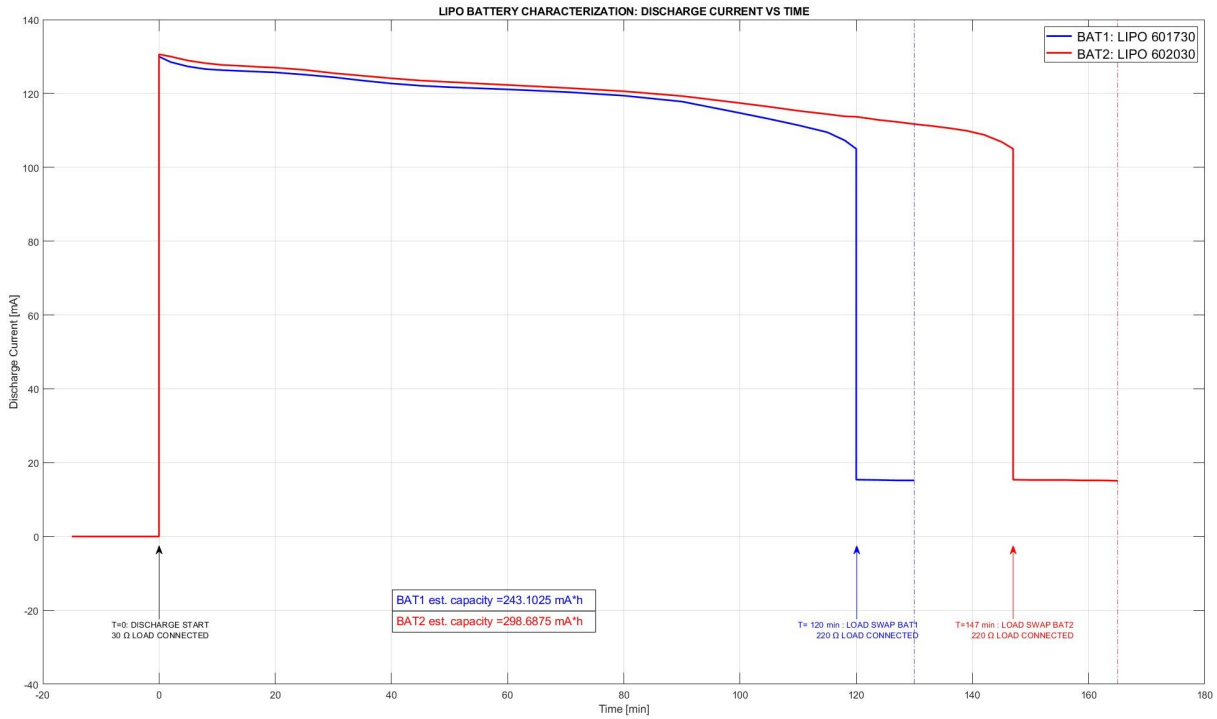


Figure 2.1: Battery characterization: Battery current vs time

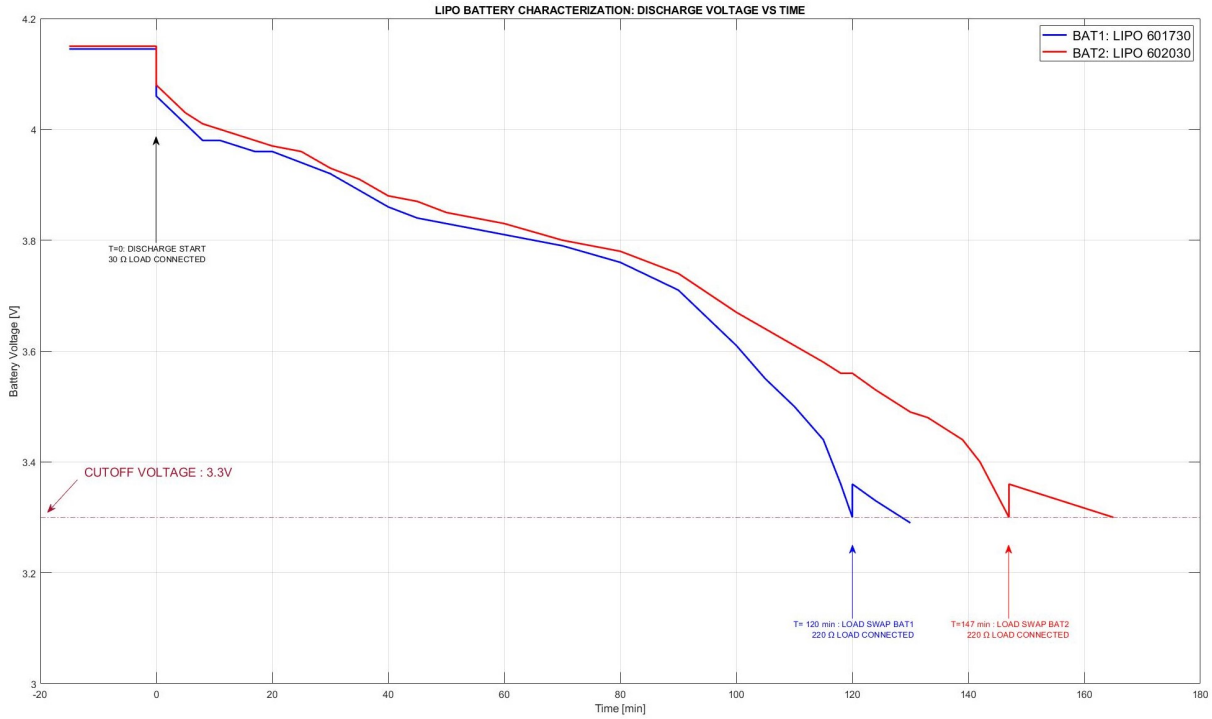


Figure 2.2: Battery characterization: Battery voltage vs time

Obviously the output resistance of the battery plays a big role in this characterization, and its effect can be observed in the battery voltage drop after the 30Ω load is connected. For this reason the output resistance needs to be estimated:

$$ESR_{BATT} = V_{ESR_{BATT}}/I_{BATT} = 0.07V/130mA \approx 500m\Omega \tag{2.1}$$

where $V_{ESR_{BATT}}$ corresponds to the battery negative step amplitude after the load insertion. For these reasons the real curve to be considered for a state of charge estimation needs to be compensated and adjusted to account for the output series resistance and battery current. In the absence of a battery current sensor it's possible to evaluate empirically the current consumption of the circuit in different power modes and consider the related shifted curve. Clearly the final result will not be as accurate as having a battery current sensing circuit, but it will give the user a reasonable idea of the battery state of charge.

2.2 Battery Manegement System [BMS]

Commercially available Li-Po batteries normally have an integrated protection directly connected to the battery tabs, covered with some kapton tape. In order to save space this protection was removed, and a new custom protection circuit was implemented directly on the POWER PCB, providing more flexibility and additional safety measures specific to the application.

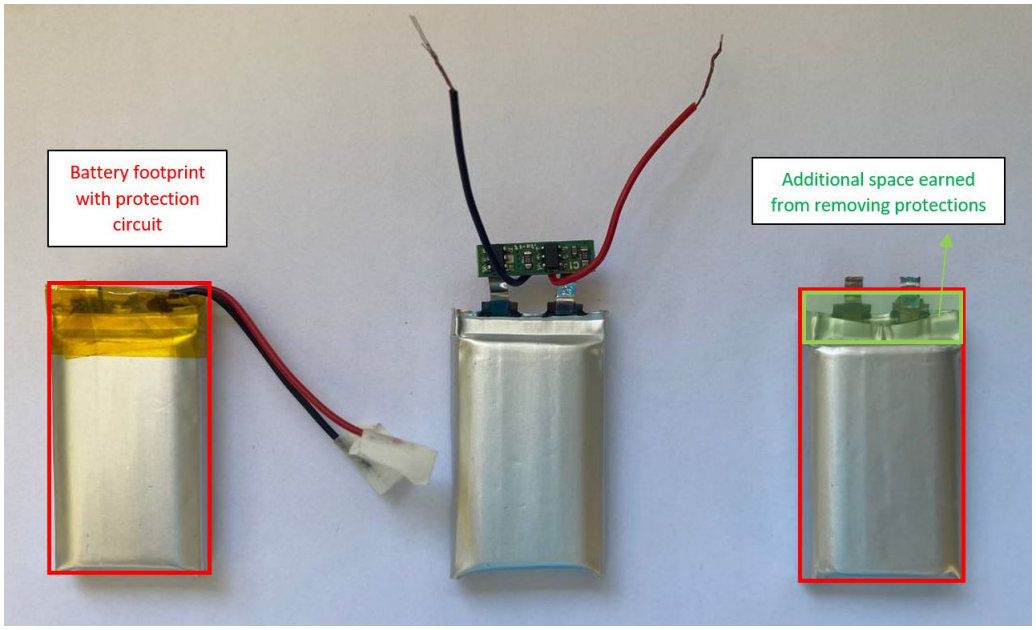


Figure 2.3: Protection circuit removal benefit

The following schematic portrays the custom protection implemented in the POWER PCB:

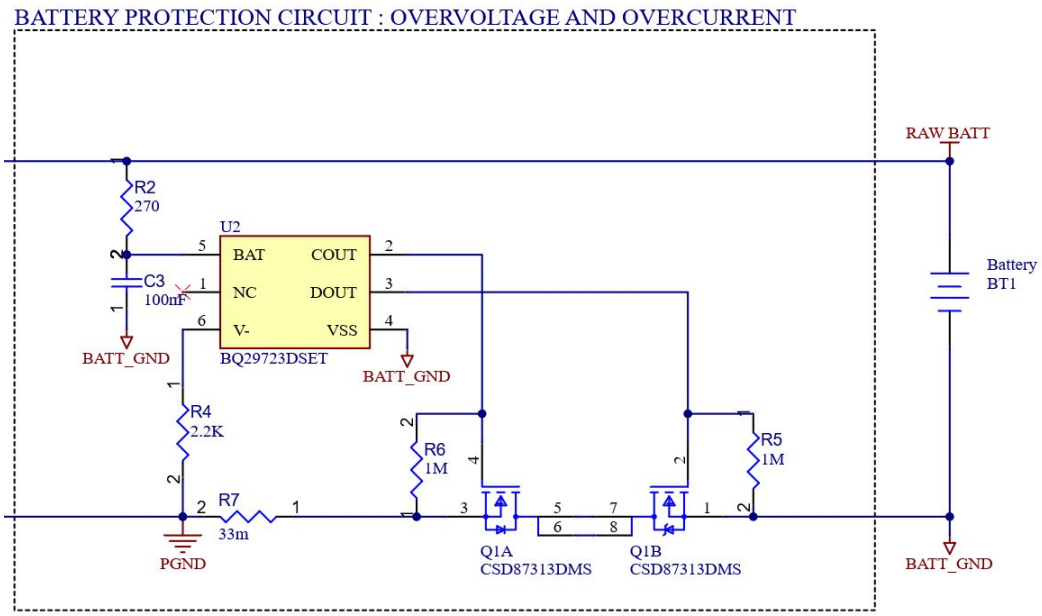


Figure 2.4: Battery overvoltage and overcurrent protection circuit

The BQ29723 [1] is a single cell Li-Po battery protection circuit, capable of detecting a number of major faults, among which are:

- Overcharge detection
- Short circuit detection
- Over-discharge detection
- Charge and Discharge overcurrent detection

The different thresholds for these safety features can be set by means of a limited number of discrete external components. The BQ29723 intervenes by isolating the battery from the rest of the circuit whenever a fault occurs, controlling the gates of a dual N-Channel mosfet (CSD87313DMS [2]) transitioning the system into a safe state. The BQ29723 datasheet [1] is very detailed and extensive and should be examined carefully, but here is a summary of the relevant characteristics and expected results of the solution illustrated above:

- Overvoltage limit = 4.425V
- Undervoltage limit = 2.5V
- Charge overcurrent threshold = 1A, but irrelevant since the current is already limited to 200mA by the charging circuit

- Discharge overcurrent threshold = 2.5 A
- short circuit overcurrent threshold = 7 A

While for selecting the under/over voltage [OVP,UVP] limit it is sufficient to choose the right IC model from the table below, the current thresholds [OCD, SCD] are given as the voltage drop of the series combination of the shunt resistor R7 and the ON-resistance of the dual N-channel mosfet.

4 Device Comparison Table

PART NUMBER(1)	OVP (V)	OVP DELAY (sec)	UVP (V)	UVP DELAY (ms)	OCC (V)	OCC DELAY (ms)	OCD (V)	OCD DELAY (ms)	SCD (V)	SCD DELAY (µs)
BQ29700	4.275	1.25	2.800	144	–0.100	8	0.100	20	0.5	250
BQ29723	4.425	1	2.500	96	–0.060	4	0.100	8	0.3	250
BQ29702	4.350	1	2.800	96	–0.155	8	0.160	16	0.3	250
BQ29703	4.425	1.25	2.300	20	–0.100	8	0.160	8	0.5	250

Figure 2.5: Device comparison table from [1]

Since the mosfet on-resistance depends on the operating point of the circuit, R7 needs to be selected carefully. A first value for R7 was calculated from the $R_{DS_{ON}}$ vs V_{GS} curve that can be found in the CSD87313DMS datasheet [2], and then refined with SPICE simulations to ensure correct operation and fault detection under typical operating condition.

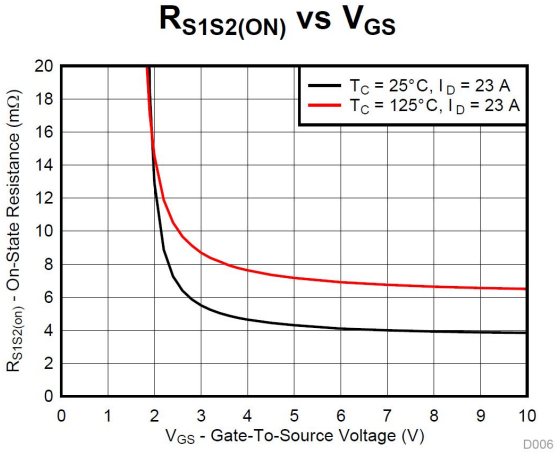


Figure 2.6: $R_{DS_{ON}}$ vs V_{GS} of CSD87313DMS [2]

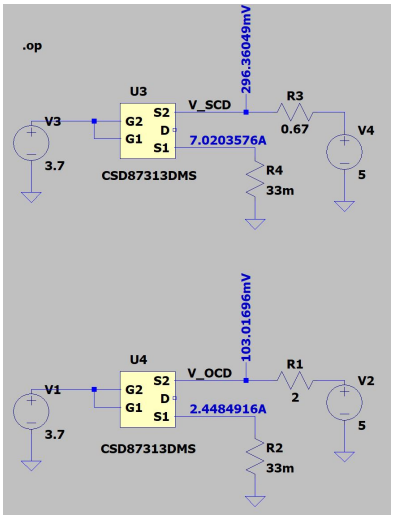


Figure 2.7: Overcurrent discharge and short circuit threshold [SCD, OCD] SPICE simulation

Charging circuit

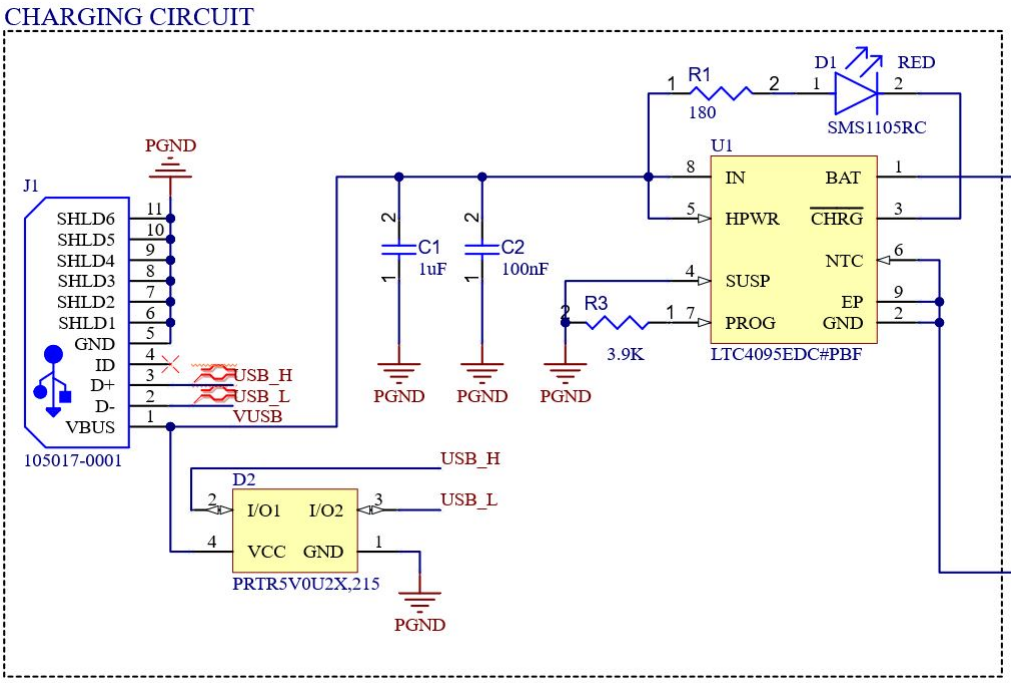


Figure 2.8: Battery charging circuit

The charging circuit is based on the LTC4095 [3], a standalone USB Li-Po battery charger. The schematic is fairly simple and includes:

- Micro-USB connector: it supplies the charging IC and provides USB communication to the Microcontroller,
- LED (D1) to indicate the state of the charging process
- ESD protection for USB differential pair lines (PRTR5V0U2X) [4]
- Bypass capacitance for USB supply

The LTC4095 is a constant current/voltage charger that implements multiple strategies to guarantee correct and safe battery charging:

- Bad battery detection: when a defective / unresponsive battery is connected
- Automatic recharge: in case of battery self-discharge after the device has been on charge for a long time.

- Low battery trickle charge: if the battery is significantly discharged, the current is reduced to 10% of its full scale value (20mA), until it reaches a safe condition.

The charging current can be programmed by setting the resistor R3, a general rule of thumb to safely charge Li-Po batteries is to set the current at around 1C, equivalent to a total charging time of 1 hour. For this design, a current of 200 mA was selected, and from [3] :

$$R_3 \approx 800V/I_{CHG} = 800V/200mA = 4k\Omega \Rightarrow R_3 = 3.9k\Omega \tag{2.2}$$

2.3 High-Voltage Pulse Generator

High-Voltage transformer

The most distinctive component used in this project is a very small, high turn-ratio ($n = 75$), high-voltage transformer. Unfortunately, the biggest drawback of such a device is the lack of documentation, and some important parameters like the primary winding magnetizing inductance, were unknown. Nevertheless, a characterization of the primary winding was performed by building a simple RLC series circuit, where L is the primary winding, C is an arbitrary capacitance, and R is chosen so that the function generator can provide the necessary current in all cases.

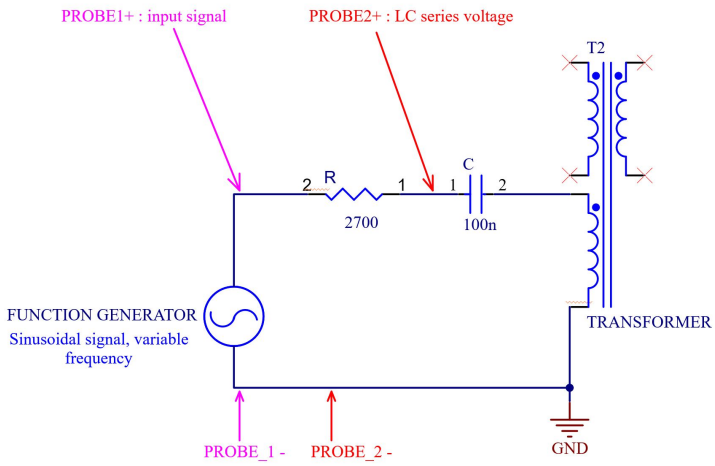


Figure 2.9: Primary measurement schematic

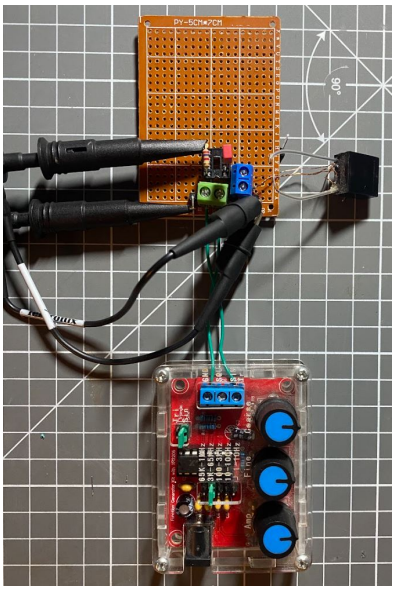


Figure 2.10: Measurement circuit realized on a proto-board

By manually sweeping the signal generator frequency, it was possible to evaluate the resonance frequency of the circuit. Indeed, at the resonance frequency, the impedance of the inductor and the capacitor cancel each other out, resulting in an almost zero-flat signal on PROBE2.

$$F_{RES} \approx 75KHz \tag{2.3}$$

$$F_{RES} = \frac{1}{2\pi\sqrt{L_1 C}} \Rightarrow L_1 = \frac{1}{(2\pi F_{RES})^2 * C} = \frac{1}{(2\pi * 75KHz)^2 * 100nF} = 45uH \quad (2.4)$$

Since the turn ratio is known ($n = 75$) , it's easy to determine the secondary winding inductance :

$$L_2 = n^2 * L_1 = 75^2 * 45uH \approx 250mH \quad (2.5)$$

Switching circuit

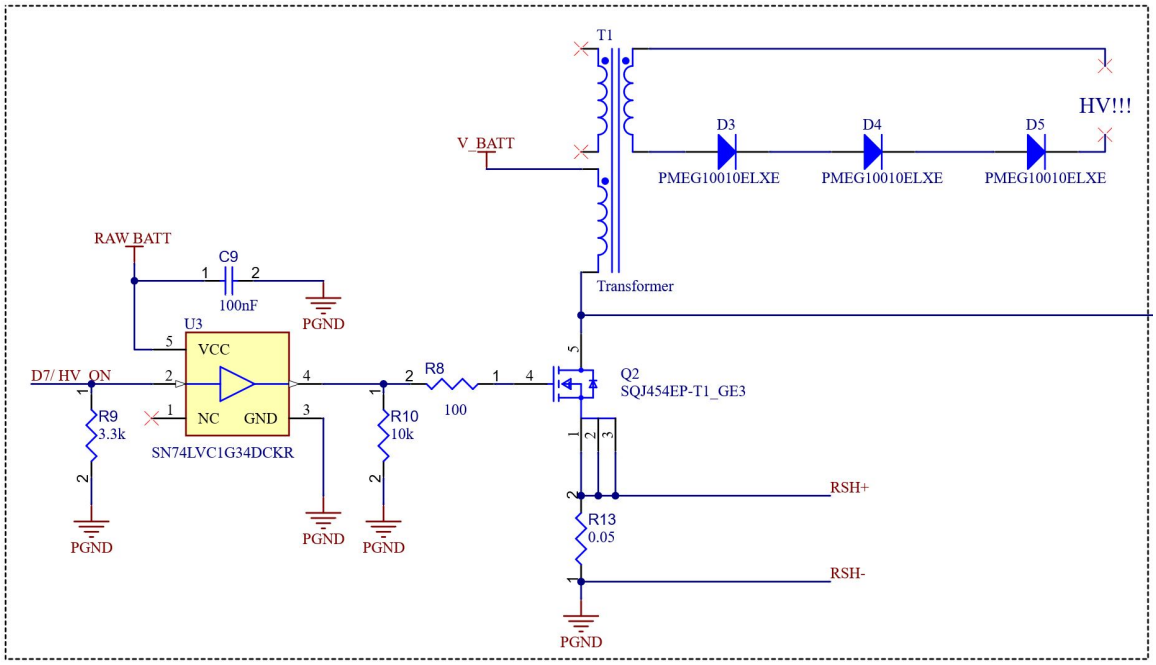


Figure 2.11: Pulse Generator / Switching Circuit Schematic

The circuit includes:

- Current buffer (U3 - SN74LVC [5]): The maximum output current that can be sourced from the GPIO pins of the microcontroller is 8 mA, the purpose of this buffer is to boost it up to ≈30 mA and work as a gate driver for the power transistor.
- HV transformer: already discussed in the previous section
- Power Switch (Q2 - SQJ45EP [6]): An automotive N-channel, 200V Vds , 13A power MOSFET. This transistor needs to sustain high currents and significant voltage spikes at the Drain terminal. For these reasons, it's also essential to have good power dissipation

characteristics and low thermal impedance: the PowerPAK® package definitely accomplishes this. Further considerations to ensure good power dissipation will be addressed in the PCB layout section.

- Diodes (D3-D5 - PMEG1001 [7]): they guarantee the correct direction of power flow at the secondary winding.

The gate of the MOSFET is driven by a PWM signal. Consequently, the operation of this circuit can be analyzed and divided in two main phases. In order to simplify the analysis, ideal components and no load (secondary winding OPEN) will be initially considered:

1. SWITCH-ON PHASE: When the switch is ON, the voltage across the primary winding L_1 is equal to V_{BATT}. By applying a constant voltage to L_1, the inductor current increases linearly, with a slope proportional to V_{BATT}:

$$i_{L1}(t) = \frac{V_{BATT}}{L_1} * t \tag{2.6}$$

$$I_{L1_{PEAK}} = \frac{V_{BATT}}{L_1} * t_{ON} \tag{2.7}$$

2. SWITCH-OFF PHASE: When the gate voltage drops below $V_{GS_{TH}}$, the mosfet turns off and the inductor current abruptly drops to zero. According to Faraday's law of induction, known more commonly as fundamental inductance law, a voltage spike proportional to the derivative of the Inductor's current is produced:

$$v_{L1}(t) = L_1 * \frac{di_{L1}(t)}{dt} \tag{2.8}$$

It's also reasonable to make a further simplification by considering a constant switch-off time for the mosfet $T_{SW_{OFF}}$. Thanks to this information the value of the voltage peak can be evaluated as:

$$\frac{di_{L1}(t)}{dt} = -\frac{I_{L1_{PEAK}}}{T_{SW_{OFF}}} \tag{2.9}$$

$$V_{L1_{PEAK}} = L_1 * -\frac{I_{L1_{PEAK}}}{T_{SW_{OFF}}} \tag{2.10}$$

$$V_{L1_{PEAK}} = L_1 * -\frac{\frac{V_{BATT}}{L_1} * t_{ON}}{T_{SW_{OFF}}} \tag{2.11}$$

$$V_{L1_{PEAK}} = -\frac{V_{BATT}}{T_{SW_{OFF}} * F_{SWITCHING}} * \delta \tag{2.12}$$

Equation (2.12) is the very important, since it expresses the mathematical relation between the voltage peak amplitude generated at the primary winding ($V_{L1_{PEAK}}$) and the duty cycle δ. Obviously, the secondary winding voltage (OUTPUT VOLTAGE) is equal to $V_{L1_{PEAK}} * n$, and can reach significant and possibly dangerous values.

Let's now consider the case of a RESISTIVE LOAD R_{LOAD}, connected at the output (secondary winding). The circuit analysis changes:

1. SWITCH-ON PHASE: Unchanged, thanks to the diodes in series with the load at the secondary, which are inversely polarized.

2. SWITCH-OFF PHASE: The effects of the output load can be transferred to the primary side by adding a resistor in parallel with L_1. To preserve the equivalence with the initial circuit, the load resistor needs to be scaled down by a factor of $n^2 = 75^2$.

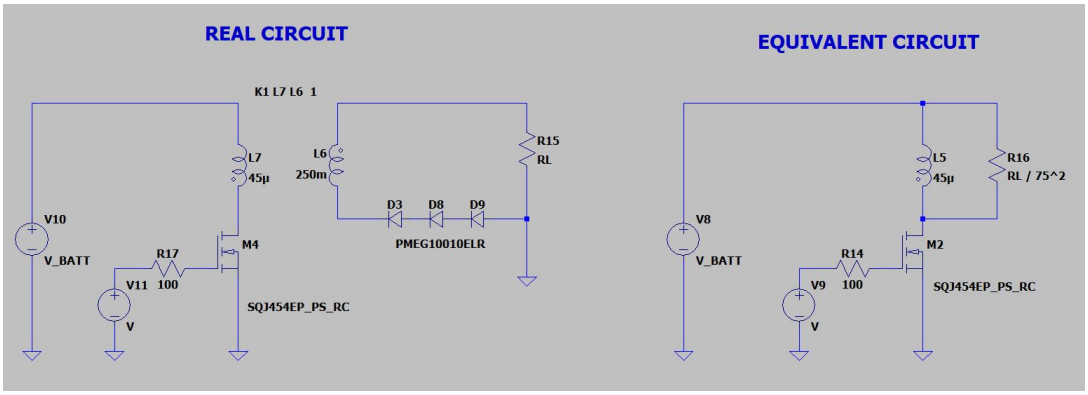


Figure 2.12: Switching schematic simplification for circuit analysis

At this point, two scenarios should be taken into account:

- **HEAVY LOAD** [$R_{LOAD} < 100K\Omega$]: The value of $\frac{R_{LOAD}}{n^2}$ is fairly small, and after the MOSFET switch-off, most of the current circulates into the loop formed by the primary winding inductance and the equivalent load resistance [Figure (2.13)], generating a voltage peak of:

$$V_{L1_{PEAK}} = -\frac{R_{LOAD}}{n^2} * I_{L1_{PEAK}} = -\frac{R_{LOAD}}{n^2} * \frac{V_{BATT}}{L_1} * t_{ON} \tag{2.13}$$

$$V_{L1_{PEAK}} = -\frac{R_{LOAD}}{n^2} * \frac{V_{BATT}}{L_1 * F_{SWITCHING}} * \delta \tag{2.14}$$

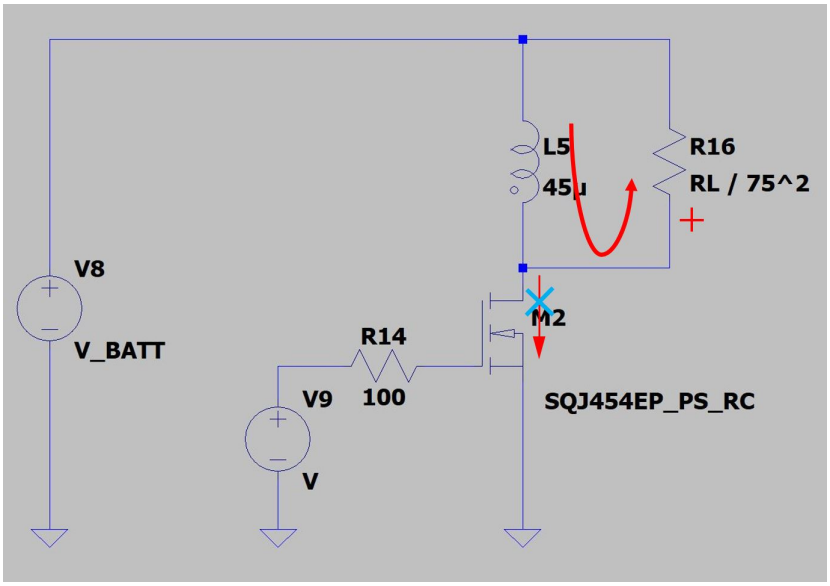


Figure 2.13: TRANSIENT current path in the case of heavy load

Unlike the open load case where the MOSFET was abruptly cutting off all the drain current, causing a very high $\frac{di_{L1}(t)}{dt}$, now the current has an alternative resistive path to flow into. As a result, a typical R-L series circuit loop is formed, where the inductor (initially charged) discharges through R, generating a negative exponential decay in the primary winding voltage (and current) profile after the initial peak produced according to equation (2.14).
It should be very intuitive that the smaller the load resistance, the better approximation this model provides.

- **LIGHT LOAD** [$R_{LOAD} > 100K\Omega$]: The analysis of the circuit when a light load is connected, for example $500K\Omega$, represents a hybrid situation that includes both effects discussed previously: part of the primary current circulates into the $L_1 - R_{LOAD_{EQ}}$ loop, the other part is cut off by the power switch.
It's very challenging to quantify correctly the voltage peak produced in this situation, but a possible solution is to determine a value of R_{LOAD} above which the OPEN-LOAD model is considered valid, and below which the HEAVY-LOAD applies. Simulation tools like LTSPICE can help to identify this special value for R_{LOAD}.

Snubber circuit

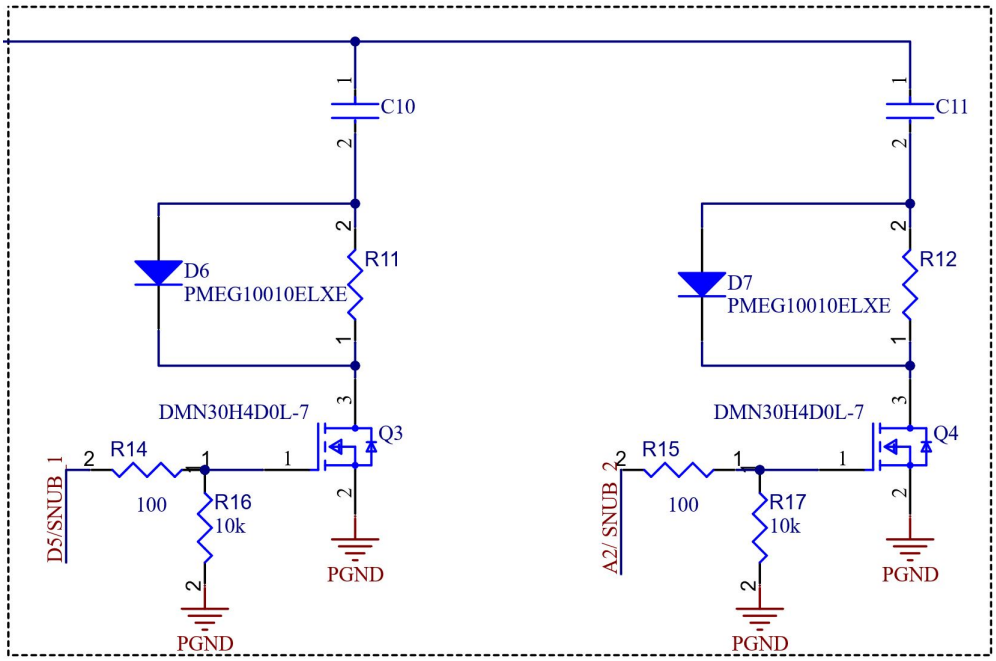


Figure 2.14: Snubber circuits

Since the value of the primary winding inductance is quite low, the current slope tends to be high. As will be seen in simulations, even with very small values of t_{ON}, the output voltage ($V_{L1_{PEAK}} * n^2$) can reach substantial values in OPEN LOAD condition. This phenomenon makes it very hard to accurately regulate the output for lower output voltages, considering that even increasing t_{ON} by a couple of microsecond will be translated into an output voltage step of hundreds of volts.

To provide an additional degree of accuracy and increase resolution for ”lower” output voltages (< 500V), two independent snubber circuits were designed. Either one of these circuits (or neither) can be activated using one of the ENABLE signal that control the gate of Q3 or Q4.

Both circuits are connected to the drain of the power MOSFET, and they both ”see” the voltage pulse produced by the primary winding right after the switch off. Let’s assume D5/SNUB1 is activated. Since the current in a capacitor is proportional to the derivative of the voltage, most of the switch-off drain current flows into C10 through D6 and Q3. As C10 now stores some energy, it must be discharged before the following voltage peak, through R11.

The problem can be analyzed more precisely by applying the principle of conservation of energy. In fact, in the case of an ideal switch and OPEN LOAD, the energy stored in the inductor during t_{ON} is transferred to the capacitor and then released before the next voltage peak.

$$E_{L1} = \frac{1}{2} * I_{L1_{PEAK}}^2 * L_1 = \frac{1}{2} * {V_{C_{PEAK}}}^2 * C = E_C \tag{2.15}$$

$$V_{C_{PEAK}} = I_{L1_{PEAK}} \sqrt{\frac{L_1}{C}} \tag{2.16}$$

$$V_{C_{PEAK}} = \frac{V_{BATT}}{L_1} \sqrt{\frac{L_1}{C}} * t_{ON} = \frac{V_{BATT}}{F_{SWITCHING} \sqrt{L_1 C}} * \delta \tag{2.17}$$

$$V_{L1_{PEAK}} = V_{BATT} - (V_{D6} + V_{C_{PEAK}}) \tag{2.18}$$

Equation (2.17) shows that by choosing a large capacitor, the voltage pulse amplitude generated decreases for the same δ, obtaining the desired output resolution increase.

Having two optional snubber circuits provides the system with two more degrees of freedom in terms of resolution, which can be set according to the application.

The value of the capacitors will be refined thanks to simulations, but initial values will be set at 47nF and 330nF. Care must be taken when choosing these capacitors as well as Q3 and Q4 [8], because they need to withstand voltage spikes up to 200V.

The resistor in parallel with the capacitor must be chosen so that the RC time constant is approximately $\frac{1}{2}$ or $\frac{1}{3}$ of the switching period, ensuring full capacitor discharge.

2.3.1 SPICE Simulation

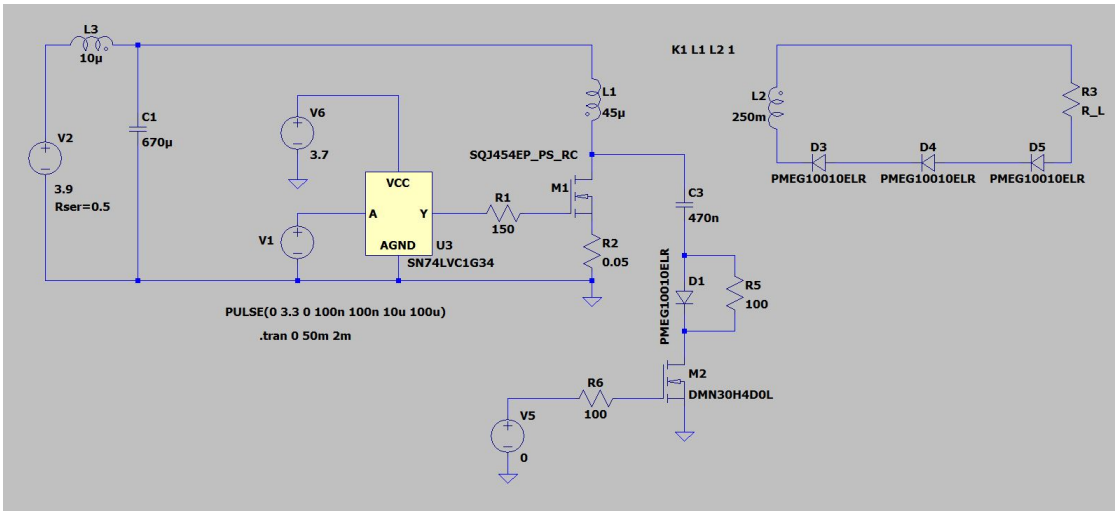


Figure 2.15: LTSPICE simulation schematic

Several simulations were performed but only the most relevant ones will be included in this document. The circuit was tested in the three different output load situations previously discussed.

- OPEN LOAD: $R_L = \infty$
- LIGHT LOAD: $R_L = 500K$
- HEAVY LOAD: $R_L = 50K$

In order to compare the simulation results, the control signals and the circuit parameters were kept constant except for the load. By performing the calculations from the analytical model found in previous sections, we can predict the value of the primary output voltage peak.

Using equation (2.12), for OPEN LOAD we expect:

$$V_{L1_{PEAK}} = -\frac{V_{BATT}}{T_{SW_{OFF}} * F_{SWITCHING}} * \delta = -\frac{3.9V}{300ns * 10KHz} * 0.1 = -130V \tag{2.19}$$

Using equation (2.14) for HEAVY LOAD we expect:

$$V_{L1_{PEAK}} = -\frac{R_{LOAD}V_{BATT}}{n^2 L_1 F_{SWITCHING}} * \delta = -\frac{50K\Omega * 3.9V}{75^2 * 45\mu H * 10KHz} * 0.1 = -7.7V \tag{2.20}$$

Afterwards, in the OPEN LOAD condition, the SNUBBER circuits were activated:

- SNUBBER CIRCUIT 1: $(R = 180\Omega, C = 47nF)$
- SNUBBER CIRCUIT 2: $(R = 100\Omega, C = 330nF)$

Using equations (2.17) and (2.18) we can estimate the value of the primary voltage peak when SNUBBER CIRCUIT 1 is activated: (the same applies to SNUBBER CIRCUIT 2).

$$V_{C_{PEAK}} = \frac{V_{BATT}}{F_{SWITCHING}\sqrt{L_1 C}} * \delta = \frac{3.9V}{10KHz\sqrt{45\mu H * 47nF}} * 0.1 = 26.8V \tag{2.21}$$

$$V_{L1_{PEAK}} = V_{BATT} - (V_{D6} + V_{C_{PEAK}}) = 3.9V - (0.6V + 26.8V) = -23.5V \tag{2.22}$$

ALL The results obtained analytically are consistent with the simulations
Finally, to ensure a correct operation of the snubber circuit, the current and the voltage of the snubber capacitor were plotted.

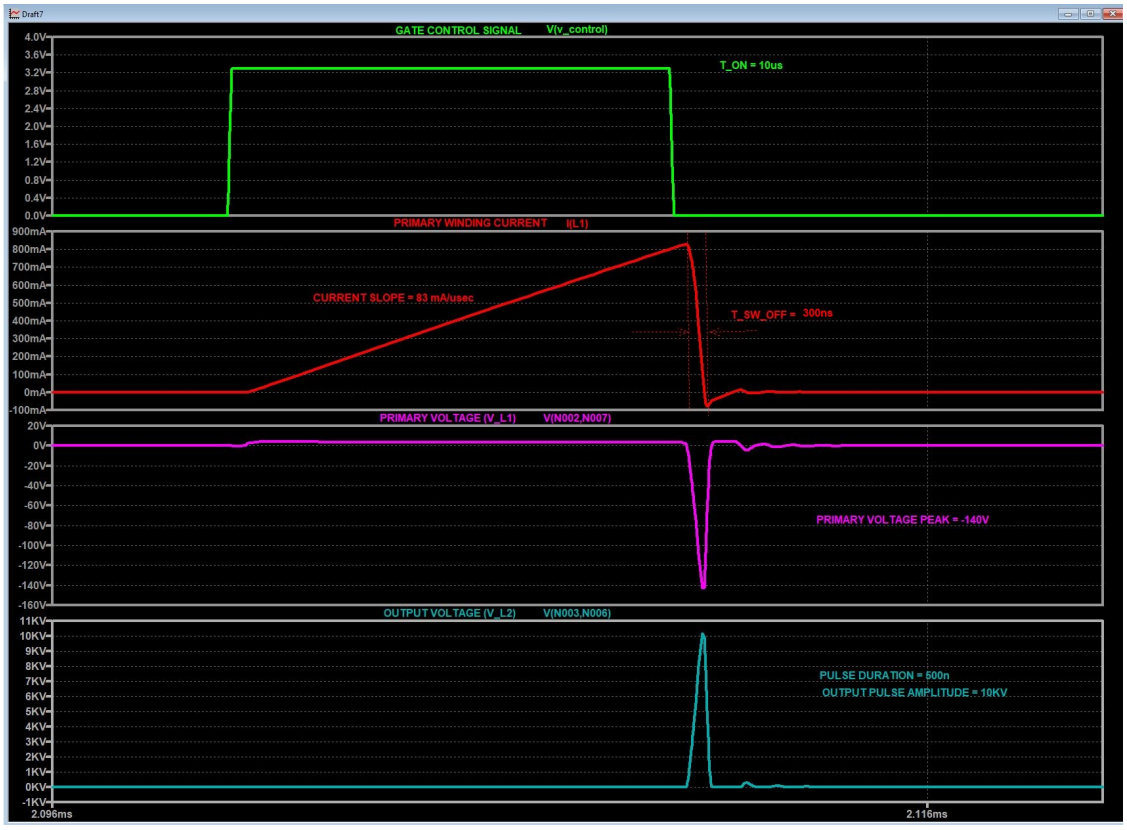


Figure 2.16: OPEN LOAD SIMULATION

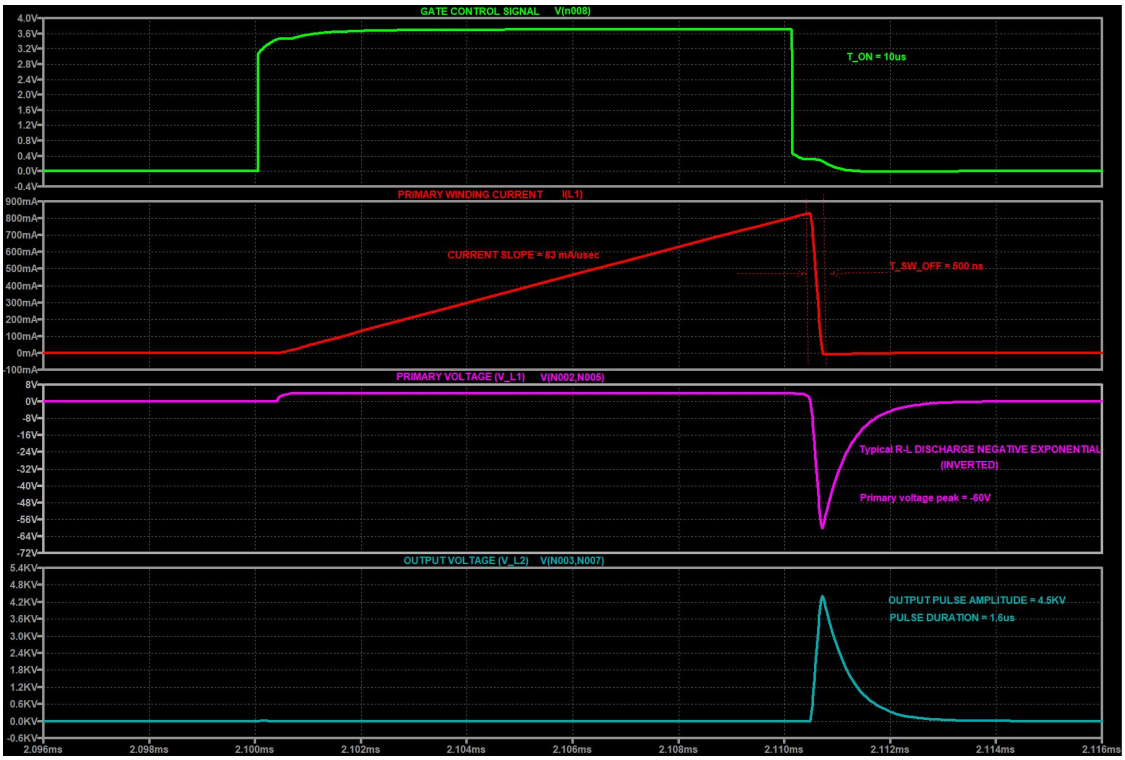


Figure 2.17: LIGHT LOAD SIMULATION

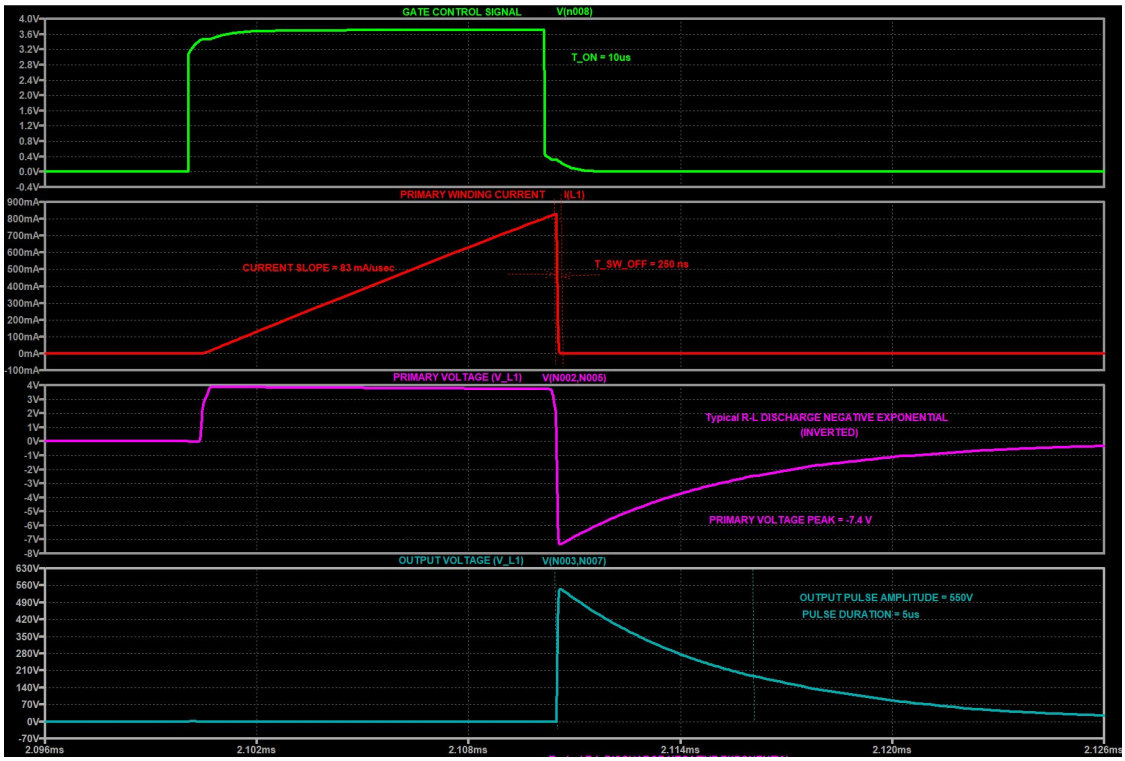


Figure 2.18: HEAVY LOAD SIMULATION

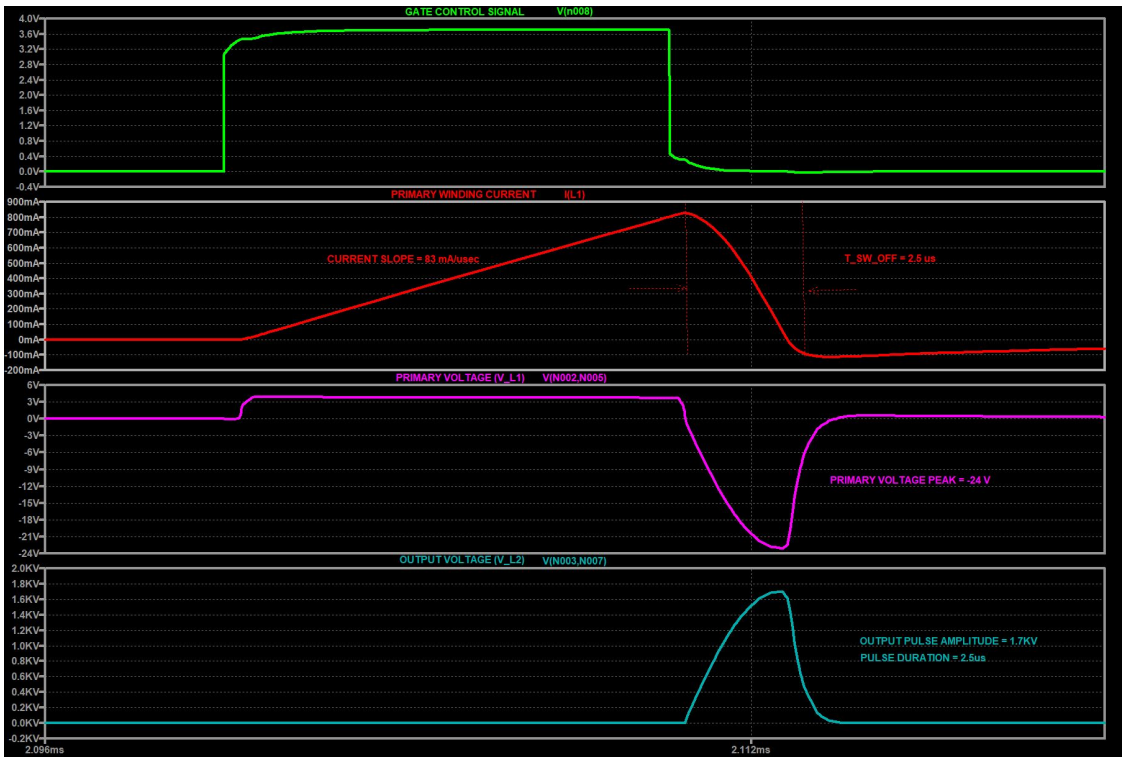


Figure 2.19: SNUBBER CIRCUIT 1: ACTIVATED - SIMULATION

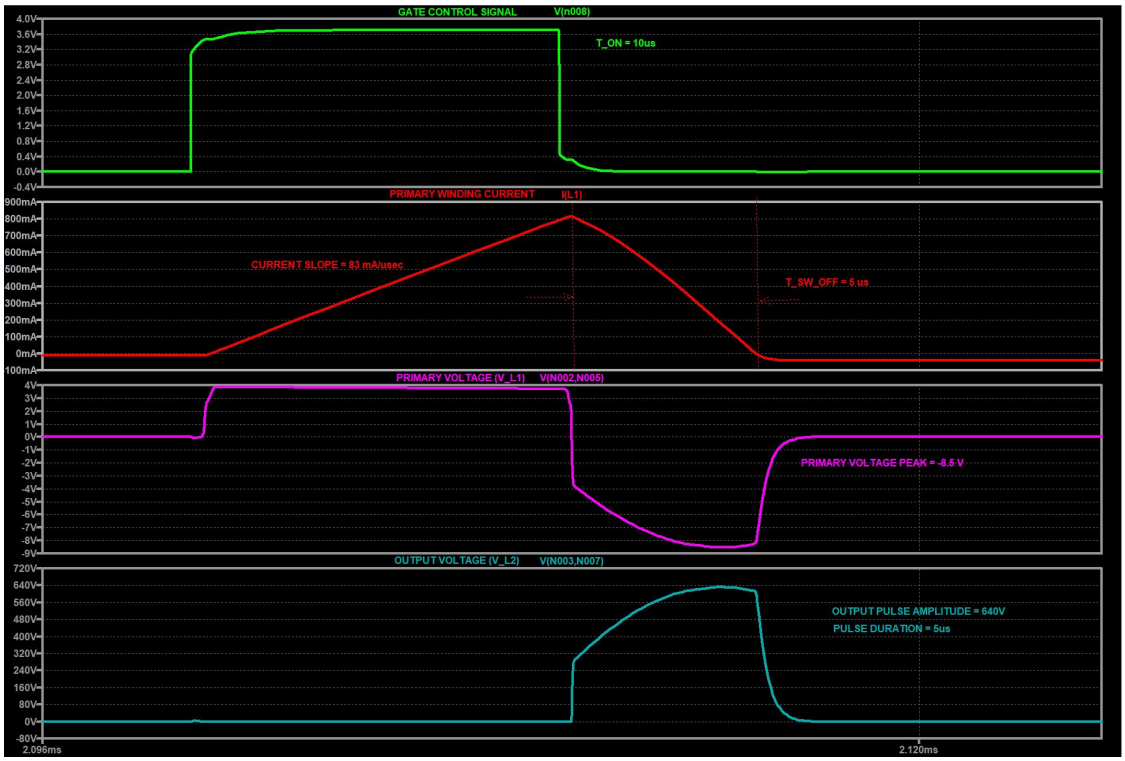


Figure 2.20: SNUBBER CIRCUIT 2: ACTIVATED - SIMULATION

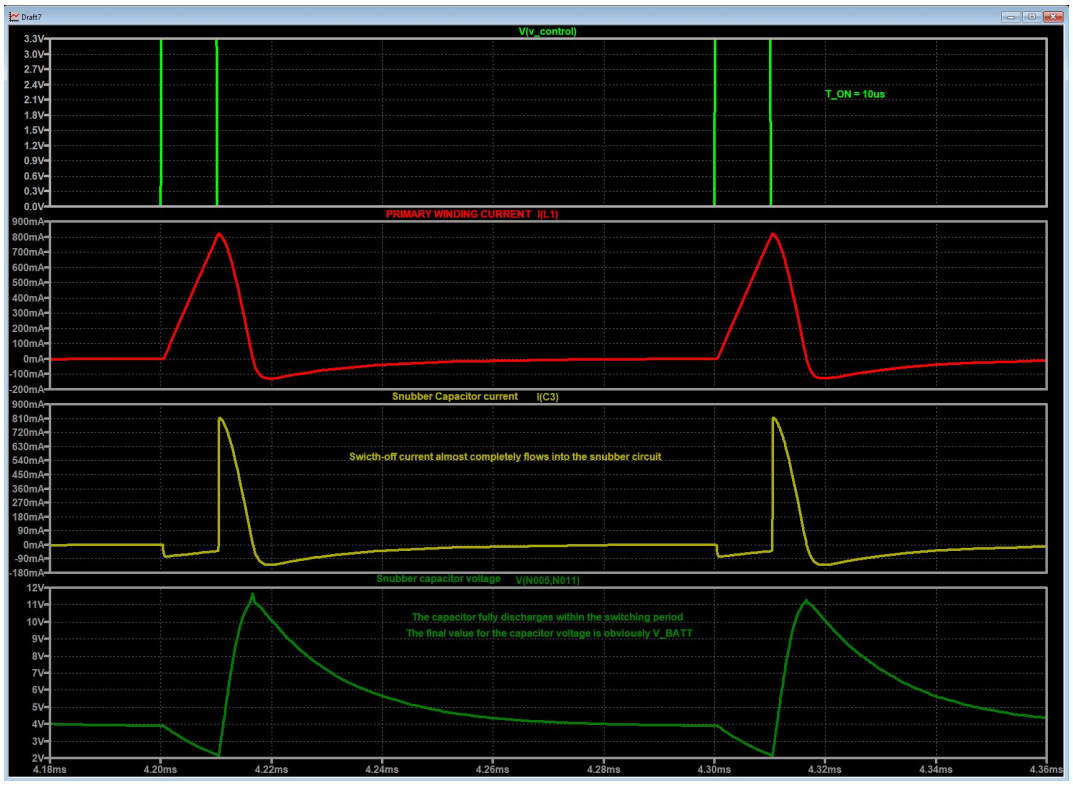


Figure 2.21: SNUBBER CIRCUIT 2: CAPACITOR CURRENT AND VOLTAGE PLOT

2.4 LC Filter design

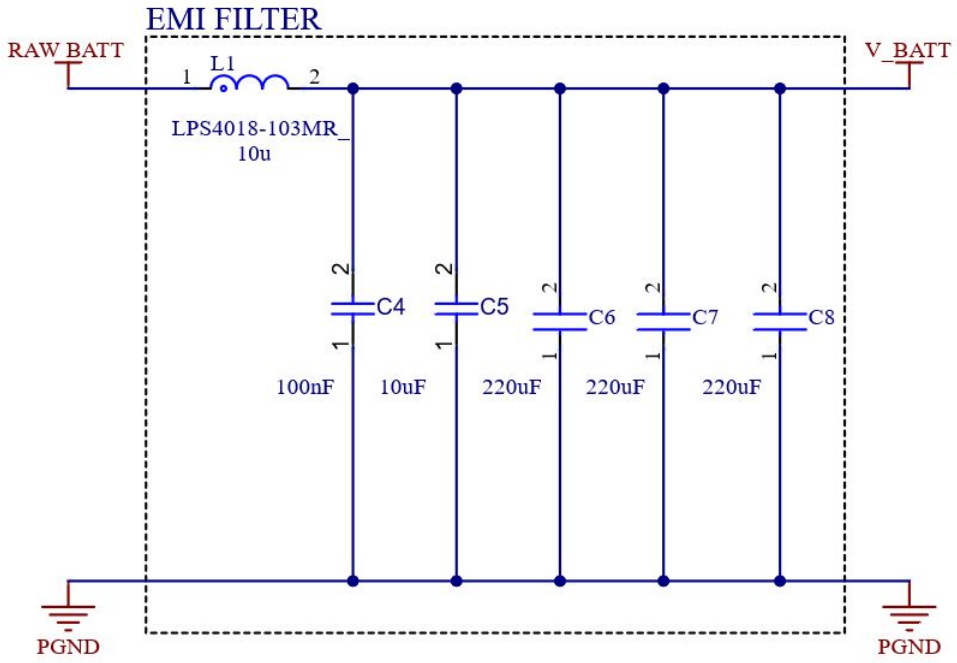


Figure 2.22: LC filter schematic

The main challenge for the design of this filter is the component selection, that needs to focus on small footprint components to facilitate their integration. As previously discussed, the operating fundamental frequency of the switching circuit is 10 KHz, the purpose of this filter is to eliminate the higher harmonic components of the primary winding current, that could reach harmful peaks for the battery.

In the ideal case of a perfect attenuation of all the AC harmonics, the battery would need to source only the average primary current over the switching period (DC component), but unfortunately this is not possible in reality.

The components selected for this design are : a 10 uH inductor [9], and the parallel of three 220μF ceramic capacitors [10].

An example of the spectrum of the primary winding current signal to be filtered is plotted in Figure 2.23: as expected, the fundamental frequency (10 KHz) is the largest harmonic component of the spectrum, while the other harmonics, located at integer multiples of the fundamental, decay significantly in magnitude.

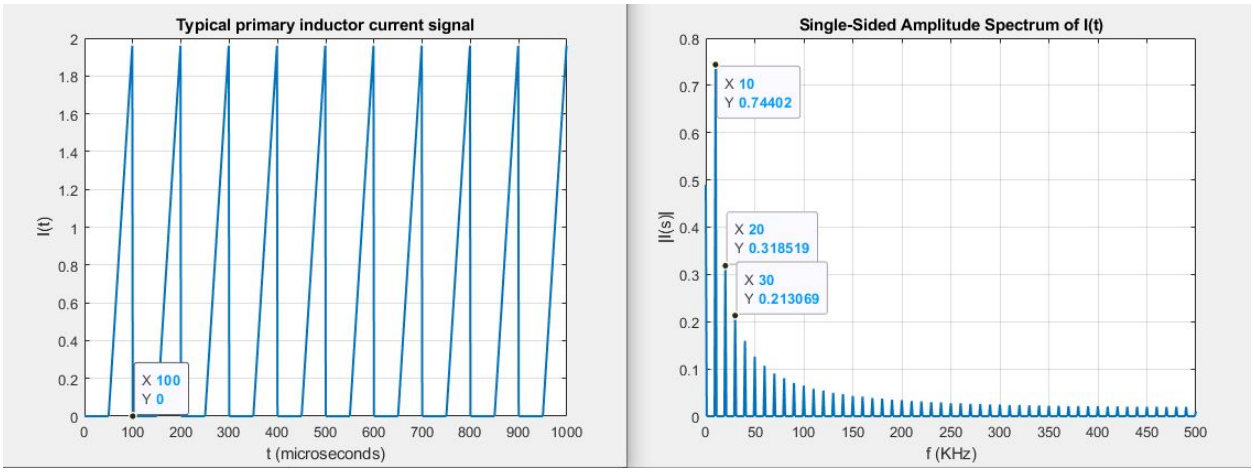


Figure 2.23: Spectrum of the primary winding current

The transfer function of a simple RLC circuit is:

$$G(s) = \frac{1}{1 + sR_LC + s^2LC} \tag{2.23}$$

Where R_L is the inductor parasitic series resistance, in this case 200mΩ. By comparing this equation with the general transfer function of a second order system, it's possible to derive the characteristic parameters of this circuit:

$$H_{2^{nd}_{order}}(s) = \frac{1}{1 + s\frac{2\xi}{\omega_n} + s^2\frac{1}{\omega_n^2}} \tag{2.24}$$

$$\omega_n = \sqrt{\frac{1}{LC}} = \sqrt{\frac{1}{10\mu H * 670\mu F}} = 12.2Krad/s \;\Rightarrow\; f_{cutoff} = \frac{\omega_n}{2\pi} = 1.9KHz \tag{2.25}$$

$$\xi = \frac{R_LC\omega_n}{2} = \frac{200m\Omega * 670\mu F * 12.2Krad/s}{2} = 0.81 \tag{2.26}$$

Observations:

- The filter cut-off frequency is lower than the switching frequency (10 KHz), but still *only* 5 times smaller. Anyways, a further reduction of the cutoff frequency would result in a considerable increase in the components size, which would be prohibitive for this application.

- A possible issue concerning the use of a simple LC filter resides in the resonance frequency peak in the transfer function. Fortunately, the inductor series resistance R_L increases the damping ratio ξ to a value of $0.81 > \frac{\sqrt{2}}{2}$, resulting in a system without a resonance peak.

- The battery output series resistance should also be considered in this circuit, but since it would only improve the system in terms of stability, a worst case scenario is taken into account, neglecting it.

The BODE plot of the filter transfer function was realized using SPICE. The simulation matched the theoretical results, and the attenuation value at the switching frequency is around -28 dB, which is reasonable.

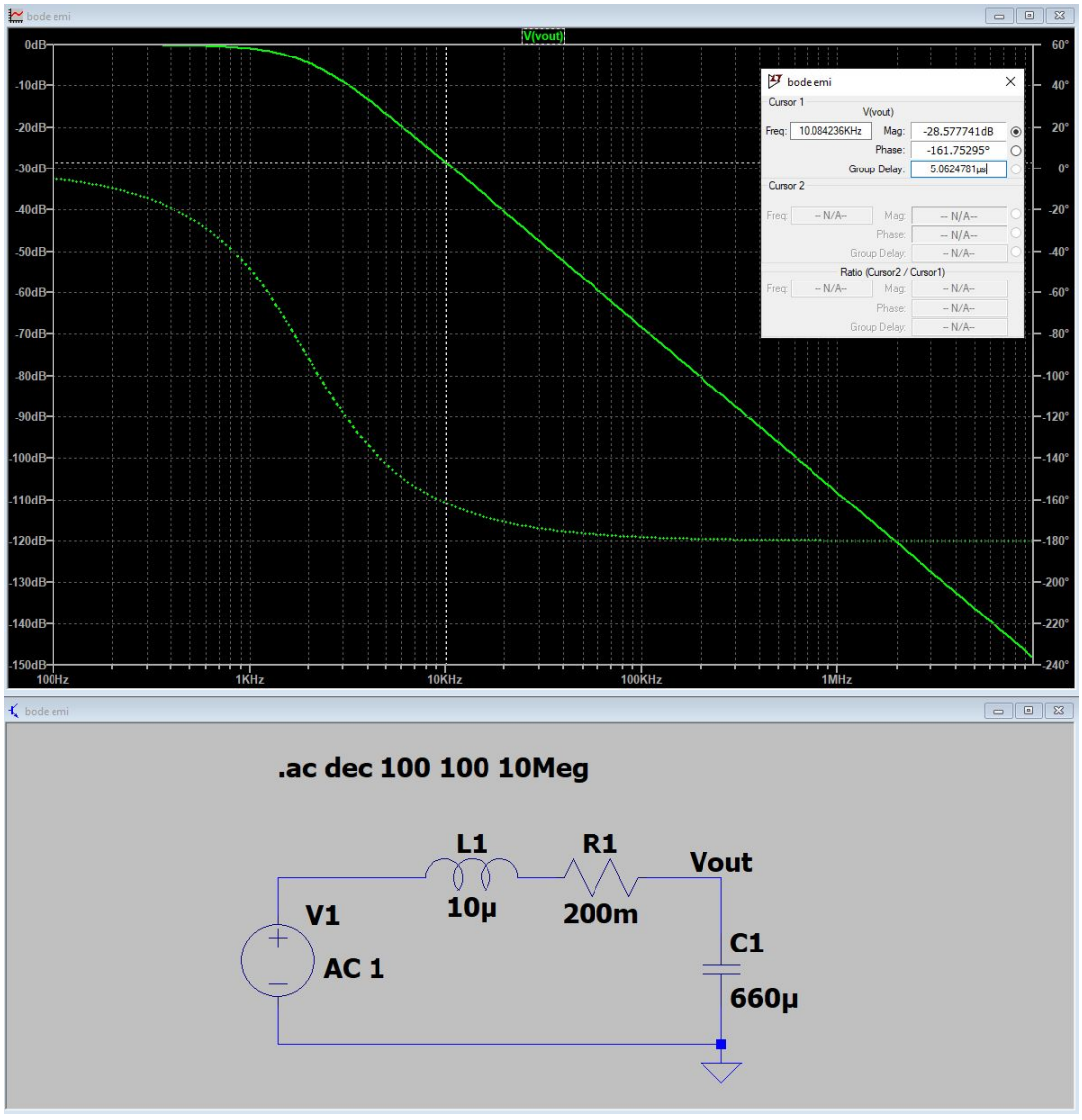


Figure 2.24: LC filter SPICE simulation

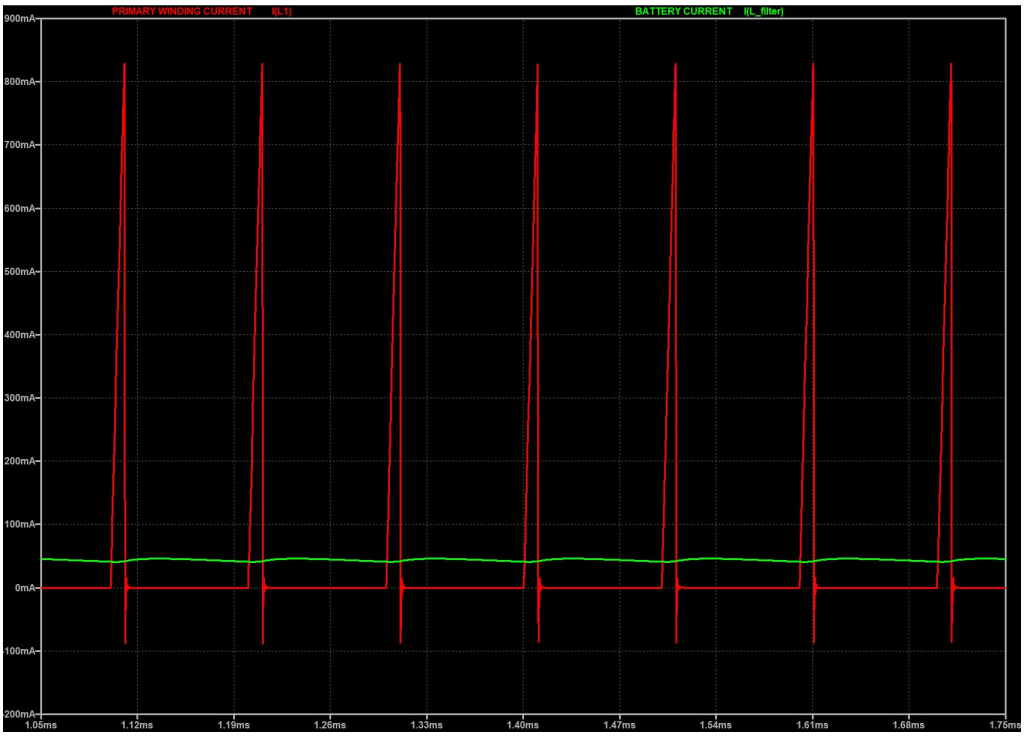
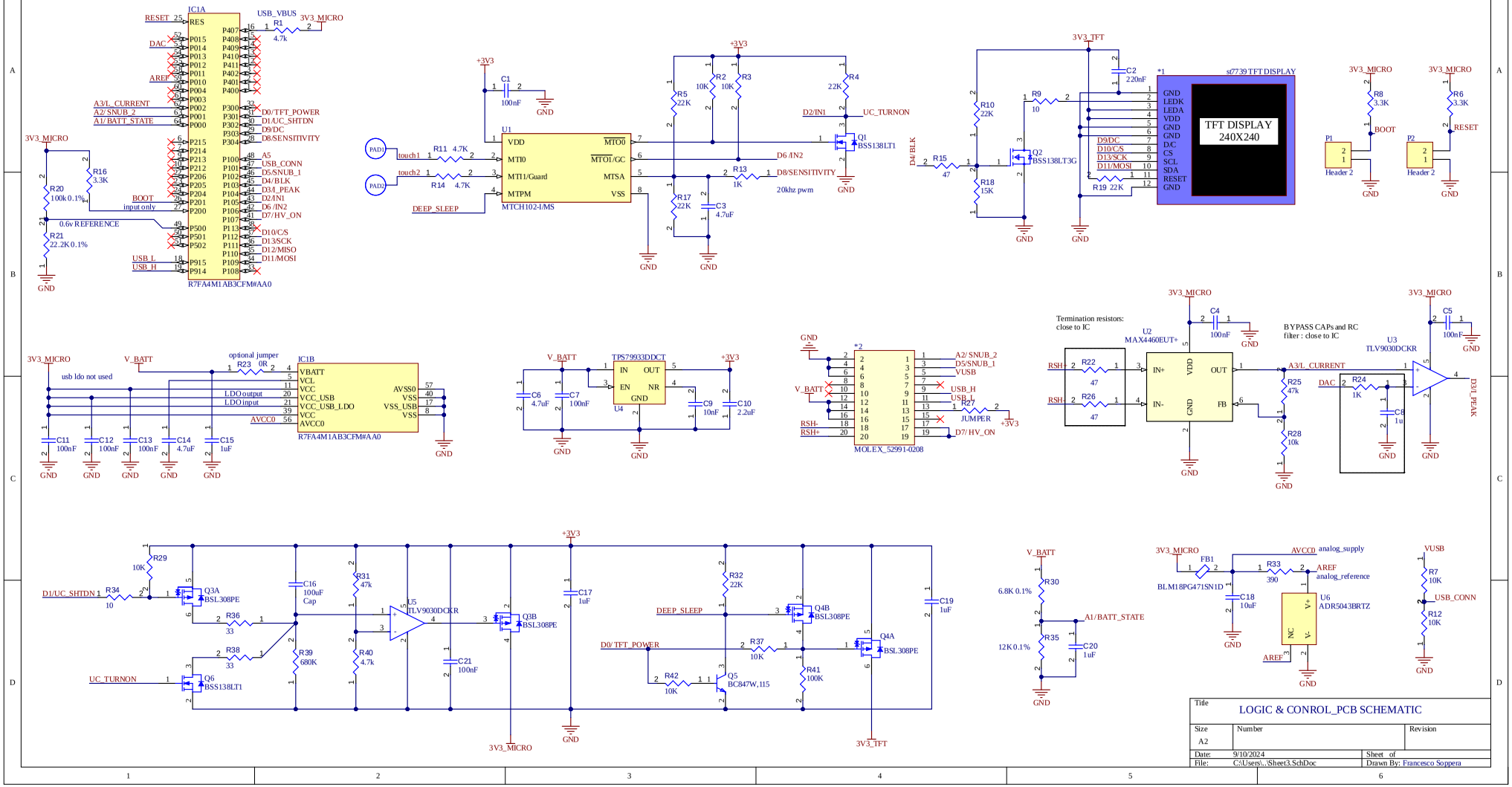


Figure 2.25: LC filter effects: SWITCHING CURRENT vs BATTERY CURRENT


IC1A
R7FA4M1AB3CFM#AA0
MTCH102-I/MS
TFT DISPLAY
240X240
st7739 TFT DISPLAY
IC1B
R7FA4M1AB3CFM#AA0
TPS79933DDCT
MOLEX_52991-0208
MAX4460EUT+
TLV9030DCKR
ADR5043BRTZ
BSL308PE
BSS138LT1
BC847W,115
LOGIC & CONROL_PCB SCHEMATIC
Size A2
Number
Revision
Date: 9/10/2024
Sheet of
File: C:\Users\..\Sheet3.SchDoc
Drawn By: Francesco Soppera

Chapter 3

LOGIC AND CONTROL PCB

In this chapter the schematic of the LOGIC&CONTROL PCB will be described. The full schematic is available in the previous page.

3.1 Microcontroller

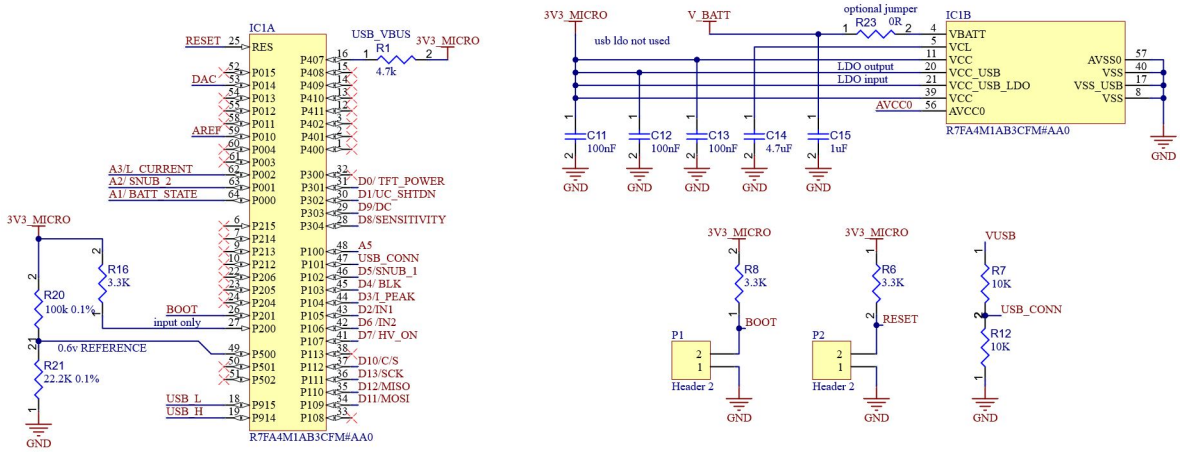


Figure 3.1: Microcontroller schematic

The microcontroller chosen for this application is the R7FA4M1AB3CFM from Renesas: [11], a 32 bit, 48 MHz, Arm Cortex-M4 microcontroller. The most relevant features are:

- CONNECTIVITY: A number of communication protocols modules are natively built-in: UART, I2C, SPI, CAN and USB 2.0 FULL SPEED.
- High resolution ANALOG-TO-DIGITAL CONVERTER: [14 bit resolution]
- High resolution DIGITAL-TO-ANALOG CONVERTER: [12 bit resolution]

- OPERATING VOLTAGE 1.6 to 5.5 V: compatible with this design [3.3V]
- LOW POWER MODE: to achieve longer battery life

All the supply (VCC) pins should be bypassed to ground by 100 nF capacitors with the exception of C14, the 4.7 uF capacitor used to stabilize the internal power supply at the VCL pin. The BOOT and RESET pins are crucial for the microcontroller programming during the initial test and debug phase, they must be reachable and need to be easily grounded when needed. The VBAT supply pin can be used to supply the internal RTC, to keep track of time even when the device is turned off, R23 acts as a jumper to enable this option. An additional input monitors the presence of USB connection, adapted by a simple voltage divider (R7,R12). The following table summarizes the input/outputs and their function:

PIN	NAME	TYPE	FUNCTION
P000	BATT_STATE	Analog IN	Battery voltage
P001	SNUB_2	Digital OUT	Snubber circuit 2 ENABLE
P002	L_CURRENT	Analog IN	Primary winding current
P014	DAC	Analog OUT	Peak current value set
P101	USB_CONN	Digital IN	Usb connection detection
P102	SNUB_1	Digital OUT	Snubber circuit 1 ENABLE
P103	LCD_BLK	PWM OUT	Display luminosity
P104	I_PEAK	Digital IN	Interrupt pin, peak current reached
P105	IN1	Digital IN	Touch input 1
P106	IN2	Digital IN	Touch input 2
P107	HV_ON	PWM OUT	Driver signal for power switch
P109	TFT C/S	SPI	TFT display SPI chip select
P110	TFT SCK	SPI	TFT display SPI clock
P111	TFT MISO	SPI	TFT display MISO
P112	TFT MOSI	SPI	TFT display MOSI
P301	TFT_POWER	Digital OUT	TFT supply enable
P302	UC_SHTDN	Digital OUT	MICROCONTROLLER supply enable
P303	TFT DC	Digital OUT	TFT display DC
P304	SENSITIVITY	PWM OUT	TOUCH sensitivity set

3.2 Hardware user interface

Touch inputs

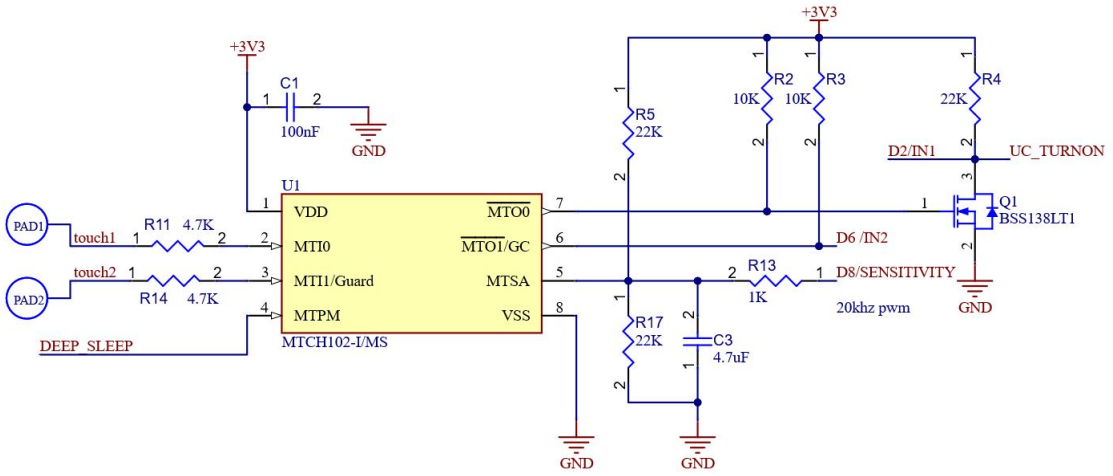


Figure 3.2: Touch inputs circuit

The touch inputs circuit is based on the MTCH102 [12] by Microchip, a 2-Channel capacitive Proximity/Touch controller. This IC has 2 open drain outputs (which need to be pulled up (R2,R3)) that are driven to zero (GND) when a change in capacitance is detected at the two touchpads connected at its inputs. The output MTO1 is directly fed into the Microcontroller , while the MTO0 is inverted (Q1,R4) for a reason that will be clear in next sections. The input MTPM sets the power mode for the device and is connected to a signal called DEEP_SLEEP coming from the power management circuit:

- If DEEP_SLEEP is HIGH, normal power mode is selected (continuous input scan)
- If DEEP_SLEEP is LOW, low power mode is activated (burst scan at 256 ms interval)

Touch sensitivity and/or proximity can be adjusted according to the voltage level presented at the MTSA pin. To control this value, two scenarios are possible:

- When the microcontroller is OFF (HIBERNATION), D8/SENSITIVITY is floating, and the value of MTSA is given by the voltage divider R5,R17 (to be adjusted during test and debug).
- When the microcontroller is ON, driving D8/SENSITIVITY with a PWM signal, generates an arbitrary value of sensitivity in the supply range by adjusting the duty cycle. Without getting into too many details for such a simple circuit, R13 AND C3 essentially

extract the average value of the input signal, acting as a very simple Digital to analog converter. In order for this circuit to work as intended, two main requirements need to be satisfied:

1. The PWM frequency of D8/SENSITIVITY is much higher than the cut-off frequency of the RC filter
2. R13 is much lower than R5,R17 (approximately 1/10). This condition reduces the influence of the voltage divider formed by R5 and R17, when D8/SENSITIVITY is driven by the PWM signal, allowing for a nearly rail to rail supply possible variation of the MTSA voltage. The minimum and maximum MTSA voltage can be evaluated by considering the extreme cases D8 = 3.3V (100% duty cycle) , D8 = 0 V (0% duty cycle). With the values in the circuit above we obtain:

$$f_{CUT-OFF} = \frac{1}{2 * \pi * RC} = 34Hz \quad \rightarrow f_{PWM} > 3kHz \tag{3.1}$$

Two decades spacing should guarantee decent filtering, ∼-40 dB attenuation of the first harmonic

$$MTSA_{MAX} = VDD * \frac{R17}{R5||R13 + R17} = 3.1625V \tag{3.2}$$

$$MTSA_{MIN} = VDD * \frac{R17||R13}{R5 + R13||R17} = 0.1375V \tag{3.3}$$

Display

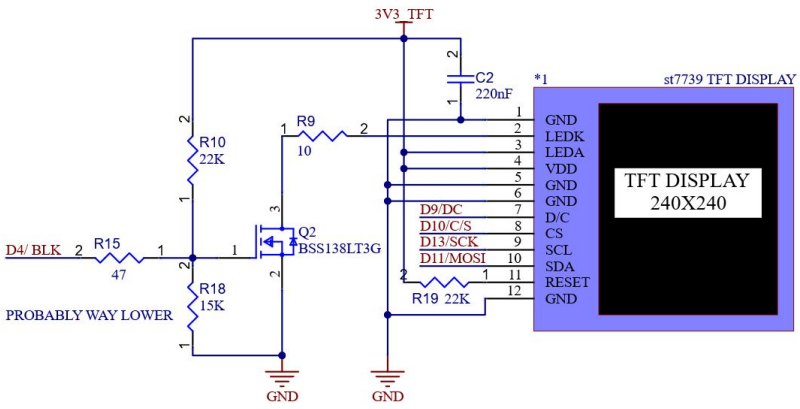


Figure 3.3: TFT Display schematic

Figure 3.4: LCD TFT 240x240 IPS display

The user interface is shown on a IPS LCD coloured TFT 1.3” display, 240 x 240 pixels. It communicates using SPI, and an open source library is available online for easy configuration and programming. The pin LEDK is the cathode of the LCD back-light LED and it regulates luminosity. Similarly as before, two scenarios are possible:

- When the microcontroller is OFF (HIBERNATION), D4/BLK is floating: in this situation the gate voltage of Q2 is given by the divider R10,R18. The overdrive voltage of Q2 determines the LCD back-light LED current, and this level will be adjusted during test and debug to find the optimal value to guarantee a good ALWAYS ON / STAND BY luminosity level as well as a limited power consumption.
- When the Microcontroller is ON, D4/BLK is driven by a PWM signal, allowing for a dynamic and configurable luminosity level.

3.3 Power Management

Main Power Supply

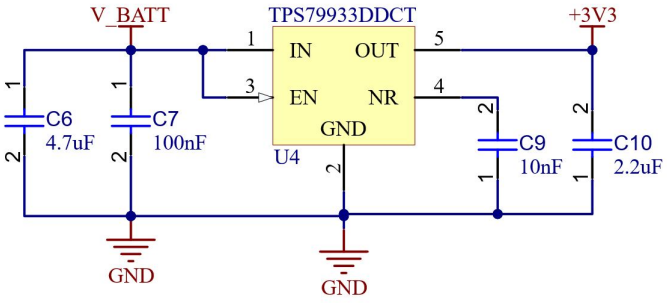


Figure 3.5: linear voltage regulator

The main supply of the LOGIC & CONTROL PCB is 3.3 V, and needs to be obtained starting from the battery voltage. In the general case, when an electronics designer needs to create a step down voltage conversion circuit, three main options should be considered:

- LINEAR REGULATOR: suited for applications where the output current is not significant (ex. <500 mA) and the dropout voltage (Vin-Vout) is generaly low.These requirements avoid unreasonable power dissipation on the regulator.
  The main drawback of this solution is the low efficiency, but if the power loss is low in absolute value, it can be accepted. The biggest advantage is the simplicity of the circuit,

the limited number of external components, the low cost, and the absence of EMI noise due to switching at high frequencies.

- DC-DC CONVERTER: suited for high power applications. These circuit can reach efficiencies of $\sim$90% and represent the only option when voltage isolation is a necessity, but they are usually pretty expensive, space demanding, and could generate unwanted noise at the operating switching frequency.

It should be clear by now that the linear regulator is the best option for this application. The expected maximum output current is around $80mA$, mainly drawn by the Microcontroller and the Display combined, while the maximum dropout voltage is about: $4.2 - 3.3 = 0.9V$, resulting in a maximum power dissipation on the regulator equal to: $80mA * 0.9V = 72mW$, which can be easily managed.
The component chosen for this purpose is the TPS79933 [13], a fixed 3.3V output voltage regulator from Texas Instruments. The maximum permissible output current is 200 mA (well above 80mA), and the typical dropout voltage is 100mV, this means that for input voltages greater or equal than 3.4V the circuit will operate as intended. A limited number of external components is required, in particular: the input/output decoupling capacitors and another capacitor at the NR pin to reduce output noise.
A possible issue could emerge when the battery voltage is close to the lower limit of 3.3V, at this point the output voltage will not be precisely 3.3V, and will follow the input with an error equal to the dropout voltage. This means that if, for example, the input voltage was 3.2V, the output would be equal to $3.2 - 100mV = 3.1V$. At this voltage both the Microcontroller and the display would still operate correctly but of course this situation should be avoided and immediately alert the user that the battery should be recharged as soon as possible.
Anyhow, a simulation was performed with $V_{IN} = 3.3V$, to check for any unexpected problems: the predicted behavior was confirmed and the resulting output was $3.19V$.

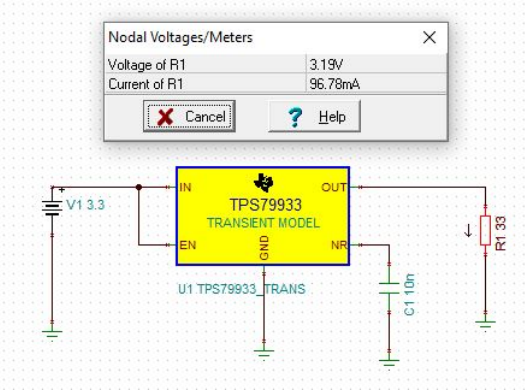


Figure 3.6: TPS79933 worst case scenario simulation, using TINA-TI tool

Power modes and Selective power shutdown

The device will have the following optional power modes, summarized and described in the next table:

POWER MODE	Microcontroller	Display	Consumption →Battery Life
ACTIVE	Fully operational	Always on	30+15= 45mA → ∼**6 h**
STANDBY	low power/sleep mode	Always on	10+9= 19mA → ∼**13 h**
SLEEP	low power/sleep mode	Normally off	10+0= 10mA → ∼**1 day**
WALKING-DEAD	Intermittent Power ON	Always on	1+9= 10mA → ∼**1 day**
HIBERNATION	Intermittent Power ON	Normally off	1+0= 1mA → ∼**11 days**

In all the possible power modes the device can be woken up easily and quickly by interacting with the touch inputs, this means that it will never be really ”OFF” unless the battery goes into under-voltage protection and cuts the whole supply to the circuit.

The main difference between STANDBY and WALKING-DEAD mode, as well as between SLEEP and HIBERNATION mode is the Microcontroller power management:

- **STANDBY, SLEEP**: the Microcontroller is always on and in a low power state, that allows it to absorb a fraction of the normal operational current. It immediately reacts to interrupts, and for this reason in order to wake it up it’s enough to tap the TOUCH1 pad and the device will be immediately ready-to-use.

- **WALKING-DEAD, HIBERNATION**: These power modes are less common, they were developed ad hoc to push the battery life of the device as much as possible.
  The general idea is to periodically turn on the device every 1 or 2 minutes, just for a few seconds to refresh the display and check the general state of the device (battery state, temperature...) and then turn it immediately off. By adopting this technique the average current absorbed by the Microcontroller is reduced to a fraction of a mA, and the maximum achievable battery life in HIBERNATION MODE can be more than 10 days.
  The only difference with the other case is the time delay of about 1.5 second needed to reach full operating condition after the TOUCH1 pad has been pressed. The reason behind this ”time lag” is simple: the Microcontroller needs about 1 second to turn on, which is accepatble for an occasional use of the device. This requires an external monitoring circuit to handle the periodic turn on and the sudden possible power on due to user interaction with the TOUCH1 pad.

It should be clear by now that a timing and power enable control circuit is needed to implement these power mode options. The requirements for this kind of system are:

- Independent power shutdown / enable for Microcontroller and/or the Display
- Timing Unit that periodically (about 1 or 2 minute) turns on the Microcontroller supply for WALKING-DEAD and HIBERNATION MODE
- Touch-Input interaction / Priority over the timing circuit, to always guarantee wake up in all possible conditions.

Display power enable

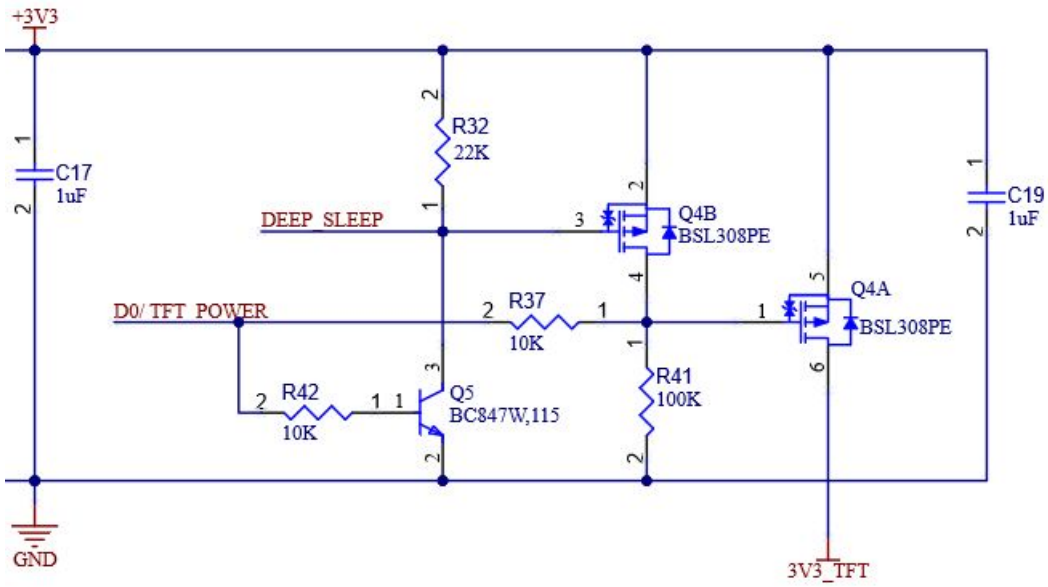


Figure 3.7: Display power enable circuit

The transistor Q4A enables power to the Display.
When the Microcontroller is ON, it constantly drives the D0/TFT POWER PIN:
D0 = 0 → Display ON
D0 = 1 → Display OFF
When the Microcontroller is OFF, D0 is floating, but the display power state is retained thanks to the feedback provided by R37. This allows the MCU to set the D0 state during the periodic turn on and then leave it memorized during the rest of the interval.

Microcontroller power enable

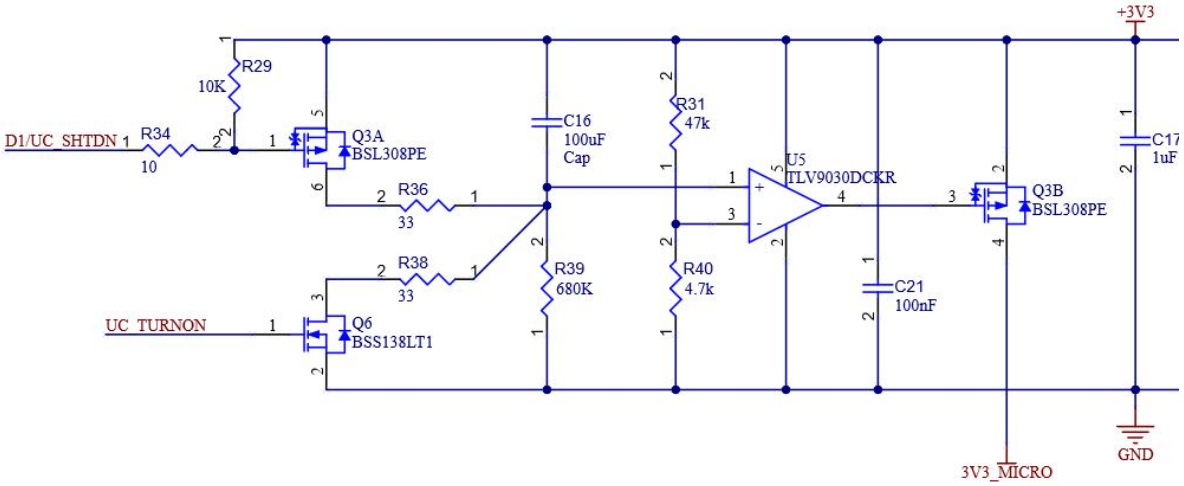


Figure 3.8: Microcontroller power enable circuit

Let's suppose an initial condition where C16 is discharged: The series C16,R39 represents the timing unit (TU), with a time constant of $\tau = C16 * R39$: the transient output of this circuit will be a negative exponential decay starting from 3.3 V

$$V_{OUT_{TU}} = 3.3 * e^{-\frac{t}{\tau}} V \tag{3.4}$$

The voltage divider R31 and R40 provides a reference for the comparator U5 [14]:

$$V_{REF_{TU}} = 3.3 * \frac{R40}{R40 + R31} V \tag{3.5}$$

As long as $V_{OUT_{TU}} > V_{REF_{TU}}$ the output of the comparator will be HIGH, or more precisely, 3.3V $\rightarrow$ Q3B OFF $\rightarrow$ MCU is OFF.
When $V_{OUT_{TU}}$ reaches $V_{REF_{TU}}$ the output of the comparator will transition to LOW, or 0V $\rightarrow$ Q3B ON $\rightarrow$ MCU is ON and will start performing the DISPLAY refresh (if in WALKING-DEAD mode) as well as check the general safety state of the device (battery state, temperature). Afterwards, the MCU drives the D1/UC_SHTDN pin to a LOW state, discharging C16 and shutting itself down. While the MCU is off, the D1/UC_SHTDN output is floating and Q3A turns off (R29 pull-up), at this point the cycle can restart.

At any moment during the cycle, the signal UC/TURN_ON that is directly connected to the D2/IN1 TOUCH1 SIGNAL, can suddenly charge C16, and immediately turn the MCU supply ON.

The refresh period T_{RFSH} can be calculated as:

$$V_{REF_{TU}} = 3.3V * e^{-\frac{T_{RFSH}}{\tau}} \quad \rightarrow \quad T_{RFSH} = \tau * \ln \frac{3.3V}{V_{REF_{TU}}} = \tau * \ln \frac{R40 + R31}{R40} \tag{3.6}$$

This relation reveals that there are two degrees of freedom to set the refresh period T_{RFSH}:

- Changing the RC constant τ: C16 , R39
- Changing $V_{REF_{TU}}$: R31, R40

With the values reported in the schematic above :

$$V_{REF_{TU}} = 3.3V * \frac{R40}{R40 + R31} = 3.3V * \frac{4.7k\Omega}{4.7k\Omega + 47k\Omega} = 0.3V \tag{3.7}$$

$$T_{RFSH} = \tau * \ln \frac{3.3V}{V_{REF_{TU}}} = 680k\Omega * 100\mu F * \ln \frac{3.3V}{0.3} = 163s = 2min\ 42s \tag{3.8}$$

3.4 Sensors and Control

Battery voltage sensing and ADC reference voltage

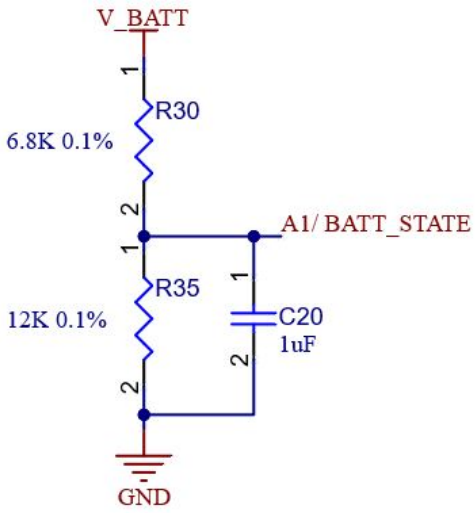


Figure 3.9: Battery voltage reading circuit

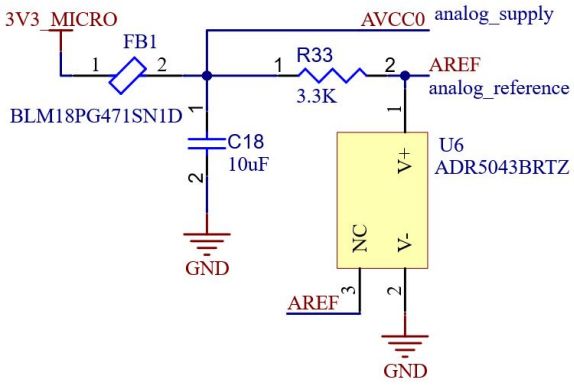


Figure 3.10: ADC supply and reference circuit

The battery voltage sensing circuit is implemented by a simple voltage divider.
A more accurate measurement would also require a voltage follower between the output of the divider and the ADC, but this is necessary only if the current in R30,R35, was around the order of magnitude of the input ADC current. By choosing two precision (0.1% tolerance) resistors, with combined values of $\sim$20KΩ, the divider current should be high enough to neglect the ADC input current.

A consideration should be made on the ADC voltage measurement range, which can be set on the AREF pin of the microcontroller. This value cannot coincide with the output voltage of the linear regulator (VCC), since this would give a huge error in the ADC readings when the value of the battery voltage is below 3.4V. An example should clarify this last statement:

The output of the ADC is a binary number which needs to be multiplied by the ”quantum”, i.e. the voltage value of 1 bit, which depends on the ADC voltage range (AREF) and the number of bits. For this reason it is essential for AREF to be constant throughout all the device operating conditions. If the battery is running low, for instance $V_{BATT} = 3.3V$, the output of the voltage regulator will be $VCC = 3.19V$ (Figure 3.6). Due to this dependency on the battery voltage, it’s not possible to directly connect the ADC reference to VCC.

To overcome this problem, a simple 3.3 V reference was designed using the ADR5043 [15] voltage reference. In principle, this integrated circuit can be treated as a Zener diode that can be used in a wide operating current range $50uA$ to $15mA$.

R33 can be chosen by setting the ADR5043 current and considering the maximum AREF supply current:

$$R33 = \frac{VCC_{MIN} - V_{AREF}}{I_{AREF_{MAX}} + I_{ADR5043}} = \frac{3.19V - 3V}{150uA + 300uA} = 422\Omega \qquad \rightarrow R33 = 390\Omega \qquad (3.9)$$

The AVC00 is the ADC supply pin. It is used to power the ADC internal circuit and can be connected to VCC. An additional filter formed by a ferrite bead (FB1) and a capacitor (C18) filters out any high frequency noise coming from the microcontroller supply.

Primary winding current sensing and Peak Current control

A requirement for implementing a peak current mode control is to measure the primary winding current. Usually two main options are considered for this purpose:

- HALL SENSOR: it uses the Hall effect to determine the current passing through a conductor from the generated electromagnetic field. Using one of these sensors facilitates a fully isolated measurement as well as a very small power loss on the sensor itself due the absence of voltage drop on the high current path caused by the measurement. The main drawback with this kind of approach is the generally higher cost of implementation, the smaller bandwidth compared with other strategies, and a lower resolution which is not ideal for currents in the order of hundreds of mA.

- SHUNT RESISTOR: Measuring current by means of a shunt resistor is the simplest and cheapest solution. The greater disadvantage is the power loss on the resistor, but it guarantees much more flexibility in terms of resolution and bandwidth.

The current measurement circuit translates the primary current waveform into a voltage signal. A typical waveform to be acquired can be the following :

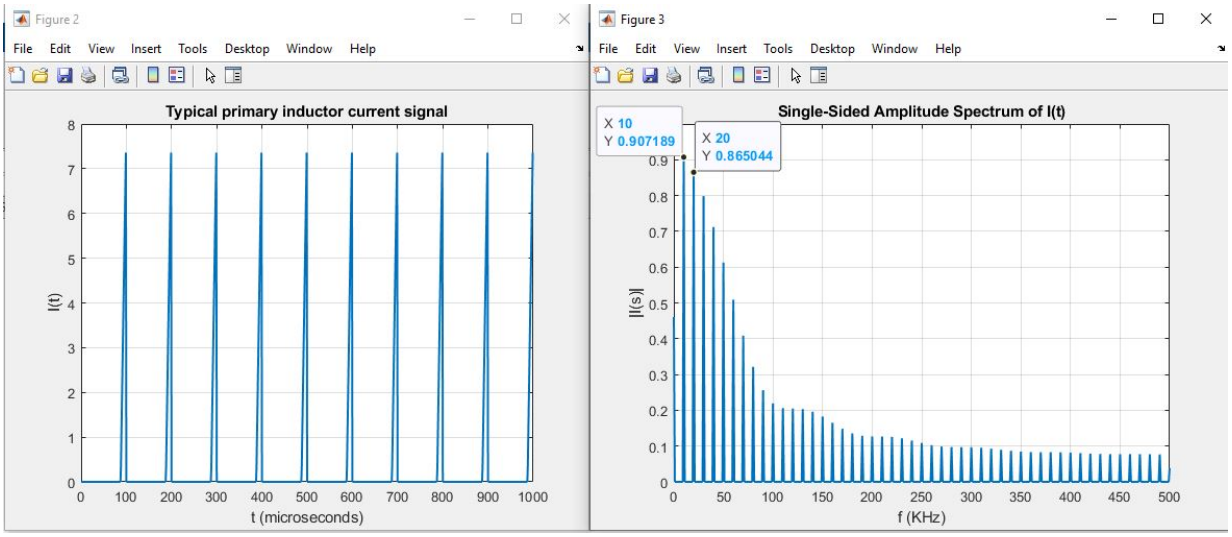


Figure 3.11: 10KHz primary current waveform: $t_{ON} = 13us$. The spectrum is represented on the right

It should be quite evident from the spectrum of this typical signal that the bandwidth of the measurement system should be relatively extended to accurately acquire the current signal, and with low delay. For these reasons, a SHUNT RESISTOR was used, as the limited bandwidth of the Hall sensor was prohibitive.

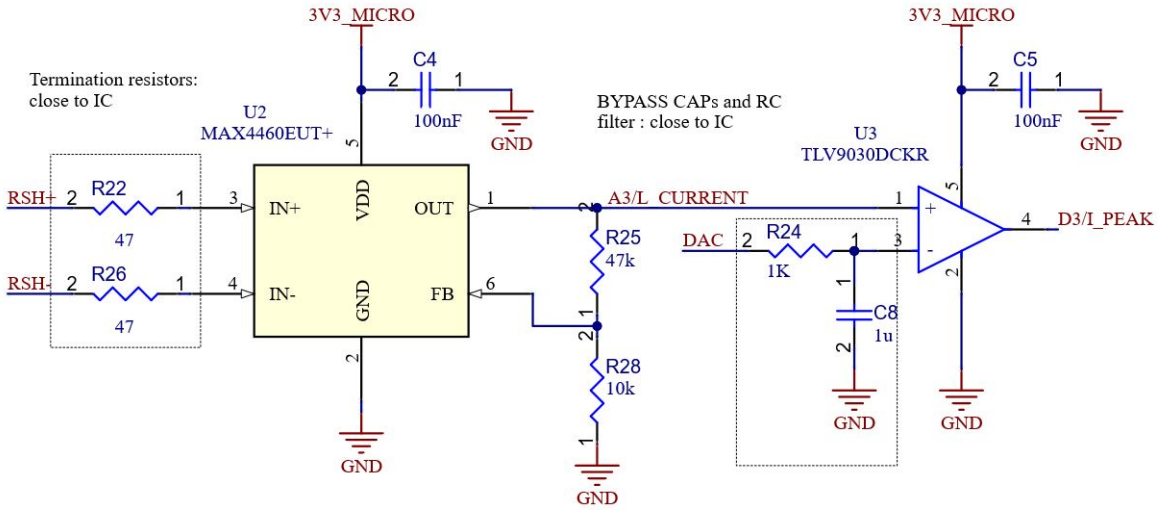


Figure 3.12: Primary current measurement circuit

The value of the shunt resistor has been set to 100 mΩ, but different values will be tested during debug for example $50m\Omega$ or $150m\Omega$.

As previously mentioned, the control technique adopted for the switching circuit is a pseudo-peak current mode control. As the name suggests, it is a current control methodology that can

be divided into the following phases:

1. At the start of the period, the switch is ON, and the current in the primary winding ramps up proportionally to the battery voltage
2. A peak value for the current must be set in advance: I_{PEAK}. As the current increases, it is monitored and measured: as long as the primary current stays below I_{PEAK}, the switch is ON.
3. As soon as the primary winding current reaches I_{PEAK}, the switch is turned OFF, and the current drops
4. The switch remains OFF until the end of the period and afterwards the cycle repeats itself.

To implement this technique, the necessary hardware includes:

- Voltage Amplifier for the shunt resistor voltage
- Voltage Comparator

The voltage amplification will be implemented by an instrumentation amplifier: the MAX4460 [16]. Given that the shunt resistor is referred to ground, there was no apparent need for a differential amplifier, but since this is a PCB where high currents are involved, the ground potential might not be perfectly uniform throughout the circuit boards. As a consequence, a differential measurement was found to be more appropriate.

An important parameter to take into account in this particular case is the Gain Bandwidth Product, that corresponds to the bandwidth of the amplifier at unity gain, this information can be retrieved from the datasheet of the MAX4460 [16], and is equal to : $GBW = 2.5MHz$
By applying general Analog Electronics theory it can be observed that for a single pole amplifier the GBW (gain bandwidth product) is constant, and by increasing the Gain, the bandwidth is reduced. For this reason care must be taken when setting the gain, since this could worsen the ability of the circuit to accurately follow and amplify the input signal, without introducing delays.

The resistors R25, R28 set the gain of the device: by choosing $R25 = 47K\Omega$ and $R28 = 10K\Omega$, the low frequency gain is:

$$G = 1 + \frac{R25}{R28} = 1 + \frac{47k\Omega}{10k\Omega} = 5.7 \tag{3.10}$$

And the estimated bandwidth now is:

$$BW = \frac{GBW}{G} = \frac{2.5MHz}{5.7} = 439KHz \tag{3.11}$$

The obtained value of bandwidth should be high enough to prevent excessive distortion of the input signal and preserve most of the relevant harmonics.
Considering a maximum measurable value of current of $4A$, the voltage drop on the shunt resistor is: $(R_{SH+} - R_{SH-}) = 4A * 100m\Omega = 0.4V$. This value will be amplified by a factor of 5.7 resulting in a maximum output of $0.4V * 5.7 = 2.28V$.
The amplified shunt resistor signal is both connected to a voltage comparator (HARDWARE/ANALOG COMPARATOR) and the ADC of the Microcontroller, to be sampled (SOFTWARE COMPARATOR). This last approach is not optimal, since the ADC conversion time is quite significant relatively to the typical t_{ON}, and would introduce a huge error. Anyhow, the connection to the ADC will still be executed, but most probably ignored by the software.
The hardwware comparison will be implemented by the TLV9030 [14], a very fast, push-pull voltage comparator with a typical propagation delay of 100 ns (much faster then the software version).
The non inverting input will be connected to the primary winding current signal, while the inverting input will be connected to the Digital to analog converter DAC. The output is attached to an interrupt pin of the Microcontroller.
The relation between I_{PEAK} and the 12 bit DAC binary output is:

$$DAC_{OUT} = R_{SHUNT} * I_{PEAK} * G \tag{3.12}$$

$$DAC_{OUT_{BINARY}} = 2^{12} * \frac{DAC_{OUT}}{DAC_{RANGE}} \tag{3.13}$$

If the primary winding current is greater then the peak current value I_{PEAK}, the output transition from LOW to HIGH generates an interrupt, which indicates that the desired value of current was reached.

To validate the design and ensure a correct operation, a SPICE simulation was performed:

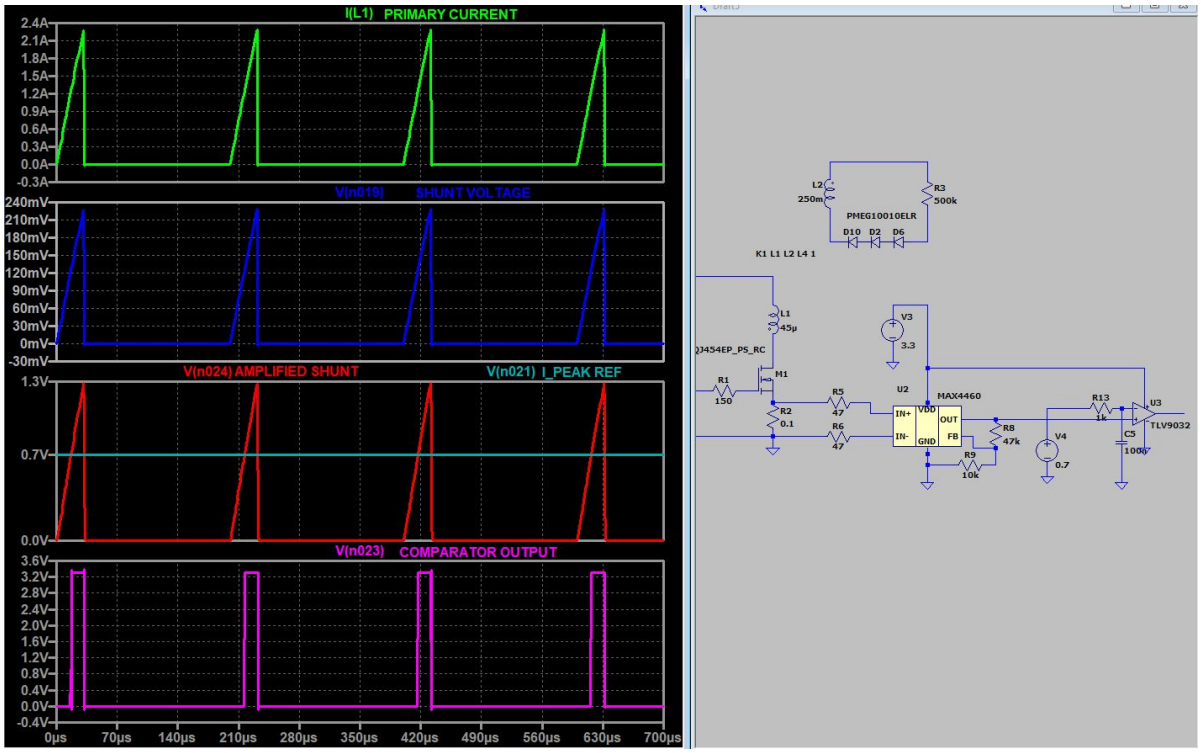


Figure 3.13: SPICE simulation of the current measurement circuit

Chapter 4

Physical Implementation and Testing

PCB Layout

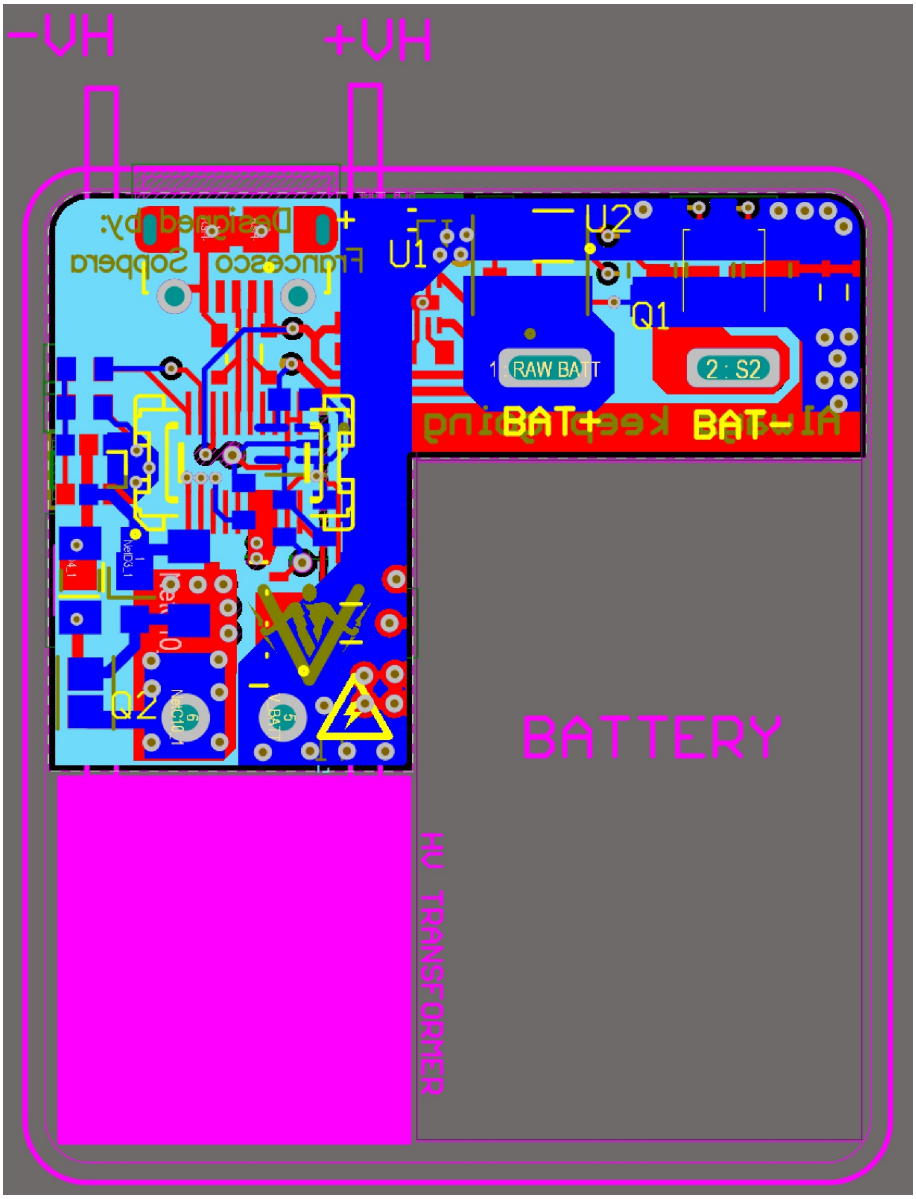
A good PCB Layout plays a crucial role in the design process to ensure a positive outcome of the circuit functionality and performance.
In the following pages a possible implementation is presented.
Great care and attention to details were dedicated to the design of these circuit boards, but it would be too extensive to include and explain every single design choice. Nevertheless, a very visual summary will give a pretty clear idea of the general design approach.

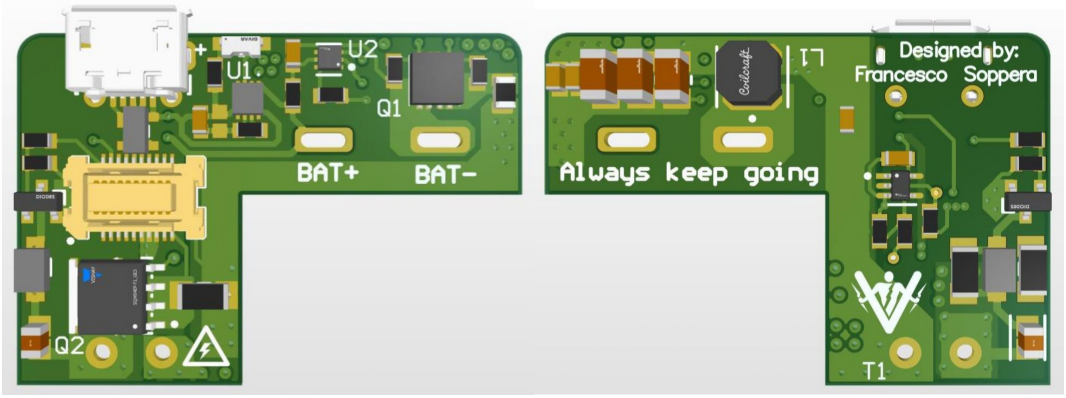
Both the POWER PCB and the CONTROL & LOGIC PCB are multi-layer boards:

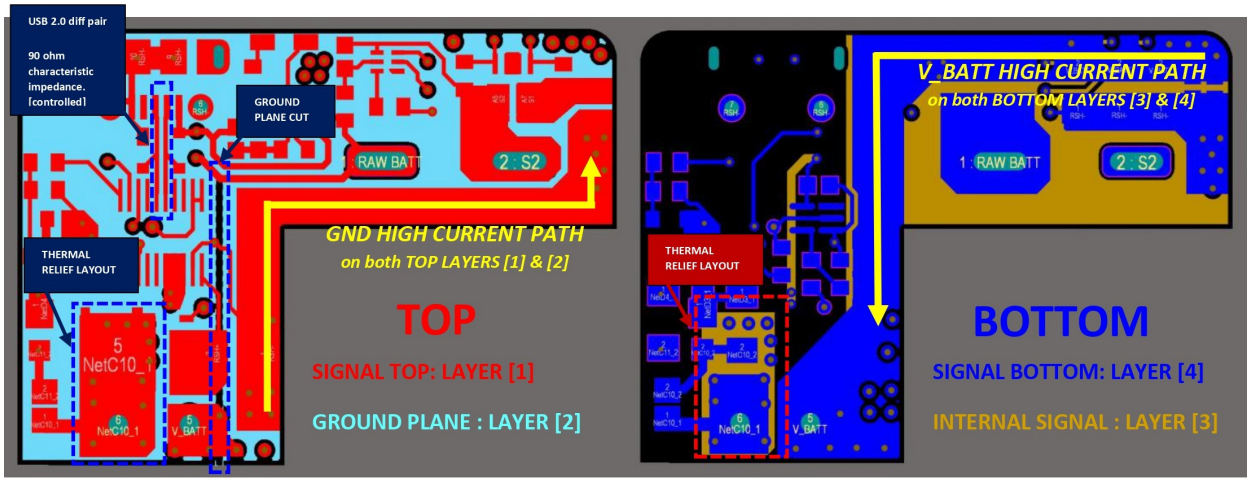
- TOP LAYER
- INTERNAL SIGNAL LAYER
- GROUND PLANE
- BOTTOM LAYER

After the design was completed, the boards were manufactured in CHINA. The soldering and assembly was completely done manually and without external support, using low temperature solder paste, the board stencil ordered with the PCBs, and a small reflow heating surface.

4.1 POWER PCB Layout

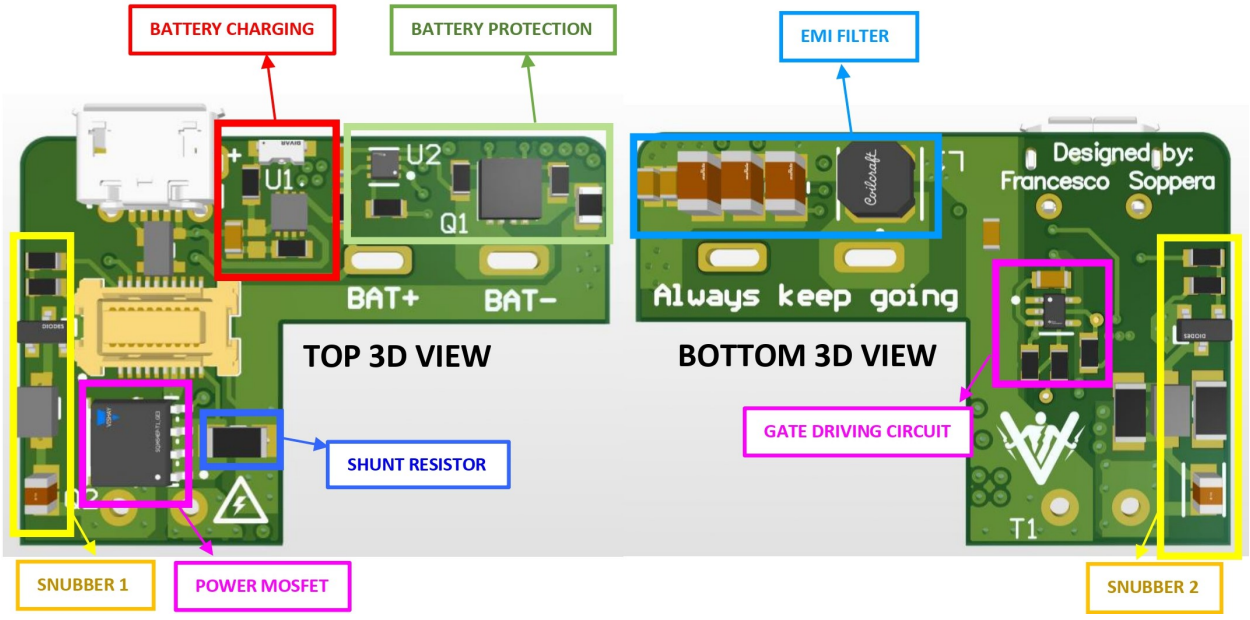




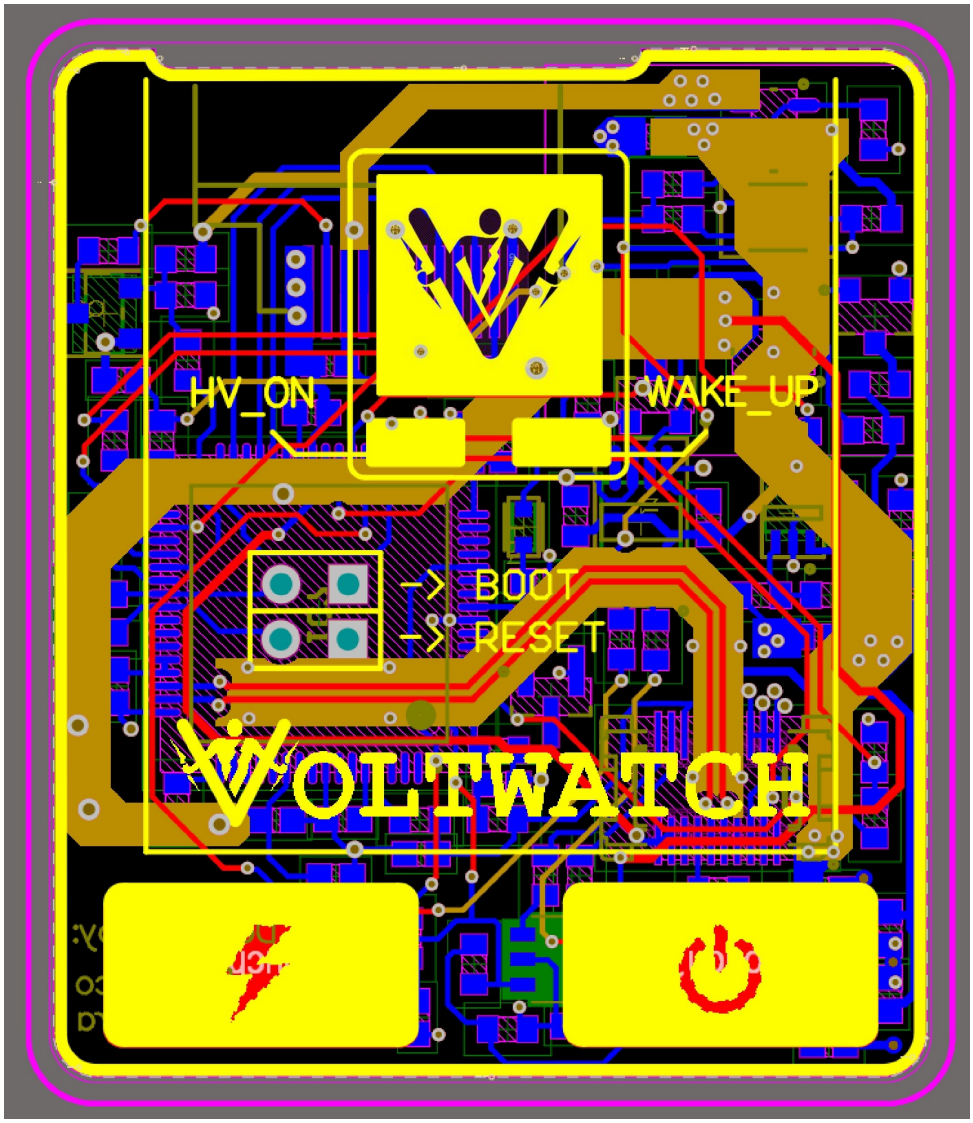


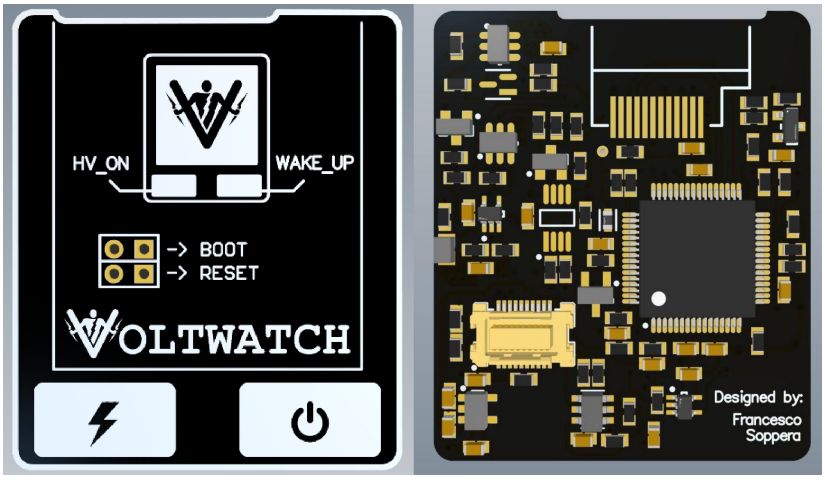
The most critical aspect in this layout is the high current path going from the battery to the HV transformer. There are two main things to consider in this case:

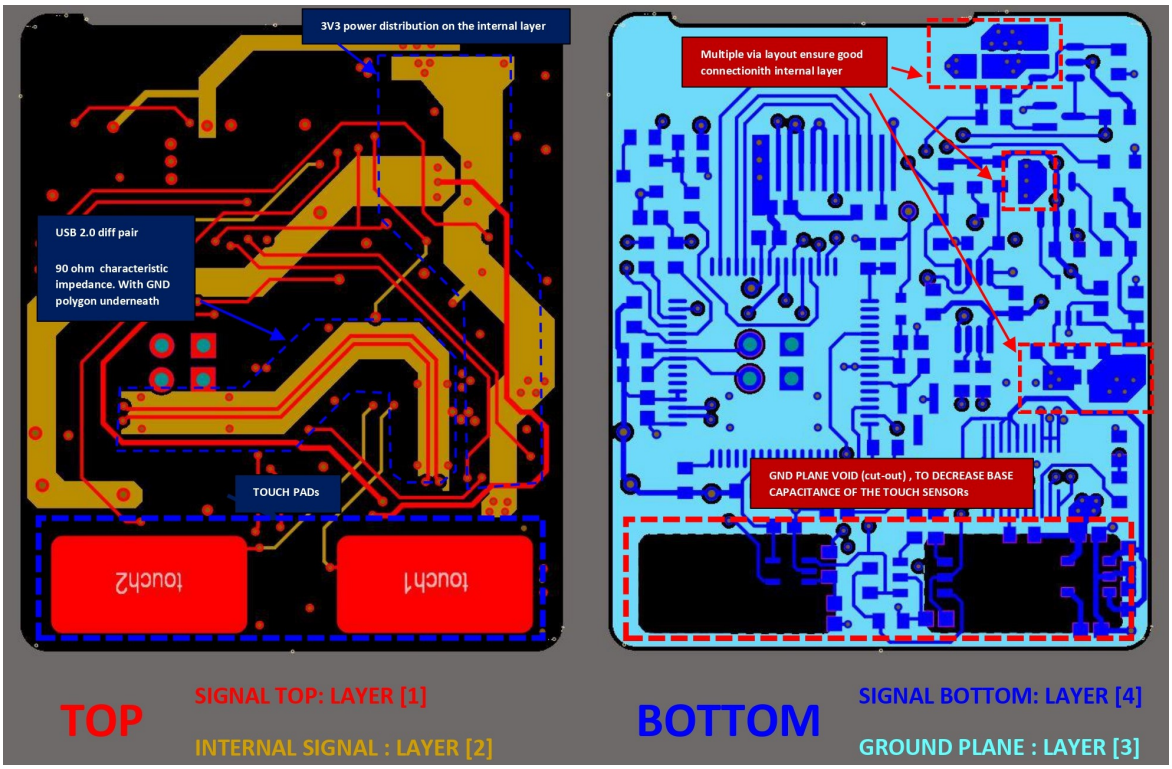
- **Thermal problems:** the traces and/or polygons carrying the high current must be sized accordingly. Both the positive and negative high current path involve two layers each, to share the thermal stress.
- **EMI noise:** Considering the high pulsed current involved, it's fundamental to take into account the electromagnetic impact on the whole PCB stack. In order to mitigate this issue, the positive and negative high current path run on opposite sides of the board but overlap as much as possible to achieve the cancellation of the electromagnetic fields. For example, as indicated in the picture, a GND plane cutout was also created to "guide" and confine the negative current path to the desired portion of the board.

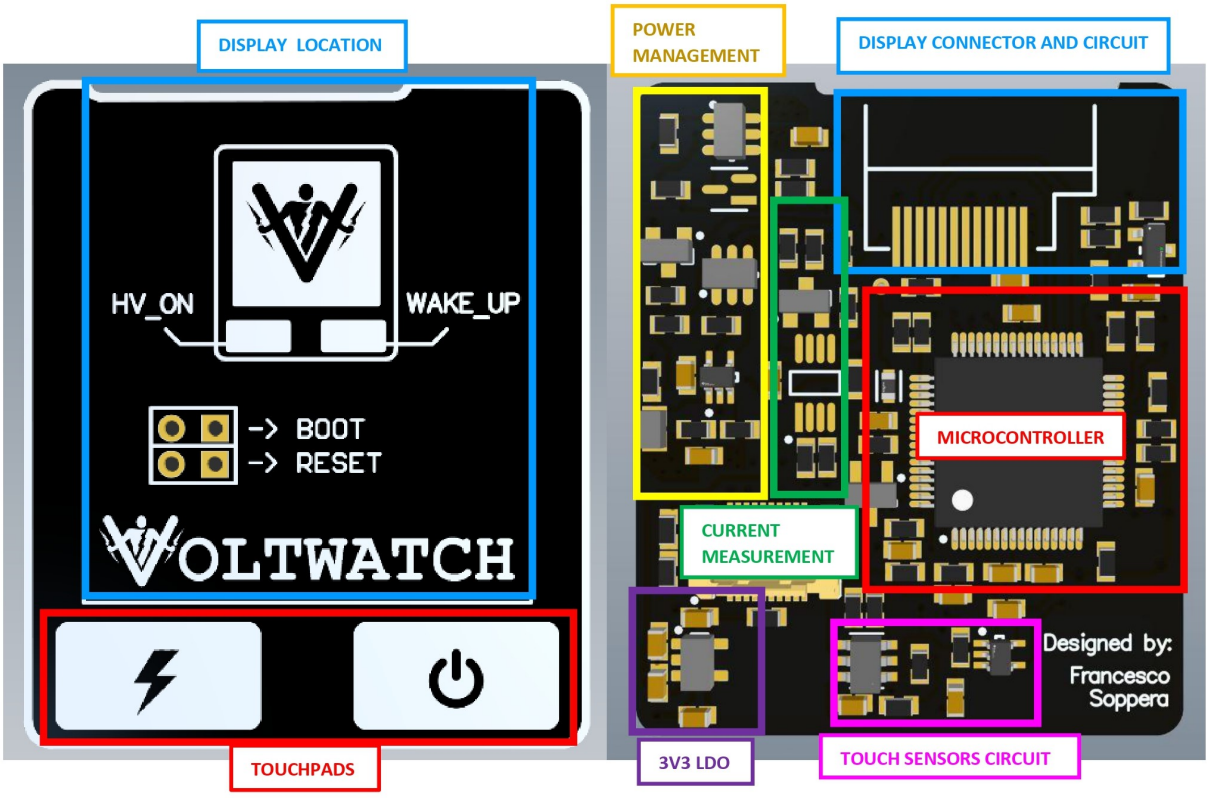


4.2 LOGIC & CONTROL PCB Layout






3V3 power distribution on the internal layer
USB 2.0 diff pair
90 ohm characteristic impedance. With GND polygon underneath
TOUCH PADs
touch2
touch1
Multiple via layout ensure good connectionith internal layer
GND PLANE VOID (cut-out) , TO DECREASE BASE CAPACITANCE OF THE TOUCH SENSORs
TOP
SIGNAL TOP: LAYER [1]
INTERNAL SIGNAL : LAYER [2]
BOTTOM
SIGNAL BOTTOM: LAYER [4]
GROUND PLANE : LAYER [3]


DISPLAY LOCATION
HV_ON
WAKE_UP
-> BOOT
-> RESET
VOLTWATCH
TOUCHPADS
POWER MANAGEMENT
DISPLAY CONNECTOR AND CIRCUIT
MICROCONTROLLER
CURRENT MEASUREMENT
Designed by:
Francesco Soppera
3V3 LDO
TOUCH SENSORS CIRCUIT

4.3 INTERFACE PCB

Some 2 layer interface PCB were designed and manufactured as well. Their main function is to facilitate the connection with the secondary winding of the high voltage transformer, and to guide the high voltage path outside the device, rectifying it thanks to a series of 3 diodes.

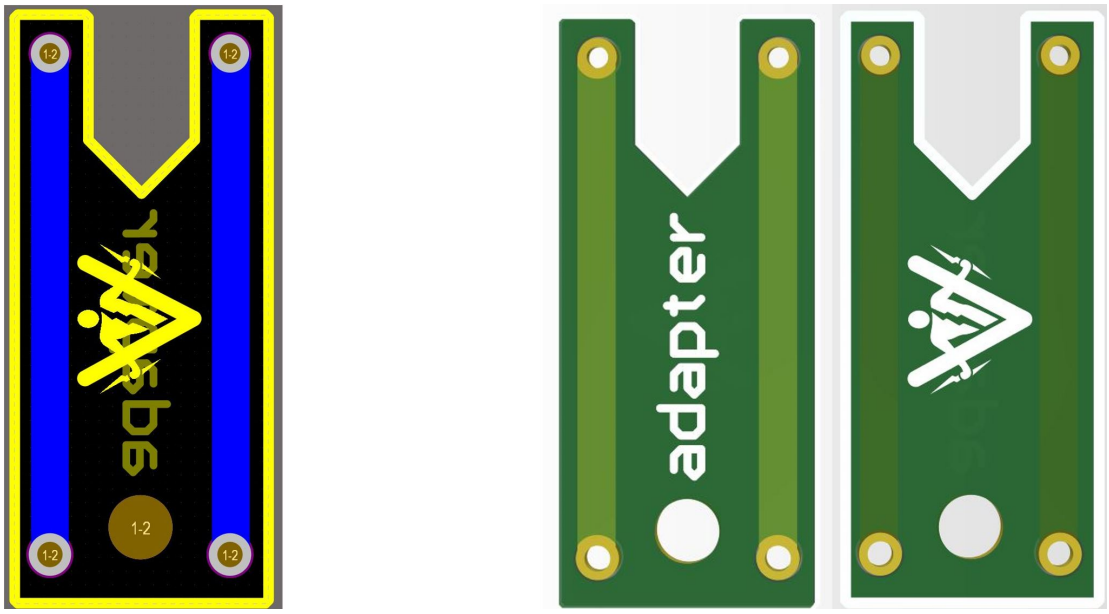


Figure 4.1: General Purpose HV adapter. To be used outside the device

Figure 4.2: High voltage GUIDE, with rectification and accessible connector. Mounted INSIDE the device

4.4 FULL ASSEMBLY

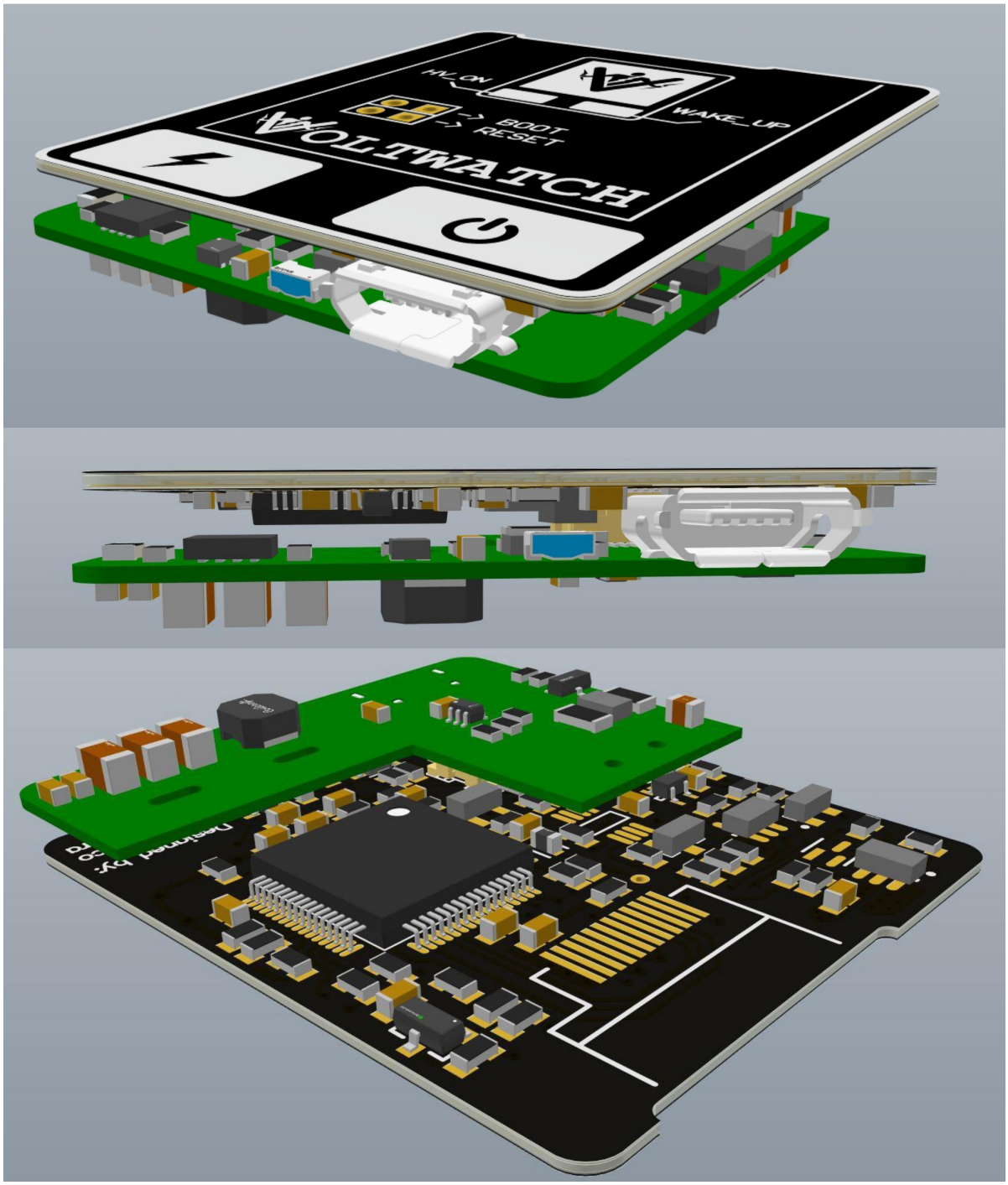


Figure 4.3: 3D assembly of the PCB stack (not including the interface boards), the display is not present in this renders

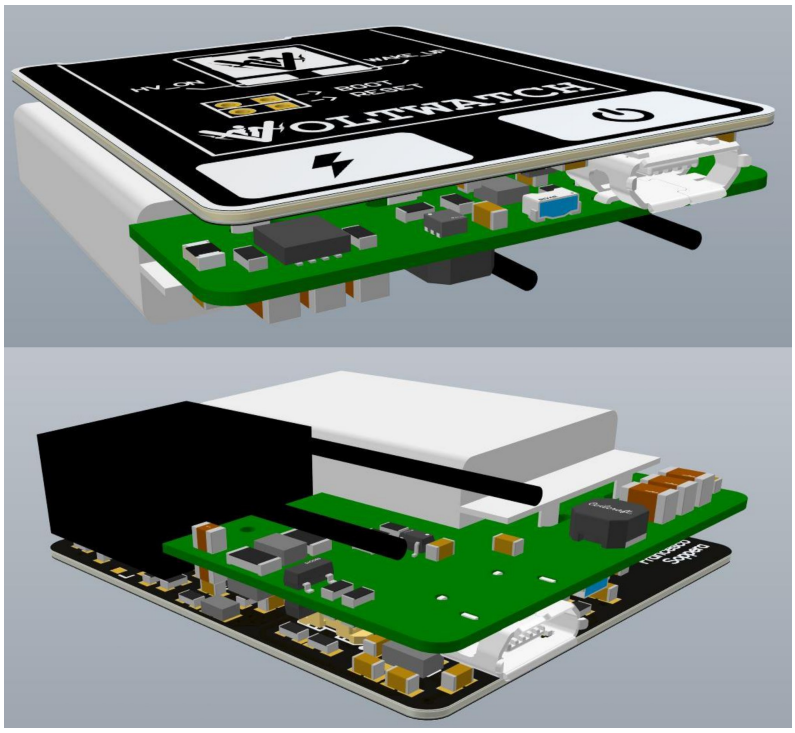


Figure 4.4: 3D assembly of the PCB stack including the battery and the HV-transformer

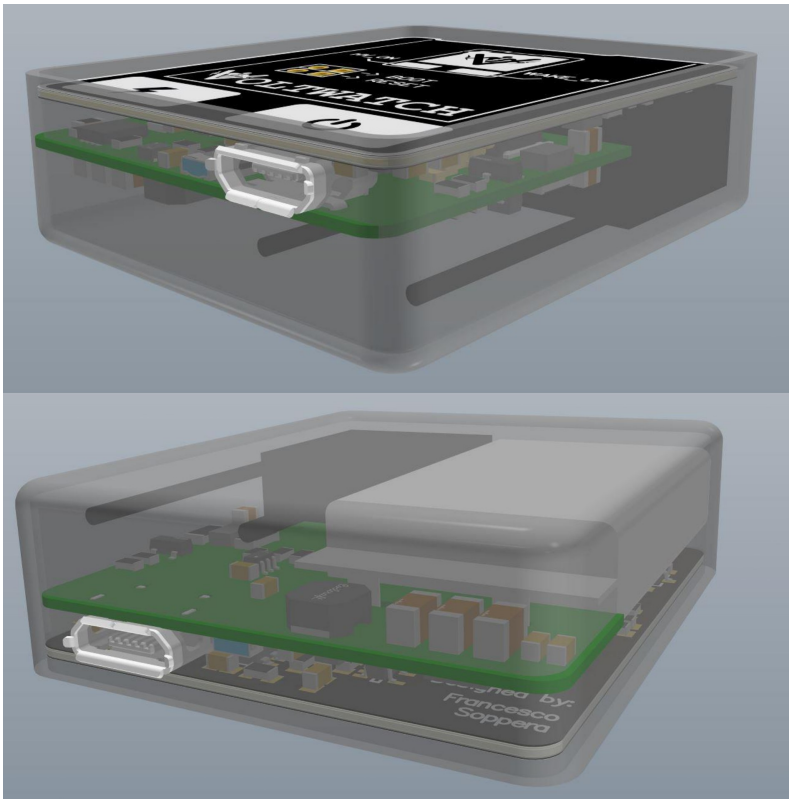


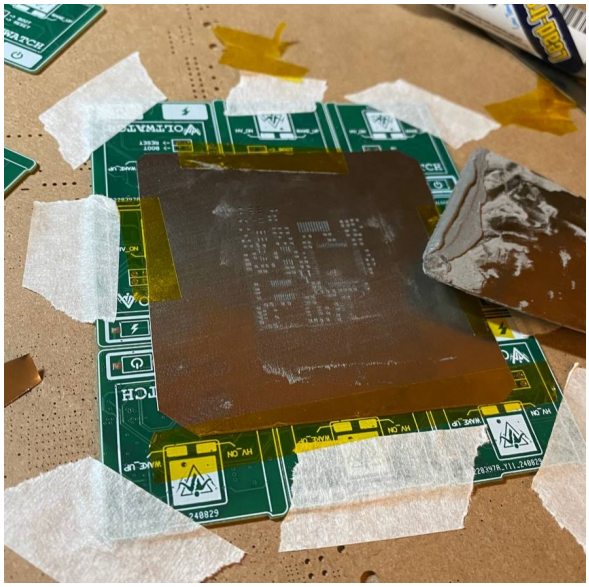
Figure 4.5: 3D assembly of the device, including the CASE: the case is not refined yet and needs be improved, but it's enough to check for proper internal electronics fitting

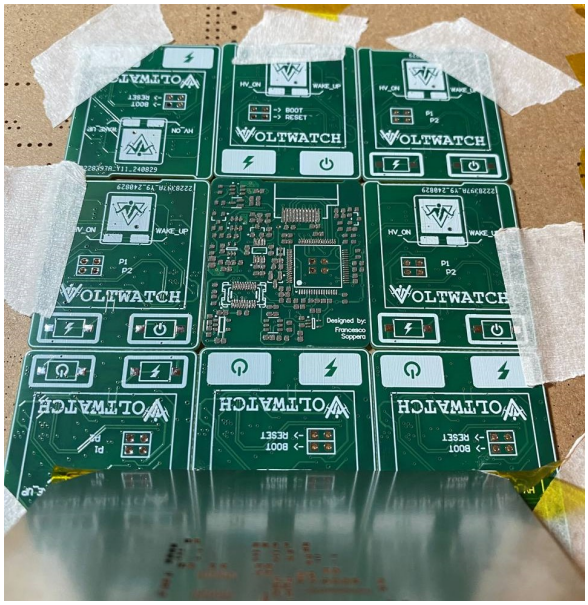
4.5 Manufacturing and Testing

Soldering and Device Assembly

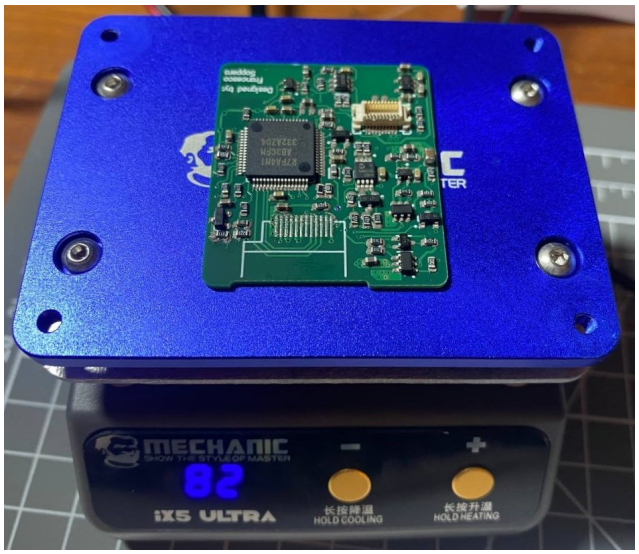
In the following pictures, the assembly and soldering process is illustrated:

1. Solder paste application, using the stencil ordered along with the boards





2. Components placement and reflow soldering



3. Final assembly

Figure 4.6: Boards-only stack-up

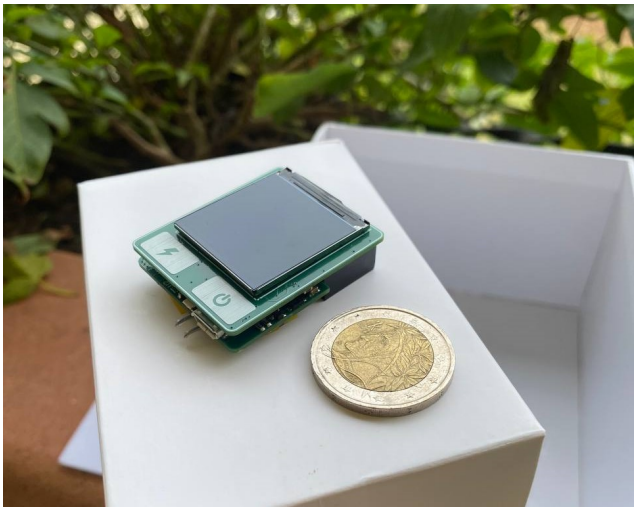


Figure 4.7: Battery and Transformer included

Figure 4.8: **VOLTWATCH**

Testing

The main objective of the testing process was to validate theoretical, analytical and simulation results previously obtained. Only the most relevant acquired waveforms will be presented in this report:

- **Primary current waveform**: measured as the voltage drop on the $100m\Omega$ shunt resistor, this means that a value of $100m\Omega$ corresponds to 1A. T_{ON} was set at $10us$, to allow for comparison with simulations performed in Chapter 2 : [Figure 2.16 $\rightarrow$ Figure 2.20] can be taken as reference.
  In LIGHT LOAD conditions non idealities are more likely to come up, since the primary voltage pulse depends more substantially on the power switch intrinsic parameters.

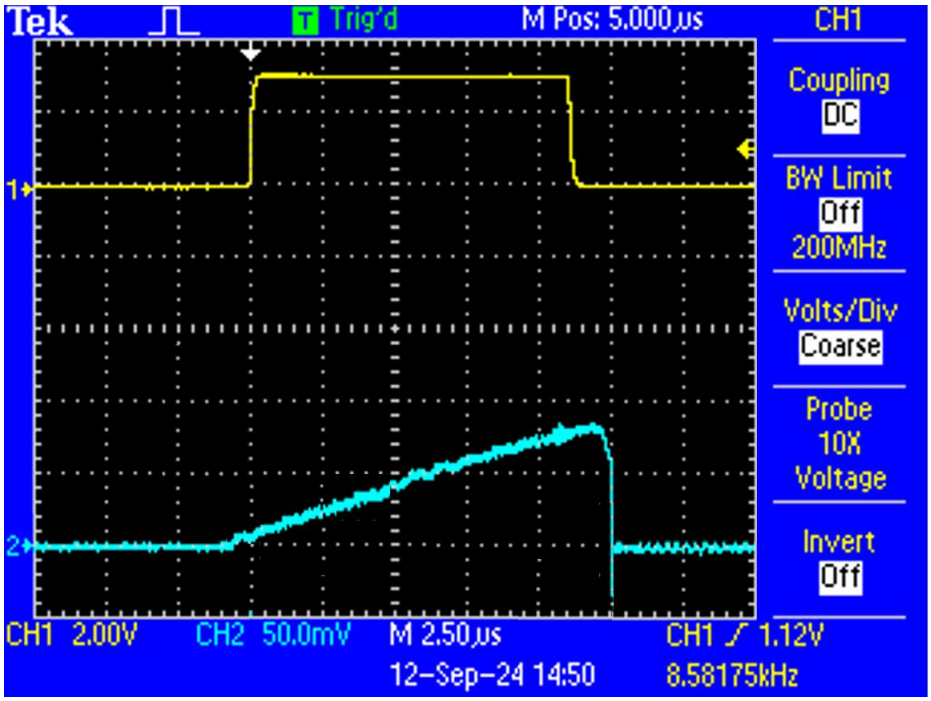
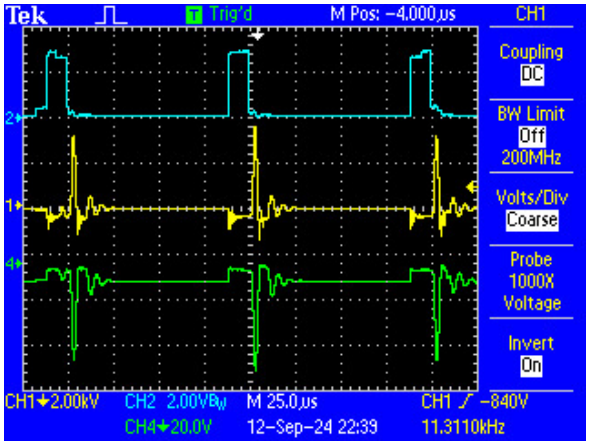
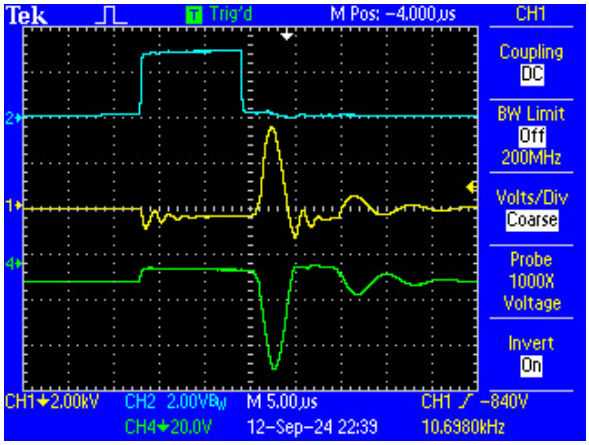


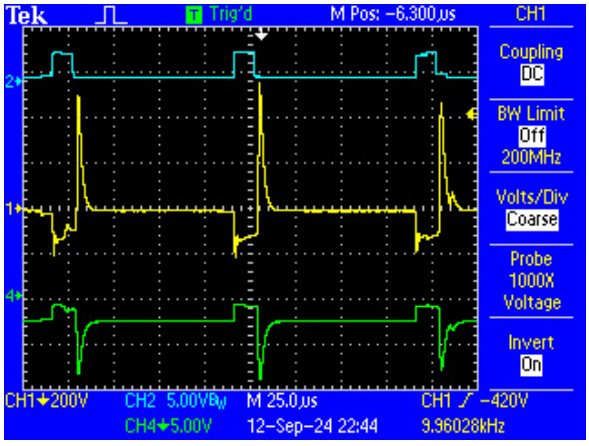
Figure 4.9: [CYAN : Primary current], [YELLOW : Gate control voltage]

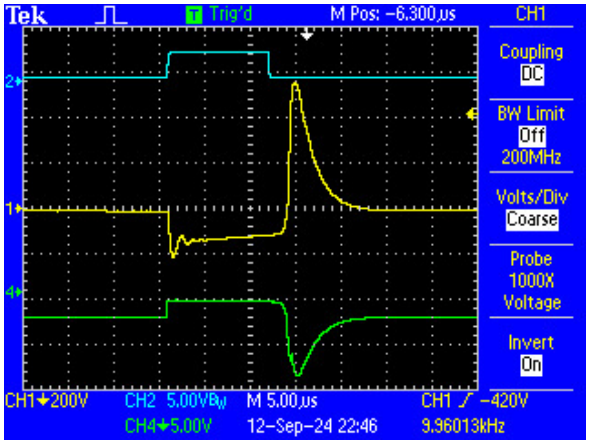
- **Primary and secondary winding voltage in LIGHT LOAD CONDITION [**$R_{LOAD} = 500k\Omega$**]**: T_{ON} was kept at 10us to check for consistency with simulations performed in chapter 2: Figure 2.17 can be taken as reference.
  EXPECTED $V_{L1_{PEAK}} = -60V \Rightarrow$ EXPERIMENTAL $V_{L1_{PEAK}} = -52V$
  EXPECTED $V_{L2_{PEAK}} = 4.5kV \Rightarrow$ EXPERIMENTAL $V_{L2_{PEAK}} = 3.9kV$
  The experimental result are consistent with the simulations within an acceptable margin of error, keeping in mind that we're now considering an OPEN LOOP control situation.
  $V_{L1_{PEAK}} : GREEN \qquad V_{L2_{PEAK}} : YELLOW \qquad V_{GATE} : CYAN$





- **Primary and secondary winding voltage in HEAVY LOAD CONDITION [**$R_{LOAD} = 50k\Omega$**]**: T_{ON} was kept at 10us to check for consistency with simulations performed in chapter 2 : Figure 2.18 can be taken as reference.
  EXPECTED $V_{L1_{PEAK}} = -7.4V \Rightarrow$ EXPERIMENTAL $V_{L1_{PEAK}} = -8V$
  EXPECTED $V_{L2_{PEAK}} = 550V \Rightarrow$ EXPERIMENTAL $V_{L2_{PEAK}} = 570V$
  $V_{L1_{PEAK}} : GREEN \qquad V_{L2_{PEAK}} : YELLOW \qquad V_{GATE} : CYAN$





- **Peak current mode control**: Multiple I_{PEAK} values were chosen to test the peak current mode control: $I_{PEAK} = 500mA$, $1A$, $2A$, $3A$.
  In the following screenshots The GREEN trace represents the voltage drop on the $100m\Omega$ shunt resistor. The gate control voltage is also displayed in CYAN color in the upper part of the screen.
  As can be observed from the images the primary winding current was correctly controlled within an acceptable margin of error.

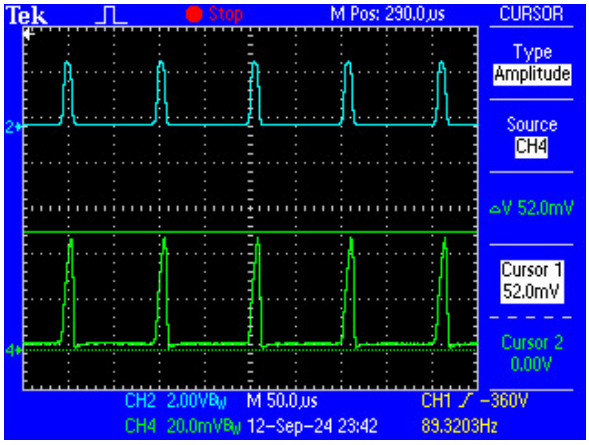


Figure 4.10: $I_{PEAK} = 500mA$

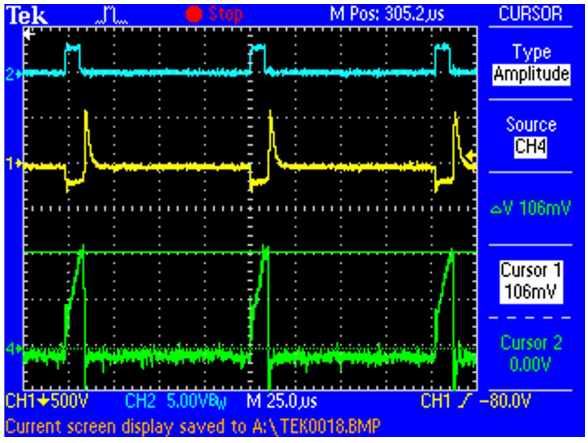


Figure 4.11: $I_{PEAK} = 1A$

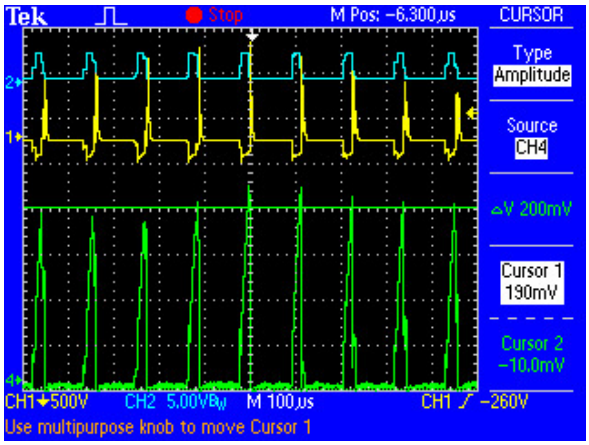


Figure 4.12: $I_{PEAK} = 2A$

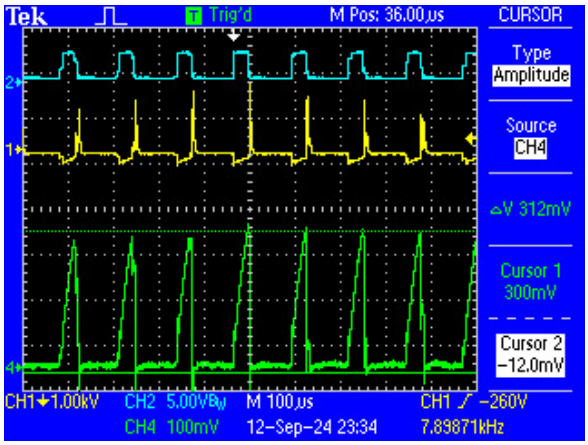


Figure 4.13: $I_{PEAK} = 3A$

- **Snubber circuit 1 and 2**: both snubber circuits were tested with T_{ON} = 10us, as it is simulated in chapter 2.
  Figure 2.19 and 2.20 can be taken as reference for this test.

  SNUBBER 1 : EXPECTED $V_{L2_{PEAK}} = 1.7kV \Rightarrow$ EXPERIMENTAL $V_{L2_{PEAK}} = 1.8kV$
  SNUBBER 2 : EXPECTED $V_{L2_{PEAK}} = 640V \Rightarrow$ EXPERIMENTAL $V_{L2_{PEAK}} = 600V$

  LEGEND: $V_{L1_{PEAK}} : GREEN$ $V_{L2_{PEAK}} : YELLOW$, $V_{GATE} : CYAN$,

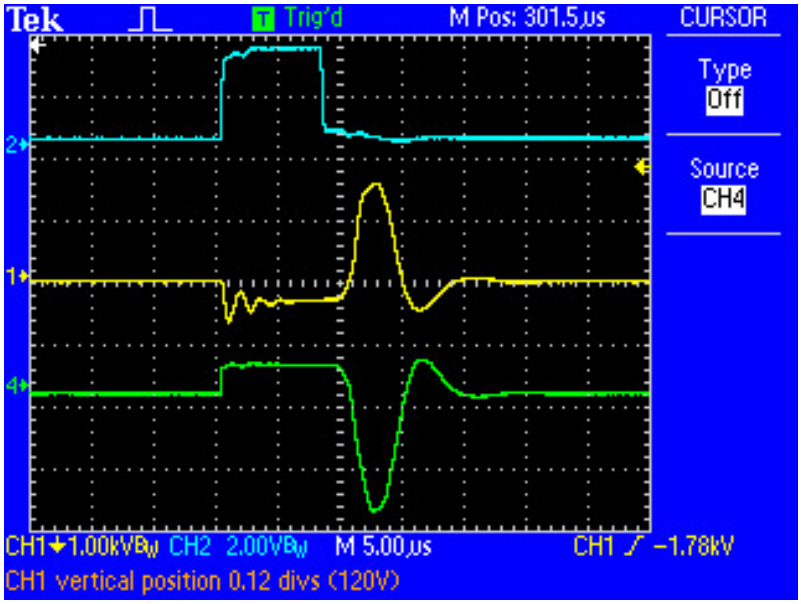


Figure 4.14: SNUBBER 1 : $R = 180\Omega$, $C = 47nF$ [Green trace = 20 V/DIV]

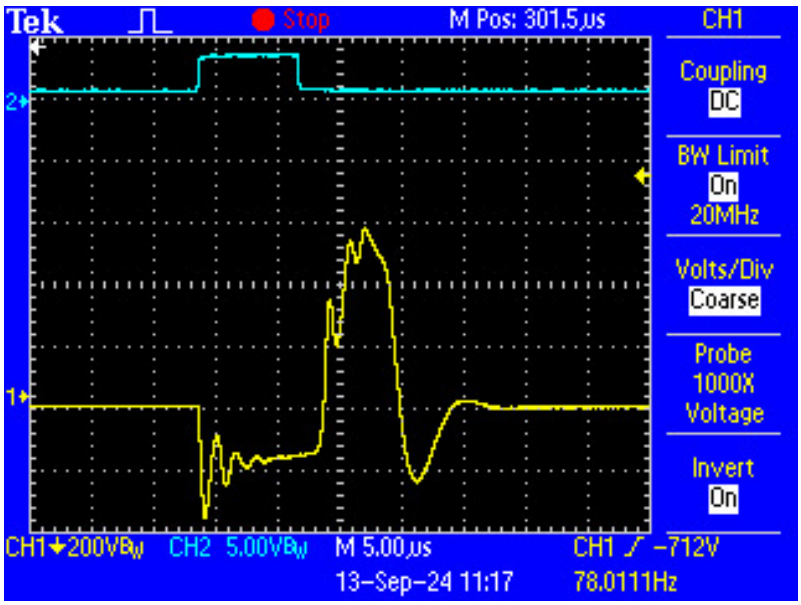


Figure 4.15: SNUBBER 2 : $R = 100\Omega$, $C = 330nF$

4.6 Electric arc generation

The range of output voltage values that can be achieved with this device is very wide, and can go up to very dangerous values.
For this reason, during the initial development and tests, only experts or highly trained technicians should be allowed to use it and/or program it.
As a demonstration of the capabilities of this project, it will be used to generate an electric arc.
The details about this physical effect is not the focus of this thesis but, generally speaking, if the potential difference between two electrodes separated by air reaches a level high enough to overcome the dielectric strength of the air, an arc will be generated.
The dielectric strength of air is equal to 3 kV/mm, this means that in order to generate a 5mm arc, the voltage at the secondary needs to be 15 kV. In the following images the adapter board was used to provide mechanical support and electrical connection to the secondary winding for this demonstration.

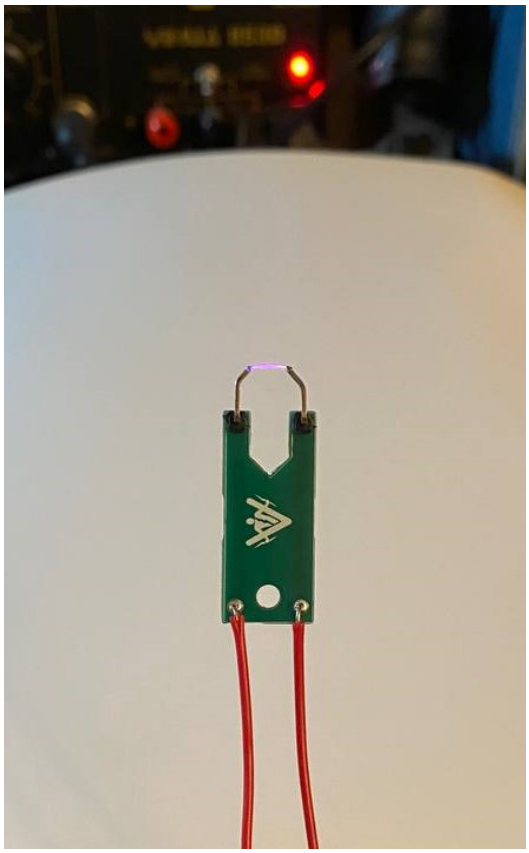


Figure 4.16: 5mm ARC, Vout= 15kV

Figure 4.17: 5mm ARC, Vout= 15kV

Conclusions

The main objective of this thesis was to design from scratch a small, portable and optionally wearable voltage conversion device to be used for electrical stimulation purposes.
Circuit analysis, simulations, manufacturing and testing procedures were presented in great detail and the results were extremely positive: the device has been fully assembled and is functional, the output waveforms generated are quantifiable, and always consistent with simulations results within an acceptable margin of error.
On the low power side, different Power managements strategies (hardware and software) were used to push the battery life of the device to up to 12 days. Furthermore, the user interface implemented by the touch buttons and the display is simple and intuitive.
The peak current mode control algorithm was successfully performed, but in future versions of the device it should be integrated with a voltage mode control in a nested closed loop configuration. Implementing a voltage feedback circuit for a train of high voltage pulses of the duration of a few microseconds will be a great challenge.
Future developments and improvements could also aim to increase the efficiency of the switching circuit and optimizing thermal management. In addition, safety is obviously a great concern, and a more detailed study should be performed on the device enclosure, to guarantee full isolation in every operating condition.

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