Università degli Studi di Padova

Department of Information Engineering

Master Thesis in Electronic Engineering

Reorganization of carrier cancellation in a filter chain for delta-sigma applications and optimization of the calibration.

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Abstract

This thesis documents a feasibility study with respect to the reorganization of a hardware filter chain of a SDADC demodulator. The investigation is based on an existing hardware filter chain architecture which is configurable in order to cover several different applications. The configuration which is in the focus of this thesis is used for a resolver application in which the rotor position of an engine is determined. It involves a 3rd order CIC filter for the demodulation of a pulse density modulated signal which is produced by a SDADC, a 1st order IIR filter for offset compensation and a rectifier circuit and an accumulator for carrier cancelation. In the future all filters except for the CIC filter shall be realized by a digital signal processor in order to provide more flexibility and enable more applications. But since the carrier cancelation is based on a quite dynamic signal, the rectification might have to be implemented in hardware.
Therefore, it will be investigated how the problem of the dynamic carrier cancelation can be solved for the new architecture. To this end, the influence of repositioning the carrier cancelation will be examined with respect to the filter chain precision. Furthermore, it will be analyzed if interpolation is a useful measure to improve the precision and trade-offs for certain conceptual considerations will be highlighted. Investigations with respect to the calibration were skipped.

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1 Introduction

1.1 Introduction

Sigma delta modulator (SDM) are widely used as common converter to acquire analog signal. They are practical to implement on integrated circuit but usually they have a few output bit length and they need a digital signal processing (DSP) stage after the digital output. The SDM uses high sampling rate to shape the noise and increase the output performance in terms of SNR in the bandwidth of interest. The noise power is distributed from the DC component to the Nyquist frequency $\frac{f_s}{2}$. If a modulator is oversampled , the input signal spectrum will be smaller than the Nyquist frequency. The noise power decrease with the sampling rate, due to this behaviour , the SDM has very high sampling rate in order to increase the SNR in the bandwidth of interest. After the Converter is necessary a processing stage in order to change the output characteristics. The current SD implementation has 1 bit width and a sampling frequency of 10 MHz, due to this performance, a decimation stage is necessary in order to adapt the sampling frequency for computational operation. The processing stage must filter the bandwidth of interest in order to attenuate the noise shaping introduced by the sigma delta. The number of applications that the sigma delta plus the filter chain are involved are many and due to this reason is necessary to adapt the architecture to deal with the required performance that can be : output sampling rate, bandwidth , SNR , bit width .

1.2 Problem Overview

The current investigation is for an automotive application that uses a sigma delta modulator in order to acquire an modulated signal. The task is measure the rotor angle position. The hall sensor provided an analog signal proportional to the rotor position. The hall sensors have a sinewave output with fixed peak amplitude. A complete rotor rotation will provide a full sinewave period. The sensors signal is modulated with an AM modulation and it is

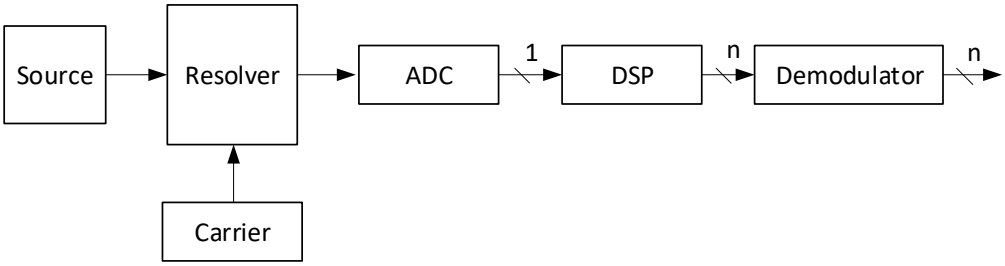

Figure 1.1: The figure represent a general schematics for many applications.

the sigma delta input . After the DSP stage , the demodulator must synchronize the processed signal with the generated carrier. Due to the delay introduced by the filter chain , it is necessary understand if is possible to reorganize the configuration in order to avoid this problem. A good point to start is to understand if the FIR filters could be bypassed and integrated in a micro-controller. After a first check is possible investigate on the demodulator reorganization .

2
State of the Art

This thesis study a different possibilities for the reorganization of the filter chain with respect of resolver application.The starting point is to analyse the state of the art with respect of the resolver application. In the next section will be propose some common filter design application for sigma delta converter.

2.1 AM Modulation in Theory

The AM modulation is a technique used to translate the payload frequency from the baseband to higher frequency, in order to transmit the signal via radio wave. Defined $x_p(t)$ the payload signal and $x_c(t) = A \cdot sin(\omega)$ the carrier component , the relationship that define the modulation is :

$$x_m(t) = (1 + x_p(t)) \cdot x_c(t) = x_c(t) + x_c(t) \cdot x_p(t) \tag{2.1}$$

The payload can be whatever signal with finite bandwidth.

2.2 AM Modulation in Practice

The modulation used in the current application is a simple multiplication between the payload signal and the carrier signal. The result is more or less the same than the theoretical version. The carrier component on frequency domain is not present due to the missing of $+1$ in the formula 2.1. The current modulated signal is define by the relation : $x_m(t) = x_c(t) \cdot x_p(t)$ that in this application is $x_c(t) = 1 \cdot cos(\omega)$ and $x_p(t) = 5 \cdot sin(\omega)$

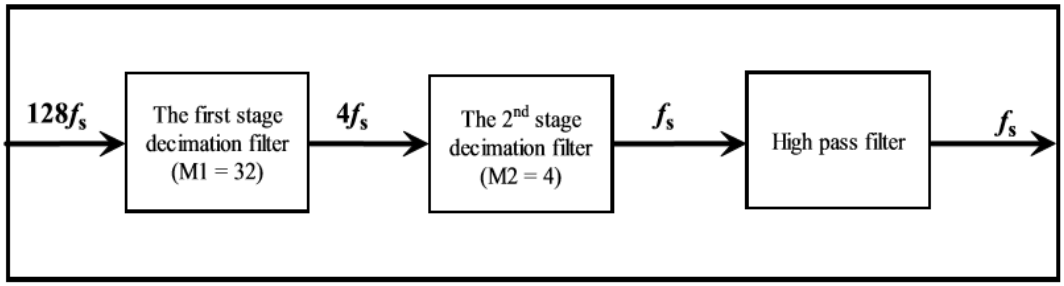

Figure 2.1: Decimation filter figure proposed by [1]

2.3 Resolver Application : Examples

2.3.1 Digital Decimation Filter Design for SDADC with high performance

A-16 bit decimation filter for a second order Sigma-Delta converter is used as first filter stage in order to elaborate the output signal, increase the world bit length and cancel the modulator carrier.A decimation filter is useful to trade bandwidth with noise power, indeed for a lower bandwidth value, that means high decimation ratio, the noise power is lower.Moreover , use only one decimation filter is not sufficient and furthermore, a second filter stage is necessary. The second stage could be an Half band filter with FIR architecture. It is also possible to compensate DC component with an IIR high pass filter made with a low bandwidth in order to keep the useful signal component and cut-off only the DC component. [1] As starting point is necessary configure the decimation filter. In order to save area and power, it is necessary use a CIC configuration. The frequency specification for this application are :

- Pass-Band 0.454fs
- Stop-Band 0.583fs
- Stop-Band-Attenuation 50dB
- Output sampling frequency span [8 32 44.1 48] kHz for an Audio application

From the frequency specification is possible calculate the filter decimation rate that is 128. Only a comb filter can not satisfy the specification due to the low slope on the transitory band. For this reason the overall decimation ratio is split between the two filter stage : 32 for the CIC and 4 for the half -band FIR filter.

The Comb filter is made by a 4th order filter with all the zeros in the unit circle and the pole in the Z-plot origin. This means unitary filter coefficient. The filter architecture is chosen, as already said, as Comb Filter in order to guarantee less hardware use and fast calculation. The

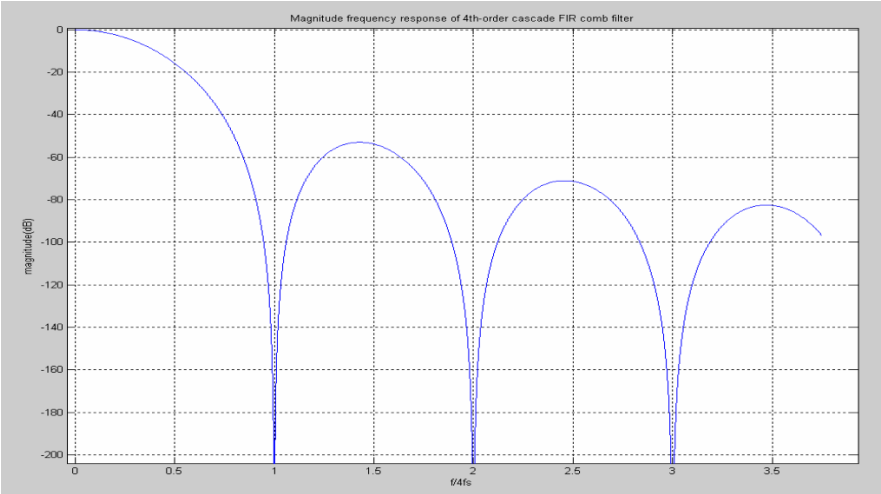

Figure 2.2: Magnitude frequency response of 4th order cascade FIR comb filter

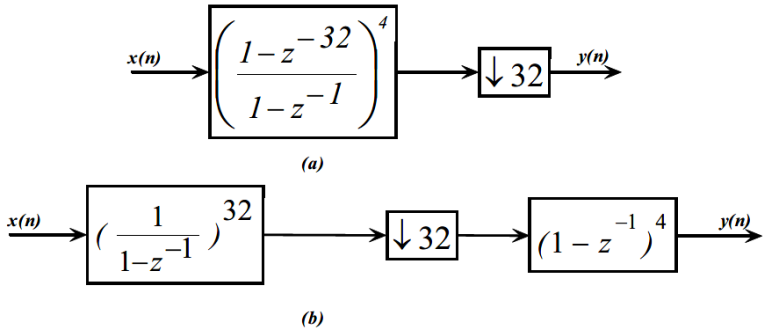

Figure 2.3: Figure (a) : comb filter followed by a decimation factor. Figure (b) : Comb filter divided by IIR stage and FIR stage with in between a decimation step. ERRATA CORRIGE : The exponent of the IIR part in the figure (b) proposed by [1] is wrong. The right order is 4.

output bit length is proportional to the decimation factor and the filter order. It is described by the formula :

$$H(z) = \left(\frac{1 - z^{-32}}{1 - z^{-1}}\right) \tag{2.2}$$

To represent the entire output range, 21 bits are necessary to avoid instability and distorsion.

$$(1 + 4log_2 32) = 21bits \tag{2.3}$$

The architecture shown in figure 2.3 is not efficient in a point of view of power consumption. The FIR stage operate at high sample rate with a long bit length. The combination of this two factors means that the power use is high. In order to reduce the power consump-

tion the decimation stage is moved in between of IIR and FIR part, using the second noble identity as show on the Appendix B. with this new configuration the FIR stage works with a lower sample rate and the power consumption will be reduced.

After the Comb stage a FIR filter is necessary in order to compensate the CIC passband drop and attenuate more on the stopband. The FIR is chosen as decimation filter with a lower decimation rate than the CIC. For this application the FIR is made by a 56-tap filter and it is symmetrical. It means that only 28 coefficient are necessary to store inside the DSP .

Furthermore , to compensate the DC component an high pass filter is necessary and for this reason, after the 2 filter, is designed an IIR high pass filter with the transfer function :

$$H(z) = \frac{1 - z^{-1}}{1 - \left(\frac{1}{256}\right) z^{-1}} \tag{2.4}$$

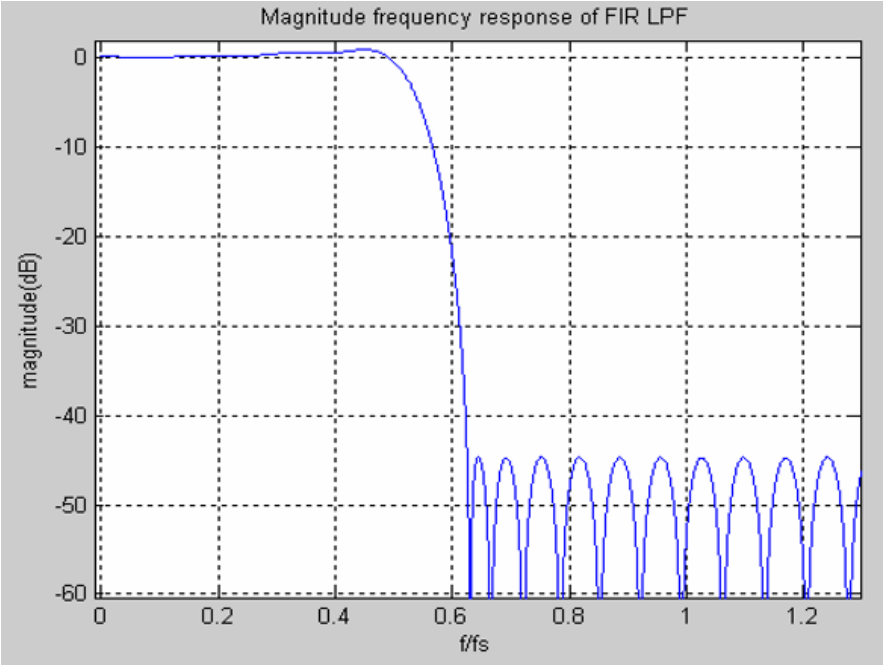

Figure 2.4: Magnitude frequency response of the 55th order FIR low pass filter proposed by [1] . The gain inside the pass-band has an oscillation near the bandwidth due to the zero position of the FIR transfer function. The stop band has a strong attenuation that the CIC filter can not provide.

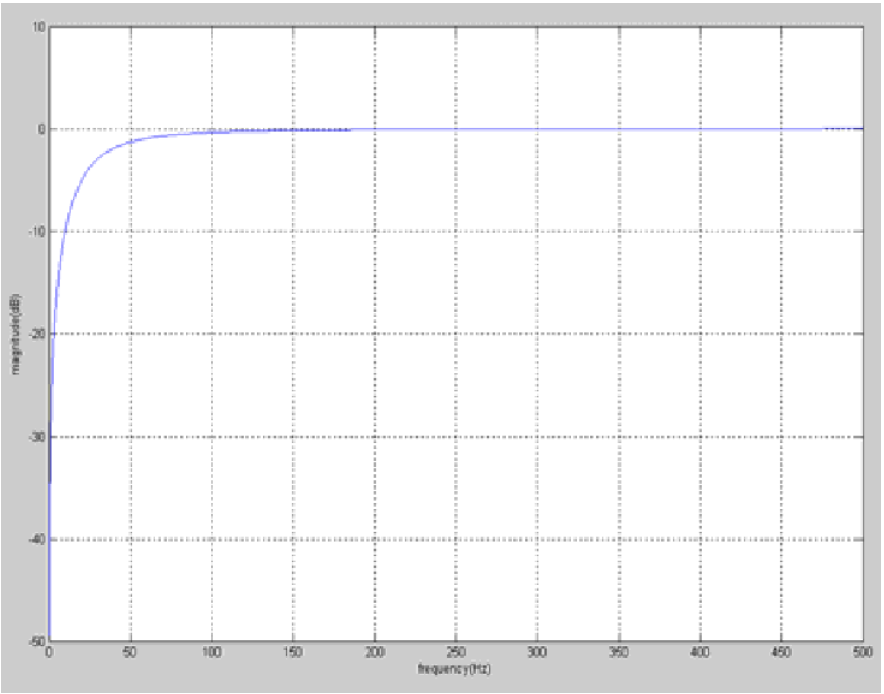

Figure 2.5: Frequency response of the High pass filter proposed by [1]

2.3.2 High Decimation Filters

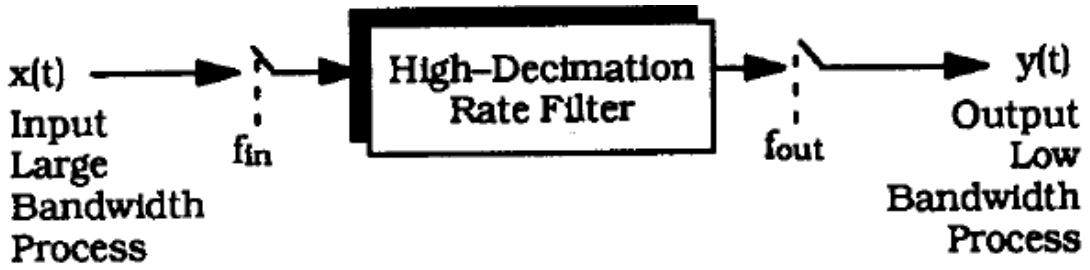

Figure 2.6: Decimation filter proposed by [3] . with a large bandwidth input and a low bandwidth output. The filter stage must down-sample and process the signal in order to reduce the sampling frequency and filter the signal.

Architecture of an efficient high-decimation rate filter for sigma delta application. The task of this filter stage is to decimate the input sample rate and filter out the unwanted frequency. An FIR used as decimation stage and filter stage is an inefficient method to process the signal due to the calculation complexity introduce by the FIR filter. The basic structure of an high-decimation filter is shown in figure 2.6. The filter stage process the signal with a filtering and decimation operations. The filter must has linear phase, in order to reduce the complexity of detection,decoding,demodulation operations after the filter stage (if necessary). A CIC architecture is the perfect solution to achieve : high decimation rate, linear phase and high stop band rejection . For example a FIR with linear phase and 120 dB of stop-band rejection is quite expensive to implement and it use a lot of mathematical operation to calculate the output. The CIC architecture use only a cascade of Integrator and Comb stage with an decimation stage in between. The CIC has linear phase whit an high stop-band rejection. The gain drop on a CIC architecture is more accentuated than the FIR version. To compensate this problem is possible to use an FIR filter designed for low sampling frequency to use after the CIC stage.

The figure 2.7 shown an example of CIC filter in order to downgrade the sampling frequency and filter the signal. The filter is made by 4 parts : the integration stages, the decimation part, the comb stages and the round block. The integration and comb stages are made as shown in the bottom diagram block, with a transfer function for each stage :

$$H_i(z) = \left(\frac{z}{z-1}\right)^n = \frac{1}{(1-z^{-1})^n} \tag{2.5}$$

$$H_c(z) = (1 - z^{-}R)^n \tag{2.6}$$

The decimation block with decimation value R is the responsible to downgrade the sampling frequency of the signal, using the second noble identity shown on the appendix B .The round stage must adjust the output bit length.

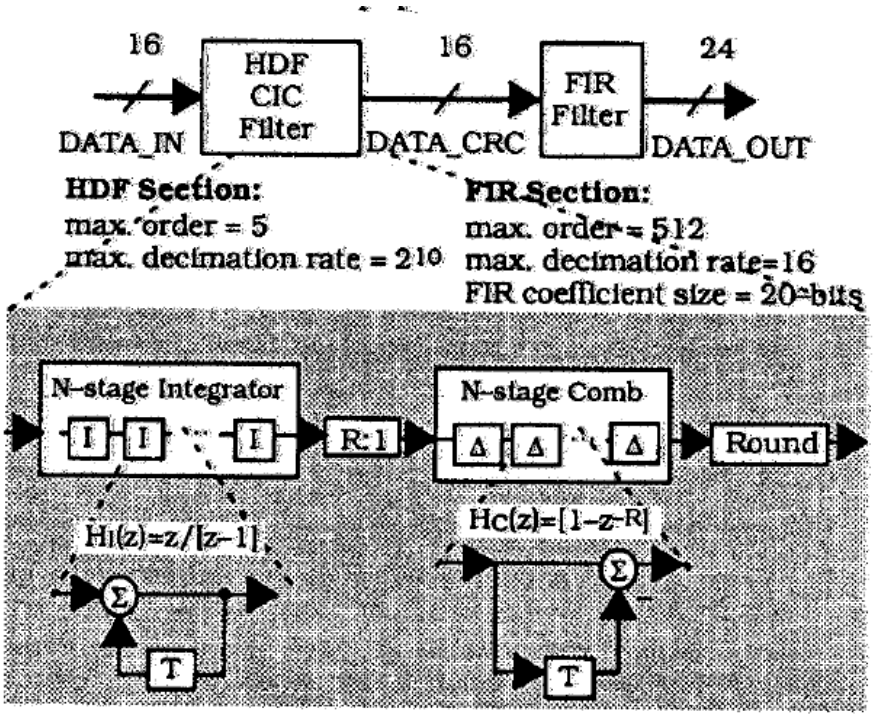

Figure 2.7: CIC architecture proposed by [3]. The CIC filter is made by 3 different part: Integrator stages, Decimation step and comb stage. The output can be rounded to be within a limited number of bits. This operation could be necessary due to the high CIC gain.

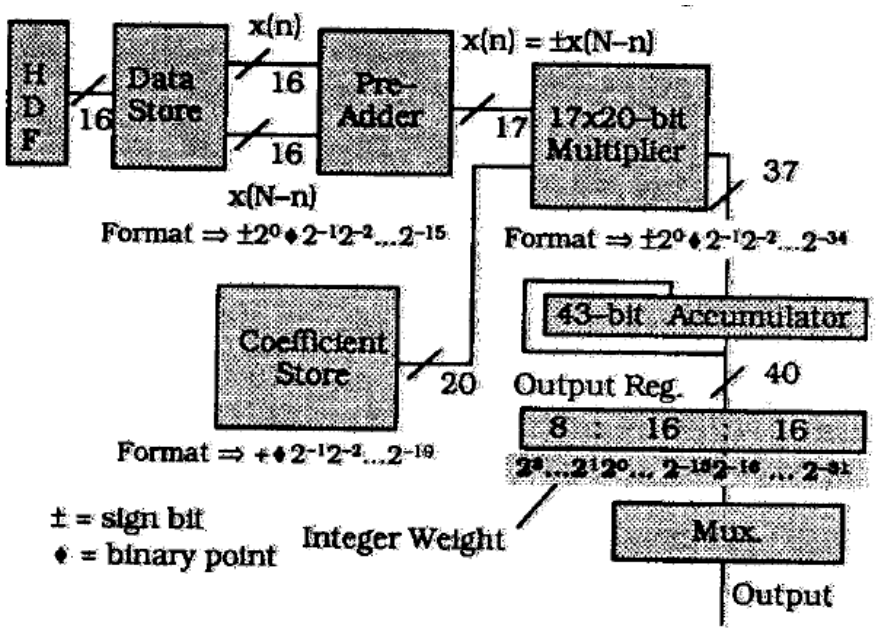

Figure 2.8: FIR architecture proposed by [3] . The multiplier block has a long bit length in order to calculate over a multiplication of 17 and 20 bits. This use a lot of area on chip.

The filter fir section is used to increase the stop-band rejection to the final output. The critical point is the operation frequency, if the FIR must works with high sampling frequency and high decimation rate, it will use a lot of hardware resource, a lot of power on chip and so it will not be efficient. The key point is to use the FIR after the CIC stage in order to operate with low frequency. In order to save some area on chip, the FIR must be symmetric. With the symmetry condition the filter coefficient to store will be half and the mutliply/accomulate operation will be N/2 + 1 as shown in figure 2.8.

3 Current Hardware Architecture

3.1 Overview

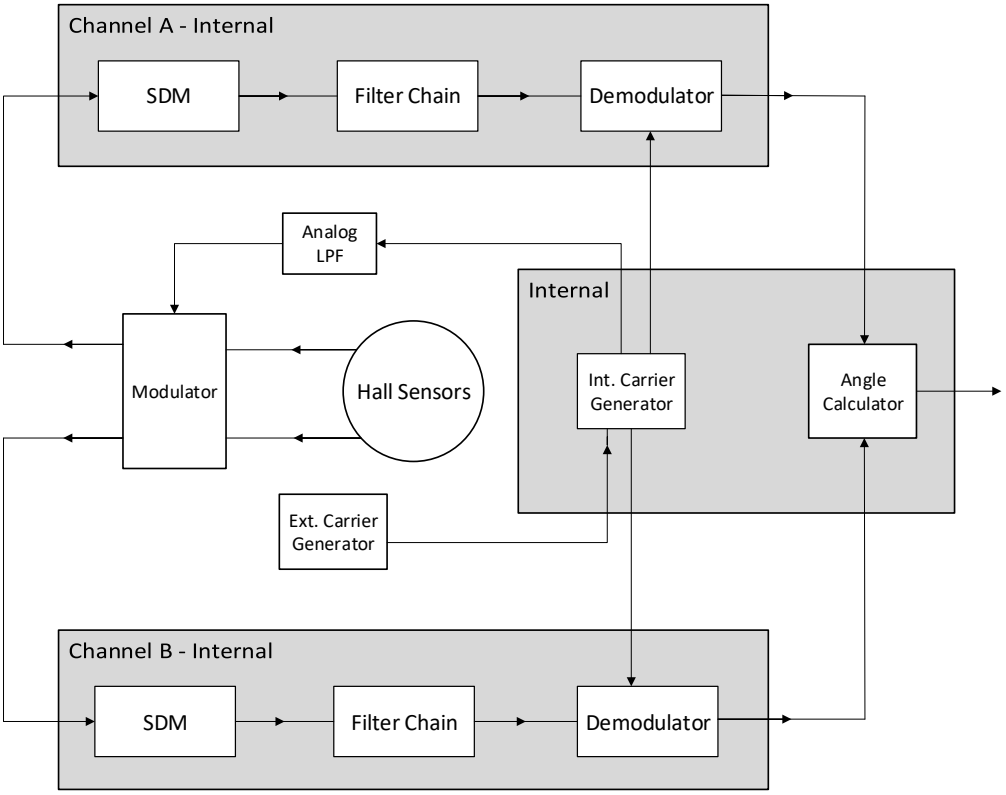

Figure 3.1: Block diagram of the resolver application

To measure the signal generated by the sensors, a Sigma-Delta ADC is used. Before the conversion is necessary modulate the payload signal. The purpose of the filter chain is to make sigma delta demodulation and AM demodulation. In other words, the filter chain must extract the payload signal from the modulated signal. The method to measure the quality of the hardware architecture is investigate the filter chain performance in terms of SNR. It is possible to keep in mind also the secondary task (but not less important) of the filter chain like as, down sampling frequency and bit growth of the output word. To guarantee the real time it is useful reduce the sampling rate at the output , in this way the micro-controller can handle the conversion result.The precision of the converter is a crucial characteristic, indeed the original SDM output has only 1 bit. The Sigma Delta in this application is of second order converter with a feed-forward , architecture and clocked in a range from 10 MHz to 40 MHz. This chapter analyses the performance of the current architecture, in order to set a general overview of the current performance to keep it in mind for the further investigations.

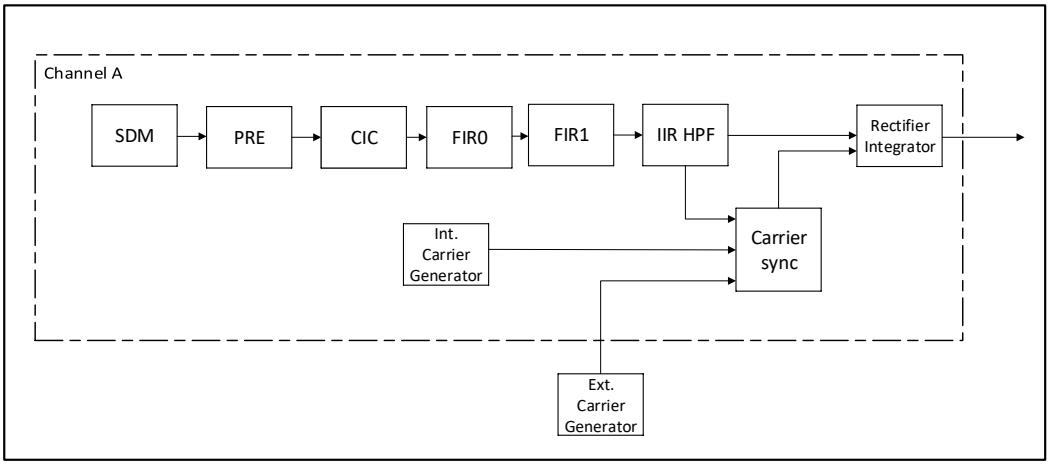

Figure 3.2: The figure represent the complete filter chain with all stages enable. The blocks from PRE to IIR are responsible for the filter part. The IIR HPF needs only to compensate the offset at the source. The carrier sync is designed to synchronize the carrier with the modulated signal. The carrier can be generated internally or can be provided by an external source. After the carrier synchronization and the offset compensation there is the rectifier and integrator to achieve an AM demodulation.

3.2 Prefilter

The SD output needs to be filtered and demodulated. As starting point it is possible to consider the cascade of SDM and a 3rd order CIC filter with high decimation ratio. The filter can achieve the decimation and attenuation task but it consume a lot power due to the high input frequency. The CIC integrator part must be clocked at the same SDM sampling frequency. The process can be improve with the introduction of a pre filter before the CIC filter and after the SDM . The pre filter could be implemented as a CIC filter or a finite state

machine , but its task is to reduce the sampling frequency by a factor of two. Since it is necessary only for the decimation, it is realized to be small as possible. The chosen order is 3 as the main CIC but it is shorted than the main filter stage. The pre filter can be represented as a FIR filter in order to study its characteristic

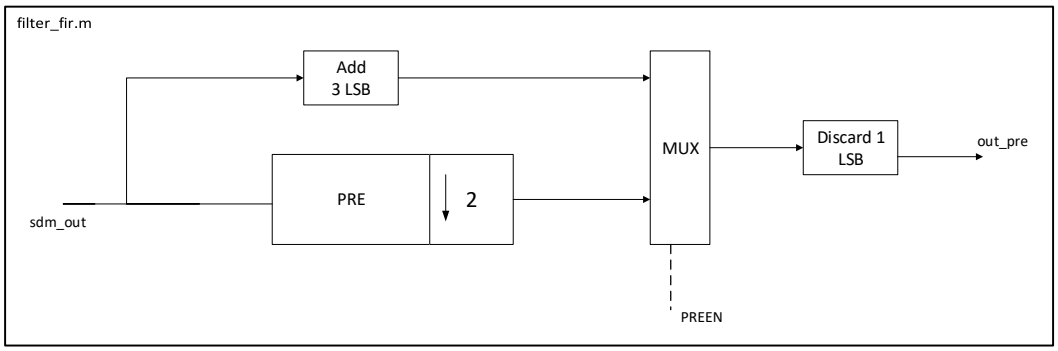

Figure 3.3: It is a 3rd order filter with fixed decimation factor by 2. It is possible to disable the filter with the flag PREEN. At the pre filter output the gain is the same no matter

3.2.1 Prefilter Transfer Function

It is useful to divide the sample rate by 2 before the CIC filter. This configuration is able to achieve high decimation factor with a small CIC decimation rate. The prefilter is made by a 3^{rd} order FIR filter with coefficients $[1\ 3\ 3\ 1]$. It means that is a convolution of 1^{st} order filters with transfer function $H_1(z) = 1 + z^{-1}$. The result of the convolution is a 3^{rd} order with transfer function $H_3(z) = 1 + 3z^{-1} + 3z^{-2} + z^{-3}$. If the number of coefficient is equal to the decimation factor filter, the frequency response is the tightest as possible. The filter chain has a finite bit width to use for mathematical calculation, it is important study the bit growth for each stage and for each sampling frequency.

3.2.2 Gain and Number of Bits

The minimum number of bits to represent correctly the output values is give by the formula:

$$1 + order \cdot log_2(decimation factor) = 1 + 3 \cdot log_2(2) = 4$$

bits. The theoretical gain of this filter is:

$$(decimation factor)^{Order} = 2^3 = 8$$

As shown in the table 3.1 is possible to find only 7 output values of the pre filter. The output values are calculated with 4 input samples $[x_0 x_1 x_2 x_4]$. The input values will be multiplied

1	3	3	1	Mux Output	Adjusted Output
1	1	1	1	8	4
1	1	1	−1	6	3
−1	1	1	1	6	3
1	1	−1	1	2	1
1	−1	1	1	2	1
−1	−1	1	1	0	0
1	−1	1	−1	0	0
−1	−1	1	−1	-2	-1
−1	1	−1	−1	-2	-1
−1	−1	−1	1	-6	-2
1	−1	−1	−1	-6	-2
−1	−1	−1	−1	-8	-4

Table 3.1: Output for all possible combination of input values

with the filter coefficients $[1331]$.

There are only 7 output values magnitude which are all even numbers therefore, to reduce the bit growth, it is possible to represent the output value with only 3 bits instead of 4. Using Matlab is possible to plot the filter magnitude as shown in figure 3.6 . The Band is wide, in according with the formula

$$BW = \frac{\frac{F_s}{2}}{3}$$

The DC gain is 18.06 dB. It means about 8 of decimal gain, as described before. (This is the theoretical filter gain, not the adjust gain).

3.2.3 Time Domain

The output waveform is sinusoidal but still shows a lot of influence from the quantization noise due to a wide transition band. The output need to be filtered again to attenuate the quantization noise. The figure 3.4 show this behavior.

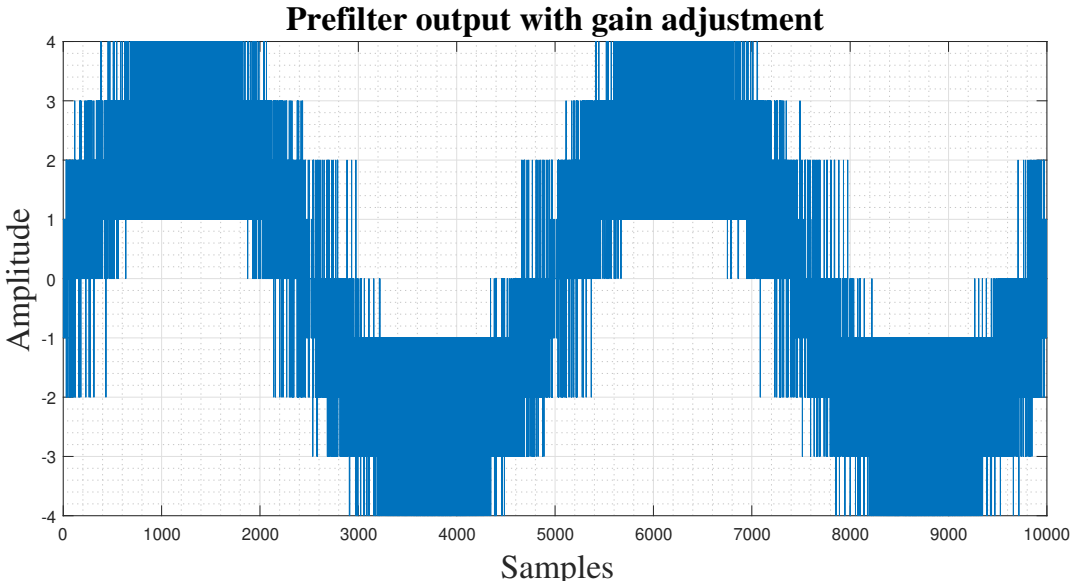

Figure 3.4: The input signal is a sine waveform with an amplitude of 5V. The output signal still has a lot of sigma-delta modulation. It is necessary another filter stage to delete the sigma-delta modulation. Another observation is that the number of samples for one period is the half of the original period length, in according with the filter decimation factor.

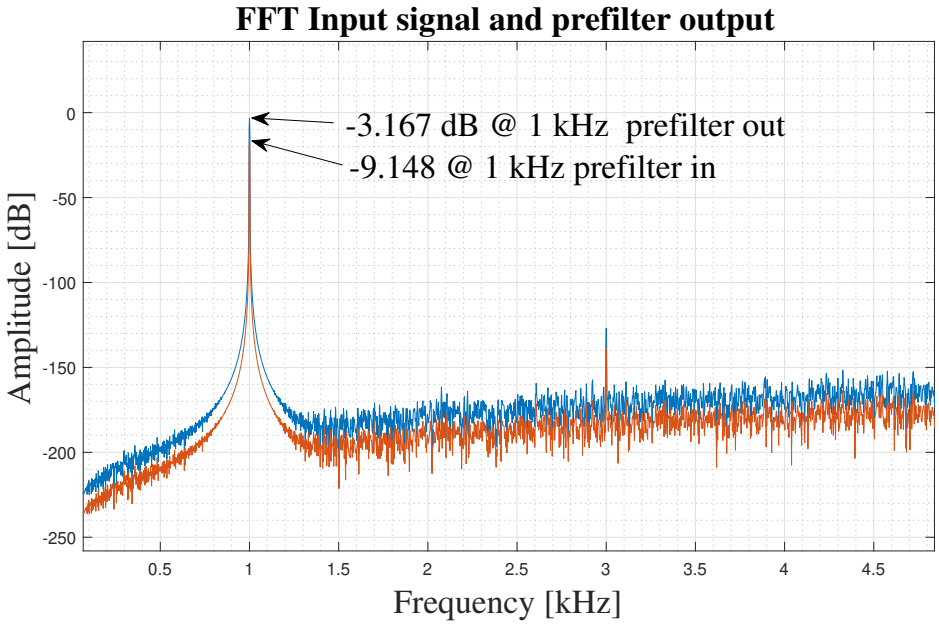

Figure 3.5: Pre Filter I/O

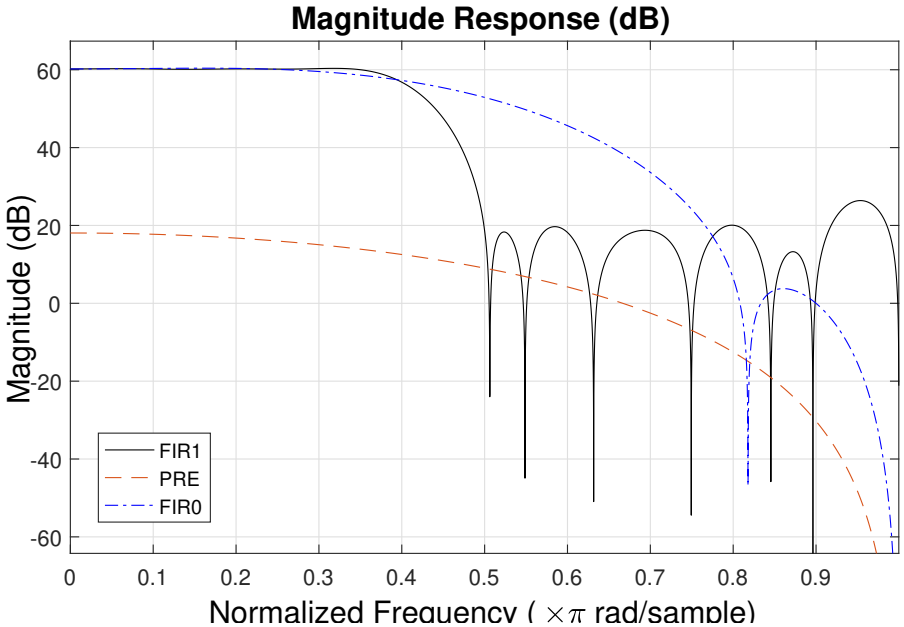

Figure 3.6: FIR and pre filters frequency response

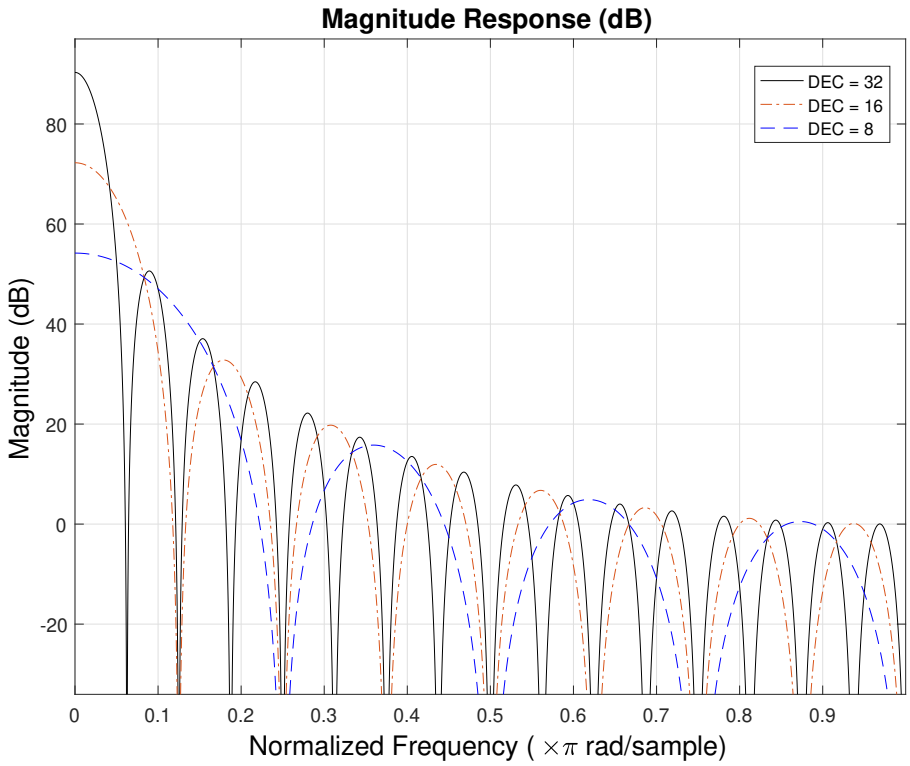

Figure 3.7: CIC frequency responses with different decimation factors. With a high decimation factor has a narrow pass-band in comparison with the lower decimation factor. The transition band is shorter for high decimation factors than for low decimation factors.

3.3 CIC Filter

It offer the most configurability with respect ofthe decimation factor. In this architecture the rangecan be from 4 to 512. In combination with the prefilter, a total decimation range from 8 to 1024 is achievable. The CIC filter is used as the main decimation filter for the simple and small implementation and use area requirement. A 3^{rd} order FIR filter required a several amount of basic operation with respect of its length. A CIC architecture can reduce the required operation. For a 3^{rd} CIC are required only three integration stages and three differentiation stages.

3.3.1 CIC Filter Transfer Function

The CIC transfer function is derived from the equivalent FIR transfer function

$$H_{FIR}(z) = \left(\frac{1}{M} \cdot \sum_{i=0}^{M-1} k_i \cdot z^{-i} \right)^n \tag{3.1}$$

with M equals to the filter length. The FIR filter just described is a moving average filter. If $M = DEC$ it can be shown that the same filter function can be achieved by one interpolator and one differentiation as shown in Appendix B. The CIC transfer function is:

$$H_{CIC}(z) = \left(\frac{1}{Dec} \cdot \frac{1 - z^{-Dec}}{1 - z^{-1}} \right)^n$$

Where n is the order of the filter and in this case is 3.
Dec is the decimation factor choose for the filter.
As described the bandwidth a CIC filter change with the decimation factor chosen. In figure 3.7 it is possible to see how the frequency response differs the bandwidth in dependence of different decimation factors. The gain is different between the two plots for this reason. The higher decimation factor has magnitude 70 dB, while the lower decimation factor has magnitude of 20 dB.

3.3.2 Decimation and Gain

Since the number of output bits of the CIC filter is given by the formula:

$$B_{in} + order \cdot log_2(Dec) \tag{3.2}$$

It becomes clear that a higher decimation results in a bigger gain. In order to guarantee the correct representation, it is necessary calculate the bit width for each gain values. Using the formula 3.2 it is possible to obtain a range from 9 to 30 bits. The bandwidth changes with

the decimation factor chosen. The empiric formula to calculate the bandwidth is:

$$BW = \frac{\frac{F_s}{Dec}}{3}$$

Normalizing the bandwidth edge, the minimum bandwidth achieve is : $0.005859 \cdot F_s$ while the maximum bandwidth is $0.75 \cdot F_s$

Since the CIC gain can be very big due to big decimation rate, the number of the output bits must be reduced. In this application the maximum output value is 25000. This value is called full scale value (FSV)). In order to achieve this FSV the output of the CIC has to be scaled. This scaling is done with the help of a bit shifter. AA bit shifter is more favorable in comparison to a multiplier due to the smaller area. The number of bits the CIC output must be shifted can be calculated by the formula:

$$N_{bitShift} = \lceil log_2 \left(\frac{2 * FSV}{G_{SD_{-3dB}} \cdot G_{PRE} \cdot (Dec)^3} \right) \rceil$$

Where $G_{SD_{-3dB}} = 0.6974$ is the gain of the sigma delta modulator at the -3 dB input value and G_{PRE} is the gain of the prefilter. The output values are multiplied by $2^{N_{bitShift}}$ to achieve the full scale of 25000. The problem with this method is the rounding the number of bits. To fix the problem it is necessary calculate how much is the error and derive a coefficient to multiply with the adjusted output to keep the error as small as possible.

$$Error = \lceil N_{bitShift} - log_2 \left(\frac{2 * FSV}{G_{SD_{-3dB}} \cdot G_{PRE} \cdot (Dec)^3} \right) \rceil$$

The result from the formula must be multiply by the chosen numerical representation, for example 4096.

3.3.3 Time Domain

As shown in figure 3.8 the CIC outout waveform is more clear than the prefilter output, this is because the CIC filter has more narrow bandwidth due to having a decimation factor of 16. Increasing the filter decimation helps to improve the sigma delta demodulation. It possible to see that the maximum CIC output value is greater than the prefilter output value.According to the bit growth formula 3.2, the CIC filter needs more bit width to represent the output value due to an increase of the filter gain. It is necessary keep the maximum CIC output value below the FSV and for this reason is emphasis that is necessary to adjust the filter gain with a dedicated stage after the comb filter.

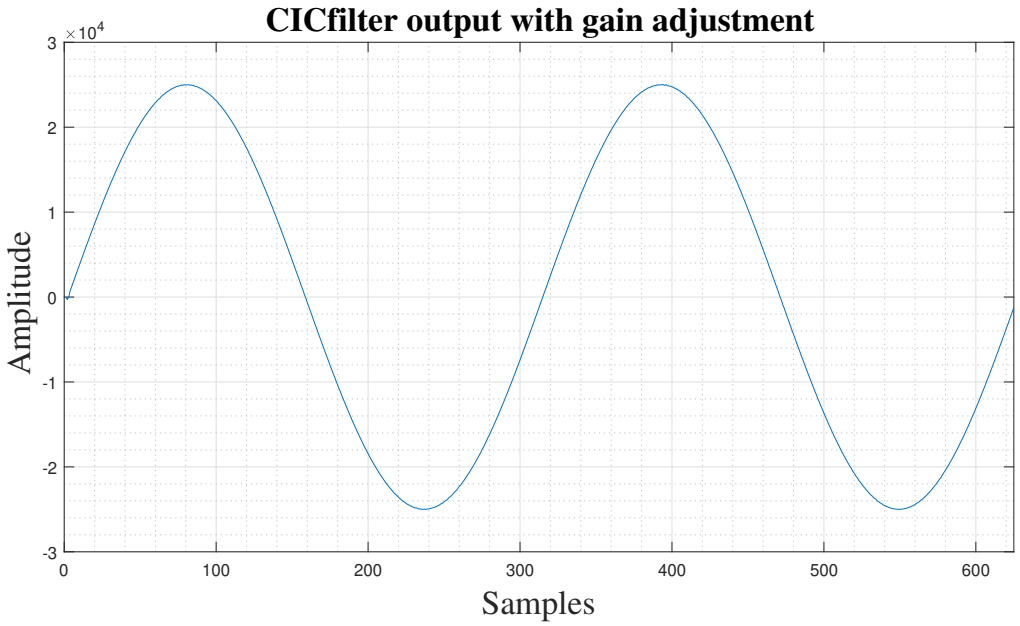

Figure 3.8: The shape is very clear, there is no sigma-delta modulation inside. The samples per period are less than the prefilter output as expected. The decimation factor in this case is 16, with a modulator sampling frequency of 10 MHz and 1 kHz of payload frequency. To test the filter a pure sinewave is used. The amplitude is higher than the maximum input amplitude, regarding with the filter gain formula.

3.4 FIR Filters

There are two filter , FIR0 and FIR1. The differences between the two filters are the decimation factor and the coefficient numbers. The FIR0 filter has a fixed decimation factor of 2. The FIR1 filter has two decimation factors : 1 or 2. Both filter can be bypassed. The filters are quite different: the FIR0 has 8 fixed coefficients and the FIR1 has 28 and both are symmetric. By using a symmetric FIR only half coefficient has to be stored. The FIR0 can be described as :

$$H_0(n) = \sum_{i=0}^{N_0-1} a(i)x(2n-i) \tag{3.3}$$

The FIR1 can be described as :

$$H_1(n) = \sum_{i=0}^{N_1-1} b(i)x(2n-i) \tag{3.4}$$

with $N_0 = 8$ and $N_1 = 28$.
Moreover, it is possible to study the frequency response of both filter in the figure 3.6. Both filter have the same bandwidth, but the attenuation in the stop band is significant different.

The filter FIR1 has more attenuation in the stop band, and the FIR0 has less performance in that portion of bandwidth. This is useful to remove more noise at high frequencies. It is important to keep it in mind that the figure 3.6 has as x-axis the normalize frequency. The true filters bandwidth have different cut-off frequency due to the different decimation ratio.

3.5 Offset Correction

In order to compensate the offset, n high pass filter has been implemented. This high pass filter is designed to filter out the DC component. The architecture of this filter is an IIR 1^{st} order . The transfer function is :

$$H_{hpf}(Z) = \frac{1 - z^{-1}}{1 + (2^{2\alpha-16} - 1)\, z^{-1}} \tag{3.5}$$

α is a configurable parameter to change the cut of frequency as shown in figure 3.9 and table 3.2.

α	Cutoff frequency -3dB
1	$1 \cdot 10^{-5} \cdot f_d$
2	$4 \cdot 10^{-5} \cdot f_d$
3	$16 \cdot 10^{-5} \cdot f_d$
4	$62 \cdot 10^{-5} \cdot f_d$
5	$25 \cdot 10^{-4} \cdot f_d$
6	$1 \cdot 10^{-2} \cdot f_d$
7	$4 \cdot 10^{-2} \cdot f_d$

Table 3.2: Cutoff frequencies for each value of α. The parameter f_d is the sampling frequency at the high pass filter.

3.6 Rectifier and Integrator

The stage made by Rectifier plus Integrator is fundamental to demodulate the input signal. To cancel the carrier component is necessary to integrate a certain number of carrier period. The carrier cancellation is done by a 1^{st} order CIC filter used as integrator. The integration window length must be adjusted with the carrier signal with a certain frequency and the data rate at the integrator stage. The integrator must include features like sample shift in order to discard a possible transient time in the modulated signal.

3.6.1 Rectifier

The rectification part is fundamental to demodulate the input AM Signal. It is done with the carrier sign information. In order to demodulate the payload signal it is necessary to

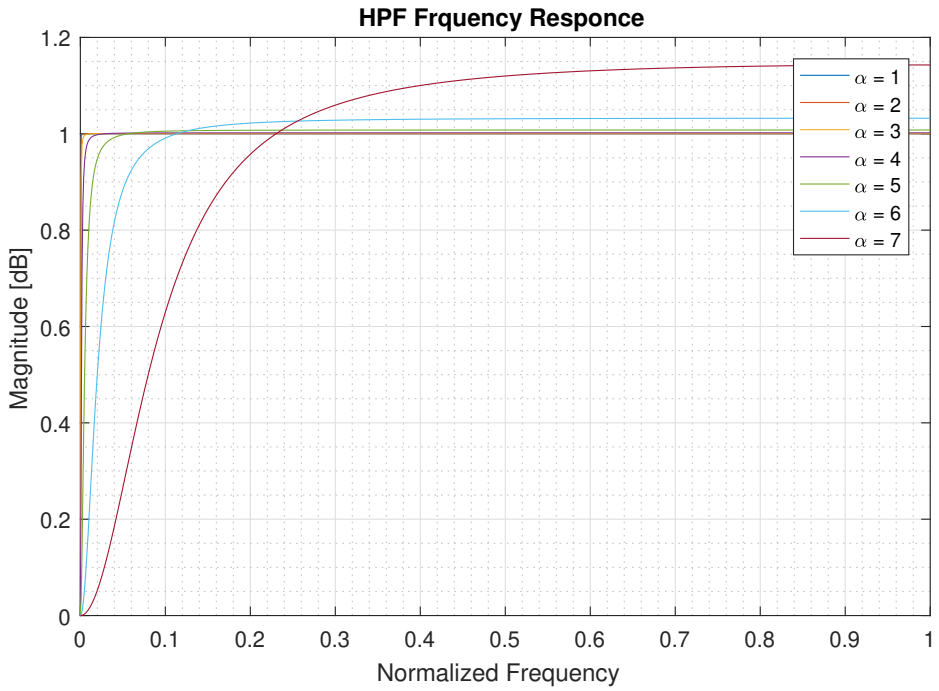

Figure 3.9: The IIR high pass filter frequency response.The cutoff frequency change by configuring the parameter α

extrapolate the carrier sign, therefore is sufficient to multiply the carrier sign with the input AM signal. In order to compensate the filter chain group delay, it is also possible to delay the carrier signal or the AM signal. Moreover, it could be necessary to discard some sample to delete the filter chain transient. This two adjustments are important to perform a better demodulation. It is important to remember that a multiplication between two signals is equal to shift the signal component in the frequency domain, indeed with the carrier sign it is possible to shift the AM signal spectrum to the baseband and after this operation is possible to integrate that signal and extract the payload signal.

3.6.2 Integrator

The integrator block is the last and the most fundamental block for the carrier cancellation. It must integrate the rectifier output in order to filter and extract the payload inside the AM signal. The integrator is of first order and provides an integration over NVAL samples. It also introduces another decimation in the filter chain. This is because the integrator is made of a CIC architecture with order one and with a decimation factor of NVAL. It is important to specify what makes the difference between a CIC filter and an integrator made with a CIC filter. In order to achieve the demodulation behavior, a CIC filter must has the output sampling rate equal to the carrier frequency or must be a multiple of a carrier period. In other words, the CIC1 filter must have the integration window equal to the same carrier period

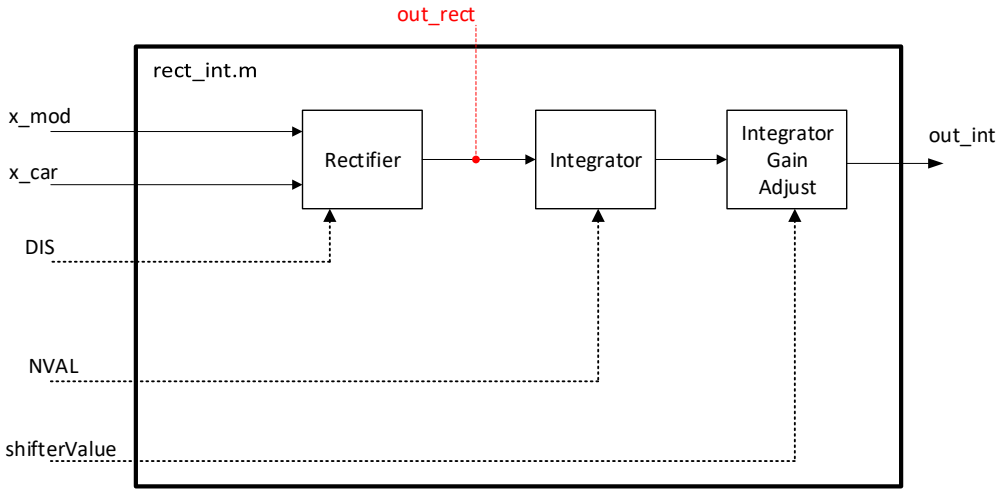

Figure 3.10: Rectifier and integrator chain overview

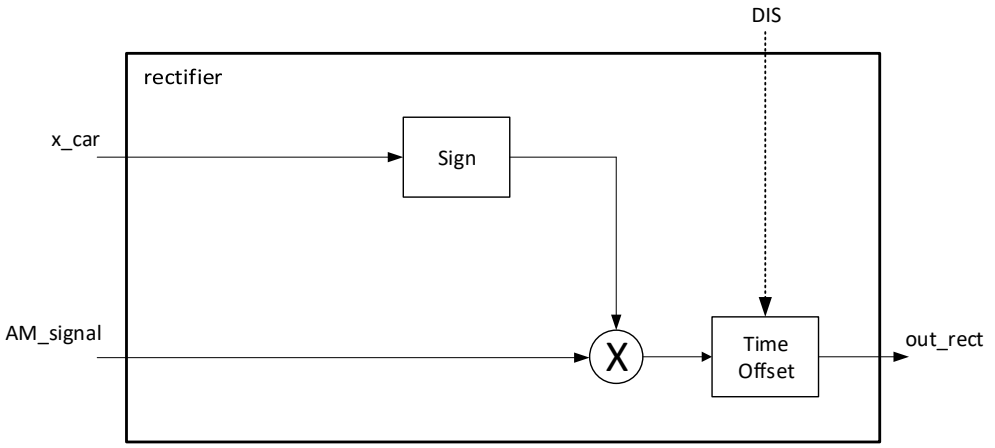

Figure 3.11: The input signal is multiplied by the carrier sign. After that it is possible to discard some initial samples to avoid include the transient into the resolver application. The decimation factor before the rectifier is necessary to adapt both signal to each others

samples. There is a lot of possibility for the value of NVAL since it is possible to integrate the signal over one carrier period or more than one. The performance of the Integrator changes with the NVAL values. For a first investigation was choose to fix the integration window over one carrier period. It means that the parameter NVAL is equal to the number of sample in one carrier period.

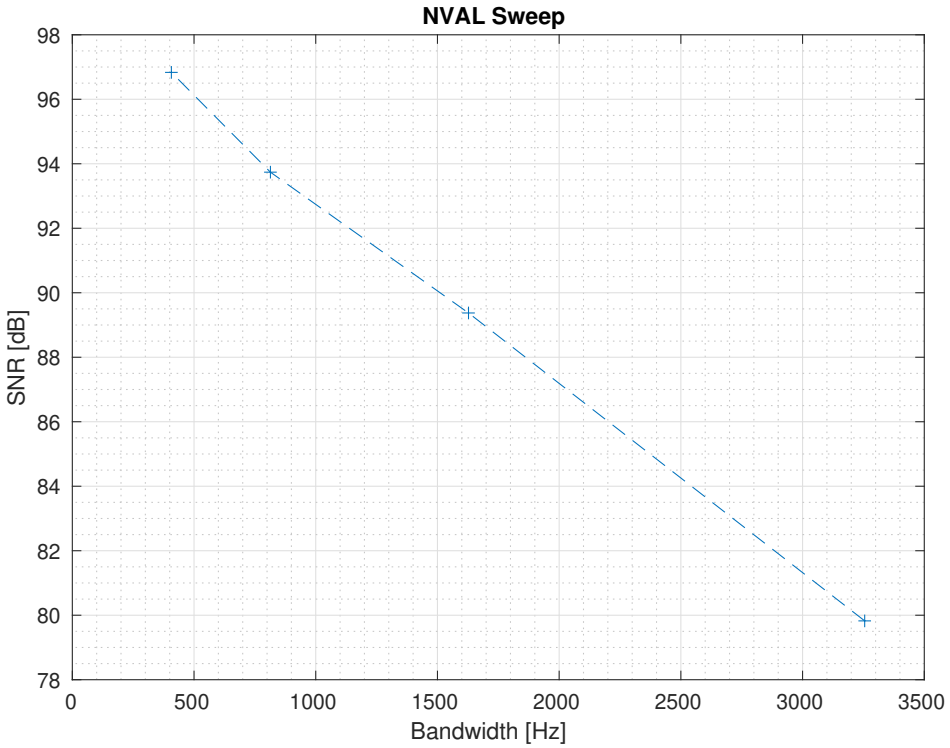

Figure 3.12: The figure represent the integrator performance for a different NVAL values. The modulator sampling frequency is 10 MHz and the CIC decimation factor is fixed to 16. The PREfilter , FIR0 and FIR1 are enabled. The carrier frequency is adjusted to fill the integration window

3.7 Complete Filter Chain

It is necessary to analyze the overall frequency response of the filter chain. The frequency specification to observe is described in the following table 3.3 :

The comparison between the filter chain frequency response and the frequency specification is shown in the figure 3.13 . The large stop-band attenuation is given by the FIR0 and FIR1 while the high decimation rate is given by the 3^{rd} order CIC filter. Using the FIR filters, it is necessary in this application to specify the ripple limit for the pass-band values. In this case the possible ripple in the passband must be within $+/-1\%$. The frequency response

Normalized Frequency Range	Attenuation
$0.5 \longrightarrow 1 \cdot f_d$	$\geq 40[\text{dB}]$
$1 \longrightarrow 1.5 \cdot f_d$	$\geq 45[\text{dB}]$
$1.5 \longrightarrow 2 \cdot f_d$	$\geq 50[\text{dB}]$
$2 \longrightarrow 2.5 \cdot f_d$	$\geq 55[\text{dB}]$
$2.5 \longrightarrow \frac{OSR}{2} \cdot f_d$	$\geq 60[\text{dB}]$

Table 3.3: The attenuation required for this application is shown. All the frequency spans are normalized to f_d , the output sampling rate.

specification for the high pass filter is about $f_{-3dB} = 10^{-5} \cdot f_d$ and the exactly value depends on the offset compensation chosen. It is important to observe in the figure 3.13 that without the FIR0 and the FIR1 enabled the frequency specification is not met.

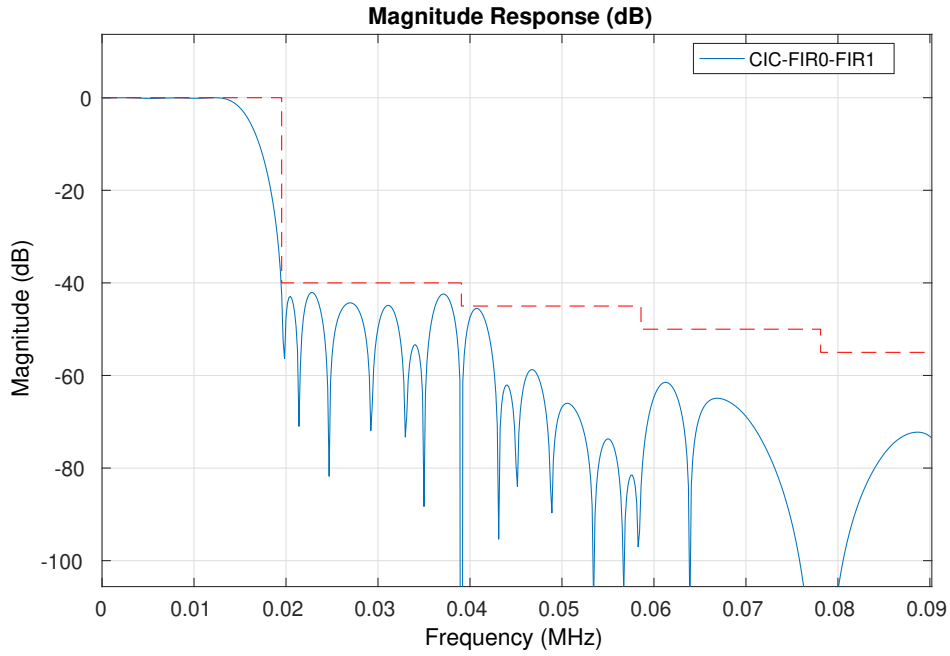

Figure 3.13: The boundary conditions on the frequency domain and the allover frequency response are depicted. The specification has been met. The modulator sampling frequency is 10 MHz. From the blue line, it is possible to see that the CIC attenuation is strong very far away from the bandwidth limit, around 0.08 MHz. The FIR0 and FIR1 are necessary to increase the attenuation in the stopband.

4 Reorganization of the filter chain

4.1 Architecture Change

Even though many parameters of the filter chain are configurable, the hardware implementation limits the functionality and therefore, also possible applications. In order to provide more flexibility, as many hardware filters as possible shall be replaced by software, running on a DSP. However, it has to be considered that for some applications the filters are controlled by quite dynamic signals which shall not be transmitted to the DSP if feasible. Therefore, it will be analyzed if a reorganization of the filter chain might help to overcome this problem. The targeted functionality for this investigation is the carrier canellation in a resolver application where CIC filter, IIR filter, rectifier and integrator are involved in the signal processing. The most dynamic part is the rectifier which controlled by a carrier synchronization unit and is placed between IIR filter and integrator. This is a disadvantageous position, if the software shall implement the IIR filter and the integrator. Therefore, it will be investigated if the rectification can be realized in front of the CIC filter without impact on the signal precision because the CIC filter shall be implemented in hardware anyway in order to reduce the data rate at the input of the DSP. To this end in the beginning of the next section the current filter chain performance will be analyzed with respect to SNR performance. This will set the benchmark for the investigation of the different architectures which shall be examined.

4.2 Original Architecture : Settings and Performance

Initially, the SNR performance of the filter chain will be analyzed with respect to the resolver setup. Since the usage of the FIR filters is optional, two configurations (one with and one without FIR filters) will be opposed to each other. But usually the configuration without FIR filters is preferred for the resolver application because the FIR filters will considerably increase the group delay of the filter chain. Since the frequency response of the filter chain

depends on the overall decimation, in the configuration without FIR filters, the integrator will accumulate four times more values in order to create a result. This adjustment balances the overall decimation rate of the FIR filters which is 4. The IIR filter will be disabled in both configurations as well because it is used in the application only for offset compensation but for the reason of simplification, further investigations will not consider an offset. Figure 4.1 shows the SNR graph for the different configurations measured at four different points. Lower bandwidths will be achieved by higher decimation rates and higher bandwidths by lower decimation rates. The influence of the FIR filters is clearly visible for higher bandwidth settings. This can be compensated partly by increasing the decimation rate of the CIC filter by 4 instead doing this at the integrator because the CIC filter has a three times higher order than the integrator. More details about the characteristics of the CIC and FIR filters will be shown later on the basis of the frequency responses of these filters. It should be considered that the lower SNR at a certain bandwidth might limit the performance of the modulator because the equivalent number of bits which is coded in the output signal decreases with SNR at a certain bandwidth. That is, it should be avoided that the modulator has a higher resolution than the filter chain. The estimated number of bits (ENOB) can be calculated for example for a SINAD of 89dB and a bandwidth of 6.2 kHz as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02} = 14.49 \rightarrow 15bits \tag{4.1}$$

The frequency responses of the different filter chain setups show the reason for the big influence of the FIR filters. Considering a certain passband (range from 0 MHz until first vertical dashed red line in figure 4.2) and stopband (remaining range after passband) which is met when the FIR filters are enabled, both band parameters will be violated when switching off the FIR filters. This is clearly visible in figure 4.2. The reason is that the CIC filter has a less sharp slope compared to the FIR filters. But the FIR filters require calculations which account to a higher group delay. It is important to mention that for this evaluation the CIC decimation factor was increased by a factor of 4. The reason for this change is described in Appendix A and it was done in order to keep the same Nyquist frequency for boith filter chain setups, so that a similar filter behavior can be compared. It is impossible to reach the considered passband and stopband characteristics by any CIC filter setting when the FIR filters are disabled. But this does not mean that such a configuration is useless for the resolver application. Especially, due to the lower group delay it is better for real time applications and therefore, considered benchmark for the reorganization of the filter chain. After this first evaluation with respect to the FIR filters the parameters for the CIC filter and integrator will be defined as basis for further investigations. Those parameters are: the CIC_3 decimation factor and the number of values to be accumulated by the integrator (NVAL). The settings are shown in the table 4.1. They all will produce the same output data rate which is important for the application.

After this first evaluation if is possible to reduce the chain complexity , in order to proceed with further investigation. Considering the reduce filter chain the main settings are :

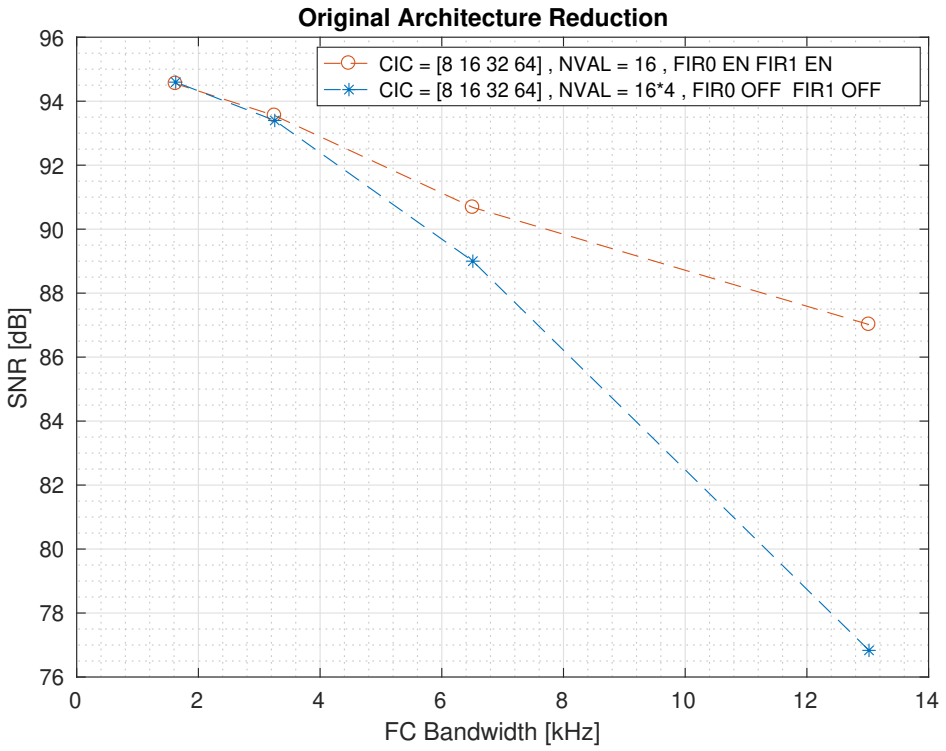

Figure 4.1: The figure represents the output SNR with of the different filter chain configurations. The blue line shows the filter chain with FIR filters, the red line shows the configuraiton without FIR filters. The bandwidth configurations fo the filter chain are same for both cases. As mentioned in Appendix A, this is a comparison of type 1.

CIC3 decimation factor and NVAL integration factor. They can be the first point to start the investigation. The settings are shown in the table 4.1.

	Setup 1	Setup 2	Setup 3
CIC3 sweep	CIC = 8 NVAL = 4*16	CIC = 16 NVAL = 16	CIC = 32 NVAL = 4*16
NVAL sweep	CIC = 16 NVAL = 4*8	CIC = 16 NVAL = 4*16	CIC = 16 NVAL = 4*32

Table 4.1: The table report the chosen settings in order to explain the behaviour of this filter cascade. The graphical result as shown in the figure 4.3. The settings respect what was said on the Appenx A, it is a type 1 comparison

The figure 4.3 shown two different sweep. The blue line represent the sweep of the CIC decimation factor, while the red line represent the sweep of the integration window NVAL with a fixed CIC value. It is possible to see that for high bandwidth value the SNR performances are different. The filter chain with fixed CIC value (fixed to 16) is the most performing solution. This is because the CIC is a 3^{rd} order filter and the integrator is a 1^{st} order filter. The CIC3 represented by the red line has the decimation factor greater that the CIC3

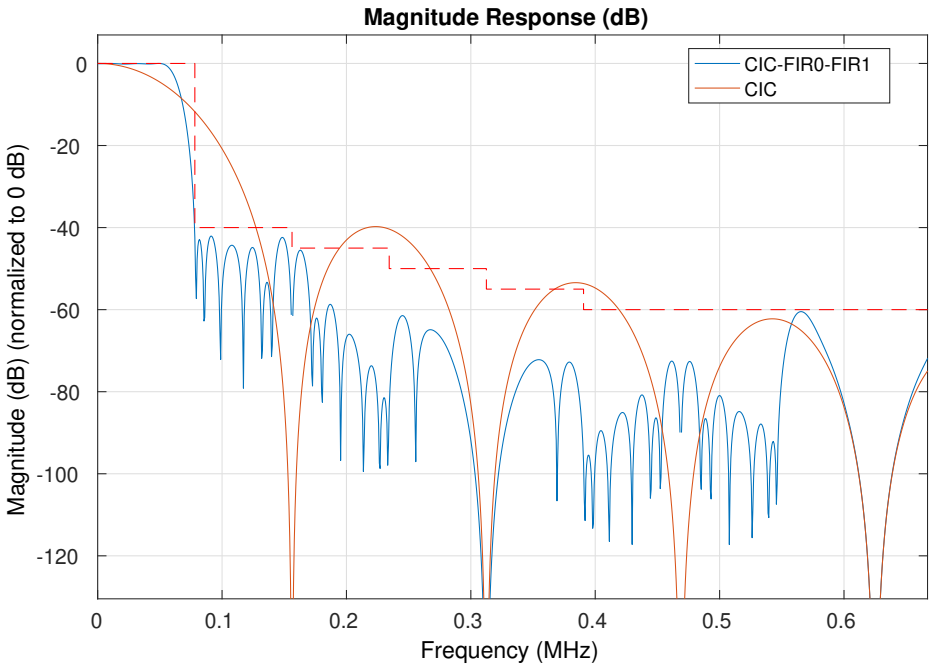

Figure 4.2: In this figure is possible to observe the specification violation in the frequency domain. Without the FIR filter the freq. response is not so sharp as before, and for this reason, with only the CIC filter is not possible to achieve the original performance. The comparison is a type 1 as describe on the appendix A.

filter represented by the blue line. The stop band for the red line is more accentuated that the other one, for this reason there is less noise on the output signal. After the merge point the situation is the opposite one. This is because the integrator with a high NVAL value can not compensate a CIC with high decimation factor, for this reason the NVAL sweep has less performance than the CIC sweep in this frequency range.

Another useful investigation is on the behaviour of the integrator with an integration window over 2 or more carrier periods. To achieve the investigation there is two possibilities: changing the length of the integration window, keeping the same carrier frequency or changing the carrier frequency and keeping the same integration window length. The figure 4.14 describe two different investigation. The red line is the simple NVAL sweep with a variable carrier frequency. It means that the red line represent the integration of 1 carrier period with different integration windows or value of NVAL, for each plotted point. The blue line is different. The carrier frequency is fixed for each integration windows. This method emphasize the performance increasing with only an integration window change. There is an improvement on the SNR values, but this is normal due to the bandwidth decreasing for high NVAL values. This first method doesn't describe the truth behaviour for a two or more carrier period in one integration window. To highlight only the integration over more periods it is

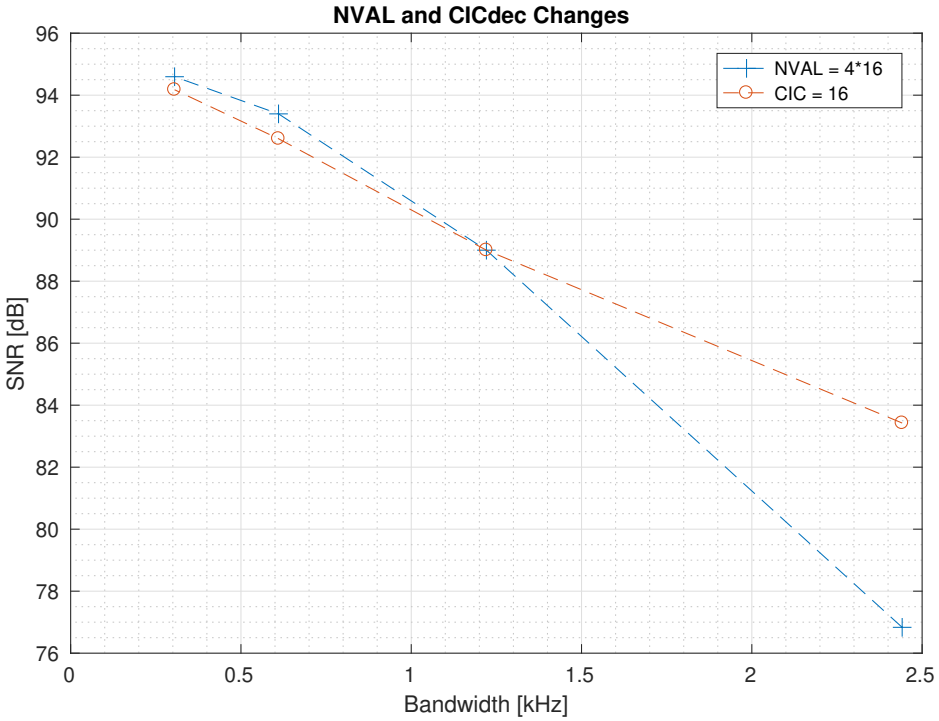

Figure 4.3: The figure represent the performance with the change of the two main parameters. It is possible to see that the CIC3 filter has more influence on the overall performance, this is because is a $3rd$ order filter while the integrator is only a first order filter. The settings are more o less the same for both simulation: Modulator sampling frequency 10 MHz and the carrier frequency is adjusted to fill one integrator period. With the CIC3 sweep, the NVAL value is fixed to 16, while with the NVAL sweep, the CIC3 value is fixed to 4*16 according the type 1 comparison explained in the Appendix A.

necessary fix the integration window length, fixing the parameter NVAL. To integrate more periods it is necessary to change the carrier frequency and keeping the same value of NVAL.

The figure 4.16 represent the output performance of the reduced filter chain. The expectation is to find an increase of SNR with integration window over 2 or more carrier periods. The result doesn't prove the expectation and in addition the performances are going to the opposite direction. In order to understand the reason of this unexpected behavior it is necessary know if it is proportional to the value of NVAL chosen. The figure 4.15 represent four investigation with different NVAL values. It is possible to see that the unexpected behavior is common for each line and it doesn't depend to the NVAL values. The reasons to explain this behavior must be found somewhere else.

As starting point is important to keep the configuration $NVAL = 16$ as reference and start to analyze the integrator output spectrum it means a carrier period made by 16 samples. The figure 4.4 show the output spectrum with two different configurations. The red line has harmonics component and more noise power. Moreover, it is possible to see with the

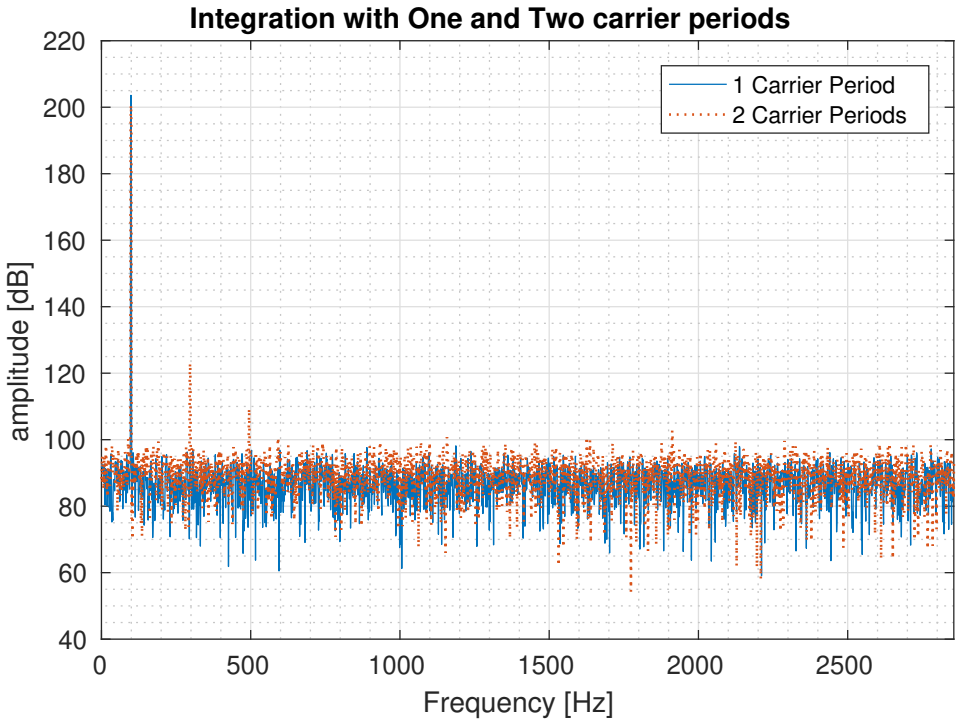

Figure 4.4: The figure represent the output signal spectrum for two set-up. It is possible to see that the red line (integration over 2 periods) has harmonics component while the blue line don't. This is a first reason for the SNR reduction. It is possible to see that also the noise floor is different. The red line has more noise power than the blue line

figure 4.5 that also the signal amplitude decrease. The amplitude effect is easy to explain, it is due to the CIC gain drop. Indeed, if the carrier frequency is double , it means that the correspondent gain is lower due to the near position with the cut-off frequency. With this results is difficult to explain why the noise power increase with an integration over 2 carrier periods. In order to clarify the situation it is necessary start the investigation from the begin of the filter chain.

The figure 4.7 represent the carrier spectrum. It is possible see that there is not so many changes regarding the noise power, and for this reason the increment of noise level must be find somewhere else. The next step is consider the modulator as possible noise source.

The figure 4.8 represent the modulator output spectrum. From the figure in possible to see that also the modulator doesn't introduce any additional noise for a different carrier frequency. The red line has the harmonics component higher than the blue line, this explain why it is possible to see harmonic component at the integrator output with an integration over two carrier periods. The reason for this additional noise must be found somewhere else.

The next step to analyse is the CIC output. It is possible to consider the PRE filter (that it is enabled) and the CIC filter together as one filter stage. The CIC output spectrum is

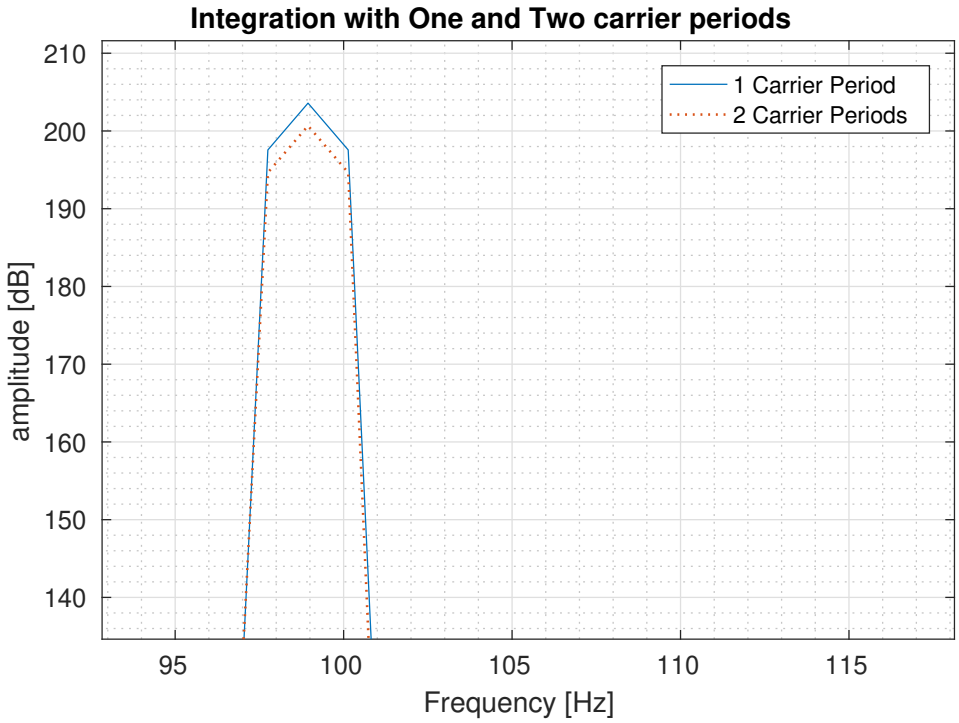

Figure 4.5: The zoomed figure can show that also the signal amplitude change for a different carrier frequency. The integration over 2 periods amplitude is lower than the blue one.

shown in the figure 4.9. It is possible to see that neither the filter stage is the responsible of the additional noise. The noise power is the same for both line : red and blue . The harmonic component amplitude are more or less the same, the red line (integration over 2 periods) has harmonics amplitude greater than the blue line, but this is already explained before. At this point the next step is to analyse the rectifier output signal.

The figure 4.10 represent the rectifier output spectrum. It is possible to see that the noise power in greater than the case with only one carrier period as integration window. The rectifier stage , in some way, causes a noise increment. After found the source, the next step it is to understand the problem and if there is a solution to fix it. Analysing the time domain is possible to get more useful information about the problem.

The figure 4.11 represent the time domain signals. It is possible to see that the blue line is wrong for one sample for each half period. The last half sample period has always the sign wrong. The wrong samples contribute to add noise during the rectification.

It is not possible to compensate the error because if the carrier will be delayed by 1 sample , the wrong sample will be at the begin of each half period. The problem is caused because it is necessary a time shift that can not met with 1 sample step. It should be necessary a delay of 0.5 sample. To prove this fact it is possible to delay the carrier for 3 samples and for 1 sample. The final result is even worst as shown in figure 4.13. The carrier delayed by 1 sample, miss the

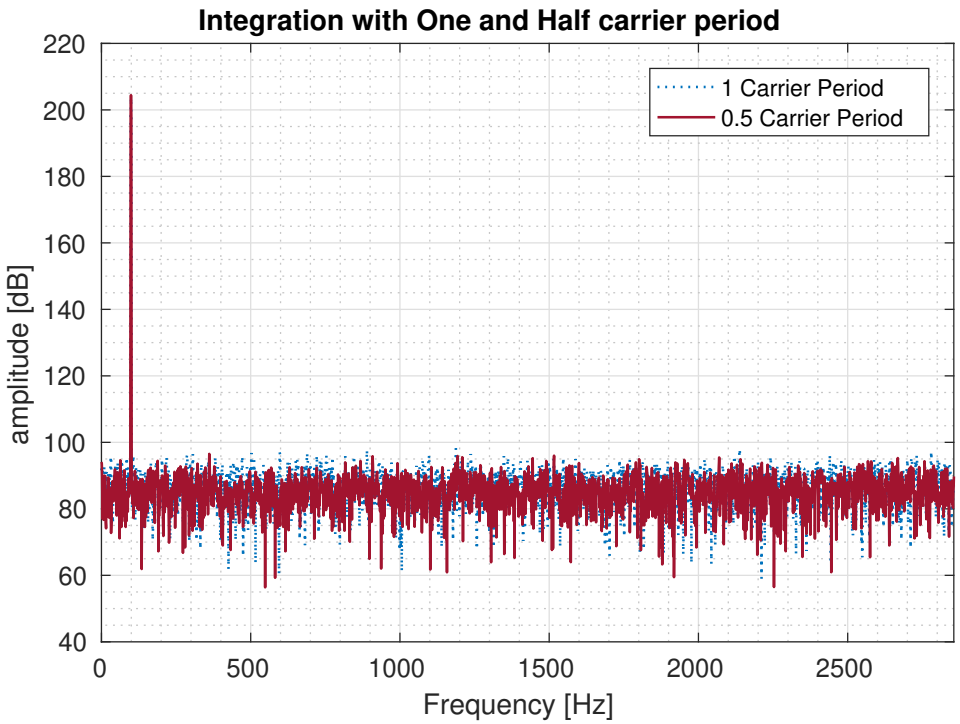

Figure 4.6: The figure represent the output signal spectrum for two set-up. The red line is for the integration on half period. It is possible to see that there is not harmonics component and the noise floor is lower than the blue line.

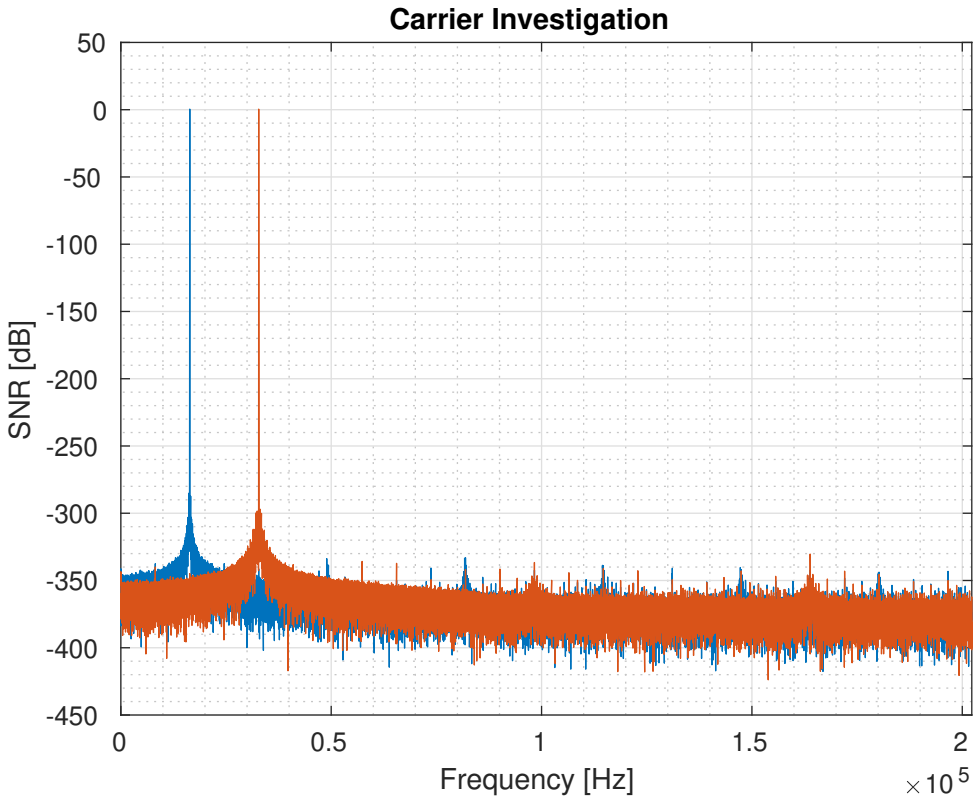

Figure 4.7: Carrier spectrum in order to understand if the noise comes from the carrier component. The red line represent the carrier for an integrator over 2 carrier periods. The blue line represent the carrier for a standard integration over 1 carrier period.

opposite sign sample and the is a small ” offset ” sinewave center on the zero that shift all the rectified signal by the its amplitude. Moreover, the carrier shifted by 3 samples has 2 wrong sample and there noise is greater than the case with 2 delayed samples. Now the unexpected SNR behaviour is explained.

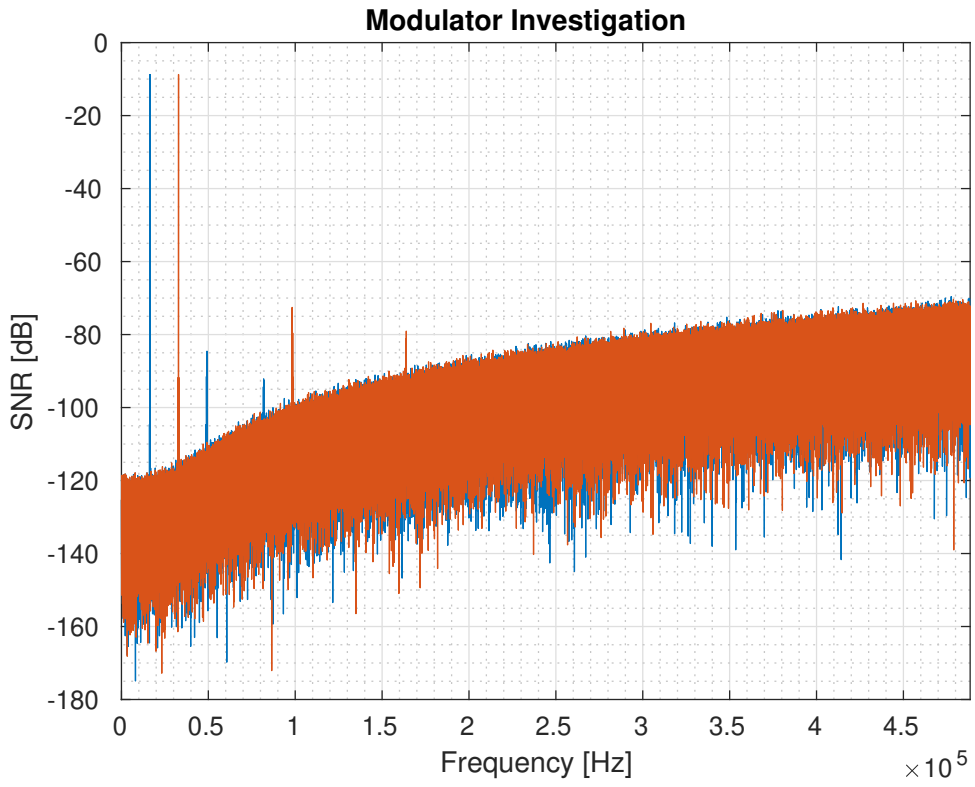

Figure 4.8: Modulator output spectrum, in order to understand if the noise power increment with a different carrier frequency. The figure shows that the noise power is more o less the same in both cases. The red line represent the carrier for an integrator over 2 carrier periods. The blue line represent the carrier for a standard integration over 1 carrier period.

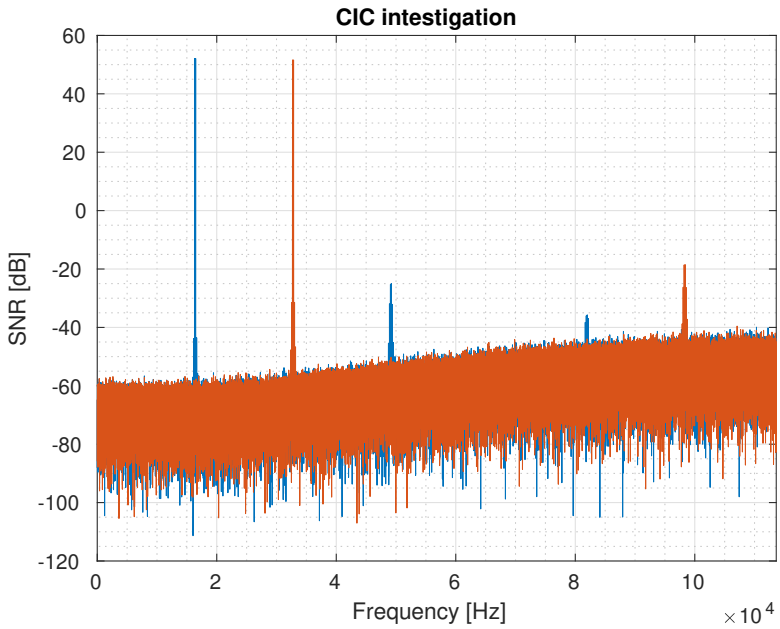

Figure 4.9: CIC output spectrum in order to understand if the noise power increment with a different carrier frequency. The figure shows that the noise power is more or less the same in both cases. The red line represent the carrier for an integrator over 2 carrier periods. The blue line represent the carrier for a standard integration over 1 carrier period.

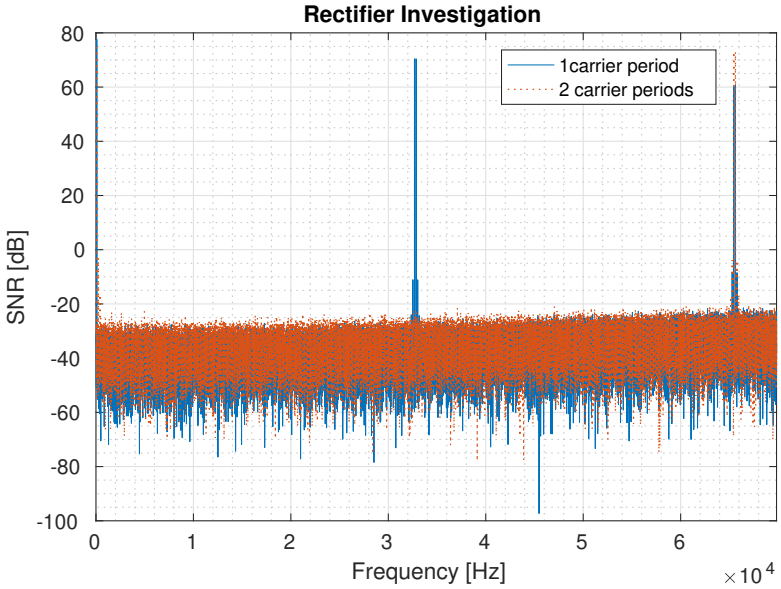

Figure 4.10: The red line represent the output spectrum with a carrier frequency double of the blue line. The red line is for an integration over 2 carrier periods. It is possible to see that the red noise floor cover all the blue line, an this is the noise source.

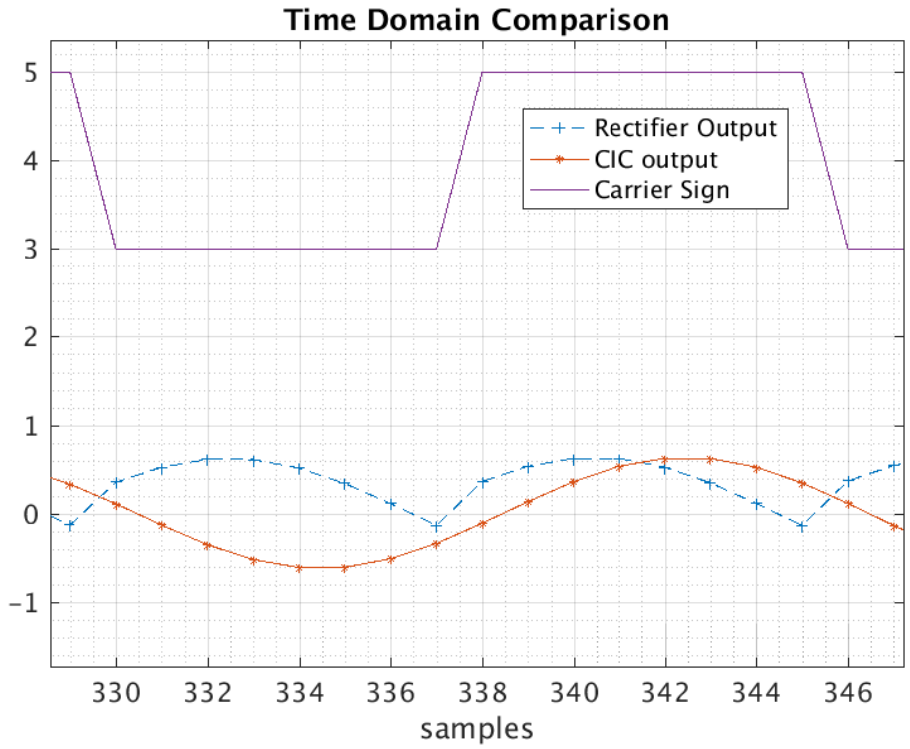

Figure 4.11: The red line represent the CIC output signal while the blue line represent the rectifier output signal. The amplitude of both lines is normalized to be 1. The purple line amplitude is not correct, it is from 3 to 5 only to plot a clear figure. It represent the sign of the carrier signal. The value 3 indicate -1 while the value 5 indicate +1

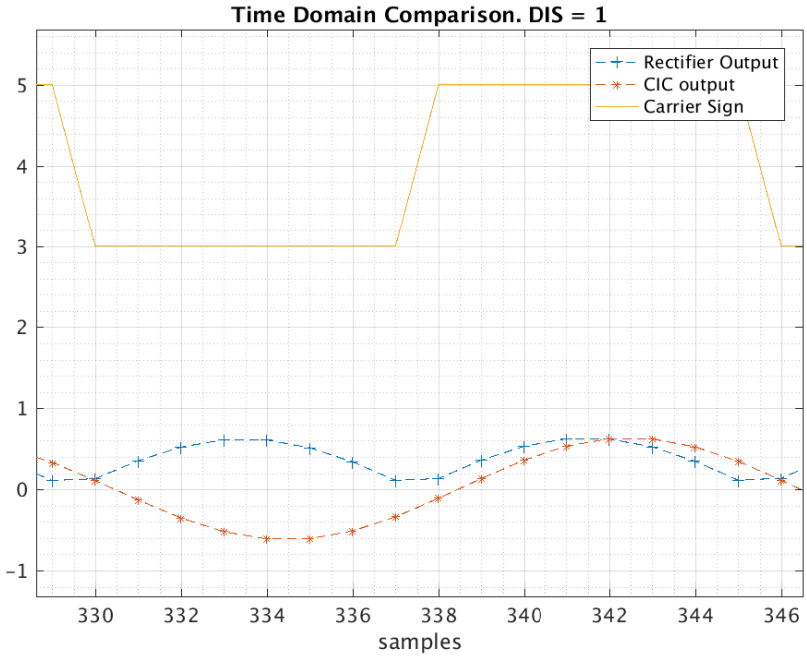

Figure 4.12: Time domain output with the carrier delayed by 1 sample. The error is different but it also introduce a small quantity of noise power if rectified.

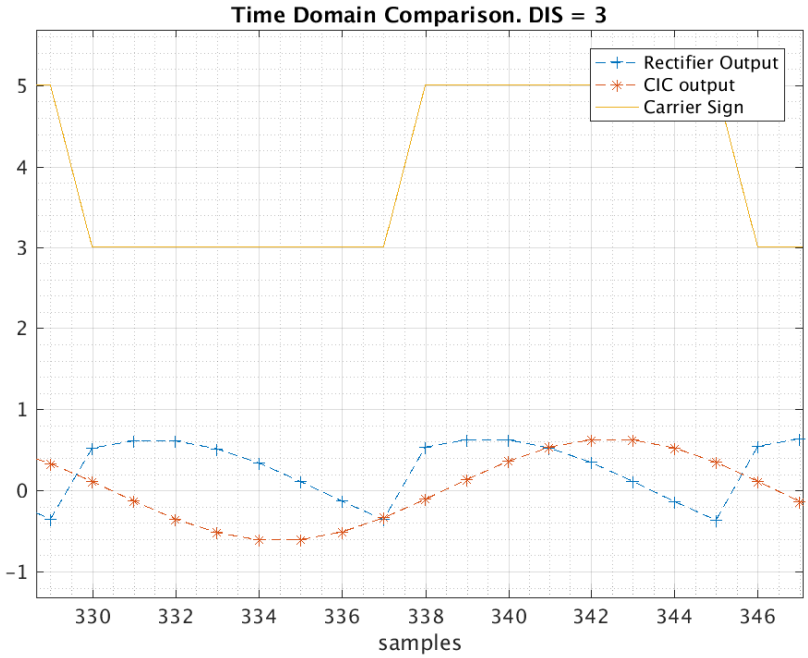

Figure 4.13: Time domain output. The error is worst than the case delayed by 2 sample. In this case, as shown in figure, the wrong samples are 2 instead of 1

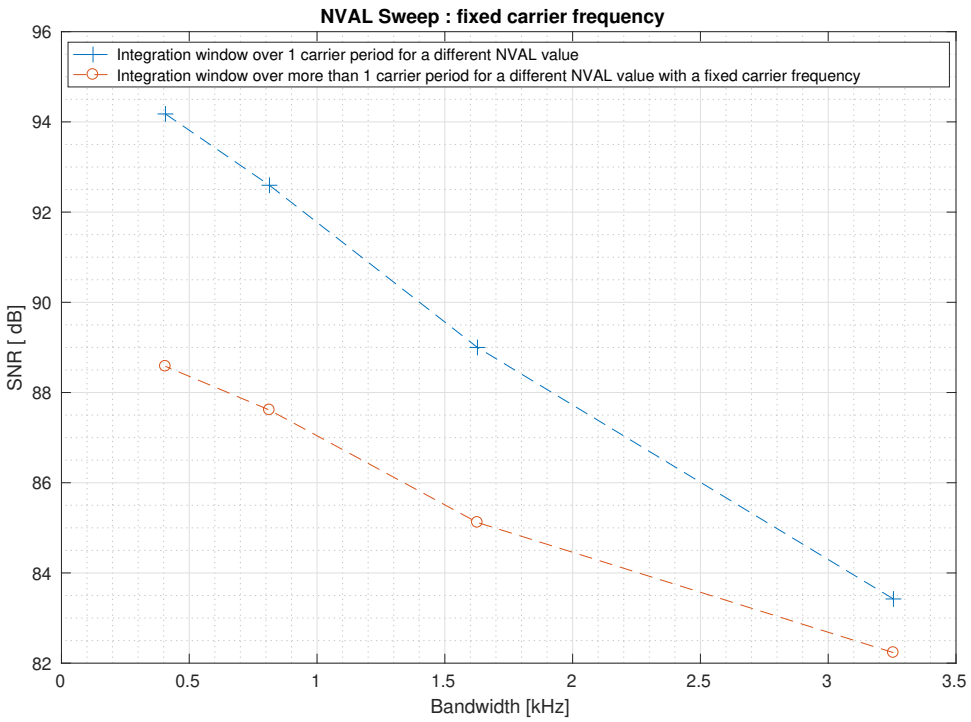

Figure 4.14: The figure represent two type of investigation on the integrator part. The red line represent the NVAL sweep fro 16 to 64 keeping the carrier frequency the same as the output sampling ratio. This means that the integrator works over one carrier period. The blue line is set to work with different carrier periods. To achieve this behaviour , the carrier frequency is fixed and the NVAL value can change.For each line the CIC decimation factor is fixed to 16 and the prefilter is enabled. The point corresponding the integration over 2 periods is at 3.2 kHz of bandwidth while the point corresponding an integration of 4 periods is at the bandwidth 1.8 kHz. For each point the CIC decimation factor is fixed to 16

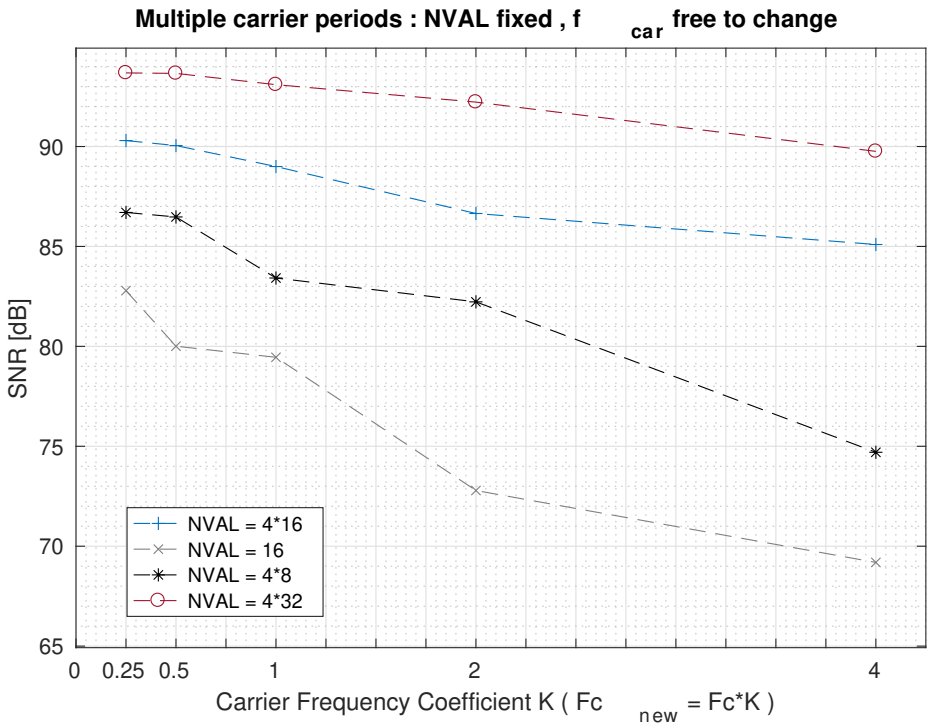

Figure 4.15: The 4 lines represent different chain set-up with a different carrier frequency. To integrate different carrier periods the carrier frequency doesn't change with the integration value. The chain set-up is : Pre filter enable, CIC decimation factor equal to 16 for each line. The comparison is the type 1 as des

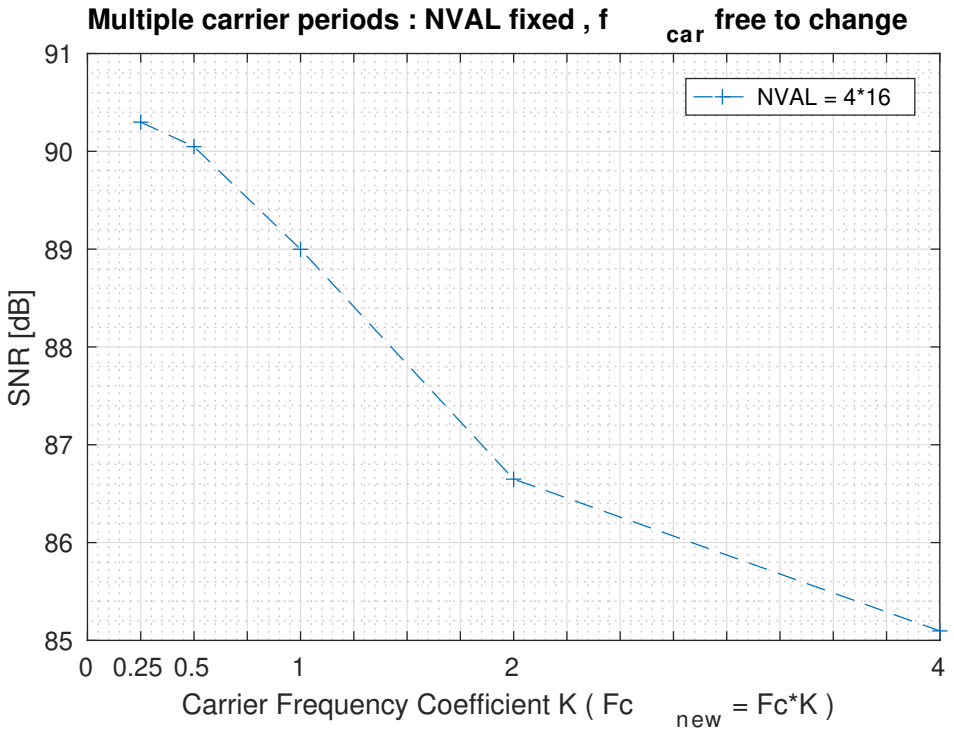

Figure 4.16: To integrate different carrier periods the carrier frequency doesn't change with the integration value. The chain set-up is : Pre filter enable, CIC decimation factor equal to 16 for each line. The comparison is the type 1 as described on the Appendix A. The parameter K indicate the number of carrier period integrated. The performance increase with an integration of less than one carrier period.

4.2.1 PRE - Rectifier - Integrator - CIC

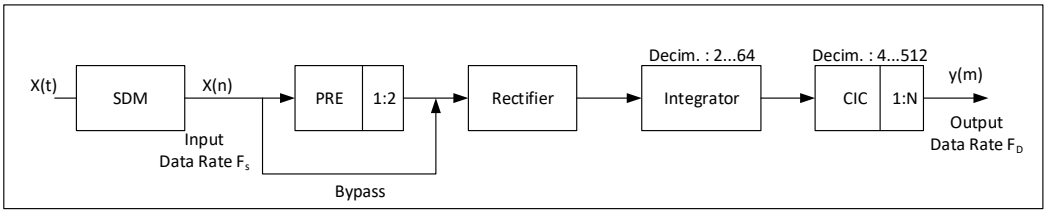

Figure 4.17: New Architecture : Sigma Delta - PRE filter - Rectifier - Integrator - CIC filter

The first architecture change is with the rectification and the integrator in the middle of the chain. The integrator in this position has a lower bit width than before and it is possible save some area on chip. To validate this solution is necessary investigate on the performance of the new filter chain. Before start with the investigation work , it is necessary fix a common comparison set-up as reference to compare the new performance with the old one. To compare the two architecture is possible to choose between type 1 or type 2 comparison as explained in the appendix A . With a type 1 comparison after the integrator is necessary introduce an interpolation block in order to increase the sampling frequency from $f_{D_{int}}$ to the original f_D after the CIC stage. The mathematical relation between the reference architecture and the first is :

$$f_{D_{out}} = \frac{f_{D_{int}}}{Dec}$$
$$L = \frac{f_{D_{ref}}}{f_{D_{out}}} = Dec \tag{4.2}$$

As point of reference is possible to choose the output sapling frequency of $f_{D_{out}} = f_{D_{ref}} = 4882.81$ Hz that means the same carrier frequency for the original architecture. The first architecture relationship between carrier frequency and sampling frequency is not anymore the same as before. In this case the carrier frequency is $f_{car} = Dec * f_D$.

The type of interpolation is a simple hold that extend the value of the signal for each sample introduced. The SNR performance are quite lower than the reduced filter chain. In order to improve the overall performance, as fist tentative,it is possible to increase the integrator and the interpolation value due to keep the same output sampling frequency. The results are shown in figure 4.18 . The blue line represent the simulations without the NVAL adjustment , it means that the NVAL range is the same and restricted to [8 16 32 64]. The red line represent the simulations with an extended integration length value. This particular case is studied with an of 16times for the integration window length. The performance are significant better due to the high decimation factor of NVAL and so on the higher integrator

performance. The criteria used to choose the new interpolation value is :

$$f_{D_1} = \frac{Fs \cdot L_1}{2 \cdot NVAL_1 \cdot Dec} \tag{4.3}$$

$$f_{D_2} = \frac{Fs \cdot L_2}{2 \cdot NVAL_2 \cdot Dec} \tag{4.4}$$

Settings the sampling frequency 1 equal to the sampling frequency 2 is possible to obtain :

$$\frac{Fs \cdot L_1}{2 \cdot NVAL_1 \cdot Dec} = \frac{Fs \cdot L_2}{2 \cdot NVAL_2 \cdot Dec}$$

$$\rightarrow L_2 = \frac{NVAL_2 \cdot Dec}{NVAL_1} = \frac{NVAL_1 \cdot k \cdot Dec}{NVAL_1} = k \cdot Dec \tag{4.5}$$

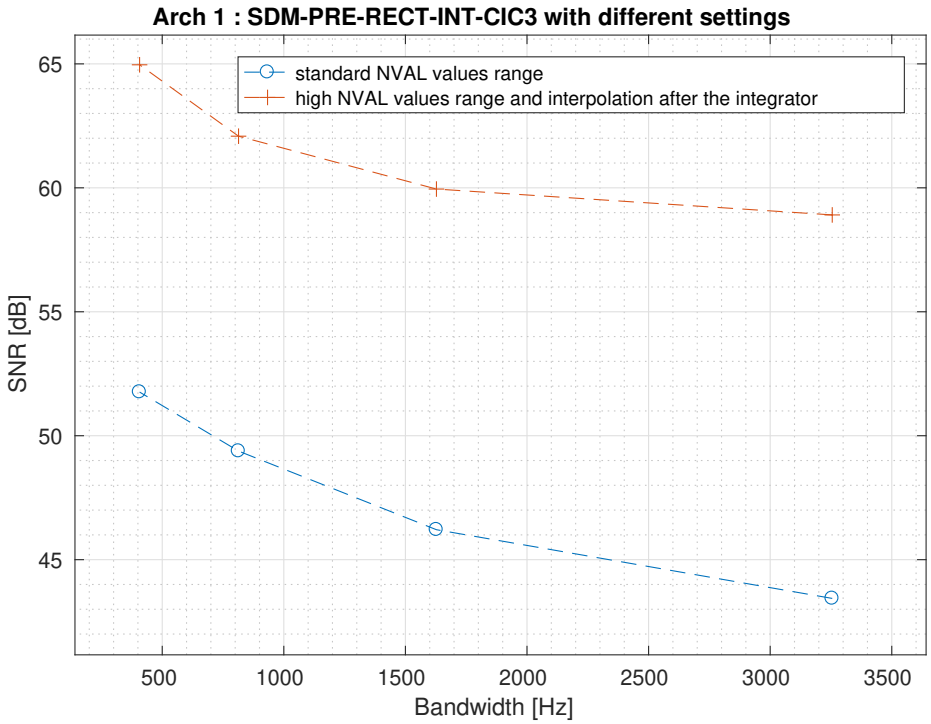

Figure 4.18: The figure represent the new configuration with two different set-up. The blue line is a set-up with a standard range for the integration value : [8 16 32 64] while the red line is with an extended range of integration values. In order to keep the same bandwidth , an interpolator stage is necessary.

4.2.2 PRE - Rectifier - CIC - Integrator

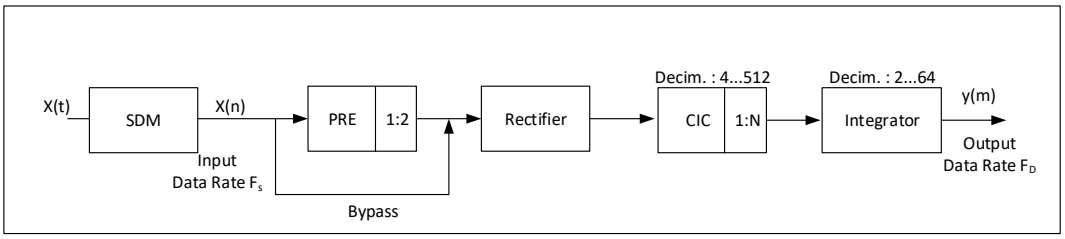

Figure 4.19: New Architecture : Sigma Delta - PRE filter - rectifier - CIC filter - integrator

The second possibility is to move the CIC filter between the rectifier and the integrator. The integrator works directly with the CIC output signal and the CIC works with a rectified signal. It is important to highlight that the demodulator stage is split in half, with a CIC filter stage in between. In order to keep the same bandwidth values , in according with the type 1 comparison, it is not necessary change the chain set-up because the integrator is in the same position as the reference case and only the rectifier changes. The only adjustment necessary is to multiply by 4 times the integration value to have the same bandwidth as the full filter chain. The figure 4.20 represent the output performance. It is possible to see that the SNR is greater than the previous case for each plotted point. The improvement is achieve with only a different position of the filter stages. At this point is necessary understand why the SNR is better than the previous case with only a different filter configuration. The reason is because the integration stage on the previous architecture is in the middle and for this reason an interpolation step is necessary. The interpolation block decrease the overall performance and for this reason the current architecture has better SNR that the previous one. The CIC has an high gain and for this reason this architecture has the same minor problem as the original one : it is necessary to take care the bit growth to avoid saturation problems. The integrator bit length must be

$$B_{out} = B_{in} + 3 \cdot log\,(Dec) \tag{4.6}$$

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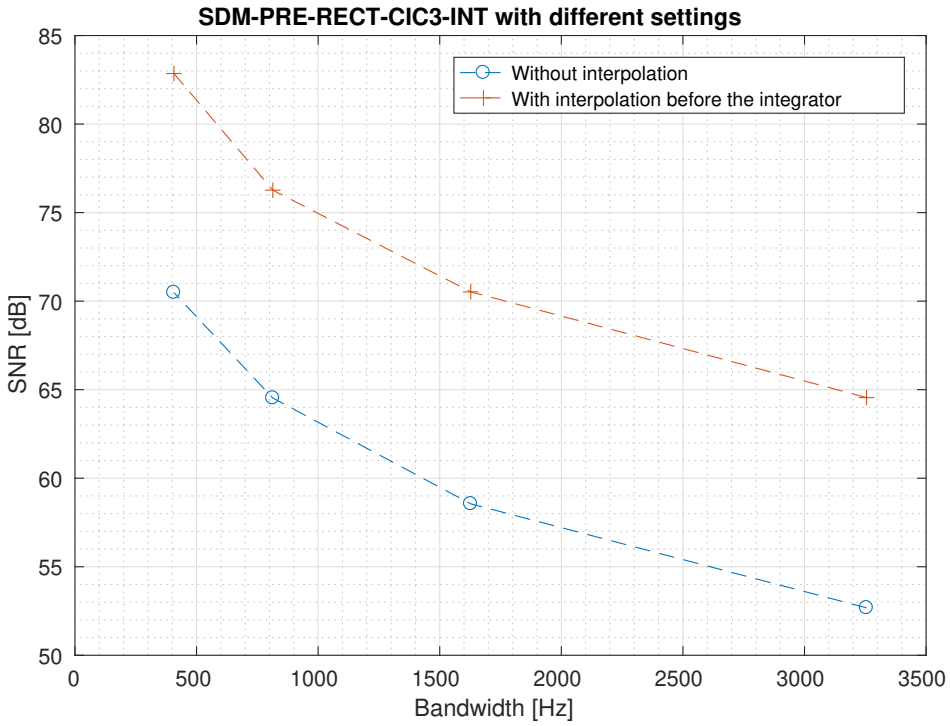

Figure 4.20: The red line represent the performance with the interpolator enabled. The SNR characteristic is higher than the blue line due to the higher integrator decimation value that change the filter magnitude. The interpolator needs to keep the same output sampling rate.

4.2.3 PRE - Rectifier - Integrator3

The last architecture proposed into this thesis is different than the previous solutions. Before to introduce the 3rd architecture is necessary to explain how the integrator-demodulator works. The integrator stage is made by a CIC structure and it is a simple first order filter with a decimation ratio equal to NVAL, that is the samples length on one carrier period. In order to extract the envelope of the modulated signal it require first of all a rectified signal (done by the rectification stage) and as second requirement it is that the integration windows with length of NVAL cover at least one carrier period or if more, a multiple of it. Moreover, it is necessary to use this information to understand the bound with the filter point of view. Defined $f_{D_{in}}$ as integrator input sampling frequency and $f_{D_{out}}$ as integrator output sampling frequency, it is possible to convert the previous information in the following concept. An integrator stage , in order to demodulate an rectified AM signal, it must has the output sampling frequency $f_{D_{out}}$ equal to the carrier frequency. Furthermore , it is possible to define a

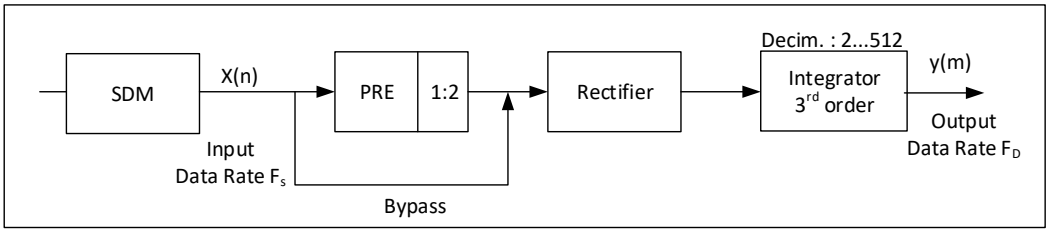

Figure 4.21: New Architecture : Sigma Delta - PRE filter - rectifier - 3rd order integrator

relationship between NVAL and f_{car} and it is :

$$NVAL = \frac{f_{D_{in}}}{f_{D_{out}}} = \frac{f_{D_{in}}}{f_{car}} \tag{4.7}$$

The current configuration has an high bit growth due to the high decimation factor of the 3^{rd} order integrator stage. It is necessary to consider this problem to avoid saturation problem at the output signal.

It is important to highlight that the overall order of the current architecture is 6 : a 3^{rd} order pre filter and a 3^{rd} integrator. The overall order of the original configuration , but also of the other solution, is 7. The chain are made by a 3^{rd} order pre filter, 3^{rd} order CIC filter and a 1^{st} order integrator. The performance with the current solution are achieved with a chain made by a lower order than the previous architecture. It is important to report because a lower order means less hardware area used, less power and faster calculation time. Indeed the chain length is lower than the other type. In order to compare the same settings with the same order for all the solution proposed, in figure 4.23 it is shown the performance with an 4^{th} order integrator. The overall performance are better than the 3^{rd} order case but not enough to fill the gap with the reference architecture. The SNR increment is only of $+0.5$ dB.

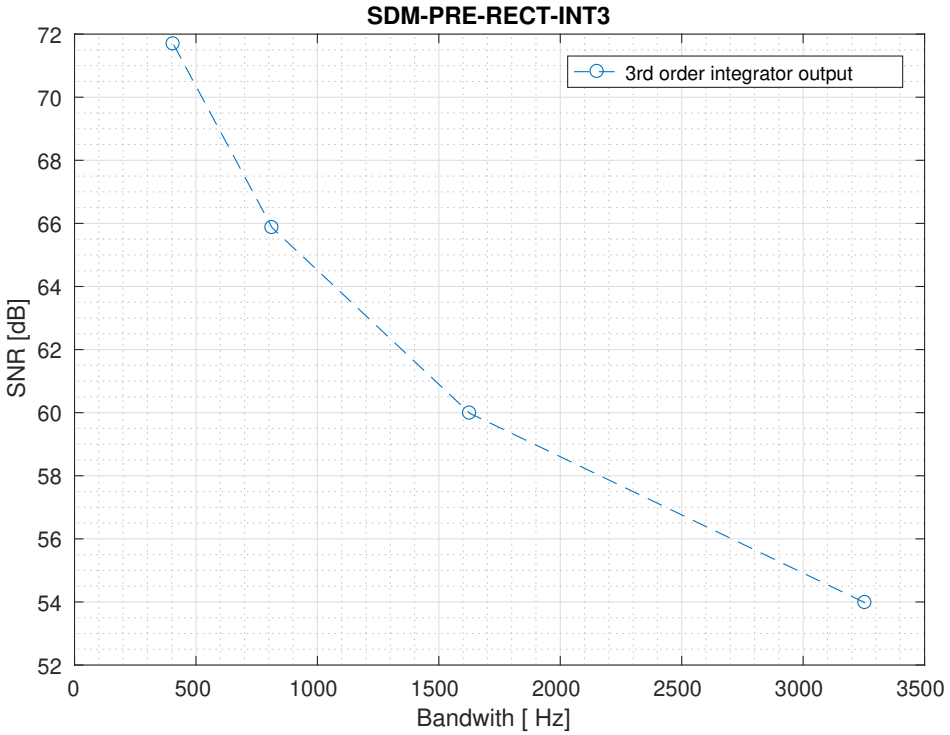

Figure 4.22: The figure represent the performance of a 3rd order integrator. The chain set-up was chosen in order to satisfy the condition for a type 1 comparison as explained on the Appendix A. The performance are quite near the reference case but a gap between the two architecture is still present.

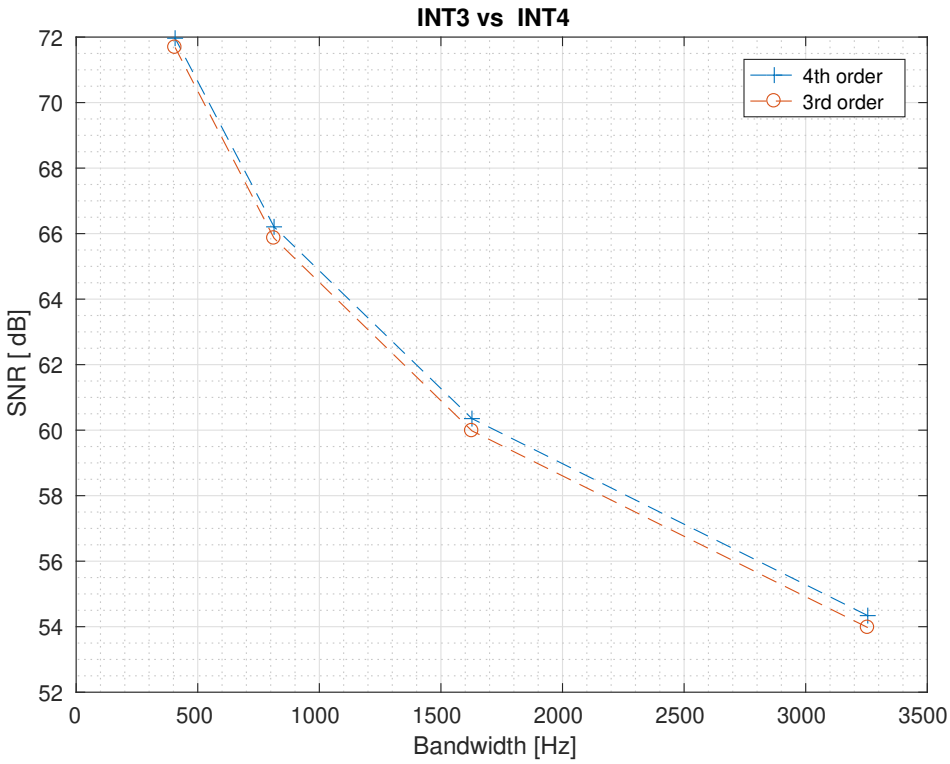

Figure 4.23: The figure represent the comparison between the performance of an 3rd order integrator and a 4th order integrator. The comparison is a type 1 as described on the appendix A. The performance are better for the 4th order integrator but the increase is not so much high.

5 Conclusion

As last chapter on this thesis the comparison between all the architecture is necessary to understand prons and cons.

5.1 Performance Comparison

For each architecture under evaluation was chosen the type 1 comparison to keep the same bandwidth range at the output. After a first evaluation without FIR filters it was chosen to keep the architecture short as possible. The minimum architecture is made by : rectifier , prefilter, CIC, integrator. The architecture one has the Integrator stage in the middle of the chain and to keep the sampling frequency equal to the carrier frequency after the CIC decimator, it is necessary use an interpolate stage after the integrator, to increase the sampling frequency before to decimate it. The performance are shown in the figure 5.1 . It is possible to see that the architecture one is the less performance solution, with a lower value of SNR for each considered point. The architecture 2 and 3 are near in terms of performance. The only difference between them is that the architecture 3 has a lower overall order of 5 instead of 6 (the prefilter is enabled for both cases). Moreover , the area on chip will be lower than the architecture 2 with better performance.

As seen in the chapter 4 , each architectures has an " enchanted " version with an interpolation stage in order to increase the decimation rate without change the comparison type. Increasing the decimation rate will increase the stop-band performance of the filter stages, and so on , the overall SNR. The figure 5.2 represent the set-ups just described. It is possible to see that the architecture 1 remains the solution with lower performance but not for all point as before. For $\simeq$ 4 kHz the SNR is greater than the 3rd architecture. After the crossing point at the value $\simeq$ 1.6 kHz the 3rd architecture performance is better than the first one. In this case the architecture 2 has the best performance.
No one of these architecture can get close to the original architecture SNR. The reason be-

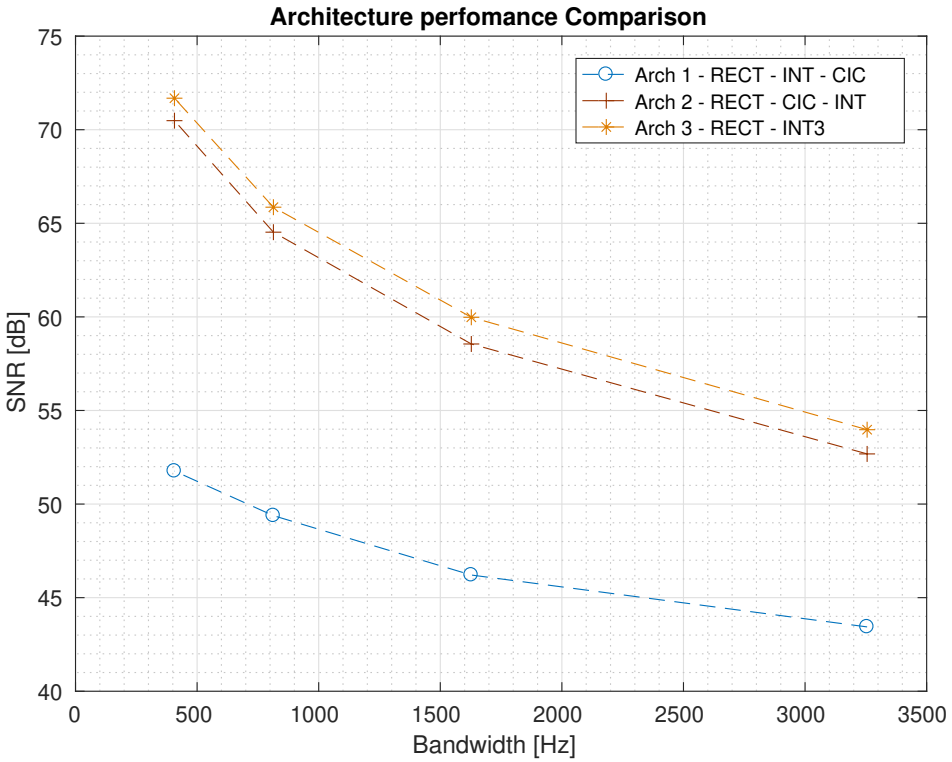

Figure 5.1: The figure represent a comparison between 3 different architectures.In order to compare the performance with the same bandwidth was chosen a type 1 comparison as describe on the appendix A. The set-up for each architecture are adjusted to get the same sampling frequency for each one.

hind this problem is because the rectify block introduce noise during the rectification process, and the best position to rectify the signal is at the end of the chain, before the integrator. Only the original architecture has this characteristic, but with the rectifier in the original position there is a different amount of group delay to compensate due to the previous filter stages.

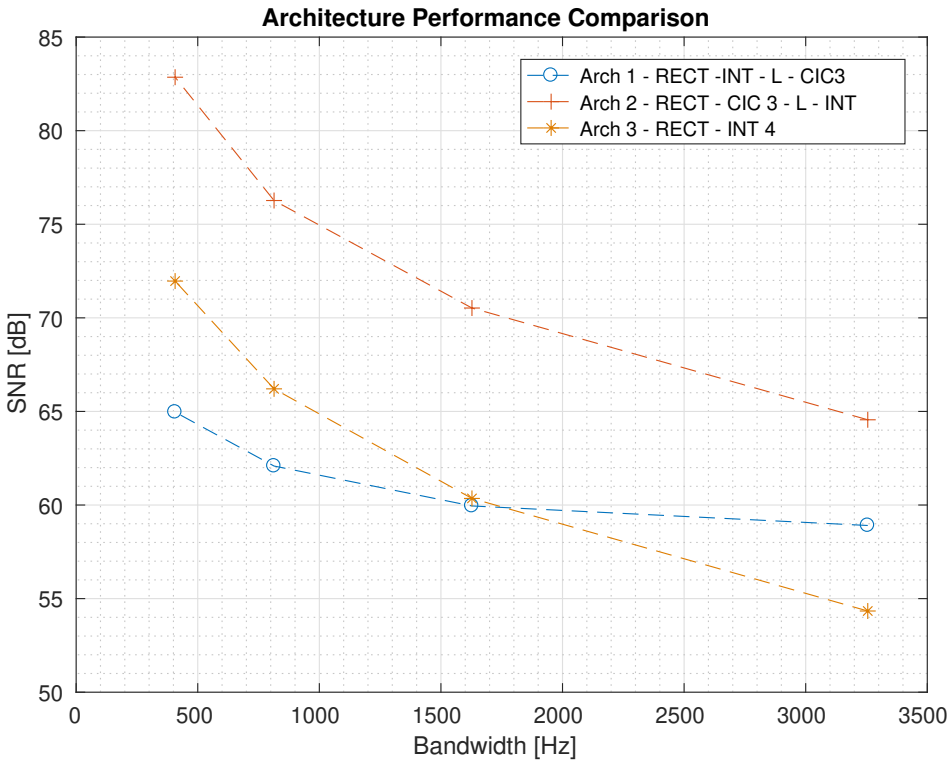

Figure 5.2: The figure represent a comparison between 3 different architectures. The architecture under investigation have an interpolation block inside the chain, in order to simulate the behaviours with high decimation rates. The interpolation block is necessary in order to keep the comparison type 1 valid.

Appendix A

Using different chain architecture, with different sampling rate is easy compare output performance in a wrong way. For this reason , on this appendix, are defined two comparison criteria for the filter chain . It is necessary define three main parameters of interest before explain the comparison type. For this application the parameters are :

- SNR as output parameter
- DEC as overall decimation factor
- BW as overall filter chain bandwidth

Type 1 : Bandwidth Comparison

As first comparison type is possible to choose the bandwidth as common point, with this method the output performance are calculated with the same sampling rate but the filter chain that has generated the output signal has a different settings. For example is possible suppose to have a general filter chain called FC_1 with bandwidth BW_1, decimation rate DEC_1 and SNR_1. The goal is compare FC_1 with another filter chain FC_2 , with the same parameters name but with the last number equal 2. To achieve the same bandwidth $BW_1 = BW_2$ in general, the architectures must have different decimation factors $DEC_1 \neq DEC_2$. With this criteria is possible to obtain the following equations :

$$\begin{cases} SNR_1 \neq SNR_2 \\ BW_1 = BW_2 \\ DEC_1 \neq DEC_2 \end{cases}$$

This comparison type is useful to compare different architecture when is not possible to guarantee the same bandwidth with the same settings. Keeping the same bandwidth is possible to compare the performance in the frequency domain, and so on , verify the performance for a chosen frequency regardless of the chosen settings.

Type 2 : Decimation Factor Comparison

As second comparison type is possible to choose the same decimation settings for two architecture. The filter chain notation are the same as before. The goal is compare the output

SNRi for both architecture. With this criteria is possible to obtain the following equations :

$$\begin{cases} SNR_1 \neq SNR_2 \\ BW_1 \neq BW_2 \\ DEC_1 = DEC_2 \end{cases}$$

With this type of comparison is possible to highlight the overall performance behaviour due a different chain topology. It is useful to understand the performance changes with a different filter combination.

Example of Comparison Type

In order to clarify the difference between the two type in this subsection is reported an example of two different filter chain for a sigma-delta application.

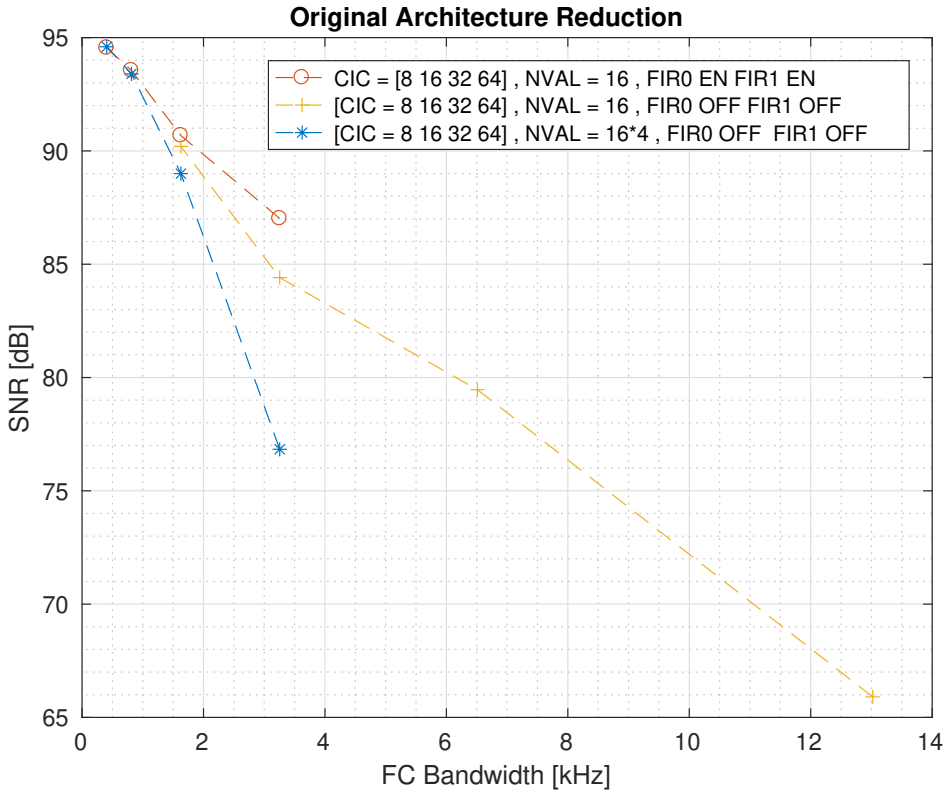

Figure 5.3: The plot shown the SNR performance for a two different architecture. The first architecture (red line) is the original one. The second architecture has two different line the blue one and the yellow one. The structure is the same, it changes only the comparison type. The yellow line represent the comparison type 2 : Same settings, different bandwidth. The blue line represent the comparison type 1 : Same bandwidth different settings.

Appendix B

Theory behind Comb filters

There are many application where the input signal frequency must be changed in order to process it at the output of the application. For example it could be necessary change the output sampling frequency from an high speed A/D converter in order to gain quality and to make the calculation more easy to implement with a lower sampling frequency. In order to change the sampling frequency are specified two operation type : Interpolation and Decimation. The interpolation is done by the increasing the input sampling frequency , in this way the output sampling frequency will be higher than the source. The interpolation is Linear an time invariant operation. The decimation operation is the opposite . The output frequency will be lower than the input sampling frequency. Keep it in mind these concept it is possible to introduce three identity useful to understand the reason why a FIR filter can be realized with a Comb architecture. The identity are :

- First Noble identity
- Second Noble identity
- Third Noble identity

First Noble Identity

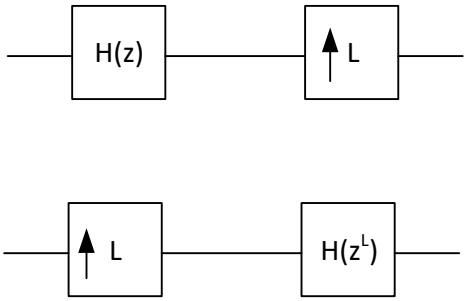

Figure 5.4: The cascade of H(z) and the interpolation stage is equal to the cascade of the interpolation stage before $H(z^L)$ [2]

Second Noble Identity

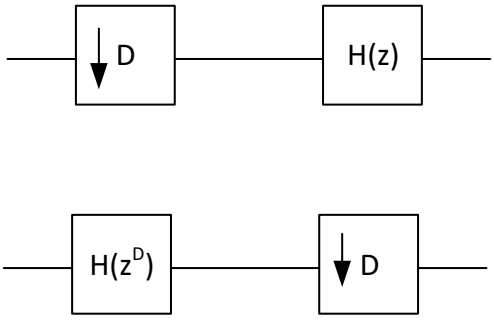

Figure 5.5: The cascade of decimation stage followed by the filter H(z) is equal to the cascade of the filter $H(z^D)$ followed by the decimation stage D[2]

Third Noble Identity

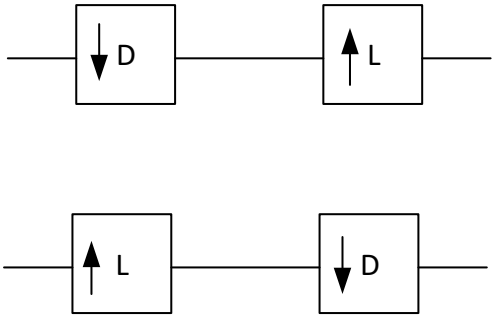

Figure 5.6: The third identity collect the propriety of both identity to merge them into only one. The cascade of Decimation stage followed by an interpolation stage is equal to the cascade of an interpolation stage followed by a decimation stage. This identity is true if and only if the value of D and L are first among them.[2]

CIC filters Theory

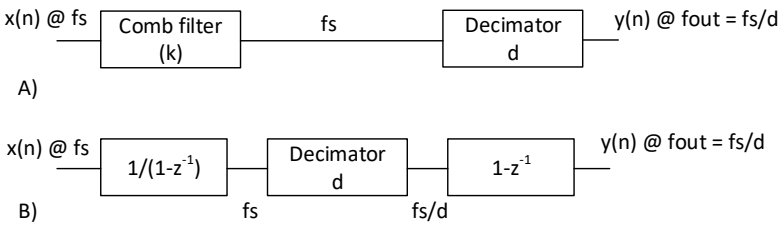

Figure 5.7: A. Comb filter followed by a decimation stage. It is use as down-converter and filter. B. Integrator stage followed by the decimation block and comb stage. The cascade is equivalent to A. for the second noble identity[2]

The filter formula on study is

$$H(z) = \frac{1 - z^{-k}}{1 - z^{-1}} = \frac{1}{1 - z^{-1}} \cdot (1 - z^{-k}) \tag{5.1}$$

The filter is followed by a decimation stage as shown in figure 5.7.A Using the second noble identity is possible to reduce the operating rate of the comb part $(1 - z^{-k})$ from "k" to "1" (express as number of delay). The result are shown in figure 5.7.B . The CIC architecture introduce a lot of advantages [2] :

- no multiplication needed
- no filter coefficient
- easy to design

Linear Phase

The necessary and sufficient condition to have a linear phase, for a real,linear ,casual and time invariant system, is that the impulse response must have a symmetry center. Moreover, it is possible to highlight that only the FIR filter can have linear phase, because the IIR filters has infinite impulse response and they can not be symmetric. All the filters in this application (at the exception of the high pass filter IIR) have linear phase.

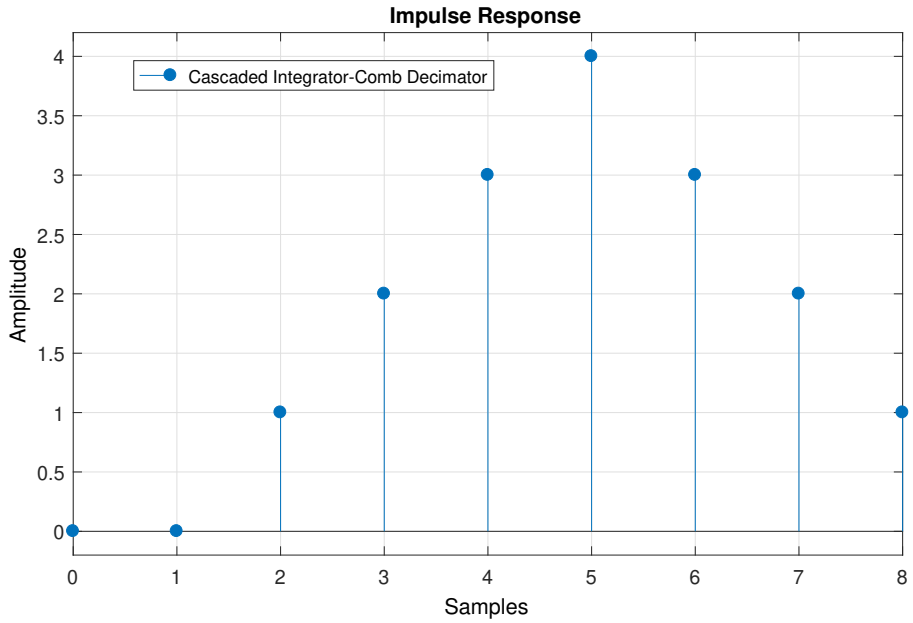

Figure 5.8: The impulse response has a center of symmetry at the sample 5. This is sufficient to conclude that the phase is linear.

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[2] M. Craig and E. Gillian, *A simple approach to Digital Signal Processing*, Oct 1993.

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