Robustness of Monochromatic LED Modules towards Electrostatic Discharge Events

July 3, 2013

Contents

1 CARRIERS RECOMBINATION **6**

1.1 RADIATIVE RECOMBINATION 7

1.1.1 VAN ROOSBROEK-SHOCKLEY MODEL 12

1.1.2 BIMOLECULAR RECOMBINATION COEFFICIENT ESTIMATION . 14

1.2 NON-RADIATIVE RECOMBINATION 14

1.2.1 SHOCKLEY-HALL-READ RECOMBINATION 16

1.2.1.1 Excess-Carrier Lifetime 19

1.2.2 AUGER RECOMBINATION 20

1.2.3 SURFACE RECOMBINATION 21

1.3 QUANTUM EFFICIENCY 23

2 LED DEVICES **25**

2.1 LED ELECTRICAL PROPERTIES 25

2.1.1 HOMOJUNCTION STRUCTURE AND ELECTRICAL MODEL 25

2.1.2 HETEROJUNCTION STRUCTURE 27

2.1.3 QUANTUM WELL 28

2.1.3.1 THE INFINITE SQUARE-SHAPED QUANTUM WELL . . . 28

2.1.3.2 THE ASYMMETRIC AND SYMMETRIC FINITE SQUARE-SHAPED QUANTUM WELL 31

2.1.4 OTHER NONIDEALITIES AND CHARACTERISTICS 35

2.2 LED OPTICAL PROPERTIES 39

2.2.1 EFFICIENCY 39

2.2.2 SPECTRAL CHARACTERISTICS 40

2.2.3 LIGHT EXTRACTION AND GENERAL EFFICIENCY IMPROVEMENT TECHNIQUES 44

2.2.4 L-I CHARACTERISTIC 48

3 ELECTROSTATIC DISCHARGE 50

3.1 ESD GENERATION MECHANISMS 50

3.1.1 LOCAL CHARGE GENERATION MECHANISMS 51

3.2 ESD STRESS MODELS 53

3.3 ESD STRESS METHODS 55

3.3.1 HUMAN BODY MODEL (HBM) 56

3.3.1.1 TEST PROCEDURE 59

3.3.2 MACHINE MODEL (MM) 60

3.3.3 CHARGED DEVICE MODEL (CDM) 61

3.3.3.1 TEST PROCEDURE 62

3.3.4 OTHER STRESS MODELS 65

3.4 DEVICES PROTECTION STRATEGIES 65

3.4.1 ESD CONTROL METHODS 65

3.4.2 ESD PROTECTION DEVICES 66

4 ESD ON LED DEVICES 72

4.1 PREVIOUS WORKS ON ESD EFFECTS ON LED DEVICES 72

4.2 CONCLUSIONS 86

5 MEASUREMENT SETUP AND EXPERIMENTAL DETAILS 87

5.1 TRANSMISSION LINE PULSE (TLP) TECHNIQUE 87

5.1.1 FUNDAMENTALS AND IMPLEMENTATIONS 87

5.1.2 CURRENT SOURCE TLP 89

5.1.3 TIME-DOMAIN REFLECTOMETER TLP (TDR-TLP) 90

5.1.4 TIME DOMAIN TRANSMISSION TLP (TDT-TLP) 91

5.1.5 TIME-DOMAIN TRANSMISSION REFLECTOMETER TLP (TDTR-TLP) 92

5.1.6 FINAL CONSIDERATIONS ON TLP STRESS-SYSTEMS STANDARDIZATION AND OPTIMIZATION 93

5.2 MEASUREMENT SETUP 94

5.2.1 STANFORD RESEARCH SYSTEMS PS350/5000V HIGH VOLTAGE GENERATOR 94

5.2.2 TEXTRONIK TDS680B OSCILLOSCOPE 95

5.2.3 KEITHLEY 2612 SOURCE METER 95

5.2.3.1 HP 3488A SWITCH/CONTROL UNIT 97

5.2.4 ANDOR LUCA 97

5.2.5 OPTIKAM PRO3 99

5.3 ANALYZED DEVICES 99

6 SINGLE LEDs ANALYSIS 105

6.1 BLUE SAMPLES 105

6.2 GREEN SAMPLES 109

6.3 RED SAMPLES 112

6.4 FINAL CONSIDERATIONS 114

7 SINGLE LEDS OPTICAL AND ELECTRICAL ANALYSIS 116

7.1 BLUE LEDs TESTING 116

7.1.1 POSITIVE BIAS ESD PULSES 116

7.1.2 NEGATIVE BIAS ESD-STRESS TESTS 119

7.2 GREEN LEDs TESTING 126

7.2.1 POSITIVE BIAS ESD PULSES 127
7.2.2 NEGATIVE BIAS ESD-STRESS TESTS 128
7.3 RED LEDs TESTING 138
7.3.1 POSITIVE BIAS ESD PULSES 138
7.3.2 NEGATIVE BIAS ESD-STRESS TESTS 139

8 LED MODULES ANALYSIS 147

8.1 GREEN LED MODULES ANALYSIS 147
8.2 RED LED MODULES ANALYSIS 158
8.3 BLUE LED MODULES ANALYSIS 164
8.4 FINAL CONSIDERATIONS 171

Preface

ABSTRACT

This work was aimed at investigating the robustness of LEDs and LED modules towards ESD events, exploiting a Transmission-Line-Pulser(TLP) system to apply negative bias ESD pulses to the devices. Three different types of LEDs (green, blue and red) were considered. In the first part of the work the devices were tested singularly, both with and without the use of an EMCCD camera to detect light emission during the ESD pulses. After that, monochromatic modules were tested. An analysis of the type of failure of the single LEDs was also carried on. The results showed that the different types of devices have a different behaviour both individually and connected in series. The waveforms analysis during the TLP test allow to identify the electrical degradation of the devices, while the camera images showed the chip areas where the discharge current is concentrated.

INTRODUCTION

Electrostatic discharges are a very important problem for electronic devices, in fact they can generate unexpected failures everywhere from the production chain to the field. Understanding the robustness of electronic devices towards these events is therefore fundamental. In particular, since LED devices are on the verge of gaining a main role in lighting applications market, it can be interesting to analyze LED module robustness. It is also something that has not been done yet.

In this thesis work the devices, both singularly and in modules, were tested by using a Transmission Line Pulser. In this system the distributed capacitance of a transmission line is charged using a high voltage generator. After that, the line is closed on a load through a switch and consequently discharges, generating a rectangular pulse with a well defined duration, determined by the line length. Since LEDs are more sensitive to reverse-bias stress, just negative pulses were applied.

An optical investigation was also carried on in order try to determine whether the ESD pulses gave emission or not, and where this emission was eventually located on the chip.

In the first part of this thesis a brief overview of the optoelectronics and ESDs theoretical principles will be given. The main ESD-stress test systems and models will be also reported. In the second part, the results of the experimental work will be shown and commented.

Chapter 1

CARRIERS RECOMBINATION

In a semiconductor at thermal equilibrium the concentrations of free carriers obey the law of mass action

$$n_0 p_0 = n_i^2 \tag{1.1}$$

When excess carriers are generated, for example through current injection or light absorption, concentrations are given by

$$n = n_0 + \Delta n \quad p = p_0 + \Delta p \tag{1.2}$$

Excess carriers can recombine in both radiative and non-radiative way.

Radiative recombination occurs when an excited electron falls to a lower energy level, recombining with a hole and giving emission of a phonon of energy equal to the one lost by the electron. These direct transitions between the valence band and the conduction band occur in all semiconductors and are the most important generation-recombination mechanisms in many of the compound semiconductors, such as gallium arsenide (GaAs) and indium phosphide (InP), composed of elements from columns III and V of the periodic table. However, in silicon and germanium the details of the crystal structure make direct transitions unlikely except when very high densities of holes and electrons are present. In silicon and germanium in fact, electrons at the lowest energy in the conduction band have nonzero momentum (we say that these materials have indirect energy gap). Because the holes at the valence-band maximum do have zero momentum, a direct transition that conserves it together with energy is impossible without a lattice (phonon) interaction occurring simultaneously. Thus, in silicon or germanium, direct transitions across the forbidden-energy gap require simultaneous interaction of three particles: the electron, the hole and a phonon that represents the lattice interaction. Three particles interactions are far less likely than two-particle interactions, such as those between a free carrier and a phonon, that can take place if there are localized allowed energy states into which electrons or holes can make transitions. In practice, localized states at energies between E_C and E_V are always present because of lattice imperfections caused by misplaced atoms or, more usually, because of impurity atoms, thus non-radiative recombination occurs even in direct band gap materials.

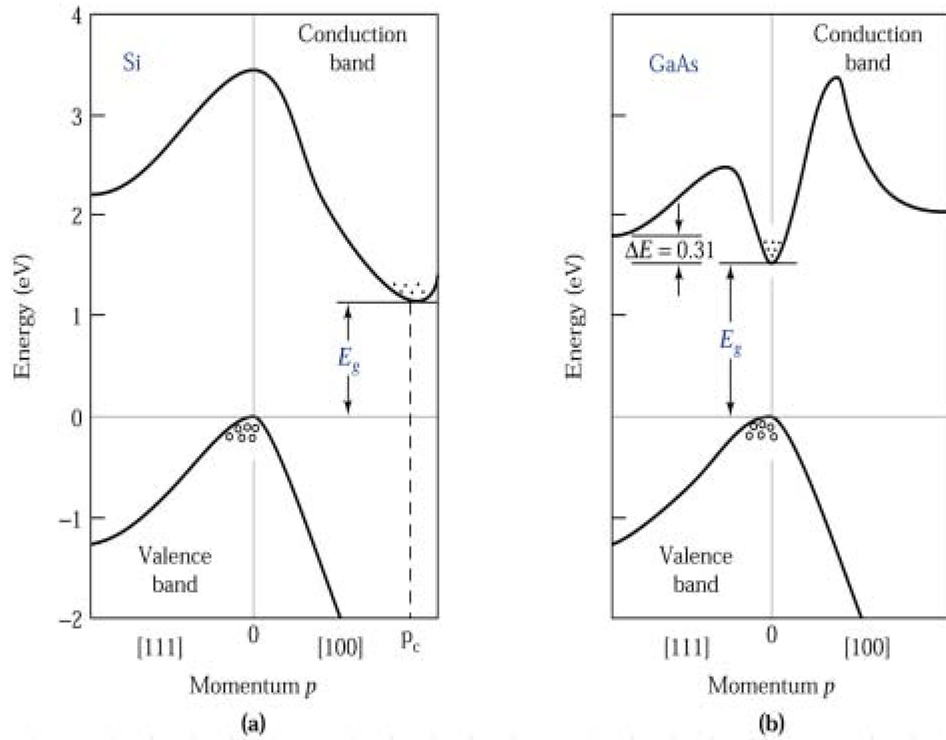


Figure 1.1: *Examples of direct (a) and indirect (b) energy gap*

These localized states act as stepping stones. In a recombining event, for example an electron falls from the conduction band to a state that we logically call a recombination center, and then it falls further into a vacant state in the valence band, thus recombining with a hole.

In a semiconductor, recombination can occur in both radiative and non radiative way, but in optoelectronic devices non-radiative recombination is an undesired effect that reduces the efficiency, so it should be eliminated. However non-radiative recombination strongly depends on the material quality, and because of the fact that it's impossible to totally eliminate defects and dislocations, it is also not feasible to make this kind of recombination disappear.

1.1 RADIATIVE RECOMBINATION

An important thing to notice is that in the recombination process, there must be not only conservation of energy (obtained through the emission of a phonon), but also of the momentum p. This makes radiative recombination much more disadvantaged in semiconductors with an indirect band gap. In fact, while in semiconductors with a direct energy gap the minimum of the conduction and the maximum of the valence band (where the most of the free electrons and holes are distributed) are located at the same value of p, in the other type of semiconductors maximum and minimum of the two bands correspond to different p values. This makes radiative recombination less likely to happen, because it becomes a three bodies process, in fact, in order to recombine with a hole, the electron has to change its momentum through interaction with a phonon (interaction with the crystal lattice).

To analyze radiative recombination in semiconductors, the first step is defining the recombination ratio R. Considering a free electron in the conduction band, the probability that it recombines

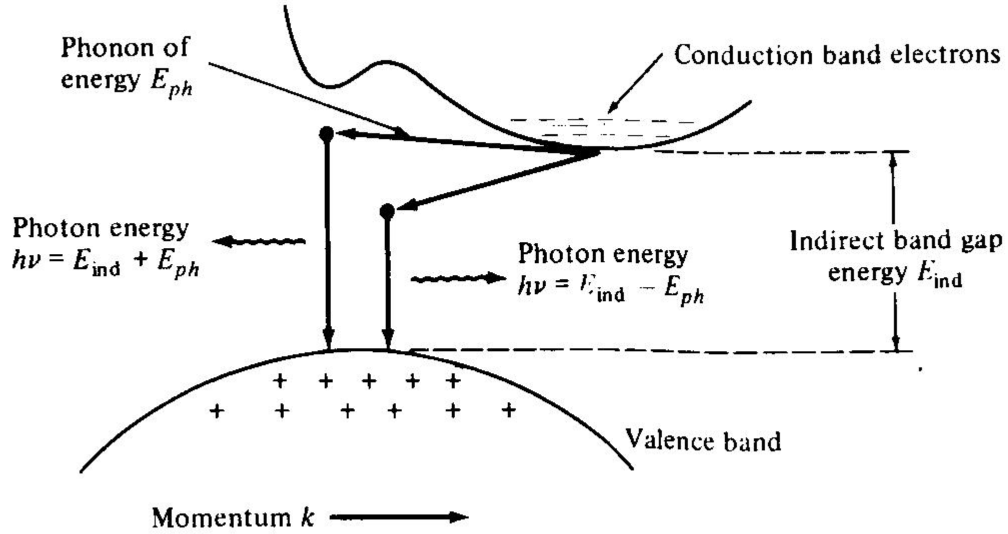


Figure 1.2: *Example of recombination processes in an indirect energy gap semiconductor.*

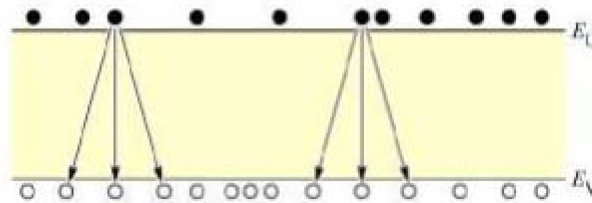


Figure 1.3: *Electrons and holes*

with a hole is proportional to the holes concentration in the valence band.

$$R \propto p$$

The number of the total recombination events is proportional to the electrons concentration too

$$R \propto np$$

We can thus define R (the recombination rate per unit volume and time) as

$$R = -\frac{dn}{dt} = -\frac{dp}{dt} = Bnp \tag{1.3}$$

Typical values of B for III-IV compounds are in the order of magnitude of $10^{-10} \div 10^{-9} cm^{-3}s^{-1}$.

We now consider the recombination dynamics as a function of time for the low-excitation case of a semiconductor exposed to light. Electrons and holes are generated in couples, thus their excess concentrations are equal

$$\Delta n(t)) = \Delta p(t) \tag{1.4}$$

The recombination rate can then be written as

$$R = B[n_0 + \Delta n(t))][p_0 + \Delta p(t))] \tag{1.5}$$

For low excitation levels the concentration of the photo-generated carriers is much lower than the majority-carriers concentration, $\Delta n \ll n_0 + p_0$, allowing us to neglect the $\Delta n \Delta p$ term in the recombination rate equation

$$R = B[n_0 p_0 + n_0 \Delta p(t) + p_0 \Delta n(t) + \Delta n(t) \Delta p(t)] \tag{1.6}$$

$$\approx B n_i^2 + B(n_0 + p_0) \Delta n(t) = R_0 + R_{excess} \tag{1.7}$$

where R_0 is the recombination rate at the equilibrium and R_{excess} the recombination rate for excess carriers.

Considering both generation and recombination

$$\frac{dn(t)}{dt} = G - R = (G_0 + G_{excess}) - (R_0 + R_{excess}) \tag{1.8}$$

where G_0 and R_0 are the generation/recombination rate at the equilibrium. Making the hypothesis that the light is turned off at $t = 0$, because of the fact that $G_0 = R_0$ for $t > 0$

$$\frac{d\Delta n(t)}{dt} = -B(n_0 + p_0) \Delta n(t) \tag{1.9}$$

The solution of this differential equation is

$$\Delta n(t) = \Delta n_0 e^{-B(n_0+p_0)t} \tag{1.10}$$

with $\Delta n_0 = \Delta n(t = 0)$. This equation can be written also as

$$\Delta n(t) = \Delta n_0 e^{-t/\tau} \tag{1.11}$$

We can thus define the carriers recombination time

$$\tau = [B(n_0 + p_0)] \tag{1.12}$$

for extrinsic semiconductors:

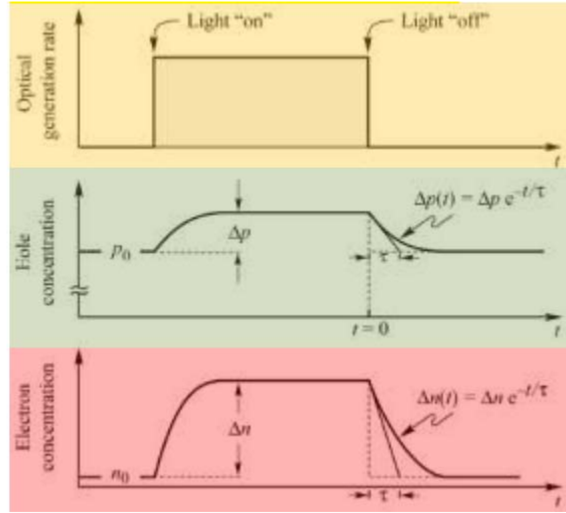


Figure 1.4: *Excitation level (yellow), holes (green) and electrons (red) concentration in a p-type semiconductor*

$$\tau_n = \frac{1}{Bp_0} = \frac{1}{BN_A} \tag{1.13}$$

in the case of p-type materials, and

$$\tau_p = \frac{1}{Bn_0} = \frac{1}{BN_D} \tag{1.14}$$

for n-type semiconductors.

Inserting these equations in the general case recombination rate formula, we obtain the *monomolecular rate equations*, valid for p-type material

$$\frac{d}{dt}\Delta n\,(t) = -\frac{\Delta n\,(t)}{\tau_n} \tag{1.15}$$

and n-type semiconductor.

$$\frac{d}{dt}\Delta p\,(t) = -\frac{\Delta p\,(t)}{\tau_p} \tag{1.16}$$

If we consider a high excitation level case, the equations obtained are different. In this situation in fact, the concentration of the photo-generated carriers is much higher than the concentration at the equilibrium, $\Delta n \gg n_0 + p_0$, and we can thus write

$$R = -\frac{dn}{dt} = -\frac{dp}{dt} = Bnp \tag{1.17}$$

$$R = B\left[n_0 + \Delta n\left(t\right)\right]\left[p_0 + \Delta p\left(t\right)\right] \quad (1.18)$$

$$R = B\left[n_0 p_0 + n_0 \Delta p\left(t\right) + p_0 \Delta n\left(t\right) + \Delta n\left(t\right)\Delta p\left(t\right)\right] \quad (1.19)$$

$$\approx B\Delta n\left(t\right)\Delta p\left(t\right) = B\Delta n\left(t\right)\Delta n\left(t\right) \quad (1.20)$$

Thus, for high injection levels, the bimolecular recombination equation becomes

$$\frac{d}{dt}\Delta n\left(t\right) = G - R = -B\Delta n^2 \quad (1.21)$$

In this case we have a non-exponential solution

$$\Delta n\left(t\right) = \frac{1}{Bt + \Delta n_0^{-1}} \quad (1.22)$$

with $\Delta n_0 = \Delta n\left(0\right)$.

In exponential processes the time-constant is calculated through the following equation

$$\tau\left(t\right) = -\frac{\Delta n\left(t\right)}{\frac{d\Delta n(t)}{dt}} \quad (1.23)$$

Applying this formula to the high injection level case, we obtain

$$\tau\left(t\right) = t + \frac{1}{B\Delta n_0} \quad (1.24)$$

In this case the time constant depends on time itself, in fact the lifetime of minority carriers increases through time, reaching in the end the low excitation value, when the decrease of carriers brings the system in a low-excitation situation.

The decrease in the carriers concentration can be measured evaluating the luminescence decay after a short excitation pulse, in fact the luminescence intensity is proportional to the recombination rate R.

Radiative recombination dynamics are very important in optoelectronic devices, for example they have a strong influence on LEDs turn-on and turn-off time. In fact recombination time is for example the parameter that limits the modulation speed of LEDs in telecommunications applications. There are two different ways to make minority carriers recombination time decrease:

- high doping in the active region

-injecting high concentrations of carriers into the active region

In practice heterojunctions are often use to confine carriers in very small regions, thus obtaining high carriers concentrations and low lifetimes.

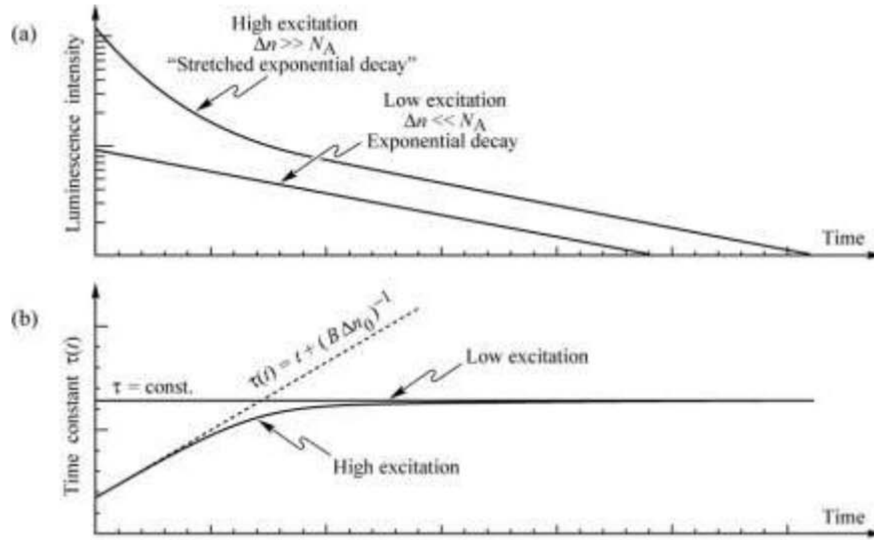


Figure 1.5: *(a) Luminescence decay for low and high excitation densities. (b) Time constants for low and high excitation densities.*

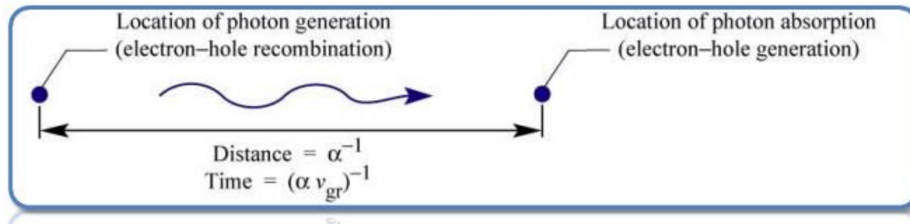


Figure 1.6: *Phonon absorption parameters*

1.1.1 VAN ROOSBROEK-SHOCKLEY MODEL

This model allows to calculate the spontaneous recombination rate both at equilibrium or not, needing the knowledge of a very limited set of parameters: the energy gap, the absorption coefficient α and the refractive index η. We can calculate the time needed for the absorption of a phonon as

$$\tau(\nu) = \frac{1}{\alpha(\nu)\, v_{gr}} \tag{1.25}$$

V_{gr} is the phonon velocity and $\frac{1}{\alpha(\nu)}$ (cm) the average distance traveled by a phonon at frequency ν before being absorbed.

Using the following equations

$$v_{gr} = \frac{d\omega}{dk} = \frac{d\nu}{d(1/\lambda)} = c\frac{d\nu}{d(n\nu)} \tag{1.26}$$

,

$$k = \frac{2\pi}{\lambda}\,,\ \omega = 2\pi\nu\,,\ \lambda = \frac{\lambda_0}{n}\,,\ \frac{c}{n} = \lambda\nu\,,\ \frac{1}{\lambda} = \frac{n\nu}{c} \tag{1.27}$$

where k is the wave vector ($2\pi n$, n the number of oscillations of the wave in the space unit $\frac{1}{\lambda}$), we can write the phonon absorption probability per unit time as

$$\frac{1}{\tau(\nu)} = \alpha(\nu)\, v_{gr} = \alpha(\nu)\, c \frac{d\nu}{d(n\nu)} \tag{1.28}$$

Multiplying the phonon absorption probability by the phonon density we get the phonon absorption rate per unit time. At the equilibrium the phonon density per unit volume, is given by Planck's black body radiation formula

$$N(\nu)\, d\nu = \frac{8\pi}{\lambda^4} \frac{1}{e^{h\nu/kT} - 1} d\lambda \tag{1.29}$$

Exploiting the relation $\lambda = \frac{c}{n\nu}$, we can write

$$d\lambda = -\frac{c}{(n\nu)^2} \frac{d(n\nu)}{d\nu} d\nu \tag{1.30}$$

and substituting this equation in the previous formula, we find the phonon distribution as a function of frequency

$$N(\nu)\, d\nu = \frac{8\pi\nu^2 n^2}{c^3} \frac{d(n\nu)}{d\nu} \frac{1}{e^{h\nu/kT} - 1} d\nu \tag{1.31}$$

The absorption rate per unit volume in the frequency interval (ν ;$\nu + d\nu$) is given by the ratio between he phonon density and the average phonon lifetime

$$R_0(\nu) = \frac{N(\nu)}{\tau(\nu)} = \frac{8\pi\nu^2 n^2}{c^3} \frac{d(n\nu)}{d\nu} \frac{1}{e^{h\nu/kT} - 1} d\nu \alpha(\nu)\, c \frac{d\nu}{d(n\nu)} \tag{1.32}$$

Integrating with respect to ν,we obtain the absorption rate per unit volume, given by the so called *Van Roosbroeck-Shockley equation*

$$R_0 = \int_0^\infty \frac{8\pi\nu^2 n^2}{c^2} \frac{\alpha(\nu)}{e^{h\nu/kT} - 1} d\nu \tag{1.33}$$

This equation can be simplified writing the absorption coefficient as

$$\alpha = \alpha_0 \sqrt{(E - E_g)/E_g} \tag{1.34}$$

the absorption coefficient is proportional to the densities of states, that has a quadratic dependence on energy ($\alpha_0$is the absorption coefficient at the energy $h\nu = 2E_g$). We can also neglect the dependence of the refractive index on the frequency, obtaining the simplified form of the Van Roosbroeck-Shockley equation

$$R_0 = 8\pi c n^2 \alpha \sqrt{\frac{kT}{E_g}} \left(\frac{kT}{ch}\right)^3 \int_{x_g}^\infty \frac{x^2\sqrt{x - x_g}}{e^x - 1} dx \tag{1.35}$$

where we have defined the following variables

$$x = \frac{h\nu}{kT} = \frac{E}{kT},\ x_g = \frac{E_g}{kT} \tag{1.36}$$

The exponential function increases rapidly with x, this means that just a small interval of energies near the energy gap contributes to the integral.

Material	E_g (eV)	α_0 (cm^{-1})	n	R_0 (cm^{-3}s^{-1})	n_i (cm^{-3})	B (cm^{-3}s^{-1})	τ_{spont} (s)
GaAs	1.42	$2\cdot10^{4}$	3.3	$7.9\cdot10^{-2}$	$2\cdot10^{6}$	$2\cdot10^{-10}$	$5\cdot10^{-9}$
GaN	3.4	$2\cdot10^{5}$	2.5	$8.9\cdot10^{-30}$	$2\cdot10^{-10}$	$2.2\cdot10^{-10}$	$4.5\cdot10^{-9}$
Si	1.12	$1\cdot10^{3}$	3.4	$3.3\cdot10^{6}$	$1\cdot10^{10}$	$3.2\cdot10^{-14}$	$3\cdot10^{-5}$

Figure 1.7: *Bimolecular recombination coefficients for some materials*

1.1.2 BIMOLECULAR RECOMBINATION COEFFICIENT ESTIMATION

At the equilibrium, generation and recombination rate are equal and we can use the Van Roosbroeck-Shockley model to estimate it. We know that the bimolecular recombination equation ($R = Bnp$) gives the number of recombination event per unit volume and time. At the equilibrium $R = R_0 = Bn_i^2$, the equilibrium bimolecular recombination rate is then given by

$$B = \frac{R_0}{n_i^2} \tag{1.37}$$

1.2 NON-RADIATIVE RECOMBINATION

While a radiative event determines the emission of a phonon with an energy equal to the energy gap of the semiconductor, when non-radiative recombination occurs the energy of the electron is transformed into reticular vibration (heat). The presence of defects such as dislocations, impurities and vacancies in the semiconductor structure can be the cause of the generation of energy levels that are localized inside the forbidden-gap thus making non-radiative recombination more likely to happen. These localized states in fact act as "stepping stones" as for example in a recombination event an electron falls from the conduction band to a state that we call a recombination center, and then it falls further into a vacant state in the valence band, thus recombining with a hole.

The recombination through interaction with localized states is described in the so called Shockley-Read-Hall theory.

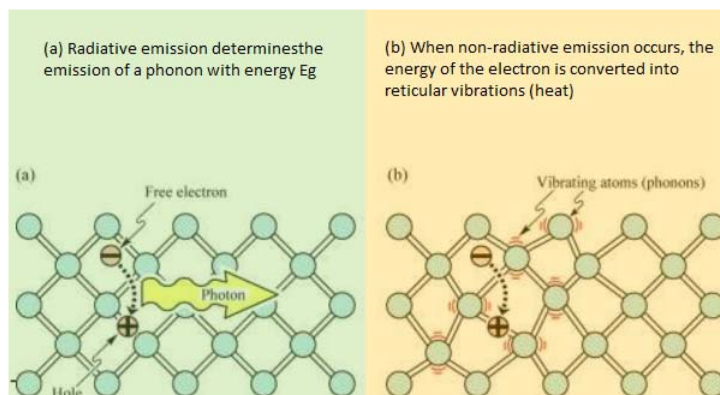


Figure 1.8: *(a) Radiative and (b)non-radiative recombination*

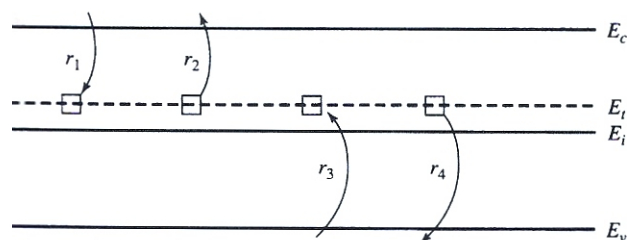


Figure 1.9: *Free carriers can interact with localized states by four processes: $r_1$electron capture, $r_2$electron emission, $r_3$hole capture, and $r_4$hole emission. The localized state shown shown is acceptor type and at energy E_t within the forbidden energy gap.*

1.2.1 SHOCKLEY-HALL-READ RECOMBINATION

In the following picture we can see the four processes through which free carriers can interact with localized states

The illustration shows a density N_t of states at an energy E_t within the forbidden gap. The states shown are acceptor type that is, neutral when empty, negative when full, but the processes described apply also to donor-type states. In the first process, electron capture, an electron falls from the conduction band into an empty localized state. The rate at which the process occurs is proportional to the density of electrons in the conduction band, the density of empty localized states and the probability that an electron passes near a state and is captured by it. The density of empty localized sates is given by the total density N_t, times one minus the probability $f(Et)$ that they are occupied. When thermal equilibrium applies, f is just f_D, the Fermi function

$$f_D(E) = \frac{1}{1 + \exp\left[\left(E - E_f\right)/kT\right]} \tag{1.38}$$

The probability per unit time that an electron is captured by a localized state is given by the product of the electron thermal velocity v_{th} and a parameter σ_n called the *capture cross section*, that is generally determined experimentally for a given type of localized space (the product $v_{th}\sigma$ can be visualized as the volume swept per unit time by a particle with cross section σ_n). We can then write the total rate of capture of electrons by the localized states as

$$r_1 = n\left\{N_t\left[1 - f\left(E_t\right)\right]\right\} v_{th}\sigma_n \tag{1.39}$$

The second process is the inverse of electron capture: that is, electron emission. The emission of an electron from a localized state into the conduction band occurs at a rate given by the product of the density of states occupied by electrons $N_t f(E_t)$ times the probability e_n that the electron makes this jump.

$$r_2 = \left[N_t f\left(E_t\right)\right] e_n \tag{1.40}$$

The emission probability can be expressed in terms of the quantities already defined in the previous equations by considering the capture and emission rates in the limiting case of thermal equilibrium. At thermal equilibrium the rates of capture and emission of carriers must be equal, thus we can write

$$r_1 = r_2 = nN_t\left[1 - f_D\left(E_t\right)\right] v_{th}\sigma_n = N_t f_D\left(E_t\right) e_n \tag{1.41}$$

and

$$e_n = v_{th}\sigma_n n_i \exp\left(\frac{E_t - E_i}{kT}\right) \tag{1.42}$$

From these equations we can observe that the electron emission from the localized states becomes more probable when its energy is closer to the conduction band because $E_t - E_i$ is greater. Corresponding relationships describe the interaction between localized states and the valence band. For example, the process of hole capture is proportional to the density of localized states occupied by electrons $N_t f(E_t)$, the density of holes and a transition probability. This probability can then be described by the product of the thermal velocity v_{th} and the capture cross section σ_p of the hole by the localized state. Thus

$$r_3 = [N_t f(E_t)] p v_{th} \sigma_p \tag{1.43}$$

The fourth process, the hole emission, describes the excitation of an electron from the valence band into an empty localized state. By arguments similar to those for electron emission, hole emission is given by

$$e_p = v_{th} \sigma_p n_i \exp\left(\frac{E_i - E_t}{kT}\right) \tag{1.44}$$

Analogously to the electron case, the probability of emission of a hole from a localized state into the valence band becomes much greater as the energy of the state approaches the valence band edge. Observing the equations previously obtained, it's interesting to consider qualitatively the physics that they represent. First we recognize that at thermal equilibrium $r_1 = r_2$and $r_3 = r_4$. When we have non-equilibrium situation, $r_1 \neq r_2$and $r_3 \neq r_4$. Imagine that the number of holes in a n-type semiconductor is suddenly increased above its thermal equilibrium value. This causes r_3 to increase. The effect of this is the increase of $r_4$and r_1 (both of which eliminate holes at E_t). If most of the holes disappear from E_t via r_1, they remove electrons from the conduction band, and the localized states are effective recombination centers. If the holes are removed from the level at E_t predominantly by an increase in r_4, they return to the valence band, and the sites are effective as hole traps. A given localized state is generally effective in only one way: either as a trap or as a recombination center; if it's closer to a band edge, it is likely to be a carrier trap rather than a recombination center. The equations describing generation and recombination through localized states or recombination centers were originally derived by Shockley, Read and Hall and the process is frequently called the Shockley-Hall-Read recombination. According to the SHR model, when non-equilibrium occurs in a semiconductor, the overall population of electrons and holes in the recombination centers is not greatly affected. The reason for this nearly constant population is that the recombination centers quickly capture majority carriers but have to wait for the arrival of a minority carrier. Thus, the states are nearly always full of carriers, whether under thermal-equilibrium conditions or in non-equilibrium.

To illustrate this behaviour, consider a typical example: acceptor-like recombination centers in an n-type semiconductor. At thermal equilibrium the Fermi level is near $E_c$and, therefore, above the energy of the recombination centers. Hence, they are virtually all filled with electrons and $r_1$and $r_2$are both much greater than $r_3$and r_4. When equilibrium is disturbed by low-level excitation, which increases the number of holes and electrons by the same amount, the electron concentration changes only by a small fraction, while the hole concentration changes by a large

fraction. In this case, $r_1$has to exceed $r_2$by only a very slight amount to accommodate the increased rate of hole capture represented by r_3. Thus, the population of the localized states remains nearly constant, and the net rate of electron capture $r_1 - r_2$equals the net rate of hole capture by the states. These net rates are just the net rate of recombination that we define by symbol U.

$$U = R_{sp} - G_{sp} = r_1 - r_2 = r_3 - r_4 \tag{1.45}$$

where the subscript *sp* stands for *spontaneous*, that is, generation and recombination that respond only to deviation from the thermal equilibrium (in contrast to the spontaneous recombination and generation transitions are those caused by stimulation, for example, by a radiative source). Inserting the expression fro r_1 through $r_4$into the expression for U, we can eliminate f and obtain

$$U = \frac{N_t v_{th} \sigma_n \sigma_p \left(pn - n_i^2\right)}{\sigma_p \left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right] + \sigma_n \left[n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right]} \tag{1.46}$$

$$= \frac{\left(pn - n_i^2\right)}{\tau_{no} \left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right] + \tau_{po} \left[n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right]} \tag{1.47}$$

where $\tau_{no} = (N_t v_{th} \sigma_n)^{-1}$and $\tau_{po} = (N_t v_{th} \sigma_p)^{-1}$.

From these expressions we can observe that U is positive and there is net recombination if the pn product exceeds n_i^2. The sign changes and there is net generation if the pn product is less than n_i^2.

The dependence of U on the energy level of the recombination centers can be more easily grasped by considering the case of equal electron and hole capture cross sections. For $\sigma_p = \sigma_n \equiv \sigma_0$,we can define $\tau_0 \equiv (N_t v_{th} \sigma_0)^{-1}$and, therefore,

$$U = \frac{\left(pn - n_i^2\right)}{\left[p + n + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)\right] \tau_0} \tag{1.48}$$

The dependence on the energy level of the recombination center is contained in the hyperbolic cosine term, that is symmetric around $E_t = E_i$,reflecting a symmetry in the capture of holes and electrons by the center. The denominator has a minimum value at $E_t = E_i$, so that the recombination U is maximum for recombination centers having energies near the middle of the gap, in both generation and recombination. As practical examples, gold and copper give rise to two effective recombination centers, with $(E_t - E_i)$in silicon equal to 0.03 and 0.01 eV respectively.

1.2.1.1 Excess-Carrier Lifetime

To understand the physical significance of the net recombination rate U, we consider a semiconductor with no current flow, in which thermal equilibrium is disturbed by the sudden creation of equal number of excess electrons and holes. These excess carriers then decay spontaneously as the semiconductor returns to thermal equilibrium. Solutions of the continuity equation for this case give the excess electron density as a function of time. We consider this problem under the assumption that the disturbance of equilibrium corresponds to *low-level injection.* If we call the extra injected electron density $n^{'}$and the extra hole density $p^{'}$,then low level injection implies that $n^{'}$and $p^{'}$are both much less than $(n_o + p_o)$, where n_o and p_o represent the thermal-equilibrium densities of carriers in the semiconductor. From these definitions, $n^{'} = n - n_o$ and $p^{'} = p - p_o$, with $n^{'} = p^{'}$.

If $\sigma_n = \sigma_p$ then the continuity equation can be written

$$\frac{dn^{'}}{dt} = G - R = -U = -\frac{(n_o + p_o)\, n^{'}}{\left(n_o + p_o + 2n_i \cosh\left[\frac{E_t - E_i}{kT}\right]\right)} \quad (1.49)$$

Solving for $n^{'}$, we find that the excess carrier density decays exponentially with time

$$n^{'}(t) = n^{'}(0)\exp\left(-t/\tau_n\right) \quad (1.50)$$

where the lifetime τ_n is given by

$$\tau_n = \left[\frac{n_o + p_o + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)}{(n_o + p_o)}\right]\tau_o \quad (1.51)$$

For recombination centers to be effective, the term $E_t - E_i$ is relatively small, and, therefore, the third term in the numerator is negligible compared to the sum of the first two. The equation then reduces to

$$\tau_n = \tau_o = \frac{1}{N_t v_{th} \sigma_o} \quad (1.52)$$

and

$$U = \frac{n^{'}}{\tau_n} \quad (1.53)$$

We can observe that the excess-carrier lifetime is independent of the majority carrier concentration for recombination through recombination centers under low level injection. This behaviour

can be understood physically by considering the kinetics of the recombination process. For example, in a p-type semiconductor, assuming traps near mid gap, most of the recombination centers are empty of electrons because $E_f < E_t$. The recombination process is therefore limited by the capture of electrons from the conduction band. Once an electron is captured by a recombination center, one of the many holes in the valence band is quickly captured. Thus, the rate-limiting step in the recombination process is the capture of a minority carrier by the recombination center; this is insensitive to majority-carrier population.

Minority-carrier lifetimes can vary widely, depending on the density and type of recombination centers in the semiconductor.

1.2.2 AUGER RECOMBINATION

In the SHR recombination, an excess carrier is trapped in an intermediate center until a carrier of the opposite type interacts with the center itself and the two carriers recombine. This kind of recombination dominates at low-to-moderate carrier concentrations because electrons and holes are more likely to interact with the intermediate centers than with the low concentrations of mobile carriers However, at high concentrations, direct interaction of electrons and holes can lead to Auger recombination. In this process, an electron in the conduction band falls into an empty state (hole) in the valence band. The energy emitted by this transition is absorbed by another carrier, which also helps conserve the momentum. Auger recombination is the inverse of the avalanche pair-production process, in which the energy and momentum of an incoming carrier create a hole and an electron. The fact that this process requires three carriers, makes it likely to happen just in highly doped materials or when a large number of excess carrier is present. In n-type materials, two electrons and one hole interact, in p-type materials, two holes and one electron interact. Because two majority carriers are involved, the recombination rate U is proportional to the square of the majority carrier concentration. The Auger recombination rate U_A is given by the expression

$$U_A = R_A - G_A = c_n n \left(pn - n_i^2\right) + c_p p \left(pn - n_i^2\right) \tag{1.54}$$

where c_n and c_p are the Auger recombination coefficients. The reciprocal of the Auger lifetime can be written as

$$\frac{1}{\tau} = c_n N_a^2 \tag{1.55}$$

for electron recombination in heavily doped p-type material. The coefficient c_n for electrons in silicon is approximately $1 \times 10^{-31} cm^{-6} s^{-1}$. The Auger lifetime for holes in n-type material is about one-half to one-third that for electrons in a p-type. The effective lifetime, which considers

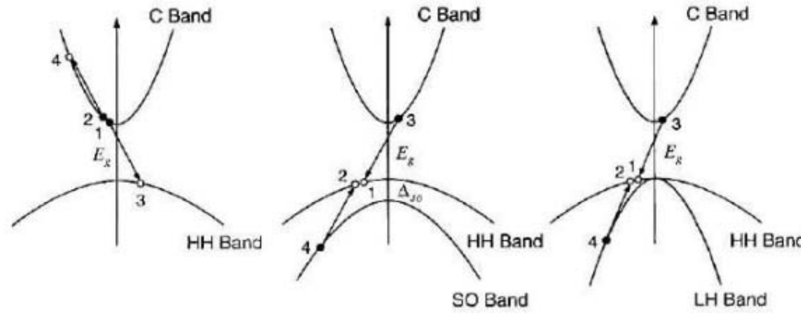


Figure 1.10: *Auger recombination*

both SHR and Auger recombination, is the sum of the recombination rates of the two processes so that

$$\frac{1}{\tau} = \frac{1}{\tau_{SHR}} + \frac{1}{\tau_A} \tag{1.56}$$

1.2.3 SURFACE RECOMBINATION

Thus far, we have considered generation/recombination centers that are uniformly distributed throughout the bulk of the semiconductor material. In practical cases the surface can be the location of an abundance of extra localized states having energies within the forbidden gap. The presence of a passivating layer of silicon dioxide over the semiconductor surface, as is usual in devices made by the planar process, ties up many of the bonds that would otherwise contribute to surface states and protects the surface from foreign atoms. A passivating oxide can reduce the density of surface states from about 10^{-15} $cm^{-2}$to less than $10^{11}cm^{-2}$. Even with passivated surface , however, surface states provide generation-recombination centers in addition to those present in the bulk.

The kinetics of generation-recombination at the surface are similar to those considered for bulk centers with one significant exception. While we considered the volume density $N_t(cm^{-3})$ of bulk centers, we must discuss the area density $N_{st}(cm^{-2})$ of surface centers. Although the $N_{st}(cm^{-2})$ surface centers can be distributed over a thickness of several atomic layers, the poorly defined atomic structure near the semiconductor surface makes useful a description in terms of an equivalent number of states located at the surface. We can write an expression for the recombination rate U per unit area at the surface analogous to the Schockley-Hall-Read case.

$$U_s = \frac{N_{st}v_{th}\sigma_n\sigma_p(p_s n_s - n_i^2)}{\sigma_p[p_s + n_i\exp(\frac{E_i - E_{st}}{kT})] + \sigma_n[n_s + n_i\exp(\frac{E_{st} - E_i}{kT})]} \tag{1.57}$$

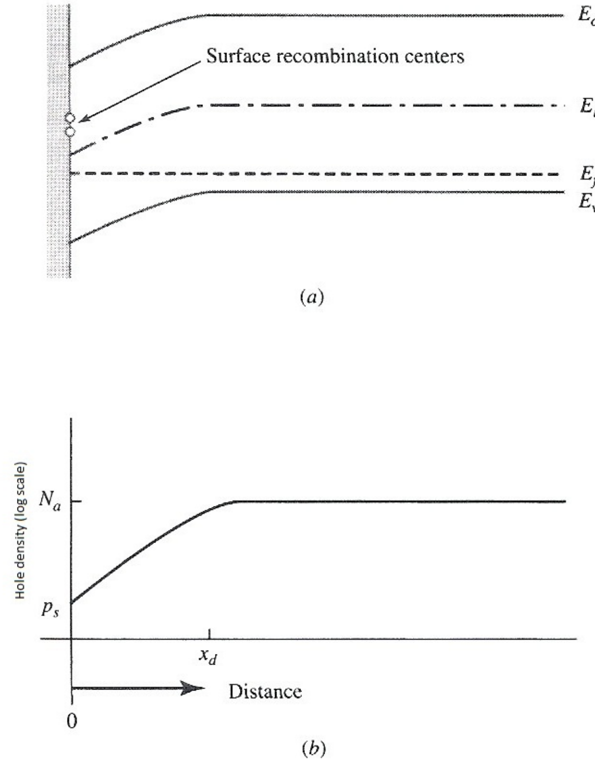


Figure 1.11: *(a) Sketch of the energy-band diagram near the surface of p-type silicon covered with a passivating oxide. (b) Hole density near the surface*

where the subscript s denotes concentrations and conditions near the surface and $E_{st}$is the energy of the surface generation/recombination centers. To stress the physical significance of surface recombination, we simplify the mathematics by considering the most efficient centers, which are located near mid gap, and equal capture cross sections for electrons and holes. With these assumptions the recombination rate equation reduces to

$$U_s = N_{st} v_{th} \sigma \frac{(p_s n_s - n_i^2)}{p_s + n_s + 2n_i \cosh\left(\frac{E_{st}-E_i}{kT}\right)} \tag{1.58}$$

The surface of a semiconductor is often at a different potential than the bulk so that surface carriers concentrations can differ from their values in the neutral bulk region. Even in the case of oxide-passivated surfaces, a space-charge region generally forms near the surface of the semiconductor. Dopant segregation at the oxide-silicon interface causes silicon surfaces to be less strongly p-type or more strongly n-type than the bulk. If we assume that the pn product remains constant throughout the space-charge region, the product at the surface $p_s n_s$ can be expressed in terms of quantities at the neutral edge of the space-charge region:

$$p_s n_s = p_p(x_d) n_p(x_d) \approxeq N_a n_p(x_d) \tag{1.59}$$

in a p-type semiconductor. The recombination rate equation can then be written

$$U_s = N_{st} v_{th} \sigma \frac{N_a[n_p(x_d) - n_{p0}]}{(p_s + n_s + 2n_i)} = N_{st} v_{th} \sigma \frac{N_a}{(p_s + n_s + 2n_i)} n_p^{'}(x_d) \tag{1.60}$$

where we have assumed $E_{st} \approxeq E_i$. In this equation we have expressed the surface recombination rate U_s in terms of of the deviation $n_p^{'}$ of the minority carrier (electron) concentration from its equilibrium value at the interior boundary of the surface space charge region.

The coefficient of $n_p^{'}$on the right of the equation is usually defined as a parameter s, which describes the characteristics of the surface recombination process:

$$s = N_{st} v_{th} \sigma \frac{Na}{(p_s + n_s + 2n_i)} \tag{1.61}$$

The value of s depends on the physical nature and density of the surface generation/recombination centers as well as on the potential at the surface. If the surface region is depleted of mobile carriers, $n_s$and p_s are small and s is large. If the surface is neutral, $p \approxeq N_a$; s is small and is given by

$$s = s_o = N_{st} v_{th} \sigma \tag{1.62}$$

where the subscript o denotes that the surface and the bulk are at the same potential; that is, the surface region is neutral. The dependence of s on surface potential is important in silicon integrated circuits.

The dimensions of s are $cm\, s^{-1}$, and s is consequently called the $surface\, combination\, velocity$, although it is not directly related to an actual velocity. A physical interpretation of $s$can be obtained comparing the previous equation with the one that gives the minority-carriers lifetime; s is related to the rate at which excess carriers recombine at the surface, just as $\frac{1}{\tau}$ is related to the rate at which they recombine at the bulk.

1.3 QUANTUM EFFICIENCY

Radiative and non-radiative recombination processes are in competition one with the other, especially in optoelectronic devices, where we an increase in the second makes the efficiency of the device decrease. In a semiconductor with non-radiative recombination centers, the total recombination probability is given by

$$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} \tag{1.63}$$

thus the probability of having radiative emission is defined as

$$\eta_{int} = \frac{\frac{1}{\tau_r}}{\frac{1}{\tau_r} + \frac{1}{\tau_{nr}}} \tag{1.64}$$

The parameter η_{int} is called *internal quantum efficiency*, and is the ratio between the number of phonons emitted and the total number of carriers that recombine. It's important to notice that, in a real device, not all the phonons emitted will be able to exit the material, come of them will be in fact refracted and re-absorbed.

We have seen that non-radiative recombination is a big problem in optoelectronic devices and it is not possible to avoid it, but even if it is not possible to make it completely disappear, there are some ways to reduce it, increasing the internal quantum efficiency. In general, because of the fact that non-radiative recombination is strongly connected to the material quality, we should increase it, reducing the defects densities, but we could also use some tricks to reduce surface recombination, like designing the device with the active region far enough from the surface and we could also increase the volume of the recombination region to decrease carriers densities and thus Auger recombination. Despite the fact that it's not possible to produce pure materials (in fact the impurities concentration is always higher than $10^{12} cm^{-3}$) in the last fifty years things have greatly improved and through the optimization of fabrication and growth processes, the internal quantum efficiency has gone from 1% to 90/95%.

Chapter 2

LED DEVICES

2.1 LED ELECTRICAL PROPERTIES

2.1.1 HOMOJUNCTION STRUCTURE AND ELECTRICAL MODEL

To understand the LEDs properties, we can start analyzing the pn homojunction, in fact LED devices are diodes, even if with some particular characteristics.

The I-V law of a LED device is the same of a pn junction

$$I = I_s \left(e^{qV/kT} - 1 \right) \tag{2.1}$$

with

$$I_s = qA \left(\sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_A} \right) \tag{2.2}$$

As usual if $V \gg \frac{kT}{q}$ we can simplify the I-V relation and write

$$I_s = qA \left(\sqrt{\frac{D_p}{\tau_p}} N_A + \sqrt{\frac{D_n}{\tau_n}} N_D \right) e^{q(V-V_D)/kT} \tag{2.3}$$

We know that

$$V_D = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) \tag{2.4}$$

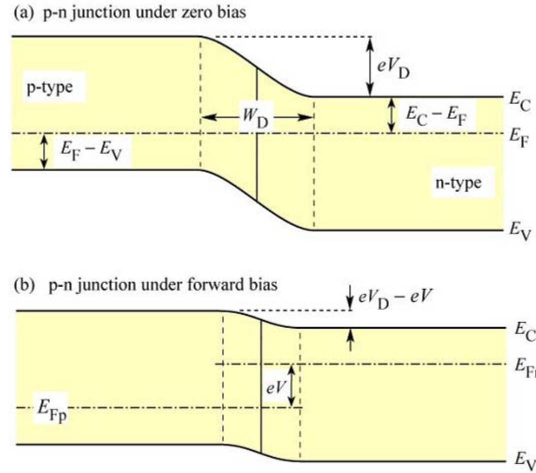


Figure 2.1: *P-n junction under (a)zero bias and (b)forward bias*

$$qV_D - E_G + (E_F - E_V) + (E_C - E_F) = 0 \tag{2.5}$$

In a highly doped semiconductor $E_C - E_F \ll E_G$, $E_F - E_V \ll E_G$, furthermore $E_C - E_F$ and $E_F - E_V$ weakly depend on the doping level. We can thus write

$$V_{th} \approx V_D \approx E_G/q \tag{2.6}$$

Under direct polarization conditions, the Shockley diode equation is usually simplified in the following way

$$I = I_s e^{qV/(\eta_{ideal} kT)} \tag{2.7}$$

where η_{ideal} is the diode ideality factor. For an ideal diode, this parameter value is one, while for real devices it's higher. In a homojunction diode this parameter is higher than one, but normally lower than than tow, in heterojunctions (that as we will see later are very important for LED devices) instead, it can be even higher, in fact in these cases the externally measured ideality factor, is the sum of the ideality factors of the individual rectifying junctions, changing the I-V of the LEDs with respect to the ideal diode.

Another important parameter that influences the real device I-V, is the parasitic resistance. The effects of this resistance can be modeled through two circuital elements, a series resistance and a shunt resistance in parallel to the ideal diode. These two parameters strongly affect the real device characteristics, and an example of their effects can be seen in the following image. In figure (a) we can see the effects of the shunt and the series resistances, while in figure (b) we see the sub-threshold turn-on caused bu the shunt resistance only.

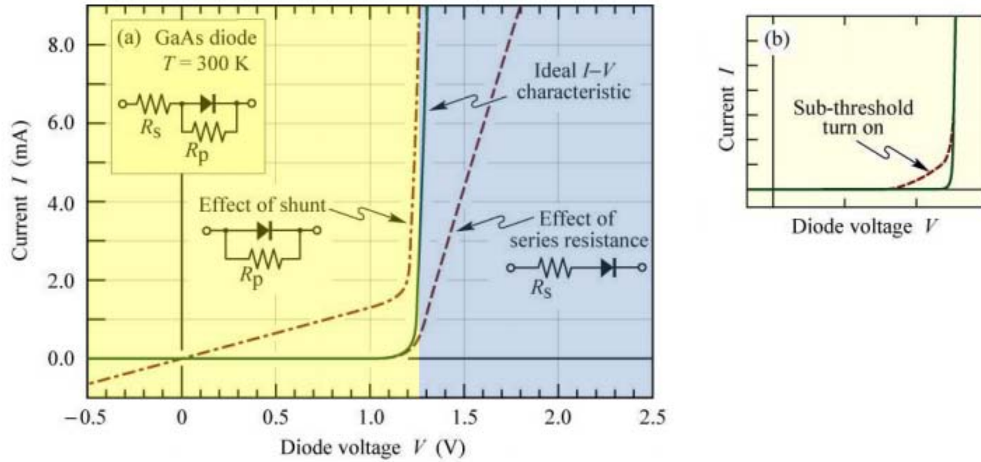


Figure 2.2: *(a) Effect of series and parallel resistance (shunt) on I-V characteristic. (b) I.V with clearly discernible sub-threshold turn-on caused by defects or surface states*

2.1.2 HETEROJUNCTION STRUCTURE

We have seen that the radiative recombination rate is proportional to the product of the electrons and holes concentration, it is therefore important to observe the distribution of carriers under direct polarization conditions, to understand if the homojunction structure is suitable for LEDs fabrication.

A useful parameter to analyze this situation is the diffusion length, that we can evaluate using the following equations

$$L_n = \sqrt{D_n \tau_n} \ , \ \ L_p = \sqrt{D_p \tau_p} \ , \tag{2.8}$$

knowing that

$$D_n = \frac{kT}{q}\mu_n \ , \ \ D_p = \frac{kT}{q}\mu_p \tag{2.9}$$

In a LED based on a homojunction structure, carriers recombine in a region with a length of about $3/4$ times the diffusion length $L_{p,n}$ (carriers diffuse on average over the diffusion lengths before recombining).

This is a problem for a LED, in fact it reduces radiative efficiency because it doesn't allow to have high concentrations of both holes and electrons in the same region ($R = Bnp$). To increase the device efficiency, it's useful to reduce the width recombination region, and to make this, double heterostructures are used. When this solution is employed, the dimension of the active region is determined by the geometry of the device, and not by the diffusion length anymore, we have in fact built a so called *quantum well*. Suppose that the active region were about $10 - 100\,nm$ long, this shows clearly the improvement in the efficiency over the homojunction case, in which carriers can diffuse for several μm.

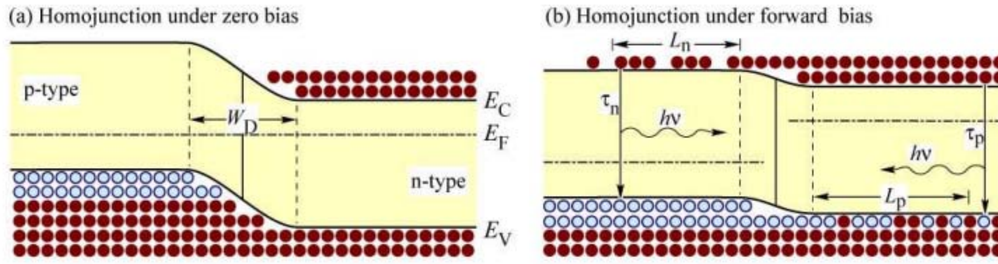


Figure 2.3: *Carriers diffusion and recombination in an homojunction LED under (a)zero bias and (b)forward bias.*

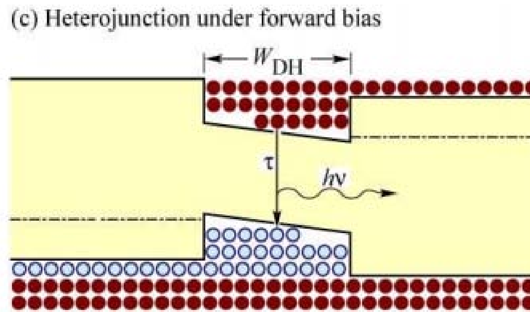


Figure 2.4: *P-n heterojunction under forward bias. Carriers are confined by the barriers.*

2.1.3 QUANTUM WELL

2.1.3.1 THE INFINITE SQUARE-SHAPED QUANTUM WELL

The infinite.square shaped well potential is the simplest of all possible potential wells, and is defined as

$$U(x) = 0 \qquad \left(-\frac{1}{2}L \leq x \leq \frac{1}{2}L\right) \tag{2.10}$$

$$U(x) = \infty \qquad \left(|\,x\,| > \frac{1}{2}L\right) \tag{2.11}$$

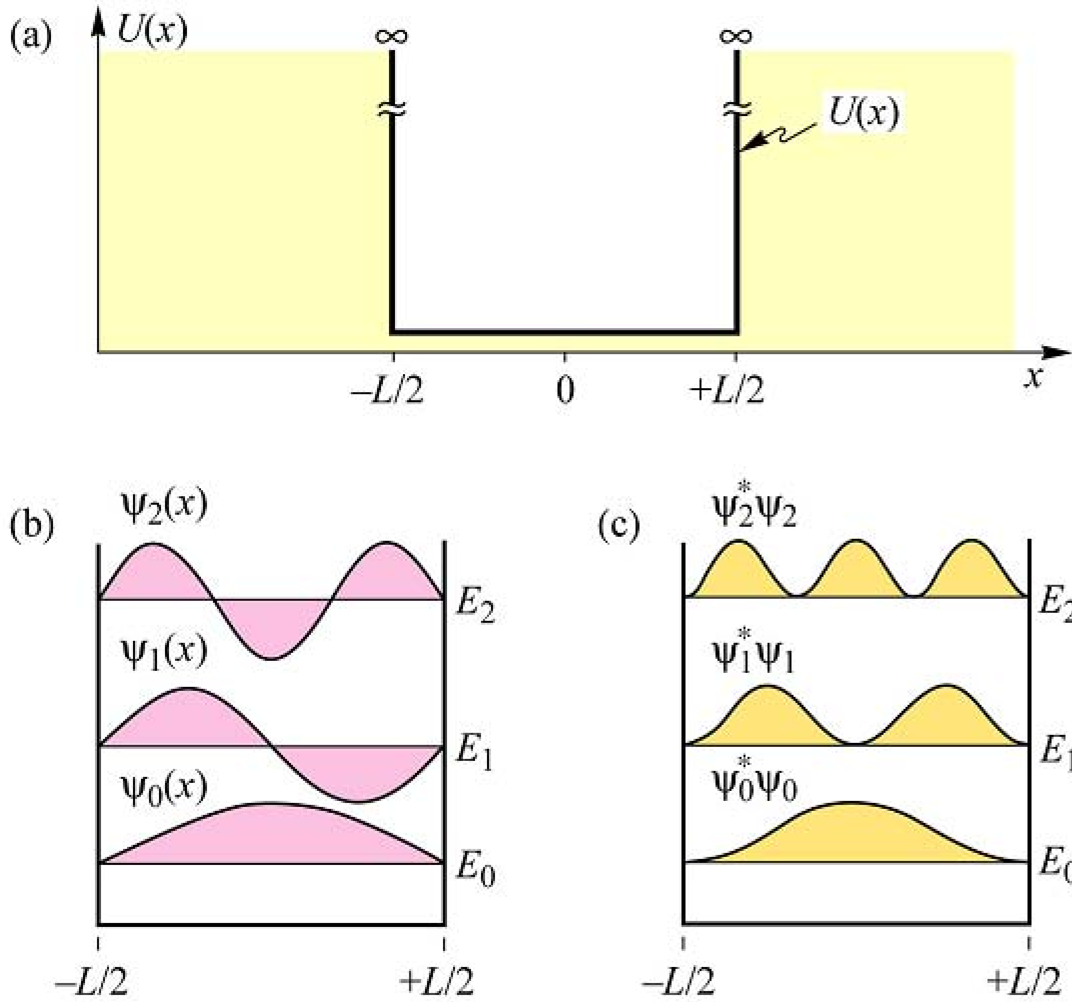


Figure 2.5: *(a) Schematic illustration of the infinite square well potential. The solutions of this potential well are shown in terms of (b) eigenfunctions* $\psi_n(x)$*, (b) eigenstate energies* E_n*, and (c) probability densities* $\psi_n^*\psi_n$*.*

To find the stationary solutions for $\psi_n(x)$ and $E_n we$must find functions for $\psi_n(x)$,which satisfy the Schrödinger equation. The time-independent The time-independent Schrödinger equation contains only the differential operator d/dx, whose eigenfunctions are exponential or sinusoidal functions. Since the Schrödinger equation has the form of an eigenvalue equation, it is reasonable to try only eigenfunctions of the differential operator. Furthermore, we assume that$\psi_n(x) = 0$ for$|x| > L/2$, because the potential energy is infinitely high in the barrier regions. Since the 3rd Postulate of quantum mechanics requires that the wave function be continuous, the wave function must have zero amplitude at the two potential discontinuities, that is $\psi_n(x = \pm L/2) = 0$. We therefore employ sinusoidal functions and differentiate between states of even and odd symmetry. We write for even-symmetry states

$$\psi_n(x) = A\cos\left[\frac{(n+1)\pi x}{L}\right] \quad \left(n = 0\,,\ 2\,,\ 4 ... and\ |x| \leq \frac{L}{2}\right) \tag{2.12}$$

and for odd symmetry states

$$\psi_n(x) = A\sin\left[\frac{(n+1)\,\pi x}{L}\right] \quad \left(n = 1\,,\,3\,,\,5...and\ |x| \leq \frac{L}{2}\right) \tag{2.13}$$

Both functions have a finite amplitude in the well-region ($|x| \leq L/2$) and they have zero amplitude in the barriers, that is

$$\psi_n(x) = 0 \quad \left(n = 0\,,\,1\,,\,2...and\ |x| > \frac{L}{2}\right) \tag{2.14}$$

The shapes of the three lowest wave functions ($n = 0, 1, 2\ldots$) are shown in *Figure 2.5*. In order to normalize the wave functions, the constant A must be determined. The condition $< \psi|\psi >= 1$ yields

$$a = \sqrt{2/L} \tag{2.15}$$

One can verify that the previous sinusoidal equations are solutions of the infinite square well by inserting the normalized wave functions into the Schrödinger equation. Insertion of the ground-state wave function ($n = 0$) into the Schrödinger equation yields

$$-\frac{\hbar^2}{2m}\frac{d^2}{dx^2}\sqrt{\frac{2}{L}}\cos\left(\frac{\pi x}{L}\right) = E_0\sqrt{\frac{2}{L}}\cos\left(\frac{\pi x}{L}\right) \tag{2.16}$$

Calculating the derivative on the left-hand side of the equation yields the ground state energy of the infinite square well

$$E_0 = \frac{\hbar^2}{2m}\left(\frac{\pi}{L}\right)^2 \tag{2.17}$$

The excited state energies ($n = 1, 2, 3\ldots$) can be evaluated analogously. One obtains the eigenstate energies in the infinite square well as

$$E_n = \frac{\hbar^2}{2m}\left[\frac{(n+1)\,\pi}{L}\right] \quad (n = 0, 1, 2...) \tag{2.18}$$

The spacing between two adjacent energy levels, that is$E_n - E_{n-1}$, is proportional to n. Thus, the energetic spacing between states increases with energy.

The probability density of a particle described by the wave function ψ is given by $\psi \times \psi$ (2nd Postulate). The eigenstate energies are, as already mentioned, expectation values of the total energy of the respective state. It is therefore interesting to know if the eigenstate energies are purely kinetic, purely potential, or a mixture of both. The expectation value of the kinetic energy of the ground state is calculated according to the 5th Postulate:

$$< E_{Kin,0} >=< \psi_0|\frac{p^2}{2m}|\psi_0 > \tag{2.19}$$

Using the momentum operator $p = \left(\frac{\hbar}{i}\right)\left(\frac{d}{dx}\right)$ one obtains the expectation value of the kinetic

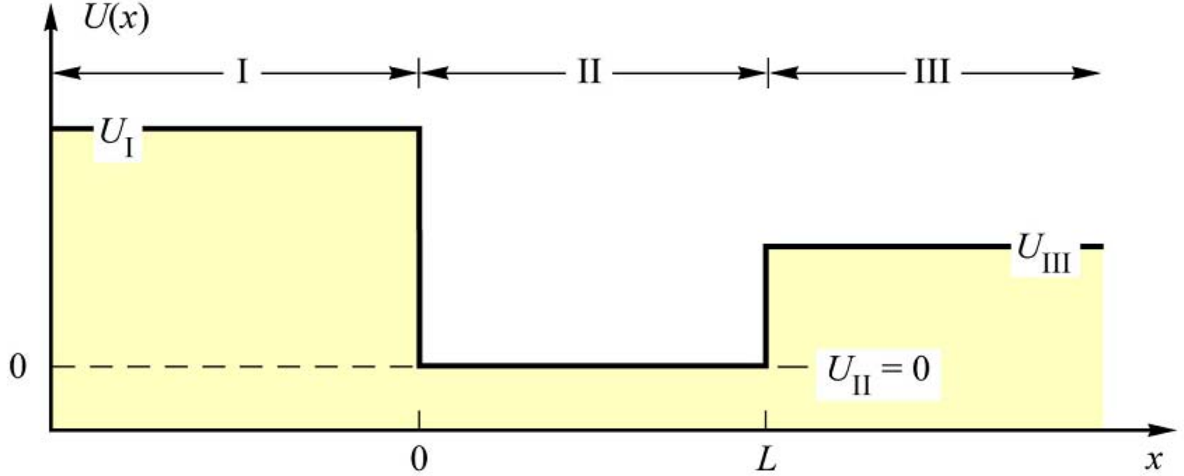


Figure 2.6: *Asymmetric square well potential with well width L and barrier heights U_I and U_{III}.*

energy of the ground state

$$< E_{kin,0} >= \frac{\hbar^2}{2m}\left(\frac{\pi}{L}\right)^2 \tag{2.20}$$

which is identical to the total energy given in Eq. (2.17). Evaluation of kinetic energies of all other states yields

$$< E_{kin,0} >= \frac{\hbar^2}{2m}\left[\frac{(n+1)\,\pi}{L}\right]^2 \tag{2.21}$$

The kinetic energy coincides with the total energy given in Eq. (2.18). Thus, the energy of a particle in an infinite square well is purely kinetic. The particle has no potential energy.

2.1.3.2 THE ASYMMETRIC AND SYMMETRIC FINITE SQUARE-SHAPED QUANTUM WELL

In contrast to the infinite square well, the finite square well has barriers of finite height and considering the asymmetric well, the two barriers have a different height.

The potential energy is constant within the three regions I, II, and III, as shown in *Figure 2.6*. In order to obtain the solutions to the Schrödinger equation for the square well potential, the solutions in a constant potential will be considered first. Assume that a particle with energy E is in a constant potential U. Then two cases can be distinguished, namely $E > U$ and $E < U$. In the first case ($E > U$) the general solution to the time- independent one-dimensional Schrödinger equation is given by

$$\psi\,(x) = A\cos\,(kx) + B\sin\,(kx) \tag{2.22}$$

where A and B are constants and

$$k = \sqrt{2mE/\hbar^2} \tag{2.23}$$

Insertion of the solution into the Schrödinger equation proves that it is indeed a correct solution. Thus the wave function is an oscillatory sinusoidal function in a constant potential with $E > U$. In the second case ($E < U$), the solution of the time-independent one-dimensional Schrödinger equation is given by

$$\psi\left(x\right) = Ce^{\kappa x} + De^{\kappa x} \tag{2.24}$$

where C and D are constants and

$$\kappa = \sqrt{\frac{2m\left(U-E\right)}{\hbar^2}} = \sqrt{\frac{2mU}{\hbar^2} - k^2} \tag{2.25}$$

Again, the insertion of the solution into the Schrödinger equation proves that it is indeed a correct solution. Thus the wave function is an exponentially growing or decaying function in a constant potential with$E < U$. Next, the solutions of an asymmetric and symmetric square well will be calculated. The potential energy of the well is piecewise constant, as shown in *Figure 2.6*. Having shown that the wave functions in a constant potential are either sinusoidal or exponential, the wave functions in the three regions I ($x \leq 0$), II ($0 < x < L$), and III ($x \geq L$), can be written as

$$\psi_I\left(x\right) = Ae^{\kappa_I x} \tag{2.26}$$

$$\psi_{II}\left(x\right) = A\cos\left(kx\right) + B\sin\left(kx\right) \tag{2.27}$$

$$\psi_{III}\left(x\right) = \left[A\cos\left(kL\right) + B\sin\left(kL\right)\right]e^{-\kappa_{III}\left(x-L\right)} \tag{2.28}$$

where A and B are unknown normalization constants. In this solution, the first boundary condition of the 3rd Postulate, i. e. $\psi_I(0) = \psi_{II}\left(0\right)$ and $\psi_{II}\left(L\right) = \psi_{III}\left(L\right)$, is already satisfied. From the second boundary condition of the 3rd Postulate, i. e. $\psi_I'\left(0\right) = \psi_{II}'\left(0\right)$ and $\psi_{II}'\left(L\right) = \psi_{III}'\left(0\right)$, the following two equations are obtained

$$A\kappa_I - Bk = 0 \tag{2.29}$$

$$A\left[\kappa_{III}\cos\left(kL\right)-k\sin\left(kL\right)+\right]+B\left[\kappa_{III}\sin\left(kL\right)+k\cos\left(kL\right)\right] \tag{2.30}$$

This homogeneous system of equations has solutions, only if the determinant of the system vanishes. From this condition, one obtains

$$\tan kL=\frac{kL\left(\kappa_{I}L+\kappa_{III}L\right)}{k^{2}L^{2}-\kappa_{I}L\kappa_{III}L} \tag{2.31}$$

which is the eigenvalue equation of the finite asymmetric square well. For the finite symmetric square well, which is of great practical relevance, the eigenvalue equation is given by

$$\tan kL=\frac{2kL\kappa L}{k^{2}L^{2}-\kappa L^{2}} \tag{2.32}$$

where $\kappa=\kappa_{II}=\kappa_{III}$. If κ is expressed as a function of k, then Eq. (2.32) depends only on a single variable, i. e., k. Solving the eigenvalue equation yields the eigenvalues of k and, by using Eqs. (2.23) and (2.25), the allowed energies E and decay constants κ, respectively. The allowed energies are also called the eigenstate energies of the potential. Inspection of Eq. (2.32) yields that the eigenvalue equation has a trivial solution $kL=0$ (and thus $E=0$) which possesses no practical relevance. Non-trivial solutions of the eigenvalue equation can be obtained by a graphical method. *Figure 2.7* shows the graph of the left-hand and right-hand side of the eigenvalue equation. The dashed curve represents the right-hand side of the eigenvalue equation. The intersections of the dashed curve with the periodic tangent function are the solutions of the eigenvalue equation. The quantum state with the lowest non-trivial solution is called the ground state of the well. States of higher energy are referred to as excited states.

The dashed curve shown in *Figure 2.7* has two significant points, namely a pole and an end point. The dashed curve has a pole when the denominator of the right-hand side of the eigenvalue equation vanishes, i. e., when $kL=\kappa L$. Using Eq (2.25), it is given by

Pole:

$$kL_{|Pole}=\sqrt{mU/\hbar^{2}}L \tag{2.33}$$

The dashed curve ends when $k=(2mU/\hbar^{2})^{\frac{1}{2}}$. If k exceeds this value, the square root in Eq (2.25) becomes imaginary. The end point of the dashed curve is thus given by *End Point:*

$$kL_{|End\,Point}=\sqrt{2mU/\hbar^{2}}L \tag{2.34}$$

There are no further bound state solutions to the eigenvalue equation beyond the end point.

Now that the eigenvalues of k and κ are known, they are inserted into Eqs. (2.29) and (2.30); this allows for the determination of the constants A and B and the wave functions. Thus the allowed energies and the wave functions of the square well have been determined. It is possible to show that all states with even quantum numbers $(n=0,1,2\ldots)$ are of even symmetry with respect to the center of the well, i. e. $\psi\left(x\right)=\psi\left(-x\right)$. All states with odd quantum numbers

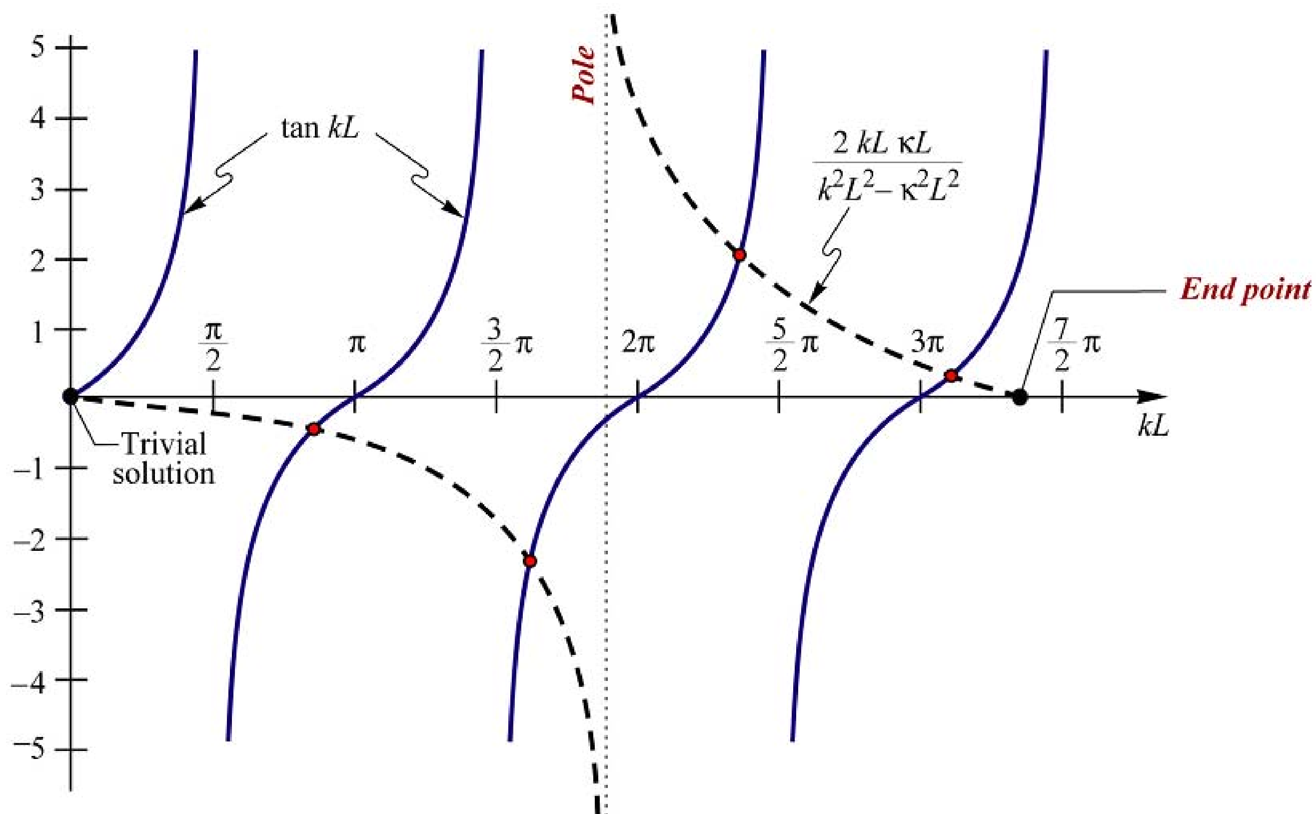


Figure 2.7: *Graphical solution of the eigenvalue equation for a symmetric quantum well. The function* $2kL\kappa L/\left(k^2L^2-\kappa^2L^2\right)$ *is the right-hand side of the eigenvalue equation. The crossing points of the tangent function and the dashed curve are solutions of the eigenvalue equation. The solution at* $kL=0$ *is a trivial solution having no practical relevance.*

$(n = 1, 3, 5 \ldots)$ are of odd symmetry with respect to the center of the well, i. e. $\psi(x) = -\psi(-x)$. The even and odd state wave functions in the well are thus of the form

$$\psi_{II}(x) = A_{11} \cos\left[k_n \left(x - \frac{L}{2}\right)\right] \qquad (for\ n = 0, 2, 4...) \tag{2.35}$$

and

$$\psi_{II}(x) = A_{11} \sin\left[k_n \left(x - \frac{L}{2}\right)\right] \qquad (for\ n = 1, 3, 5...) \tag{2.36}$$

The three lowest wave functions of a symmetric square well are shown in

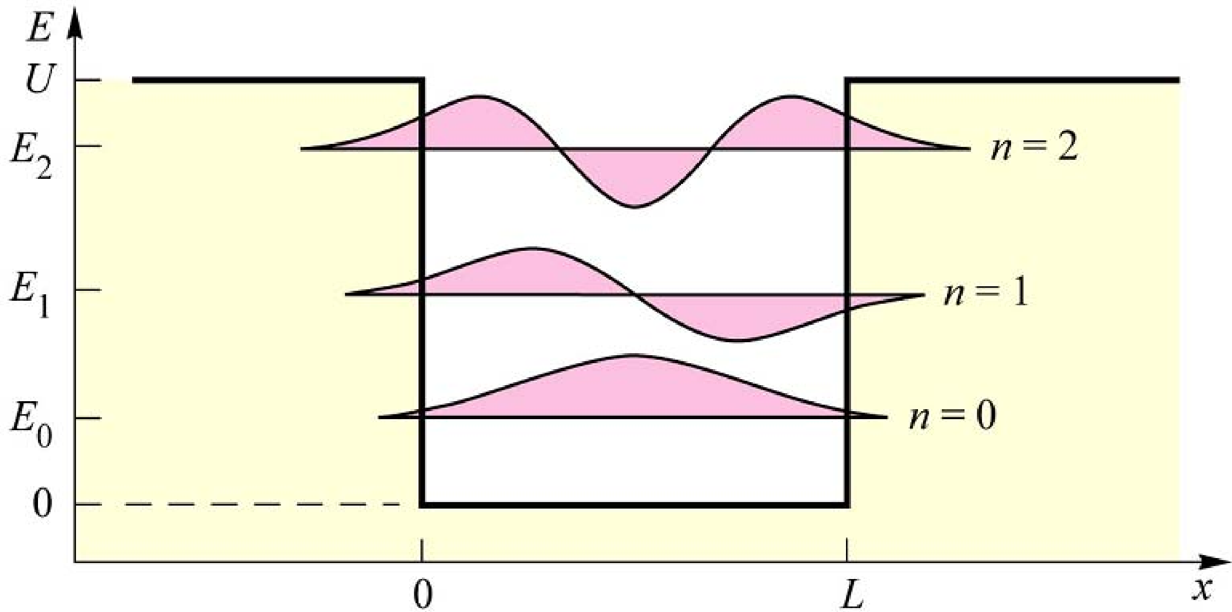


Figure 2.8: *Schematic illustration of the three lowest wave functions of the symmetric quantum well.*

2.1.4 OTHER NONIDEALITIES AND CHARACTERISTICS

In practice, active region are not infinite-square shaped quantum wells, and even though barriers are usually higher than $\frac{kT}{q}$, some of the carriers can have enough energy to escape the well. This phenomenon is called *carrier escape*.

$$n_B = \int_{E_B}^{\infty} \rho_{dos} f_{FD}(E)\, dE \tag{2.37}$$

Another important leakage mechanism is the so called *carrier overflow.* When current becomes higher, the carriers concentration and Fermi energy increase, thus carriers can travel the quantum well without being captured, and radiative efficiency decreases.

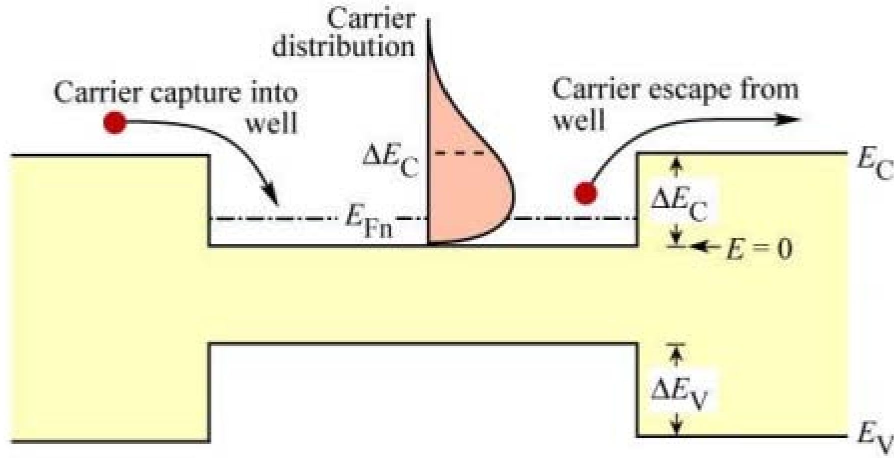


Figure 2.9: *Carrier capture and escape in a double heterostructure. Also shown is the carrier distribution in the active layer.*

Considering a double heterostructure LED, with an active region with width W_{DH}, the continuity equation is

$$\frac{dn}{dt} = \frac{J}{qW_{DH}} - Bnp \tag{2.38}$$

In stationary condition ($\frac{dn}{dt} = 0$) and high injection hypothesis ($n = p$) we can write

$$n = \sqrt{\frac{J}{qBW_{DH}}} \tag{2.39}$$

In these conditions it can be demonstrated that the following equation is also valid

$$\frac{E_F - E_C}{kT} = \left(\frac{3\sqrt{\pi}}{4}\frac{n}{N_C}\right)^{\frac{2}{3}} \tag{2.40}$$

In high injection conditions the Fermi energy increases and can reach the barrier value ($E_F - E_C = \Delta E_C$). Carrier overflow takes place when

$$\frac{\Delta E_C}{kT} = \left(\frac{3\sqrt{\pi}}{4}\frac{n}{N_C}\right)^{\frac{2}{3}} \Longrightarrow \left(\frac{\Delta E_C}{kT}\right)^{\frac{3}{2}} = \frac{3\sqrt{\pi}}{4}\frac{n}{N_C} \Longrightarrow n^2 = \left(\frac{\Delta E_C}{kT}\right)^3 \left(\frac{4N_C}{3\sqrt{\pi}}\right)^2 \tag{2.41}$$

We can exploit this result and write

$$J = qW_{DH}Bn^2 = \left(\frac{\Delta E_C}{kT}\right)^3 \left(\frac{4N_C}{3\sqrt{\pi}}\right)^2 qBW_{DH} \tag{2.42}$$

To reduce the influence of this undesired phenomenon multiple quantum-wells structures have been developed together with the introduction of electron blocking layers, pieces of different materials that change the band-diagram and prevent the carriers from flowing away from the wells.

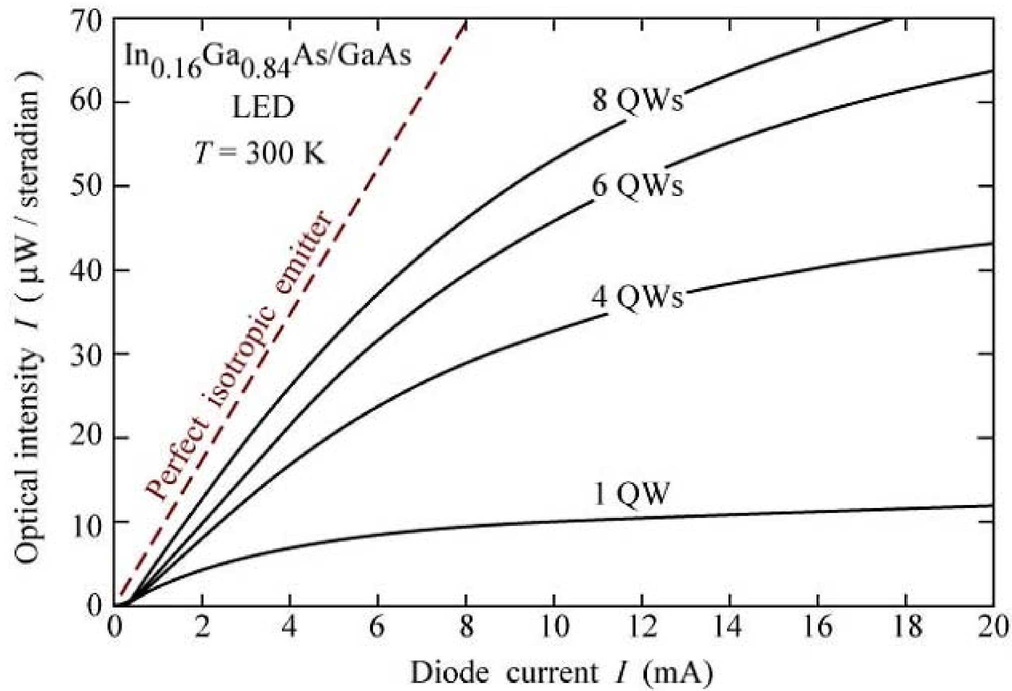


Figure 2.10: *Optical intensity emitted by $In_{0.16}Ga_{0.84}As/GaAs$ LEDs with active regions consisting of one, four, six and eight quantum wells and theoretical intensity of a perfect isotropic emitter (dashed line).*

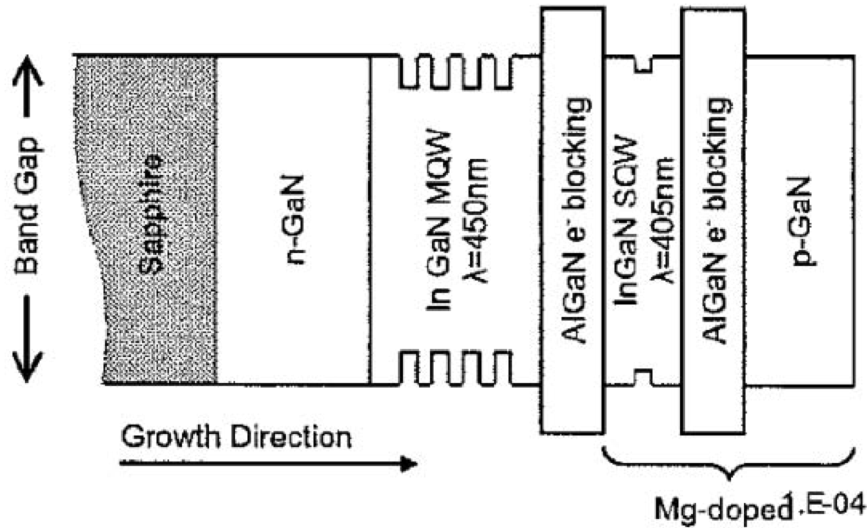


Figure 2.11: *An example of multi-quantum well with electron blocking layer structure.*

There's also another problem in the heterostructures, the parasitic resistance, due to the parabolic shape of the band diagram. This problem can be solved using a graded change in the composition of the material.

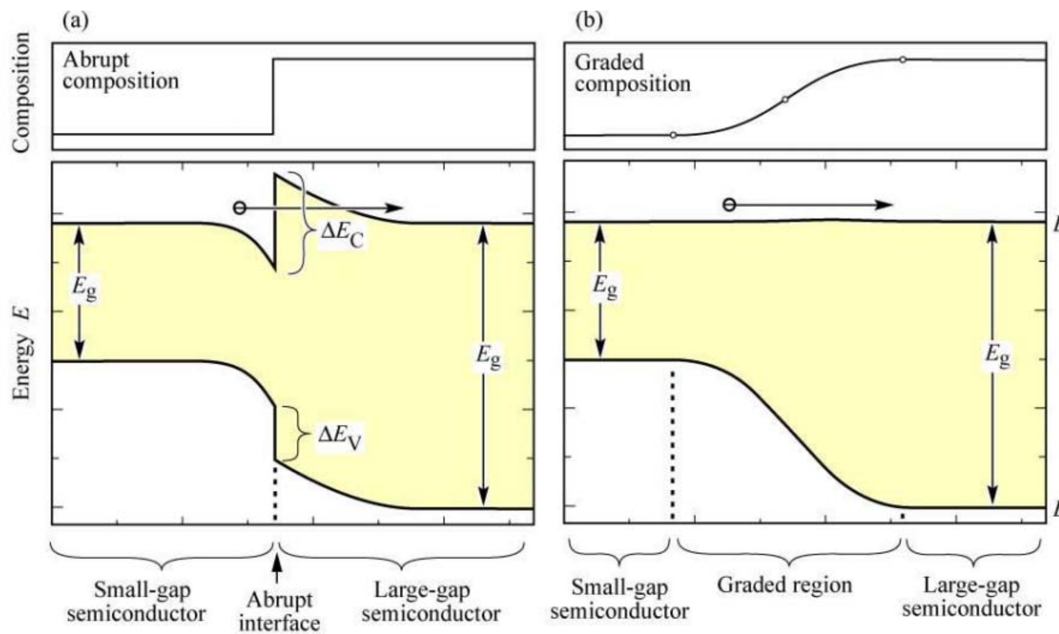


Figure 2.12: *(a) Band diagram of an abrupt n-type - n-type heterojunction and (b) a graded heterojunction of two semiconductors with different band gap energy. The abrupt junction is more resistive than the graded junction due to the electron barrier forming at the abrupt junctions.*

2.2 LED OPTICAL PROPERTIES

2.2.1 EFFICIENCY

The efficiency of a LED device is a complex parameter, that can be defined and calculated in different ways. In fact, the overall efficiency can be written as

$$\eta_0 = \eta_{inj}\eta_r\eta_{extraction} \tag{2.43}$$

where η_{inj} is the *injection efficiency*, $\eta_r$the radiative efficiency and $\eta_{extraction}$ is the extraction efficiency.

The injection efficiency takes into account the fact that not all of the carriers injected reach the active region to give recombination, and is given by

$$\eta_{inj} = \left(1 + \frac{\mu_h N_A L_e}{\mu_e N_D L_h}\right)^{-1} \tag{2.44}$$

The second parameter on which the overall efficiency depends, the radiative efficiency η_r, is calculated through the following equation

$$\eta_r = \frac{1}{1 + \tau_r/\tau_{NR}} \tag{2.45}$$

and describes how many of the carriers that recombine, do it in a radiative way. As we already explained in chapter 1, this quantity strongly depends on the material quality.

The product $\eta_{inj}\eta_r$ gives the so called *internal quantum efficiency*, that is defined as the ratio between the number of phonons emitted from the active region per second, and the number of electrons injected into the LED per second

$$\eta_{int} = \frac{(P_{int}/h\nu)}{(I/q)} \tag{2.46}$$

where $P_{int}$is the optical power emitted from the active region, and I the injected current. In an ideal LED this efficiency is one, because in it each charge quantum-particle (electron) produces one light quantum-particle (photon).

The last parameter in Eq. (2.43) is the extraction efficiency $\eta_{extraction}$. This is defined as the ration between the number of photons emitted from the LED's package per second, and the number of phonons emitted from the active region per second. It can be calculated also as

$$\frac{(P/h\nu)}{(P_{int}/h\nu)} \tag{2.47}$$

where P is the optical power emitted from the LED (package included). The extraction efficiency

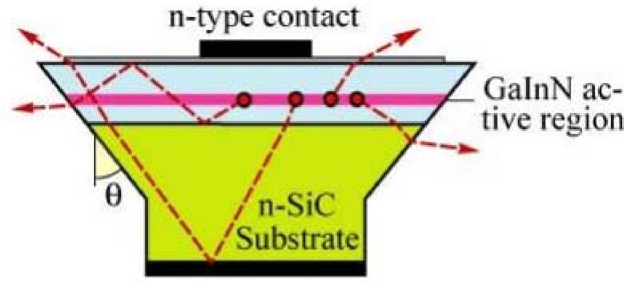


Figure 2.13: *Phonons emission and reflection in a GaInN LED.*

is usually less than 100% because not all of the photons emitted can escape from the LED; in fact these photons can be trapped inside the semiconductor because of what we call *"total internal reflection"*, that is a multiple reflections phenomenon, and they can be absorbed by the metal contacts or the semiconductor itself, if they have higher energy than the band-gap E_g.

We can finally define the *external quantum efficiency* η_{ext} as the ratio between the number of phonons emitted outside the package per second, and the number of electrons injected into the LED per second

$$\frac{(P/h\nu)}{(I/q)} = \eta_{int}\eta_{extraction} \tag{2.48}$$

where P is the optical power emitted outside the package and I the injected current.

2.2.2 SPECTRAL CHARACTERISTICS

A LED device operates through spontaneous radiative emission, with the recombination of an electron-hole couple and transfer of the resulting energy to a phonon. The carriers distribution is described by the Fermi statistics, and at a temperature higher than zero they occupy a certain number of states with energy higher than the minimum. We know that

$$E_{kin} = \frac{p^2}{2m^*} \tag{2.49}$$

where

$$p = \frac{hk}{2\pi} \tag{2.50}$$

Therefore, if the valence and conduction bands have a parabolic shape, the carriers energies are

$$E = E_C + \frac{(\hbar k)^2}{2m_e^*} \tag{2.51}$$

for the electrons, and

$$E = E_C - \frac{(\hbar k)^2}{2m_h^*} \tag{2.52}$$

for the holes ($m_e^*$and $m_h^*$are the effective masses).

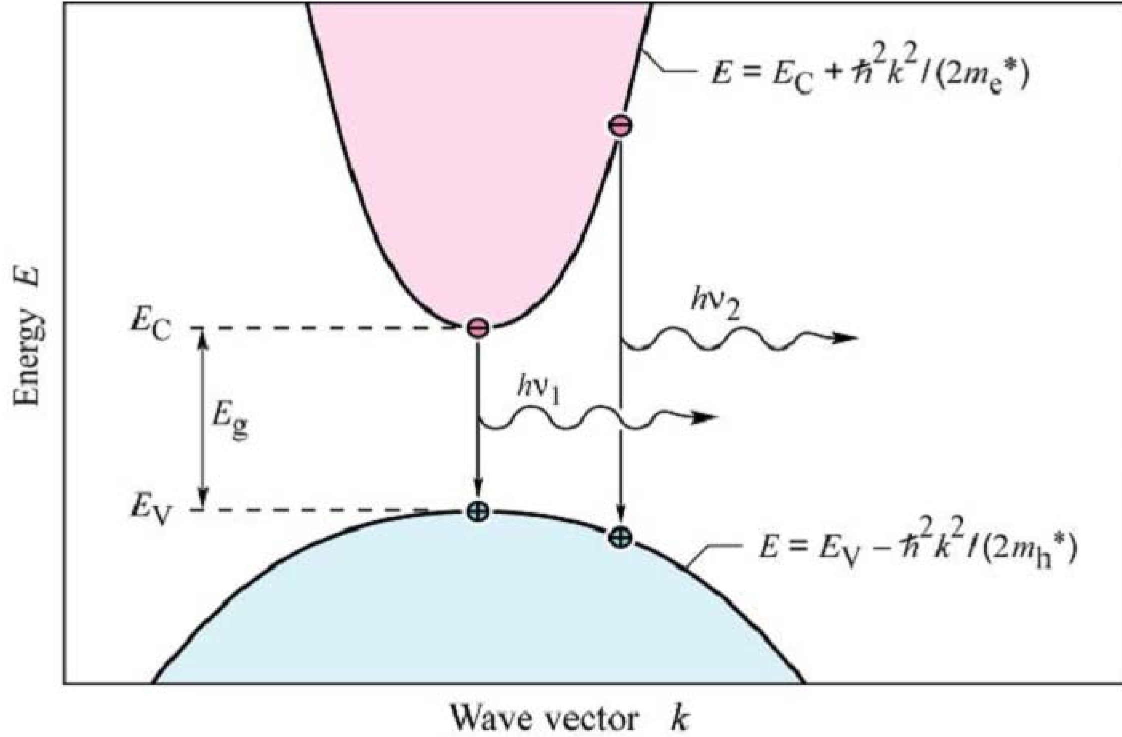


Figure 2.14: *Parabolic electron and hole dispersion relations showing "vertical" electron-hole recombination and photon emission.*

In the emission process both energy and momentum must be preserved. The momentum of the electron is given by

$$p = m \times v = \sqrt{2m * kT} \tag{2.53}$$

and the photon momentum by

$$p = (h/2\pi)\, k = h\nu/c = E_g/c \tag{2.54}$$

In order to have momentum conservation only "vertical" transitions can occur, and the condition on the conservation of energy, allows us to write

$$h\nu = E_C + \frac{(h/2\pi)^2 k^2}{2m_e^*} - E_V + \frac{(h/2\pi)^2 k^2}{2m_h^*} = E_g + \frac{(h/2\pi)^2 k^2}{2m_r^*} \tag{2.55}$$

where we have used the *"reduced mass"* m_r^*, defined as

$$\frac{1}{m_r^*} = \frac{1}{m_e^*} + \frac{1}{m_h^*} \tag{2.56}$$

The density of states has a parabolic dependence on energy, as we can see in the following equation

$$density\ of\ states = \frac{1}{2\pi}\left(\frac{2m_r^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E-E_g} \tag{2.57}$$

and the carriers in the bands obey Boltzmann distribution

$$f_B\left(E\right) = e^{-E/kT} \tag{2.58}$$

we can therefore deduce that the emitted radiation intensity (as a function of energy) is proportional to the product of the former two equations.

$$I\left(E\right) \propto \sqrt{E-E_g}e^{-E/kT} \tag{2.59}$$

Exploiting this relation we can deduce the LED's theoretical emission spectrum, the *I*-*E* curve

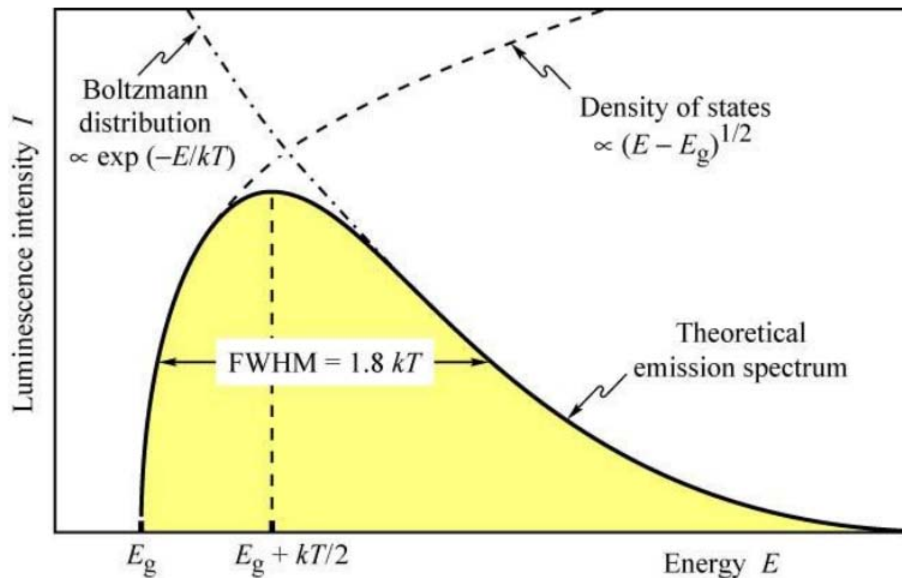


Figure 2.15: *LED's theoretical emission spectrum*

(luminescence intensity as a function of energy) and observe that the emission peak does not correspond to E_g,instead it is set at $E_g + kT/2$. Therefore we can also see that the width at half maximum of the emission spectrum as

$$FWHM = 1.8kT \tag{2.60}$$

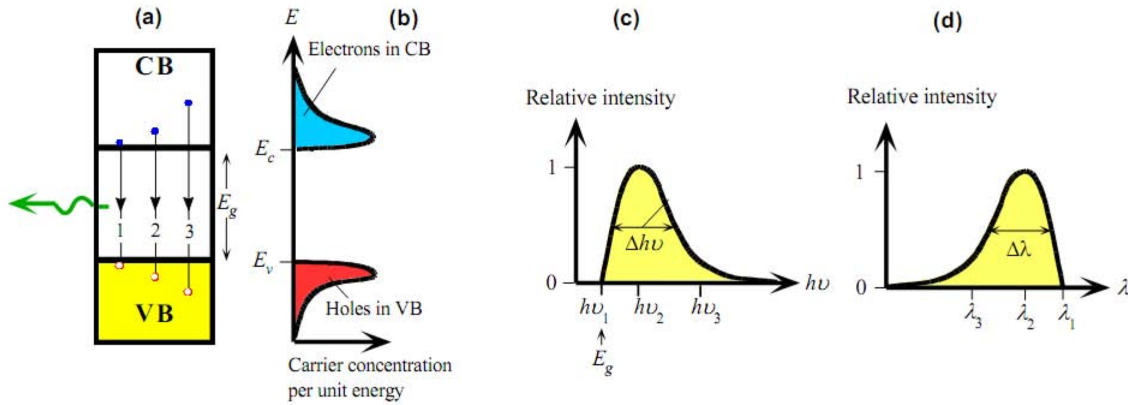


Figure 2.16: *(a) Energy band diagram with recombination paths. (b) Energy distribution of electrons in the conduction band and holes in the valence band. The highest electron concentration is* $\left(\frac{1}{2}\right) k_B T$ *above* E_C*. (c) The relative light intensity as a function of photon energy based on (b). (d) Relative intensity as a function of wavelength in the output spectrum based on (b) and (c).*

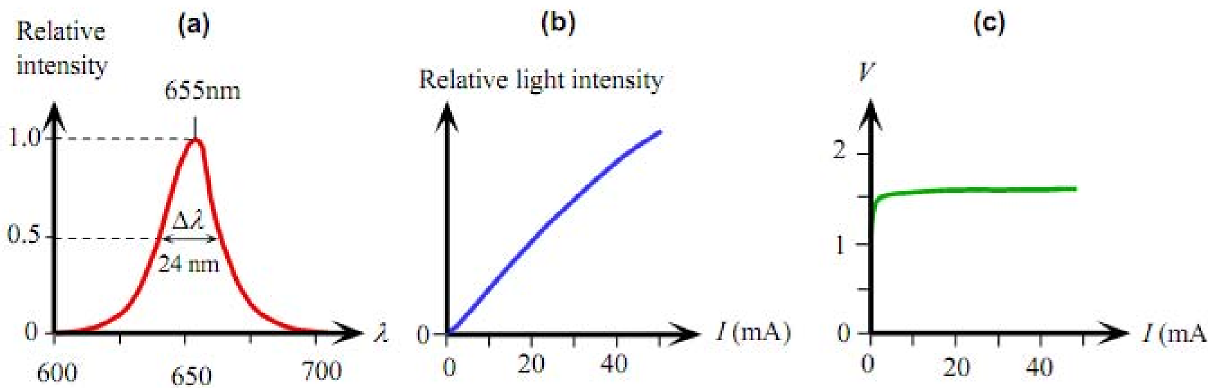


Figure 2.17: *(a)Typical output spectrum (relative intensity vs. wavelength) from a red GaAsP LED. (b)Typical output light power vs. forward current. (c) Typical I-V characteristics of a red LED. The turn-on voltage is around 1.5V.*

The width of the LED spectrum is of about $30 - 40nm$, and if we consider human vision it is short enough to make us see it as a single colour. nevertheless it is long enough to influence the practical applications of the device, for example in transmission through optical fiber. In fact in this medium, radiations with different wavelength travel at different velocities and scattering limits the bit-rate distance product. A LED spectrum characteristics can vary for different reasons, for example in high injection conditions it broadens, but the main parameter that influences it, is temperature. In fact an increase in temperature makes Shockley-Read-Hall non-radiative recombination and surface recombination higher, and also the number of carriers that can escape the well increases, therefore emission intensity decreases.

$$I = I_{|300K} \exp\left(-\frac{T - 300K}{T_1}\right) \tag{2.61}$$

Another important effect of temperature is the decrease of the energy gap, consequently, with

an increase in temperature, the LED spectrum peak shifts to lower energies, and its intensity decreases. Finally, as we already saw in Eq. (2.60), at higher temperatures the width at half maximum increases.

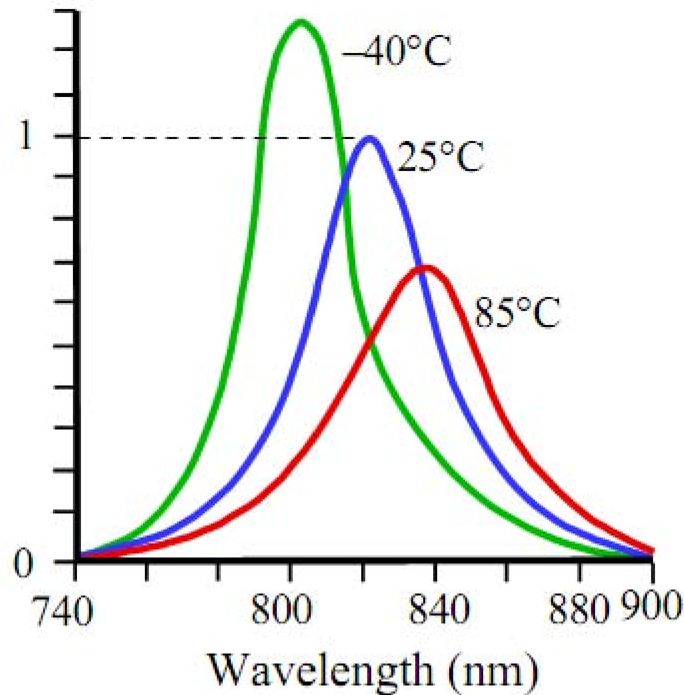


Figure 2.18: *The output spectrum from AlGaAs LED.Values normalized to peak emission at 25°C.*

2.2.3 LIGHT EXTRACTION AND GENERAL EFFICIENCY IMPROVEMENT TECHNIQUES

Light generated inside a semiconductor cannot escape from the semiconductor if it is totally internally reflected at the semiconductor-air interface. If the angle of incidence of the a light ray is close to normal incidence, light can escape from the semiconductor. However, when the angle of incidence is higher tan the so called *critical angle*, we have total internal reflection that reduces the external efficiency significantly. This parameter is determined by the ratio between the refractive indices at the air-semiconductor surface, and, assuming that the angle of incidence in the semiconductor at the semiconductor-air interface is given by ϕ, we can evaluate the critical angle exploiting the *Snell law.*

$$n_s \sin\varphi = n_{air} \sin\phi \tag{2.62}$$

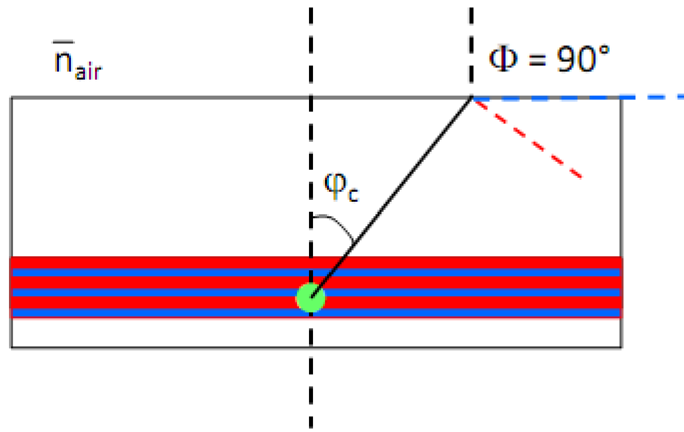


Figure 2.19: *Critical angle*

$$\sin\varphi_c = \frac{n_{air}}{n_s} \approx \varphi_c \tag{2.63}$$

This approximation is valid because refractive index of semiconductors is usually high.

The angle of total internal reflection defines a light escape cone. Light emitted into this cone can escape from the semiconductor, whereas light emitted outside the cone is subject to total internal reflection.

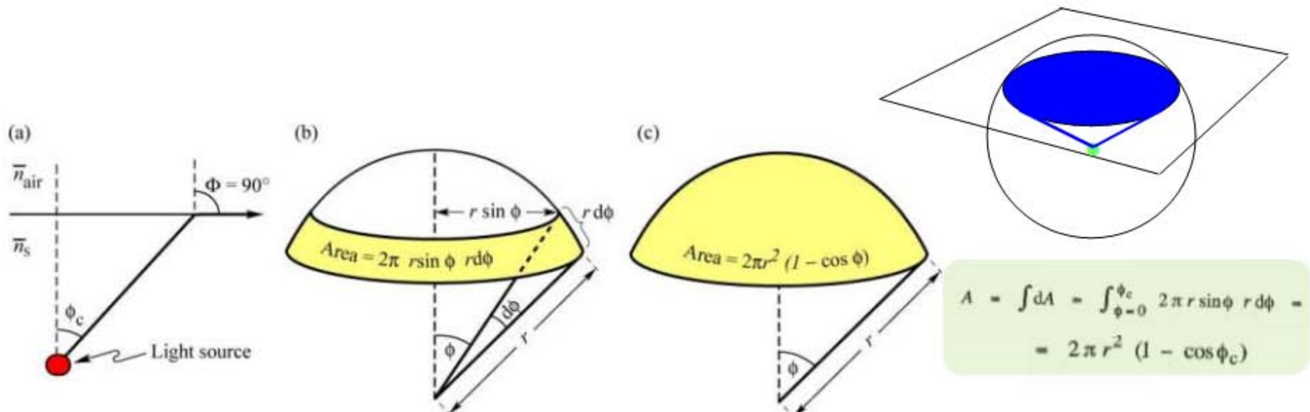


Figure 2.20: *(a) Definition of the escape cone by the critical angle ϕ_C. (b) Area element dA. (c) Area of calotte-shaped section of the sphere defined by radius r and angle ϕ_C.*

To determine the total fraction of light that is emitted into the light escape cone, we calculate the surface area of the calotte.shaped surface shown in Fig. (2.20) (b) and (c).

$$A = \int dA = \int_{\phi=0}^{\phi_C} 2\pi r \sin\phi \, r d\phi = 2\pi r^2 \left(1 - \cos\phi_C\right) \tag{2.64}$$

Let us assume that light is emitted from a point.like source in the semiconductor with a total

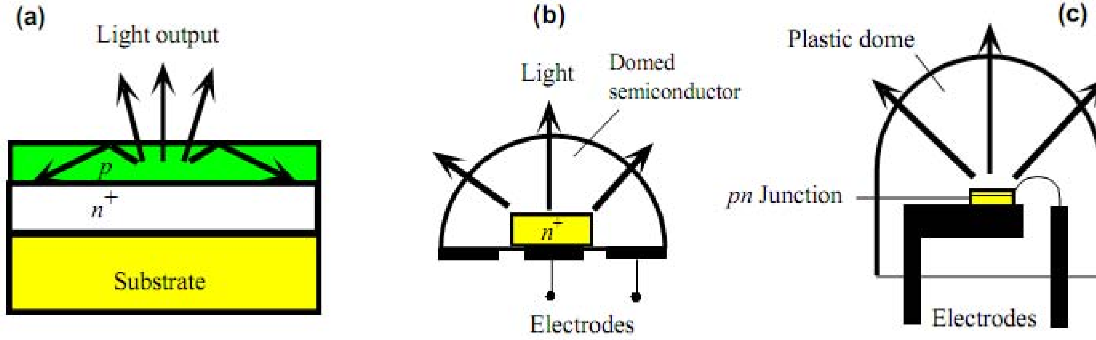


Figure 2.21: *(a) Reflection of part of the light generated in a flat LED. (b) Dome shaped semiconductor to improve extraction. (c) LED encapsulated in a plastic dome.*

power of P_{source}.Then the power that can escape from the semiconductor is given by

$$P_{escape} = P_{source} \frac{2\pi r^2 (1 - \cos\phi_C)}{4\pi r^2} \tag{2.65}$$

where $4\pi r^2$ is the entire surface area of the sphere with radius r. The calculation indicates that only a fraction of the light emitted inside a semiconductor can escape from it. This fraction is given by

$$\frac{P_{escape}}{P_{source}} = \frac{1}{2}(1 - \cos\phi_C) \tag{2.66}$$

Because the critical angle of total internal reflection for high-index materials is relatively small, the cosine term can be expanded into a power series. Neglecting higher-than second order terms yields

$$\frac{P_{escape}}{P_{source}} = \frac{1}{2}\left[1 - \left(1 - \frac{\phi_C^2}{2}\right)\right] = \frac{1}{4}\phi_C^2 \approx \frac{1}{4}\frac{n_{air}^2}{n_s} \tag{2.67}$$

The escape phenomenon is a significant problem for high-efficiency LEDs. In most semiconductors, the refractive index is quite high (> 2.5) and thus only a few percent of the light generated in the semiconductor can escape from a planar LED. To improve the extraction efficiency a number of different solutions have been developed, in particular different shapes of the LED have been introduced. In fact, an economic method to allow more light to escape from the LED is to encapsulate it in a transparent plastic dome, otherwise the semiconductor itself can be shaped into a dome, in both cases a reduction of the angles of incidence at the semiconductor-air interface is obtained, reducing internal reflection. The materials used for the encapsulating dome vary basing on the refractive index of the specific semiconductor used for the LED, and some examples can be seen in Fig. (2.22). The dome shape is not the only one that can be employed, in fact LEDs can also be shaped in a different way like, for example, in a truncated pyramid way, as in the example of Fig. (2.23).

Another way to improve extraction efficiency is the usage of thin-films. Thin film technology in fact, allows to prevent absorption in the substrate, both because the small thickness of the

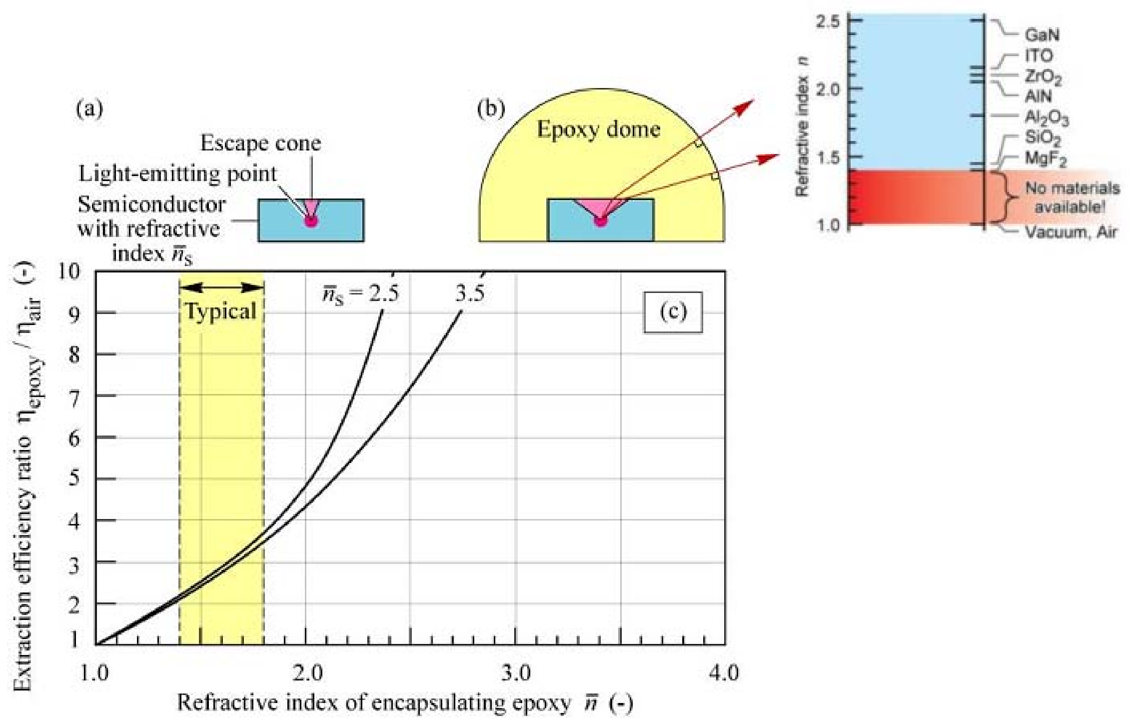


Figure 2.22: *(a) LED without and (b) with dome-shaped epoxy encapsulant. A larger escape angle is obtained for the LED with an epoxy dome. (c) Calculated ratio of light extraction efficiency emitted through the top surface of a planar LED with and without an epoxy dome. The refractive indices of typical epoxies range between 1.4 and 1.8.*

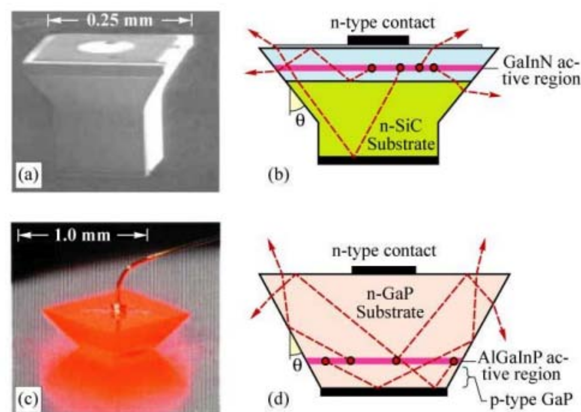


Figure 2.23: *Die-shaped devices: (a) Blue GaInN emitter on SiC substrate with trade name "Aton". (b) Schematic ray traces illustrating enhanced light extraction. (c) Micro-graph of truncated inverted pyramid (TIP) AlGaInP/GaP LED. (d) Schematic diagram illustrating enhanced extraction.*

materials layers and the usage of highly reflecting mirrors, and allows also to prevent waveguiding through the optimization of the surface roughness. With thin film structures, like the one shown in Fig. (2.24), extraction efficiencies in the order of 75% have been reached.

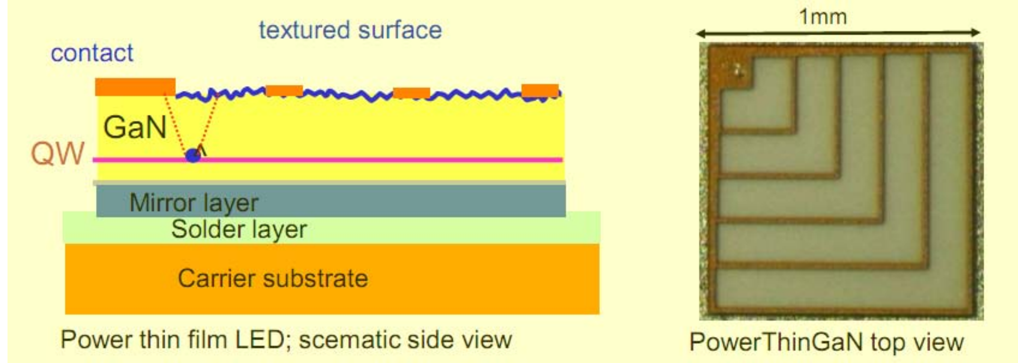


Figure 2.24: *Example of power thin film LED structure.*

Internal reflection is not the only problem that limits the device efficiency, thus other techniques to improve LEDs performance have been developed. An example is the usage of current spreading layers to improve the chip usage, as shown in Fig. (2.25).

2.2.4 L-I CHARACTERISTIC

Under steady-state conditions, the rate equation for a LED device can be expressed as

$$\frac{dn}{dt} = \frac{J}{qd} - (Bnp + AN_T n) = 0 \tag{2.68}$$

where J is the current density through the active region, d is the active layer thickness, B is the bimolecular recombination coefficient, A is the non-radiative recombination coefficient, N_T is the density of the defects responsible for non-radiative recombination, and n and p are the concentrations of electrons and holes in the active layer, respectively.

Under high injection conditions, one can write

$$n \approx p \gg N_a\,,\, N_d \Rightarrow Bn^2 + AN_T n - \frac{J}{qd} = 0 \tag{2.69}$$

If radiative recombination dominates over non-radiative processes

$$AN_T n \ll Bn^2 \Rightarrow L = Bn^2 \approx \frac{J}{qd} \tag{2.70}$$

On the other hand, if the non-radiative recombination processes dominate

$$AN_T n \gg Bn^2 \Rightarrow AN_T n = \frac{J}{qd} \tag{2.71}$$

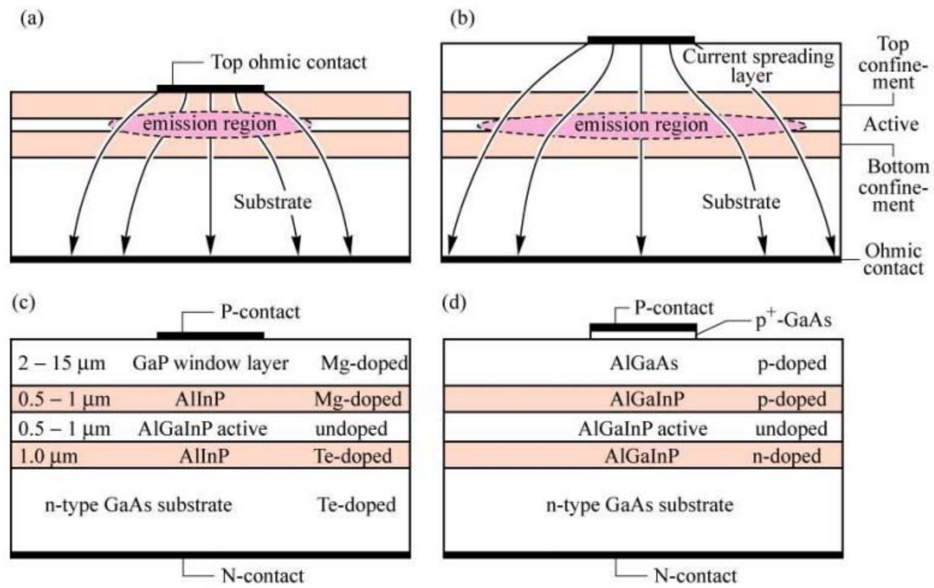


Figure 2.25: *Current spreading structures in high-brightness AlGaInP LEDs. Illustration of the effect of a current-spreading layer for LEDs (a) without and (b) with a spreading layer on the light extraction efficiency. (c) GaP current-spreading structure.*

which means that$n$ is proportional to the injected current, and therefore, light intensity (Bn^2) is proportional to the square of the injected current.

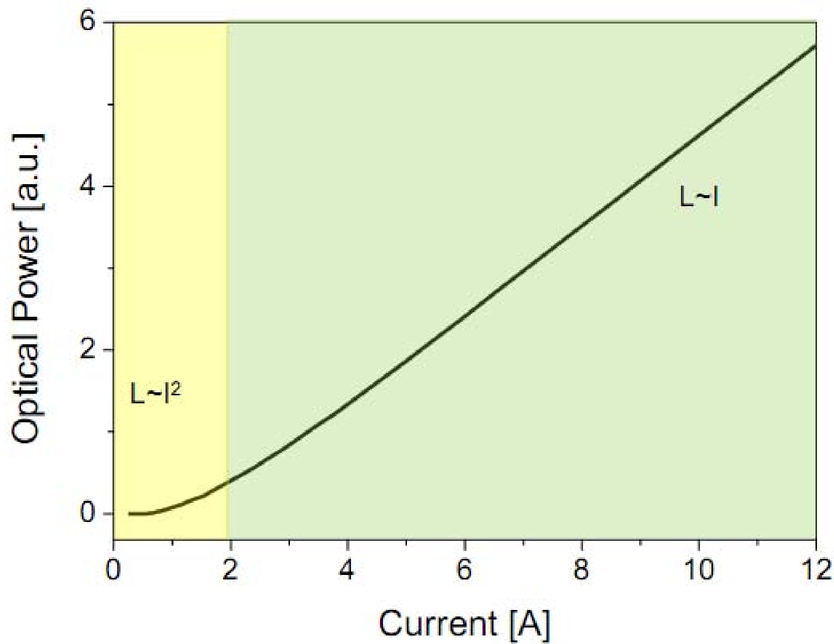


Figure 2.26: *L-I characteristic of a generical LED.*

Chapter 3

ELECTROSTATIC DISCHARGE

Consider two charged objects near each other, if some particular conditions are met, there can be a sudden and fast flow of charged particles from one to the other, this phenomenon is what we call an electrostatic discharge (or ESD). An ESD event can give rise to a current with very limited duration, between a few tens and a hundred nanoseconds, but with an intensity that can easily reach values in the order of 10 Amperes and with a rate of change of current $\frac{dI}{dt}$ that can be as high as 10 $\frac{A}{ns}$. This current can be an important problem for electronic components and devices, not only as a source of noise, but also causing permanent damage that originates unexpected destruction anywhere from fabrication to field, in fact it is estimated that 25% of all component failure are due to electrostatic discharge phenomena. These considerations show that, in addition to designing specific electronic structures to provide adequate ESD protection, it is fundamental to understand the causes that originate these electrostatic discharge events in order to limit them.

3.1 ESD GENERATION MECHANISMS

To understand the causes of the ESD phenomenon, it is useful to first consider a simplified model.

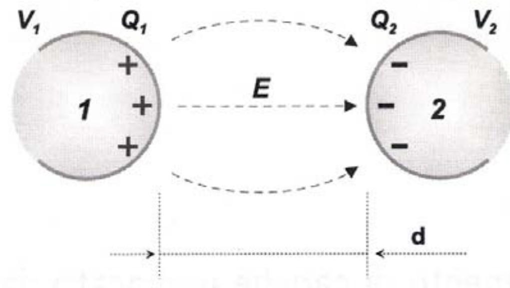


Figure 3.1: *Two charged bodies at a distance d from each other.*

In the previous image we can see two conductive objects at a distance d one from each other. On the two surfaces there is an accumulation of charge (positive on the first one, negative on

the other) that generates an electric field E in the surrounding space. The intensity of this field depends on many factors, such as the quantity of charge stored on the two facing surfaces, the distance d and the shape and characteristics of the two surfaces (especially their roughness). This field generates a force that acts on the atoms, free electrons and ions in the medium (air or another dielectric material) between the two objects, generating a current that in most of the cases, if the intensity of E is low, is negligible.

If the quantity of charge on the surfaces increases, or the distance d decreases, the intensity of E becomes higher and the induced force can be strong enough to both break the bonds between electrons and nucleus in the atoms of the medium, and free the electrons stored on the surface, increasing the number of free charged particles in the space between the surfaces and thus the current. High values of E can also lead to impact generation of electron-ion couples because of the increased kinetic energy of the free charged particles. This phenomenon can generate high quantities of free charged moving particles and therefore a high current, known as avalanche discharge or electrostatic discharge; if this happens, the dielectric loses its electrical insulator properties and becomes temporary conductive. The transition from isolation to conduction requires the breakdown of the insulator or, if the breakdown condition is not fulfilled during the approach of the objects, the final direct contact between them. Finally, a plasma channel of ionized gas develops to a low resistance, and the formation of this resistive phase is accompanied by a visible and audible spark. We can assume that the insulator breakdown takes place when the intensity of the electric field in the space between the objects becomes higher than the dielectric strength of the medium, that in the case of air is about $30\frac{kV}{cm}$.

After a conductive stage has been reached employing the locally available mobile charge, the amplitude and waveform of the discharge current are strongly influenced by the time and current-dependent resistance of the plasma channel, the external resistance, the capacitance, and the inductance of the discharge circuit. The current intensity of these ESDs can easily reach some tens of Amperes, with rise times of less than $1ns$, and the charge redistribution causes the electric field to decrease rapidly. In order for the electric arc to last two conditions must be satisfied: the voltage difference between the two object must be higher than a minimum value of about $10\ V$, and the discharge current has to be higher than a minimum value too. If one of these conditions is not met, charges automatically stop flowing.

It is worth to say that it can also happen that two charged objects get in touch before the conditions for the arc generation are met, we identify this situation as “direct contact ESD”. In this case, that often happens in practice, there is a real low-impedance conductive path through which charges can move from one object to the other, and the current generated can reach higher values than in the the case in which there is an arc generation;even rise times are shorter. In any case, when an ESD occurs there’s a high current flowing that can permanently damage electronic devices

3.1.1 LOCAL CHARGE GENERATION MECHANISMS

We have see that to have en ESD, we must have a difference in the electrostatic voltage of two (or more) objects. The four basic mechanisms that cause charge accumulation thus generating electrostatic voltages, are *triboelectric charging*, *ionic charging*, *direct charging*, and *field-induced charging*.

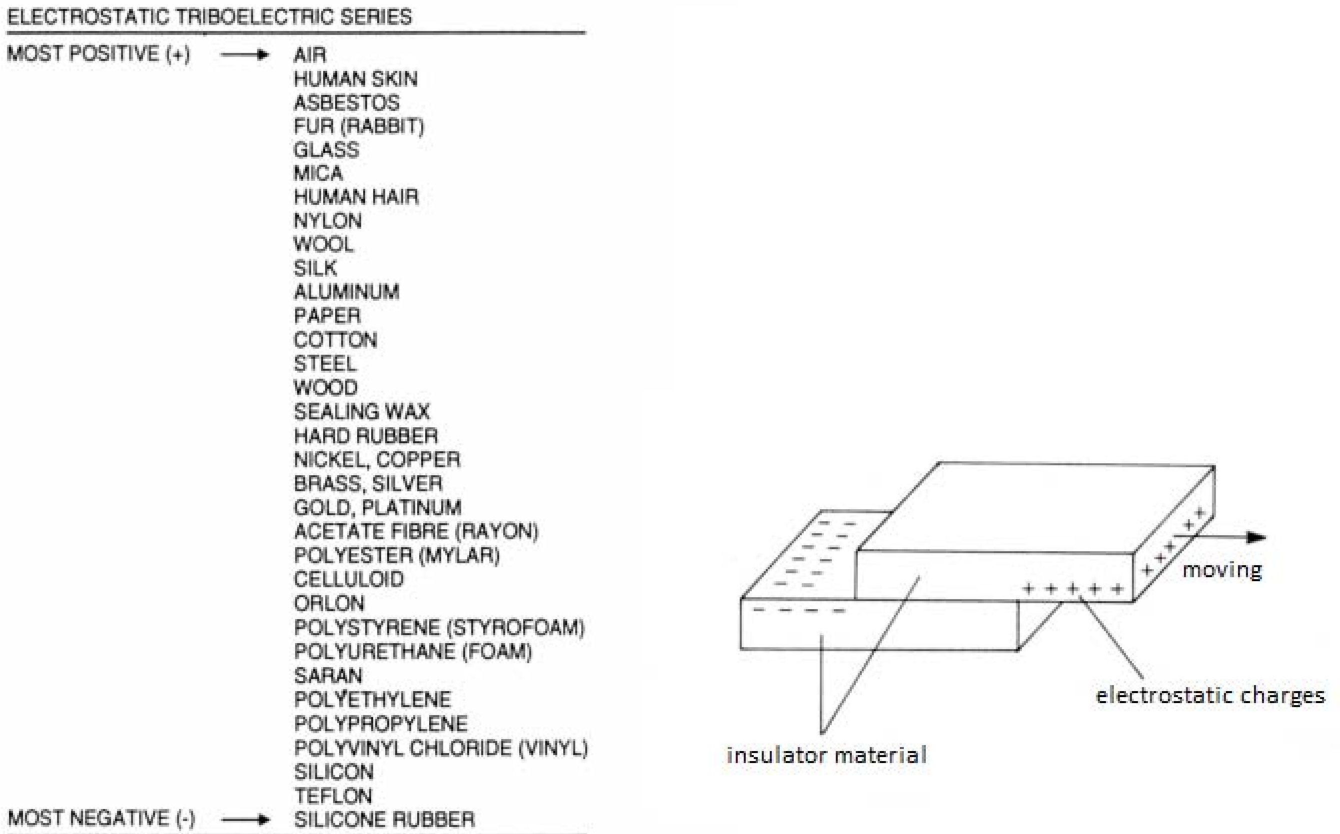


Figure 3.2: *Electrostatic triboelectric series*

Triboelectric charging results from the mechanical contact and separation of two surfaces with different electron affinity. The object with the higher affinity acquires the electron. After separation it will remain negatively charged with respect to the object that has lost the electron. If the charges cannot immediately recombine, consecutive cases of contact and separation increase the amount of charge, and that builds up a higher voltage. It is very important to notice that no friction or rubbing is necessary to generate and separate charge. The faster the separation of the objects carrying the charges occurs, the less the chance to recombine.

This slow process can be influenced by many parameters, in fact humidity, temperature, any contamination of the surface and the roughness and pressure of the surface contact have a significant influence. Humidity, in particular, increases the surface conductivity, raising the recombination rate. In general, highly insulating hydrophobic materials such as PTFE, better known as Teflon™ or silicone rubber, are the most susceptible to charging and can carry the charge for nearly an infinite time. In real-world situations, tribocharging occurs, for example, when walking or rising from a chair. It can charge moving parts of machines as well as IC packages. It also results from spray cleaning, for example, with pressurized high-resistive deionized water or from blasting with carbon dioxide pellets. Without proper grounding, for example, with wrist straps or controlled conductivity, tribocharging can generate electrostatic voltages of up to some 10 kV on persons. Voltages on parts of machines, ICs, and modules are usually lower. Corona discharges or residual conductivity may also limit the voltage.

The second charging mechanism, the *Ionic charging*, is associated with the use of air ionizers,

that are fundamental for the neutralization of immobile charge on insulating surfaces. It occurs only if the flow of ionized gas molecules is not properly balanced or adjusted to the charging properties of the individual manufacturing process step. The resulting voltage can easily exceed some hundreds of volts. Anyway this is a quite slow process, similarly to the one described previously, the triboelectric charging.

Direct charging occurs if mobile charge is directly transferred from a charged object. The amplitude and duration of the current pulse depend on the voltage difference, the capacitance of the "victim" or voltage source with respect to the environment, and the impedance of the charge path. It may be associated with the insertion of a device into a test socket.

Finally *field-induced charging*, the last process to be described, is closely related to direct charging. In this case, a neutral object is brought slowly into an external electrostatic field, or the electrostatic field increases. This external field causes the separation of mobile charge on the conductive parts of the object and, as soon as this still neutral body comes in contact with another conductive object, at a different voltage, a very narrow, very high current pulse charges it. After this first stress, the object is charged and can consequently give rise to another electrostatic discharge involving other bodies, characterized by an opposite polarity of the current flow with respect to the first stress.

Of all this mechanisms the most important is doubtless tribocharging. In most of the cases this is in fact the root cause for the generation of the external electrostatic field that causes ESD events.

3.2 ESD STRESS MODELS

We now consider specifically ESD events in an IC environment, because in this field devices are very sensitive to these phenomena and also because the subject of this thesis work is the robustness of LED modules. The first step is analyzing the ESD stress models.

The types of ESD-phenomena occurring in an IC environment that are distinguished and simplified into stress models are mainly two. The first assumes a charged person approaching a grounded IC. When the air breaks down between the finger and one pin of the IC, the capacitance of the person is discharged via the IC into ground. This model is called *Human Body Model, HBM.*

On the other hand the ESD-mechanisms in manufacturing and automatic handling are typically associated with a charged piece of equipment, a charged IC-package or the charged conductive parts of the IC itself. This type of phenomenon leads to two different models, a *charged device model, CDM,* and a *Field- Induced Charged Device Model, FCDM*, that differ in the charge-up method. In both of them in the worst case, the discharge is determined by the capacitance of the device, the inductance of the pin, and the resistance of the ionized channel, resulting in an extremely narrow pulse with a high peak current even for voltages around 1 kV.

These two models have for example been employed by Enoch and Lin in the investigation of the effects of the field-induced charging and discharging through devices soldered on printed circuit boards ([1] and [2]); it should be noted that FIM has been introduced by Unger for the damage of unprotected MOS-transistors caused by the presence of an electrostatic field without any

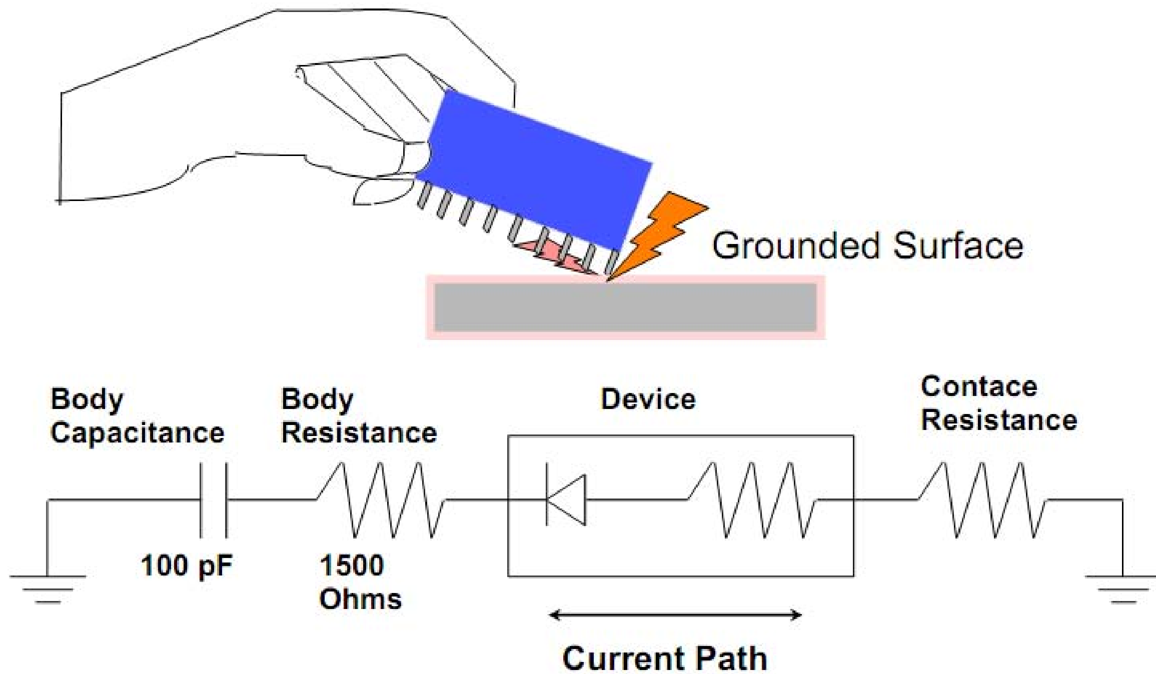


Figure 3.3: *When a charged person touches an IC pin the body charge is discharged through the device to ground. This rapid discharge causes damage and IC failure.*

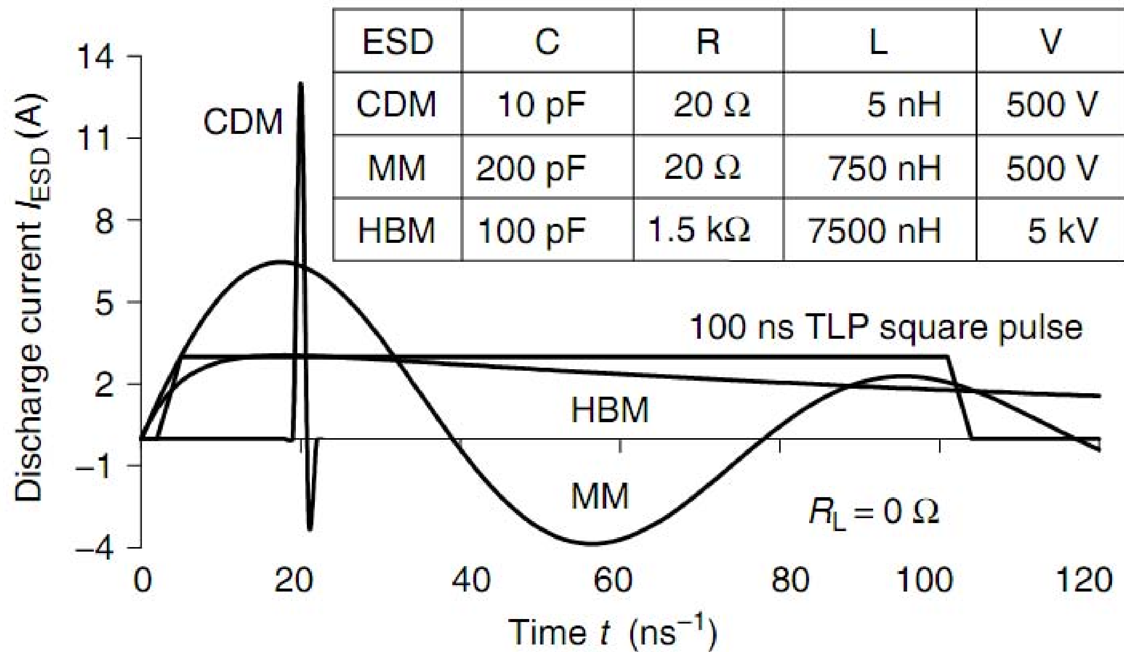
discharge event. In comparison with CDM of single ICs, the capacitance of the charged board as well as the inductances of the metal traces are significantly larger and the discharge circuit is even more complex. One important finding of Lin was that even short circuits temporarily attached to the edge connector of the board could not fully protect sensitive devices against the very fast, high-current discharges.

For the ideal stress models HBM, MM, and CDM with an assumed RLC circuit, the discharge current can be easily calculated from the solution of the second order differential equation.

$$\frac{d^2 i\,(t)}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{1}{LC} i = 0 \tag{3.1}$$

If the oscillation frequency $\omega = \frac{1}{\sqrt{LC}}$ exceeds the damping coefficient $\alpha = \frac{R}{2L}$, including the load resistance, the discharge is an oscillation as observed for the MM with low resistive loads. Otherwise it is aperiodically damped, like in the HBM case. The CDM discharge waveform varies.

Obviously not all of the practical cases can be related to just one specific model. For example, the situation in which a charged person is putting a device onto a low resistive tabletop, is something in between the HBM and CDM model. The pulse that originates in this case can in fact be considered as a combination of a fast high-current CDM impulse followed by an HBM discharge. Another case of interest not described by the previous models is the one of a charged person discharging its capacitance via a metallic tool into a grounded object or an object with a large capacitance to ground. This situation results in a initial narrow peak rising in less than 1 ns that discharges the local capacitance of the tool, followed by a longer period in which the person



ESD	C	R	L	V
CDM	10 pF	20 Ω	5 nH	500 V
MM	200 pF	20 Ω	750 nH	500 V
HBM	100 pF	1.5 kΩ	7500 nH	5 kV

Figure 3.4: *RLC- Discharge current waveforms of three basic ESD stress models, HBM, MM and CDM for typical circuits in comparison with a TLP square pulse.*

is discharged and is described by the so-called System Level HBM, a more severe two-terminals stress model, typically employing a main capacitor of 150 pF and a resistor of 330Ω.

Furthermore, all of the models that will be shown in detail in the following, describe a discharge through or into a device that is not powered, while other ESD stress cases could consider ICs in a module or system that may even be connected to the power supply. In fact, in some cases ESD effects may be worse if the device is powered, like in the case of discharges applied to CMOS-IC connected to the supply, in which there may even be a latch-up phenomenon called *Transient Latch-Up (TLU)*. Thus it is important to remember that the models that will be considered do not describe every possible practical case, nevertheless they are the ones currently employed in most of the cases for the study of ESDs and for the development and testing of experimental and commercial devices.

3.3 ESD STRESS METHODS

Manufacturers and users of ICs have derived the ESD test methods from the basic ESD stress models: the Human Body Model (HBM) and the Charged Device Model (CDM). These procedures should reproduce the different failure signatures and give informations about the sensitivity levels towards the various types of discharges, allowing also a comparison with the electrostatic voltage levels measured in a fabrication process. Nevertheless there is a number of serious challenges that these models have cope with.

One of the main problems in the study of ESDs and development of ESD test methods, is the reproducibility of this phenomenon. In fact an important thing to notice is that the lumped

element approach to model the discharge circuit, is only valid if the geometric size is smaller than 20% of the shortest wavelength in the spectrum of the discharge pulse (and the harmonic content of these pulses can reach quite high frequencies); moreover the interdependencies of the circuit parameters are very complex and yet not fully understood for the ESD voltage domain. Another very important problem for the reproducibility is the the *statistical time lag* between the time the strength of the electrical field fulfills the requirement for breakdown and the time the electron actually starting the avalanche becomes available. The fact that the avalanche multiplication factor and thus the discharge current depend exponentially on the field strength, makes this time lag the major influence on the reproducibility of a discharge across a closing air-gap. In fact during this time the closing of the gap continues and the electrical field strength increases further. These problems make standardization and reproducibility of the results obtained with the same system, and the correlation between different ones, the main issues in the ESD testing process. Moreover things are made even worse by the fact that, while the basic stress models are simple lumped RLC circuits with ideal switches, their practical implementations have to deal with many additional parasitic elements. In particular the ultrashort, varying air discharges of CDM constitute a serious challenge to reproducibility. Another problem is that failure criteria strongly influence the failure thresholds. Furthermore high-pin count devices highlight the importance of reducing test time.

To accomplish all the goals described before and try to minimize the problems, all the ESD stress models must define the way devices have be tested. In particular, acknowledging that the responsible for the majority of ESD failure mechanisms is the discharge current that generates heat and voltage differences, they must specify the discharge current waveforms for a given precharge voltage. They will also define the measurement system characteristics and all the parameters that influence the results.

We are now going to describe the main stress models and procedures, starting from the HBM, the traditional ESD stress model (employed for example in the C.E. products qualification tests).

3.3.1 HUMAN BODY MODEL (HBM)

As previously said, the HBM model is an attempt to describe and reproduce ESD events that occur when a charged person touches a device (or gets near enough to it to cause an electrostatic discharge). It consequently defines the current waveform for the discharge of a$100pF$ capacitor (representing the body capacitance to the ground) through a $1.5k\Omega$ resistor (the body resistance) and a 0Ω load for different discharge voltages.

Some useful informations about this model are given in Fig. (3.4) and (3.5). In the first one we can see the typical HBM discharge waveform compared to the other models'. The parameters that characterize the stress system, whose typical values are also shown in Fig.(3.4), are C_{HBM} , that stores the charge, R_{HBM} that limits the current and L_{HBM}, which is the effective inductance of the discharge path in a real tester. This parameter is particularly important, in fact, together with R_{HBM}, it determines the rise time of the pulse, specified as between 2 ns and 10 ns from 10% to 90% of the amplitude I_{MAX}. Besides this, the HBM model also specifies that within the $150ns$ that follow the rising edge, the pulse amplitude has to decay to $\frac{1}{e*I_{max}}$. It is a slow pulse then (the frequency content of this almost ideal pulse is not higher than 350 MHz), with typical rise times in the order of $10\,ns$, fall times of about $100-300\,ns$ and a high energy content.

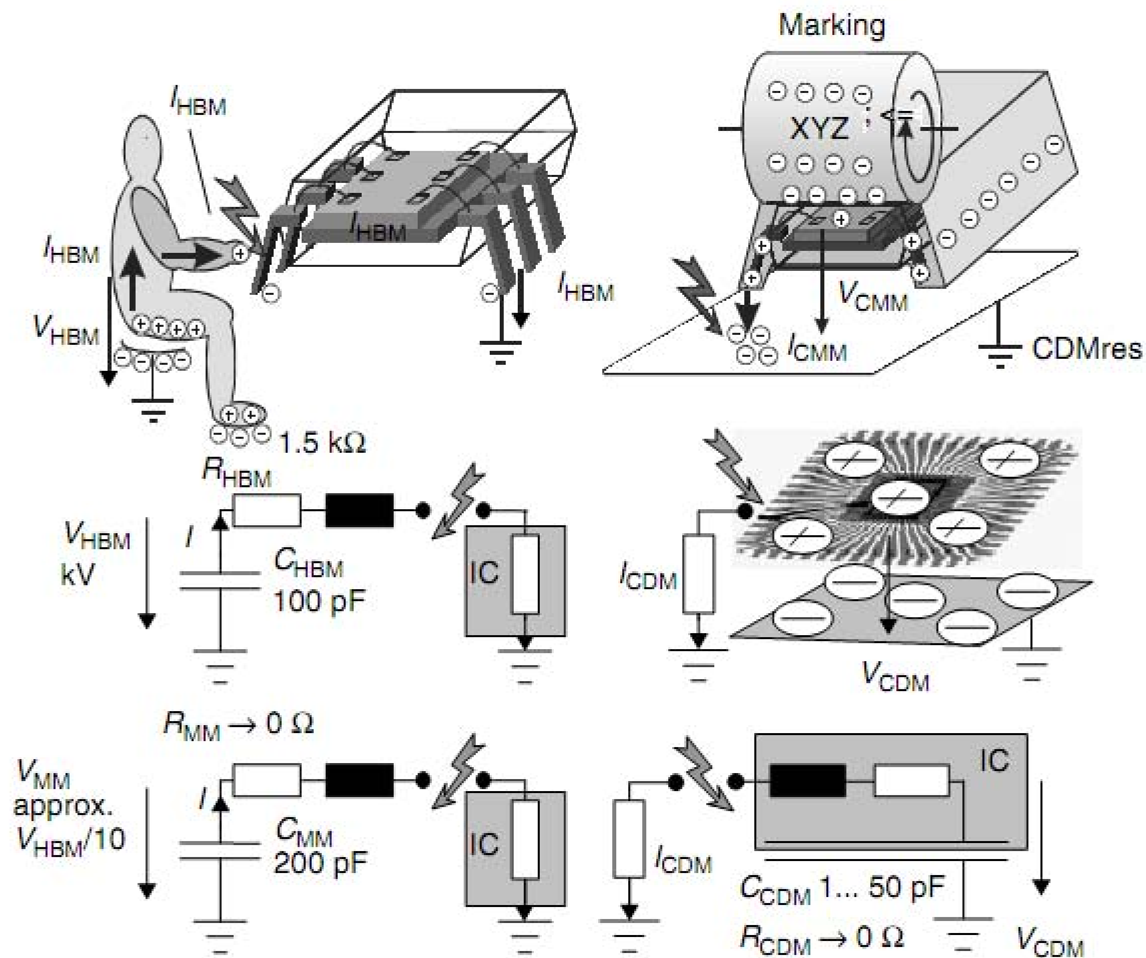


Figure 3.5: *ESD stress models HBM, MM, and (F)CDM with typical parameters.*

Stressing integrated circuits according to this standard has unveiled serious correlation issues, as shown in Fig (3.6).

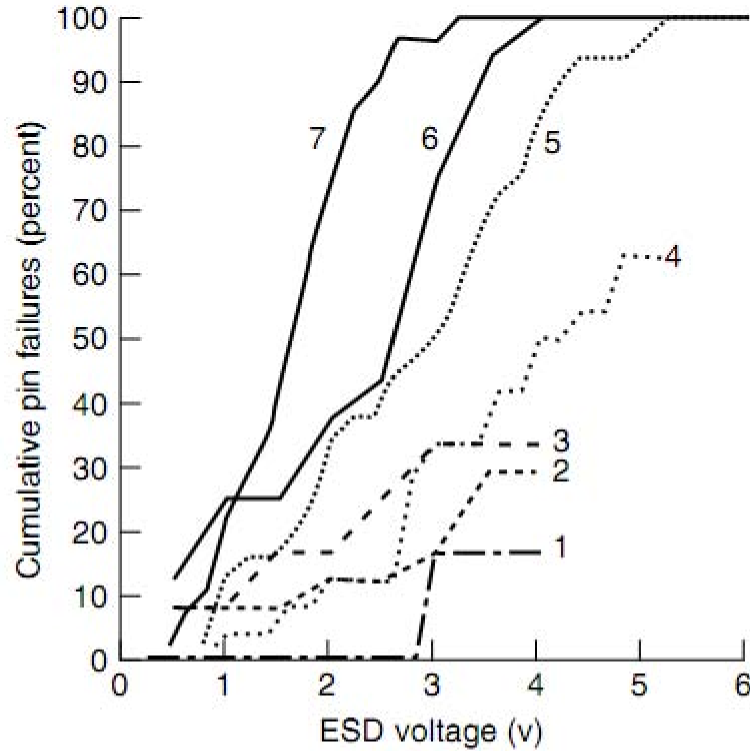


Figure 3.6: *Cumulative pin failures versus ESD voltage for the same product tested with different HBM testers (1 to 7).*

These differences were attributed to additional parasitic elements in real testers and to their effect on the discharge waveform, together with inadequate description of a real HBM-test system by the lumped element model shown in Fig (3.5). Measurement of the discharge current waveforms in the real test systems with a 500Ω resistor helped identify these additional parasitics, allowing to draw a more accurate model, shown in Fig. (3.7). In this scheme C_s is the parasitic stray capacitance of R_{HBM} and of the interconnections, C_t is the parasitic capacitance of the test board and $R_L$is the resistance of the load or device under test. The equivalent RLC circuit can be modeled numerically or even analytically up to the fourth order to obtain waveforms for different values of the elements.

Anyway, if all we need is just a simple description of the HBM current waveform, we can obtain it from a simplified solution for the differential equation of the RLC lumped elements circuit.

$$I_{HBM} = V_{HBM} C_{HBM} \frac{\omega_0^2}{\sqrt{a^2 - \omega_0^2}} e^{-\frac{R_{HBM}}{2L_{HBM}}} \sinh\left(\sqrt{a^2 - \omega_0^2}\right) t \tag{3.2}$$

with $a = \frac{R_{HBM}}{2L_{HBM}}$ and $\omega_0 = \frac{1}{\sqrt{L_{HBM} C_s}}$, and $a > \omega_0$. Exploiting this equation we can also estimate the rise time as

$$t_{rise} = \frac{2L_{HBM}}{R_{HBM}} \tag{3.3}$$

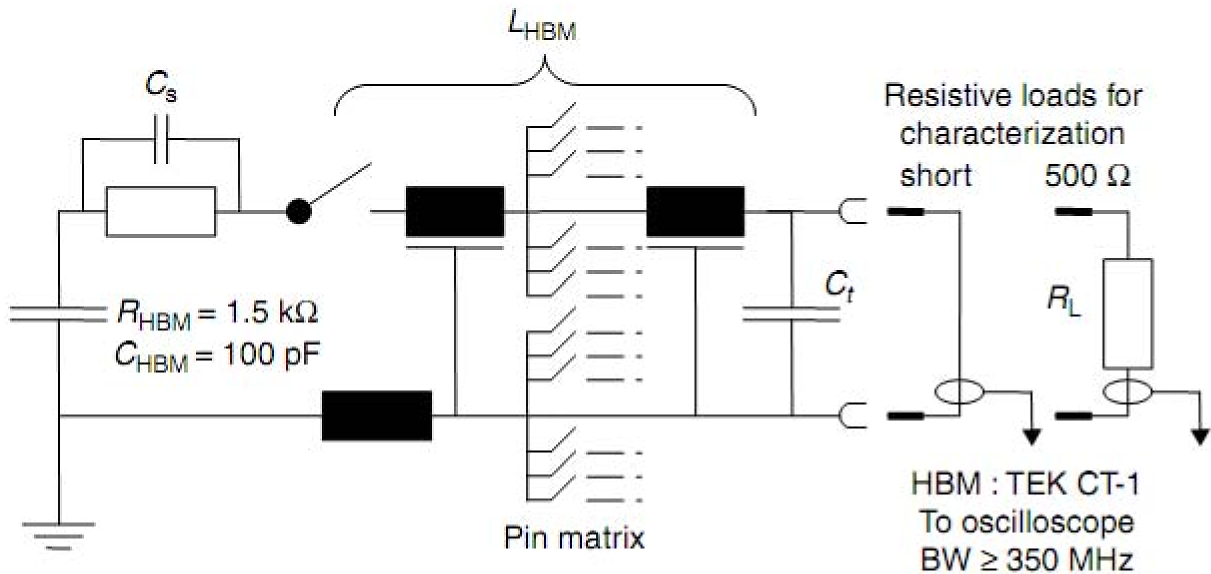


Figure 3.7: *Schematics of an HBM-tester with two resistive loads for the characterization of the waveform*

We can therefore see that to obtain a t_{rise} of 10ns, L_{HBM} is required to be about $7.5\,\mu H$.

3.3.1.1 TEST PROCEDURE

The general test procedure is defined by the ESD Association, JEDEC, and the AEC, which have their common origin in the MIL-STD 883 C method 3015. The procedure specifies the calibration of the tester, the number of samples to be tested, and the pin combinations to be tested. The standardized failure criterion is the data sheet specification. The HBM test procedure applies in principle to all stress test methods that stress one pin with respect to a single pin, other pins, or a group of pins. In principle, the real HBM discharge may occur between any combination of 2 pins. Therefore, the ideal coverage of sensitive combinations would be achieved stressing each pair individually. For devices with more than 64 pins this would be endless. The standard test methods had to select meaningful combinations that reflect the design of the protection scheme. Each pin is stressed with respect to one of the supply pins. All other pins are left floating. In a next step the standards require to stress the pin with all the other non-supply pins grounded. The effect is the same as a pin- to-pin test, but it provides a number of return paths for the stress current, which reduces the severity of the test compared to a direct pin-to-pin test. Pins such as offset adjust, compensation, clocks, control, address, data, V_{ref}, no connects (NC) are considered to be non-power supply pins. For example, a programming power pin, usually called V_{pp}, shall be considered to be a non-supply pin because it does not supply current to or interface with any other pins. For evaluation purposes of small circuits one should consider to stress all the pins against every other pin in turn. For higher pin counts a reasonable judgment must be made of which pins will provide the worst-case conditions under pin-to-pin testing in order to reduce testing time, These conditions will vary according to the type of silicon (n-substrate or p-substrate), the type of IC (e.g., nMOS, CMOS, bipolar), and the circuit design itself. As a rule of thumb, the pins furthest apart from each other (i.e., diagonally opposite) and the

pins adjacent to the stressed pin, would provide an indication of the worst-case performance. However, it may be necessary to check the layout of the IC and the bonding of the package to ensure that these are indeed the pins with the largest and smallest resistances to the stressed pin.

Regarding the number of devices to be submitted to the stress, three new components may be used at each voltage level or pin combination to avoid stress hardening or cumulative effects. The starting voltage is not specified and step stressing can begin from any value, however, different starting voltages may produce different results. In the case of on-wafer testing, investigating the distribution of the HBM failure thresholds of many devices across all the wafer, can give useful informations on process related ESD issues.

Testing specifications usually require circuits to have a minimum pass threshold voltage of ±2 kV HBM stress on all pins, as they can be handled in an ESD-protected environment with no significant loss due to HBM-type discharges. ESD pass voltages of ±1 kV HBM are still acceptable for more complex ICs. If we consider few RF pins or RF components that will be handled in well-protected environments, lower pass voltages are acceptable too. Increasing the ESD threshold beyond 4 kV does not give enough advantages to justify the additional cost. However, in some particular cases, like the ones of devices that have to be used in harsh environments, higher HBM-withstand voltages (above 10kV) may be required. This is for example the case of automotive applications or of the system-level HBM test.

3.3.2 MACHINE MODEL (MM)

The *machine model*, *MM*, originally developed in Japan as a severe HBM, is a low-impedance, high-current discharge, that oscillates if the load has a low value of impedance. The goal of this stress model is the simulation of abrupt discharge events caused by the contact of the device with equipment and/or empty sockets. The equivalent circuit is similar to the HBM-circuit of Fig. (3.7). The capacitance C_{MM} has a value of $200\,pF$, while R_{MM} is nominally 0Ω. In a real ESD tester, the resistance R_{MM} will be obviously higher 0. In comparison to the HBM, the machine model generates a very similar type of power-related failure in the pn-junctions, but the pre-charge voltages at which they take place are lower (that happens because they correspond to higher currents).

Also in this ESD-stress model the correlation between different testers is a serious issue. In fact, even if it has been improved with respect to its original characteristic by defining a discharge current waveform that implies an effective inductance of $0.75\,\mu H$ (previously it was 0.5 and $2.5\mu H$) and an effective resistance of 10Ω in the discharge path, it is still worse than in the HBM. In fact the parasitic elements of the MM-tester have a very strong influence on the discharge current waveform, in particular through an IC with its dynamically changing impedance.

The test procedures, pin combinations, and correlation issues are equivalent or worse in comparison with the HBM. Typically required withstand voltage levels are ±200V for regular devices and ±400V for higher requests. The package influence due to differences in the test boards may even be more significant as the influence of parasitics on the waveform is more significant in comparison with HBM, while the failure mechanisms with the MM are often very similar or identical with those observed with HBM.

3.3.3 CHARGED DEVICE MODEL (CDM)

The charged device model (CDM), simulates the ESD event occurring when an electrostaticallly charged device is abruptly discharged to a metallic ground, and either with direct or with field-induced charging, it is the most frequent discharge mechanism in an automated handling environment. For CDM with current pulses of fewns duration and with amplitudes of up to some tens of amperes (these are typical values for a CDM pulse), gate oxide failures due to IR drops in the metal and poly lines that may not be reproduced by HBM or MM are often seen. Another characteristic is that, unlike for the 1.5kΩ current source characteristic of HBM with a nearly ideal or at least appropriate capacitor, resistor, and relay, the CDM-discharge circuit depends strongly on the device and on several environmental conditions.

An important thing to notice about this model, is that different CDM testers exist. The schematic of the first CDM-test setup developed by Bossard and others is shown in Fig (3.8) . The device was lying in “Dead Bug” position on a ground plane to achieve a well-defined, large capacitance to ground and contacted with a charge relay and a discharge relay. Because of the relays, this mode is referred to as contact mode. The capacitance between the lead frame with the chip and the ground plane was charged via one pin and discharged via another pin. Typically, the pin with the best contact to the substrate was chosen as the charge pin.

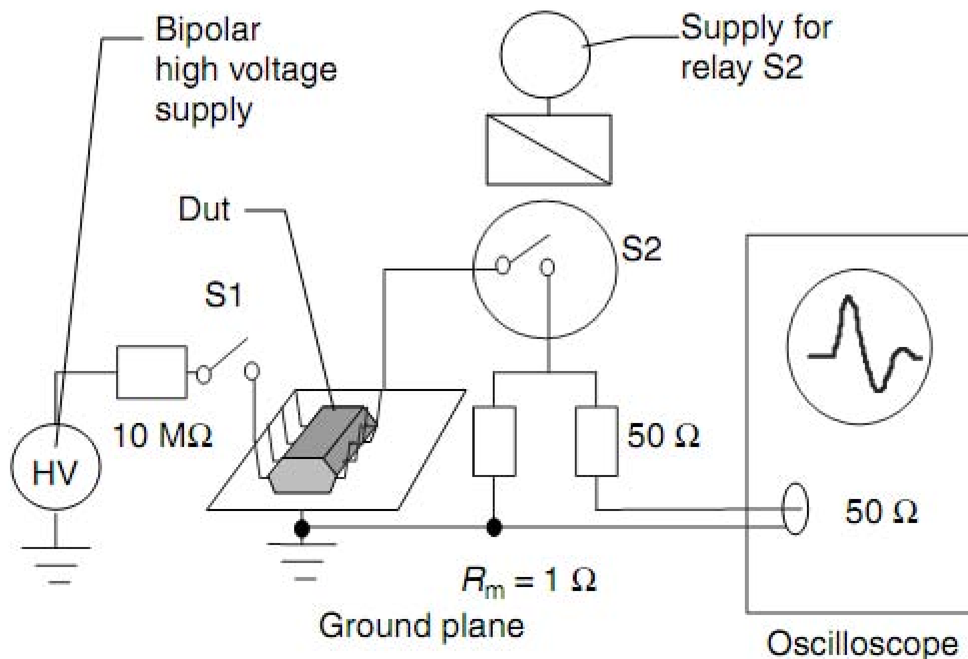


Figure 3.8: *First CDM-test system.*

The capacitance of the device to ground depends strongly on the package and on any air gap or other dielectric between the package and the ground plane. The actual voltage is determined by the resistance of the voltage source and the isolation resistance between the chip and the ground plane as well as by capacitive voltage suppression if the device is disconnected previous to discharge. The recovery of the potential due to charge retention of insulators may also have an influence. The inductance of the discharge path depends on the area that is surrounded by

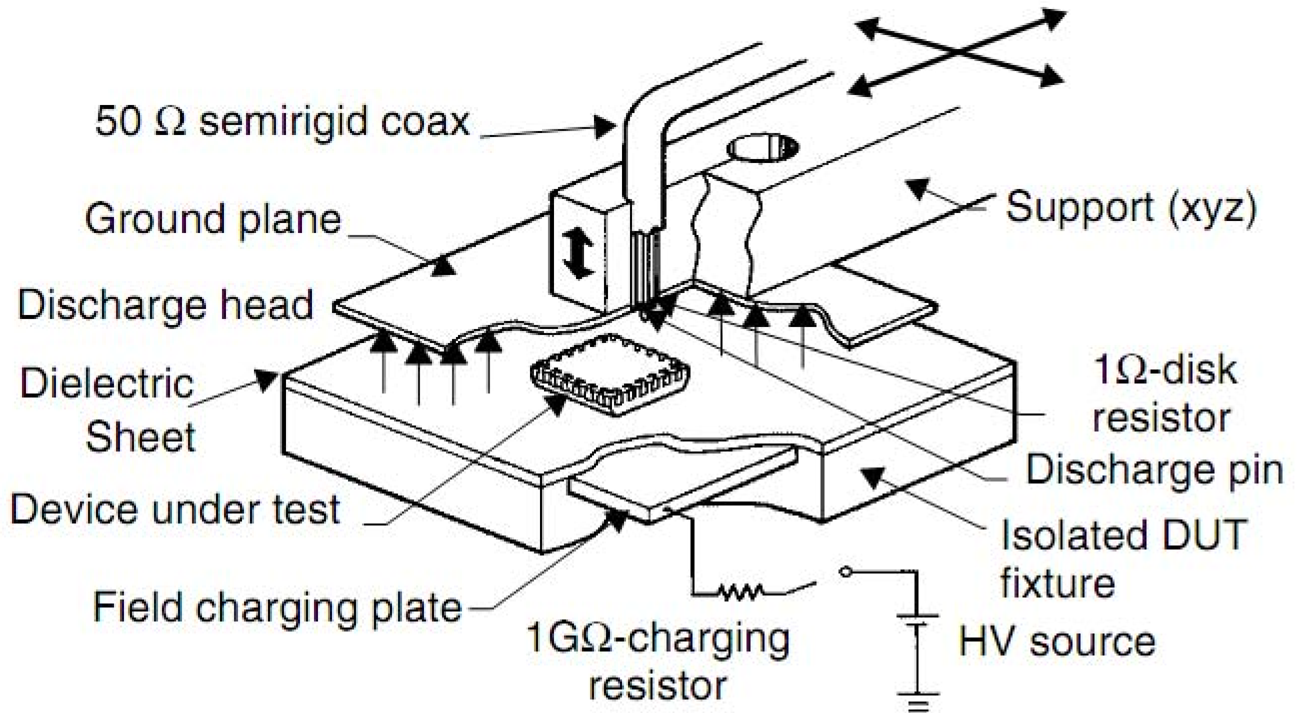


Figure 3.9: *FCDM test system with disk resistor.*

the discharge loop consisting of the bond wire, the pin, the relay, and of any additional wiring to the ground plane.

A similar, but automated, contact mode tester was built by Shaw et al. [3]. Avery has minimized the parasitic inductances of the tester putting the device on a spring-driven horizontal ground plane slider and employing a discharge through an air gap during the approach of the discharge tip.

High-pin count packages with array contacts such as PGA or BGA or bare dies require an automatic CDM-tester with an xy-positioning and a vertically approaching discharge tip preferably with an integrated resistive current sensor.The standardization focuses on these testers. Fig. (3.9) shows a schematic of the first tester of this type employing a disk resistor with extremely low series inductance that has been introduced by Renniger et al. [4]. The name Field-induced CDM (FCDM) reflects the method of field-induced charging and discharging of the device (IC). This machine became the basis for the JEDEC standard [JEDEC-FCDM00]. Correlation was mainly an issue of copying the original machine and setup precisely. For running the test, the IC is fixed by vacuum in “Dead Bug” position on the charge plate, that can be alternatively switched to high voltage or to ground via a high ohmic resistor.

3.3.3.1 TEST PROCEDURE

Four procedures of (F)CDM-charging and stress can be found implemented in the different testers.

- The JEDEC-procedure [JEDEC-FCDM00] stresses the device with two pulses of similar amplitude but of opposite polarity. Lifting the discharge pin before the field-charging plate is grounded leaves the device in a charged state at a high potential to ground. Now, the discharge pin approaches the device again in order to discharge it. This method is very time effective, but limited to qualification test Fig. (3.10) top.

- In the ESD Association FCDM case [ESDA-CDM99], the field-charging plate is contacted to the high voltage while the device is not grounded via the discharge pin. Then the discharge pin approaches the device and a stress impulse charges the device. A positive potential of the charge plate results in a stress current impulse with positive polarity. While the device remains grounded, the charge plate is slowly discharged to ground via the 1G-resistor.

- In an alternative slow charge FCDM mode, the device is contacted first, then it is charged by connecting the field-charging plate to the high-voltage HV via the 1G-resistor or raising the voltage. Then the discharge pin is raised and the charge plate is grounded. In this case, a positive voltage at the field-charge plate causes a negative discharge current Fig. (3.10) bottom.

- In the direct charging CDM specified by the ESD Association, the field-charging electrode remains connected to ground. Therefore, some CDM publications refer to the field-charge plate as ground plane. Independent from the discharge pin, a dedicated charge pin is located at one edge of the ground plane and connected to the HV-supply via a high-ohmic resistor. Moving the discharge head, this HV- pin is brought into contact with the IC for charging. A positive charge polarity results in a positive stress current.

It should be noted that the failure thresholds strongly depend on the polarity of the stress current. For analysis purposes it is mandatory to know the thresholds for both polarities and the associated failure sites. A minimum of three devices must be electrically characterized with respect to their static and dynamic parameters specified in the data sheet. At least, during development, data logging of these characterization tests is recommended for a direct comparison after stress. Before starting the CDM test, the operation of the tester needs to be verified. Any conductive contamination needs to be removed from the tester and the devices and any direct skin contact must be avoided. The devices should be cleaned in an ultrasonic bath filled with isopropanol. All pins of the device must be precisely aligned with the xy-axis of the CDM-tester. Any misalignment has a significant influence on the discharge current. Further, the height z must be adjusted such that in its lowered position the discharge pin at least touches the device pin or solder ball. For CDM, one pin after the other is stressed charging and discharging the device three times for each polarity. Then the devices are electrically characterized again. If all of them pass, the procedure is repeated with the next higher stress level. After qualification and verification, the test setup including the metrology chain (except oscilloscope for verification) must not be changed, in particular, no dielectric layers beneath the DUT and the charge plate must be added. The dielectric would reduce the capacitance and thus increase the failure threshold. It is recommended to measure and study the discharge current at least for analysis purposes at some pins of an IC as it helps to detect improper stress as a result of charge loss or misplacement, it provides good insight into the behavior of ICs under CDM-stress, and if systematically carried out helps identify under which circumstances ICs are CDM-sensitive to which discharge parameter peak current, full width at half maximum FWHM, oscillation and/or voltage. For devices with dielectrically isolated circuitry all pins need to be charged simultaneously. Experience over years

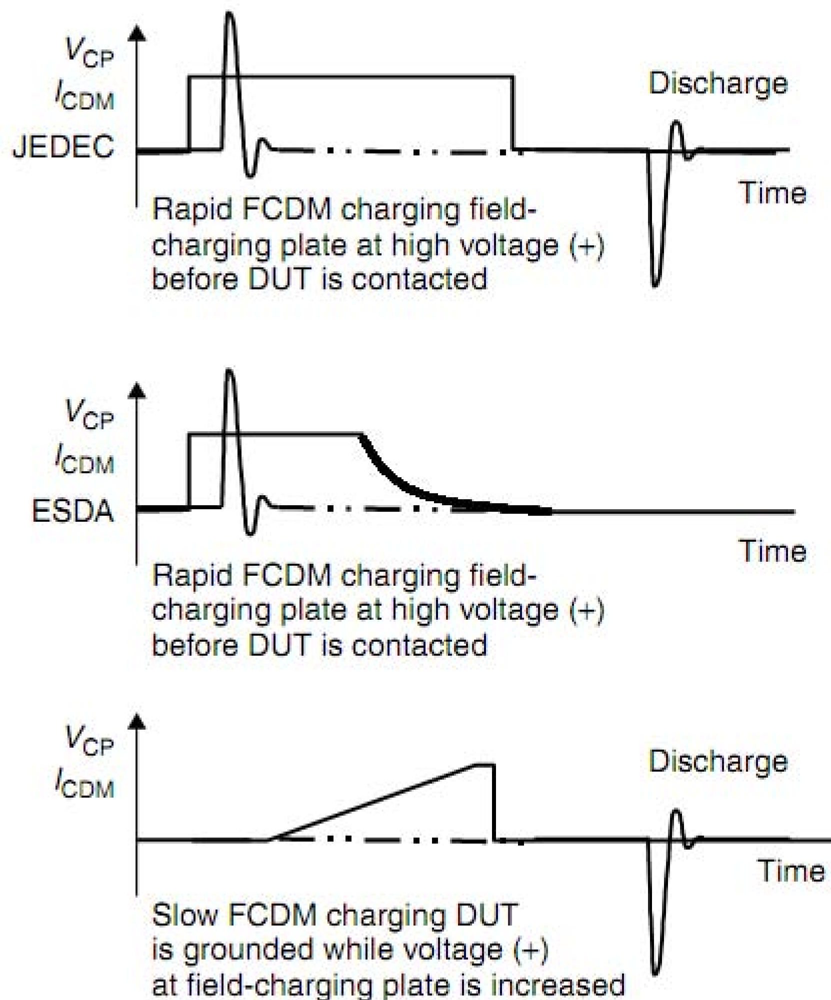


Figure 3.10: *Comparison of three FCDM charging sequences resulting in a double stress of both polarities and in a single-stress impulse during either the charge or the discharge. Depicted are the voltage of the field-charge plate and the CDM current for the different contact states of the discharge pin.*

with various (F)CDM-testers, that were or were not compliant to a specific standard, has shown that devices passing $\pm 1kV$ or even better $\pm 1.5kV$ did not fail in a protected manufacturing and handling environment, while critical devices have merely passed a $\pm 500V$ (F)CDM-test on any system [ESDA- CDM] and studies have shown that lower than $\pm 500V$ pass levels can give rise to production fallout. A minimum protection for $7A$ peak current during CDM is required.

Finally, unlike in HBM, in CDM the package determines the capacitance and contributes to the impedance of the discharge path. Therefore, the failure thresholds depend directly on the package and any change of it or its material requires a new CDM qualification with respect to the current qualification practice. This characteristic, together with the difficulty to build testers and the reproducibility problems shown in the previous sections make it difficult to develop a unique standard, and standardization efforts are still going on together with the evolution of the model.

3.3.4 OTHER STRESS MODELS

There are also other stress models that aim at reproducing some specific practical cases, like the SDM (socket discharge model), the contact discharge model, the CBM (charged board model) and the cable discharge event (CDE) that is related to any cable connection (LAN etc...), but all of them models give high reproducibility problems.

An ESD stress model that is particularly important is the TLP (transmission line pulse), that allows to monitor the current and voltage waveforms of the electrostatic discharge. This model is the one used in this thesis work and because of this it will be presented in the chapter that describes the measurement setup and experimental details.

3.4 DEVICES PROTECTION STRATEGIES

We have seen that an ESD that a person can not even feel, for example in the order of 100V, can easily damage electronic components. In fact the smaller the device the more sensitive it is. The ESD caused device damages, that mostly have a thermal nature (but can be also associated to oxide breakdown), can give not only catastrophic failures, detectable through inspection, but also latent defects, that remain unnoticed until the actual operation of the device. These latent defects are the most costly, in fact they cause the device to work for a while for customer applications, before giving unexpected and unexplained failures and consequently more returns, warranty costs and lower customer satisfaction. For these reasons ESD control methods are employed in the fabrication process and during usage where possible; furthermore protection devices can also be integrated within the IC circuits and global applications, to cancel or at least reduce the effects of ESDs.

3.4.1 ESD CONTROL METHODS

One of the possible strategies to protect devices from ESDs, consists in using some control methods to strongly reduce the probabilities of having one. This strategy is particularly effective at a manufacturing stage, where is possible to modify the environment and the handling procedures.

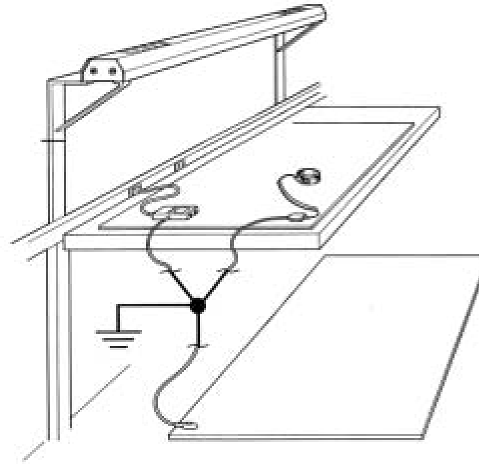


Figure 3.11: *Example of ESD preventing policy. Grounding of ESD floor materials through connection to equipment ground.*

Different solutions to reduce the risk of damage are employed at all the levels of manufacturing, for example modifying the process technology to build-in ESD robustness to the transistors at a process level, or spending resources for on-chip protection design at the signal pins connected to the package.

In general to avoid ESDs, it is useful to employ static control materials. In fact it is strongly recommended to remove insulator materials from the workplace whenever possible, while dissipative materials, that bleed off charges at a optimum rate, are a strongly preferred choice. Furthermore, to avoid ESD risks, all conductors must be grounded and, to neutralize charged insulators, that cannot be grounded, ionizers that flood the environment with ions are employed, neutralizing possible excess charge.

Not only conductors but also workers must be grounded to minimize damage risk, in fact ESD events are often caused by human handling. To achieve these goal people must wear proper clothes, together with wrist straps and/or foot grounders, that must be tested daily to guarantee their effectiveness.

Other solutions commonly employed are the usage of dissipative work surfaces and conductive floor materials, to help bleed off charges quickly and prevent charge accumulation.

Outside ESD-protected areas electrostatic discharges are much more likely to happen, it is therefore necessary to shield ESD sensitive items through the usage of close metalized shielding bags or conductive boxes.

It is important to notice that these techniques must be employed not only during the manufacturing process, but also in the testing phase, where human handling is commonly required.

3.4.2 ESD PROTECTION DEVICES

If during the manufacturing process it is possible to modify the environment and the handling procedures, during the normal operation this is not feasible. It can be thus necessary to include some active protection structures within the IC or global system.

This work is not aimed to study ESD protection devices, nevertheless they are an important subject and it is useful to know know something about them. Because of this, in the following we are gonna have a very brief overview about the requirements to these circuits and some examples.

The ESD protection circuit elements have to possess some fundamentals characteristics: they have to clamp the discharge voltage to shunt the stress current, that can be several Amperes for about $100/150ns$. The short duration of the ESD makes it clear that these devices must also be very fast. Their turn on time has to be lower than 1 ns, in fact they obviously have to be faster than the rise time of the discharge, otherwise they could not clamp it. Another fundamental property they must possess is robustness, to protect the device from numerous pulses, furthermore they must not influence the normal device operation, for example introducing minimum series resistance and capacitance. Together with these fundamental properties, they are required also to be cheap and occupy minimum area.

Some examples of circuits and devices that can be employed comprise diodes (as clamping elements), used in the following configuration

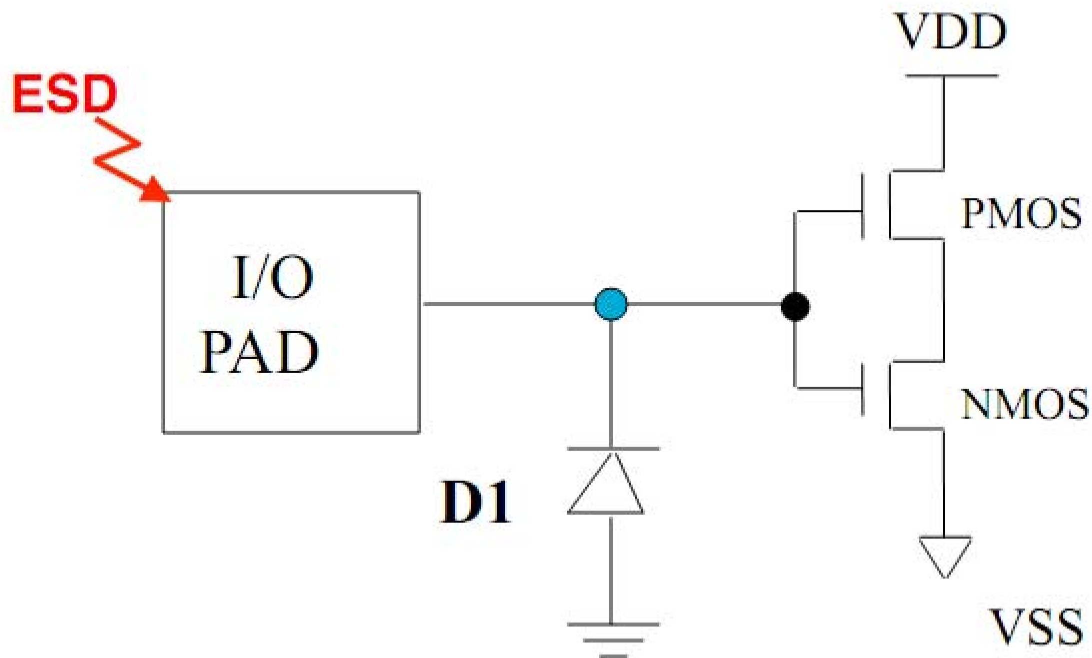


Figure 3.12: *Single diode ESD protection circuit.*

For positive overvoltages we have the breakdown of D_1 , for negative ones it is in conduction mode.

This basic scheme can be slightly modified to improve protection, adding another diode.

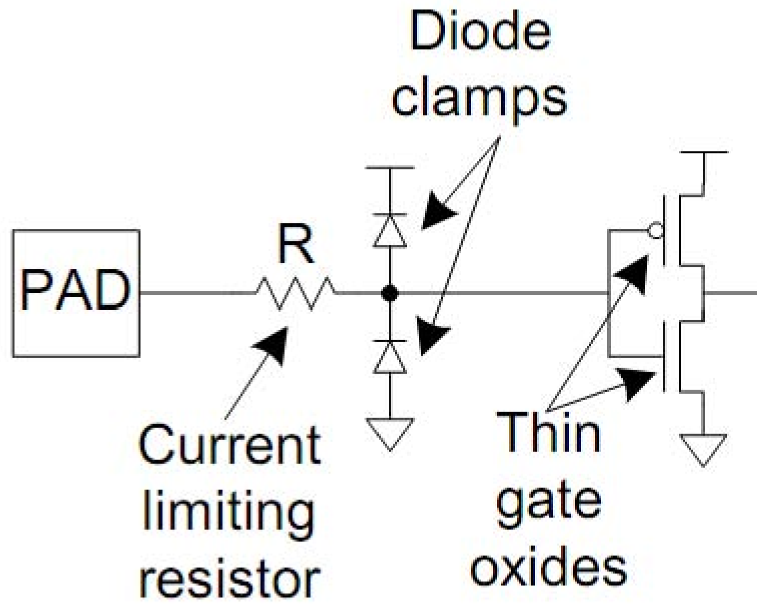


Figure 3.13: *Basic diode ESD protection network.*

The protection scheme complexity can be increased further adding two other diodes, obtaining the following circuit.

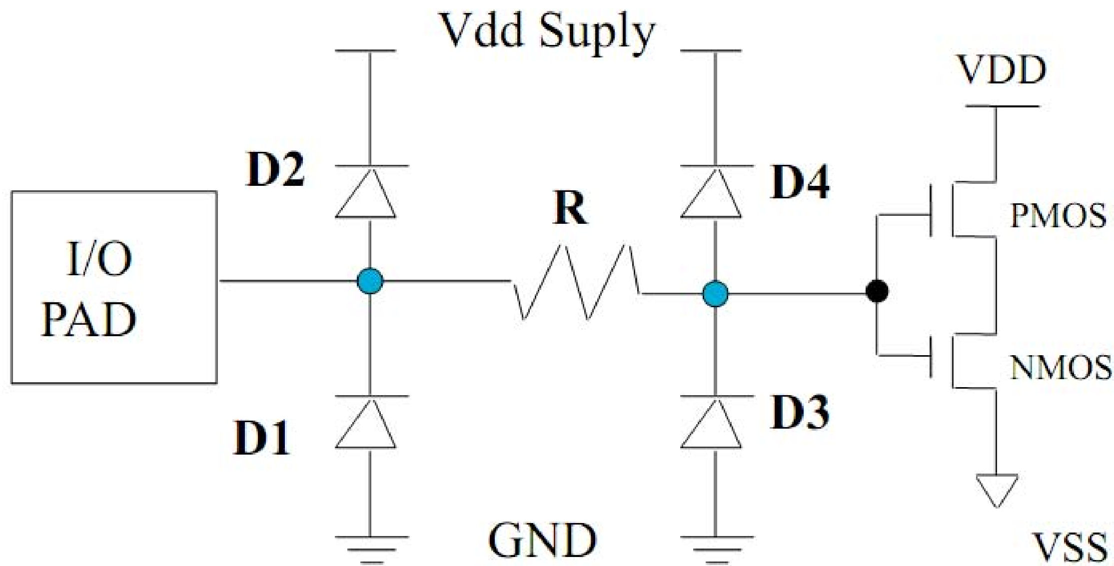


Figure 3.14: *Four diodes ESD protection circuit.*

D

This is the traditional protection concept where diodes are used. D_1 provides protection to ground, and D_2 provides it to V_{dd}. D_3 and D_4 are local clamps for oxide protection. However, in advanced technologies D_1 and $D_3$are not efficient and are replaced by NMOS protection concepts.

Another possibility to protect devices from ESD, is the usage of an NMOS transistor, exploiting

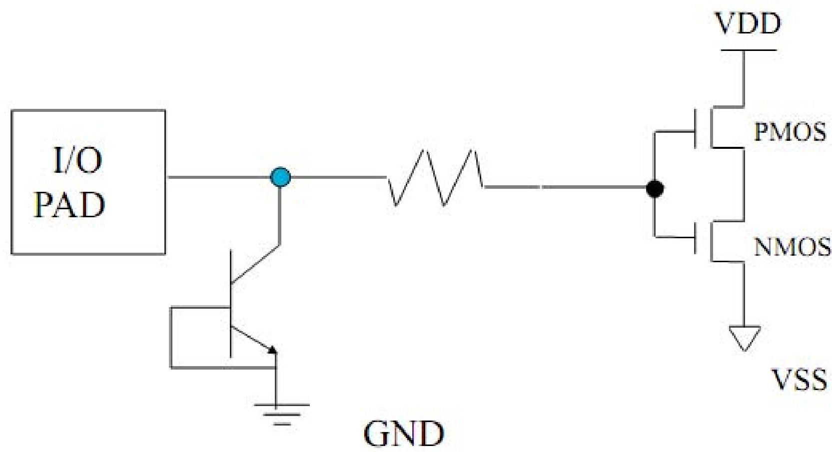


Figure 3.15: *Bjt based ESD protection.*

its parasitic BJT (what we called NMOS protection concept), obtaining the equivalent circuit of fig. (3.15) .

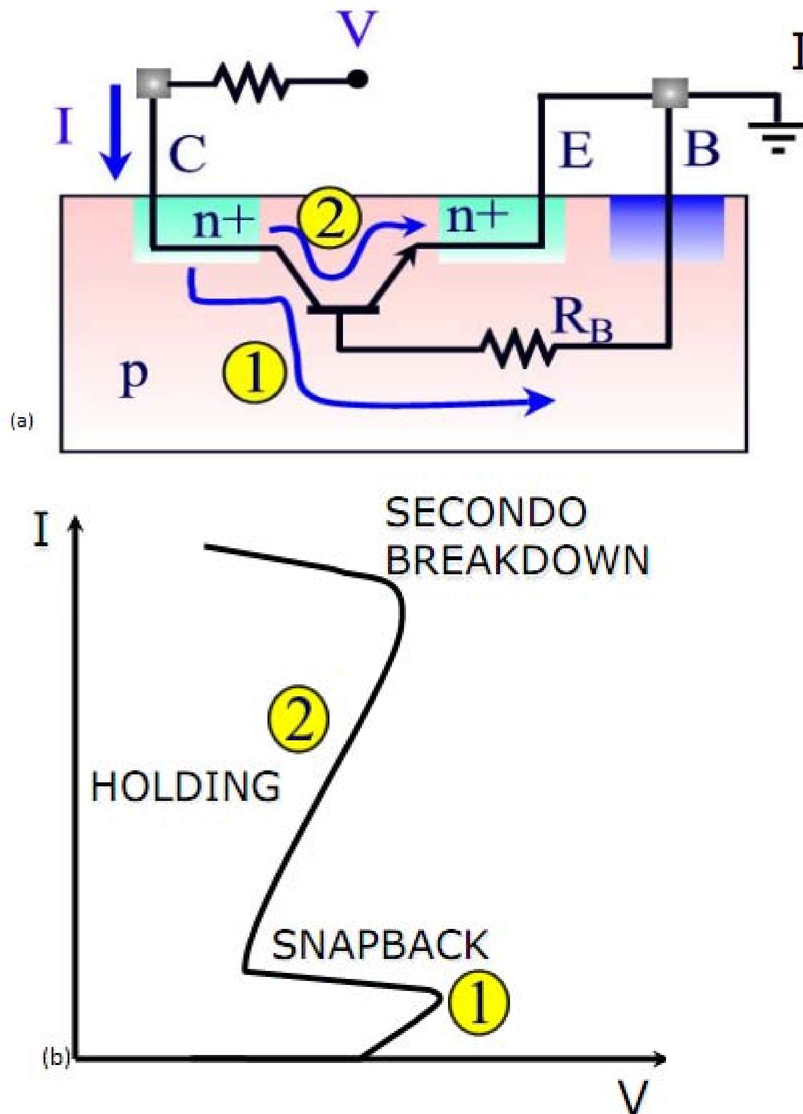


Figure 3.16: *NMOS used as ESD protection element. (a) Device section and (b) I-V characteristic under a positive stress pulse.*

In the previous image we indicated as 1 the breakdown of the collector-base junction, and as 2 the holding phase that takes place when the bjt parasitic turns on because of the voltage drop on the bulk resistance.

The NMOS device provides protection for positive stress by clamping below gate oxide breakdown and can be sized to exceed the ESD current level for 2kV HBM. For negative stress the substrate diode provides protection for greater than the current level that corresponds to 2 kV. HBM. A comparison between the different solutions shown previously can be seen in Fig. (3.18).

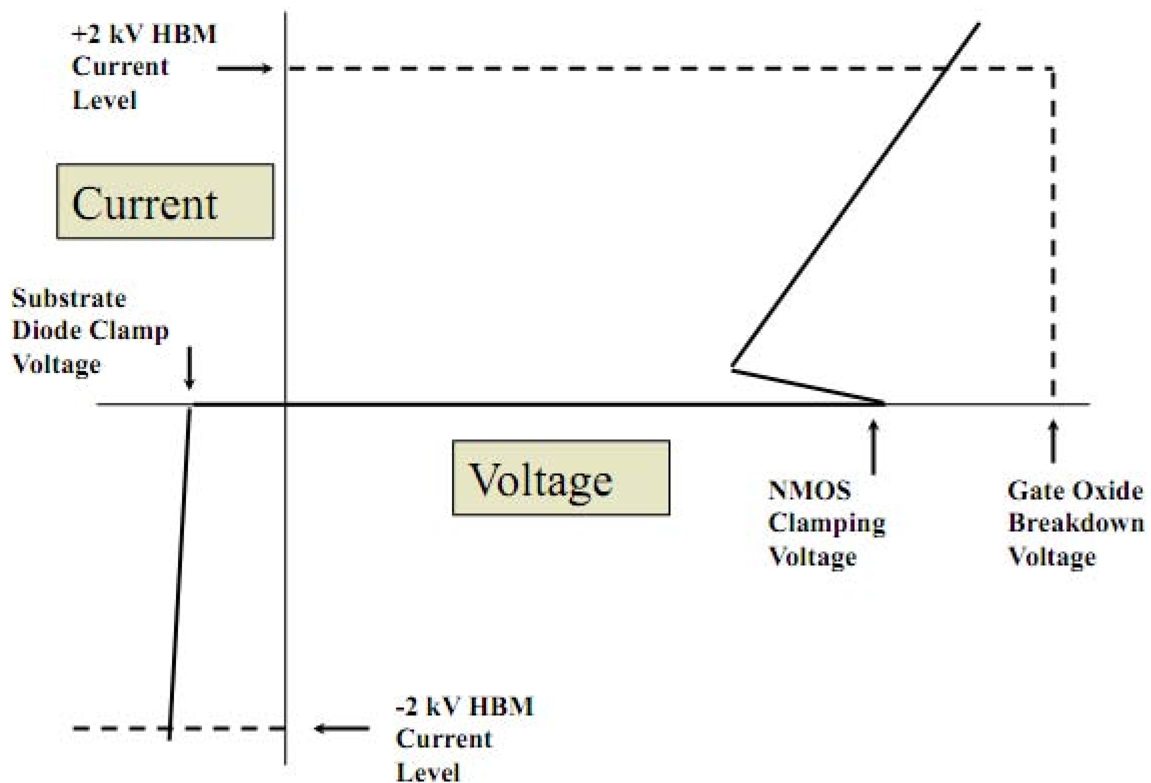


Figure 3.17: *Typical I-V of the NMOS used as ESD protection device.*

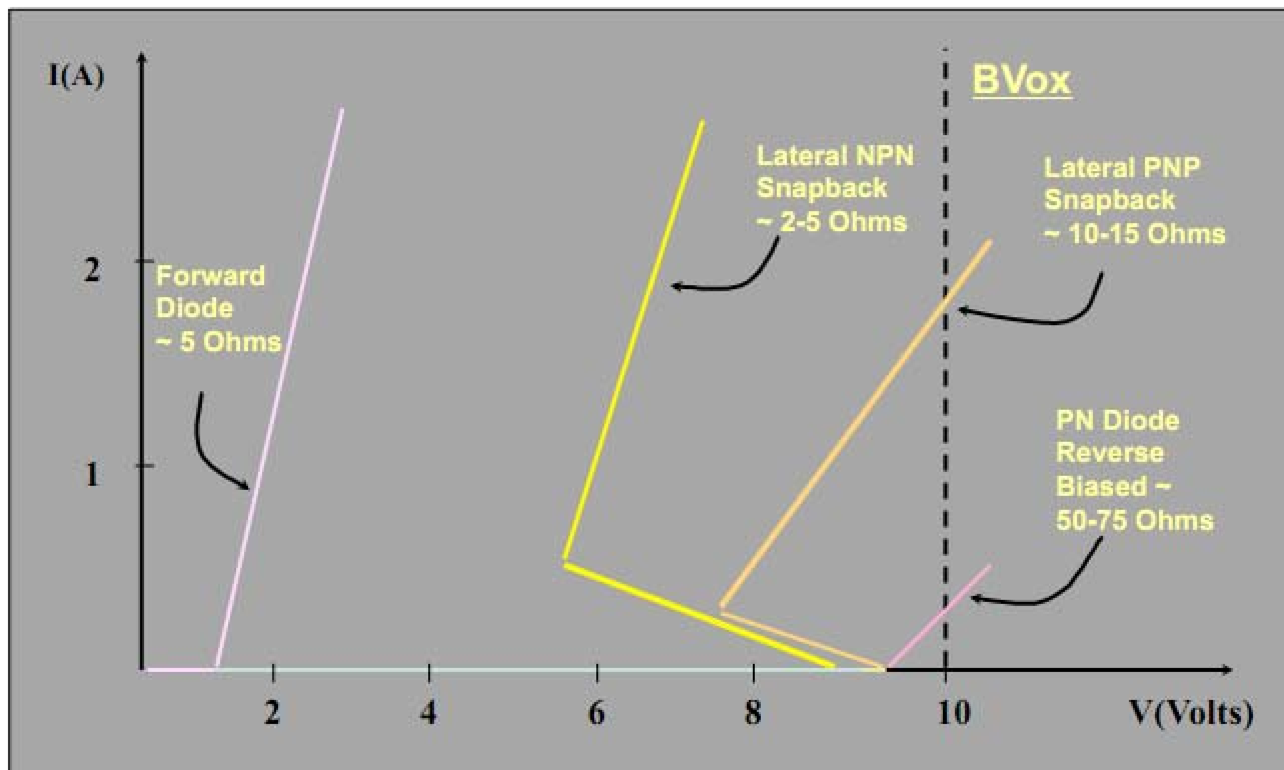


Figure 3.18: *Different ESD protection elements behaviour.*

Chapter 4

ESD ON LED DEVICES

This investigation is aimed at understanding the effects of ESDs on monochromatic LED modules, a topic that has not been widely studied yet. Before showing our work it can be useful to try to understand the results obtained by previous investigations on some related topics.

4.1 PREVIOUS WORKS ON ESD EFFECTS ON LED DEVICES

There is not much work done on the the effects of ESDs on LED devices, but a very interesting paper about this topic is [5]. This article describes an experimental work carried on green LEDs emitting at 2.33 eV (532 nm), based on multi-quantum well. In this study the devices, after an initial electro-optical characterization, were submitted to reverse-bias stress test and to reverse-bias ESD events using a Transmission Line Pulser-Time Domain Reflectometer (TLP-TDR). Characterization through emission microscopy measurements before the stresses, indicated that the LEDs could emit light when submitted to reverse-bias. The reverse-bias luminescence was found to be localized on a number of emissive spots, randomly distributed on the device area. Even if analyzing the behaviour of LEDs under reverse-bias is not part of the goals of our work, this result is nevertheless very interesting. In fact these spots correspond to the presence of preferential paths responsible for leakage current conduction, and these paths, related to the presence of structural defects, can represent weak regions with respect to reverse-bias stress or ESD events; in fact under reverse-bias conditions, they can be crossed by a significant reverse current density, that can generate both gradual and catastrophic degradation.

The most interesting part of work [5], is the ESD stress test. As previously said, the tests were carried on exploiting a Transmission Line Pulser-Time Domain Reflectometer (TLP-TDR) system. For each voltage pulse the corresponding TLP current and the leakage current after the pulse were measured (see Fig. (4.1)). The study showed that after ESD failure, LEDs behave as short circuits and Scanning Electron Microscopy (SEM) investigation demonstrated that ESD damage interests a localized region (see image in Fig. (4.2)). In most of the cases, damaged regions were located in correspondence of one of the leaky paths identified (before stress) by emission microscopy. This result suggested that leakage paths responsible for reverse current conduction constitute weak points with respect to ESD events, since they allow an extremely

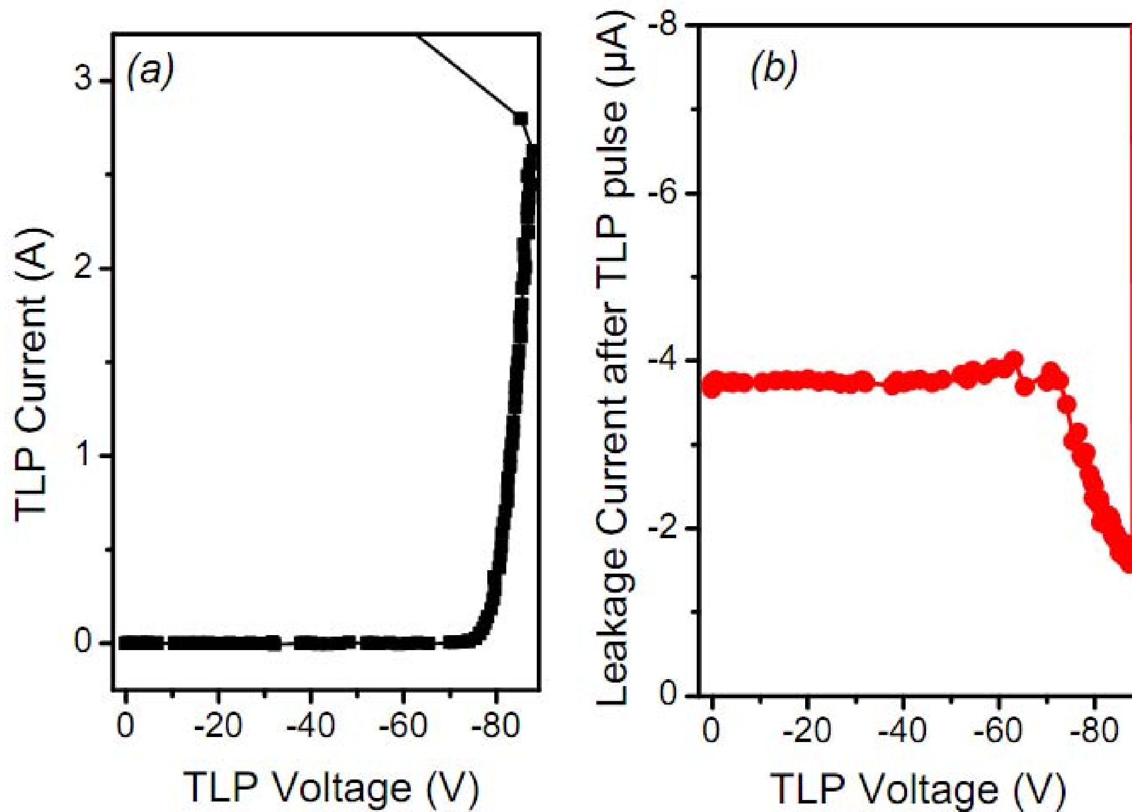


Figure 4.1: *(a) I-V curves of one of the analyzed LEDs measured by the TLP setup. The maximum TLP current reached by the LEDs before failure was used as a parameter to define the ESD robustness of the LEDs (for this device it is equal to -2.6 A). (b) leakage current measured after each TLP pulse: TLP current levels greater than 10 mA can induce a decrease in the leakage current of the devices, possibly due to the annihilation of defect-related leakage paths [5].*

high current to flow through a small-size path. The authors could therefore demonstrate that the presence of structural defects can strongly limit the ESD stability of the LEDs, because under reverse-bias current flows through localized defect-related paths. This means that a significant improvement of the ESD and reverse-bias robustness of GaN-based LEDs can be obtained only by an accurate control of the defectiveness of the active layer.

Another interesting work on the ESDs effects on LEDs is [6]. Even if this article is a bit old, it is still interesting, since some of the results there highlighted confirm what is shown in [5]. This older article describes an experimental analysis carried out on different commercial GaN LEDs available at that time. In particular products of three suppliers were tested, with different layouts and materials. The LEDs of two suppliers were grown on sapphire, and because of this (sapphire is non-conductive) they had both of the contacts on the top, while the other supplier employed a SiC substrate (conductive) that allowed to design a top and a bottom contact. The LEDs were submitted to "single polarity" ESD stress tests, with both positive and negative HBM, starting from ±500 V up to ±8 kV with 100V steps, and TLP pulses, starting from 100mA and reaching 8A for the positive stress. These tests allowed to observe that the LEDs grown on SiC has an excellent robustness in both polarities, with a better performance than the others, showing no failure at all for the range of voltages and currents considered. This is important because it shows that the quality of the material is not the only parameter that can have an influence

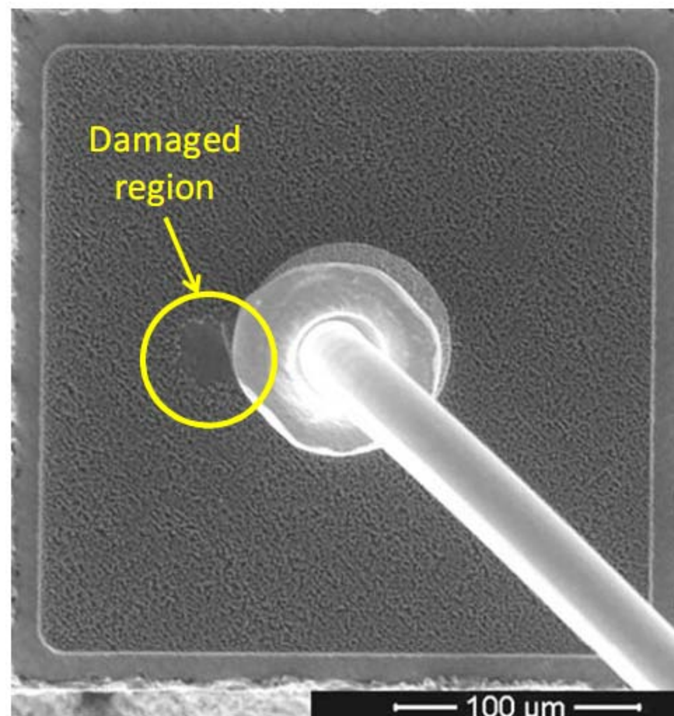


Figure 4.2: *SEM image of one LED after ESD failure. The position of the damaged region is highlighted in the figure [5].*

on the ESD robustness, but also the device structure can help improving it. In fact different layouts strongly influence the current flow and distribution, giving rise for example to current crowding phenomena. Observing the analyzed LEDs structures we can immediately understand how having a top and a bottom contact allows a vertical current flow, with a better distribution than the lateral current flow that characterizes the mesa-etched structure of the LEDs grown on sapphire. Current crowding and distribution are therefore important characteristics, and that is highlighted by the failure analysis reported in the paper. For the first type of the LEDs grown on sapphire, damages were in fact localized along the border of the semitransparent metal toward the n^+ contact, both in the positive and in the negative pulses case. Another interesting observation reported in the article is that in the case of negative pulses, damages were much larger, due to the much higher power locally dissipated in that case. In the paper is also reported that some premature-failure cases occurred, in which damages where randomly distributed on the surface, possibly in correspondence of defects.

In the case of the second type of LEDs grown on sapphire, positive pulses-induced damages were located along the border as in the previous case. After the negative pulses stress tests instead, the devices presented damages randomly distributed across the surface. This situation could be associated with a poor quality of the GaN/InGaN grown materials, resulting in high defect density and in the uneven emissivity observed in the untested devices.

This paper confirms then that ESD robustness strongly depends on the defect density, but also shows that other characteristics, such as the device layout, can have an important influence on it, with the necessity to guarantee a uniform current distribution on the chip, even at the highest current densities.

These two articles demonstrated the importance of the material quality for the ESD characteristics of the LEDs. This quality is perhaps strongly influenced by the fabrication process

parameters, that can therefore change the devices properties. An example of this is given in [7]. This paper describes an experimental work in which a certain number of GaN based LEDs with p-cap layers grown at various temperatures were fabricated. The samples used in the study were all grown on <0001> sapphire substrates by metal organic vapour phase epitaxy (MOVPE) and were characterized by a InGaN/GaN MQW structure consisting of a a 30-nm-thick GaN nucleation layer grown at 520 °C, a 1- m-thick undoped GaN layer grown at 1050 °C, a 2-μm-thick Si-doped GaN n-cladding layer also grown at 1050 °C, an InGaN/GaN MQW active region grown at 700 °C and a 0.2-μm-thick Mg-doped GaN cap layer grown at various temperatures. The MQW active region was formed by five periods of 3-nm-thick InGaN well layers and 15-nm-thick GaN barrier layers (the structure of these devices is better shown in Fig. (4.8)). Since p-GaN layers were grown on top of the active regions, growth temperature was a very important parameter (and that is true for nitride-based LEDs in general). In fact high-temperature grown p-GaN layers might result in degraded optical and structural properties of the LEDs because of quantum well intermixing and dopant redistribution that may occur when a high-temperature grown p-GaN cap layer is deposited onto the low-temperature grown InGaN/GaN MQW region. On the other hand, crystal quality of the top p-GaN layers strongly depends on the growth temperature and is better when this parameter is higher. This could result in improved ESD characteristics of the nitride-based LEDs.

Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) were used to physically characterize surface morphologies and cross sections of the samples. The ESD characteristics of the devices were then measured by an Electro-tech system ESD simulator Model 910, which could produce electrical pulses similar to those originated from human body. The authors of this article applied both negative and positive ESD pulses onto the LEDs, starting at 1000 V human-body model and successively increasing the pulse amplitude with a step of 100V. After each test the LEDs leakage current at -5 V was measured and the failure threshold was fixed at 2 μA.

The TEM microscopy analysis yielded very interesting results. In fact, considering Fig. (4.3), where a sample with a 900°C grown p-GaN cap layer is shown, we can see that in this particular device a large number of defects exist. It can be seen that these defects are V-shaped, with a threading dislocation connected at the bottom. The formation of these V-shape defects could be attributed to the fact that Ga atoms might not have enough energy to migrate to proper sites at such a low temperature, thus lateral growth rate of GaN becomes smaller. Fig. (4.4) shows SEM micrographs of two samples with p-cap layers grown at 900 °C and 1040 °C respectively. It was found that that the surface morphology of the device with a 900 °C grown p-cap layer was rough, thing that could be again attributed to the low migration speed of Ga atoms at 900°C. In contrast, the surface morphology of the sample with the 1040 °C grown p-cap layer was much smoother, with almost no visible V-shape defects.

The results regarding the ESD robustness are shown in Fig. (4.5). It can be clearly seen that all of the LEDs tested had high robustness toward positive ESD pulses, enduring voltages higher than 7kV. Much more interesting are the results of the negative pulse ESD tests. In fact it was found that while LEDs with 1040 and 1100 °C grown p-cap layers could withstand negative pulses up to 3500V, devices with 900 °C grown p-cap layer had much poorer performance, enduring just 1100 V negative pulses. This result is particularly important because it shows that is possible to significantly enhance ESD characteristics of GaN-based LEDs by simply increasing the growth temperature of p-GaN cap layers.

nevertheless, as previously said, we should notice that higher growth temperature could cause poorer optical properties. To address this issue, output power of the LEDs prior to ESD stressing

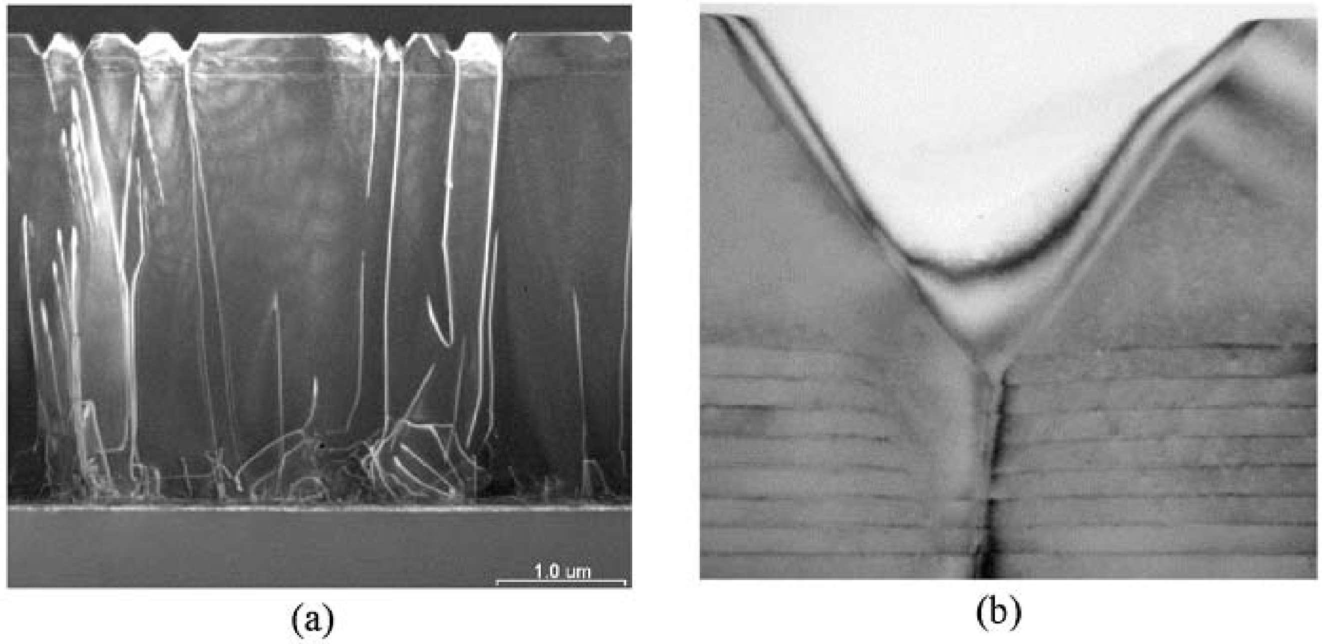


Figure 4.3: *(a) TEM micrograph of the GaN-based LED with a p-GaN cap layer grown at 900 ˚C. (b) Shows an enlarged image of the same sample [7].*

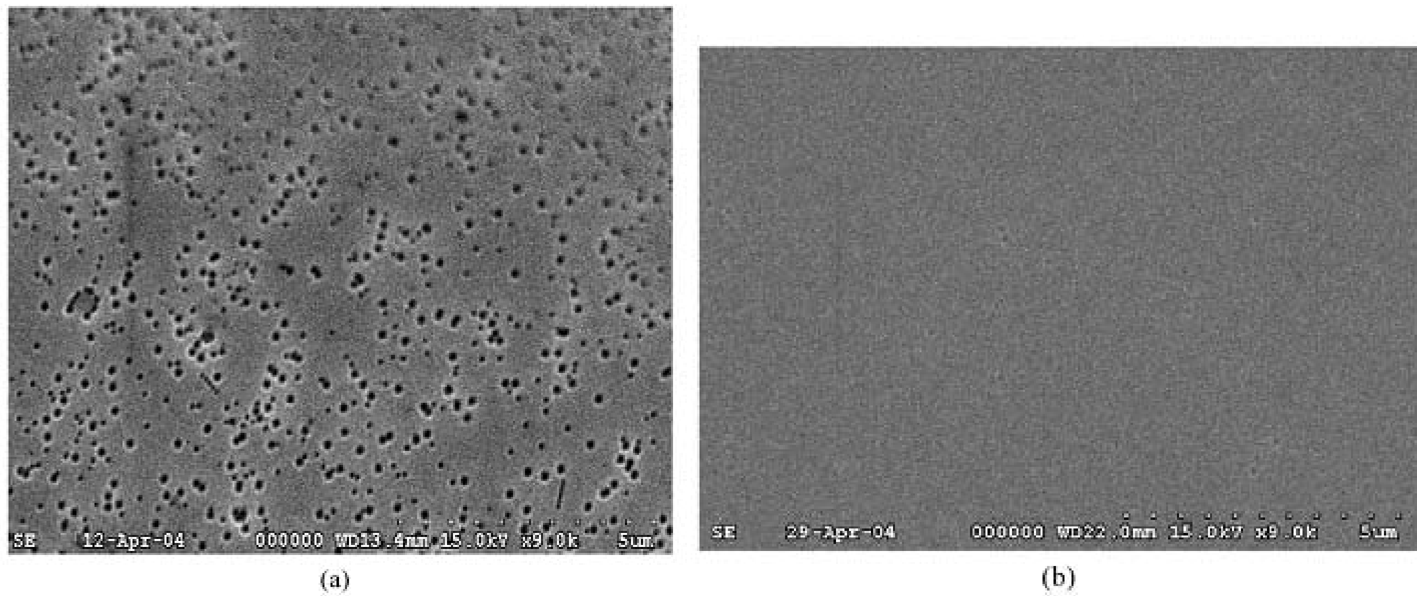


Figure 4.4: *SEM micrographs of the LEDs with p-cap layers grown at (a) 900 ˚C and (b) 1040 ˚C [7].*

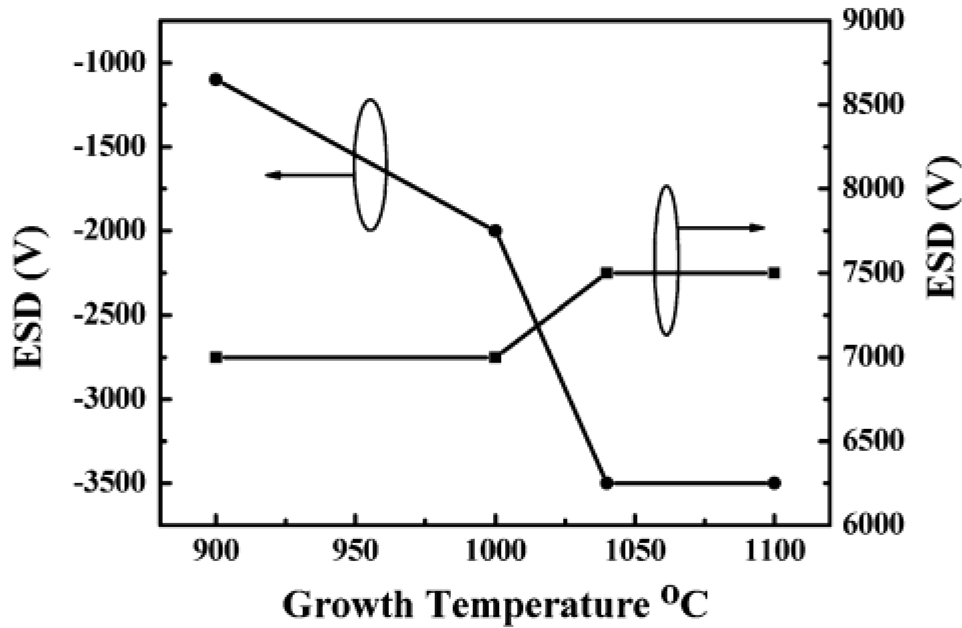


Figure 4.5: *Measured ESD results for the LEDs with p-cap layers grown at various temperatures [7].*

was also investigated. As shown in Fig. (4.6), it was found that devices with 900 °C, 1000 °C and 1040 °C grown cap-layers were all around 5.5 mW. In contrast, output power of the LED with 1100 °C grown p-cap layer was only around 2.8 mW. It was also found that increasing the p-cap layer growth temperature to 1100 °C made the device surface darker, a phenom that the authors of work [7] believed due to indium out-diffusion caused by the high temperature.

Finally some useful informations were deduced observing the photographs of the ESD damaged LEDs (Fig.(4.7)). The LEDs with 900°C grown p-cap layers presented some dark spots randomly distributed across the LED surface, that the authors of the paper believed to be related to the V-shaped defects, the weakest points in the LED (Fig.(4.7) (a) and (b)). In contrast, a whole dead-area was observed on the LED with the 1040 °C grown p-cap layer (Fig. (4.7) (c)). This area, because of the much higher ESD pulse voltages endured, was located where the electric field intensity was higher and this can be clearly seen with reference to Fig. (4.8), where the position of the anode and cathode contacts is shown. This work clearly showed that even temperature has an important influence on the LEDs robustness towards ESD events.

Some of the authors of [7] also contributed to another interesting article ([8]), showing that beside growth temperature and device layout, a different layers thickness and structure can play a major role in defining the ESD robustness characteristics of the LEDs too. In this work, three types of LEDs with a structure similar to the ones of [7] were submitted to ESD stress. Two of these types of devices, one with a low temperature and the other with a high temperature-grown p-GaN top contact, differed from the samples of [7] just for the slight variation of the growth temperature and the thickness of some layers. The other typology of LED instead, had a particular characteristic. In fact the p-GaN top contact was formed by two layers:a high temperature-grown Mg-doped p-GaN layer and a 850 °C grown p-GaN contact over it. This solution was employed to improve the optical properties of the device through a natural textured surface (given by the V-shaped defects), while avoiding the problem of dislocations

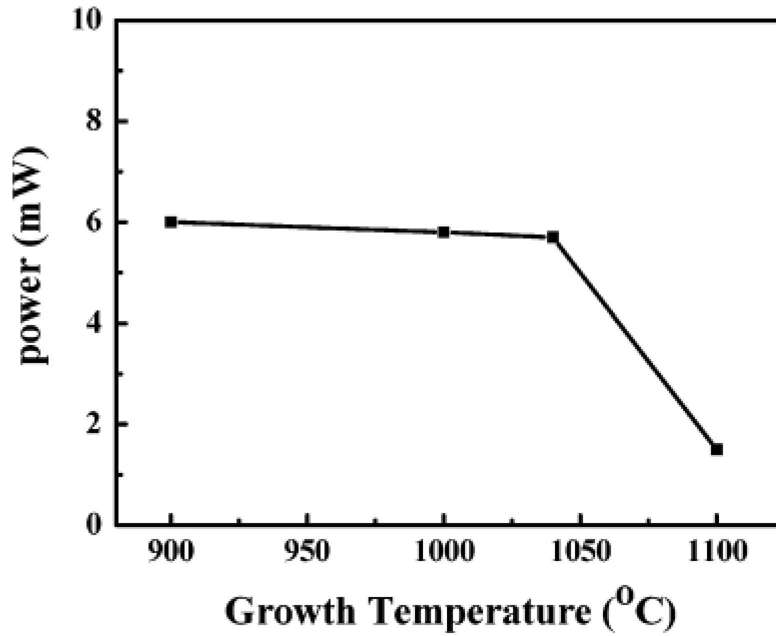


Figure 4.6: *Output power of the LEDs with p-cap layers grown at various temperatures, prior to ESD stressing [7].*

and defects in the p-contact intersecting with the MQW region, issue that would have caused a reduced ESD robustness performance.

In this article the authors referred to the first two types of LEDs respectively as LED II (the one with low temperature-grown p contact) and LED III (high temperature-grown p-contact layer), while the LEDs with the double Mg doped p-GaN layer where referred to as LED I. The ESD characteristics of the samples were measured by an electrotech system ESD simulator (Model 910), capable of generating pulses similar to those that characterize the HBM discharges. The starting voltage value was 300V HBM, and the pulses amplitude was gradually increased with a step of 500-1000V. After each testing phase, the leakage current at -5V was measured and the criterion used to determine the device failure was the same of [7] (a leakage current higher than $2\mu A$). The output power of the LEDs was also measured exploiting a calibrated integrating sphere.

The results of this investigation, summarized in Fig.(4.9), showed that, even if the differences in the LEDs of work [7] and [8] were slight, the ESD robustness of the devices changed significantly. In particular, while the positive pulse resistance was good in both of the cases, the negative-biased ESD robustness of LED I and III of work [8] was much better. In fact, while the samples of [7] could endure pulses of around 3500V, the LEDs of [8] were able to withstand discharges up to 7000V with a high pass yield. As previously said, the authors ascribed this better performance to the difference in the layer structure and growth conditions of the MQW active layer. In particular, the thicker n-GaN layer used in these devices was believed to have caused a reduction in the thread dislocations intersecting the active layer, thus enhancing the ESD characteristics. LEDs III also presented a higher total thickness of the p-layer, characteristic that was believed to have produced a better current spreading effect, contributing to the enhancement of the ESD robustness of these devices.

The importance of improving the current distribution in a LED structure and the strong influence

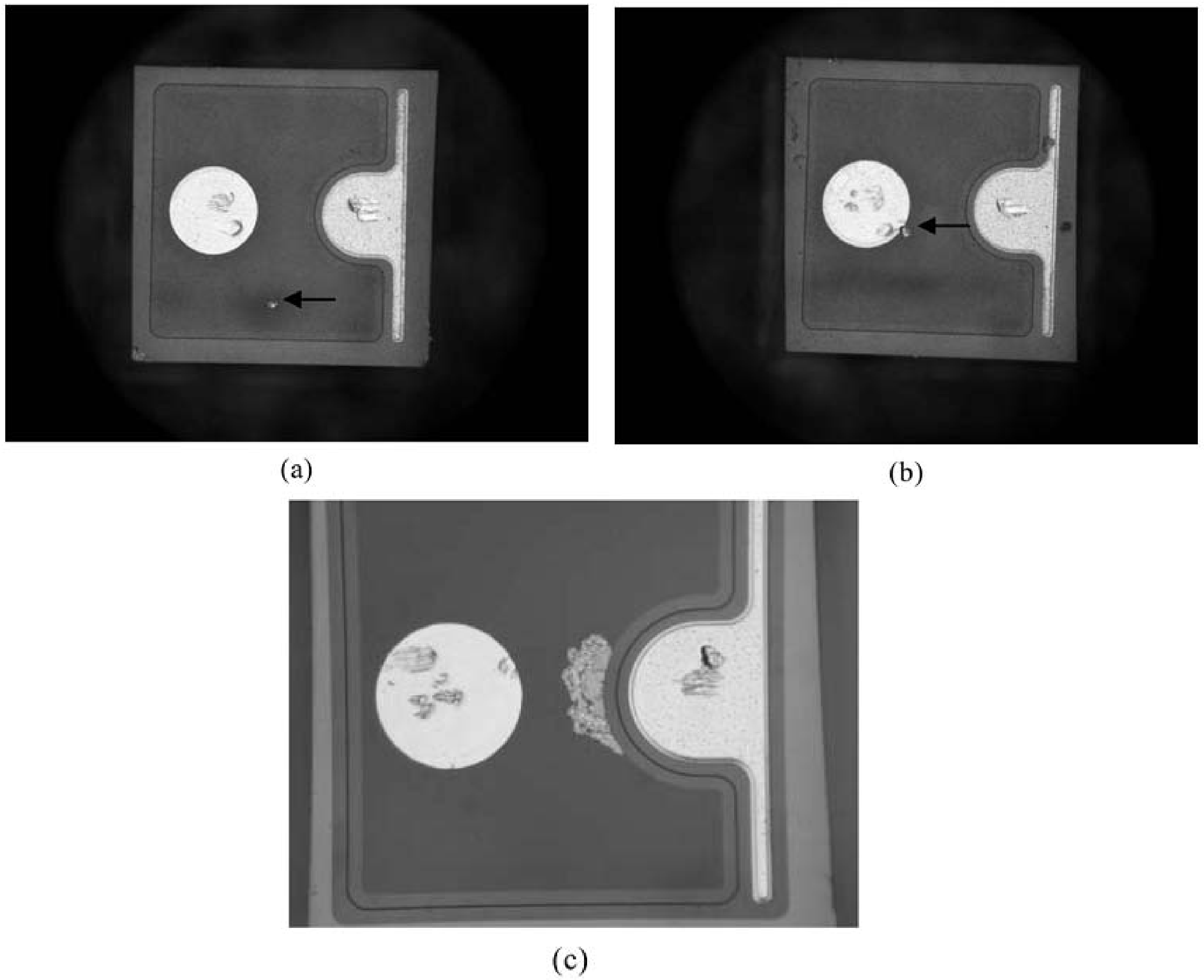


Figure 4.7: *Photographs of the ESD damaged LEDs with (a) and (b) 900 °C and (c) 1040 °C-grown p-cap layers [7].*

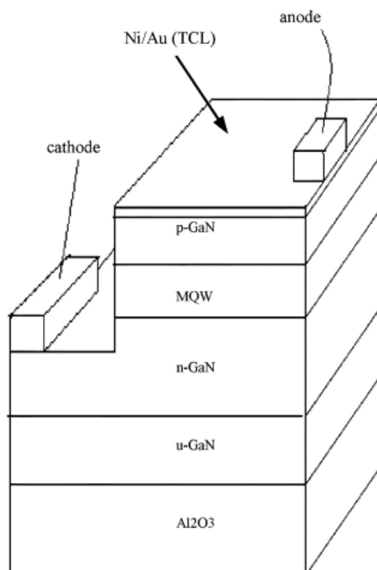


Figure 4.8: *Schematic diagram of one of the devices of work [7].*

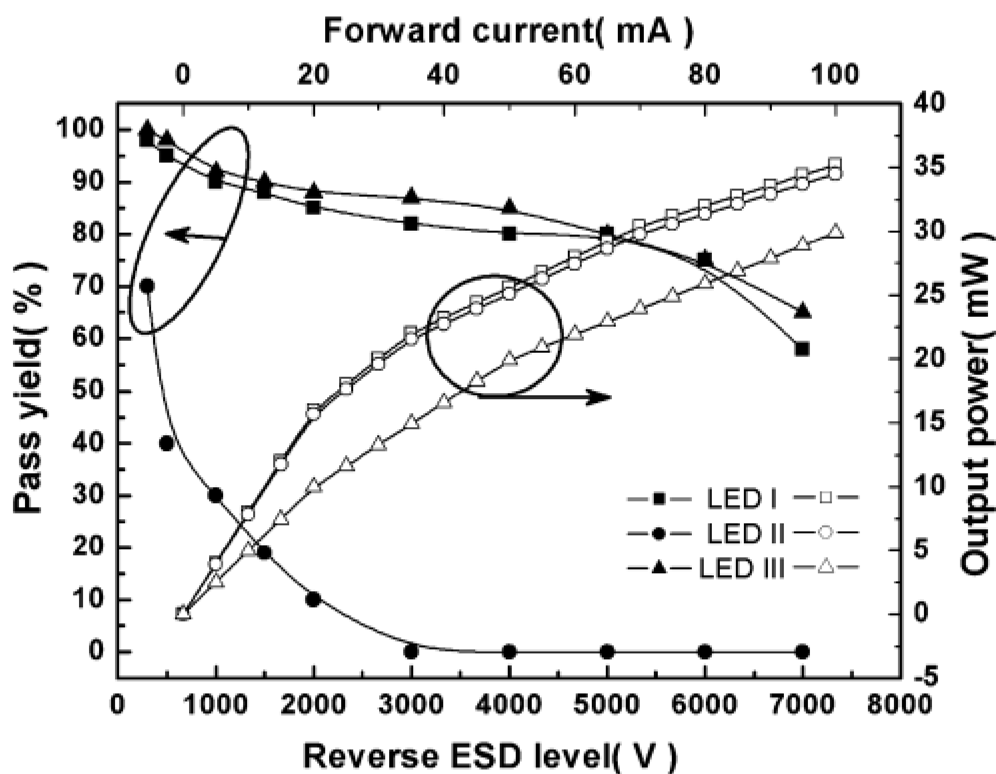


Figure 4.9: *Measured ESD results as function of stress voltages and light output power as function of forward currents for the LEDs. The values shown in the left-hand vertical axis mean the total tested device numbers (100 devices) divided by the non-failed device numbers for a given reverse stress voltage [8].*

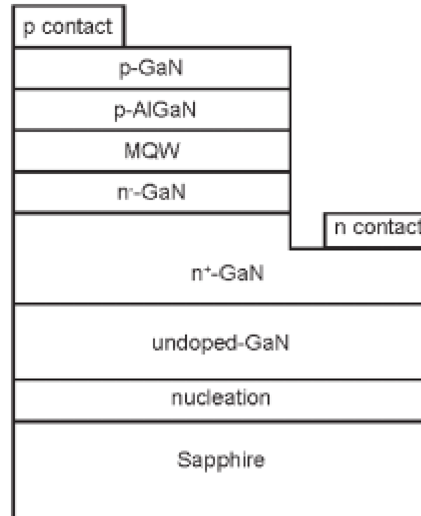


Figure 4.10: *Schematic structure of the LEDs studied in work [9].*

of the layers thickness on the ESD characteristics of a device, are confirmed also by a more recent paper [9]. The authors of this work fabricated three types of LEDs all with the same structure, shown in Fig. (4.10) , but with three different values of thickness of the Si-doped $n^- - GaN$ current spreading layer. In the following we will refer to the devices with 0.15 , 0.2 and 0.25 μm thick layers as LED I, LED II and LED III respectively. The first step of the experimental work was measuring the I-V and L-I characteristics of the samples. After that, a photo-emission-microscopy-based emission microscopy inspection (EMMI) technique was used to analyze the leakage current paths in the devices. Finally, the ESD characteristics of the LEDs were measured exploiting an Electro-Tech System ESD simulator ESS-2002 Model 910, the same used in [7] and [8].

A proof of the current spreading effectiveness of the $n^- - GaN$ layer was given by the L-I curves. In fact, as can be seen in Fig. (4.11), increasing the layer thickness clearly made the output power higher. This could have been due also to a material quality improvement, but an EMMI investigation and the output power mapping of the different LEDs revealed that the leakage paths seemed to be distributed in a very similar way in all the of types of the samples, while the output intensity observed in a LED III type device was much more uniform than in the LED I case (Fig.(4.12) and (4.13)).

The ESD characterization was carried out on 50 randomly selected samples for each type of LED, starting from 100V human body mode and successively increasing the pulse amplitude. The authors also measured the I-V characteristics of the samples before and after each stress, and decided that if the measured current varied by more than 30% from its original value, then the device was considered to have failed. The results of this analysis are shown in Fig.(4.14). It was found that only 60% of the LED-I chips survived after a 1200V stress. With the same 60% survival rate, it was discovered that LED-II and LED-III could endure ESD pulses up to 1800 and 3000 V respectively. This was attributed to the better current spreading for the samples with a thicker $n^- - GaN$. In fact, since this thick layer results in a larger serie resistance in the vertical direction (as proofed also by the I-V measurements reported in [9]), it is easier for the current to spread in the lateral directions. As a result it is possible to minimize the possibility of limited ares of the junction suffering large currents, improving this way the ESD characteristics

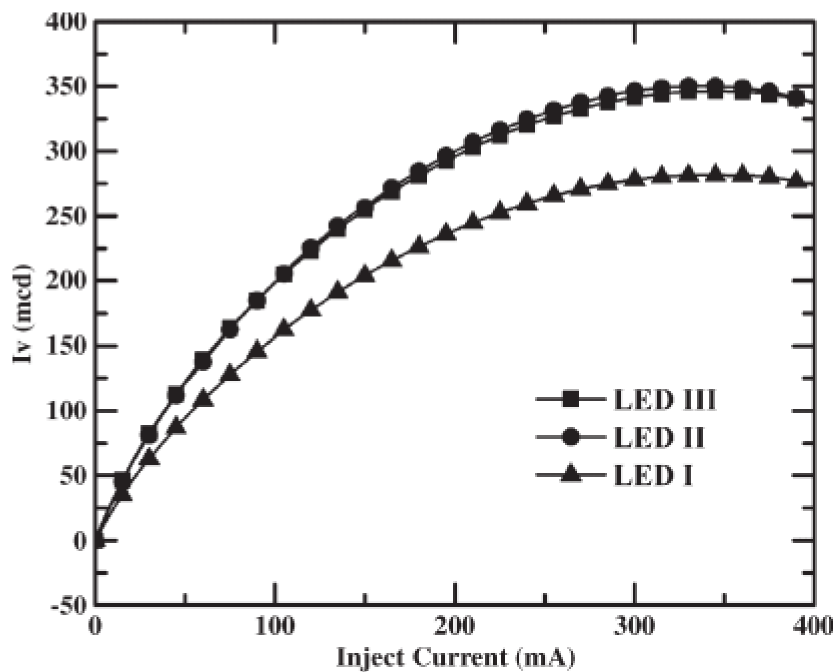


Figure 4.11: *L–I characteristics measured from the three fabricated LEDs [9].*

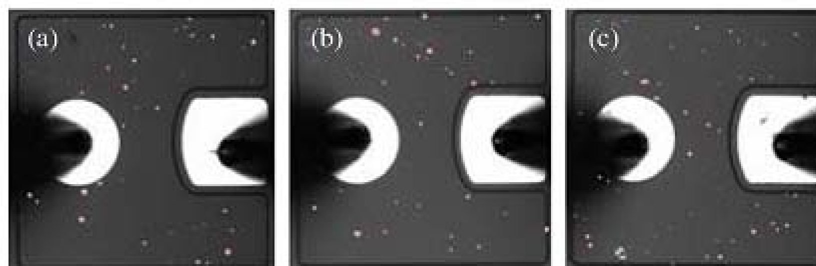


Figure 4.12: *EMMI images measured from (a) LED I, (b) LED II, and (c) LED III [9].*

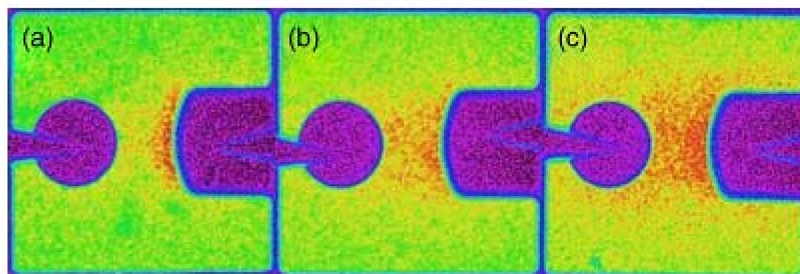


Figure 4.13: *Output power mappings for (a) LED I, (b) LED II, and (c) LED III [9].*

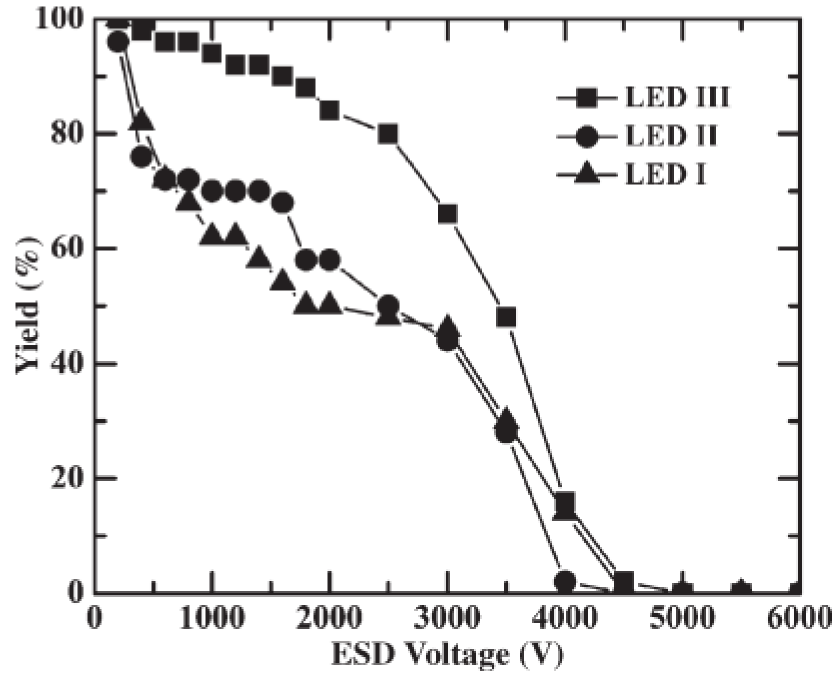


Figure 4.14: *ESD characteristics measured from the three fabricated LEDs of [9].*

of GaN-based LEDs .

Another interesting study on the parameters that affect the ESD robustness of LEDs is [10]. In this article, the electrostatic discharge properties of the InGaN-light emitting diodes, were investigated in terms of the internal capacitance of the devices. The LEDs submitted to the stresses were all grown on sapphire and with a structure made of a 30 nm low temperature buffer layer, a 2 μm unintentionally doped (un-doped) GaN layer, a 2 μm n-type layer composed of the multiple stack layers of highly Si doped GaN layer ($n \approx 2 \times 10^{19}$ cm^{-3}) and undoped GaN layer, 0.2 μm undoped GaN layer (L1), 10nm n-GaN (L2), InGaN well: 20 Å/GaN barrier: 80 Å multi-quantum wells MQWs active layer, and a 200 nm p-GaN ($Mg \approx 4 \times 10^{19} cm^{-3}$). Two typologies of devices with different silicon doping concentrations of L2 were grown, $3 \times 10^{18} cm^{-3}$ (S1), and 2×10^{19} cm^{-3}(S2) respectively.

These samples were submitted to HBM-ESD pulses and the voltage change at the low forward current (0.1 μA) was measured using a parameter analyzer. If the voltage at 0.1 μA dropped below 2.10 V (typical value≈2.25 V) the chip was considered to have been damaged by the ESD pulse. To yield reliable results the experiments were repeated more than 30 times.

The experimental data produced by this investigation, shown in Fig. (4.15) and Fig. (4.16), revealed that, while the average ESD pass yield at 500 V of S1 ($n_{L2} \approx 3 \times 10^{18} cm^{-3}$) was just between the 20 and 30%, S2 ($n_{L2} \approx 2 \times 10^{19} cm^{-3}$) was much more robust, having a pass yield up to 94%.

To investigate the reason for this higher robustness, the authors performed a C-V characterization of the LEDs at 1 MHz. The curves obtained for the two types of devices showed different results due to the diverse silicon doping level in L2. In particular, the capacitance of S1 had a sudden drop between -5 and -7 V.

To better understand the meaning of this result, the authors also analyzed the equivalent electronic circuit model for the InGaN-LED connected to the HBM-ESD simulator, described in Fig.

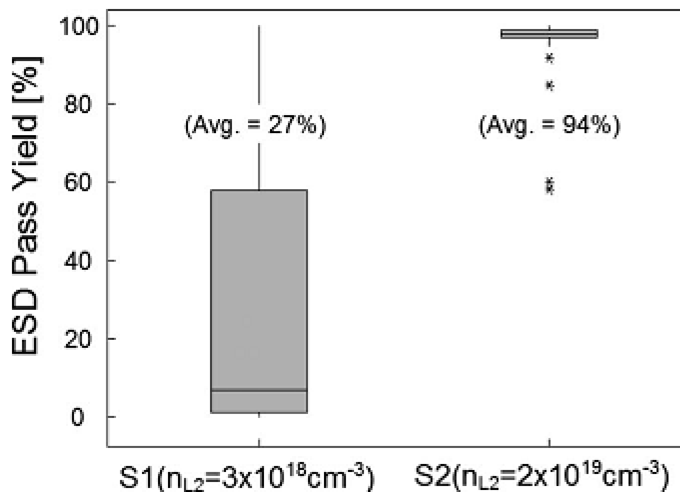


Figure 4.15: *Summary of the ESD pass yield of S1 ($n_{L2} = 3 \times 10^{18} cm^{-3}$) and S2 ($n_{L2} = 2 \times 10^{19} cm^{-3}$) of work [10].*

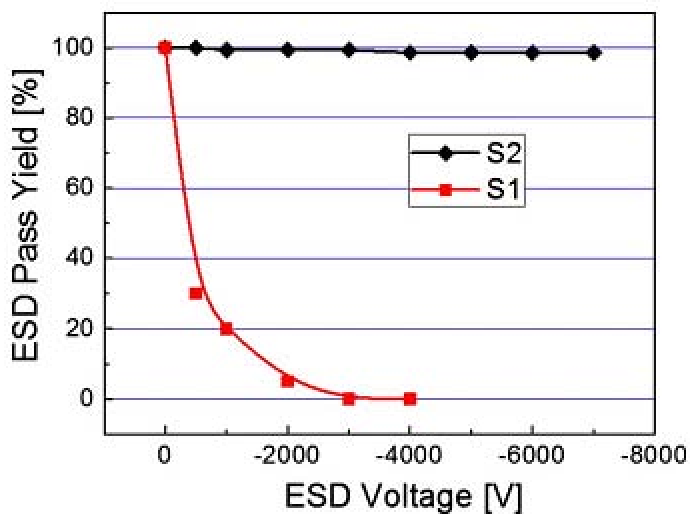


Figure 4.16: *Article [10]. HBM-ESD pass yield of S1 and S2 as a function of applied ESD voltage.*

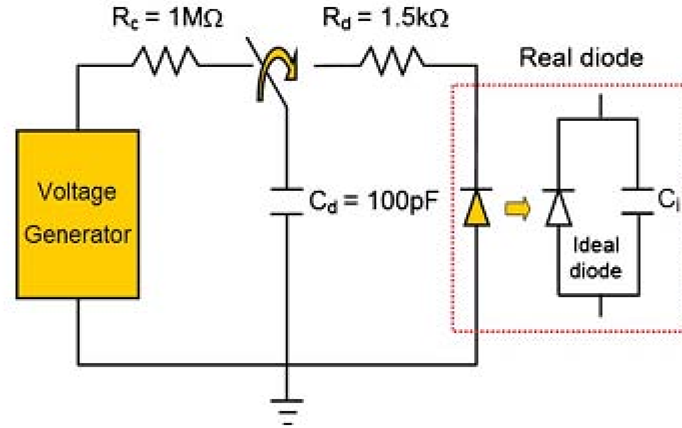


Figure 4.17: *Simplified equivalent electronic circuit for the InGaN-LED connected to the HBM-ESD simulator Rc: charging resistor, Cd: discharging capacitor, Rd: discharging resistor, Ci : internal capacitance [10].*

(4.17). The InGaN-LED can be represented by the parallel of an ideal diode and a capacitor representing the internal capacitance of the device C_i. Therefore, the total capacitance C_t Ct is given by the parallel of C_i and C_d, the discharge capacitance of the HBM-ESD simulator. Thus they found out that, because the ESD energy dissipation in the LED is inversely proportional to C_t, the S2 with high capacitance would be relatively insusceptible to the ESD shock. In fact, as shown in Fig. (4.16), its high pass yield is maintained up to 7000 V. They could therefore deduce that the internal capacitance of the diode has a major role in defining the ESD robustness properties of a LED. We can thus improve them increasing this parameter by changing the device structure (and/or the layers thickness) properly.

The importance of the internal capacitance of a LED is confirmed also by [11]. The authors of this experimental investigation submitted to ESD test three types of LEDs with the same structure, doping and growth parameters, but a different undoped GaN layer thickness. At the beginning the reverse pulse amplitude values was 1kV HBM, and it was successively increased up to 7kV. The I-V characteristics of the devices were measured before and after each stress and, if the measured current had varied by more than 30% from its original value, the chip was considered to be broken. The results of this investigation showed that, under a reverse ESD pulse voltage of 5.5 kV, the survival rate of the LEDs with an undoped GaN layer thickness of 1.5, 4 and 6 μm were 75, 65 and 55% respectively.

In order to find out the possible reasons for this differences, the authors also performed C-V measurements at 1 MHz on the samples. The curve obtained showed that the LED with a thinner undoped GaN layer had a higher internal capacitance. The authors could therefore confirm what stated in [10] about the effect of the internal capacitance on the LEDs ESD properties. On the other hand the results also showed that in this case there is a trade-off between ESD robustness and optical properties, in fact increasing the undoped layer thickness made the optical properties improve while giving poorer ESD performance.

4.2 CONCLUSIONS

The research work done until now clearly shows that, to achieve a high robustness towards reverse-bias ESDs, it is fundamental to reduce defectivity by improving growth quality and by adopting materials with lower lattice mismatch (like SiC). The fabrication process obviously plays a major role in defining the ESD robustness of a LED, thus there is a certain numbers of parameter that can strongly influence it, such as the LEDs layers structure and growth-temperature (characteristics that can all be connected to the material defectiveness). Some papers also show that improving the current distribution is another key issue to make LEDS more resistant to ESDs, and this can be obtained by adopting proper device layouts and structures (for example inserting a current spreading layer in the device). Finally also the internal capacitance of the devices can have a strong influence, and the experimental results suggest that a better ESD performance can be obtained increasing this parameter, leading to the same consideration as before (a change in the structure).

Anyway, despite the many useful and interesting informations given by the previously cited papers and summarized in the previous lines, it is important to notice that most of the work done worldwide until now was focused on the robustness of single LEDs. Furthermore in most of the cases a HBM model was used, not giving the possibility of observing the waveforms of the voltage and the current on the devices. A high number of studies has been also carried out on LEDs with protection structures, not focusing on the device inner reliability. A study on the robustness of LED modules is therefore still missing and potentially very interesting.

Chapter 5

MEASUREMENT SETUP AND EXPERIMENTAL DETAILS

5.1 TRANSMISSION LINE PULSE (TLP) TECHNIQUE

The ESD qualification tests shown in Chapter 3 yield only failure thresholds. Often they do not give a sufficiently detailed knowledge of the DUT behaviour to allow for example the optimization of the protection structures. In view of shrinking safety margins for most advanced technologies and applications, measuring the exact parameters in the ESD-relevant regime is of utmost importance. Furthermore, DC-characterization causes strong self-heating for higher currents and does not address the transient behavior. As a consequence pulsed characterization techniques are necessary in addition to the DC-characterization. These techniques measure the dynamic and the quasi-static device behavior of protection elements and sensitive elements for ESD-relevant times. This explains why the *Transmission line pulse* technique became a very important tool for testing and ESD protection structures development. Among the trademark features of this technique, we find the very good repeatability of the stress-tests both on the same and on different systems, the possibility of acquiring the waveforms of the voltage and current on the DUT in addition to the capability of giving more complete and accurate results.

Because of these characteristics and of the well-defined physics exploited by this system, TLP has even a high potential to replace traditional methods for the qualification of products.

5.1.1 FUNDAMENTALS AND IMPLEMENTATIONS

The TLP stress test system can generate rectangular pulses of selectable duration and amplitude by charging the distributed capacitance of a transmission line (TL), that will be consequently discharged on the DUT. This system is known for the possibility of plotting the quasi-static IV-characteristic in combination with the evolution of the leakage current as the amplitude of the square pulses increases in steps. The quasi-static values for the voltage and the current on the DUT are be obtained by means of averaging a certain region in the second half of the transient waveforms, at a time when most of the oscillations caused by the parasitic capacitance and inductance of the TLP setup should have settled. In the following we will give a brief overview

of the theoretical principle on which the TLP system is based, and we will describe its different implementations.

A transmission line is a waveguide with a characteristic impedance Z_0 that only depends on the material and the geometry of the conductors and the dielectric isolating them. The distributed capacitance and inductance are expressed in F/m and H/m. For negligible losses the electric and the magnetic field can be considered transversal to the direction of propagation. If a pulse travels along a transmission line, any discontinuity of the impedance$Z(x) = Z_0$ causes a partial reflection of the energy of the incident pulse. The reflection is of the same polarity as the incident pulse if the impedance difference $Z(x)-Z(x-1)$ is positive and of opposite polarity else. This effect is used for the characterization of unknown devices in the time domain reflectometer but must be minimized in the rest of the system.

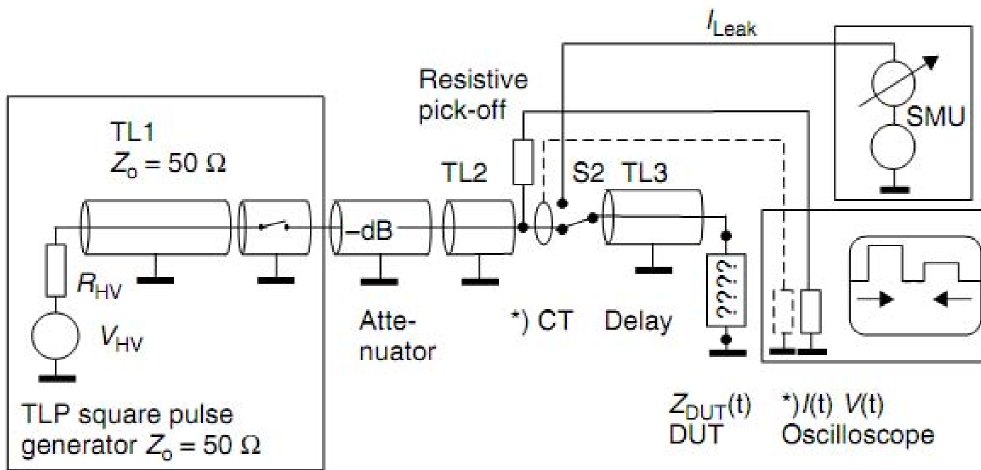


Figure 5.1: *Time domain reflectometer TLP.*

In Fig. (5.1) it is possible to see the structure of one of the possible TLP system implementations. A high-voltage source is used to charge the distributed capacitance of the transmission line TL1 via a high-ohmic resistor while the coaxial switch S1 is open. After the switch closes, the discharge of such a transmission line (TL1) into a resistive load or into TL2 produces a square pulse. The duration of the square pulse is equal to the length of the charged line divided by the velocity the signal "switch closed" propagates from the switch to the high-ohmic end of this line and back to the switch. 10m of the typical RG58 transmission line with a propagation velocity of 20 cm/ns generate a 100-ns wide pulse. The amplitude of the voltage pulse V is determined by the precharge voltage V_0 and the impedances of the source Z_S and the load Z_L.

$$V = V_0 \frac{Z_L}{Z_L + Z_S}$$

Deviations from the ideal square shape of the pulse result from resistive and dielectric losses that are frequency-dependent as well as from variations in the impedance along the line through the whole system. Therefore, it is mandatory to employ cables and components that are well matched, as short as necessary, and with low losses throughout the whole system. However, a dedicated long transmission line may be employed to tailor the rise time in order to comply with HBM or MM.

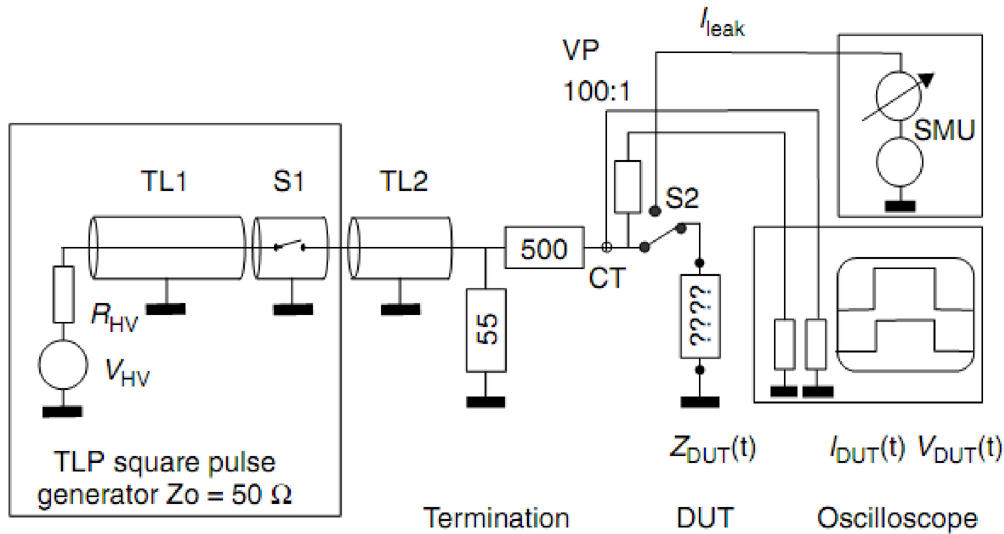


Figure 5.2: *Current Source TLP* $Z_S = 500\Omega$.

The most critical element of the TLP-system is the relay switch. Implementations with a Reed relay surrounded by a metal sleeve or cylinder are commonly in use, although with standard dimensions of commercially available Reed relays the impedance is in the order of 60Ω. At least, for a significant pulse duration, for example, 100 ns, the resulting degradation of the leading corner of the pulse top and after the falling edge is acceptable. Another issue is the repeatability of the switching over the full voltage range. A low series resistance by means of a metallic contact should be established instantaneously and maintained for the full duration of the pulse and possible reflections. Otherwise, a lower amplitude with a trailing pulse of the same polarity or even steps on the top of the pulse can be found. Mechanical contact bouncing is not an issue as it takes place in ms. Obviously, the shorter the pulses become, the more emphasis needs to be put on the impedance of the signal path. Only few commercial coaxial components are explicitly rated for high voltages. Thus, it is a matter a certain amount of time, experience and trials are required to find the most suitable relays, attenuators, and other components.

In principle, the different TLP systems can be seen as a modular combination of impedance controlled RF components. The equipment is controlled by a software that also extracts the actual current through the device $I_{DUT}\left(t\right)$ and the voltage across it $V_{DUT}\left(t\right)$, and that derives the various parameters from these measured data. Necessary equipment are the controller, the high voltage source, the oscilloscope and a source measuring unit for leakage measurement and for optional additional voltage bias of the DUT. itself. The main practical implementations of a TLP-system will be discussed in the following paragraphs.

5.1.2 CURRENT SOURCE TLP

Fig (5.2) shows the Current Source TLP, sometimes referred to as TLP500 and mainly used to simulate HBM-stress by means of a 100 ns wide pulse. It is characterized by the termination resistor and the source resistor that forces the current trough a low ohmic DUT. Voltage and current are measured independently as close as possible to the DUT and this makes the method rather tolerant to pulse variations. Additional switches disconnect the DUT from the stress

circuit and connect it to the DC-parameter analyzer. High parasitic elements at the DUT slow the achievable dV/dt and increase the probability for ringing. The matched termination eliminates multiple reflections between the open end of TL1 and the DUT. The oscilloscope and the probes determine the accuracy that is nearly independent from the load impedance Z_{DUT}. For low DUT voltages the voltage probe should be placed between the current probe and the DUT, otherwise all measured and applied DUT-voltages require correction for the dynamic impedance of 1 ohm in the ground path. The verification of the system can be done using low-inductance resistors.

5.1.3 TIME-DOMAIN REFLECTOMETER TLP (TDR-TLP)

The time-domain reflectometer-TLP (TDR-TLP), which has the advantage of maintaining the 50Ω impedance from the generator to the device with minimum parasitic elements and pulse distortion, is based on the high frequency propagation effects. In fact it employs the principle, that if an incident square pulse reaches the DUT at the end of a transmission line, it is reflected depending on the impedance $Z_{DUT}(t)$ of the DUT relative to the impedance Z_0 of the transmission line according to the following equation:

$$V_{reflected}\left(t\right) = \frac{Z_{DUT}\left(t - t_{delay}\right) - Z_0}{Z_{DUT}\left(t - t_{delay}\right) - Z_0} \cdot V_{incident}\left(t - t_{delay}\right) \tag{5.1}$$

The Time Domain Reflectometer TLP, whose schematic is shown in Fig. (5.1), can be implemented in two different ways: with or without a current transformer CT in the signal path. The system with the current transformer uses an oscilloscope with two channels and measures voltage and current reflected from the DUT independently, with the accuracy provided by the probes and the oscilloscope after a calibration of the attenuation factors of the system. Alternatively, for a known impedance Z_0, the current I(t) can be calculated from the relation $i\left(t\right) = V_{incindent}\left(t\right)/Z_0$ for the incident pulse and $I\left(t\right) = -V_{reflected}\left(t\right)/Z_0$ for the reflected one. The transmission line TL3 between the resistive pick-off and the DUT delays the reflected pulse with respect to the incident one. Using Eq. 5.1 and 5.2 voltage $V_{DUT}(t)$ and current $V_{DUT}(t)$ at the DUT are calculated from the measured incident and reflected voltage pulse after a shift of the reflected pulse to the left by twice the one-way delay time t_{delay} and a correction for the attenuation of the resistive voltage pick-off and transmission lines.

$$V_{DUT}\left(t\right) = V_{incident}\left(t\right) + V_{reflected}\left(t - 2 \cdot t_{delay}\right) \tag{5.2}$$

$$I_{DUT}\left(t\right) = \frac{V_{incident}\left(t\right) - V_{reflected}\left(t - 2 \cdot t_{delay}\right)}{Z_0} \tag{5.3}$$

Some uncertainty results from numerical effects when the DUT impedance is close to an open or a short and from distortion on the delay line TL3 in the phase of transition. It is possible to improve the accuracy through a calibration to 0Ω and the usage of a resistor together with

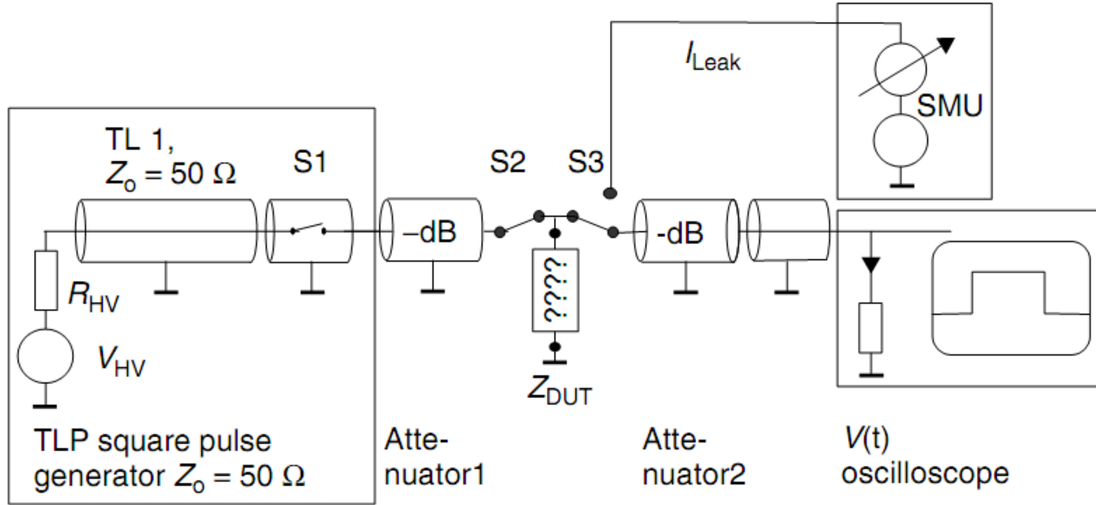


Figure 5.3: *Time domain transmission TLP.*

correction. If the reflected pulse is not completely separated from the incident pulse the incident pulse must be very repeatable and flat. An attenuator between the pulse generator and the DUT is recommended in order to reduce multiple stress caused by multiple reflections that depend on the DUT impedance. Other solutions employ a diode in series with a termination resistor in order to reduce reflections from low-impedance DUTs ($Z_{DUT} \leq Z_0$) at the open end of the transmission line. This termination, that may even be switched in order to generate bipolar pulses, depends on polarity and should not be used for the characterization of oxides. A coaxial relay in the delay line allows to connect a DC-parameter analyzer to the DUT.

5.1.4 TIME DOMAIN TRANSMISSION TLP (TDT-TLP)

The *Time Domain Transmission method*, shown in Fig. (5.3), avoids the uncertainties associated with the dispersion of the reflected pulse signal. However, it requires that first a reference voltage pulse $V_{chg}(t)$ is captured for every voltage step without the DUT in place. The voltage $V_{chg}(t)$ equals the measured voltage $V(t)$ times the attenuation factor a. After this first step the device is inserted in the fixture and the resulting pulses $V_{DUT}(t)$ are captured for the same precharge voltage levels. This method can also be implemented with minimum parasitic elements and in particular it can minimize distortion. It has to be proofed in advance that, while in conduction, the impedance of the relay is constant and repeatable, generating repeatable pulses in the full voltage range. An attenuator between the pulse source and the DUT reduces multiple reflections and stabilizes the source impedance Z_0. For the first pulse of a series of decaying reflections the following Equations 5.4 and 5.5 are used to calculate the current through the DUT for the directly measured voltage $V_{DUT}(t)$ attenuated to an amplitude safe for the oscilloscope. Two relays are necessary in order to isolate the DUT for leakage measurements between stress pulses.

$$Z_{DUT}(t) = \frac{V_{DUT}(t)}{V_{chg}(t) - V_{DUT}(t)} \cdot Z_0 \tag{5.4}$$

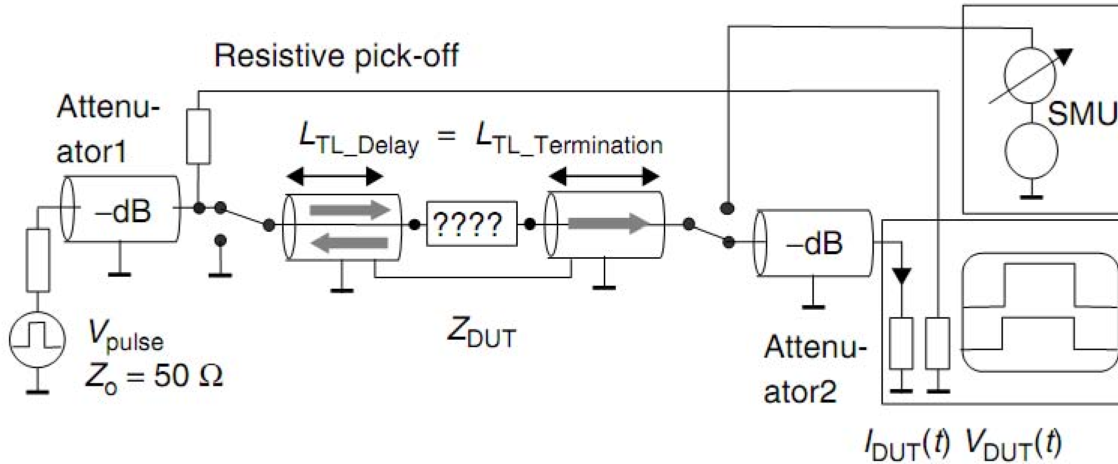


Figure 5.4: *Time domain transmission reflectometer*, *TDTR* or *"Embedded DUT™"*.

$$I_{DUT}(t) = \frac{V_{DUT}(t)}{Z_{DUT}(t)} \tag{5.5}$$

5.1.5 TIME-DOMAIN TRANSMISSION REFLECTOMETER TLP (TDTR-TLP)

Fig. (5.4) shows the *time domain transmission reflectometer*, *TDTR* or *"Embedded DUT™"* (Trademark of Oryx Instruments Inc. developed by Larry Edelson), that embeds the DUT between the center conductors of two transmission lines of equal length and requires a two-channel oscilloscope. The grounded outer conductors of the two lines are connected to each other. The equal length of the lines is necessary in order to align the transmitted and the reflected signal on the screen of the oscilloscope. The length of the delay and termination line should exceed the length of the pulse generating TL1 in order to separate the reflected from the incident pulse at the pick-off. Employing Equation 5.6, the voltage $V_{DUT}(t)$ is calculated from the reflected pulse considering the attenuation factor of the pick-off and the transmission lines. With Equation 5.7 the current $I_{DUT}(t)$ is calculated from the transmitted pulse voltage at the 50Ω input resistor of the oscilloscope. Both signals may need some additional attenuation. This system has a source impedance of 100Ω, as the DUT is in series with the 50Ω-line connected to the oscilloscope. Although even a short does not generate reflections of opposite polarity, using an attenuator between the pulse generator and the pick-off is recommended. In order to test the leakage, additional coaxial relays may be necessary for DC insulation. The calibration of the system is done at least with a short. With the symmetrical outline of the controlled impedance paths, this TLP method has a high potential for an implementation in an automated multiplying TLP-test system.

$$V_{DUT}(t) = a \cdot 2 \cdot V_{refl}(t) \tag{5.6}$$

$$I_{DUT}(t) = \frac{V(t)}{Z_0} \tag{5.7}$$

5.1.6 FINAL CONSIDERATIONS ON TLP STRESS-SYSTEMS STANDARDIZATION AND OPTIMIZATION

The possibility of generating repeatable stress pulses in combination with the measurement of current and voltage, should in principle be sufficient for the relative comparison of two protection elements. Anyway, looking at the HBM qualification test of the product, correlation between TLP and the standard test methods employed for qualification became a concern for the worth of the TLP procedure. With the extended application of the TLP method also the results obtained with different TLP testers should be comparable. The development of a widely accepted TLP standard will significantly contribute to this comparability. TLP-pulses with a rise time in the order of 5 ns and a pulse duration of 100 ns are typically used, and they translate 0.66A into almost 1 kV HBM. Depending on the device and its electrical and physical failure signature, a more detailed analysis may be necessary.

A higher source impedance of the TLP system increases the resolution but additional parasitics associated with the high impedance setup affect the initial dV/dt at low currents. The interconnect between the TLP-generator and both probe needles, must be kept to a minimum of few centimeters and also be in place for calibration (it has in fact no controlled impedance and may affect the waveform). Whether the pulse is injected via two symmetrical terminals employing a balun or using one coaxial line may have an influence on the device behavior. Anyway, if coaxial RF probes are employed to contact the DUT and the substrate is always connected to the grounded shield of the probe, this effect should be negligible.

Depending on the setup and the device to be stressed, electromagnetic interference between the stress and control terminals (for example the gate terminal) of the DUT can become an issue. For each TLP type, the appropriate calibration technique must be applied in order to gain the correct attenuation factors of the system, including the resistance of the probe needles in the case of on wafer-testing. Another correlation issue is the elimination or attenuation of multiple reflections, which may cause additional stress to the DUT depending on the tested structure.

During the test, that has always to be preceded by a calibration or verification phase, the leakage current should be measured before and after each pulse, carefully choosing the reverse bias voltage. In fact it has to be adequate to make changes well visible while avoiding to cause additional stress during the leakage measurement. The application of one pulse per voltage step should be sufficient. In the case of on-wafer devices analysis, it is recommended to test at least three structures, preferably from different positions on the wafer to take into account eventual technological variations that can have a strong effect on the ESD characteristics. The rise time and the duration of the pulses can be varied either to study rise time or self-heating effects until failure occurs. Rise-time filters may also be inserted into the transmission line with this purpose.

Finally, the control program of a TLP-tester should provide excellent handling and analysis of significantly more data in comparison with HBM. It should also be highly automated for routine characterization or process monitoring and must be very flexible for the expert user. As TLP has a good chance to become accepted for the product qualification, test procedures equivalent to the HBM qualification are expected to emerge in the future.

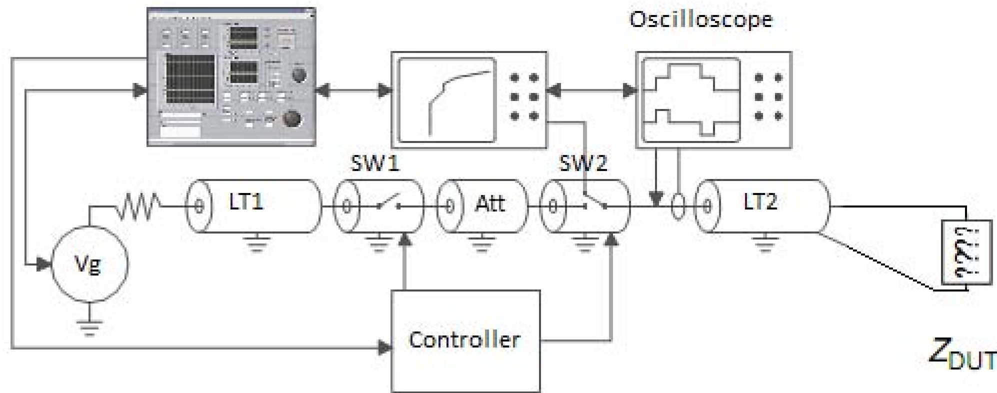


Figure 5.5: *Schematic of the implemented TDR-TLP.*

Figure 5.6: *Example of a Stanford Research Systems ps serie high voltage generator.*

5.2 MEASUREMENT SETUP

For our stress-system practical implementation, we chose a time domain reflectometer-TLP, whose schematic can be seen in Fig. (5.5). In the rest of this chapter the characteristics instruments used for this implementation will be shown. Furthermore the other measurement systems employed in the experimental investigation and the LEDs tested will also be shown.

5.2.1 STANFORD RESEARCH SYSTEMS PS350/5000V HIGH VOLTAGE GENERATOR

To generate the high voltage needed to charge the TLP transmission line, we used a PS350 high voltage generator. This device can generate voltages up to $\pm 5000V$ with a maximum output current of 5mA. The voltage set accuracy is 0,001% plus 0,05% of full scale, and the voltage resolution is 1V. Other interesting parameters are the rms output ripple, that is the 0,002% of full scale, the current resolution ($1\ \mu A$) and the temperature drift, which is 50ppm/°C for temperatures between 10 and 40 °C.

In our measurement setup this instrument was controlled via the GPIB interface, using a labview program.

5.2.2 TEXTRONIK TDS680B OSCILLOSCOPE

To acquire the pulse waveforms we employed a Tektronik TDS680B digital oscillocsope. This device, which is a four channels instrument with an 8 bits vertical resolution, was connected to the transmission line through a current and an high voltage probe to avoid pulse induced damage. The time window of the acquisition was set at 200 ns, while the vertical axis scale was set automatically in every discharge event exploiting the auto range function. As all the other instruments of the system even this one was automatically controlled through a labview program via a GPIB interface. This oscilloscope was found to be suitable for the TLP system implementation especially because of its bandwidth of 1 GHz, a high frequency value fundamental to acquire the very fast pulses generated.

5.2.3 KEITHLEY 2612 SOURCE METER

To measure the LEDs leakage current and I-V curves we employed a sourcemeter, a Keithley 2612. Sourcemeters are instruments that can be used as stand-alone current or voltage sources and stand-alone voltmeters or ammeters, but they also allow to supply current to a device under test while simultaneously measuring the voltage drop across it (or vice versa), characteristics that we widely exploited in our tests.

Controlling the sourcemeter via GPIB interface using a labview program, allowed us to measure the leakage after every TLP pulse, applying a voltage on the LED and measuring the current flowing through it. Furthermore we also exploited this instrument to measure the I-V characteristic of each single LED after a certain number of pulses; this measure was done by applying a pulsed voltage (obtained turning the chosen channel on and off repeatedly) from -10 to 5V, with an integration time low enough to avoid the self-heating of the LED and the modification of its I-V curve, but also high enough to reduce the noise to acceptable levels, and measuring the current flowing through the device. As a consequence we are interested in knowing the characteristics of the Keithley 2612 as a voltage source and as a current measure system.

Reading the information shown in Keithley's application notes and datasheets we see that, regarding the voltage sourcing, this instrument has a programming resolution that varies with the chosen voltage range, and goes from $5\mu V$ in the case of a 200mV range, to 5mV when we choose a 200V range. Another important parameter is its accuracy, described in Fig. (5.7). Finally the set time in the 20V range is typically lower than $110\mu s$ and for the 200mV and 2V range it is lower than $50\mu s$.

As a current meter, the accuracy is given by Fig. (5.8). Notes 6 specifies to de-rate accuracy by $V_{out}/2\text{x}10^{11}$ when operating between 18 and 28 °C, and by $V_{out}/2\text{x}10^{11}+$ (0,15*$V_{out}/2\text{x}10^{11}$) per °C when operating at temperature outside this range. Note 7 suggests to de-rate accuracy specifications for NPLC setting <1 by increasing error term, adding the appropriate percentage of range term using the table in Fig.(5.9). Another interesting data is the sensing input impedance value, that is higher than $10G\Omega$.

This data are valid for operation between 18 and 28 °C, when the relative humidity is lower than 70%, at normal speed (1 NPLC), after tow hours warm-up, with A/D auto-zero enabled, with remote sense operation or properly zeroed local sense operation and within a year from calibration.

Range	Programming Resolution	Accuracy (1 Year) 23°C ±5°C ±(% rdg. + volts)	Noise (Peak-Peak) 0.1Hz–10Hz
200.000 mV	5 µV	0.02% + 375 µV	20 µV
2.00000 V	50 µV	0.02% + 600 µV	50 µV
20.0000 V	500 µV	0.02% + 5 mV	300 µV
200.000 V	5 mV	0.02% + 50 mV	2 mV

Figure 5.7: *Keithley 2612 voltage source specifications.*

Range	Display Resolution[3]	Voltage Burden[2]	Accuracy (1 Year) 23°C ±5°C ±(% rdg. + amps)
100.000 nA	1 pA	<1 mV	0.05 % + 100 pA
1.00000 µA	10 pA	<1 mV	0.025% + 500 pA
10.0000 µA	100 pA	<1 mV	0.025% + 1.5 nA
100.000 µA	1 nA	<1 mV	0.02 % + 25 nA
1.00000 mA	10 nA	<1 mV	0.02 % + 200 nA
10.0000 mA	100 nA	<1 mV	0.02 % + 2.5 µA
100.000 mA	1 µA	<1 mV	0.02 % + 20 µA
1.00000 A	10 µA	<1 mV	0.03 % + 1.5 mA
1.50000 A	10 µA	<1 mV	0.05 % + 3.5 mA
10.0000 A[5]	100 µA	<1 mV	0.4 % + 25 mA

TEMPERATURE COEFFICIENT (0°–18°C & 28°–50°C): ±(0.15 × accuracy specfication)/°C.

Figure 5.8: *Current measurement accuracy.*

NPLC Setting	200mV Range	2V–200V Ranges	100nA Range	1µA–100mA Ranges	1A–1.5A Ranges
0.1	0.01%	0.01%	0.01%	0.01%	0.01%
0.01	0.08%	0.07%	0.1 %	0.05%	0.05%
0.001	0.8 %	0.6 %	1 %	0.5 %	1.1 %

Figure 5.9: *Coefficients for Keitley 2612 current sensing accuracy de-rating.*

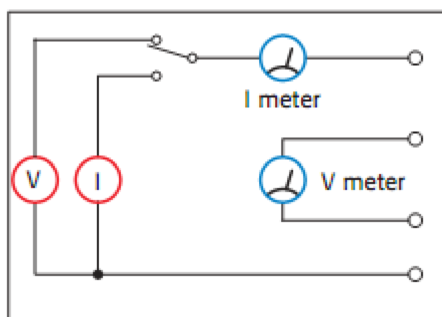


Figure 5.10: *Sourcemeter basic topology.*

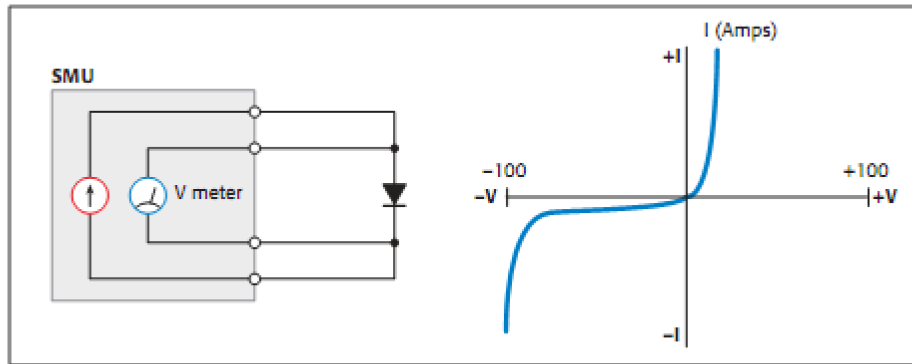


Figure 5.11: *Typical diode characterization using a sourcemeter.*

Figure 5.12: *Keithley 2612 source meter.*

5.2.3.1 HP 3488A SWITCH/CONTROL UNIT

Another instrument that was used is the HP 3488A switch/control unit. This is a very simple device, constituted of a matrix of relays that allow to dynamically change the measurement setup by changing the interconnections between the single elements, while the measure is running. This instrument was exploited to measure the leakage current and I-V curve of each LED of the modules singularly. The usage of this device was needed, because otherwise we couldn't have had any information about the single LEDs and the failure order, but it caused a problem that could not be solved but just limited. The interconnection of the relays in parallel to the LEDs in fact changed the impedance seen by the pulse, modifying its waveforms. In fact because of the high frequencies that characterize the ESD phenomena, even an open circuit in parallel can change the impedance seen on the line. This problem was limited by reducing the length of the cables used to connect the single LEDs and the switching matrix.

This instrument was controlled via GPIB interface through a labview program.

5.2.4 ANDOR LUCA

In the final stage of the experimental work an optical investigation was carried on together with the electrical one. To observe the light emission during the ESD event, an Andor Luca S camera was employed This instrument is an EM CCD that through the electron multiplying mechanism, allows to detect even low-intensity emission, providing single photon detection sensitivity and high quantum efficiency (52% max). The pixel size is 10x10 μm, giving high resolution, and the image area is 6.58x4.96 mm.

The camera was mounted on a Mitutoyo microscope, which allowed to take accurate photos of the LED chip, with a sufficiently high resolution to understand in which part of the surface the emission was located.

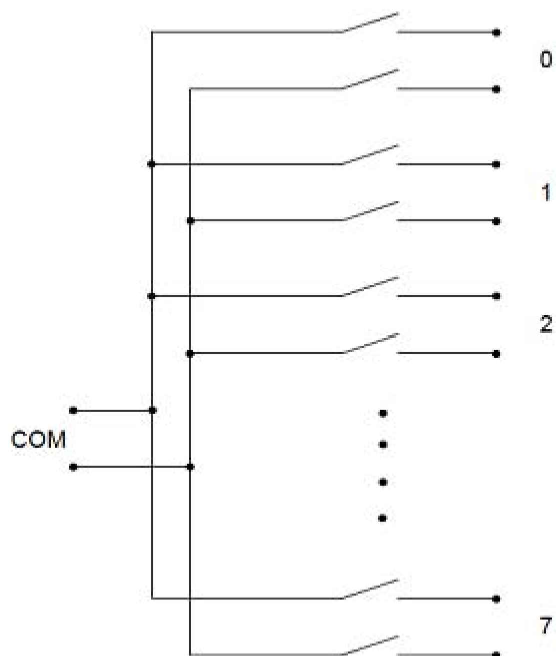


Figure 5.13: *HP 3488A switch/control unit scheme*

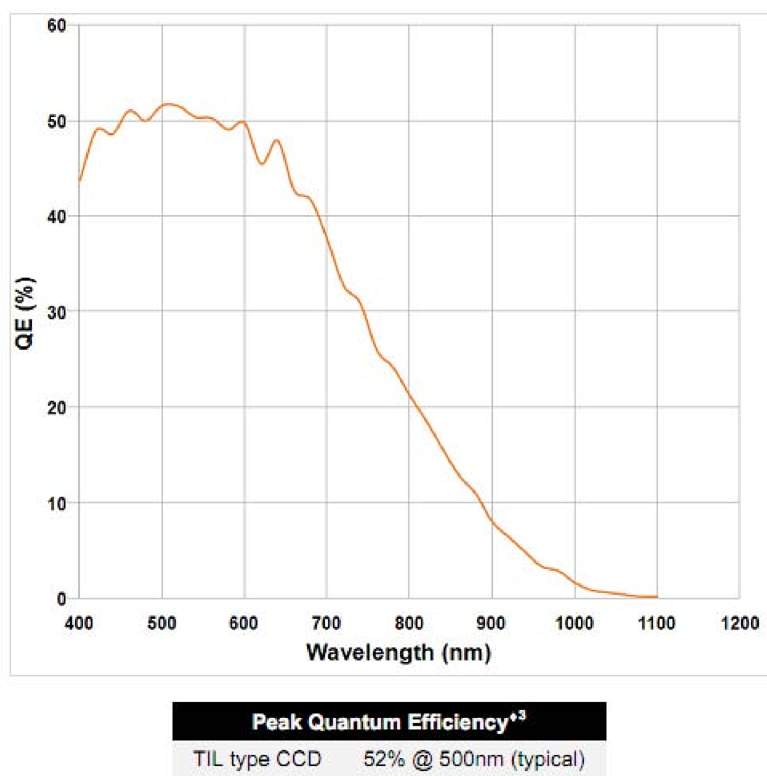


Figure 5.14: *Andor Luca quantum efficiency as a function of wavelength.*

Figure 5.15: *Andor Luca image.*

Figure 5.16: *Optikam pro 3.*

5.2.5 OPTIKAM PRO3

In some cases, it is possible that the device degradation turns into a visible damage on the chip surface. To determine whether this was our case or not and to understand if there were visible differences in the three types of LEDs (green, red and blue), we employed a camera, the Optikam pro 3, mounted on the Mitutoyo microscope. This device has a 3.2 Mpixel resolution (2048 x 1536) and allowed us to observe the LEDs chip before and after the stress, with the results that will be shown in the next chapters.

5.3 ANALYZED DEVICES

This analysis was carried out on commercially available devices belonging to the Topled®family, produced by Osram. We considered samples of three different colours: blue, green and red.

Figure 5.17: *Osram Topled®*

The blue LED analyzed is the Topled® LB T673, an InGaN based device with a typical emission wavelength of 471 nm. Reading the datasheet we can notice that it has a declared ESD-withstand voltage up to 2 kV according to JESD22-A114-F. The operating temperature range goes from -40 to 100 °C, and the maximum ratings are, for the junction temperature 110 °C, for the forward current 20 mA and 200 mA for the surge current (with a duration lower than 10 μs, at 25 °C and with a duty cycle of 0,005). Other characteristics are the forward voltage (measured during a current pulse of typical 8 ms, with an internal reproducibility of +/- 0,05 V and an expanded uncertainty of +/- 0,1 V), whose values range from a minimum of 2.70 and a maximum of 3,70V, while the average is 3.10V , and the reverse current I_R measured at $V_{DUT} = -5V$, whose typical reported value is $0.01\mu A$ and the maximum $10\mu A$.

In our case, we are especially interested in the declared robustness towards current pulses, some interesting informations about this are given in Fig. (5.18). The green LEDs were Osram Topled® LG T67K. Some of the characteristics of these devices reported in the datasheet are the same of the blue LEDs. In fact their operating temperature range goes from -40 to 100 °C, the maximum forward current is 20 mA and the surge current can be 100 mA at maximum (with a duration lower than 10 μs, at 25 °C and with a duty cycle of 0.005). Furthermore the ESD-withstand voltage can reach 2 kV according to JESD22-A114-D. Despite these similarities, some other parameters are different, for example the maximum junction temperature is 125 °C. The forward voltage is different too, and its values vary from a minimum of 1.7 and a maximum of 2.2V, with an average of 1.8 V. Another important difference is that the typical reverse current reported in the datasheet is measured at -12 V. Its typical and maximum values are 0.01 and 10 μA respectively. Also in this case in the datasheet is reported the permissible pulse handling capability, shown in Fig. (5.19).

The last type of LEDs analyzed was the super-red LS T67K Topled®. Reading the datasheet we can see that these devices are InGaAlP based, with a dominant wavelength of 630 nm and an ESD-withstand voltage up to 2kV, according to JESD22-A114-B. The maximum ratings are 125 °C for the junction temperature, 20 mA for the forward current and 100mA for the surge current (at 25°C, with a period lower than $10\mu s$ and a duty cycle of 0.005). The forward voltage (measured at I_F = 2 mA) is typically 1.8 V, but can vary between a minimum of 1.7 and a maximum of 2.2 V. The reverse current typical value (measured at $V_{DUT} = -12$ V) is 0.001 μA, while the maximum can be as high as $10\mu A$. The operating temperature range is the same as usual (-40/+100 °C).

Informations regarding the pulse handling capability are given in Fig. (5.19).

The LEDs characteristics that were reported previously are summarized in Table (5.1) and (5.2) together with some other interesting parameters, such as the thermal resistance, the optical

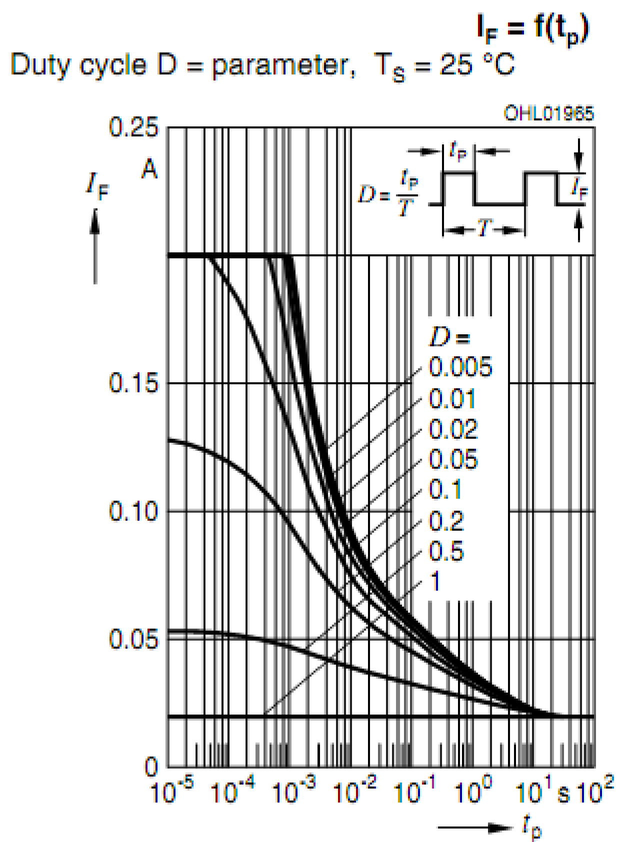


Figure 5.18: *Permissible pulse handling capability of blue Topled® devices.*

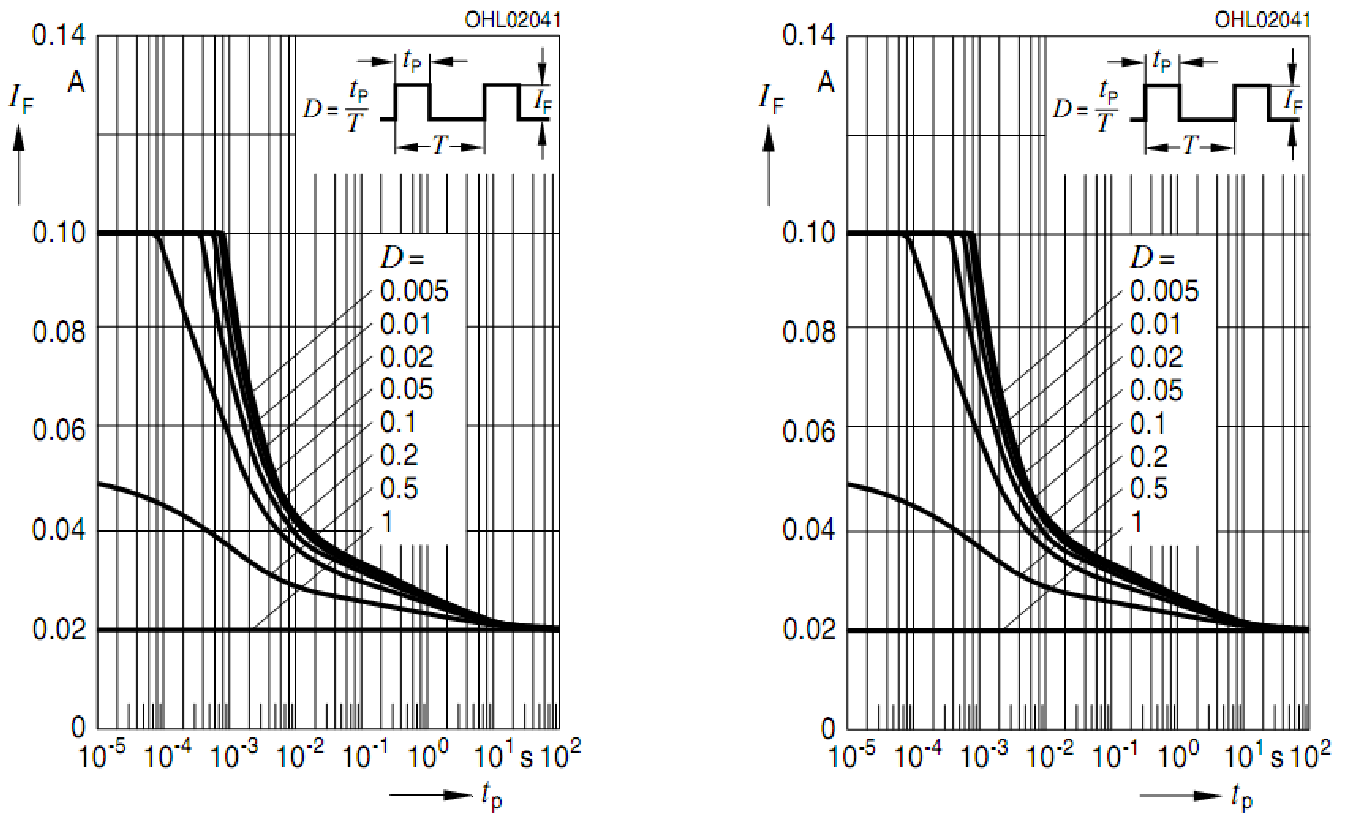


Figure 5.19: *Permissible pulse handling capability of the analyzed green Topled® devices at 25 (on the left) and 85 °C respectively.*

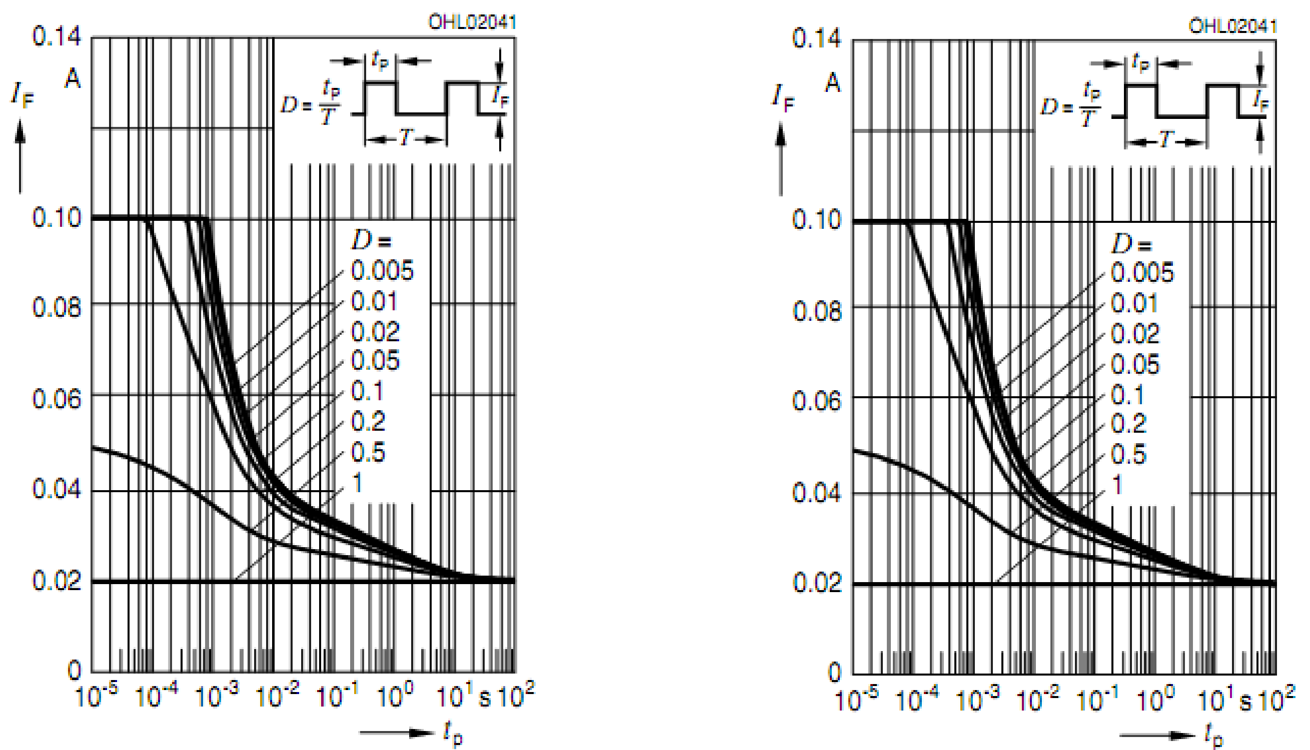


Figure 5.20: *Super red LS T67K LEDs permissible pulse handling capability as a function of duty cycle, specified at 25 °C (on the left) and 85°C respectively.*

Maximum Ratings	LB T673 blue LEDs	LG T67F green LEDs	LS T67K super red LEDs	Unit
$T_{JUNCTION}$	110	125	125	°C
Operating temperature range	-40...100	-40...100	-40...100	°C
Forward current ($T_A = 25$°C)	20	20	20	mA
Surge current (t $\leq$10μs; δ=0.005; T=25°C)	200	100	100	mA
Reverse voltage	5	12	12	V

Table 5.1: *Analyzed LEDs maximum ratings summary.*

efficiency and the spectral bandwidth.

Parameter	LB T673 blue LEDs	LG T67K green LEDs	LS T67K super red LEDs	Unit
Wavelength at peak emission (typ.)	466	572	643	nm
Dominant wavelength	465 (min.) 471(typ.) 477(max.)	570 -4/+5	630 ±6	nm
Spectral bandwidth at 50% $I_{rel\,max}$ (typ.)	25	22	16	nm
Forward voltage	(min.) 2.70 (typ.) 3.10 (max.) 3.70	(min.) 1.7 (typ.) 1.8 (max.) 2.2	(min.) 1.7 (typ.) 1.8	V
Reverse current (typ.) (max.)	(V_{dut}= - 5) 0.01 10	(V_{dut}=-12) 0.01 10	(V_{dut}=-12) 0.01 10	μA
Thermal resistance junction/ambient	400 (max.)	420 (max.)	420	K/W
Thermal resistance junction/solder point	180 (max.)	260 (max.)	260	K/W

Table 5.2: *Analyzed LEDs characteristics comparison.*

Chapter 6

SINGLE LEDs ANALYSIS

The first step of our experimental work was the ESD-stress testing of the single LEDs in order to get some useful information and eventually discover differences in the behaviour of the different types of devices. We exploited our TLP-system to apply negative biased pulses to the devices, starting from the minimum voltage possible (setting "V_{start}" parameter in our labview program to zero) and increasing the pulse amplitude with 3 volts steps. After each discharge we measured the leakage current at -5 V, and when its value became equal or higher than 100 μA for a certain number of measures, we considered the device failed and stopped the stress-test. This measurement was carried out on 4 samples for each type of LED. In the following the results obtained for each of the LEDs type will be shown and commented.

6.1 BLUE SAMPLES

In this paragraph we show the results of the experimental measurements carried out on the blue LEDs. The first curve we are interested in is the pulsed I-V. This characteristic is obtained by averaging the amplitude of the voltage and current pulse waveforms in an appropriate time window. The I-V curves of the four different tests are shown in Fig. (6.2) and as we can see, they seem to recall a diode I-V characteristic. These curves indeed are a reverse-biased diode I-V; we are in fact plotting the I-V characteristic of a reverse-bias pulse applied to LED devices.

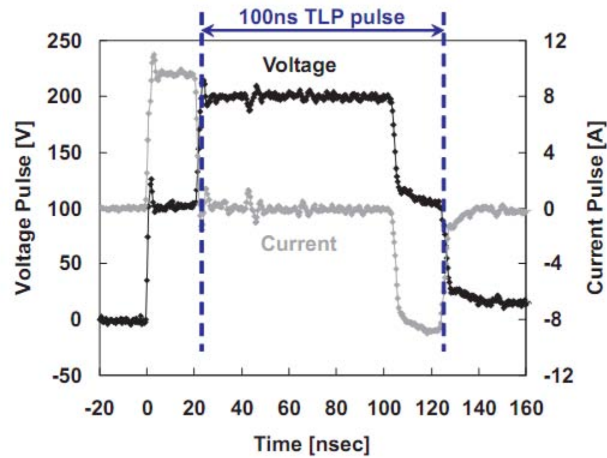


Figure 6.1: *Typical open circuit voltage and current waveforms of the 100ns TDR-TLP implemented.*

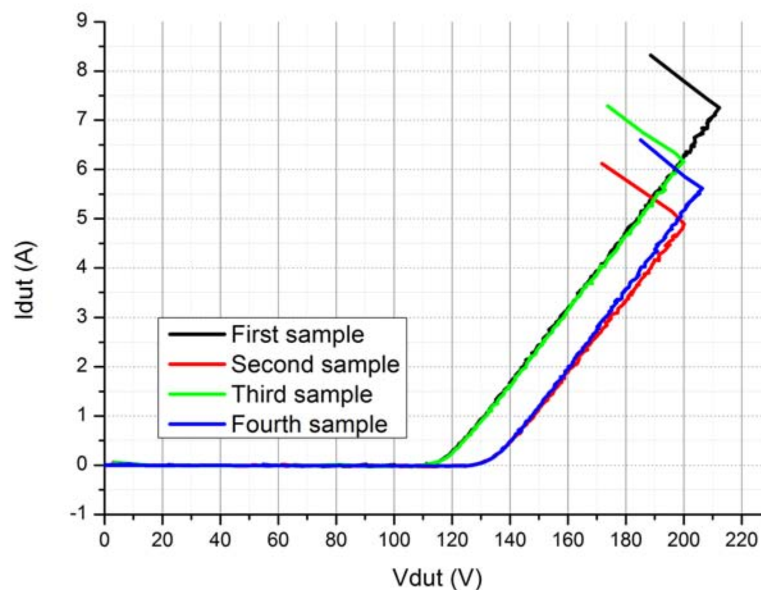


Figure 6.2: *Pulsed I-V characteristic of each of the four blue LEDs submitted to ESD-stress testing.*

Observing this image one can notice that the blue LEDs behaviour can be quite different depending on the specific sample. We can also notice that in the breakdown region the I-V characteristic is almost linear, suggesting that all the devices have a high serie resistance. Furthermore the breakdown voltage is not the same for all of the samples.

The I-V of the DUT was not the only characteristic evaluated. In fact, as previously explained, the leakage current after every stress was also measured. Combining this informations with the other data we collected, some very interesting curves can be obtained. For example in Fig. (6.3) it is possible to see the leakage current of the device as a function of V_{LINE}, the TLP transmission

line pre-charge value.

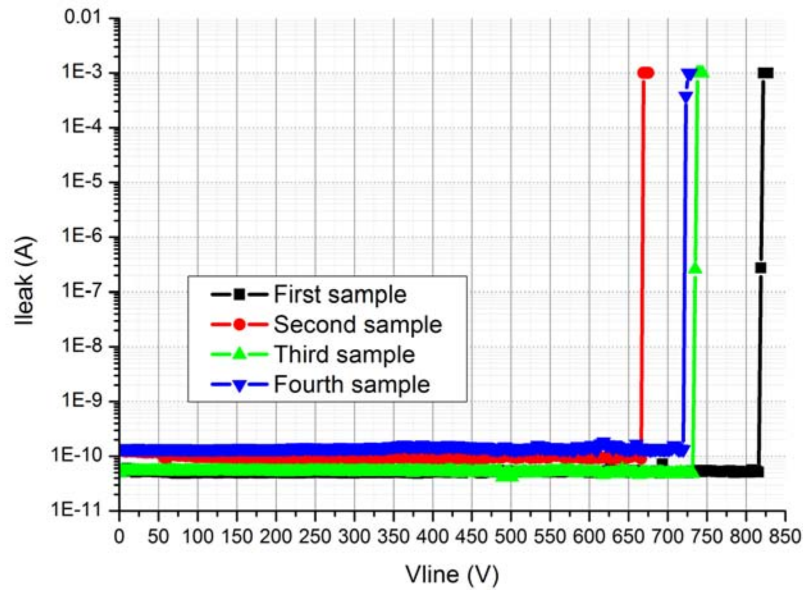


Figure 6.3: *The blue LEDs leakage current as a function of the pre-charge voltage.*

Despite the pre-charge voltage being a useful information, it is not the real voltage applied to the device under test. Thus it can be more interesting to express the leakage current as a function of V_{DUT}, obtaining the graph shown in Fig. (6.4).

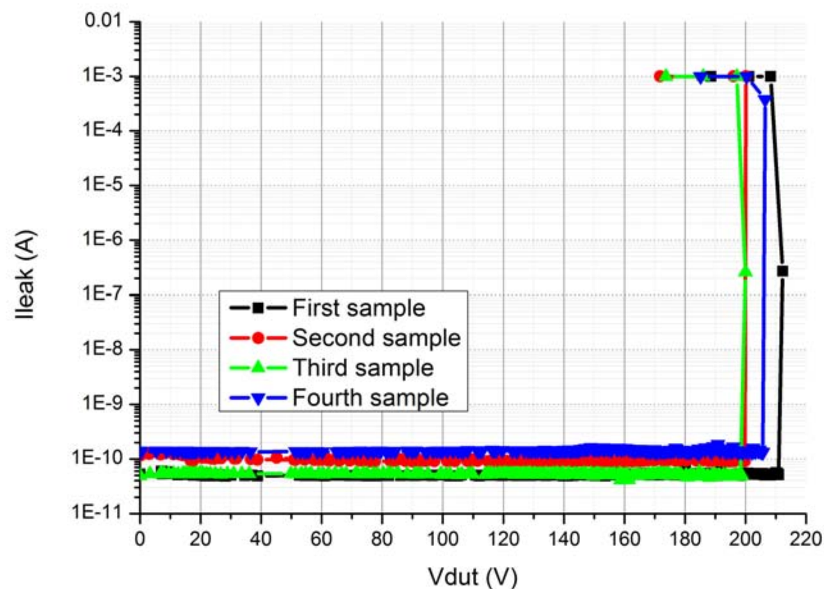


Figure 6.4: *Blue LEDs leakage current as a function V_{DUT}.*

Observing Fig. (6.3) it is interesting to notice that two of the tested LEDs were characterized by a higher leakage since the beginning. This is especially meaningful because these two LEDs also seem to be the first to fail, showing a poorer ESD performance. Even if the differences between the four samples behaviours are not significantly marked, the previous observation could suggest an important role of the leakage paths (and thus the material quality) in the ESD performance of the devices. Even if this suggestion does not seem to be confirmed by Fig. (6.4), we can see from Fig.(6.5) that the failure of samples 2 and 4 (the devices with higher leakage) takes place at lower values of current, confirming what is shown in Fig. (6.3).

Another very interesting thing one can notice, is that the degradation process seems to be catastrophic. In fact the leakage current remains stable and very low until the ESD that causes the failure (or the one before), when the leakage varies abruptly, sometimes even varying from the initial values to the compliance in just one step.

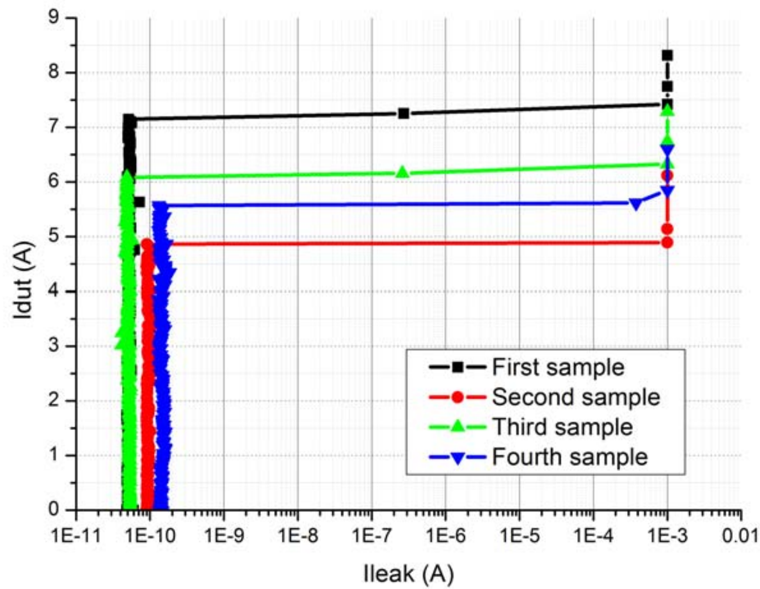


Figure 6.5: *Pulse current as a function of the DUT leakage current in the blue LEDs stress-tests.*

Analyzing the graph in Fig. (6.5) the variation of the current that flows on the DUT when the failure occurs does not seem very high. Anyway, as we will show in Chapter 7, ESD reverse current conduction takes place in just a small part of the devices, perhaps even a small current increase can cause a variation in the current density much higher than we may think.

The results obtained with the experimental work on the blue samples are summarized in Table (6.1). $V_{failure}$ and $I_{failure}$ are the voltage and the current of the pulse that causes the failure, $I_{pre-failure}$ and $V_{pre-failure}$ are the current and voltage of the one that comes before it.

	$V_{pre-failure}$ [V]	$V_{failure}$ [V]	$I_{pre-failure}$ [A]	$I_{failure}$[A]
sample1	212.24	208.29	7.25	7.42
sample2	199.79	200.11	4.86	4.89
sample3	199.98	197.13	6.16	6.33
sample4	205.68	206.41	5.57	5.62
mean	204.42	202.99	5.96	6.06
std. deviation	5.8823	5.2423	1.0166	1.0789

Table 6.1: *Blue LEDs behaviour statistical summary.*

6.2 GREEN SAMPLES

We applied the same procedure employed for the investigation on the blue LEDs also in case of the green samples. As done before, we can then begin our analysis observing the pulsed I-V characteristic, shown in Fig. (6.6).

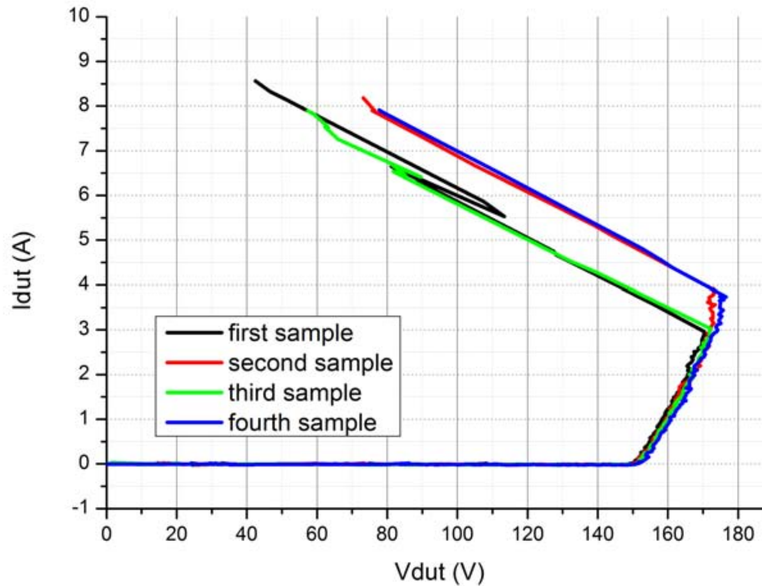


Figure 6.6: *Pulsed I-V characteristic of the green LEDs submitted to ESD-stress testing.*

Comparing these curves with the ones obtained in the blue LEDs analysis, we can notice that in this case the serie resistance of the devices seems to be lower, with less influence on the I-V. On the other hand, also the green LEDs, despite having all a very similar breakdown voltage (about 150 V, higher than in the blue LEDs case), seem to have behaviours that differ depending on the specific sample, failing at different current values.

The investigation continued considering the data regarding the leakage current. In fig. (6.7) and (6.8) we can observe the leakage as a function of the transmission line precharge-voltage and of the V_{DUT} respectively. The first and most important thing one can notice, is that the degradation is gradual in all of the four samples.

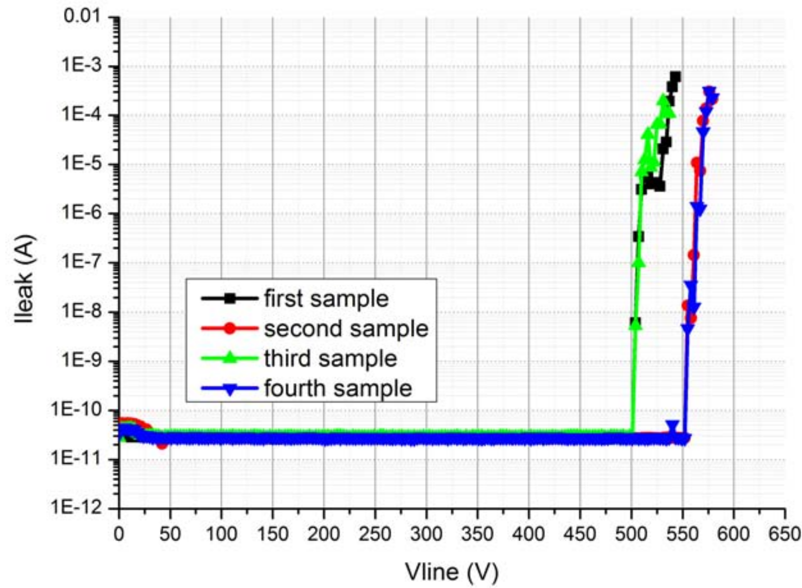


Figure 6.7: *Green LEDs leakage current as a function of the pre-charge voltage.*

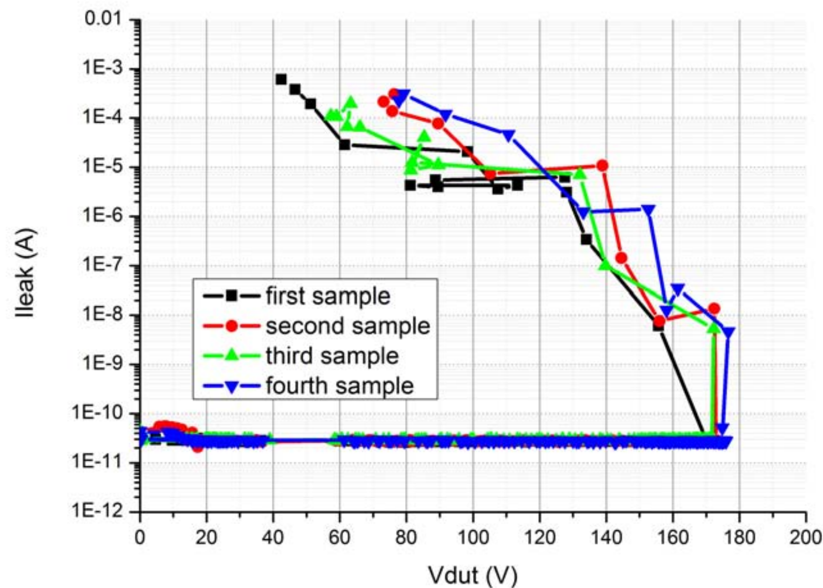


Figure 6.8: *Green LEDs leakage current as a function V_{DUT}.*

This behaviour is confirmed by the graph showing the pulse current (I_{DUT}) as a function of

the leakage (Fig. (6.9)). In these curves we can clearly see how the leakage current gradually increases, needing in some cases even more than ten steps from the beginning of the degradation, to reach the failure value.

However this is not the only information we can obtain from this graph. In fact we can see that the degradation process begins at a current value much lower than in the blue LEDs case. The leakage begins to increase when I_{DUT} is comprised between 3 and 4 amperes, while the blue samples leakage remained stable until about 4.8 A at least, with a maximum of more than 7 A. at first sight one could think that green devices are less resistant, anyway, even if these LEDs degradation begins at low level of currents, its graduality makes the failure current average higher than in the blue LEDs case, as we will show in paragraph 6.4.

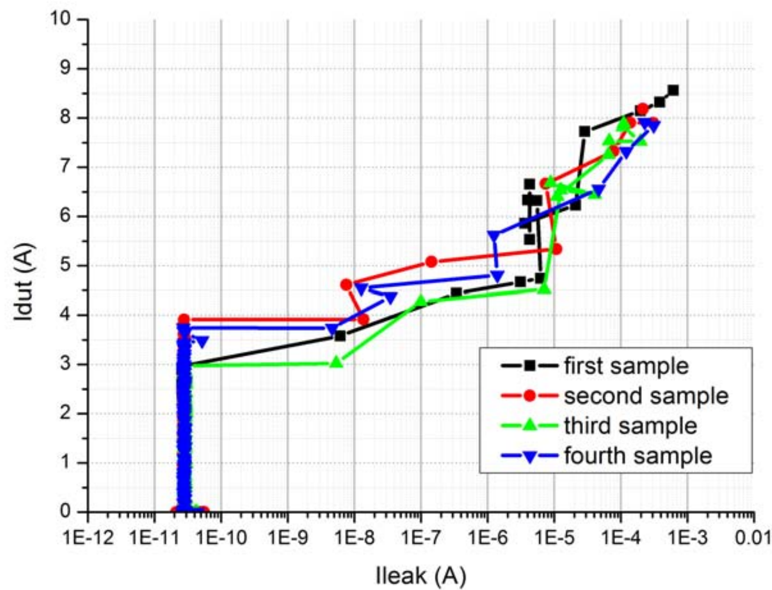


Figure 6.9: *Pulse current as a function of the DUT leakage current in the green LEDs stress-tests.*

The main information we could obtain from the green samples analysis is that their degradation process is gradual. The hypothesis we make to explain this characteristic, is that the higher content of Indium in these LEDs makes the defectivity of the material higher. Thus the devices have many leakage paths through which the reverse current can flow. This would explain the lower value of current at which the degradation begins. Furthermore, the presence of many conductive paths could lead to a lower current density and then to a more gradual degradation.

Finally, in Table (6.2) it is possible to observe a brief statistical summary of some significant data. $V_{failure}$ and $I_{failure}$ are the voltage and the current of the pulse that causes the failure; $I_{pre-failure}$ is the current of the one that precedes it; V_{deg} and I_{deg} are the voltage and the current of the pulse at which the degradation process begins and $I_{pre-deg}$ is the current of the pulse before that one.

	V_{fail} [V]	$I_{pre-fail}$ [A]	I_{fail} [A]	$V_{pre-deg}$	V_{deg}[V]	$I_{pre-deg}$ [A]	I_{deg}[A]
sample1	51.21	7.72	8.15	170.34	155.71	2.96	3.58
sample2	75.75	7.32	7.90	172.93	172.43	3.91	3.91
sample3	63.24	7.53	7.53	171.69	172.29	2.98	3.03
sample4	91.71	6.56	7.32	174.76	176.58	3.75	3.74
mean	70.48	7.28	7.72	172.43	169.25	3.40	3.57
std.deviation	17.3443	0.5108	0.3694	1.8792	9.2438	0.5011	0.3853

Table 6.2: *Green LEDs behaviour statistical summary.*

6.3 RED SAMPLES

We finally consider the red LEDs. The first step is as usual the analysis of the pulsed I-V. This curve already gives us a very interesting information, in fact, as it is possible to see, all the four samples behave almost in the same way, with a breakdown voltage of about 80V and failing at similar current values. We can also see that, as in the green LEDs case, the devices seem to have a low serie-resistance.

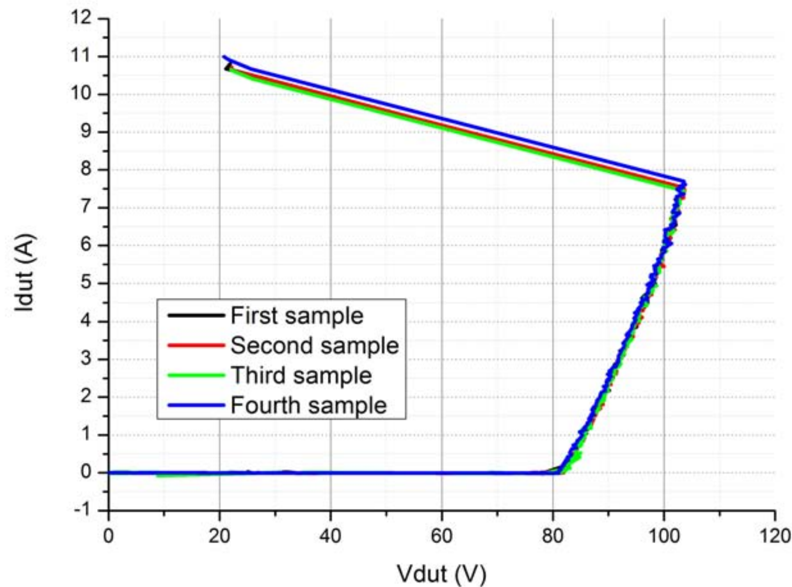


Figure 6.10: *Pulsed I-V characteristic of the green LEDs submitted to ESD-stress testing.*

The curves that show the leakage as a function of V_{line} and V_{DUT} also confirm what we have previously observed. In fact, in Fig.(6.11) and (6.12) we can see how the leakage starts to increase in correspondence of a very similar value in all of the four cases. Furthermore we can observe that the failure seems to be catastrophic, without a gradual increase in the leakage current as it

was the case for the green LEDs. In particular, after a first limited increase of about one order of magnitude, the leakage current reaches directly the failure value with a single abrupt increase.

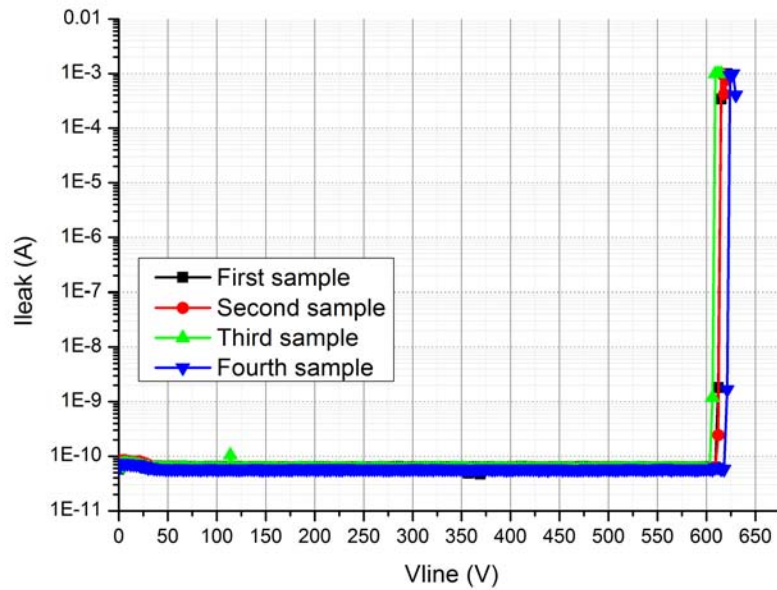


Figure 6.11: *Red LEDs leakage current as a function of the pre-charge voltage.*

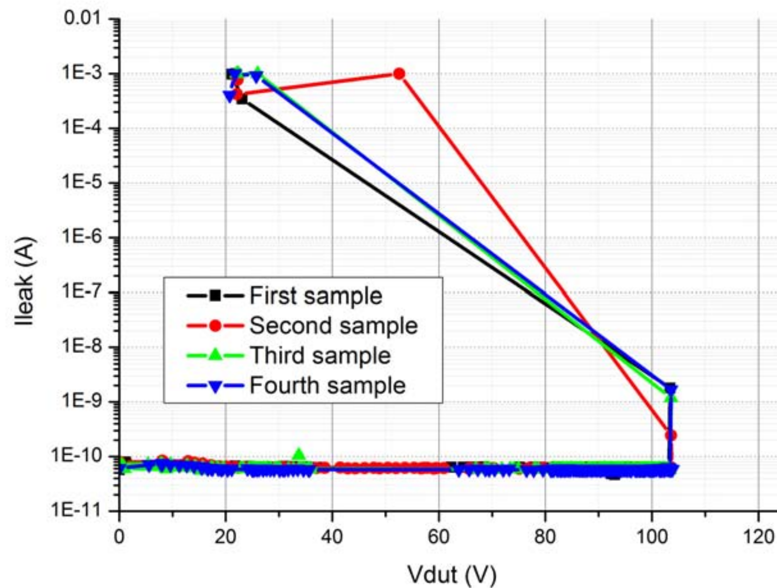


Figure 6.12: *Red LEDs leakage current as a function* V_{DUT}.

Finally analyzing the graph in Fig. (6.13) makes things even more explicit. In fact there seem to be some sort of threshold current value after which the LED catastrophically fails. This

	$V_{pre-fail}$ [V]	V_{fail} [V]	$I_{pre-fail}$ [A]	I_{fail} [A]	$V_{pre-deg}$ [V]	V_{deg} [V]	$I_{pre-deg}$ [A]	I_{deg} [A]
sample1	103.41	23.05	7.496	10.611	103.23	103.411	7.416	7.496
sample2	103.56	52.58	7.531	9.466	103.71	103.563	7.448	7.531
sample3	103.58	25.96	7.447	10.404	103.36	103.576	7.393	7.447
sample4	103.58	25.73	7.698	10.668	103.37	103.575	7.617	7.698
mean	103.53	31.829	7.543	10.287	103.42	103.531	7.469	7.543
std.deviation	0.0805	13.8950	0.1089	0.5589	0.2057	0.0805	0.1018	0.1089

Table 6.3: *Red LEDs behaviour statistical summary.*

behaviour can be due to the fact that the technology on which these devices are based, is quite old and as a consequence the material quality is high. The devices should then have a very low defects density and their properties should have a low instability.

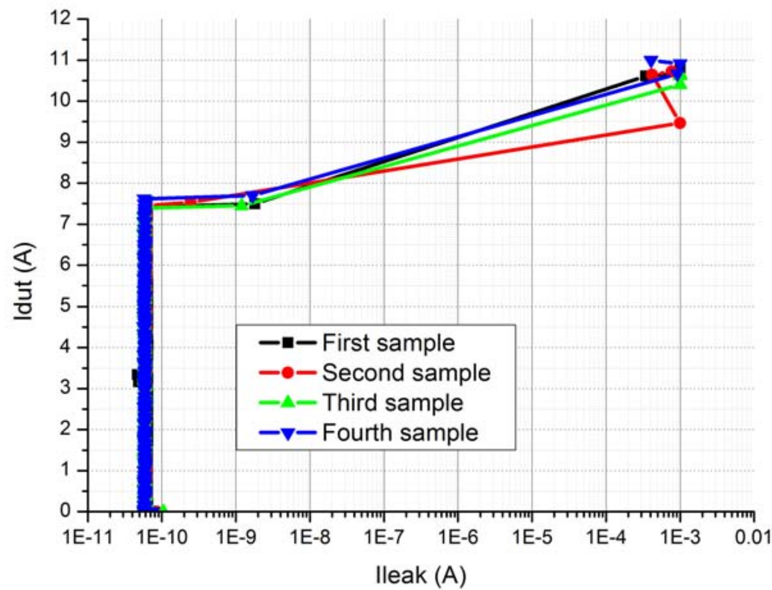


Figure 6.13: *Pulse current as a function of the DUT leakage current in the red LEDs stress-tests.*

In the following table we show some meaningful parameters we were able to evaluate during these measurements. Once again observing the very low standard deviation values, we can understand the high level of reliability and development reached by this technology.

6.4 FINAL CONSIDERATIONS

In this section the results obtained in the three different cases are summarized and compared. In particular, a global overview of the mean values of the data shown in the experimental statistical

	Blue LEDs	Green LEDs	Red LEDs	Unit
V_{fail}	202.99	70.48	31.829	V
$I_{pre-fail}$	5.96	7.28	7.543	A
I_{fail}	6.06	7.72	10.287	A
V_{deg}	\	169.25	103.531	V
$I_{pre-deg}$	\	3.40	7.469	A
I_{deg}	\	3.57	7.543	A

Table 6.4: *Mean values of some ESD-robustness related parameters for each type of LED.*

summaries is given in Table (6.4), where it is also possible to compare the results obtained for each type of LED.

Since our goal is to investigate the robustness of the LEDs towards ESD events, the most interesting parameter shown in Table 6.4 is I_{fail}, which is the highest current that the device could withstand before failing.

The green LEDs show a quite poor ESD-withstand performance, in fact their degradation starts at very low current value. Perhaps, according to our failure criteria, their extremely gradual degradation allows them to resist more than the blue samples did.

The red LEDs are the devices whose properties are the most stable, and are also the most robust, with the highest ESD-reverse current withstanding capability.

The blue LEDs show intermediate performance, because they do not have a low current degradation like the green LEDs, but they also show the lowest mean I_{fail} of the three types of devices. Anyway it is important to notice that the blue samples also showed highly unstable properties, as can be seen reading the standard deviation values in Table (6.1). A more accurate analysis is therefore needed to study the properties of these type of LEDs, that are also the most interesting for practical applications.

Chapter 7

SINGLE LEDS OPTICAL AND ELECTRICAL ANALYSIS

In the second part of this work, the different types of LEDs were once again individually submitted to reverse-bias ESD stress. In order to extend the comprehension of the ESD failure mechanism, optical analysis was added to the TLP measurement. In fact, some samples of each type of device were initially observed exploiting a microscope and an optical camera, and after that they were stressed while an EMCCD (the Andor Luca) registered the light eventually emitted during the discharge. Some photos of the chips after the failure were also taken, in order to observe possible visible degradation signs. Moreover the samples, before the negative pulses stress, were submitted also to non-destructive positive biased ESD-testing. This analysis, carried out at low pulse voltages (the maximum precharge voltage employed had a value of 153 V), was done with the purpose of investigating the ESD-current distribution on the chip.

7.1 BLUE LEDs TESTING

In this paragraphs the results of the investigation on the blue samples are described. Before analyzing the data obtained from the ESD-testing, it is useful to notice the particular structure of these devices. In fact, as can be seen in Fig. (7.1), the blue LEDs are characterized by a grid-shaped top contact. This solution was probably employed to obtain a spreading effect on the flowing carriers, improving this way the current distribution, an important parameter that can influence the robustness of the devices. On the other hand, it certainly causes a decrease in the extraction efficiency.

7.1.1 POSITIVE BIAS ESD PULSES

As already explained in Chapter 2, LED devices electrically behave as a diode. Since conducting a positive current is part of their normal operation, they are expected to have a high robustness towards positive biased ESDs (as proofed also by some of the articles cited in Chapter 4). In fact, even if the pulses applied for testing purposes can have a very high amplitude, they also

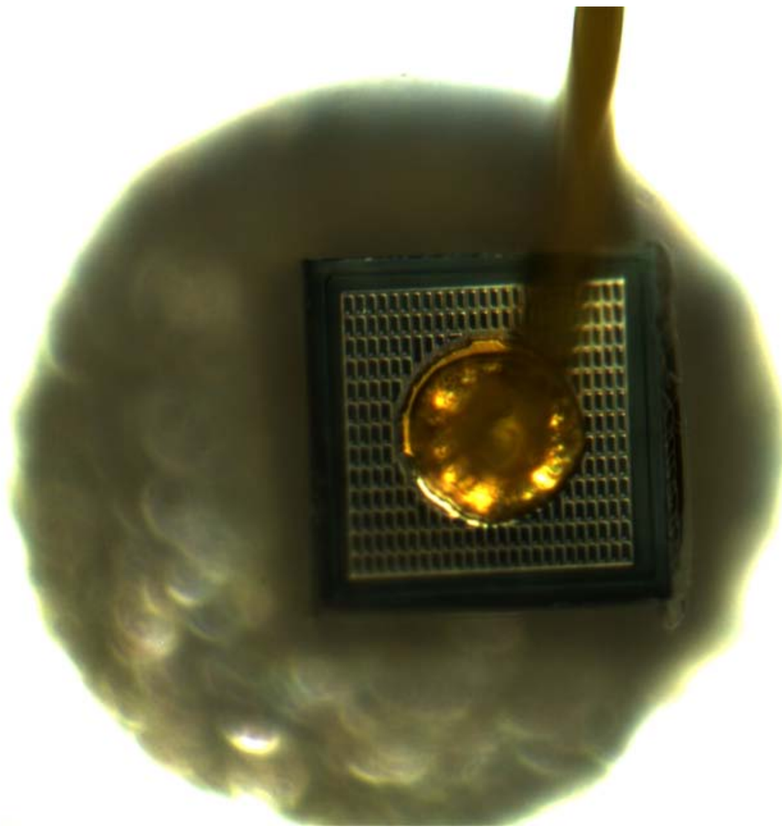


Figure 7.1: *Microscope photo of a blue LED.*

have a very short duration. Nevertheless, it is interesting to analyze the behaviour of the devices submitted to positive pulses, because at the very high frequencies that characterize the ESD phenomena, it can be different from expected.

In the following images it is possible to see the evolution of the light emission under direct biased ESDs as the pulse amplitude increases.

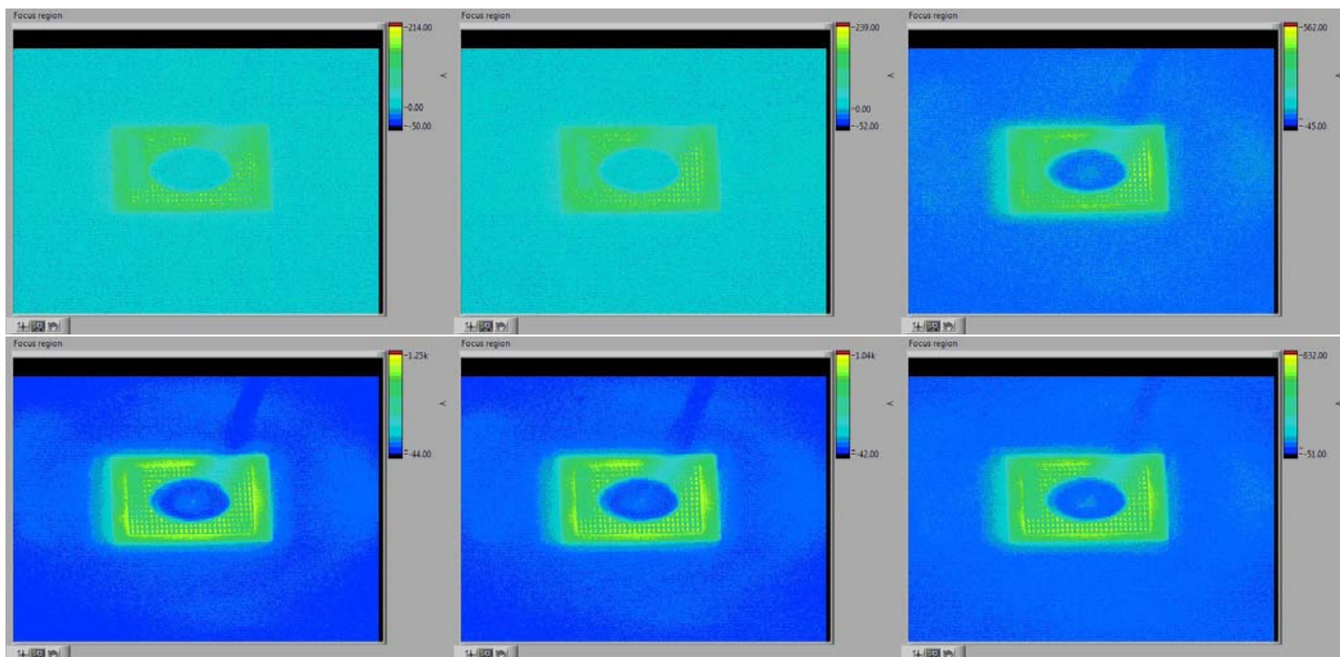


Figure 7.2: *Light emission of a blue LED submitted to positive TLP-pulses. The images show how the emission varies with the increase of the pre-charge voltage. The pictures refer to* V_{line} *values of 3, 33, 105, 201, 303 and 402* V *, clockwise.*

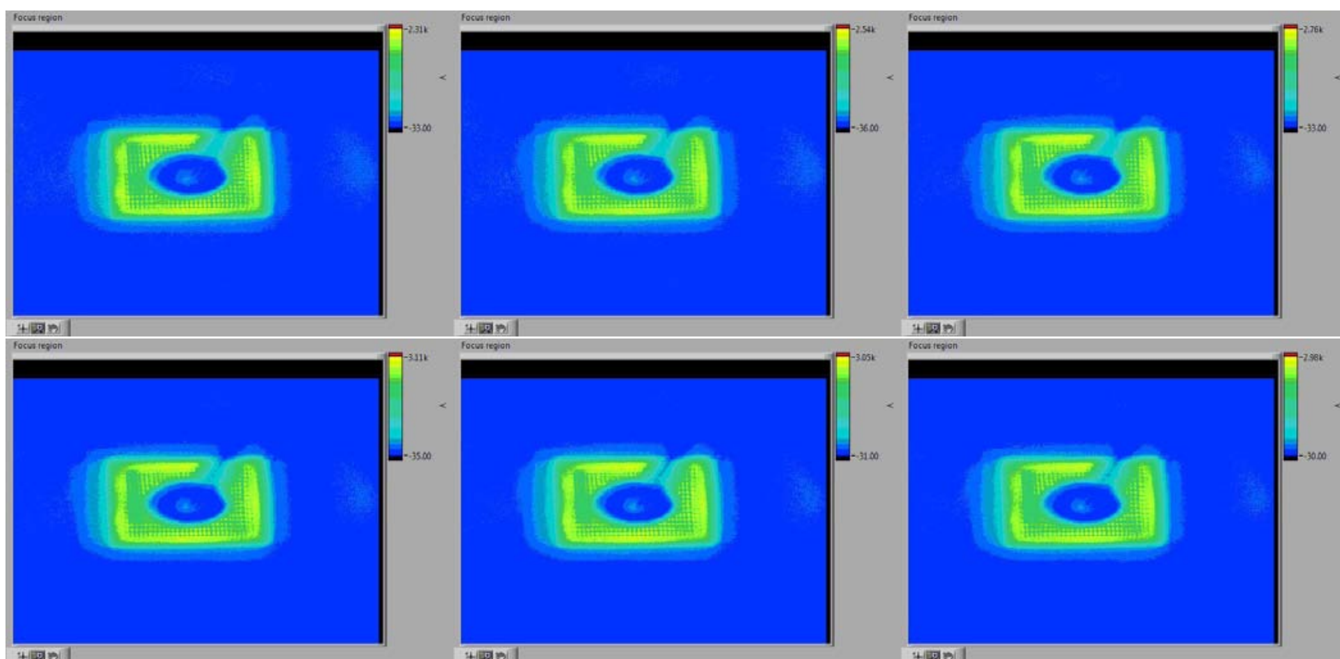


Figure 7.3: *Light emission of a blue LED submitted to positive TLP-pulses. The images show how the emission varies with the increase of* V_{line}. *In this case the pulse amplitude is higher. The precharge-voltages are 1401, 1602,1800,2004,2202 and 2301 volts respectively (clockwise).*

Looking at Fig. (7.2) it is possible to see how the light emission is detectable since the smallest pulses. Moreover, the grid-shaped contact seems to be very effective in spreading the current

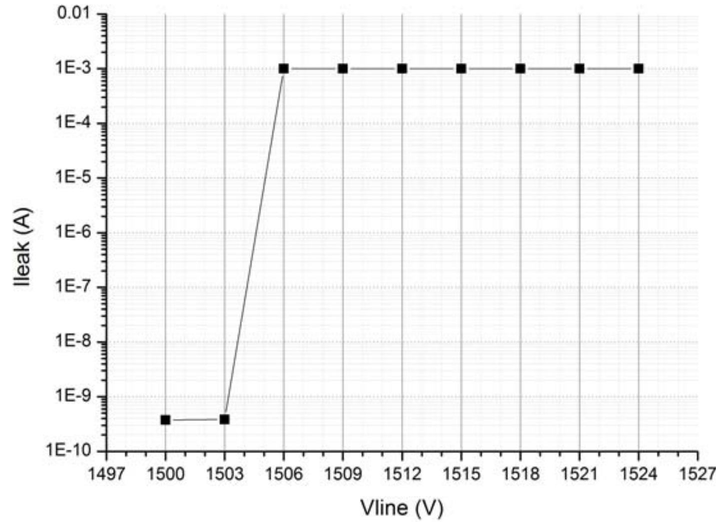


Figure 7.4: *Sample1 leakage current as a function of the pre-charge voltage.*

flow. In fact the emission is always distributed all over the chip surface, avoiding current crowding phenomena. This is true even at higher pulses amplitudes, as shown in Fig. (7.3).

7.1.2 NEGATIVE BIAS ESD-STRESS TESTS

To better understand the ESD-properties of the blue LEDs, leakage behaviour as a function of the transmission line pre-charge voltage V_{line} will be analyzed (as already done at the first stage of this experimental work). In addition to this, an investigation on the TLP pulse waveforms will be also performed. Combining these informations with the light emission data should provide a much higher knowledge of the ESD-related failure process in these samples. Furthermore, to assure that the catastrophic failure was not due to the additional stress provided by the reverse biasing during the leakage evaluation, the leakage current was measured applying $V_{DUT} = +1V$.

In Fig. (7.4) we can see the leakage current evolution during the stress test.

As already seen in the other blue devices tests (Chapter 6), even this sample seems to be characterized by a sudden, catastrophic failure. Exploiting the information on the pulse waveforms and the emission, it is possible to try to understand what happens when the leakage abruptly increases. In fig. 7.5 the pulse voltage and current waveforms are shown.

The leakage versus V_{line} graph, tells that the failure occurs when the pre-charge voltage reaches the value of 1503V. Observing the pulse waveforms, it is possible to notice a change in the shape of both the voltage and the current in correspondence of that discharge. Anyway it is possible to see that a slight variation occurs also in the tail of the pulse before (V_{line}=1500V). This change can be interpreted as a the beginning of the degradation process.

Observing the images of the light emission in correspondence of the ESD discharge, it is possible to notice that the degradation of the sample is confirmed by the detection of a small emissive spot on the chip surface (Fig. (7.6) V_{line} = 1503V). Even more interesting is to observe the emission

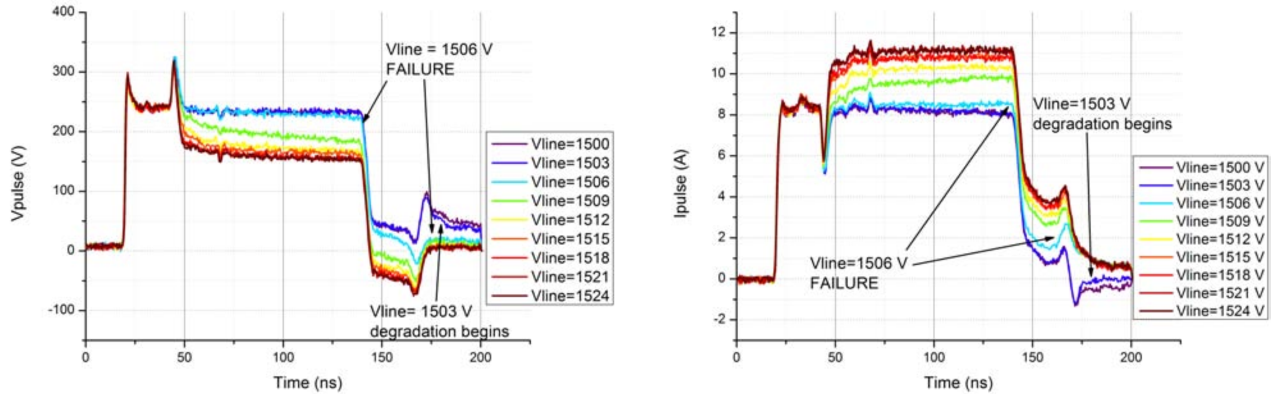


Figure 7.5: *The pulse voltage (left) and current (right) in correspondence of the last nine ESDs applied to the device.*

at the sample failure (V_{line} = 1506V). In fact it can clearly be seen that the emission intensity increases of more than one order of magnitude with respect to the previous ESD, denoting a catastrophic decrease in the blocking properties of the device. Even if the pulse voltage and current waveforms seem to show just a slight change in correspondence of $Vline$ = 1506V, the light emission clearly shows the the device has already failed and this result is consistent with the leakage data.

Interesting informations can be obtained also form the failed LED chip pictures shown in Fig. (7.7).

The LED's surface presents clear signs of the effects of the ESDs. A whole part of the device, corresponding to emitting area of Fig. (7.6), is totally burnt. The contact grid has molten and the contact metal seems to have diffused on the chip surface, due to the discharge thermal effects.

The same type of analysis was carried out also on two other samples, with the results shown in the following. The two samples will be referred to as *sample2* and *sample3.*

The pulse waveforms and leakage current evolution of sample2 can be observed in Fig. (7.8). The emission corresponding to the pulses of Fig.(7.8) (b) and (c) is shown in Fig. (7.9).

Also in this case the failure is catastrophic and highlighted by the appearance of ESD-related emission (V_{line} = 975V). Furthermore also here it is possible to notice a slight variation in the pulse waveforms in the ESD that comes before the failure.

Finally once again the ESD pulses have caused visible effects on the chip surface, as can be seen in Fig. (7.10).

This picture is particularly interesting because it allows to clearly identify the region where the degradation occurred. Comparing this image to Fig. (7.7), the failure effects seem less extreme in this sample, anyway the bonding metal seems to have diffused in both cases.

The same curves already seen for *sample1* and *2*, can be observed also for *sample3* in Fig.(7.11).

Once more the leakage has an abrupt and catastrophic increase (Fig. (7.11)), but this time it is possible to observe light emission just from the discharge that follows the failure (V_{line} = 1032V, Fig.(7.12) (d)). Even the changes in the waveforms corresponding to the ESD that caused the failure seem to be subtle.

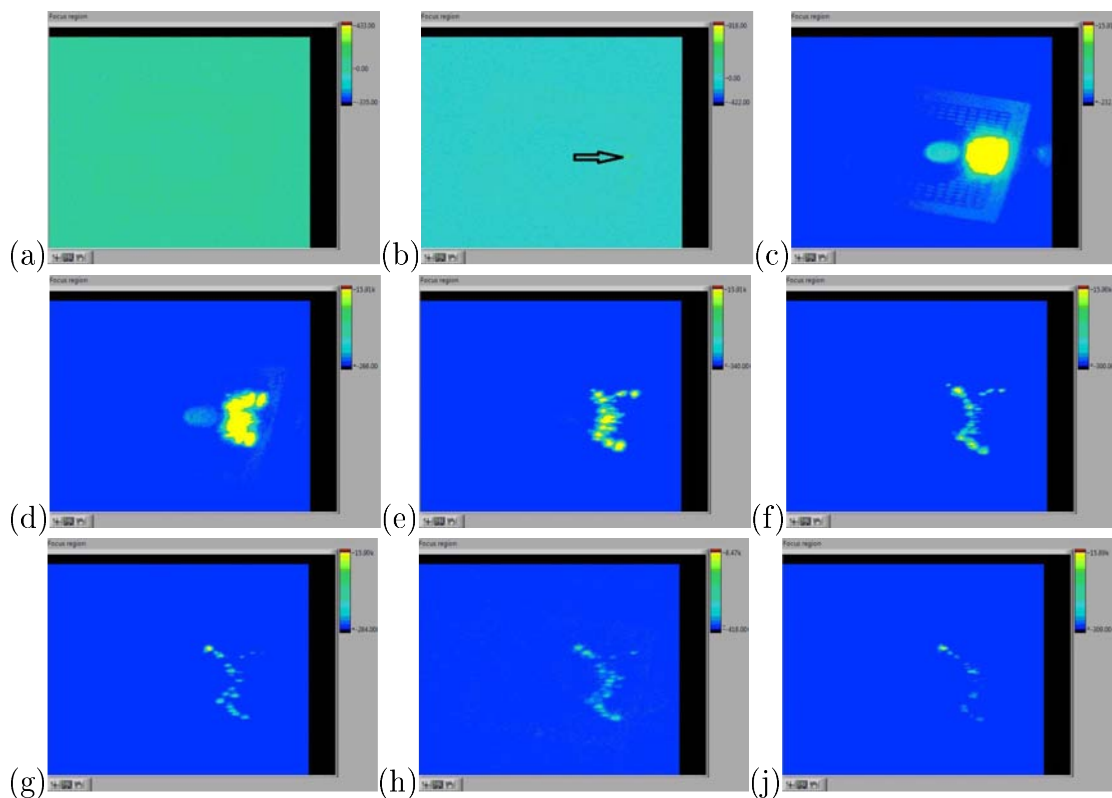


Figure 7.6: *Light emission in correspondence of the last 9 ESDs. The pre-charge voltage goes from 1500 to 1524 volts . (a) corresponds to* $V_{line} = 1500$ *and (j) to1524V, the voltage increases with steps of 3 volts.*

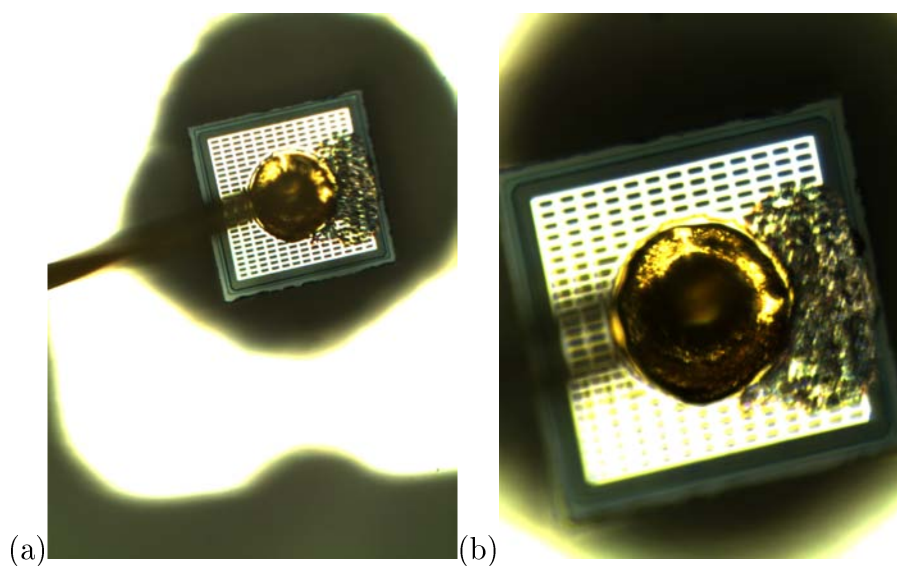
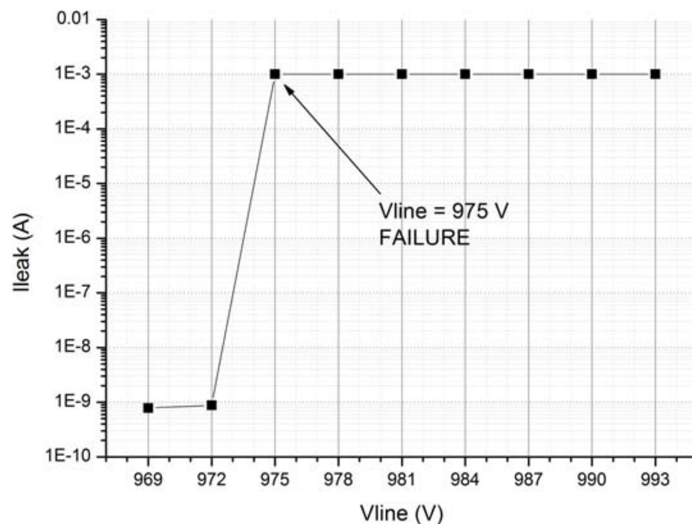
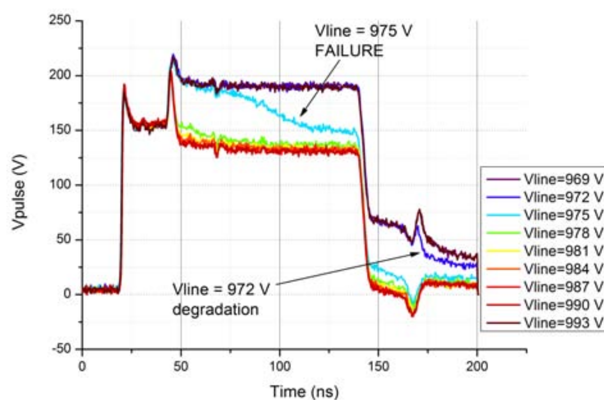


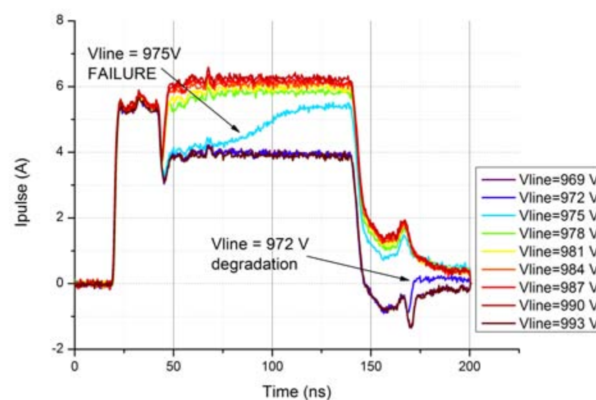
Figure 7.7: *Post-stress picture of the LED chip. Fig. (b) shows the damaged area in detail.*



(a)



(b)



(c)

Figure 7.8: Sample2 leakage current as a function of $Vline$ (a). Pulse voltage (b) and current (c) waveforms in correspondence of the last 9 ESDs applied.

Figure 7.9: *Sample2 light emission in correspondence to the ESD pulses for different values of the pre-charge voltage.* V_{line} *goes from 969(a) to 993(j) V with steps of 3 volts.*

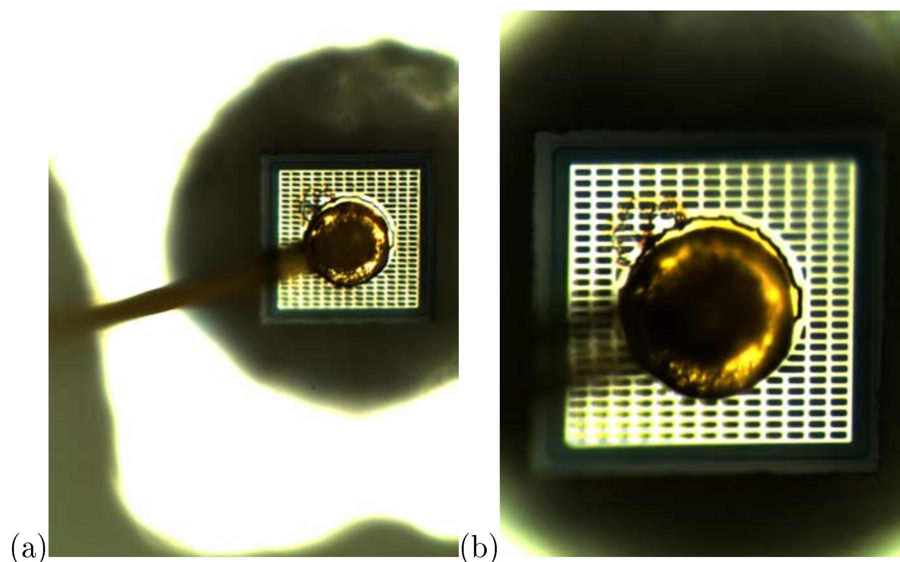


Figure 7.10: *Sample2 post-stress picture. Fig. (b) shows the damaged area in detail.*

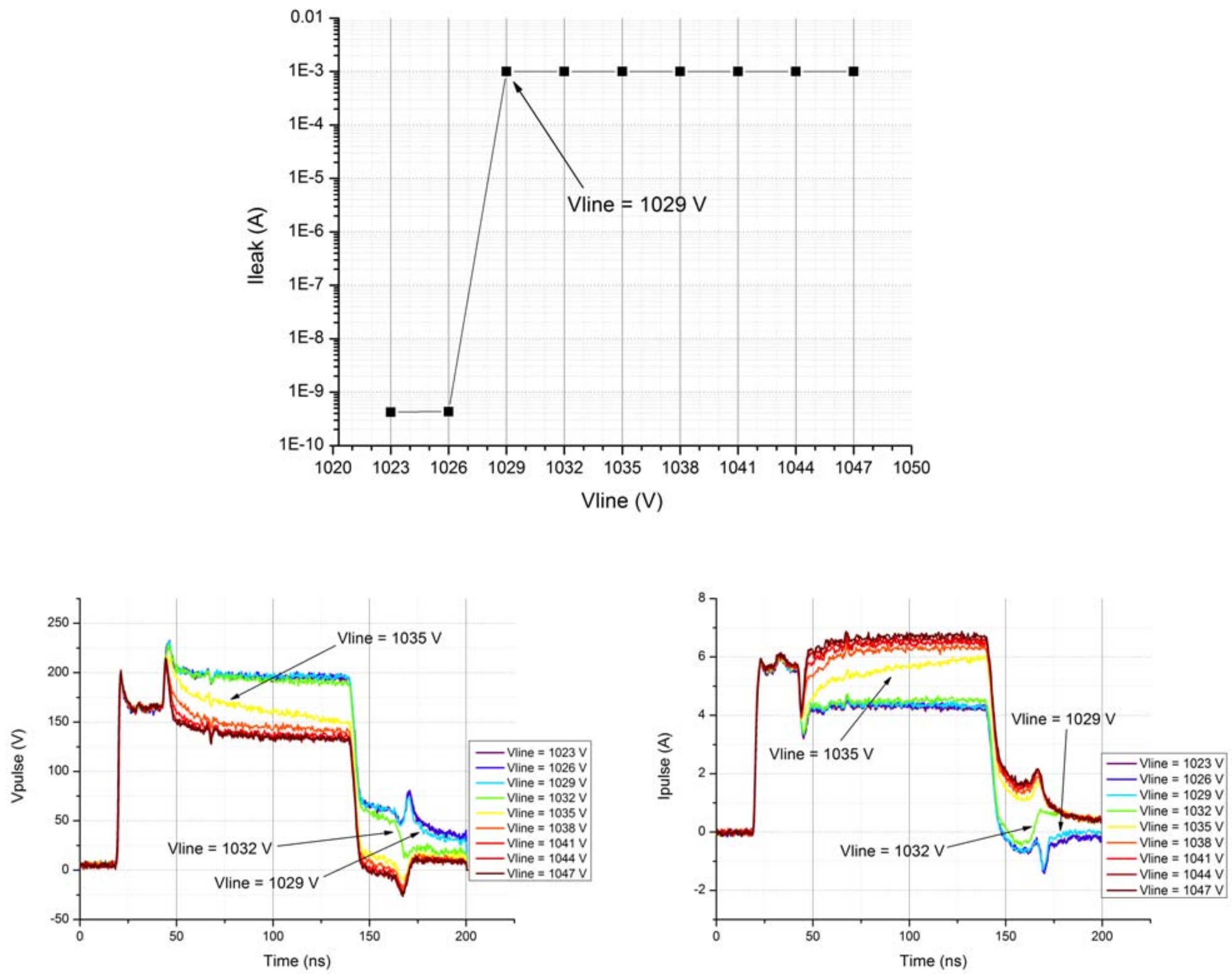


Figure 7.11: *Sample3 leakage current as a function of $Vline$ (a). Pulse voltage and current waveforms in correspondence of the last.*

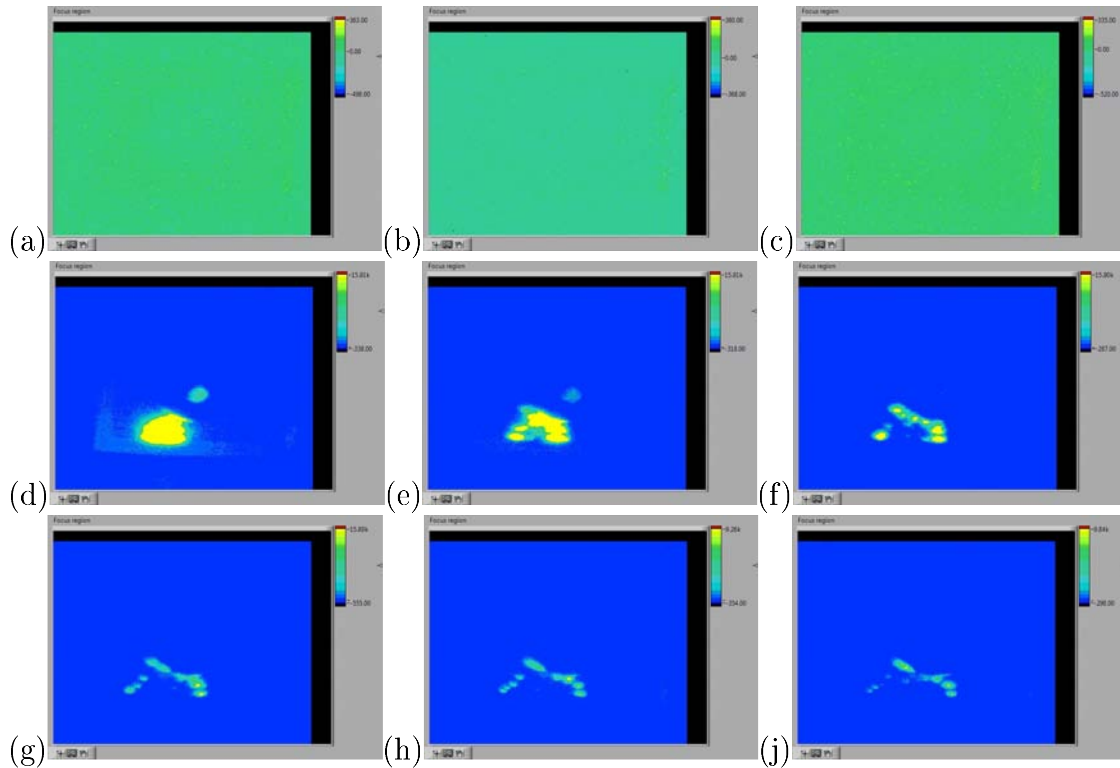


Figure 7.12: *Sample3 light emission in correspondence to the ESD pulses for different values of the pre-charge voltage.* V_{line} *goes from 1023(a) to 1047(j) V with steps of 3 volts.*

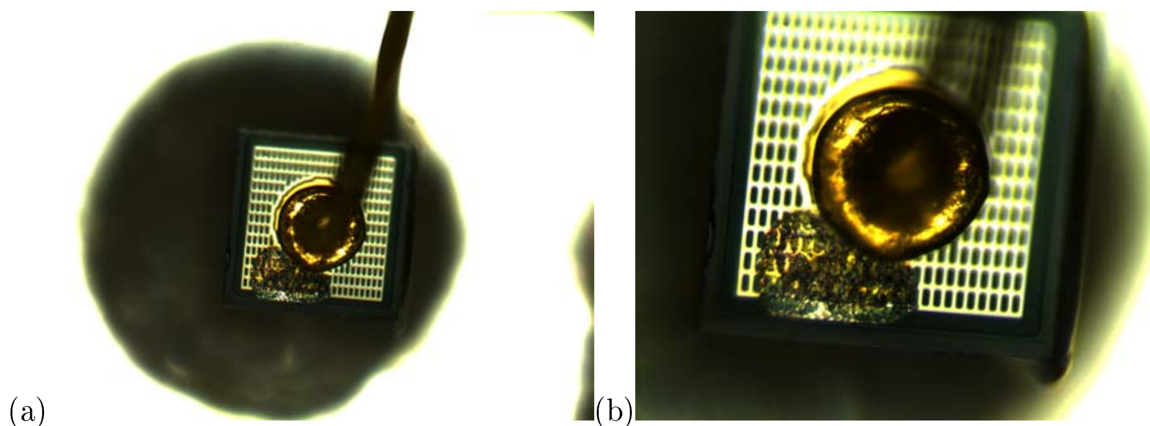


Figure 7.13: *Sample3 post-stress picture. Fig. (b) shows the damaged area in detail.*

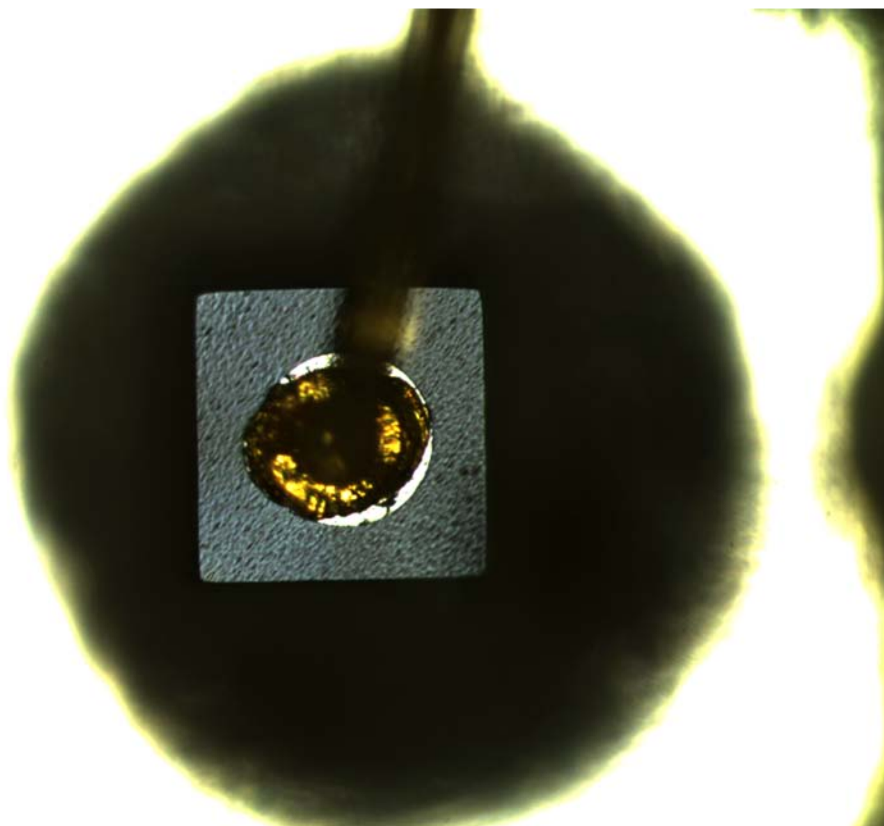


Figure 7.14: *Picture of a green LED chip.*

The images of sample3 chip surface after the failure are very similar to the ones reported in Fig.(7.7) and confirm what already observed in that case.

The analysis carried out on the blue LEDs confirmed that they are characterized by a sudden, catastrophic failure. It is also possible to notice that the failure is highlighted by ESD-related light emission. However the intensity of this emission seems to decrease after a peak in correspondence of the ESDs that immediately follows the failure.

Furthermore, observing the waveforms of the ESD pulse, it seems that the degradation begins in correspondence of the negative (positive with reference to the LED biasing) current peak in the final part of the impulse.

7.2 GREEN LEDs TESTING

The green LEDs gave the most interesting results at this stage and were thus more deeply studied; in the following a summary of the results obtained will be shown.

The first thing that is possible to observe, is that in this type of LEDs, there is no grid-shaped top contact. There is indeed just a metallic contact through bond-wire. This characteristic makes an investigation on the ESD current distribution particularly interesting. A photograph of one of these samples, taken through a microscope, can be seen in Fig. (7.14).

7.2.1 POSITIVE BIAS ESD PULSES

For the same reasons explained in section 7.1.1, and for what was said in the previous section, it is interesting to observe the light emission of the green samples submitted to positive-bias ESD pulses. In Fig. (7.15) and (7.16) a set of images of the emission of a green LED submitted to positive-bias pulses is reported. These images refer to just one particular sample, but the results are confirmed also in the other cases.

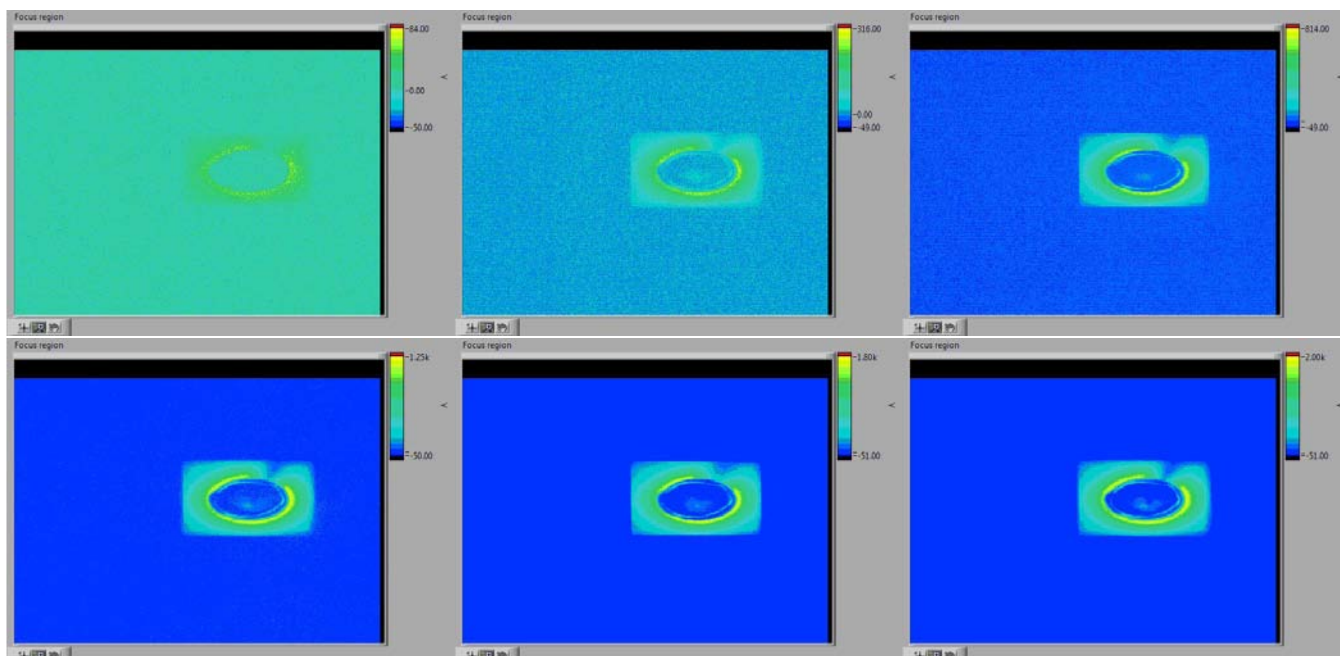


Figure 7.15: *Light emission of a green LED submitted to positive TLP-pulses. The images show how the emission varies with the increase of the pre-charge voltage.*V_{line} *values are 3, 33, 102, 201, 303 and 402 V (clockwise).*

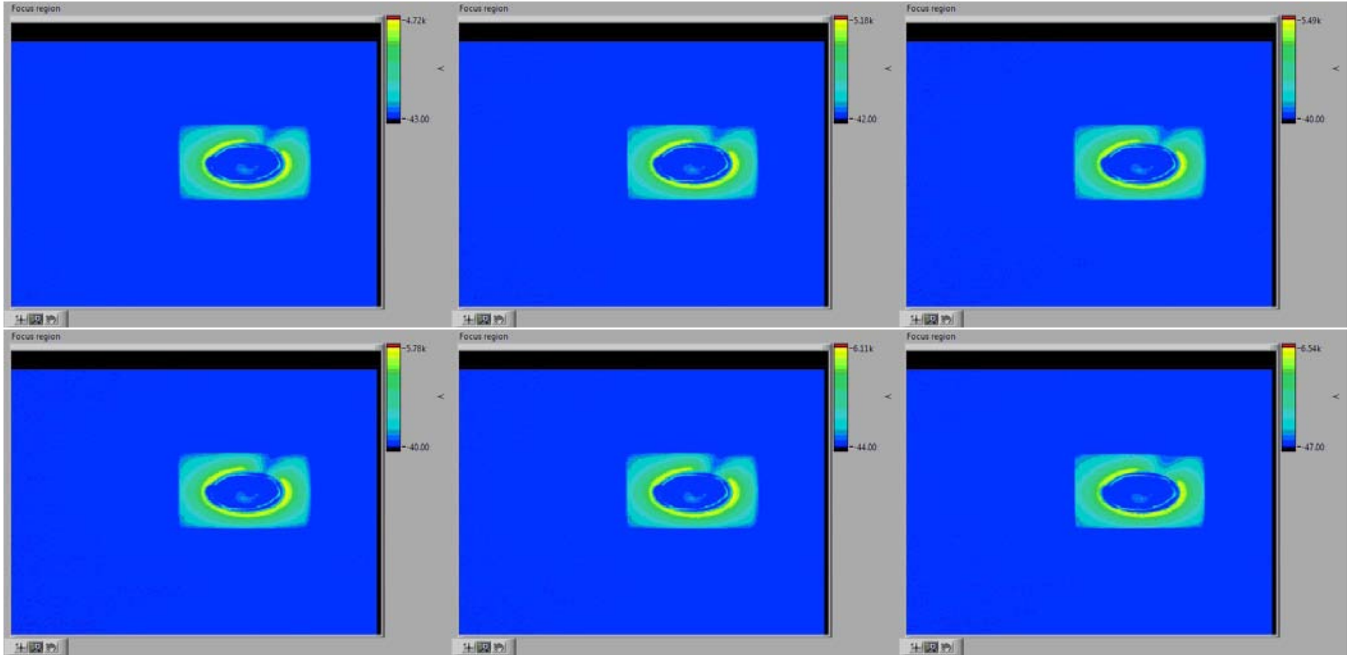


Figure 7.16: *Light emission of a green LED submitted to positive TLP-pulses. The images show how the emission varies with the increase of V_{line}. In this case the pulse amplitude is higher. The precharge-voltages are 1401, 1602,1800,2004,2202 and 2301 volts respectively (clockwise).*

The analysis of the light emission images immediately allows to notice that a heavy current crowding effect is present. In fact the emission is concentrated around the bonding. This behaviour is already visible at low pulses amplitude and characterizes the device also when the current increases. Even if the region where the emission is located seems to slightly broaden as the pulse amplitude increases, it always remains a very limited part of the chip. It is therefore possible to deduce that the absence of a grid-shaped contact strongly affects the current distribution.

7.2.2 NEGATIVE BIAS ESD-STRESS TESTS

As previously done with the blue LEDs, some green samples were submitted to reverse bias ESD stress tests while detecting the light emitted using the Andor Luca camera. In the following, the most significant data obtained in this way will be shown.

One of the most interesting behaviours was shown by s*ample3*. In Fig.(7.17) it is possible to see its leakage evolution as a function of V_{line}.

This sample has a very long gradual failure, in fact the leakage increases significantly a first time at about V_{line} = 660 V, but after that it remains stable for more than 30 ESDs. It is now interesting to observe the correspondent pulse waveforms, and check if the increase in the leakage current produced a detectable light emission.

Analyzing Fig.(7.18) and (7.19) it can be seen that, as expected, there is a clearly noticeable alteration of the pulse waveforms in correspondence of the leakage increase. Furthermore this degradation is accompanied by emission of light, located on the device border (it is possible to distinguish the chip shape because of the ambient light. See also Fig.(7.21)).

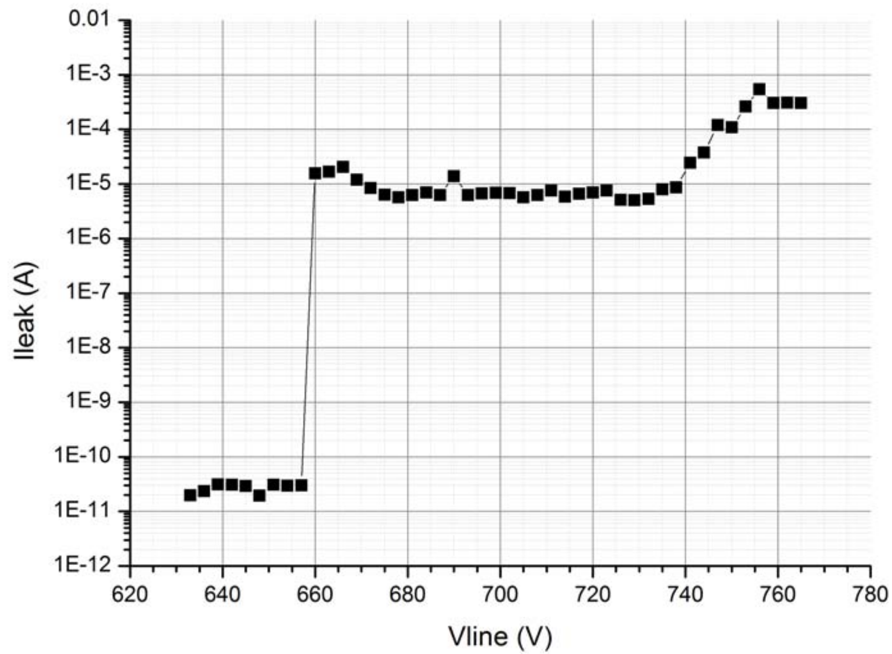


Figure 7.17: *Sample3 leakage current as a function of V_{line}.*

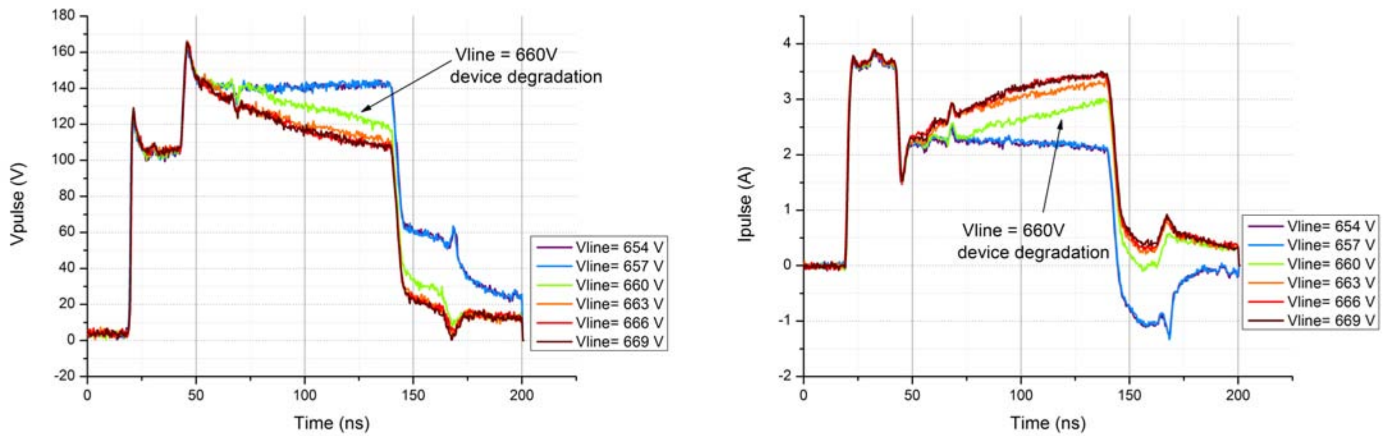


Figure 7.18: *Pulse voltage (left) and current waveforms in correspondence of the initial degradation of sample3.*

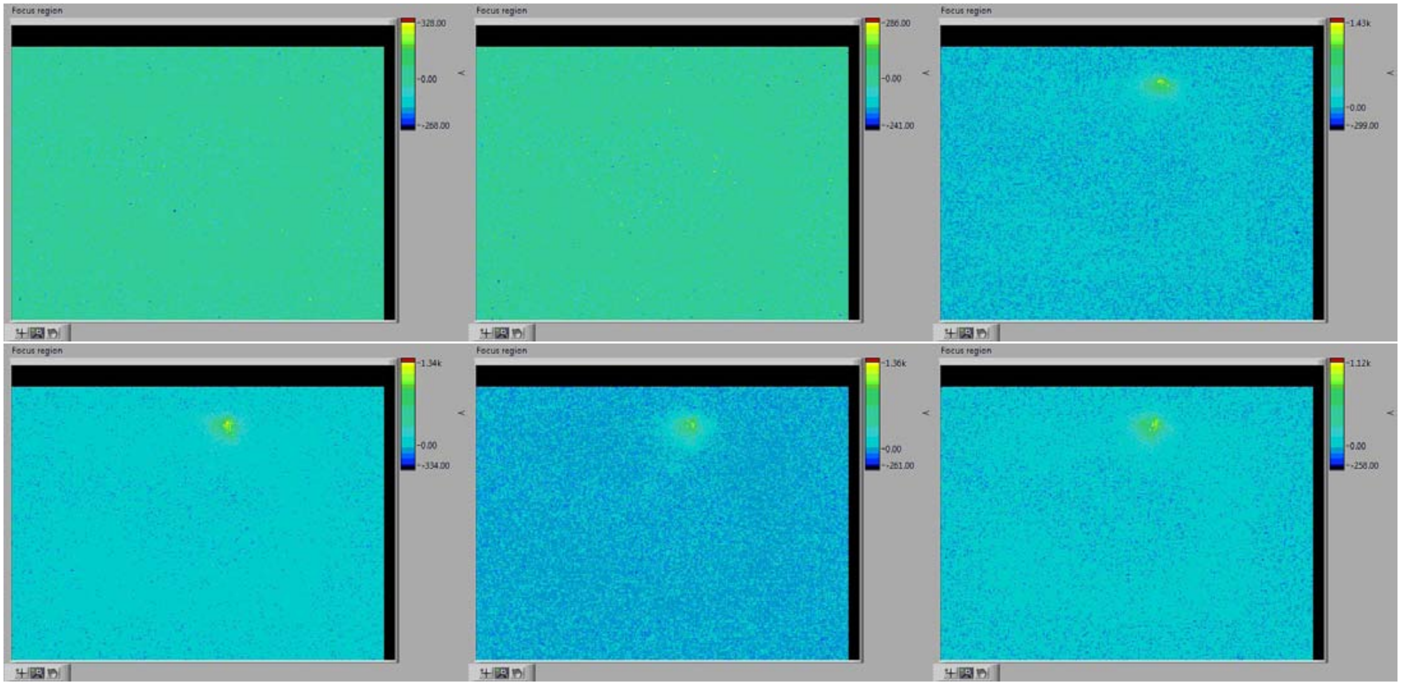


Figure 7.19: *Sample3: light emission as V_{line} increases from 654 to 669 volts (clockwise).*

After the initial increase, the leakage current remains quite stable and also does the emission. Anyway, after a certain number of applied pulses, the area where the emission is located starts to change (Fig.(7.20)).

This behaviour can be noticed even at a later stage (Fig.(7.22)). It could be due to the destruction of the old parasitic leakage paths and the consequent creation of new ones, it could also be a diffraction induced effect, or even an error due to the presence of the material that covers the chip.

While the emission spot keeps changing the leakage remains quite stable until the final degradation. When this happens, the light emission seems to stabilize both in area and in intensity (even if this could be due to the camera saturation).

The graphs of Fig.(7.24) clearly show that the LED is failing. The increase in the leakage corresponds to the waveforms deformation, with the voltage that starts dropping (while the current has a peak). As can be seen, the way the waveforms change is very particular. In fact, at the beginning this change is temporary; there is a drop that occurs just in the final part of the waveform and the next pulse has not an altered shape at the beginning. The voltage and current curves change in a stable way just when the leakage current reaches the failure threshold.

The sample whose analysis has just been reported is not the only one that showed a gradual failure. Also another one in fact, had a very long and gradual degradation. Anyway, even if also in that case it was possible to observe ESD-related light emission in correspondence of the first degradation, after that discharge this phenomenon disappeared, and it was detected again just after a further increase in the leakage current.

Another interesting case of study is given by *sample6*. This LED failed in a gradual way, but very differently from *sample3*. To better understand this difference, it must be explained that the failure was considered to be catastrophic if the leakage increased from values lower than 1×10^{-8} to the failure level in just one step. *Sample6* failure is therefore considered gradual.

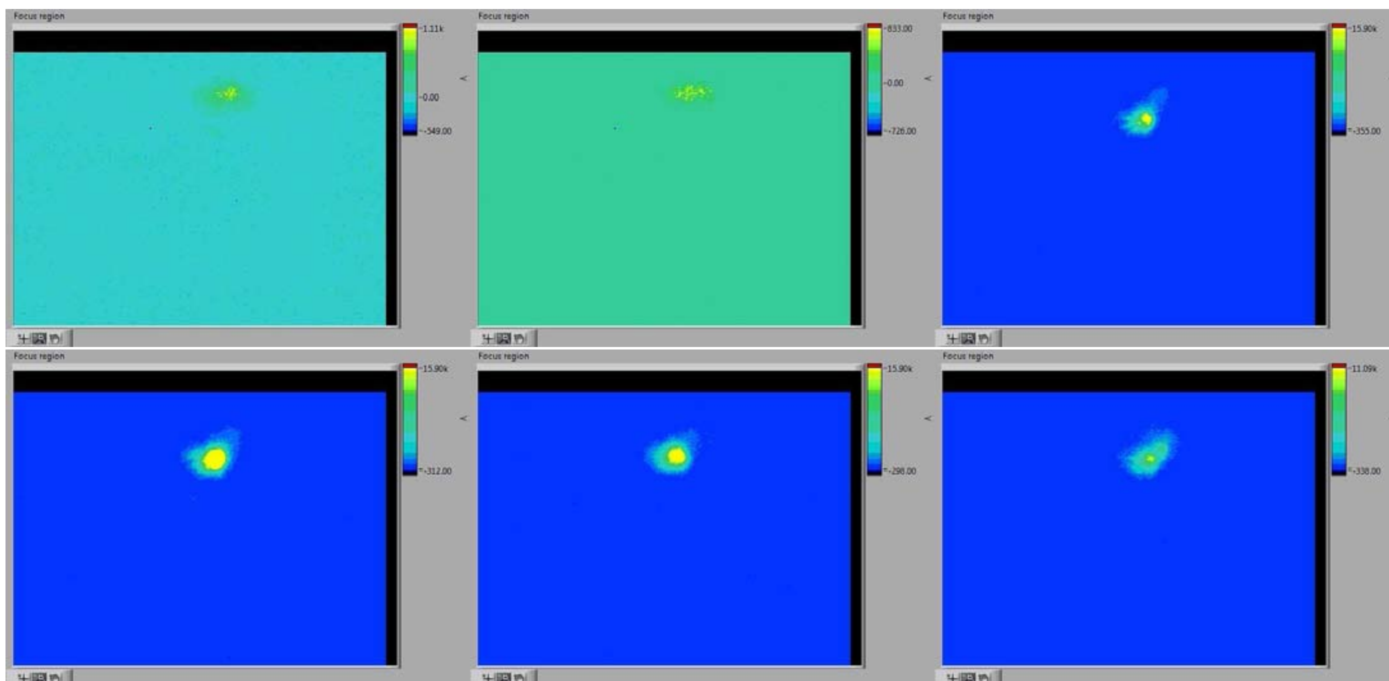


Figure 7.20: *Sample3: evolution of the emission as* V_{line} *increases from 675 to 690 with steps of 3 volts (clockwise). The area where the emission is located seems to vary.*

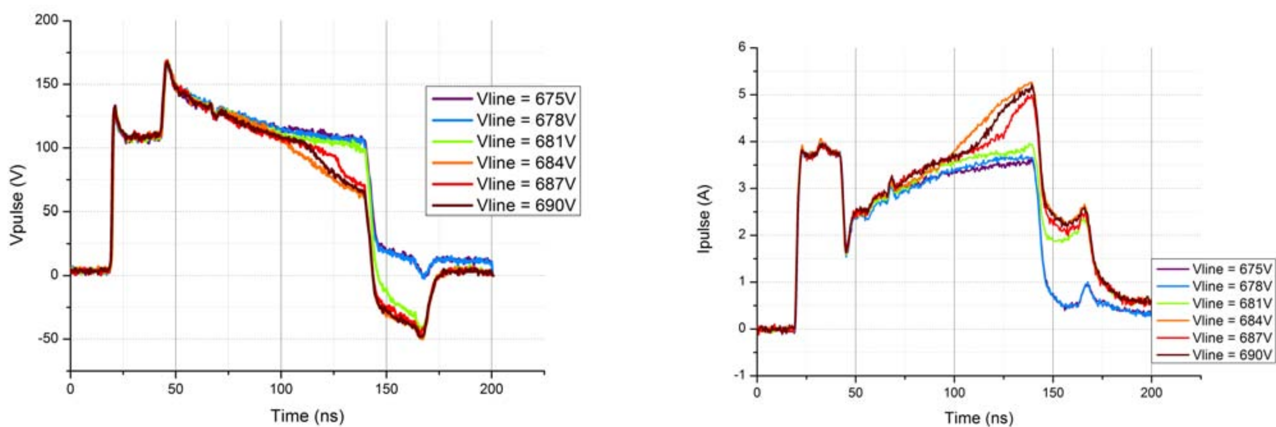


Figure 7.21: *Sample3: pulse voltage and current waveforms corespondent to the emission pictures of Fig.(7.20).*

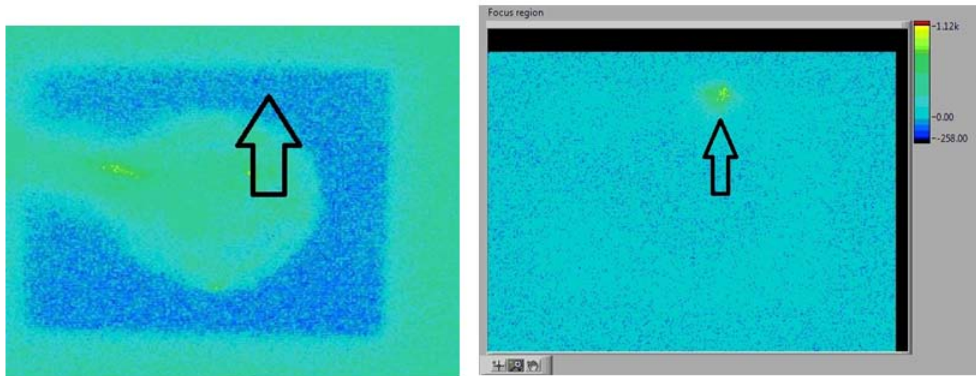


Figure 7.22: *A pre-stress picture of green LED sample3 is compared with an image of the same device under reverse bias ESD.*

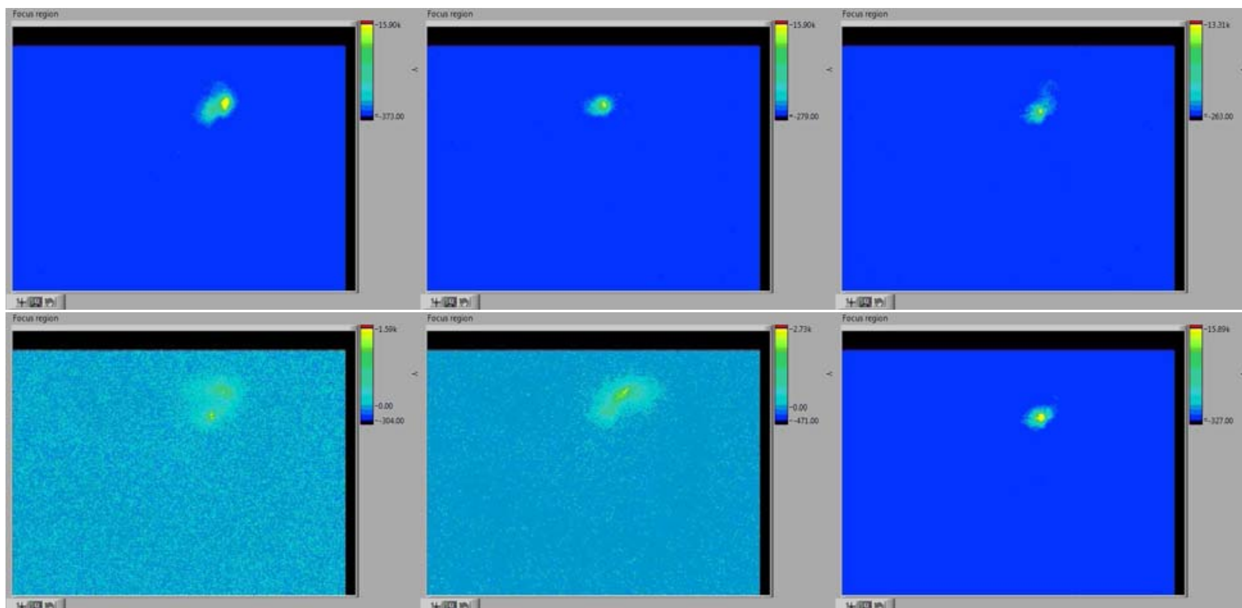


Figure 7.23: *Sample3: change in the emission area as* V_{line} *varies from 708 to 723 volts with steps of 3V (clockwise).*

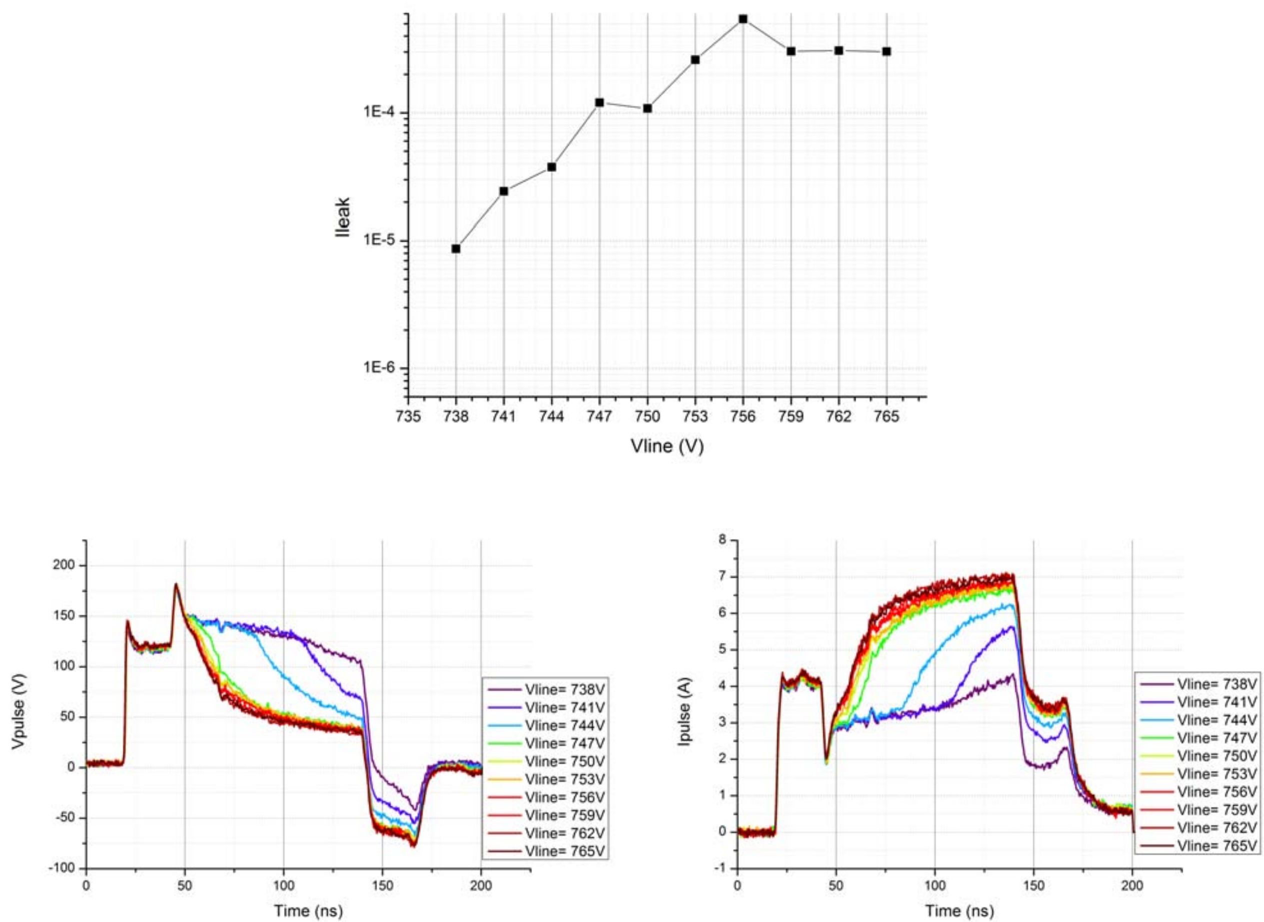


Figure 7.24: *Leakage current and pulse waveforms in correspondence of the final LED (sample3) degradation.*

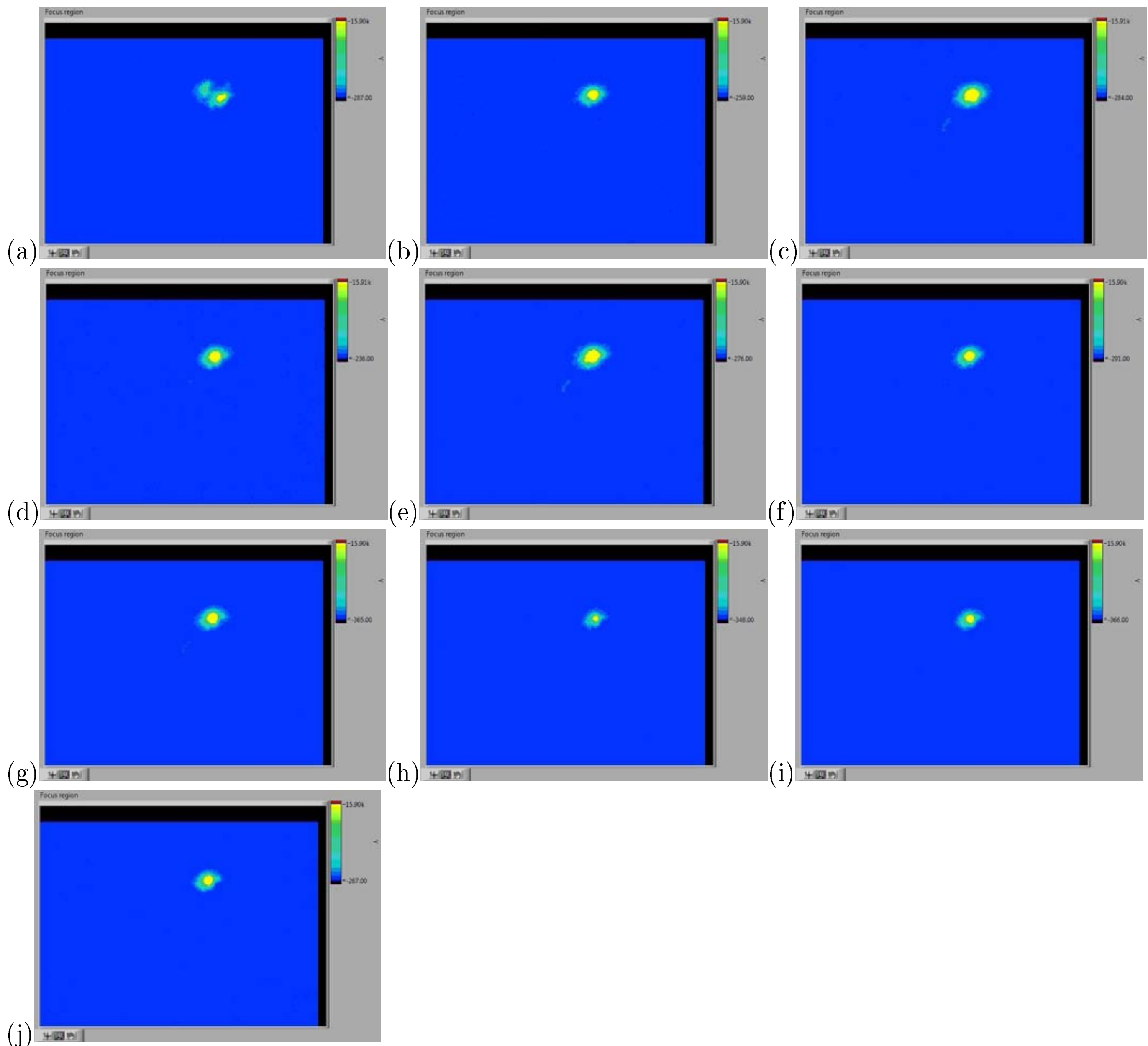


Figure 7.25: *Sample3: luminous emission in correspondence of the final degradation. The corresponding V_{line} goes from 738 (a) to 765V (j), with 3 volts step size . The emission in correspondence of the discharge that causes the failure is shown in (d).*

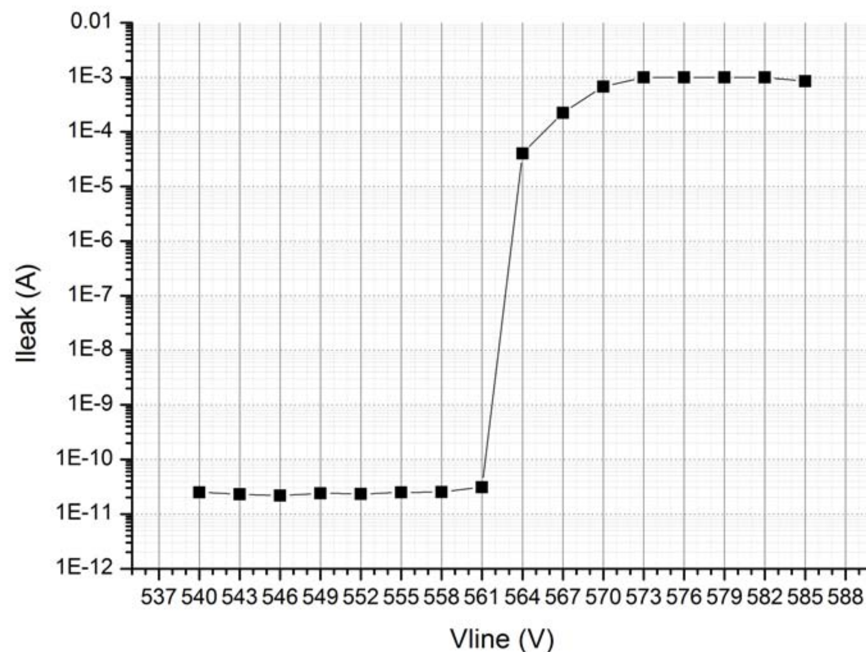


Figure 7.26: *Sample6 leakage current as a function of the transmission line pre-charge voltage* V_{line}.

In Fig. (7.26) a global view of *sample6* leakage current evolution during the stress is given.

An analysis of the pulse voltage and current waveforms during the degradation, shown in Fig. (7.27), highlights the graduality of this process. It is interesting to notice how the waveforms shape changes in correspondence of the ESD that causes the degradation of the leakage. Furthermore, it is also possible to see that the changes are in general very gradual, suggesting a degradation process still ongoing even after the failure.

To gain a better knowledge about the phenomenon, it is possible to analyze the emission in correspondence of the degradation too (Fig.(7.28)). As previously seen in the *sample3* case, light emission occurs when the device starts to degrade. Moreover the emission is located in a border region of the chip (more precisely in the corner). This is particularly clear observing Fig.(7.28)(g) and Fig.(7.29).

Even if in the previous examples the samples degradation was gradual, catastrophic failure also occurred. This is the case of the so-called *sample7*. In that case, as can be seen in Fig.(7.30), the leakage current is stable at a low value until it has an abrupt increase and reaches the failure level.

The waveforms of the last 9 pulses applied are reported in Fig. (7.31). The device failure can be clearly identified in the pulse denoted as "V_{line}= 573 V" and this is consistent with what is noticeable in Fig. (7.30). The voltage waveform is stable until at a certain moment it starts decreasing (while at the same time the current starts increasing).

Other interesting informations can as usual be deduced observing also the emission pictures, Fig.(7.32). Once again light emission is detected in correspondence of the ESD that causes the failure (c) (V_{line}=573 V), and also this time this emission is located on the chip border,

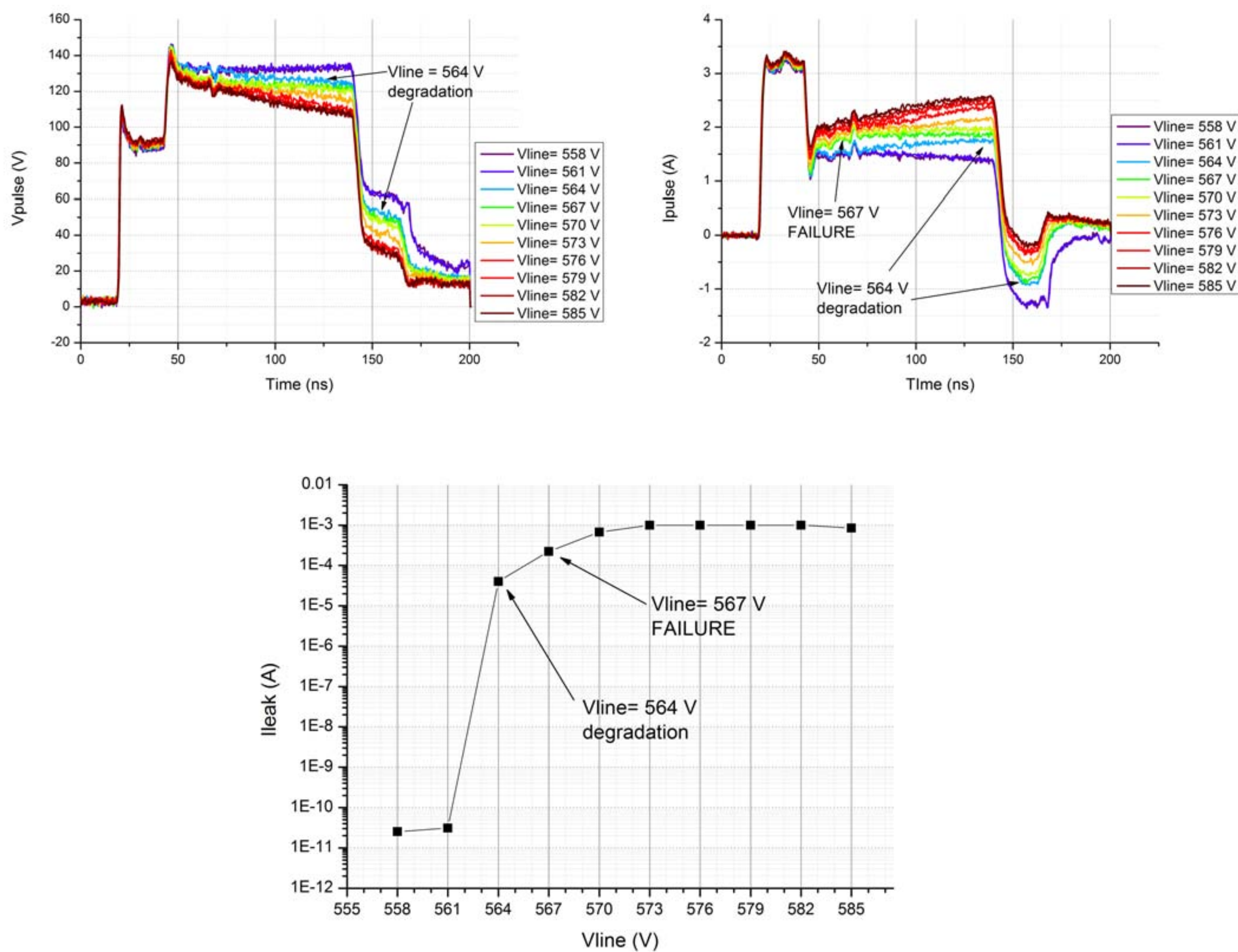


Figure 7.27: *Sample6: pulse voltage and current waveforms and leakage current as a function of* V_{line}.

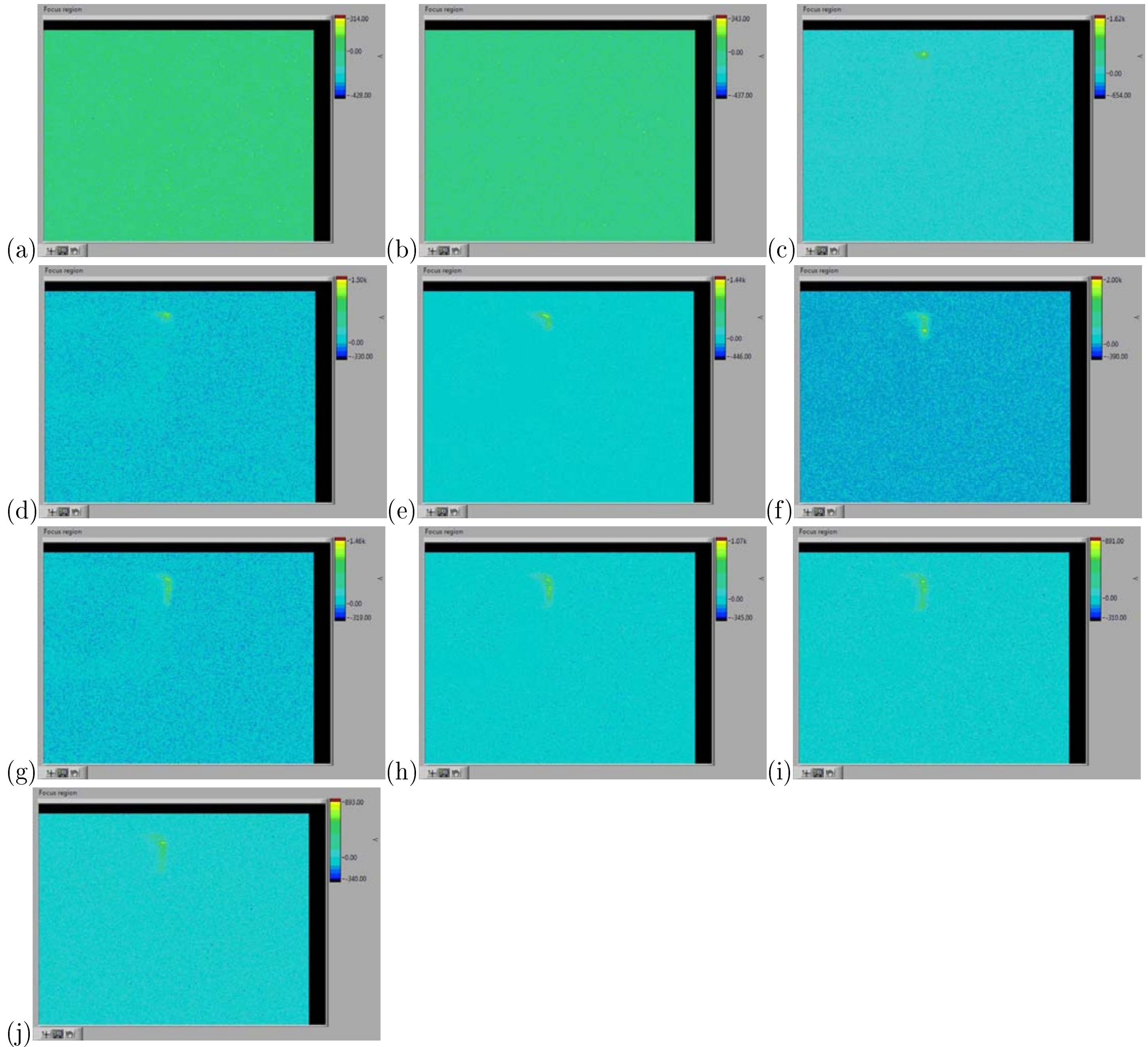


Figure 7.28: *Luminous emission in correspondence of sample6 degradation. The corresponding* V_{line} *goes from 558 (a) to 585V (j), with 3 volts step size .*

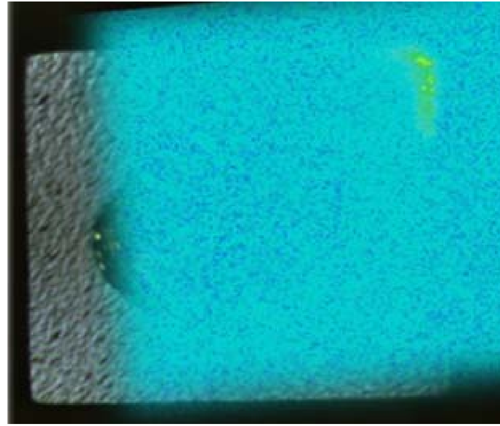


Figure 7.29: *A picture of sample3 chip and an image of the ESD-related emission overlapped to show that the emission is located on the chip corner.*

Fig.(7.33).

The obtained results confirm that the green LEDs tend to degrade more gradually than the blue ones. Furthermore this degradation seems to produce a reverse-bias emission related to the negative current conduction. Another important thing that it was possible to find out, is that in the green samples this emission is localized in the border regions of the chip, suggesting an important role of the material defects in the reverse current conduction. These areas are in fact the ones where the defectivity is higher. Indeed it can be supposed that the green samples degradation is due to the worsening of defects-related leakage paths that already exist.

Finally it seems possible to clearly identify the moment in which the degradation and/or failure occurs by observing the voltage and current pulse waveforms. This fact allowed to observe that the failure can take place both when the voltage is maximum and in correspondence of the pulse tail, when the amplitude is lower.

7.3 RED LEDs TESTING

7.3.1 POSITIVE BIAS ESD PULSES

Fig.(7.34) and (7.35) show the images of the red LEDs emission under positive ESD pulses. As previously seen for the green LEDs the emission is concentrated in a small annulus near the metal contact. This current crowding phenomenon is probably due to the absence of a grid-shaped contact. In fact, these LEDS have the same type of contact of the green ones and this can explain the similarity of the behaviour.

Anyway in this case, even if current crowding can be observed both at low and high current values, when the pulse amplitude increases the emission seems to become more distributed than in the green LEDs case.

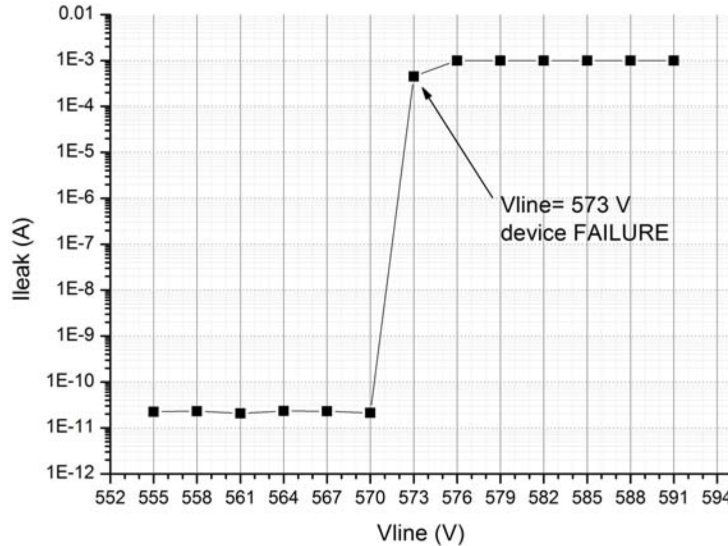


Figure 7.30: *Sample7 leakage current as a function of V_{line}.*

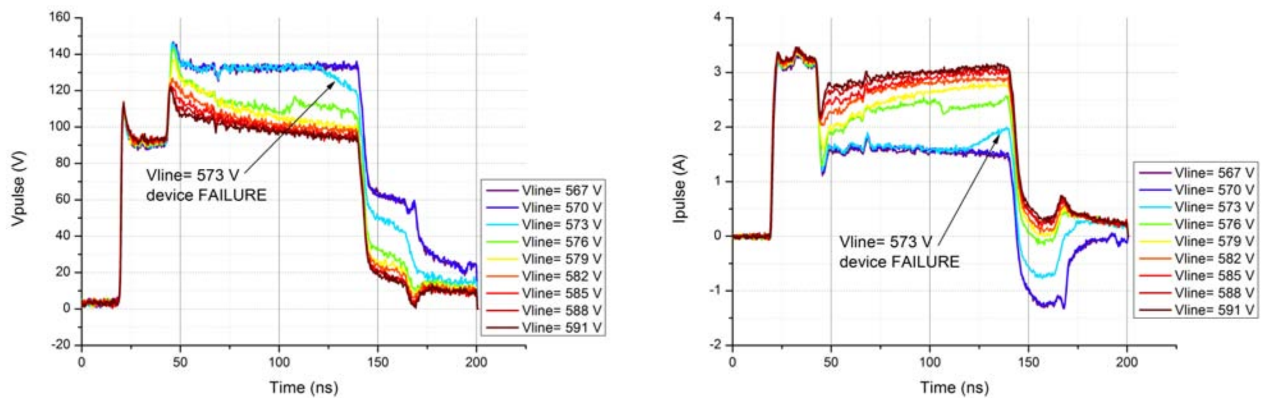


Figure 7.31: *Voltage and current waveforms of the last 9 pulses applied to sample7.*

7.3.2 NEGATIVE BIAS ESD-STRESS TESTS

Also in the red LEDs case the leakage current and the pulse waveforms were analyzed, Fig.(7.36) and (7.37). Analyzing the behaviour of sample3, it is possible to observe that a catastrophic failure occurs in correspondence of $V_{line} = 1044$ V. This is consistent with what it can be seen in the pulse waveforms graphs. In fact it is clearly possible to identify the moment corresponding to the failure. Observing the pulse denoted as "$V_{line} = 1044$", there is a sudden drop in the voltage waveform (and at the same time there is a sudden increase in the current value). This is the sign that the device has failed and has been transformed into a resistance. In fact, all the pulses that come after this one, are characterized by high values of current and low voltages, then the sample has become a short-circuit.

It is also interesting to investigate the emission in correspondence of the ESDs, as already done for the blue and green LEDs. In Fig. (7.38) the light emission in the sample3 case is shown. Once

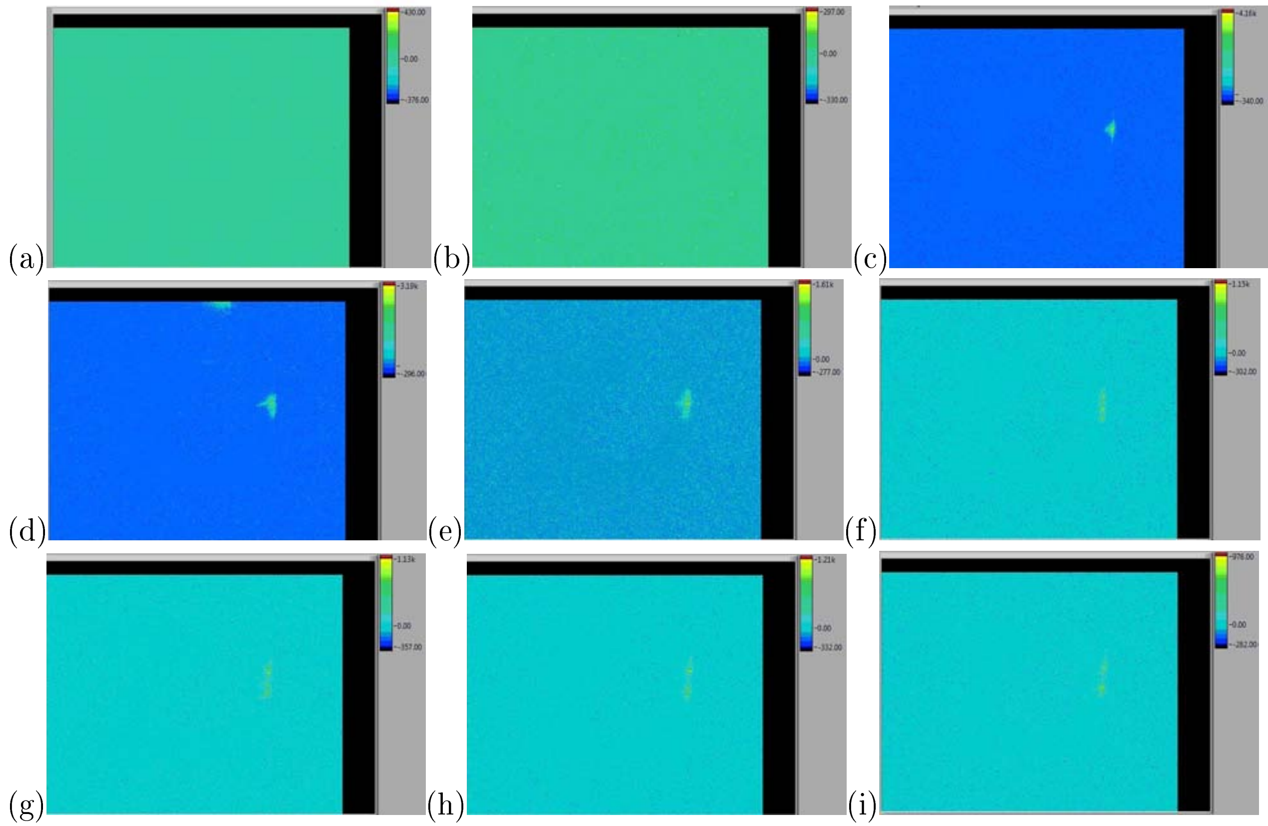


Figure 7.32: *Light emission in correspondence of the last 9 pulses (from a to i) applied to sample7.* V_{line} *goes from 567 to 591 volts.*

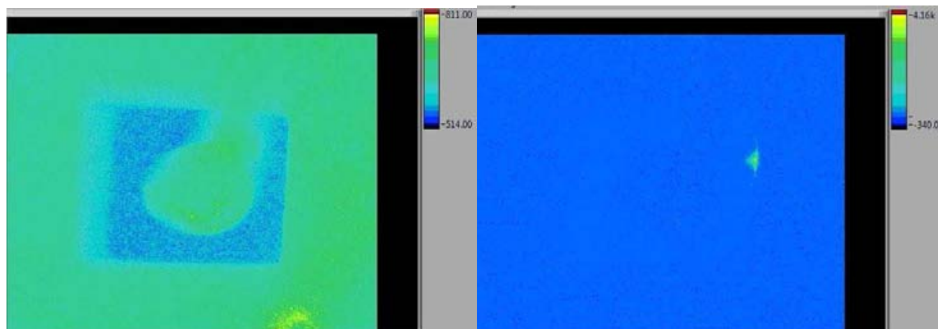


Figure 7.33: *Comparison between an image of the chip with high ambient light and Fig.(7.32)(c). It can be seen that the emissive spot is on the border of the device.*

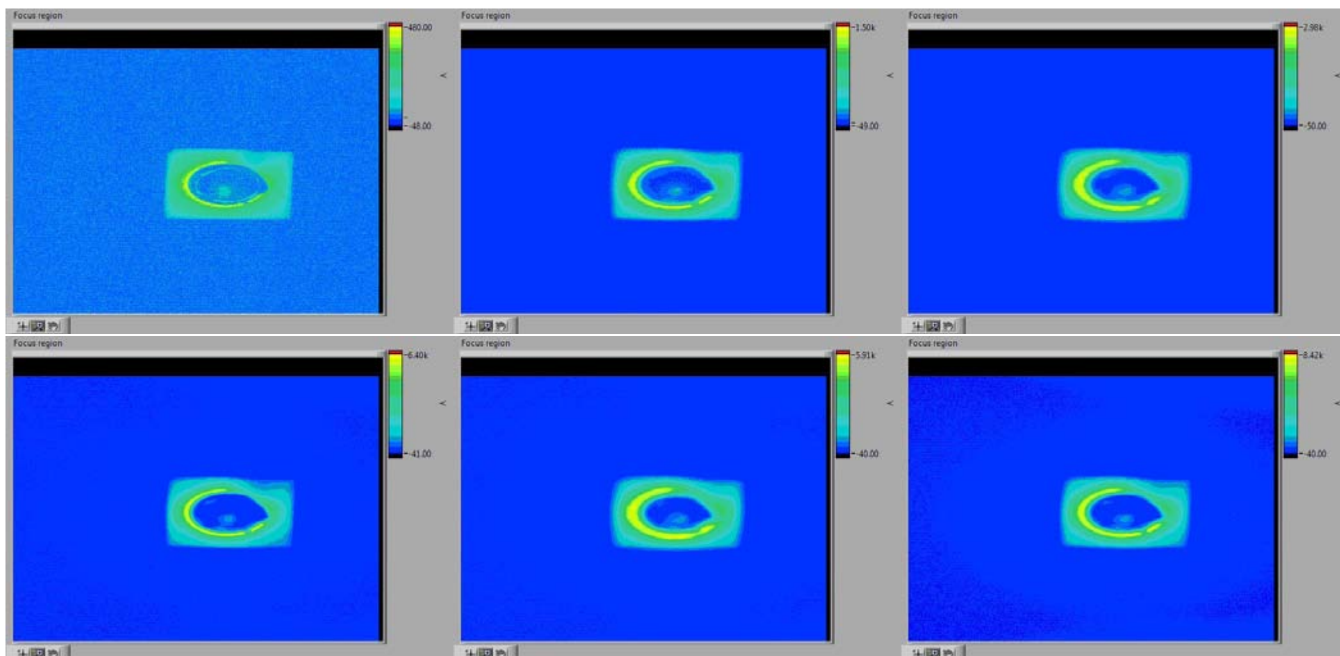


Figure 7.34: *Light emission of a red LED submitted to low amplitude positive TLP-pulses. The images show how the emission varies with the increase of* V_{line}*, whose values are 3, 39,102,201,303 and 402 volts respectively (clockwise).*

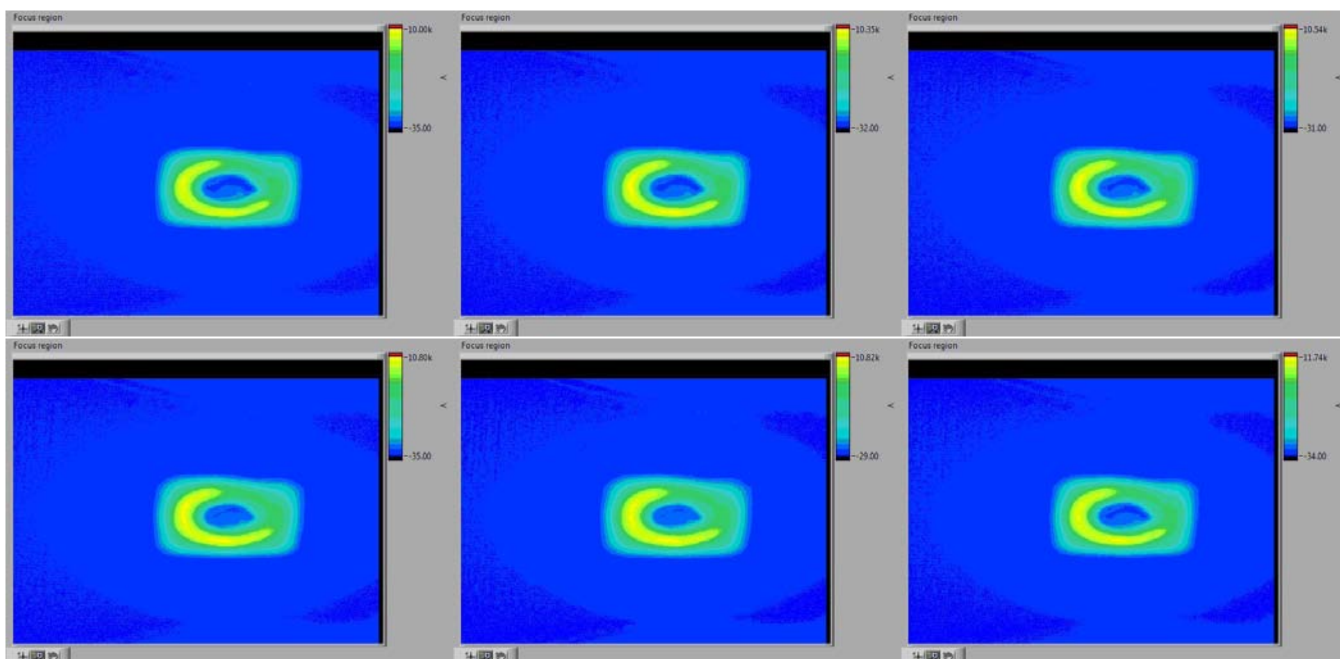


Figure 7.35: *Light emission of a red LED submitted to positive TLP-pulses. The images show how the emission varies with the increase of* V_{line}*. In this case the pulse amplitude is higher. The precharge-voltages are 1401, 1602,1800,2004,2202 and 2301 volts respectively (clockwise).*

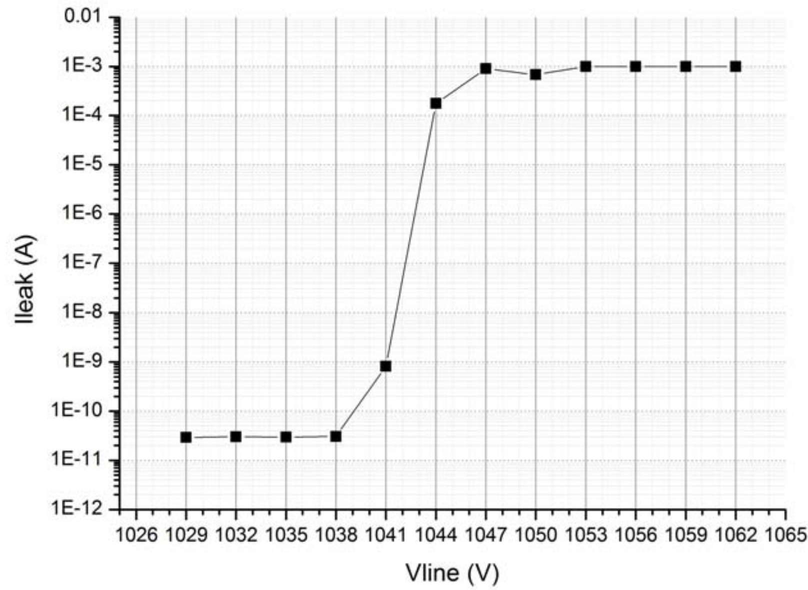


Figure 7.36: *Sample3 leakage current as a function of V_{line}.*

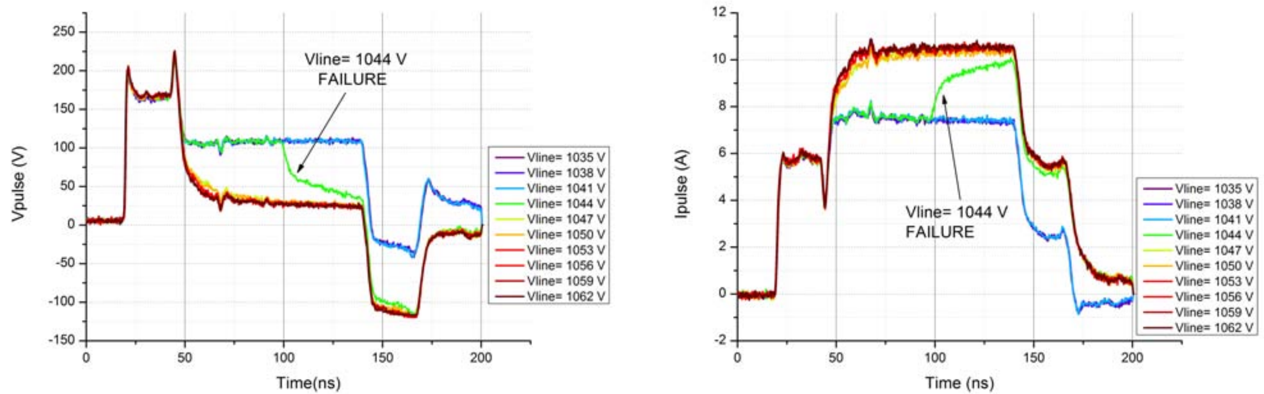


Figure 7.37: *Sample3 pulse waveforms.*

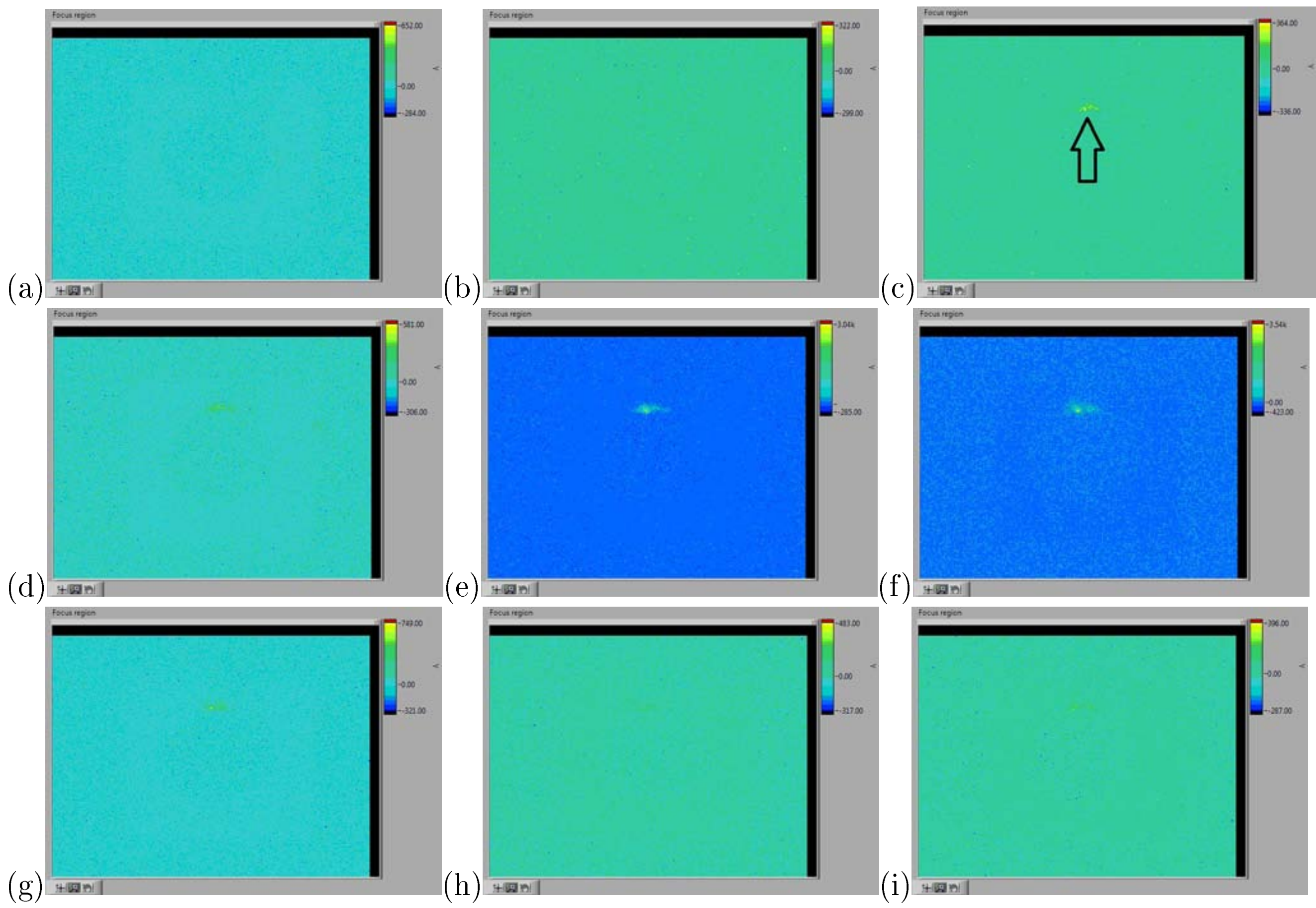


Figure 7.38: *Sample3 luminous emission in correspondence of the applied ESD pulses. The corresponding V_{line} goes from 1038V (a) to 1062V (i), with 3 volts step size . The emission in correspondence of the discharge that causes the failure is shown in (c).*

more the failure of the LED can be identified because of the appearance of luminous emission (V_{line} = 1044V).

An example of a different typology of behaviour is given by *sample4*. In this case, as can be seen in Fig.(7.39), the device degradation can be considered gradual. The leakage current does not abruptly change, but reaches the failure level through some limited increases. Because of this, the change in the pulse waveforms would be expected to be gradual too. Anyway Fig.(7.40) shows that this is not true. In fact there is an abrupt change in the pulse shape after the ESD corresponding to a pre-charge voltage of 1050V. This pulse clearly causes a degradation in the device (the leakage slightly increases and it is possible to observe a small voltage drop in the waveform “tail”). Once the device has been damaged it can not withstand any other pulse, and the new ESD applied makes it fail.

Also in this case it is possible to analyze the light emission during the discharge. Observing the images in Fig.(7.41), it is possible to notice that the light emission is detected for the first time during the ESD corresponding to V_{line} = 1053V. This is very interesting, because it corresponds to the first significant increase in the leakage. Another thing that is important to notice is that the luminous emission is located in a very small region (that can be even much smaller than the bright spot in the images Fig.7.41) near the metal contact. This suggests current crowding as a possible cause of the failure. In fact, as already shown in Fig.(7.34) and (7.35), the absence of a grid-shaped contact strongly influence the current distribution in these devices.

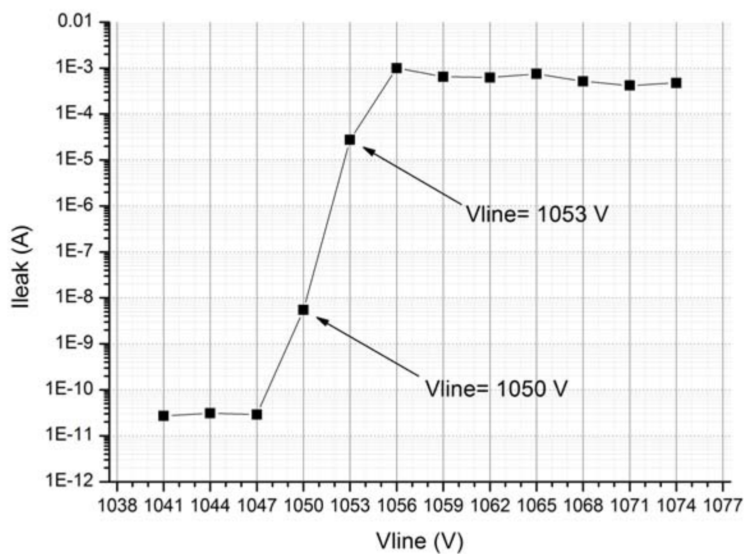


Figure 7.39: *Sample4 leakage current as a function of* V_{line}.

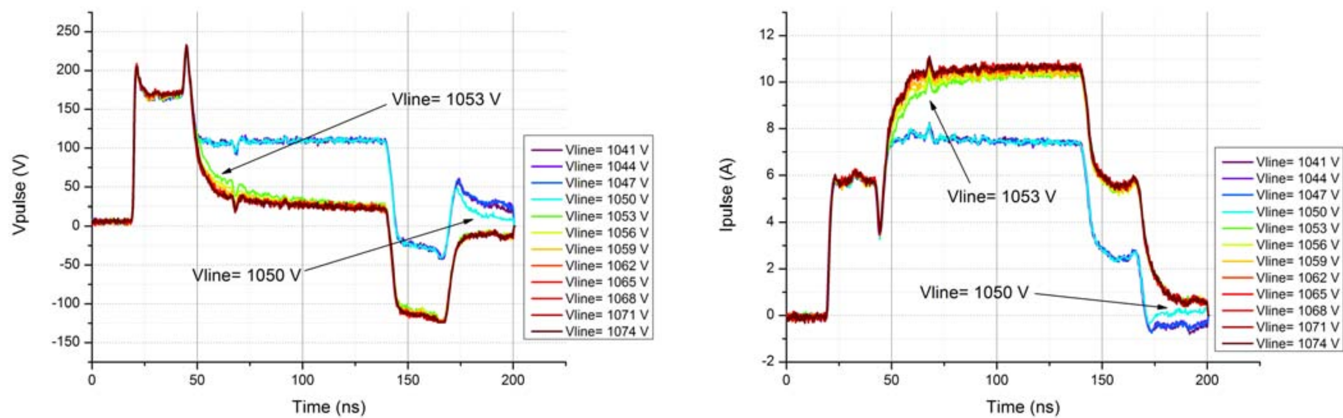


Figure 7.40: *Sample4 pulse voltage and current waveforms.*

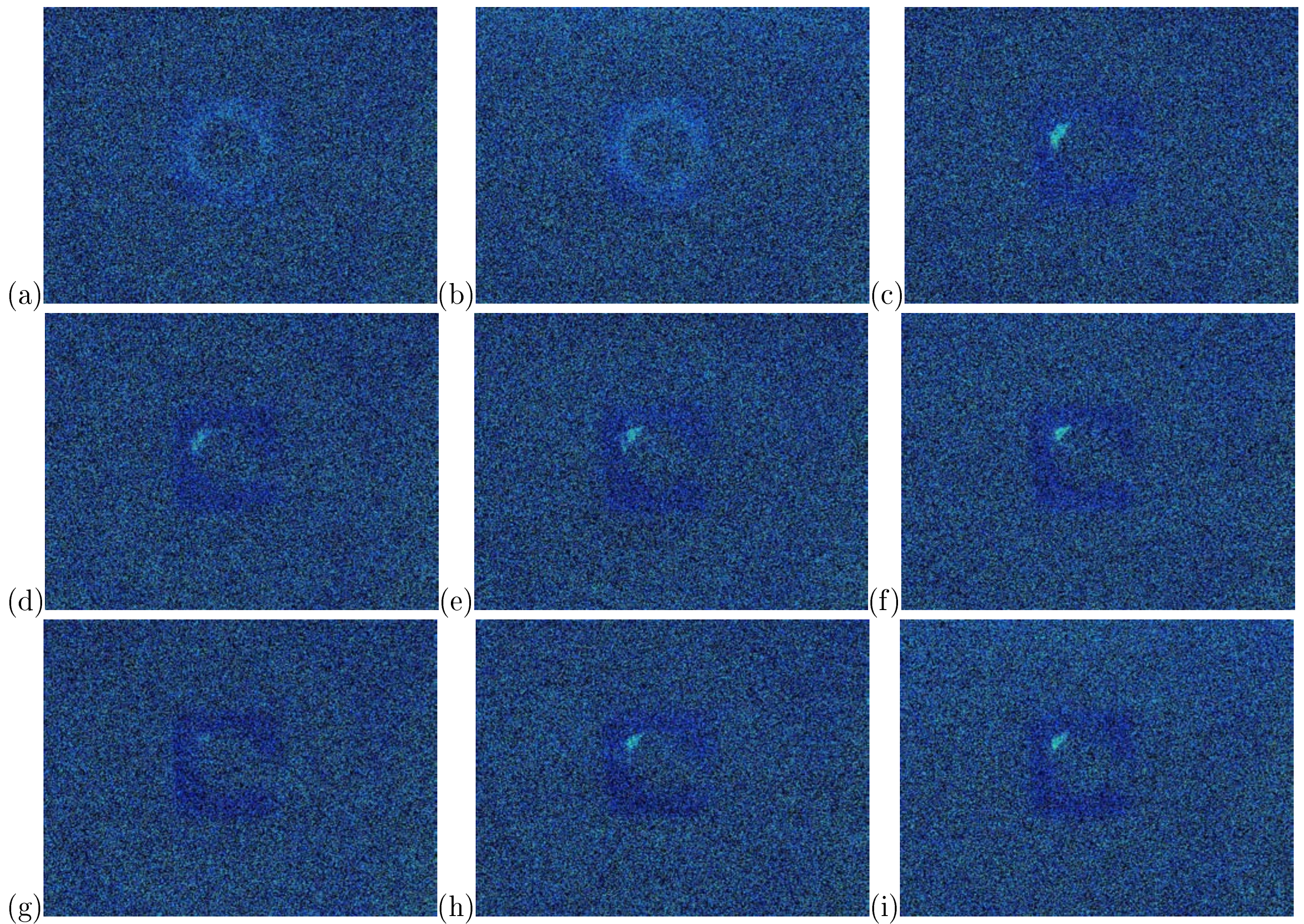


Figure 7.41: *Sample4 luminous emission in correspondence of the applied ESD pulses. The corresponding V_{line} goes from 1047V (a) to 1071V (i), with 3 volts step size . The emission in correspondence of the discharge that causes the failure is shown in (c).*

The data previously shown suggest that the red LEDs behaviour differs significantly from the green LEDs. Even the area were the emission seems to be located is different, despite having the same type of contact on both of the cases.

Chapter 8

LED MODULES ANALYSIS

LED devices are typically connected in series to increase the optical power emitted. Studying the ESD characteristics of the modules is therefore particularly interesting and is also an analysis that has not been done yet. Because of this, in the final part of this work, the robustness of monochromatic LED modules was analyzed.

To do this, the samples were mounted on a board built for the purpose, which allowed to connect up to 20 devices in serie. After a first phase in which series with a different number of LEDs were considered, it was chosen to test modules constituted by 4 LEDs. This choice allowed to study the behaviour of the modules while keeping the testing voltage and time within reasonable values (the voltage source had a limited operating range).

A switching unit allowed to measure the leakage of the LEDs of the chain separately (the evaluation was done at $V_{DUT} = -5$ V), and this information was used to determine the failure of the samples (the criterion remained the same employed also in the analysis shown in Chapter 7 and 6). Monochromatic modules of the three different types of LEDs were tested and the stress-tests were carried out applying TLP pulses with pre-charge voltages V_{line} starting from 0 V and increasing with steps of 3 V. The test was considered concluded after all the LEDs failed. In the following this condition will be referred to as "module failure". During the stresses the I-V curves of the single devices were also measured from time to time, to better characterize the change in the LEDs characteristics. Since they are the ones with the most interesting applications and possible development, an extensive analysis was carried out on the blue LEDs modules, testing more than 30 of them. The analysis on the green and red LEDs modules was instead more limited.

In the following the different types of modules will be analyzed separately, and the different samples of each serie will be referred to as *led0*, *1*, *2* or *3*, with reference to Fig. (8.1).

8.1 GREEN LED MODULES ANALYSIS

This investigation allowed to highlight some intriguing characteristics of the green LED modules. The first thing that is interesting to observe is the pulsed I-V. A typical one is reported in Fig.(8.2). As can be seen, the curve is very similar to the pulsed I-V of the single LEDs; in the modules case anyway, the voltage needed to reach the breakdown is much higher (more than

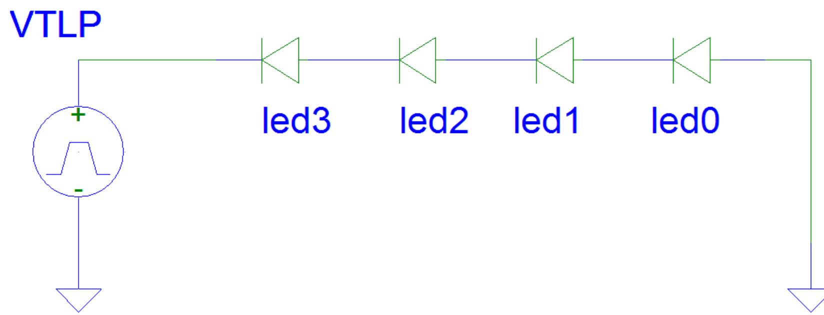


Figure 8.1: *Schematic of the analyzed modules. It is important to remember that the applied pulses where negative with reference to the LEDs biasing.*

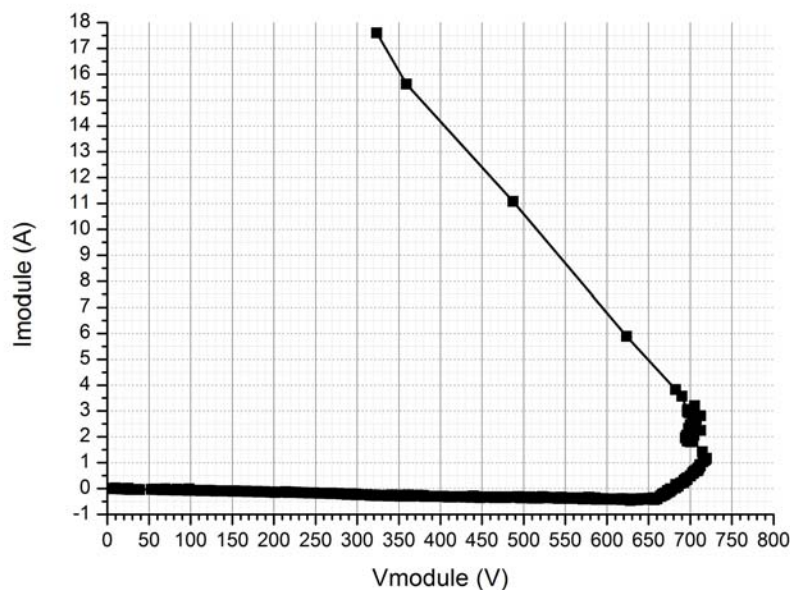


Figure 8.2: *Example of the pulsed I-V of a green LED module.*

four times the voltage needed in the single LED case, that was about 150 V). Another very interesting thing to notice is the discontinuity at about $I_{pulse} = 1.5$ A. This change corresponds to the degradation of one of the LEDs. Despite this, the shape of the curve remains the typical one for the I-V of a LED in the breakdown region. This is very interesting because it means that the module can endure the degradation of one of its LEDs without failing.

A further proof of this fact is given in Fig.(8.3). This image shows the leakage evolution of the LEDs of the so-called *module 4*. The curve reports the leakage current of each device as a function of V_{line}. The pulsed I-V of this module can be seen in Fig. (8.4) and is very similar to the one of Fig. (8.2). Observing Fig. (8.3) it is possible to see how the failure of one of the LEDs did not affect the others, allowing the module to survive. Another very interesting thing that can be seen, is the strange behaviour of *led0*. Its leakage in fact, has an abrupt increase at about $V_{line} = 1450$ V reaching the failure level, but after that it decreases and remains stable. It becomes higher than the failure threshold again, but just in proximity of the module failure. This behaviour was encountered also in another module and in general, a non-monotone leakage was

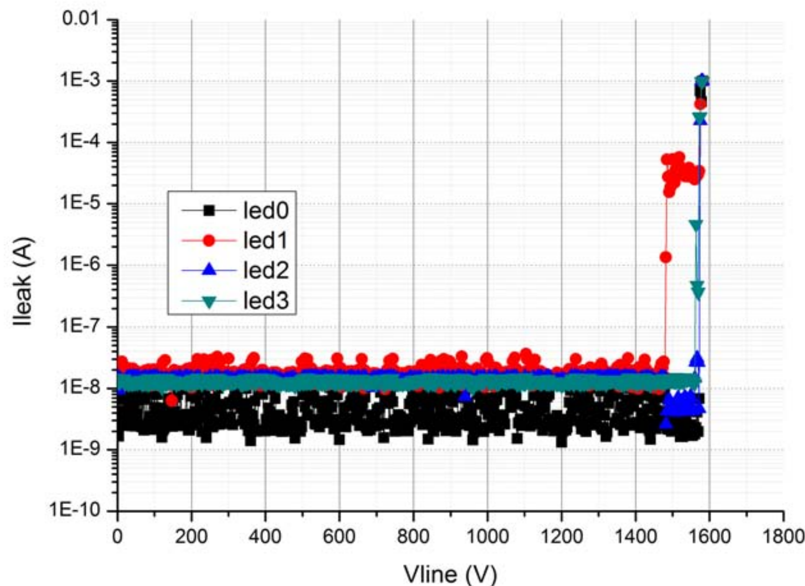


Figure 8.3: *Module 4 single LEDs leakage current as a function of the TLP pre-charge voltage.*

observed in other cases too. A possible explanation of this phenomenon can be the destruction of some of the old parasitic leakage paths due to the ESDs, and the consequent creation of new ones.

Another example of what has been previously shown about the modules robustness, is given by *module 5* and can be clearly seen observing its LEDs leakage current as a function of V_{line}, Fig. (8.5) . Also in this case the degradation of *led1* does not compromise the module robustness. Even a more deeper investigation, obtained analyzing the ESD-pulse waveforms, Fig. (8.6), confirms that the degradation of this LED seems to have little effect on the module ESD-withstand capability. In fact, there is no significant change in the pulse waveforms in correspondence of this event.

Things are much different when also *led3* degrades. After this event, waveforms start to change significantly, Fig.(8.7). It can be said in fact, that this event marks the beginning of the degradation process that brings to the module failure. This is particularly clear looking at Fig. (8.8), where the pulse waveforms corresponding to the last 5 ESDs are reported. It is important to notice that these waveforms refer to the discharges that come immediately after the ones of Fig. (8.7).

Analyzing the pulse waveforms of *module 4* yields similar informations. In fact, as can be seen in Fig. (8.9), the degradation of *led0* seems not to cause a change in the pulse waveforms.

On the other hand, when the module starts to degrade, the pulse shape is strongly modified. The current starts increasing significantly and the voltage starts decreasing. The module failure is marked by a dramatic increase in the current, whose peak reaches values higher than 20A.

A further overview of the green modules behaviour can be given by analyzing *module6*. Fig. (8.12) gives a global overview of the single LEDs leakage currents evolution. In this case, the behaviour is not so clear. To better understand it an expanded view of the curves can be considered, Fig.(8.13).

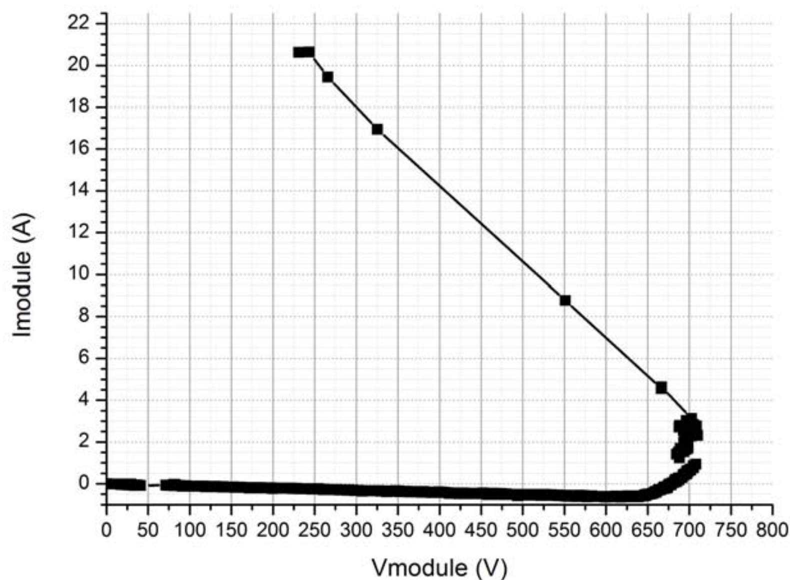


Figure 8.4: *Module 4 pulsed I-V.*

Figure 8.5: *Module 5 LEDs leakage currents as a function of V_{line}. Because the current values were similar to the the sensibility of the instrument, in some cases the measured values were negative. Because of this the leakage current values had to be considered in module, otherwise they could have not been represented on a logarithmic scale.*

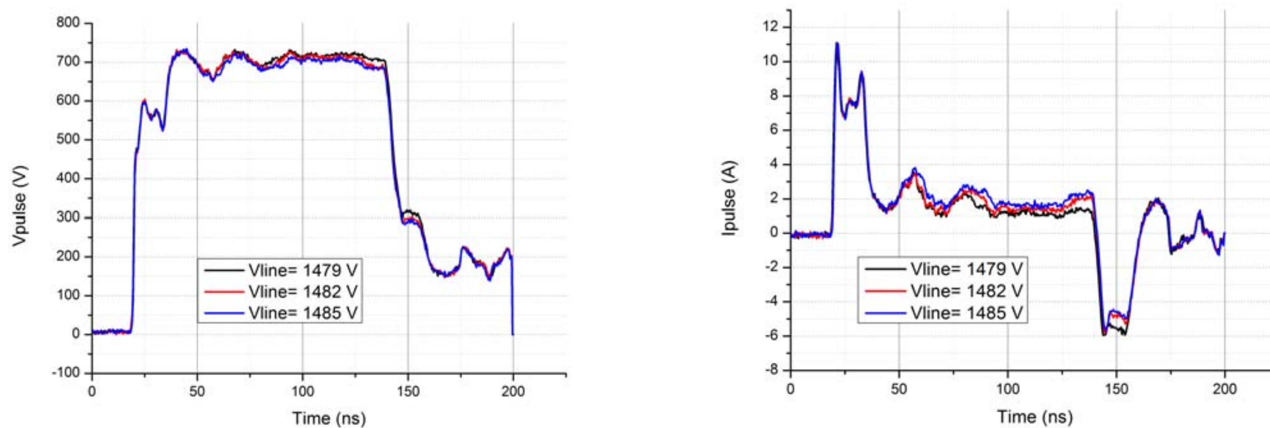


Figure 8.6: *Pulse voltage and current waveforms in correspondence of led1 degradation ($V_{line} =$ 1482 V).*

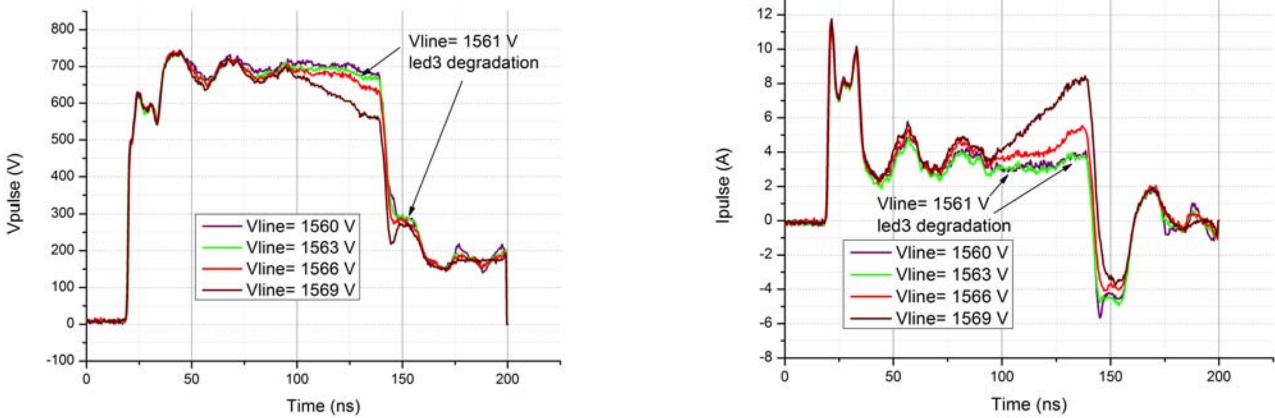


Figure 8.7: *Module 5 pulse voltage and current waveforms in correspondence of led3 degradation.*

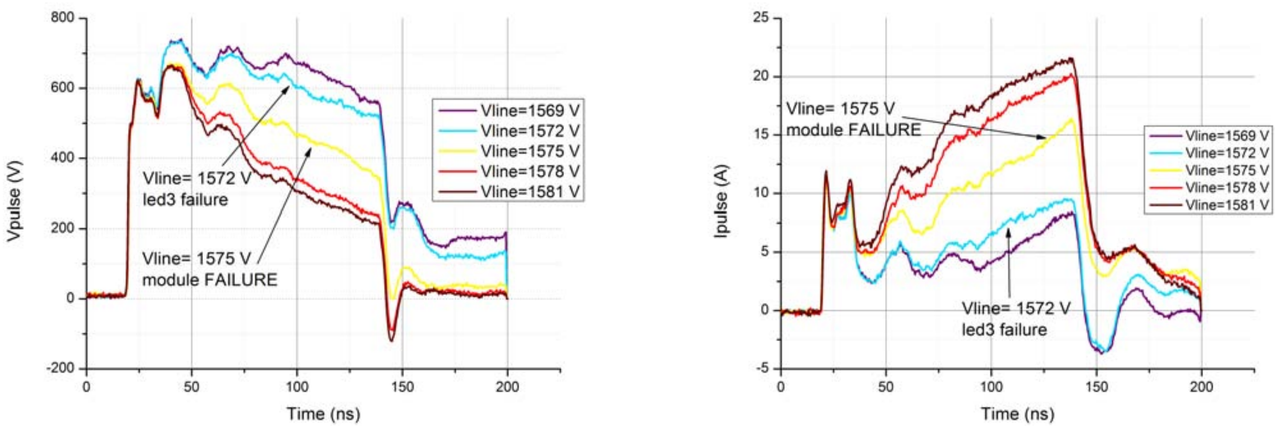


Figure 8.8: *Module 5 degradation and failure: corespondent pulse voltage and current waveforms.*

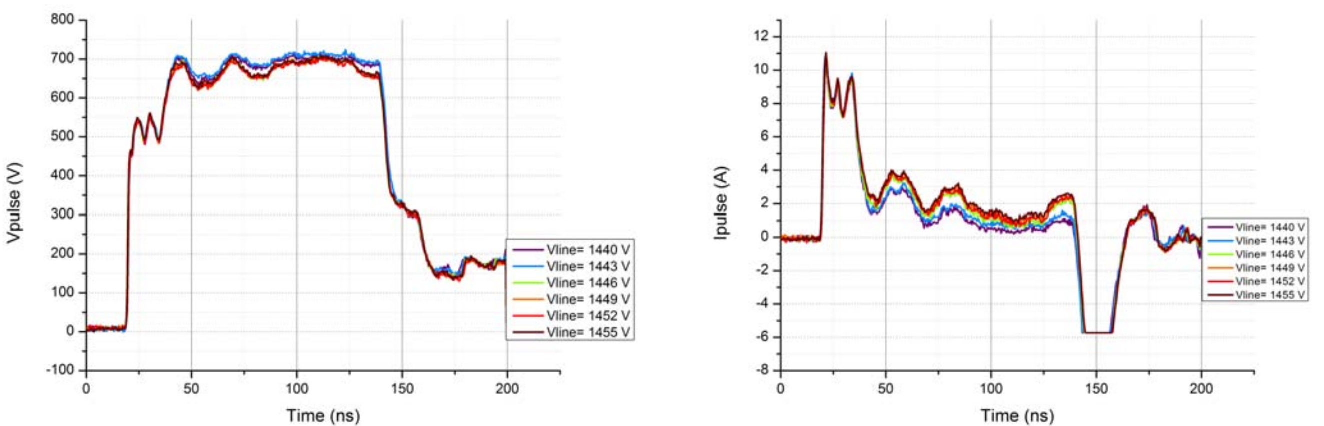


Figure 8.9: *Module 4 pulse waveforms in correspondence of led0 degradation.*

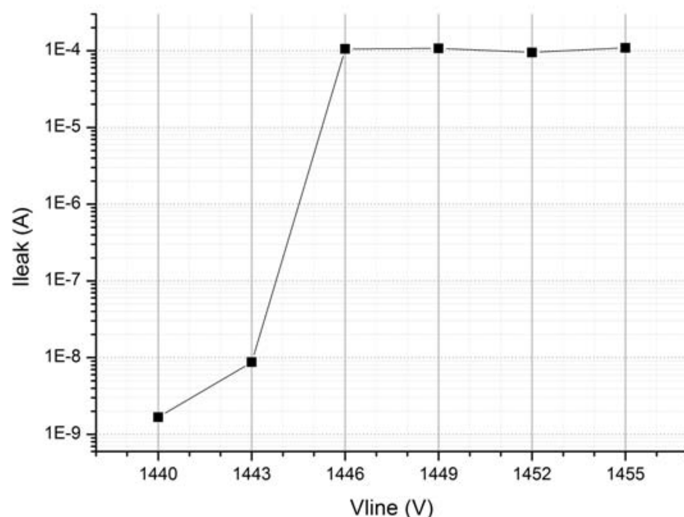


Figure 8.10: *Led0 leakage current in correspondence of the device degradation.*

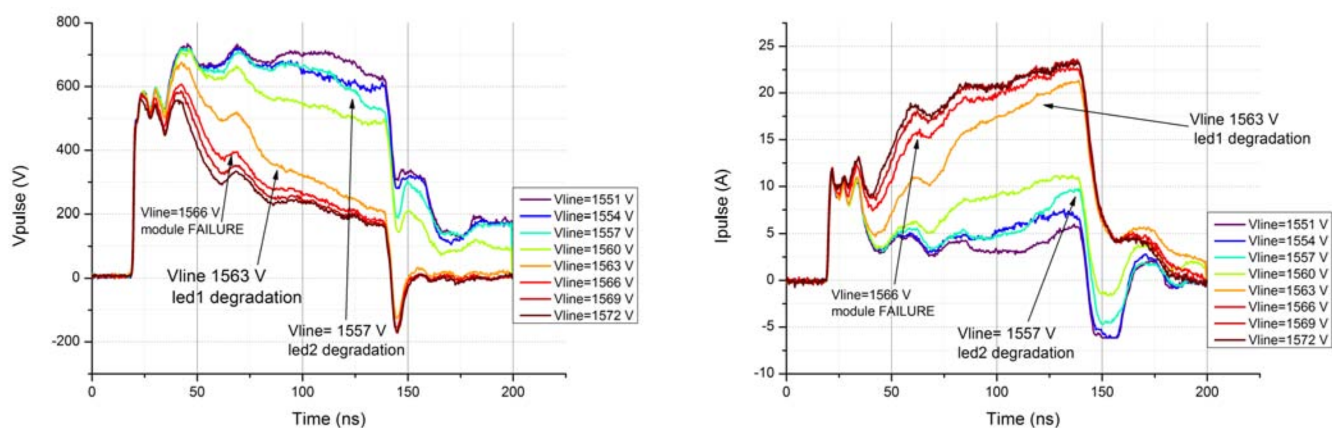


Figure 8.11: *Module 4 degradation and failure: corespondent pulse voltage and current waveforms.*

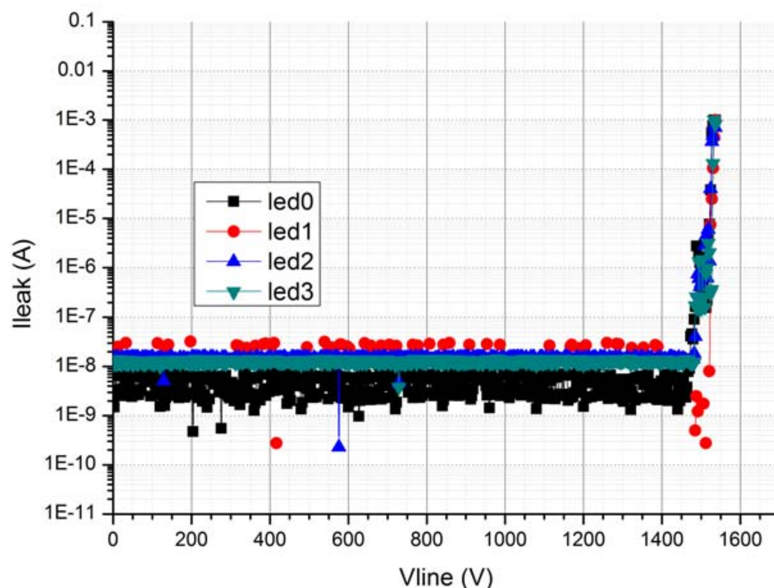


Figure 8.12: *Module 6 single LEDs leakage current as a function of* V_{line}.

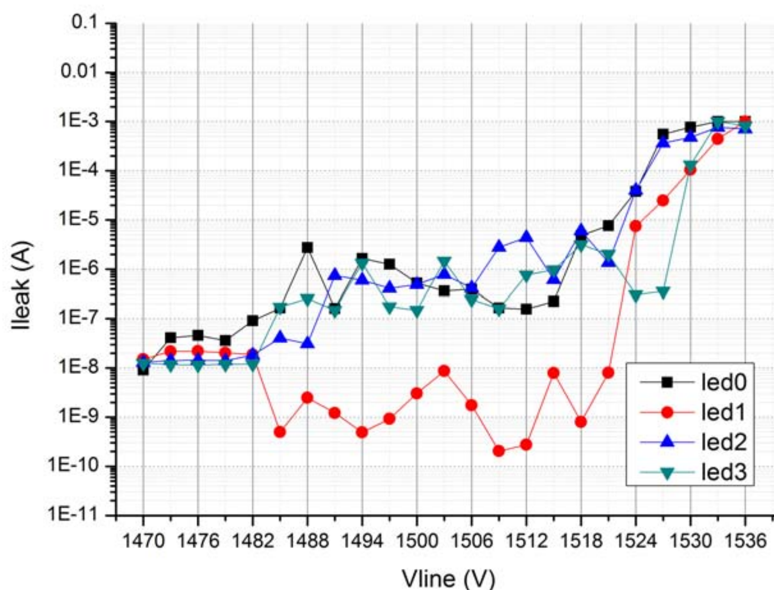


Figure 8.13: *Expanded view of module 6 LEDs leakage. Because the current values were similar to the the sensibility of the instrument, in some cases the measured values were negative. Because of this the leakage current values had to be considered in module, otherwise they could have not been represented on a logarithmic scale.*

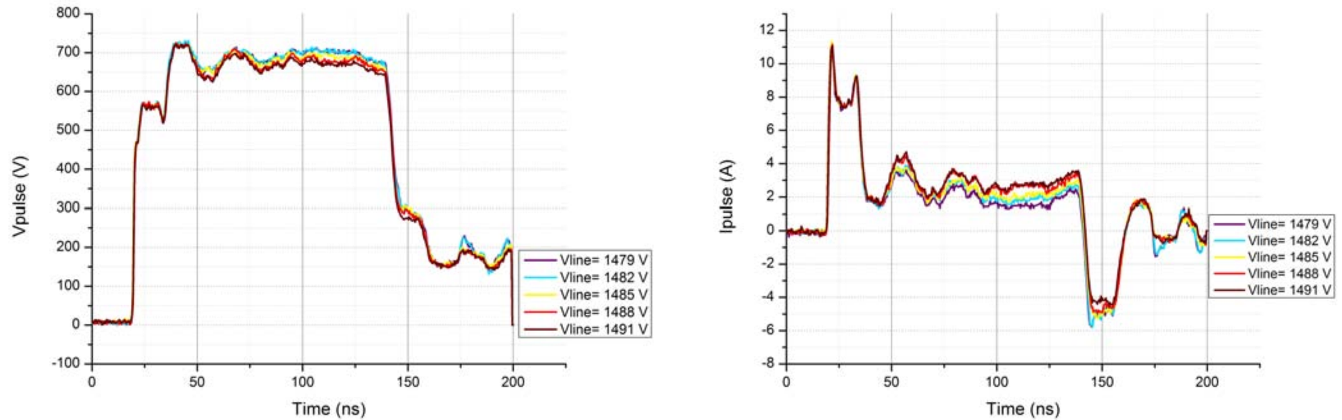


Figure 8.14: *Pulse voltage and current waveforms in proximity and correspondence of the beginning of the degradation process (it starts at $V_{line} = 1485$ V).*

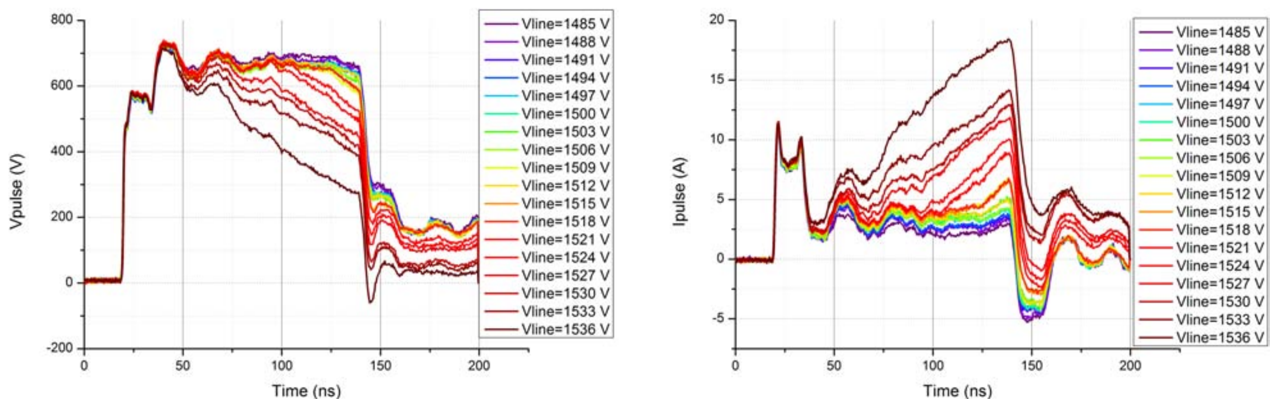


Figure 8.15: *Pulse voltage and current waveforms as a function of the TLP pre-charge voltage. $V_{line} = 1536$ V corresponds to the last pulse of the stress-test. $V_{line} = 1530$ V corresponds to the module failure.*

Also in this case it can be seen that the degradation of one device (even more than one this time) does not immediately affect the module. In fact a significant number of ESDs are needed after the first degradation of one of the LEDs, to make the module fail. Also the waveform analysis confirms this. Studying the pulses shape after the beginning of the degradation process (Fig. (8.14)), it is possible to notice that the first degradation of *led0* and *led3* (highlighted by the increase of their leakage currents, $V_{line} = 1485$ V) does not produce significant alterations in the corespondent waveforms.

An overview of the evolution of the pulse waveforms as the degradation process takes place, can be seen in Fig. (8.15).

This degradation is similar to the one already seen for modules *4* and *5*. Considering just the pulses corresponding to the last ten ESDs applied to the module during the stress-test we obtain the graphs of Fig. (8.16), where the leakage currents are also shown. It can be seen that the pulse waveforms remain quite stable while V_{line} is lower than 1518 V. After that the single devices are too degraded and even *led1*, that had previously remained untouched, fails.

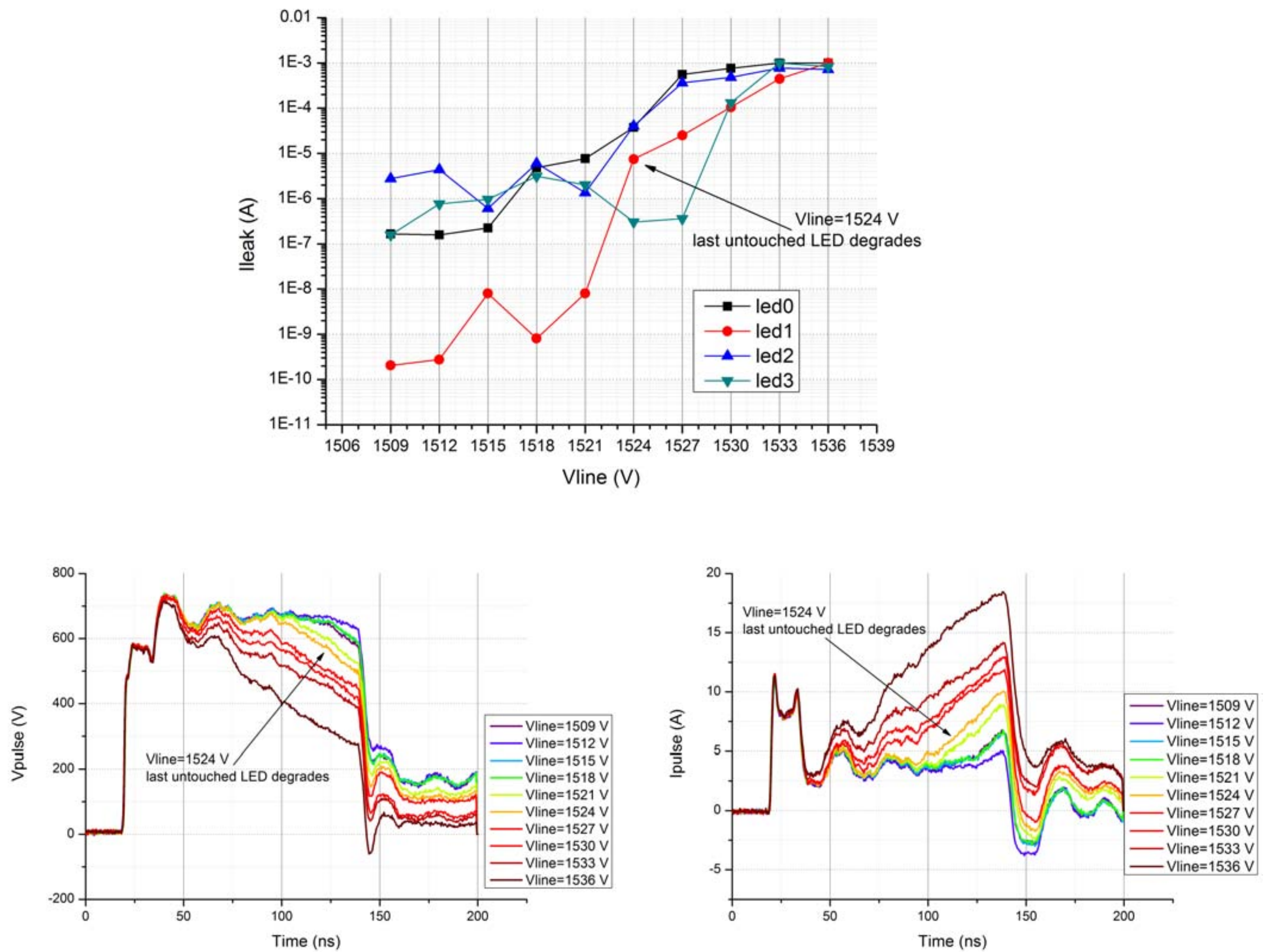


Figure 8.16: *LEDs leakage and pulse waveforms corresponding to the last ten ESDs applied to the module during the stress-test.*

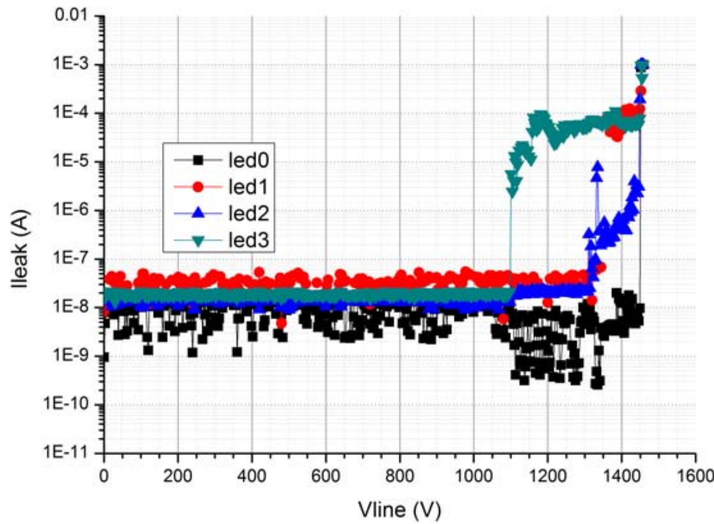


Figure 8.17: *Module 3: the single LEDs leakage current as a function of* V_{line}.

	$V_{pre-deg}$ [V]	V_{deg} [V]	$I_{pre-deg}$ [A]	I_{deg} [A]	$V_{pre-fail}$ [V]	V_{fail} [V]	$I_{pre-fail}$ [A]	I_{fail} [A]
Max.	719.30	714.57	1.996	2.190	623.67	578.41	16.935	19.438
Min.	551.14	554.55	0.049	0.161	325.52	265.95	5.884	7.010
Mean	677.33	669.10	0.977	1.251	543.07	460.96	8.364	11.426
std. dev.	70.93	64.89	0.707	0.725	123.76	116.25	4.797	4.775

Table 8.1: *Statistical summary of green LED modules characteristics.*

Finally, a further evidence of the fact that the module can withstand the degradation of one of the LEDs is given by Fig. (8.17), that shows the leakage of the devices of what was called *module3*.

This investigation was mainly about modules behaviour, but it gave some useful informations about the single LEDs too. In particular it highlighted the gradual degradation that often characterize these devices. The most blatant example of this, is given by LED2 of *module 3*, whose I-V curves measured during the stress are shown in Fig. (8.18).

A summary of the data obtained through this investigation are shown in Fig. (8.19) and Table (8.1) and (8.2), where V_{deg} and I_{deg} are the voltage and current of the ESD that causes the first degradation (or failure) of a LED of the module, while $V_{pre-deg}$and $I_{pre-deg}$ are the voltage and current of the pulse before. $V_{fail}/V_{pre-fail}$ and $I_{fail}/I_{pre-fail}$ are instead the voltage and current of the pulse that causes the module failure and the one before.

Comparing the data of Table (8.1) with ones in Table (6.2), that refers to the single LEDs testing, some interesting informations can be deduced. First of all, it seems that being in a module does not make a LED more resistant to the pulse current. In fact, the average current that the module can withstand before having the degradation of one of its LEDs takes place, is 0.977A. The same parameter in the single LED case was 3.40 A. Anyway, considering the average current that the module can withstand before failing, things improve (as expected). In fact, the average maximum current that the green modules could withstand was 8.364 A (while

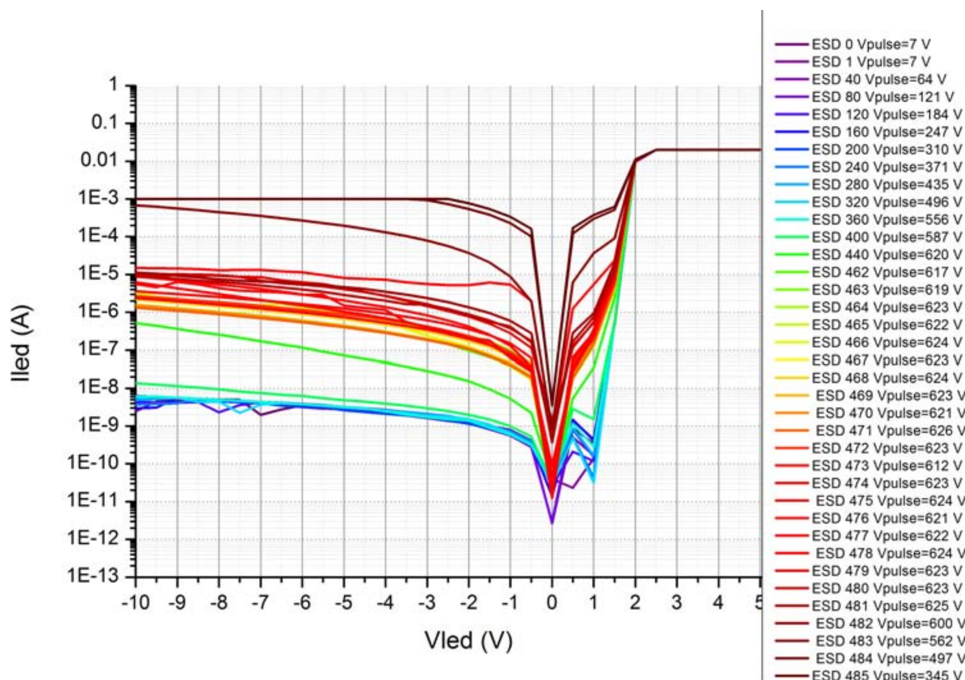


Figure 8.18: *The measured I-V curves of LED2 in module 3. It can be seen the gradual degradation as the pulse amplitude increases.*

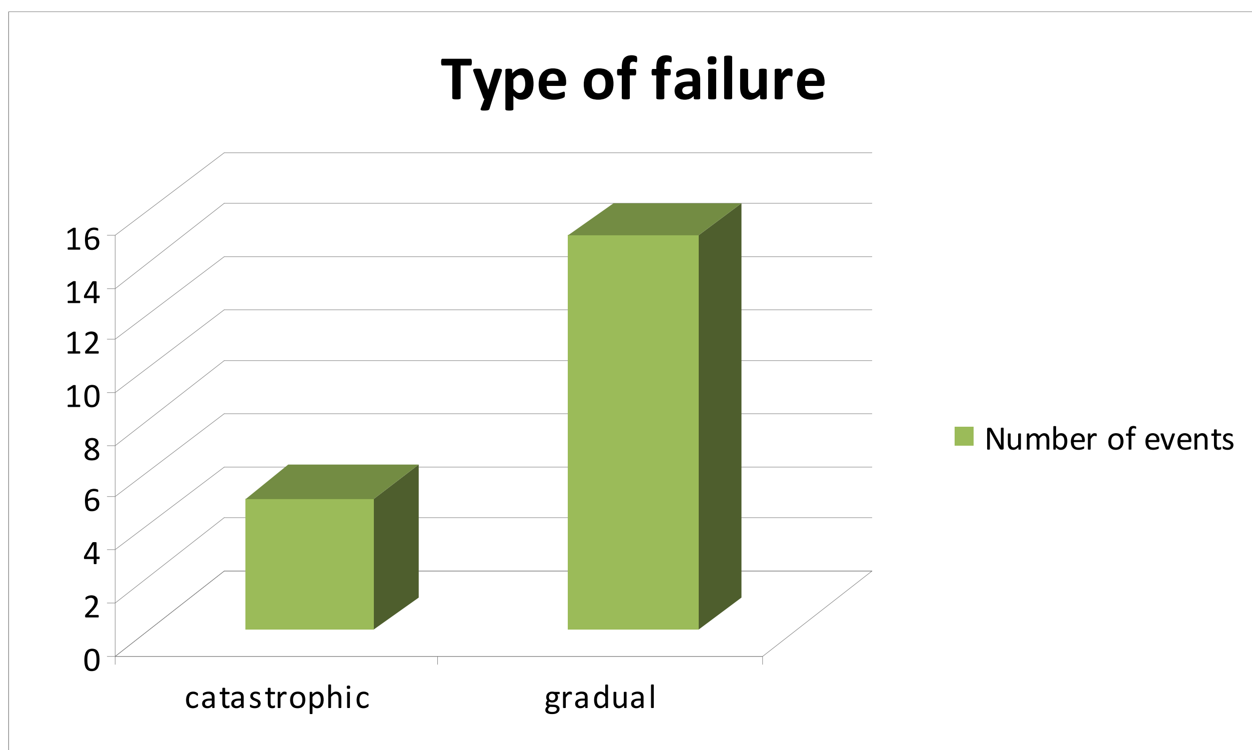


Figure 8.19: *Green modules LEDs type of failure.*

Type of failure	Catastrophic	Gradual
Percentage	25%	75%

Table 8.2: *Statistical summary of the single green LEDs type of failure during the module testing.*

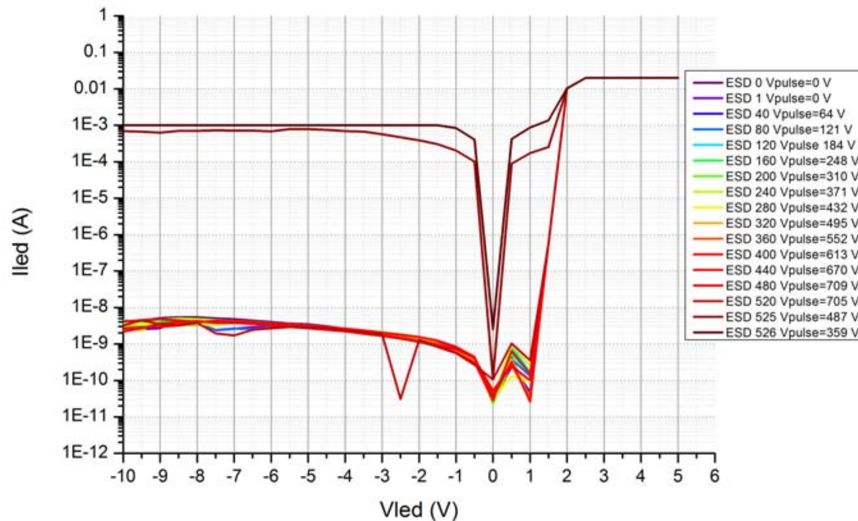


Figure 8.20: *The measured I-V curves of LED2 in module 5. Example of catastrophic failure.*

in the single LEDs case it was 7.28A). The module is therefore more robust, but not as much as expected.

The average ESD-voltage withstanding capability is instead of about 543 V. This is a good result but it cannot be compared with the single LEDs one, because in that case the pulse voltage started to drop when the degradation of the sample occurred. Using the maximum voltage that the single device could stand before degrading for a comparison, it is possible to notice that the module shows a much improved robustness, about 543 versus 172.4 V.

These data also show that the green LEDs tend to fail gradually when in modules. Despite this, catastrophic failure sometimes occurs too. An example of the I-V of a green sample which failed in a catastrophic way is given in Fig. (8.20).

8.2 RED LED MODULES ANALYSIS

One of the main properties of the green modules was their capability of surviving the degradation of one of their LEDs. This characteristic is not present in the red ones. In these modules in fact the single LEDs tend to fail and degrade together, leading directly (or in a very small number of ESDs) to the module failure. This characteristic was detected in all the tested modules (at maximum 5 ESDs from the first degradation of one of the LEDs of the serie were needed to make the module fail).

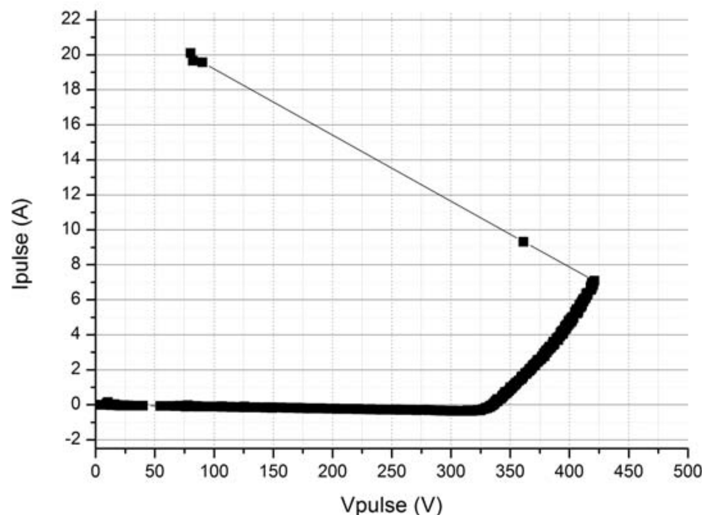


Figure 8.21: *Module 5 pulsed I-V.*

An example of this behaviour can be seen analyzing the data regarding the stress-test of the so-called *module5*. Observing the pulsed I-V in Fig.(8.21), it is possible to notice that the module seems to have a sudden and catastrophic failure, characterized by an incredibly high increase in the pulse current.

A further proof of what previously said is given also by the leakage currents curves, Fig. (8.22). There is no sign of degradation before the failure. Even a closer look at these curves (Fig. (8.23)) confirms it.

At this point it is very interesting to analyze the pulse waveforms, in order to understand what happens exactly during the failure. In Fig.(8.24) it is possible to see the way these waveforms change as the module degrades.

These images are the final proof that was needed. The moment in which the module fails can be clearly identified with the current peak at V_{line} = 1212 V. The fact that this waveform corresponds to the degradation or failure of all the LEDs of the module, confirms what has been previously said. Comparing the peak value before and after that pulse, we can see that it has more than doubled.

To prove this behaviour further, the waveforms corresponding to the failure of some other modules will be also shown. In Fig. (8.25) the waveforms corresponding to *module 1* testing can be observed.

Also in this case the moment in which the module degradation takes place can be clearly identified (V_{ine} = 1209 V). After this pulse the module is so deeply damaged that the next stress makes it fail.

Another example is given by *module 4*. Even in this case, the moment the module degrades and fails is clearly detectable observing the pulse waveforms, Fig. (8.26).

The only case in which the module seemed to need a higher number of stresses to fail after the degradation process had begun, was the one of *module2*. The correspondent leakage currents curves and pulse waveforms can be seen Fig. (8.28) and (8.29) respectively. It is particularly

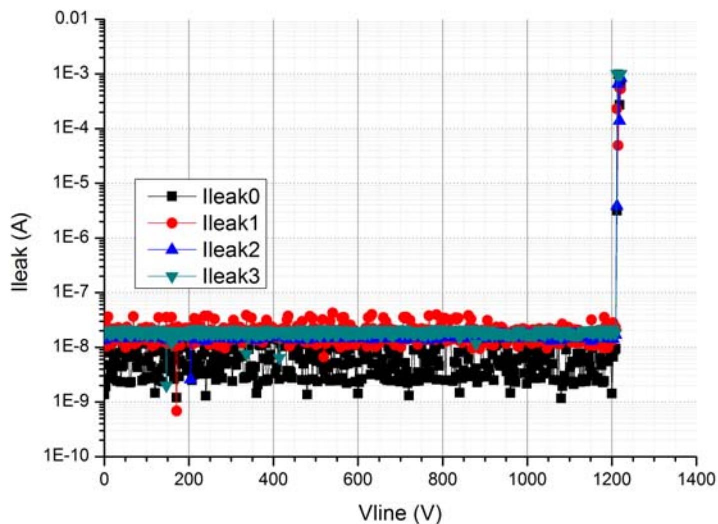


Figure 8.22: *The leakage currents of the single LEDs of module 5.*

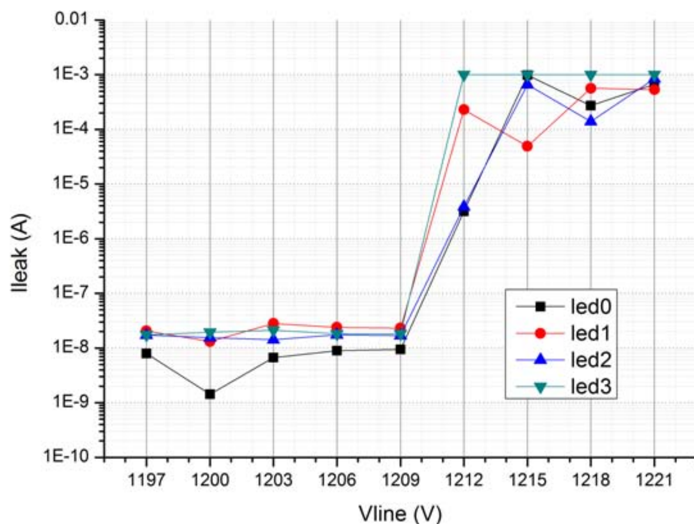


Figure 8.23: *Expanded view of module 5 LEDs leakage. Because the current values were similar to the the sensibility of measurement system, in some cases the measured values were negative. Because of this the leakage current values had to be considered in module, otherwise they could have not been represented on a logarithmic scale.*

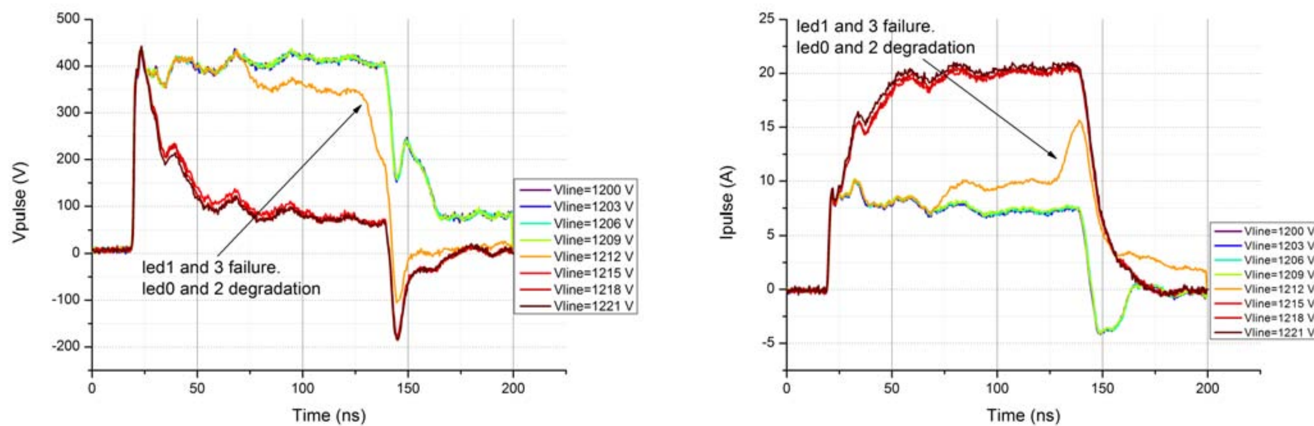


Figure 8.24: *Module5: pulse voltage and current waveforms evolution as the module degrades.*

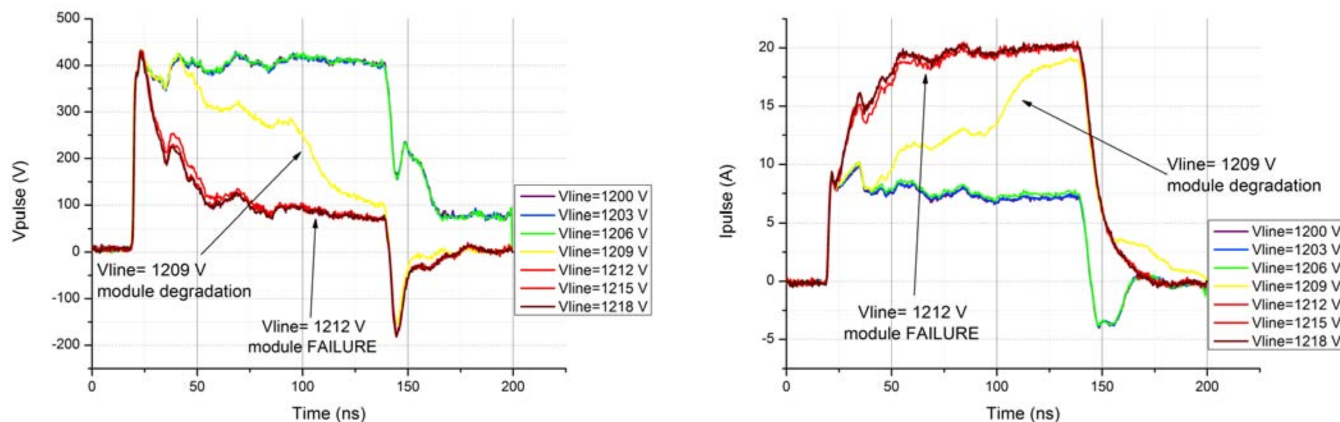


Figure 8.25: *Pulse voltage and current waveforms alteration as module 1 degrades.*

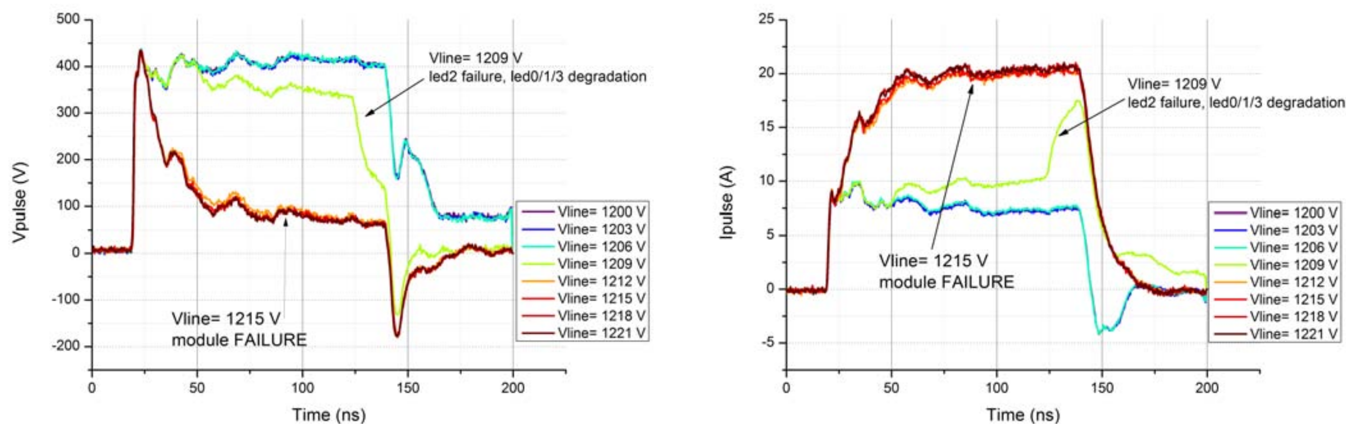


Figure 8.26: *Module4: pulse voltage and current waveforms evolution as the module degrades*

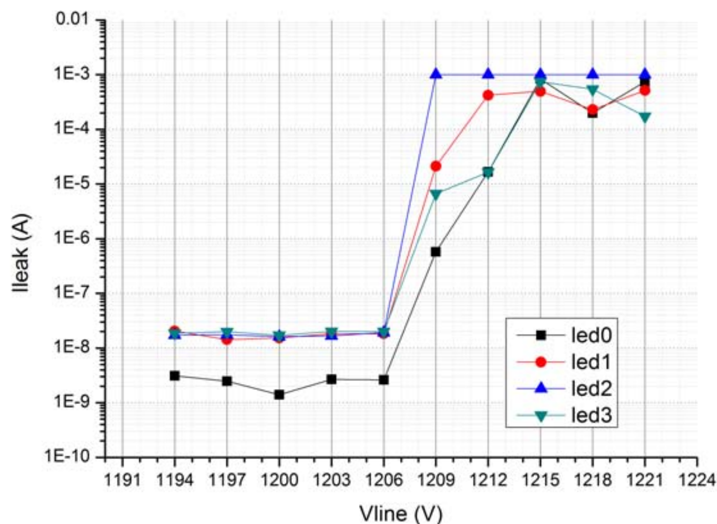


Figure 8.27: *Expanded view of module 4 LEDs leakage. Because the current values were similar to the the sensibility of the measurement system, in some cases the measured values were negative. Because of this the leakage current values had to be considered in module, otherwise they could have not been represented on a logarithmic scale.*

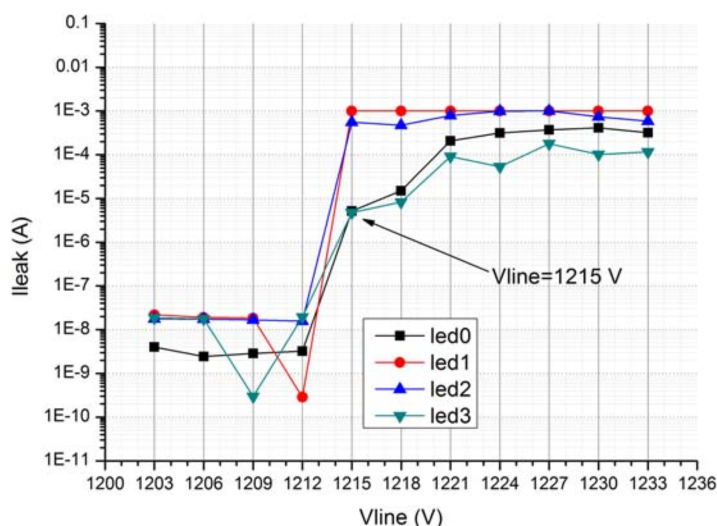


Figure 8.28: *Expanded view of module 2 LEDs leakage. Because the current values were similar to the the sensibility of the measurement system, in some cases the measured values were negative. Because of this the leakage current values had to be considered in module, otherwise they could have not been represented on a logarithmic scale.*

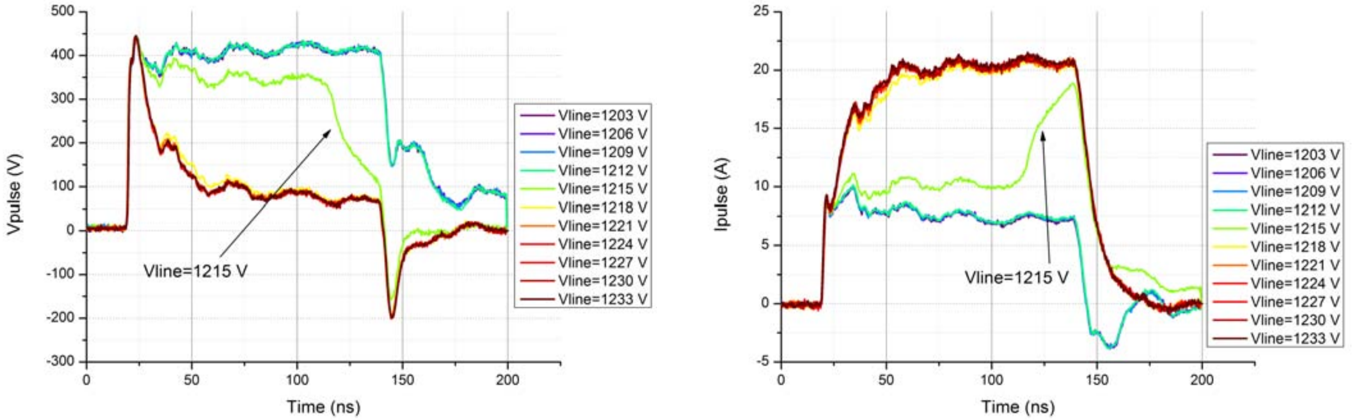


Figure 8.29: *Module2: pulse voltage and current waveforms evolution as the module degrades.*

	$V_{pre-deg}$ [V]	V_{deg} [V]	$I_{pre-deg}$ [A]	I_{deg} [A]	$I_{pre-fail}$ [A]	I_{fail} [A]
Max.	421.332	361.225	7.319	17.690	20.224	19.596
Min.	414.374	140.502	7.084	9.317	12.861	20.272
Mean	418.182	292.254	7.214	11.906	17.954	19.180
std. dev.	3.3923	92.9425	0.0916	3.5296	3.0096	0.4301

Table 8.3: *Statistical summary of red LED modules characteristics.*

interesting to observe that the leakage current of *led3* needs 5 ESD pulses after the degradation to get to the failure threshold. Despite this, the pulse waveforms change abruptly in correspondence of the ESD marked as "V_{line} = 1215 V". Therefore, the module seems once again to fail in a very abrupt way, as the very high increase in the pulse current confirms.

The results of the investigation on the red LED modules are summarized in Table (8.3). V_{deg} and I_{deg} are the voltage and current of the ESD that causes the first degradation (or failure) of a LED of the module, while $V_{pre-deg}$and $I_{pre-deg}$ are the voltage and current of the pulse before. $I_{fail}/I_{pre-fail}$ are instead the voltage and current of the pulse that causes the module failure and the one before. Since most of the modules failed in just a couple of pulses and after the first degradation the voltage rapidly dropped, the value of the pulse voltage before and in correspondence of the failure was not reported.

The most interesting data are $V_{pre-deg}$and $I_{pre-deg}$. In fact, since it has been showed that after the initial degradation the module is already deeply damaged, these are the robustness levels of the red modules. Similarly to the green LED modules, if compared to the single devices, the module does not seem to have a higher ESD-current robustness level (the mean values is even lower actually, 7.21 versus 7.47A). Anyway this is consistent with what has been previously observed (also in Chapter 6), since these devices seem to have a threshold current value after which they fail. On the other hand, considering the maximum pulse voltage amplitude that the module can withstand, it is about four times the value of the same parameter in the single LEDs case (the mean values are about 418 and 103V respectively).

Another important thing to observe is that, as already noticed for the single devices, even the

red LED modules seem to have very stable properties.

As previously done for the green modules, even from the tests on the red ones we can deduce some informations about the single LEDs type of failure, Fig. (8.30) and Table (8.4).

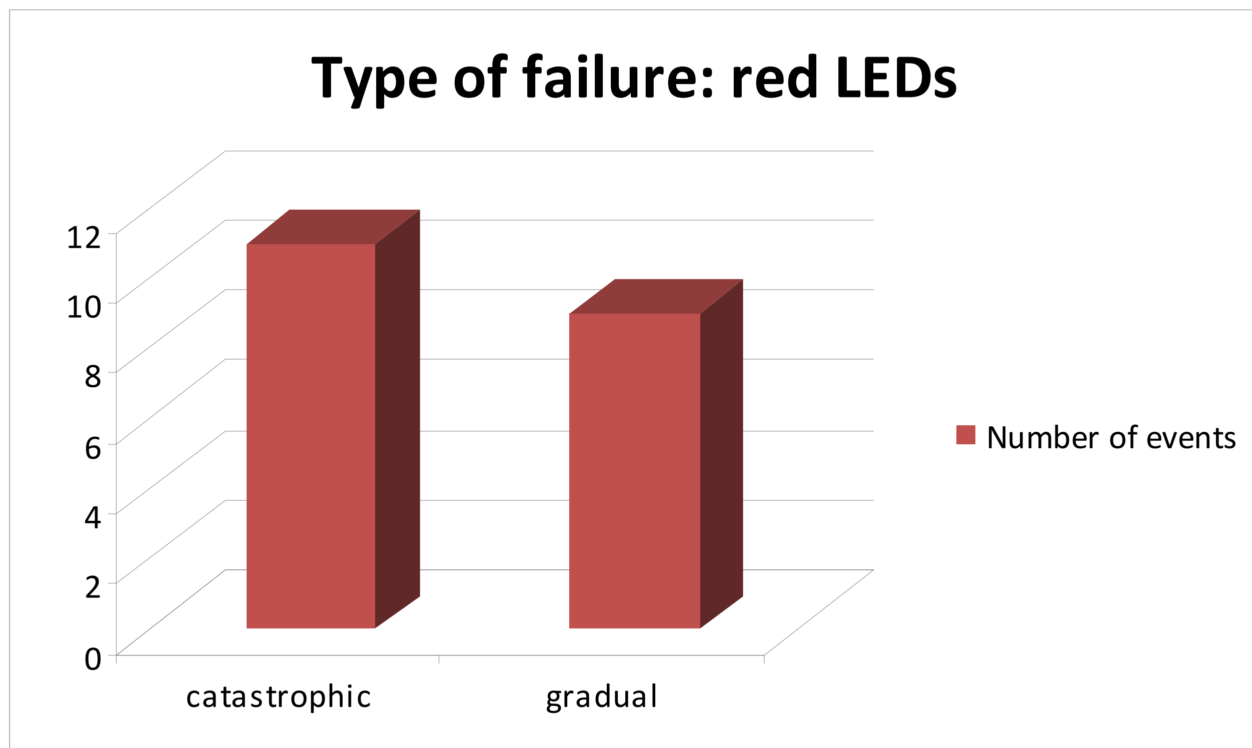


Figure 8.30: *Summary of the single red LEDs type of failure during the module testing.*

Type of failure	catastrophic	gradual
percentage	55%	45%

Table 8.4: *Statistical summary of the single red LEDs type of failure during the module testing.*

In particular it can be observed that the red devices can fail in both catastrophic and gradual way with very similar probability.

8.3 BLUE LED MODULES ANALYSIS

The blue LEDs modules are the most interesting ones. In fact blue LEDs are highly used for illumination purposes, an application field that could determine a huge expansion of the LEDs market. Moreover, these devices also showed highly variable properties and, as will be shown in the following, they used to fail separately one from the other when in module. Because of these (and other) reasons, the blue modules were studied more in depth, and an extended statistical analysis of their properties was carried out.

The first characteristic that this investigation allowed to notice is that, as in the green LED modules case, the failure of one of the LEDs does not compromise the module robustness. In

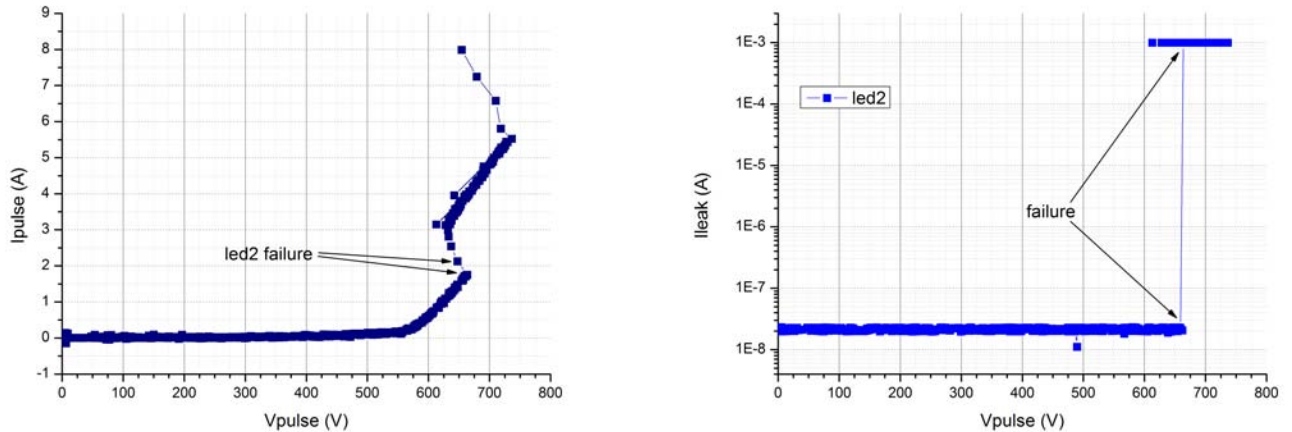


Figure 8.31: *Module 26 pulsed I-V and led2 leakage current.*

many cases in fact, the module survived the failure or degradation of one of even two of the LEDs. An example of this behaviour is shown in Fig. (8.31) and (8.32).

The pulsed I-V is particularly interesting. In fact it is clearly possible to see the way the failure of *led2* altered the curve. Anyway, it is also clear that this event did not compromise the robustness of the module. The proof of this is given by the fact that the pulsed I-V remains the typical one for a LED device in the breakdown region even after *led2* failure. It is interesting to notice that the module could withstand many more ESDs before failing. The leakage currents of the single LEDs, Fig. (8.32), confirm what previously said.

This behaviour was observed in many cases and other examples can be seen in Fig. (8.33) and (8.34).

Another module in which it was possible to notice this characteristic, even if in a less blatant way, was the so-called *module 17*, Fig.(8.35).

It is possible to notice how the failure of led2 determines a discontinuity in the pulsed I-V, without changing its shape, as already shown for *module 26*.

In general, during the blue LED modules analysis, the pulse waveforms did not show any significant characteristic, not providing any useful information. Because of this they were not reported here.

The data on the robustness are summarized in Table (8.5). In this case the parameters considered to characterize the ESD properties of the modules are V_{fail},I_{fail}, $V_{pre-fail}$, $I_{pre-fail}$,V_{FAIL}, $V_{pre-FAIL}$,I_{FAIL}, $I_{pre-FAIL}$. V_{fail} and I_{fail} are the voltage and current of the ESD that causes the first failure of a LED of the module, while $V_{pre-fail}$and $I_{pre-fail}$ are the voltage and current of the pulse before. $I_{FAIL}/I_{pre-FAIL}$ ($V_{FAIL}/V_{pre-FAIL}$) are instead the currents (voltages) of the ESD that causes the module failure and the one before respectively. Since gradual failure was not so common (as it will be shown later) and there would not have been similar data in the single LEDs case to compare them with, voltage and current of the pulse that caused the first LED degradation were not considered.

Before analyzing these results, it is very important to say that the V_{FAIL} and $V_{PRE-FAIL}$ measures in some cases were strongly influenced by the limitations of the measurement system. In particular the maximum voltage that could be measured was limited to about 810 V.

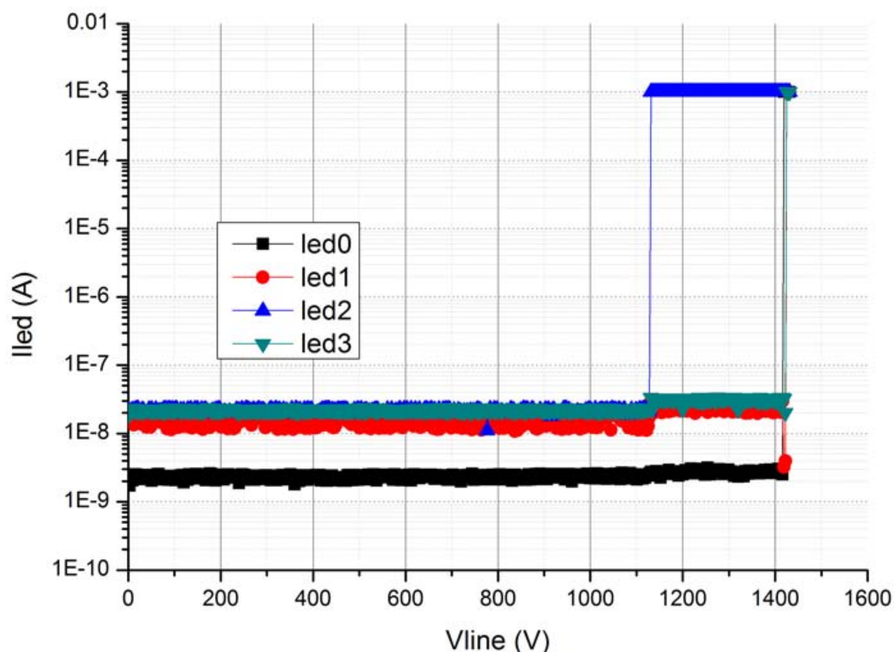


Figure 8.32: *Module26: leakage currents of the single devices.*

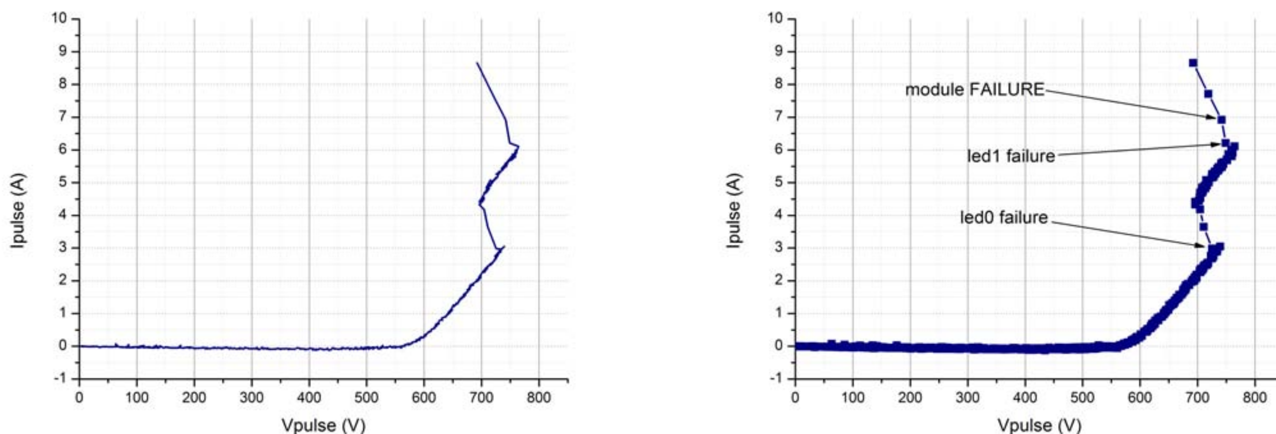


Figure 8.33: *Module 30 pulsed I-V. On the right the points corresponding to the failures are shown.*

	$V_{pre-fail}$ [V]	V_{fail} [V]	$I_{pre-fail}$ [V]	I_{fail} [V]	$V_{pre-FAIL}$ [V]	V_{FAIL} [V]	$I_{pre-FAIL}$ [A]	I_{FAIL} [A]
Max.	810.904	810.904	7.618	7.915	809.572	808.554	12.572	12.653
Min.	393.845	565.488	1.340	1.340	626.214	613.061	4.031	4.890
Mean	731.072	745.757	4.532	4.614	748.650	738.477	7.509	8.198
std. dev.	93.5474	68.0833	1.7088	1.7306	56.5705	59.3850	2.0955	1.9285

Table 8.5: *Robustness of blue LED modules towards ESD events summary.*

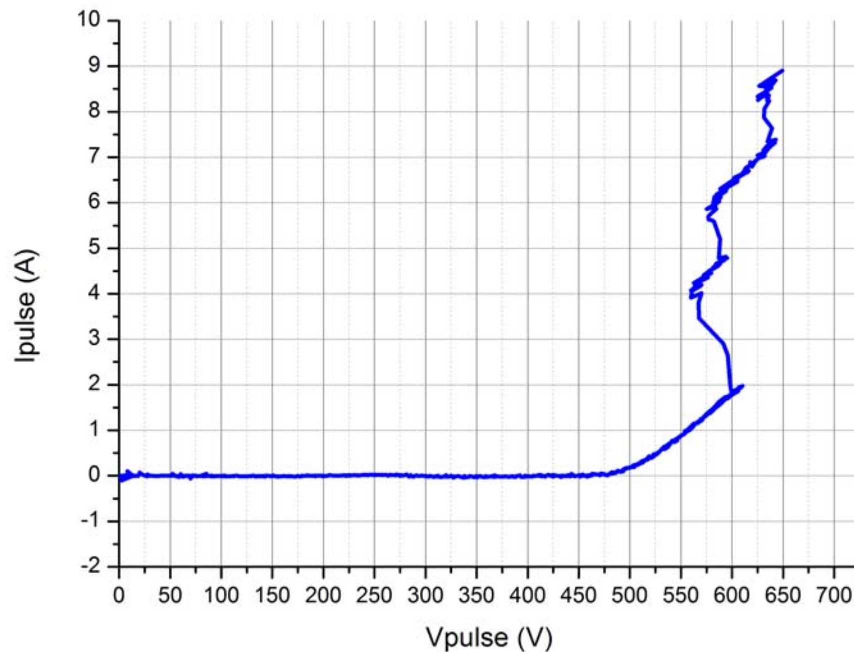


Figure 8.34: *Module 5 pulsed I-V.*

Comparing these results with those obtained in the single LEDs case, Table (6.1), it is possible to see that being in a module seems not to make the single LEDs more resistant to ESDs. In fact, while the mean value of the maximum pulse current that the single LEDs could withstand was 5.96 A, in the modules the first device failed at 4.61 A (mean value). Considering the robustness of the whole module things improve. In fact $I_{pre-FAIL}$ is about 7.5 A. This is a good result if compared for example to the case of the red LED modules (they showed poorer current-withstanding properties than the single devices).

Considering the mean voltage withstanding level, it is possible to see that for the modules this parameter value is more than three times higher than in the single LEDs case. Anyway, since this result is limited by the characteristics of the measurement system (as previously said), the real voltage withstand properties are therefore expected to be better.

Another characteristic highlighted by the results of this investigation, was the predominance of catastrophic failures, Fig. (8.36). An example of the I-V of a LED that failed in a catastrophic way is shown in Fig. (8.37).

Anyway, despite the majority of the LEDs failing catastrophically, there still were some devices that showed a very gradual degradation, like the one shown in Fig. (8.38) and (8.39).

An investigation was carried out also to try to determine whether the LED position inside the module has an influence on that specific device robustness or not. For every stress-test (remember that the stresses were stopped just when the whole module failed), the position of the first LED that failed was observed, Fig. (8.40). These results seem to suggest that the position in the serie might have little influence on the robustness of a LED. Only *led3* could be more protected, anyway more experimental measures are needed to determine it.

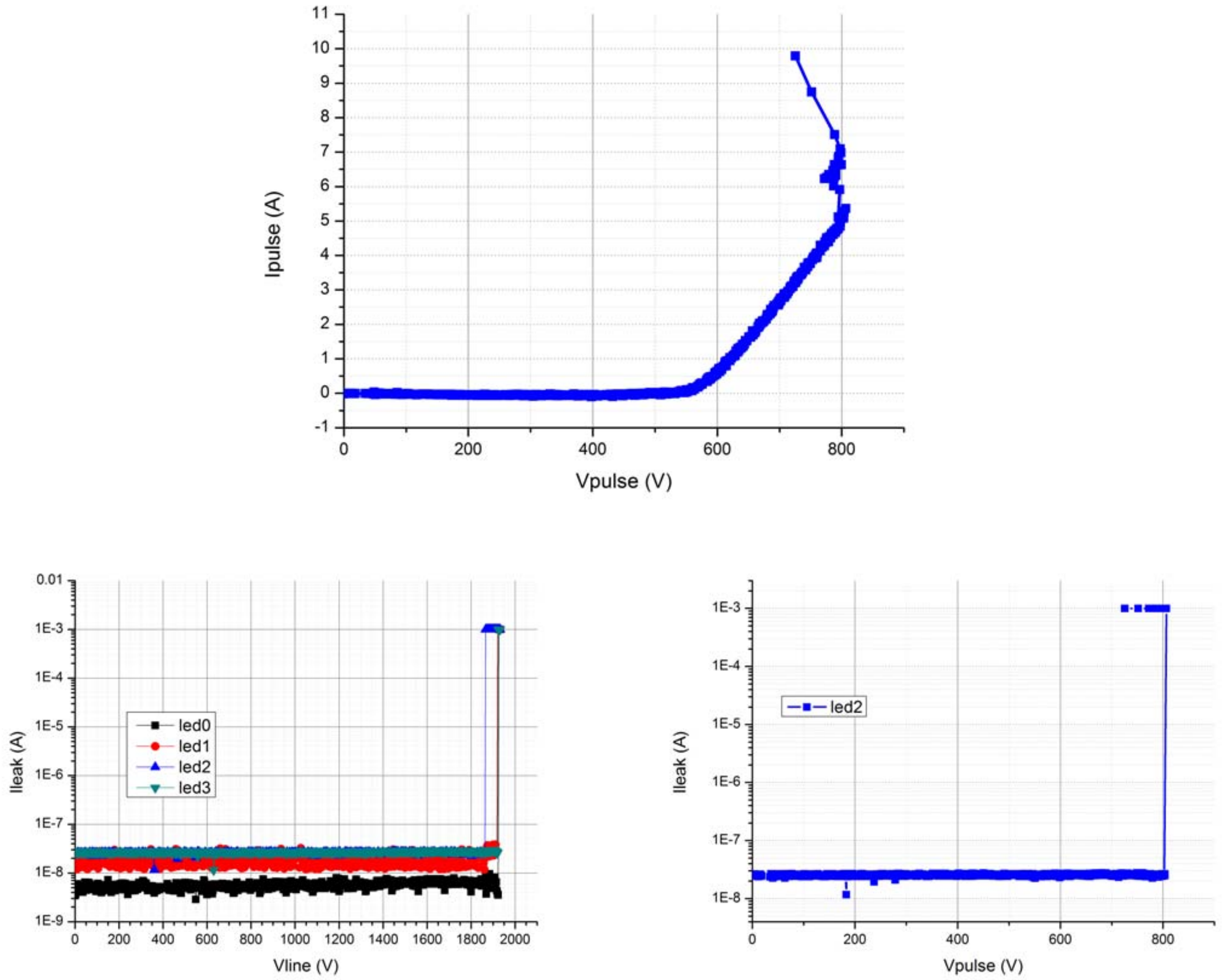


Figure 8.35: *Module 17 stress-test results.*

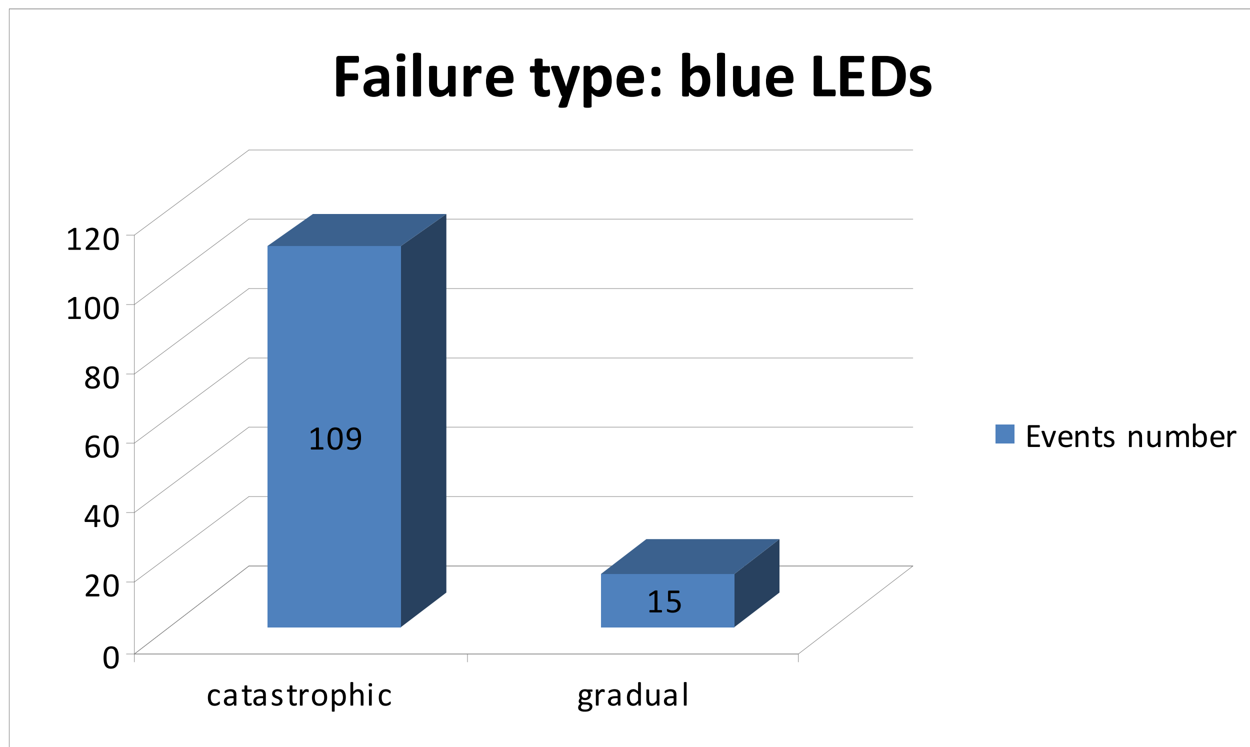


Figure 8.36: *Summary of the types of failure that characterize the blue LEDs when in module.*

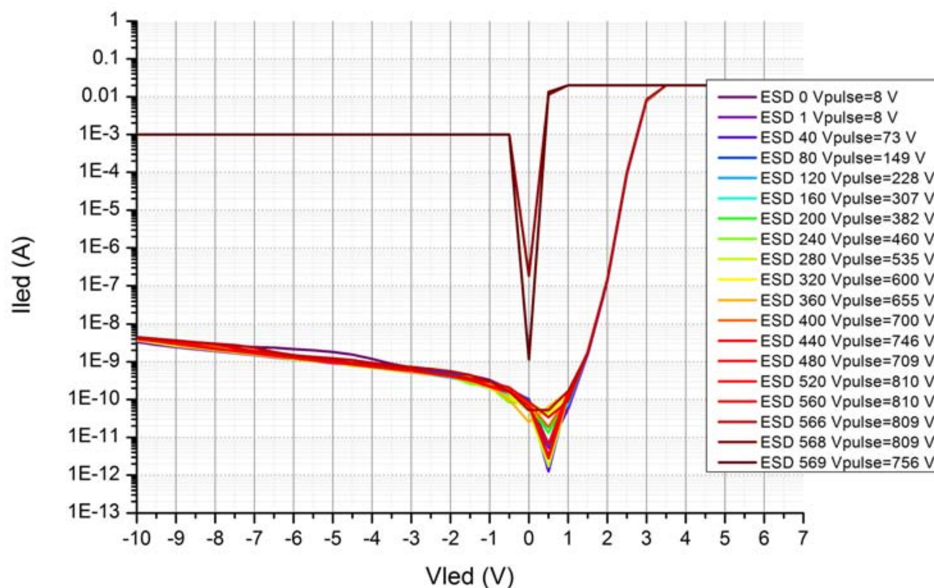


Figure 8.37: *Example of a catastrophic failure. Measured IV curves of Led0, module 20.*

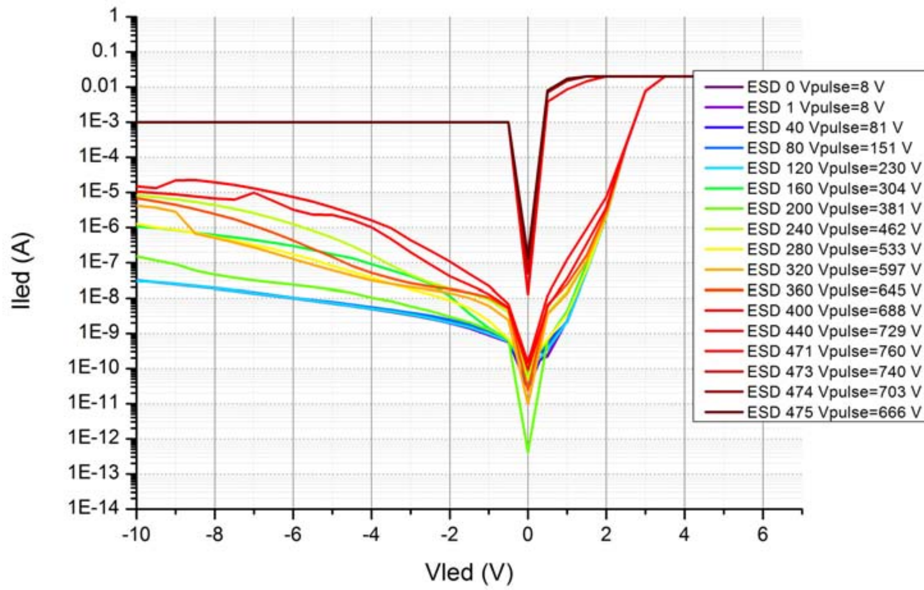


Figure 8.38: *The measured I-V curves of led3 (belonging to module 19).*

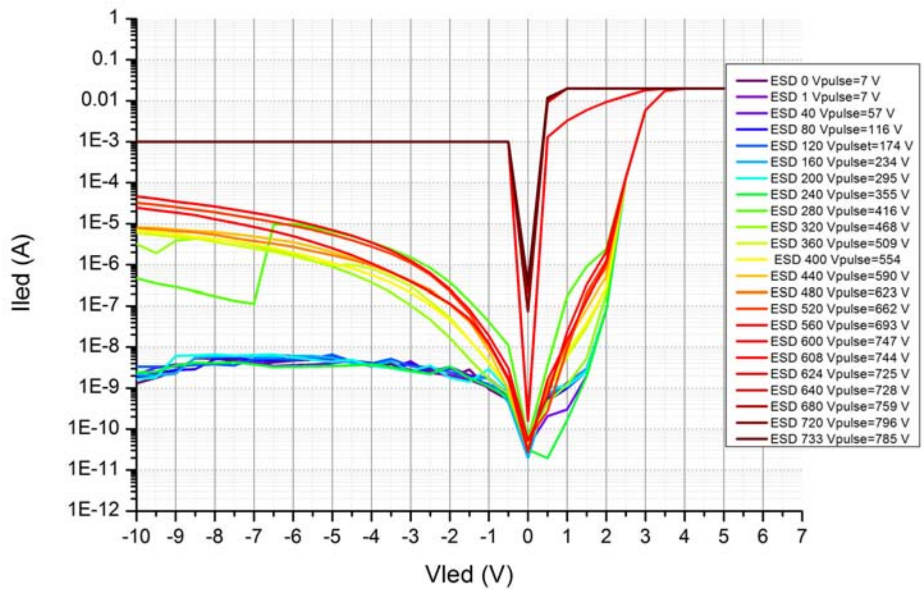


Figure 8.39: *Module6 led1 I-V curves measured during the stress-test.*

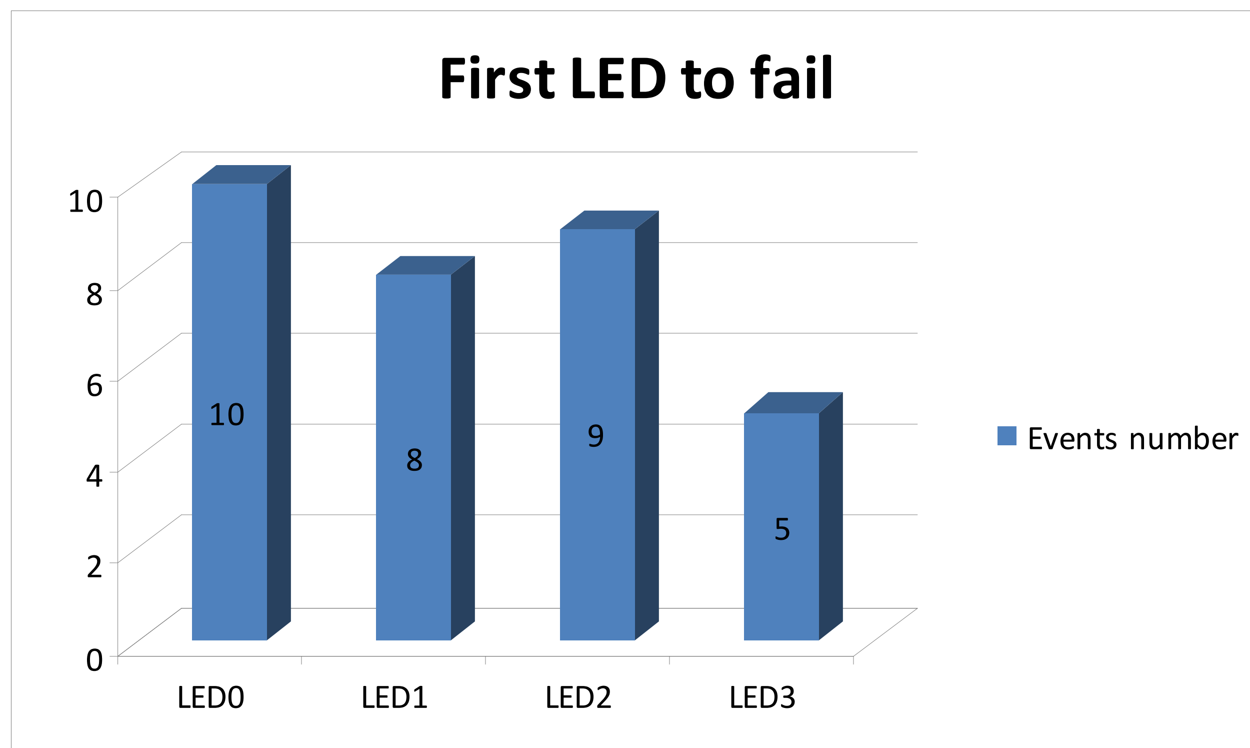


Figure 8.40: *Summary of the investigation on the dependence between*

8.4 FINAL CONSIDERATIONS

The results of this investigation showed that the different types of modules have different behaviours. In particular, while the blue and green ones seem to be capable of surviving the failure of one of their LEDs, red modules do not.

Comparing the average current and voltage-withstand levels in Table (8.5), (8.3) and (8.1), red LEDs modules seem to be the most robust, with $I_{pre-fail}$ equal to 17.95 A. However, the average current that they could withstand before degradation was about 7.2 A and once this process had started the module was already deeply damaged. The average maximum voltage that they could stand was instead about 418 V. On the other hand, despite being capable of surviving the failure or degradation of one of their LEDs, green and blue modules could withstand lower currents without failing, about 8.36 and 7.51 A respectively. The maximum voltage values were about 543.1 volts for the green and 748.6 V for the blue modules.

It is also interesting to notice that the first degradation of one of the devices of the green modules, took place at very low current values (the average maximum current before degradation was 0.977 A). The average current that the blue ones could endure before the first failure of a LED took place was instead 4.5 A.

Useful informations were given also about the type of failure of the single devices. The green LEDs failed in most part gradually, the blue ones catastrophically, while the red ones showed both.

Finally, the extended analysis on the blue LED modules seems to suggest for the single devices the absence of a correlation between position in the module and ESD robustness. Anyway further measures are needed to prove this.

Bibliography

[1] R.D. Enoch and R.N. Shaw, “An Experimental Validation of the Field Induced ESD Model”, in Proc. 8th EOS/ESD Symposium, ESD Association, Rome, NY, USA, pp. 224–231, 1986.

[2] D.L. Lin and M.-C. Jon, “Off-Chip Protection: Shunting of ESD Current by Metal Fingers on Integrated Circuits and Printed Circuit Boards”, in Proc. 16th EOS/ESD Symposium, ESD Association, Rome, NY, USA, pp. 279–285, 1994.

[3] R.N. Shaw, “A Programmable Equipment for ESD Testing to the Charged Device Model”, in Proc. 8th EOS/ESD Symposium,ESD Association, Rome, NY, USA, pp. 232–237, 1986.

[4] R.G. Renninger, M.-C. Jon, D.L. Lin, T. Diep and T.L. Welsher, “A field-induced charged device model simulator”, in Proc. 11th EOS/ESD Symposium, ESD Association, Rome, NY, USA, pp. 59–71, 1989.

[5] M.Meneghini, A.Tazzoli, N.Trivellin, G.Meneghesso, E.Zanoni, M.Pavesi, M.Manfredi, R.Butendeich, U.Zehnder and B.Hahn, “A study on the failure of GaN-based LEDs submitted to reverse-bias stress and ESD events”, in Reliability Physics Symposium (IRPS), pp. 522 - 527, 2010.

[6] G.Meneghesso, A.Chini, A.Maschietto, E.Zanoni, P.Malberti, M.Ciappa, “Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes”, in Electrical Overstress/Electrostatic Discharge Symposium, pp 247-252, 2001.

[7] Y.K. Su, S.J. Chang, S.C. Wei, Shi-Ming Chen, Wen-Liang Li, “ESD Engineering of Nitride-Based LEDs”, IEEE Transactions on Device and Materials Reliability, Vol. 5, No.2, pp 277-281, June 2005.

[8] C. M. Tsai, J. K. Sheu, P. T. Wang, W. C. Lai, S. C. Shei, S. J. Chang, C. H. Kuo, C. W. Kuo, and Y. K. Su, “High Efficiency and Improved ESD Characteristics of GaN-Based LEDs With Naturally Textured Surface Grown by MOCVD”, in IEEE Photonics Technology Letters, Vol.18, No.11, June 1, 2006.

[9] T. H. Chiang, Y. Z. Chiou, S. J. Chang, C.K.Wang,T.K.Ko,T.K.Lin,C.J.Chiu,andS.P.Chang, “Improved Optical and ESD Characteristics for GaN-Based LEDs With an n—-GaN Layer”, in IEEE Transactions on a Device and Materials reliability, Vol.11, No.1 march 2011.

[10] Soo-Kun Jeon, Jae-Gab Lee, Eun-Hyun Park, Jin Jang, Jae-Gu Lim et al., “The effect of the internal capacitance of InGaN-light emitting diode on the electrostatic discharge properties” , in Applied Physics Letters 94, 2009.

[11] Tsung-Hsun Chiang, Chun-Kai Wang, Shoou-Jinn Chang, Yu-Zung Chiou, Tsun-Kai Ko, Tien-Kun Lin, and Sheng-Po Chang, “Effect of Varied Undoped GaN Thickness on ESD and Optical Properties of GaN-Based LEDs”, in IEEE Photonics Technology Letters, Vol.24, No.10, may 15, 2012.

[12] A. Amerasekera, C. Duvvury, “ESD in Silicon Integrated Circuits”, 2nd Edition, Chichester, England: John Wiley and Sons, 2002.

[13] E. Fred Schubert, “Light-Emitting Diodes”, 2nd Edition, Cambridge University Press , 2006.

[14] E. Fred Schubert, “Physical Foundations of Solid-State Devices”, Troy NY, Usa, September 2009.

[15] Richard S. Muller, Theodore I.Kamins, Mansun Chan, “Device Electronics for Integrated Circuits”, 3rd Edition, Milton Keys, UK, John Wiley and Sons, February 2011.

[16] Matteo Bertocco, Alessandro Sona, “Manuale di Compatibilità Elettromagnetica”, 2nd Edition, Lulu, February 17th 2010.