Università degli studi di Padova
Engineering Department
Electronic Engineering

Digital current control of a dc-dc Boost converter

Master Thesis

Author:
Mahnaz Behnamazad

Thesis Supervisor:
Prof. Luca Corradini

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Abstract

Switched mode power supplies offer many advantages, one of those is the high efficiency factor. They can be implemented with analog components or digitally such as microcontroller, digital signal processor (DSP) or FPGA. Digital controllers have advantages over its analog, such as changing the calculated coefficient whenever needed without any change in hardware, reduction number of components and protection against noise. The digital control of power electronic converters consist operation, modeling and control of converters.

This thesis is focused on the analysis, modeling, design and implement of digital current control of the Boost converter by FPGA. The current control of a Boost converter has various applications. One of those applications is the photovoltaic system using solar panels. In this system, solar panels absorb the sunlight and creates an electricity direct current (DC). Then it converts to an alternating current (AC) using an inverter. So the purpose of the Boost converter as a part of the PV system is to increase and regulate the amount taken from the solar panels to feed the inverter. The another example appears in the power factor correction (PFC) converters used as first stage in switched mode power supplies. So using a Boost PFC needs to control the input current, because of being the sinusoidal transitory current after power returns. Therefore it realizes by averaged current mode control.

Chapter 1

Introduction

Control and regulate of electric current is required in many applications which is provided by a Boost converter. In this chapter consider two applications such as photovoltaic system and PFC.

1.1 Photovoltaic system

A photovoltaic system is a power system consist of solar panels which convert the energy in photons of light into an electrical voltage and current by semiconductor materials related to the solid state technologies. PV systems have different sizes [1]. According to needed application, they can be small such as rooftop-mounted or can be large such as utility-grid. The grid-connected PV systems can be produced AC power by synchronizing to an electric utility grid [2]. In this power system, the function based on convert the DC power generated by PV panels into AC power. The grid-connected PV system on constructions bring electric generation to the load for usage. The load is a domestic appliance, for example might be a battery or a dc motor. In fig. 1.1 shows a schematic of connecting the solar panels into the utility grid. If after the module sitting in the sun, not connected a load, no power is delivered to load by the module. Because of being the zero output voltage in case of the module short-circuit, and no flow the current in case

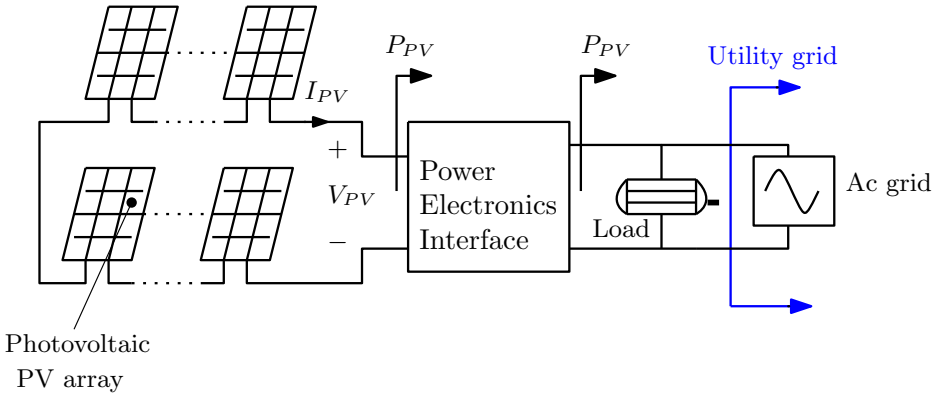


Figure 1.1: *Grid-connected PV system*

of open-circuit. Therefore by connecting a load, the power will be delivered because of existing the current and voltage. The same voltage and current runs across the PV and load. So exist an operating point at the intersection between the PV and load in the I-V curves. If the load is a resistance, define

$$I = (\frac{1}{R})V. \tag{1.1}$$

So by plotting the load on the current and voltage axes, it has a straight line with slope $1/R$. With increasing the resistance, the operating point can be moved. When the current and voltage reach their maximum value with best value of the resistance, the maximum power is produced. This point is called MPP which also depends on the temperature and radiation factors and can be increased with increasing the solar radiation [3, 4]. The Fig. 1.2 shows the I-V curves with MPP point. In the residential usage such as residential rooftop, the system usually are in the 1 to 10 kW range. The PV output occurs during the sunlight hours and at the same time (during the day) sell power to the utility. So there is a growing trend to store energy.
Devices to have an PV system grid-connected with maximum power point called maximum power trackers (MPPT) which the target is keeping the PV operation at its highest efficiency point at all times with going up and down of the sun. There is some circuits to achieve the MPPT. As the key is convert dc voltage from one level to a higher level, a switched mode Boost converter

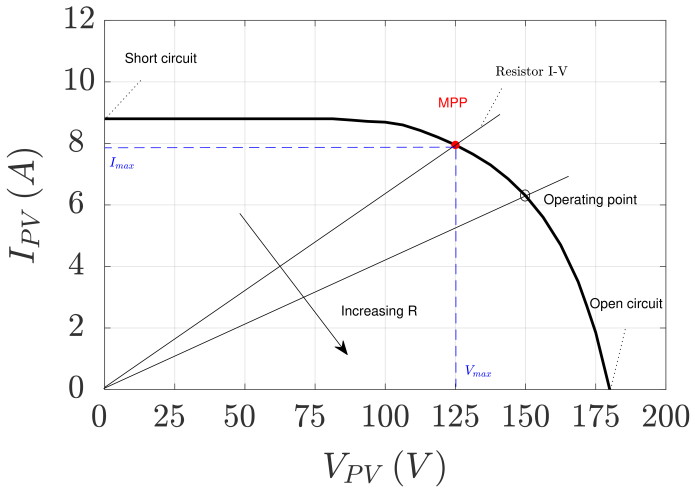


Figure 1.2: *The current-voltage curves for PV and load*

is suitable for use as power electronics interface. In point of controlling the input current, the PV system can be remained at the maximum power point. After bringing the required voltage from source to load by Boost converter, it needs to an inverter (DC/AC), for sending AC power usually at 240 V. Then the AC output of a grid-connected PV system sent into the main electrical distribution panel. The block diagram of the PV system with current controlled Boost to track maximum power point is illustrated in Fig. 1.3. There are two conditions of power,

- $P_{PV} < P_{load}$:
  In this case, the PV power completely used to supply the load and the rest of the power needed is provided by the utility grid.

- $P_{PV} > P_{load}$:
  The PV power is more than to supply the load and PV power injected into the AC grid. So grid absorbs power for building up a credit with the utility.

If the load is a complicated thing such as a DC motor, the I-V relationship consist of also the motor speed. at start-up when the speed of motor is zero,

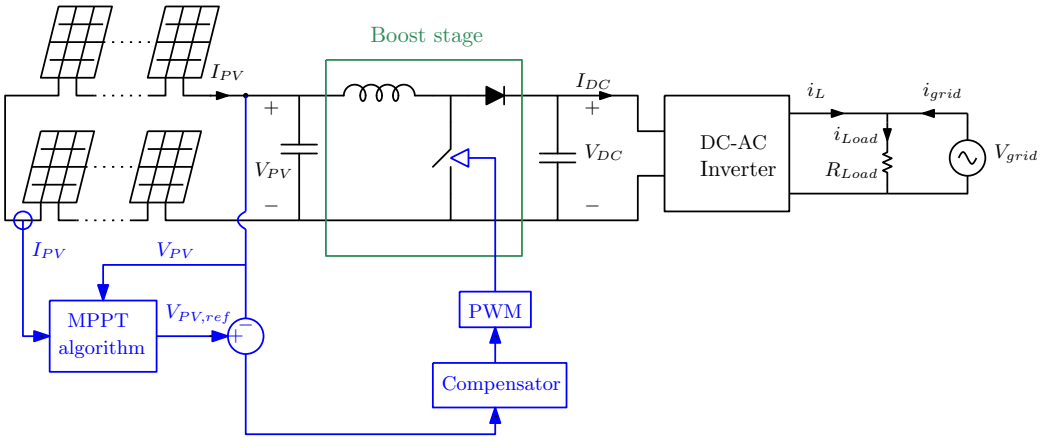


Figure 1.3: *Pv system with current controlled Boost converter*

the current increases with increasing the voltage until is sufficient for create torque. So with starting to speed the motor, current increases more slowly with increasing voltage. On the other hand by stalling a dc motor while the voltage is much higher than its initial voltage, the current rises continuously and leads to the burning the armature coil. Therefore the dc motor I-V curve is not a direct line like the resistance load, so discontinuity of operating point occurs with the ideal MPP.

1.2 Power factor correction (PFC)

All electronic devices need a power supply to convert the AC voltage from the grid to the DC voltage. Use a large number of power supplies, will be affect its quality. So can be improved this effect by using the single phase power factor correction circuit as input stage of electronic appliances which increase the power factor and reduce harmonic current. The power factor defines the relationship between the active power supplied to the load and the output power that should be close to one. On the other hand the total harmonic distortion (THD) related to current harmonic content of the input AC current which should be low as possible. The PFC controller uses Boost topology as AC/DC rectifiers in power systems.[5, 6]

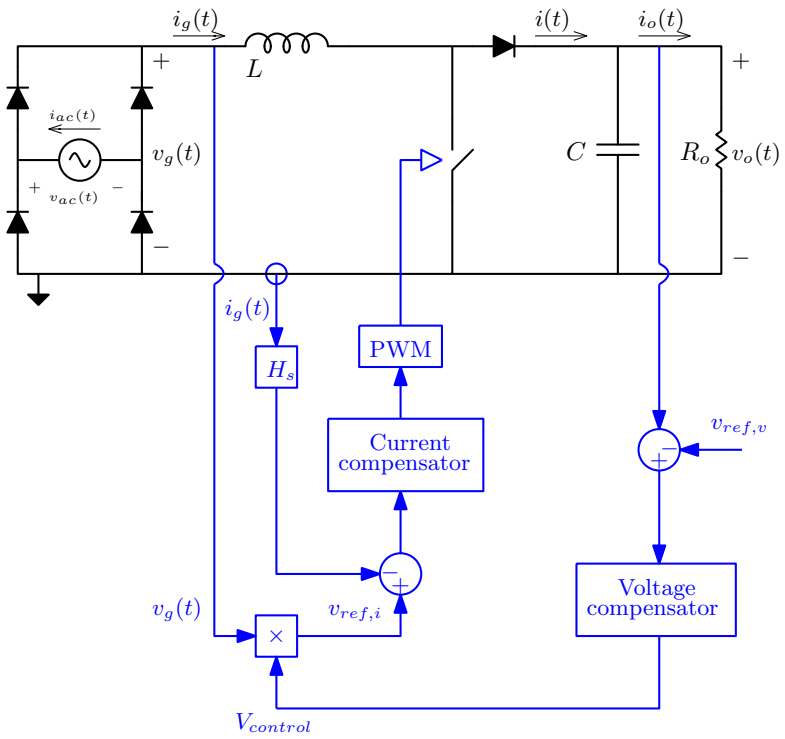


Figure 1.4: *Block diagram of controlled Boost power factor correction*

The block diagram of a controlled Boost PFC is shown in Fig. 1.4. By this control will be maintain the AC current in same phase with the AC voltage and being a sinusoidal wave with minimum distortion for the current. Therefore a Boost PFC circuit with inductor current control can be ensure that it tracks the rectified AC voltage. The steady state waveform with the Boost PFC controller is illustrated in Fig. 1.5. As seen, the AC current and voltage are in same phase. The first is rectified by diode bridge, then by using Boost controller can be regulated the dc output voltage and supplied a dc power to the load. This controller consist of two parts, current control loop and voltage control loop. The voltage loop is used to regulate the converter output voltage and operate a power balance loop. So with the output voltage lower than $v_{ref,v}$, the feedback voltage V_{cntrl} should increase in order to attract more ac power. The current loop utilized to control the rectified current $i_g(t)$ with the rectified voltage $v_g(t)$. Therefore the input

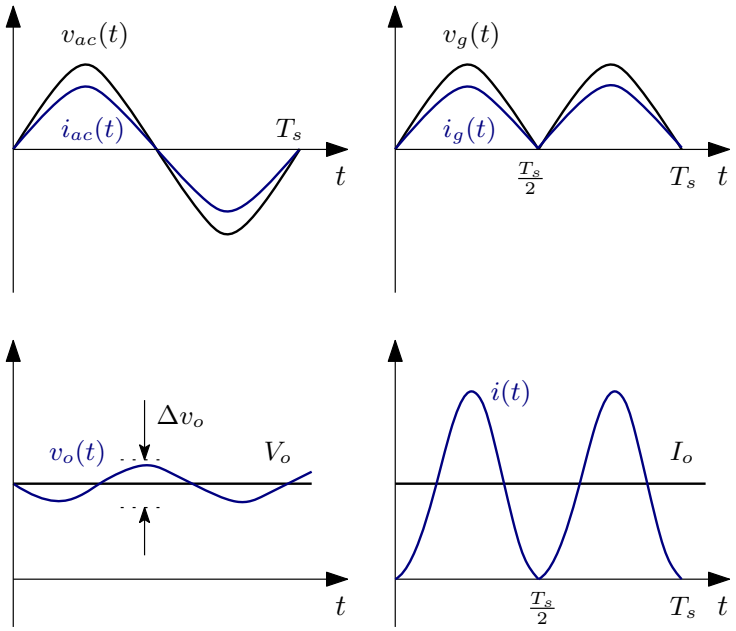


Figure 1.5: *PFC waveform in steady state*

side of the rectifier behaves as a emulated resistance. By multiplying $v_g(t)$ into a controllable signal V_{cntrl} will be achieved the set point value $v_{ref,i}$. The emulated resistance can be defined as

$$R_{em} = \frac{v_g(t)}{i_g(t)} = \frac{H_s}{V_{cntrl}}. \tag{1.2}$$

Then can be defined the active power of the dc load as follow.

$$P = \frac{V_{as,rms}^2}{R_{em}} = \frac{V_{as,rms}^2 \cdot V_{cntrl}}{H_s}, \tag{1.3}$$

where

$$V_{ac,rms} = \frac{v_{ac}(t)}{\sqrt{2}sin(\omega t)}. \tag{1.4}$$

Thesis structure

In the following, will be expanded the averaged current control of a Boost converter. In chapter 2, a synchronous Boost converter will be analyzed and modeled. The current mode control of a Boost converter consist of various digital controllers, that in chapter 3 will be designed the convenient controller. Also proposed the switch current sensing which achieve to the inductor average current. The chapter 4 will be allocated to simulation of the system designed and in chapter 5, experimental results will be provided to verify the analysis.

Chapter 2

Steady-state and dynamical analysis of the Boost converter

2.1 Boost converter

A Boost converter is a switched-mode DC to DC converter, that is also called step up converter, because the output voltage is greater than the input voltage. The input power has to be equal to output power, this equality comes from the law of energy conservation.

2.1.1 Circuit Analysis

As shown in the Fig. 2.1, a Boost converter including a DC voltage source, an inductor L, a switch, a capacitor C and a load resistor R. In practice a Mosfet and Diode are used instead of switches. With the switch in position 1, the right-hand side of the inductor is connected to ground, as illustrated in Fig. 2.2.
The inductor voltage and capacitor current for this subinterval are given by

$$V_L = V_g, \tag{2.1}$$

$$i_C = -\frac{V_o}{R_o}. \tag{2.2}$$

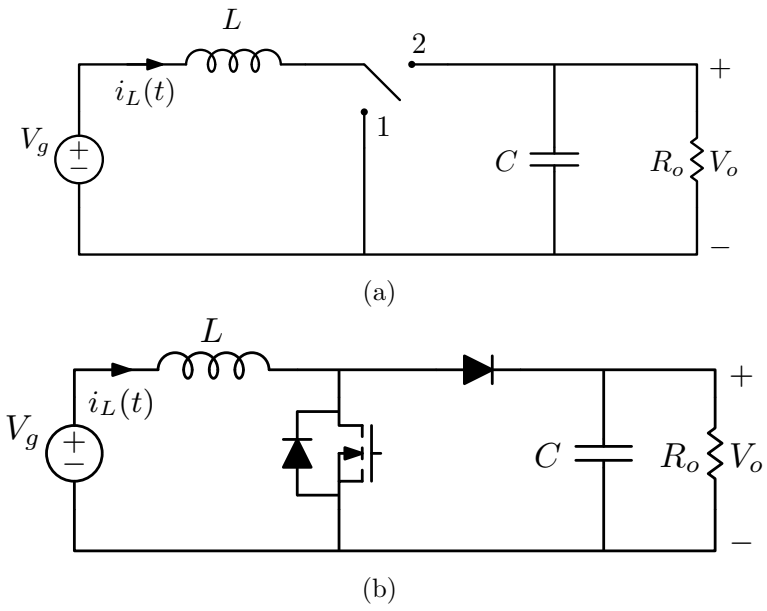


Figure 2.1: *Boost converter: (a) ideal switch, (b) practical realization*

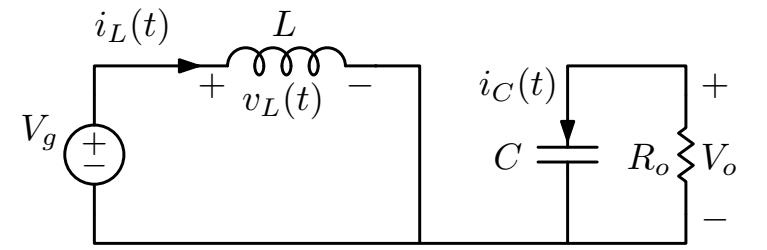


Figure 2.2: *Boost converter with switch in position 1*

With the switch in position 2, the inductor is connected to the output, as shown in Fig. 2.3. The inductor voltage and capacitor current are then

$$V_L = V_g - V_o, \tag{2.3}$$

$$i_C = i_L - \frac{V_o}{R_o}. \tag{2.4}$$

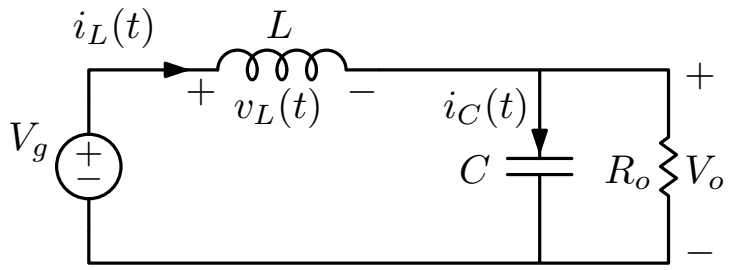


Figure 2.3: *Boost converter with switch in position 2*

2.1.2 Converter in steady-state

In steady state, each of converter voltage and current is periodic in time, with a period equal to the converter switching period T_s. When the converter input and duty cycle are constant, and after all transient are turened off, it is achieved to steady-state position.

2.1.2.1 Inductor volt-second balance, Capacitor charge balance and the small ripple approximation

Steady-state analysis includes the dc values of all the voltages and currents of converter inputs. The analysis consist of the following by two basic principle:

- Inductor Volt-second balance:
  Inductor voltage is defined by

$$v_L(t) = L\frac{di_L(t)}{dt}, \tag{2.5}$$

  and with integrating on a switching period

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)dt. \tag{2.6}$$

  In steady-state, the net flux (volt-seconds) in an inductor must be zero. So the average inductor voltage on a switching period is zero

$$\langle v_L \rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = 0. \tag{2.7}$$

- Capacitor ampere (charge)-second balance:
  Capacitor current is defined by

$$i_C(t) = C\frac{dv_C(t)}{dt}, \tag{2.8}$$

  and with integrating on a switching period

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{T_s} i_C(t)dt. \tag{2.9}$$

  In steady-state, the net charge in a capacitor must be zero. So the average capacitor current on a switching period is zero

$$\langle i_C \rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} i_C(t)dt = 0. \tag{2.10}$$

The actual output voltage $v_o(t)$ is illustrated in Fig. 2.4 and expressed as

$$v_o(t) = V_o + \Delta v_o(t). \tag{2.11}$$

So it consist of the dc value V_o, plus a small ac value Δv_o created on effect of the switching harmonic attenuation.
The target is to produce a dc output, then the output voltage switching ripple should have an small value. So the magnitude of the switching ripple is smaller than the dc value:

$$\mid \Delta v_o \mid \ll V_o, \tag{2.12}$$

Hence, the small ripple Δv_o neglected and the output voltage $v_o(t)$ is approximated by its dc component V_o:

$$v_o(t) = V_o. \tag{2.13}$$

This approximation, called the small-ripple approximation, or the linear-ripple approximation.

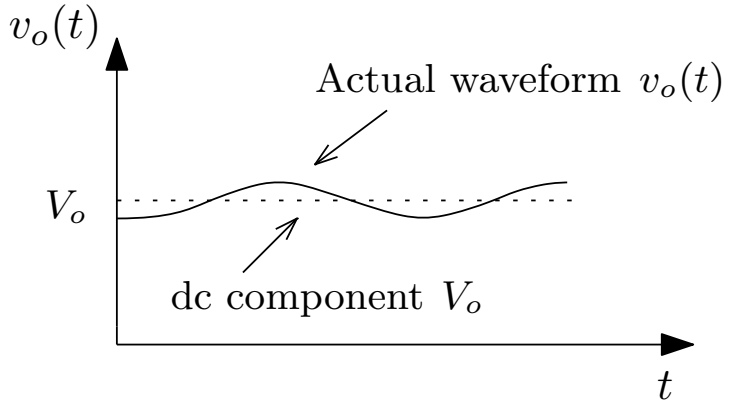


Figure 2.4: *Actual output voltage waveform*

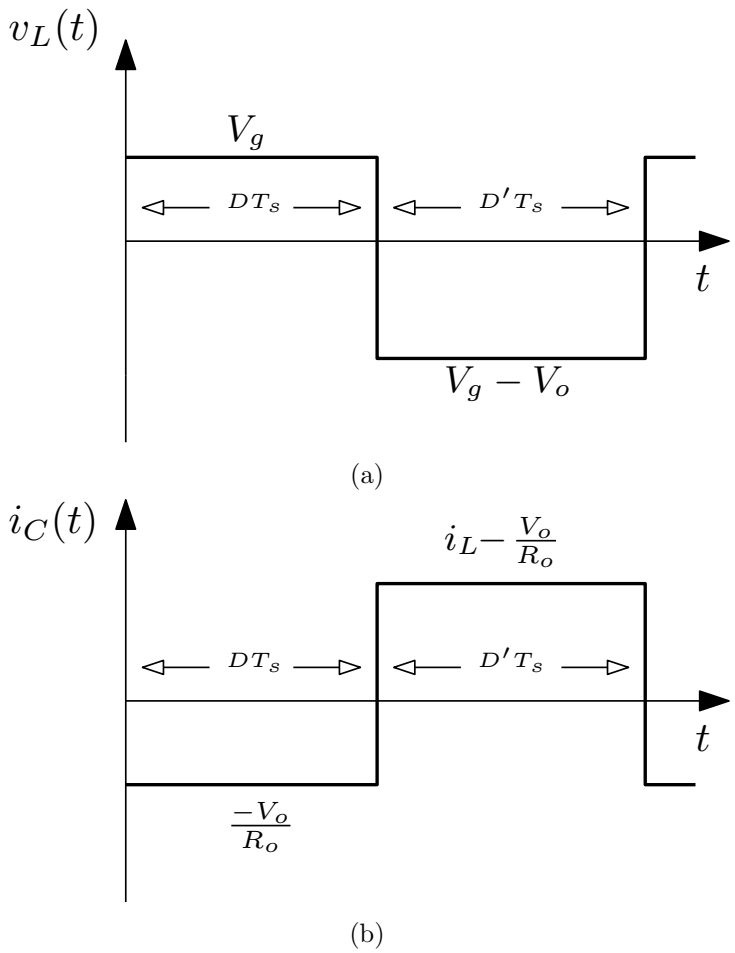


Figure 2.5: *(a) inductor voltage waveform, (b) capacitor current waveform*

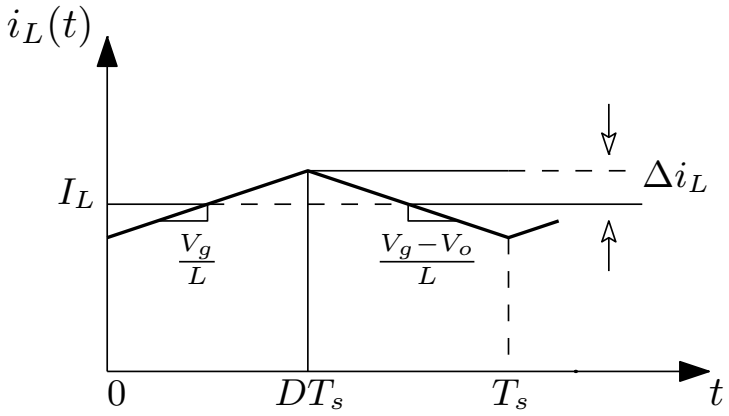


Figure 2.6: *Inductor current waveform*

2.1.2.2 DC conversion ratio and Inductor current

As mentioned in section. 2.1.1, with the inductor voltage and capacitor current equations we reach to theirs waveform in the fig. 2.5. As shown, during the first subinterval $v_L(t)$ is equal to the dc input voltage V_g, and during the second subinterval the inductor voltage is equal to $(V_g - V_o)$. So with keeping the volt-second balance principle, the inductor over one switching period is equal to

$$\int_0^{T_s} v_L(t)\,dt = (V_g)DT_s + (V_g - V_o)D'T_s = 0. \tag{2.14}$$

By noting that $(D + D') = 1$, the output voltage is equal to

$$V_o = \frac{V_g}{D'}. \tag{2.15}$$

So the voltage conversion ratio $M(D)$ is a proportion of the output voltage and input voltage of the converter, that is given by

$$M(D) = \frac{V_o}{V_g} = \frac{1}{D'} = \frac{1}{1-D}, \tag{2.16}$$

And is illustrated in Fig. 2.7.

To express the inductor current, the capacitor charge balance principle is used. As mentioned in previously, during the first subinterval, the capacitor current is equal to load current and the capacitor discharged. In the

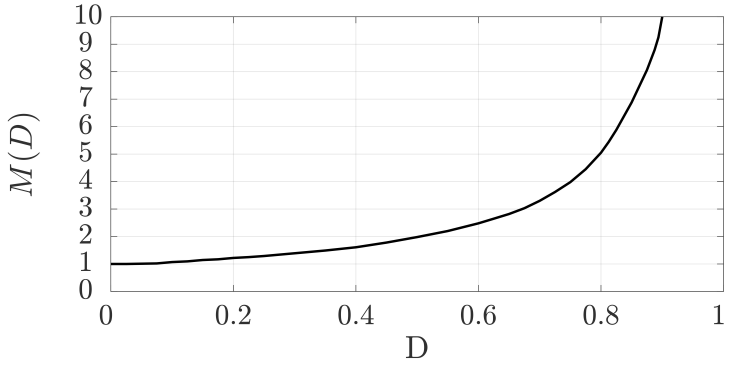


Figure 2.7: *Voltage conversion ratio $M(D)$*

second subinterval, the inductor current recharges the capacitor. By using the ampere-second balance principle, the capacitor over one switching period obtains:

$$\int_0^{T_s} i_C(t)\,dt = (-\frac{V_o}{R_o})DT_s + (I_L - \frac{V_o}{R_o})D'T_s = 0. \tag{2.17}$$

By noting that $(D + D') = 1$, the inductor current as dc component is equal to

$$I_L = \frac{V_o}{D'R_o}, \tag{2.18}$$

2.1.3 CCM and DCM operation

Two fundamental modes for the dc-dc converters are possible: Continuous-Conduction Mode (CCM) and Discontinuous-Conduction Mode (DCM).
In the Continuous Conduction mode, the inductor current flows continuously as is always above zero throughout the switching period. When the boost converter operates in CCM mode, the output voltage can be controlled by controlling the duty cycle D. As seen in Fig. 2.6, the inductor voltage waveform $v_L(t)$ is almost a constant signal. So the inductor current ripple is a triangular waveform with slopes $\frac{v_L(t)}{L}$.
Then the peak-to-peak current ripple Δi_L can be defined by

$$\Delta i_L = \frac{1}{L}\int_0^{DT_s} v_L(t)\,dt = \frac{V_g}{L}DT_s = \frac{T_s}{L}V_g(1 - \frac{V_g}{V_o}). \tag{2.19}$$

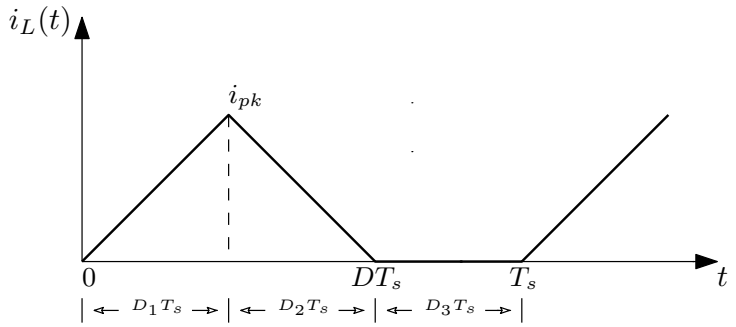


Figure 2.8: *Inductor current in DCM*

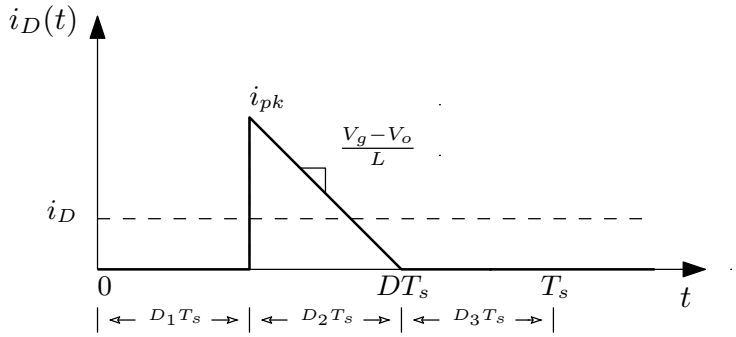


Figure 2.9: *Diode current in DCM*

Similarly, from the capacitor voltage ripple waveform, the peak-to-peak output voltage ripple can be defined by

$$\Delta v_C = \frac{1}{C}\int_0^{DT_s} i_C(t)\,dt = \frac{V_o}{R_oC}DT_s = \frac{T_s}{R_oC}(V_o - V_g). \tag{2.20}$$

In the Discontinuous Conduction Mode, the inductor current reaches to zero before the end of each switching period T_s, as shown in Fig. 2.8. There are now three subintervals during each T_s. The transistor conducts in the first subinterval, the diode conducts during the second subinterval and it is equal to the inductor current. At the end of the second subinterval, the diode current and as a result, the inductor current, reaches to zero.
For the third subinterval, neither the transistor nor the diode conduct. So the converter operates as discontinuous conduction mode. In this mode, the

input and output voltage conversion ratio is defined by

$$M = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}, \tag{2.21}$$

where

$$K = \frac{2L}{R_o T_s}. \tag{2.22}$$

2.2 CCM Boost converter dynamics and control

It is necessary to mention that in this project, all of the operations work only at the CCM. The Boost converter is controlled to regulate the inductor current $i_L(t)$. So feedback is required. In this section, target is the Boost converter averaged small-signal modeling with the consideration of current-mode control. A block diagram of the system is illustrated in Fig. 2.10. For inductor current regulation of the Boost converter, as seen in Fig. 2.10, $i_L(t)$ is modeled by sensing gain H_s and compared with the setpoint value of V_{ref}. Then with a regulation transfer function $G_c(s)$ estimates and converts the comparison output into a control signal $u(t)$.Then, $u(t)$ compares with an oscillator and converts into the gate control $c(t)$. To design this system, it is required a dynamic model of the switching converter and to achieve of this model, consider the converter averaged and small-signal modeling.

2.2.1 Averaging and linearization

The averaging operation has the objective to remove the time variance of the converter and the linearization removes the nonlinearities and dfines the small-signal models[7]. In boost converter, as it shown in section. 2.1.1, in the first subinterval

$$V_L = v_g(t), \tag{2.23}$$

$$i_C = -\frac{v_o(t)}{R_o}. \tag{2.24}$$

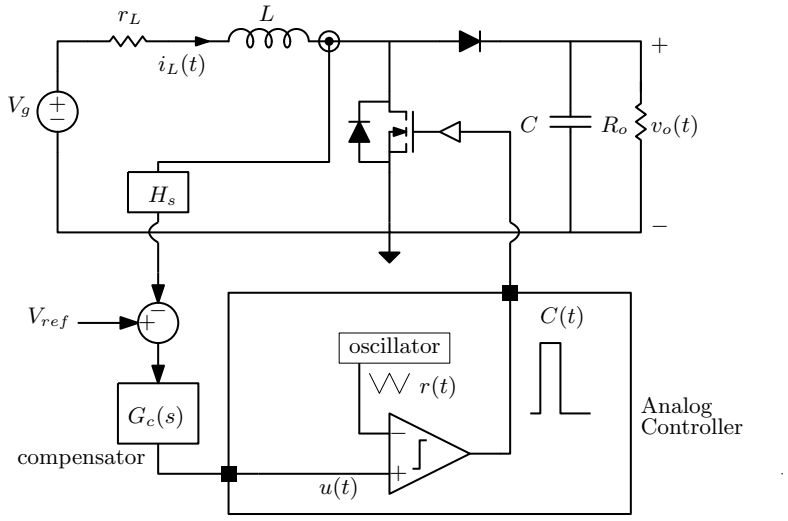


Figure 2.10: *Average current mode control of Boost converter*

And in the second subinterval

$$V_L = v_g(t) - v_o(t), \tag{2.25}$$

$$i_C = -\frac{v_o(t)}{R_o} + i_L(t). \tag{2.26}$$

By averaging, the switching ripple in the inductor current and the capacitor voltage waveforms are removed. So, by averaging of the inductor voltage and the capacitor current waveforms, one has

$$\langle v_L(t)\rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} v_L(\tau)\,d\tau = \langle v_g(t)\rangle_{T_s} - d'(t)\langle v_o(t)\rangle_{T_s}, \tag{2.27}$$

$$\langle i_C(t)\rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} i_C(\tau)\,d\tau = -\frac{\langle v_o(t)\rangle_{T_s}}{R_o} + d'(t)\langle i_C(t)\rangle_{T_s} \tag{2.28}$$

where

$$d'(t) = 1 - d(t). \tag{2.29}$$

As seen, these equations are nonlinear because they contain the multiplication of time-varying quantities. These multiplication signals generates harmonics, and is a nonlinear system. So it is required to linearize equations by a small-signal model. With the hypothesis of driving the converter at

steady-state, $d(t) = D$. With the steady-state analysis and having extinguished after each transients, the inductor current and the capacitor voltage will reach to the dc values I, V. With this assumption, also the input voltage $v_g(t)$ and the duty cycle $d(t)$ are equal to the dc values V_g and D plus several small ac variations $\hat{v}_g(t)$ and $\hat{d}(t)$:

$$\langle v_g(t) \rangle = V_g + \hat{v}_g(t), \tag{2.30}$$

$$d(t) = D + \hat{d}(t). \tag{2.31}$$

The same holds for the inductor and capacitor:

$$\langle i_L(t) \rangle = I_L + \hat{i}_L(t), \tag{2.32}$$

$$\langle v_C(t) \rangle = V_C + \hat{v}_C(t). \tag{2.33}$$

So, the nonlinear equations (2.25) and (2.26) can be linearized with the hypothesis of being smaller the ac variations in magnitude than the dc values:

$$L\frac{d(I_L + \hat{i}_L(t))}{dt} = (V_g + \hat{v}_g(t)) - (D' - \hat{d}(t))(V_o + \hat{v}_o(t)), \tag{2.34}$$

$$C\frac{d(V_C + \hat{v}_C(t))}{dt} = \frac{-(V_o + \hat{v}_o(t))}{R_o} + (D' - \hat{d}(t))(I_C + \hat{i}_C(t)). \tag{2.35}$$

Which leads to:

$$L\left(\frac{dI_L}{dt} + \frac{d\hat{i}_L(t)}{dt}\right) = \underbrace{(V_g - D'V_o)}_{DC\,value} + \underbrace{(\hat{d}(t)V_o + \hat{v}_g(t) - D'\hat{v}_o(t))}_{1^{st}-order\,ac\,value} + \underbrace{(\hat{d}(t)\hat{v}_g(t))}_{2^{nd}-order\,ac\,value}, \tag{2.36}$$

$$C\left(\frac{dV_C}{dt} + \frac{d\hat{v}_C(t)}{dt}\right) = \underbrace{(D'I_C - \frac{V_o}{R_o})}_{DC\,value} + \underbrace{(D'\hat{i}_C(t) - \frac{\hat{v}_o(t)}{R_o} - \hat{d}(t)I_C)}_{1^{st}-order\,ac\,value} - \underbrace{(\hat{d}(t)\hat{i}_C(t))}_{2^{nd}-order\,ac\,value}. \tag{2.37}$$

These equations contain three terms, $DC\,value$, $First-order\,ac\,value$ and $Second-order\,ac\,value$.

It is can be neglected the second-order ac values, as a result of containing the multiplication of time varying signals. On the other hand, the dc value

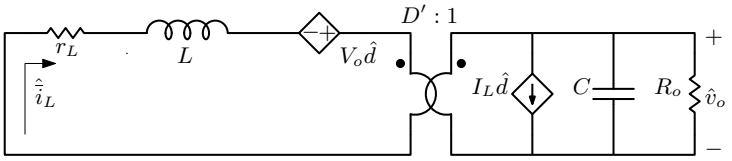


Figure 2.11: *Averaged small-signal model of Boost converter*

can be zero, as a result of the equality to the dc value on the left side of equation. Therefore

$$L\frac{d\hat{i}_L}{dt} = \hat{d}(t)V_o + \hat{v}_g(t) - D'\hat{v}_o(t), \tag{2.38}$$

$$C\frac{d\hat{v}_C}{dt} = D'\hat{i}_C(t) - \frac{\hat{v}_o(t)}{R_o} - \hat{d}(t)I_C. \tag{2.39}$$

So there are the intended small-signal linearized equations that describe the capacitor voltage and the inductor current variations.

2.2.2 Averaged small-signal model

As shown in section. 2.2.1, a small-signal model, can have the equivalent circuit illustrated in Fig. 2.11. For this current control project one needs to calculate the transfer function $G_{id}(s)$. It can be modeled by AC form, that is illustrated in Fig. 2.12. In AC model, it is brought all elements to the elementary and with the thevenin equivalent, represented in Fig. 2.13. As shown in Fig. 2.13, the loop equation is equal to:

$$\begin{aligned} V_{eq} = V_o\hat{d} + \hat{d}\frac{I_L}{D'}\cdot\frac{D'^2R_o}{1+sR_oC} &= \hat{d}V_o\left(1+\frac{1}{1+sR_oC}\right) \\ &= \hat{d}V_o\left(\frac{2+sR_oC}{1+sR_oC}\right) = 2\hat{d}V_o\left(\frac{1+\frac{sR_oC}{2}}{1+sR_oC}\right), \end{aligned} \tag{2.40}$$

where

$$V_o = R_oI_o = R_oD'I_L. \tag{2.41}$$

V_{eq} in the AC model, is represented in Fig. 2.14. As a result, the small-signal

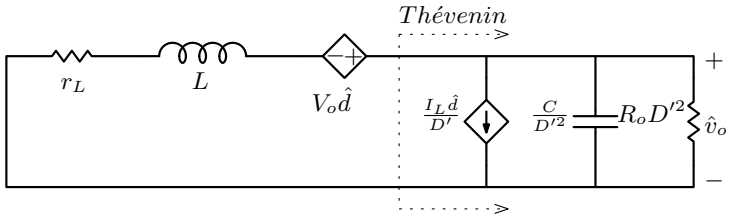


Figure 2.12: *Equivalent circuit of bringing elements to the elementary side*

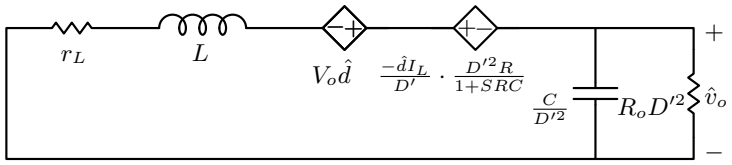


Figure 2.13: *Equivalent circuit of V_{eq} equation (2.40)*

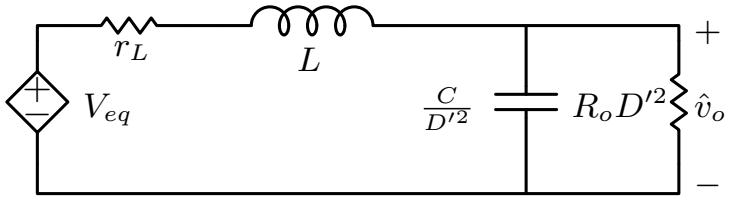


Figure 2.14: *Equivalent ultimate circuit*

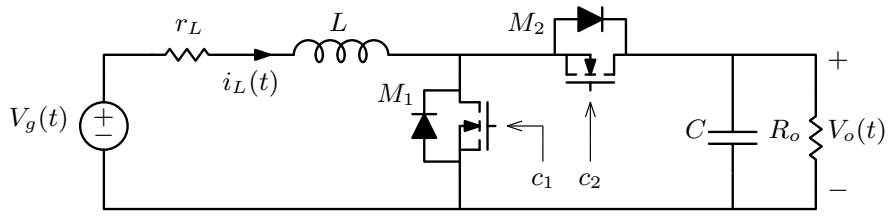


Figure 2.15: *Synchronous Boost converter*

component of the inductor current $\hat{\tilde{i}}_L(s)$ is equal to

$$\begin{aligned}\hat{\tilde{i}}_L(s) &= V_{eq} \cdot \frac{1}{sL + \frac{D'^2 R_o}{1+sR_oC}} \\ = 2\hat{d}V_o\left(\frac{1+\frac{sR_oC}{2}}{1+sR_oC}\right)&\left(\frac{1+sR_oC}{sL+s^2LR_oC+D'^2R_o+r_L+sR_oCr_L}\right) \\ &= \frac{2\hat{d}V_o}{D'^2R_o} \cdot \frac{1+\frac{sR_oC}{2}}{1+\frac{sL+r_L}{D'^2R_o}+\frac{s^2LC+sCr_L}{D'^2}},\end{aligned} \tag{2.42}$$

So the current control transfer function, can be represented by

$$G_{id}(s) = \frac{\hat{\tilde{i}}_L(s)}{\hat{d}(s)} = \frac{2V_o}{D'^2R_o} \cdot \frac{1+\frac{sR_oC}{2}}{1+\frac{sL+r_L}{D'^2R_o}+\frac{s^2LC+sCr_L}{D'^2}}. \tag{2.43}$$

2.3 Synchronous Boost converter

The capability of the MOSFET channel to conduct current in the opposite direction provides the possibility to employ a MOSFET where a diode otherwise would be needed. This implementation of the converter is known as synchronous Boost converter. When the MOSFET is connected, the device can now block negative voltage and conduct positive current, with properties similar to the diode. The MOSFET must be controlled such that it operates in the on state when the diode would be normally conduct, and in the off state when the diode would be reverse-biased. Thus, in the Boost converter, the diode could be replace with a MOSFET, as in Fig. 2.15.

Chapter 3

Digital average current control of Boost converter

3.1 Boost converter case study

As a case study, consider now the digital version of the Boost converter average current control that the block diagram is illustrated in Fig. 3.1. The Boost converter $i_L(t)$ is converted into a sensing voltage $v_s(t)$ by a shunt resistor R_{sense}, compared with a control setpoint V_{ref} and converted a regulation error produced into the control command $u[k]$ by a digital compensator. Then $u[k]$ converts to a necessary gate pulse by symmetrical digital pulse width modulator which is employed with sampling at the midpoints of the turn-on intervals. This process is explained separately at the follows. In the Boost converter, the physical inductor is represented by a sequence of an ideal inductor L and a resistive component r_L, modeling the inductor losses. The converter parameters are listed in table. 3.1.
The Boost converter, has a dc input voltage equal to 5 V and an output voltage equal to 12 V, and can delivered a maximum power of 5 W to a resistive

Input Voltage V_g	5 V
Output Voltage V_o	12 V
Power rating P_o	5 W
Switching Frequency f_S	125 kHz
Filter Inductance L	10 μH
Inductor series resistance r_L	30 mΩ
Filter Capacitance C	311 μF

Table 3.1: *List of parameter's value*

load R_o. So

$$P_o = \frac{{V_o}^2}{R_o} = \frac{12^2}{R_o} = 5\ W \qquad R_o = 28.8\ \Omega. \tag{3.1}$$

The steady-state voltage conversion ratio is

$$M(D) = \frac{V_o}{V_g} = \frac{12}{5} = \frac{1}{1-D} \qquad D = 0.58. \tag{3.2}$$

As shown in section. 2.1.3, for the peak-to-peak current ripple:

$$\Delta i_L = \frac{V_g \cdot D}{f_s \cdot L} = 2.3\ A, \tag{3.3}$$

And for the peak-to-peak output voltage ripple:

$$\Delta V_c = \Delta V_o = \frac{(V_o - V_g)}{f_s \cdot C \cdot R_o} = 6\ mV. \tag{3.4}$$

3.1.1 Digital current-mode control

In this case with digital current-mode control, the inductor current is sampled at the middle of the turn-on interval [8], as illustrated in the diagram of Fig. 3.2.

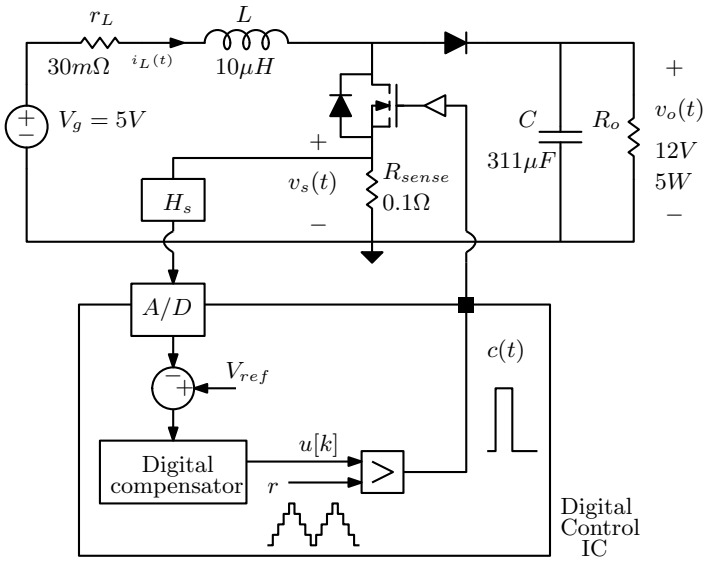


Figure 3.1: *Boost digital current-mode control*

As it will be shown in the next section, the target of this sampling strategy is to regulate the average value of the current and is implemented by employing a symmetrical digital pulse width modulator. The control-to-inductor current, described by the transfer function $G_{id}(s)$, has the form of

$$\begin{aligned} G_{id}(s) &= \left(\frac{2V_o}{r_L + DR_{sense} + D'^2R_o}\right)\left(\frac{1+\frac{sR_oC}{2}}{\Delta(s)}\right) \\ &= \frac{0.19s + 42.3}{1.6\times10^{-7}s^2 + 5.8\times10^{-4}s + 8.9}, \end{aligned} \tag{3.5}$$

where

$$\begin{aligned} \Delta(s) = 1 &+ \left(\frac{s(r_L + DR_{sense})}{D'^2R_o}\right)\left(\frac{R_oC + \frac{L}{r_L+DR_{sense}}}{1+\frac{r_L+DR_{sense}}{D'^2R_o}}\right) \\ &+ \left(\frac{s^2LC}{D'^2}\right)\left(\frac{1}{1+\frac{r_L+DR_{sense}}{D'^2R_o}}\right). \end{aligned} \tag{3.6}$$

The bode plot of transfer function $G_{id}(s)$ is illustrated in Fig. 3.3.

3.1.2 Digital loop control

The Fig. 3.4, shows a block diagram of the small-signal model of a closed-loop regulated converter. In the block diagram, $T(s)$ represents the system

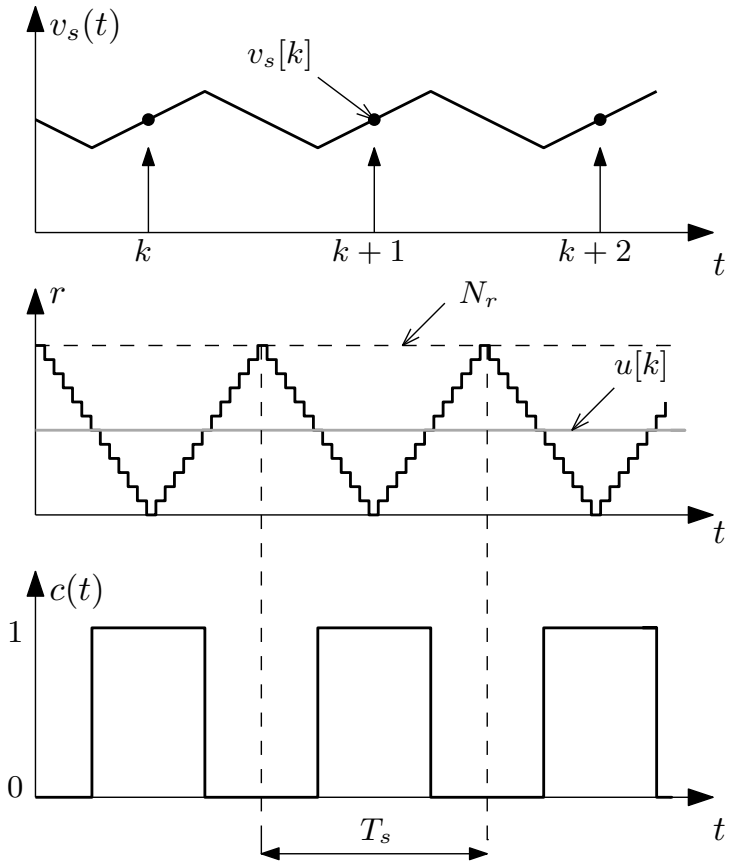


Figure 3.2: *Sample diagram of inductor current*

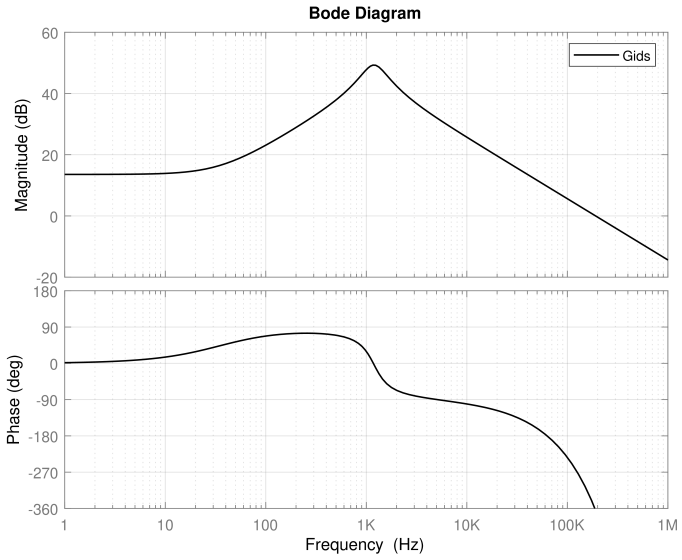


Figure 3.3: *Bode plot of the control to inductor current transfer function*

loop gain and is defined by

$$T(s) = G_c(s)G_{DPWM}(s)G_{id}(s)R_{sense}H_s. \tag{3.7}$$

The $G_c(s)$ represents the compensator transfer function that will be designed in the next section. On the other hand, the compensated loop gain $T_u(s)$ is detrmined when the compensator transfer function has a unit value, $G_c(s) = 1$,

$$T_u(s) = G_{DPWM}(s)G_{id}(s)R_{sense}H_s. \tag{3.8}$$

3.2 A/D conversion

The Fig. 3.5 shows a block diagram of the A/D converter. The process of A/D conversion can be formed as analog input sampling and amplitude quantization [9]. As seen, the analog sensed signal $v_s(t)$ of the Boost converter is specified as input quantization and then by the A/D converter.

- Sampling Rate
  Sampling is synchronized with the PWM carrier. The sensed signal that

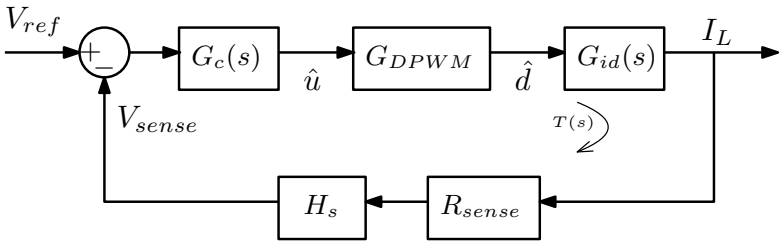


Figure 3.4: *Closed-loop current-mode control*

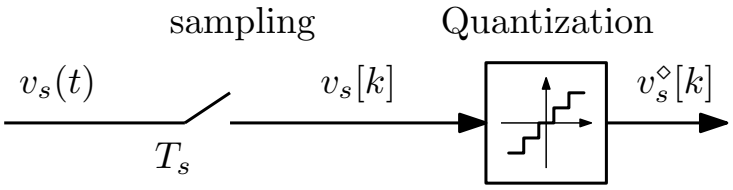


Figure 3.5: *A/D conversion process diagram*

is produced by R_{sense}, consist of switching content at high frequency. On the other hand, in PWM, the variables include an spectrum with dc and low frequency components, as high frequency spectral components focalize in the vicinity of the switching frequency f_s. So some degree of spectral aliasing occurs. For controlling this aliasing, the sampling frequency must be equal to the converter switching frequency. In the digital section, it is required to keep the periodicity, then the sampling rate is constrained to the multiple of f_s.

As it mentioned, $f_{sampling} = f_s$, so the output signal sampling appears once for switching period, as illustrated in the Fig. 3.6. Spectral aliasing now arise around dc. In steady-state, spectral aliasing appears as $v_s(t)$ and switching harmonics present in $v_s(t)$ alias at the dc value, as illustrated in Fig. 3.7. DC spectral aliasing determined by

$$T = T_s. \tag{3.9}$$

Therefore it can be removed the switching harmonics from the feedback signal. As a result, no high-frequency poles are required for attenuating the switching harmonic in the compensator.

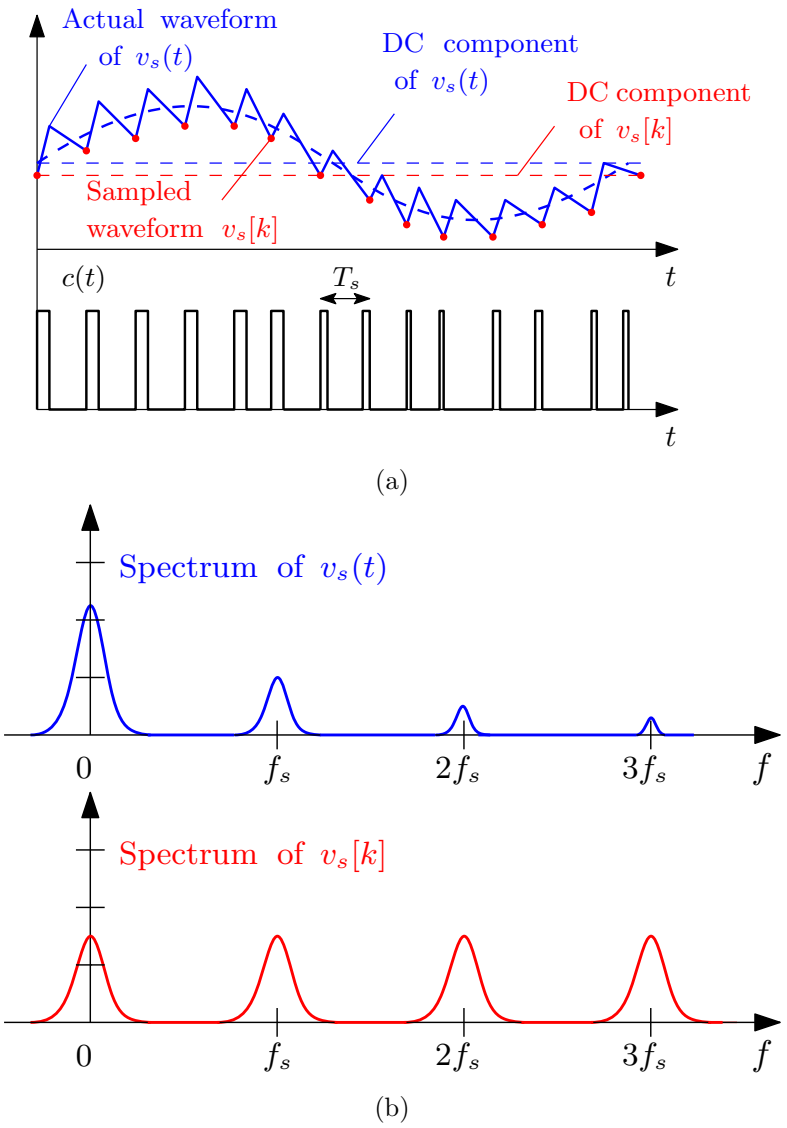


Figure 3.6: *(a) Time-domain waveform of the sensed signal (b) Signal spectrum*

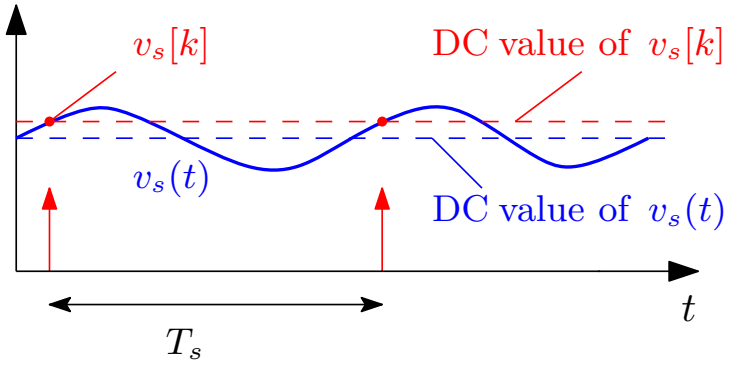


Figure 3.7: *Sampling waveform in A/D conversion*

In digital average current sampling in boost converter, the current switching ripple may not be smaller than its dc value. Then the dc spectral aliasing creates a regulation error. The solution of this problem is to employ a symmetrical PWM modulation with triangular carrier. As illustrated in Fig. 3.8, can be acquired the average value of $i_L(t)$ by its sampling at the PWM carrier peack or valley point.

- Amplitude Quantization
  The internal quantizer of the A/D converter is acquired with a resolution of $n_{A/D}$ bits and over a full-scale range V_{FS}. The A/D parameters are listed in table. 3.2.

Full-scale range V_{FS}	1 V
Bit number $n_{(A/D)}$	11
Setpoint value V_{ref}	0.25 V

Table 3.2: *List of A/D parameters*

The A/D quantization step in $v_s[k]$ is equal to

$$q_{v_s}^{(A/D)} = \frac{V_{FS}}{2^{n_{A/D}}} = \frac{1}{2^{11}} = 4.88 \times 10^{-4}. \tag{3.10}$$

The quantized range introduced into a number of voltage intervals as the linear range, called bins and each bin has $q_{v_s}^{(A/D)}$ wide. The A/D

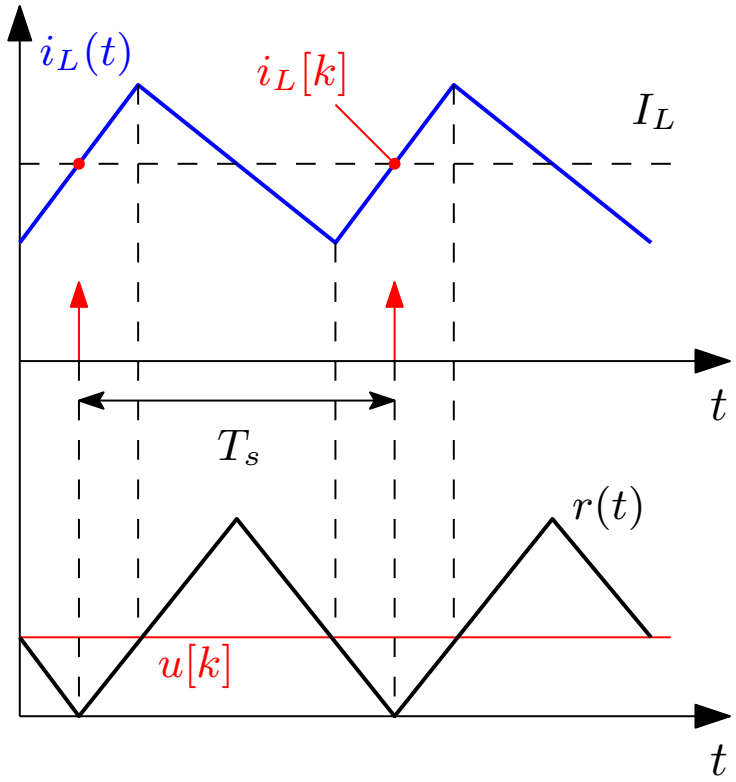


Figure 3.8: *Sampling waveform with accepted PWM*

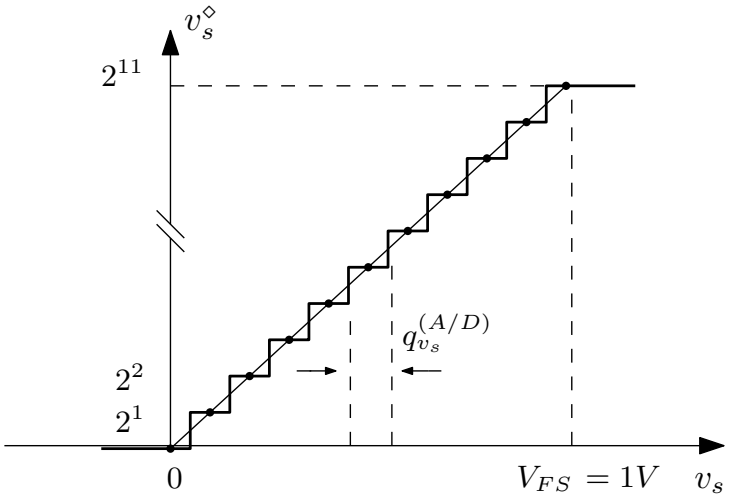


Figure 3.9: *A/D converter quantization*

converter quantization is illustrated in Fig. 3.9. The digital output of the A/D converter $v_s^{\diamond}[k]$ is a binary code of $v_s[k]$ that is given by

$$v_s^{\diamond}[k] = q_{v_s}^{(A/D)} v_s[k], \tag{3.11}$$

In regulation applications, the zero error bin represents the quantization level at the sensed signal v_s and can be regulated by multiplying to the sensing gain ($H_s = 25$). Then, the digital sequence $v_s^{\diamond}[k]$ compares with the control setpoint $V_{ref}[k]$. The resulting of this comparison is a regulation error $e[k]$ that will be processed by the digital compensator in the next section. The setpoint value is identified by

$$V_{ref} = H_s \cdot v_s = 0.25, \tag{3.12}$$

where, with the average current inductor regulated in 1A, the sensing signal is equal to

$$v_s = R_{sense} \cdot I_L = 0.01. \tag{3.13}$$

In this case the Full-scale range (V_{FS}) is equal to 1V that in this range exist the resolution of 11 *bit*, with digital value equal to $2^{11} = 2048$. As it defiend in equation (3.12), with the setpoint value (V_{ref}) of 0.25V it has the digital value equal to 512.

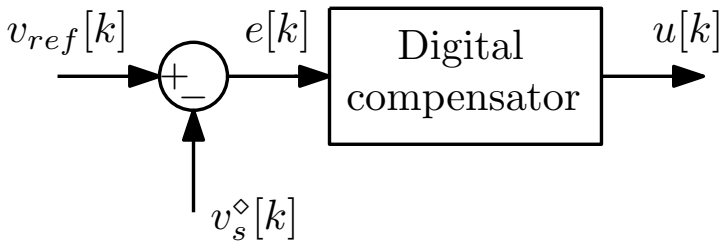


Figure 3.10: *Digital compensator process diagram*

3.3 Digital compensator

The digital compensator updates the control command $u[k]$ on a switching cycle basis from the regulation error $e[k]$, and it's equal to

$$e[k] = v_{ref}[k] - v_s^{\diamond}[k]. \tag{3.14}$$

The block diagram of digital compensator is illustrated in Fig. 3.10.
Some known strategies for design of the compensator transfer function $G_c(s)$ are expressed at the follow:

- Lead (PD) compensator
  This type of compensator is a proportional-derivative controller and it can improve the phase margin. A zero with a frequency f_z lower than the crossover frequency f_c, is added to the loop gain of the compensator and causes to differentiate the error signal. Also the controller contains a pole response at f_p. As a result the compensator transfer function includes a zero and pole, that is defined by

$$G_c(s) = G_{c_0}\left(\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}\right). \tag{3.15}$$

- Lag (PI) compensator
  This type of compensator is a proportional-integral controller and is used to increase the low frequency loop gain. An inverted zero with a frequency f_l lower than the crossover frequency f_c, is added to the loop

gain of the compensator and causes to integrate the error signal. It is described by

$$G_c(s) = G_{c_\infty}\left(1 + \frac{\omega_l}{s}\right). \tag{3.16}$$

- (PID) compensator
  This compensator is proportional-integral-derivative controller and can be combined the properties of PD and PI compensators. PID compensator by integrating the error signal at low frequencies can improve the steady-state response, and by improving the phase margin at high frequencies can have a good transient behaviour.

For designing the compensator, two techniques are discussed at the follow.

3.3.1 Continuous-time modeling approach

Continuous-time model is the pure s-domain approach. Based on averaged small-signal models explained in previous section for analog control design. The block diagram of this modelling is illustrated in Fig. 3.11. As seen, the proportional,integral and derivative gains (K_p, K_i, K_d respectively), can be regulated independently. Equation of the analog PID compensator can be described by

$$\begin{aligned} u(t) &= u_p(t) + u_i(t) + u_d(t) \\ &= K_p e(t) + K_i \int e(\tau)d\tau + K_d \frac{de(t)}{dt}, \end{aligned} \tag{3.17}$$

in the s-domain

$$G_{PID}(s) = G_c(s) = \frac{u(s)}{e(s)} = K_p + \frac{K_i}{s} + sK_d. \tag{3.18}$$

As the modulator and converter are modeled in the continuous-time domain, the uncompensated loop gain of Boost converter is equal to

$$T_u(s) = G_{id}(s)G_{DPWM}(s)R_{sense}K_{AD}e^{-st_{PWM}}. \tag{3.19}$$

After a continuous-time control transfer function $G_c(s)$ is determined via analog control design, can be continued with its discretization.

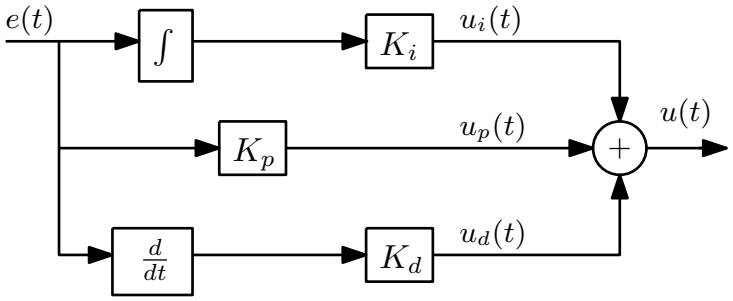


Figure 3.11: *Continuous-time PID compensator digram*

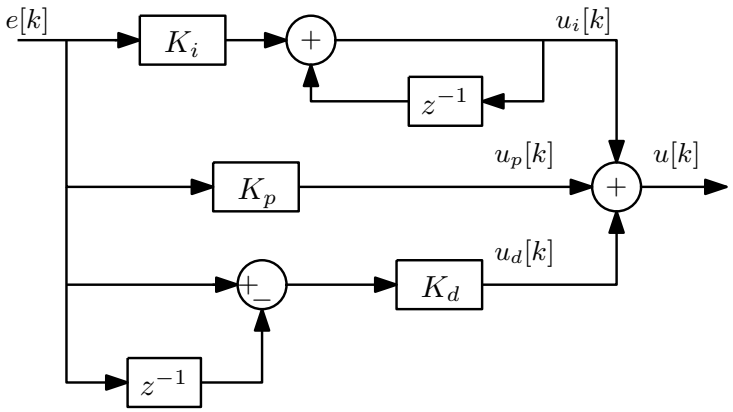


Figure 3.12: *Discrete-time PID compensator diagram*

3.3.2 Discretization-based modeling approach

The method based on impulse response discretization and converts a continuous-time system into a discrete-time system [12, 13]. So the compensator can be defined by transforming the s-domain into the z-domain:

$$G_{PID}(z) = G_c(z) = K_p + \frac{K_i}{1 - z^{-1}} + K_d(1 - z^{-1}). \tag{3.20}$$

As is illustrated in Fig. 3.12.
According to the discretization-based approach, the continuous-time uncompensated loop gain (3.19) must be discretized by

$$T_u(z) = T_s Z[T_u(s)], \tag{3.21}$$

where $Z[T_u(s)]$ defines the operation of impulse-invariant discretization, that can be performed by using Matlab command c2d.
Various methods exist to synthesize $G_c(z)$. One is the *bilinear transform* method that is explained as follow.

3.3.2.1 Bilinear transform design

As a first step, the uncompensated loop gain $T_u(z)$ and the designed compensator transfer function $G_c(z)$,are mapped into an analog equivalent. So it needs to transfer from z-domain to p-domain by mapping principle of

$$z(p) = \frac{1 + p\frac{T_s}{2}}{1 - p\frac{T_s}{2}}, \tag{3.22}$$

The result of this mapping is the compensator function defined as

$$G'(p) = G(z(p)). \tag{3.23}$$

Then the compensator designed in p-domain is brought to the z-domain by an inversion map

$$p(z) = \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}}, \tag{3.24}$$

and now, can be implemented into the digital controller.
Therefore $T'_u(p)$ has been acquired from the bilinear transform of $T_u(z)$, where

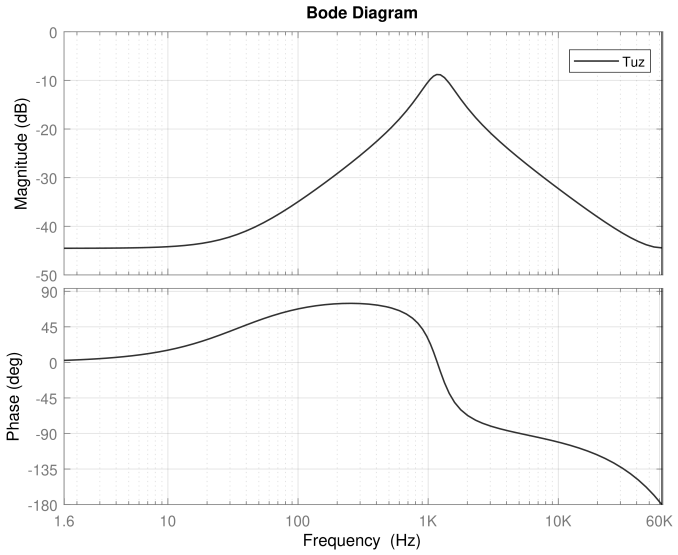


Figure 3.13: *Bode plot of the uncompensated loop gain* $T_u(z)$

$T_u(z)$ is mentioned through (3.21). Target is to synthesize a digital compensator from frequency-domain specifications as control bandwidth ω_c and phase margin φ_m.
In the case of study, $\varphi_m = 45°$ and crossover frequency is equal to $f_c = f_s/10$. Then

$$\omega_c = 2\pi(12.5\,kHz) = 7.85 \times 10^4. \tag{3.25}$$

By the crossover frequency which desired to control bandwidth, frequency distortion represented by the bilinear transform has been neglected. As it has been needed to compensate the frequency distortion, one of the solutions is transform the control bandwidth specification ω_c into a corresponding specification ω_c' in the p-plane and define as prewarping operation

$$\omega_c' = \omega_p \tan\frac{\omega_c}{\omega_p} = 8.12 \times 10^4, \tag{3.26}$$

Where

$$\omega_p = 2f_s = \frac{2}{T_s} = 25 \times 10^4. \tag{3.27}$$

The bode plot of the uncompensated loop gain is illustrated in Fig. 3.13. As

it seen, in the bode plot of the uncompensated loop gain, the magnitude and phase at the desired crossover frequency will be express as

$$\begin{aligned} \left|T_u(z=e^{j\omega_c T_s})\right| &= |T'_u(p=j\omega'_c)| = 1.94\times 10^{-2}, \\ \angle T_u(z=e^{j\omega_c T_s}) &= \angle T'_u(p=j\omega'_c) = -105^\circ. \end{aligned} \tag{3.28}$$

Then, the uncompensated phase margin will be equal to

$$\varphi_{m,u} = \pi + \angle T'_u(p) = \pi + \angle T_u(z) = 75^\circ. \tag{3.29}$$

As it is reported in value of uncompensated phase margin, it dosen't need to improve the phase margin. So consider just a PI compensator for increasing low-frequency loop gain. Obviously in PI compensator, derivative gain is equal to zero ($K_d = 0$).

As following the bilinear transform design, the form of PI compensator in the p-domain will be written as

$$G'_{PI}(p) = G'_{PI\infty}\left(1 + \frac{\omega_{PI}}{p}\right). \tag{3.30}$$

By imposing the target phase margin prossess

$$\angle T'(p) = \angle T'_u(p) + \angle G'_{PI}(p) = -\pi + \varphi_m, \tag{3.31}$$

it follows

$$\begin{aligned} \arctan\left(\frac{\omega_{PI}}{\omega_c}\right) &= -\pi + \angle T'_u(p) + \varphi_m = \varphi_m + \varphi_{m,u}, \\ \omega_{PI} &= \omega'_c \tan(\varphi_{m,u} - \varphi_m) = 4.64\times 10^4. \end{aligned} \tag{3.32}$$

As for the crossover frequency limitation,

$$|G'_{PI}(p)| \cdot |T'_u(p)| = 1 \tag{3.33}$$

Which yields

$$G'_{PI\infty} = \frac{1}{|T'_u(p)| \cdot \sqrt{1 + (\frac{\omega_{PI}}{\omega_c})^2}} = 44.36. \tag{3.34}$$

So, the p-domain parameters $(G'_{PI\infty}, \omega_{PI})$ have been determined at above, the PI gains K_p, K_i (proportional and integral gains) of digital compensator

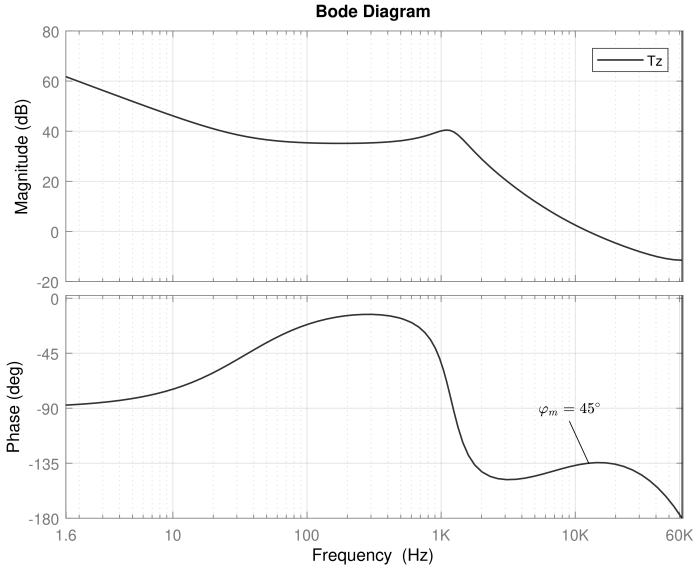


Figure 3.14: *Bode plot of the compensated loop gain $T(z)$*

by the conversion equations from p-domain to the z-domain are calculated as

$$G'_{PI}(p) = K_p + \frac{K_i}{T_s}\frac{1+\frac{p}{\omega_p}}{p}, \tag{3.35}$$

Where

$$\begin{aligned} G'_{PI\infty} &= K_p + \frac{K_i}{2}, \\ \omega_{PI} &= \frac{\omega_p}{1+\frac{2K_p}{K_i}}. \end{aligned} \tag{3.36}$$

Then

$$\begin{aligned} K_p &= G'_{PI\infty}\left(1-\frac{\omega_{PI}}{\omega_p}\right) = 36.12, \\ K_i &= G'_{PI\infty}\frac{2\omega_{PI}}{\omega_p} = 16.49. \end{aligned} \tag{3.37}$$

The z-domain compensator loop gain $T(z) = D_c(z)T_u(z)$ is illustrated in Fig. 3.14.

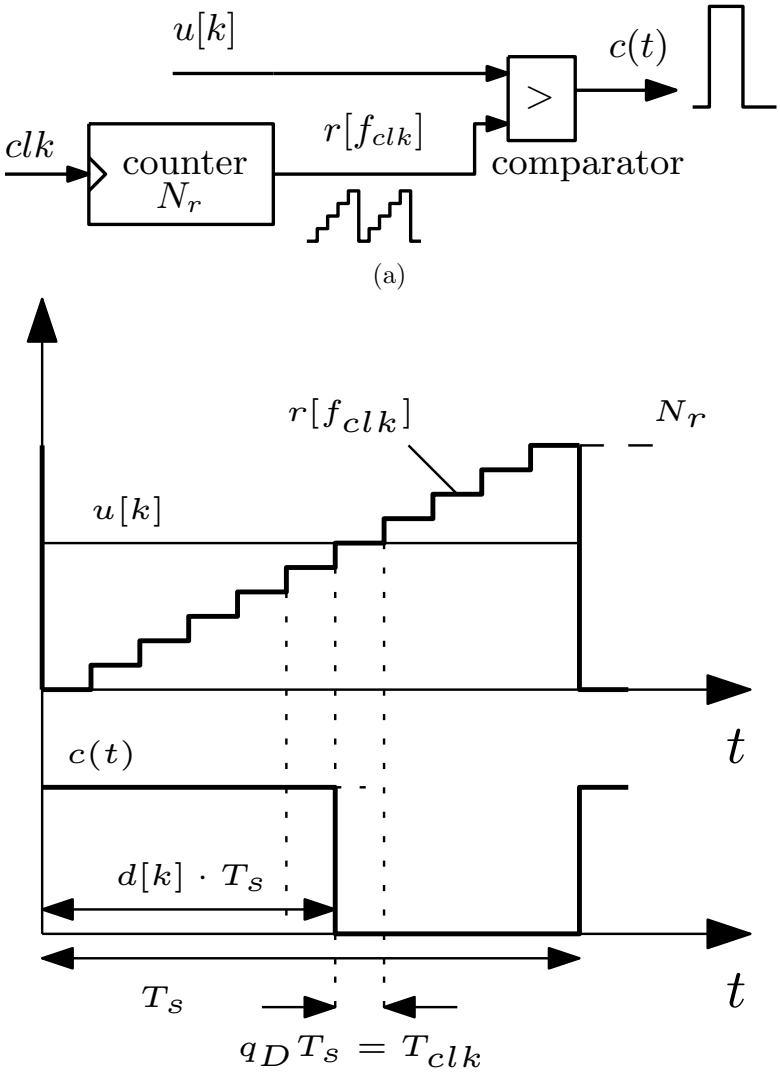


Figure 3.15: *(a) Counter-based DPWM diagram (b) associated waveform*

3.4 Digital pulse width modulation(DPWM)

The function of DPWM generates a square wave as a pulse with duty cycle $d[k]$ proportional to control command $u[k]$ that is acquired on a sampling rate [14]. In this case consider a counter-based DPWM for generating $C(t)$, which is illustrated its diagram in Fig. 3.15. The $N_r = 200$ counter clocked at frequency $f_{clk} = 50$ MHz and generates PWM carrier $r[f_{clk}]$ with amplitude N_r and period T_s. Time resolution can be determined by T_{clk}.The clocked frequency f_{clk} is proportional to switching frequency f_s, number of bit n_{DPWM} and can be expressed by

$$T_{clk} = T_s \cdot 2^{n_{DPWM}} \tag{3.38}$$

In the counter, as a number of the bits n_{DPWM} goes higher, therefore resolution goes higher too. In DPWM, the input control command $u[k]$ is compared with the PWM carrier $r[f_{clk}]$ on a clock cycle, so a pulse is produced with duty cycle as

$$d[k] = \frac{u[k]}{N_r}, \tag{3.39}$$

and in the steady-state is equal to

$$D = \frac{U}{N_r}. \tag{3.40}$$

Where

$$N_r = \frac{F_{clk}}{f_s} = \frac{T_s}{T_{clk}}. \tag{3.41}$$

Therefore, the duty cycle D depends on the control command and carrier amplitude.

The minimum duty cycle resolution can be defined by

$$q_D = \frac{1}{N_r} = \frac{1}{2^{n_{DPWM}}}, \tag{3.42}$$

and minimum command variation of the modulator can be defined by

$$q_u = q_D N_r = \frac{N_r}{2^{n_{DPWM}}}. \tag{3.43}$$

On the other hand, q_D produces a variation $q_{v_o}^{(DPWM)}$ by

$$q_{v_o}^{(DPWM)} \cong \frac{\partial M}{\partial D} V_g q_D, \tag{3.44}$$

as in the Boost converter $M(D) = 1/(1-D)$, it is estimated by

$$q_{v_o}^{(DPWM)} \cong \frac{1}{(1-D)^2} V_g q_D = \frac{q_u}{N_r} \frac{V_g}{(1-D)^2}. \tag{3.45}$$

The three types of counter based technique modulators are trailing-edge, leading-edge, and symmetrical (triangle-wave) modulator.

3.4.1 Modulation Delay

The modulation delay is an important part of digital control design for setting the necessary delay time in digital modulator. The small signal frequency response of PWM can be defined by

$$G_{PWM}(j\omega) = A_{PWM}(j\omega) e^{-j\omega_{PWM}}. \tag{3.46}$$

The function A_{PWM} is a real value approximately equal to $1/N_r$ with negligible loss in modeling design. on the other hand, t_{DPWM} is the small signal delay and depends on the type of modulation and duty cycle D.

- Trailing-edge modulation
  In this type of modulation, the counter is an up counter. As, the DPWM is turned on by the clock signal and is turned off by output of the comparator. The waveform for the trailing-edge modulation is illustrated in Fig. 3.16. As seen, the time delay of DPWM is equal to

  $$t_{DPWM} = DT_s. \tag{3.47}$$

  So, the expression of small signal frequency response is equal to

  $$G_{PWM,TE}(j\omega) = \frac{1}{N_r} e^{-j\omega DT_s}. \tag{3.48}$$

- Leading-edge modulation

  In this type of modulation, the counter is a down counter. As, the output of the comparator is turned on the DPWM pulse and DPWM is turned off at the end of switching cycle. The Fig. 3.17, is illustrated the waveform for the leading-edge modulation. as seen, the time delay of DPWM is equal to

$$t_{DPWM} = (1 - D)T_s, \tag{3.49}$$

  So, the expression of small signal frequency response is equal to

$$G_{PWM,LE}(j\omega) = \frac{1}{N_r} e^{-j\omega(1-D)T_s}. \tag{3.50}$$

- symmetrical modulation

  In this type, the counter is an up-down counter. In one half of the switching cycle the counter operation is as either up or down and in the other half of the cycle its operation is as either down or up. So, half of the switching cycle is same as the leading edge and other half is same as the trailing edge. Therefore, in this modulation both of turn on and turn off delay times exists. The Fig. 3.18, is illustrated the waveform for the symmetrical DPWM. as seen, the time delay of DPWM is equal to

$$t_{DPWM} = \frac{T_s}{2}, \tag{3.51}$$

  So, the expression of small signal frequency response is equal to

$$G_{PWM,Symm}(j\omega) = \frac{1}{N_r} e^{-j\omega\frac{T_s}{2}}. \tag{3.52}$$

  In this case study, in digital current mode control of boost converter, exist an symmetrical modulation as DPWM modulator with time delay equal to $T_s/2$.

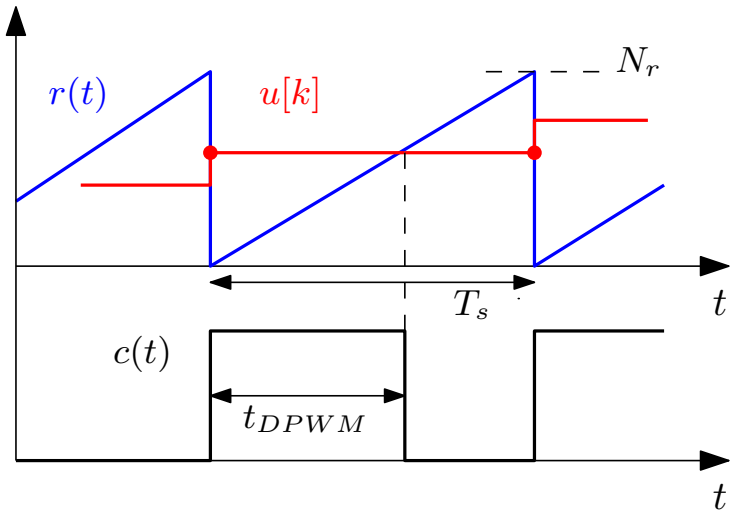


Figure 3.16: *Trailing-Edge modulation*

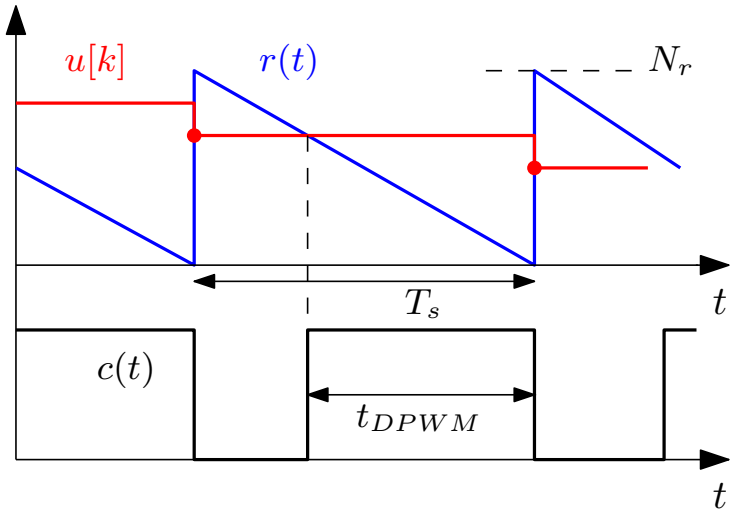


Figure 3.17: *Leading-Edge modulation*

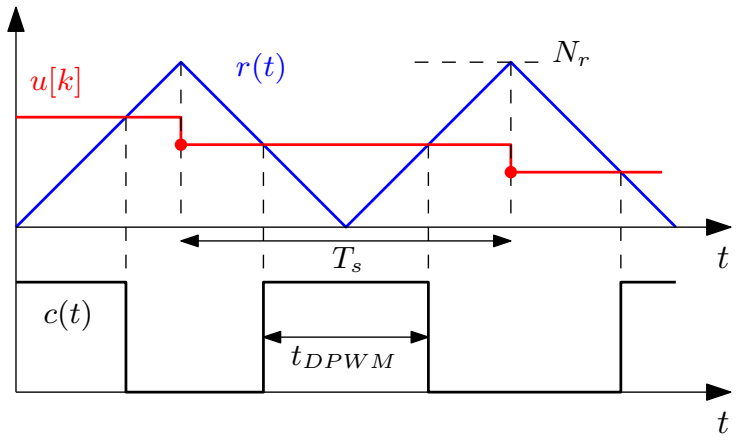


Figure 3.18: *Summetrical modulation*

Chapter 4

Simulation and results

4.1 Open-loop system

The first, operate the Boost converter in open-circuit without any feedback of the regulator, which the values of its parameters are reported in table. 3.1. The model of the system in Matlab program is reported in appendix A by Fig. A1, and Matlab code for this model is given in appendix B part B.1. Also the Boost converter block diagram and PWM block diagram are reported on appendix A by Fig. A2, Fig. A3. In order to achieve the value of the output voltage 12 V, peak-to-peak inductor current ripple 2.3 A and peak-to-peak output voltage ripple 6 mV, represent the simulation result in Fig. 4.1. As seen, the voltage of Boost converter amount has been reached 12 V approximately with $\Delta V_o \cong 6$ mV. The inductor current has peak-to-peak ripple amount 2.3 A.

4.2 Closed-loop system

Now consider the Boost converter with digital average current-mode control of inductor equal to 1 A that its block diagram reported in appendix A by Fig. A4. As mentioned in previous sections, the converter is modulated by a symmetrical modulator having a carrier amplitude $N_r = 200$. The inductor

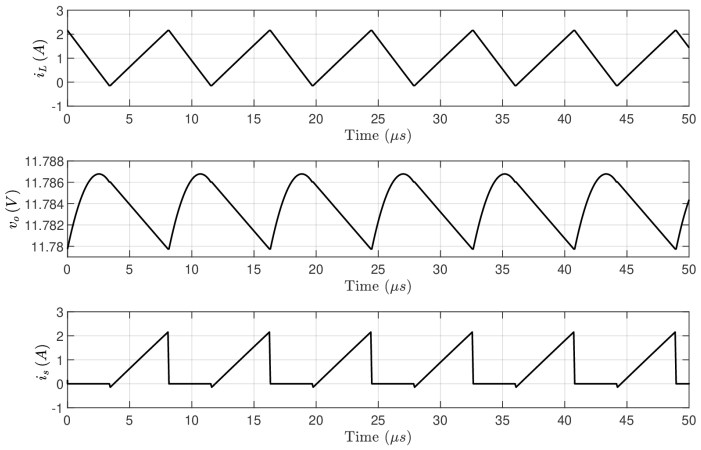


Figure 4.1: *Open loop waveforms in steady state: (Top: inductor current), (Middle: output voltage), (Bottom: switch current)*

current is sampled at the midpoints of the turn-on intervals and, the control command $u[k]$ latches at the valley point of each switching period.

4.2.1 Controlling with integral compensator

Let's start first with integral compensator. The idea is a low band control with frequency equal to $f_c = 5$ Hz, so it would be needed an small K_i.
The integral compensator block digram in Matlab based on the code given in appendix B part B.2, is reported in appendix A by Fig. A5. As seen, $K_p = 0$ and integral gain value K_i calculated based on discretization approach, is equal to 0.041. The Fig. 4.2 can be represented as simulation result of the integral controller.

4.2.2 Controlling with PI compensator

Now with adding proportional gain as a PI compensator reported in appendix A by Fig. A6, based on the Matlab code in appendix B part B.3, the inductor current can be controlled as shown the simulation result in Fig. 4.3. As seen, the average value controlled of inductor current is equal to 1 A. The

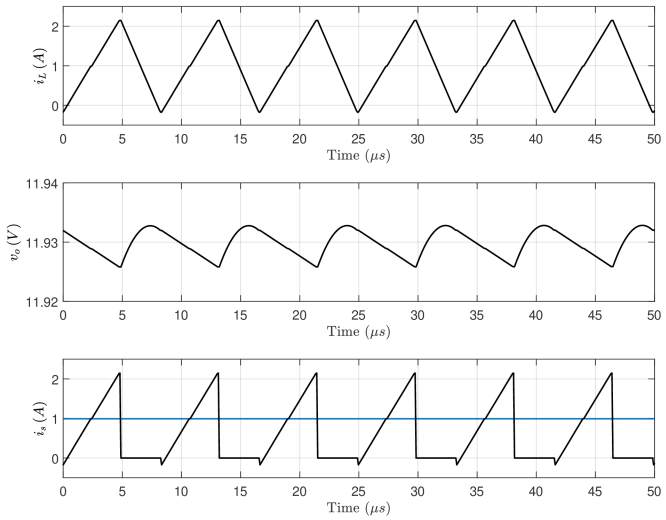


Figure 4.2: *Closed-loop waveforms in steady state by integral compensator: (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

output Voltage of Boost converted amount has been reached approximately to 12 V and, average value of the switch current (i_s) is equal to 1 A that is sampled at the midpoint of the on state switching period. The stabled sample signal is illustrated in blue.

In the following, consider the transient function at the switching frequency. With step-up transient in the load current of the Boost converter from 416 mA to 466 mA, Fig. 4.4 illustrates the simulated closed-loop response. As seen, with this transient the inductor current and switch current remain in the steady state situation, and the output voltage is changed. Obviously with keep on adjusting the input current $i_L(t)$, the input voltage V_g is fixed. It means that it is absorbing the same power. As a result, the same power exists on the load with assuming unitary efficiency $\eta = 1$. So with increasing the load current I_o, the output voltage V_o must be decreased and reaches to its steady-state (the minimum value), which is shown clearly in the Fig. 4.5.

With step-up transient in the input voltage V_g of the Boost converter from

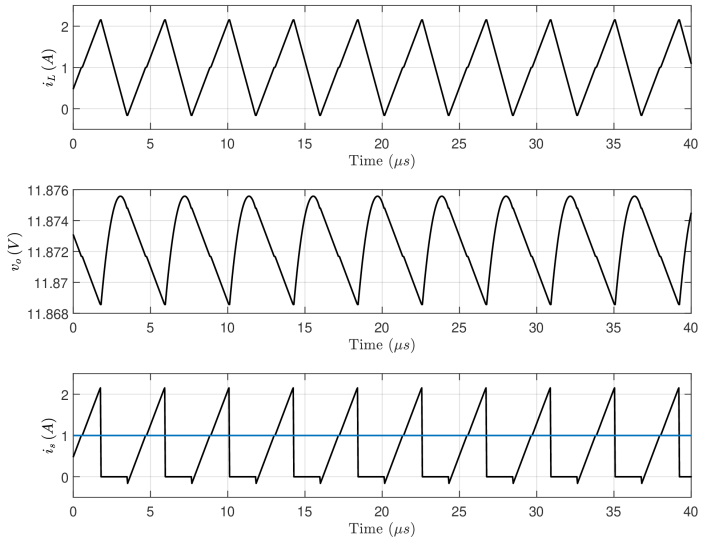


Figure 4.3: *Closed loop waveforms in steady state by PI compensator: (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

5 V to 6 V, Fig. 4.6 illustrates the simulated closed-loop response. As seen, when the input voltage V_g is increasing, the inductor must throw the load on the capacitor. So there will be a transient condition and then it will back to normal with averaged value equal to 1 A. There is also this same situation for the switch current and its sample signal. On the other hand, with increasing the input voltage V_g, also the input power is increased. Then the power on the load is increased by increasing the output power. So the output voltage V_o must be increased and reaches to its steady-state (the maximum value). With step-up transient in the set point value V_{ref} from 0.25 to 0.375, Fig. 4.8 illustrates the simulated closed-loop response. As it mentioned, in the set point value equal to 0.25, the system can be regulated the inductor averaged current equal to 1 A, and with this increasing regulates the inductor averaged current equal to 1.5 A. So as seen in the simulated response, it will be a transient condition about 0.5 A increasing for averaged value of the inductor current, switch current and its sampled signal. On the other hand with

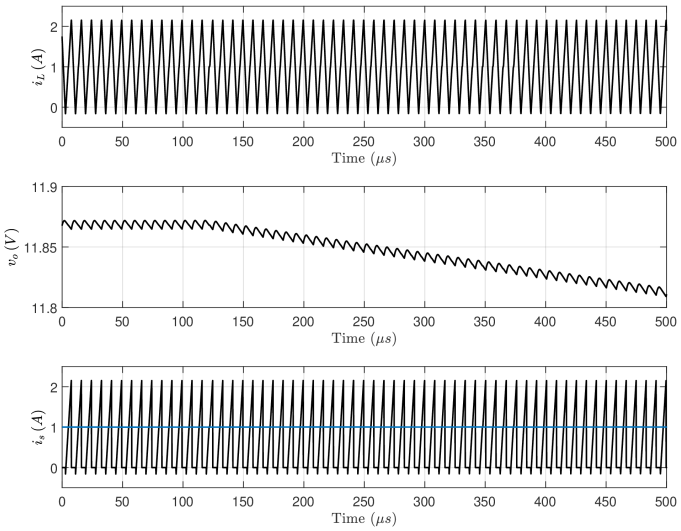


Figure 4.4: *Closed-loop response to* $50\,mA$ *step in output current* $(416\,mA \longrightarrow 466\,mA)$*: (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

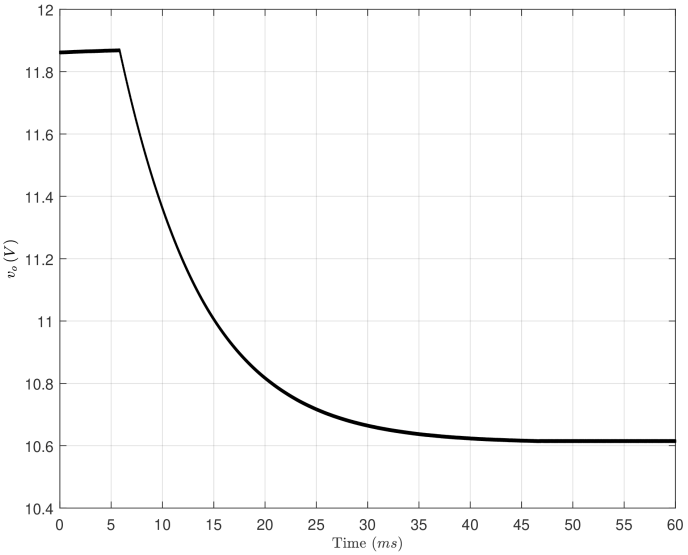


Figure 4.5: *Output voltage response to* $50\,mA$ *step in output current* $(416\,mA \longrightarrow 466\,mA)$

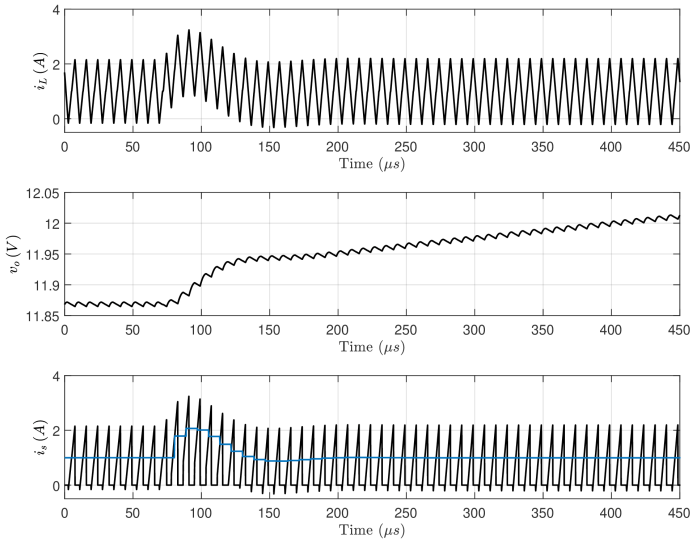


Figure 4.6: *Closed-loop response to* $1\,V$ *step in input voltage* ($5\,V \longrightarrow 6\,V$)*: (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

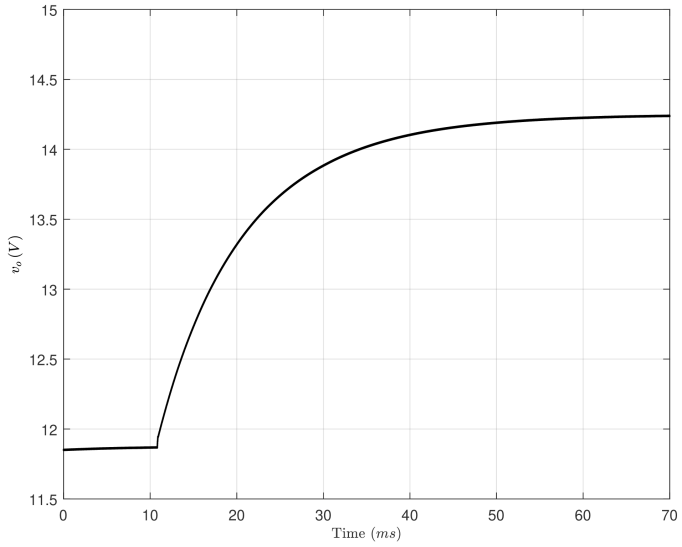


Figure 4.7: *Output voltage response to* $1\,V$ *step in input voltage* ($5\,V \longrightarrow 6\,V$)

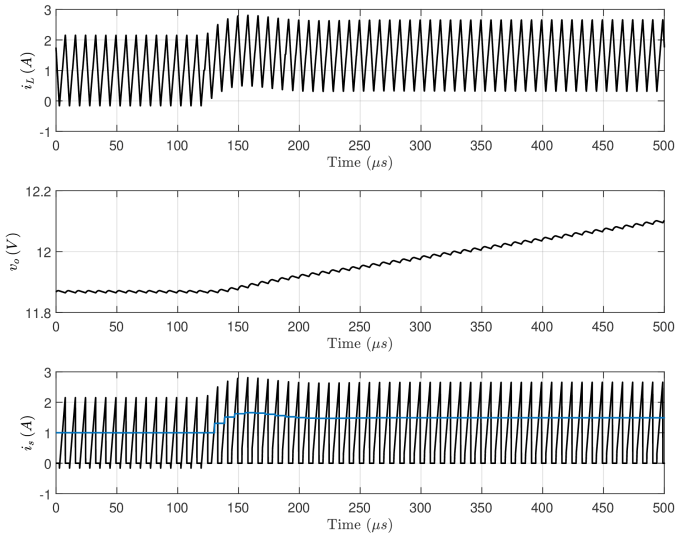


Figure 4.8: *Closed-loop response to* 0.125 *step in set point (*0.25 $\longrightarrow$ 0.375*): (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

increasing the input current due to increased V_{ref}, input power is increased and because of absorption the same power at the output side, the output voltage V_o must be increased and reaches to its steady-state (the maximum value).

With transient in the set point value V_{ref} from 0.25 to 0.5, Fig. 4.10 illustrates the simulated closed-loop response. As a same at $V_{ref} = 0.5$, can be regulated the inductor averaged current equal to 2 A. So exists a transient condition about 1 A increasing for the inductor current, switch averaged current and its sampled signal. Also with increasing the input current, the output voltage V_o will be increased and reaches to its steady-state (the maximum value).

To verify the phase margin of the system φ_m, it is necessary injecting a perturbation at the output of the PI compensator with a frequency equal to the f_c and having an amplitude about of $\frac{1}{10}$, at the sample time T_s. Its block diagram is illustrated in Fig. 4.12.

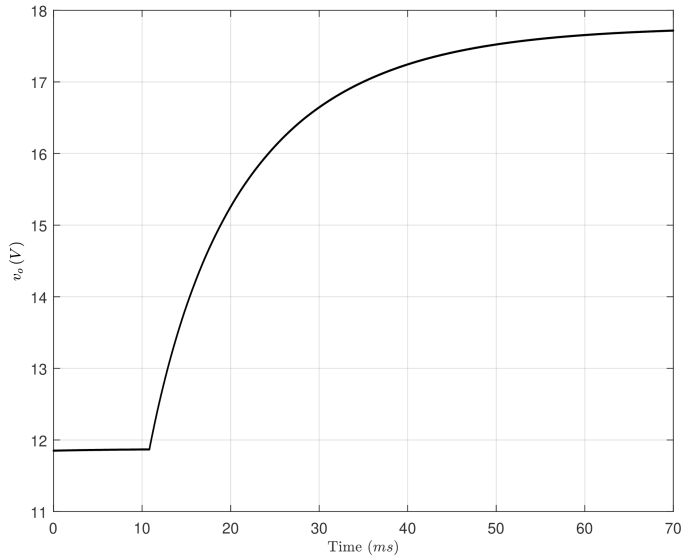


Figure 4.9: *Output voltage response to* 0.125 *step in set point (*0.25 $\longrightarrow$ 0.375*)*

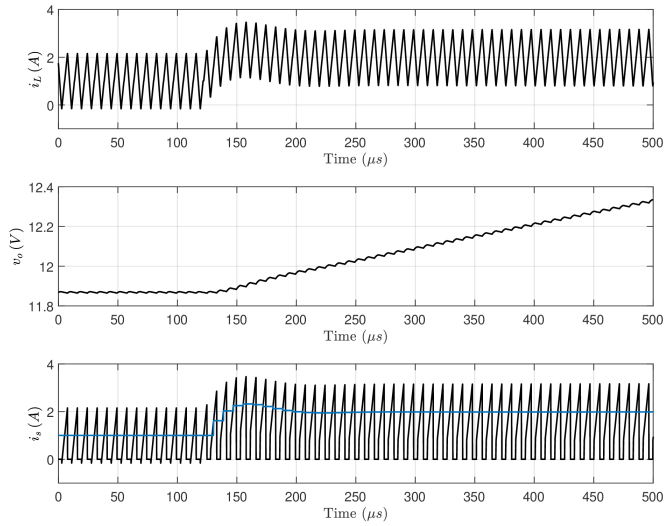


Figure 4.10: *Closed-loop response to* 0.25 *step in set point (*0.25 $\longrightarrow$ 0.5*): (Top: inductor current), (Middle: output voltage), (Bottom: sampled switch current)*

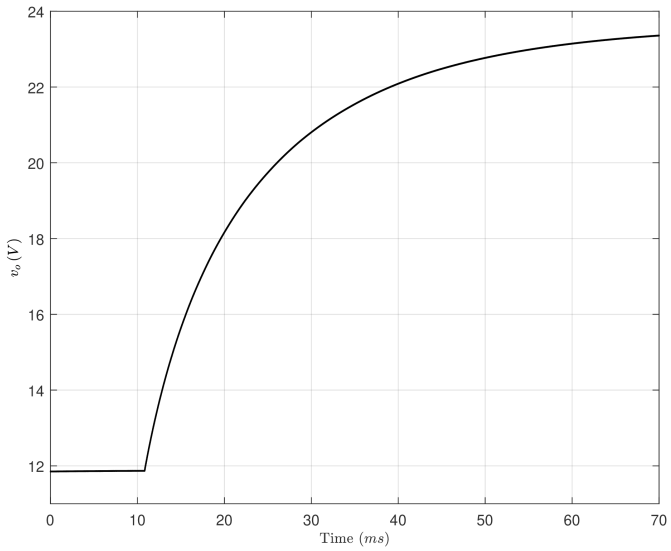


Figure 4.11: *Output voltage response to* 0.25 *step in set point (*$0.25 \longrightarrow 0.5$*)*

As it is known, before and after the injection point, signal amplitude is connected at the system compensated loop gain $T(s)$. So as illustrate in Fig. 4.13, the relation is equal to

$$\frac{u_y}{u_x} = -T(j\omega_c). \tag{4.1}$$

Then the phase is defined by

$$\angle\frac{u_y}{u_x} = \pi + \angle T(j\omega_c) = \pi + (-\pi + \varphi_m) = \varphi_m. \tag{4.2}$$

As illustrated the simulation result in Fig. 4.14, we have two signal u_y and u_x before and after the injection point with the same amplitude and a time difference ΔT between them, that is defined by

$$\Delta T = \frac{\varphi_m}{\omega_c}. \tag{4.3}$$

So the time difference value as it is shown, is equal to 0.01 ms. Therefore the phase margin is verified by

$$\varphi_m = 0.78(rad) = 0.78 \cdot \frac{180}{\pi} = 45^\circ. \tag{4.4}$$

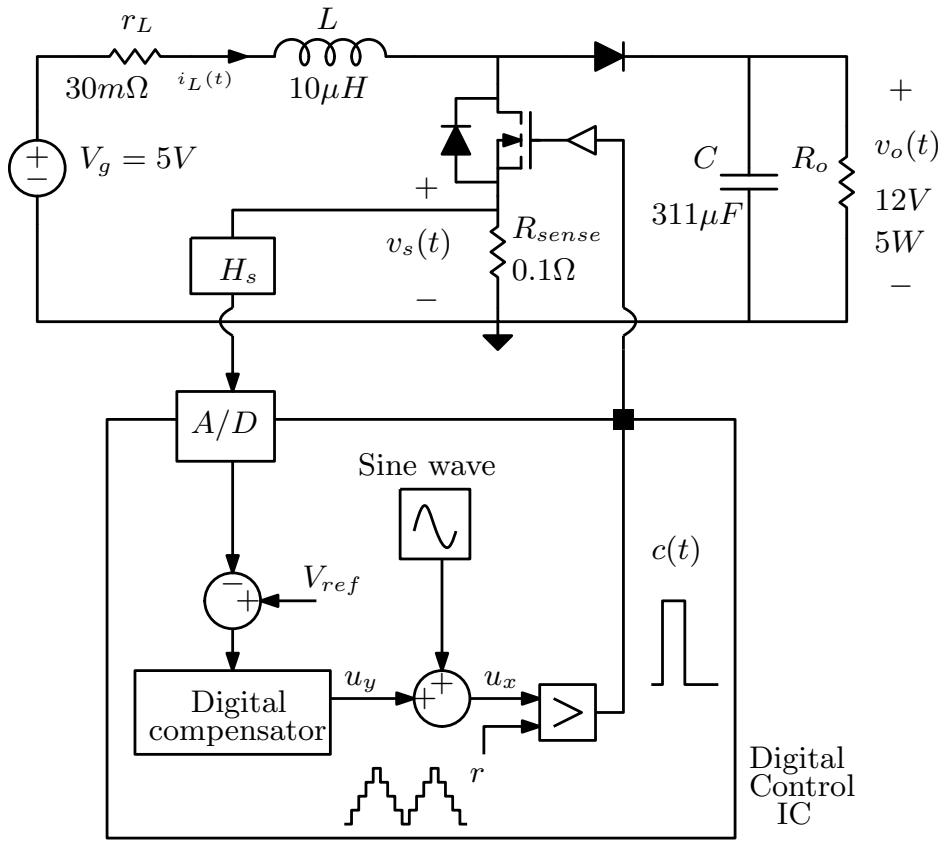


Figure 4.12: *The block diagram of digital current control with injecting perturbation*

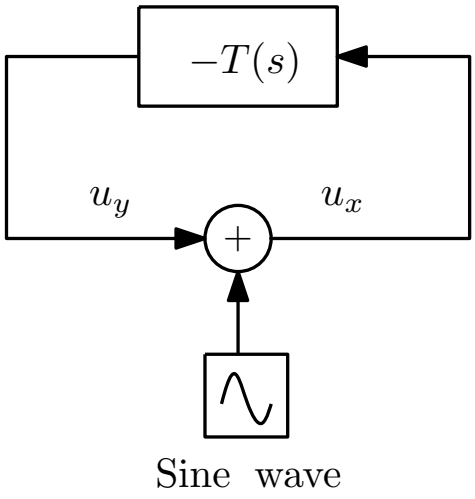


Figure 4.13: *Definition of the loop gain $T(s)$ at the injection point*

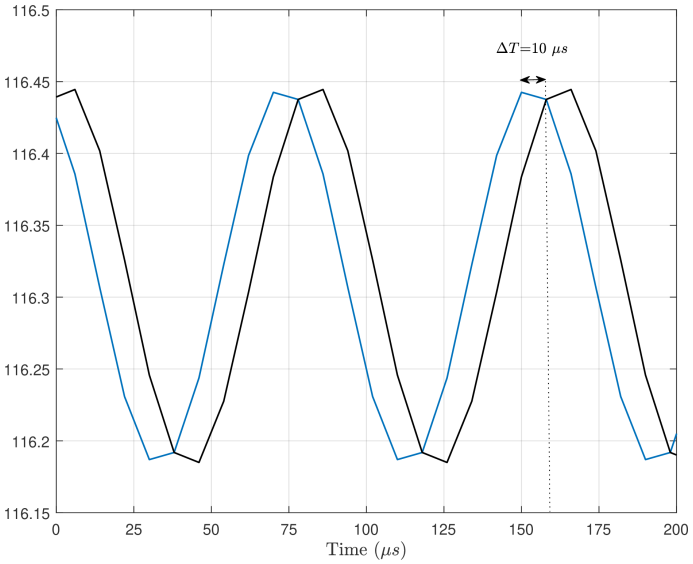


Figure 4.14: *u_y and u_x signals before and after injection*

Chapter 5

Experimental verification

5.1 Prototype

The block diagram of the digital current-mode controller used in the project, is illustrated in Fig. 5.1. As shown, the process is included a Power Board interfaced to an FPGA Board via a 40 pin I/O connector.

5.1.1 Power board

The power board consists of a dc-dc Boost converter which its parameters are reported in table. 3.1, with a current sensing channel H_s and a A/D converter. For the measurement, operate the Boost converter by connecting the physical load $R_o = 22\ \Omega$ to the converter output. It should be noted the driver supply voltage is 14 V and the inductor saturation current $I_{L,sat} = 3.8$ A.

5.1.2 FPGA board

Now, the process is configuring and implementing the power circuit in an actual FPGA device. FPGA is an integrated circuit designed that is programmed by using a hardware description language VHDL realized in the Quartus Prime software which is coded for this implementation [16]. Then

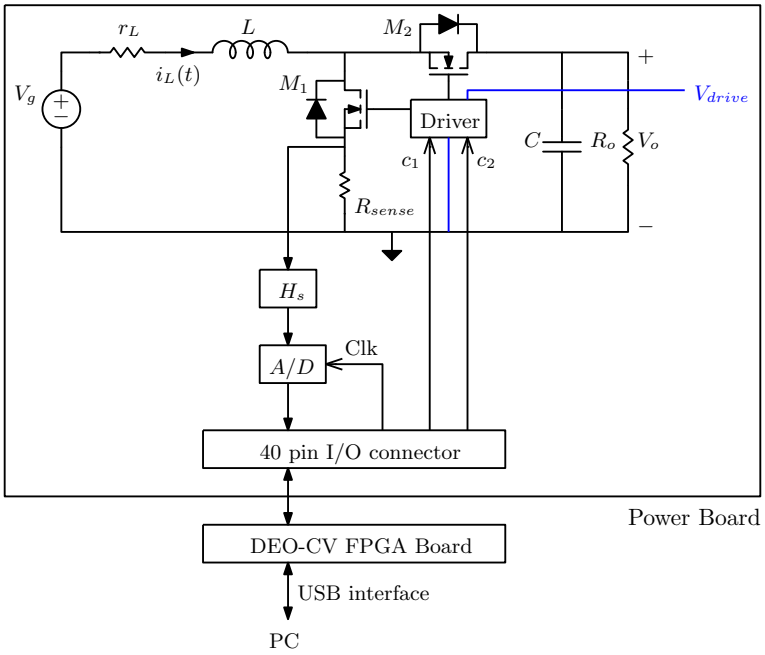


Figure 5.1: *The prototype block diagram, consist of a power board and a FPGA board*

can be measured the required values by importing control commands into the PC-console, such as achieve $V_o = 12$ V, must be set the control command U into the PC-console of programming file in the open-loop operation. On the other hand in the closed-loop operation, first it is needed to carried out all calculations into the fixed-point arithmetic [15], as will be explained in the next section, and then importing them into the PC-console.

5.2 Fixed-point controller implementation

In the A/D conversion, as it explained previously, the corresponding between the analog sensed signal v_{sense} (introduced by multiplication of v_s into the current sensing H_s), and the A/D converted digital signal $\tilde{v}_{sense}$ is illustrated in Fig. 5.2. As seen, for inductor current regulated (1 A) that is corresponded with ($\tilde{v}_{sense} = 0.25$ V), is necessary importing in the PC-console an LSB value equal to 512. Now for defining the digitized error signal $\tilde{V}_{err}$,

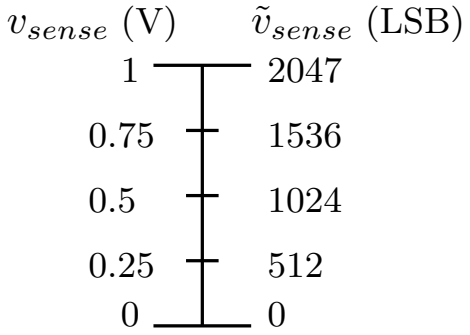


Figure 5.2: *Representation of the A/D range*

it is calculated by subtracting the A/D converted output from the digital set point:

$$[\tilde{v}_{err}]_0^{12} \Leftarrow [\tilde{V}_{ref}]_0^{12} - [\tilde{v}_{sense}]_0^{12}. \tag{5.1}$$

it is neccesary to be noted, the digital set point expressed as a same bit of A/D converter (11 bit).

The fixed-point implementation for the compensator obtained from Fig. 3.12, is illustrated in Fig. 5.3. As shown, the main compensator coefficients are quantized. In the following is described, quantization of the coefficients and $\tilde{u}_{PID}$.

The first is necessary an scaled coefficient, that is given by multiplication between the compensator scaling factor (λ) and the compensator gains (K_p, K_i, K_d). The scaling factor is equal to the A/D converter quantization $q_{V_o}^{(A/D)}$. As is mentioned previously, corresponding to (3.10), the A/D converter quantization step over a full scale voltage (1 V) is equal to 4.88 μV.

For the quantization of $\tilde{u}_{PID}$, consider first the proportional term $\tilde{u}_p$. This term can be obtained from a multiplication between the error signal and proportional coefficient:

$$[\tilde{u}_p]_{-9}^{22} \leftarrow [\tilde{K}_p]_{-9}^{10} \times [\tilde{v}_{err}]_0^{12}. \tag{5.2}$$

Also the derivative term $\tilde{u}_d$ can be determined similarly:

$$[\tilde{u}_d]_{-6}^{22} \leftarrow [\tilde{K}_d]_{-6}^{10} \times [delta\, \tilde{v}_{err}]_0^{12}. \tag{5.3}$$

Which $delta\,\tilde{v}_{err}[k]$ is the differential between the previous error:

$$delta\,\tilde{v}_{err}[k] = \tilde{v}_{err}[k] - \tilde{v}_{err}[k-1]. \tag{5.4}$$

On the other hand, the integral term $\tilde{u}_i$ can be determined by adding the two terms. One obtains a multiplication between the error signal and integral coefficient as above, and the other obtains the integral saturation term $\tilde{u}_{i,sat}$. Finally, the compensator control signal $\tilde{u}_{PID}$ is determined by

$$\tilde{u}_{PID} = \tilde{u}_p + \tilde{u}_{i,sat} + \tilde{u}_d. \tag{5.5}$$

As the integral term is a biased signal and needs the largest hardware dynamic range between the three control terms, it is necessary the alignment of both proportional and derivative term to the integral term. The last step is the saturation of $\tilde{u}_{PID}$ to have the compensator output matching the DPWM resolution. The block diagram of the fixed-point implementation of the PID compensator is illustrated in Fig. 5.4.
The proposed regulator was experimentally tested, a VHDL code was written for the corresponding regulator allowed in FPGA. for importing the HDL values by PC-console, obviously for the PI compensator $K_{d,HDL} = 0$, and the proportional and integral gains can be quantized by 10 bit over a scale of 2^{-9}, 2^{-13} respectively. Where the scaled coefficient is determined by

$$\begin{aligned} \check{K}_p &= \lambda \cdot K_p = (488 \times 10^{-6})(36.12) = 176 \times 10^{-4}, \\ \check{K}_i &= \lambda \cdot K_i = (488 \times 10^{-6})(16.49) = 8.04 \times 10^{-3}. \end{aligned} \tag{5.6}$$

So, their HDL values are equal to

$$\begin{aligned} \tilde{K}_p &= 0000001001 \times 2^{-9} = 0.0175_{10} \rightarrow \tilde{K}_{p,HDL} = 66, \\ \tilde{K}_i &= 00001000010 \times 2^{-13} = 0.008_{10} \rightarrow \tilde{K}_{i,HDL} = 9. \end{aligned} \tag{5.7}$$

In the integral compensator is existed just the integral term ($K_{p,HDL} = 0$, $K_{d,HDL} = 0$) and its HDL value is given by

$$\check{K}_i = \lambda \cdot K_i = (488 \times 10^{-6})(0.041) = 2.04 \times 10^{-5} \rightarrow \tilde{K}_{i,HDL} = \frac{\check{K}_i}{2^{-13}} \cong 1. \tag{5.8}$$

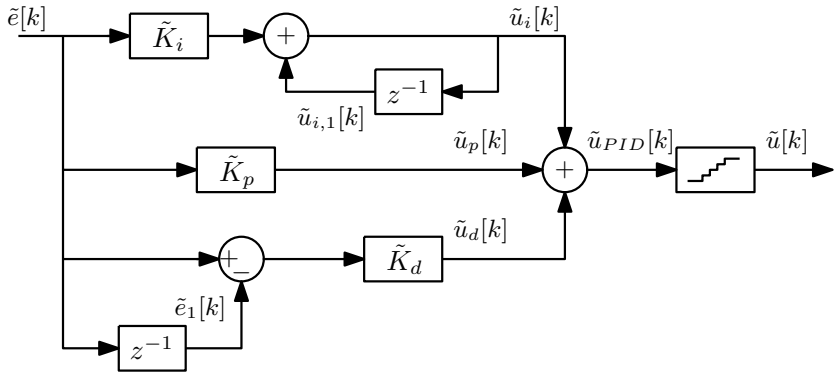


Figure 5.3: *Compensator realization with coefficient scaling and quantization*

5.3 Experimental results

In this section the results of the experimental analysis will be presented, that is consist of two parts. The output signals seen by oscilloscope, and the regulator signals by the signal tap digital logic analyzer of the FPGA console.

5.3.1 Open-loop characterization

For this measurement, is connected the electronic load to the converter output and it is set to constant resistance mode with maximum $R = 28\ \Omega$. By programming the FPGA using the quartus prime, can be set the control command U to achieve the output voltage $V_o = 12$ V. As the duty cycle is constant $D = 0.58$, with the carrier amplitude $N_r = 200$, the control command is

$$D = \frac{U}{N_r} \rightarrow U = 116. \tag{5.9}$$

By importing this value into the PC-console, can be seen the output signals by the oscilloscope as illustrated in Fig. 5.5. As seen, the converter reached 12 V (yellow line), and in this value is existed an average input current equal to 1 A (green line).

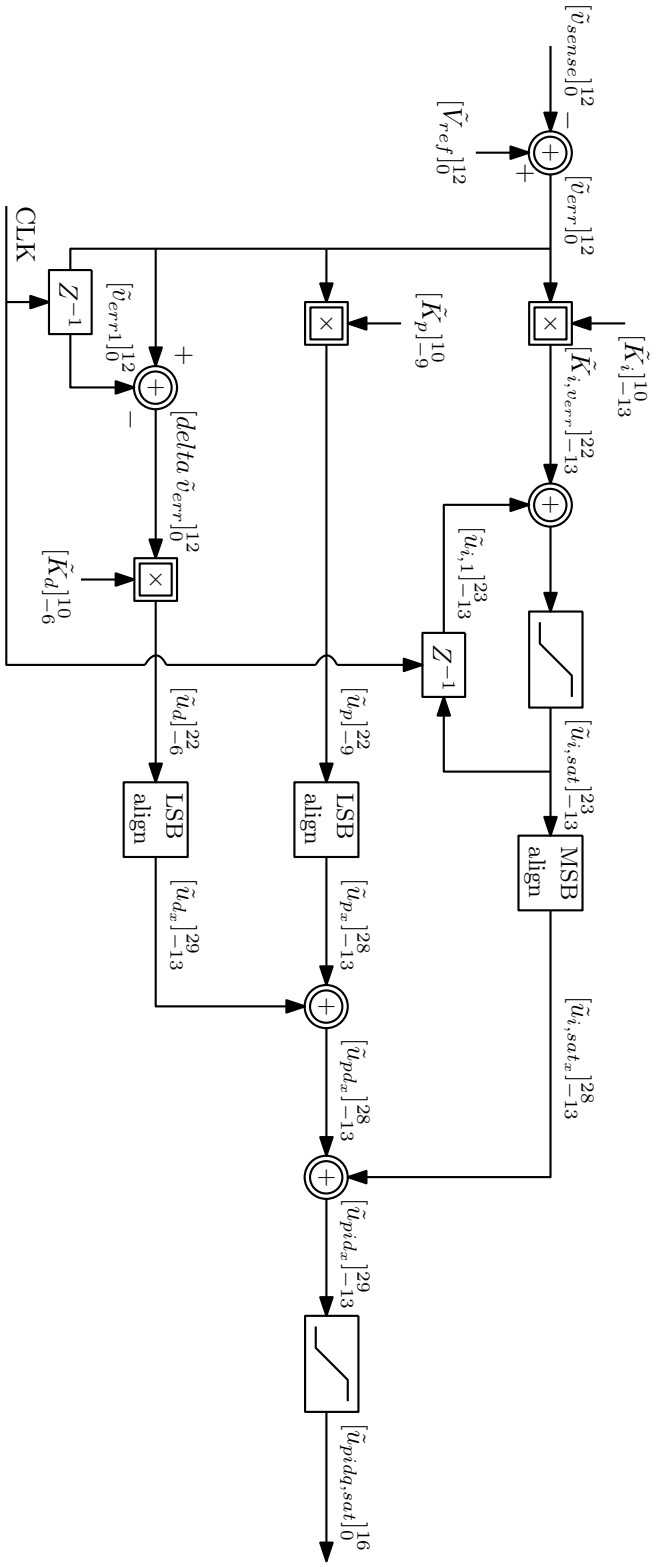


Figure 5.4: *Fixed-point implementation of the PID compensator*

5.3.2 Closed-loop characterization

For this measurement, is connected a passive resistance to the converter output $R = 22\ \Omega$. In this characterization need to set the sensing value for regulating the required inductor current. Let's start first with characterization of the sensing channel.

5.3.2.1 sensing characterization

By programming the FPGA, as it mentioned can be set the sensing value of 512 LSB to achieve the inductor average current 1 A. In case of integral compensator, also is imported the integral gain value $\tilde{K}_{i,HDL} = 1$ with $\tilde{K}_{p,HDL} = 0$ and $\tilde{K}_{d,HDL} = 0$. After setting these values it can be seen there are some difference between experimental and theoretical results. Like so is regulated the average value 0.81 A of the inductor current by using 512 LSB. It should be noted that, every 1 LSB, can be changed 1.95 mA according to

$$\frac{I_{FS}}{2048} = \frac{4\,A}{2048} = 1.95\ mA. \tag{5.10}$$

So 140 mA is needed to reach 1 A that is proportional to increasing 70 LSB:

$$\frac{140\,mA}{1.95\,mA} = 70\ LSB. \tag{5.11}$$

Therefore 610 LSB must be used to achieve 1 A averaged regulated. So this difference can be due to the offset. To acquire the offset value is needed to measure average value of the inductor current at the set point value imported which is done every 64 bits. The form of this measurement is reported in Fig. 5.6. The measured sensed values are shown as red dots which compared to the linear diagram of theoretical contents that shown in blue. Therefore it can be seen in the line regression which shown in red with equation of

$$\bar{I}_L = 0.0017 I_{ref} - 0.059. \tag{5.12}$$

It is necessary to mention, at above equation I_{ref} is described in LSB, also the line equation in ampere. So the slope of this line is 0.0017 which is described

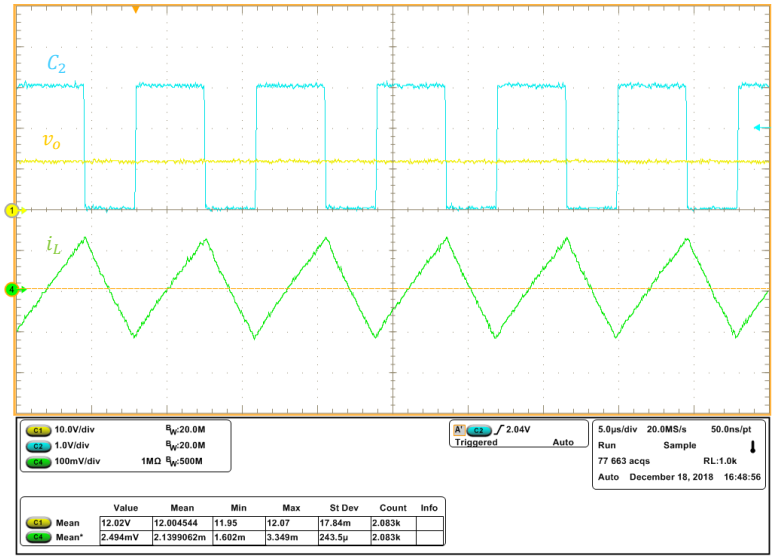


Figure 5.5: *The oscilloscope display of the open loop Boost converter outputs, (C_2:gate pulse, v_o:output voltage, i_L:inductor current)*

in $\frac{A}{LSB}$ and also exist an offset value equal to 0.059 A. In the absence of the offset, the measured dots must be started from zero like the line of the theoretical values. As seen initial measured dots value is not starting from zero. As stated before, the sensing value is equal to

$$\begin{aligned} v_{sense} &= \frac{I_{ref}}{2048} = 0.25\bar{I}_L, \\ \bar{I}_L &= \frac{I_{ref}}{0.25 \times 2048} = 0.0019 I_{ref}. \end{aligned} \tag{5.13}$$

Therefore, is almost compatible with its slope. On the other hand, by multiplication of the slope value 0.0017 into the full scale value 2048 can be obtained the inductor average current equal to 3.48 A. So it is different from the theoretical amount 4 A, because of existence the offset.

On the other hand, was seen in the output display by oscilloscope, the signals move and have not constant values. As shown in Fig. 5.7 about the inductor current waveform, the track not stopped and exist a wide of the variation. It is because of a limit cycle which is happened with 12 bits quantization in the A/D converter. Therefore it must reach a permanent regime in which the output voltage fluctuates a little to an intermediate value at 1 A. So can be

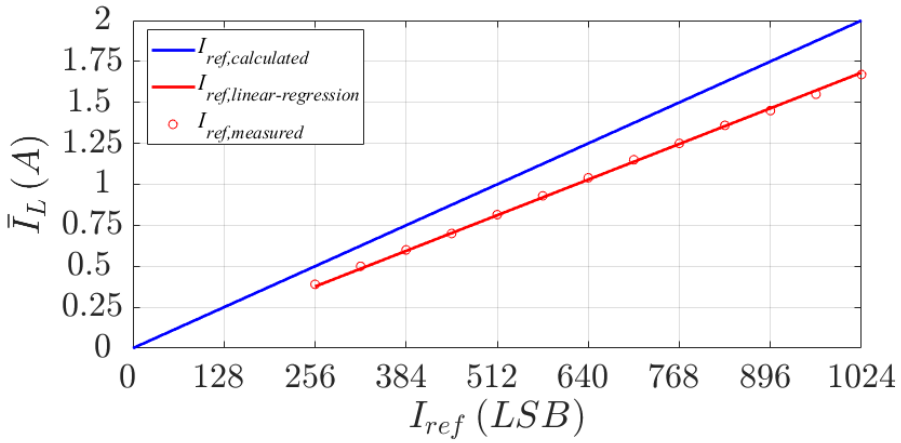


Figure 5.6: *The Comparison between measured(red dots) and calculated(blue line) sensed signal*

reduced the resolution of the A/D converter by rounding the digitized signal. In the VHDL code, it can be done by removing the first least significant bits n_{reduce}, that is implemented by masking them from the A/D output. It can be seen experimentally that is necessary to remove 6 bits to reach stability. Also in theoretical calculation can be defined the number of bits that needed to be removed. As q_{AD} must be greater than q_{DPWM}, number of reduced bits described by

$$\begin{aligned} q^{(AD)} > q^{(DPWM)} \implies \frac{1}{2^{n,reduce}} > \frac{2I_L \cdot q_D}{1-D} \\ 2^{n,reduce} > 43.5 \implies n_{reduce} \geqslant 6. \end{aligned} \tag{5.14}$$

Where

$$q^{(DPWM)} = \frac{\partial I_L}{\partial D} \cdot q_D = \frac{2V_g}{R_o} \cdot \frac{q_D}{(1-D)^3} = \frac{2I_L}{1-D} \cdot q_D, \tag{5.15}$$

with $q_D = \frac{1}{N_r}$. Now with removing 6 bits, the set point value must be rounded by a coefficient of $2^6 = 64$ bits. Then by $\frac{610}{64}$ can be produced the value required as 576 LSB or 640 LSB. Therefore can be reached a stable system with the average inductor current 1 A regulated, as shown in Fig. 5.8.

As it mentioned by removing bit, certain limit cycle point disappeared.

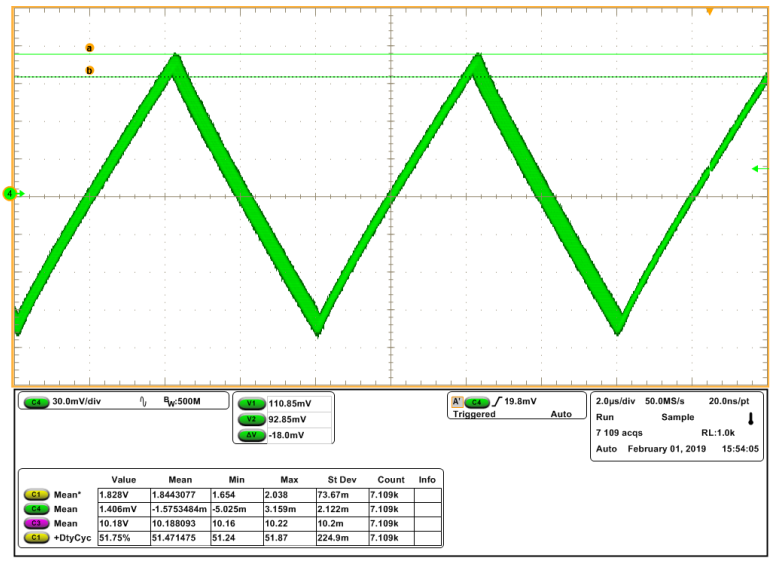


Figure 5.7: *The oscilloscope display of the inductor current persistence, at* $I_L = 1\ A (I_{ref} = 610\ LSB)$

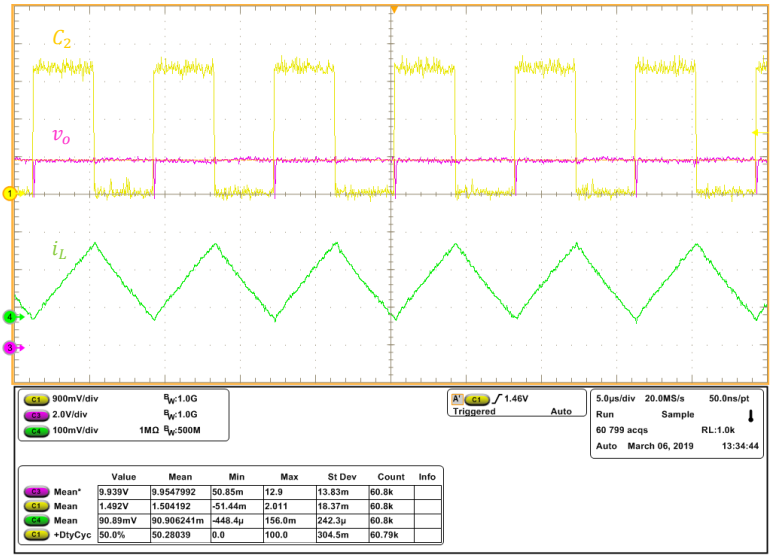


Figure 5.8: *The oscilloscope display of the Boost converter outputs, used Integral compensator with removing 6 bits at* $I_L = 1\ A (I_{ref} = 576\ LSB)$, *($C_2$:gate pulse, v_o:output voltage, i_L:inductor current)*

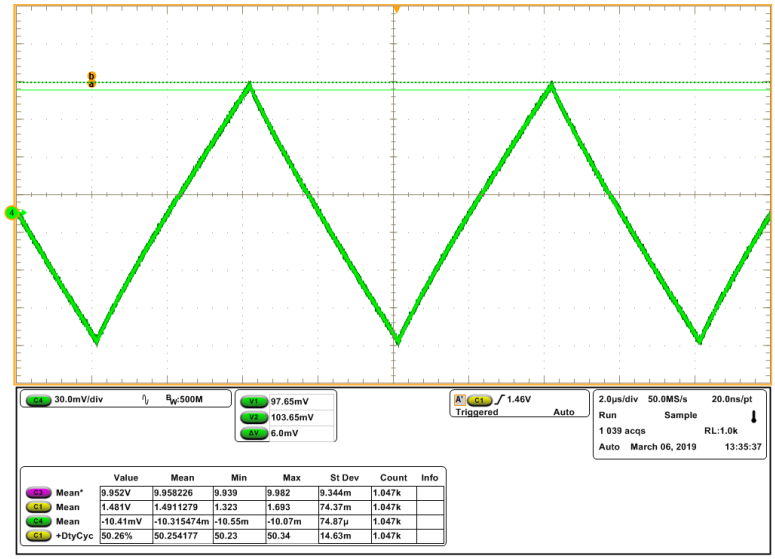
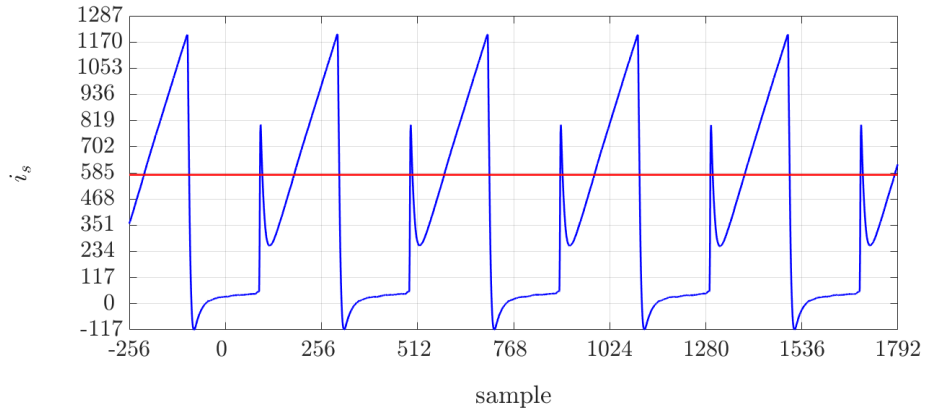


Figure 5.9: *The oscilloscope display of the inductor current persistence, with removing 6 bits at* $I_L = 1\ A (I_{ref} = 576\ LSB)$

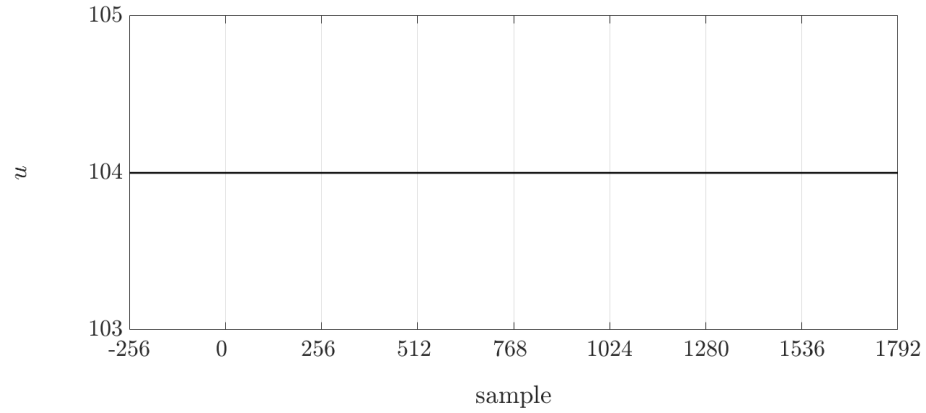
As seen in Fig. 5.9, the track stops moving and wide of the variation in the inductor current signal is a negligible value (6 mA), it means that the waveform remains constant forever. Also can be seen the sensing and A/D signal acquisition. The Fig. 5.10 shows the graphic of its digital signals. As seen, the limit cycle is eliminated and switch current is sampled at the midpoint of the on state switching by a constant sensed signal as 576 LSB. It should be noted, the switching current has a small transient at the beginning of each period. Also there are 2048 samples with 8 μs period interval. As it mentioned previously, A/D is sampled at 50 MHz and the sensing signal is sampled at the switching frequency 125 KHz. Then the output signal of the integral compensator is an constant signal.

5.3.2.2 PI compensator characterization

In the case of PI compensator, are imported the gain values as $\tilde{K}_{p,HDL} = 66$, $\tilde{K}_{i,HDL} = 9$, $\tilde{K}_{d,HDL} = 0$. As is seen in the sensing characterization, based on chart of Fig. 5.6, must put 610 LSB to regulate 1 A for the inductor



(a)



(b)

Figure 5.10: *The graphic of the A/D acquisition by integral compensator: (a) switch current(blue) and sensing signal(red line), (b) the integral compensator output*

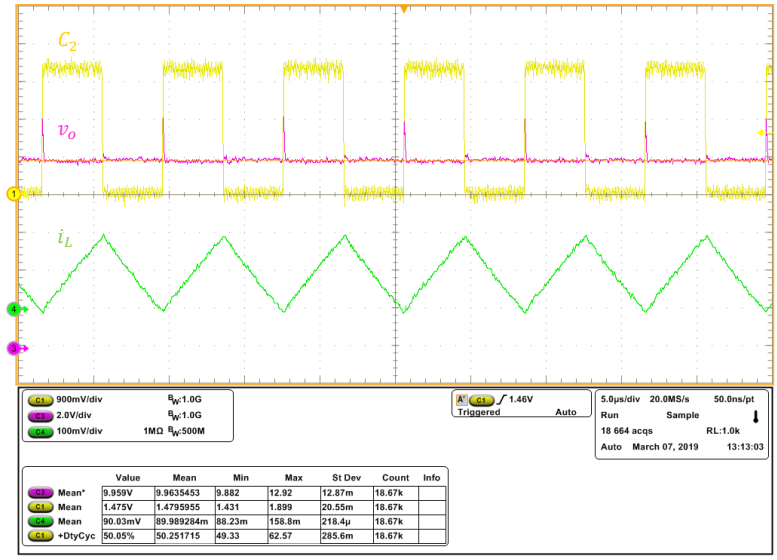


Figure 5.11: *The oscilloscope display of the Boost converter outputs, used PI compensator with removing 6 bits at* $I_L = 1$ *(*$I_{ref} = 576$ *LSB), (*C_2*:gate pulse,* v_o*:output voltage,* i_L*:inductor current).*

averaged current. Also to eliminate the limit cycle must remove 6 bits. The output display is shown in Fig. 5.11 and Fig. 5.12, which the waveforms remain stable. The Fig. 5.13 shows the graphic of its digital signals. As seen, the limit cycle is eliminated by constant sensed signal at 576 LSB and the output signal of the PI compensator determined by $u_p + u_i$ which has a constant value.

To verify the sensing gain $H_s = 25$, is needed to measured the sensing value v_{sense} and the average inductor current I_L as follows. As seen in Fig. 5.11, the average inductor current is 0.9 A, in the Fig. 5.12 it is equal to 1.02A and the difference between them is $\Delta I_L = 120$ mA. ΔI_L is corresponding to the 64 bits difference between the two implementation value as 576 LSB and 640 LSB that is defined by

$$\frac{64}{2048} \cdot 4\,A = 125\ mA. \tag{5.16}$$

The sensing value measured on the power board at the 576 LSB is 141.8 mV, and at the 640 LSB is 171.2 mV. The difference between them is equal to

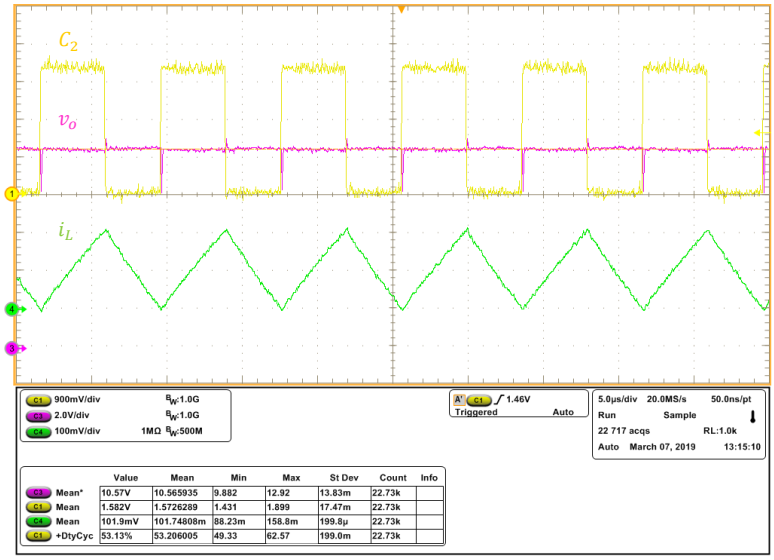
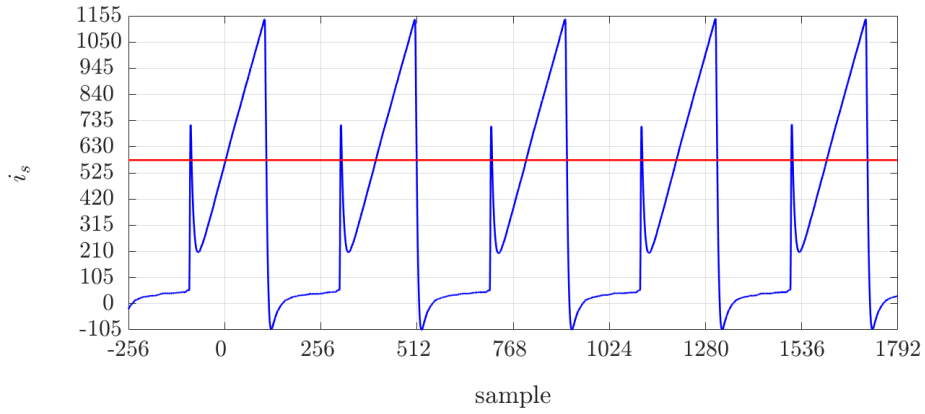


Figure 5.12: *The oscilloscope display of the Boost converter outputs, used PI compensator with removing 6 bits at* $I_L = 1$ *(*$I_{ref} = 640$ *LSB), (*C_2*:gate pulse,* v_o*:output voltage,* i_L*:inductor current).*

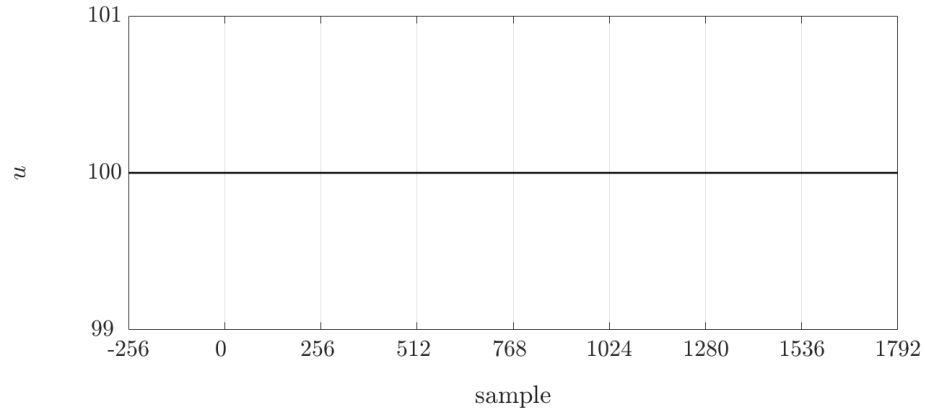
29.4 mV. Therefore

$$\begin{aligned} \frac{\Delta v_{sense}}{\Delta I_L} &= 0.24 \\ \Longrightarrow H_s = \frac{0.24}{R_{sense}} &= 24. \end{aligned} \tag{5.17}$$

To regulate the average current 1.5 A is required 768 LSB as the set point value. But because of the offset as shown in the diagram of Fig. 5.6, must be imported 900 LSB. As seen before, with 768 LSB can be regulated 1.24 A. So according to (5.11), is needed to increasing 132 LSB to reach 1.5 A.



(a)



(b)

Figure 5.13: *The graphic of the A/D acquisition by PI compensator with removing 6 bits at* $I_{ref} = 576$ *LSB: (a) switch current(blue) and sensing signal(red line), (b) the PI compensator output*

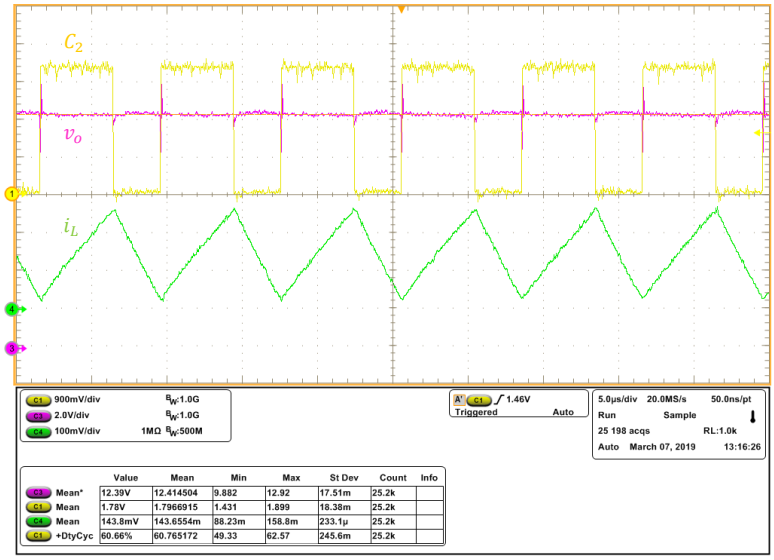


Figure 5.14: *The oscilloscope display of the Boost converter outputs, used PI compensator with removing 6 bits at* $I_L = 1.5\ A (I_{ref} = 896\ LSB)$, *($C_2$:gate pulse, v_o:output voltage, i_L:inductor current)*

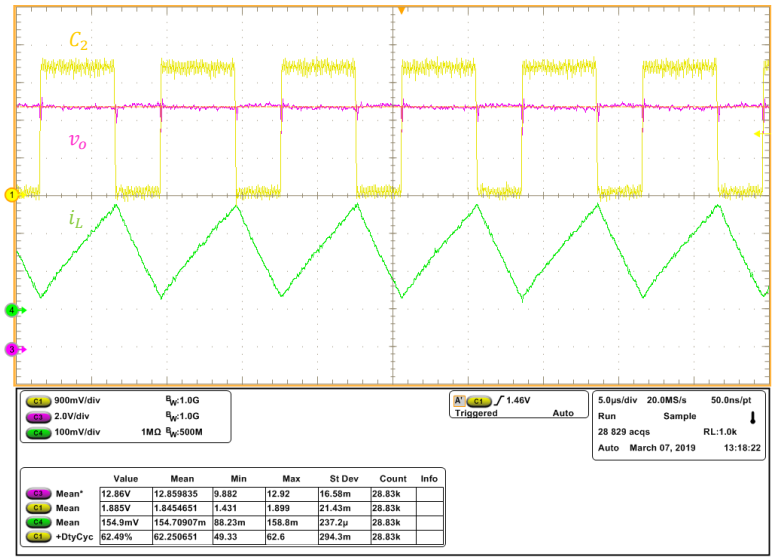
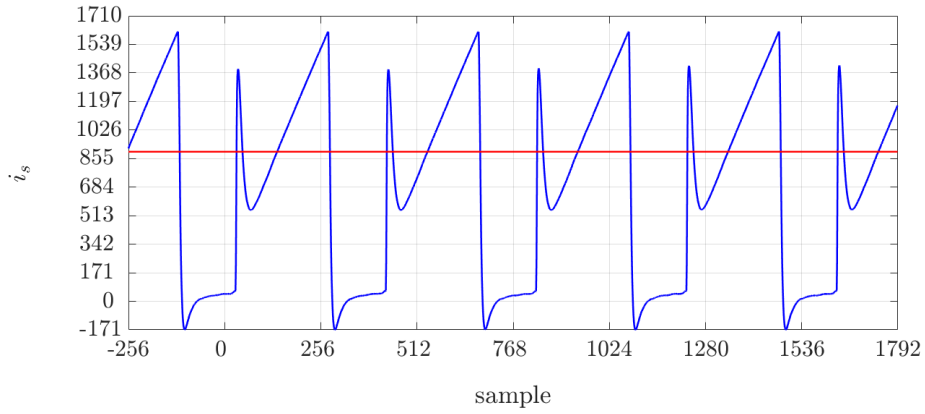
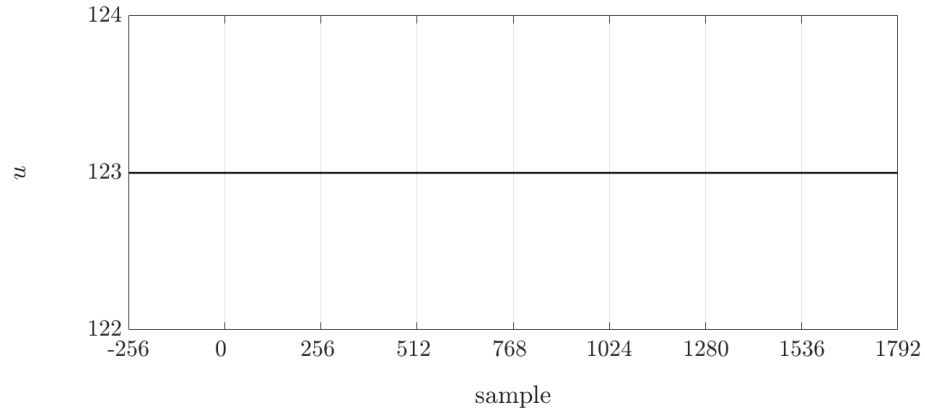


Figure 5.15: *The oscilloscope display of the Boost converter outputs, used PI compensator with removing 6 bits at* $I_L = 1.5\ A (I_{ref} = 960\ LSB)$, *($C_2$:gate pulse, v_o:output voltage, i_L:inductor current)*



(a)



(b)

Figure 5.16: *The graphic of the A/D acquisition by PI compensator with removing 6 bits at* $I_{ref} = 896$ *LSB: (a) switch current(blue) and sensing signal(red line), (b) the PI compensator output*

The oscilloscope display with eliminated limit cycle at 896 LSB and 960 LSB are shown in Fig. 5.14 and Fig. 5.15. As seen, the average inductor current at the 896 LSB and 960 LSB is equal to 1.43 A, 1.55 A respectively. Also the sensing value measured on the power board are 278.7 mV (at 896 LSB) and 308.4 mV (at 960 LSB). Therefore the sensing gain can be verified by

$$\begin{aligned} \frac{\Delta v_{sense}}{\Delta I_L} &= \frac{29.7\,mV}{120\,mA} = 0.24 \\ \Longrightarrow H_s &= \frac{0.24}{R_{sense}} = 24. \end{aligned} \tag{5.18}$$

Also, the eliminated limit cycle in the scale of regulated 1.5 A is illustrated by digital signals graphic in Fig. 5.16.

To regulate the average current 2 A is needed to importing 1024 LSB as the set point value. Also here must be importing 1160 LSB due to the offset. To achieve a constant waveform without limit cycle is required 1152 LSB or 1216 LSB by removing 6 bits. The oscilloscope display is illustrated in Fig. 5.17. The eliminated limit cycle can be seen by graphic of the digital signals in Fig. 5.18. As is described the transient discussion previously, for transition in the set point value, the first is necessary to enable a periodic step variation by acting on the switch intended in the FPGA board. Then can be imported the desired value of the transition by the reference step in PC-console. Also the step reference is an 11 bit signed word. In transition from 1 A to 1.5 A, the set point value must be transferred from 576 LSB to 896 LSB. Therefore the step reference imported is 320 LSB. The output display of this transition is shown in Fig. 5.19. As seen, the inductor averaged current has a transient of 0.5 A increasing every switching period. Also for the output voltage this increase is done. The digital sensing acquisition which sampled in 1024, change with a difference equal to the step value. Its graphic is illustrated in Fig. 5.21.

As a same condition, in transition from 1 A to 2 A, the set point has a transition from 576 LSB to 1152 LSB. So the required reference value is 576 LSB that its display is illustrated in Fig. 5.20. Also the inductor averaged current

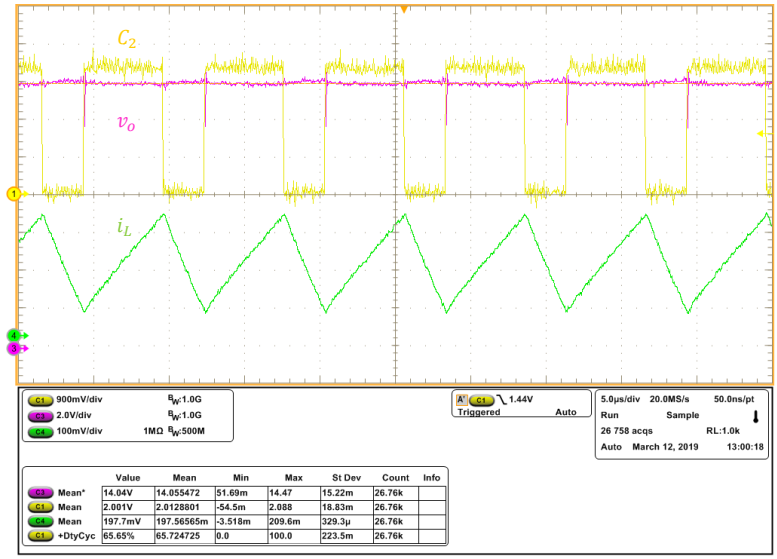
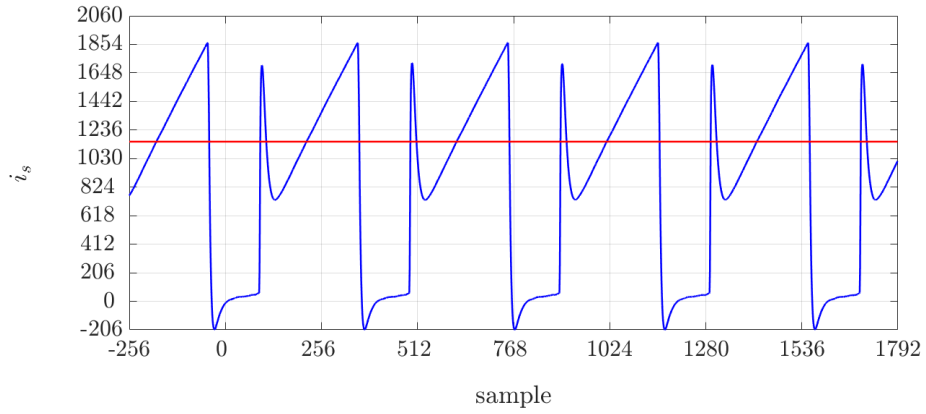
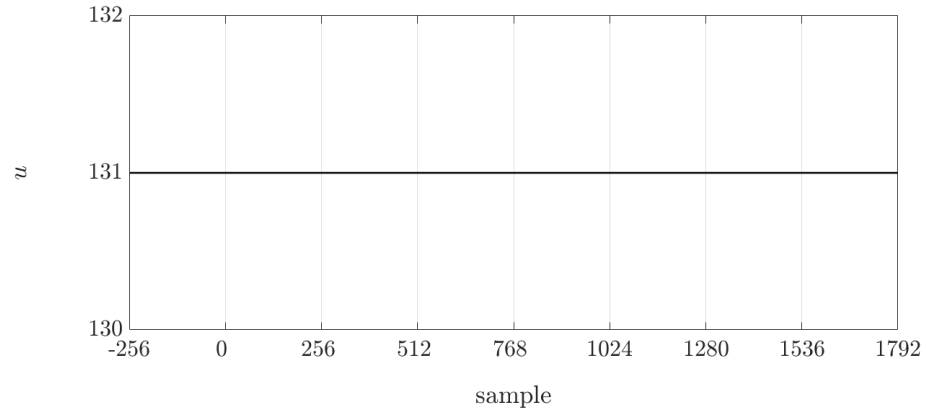


Figure 5.17: *The oscilloscope display of the Boost converter outputs, used PI compensator with removing 6 bits at* $I_L = 2\ A (I_{ref} = 1152\ LSB)$, *(*$C_2$*:gate pulse,* v_o*:output voltage,* i_L*:inductor current)*

has a transient of 1 A increasing every switching period. The Fig. 5.22 illustrates the graphic of digital sensing acquisition which changed in step value equal to 576 LSB, also the PI compensator output is changed identically.

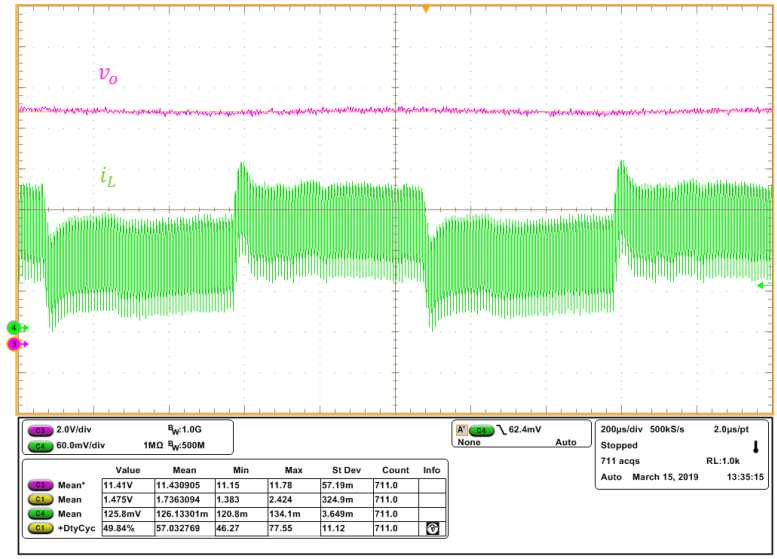


(a)

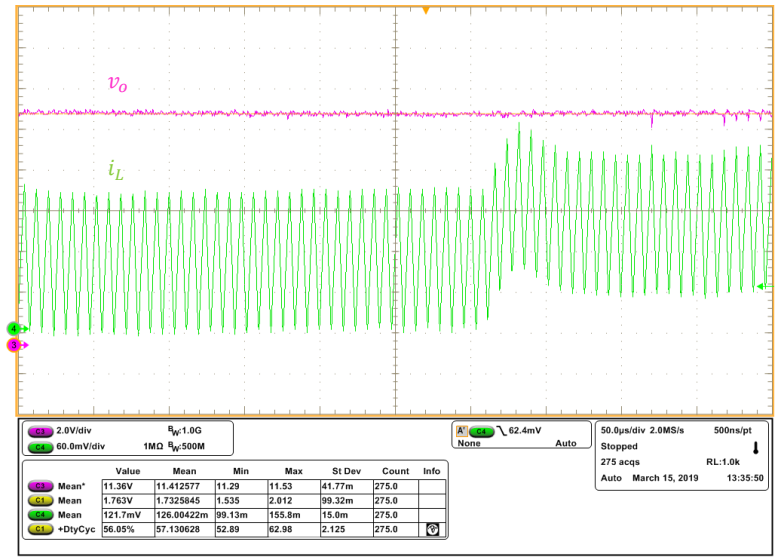


(b)

Figure 5.18: *The graphic of the A/D acquisition by PI compensator with removing 6 bits at I_{ref} = 1152 LSB: (a) switch current(blue) and sensing signal(red line), (b) the PI compensator output*

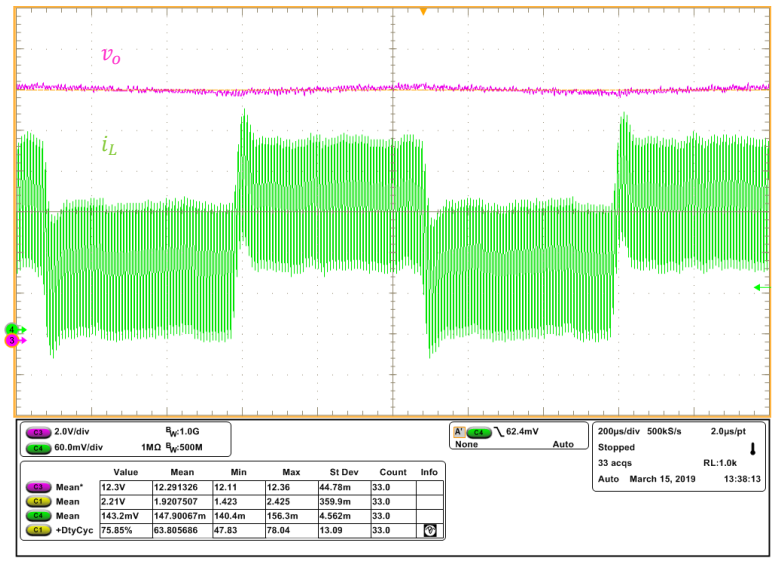


(a)

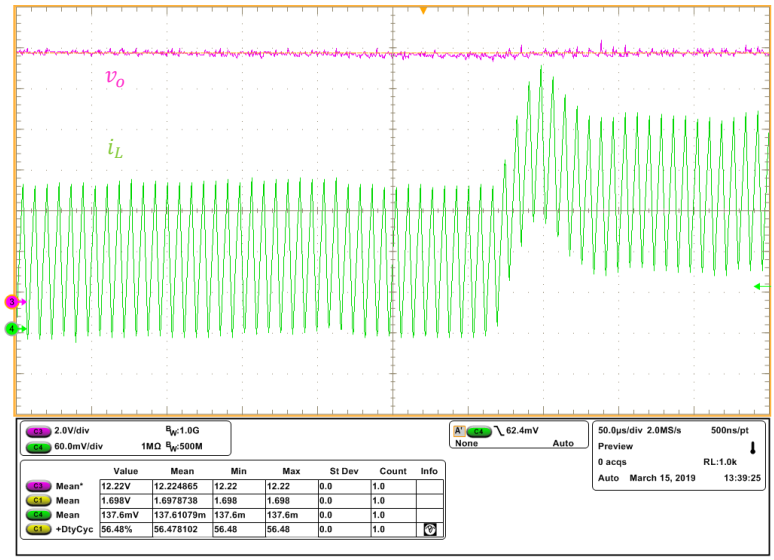


(b)

Figure 5.19: *The oscilloscope display of the Boost converter outputs, used PI compensator in 0.5 A transition: (a) 200 $\mu s/div$, (b) 50 $\mu s/div$, (v_o:output voltage, i_L:inductor current)*

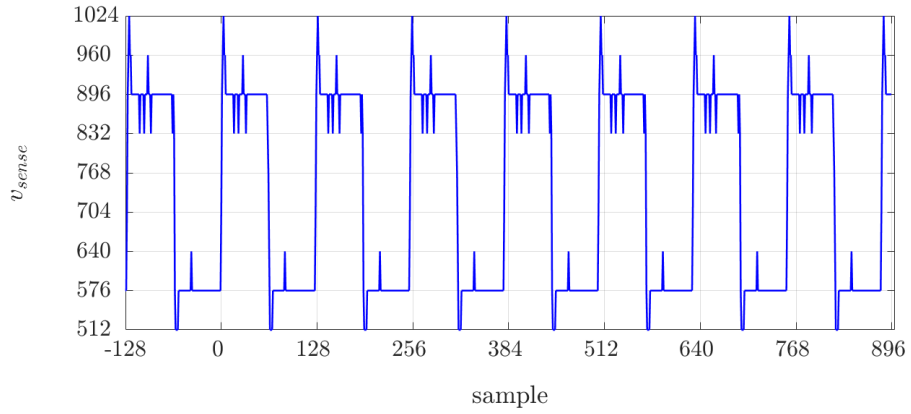


(a)

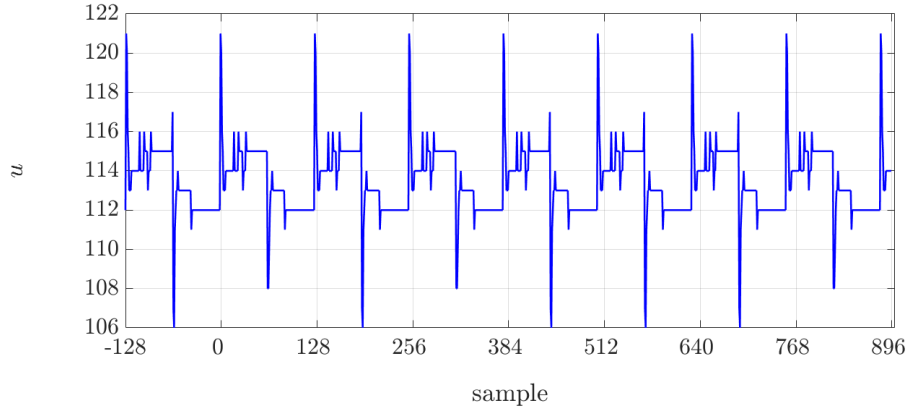


(b)

Figure 5.20: *The oscilloscope display of the Boost converter outputs, used PI compensator in 1 A transition: (a) multiple period, (b) one (a) 200 $\mu s/div$, (b) 50 $\mu s/div$, (v_o:output voltage, i_L:inductor current)*

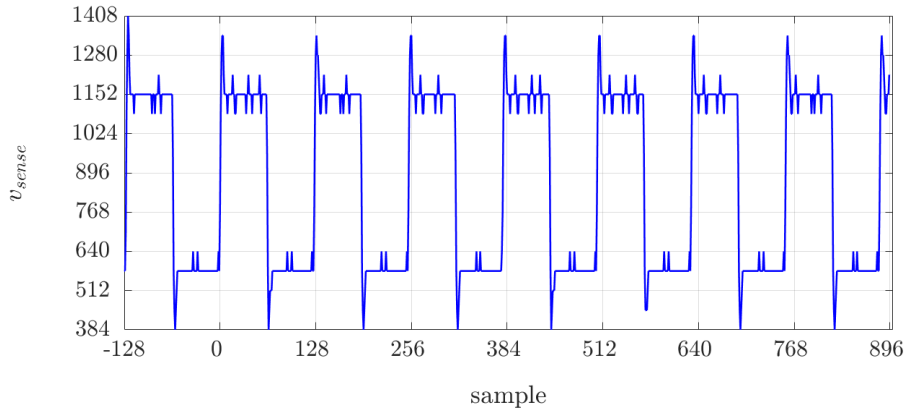


(a)

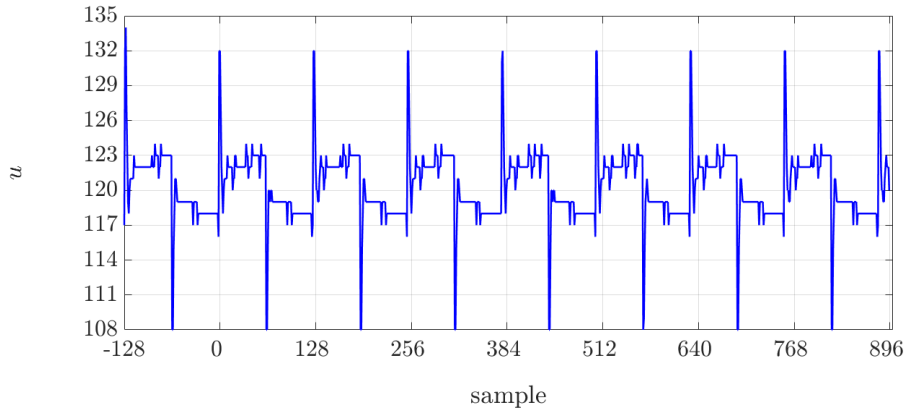


(b)

Figure 5.21: *The graphic of the sensing acquisition by PI compensator in 0.5 A transition(I_{ref} from 576 LSB to 896 LSB): (a) the sensing signal, (b) the PI compensator output*



(a)



(b)

Figure 5.22: *The graphic of the sensing acquisition by PI compensator in 1 A transition(I_{ref} from 576 LSB to 1152 LSB): (a) the sensing signal, (b) the PI compensator output*

Appendix A

Simulink block diagram

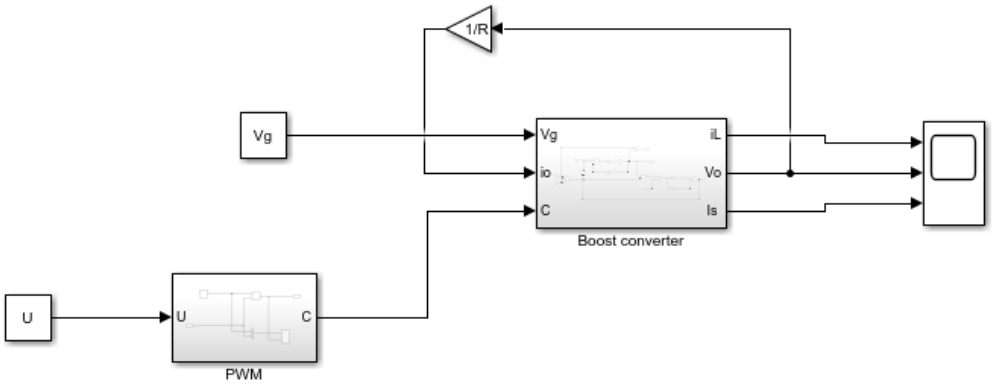


Figure A1: *Boost open loop operation*

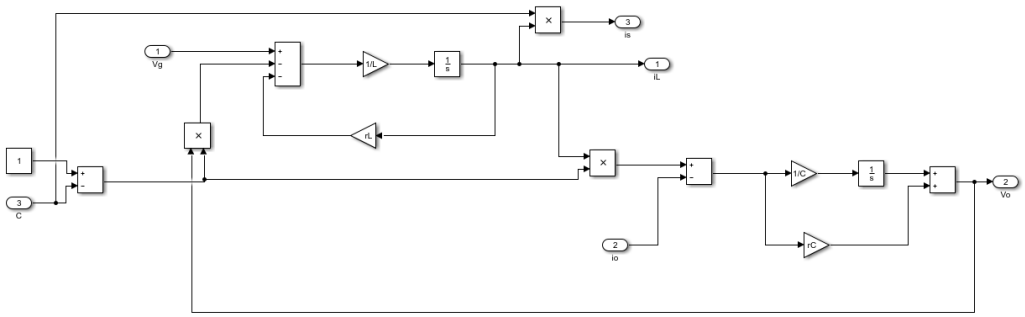


Figure A2: *Boost converter block diagram*

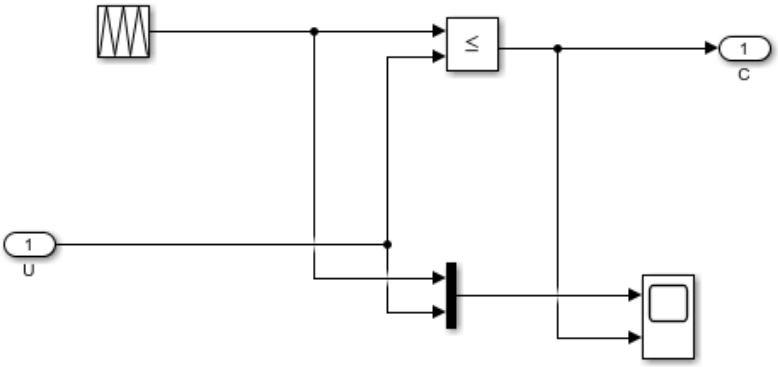


Figure A3: *PWM block diagram*

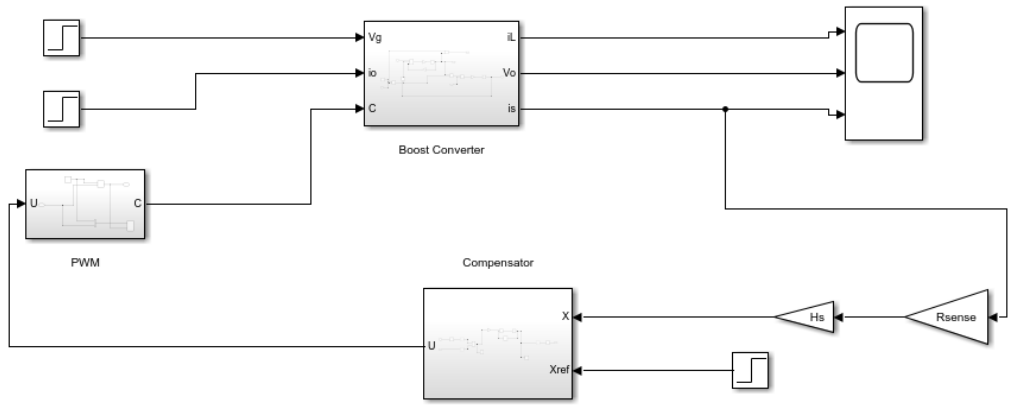


Figure A4: *Boost closed-loop operation*

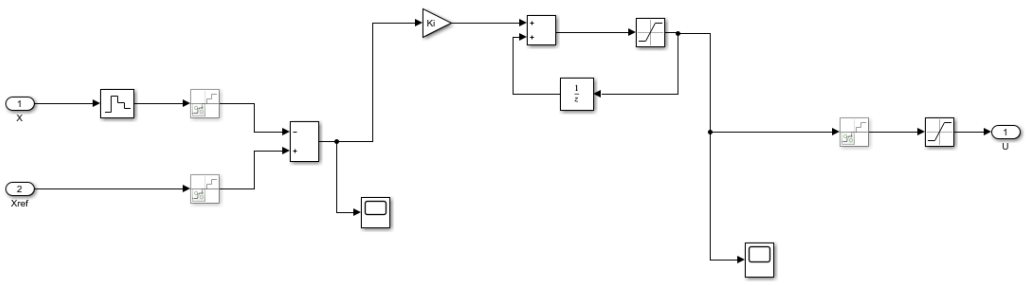


Figure A5: *Integral compensator block diagram*

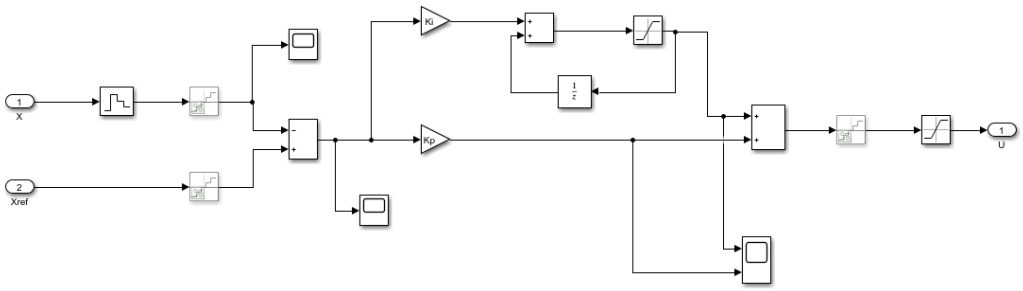


Figure A6: *PI compensator block diagram*

Appendix B

Matlab script

B.1

```
1  %   ******************************
2  %   Open-loop Boost converter
3  %   Initialization script
4  %   ******************************
5
6  close all;
7  clearvars;
8  clc;
9  %   Switching frequency and period
10 fs  =   125e3;
11 Ts  =   1/fs;
12 %   Input voltage
13 Vg  =   5;
14 %   Boost parameters
15 L   =   10e-6;     %   Inductance
16 rL  =   0.05;      %   Inductor parasitic resistance
17 C   =   311e-6;    %   Capacitance
18 rC  =   0;         %   Capacitor series resistance
19 %   Load resistance
```

```
20 R    =    28;
21 %    PWM
22 D    =    0.58;
23 Nr   =    200;        %    PWM carrier amplitude
24 U    =    D*Nr;       %    Modulating signal
25 M    =    1/(1-D);
26 %    Simulation time
27 Tsim     =  20e-3;
```

B.2

```
1  %    ******************************
2  %    Closed-loop Boost converter
3  %    Initialization script
4  %    ******************************
5  close all;
6  clearvars;
7  clc;
8  %    Switching frequency and period
9  fs   =    125e3;
10 Ts   =    1/fs;
11 %    Input voltage and output voltage setpoint
12 Vg     =    5;
13 Vo     =    12;
14 D      =    (Vo-Vg)/Vo;
15 Vref   =    0.25;
16 %    power rating
17 Po     =    5;
18 %    Output current at full load
19 Io     =    0.41;
20 %    boost parameters
```

```
21 L      =    10e-6;
22 rL     =    30e-3;
23 C      =    311e-6;
24 R      =    28.8;
25 %   PWM Resolution and Carrier amplitude
26 ndpwm  =   14;
27 Nr     =   200;
28 %   current sensing gain
29 Rsense =   10e-3;
30 % PWM small-signal delays
31 tpwm   =    Ts/2;
32 sampling_vect   =   [0   Ts];
33 %   A/D and DPWM Quantization
34 qAD    =    1/2^11;
35 qu     =    Nr/2^ndpwm;
36 %   Sensing gain
37 Hs     =     25;
38 %   Equivalent quantization on vout
39 qPWMo   =    (qu/Nr)*(Vg/(1-D)^2);
40 qADo    =    qAD/(Rsense*Hs);
41 %   Simulation time
42 Tsim    =    20e-3;
43 %   ************************************************
44 %   I Compensator design with the discretization-based
45 %   approach
46 %   ************************************************
47 %   s-domain modeling of the control-to-output
48 %   transfer function
49 s        =   tf('s');
50 delta    =   1+(s*(rL+Rsense)*R*C+s*L)/((1-D)^2*R+rL+
51 Rsense)+(s^2*L*C)/((1-D)^2+(rL+Rsense)/R);
```

```
52 Gids     =   [2*Vo*(1+s*R*C/2)]/[(rL+Rsense+(1-D)^2*R)*
53 delta];
54 Gids.inputdelay   =   tpwm;
55 %   s-domain uncompensated loop gain
56 Tus      =    (1/Nr)*Gids*Rsense*Hs;
57 %   z-domain uncompensated loop gain
58 %   (impulse response discretization)
59 Tuz      =    c2d(Tus,Ts,'imp');
60 %   Angular crossover frequency and phase margin
61 wc       =    2*pi*5;
62 phim     =    (pi/180)*45;
63 %   Magnitude and phase of Tuz at wc
64 [m,p]    =    bode(Tuz,wc);
65 %   Uncompensated phase margin
66 phim_u   =    pi+(pi/180)*p;
67 %   Prewarping on wc
68 wcpw     =    (2/Ts)*tan(wc*Ts/2);
69 %   Discrete-time I - additive form ('bilinear' type)
70 Ki       =    (Ts*wcpw)/(m*sqrt(1+(wcpw*Ts/2)^2))
71 %   z-domain PI transfer function
72 z        =    tf('z',Ts);
73 Dz       =    Ki/(1-z^-1);
74 %   z-domain compensated loop gain
75 Tz       =    Dz*Tuz;
```

B.3

```
%   ************************************************
%   PI Compensator design with the discretization-
%   based approach
%   ************************************************
%   s-domain modeling of the control-to-output
%   transfer function
s       =   tf('s');
delta   =1+(s*(rL+Rsense)*R*C+s*L)/((1-D)^2*R+rL+
Rsense)+(s^2*L*C)/((1-D)^2+(rL+Rsense)/R);
Gids    = [2*Vo*(1+s*R*C/2)]/[(rL+Rsense+(1-D)^2*R)*
delta];
Gids.inputdelay  =  tpwm;
%   s-domain uncompensated loop gain
Tus     = (1/Nr)*Gids*Rsense*Hs;
%   z-domain uncompensated loop gain
%   (impulse response discretization)
Tuz     =  c2d(Tus,Ts,'imp');
%   Angular crossover frequency and phase margin
wc      =   2*pi*12.5e3;
phim    =  (pi/180)*45;
%   Definition of wp
wp      =   2/Ts;
%   Magnitude and phase of Tuz at wc
[m,p]   =   bode(Tuz,wc);
%   Uncompensated phase margin
phim_u  =   pi+(pi/180)*p;
%   Prewarping on wc
wcpw    =   (2/Ts)*tan(wc*Ts/2);
%   PI design
```

```
30 wPI     =    wcpw*tan(phim_u-phim);
31 GPIinf  =    1/m/sqrt(1+(wPI/wcpw)^2);
32 %   Discrete-time PI - additive form ('bilinear'type)
33 Kp      =    GPIinf*(1-wPI/wp)
34 Ki      =    GPIinf*2*wPI/wp
35 %   z-domain PI transfer function
36 z       =    tf('z',Ts);
37 Dz      =    Kp+Ki/(1-z^-1);
38 %   z-domain compensated loop gain
39 Tz      =    Dz*Tuz;
```

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