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Design, Simulation, and Commissioning of a 5-level CHB Inverter

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Sommario

Questo elaborato presenta uno studio su un inverter Cascaded H-bridge (CHB) a cinque livelli. L'inverter è composto da due moduli H-bridge in cascata; con questa configurazione è possibile ottenere cinque livelli di tensione in uscita utilizzando due sorgenti distinte in corrente continua come ingresso.
La prima parte di questo lavoro, esposta nel primo e nel secondo capitolo, tratta principalmente di basi teoriche riguardanti invertitori, strategie di controllo, sistemi di filtraggio e power quality.
Successivamente, sono stati sviluppati e simulati dei metodi di controllo di tensione e corrente, specifici per questa tipologia di inverter, come presentato nel terzo capitolo.
Nel quarto capitolo viene esposta la scelta dei componenti ed il dimensionamento che hanno portato alla realizzazione fisica di un modulo H-bridge, cella elementare che costituisce l'inverter CHB.
Nel quinto ed ultimo capitolo dell'elaborato sono illustrati i risultati ottenuti dai test in laboratorio, necessari per valutare il corretto funzionamento del prototipo. Lo scopo di questo lavoro era quello di creare un modello in scala ridotta di un inverter che in futuro sarà parte di un sistema elettrico atto ad azionare una singola fase di un motore a nove fasi a magneti permanenti (PMSM).
L'obiettivo finale è di poter azionare il motore con nove inverter CHB separati, garantendo un'indipedenza totale dell'alimentazione di ciascuna delle fasi. Per ambire a questo, è stato necessario dapprima investigare le varie tipologie ed architetture degli invertitori, partendo dalle più elementari fino ad arrivare alle tipologie multilivello, per poi concentrarsi sui Cascaded H-bridge. Successivamente sono state implementate delle strategie di controllo in catena aperta ed in catena chiusa, con l'obiettivo di controllare la tensione e la corrente d'uscita del dispositivo. Infine, un prototipo di un modulo H-Bridge è stato dimensionato, assemblato e testato, i risultati ottenuti sono stati discussi assieme ad alcuni possibili miglioramenti ed evoluzioni da attuare in futuro.
Questa tesi rappresenta un primo passo verso lo sviluppo di un inverter parte di un azionamento di un motore a nove fasi a magneti permanenti; i risultati ottenuti assieme alle conoscenze fornite, potranno essere d'aiuto per i futuri sviluppi ed avanzamenti nell'ambito di questo progetto.

Abstract

In this work a 5-level CHB inverter (5LCHBI) has been studied, simulated, and finally a prototype has been designed, realized, and tested. The device is composed by two H-bridge inverters connected in series; with this configuration is possible to obtain five different voltage levels as output using two different DC sources as input. The aim of this thesis was to create a small-scaled model of an inverter that will be part of a drive system for 9-phase permanent magnet synchronous motor (PMSM). To achieve this, the inverter topology and its architecture have been investigated, along with possible voltage and current control strategies. Subsequently open-loop techniques and novel closed-loop control strategies have been developed and simulated, aiming at the device's output current and voltage control. Eventually, a H-bridge module prototype has been designed, realized, assembled, and tested. This master thesis is a first step towards the development of the inverter stage for the 9-phase PMSM drive system. Notwithstanding, the results obtained, and the knowledge provided, will help achieving future advancements in this project.

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1 Introduction

The electrification of road and air vehicles is playing an important role in the environmental and energy sector all over the world. Due to the climate change, in the last decade countermeasures have been adopted by international communities in order to mitigate and reduce these issues. Thanks to the advancements obtained in batteries, controllers and semiconductor technologies, the performances in electric drives and systems are continuously improving. Also, thanks to these progresses, electric vehicles became very common on our roads, and they are still evolving. The ongoing research on these topics is not only focused to the electrification of the road system, but also to the other transportation segments, such as air and naval sectors. As shown in previous research papers [12], safety critical drive trains, such for aircrafts, require a high fault tolerance and reliability. In order to provide these requirements, optimal choices within the drives architecture and the electrical machines must be made. For safety-critical operation, the best choice for the electric machine is the 9-phase permanent magnet synchronous motor (PMSM). It is possible to drive the machine with different connection topologies, however the separated nine-phase system, focus of this project, is the most promising and innovative solution. This topology consists in nine 5-level cascaded H-bridge inverters (5LCHBI), each of one connected to one motor phase, as shown in figure 1.1. This solution provides galvanic insulation between different phases which are not electrically connected neither influenced by each other.

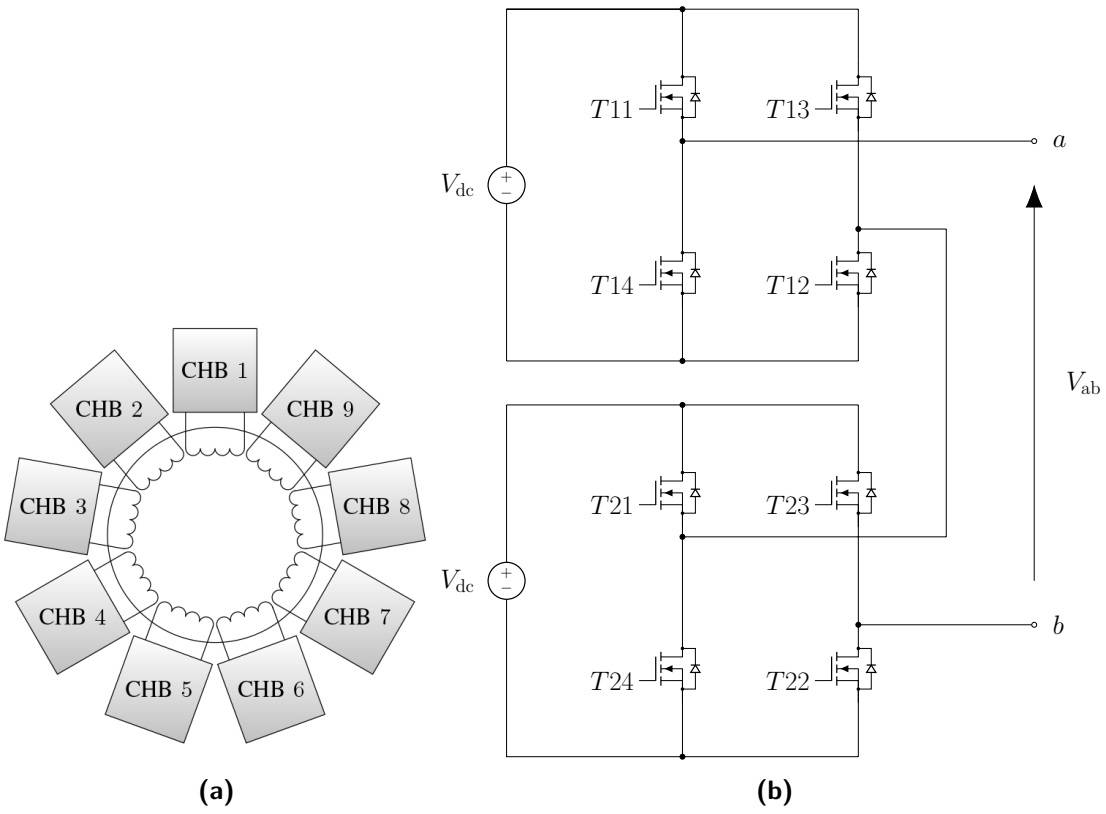


Figure 1.1 – 9-phase PMSM connection topology with nine galvanically separated phases [31] (a) and a 5-level CHB inverter (b).

The separated nine-phase system has more advantages compared to other connection topologies, as follows [12].

- The phases are electrically insulated, for reducing power electronic faults and for avoiding phase-phase shortcuts.
- The windings are thermally isolated, to avoid power degradation in case of phase failure.
- Positioning the inverters becomes easier thanks to the modular structure.
- The phases are physically separated, to increase the thermal isolation and to avoid error propagation to adjacent phases.
- Thanks to the modular structure of the CHB inverter, it is possible to increase the number of the H-modules and subsequently obtaining additional output voltage levels.
- In case of inverter fault, it is possible to bypass the faulty cell to guarantee the motor drive operations, despite a reduced number of voltage levels.

This thesis reports a full investigation on the 5-level CHB inverter, which it is the candidate for the inverter in the nine-phase PMSM system electric drive.

1.1 Motivation and Aim

The 5-level cascaded H-bridge, as it will more deeply explained in the following chapters, is composed by two H-bridge inverters connected in series. This inverter topology has the main advantage to give good quality output in terms of total harmonic distortion (THD), besides having a small number of components. Thanks to its cascaded structure it's also possible to bypass the eventual faulty cell(s) ensuring the fault tolerance.

The primary goal of this work is to create a 5LCHBI prototype, a small-scaled model of an inverter that in future will be part of a driving system for a 9-phase PMSM, which is already set down on a test bench in the university's laboratory. The specification of the scaled device is an output voltage $V_{\text{out}}= 30\,\text{V}$ and an output current $I_{\text{out}}= 20\,\text{A}$. To achieve this aim, the hardware stage must be realized, and proper inverter control techniques have to be implemented.

In order to create a prototype, it is necessary to start the analysis from the CHB inverter architecture topology and its sub-modules. After the prototype architecture selection, components such as switches, power supplies and sensors must be chosen. Subsequently it is necessary to design the printed circuit board (PCB), device that will affix and electrically connect the previous selected components. This can be the main challenge of this work, in fact, a bad designed PCB can cause unhealthy device functioning, making difficult the testing and debug procedures.

For interfacing the inverter to the electrical machine, proper control strategies must be implemented, aiming at a good output quality and fast and stable control response for the subsequent extension of these techniques to the 9-phase PMSM drive system. This process starts with the analysis and simulation of open-loop control strategies applied to the 5LCHBI, based on the sinusoidal pulse width modulation. Various open-loop strategies have been analyzed and simulated, subsequently two different closed-loop techniques have been developed: a voltage control technique, based on a dual PI loop, and a novel current control strategy, based on a multi-band hysteresis current control.

1.2 Methodology and Limitations

It is possible explain the methodology of this work using the incremental model as follows.

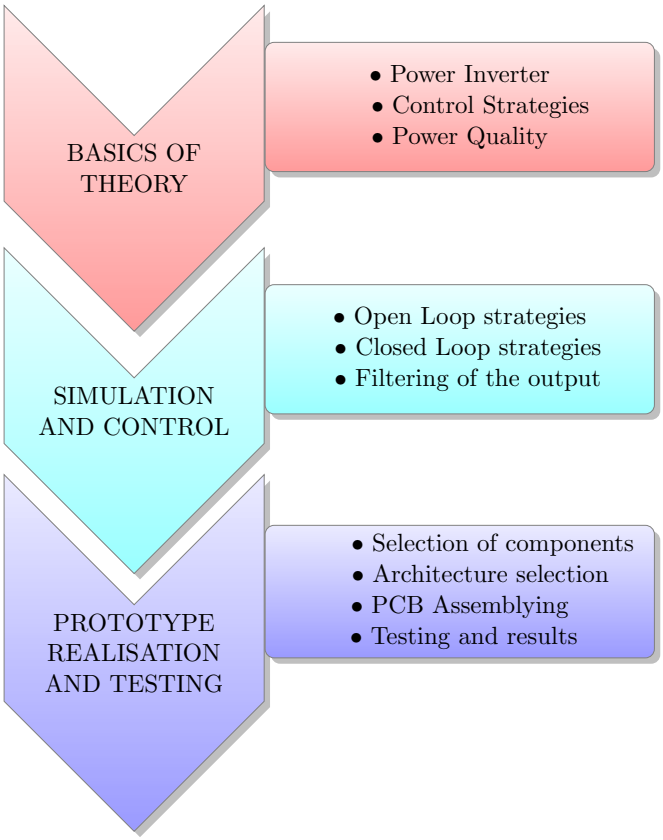


Figure 1.2 – Development process of the work.

The work is divided in four main parts. The first part, delineated in chapters 1 and 2, describes the prior knowledge to identify the concept of power inverter and multilevel inverter. Moreover, basic information on control strategies is also given, alongside with power quality observations.

The second part, which is elucidated in chapter 3, is about simulation and control of the 5LCHBI; open-loop and closed-loop strategies have been implemented, intending to control the output current and output voltage of the device. To obtain a better output quality, a filtering procedure has also been carried out. Due to the early stage of the project, this section was not focused on the development of a specific control strategy, but the effort has been put in simulating a wide range of control techniques such as sinusoidal pulse width modulation methods and closed-loop techniques based on PI and hysteresis controllers. The conventional two-level hysteresis current control, analyzed in section 2.7, has been extended to the five-level inverter. Afterwards, in section 3.4 a novel control algorithm, based on the multi-offset-band hysteresis current control [18] has been formulated and simulated, to evaluate its operations and stability. The results obtained in this section will be helpful in identifying, in future, the best control strategy to be applied on the electric machine drive.

Chapter 4 describes the third part, which is dedicated to the prototype realization, from the selection of the components to the subsequent architecture design and printed circuit board realization. Unlikely in mostly research paper and thesis, the whole designing process has been carefully explained, from the selection of components (section 4.2) to the consideration about the PCB design, delineated in section 4.3. In the prototype realization procedure, examined in 4.3.2, specific attention has also been put in the device parasitics reduction and mitigation.

The last part of this work, referring to chapter 5, is dedicated to test the device performances. The experiments that have been carried out, explained in section 5.1, started with the evaluation of the switches response to the gating signals. Subsequent tests, explicated in section 5.3, analyzed the full operativity of the inverter, which was connected to a DC input voltage and to an output load. The last experiments that has been carried through, explained in section 5.5, evaluated the thermal behavior of the device. A current of 13.2 A, which is greater that the one that will flow thorough the inverter in its final application, has been applied to the device for generating heat. The pictures obtained with the thermal camera enlighten the PCB hot zones, this procedure has been carried out also for identifying undesired hotspots, that could compromise the healthy operations of the device.

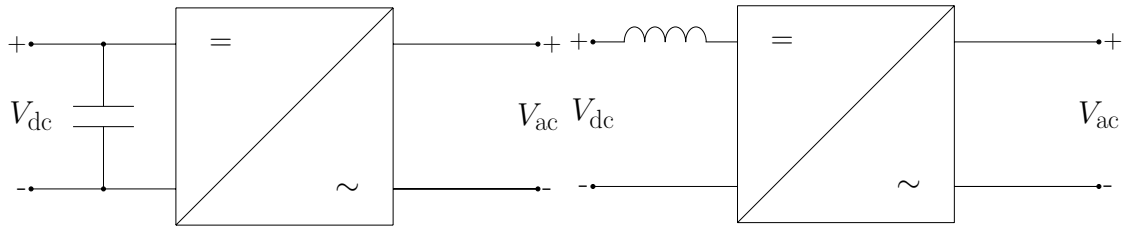
Due to the early stage of this project, it is necessary to identify some limitations:

- Most of the simulations have been performed on a generic load and the parameters have been chosen arbitrarily.
- All the simulations have been performed considering ideal and balanced input DC sources.
- The simulation that has been conducted on the feeding of a single phase of a multiphase PMSM machine, treats the load as a single-phase PMSM.
- Only bipolar Sinusoidal Pulse Width Modulation (SPWM) methods based have been implemented, with unity modulation index only.
- The tests conducted in the laboratory have been done on a single H-bridge module only.

2 Theoretical Basis

2.1 Introduction to the Power Inverter

Power inverters or simply known as inverters are power electronic devices able to produce, starting from a DC source, an AC output defined in phase, frequency and amplitude. Based on the type of the input and output they can be classified in two categories: Voltage Source Inverters (VSI) and Current Source Inverters (CSI) as shown in figure 2.1. VSIs are capable of converting a DC input voltage into a controlled AC voltage, similarly CSIs can perform a conversion of an input DC current into a controlled AC output current [5].



(a) Voltage Source Inverter **(b)** Current Source Inverter

Figure 2.1 – DC-AC inverter topologies (a) VSI and (b) CSI topology.

Depending by type of their output waveform, shown in figure 2.2, they can be categorized in three families:

- **Square Wave Inverters (SVI)** give as output a two-level output waveform.
- **Modified Square Wave Inverters (MSWI) or quasi-sine wave inverters** give as output a multi-step output waveform.
- **Pure-sine Inverters (PSI)** give as output a sine-wave output signal.

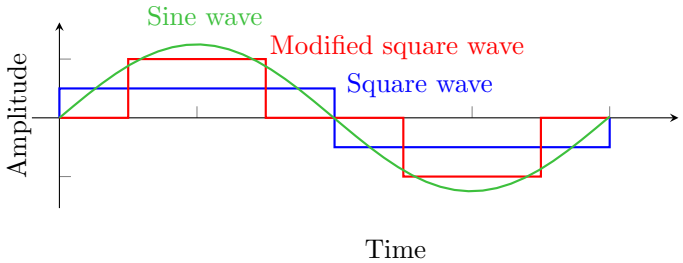
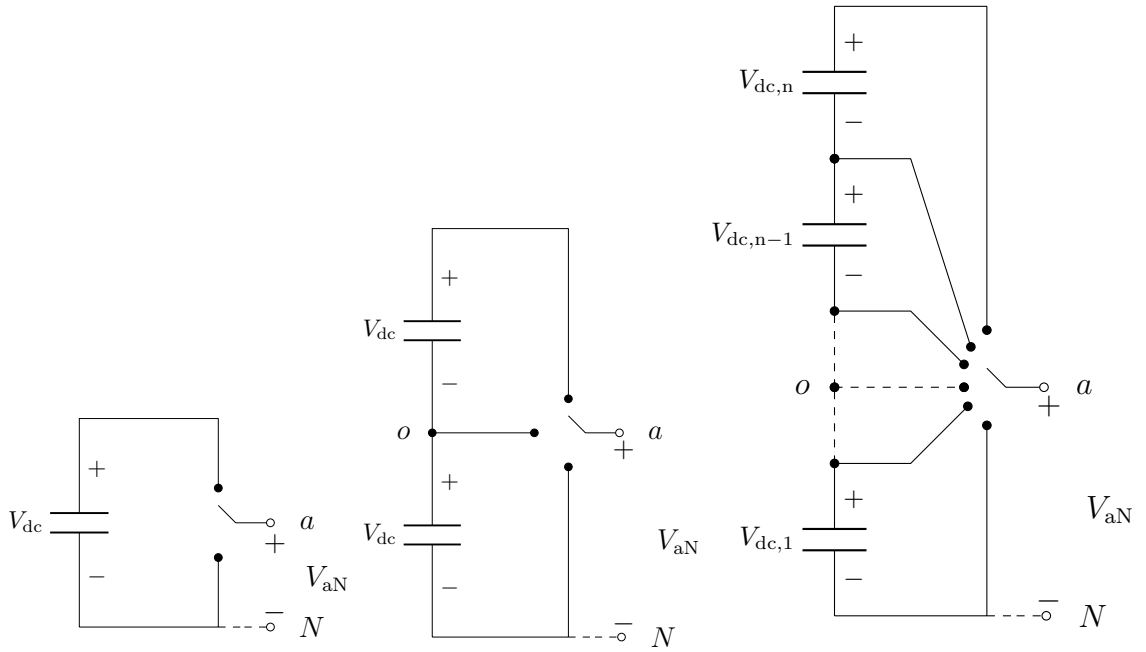


Figure 2.2 – Different output waveforms generated by inverters.

Square-wave inverters have been almost totally replaced by modified square wave inverters or pure-sine inverters because the output waveform they produce doesn't suit modern electrical appliances. Thanks to the recent advancements in semiconductor technology and digital controllers, it is possible to implement modified square wave inverters and pure sine inverters with high efficiency, good power quality and high reliability.

2.1.1 Introduction to the Multilevel Inverter

Square-wave inverters can produce only a two-levels output waveform nevertheless their design and control are relatively simple. They generally operate at high switching frequencies, that brings at having high switching losses and voltage stress on the switches, moreover it's difficult to interface these devices with high or medium voltage sources. The output is also affected by a high total harmonic distortion due to the low number of voltage output levels, which does not well approximate a sine wave. In 1975 the multilevel inverter topology concept has been introduced in order to face these drawbacks [13]. It's possible to increase the power rating of the inverter adding more voltage levels at its input, in this way, a multi-step output voltage waveform is achievable, that better approximates a sine wave. Next figure shows a general representation of the multilevel inverter concept.



(a) 2-level Inverter **(b)** 3-level Inverter **(c)** n-level Inverter

Figure 2.3 – Two-level inverter, three-level inverter and n-level inverter [24].

Considering n the number of voltage steps with respect [13] to the neutral terminal of the inverter o, then the number of voltage steps between two phases of the load m is

$$m = 2n + 1 \tag{2.1}$$

Table 2.1 make a comparison of the two-level inverter and the multilevel inverter main characteristics.

Table 2.1 – Comparison between two-level and multilevel inverters.

Subject of the analysis	Two-level inverter	Multilevel inverter
Output waveform THD	high	low
Switching stress	high	low
Voltage application	low voltage	high voltage
$\mathrm{d}v/\mathrm{d}t$ and EMI	high	low
Number of components	low	high

In the next sections multilevel inverter topologies will be better described, before this it's necessary to analyze the elementary inverter topologies on which multilevel inverter architectures are based.

2.2 Half-bridge Inverter

The half-bridge inverter is one of the simplest inverters, it's the elementary cell that constitutes the H-bridge inverter. It is composed by a DC voltage supply, two switches and two diodes. The node 0, the capacitors $C+$ and $C-$ are fictitious, generally they are not physically accessible, they are introduced in the schematics for future considerations only. The switches $T+$ and $T-$ work in a complementary: when $T+$ is ON, $T-$ is OFF and on the nodes a and o we obtain the voltage $+V_{\mathrm{dc}}/2$. Likewise, when $T+$ is OFF, and $T-$ is ON as output we obtain the voltage -$V_{\mathrm{dc}}/2$.

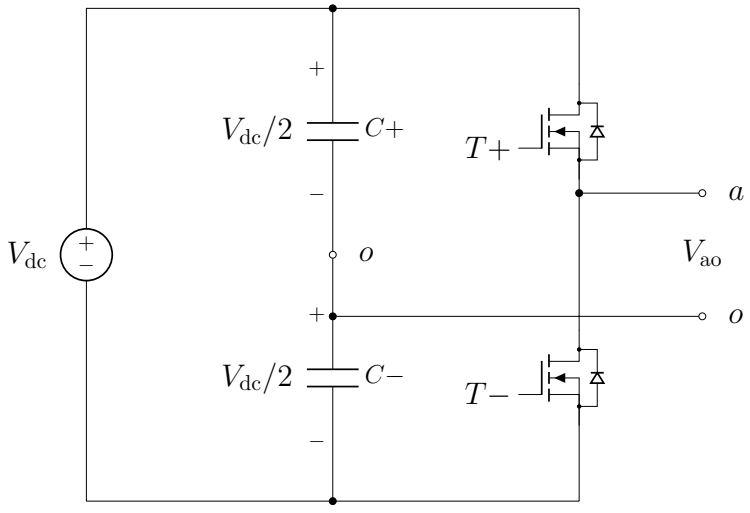


Figure 2.4 – Scheme of the half-bridge module.

Table 2.2 gives a summary of the half-bridge switching states, it is possible to notice that this device is only capable to give as output a 2-level voltage.

Table 2.2 – Half-bridge switching states.

$T+$	T-	(V_{ao})
1	0	$+\frac{V_{\text{dc}}}{2}$
0	1	$-\frac{V_{\text{dc}}}{2}$

2.3 H-bridge Inverter

The H-bridge inverter is composed by two half-bridge modules and it is the elementary cell that constitutes the cascaded H-bridge inverter, which is the focus of this thesis. The name H-bridge derives by the graphical representation of its circuit. The device is composed by four switches, two by two connected in series forming two legs.

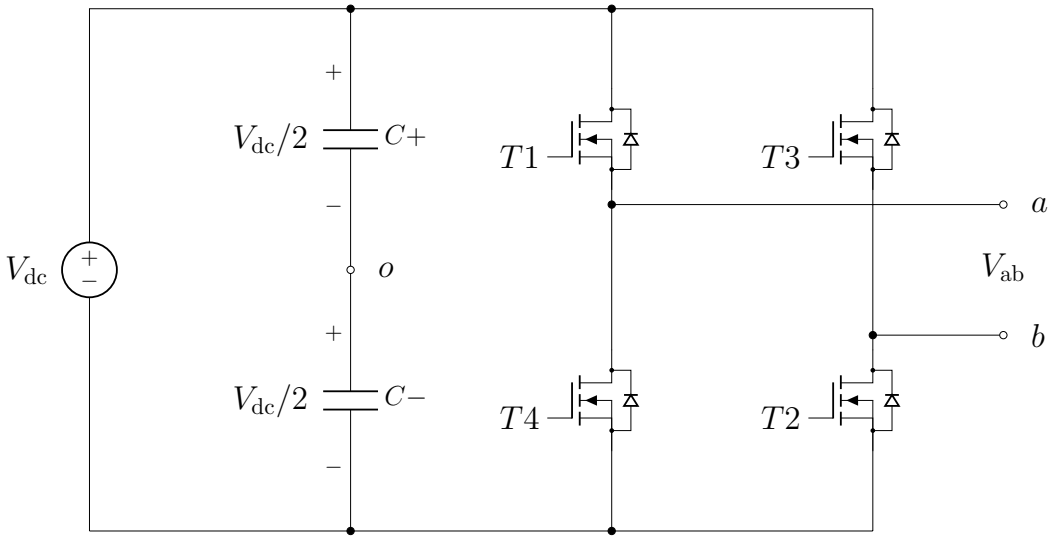


Figure 2.5 – Scheme of the H-bridge module.

The input DC voltage is usually fixed and constant while the output voltage V_{ab} can be adjusted by proper control strategies. The switches on the same leg operate in a complementary manner in order to avoid shortcuts. For driving a H-bridge module only two independent gating signals are necessary, these signals are generated by the control strategy. Keeping $T1$ and $T2$ closed (ON) give as output the voltage V_{dc}, this consequently means keeping T3 and T4 opened (OFF). On the contrary, keeping $T3$ and $T4$ closed gives as output the voltage $-V_{\text{dc}}$. The third possible switching state is obtained when $T1$ and $T3$ are ON, this gives as output the voltage 0.

Table 2.3 gives a summary of the H-bridge switching states, it is possible to notice that the additional half-bridge leg that has added to the circuit shown in figure 2.4 allows a third output value, in accord with equation 2.1.

Table 2.3 – H-bridge switching states.

T1-T2	*T3-T4*	Output voltage (V_{ab})
1	0	$+V_{dc}$
0	1	$-V_{dc}$
1	1	0

2.4 Generalities about Control Strategies

To obtain the desired output is necessary to drive the inverter's switches with proper control strategies. The inverter's final purpose and application will determine the most suitable control technique. It is possible to divide the control strategies in two families: open-loop control and closed-loop control techniques.

2.4.1 Open-loop Control Strategies

This type of control is also known as "non-feedback system" because the output doesn't influence the control action of the input. Initial parameters are sent to the controller that applies the desired control strategy, consequently it produces the control signal necessary to drive the inverter. The inverter's switches are driven only according to the input signal, disturbances such as load changes, faults and interference of any kind does not affect the control strategy [14]. The scheme of this principle is shown in figure 2.6.

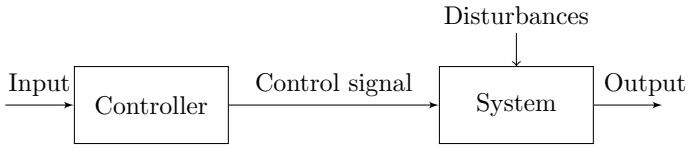


Figure 2.6 – Open-loop control block diagram [14].

It is possible to summarize the main characteristics of the open-loop control techniques:

- There is no comparison between the output and the desired values, the output only depends by the input parameters, which are fixed.
- Disturbs or changes in the systems do not affect the output.

- Generally, the implementation of these strategies is simple, and the system does not require a measurement process in order to operate.

Examples of open-loop strategies are the Sinusoidal Pulse Width Modulation (SWPM), which are probably the most used open-loop techniques to drive VSIs inverters. In this thesis some of these strategies have been studied and simulated and they will be presented more specifically in the following sections.

2.4.2 Closed-loop control strategies

In closed-loop control strategies a feedback control action is used to reduce the errors within the system, this aspect causes the main difference between these techniques and the open-loop ones. The output depends by the input parameters and by the feedback process. The control signal, which in the open-loop strategy was generated depending only by the input reference, now it is created by the controller that evaluates and processes an error. Generally, these strategies are more advantageous than the open-loop techniques because the controller can compensate any disturbances or changes in the system [14]. This error is generated in the following way:

$$\text{Error} = \text{Input} - \text{Feedback}$$

The purpose of the controller is to bring the error close to zero, as fast and in the best way as possible, guaranteeing the stability of the system. The block scheme of this principle is shown in figure below.

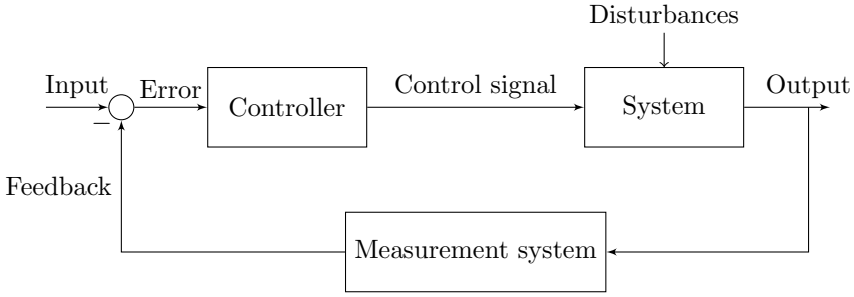


Figure 2.7 – Closed-loop control block diagram [14].

The main characteristics of the closed-loop strategy are:

- The controller can reduce the error adjusting the system input (Feedback).
- The controller is capable to compensate eventual disturbances or changes in the system.
- The control strategy becomes more complex and additional components such as measurement devices are necessary in the system.
- It is necessary to tune the controller(s) in order to guarantee the stability, this operation can be complex.

Hysteresis current control is an example of a closed-loop control technique, applied to an inverter, it allows to have an output generated from a current input reference. Inverters driven in this way are part of the CSI typology. It is possible to implement a closed-loop control

strategy on VSIs as well, for example using PI controllers to control the output voltage. In this work both methods have been analyzed and simulated, they will be deeply explained in the following sections.

2.5 SPWM Control Strategy

The SPWM process compares a high frequency triangular wave v_{tri} and a sinusoidal reference wave v_{sin} for generating the switching pulses necessary to drive the inverter. v_{tri} is at a frequency f_{s}, which determines the frequency at which the switches are switched. v_{sin} is used to modulate the switching duty ratio, its frequency is equal to f_1, which corresponds to desired fundamental frequency of the inverter voltage output. The ratio between the reference voltage amplitude and the triangular wave amplitude is called amplitude modulation index m_{a} ($\frac{vsin}{v_{\text{tri}}}$), if this parameter is kept in the range $0 \leqslant m_{\text{a}} \leqslant 1$ the inverter generates an output voltage linearly proportional to v_{sin}.
The frequency modulation index m_{f} ($\frac{f_{\text{s}}}{f_1}$) denotes the ratio between the carrier's frequency f_{s} and the fundamental frequency of the output voltage, the harmonic content of the output strongly depends by this parameter. Generally increasing the switching frequency improves the quality of the output voltage waveform and the eventual filtration process can be done easily [20].

2.5.1 SPWM Applied to the Half-bridge

The SPWM control strategy is first discussed referring to the half-bridge circuit topology shown in figure 2.4. The following table shows the generation of the pulses for the switches $T+$ and $T-$. When the sinusoidal wave amplitude is bigger than the triangular wave amplitude the comparator gives as output the logic value high, otherwise it's low [4, 24].

Table 2.4 – SPWM working principle.

	$T+$	T-	Output voltage (V_{ao})
$V_{\text{sin}}>V_{\text{tri}}$	1	0	$+\frac{V_{\text{dc}}}{2}$
$V_{\text{sin}}<V_{\text{tri}}$	0	1	$-\frac{V_{\text{dc}}}{2}$

Figure 2.8 illustrates the comparison process of the SPWM for the generation of the switching pulses. It is possible to see that the pulses correspond to the output voltage of the half-bridge inverter driven with this strategy, shown in figure 2.9.

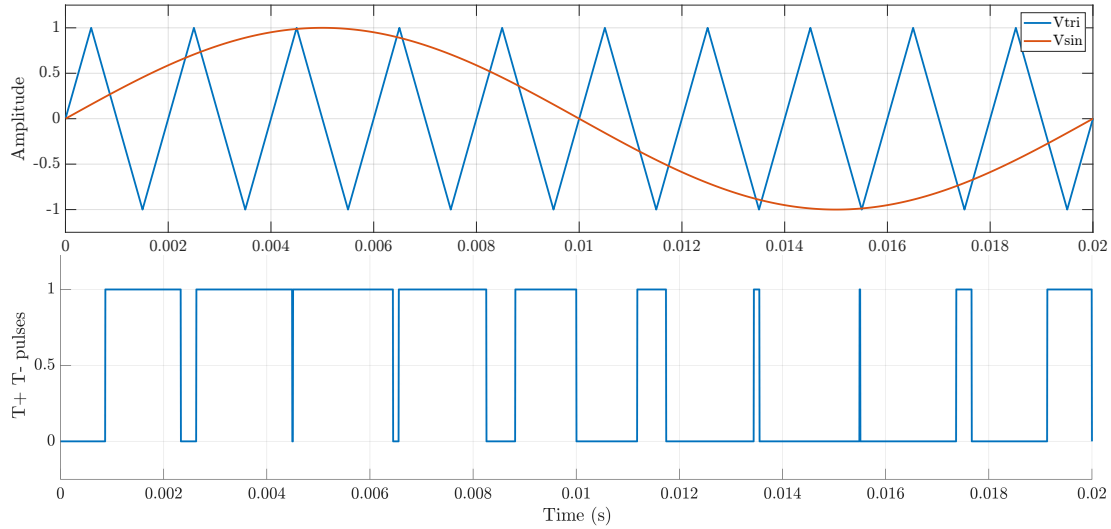


Figure 2.8 – Half-bridge SPWM principle.

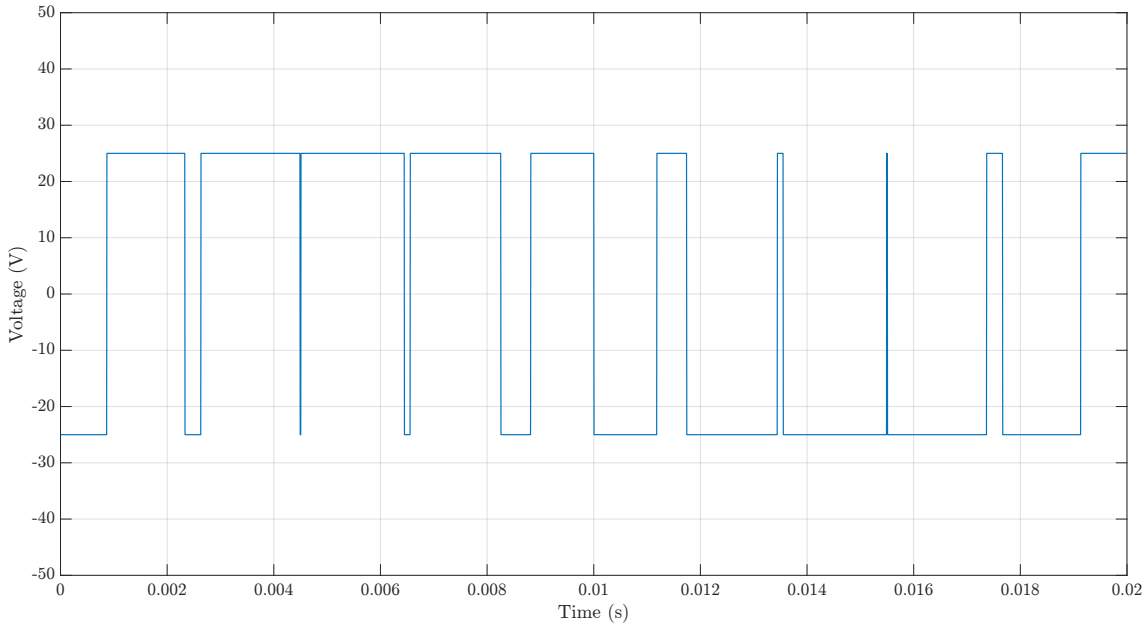


Figure 2.9 – Half-bridge output voltage obtained with SPWM.

2.5.2 SPWM Applied to the H-bridge

It's possible to extend the SPWM control method to the H-bridge module, starting from the considerations done in the half-bridge analysis. $T1 - T2$ and $T3 - T4$ are turned on and off at the same time. The switches on the diagonals of the inverter work synchronized and the upper and the lower switch on the same leg work in a complementary way. In this work only the bipolar SPWM will be analyzed but in the literature is possible find other SPWM control strategies, for example the unipolar voltage switching [20].

The following equations illustrate the SPWM principle applied to the H-bridge, the inverter driven in this way gives as output the double of the voltage obtainable with the half-bridge.

$$+\frac{V_{\mathrm{dc}}}{2}(T1-T4)=V_{\mathrm{ao}} \tag{2.2}$$

$$+\frac{V_{\mathrm{dc}}}{2}(T3-T2)=V_{\mathrm{bo}} \tag{2.3}$$

$$V_{\mathrm{ab}}=V_{\mathrm{ao}}-V_{\mathrm{bo}}=2V_{\mathrm{ao}} \tag{2.4}$$

Table 2.5 shows the output voltage of the inverter and the corresponding switching states.

Table 2.5 – H-bridge SPWM switching states and output voltages.

	T1-T2	*T3-T4*	V_{ao}	V_{bo}	$V_{ab}=V_{ao}-V_{bo}$
$V_{\mathrm{sin}}>V_{\mathrm{tri}}$	1	0	$+\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$+V_{\mathrm{dc}}$
$V_{\mathrm{sin}}<V_{\mathrm{tri}}$	0	1	$-\frac{V_{\mathrm{dc}}}{2}$	$+\frac{V_{\mathrm{dc}}}{2}$	$-V_{\mathrm{dc}}$

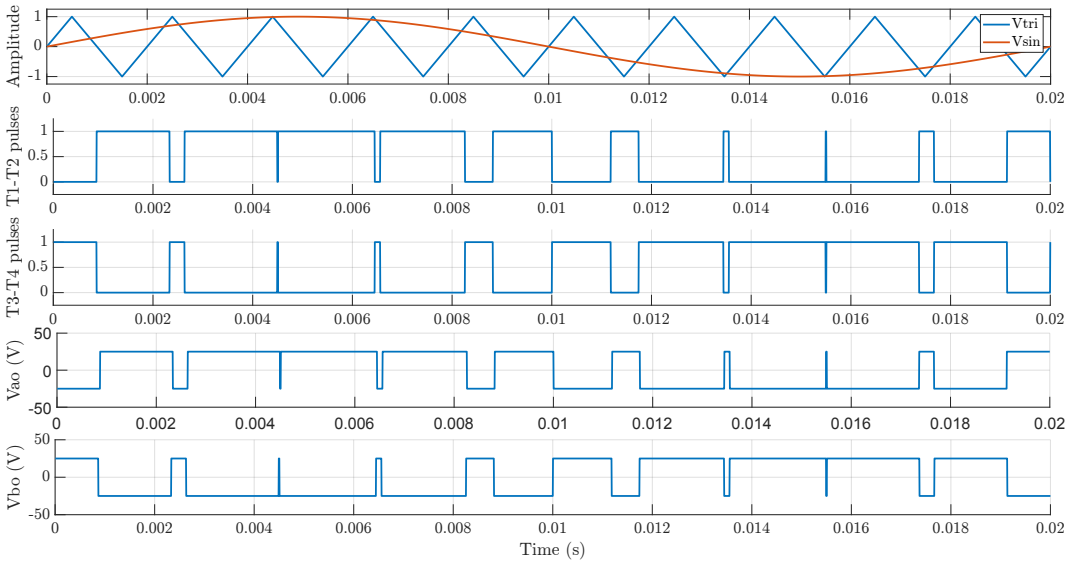


Figure 2.10 – SPWM principle applied on the H-bridge.

In figure 2.10 it is possible to see the working principle of the SPWM applied to the H-bridge inverter. The control strategy has been extended starting from the one applied to the half-bridge inverter, but equation 2.1 is not respected. In fact, this control strategy is not able to drive the inverter to generate the third output level, value which it is obtainable by this inverter. To obtain a 3-level output voltage, the control strategy must be further extended.

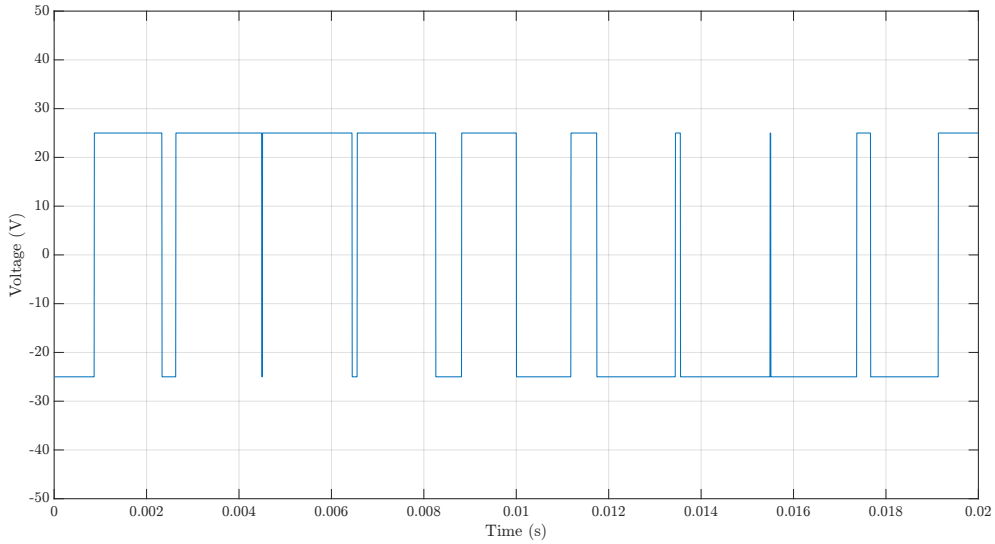


Figure 2.11 – H-bridge output voltage obtained with SPWM.

From figure 2.11 it is possible to see the output voltage generated by the H-bridge inverter driven with the SPWM. V_{out} is obtained according with equation 2.4.

2.6 Multiple Carrier PWM Techniques

In the SPWM technique a reference sine wave v_{sin} is compared with a single triangular wave v_{tri} (carrier) for generating the pulses to pilot the inverter's switches. It is possible extend this strategy increasing the number of carriers, this process is called multiple carrier modulation technique (MCPWM).
For driving a H-bridge inverter with this strategy, two carriers v_{tri1} and v_{tri2} are required, generally there are necessary $(n-1)$ carriers for a n level inverter. This control strategy allows to increase the number of output voltage levels, improving the quality of the signal reducing its harmonic content. The H-bridge driven in this way will give as output a three-level output voltage. In this work only the level-shifted MCPWM is applied to the H-bridge. Table 2.6 illustrates the MCPWM working principle and the possible switches states.

Table 2.6 – Multi-carrier PWM working principle.

	T1	*T4*	V_{ao}
$V_{\text{sin}}>V_{\text{tri1}}$	1	0	$+\frac{V_{\text{dc}}}{2}$
$V_{\text{sin}}<V_{\text{tri1}}$	0	1	$-\frac{V_{\text{dc}}}{2}$
	T2	*T3*	V_{bo}
$V_{sin}>V_{tri2}$	1	0	$-\frac{V_{dc}}{2}$
$V_{sin}<V_{tri2}$	0	1	$+\frac{V_{dc}}{2}$

Table 2.7 shows the switches states of the H-bridge driven with the MCPMW, the available output voltage levels are three: 0, $+V_{\mathrm{dc}}$ and $-V_{\mathrm{dc}}$. It can be noticed that the output voltage level 0 is obtainable by two different switches combinations (redundancy), this can be useful for optimizing the switching operations and for development of fault tolerant inverter drives.

Table 2.7 – H-bridge switches states with MCPWM

T1	*T2*	*T3*	*T4*	$V_{ab} = V_{ao} - V_{bo}$
1	1	0	0	$+V_{\mathrm{dc}}$
0	0	1	1	$-V_{\mathrm{dc}}$
1	0	1	0	0
0	1	0	1	0

Figure 2.12 shows the MCPWM principle, it is possible to distinguish the carriers v_{tri1} and v_{tri2} which are vertically shifted. The reference sine wave V_{sin} oscillates from the maximum value of +1 to the minimum value of -1, according to the modulation index $m_{\mathrm{a}} = 1$.

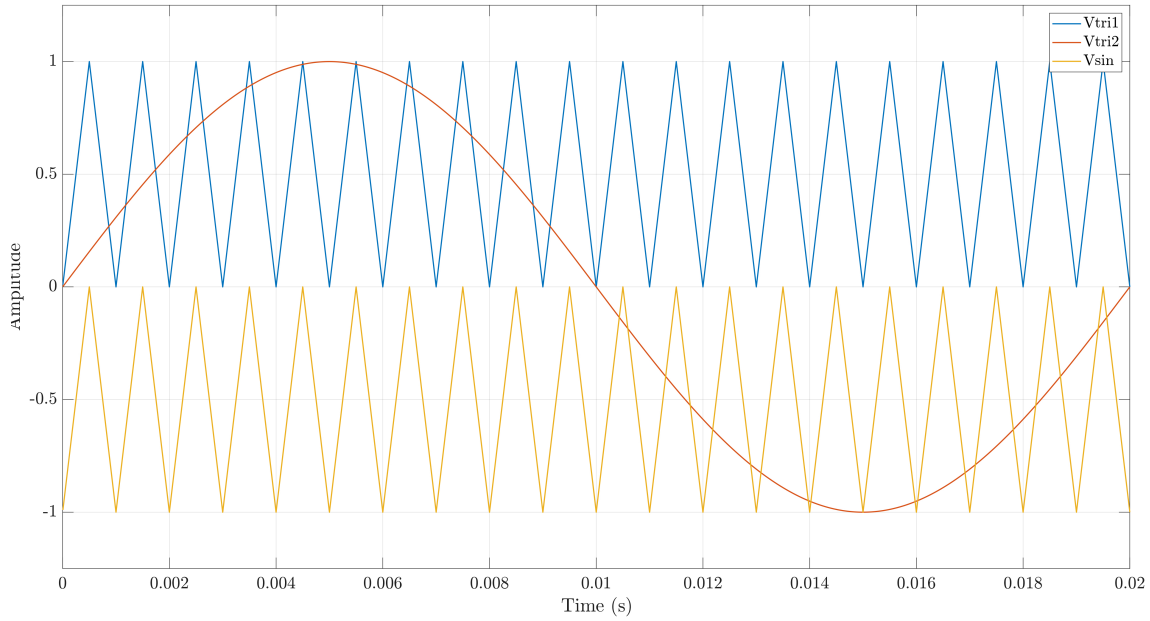


Figure 2.12 – Multi carrier PWM principle.

Figure 2.13 shows the output voltage obtained with the MCPWM strategy applied to the H-bridge inverter, it is possible to distinguish the three different output voltage levels. It is important to remark the fact that without the addition of more components to the H-bridge scheme shown in figure 2.5, an additional voltage step is obtained as output, thanks to the MCPWM technique.

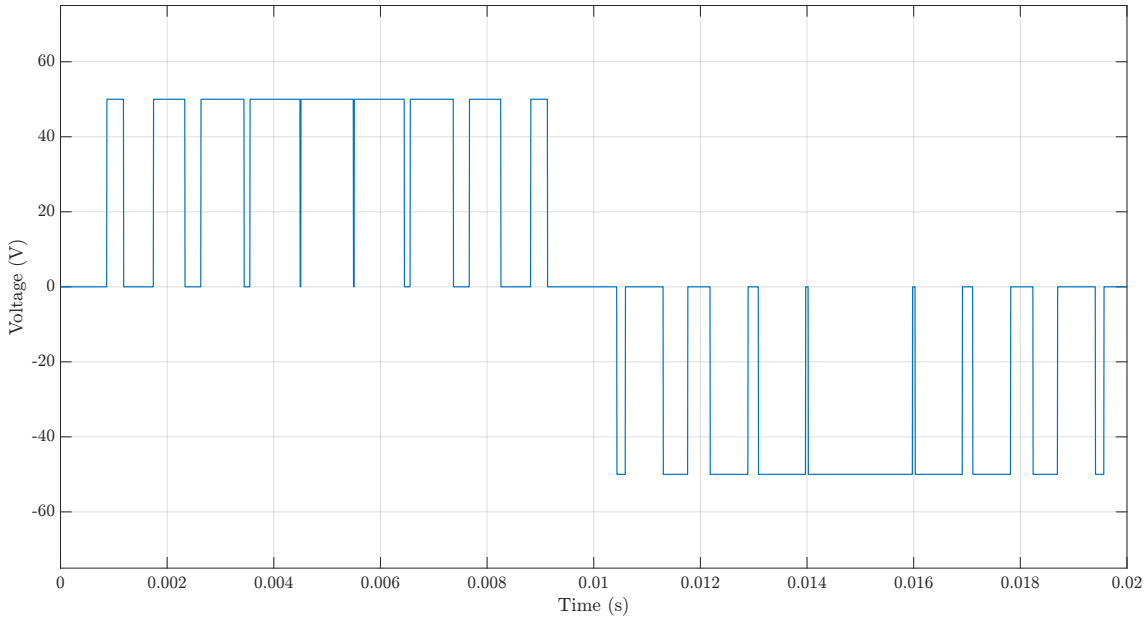


Figure 2.13 – H-bridge output voltage obtained with MCPWM.

By the introduction of an additional level, thanks to the MCPWM strategy, the output voltage V_{ab} improves in quality, it approximates better a sinewave, with a consequent reduction of the THD.

2.7 Hysteresis Current Control

In the perspective of a current-controlled inverter realization, the hysteresis current control is introduced and analyzed. Subsequently this technique will be applied to the previous explained inverter topologies, and the results will be presented and discussed. Hysteresis current control is a very simple, stable and effective method which gives a good dynamic performance. Despite the large number of advantages, the switching frequency is not limited because it is a function of the input parameters, however it can be limited using additional circuitry [23].

2.7.1 Hysteresis Current Control Applied to the Half-bridge

This control strategy generates the switching signals from the evaluation of the actual current error with a tolerance band. The current follows the reference current included in a hysteresis band. If the current goes over the upper limit, the upper switch of the inverter leg is turned off, simultaneously the lower switch of the inverter leg is turned on, making the current fall. If the current goes under the inferior limit, the lower switch of the inverter leg is turned off and the upper switch is turned on, making the current rise. The block scheme is represented in figure 2.14.

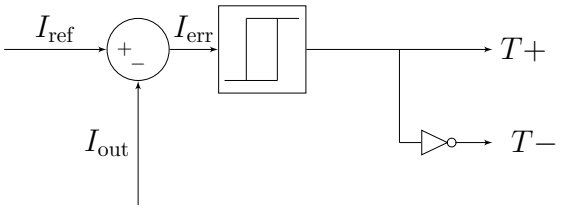


Figure 2.14 – Block scheme of the hysteresis control principle.

This process forces the current to stay between in the boundaries of the hysteresis band [23]. The following table shows the working principle of the hysteresis control applied to the half-bridge; h is the amplitude of the hysteresis band. The value of the amplitude band strongly influences the switching frequency, in fact, decreasing the amplitude band value means decreasing the output current error. The switching frequency increases because the output current path between the two hysteresis boundaries becomes shorter.

Table 2.8 – Hysteresis current control working principle.

	$T+$	T-
Output current $> +h$	0	1
Output current $< -h$	1	0

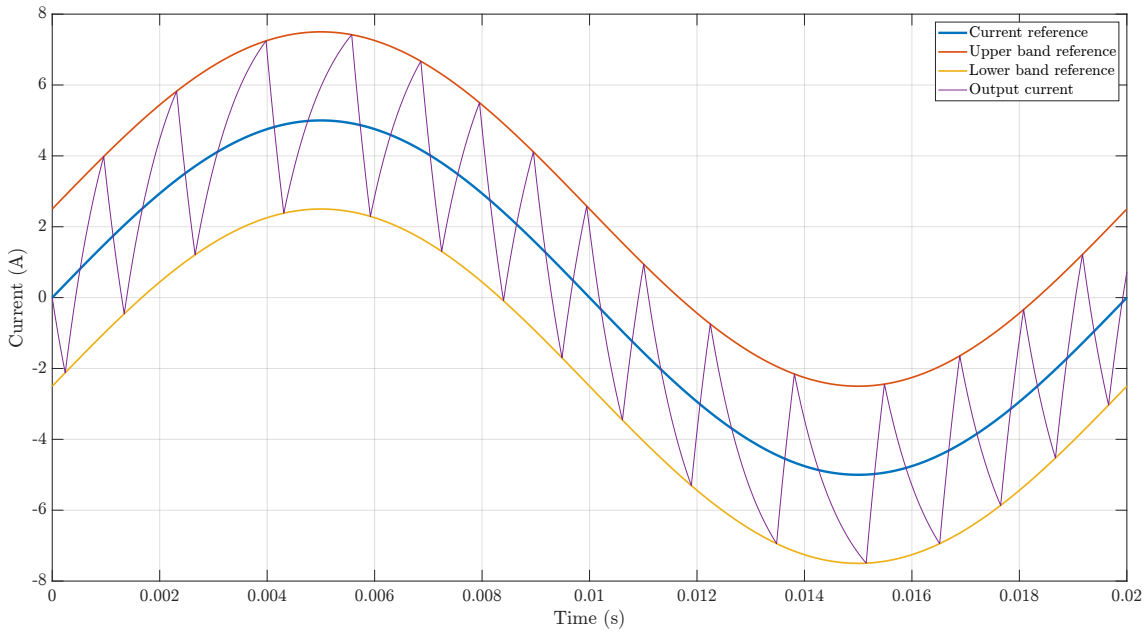


Figure 2.15 – Hysteresis current control principle.

In figure 2.15 it is possible to see the control principle of this method, the sinewave current reference I_{ref} is set and consequently the upper I_{up} and lower I_{lo} band references. The controller forces the output current I_{out} to stay in between the boundaries. A reduction in the hysteresis band amplitude value will result in a better-quality output current which will be closer to the current reference I_{ref}. A consequence of this will be an increase of the switching frequency because the current will encounter the boundaries I_{ref} and I_{lo} in a shorter time, fastening the switching speed. As aforementioned, the switching frequency is a function of the maximum error set, which corresponds to the hysteresis band amplitude.

Figure 2.16 shows the output voltage obtained running the half-bridge inverter with the hysteresis current control, as it is for the switching frequency, V_{out} is a function of the set hysteresis band amplitude. The hysteresis current control is applied on a half-bridge, consequently only a 2-level output voltage is obtained, according to equation 2.1. The device obtained is called bang-bang controller [16] and it is able only to switch the output conditions from a "ON" value to an "OFF" value and vice versa. Conforming to this, the half-bridge inverter driven in this way is only able to produce a output voltage swinging between $+V\text{dc}/2$ and $-V\text{dc}/2$. In the next sections, it will be possible to see that the introduction of additional voltage levels in the system, and a consequent extension of the hysteresis current control, will result in less distorted output current and voltage waveforms.

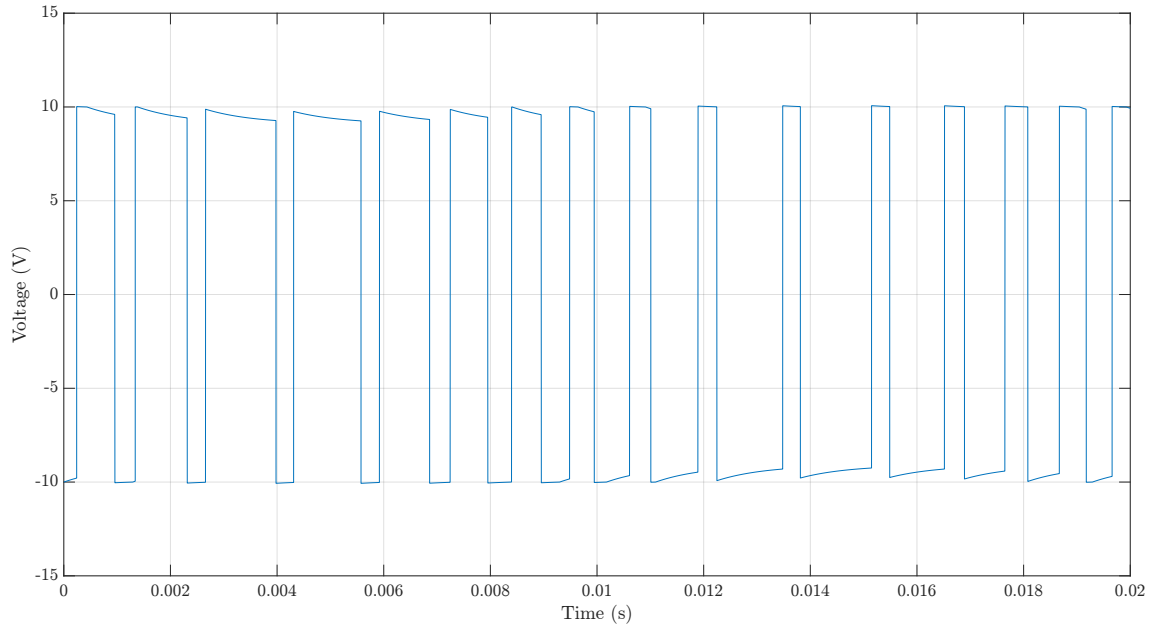


Figure 2.16 – Output voltage obtained with the hysteresis current control applied to the half-bridge inverter.

2.7.2 Multi-offset-band Hysteresis Current Control

To extend the hysteresis control to the H-bridge, a novel algorithm based on the multi-offset-band Hysteresis Current Regulation (MOBHM) [11] has been formulated, implemented and simulated. Starting from the evaluation of the difference between the current reference and the output current (current error), the control system chooses the most suitable voltage level. Subsequently the system generates the switching pulses to give as output the desired value. The working principle of the strategy is the following: multiple bands are introduced in the control architecture; these bands have the same fixed amplitude and they are vertically shifted by a parameter α. A dead zone δ is introduced between the bands to avoid any overlapping. If the voltage level that appears at the boundaries of the hysteresis band is not sufficient to reduce the error, the control strategy allows to move in another band. Two hysteresis bands are necessary to drive an H-bridge inverter with this strategy, generally there are necessary $(n-1)$ hysteresis bands for a n level inverter. Figure 2.17 shows the working principle of the MOBHM applied to the H-bridge, the two hysteresis bands are visible, vertically shifted and delimited by the blue and red dashed lines.

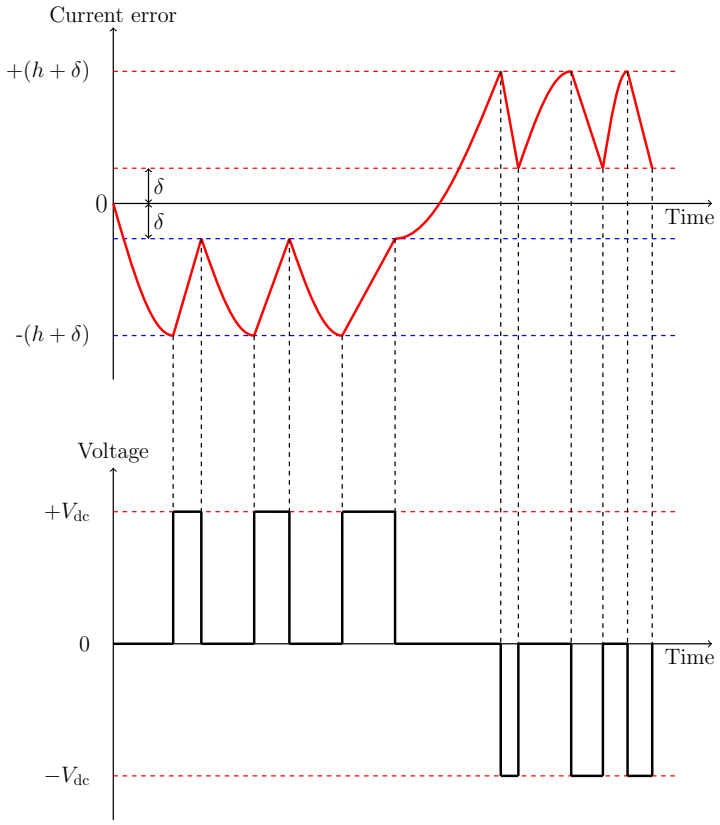


Figure 2.17 – Principle of the implemented multi offset band hysteresis current control technique.

The parameters of the simulation were chosen arbitrarily, and they are reported in table 2.9.

Table 2.9 – Parameters used to simulate the MOBHM control technique.

Parameter	Name	Value
Input voltage	V_{dc}	20 V
Resistive load	R_{load}	1 Ω
Inductive load	L_{load}	1 mH
Current reference	I_{ref}	5 A
Anti-overlapping gap	δ	0.05 A
Maximum current error / Band amplitude	h	1 A
Shifting between two adjacent bands	α	1.2 A

This method is effective and relatively simple to implement, the result plots shows that the current error is always kept below the set value. Thanks to the introduction of the additional voltage level, it is possible to see a less distorted voltage at the output terminal. During the voltage change of polarity there is an interval of time in which the current has a free-wheeling behavior, the waveform of the current in this portion of time strongly depends by the load characteristics. Even if the current error is kept in the acceptance band in the free-wheeling zone the current is not well controlled. The switching frequency is not limited, and that can result into high voltage stress or even faults in the switching devices. It is possible overcome these issues implementing the multiband hysteresis current control based on time and magnitude error [8], which it is an evolution of the described method.

Figure 2.18 shows the output voltage, current and the current error. In the current waveform plot is it possible to distinguish the free-wheeling effect, direct consequence of the voltage change of polarity, this is also evident in the current error plot.

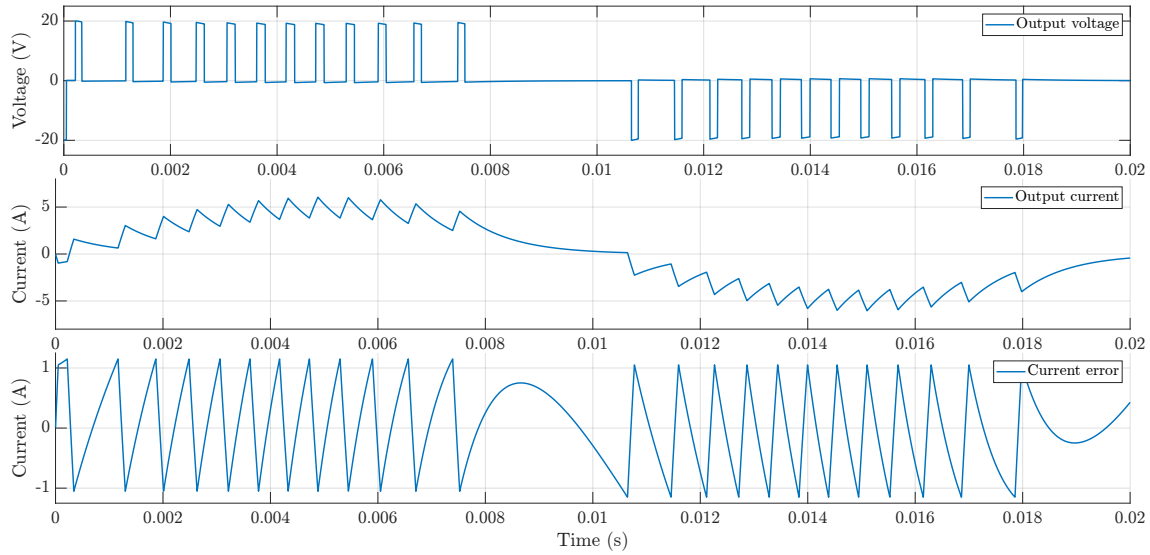


Figure 2.18 – Output voltage, current, and current error.

2.8 Topological Overview of Multilevel inverters

The concept of the multilevel inverter has been introduced in subsection 2.1.1 In this section a deeper analysis will be conducted, showing the main inverter topologies, their advantages and limitations. There are three main multilevel inverter topologies: Neutral Point Clamped (NPC) and Flying Capacitors (FC) inverters which require a single DC input source and Cascaded H-bridge (CHB) which require multiple input DC sources, as it is schematized in figure 2.19.

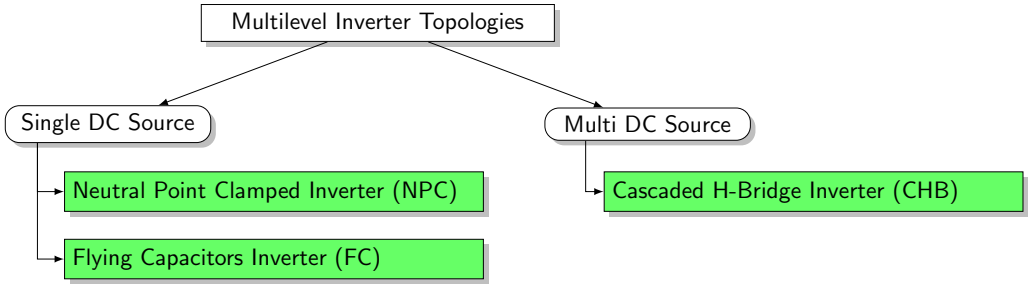


Figure 2.19 – Multilevel inverter topologies.

2.8.1 Neutral Point Clamped Multilevel Inverter

An NPC inverter is shown in the figure 2.20, in the specific it is a three-level clamped inverter. A DC input voltage is split into three levels by two capacitors C_1 and C_2 connected in series. The node between the two capacitors can be defined as a neutral point n. Using this configuration in possible to have as output three voltage levels: $+V_{\mathrm{dc}}/2$, $-V_{\mathrm{dc}}/2$ and 0. If the switches T1 and T2 are ON, the output voltage at the output nodes a and n is $+V_{\mathrm{dc}}/2$. For getting as output the voltage $-V_{\mathrm{dc}}/2$, T3 and T4 must be ON. If T2 and T3 are ON, as output we get the 0 level [34]. The switching states are shown in table below.

Table 2.10 – NPC switching states.

T1	*T2*	*T3*	*T4*	V_{an}
1	1	0	0	$+V_{\mathrm{dc}}$
0	0	1	1	$-V_{\mathrm{dc}}$
0	1	1	0	0

The main feature of this multilevel inverter topology are the two diodes $D1$ and $D2$, they clamp the voltage of the switch half of the input DC voltage. Thanks to this is possible to obtain multiple input levels starting from a single DC input. The main characteristics of the NPC are [34]:

- If enough voltage levels are deployed it's not necessary to filter the output.

- The NPC has a high efficiency because the switches are driven at the fundamental frequency.
- The NPC allows to control the reactive power flow.
- When the number of level grows, it's necessary to use a big amount of clamping diodes.
- The maximum number of level obtainable is limited by the recovery time of the diodes.

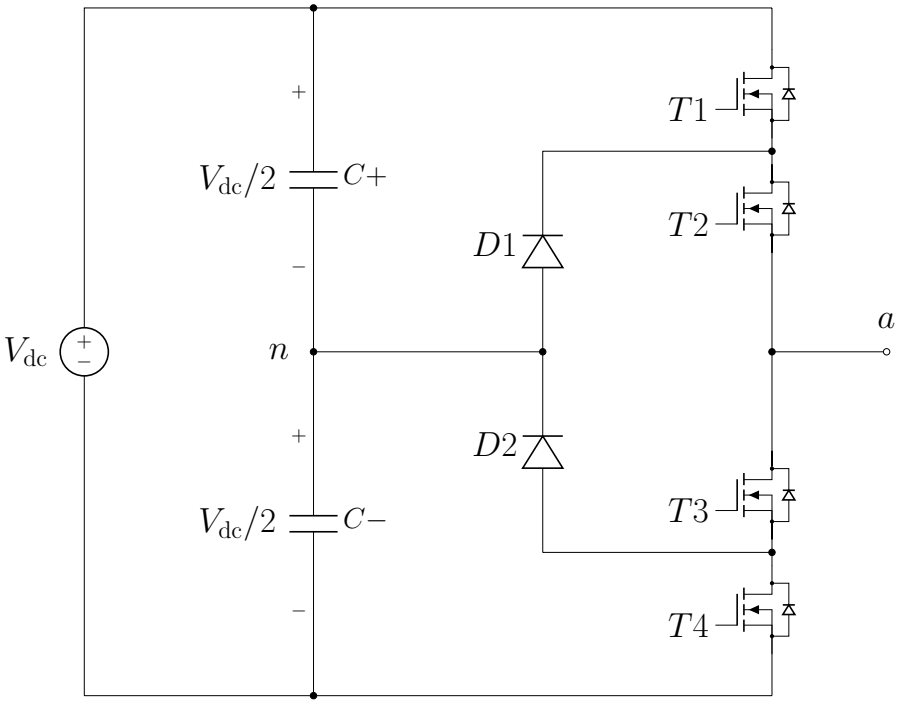


Figure 2.20 – Three-level NPC inverter [24].

2.8.2 Flying Capacitors Multilevel Inverter

A FC multilevel inverter is shown in figure 2.21, more precisely a three-level FC. The voltage clamping operation in this inverter topology is done by capacitors instead of diodes, the name of this inverter derives by the fact that the output potential floats respect to the ground potential. $C1$ is the clamping capacitor, it's charged when $S1$ and $S3$ are turned on, and it's discharged when $S2$ and $S4$ are turned off [34]. The inverter in this configuration is able to give as output three voltage levels across a and n : $+V_{dc}/2$, $-V_{dc}/2$ and 0. When $T1$ and $T2$ are ON as output it is obtained the voltage $+V_{dc}$. To get $-V_{dc}$ $T3$ and $T4$ are kept closed while for getting as output the voltage level 0 either pair $S1$ and $S3$ or $S2$ and $S4$ needs to be turned on [34]. The summary of the switching states is shown in table 2.11.

Table 2.11 – FC switching states.

T1	*T2*	*T3*	*T4*	V_{an}
1	1	0	0	$+V_{\mathrm{dc}}$
0	0	1	1	$-V_{\mathrm{dc}}$
0	1	0	1	0
1	0	1	0	0

The main characteristics of the FC multilevel inverters are:

- Many voltage levels can be achieved with different switching states (Redundancy for voltage levels).
- If enough voltage levels are deployed, it's not necessary to filter the output.
- The NPC allows to control the reactive and active power flow.
- When the number of level grows, it's necessary to use a big amount of capacitors.
- In active power transmission the losses are high, and the control of the inverter is difficult.
- In the beginning it's necessary to control the capacitors' charge.

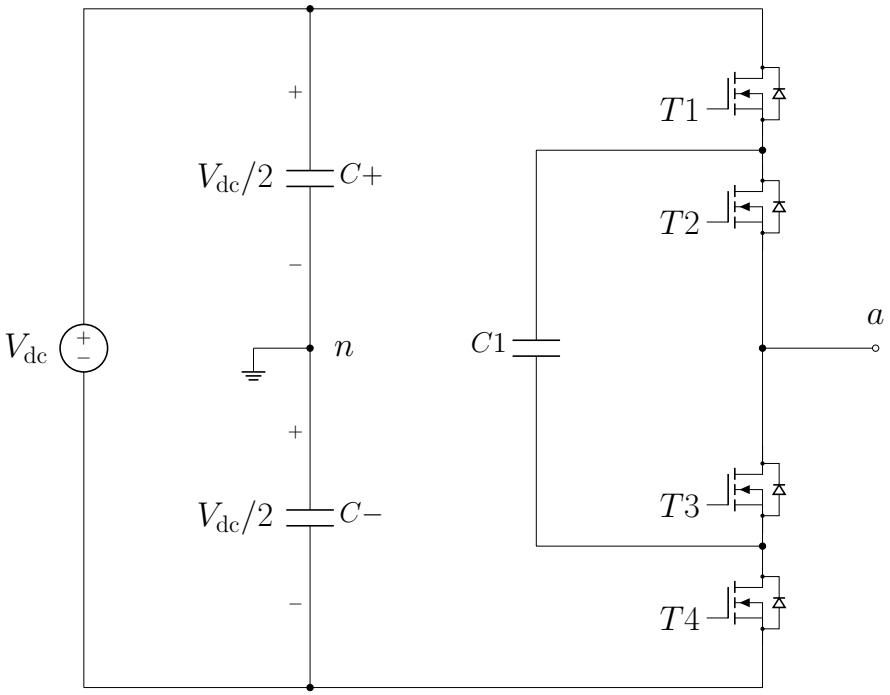


Figure 2.21 – Three-level FC inverter [24].

2.8.3 Cascaded H-bridge Multilevel Inverter

In the Cascaded H-bridge (CHB) inverter, multiple H-bridges with independent DC sources are connected in series. Every module can give as output three different voltage levels, the output voltage of the inverter V_{ab} is the sum of the output voltage that is generated in every cell. The number of the output voltages are $(2N + 1)$ where N is the number of H-bridge modules connected in series. Due to its modular structure some voltage levels are obtainable from different (redundant) switching states, this allows to have a great flexibility in the switching pattern design [34].

The main features of this topology are:

- **Reduced number of components**: Compared with the other multi-level inverter topologies, the CHB requires a reduced number of components, and it doesn't require clamping diodes and clamping capacitors.
- **Flexible structure and design:** Thanks to its flexible structure it's possible to extend the inverter to any number of levels.
- **Low voltage stress on the switch:** Since the CHB is composed by single H-bridge modules, the voltage that the switches must stand is determined by the voltage of the DC input source.
- **Good output quality:** The voltage output quality obtainable with this inverter has a low Total Harmonic Distortion (THD), and this value is directly affected by the number of voltage levels exploited to create the output waveform.
- **Fault tolerance:** Because of their cascaded structure in case of failure is possible to bypass the faulty cell reducing the number of the voltage levels originally available but ensuring the fault tolerance.

The disadvantages of the CHB inverter are the:

- **Requirement of multiple DC sources**: This inverter requires multiple DC sources; it is possible to use multi-winding transformers to make multiple input sources but this solution will increase the cost and the complexity of the system.
- **DC Voltage stress if using Level-Shifted modulation strategies**: H-bridge modules can generate higher and lower voltage levels, this can bring to an unequal discharge of the batteries, if used as DC source. The lifespan of the battery can decrease significantly, but this issue can be solved using DC side capacitors.

Figure 5.6 represents the 5-level CHB inverter, which it is the focus of the thesis, the two H-Bridge modules connected in series are clearly visible. With this configuration, the 5LCHBI can give as output five different voltage levels: $+2V_{\mathrm{dc}}$, V_{dc}, 0, $-V_{\mathrm{dc}}$, $-2V_{\mathrm{dc}}$.

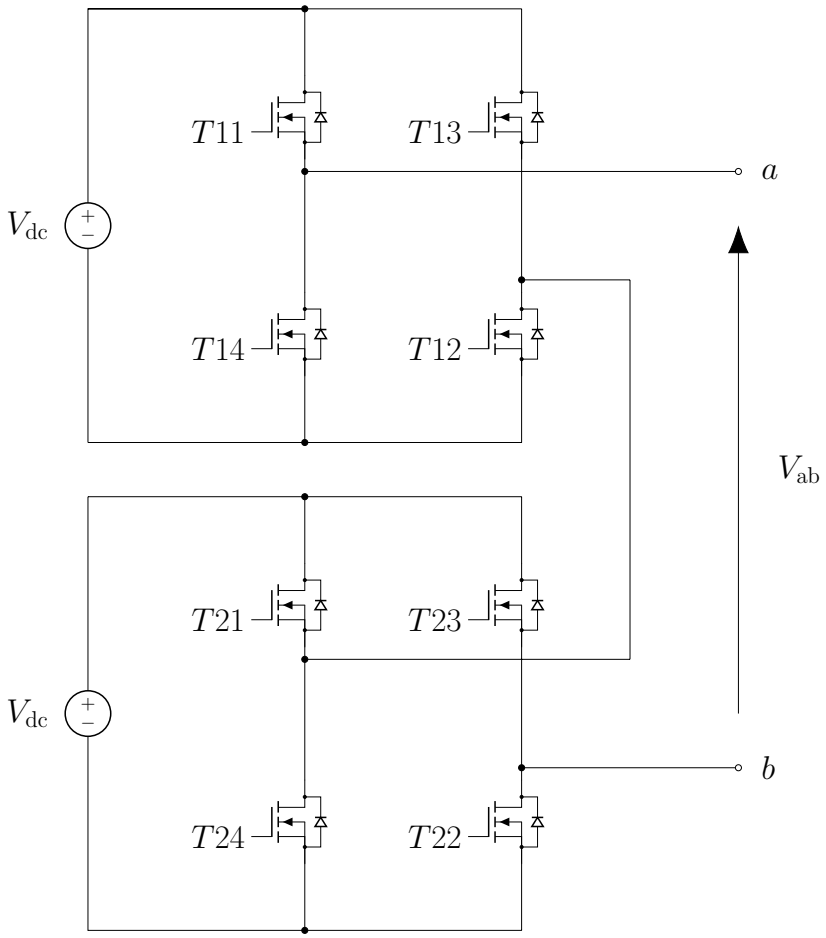


Figure 2.22 – Scheme of the five-level CHB inverter.

Table 2.12 – CHB inverter switching states and voltage output values.

T11	*T12*	*T13*	*T14*	*T21*	*T22*	*T23*	*T24*	V_{ab}
1	1	0	0	1	1	0	0	$+2V_{\mathrm{dc}}$
0	0	1	1	0	0	1	1	$-2V_{\mathrm{dc}}$
1	0	1	0	1	1	0	0	$+V_{\mathrm{dc}}$
0	1	0	1	0	0	1	1	$-V_{\mathrm{dc}}$
0	1	0	1	0	1	0	1	0

Table 2.12 represents the CHB inverter switching states along with the correspondent output voltage values. There are other possible switching combinations that have been omitted because redundant.

2.9 Power Quality

To understand better the simulation results that will be introduced in the next sections, it's important to give some definitions to define what power quality is. Generally, the goal of a DC-AC inverter is to produce an output waveform which is as close as possible to a sine wave. Because of several causes such as the modulation strategy used and disturbances in the system, the output result shows harmonic distortion. The Fourier decomposition theory is briefly presented to subsequently describe the concept of Total Harmonic Distortion (THD).

2.9.1 Fourier Analysis of Repetitive Waveforms

Generally, a non-sinusoidal waveform $f(t)$, repeating with an angular frequency ω can be expressed as [20]

$$f(t) = F_0 + \sum_{\mathrm{h}=1}^{\infty} f_{\mathrm{h}}(t) = \frac{1}{2}a_0 + \sum_{\mathrm{h}=1}^{\infty}\{a_{\mathrm{h}}\cos(h\omega t) + b_{\mathrm{h}}\sin(h\omega t)\} \tag{2.5}$$

where $F_0 = \frac{1}{2}a_0$ is the average value.

$$a_{\mathrm{h}} = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(h\omega t)\,d(\omega t) \qquad h = 0, ..., \infty \tag{2.6}$$

$$b_{\mathrm{h}} = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(h\omega t)\,d(\omega t) \qquad h = 0, ..., \infty \tag{2.7}$$

From the equations 2.1, 2.2 and 2.3 it is possible to define the average value

$$F_0 = \frac{1}{2}a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(t)\,d(\omega t) = \frac{1}{T}\int_0^{T} f(t)\,d(t) \tag{2.8}$$

Every component of equation 2.1. can be represented in terms of its rms value

$$\mathbf{F}_{\mathrm{h}} = F_{\mathrm{h}} e^{\mathrm{j}\phi_{\mathrm{h}}} \tag{2.9}$$

and its rms magnitude is

$$F_{\mathrm{h}} = \frac{\sqrt{a_h^2 + b_h^2}}{\sqrt{2}} \tag{2.10}$$

The rms for the whole signal is defined as it follows

$$F = \sqrt{F_0^2 + \sum_{\mathrm{h}=1}^{\infty} F_{\mathrm{h}}^2} \tag{2.11}$$

The total distortion power is defined as

$$F_{\mathrm{dis}} = \sqrt{F^2 - F_1^2} = \sqrt{\sum_{\mathrm{h}\neq 1}^{\infty} F_{\mathrm{h}}^2} \tag{2.12}$$

2.9.2 Total Harmonic Distortion and Harmonic Spectrum Analysis

The Fourier decomposition allows to build the harmonic spectrum and consequently evaluate the waveform quality. A typical output waveform is constituted by a fundamental component, that has the same frequency (f_1) as the desired output, and other harmonics, which can be multiple or submultiple of the fundamental component. The total harmonic distortion (THD) quantifies the distortion in the voltage or in the current waveform, it is defined as the ratio between the harmonic content except the first harmonic and the first harmonic.

$$\mathrm{THD}_{\%} = 100\frac{F_{\mathrm{dis}}}{F_1} = 100\frac{F^2 - F_1^2}{F_1} = 100\sqrt{\sum_{\mathrm{h}\neq 1}^{\infty} \left(\frac{F_{\mathrm{h}}}{F_1}\right)^2} \tag{2.13}$$

Current and voltage THD values should be as low as possible because high distorted waveforms reflect into high injection of harmonics in the input and in the output of the inverter. These harmonics can cause a reduction of the active power transmitted, diminishing the efficiency of the system. Also, if for example the inverter is feeding an electrical machine, highly distorted current and voltage can generate vibrations, noise, and overheat in the machine. For reducing the THD is it possible to act on the modulation strategy, however if the inverter's application demands low distorted output voltage and current it is possible to implement some filtering strategies, which are highly effective in the THD value diminishing.

3 Control and Simulation of the 5-level CHB Inverter

In the previous chapter, the control techniques mentioned and explained have been considered for half-bridge and H-bridge inverters only. These inverters are the elementary blocks that constitute the CHB inverter. Thanks to this modularity concept, it is possible to extend the previous examined control strategies on the 5LCHBI. In first there will be explained the MCPWM control strategies and afterwards the multi-band hysteresis control and dual loop PI voltage control techniques will be analyzed.

3.1 Multiple Carrier PWM Strategies Applied to the 5-level CHB Inverter

These control techniques are are a natural extension of the MCPWM previously explained applied to the H-bridge. The main difference between the methods relies in the disposition of the carriers signals. The phase shifted method, as the name suggests, uses a phase shifted carrier to generate the switching pulses. Meanwhile the level shifted techniques, which include three different techniques, rely on a distinct vertically shifted carriers. All these MCPWM techniques have been simulated and analyzed and they will be explained in the next sections.

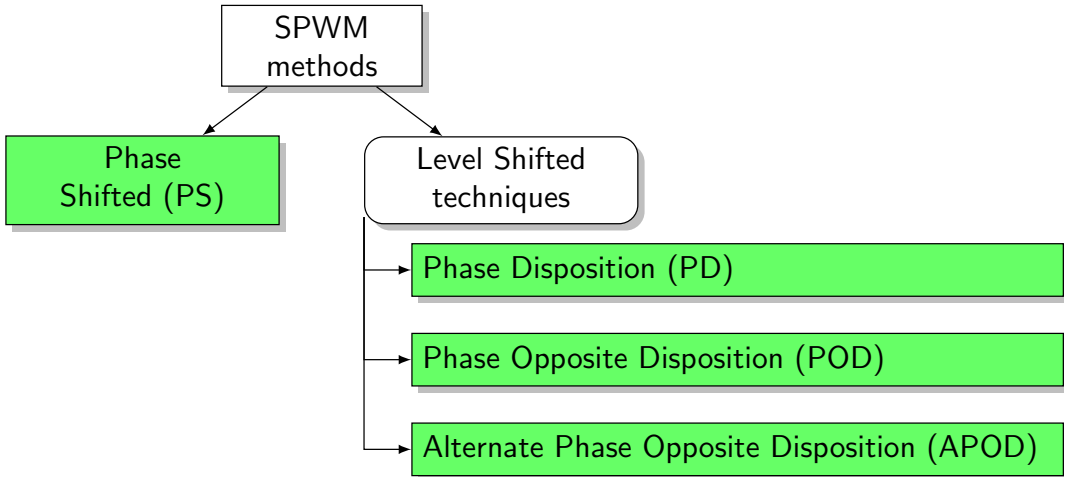


Figure 3.1 – Multilevel SPWM methods.

3.2 Phase Shifted Method

In order to generate the switching pulses for the 5LCHBI using the PS PWM strategy four carriers must be deployed. The carriers have the same frequency and the same peak-to-peak amplitude, but they are phase-shifted between adjacent carriers by:

$$\varphi_{\text{cr}} = \frac{360°}{n-1} \tag{3.1}$$

where n is the number of the inverter's voltage levels.

The modulating signal used is a sinusoidal wave v_{sin}, adjustable in amplitude, frequency and phase angle. The four carriers are phase shifted by 90° according to the equation 3.1. Each triangular wave is assigned to a leg of the inverter, the comparison process with v_{tri} generates the switching pulses for the two switches of the considered sub-module. The principle pf the phase shifted PWM is shown in figure 3.2.

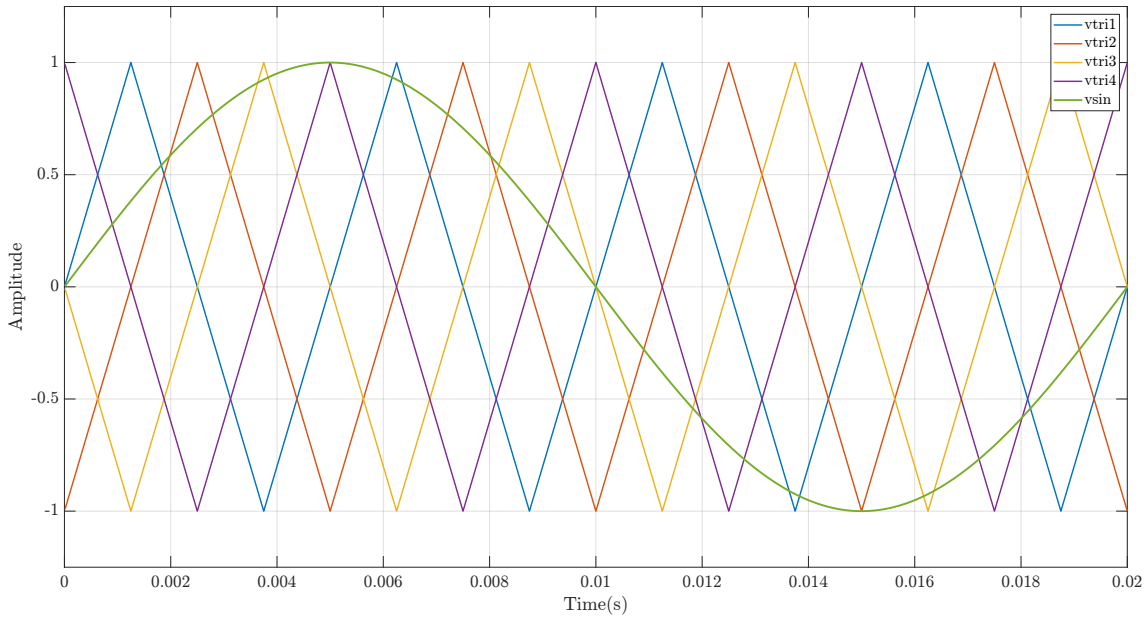


Figure 3.2 – Phase shifted working principle.

The 5LCHBI driven with strategy has been simulated with MATLAB-SIMULINK, the output voltage and current are shown in figure 3.3.

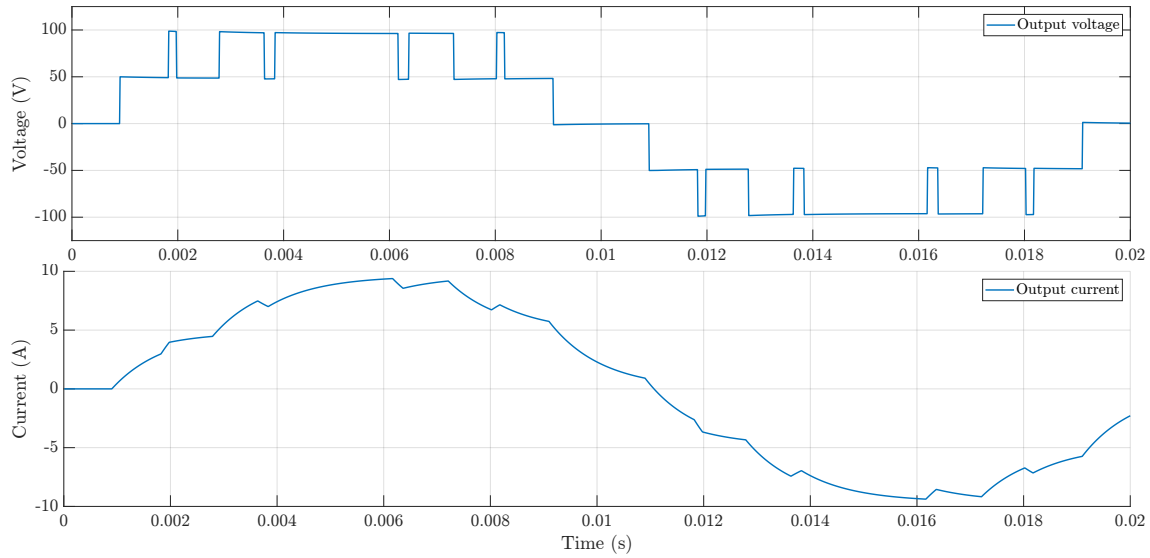


Figure 3.3 – Output voltage and current obtained with PS control strategy.

3.3 Level Shifted Techniques

Similarly to the PS control strategy, four carriers are necessary to drive the 5LCHBI. These signals have the same amplitude, frequency and they are vertically shifted such as the bands they occupy are contiguous [34]. The carriers' characteristics are summarized as it follows:

Table 3.1 – Analysis of the carriers of different level shifted methods.

Name of the carrier	Switches influenced	Carrier range (y axis)
v_{tri1}	T11-T14	[+1 +2]
v_{tri2}	T21-T24	[0 +1]
v_{tri3}	T13-T12	[0 -1]
v_{tri4}	T23-T22	[-1 -2]

Each carrier is associated to a specific voltage level, the switching pulses are generated at the same way as the SPWM principle, the only difference is that v_{sin} is compared with the four carriers. Every single cell is used only when the corresponding voltage level is requested, this leads to an uneven power distribution and switching conditions between the modules. Because of these aspects, the output voltage distortion and the input current distortion increase. The difference between different level shifted method relies in the phase shift angle between the carriers, which set differently depending by the implemented technique, this aspect is shown more in the detail in the following sections.

3.3.1 Phase Disposition Method

In this control strategy, the four carrier are phase shifted by zero degrees, they are only vertically shifted by a unitary value, as it is shown in figure 3.4.

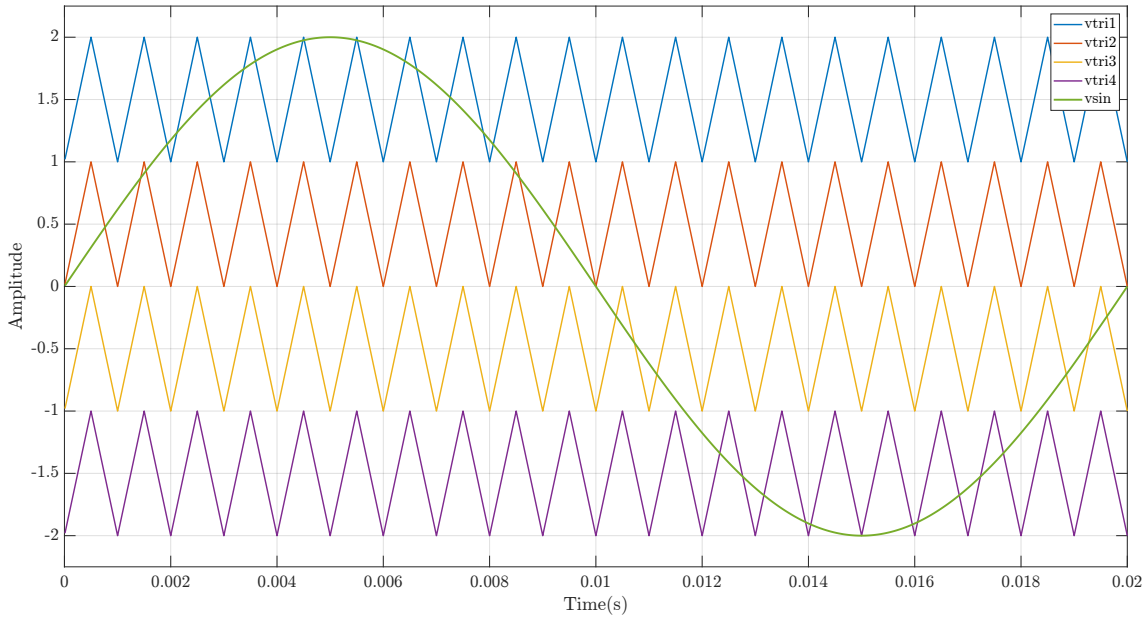


Figure 3.4 – PD working principle.

The output voltage and current obtained with this control strategy are plotted in figure 3.5.

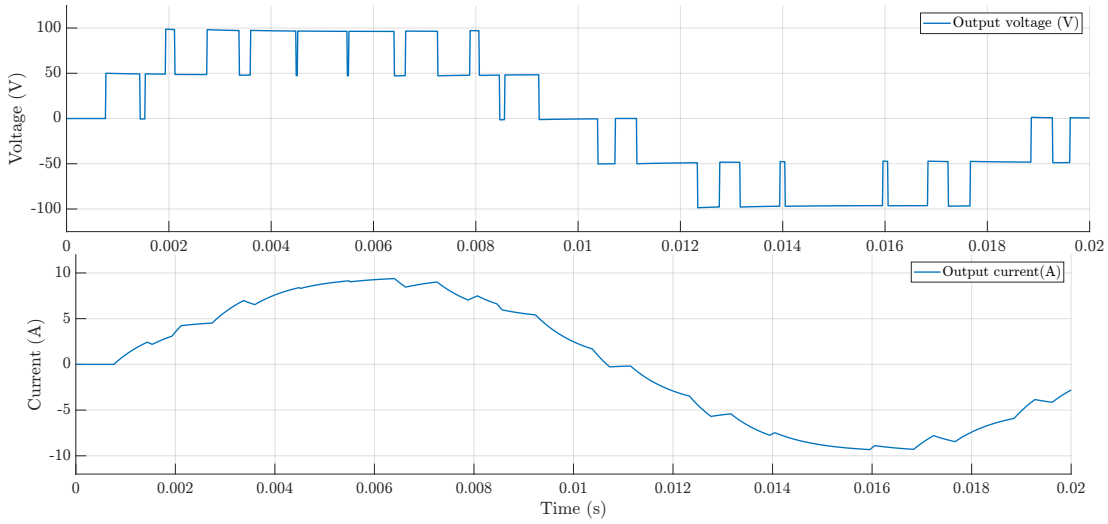


Figure 3.5 – Output voltage and current obtained with PD control strategy.

3.3.2 Phase Opposite Disposition Method

In this control strategy, the carriers v_{tri1} and v_{tri2} i.e., the carriers located in the range [0 +2] have the same phase angle, while the carriers v_{tri3} and v_{tri4} i.e., the carriers located in the range [0 -2] are phase shifted by 180°, consequently they are opposite in phase, as the strategy's name suggests. The POD working principle is shown in the figure 3.6.

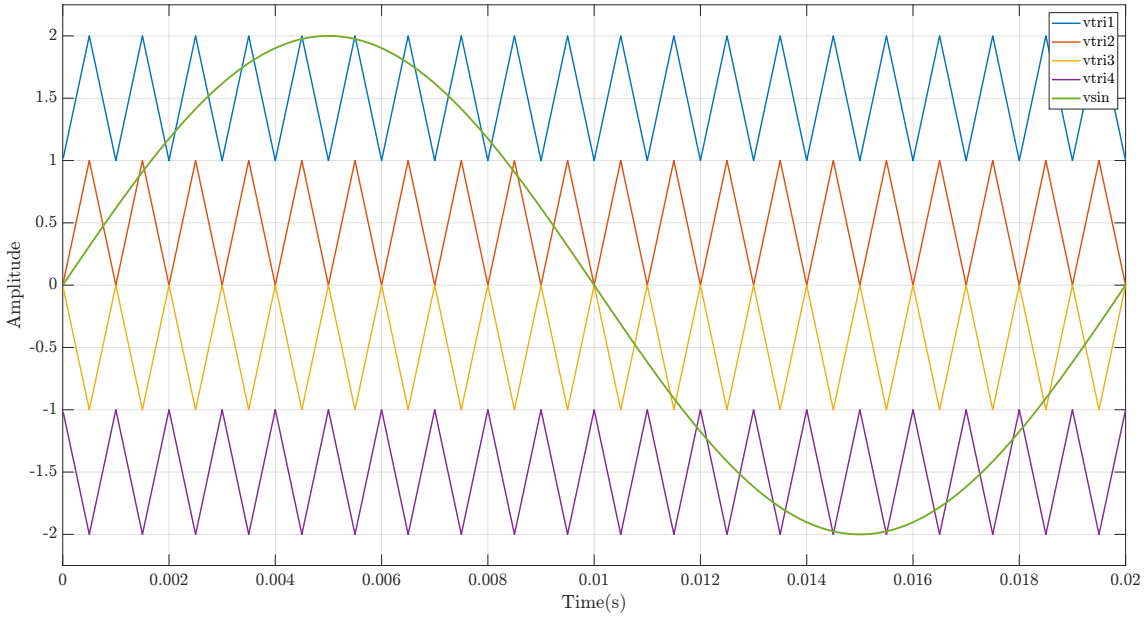


Figure 3.6 – POD working principle.

The output voltage and current obtained with this control strategy are plotted in figure 3.7.

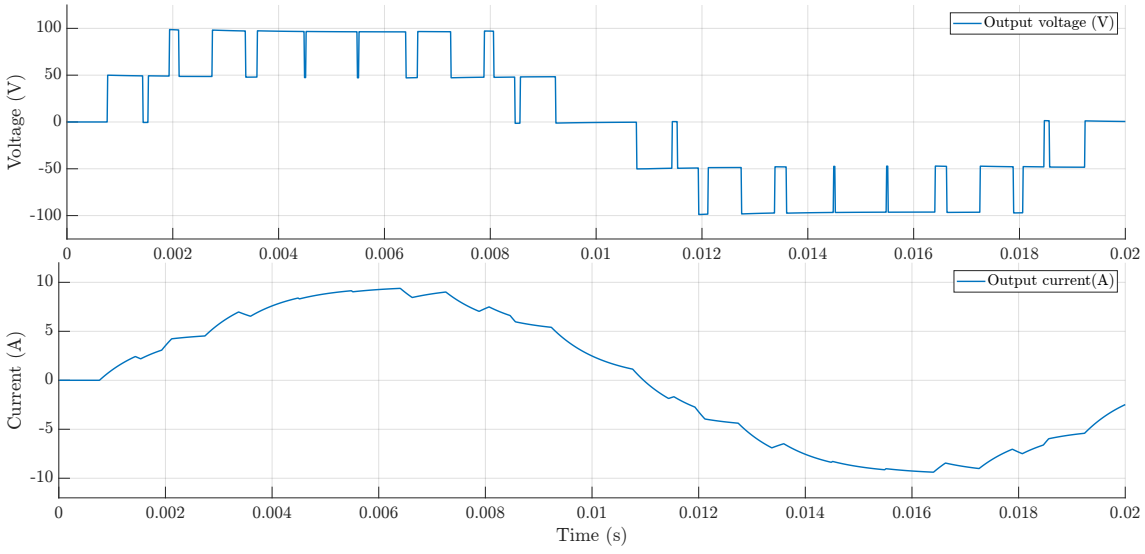


Figure 3.7 – Output voltage and current obtained with POD control strategy.

3.3.3 Alternate Phase Opposite Disposition Method

In this control strategy the adjacent carriers are phase shifted by 180° consequently v_{tri1} is in phase with v_{tri3} and v_{tri2} is in phase with v_{tri4} as shown in figure 3.8.

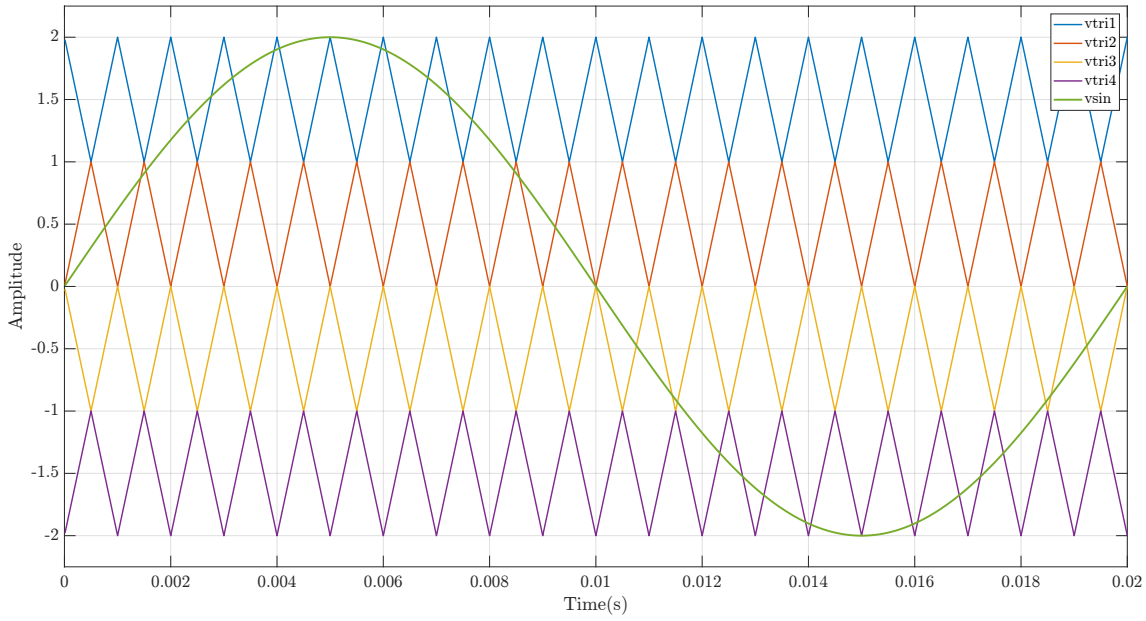


Figure 3.8 – APOD working principle.

The output voltage and current obtained with this control strategy are plotted in figure 3.9.

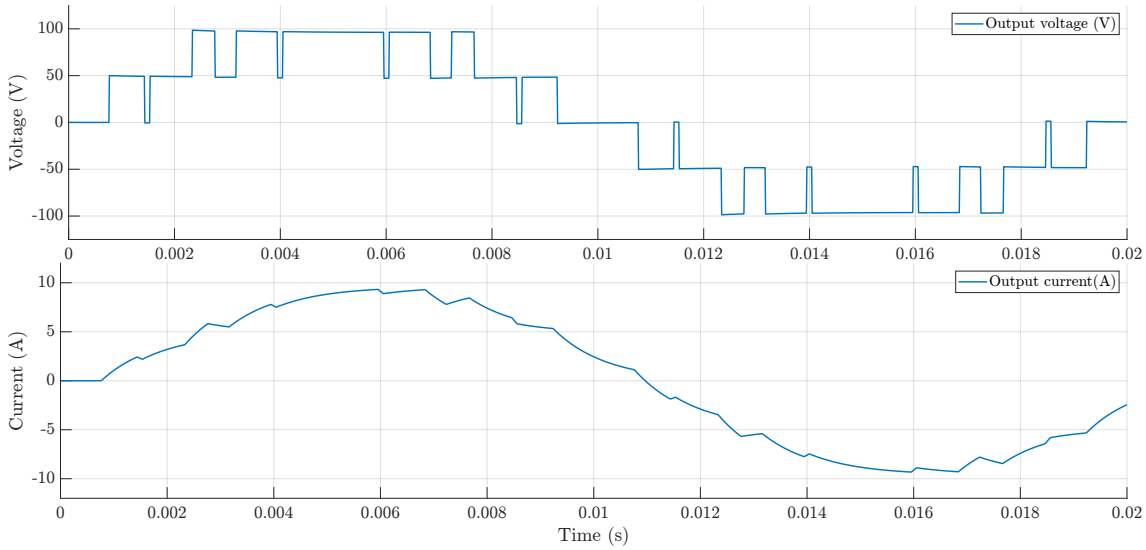


Figure 3.9 – Output voltage and current obtained with APOD control strategy.

3.3.4 Comparison Between Phase and Level Shifted Methods

To compare the performance of phase and level shifted SPWM techniques, different simulations have been conducted on MATLAB-SIMULINK. The same parameters have assumed for performing the simulations and they are summarized in table 3.2, the values have been chosen arbitrarily.

Table 3.2 – Parameters used in the SPWM simulations.

Parameter	Name	Value
Input voltage	V_{dc}	2 x 50 V
Resistive load	R_{load}	10 Ω
Inductive load	L_{load}	10 mH
Switching frequency	f_{s}	1 kHz
Frequency modulation index	m_{f}	20

The parameter m_{a}, responsible for the output wave magnitude and its harmonic content, has been varied between 0.6 and 1.2. V_1 represent the magnitude value of the output voltage's first harmonic. The results are reported in table 3.3.

Table 3.3 – Comparison between SPWM techniques applied to the 5LCHBI.

PD PWM	m_{a}=0.6	m_{a}=0.8	m_{a}=1	m_{a}=1.2
THD_{V}%	44.88	40.39	27.91	22.15
V_1 amplitude (V)	58.02	76.47	98.01	107.7
POD PWM	m_{a}=0.6	m_{a}=0.8	m_{a}=1	m_{a}=1.2
THD_{V}%	45.69	41.02	28.88	23.54
V_1 amplitude (V)	58.65	76.97	97.76	107.8
APOD PWM	m_{a}=0.6	m_{a}=0.8	m_{a}=1	m_a=1.2
THD_{V}%	47.29	41.47	29.91	23.57
V_1 amplitude (V)	56.54	76.86	97.69	107.6
PS PWM	m_{a}=0.6	m_{a}=0.8	m_a=1	m_{a}=1.2
THD_{V}%	45.89	41.04	28.11	22.73
V_1 amplitude (V)	57.61	77.12	98.05	107.8

The results obtained with these simulations are in accord with the data and values available in research papers about this topic [19]. From the table 3.3 it is possible to see that PD method offers the lowest THD_{V}% compared to the other SPWM methods, also a good rms voltage output value is obtained. After the evaluation of the harmonic spectrum of the output signal it is possible to see that the dominant harmonics in PD are present at carrier frequency range while in POD and APOD methods the harmonic content is mainly located lower than the

carrier frequency, making the eventual filtering procedure more complex. The main difference between the PS and the CS methods is that in the first method the conduction time of the switches is evenly distributed. This is no longer held true for the CS methods, in fact, to evenly distribute the switching and conduction losses, the switching pattern should rotate among the inverter sub-modules [36]. Table 3.4 summarizes the comparison between phase and level shifted methods.

Table 3.4 – Comparison between phase and level shifted SPWM methods.

Comparison	Phase Shifted method	Level Shifted methods
THD_{V}	Good	Better
Device conduction period	Same for all devices	Different
Implementation difficulty	Medium	Low
Rotating of switching patterns	Not required	Required

3.4 Multi-band Hysteresis Based Control Method Applied to the 5-level CHB Inverter

A novel control algorithm based on the multi-offset hysteresis technique has been implemented, this is the natural extension of the algorithm explained in 2.7.2. $(n-1)$ hysteresis bands are necessary for driving the inverter with this strategy, where n is the number of the inverter voltage levels thus four hysteresis bands are deployed: $hyst_1$, $hyst_2$, $hyst_3$, $hyst_4$. The block scheme of this principle is shown in figure 3.10.

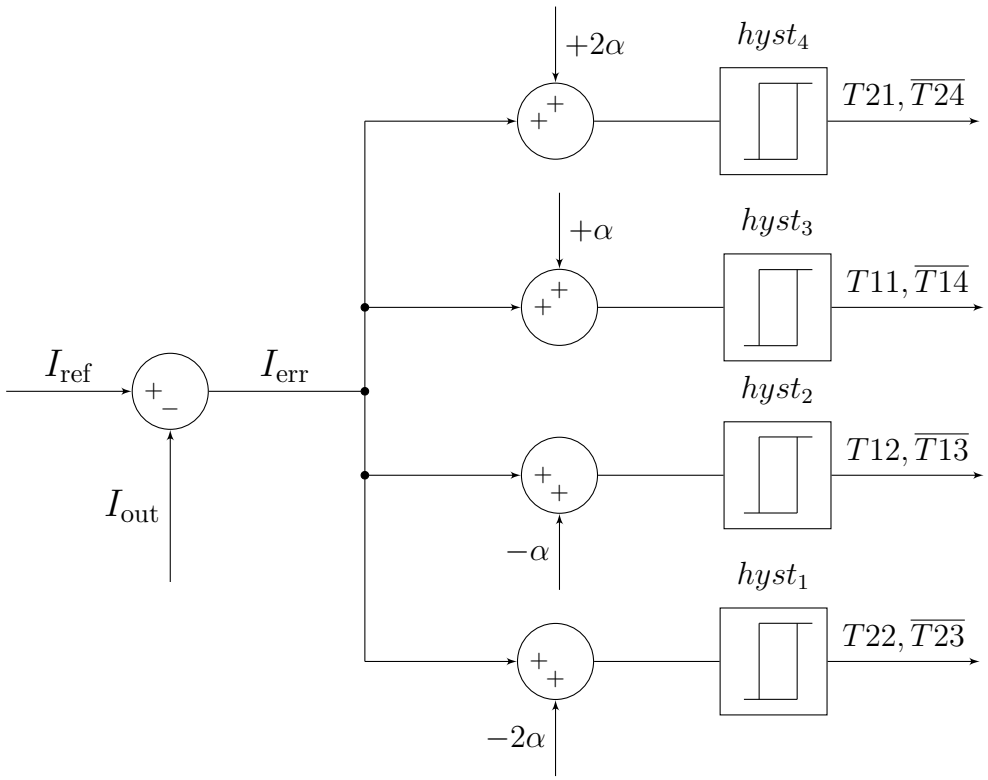


Figure 3.10 – Working principle of the developed multi-band hysteresis control method.

These bands have the same fixed amplitude h, they are vertically shifted by different combination of the parameter α, between the adjacent bands a small gap δ is introduced for avoiding overlaps in the switching pattern. The current error is processed by these hysteresis bands, which generate the necessary switching pulses for having as output the required voltage level.

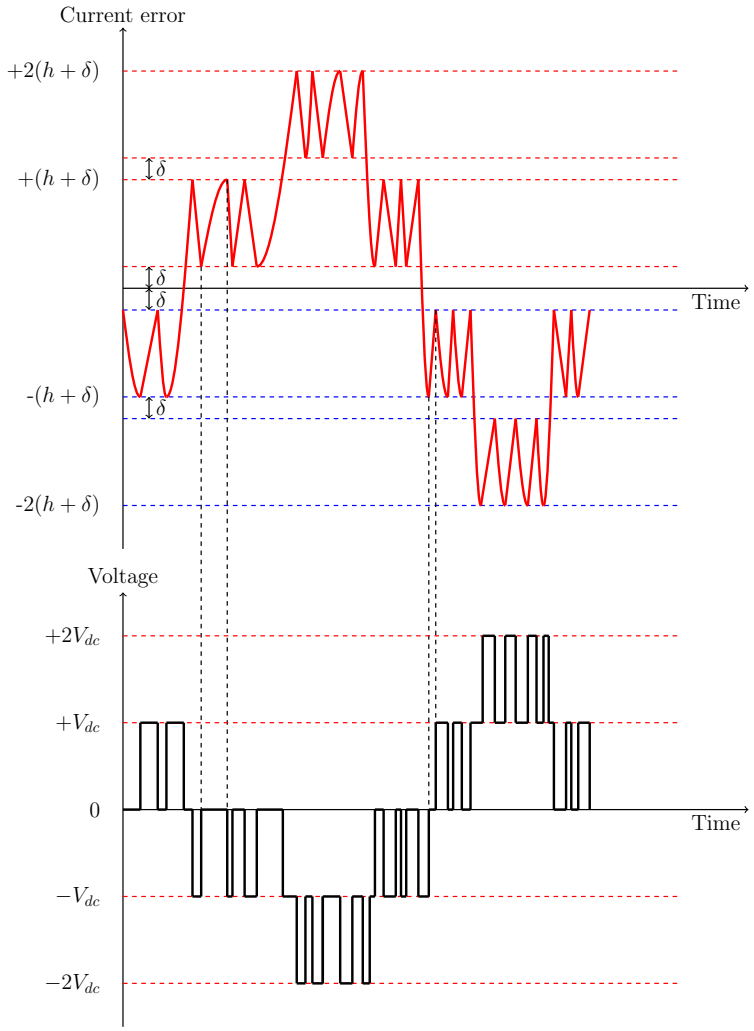


Figure 3.11 – Representation of the MOBHM working principle in the time domain, showing the switching function and the corresponding voltage output.

Figure 3.11, in the superior part, represents the current error and the four different hysteresis bands, shifted by the parameter α and divided by δ. It is possible to see that I_{err} swings between the upper and lower limits of the corresponding band. If the error exceeds these boundaries, I_{err} drives into an adjacent hysteresis band. The lower part of the same figure shows the corresponding voltage value to the current error. The control strategy selects the optimal output voltage value depending by the error magnitude, which is defined by the four hysteresis bands.

The control algorithm of this strategy has been formulated for a consequent implementation in MATLAB-SIMULINK, the algorithm can be divided in two steps:

1. The hysteresis control evaluates the error and generates the switching logic parameter u.
2. The switching pulses are generated based on the evaluation of u.

u is a parameter generated by the control strategy; it represents the switching logic of the inverter. It can assume five different values: -2, -1, 0, +1, +2 and the final output of the inverter can be defined as:

$$V_{\text{out}} = uV_{\text{dc}}$$

The detailed control algorithm for the 5LCHBI based on the MOBHM is described in the following:

Condition 1: if $err > 0$, then

Condition 1.1: if $err > +\delta$, then

$$\begin{cases} u = -1 & \text{for } +(h+\delta) < err < +(h+2\delta) \\ u = 0 & \text{for } err < +\delta \end{cases}$$

Condition 1.2: if $err > +(h+2\delta)$, then

$$\begin{cases} u = -2 & \text{for } err > +2(h+\delta) \\ u = -1 & \text{for } err < +(h+2\delta) \end{cases}$$

Condition 2: if $err < 0$, then

Condition 2.1: if $err <$ -δ, then

$$\begin{cases} u = +1 & \text{for } -(h+\delta) > err > -(h+2\delta) \\ u = 0 & \text{for } err > -\delta \end{cases}$$

Condition 2.2: if $err <$ -$(h+2\delta)$, then

$$\begin{cases} u = +2 & \text{for } err < -2(h+\delta) \\ u = +1 & \text{for } err > -(h+2\delta) \end{cases}$$

The control system should be able to generate the switching pulses depending by parameter u:

Condition 1: if $err > 0$, then

Condition 1.1: if $err > +\delta$, then

$$\begin{cases} T11, T13, T23, T24 = \text{ON} & \text{for } u = -1 \\ & \text{such that } V_{\text{out}} = -V_{\text{dc}} \end{cases}$$

$$\begin{cases} T11, T13, T21, T23 = \text{ON} & \text{for } u = 0 \\ & \text{such that } V_{\text{out}} = 0 \end{cases}$$

Condition 1.2: if $err > +(h + 2\delta)$, then

$$\begin{cases} T13, T14, T23, T24 = \text{ON} & \text{for } u = -2 \\ & \text{such that } V_{\text{out}} = -2V_{\text{dc}} \end{cases}$$

$$\begin{cases} T11, T13, T23, T24 = \text{ON} & \text{for } u = -1 \\ & \text{such that } V_{\text{out}} = -V_{\text{dc}} \end{cases}$$

Condition 2: if $err < 0$, then

Condition 2.1: if $err <$ -δ, then

$$\begin{cases} T11, T12, T21, T23 = \text{ON} & \text{for } u = +1 \\ & \text{such that } V_{\text{out}} = +V_{\text{dc}} \end{cases}$$

$$\begin{cases} T11, T13, T21, T23 = \text{ON} & \text{for } u = 0 \\ & \text{such that } V_{\text{out}} = 0 \end{cases}$$

Condition 2.2: if $err <$ -$(h + 2\delta)$, then

$$\begin{cases} T11, T12, T21, T22 = \text{ON} & \text{for } u = +2 \\ & \text{such that } V_{\text{out}} = +2V_{\text{dc}} \end{cases}$$

$$\begin{cases} T11, T13, T21, T23 = \text{ON} & \text{for } u = +1 \\ & \text{such that } V_{\text{out}} = +V_{\text{dc}} \end{cases}$$

3.4.1 Simulation of the MOBHM Applied to the 5LCHBI

After the theoretical analysis and the mathematical approach, the MOBMH has been implemented in MATLAB-SIMULINK on the 5LCHBI in order to evaluate its performances. This control strategy does not require the knowledge of the load parameters, this can be the main advantage of this control strategy. However, the switching frequency is not controlled and it's not constant during the fundamental period because it acts as a consequence of the input parameters. The simulation parameters are summarized in table 3.5.

Table 3.5 – Parameters used in the MOBHM applied to the 5LCHBI.

Parameter	Name	Value
Input voltage	V_{dc}	2 x 20 V
Resistive load	R_{load}	1 Ω
Inductive load	L_{load}	1 mH
Current reference	I_{ref}	20 A
Anti-overlapping gap	δ	0.01 A
Maximum current error / Band amplitude	h	0.2 A
Shifting between two adjacent bands	α	0.2 A

In this strategy the output voltage is a function of the current, the voltage is modulated by the control strategy to achieve as output the requested output current (current reference). Figure 3.12 and figure 3.13 show the Output voltage and output current waveforms.

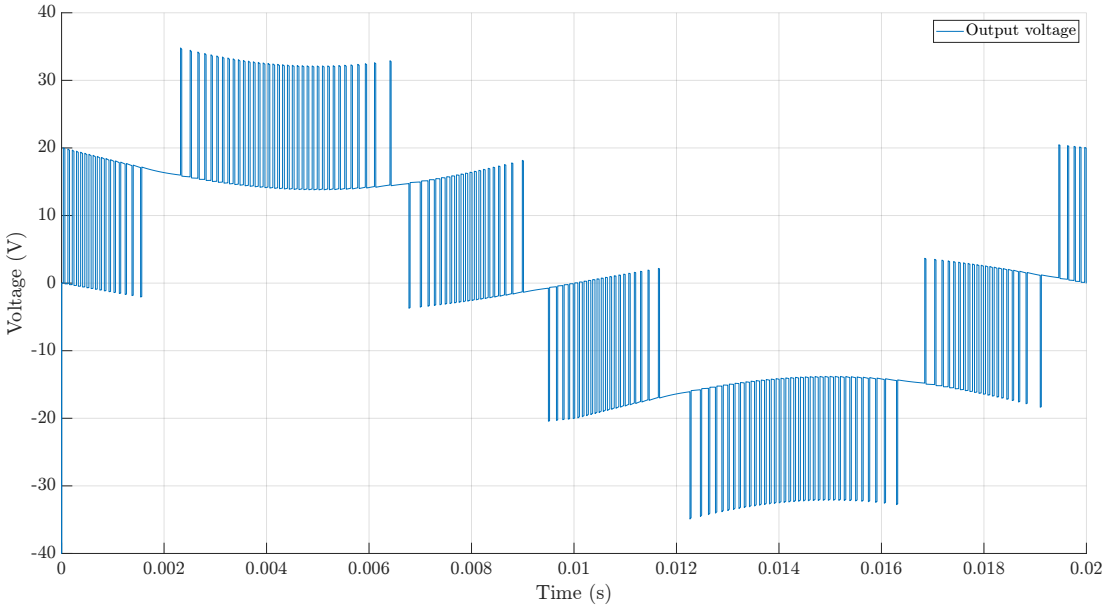


Figure 3.12 – Output voltage obtained with the multi-band hysteresis current control applied on the 5LCHBI.

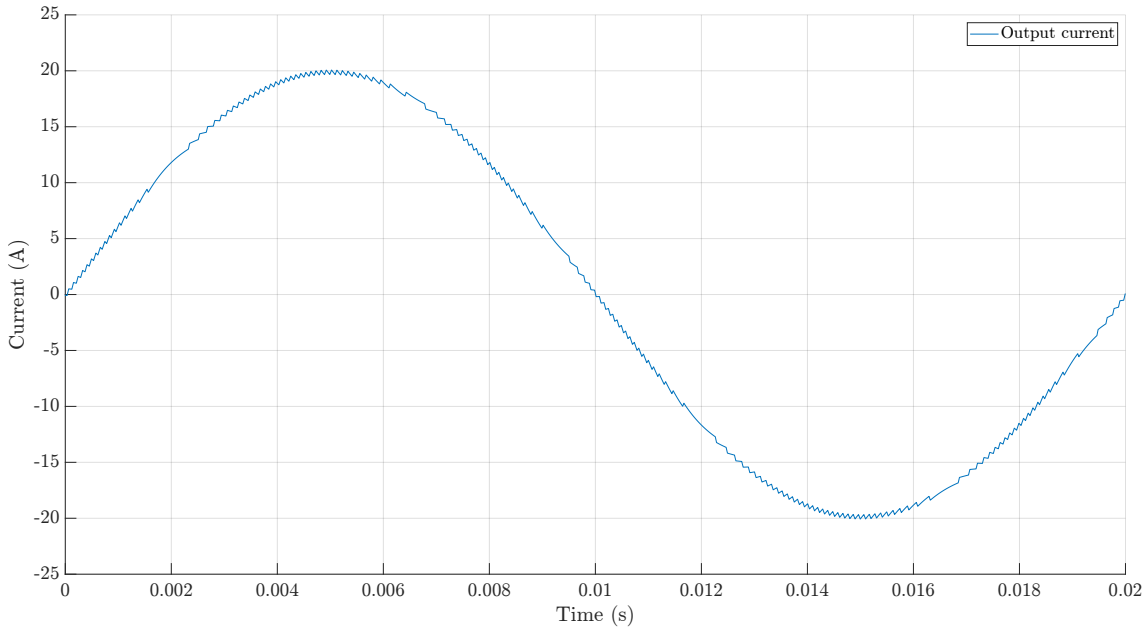


Figure 3.13 – Output current obtained with the multi-band hysteresis current control applied on the 5LCHBI.

It is possible to notice that the current is almost close to a sinewave because the maximum error set in the simulation is relatively small compared to its magnitude. The voltage waveform presents a relatively high harmonic distortion, this is mainly caused by the inductive component of the load that at high frequencies bends the voltage waveform. The magnitude of output voltage, output current and their relative THD are reported in table 3.6.

Table 3.6 – Results obtained with the MOBHM applied to the 5LCHBI.

Parameter	Name	Value
Output current total harmonic distortion	THD_{I}	0.87 %
Output current fundamental magnitude	I_1	19.93 A
Output voltage total harmonic distortion	THD_{V}	50.07 %
Output voltage fundamental magnitude	V_1	20.89 V

3.4.2 Simulations of Dynamic Changes in the System

The fast response and high adaptability of the hysteresis current control is one of the strong points of this technique. The system should be able to adapt when some changes in the load or in the input parameter occur, and at the same time guaranteeing a fast and stable dynamic response. Simulations have been performed to evaluate these aspects, a brief summary will be presented and subsequently the obtained results will be explained and discussed.

Dynamic Change of the Input Reference Current

A dynamic change in the system is introduced at the instant of time t_1=0.037 s, the current reference changes from an initial value of $I_{\text{ref},1}$=10 A to $I_{\text{ref},2}$=10 A. The other parameters of table 3.5 are left untouched. The system should adapt to this perturbation as fast as possible and guaranteeing at the same time a stable transient. Figure 3.14 shows the current and voltage behavior. The simulation has been performed on a total time t_{tot}=0.06 s equivalent to three fundamental periods.

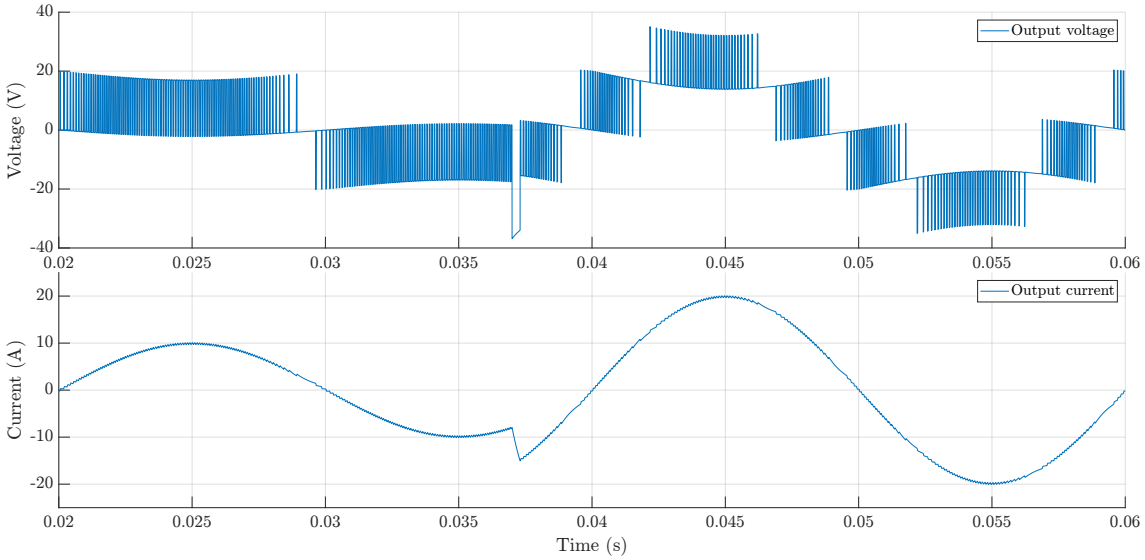


Figure 3.14 – Output voltage and current waveforms obtained in the simulation of the system dynamic perturbation.

It is possible to see in figure 3.14 that at t_1 the current perturbation has been introduced. A feature of this his control strategy is the capability to select the optimal number of output voltage levels, to better satisfy the input conditions. It is possible to see that before t_1, a two-level output voltage was enough to produce the desired current, however, to produce the new requested value, after t_1, the controller applies all the five voltage levels available. This is another difference compared to the SPWM methods, in which always a five-level voltage output is generated. It is possible to notice that about 2 µs are necessary for the controller to follow the new current reference, confirming the fact that the hysteresis current method has a fast and stable response even if the system is subjected to disturbances and dynamic changes.

3.5 Voltage Control Strategy Applied to the 5-level CHB Inverter

In the previous section a current control strategy applied to the 5LCHBI has been simulated and analyzed. However, there is a wide range of electrical applications that require voltage source inverters; for this reason and for expanding the analysis about the control strategies, a voltage control closed-loop method applied to the 5LCHBI is presented, analyzed and simulated.

This control strategy has been developed according to these steps:

1. The **voltage closed-loop control strategy** has been applied to the system composed by the 5LCHBI and a generic R-L load.
2. In order improve the quality of the output waveform, an **output filtering procedure** has been implemented.
3. The **voltage closed-loop control strategy** has been applied to the system composed by the 5LCHBI and the output filter.
4. Subsequently **some simulations have been performed** on MATLAB-SIMULINK to evaluate the strategy, to compare the output with and without filter and to analyze the behave of the system if affected by dynamic changes in its input and output.

This technique relies on a multiloop PI architecture, to understand better its working principle, some basic information regarding this topic are presented.

3.5.1 Overview on Controllers

Proportional (P), Proportional Integral (PI) and Proportional Integral Derivative (PID) controllers have been widely used in control engineering applications for a lot of decades. However, in this work only the PI controller will be discussed and implemented in the control strategy. The PI controller produces an output, which is the combination of the proportional and the integral controllers [26]:

$$u(t) = K_{\mathrm{P}} e(t) + K_{\mathrm{I}} \int e(t)\, dt \tag{3.2}$$

it is possible to apply the Laplace transform on both sides:

$$U(s) = \left(K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{\mathrm{s}} \right) E(\mathrm{s}) \tag{3.3}$$

thus:

$$\frac{U(\mathrm{s})}{E(\mathrm{s})} = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{\mathrm{s}} \tag{3.4}$$

Therefore, the transfer function of the PI controller is:

$$K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{\mathrm{s}} \tag{3.5}$$

K_{P} that stands for the proportional gain, K_{I} is the integral constant, $E(\mathrm{s})$ is the controller input and $U(\mathrm{s})$ is the controller output. Figure 3.15 shows the block diagram of the negative feedback closed-loop system in which the PI controller is applied. $Y(\mathrm{s})$ is the closed-loop measured value and $R(\mathrm{s})$ represents the desired value which is sent as input to the closed-loop.

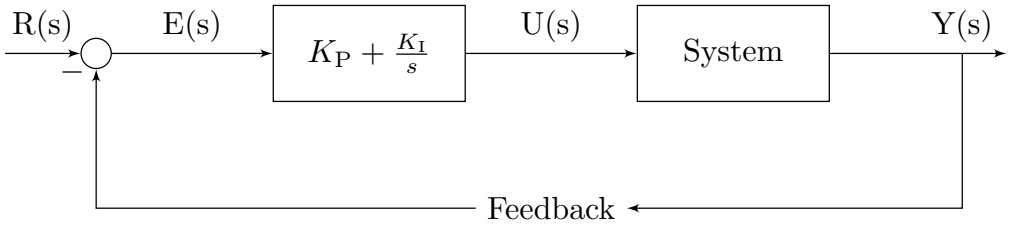


Figure 3.15 – Block diagram of closed-loop system along with the PI controller.

If $K_{\mathrm{I}} = \infty$ (a P controller is obtained), the closed-loop measured value $Y(\mathrm{s})$ will always be less than the desired value R(s). The introduction of the integral action helps achieving the equality between the measured value and the desired value, as a constant error produces an increasing controller output. After these considerations it is possible to say that the PI controller allows contributions from the present and the past time [22].

3.5.2 The Voltage Control Strategy

The voltage control strategy that has been implemented consists in a double loop feedback strategy based on a inner loop and an outer loop, in each of these loops there is a PI controller. The algorithm of this control strategy can be described as follows:

1. The voltage reference V_{ref}, which is the input parameter, is compared with the inverter's output voltage V_{ab}, an error is produced. This error is processed by a first PI controller, which generates the current reference I_{ref} for the inner loop.
2. The current reference, produced by the outer loop, is compared with the inverter output current I_{out} and a second error is generated. This error is processed by a second PI controlled, which generates a signal control v_{cont}.
3. The signal control, generated by the inner loop, is used in a SPMW process to be compared with four carriers in order to generate the switching pulses to drive the inverter. The carriers are arranged according to the PD strategy, which was seen previously that it's the MCPWM technique that produces the best quality output. Instead of having a constant and set reference signal, as it was in the PD open-loop strategy, the voltage reference now is produced by the control strategy.

Figure 3.16 shows the block diagram of the control strategy.

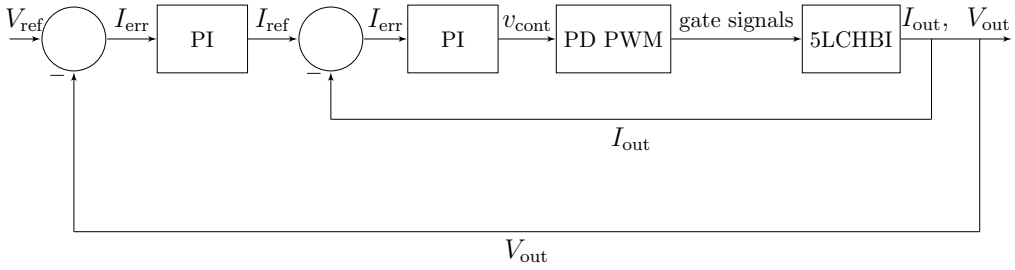


Figure 3.16 – Block diagram of dual loop PI voltage control.

The stability of the system is determined by the study of the transfer function of the system, in this way it is possible to tune the two PI controllers. To obtain the proportional and integral constants K_{I} and K_{P}, necessary for the PI controllers to operate, the two loops are studied independently. In first the PI controller of the inner loop will be tuned and secondly the PI of the outer loop. The PI controllers can be tuned using several methods for example using Ziegler-Nichols method, pole placement or frequency response [6]. For simplicity SISOTOOL from MATLAB-SIMULINK has been used to tune the controllers.

3.5.3 Simulation of the Voltage Control Strategy

For evaluating this strategy some simulations have been performed on MATLAB-SIMULINK. The control system is designed for a non-linear load (R-L), the simulation parameters are chosen arbitrarily, and they are as given in table 3.7.

Table 3.7 – Parameters used in the voltage control strategy applied to the 5LCHBI.

Parameter	Name	Value
Input voltage	V_{dc}	2x30 V
Resistive load	R_{load}	10 Ω
Inductive load	L_{load}	10 mH
Voltage reference	V_{ref}	45 V
Switching frequency	f_{s}	10 kHz
Outer loop PI proportional constant	K_{PO}	0.3
Outer loop PI integral constant	K_{IO}	1015.6
Inner loop PI proportional constant	K_{PI}	11.7
Inner loop PI integral constant	K_{II}	17722

The switching frequency f_{s} is a parameter requested by the controller; this is an advantage of this control technique because it is possible to set this parameter to not exceed the maximum switching speed or to contain the switching losses. A back draw of this strategy is the requirement of the load parameters knowledge, which is necessary create the state-model of the system, necessary to tune the PI controllers. However, once this procedure is done, if

the load is not changed drastically, the system guarantees appreciable results even in case of system dynamic changes or perturbations, as it will be analyzed in the next sections. Figures 3.17 and 3.18 show the output voltage and current obtained with the dual loop PI voltage control strategy applied to the 5LCHBI.

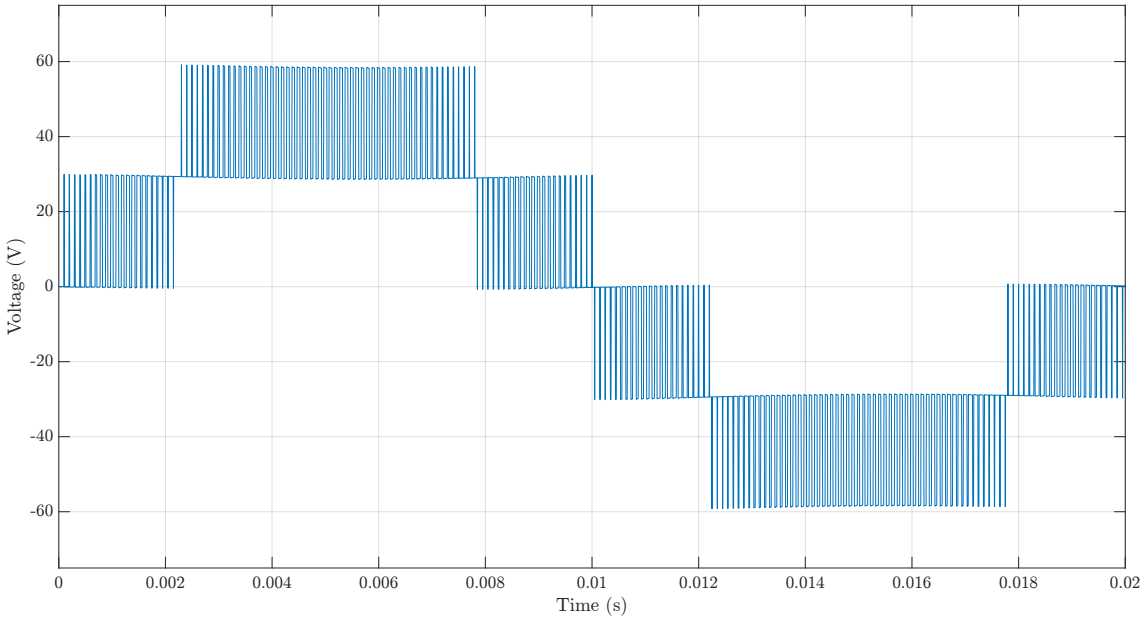


Figure 3.17 – Output voltage obtained with the dual loop PI control strategy.

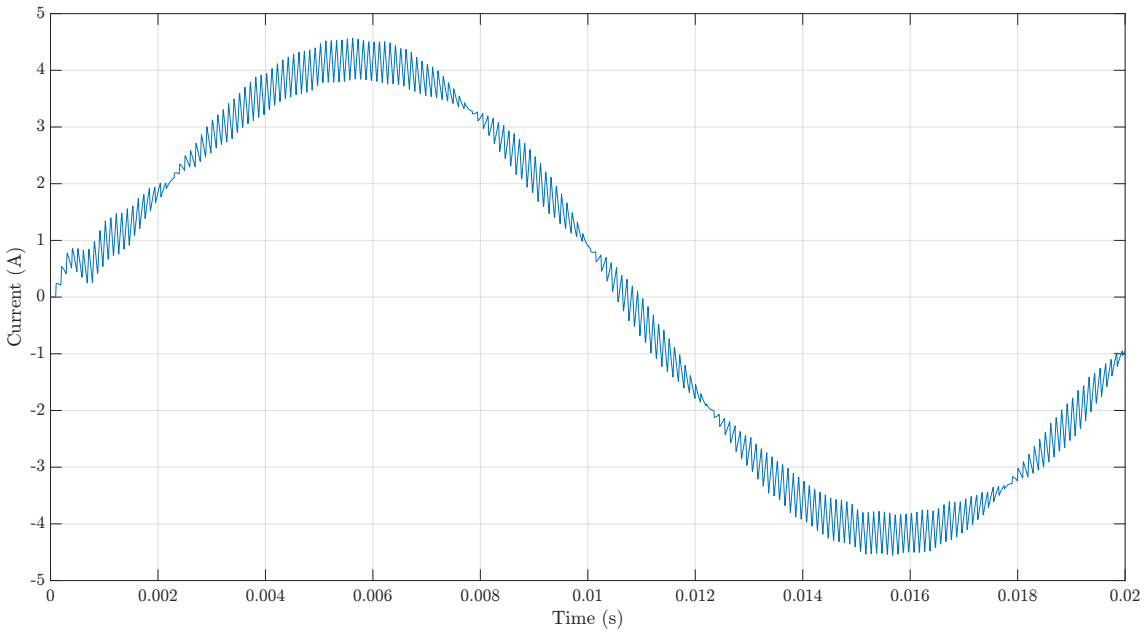


Figure 3.18 – Output current obtained with the dual loop PI control strategy.

The control strategy, without any filtering is able to give as output relatively good quality current and voltage. It is possible to see in the current plot, approximately at t=0.001 s a small perturbation due to the response time of the control strategy. The magnitude value and the THD values of the output and voltage current are shown in table 3.8.

Table 3.8 – Results obtained with the dual loop PI voltage control applied to the 5LCHBI.

Parameter	Name	Value
Output current total harmonic distortion	THD_{I}	5.98 %
Output current fundamental magnitude	I_1	4.12 A
Output voltage total harmonic distortion	THD_{V}	43.86 %
Output voltage fundamental magnitude	V_1	44.9 V

It has to be noticed that the current shows a smaller THD compared the voltage one because of the inductive component of the load. The load itself acts as a load, this phenomena can be seen as well when feeding electric motors, where the inductive components of the windings act as filters, smoothing the current.

3.5.4 Switching Pulses Generation in the Dual PI Loop Voltage Control Strategy

The switching pulses generation process requires to be seen more in the detail. The control strategy is not able alone to generate the switching pulses to drive the inverter. In fact, the control technique, starting from the input voltage, only produces a voltage reference, this signal that can be used to implement a switching pulses generation process based on a PD-SPWM technique. As explained in the previous sections, the aim of the PI controller is to calculate an error between a desired reference ad a feedback input and subsequently applying a correction based on a proportional and integral term. It is possible to use the signal produced by the control strategy, which is a voltage reference, scaled it by a factor K_{PWM} to be used as input of a PD-SPWM process, as reference voltage signal. It is possible to define K_{PWM} as it follows:

$$K_{\mathrm{PWM}} = \frac{1}{V_{\mathrm{dc,tot}}}$$

where $V_{\mathrm{dc,tot}}$ represents the value of the highest voltage value obtainable by the inverter. In the specific, considering a 5LCHBI, this value is obtained from the addition of the DC input sources values. For example, in the simulation that has been performed, K_{PWM} was obtained in the following way:

$$K_{\mathrm{PWM}} = \frac{1}{V_{\mathrm{dc,tot}}} = \frac{1}{V_{\mathrm{dc}} + V_{\mathrm{dc}}} = \frac{1}{30 + 30} = \frac{1}{60} \tag{3.6}$$

In this way, it is possible to scale the output voltage generated by the control strategy to make it usable by the PD-SPWM technique.

The block scheme of this process is shown in figure 3.19.

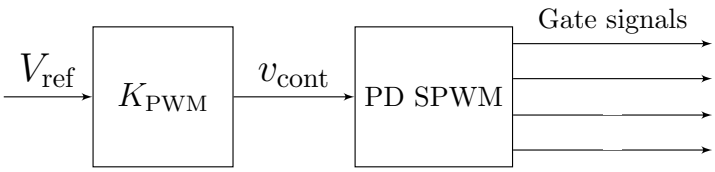


Figure 3.19 – Switching signals generation process.

Is it possible to see more in the detail how the switching signals are generated, the principle, as aforementioned, is based on the PD-SPWM. Four carriers are deployed in the same way as it was described in subsection 3.3.1 The switching pulses are generated from the comparison between the four triangular carriers and v_{cont}, which it's the output of the dual PI loop control strategy. This signal, is not constant in amplitude as was v_{sin}, used in the traditional PD-SPWM, but it's variable, depending by the control strategy.

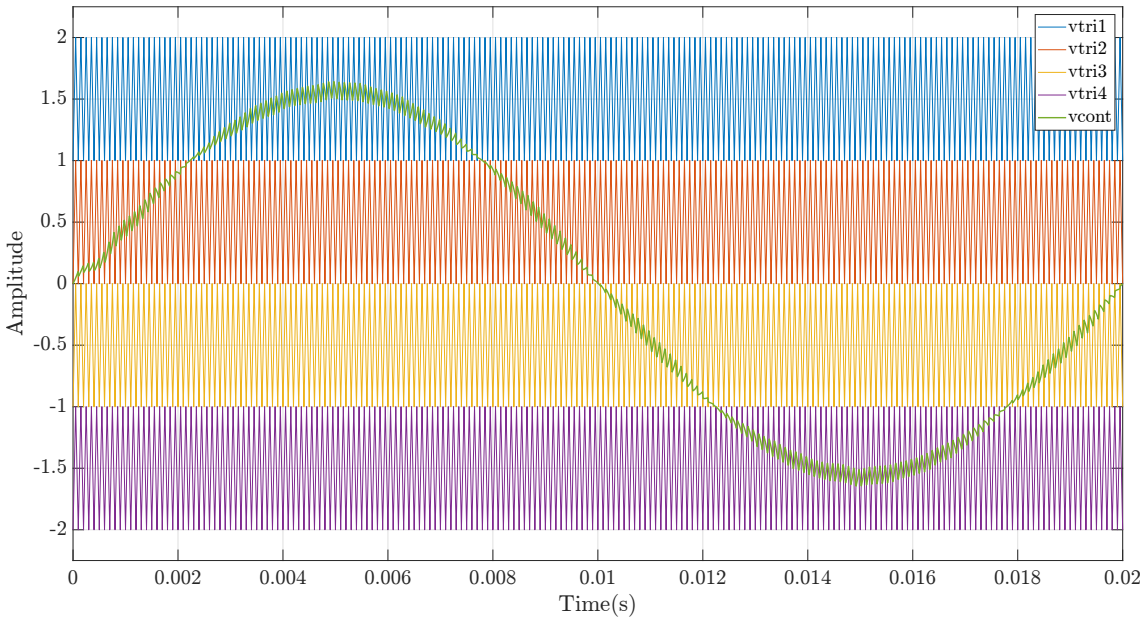


Figure 3.20 – Working principle of the PD-SPWM based method applied to the dual loop PI voltage control strategy.

To see clearly this principle, a detail of 3.20 is shown in the figure 3.21. It is possible to see that between one carrier switching period and the other, the control strategy changes V_{cont} in order to correct and to compensate better the error.

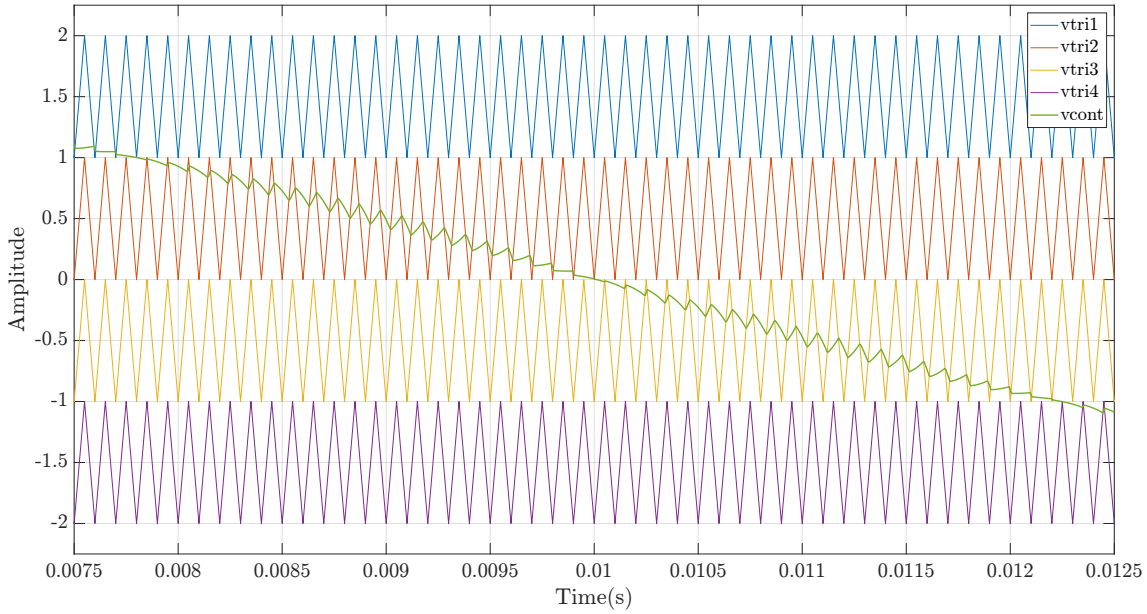


Figure 3.21 – Detail of the working principle of the dual loop PI voltage control strategy.

3.5.5 Output Filtering Procedure

The selected control strategy relies on the PD-SPWM technique for the generation of the switching pulses. As it was described in the previous sections, driving inverters with SPWM based methods brings at having distorted output voltages, these waveforms, consisting in sharp-edged voltage pulses may cause excessive stress in the load. If, for example, the inverter is feeding an electric motor, these distorted voltage waveforms can stress its stator windings insulations [28]. In order to overcome these problems, it is possible to use an inverter output filter, that helps achieving an output waveform closer to a sinewave, for this reason these filters also known as sine-wave filters.
A lot of studies have been conducted on the optimal way to filter the output of an inverter [37], it is shown in the literature that the LC filter is the most effective filter to reduce the harmonics generated by the pulsing modulating control strategies. For this reason, this low-pass filter has been applied to the system.

The filter it is composed by an inductance L connected in series to the output of the inverter, and a capacitance C connected in parallel. The new output terminals a and b of the inverter corresponds to the terminals of the filter's capacitor. The 5LCHBI and its L-C filter are shown in figure 3.22, R_{L} and R_{C} are the internal resistances of the inductor and the capacitor, which must be taken in consideration during the filter dimensioning process.

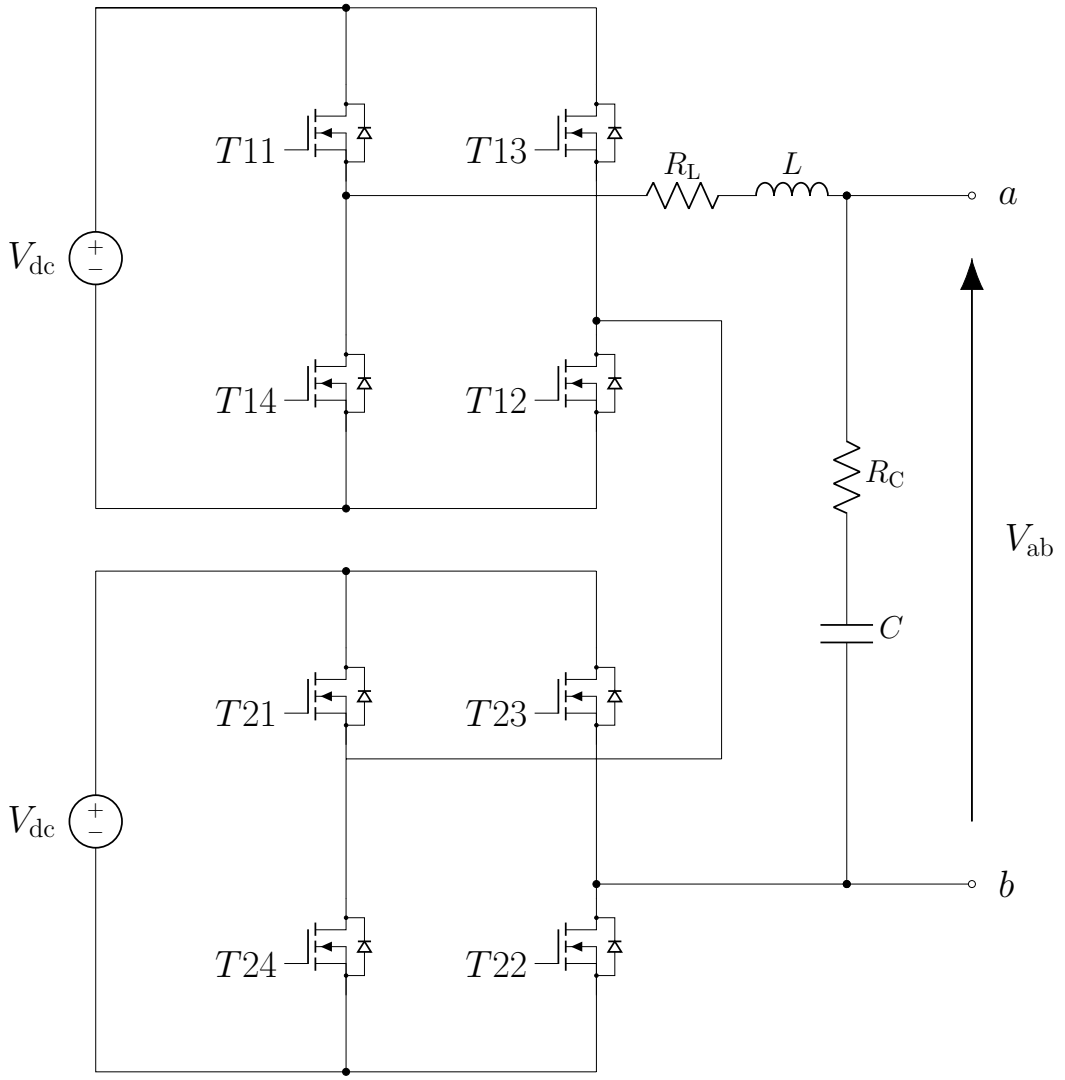


Figure 3.22 – Scheme of the 5LCHBI and the additional L-C filter.

The inductance L blocks high frequency currents and allows lower frequency currents to pass. Conversely the capacitor C allows to pass high frequency voltages blocking low frequencies voltages. Combining these two properties it is possible to remove from the output signals undesired high frequency components, generated by the SPWM [17].

To apply the L-C filter to the inverter, it is necessary to dimension the inductance and the capacitance independently from the control strategy. The dimensioning algorithm is the following:

1. The inductance L will be dimensioned according to the **maximum current ripple method**:
$$L = \frac{T_s}{2}\frac{V_{max}}{2}\frac{1}{\Delta I_{max}} \tag{3.7}$$
T_s is the switching period, V_{max} is the maximum voltage value available as output and ΔI_{max} is the maximum output current ripple allowable as output. The maximum current ripple value has been chosen arbitrarily and it is equal to ΔI_{max}=2 A It is possible to substitute the values in the equation 3.7 with the parameters available in table 3.7, this brings at having:
   - L =7.5 mH that later has been approximated to 1 mH.
   - R_L =0.1 mΩ, this value has been selected as a possible plausible internal resistance for the filter inductance.
2. Once the inductance value has been set, it is possible to choose the size of the capacitor, according to the **cut off frequency method**:
It is possible to set the cut off frequency of the filter as it follows:
$$F_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.8}$$
F_c represents the cut-off frequency, defined as the filtering system's frequency response in which the energy flowing through the system begins to be attenuated. This value can be set according to the maximum harmonic order that is allowable in the output voltage. F_c has be set arbitrarily and it is equal to:
$$F_c \leqslant \frac{f_s}{10} \tag{3.9}$$
Where f_s is the switching frequency, this brings at having F_c=1 kHz.
It is possible to reorganize the equation 3.8 to emphasize the capacitor as it follows:
$$C = \left(\frac{10}{2\pi f_s}\right)^2 \frac{1}{L} \tag{3.10}$$
This brings at having:
   - C =0.033 75 µF
   - R_c =0.01 mΩ, this value has been selected as a possible plausible internal resistance for the filter capacitor.

It is necessary to include the filter in the system in order to apply the dual PI loop voltage control strategy. The L-C circuit is introduced in the block scheme of figure 3.16 and subsequently the PI controllers are tuned. The new control strategy loops will be shown separately, in figure 3.23 the outer and in 3.24 the inner.

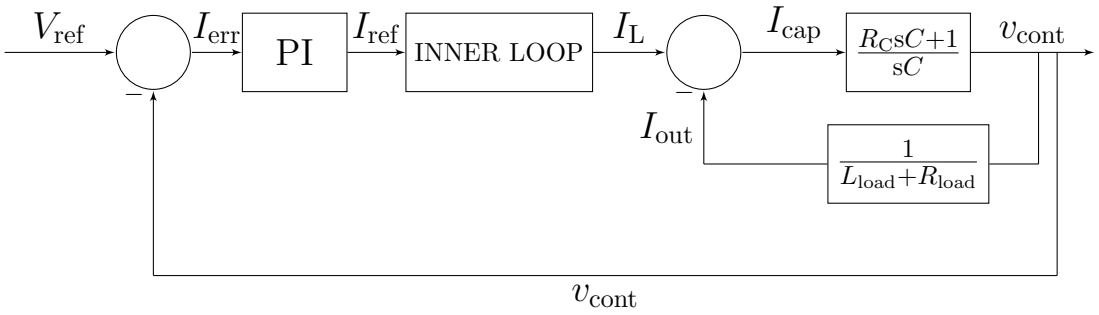


Figure 3.23 – Block scheme of the outer loop after the introduction of the LC filter in the system.

I_{L} represent the current which is flowing through the filter's inductor, I_{C} is the current which flows through the filter's capacitor and I_{out} is the output current, which goes to the load.

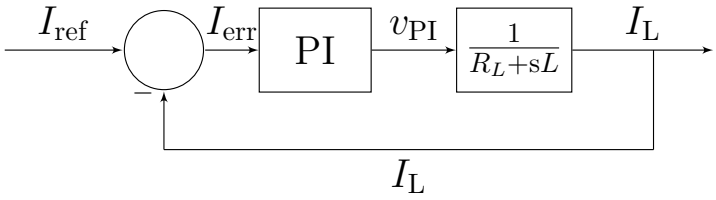


Figure 3.24 – Block scheme of the inner loop after the introduction of the LC filter in the system.

Is it possible now to tune the PI controllers using the same procedure illustrated in subsection 3.5.2.

To evaluate the performances of the voltage control strategy applied to the system composed by the 5LCHBI and the filter some simulations have been performed in MATLAB-SIMULINK. The results to be expected are a reduction of the output voltage and current total harmonic distortion. Figure 3.25 and 3.26 show the output waveforms.

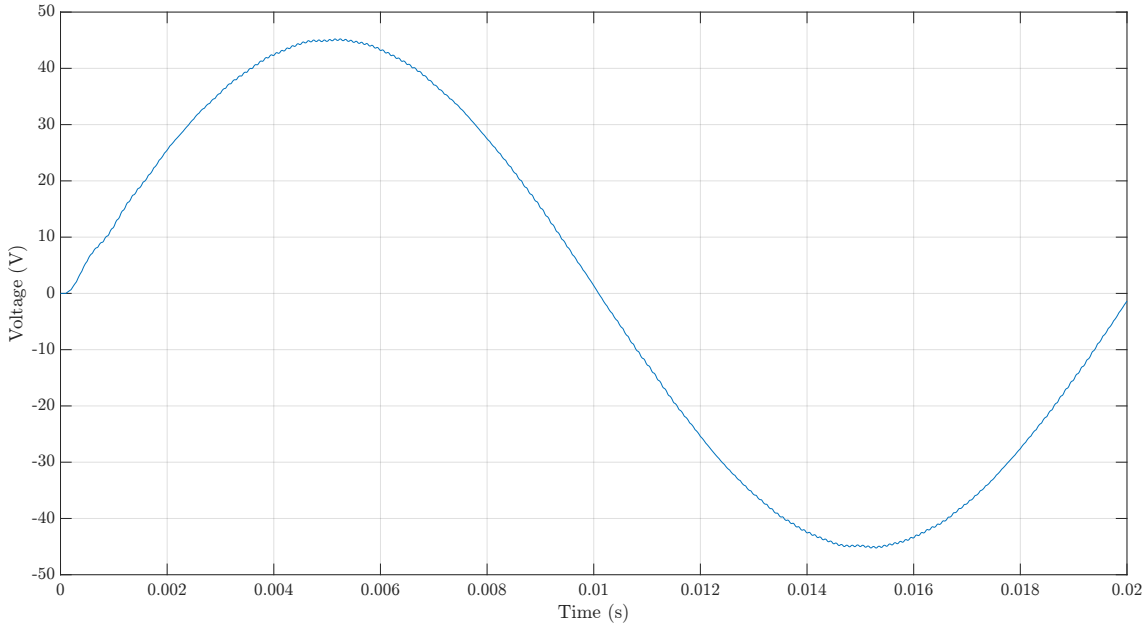


Figure 3.25 – Output voltage obtained with the dual loop PI control strategy after the introduction of the L-C filter.

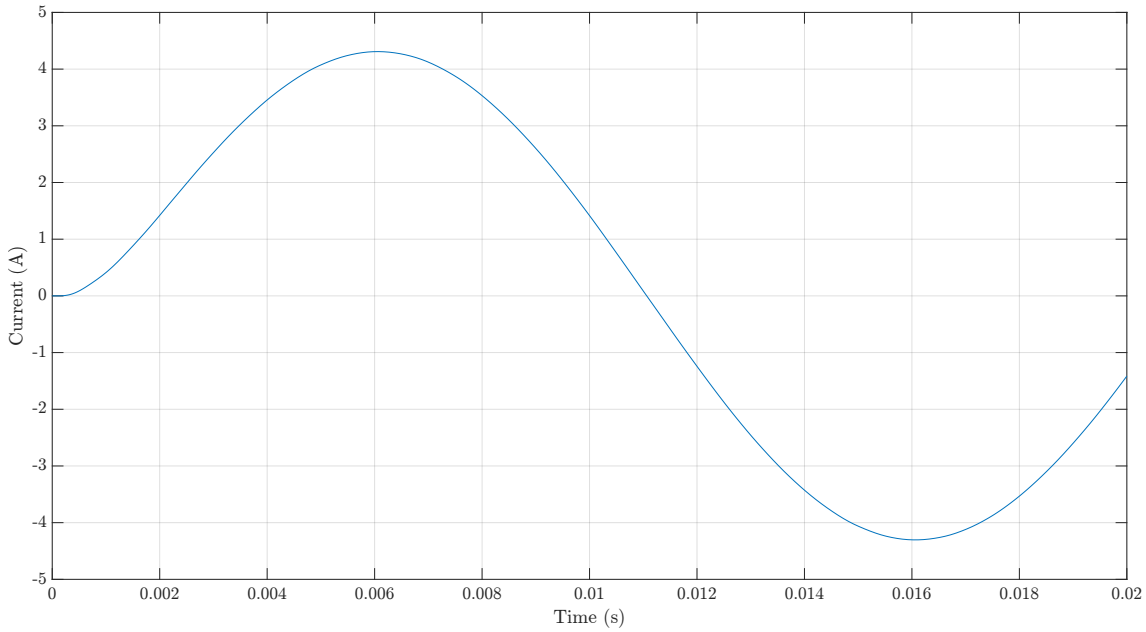


Figure 3.26 – Output current obtained with the dual loop PI control strategy after the introduction of the L-C filter.

The result obtained are satisfactory, the quality of the waveform improved, and the control strategy shows a quick response and a good stability. It is possible to notice a small waveform in the current and voltage approximately at t=0.001 s but this deficiency is compensated after some milliseconds.

Table 3.9 reports the magnitude and the THD values of output voltage and current.

Table 3.9 – Results obtained with the dual loop PI voltage control after the addition of the output filter.

Parameter	Name	Value
Output current total harmonic distortion	THD_{I}	0.05 %
Output current fundamental magnitude	I_1	4.302 A
Output voltage total harmonic distortion	THD_{V}	0.17 %
Output voltage fundamental magnitude	V_1	45.09 V

3.5.6 The Single Phase of the Permanent Magnet Synchronous Motor

As aforementioned, the final application of the inverter is feeding a single phase of a permanent magnet synchronous motor. At this point is interesting analyzing the simulations that have been conducted on the device connected to a load that simulates a single phase of a PMSM. Before this it is important to give some knowledge about the machine and more in the specifically about one of its phases. The single of phase of a PMSM it is composed by a resistance R, an inductance L and a back electro-motive force v_{s}. As previously mentioned, due to the early stage of the project, the analysis that has been conducted treated the single phase of a PMSM as a single phase PMSM. Due to the simplicity of the test realized, these assumptions are valid and consistent to carry out the simulations. Next figure shows the equivalent circuit for a single phase of a PMSM.

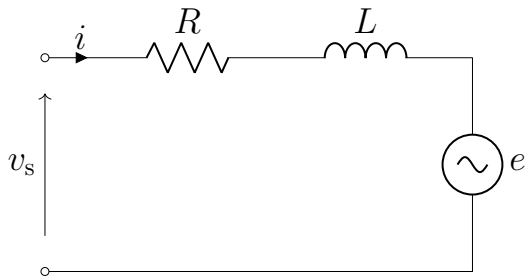


Figure 3.27 – Circuit of a PMSM single phase.

Is it possible to write the motor voltage equations:

$$v_{\mathrm{s}} = Ri + L\frac{\mathrm{d}i}{\mathrm{d}t} + e \tag{3.11}$$

and

$$v_{\mathrm{s}} = V_{\mathrm{m}} \sin(\omega_{\mathrm{s}} t + \varepsilon) \tag{3.12}$$

where [10]:

- v_s is the supply voltage.
- i is the instantaneous motor current.
- R is the resistance of the windings.
- L is the inductance of the windings.
- e is the back-electromotive force (BEMF).
- ω_s is the angular frequency of the supply voltage.
- ε is the angle of the supply voltage.

The Back electro-motive force (BEMF) is:

$$e = k_e \omega_e \sin(\theta_e) \tag{3.13}$$

where:

- ω_e is the rotor electrical angular velocity.
- θ_e is the rotor electrical angle.
- k_e is the BEMF constant.

It is possible now to write the electric torque equations:

$$T_e = i\Psi \sin(\theta_e) \tag{3.14}$$

and

$$\Psi_m = \frac{k_e}{p} \tag{3.15}$$

where:

- T_e is the electric torque.
- Ψ_m is the permanent magnet flux linkage.
- p is the number of pole pairs.

It is interesting performing some simulations simulating dynamic changes that can occur when driving an electrical machine, such variations can mean a different demand of speed and torque. From equations 3.13 and 3.14 it is possible to notice that the BEMF e and the absorbed current i are respectively proportional to the rotor electrical angular velocity ω_e and the electric torque T_e. It is possible to simulate these conditions introducing in the system dynamic changes in output current and input voltage reference values. Due to the early stage of this work, it is not possible to retrieve every motor parameter from the equations in order to build a close-to-reality motor phase, however the simulation parameters have been chosen to make evident the dynamic changes and the system responses to these variations.

3.5.7 Simulations of Dynamic Changes in the System

To test the response and adaptability of the control technique, some dynamic changes in the system composed by R, L, and the BEMF. It is possible to summarize the conducted tests as it follows:

1. In the first test a **dynamic change of the input reference voltage** is simulated, this means that a different rotor speed is requested. The system should adapt to this perturbation giving as output the new requested voltage value (new rotor speed value).
2. In the second test a dynamic **change of the load is simulated**, a different load means a modification in the current output value which translates in a different motor electric torque, according to equation 3.14. The system should adapt giving the same output voltage (same speed) despite the different load condition.

Dynamic Change of the Input Reference Voltage

A dynamic change in the system is introduced at time t_1=0.035 s, the voltage reference changes from $V_{\text{ref},1}$=30 V to $V_{\text{ref},2}$=30 V, the other simulation parameter are left the same as shown in table 3.7 The result that has to be expected is a fast and stable response to the perturbation, the system should react and give as output the new voltage reference in less time as possible while guaranteeing the stability. The result obtained are shown in figure 3.28.

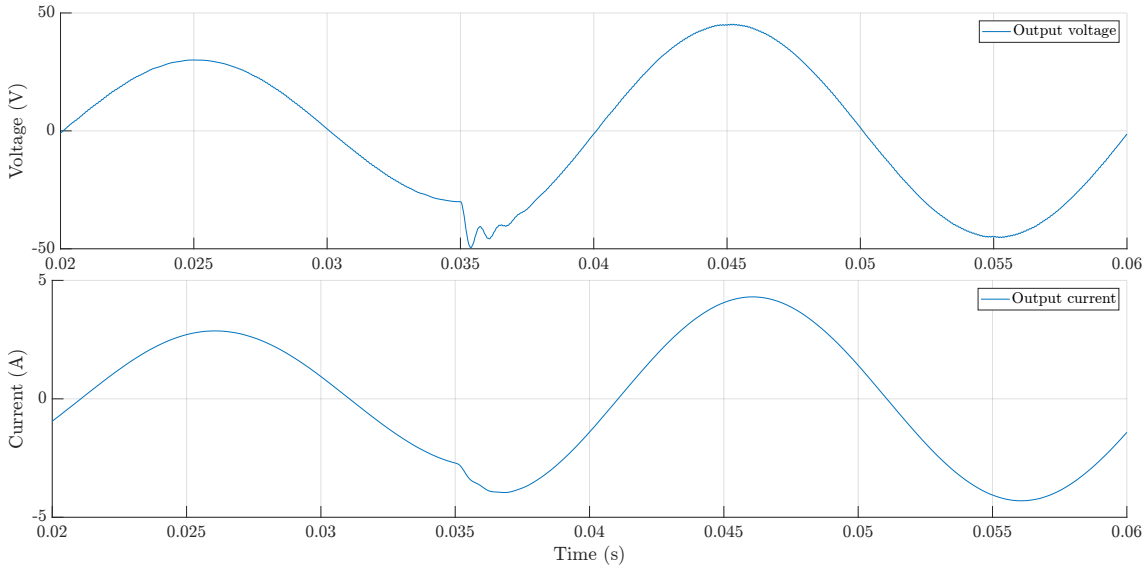


Figure 3.28 – Output voltage and current waveforms obtained in the simulation of voltage reference dynamic perturbation.

It is possible to see that the dynamic change in the voltage reference introduces some perturbation in the output voltage and current, but this issue is solved after a short time. The current is subjected to a phase shift due to the inductive component of the load. The dual PI voltage control is a control technique that gives satisfactory results even if subjected to a dynamic change of the voltage reference.

Dynamic Change of the Load Parameters

It is interesting to simulate the behave and response of the controller if the inverter is subjected to a change in the load, that will result in a different current demand. At time t_2=0.035 s to the load is connected in series an additional R_{load}, the control strategy should adapt to this perturbation, guaranteeing as output the requested voltage despite a higher current demand caused by the additional load. Figure 3.29 shows the output voltage and current obtained simulating this condition.

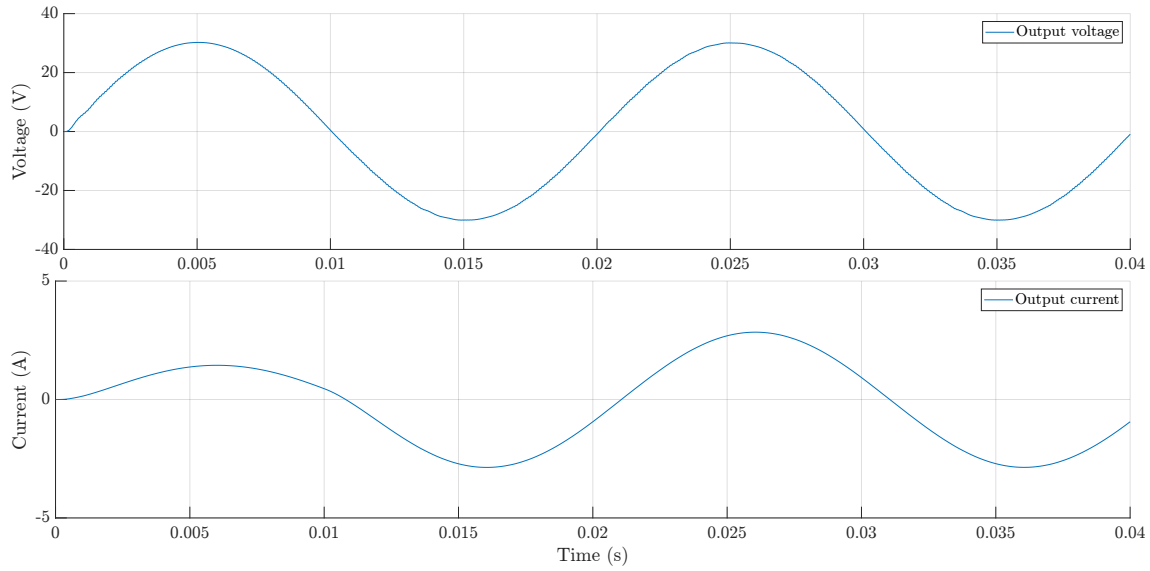


Figure 3.29 – Output voltage and current waveforms obtained in the simulation of the load dynamic perturbation.

Is it possible to see that the introduction of the additional load at t_1 brings at a higher output current, the output voltage is not subjected to perturbations of changes and it is kept at the desired value, the result obtained from this simulation is satisfactory.

3.6 Comparison between the Purposed Current and Voltage Control Strategies

The closed-loop strategies applied to the 5LCHBI introduced in the previous sections differ in the way of operating, in the physical quantities controlled and in the parameters needed in order to work. However, it is interesting to give a comparison table for summarising the strong points, advantages, disadvantages and limitations of these two control techniques.

Table 3.10 – Comparison between the multi offset hysteresis band and the dual PI loop voltage control applied on the 5LCHBI.

Object of the analysis	MOBHM	Dual PI Loop
Value controlled	Output current	Output voltage
Switching frequency	Not set and not constant	Set and constant
Stability of the strategy	Always guaranteed	PIs have to be tuned
Main input parameter	Current reference and max. error	Voltage reference
Knowledge of the load	No	Yes
Implementation difficulty	Low-Medium	Medium-High
Additional output filter	Yes, without extra procedures	Yes, re-tuning the PIs

4 Realization of the 5-Level CHB Inverter Physical Prototype

After the theoretical analysis of the 5LCHBI and the evaluation of the results obtained with the simulations, the focus of this work has been moved on the realization of the inverter prototype. The purpose of the design and construction of the aforementioned device is to give a small-scaled 5LCHBI that in future should feed a phase of a nine-phase PMSM. Innovative components such as GaN FET switches and new-generation isolated drivers has been introduced in the PCB design in order to perform notable tests and collecting useful feedback results that can help achieving, the full-scale prototype realization.

4.1 Structure of the Chapter and Methodology

As explained in previous sections, the main feature and advantage of this inverter topology it the possibility to increase the number of voltage output levels by increasing the number of H-bridges modules connected in series. The most logical designing approach consists in the realization of the single prototype. In this way this procedure becomes easier compared to designing a single-block 5LCHBI PCB. Moreover, realizing multiple H-bridge gives the chance of increasing in future the number of sub-modules connected in series to realize for example seven or eleven levels CHB inverter.

The H-bridge inverter is composed by two half-bridge devices, as the two sub-modules are identical, it is possible focusing the design process on the realization of the single half-bridge printed circuit board. Subsequently it is possible to extend the half-bridge circuit design to generate the H-bridge module.

The scheme structure of the PCB prototype realization can be schematized as it follows:

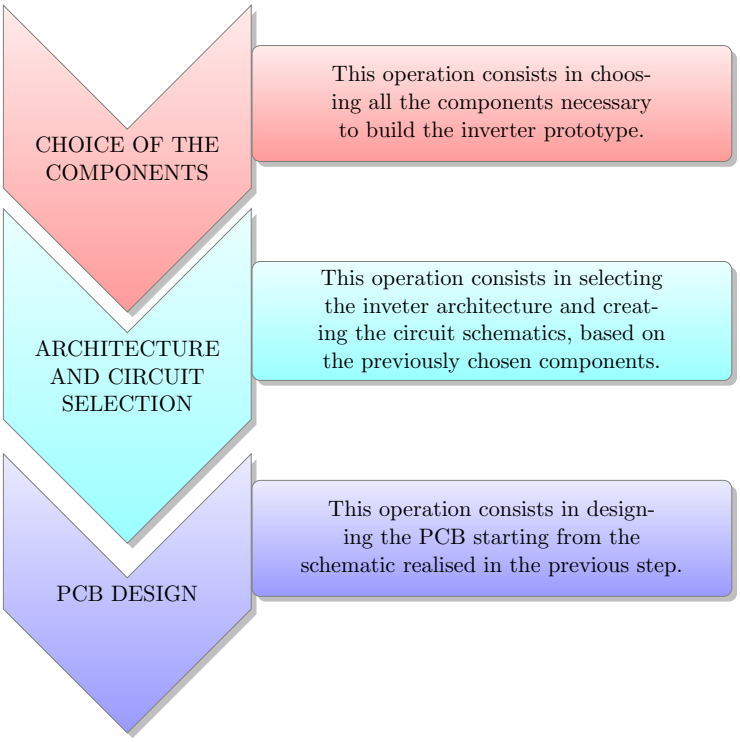


Figure 4.1 – Scheme of the prototype realization process.

4.2 Selection of the Components

This analysis will be conducted starting with the switching devices, that can be seen as the most important components of the inverter. Subsequently the drivers will be illustrated along with the other components such as power supplies and sensors will be analyzed.

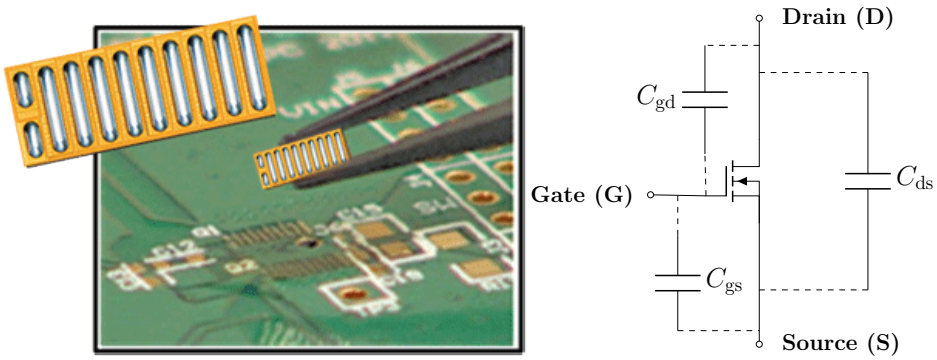
4.2.1 Switching Devices

The switch is probably the most important component that constitutes the inverter. In power electronics the switches act as solid-states devices, which means that they are able to guarantee the switching operations without mechanical movement. The first solid-state switching device was the transistor invented in Bell Labs in 1947, and since that moment the progress in the switching industry never stopped, aiming at achieving higher switching speeds, reduced losses and smaller dimensions. Silicon became the most used material for the semiconductor transistors not only because of its superior electrical proprieties but also because it was easy to produce than the vacuum tube [7]. During the 70's and 80's the performances of the transistors exponentially improved, Moore's Law [30] showed a doubling of the performances with a reduction of the cost approximately every 18 months. The silicon power MOSFETs led this race for decades, and as it was with the vacuum tube, nowadays

they reached the end of the road in improving their performances while reducing their cost. The device that is the candidate to lead the electronic performance progress to higher levels is gallium nitride [15].

Gallium Nitride (GaN)

GaN is a wide band-gap semiconductor used in power transistors and integrated circuits. A thin layer of aluminum gallium nitride (AlGaN) is grown on the top of a GaN crystal, a strain is created at the interface that includes a compensating two-dimensional electron gas (2DEG)[7], this 2DEG is used efficiently to conduct electrons when an electric field is applied to it. This characteristic allows GaN to conduct electrons 1000 times more efficiently than silicon, while being produced at a lower cost.



(a) GaN transistor [9] **(b)** GaN circuit representation

Figure 4.2 – Gallium Nitride (GaN).

It is interesting at this point to compare the GaN and MOSFET characteristics, to enlighten their similarities and differences:

In Common with Si MOSFET:

- Voltage driven, the driver discharges the capacitance C_{ISS}, which is the capacitance given by the sum of the gate drain capacitance C_{GD} and the gate source capacitance C_{GS}, as shown in figure 4.2b.
- The slew rate is controllable by an external gate resistance R_{G}.
- Generally, GaNs are compatible with (recent) Si MOSFET driver chips.

Differences with Si MOSFET:

- The gate charge Q_{g} necessary to drive the GaN is much lower than the MOSFET one, this feature translates into lower drive losses and faster switching.
- GaNs have higher gain and lower V_{GS}.
- The voltage threshold V_{th} of GaNs is lower, typically 1.25 V, this helps achieving faster switching speeds but makes the driving procedure more delicate, the Miller Effect [29] has to be better controlled.

- GaN has zero reverse recovery charge Q_{rr}, making the device suitable for half bridge hard switching, giving the possibility to replace IGBT switches.

The prototype should help achieving innovative and useful test results, thus it is necessary to accomplish modern and newfangled design and components; for this reason GaN have been selected as power switch to be used in the inverter's prototype. These devices have switching speed that can reach values above 1 MHz [15]. For accomplishing this, GaN's gate-to-source voltage rises from the OFF value to the ON value in a very short time, making the V_{gs} rising curve very steep, also compared to the typical MOSFET's one. By the evaluation of this waveform, in the test site, it is possible to measure the parasitic capacitances that affect the system and estimate the current that flows through them, determining the parasitic losses. This result is achievable thanks to the unique characteristics of GaN. Also, driving the switches at high switching speeds, in the order of 100 kHz, which is generally faster than conventional electric drives inverters [25], will help achieve innovative results in this research field.

GaN Driving Procedure

As aforementioned, the driving procedure for GaN is more complex and delicate than driving MOSFET FETs. The gate of the GaN can be considered as a capacitance, as shown in figure 4.2. The gate voltage, which is the aspect that activates or deactivates the conduction of the switch, does not increase unless its gate input capacitance is charged. The GaN does not turn on until its gate voltage reaches the voltage threshold V_{th}, which is the minimum voltage to create a conduction channel between the source and the drain [32]. While considering driving operations, the gate charge Q_g of the GaN becomes more important than its capacitance, figure 4.3 shows the charging mechanism of the GaN capacitances, introduced in figure 4.2.

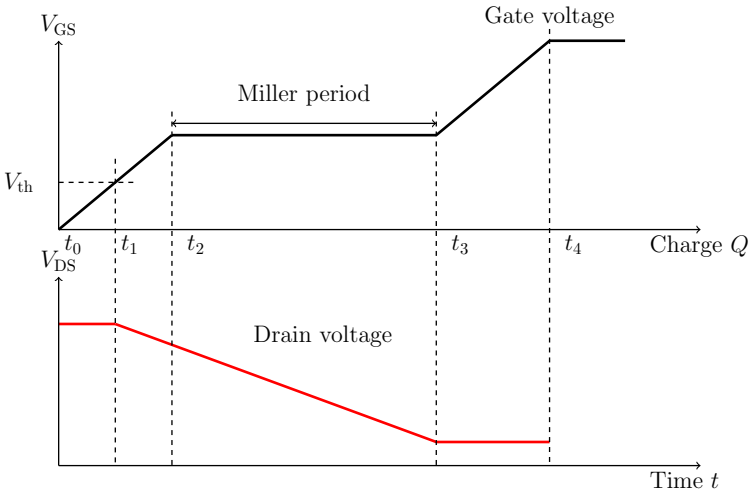


Figure 4.3 – GaN gate charge vs gate voltage [15].

The input capacitance can be defined as: $C_{iss} = C_{gd} + C_{gs}$ while the output capacitance can be defined as: $C_{oss} = C_{ds} + C_{gd}$. The gate of a GaN starts accumulating electric charge when a voltage is applied to it, as shown in figure 4.3.

It is possible to briefly summarize the gate charge mechanism as it follows:

1. From the period t_0 to t_1, the gate drive circuit charges the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} via the gate series resistor (shown in figure 4.3) until the threshold voltage V_{th} is reached.
2. From the period t_1 to t_2, V_{DS} is greater than V_{th}, causing a current to flow in the drain. C_{gd} and C_{gs} continue to be charged in this period of time. As the gate voltage increases, the current drain increases. At t_2 the gate voltage reaches the Miller Voltage [29].
3. From the period t_2 to t_3, V_{GS} remain constant at the Miller Voltage, due to the Miller Effect. Since the gate voltage remains constant while the main current increases, the drive current flows to C_{gd} and not to C_{gs}.
4. From the period t_3 to t_4, the gate is charged to the over saturated state [32]. Both C_{gd} and C_{gs} are charged until the voltage V_{GS} reaches the supply voltage.

It is possible to summarize the main characteristics of the chosen GaN:

Table 4.1 – Characteristics of the selected GaN device: EPC EPC2065 [7].

Parameter	Name	Value
Drain-to-Source Voltage (continuous)	V_{DS}	80 V
Drain current (continuous)	I_{D}	60 A
Minimum Gate-to-Source Voltage	$V_{\text{GS,min}}$	−4 V
Maximum Gate-to-Source Voltage	$V_{\text{GS,max}}$	6 V
Gate threshold Voltage	V_{th}	1.2 V
Drain Current (pulsed, $T_{\text{puls}} = 300\,\mu\text{s}$)	$I_{\text{D,puls}}$	215 A
Drain-Source On Resistance	$R_{\text{DS,ON}}$	3.6 mΩ

4.2.2 Drivers

The basic requirements for a GaN drive circuit consists in applying a voltage sufficiently higher than V_{th} and a drive capability to sufficiently charge the input capacitance [21]. The other requirements of the driver are guaranteeing a fast propagation of the input signal, avoiding undesired activation of the GaN which is driven (prevention of the Miller turn-on). At the present, the driving operations are done by microcontrollers, which combined with additional circuitry and components, can drive the switches optimally. An advantage of using driver microcontrollers is that they integrate some features which improve the safety and the reliability of the driving process. A Block diagram of the driver which will be used in this application is shown in figure 4.4.

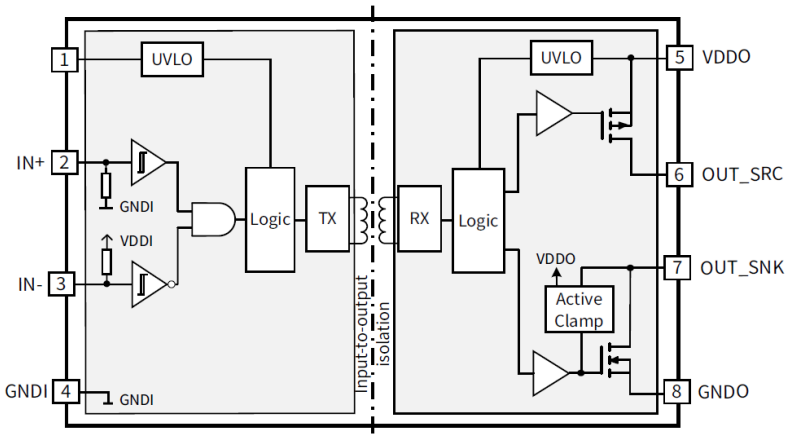


Figure 4.4 – Block diagram of a single-channel isolated gate-driver Infineon 1EDB7275F [27].

A functional description summary is given, in order to illustrate the main features that this driver microprocessor can offer [27]:

- There is **insulation between the input and the output side**, this aspect increases the safety for the user in case of fault and also for the components at the input stage, which generally don't well tolerate overvoltages that can occur in case of fault. Due to the insulation between circuitry side and power side, independent power management are required. Undervoltage Lockout (UVLO) functions for both input and output supplies ensure a defined startup and robust functionality under all conditions.
- **The UVLO ensures no driver operations for supplies below the UVLO threshold**, but due to transients-induced currents on the GaN side, there can be unwanted turn-on of the switch. This specific driver improves UVLO function with an "Output active clamping", that ensures that the output is actively held low in case of insufficient output-side supply voltage.
- There are **two driver output sources**, which give the possibility of using separate gate resistances R_g for turn-on and off, this feature improves the Miller effect control, as it will be deeper explained in next sections. A driver with this configuration, requires two input PWM signals to give as output two gating signals.
- **The driver requires two different power supplies**, at the input side a voltage is necessary to feed the driver itself while at the output side a power supply is needed to generate the V_{GS}.

The driver that has been selected for this purpose is the 1EDB7275F [27], which is a single-channel isolated gate driver. It is possible to summarize the main characteristics of the chosen driver:

Table 4.2 – Characteristics of the chosen driver device: INFINEON 1EDB7275 [27]

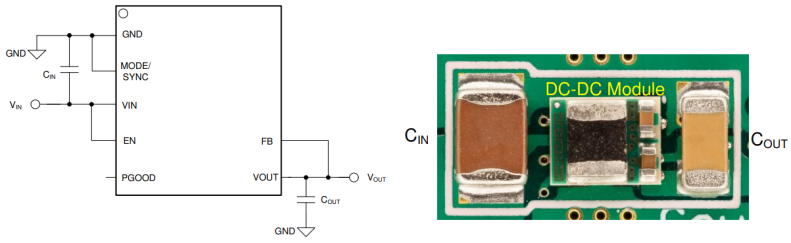
Parameter	Name	Value
Minimum Input Supply Voltage	$V_{\mathrm{DDI,min}}$	3 V
Maximum Input Supply Voltage	$V_{\mathrm{DDI,max}}$	15 V
Minimum Output Supply Voltage	$V_{\mathrm{DDO,min}}$	4.5 V
Maximum Output Supply Voltage	$V_{\mathrm{DDO,max}}$	20 V
Input Voltage Threshold for transition LH	V_{INH}	2.2 V
Input Voltage Threshold for transition HL	V_{INL}	1.3 V
Input-to-Output Isolation Voltage	V_{ISO}	3000 $\mathrm{V_{RMS}}$
Drain-Source On Resistance	$R_{\mathrm{DS,ON}}$	3.6 mΩ
Input-To-Output Propagation delay	T_{prog}	45 ns
Minimum Input-To-Output Propagation delay accuracy	$T_{\mathrm{acc,min}}$	−4 ns
Maximum Input-To-Output Propagation delay accuracy	$T_{\mathrm{acc,max}}$	6 ns
Common mode transient Immunity	$CMTI$	>300 $\mathrm{V\,ns^{-1}}$

4.2.3 Power Supplies

As previously mentioned, it is to necessary to feed the driver and the GaN using different supplies, to guarantee the insulation between the output (GaN) and input side (Driver). These two distinct power rails are analyzed and explained separately.

Input Power Rail

It is necessary to implement a power rail to feed the driver and the current sensors, these devices require a 5 V input voltage to operate. The device that has been selected to generate the 5 V rail is a Step-Down DC/DC converter, the LMZM23601 [3], which can convert a wide range of voltages (4 V to 36 V) into a 5 V output. This will give the chance, while testing the prototype, to connect to the PCB a wide range of voltage values for always having as output, thanks to this device, a constant 5 V rail. The pictures of the converter and its electric schematics are shown in figure 4.5.



(a) Electric scheme **(b)** Converter

Figure 4.5 – LMZM23601 Step Down DC/DC Power module (b) with its circuit (a) [3]

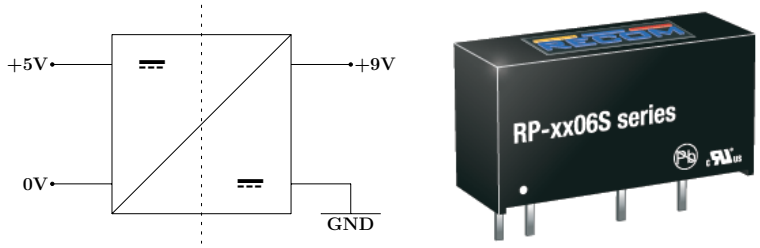
It is possible to summarize the main characteristics of the chosen input DC/DC converter:

Table 4.3 – Characteristics of the selected converter: TI LMZM23601 [3].

Parameter	Name	Value
Minimum Input Voltage	$V_{\mathrm{DDI,min}}$	4 V
Maximum Input Voltage	$V_{\mathrm{DDI,max}}$	36 V
Output Voltage	V_{DDO}	5 V
Output Current	I_{O}	1 A
Efficiency	η	70/90 %

Output Power Rail

To drive the GaNs switch, it is necessary to apply a positive voltage V_{GS} between its gate and source. The most common solution to provide this voltage at the switches' side in power electronic applications is using a bootstrap capacitor. Despite its low cost and simplicity, the bootstrap circuit has some limitations, especially in duty cycle values and switch on-time. The capacitor, when charged, provides the required V_{GS} but its charge needs to be refreshed and this operation can't be always be guaranteed, especially if the inverter is, for example, part of a electric drive system. When driving a electrical machine, it is possible to occur in situations in which the in duty cycle of the inverter's switches is extremely high, in some situations even unitary. If the switches' duty cycle is that high ($\sim$1), the capacitor charge cannot be refreshed due to the reduced time between one switching operation and the other. It is possible to overcome this back draw supplying the output power rail with isolated DC/DC converters. These devices require a voltage input, in this case the 5 V provided by the step down converter LMZM23601[3] previously analyzed in section 4.2.3. ISO DC/DC converters provide the necessary voltage to drive the GaN FETs while guaranteeing the insulation between the output and input side. The main advantage of using these devices is that they always guarantee the desired gate-source voltage, the main back draw of this solution is an increase in the circuit complexity and cost, while the overall system efficiency decreases. The device that has been chosen to suit this purpose is the RECOM RP-0509S [2], the device with its circuit it is shown in figure 4.6.



(a) Electric scheme **(b)** DC/DC Converter [2]

Figure 4.6 – ISO DC/DC Power module (b) with its circuit (a).

It is possible to summarize the main characteristics of the chosen ISO DC/DC converter for the power rail:

Table 4.4 – Characteristics of the chosen ISO DC/DC converter: RECOM RP-0509S [2].

Parameter	Name	Value
Input Voltage	V_{DDI}	5 V
Output Voltage	V_{DDO}	9 V
Output Current	I_O	111 mA
Efficiency	η	75 %
Maximum Capacitive Load	CL_{max}	1000 µF
Input-to-Output Isolation Voltage	V_{ISO}	5200 V_{RMS}

4.2.4 Additional Driver Circuitry

To improve the switching process performances, an additional driver circuit has been implemented. As aforementioned, the low voltage threshold of the GaN makes the switching process more complex and delicate. It is possible to apply a negative V_{gs} while the switch is off, to avoid unwanted Miller activation, that can be caused by overshooting that can occur in turning off procedures. Because of this negative potential, the the chances of a unwanted V_{th} exceeding are remarkably reduced.

A voltage divider composed by a Zener diode and a resistance splits the 9 V output voltage generated by the ISO DC/DC, examined in section 4.2.3, in a positive and a negative voltage. The positive voltage is subsequently controlled by a Low Drop regulator (LDO), making it suitable for the ON switch operations while the residual negative voltage is applied to the switch in the OFF switch operation.

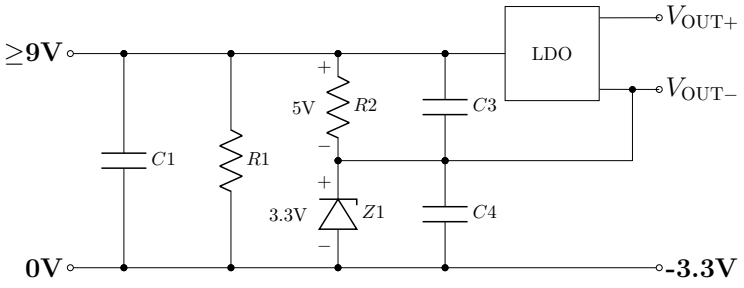


Figure 4.7 – Additional driver circuitry.

The input of the circuit is given by the ISO DC/DC converter, an input filter composed by $C1$ and $R1$ has been included in the circuit. A Zener Diode $Z1$, combined with a resistance $R2$ is used to generate the negative gate drive rail. The Zener diode has been located under the resistance to avoid possible overvoltages that can damage the switch in turning on operations. In the circuit a 3.3 V Zener diode has been included, however it is possible to change its value during test operations to evaluate different negative V_{gs} situations. Thanks to the LDO, a constant 5 V V_{gs} is applied to the GaN in ON-switching operations, avoiding switching failures due to gate-source overvoltages. It is possible to apply to apply Kirchoff's voltage law (KVL) combined with the voltage partitioning formulas to see that the 9 V input voltage has been split in a 5.7 V voltage at $R2$'s terminal and a 3.3 V voltage at $Z1$'s terminal, which referred to the ground potential becomes -3.3 V. In this way controlled negative and positive voltage voltage rails have been generated.

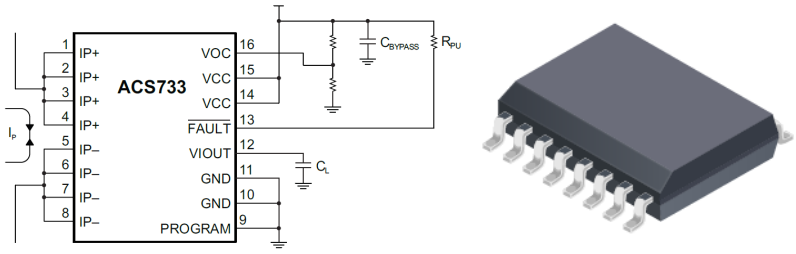
It is possible to summarize the main characteristics of the chosen LDO for the additional driver circuitry:

Table 4.5 – Characteristics of the selected Low-Dropout regulator: ST LD2980 [33].

Parameter	Name	Value
Minimum Input Voltage	$V_{\mathrm{DDI,min}}$	$-0.3\,\mathrm{V}$
Maximum Input Voltage	$V_{\mathrm{DDI,max}}$	$16\,\mathrm{V}$
Output Voltage	V_{DDO}	$5\,\mathrm{V}$
Maximum Output Current	$I_{\mathrm{O,max}}$	$50\,\mathrm{mA}$
Efficiency	η	75 %
Maximum Capacitive Load	CL_{max}	$1000\,\mu\mathrm{F}$
Dropout Voltage	V_{drop}	$0.12\,\mathrm{V}$ @ $50\,\mathrm{mA}$
Output Voltage Tolerance	V_{tol}	+/-0.5 %

4.2.5 Current Sensors

Two current sensors are added to the PCB circuit, the first sensor measures the current absorbed from the DC input and second measures the AC current generated by the inverter, absorbed by the load. The device ALLEGRO ACS732KMA [1] has been selected for this purpose. ACS732KMA is a compact device for measuring high frequency currents in DC-DC converters and switching power applications. The sensor offers high insulation and high bandwidth Hall-effect based current sensing. The device with its circuit it is shown in figure 4.8.



(a) Electric scheme **(b)** Current Sensor

Figure 4.8 – Current sensor device (b) with its circuit (a) [1].

It is possible to summarize the main characteristics of the chosen current sensor:

Table 4.6 – Characteristics of the chosen Current Sensor: ALLEGRO ACS732KMA [1].

Parameter	Name	Value
Minimum Input Current	$I_{\mathrm{P,min}}$	$-65\,\mathrm{A}$
Maximum Input Current	$I_{\mathrm{P,max}}$	$65\,\mathrm{A}$
Sensitivity	S_{e}	$26.67\,\mathrm{mV\,A^{-1}}$
Nominal Voltage Supply	V_{cc}	$5\,\mathrm{V}$
Efficiency	η	75 %
Maximum Capacitive Load	CL_{max}	$1000\,\mu\mathrm{F}$
Dropout Voltage	V_{drop}	$0.12\,\mathrm{V}$ @ $50\,\mathrm{mA}$
Output Voltage Tolerance	V_{tol}	+/-0.5 %
Dielectric Strength Voltage	V_{ISO}	$4800\,\mathrm{V_{RMS}}$
Primary Conductor Resistance	R_{cond}	$0.85\,\mathrm{m\Omega}$
Output Analog Bandwidth	O_{B}	$1\,\mathrm{MHz}$

4.2.6 DC Side Capacitors

Switching an inverter at high frequencies brings at having high frequency currents and voltage ripple on the DC side. These high frequency currents can damage the DC input source especially if it consists in a single or multiple batteries which are particularly sensible, and delicate compared to other DC sources. It is possible solve these issues including in the circuit between the voltage input source and the inverter some capacitors. The capacitors generate a low impedance path for the return oh high frequency currents allowing to pass only low frequency currents (ideally only DC currents). The capacitance value has been calculated starting from the maximum voltage ripple $\Delta_{\mathrm{V,max}}$, the maximum output current $I_{\mathrm{o,max}}$ and the max switching frequency f_{s}, the procedure for obtaining the DC side capacitor values C_{DC} is the following [35]:

$$C_{\mathrm{DC}} = \frac{1}{4} \frac{I_{\mathrm{o,max}}}{f_{\mathrm{s}} \Delta_{\mathrm{V,max}}} \tag{4.1}$$

The values are chosen arbitrarily and they are the following:

- $\Delta_{V,\mathrm{max}} = 1\,\mathrm{V}$
- $I_{\mathrm{o,max}} = 20\,\mathrm{A}$
- $f_{\mathrm{s}} = 1\,\mathrm{kHz}$

Substituting the values in the equation brings to obtaining C_{DC}=50 µF. The capacitors that have to be used at the DC side have to fulfill some requirements:

- High capacity density.
- Low parasitic values (Internal series resistance ESR and Internal resistance inductance ESL), especially at high frequency these parasitics can be problematic.
- Low losses.
- Stable value across the temperature spectrum.

A total capacitance value of 105 µF has been chosen and used in the prototype for precautionary reasons. Capacitors with different values have been used to widen the frequency spectrum of the filter.

4.3 Prototype Realization

4.3.1 Prototype Architecture

To introduce the PCB design, firstly it is interesting analyzing the half-bridge module circuit architecture that has been selected. Because of the H-bridge circuit is symmetrical, i.e. composed by two identical half-bridges, the circuit scheme of figure 4.9 only represents a half-bridge sub-module. Based on this architecture, the final prototype will consist in a H-bridge module.

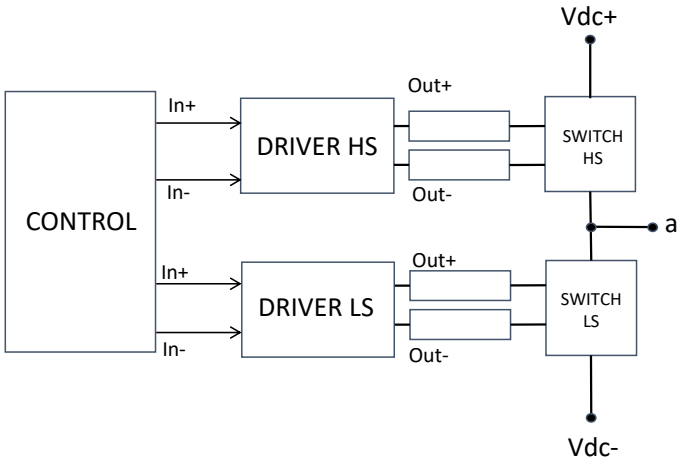


Figure 4.9 – Scheme of the chosen circuit architecture for the half-bridge.

It is possible to briefly analyze figure 4.9 dividing the circuit in three main stages:

- **Control**: the control stage is responsible for the generation of the switching pulses, low-power signals are generated are sent to the drivers.
- **Drivers**: as saw in section 4.2.2, the drivers are power amplifiers that accept low-power input signals coming from the control stage to produce high-current output signals for the gate of the switches. In figure 4.9 is possible to distinguish High Side (HS) and Low Side (LS) drivers. The LS driver is placed between the load a and the negative DC input supply $V_{\text{dc-}}$ whereas the HS driver is placed between the load and the positive DC input supply $V_{\text{dc+}}$.
- **Power side**: this stage is composed by the LS switch and HS switch, driven respectively by the HS and the HS drivers. The switching devices that have been chosen are the GaN FETs, the other elements of this stage are the DC source input terminals, represented by $V_{\text{dc+}}$ and $V_{\text{dc-}}$ while the inverter AC output is represented by the terminal a.

Subsequently to the architecture selection, the schematics has been realized using the software AUTODESK EAGLE, the complete blueprints of the prototype are available at appendix A.

4.3.2 Considerations about the PCB Design

During the PCB design process, it is necessary to take in consideration the parasitic elements which can cause disturbs and malfunctioning in the device healthy operations. The presence of these elements is inevitable, however it is possible to mitigate them introducing some designing solutions. The PCB is composed by certain number of parallel conducting elements divided by an insulator, forming a capacitor. Likewise, the PCB conductors form complete loops, creating an inductor. The sections of the PCB which are mostly affected by parasitics are the **gate drive loop** and the **power loop**, as shown in figure 4.10.

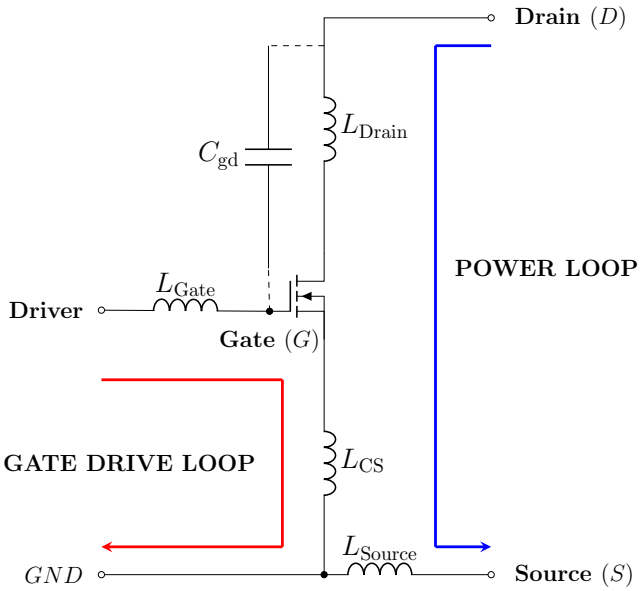


Figure 4.10 – Parasitic elements of the power and of the gate loop [15].

It is possible now to examine the parasitic element and at the same time summarize some possible solutions to mitigate these unwanted elements.

- **Drain-to-Gate coupling capacitance** C_{gd}: Can cause capacitive noise coupling, it is possible to reduce it avoiding the overlapping between drain and gate driver copper track.
- **Power Loop inductance** L_{Drain} and L_{Source}: They can cause drain voltage overshoots and turn-on/off ringing in the drain current/voltage. It is possible to reduce them minimizing the power loop length and placing decoupling capacitors as close as possible to the power devices.
- **Gate Loop inductance** L_{Gate}: Can cause gate signal over/undershoot and Miller turn-on. It is possible to reduce these effects by placing the driver close to the GaN FET reducing the length of the gate loop.
- **Common Source inductance** L_{CS}: The minimization of this element is critical for the gate drive stability; it can cause gate ringing and oscillations and reduce the switching speed. It is possible to reduce it using the Kelvin connection [7] or by making the gate drive loop as short as possible.

The parasitics have to be minimized in the following order, according to their impact on the PCB healthy operations [15]:

1. **Common Source inductance** L_{CS}.
2. **Gate Loop inductance** L_{Gate}.
3. **Power Loop inductance** L_{Drain} and L_{Source}.
4. **Drain-to-Gate coupling capacitance** C_{gd}.

The general approach that has been followed in the PCB design was intended to create a compact prototype, with minimized distances and tight traces, aiming at the optimal reduction of the parasitic elements.

4.3.3 Design of the Prototype Printed Circuit Board

After the realization of the complete prototype schematics that includes the aforementioned devices and all the additional components to guarantee the prototype safe and healthy operations, the PCB design has been made. The prototype board consists in a 4-layers PCB and it is shown in figure 4.11.

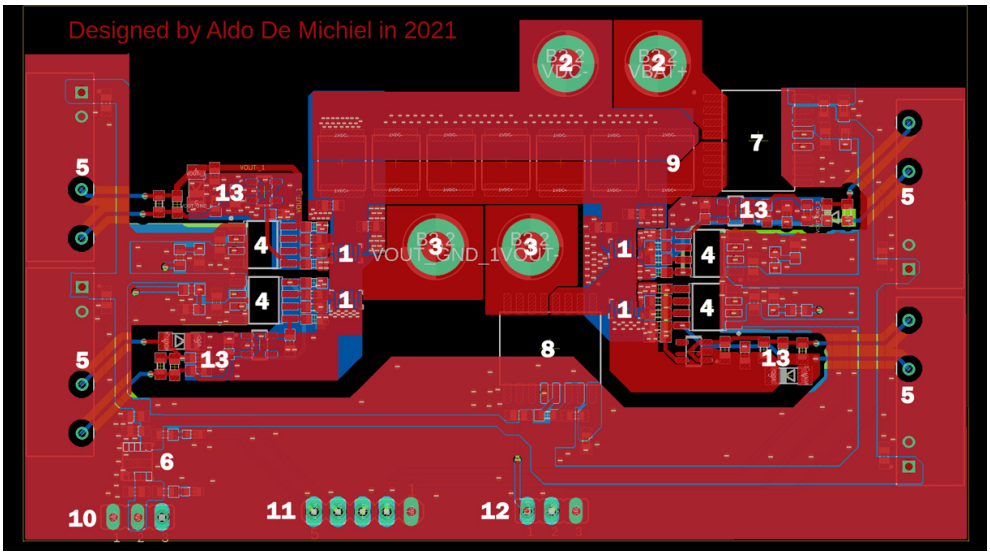


Figure 4.11 – PCB of the H-bridge inverter module.

The components of the PCB are summarized in the next table.

Table 4.7 – Components of the H-bridge module PCB.

#	Component	Name
1	GaN Switches	EPC2065 (EPC)
2	DC input terminals	-
3	AC output terminals	-
4	Drivers	1EDB7275F (Infineon)
5	ISO DC/DC Converters	RP-0509 (RECOM)
6	Input DC/DC Converter	LMZM23601 (Texas Instruments)
7	Input Current Sensor	ACS732KMA (ALLEGRO)
8	Output Current Sensor	ACS732KMA (ALLEGRO)
9	DC Side Capacitors	C5750X7S2A156MT000N (ICSOSO)
10	12V Input Supply	-
11	PWM Input Signals	-
12	Current Sensors Output	-
13	Additional Driver Circuitry	-

The GaN switches, as it is possible from the figure 4.11, have been placed as close as possible to their respective gate resistances and to the drivers to reduce the gate inductance. In order to minimize the drain and source inductance, the power loop has been made as short as possible. All the converters and active components have been decoupled using capacitors. Each PCB layer is analyzed separately, in order to enlighten its power traces and circuits.

First Layer

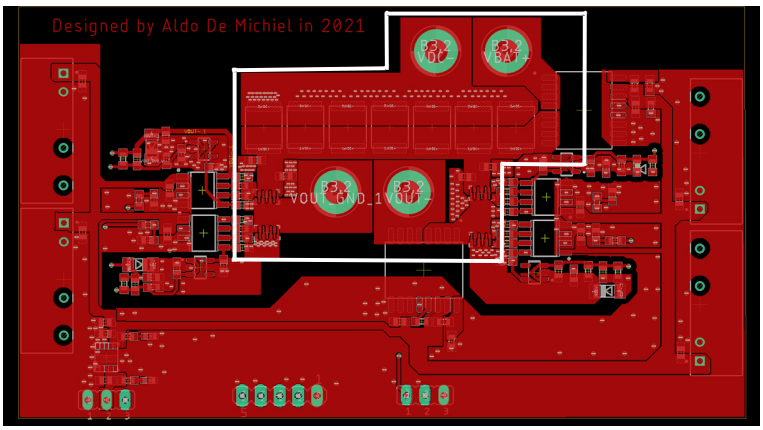


Figure 4.12 – First layer of the PCB.

To analyze better the first layer's traces and circuits, it is possible marking two different areas:

- **The power rail** which is enclosed in the white box. The power rail circuit is made by the input and output terminal, the four switches that compose the H-bridge and their respective connections.
- 5 V **rail and connections** which is outside the white box. This layer has been used to trace the 5 V rail and for connecting the devices that populate the PCB.

Second Layer

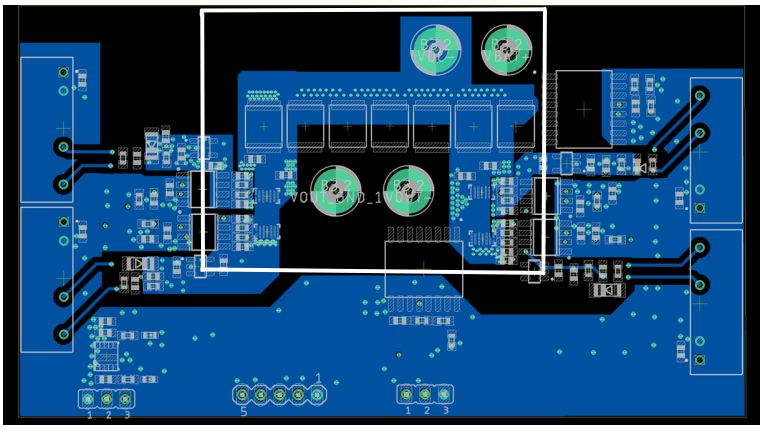


Figure 4.13 – Second layer of the PCB.

The second PCB layer can be seen as the dual layer of the first one. The white box enlightens the negative DC input supply with its circuit and terminal. The area outside this perimeter has been used to trace the ground plane. In order to keep this potential as close as possible to GND value, this trace has been made as large as possible, using all the surface available on this layer.

Third Layer

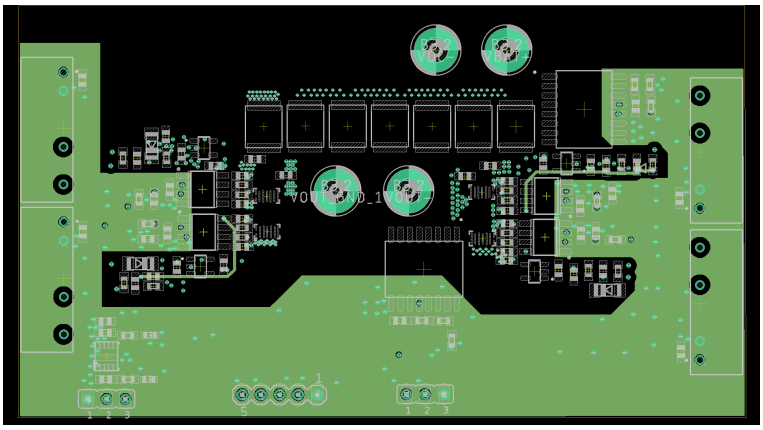


Figure 4.14 – Third layer of the PCB.

The third layer has been mainly used to create a wide ground plane trace to keep the potential as close as possible to GND value. This layer has also been used to make some connections between components that did not fit on the first layer.

Fourth Layer

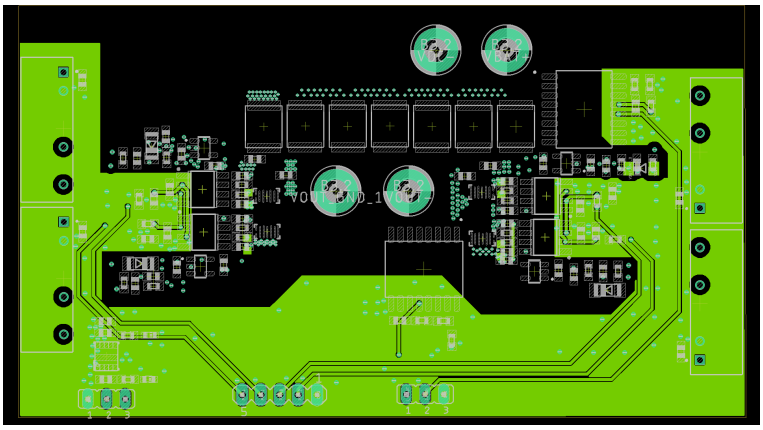


Figure 4.15 – Fourth layer of the PCB.

The fourth layer, which stands on the bottom side of the PCB, has been mainly dedicated to the signal traces. It is possible to notice the PWM signal and the Current sensor output traces, the wide trace stands for the 5 V rail.

4.3.4 PCB Assembling Process

To give some conclusive information about this chapter, a illustrative process of the prototype design and realization is given.

Manufacturing

Before the prototype commissioning, it is possible to see in figure 4.11 the manufacturing picture that has been generated from the designing program.

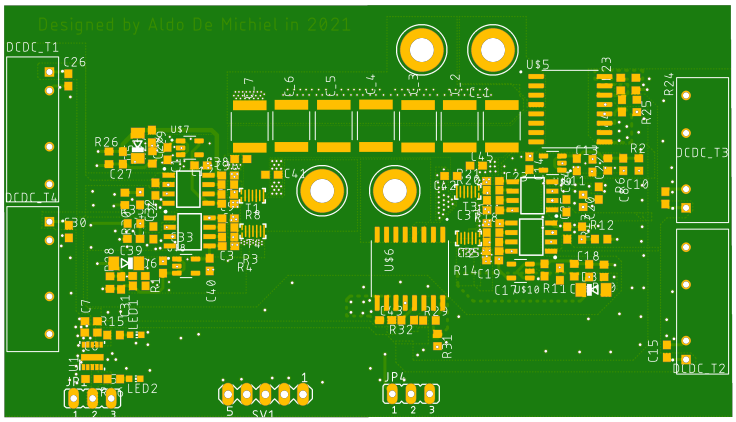


Figure 4.16 – Manufacturing picture of the PCB prototype.

Before the commissioning of the prototype, the analysis of this picture can enlighten eventual issues, for example traces overlapping or missing labels, that can affect the future PCB assembling.

Empty PCB

Figure 4.17 shows the PCB after the realization, which is empty, ready to be populated with the components. It is possible to see that the figure it's identical to figure 4.16, antecedent to the manufacturing process. A comparison with a 5-cent coin helps figuring out the PCB size, which is 5 cm wide and 11 cm long.

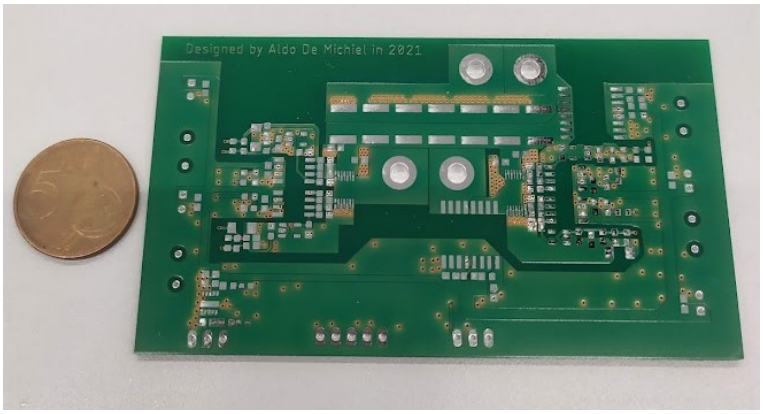


Figure 4.17 – Empty PCB.

Populated PCB

The PCB shown in figure 4.17, has been populated with all the parts aforementioned in section 4.2. After affixing the components, the connections have been tested to identify eventual soldering issues like shortcuts or open circuits. Once completed this task, the test procedures can start.

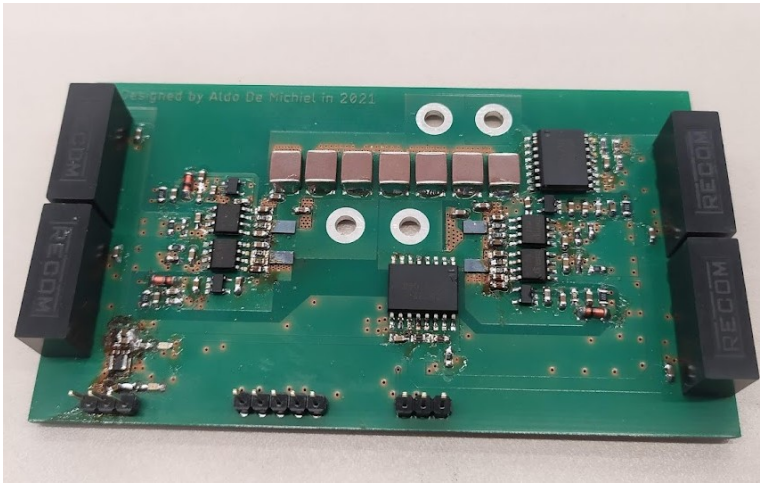


Figure 4.18 – Populated PCB.

5 Tests and Results

For evaluating the prototype performances, some experiments have been conducted on the H-bridge PCB module. An oscilloscope with an internal function generator has been used to generate the PWM signals to drive the switches and to collect the results and images of the tests.

5.1 Rising and Falling of the V_{gs}

Rising of the V_{gs} with the Inverter Unloaded

To verify the gate driver response stability, some tests have been performed to evaluate the rising and the falling of the gate-source voltage V_{gs}. A function generator, internal to the oscilloscope, has been used to produce a arbitrary square-wave signal to drive the switches. The input and the output terminal have been open-circuited, for only evaluating the V_{gs} behavior, without any DC input source or load connected to the inverter, that can interfere with the test.

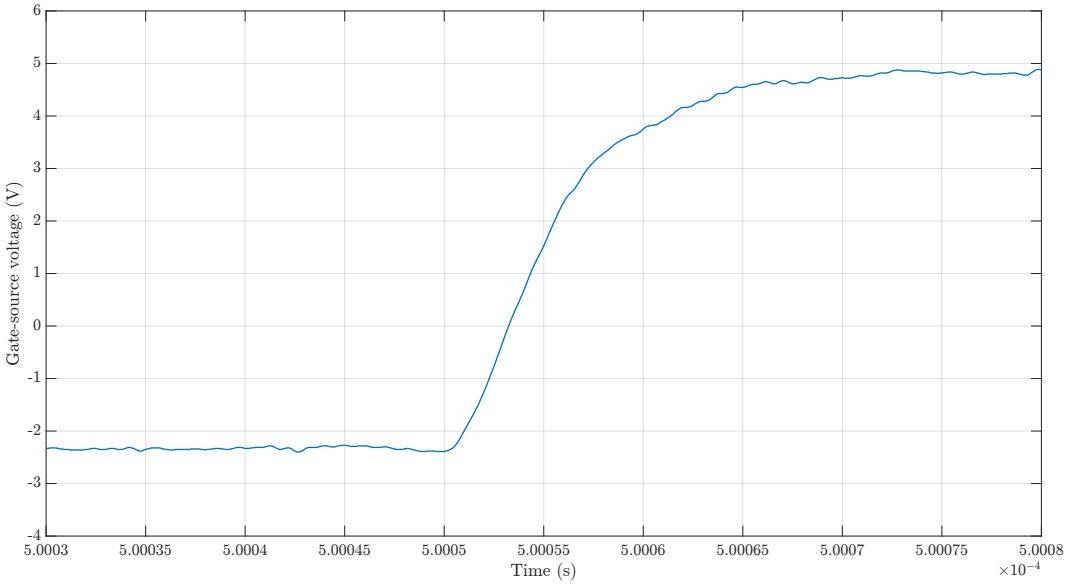


Figure 5.1 – Rising waveform of the gate-source voltage V_{gs}.

The V_{gs} waveform shows a fast and stable response, the voltage rises to 5 V from −2.2 V (voltage value set by the Zener diode) in c.a. 20 ns, without any under or overshoots. This result confirms that it is possible to reach high speed switching.

Falling of the V_{gs} with the Inverter Unloaded

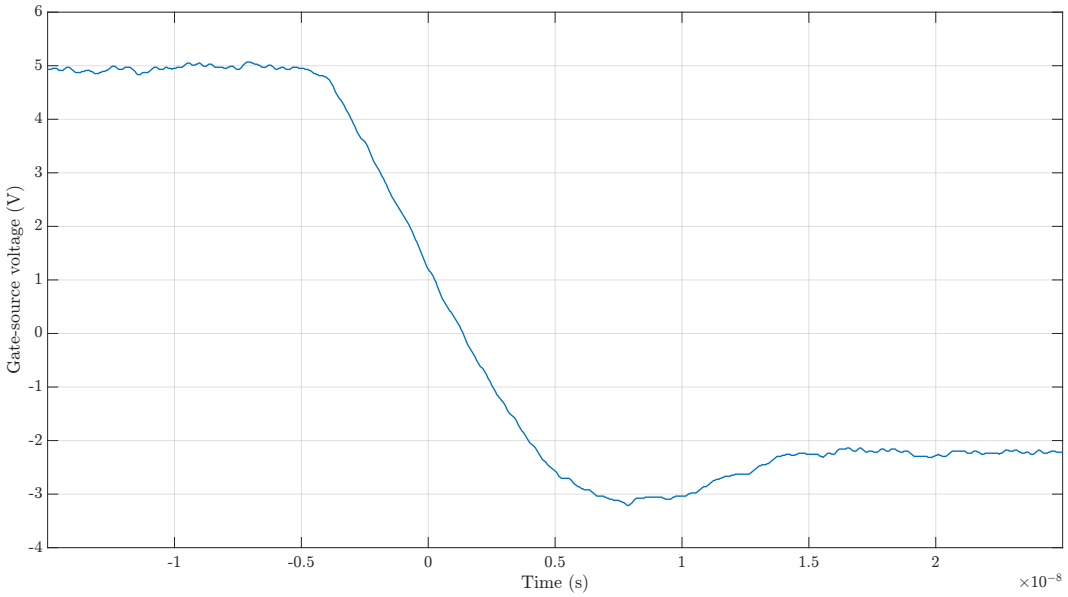


Figure 5.2 – Falling waveform of the gate-source voltage V_{gs}.

In figure 5.2 shows the V_{gs} falling waveform. The voltage falls from 5 V to −2.2 V, complementarily of what was obtain in test explained in 5.1. There is an undershoot that brings the V_{gs} below −3 V, this behavior is caused by parasitic L-C elements at the driver gate that make the V_{gs} oscillating. It is possible to avoid this phenomena increasing the off-gate-resistance $R_{G,off}$, that acts as a dumper in a RLC circuit composed by the parasitics shown in figure 4.10. The additional resistance should prevent these oscillations despite an increase of V_{gs} falling time, that will reduce the overall switching speed.

5.2 Output Voltage

As aforementioned, the H-bridge module is capable of giving as output a 3-levels voltage waveform. To test this feature have been generated, using the oscilloscope's internal function generator, two distinct PWM square-waves to drive the four inverter's switches. Next figure shows the H-bridge output voltage obtained by driving the inverter with a 10 kHz switching frequency f_s and an input voltage V_{in} of 2.25 V.

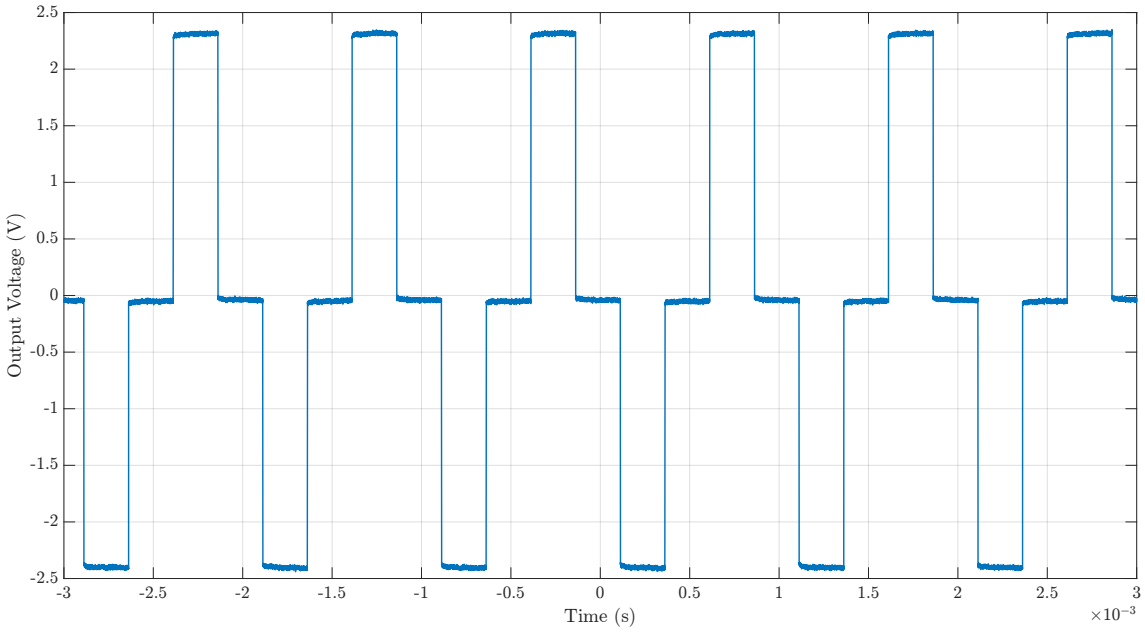


Figure 5.3 – Three-level output voltage obtained with the H-bridge PCB prototype.

The results obtained from the output voltage are satisfactory. The voltage switches from one value with the other without disturbances or oscillations, and the steady values between one transition and the other are kept constants without ringings.

5.3 Rising and Falling of the V_{gs} with the Application of a DC Input Voltage

In this test, a DC input voltage with different values has been applied at the H-bridge input in order to evaluate the gate driver response stability in different input conditions. The application of a DC input voltage, which was left out from the tests 5.1 can cause disturbances, nevertheless the results to be expected are a good quality V_{gs} waveform. Figure 5.4 and figure 5.5 show the rising and falling of the V_{gs} with a H-bridge input voltage V_{in} of 15 V.

Rising of the V_{gs} with the Application of a DC Input Voltage

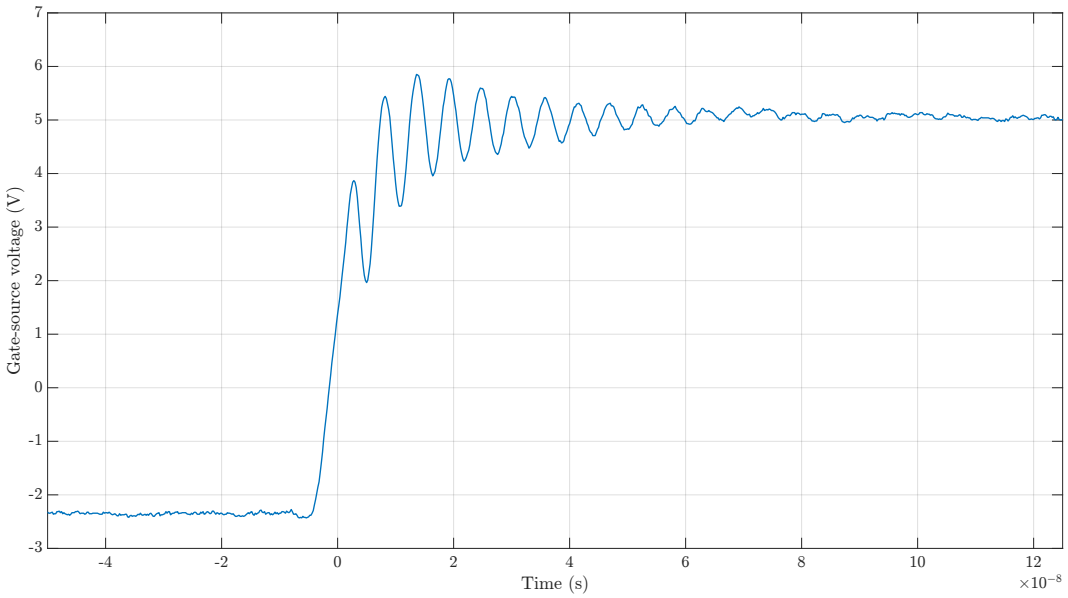


Figure 5.4 – Rising waveform of the gate-source voltage V_{gs} with a DC input of 15 V.

Is it possible to see in figure 5.4 how the waveform of the rising V_{gs} got worse compared with the one shown in figure 5.1 The application of a input voltage increases the disturbances and the oscillations of the gate source voltage. Is it possible to notice a undershoot that brings the V_{gs} almost below the value 2 V, at this voltage the GaN conductivity is seriously reduced, almost brought to an open circuit, in fact the switch threshold voltage V_{th} is 1.25 V. It is also important to notice that there are dangerous voltage overshoots, a 6 V value is almost reached, which is equal to the maximum gate-to-source voltage applicable to the device. It was not possible to increase the input voltage V_{in} to higher values than 15 V in order to not harm the switches. This is the maximum input voltage that can applied at the inverter's input, in these actual conditions, without damaging the switches. This is unfortunate because the prototype was designed to operate at voltages up to 100 V. To solve this issue it is possible to increase the ON-gate resistance $R_{G,ON}$, this should control better the under/overshoots, allowing to operate the device with higher input voltages.

Falling of the V_{gs} with the Application of a DC Input Voltage

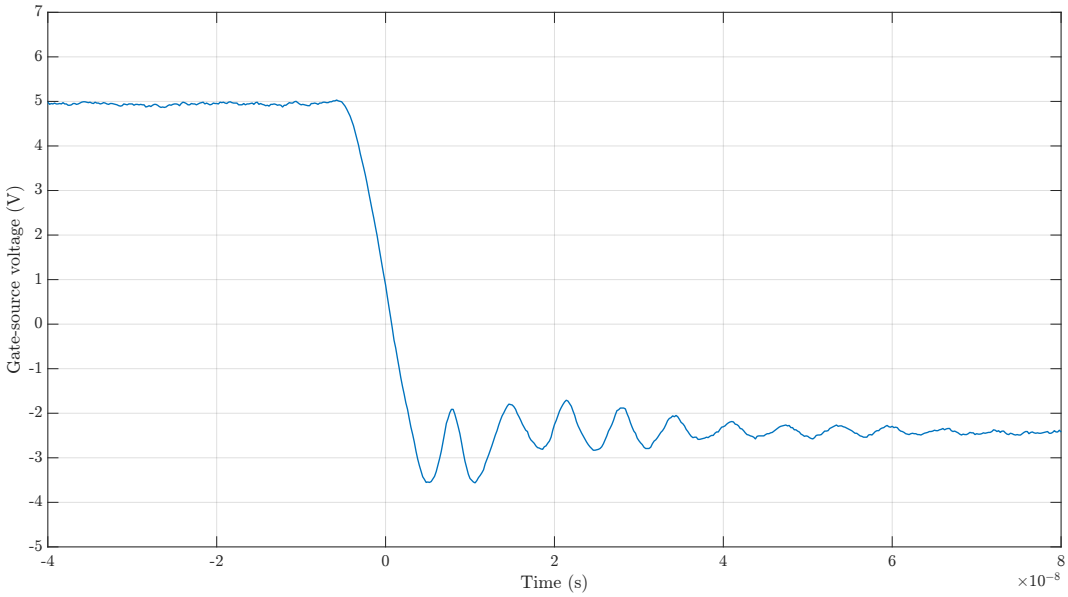


Figure 5.5 – Falling waveform of the gate-source voltage V_{gs}.

Likewise the previous test, the falling waveform of the V_{gs} got worse after the application of a DC input voltage. It is possible to notice, from figure 5.5 that some undershoots are present in the V_{gs} falling waveform. The minimum gate-source voltage of the device is $-4\,\mathrm{V}$, seriously close to the one obtained in the test, risking to damage the switch. However, it is possible to see how, thanks to the application of the negative voltage in the OFF-procedures, the overshoots are well kept under the V_{th}, avoiding undesired Miller activation.

5.4 R-L Load

The last test that has been conducted allows to evaluate the prototype performances after the application of a R-L circuit at its output terminals. The load consists in an inductor and a digital load, that simulates a resistance. The results obtained with this test showed a peak-to-peak output voltage unexpectedly lower than the peak-to-peak input voltage. This was caused by a partial overlapping of the switches, that caused some shortcuts that reduced the output voltage value. The function generator that has been used to generate the switching pulses didn't allow to set a dead time between one switching operation and the other, this caused the unhealthy switching operations that reduced the amplitude of the output voltage The voltage expected at the inverter's output terminals would have oscillate between 0 and V_{dc} and because of the partial overlapping of the switches, caused by the absence of the dead time, the maximum voltage value obtained as output was approximately $+V_{\mathrm{dc}}/2$. In order to proceed with further tests, it is fundamental to implement a better switching pulses generating strategy, using microcontrollers that can allow to set the PWM dead time digitally or using external circuitry that can analogically set the dead time.

5.5 Prototype Thermal Behavior

To evaluate the thermal behavior of the prototype, the digital load has been set to absorb a high current (I_{out}), in this best way it is possible to raise the temperature of the PCB components, to study their response to the heat caused by the Joule effect. Pictures obtained with a thermal camera help enlightening the hotspots and eventually spot areas unexpectedly affected by high temperatures. The picture below has been taken with a input DC voltage V_{in} of 8.1 V and a output current I_{out} of 13.2 A, which is a greater value than the current that will pass through the inverter while feeding the single phase of the 9-phase PMSM.

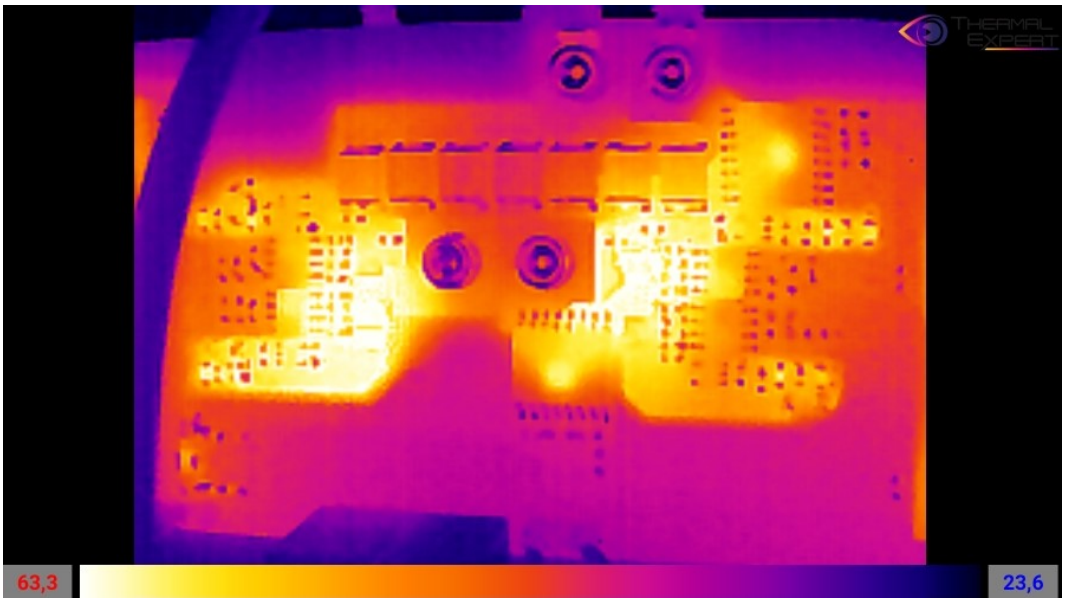


Figure 5.6 – Thermal image of the PCB.

As expected, the areas in which GaN FETs are located are the hottest zones. The drivers surrounding areas, which are populated by the additional driver circuitry also enlighten high temperatures. The current that flows in narrow traces, corresponds to the one passing through the power loop generates this unexpected heat. A possible solution to reduce the temperature in these areas could be enlarging the copper traces on which the additional driver components are located, in this way the current will flow in a circuit with reduced impedance, resulting in smaller Joule losses. Also, thanks to a wider trace, the heat dissipation will improve because of an higher heat transmission surface. There are two more zones in which it is possible to see high temperatures: where the current sensors are located. The heat is mainly generated by the current that is flowing through them and also by their internal circuitry. It is important to say that the thermal analysis did not bring to light any criticality about the PCB thermal behavior.

6 Conclusions

This thesis has presented a 5-level cascaded H-bridge alongside with various voltage and current control strategies. A prototype has been made and tested; the realization process, from the choice of the components to the testing results has been deeply analyzed and explained.

A detailed and deep analysis on power inverters and multilevel inverters has been conducted to enlighten strong points, advantages and disadvantages of the different topologies. A wide range of simulation have been carried through, with the aim of controlling the output current and voltage generated by the inverter. To understand better the 5LCHBI working principle, open-loop strategies have initially been simulated with the subsequent implementation of closed loop techniques. A novel current control algorithm based on the multiband hysteresis control has been developed and tested in MATLAB-SIMULINK. To evaluate the response and the stability of the purposed techniques, dynamical changes have been introduced in the system. Some experiments have been carried out to study the behavior of the system feeding a load that simulates a single phase of a PMSM machine. All the results obtained from the tests have been analyzed and discussed also from the point of view of the power quality.

The realization process of the device has been deeply explained, the components choice and the architecture selection have been deeply described and argued. A guideline about the PCB scheming and design was given, along with considerations about the parasitic elements reduction.

The last part was focused on the prototype testing procedures, the obtained results have been explained and discussed, showing the strong and weak points of the prototype, alongside with some possible improvements that can be applied, to solve some back draws and to obtain better results in future research and tests.

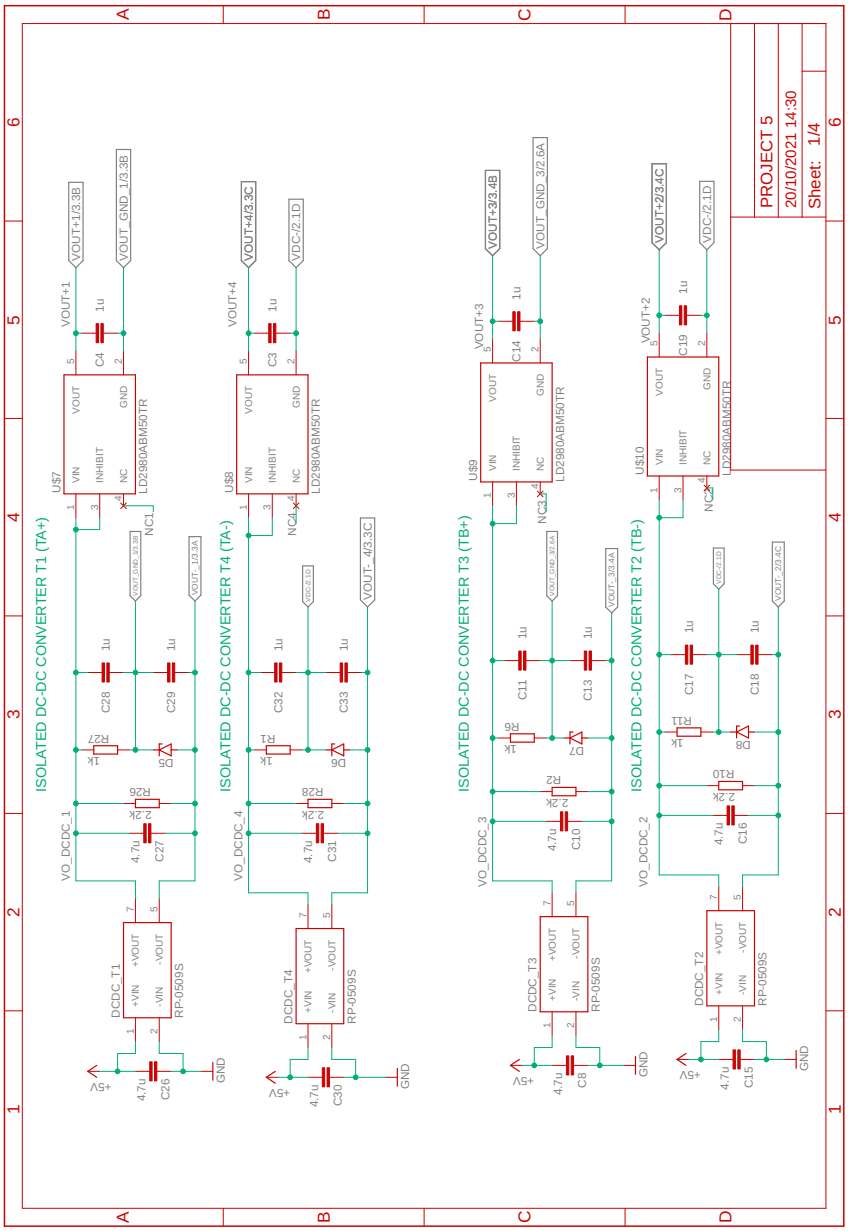
6.1 Future Work

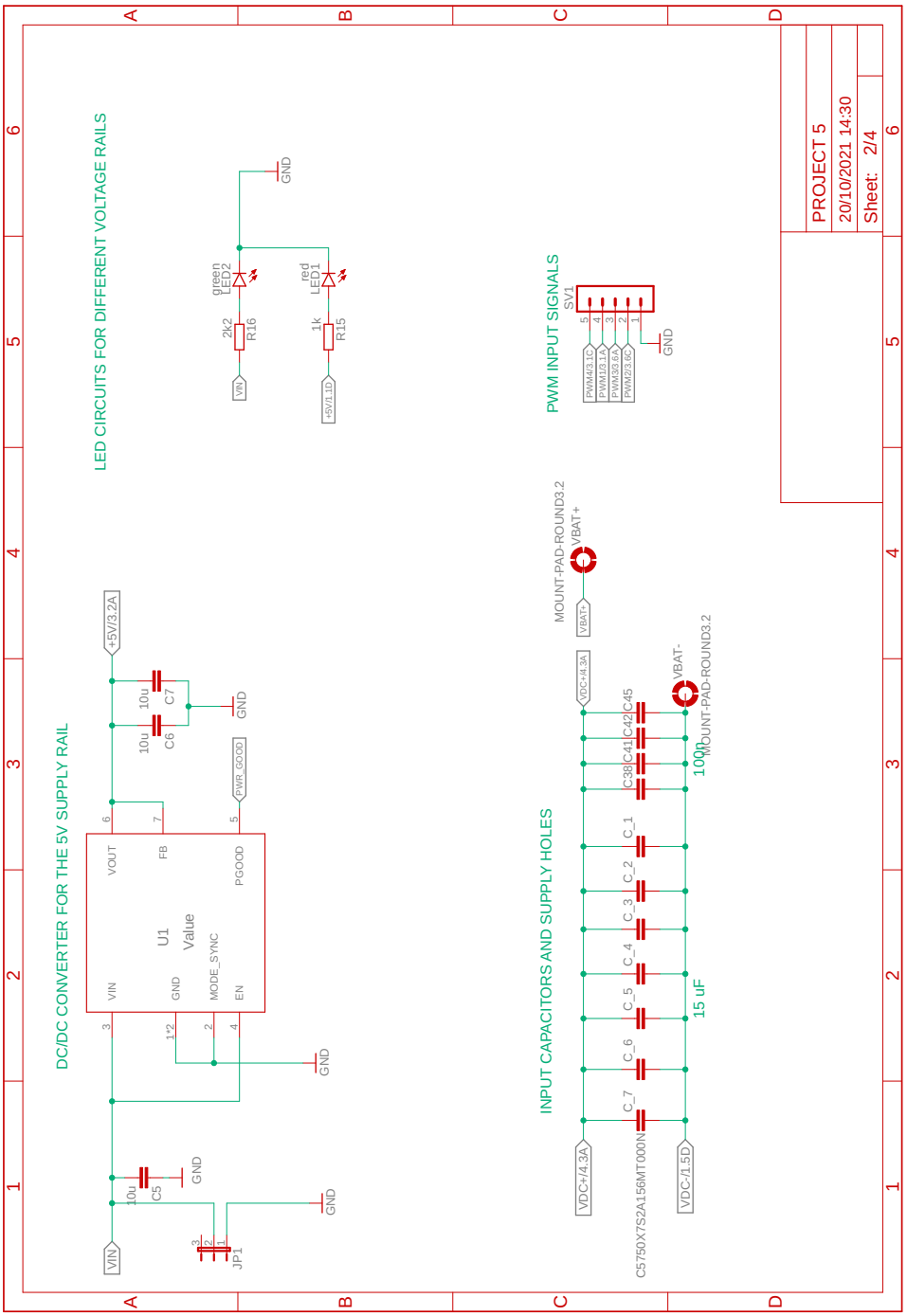
The control strategies and the manufactured prototype are expected to be useful in the development of the nine-phase permanent magnet synchronous motor drive. The future effort has to be put in the adaptation and extension of the purposed control strategies aiming at driving a multiphase PMSM and also to enhance the inverter prototype.

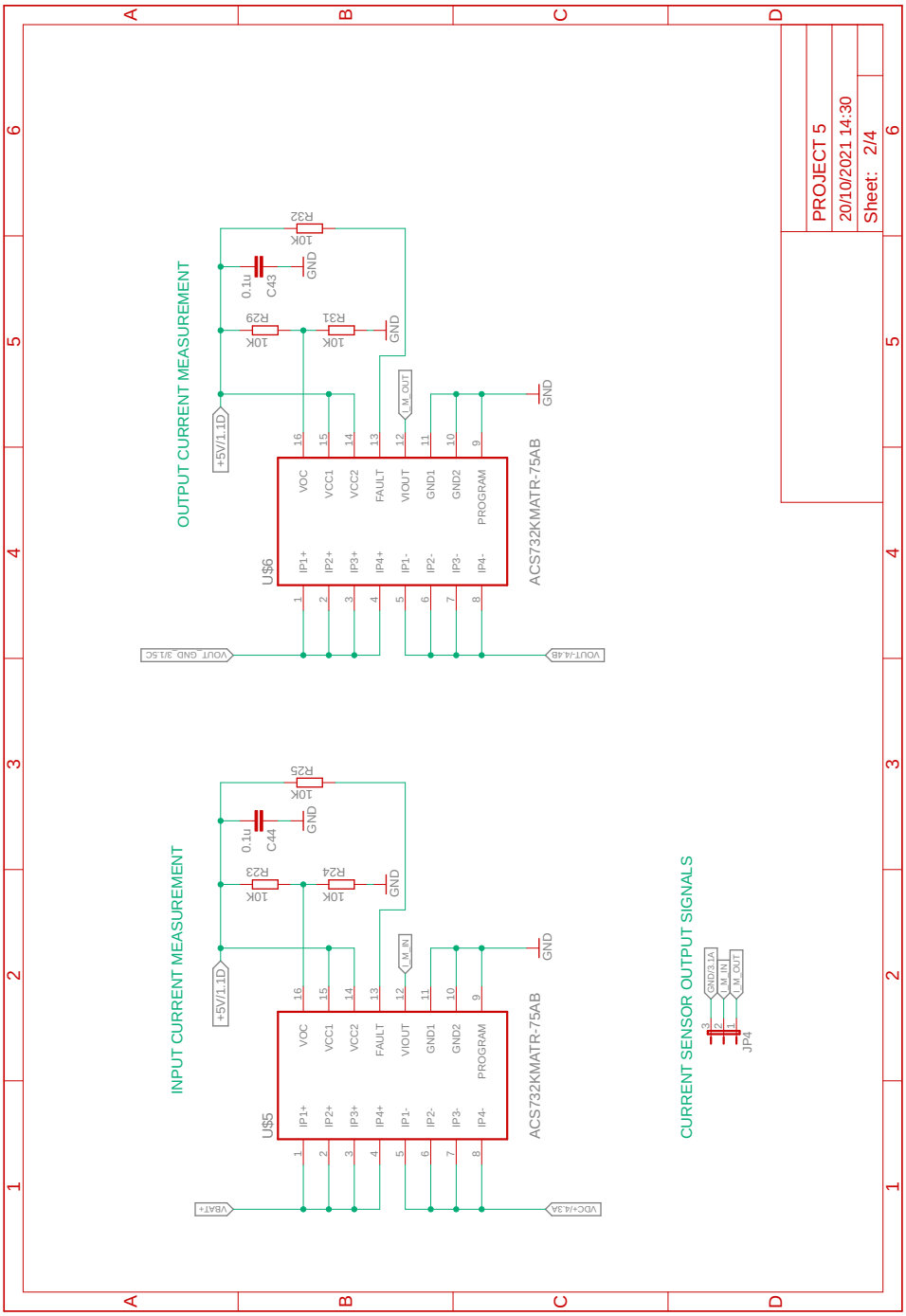
Future research should aim at achieving the following aspects:

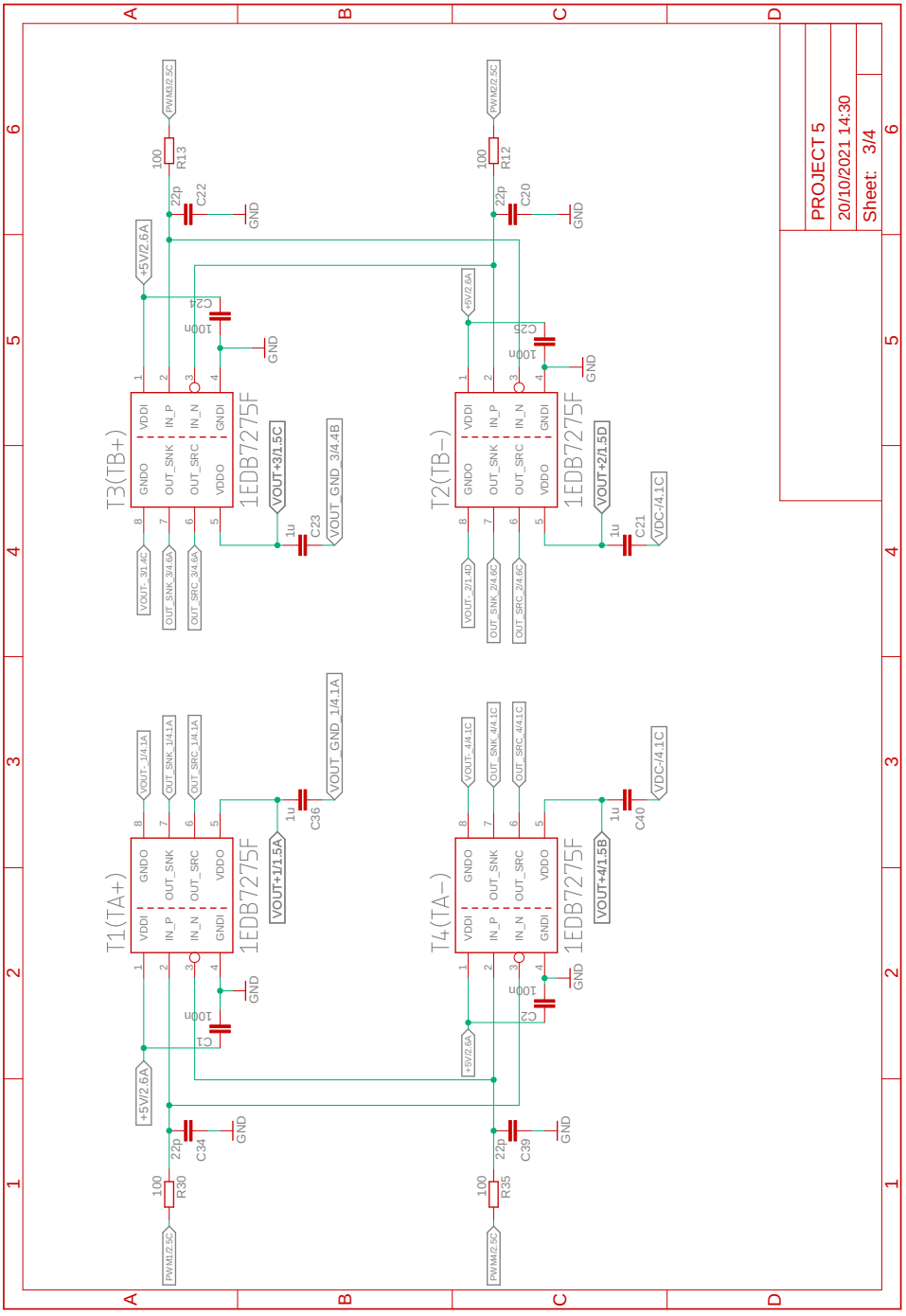
- It is necessary to identify the most suitable control strategy that in future will drive the electric machine.
- It is necessary to extend and the selected control strategy to a single phase of the PMSM machine, to subsequently drive to all the nine PMSM phases with nine 5LCHBI.
- Some PCB components have to be replaced, for example the ON/OFF gate driver resistances, in order to obtain more stable V_{gs} rising and falling; to guarantee the full operativity of the prototype at higher input and load conditions.
- More tests must be conducted to evaluate the common mode voltage.
- More tests must be conducted to measure the input and output current with the PCB integrated current sensors.
- The voltage of the Zener diode, present in the additional driver circuit, has to be set optimally.
- Further tests must be conducted for evaluating the 5LCHBI performances, thus connecting in series two H-bridge prototypes.
- To improve the insulation between the PCB stages, it is possible to place the ISO DC/DC capacitors vertically above and below to the driver; this solution will allow to draw the power traces in a more optimal way, guaranteeing a better insulation between power and driver side in case of failures.

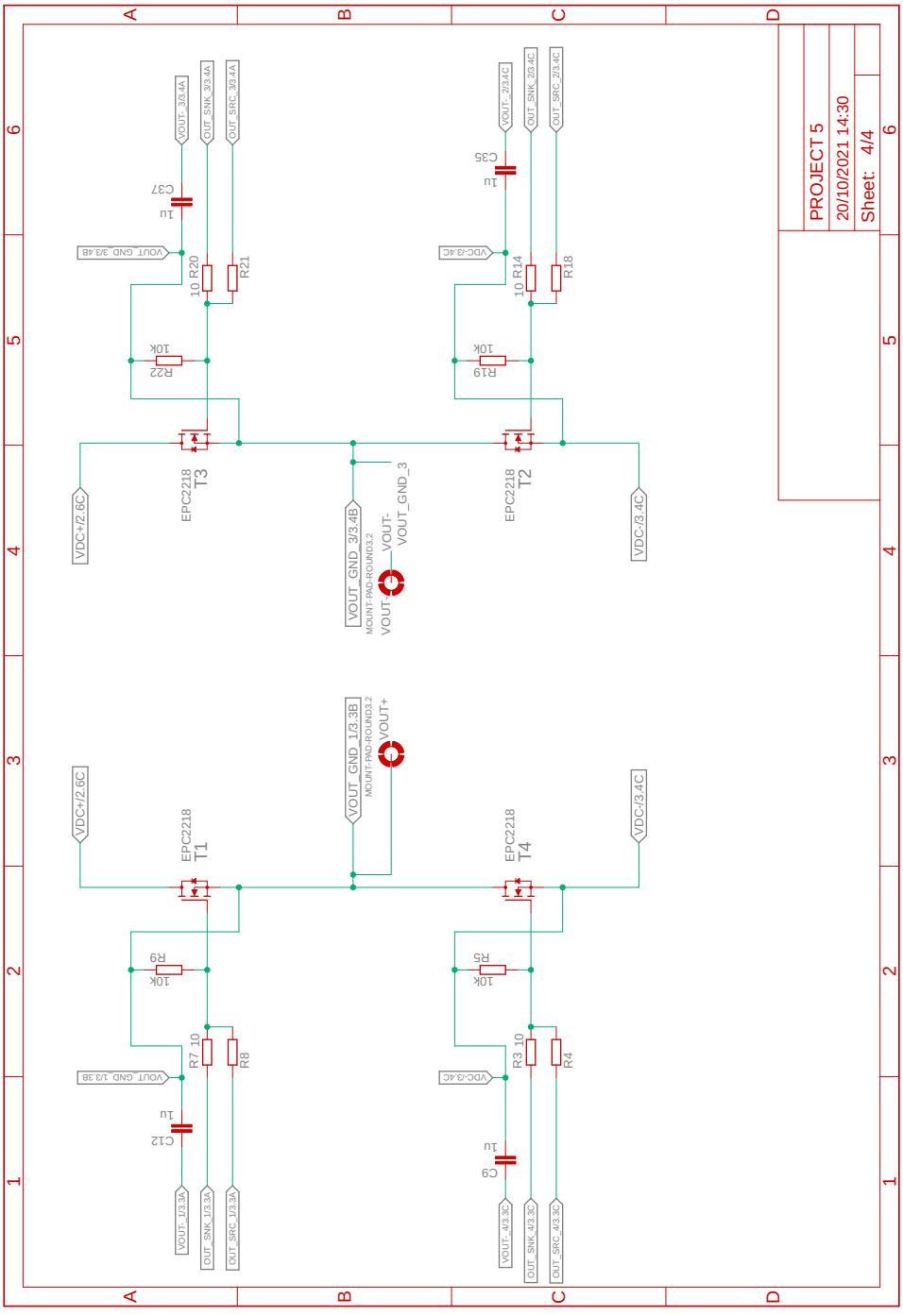
A Schematics for the PCB




LED CIRCUITS FOR DIFFERENT VOLTAGE RAILS
green
LED2
red
LED1
2k2
R16
1k
R15
GND
VIN
+5V/1.1D
PWM INPUT SIGNALS
SV1
PWM43.1C
PWM13.1A
PWM33.6A
PWM23.6C
GND
DC/DC CONVERTER FOR THE 5V SUPPLY RAIL
+5V/3.2A
10u
C7
C6
GND
PWR_GOOD
U1
Value
VIN
GND
MODE_SYNC
EN
VOUT
FB
PGOOD
1*2
C5
JP1
INPUT CAPACITORS AND SUPPLY HOLES
MOUNT-PAD-ROUND3.2
VBAT+
VDC+/4.3A
VBAT-
C38
C41
C42
C45
100n
C_1
C_2
C_3
C_4
C_5
C_6
C_7
15 uF
C5750X7S2A156MT000N
VDC-/1.5D
PROJECT 5
20/10/2021 14:30
Sheet: 2/4


PROJECT 5
20/10/2021 14:30
Sheet: 2/4
OUTPUT CURRENT MEASUREMENT
INPUT CURRENT MEASUREMENT
CURRENT SENSOR OUTPUT SIGNALS
ACS732KMATR-75AB
U$6
U$5
JP4
+5V/1.1D
GND
I_M_OUT
I_M_IN
VOUT-/4.4B
VDC+/4.3A
VBAT+
R32
R29
R31
R25
R23
R24
C43
C44
0.1u
10K


PROJECT 5
20/10/2021 14:30
Sheet: 3/4
T3(TB+)
T2(TB−)
T1(TA+)
T4(TA−)
1EDB7275F
VDDI
IN_P
IN_N
GNDI
GNDO
OUT_SNK
OUT_SRC
VDDO
+5V/2.6A
GND
VOUT+3/1.5C
VOUT+2/1.5D
VOUT+1/1.5A
VOUT+4/1.5B
VOUT_GND_3/4.4B
VOUT_GND_1/4.1A
VDC/4.1C
PWM2/2.5C
PWM1/2.5C
R13
R12
R30
R35
C22
C20
C34
C39
C24
C25
C1
C2
C23
C21
C36
C40
100
22p
100n
1u


PROJECT 5
20/10/2021 14:30
Sheet: 4/4
EPC2218 T1
EPC2218 T2
EPC2218 T3
EPC2218 T4
VDC+/2.6C
VDC-/3.4C
VOUT_GND_1/3.3B
VOUT_GND_3/3.4B
VOUT+
VOUT-
VOUT_GND_3
R7 10
R8
R9 10K
R3 10
R4
R5 10K
R20 10
R21
R22 10K
R14 10
R18
R19 10K
C12 1u
C9 1u
C37 1u
C35 1u
VOUT_GND_1/3.3B
VOUT_GND_3/3.4B
VDC-/3.4C
VOUT-_1/3.3A
OUT_SNK_1/3.3A
OUT_SRC_1/3.3A
VOUT-_4/3.3C
OUT_SNK_4/3.3C
OUT_SRC_4/3.3C
VOUT-_3/3.4A
OUT_SNK_3/3.4A
OUT_SRC_3/3.4A
VOUT-_2/3.4C
OUT_SNK_2/3.4C
OUT_SRC_2/3.4C

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