Università degli Studi di Padova

Master of Science in Electronic Engineering

Modeling and Control of a Tapped-Inductor Buck Converter with Pulse Frequency Modulation

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Ai miei genitori.

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Chapter 1

Introduction

1.1 Auxiliary power supply for cascaded converter submodules

Cascaded-bridge converters, i.e. converters consisting of a large number of identical submodules, have recently shown to be a very promising solution for many high-voltage high-power grid applications, such as:

- modular multilevel converters (M2C) for high-voltage direct-current transmission (HVDC) [1, 2, 3, 4, 5];
- supplies for electric railway systems [6, 7];
- cascaded H-bridge converters (CHB) [8] for flexible AC transmission system (FACTS) applications.

One of the prominent advantages of cascaded converters is the splitting of the voltage blocking capability among the converter submodules, making series connection of devices in a single valve unnecessary. A simplified schematic diagram of a M2C, implemented with half-bridge submodules, is shown in Figure 1.1. The submodule schematic, which includes GDUs and the power supply unit (PSU) is also shown.

For high-voltage applications there is an incentive to increase the voltage blocking capability of each submodule in order to reduce the number of submodules and the per-submodule associated costs. As the submodule voltage blocking capability is increased certain issues become harder to address, even in cases where series-connection is not used within the valves. One such issue is the supply of power to gate driver units (GDUs) and control circuitry. These auxiliary power supplies, which have an influence on the reliability and efficiency of the complete converter system, have not been developed properly.

The auxiliary power requirement for M2C [9, 10, 11] submodules depends on the specific submodule topology and the switching device. The power consumption of a GDU ranges from few watts for an Insulated Gate Bipolar Transistors (IGBTs) switch to a few tens of watts for an Integrated Gate Commutated Thyristors (IGCTs). By considering also the power requirement for the control and communication circuitry, the overall power requirement for a submodule equals $5 - 100$W.

The PSU of each submodule must provide the power as quickly as possible, especially at low energy levels, in order to allow the investigation of fault conditions

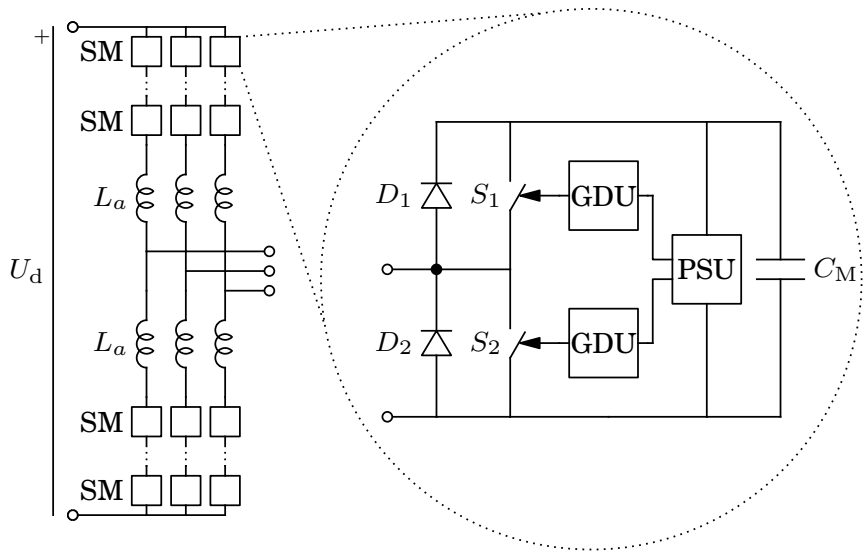

Figure 1.1: Modular multilevel converter topology with half-bridge submodule showing auxiliary power supply unit (PSU) and gate drive units (GDU).

and erroneous behavior in the submodule at non-dangerous conditions. Furthermore, the PSU should be sufficiently reliable so that the failure rate of the submodule is not appreciably reduced.

Since the voltage across the main DC capacitor of the submodule could be few kilovolts, the design of the PSU could not be trivial. The use of low-power high-voltage large step-down ratio converters have been limited to special applications, which are not commonly available.

The tapped-inductor buck (TI-buck) converter [12] is a suitable solution for the application of interest. This converter topology allows for an auxiliary converter with only one high-voltage valve, which features autonomous operations [13]. Furthermore, the TI-buck could find use as an efficient and reliable auxiliary power supply in cascaded bridge converters.

The TI-buck converter implements only the first stage of the PSU, where the voltage is converted from several kilovolts to roughly 100V. The second stage of the PSU consists of a secondary converter, which features an output voltage which satisfies the specific GDU requirements, e.g. 24V. The presence of a second stage relaxes the requirements on the TI-buck output voltage waveform, i.e. high variability of the output voltage is tolerated. Since the secondary converter features common specifications, it can be implemented with a standard step-down converter with galvanic isolation.

The studied TI-buck converter operates in discontinuous conduction mode (DCM) and the high-side switch is operated in a fixed peak-current mode. Therefore, at each switching cycle a nearly constant energy is delivered to the output. Therefore, the output voltage can be controlled by varying the switching frequency, i.e. by using a Pulse Frequency Modulation (PFM).

1.2 Project description

The department of Electrical Energy Conversion at the KTH Royal Institute of Technology is focused on research and education in power electronics and electrical machines and drives. One research area is focused on cascaded-bridge converters for high-voltage high-power grid applications.

A large step-down ratio tapped-inductor buck converter auxiliary power supply for cascaded converter submodules has been developed with main focus on the high-side valve design [13] and the tapped inductor design [14].

The present project is focused on improving the TI-buck converter, specifically:

- deepen the study of the converter, both static and dynamic analysis;
- design a closed-loop output voltage control system, which uses the switching frequency as a control variable, i.e. Pulse Frequency Modulation (PFM);
- implement the control system with a low-power micro-controller;
- build and test a scaled prototype of the converter;
- analyze and achieve the start-up of the converter.

The project is described in detail in the present report, which is organized as follow:

Chapter 1: Introduction

Chapter 2: Large step-down ratio TI-buck converter
The converter is described in detail and an average output current model is proposed.

Chapter 3: Closed-loop control design
The design of the closed-loop output voltage control system with a micro-controller implementation is illustrated.

Chapter 4: Experimental verification
The results of the converter testing are shown and a solution for the start-up is illustrated.

Chapter 5: Conclusion

Chapter 2

Large step-down ratio TI-buck converter

2.1 Topology considerations

Buck converter

There is a multitude of non-isolated step-down converter topologies that can be considered for this application. The first topology considered for a non-isolated step-down converter is the buck converter, shown in Figure 2.1. However, in high-voltage, low-power applications, the buck converter has some significant drawbacks. Especially, both the switch and the diode must be able to block the input voltage

$$\hat{v}_S = v_i \tag{2.1a}$$

$$\hat{v}_D = v_i \tag{2.1b}$$

where $\hat{v}_S$ denotes the maximum voltage stress of the switch and $\hat{v}_D$ denotes the maximum voltage stress of the diode.

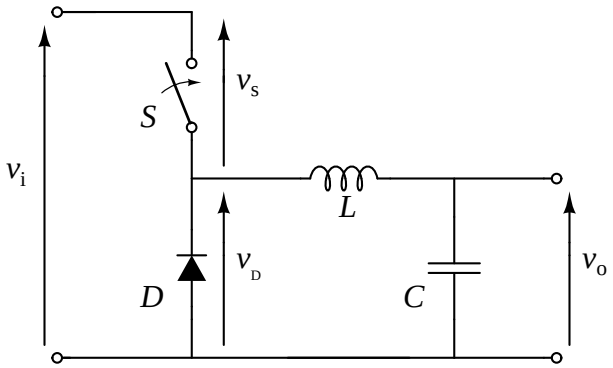

Figure 2.1: Buck converter topology.

Tapped-inductor buck converter

Unlikely the standard buck converter, the TI-buck converter topology, shown in Figure 2.2, allows to greatly reduce the stress of the diode, thanks to the tapped-inductor transform action. On the other hand, the voltage stress of the switch is increased, but since this is an large step-down ratio application, where $v_i >> v_o$,

this is not a relevant drawback. The maximum voltage stress of the switch and the diode can be expressed as

$$\hat{v}_S = v_i + N v_o \tag{2.2a}$$

$$\hat{v}_D = v_i + \frac{1}{1+N}(v_i - v_o) \tag{2.2b}$$

where the factor $N = \frac{N_1}{N_2}$ denotes the turns ratio of the tapped-inductor. These relations are shown graphically in Figure 2.3.

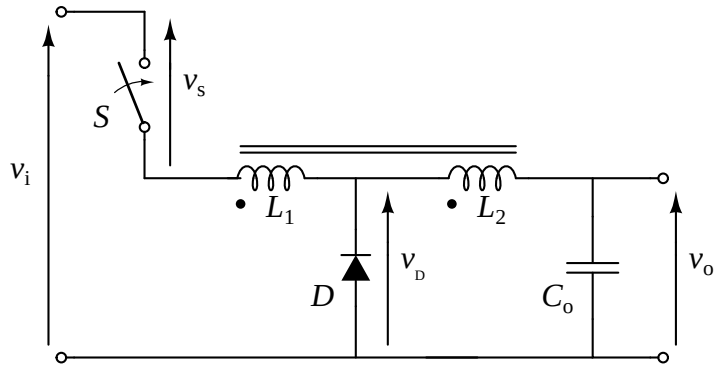

Figure 2.2: Tapped-inductor buck converter topology.

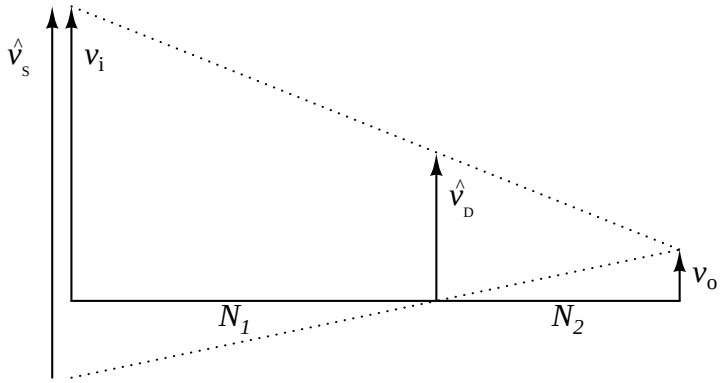

Figure 2.3: Illustration of the relation between turns ration $N = \frac{N_1}{N_2}$, input voltage v_i, output voltage v_o, switch voltage stress $\hat{v}_S$ and diode voltage stress $\hat{v}_D$.

The TI-buck converter topology allows another considerable advantage. If the diode is replaced with a synchronous rectifier, then it is possible to turn on the main switch with zero voltage switching (ZVS) [15, 16]. The ZVS condition is achieved by turning on the synchronous rectifier before turning on the main switch, which allows to store energy in the tapped-inductor. As soon as the synchronous rectifier is turned off, a resonance between the tapped-inductor and the main switch snubber capacitance decreases the voltage over the main switch, until it is reverse biased. An in-depth description of the TI-buck operation is presented in Section 2.2. Figure 2.4 shows the TI-buck converter with current injection topology.
In the studied TI-buck, developed in [13, 14], the ZVS condition is sensed by the main switch, which turns on autonomously. Furthermore, by operating in peak-current mode, the main switch can turn off independently, becoming a completely autonomous device. A detailed description of the main switch operation is presented in Section 2.3.

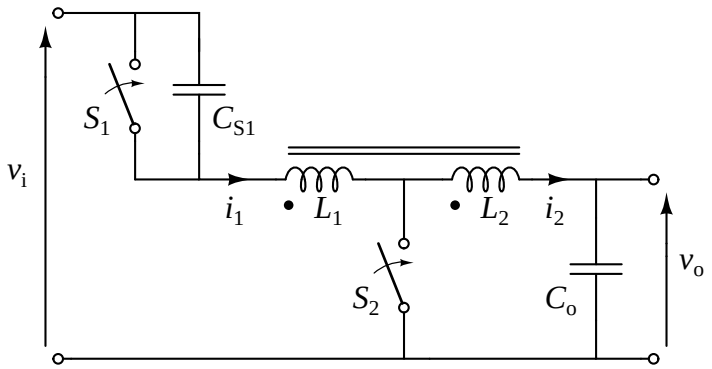

Figure 2.4: Tapped-inductor buck converter with current injection topology.

Component stress

With reference to Figure 2.4, equations (2.2a) and (2.2b) become

$$\hat{v}_{S1} = v_i + N v_o \tag{2.3a}$$

$$\hat{v}_{S2} = v_o + \frac{1}{1+N}(v_i - v_o) \tag{2.3b}$$

where $\hat{v}_{S1}$ denotes the maximum voltage stress of the main switch and $\hat{v}_{S2}$ denotes the maximum voltage stress of the synchronous rectifier.

By choosing an appropriate tapped-inductor turns ratio N, the voltage stress of the synchronous rectifier (2.3b), also called low-side switch (LS-SW), can be greatly reduced, if compared with (2.1b). Therefore, the LS-SW can be realized utilizing a single high-voltage super-junction MOSFET.

Differently, the main switch, also called high-side switch (HS-SW), must be able to block the input voltage plus N times the output voltage, according to (2.3a). A high block capability can be achieved by series-connected switch devices. Therefore, the HS-SW consists of N_{cell} switching cells, connected in series. Each cell contains a high-voltage super-junction MOSFET, which must be able to block

$$\hat{v}_{cell} = \frac{v_i + N v_o}{N_{cell}} \tag{2.4}$$

By using several series-connected switching cells, the HS-SW can handle rather high voltage stress. On the other hand, a high value of N_{cell} represent a challenge for the HS-SW design. The requirements on the HS-SW cells turn-off synchronization are strict, in order to achieve (2.4). A non-synchronized turn off leads to an unequal distribution of the voltage stress through the cells, which can cause break-down failure of the MOSFETs, due to the excessive voltage stress. With the HS-SW design adopted in the studied converter, N_{cell} is approximately limited to few units, e.g. $N_{cell} \leq 10$.

Since this is a low power application, the current stress of the components is not a relevant issue. The converter operates in peak-current mode and the maximum values of the currents are

$$\hat{i}_1 = \frac{I_p}{1+N} \tag{2.5a}$$

$$\hat{i}_2 = I_p \tag{2.5b}$$

where I_p denotes the peak output current. A high value of I_p can lead to the saturation of the tapped-inductor magnetic core. Therefore, I_p must be limited to an appropriate value.

2.2 Converter operation

The analyzed TI-buck converter operates in discontinuous conduction mode DCM, i.e. the current through the inductance is null at the beginning of each switching cycle. Figure 2.5 shows the TI-buck converter during each operation, while Figure 2.6 shows the significant waveforms. With reference to these figures, the operation of the studied TI-buck converter is described in the following.

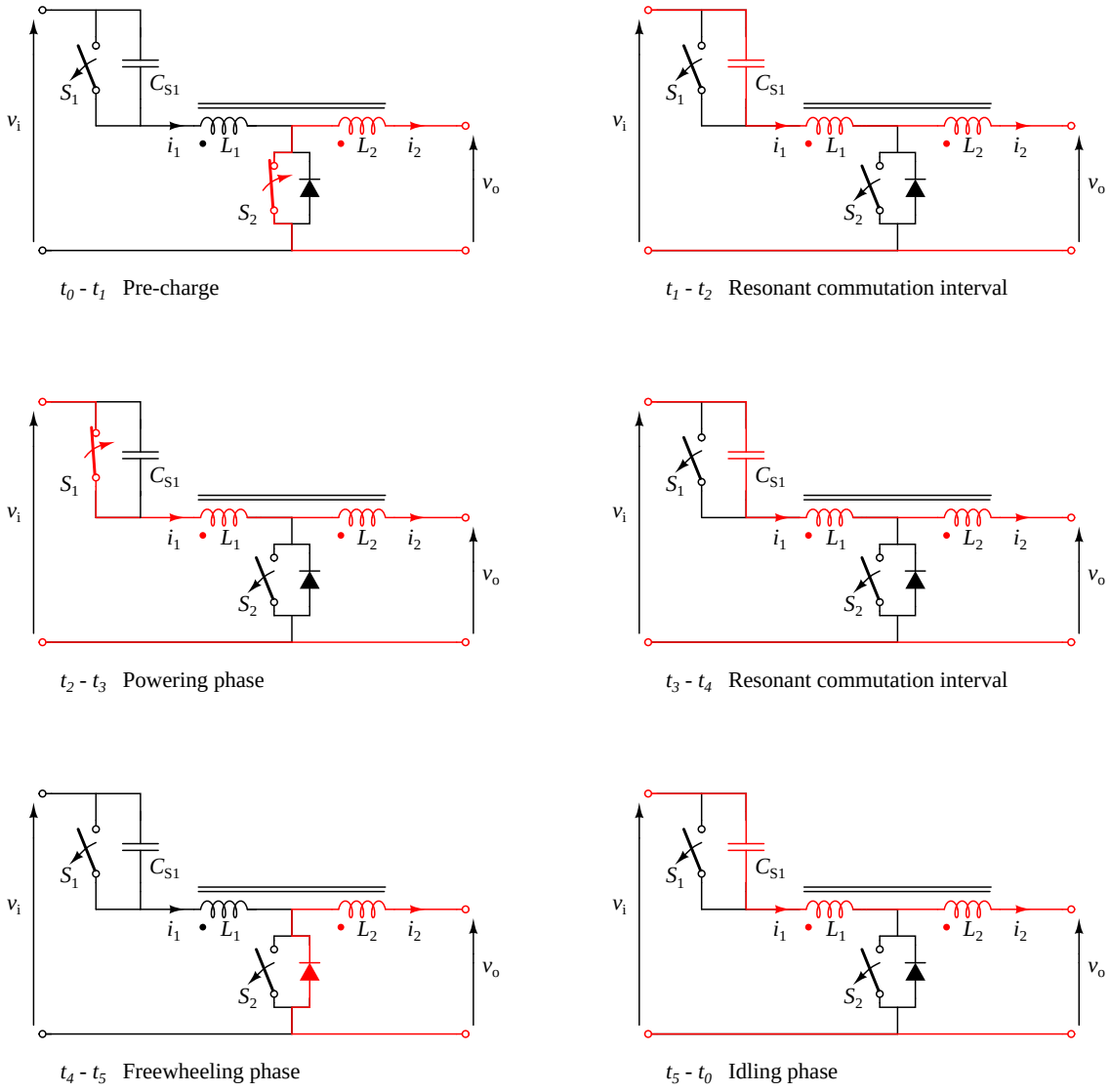

Figure 2.5: Tapped-inductor buck converter operation states.

$t_0 - t_1$ Pre-charge

The pre-charge phase aims at storing energy in the tapped-inductor, which will flow toward the main switch snubber capacitance, C_{S1}, during the next phase, allowing ZVS of the HS-SW.
At t_0 the LS-SW, S_2, is turned on. The voltage over L_2 is reflected in the voltage over L_1, according to the tapped-inductor turns ratio. Therefore, the voltage over the HS-SW, S_1, quickly reaches the maximum value (2.3a).

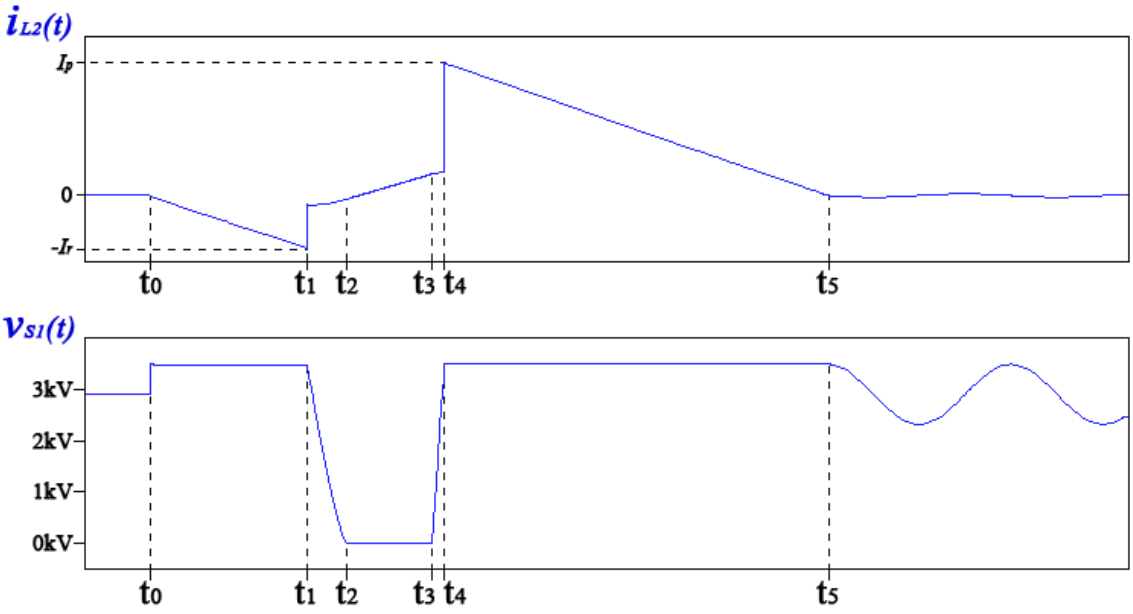

Figure 2.6: Waveform describing the converter operation.

The output current, i_2, decreases linearly as

$$\frac{\mathrm{d}i_2}{\mathrm{d}t} = -\frac{v_o}{L_2} \tag{2.6}$$

If the tapped-inductor coupling factor is less than unity, then there will be some ringing between the primary leakage inductance and C_{S1}.

$t_1 - t_2$ Resonant commutation interval

S_2 turns off when $i_2 = -I_r$, then the current decreases by a factor $\frac{1}{1+N}$ and flows through both windings $i = i_1 = i_2$. A detailed description of the current behaviour when S_2 switches is given is Appendix A. A resonant commutation interval starts, whereby energy is transferred between L_{tot} and C_{S1}. With reference to Figure 2.7, the resonant commutation interval is described by the following equations

$$i(t) = C_{S1}\frac{\mathrm{d}v_{S1}(t)}{\mathrm{dt}} \tag{2.7a}$$

$$v_L(t) = L_{tot}\frac{\mathrm{d}i(t)}{\mathrm{dt}} \tag{2.7b}$$

$$v_i - v_o = v_{S1}(t) + L_{tot}C_{S1}\frac{\mathrm{d}^2}{\mathrm{dt}^2}v_{S1}(t) \tag{2.7c}$$

Initial conditions

$$v_{S1}(t_1) = v_i + Nv_o \tag{2.8a}$$

$$i(t_1) = -\frac{I_r}{1+N} \tag{2.8b}$$

The voltage across the high-voltage switch can be expressed as:

$$v_{S1}(t) = V_{S1}\sin(\omega_0 t + \varphi) + (v_i - v_o) \tag{2.9}$$

where:

$$V_{S1} = -\sqrt{v_o^2(N+1)^2 + \frac{L_{tot}}{C_{S1}}\frac{I_r^2}{(1+N)^2}} \tag{2.10a}$$

$$\omega_0 = \frac{1}{\sqrt{L_{tot}C_{S1}}} \tag{2.10b}$$

$$\varphi = \arctan\left[-\sqrt{\frac{C_{S1}}{L_{tot}}}\frac{v_o(1+N)^2}{I_r}\right] \tag{2.10c}$$

If the condition

$$|V_{S1}| > v_i - v_o \tag{2.11}$$

is verified, then the main switch S_1 can be reverse biased and ZVS can be achieved.

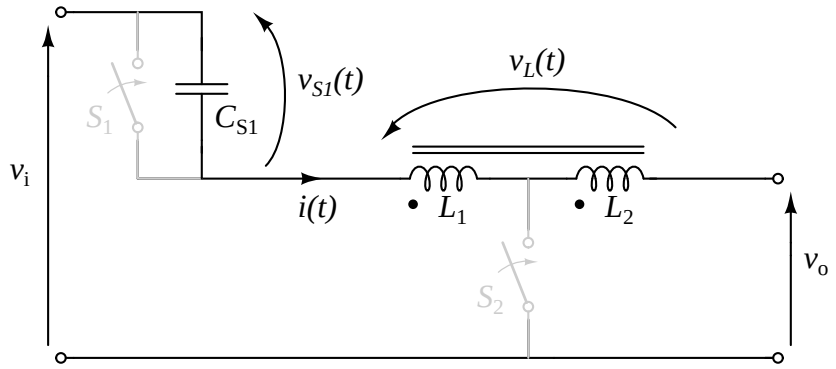

Figure 2.7: Tapped-inductor buck converter during the resonant commutation interval.

$t_2 - t_3$ Powering phase

The high-voltage switch S_1 senses the reverse bias condition and turns on. Similarly to a standard buck converter, during the powering phase the energy flows from the input to the output. The current through the tapped-inductor increases as

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{v_i - v_o}{L_{tot}} \tag{2.12}$$

$t_3 - t_4$ Resonant commutation interval

At a predetermined current level $i = \frac{I_p}{1+N}$, S_1 turns off autonomously. A resonant commutation interval starts, whereby energy is transferred between L_{tot} and C_{S1}. The resonance is described by equations (2.7a), (2.7b) and (2.7c), with initial conditions

$$v_{S1}(t_3) = 0 \tag{2.13a}$$

$$i(t_3) = \frac{I_p}{1+N} \tag{2.13b}$$

The voltage across the high-voltage switch increases as:

$$v_{S1}(t) = V_{S1}^I \sin(\omega_0 t + \varphi^I) + (v_i - v_o) \tag{2.14}$$

where:

$$V_{S1}^{I} = \sqrt{(v_i - v_o)^2 + \frac{L_{tot}}{C_{S1}} \frac{I_p^2}{(1+N)^2}} \tag{2.15a}$$

$$\varphi^{I} = \arctan\left[-\sqrt{\frac{C_{S1}}{L_{tot}}} (v_i - v_o) \frac{(1+N)}{I_p} \right] \tag{2.15b}$$

$t_4 - t_5$ Freewheeling phase

When S_2 is reversed bias, the LS-SW body diode turns on, clamping the voltage over S_1 to (2.3a). The current i_1 drops to zero and the current i_2 increases by a factor $(1 + N)$ in order to maintain ampere-turn balance. Then, the output current decreases linearly as (2.6).

$t_5 - t_0$ Idling phase

When the output current is null the LS-SW body diode turns off. Again, resonance between L_{tot} and C_{S1} occurs, as described by (2.7a), (2.7b) and (2.7c), with initial conditions

$$v_{S1}(t_5) = v_i + N v_o \tag{2.16a}$$

$$i(t_5) = 0 \tag{2.16b}$$

The voltage across the high-voltage switch evolves as:

$$v_{S1}(t) = V_{S1}^{II} \sin(\omega_0 t + \varphi^{II}) + (v_i - v_o) \tag{2.17}$$

where:

$$V_{S1}^{II} = v_o(1 + N) \tag{2.18a}$$

$$\varphi^{II} = \frac{\pi}{2} \tag{2.18b}$$

2.3 Main switch operation

In the studied TI-buck, the HS-SW is a completely autonomous device, which operates in a fixed, pre-programmed, peak-current mode. Each switching cell can sense the reverse bias condition and turn on. Differently, the turn off condition is sensed by a current-sense resistor R_{sense}. When the current through the HS-SW reaches the peak level, a Schmitt trigger provides the turn-off signal, which is propagated through the switch cells as a logic level signal. Figure 2.8 shows a simplified schematic of the HS-SW, while Figure 2.9 shows a simplified schematic of a switching cell. Transistor Q_2 consists in a high-voltage super-junction MOSFET, i.e. the switching device of the cell, with high blocking capability. Terminals $N_0 \div P_0$ to $N_{Ncell-1} \div P_{Ncell-1}$ connects the switching devices of the cell in series, while terminals $R_{IN\_0} \div R_{OUT\_0}$ to $R_{IN\_Ncell-1} \div R_{OUT\_Ncell-1}$ propagates the turn off signal through the cells. The $+$ and $-$ terminals are the only external connections of the HS-SW.

In Figure 2.9 the ground symbol indicates the local ground of the single cell. The local power supply of each switching cell consists in a capacitance, C_4, which is charged every switching cycle, during the reverse bias interval. The labels S and R denote the set and the reset terminals of the SR-latch respectively.

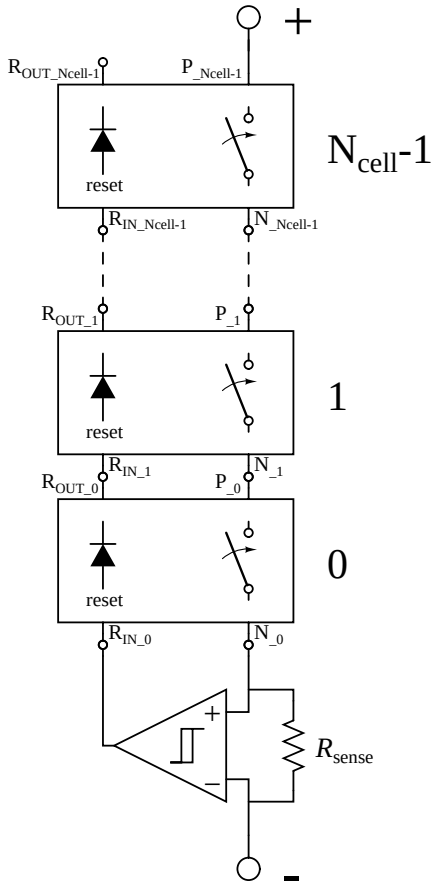

Figure 2.8: Simplified schematic of the HS-SW, showing the switching cells (numbered from 0 to $N_{cell} - 1$), the current sense resistor and the comparator used for the peak current control. The + and - terminals are the only external connections of the HS-SW.

Since ZVS is achieved, a synchronized turn on of the switching cells is not needed,

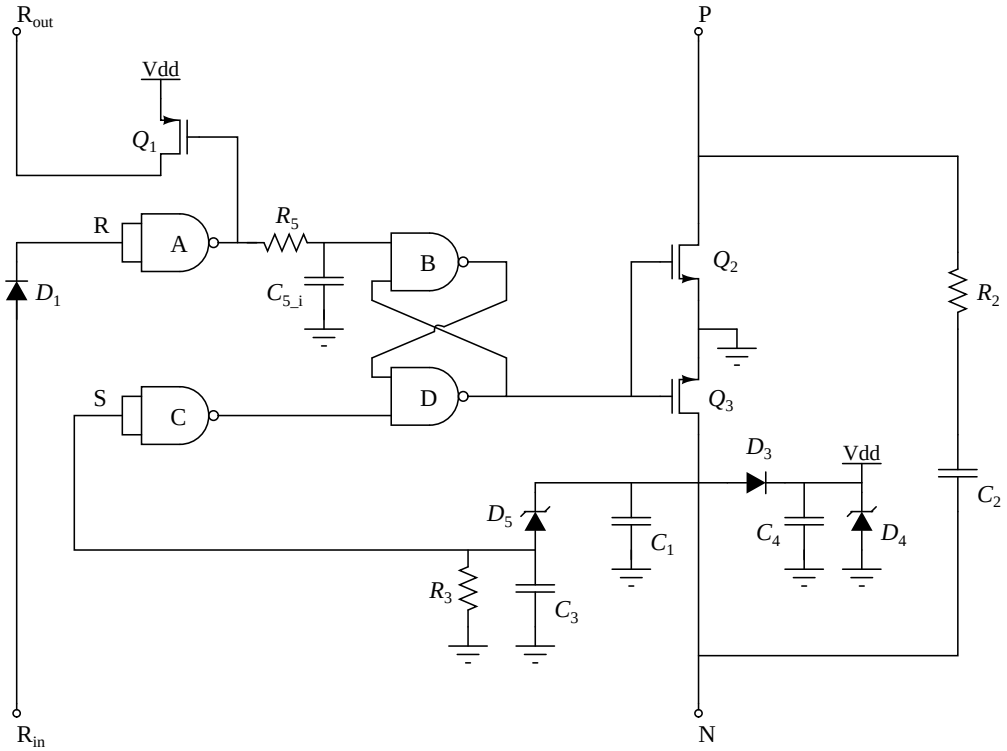

Figure 2.9: Simplified schematic of a switching cell. The ground symbol indicates the local ground of the single cell. Transistor Q_2 consists in a high-voltage super-junction MOSFET.

because the components of the HS-SW are not stressed during the turn on. Differently, the requirements on the HS-SW cells turn-off synchronization are strict, in order to achieve (2.4) and avoid damage of the components. A single cell causes a propagation delay of the turn off signal t_{off}, which is given by the sum of the propagation delay of the diode D_1, the NAND port A and the transistor Q_1. In a generic cell i, where $0 \leq i \leq N_{cell} - 1$, when the NAND port A commutates during the turn off (high-to-low transition), the NAND port B commutates after a time t_{port_B}, which is given by

$$t_{port\_B\_i} = it_{off} - R_5(C_{5\_i} + C_{in\_port})ln\left(\frac{V_{T-}}{V_{DD}}\right) \tag{2.19}$$

where V_{T-} and C_{in_port} are the negative threshold voltage and the input capacitance of the NAND port B respectively.

The low-pass filter (R_5, C_{5_i}) aims to compensate the propagation delay of the turn off signal through the cells, therefore the quantity

$$it_{off} - R_5C_{5\_i}ln\left(\frac{V_{T-}}{V_{DD}}\right) \tag{2.20}$$

must be constant. The capacitance C_{5_i} implements a different value in each cell

$$C_{5\_i} = (N_{cell} - 1 - i)C_5 \tag{2.21}$$

Furthermore, by choosing R_5 and C_5 according to

$$t_{off} = -R_5C_5ln\left(\frac{V_{T-}}{V_{DD}}\right) \tag{2.22}$$

the quantity (2.20) is constant.

This solution suffers for the tolerance of the components, e.g. value of resistance and capacitance, logic threshold of the NAND ports, value of the propagation delay. Therefore, this solution is not completely reliable.
The capacitance C_2 relaxes the requirements on the cells turn-off synchronization. During the turn-off, the slope of the voltage across the switching cell v_{pn} and the capacitance C_2 are inversely proportional

$$\frac{\mathrm{d}v_{pn}}{\mathrm{d}t} \propto \frac{1}{C_2} \tag{2.23}$$

Therefore, with an appropriate value of C_2, a non-synchronized turn-off of the cells has a limited effect.

The operation of the studied TI-buck converter is described in the following.

Off state

The HS-SW is off and the voltage over the switch is blocked by the super-junction MOSFET Q_2.

Reverse bias interval

During the resonance commutation interval of the converter, as soon as the HS-SW is reverse biased, the super-junction MOSFET body diode D_2 turns on, connecting the cell local ground voltage to the positive terminal V_p. As the resonance continues, the negative terminal voltage V_n increases, providing local power supply V_{DD} by charging C_4. The zener diode D_4 clamps the local power supply to the desired value.

On state

For a certain value of V_n the SR-latch is set and the transistors Q_2 and Q_3 are turned on. Q_3 connects the N terminal to the cell local ground and the set signal drops to zero, bringing back the SR-latch to the memory state.

Turn off

At a predetermined current level $i = \frac{I_p}{1+N}$, the current-sense resistor R_{sense} provides the reset signal, which propagates through the cells via R_{in} and R_{out}. The propagation delay is compensated by a low-pass filter (R_5, C_{5_i}) in the SR-latch.

2.4 Control strategy

Given the HS-SW implementation, the converter operation is fixed. The pre-programmed turn-off current of the HS-SW means that each switching cycle delivers nearly constant energy to the output. Therefore, the output voltage can be controlled by varying the switching frequency, i.e. by using a Pulse Frequency Modulation (PFM). Figure 2.10 illustrates the concept of the adopted control method, while Figure 2.11 illustrates the PFM. Since the switching cycle is triggered by turning-on the LS-SW, the PFM can be easily implemented by managing the LS-SW properly.

In the following Section, an average model of the studied converter is developed. By using such average model, a closed-loop output voltage control system, which uses the switching frequency as a control variable, can be designed and implemented.

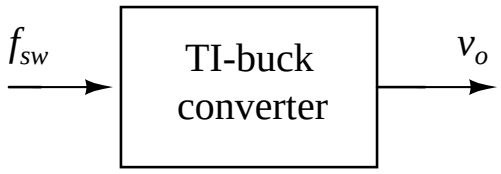

Figure 2.10: Concept of the adopted control method. The output voltage can be controlled by varying the switching frequency.

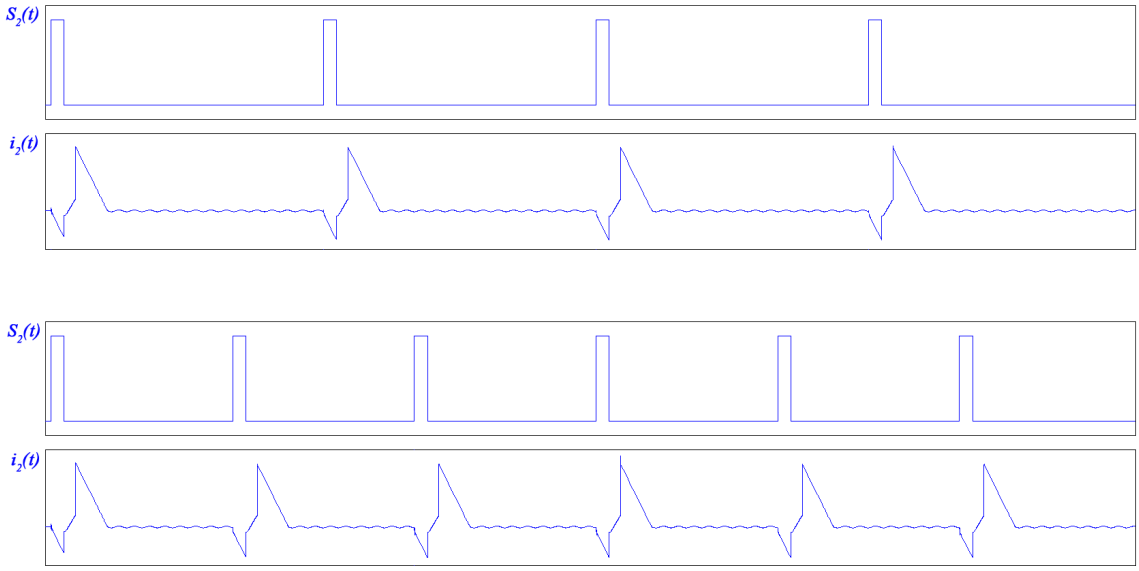

Figure 2.11: Example of Pulse Frequency Modulation (PFM). The LS-SW gate signal, $S_2(t)$, and the output current, $i_2(t)$, are shown at two different switching frequencies.

2.5 Average output current model

This Section describes a model of the converter based on the average output current $\overline{i_2}$, which is given by

$$\overline{i_2} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_2(t)\,\mathrm{d}t \tag{2.24}$$

where T_{sw} is the switching period.

The average output current model is developed for:

- an in depth study of the converter, aimed to obtain the conversion ratio M, defined as:
$$M = \frac{v_o}{v_i} \tag{2.25}$$
- obtaining the small signal model of the converter, essential for the closed-loop control design.

Given the studied TI-buck operation, the exact expression of $\overline{i_2}$ is complicated. Therefore, an approximated expression is used instead. In order to have a good approximation, the following statements must be true:

- the resonance commutation interval must be negligible if compared to the total duration of the converter operation;
- the output voltage static ripple must be negligible, i.e. $v_o(t) \simeq v_o$.

Also the input voltage must be nearly constant during a switching period, which is usually true in the application of interest. The waveform of the approximated output current is shown in Figure 2.12.

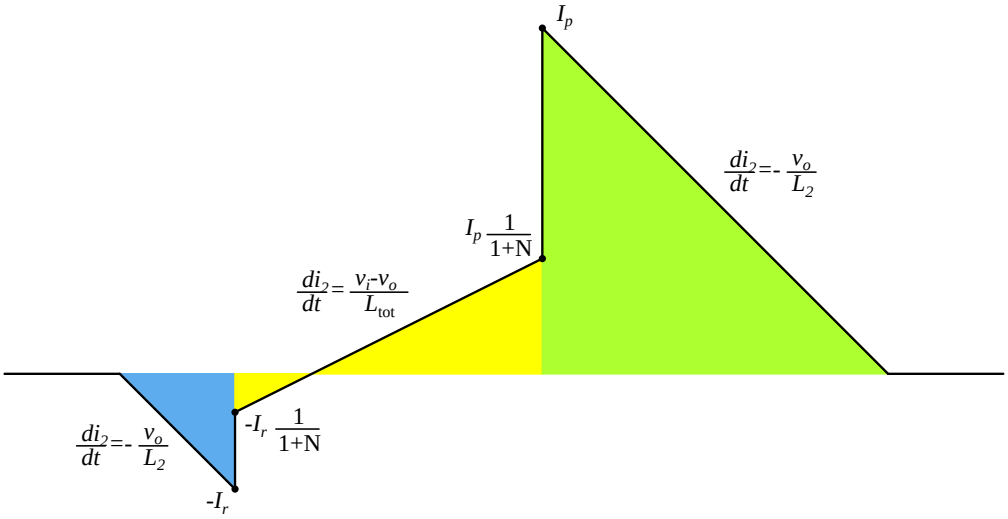

Figure 2.12: Waveform of the approximated output current.

From the approximated expression, the average output current can be expressed as

$$\overline{i_2} = f_{sw} \frac{L_2}{2} (I_p^2 - I_r^2) \left[\frac{1}{v_o} + \frac{1}{v_i - v_o} \right] \tag{2.26}$$

where I_p and I_r are the positive and the negative peak output current respectively. The relation:

$$L_2 = \frac{1}{(1+N)^2} L_{tot} \tag{2.27}$$

has been used in order to obtain (2.26). A description of the tapped-inductor properties is presented in Appendix A.

Figure 2.13 shows the average output current model of the studied converter, which simply consists in the non-linear current source $\overline{i_2}$ connected to the output capacitance C_o and the load R_{LOAD}.

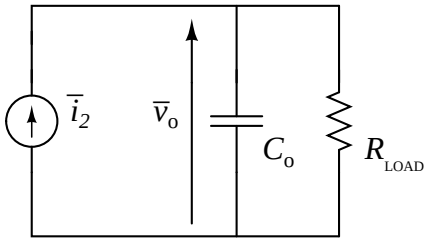

Figure 2.13: TI-buck average output current model.

2.6 Control characteristic

The control characteristic shows the conversion ratio $M = \frac{v_o}{v_i}$ as function of the control variable, i.e. as function of f_{sw} in the studied converter.

The expression (2.26), with the average output current expressed as $\overline{i_2} = \frac{v_o}{R_{\text{LOAD}}}$, leads to the relation

$$M^2(1 - M) = \frac{f_{sw}}{f_{norm}} \tag{2.28}$$

where

$$f_{norm} = \left[\frac{L_2}{2}\frac{R_{\text{LOAD}}}{v_i^2}(I_p^2 - I_r^2)\right]^{-1} \tag{2.29}$$

denotes the normalization frequency. Since this is an large step-down ratio application, where $v_i >> v_o$, the term $(1 - M)$ in the equation (2.28) can be neglected, resulting in a explicit expression of the conversion ratio as a function of the ratio between the switching frequency and the normalization frequency

$$M = \sqrt{\frac{f_{sw}}{f_{norm}}} \tag{2.30}$$

Figure 2.14 shows the control characteristic of the converter, comparing (2.28) with (2.30).

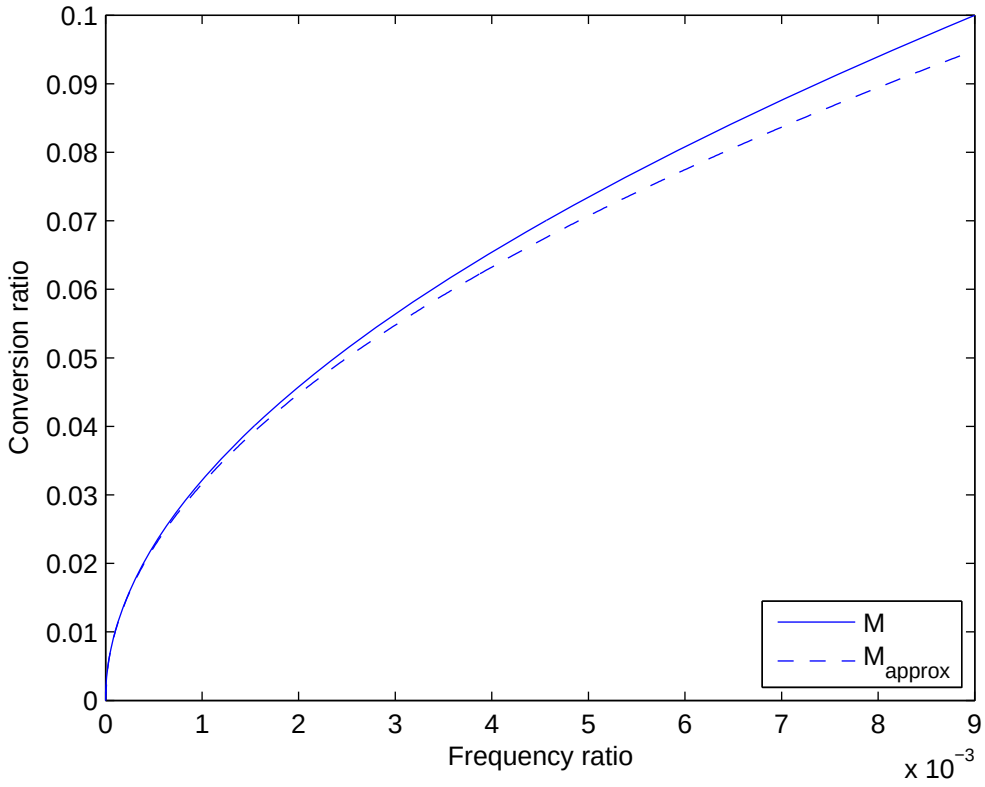

Figure 2.14: Conversion ratio vs frequency ratio, which denotes the ratio between the switching frequency and the normalization frequency. The solid curve shows a numerical evaluation of (2.28), while the dashed curve shows a plot of (2.30).

Another interesting expression to evaluate is the maximum conversion ratio achievable M_{max}. The studied converter operates in DCM, i.e. the output current is null at the beginning of each switching cycle. This condition happens when the switching period T_{sw} is greater than T_{busy}, which denotes the sum of the intervals where the converter operates ($t_0 - t_5$ in Figure 2.6). From Figure 2.12, T_{busy} can be expressed as

$$T_{busy} = \frac{L_2(I_p + I_r)(1 + NM)}{v_i M(1 - M)} \tag{2.31}$$

The maximum conversion ratio achievable M_{max} occurs when the converter operates in critical conduction mode, which is the boundary condition between continuous conduction mode and discontinuous conduction mode. This condition happens when the switching period T_{sw} is equal to T_{busy}. Therefore, from (2.28) and (2.31)

$$\begin{aligned} f_{sw} = \frac{1}{T_{busy}} &\implies \frac{2v_i^2 M_{max}^2(1 - M_{max})}{L_2 R_{\text{LOAD}}(I_p^2 - I_r^2)} = \frac{v_i M_{max}(1 - M_{max})}{L_2(I_p + I_r)(1 + NM_{max})} \\ &\implies M_{max}(1 + NM_{max}) = \frac{R_{\text{LOAD}}(I_p^2 - I_r^2)}{2v_i(I_p + I_r)} \\ &\implies M_{max} = -\frac{1}{2N} + \sqrt{\frac{1}{4N^2} + \frac{R_{\text{LOAD}}(I_p^2 - I_r^2)}{2Nv_i(I_p + I_r)}} \end{aligned} \tag{2.32}$$

2.7 Converter design

In this Section a basic design of the studied converter is shown. From the main specification, i.e. input voltage, output voltage and output power, the converter is designed. The components chosen in the following refers to the large step-down ratio TI-buck converter analyzed in [13], which has the following specifications:

- input voltage v_i: 3kV
- output voltage v_o: 100V
- output power p_o: 70W

As described in Section 1.1, the converter must be able to operate at low input voltage, in order to allow the investigation of fault conditions and erroneous behavior in the submodule at non-dangerous conditions. Therefore, another specification must be included:

- minimum input voltage v_i: 250V

Switching devices

Firstly, the switching devices are chosen. A high blocking voltage capability is needed. The super-junction MOSFET *Infineon Cool MOS Power Transistor 17N80C3* is a good compromise between features and cost. Furthermore, this is a surface-mount device, which helps the design of the printed circuit board of the converter. The main features of this device is:

- drain-source breakdown voltage: 800V
- drain-source on resistance: 0.29Ω

This device is used both in the HS-SW switching cells and also as LS-SW.

Tapped-inductor turns ratio

The tapped-inductor turns ratio is chosen so that the power MOS drain-source breakdown voltage matches the LS-SW voltage stress (2.3b). The chosen value is

$$N = 4.6 \tag{2.33}$$

which imply a LS-SW voltage stress $\hat{v}_{S2} = 618\text{V}$.

HS-SW switching cells

Once the tapped-inductor turns ratio is set, the number of switching cells in the HS-SW is set according to the HS-SW voltage stress (2.3a). This voltage stress, divided by the number of cells, must match the power MOS drain-source breakdown voltage. A number of cells

$$N_{cell} = 6 \tag{2.34}$$

is chosen, which imply a cell voltage stress $\hat{v}_{cell} = 577\text{V}$.

Positive and negative peak output current

Starting from this point, the design procedure is explained as linearly as possible, even though in reality some iterations could be needed. This is because 5 parameters need to be set (I_p, I_r, C_{S1}, L_{tot} and f_{sw}) according to 5 constraints, which makes the design procedure hard to be done linearly.

The analyzed converter must operate in discontinuous conduction mode. This condition can be expressed as

$$\frac{T_{busy}}{T_{sw}} < 1 \tag{2.35}$$

by substituting (2.26) for T_{sw} and (2.31) for T_{busy} the DCM condition becomes

$$\frac{T_{busy}}{T_{sw}} = \frac{2p_o(v_i + Nv_o)(k_{pr}+1)}{v_i v_o I_r (k_{pr}^2 - 1)} < 1 \tag{2.36}$$

where k_{pr} denotes the ratio between I_p and I_r. By choosing the pair of values

$$I_r = 8\text{A} \tag{2.37a}$$
$$k_{pr} = 2 \implies I_p = 16\text{A} \tag{2.37b}$$

the DCM condition is always guaranteed, especially in the worst case, when the input voltage is minimum and the converter operates at full output power

$$\frac{T_{busy}}{T_{sw}} \leq 0.5 \tag{2.38}$$

The above-mentioned choice of I_p and I_r is the result of an iterative design procedure, which satisfies more constraints, described in the following.

HS-SW snubber capacitance

During the HS-SW turn-off, the snubber capacitance of a single cell C_{S_cell} is charged with constant current $\frac{I_p}{1+N}$. Therefore, the voltage across each cell v_{pn} increases with constant slope

$$\frac{\mathrm{d}v_{pn}}{\mathrm{d}t} = \frac{I_p}{C_{S\_cell}(1+N)} \tag{2.39}$$

An error in the turn-off synchronization of the HS-SW cells $t_{mismatch}$ results in a difference between the voltage across the cell at the end of the HS-SW turn-off phase $v_{mismatch}$

$$v_{mismatch} = t_{mismatch}\frac{I_p}{C_{S\_cell}(1+N)} \tag{2.40}$$

The snubber capacitance of a single cell C_{S_cell} is set according to the last equation, by setting $t_{mismatch} = 50\text{ns}$, according to the variability of the propagation delay of the turn off signal, and $v_{mismatch} < 50\text{V}$

$$C_{S\_cell} = 3.3\text{nF} \implies C_{S1} = \frac{C_{S\_cell}}{N_{cell}} = 550\text{pF} \tag{2.41}$$

Tapped-inductor inductance

The tapped-inductor inductance must provide sufficient energy storage in order to achieve the ZVS, according to (2.11). The chosen value is

$$L_{tot} = 13.4\text{mH} \tag{2.42}$$

Furthermore, the tapped-inductor must feature a core saturation current greater than I_p. A detailed description of the tapped-inductor design is given in [14].

Switching frequency

The value of the switching frequency can be obtained with sufficient accuracy from equation (2.26)

$$f_{sw} = 1.65\text{kHz} \tag{2.43}$$

The exact value of the switching frequency is automatically set by the microcontroller when the converter runs in closed-loop mode.

The resulting switching frequency also satisfies another constraint, which states that f_{sw} must be much less than the resonance frequency of L_{tot} and C_{S1}, in order to limit the duration of the resonance intervals compared to the switching period

$$f_{sw} \ll \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L_{tot}C_{S1}}} \tag{2.44}$$

Thus, the converter design meets all the requirements.

Output capacitance

The output capacitance C_o affects:

- the output voltage static ripple;
- the dynamic response of the converter, e.g. the evolution of the output voltage after a step response of the load;
- the duration of the start-up procedure of the converter, discussed in Section 4.4.

A bigger output capacitance reduces the static ripple, but it also slows the dynamic response and the start-up procedure of the converter. Therefore, a compromise between these features is needed. As discussed in Section 1.1, the analyzed converter should start-up as quickly as possible, while a high variability of the output voltage is tolerated.

An approximated expression of the peak-to-peak static ripple, which neglect the change of the output voltage during the pre-charge phase, can be evaluated during the idling phase, when the output voltage evolves as a basic RC circuit

$$v_o(t) = (v_o + \frac{v_{ripple}}{2})\mathrm{e}^{-\frac{t}{R_{load}C_o}} \tag{2.45}$$

where v_{ripple} denotes the static ripple of the output voltage. Since the idling phase lasts for $T_{idling} = T_{sw} - T_{busy}$, v_{ripple} can be expressed as

$$v_{ripple} = \frac{2v_o(1 - \mathrm{e}^{-\beta})}{(1 + \mathrm{e}^{-\beta})} \tag{2.46}$$

where

$$\beta = \frac{T_{sw} - T_{busy}}{R_{load} C_o} \tag{2.47}$$

A static ripple $v_{ripple} < 50\text{V}$ is required for this application. The chosen output capacitance is

$$C_o = 10\mu\text{F} \tag{2.48}$$

which implies a static ripple $v_{ripple} = 33.6\text{V}$.

Conversion ratio vs switching frequency

Once the converter is designed, the conversion ratio can be evaluated according to (2.28) or (2.30). Figure 2.15 shows the conversion ratio of the converter at 3 different load conditions and the boundary between CCM and DCM. The x-axis shows f_{sw} instead of the ratio $\frac{f_{sw}}{f_{norm}}$ so that the differences between different load conditions become visible.

A zoom of the figure, which focus on the conversion ratio of interest $M = 0.33$ is shown in Figure 2.16. The switching frequency results:

- $f_{sw} = 1.65\text{kHz}$ at full output power;
- $f_{sw} = 825\text{Hz}$ at half output power;
- $f_{sw} = 413\text{Hz}$ at a quarter output power.

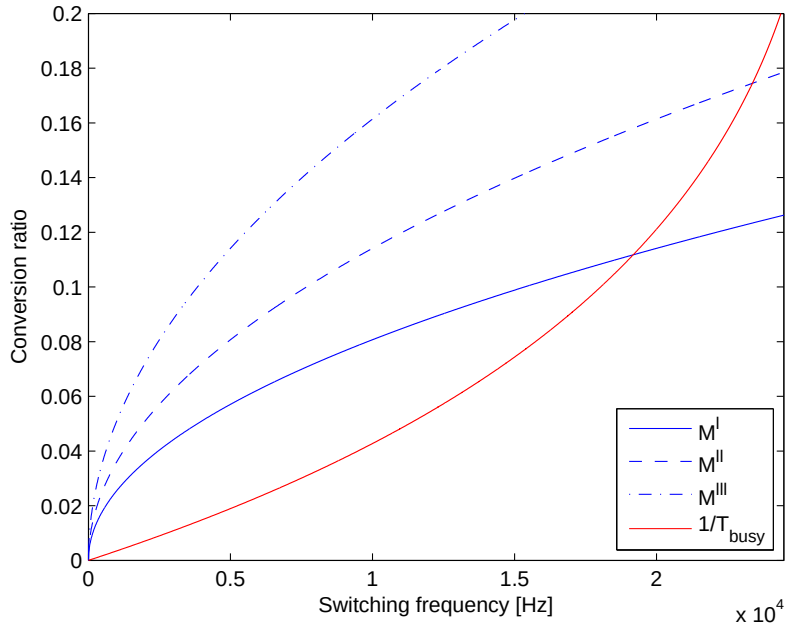

Figure 2.15: Conversion ratio of the converter vs switching frequency. M is evaluated at full output power (solid blue curve), at half output power (dashed blue curve) and at a quarter output power (dashed-dotted blue curve). The red curve, $\frac{1}{T_{busy}}$, shows the boundary between CCM and DCM. The converter operates in DCM condition above the red curve, while it can not operate below the red curve. The maximum conversion ratio M_{max} at full output power occurs when the blue solid curve crosses the red curve.

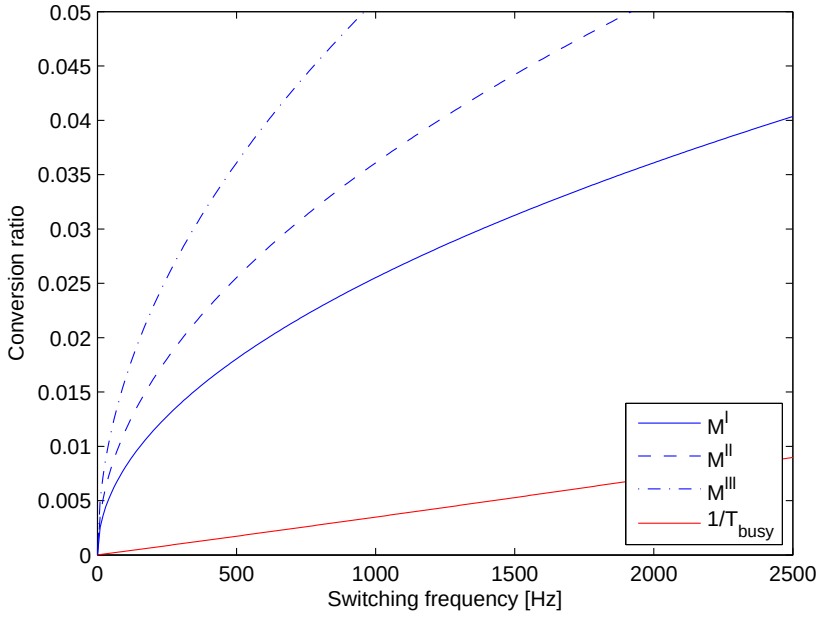

Figure 2.16: Conversion ratio of the converter vs switching frequency, zoom on the values of interest. M is evaluated at full output power (solid blue curve), at half output power (dashed blue curve) and at a quarter output power (dashed-dotted blue curve). The red curve, $\frac{1}{T_{busy}}$, shows the boundary between CCM and DCM.

2.8 Simulations

Once the converter is designed, the software *PLECS* is used for simulating the TI-buck behaviour. The model used for the simulations is shown in Appendix B. Static waveforms are shown in Figure 2.17 and Figure 2.18. A coupling factor $k_{ind} = 0.995$ has been used during the simulation, which causes some ringing after the LS-SW turn-on and after the HS-SW turn-off. The model does not implement the saturation of the tapped-inductor magnetic core, therefore the ringing phenomena could be inaccurate.

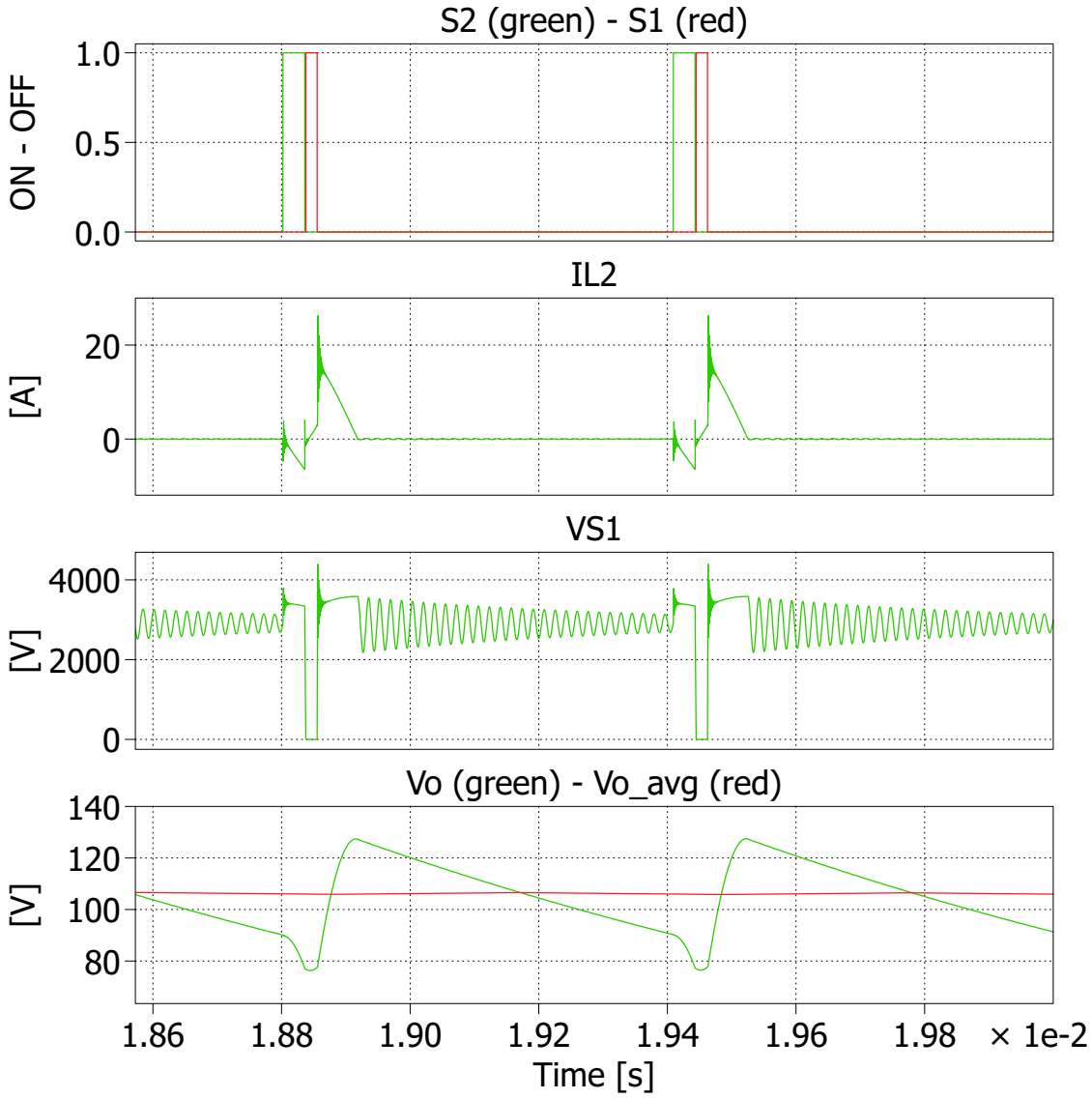

Figure 2.17: Simulation of the static behaviour of the converter, showing a complete switching cycle.

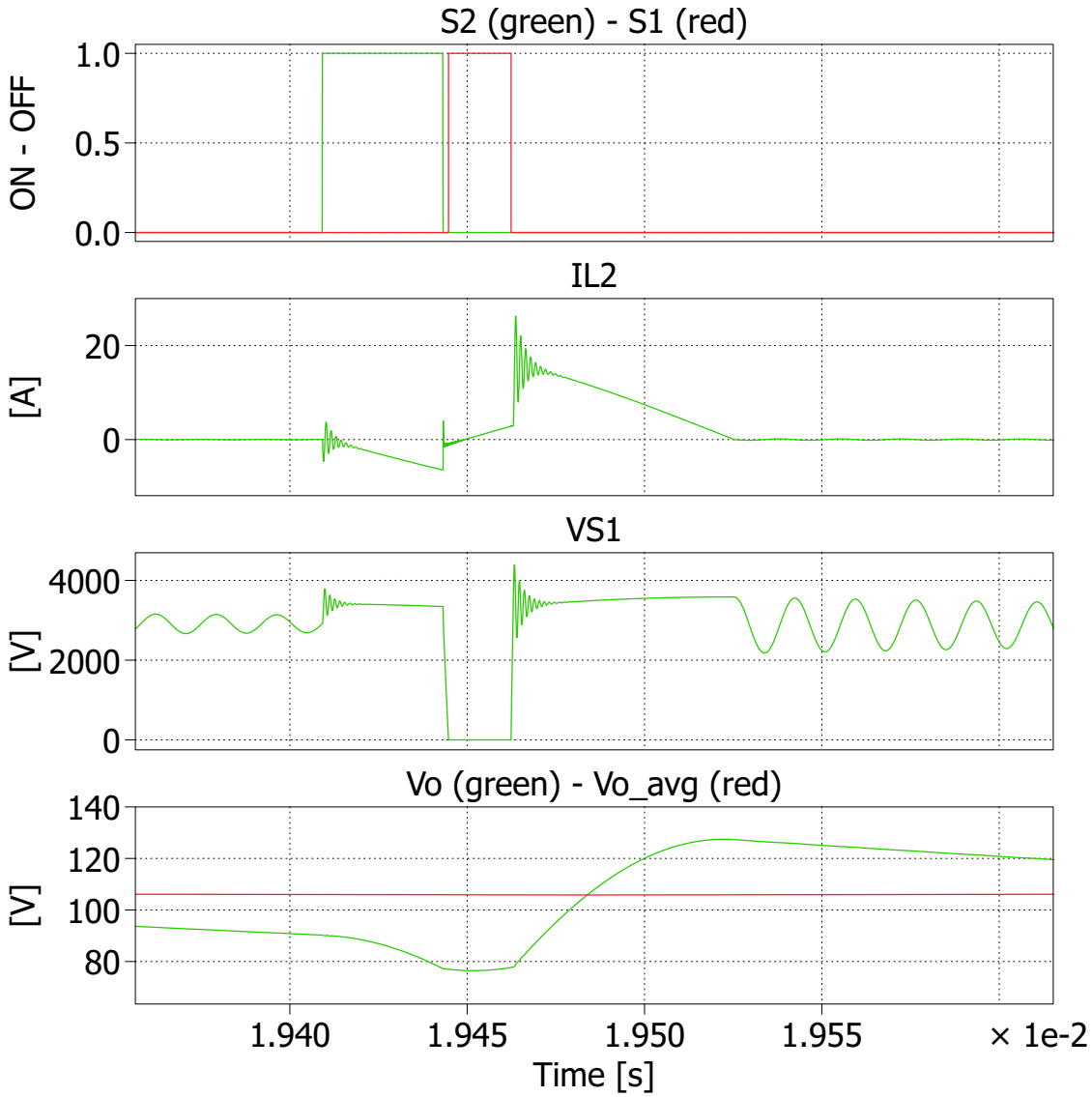

Figure 2.18: Simulation of the static behaviour of the converter, showing the time interval where the converter operates ($t_0 - t_5$ in Figure 2.6).

A measurement of the conversion ratio as a function of the switching frequency is made. Figure 2.19 shows a comparison between the conversion ratio given by (2.28) and the conversion ratio measured on the simulation model. The comparison shows how the model tends to over-estimate the switching frequency, reason why the average output voltage in Figure 2.17 and Figure 2.18 is greater than 100V.

The mismatch between the conversion ratio given by (2.28) and the conversion ratio measured on the simulation model is mainly due to the approximation adopted in Section 2.5, especially the neglect of the the output voltage static ripple. Simulations with a reduced static ripple, achieved with an enhanced output capacitance (Figure 2.20) shows a better match with the analytical expression (2.28).

Another cause of the above-mentioned mismatch is the error in the negative peak output current I_r. At the end of the idling phase, the residual resonance between L_{tot} and C_{S1} causes the output current to be different from zero. Since the duration of the pre-charge phase is calculated on the output voltage, $i_2(t_0) \neq 0$ implies $i_2(t_1) \neq -I_r$ and consequently an error in the conversion ratio.

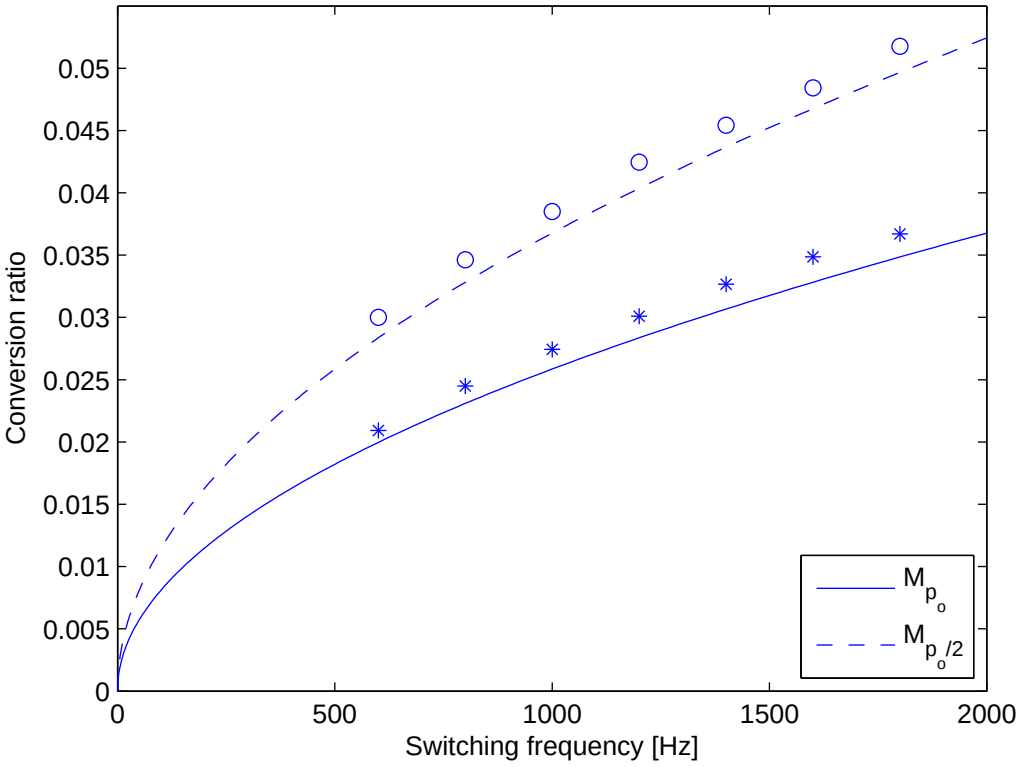

Figure 2.19: Comparison between the conversion ratio given by (2.28) (solid blue curve) and measured on the simulation model (blue stars). Another comparison is made at half output power, by evaluating (2.28) (dashed blue curve) and from measurement on the model (blue circles).

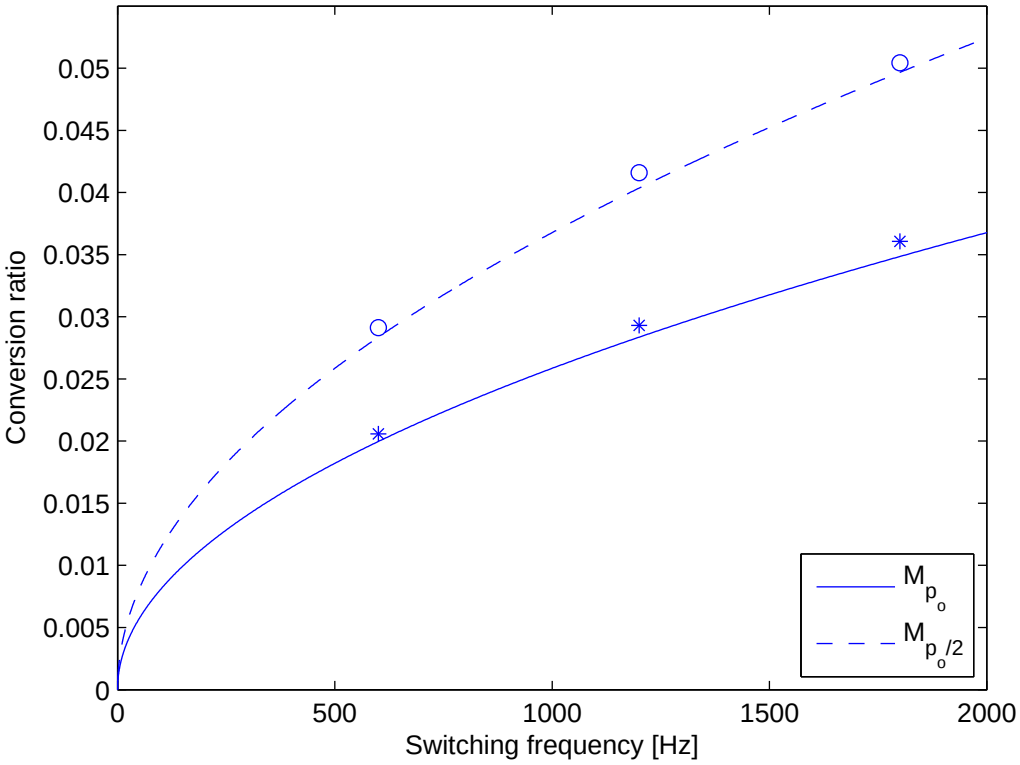

Figure 2.20: Comparison between the conversion ratio given by (2.28) (solid blue curve) and measured on the simulation model (blue stars) with an enhanced output capacitance. Another comparison is made at half output power, by evaluating (2.28) (dashed blue curve) and from measurement on the model (blue circles).

Chapter 3

Closed-loop control design

3.1 Small-signal model

An average model, which describes only the low-frequency converter dynamics, is developed for the control synthesis. The studied converter operates in DCM, i.e. the output current is null at the beginning of each switching cycle, even during transient states. Therefore, as described in [17, 18, 19], the output current dynamics can be neglected, since it is a variable with no "memory". This approach leads to a first order model, which can be obtained by linearizing the average output current equation (2.26). The small signal model of the studied TI-buck converter is obtained by using the first order Taylor series on the average output current equation

$$\hat{i}_2 = \frac{\partial \overline{i_2}}{\partial f_{sw}}\hat{f}_{sw} + \frac{\partial \overline{i_2}}{\partial v_o}\hat{v}_o + \frac{\partial \overline{i_2}}{\partial v_i}\hat{v}_i = k_f \hat{f}_{sw} - r_o^{-1}\hat{v}_o + k_i \hat{v}_i \tag{3.1}$$

where

$$k_f = \frac{L_2}{2}(I_p^2 - I_r^2)\left[\frac{1}{v_o} + \frac{1}{v_i - v_o}\right] \tag{3.2a}$$

$$r_o = \left\{ f_{sw}\frac{L_2}{2}(I_p^2 - I_r^2)\left[\frac{1}{v_o^2} - \frac{1}{(v_i - v_o)^2}\right]\right\}^{-1} \tag{3.2b}$$

$$k_i = -\left[f_{sw}\frac{L_2}{2}(I_p^2 - I_r^2)\frac{1}{(v_i - v_o)^2}\right] \ . \tag{3.2c}$$

The TI-buck small signal model is shown in Figure 3.1. The current generator $\hat{i_o}$ is added in order to study the effect of load variations.

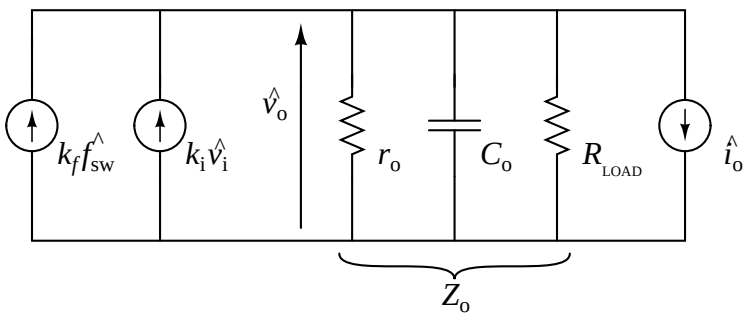

Figure 3.1: TI-buck small-signal model.

The output voltage s-domain expression is obtained by using the superposition principle

$$\hat{V}_o(s) = Z_o(s)[k_f \hat{F}_{sw}(s) + k_i \hat{V}_i(s) - \hat{I}_o(s)] \tag{3.3}$$

where

$$Z_o(s) = \frac{r_o // R_{\text{LOAD}}}{1 + sC_o(r_o // R_{\text{LOAD}})} = \frac{k_o}{1 + s\tau_o} \tag{3.4}$$

denotes the total output impedance. The open-loop block diagram of the analyzed TI-buck converter is shown in Figure 3.2.

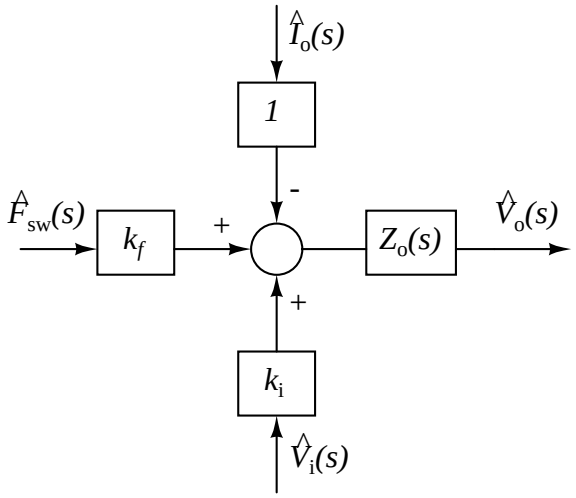

Figure 3.2: TI-buck open-loop block diagram.

The transfer function $V_o(s)/F_{sw}(s)$ of the small-signal model obtained in this Section can be compared with measurements made on the *PLECS* simulation model. Figure 3.3 shows that the small-signal model matches the measurements with sufficient accuracy.

The dependency of the model parameters from f_{sw} could be a non-negligible drawback of this model. During the control operation, significant variation of f_{sw} might be needed. Therefore, a parameters drift occurs and the control system must be robust in this eventuality.

In the following chapter a description of the closed-loop control design is given.

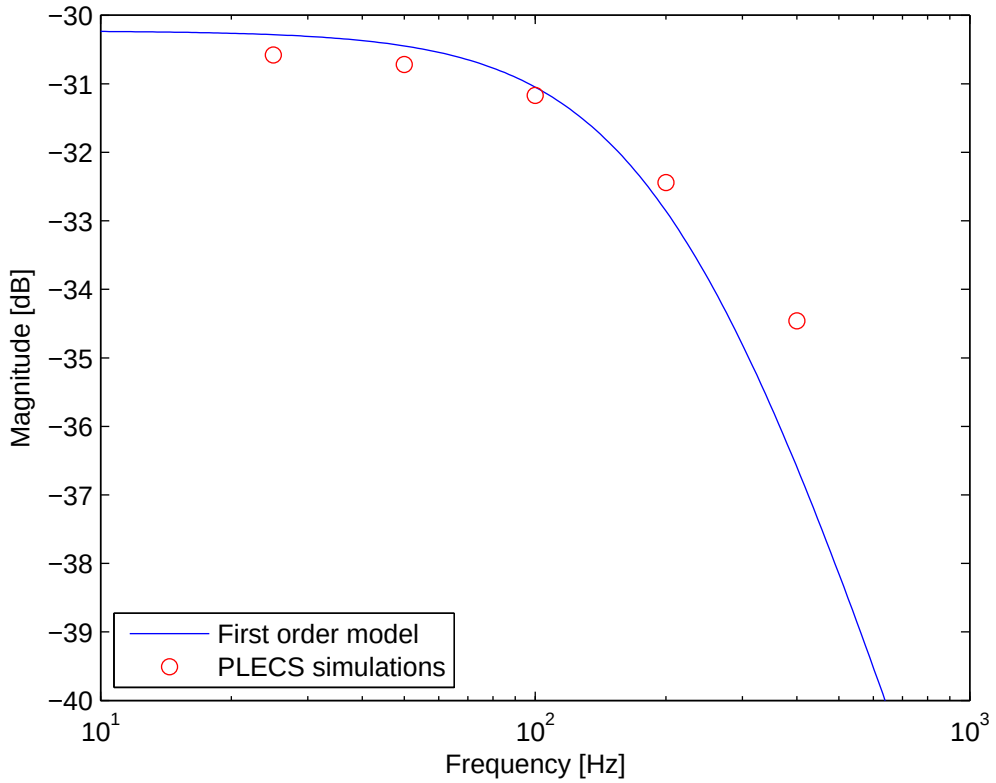

Figure 3.3: Transfer function $V_o(s)/F_{sw}(s)$ of the studied converter. The blue curve shows the prediction of the first order model, while the red dots are measured from PLECS simulations. The prototype data presented in Section 2.7 is used both for the model prediction and the simulations.

3.2 Closed-loop model

As described in Section 2.4, the output voltage can be controlled by using a PFM. Therefore, the LS-SW gate signal must be handled properly. In the studied converter, a micro-controller (μC) is used for the whole control operation. The μC implements:

- an ADC converter, which measures the output voltage;
- a digital low-pass filter, in order to reduce the static ripple and the high-frequency noise from the output voltage samples;
- a discrete-time controller;
- a pulse generator, which provides the LS-SW with a proper gate signal.

Since the ADC sampling frequency is much greater than the converter low-frequency dynamics, e.g. one order of magnitudes, the closed-loop converter can be studied as a continuous-time device. The digital low-pass filter and the discrete-time controller are first designed in the s-domain, then a conversion to the z-domain is made in order to obtain the discrete-time equations, which are implemented by the μC.

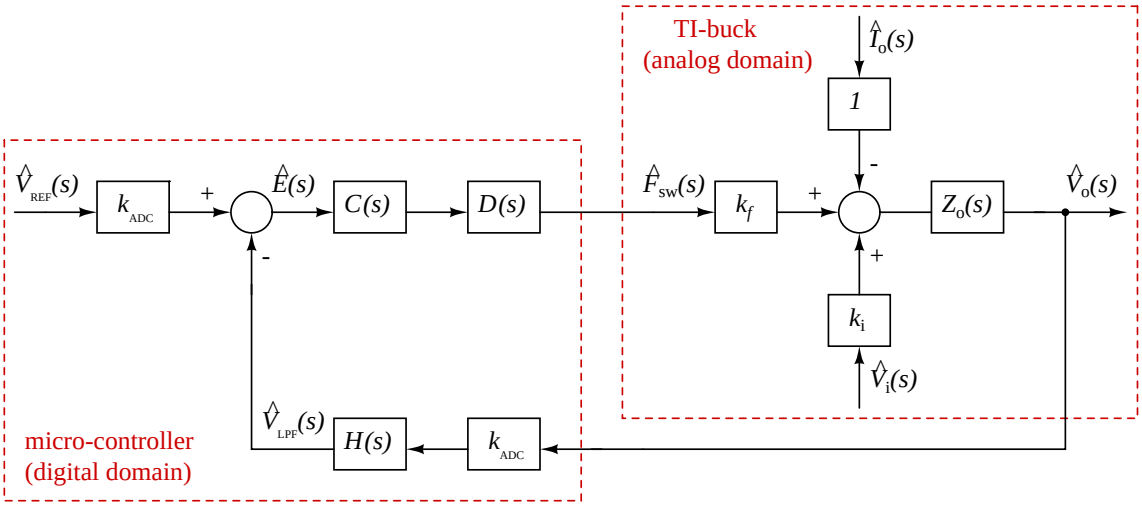

Figure 3.4: Block diagram of the closed-loop output voltage control.

The closed-loop block diagram is shown in Figure 3.4. The model includes:

- the ADC conversion factor k_{ADC};
- the digital low-pass filter $H(s)$;
- the discrete-time controller $C(s)$;
- the μC delay $D(s)$. In the worst case, the μC delay consists of the sum of the ADC sampling period t_s and the switching period T_{sw}, because the switching frequency is updated at the end of every switching period. Therefore

$$D(s) = \mathrm{e}^{-st_{\mu C}} \tag{3.5}$$

where $t_{\mu C} = t_s + T_{sw}$.

The closed-loop output voltage s-domain expression is given by

$$\hat{V}_o(s) = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \hat{V}_{ref}(s) + \frac{k_i Z_o(s)}{1+T(s)} \hat{V}_i(s) - \frac{Z_o(s)}{1+T(s)} \hat{I}_o(s) \tag{3.6}$$

where

$$T(s) = k_f k_{ADC} D(s) Z_o(s) H(s) C(s) \tag{3.7}$$

denotes the loop gain.

3.3 Filter design

The digital low-pass filter reduces the the static ripple and the high-frequency noise from the output voltage samples. There are no particular constraint in the filter design. A second order Butterworth low-pass filter is used

$$H(s) = \frac{1}{1 + \frac{2\xi}{\omega_{lpf}} s + \frac{s^2}{\omega_{lpf}^2}} \tag{3.8}$$

The Butterworth filter, which is also referred to as a maximally flat magnitude filter, ensures a flat response for frequencies $f < f_{lpf}$, and a $-20{\cdot}N$ dB/dec attenuation for frequencies $f > f_{lpf}$, where N is the order of the filter. Figure 3.5 shows the Bode plot of a second order Butterworth low-pass filter.

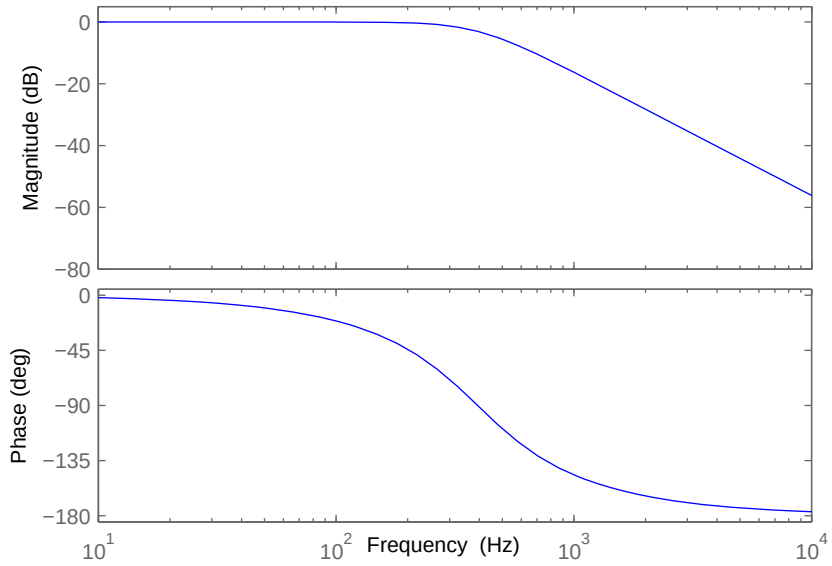

Figure 3.5: Bode plot of a second order Butterworth low-pass filter.

In the complex plane, according to the Butterworth condition, the poles of the filter and their reflections on the imaginary axis must be placed on a circumference with radius ω_{lpf}, equally distant from each other. Therefore

$$\xi = \cos(\varphi) = \frac{\sqrt{2}}{2} \tag{3.9}$$

Figure 3.6 shows the Butterworth condition for a second order filter.

The crossing frequency of the filter, f_{lpf}, is set according to the desired attenuation at the switching frequency, f_{sw}, given by

$$\alpha_{\text{dB}} = 20 \log(|H(j\omega_{sw})|) \tag{3.10}$$

In the frequency range $f > f_{lpf}$, the filter produces a -40dB/dec attenuation. Therefore

$$\alpha_{\text{dB}} = -40\,[\log(f_{sw}) - \log(f_{lpf})] \implies f_{lpf} = \frac{f_{sw}}{10^{-\frac{\alpha_{\text{dB}}}{40}}} \tag{3.11}$$

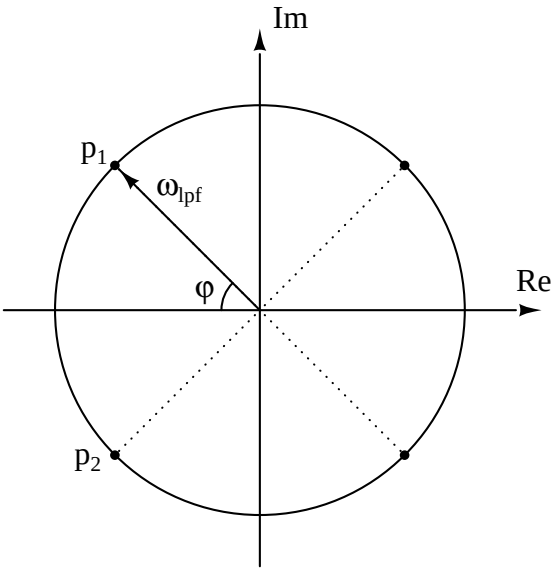

Figure 3.6: Poles of a second order Butterworth filter and their reflections on the imaginary axis.

3.4 Controller design

The controller must ensures both stability and null static error. Also, the controller is designed in order to maximize the loop gain magnitude in the greatest frequency range, i.e. the system bandwidth, by ensuring a phase margin greater than 60°.

The proportional-integral (PI) controller

$$C(s) = k_p + \frac{k_i}{s} \tag{3.12}$$

satisfies all the requirements. Furthermore, due to its simplicity, it can be easily implemented by a low-power μC, which usually has limited computing capacity.

With the PI controller, the loop gain can be expressed as:

$$\begin{aligned} T(s) &= k_f k_{ADC} D(s) Z_o(s) H(s) C(s) \\ &= k_f k_{ADC}\, \mathrm{e}^{-s t_{\mu C}} \frac{k_o}{1+s\tau_o} \frac{1}{1+\frac{2\xi}{\omega_{lpf}}s+\frac{s^2}{\omega_{lpf}^2}} \frac{k_i}{s}\left(1+\frac{k_p}{k_i}s\right) \end{aligned} \tag{3.13}$$

A simple and effective PI controller design, i.e. the tuning of k_p and k_i, can be made by using an iterative procedure, shown in Figure 3.7. The PI controller is designed in order to achieve specific crossing frequency, ω_c, and phase margin, PM, which are respectively defined as

$$\omega_c \quad \Big| \quad |T(j\omega_c)| = 1 \tag{3.14a}$$

$$PM = 180^\circ - \angle T(j\omega_c) \tag{3.14b}$$

The PI controller parameters k_p and k_i are calculated as follow

$$\frac{k_p}{k_i} = \frac{1}{\omega_c} \tan\left\{ PM\frac{\pi}{180} - \frac{\pi}{2} + \arctan\left[\frac{\frac{2\xi}{\omega_{lpf}}\omega_c}{1-\frac{\omega_c^2}{\omega_{lpf}^2}}\right] + \omega_c t_{\mu C} + \arctan(\omega_c\tau_o)\right\} \tag{3.15a}$$

$$k_i = \frac{\omega_c\sqrt{1+(\omega_c\tau_o)^2}\sqrt{\left(1-\frac{\omega_c^2}{\omega_{lpf}^2}\right)^2+\left(\frac{2\xi}{\omega_{lpf}}\omega_c\right)^2}}{k_f k_{ADC} k_o \sqrt{1+\left(\frac{k_p}{k_i}\omega_c\right)^2}} \tag{3.15b}$$

$$k_p = \frac{k_p}{k_i} k_i \tag{3.15c}$$

Then, an evaluation of the resulting loop gain is made. If the new loop gain has higher performance, i.e. higher magnitude in the frequency range of interest $f < f_c$, than the loop gain from the previous iteration, then the PI controller parameters are updated and a new iteration, with a higher crossing frequency, is performed. Otherwise the loop gain resulting form the last iteration has the best performance and the design procedure ends. Figure 3.8 shows the loop gain resulting from three different iterations of the design procedure.

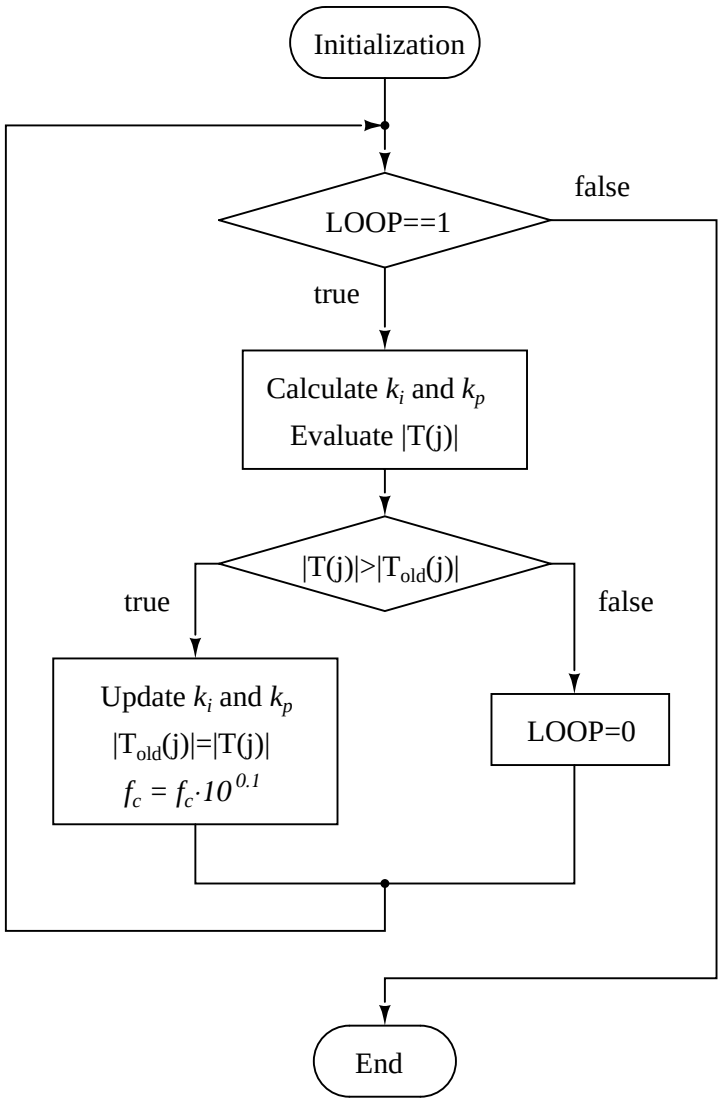

Figure 3.7: Flow chart of the design procedure. The loop gain is evaluated at $\omega =$ 1rad/s. The update of the crossing frequency $f_c = f_c \cdot 10^{0.1}$ is due to increment f_c of $1/10$ of decade.

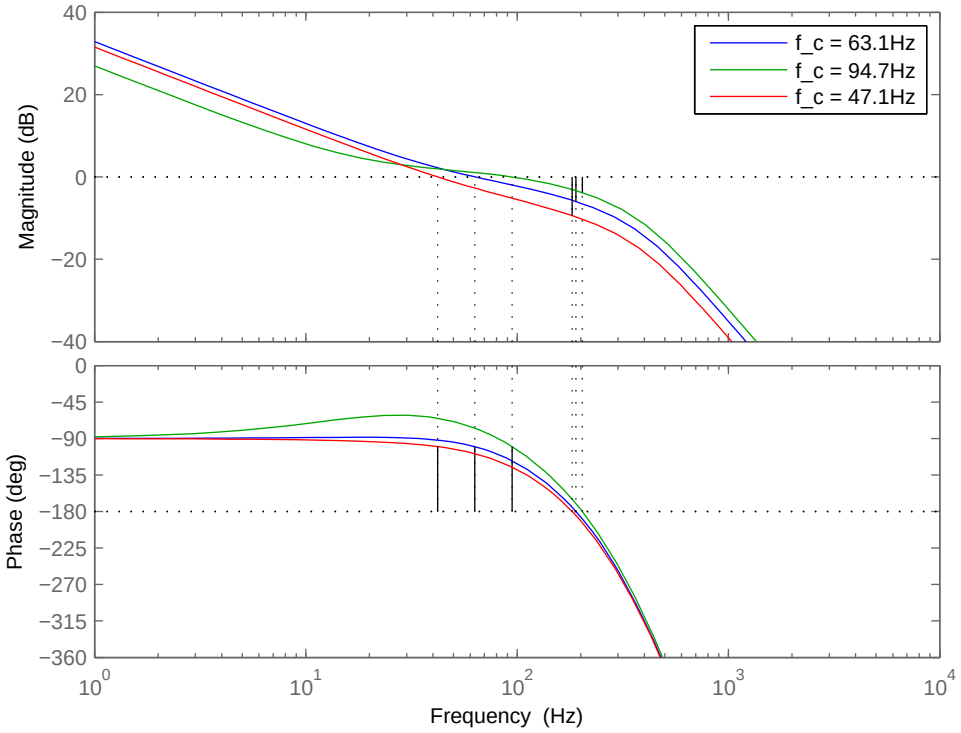

Figure 3.8: Bode plot of the loop gain resulting from three different iterations of the design procedure. The phase margin is set to 80^o, while the crossing frequency increases at each iteration. The blue curve has the best performance, i.e. the highest loop gain magnitude at $f < f_c$.

3.5 Conversion to discrete-time domain

Once the digital low-pass filter and the discrete-time controller are designed in the s-domain, then a conversion to the z-domain is made in order to obtain the discrete-time equations, which are implemented by the μC. The backward Euler method, or implicit Euler method, is used for the conversion. According to this method, a z-domain expression of a general function can be obtained from the s-domain expression by substituting:

$$s = \frac{1 - z^{-1}}{t_s} \tag{3.16}$$

where t_s denotes the ADC sampling period.

PI controller

The z-domain expression of the PI controller is given by

$$\begin{aligned} C(z) &= C(s)\Big|_{s=\frac{1-z^{-1}}{t_s}} \\ &= k_p + \frac{k_i}{s}\Big|_{s=\frac{1-z^{-1}}{t_s}} = k_p + k_i \frac{t_s}{1 - z^{-1}} \end{aligned} \tag{3.17}$$

The output of the PI controller, F_{sw}, is given by the sum of the proportional action, $P(z)$, and the integral action, $I(z)$

$$F_{sw}(z) = P(z) + I(z) \tag{3.18}$$

Therefore, the discrete time expression of the switching frequency, $f_{sw}(n)$, is obtained from the sum of the inverse z-transform of the two actions

$$f_{sw}(n) = p(n) + i(n) \tag{3.19}$$

where

$$p(n) = \mathcal{Z}^{-1}\{P(z)\} = \mathcal{Z}^{-1}\{k_p E(z)\} = k_p e(n) \tag{3.20a}$$

$$i(n) = \mathcal{Z}^{-1}\{I(z)\} = \mathcal{Z}^{-1}\left\{k_i \frac{t_s}{1 - z^{-1}} E(z)\right\} = i(n-1) + k_i t_s e(n) \tag{3.20b}$$

where n denotes the time variable in the discrete-time domain, while $e(n)$ denotes the error signal, i.e. the input signal of the PI controller

$$e(n) = v_{_{REF}} - v_{lpf}(n) \tag{3.21}$$

Low-pass filter

The digital low-pass filter discrete-time equations are obtained similarly

$$v_{lpf}(n) = k_1 v_o(n) + k_2 v_{lpf}(n-1) - k_3 v_{lpf}(n-2) \tag{3.22}$$

where

$$k_1 = \frac{t_s^2}{t_s^2 + \frac{2\xi t_s}{\omega_{lpf}} + \frac{1}{\omega_{lpf}^2}} \qquad k_2 = \frac{\frac{2\xi t_s}{\omega_{lpf}} + \frac{2}{\omega_{lpf}^2}}{t_s^2 + \frac{2\xi t_s}{\omega_{lpf}} + \frac{1}{\omega_{lpf}^2}} \qquad k_3 = \frac{\frac{1}{\omega_{lpf}^2}}{t_s^2 + \frac{2\xi t_s}{\omega_{lpf}} + \frac{1}{\omega_{lpf}^2}} \tag{3.23}$$

3.6 Micro-controller operation

As described in Section 3.2, the μC implements an ADC converter, a digital low-pass filter, a discrete-time controller and a pulse generator, which provides the LS-SW with a proper gate signal. The μC program consists of two main parts:

- Main loop. The output voltage is read from the ADC register and the pulse generator parameters (T_{on} and T_{sw}) are calculated.
- Interrupt routine. Based on an internal timer, the interrupt routine implements the LS-SW pulse generator.

The μC continuously runs the main loop, where all the calculations are made. Whenever the internal timer throws an interrupt, the program jumps to the interrupt routine, where the LS-SW gate signal is generated.

With reference to Figure 3.9, the operation of the μC is described as follows:

1. During the initialization the μC registers are set, the constants are declared and the variables are initialized.
2. The output voltage is read form the ADC register.
3. The digital low-pass filter is implemented by using (3.22)
4. The LS-SW on interval, T_{on}, is set in order to obtain the desired value of i_{r}, according to (2.6)
$$T_{on} = \frac{L_2 i_{\mathrm{r}}}{v_{lpf}} \tag{3.24}$$
5. The PI controller parameters are updated according to (3.21), (3.20a), (3.20b) and (3.19). Then the switching period is obtained from the inverse of the switching frequency.
6. The interrupt service routine switches the LS-SW and loads in the timer T_{on} and $(T_{sw} - T_{on})$ alternately. Then the program returns to the main loop, where it was interrupted.

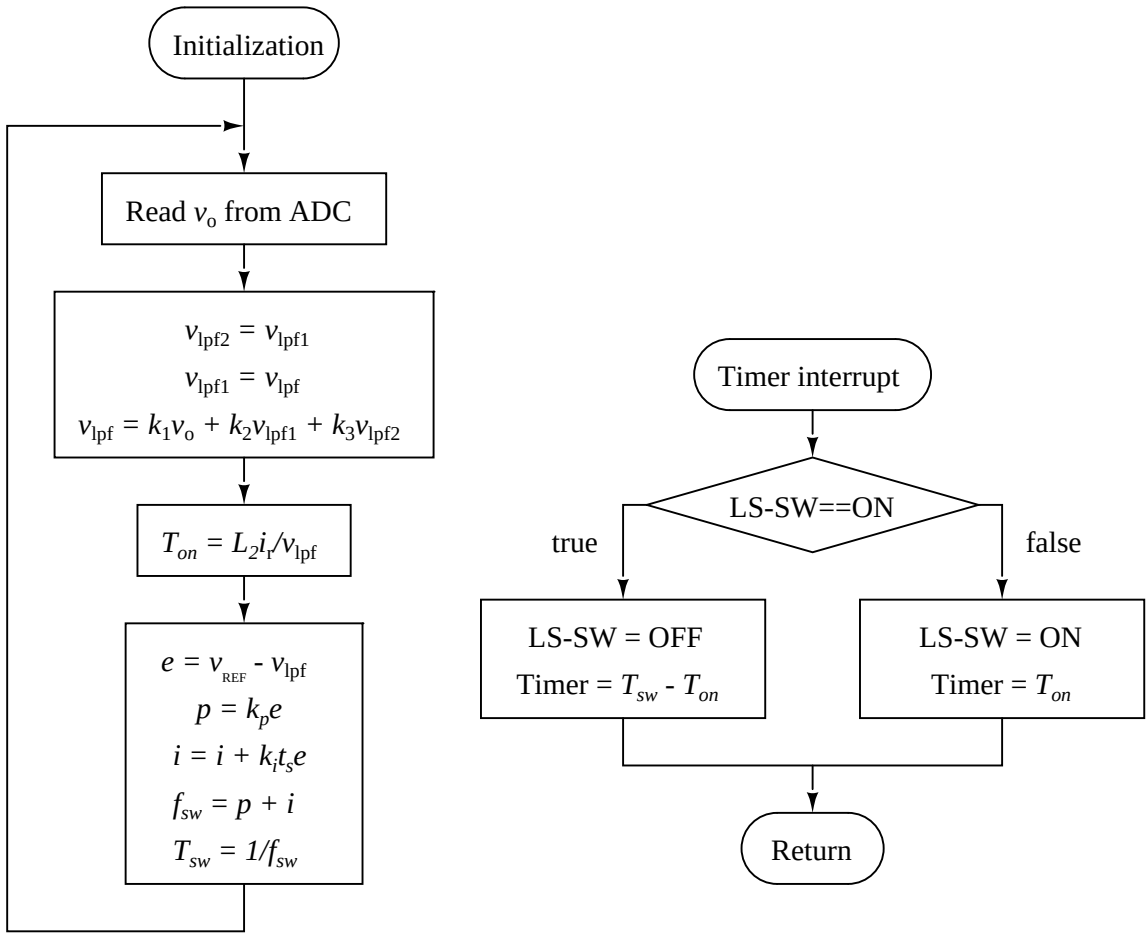

Figure 3.9: Flow chart of the μC program: the main loop (left) and the interrupt routine (right).

3.7 Micro-controller implementation

Texas Instrument MSP430 Launchpad (MSP-EXP430G2), shown in Figure 3.10, is used as μC. This is ultra-low power μC which features:

- 16MHz CPU speed;
- 16kB Flash;
- 512B RAM;
- 8ch 10-bit ADC;
- Comparator;
- 2 16-bit Timers.

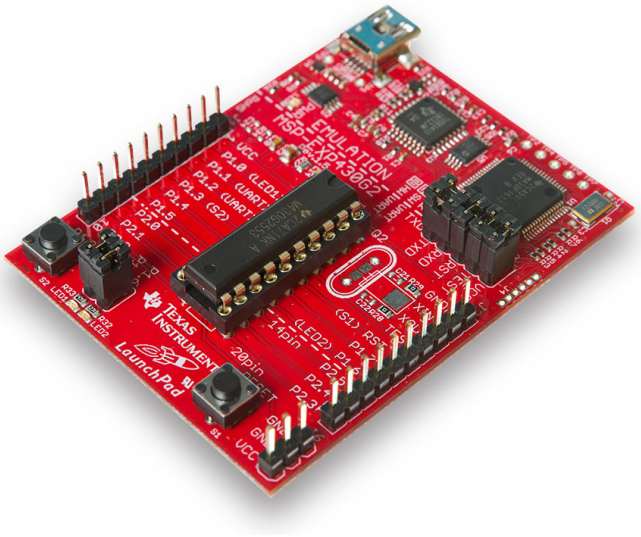

Figure 3.10: *Texas Instrument MSP430 Launchpad (MSP-EXP430G2)*.

The μC implements all the operations described in Section 3.6. During the initialization of the program, the following operations are implemented:

- the constants are declared;
- variables are initialized;
- the watchdog timer is stopped;
- the digital I/O register is set;
- the ADC register is set;
- the CPU clock frequency is set;
- the timer register is set.

After the initialization, the program implements the flow chart shown in Figure 3.9. Furthermore, after the calculation of both T_{sw} and T_{on}, a saturation of these value is added. This is a safety feature, in order to avoid dangerous value of T_{sw} and T_{on}.

During the μC programming, *MSP430x2xx Family User's Guide* has been used as reference manual [20]. In Appendix B the whole μC program is shown.

A test of the μC program, without the converter connected, is made in order to measure the sampling period, t_s, i.e. the duration of a single iteration of the main loop. Due to the μC limited computing capacity, the measure shows $t_s = 200\mu$s, even though the CPU clock frequency is set to the maximum value $f_{clk} = 21.57$MHz.

The ADC conversion factor, k_{ADC} is obtained from the expression of the digital output of the converter N_{ADC}

$$N_{\mathrm{ADC}} = (2^b - 1)\,\frac{v_{IN} - V_{R-}}{V_{R+} - V_{R-}} \tag{3.25}$$

where b is the number of bits of the ADC, V_{R+} and V_{R-} are the ADC reference voltages and v_{IN} is the ADC input, which is given by

$$v_{IN} = v_{\mathrm{o}}\,\frac{R'}{R' + R''} \tag{3.26}$$

due to a voltage divider connected from the converter output, v_{o}, to the ADC input, v_{IN}. k_{ADC} results

$$k_{\mathrm{ADC}} = \frac{N_{\mathrm{ADC}}}{v_{\mathrm{o}}} = 6.75 \tag{3.27}$$

Detailed data about the k_{ADC} calculation is given in Table 3.1.

b	10	number of bits of the ADC
V_{R+}	1.5V	positive ADC reference voltage
V_{R-}	0V	negative ADC reference voltage
R'	4.7kΩ	voltage divider first resistance
R''	470kΩ	voltage divider second resistance

Table 3.1: k_{ADC} calculation data.

3.8 Scaled converter design

The studied converter is an large step-down ratio converter, with an input voltage of several kV. Therefore, the testing procedure of the prototype could be difficult and dangerous.

By implementing a single cell on the HS-SW, the converter operation is still the same. Therefore, it is possible to test the converter with a lower input voltage, i.e. the test of the prototype is easier and less dangerous. Since this project is focused on the modeling and the control of the converter, building a scaled prototype does not compromise the experimental verification. Furthermore, the HS-SW realization and testing is the focus of a previous project on the analyzed converter [13].

As described in Table 3.2, the scaled converter adopts an input voltage of 250V. This is because the voltage stress of the HS-SW, (2.3a), must be handled by a single cell. Furthermore, also the average output voltage, the average output power and the peak output current have been reduced for safety reasons.

	ORIGINAL	SCALED	
$\overline{v_\mathrm{i}}$	3kV	250V	average input voltage
$\overline{v_\mathrm{o}}$	100V	80V	average output voltage
$\overline{p_\mathrm{o}}$	70W	30W	average output power
L_tot	13.4mH	13mH	total inductance
N	4.6	2	turns ratio
C_out	10μF	10μF	output capacitance
i_p	16A	5A	positive peak output current
i_r	8A	1.5A	negative peak output current

Table 3.2: TI-buck prototypes data.

The whole closed-loop control design is summarized in a *Matlab* script, shown in Appendix B. From the converter specifications, the script implements:

- the calculation of the small-signal parameters;
- the design of a second order Butterworth low pass filter;
- the iterative design of the PI controller;
- the evaluation of the discrete-time equation constants.

Therefore, the script provides all the parameters needed by the μC program. Table 3.3 lists other data about the μC features and implementations.

f_{sw}	1.34kHz	estimated switching frequency
t_s	200μs	sampling period
k_{ADC}	6.75	ADC conversion factor
$\lvert H(j\omega_{sw})\rvert$	0.1	low-pass filter attenuation at f_{sw}
PM	80$^{\text{o}}$	phase margin
f_c	63.1Hz	loop gain crossing frequency

Table 3.3: Other data about the μC features and implementations.

3.9 Closed-loop simulations

Once the closed-loop converter is designed, the software *PLECS* is used for simulating the TI-buck static and dynamic behaviour. The model used for the simulations is shown in Appendix B. Figure 3.11 shows the static behaviour of the converter in standard conditions. Figure 3.12 and Figure 3.13 show the evolution of the output voltage after a step response of the reference voltage. Figure 3.14 and Figure 3.15 show the evolution of the output voltage after a step response of the output power, i.e. a step response of the load.

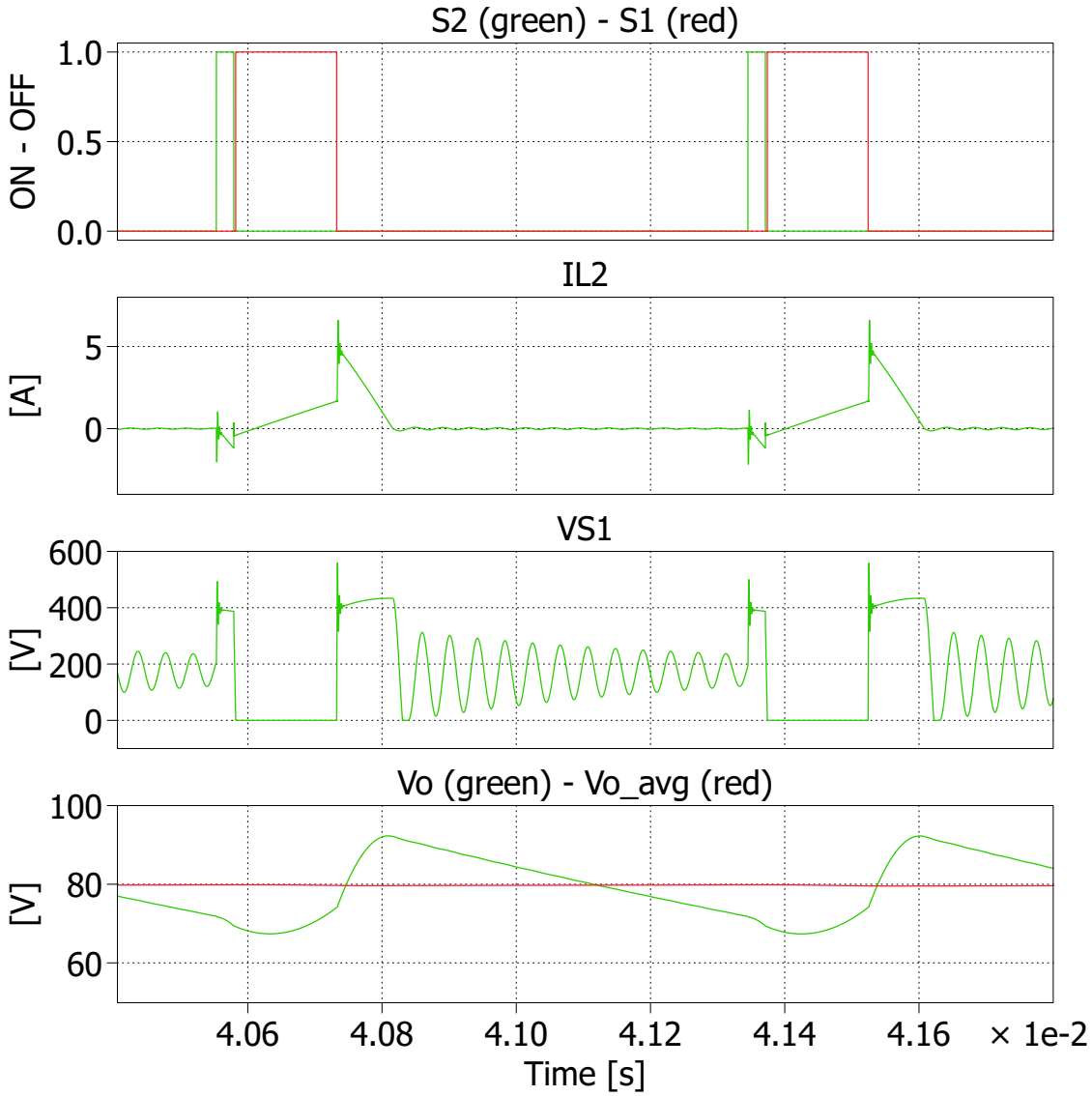

Figure 3.11: Simulation of the static behaviour of the scaled converter, showing a complete switching cycle.

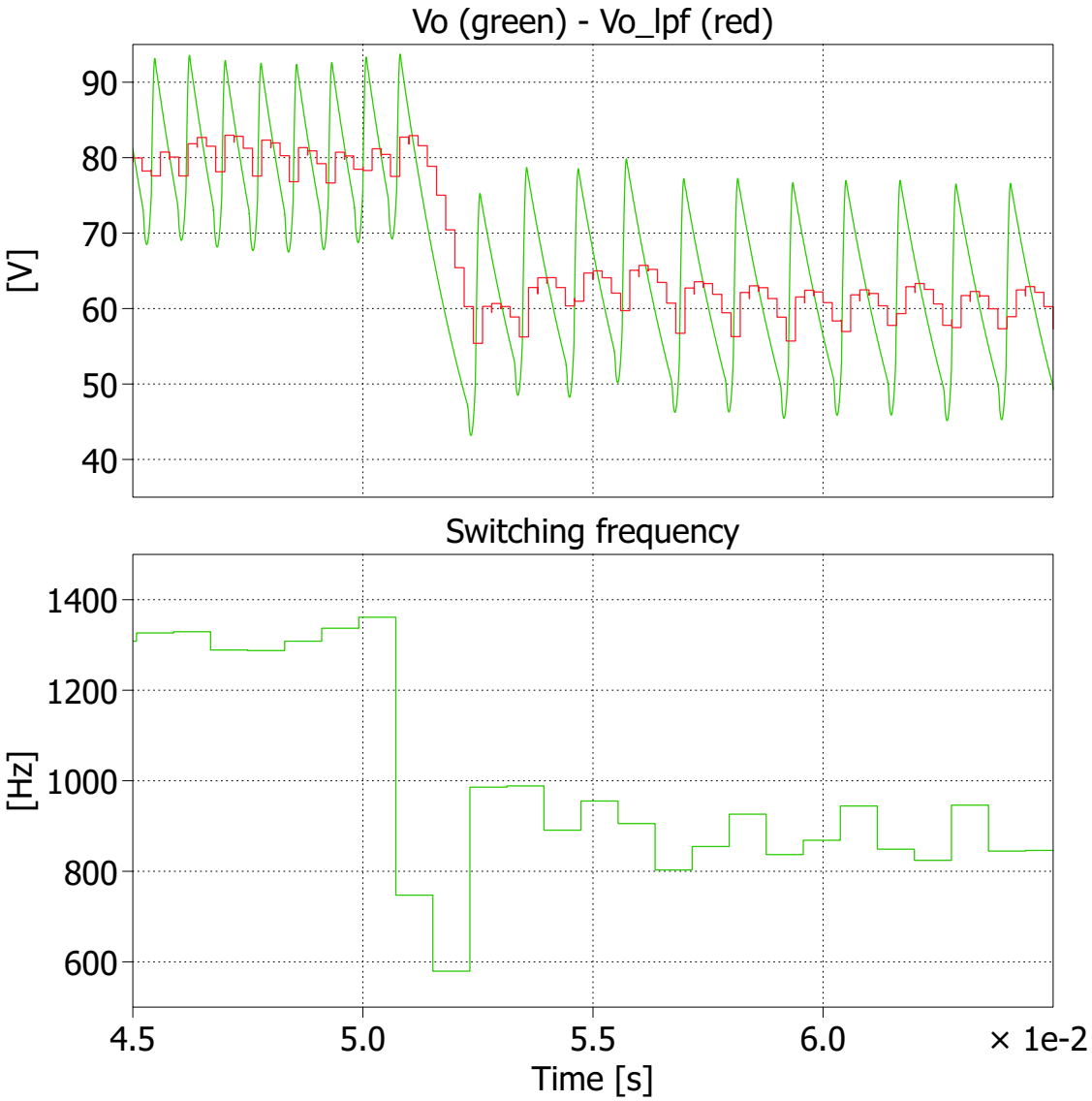

Figure 3.12: Evolution of the output voltage after a step response of the reference voltage. The reference voltage changes from 80V to 60V at $t_{step} = 50$ms.

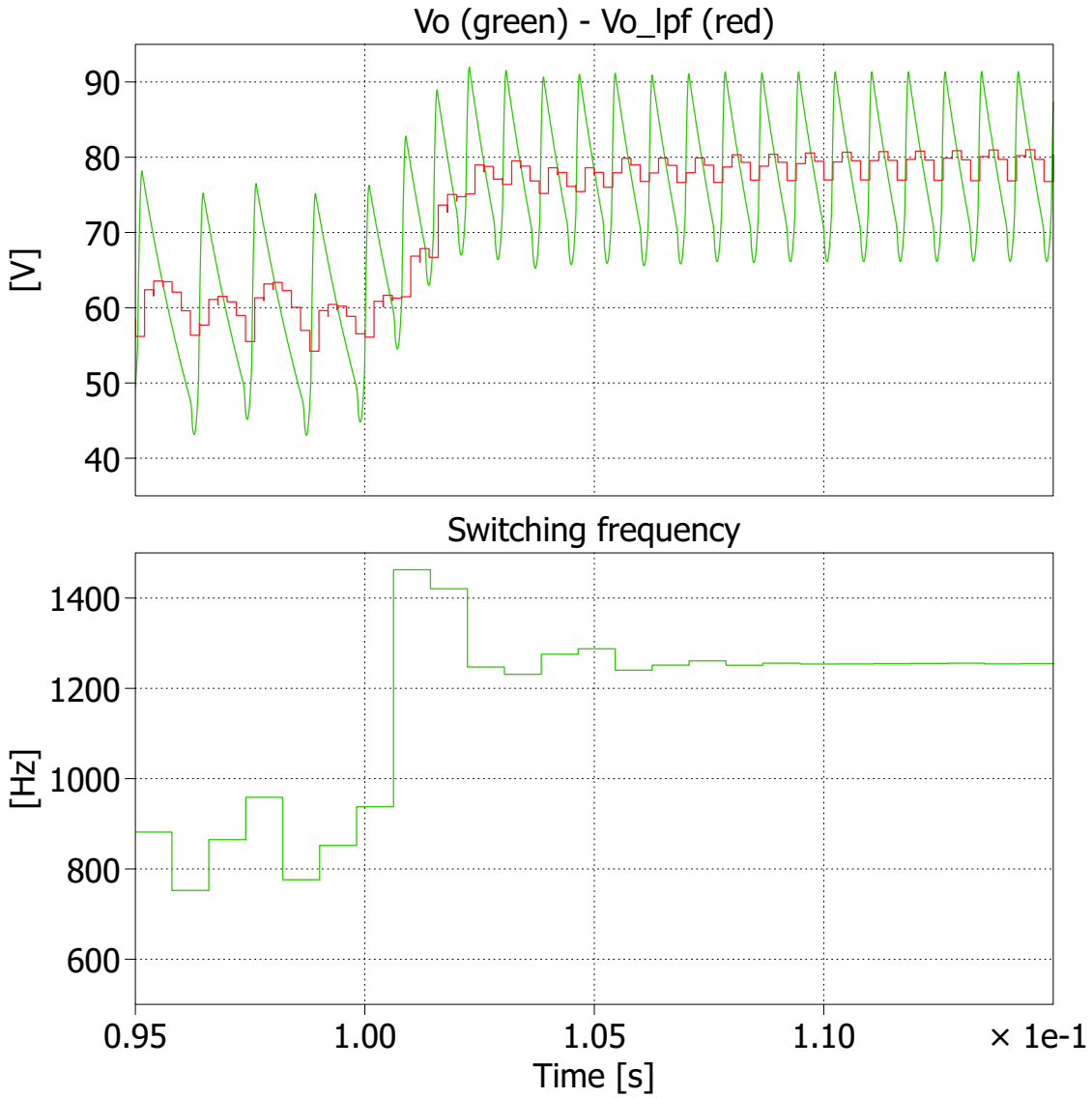

Figure 3.13: Evolution of the output voltage after a step response of the reference voltage. The reference voltage changes from 60V to 80V at $t_{step} = 100$ms.

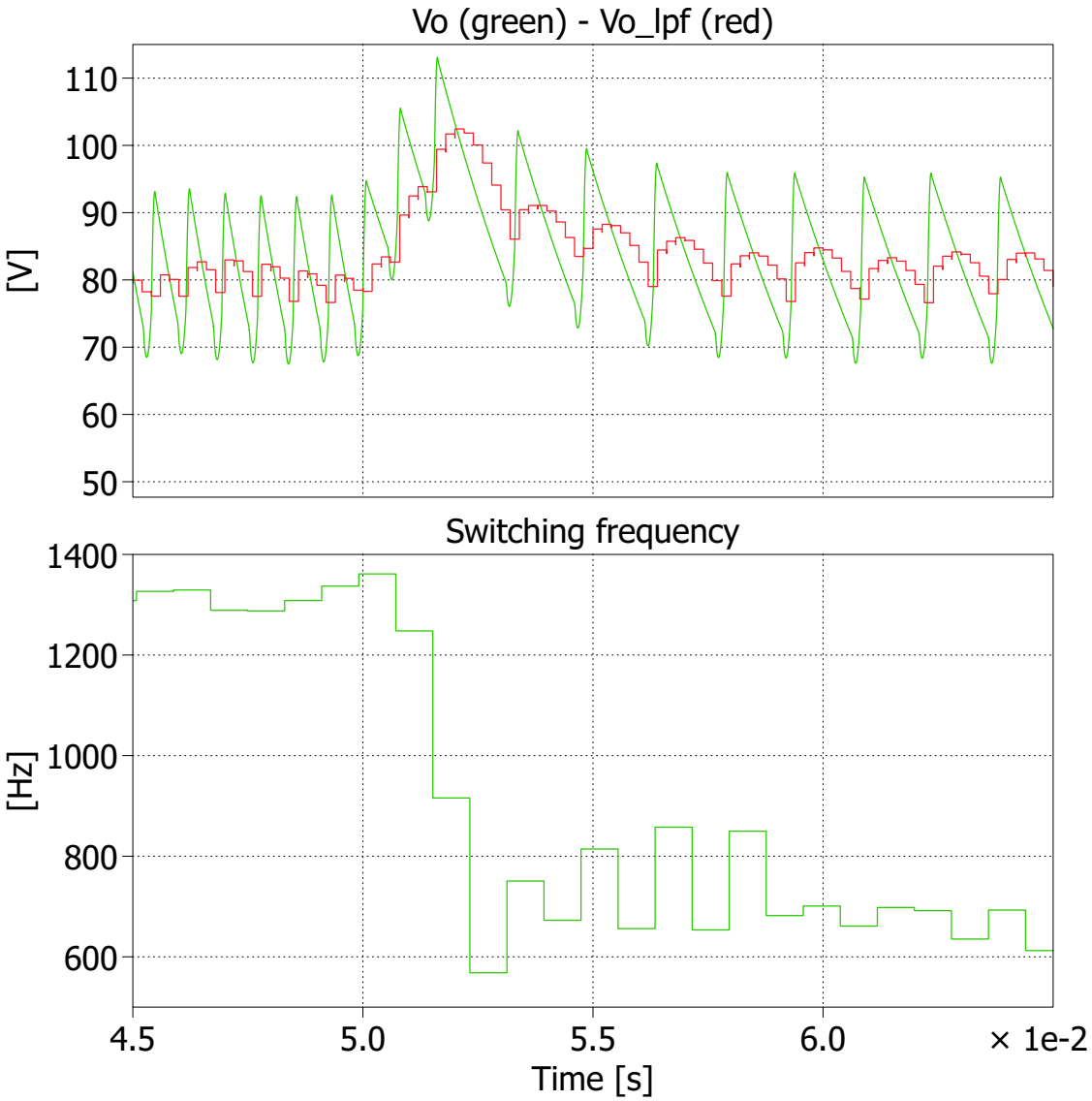

Figure 3.14: Evolution of the output voltage after a step response of the output power, i.e. a step response of the load. The output power changes from 30W to 15W at $t_{step} = 50$ms.

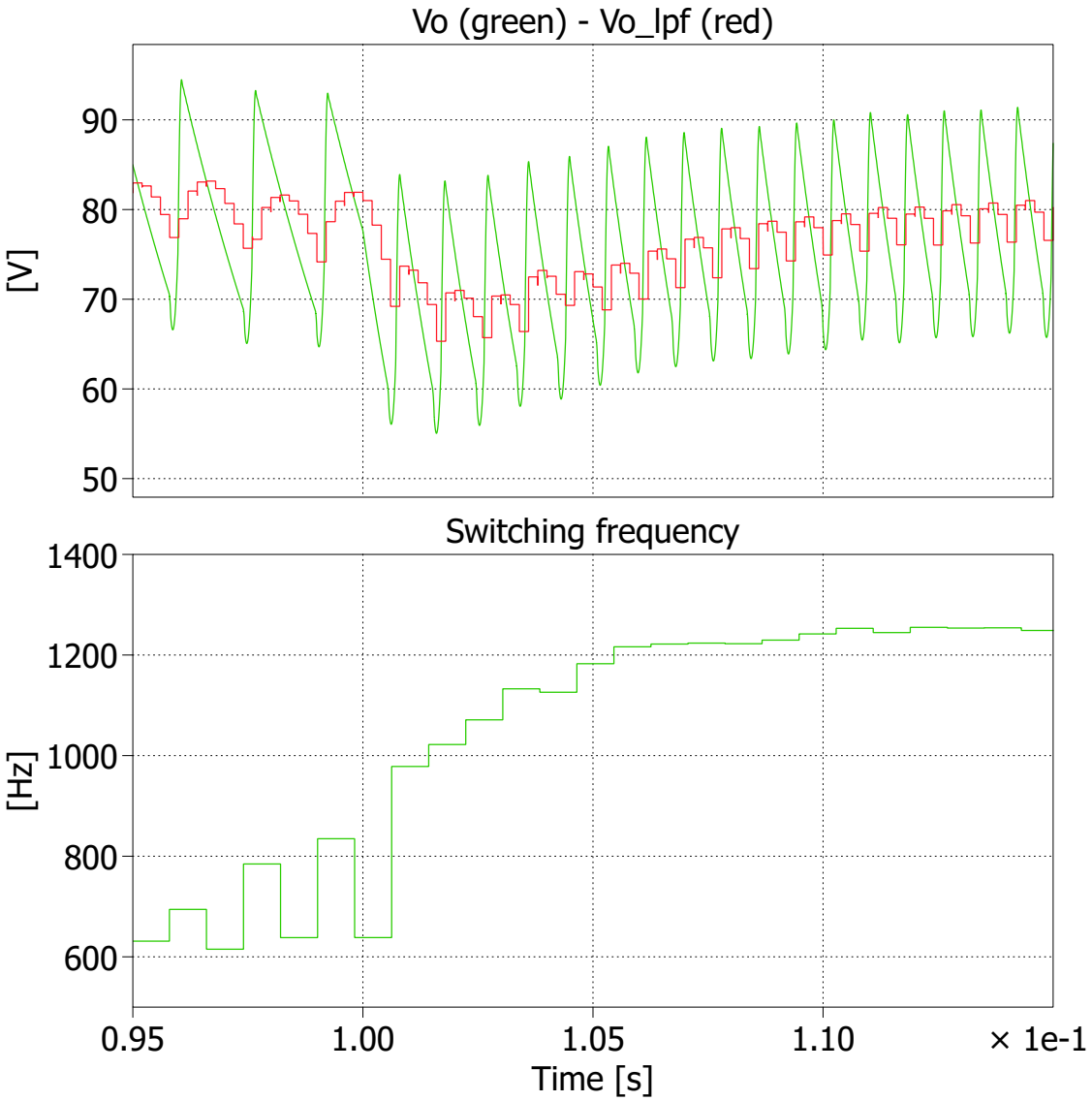

Figure 3.15: Evolution of the output voltage after a step response of the output power, i.e. a step response of the load. The output power changes from 15W to 30W at $t_{step} = 100$ms.

Chapter 4

Experimental verification

4.1 Open-loop testing

The scaled prototype described in Section 3.8 has been builded and tested. The complete schematics are shown in Appendix C. The experimental verification allows to check if the modeling and the closed-loop control design matches the real behaviour of the studied converter. Figure 4.1 shows a photograph of the builded prototype.

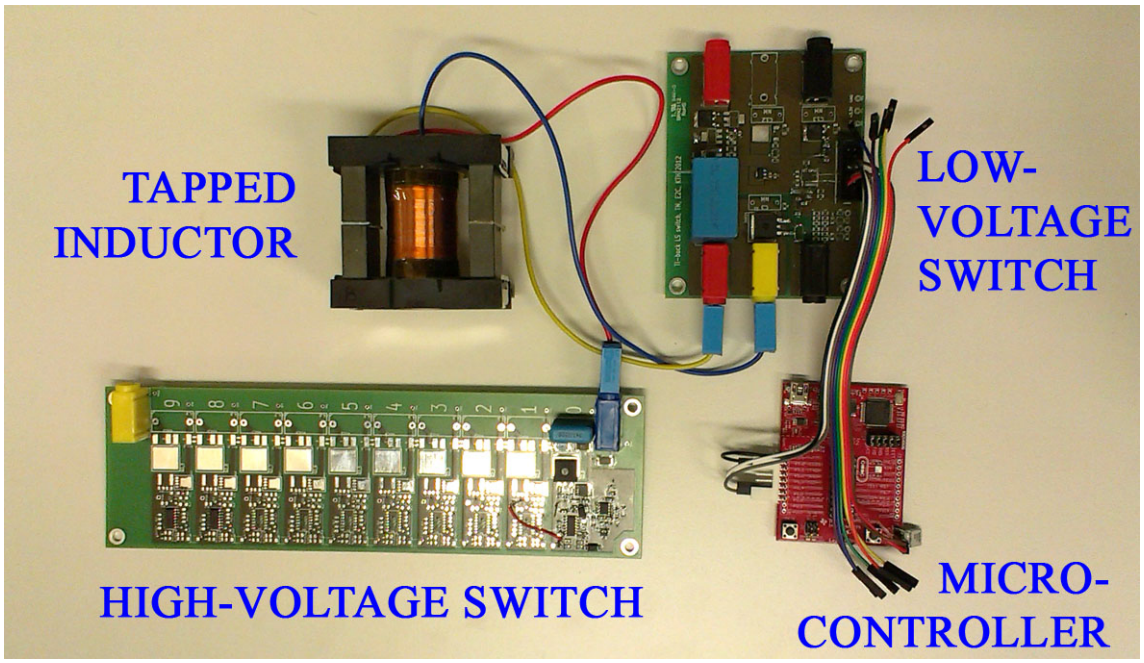

Figure 4.1: Photograph of the tapped-inductor buck converter. Since this is the scaled version, the HS-SW implements only one switching cell.

The first testing session is aimed to check the correctness of the converter operation, i.e. the static behaviour. Therefore, the converter is tested in open-loop and the μC is simply used as a pulse generator. This testing session helps to fix all the small and unavoidable problems which occur during the prototype realization, e.g. a bad soldering, etc.

Since the start-up procedure of the converter has not been studied yet, the output of the converter is connected to a constant voltage source, v_{test}, which provides the desired output voltage initial value. Figure 4.2 shows the converter set-up for the

open-loop testing. The start-up procedure of the converter is analyzed in Section 4.4.

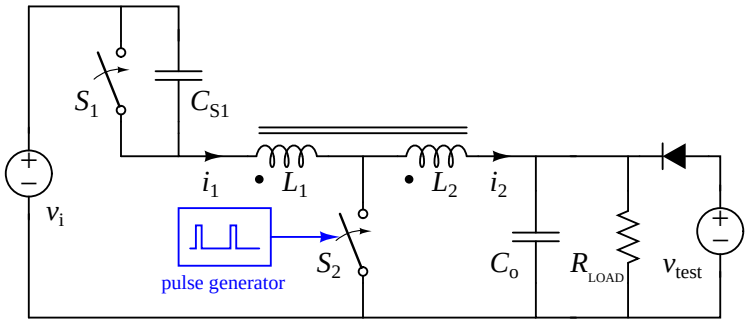

Figure 4.2: Open-loop testing set-up.

The LS-SW gate signal, the LS-SW drain signal, the output voltage and the output current are shown in figure Figure 4.3 all together, then in figures Figure 4.4, Figure 4.5 and Figure 4.6 individually with the LS-SW gate signal. The voltage across the HS-SW can not be measured with a standard probe, because it exceeds the probe maximum voltage ratings.

The open-loop testing session confirms that the converter operates as described in Section 2.2.

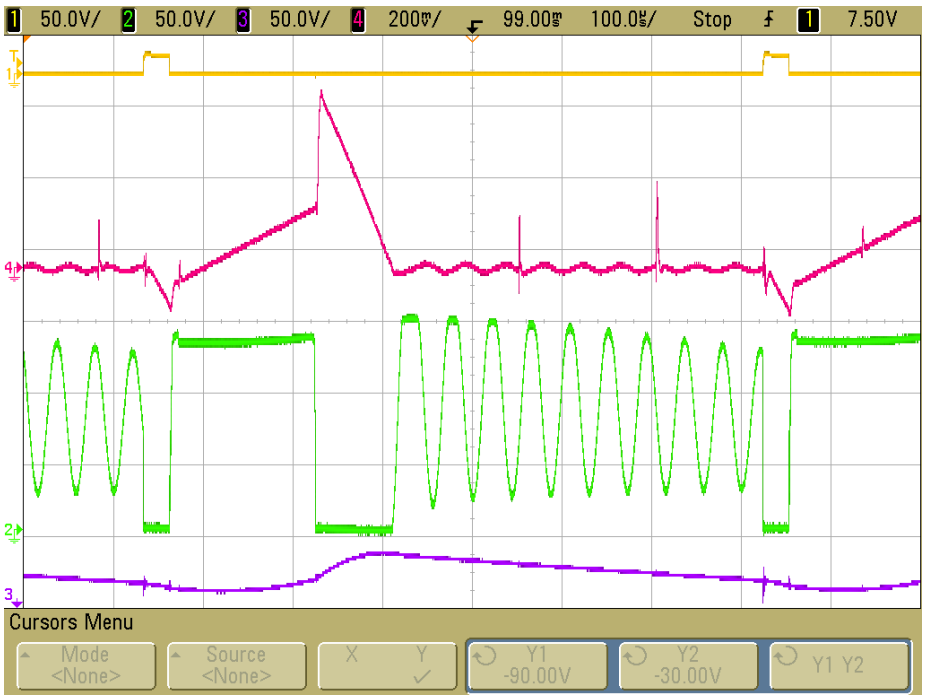

Figure 4.3: Measurement of the static behaviour of the converter, showing a complete switching cycle. The displayed waveforms are the LS-SW gate signal (yellow), the LS-SW drain signal (green), the output voltage (purple) and the output current (magenta). The current probe is set to 100mV/A.

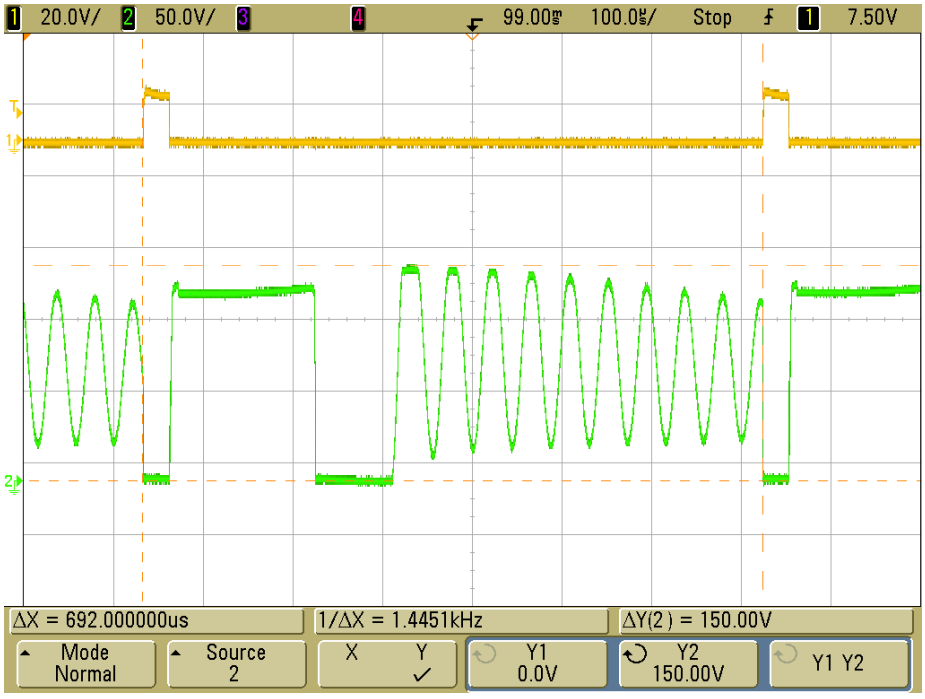

Figure 4.4: Measurement of the static behaviour of the converter, showing a complete switching cycle. The displayed waveforms are the LS-SW gate signal (yellow) and drain signal (green).

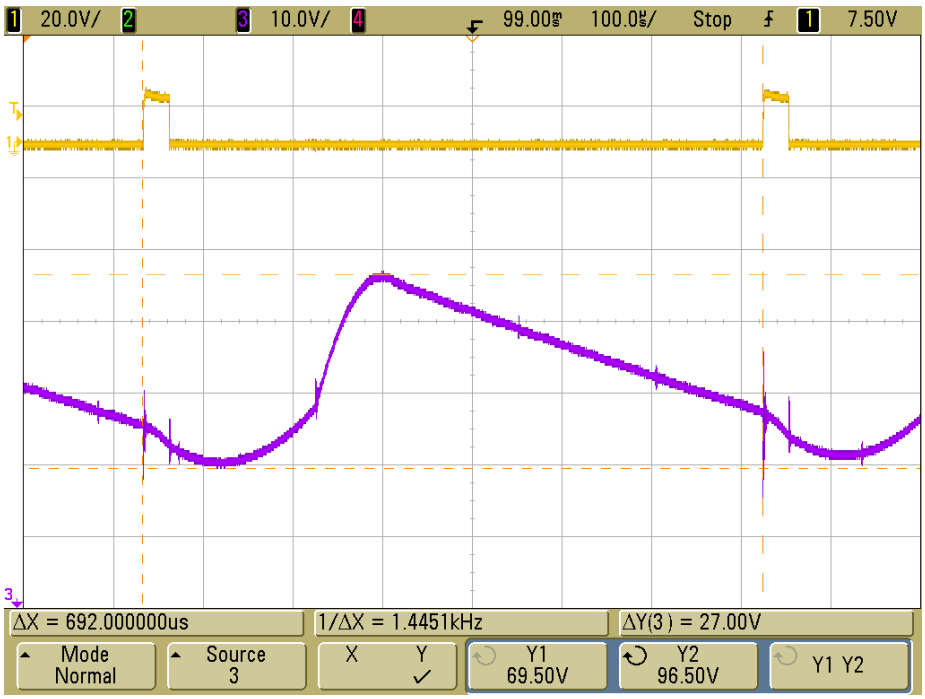

Figure 4.5: Measurement of the static behaviour of the converter, showing a complete switching cycle. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple). The cursors measure the peak-to-peak amplitude of the static ripple, which results $v_{ripple} = 27\text{V}$.

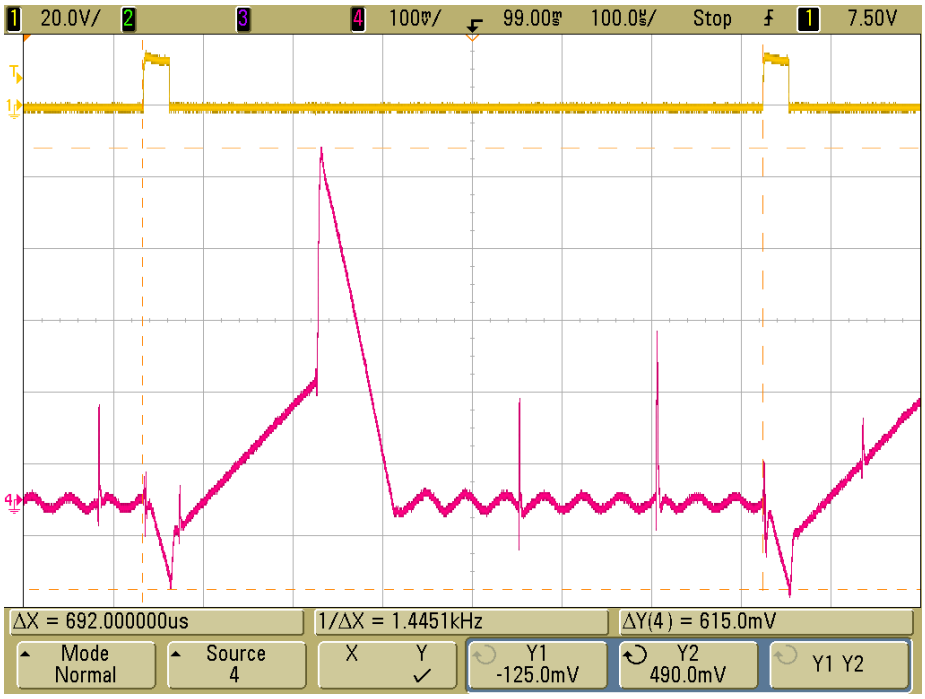

Figure 4.6: Measurement of the static behaviour of the converter, showing a complete switching cycle. The displayed waveforms are the LS-SW gate signal (yellow) and the output current (magenta). The current probe is set to 100mV/A. The cursors measure the positive and the negative peak output current, which result $i_p = 4.9\text{A}$ and $i_r = 1.25\text{A}$ respectively.

4.2 Closed-loop testing

This testing session is aimed to check the correctness of the closed-loop output voltage control. Therefore, the testing set-up features the μC connected in closed-loop mode. Based on the output voltage samples, the μC provides the LS-SW with a proper gate signal.

Since the start-up procedure of the converter has not been studied yet, the output of the converter is connected to a constant voltage source, v_{test}, which provides the desired output voltage initial value. Figure 4.7 shows the converter set-up for the closed-loop testing. The start-up procedure of the converter is analyzed in Section 4.4.

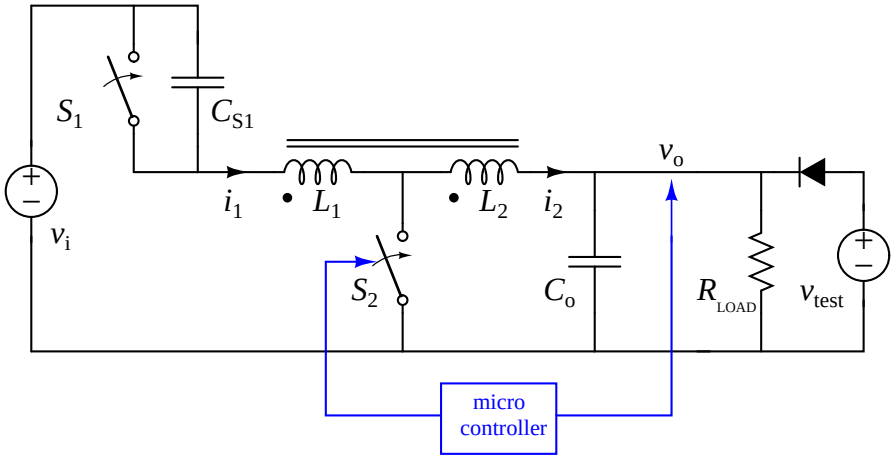

Figure 4.7: Closed-loop testing set-up.

Firstly, the output voltage is measured in standard condition, i.e. in absence of transient, as is shown in Figure 4.8. This measure shows two issues, which are investigated as follow.

Average output voltage

The average output voltage value is higher than 80V

$$\overline{v_o} \simeq 83\text{V} \tag{4.1}$$

This problem is due to error in the k_{ADC} calculation (3.27). Since in the digital domain $v_{ref\_dig} = k_{ADC} v_{ref}$, an error in k_{ADC} causes an error in $\overline{v_o}$.

In the worst case, when due to the tolerances R' is minimum and R'' and V_{R+} are maximum, k_{ADC} assumes the minimum value

$$k_{ADC\_min} = \frac{(2^b - 1)}{V_{R+\_min}} \frac{R'\_max}{R'\_max + R''\_min} = 6.25 \tag{4.2}$$

therefore the μC sets the output voltage to the value v_{o_max}

$$v_{o\_max} = v_{ref} \frac{k_{ADC}}{k_{ADC\_min}} = 86.5\text{V} \tag{4.3}$$

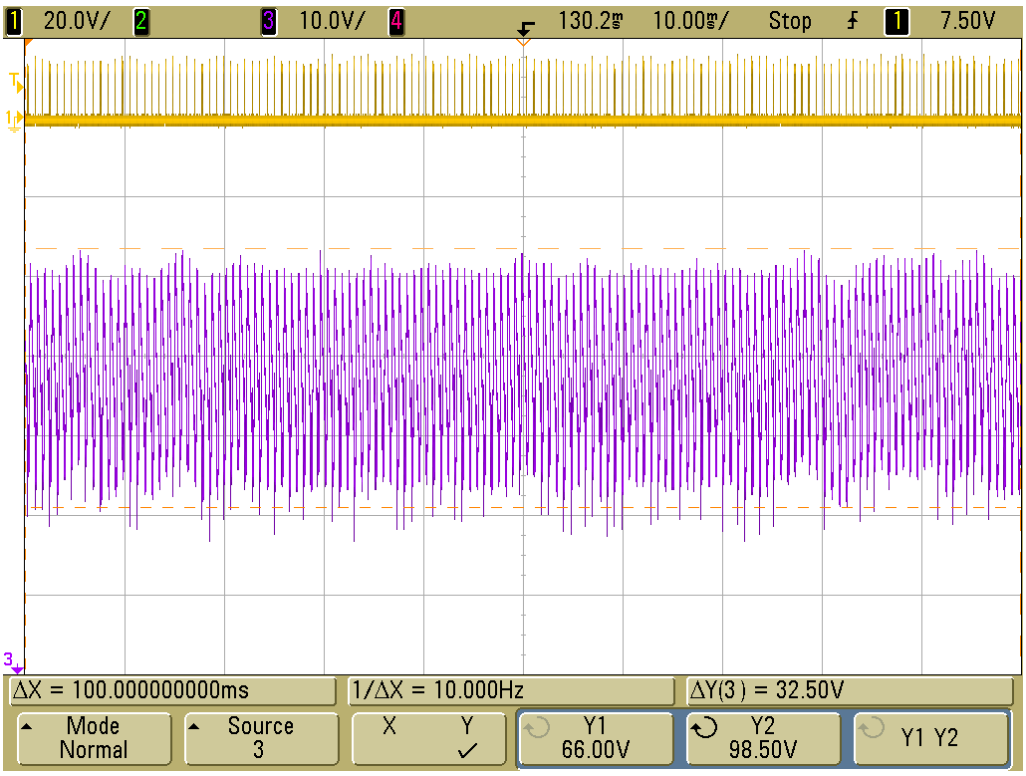

Figure 4.8: Closed-loop output voltage in standard condition, i.e. in absence of transient. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple). The cursors measure the maximum and the minimum value of the output voltage. Since $v_{ripple} = 27\text{V}$ the peak-to-peak amplitude of the low-frequency noise results $v_{noise} = 5.5\text{V}$.

Similarly, when due to the tolerances k_{ADC} assumes the maximum value $k_{ADC\_max} = 7.33$, the μC sets the output voltage to the value

$$v_{o\_min} = 73.7\text{V} \tag{4.4}$$

The measured average output voltage fits in the range $v_{o\_min} \div v_{o\_max}$, therefore is acceptable.

Low-frequency noise

A significant low-frequency noise is overlapped to the output voltage. Also the switching frequency contains a significant low-frequency noise, which is a symptom of a problem in the control system. The same problem can be observed in the simulation, shown in Figure 4.9.

This problem is caused by the value of the sampling frequency $f_{sample} = 5\text{kHz}$, which is too low compared to the switching frequency $f_{sw} = 1.3\text{kHz}$. The above-mentioned sampling frequency does not allow to reconstruct the output voltage waveform in the digital domain with sufficient precision, causing the low-frequency noise.

A simulation with a sampling frequency $f'_{sample} = 100\text{kHz}$ confirms that the low-frequency noise is caused by a low sampling frequency.

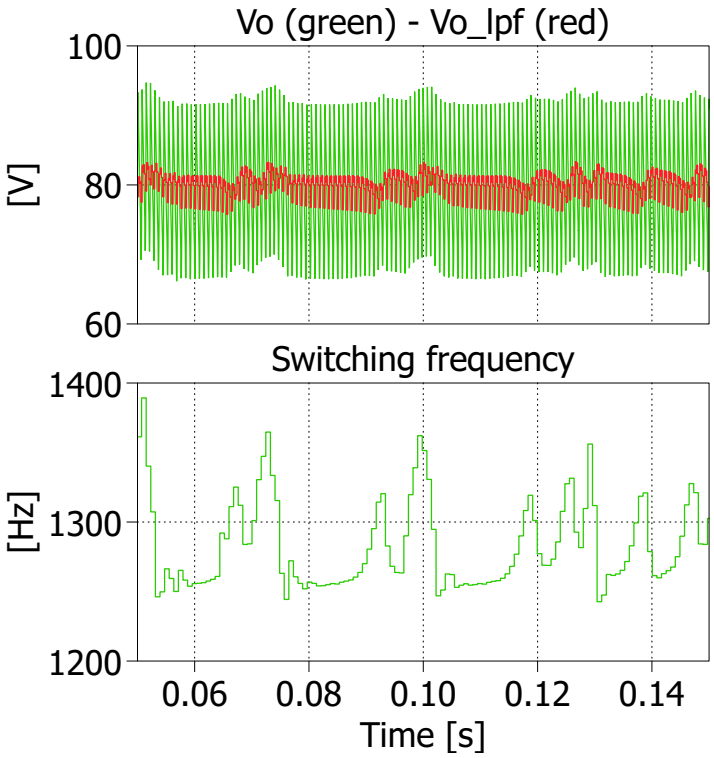

Figure 4.9: Simulation of the closed-loop converter in standard condition. A low-frequency noise is overlapped to the output voltage and the switching frequency.

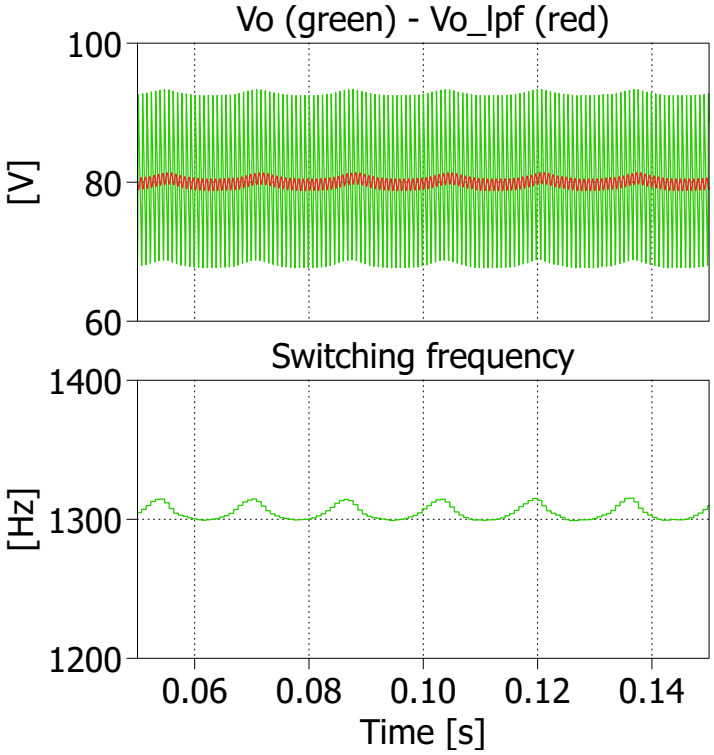

Figure 4.10: Simulation of the closed-loop converter with a sampling frequency f'_{sample} = 100kHz. This simulation confirms that the low-frequency noise is caused by a low sampling frequency.

Dynamic response

The closed-loop performance is tested also in transient conditions, specifically:

- evolution of the output voltage after a step response of the reference voltage, from 80V to 70V;
- evolution of the output voltage after a step response of the output power, i.e. a step response of the load, from 30W to 15W.

Measured waveforms are shown in Figure 4.11 and Figure 4.12.

Furthermore, a comparison between the measured waveforms and the model prediction (3.6) is made. In order to be overlapped with the model prediction, the measured waveforms are post-processed as follow:

- the data is exported from the oscilloscope and imported with *Matlab*;
- the data is low-pass filtered in order to remove the static ripple;
- the data is normalized to a unit step response of v_{ref} and i_o respectively. Specifically:
  - the average value before the step (4.1) is subtracted;
  - a division by the amplitude of the step is made

$$v'_{ref} - v_{ref} = 70 - 80 = -10\text{V} \tag{4.5}$$

and

$$i'_o - i_o = \frac{15 - 30}{80} = -187.5\text{mA} \tag{4.6}$$

The comparison is shown in Figure 4.13 and Figure 4.14. Since the low-frequency noise has a strong impact on the comparison between the measured waveforms and the model prediction, the performances of the closed-loop control can not be evaluated with precision.

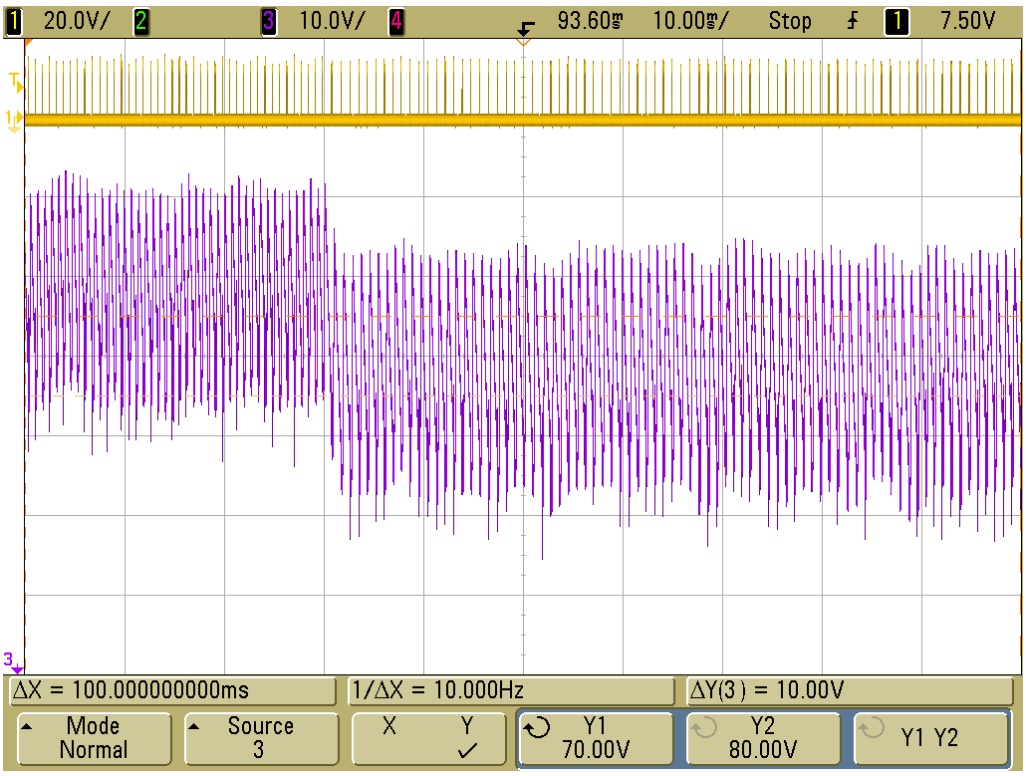

Figure 4.11: Evolution of the closed-loop output voltage after a step response of the reference voltage, from 80V to 70V. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple).

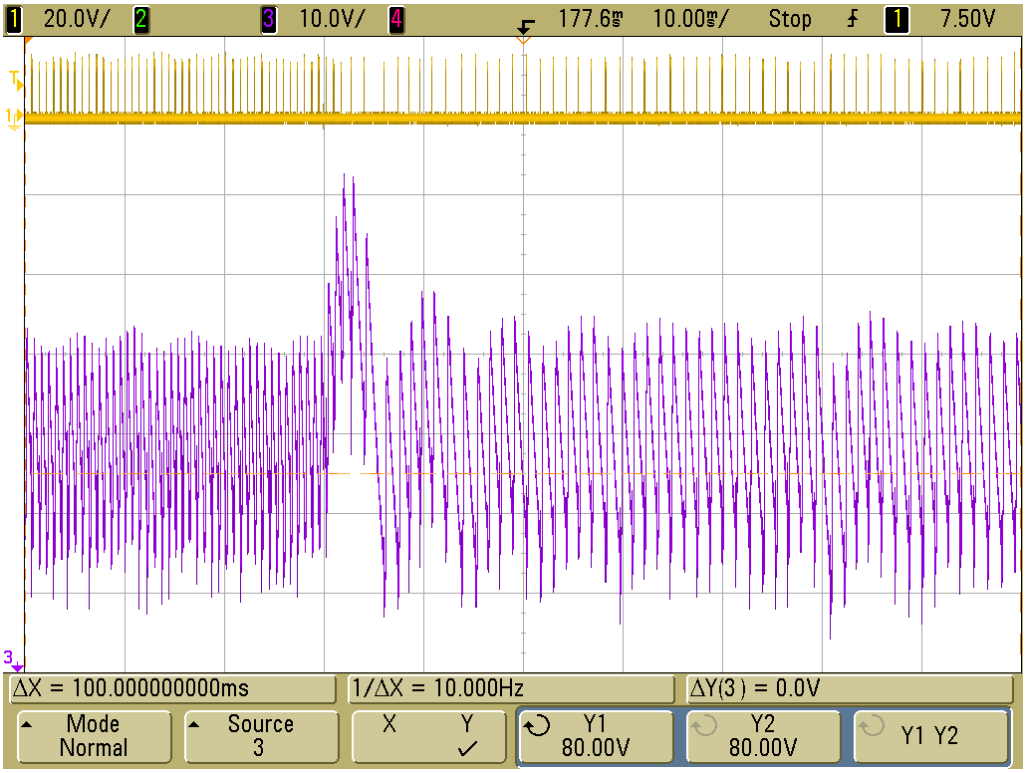

Figure 4.12: Evolution of the output voltage after a step response of the output power, i.e. a step response of the load, from 30W to 15W. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple).

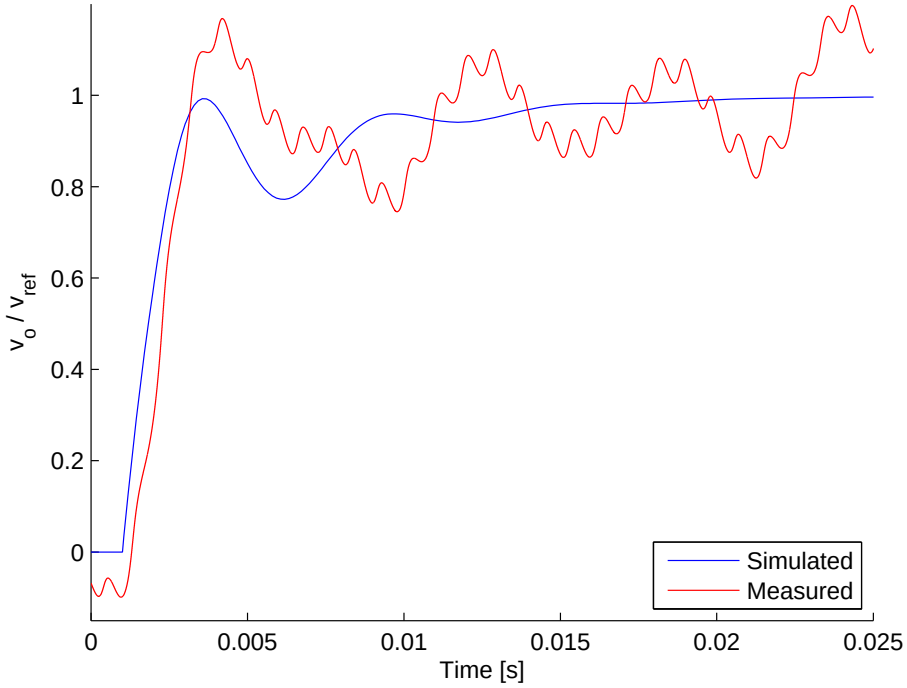

Figure 4.13: Comparison between the measured waveforms with the model prediction: evolution of the closed-loop output voltage after a unit step response of the reference voltage v_{ref}.

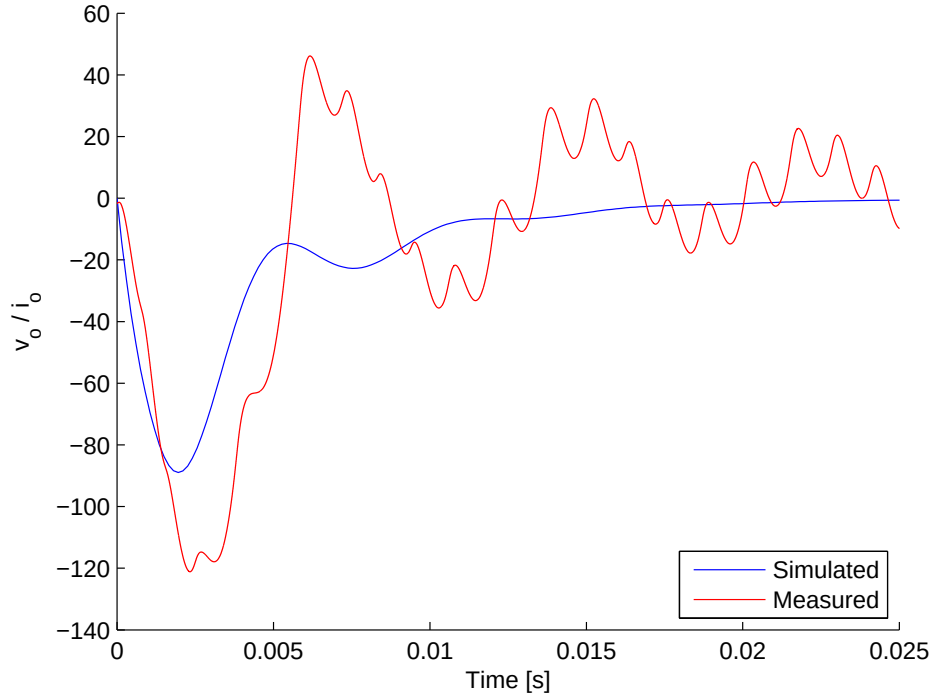

Figure 4.14: Comparison between the measured waveforms with the model prediction: evolution of the output voltage after a step response of the output current i_o.

4.3 Model evaluation

As observed in the previous Section, the low-frequency noise has a strong impact on the comparison between the measured waveforms and the model prediction. Therefore, the performances of the closed-loop control can not be evaluated from the previous testing session.

In order to overcome this problem, the value of the output capacitance can be increased. A higher value of C_o implies:

- a lower output voltage static ripple, which improves the reconstruction of the the output voltage waveform in the digital domain;
- a higher time constant τ_o in (3.4), which reduces the loop gain crossing frequency ω_c;
- a slower start-up of the converter, described in detail in Section 4.4.

The increase of the output capacitance is only aimed to the evaluation of the closed-loop control model, because the value of C_o chosen in Section 3.8 matches the requirements of the application of interest.

The new value of the output capacitance is $C'_o = 50\mu F$ (5x10μF).

Firstly, the output voltage is measured in standard condition, i.e. in absence of transient, as is shown in Figure 4.15. With the new value of the output capacitance, both static ripple and low-frequency noise have been reduced roughly 5 times.

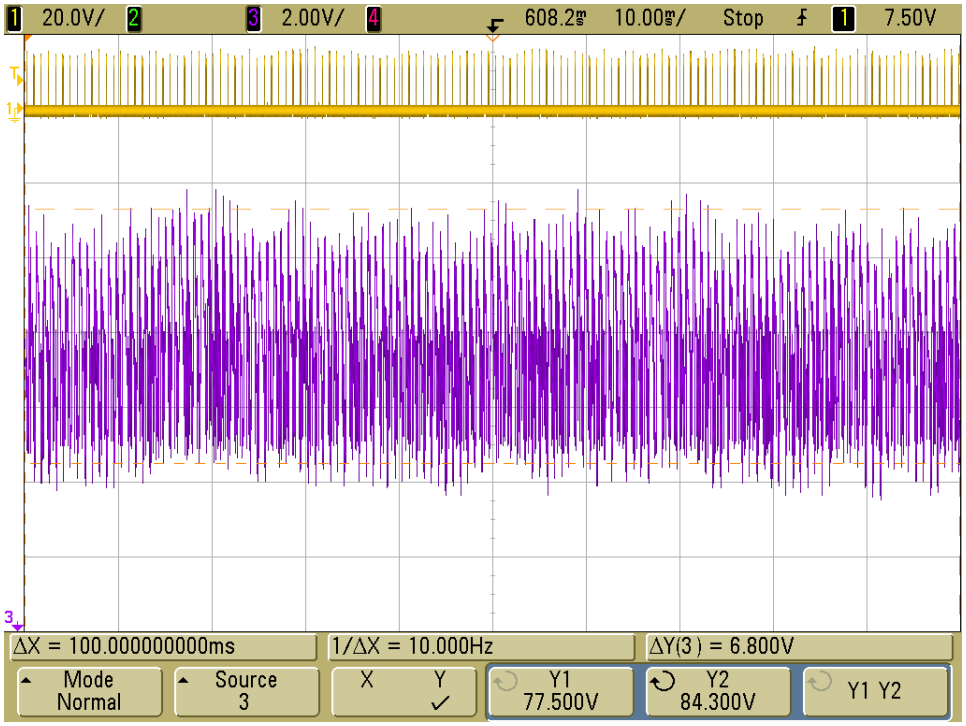

Figure 4.15: Closed-loop output voltage in standard condition, i.e. in absence of transient. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple). With the new value of the output capacitance, the peak-to-peak output voltage has been reduced roughly 5 times.

Dynamic response

The closed-loop performance is tested also in transient conditions, specifically:

- evolution of the output voltage after a step response of the reference voltage, from 80V to 70V;
- evolution of the output voltage after a step response of the output power, i.e. a step response of the load, from 30W to 15W.

Measured waveforms are shown in Figure 4.16 and Figure 4.17.

A comparison between the measured waveforms, the *PLECS* simulations and the analytical model (3.6) is made, as described in Section 4.2. The comparison is shown in Figure 4.18 and Figure 4.19.

The low-frequency noise still interferes with the evaluation of the closed-loop performances, but less then before.

The evolution of the output voltage after a step response of the reference voltage shows no overshoot in each of the three cases. The analytical model is slower than the other waveforms. Also the *PLECS* simulation model does not give an exact prediction of the real behaviour of the converter, but is more accurate than the analytical model. This implies that the approximations on which the model is based make the model slower than reality.

The evolution of the output voltage after a step response of the output power, i.e. a step response of the load, shows no overshoot in the analytical model and in the *PLECS* simulation, while it shows an overshoot comparable with the low-frequency noise in the measured waveform. Similarly to the step response of the reference voltage, the analytic model is slower than the other two waveforms, while the *PLECS* simulation waveform is more accurate.

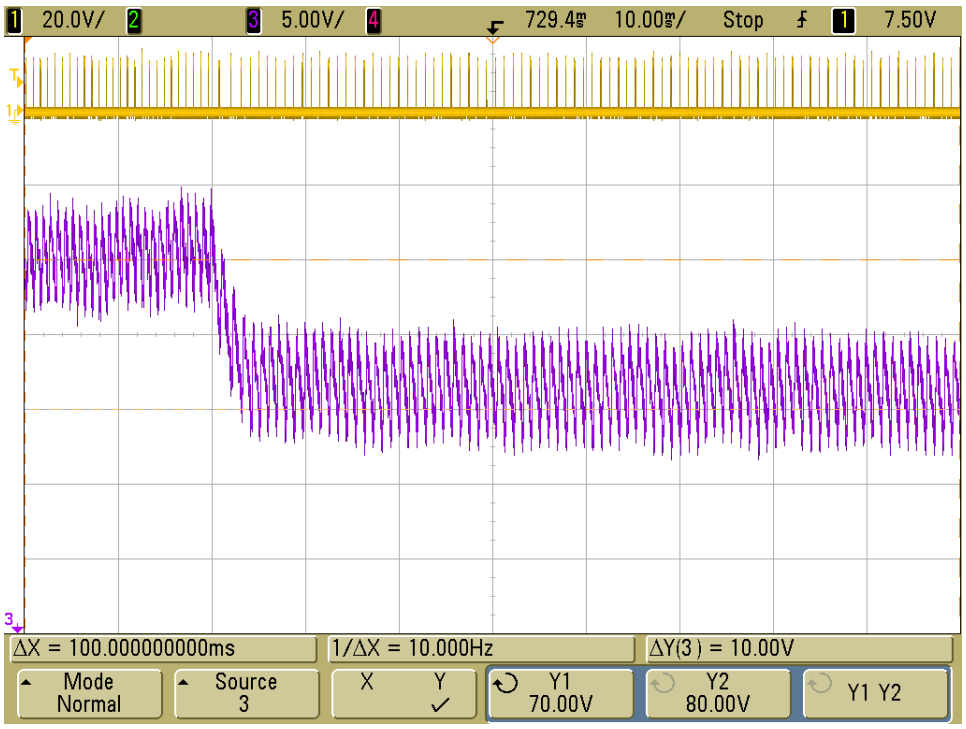

Figure 4.16: Evolution of the closed-loop output voltage after a step response of the reference voltage, from 80V to 70V. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple).

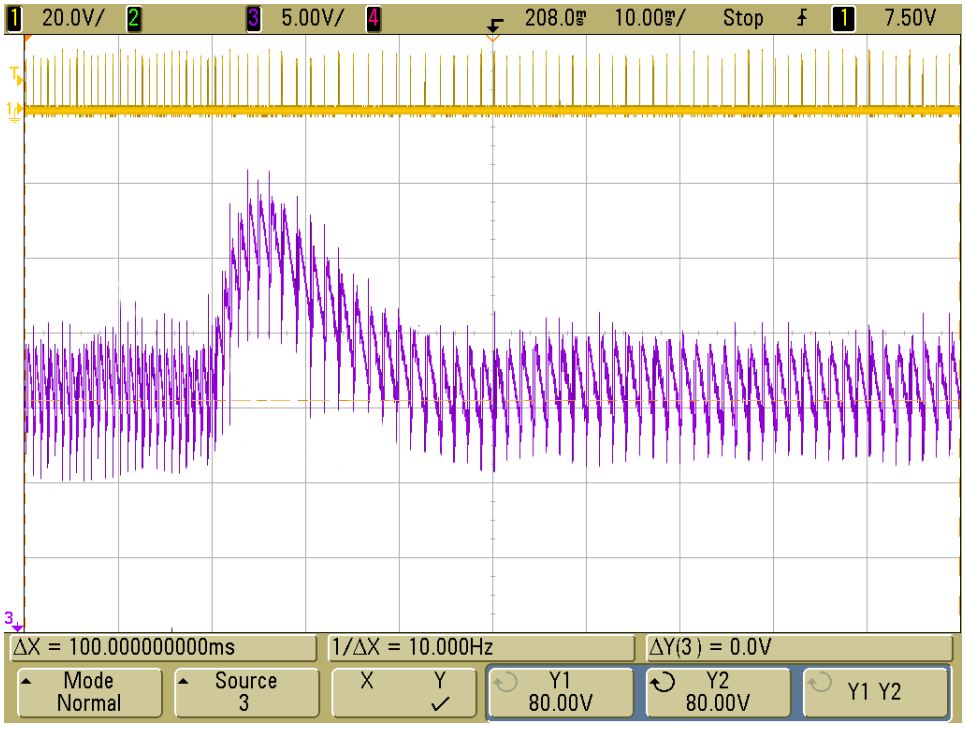

Figure 4.17: Evolution of the output voltage after a step response of the output power, i.e. a step response of the load, from 30W to 15W. The displayed waveforms are the LS-SW gate signal (yellow) and the output voltage (purple).

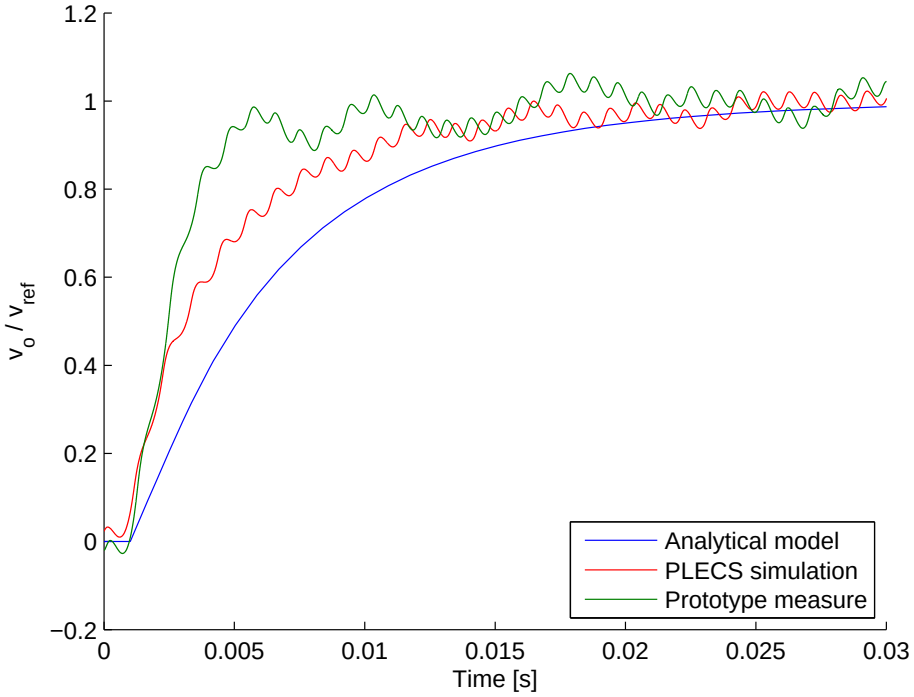

Figure 4.18: Comparison between the measured waveforms with the model prediction: evolution of the closed-loop output voltage after a unit step response of the reference voltage v_{ref}.

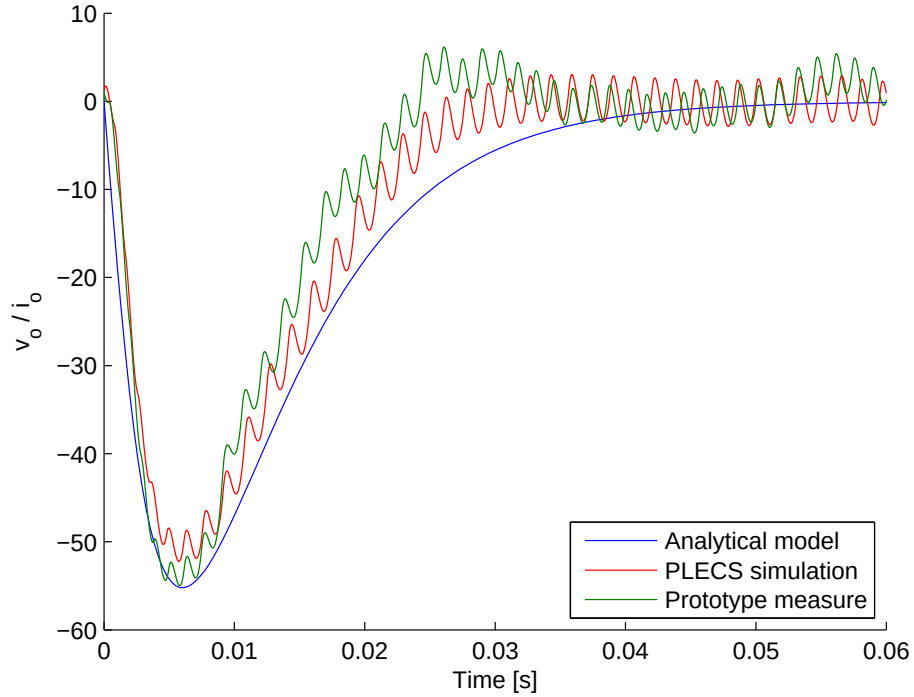

Figure 4.19: Comparison between the measured waveforms with the model prediction: evolution of the output voltage after a step response of the output current i_o.

4.4 Start-up procedure of the converter

This Section describes how the start-up procedure of the converter is studied and implemented. When energized from the high-voltage side, the studied converter should be a completely autonomous device. In other words, when the input voltage is provided, the converter should be able to turn itself on and start the switching operation.

In order to start the switching operation, two auxiliary supply voltages must be provided:

- the LS-SW gate driver supply voltage, $v_{gd} = 12V$, which consists in a linear voltage regulator connected to the output terminal;
- the micro-controller supply voltage, $v_{\mu C} = 3.3V$, which consists in a linear voltage regulator connected to the LS-SW gate driver supply voltage v_{gd}.

If these supply voltages are not provided, the converter can not start the switching operation.

The converter schematic analyzed so far does not implement the start-up procedure. When the input voltage is provided to the converter in the off state, it simply causes the voltage across the HS-SW to be equal to v_i. The two auxiliary supply voltage are not provided and the converter can not start the switching operation.

First solution

A first solution is proposed in Figure 4.20. The schematic features:

- a resistance R_{S1} added in parallel to the HS-SW;
- a switch $S3$ connected in series to the load.

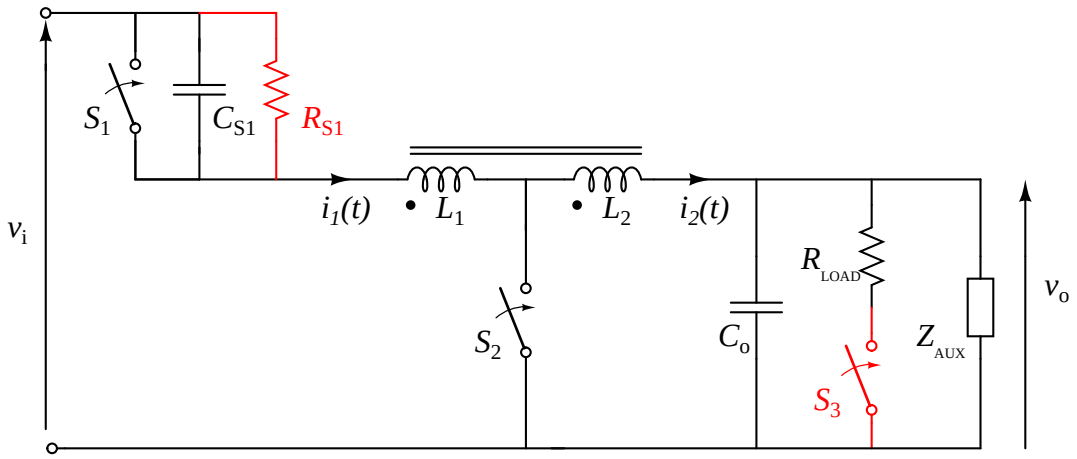

Figure 4.20: Circuit schematic showing the first solution for the start-up procedure of the converter. The component Z_{AUX} symbolizes the sub-circuit containing the two linear voltage regulator for the two auxiliary supply voltage.

Since the resistance R_{S1} has a MΩ order of magnitude, it does not affect the converter operation and does not cause relevant losses. The start-up procedure featured by this solution is described as follow:

- the input voltage is provided;
- the output capacitor is slowly charged through R_{S1}; given that the component values, C_{S1} and L_{tot} can be neglected during this transient, the output voltage can be expressed as

$$v_o(t) = (1 - \mathrm{e}^{-\frac{t}{R_{S1}C_o}})v_i \tag{4.7}$$

- at a certain value of the output voltage $v_o(t) = v_{aux\_on}$ the two auxiliary supply voltage are provided;
- the μC turns on;
- the μC closes the switch $S3$, connecting the load to the ground terminal;
- the converter starts the switching operation;

Unfortunately, this solution does not work. The sub-circuit Z_{AUX}, which symbolizes the two linear voltage regulator for the two auxiliary supply voltage, establishes a voltage divider between R_{S1} and Z_{AUX}, which limits the output voltage to only a few volts.

Second solution

In order to overcome the voltage divider problem, a second solution is proposed, as shown in Figure 4.21. The schematic features:

- a resistance R_{S1} added in parallel to the HS-SW;
- a switch $S3$ connected in series to the load;
- a SCR-DIAC sub-circuit, connected between the output terminal and Z_{AUX}.

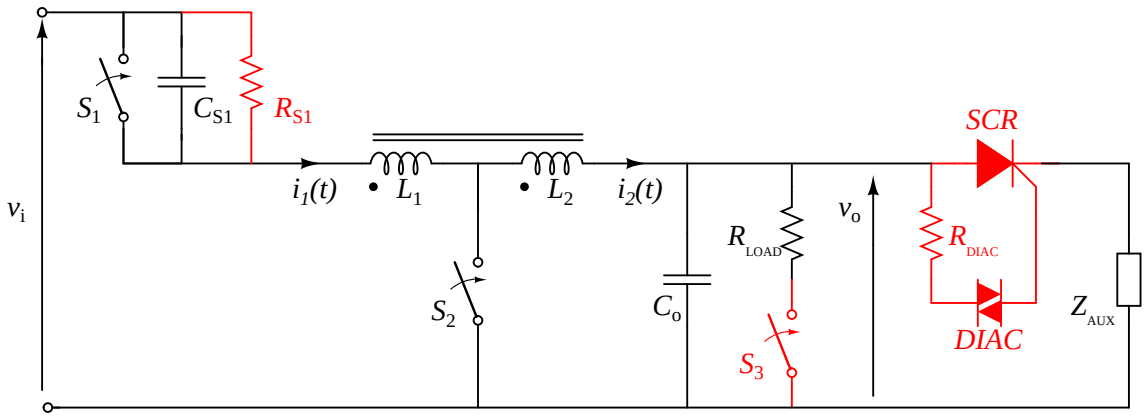

Figure 4.21: Circuit schematic showing the second solution for the start-up procedure of the converter.

The start-up procedure featured by this solution is described as follow:

- the input voltage is provided;
- since the SCR is in the off state, Z_{AUX} is disconnected from the output terminal;

- the output capacitor is slowly charged through R_{S1}

$$v_o(t) = (1 - \mathrm{e}^{-\frac{t}{R_{S1}C_o}})v_i \tag{4.8}$$

- at a certain value of the output voltage $v_o(t) = v_o^*$ the DIAC turns on, providing a current pulse $I_{pulse} = \frac{v_o^*}{R_{DIAC}}$;
- the current pulse I_{pulse} turns on the SCR, which connects Z_{AUX} to the output terminal;
- given that $v_o^* > v_{aux\_on}$, the two auxiliary supply voltage are provided;
- the μC turns on;
- the μC closes the switch $S3$, connecting the load to the ground terminal;
- the converter starts the switching operation;

Experimental verification

The first test is aimed to measure the minimum voltage required by the two auxiliary supply voltage. It results

$$v_{aux\_on} \simeq 24\mathrm{V} \tag{4.9}$$

Then, a DIAC featuring a breakdown voltage $v_{DIAC} = 32\mathrm{V}$ is chosen, so that

$$v_{DIAC} > v_{aux\_on} \tag{4.10}$$

A SCR for generic application is chosen, which features a gate trigger current

$$5\mu\mathrm{A} < I_{GT} < 200\mu\mathrm{A} \tag{4.11}$$

A $R_{DIAC} = 470\mathrm{k}\Omega$ is chosen, so that the current pulse is in the I_{GT} range

$$I_{pulse} = 68\mu\mathrm{A} \tag{4.12}$$

Since this is a scaled prototype with a reduced input voltage, a $R_{S1} = 750\mathrm{k}\Omega$ is chosen.

Figure 4.22 shows the converter set-up for the start-up testing. The measured waveforms are shown in Figure 4.23.

The experimental verification shows that, by adopting the second solution, the start-up of the converter is achieved.

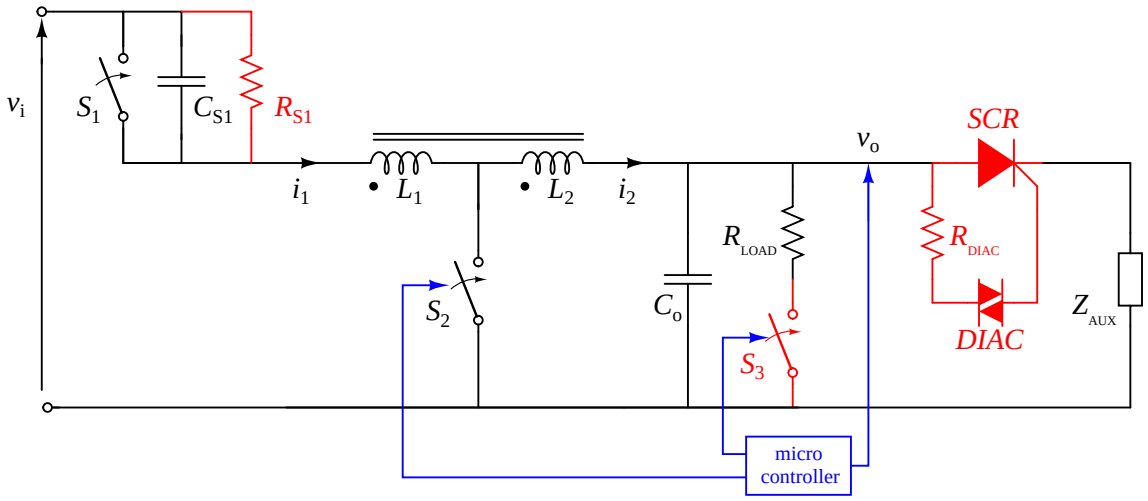

Figure 4.22: Start-up testing set-up.

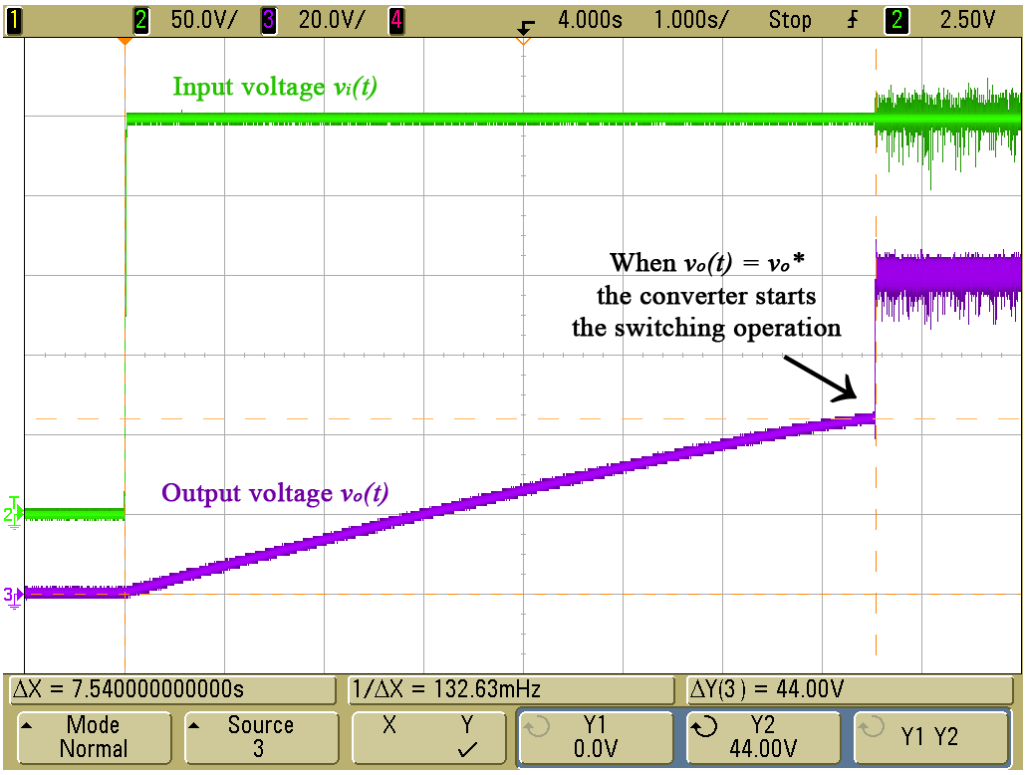

Figure 4.23: Start-up of the converter. The displayed waveforms are the input voltage (green) and the output voltage (purple). The cursors measure $v_o^* = 44$V.

Chapter 5

Conclusion

This report presents a study and an improvement of the large step-down ratio tapped-inductor buck converter, described in [13].

The average output current model allows to deepen the study of the converter, both the static and the dynamic behaviour. A small-signal model, which describes the low-frequency converter dynamics, is obtained from the average output current model.

By using pulse frequency modulation, i.e. by using the switching frequency as a control variable, a closed-loop output voltage control is designed. The closed-loop control design aims to maximize the loop gain magnitude in the greatest frequency range, i.e. the system bandwidth, by ensuring the desired phase margin.

The control is based on a micro-controller, therefore a program which implements the closed-loop control is developed.

A scaled prototype is built and tested. Experimental verification shows a low-frequency noise, which prevents the closed-loop control performances to be evaluated with precision. Nevertheless, the control system provides a well-controlled average output voltage, which is stable under significant load variation. Additional tests with a higher output capacitance shows that the approximations on which the model is based make the model dynamic response slower than reality.

A variation of the TI-buck circuit schematic, which involves a SCR-DIAC sub-circuit, is developed in order to achieve the start-up of the converter. Therefore, when energized from the high-voltage side, the studied TI-buck converter is completely autonomous.

Appendix A

Tapped-inductor

This appendix explains the behaviour of the tapped-inductor, shown in Figure A.1. Starting from the lossless and perfectly-coupled transformer, all the relations between the tapped-inductor physical quantities are derived.

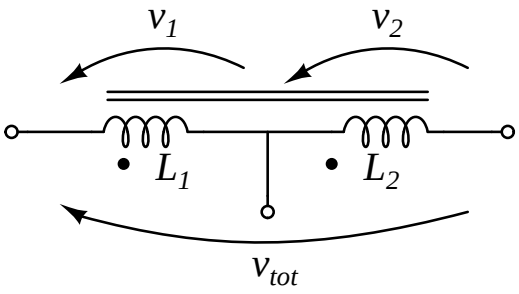

Figure A.1: Tapped-inductor.

Lossless and perfectly-coupled transformer

The analyzed transformer model, shown in Figure A.2, assumes that all flux generated by the current in the windings links all the turns of each winding. The magnetic flux can be expressed as

$$\Phi = \frac{N_1 i_1 + N_2 i_2}{\mathcal{R}} \tag{A.1}$$

where N_1 and N_2 are the number of turns in the primary and secondary windings respectively, i_1 and i_2 are the currents in the primary and secondary windings respectively and $\mathcal{R}$ is the magnetic reluctance of the magnetic core.
The magnetic flux can also be expressed as

$$\Phi = \frac{N_1 i_{1\mu}}{\mathcal{R}} = \frac{N_2 i_{2\mu}}{\mathcal{R}} \tag{A.2}$$

where

$$i_{1\mu} = i_1 + \frac{N_2}{N_1} i_2 \tag{A.3a}$$

$$i_{2\mu} = \frac{N_1}{N_2} i_1 + i_2 \tag{A.3b}$$

are the magnetizing currents referred to the primary and the secondary winding respectively. Furthermore, expression (A.2) implies

$$i_{2\mu} = N i_{1\mu} \tag{A.4}$$

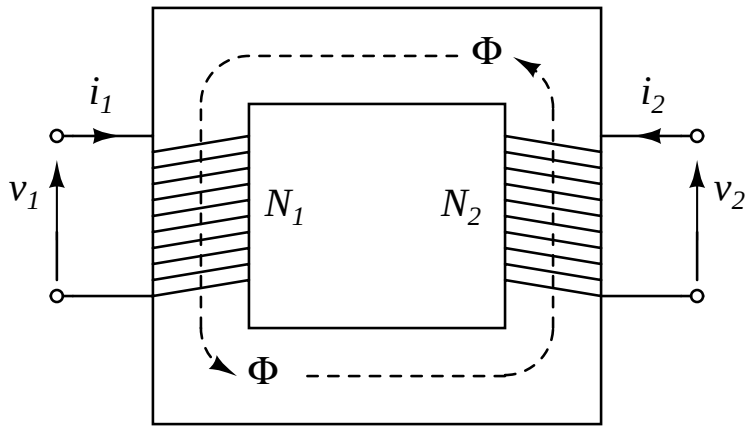

Figure A.2: Lossless and perfectly-coupled transformer.

The voltages induced across the primary and the secondary coil can be calculated from Faraday's law of induction

$$v_1 = N_1 \frac{\mathrm{d}\Phi}{\mathrm{d}t} \tag{A.5a}$$

$$v_2 = N_2 \frac{\mathrm{d}\Phi}{\mathrm{d}t} \tag{A.5b}$$

therefore

$$v_1 = N v_2 \tag{A.6}$$

where

$$N = \frac{N_1}{N_2} \tag{A.7}$$

denotes the turns ratio.

Relations (A.3a), (A.6) and (A.7) allow to model the studied transformer with the two schematics shown in Figure A.3. The first schematic consists of an ideal transformer and a primary magnetizing inductance L_1. The flux linked with current $i_{1\mu}$ in the inductance L_1, i.e. $\lambda_1 = L_1 i_{1\mu}$, must be equal to $\lambda_1 = N_1 \Phi$, in order to have induce the voltage (A.5a). Therefore, L_1 can be calculated as follow

$$\lambda_1 = L_1 i_{1\mu} = N_1 \Phi = N_1 \frac{N_1 i_{1\mu}}{\mathcal{R}} \implies L_1 = \frac{N_1^2}{\mathcal{R}} \tag{A.8}$$

The inductance L_2 in the second schematic is calculated similarly

$$\lambda_2 = L_2 i_{2\mu} = N_2 \Phi = N_2 \frac{N_2 i_{2\mu}}{\mathcal{R}} \implies L_2 = \frac{N_2^2}{\mathcal{R}} \tag{A.9}$$

Expressions (A.8) and (A.9) implies

$$L_1 = N^2 L_2 \tag{A.10}$$

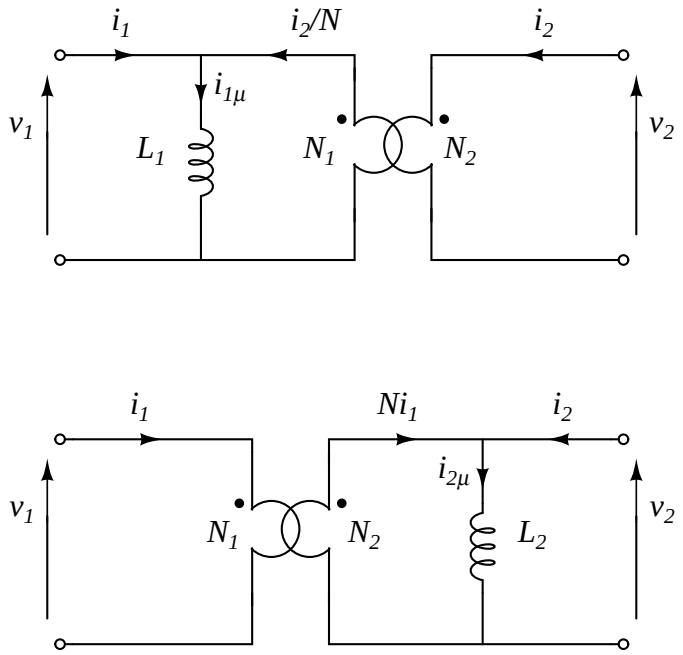

Figure A.3: Models of the lossless and perfectly-coupled transformer, with the magnetizing inductance referred to the primary and the secondary winding respectively.

Tapped-inductor properties

The tapped-inductor adopted in the studied converter can be modeled from the lossless and perfectly-coupled transformer by connecting together the negative terminal of the first port with the positive terminal of the second port. The resulting circuit schematic are shown in Figure A.4, for the first and the second transformer model respectively.
The voltage relations can be easily derived from (A.6)

$$v_{tot} = v_1 + v_2 = \frac{(1+N)}{N} v_1 \tag{A.11a}$$

$$= (1+N) v_2 \tag{A.11b}$$

Inductances L_1 and L_2, calculated when $i_2 = 0$ and $i_1 = 0$ respectively, are obviously the same as the transformer. The total inductance L_{tot} is calculated when

$$i_{tap} = 0 \implies i_1 = i_2 = i \tag{A.12}$$

By using (A.3a), (A.4) and (A.10), L_{tot} can be expressed as

$$L_{tot} = \frac{\lambda_1 + \lambda_2}{i} = \frac{L_1 i_{1\mu} + L_2 i_{2\mu}}{i} = L_1 \left(\frac{1+N}{N} \right)^2 \tag{A.13a}$$

$$= L_2 (1+N)^2 \tag{A.13b}$$

In the application of interest, the current through the tapped-inductor can be forced

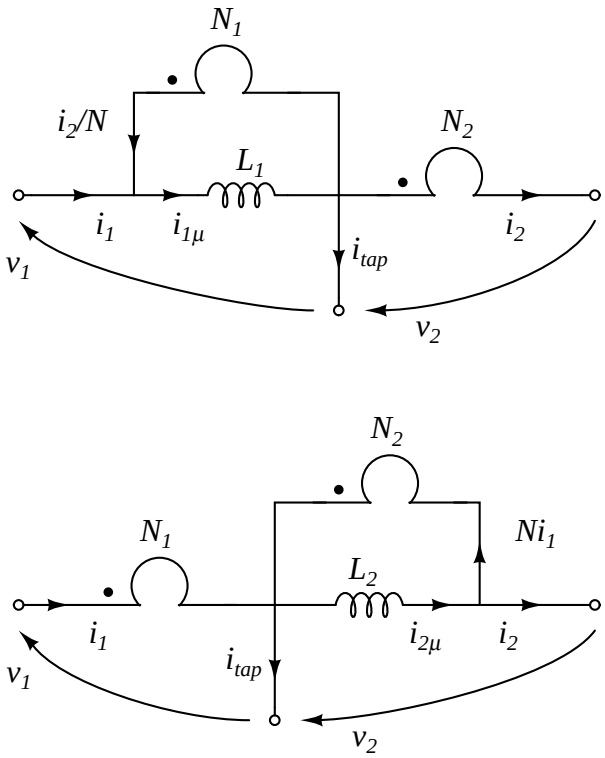

Figure A.4: Models of the tapped-inductor derived from the models of the lossless and perfectly-coupled transformer, with the magnetizing inductance referred to the primary and the secondary winding respectively.

to flow from one winding to both or vice versa, e.g. at t_1 in Figure 2.6

$$i_1(t_{1-}) = 0 \implies i_{1\mu}(t_{1-}) = \frac{1}{N} i_2(t_{1-}) \tag{A.14a}$$

$$i_{tap}(t_{1+}) = 0 \implies i_{1\mu}(t_{1+}) = \frac{1+N}{N} i_2(t_{1+}) \tag{A.14b}$$

In the magnetic core $\Phi(t)$ is continuous, therefore from (A.2) also $i_{1\mu}(t)$ is continuous

$$i_{1\mu}(t_{1+}) = i_{1\mu}(t_{1-}) \implies i_2(t_{1+}) = \frac{1}{1+N} i_2(t_{1-}) \tag{A.15}$$

which explains why the output current is discontinuous. Similar situations, e.g. at t_4 in Figure 2.6, can be studied with the same procedure.

Appendix B

Codes and models

Closed-loop control design Matlab script

```
close all
clear all

% Main specifications
v_i = 250;
v_o = 80;
p_o = 30;
L_tot = 13e-3;
N = 2;
C_o = 10e-6;
i_r = 1.5;
i_p = 5;

% Other data
t_s = 200e-6;
k_adc = 6.75;
attenuation_at_f_sw = 0.1;
PM = 80;
f_c = 10;
omg_c = 2*pi*f_c;

R_load = v_o^2/p_o;
L_1 = L_tot*(N/(N+1))^2;
L_2 = L_tot*(1/(N+1))^2;
f_sw = v_o/R_load *2/L_2/(i_p^2-i_r^2)/(1/v_o+1/(v_i-v_o));
t_uc = t_s+1/f_sw;

% TI-buck average model
k_f = L_2/2 * (i_p^2 - i_r^2) * (1/v_o + 1/(v_i-v_o));
r_o = (L_2/2 * (i_p^2 - i_r^2) * f_sw * (1/v_o^2 + 1/(v_i-v_o)^2))^(-1);
k_i_model = -L_2/2 * (i_p^2 - i_r^2) * f_sw * 1/(v_i - v_o)^2;
k_o = r_o * R_load / (r_o + R_load);
tau_o = C_o * k_o;

% Second order Butterworth low-pass filter design
Xi = sqrt(2)/2;
alpha = 20 * log10(attenuation_at_f_sw);
f_lpf = f_sw / (10^(-alpha/40));
omg_lpf = 2*pi*f_lpf;

% Iterative loop gain design
```

```
loop = 1;
T_1_old = 0;

while(loop==1)

    % Calculate k_i and k_p from PM e f_c
    k_ratio = tan(-pi+PM*pi/180-(-pi/2-atan2(2*Xi*omg_c/omg_lpf,...
        (1-(omg_c/omg_lpf)^2))-omg_c*t_uc-atan2(omg_c*tau_o,1)))/omg_c;
    k_i = 1/((k_f*k_adc*k_o/sqrt(1+(omg_c*tau_o)^2)...
        /sqrt((1-(omg_c/omg_lpf)^2)^2+(2*Xi*omg_c/omg_lpf)^2)/omg_c)...
        *sqrt(1+(k_ratio*omg_c)^2));
    k_p = k_ratio * k_i;

    % Is |T(jw)| maximized at f < f_c ?
    T_1 = abs(k_f*k_adc*k_o*exp(-i*t_uc)/(1+i*tau_o)...
        /(1+2*Xi*i/omg_lpf+(i/omg_lpf)^2)*k_i/i*(1+k_p/k_i*i));

    if(T_1 > T_1_old)

        % Update loop output
        k_i_fin = k_i;
        k_p_fin = k_p;
        f_c_fin = f_c;

        % Update f_c for next iteration
        T_1_old = T_1;
        f_c = f_c*10^0.1;
        omg_c = 2*pi*f_c;

    else

        % Exit loop
        loop = 0;
    end
end

% Discrete-time equation constants
k_p = k_p_fin
k_i_t_s= k_i_fin * t_s

a = 2*Xi/omg_lpf;
b = 1/omg_lpf^2;
k_1 = t_s^2/(t_s^2+a*t_s+b)
k_2 = (a*t_s+2*b)/(t_s^2+a*t_s+b)
k_3 = b/(t_s^2+a*t_s+b)

% Loop gain plot
s = tf('s');
T = k_f*k_adc*k_o*exp(-s*t_uc)/(1+s*tau_o)...
    /(1+2*Xi*s/omg_lpf+(s/omg_lpf)^2)*k_i_fin/s*(1+k_p_fin/k_i_fin*s);
figure(1)
margin(T);
ylim ([-360 0])
```

Micro-controller program

```
#include  <msp430g2231.h>

// define labels
#define LED0 BIT0   // S2 gate signal
#define LED1 BIT4   // Load connect or disconnect
#define LED2 BIT6   // Measure of T_sample

// LPF constants and variables
unsigned int Vo;
int Vo_lpf;
int Vo_lpf1;
int Vo_lpf2;
const float k1 =  0.1254;
const float k2 =  1.3897;
const float k3 =  0.5151;

// Ton constants and variables
const int Vo_max = 675; // 100V * k_adc
const int Vo_min = 135; // 20V * k_adc
int Vo_ton;
const long k_on = 322353; // i_r*L_2*f_clk*k_adc=1.5*1.476m*21.57M*6.75
unsigned int Ton = 1592;// initial T_on = 73.8us (hp: Vo=30V)
unsigned int S2 = 1;

// PI controller constants and variables
int V_ref = 540;// 80*K_adc
const float Kp =   3.5925;
const float KiTs = 0.2326;
int E;
int P;
int I = 270; //40V*k_adc

// Frequencies constants and variables
int fsw;
const int fsw_max = 1700;
const int fsw_min = 500;
unsigned int Tsw = 21570;// initial f_sw=1000Hz (matches with Vo=44V)
const long fclk = 21570000;

// Vref variations
int i = 0;


void main(void){

    // Stop watchdog timer
    WDTCTL = WDTPW + WDTHOLD;

    // Set output
    P1DIR |= (LED0 + LED1 + LED2);  // Set P1.0 P1.4 P1.6 as output
    P1OUT &= ~(LED0 + LED2);        // set P1.0 P1.6 to 0
    P1OUT |= LED1;                  // set P1.4 to 1

    // Set ADC (Vr=1.5V & Vss=0)
    ADC10CTL0 = SREF_1 + ADC10SHT_0 + REFON + ADC10ON + ADC10IE;
    __delay_cycles(128);// Wait ADC ref to settle
    ADC10AE0 |= BIT5;// P1.5 ADC input enable
```

```
ADC10CTL1 = INCH_5 + ADC10DIV_7;// Channel 5 input, ADC_clk/8

// Set the maximum clock frequency (21.57MHz)
BCSCTL1 |= BIT0 + BIT1 + BIT2 + BIT3;
DCOCTL |= BIT5 + BIT6 + BIT7;

// Enable interrupt
_enable_interrupt();

// Initial output voltage value
ADC10CTL0 |= ENC + ADC10SC;
__bis_SR_register(CPUOFF);
Vo_lpf = ADC10MEM;
Vo_lpf1 = ADC10MEM;
Vo_lpf2 = ADC10MEM;

// Set Timer_A
TACCR0 = 128;// Wait 6ns
TACCTL0 ^= CCIE;// Enable interrupts for CCR0.
TACTL = TASSEL_2 + MC_1 + TACLR;// SMCLK, up mode, clear timer

// Main loop
while(1){

    // Measure of T_sample
    P1OUT ^= LED2;

    // Vo measure and LPF
    ADC10CTL0 |= ENC + ADC10SC;
    __bis_SR_register(CPUOFF);
    Vo = ADC10MEM;
    Vo_lpf = k1*Vo + k2*Vo_lpf1 – k3*Vo_lpf2;
    Vo_lpf2 = Vo_lpf1;
    Vo_lpf1 = Vo_lpf;

    // Set Ton with saturation
    Vo_ton = Vo_lpf;
    if(Vo_lpf>Vo_max){
        Vo_ton = Vo_max;
    }
    else if(Vo_lpf<Vo_min){
        Vo_ton = Vo_min;
    }
    Ton = k_on/Vo_ton;

    // PI control routine
    E = V_ref–Vo_lpf;
    P = Kp*E;
    I = I + KiTs*E;
    fsw = P + I;

    // Set Tsw with saturation
    if(fsw > fsw_max){
        fsw = fsw_max;
    }
    else if(fsw < fsw_min){
        fsw = fsw_min;
    }
    Tsw = fclk/fsw;
}
```

```
}


//  Timer_A Interrupt Service Routines
#pragma vector = TIMERA0_VECTOR
__interrupt void CCR0_ISR(void) {

    // Switch the LS-SW
    P1OUT ^= LED0;

    // Load Ton in the timer
    if(S2 == 1){
        TACCR0 = Ton;
        S2 = 0;
    }

    // Load Tsw-Ton in the timer
    // 388 is a fixed delay due to the uC operation
    else{
        TACCR0 = Tsw-Ton-388;
        S2 = 1;

        //step V_ref
        //i = i+1;
        //if(i == 100){ //wait
        //  V_ref = 472;// 70*k_adc
        //}
    }

    // Return to active mode
    __bic_SR_register_on_exit(CPUOFF);
}


// ADC10 interrupt service routine
#pragma vector=ADC10_VECTOR
__interrupt void ADC10_ISR (void)
{
    // Return to active mode
    __bic_SR_register_on_exit(CPUOFF);
}
```

PLECS simulation models

This Section shows the *PLECS* closed-loop TI-buck model used for the simulations. Subsystems are used for the sub-circuits, in order to simplify the analysis of the converter.

The main schematic includes:

- the TI-buck converter;
- the micro-controller;
- scopes for the visualization of static and dynamic waveforms;
- tools for simulating the open-loop transfer function $V_o(s)/F_{sw}(s)$;
- a load switch, for simulating the effects of load variation.

The model does not implement the start-up procedure of the converter, therefore the output capacitance initial voltage is set to $v_o/2$.

The subsystem "HS-SW control" implements the HS-SW behaviour, i.e. ZVS turn-on and peak-current turn-off.

The subsystem "Micro Controller" implements the μC operation, i.e. the digital low-pass filter, the PI controller and a pulse generator, which provides the LS-SW with a proper gate signal.

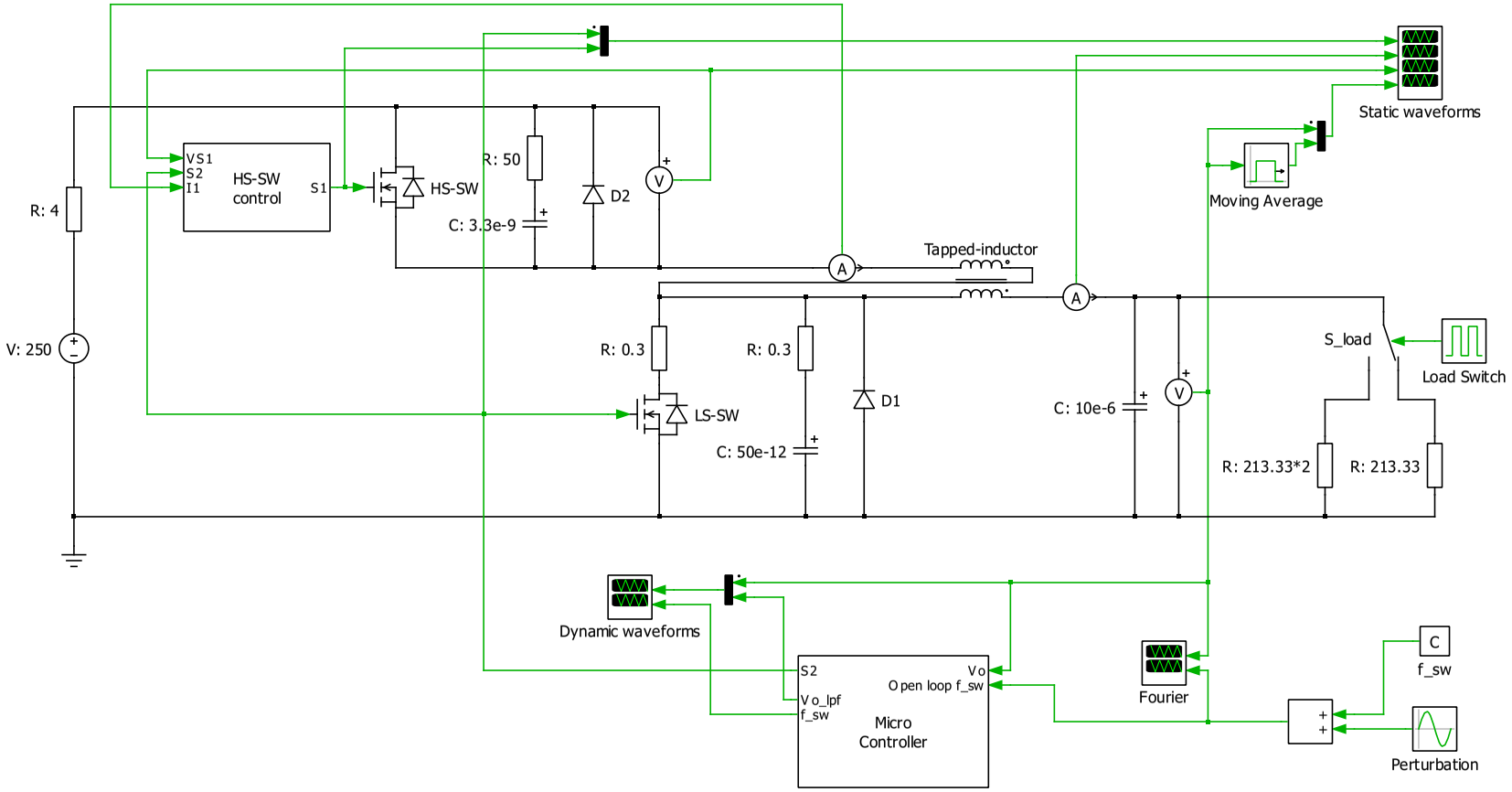

Figure B.1: TI-buck converter. This circuit implements the closed-loop TI-buck converter.

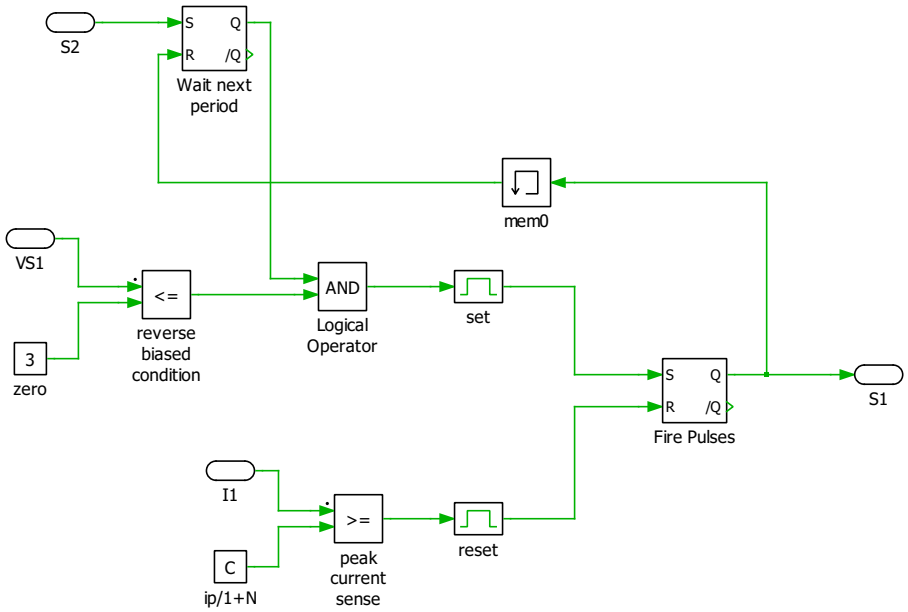

Figure B.2: HS-SW gate signal generator. This circuit implements the HS-SW behaviour, i.e. ZVS turn-on and peak-current turn-off.

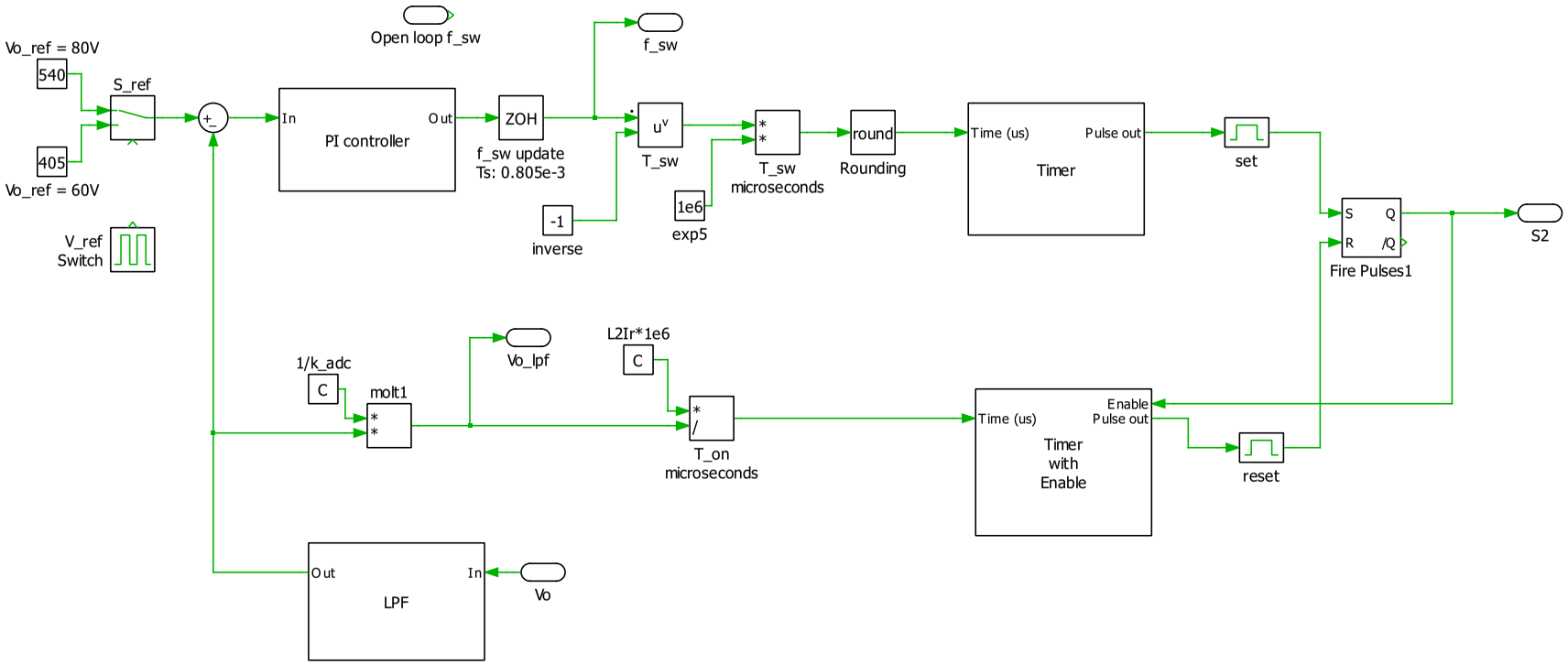

Figure B.3: Micro-controller. This circuit implements the μC operation, i.e. the digital low-pass filter, the PI controller and a pulse generator, which provides the LS-SW with a proper gate signal.

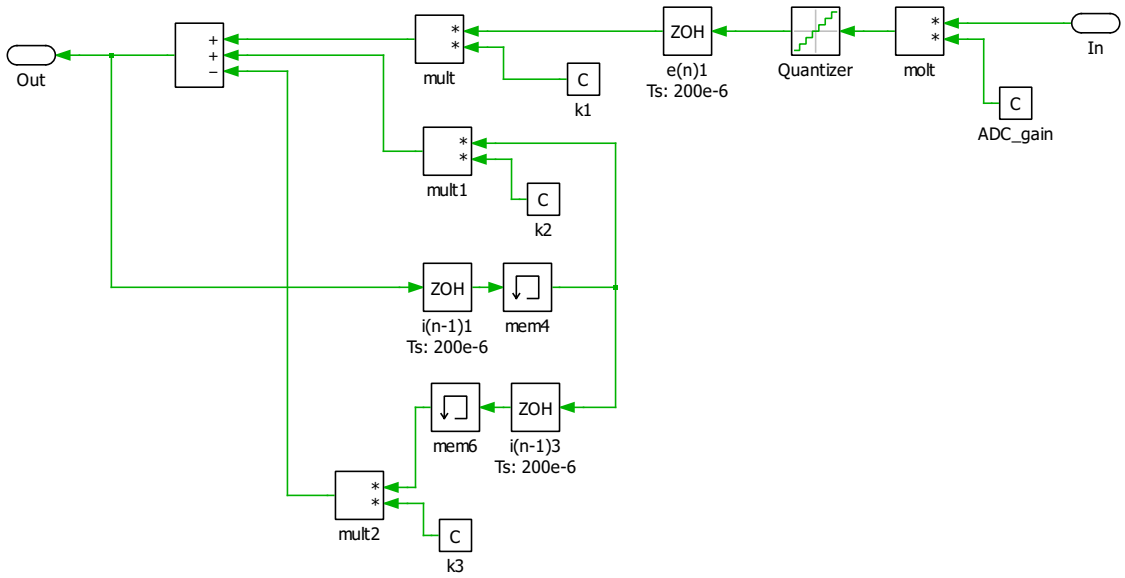

Figure B.4: Second order digital low-pass filter. This circuit implements the second order low-pass filter discrete-time equations.

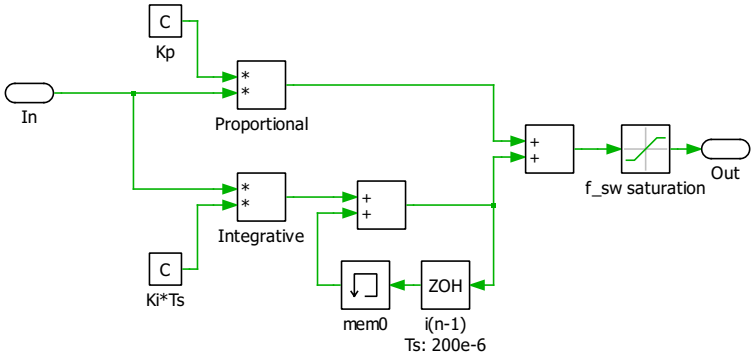

Figure B.5: PI controller. This circuit implements the PI controller discrete-time equations. A saturation is added before the output, in order to avoid extreme values of f_{sw}.

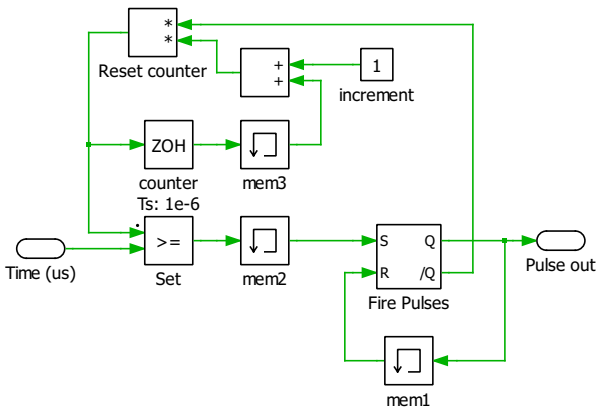

Figure B.6: Timer. This circuit provides a positive pulse every T[us], which denotes the input of the subsystem, specified in μs.

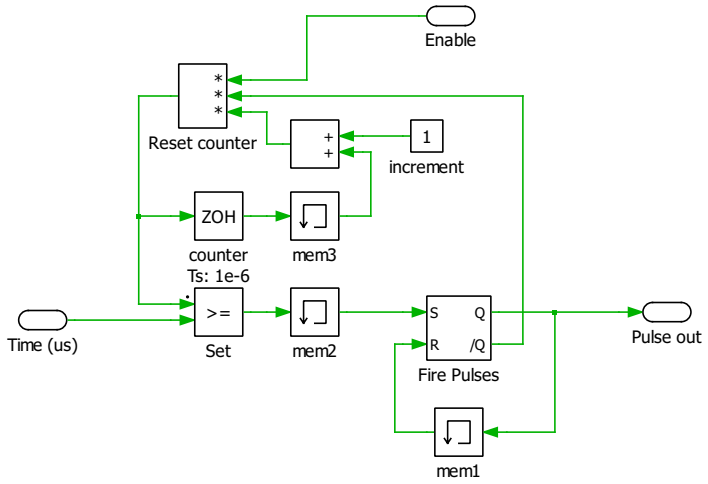

Figure B.7: Timer with enable. If enabled, this circuit provides a positive pulse every T[us], which denotes the input of the subsystem, specified in μs.

Appendix C

Complete schematics

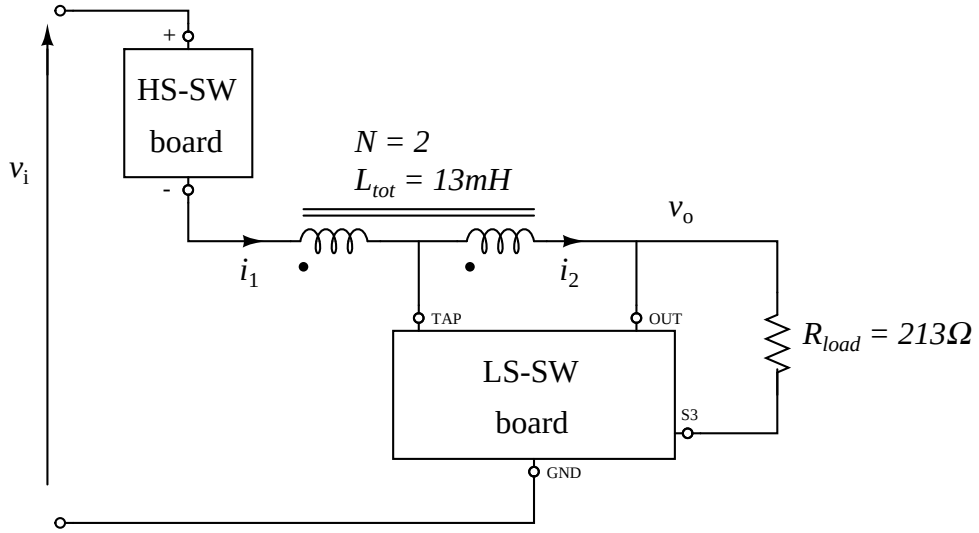

Figure C.1: Tapped-inductor buck converter.

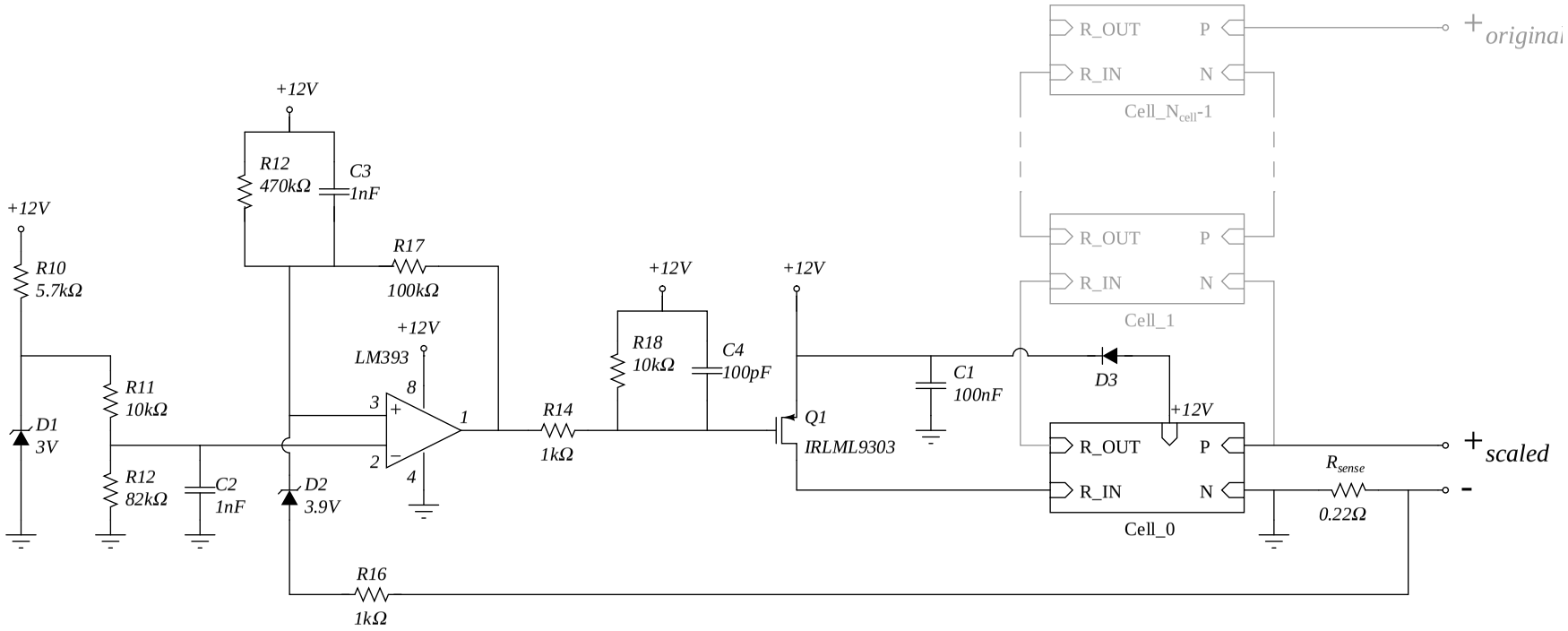

Figure C.2: High-side switch PCB schematic. The ground symbol indicates the local ground of the HS-SW PCB.

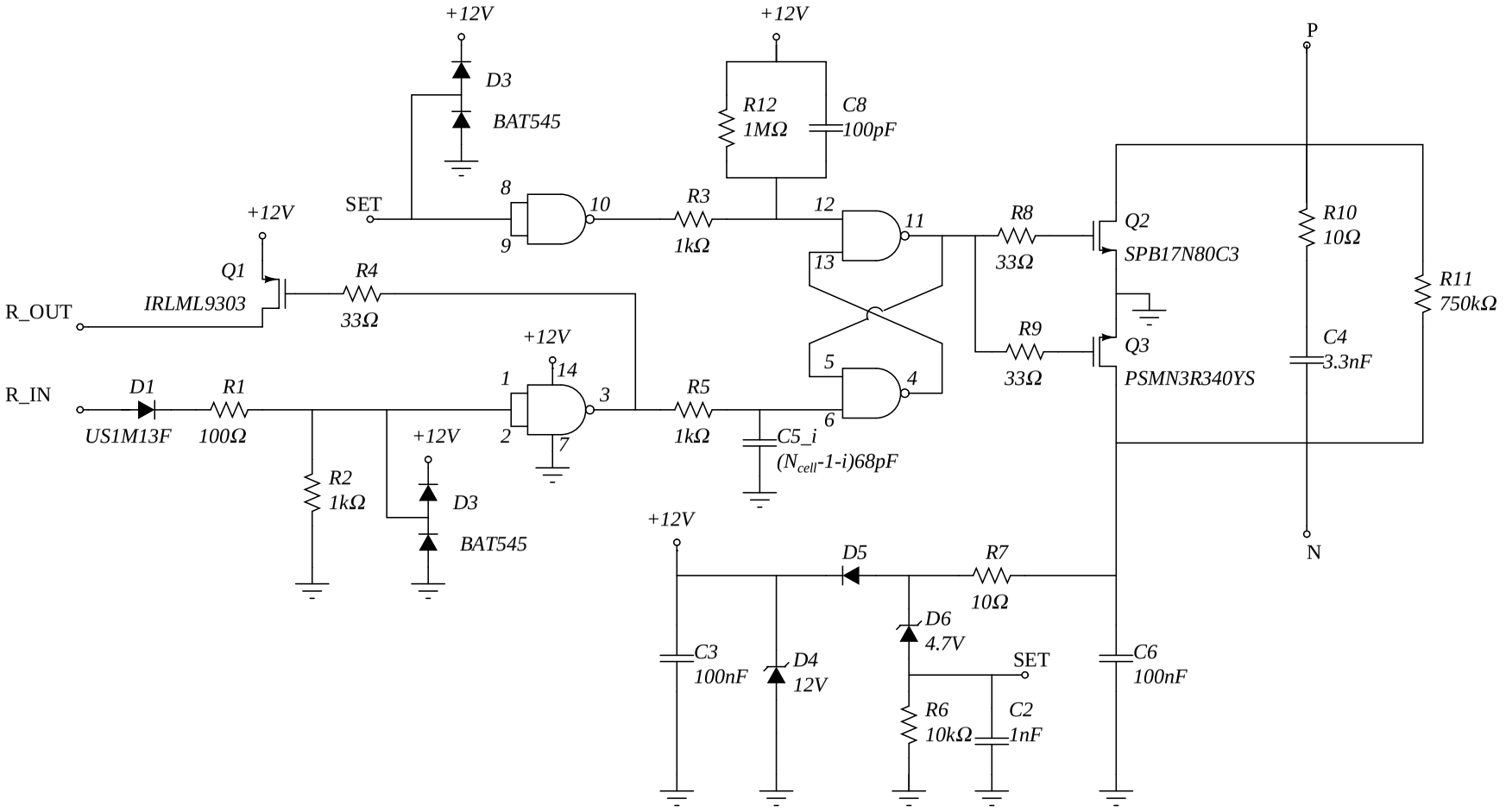

Figure C.3: HS-SW switching cell PCB schematic. The ground symbol indicates the local ground of the switching cell.

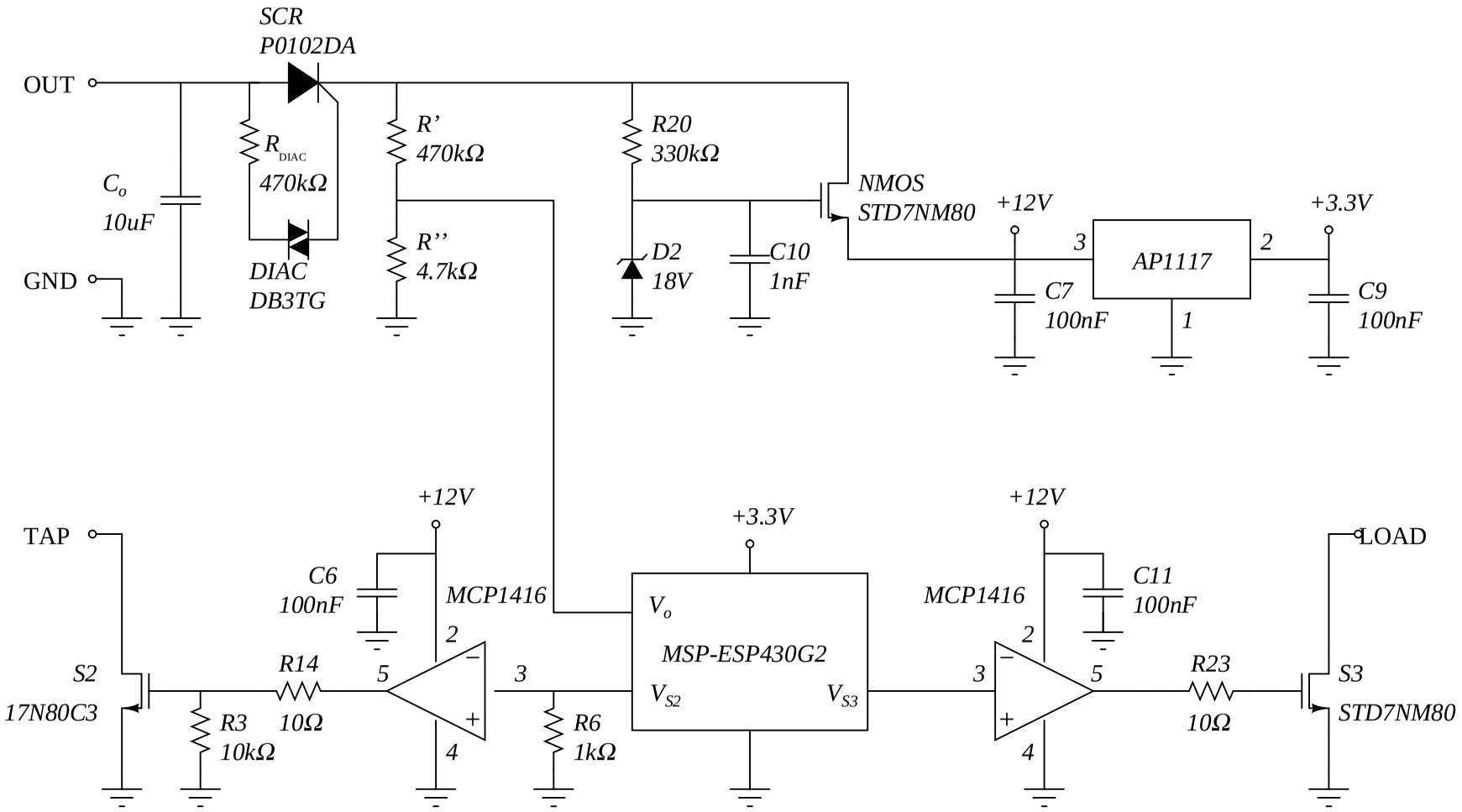

Figure C.4: Low-side switch PCB schematic.

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