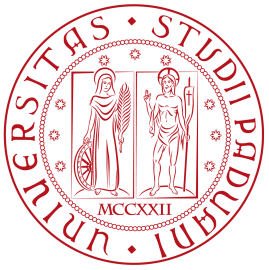

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STUDY OF LOW-NOISE DESIGN TECHNIQUES FOR LDO VOLTAGE REGULATORS

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Abstract

This work provides a wide knowledge of the electronic noise, its physical modeling, its behavior in time-domain and frequency-domain and its simulation. Then the thesis focuses on the feasibility study and an example of design of a low-noise LDO voltage regulator. To reach low-noise performance the main noise sources are analyzed (Error Amplifier, Voltage Reference and the Voltage Feedback Network) and then a deepen study of the regulation loop is made because its performance are crucial for noise. This work illustrates an example of design to reach low-noise performance, many other design choices and specific topologies could be taken into account, however, this work proposes to explore the minimum noise-limits of the classical configuration of a voltage regulator (voltage reference+error amplifier+resistive feedback network) and to give some useful concepts of electronic low-noise design.

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Chapter 1

Electronic Noise

The *Electronic Noise* is a small voltage or current fluctuation generated by the circuit itself, may be amplified or reduced but not completely eliminated. The main causes of electronic noise are the thermal agitation of carriers and the charge quantization, but there are many other physical phenomena and many others have yet to be discovered. The amplitude and phase of noise are a random process and therefore we can not predict their behavior in time, but using statistical methods it is possible to obtain a spectral model of noise.

The noise is an important subject to study because it sets the lowest signal level that can be elaborated with acceptable quality, nowadays this is one of the most important problems that affects circuits for the signal elaboration, above all those portables, because the scaling of voltages and currents decreases the $SNR = \frac{P_{signal}}{P_{noise}}$ (*Signal to Noise Ratio*) of the signal. For this reason we should supply these devices with a "as clean as possible" source (i.e. "less noisy as possible") and then we need a voltage (or current) regulator with a good noise performance.

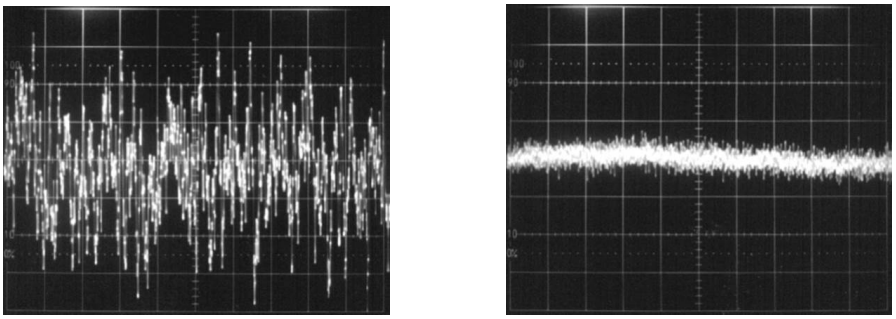

Fig. 1.1: Examples of noisy voltages

1.1 Statistical Characterization of noise

Noise is a random process, so its complete behavior is very difficult to know, but to make simple predictions we just need to know few statistical quantities like the *mean value* and *variance* to model noise in the time domain and *power spectral density* (PSD) to model noise in the frequency domain.

An important property of noise is the *stationarity* and *ergodicity* (this is not a general characteristic of all types of noise but for this discussion will be taken as a property).

Stationarity means that observing little and separated portions of the noisy signal, we find *the same* characteristics (i.e. mean and variance) in every portion.

Ergodicity means that, taken a set of identical systems (ensemble) and fixed a temporal reference, the statistical averages of the ensemble converge ($\doteq$) to the temporal averages (Formulas (1.1) and (1.2)).

$$\overline{v_n(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} v_n(t)dt \doteq E[v_n(t)] =< v_n(t) > \tag{1.1}$$

$$\overline{v_n^2(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} v_n^2(t)dt \doteq E[v_n^2(t)] = \sigma_{v_n}^2 \tag{1.2}$$

We can help ourselves to understand this concept looking the Figure 1.2, henceforth we don't use the concept of ensemble because the noise of one device (element of ensemble) is sufficient to show the entirely noise performance, and so we concentrate only on the temporal averages.

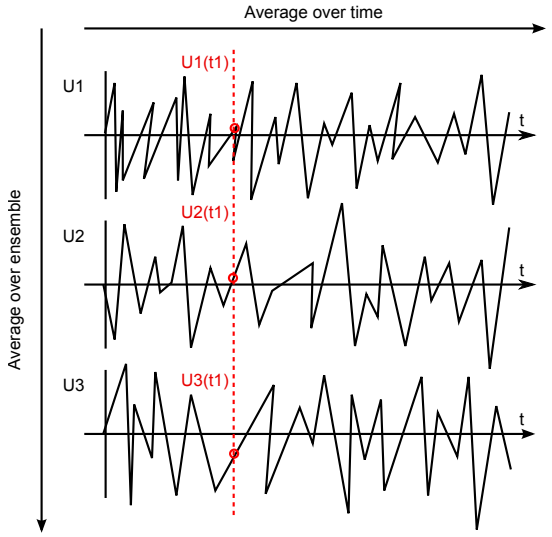

Fig. 1.2: Ensemble and temporal average

The *noise mean* is *zero*, we can convince ourselves looking the Figure 1.1, so referring to Eq. (1.1):

$$< v_n(t) >= 0$$

As regard the *variance* we have to make a brief introduction, in the signal theory it is defined the *autocorrelation* of a signal *x(t)* as in Eq. (1.3):

$$r_{xx}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} x(t)^* x(t+\tau)dt \tag{1.3}$$

The *Available Power* (it is the *statistical power*) of the signal is the autocorrelation in the origin $r_{xx}(0)$ (signals are overlapped), and considering that $x(t)^*x(t) = |x(t)|^2$:

$$P_{av} = r_{xx}(0) = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} |x(t)|^2 dt \geq 0 \tag{1.4}$$

Thus the comparison between Eq. (1.4) and Eq. (1.2) becomes easy because a signal in the real world is a real-valued signal and so (thinking to a voltage signal $v_n(t)$):

$$|v_n(t)|^2 = v_n(t)^2$$

thus:

$$P_{av} = \sigma_{v_n}^2 \tag{1.5}$$

or even the root mean square value:

$$v_{n,RMS} = \sqrt{\sigma_{v_n}^2} = \sigma_{v_n} \tag{1.6}$$

Note that the available power P_{av} of a noise signal is ever greater than zero, just think that the power is proportional to the area of the ${v_n}^2$ as in the Figure 1.3 (an area is a positive value).

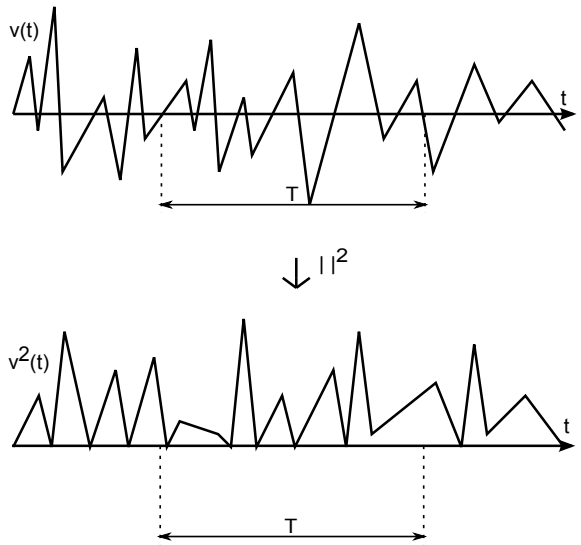

Fig. 1.3: Voltage squared noise

Now we start to think what happens in the frequency domain: a *deterministic signal* like a sine wave or a square wave has its power concentrated only at certain frequencies (i.e. lines) so the spectrum looks like a *lines spectrum*. The total power is simply the arithmetic sum of the power of the single harmonics. A *non-deterministic signal* like noise, has an infinite number of harmonics, that is a *continuous spectrum*. The power is thus distributed at all frequencies and so is called a *Power Spectral Density* (Figure 1.4).

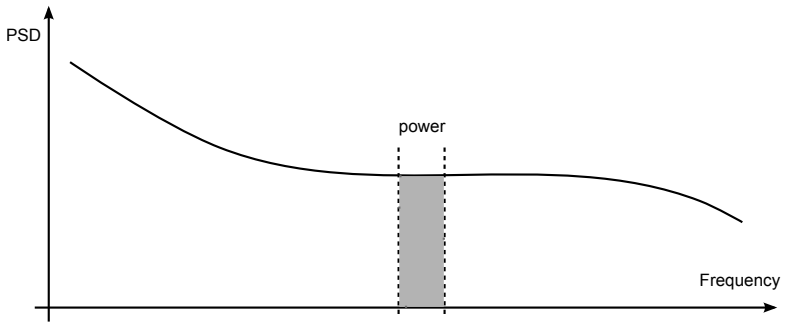

Fig. 1.4: Power Spectral Density

$$P_{tot} = \int_{-\infty}^{+\infty} PSD(f)df \tag{1.7}$$

where the $PSD(f)$ has the physical dimension of $\left[\frac{V^2}{Hz}\right]$ thinking to a voltage signal or $\left[\frac{A^2}{Hz}\right]$ thinking to a current one.

Are we sure that $P_{tot} = P_{av}$?

The demonstration is simple because *Wiener-Khinchin theorem* shows that, in particular conditions that we can consider satisfied with random processes of electronic noise:

$$r_{xx}(\tau) = \int_{-\infty}^{+\infty} S(f) e^{j2\pi\tau f} df \tag{1.8}$$

we know that:

$$P_{av} = r_{xx}(0) = \int_{-\infty}^{+\infty} S(f) df \tag{1.9}$$

and so comparing Eq. (1.9) with Eq. (1.7) we can conclude that $P_{av} = P_{tot} = \sigma_{v_n}^2$ and $S(f)$ is just the $PSD(f)$.

We can also observe that inverting Eq. (1.8):

$$S(f) = \int_{-\infty}^{+\infty} r_{xx}(\tau) e^{-j2\pi\tau f} d\tau \tag{1.10}$$

we find that

$$S(f) = PSD(f) = F[r_{xx}(\tau)] \tag{1.11}$$

where $F[\cdot]$ means the *Fourier Transform.*

Summarizing, the $PSD(f)$ represents the power (statistical) of the noise signal in the frequency domain so it is the best physical quantity to study the noise performance of an electronic device because knowing the bandwidth of the system (B) we can easily find the total power of noise that affects the circuit using Eq. (1.12) (with a good approximation because the real bandwidth is $0 < f < +\infty$).

$$P_{noise} = \int_{-B}^{+B} PSD(f) df \tag{1.12}$$

Note that Eq. (1.7) and Eq. (1.12) use the *bilateral spectrum* $-\infty < f < +\infty$, fortunately we work with real-valued signals so thanks to the *Hermitian symmetry* $H(f) = H(-f)^*$, the module of $PSD(f)$ over the negative band $-B$ is the same as over the positive band $+B$, therefore Eq. (1.12) simplifies in:

$$P_{noise} = \int_{0}^{+B} 2 \times PSD(f) df = \int_{0}^{+B} PSD(f)' df \tag{1.13}$$

However the factor 2 in Eq. (1.13) is only a scale factor, so for the rest of this work and for practical simplicity we will use Eq. (1.14):

$$P_{noise} = \int_{0}^{+B} PSD(f) df \tag{1.14}$$

1.2 Types of Noise

Electronic devices are affected by *external* noise (or *environmental* noise) and *internal* noise (or *semiconductor* noise), we will focus on the latter one in this work.

Semiconductor noise is self-generated by the device itself, there are many known physical sources of this noise. *Thermal*, *Shot* and *Flicker* are the main noise sources, but there are also many unknown physical sources.

1.2.1 Thermal Noise

Thermal Noise is always associated with a passive physical resistance, it is due to the random thermal motion of electrons (random "walk") that cause random fluctuations in the voltage measured across the conductor, this does not require a DC current flux so even a disconnected resistor shows thermal noise. The carrier agitation (electrons and holes) is favored by the temperature and thus thermal noise is directly proportional to the absolute temperature T (in Kelvin).

In a resistor R, thermal noise can be represented alternatively by a Thevenin or a Norton representation as shown in in Figure 1.5

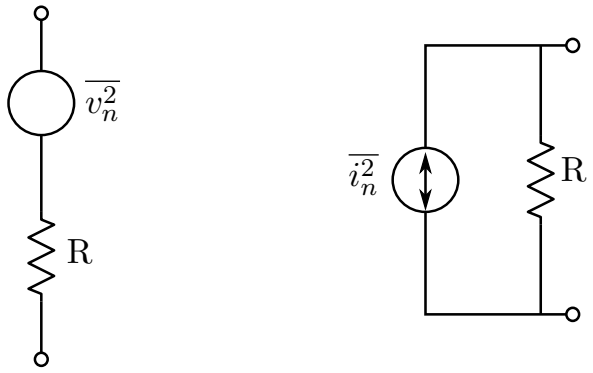

Fig. 1.5: Equivalent circuits of resistor thermal noise, R is a noiseless resistor

The expressions of *powers* are (k is the Boltzmann constant):

$$\overline{v_n^2} = 4kTR\Delta f \tag{1.15}$$

$$\overline{i_n^2} = \frac{4kT}{R}\Delta f \tag{1.16}$$

and PSD:

$$S_v(f) = \frac{\overline{v_n^2}}{\Delta f} = 4kTR \tag{1.17}$$

$$S_i(f) = \frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R} \tag{1.18}$$

As we can see from Eq. (1.17) and Eq. (1.18), the PSD (either voltage or current) is *white*, so its spectrum is *independent* of frequency (Figure 1.6), indeed this is true at least until about 10^{13}Hz. The terminology *white* derives from the analogy with the solar spectrum, if we "see" a radiation with a similar spectrum in the visible band we feel the color white.

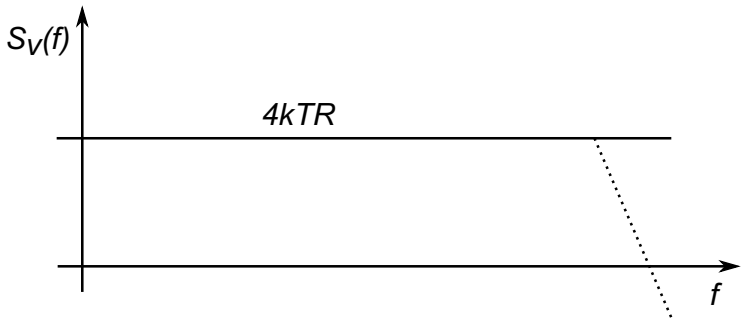

Fig. 1.6: Voltage power spectral density

In general if we have an impedance $Z(j\omega)$ measured at a generic port of a linear and passive network, only the resistive passive part (real part, so $\Re[Z(j\omega)]$) generates noise, and the equivalent circuit is represented as in Figure 1.5 with the noiseless resistance and PSD:

$$\frac{\overline{v_n^2}}{\Delta f} = 4kT\Re[Z(f)] \tag{1.19}$$

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{\Re[Z(f)]} \tag{1.20}$$

the imaginary part $\Im[Z(j\omega)]$ represents the reactance and doesn't generates thermal noise.

1.2.2 Shot Noise

Shot Noise is *always* associated with a DC current flux through a potential barrier of a junction, so it is present most in diodes and BJT and is minor in MOS transistor. It is due to the uncertainty on the number of carriers passing the potential barrier, since the passage of the barrier is a random event because of only those carriers having enough energy are able to pass the barrier. This is translated in fluctuations (i.e. *shot noise*) of the current from the mean value, best expressed in terms of mean-square variation:

$$\overline{i_n^2} = \overline{\big(i(t) - I_{DC}\big)^2} = \lim_{T\to\infty} \frac{1}{T}\int_0^T \big(i(t) - I_{DC}\big)^2 dt$$

The spectrum of a signal compound by the series of random independent pulses (i.e. *shots*) can be shown to be constant in frequency (i.e. *white*), and the PSD of shot noise is:

$$\frac{\overline{i_n^2}}{\Delta f} = 2qI_{DC} \tag{1.21}$$

q is the elementary charge. Equation (1.21) is valid until the frequency not approaching $1/\tau$, where τ is the transit time of carriers to cross the depletion region of the potential barrier. With recent technologies $1/\tau$ is at least in the GigaHertz bandwidth, therefore at all effects we will consider shot noise as a white noise.

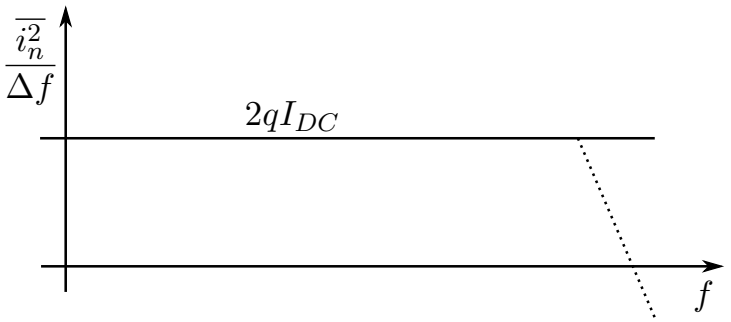

Fig. 1.7: PSD of shot noise

1.2.3 Flicker Noise

Flicker Noise is a quite strange type of noise, its physical causes are nowadays not fully understood, it affects all active devices and also carbon resistors. The transistor MOS shows an important contribute of flicker noise because the drain current flows near the interface substrate-SiO_2. This interface is full of dangling bonds (Figure 1.8), due to the material discontinuity, that act as traps for carriers and this leads to fluctuations in the current (i.e. noise).

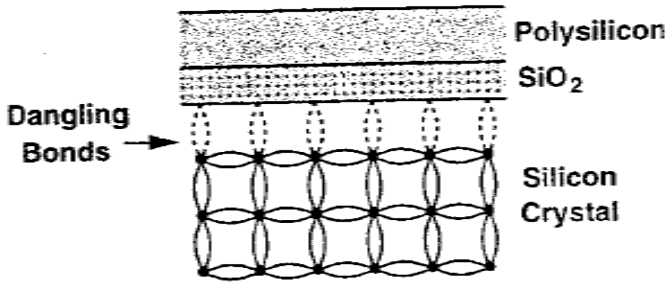

Fig. 1.8: Defects at the interface in the Metal Oxide Semiconductor structure

In general, however, Flicker noise can be produced by discontinuities that the current meets for the imperfections of the material.

Flicker noise has a spectral density:

$$\frac{\overline{i_n^2}}{\Delta f} = K_f \frac{I^a}{f^b} \tag{1.22}$$

where $\mathbf{K}_f$ is a particular process constant, **I** is the direct current, **a** is a constant in the range 0.5 to 2, **b** is a constant of about a unity and, of course, **f** is the frequency.

We note that Flicker noise exists only if there is a DC current flux, and in the case b=1 it takes the form of $1/f$ noise as in Figure 1.9 (flicker noise is also called *1/f noise* or *pink noise*). The unknown constant K_f can vary orders of magnitude from different types of transistors and also can vary randomly from transistors of the same wafer, so this parameter is a fitting parameter determined from measurements on a number of devices from a given process.

Electronic devices are affected by lots of noise sources, many of them are still in the study phase, like *Burst* or *Avalanche* noise for example, in this work we take into account only *thermal*, *shot* and *flicker* noise because they are the main noise sources in transistors (bipolar and MOS) and resistors.

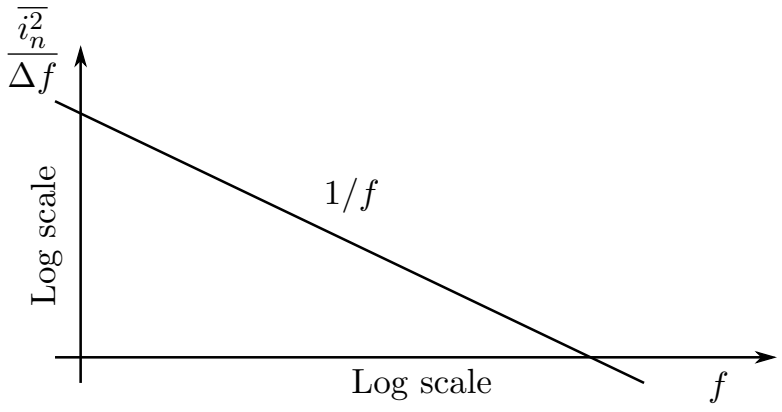

Fig. 1.9: PSD of Flicker noise

1.3 Noise Models in IC Devices

The three noisy devices taken into account in this work are resistors, bipolar transistors and MOS, the fourth element very used in integrated circuits (IC) is the capacitor, but an ideal reactive component doesn't show noise.

Resistors Noise is already been explained and the equivalent model is shown in Figure 1.5, its PSDs are Eq. (1.17) and Eq. (1.18).

1.3.1 MOS Transistor

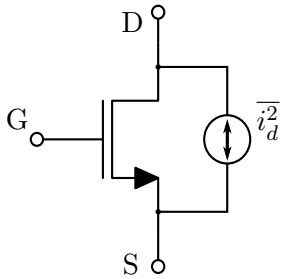

Fig. 1.10: MOS Noise model

The MOS transistor has two main noise sources, thermal and flicker, both of them influences the drain current, at the input port (gate-source) there isn't a DC current so (in the approximation of no leakage) is a noiseless port. The MOS noise model is shown in Figure 1.10 and the noise PSD is:

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{\overline{i_{th}^2}}{\Delta f} + \frac{\overline{i_{1/f}^2}}{\Delta f} \tag{1.23}$$

Thermal Noise exists because of the drain-source channel is a *resistive* channel:

$$\frac{\overline{i_{th}^2}}{\Delta f} = 4kT\gamma gm \tag{1.24}$$

The constant γ is 2/3 for long-channel MOS (for L greater than few μm) and is about 2-2.5 for short-channel devices, gm is the transconductance.

Flicker Noise is explained in Page 7 and is modeled as:

$$\frac{\overline{i_{1/f}^2}}{\Delta f} = \frac{K_f I_d}{L^2 C_{ox}} \frac{1}{f} \propto \frac{1}{f} \tag{1.25}$$

The noise power is:

$$\overline{i_{1/f}^2} = \int_{f_1}^{f_2} \frac{K_f I_d}{L^2 C_{ox}} \frac{1}{f} df = \frac{K_f I_d}{L^2 C_{ox}} ln \frac{f_2}{f_1} \tag{1.26}$$

It's interesting to note that *every frequency decade has the same Power* because the ratio $ln\frac{f_2}{f_1}$ is constant.

Looking the Eq. (1.26) a question arises: **what happens if f_1 tends to zero?** (Appendix A.1)

Another important parameter for MOS Noise performance (and for a certain technology) is the *Corner frequency* that it determines the minimum frequency where the Flicker noise is smaller (and then can be confused) than Thermal noise (Figure 1.11).

o

Fig. 1.11: corner frequency

We can calculate corner frequency equating Eq. (1.24) with Eq. (1.25):

$$f_{co} = \frac{K_f}{4kT\gamma L^2 C_{ox}} \frac{1}{gm/I_d} \tag{1.27}$$

The parameter $\frac{1}{gm/I_d}$ is relatively constant for a fixed technology, so the corner frequency is relatively constant at a certain L, in fact the best design parameter to vary Flicker Noise is $f_{co} \propto \frac{1}{L^2}$, the corner frequency can be at hundreds of kHz for submicron transistors.

To vary the noise in a MOS transistor we can change either the physical dimensions (W and L) and the bias drain current I_D.

1.3.2 Bipolar Transistor

Bipolar transistor shows *shot* noise in the collector and base current:

$$\frac{\overline{i_c^2}}{\Delta f} = 2qI_C \tag{1.28}$$

$$\frac{\overline{i_b^2}}{\Delta f} = 2qI_B \tag{1.29}$$

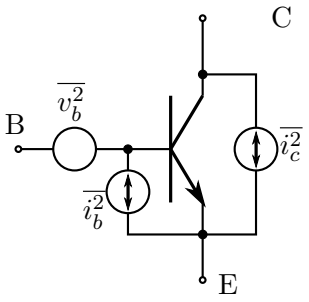

Fig. 1.12: BJT Noise model

and *thermal* noise due to the base resistance R_b (this is a physical resistance):

$$\frac{\overline{v_b^2}}{\Delta f} = 4kTR_b \tag{1.30}$$

There are also resistances at collector and emitter that generates thermal noise but, in practice, their contribute is negligible, instead the noise of base resistance is then amplified by the device and is not so small at the output (collector or emitter).

Indeed, Flicker Noise is observed also in BJT and is modeled as a current noise source at the base:

$$\frac{\overline{i_{b,1/f}^2}}{\Delta f} = K_f I_B^{\alpha} \frac{1}{f} \tag{1.31}$$

It is possible to define the *corner frequency* also for the base current noise, anyway, for bipolar transistors using careful processing, f_{co} can be as low as 100Hz, so the flicker noise contribute can be negligible.

To vary the noise in a BJT we can only change the bias current I_B and consequently $I_C = \beta I_B$.

1.4 Circuit Noise Calculations

We introduce the argument with a simple example: the series of two resistors as shown in Figure 1.13.

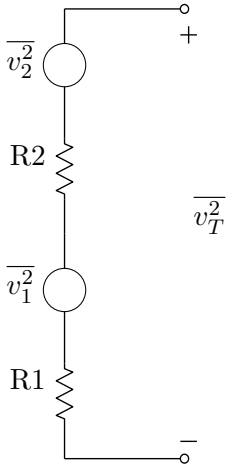

Fig. 1.13: Noise produced by two resistors in series

Resistors R_1 and R_2 have respective noise generators (assuming a 1Hz bandwidth):

$$\overline{v_1^2} = 4kTR_1$$
$$\overline{v_2^2} = 4kTR_2$$

Considering the time domain, the total noise voltage is:

$$v_T(t) = v_1(t) + v_2(t)$$

and thus:

$$\overline{v_T(t)^2} = \overline{v_1(t)^2 + v_2(t)^2} = \overline{v_1(t)^2} + \overline{v_2(t)^2} + \overline{2v_1(t)^2 v_2(t)^2} \tag{1.32}$$

Since $v_1(t)$ and $v_2(t)$ arise from different resistors, they can be considered *independents* and so $\overline{2v_1(t)^2 v_2(t)^2} = 0$, therefore Eq. (1.32) becomes:

$$\overline{v_T(t)^2} = \overline{v_1(t)^2} + \overline{v_2(t)^2} \tag{1.33}$$

In the frequency domain:

$$\overline{v_T^2} = \overline{v_1^2} + \overline{v_2^2} = 4kT(R_1 + R_2) \tag{1.34}$$

it's as there is an only resistance $R_1 + R_2$ that produces the noise.

This is a simple example but, seeing Eq. (1.34), it seems that the two PSD are simply added, this is true for all noise sources if we use the Noise models described in Sec. 1.3 because the noise sources derives from different physical processes and thus are independents.

To calculate the Noise in an arbitrary circuit we proceed in this way:

1. We have to use the *AC-circuit* because the noise is assumed to be a *small signal*, so we have to short all independent voltage generators and to open all independent current generators.

2. For every Noise Source ($v_{n,x}$ or $i_{n,x}$), we have to calculate the transfer function (TF) to the output ($v_{n,o}$ or $i_{n,o}$):
$$H_x(s) = \frac{s_{n,o}}{s_{n,x}}$$

3. Under the hypothesis of *independents sources* we can calculate the total PSD:
$$\frac{\overline{s_{n,o}^2}}{\Delta f} = \sum_x |H_x(j2\pi f)|^2 \frac{\overline{s_{n,x}^2}}{\Delta f}$$

4. Let's calculate the noise power at the output:
$$\overline{s_{n,o}^2} = \int_{f_1}^{f_2} \frac{\overline{s_{n,o}^2}}{\Delta f} df$$

Important: since the Noise has a *random phase* (why? see Appendix A.2), the only quantity of interest is the **module** of the noise, so even for the transfer function we are interested only at its **module** $|H_x(j2\pi f)|^2$, henceforth in this work we will use the more common annotation $H_x(j2\pi f)^2$, but *we must remember that we are referring at the module.*

Now we know how to calculate the output PSD or power, in some circuits we are interested exactly at the output noise, but in others, like *systems closed in feedback*, this is not the best way to treat the noise. A better choice is to think noise concentrated at the input as in in Figure 1.14.

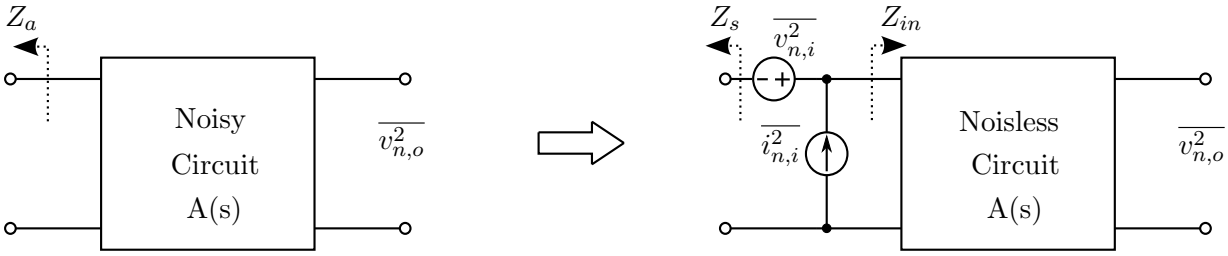

Fig. 1.14: Input-referred noise

In general the input-referred noise model expected a voltage noise generator $\overline{v_{n,i}^2}$ and a current noise generator $\overline{i_{n,i}^2}$ (a 1Hz bandwidth is assumed), if the noiseless circuit has a transfer function $A(s)^2 = \dfrac{\overline{v_{n,o}(s)^2}}{\overline{v_{n,in}(s)^2}}$ with $\overline{v_{n,in}(s)^2}$ is the voltage at the Z_{in} port:

$$\overline{v_{n,o}(s)^2} = \left(\frac{Z_{in}(s)}{Z_{in}(s)+Z_s(s)}\right)^2 A(s)^2\overline{v_{n,i}(s)^2} + \left(Z_{in}(s)//Z_s(s)\right)^2 A(s)^2\overline{i_{n,i}(s)^2} \qquad (1.35)$$

To calculate $\overline{v_{n,i}(s)^2}$ and $\overline{i_{n,i}(s)^2}$ is simple:

- we *short* the input port $Z_a = 0$ in the Noisy circuit and $Z_s = 0$ in the Noiseless one in Figure 1.14 and then we equate the $\overline{v_{n,o}(s)^2}$, in agreement with Eq. (1.35) ($Z_s = 0$) we find
$$\overline{v_{n,i}(s)^2} = \frac{\overline{v_{n,o}(s)^2}}{A(s)^2}$$
- we *open* the input port $Z_a = \infty$ in the Noisy circuit and $Z_s = \infty$ in the Noiseless one in Figure 1.14 and then we equate the $\overline{v_{n,o}(s)^2}$, in agreement with Eq. (1.35) ($Z_s = \infty$) we find
$$\overline{i_{n,i}(s)^2} = \frac{\overline{v_{n,o}(s)^2}}{Z_{in}^2 A(s)^2}$$

Now we have all the elements to analyze the noise performance of a circuit. For completeness we study a very important (and surprising) example.

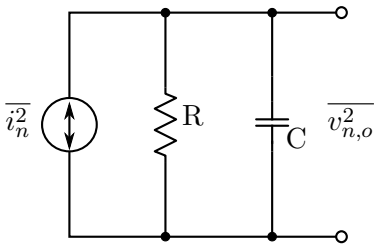

Fig. 1.15: RC cell

In a simple RC cell, Figure 1.15, that it can be either a *Low-pass* or a *High-pass* filter, noise is produced by the resistance:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R}$$

and the capacitor shapes the PSD (*spot noise*) because acts on the transfer function:

$$\frac{v_{n,o}}{i_n} = \frac{R}{1+sRC}$$

and thus:

$$\frac{\overline{v_{n,o}^2}}{\Delta f} = \left|\frac{R}{1+j2\pi fRC}\right|^2 \frac{\overline{i_n^2}}{\Delta f} \tag{1.36}$$

The capacitor makes a pole at the frequency $f_0 = \frac{1}{2\pi RC}$. The PSD is plotted in Figure 1.16 by varying the resistance R.

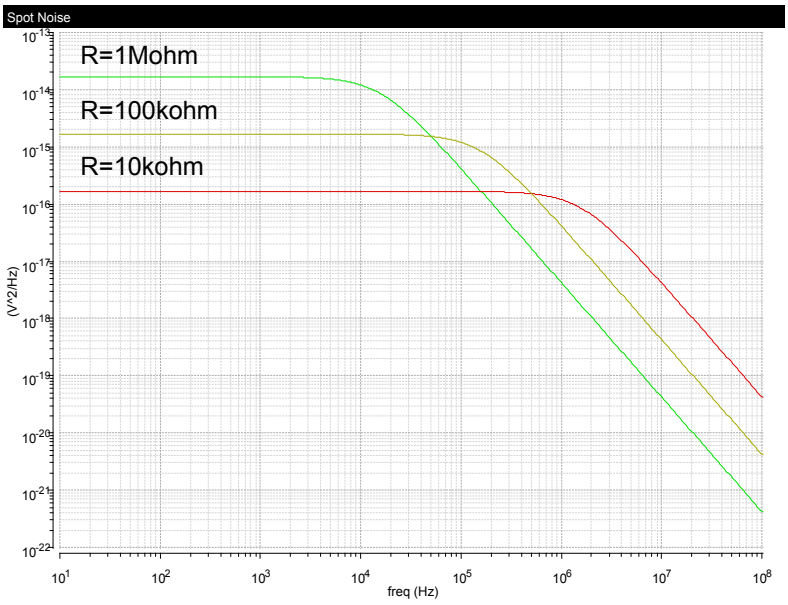

Fig. 1.16: Spot noise, C=10pF

Integrating Eq. (1.36) we calculate the *power*:

$$\overline{v_{n,o}^2} = \int_{f_{min}}^{f_{MAX}} \left|\frac{R}{1+j2\pi fRC}\right|^2 \frac{4kT}{R} df \tag{1.37}$$

so,

$$\overline{v_{n,o}^2} = \int_{f_{min}}^{f_{MAX}} \frac{R^2}{1+4\pi^2 f^2 R^2 C^2} \frac{4kT}{R} df \tag{1.38}$$

which, since

$$\int \frac{1}{1+x^2} dx = tan^{-1}(x) \tag{1.39}$$

it reduces to:

$$P_{n,o} = \frac{2kT}{\pi C} tan^{-1}(2\pi RCf)\Big|_{f_{min}}^{f_{MAX}} \tag{1.40}$$

or the more common used RMS value (Figure 1.17):

$$V_{RMS} = \sqrt{P_{n,o}} = \sqrt{\frac{2kT}{\pi C} tan^{-1}(2\pi RCf)}\Bigg|_{f_{min}}^{f_{MAX}} \tag{1.41}$$

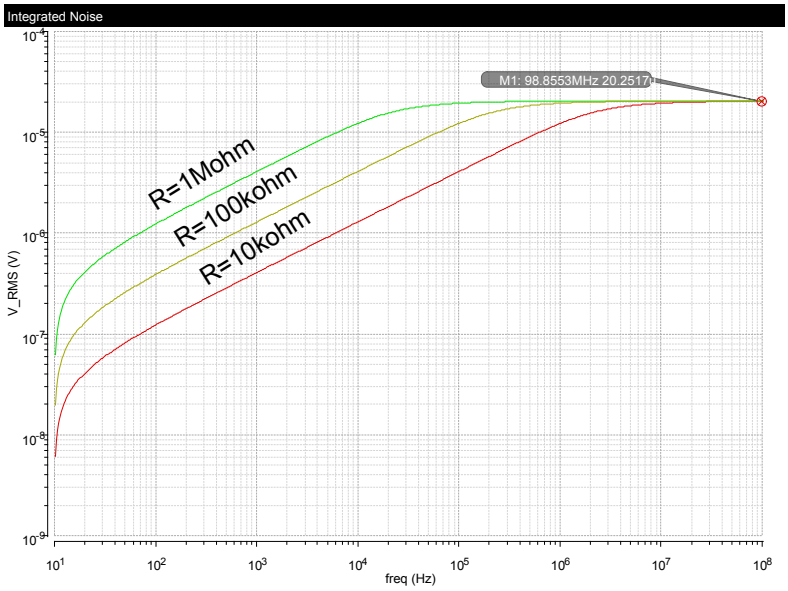

Fig. 1.17: Integrated noise, C=10pF

If we consider the full bandwidth Eq. (1.41) reduces to:

$$V_{RMS}\Big|_{f_{min}\to 0}^{f_{MAX}\to\infty} = \sqrt{\frac{kT}{C}} \tag{1.42}$$

This is an important and curious result that shows us that the V_{RMS} is *independent from the resistance* as shown in Figure 1.17 where we see that at a $f >> f_0$ the RMS value does not increase more and all the three curves converge at $\sqrt{\frac{kT}{C}}$.

This "curious" result leads us to think that if we want to reduce the Noise we must increase the capacitor, this is completely true if we are interested in the full bandwidth noise, but if we have a Noise specific in a frequency range $f_{min} < f < f_{MAX}$, some R-C values can be better that others (think to consider the $f_{MAX} = 100kHz$ in the Figure 1.17) and so we have to design in an efficient way.

Chapter 2

Realizations

Until now we talked about the Noise always referring to the *PSD* (*Power Spectral Density*), but in the time domain how is it manifested?

Some *white* noise sources as *thermal* and *shot* have a *Gaussian distribution of amplitudes* in the time domain, but in general a Noise PSD has *any shape* and not necessarily constant, so we can not to know *how* is its *time behavior*. The only thing we can made is trying to observe directly in the time domain the signal or, if we have a measure of the *PSD*, to make a *Realization* in time.

During my stage at *Infineon Technologies Italia* I spent a time period to realize a program in *Matlab* to make some *Realizations in time domain* from a PSD measure or a PSD simulation (*Noise Analysis*) to solve the following problem:

To characterize the stability of an *LDO* (Linear Voltage Regulator with *Low Drop Out*) it is convenient to apply a I_{LOAD} *step* very small (that can be treated as a *small signal* and at a first approximation it doesn't change the *DC operating point* of the regulator I_{LOAD}, $V_{o,REG}$) and to measure the output voltage, this is made for *"all"* operating conditions: C_L, R_{ESR}, I_{LOAD}, *temperature*, etc... A voltage regulator may be modeled as a *2 poles system* (this is explained in Chapter 3) so its voltage response to a load current step may be *oscillatory* or *monotonic* in dependence to the *Phase Margin* (PM). Measuring the amplitude of the *overshoot* it's possible to calculate the *PM*, however, the amplitude of the overshoot is small (mV or less) because the load current step is very small and if the regulator presents a lot of Noise ($V_{o,N,RMS}$ may be few mV), it's possible that the Noise covers completely the voltage response (see Figure 2.1).

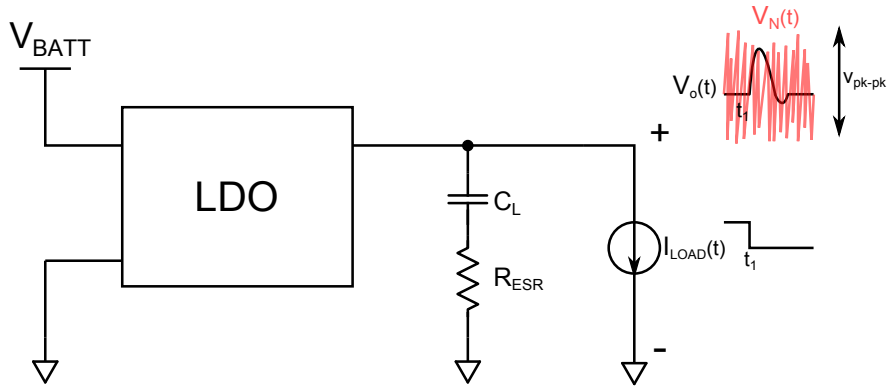

Fig. 2.1: Stability measure in a Noisy LDO

However the output voltage doesn't diverge if the regulator is *stable*, but measuring the overshoot become impossible because of Noise. The best solution would be to project a *Low Noise* voltage regulator, but if *Noise* is not a specific we can design a *Noisy* LDO and however we would like to measure its stability.

Since it's useless to make the measure of the overshoot, we rely on the *Noise simulations* and their subsequent realization in time domain. Referring to Figure 2.1, it was established that if the realization in time domain presents a noise band less than $3mV_{pk-pk}$ ($1.5mV_{pk}$)

the stability is assured because the phase margin is surely greater than $20 - 25°$ (the minimum allowed), but if the V_{pk-pk} is greater than $3mV$ the system may be unstable or may have a too small phase margin.

To make this test we have to be able to make a temporal realization from a *PSD* simulation.

Let's show first how to obtain the *PSD* from a signal in time domain, that is an easier and introductory problem, and then we show how to make a *temporal realization* from a PSD.

2.1 PSD Calculation

We have N *samples* from a signal in time domain (so *Real numbers*) $x(nT_s)$ with $n = 1, 2, ..., N$ and $\frac{1}{T_s}$ is the sampling frequency, at first we have to calculate the *Discrete Fourier Transform (DFT). DFT* supposes to receive a *periodic repetition* of input samples and it returns N values X_k (*Complex numbers*) that are the *Fourier Coefficients*, in Eq. (2.1):

$$X(k\Delta f) = \frac{1}{N}\sum_{n=1}^{N} x(nT_s)e^{-j\frac{2\pi}{N}(n-1)(k-1)} \tag{2.1}$$

$\Delta f = \frac{1}{NT_s}$ is the *frequency quantum* and k is an integer variable. *Matlab* calculates Eq. (2.1) using an *FFT* algorithm (*Fast Fourier Transform*) that is faster that the exact calculation of *DFT*.

An important thing to know is that, because of the hypothesis that input samples are a periodic repetition, the coefficients calculated refer to a *periodic repetition in frequency* of the spectrum as in Figure 2.2.

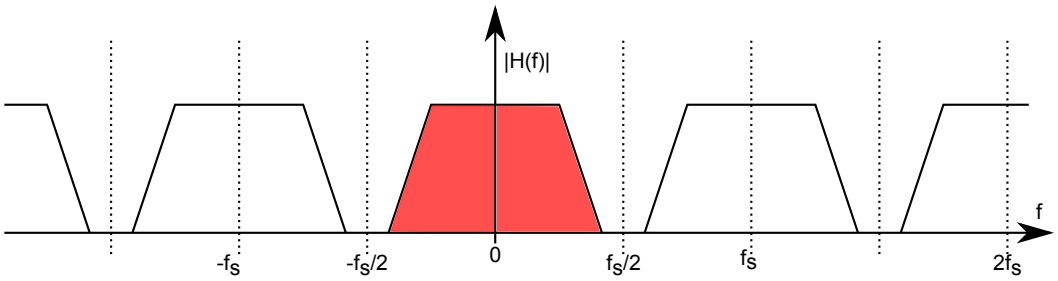

Fig. 2.2: Spectrum repetition

As depicted in Figure 2.2 only the *red* spectrum brings an *information*, the others are only a repetition around kf_s with $k = ..., -2, -1, 1, 2, ...$ To note that if we sample the signal at a rate f_s, the maximum frequency at which it's possible to have a correct information is the *Nyquist frequency* $\frac{f_s}{2}$, in agreement with the *Nyquist Theorem*.

Let's look more closely how are the coefficients give back from Eq. (2.1) (remember that are *complex numbers*), they are slightly different according that $x(nT_s)$ has an *even* or *odd* number N of samples:

- **Even**

$$X(1), X(2), ..., X\left(\frac{N}{2}\right), X\left(\frac{N}{2}+1\right), X\left(\frac{N}{2}+2\right), ..., X(N) \tag{2.2}$$

that they correspond to

$$X(f=0), X(f=\Delta f), ..., X\left(\frac{f_s}{2}-\Delta f\right), X\left(\frac{f_s}{2}\right), \overline{X\left(\frac{f_s}{2}-\Delta f\right)}, ..., \overline{X(f=\Delta f)} \tag{2.3}$$

the $\overline{(\cdot)}$ means the *complex conjugate*.

- **Odd**

$$X(1), X(2), ..., X\left(\left\lceil\frac{N}{2}\right\rceil\right), X\left(\left\lceil\frac{N}{2}\right\rceil+1\right), ..., X(N) \tag{2.4}$$

that they correspond to

$$X(f=0), X(f=\Delta f), ..., X\left(\frac{f_s}{2}-\Delta f\right), \overline{X\left(\frac{f_s}{2}-\Delta f\right)}, ..., \overline{X(f=\Delta f)} \tag{2.5}$$

the $\lceil(\cdot)\rceil$ means the *up rounding*.

For simplicity we assume N *is even*, so referring to Relation (2.3), we note that about the first half of coefficients bring the information of the *module* and *phase* and the second half don't add information because has the same module and inverted phase. This is because of we are working with real-valued signals in time domain, so they enjoy (in frequency) of the *Hermitian property* $X(f)=\overline{X(-f)}$. Eq. (2.1) and so Relation (2.3) refers to the *Bilateral spectrum* ($0 \le f \le f_s$ or equivalently $-f_s/2 \le f \le +f_s/2$) but, thanks to Hermitian symmetry, we can use only the *Single-side spectrum* so $X(1), ..., X\left(\frac{N}{2}+1\right)$.

Now we have $\frac{N}{2}+1$ data that *dimensionally* are not a *PSD*, if for example the temporal signal is a voltage $v(t)$, the $|X(k\Delta f)|$ have the dimension of $Volts$, so it is necessary a division for a frequency (or a root frequency).

Another fundamental feature is to *conserve the power* from the passage bilateral to monolateral spectrum, this is simple because the total power of two harmonics is

$$|X(k\Delta f)|^2 + |\overline{X(k\Delta f)}|^2 = A^2 + A^2 = 2A^2$$

so we may replace them with a single harmonic of amplitude $\sqrt{2}A$.

PSD values ($N/2+1$ in total) can be calculated as:

$$V^2(k\Delta f)\Big|_{V^2/Hz} = \frac{2|X(k\Delta f)|^2}{\Delta f} \tag{2.6}$$

or the square root value:

$$V(k\Delta f)\Big|_{V/\sqrt{Hz}} = \frac{\sqrt{2}|X(k\Delta f)|}{\sqrt{\Delta f}} \tag{2.7}$$

or, in a common logarithmic scale (R_{ref} is a reference resistance, usually is 50Ω):

$$V(k\Delta f)\Big|_{dBm/Hz} = 10log_{10}\left(\frac{V^2(k\Delta f)\Big|_{V^2/Hz}}{R_{ref}\times 1mW}\right) \tag{2.8}$$

These Relations (2.6), (2.7) are used for $X(k)$ with $k=2,3,...,N/2$ because these harmonics are mirrored (bilateral spectrum), otherwise $X(1)$ (DC component) and $X(N/2+1)$ ($f_s/2$ component) are *unique* (see Relation (2.3)) so don't need of the 2 and $\sqrt{2}$ factors respectively in Relations (2.6), (2.7).

The frequency axis is discretized in $N/2+1$ values equispaced by Δf, thus $f = 0, \Delta f, ..., \frac{f_s}{2} - \Delta f, \frac{f_s}{2}$.

Total Power may be calculated in this way:

$$P_{tot}\Big|_{V^2} = \Delta f \sum_{k=0}^{N/2+1} V^2(k\Delta f)\Big|_{V^2/Hz} \tag{2.9}$$

ans thus:

$$V_{RMS}\Big|_{V} = \sqrt{P_{tot}\Big|_{V^2}} \tag{2.10}$$

An example of PSD calculation is in Appendix A.4.

2.2 Realization in time domain

To realize a signal from the frequency to the time domain, the core of this "transformation" is the *Inverse DFT*:

$$x(nT_s) = \sum_{k=1}^{N} X(k\Delta f) e^{+j\frac{2\pi}{N}(n-1)(k-1)} \tag{2.11}$$

N is the total number of frequency samples.

In general we may have as input a *PSD single-sided spectrum* (the *module*) existing in $f_{min} < f < f_{MAX}$ with N' points *equispaced*. In most cases, both in simulations or in measures with network analyzer, we have points equispaced in a logarithmic scale, for working the Relation (2.11) needs equispaced points in linear scale with a fixed Δf, so if it is necessary, we must interpolate data to obtain (from N' points to M points):

$$V(f_{min}), V(f_{min} + \Delta f), ..., V(f_{MAX} - \Delta f), V(f_{MAX}) \tag{2.12}$$

There are M points equispaced by Δf (M is not chose at random). We will assume $V(k\Delta f)$ have dimension of $V/\sqrt{Hz}$, if they derive from a measure with Network Analyzer, probably they could be in dBm, so at first we have to make the conversion, considering that:

$$P(k\Delta f)\Big|_{dBm/Hz} = P_{measured}\Big|_{dBm} - 10log_{10}IFBW \tag{2.13}$$

IFBW [Hz] is the *Intermediate Frequency Bandwidth* to set in the Network Analyzer. And it is also:

$$P(k\Delta f)\Big|_{dBm/Hz} = 10log_{10}\left(\frac{V^2(k\Delta f)\Big|_{V^2/Hz}}{R_{in} \times 1mW}\right) \tag{2.14}$$

so equating Eq. (2.13) to Eq. (2.14) we may calculate:

$$V(k\Delta f)\Big|_{V/\sqrt{Hz}} = 10^{\left(P_{measured}\Big|_{dBm} - 10log_{10}IFBW + 10log_{10}(R_{in} \times 1mW)\right)/20} \tag{2.15}$$

Now we have PSD data of a *single-sided spectrum*, to obtain a correct realization in time domain we have to pass to *IFFT* Relation (2.11) some coefficients in the form like (2.3) with the *Hermitian property* and the same *unit of measure*.

Coefficients in (2.3) are equispaced by Δf in $0 \leq f \leq f_{MAX}$ so it's necessary to add a number $m = \dfrac{f_{min}}{\Delta f}$ of points that cover the band $0 \leq f < f_{min}$, this points must have zero amplitude so they don't add power to the original spectrum. The best choice is to be able to chose the frequency quantum Δf (Δf must be chosen so that m will be an *integer* number), in this way m is fixed and also the number M (2.12) is fixed because $M = \dfrac{f_{MAX} - f_{min}}{\Delta f}$. This implies that the total number of frequency points for the single-sided spectrum is fixed too because is $m + M = \dfrac{f_{MAX}}{\Delta f}$.

Now we multiply the values by $\sqrt{\Delta f}$ to ensure the values represent *Volts* in this case, and to convert them in *complex numbers* we associate for every value a *random phase* φ generated from a *uniform distribution* (see A.2).

$$X(k\Delta f) = \alpha + j\beta = V(k\Delta f) \times \sqrt{\Delta f} \times \frac{1}{\sqrt{2}} \times e^{j\varphi} \tag{2.16}$$

for $k = 2, ..., m + M - 1$.

The factor $1/\sqrt{2}$ represents the necessity to split in 2 the *power* because the coefficients (2.3) represent the *double-sided spectrum* (the DC harmonic $X(0)$ and the last at f_{MAX} $X(m + M)$ are *unique*, so don't need the factor $1/\sqrt{2}$), see Figure 2.3 for clarity. The last step is thus to mirror values (2.16) with *opposite phase* to respect Hermitian symmetry.

$$X(1), X(2), ..., X(m+M-1), X(m+M), X(m+M+1), ..., X(N = 2m+2M-2) \tag{2.17}$$

that they correspond to

$$X(f = 0), X(f = \Delta f), ..., X\left(\frac{f_{MAX}}{2} - \Delta f\right), X\left(\frac{f_{MAX}}{2}\right), \overline{X\left(\frac{f_{MAX}}{2} - \Delta f\right)}, ..., \overline{X(f = \Delta f)} \tag{2.18}$$

To obtain a real-value signal from Eq. (2.11) we must set $\varphi(X(f_{MAX}/2)) = 0$, the phase of $X(0)$ is not relevant because its module is null.

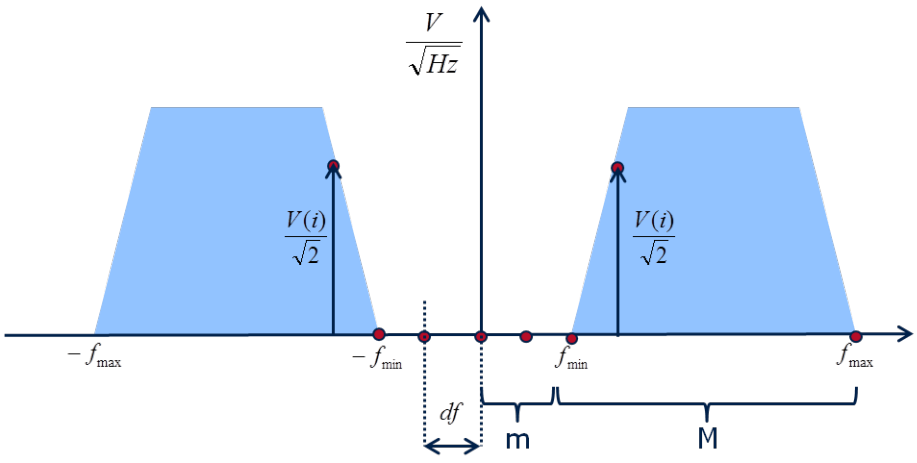

Fig. 2.3: Single-sided to Double-sided spectrum

Let's pass coefficients (2.18) to Eq. (2.11) and we obtain N $N = 2m + 2M - 2$ values that represent the amplitude of the signal in time-domain $x(nT_s)$ (in *Volts* in this case).

To obtain the *time* axis is simply because there are N points equispaced by the the "sampling time" $t_s = \frac{1}{N\Delta f}$.

An example of realization is shown in Appendix A.5.

2.3 Test pk-pk and Comparison

The purpose of the *Realization program* is to be used for performing the $3mV_{pk-pk}$ *Test* as discussed in Chapter 2-Introduction.

The Test is performed by making a *Realization* $v(nT_s)$ in time domain of an input *PSD Single-sided spectrum*, then we keep the absolute value $|v(nT_s)|$ so the signal is only positive (remember that $v(nT_s)$ has zero-mean for construction), we define a *threshold* $x\%$, if the percentage of values $|v(nT_s)|$ that exceed $1.5mV_{zero-pk}$ is more than $x\%$, therefore the Test is *Failed*, otherwise the Test is *Successful*. Test *Failed* means that we cannot ensure the testability of the device, Test *Successful* means that the simulated *LDO* can be considered stable.

The program *Realization+Test* is been conceived mainly to be used with the parameterization of *Noise Simulations* in *CADENCE*. For default the threshold percentage is set $x\% = 95\%$, in this way the signal, to pass the test, would be remain in the band $\pm 2\sigma_v$, however the failure percentage can be varied. Indeed the $x\% = 95\%$ does not match the $\pm 2\sigma_v$ because the realization $v(nT_s)$ has not a *Gaussian distribution of amplitudes* because derives from a general *PSD*.

2.3.1 Measurement

As verification of my work and as example I report a measurement on a quite noisy LDO, the setup is explained in A.2 and also I made some measures with the *oscilloscope* with the same load conditions of Figure A.8 and the oscilloscope is simply connected at V_{out}.

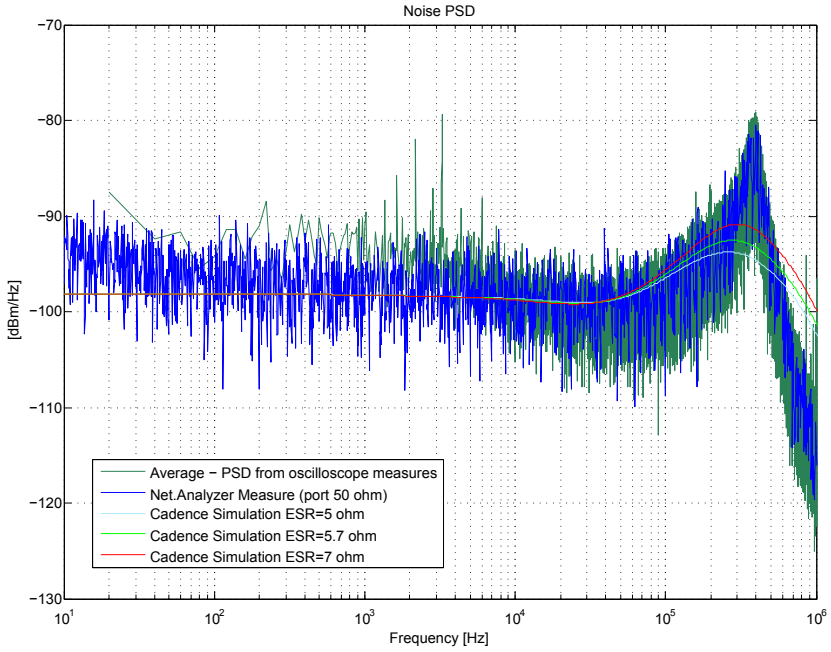

Fig. 2.4: Comparison between Measures and Simulations

Let's compare the integrated V_{RMS}:

- in the approximately *white* bandwidth $100Hz \leq f \leq 100kHz$:

$Net.Analyzer - V_{RMS}[mV]$	$Aver.Oscilloscope - V_{RMS}[mV]$	$Simulation - V_{RMS}[mV]$
0.84	0.86	0.91

- and in the full bandwidth $10Hz \leq f \leq 1MHz$:

$Net.Analyzer - V_{RMS}[mV]$	$Aver.Oscilloscope - V_{RMS}[mV]$	$Simulation - V_{RMS}[mV]$
5.4	5.1	4.5

The resonant peak in relatively high frequency (see Figure 2.4) generates a lot of noise and it derives from the small *phase margin* in this load condition, this example show us that a good compensation is one of the most important thing to ensure for reaching low noise performance.

Chapter 3

Noise in LDO

3.1 Introduction to LDO

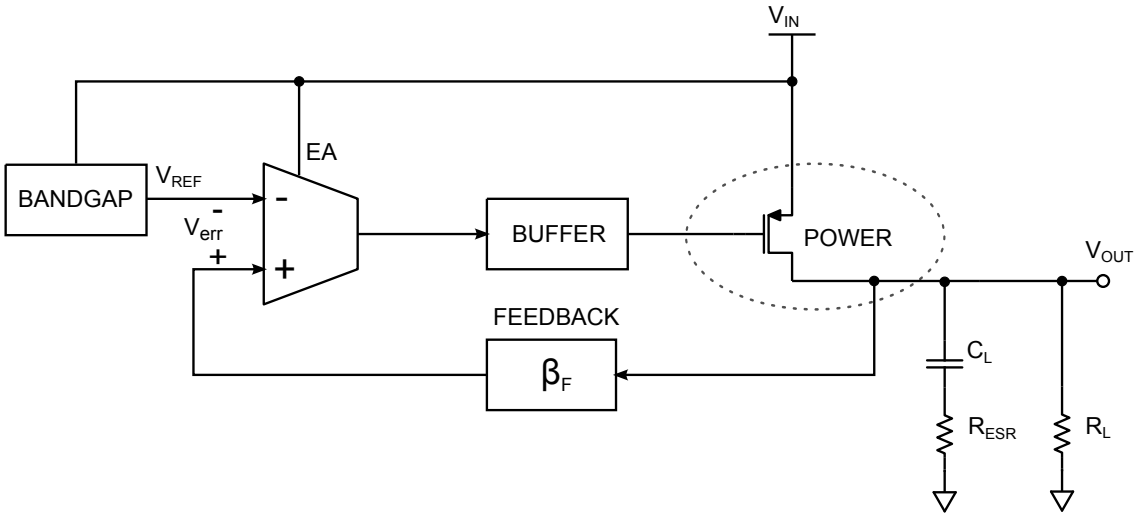

Fig. 3.1: Linear Voltage Regulator

A *Voltage Regulator* is a common circuit in ICs, it is indispensable in electronics because, as the name says, it regulates and maintains constant the output voltage at a variation of load R_L. There are two classes of voltage regulators: *Linears* and *Switching*.

Switching regulators are complex to design and the output voltage is *constant* only in *"average"* because the waveform is discontinue ("switched") and so is "dirty" of harmonics, but their strength is the *high efficiency* that in theory could reach the 100%, in practice good values obtained are $90 - 96\%$.

Otherwise, *Linear regulators* are relatively simple to design, have a fast response to a load/line step, and are generally low Noise, the weak point is the *low efficiency*:

$$\eta_{Lin-Reg} = \frac{P_{OUT}}{P_{IN}} = \frac{I_{LOAD}V_{OUT}}{(I_{LOAD} + I_Q)V_{IN}} < \frac{V_{OUT}}{V_{IN}} \tag{3.1}$$

where I_Q is the quiescent current that flows to ground but not in the load ($V_{IN} = V_{DD}$ in Figure 3.1).

Thus to maximize the efficiency we would work with $V_{OUT} \approx V_{IN}$, the term $V_{IN} - V_{OUT} = V_{DO}$ is just the *drop-out* voltage that falls across the pass device ($V_{OUT} - V_{IN} = |V_{DS}|$ of the *Power* stage in Figure 3.1), the name *LDO* means *Low Drop Out*, so a linear regulator with a voltage drop-out of *few hundred of mV*, so their efficiency is quite good.

A Linear Regulator is a negative feedback system, the circuit (Figure 3.1) tends to delete the voltage error

$$V_{err} = \beta_F V_{OUT} - V_{REF} \to 0 \tag{3.2}$$

so

$$V_{OUT} = \frac{1}{\beta_F} V_{REF} \tag{3.3}$$

β_F is a scale factor introduced by the *Feedback* and V_{REF} is a voltage reference. The power flux (so the I_{LOAD} flux) flows through the power device to the load. Let's give a brief description of the blocks in Figure 3.1:

- **BANDGAP**: this is the circuit that generates the V_{REF}, it must be precise respect variations of V_{IN} and *Temperature*, usually is not connected directly to V_{IN} but it is powered by an internal supply. This block produces a lot of Noise and is the most critical block to reach low-Noise performance.

- **ERROR AMPLIFIER**: this is a *single-ended OTA* (*Operational Transconductance Amplifier*) that produces a current proportional to the input voltage error $i_{EA} = gm_{EA} v_{err}$, then the current flows in the output resistance and produces a voltage $v_{out,EA} = i_{EA} R_{out,EA}$. The role of this block is to amplify v_{err} with high gain (this is the core of the circuit), the higher the gain, the smaller will be the static error on V_{out}.

- **BUFFER**: the buffer has an AC gain close to 1, its job is to drive the power stage the best possible, so its output should be nearest as possible to the extremes V_{DD} and *ground*. This to ensure the maximum V_{GS} to the power transistor. Moreover, the buffer output resistance should be the smallest as possible to push in high frequency the pole at the power stage input $f_{pole} = \frac{1}{2\pi R_{o,BUFF} C_{in,POW}}$ because this is a parasitic pole.

- **POWER**: the power transistor may be both *Bipolar* or *MOS* and also to be *N-type* or *P-type*. To design the pass device we have to make some tradeoffs, to reduce the power loss through the pass device ($P_{pass} = (I_{o(max)} + I_{GND}) V_{DO}$ with $V_{DO} = V_{in} - V_{out}$) the best choice is a P-type transistor (specially P-MOS), instead to have a fast response at the output it is convenient to use a N-type transistor due to its smaller output resistance. A general comparison is summarized in Table 3.1, the $\surd$ symbol represents the best choice.

	N-type Power Pass Devices		**P-type Power Pass Devices**	
Parameter	**BJT**	**MOS**	**BJT**	**MOS**
$V_{IN(min)}$	$V_{OUT} + V_{DO}$	$V_{OUT} + V_{DO}$	$V_{BE} + V_{CE(sat)}$ $\surd$	$V_{GS} + V_{DS(sat)}$
V_{DO}	$V_{BE} + V_{CE(sat)}$	$V_{GS} + V_{DS(sat)}$	$V_{CE(sat)}$ $\surd$	$V_{DS(sat)}$
I_{GND}	$0A$ $\surd$	$0A$ $\surd$	$I_{o(max)}/\beta$	$0A$ $\surd$
$I_{o(max)}$	Highest $\surd$	Low	High	Moderate
R_o	$1/gm_{BJT}$ $\surd$	$1/gm_{MOS}$	r_o	r_{ds}

Tab. 3.1: Comparison power pass devices

- **FEEDBACK**: the most common element to sense the output voltage is a voltage divider as in Figure 3.2:

$$V_{FB} = \frac{R_2}{R_1 + R_2} V_{OUT} \tag{3.4}$$

and β_F is the feedback factor

$$\beta_F = \frac{R_2}{R_1 + R_2} \tag{3.5}$$

To design this simple divider we may choose the two resistors to set the right V_{OUT} in Eq. 3.4 (V_{REF} is known), instead the value of the resistors fixes the feedback current

$$I_{FB} = \frac{V_{OUT}}{R_1 + R_2} \tag{3.6}$$

the smaller I_{FB} is, the better is in terms of global efficiency.

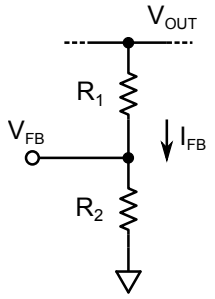

Fig. 3.2: Sensing block

Regarding to C_L and its parasitic R_{ESR} (Figure 3.1), the value of C_L is chosen to guarantee the stability of the LDO and to have a desired transient response to a load/line step (velocity response, small over/undershoot, etc..). Usually a minimum value of $C_{L(min)}$ and a maximum value of $R_{ESR(max)}$ are specified to ensure the stability.

3.1.1 Steady-state performance

Some *Static Regulating performance* of a linear regulator are:

- **LOAD REGULATION**: this static parameter describes how much is the *DC variation* (steady-state) of the output voltage respect to a load current variation, that is:

$$LDR = R_{LDR} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} = R_{out(REG)} + R_{parasitic} \approx \frac{R_{OL}}{1 + \beta A_{OL}}\bigg|_{DC, I_{LOAD}} \tag{3.7}$$

  where R_{LDR} is the load-regulation resistance calculated in steady-state (DC) and dependent from the load current I_{LOAD}, $R_{out(REG)}$ the closed loop output resistance of the regulator, $R_{PARASITIC}$ the bonding and the *PCB* wire parasitic resistance, R_{OL} the open loop output resistance and the A_{OL} the open loop gain of the regulator.

  The load regulation has the dimension of a resistance and smaller is, the better is.

- **LINE REGULATION**: this is also a *static* parameter and it refers to output voltage variations arising from DC changes in the input supply, that is:

$$LNR = A_{in}\bigg|_{DC} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}\bigg|_{DC} \tag{3.8}$$

LNR is the DC supply gain. In general the *supply gain* A_{in} is:

$$\begin{aligned} A_{in}(f) &= A_{in(REG)} + A_{in(REF)} A_{CL} \\ &= \frac{\Delta V_{OUT}}{\Delta V_{IN(REG)}}\bigg|_{\Delta V_{REF}=0}(f) + \frac{\Delta V_{REF}}{\Delta V_{IN(REF)}} A_{CL}\bigg|_{\Delta V_{IN(REG)}=0}(f) \end{aligned} \tag{3.9}$$

where A_{CL} is the closed-loop gain of the regulator. Eq. 3.9 could be calculated with superposition principle with respect to Figure 3.3. To correctly have a good voltage regulation the supply gain may be the smaller as possible.

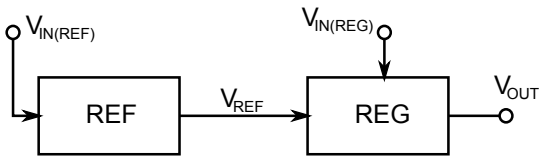

Fig. 3.3: Line regulation scheme

Usually in datasheets, instead of A_{in}, it's possible to find the *PSRR* (*Power Supply Ripple Rejection*, sometimes wrong called Power Supply Rejection Ratio):

$$PSRR(f) = \frac{1}{A_{in}(f)} \tag{3.10}$$

so the $PSRR(f)$ must be the highest as possible. The line regulation is simply

$$LNR = \frac{1}{PSRR(0)}$$

3.1.2 AC analysis

The *AC* study of the regulator is important for the analysis of the *Stability*, we may model the regulator as in Figure 3.4.

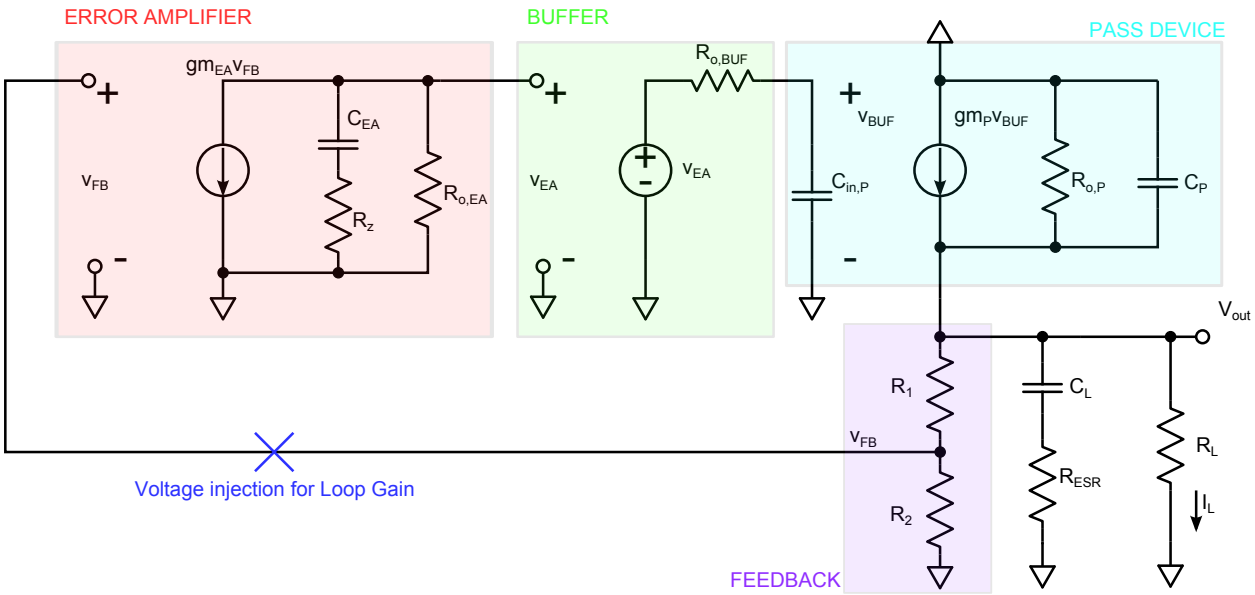

Fig. 3.4: LDO's AC model

In Figure 3.4 all components are of easy intuition, otherwise the capacitor C_P is the sum of more components $C_P = C_{pass-transistor} + C_{in-LOAD}$, $C_{in-LOAD}$ is the input capacitor of the load (every real load has its input capacitor) that is in parallel with R_L.

To study the stability we refer at the *Loop-Gain*, to calculate it the best way is to use the *Middlebrook Voltage injection* ([5]) breaking the loop as in Figure 3.4.

At low frequency (capacitors *open*) the Loop-gain T is

$$T\Big|_{DC} = gm_{EA}R_{o,EA} \times gm_P\big(R_P//R_L//(R_1+R_2)\big) \times \frac{R_2}{R_1+R_2} \tag{3.11}$$

and the general calculation in frequency leads to

$$T(f) = T\Big|_{DC} \frac{\left(1+\frac{s}{2\pi f_{z_{EA}}}\right)\left(1+\frac{s}{2\pi f_{z_{ESR}}}\right)}{\left(1+\frac{s}{2\pi f_{EA}}\right)\left(1+\frac{s}{2\pi f_o}\right)\left[\left(1+\frac{s}{2\pi f_1}\right)\left(1+\frac{s}{2\pi f_2}\right)\right]} \tag{3.12}$$

where:

$$f_{z_{EA}} = \frac{1}{2\pi R_z C_{EA}} \tag{3.13}$$

$$f_{z_{ESR}} = \frac{1}{2\pi R_{ESR} C_L} \tag{3.14}$$

$$f_{EA} = \frac{1}{2\pi R_{o,EA} C_{EA}} \tag{3.15}$$

$$f_o \cong \frac{1}{2\pi (R_{o,P}//R_L) C_L} \tag{3.16}$$

and the terms in [...] are two of the most important *parasitic poles* (there are many others):

$$f_1 = \frac{1}{2\pi R_{o,BUF} C_{in,P}} \tag{3.17}$$

$$f_2 = \frac{1}{2\pi (R_{o,P}//R_L) C_P} \tag{3.18}$$

These pole at f_1 is usually the lowest frequency parasitic pole because $C_{in,P}$ is a quite big capacitor $C_{in,P} = C_{gs} + A_{pass}C_{gd}$, the pass transistor is *big* because it has to supply a high current with a low drop-out, so even the parasitic capacitors are big. To ensure this pole is pushed in high frequency the buffer must have a quite low $R_{o,BUF}$, this requires a challenging design.

If we are able to push parasitic poles in high frequency (at least over few MHz), we can consider the *LDO* like *2 poles system* (f_{EA}, f_o). We have the full control on the error amplifier pole f_{EA}, but the output pole f_o can vary of several decades because the value of C_L can vary of orders of magnitude, this because is the final user (and not the designer) that choose the value of C_L according to various needs (temporal response, over/undershoot, etc.). Usually is indicated the minimum value of C_L that ensure the stability, the user may choose any C_L greater that $C_{L(min)}$ (usually $C_{L(min)}$ is few μF), anyway this is a big capacitor so there is associated a R_{ESR}, its value however is highly unpredictable and varies from few tens of $m\Omega$ to Ω.

From the designer point of view, to ensure the stability for all possible C_L and I_L is a challenge and the *dominant pole compensation* can be made with an *Internal compensation* (f_{EA} is the dominant pole) or with an *External compensation* (f_o is the dominant pole) or a mix. A possible compensation choice is shown in Figure 3.5, where the first pole is the error amplifier pole, then has been created a zero in the error amplifier and the second pole that ensure the crossing (at $0dB$) is the output pole. The zero of the *ESR* can help to save the *phase* but its position is highly unpredictable. In Figure 3.5 are shown two cases of output capacitor $C_L = 1\mu F$ and $C_L = 100\mu F$ to better understand how changes the compensation.

To improve the compensation we can't change appreciably the DC value of the loop gain because this impacts on the *static regulation error* ε_0:

$$\varepsilon_0 \approx \frac{1}{T_0} \tag{3.19}$$

and we would like it to be the smallest as possible.

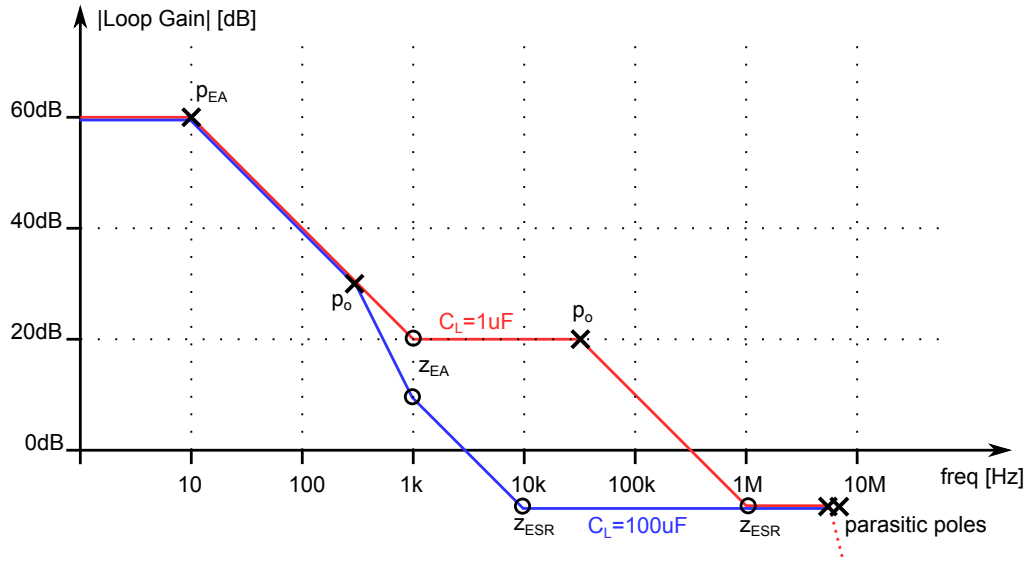

Fig. 3.5: Loop Gain proposed compensation

LDO quasi-ideal circuit for AC study

To study the STABILITY we may use a quasi-ideal model in *Cadence* as in Figure 3.6.

The Error Amplifier is designed to ensure a compensation like that of Figure 3.5 so the $f_{EA} \approx 40Hz$ and $f_{z_{EA}} \approx 4kHz$, the output pole at f_o depends on the I_L and C_L and I used a $ESR = 100m\Omega$. The most problematic parasitic pole at the gate of the pass-device is at about $f_1 \approx 5MHz$ and the other parasitic pole at f_2 is at a higher frequency, we must bring in mind that this is a quasi-ideal circuit so it doesn't describe all parasitic poles, we can assume that in the real circuit there are some parasitic poles close at $10MHz$ so the Loop-Gain can not cross the $0dB$ at a frequency close to $1MHz$. The voltage reference is $V_{REF} = 1.2V$ and the voltage divider $R_1 = 63k\Omega$, $R_2 = 20k\Omega$ is set to regulate $V_o = 5V$. It will be explained further what is the effect of the *Bypass capacitor* C_B.

The Loop-Gain module and phase is shown by varying the R_L $\left(I_L = \frac{5[V]}{R_L}\right)$ and C_L:

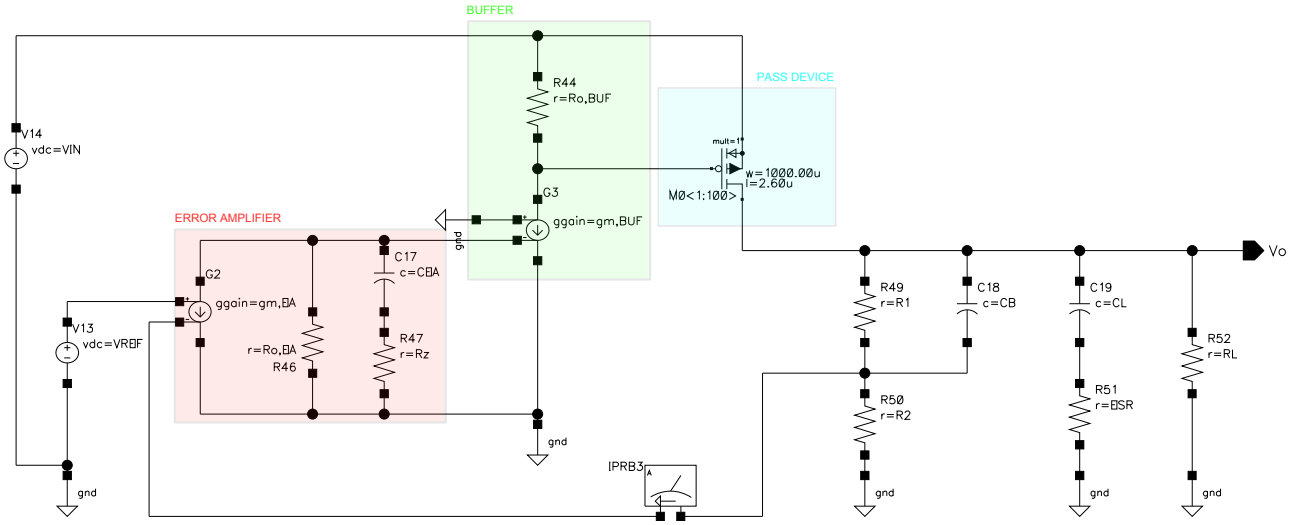

Fig. 3.6: Quasi-ideal LDO circuit

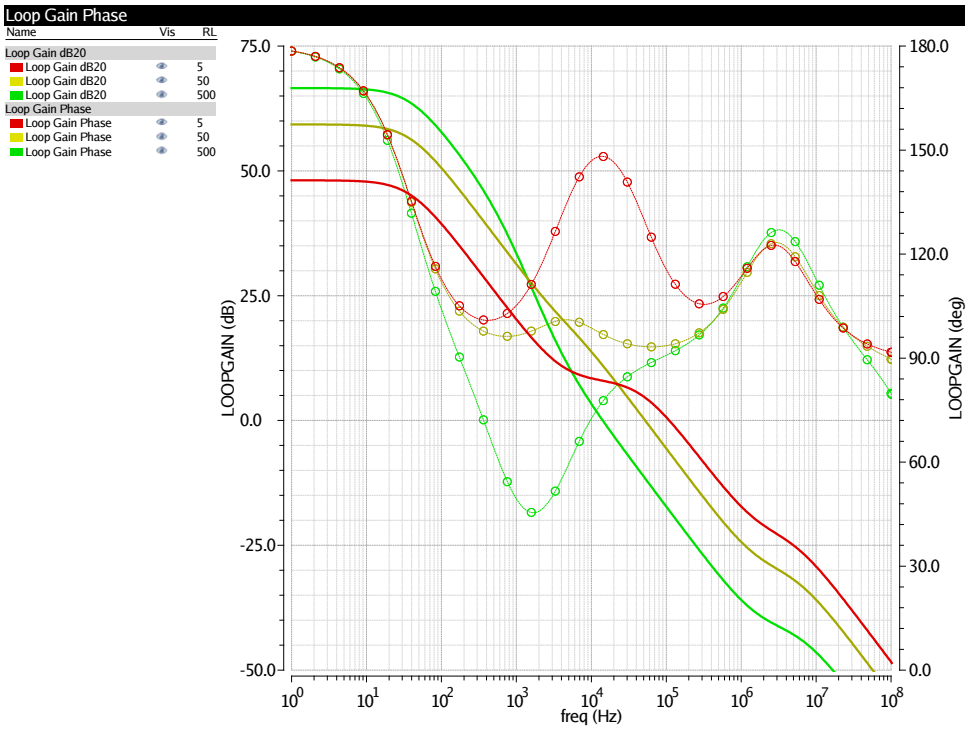

Fig. 3.7: $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 0$

- R_L

  The solid lines in Figure 3.7 are the Loop-Gain *Module* at respectively $I_L = 1A, 100mA, 10mA$ and the dotted lines are the *Phase*, the resulting *Phase margin* is in Tab. 3.2.

- C_L

  The solid lines in Figure 3.8 are the Loop-Gain *Module* at respectively $C_L = 1\mu F, 10\mu F, 100\mu F$ and the dotted lines are the *Phase*, the resulting *Phase margin* is in Tab. 3.3.

Note that the *ESR* is fixed in this case, in a real capacitor the ESR increases as the capacitor increases (almost in a common capacitor, not in a high-performance one) so this may help to save the phase and slightly increase the Phase margin.

R_L [Ω]	PM [deg]
5	114
50	93
500	77

Tab. 3.2: Phase margin, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 0$

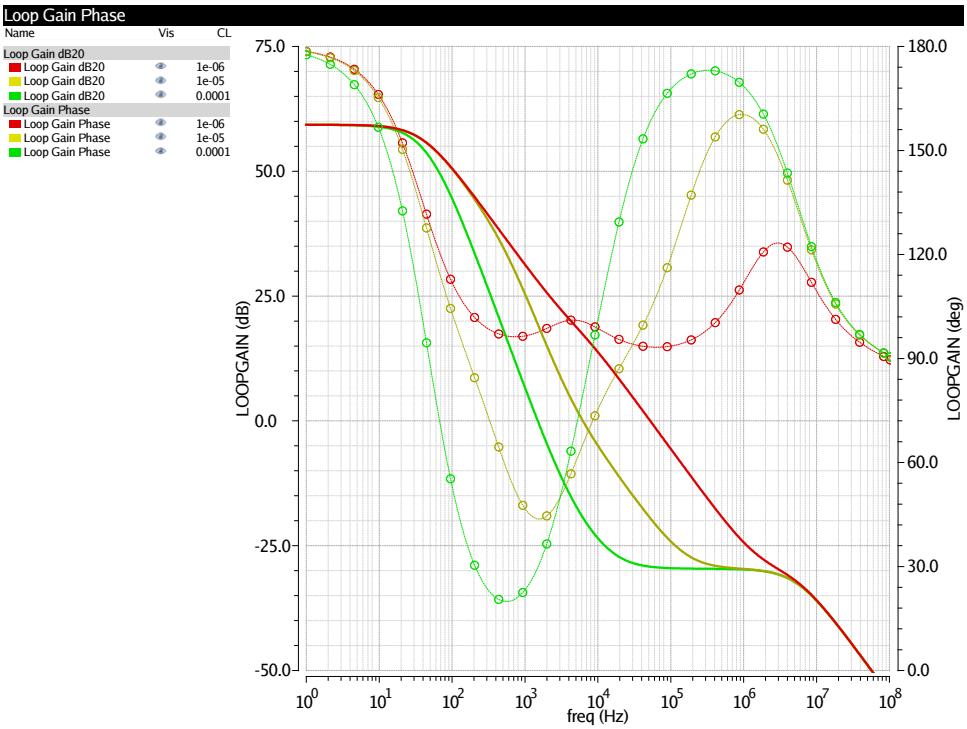

Fig. 3.8: $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 0$

C_L [μF]	PM [deg]
1	93
10	65
100	30

Tab. 3.3: Phase margin, $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 0$

3.2 Noise Model LDO

To develop an *LDO's Noise model* we refer to the block scheme in Figure 3.1, every block produce some noise that we refer at its input as equivalent input noise, the proposed model is depicted in Figure 3.9.

The *Loop-gain* T is:

$$T(s) = G_A Z_A G_P Z_o \beta_F \tag{3.20}$$

with $Z_A = Z_A(s)$ and $Z_o = Z_o(s)$ that contains poles and zeros as in Eq. 3.12.
The transfer functions (TF) are:

$$\frac{V_{N,out}}{V_{N,BG}} = \frac{V_{N,out}}{V_{N,EA}} = \frac{G_A Z_A G_P Z_o}{1 + T(s)} \tag{3.21}$$

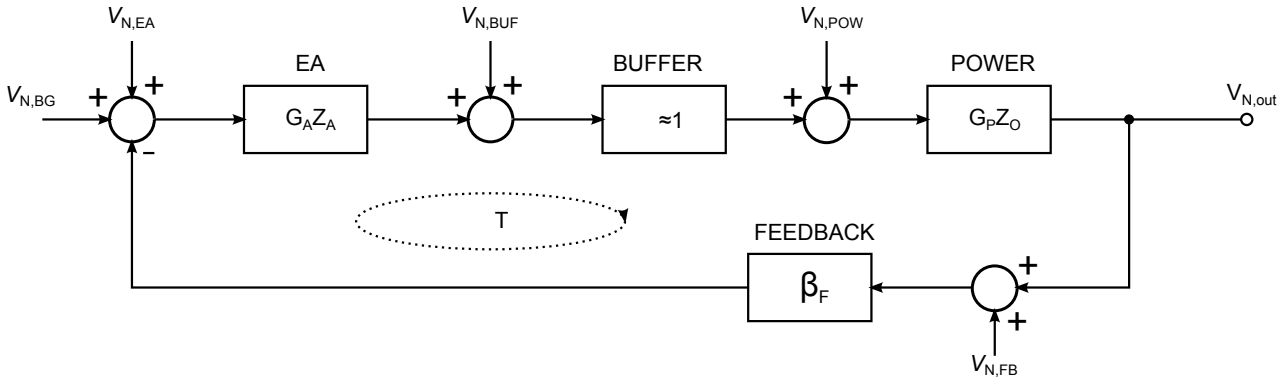

Fig. 3.9: Noise model LDO

$$\frac{V_{N,out}}{V_{N,BUF}} = \frac{V_{N,out}}{V_{N,POW}} = \frac{G_P Z_o}{1+T(s)} \tag{3.22}$$

$$\frac{V_{N,out}}{V_{N,FB}} = -\frac{G_A Z_A G_P Z_o \beta_F}{1+T(s)} \tag{3.23}$$

these transfer functions have to be intended for *PSD* quantities $\left(\text{i.e. } \frac{V_{N,out}/\sqrt{Hz}}{V_{N,X}/\sqrt{Hz}}\right)$.

If we consider to be in the band of the regulator ($|T| >> 1$), the transfer functions reduce to:

$$\frac{V_{N,out}}{V_{N,BG}} = \frac{V_{N,out}}{V_{N,EA}} \approx \frac{1}{\beta_F} \tag{3.24}$$

$$\frac{V_{N,out}}{V_{N,BUF}} = \frac{V_{N,out}}{V_{N,POW}} \approx \frac{1}{G_A Z_A \beta_F} << 1 \tag{3.25}$$

$$\frac{V_{N,out}}{V_{N,FB}} \approx -1 \tag{3.26}$$

as we can see the $V_{N,POW}$ and $V_{N,BUF}$ have a poor effect because are attenuated from the regulation loop, and the strongest impact is from $V_{N,BG}$ and $V_{N,EA}$ because they are injected at the input of the loop and "see" the TF $\frac{1}{\beta_F} > 1$.

Now we understand the importance of a *good compensation* to avoid a *resonance peak* that arises a lot the $1/\beta_F$ factor and it increases the input noise (an example is in Figure 2.4). To avoid the resonance peak the *phase margin* would be greater than about 60° and is difficult to guarantee this for all the operative conditions of the LDO.

Regarding the $V_{N,FB}$ the Eq. 3.23 is based on the hypothesis that the feedback block is a *VCVS* (*Voltage Controlled Voltage Source*), this is true for a high impedance feedback like an *ADC+DAC* but this is not true for the classical *voltage divider*, so it's correct to calculate directly the voltage divider Noise regardless Eq. 3.23.

Aim of the Thesis The aim of this work is to study the feasibility of a **Low Noise LDO** with a $V_{N,out} \leq 20\mu V_{RMS}$ *integrated* output Noise in the bandwidth $10Hz \leq f \leq 100kHz$.

We have just seen that the Noise produced by the power and the buffer is negligible, so the output integrated noise is roughly

$$V_{N,out} \approx \sqrt{V_{N,out(BG)}^2 + V_{N,out(EA)}^2 + V_{N,out(FB)}^2} \tag{3.27}$$

where, in this case, $V_{N,out(BG)}$, $V_{N,out(EA)}$, $V_{N,out(FB)}$ are intended as the Noise, due to these blocks, measured at the output of the regulator. Carefully, we have to partition the Noise budget at the three blocks to reach the target of $V_{N,out} \leq 20\mu V_{RMS}$.

3.2.1 Voltage Divider Noise

The Noise of the classical voltage divider feedback is shown in Figure 3.2, in the band of the regulator ($|T| >> 1$), it is:

$$\frac{\overline{V_{N,out}^2}}{\Delta f} = \frac{\overline{V_{N,R_1}^2}}{\Delta f} + \left(\frac{R_1}{R_2}\right)^2 \frac{\overline{V_{N,R_2}^2}}{\Delta f} \tag{3.28}$$

that, since $\beta_F = \dfrac{R_2}{R_1 + R_2}$, it reduces to

$$\frac{\overline{V_{N,out}^2}}{\Delta f} = \frac{1}{\beta_F} \frac{\overline{V_{N,R_1}^2}}{\Delta f} \tag{3.29}$$

the complete calculation is in Appendix A.6.

This Noise is Thermal resistor noise so it's *white* in the band of the regulator and decreases with the loop-gain when this is smaller than one (so the regulator ceases to regulate), to understand this is helpful to compare Figure 3.10 vs Figure 3.7 and Figure 3.11 vs Figure 3.8.

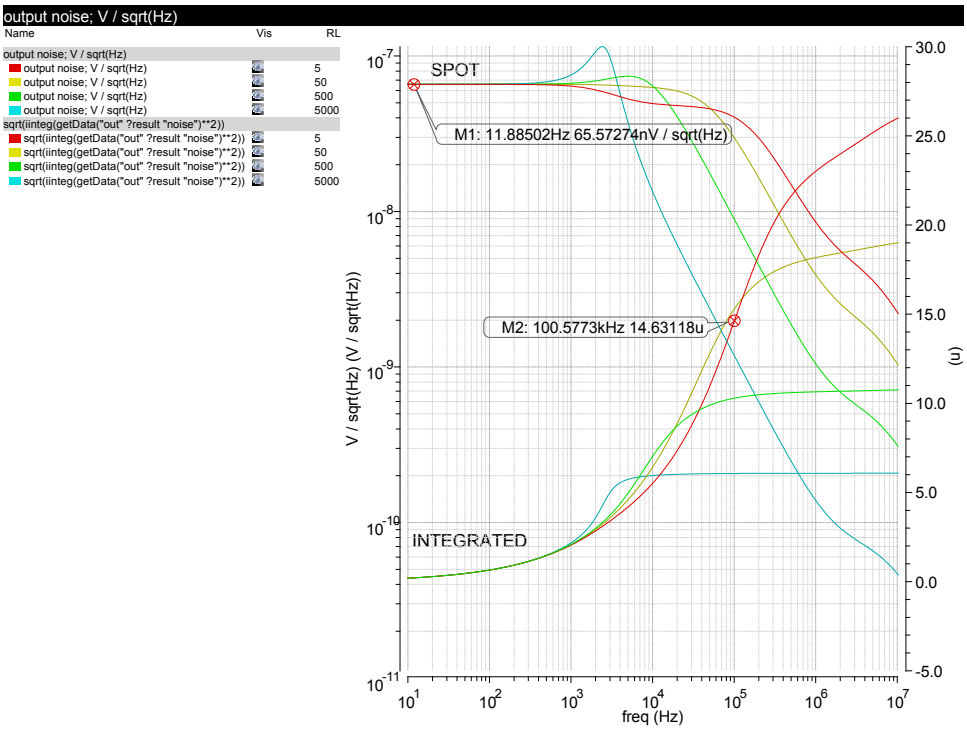

Fig. 3.10: Feedback Noise, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 0$

We can see the peak due to the low phase margin, that increase the Noise, fortunately this happens when the crossing frequency of the loop-gain is quite low respect $100kHz$ so the integrated Noise is acceptable. Instead, when the loop-gain bandwidth is comparable with $100kHz$ the integrated Noise is too high respect the available budget of $20\mu V_{RMS}$. Consider a normal load condition $I_L = 100mA$ and $C_L = 1\mu F$ (the yellow curve in

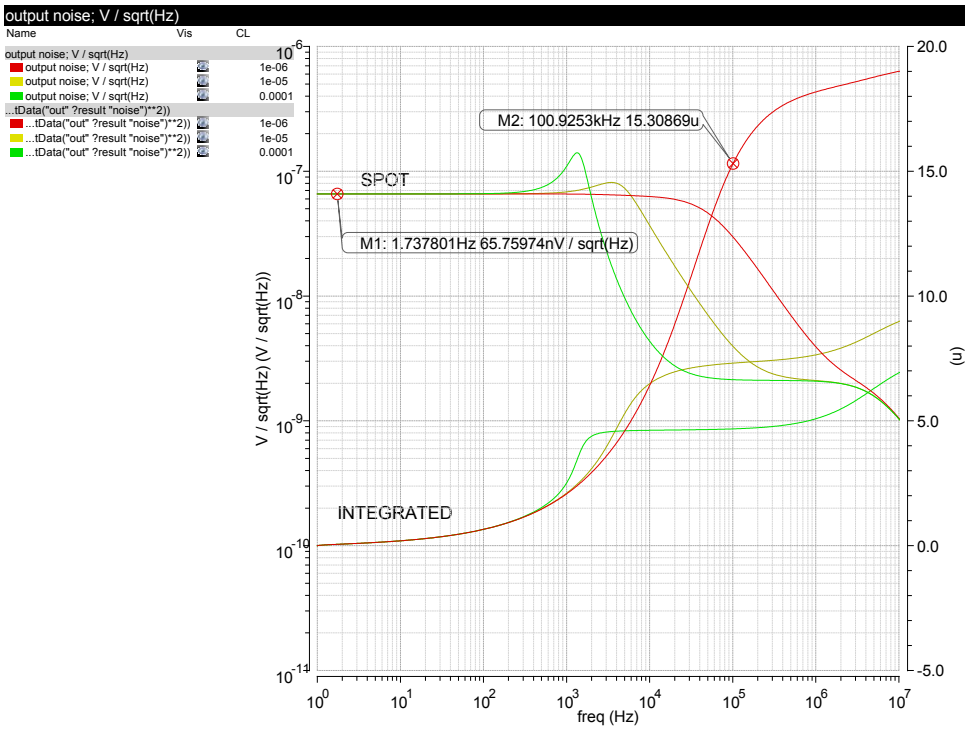

Fig. 3.11: Feedback Noise, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 0$

Figure 3.10), the integrated Noise at the frequency limit $100kHz$ is about $15\mu V_{RMS}$, this is too much, the Noise (spot and integrated) scales with resistance:

$$V_{N,out}^2 \propto R \tag{3.30}$$

thus

$$V_{N,out} \propto \sqrt{R} \tag{3.31}$$

this implies that if resistors R_1 and R_2 increase of 10 so the output noise increases of $\sqrt{10} \approx 3.16$, in this case the Noise will increase as in Tab. 3.4.

R_1 [Ω]	R_2 [Ω]	$V_{N,out}$ [μV]
63k	20k	15
630k	200k	47
6.3M	2M	150

Tab. 3.4: Integrated Noise @100kHz, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 0$

To bypass this problem we have to create a pole at a frequency $f \ll 100kHz$ in the transfer function (Spot Noise figure), this is made by the connection of a *Bypass* capacitor C_B in parallel to R_1 as in Figure 3.6. This capacitor creates a pole at the frequency:

$$f_B = \frac{1}{2\pi C_B R_1} \tag{3.32}$$

The worst case for the pole f_B (so when it is at the higher frequency) is with $R_1 = 63k\Omega$ and $R_2 = 20k\Omega$, in Figure 3.12 is shown the effect at the variation of C_B.

From Figure 3.12 we may see that acceptable values for C_B are $C_B \geq 1nF$, this requires that C_B should be an *external* capacitor, unfortunately this is a bad notice for an integrated LDO but this is necessary for the Noise requirement.

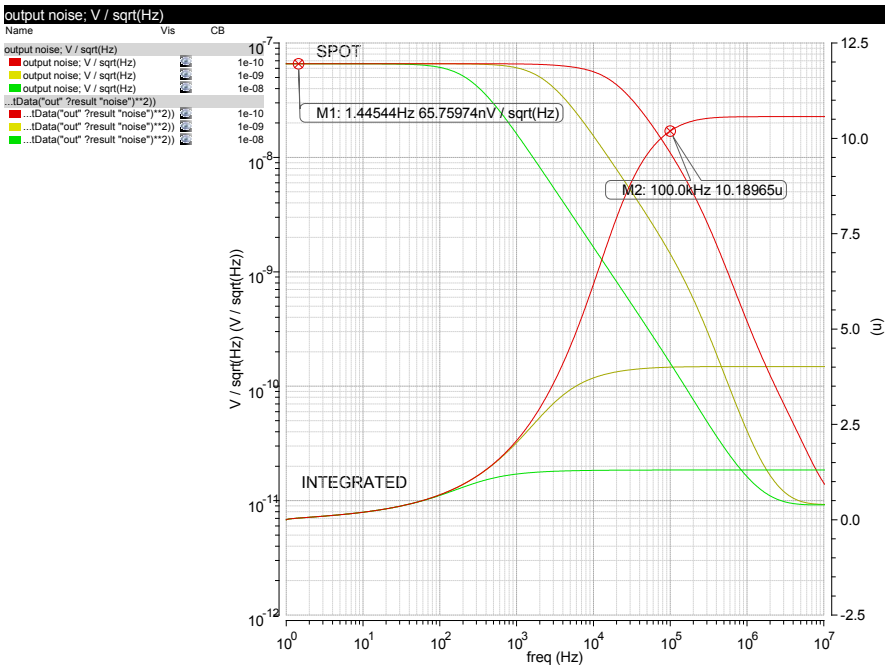

Fig. 3.12: Feedback Noise, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$

Increasing the divider resistances the Noise produced by themselves is increased, but the frequency of pole is moved to a lower frequency as in Figure 3.13.

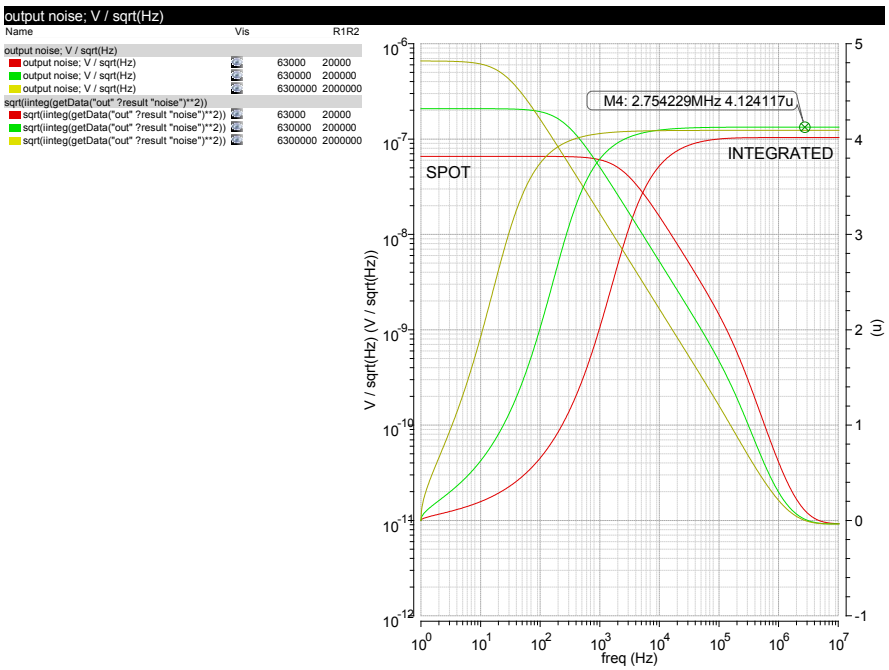

Fig. 3.13: Feedback Noise, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

Seeing Figure 3.13, it seems that the integrated Noise saturates at about $4\mu V_{RMS}$, this is true because, at least until to $100kHz$, the Noise transfer function has a *one pole shaping* like the simply $R - C$ example in Paragraph. 1.4. So when the maximum integration frequency (in this case $100kHz$) is at least a decade greater than f_B, the total

integrated voltage V_{RMS} saturates (Eq. 1.42) at:

$$V_{N,out_{RMS}} = \sqrt{\frac{1}{\beta_F}\frac{kT}{C_B}} \tag{3.33}$$

Therefore the integrated Noise is determined by the C_B, $C_B = 1nF$ leads to a $V_{N,out} = 4.15\mu V_{RMS}$ and $C_B = 10nF$ leads to a $V_{N,out} = 1.31\mu V_{RMS}$.

3.2.2 Load Resistance Noise

The Noise of the *Load* depends at first from the load nature, if we supply a real circuit it absorbs a current but injects some Noise. For example if the load is a physical resistance, it injects its noise in the output node. From the load point of view the circuit is presented as in Figure 3.14.

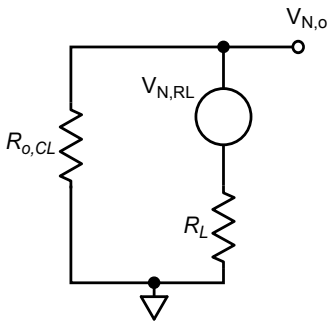

Fig. 3.14: R_{LOAD} Noise circuit

It is a voltage divider between R_L and $R_{o,CL}$, so

$$\frac{V_{N,o}}{\sqrt{\Delta f}} = \frac{R_{o,CL}}{R_{o,CL} + R_L}\frac{V_{N,R_L}}{\sqrt{\Delta f}} \tag{3.34}$$

$R_{o,CL}$ is the closed-loop output resistance of the regulator, it varies in frequency and it is dependent from the load current I_L. To calculate it with an explicit calculation using the circuit in Figure 3.4 it's important to note that we have to remove R_L and we have to maintain the information on the I_L by the insertion of a DC current generator as in Figure 3.15.

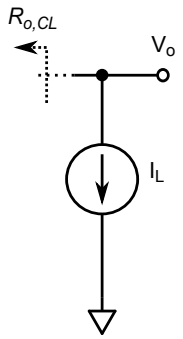

Fig. 3.15: I_L current generator for the calculation of $R_{o,CL}$

An easier way to calculate $R_{o,CL}$ is to observe that a linear voltage regulator with a voltage reference is a feedback system that tends to simulate an ideal $VCVS$ block

(*Voltage Controlled Voltage Source*), the output resistance of a voltage generator is ideally null, so the output resistance of the regulator is a very small quantity:

$$R_{o,CL}(s)\Big|_{I_L} = \frac{R_{o,OL}(s)}{1+T(s)}\Big|_{I_L} \tag{3.35}$$

It's the open-loop output resistance $R_{o,OL} = R_P//(R_1+R_2) \approx R_P$ (at low frequency) reduced by the Loop-Gain, at high frequency the resistances in parallel at the output node tends to the ESR of the C_L. $R_{o,CL}(f)$ is shown in Figure 3.16.

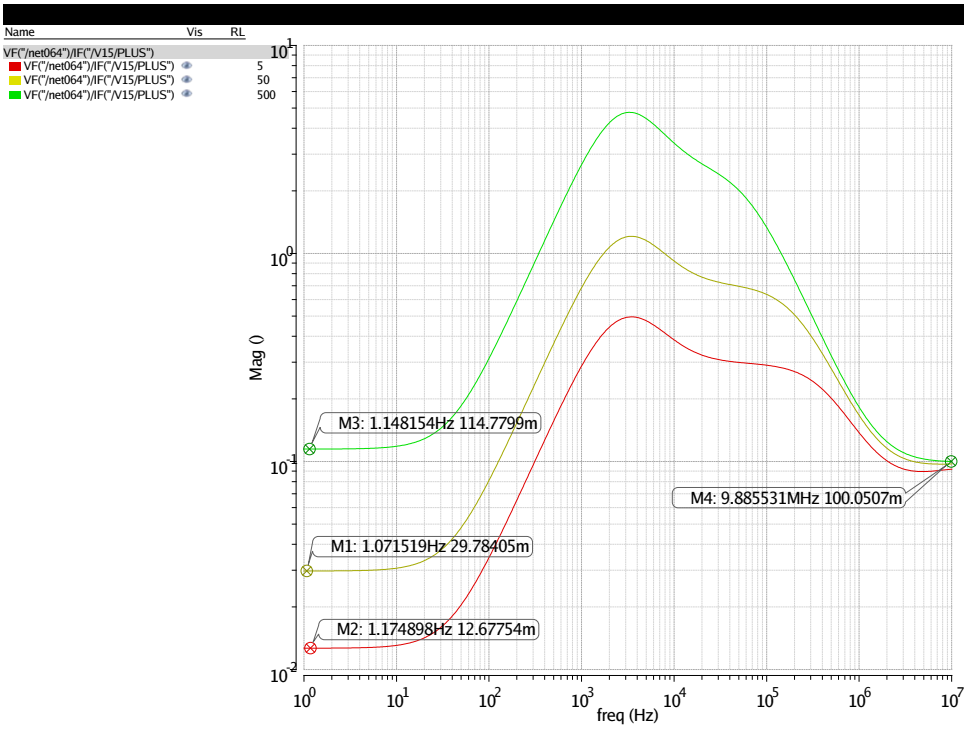

Fig. 3.16: $R_{o,CL}(f)$ [Ω], $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

Back to Noise, at low frequency Eq. 3.34 predicts that the Noise is strongly reduced because $R_{o,CL} \ll R_L$ and at high frequency too is strongly reduced because $R_{o,CL} \approx R_{ESR} \ll R_L$, this is depicted in Figure 3.17.

The integrated noise at $100kHz$ as we can see in Figure 3.17 is always very small for our purpose (about $5nV_{RMS}$), so it can be neglected.

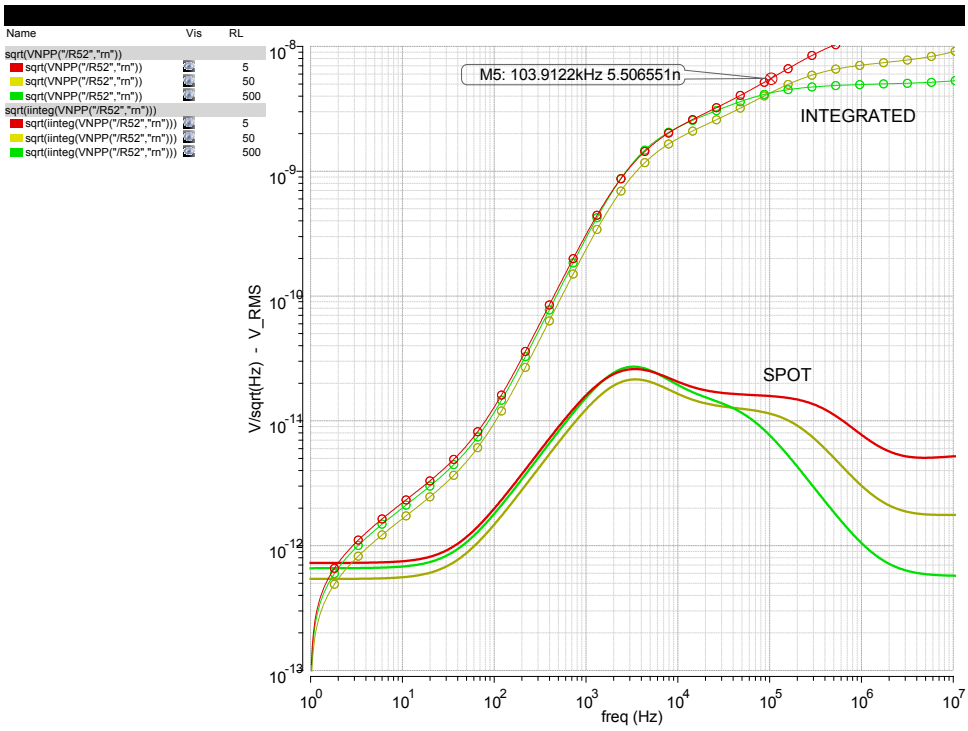

Fig. 3.17: R_L Noise , $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

3.3 Methods To Reduce Noise

3.3.1 Bypass Capacitor

The *Bypass capacitor* not only reduces the resistor divider Noise, but it acts also on the input Noise (*Reference* and *Error Amplifier*) that is the dominant Noise. Let's calculate the transfer function from input to output using the circuit depicted in Figure 3.18.

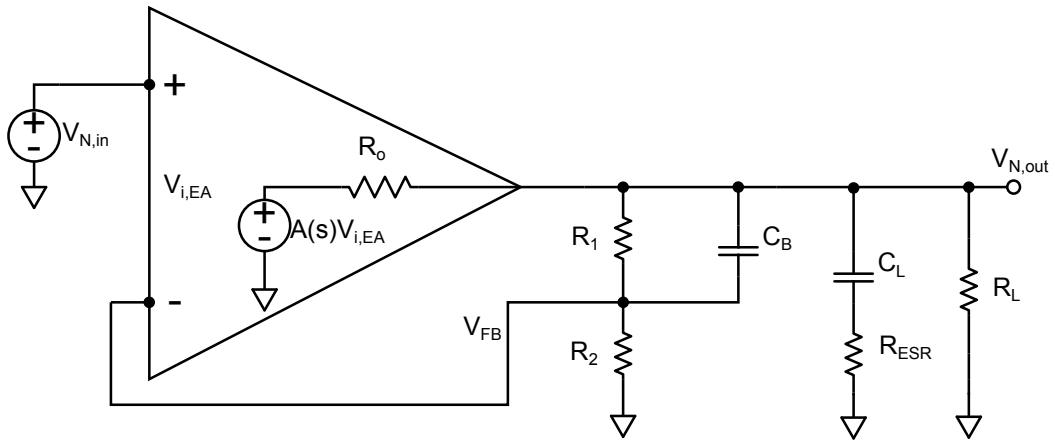

Fig. 3.18: Simplified AC model to show C_B impact on the circuit

From the input "point of view" ($V_{N,in}$) this is a *non-inverting amplifier* with the following transfer function:

$$\frac{V_{N,out}}{V_{N,in}}(s) = \frac{V_{out}}{V_{in}}(s) = \frac{1}{\beta_F(s)} = 1 + \frac{Z_1(s)}{Z_2(s)} \tag{3.36}$$

where $Z_2(s) = R_2$ and $Z_1(s) = R_1 // \frac{1}{sC_B} = \frac{R_1}{1+sR_1C_B}$ so Eq. 3.36 reduces to Eq. 3.37:

$$\frac{V_{out}}{V_{in}}(s) = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{1+sC_B(R_1//R_2)}{1+sC_BR_1}\right) \tag{3.37}$$

At low frequency the input Noise is amplified by $\frac{1}{\beta_{F_0}} = 1 + \frac{R_1}{R_2}$, to avoid to amplify input Noise over the full bandwidth the C_B is necessary to reduce to a unitary gain, Eq. 3.37 is depicted in Figure 3.19 where $f_{p_{FB}} = \frac{1}{2\pi C_B(R_1//R_2)}$ and $f_{z_{FB}} = \frac{1}{2\pi C_BR_1}$.

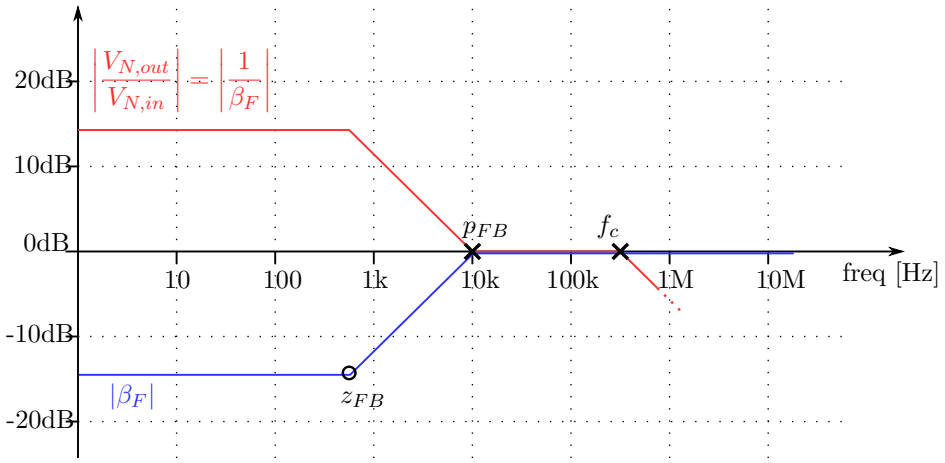

Fig. 3.19: MOS Noise model

Assuming the input Noise is *white*, to avoid an appreciably increase at the Noise due to $1/\beta_F$, the gain must remain unitary at least in the last decade of interest $10kHz - 100kHz$, because the integrated power $Pow = K \times (1/\beta_F)^2 \times (f_{max} - f_{min}) \approx K \times 1 \times 100kHz$.

The input transfer function remains $\frac{V_{out}}{V_{in}}(s) = \frac{1}{\beta_F(s)}$ in the regulation band ($|T| \gg 1$, $|T| = 1$ at the crossing frequency f_c), then inevitably the gain falls to zero with the loop-gain. This reduction may help to reduce input Noise if $f_c < 100kHz$ but this happens only with high C_L or at low I_L, so usually this doesn't help.

The *worst* case to design C_B is when R_1, R_2 are the smallest (we consider the minimum is tens of $k\Omega$) because C_B would be bigger. An example is reported in Figure 3.20.

In the real case of Noise shaping in Figure 3.20, an interesting parameter to consider to choose C_B is:

$$\alpha = \frac{V_{N,out-integrated,RMS}\Big|_{C_B}}{V_{N,in-integrated,RMS}} \tag{3.38}$$

with $V_{N,in-integrated,RMS}$ is the input integrated Noise in $10Hz - 100kHz$ considering a white input Noise, and $V_{N,out-integrated,RMS}\Big|_{C_B}$ is the integrated Noise at the output, depending on the C_B value.

If C_B is big enough, we should transfer the input Noise to output without amplification and the $\alpha - ratio \approx 1$. From Tab. 3.6 optimal values of C_B are few nF.

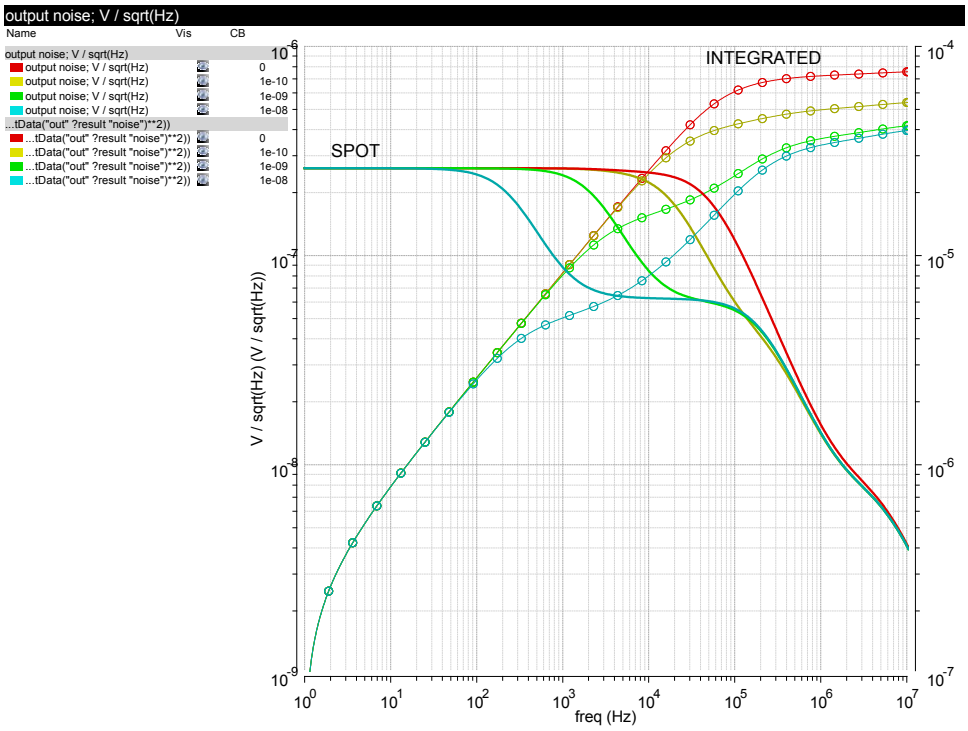

Fig. 3.20: Effect of C_B on the spot and integrated Noise. $V_{i,N}/\sqrt{\Delta f} = 63nV/\sqrt{Hz}$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $I_L = 100mA$

C_B [F]	α
0	3.0
100p	2.1
1n	1.2
10n	1.0

Tab. 3.5: C_B effect, comparison

The connection of C_B also modifies the Loop-Gain (using the circuit depicted in Figure 3.18 and considering $R_o, R_L \ll R_1, R_2$):

$$T(s) \approx A(s)\frac{R_L}{R_o + R_L}\beta_F(s) \tag{3.39}$$

with

$$\beta_F(s) = \left(\frac{R_2}{R_2 + R_1}\right)\left(\frac{1 + sC_BR_1}{1 + sC_B(R_1//R_2}\right) \tag{3.40}$$

The effects on the loop-gain is shown in Figure 3.21 (compare with Figure 3.5).

The Loop-Gain may cut the frequency-axis at a higher frequency depending from the amplitude of $\beta_{F_0} = \frac{R_2}{R_2 + R_1}$, this may lead to instability because parasitic poles are nearest the cutting frequency f_c (above all parasitic poles are around the MHz). This problem is independent from the value of C_B, but depends only from β_{F_0} as depicted in Figure 3.22.

The stability is also checked in Figure 3.23 and Figure 3.24 with a common choice of $C_B = 1nF$ and at the variation of load conditions.

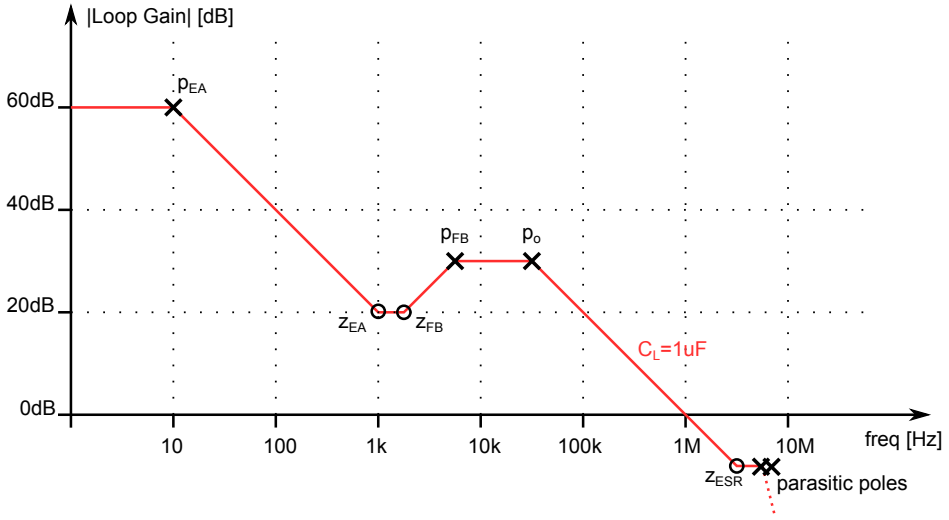

Fig. 3.21: Effect of C_B on the loop gain, theory

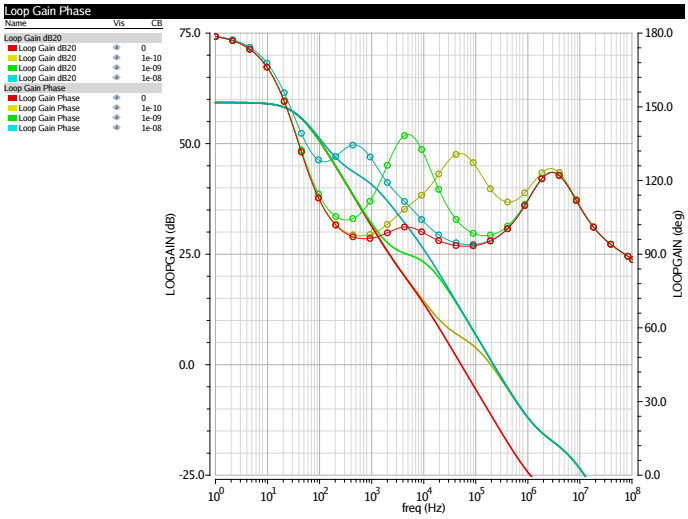

Fig. 3.22: Effect of C_B on the loop gain, simulation

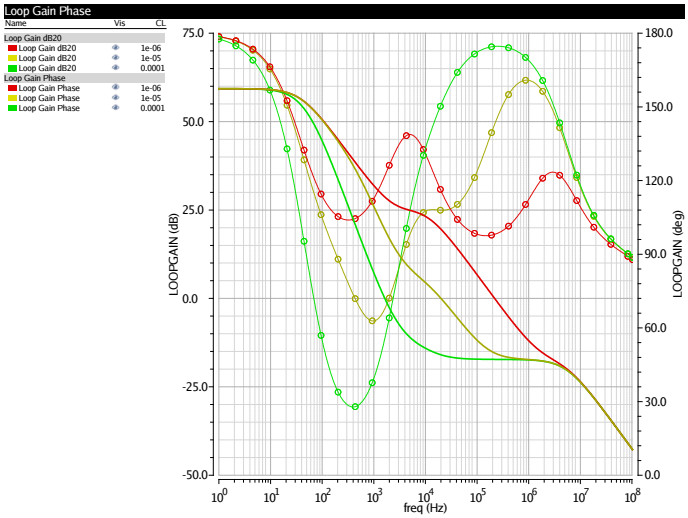

Fig. 3.23: Loop-Gain module and phase, $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 1nF$

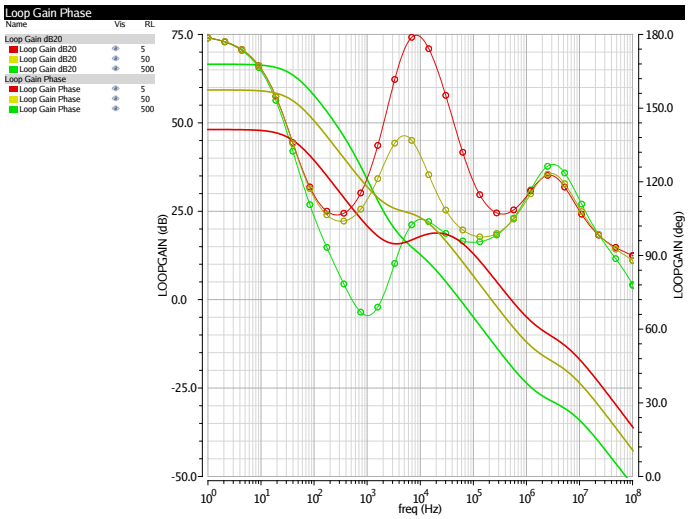

Fig. 3.24: Loop-Gain module and phase, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

3.3.2 Active Feedback

The input to output Noise transfer function is $\frac{1}{\beta_F}$, if we use as feedback a simple voltage divider $\frac{1}{\beta_F} \geq 1$, so at the best we can transfer unitary the input Noise at output. If we use an active feedback with $\beta_F > 1$ at certain frequencies, $\frac{1}{\beta_F} < 1$ so we can reduce the input Noise contribution. For our purpose an appropriate active feedback could be that in Figure 3.25.

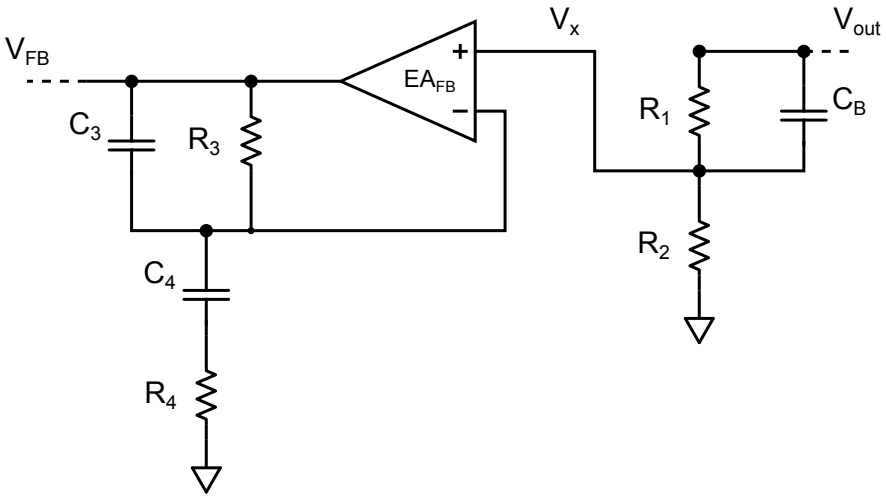

Fig. 3.25: Active Feedback proposed

The first voltage divider $R_1 - R_2$ sets the $\beta_F(0)$, then in the band $1kHz - 100kHz$ the feedback factor is $\beta_F \approx 1 + \frac{R_3}{R_4}$. The complete calculation leads to:

$$\frac{V_x}{V_{out}}(s) = \left(\frac{R_2}{R_2 + R_1}\right)\left(\frac{1 + sC_BR_1}{1 + sC_B(R_1//R_2}\right) \tag{3.41}$$

$$\frac{V_{FB}}{V_x}(s) = 1 + \frac{R_3 // \frac{1}{sC_3}}{R_4 + \frac{1}{sC_4}} \tag{3.42}$$

where in the Eq. 3.42, at DC $\frac{V_{FB}}{V_x}(0) = 1$ and it's the same in high frequency. At intermediate frequency, when C_3 can be considered open and C_4 can be considered a short, $\frac{V_{FB}}{V_x} \approx 1 + \frac{R_3}{R_4}$. If the "gain" band is quite wide there are 2 poles and 2 zeros in the transfer function $\frac{V_{FB}}{V_x}(s)$:

$$f_{z_1} \approx \frac{1}{2\pi R_3 C_4} \tag{3.43}$$

$$f_{z_2} \approx \frac{1}{2\pi R_4 C_3} \tag{3.44}$$

$$f_{p_1} = \frac{1}{2\pi R_4 C_4} \tag{3.45}$$

$$f_{p_2} = \frac{1}{2\pi R_3 C_3} \tag{3.46}$$

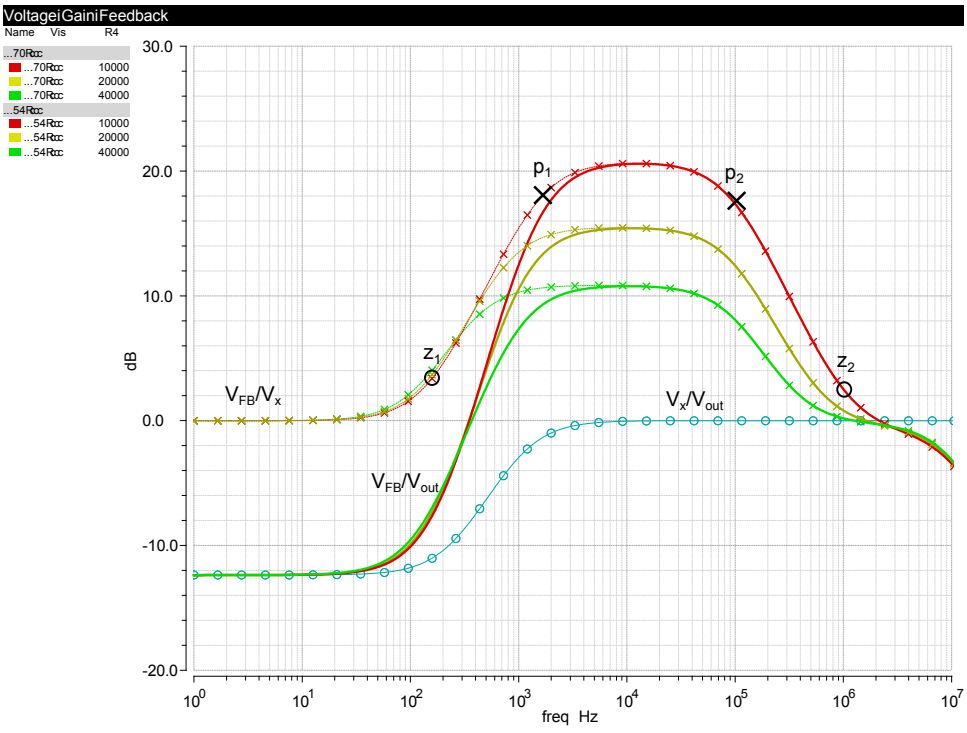

Fig. 3.26: Voltage gain Feedback, $R_3 = 100k\Omega$, $C_3 = 16pF$, $C_4 = 10nF$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $C_B = 1nF$

The total feedback transfer function is $\frac{V_{FB}}{V_{out}}(s) = \frac{V_{FB}}{V_x}(s) \times \frac{V_x}{V_{out}}(s)$, it's shown in Figure 3.26 by varying the gain (at high frequency, up to the *MHz*, the feedback transfer function decreases because the feedback loop-gain has crossing the unitary gain). The general stability of the LDO and that of the feedback loop are studied in Appendix. A.7.

When the feedback gain is $1 + \frac{R_3}{R_4} = 11$ between $1kHz - 100kHz$, the input Noise is decreased of theoretically $\frac{V_{N,out}}{V_{N,in}} = \frac{1}{11}$ (in the hypothesis that input Noise is *white*) as depicted in Figure 3.27.

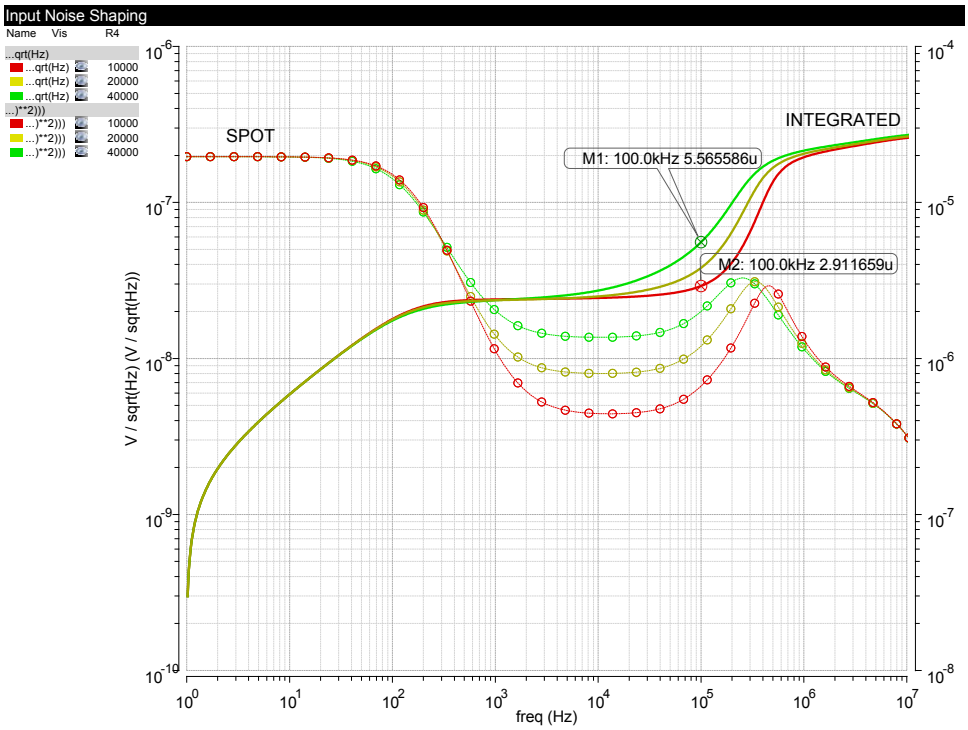

Fig. 3.27: Output Noise due to Input Noise $V_{i,N}/\sqrt{\Delta f} = 48nV/\sqrt{Hz}$, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$

Indeed the reduction is smaller and is summarized by the $\alpha - ratio$.

$$\alpha = \frac{V_{N,out-integrated,RMS}\Big|_{A_{v(FB)}}}{V_{N,in-integrated,RMS}} \tag{3.47}$$

$V_{N,in}$ is considered a white Noise, $A_{v,FB}$ is the feedback gain in the gain band $1kHz - 100kHz$ and the integration band of Eq. 3.47 is $10Hz - 100kHz$.

$A_{v,FB}$	α
11	0.19
6	0.25
3.5	0.37

Tab. 3.6: Feedback gain effect, comparison

However the active feedback generates Noise too, the calculation of R_3, R_4 and $EA(FB)$ Noise is made in Appendix. A.7, and R_1 and R_2 Noise remains the same as Appendix. A.6. All this contributions, if added, they produce the total feedback Noise of Figure 3.28.

So the overall output integrated Noise is:

$$V_{N,out-integrated,RMS}\Big|_{A_{v(FB)}} = \sqrt{V^2_{N,FB-integrated,RMS} + \alpha^2 V^2_{N,in-integrated,RMS}} \tag{3.48}$$

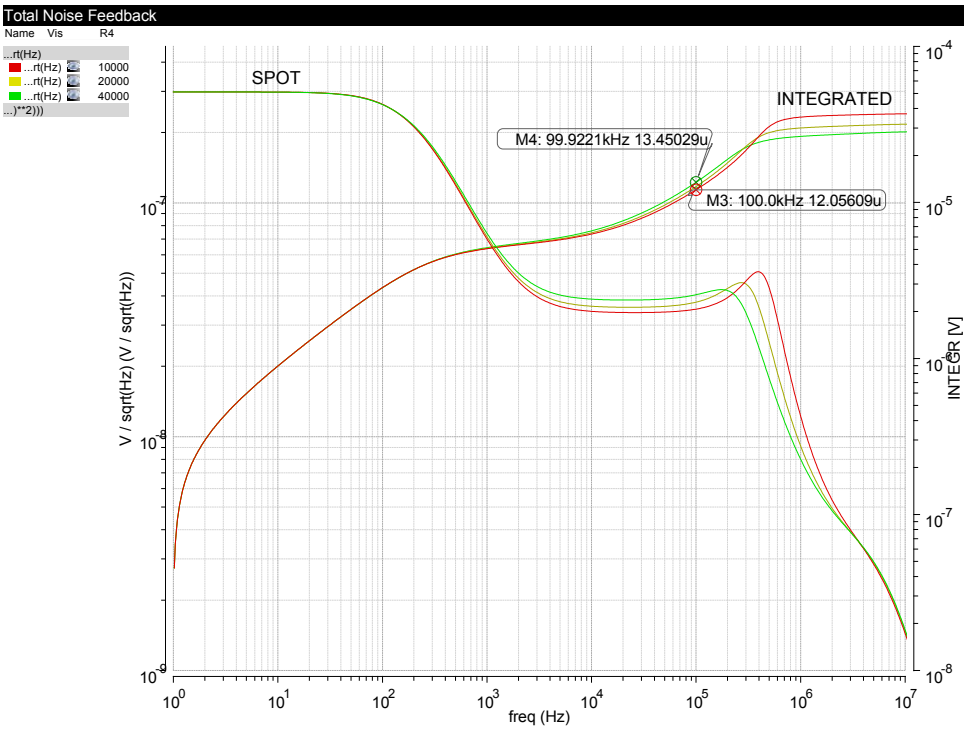

Fig. 3.28: Output Noise due to Active Feedback: $V_{i,N_{EA(FB)}}/\sqrt{\Delta f} = 31.5nV/\sqrt{Hz}$, $R_4 = 10/20/40k\Omega$, $R_3 = 100k\Omega$, $C_3 = 16pF$, $C_4 = 10nF$, $R_1 = 630k\Omega$, $R_2 = 200k\Omega$, $C_B = 1nF$

The very interesting curves to observe it's how vary the Eq. 3.48 at the varying of $V_{N,in-integrated,RMS}$, this is shown in Figure 3.29.

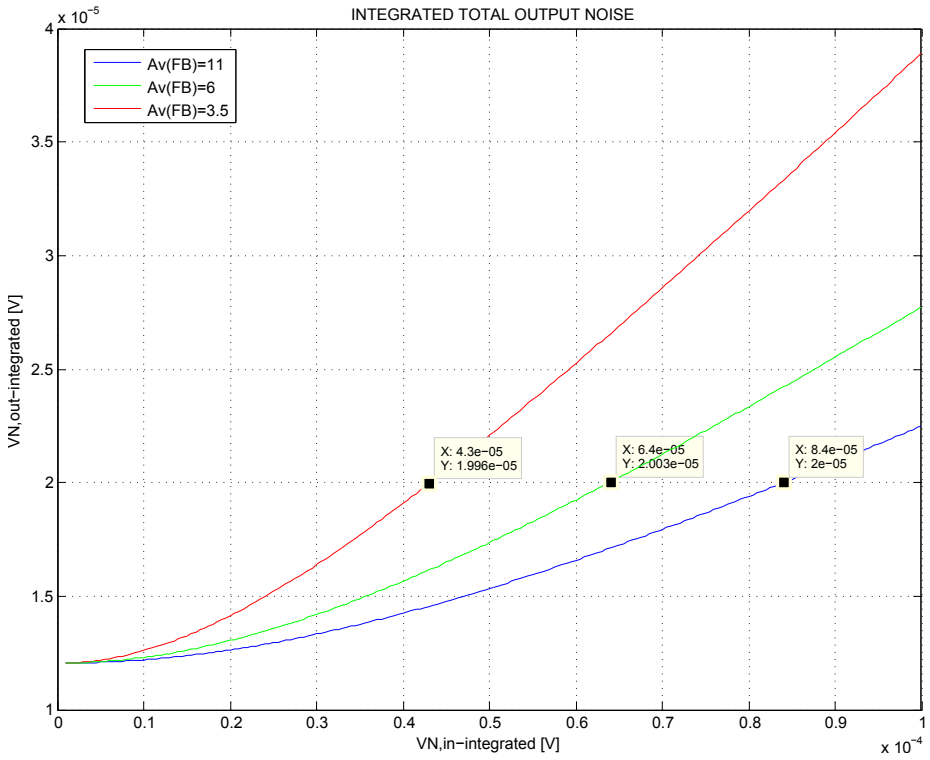

Fig. 3.29: Total output Noise with active feedback, $V_{N,FB-integrated,RMS} = 12\mu V$

The use of an active feedback may be an interesting choice to reduce the input Noise

(the most part is from the reference), the effort is above all to guarantee the stability of the main loop and the requirement of an external C_4 (nF to *tens of* nF) that is not good for a fully integrated regulator.

3.3.3 Output Nested Feedback

In order to decrease at a lower frequency the transfer function $\frac{V_{N,out}}{V_{N,in}}$ we can act on the Loop-Gain, pushing at a very low frequency the dominant pole of the Loop-gain, thus the overall band of the regulator is very poor (the crossing frequency f_c is in low frequency) and output Noise decreases early in frequency.

To set this pole we may use a *Miller* compensation as in Figure 3.30.

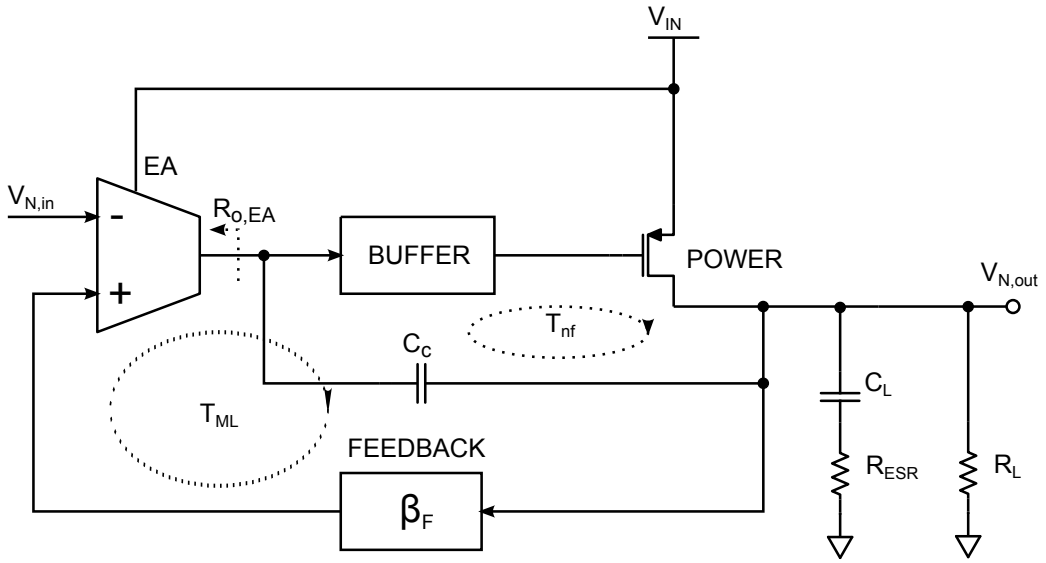

Fig. 3.30: Output nested Loop

The capacitor C_c creates a new negative feedback path (nested loop) that acts as *Miller* compensation of the Error Amplifier, so in this case of compensation, regarding Figure 3.4, C_{EA} and R_z are not needed. Thanks to the *Miller theorem* (Appendix. A.8) at the output node of the Error Amplifier we create a pole at a frequency very low

$$f_{dp} \approx \frac{1}{2\pi\left[\left(C_c A_{v(BUF)} g m_p (R_{o,p}//R_L)\right) R_{o,EA}\right]} \tag{3.49}$$

this is the dominant-pole of the *main* Loop-Gain.

Instead at the output node C_c "seems" to have the same value, since $C_L \gg C_c$ the output pole f_o remains about at the same frequency (Eq. 3.16).

If the nested feedback is a simply capacitor there is also a *feedforward* path from the EA-output to the Regulator-output, this creates a *zero* $\left(1 - s/z\right)$ in the main Loop-Gain, this is a *Positive Real-part* zero so it is bad for stability analysis because it leads to a contribution of $-90°$ in the Loop-gain phase (instead of $+90°$ like a normal zero). This zero is at the frequency:

$$f_z \approx \frac{1}{2\pi \dfrac{C_c}{A_{v(BUF)} g m_p}} \tag{3.50}$$

$A_{v(BUF)} \leq 1$ and gm_p is a very high transconductance because the power-transistor is very big and the output current may be high (gm_p may be hundreds of mS up to S),

so this zero can be pushed in the MHz range where it does not bother (the crossing frequency of the main Loop-gain is much less than MHz).

The main Loop-Gain (T_{ML}), that determines the dynamic of the regulator, can be seen as a *2-poles* system with the poles at f_{dp} and f_o, the zero is at a higher frequency, and if C_c is big enough the Loop-Gain becomes a *1-dominant pole* system (Figure 3.31).

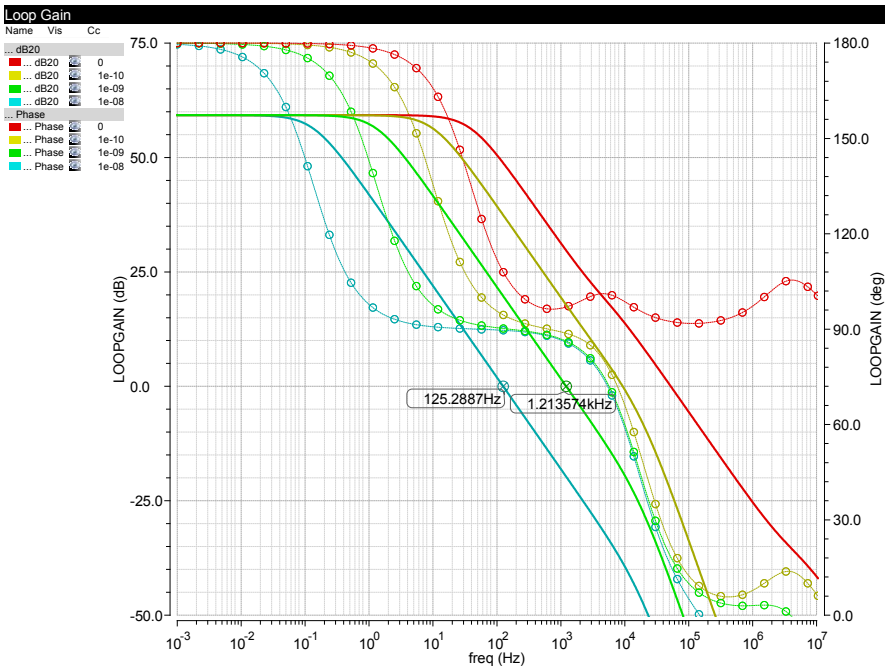

Fig. 3.31: Main Loop-gain, $I_L = 100mA$, $C_L = 1\mu F$, $C_B = 0$

To design a correct value of C_c for our purpose we see the Figure 3.32.

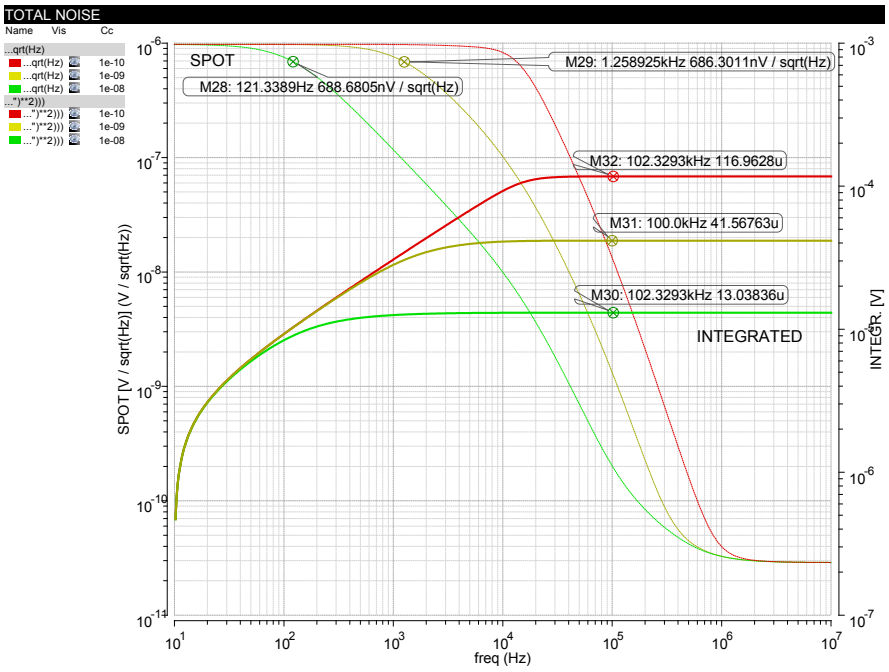

Fig. 3.32: Total output Noise, $I_L = 100mA$, $C_L = 1\mu F$, $V_{N,in}/\sqrt{\Delta f} = 74.2nV/\sqrt{Hz}$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $C_B = 0$

As we can see in Figure 3.32, the transfer function $\frac{V_{N,out}}{V_{N,in}}$ starts to decrease when the main Loop-Gain crosses $0dB$, so at a frequency very small. Even the Noise produced by feedback resistor divider R_1, R_2 starts to fall at this frequency because the Loop stops to regulate. If we increase C_c the Noise can be reduced a lot, the reduction can be summarized by the $\alpha - ratio$.

$$\alpha = \frac{V_{N,out-integrated,RMS}\Big|_{C_c}}{V_{N,in-integrated,RMS}} \tag{3.51}$$

$V_{N,in}$ is considered a white Noise, the integration band of Eq. 3.51 is $10Hz - 100kHz$.

C_c $[F]$	α
100p	1.57
1n	0.56
10n	0.17

Tab. 3.7: C_c Noise reduction effect, comparison

However, R_1 and R_2 Noise can be considerably high if the resistances value is high and C_c is small, the integrated output Noise in $10Hz \leq f \leq 100kHz$ due only to these resistors is reported in Tab. 3.8

	$V_{FB-integrated}$ $[\mu V]$		
C_c [F]	$R_1 = 63k\Omega$, $R_2 = 20k\Omega$	$R_1 = 630k\Omega$, $R_2 = 200k\Omega$	$R_1 = 6.3M\Omega$, $R_2 = 2M\Omega$
100p	7.96	25.17	79.58
1n	2.81	8.88	28.09
10n	0.89	2.78	8.80

Tab. 3.8: Resistor Divider Noise, $C_B = 0$

It's clear that, for example, if we use $C_c = 1nF$ and the resistor divider is particularly high on the order of $M\Omega$, to ensure $V_{N-integr.RMS} \leq 20\mu V$ we have to place a C_B (for example $1nF$) that acts as explained in Par. 3.2.1. The insertion of C_B, however, acts in the Loop-Gain (Par. 3.3.1) and may degrading the stability because the crossing frequency f_c moves to a higher frequency and so the second pole at f_o (output pole Eq. 3.16) has a stronger effect.

The overall integrated output Noise is

$$V_{N,out-integrated,RMS}\Big|_{C_c} = \sqrt{V^2_{N,FB-integrated,RMS} + \alpha^2 V^2_{N,in-integrated,RMS}} \tag{3.52}$$

How vary the $V_{N,out-integrated,RMS}$ at the varying of $V_{N,in-integrated,RMS}$ is shown in Figure 3.33.

So this compensation method can be good for the Noise reduction and a simply C_c is usually not a problem regard the stability, instead for other specifics (over/undershoot etc.) is not a good thing to have a feedforward path, so a buffer in series with C_c (both current or voltage) may be needed to cancel it and to ensure only the feedback path. Anyway, a real buffer produces Noise that increments slightly the total Noise.

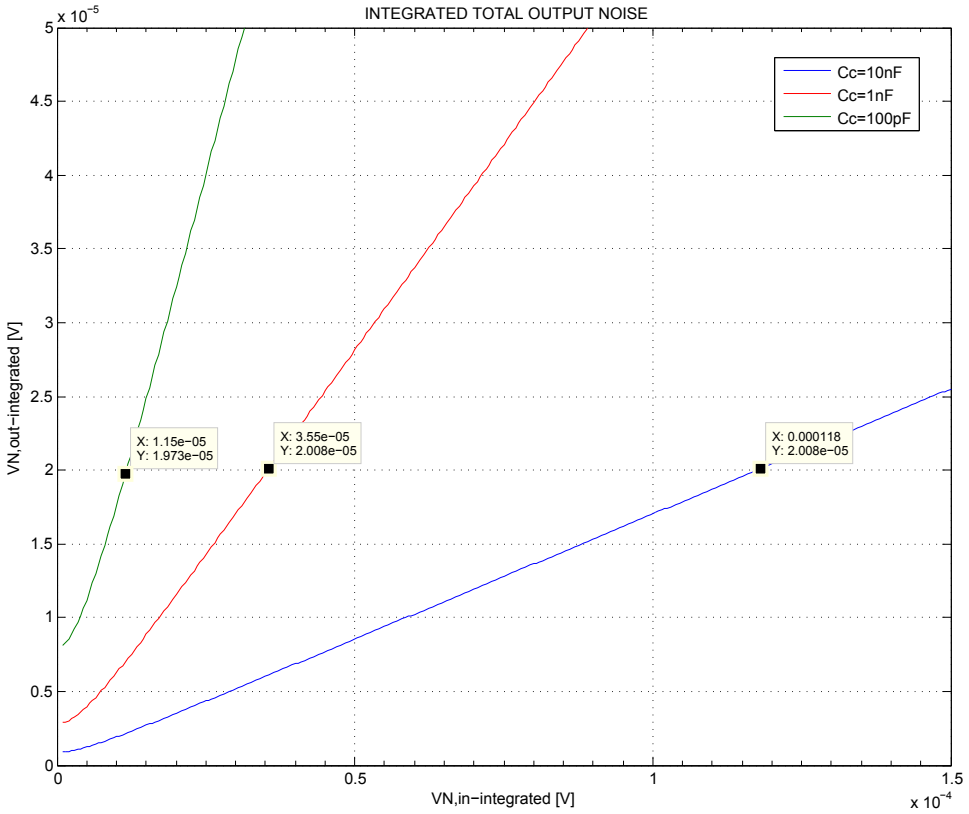

Fig. 3.33: Overall integrated output Noise, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$

3.3.4 Two-Stage Regulator

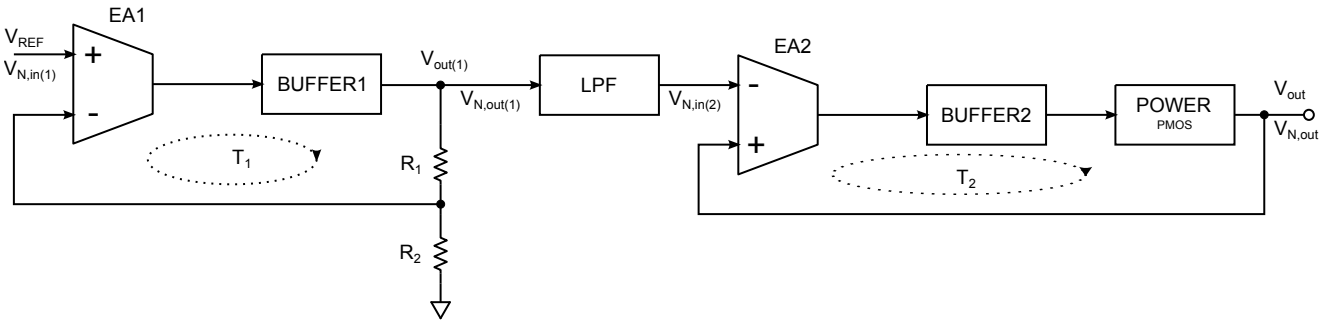

Fig. 3.34: Two-stage Regulator block scheme

This type of regulator works in two steps, the first stage is the *regulation* stage because setting the resistor divider (R_1, R_2) we regulate $V_{out(1)}$ at the correct voltage. The second stage is the *power* stage because it includes the power transistor, it is a loop closed in unitary feedback so it simply regulates $V_{out} = V_{out(1)}$. The block *LPF* between the two stages is a simple R-C *Low Pass Filter* with a very low cut frequency f_{LPF}:

$$f_{LPF} = \frac{1}{2\pi R_x C_x} \tag{3.53}$$

So, since f_{LPF} is very low, the Noise from the first stage (that includes the Noise from the reference) is decreased a lot. Therefore it remains at the output ($V_{N,out}$) only the Noise produced by the second stage ($EA2$) and that of R_x.

First Stage The first stage has to guarantee a fixed voltage $V_{out(1)}$, since the DC current flows into R_1+R_2 is small and is the same that flows through the voltage buffer, the buffer could be a simple *common drain* stage with a relatively small transistor. Thus there are no parasitic poles at medium/low frequency and it is not a problem to guarantee the stability of the Loop (T_1) creating the dominant pole in $EA1$.

The Noise produced by this stage ($Reference/EA1/R_1/R_2$) is then filtered by the low pass filter and it's lead unitary at the output.

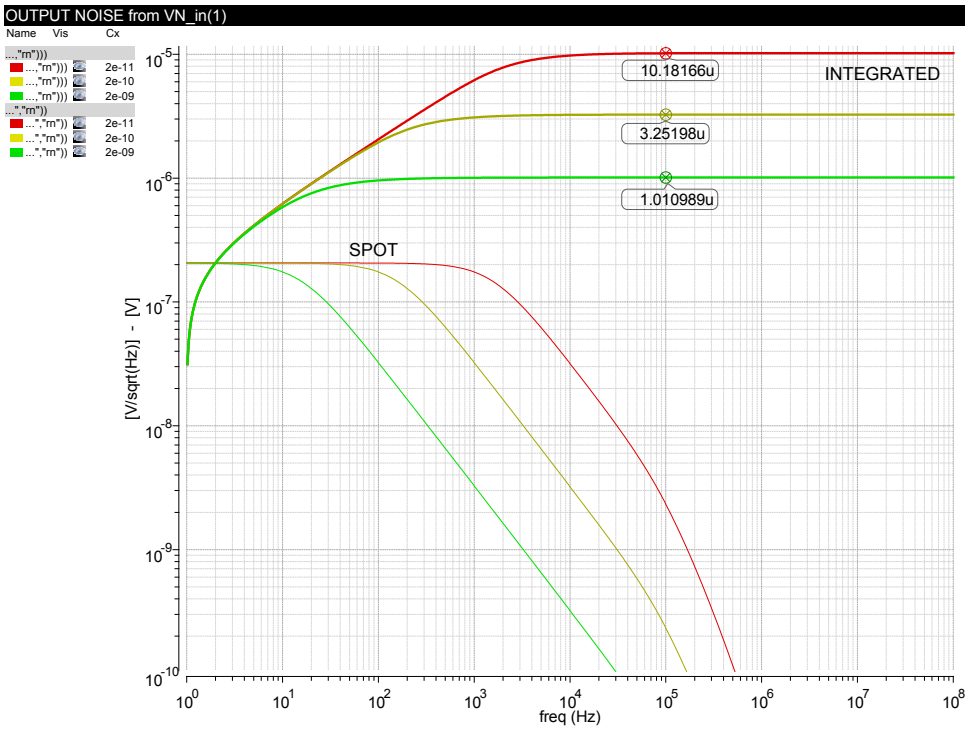

Fig. 3.35: Output Noise from the First Stage, $I_L = 100mA$, $C_L = 1\mu F$, $V_{N,in}/\sqrt{\Delta f} = 50nV/\sqrt{Hz}$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$

The most interesting figure (that not depends from a particular $V_{N,in}/\sqrt{\Delta f}$) is:

$$\alpha = \frac{V_{N,out-integrated,RMS}\Big|_{f_{LPF}}}{V_{N,in-integrated,RMS}} \tag{3.54}$$

$V_{N,in}$ is considered a white Noise, the integration band of Eq. 3.54 is $10Hz - 100kHz$.

f_{LPF} $[Hz]$	α
16	0.06
160	0.21
$1.6k$	0.64

Tab. 3.9: Low-pass filter Noise reduction effect, comparison

Low-pass Filter The LPF could be a simple R-C circuit with a low f_{LPF} (Eq. 3.53), to design for a low cut frequency, R_x and C_x values could be high for an integrated circuit.

Since the $V_{out(1)}$ node is a low-impedance node, the Noise produced by R_x is "totally" injected in the second stage at low frequency and then is shunted to ground by the C_x.

Therefore the transfer function is:

$$\frac{V_{N,out}}{\sqrt{\Delta f}} = \left(\frac{1}{1 + j\dfrac{f}{f_{LPF}}} \right) \frac{V_{N,R_x}}{\sqrt{\Delta f}} \tag{3.55}$$

If the integrated Noise is already "saturated" at $100kHz$, the output Noise depends only by the C_x (see also Eq. 1.42):

$$V_{N,out-RMS} = \sqrt{\frac{kT}{C_x}} \tag{3.56}$$

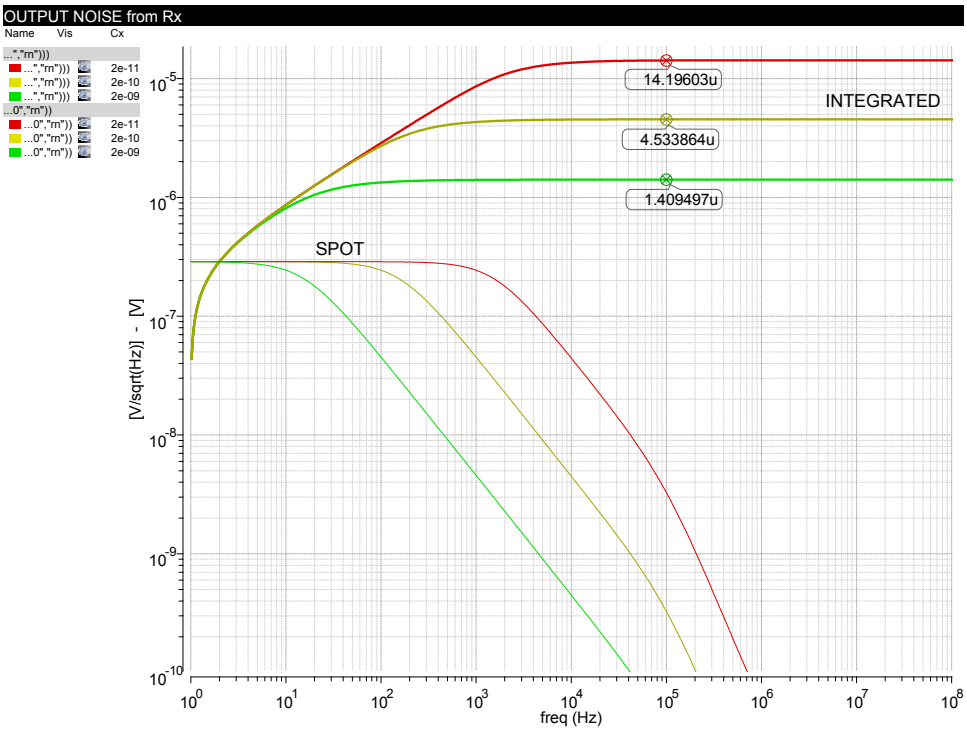

Fig. 3.36: Output Noise from R_x, $I_L = 100mA$, $C_L = 1\mu F$, $R_x = 5M\Omega$

Second Stage The second stage is substantially a complete regulator closed in unitary feedback, so we may ensure the stability of the Loop T_2 with the proposed compensation in Par. 3.1.2, the Loop-gain is depicted in Fig. 3.37.

An aspect to be highlighted is that *EA2* works with a common input voltage $V_{ic} = V_{out(1)} = V_{out}$, so is dependent from the output voltage and thus from $R_1 - R_2$ chosen. If we know V_{out} we can design a suitable OTA (so we chose if its better a *P-type* or *N-type* input couple) instead, if we don't know what will be V_{out}, probably we may design a *Rail-to-Rail OTA* with both *P-type* and *N-type* input couple, this leads to a roughly *double* in the $EA2$ Noise power (so a $\sqrt{2}$ factor in $V_{N(EA2)_{RMS}}$).

The Noise of this stage is about only the Noise of the $EA2$ that we find the same at the output of the regulator (except the reduction effect due to the finite band of the second

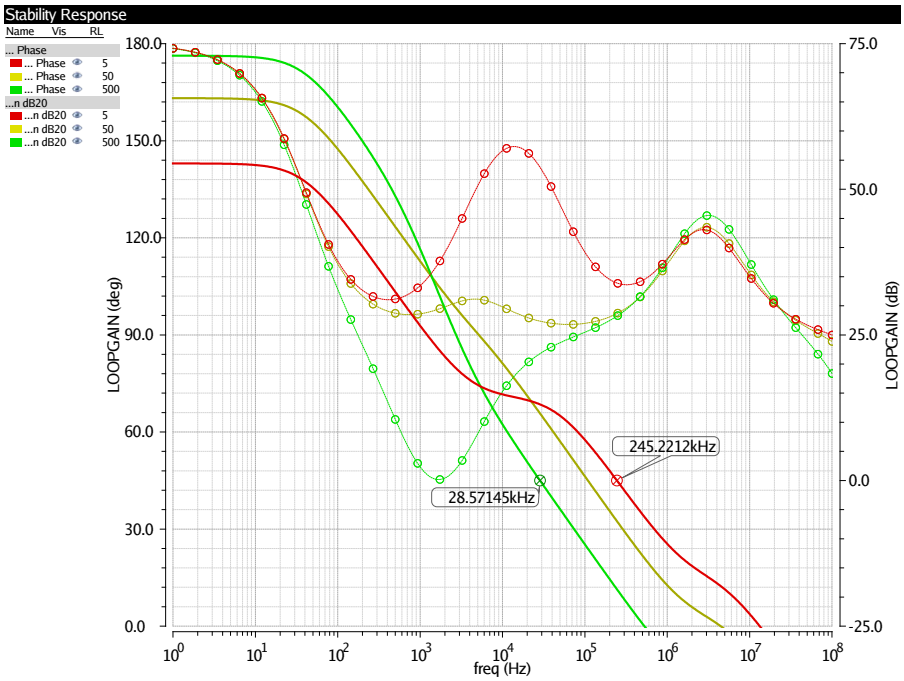

Fig. 3.37: Loop-Gain Power Stage, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$

stage). Thus the total output Noise is:

$$\frac{\overline{V_{N,out}^2}}{\Delta f} \approx \left(\frac{1}{1 + j\frac{f}{f_{LPF}}} \right)^2 \left(\frac{\overline{V_{N,out(1)}^2}}{\Delta f} + \frac{\overline{V_{N,R_x}^2}}{\Delta f} \right) + \frac{\overline{V_{N,EA2}^2}}{\Delta f} \tag{3.57}$$

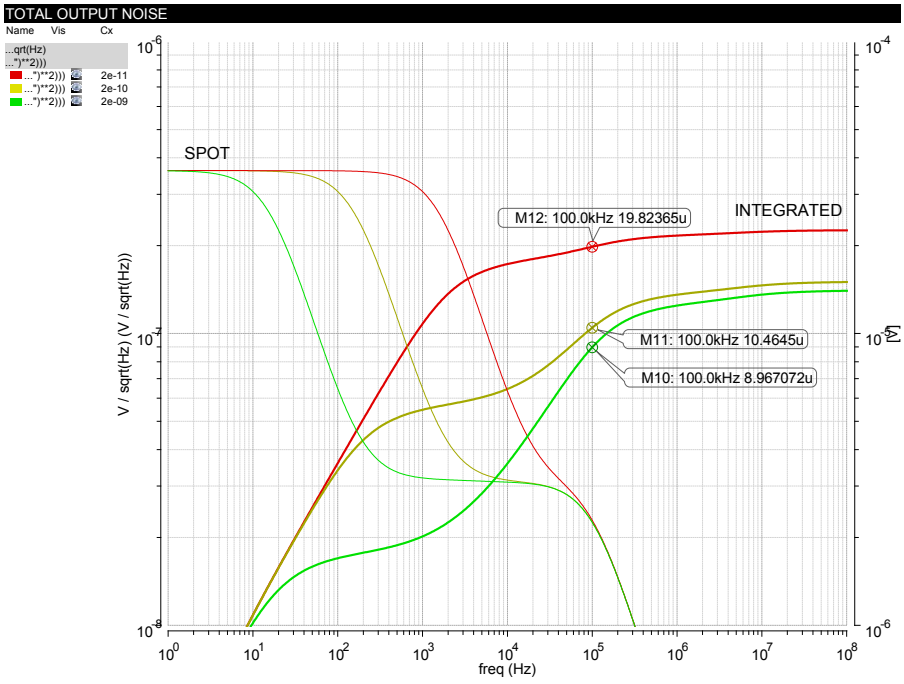

Fig. 3.38: Total output Noise, $I_L = 100mA$, $C_L = 1\mu F$, $R_x = 5M\Omega$, $V_{N,in}/\sqrt{\Delta f} = 50nV/\sqrt{Hz}$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $V_{N,EA2}/\sqrt{\Delta f} = 31.5nV/\sqrt{Hz}$

If we make a good low-Noise design for the $EA2$ and chosen R_x, R_1 and R_2, it's interesting to know the Noise budget for $V_{N,in(1)} \approx V_{N,REF}$, this is depicted in Fig. 3.39.

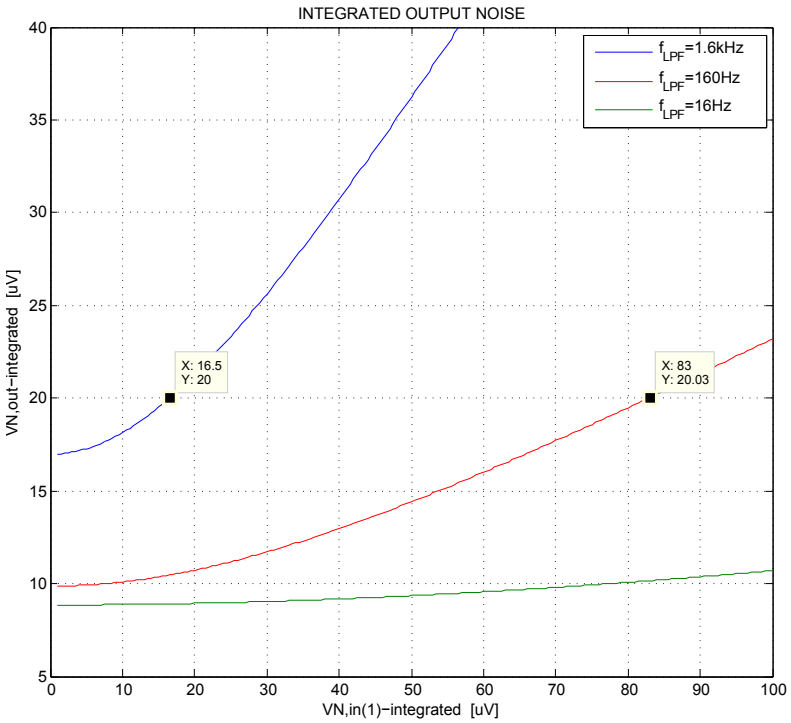

Fig. 3.39: Overall output integrated Noise, $R_x = 5M\Omega$, $V_{N,in(1)_{integrated}} = 15.7\mu V$, $R_1 = 63k\Omega$, $R_2 = 20k\Omega$, $V_{N,EA2_{integrated}} = 10\mu V$

This Two-stage regulator could filter very well the Noise produced by the first stage that is dominated by the Reference Noise, however we should be able to design low-Noise EA2. Another bad requirement is that 2 further *pins*, the input and output nodes of the LPF block, are probably necessary (respect a classical LDO) if we couldn't integrate $R_x - C_x$ in the chip.

3.3.5 Paralleling Regulators

Paralleling Regulators is not a true design method for a low-Noise LDO but it's a way with which it's possible to further reduce the Noise of a single LDO. Paralleling allows a higher $I_{out(max)} = I_{LDO1(max)} + I_{LDO2(max)}$ (in the case of 2 regulators in parallel) and the heat generated is equally distributed between the regulators.

To study the Noise performance of paralleling we consider the case of 2 *identical* LDO in parallel, the AC-circuit that the Noise "sees" is that of Fig. 3.40.

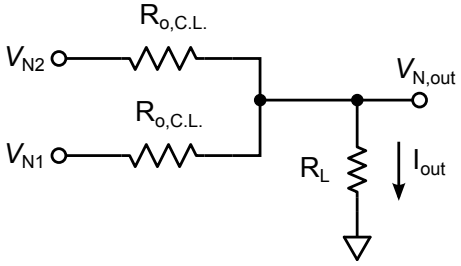

Fig. 3.40: Parallel of 2 Regulators: Noise model

$R_{o(C.L.)}$ is the closed-loop output resistance of the LDO, we consider $R_{o(C.L.)} \ll R_L$

(this is surely true almost in the band of the regulators) so $R_{o(C.L.)}//R_L \approx R_{o(C.L.)}$. In the hypothesis of two identical regulators the $R_{o(C.L.)}$ is the same and $V_{N(1)} = V_{N(2)}$, so applying the superposition of effects:

$$\begin{aligned}\frac{\overline{V_{N,out}^2}}{\Delta f} &= \left(\frac{R_{o(C.L.)}//R_L}{R_{o(C.L.)}//R_L + R_{o(C.L.)}}\right)^2 \frac{\overline{V_{N(1)}^2}}{\Delta f} + \left(\frac{R_{o(C.L.)}//R_L}{R_{o(C.L.)}//R_L + R_{o(C.L.)}}\right)^2 \frac{\overline{V_{N(2)}^2}}{\Delta f} \\ &\approx \left(\frac{1}{2}\right)^2 \frac{\overline{V_{N(1)}^2}}{\Delta f} + \left(\frac{1}{2}\right)^2 \frac{\overline{V_{N(2)}^2}}{\Delta f} \\ &\approx \frac{1}{2}\frac{\overline{V_{N(1)}^2}}{\Delta f}\end{aligned} \tag{3.58}$$

So, since there is a reduction of 2 in the Spot Noise Power (so a $\sqrt{2}$ reduction in Spot Noise Voltage), the Total integrated Noise at the output ($V_{N,out_{RMS}}$) is reduced by a $\sqrt{2}$ factor as shown in Fig. 3.41. In general if we parallel N LDO:

$$V_{N,out_{RMS}}\Big|_{N//-LDO} \approx \frac{1}{\sqrt{N}} V_{N,out_{RMS}}\Big|_{1-LDO} \tag{3.59}$$

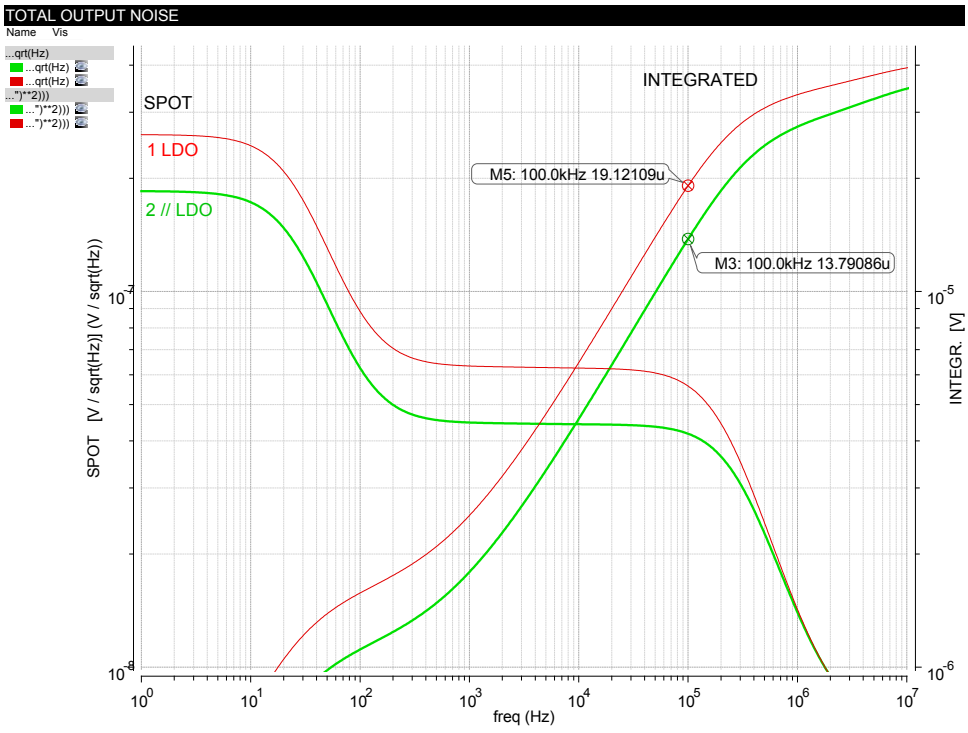

Fig. 3.41: Parallel of 2 Regulators: Total Output Noise

This is an effective technique to have a greater output current and a lower Noise, obviously this is suitable for the customer that can buy more LDOs, from an integrated point of view this technique requires a bigger area (double or in general N times the area of a single LDO) which must be integrated in a single chip.

Chapter 4

Error Amplifier Noise

The *EA* is an important part to design because its Noise is injected at the input of the regulator ad so it "sees" the closed-loop transfer function, the effect due to the Loop is explained in Chapter. 3. The Noise produced by the *EA* is Thermal, Shot and obviously also Flicker, unfortunately in the technology with which I work, Flicker Noise is not modeled, this is not a good notice because we would like to design a Low-Noise OTA. However I could choose both a Bipolar or a MOS Technology, Bipolar is less affected by Flicker Noise or we could use a quite long channel MOS ($L \approx 1 - 10\mu m$) with a quite low corner frequency f_{co}. Conscious of Flicker Noise will increase, we hope slightly, the total Noise, we will take care only of Thermal and Shot Noise analysis.

In this chapter are explained two types of *OTA*, a *Double-stage OTA* and a *Mirrored OTA*, the first one has generally too much voltage gain for our purpose but is very Low-Noise, the second one is a more useful topology for our purpose but its Noise is a little more that the other one. In general, a *Single-Stage OTA* with a simple stage ("5 transistors OTA" or with "Load Resistances") has the *Lowest* Noise, fortunately a *Multi-Stage OTA* can be approximated to a Single-Stage as Noise Performance. Let's show this with an example of a Two-Stage OTA.

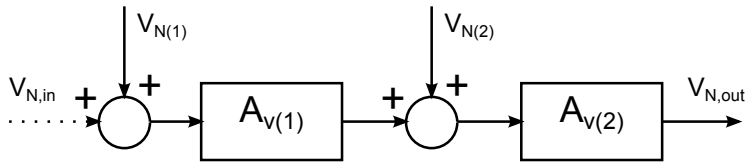

Fig. 4.1: Two-Stage OTA, Noise model

$$\begin{aligned}\frac{\overline{V_{N,out}^2}}{\Delta f} &= A_{v(1)}^2 A_{v(2)}^2 \frac{\overline{V_{N(1)}^2}}{\Delta f} + A_{v(2)}^2 \frac{\overline{V_{N(2)}^2}}{\Delta f} \\ &= A_{v(1)}^2 A_{v(2)}^2 \left(\frac{\overline{V_{N(1)}^2}}{\Delta f} + \left(\frac{1}{A_{v(1)}^2} \right) \frac{\overline{V_{N(2)}^2}}{\Delta f} \right)\end{aligned} \tag{4.1}$$

And if we want to describe the total Noise as an *Equivalent Input* Noise:

$$\frac{\overline{V_{N,out}^2}}{\Delta f} = A_{v(1)}^2 A_{v(2)}^2 \frac{\overline{V_{N,in}^2}}{\Delta f} \tag{4.2}$$

thus equating Eq. 4.2 with Eq. 4.1, it results

$$\begin{aligned}\frac{\overline{V_{N,in}^2}}{\Delta f} &= \frac{\overline{V_{N(1)}^2}}{\Delta f} + \left(\frac{1}{A_{v(1)}^2} \right) \frac{\overline{V_{N(2)}^2}}{\Delta f} \\ &\approx \frac{\overline{V_{N(1)}^2}}{\Delta f}\end{aligned} \tag{4.3}$$

where the approximation in Eq. 4.3 is true if $A_{v(1)} \gg 1$.

4.1 MILLER OTA

The *Miller OTA* is essentially a *Double-Stage OTA* where the compensation uses the *Miller Effect* (Par. A.8).

As we have shown in the previous page, the Noise of a Miller OTA is about that of the first gain stage so this Noise analysis coincides with that of a simply "*5 transistor OTA*". Before entering in the details of the OTA is well to have some concepts on the Noise explained in Appendix. A.9 A.10 A.11.

4.1.1 MOS Input Couple

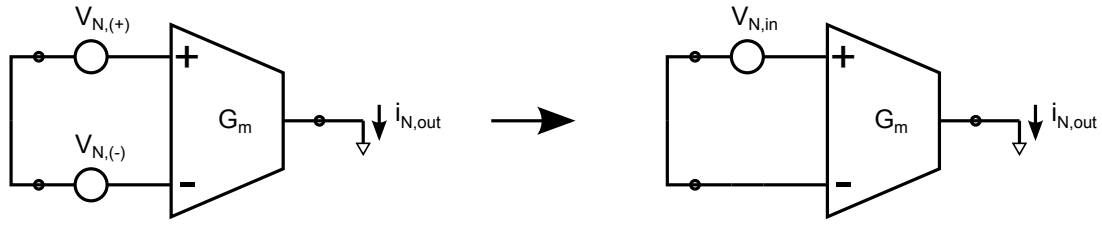

Fig. 4.2: MOS OTA, equivalent input Noise

At both of the two inputs of the OTA is associated an equivalent voltage Noise generator ($v_{N,(+)}$ and $v_{N,(-)}$) that we can add in the more useful $\frac{\overline{v^2_{N,in}}}{\Delta f} = \frac{\overline{v^2_{N,(+)}}}{\Delta f} + \frac{\overline{v^2_{N,(-)}}}{\Delta f}$, so the Noise at the output is $\frac{\overline{i^2_{N,out}}}{\Delta f} = (G_m)^2 \frac{\overline{v^2_{N,in}}}{\Delta f}$. However we are interested at $v_{N,in}$ because it's injected at the input of the total loop of the regulator.

First Stage

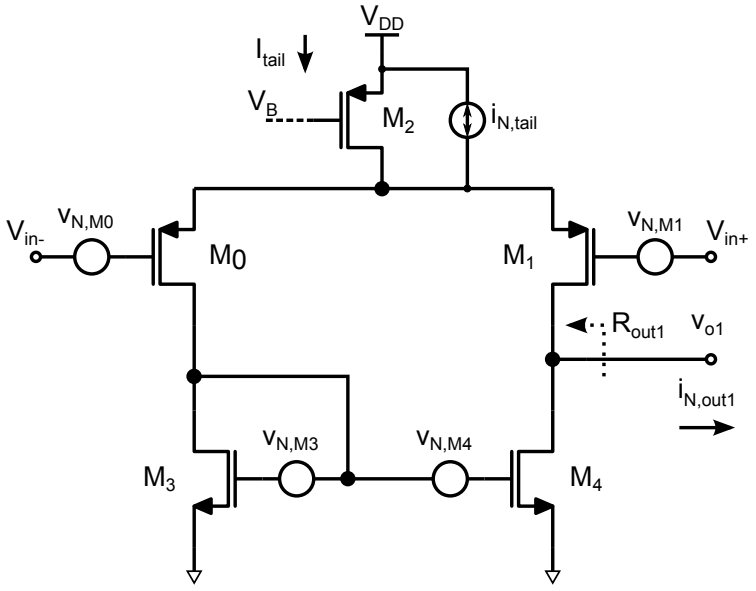

Fig. 4.3: MOS OTA, I Stage with Noise sources

We consider transistors *M0-M1* are matched and also transistors $M3 - M4$, so $g_{m1} =$

g_{m0} and $g_{m3} = g_{m4}$. The voltage gain of the stage is:

$$A_{v_I} = \frac{v_{o1}}{v_{in+} - v_{in-}} = g_{m1} R_{out1} \tag{4.4}$$

where $R_{out1} = R_{o1} // R_{o4}$, and the transconductance of the first stage is g_{m_I}:

$$g_{m_I} = \frac{i_{out1}}{v_{in+} - v_{in-}} = g_{m1} \tag{4.5}$$

With the hypothesis made on the matching of transistors, it's simple to calculate the $i_{N,out1}$:

$$\frac{\overline{i^2_{N,out1}}}{\Delta f} = (g_{m1})^2 \left(\frac{\overline{v^2_{N,M0}}}{\Delta f} + \frac{\overline{v^2_{N,M1}}}{\Delta f} \right) + (g_{m4})^2 \left(\frac{\overline{v^2_{N,M3}}}{\Delta f} + \frac{\overline{v^2_{N,M4}}}{\Delta f} \right) \tag{4.6}$$

where $\dfrac{\overline{v^2_{N,Mx}}}{\Delta f}$ are those of Eq. A.27.

In Eq. 4.6 there isn't the effect of $i_{N,tail}$ because a current (or voltage) signal injected in that node of the circuit is a *common mode signal* so, if the OTA has a high enough CMRR (*Common Mode Rejection Ratio*), this does not produce a *differential signal* at the output (Figure 4.4 helps to understand this concept).

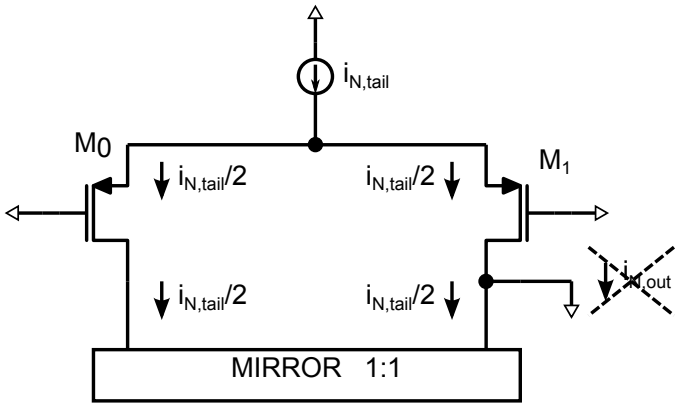

Fig. 4.4: I_{tail} Noise propagation

Now if we divide Eq. 4.6 by the square of the transconductance of the stage $g^2_{m_I}$, we find the equivalent input voltage Noise $v_{N,in}$:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} = \frac{\overline{v^2_{N,M0}}}{\Delta f} + \frac{\overline{v^2_{N,M1}}}{\Delta f} + \left(\frac{g_{m4}}{g_{m1}} \right)^2 \left(\frac{\overline{v^2_{N,M3}}}{\Delta f} + \frac{\overline{v^2_{N,M4}}}{\Delta f} \right) \tag{4.7}$$

And since $v_{N,M0} = v_{N,M1}$ and $v_{N,M3} = v_{N,M4}$ (with the symmetry and matching hypothesis), Eq. 4.7 reduces to:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} = \frac{16}{3} kT \left(\frac{1}{g_{m1}} + \frac{g_{m4}}{(g_{m1})^2} \right) = \frac{16}{3} kT \frac{1}{g_{m1}} \left(1 + \frac{g_{m4}}{g_{m1}} \right) \tag{4.8}$$

We note from Eq. 4.8 that the Noise depends only on the transconductances g_{m1}, g_{m4} (at a first analysis but with a good approximation). The best case would be if it was negligible the term g_{m4}/g_{m1}, so all the Noise, the *minimum Noise*, would be:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} \approx \frac{16}{3} kT \frac{1}{g_{m1}} \tag{4.9}$$

that is only the Noise due to the input couple $M0 - M1$.

In general the term g_{m4}/g_{m1} is not small and the current mirror $M3 - M4$ produces a non negligible Noise, how we could design transistors to make $g_{m4}/g_{m1} \ll 1$?

The transconductance of a MOS is $g_m = \sqrt{2I_D\mu C_{ox}(W/L)}$ (important is to observe that electrons mobility is higher that that of holes, $\mu_n \approx 3\mu_p$) so:

$$\begin{aligned} \frac{g_{m4}}{g_{m1}} &\ll 1 \\ \frac{g_{m1}}{g_{m4}} &\gg 1 \\ \sqrt{\frac{2I_{D1}\mu_p C_{ox}(W/L)_1}{2I_{D4}\mu_n C_{ox}(W/L)_4}} &\gg 1 \end{aligned}$$

and therefore

$$\frac{g_{m1}}{g_{m4}} \approx \sqrt{\frac{(W/L)_1}{3(W/L)_4}} \tag{4.10}$$

It's difficult to make $\frac{g_{m1}}{g_{m4}} \gg 1$ because of the square root and the factor "3", to make $\frac{g_{m1}}{g_{m4}} = 10$ it would be $(W/L)_1 \approx 300(W/L)_4$, this is probably a too high value that makes too big $M0 - M1$. Note that we are considering a *PMOS* input couple because generally the reference voltage, that is the common mode input voltage ($V_{in,cm} = V_{REF}$), is a low voltage (generally $V_{REF} \approx 1.2V$), so the factor "3" has a negative effect. If we have a *NMOS* input couple with the *PMOS* current mirror, the "3" coefficient helps us and it would be $(W/L)_1 \approx 33(W/L)_4$ that is a not so high value.

Another method to reduce g_{m4} is to degenerate the current mirror $M3-M4$, this effect is explained in Par. A.11, obviously we couldn't degenerate so much because an increase of the $R_{deg.} \uparrow$ decreases the output *swing* of the stage.

Finally, to strongly decrease $v_{N,in} \downarrow$ we have to increase $g_{m1} \uparrow$, how predicts Eq. 4.8 and Eq. 4.9. Since $g_{m1} \propto \sqrt{I_{D1}} \propto \sqrt{I_{tail}}$ and $g_{m1} \propto \sqrt{(W/L)_1}$ we may increase the current $I_{tail} \uparrow$ or we may increase the body factor $(W/L)_1 \uparrow$. If we increase very much the body factor $(W/L)_1 \uparrow\uparrow$ (so $V_{GS} - V_{th} = V_{ov} \leq 0$) we lead the MOS to operate in the *weak-inversion* region where

$$I_D \propto e^{\left(\frac{V_{ov}}{nV_T}\right)}$$

$n \approx 1 - 2$ is the *ideality coefficient* and $V_T = kT/q$ is the *thermal voltage*, so

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \propto \frac{I_D}{nV_T} \tag{4.11}$$

Thus in *weak-inversion* the MOS has a higher transconductance $g_m \propto I_D$ (like a Bipolar transistor) that may considerably decreases $v_{N,in}$.

Flicker Noise We already said that Flicker Noise is not modeled in the technology with which I work, anyway we can derive some useful design rules from the theory. Flicker Noise sources can be described exactly as those of Figure 4.3 where $v_{N,Mx(1/f)}$ are those

of Eq. A.29, so $v_{N,in(1/f)}$ has the same expression of Eq. 4.7. After the substitution of $v_{N,Mx(1/f)}$ we find:

$$\frac{\overline{v^2_{N,in(1/f)}}}{\Delta f} = 2\frac{B_p}{W_1 L_1}\frac{1}{f}\left(1+\left(\frac{K'_n B_n}{K'_p B_p}\right)\left(\frac{L_1}{L_4}\right)^2\right) \tag{4.12}$$

where $K'_{n/p} = \mu_{n/p} C_{ox}$. So we can make $L_1 \ll L_4$ to make negligible the contribution of the current mirror $M3 - M4$ (note that $K'_n B_n > K'_p B_p$), and then to reduce the contribution of the input couple $M0 - M1$ we can make a big area $W_1 L_1$.

As the last thing, if we know the Flicker parameters of the technology, we could calculate the *corner frequency* f_c by equating:

$$\frac{16}{3}kT\frac{1}{g_{m1}} = 2\frac{B_p}{W_1 L_1}\frac{1}{f_c}$$

therefore

$$f_c = \frac{3 g_{m1} B_p}{8 k T W_1 L_1} \tag{4.13}$$

Second Stage

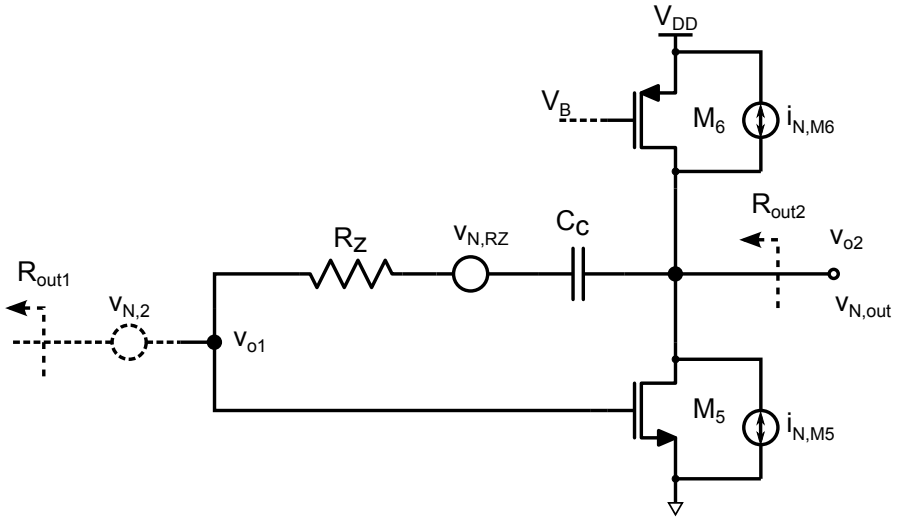

Fig. 4.5: II Stage Miller OTA with Noise sources

The second stage is a simple gain stage with a voltage gain (at low frequency):

$$A_{v_{II}} = \frac{v_{o2}}{v_{o1}} = g_{m5} R_{out2} \tag{4.14}$$

with $R_{out2} = R_{o5} // R_{o6}$. C_c is used to create the dominant pole at low frequency $f_{dp} = \dfrac{1}{2\pi R_{out1} C_c g_{m5} R_{out2}}$ and R_z to create the zero at $f_z = \dfrac{1}{2\pi C_c (R_z - 1/g_{m5})}$, so the overall voltage gain has the correct shape as in Figure 3.5, at low-medium frequency it is:

$$A_{v_{tot}} = g_{m1} R_{out1} g_{m5} R_{out2} \frac{\left(1+\dfrac{s}{2\pi f_z}\right)}{\left(1+\dfrac{s}{2\pi f_{dp}}\right)} \tag{4.15}$$

Remember that A_{v_I} has the form:

$$A_{v_I} = g_{m1} R_{out1} \frac{\left(1 + \frac{s}{2\pi f_z}\right)}{\left(1 + \frac{s}{2\pi f_{dp}}\right)} \tag{4.16}$$

so the shaping is as depicted in the example of Figure 4.6 (it is shown A_{v_I} by varying the position of the zero, so the value of R_z).

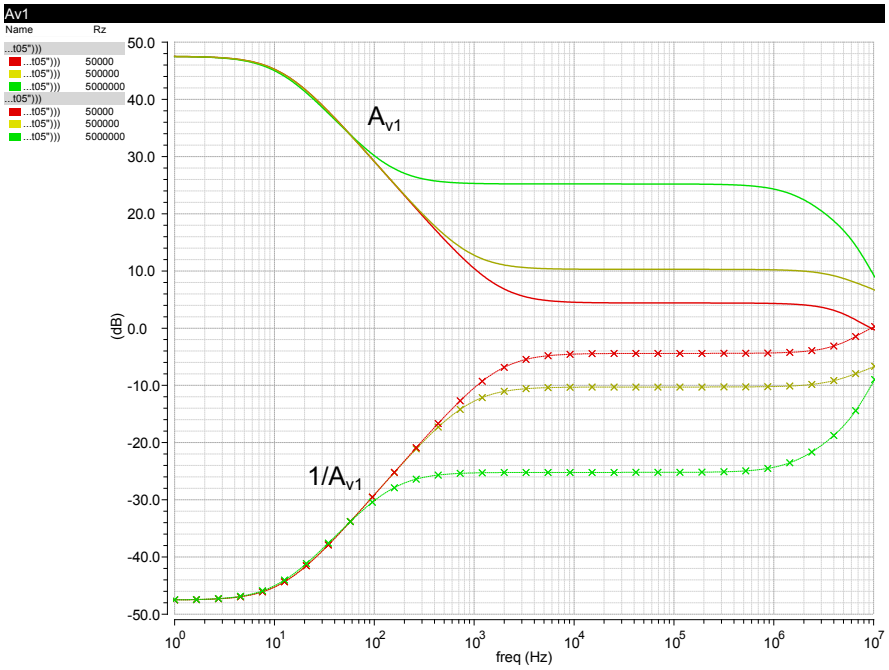

Fig. 4.6: A_{v_I}

The Noise of the second stage can be replaced by its equivalent input Noise voltage $v_{N,2}$, it's not very important to calculate the exact relation with the true Noise sources v_{N,R_z}, $i_{N,M6}$, $i_{N,M5}$, because at the input of the OTA we have an equivalent Noise:

$$\frac{\overline{v_{N,in}^2}}{\Delta f} = \frac{1}{A_{v_I}^2} \frac{\overline{v_{N,2}^2}}{\Delta f} \tag{4.17}$$

and it is very small and negligible as long as $A_{v_I} \gg 1$, but it may increase with the shaping of $1/A_{v_I}$ (see Figure 4.7 and Figure 4.6).

The total equivalent input Noise is:

$$\frac{\overline{v_{N,in(tot)}^2}}{\Delta f} = \frac{\overline{v_{N,1}^2}}{\Delta f} + \frac{1}{A_{v_I}^2} \frac{\overline{v_{N,2}^2}}{\Delta f} \tag{4.18}$$

where $v_{N,1}$ is that of Eq. 4.8. The total input Noise is $\frac{\overline{v_{N,in(tot)}^2}}{\Delta f} \approx \frac{\overline{v_{N,1}^2}}{\Delta f}$ as long as $A_{v_I} \gg 1$, and it may slightly increases at medium-high frequencies because of $v_{N,2}$ increases (see the effect comparing Figure 4.7 and Figure 4.8). However this increase is very slightly at a frequency $f \leq 100kHz$.

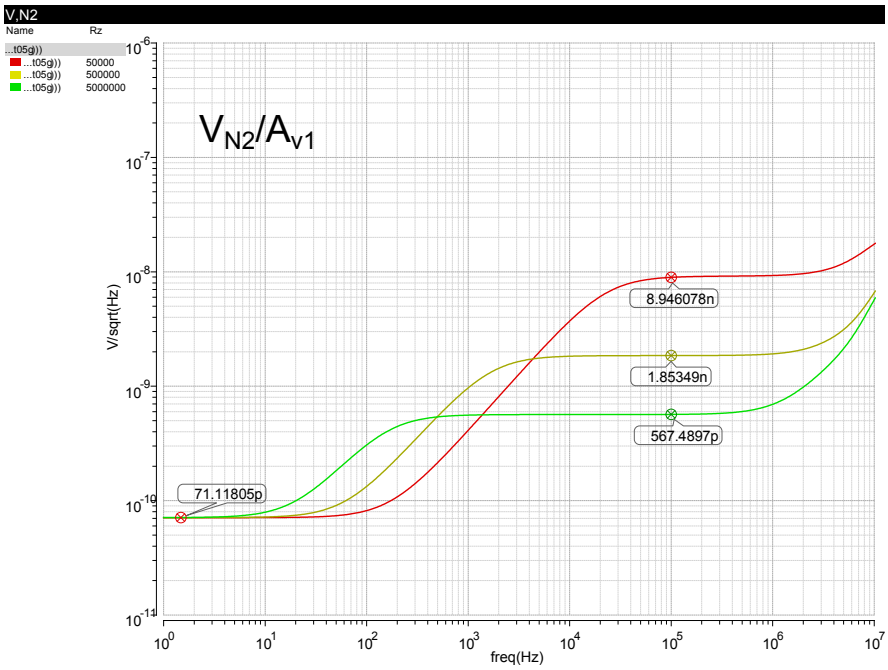

Fig. 4.7: $\frac{v_{N,2}}{\sqrt{\Delta f}}/A_{v_I}$

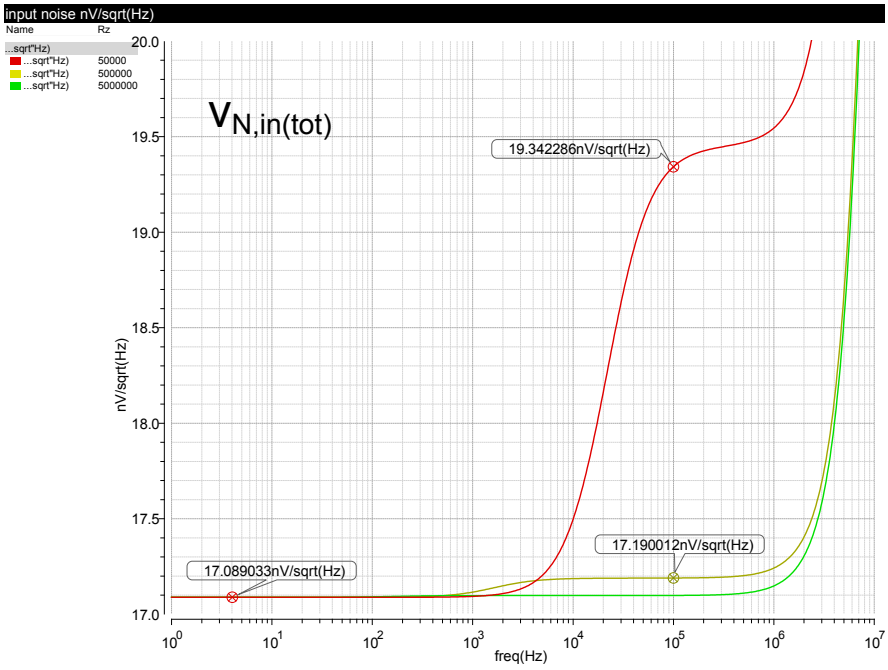

Fig. 4.8: Effect of $v_{N,2}$ on $v_{N,in(tot)}$

4.1.2 Bipolar Input Couple

An OTA with a Bipolar input couple presents (as an OTA with MOS) an equivalent input voltage Noise generator $v_{N,in}$ and an input current Noise generator $i_{N,in+/-}$ for each input (see Figure 4.9). We can add the various sources in an equivalent and total voltage Noise

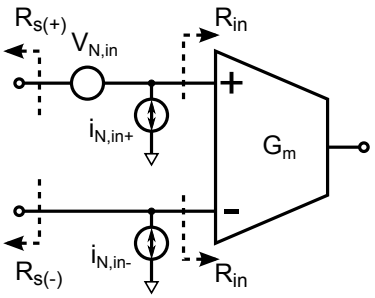

Fig. 4.9: MOS BJT, equivalent input Noise

source $v_{N,in(tot)}$:

$$\frac{\overline{v^2_{N,in(tot)}}}{\Delta f} = \frac{\overline{v^2_{N,in}}}{\Delta f} + (R_{s(+)}//R_{in})^2 \frac{\overline{i^2_{N,in+}}}{\Delta f} + (R_{s(-)}//R_{in})^2 \frac{\overline{i^2_{N,in-}}}{\Delta f} \tag{4.19}$$

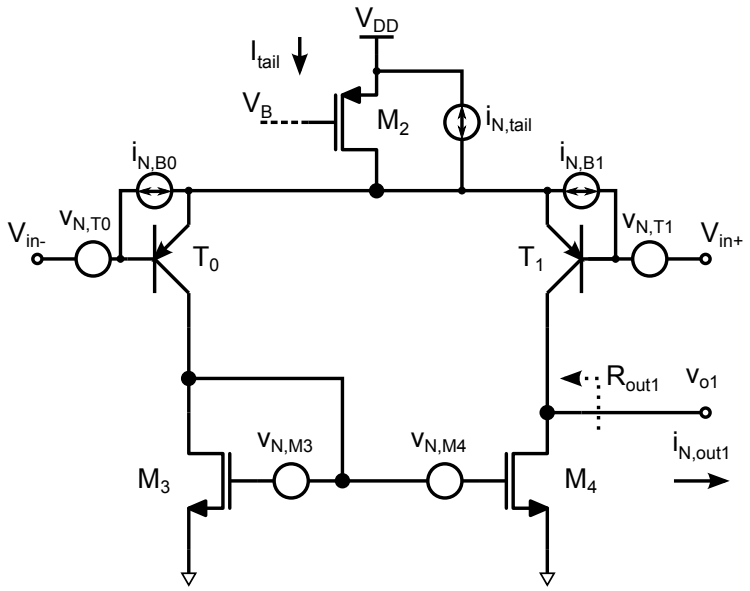

Fig. 4.10: MOS BJT, I Stage with Noise sources

Input Voltage Noise

As regard $v_{N,in}$, it derives from the contribute of $v_{N,T0}$, $v_{N,T1}$, $v_{N,M4}$, $v_{N,M3}$:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} = \frac{\overline{v^2_{N,T0}}}{\Delta f} + \frac{\overline{v^2_{N,T1}}}{\Delta f} + \left(\frac{g_{m4}}{g_{m1}}\right)^2 \left(\frac{\overline{v^2_{N,M3}}}{\Delta f} + \frac{\overline{v^2_{N,M4}}}{\Delta f}\right) \tag{4.20}$$

and since $v_{N,T0} = v_{N,T1}$ and $v_{N,M3} = v_{N,M4}$ (with the symmetry and matching hypothesis), $v_{N,Tx}$ is that of Eq. A.31 and $v_{N,Mx}$ is that of Eq. A.27. After the substitutions Eq. 4.20 reduces to:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} = 4kT \frac{1}{g_{m1}} \left(1 + \frac{4}{3}\frac{g_{m4}}{g_{m1}}\right) \tag{4.21}$$

Remember that $g_{m4} = \sqrt{2I_{D4}\mu_n C_{ox}(W/L)_4}$ and $g_{m1} = I_{C1}/V_T$ ($I_{C1} = I_{D4} = I_{tail}/2$), so to make negligible the second term in Eq. 4.21:

$$\frac{g_{m4}}{g_{m1}} \propto \frac{1}{\sqrt{I_{tail}}}$$

we can increase the current $I_{tail} \uparrow$, or we could decrease $g_{m4} \downarrow$ decreasing $(W/L)_4 \downarrow$ or degenerating the current mirror $M3-M4$ as explained in Par. A.11. However with BJT as input transistors it's easier to guarantee $\frac{g_{m4}}{g_{m1}} \ll 1$ because generally $g_{m(BJT)} \gg g_{m(MOS)}$. The best choice to reduce Noise of Eq. 4.21 is, anyway, increasing the I_{tail} because the limit of $v_{N,in}$ is the Noise produced by the input couple $T0-T1$, so to increase $g_{m1} \uparrow$ we can only increasing the $I_{tail} \uparrow$:

$$\frac{\overline{v_{N,in}^2}}{\Delta f} \approx 4kT\frac{1}{g_{m1}} = 8qV_T^2\frac{1}{I_{tail}} \tag{4.22}$$

Flicker Noise Flicker Noise may be neglected in some Bipolar technologies, but it is not so for MOS transistors, thus $M3-M4$ produce some $1/f-$Noise. The equivalent input Noise voltage is (consider $v_{N,M3(1/f)} = v_{N,M4(1/f)}$):

$$\frac{\overline{v_{N,in(1/f)}^2}}{\Delta f} = \frac{1}{g_{m1}^2}\left(2\frac{K_f I_{D4}}{L_4^2 C_{ox}}\frac{1}{f}\right) \tag{4.23}$$

so the only way to reduce it, it's increasing $g_{m1} \uparrow$ and using transistors with a long channel $L \uparrow$.

A theoretical *corner frequency* f_c may be calculated equating PSDs of Eq. 4.22 and Eq. 4.23 and it results:

$$f_c = \frac{K_f}{2qC_{ox}L_4^2} \tag{4.24}$$

so it may be pushed to a lower frequency increasing $L \uparrow$.

Input Current Noise

The input Noise current generator $i_{N,B1}$ see a low-degenerated CE stage (the same is for $i_{N,B0}$), low-degenerated because the resistance seen from the emitter of $T1$ is $R_{o,tail}//\frac{1}{g_{m0}} \approx \frac{1}{g_{m0}}$, so $g_{m1}\left(\frac{1}{g_{m0}}\right) \approx 1$ is not a so high value. Thus, as we say in Par. A.10.1, we may assume $i_{N,in+/-} \approx i_{N,B1/0}$ and the effect on the input voltage Noise is:

$$\frac{\overline{v_{N,in(I_B)}^2}}{\Delta f} = (R_{s(+)}//R_{in})^2\frac{\overline{i_{N,in+}^2}}{\Delta f} + (R_{s(-)}//R_{in})^2\frac{\overline{i_{N,in-}^2}}{\Delta f} \tag{4.25}$$

so the influence of Eq. 4.25 on Eq. 4.19 may be very different in dependence from the value of the resistances. $R_{in} \approx 2r_\pi$ (since there is a low-degeneration) so is some hundreds of $k\Omega$ or few $M\Omega$, let's try to know what are $R_{s(+)}$ and $R_{s(-)}$.

The error amplifier is connected to the rest of the circuit as in Figure 3.1, the feedback network includes the voltage divider $R_1 - R_2$ and the bypass capacitor C_B as in Figure 3.18. $R_{s(-)} = R_{out(REF.)}$ and it may vary in dependence with the used topology for the voltage reference. However, if it's necessary, we can reduce the $R_{out(REF.)}$ at medium-high frequency with the insertion of a capacitor $C_{out(REF.)}$ in parallel, that reduces this impedance $R_{out(REF.)}//\left(\frac{1}{sC_{out(REF.)}}\right)$. So $(R_{s(-)}//R_{in})^2\frac{\overline{i_{N,in-}^2}}{\Delta f}$ is not a very important

contribution (it must be verified), otherwise, $(R_{s(+)}//R_{in})^2\frac{\overline{i^2_{N,in+}}}{\Delta f}$ may be a serious problem that may increase strongly and dominate Eq. 4.19. If there is not the C_B in the feedback network, $R_{s(+)} = R_1//R_2$, since R_1 and R_2 are generally very big resistances (hundreds of $k\Omega$ to few $M\Omega$) the total resistance $R_{in}//R_1//R_2$ is still very high and even the small noise source $i_{N,in+}$ can produce high voltage fluctuations. Fortunately, the insertion of C_B in parallel to R_1 (as in Figure 3.18, note that the two inputs are exchanged respect Figure 3.1) modifies the impedance:

$$Z_{s(+)}(s) = \frac{R_1//R_2}{1 + s[(R_1//R_2)C_B]} \tag{4.26}$$

therefore the total impedance decreases at medium-high frequencies like $R_{in}//Z_{s(+)}(s) \approx \frac{1}{sC_B}$ and the Noise voltage produced by $i_{N,in}$ becomes negligible.

In conclusion, if the input couple is in Bipolar technology, to reach low-noise performance we have to assure at medium-high frequencies a low $Z_{out(REF.)}$ and the bypass capacitor C_B is needed.

4.2 MIRRORED OTA

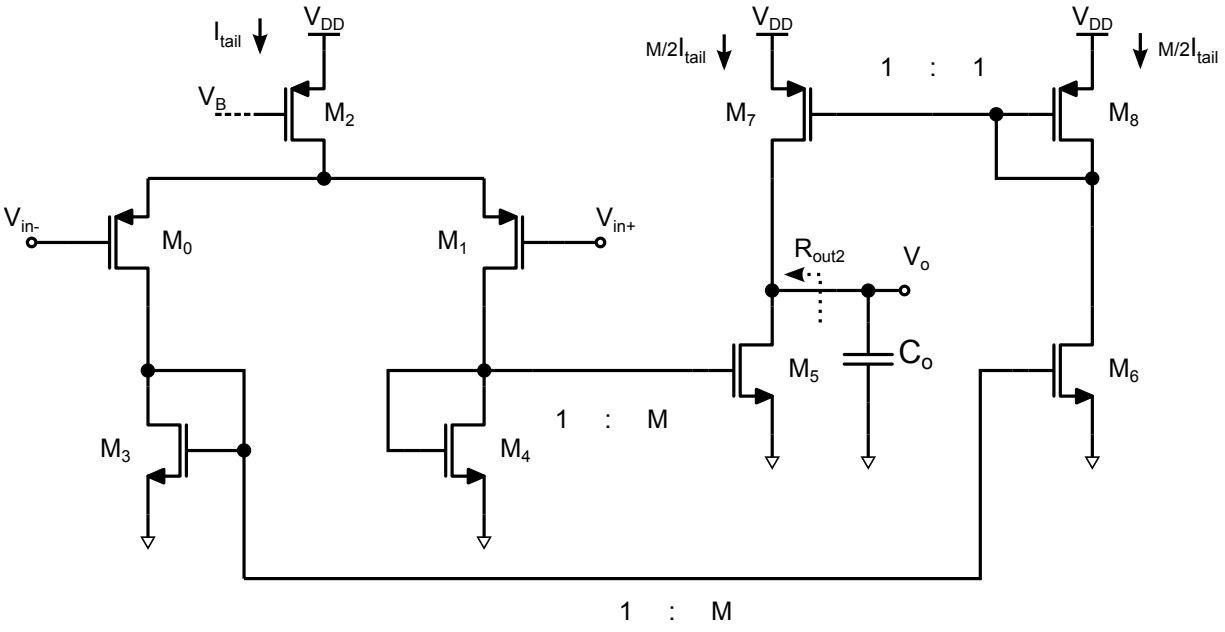

Fig. 4.11: Mirrored OTA, circuit

In the *mirrored OTA* the voltage gain is reached at the output, so it has a single voltage gain stage with a lower gain than *Miller OTA*. The voltage gain at low-medium frequency is:

$$A_{v(DC)} = \frac{v_o}{v_{in+} - v_{in-}} = M g_{m1} R_{out2} \tag{4.27}$$

where $M = \frac{(W/L)_5}{(W/L)_4}$ and $R_{out2} = R_{o5}//R_{o7}$. We consider a perfect matching of transistors $M1 = M0$, $M3 = M4$, $M5 = M6$, $M7 = M8$. The compensation is done in

order to create the dominant pole at the output (because R_{out2} is a high-resistive node), so:

$$A_v(s) = \frac{M g_{m1} R_{out2}}{\left(1 + \frac{s}{2\pi f_{dp}}\right)} \tag{4.28}$$

with $f_{dp} = \frac{1}{2\pi R_{out2} C_o}$.

To increase the voltage gain we may increase the mirror-ratio M, but in this way the total current consumption of the OTA $I_{tot} = I_{tail}(1 + M)$ is increased too.

Noise

Also for this type of OTA we can calculate the $v_{N,in}$ in order to have the equivalent input Noise model of Figure 4.2.

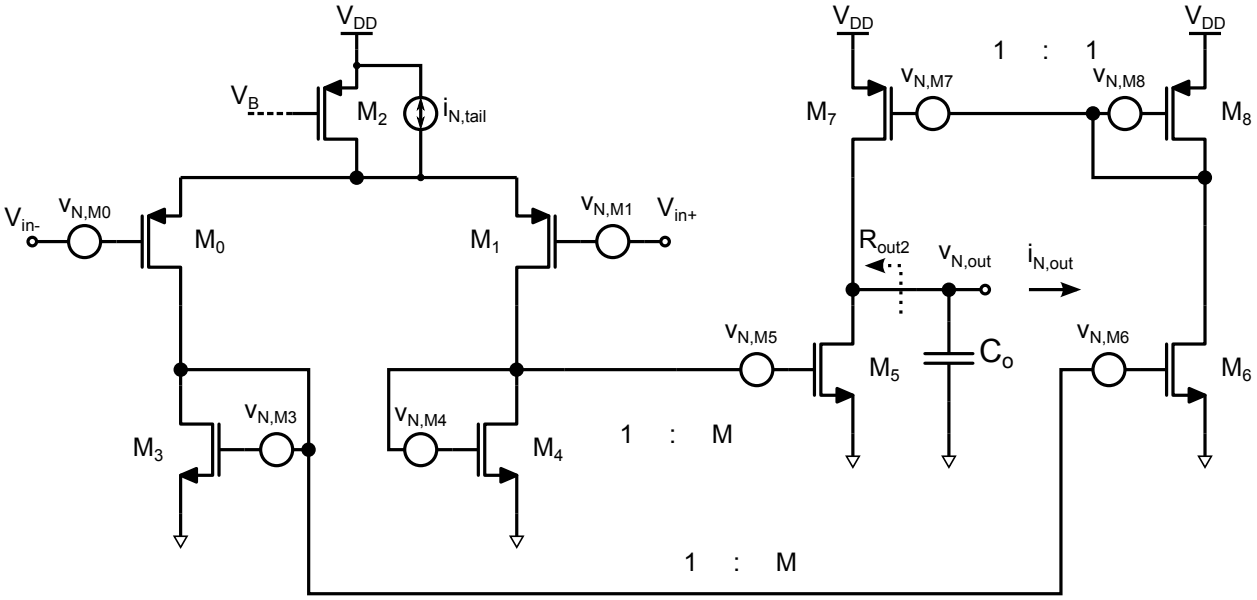

Fig. 4.12: Mirrored OTA, Noise sources

Short the output of the OTA in Figure 4.12 to calculate $i_{N,out}$ at low-medium frequency:

$$\begin{aligned}\frac{\overline{i^2_{N,out}}}{\Delta f} =& (g_{m1})^2 M^2 \left(\frac{\overline{v^2_{N,M0}}}{\Delta f} + \frac{\overline{v^2_{N,M1}}}{\Delta f}\right) + (g_{m4})^2 M^2 \left(\frac{\overline{v^2_{N,M3}}}{\Delta f} + \frac{\overline{v^2_{N,M4}}}{\Delta f}\right) + \\ &+ (g_{m5})^2 \left(\frac{\overline{v^2_{N,M5}}}{\Delta f} + \frac{\overline{v^2_{N,M6}}}{\Delta f}\right) + (g_{m7})^2 \left(\frac{\overline{v^2_{N,M7}}}{\Delta f} + \frac{\overline{v^2_{N,M8}}}{\Delta f}\right)\end{aligned} \tag{4.29}$$

consider $g_{m0} = g_{m1}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, $g_{m7} = g_{m8}$ and $g_{m5} = M g_{m4}$.

Thus dividing Eq. 4.29 by the square of the transconductance of the OTA $(g_{m1}M)^2$ we can find $v_{N,in}$:

$$\frac{\overline{v^2_{N,in}}}{\Delta f} = \frac{16}{3} kT \frac{1}{g_{m1}} \left(1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m4}/M}{g_{m1}} + \frac{g_{m7}/M^2}{g_{m1}}\right) \tag{4.30}$$

It's evident that to reach low-noise performance we have to minimize $\frac{g_{m4}}{g_{m1}}$ and $\frac{g_{m7}}{g_{m1}}$, this can be made as is explained in Par. 4.1.1, so making $(W/L)_1 \gg (W/L)_4, (W/L)_7$, using

degeneration in current mirrors or doing work in *subthreshold* region transistors $M0-M1$. Then we have to increase g_{m1} to decrease the overall Noise, so $I_{tail} \uparrow$ or $(W/L)_1 \uparrow$.

As regard *Flicker Noise*, Eq. 4.12 is still valid for transistors $M0-M1-M3-M4$, the contribution of the other transistors acts (as in Eq. 4.30) with a transconductance ratio $\frac{g_{m4}}{g_{m1}}$ or $\frac{g_{m7}}{g_{m1}}$, so the design rules to minimize Flicker Noise are making $L_1 \ll L_4, L_5, L_7$ and making as bigger as possible the area of input transistors $W_1 L_1 \uparrow$.

Mirrored OTA produces slightly more Noise than *Miller OTA* because there are more transistors that contribute to $v_{N,in}$, as example consider $g_{m4} = g_{m5} = g_{m7}$ (so $M = 1$), Eq. 4.30 reduces to:

$$\frac{\overline{v_{N,in}^2}}{\Delta f} = \frac{16}{3} kT \frac{1}{g_{m1}} \left(1 + 3\frac{g_{m4}}{g_{m1}}\right) \tag{4.31}$$

therefore Eq. 4.31 predicts a little Noise than Eq. 4.8, however this difference can be negligible if $\frac{g_{m4}}{g_{m1}} \ll 1$.

4.2.1 Asymmetric Compensation

In order to achieve the total compensation of the regulator explained in Par. 3.1.2, the voltage gain of the OTA should have a dominant pole and a zero at medium frequency. We can use the *Miller effect* on a single output branch as in Figure 4.13.

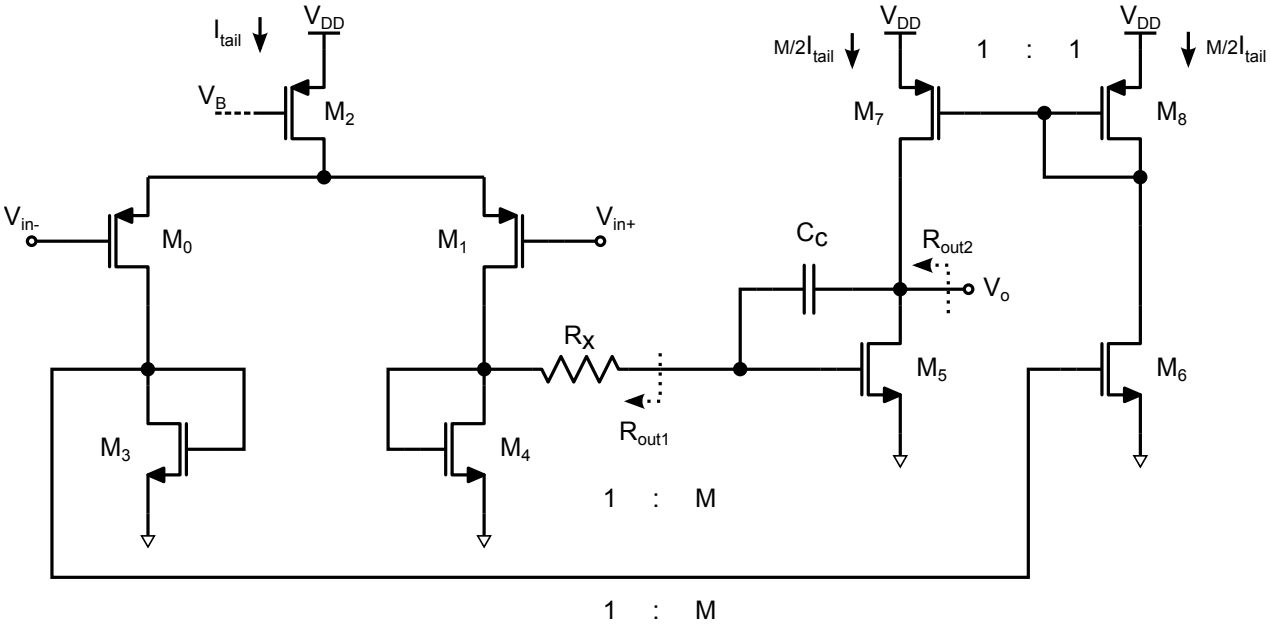

Fig. 4.13: Mirrored OTA, asymmetric compensation

To find the voltage gain, first we have to calculate the transconductance of the OTA (the calculation is made in Appendix. A.12). As regard the output impedance $R_{out2}(s)$, at DC $R_{out2}(DC) = R_{o5}//R_{o7}$ so is a big value, then at low frequency it begins to decrease because of the C_c. The R_x is used to increase the resistance $R_{out1} \approx R_x + (R_{o1}//(1/g_{m4})) \approx R_x$ in order to create a low-frequency pole due to the *Miller effect*:

$$f_{low-f.pole} \approx \frac{1}{2\pi R_x C_c g_{m5} R_{o5}//R_{o7}} \tag{4.32}$$

Then at medium frequencies when the C_c can be considered a short, the transistor $M5$ "becomes" a *diode* so the output resistance is constant at $1/g_{m5}$. Summarizing:

$$R_{out2}(s) \approx \begin{cases} \dfrac{R_{o5}//R_{o7}}{1+\dfrac{s}{2\pi f_{low-f.pole}}} & \text{Low-frequency} \\ R_{o7}//\dfrac{1}{g_{m5}} \approx \dfrac{1}{g_{m5}} & \text{Medium-frequency} \end{cases} \tag{4.33}$$

The voltage gain is $A_v(s) = g_{m(TOT)}(s)R_{out2}(s)$, so using Eq. 4.33, Eq. A.51 and some mathematical properties of the logarithmic scale like the GBW product (Gain Bandwidth), we can calculate the $A_v(s)$:

$$A_v(s) = g_{m1}MR_{o5}//R_{o7}\frac{\left(1+\dfrac{s}{2\pi f_z}\right)}{\left(1+\dfrac{s}{2\pi f_{dp}}\right)} \tag{4.34}$$

with $f_{dp} = f_{low-f.pole}$ and $f_z \approx \dfrac{1}{2\pi C_c R_x/2}$. Note that there is a negative-real part zero (that it creates a phase displacement of $+90°$) and at medium frequency the voltage gain is (this is due to the signal path through transistors $M0/M3/M6/M8/M7$, $g_{m0} = g_{m1}$):

$$A_v(MF) \approx \frac{1}{2}g_{m0}\frac{1}{g_{m3}}g_{m6}\frac{1}{g_{m5}} = \frac{1}{2}\frac{g_{m1}}{g_{m5}/M} = \frac{1}{2}\frac{g_{m1}}{g_{m4}} \tag{4.35}$$

At low frequency $A_v(LF)$ is the same as Eq. 4.27.

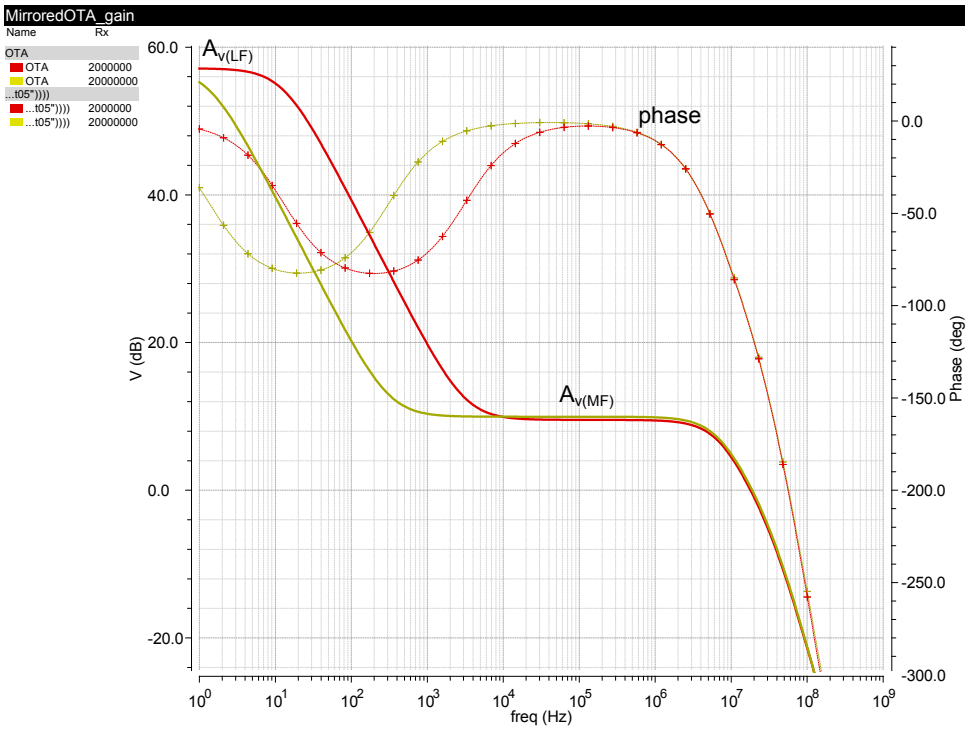

Fig. 4.14: Voltage gain with asymmetric compensation

Note that this is not a general good compensation because the voltage gain is not only a 1-pole transfer function but there is an intrinsic zero, but it's suitable for our purpose.

The distance pole-zero is not a free design-choice but is determined by:

$$\frac{f_z}{f_{pd}} \approx 2g_{m5}(R_{o5}//R_{o7}) \tag{4.36}$$

The distance pole-zero is approximately the voltage gain of a single stage so about $2-3$ decades, this is enough for our purpose.

Noise

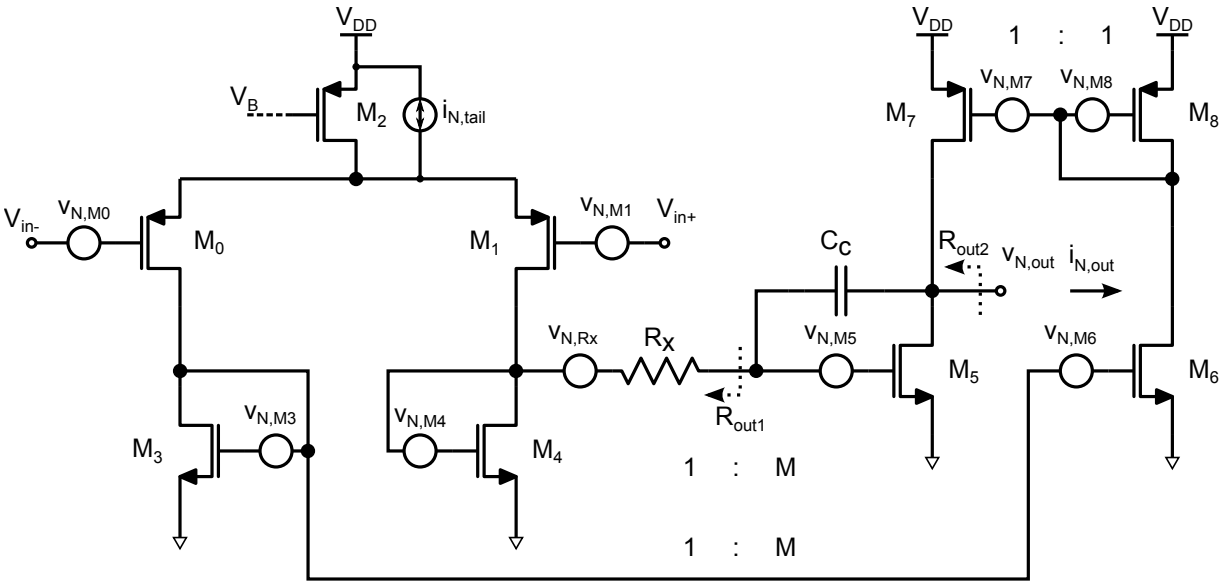

Fig. 4.15: Asymmetric compensation, Noise sources

The input couple (transistors $M0-M1$) influences directly the $v_{N,in}$:

$$\frac{\overline{v^2_{N,in(M0-M1)}}}{\Delta f} = \frac{16}{3}kT\frac{1}{g_{m1}} \tag{4.37}$$

the Noise of the other transistors and of R_x is discussed below.

R_x Noise

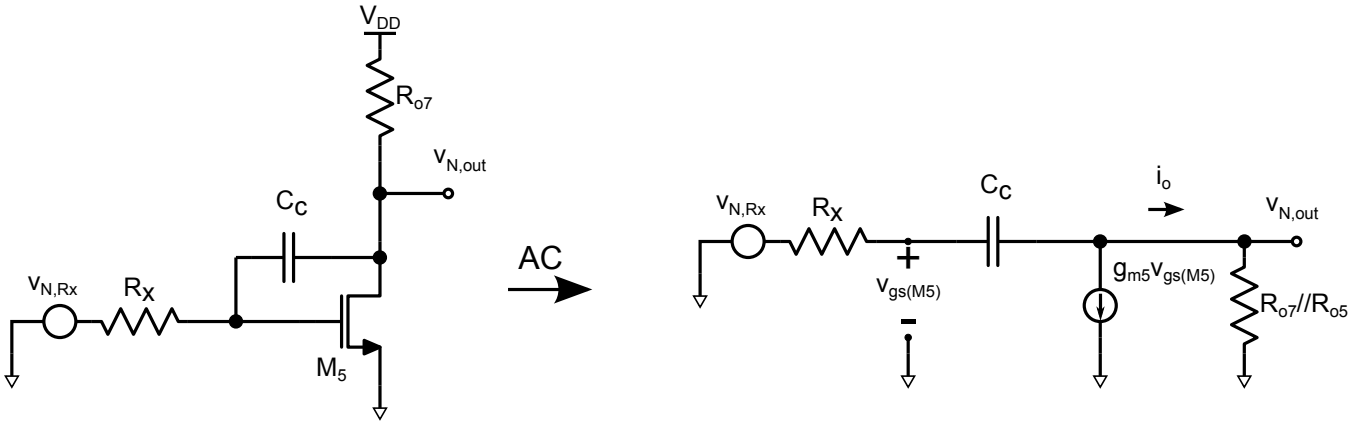

Fig. 4.16: R_x Noise, circuit and AC model

The circuit "seen" from v_{N,R_x} is in Figure 4.16, R_x is connected in series with $R_{o1}//(1/g_{m4}) \approx 1/g_{m4}$ so this last term may be neglected. To find the transfer function to the output we have to solve this system of equations (consider voltages and currents expressed in $[V/\sqrt{Hz}]$, $[A/\sqrt{Hz}]$):

$$\begin{cases} v_{N,out(R_x)} = i_o(R_{o7}//R_{o5}) \\ i_o = \dfrac{v_{N,R_x} - v_{N,out(R_x)}}{R_x + \dfrac{1}{sC_c}} - g_{m5}v_{gs(M5)} \\ v_{gs(M5)} = v_{N,R_x} - \dfrac{v_{N,R_x} - v_{N,out(R_x)}}{R_x + \dfrac{1}{sC_c}} R_x \end{cases} \tag{4.38}$$

This is a classical gain stage with Miller capacitor C_c so the voltage transfer function is:

$$\left| \frac{v_{N,out(R_x)}}{v_{N,R_x}}(s) \right| = g_{m5}(R_{o7}//R_{o5}) \frac{\left(1 - s\dfrac{C_c}{g_{m5}}\right)}{(1 + sR_xC_cg_{m5}R_{o7}//R_{o5})} \tag{4.39}$$

We can see the shaping of $v_{N,out(R_x)}$ in Figure 4.17 (pole and zero are calculated in Eq. 4.39).

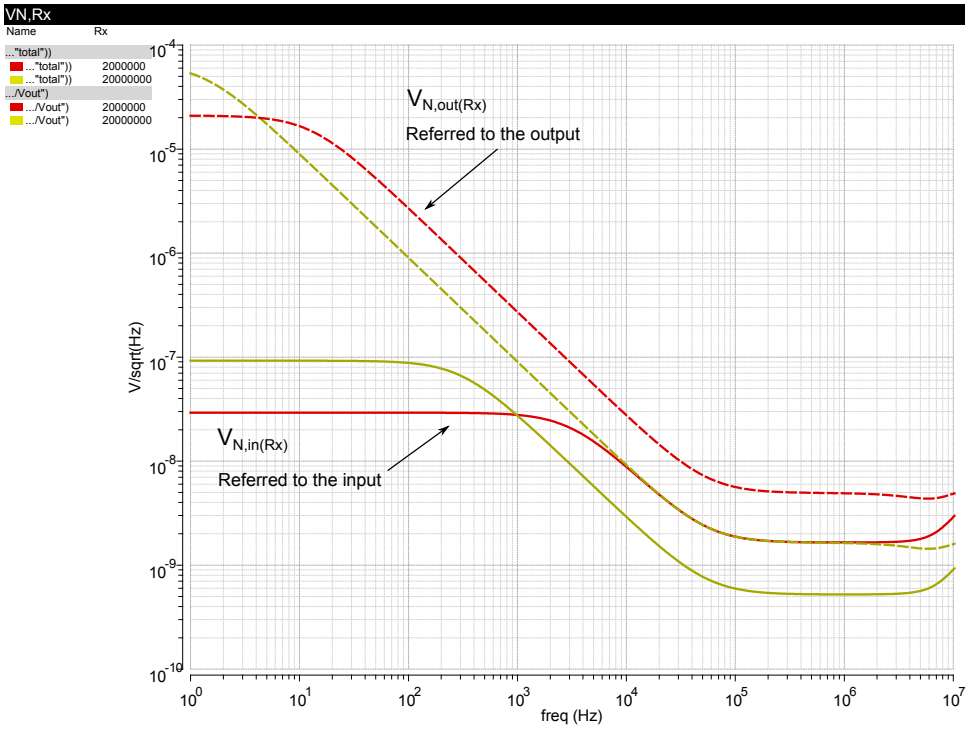

Fig. 4.17: R_x Noise, input-referred and output-referred

Then the input-referred Noise, so $v_{N,in(R_x)}$, it's simple to obtain (compare with Figure 4.17):

$$\left| \frac{v_{N,in(R_x)}}{v_{N,R_x}} \right| = \left| \frac{v_{N,out(R_x)}}{v_{N,R_x}} \right| \left| \frac{1}{A_v(s)} \right| = \frac{g_{m4}}{g_{m1}} \frac{\left(1 - s\dfrac{C_c}{g_{m5}}\right)}{(1 + sC_cR_x/2)} \tag{4.40}$$

At Low-frequency the Noise is slightly reduced by the factor $g_{m4}/g_{m1} < 1$ and at medium-high frequency it's considerably reduced by roughly $\frac{2}{g_{m1}MR_x} \ll 1$, so this is a good notice because R_x Noise can be made negligible respect the Noise of the other transistors.

As regard transistor $M4$, $v_{N,M4}$ "see" roughly the same transfer function of v_{N,R_x} (Eq. 4.40), since usually $1/g_{m4} \ll R_x$, $v_{N,in(M4)}$ is completely negligible.

$M3/5/6/7/8$ Noise

Transistors Mi with $i = 3, 5, 6, 7, 8$ transfer (directly or mirrored) their current Noise $i_{N,Mi}$ into the output node with impedance $R_{out2}(s)$, so the $v_{N,out(Mi)}$:

$$\begin{aligned} \frac{v_{N,out(Mi)}}{\sqrt{\Delta f}} &= R_{out2}(f)\frac{i_{N,Mi}}{\sqrt{\Delta f}} \\ &= R_{out2}(f)g_{mi}\frac{v_{N,Mi}}{\sqrt{\Delta f}} \end{aligned} \tag{4.41}$$

We have already explained what is the behavior of $R_{out2}(f)$ in Eq. 4.33, so it's possible to demonstrate that:

$$\frac{v_{N,in(Mi)}}{v_{N,Mi}}(s) = \frac{1}{A_v(s)}\frac{v_{N,out(Mi)}}{v_{N,Mi}}(s) = \frac{g_{mi}}{Mg_{m1}}\frac{(1+sC_cR_x)}{(1+sC_cR_x/2)} \tag{4.42}$$

compare Eq. 4.42 with Figure 4.18.

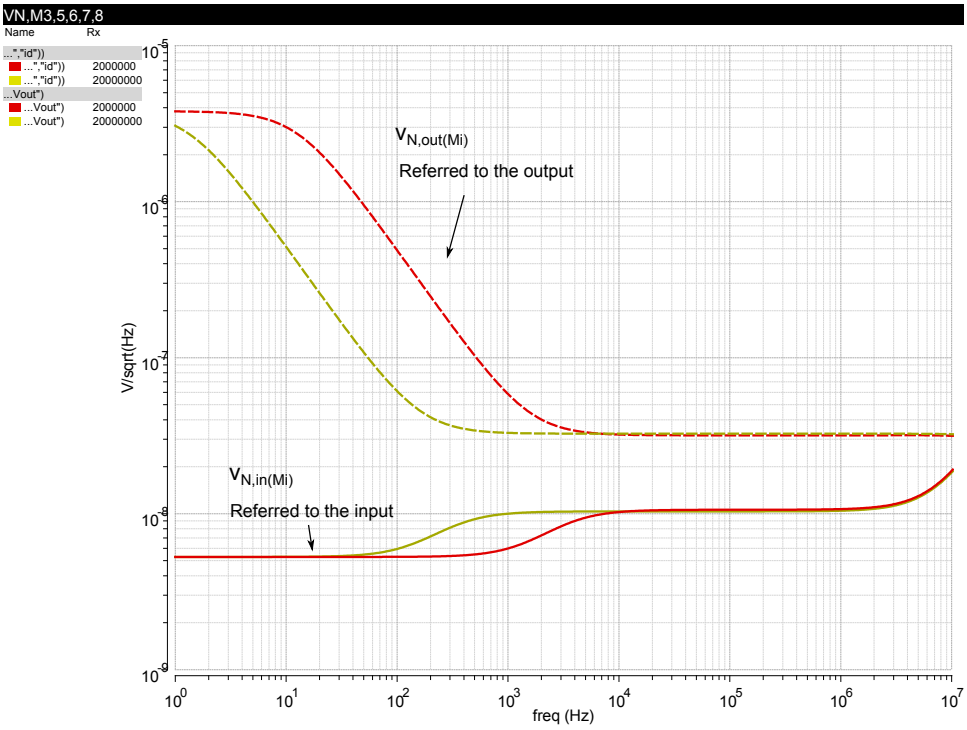

Fig. 4.18: $M3/5/6/7/8$ Noise, input-referred and output-referred

At medium-high frequency, when we have the simultaneous effect of pole and zero, the transfer function $\frac{v_{N,in(Mi)}}{v_{N,Mi}} \approx \frac{2g_{mi}}{Mg_{m1}}$, so is doubled. Since the transfer function is doubled at least in the last decade $10kHz \leq f \leq 100kHz$ (see Figure 4.18, remember that

our integration band is until $f_{MAX} = 100kHz$) we can consider a 2 factor over all the bandwidth (a factor 4 if we consider the power instead the voltage).

We can sum together all the contributions to obtain a compact formula:

$$\frac{\overline{v^2_{N,in(TOT)}}}{\Delta f} \approx \frac{16}{3}kT\frac{1}{g_{m1}}\left(1 + 2\frac{g_{m4}}{g_{m1}} + 4\frac{g_{m4}/M}{g_{m1}} + 4\frac{g_{m7}/M^2}{g_{m1}}\right) \tag{4.43}$$

Remember that we have neglected the Noise of $M4$ and R_x.

As regard *Flicker* Noise, like the classical Mirrored OTA we have to make $L_1 \ll L_4, L_5, L_7$ and making as bigger as possible the area of input transistors $W_1L_1 \uparrow$.

Comparing Eq. 4.43 with Eq. 4.30 we can see that the Noise is increased, but we can easily choose a suitable R_x to perform the desired compensation and this resistance does not increase appreciably the total Noise. However we would like high g_{m4}/g_{m1} to have low-Noise but doing this we increase the $A_v(MF)$ of the OTA (Eq. 4.35) and this is a problem for the compensation of the regulation Loop, so it must be found a trade-off Noise-Gain in medium frequency. The performance of $CMRR$ and $PSRR$ have to be analyzed in detail to be sure that this type of compensation is suitable for our purpose.

4.3 OTA Design

4.3.1 Requirements

In order to design the EA (the OTA) for the regulator, there are three main requirements to take into account: the *Steady-state* performance, the compensation of the regulation Loop and the Noise budget.

Steady-state Performance

Steady-state Performance were discussed in Par. 3.1.1, *Line regulation* is a function of the Voltage Reference and the regulation-Loop, however is the behavior of voltage reference that dominates Line regulation performance. Instead the *Load regulation* depends directly from the regulation Loop (see Eq. 3.7) which in turn it depends from the EA, so there are some constraints that the EA must respect.

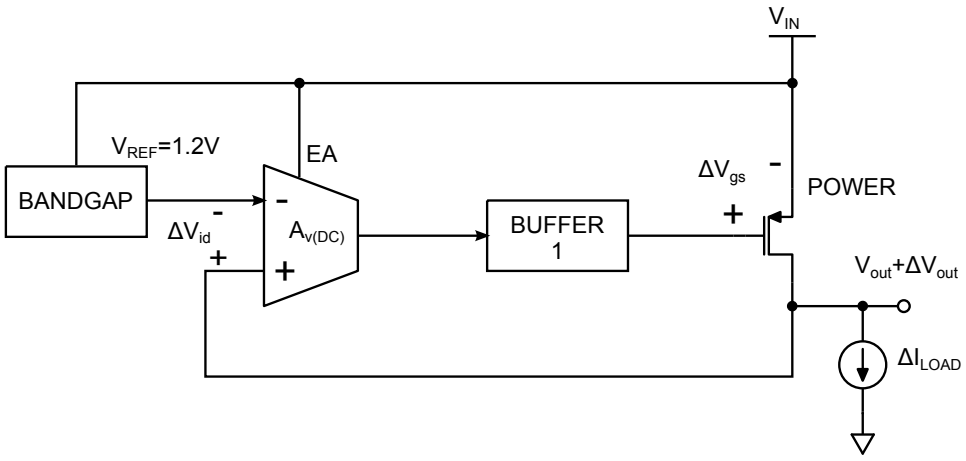

Fig. 4.19: Load Regulation

Usually Load regulation is measured with the LDO closed in unitary feedback so we consider $V_{REF} = V_{out} = 1.2V$. In response to a *Load change* ΔI_{LOAD}, the variation of the output voltage so ΔV_{out} must not exceed a given value, usually expressed as percentage of the output voltage $\epsilon\% = \frac{\Delta V_{out}}{V_{out}}\%$.

Think the load step is from the minimum to the maximum current $|\Delta I_{LOAD}| = |I_{LOAD,max} - I_{LOAD,min}| \approx |1A - 10mA| \approx 1A$ and consider a usual value of $\epsilon\% = 0.5\%$ so $|\Delta V_{out}| = |\epsilon\% V_{out}| = \frac{0.5}{100}1.2 = 6mV$. To support a $|\Delta I_{LOAD}| = 1A$ the power transistor has to change its V_{gs}, so there is a variation of about $|\Delta V_{gs}| \approx 1V$ ($|\Delta V_{gs}|$ has to be determined by a simulation because depends on the transistor parameters, dimensions...). The $|\Delta V_{gs}|$ moves through the buffer and the output of the EA varies as $|\Delta V_{o(EA)}| \approx |\Delta V_{gs}| \approx 1V$, on the other side the differential input of the EA varies as $|\Delta V_{id(EA)}| \approx |\Delta V_{out}| \approx 6mV$, so the voltage gain of the EA should be at least:

$$A_{v(DC)} = \left|\frac{\Delta V_{o(EA)}}{\Delta V_{id(EA)}}\right| \geq \quad \approx 60dB$$

Stability of the Regulation Loop

The study of the Stability of the Regulation Loop was discussed in Par. 3.1.2 and Par. 3.3.1, let us now to find some constraints for the EA by the simulation of the regulator with the following blocks:

- ERROR AMPLIFIER

  Its transfer function can be considered that depicted in Figure 4.14 with the transfer function of Eq. 4.34.

  Simulation parameters: $A_{v(DC)} = 60dB$, $f_{dp(EA)} \approx 10Hz$, $f_{z(EA)} \approx 10kHz$, a parasitic pole at $f_{par.(EA)} \approx 10MHz$.

  By varying slightly $f_{z(EA)}$ we vary slightly the $A_{v(MF)}$ (refer to Figure 4.14), the main problem for the stability we will explain that is precisely the $A_{v(MF)}$, and we'll have to find a tradeoff gain/Noise.

- BUFFER

  The Buffer has unitary gain in a large bandwidth, however the input capacitance of the power transistor creates a parasitic pole p_{BUF} (Eq. 3.17).

  Simulation parameters: $f_{p(BUF)} \approx 1MHz$.

- FEEDBACK

  The Feedback Network is the voltage divider which guarantees the regulation $V_{out} = 5V$, the Bypass capacitor is used to reduce Noise. The Feedback transfer function is that depicted in Figure 3.19.

  Simulation parameters: $R_1 = 630k\Omega$, $R_1 = 200k\Omega$, $C_B = 1nF$, $f_{z(FB)} \approx 250Hz$, $f_{p(FB)} \approx 1kHz$.

- POWER STAGE

  The Power stage uses a PMOS transistor so, in AC, it's a gain stage that depends on the I_{LOAD}, the C_L creates the output pole p_{out}(Eq. 3.16) and the ESR creates a zero (Eq. 3.14).

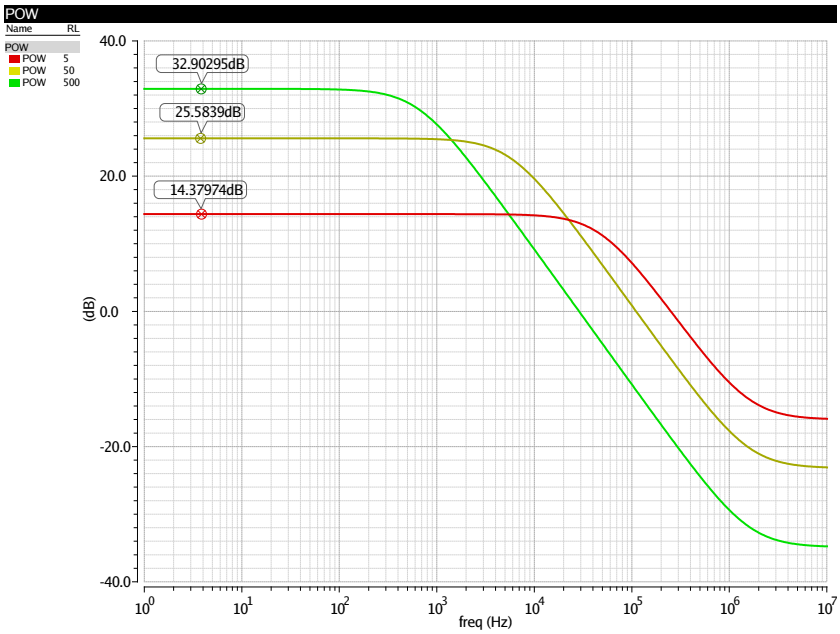

Fig. 4.20: Power stage, $C_L = 1\mu F$, $ESR = 100m\Omega$, $I_L = 1A, 100mA, 10mA$

The desired Loop-gain of the regulation loop is that proposed in Figure 3.5 and, of course, with the bypass capacitor in Figure 3.24. The biggest problem is that at medium frequency, about $1kHz < f < 100kHz$, we would like that the Loop-gain $|T| \leq 20dB$ because then there is the output pole p_{out}. The Power stage has a roughly gain of $A_{v(POW)} \approx 20dB$, the feedback network has a unitary gain at medium frequency thanks to C_B and the EA has a voltage gain $A_{v,EA(MF)}$, so at medium frequency the Loop-gain has $|T_{(MF)}| \approx A_{v(POW)} A_{v,EA(MF)}$ that it could be $|T_{(MF)}| > 20dB$. This leads the Loop-gain to cut the frequency axis at a too high frequency $f_{c(LG)} \approx 1MHz$ where there could be many more parasitic poles than those simulated, these could lead to the *instability*.

The principal constraint is therefore the $A_{v,EA(MF)}$, the worst-case is at the maximum $I_{LOAD} = 1A$ because p_{out} is at the highest frequency and so $f_{c(LG)}$ is the highest.

$f_{z(EA)}$ [kHz]	$A_{v,EA(MF)}$ [dB]	$f_{c(LG)}$ [kHz]	PM [°]
10	0	231	93
5	6	453	85
3	10	655	81

Tab. 4.1: $A_{v,EA(MF)}$ effect on the Loop-gain at $I_L = 1A$

The position of the EA zero is not so relevant, thus the suitable range is $1kHz \leq f_{z(EA)} \leq 100kHz$. $A_{v,EA(MF)}$ has a big impact on the $f_{c(LG)}$ even if the Phase Margin is very good ($PM > 80°$ but in the simulation are not taken into account many parasitic poles that there are in a real circuit so the phase margin could be smaller), because the crossing frequency is quite high, we should design the OTA to maintain $f_{c(LG)} \leq 500kHz$, so it must be $A_{v,EA(MF)} \leq 6 - 7dB$.

Figure 4.22 and Figure 4.23 show how the Loop-gain module varies in the "worst case" with $A_{v,EA(MF)} = 10dB$: the compensation is good because $PM > 80°$ for all simulations, however the phase margin could be much smaller in particular at $I_L = 1A$ and $C_L = 1\mu F$ (the red curve).

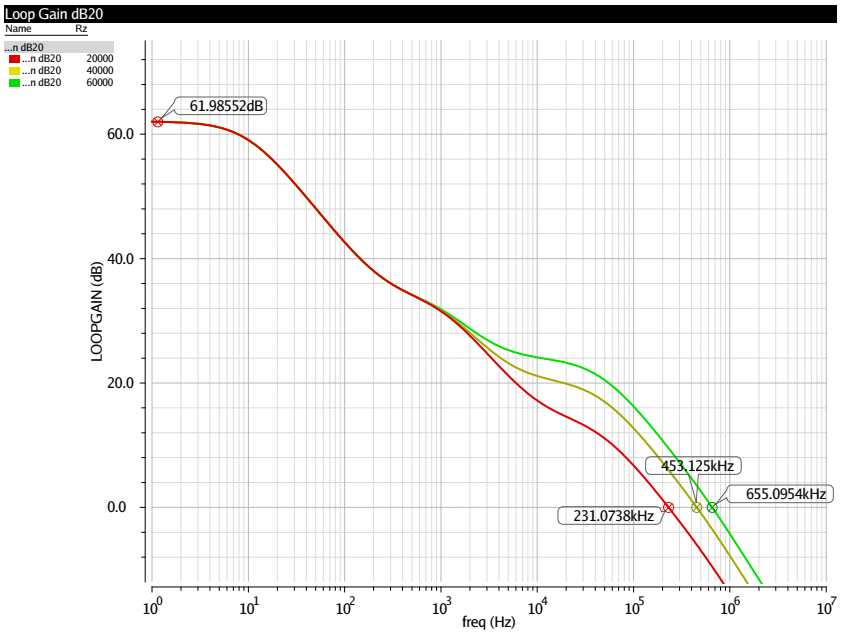

Fig. 4.21: Loop-gain Module at $I_L = 1A$, $C_L = 1\mu F$, $C_B = 1nF$, varying $f_{z(EA)}$, $A_{v,EA(MF)}$

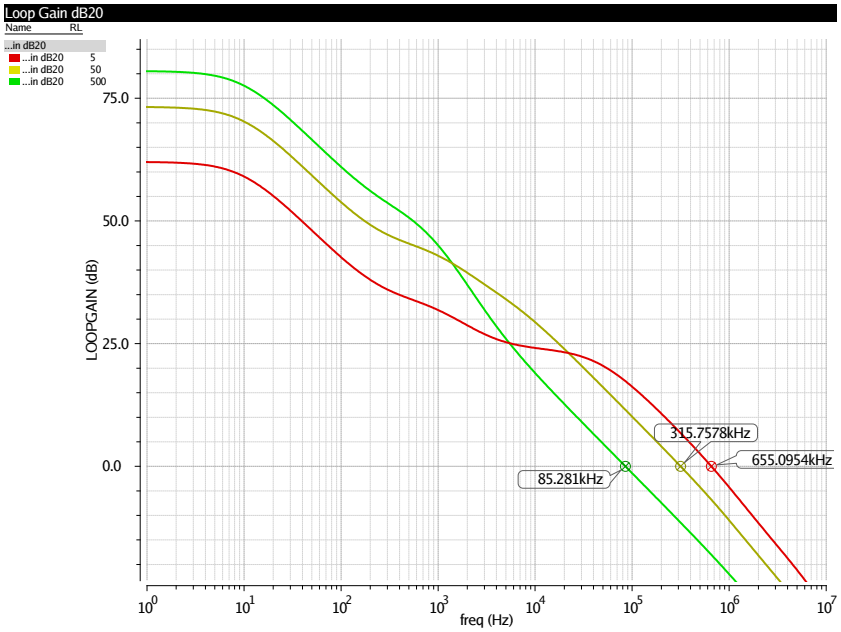

Fig. 4.22: Loop-gain Module at $A_{v,EA(MF)} = 10dB$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$, varying $I_L = 1A, 100mA, 10mA$

Noise Budget

With the use of the bypass capacitor C_B we prevent the amplification $1/\beta_F$ of the Voltage Reference (Bandgap) and EA Noise, so the transfer function from the input of the EA to the output of the regulator is unitary (see Par. 3.3.1). Remember that the integration band is $10Hz \leq f \leq 100kHz$ and the target is $V_{N,out(INTEGRATED)} \leq 20\mu V_{RMS}$ over the band. Since we have not modeled the Flicker Noise, we may consider that few μV_{RMS} are produced by Flicker, so we have to keep a safety margin of few μV_{RMS}.

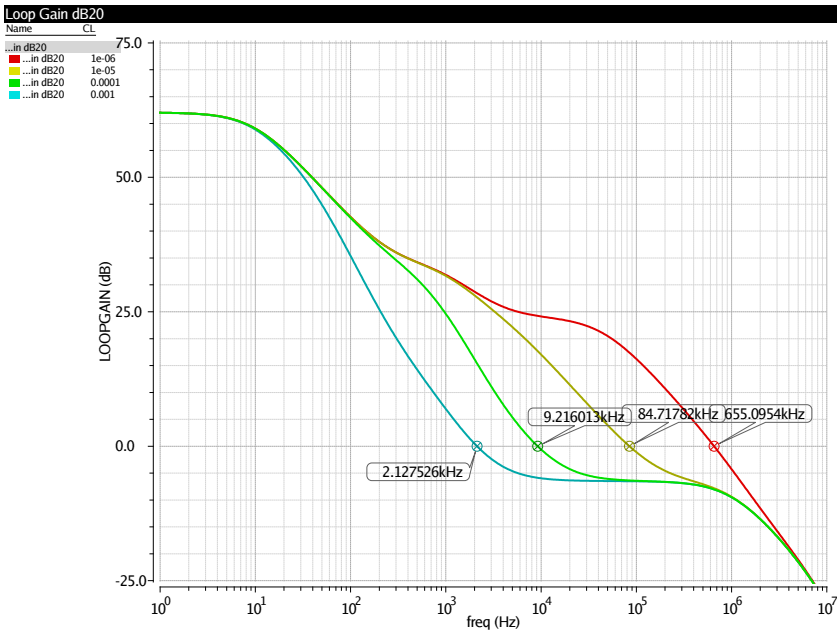

Fig. 4.23: Loop-gain Module at $A_{v,EA(MF)} = 10dB$, $I_L = 1A$, $ESR = 100m\Omega$, $C_B = 1nF$, varying $C_L = 1\mu F, 10\mu F, 100\mu F, 1mF$

A reasonable Noise budget can be divided in this way:

$$\begin{aligned} V_{N,out(INT.)} &\approx \sqrt{\left(V_{N,BG(INT.)}\right)^2 + \left(V_{N,EA(INT.)}\right)^2 + \left(V_{N,FB(INT.)}\big|_{C_B}\right)^2} \\ &\approx \sqrt{\left(13\mu V_{RMS}\right)^2 + \left(10\mu V_{RMS}\right)^2 + \left(4.1\mu V_{RMS}\big|_{C_B=1nF}\right)^2} \\ &\approx 17\mu V_{RMS} \end{aligned} \tag{4.44}$$

Therefore we should be able to design an EA with $V_{N,EA(INT.)} \leq 10\mu V_{RMS}$, obviously more low-Noise it is and better is.

4.3.2 Proposed OTA

The proposed OTA is a mirrored OTA with an asymmetrical compensation to the output, the circuit is depicted in Figure 4.31, the analysis of the OTA is in Par. 4.2.1. For the transistor number (M_x) refer to Figure 4.13 instead to Figure 4.31.

The constraints for the design are explained in Par. 4.3.1, but are quickly repeated below for convenience:

1. $A_{v(DC)} \geq 60dB$
2. $1kHz \leq f_{z(EA)} \leq 10kHz$
3. $A_{v(MF)} \leq 7dB$
4. $V_{N,in(INTEGRATED)}\Big|_{10Hz-100kHz} \leq 10\mu V_{RMS}$
5. maximum total current consumption $I_{TOT(MAX)}$ few tens of μA

Initial design choices taken (consider $(W/L)_0 = (W/L)_1$, $(W/L)_3 = (W/L)_4$, $(W/L)_5 = (W/L)_6 = M(W/L)_4$, $(W/L)_7 = (W/L)_8$):

- $I_{tail} = 10\mu A$ (but can be increased up to $15\mu A$).
- $g_{m1} \uparrow$ is high thanks to a big $(W/L)_1 \uparrow\uparrow$, this helps to increase $A_{v(DC)}$ and to decrease *Thermal* Noise. Since the area $(WL)_1 \uparrow\uparrow$ is big the *Flicker* Noise is decreased.
- $L_{3/4/5/6/7/8} < L_1$ to not increase *Flicker* Noise.
- $M = \dfrac{(W/L)_5}{(W/L)_4} = 2$ to not increase *Thermal* Noise. M may not be very big because the total current consumption is increased $I_{TOT} = I_{tail}(1 + M)$.
- $g_{m7} \ll g_{m1}$ to not increase *Thermal* Noise. To make a small $g_{m7} \downarrow$ is necessary $(W/L)_7 < 1$.
- $C_c = 50pF$, $R_x = 2M\Omega$ in order to have $f_{z(EA)} \approx 3kHz$.

In order to respect the specifications $1, 3, 4$ we have to find a suitable $W_{3/4}$ to determine a right g_{m4}, this is made by simulations shown in Figure 4.24 and Figure 4.25.

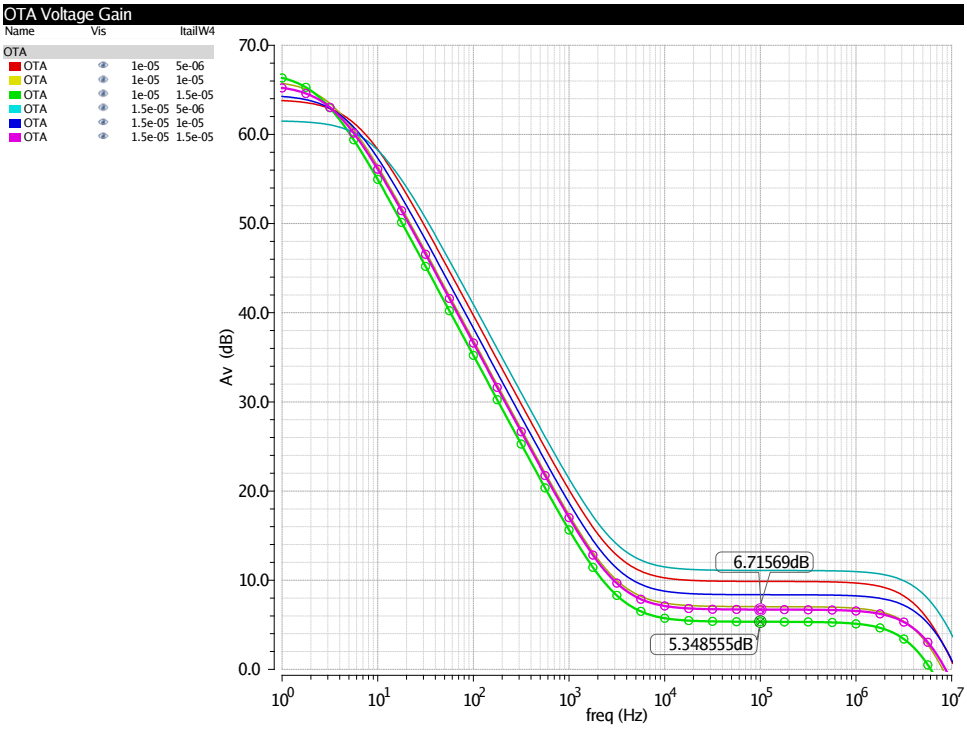

Fig. 4.24: Voltage gain, $W_1 = 200\mu m$, $(W/L)_5 = 2(W/L)_4$

W_4 $[\mu m]$	I_{TOT} $[\mu A]$	$A_{v,(DC)}$ [dB]	$A_{v,(MF)}$ [dB]	$V_{N,in(INT.)}$ $[\mu V_{RMS}]$
15	30	≈ 66	5.3	8.8
15	45	≈ 66	6.7	7.1

So with $W_4 = 15\mu m$ and $I_{TOT} = 30 - 45\mu A$ we met the specifications.

We can try to change g_{m1} by varying W_1 to increase/decrease the Noise and Voltage gain(Figure 4.26 and Figure 4.27).

We may see by varying W_1 that the voltage gain A_v and $V_{N,in(INT.)}$ remain practically unchanged, this because the g_{m1} is near to saturate and doesn't vary more appreciably. So

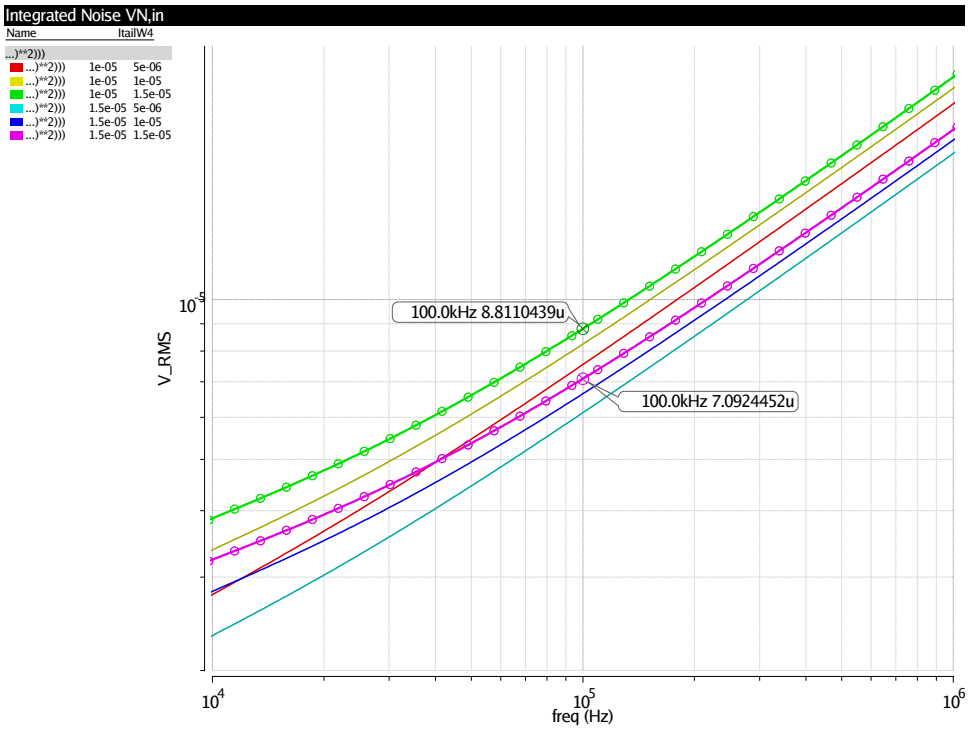

Fig. 4.25: Integrated input Noise voltage, $W_1 = 200\mu m$, $(W/L)_5 = 2(W/L)_4$

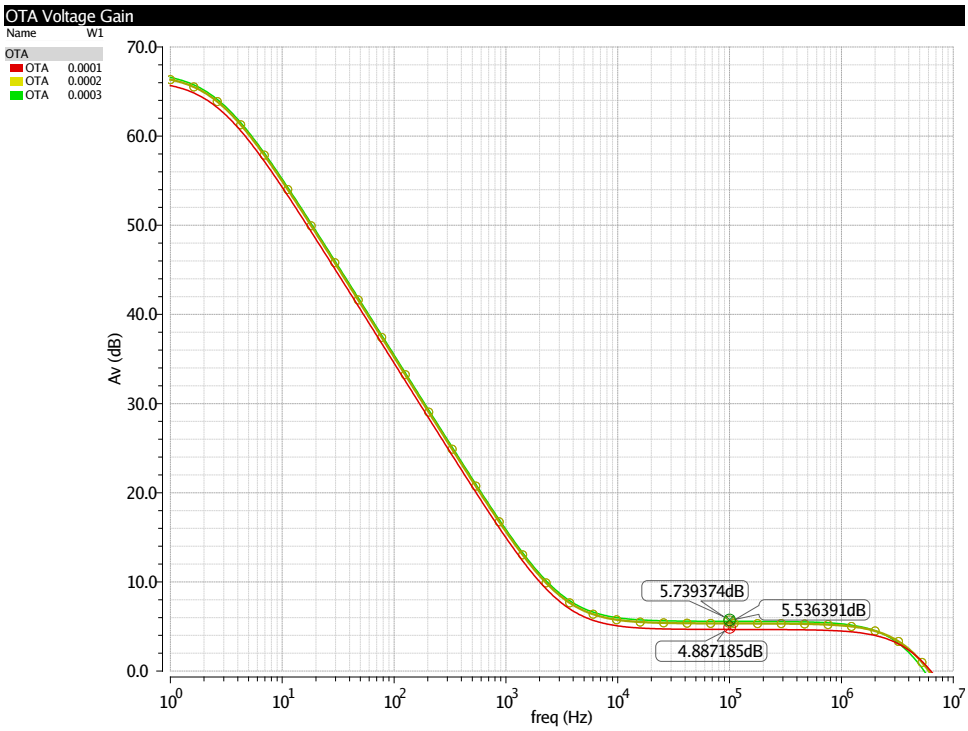

Fig. 4.26: Voltage gain, $W_4 = 15\mu m$, $(W/L)_5 = 2(W/L)_4$, $I_{TOT} = 30\mu A$

in the view to reduce *Flicker* Noise and don't occupy too much area, I choose to maintain $W_1 = 200\mu m$.

It's interesting to observe what are the Noise contributions of the single transistors and the resistance (Figure 4.28).

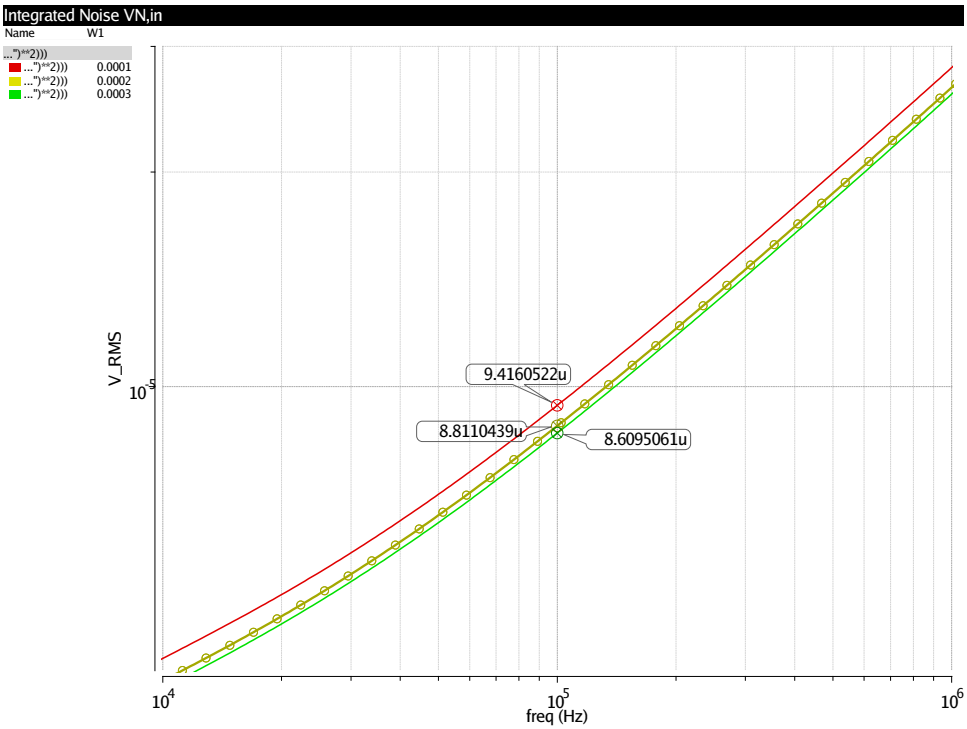

Fig. 4.27: Voltage gain, $W_4 = 15\mu m$, $(W/L)_5 = 2(W/L)_4$, $I_{TOT} = 30\mu A$

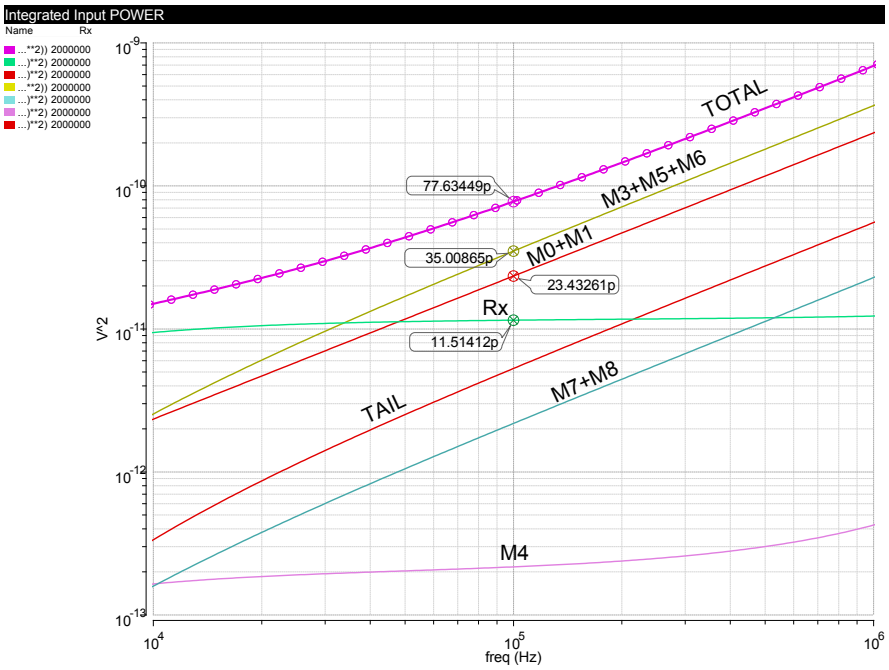

Fig. 4.28: $V^2_{N,in(INT.)}$ with $W_1 = 200\mu m$, $W_4 = 15\mu m$, $(W/L)_5 = 2(W/L)_4$, $I_{TOT} = 30\mu A$

Figure 4.28 confirms that the most of Noise is produced by the input couple $M0 - M1$ (15% each one) and from transistors $M3 - M5 - M6$ (15% each one), we have minimized the Noise of $M7 - M8$ that is negligible and the Noise of $M4$ is totally negligible as we said in Par. 4.2.1, R_x contributes to the total Noise power with about a 15%.

Theoretically we can calculate $V_{N,in(INT.)}$ integrating over the band ($B = 100kHz - 10Hz \approx 100kHz$) the Eq. 4.43 and then making the square root, since $M = 2$ and

neglecting g_{m7}/g_{m1}, the more compact formula is:

$$V_{N,in(INT.)} \approx \sqrt{\frac{16}{3}kT\frac{1}{g_{m1}}\left(1+4\frac{g_{m4}}{g_{m1}}\right)} \times \sqrt{B} \tag{4.45}$$

With the manual calculation of Eq. 4.45 it results $V_{N,in(INT.)} \approx 6.3\mu V_{RMS}$, instead with the help of Figure 4.28, considering only the Noise produced by $M0-M1-M3-M5-M6$ it results $V_{N,in(INT.)} \approx 7.6\mu V_{RMS}$.

The designed OTA has a current consumption of $I_{TOT} = 30\mu A$, the dimensions of transistors are shown in Figure 4.31 and $W_1 = 200\mu m$, $W_4 = 15\mu m$. It respect all the specifications 1/2/3/4/5 and there is a parasitic pole in the voltage gain in high frequency at about $f_{par.(EA)} \approx 4MHz$.

Stability and Noise performance of the Regulator with the designed OTA

The Stability and Noise performance of the Regulator with the proposed OTA are depicted in Figure 4.29 and Figure 4.30 (except the EA, which is that designed, the other blocks are those explained in Par. 4.3.1).

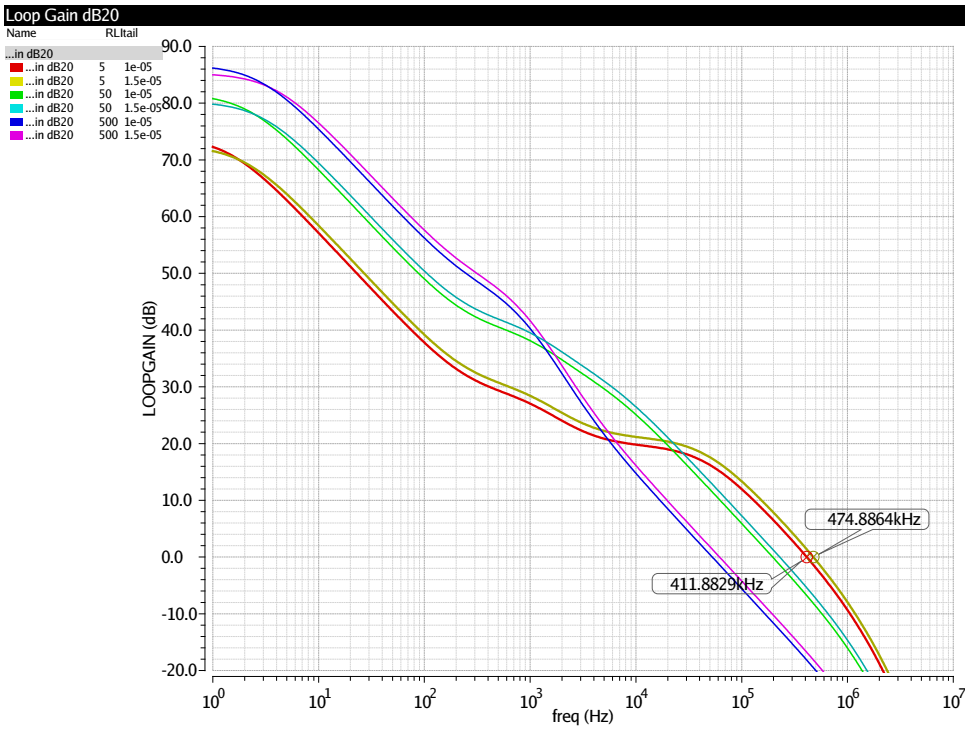

Fig. 4.29: Loop-gain Module, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$, $R_1 = 630k\Omega$, $R_2 = 200k\Omega$

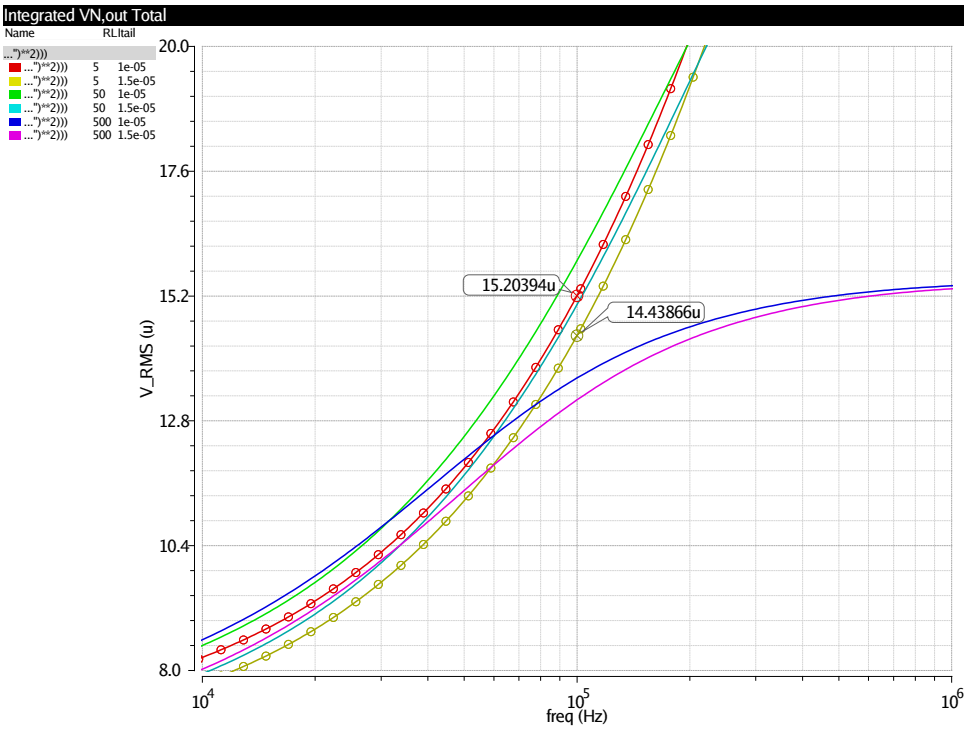

Fig. 4.30: $V_{N,out(TOT,INT.)}$ with $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$, $R_1 = 630k\Omega$, $R_2 = 200k\Omega$, simulated Bandgap $V_{N,BG(INT.)} \approx 12\mu V_{RMS}$

I_{tail} $[\mu A]$	$I_{TOT(EA)}$ $[\mu A]$	$f_{c(LG)}$ [kHz]	PM [°]	$V_{N,out(TOT,INT.)}$ $[\mu V_{RMS}]$
10	30	412	77	15.2
15	45	475	74	14.4

Tab. 4.2: Stability and Noise performance of the Regulator at $I_L = 1A$

The Loop-gain cuts the frequency axis at a frequency lower than $500kHz$, this is really good and also the Phase Margin is quite good $\approx 75°$ at $I_L = 1A$ and also better at $I_L = 10 - 100mA$ at about $\approx 85°$.

As regard the Noise performance, considering $V_{N,BG(INT.)} \approx 12\mu V_{RMS}$, we have $V_{N,out(TOT,INT.)} \approx 15\mu V_{RMS}$ that is a very good performance because we have a good margin of $5 - 4\mu V_{RMS}$ for the *Flicker* Noise, however we should be able to design a low-Noise voltage reference with about $V_{N,BG(INT.)} \approx 12 - 13\mu V_{RMS}$.

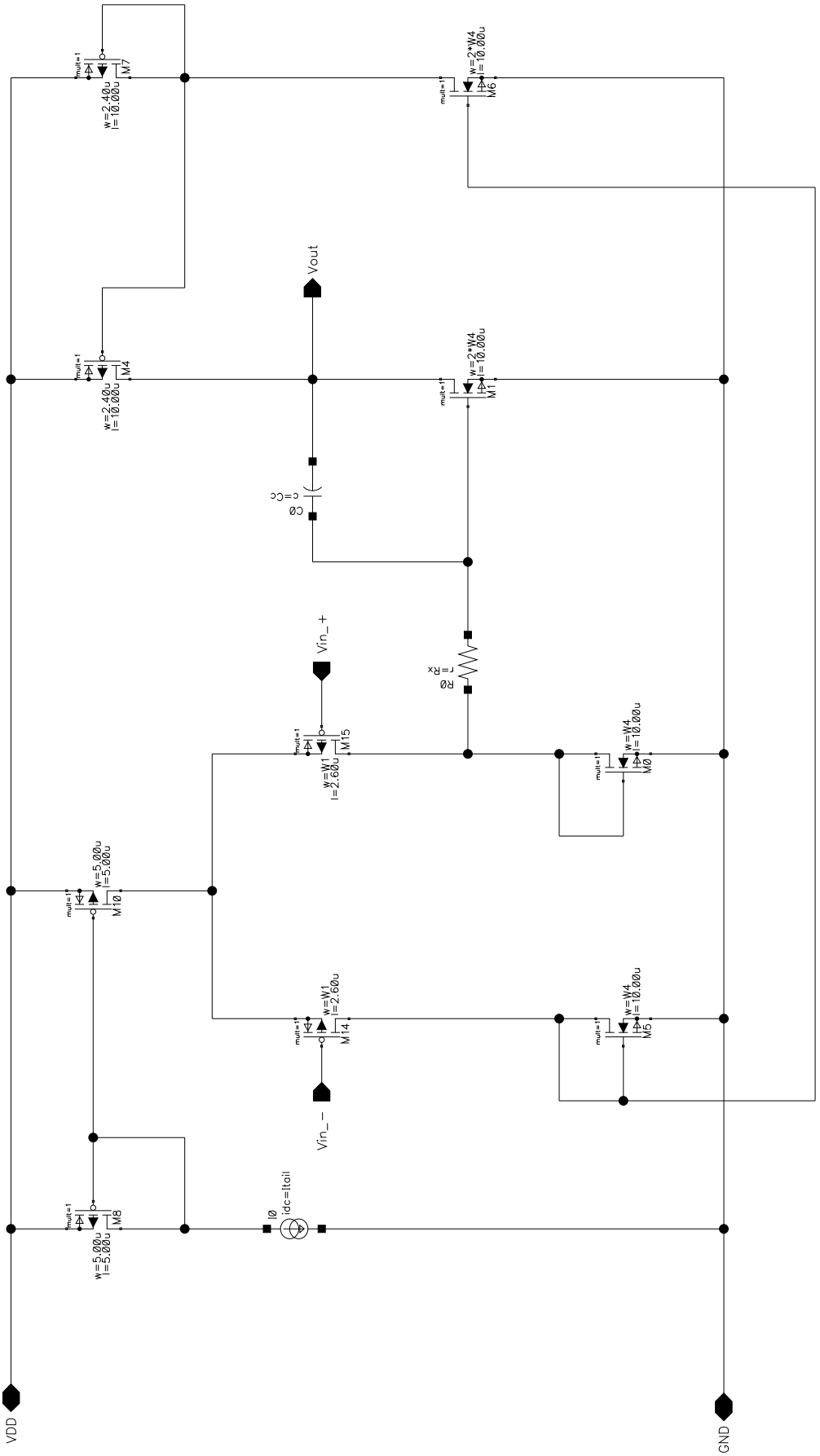

Fig. 4.31: Proposed OTA

Chapter 5

Voltage Reference Noise

The Voltage Reference, also called simply *Bandgap* generator, is a circuit that provides an output voltage insensitive to the absolute Temperature. There are many topologies that allow to obtain this insensitive voltage, I choose to analyze and to design the *Brokaw Bandgap* (see [1]), the theoretical analysis refers to Figure 5.1 and simulations are made with the designed Bandgap with NMOS-output of Figure 5.10.

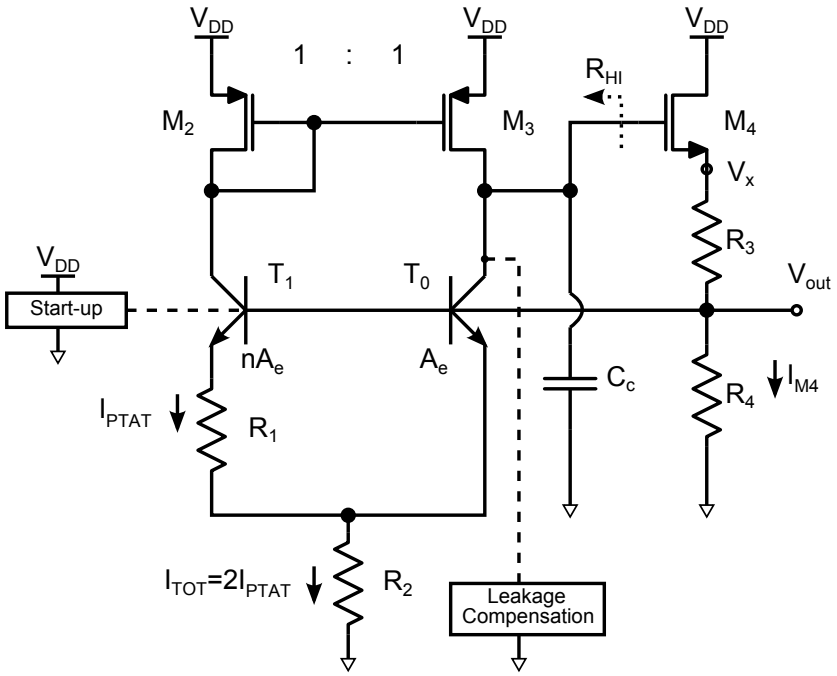

Fig. 5.1: Brokaw Bandgap

The working of this circuit is simple, applying the KVL (*Kirchhoff Voltage Law*) it results:

$$V_{out}(T) = V_{BE_0}(T) + R_2(2I_{PTAT}(T)) \tag{5.1}$$

now it's necessary to investigate V_{BE_0} and I_{PTAT} behaviors, this is made in Appendix. A.13.

We would like V_{out} to be insensitive to the absolute Temperature, so:

$$\frac{\partial V_{out}(T)}{\partial T} = \frac{\partial V_{BE_0}(T)}{\partial T} + 2R_2\frac{\partial I_{PTAT}(T)}{\partial T} = 0 \tag{5.2}$$

and substituting Eq. A.56, Eq. A.58 it results:

$$\frac{\partial V_{out}(T^* = 300K)}{\partial T} \approx -2 \times 10^{-3} + 2\frac{R_2}{R_1}\frac{k}{q}ln(n) = 0 \tag{5.3}$$

so we calculate R_2 as:

$$R_2 = \frac{2 \times 10^{-3} R_1 q}{2k \cdot ln(n)} \tag{5.4}$$

Now V_{out} is insensitive to the Temperature (in a first approximation) and it results:

$$V_{out}(T = 300K) \approx V_{G0} = 1.2V \tag{5.5}$$

The value of R_1 fixes the total current consumption of the Bandgap:

$$I_{TOT} = 2I_{PTAT} + \frac{V_{out}}{R_4} \approx 2I_{PTAT} \tag{5.6}$$

so we size R_1 as:

$$R_1 = \frac{|\Delta V_{BE}|}{I_{PTAT}} = \frac{1}{I_{PTAT}} \frac{kT}{q} ln(n) \tag{5.7}$$

The starting point to design the Bandgap is using Eq. 5.7 and Eq. 5.4, we have assumed that $\frac{\partial V_{BE}}{\partial T}(T^* = 300K) \approx -2mV/K$ and also the physical resistances $R_1 - R_2$ have their own temperature coefficient, so the combination of values $R_1 - R_2$ that makes true the Eq. 5.3 must be determined with the help of the simulator.

At high temperatures the transistor with more emitters (T_1) has more leakage current towards the substrate respect the one-emitter transistor (T_0), so we should design a specific block to ensure the leakage compensation. To match leakage a starting point is to put a off-transistor, with $n - 1$ emitters, with the drain connected with that of T_0 (like T_4 in Figure 5.10). Therefore since it is off it has effect only with its leakage current to the substrate, however a correct matching circuit is found only with simulations and a very nice layout. The leakage compensation ensures a lower drift in temperature of $V_{out}(T)$, so a curve similar to a "bell", as in Figure 5.2.

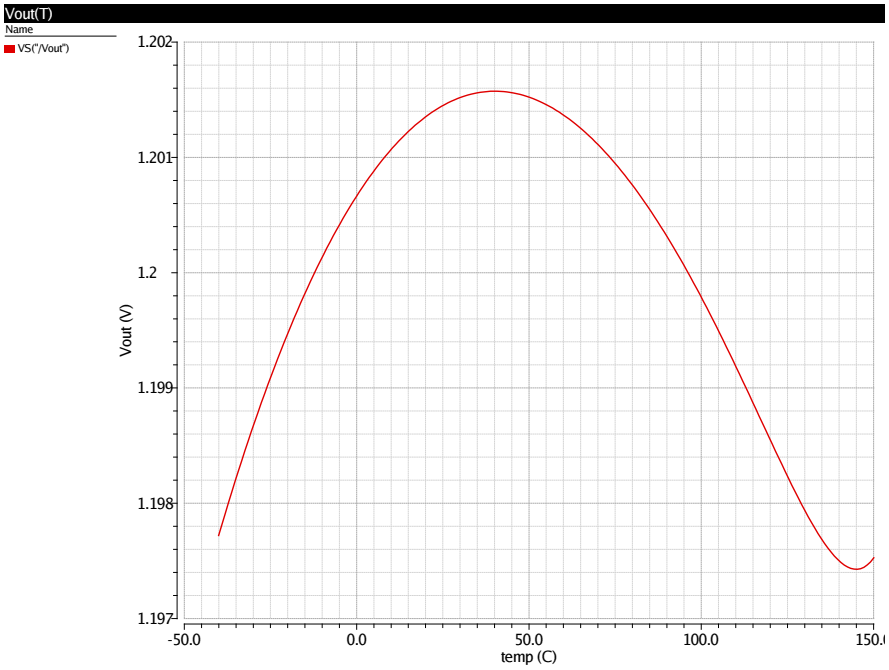

Fig. 5.2: V_{out}, sweep in temperature

If we want to have a voltage $V_{out} \neq 1.2V$ it's simple because we can take as output voltage the V_x (Figure 5.1):

$$V_x = \left(1 + \frac{R_3}{R_4}\right) V_{out} \tag{5.8}$$

or we can scale down V_{out} with a voltage divider as in Figure 5.10.

Since the Bandgap is "self-polarized" there are 2 suitable DC operating points: the first (the desired) is when $V_{out} \approx 1.2V$ (or scaled) and $I_{PTAT} \neq 0$, the second is with $I_{PTAT}, V_{out} = 0$. To avoid the second operating point it should be designed a specific start-up circuit.

As regard the minimum supply headroom ($V_{DD(min)}$) to correct regulate V_{out}, consider to have a NMOS-output Bandgap (that of Figure 5.1) and $V_{out} = 1.2V$ so $R_3 = 0$:

$$V_{DD(min)}\Big|_{N-out} = 1.2 + |V_{GS_{M4}}| + |V_{DS_{sat.(M3)}}| \tag{5.9}$$

The supply headroom of circuit in Figure 5.10 is shown in Figure 5.3, a Bandgap with PMOS-output has a lower supply headroom.

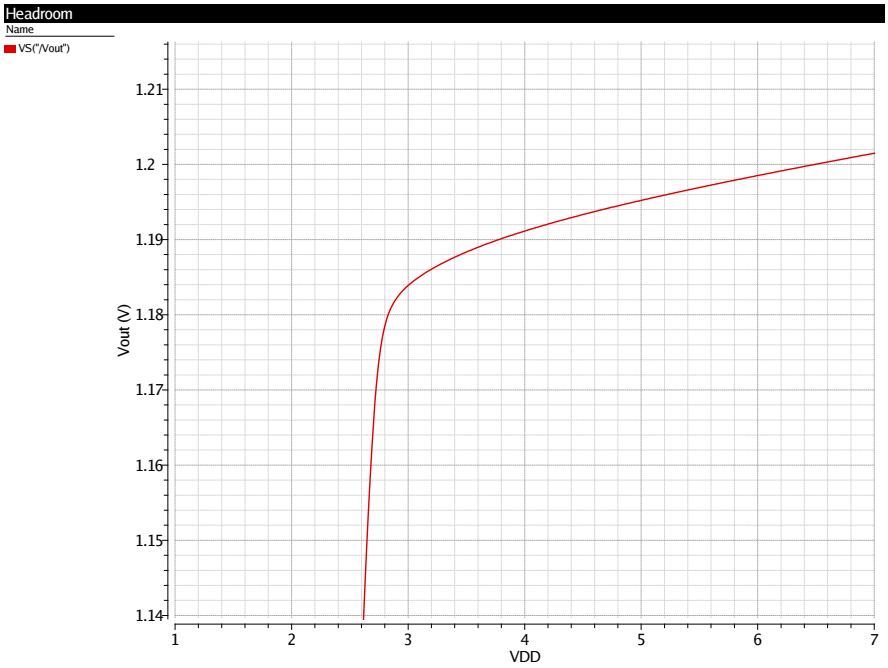

Fig. 5.3: Supply Headroom, NMOS-output

5.1 Frequency Compensation

The circuit works in closed Loop to regulate the output voltage V_{out}. There are 2 Loops: a *Negative* Loop due to the signal path of transistor T_0 and a *Positive* Loop due to the path of transistor T_1. The Negative Loop has a higher Loopgain module: T_0 has a higher transconductance than T_1 because it has not the degeneration resistance R_1, so the overall circuit is regulated from a *Negative* Loop. In order to guarantee the stability of the circuit we have to calculate the Loopgain.

First we calculate the transconductance $\frac{i_{HI}}{V_x}$, we know that the resistance seen into the emitter of a BJT is about $R_e \approx 1/g_m$, so making the KVL it results:

$$i_0 \left(\frac{1}{g_{m0}}\right) = i_1 \left(R_1 + \frac{1}{g_{m1}}\right) \tag{5.10}$$

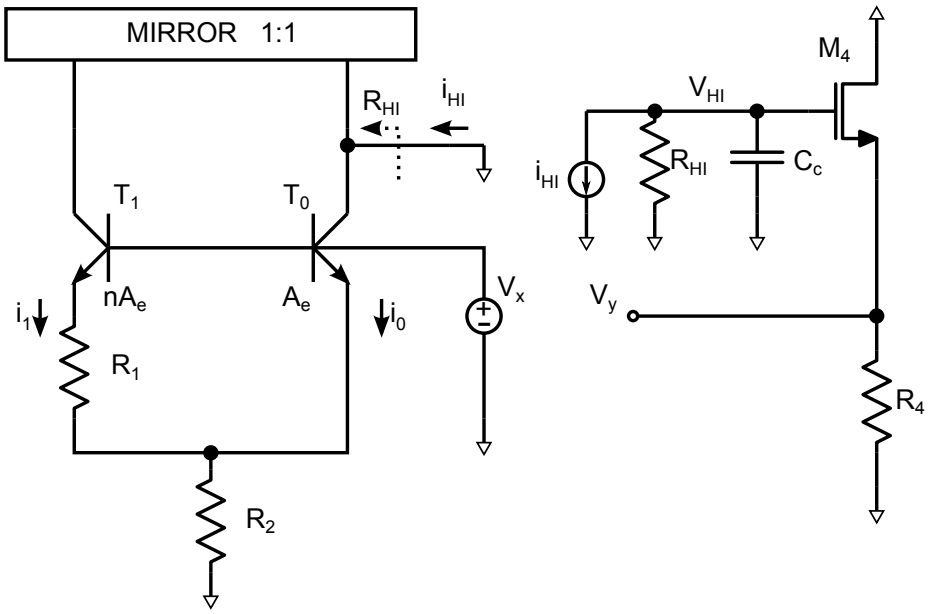

Fig. 5.4: Loopgain calculation with AC circuit

We know that $g_m = \dfrac{qI_C}{kT}$, the transistors operates at equal currents $I_{C_0} = I_{C_1}$ so $g_{m0} = g_{m1}$, R_1 is calculated in Eq. 5.7, thus making this substitutions in Eq. 5.10 it results:

$$i_0 = i_1\big(1 + ln(n)\big) \tag{5.11}$$

Now we suppose that $R_2 \gg \dfrac{1}{g_m}, R_1$ (a strong degeneration), therefore the total current $i_0 + i_1$ is due to the voltage change across R_2 resulting from the voltage V_x at the common bases. That is:

$$i_0 + i_1 = \frac{V_x}{R_2} \tag{5.12}$$

The combination of Eq. 5.11 and Eq. 5.12 can be manipulated to find the transconductance

$$\frac{i_0 - i_1}{V_x} = \frac{i_{HI}}{V_x} = \frac{1}{R_2}\left(\frac{ln(n)}{2 + ln(n)}\right) \tag{5.13}$$

The current i_{HI} flows into a *H*igh-resistive *I*nternal node $R_{HI} = R_{o0}//R_{o3}$ and produces a voltage $V_{HI} = -i_{HI}R_{HI}$ that, thanks to the voltage buffer M_4, is the same as $V_y = V_{HI}$.

We can ensure a dominant pole-compensation of the Loop with the insertion of a capacitor C_c connected to the high-impedance internal node, in order to create a low-frequency pole. Therefore the total Loopgain has the form:

$$T(s) \approx -\frac{V_y}{V_x}(s) = \frac{R_{o0}//R_{o3}}{R_2}\left(\frac{ln(n)}{2 + ln(n)}\right)\left(\frac{1}{1 + sC_c(R_{o0}//R_{o3})}\right) \tag{5.14}$$

Note that the low-frequency Loopgain module does not depend on the current $I_{C_{0/1}} = I_{PTAT}$ at a first approximation, because $|T_{(DC)}| = \left((R_{o0}//R_{o3}) \propto \dfrac{1}{I_C}\right)\left(\dfrac{1}{R_2} \propto I_C\right)$, how-

ever the pole is proportional to $R_{o0}//R_{o3}$ so it moves with I_C. We can roughly estimate the unity-gain frequency f_c of the Loopgain:

$$\begin{aligned} f_c &= \left(\frac{ln(n)}{2+ln(n)}\right)\frac{1}{2\pi C_c R_2} \\ &= \left(\frac{ln(n)}{2+ln(n)}\right)\frac{I_{PTAT}}{2\pi \times 10^{-3} T C_c} \end{aligned} \tag{5.15}$$

where in Eq. 5.15 we have substituted $R_2 = \dfrac{1\times 10^{-3}T}{I_{PTAT}}$ (found substituting Eq. 5.7 into Eq. 5.4). The Loopgain of circuit in Figure 5.10 is shown in Figure 5.5, a manual estimation of $f_c\Big|_{I_{PTAT}=1\mu A} \approx 5.3kHz$ and the simulated value is about $f_c \approx 4.6kHz$, in good agreement.

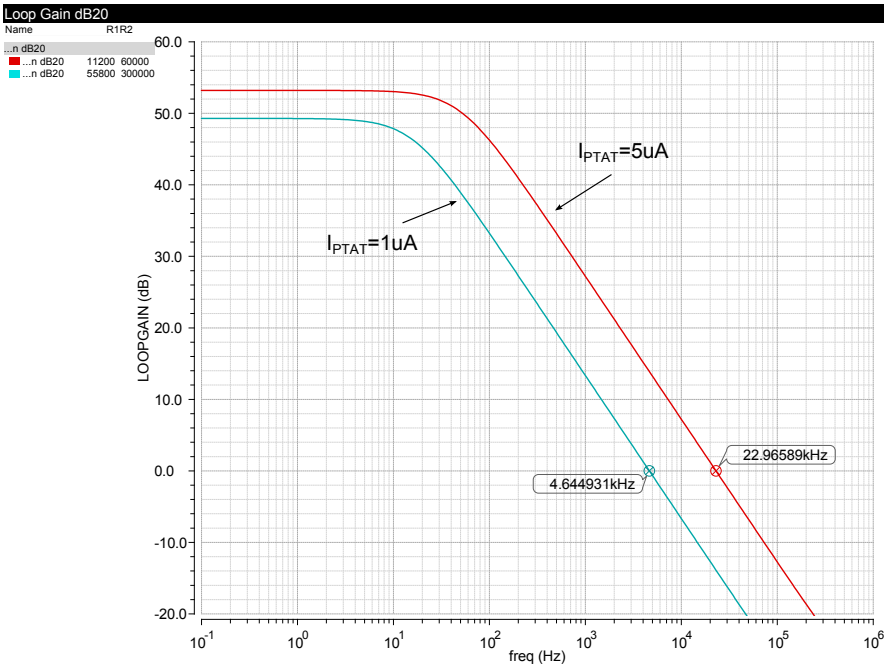

Fig. 5.5: Loopgain, $I_{PTAT} = 1-5\mu A$, $C_c = 50pF$, $n = 8$, $T = 300K$

5.2 Noise

It's very important to understand and analyze the Noise produced by the Bandgap, the Noise sources are transistors and resistors and are highlighted in Figure 5.6 (the Shot Noise of the base current of $T_{0/1}$ has been neglected in this analysis).

R_2 Noise

R_2 produces a Noise signal that is a *common mode signal*, so it is deleted in the R_{HI}-node and it does not propagate to the output (the Noise path is very similar to that of Figure 4.4). However the two paths through T_0 and T_1 are not completely symmetric so the Noise at output is not zero, but it is so small that it can be surely neglected.

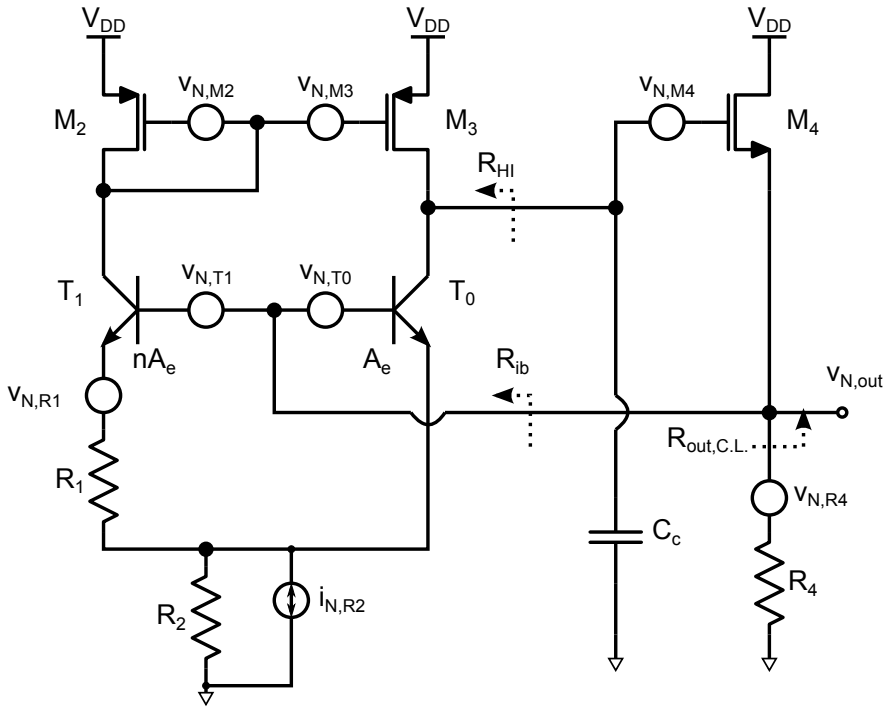

Fig. 5.6: Bandgap Noise sources

$T_1/T_0/M_2/M_3$ Noise

The Noise produced by these transistors is transferred to the output with a *Closed-Loop* transfer function, so the voltage gain to the output is of the form:

$$\frac{v_{N,out}}{v_{N,M_x/T_x}}(s) = A_{v,C.L.}(s) = \frac{A_{v,O.L.}(s)}{1+T(s)} \tag{5.16}$$

generally it's a low voltage gain and it starts to decrease when the Loopgain reaches the unitary-gain frequency f_c. Therefore the Noise of these transistors is *white* and it starts to decrease when $f \geq f_c$, if we add the 4 contributions this Noise is not negligible, however it is not the main Noise source.

M_4 Noise

$v_{N,M4}$ "sees" a closed-Loop transfer function like Eq. 5.16, now $A_{v,O.L.}(s) \approx 1$ because M_4 is a voltage buffer, thus the total transfer function is just:

$$\frac{v_{N,out}}{v_{N,M_4}}(s) \approx \frac{1}{1+T(s)} \tag{5.17}$$

so the Noise is strongly attenuated for $f < f_c$ and it is unitary transferred to the output for $f \geq f_c$, this Noise source however is negligible.

R_4 Noise

First we explain how is the Bandgap output resistance R_{out}, the Bandgap provides a constant and regulated V_{out} so it is itself a voltage regulator, we know that a voltage regulator has a very low output resistance. The *Open-Loop* output resistance is

$$R_{out,O.L.}(s) = R_{ib}//\frac{1}{g_{m4}} \approx \frac{1}{g_{m4}} \tag{5.18}$$

and the *Closed-Loop* output resistance is

$$R_{out,C.L.}(s) \approx \frac{1/g_{m4}}{1+T(s)} \tag{5.19}$$

R_4 is a resistance of the order of $M\Omega$ because we want a small DC current $I_{M4} = \frac{V_{out}}{R_4}$, so it produces a lot of Noise. Fortunately the voltage transfer function to output is very low:

$$\frac{v_{N,out}}{v_{N,R_4}}(s) = \frac{R_{out,C.L.}(s)}{R_{out,C.L.}(s)+R_4} \ll 1 \tag{5.20}$$

therefore the Noise of this big resistance is negligible.

R_3, R_4 Divider If V_{out} is scaled up with the use of the feedback divider R_3, R_4 (Figure 5.1), these resistances play the role of R_1, R_2 in the total regulator (Figure 3.4), so as it is explained in Appendix. A.6:

$$\left|\frac{v_{N,out}}{v_{N,R_4}}\right|(s) \approx \frac{R_3}{R_4} \tag{5.21}$$

and

$$\left|\frac{v_{N,out}}{v_{N,R_3}}\right|(s) \approx 1 \tag{5.22}$$

at least until $|T(s)| \gg 1$.
This Noise is very deleterious, so a Bypass capacitor is needed (as explained in Par. 3.3.1).

R_1 Noise

First we calculate the Open-loop transfer function $\left.\frac{v_{N,out}}{v_{N,R_1}}(s)\right|_{O.L.}$.

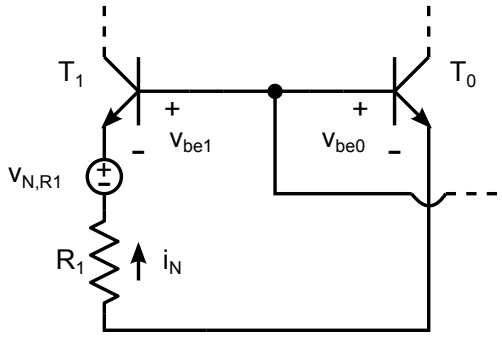

Fig. 5.7: R_1 Noise, circuit zoom

Neglecting R_2 and considering $g_{m1} = g_{m0}$, the Noise v_{N,R_1} produces a noise current that circulates in the "internal" network

$$i_N = \frac{v_{N,R_1}}{R_1 + \frac{2}{g_{m0}}} \tag{5.23}$$

Applying KVL to the internal network we may calculate

$$\begin{aligned} |\Delta v_{be}| = |v_{be_1} - v_{be_0}| &= R_1 i_N - v_{N,R_1} \\ &= \left(\frac{R_1}{R_1 + \dfrac{2}{g_{m0}}} - 1 \right) v_{N,R_1} \end{aligned} \tag{5.24}$$

and since $g_{m0} = \dfrac{qI_{PTAT}}{kT}$ and R_1 is expressed by Eq. 5.7, we can manipulate Eq. 5.24 and rewriting as

$$|\Delta v_{be}| \approx \left(\frac{2}{2 + ln(n)} \right) v_{N,R_1} \tag{5.25}$$

Now referring to Figure 5.4 we easily found:

$$\left| \frac{v_{N,out}}{v_{N,R_1}} \right| (s) \Big|_{O.L.} = g_{m0}(R_{o0} // R_{o3}) \left(\frac{2}{2 + ln(n)} \right) \left(\frac{1}{1 + sC_c(R_{o0} // R_{o3})} \right) \tag{5.26}$$

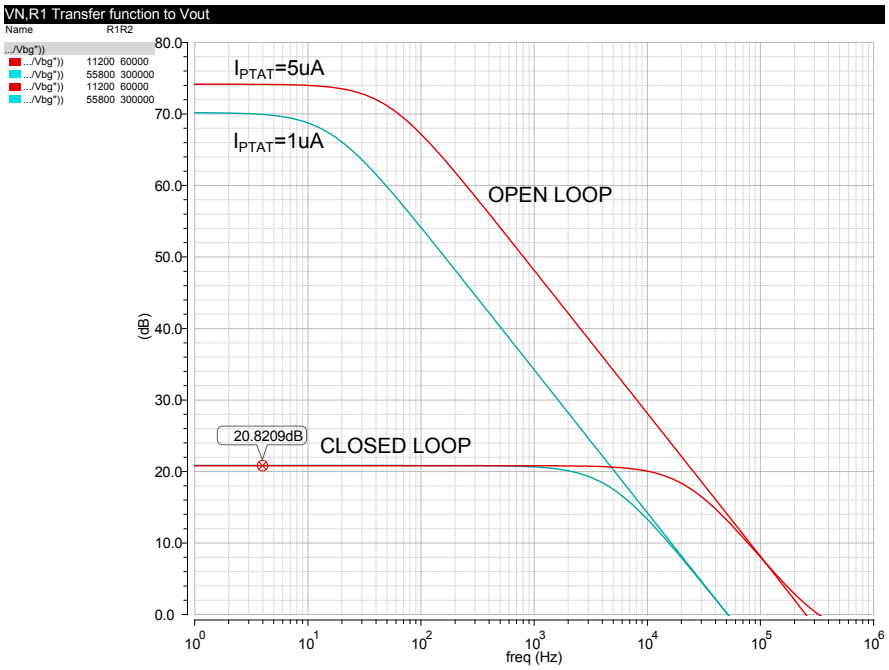

Fig. 5.8: $v_{N,out(R_1)}$

Therefore the Closed-Loop transfer function has the form of Eq. 5.16 and when $|T(s)| \gg 1$, Eq. 5.26 reduces to

$$\begin{aligned} \left| \frac{v_{N,out}}{v_{N,R_1}} \right| (s) \Big|_{C.L.,|T(s)| \gg 1} &\approx g_{m0} R_2 \frac{2}{ln(n)} \\ &\approx 1 \times 10^{-3} \frac{q}{k} \frac{2}{ln(n)} \\ &\approx 11.6 \frac{2}{ln(n)} \end{aligned} \tag{5.27}$$

This is a very important and curious result because the transfer function is *independent* of temperature and of all other parameters (n appears with the logarithm so has a small impact). If we consider $n = 8$ so $ln(n) \approx 2$, it results $\left|\frac{v_{N,out}}{v_{N,R_1}}\right| \approx 21dB$, therefore the Noise at the output produced by R_1 is that of a resistance of value $100R_1$ (!). This is the main contribution to the total output Noise.

Total Noise

All contributions explained above form the total output Noise $v_{N,out(TOT)}$, the Noise of most of contributions ($R_1/T_1/T_0/M_2/M_3$) decreases when $f \geq f_c$ so when $|T(s)| \leq 1$, therefore is important to have the smaller as possible bandwidth (f_c) of the Loopgain. However this is not simple because (see Eq. 5.15) to decrease the band we have two choices: decrease the I_{PTAT} or increase C_c. Decreasing I_{PTAT} is to avoid because we increase the Noise produced by all resistances and all transistors, we can increase C_c but for an integrate capacitor there are some limits on the value that can be integrated, we can assume that the biggest integrated $C_{c(max)} \approx 50pF$. However if we give to the customer the possibility to put an external capacitor $C_c \geq 1nF$, we can easily filter all the Noise.

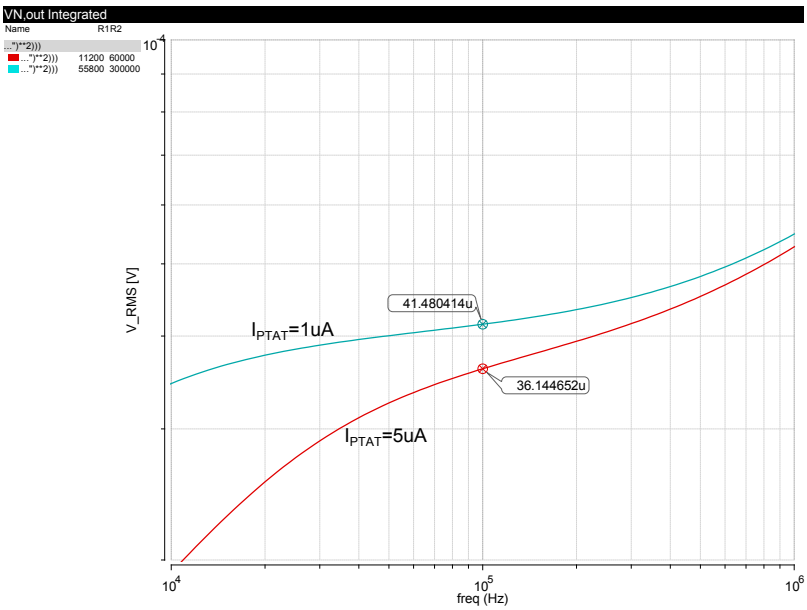

Fig. 5.9: $v_{N,out(TOT)}$ Integrated, $I_{PTAT} = 1 - 5\mu A$, $C_c = 50pF$

component	% of $v^2_{N,out(TOT,INT.)}$
R_0	46.3
T_0	13.3
T_1	11.4
M_7	5.5
M_6	5.0
M_5	5.0
R_7	4.5
R_8	4.5
others	4.5

Tab. 5.1: Components are referred to the circuit in Figure 5.10

The Noise budget for the Bandgap is $V_{N,BG(INT.)} \leq 13\mu V_{RMS}$ as explained in Par. 4.3.1, with a $C_c = 50pF$ we don't reach the target and varying I_{PTAT} the Noise varies slightly. Thus this simple Bandgap with integrate C_c is not good for our purpose.

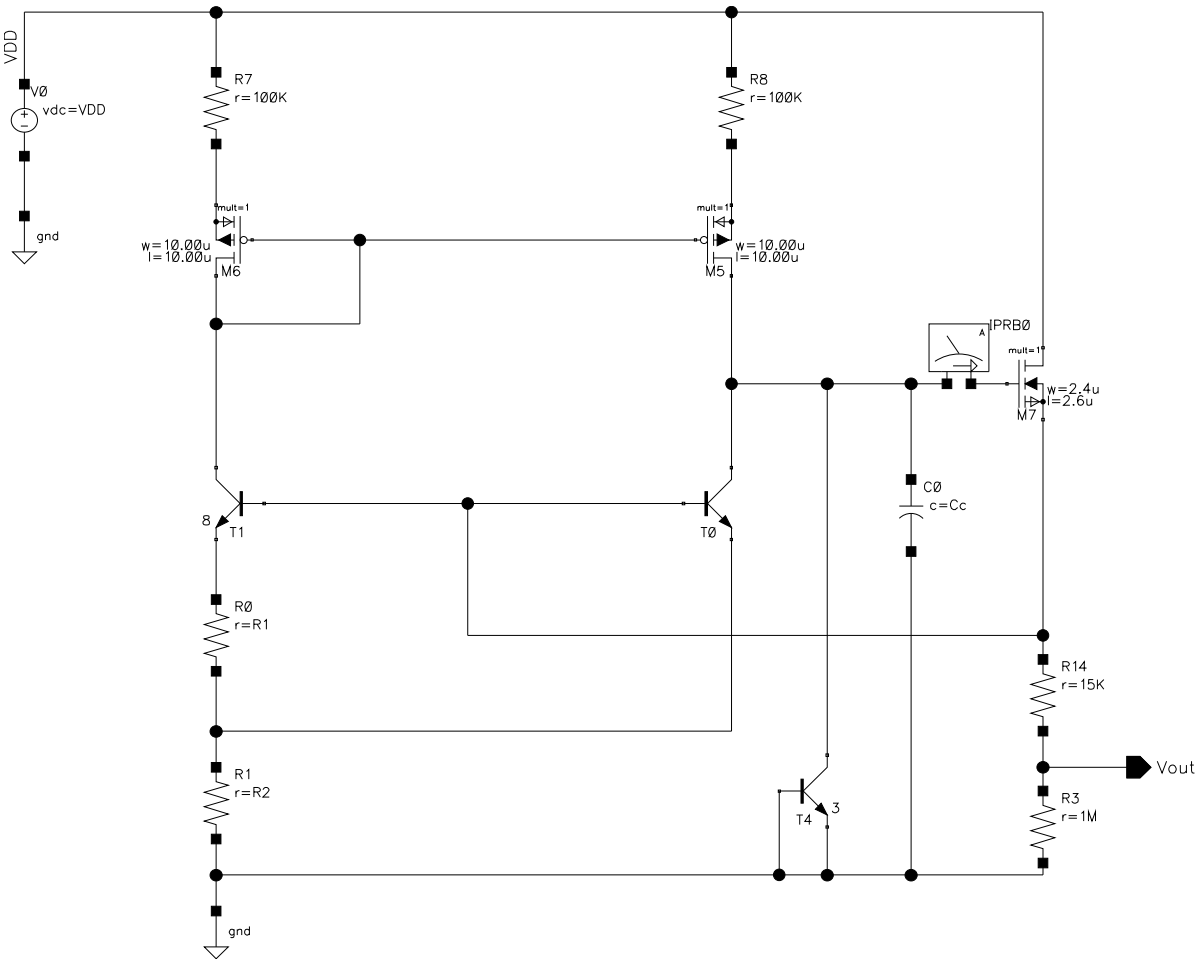

Fig. 5.10: Brokaw Bandgap N-output

5.3 Proposed Bandgap

To decrease the Noise the idea is to scale down all the Noise produced by the previous Bandgap and further filtering the output. To scale down the Noise by a 2 factor and maintaining $V_{out(DC)} = 1.2V$ it's necessary to have a Bandgap that regulates a "High-voltage" $V_{BG(DC)} = 2.4V$. Then we may insert a capacitor C_o at the output for filtering, because now we have a high-impedance output node $R_{out} \approx R_x//R_x = R_x/2$.

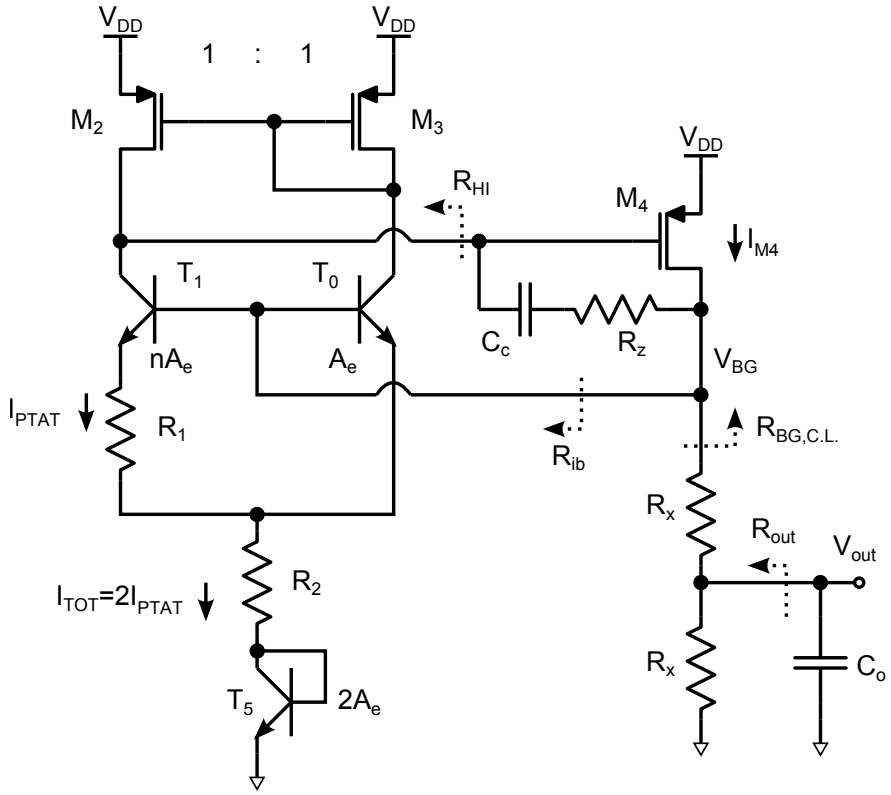

Fig. 5.11: Bandgap "High Voltage " P-output

I choose a PMOS-output because the Bandgap requires a lower Supply-Headroom ($V_{DD(min)}$) than the NMOS-output (for Eq. 5.29 think to make "High-Voltage" the circuit in Figure 5.1):

$$V_{DD(min)}\Big|_{P-out} = 2.4 - V_{BE_{T0}} + V_{CE_{sat.(T0)}} + |V_{GS_{M3}}| \tag{5.28}$$

$$V_{DD(min)}\Big|_{N-out} = 2.4 + |V_{GS_{M4}}| + |V_{DS_{sat.(M3)}}| \tag{5.29}$$

thus $V_{DD(min)}(P) < V_{DD(min)}(N)$. The designed Bandgap has $V_{DD(min)} \approx 4V$.

The manual design of the Bandgap is essentially the same explained in Par. 5, the output voltage is $V_{out} = \dfrac{V_{BG}}{2}$, considering 2 equal resistances of value R_x. Choosing the value of R_1 as in Eq. 5.7 we choose the current I_{PTAT} and so the total current consumption $I_{TOT} = 2I_{PTAT} + 1.2/R_x \approx 2I_{PTAT}$. The circuit regulates V_{BG}:

$$\begin{aligned} V_{BG}(T) &= V_{BE_0}(T) + R_2(2I_{PTAT}(T)) + V_{BE_5}(T) \\ &\approx 2V_{BE_0}(T) + R_2(2I_{PTAT}(T)) \end{aligned} \tag{5.30}$$

note that to match $V_{BE_0}(T) = V_{BE_5}(T)$ is necessary that T_5 has $A_{e5} = 2A_{e0}$ because $I_{C_5} = 2I_{C_0}$. R_2 is calculated to make $\dfrac{\partial V_{BG}(T^* = 300K)}{\partial T} = 0$ but now the voltage change across R_2 has to compensate $2V_{BE_0}$ so

$$R_2 = \frac{2 \times 10^{-3} R_1 q}{k \cdot ln(n)} \tag{5.31}$$

Therefore V_{BG} is insensitive to the Temperature (in a first approximation) and it results:

$$V_{BG}(T = 300K) \approx 2V_{G0} = 2.4V \tag{5.32}$$

As a result

$$V_{out}(T = 300K) = V_{BG}/2 = 1.2V \tag{5.33}$$

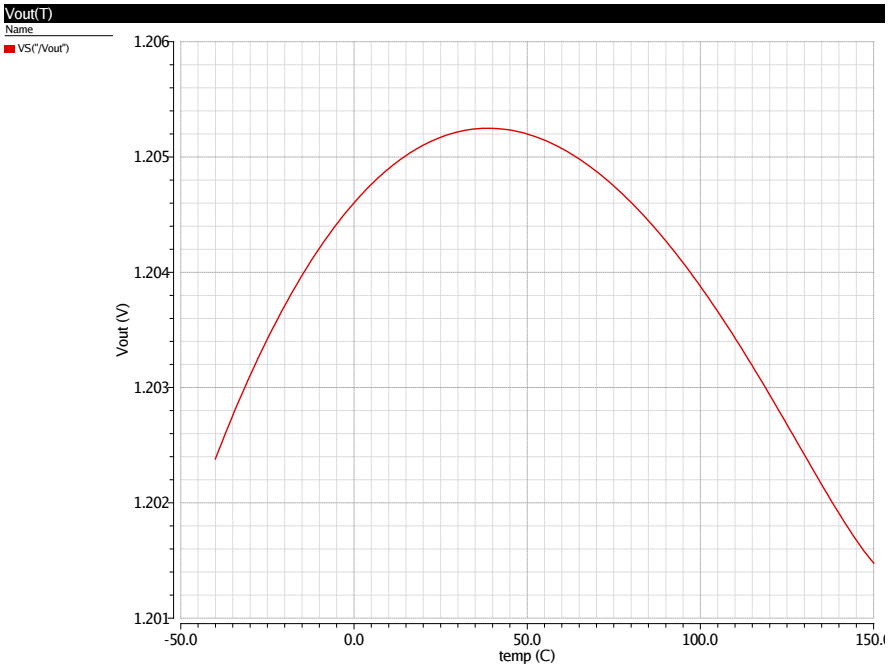

Fig. 5.12: $V_{out}(T)$, designed Bandgap

5.3.1 Frequency Compensation

The frequency analysis and the Loopgain calculation is essentially the same explained in Par. 5.1, the only difference is that the output stage is a voltage gain stage (CS-stage) so the Loopgain is higher. In order to create a low-frequency pole we can exploit the *Miller* effect to "increase" the capacitor, the voltage gain of the CS-stage M_4 is the same as Eq. 4.39 (Par. 4.2.1) and to eliminate the zero we choose a $R_z = 1/g_{m4}$. So the Loopgain results:

$$T(s) \approx \frac{R_{o1}//R_{o2}}{R_2} \left(\frac{ln(n)}{2 + ln(n)} \right) A_{v4(LF)} \left(\frac{1}{1 + sC_c A_{v4(LF)}(R_{o1}//R_{o2})} \right) \tag{5.34}$$

where $A_{v4(LF)} = g_{m4}\big(R_{o4}//(R_{ib}//2R_x)\big)$ (at low-frequency).

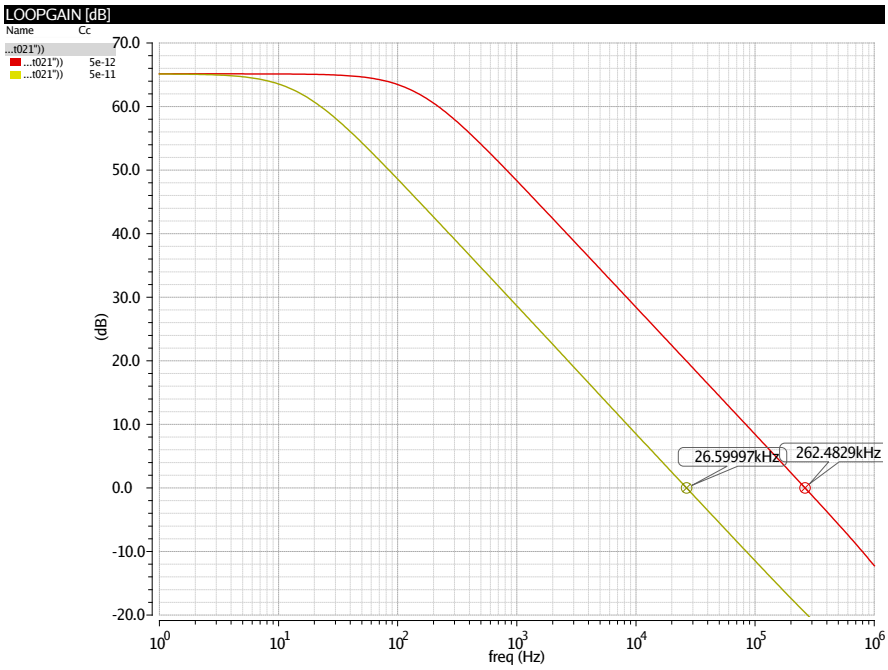

Fig. 5.13: Loopgain of designed Bandgap, $I_{TOT} \approx 16\mu A$, $C_c = 5 - 50pF$

The output capacitor C_o doesn't have effect (at a first approximation) on the Loopgain because, even when C_o shorts one R_x, the node $V_{BG}(s)$ still "sees" a high-impedance path to ground $R_{ib}//R_x$. Therefore to guarantee a 1-pole Loopgain and filter the Noise at the output are two decoupled problems.

5.3.2 Noise

The Noise measured at V_{BG} is approximately the same as the previous Bandgap (Par. 5.2, except for the noise produced by R_x, R_x), transistor M_4 is not a voltage buffer so its Noise is different but it's not a main Noise source, different is for R_1 Noise. v_{N,R_1} "sees" a transfer function to V_{BG} which is proportional to R_2 (Eq. 5.27), now R_2 is doubled so $\left|\frac{v_{N,BG}}{v_{N,R_1}}\right| \approx 11.6\frac{4}{ln(n)}$. However there is a down-scale to V_{out}

$$\frac{v_{N,out}}{v_{N,BG}} = \frac{1}{2} \tag{5.35}$$

so the Noise produced by transistors is decreased and the Noise produced by R_1 is about the same as Eq. 5.27. Now we analyze the Noise of R_x, R_x and the effect of C_o (a comparison with or without C_o is in Figure 5.14, make attention to the linear and logarithmic scale).

- without C_o

  Consider R_x, R_x 2 resistances of the order of few $M\Omega$, $R_{BG,C.L.}$ is a low-impedance node (at least until $|T(s)| \gg 1$) so we consider $R_{BG,C.L.} \ll R_x$. Thus it is as the two resistances are in parallel and at the output node we take all the Noise produced by an equivalent resistance of value $R_x/2$: $v_{N,out} \approx v_{N,R_x/2}$. This is a quite high Noise, because $R_x/2$ is a big resistance, comparable with that of R_1.

- with C_o

  Fortunately the output node is a high-impedance node $R_{out} = (R_x + R_{BG,C.L.})//R_x \approx R_x/2$ so this allows us to insert a capacitor C_o to create a low/medium-frequency pole to filter Noise:

$$f_o = \frac{1}{2\pi C_o R_x/2} \tag{5.36}$$

  This is a very good thing because with C_o we filter completely all the Noise produced by the Bandgap, however we cannot exceed values of few $M\Omega$ for R_x and about $C_{o,(max)} \approx 50pF$ so we cannot pull f_o to a frequency arbitrarily low.

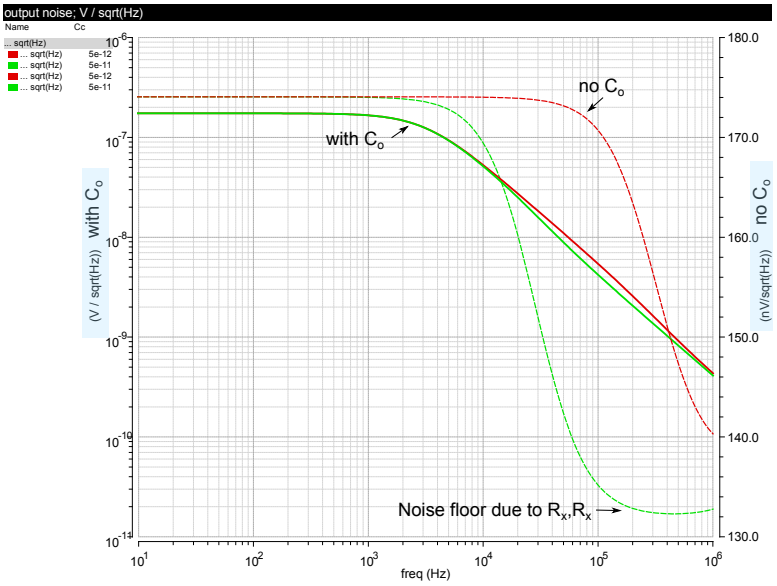

Fig. 5.14: $v_{N,out}$ Spot Noise, $I_{TOT} \approx 16\mu A$, $n = 20$, $C_c = 5-50pF$, $C_o = 50pF$, $R_x = 2M\Omega$

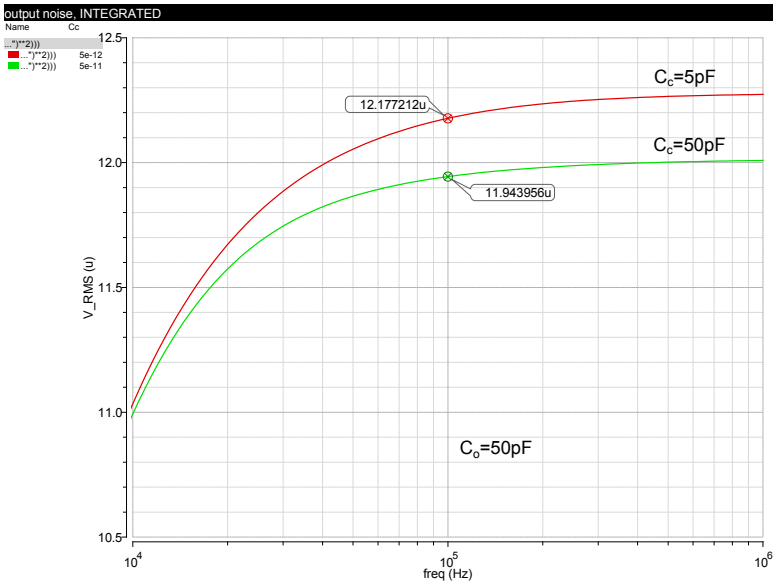

Fig. 5.15: $v_{N,out}$ Integrated Noise, $I_{TOT} \approx 16\mu A$, $n = 20$, $C_c = 5 - 50pF$, $C_o = 50pF$, $R_x = 2M\Omega$

Noise contributions are such distributed:

component	% of $v^2_{N,out(TOT,INT.)}$
R_{32}	27.5
R_{33}	27.5
R_0	24.0
T_0	5.5
T_1	5.0
M_5	5.0
M_6	4.5
others	2.0

Tab. 5.2: Components are referred to the circuit in Figure 5.16

As we can see in Figure 5.14/Figure 5.15 the unity-gain frequency of the Loop-gain has a marginal effect on the Noise so we can use a smaller $C_c = 5pF$ and a bigger capacitor $C_o = 50pF$ has been chosen. The Noise Budget is reached because $V_{N,out(INT.)} \approx 12.2\mu V_{RMS}$.

In this chapter a "high-voltage" Bandgap has been explained and designed, it's also possible to use a classical Bandgap (as the first explained) and scale down the output voltage to $V_{out} < 1.2V$. This solution is suitable if the *Error Amplifier* can work with low $V_{i,cm}$ like an OTA with P-input couple. However the Noise of a "Low-Voltage" Bandgap should be comparable to the "High-Voltage" version, in addition the resistor divider of the regulator is a little noisier (Eq. 3.33) because, to regulate at the same voltage, $1/\beta_F$ is higher.

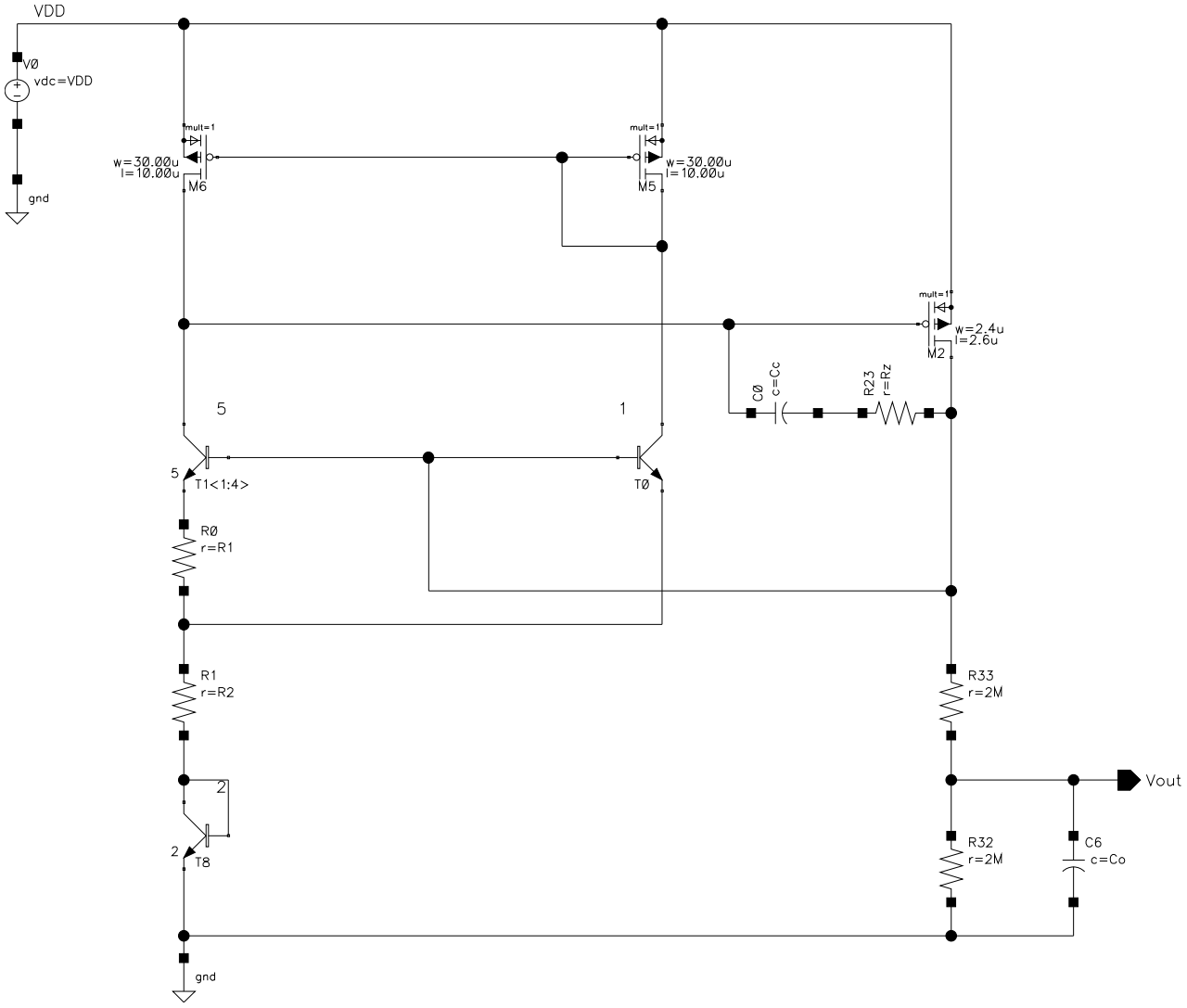

Fig. 5.16: Designed Bandgap "High-Voltage" with P-output

Chapter 6

Conclusions

This work starts to explain some useful knowledge on the electronic Noise, its behavior and link between the frequency and time domain, and some theoretical concepts on Noise simulation and analysis. Then the main focus of the thesis is the feasibility study of a low-noise LDO voltage regulator with $V_{N,out} \leq 20\mu V_{RMS}$ integrated in the bandwidth $10Hz \leq f \leq 100kHz$, an example of low-noise LDO is explained and designed. To reach low-noise performance we have to consider the effect of the Voltage Reference, the Error Amplifier, the Voltage Feedback and the Regulation Loop. In Chapter. 3 is explained the Noise produced by the voltage feedback and the effect of the regulation loop on the Noise performance, several methods to act on the regulation loop for decreasing the Noise are analyzed. Chapter. 4 regards the Error Amplifier and the designed OTA is explained and simulated. At last, Chapter. 5, takes into account the Noise of the voltage reference that is the main noise source of a voltage regulator, a suitable low-noise Bandgap reference has been designed.

6.1 Noise Performance of the Designed LDO Voltage Regulator

The main designed blocks have these Noise performance:

- $V_{N,out(BG)_{INTEGRATED}} \approx 12.2\mu V_{RMS}$
- $V_{N,in(EA)_{INTEGRATED}} \approx 8.8\mu V_{RMS}$

the overall voltage regulator produces this Noise:

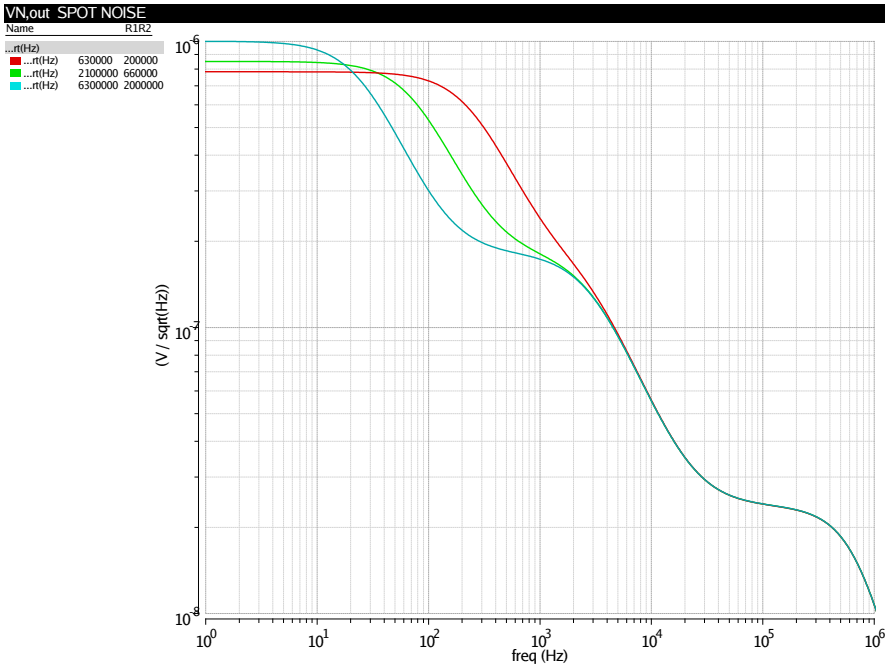

Fig. 6.1: $v_{N,out}$ Spot Noise, $V_{OUT} = 5V$, $I_L = 1A$, $C_c = 1\mu F$, $C_B = 1nF$

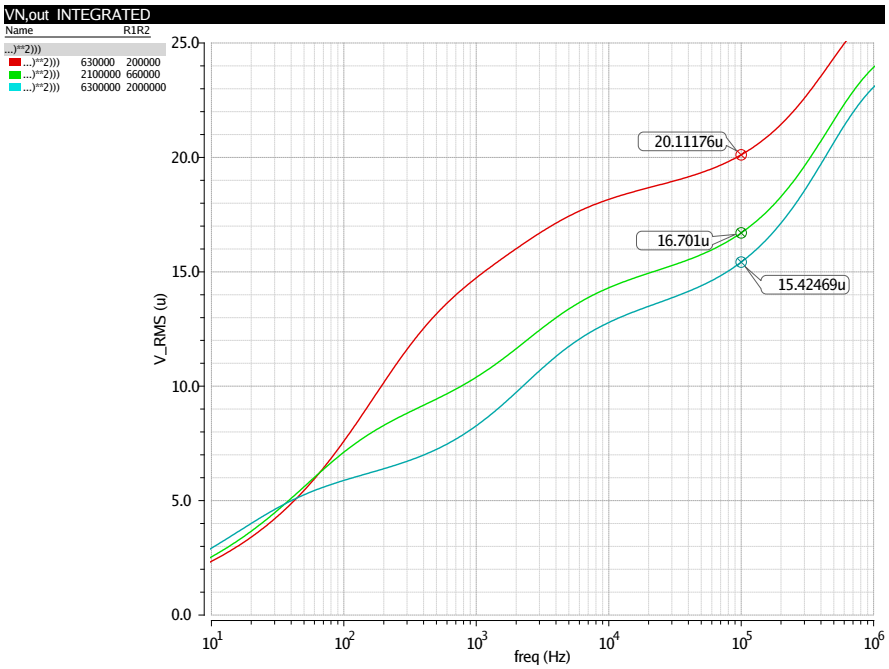

Fig. 6.2: $v_{N,out}$ Integrated Noise, $V_{OUT} = 5V$, $I_L = 1A$, $C_c = 1\mu F$, $C_B = 1nF$

The effect of the voltage divider changes the Spot Noise figure, which in turn influences the Integrated Noise, with a regulated voltage of $V_{OUT} = 5V$ to reach the Noise target values of $R_1 \geq 2.1M\Omega$, $R_2 \geq 600k\Omega$ are suitable (in order to inevitable leave few μV_{RMS} for *Flicker* Noise).

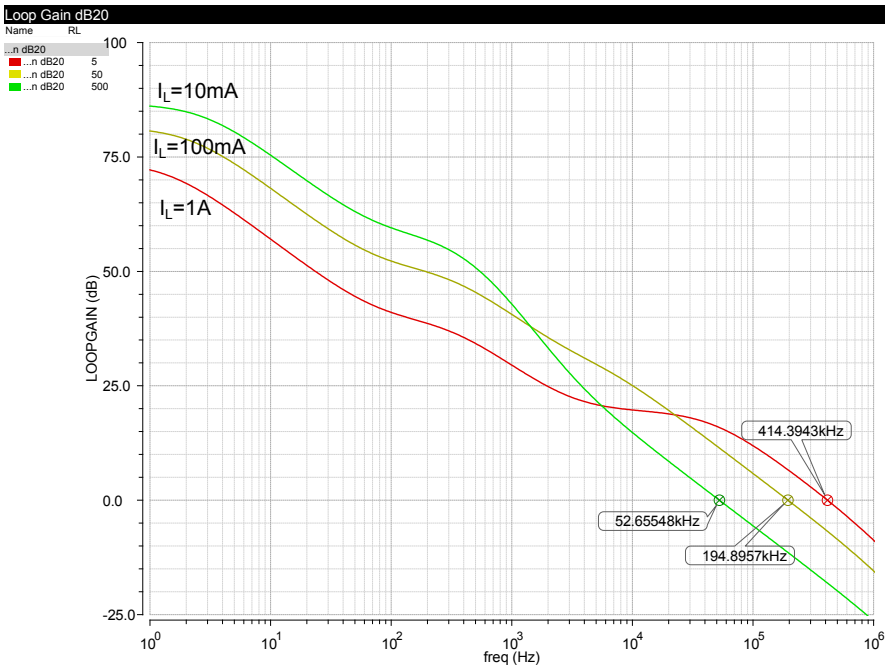

Fig. 6.3: Loopgain module, $V_{OUT} = 5V$, $C_c = 1\mu F$, $C_B = 1nF$, $R_1 = 2.1M\Omega$, $R_2 = 600k\Omega$

The regulator is well stable at all load currents with a good phase-margin $PM > 80°$.

6.2 Future Work

To increase Noise performance of an LDO we can take into account and analyze with more detail this options:

- Other **compensation schemes** may be studied: the smaller is the regulation bandwidth, the smaller is the output integrated noise. However there must be a trade-off with stability and with the speed of the temporal response.
- The use of a **current reference** instead of a voltage reference: we can set the correct regulated voltage at the input of the error amplifier so the regulation loop is closed in unitary feedback and we avoid the noise gain due to the feedback. The noise of the current reference has to be investigated.
- The use of a **Two-Stage Regulator** as explained in Par. 3.3.4.
- With an **Active Feedback** (Par. 3.3.2) we can reduce very much the noise produced by the voltage reference and the error amplifier, therefore these two last blocks may be less complex to design respect noise performance. Also dynamic performance like PSRR and step-response are improved, however the active feedback should be low-noise and the compensation of the regulation loop must be analyzed in detail.
- **Parallelizing Regulators** may decrease the output noise, it's also possible to parallelize regulators that have specific functions (low-noise, high output current etc...).
- To reduce very much $1/f$-noise we may use **Chopper stabilization** techniques. Chopper stabilization modulates the low frequency noise and offset components to higher frequencies by a mixing operation, followed by low-pass filtering. Further information and a full explanation can be found in [12].

Appendix A

Appendix

A.1 Flicker Noise Divergence

The term $ln\frac{f_2}{f_1}$ suggests that the Power will be infinite, but obviously it's not possible that the power is infinite. If we measure the voltage or current, we don't see the signal diverge, so we have to investigate the problem under a physical side. Push the frequency to zero means that we are measuring the system for a time much long because $f_{min} = \frac{1}{T_{observation}}$, to reach a true DC signal ($f = 0$) we should measure the system for an infinite time, obviously this is not possible. In practice we are interested only at the time of use of the device, for example, a voltage regulator how long it will stay on? Few seconds or a full day? This time sets the minimum frequency that we can reach.

Example: we have a system affected only by Flicker Noise and the $f_{MAX} = 100kHz$, we know that the output current is noisy and:

$$i_{out,RMS} = \sqrt{\overline{i_{out}^2}} = \sqrt{\overline{i_{1/f}^2}} = \int_{f_{min}=1Hz}^{f_{MAX}} K_f \frac{1}{f} df = 1mA_{RMS}$$

if we vary the f_{min}, so the $T_{observation}$, how does the Noise vary?

$f_{min}[Hz]$	$T_{obs}[s]$	$i_{out,RMS}[mA]$
1	1	1
10^{-1}	10^1	1.52
10^{-3}	10^3	2.63
10^{-5}	10^5	3.39
10^{-6}	10^6	3.72

Note that $10^5 sec$ is about a day and $10^6 sec$ is about two weeks and the $i_{out,RMS}$ is increased of very little. This example can help to convince us that really the Flicker noise can't diverge any physical signal (voltage or current in electronics).

A.2 Noise Phase

A complete characterization in frequency of the Noise can be represented, like all signals, by two quantities: the *module* and the *phase*. The module was explained in Chapter 1 when we have illustrated Thermal, Shot and Flicker noise, but, the phase how it can be? Can we make some statistics on it?

We can expect that the phase is *random* because the noise module in frequency domain is well defined (think the module of thermal noise that is constant in frequency) so the uncertainty must be in the phase, otherwise we don't have a random waveform in time domain.

The best way to understand how is the phase is trying to realize some noise signals in time domain, starting from its characteristics in frequency domain: a well known module and some different phases.

We use a *constant* module in frequency as in Figure A.1 (it could be a Thermal or Shot noise spectrum):

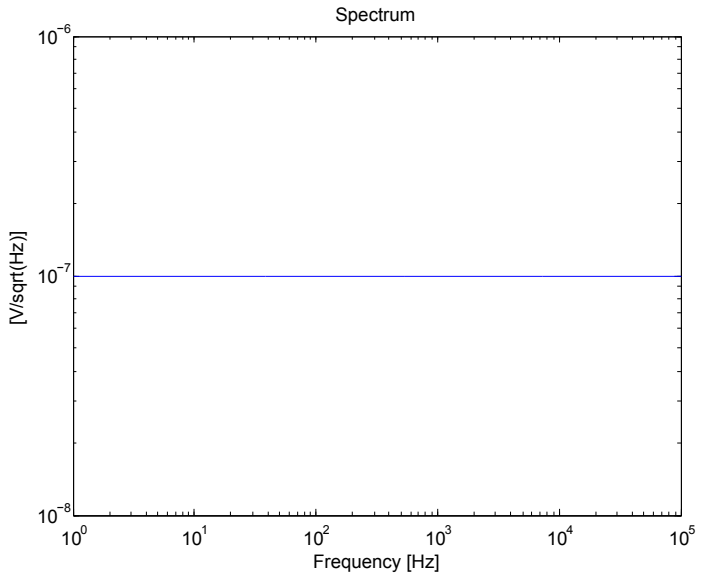

Fig. A.1: Noise spectrum module

the *RMS voltage*, that contain the information on the *Power*, is:

$$V_{RMS} = V_{level}\sqrt{f_{MAX} - f_{min}} \cong V_{level}\sqrt{f_{MAX}} \tag{A.1}$$

where V_{level} is in this case $10^{-7}\frac{V}{\sqrt{Hz}}$.

Now we try to associate three different phases and to discover the time domain realization.

Constant Zero Phase

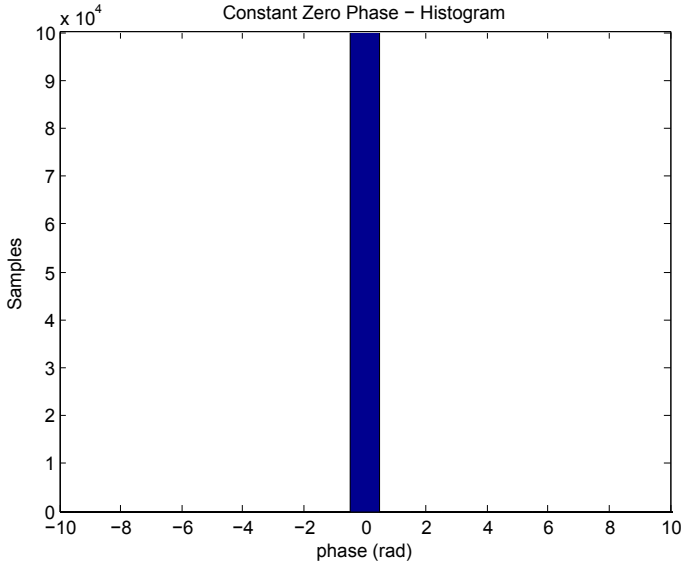

Fig. A.2: Constant zero phase

The realization in time domain with module and phase shown respectively in Figure A.1 and Figure A.2 is depicted in Figure A.3.

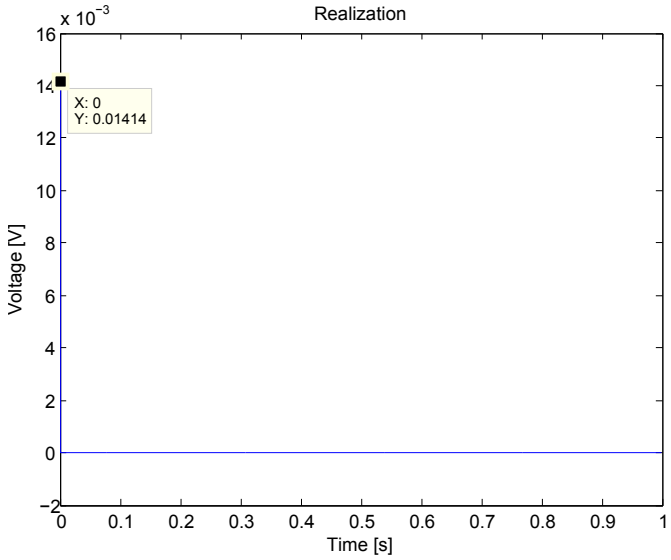

Fig. A.3: Realization in time domain

Obviously this signal can't be a true realization of noise (we can easily convince ourselves comparing Figure A.3 with Figure 1.1) because there is an impulse in the origin at $t = 0$ ($V_{\delta(t)} = V(1)$) and the rest of the signal is null $V(i) = 0$ for $i \neq 1$ (there are N samples).

The power (or equivalently the V_{RMS}), anyhow, must be conserved from frequency to time domain:

$$V_{RMS}\Big|_{time} = V_{RMS}\Big|_{frequency}$$

so we can calculate the amplitude of the impulse $V_{\delta(t)}$, we know that

$$V_{RMS}\Big|_{time} = \sqrt{\frac{\sum_N V(i)^2}{N}} = \sqrt{\frac{V_{\delta(t)}^2}{N}} \tag{A.2}$$

thus comparing Eq. (A.1) with Eq. (A.2):

$$V_{\delta(t)} = V_{level}\sqrt{N}\sqrt{f} \tag{A.3}$$

We could expect this time realization from the beginning because the *Fourier transform* of the *Dirac impulse* $\delta(t)$ has just a constant module and constant phase. This example use a null constant phase ($\angle = 0$), if we use another constant phase we obtain again an impulse at $t = 0$ but with a different amplitude, for example if we use $\angle = \pi$ the impulse will be $-V_{\delta(t)}$.

N.B. Eq. (A.2) assume that the mean value of the signal is null, $\overline{V(t)} = 0$, this is not obvious, indeed if we make a zoom at the null signal in Figure A.3 we could observe that the signal is slightly negative, this because the mean value results null. $\overline{V(t)} = 0$ because to make the realization I force the DC component $f(0) = 0$ because is realistic that Noise has a null mean value.

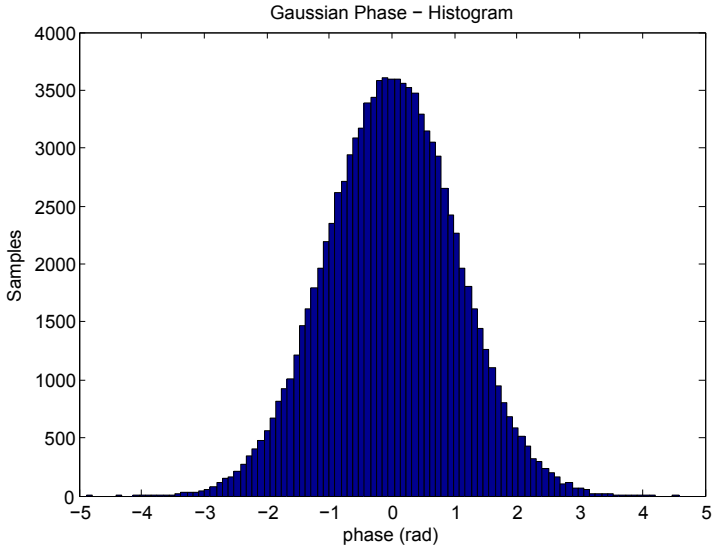

Fig. A.4: Gaussian phase $\sigma_{phase} = \pi/3$

Gaussian Phase

The phase for every frequency sample is created from a *gaussian distribution* (or *normal distribution*) with $\sigma_{phase} = \pi/3$, so about the 99.7% of the generated phase is between $\pm\pi$ because is in the band $-3\sigma < phase < +3\sigma$ therefore $-\pi < phase < +\pi$.

The realization in time domain with module and phase shown respectively in Figure A.1 and Figure A.4 is depicted in Figure A.5.

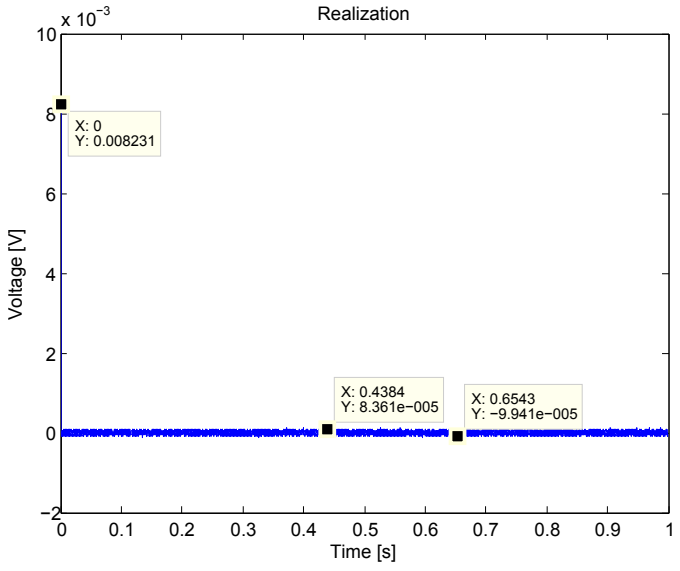

Fig. A.5: Realization in time domain

This signal $V(t)$ shows a band with random values, that may seem a noise, and an impulse in $t = 0$.

The impulse arises because of there are a lot of frequencies *in phase* (or *quasi in phase*) with $\angle \simeq 0$ and so there are the same conditions of the previous example Sec. A.2. The impulse has a contribute not negligible and even dominant in the V_{RMS} of the signal, so we can not believe this is a good realization of the Noise.

Uniform Phase

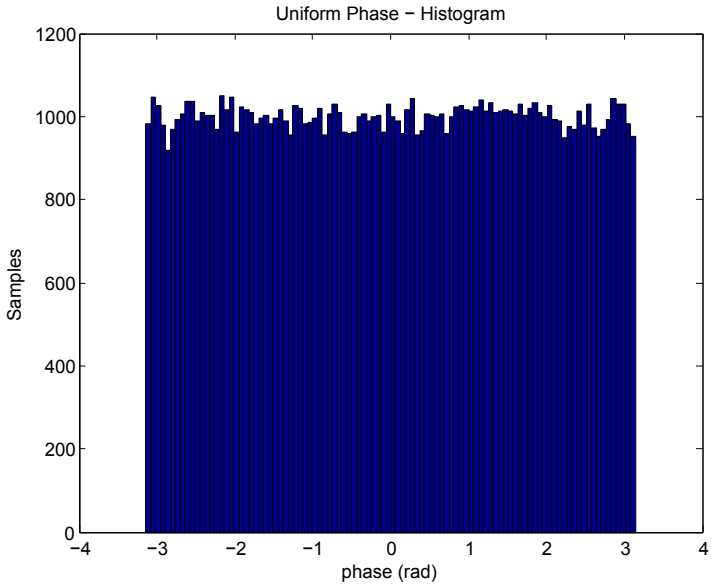

Fig. A.6: Uniform phase

The phase for every frequency sample is created from a *uniform distribution* in $\pm\pi$.

The realization in time domain with module and phase shown respectively in Figure A.1 and Figure A.6 is depicted in Figure A.7.

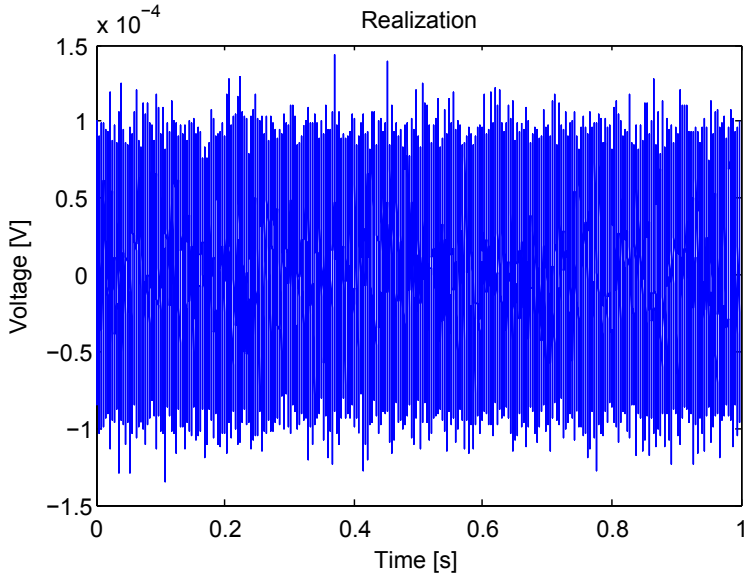

Fig. A.7: Realization in time domain

Already at a glance between Figure 1.1 and Figure A.7 we can see the similarity, in this realization there are not impulses much larger among them.

The calculation of V_{RMS} made with

$$V_{RMS}\Big|_{time} = \sqrt{\frac{\sum_N V(i)^2}{N}} \tag{A.4}$$

leads to the same results of Eq. (A.1), so this is a correct realization (in the Eq. (A.4) is assumed a null mean value $\overline{V(t)} = 0$).

The uniform phase seems to be the correct phase to be associated to the Noise, to be sure, it's possible to make the opposite test, that is to measure the module and the phase of a noisy signal.

Measurement of Noise

I made a measurement of the Noise spectrum of a *Linear Voltage Regulator LDO* (*Low Drop Out*) with a *Network Analyzer*, I measured the module and the phase.

Setup

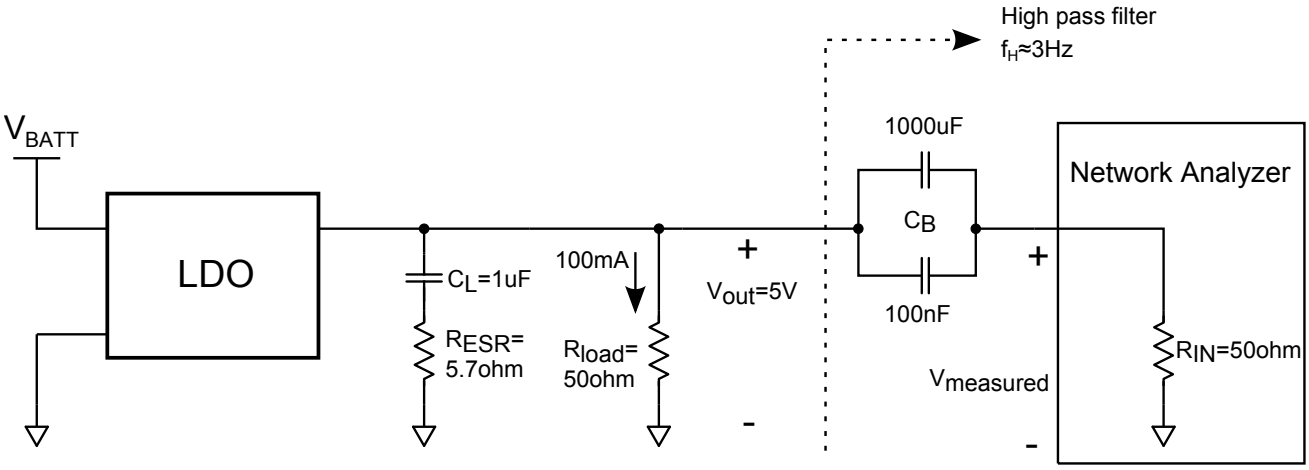

Fig. A.8: Measurement setup

As depicted in Figure A.8, components and the DC operating point are:

$C_{LOAD}[uF]$	$R_{ESR}[\Omega]$	$R_{LOAD}[\Omega]$	$I_{LOAD}[mA]$	$V_{BATT}[V]$	$V_{out}[V]$
1	5.7	50	100	12	5

more informations about an *LDO* are given in Chapter 3.

The Network Analyzer has an input resistance $R_{in} = 50\Omega$ and it accepts at its input port a DC voltage of few *Volts*, thus we have to use a block capacitor C_B that is indispensable for two reasons:

- decouple in DC the input port.
- if the input voltage is allowed ($5V$ are allowed), the load resistance becomes $R_{LOAD}//R_{in}$, so I_{LOAD} becomes different and the Noise too varies.

To design C_B it's necessary to know the bandwidth we want to make the measure, in this case $[10Hz < f < 1MHz]$, because:

- at *Low frequency* there is a high-pass filter $C_B - R_{in}$ (see Figure A.8)

$$\frac{V_{measured}(s)}{V_{out}(s)} = \frac{sC_BR_{in}}{1 + sC_BR_{in}} \tag{A.5}$$

  so it must be $f_0 << f_{min}$, with $f_0 = \frac{1}{2\pi C_B R_{in}}$ the cut-frequency of the filter and $f_{min} = 10Hz$ in this case. C_B results a big capacitor, I chose a commercial value $C_B = 1000\mu F$, so it results $f_0 \approx 3Hz$.

- at *High frequency*, because of C_B is a big and electrolytic capacitor, it has not negligible parasitic components like R_{ESR} and L_{ESR}, so at a frequency $10-100kHz$ the capacitor seems like an inductance. To avoid this problem is possible to connect in parallel a smaller ceramic capacitor ($C_{small} = 100nF$) that relieves the effect of $L_{ESR(C_{BIG})}$ and it has no effect at low frequency because $C_B = C_{BIG} + C_{small} \approx C_{BIG}$.

Measure

Figure A.9 shows the *module* of the spectrum of the measure

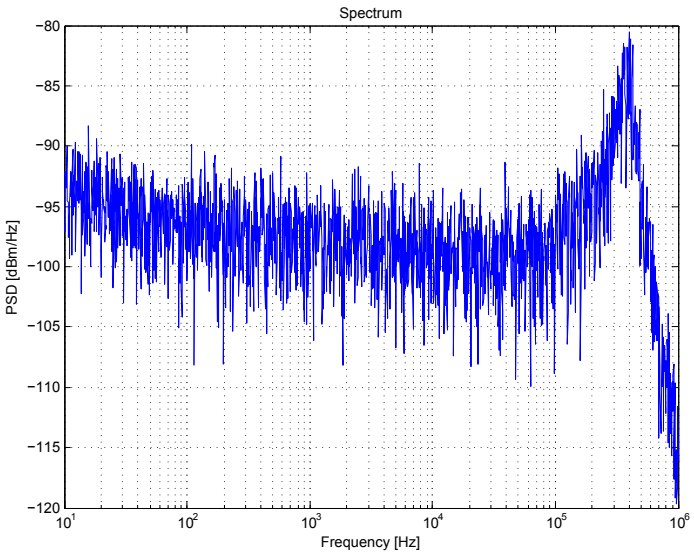

Fig. A.9: Module

and in Figure A.10 is shown the measured *phase*

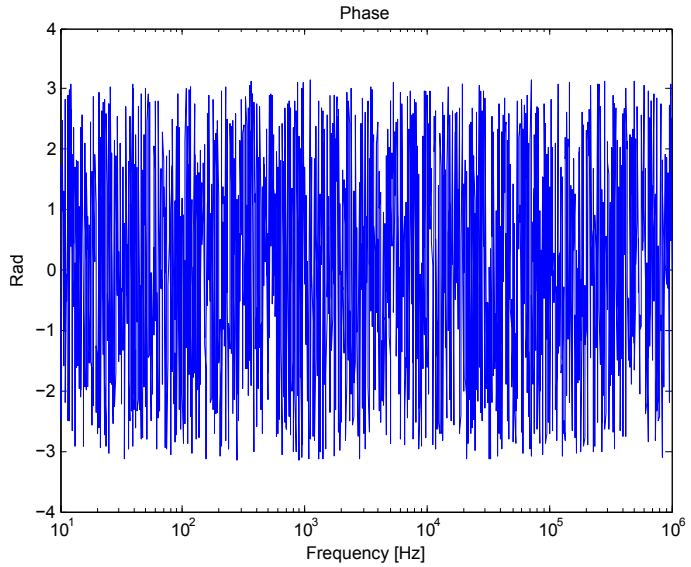

Fig. A.10: Phase

We are interested at the *phase* and the question is: has it a *uniform distribution*? To answer, let's see the histogram in Figure A.11 and make some calculations.

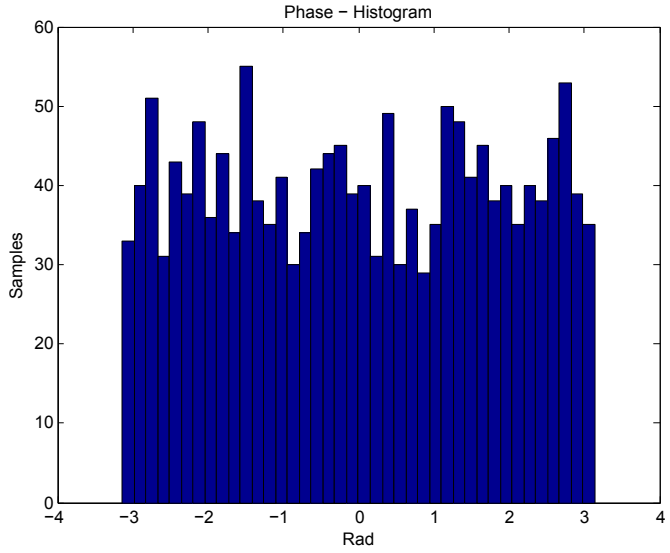

Fig. A.11: Phase histogram

Theory A variable *uniformly distributed* between $\pm\pi$ has *zero mean*, $\overline{x} = 0$ (because the two extremes are opposite), and *variance* $\sigma_x^2 = \frac{\pi^2}{3} \approx 3.3$.

The measured phase presents a mean value $\overline{phase} = 0.0145 \approx 0$ and variance $\sigma^2_{phase} = 3.33 \approx 3.3$, so we may reasonably think that the Noise phase is a *random variable* with a *uniform distribution*.

A.3 Nyquist Theorem

If we want to pass from a *continuous* signal in time domain ($time \in \Re$) to a *discrete* signal ($time \in kT_s$), there is *no information loss* in this passage if:

- the spectrum of the signal is *band-limited* with $f_{MAX} = B$
- the sampling frequency f_s respects the condition: $f_s \geq 2B$

otherwise there is the *Aliasing* phenomenon (think that repetitions in Figure 2.2 are partially overlapped) and we can not exactly rebuilt the original signal from samples.

A.4 PSD

Let's make an example of PSD calculation and let's give some practical and useful knowledge.

We consider this signal:

$$v(t) = 10sen(2\pi ft) + \alpha(t)$$

$\alpha(t)$ is a *random variable* with a *gaussian distribution* and $\sigma_\alpha = 1V$, $f = 10Hz$ and the sampling rate is $f_s = 1MHz$.

The V_{level} indicated in Figure A.13 represents the *white PSD* of the gaussian process $\alpha(t)$ and thus $\sigma_\alpha^2 = V_{level}^2 B$ (B is the bandwidth, so $B = f_s/2$)

$$V_{level} = \sqrt{\frac{\sigma_\alpha^2}{B}} \tag{A.6}$$

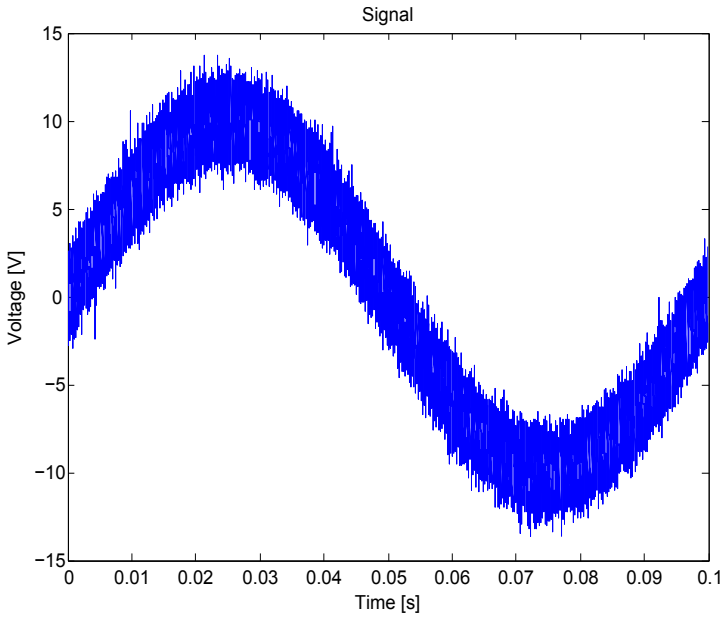

Fig. A.12: Signal, $N = 100k$ Samples

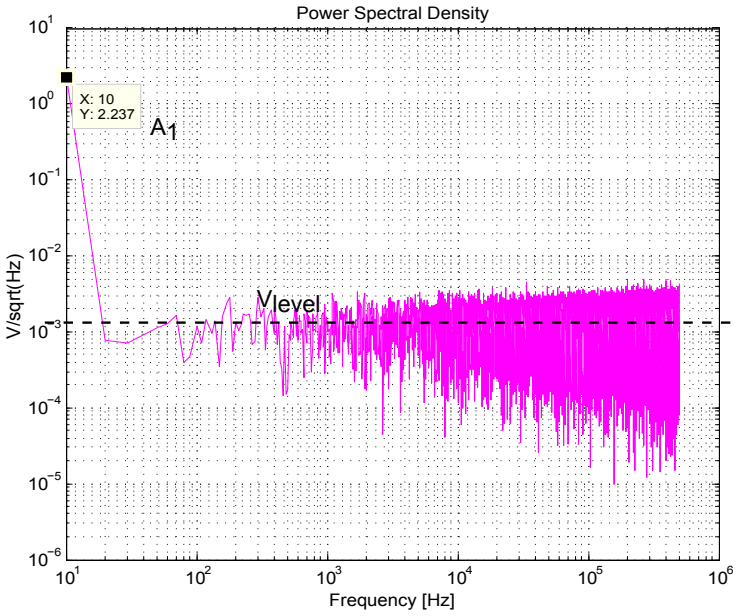

Fig. A.13: PSD, $N = 100k$ Samples

If the number of samples is increased (we sample the signal for a longer time) we obtain Figure A.15, as we can see the V_{level} is the same because of the bandwidth is about the same ($f_{MAX} >> f_{min}$) and thus Eq. (A.6) leads the same result.

The interesting thing to note is that the amplitude of the sine is different in the two cases $A_1 \neq A_2$, this because in the PSD graph the amplitude is scaled by the factor $1/\sqrt{\Delta f}$ as in Eq. (2.7). This is correct for *random signals* that have a *wide spectrum* but this is not correct for *deterministic signals* that have a *line spectrum*, indeed only A_1 is the true *RMS value* so $A_1 = 10/\sqrt{2}$ because of $\Delta f = 1Hz$ in Figure A.13.

With this example we have to remember that the PSD spectrum gives the correct information only for *random signals* that have a *wide spectrum*, otherwise for *deterministic signals* is better to use a simply FFT graph.

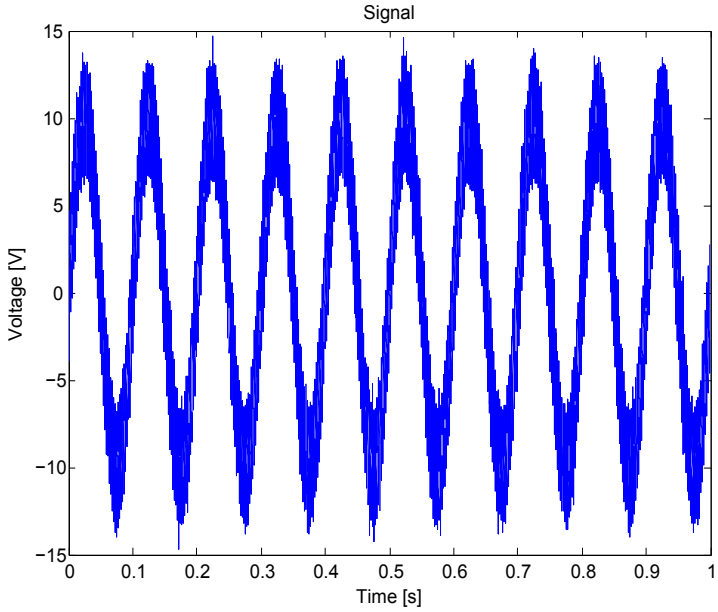

Fig. A.14: Signal, $N = 1M$ Samples

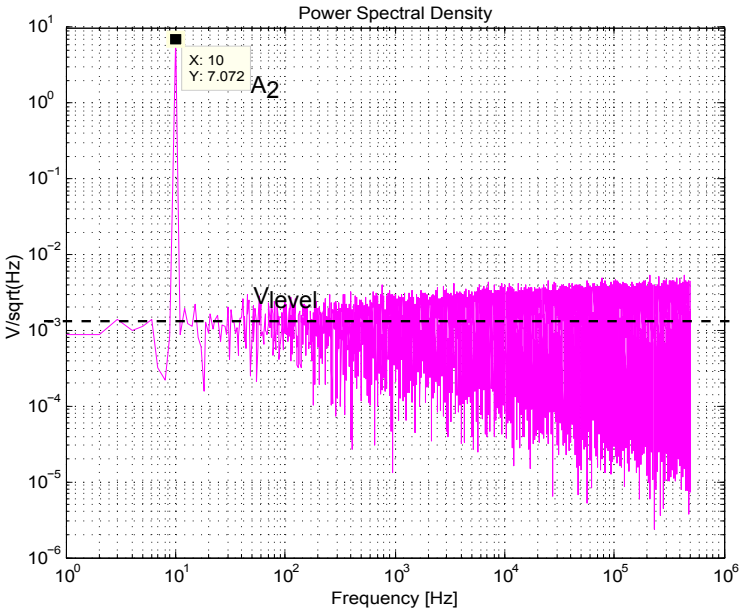

Fig. A.15: PSD, $N = 1M$ Samples

At last I want to make a short digression on the *DC value* $X(f = 0)$ in (2.3), the Relation (2.1) returns the DC value only because it's based on a fictitious periodic repetition of samples $x(nT_s)$. Indeed, we measure only a portion $T_{measured} = NT_s$ of the signal, so we can correctly calculate only the harmonic at $f_{min} = \Delta f = 1/(NT_s)$. The DC value would be correctly calculated only if we sample the signal for an infinite time and this is obviously impossible.

A.5 Flicker Noise Realization

Starting from a *Flicker Noise PSD*, let's try to make a realization in time domain.

Flicker Noise has its PSD that is $\frac{V^2}{Hz} \propto \frac{1}{f}$ and thus $\frac{V}{\sqrt{Hz}} \propto \frac{1}{\sqrt{f}}$, so the module amplitude as in Figure A.16 reduces by 10 in two dacades.

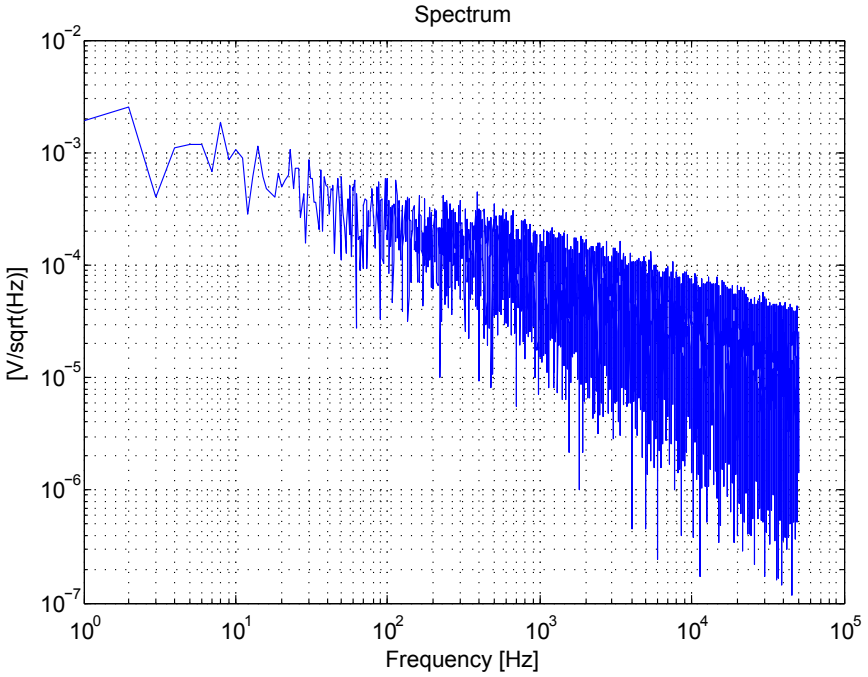

Fig. A.16: Flicker Noise

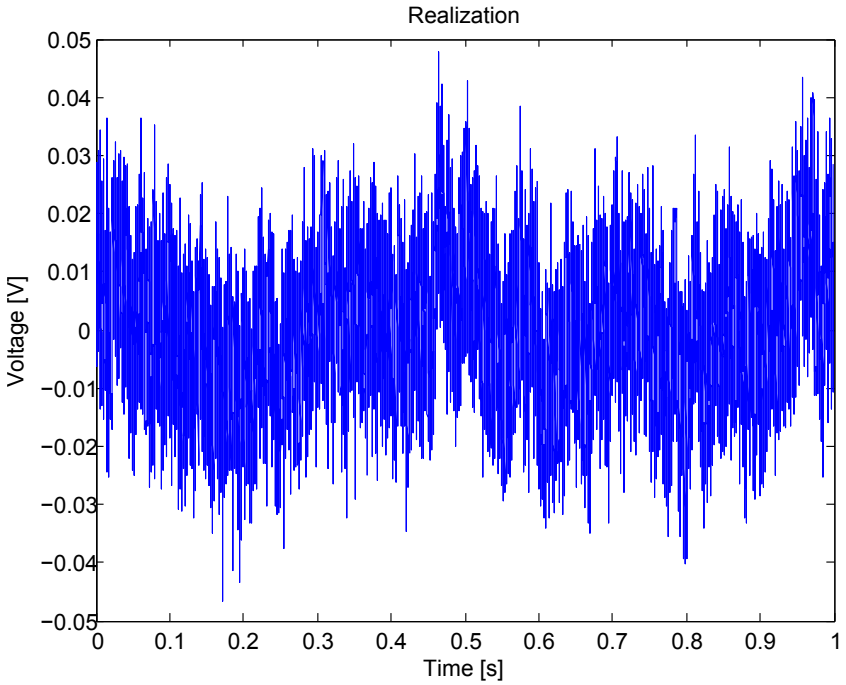

Fig. A.17: Flicker Noise Realization

A.6 Voltage Divider Noise

R_1 Noise

To calculate the Noise transfer function we start with the AC model depicted in Figure 3.4, we can simplify this model in that of Figure A.18.

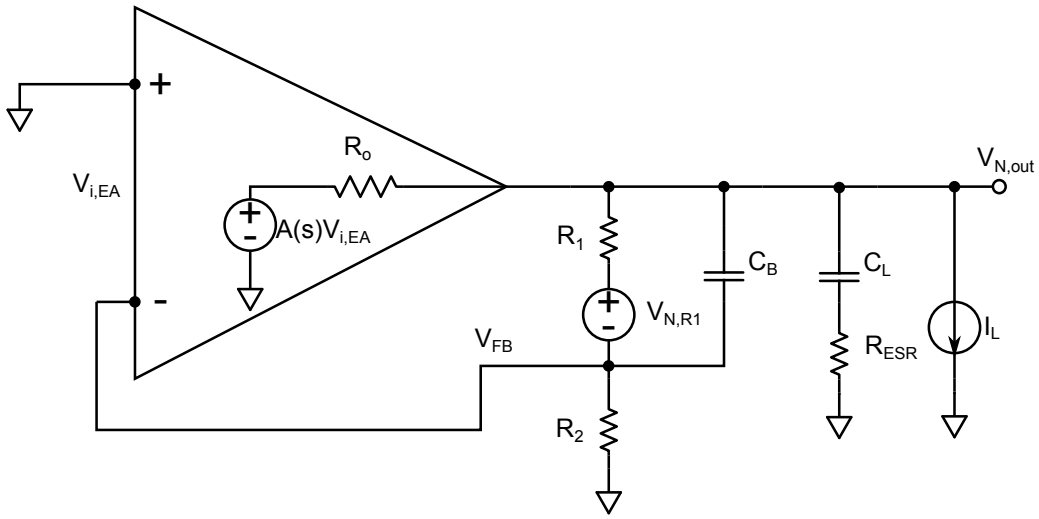

Fig. A.18: Simplified AC model for R_1 Noise calculation

Where $R_o = R_{o,P}$ and $A(s) = A_{EA} \times A_{BUF} \times A_{PASS}$.

For the moment we calculate the transfer function at low frequency so we neglect the contribute of C_L and C_B. Let's apply the KVL (*Kirchhoff Voltage Law*) at the main loop (we consider $I_L = 0$):

$$V_{FB}(s) = \big(A(s)V_{i,EA}(s) - V_{N,R_1}\big)\frac{R_2}{R_1 + R_2 + R_o} \tag{A.7}$$

we make the substitution $\beta = \dfrac{R_2}{R_1 + R_2 + R_o} \approx \dfrac{R_2}{R_1 + R_2}$, $V_{i,EA} = -V_{FB}$ and let's develop the Eq. A.7:

$$V_{FB}(s) = -\frac{\beta V_{N,R_1}}{1 + \beta A(s)} \tag{A.8}$$

To calculate the output voltage:

$$\begin{aligned} V_{N,out}(s) &= A(s)V_{i,EA}(s) - V_{R_o} \\ &= -A(s)V_{FB}(s) - \left(\big(-A(s)V_{FB}(s) - V_{N,R_1}\big)\frac{R_o}{R_1 + R_2 + R_o}\right) \end{aligned} \tag{A.9}$$

and replacing Eq. A.8 in Eq. A.9, we obtain:

$$\begin{aligned} V_{N,out}(s) &= \frac{\beta A(s)}{1 + \beta A(s)}V_{N,R_1} - \frac{\beta A(s)}{1 + \beta A(s)}\frac{R_o}{R_1 + R_2 + R_o}V_{N,R_1} + \frac{R_o}{R_1 + R_2 + R_o}V_{N,R_1} \\ &= \left(\frac{\beta A(s)}{1 + \beta A(s)} - \frac{\beta A(s)}{1 + \beta A(s)}\frac{R_o}{R_1 + R_2 + R_o} + \frac{R_o}{R_1 + R_2 + R_o}\right)V_{N,R_1} \end{aligned} \tag{A.10}$$

We recognize that the Loop-gain $T(s) = \beta A(s)$ is at low frequency $T(s) \gg 1$, and since $R_o \ll R_1 + R_2$ the term $\frac{R_o}{R_1 + R_2 + R_o}$ is $\frac{R_o}{R_1 + R_2 + R_o} \ll 1$. Thus Eq. A.10, in the band of the regulator ($|T| \gg 1$), reduces to:

$$\frac{V_{N,out}}{V_{N,R_1}}(s) \approx \frac{\beta A(s)}{1 + \beta A(s)} \approx 1 \tag{A.11}$$

therefore

$$\frac{\overline{V_{N,out}}^2}{\Delta f} \approx \frac{\overline{V_{N,R_1}}^2}{\Delta f} \tag{A.12}$$

The effect of C_B is to short, at medium frequency (but smaller that $100kHz$), the Noise produced by R_1, so the Noise current flows through C_B and has not influence on the output. Try to think that C_B is a short and C_L is opened, the output voltage will be (respect Eq. A.9):

$$V_{N,out}(s) = -A(s)V_{FB}(s)\frac{R_2}{R_2 + R_o}$$

independent from the noise, so C_B decreases the Noise because it creates a pole at medium-low frequency f_B.

$$f_B = \frac{1}{2\pi R_1 C_B} \tag{A.13}$$

C_L contributes to decrease the Noise because it shorts Noise to ground, but it acts at a higher frequency because it creates a pole at the frequency $f_o \gg f_B$ ($R_{o,CL}$ is very low).

$$f_o = \frac{1}{2\pi R_{o,CL} C_L} \tag{A.14}$$

So R_1 Noise, usually, "sees" a 1-pole transfer function (see Figure 3.12):

$$\frac{\overline{V_{N,out}}^2}{\Delta f} \approx \left(\frac{1}{1 + j\frac{f}{f_B}} \right)^2 \frac{\overline{V_{N,R_1}}^2}{\Delta f} \tag{A.15}$$

R_2 Noise

As R_1 Noise calculation we use a simplified AC model respect that depicted in Figure 3.4, in Figure A.19 the circuit is drawn in a different way.

We easily identify a classical *inverting integrator*, so when the circuit works well (when $|T| \gg 1$), the transfer function for R_2 Noise is:

$$\frac{\overline{V_{N,out}}^2}{\Delta f} \approx \left(-\frac{\frac{R_1}{R_2}}{1 + j\frac{f}{f_B}} \right)^2 \frac{\overline{V_{N,R_2}}^2}{\Delta f} \tag{A.16}$$

with f_B the same as in Eq. A.13.

In this case too, C_L creates a pole (the same as in Eq. A.14) at high frequency so it has a poor effect.

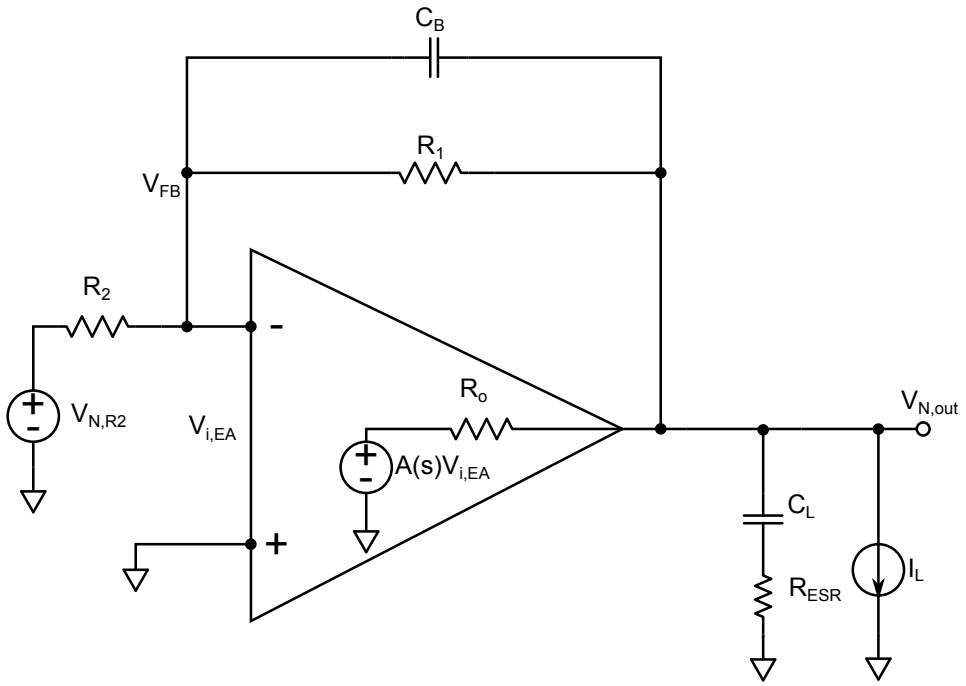

Fig. A.19: Simplified AC model for R_2 Noise calculation

A.7 Active Feedback: Stability and Noise

Stability

It's quite simple to guarantee the stability of the active feedback loop and for this choice of values the Loop-Gain is shown in Figure A.20.

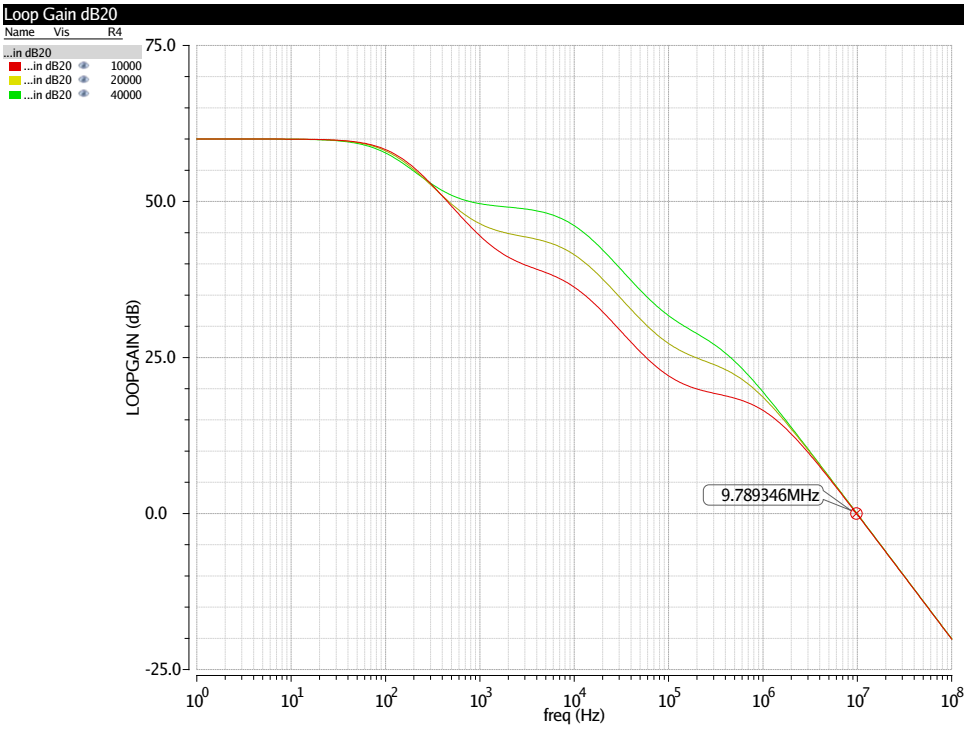

Fig. A.20: Feedback Loop-gain, $Voltage\text{-}gain_{EA,FB}(0) = 60dB$, $f_{pole_{EA,FB}} = 10kHz$, $R_3 = 100k\Omega$, $C_3 = 16pF$, $C_4 = 10nF$

Instead, the main loop is more difficult to compensate, using the circuit in Figure 3.18 except for the feedback that is that in Figure 3.25, $T(s) \approx A(s)\frac{R_L}{R_L + R_o}\beta_F(s)$ and β_F is that of Figure 3.26.

If there is not the active feedback, the loop-gain crossing frequency is *tens of kHz*, now with the active feedback, at those frequencies the loop-gain magnitude is $A_{v,FB}$ times greater and so the crossing frequency f_c shifts to higher frequencies, *hundreds of kHz*. This is a very big problem because at few MHz there are parasitic poles, so shifting f_c near the MHz is dangerous, this is the biggest problem using an active feedback. Using a quasi-ideal circuit to simulate the loop-gain we have not the problem of lots of parasitic poles, so the only thing that decreases the phase margin is the proximity of p_2 (Eq. 3.46) and p_o (Eq. 3.16) that leads to a *2-poles system*, this is depicted well in Figure A.21.

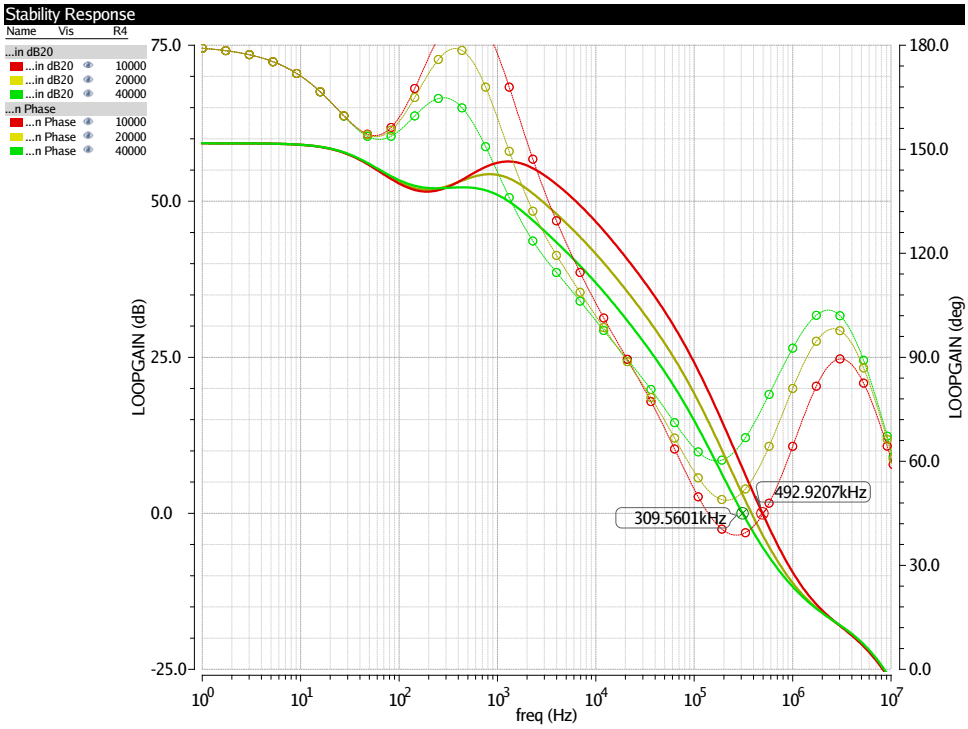

Fig. A.21: Main-Loop Loop-gain, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

$A_{v,FB}$	PM [°]
11	45
6	54
3.5	66

Tab. A.1: Phase Margin referred to Figure A.21, $I_L = 100mA$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

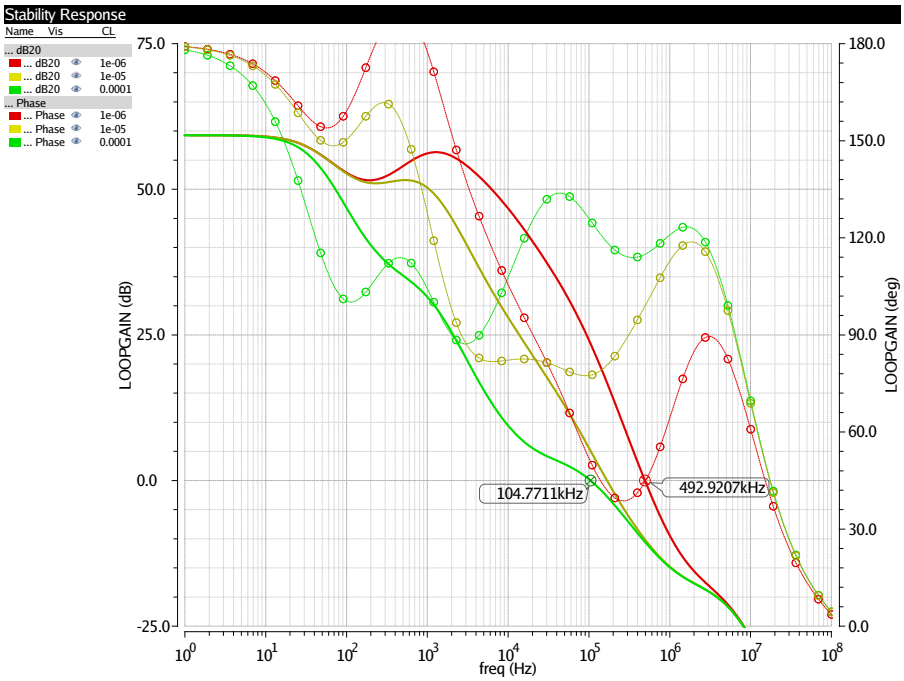

Fig. A.22: Main-Loop Loop-gain, $A_{v(FB)} = 11$, $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 1nF$

C_L $[\mu F]$	PM $[^\circ]$
1	45
10	80
100	125

Tab. A.2: Phase Margin referred to Figure A.22, $A_{v(FB)} = 11$, $I_L = 100mA$, $ESR = 100m\Omega$, $C_B = 1nF$

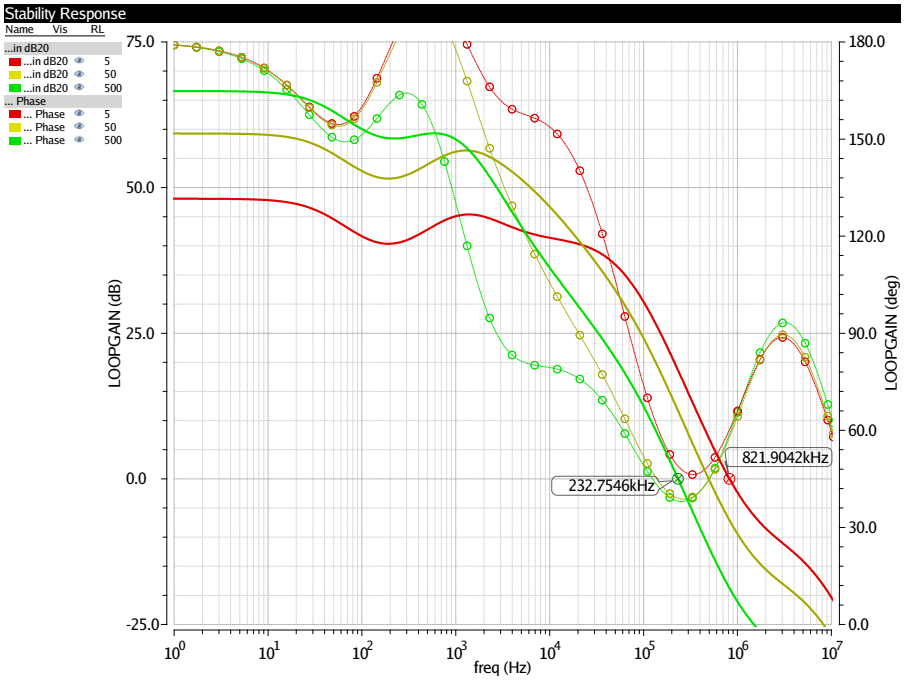

Fig. A.23: Main-Loop Loop-gain, $A_{v(FB)} = 11$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

I_L [A]	PM [°]
1	60
100m	45
10m	38

Tab. A.3: Phase Margin referred to Figure A.23, $A_{v(FB)} = 11$, $C_L = 1\mu F$, $ESR = 100m\Omega$, $C_B = 1nF$

Active Feedback Noise

The active feedback produces itself a Noise that is injected in the circuit, this Noise is produced by R_3, R_4 and the *feedback error amplifier*. The noise of the feedback EA can be represented as an input noise of the EA so it is added at the V_x node (referring to Figure 3.25), the Noise produced by R_3 and R_4 is more useful to consider injected in the V_{FB} node.

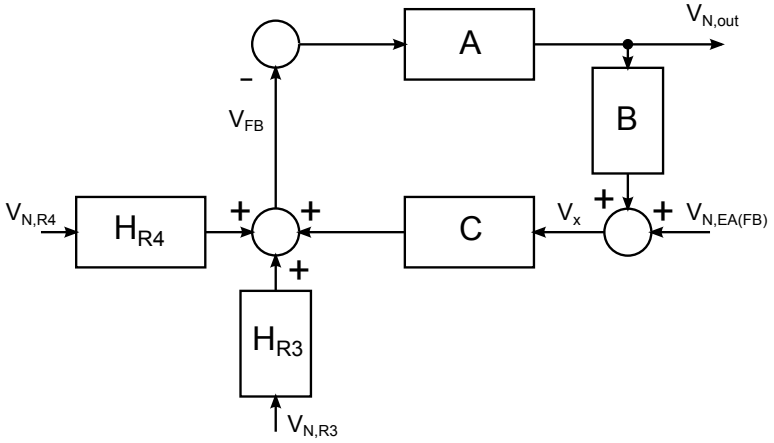

Fig. A.24: Active feedback Noise scheme

In the block scheme of Figure A.24

$$A = A(s) = A_{EA}(s) \times A_{BUF}(s) \times A_{PASS}(s) \tag{A.17}$$

and $B = B(s)$ is that of Eq. 3.41 and $C = C(s)$ is that of Eq. 3.42 depicted in Figure 3.26.

The output Noise due to active feedback is:

$$\frac{V_{N,out}}{\sqrt{\Delta f}} = -\frac{A(f)H_{R_4}(f)}{1+A(f)B(f)C(f)}\frac{V_{N,R_4}}{\sqrt{\Delta f}} - \frac{A(f)H_{R_3}(f)}{1+A(f)B(f)C(f)}\frac{V_{N,R_3}}{\sqrt{\Delta f}} - \frac{A(f)C(f)}{1+A(f)B(f)C(f)}\frac{V_{N,EA(FB)}}{\sqrt{\Delta f}} \tag{A.18}$$

that in the band of the regulator $|T(s)| = |A(s)B(s)C(s)| \gg 1$ it reduces to

$$\frac{V_{N,out}}{\sqrt{\Delta f}} \approx -\frac{H_{R_4}(f)}{B(f)C(f)}\frac{V_{N,R_4}}{\sqrt{\Delta f}} - \frac{H_{R_3}(f)}{B(f)C(f)}\frac{V_{N,R_3}}{\sqrt{\Delta f}} - \frac{1}{B(f)}\frac{V_{N,EA(FB)}}{\sqrt{\Delta f}} \tag{A.19}$$

The calculation of H_{R_3} and H_{R_4} is similar to that of R_1 and R_2 Noise in Appendix. A.6 because the two circuits (Figure 3.25 and Figure 3.18) are the same except for C_4.

R_4 Noise

R_4 Noise "sees" substantially the same transfer function (H_{R_4}) of R_2 Noise, so it seems injected in an *inverting integrator* at medium-high frequencies, it is amplified by $-\frac{R_3}{R_4}$ at medium frequency and then, when C_3 starts to make effect, the transfer function decreases. The difference is at low frequency, because C_4 "opens" the branch $C_4 - R_4$ at DC and so the R_4 Noise has no effect. It starts to have effect when C_4 impedance is comparable to R_4 one. These explained effects leads to a transfer function of this type:

$$\frac{V_{FB}}{V_{N,R_4}}(s) = H_{R_4}(s) = -\frac{sR_3C_4}{(1+sR_4C_4)(1+sR_3C_3)} \tag{A.20}$$

The total transfer function to output is obtained combining Eq. A.19 with Eq. A.20 and its shaping is shown in Figure A.25.

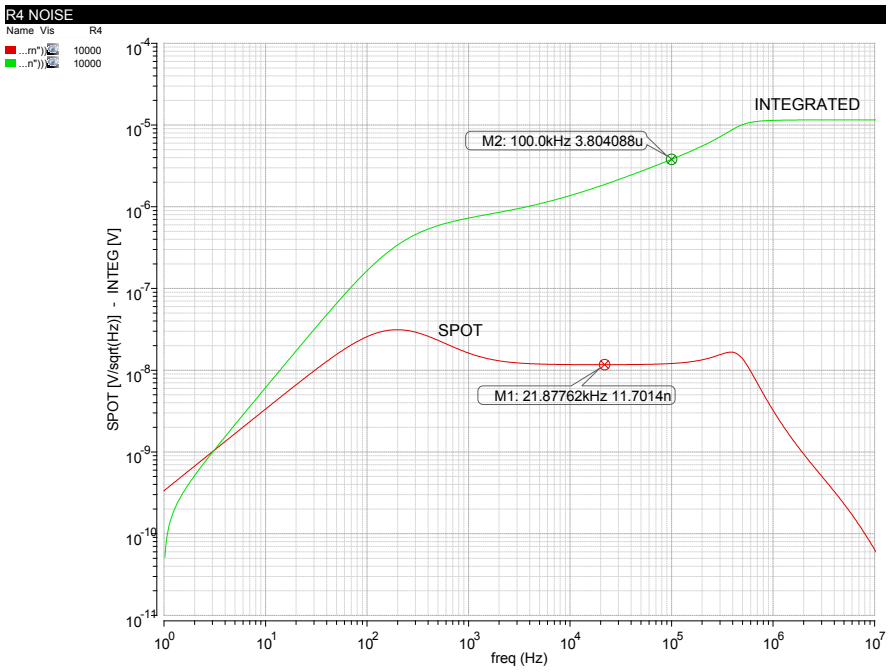

Fig. A.25: R_4 Noise, $R_4 = 10k\Omega$, $R_3 = 100k\Omega$, $C_3 = 16pF$, $C_4 = 10nF$

R_3 Noise

R_3 Noise has the same transfer function (H_{R_3}) of R_1 Noise, it is transferred with a unitary gain at the V_{FB} node until C_3 shorts it, so the gain reduces definitively.

$$\frac{V_{FB}}{V_{N,R_3}}(s) = H_{R_3}(s) = -\frac{1}{1+sR_3C_3} \tag{A.21}$$

The total transfer function to output is obtained substituting Eq. A.21 in Eq. A.19 and its shaping is shown in Figure A.26.

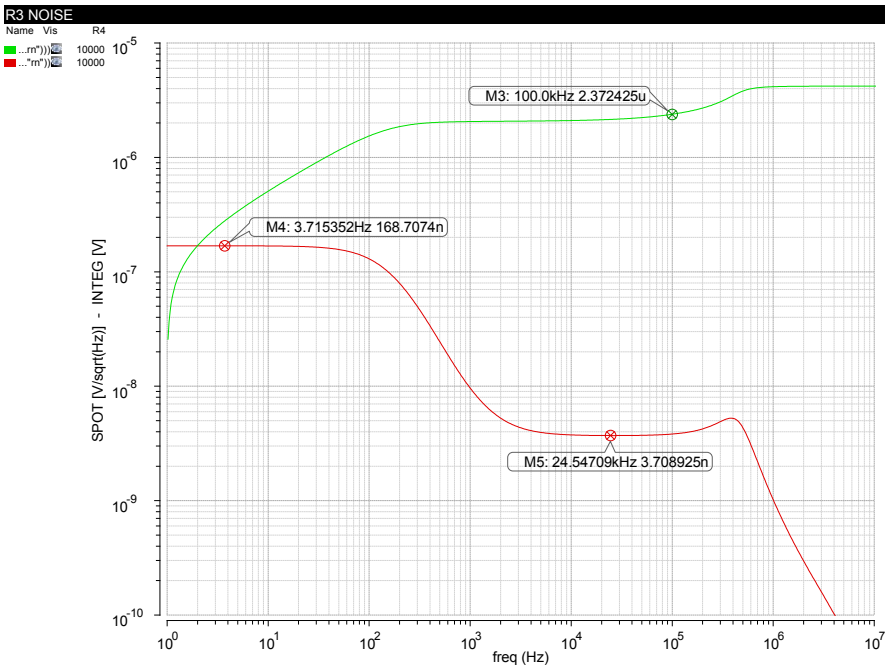

Fig. A.26: R_4 Noise, $R_4 = 10k\Omega$, $R_3 = 100k\Omega$, $C_3 = 16pF$, $C_4 = 10nF$

Feedback Error Amplifier Noise

The $EA(FB)$ contributes to the output Noise as in Eq. A.19, so its transfer function is simply $\approx \dfrac{1}{B(s)}$, in fact we recognize the shape of Figure 3.19 in Figure A.27.

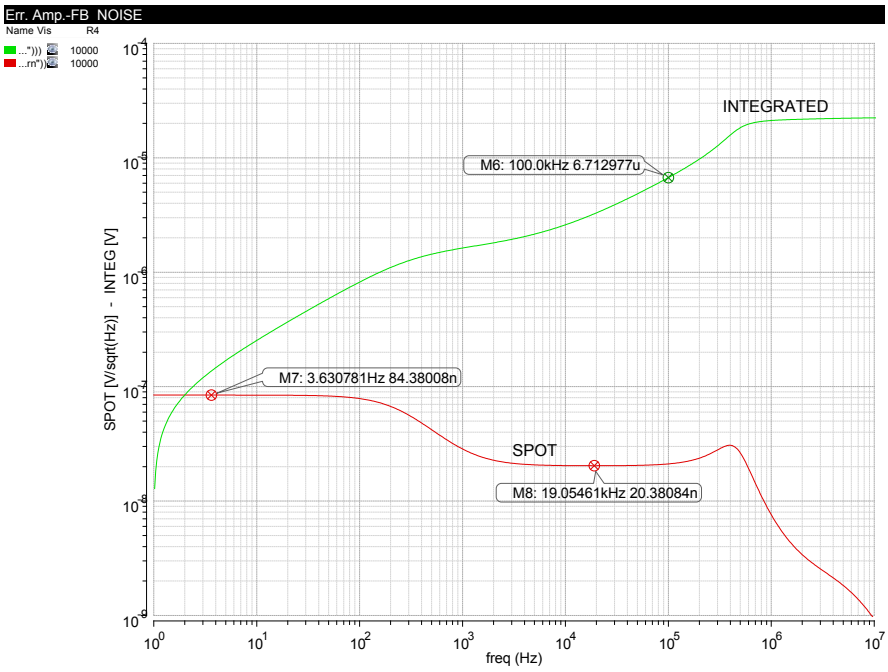

Fig. A.27: $EA(FB)$ Noise, $V_{i,N}/\sqrt{\Delta f} = 20nV/\sqrt{Hz}$, $R_1 = 630k\Omega$, $R_2 = 200k\Omega$, $C_B = 1nF$

A.8 Miller Theorem

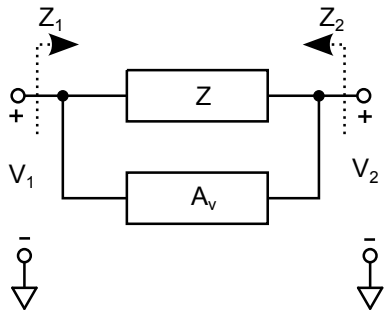

Fig. A.28: Miller Effect

If we have a "longitudinal" bipole of impedance Z, $A_v = V_2/V_1$ is the voltage gain, we can substitute this bipole with two "transverse" bipoles (one at input port and one at output port) with impedance:

$$Z_1 = \frac{1}{1 - A_v} Z \tag{A.22}$$

$$Z_2 = \frac{A_v}{A_v - 1} Z \tag{A.23}$$

This is true if the voltage gain doesn't vary appreciably after the substitution.

In practical cases we usually use this theorem to "increase" a capacitor. We think $Z(s) = \frac{1}{sC}$ and $A_v < 0$, in this case if $A_v \ll -1$:

$$Z_1 \approx \frac{1}{s(CA_v)} \tag{A.24}$$

$$Z_2 \approx \frac{1}{sC} \tag{A.25}$$

So at the input port the capacitor "seems" increased and it "seems" the same at the output port.

A.9 MOS and BJT Noise

MOS transistor may be modeled for Noise analysis in two equivalent ways as in Figure A.29.

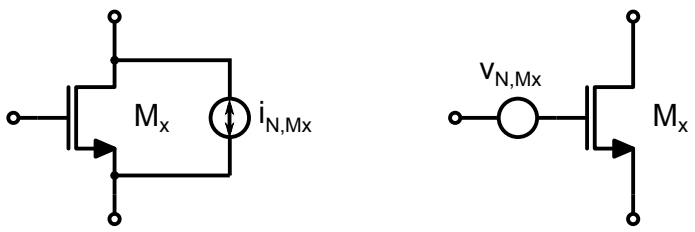

Fig. A.29: MOS, equivalent Noise models

Thermal Noise The model that shows the physical Noise phenomena is the "Current Model" where, for long-channel devices:

$$\frac{\overline{i_N^2}}{\Delta f} = \frac{8}{3} kT g_m \tag{A.26}$$

But in some cases is useful to use the *equivalent* "Voltage Model" obtained by the division by g_m^2:

$$\frac{\overline{v_N^2}}{\Delta f} = \frac{8}{3} kT \frac{1}{g_m} \tag{A.27}$$

so it's like the device is an equivalent resistance of $R_{eq.MOS} = \frac{2}{3}\frac{1}{g_m}$.

Flicker Noise Flicker Noise is modeled, exactly as Thermal, with a current generator between Source and Drain:

$$\frac{\overline{i_{N,1/f}^2}}{\Delta f} = \frac{K_f I_D}{C_{ox} L^2} \frac{1}{f} \tag{A.28}$$

if we are interested in the *equivalent* input voltage Noise, we have to divide by g_m^2 (remember that $g_m = \sqrt{2 I_D \mu C_{ox} (W/L)}$):

$$\frac{\overline{v_{N,1/f}^2}}{\Delta f} = \frac{B}{WL} \frac{1}{f} \tag{A.29}$$

where $B = \dfrac{K_f}{2\mu C_{ox}^2} = \dfrac{K_f}{2 C_{ox} K'}$ is a coefficient depending from a particular technology.

BJT transistor has its two equivalent Noise models of Figure A.30.

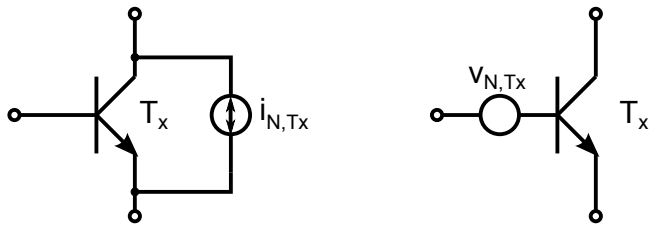

Fig. A.30: BJT, equivalent Noise models

Neglecting the effect of the Shot Noise in the Base current, the "Current Model" has a Noise power:

$$\frac{\overline{i_N^2}}{\Delta f} = 2 q I_c \tag{A.30}$$

The *equivalent* "Voltage Model", obtained by the division by g_m^2 and observing that $g_m = \dfrac{I_c}{V_T}$ ($V_T = kT/q$), has a Noise power:

$$\frac{\overline{v_N^2}}{\Delta f} = 4kT \frac{1}{2 g_m} \tag{A.31}$$

so it's like the device is an equivalent resistance of $R_{eq.BJT} = \dfrac{1}{2 g_m}$. BJT presents generally a lower input Voltage Noise than MOS, due to the greater transconductance, but the big problem is the Base Shot Noise.

A.10 Gain Stage, Noise

A fundamental circuit to study Noise performance is a gain stage like a *Common Emitter* stage (CE) or a *Common Source* stage (CS), we study the CE-stage because the presence of Shot Noise in the base current ($i_{N,B}$) and the finite input resistance (r_π) make more complicated the calculation.

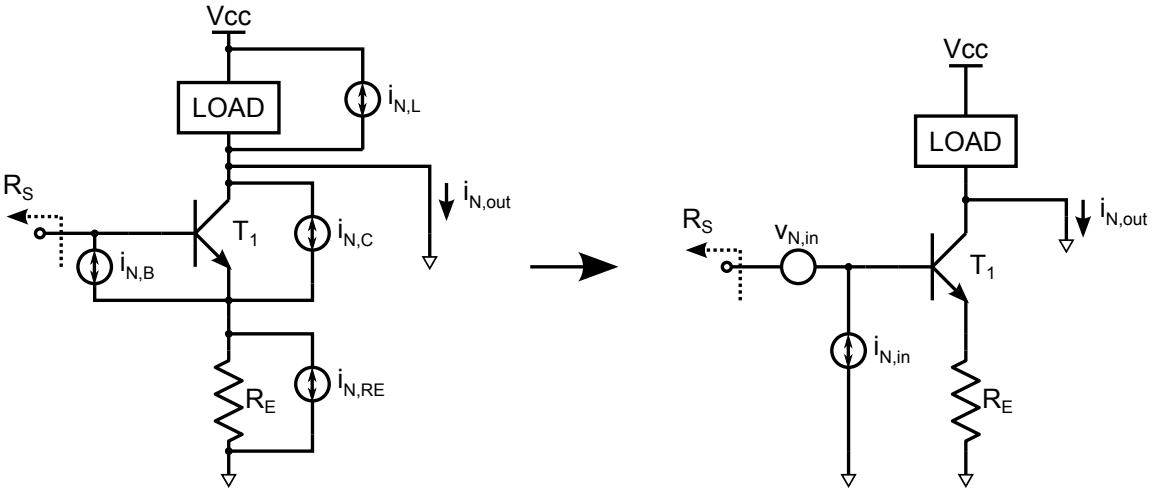

Fig. A.31: CE stage, complete circuit and the equivalent input referred Noise model

The target is to have an equivalent input referred Noise model of the stage, so to calculate $v_{N,in}$ and $i_{N,in}$ (notations are referred to Figure A.31). At first we concentrate to $v_{N,in}$, its main sources are $i_{N,L}$, $i_{N,C}$, i_{N,R_E} so we calculate their effect on $i_{N,out}$ using the complete circuit:

$$\frac{\overline{i^2_{N,out}}}{\Delta f} = \frac{\overline{i^2_{N,L}}}{\Delta f} + \left(\frac{1}{1+g_m R_E}\right)^2 \frac{\overline{i^2_{N,C}}}{\Delta f} + \left(\frac{g_m R_E}{1+g_m R_E}\right)^2 \frac{\overline{i^2_{N,R_E}}}{\Delta f} \tag{A.32}$$

Eq. A.32 may be found with the complete calculations using the AC-model, in practice there are two case of interest: *Low degeneration* $g_m R_E \ll 1$ and *High degeneration* $g_m R_E \gg 1$.

Low degeneration in this case Eq. A.32 reduces to Eq. A.33

$$\frac{\overline{i^2_{N,out}}}{\Delta f} \approx \frac{\overline{i^2_{N,L}}}{\Delta f} + \frac{\overline{i^2_{N,C}}}{\Delta f} + (g_m R_E)^2 \frac{\overline{i^2_{N,R_E}}}{\Delta f} \tag{A.33}$$

$i_{N,C}$ tends to flow at the output and i_{N,R_E} tends to circle in R_E and not to reach the output.

High degeneration in this case Eq. A.32 reduces to Eq. A.34

$$\frac{\overline{i^2_{N,out}}}{\Delta f} \approx \frac{\overline{i^2_{N,L}}}{\Delta f} + \left(\frac{1}{g_m R_E}\right)^2 \frac{\overline{i^2_{N,C}}}{\Delta f} + \frac{\overline{i^2_{N,R_E}}}{\Delta f} \tag{A.34}$$

$i_{N,C}$ tends to circle in the BJT and not to reach the output and i_{N,R_E} tends to flow in the BJT and to reach the output (remember that $i_{N,R_E} \propto 1/\sqrt{R_E}$). So with high degeneration $i_{N,out}$ is reduced (see Figure A.32).

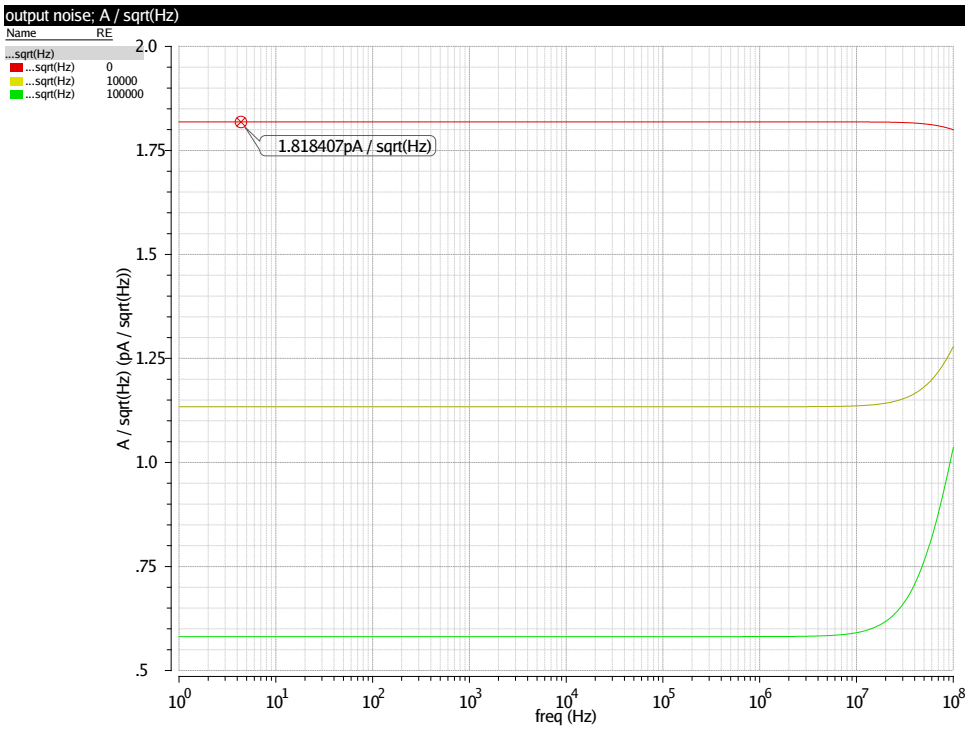

Fig. A.32: $i_{N,out}$ of a CE stage

Using the equivalent model (neglecting for the moment the effect of $i_{N,in}$ and considering $R_S \ll R_{in-stage}$) the $i_{N,out}$ is:

$$\frac{\overline{i_{N,out}^2}}{\Delta f} = (g_{m,tot})^2 \frac{\overline{v_{N,in}^2}}{\Delta f} \tag{A.35}$$

with

$$g_{m,tot} = \frac{g_m}{1 + g_m R_E}$$

is the effective transconductance of the stage.

Equating Eq. A.35 with Eq. A.32 we find

$$\frac{\overline{v_{N,in}^2}}{\Delta f} = \left(\frac{1}{g_{m,tot}}\right)^2 \frac{\overline{i_{N,L}^2}}{\Delta f} + \left(\frac{1}{g_m}\right)^2 \frac{\overline{i_{N,C}^2}}{\Delta f} + \frac{\overline{v_{N,R_E}^2}}{\Delta f} \tag{A.36}$$

An interesting thing is that R_E influences directly the input with its voltage Noise and this is bad because at high degeneration when R_E is a big resistance we have $v_{N,in} \propto \sqrt{R_E}$ (see Figure A.33).

Therefore *degeneration* is suitable if we are interested at a low $i_{N,out}$ and is to avoid if we are interested at a low $v_{N,in}$.

As regards $i_{N,B}$, its effect in $i_{N,out}$ is

$$\frac{\overline{i_{N,out}^2}}{\Delta f} = f(R_E, R_S) \frac{\overline{i_{N,B}^2}}{\Delta f} \tag{A.37}$$

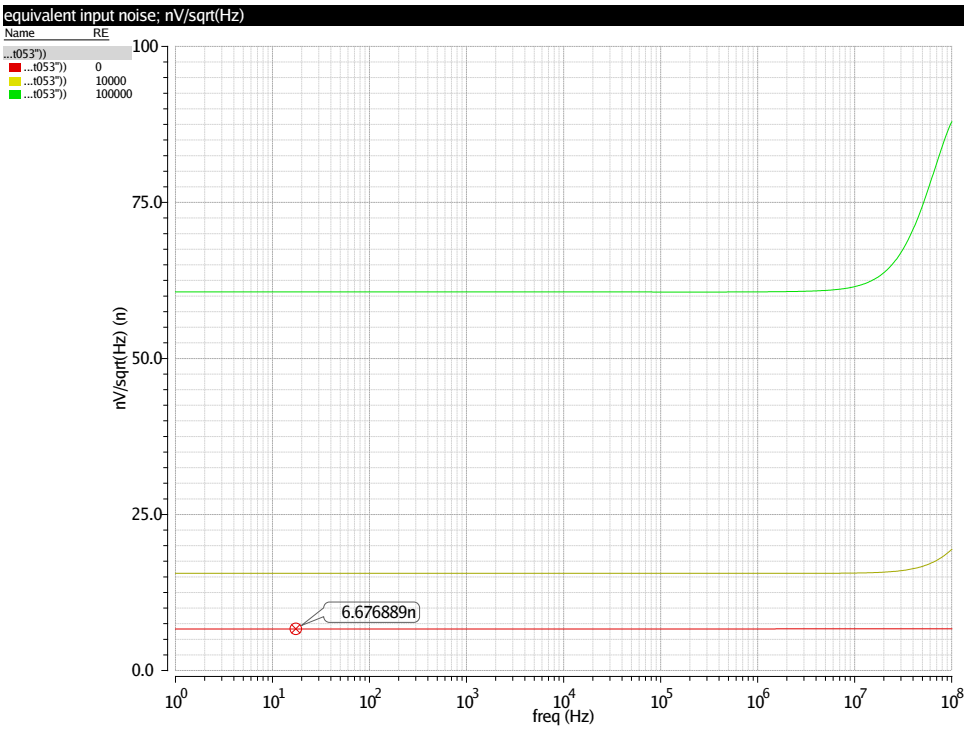

Fig. A.33: $v_{N,in}$ of a CE stage

with in the two cases of practical interest (considering also $R_S \ll R_E$):

$$f(R_E, R_S) = \begin{cases} \left(g_m(R_S//r_\pi)\right)^2 \approx \left(g_m R_S\right)^2 & \text{if } g_m R_E \ll 1 \\ \left(\dfrac{g_m(R_E//r_\pi)}{1+g_m(R_E//r_\pi)}\right)^2 \approx 1 & \text{if } g_m R_E \gg 1 \end{cases} \tag{A.38}$$

Instead, the effect on $v_{N,in}$ due to $i_{N,B}$ (so $v_{N,in(B)}$) is

$$\frac{\overline{v^2_{N,in(B)}}}{\Delta f} = g(R_E, R_S)\frac{\overline{i^2_{N,B}}}{\Delta f} \tag{A.39}$$

with, as in the previous case:

$$g(R_E, R_S) = \begin{cases} (R_S//r_\pi)^2 \approx (R_S)^2 & \text{if } g_m R_E \ll 1 \\ (R_E)^2 & \text{if } g_m R_E \gg 1 \end{cases} \tag{A.40}$$

A.10.1 Low degenerated CE stage

An important thing to keep in mind is that in the case of Low degeneration (or not degeneration), we can confound $i_{N,in} \approx i_{N,B}$, so there is a total effect on input voltage Noise by the addition of effects of Eq. A.36 and Eq. A.39:

$$\frac{\overline{v^2_{N,in(tot)}}}{\Delta f} = \frac{\overline{v^2_{N,in}}}{\Delta f} + (R_S//r_\pi)^2\frac{\overline{i^2_{N,B}}}{\Delta f} \tag{A.41}$$

and since $g_m R_E \ll 1$ the Noise of R_E is negligible respect the Noise $i_{N,C}$ and Eq. A.41 simplifies in

$$\frac{\overline{v^2_{N,in(tot)}}}{\Delta f} = \left(\frac{1}{g_m}\right)^2\left(\frac{\overline{i^2_{N,C}}}{\Delta f} + \frac{\overline{i^2_{N,L}}}{\Delta f}\right) + (R_S//r_\pi)^2\frac{\overline{i^2_{N,B}}}{\Delta f} \tag{A.42}$$

It is evident from Eq. A.42 that the $i_{N,B}$ may increase strongly the Noise. We may calculate to which value of R_S the Power of Base current Shot Noise is equal to the Power of Collector current Shot Noise, considering $R_S \ll r_\pi$ and neglecting the contribution of $i_{N,L}$:

$$\left(\frac{1}{g_m}\right)^2 \frac{\overline{i_{N,C}^2}}{\Delta f} = (R_S)^2 \frac{\overline{i_{N,B}^2}}{\Delta f}$$
$$\left(\frac{1}{g_m}\right)^2 (2qI_C) = (R_S)^2 (2qI_B)$$

therefore

$$R_S = \frac{\sqrt{\beta}}{g_m} \tag{A.43}$$

where β is the current gain of the BJT, with I_C few or tens of μA, R_S will be tens or hundreds of $k\Omega$ that could be in some cases. The $i_{N,B}$ could be a serious problem using Bipolars, this problem there isn't using MOS because there isn't a gate current of polarization.

A.11 Current Mirror Noise

Another very important circuit is the Current Mirror, we study the Noise performance of the Bipolar version because the MOS version is totally identical except for the absence of Base current Shot Noise (remember that $i_{N,C}$ plays the role of $i_{N,D}$ with MOS, but Noise formulas are different).

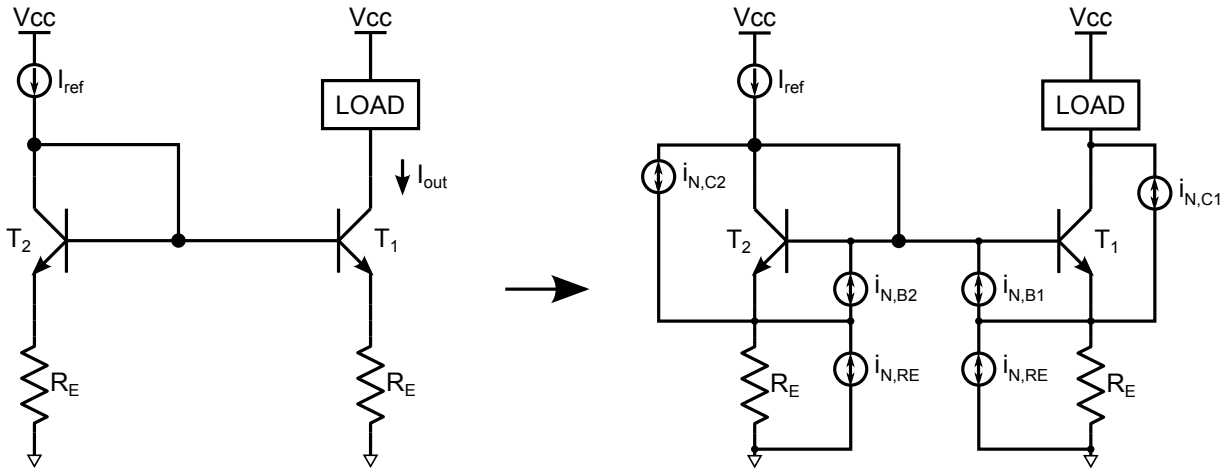

Fig. A.34: Bipolar Current Mirror, circuit and Noise sources

We are interested in the $i_{N,out}$, so the best way to make the calculation is to transform some Noise sources in their equivalent voltage Noise sources in the Base node of BJT $T1$, as in Figure A.35, and then we know the behavior of the CE stage $T1$.

In Figure A.35, the contribution of i_{N,B_2} is incorporated (but can be neglected) in that of i_{N,C_2}, we suppose $g_{m(1)} = g_{m(2)} = g_m$ and, as we have seen in the CE stage, the equivalent voltage Noise sources are (see Eq. A.36):

$$\frac{\overline{v_{N,C_1}^2}}{\Delta f} = \frac{\overline{v_{N,C_2}^2}}{\Delta f} = \left(\frac{1}{g_m}\right)^2 \frac{\overline{i_{N,C}^2}}{\Delta f}$$

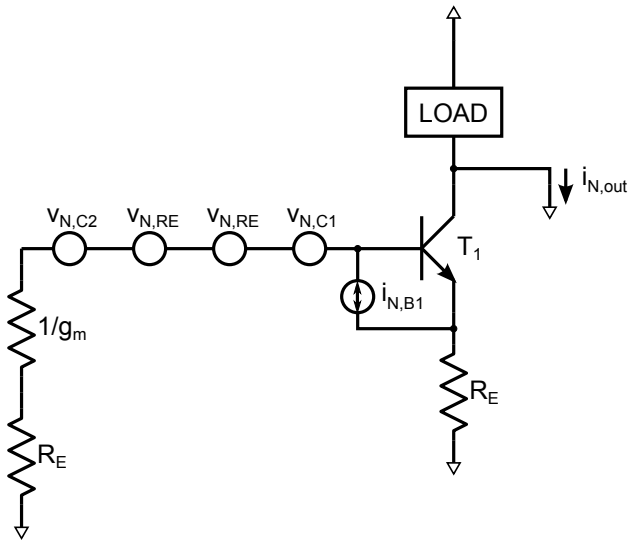

Fig. A.35: Bipolar Current Mirror, AC model

and

$$\frac{\overline{v_{N,R_E}^2}}{\Delta f} = 4kTR_E$$

For the contribute of i_{N,B_1}, we can consider that no current flows into the base of $T1$ so all the current flows in the sum of three resistances $2R_E + 1/g_m$ and thus produce a voltage Noise source at the base of $T1$:

$$\frac{\overline{v_{N,B_1}^2}}{\Delta f} = (2R_E + 1/g_m)^2 \frac{\overline{i_{N,B_1}^2}}{\Delta f}$$

Now we know that the effective transconductance of $T1$ is

$$g_{m,tot} = \frac{g_m}{1 + g_m R_E}$$

thus:

$$\frac{\overline{i_{N,out}^2}}{\Delta f} = (g_{m,tot})^2 \left(2\frac{\overline{v_{N,C}^2}}{\Delta f} + 2\frac{\overline{v_{N,R_E}^2}}{\Delta f} + \frac{\overline{v_{N,B_1}^2}}{\Delta f} \right) \tag{A.44}$$

So, substituting:

$$\frac{\overline{i_{N,out}^2}}{\Delta f} = 2 \times 2qI_C \left(\frac{1}{1 + g_m R_E} \right)^2 + 2 \times 4kTR_E \left(\frac{g_m}{1 + g_m R_E} \right)^2 + 2qI_B \left(\frac{1 + 2g_m R_E}{1 + g_m R_E} \right)^2 \tag{A.45}$$

Eq. A.45 predicts that if we make a strong degeneration ($g_m R_E \gg 1$), $i_{N,out}$ could be strongly decreased (very similar to Figure A.32) until the limit of i_{N,B_1}. Theoretically a MOS current mirror doesn't suffer of this minimum limit but indeed it's impossible to eliminate at all the Noise. In practice MOS or Bipolar current mirror could reach the same Noise performance.

A.12 Transconductance of the Mirrored OTA with asymmetric compensation

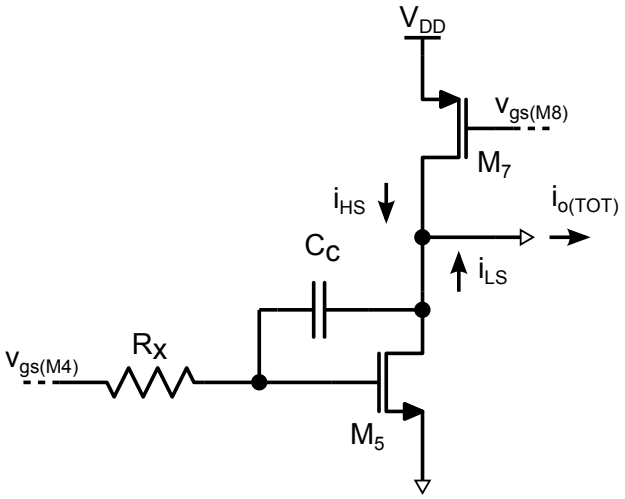

Fig. A.36: Output stage of the Mirrored OTA with asymmetric compensation

For the complete circuit see Figure 4.13.

The current of the *high-side* (i_{HS}) is roughly:

$$i_{HS} = -\frac{g_{m0}}{g_{m3}} g_{m6} \left(-\frac{v_{i,diff}}{2}\right) \tag{A.46}$$

The *low-side* current (i_{LS}) can be calculated solving the following system (use the AC model for the transistor $M5$):

$$\begin{cases} i_{LS} = v_{gs(M4)} \dfrac{1}{R_x + \dfrac{1}{sC_c}} - g_{m5} v_{gs(M5)} \\ v_{gs(M5)} = v_{gs(M4)} \dfrac{\dfrac{1}{sC_c}}{R_x + \dfrac{1}{sC_c}} \end{cases} \tag{A.47}$$

it leads to:

$$i_{LS} = -g_{m5} \frac{\left(1 - s\dfrac{C_c}{g_{m5}}\right)}{(1 + sR_xC_c)} v_{gs(M4)} \tag{A.48}$$

with $v_{gs(M4)} = -\dfrac{g_{m1}}{g_{m4}} \left(+\dfrac{v_{i,diff}}{2}\right)$.

Thus the total output current is (consider $g_{m1} = g_{m0}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, $g_{m7} = g_{m8}$):

$$\begin{aligned} i_{o(TOT)} &= i_{LS} + i_{HS} \\ &= \frac{1}{2} \frac{g_{m1}}{g_{m4}} \left(g_{m5} \frac{\left(1 - s\dfrac{C_c}{g_{m5}}\right)}{(1 + sR_xC_c)} + g_{m6} \right) v_{i,diff} \end{aligned} \tag{A.49}$$

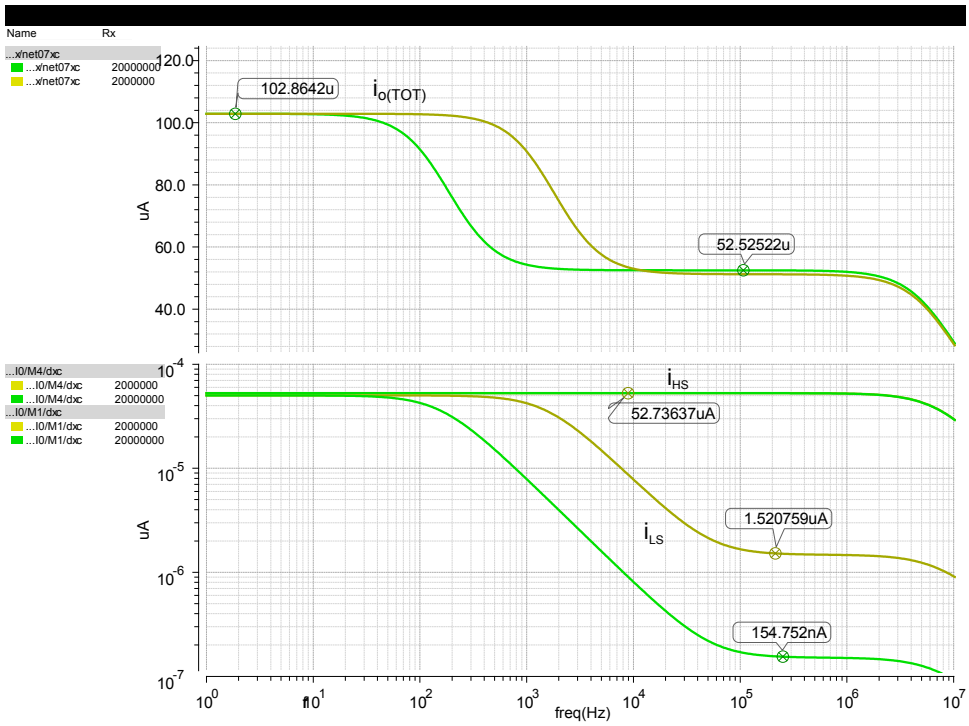

Fig. A.37: Example of $i_{o(TOT)}$ and i_{LS},i_{HS}

An example of the shaping of $i_{o(TOT)}$ is depicted in Figure A.37.

The transconductance of the OTA is:

$$g_{m(TOT)} = \frac{i_{o(TOT)}}{v_{i,diff}} = \frac{1}{2}\frac{g_{m1}}{g_{m4}}\left(g_{m5}\frac{\left(1 - s\dfrac{C_c}{g_{m5}}\right)}{(1 + sR_xC_c)} + g_{m6}\right) \tag{A.50}$$

Important is to note that in the two cases of *low* and *medium* frequency the total transconductance becomes:

$$g_{m(TOT)} = \begin{cases} \dfrac{1}{2}\dfrac{g_{m1}}{g_{m4}}(g_{m5} + g_{m6}) \approx \dfrac{g_{m1}}{g_{m4}}g_{m5} & \text{Low-frequency} \\ \dfrac{1}{2}\dfrac{g_{m1}}{g_{m4}}(g_{m6} - 1/R_x) \approx \dfrac{1}{2}\dfrac{g_{m1}}{g_{m4}}g_{m6} & \text{Medium-frequency} \end{cases} \tag{A.51}$$

so at medium frequency the total transconductance is only that of the *High-side path*, therefore is halved. The same, obviously, it's for the output current that reduces to $i_{o(TOT)} \approx i_{HS}$ as depicted in Figure A.37.

A.13 PTAT and CTAT behaviors

How we can create a *PTAT* (*Proportional To Absolute Temperature*) or *CTAT* (*Complementary To Absolute Temperature*) reference?

The starting point is the relation $I_C - V_{BE}$ of a Bipolar transistor:

$$I_C(T) = I_S(T)e^{\left(\dfrac{V_{BE}(T)}{V_T}\right)} \tag{A.52}$$

where $I_S(T) = A_e J_S(T)$ is the saturation current (A_e is the emitter area and $J_S(T)$ is the saturation current density), $V_T = kT/q$ is the Thermal Voltage.

The inverse relation is:

$$V_{BE}(T) = V_T ln\left(\frac{I_C(T)}{I_S(T)}\right) \tag{A.53}$$

- PTAT

  Consider a structure like that of circuit in Figure 5.1, transistors T_0 and T_1 differs only for the emitter area and the mirror current $M_2 - M_3$ imposes $I_{C_0}(T) = I_{C_1}(T)$. The voltage drop on R_1 is:

$$\begin{aligned} |\Delta V_{BE}| &= |V_{BE_0}| - |V_{BE_1}| \\ &= \frac{kT}{q} ln\left(\frac{I_{C_0}(T)}{A_e J_S(T)} \frac{n A_e J_S(T)}{I_{C_1}(T)}\right) \\ &= \frac{kT}{q} ln(n) \end{aligned} \tag{A.54}$$

  that is a PTAT voltage. Related to the voltage there is a PTAT current that is simply:

$$I_{PTAT} = \frac{V_{R_1}}{R_1} = \frac{|\Delta V_{BE}|}{R_1} = \frac{1}{R_1}\frac{kT}{q} ln(n) \tag{A.55}$$

  The derivative in temperature is:

$$\frac{\partial I_{PTAT}}{\partial T} = +\frac{1}{R_1}\frac{k}{q} ln(n) \tag{A.56}$$

- CTAT

  Deepen the Eq. A.53, considering that $I_S(T) = I_0 e^{\left(-\frac{V_{G0}}{V_T}\right)}$ (consider I_0 independent from the temperature in a first approximation, $V_{G0} = 1.205V$ is the Bandgap of Si at $0K$):

$$\begin{aligned} V_{BE}(T) &= \frac{kT}{q} ln\left(\frac{I_C}{I_0} e^{\frac{qV_{G0}}{kT}}\right) \\ &= V_{G0} - \frac{kT}{q} ln\left(\frac{I_0}{I_C}\right) \end{aligned} \tag{A.57}$$

  so this is a CTAT behavior around the voltage shift V_{G0}.

  The derivative in temperature is:

$$\left.\frac{\partial V_{BE}(T)}{\partial T}\right|_{T=T^*} \approx -\frac{k}{q} ln\left(\frac{I_0}{I_C}\right) = \frac{V_{BE}(T^*) - V_{G0}}{T^*} \tag{A.58}$$

  Considering the ambient temperature $T^* = 300K$ and a classic $V_{BE} \approx 0.6V$, we can calculate $\frac{\partial V_{BE}}{\partial T}(T^* = 300K) \approx \frac{0.6 - 1.205}{300} \approx -2mV/K$ that is a useful value to start with a manual design.

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