UNIVERSITÀ DEGLI STUDI DI PADOVA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

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CORSO DI LAUREA MAGISTRALE IN INGEGNERIA ELETTRONICA

Output stage design of voltage regulator for synchronous generators

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Contents

Abstract

The aim of this thesis is the design of the output stage for voltage regulators used in synchronous generators made by the company Mecc Alte SpA. For design it is understood: the study, development, simulation, implementation and test of such a circuit, in order to provide an innovative design that Mecc Alte can exploit for its future regulator product releases. Obviously, at the moment, the company has already developed multiple regulators, currently working correctly on the alternators already sold. For this reason, it is necessary to say that in this context the thesis has the objective of improving the existing regulators by modifying the output stage that regards the power circuitry that controls the current supplied to the alternator, fundamental in order to guarantee its correct control.

Lo scopo di questa tesi è la progettazione dello stadio di uscita per regolatori di tensione usati in generatori sincroni prodotti dall'azienda Mecc Alte SpA. Per progettazione si intende lo studio, lo sviluppo, la simulazione, l'implementazione ed il test di tale circuito, al fine di offrire un'innovazione che Mecc Alte possa sfruttare per le sue future versioni di regolatori. Ovviamente durante lo svolgimento di questa attività l'azienda ha già sviluppato diversi regolatori, che funzionano correttamente e che sono venduti assieme agli alternatori. Per questa ragione c'è da dire che in questo contesto la tesi ha l'obiettivo di migliorare i regolatori esistenti attualmente usati modificando lo stadio di uscita, che riguarda il circuito di potenza che controlla la corrente fornita all'alternatore, fondamentale per garantire il suo corretto controllo.

Introduction

This thesis is the result of the curricular internship in Mecc Alte SpA. The company main business is the manufacture of synchronous generators. In fact, generators, in addition to the fundamental mechanical and electrical elements, are often controlled in order to guarantee the correct operation in every working condition. In particular, the controller aims to regulate the alternating output voltage to a constant level, which is desired to be independent on the electric utilities the generator supplies. Typically this control, as done in Mecc Alte, is electronically performed by a microcontroller based PCB. This explains the interest of electronic engineering in this environment.

One of the most exciting aspects of this thesis is that it is developed within a real industrial environment. The possibility to get involved in the industrial world, which has an actual interest in this work activity, is extremely important for the student. Certainly some adding difficulties are present, like the high level of autonomy required, the obvious company precedence in its business or the need to learn basic practical skills to make do as much as possible. However, if on one hand those represent a step to overcome, on the other hand, they allow the student to develop extra experience for personal background.

Additional interest for this thesis is generated because it is developed on and for real industrial products, which, at the time this thesis is written, are currently produced and sold to customer companies. The possibility to design and develop a solution for the pragmatic environment of the industrial world is an element of great interest for a graduation thesis, because the proposed solution has to guarantee a series of properties regarding the meeting of regulation requirements, reliability and durability over time, all features not commonly required in the execution of a common project, in which the focus is only the project functionality.

The aim of this thesis is the investigation of the modification of a part of the voltage regulator circuit, that is its output stage. This part has the role to manage the power signals of voltage and current involved to enable the possibility to adjust the output voltage the machine generates. The company already has a series of voltage regulators

that are currently mounted and sold with the generators. The company objective is to develop a new circuit based on a different kind of power switch. Specifically, the current versions of the power stage of the voltage regulators are based on a thyristor. The aim is to substitute the thyristor with a both turn-on and turn-off controllable silicon power switch, like a power MOSFET or IGBT, because some advantages in the control system, which are going to be described throughout the thesis, are expected. In order to do so the thesis discusses the study, development, simulation, implementation and test of such a circuit, in order to provide an innovative design that Mecc Alte can exploit for its future regulators releases.

The thesis work is subdivided in the following chapters:

- Chapter 1: an overview regarding the electrical generator, the excitation system and the voltage regulator is presented.
- Chapter 2: the current thyristor-based output stage of the voltage regulator is analyzed, with an emphasis on its issues and limitations.
- Chapter 3: in the core of the thesis, the following topics are discussed: the development of the new circuit, the encountered issues, the solution attempts, the reasons for their inapplicability, the final proposed solution.
- Chapter 4: the thermal analysis of the power devices is performed to evaluate the power losses and to compute the required thermal resistances of the heat sinks.
- Chapter 5: the results of the thesis work are reported.
- Chapter 6: the conclusion provides a summary of the work completed, including a commentary on the advantages and disadvantages of the proposed circuit compared with the present design and describes possible future developments.

Chapter 1

Voltage regulation in electrical generators

This chapter is intended to introduce gradually the voltage regulation in synchronous generators. For this reason, the discussion starts from the electrical generator, known also as alternator, with a particular focus on the AC three-phase synchronous generator, since it is the electrical machine on which the consequent discussion on the development of the output stage of voltage regulator will be about.

The electrical generator is an electrical machine which converts mechanical energy into electrical energy. Its operation is based on the electromagnetic induction phenomenon, ruled by Faraday's law: the variation of magnetic flux linked by a coil induces an electromotive force (EMF) at the coil terminals.

$$f_{em} = -\frac{d\Phi(\vec{B})}{dt} \tag{1.0.1}$$

This old principle, discovered by the english physician Michal Faraday in 1831 (but important are the contributions also of Heinrich Lenz and Franz Ernst Neumann) is the one exploited to produce eletricity starting from a mechanical source of energy.

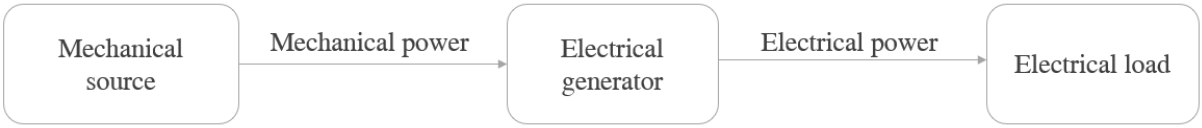

Figure 1.0.1: Power flow in the electrical generator.

Even if it's possible to hypothesize the existence of electrical machines characterized by translational motion (linear machines), for reasons of cost and simplicity, elec-

trical generators are always rotational machines. This means they use a rotating magnetic field with a stationary armature.
Rotating electrical generators can be classified in continuous current (DC) and alternating current (AC) generators related to the kind of voltage and current they produce. The former produce electrical energy having constant voltage and current in time; the latter produce electrical energy having a sinusoidal varying voltage and current in time.
In case of AC generators it is possible to distinguish also on the number of phases of the electrical circuit connected to the load. Typically there are single-phase and three-phase generators.
Another classifying factor differentiates asynchronous from synchronous generators. In an asynchronous generator, the rotational element angular velocity differs from that of the magnetic field; in the synchronous generators, those two velocities are coincident, since the magnetic field is fixed with the rotating element.
Finally, there are two ways the magnetic induction field can be produced in synchronous generator rotors: either using permanent magnets or electromagnets, a continuous current-carrying winding wrapped around a ferromagnetic core. Considering these multi-level classifications, this thesis will consider only rotating AC synchronous generators with an electromagnet excitation rotor. The reader has to keep in mind that from here on the treatment will consider only three-phase generators; mono-phase ones can be considered as a more simple sub-case of three-phase systems, for which the following description represents a more complete discussion.

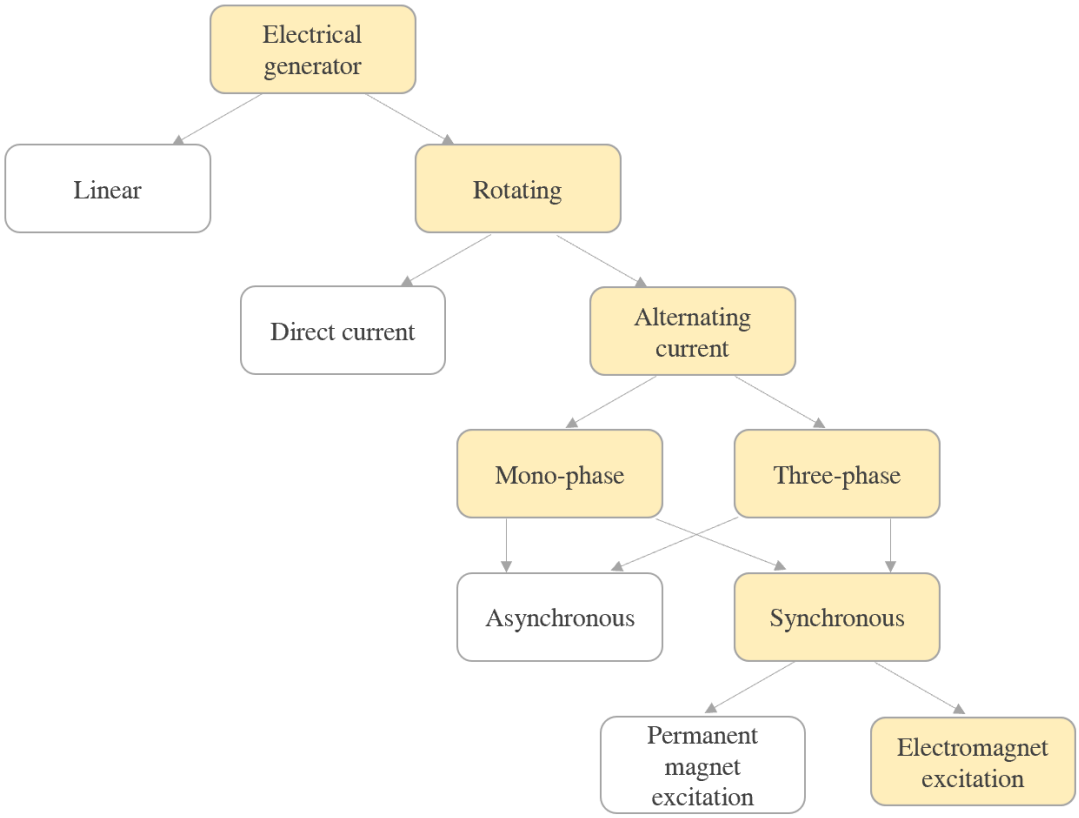

Figure 1.0.2: Generator classification. The coloured blocks highlight the sub-class of interest for the thesis.

1.1 The three-phase synchronous generator

In this section the general structure of a three-phase synchronous generator is described, with the objective of introducing the excitation system, and subsequently, the voltage regulation.

Three-phase synchronous generators are used in many fields. A typical application is the energy production in power plants, where the mechanical power coming from a hydraulic, steam or gas turbine is converted into electricity. Another application, characterized by much lower power and voltage, is the genset, in which a diesel combustion engine feeds the alternator providing electrical energy to sites not reached by the electric grid, for emergency services supply and in case of the main grid blackouts. Mecc Alte alternators belong to this second category.

Figure 1.1.1: Historical image of a three-phase alternator made by Kraftwerk Heimbach, Germany.

Figure 1.1.2: An example of a three-phase Mecc Alte alternator, utilized in gensets.

1.2 General structure

The structure of a three-phase alternator is typically characterized by a *fixed induced* and a *rotating inductor* (as in case of all Mecc Alte products). Going from the center-out it is possible to find:

- **Mechanical shaft** that transfer the mechanical energy from the source to the alternator.

- **Rotor magnetic circuit** fixed and solidly rotating with the shaft, is crossed by the magnetic flux present in the machine.

- **Rotor winding** creates the magnetic field enabling the machine operation. In the typical use case of gensets the salient-pole field coil is used: the rotor winding is composed of coils wound around the poles. A constant excitation current flowing through the coils energizes the poles. The resulting inductor magnetic field, costant in value, rotates at the same angular velocity as the shaft.

- **Stator magnetic circuit**, separated from the rotor magnetic circuit by a small airgap, presents slots for the stator winding conductors.

- **Stator winding**, a stationary set of conductors wound in coils fixed in the slots are separated in three phases 120° apart. The magnetic field cuts across the conductors, generating an induced EMF, as the mechanical input causes the rotor to turn. The rotating magnetic field induces an AC voltage at the stator winding terminals.

- **Stator case**, mechanically connected to the stator magnetic circuit, the purpose of which is to support and provide suitable mounting points for the entire alternator assembly.

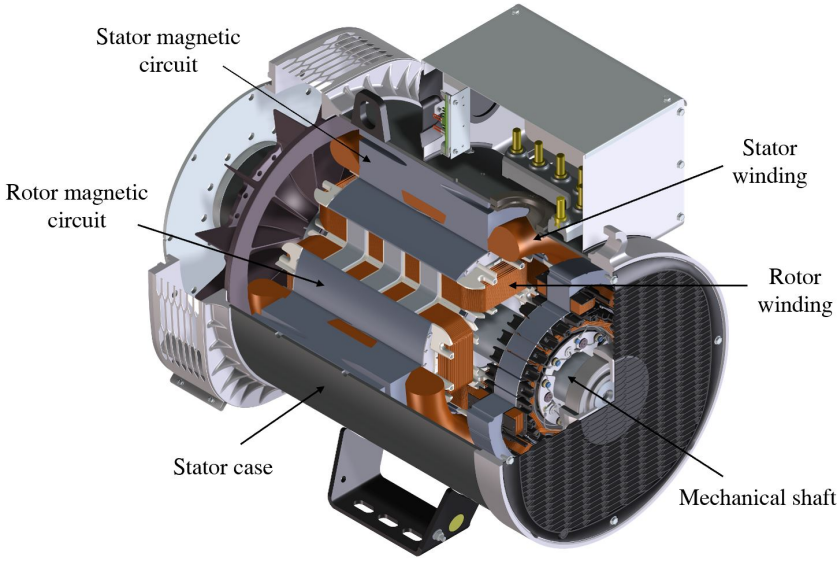

Figure 1.2.1: Visible structure of a Mecc Alte synchronous generator. It is possible to recognize the listed elements.

1.3 The excitation system

The excitation system has the purpose of appropriately energizing the inductor circuit. A direct current provided by this system, flowing into the pole windings, creates electromagnets generating the required magnetic field.

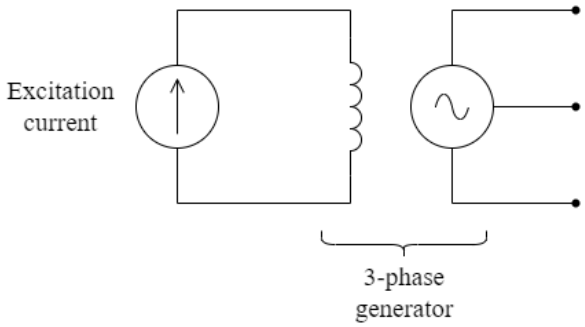

Figure 1.3.1: Basics of excitation system.

All the windings are series-connected so the same current flows in each one. This way, each field coil produces the same magnetic flux intensity. In addition adjacent poles windings are arranged in such a way that they have opposing current directions, thus creating alternating magnetic poles N-S. The direct current can be provided to the

rotor winding using three excitation system types: rotating excitation, static excitation and brushless excitation. All these solutions have in common the necessity to vary the current in a very wide interval in order to maintain the correct operation of the generator for all the critical operation situations, like the abrupt connection or disconnection of the electric load. This continuous adjustment is performed by the voltage regulator, that will be investigated in Section 1.4.

1.3.1 Rotating excitation

Mostly used in the past, in the rotating excitation system the excitation current is supplied by a direct current generator (excitation dynamo) mounted on the main shaft, from which it receives the mechanical power. The DC voltage induced in the dynamo is used to supply the generator rotor winding, using a system of sliding contacts, formed by brushes and rings.

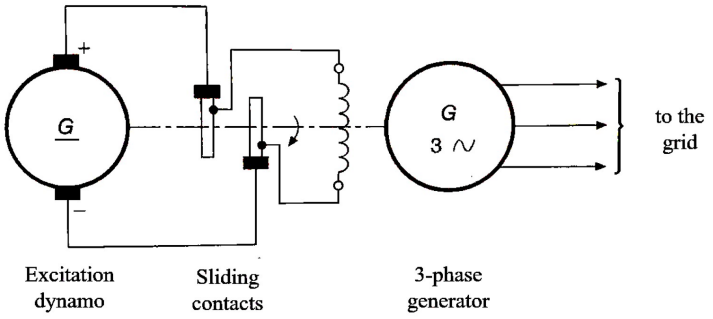

Figure 1.3.2: Rotating excitation block scheme [**1**].

1.3.2 Static excitation

Typical of high power applications, static excitation does not require any electrical machine for excitation. The DC voltage is obtained by means of either a thyristor-made or IGBT-made static rectifier supplied by a three-phase transformer from auxiliary services, allowing to regulate the voltage applied to the main rotor by means of brush and ring connection. This solution presents benefits compared to the dynamo solution: reduction of axial machine size, higher reliability and greater yield.

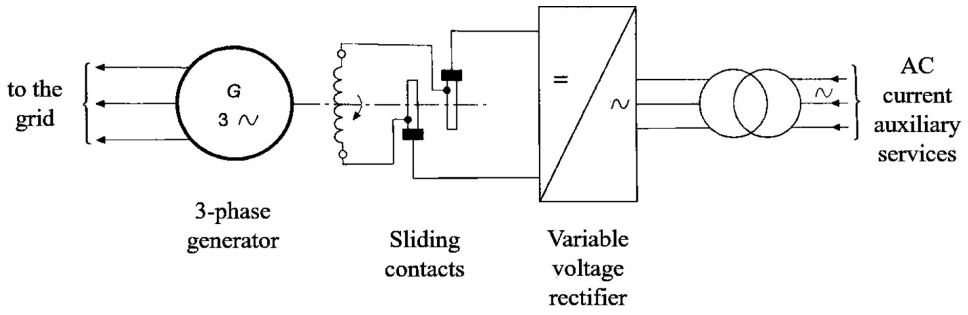

Figure 1.3.3: Static excitation block scheme [**1**].

1.3.3 Brushless excitation

Another kind of rotating excitation, but avoiding the use of brushes, is the one shown in Fig. 1.3.4. An auxiliary generator, called exciter, having opposite configuration with respect to the main generator (*fixed inductor* in the stator and a three-phase *rotation induced* in the rotor) is coupled coaxially with the main generator, rotating at same main rotor angular speed. Sinusoidal voltages induced on the exciter rotor supply a diode rectifier mounted on the main shaft. The resulting rectified voltage constitutes the excitation for the main rotor winding. Since all the connected parts rotate at the same angular speed, no brush and ring system is required. The auxiliary alternator in turn must be supplied by applying an appropriate constant voltage on the fixed inductor in the stator. Varying this parameter allows the regulation of the excitation voltage and current of the main machine. This excitation system is the one chosen by Mecc Alte for all the alternators in its catalogue that uses electromagnet excitation. This choice is made since the absence of sliding contacts avoids components wear and replacement, losses due to friction and undesirable formation of electric arcs, resulting in a more robust and long-lasting product.

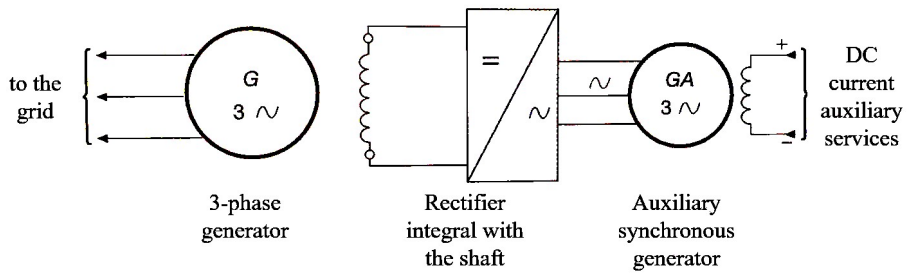

Figure 1.3.4: Brushless excitation block scheme [**1**].

1.4 The voltage regulator

It could be considered that the AVR (Automatic Voltage Regulator) is the brain of the synchronous generator and the core of the excitation system. In fact, it performs measurements and actions in order to maintain the correct alternator operation. As it is expected to do, a generator is needed to provide a constant AC voltage at its output terminals, independently of the load attached to it.

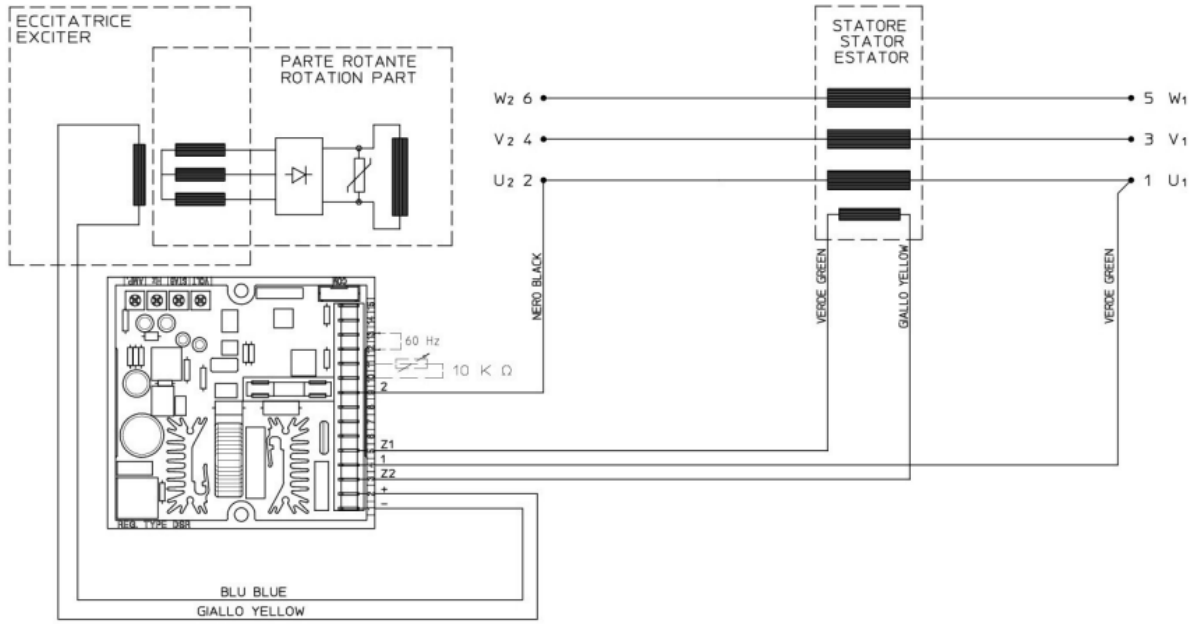

Figure 1.4.1: Excitation system block diagram from DSR digital regulator technical guide [**22**].

This control is performed by the voltage regulator, whose output consists of a pulsed voltage waveform that energizes the exciter stator, inducing on it a continuous current proportional to the signal voltage pulse duration. The magnetic field so produced by the exciter stator coils affects the amplitude of the AC voltage induced in the exciter rotor, that, after been rectified by the rotating diodes, feeds the main rotor windings by means of a proportional constant current. The resultant amplitude controlled rotating magnetic field produced in the field coils, linked by the main stator conductors, induces a proportional EMF at the output generator terminals. To complete the discussion, according to Eq. 1.0.1, it should be mentioned that the other parameter affecting the EMF is the rotational speed of the rotor. However, the real conditions in which a Mecc Alte alternator operates is under a constant rotor angular velocity im-

posed by the external mechanical energy source (a diesel engine). Being the derivative in time of the Faraday's law a non-controllable parameter the only possibility is acting on the intensity of the rotor magnetic field.

The excitation current regulation system has to satisfy the need of a very high operational safety level and a quick transient response. At a load connection or disconnection event, the terminal voltage undergoes a variation due to the armature reaction. In order to bring back the terminal voltage to the desired value, it will be necessary to act on the excitation current by increasing or decreasing the generated EMF. Moreover, the excitation system, in order to keep the voltage constant, must increase the excitation current in the case of inductive loads, while decrease it in the case of a capacitive load.

The circuit controlling and regulating the generated output voltage can be represented by the following block scheme.

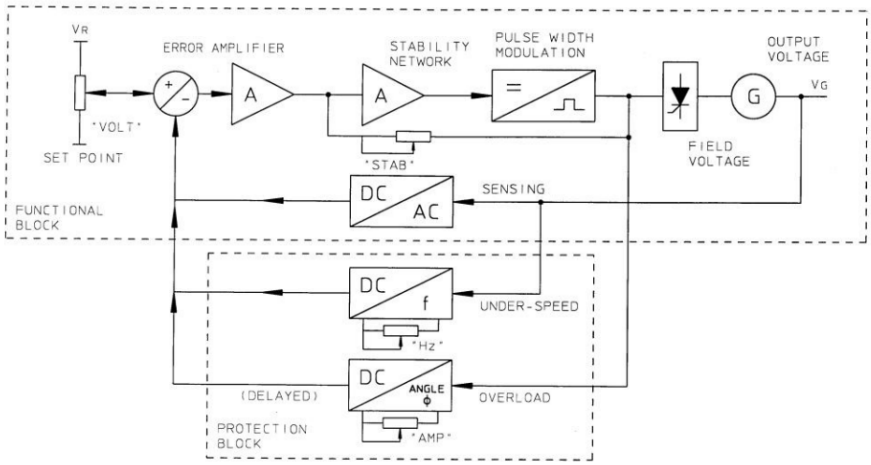

Figure 1.4.2: Voltage regulation scheme [**21**].

It is possible to recognize two main blocks that make up the regulator:

- functional block;
- protection block.

1.4.1 Functional block

This is a negative feedback system, in which the constantly maintained variable is the alternator voltage output. This voltage, after adequate conditioning, is compared with a reference signal (generated inside the electronic regulator) that is stabilized in voltage, temperature and age. The result is an error signal which, after being appropriately

amplified and compensated, produces a control level that enters the regulator. The signal generated by the regulator will control the output terminal voltage as already explained. The set of the stability network is fundamental for the dynamic behaviour of the system. When the alternator undergoes sudden load variations, the presence of this part of the calibrated circuit makes it possible to improve system performance. System regulation with short reset time can keep the system in a stability limit condition. On the contrary, a highly stabilized and calibrated system could be too slow during the reset time.

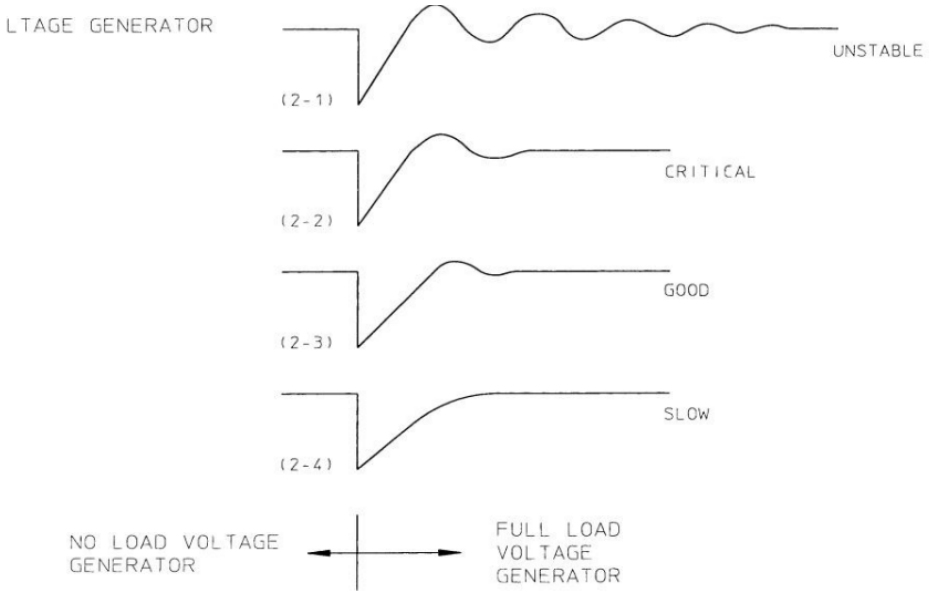

Figure 1.4.3: Comparison between different calibrations for the stability network [**21**].

1.4.2 Protection block

In addition to the error signal, additional inputs are sent to the regulator in order to enable protection features, that preserve the safe operation of the system. The two main monitored aspects are:

- **Overload protection:** in order to avoid damage to the conductors, prevent the maximum value of field current being exceeded. When the value of the continuous voltage that supplies the alternator inductor is higher than the value set by the threshold, a continuous time-delayed signal lowers the value of the alternator output voltage and limits the excitation current produced by the inductor, which guarantees safety margins for system operation. The intervention delay of this protection temporarily overloads the alternator without lowering the output

voltage to guarantee motor starting for example.

- **Low frequency protection:** when the frequency of the output voltage falls below the value of a given threshold, the output signal of this block produces a controlsignal which lowers the output voltage of the generator, in order to stop overexcitation (a typical example is the lowering of the speed for the preheating of the prime mover).

Chapter 2

Analysis of the current voltage regulator output stage

This chapter concentrates on the operation and realization of the output stage of the AVR. After a description of its working principle, the configuration currently used in Mecc Alte regulators will be exposed. Finally, a section detailing the limits of the actual design will introduce the next chapter about the company requirement and project development.

The reader should keep in mind that all the following discussion will be based on the brushless excitation system, as illustrated in Section 1.3.3.

2.1 Switching inductive load

In Section 1.4 it has been mentioned that the regulator acts on the exciter stator current controlling the duration of a voltage pulsed waveform. In order to explain this phenomenon it is preferable to take as a reference the excitation scheme of Fig. 1.4.1, where the focus is posed only on the path connecting the auxiliary winding in the main stator to the exciter stator. This section of the excitation system is illustrated in the figure below.

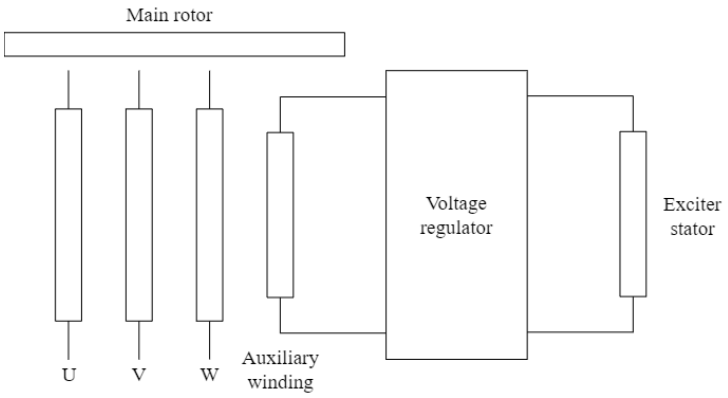

Figure 2.1.1: Auxiliary to stator exciter winding path.

According to the brushless excitation block scheme the energy provided to the exciter stator comes from an auxiliary service. This is achieved by exploiting an additional main stator winding on which, in the same manner as the three phase coils, a voltage is induced according to Faraday's law. For this reason, this auxiliary winding can be represented in a first approximation as a sinusoidal voltage generator. The voltage imposed by the auxiliary generator is applied to the exciter stator by means of a switch, which receives the command from the voltage regulator logic. This way, a pulsed voltage waveform can be applied to the exciter stator.

The aforementioned situation can be described by the following circuit-like scheme.

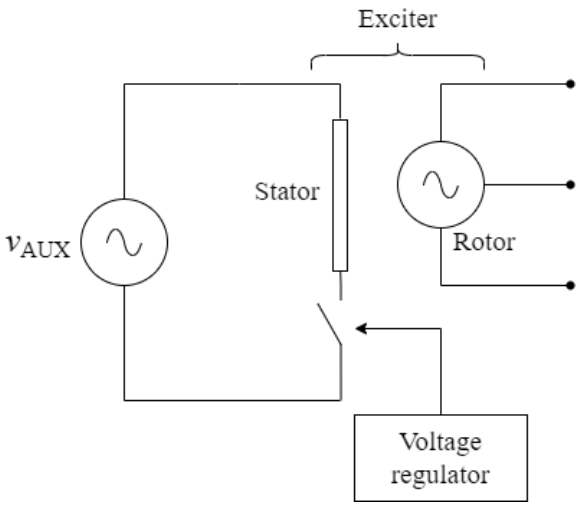

Figure 2.1.2: Voltage regulator working principle.

The application of a pulsed voltage to the exciter stator is not a trivial task since it hides problems due to the inductive nature of the exciter itself. In the two follow-

ing paragraphs the switch theory of an inductive load is presented. The discussion is necessary to understand the complete output stage circuit, which will be presented later.

2.1.1 Simultaneous dual switch - ideal case

Assuming to be in steady-state operation the pulsed voltage waveform applied to the exciter stator will induce a roughly constant current. This is because the exciter stator winding is of inductive nature. In particular, it can be modeled as an inductance L in series with a parasitic resistance R, accounting for the ohmic losses in the exciter stator conductor. The signal generated by the voltage regulator can instead be simply modeled by a constant voltage source in series with an ideal switch.

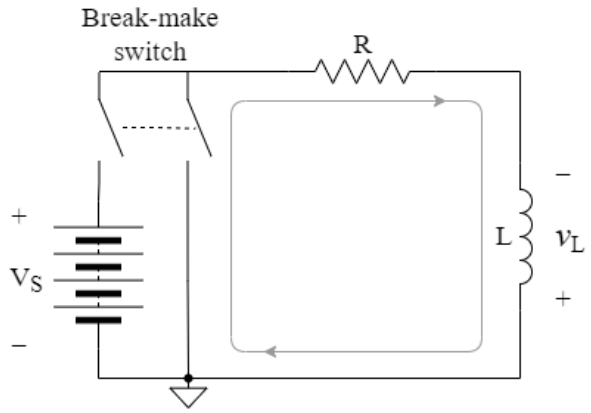

Figure 2.1.3: Circuit representing ideal inductive load switching.

The equation that relates voltage and current in an inductor is

$$v_L(t) = L\frac{di(t)}{dt} \tag{2.1.1}$$

When the switch is closed on the voltage source the Kirchhoff equation is

$$V_S - Ri(t) = L\frac{di(t)}{dt} \tag{2.1.2}$$

the current rises from 0 to V_S/R as

$$i(t) = \frac{V_S}{R}\left(1 - e^{-t\frac{R}{L}}\right) \tag{2.1.3}$$

and the inductor voltage decays to zero volts according to

$$v_L(t) = V_S e^{-t\frac{R}{L}} \tag{2.1.4}$$

When the switch instantly connects the RL series to a short circuit the Kirchhoff equation becomes

$$-Ri(t) = L\frac{di(t)}{dt} \tag{2.1.5}$$

the current drops to zero as

$$i(t) = \frac{V_S}{R} e^{-t\frac{R}{L}} \tag{2.1.6}$$

and the voltage across the inductor instantly reverses to $-V_S$ and increases towards zero volts according to

$$v_L(t) = -V_S e^{-t\frac{R}{L}} \tag{2.1.7}$$

When the voltage source is disconnected to the load the reverse voltage spike across the inductor is constrained in amplitude to -V_S (a benefit of simultaneous switching). In fact, at the switching instant the broken inductor current path is replaced with an alternate one.

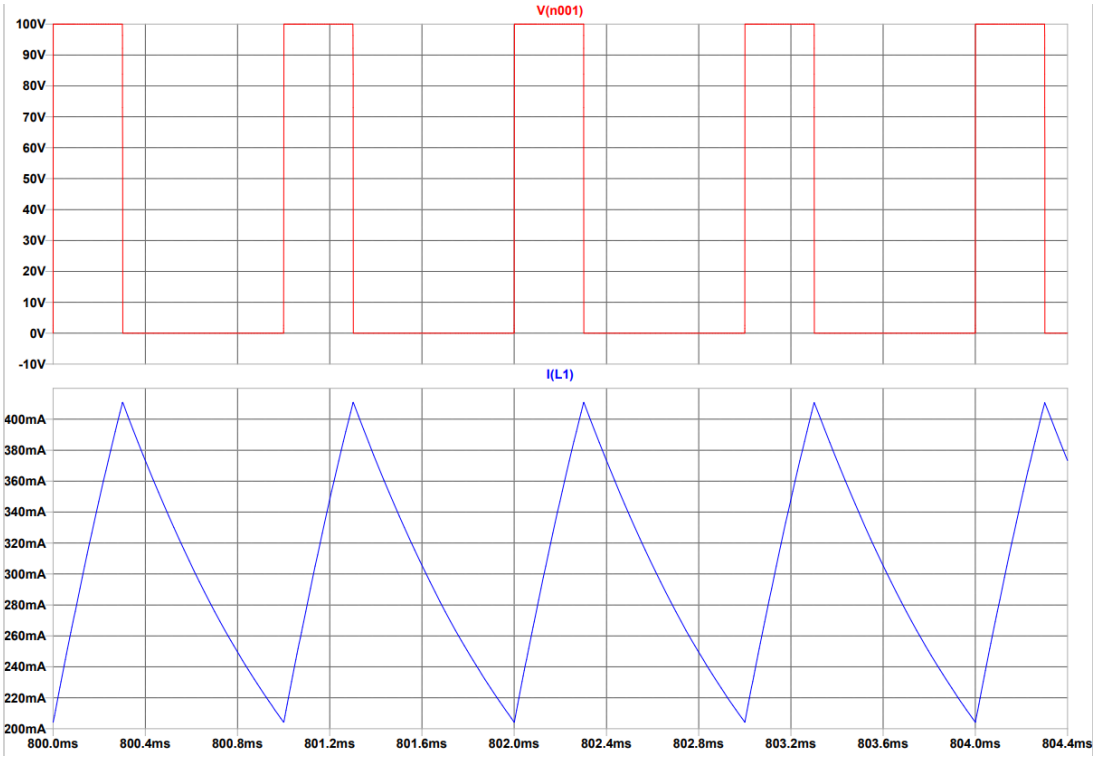

Figure 2.1.4: LTspice simulation: V(n001) inductor voltage v_L, I(L1) inductor current i_L in steady state for ideal switching case.

The above figure shows an LTspice simulation of the above circuit with $V_S = 100V$, $L = 0.1\,H$, $R = 100\,\Omega$ and a switching frequency of $1\,kHz$, with a 30% duty cycle. The continuous switching activity makes the current stabilizing around an average value that depends on the duration of the voltage pulses.

2.1.2 Single switch - real case

Actually a simultaneous dual switch is very difficult to implement. It is more likely that there would be a small gap time between the individual break and make switches that would result in a transient voltage spike greater than V_s, which could possibly drive an arc in the circuit. The inductor voltage spikes very quickly and gap time must be very fast or nearly zero.

More commonly inductors are switched on and off using an electro-mechanical or solid-state device that simply opens and closes the circuit to the inductor. However, the switching of inductive loads deserves special attention because this operation may lead to high-voltage transients that can damage the equipment.

Let's now take the example of the circuit in the figure below. It comprises the same inductor L and resistor R connected to a voltage source V_S through a switch.

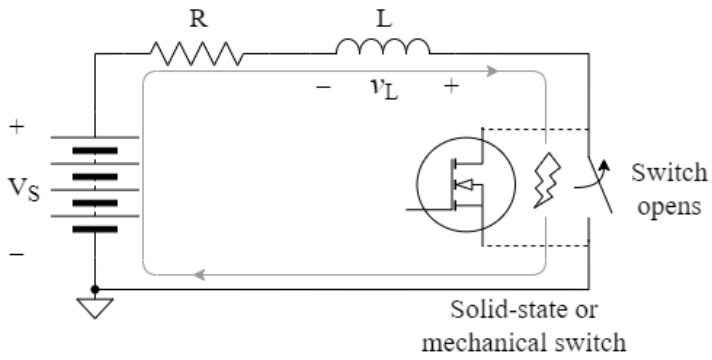

Figure 2.1.5: Circuit illustrating the issue with real inductive load switching.

Suppose that the switch is initially connected, and a given current $I_0 = V_S/R$ flows through the resistor and the inductor. This time, when the current path from the source is broken, no alternate path for the discharge current is introduced. The inductor resists an instant change its current from I_0 by instantly imposing a rapid reverse voltage across it that reinforces current flow in the inductor in the same direction as before the switch opened. The physical reason of this phenomenon is that the energy stored by the inductor (in the form of a magnetic field) must be abruptly released when its current vanishes. Upon discharging, the voltage across the inductor instantly reverse

to an unpredictable $-V_x$ (depending on the rate of drop of the current) and increases towards zero volts according to

$$v_L(t) = -V_x e^{-t\frac{R}{L}} \tag{2.1.8}$$

The negative voltage spike will go to whatever reverse amplitude is required to complete the current path that reinforces the initial steady-state inductor current prior to the switch opening. This high reverse voltage spike, if left unconstrained, can cause significant damage to any circuitry along the circuit path. For control via a mechanical switch, an arc may occur as the switch is being gapped open, eventually fouling its contacts, or the relay coil may arc over to metal inside the relay, like its armature. For a solid-state MOSFET switch, the high voltage reverse spike can destroy the switch. Moreover, a voltage spike distributed along the wiring between the switch and the load may generate noise in adjacent circuits by radiating or inductively coupling into adjacent conductors.

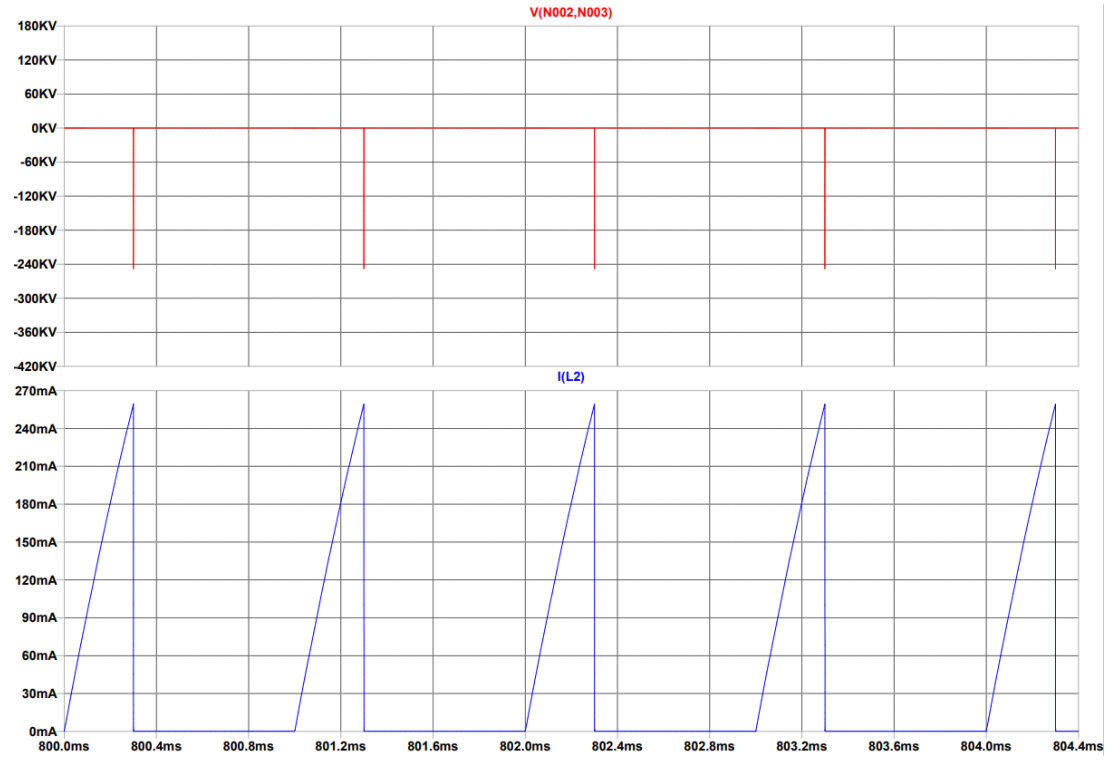

Figure 2.1.6: LTspice simulation: V(n002,N003) inductor voltage v_L, I(L2) inductor current i_L in steady state for real switching case.

The above waveforms are produced by simulating the circuit of Fig. 2.1.5, starting

from the same parameters as before. It's possible to notice the extremely high reverse voltage peaks across the inductive load at switch turn-off events.

A common solution to curb destructive switching transient voltage is illustrated in Figure 2.1.7. It requires a diode (known as freewheeling diode) in parallel with the inductive load.

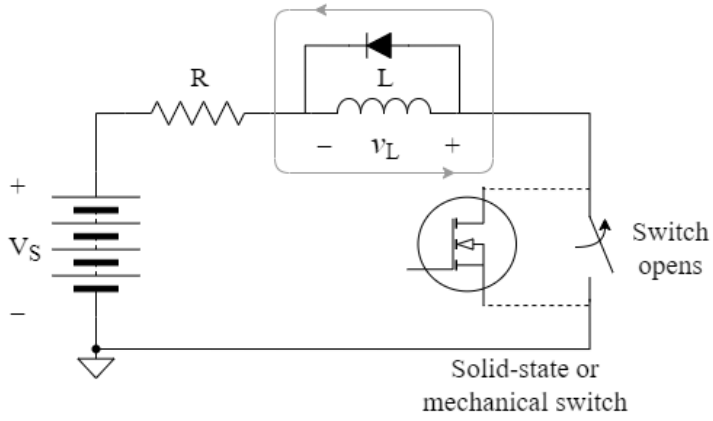

Figure 2.1.7: Circuit for real case switching including the freewheeling diode.

When the switch is closed, the diode is reverse-biased and therefore it does not effect the circuit. As the switch is opened, an alternate path for discharge current is present by placing the diode near the load. The voltage across the inductor instantly reverses to $v_L(t) = -V_D e^{-t\frac{R}{L}}$ but the magnitude V_D is clamped to the forward voltage drop of the diode. The stored energy $W_L = \frac{1}{2}LI_0^2$ in the inductor is instead dissipated via heat through the resistance of the coil-diode circuit.

The following figure shows the absence of reverse peaks at switch turn-off due to the freewheeling diode presence. The waveforms are comparable with the ones of Fig. 2.1.4.

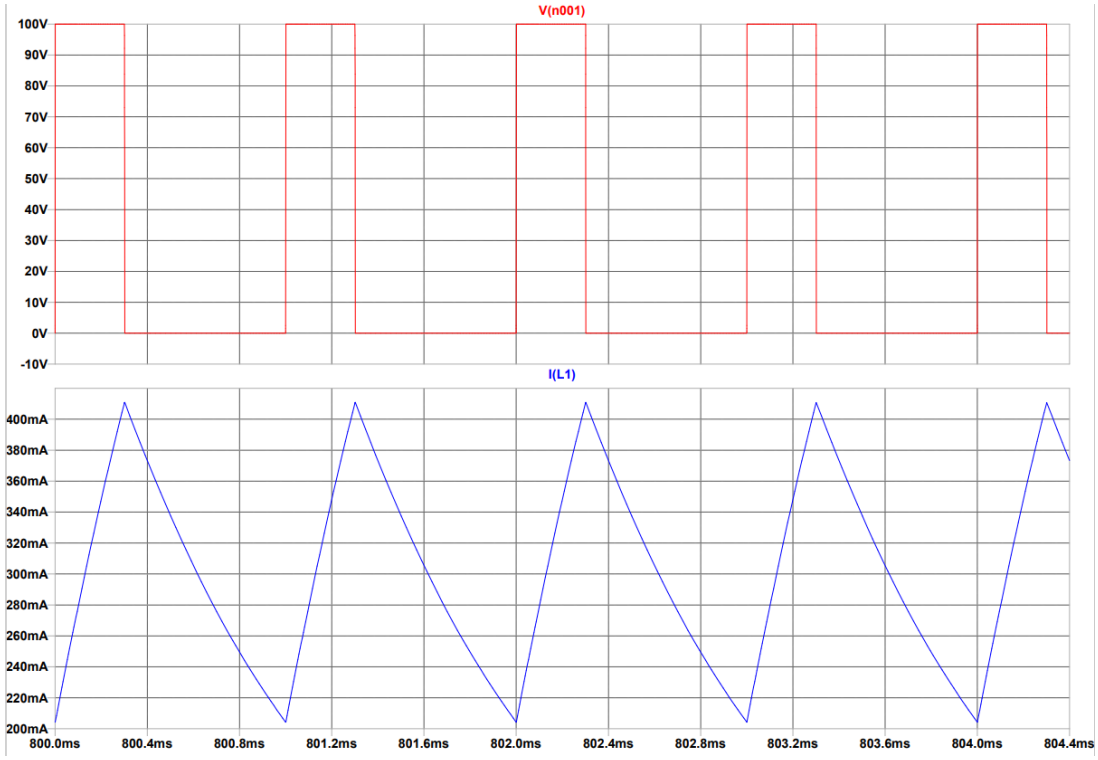

Figure 2.1.8: LTspice simulation: V(n001) inductor voltage v_L, I(L1) inductor current i_L in steady state for real switching case where a freewheeling diode is used.

It is usually recommended to add the freewheeling diode at the load even though solid-state switching devices like MOSFETs actually include a source-drain built-in diode that could shunt voltage spikes. However, building this protection local to the load being switched is important because it prevents the transient from being distributed along the wiring between the switch and load. To place it anywhere else would not be as effective and would allow the transient energy to move along the wiring back to the switch, radiating or inductively coupling noise into adjacent wiring and other devices, and possibly damaging the switch. Moreover, taking care of the switching device by avoiding stresses in excess of the nominal rating results in a higher operation reliability over time.

2.2 Current Mecc Alte voltage regulator output stage implementation

At this point, after having explained the basic theory of inductive loads driving, it is possible to present the current Mecc Alte implementation of the voltage regulator

output stage and in particular the device used to enable the exciter inductor driving.

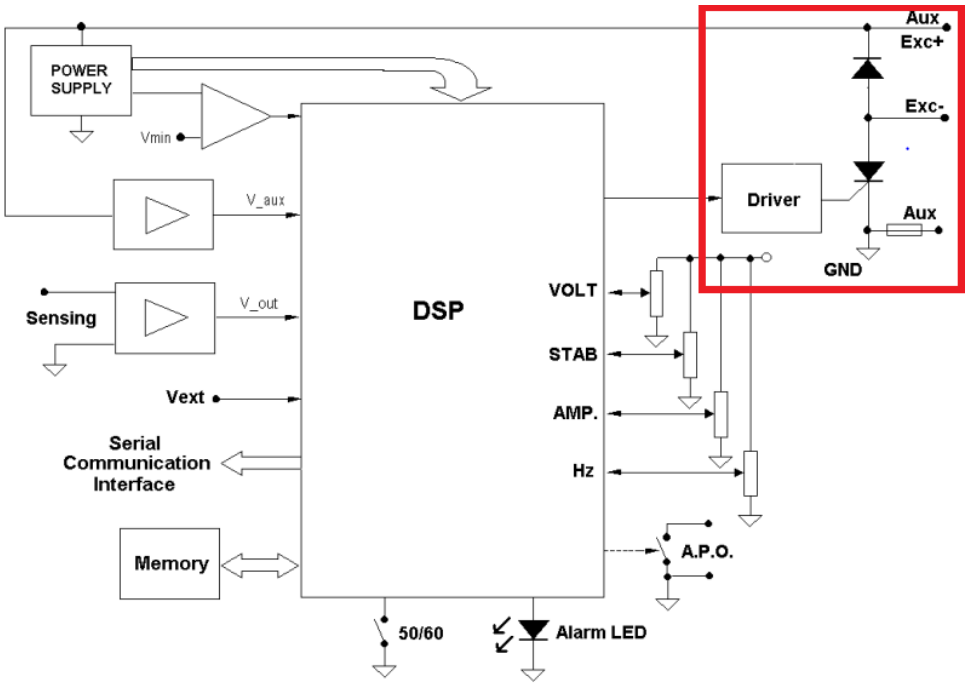

Figure 2.2.1: Block diagram of DSR Mecc Alte regulator [**22**]. In the red rectangle the output stage of the voltage regulator.

Such output stage can be fully described by the elements presented in the following circuit.

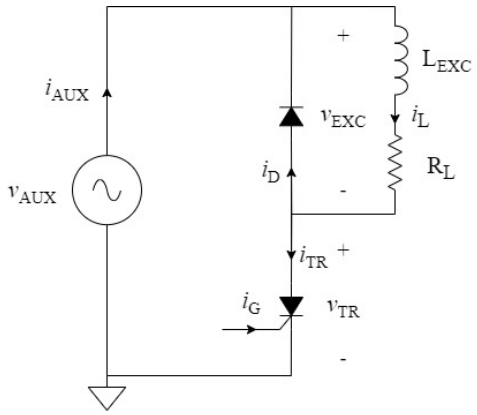

Figure 2.2.2: Current voltage regulator output stage implementation via thyristor.

The reader can recognize this circuit configuration is directly derived from the scheme of Fig. 2.1.2. It is possible to notice the auxiliary winding supply, represented as a voltage generator, on the right and the exciter stator represented as a RL series.

The freewheeling diode in parallel to the inductive load is placed as explained in Section 2.1.2. The switch consists of a thyristor that receives the gate command from the voltage regulator logic. A brief explanation of thyristors behaviour (Section 2.2.1) is necessary to understand how they can be used to operate the inductive load driving and therefore to regulate the current flowing through the exciter stator (Section 2.2.2). Finally, a short section about the limits of this implementation will introduce the next chapter.

2.2.1 Thyristors

Thyristors (sometimes termed SCRs, meaning semiconductor-controlled rectifiers) are one of the oldest types of solid-state power device and still have the highest power-handling capability. They are a latching switch that can be turned on by the control terminal (gate) but cannot be turned off by the gate.

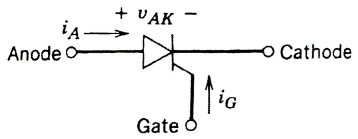

Figure 2.2.3: Thyristor circuit symbol [**2**].

The thyristor *i-v* characteristic (anode current i_A as a function of the anode-to-cathode voltage v_{AK}) shows the device operation.

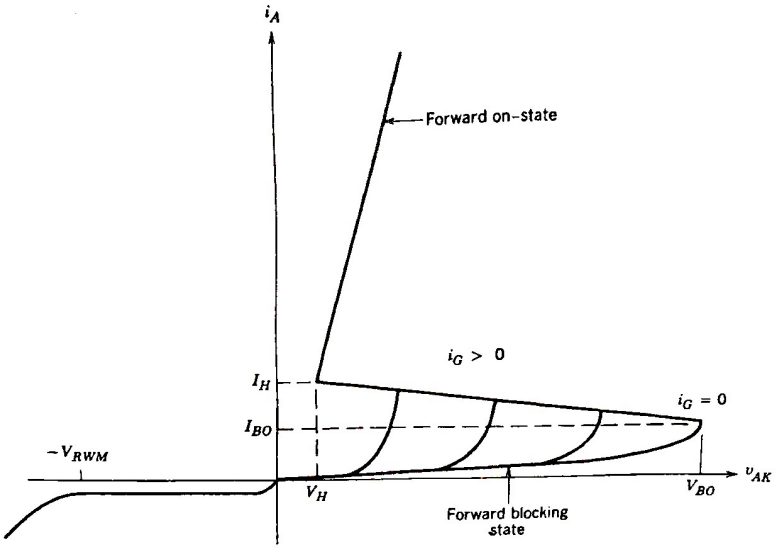

Figure 2.2.4: Thyristor current-voltage characteristic [**2**].

In the reverse direction the thyristor appears similar to a reverse-biased diode, which conducts very little current until avalanche breakdown occurs at V_{RWM}. In the forward direction the thyristor has two stable states of modes of operation that are connected together by an unstable mode that appears as a negative resistance on the *i-v* characteristic. The low-current, high voltage region is the forward-blocking state or the off-state, and the low-voltage, high current mode is the on-state.

Specific voltage and current values in the forward-bias quadrant of the *i-v* characteristic are of interest because they discriminate the regions of operation. The holding current I_H represents the minimum current that can flow through the thyristor and still maintain the device in the on-state. This current value and the accompanying voltage across the device, termed the holding voltage V_H, represent the lowest possible extension of the on-state portion of the *i-v* characteristic. For the forward-blocking state, the quantities of interest are the forward-blocking voltage V_{BO} (also termed breakover voltage because the *i-v* curve breaks over and goes to the on-state portion of the characteristic) and the accompanying breakover current I_{BO}.

The breakover voltage and current are defined for zero gate current, that is, the gate is open-circuited. If a positive gate current is applied to the thyristor, then the transition or breakover to the on-state will occur at smaller values of anode-to-cathode voltage, as indicated in Fig. 2.2.4. As shown in this figure, the thyristor will switch to the on-state at low values of v_{AK} if the gate current is reasonably large. Although not indicated on the *i-v* characteristic, the gate current does not have to be a DC current, but instead can be a pulse of current having some minimum time duration. This ability to switch the thyristor on by means of a current pulse has been the basis of the widespread applications of the device.

However, once the thyristor is in the on-state, the gate cannot be used to turn the device off. The only way to turn-off a thyristor is for the external circuit to force the current through the device to be less than the holding current for a minimum specified time period.

2.2.2 Circuit operation

Taking as a reference the circuit of Fig. 2.2.2 it is possible to show the operation of the circuit.

The steady-state condition is assumed: this means the switching activity makes the current flowing through the exciter stator (modeled as the series RL) to be a constant value equal to the average superimposed to a periodic ripple, as already seen in Section 2.1.1.

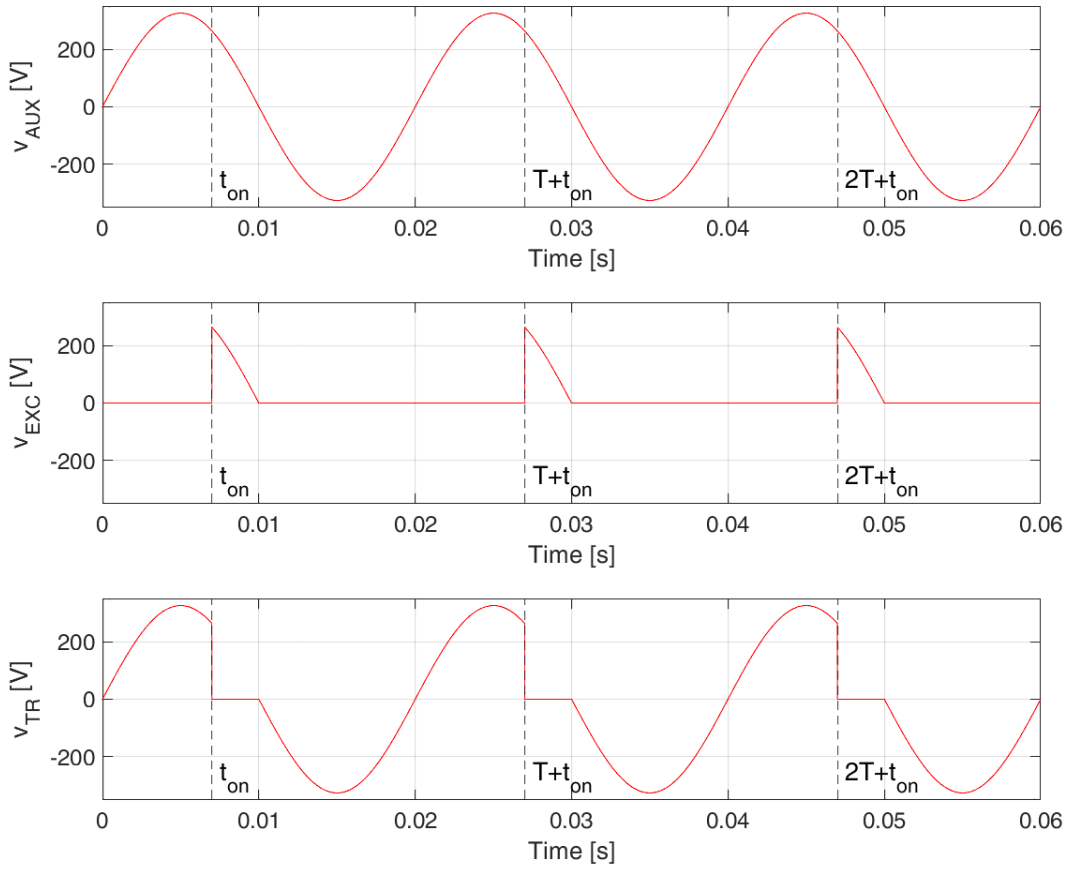

Figure 2.2.5: Voltages in the circuit.

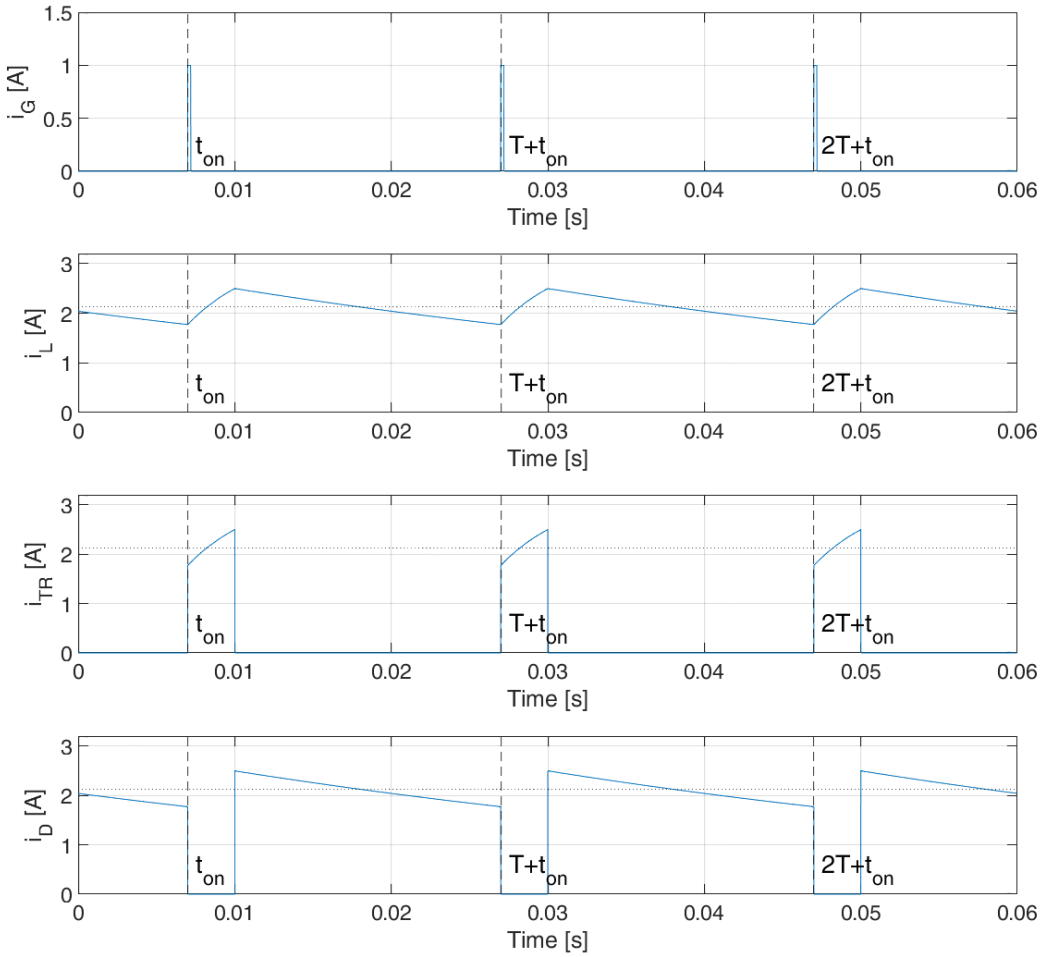

Figure 2.2.6: Currents in the circuit.

For the sake of illustration the plotted waveforms are produced considering the following parameters: auxiliary waveform having a frequency of $f = 50\,Hz$ and a root-mean-square voltage of $V_{AUX}^{rms} = 230\,V$; the thyristor trigger angle is $\alpha = 54°$ and the exciter stator parameters are $L_{EXC} = 0.5\,H$ and $R_L = 10\,\Omega$.

The auxiliary winding represented by an equivalent voltage generator applies a sinusoidal waveform between the nodes A and B of the circuit.

Focusing firstly on the half period in which the auxiliary voltage assumes positive values $[nT, nT + T/2]$ (T is the sinewave period and n a positive integer counter). Until a current pulse is not given to the thyristor gate terminal, the thyristor is in its off-state and can be approximated as an open circuit. The path for the current through the inductive load is provided by the freewheeling diode, that can be seen as a short

circuit in a first approximation. According to the RL series switching theory expressed in Section 2.1 in this considered time interval the current decreases exponentially with the time constant $\tau = L_{EXC}/R_L$. Thus voltages and currents in the circuit are:

$$\begin{cases} v_{EXC} = 0\,V \\ v_{TR} = v_{AUX} \\ i_L = i_D \\ i_{TR} = i_{AUX} = 0\,A \end{cases} \tag{2.2.1}$$

As a current pulse is given to the gate terminal of the thyristor at instants $nT + t_{on}$ the device breakovers to the on-state. Now the thyristor, behaving like a diode, can be approximated as a short circuit and the current i_L flows through the thyristor to close the loop on the "auxiliary" generator. The freewheeling diode, on the other side, turns off since the current is no longer flowing through. Since now the inductance is connected to a voltage generator by means of a resistor, the inductor current i_L grows exponentially according to the same time constant τ. In this time interval voltages and currents in the circuit are:

$$\begin{cases} v_{EXC} = v_{AUX} \\ v_{TR} = 0\,V \\ i_L = i_{TR} = i_{AUX} \\ i_D = 0\,A \end{cases} \tag{2.2.2}$$

As the auxiliary voltage reverses to negative values (during the second half period of the sinewave) the thyristor returns to the off-state. If, as assumed thus far, the thyristor in its on-state can be approximated as a short circuit, at instants $nT + T/2 + \epsilon$ the auxiliary voltage reverses and forward polarizes the freewheeling diode, turning it on. The current continuously flowing in the inductive load is forced to close the loop through the freewheeling diode. The absence of current in the thyristor makes it turn-off, as explained in Section 2.2.1. The situation is similar to the first analyzed interval: the freewheeling diode being a short circuit and the thyristor an open circuit, the voltages and currents assume the same values of system of Eq. 2.2.1. The inductor current i_L returns to exponentially decay like in the first analyzed time interval.

Up to now it has been explained that a thyristor is able to "cut" the sinewave voltage coming from the auxiliary winding and apply the voltage pulses to the exciter stator. Due to the inductive nature of the load, it is possible to induce on it a periodic current that, except for the superimposed ripple, has a constant value.

At this point, of the discussion it's clear that acting on the trigger angle α, by which current pulses are sent to the gate terminal of the thyristor, has a direct impact on the average current I_L flowing in the exciter stator. Using the model considered so far it is possible to derive the relation α-I_L. Since it is assumed to be in steady state condition and the focus is on the mean value of the current (no interest in the ripple), the volt-second balance principle can be applied to the inductance L_{EXC}. In switch-mode power conversion circuits "volt-second balance" refers to the fact that over one complete switching cycle the total volt-seconds applied to an inductor must be zero (in steady state):

$$\int_t^{t+T} v_L(\tau)d\tau = \int_t^{t+T} L_{EXC}\frac{di_L(\tau)}{d\tau}d\tau = L[i_L(t+T) - i_L(t)] = 0 \tag{2.2.3}$$

because of the periodicity of current i_L. For this reason, no voltage drops on the inductor in average value.

The average value V_{EXC} of v_{EXC} is going to fall all across the resistor terminal. Looking at the circuit of Fig. 2.2.2:

$$v_{EXC} = v_L + v_R \tag{2.2.4}$$

Taking the averages over the period T:

$$\int_t^{t+T} v_{EXC}(\tau)d\tau = \int_t^{t+T} v_L(\tau)d\tau + \int_t^{t+T} v_R(\tau)d\tau \tag{2.2.5}$$

$$V_{EXC} = V_L + V_R \tag{2.2.6}$$

$$V_{EXC} = V_R \tag{2.2.7}$$

Furthermore, the average current on the exciter I_L will be the average current flowing in the resistor, so $I_L = V_R/R_L$.

On the other side voltage V_{EXC}, being the average value of the voltage applied to the RL series, can be computed as a function of the trigger angle and the sinewave auxiliary voltage.

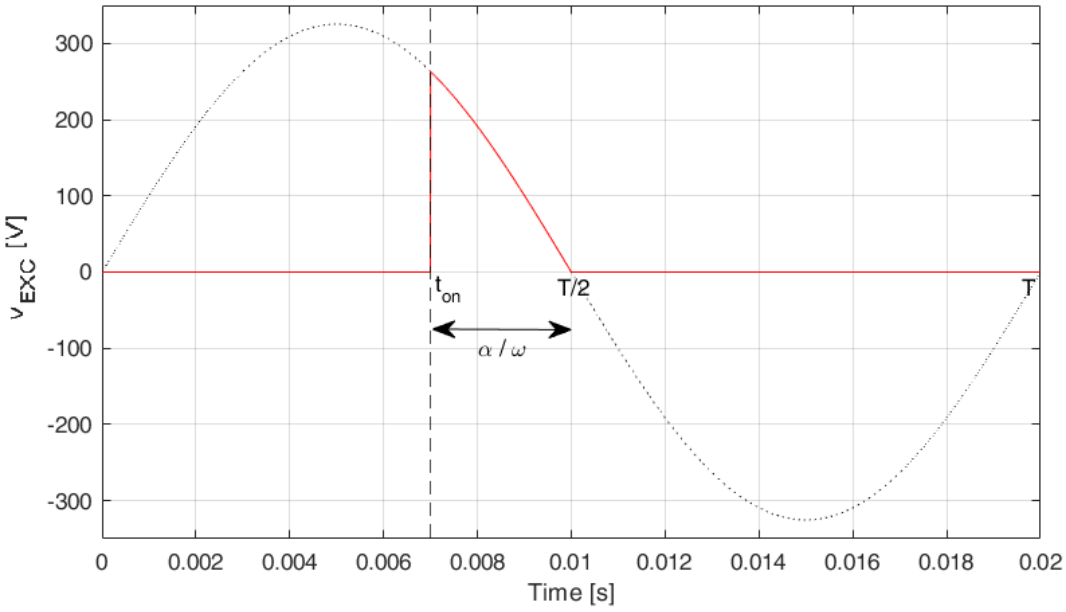

Figure 2.2.7: Exciter voltage.

The calculation is the following:

$$V_{EXC} = \frac{1}{T}\int_{t_{on}}^{T/2} v_{AUX}(\tau)d\tau = \frac{1}{T}\int_{t_{on}}^{T/2} \sqrt{2}V_{AUX}^{rms}\sin(\omega\tau)d\tau = \frac{V_{AUX}^{rms}}{\sqrt{2}\pi}\Big[1+cos(\omega t_{on})\Big] \tag{2.2.8}$$

that, in terms of $\alpha = \omega\Big(\frac{T}{2} - t_{on}\Big)$, can be reduced to

$$V_{EXC} = \frac{V_{AUX}^{rms}}{\sqrt{2}\pi}\Big[1+cos(\pi-\alpha)\Big] \tag{2.2.9}$$

Finally, the relation α-I_L is found:

$$I_L = \frac{V_R}{R_L} = \frac{V_{AUX}^{rms}}{\sqrt{2}\pi R_L}\Big[1+cos(\pi-\alpha)\Big] \tag{2.2.10}$$

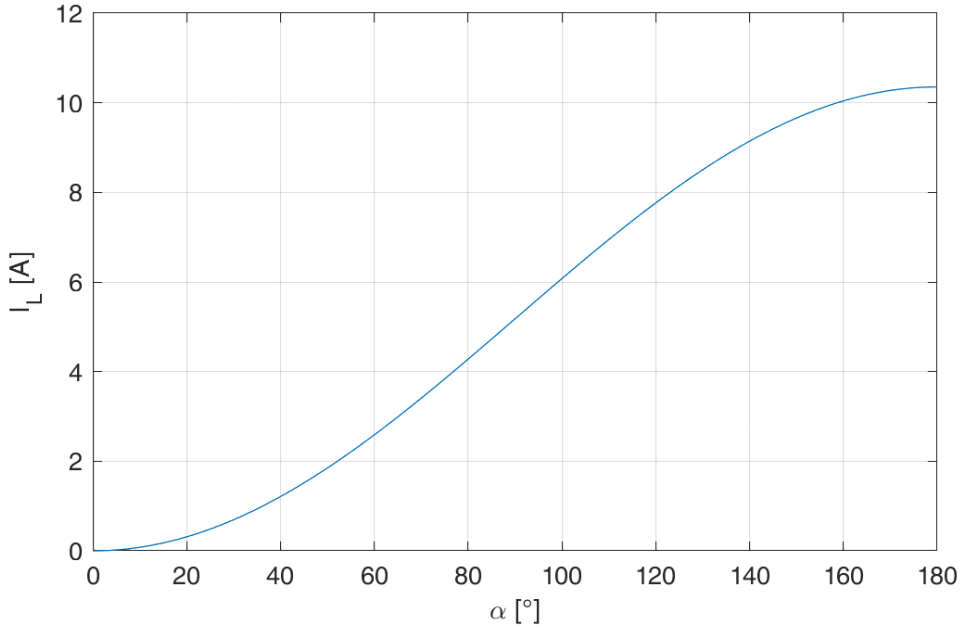

Figure 2.2.8: α-I_L relation.

2.2.3 Limits

As shown in the previous section, an output stage for a voltage regulator involving thyristors functions to enable control on the current flowing in the exciter stator and thus consequently on the voltage induced in the exciter rotor and finally the current in the main rotor. However, this configuration brings with it some as yet undiscussed aspects that make the utilization of thyristors more complex than one would expect on a first approach to the problem.

The first aspect is linked to the fact that the current pulse needs to be given to the gate terminal of the thyristor at the desired trigger angle within the first half period of the waveform generated by the auxiliary winding. This means the regulator logic needs firstly to "synchronize" on the auxiliary waveform and then to compute the time interval after which the current pulse to the gate terminal must be applied. Synchronization means that the regulator must recognize the waveform zero crossings. This activity needs the execution of a custom algorithm, typically implemented in the regulator microcontroller. This would not require an excessive effort, if not for the fact that the auxiliary voltage results not to be an ideal sinewave. Instead, due to noise, the waveform undergoes multiple zero crossings.

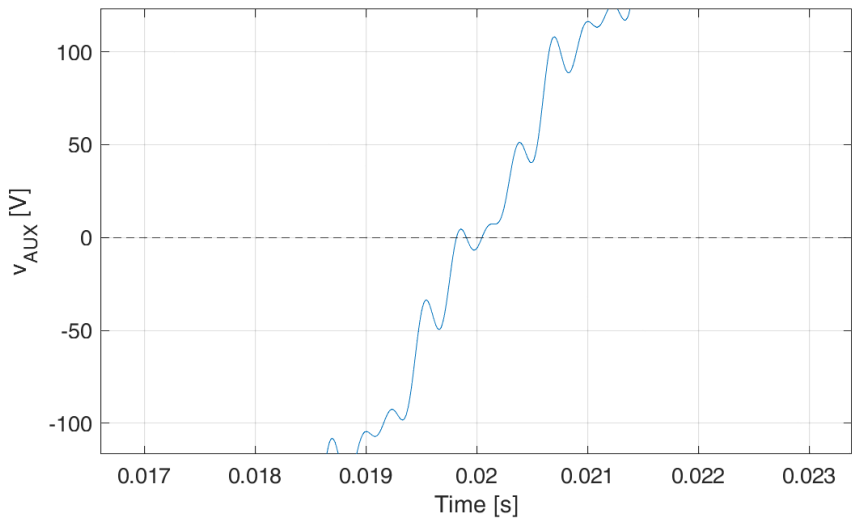

Figure 2.2.9: Extra zero crossings in auxiliary winding voltage waveform.

A further aspect that makes the synchronization problem a non-trivial task is that the auxiliary winding is arranged in the main stator in such a way that the induced EMF is not even expected to be a sinusoidal waveform. Actually the auxiliary voltage presents a significant third harmonic content, needed to satisfy the short circuit oper-

ation requirement, of which a more detailed discussion will be provided in the next chapter. It is possible that in some working conditions the third harmonic content is so high that the auxiliary voltage undergoes extra zero crossing that mustn't be accounted for the synchronization task, adding complexity to the algorithm.

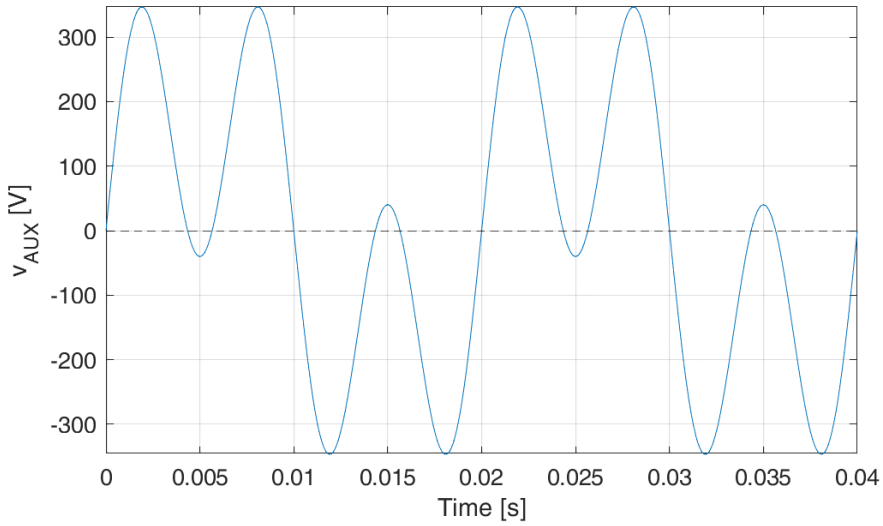

Figure 2.2.10: Auxiliary winding voltage waveform having a third harmonic content which causes extra zero crossings.

It has to be specified the microcontroller firmware developed by Mecc Alte solves the issues related to synchronization. An appropriate strategy to recognize and discard extra zero crossings due to noise and third harmonic amplitude, based on a series of filters and time windows, is currently used in the company AVRs. However, a much simpler implementation of the microcontroller firmware would be sufficient in the case if synchronization was not required and the way the gate command is given to the device was independent of the waveform generated by the auxiliary winding.

A second aspect of placing a limit on the circuit implementation involving thyristors is the missing exploitation of the negative half period auxiliary voltage to drive the exciter stator. The reader may have noticed that the trigger angle can only span the range $[0°, 180°]$. This prevents the utilization of the energy carried by the waveform in the second half period. The energy of a voltage waveform is in fact linked to the square of the voltage itself, making the energy in a period equally divided in the two half periods. This means that the utilization of thyristors to implement the power stage of the regulator gives the disadvantage of losing half of the energy that is specifically generated in order to energize the excitation system. A diode bridge to rectify the sinusoidal waveform could potentially remove this issue, since the negative voltage half

period would reverse to positive values and be exploited like first half period. However, it should be remembered that a diode bridge cannot be used since the thyristor in the considered circuit can turn-off only if the anode-to-cathode voltage reverses. Otherwise there would be a situation in which the thyristor, after the first breakover to the on-state, would remain forever turned on, losing the control of the current I_L.

As discussed, the choice to use thyristors in order to implement the output stage of the voltage regulator, brings with it some disadvantages that could actually be removed if the thyristor was substituted by a both turn-on and turn-off controllable power switch, like a power MOSFET or IGBT.

Chapter 3

Development of the voltage regulator output stage circuit

This chapter is the core of the thesis. The actual development of the circuit, from the company requirements and the component selection, through the circuit simulation, the faced issues and the proposed solutions until the actual circuit production are discussed in Chapter 3.

3.1 Company request

It should be remembered that this thesis comes from an internship activity at Mecc Alte. The objective of this internship is to investigate an alternative approach, with respect to thyristor, to drive the exciter stator for the synchronous generator voltage regulator. The output stage used in regulators up to the present day is of course working well on the whole wide range of available alternators. However, the utilization of a both turn-on and turn-off controllable power switch takes with it many advantages, some of them mentioned at the end of the last chapter, that will be discussed and summarized in the conclusion chapter.

3.2 Project specification

The project specification is fundamental as the first step of project flow because it provides the design input needed to develop the project.

Since the circuit developed in this activity must deal with the same synchronous generators currently controlled by the regulator implemented via thyristor, the project

specification, on which the design is based, is almost identical. Even if this thesis activity could potentially be exploited to study and realize a higher-performing stage (in terms of providing higher exciter stator current values from lower auxiliary voltage levels), this would not make sense because the upstream decision was that the proposed regulator output stage is designed to be backwardly compatible to fit existing Mecc Alte products. These machines are designed to sustain up to a certain amount of current through their conductors and going beyond such bounds would be counterproductive because of magnetic saturation and windings overheating.

The meaningful project specification for this application, that consists of the worst-case scenario, in terms of stresses, the circuit has to deal with, are:

- the maximum peak value of the input alternating voltage provided by the auxiliary winding: $V_{peak} = 450\,V$. This value matches the voltage rating of the electronic components mounted on the voltage regulator board;
- the nominal RMS value of the auxiliary voltage in steady condition: $V_{AUX}^{rms} = 230\,V$;
- the maximum constant current that must be provided to the exciter stator: $I_L = 6.5\,A$.

As regards the voltage specifications, it should be remembered that the waveform produced by the auxiliary winding is not a pure sinewave but contains an important third harmonic content needed to guarantee the correct machine operation in a particular working condition, that is the short circuit test. The reason for this is explained in greater depth in Subsection 3.2.1. The RMS and the peak values of such voltage are not dependent only on the machine, but also on the load connected to the alternator. The armature reaction induced by the load has, among its effects, the effect of raising and distorting (in the sense of modifying the harmonics amplitudes) the auxiliary voltage waveform. The voltage design inputs reported above are a consequence of such considerations.

With regards to the maximum exciter stator current a similar analysis is used. The current that needs to flow through the exciter stator, in addition to being dependent on the kind of machine, is extremely prone to the effects of a load attached to the generator. In fact, the armature reaction that is generated when a load is connected to the generator, modifying the total magnetic flux linked to the main stator windings, has a direct impact on the current requested to flow through the exciter stator. In particular, the armature reaction induced by an inductive or resistive load requires an increase in the exciter stator current to be able to maintain the output voltage at the

nominal value. In the uncommon capacitive load case, instead, a smaller current value would be sufficient. Despite the typical increase in requested current due to the load connection, the situation involving the maximum current is the *short circuit* test, briefly described in the following subsection.

3.2.1 Short circuit test

The short circuit test on the synchronous machine has two goals:

- the determination of the short circuit machine characteristics, that is the current provided short circuiting the phases as a function of the excitation current;
- the measurement of the conductor losses for efficiency evaluation.

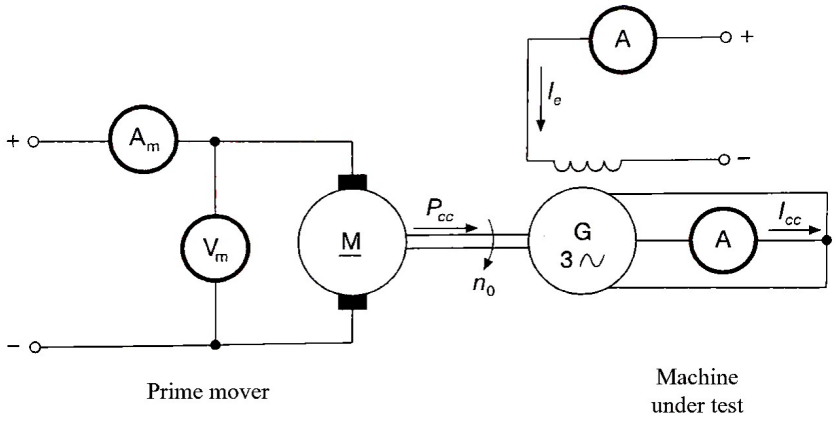

Figure 3.2.1: Short circuit test scheme for the synchronous machine [**1**].

The excitation current is regulated by acting on the current flowing through the exciter stator, as already explained.

The reader should know a particular legislation regarding synchronous generators for marine application requires each synchronous generator to be able to provide a short circuit current I_{SC} equal to three times the machine nominal current I_N. The peaks of current and torque the machine is subjected represent the highest mechanical and electrical stresses, which allow also to assess the ability of the alternator to supply large inductive loads, like motors.

A non-trivial consequence of generator short circuit operation is the effect on the auxiliary winding induced waveform. Unlike the main three phases, which feature almost null voltages because short circuited, the auxiliary winding, which is an extra

winding electrically isolated from the ones that make up the three phases, continues to present an induced voltage at its terminals. However, this induced waveform is strongly affected by the armature reaction manifesting in the short circuit situation. In the case of large load, like the short circuit, the generator works in "strong desaturation" condition: the excitation system provides the highest excitation current possible; at this point the first harmonic of each stator winding alternating voltage is gradually attenuated (also the auxiliary one). For this reason, it is necessary to design an auxiliary winding having a geometric arrangement such that the energy induced is not concentrated only in the first harmonic, but also in higher order harmonics. This is the reason why the auxiliary winding is rearranged in such a way the induced voltage is rich in third harmonic content. During the short circuit test the third harmonic is the only one surviving and providing the energy to use in order to drive the exciter stator and energize the excitation system.

Among every possible functional situation a synchronous generator can face up to, it is known that reaching $3 \cdot I_N$ during the short circuit test is the worst-case scenario for the excitation system in terms of current that has to be flow through the exciter stator, even more than the fully-demagnetizing case of the purely inductive load.

3.3 Circuit development

This section is intended to give to the reader a detailed explanation about the project development process: the justifications for the design choices, the encountered issues, the solution attempts and the reasons for their failures and the final solution chosen. The starting point is the willingness to substitute the thyristor with both a controllable turn-on and turn-off power switch, typically a power MOSFET or IGBT. The reason for this choice has already been explained in Subsection 2.2.3 about the limits of the regulator output stage implementation via thyristor. The use of a power MOSFET or IGBT is able to provide advantages, some explained in such subsection, others presented later on as the thesis discussion is developed. From this point on the reader can appreciate the design steps that have characterized the development of the project. The submission order of such steps is the same logical order with which it has been addressed to propose the solution for this problem.

3.3.1 Switching frequency

The first design choice regards the controllable power switch commutation frequency on which the exciter stator current regulation is performed. Differently from the thyristor, whose switching frequency is forced to coincide with the $50\,Hz$ alternating auxiliary waveform frequency, in the case of both a controllable turn-on and turn-off switch it is possible to uncouple from the characteristics of such supply waveform. For this reason, the designer has the freedom to choose the appropriate operating frequency, of course within the limits set by physical properties of commercially available devices.

Regulation velocity Since the driving frequency of the inductive load is not forced to be $50\,Hz$ any more, there is a clear advantage in raising the switching frequency because of a direct impact on regulation velocity. In fact, operating at $50\,Hz$ allows to update the trigger angle once every switching period $T_S = \frac{1}{f_S} = 20\,ms$. This may be critical in transient events, for example in a load connection or disconnection: at the instant such event happens, the generator output voltage undergoes a step in its value due to armature reaction phenomenon, linked to the kind of load supplied by the machine. Even making two assumptions: the first being the firmware uploaded on the regulator microcontroller performing a continuous sampling activity on the output voltage sensed signal and so recognizes immediately a difference between the setpoint and the sensed value; the second being the instantaneous microcontroller execution of the control algorithm for computation of the regulator output (the command for the switch), one must wait till the next switching period T_S before applying the latest updated trigger angle. No command can be sent to the switch before the next period because the regulator logic has to recognize a new zero crossing determining a new period from which to wait for the trigger event. This places an upper limit on the regulation velocity, that could be improved if the switching period was reduced.

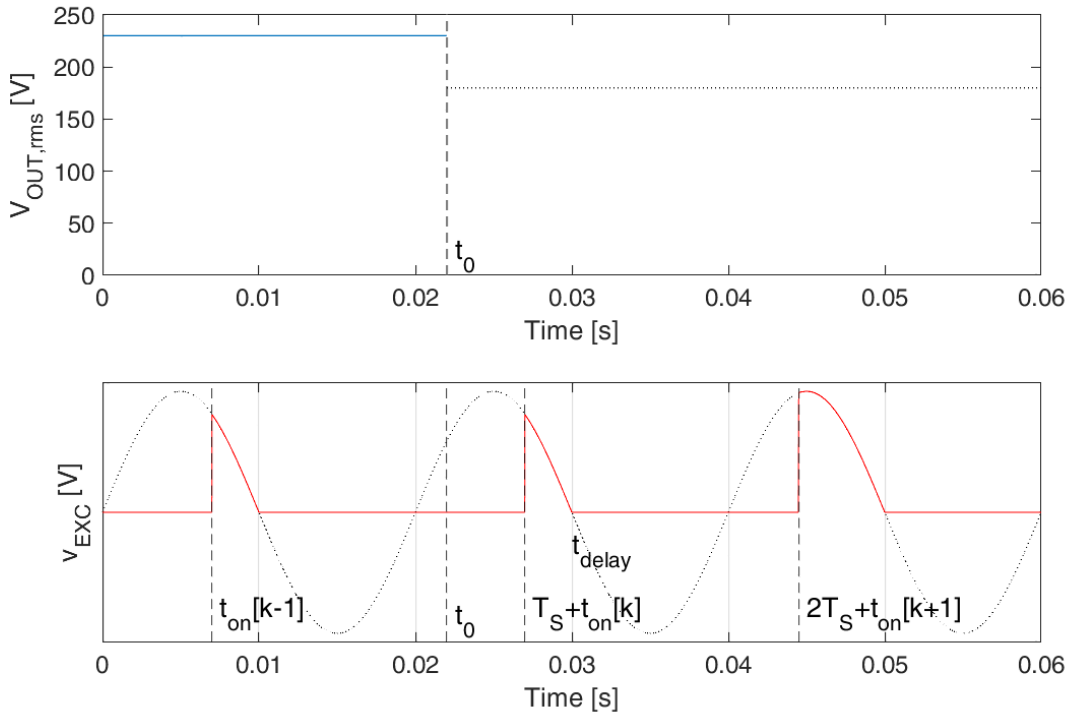

Figure 3.3.1: Evidence of delay time from load connection at t_0 to the next switching period, when a new command to the switch can be applied.

Exciter stator current ripple Another reason to increase the switch commutation frequency regards its effect on the inductive load current waveform. As described in Section 2.2.2 the application of a pulsed voltage waveform to an inductive RL load generates a periodic current characterized by a constant value superimposed on a ripple. Such a ripple acts as undesired noise in the excitation system chain: an oscillating current through the exciter stator generates an oscillating magnetic field, that induces non-sinusoidal EMF on exciter rotor windings and a less constant current on the main rotor electromagnets. Eventually the effect is to distort the synchronous generator output voltage to a non-ideal sinewave. Where possible, it is always better practice to reduce upstream any possible source of disturbance. Increasing the switch commutation frequency allows the reduction of the current ripple amplitude. In fact, as will be demonstrated, its value is inversely proportional to the switching frequency.

The value of the current ripple ΔI_L can be computed looking either at the switch on or off phase. For example, looking at the off phase it is recalled the switch can be seen as an open circuit, while the path for the current through the inductive load is provided by the freewheeling diode, that can be seen as a short circuit. In the off

period the inductive load switching circuit illustrated in Fig. 2.1.7 is simplified by the following circuit:

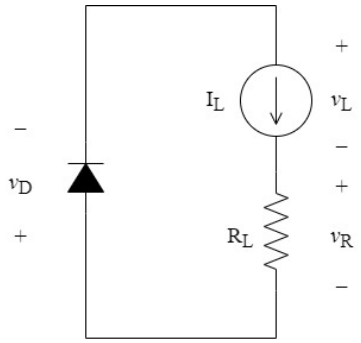

Figure 3.3.2: Equivalent circuit during the thyristor off phase.

For the sake of computation a constant current equivalent to the average value is assumed to flow in the circuit. The voltage across the inductor v_L is shown to be the reverse of the sum of the voltage drop across the parasitic resistance $v_R = R_L \cdot I_L$ plus the voltage drop on the diode, negligible in a first approximation. Given $t_{off} = (1-d) \cdot T_S$ the off phase time duration, With these assumptions the current will vary linearly in time, producing a current ripple equal to

$$\Delta I_L = \frac{v_L}{L} t_{off} = \frac{R_L \cdot I_L}{L}(1-d) \cdot T_S = \frac{R_L \cdot I_L}{L}\frac{(1-d)}{f_S} \tag{3.3.1}$$

After having shown the current ripple amplitude dependence on the switch commutation frequency, it is clear the best choice would be to raise the frequency as much as possible to obtain small current ripple. However, in addition to the physical limits of on the market power switches to reach arbitrary high frequencies, another reason preventing the choice of very high frequencies is shown below.

Switching losses An ideal switch is represented in a generic manner by the circuit symbol shown in Fig. 3.3.3. No current flows when the switch is off and, when it is on, current can flow in the direction of the arrow only.

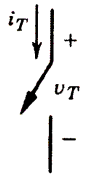

Figure 3.3.3: Generic controllable switch [**2**].

The ideal controllable switch has the following characteristics:

- block arbitrarily large forward and reverse voltages with zero current flow when off;
- conduct arbitrarily large currents with zero voltage drop when on;
- vanishingly small power required from control source to trigger the switch;
- switch from on to off or vice versa instantaneously when triggered.

Real devices, as intuitively expected, do not have these ideal characteristics and hence will dissipate power when they are used. In particular, the non-ideality in the instantaneous switch from one state to the other is an important factor that could make the device dissipate too much power, leading to its failure and, in doing so, the damage of the other system components.

In order to explain the link between the switching frequency and the switching power losses, a simplified version of the inductive load drive circuit is considered, shown below.

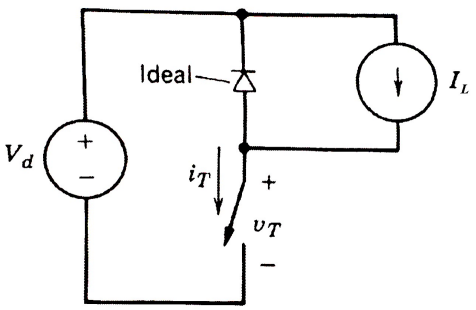

Figure 3.3.4: Simplified version of inductive load drive circuit [**2**].

The DC current source approximates the current that would actually flow due to inductive energy storage. The diode is assumed to be ideal because the focus is on the switch characteristics, though in practice the diode reverse-recovery current can significantly affect the stresses on the switch.

When the switch is on, the entire current I_L flows through the switch and the diode is reverse biased. When the switch is turned off, I_L flows through the diode and a voltage equal to the input voltage V_d appears across the switch, assuming a zero voltage drop across the ideal diode.

Figure 3.3.5b shows the waveforms for the current through the switch and the voltage across the switch when it is being operated at a switching frequency of $f_S = 1/T_S$, with T_S being the switching time period. The switching waveforms are represented by linear approximations to the actual waveforms in order to simplify the discussion.

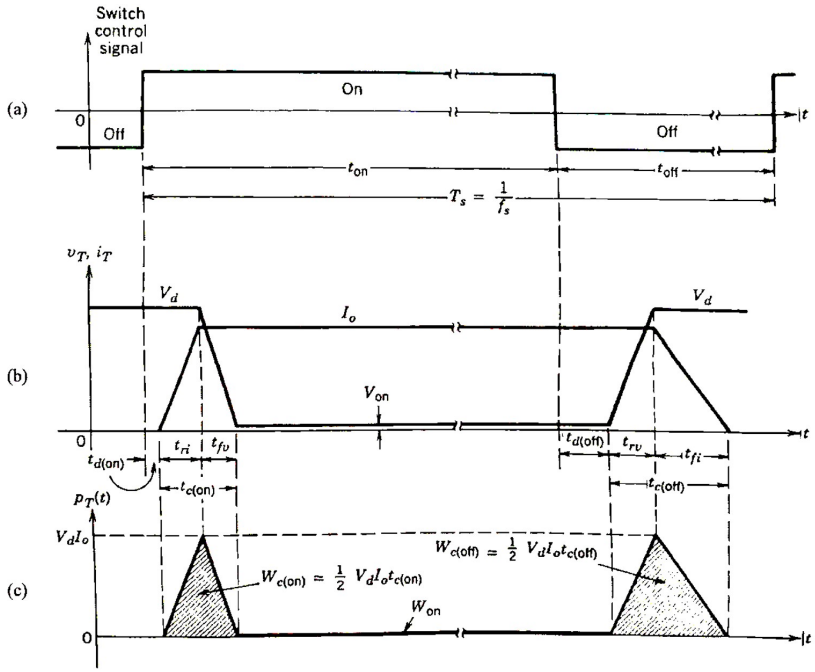

Figure 3.3.5: Switch waveforms and instantaneous switch power loss [**2**].

When the switch has been off for a while, it is turned on by applying a positive control signal to the switch, as shown in Fig. 3.3.5a. During the turn-on transition of this generic switch, the current buildup consists of a short delay time $t_{d,on}$ followed by the current rise time t_{ri}. Only after the current I_L flows entirely through the switch can the diode become reverse biased and the switch voltage fall to a small on-state value, negligible for this discussion, with a voltage fall time of t_{fv}. The waveforms indicate that large values of switch voltage and current are present simultaneously during the

turn-on crossover interval $t_{c,on} = t_{ri} + t_{fv}$.

The energy dissipated in the device during this turn-on transition can be approximated from Fig. 3.3.5c as

$$W_{c,on} = \frac{1}{2} V_d \cdot I_L \cdot t_{c,on} \tag{3.3.2}$$

where it is recognized that no energy dissipation occurs during the turn-on delay interval $t_{d,on}$.

In order to turn the switch off, a negative control signal is applied to the control terminal of the switch. During the turn-off transition period of the generic switch, the voltage build-up consists of a turn-off delay time $t_{d,off}$ and a voltage rise time t_{rv}. Once the voltage reaches its final value of V_d, the diode can become forward biased and begins to conduct current. The current in the switch falls to zero with a current fall time t_{fi} as the current I_L commutates from the switch to the diode. Large values of switch voltage and switch current occur simultaneously during the crossover interval $t_{c,off} = t_{rv} + t_{fi}$. The energy dissipated in the switch during this turn-off transition can be written, using Fig. 3.3.5c, as

$$W_{c,off} = \frac{1}{2} V_d \cdot I_L \cdot t_{c,off} \tag{3.3.3}$$

where no energy dissipation occurs during the turn-off delay interval $t_{d,off}$.

The instantaneous power dissipation $p_T(t) = v_T \cdot i_T$ plotted in Fig. 3.3.5c makes it clear that a large instantaneous power dissipation occurs in the switch during the turn-on and turn-off intervals. There are f_S such turn-on and turn-off transitions per second. Hence the average switching power losses P_S in the switch due to these transitions can be approximated from Eqs. 3.3.2 and 3.3.3 as

$$P_S = \frac{1}{2} V_d \cdot I_L \cdot f_S \cdot (t_{c,on} + t_{c,off}) \tag{3.3.4}$$

This is an important result because it shows that the switching power loss in a semiconductor switch varies linearly with the switching frequency. Choosing a large value means increasing the dissipated power. Increasing the dissipated power means a greater effort and cost in removing the heat from the device die and disperse it in the ambient. For this reason, the designer has all the interest in the minimization of power losses. Therefore, from this point of view lowering the switching frequency is desirable.

From the three above mentioned switching frequency discussions about regulation velocity, exciter stator current ripple and switching losses it is evinced that the designer

has not a complete freedom in choosing the operating frequency for this application. Instead, as it happens rather often in any engineering field, the switching frequency choice is the result of a trade-off between many different issues that must be all kept into account in order to provide a good choice.

As results of this discussion it has been decided that a good switching frequency is in the order of $1\,kHz$. This allows to exploit the benefit of a both turn-on and turn-off controllable power switch in order to provide a significant gain in terms of regulation velocity and current ripple with respect to the thyristor-based implementation.

As regards the regulation velocity, if before the control signal could be updated once every $20\,ms$, an about 20 times shorter switching period allows to update the control signal approximately every millisecond. Regarding the current ripple there is an around 20 times reduction too. Assuming the project specification load current of $I_L = 6.5\,A$ and the typical exciter stator $L = 0.8\,H$ and $R_L = 10\,\Omega$, the worst-case current ripple changes from $\Delta I_{L,max,50Hz} = 1.625\,A$ to about $\Delta I_{L,max,1000Hz} = 0.081\,A$. Being such ripple approximately the 1.25% of the average value, from now on the inductive load current i_L in the case of the higher switching frequency implementation is going to be considered equal to its average value I_L. Simultaneously the around $1\,kHz$ switching frequency value results small enough to make sure that switching losses represent a negligible amount with respect to the total device operating power loss. A dedicated treatment showing this is provided in Chapter 4.

For a reason explained in Subsection 3.3.4 the ultimate value of the chosen switching frequency for this application is set to $f_S = 976\,Hz$.

3.3.2 Full wave rectification

One of the thyristor-based implementation limits exposed in Section 2.2.3 regards the impossibility to exploit the entire energy carried by the auxiliary winding to supply the excitation system. Only the positive half wave of the alternating auxiliary waveform is used to generate the voltage pulses sent to the inductive load in the currently used voltage regulator release. The reason for this is in the thyristor physical working principle: once the gate terminal is supplied by a current pulse and the thyristor turns-on, the device acts exactly as a diode. It conducts until the current through it is not brought to zero by the external circuit. To make this happen, the thyristor anode-to-cathode voltage has to reverse to negative values: assuming the thyristor is a short circuit when on, as the auxiliary alternating voltage reverses a positive bias forward-polarizes the freewheeling diode, making it to conduct. The current through the inductive load is drawn by the freewheeling diode, interrupting the current flow through the thyristor,

which turns off. If no zero crossing was present between the anode and cathode of the thyristor (as if a full wave rectifier was used) the current through it wouldn't have way to close up in the alternative path constituted by the freewheeling diode. Thus, it means once turned on the first time, the thyristor is not able to turn off any more and so no control is performed on the inductive current average value I_L. This is a clear disadvantage in the use of a thyristor as power switch because it automatically prevents the exploitation the energy carried by the negative half wave of the auxiliary waveform, that accounts for the half of the total energy, since it is proportional to the square of the voltage. The entire energy carried by the auxiliary waveform can instead be exploited if a controllable power switch is used: independently on the voltage applied across the device terminals, if a negative control signal is applied to the control terminal of the switch, the current flow through the device is interrupted and directed to the freewheeling diode. For this reason, a full wave rectifier can be used. A diode bridge performs exactly this task: it rectifies the input alternating voltage waveform so the voltage pulses from either positive or negative half waves can be exploited to energize the inductive load and eventually supply the excitation system. The advantage in rectifying the auxiliary waveform and being able to exploit all the energy carried by it is the possibility to obtain higher current ratings on the exciter stator starting from the same supply alternating waveform or, on the contrary, to obtain the same current level from a smaller amplitude auxiliary alternating voltage. Assuming the waveform amplitude V_{AUX} is fixed, it can be shown that a rectified waveform is able to produce up to the double of the current on the load. Recalling the relation between the average voltage applied to the load V_L and the inductive current I_L of Eq. 2.2.10, the maximum values for the average current respectively for the two cases are:

$$I_{L,max,halfwave} = \frac{V_{AUX}}{\pi \cdot R_L} \tag{3.3.5}$$

$$I_{L,max,fullwave} = \frac{2V_{AUX}}{\pi \cdot R_L} \tag{3.3.6}$$

A direct consequence of this result is that, seen from the opposite perspective, the same current level from the not rectified waveform can be obtained by a half amplitude rectified waveform.

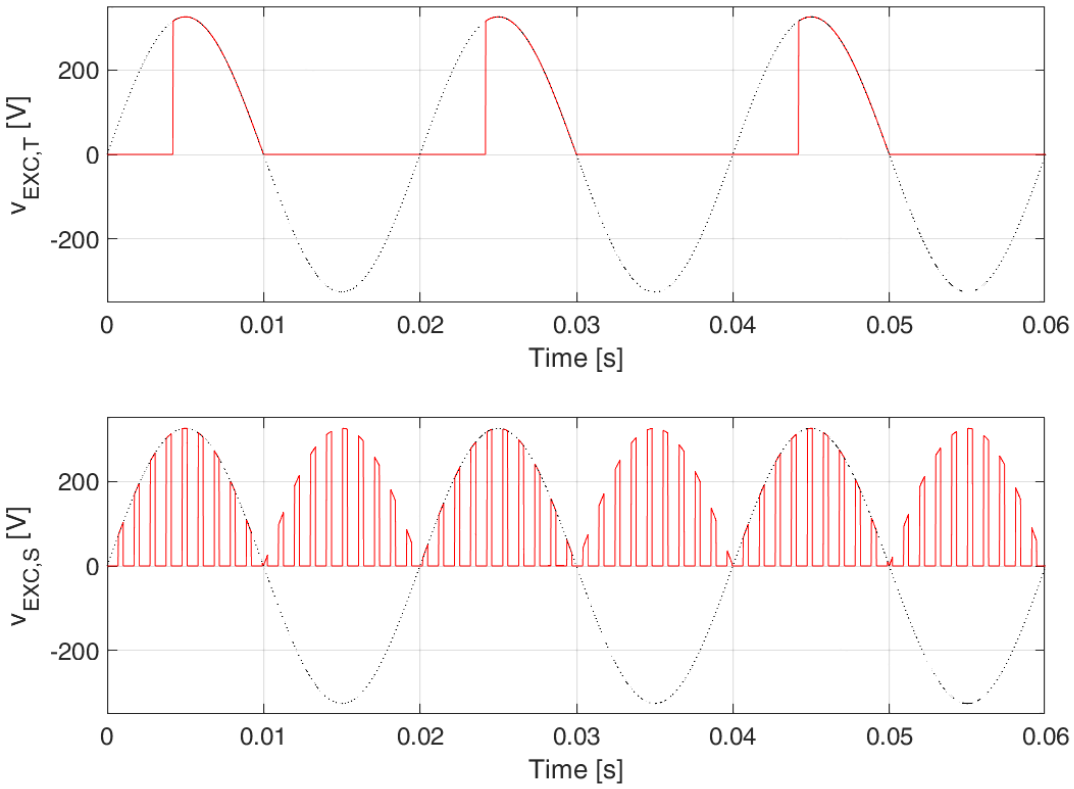

Figure 3.3.6: Exciter stator voltage pulses from not rectified auxiliary voltage for thyristor implementation and rectified auxiliary voltage for controllable switch implementation. The switching frequency for the second plot is the one decided in the last section, being 976 Hz. The pulse duration is chosen in order to provide the same I_L current starting from the same auxiliary voltage amplitude (remember I_L is independent of the switching frequency).

The chosen commercial device for implementing such task is the GBU4J silicon bridge rectifier [**31**]. It is a 4 A nominal current at 50°C, 600 V repetitive peak reverse voltage, less than 1 V forward voltage diode bridge. The reader should not get confused by the device current rating to be less than the 6.5 A flowing through the inductive load. The average current provided by the diode bridge is well below the datasheet limitation.

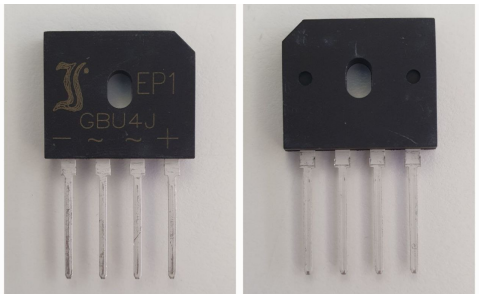

Figure 3.3.7: GBU4J silicon bridge rectifier [**31**].

3.3.3 Controllable power switch

The core of the output stage of the voltage regulator is surely the power switch.

The aim of this thesis is to substitute the currently used MCR8SN thyristor [**34**] with a both turn-on and turn-off controllable power device. Typically used switches for this kind of applications are power MOSFETs or IGBTs. The justification for the choice made in this thesis is to be found in two reasons.
The first is the suitability of the device voltage and current ratings on the actual application. Similarly to the MCR8SN thyristor, an about 800 V repetitive off-state voltage, 8 A on-state RMS current power switch is desired, because this ratings well suited the requirements of the company. In the case of IGBTs, commercially available devices having similar off-stage sustainable voltage are characterized by either 750 V or 900 V repetitive collector-to-emitter off-state voltage. However, for such voltage ratings the current capabilities are much greater, at least 20 A, which is not needed in this application.
The second reason is the device cost: searching on the main online electronic components sellers it turns out that power MOSFETs, with needed ratings, has on average a lower price than similar ratings IGBTs. The cost is an important factor to consider in the design of a solution for the industrial world. It is comprehensible that, since each alternator is sold with its voltage regulator mounted on, the massive production of voltage regulators implies the desire to minimize as much as possible the cost of each component. Every little saving multiplied times lots of regulator replicas allows the company to maximize the profit.

For these reasons, the real device chosen to implement the controllable switch is the STP13N80K5 power MOSFET [**32**]. It is an N-channel low gate charge, low on resistance MOSFET suited to switching application, which provides 800 V drain-source breakdown voltage and 12 A continuous drain current at 25°C.

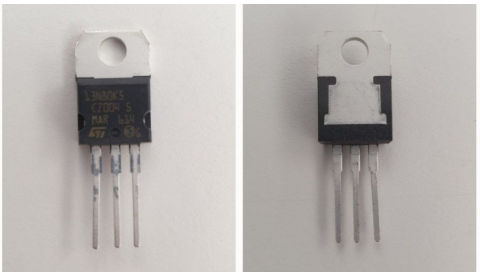

Figure 3.3.8: STP13N80K5 power MOSFET [**32**].

3.3.4 Driving circuit

While a description of the internal structure of a power MOSFET is considered not interesting in the thesis discussion, a brief explanation about the physics of the MOSFET control operation and the MOSFET circuit models is useful to introduce the driving circuit used to control the power switch for the application developed in this thesis.

The MOSFET is a three-terminal device where the input, the gate, controls the flow of current between the output terminals, the drain and the source. In power electronics applications, the MOSFET traverses the i_D-v_D characteristics from cutoff through the active region to the ohmic region as the device turns on and back again when it turns off. The cutoff, active and ohmic regions of the characteristics are shown on the following figure.

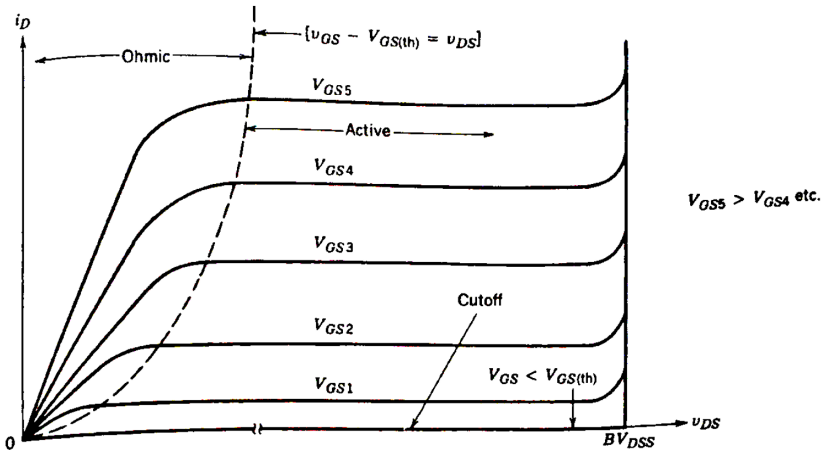

Figure 3.3.9: Current-voltage characteristics of an n-channel enhancement mode MOSFET [**2**].

The gate portion of the MOSFET structure is the key to understand how the MOSFET operates. The gate region is composed of the gate metallization, the silicon dioxide

underneath the gate conductor, which is termed the gate oxide, and the silicon beneath the gate conductor. This region forms a high-quality capacitor, as shown in Fig. 3.3.10 and sometimes termed the MOS capacitor.
When a small positive gate-source voltage is applied to the capacitor structure in the simplified diagram of the n-channel MOSFET shown in Fig. 3.3.10a, a depletion region forms at the interface between the SiO_2 and the silicon. The positive charge induced on the upper metallization (the gate size) by the applied voltage requires an equal negative charge on the lower plate, which is the silicon side of the gate oxide. The electric field form the positive charge repels the majority-carrier holes from the interface region and thus exposes the negatively charged acceptors, thus creating a depletion region.

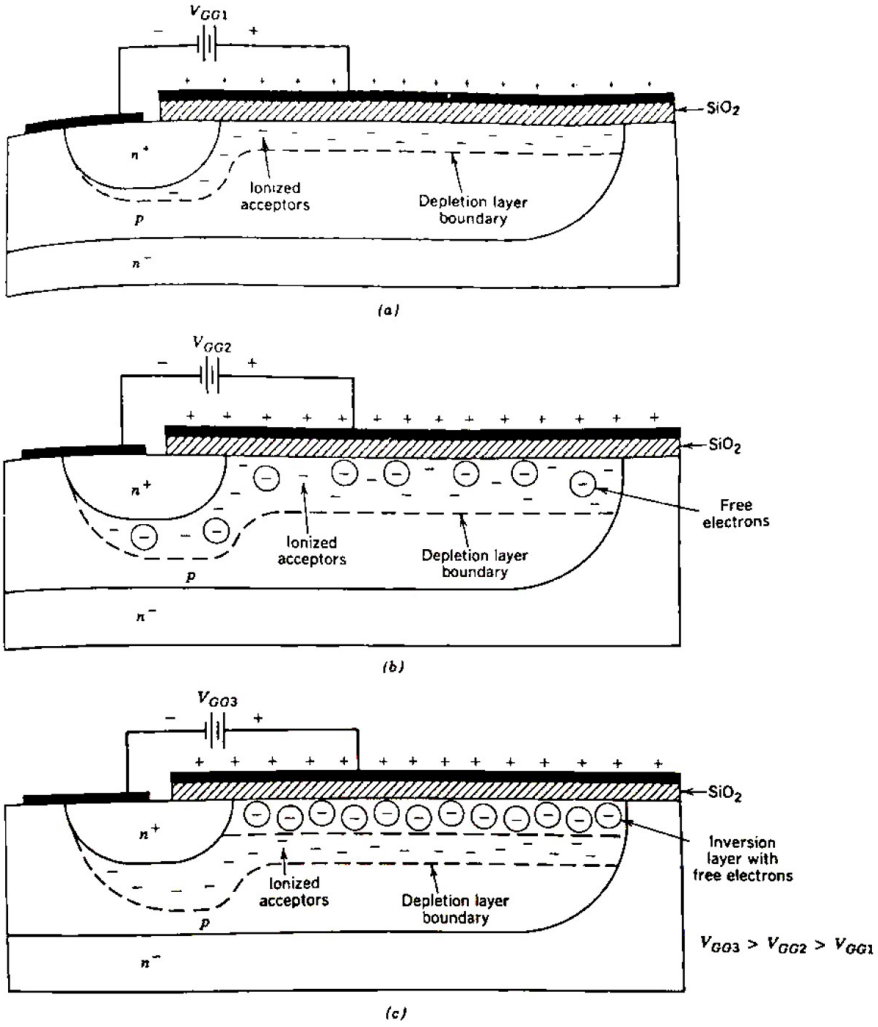

Figure 3.3.10: (a) Formation of the depletion layer. (b,c) Inversion layer at the Si-SiO_2 interface as the gate-source voltage is increased [**2**].

Further increases in v_{GS} cause the depletion layer to grow in thickness, as is shown

in Fig. 3.3.10b, to provide the additional negative charge. As the voltage is increased, the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as well as repelling free holes. The immediate source of the electrons is electron-hole generation via thermal ionization with the free holes being pushed into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons that are attracted from the n^+ source by the positive charge of the holes.

Eventually, as the bias voltage is increased, the density of free electrons at the interface will become equal to the free hole density in the bulk of the body region away from the depletion layer. The layer of free electrons at the interface will be highly conducting and will have all the properties of a n-type semiconductor. At this point, the layer of free electrons is termed an inversion layer, as is illustrated in Fig. 3.3.10c. This n-type layer realizes a conductive path channel between the n^+ drain and the source regions, which permits the flow of current between source and drain.

The value of v_{GS} where the inversion layer is considered to have formed is termed the threshold voltage $V_{GS,th}$. As v_{GS} is increased beyond $V_{GS,th}$, the inversion layer gets thicker and more conductive as the density of free electrons gets larger as the bias voltage increases. The inversion layer screens the depletion layer adjacent to it from the further bias voltage increases so that the depletion layer thickness now remains constant. The value of the threshold voltage is a function of several factors. Some of them are the oxide capacitance $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ (where ϵ_{ox} is the dielectric constant of the silicon dioxide and t_{ox} is the thickness of the gate oxide), the work functions of the silicon and the gate metal, any charge bound or trapped in the silicon dioxide, impurities at the interface or in the silicon dioxide. For example, the gate-source threshold voltage of the STP13N80K5 power MOSFET has a value around $4\,V$.

MOSFETs are the fastest among the power semiconductors switches because the transition from the off to on-state (and vice versa) implies only the charges that must be moved on the stray capacitances and depletion layer capacitances, which are shown in the cross-sectional view of the MOSFET in Fig. 3.3.11. In other types of semiconductor switches, like bipolar devices, excess minority carriers must be moved into or out of the device as it turns on or off.

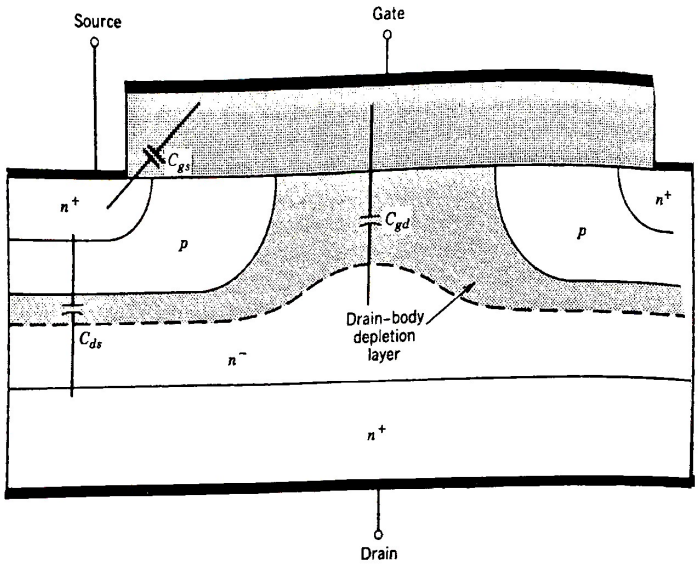

Figure 3.3.11: Cross-sectional view of an n-channel MOSFET showing the origin of the parasitic capacitances that governs the switching speed of the device [**2**].

These capacitances can be modeled by an equivalent circuit which is valid when the MOSFET is in cutoff or in the active region, that means during MOSFET commutations. The drain-source capacitance shown in Fig. 3.3.11 is not included in the equivalent circuit because it does not materially affect any of the switching characteristics of waveforms. In the following figure the MOSFET equivalent circuit is inserted in the simplified version of the inductive load drive circuit.

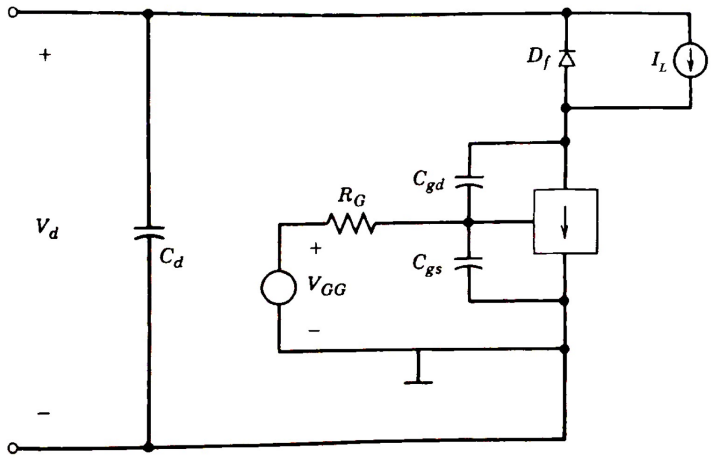

Figure 3.3.12: The MOSFET equivalent circuit applied to a simplified version of inductive load drive circuit [**2**].

The gate is driven by an ideal voltage source, which is assumed to be a step voltage

between zero and V_{GG} in series with an external gate resistance R_G. During the turn-on process the gate-source voltage v_{GS} rises from zero to $V_{GS,th}$ because of the currents flowing through C_{gs} and C_{gd}. The rate of rise of v_{GS} is, in a first approximation, the exponential one of an RC circuit. In fact, it is possible to further simplify the MOSFET equivalent model and represent it as follows.

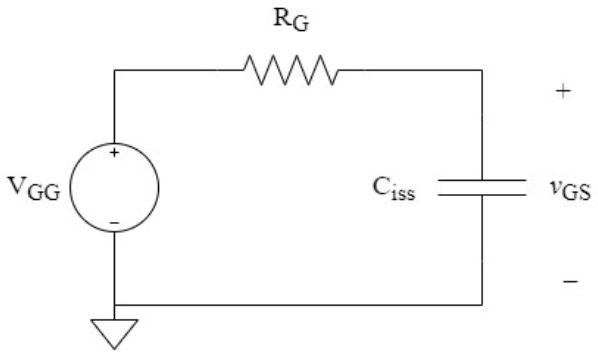

Figure 3.3.13: The MOSFET equivalent circuit to model the rise of the gate-source voltage v_{GS}.

C_{iss} is the input capacitance, and is the capacitance obtained by totaling the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd}; it is the capacitance of the MOSFET as a whole, as seen from the input. This capacitance must be driven (charged) in order to cause the MOSFET to operate, and so is a parameter of importance when studying the drivability of an input device or input losses. Q_g is the amount of charge necessary to drive (charge) C_{iss}. It is clear a large input gate current can carry more charge on the input capacitor and eventually rise faster the gate-source voltage to the threshold value. This is why a power MOSFET is not driven directly by the digital output pin of a microcontroller. The limited amount of current a microcontroller can supply leds to a slow input capacitor charging time. The consequences are large crossover intervals for v_{DS} and i_D, which both set an upper limit for the MOSFET switching frequency and raise switching power losses.

In order to allow faster turn-on and turn-off commutations and reduce the power dissipated during transitions, one should charge (and discharge) the input C_{iss} capacitance as fast as possible. This task requires specific circuits, called gate drivers. These devices can supply (and sink) large output currents, typically greater than $1\,A$ (compared to the typical tens of milliamps capability of a microcontroller output pin).

The gate driving task is assigned to the EVALSTGAP1AS evaluation board, that is a board implementing all the circuitry needed for the STGAP1AS chip operation. The STGAP1AS is a galvanically isolated single gate driver for N-channel MOSFETs and

IGBTs with some protection, configuration and diagnostic features. The architecture of the STGAP1AS is perfect for a thesis work: in a first prototyping step, like the one treated in this activity, the isolation of the channel from the control and the low voltage interface circuitry through galvanic isolation is a very important safety feature. The STGAP1AS is suited for a voltage rating up to 1500 V and is capable of sourcing (and sinking) 5 A at 25°C. Power switches in both TO-220 or TO-247 packages can be evaluated, and the board allows the connection of a heatsink.

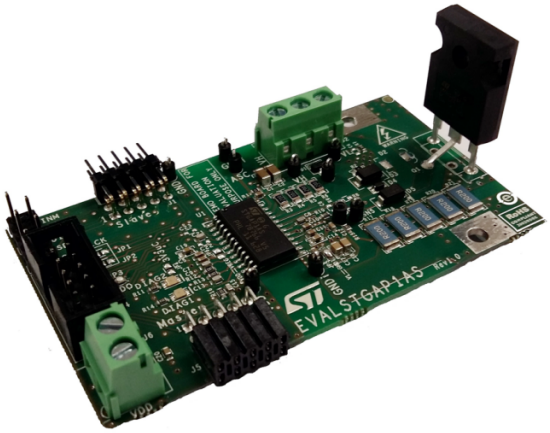

Figure 3.3.14: EVALSTGAP1AS evaluation board.

The EVALSTGAP1AS evaluation board is in combination with the STEVAL-PCC009V2 communication board and the STGAP1AS evaluation software, which allow to enable, configure or disable all of the driver's protection and control features through the SPI interface.

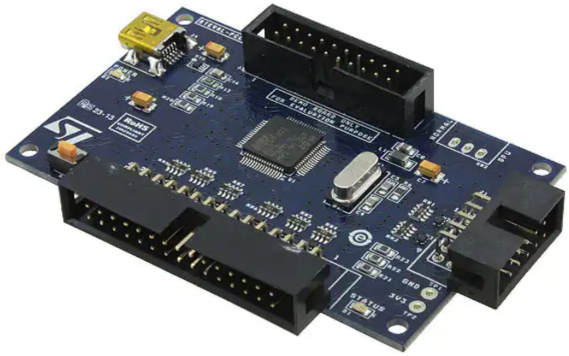

Figure 3.3.15: STEVAL-PCC009V2 communication board.

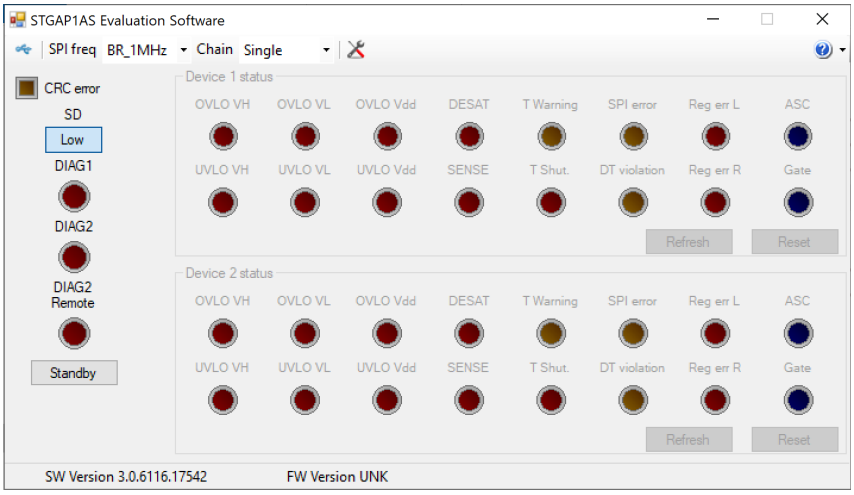

Figure 3.3.16: STGAP1AS evaluation software.

The control signal sent to the logic side of the gate driver is managed by the Arduino Uno microcontroller board. It allows to program easily and generate a 5 V PWM signal suited for the 3.3/5 V logic input interface of the STGAP1AS gate driver.

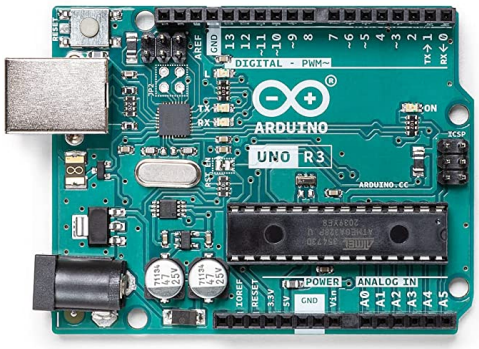

Figure 3.3.17: Arduino Uno Rev3 microcontroller board.

The Arduino PWM signal is generated from a 31250 Hz or 62500 Hz timer depending on the digital pin. It is possible to program the PWM frequency acting on the timer prescaler, which divides the timer frequency by a set of predefined numbers, being 1, 8, 32, 64, 128, 256 and 1024. This way, it is possible to obtain a PWM signal having a carrier frequency very similar to the one identified in Subsection 3.3.1: $31250/32 \simeq 976\ Hz$.

3.3.5 Freewheeling diode

As already described the freewheeling diode is required to provide an alternative path for the inductive load current to flow when the main switch is closed. For this reason, such diode acts in a complementary way with respect to the power switch: when the MOSFET is off the diode is forward biased, it begins to conduct with only a small forward voltage across it (in the order of $1\,V$). As the switch turns on, the diode is reversed biased; only a negligibly small leakage current flows through the device until the reverse breakdown voltage is reached. In order to be able to block the reverse voltage, the reverse-bias should not reach the breakdown rating.

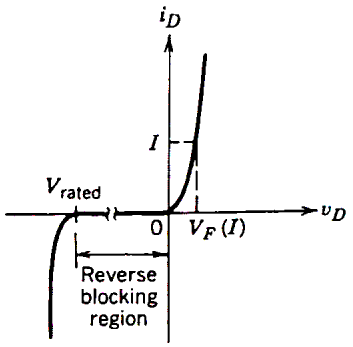

Figure 3.3.18: Diode *i-v* characteristics [**2**].

A brief description of the internal structure of a power diode is necessary to understand its behaviour in its switch-operation mode. Differently from their low-power counterparts, power diodes are more complicated in structure and operational characteristics. The power *pn* junction consists of a heavily doped *n*-type substrate on top of which is grown a lightly doped n^- epitaxial layer of specified thickness. Finally, the *pn* junction is formed by diffusing in a heavily doped *p*-type region that forms the anode of the diode. The thickness W_d of the drift region determines what the reverse breakdown voltage will be. Instead, the cross-sectional area of the diode will vary according to the amount of total current the device is designed to carry.

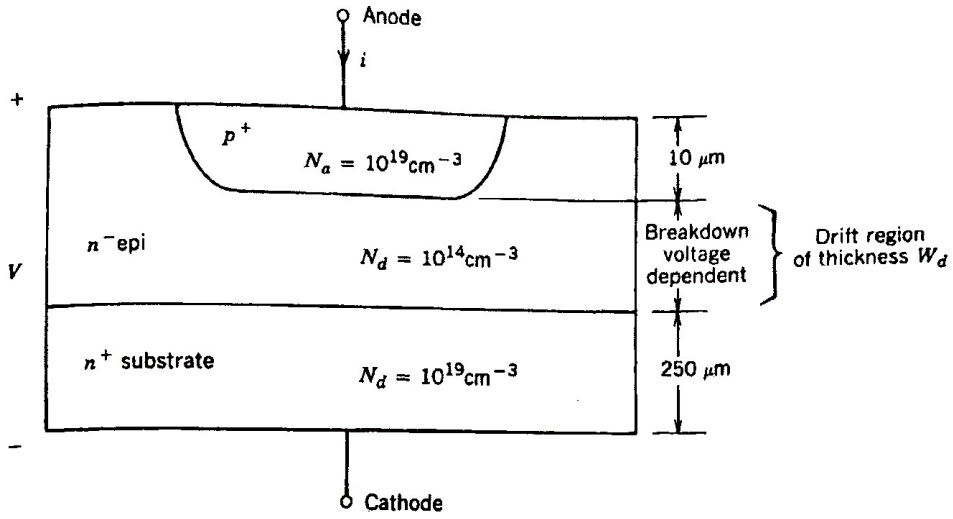

Figure 3.3.19: Cross-sectional view of a *pn*-junction diode intended for power applications [**2**].

At turn-on, the diode can be considered an ideal switch because it turns on rapidly compared to the transients in the power circuit. However, at turn-off, the diode current reverses for a reverse-recovery time t_{rr}, as is indicated in Fig. 3.3.20, before falling to zero. This reverse-recovery (negative) current is required to sweep out the excess carriers stored in the drift region of the diode before the metallurgical junctions can become reverse biased. Once the carriers are removed by the combined action of recombination and sweep-out by negative diode currents, the depletion layer acquires a substantial amount of space charge from the reverse-bias voltage and expands into the drift region from both junctions. As long as there are excess carriers at ends of the drift region, the p^+n^- and n^+n^- junctions must be forward biased. Thus, the diode voltage will be little changed from its on-state value except for a small decrease due to ohmic drop caused by the reverse current. But after the current goes negative and carrier sweepout has proceeded for a sufficient time to reduce the excess-carrier density at one or both junctions to zero, the junctions become reverse biased. At this point, the diode voltage goes negative and rapidly acquires substantial negative values as the depletion regions from the two junctions expand into the drift region toward each other. At this time the negative diode current demanded by the stray inductance of the external circuit cannot be supported by the excess-carrier distribution because too few carriers remain. The diode current ceases its growth in the negative direction and quickly falls, becoming zero. The reverse current has its maximum reverse value I_{rr}.

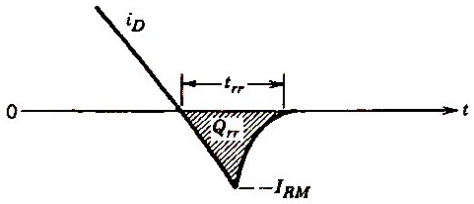

Figure 3.3.20: Diode turn-off [**2**].

The reverse-recovery current can lead to overvoltage in inductive circuits and raises the switching power losses of the switching devices, in particular the power MOSFET. For these reasons, a fast recovery diode is desirable. It should have voltage and current ratings comparable with the power MOSFET ones. The STTH1210D power diode is chosen [**33**]. It is an ultrafast, high voltage diode: its main characteristics are 1000 V breakdown voltage, 12 A average forward current and a typical reverse-recovery time of 48 ns.

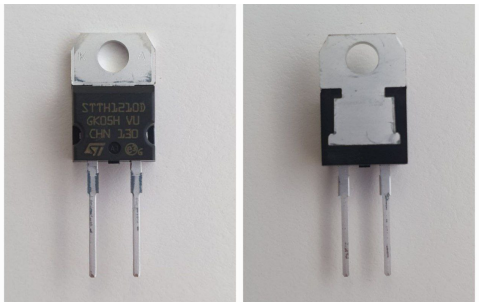

Figure 3.3.21: STTH1210D power diode [**33**].

3.3.6 Auxiliary winding electric equivalent model

The energy used to power the excitation system comes from the generator itself. It has already been said in Section 2.1 that in the main stator, in addition to the sets of windings building up the three phases, there is an additional conductor, called the auxiliary winding, on which terminals an alternating voltage is induced due to Faraday's law. This AC voltage is exploited by the excitation system to adjust the current flowing on the main rotor electromagnets, regulating the output voltage. Providing an accurate electric equivalent model of the auxiliary winding is fundamental. In fact, as it will be explained, the auxiliary winding owns some characteristics which led important issues in the realization of the circuit for the output stage of the voltage regulator.

So far, the auxiliary winding has been assumed to act like an ideal voltage source

which generates an alternating wave, called the auxiliary voltage. Independently of the actual waveform shape (that in Subsection 3.2.1 has been anticipated not to be a sinewave, but to be characterized also by a third harmonic content) the generator output impedance was considered zero. Actually, the auxiliary winding is a wire conductor wrapped in coils. For this reason, there are both resistive and inductive terms that it is necessary to consider when designing the regulator output stage circuit. These parasitic terms can be accounted placing a resistor and an inductor in series with the ideal voltage generator.

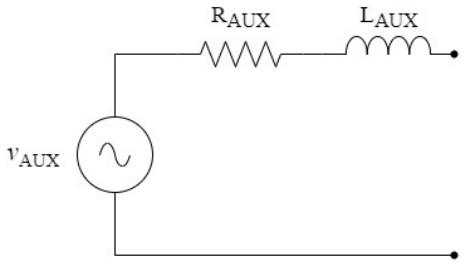

Figure 3.3.22: Electrical equivalent model of the auxiliary winding.

Values for such parasitic components, as it is possible to imagine, depend from machine to machine. However, it is meaningful to provide these values for one of the machines considered during the thesis activity, at least to give the reader some information about the order of magnitude of such parasitic terms.

As regards the resistive component, a typical value for the resistance R_{AUX} is 1Ω. This value is easily achievable using a tester connected to the winding terminals.

The inductive term, on the contrary, is more difficult to assess. This is because the inductive component playing a role in the circuit model of Fig. 3.3.22 is not the auxiliary winding inductance when the generator is at rest. On the contrary, in a similar way to what describes the operation of a transformer, it is possible to model the winding inductance with the circuit below.

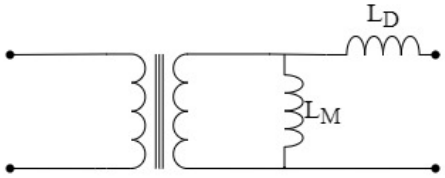

Figure 3.3.23: Magnetization and dispersion inductances in the auxiliary winding transformer-like model.

The output side of the winding is modeled with two inductors: L_M called magnetization inductance and L_D called dispersion inductance. The parasitic auxiliary inductance L_{AUX} coincides with the dispersion inductance L_D only. For this reason, L_{AUX} is not easily assessable measuring the inductance at rest. Instead, an expedient has been found that makes possible to obtain the desired L_{AUX} value with a good accuracy. It is done exploiting the resonating frequency of the RLC oscillating circuit shown below.

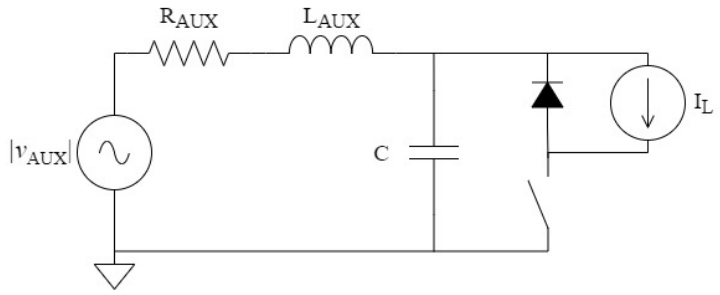

Figure 3.3.24: Circuit for auxiliary inductance L_{AUX} evaluation.

The reader can notice in the topology of this circuit a significant similarity to the inductive load drive circuit. The differences are on the generator side, where the electrical equivalent model for the auxiliary generator is used, and on the bypass capacitor placed in parallel with the output terminals of the non-ideal generator. $|v_{AUX}|$ is a notation that allows not to include the full bridge rectifier in the circuit and so to simplify the topology for easy understanding. It means the AC auxiliary voltage waveform in rectified so that it assumes only positive values.

The insertion of the capacitor allows to realize a resonant circuit: when the switch is on the voltage v_C is going to oscillate at the resonant frequency $f_0 = \frac{1}{2\pi\sqrt{L_{AUX}C}}$.

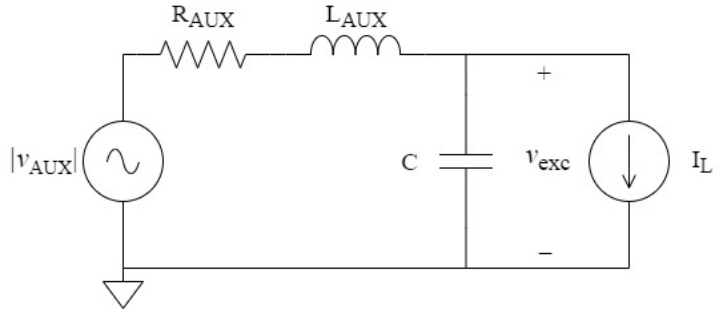

Figure 3.3.25: Equivalent circuit for auxiliary inductance L_{AUX} evaluation when the switch is on.

The circuit is realized using the components described so far: the GBU4J silicon

bridge rectifier, the STP13N80K5 power MOSFET and the STTH1210D power diode. The capacitor is a $330\,nF$ polypropylene film capacitor. Its value is chosen so that an oscillation is observable. The alternator used for this test is the model ECO38 1M4 C [**34**]. Channel 3 of the oscilloscope screenshot shows the voltage across the capacitor v_C.

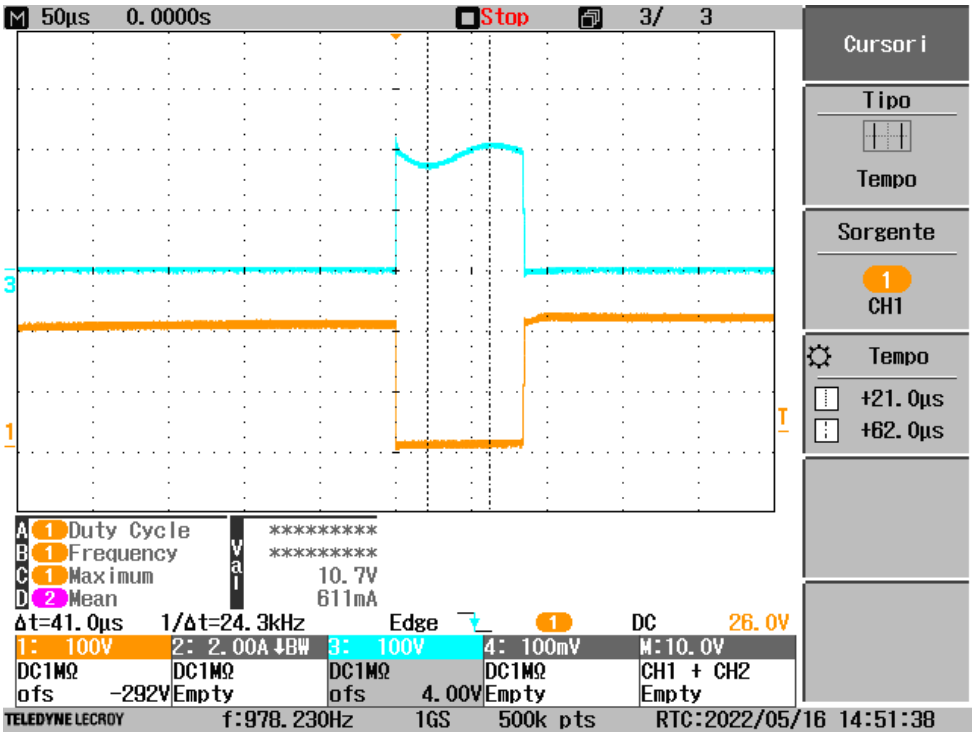

Figure 3.3.26: Oscilloscope screenshot: Ch. 1: v_{DS}; Ch. 3: v_C.

The horizontal time axe cursors show the frequency related to a half of an oscillation to be $24.3\,kHz$. This means $f_0 = 12.15\,kHz$ and eventually $L_{AUX} = \frac{1}{(2\pi f_0)^2 C} \simeq 0.5\,mH$

Auxiliary inductance problem In order to explain the problem associated to the parasitic inductive term of the auxiliary voltage generator, the circuit composed by the elements described so far is reported below. As already done, the ideal voltage generator is assumed to produce a rectified alternating voltage waveform $|v_{AUX}|$, so to avoid the inclusion in the representation of the diode bridge, not affecting the circuit operation.

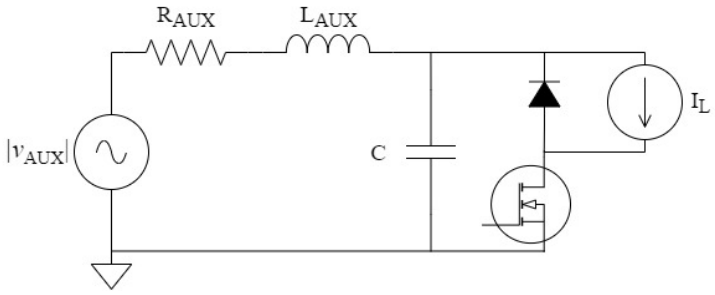

Figure 3.3.27: Circuit for inductive load driving.

The problem is due to the presence of a switching element, the MOSFET, in series with an inductive one, the auxiliary inductance. In a very similar way to the inductive load switch situation, described deeply in Section 2.1, the MOSFET forces the current through the auxiliary winding to change quickly. In fact, when the MOSFET is on (and the freewheeling diode is reverse biased) the current through the inductive load I_L is provided by the auxiliary voltage generator. In this time interval $i_{AUX} = i_S = I_L$. During the turn-off switching the transistor voltage begins to rise, but the currents in the various parts of the circuit remain the same until the diode begins to conduct. The inductive load current is forced to close in the diode loop. The current provided by the auxiliary generator, since equal to the MOSFET one, is zero. In this time interval $i_D = I_L$, while $i_S = i_{AUX} = 0\,A$. Thus, the current through the auxiliary inductance L_{AUX} is forced to decrease steeply with a rate dictated by the transistor properties and its gate drive circuit. The transistor voltage can be expressed as

$$v_{DS} = v_{AUX} - R_{AUX} i_{AUX} - L_{AUX} \frac{di_{AUX}}{dt} \tag{3.3.7}$$

The rate of fall of the current is in the order of $t_{fi} = 40\,ns$. Assuming to consider the $0.5\,mH$ auxiliary inductance value obtained earlier and the specifications $6.5\,A$ inductive load current, the voltage difference that would present at the auxiliary inductance terminals is in the order of $\Delta V_{Laux} = L_{AUX} \frac{I_L}{t_{fi}} = 81.250\,kV$. This huge voltage difference results in a positive voltage spike on the diode cathode and, since the diode is already conducting when the current of the MOSFET drops, the peak appear also on the drain terminal of the MOSFET. Such massive voltage peak would destroy immediately the transistor. An oscilloscope screenshot allows to appreciate the presence of very large voltage peaks in the drain-source voltage. The acquisition is obviously performed at a much lower current value ($\simeq 680\,mA$) in order to keep the voltage peaks below the voltage rating of the transistor.

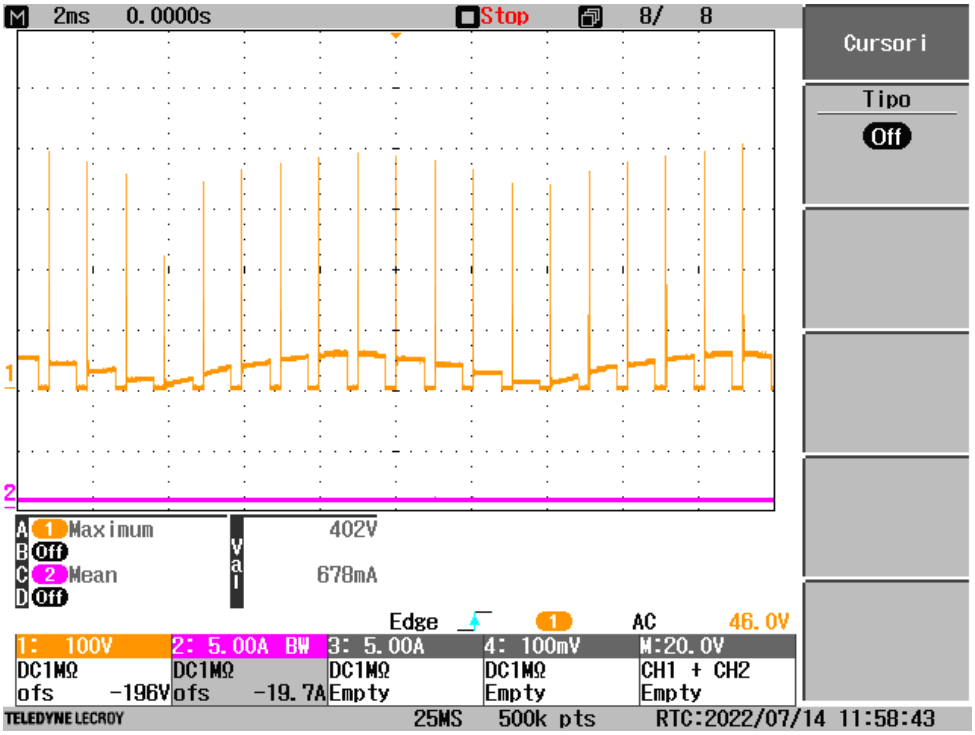

Figure 3.3.28: Oscilloscope screenshot: Ch.1: v_{DS}; Ch.2: i_L.

One could wonder how the currently used topology using the thyristor could work, since the same issue concerning the voltage peaks induced on the auxiliary inductance terminals occur as the power switch turns off. The answer is in the turn-off time of a thyristor, typically being in the order of tens of microseconds. With such times the voltage spike induced on the inductive element terminals is the order of tens of volts, much more manageable using some precautions, like a snubber.

Another observation that could arise is why another freewheeling diode cannot be used in parallel with the auxiliary inductance, similarly to what was done for the inductive load, which presented the same voltage spikes issue. The reader must notice the auxiliary inductance is not a passive component connected to the circuit, like the exciter stator on the contrary is. The auxiliary inductance L_{AUX} represents the dispersion inductance of the auxiliary winding, that is a parasitic term distributed all along the wiring constituting the coils. The representation of the auxiliary generator as the series of an ideal voltage generator, a resistance and an inductance, is just a model useful to describe the circuit operation. For this reason, the issue concerning the switch of an inductor current has to be treated and resolved in a different way.

3.3.7 Solution attempts

In this subsection the attempts to solve the issue related to the auxiliary inductance will be described. The reader has to consider these steps as a design process which, starting from the easiest solution, try to make the circuit working enabling the coexistence of the fast-switching commutation capability of the MOSFET and the auxiliary inductance. As it will be exposed, the proposed attempts provide a partial solution to the problem, in the sense that if on one side they manage the main inductive switch issue, on the other they cause other issues that make that attempt not applicable. This "search for a solution" process is considered interesting both to give the reader the idea of the electronic designer work flow and to justify the final circuit topology choice as the only solution found to solve the problem.

Overvoltage snubber The first idea is to absorb the voltage spikes induced on the auxiliary inductance terminals by means of a filtering circuit, called overvoltage snubber. The circuit here shown assumes, without loss of generality, a constant supply voltage V_d.

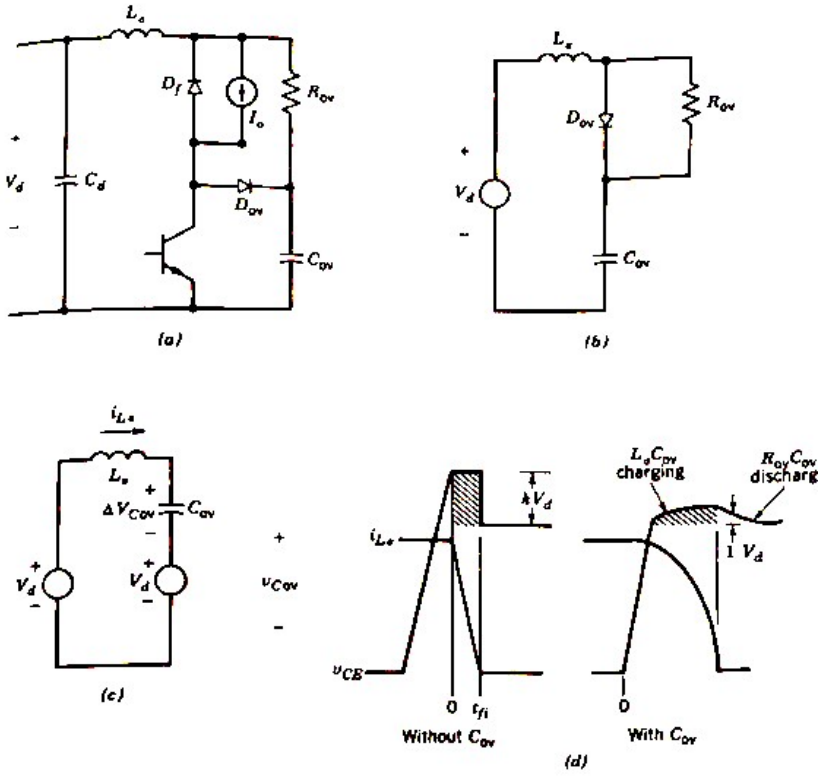

Figure 3.3.29: (a) Overvoltage snubber and (b,c) its equivalent circuit during transistor turn-off. (d) The drain-source voltage with and without snubber [**2**].

Initially the transistor is conducting and the voltage $v_{C,ov}$, across the overvoltage snubber capacitor, equals V_d. At turn-off, assuming the power MOSFET current fall time is small, the current through L_{AUX} is essentially I_L when the transistor current decreases to zero, and the output current then freewheels through the freewheeling diode. At this stage the equivalent circuit is as shown in Fig 3.3.29b where the diode, current generator combination appears as a short circuit and the transistor is an open circuit. Now the energy stored in the auxiliary inductance gets transferred to the overvoltage capacitor through the diode D_{OV} and the overvoltage ΔV_{DS} across the transistor (noting that in this state the capacitor C_{OV} and the transistor have the same voltage) can be obtained by replacing the pre-charged capacitor with its equivalent circuit as shown in Fig. 3.3.29c. Using energy considerations and noting that $\Delta V_{C,OV} = \Delta V_{CE}$, it results

$$\frac{C_{OV}\Delta V_{CE,max}^2}{2} = \frac{L_{AUX}I_L^2}{2} \tag{3.3.8}$$

Assuming to be able to withstand an overvoltage equal to one-tenth of the maximum value of the input alternating voltage provided by the auxiliary winding given in the project specifications $V_{peak} = 450\,V$, the needed overvoltage capacitance would result

$$C_{OV} = \frac{L_{AUX}I_L^2}{(0.1V_{peak})^2} = \frac{0.5\,mH \cdot (6.5\,A)^2}{(0.1 \cdot 450\,V)^2} \simeq 10\,\mu F \tag{3.3.9}$$

Once the current through L_{AUX} has decreased to zero, it can reverse its direction due to the diode D_{OV}, and the overvoltage on the capacitor decreases to V_d through the resistor R_{OV}. The capacitor discharge time constant $\tau_{OV} = R_{OV}C_{OV}$ should be small enough so that the capacitor voltage has decayed approximately to V_d prior to the next turn-off of the transistor. Assuming $4\tau_{OV}$, the full transient time of an RC exponential function, to be smaller than 1% of the switching period, the resistance would result

$$R_{OV} = \frac{0.01}{4C_{OV}f_S} = 0.256\,\Omega \tag{3.3.10}$$

The interesting fact is that the snubber resistor must dissipate an amount of energy independent on the resistance value. Such energy is the magnetic energy stored in the auxiliary inductance before the transistor turns off, that is $E_{Laux} = \frac{1}{2}L_{AUX}I_L^2$. Such energy gets transferred to the snubber capacitor and gets dissipated by the snubber resistor every switching cycle. Thus, the average power dissipated by the resistor is

$$P_d = \frac{1}{2}L_{AUX}I_L^2 f_S = \frac{1}{2} \cdot 0.5\,mH \cdot (6.5\,A)^2 \cdot 976\,Hz \simeq 10.3\,W \tag{3.3.11}$$

that is an incredibly high value to dissipate for a classical through-hole resistor. No device of such technology can dissipate this amount power. Other kinds of technologies should be used, but the cost increases a lot. For this reason, this solution is considered not viable.

The reader should know this incredibly high-power value is a consequence of the large value of auxiliary inductance. Typically, the overvoltage snubber is used to absorb overvoltage peaks caused by stray inductances distributed in the various connections of the circuit, accounting for an overall inductance typically in the order of the nH. In the thesis application case, the inductance is larger of four orders of magnitude, leading the impossibility to exploit this kind of solution.

Bus polypropylene film capacitor As the evidence that dissipating the energy stored in the auxiliary winding is not convenient, the next idea is instead to store temporarily that energy in a device, like a capacitor. At a later time, the energy is released and used to supply the inductive load. The proposed circuit topology is the following.

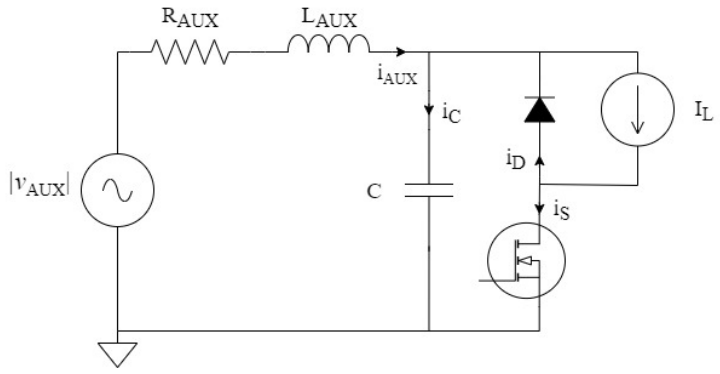

Figure 3.3.30: Circuit for inductive load driving with bus film capacitor.

At every transistor turn-off, the current flowing through the auxiliary inductor i_{AUX} is not forced any more to drop with the same rate as the drain current. Instead, the auxiliary current can continue to flow through the bus film capacitor. The result is that the voltage spike that would induce on the cathode node of the freewheeling diode (and on the MOSFET drain) is absorbed by the bus film capacitor, which charges up. During the off phase the capacitor keeps charged since no connection to the ground is provided by the off-state transistor. As the MOSFET turns-on the bus capacitor discharges releasing the current for the inductive load and gets ready for the next turn-off event.

The designer surely desires to use the cheapest and smallest components possible. In this perspective the use of low value film capacitors is a wished choice (typically

below 1 μF). However, this topology involves two main issues.

The first is the oscillatory behaviour produced by the resonance of the auxiliary inductance with the added capacitor during the on phase. It is exactly the situation shown in Subsection 3.3.6, whose circuit is used to measure L_{AUX}. If in that case the resonance is a desired phenomenon useful to measure a parameter in an indirect way, the same approach cannot be used as a solution to account for the auxiliary inductance issue. In fact, if the ringing doesn't compromise the pulsed waveform v_{EXC} at low auxiliary supply voltage and low load current levels (as observable in Fig. 3.3.31: $V_{AUX}^{rms} = 60\,V$, $I_L = 750\,mA$), the amplitude of the oscillation dramatically enhances and ruins the pulses applied to the inductive load as the voltage and current ratings approach the project specification ones (see Fig. 3.3.32: $V_{AUX}^{rms} = 230\,V$, $I_L = 1.6\,A$). The test is performed using a common use 330 nF polypropylene film capacitor.

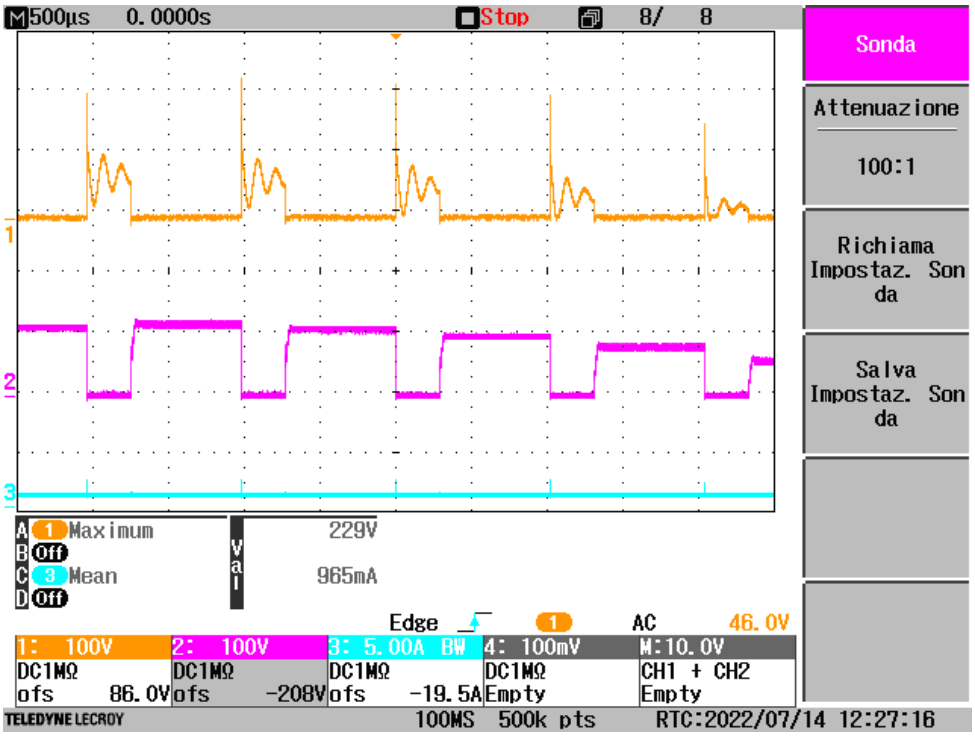

Figure 3.3.31: Oscilloscope screenshot: Ch. 1: v_{EXC}; Ch. 3: v_{DS}.

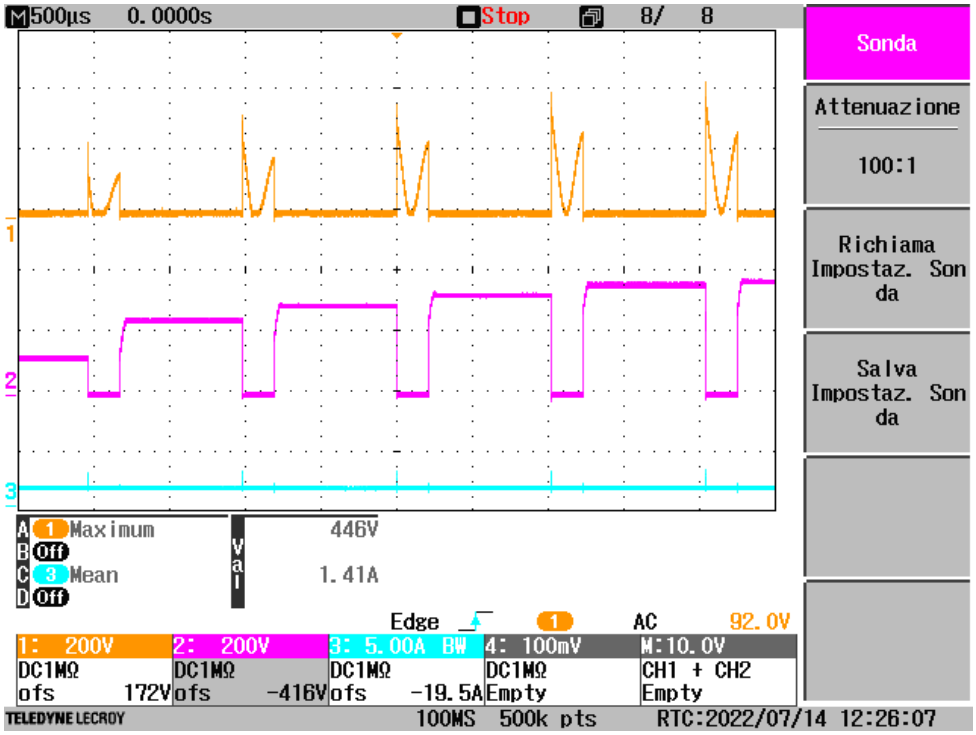

Figure 3.3.32: Oscilloscope screenshot: Ch. 1: v_{EXC}; Ch. 3: v_{DS}.

As it is possible to appreciate from the last image, the oscillation amplitude is so large to partially zero the voltage pulses applied to the inductive load. At higher current levels the ringing amplitude is so large to zero the pulse for most of the time.

The second issue related to the use of a low capacitance bus polypropylene film capacitor is the voltage level the capacitor charges up to. At turn-off the energy stored in the auxiliary inductor gets transferred to the capacitor. In the same way of the overvoltage snubber case, described in the previous paragraph, the voltage v_{Cf} across the capacitor raises by

$$\Delta V_{Cf} = \sqrt{\frac{L_{AUX}}{Cf}} I_{AUX} \tag{3.3.12}$$

Larger the capacitance, smaller the voltage increase. It is possible to notice this behaviour in the last two figures: v_{DS} (acquired in channel 1) at turn-off raises and reaches voltage levels higher than the auxiliary waveform sinusoidal peaks ($V_{AUX} = \sqrt{2}V_{AUX}^{rms}$, respectively 88 V and 325 V). In order to appreciate better such phenomenon an LTspice simulation of the circuit is run. It is assumed a sinusoidal auxiliary voltage having the project specification nominal RMS value of the auxiliary voltage in steady condition $V_{aux}^{rms} = 230\,V$ and the nominal inductive current value $I_L = 6.5\,A$. The capacitance value is again $330\,nF$. The auxiliary current i_{AUX}, the auxiliary voltage v_{AUX}

and the drain-source voltage v_{DS} trajectories are shown at a turn-off event, correspondent to an auxiliary voltage sinewave peak.

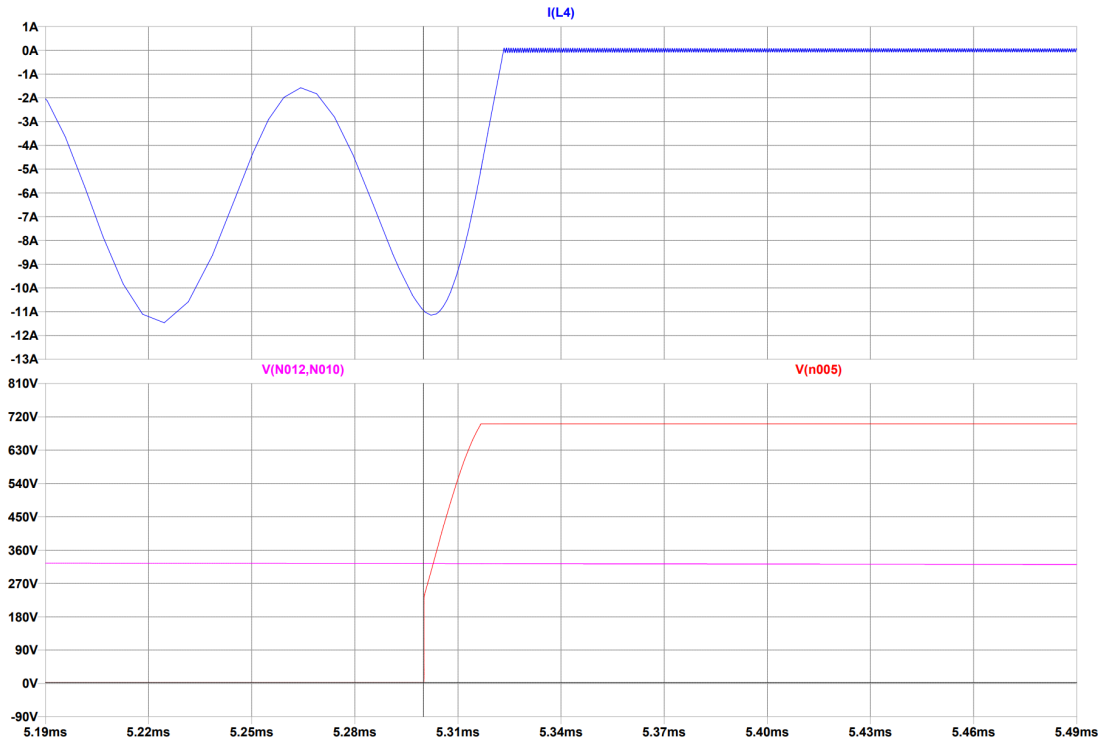

Figure 3.3.33: LTspice simulation: I(L4) inverse of auxiliary current -i_{AUX}, V(N012,N010) auxiliary voltage v_{AUX}, V(n005) drain-source voltage v_{DS}.

After the turn-off event, shown by the horizontal cursor, the drain-source voltage keeps rising because the bus capacitor is charged by the oscillating auxiliary current. It is possible to see the voltage level increases up to the maximum tolerable breakdown voltage of the STP13N80K5 MOSFET model used in the simulation.

Even if the polypropylene film capacitor is capable to remove the peaks on the switch terminals, the two reasons just exposed make this solution not applicable for the thesis application.

Bus polypropylene film capacitor with in series and in parallel resistors The intuition for the following solution attempt comes from the issues led by the last proposed circuit topology. It tries to solve the two problems regarding the ringing of the inductive load voltage v_{EXC} and the raise of the drain-source voltage v_{DS} at turn-off. The circuit topology describing this solution attempt is the following.

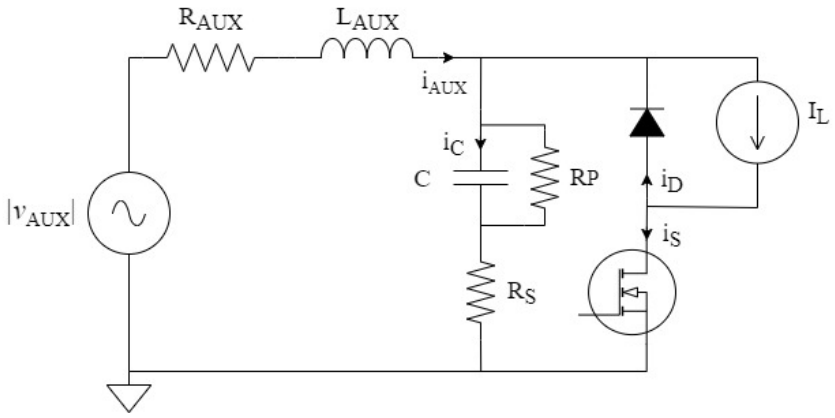

Figure 3.3.34: Circuit for inductive load driving with a resistor in series with bus film capacitor.

As regards the voltage ringing, a solution could be the one to place a resistor R_s in series with the bus capacitor. During the on phase, the RLC ringing circuit now presents the larger resistance $R_{AUX} + R_s$. Recalling the damping factor for an RLC circuit is $\gamma = R/2L$, an appropriate resistance value could be able to cancel the oscillation.

As regards the raise of the drain-source voltage during the off phase a way to solve the problem can be placing a resistor in parallel to the bus capacitor in order to dissipate the energy stored in the capacitor itself at turn-off. In this way, after the charging up of the capacitor, the voltage across it is allowed to drop because of the local R_pC_f loop. In this way, since the freewheeling diode is approximately a short circuit, also the drain-source voltage is allowed to drop.

Unfortunately, even if these two resistors are able to solve the issues for which they are included in the circuit, they add other problems. In fact, the series resistor R_s makes voltage spikes appear again at turn-off events: the auxiliary inductance current, forced to flow through the branch of the capacitor, induces on the resistor terminals a voltage drop $v_{Rs} = R_s \cdot i_{AUX}$ proportional to the resistance value. In a cascade effect also the voltage at the cathode of the freewheeling diode and the drain-source voltage undergoes the same voltage spike. If from this point of view a small resistor would be preferable, on the other a small resistor is less able to damp the oscillation. On the other side, the parallel resistor R_p, in order to reduce the voltage across the bus capacitor, has to dissipate the energy stored in it. This energy is, as a first approximation, the one transferred by the auxiliary inductance to the bus capacitor. The situation is comparable to the one of the overvoltage snubber, already discussed. The parallel resistor, independently on its value, must dissipate a power equal to $\frac{1}{2}L_{AUX}I_L^2 f_S$. Keeping the

same parameters used so far this power accounts for 10.3 W, being a too high value to dissipate for a resistor. Series and parallel connections of multiple resistors have also been considered. However, the high cost and the large space occupied by multiple high-power resistors, led to the rejection of this solution.

Small capacitance bus aluminum electrolytic capacitor The last paragraphs discussed possible solutions exploiting a low value film capacitor. As already mentioned, the use of such kind of capacitor is convenient in terms of cost, high voltage rating capability and limited space occupied on the PCB. However, voltages and currents involved in the circuit led the impossibility to use low value capacitors. The main problem is the drain-source voltage level reached during off phase. The energy transfer from the auxiliary inductance to the bus capacitor causes a voltage raise that must be monitored in order not to go beyond the value given in the project specifications, being 450 V. It is possible to see from Eq. 3.3.12 the voltage raise is proportional to the inverse of the square root of the capacitance. A larger capacitance undergoes a lower increase in its voltage for the same stored energy. It is comprehensible there will be a capacitance value so that the raise in voltage does not cause to exceed the maximum tolerable voltage. The evaluation of such capacitance value is not trivial. In fact, other than the capacitance itself, the raise in voltage depends on the auxiliary current waveform, which in turn depends on the capacitance value too. In order to understand this phenomenon, extreme cases can be addressed: no capacitor or infinite capacitance. In the former case the auxiliary current assumes a rectangular pulse train shape: during on phase $i_S = i_{AUX} = I_L$, during off phase $i_S = i_{AUX} = 0\,A$. In the latter case the auxiliary winding has never to provide any current; it is all supplied by the infinite capacitance: during on phase $i_S = i_C = I_L$, during off phase $i_S = i_C = 0\,A$. All the intermediate cases between these two extremes, using finite value capacitances, feature combinations of i_{AUX} and i_C such that during the on phase

$$i_S = i_{AUX} + i_C = I_L \tag{3.3.13}$$

and during off phase

$$i_S = i_{AUX} + i_C = 0 \tag{3.3.14}$$

The basic concept is that during on phase the capacitor provides current until it can. As it is discharged, the auxiliary winding is involved and supplies all the remaining current to satisfy the upper equations. In addition, at the next turn-off the auxiliary generator charges again the capacitor, which will release its energy at the next turn-on.

Remember the auxiliary inductance transferring energy to the capacitor is the reason for which voltage spikes are eliminated. As it has just been described the complexity and multi-dependence of the variables involved make the analytic approach extremely difficult. For this reason, an appropriate value for the capacitance is obtained by means of a simulation-based approach. The LTspice simulation of the circuit with the bus capacitor is run. As already done for previous cases, it is assumed a sinusoidal auxiliary voltage having the project specification nominal RMS value of the auxiliary voltage in steady condition $V_{aux}^{rms} = 230\,V$ and the nominal inductive current value $I_L = 6.5\,A$. The simulation shows a $470\,nF$ capacitor can satisfy the voltage limit requirement, as appreciable in the following figure.

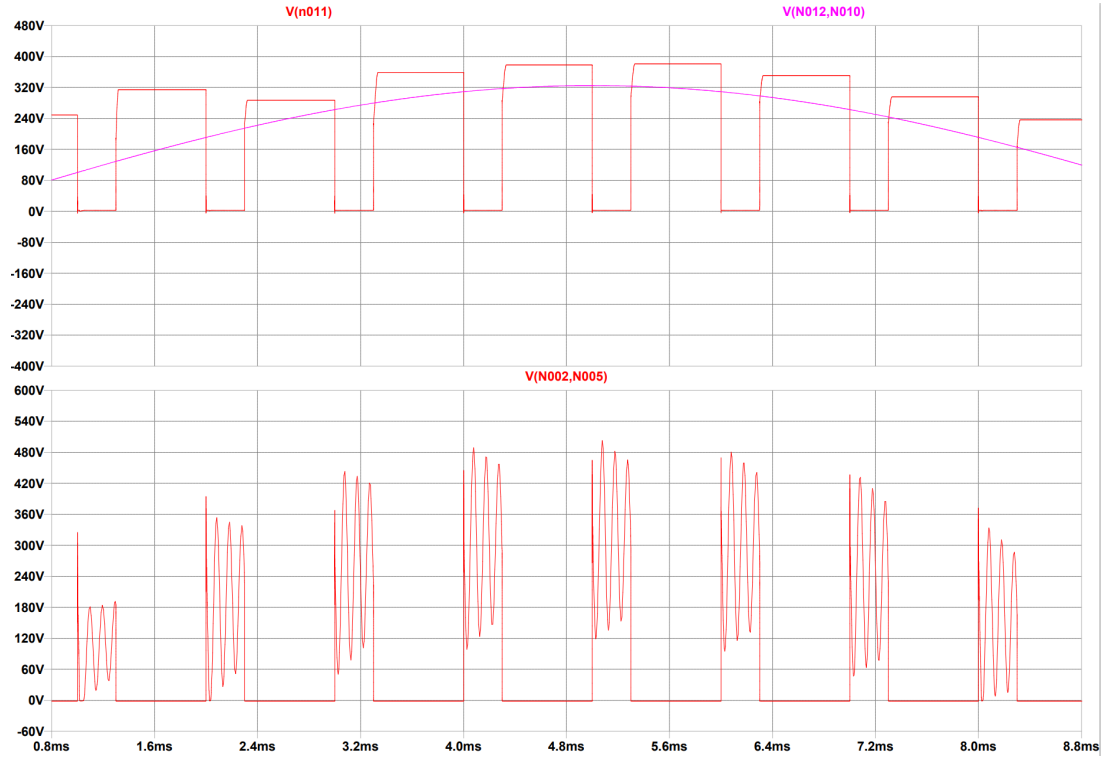

Figure 3.3.35: LTspice simulation: V(n011) drain-source voltage v_{DS}, V(N012,N010) auxiliary voltage, V(N012,N010) exciter stator voltage v_{EXC}.

It must be mentioned the simulation is run setting the PWM duty cycle to 0.3, because it is a common use case situation, as it will be shown later on.

However, one should notice that for such capacitance value the ringing of exciter voltage v_{EXC} is yet too high in frequency. This means that, like in Fig. 3.3.32, the voltage oscillations could zero v_{EXC}, something unwanted. At the same time of the voltage requirement, one should guarantee the ringing frequency to be large enough not to ruin the voltage pulses applied to the inductive load. A larger capacitance must be used. A

simulation using a 10 uF capacitor shows the combination of the two requirements is satisfied.

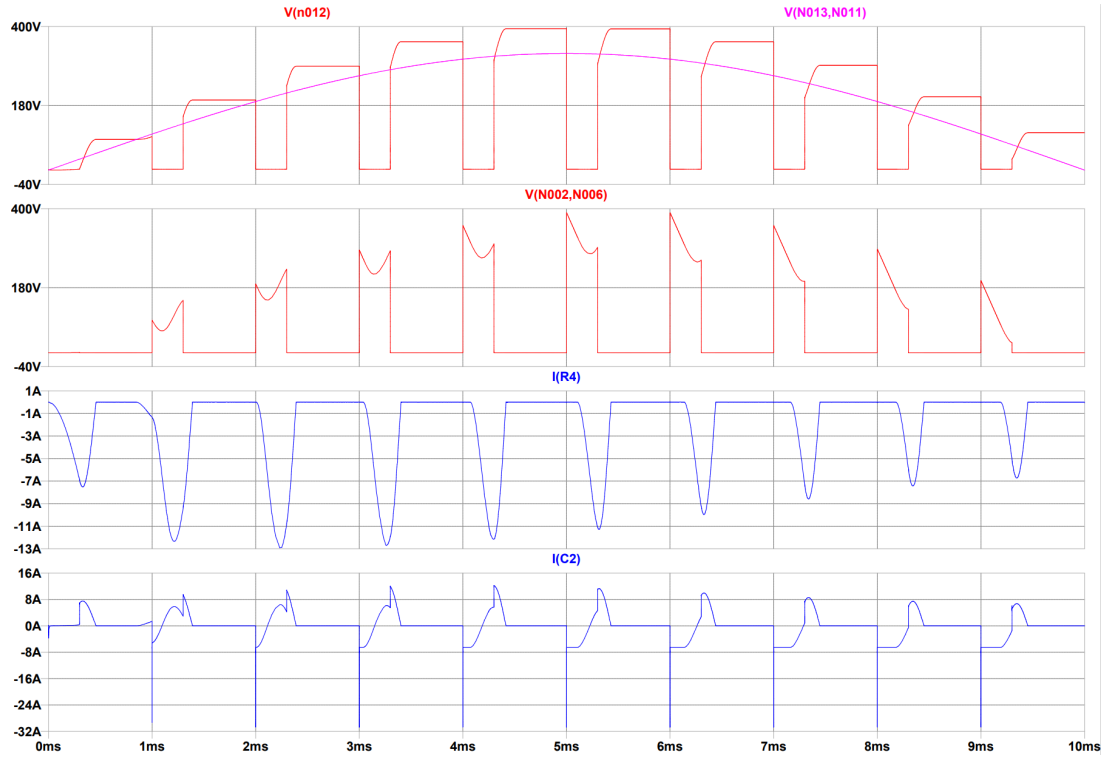

Figure 3.3.36: LTspice simulation: V(n012) drain-source voltage v_{DS}, V(N013,N011) auxiliary voltage, V(N002,N006) exciter stator voltage v_{EXC}, I(R4) inverse of auxiliary current -i_{AUX}, I(C2) inverse of bus capacitor current -i_C.

Now the oscillations of v_{EXC} are slower, whose period is comparable to the switch on-time. By means of the simulation the reader can also appreciate the waveforms assumed by the auxiliary and capacitor currents: at each turn-on the capacitor provides current until it is able to. The difference between the load current I_L and the capacitor current i_C comes from the auxiliary winding. At turn-off the auxiliary current can drop with a rate smaller than the one of the switch because it continues flowing through the capacitor, which is charged again. In order to provide a complete discussion, the spikes one can see on the capacitor current at turn-on are due to the freewheeling diode reverse recovery.

Even if there are polypropylene film capacitors, available on the market, having capacitances of 10 μF, their high cost and large size make the design choice to direct towards other kinds of technologies. Specifically, the capacitor technology capable of providing both large capacitance values and high voltage ratings is the aluminum electrolytic capacitor. Therefore, using a 10 μF, 450 V aluminum electrolytic capacitor

would seem an appropriate choice.

However, also this solution is not feasible. The reason is to be found in the fact that practical capacitors are not ideal components with only capacitance. On the contrary they can be treated, to a very good degree of approximation, as being a series of capacitance, inductance and resistance.

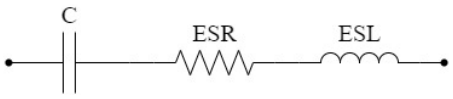

Figure 3.3.37: AC equivalent circuit of an aluminum capacitor.

The equivalent series resistance (ESR) is due to the presence of resistance of the electrolyte and paper separator and other contact resistances. Any pulsating voltage across a capacitor result in an alternating current through the capacitor. Because of the presence of ESR, this alternating current produces an increase of temperature in the capacitor cell. The heat generation depends on frequency and waveform of the alternating current. The maximum RMS value of this alternating current, which is permitted to pass through the capacitor during its entire specified useful life is called *rated ripple current* I_R. The rated ripple current is specified in the relevant detail specifications typically at 100 or 120 Hz. The temperature rise is thus the result of the heat generated by electrical losses $P = I_R^2 \cdot ESR$. Excessive ripple current will increase heat production within the capacitor, causing the capacitor to be damaged because of shorten life, open pressure relief vent and short circuit.

From the most famous electronic components manufacturers catalogues it is possible to read that 10 μF 450 V aluminum electrolytic capacitors can't sustain ripple currents beyond 200 mA. Unfortunately, this value is an order of magnitude smaller compared to the RMS current that is going to flow through a $10\mu F$ capacitor in this thesis application.

As it is possible to appreciate from Fig. 3.3.36 the analytical computation of the RMS value for such current waveform is very difficult. For this reason, the value provided by the simulation software is used. Such value results to be $I_{R,10\mu F} \simeq 3.7\,A$. In this situation, a $10\mu F$ electrolytic capacitor would heat up and fail in a short time.

3.3.8 Solution for auxiliary inductance problem

After showing that a $10\mu F$ $450\,V$ aluminum electrolytic capacitor would be able to satisfy all the requirements in order to make the circuit working properly, the further information about the limit in the ripple current leads to the discard of this option too.

To sustain higher ripple currents a larger capacitance is required. This happens because in aluminum electrolytic capacitors the capacitance is inversely proportional to the ESR. The reader should remember the capacitor current waveform depends on the capacitance value. Consequently, also the capacitor RMS current will be dependent on the capacitance value.

In order to find an appropriate value for the capacitance so that the capacitor is able to sustain the ripple current it is going to flow through it, the following approach is considered. Firstly, a series of LTspice simulations provide the capacitor RMS currents obtained in the range of capacitances $[10\mu F, 1000\mu F]$. This result is compared to the ripple currents values provided by manufacturer catalogues for the same range of capacitances. The combination of these two pieces of information will provide the value for a sufficiently large capacitance able to sustain the ripple current is going to flow through.

Among all the possible electronic components stores, information about on market components is searched on the online webstore *RS Components* **[26]** **[27]** **[28]**. The choice is due to the fact that the company Mecc Alte has RS Components among its main components suppliers. Moreover, looking for a desired technical specification in a components store, differently from a single manufacturer catalogue, allows to take into consideration, if not all, many manufacturers. For each capacitance value in the considered range a filter-based research allows to obtain the highest ripple current sustainable. Before proceeding in the capacitance estimation another information must be derived. In fact, as previously mentioned, the ripple current a capacitor is able to sustain depends on the capacitor alternating current frequency. As it is possible to evince from the plot of Fig. 3.3.36 the capacitor current waveform is far from assuming a single spectral line. For this reason, the LTspice simulation software is used to look also at the FFT of the capacitor currents waveforms for the whole capacitance range. The current waveform FFT for the $10\mu F$ and $1000\mu F$ cases is shown below.

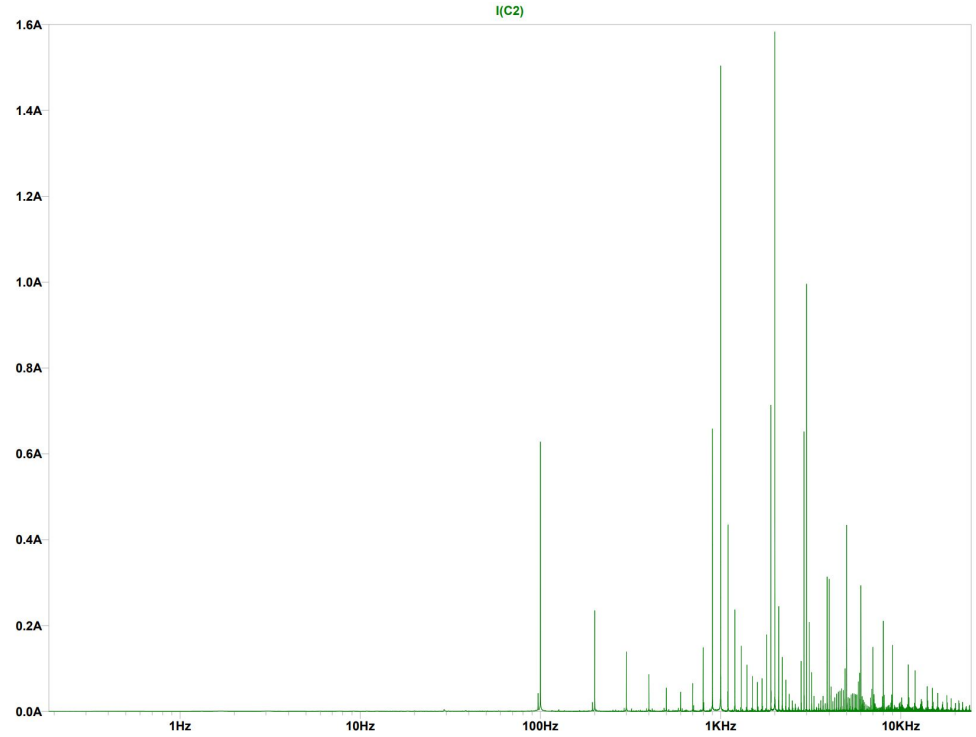

Figure 3.3.38: LTspice simulation: FFT of $10\mu F$ capacitor current.

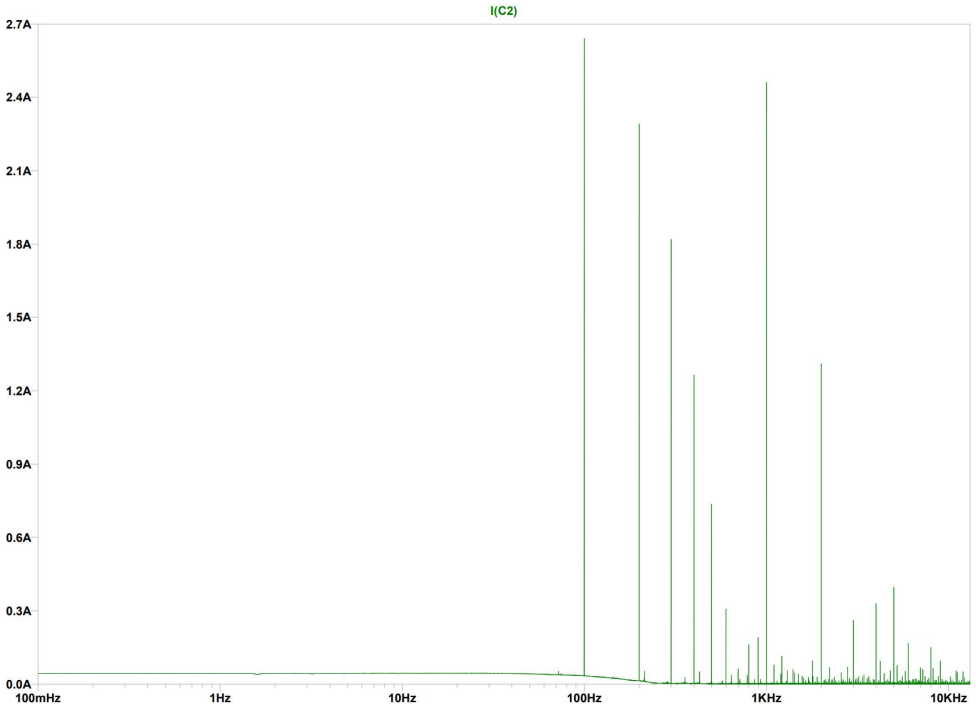

Figure 3.3.39: LTspice simulation: FFT of $1000\mu F$ capacitor current.

The simulations show for both cases a peak-distributed spectrum. However, for both the cases, it is possible to assume the main harmonic content to be in the range $[100, 10000]\ Hz$. This information is useful because ripple current information in datasheets is obtained by the given value at a certain frequency and a table, like the following, showing the multiplier by which the given value has to be multiplied to obtain the actual data.

W. V. (V. DC)	Cap. (μF)	Frequency (Hz)					
		60 ≦	120 ≦	300 ≦	1 k ≦	10 k ≦	100 k ≦
160 to 450	10 to 82	0.25	0.35	0.50	0.65	0.90	1.00
	100 to 330	0.30	0.40	0.55	0.70	0.90	1.00

Figure 3.3.40: Frequency correction factor for ripple current **[28]**.

At this point, it is possible to cross the information coming from the simulations and the catalogues to produce a plot that relates the ripple current with capacitance.

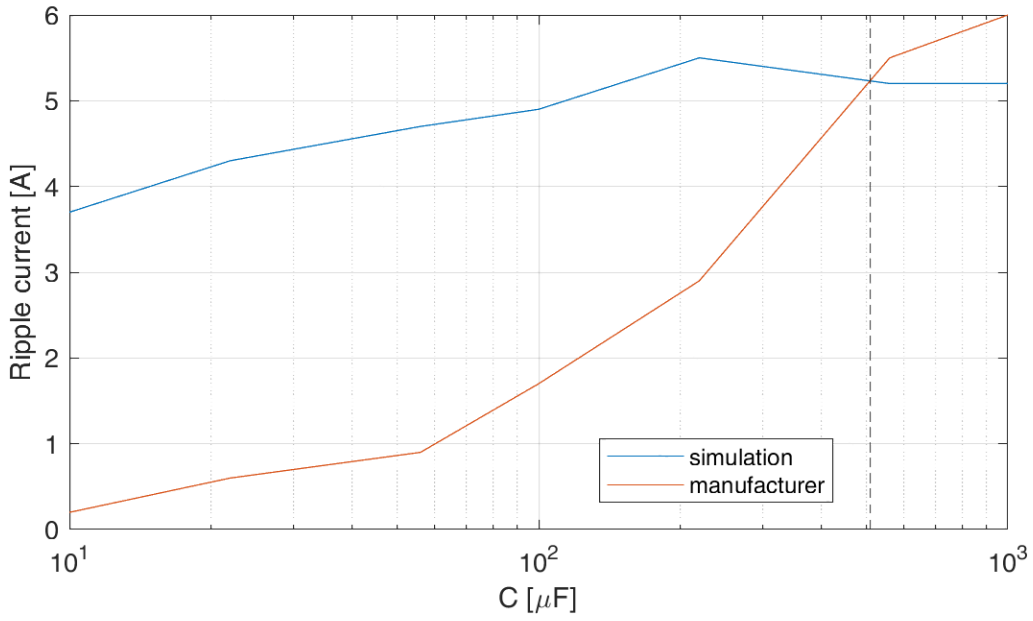

Figure 3.3.41: Ripple current vs capacitance relation from simulation and catalogue information.

From the upper chart it is possible to appreciate the trends of the ripple current in function of the capacitance. The most obvious trend is the one obtained from the manufacturers data: as it has already been mentioned, the larger the capacitance is, the more current the device is able to sustain. The less intuitive trend is the one showing

the actual RMS current flowing through the capacitor in function of the capacitance, computed by means of simulations. Even in this case the RMS current increases with the capacitance. The interesting fact is that there is a capacitance value $C_0 = 508\mu F$ for which the two characteristics coincide. For that value over the capacitors have technical specifications making them able to sustain the ripple current that would flow through them. This discussion leads to the final choice for the capacitor. Since it should have a capacitance larger than C_0, a $560\mu F$ aluminum electrolytic capacitor is selected.

Figure 3.3.42: Jackcon LHK Series $560\mu F$, $450\,V$, $105°C$ aluminum electrolytic capacitor [**29**].

A good design practice is to place in parallel to the electrolytic capacitor an additional low capacitance low ESR capacitor. This is done in order to improve the non-ideal impedance of a real capacitor at high frequencies. Ideally a capacitor should reduce its impedance as the frequency increases due to its $1/sC$ impedance transfer function. However, as described earlier, the ESR and ESL in series parasitic components make the capacitor impedance modulus to reach an absolute minimum and then increase beyond that frequency, according to

$$Z_{C,real} = \frac{1}{sC} + R + sL = \frac{1 + sRC + s^2LC}{sC} \tag{3.3.15}$$

Placing an additional in parallel low capacitance helps keeping the impedance low for a wider range of frequencies. This is a desired behaviour because it allows the equivalent capacitor to provide higher frequency currents, like sharp edges, as required by the thesis application. For this reason, a $100\,nF$ polypropylene film capacitor is placed in parallel to the $560\mu F$ aluminum electrolytic capacitor.

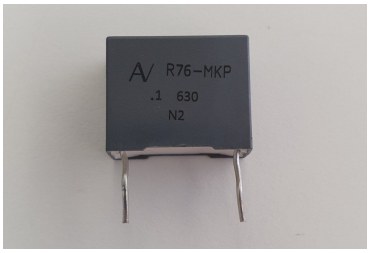

Figure 3.3.43: KEMET 100 nF, 630 V polypropylene film capacitor **[30]**.

An important point should be clarified. The previous Subsection 3.3.7 develops a "trial and error" discussion about how in this thesis the issue of this application (the current switch of the auxiliary inductance) is faced and managed. The theoretical explanations, the additional problems created by the solution attempts and the choices to avoid them are all described and justified. The whole process ends up to the conclusion that the best solution is to involve the use of a large aluminum electrolytic capacitor. This, in contrast with the electronic designer desire to minimize the space and cost, means the use of a large and quite expensive component (compared to all the other components present in the circuit). However, the point wanted to emphasize is that the auxiliary inductance is source of a problem that is no possible to eliminate, since inherently present in the circuit supply (the auxiliary winding). Unfortunately, this inductance has a value large enough to make the dissipation of the energy stored in it not desirable. Other than for the cost of the dissipating elements, it is not desirable also to avoid adding an extra source of heat generation in a PCB, a reason that could create reliability problems as time goes by. For these reasons, storing the auxiliary inductance energy is seen as a better solution: even if it represents an expensive solution too, it allows to provide a "cleaner" solution, in the sense that the basic working principle is simple and it does not involve heating degrading elements.

After having clarified this point another explanation has to be done. As the reader surely knows, the effect of connecting a large value capacitance to the output terminals of a diode bridge, which is fed by an alternating voltage waveform, is the realization of the simplest form of an AC/DC rectifier, known as *Graetz rectifier*. In this circuit the goal is to convert an alternating voltage into a continuous voltage. As it is possible to see from the following oscilloscope capture, the 560μF capacitance is large enough to rectify the input auxiliary AC voltage. The reader has to understand that in selecting the capacitance size there is not the willingness to create a Graetz rectifier. The output stage circuit of the voltage regulator could work perfectly even without the rectification of the input voltage. However, the already described reasons concerning the

capacitor ESR and ripple current limitation have the consequence to use a capacitor able to perform a good rectification.

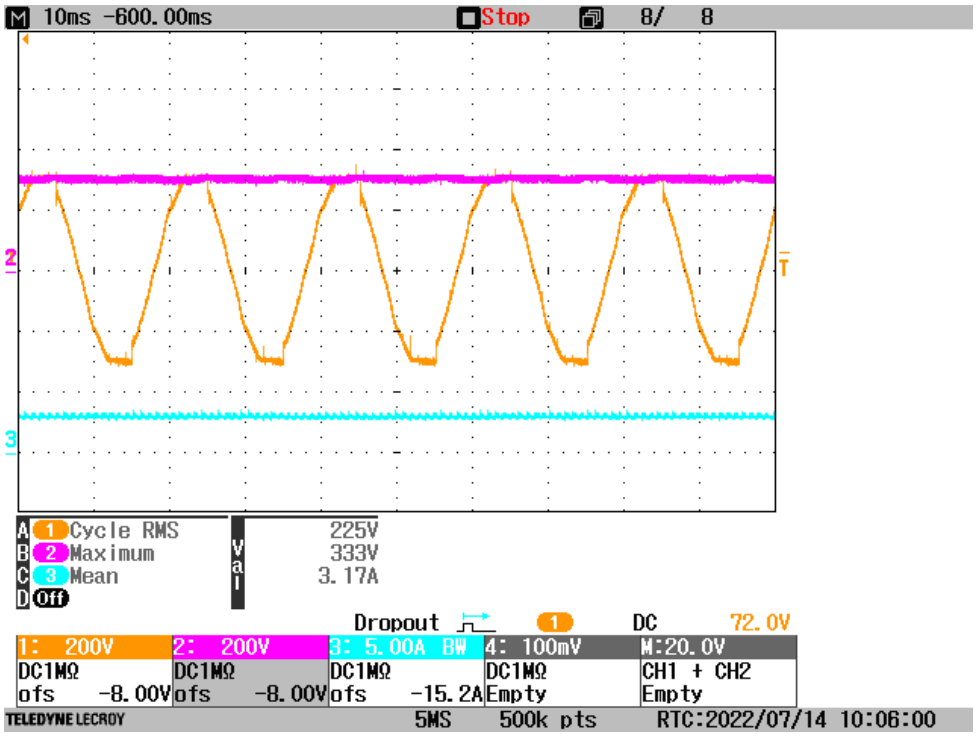

Figure 3.3.44: Oscilloscope capture. Ch1: v_{AUX}; Ch2: v_C; Ch3: i_L

3.3.9 Turn-off snubber

At this point, of the discussion about the development of the MOSFET-based output stage of the voltage regulator, the main problem faced during the design process has been addressed and resolved. If from the theoretical point of view, as described in the last subsection, the proposed circuit including the electrolytic capacitor is able to account for the auxiliary inductance current switching issue, at the time a first prototype is assembled and tested, another relevant issue came up. This problem, as it is going to be explained, is related to the practical implementation of the circuit by means of real components and connections, which adds non-idealities in the circuit operation that are not accounted in the first theoretical project analysis.

Even if the practical setup used to test the circuit prototype is going to be described in detail in a next section, the inclusion of the discussion about the turn-off snubber in this section dealing with the circuit development is considered the most appropriate choice. However, the reader should not be confused by this since the only elements useful for this discussion are the non-idealities led by the wires connecting the circuit

components and the behaviour of a real MOSFET.

After this introduction, it is here reported the acquisition of the MOSFET drain-source voltage in the prototype realization of the circuit developed so far.

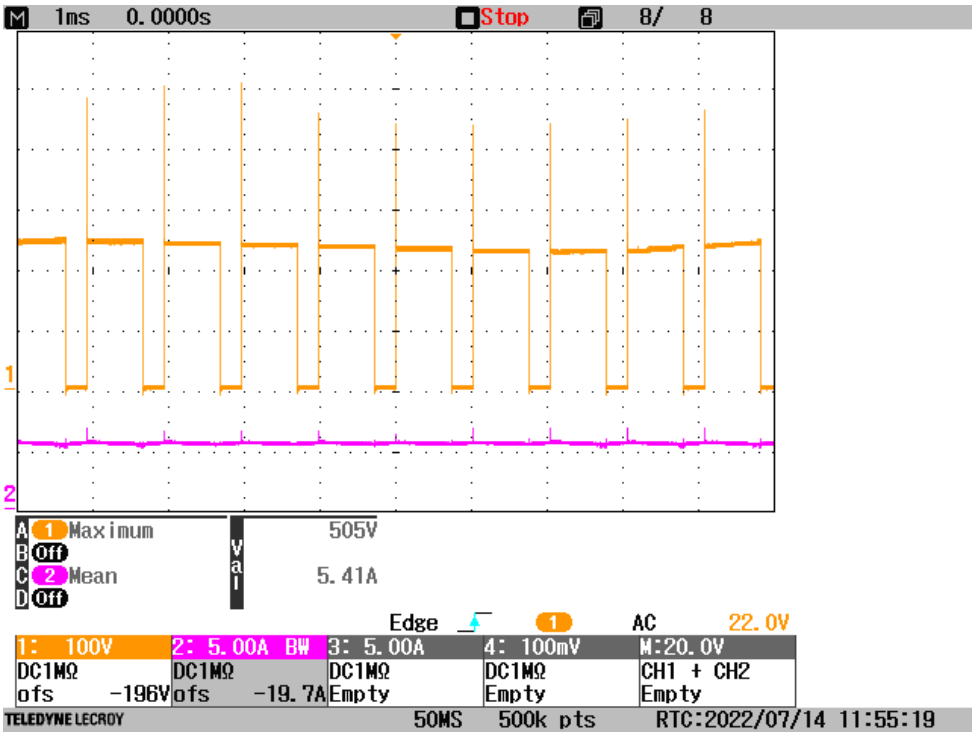

Figure 3.3.45: Oscilloscope capture. Ch.1: vDS; Ch.2: i_L.

Yet, the reader can notice the presence of relevant spikes at transistor turn-off events. These peaks are not the ones induced by current switching in the auxiliary winding. In fact, as it is possible to appreciate from the rectification of the voltage, a large capacitance is used. Moreover, notice the peaks extension is much smaller than the one that would be generated by the auxiliary inductance current switch. Instead, these peaks are due to stray inductance distributed along all the wiring connection between the components.

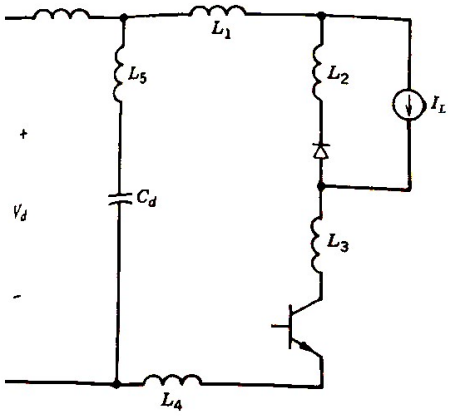

Figure 3.3.46: Simplified switch inductive load circuit with stray inductances shown explicitly [**2**].

Because of high switching performance of the MOSFET, relevant voltage surges are applied to the transistor. The drain-source voltage can be expressed as

$$v_{DS} = V_d - L_\sigma \frac{di_S}{dt} \tag{3.3.16}$$

where $L_\sigma = L_1 + L_2 + \ldots$. During the turn-off switching, the presence of stray inductances results in overvoltages since di_S/dt is negative.

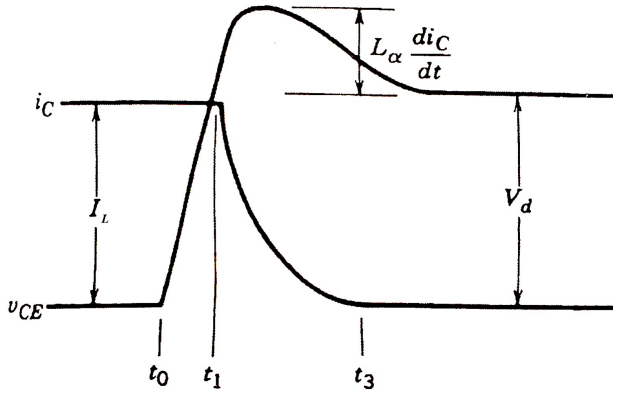

Figure 3.3.47: Turn-off switching trajectory with no snubber [**2**].

Voltage surges are critical in the discussion because the designer must ensure the i_S-v_{DS} operating points during device working do not exceed the safety conditions delimited by the MOSFET *Safe Operating Area* (SOA). This diagram, provided by the device manufacturer in the datasheet, gives an indication about the maximum time

intervals the component is able to sustain contemporarily high voltage and current during switching activity. Otherwise, the power dissipated by the transistor would raise the junction temperature above the sustainable limit and the device would fail.

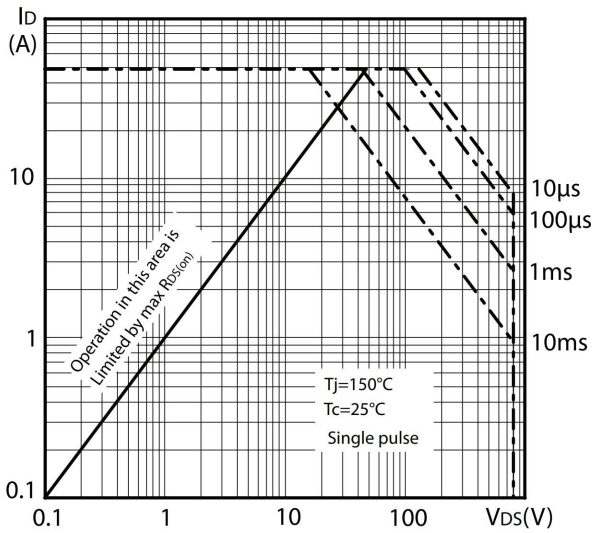

Figure 3.3.48: Safe operating area for STP13N80K5 power MOSFET [**32**].

The effect of stray inductances is to modify the switching i_S-v_{DS} trajectory. From the ideal one described in the previous Section 3.3.1, appreciable in Fig. 3.3.5, the stray inductances cause the ideal squared trajectory to be exceeded.

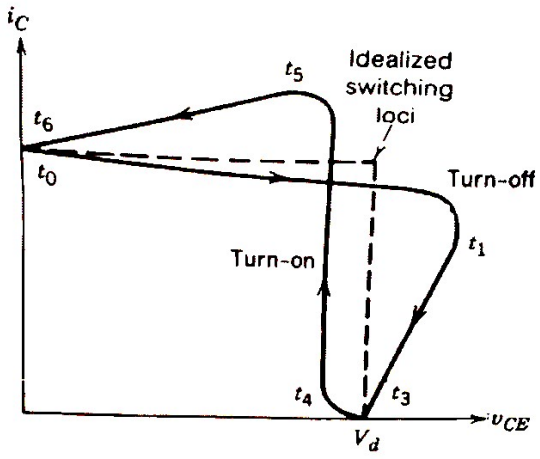

Figure 3.3.49: Switching trajectory [**2**].

The dotted lines represent idealized switching loci both for turn-on and turn-off, assuming zero stray inductances and no reverse-recovery current through the diode.

Even in this ideal case the transistor experiences high stresses at turn-on and turn-off when both its voltage and current are high simultaneously, thus causing a high instantaneous power dissipation. Moreover, the stray inductances result in overvoltage beyond V_d and the current diode reverse-recovery current causes overcurrent beyond I_L, which promote the device to exceed the SOA.

Because of the relevant voltage spikes on v_{DS} at turn-off, including a turn-off snubber in the circuit is considered a good precautionary measure. In the snubber discussion it is assumed that the transistor current changes linearly in time with a constant di/dt, which in only dictated by the transistor and its base drive circuit. Therefore, di/dt is assumed not to be affected by the addition of the snubber circuit.

To reduce the problems at turn-off, the goal of a turn-off snubber is to provide a zero voltage across the transistor while the current turns off. This can be approached by connecting a RCD network across the MOSFET as shown in the following figure.

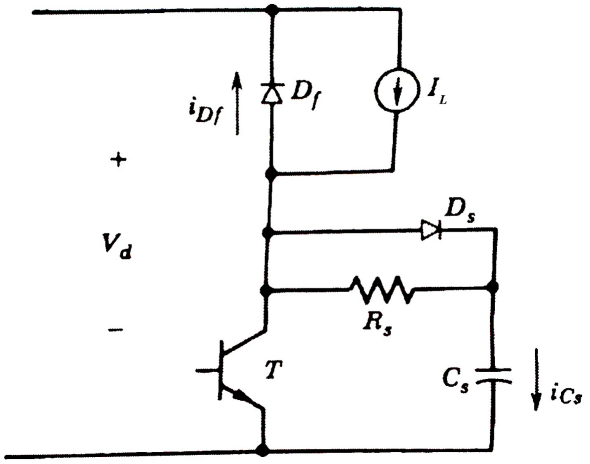

Figure 3.3.50: Turn-off snubber circuit [**2**].

Prior to turn-off, the transistor currents is I_L and the transistor voltage is essentially zero. At turn-off in the presence of the snubber, the transistor current i_S decreases with a constant di/dt and $(I_L - i_S)$ flows into the capacitor through the snubber diode D_s. Therefore, for a current fall time of t_{fi}, the capacitor current can be written as

$$i_{Cs} = I_L \frac{t}{t_{fi}} \qquad 0 < t < t_{fi} \tag{3.3.17}$$

where i_{Cs} is zero prior to turn-off at t = 0. The capacitor voltage, which is the same as

the voltage across the transistor when D_s is conducting, can be written as

$$v_{Cs} = v_{DS} = \frac{1}{C_s}\int_0^t i_{Cs}\,dt = \frac{I_L t^2}{2C_s t_{fi}} \tag{3.3.18}$$

which is valid during the current fall time so long as the capacitor voltage is less than or equal to V_d. The equivalent circuit that represents this condition is the following.

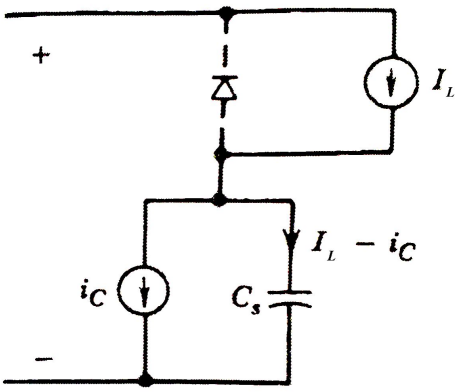

Figure 3.3.51: Turn-off snubber equivalent circuit during turn-off transient [**2**].

Depending on the value of capacitance, the capacitor voltage reaches V_d before or after the current fall time is over. The capacitance C_{s1} that causes the capacitor voltage to reach V_d exactly at the current fall time t_{fi} can be calculated by substituting $t = t_{fi}$ and $v_{Cs} = V_d$ in Eq. 3.3.18. For this computation the datasheet typical turn-off time $t_{fi} = 42ns$, the specification maximum voltage $V_d = V_{peak} = 450\,V$ and nominal current $I_L = 6.5\,A$ are considered:

$$C_{s1} = \frac{I_L t_{fi}}{2V_d} = \frac{6.5\,A \cdot 42\,ns}{2 \cdot 450\,V} \simeq 0.3\,nF \tag{3.3.19}$$

For a capacitance larger than C_{s1}, the waveforms in Fig. 3.3.52 show that the transistor voltage rises slowly and takes longer than t_{fi} to reach V_d. Beyond t_{fi}, the capacitor current equals I_L and the capacitor and the transistor voltages rise linearly to V_d.

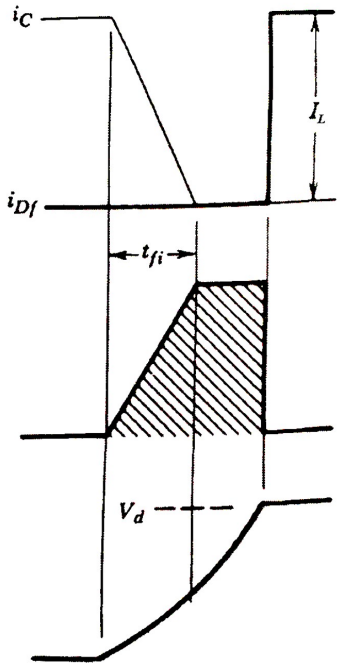

Figure 3.3.52: Current and voltage waveforms during the turn-off transient [**2**].

Keeping in mind the desire to reduce the stresses at turn-off and help the turn switching locus to stay within the SOA, a capacitance larger than C_{s1} is chosen. The turn-off switching locus with $C_s > C_{s1}$ shown below make the reader appreciate the effect on the turn-off trajectory.

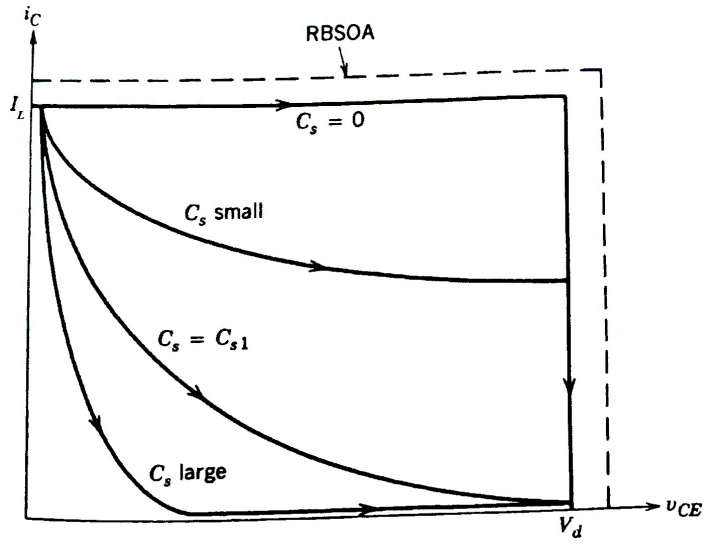

Figure 3.3.53: Switching trajectory during turn-off with snubber capacitance larger than C_{s1} [**2**].

A welcome side effect of reducing turn-off stresses is the reduction in the turn-off switching losses: separating the fall of current from the rise of voltage deletes the i_S-v_{DS} overlap and so the power dissipated.

Moreover, the larger the capacitance is, the more energy of the surge voltage the capacitor is able to absorb; eventually, the smaller the spike will be.

However, the selection of an arbitrary large capacitance is not a good design choice. The reason for this is to be found in the transistor turn-on transition. During the turn-on commutation the MOSFET current begins to rise at a rate dictated by the transistor properties and the base drive circuit. Eq. 3.3.18 is still valid, but due to a positive di_C/dt the transistor voltage v_{DS} is slightly less than V_d. The presence of C_s causes the turn-on current to increase beyond I_L and the reverse recovery current of the free-wheeling diode. After the freewheeling diode recovers at t_x the drain-source voltage decreases to approximately zero at a rate dictated by the devices properties (almost instantaneously).

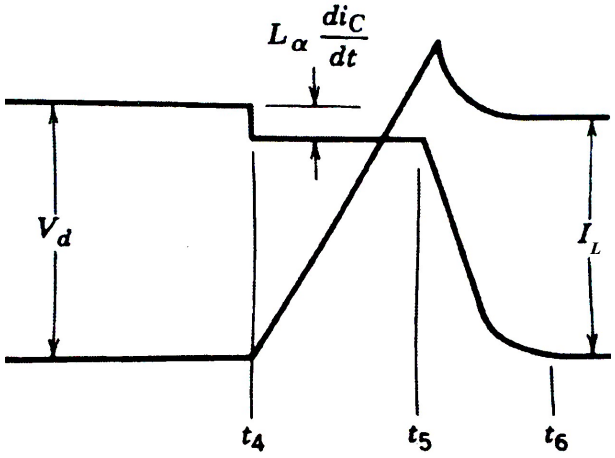

Figure 3.3.54: Turn-on switching trajectory with no snubber [**2**].

The designer must ensure the capacitor has sufficient time to discharge down to a low voltage during the minimum on-state time of the transistor in order that the turn-off snubber is effective at the next turn-off event. The loop constituted by snubber capacitor, snubber resistance and on-state switch realize a discharging RC circuit. During the on-state of the power switch, the capacitor discharges with a time constant $\tau_c = R_s C_s$ and

$$v_{Cs} = V_d\, e^{-t/\tau_c} \tag{3.3.20}$$

Therefore, the use a of large snubber capacitor is to avoid in order not to have a minimum duty cycle too large for the application. For this reason, a $C_s = 2.2\,nF$ single layer

ceramic capacitor is selected for this task. Its $2\,kV$ voltage rating makes it appropriate for the voltages involved in this application.

Figure 3.3.55: $2.2\,nF$, $2\,kV$ single layer ceramic capacitor for turn-off snubber.

The snubber resistor has the goal to dissipate the energy stored into the capacitor at turn-off, that is $W_R = C_s V_d^2/2$. Considering the project specifications maximum auxiliary voltage $V_{peak} = 450V$ as V_d, at the switching frequency of 976 Hz this involves dissipating a power of

$$P_R = W_R \cdot f_S = \frac{C_s V_d^2}{2} f_S = \frac{2.2\,nF \cdot (450\,V)^2}{2} \cdot 976\,Hz \simeq 0.217\,W \tag{3.3.21}$$

Notice that the dissipating power does not depend on the value of the resistance, but instead on the chosen capacitance one. This is another reason not to select an excessively large capacitance. The snubber resistance is selected keeping into account two phenomena. The first is the peak current stressing the transistor at turn-on: the RC discharging circuit involves an initial peak current $I_{s0} = V_d/R_s$ that adds to the sum of the nominal current I_L with the freewheeling diode reverse-recovery current I_{RR}. This current could cause the transistor to exceed the SOA. For this reason, it is preferable a large value for the snubber resistance. On the other hand, a small snubber resistance is desirable since R_s represents the other factor determining, with the snubber capacitance, the capacitor voltage discharge time. In order to provide a reasoning on which to base the snubber resistance selection, it is necessary to show which is the minimum duty cycle that has to be applied for this application. This is provided by a test of the circuit on a Mecc Alte generator. The following capture shows the steady-state drain source voltage in a no-load situation for the ECO38 model. The no-load represents the less stressed situation possible, where the output voltage is obtained with the lowest excitation current possible.

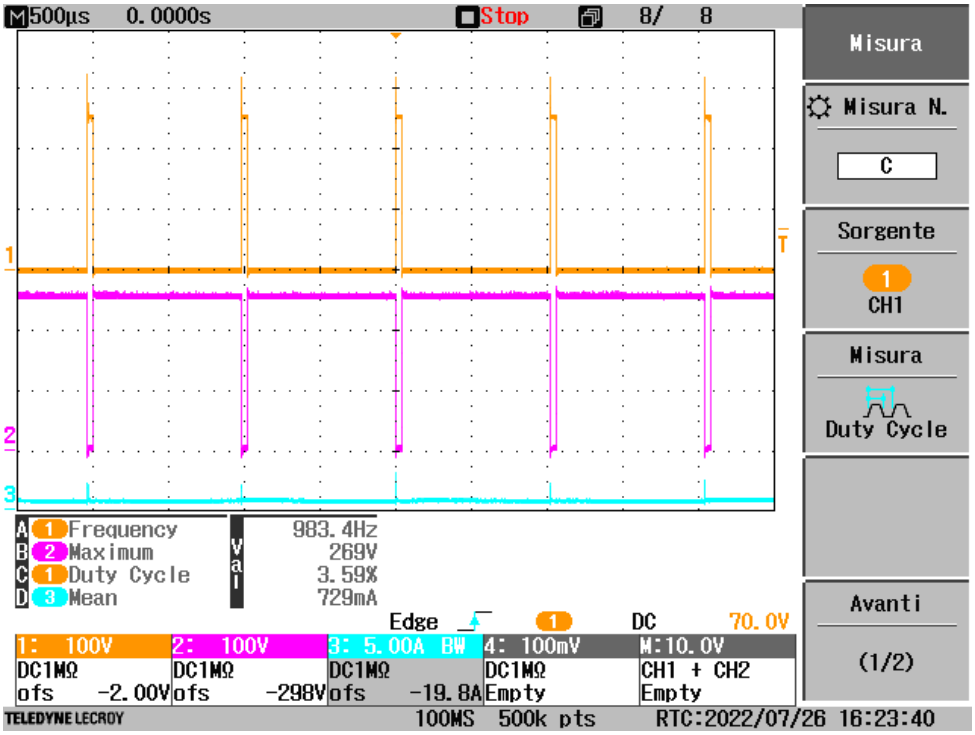

Figure 3.3.56: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

From the oscilloscope automatic measurement of the duty cycle of exciter voltage v_{EXC}, it is possible to say the minimum PWM duty cycle needed is $d_{min} = 3.6\%$. At this point, the computation can proceed. Considering the snubber capacitor voltage exponential discharge time to be $4\tau_c$, the following condition is obtained:

$$R_s < \frac{d_{min}}{4C_s f_S} = \frac{0.036}{4 \cdot 2.2\,nF \cdot 976\,Hz} \simeq 4.2\,k\Omega \tag{3.3.22}$$

From the combination of the two requirements above discussed the value of the snubber resistance is finally set to $1\,k\Omega$. This value allows to add to the turn-on current a low peak (compared to the continuous $12\,A$ MOSFET current rating) of amplitude

$$I_{s0} = \frac{V_d}{R_s} = 0.45\,A \tag{3.3.23}$$

and contemporary to limit the snubber to be effective from a PWM duty cycle larger than

$$d_{min} = 4R_s C_c f_S \simeq 0.86\% \tag{3.3.24}$$

which allows to keep a margin from the previously assessed value.

In order to be able to select the snubber resistor a last parameter has to be consid-

ered: the maximum sustainable voltage. No voltage is applied on the resistor terminals during the most of its operation time. Only during the turn-on transitions it has to sustain a voltage peak equal to V_d, which extinguish in the order of μs. For this reason, a common use $0.25\,W$, $250\,V$ maximum working condition voltage, $500\,V$ maximum overload voltage though-hole resistor is good for this application.

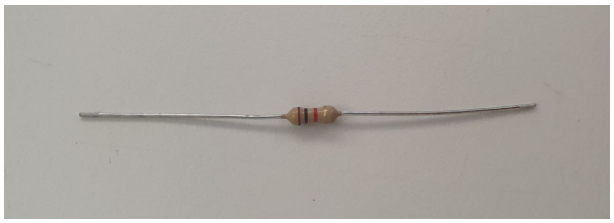

Figure 3.3.57: $1\,k\Omega$, $0.25\,W$ through hole snubber resistor.

Finally, regarding the snubber diode, the UF4007 ultrafast diode is used. It is a $1\,kV$ peak reverse voltage, $1\,A$ average forward current, $30\,A$ peak forward surge current rectifier.

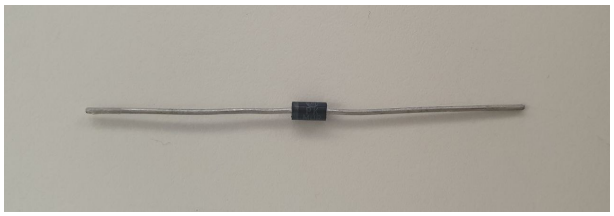

Figure 3.3.58: UF4007 diode.

Figure 3.3.59 shows the acquired turn-off transition. It is possible to appreciate the reduction in the turn-off voltage spikes on v_{DS}. The $2.2\,nF$ does not completely remove the voltage spikes. However, even in the worst-case condition illustrated in the figure, the voltage peaks are kept far below the voltage rating specifications.

The reader could argue the turn-off voltage surges issue is typically solved using an overvoltage snubber, like the one described in Subsection 3.3.7, instead of the turn-off snubber. In fact, theoretically speaking, the overvoltage snubber purpose is to absorb voltage spikes caused by stray inductances in the circuit, while the turn-off snubber one is to reduce the transistor stresses during turn-off transitions, making the current fall before the voltage rises. For these reasons, in many applications both snubbers are often simultaneously applied to the power switch. However, at the time the voltage surges issue is faced and practical measurements are performed, the evidence is that a turn-off snubber results to be effective enough in reducing the spikes. There is

a tradeoff between performance and cost: from one side the overvoltage snubber is more effective in erasing the spikes; on the other that snubber requires a two order of magnitude larger capacitance. Therefore, in the circuit design there is all the interest in promoting the turn-off snubber because the less expensive solution. Since, from measurements, the turn-off snubber turned out to be sufficient for the thesis application, it is not considered appropriate the use of an overvoltage snubber.

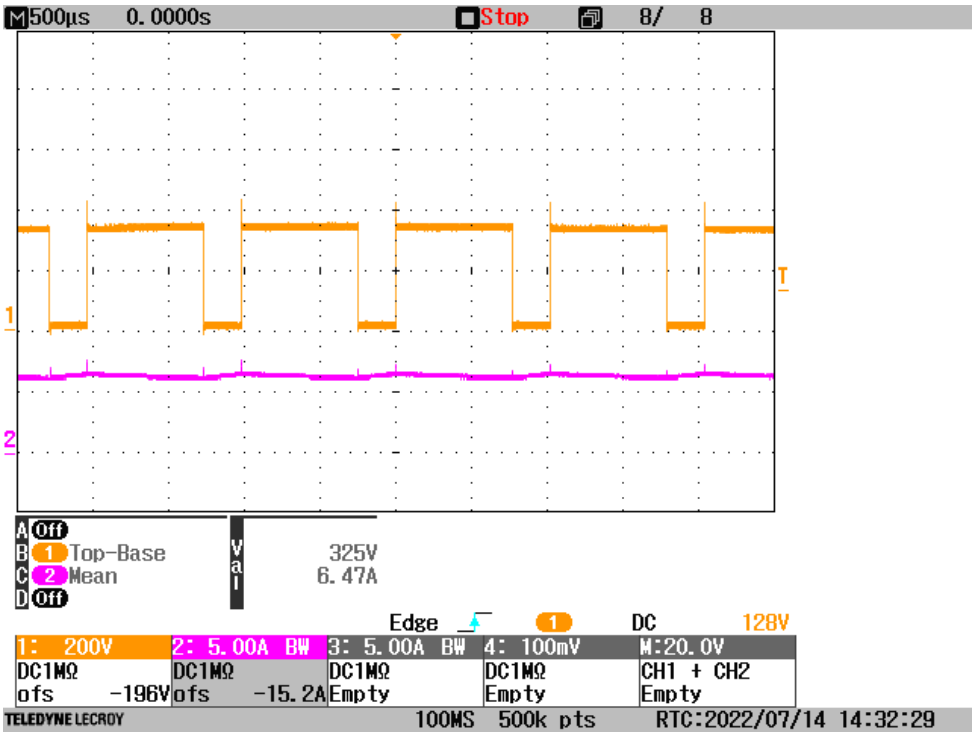

Figure 3.3.59: Oscilloscope screenshot: Ch.1: v_{DS}; Ch.2: i_L.

3.4 Final circuit topology

Once discussed all the single choices made in order to satisfy the application project requirements, this section is intended to present the complete circuit topology proposed to implement the output stage of the voltage regulator based on both turn-on and turn-off controllable power switch.

The circuit is here shown. Notice the auxiliary winding power supply and the exciter stator are substituted with their electric equivalent models.

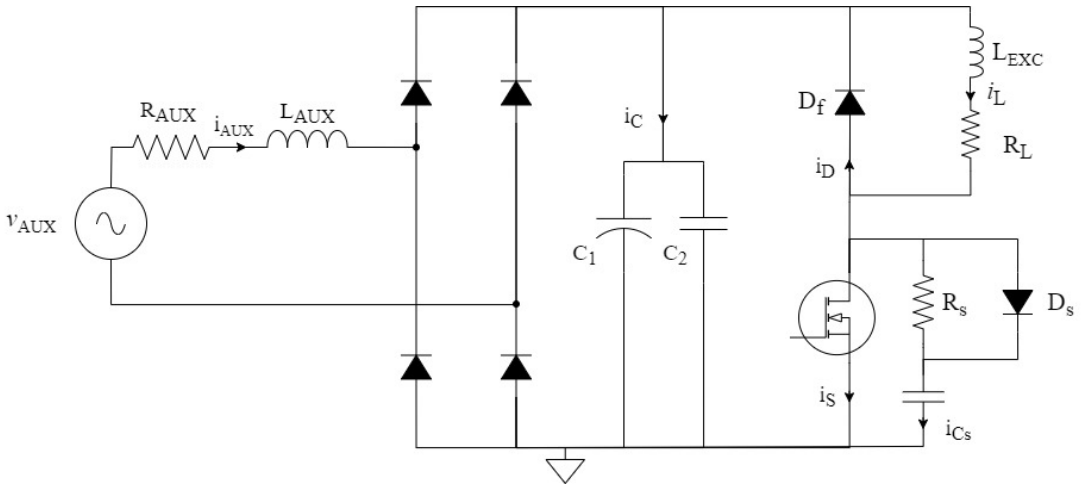

Figure 3.4.1: Complete circuit topology for the output stage of the voltage regulator.

Below it is shown a picture of the whole circuit prototype: the MOSFET soldered on the gate driving board, the other components assembled and soldered on the matrix board, the control boards.

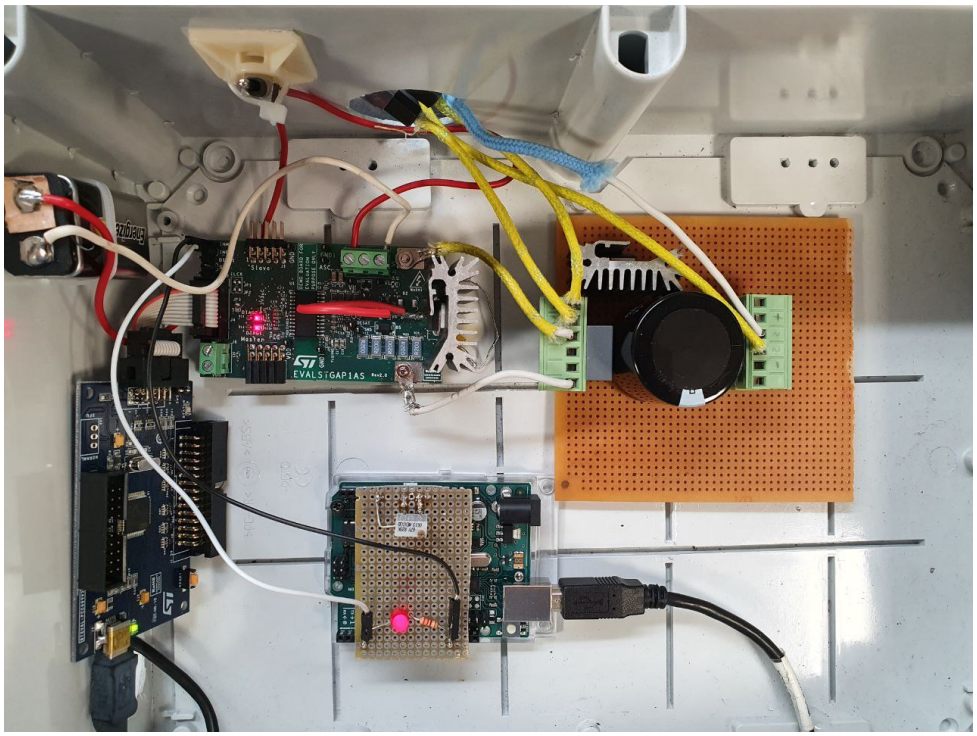

Figure 3.4.2: Circuit prototype for the output stage of the voltage regulator.

3.5 Circuit simulation

An important tool used to develop and obtain the final circuit is the software simulation. In this case the choice fell on LTspice, the famous SPICE-based analog electronic circuit simulator computer software. The particular reason why it is chosen is the possibility to include third-party models, in order to provide a simulation as much similar as possible to the reality. Indeed, specific models for the GBU4J silicon bridge rectifier, STP13N80K5 power MOSFET and STTH1210D power diode are imported into the model. Simulations, as the reader has surely noticed, is continuously exploited within the thesis development, in order to observe particular behaviours and issues which help in the description of the various situations and problems. For example, it is used to try to experiment the possible solutions in Subsection 3.3.7, allowing to analyze (and in case discard) ideas quickly and without effort.

Here below it is shown the LTspice model used to simulate the final circuit exposed in the previous section. The circuit follows what is illustrated in Fig. 3.4.1.

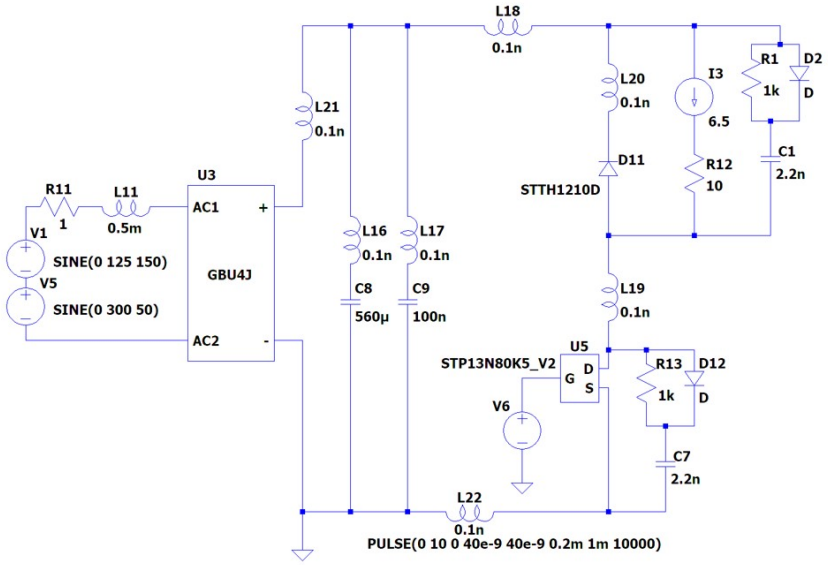

Figure 3.5.1: LTspice circuit model.

According to the specific shape of the auxiliary waveform, a series of two voltage generators is used to reproduce the desired auxiliary voltage. The two sinewave amplitudes are chosen in order to obtain the nominal RMS level

$$V_{AUX}^{rms} = \sqrt{\frac{V_1^2}{2} + \frac{V_3^2}{2}} = \sqrt{\frac{(300\,V)^2}{2} + \frac{(125\,V)^2}{2}} \simeq 230\,V \tag{3.5.1}$$

In order to make the simulation as similar as possible to the real case, distributed stray inductances are added in the model to simulate real wiring connections between the components. Exact evaluation of such inductances is impossible until a definitive realization of the circuit is not pursed. For this reason, it is chosen $0.1\,nH$ for all the connection, being a credible, if not pejorative, case. As regards the inductive load, a constant current generator is substituted to the inductance value of the exciter stator, like legitimately done in many previous simplified circuit representations. In the simulation this substitution is convenient in order to speed up the simulation. Finally, the MOSFET gate command signal is provided by a voltage pulse generator, emulating the PWM signal, whose raising and falling times are set to $40\,ns$, in accordance with the MOSFET datasheet switching times.

The main voltages and currents in the circuit are shown in the two following images.

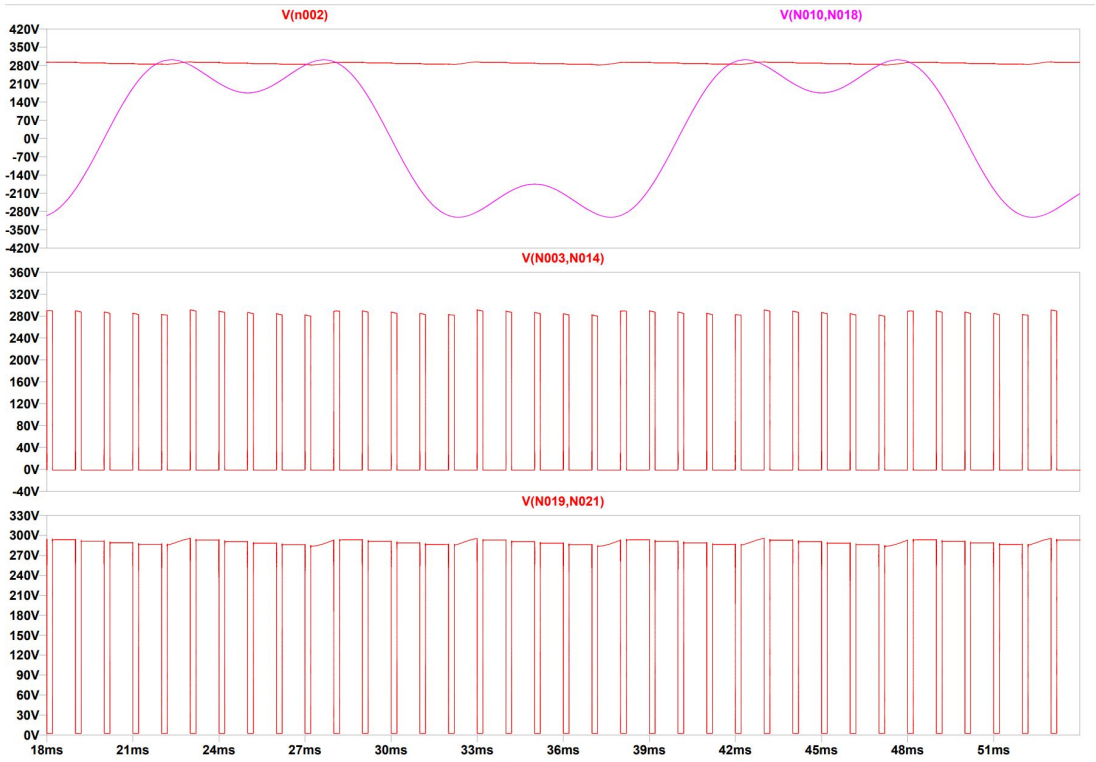

Figure 3.5.2: LTspice simulation: V(N010,N018) auxiliary voltage v_{AUX}, V(n002) bus capacitor voltage v_C, V(N003,N014) exciter stator voltage v_{EXC}, V(N019,N021) MOSFET drain-source voltage v_{DS}.

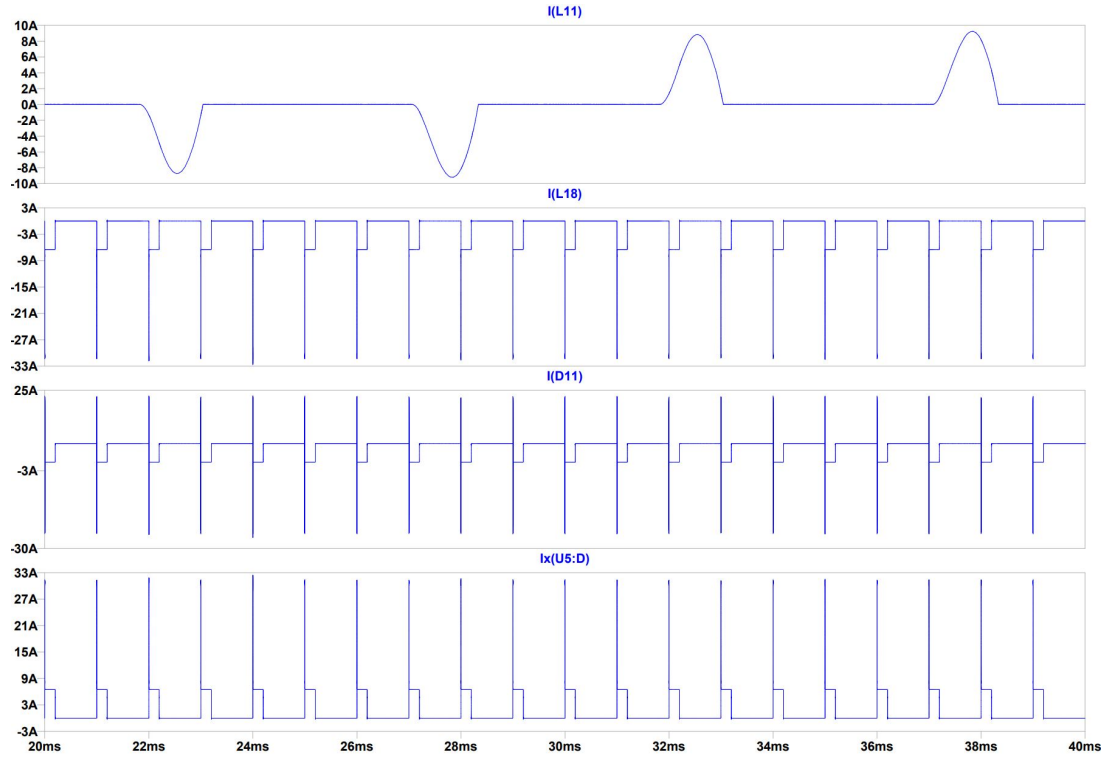

Figure 3.5.3: LTspice simulation: I(L11) inverse of auxiliary current -i_{AUX}, I(L18) inverse of bus current -i_{bus} =-$i_{AUX} - i_C$, I(D11) freewheeling diode current i_D, Ix(u5:D) MOSFET current i_S.

Current spikes at turn-on are due to the freewheeling diode reverse-recovery and do not compromise the circuit operation. As a matter of fact, the real recovery current measured and shown in the next chapter, has a much lower amplitude.

Chapter 4

Thermal management

A fundamental part of the project development consists in the evaluation of the power dissipated by the devices selected to make up the circuit. The goal of these calculations is the proper design and specification of the heat sinks to pull over the power devices, in order to keep the latters in their safe operating region, preventing reliability and performance drops or, worse, the device failure. In fact, high temperature enhances physical phenomena that lead to device degradation or rupture. Therefore, a chapter discussing the need to control the internal temperature of power electronic components and the factors to be considered is of great importance in the thesis discussion.

4.1 Control of semiconductor device temperatures

The theoretical upper limit on the internal temperature of a semiconductor device is the so-called intrinsic temperature, T_i, which is the temperature at which the intrinsic carrier density in the most lightly doped region of the semiconductor device equals the majority carrier doping density in that region. Taking a silicon diode as an example, if this temperature is exceeded, the rectifying characteristics of the junction are lost because the intrinsic carrier density greatly exceed the doping density, and the depletion region that gives rise to the potential barrier is shorted out by the intrinsic carriers.

However, the maximum internal temperatures specified on data sheets are much less than this limit. The power dissipation in power semiconductors normally increases with the internal temperature, and the losses become excessively high even at temperatures lower than the intrinsic one. Typical temperatures for which the device manufacturers guarantee the maximum values of device parameters such as on-state conduction voltages, switching times and switching losses at a specified maximum temperature, span from 125° to 175°.

4.2 Heat dispersal

The power dissipation occurs inside the silicon die and causes a rise in temperature that needs to be controlled in order to keep the maximum junction temperature below the device manufacturer's indication. For this purpose, a heat sink is typically used to facilitate the heat removal from the device die and the dispersion in the ambient. The heat flow goes through different materials before reaching the ambient. The following figure shows the situation.

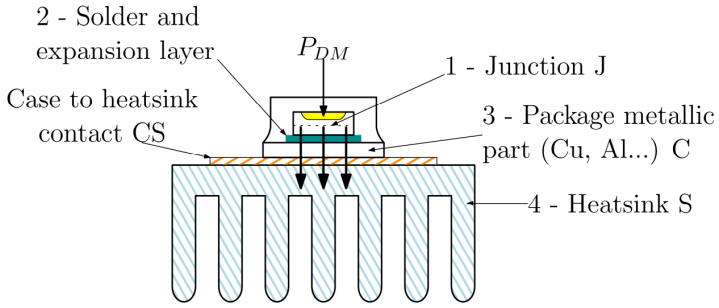

Figure 4.2.1: Multiple layer structure for thermal discussion [**4**].

The heat produced in the silicon die is transferred to the package through the solder and expansion layer, needed to avoid mechanical stresses due to the different expansion coefficient between die and package. After that, the heat flow goes through the package's metallic part, which most of packages are equipped with, that helps heat transfer. This metallic part is electrically connected to one of the device terminals, for example to the drain of a MOSFET or the collector of an IGBT. Since the heat sink is usually grounded, a case to heat sink contact is required to guarantee electrical isolation. Finally, the heat reaches the heat sink, shaped to maximize the air contact as to facilitate the heat transfer towards the ambient. The heat, flowing through these materials, produces a temperature drop, that, as a first approximation, can be considered proportional to the heat flux. The proportionality factor is called "thermal resistance" R_{th}, measured in $°C/W$. The heat dispersal can be represented by an electrical equivalent circuit, in which all interfaces between two materials are represented by thermal resistances. The heat flux is instead represented by a current proportional to the power dissipated in the device. In order to take into account also the time varying power dissipation the thermal capacity of the materials has to be considered. In fact, a material must absorb a given heat quantity in order to increase its temperature. This can be accounted for by adding capacitances C_{th} in the equivalent electrical circuit, measured in $J/°C$. The voltage drop across each resistor represents the related temperature drop

across two in contact materials. The ambient is represented as a voltage generator that keeps the voltage constant, assuming the ambient temperature isn't affected by the heat transfer.

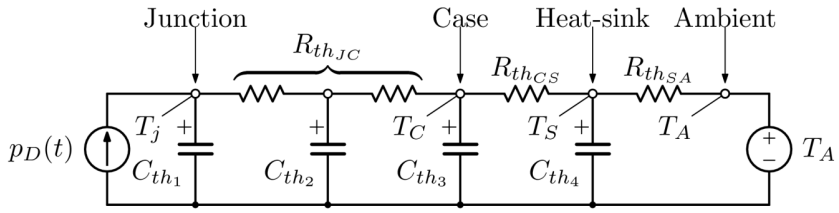

Figure 4.2.2: Transient electrical equivalent model of the heat flux [**4**].

This distributed *R-C* network justifies the temperature behaviour of different nodes when a time-varying (typically pulsed) dissipated power is applied. The maximum reached temperature T_{Jmax} depends on the power pulse peak value P_{DM} and its duration t_p and can be calculated only if the network elements are known. Assuming a linear system, all resistances and capacitances are constants. Under this assumption, the maximum junction temperature can be estimated from the dissipated power pulse as follows:

$$T_{Jmax} = T_A + P_{DM} \cdot Z_{th}(t_p) \tag{4.2.1}$$

where $Z_{th}(t_p)$, called "transient thermal impedance", depends on the equivalent network structure and is a function of t_p. Usually the heat sink thermal capacitance C_{thS} is much greater than the one associated to its junction area. The same goes for the thermal capacity of the package C_{thC}, since the latter is well thermally connected to the heat sink. For typical values of power pulse duration t_p, the case temperature T_C can be considered constant. Thus, T_J is usually expressed as a function of T_C and the junction to case transient thermal impedance Z_{thJC}:

$$T_{Jmax} = T_C + P_{DM} \cdot Z_{thJC} \tag{4.2.2}$$

The previous expressions yield the maximum junction temperature for a single dissipated power pulse, starting from a rest situation. When the dissipated power pulses repeat with a period Ts, the junction cannot completely cool down between two consecutive pulses. In this situation, the maximum junction temperature is lower than the value there would be if the power P_{DM} was continuously applied, but higher than the value corresponding to the average dissipated power, as illustrated in the following figure.

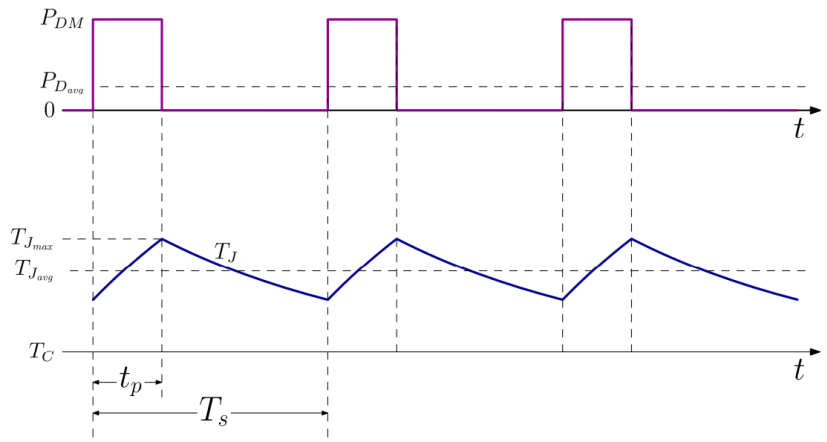

Figure 4.2.3: Thermal response to a periodic pulsed power [**4**].

The repetition of dissipated power pulse of duration t_p and period T_S have an average power dissipation that corresponds to an average junction temperature. However, the periodic repetition causes a ripple in the junction temperature that must be kept into account to consider the maximum value reached by the junction.

4.3 Power losses computation

After describing how the heat transfer in a power device can be modeled, the discussion proceeds with the computation of the power devices dissipation losses. The results, as seen in the previous section, will allow the proper sizing of the heat sinks.

The computation will be referred to the power devices that are predisposed for the heat sink pull over. In this case they are:

- Power switch
- Freewheeling diode

Moreover, the power losses calculation will be performed for the implementation via thyristor of the current configuration of the output stage of the voltage regulator. This will allow to make a comparison to understand if there is an advantage in the use of controllable power switch, instead of the thyristor, from the heat sink size point of view.

Since the heat sink must be suited for every excitation system operating condition, the worst-case scenario has to be considered. This means the calculations are going to be performed assuming a situation in which the device power loss is maximised, so

the resulting heat sink will be able to remove sufficient heat from the die up to that condition, as well as all the other less critical operating situations.

Such worst-case operating conditions coincide with the absolute ratings described in Section 3.2, which are the specifications given by the company in order to guarantee the desired excitation system capability for every situation and product. The design inputs needed for the following computations are reported below:

- Auxiliary generator RMS voltage: $V_{AUX,rms} = 230\,V$
- Exciter stator excitation current: $I_L = 6.5\,A$

The following three sections will compute the power losses of switch, thyristor and freewheeling diode (coupled with either the switch or the thyristor) considering the above-mentioned operating situation.

4.3.1 MOSFET power losses

Power losses P_l in any component operating in the switch-mode can be divided in three groups:

- Conduction losses P_C
- Switching losses P_S
- Blocking (leakage) losses P_B, normally being neglected

Therefore:

$$P_l = P_C + P_S + P_B \simeq P_C + P_S \tag{4.3.1}$$

Conduction losses When the device is fully on, the only electrical resistance is represented by the drain-source on-state resistance (R_{DSon}):

$$v_{DS}(i_D) = R_{DS,on} \cdot i_S \tag{4.3.2}$$

v_{DS} and i_S are drain-source voltage and the drain current, respectively. This resistance is due to many contributions, as Fig. 4.3.1 shows:

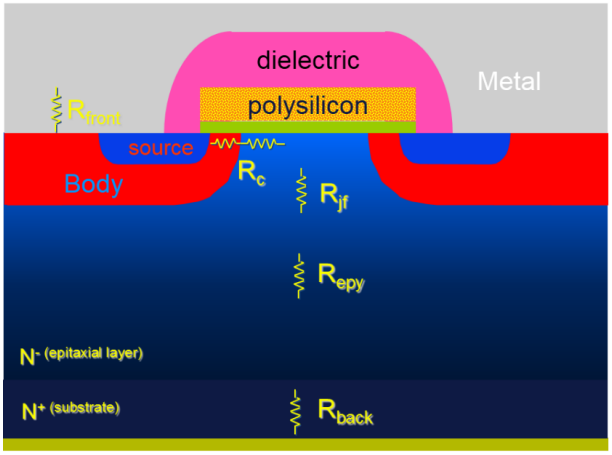

Figure 4.3.1: Power MOSFET structure [**15**].

The typical on-state resistance at ambient temperature can be read from the datasheet diagram of the device (reported below).

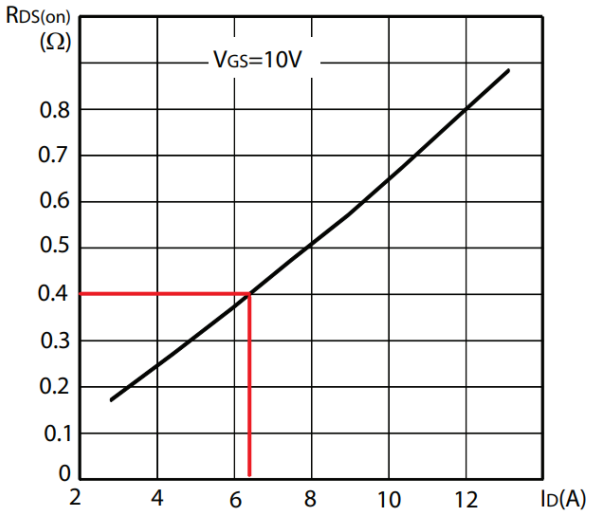

Figure 4.3.2: On-state resistance VS drain current characteristics at 25°C [**32**].

In the case of a drain current of 6.5 A the on resistance would result to be 0.4 Ω at 25°C. However, looking at the resistance characteristic at ambient temperature is not enough. In fact, the on-state resistance increases significantly with increasing junction temperature. The positive temperature coefficient of the on-state resistance arises from the decrease of the carrier mobility as the semiconductor temperature increases. This occurs because at higher temperatures the charge carriers undergo more collisions per unit time with the semiconductor lattice because each lattice atom has a larger amplitude of vibration at higher temperatures. The mobility is approximately inversely

proportional to the number of collisions per unit time with the lattice, and R_{DSon} is inversely proportional to the mobility. The overall behaviour is also reported in the datasheet. It is clear it is necessary to consider the maximum temperature the silicon die is going to work at, because a higher temperature results in a higher resistance and thus higher conduction losses. From the MOSFET datasheet [**32**] it's also possible to read the maximum operating junction temperature T_j is $150°C$. Keeping the junction temperature even below this maximum temperature level is a good design rule. For this reason, a 10% safety margin has been kept, fixing the considered maximum junction temperature at $135°C$. From the datasheet on-state resistance versus junction temperature diagram, reported below, a 2.25 times factor compared to the ambient temperature one is found.

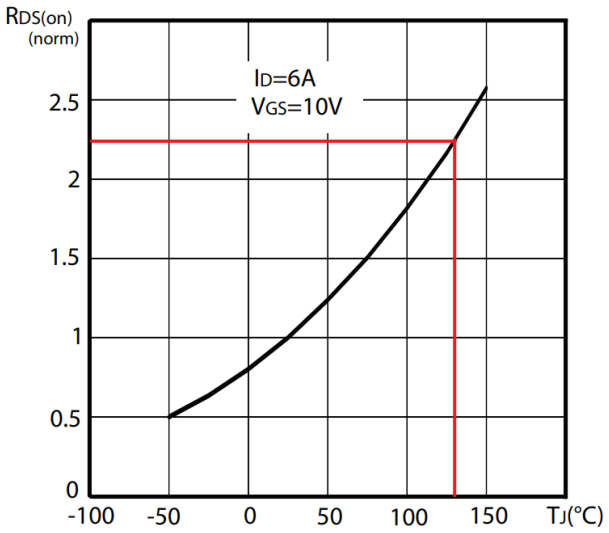

Figure 4.3.3: $R_{DS,on}$ VS T_j characteristics [**32**].

So the final value considered for the on-state drain-source resistance is:

$$R_{DS,on}(135°C) = 0.4\,\Omega \cdot 2.25 = 0.9\,\Omega$$

Once the on-state resistance is found, the conduction power losses can be evaluated as they are due to the Joule's effect in the structure. Therefore, the instantaneous value of the MOSFET conduction losses is:

$$p_C(t) = v_{DS}(t) \cdot i_S(t) = R_{DS,on} \cdot i_S^2(t) \tag{4.3.3}$$

During MOSFET conduction the instantaneous power losses result in:

$$P_{DM} = R_{DS,on} \cdot i_L^2(t) = 38.025\,W \tag{4.3.4}$$

Integration of the instantaneous power losses over the switching cycle gives an average value of the MOSFET conduction losses,

$$P_C = \frac{1}{T_S}\int_0^{T_S} p_C(t)\,dt = \frac{1}{T_S}\int_0^{T_S} R_{DS,on} \cdot i_S^2(t)\,dt = R_{DS,on} \cdot I_{S,rms}^2 \tag{4.3.5}$$

where I_{Drms} is the RMS value of the MOSFET on-state current. When the MOSFET is in its off-state no power losses are experienced since no current is flowing through the device. Thus, it is possible to restrict the area analysis to the conduction phase. When the MOSFET is on the drain current i_D is equal to the current flowing through the inductive load i_L. As explained in Subsection 3.3.1, such current can be considered roughly constant, equal to its switching period average I_L, because of the large value of inductance of the exciter stator compared to the driving switching frequency. For these reasons, the RMS value of the drain current results to be

$$I_{S,rms} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_S(t)^2 dt} = \sqrt{\frac{1}{T_S}\left(\int_0^{d\cdot T_S} I_L^2\,dt + \int_{d\cdot T_S}^{T_S} 0\,dt\right)} = \sqrt{d}\cdot I_L \tag{4.3.6}$$

where d is the MOSFET gate command PWM duty cycle allowing to obtain $6.5A$ from $230\,Vrms$ of auxiliary voltage. Such a duty cycle value can be computed as follows: assuming the auxiliary voltage to be a sinewave, the diode bridge and the electrolytic capacitor convert the alternating waveform in a roughly constant voltage equal to $V_d = \sqrt{2}\,V_{AUX}^{rms} = \sqrt{2}\cdot 230\,V \simeq 325\,V$. Being the switching period average voltage applied to the inductive load equal to $d \cdot V_d$, the switching cycle average current through the inductor is going to be that voltage divided by the resistance R_L of the exciter stator. Therefore:

$$d = \frac{R_L I_L}{V_d} = \frac{10\Omega \cdot 6.5\,A}{325\,V} = 0.2 \tag{4.3.7}$$

Finally, the average value of the MOSFET conduction losses results

$$P_C = R_{DS,on} \cdot I_{S,rms}^2 = d \cdot R_{DS,on} \cdot I_L^2 = 0.2 \cdot 0.9\,\Omega \cdot (6.5\,A)^2 = 7.605\,W \tag{4.3.8}$$

Switching losses During the on-off and off-on transitions, some power losses are present. They are due to the simultaneous presence of voltage across and current through the MOSFET during commutations. For this reason the typical approach is

to measure the energies involved during switching operations. Then, since they repeat periodically every switching cycle, the related power losses are computed multiplying the energies times the switching frequency:

$$P_S = (E_{on} + E_{off}) \cdot f_S \tag{4.3.9}$$

Since the switching frequency of this application is low, just $1\,kHz$, it is expected the contribution of switching losses to the overall power losses to be small compared to the conduction ones, being the dominant term. However, in the following the switching losses for this application are discussed, with the purpose to prove its negligibility.

With regard to the turn-off losses it is possible to assert that, in the presence of the turn-off snubber, they are almost deleted. In fact, the turn-off snubber, forcing the drain-source voltage to stay low while the drain current decreases, has the effect to cancel the overlap between voltage and current in the device at turn-off. In reference to the discussion on the turn-off snubber design, in Subsection 3.3.9, the chosen snubber capacitance is large enough so that the current fall time t_{fi} is much smaller than the time the capacitor takes to charge up to reach V_d, named t_{rv}. The following capture shows such trends.

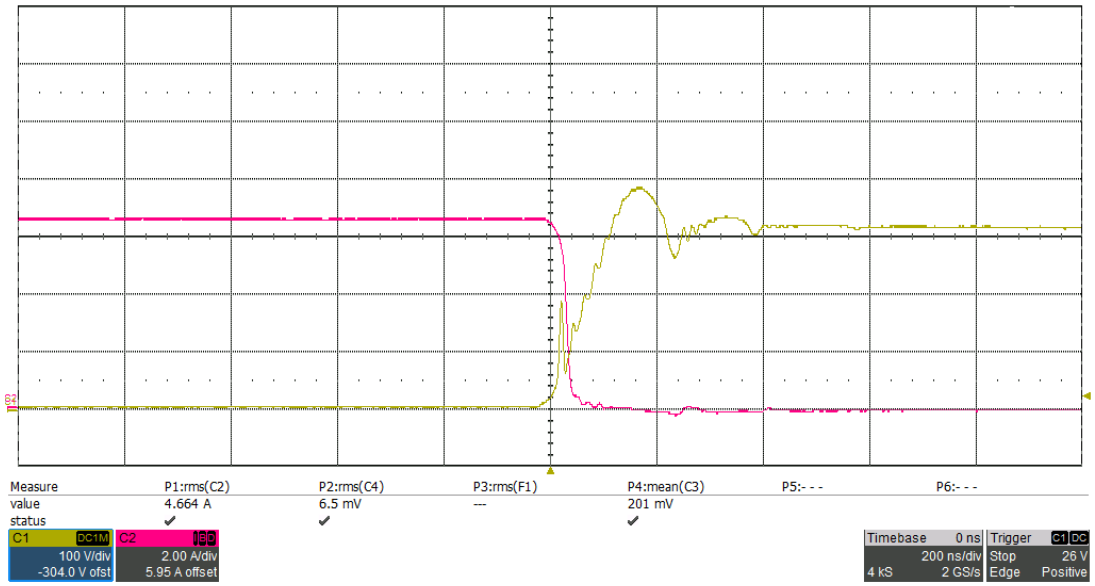

Figure 4.3.4: MOSFET turn-off transient. C1: v_{DS}; C2: i_S.

A rough computation can be made looking at these waveforms. In order to simplify the computation it is assumed the drain current drops linearly from I_L to $0\,A$ during a fall time $t_{fi} = 43.5\,ns$ and the drain-source voltage to have a constant value equal to

the average value during t_{fi}, that is about $V_{DS,off} = 100\,V$. With this assumption the turn-off switching losses result:

$$P_{S,on} = \frac{I_L \cdot V_{DS,off} \cdot t_{fi} \cdot f_S}{2} = \frac{6.5\,A \cdot 100\,V \cdot 43.5\,ns \cdot 1\,kHz}{2} = 0.014\,W \qquad (4.3.10)$$

that is 0.19% with respect to the conduction losses previously computed.

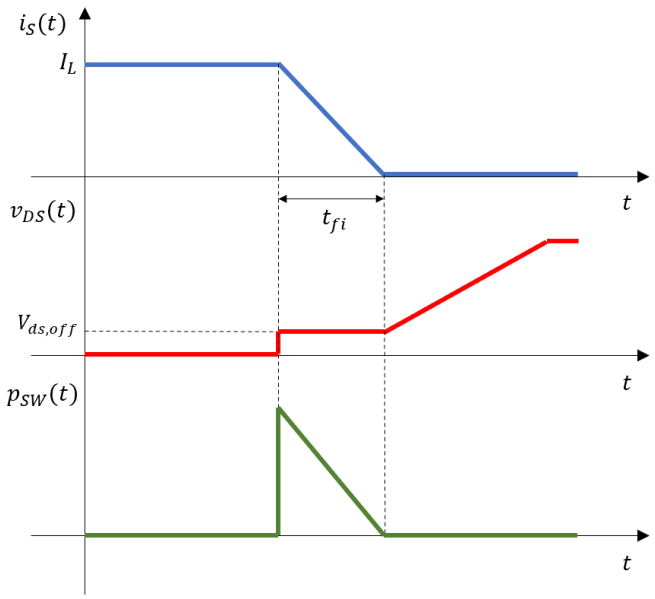

Figure 4.3.5: MOSFET turn-off simplified trends of drain current, drain-source voltage and instantaneous power losses for switching losses computation.

The main contribution to the switching losses is determined instead by the turn-on transient. In such event the drain-source voltage is allowed to drop only after the drain current has risen up to the on current plus the reverse recovery current of the freewheeling diode, as described in Subsection 3.3.9. During the time interval i_S rises, t_{ri}, v_{DS} undergoes a voltage drop ΔV_{on} due to the presence of distributed stray inductances in the circuit. The following image shows such trends.

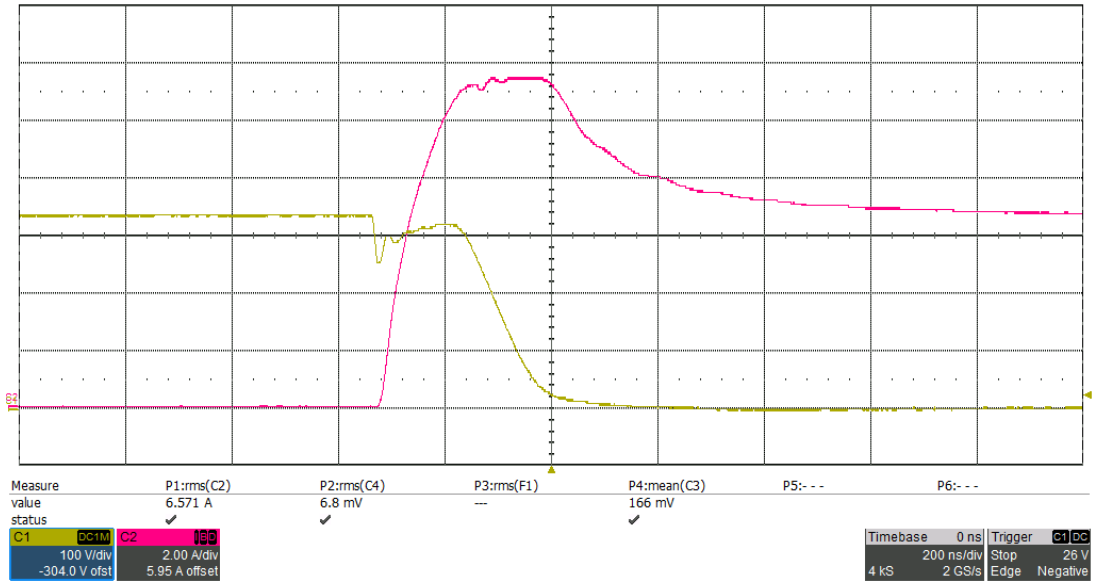

Figure 4.3.6: MOSFET turn-on transient. C1: v_{DS}; C2: i_S.

In order to compute the energy dissipated during the turn-on transient it is convenient to divide the voltage and current overlapping time interval in two sub-intervals: the first, lasting $t_{ri} = 163\,ns$, related to the period the drain current takes to reach its top value; the second, lasting $t_{fv} = 168\,ns$, linked to the time the drain-source voltage takes to drop from the intermediate value $V_d - \Delta V_{off}$ to $0\,V$. As it has been done for the turn-off transient, also in this case the trajectories are subdivided in straight lines, simplifying the power loss computation. With these assumptions the turn-on switching losses can be computed:

$$P_{S,off} = \frac{(I_L + I_{RR}) \cdot (V_d - \Delta V_{off}) \cdot (t_{ri} + t_{fv}) \cdot f_S}{2} = \frac{11.5\,A \cdot 300\,V \cdot 331\,ns \cdot 1\,kHz}{2} = \\ = 0.571\,W \tag{4.3.11}$$

that is 7.51% with respect to the conduction losses.

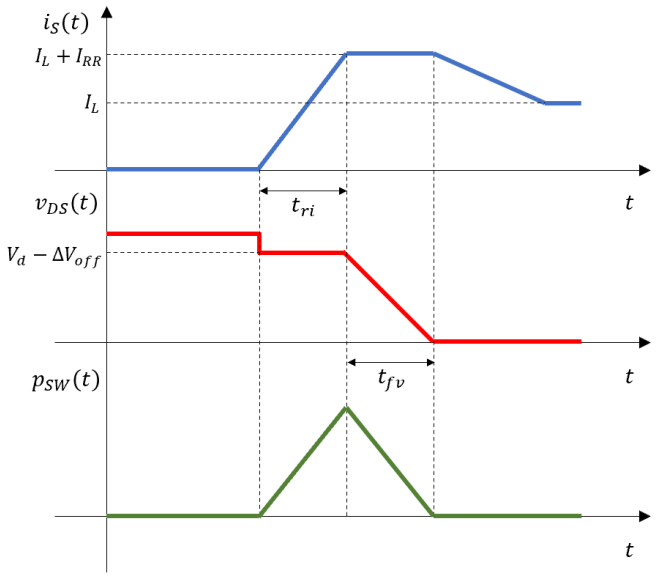

Figure 4.3.7: MOSFET turn-on simplified trends of drain current, drain-source voltage and instantaneous power losses for switching losses computation.

The following table summarizes and compares the terms that compose the MOSFET power losses.

	Power losses $[W]$	Percentage $[\%]$
Conduction	7.605	93
Switching	0.585	7
Total	8.190	100

This demonstrates that, as expected, the contribution of the switching losses accounts for an extremely small part of the overall MOSFET power losses. For this reason the heatsink sizing is going to be based to the only conduction losses of the device. The reader has to note the key reason why the switching losses are negligible is the operating MOSFET switching frequency: the low $1kHz$ value, compared to the nowadays controlled power switch capability to operate in the MHz order of magnitude, allows to delete the losses related to the power switch commutations.

4.3.2 Thyristor power losses

The power losses evaluation for the thyristor-based output stage of the voltage regulator is useful in order to provide a comparison between the current topology and the proposed one in this thesis from the heat sink sizing point of view.

Like the MOSFET the thyristor is a power switch too. As already explained the main difference is that the thyristor is a only turn-on controllable device, because the

turn-off transition is forced by the external circuit. Despite this, the power losses are composed by a conduction and a switching term, like the already discussed MOSFET. However, it is immediately possible to notice the conduction term is the dominant one. In fact, the switching frequency the thyristor operates in this application is the same of the auxiliary voltage waveform, that is $50Hz$. This extremely low switching frequency let the discussion to neglect a priori the switching losses term.

The average conduction power loss can be calculated using the following equation:

$$P_C = V_{T0} \cdot I_{T,av} + r_T \cdot I^2_{T,rms} \tag{4.3.12}$$

where V_{T0} and r_T are the parameters describing the approximated model for the i-v characteristic of the on-state diode-like behaviour of the thyristor. However, the MCR8SN thyristor datasheet does not provide such parameters. Instead the power dissipation is assessable from the following diagram.

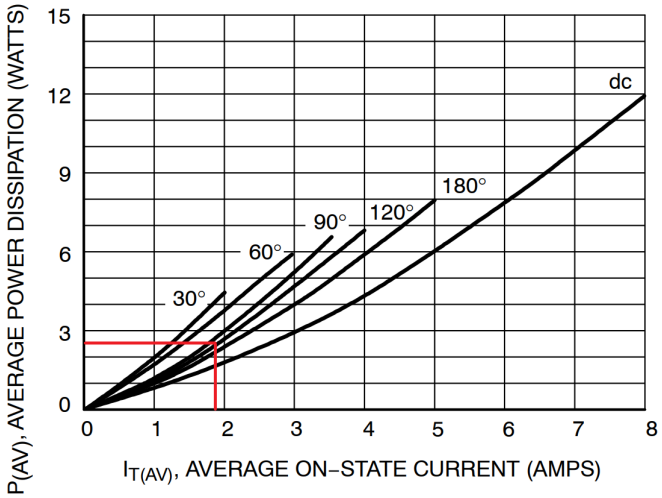

Figure 4.3.8: Average power dissipation VS average on-state current **[34]**.

The reported characteristic provides the average value of the power dissipation as function of the average on-state current and the trigger angle α the device is controlled by. From Eq. 2.2.10 it results an angle $\alpha = 104.4°$ is able to provide on average 6.5 A of current on the inductive load from a 230 $Vrms$ auxiliary sinewave supply. As regards the on-state average current let's recall that in case of the thyristor implementation the current ripple is no negligible as in the case of the much higher commutation frequency at which the MOSFET is driven. Recalling the thyristor current trajectory shown in Fig. 2.2.6, reported below for sake of simplicity, it is possible to derive the value of the average on-state current.

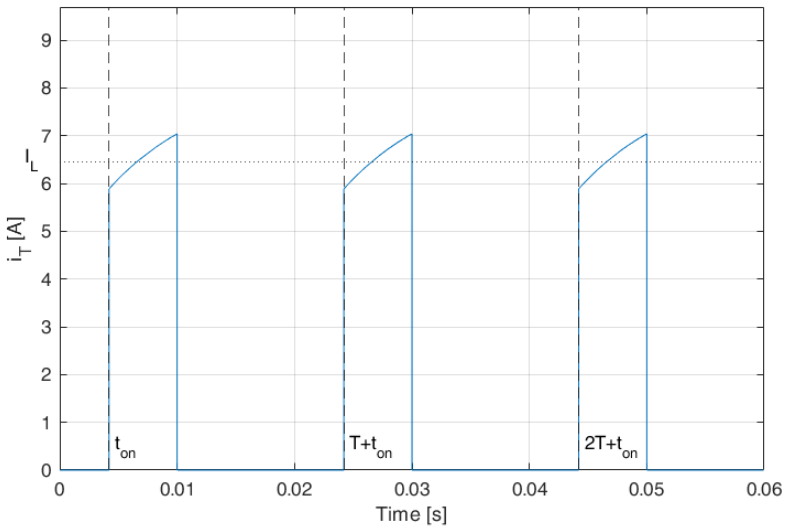

Figure 4.3.9: Thyristor current.

$$I_{T,av} = \frac{1}{T}\int_0^T i_T(t)\,dt = \frac{1}{360}\int_{180°-\alpha}^{180°} i_T(t)\,dt = \frac{\alpha}{360°}I_L = \frac{104.4°}{360°}6.5\,A = 1.885\,A \tag{4.3.13}$$

From Fig. 4.3.8 it is possible to see the corresponding average power dissipation is $P_C = 2.5\,W$, that is about one-third of the MOSFET power losses. The main reason for this difference is to be found in the thyristor to have an on-state voltage drop lower than the MOSFET one.

4.3.3 Freewheeling diode power losses

As anticipated in Section 4.3 the power losses for the freewheeling diode are going to be computed both for the proposed MOSFET-based topology and the current thyristor-based one. This is because the diode losses do not only depend on the device itself, but also on the overall circuit properties, as it will be described later. It is important to say the chosen STTH1210D diode is not the one used in the current Mecc Alte thyristor-based implementation of the voltage regulator. However, independently on the diode selection, a fair comparison between the two topologies requires the assumption to use the same freewheeling diode. It's clear that the future shown advantage of one topology in power dissipation point of view will be kept independently from the selected device.

Like the MOSFET and the thyristor, the freewheeling diode operates as a power

switch in the circuit. Recalling the basics about switching an inductive load from Subsection 2.1.2, the freewheeling diode acts in a complementary way with respect to the main switch: when the switch is on the diode is reversely polarized (off); when the switch turns off the diode closes the loop for the inductive load current, so being forced to conduct from the external circuit. For this reason, as done for the two previous subsections, it is possible to divide the freewheeling diode power losses in conduction and switching losses.

Conduction losses The conduction losses in a diode appear when the diode is in forward conduction mode due to the on-state voltage drop v_D. On the contrary, when the diode is reversely-biased, the extremely low value for the reverse leakage current (in the μA range) make the off-state losses to be completely negligible.

There are many ways to model the diode *i-v* characteristics. Similar to any device, diode equivalent models assume different positions in the accuracy-simplicity tradeoff. The following image summarize the typical methods of replacing diode by its circuit equivalent model.

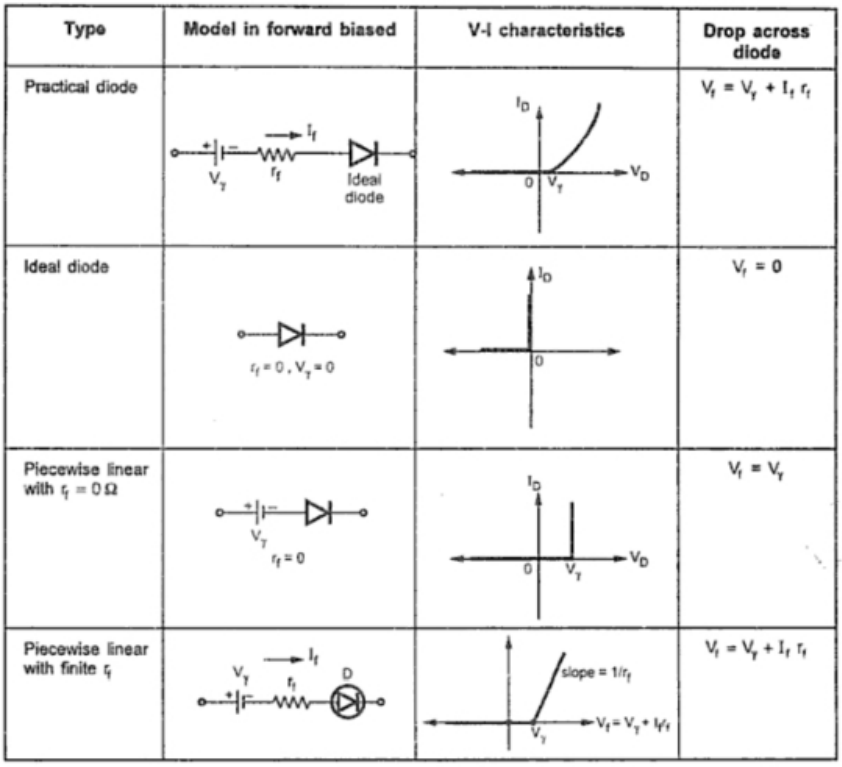

Figure 4.3.10: Diode equivalent circuits.

The typical conduction losses description in power rectifiers exploits the so called

piecewise linear (PWL) modelling. This method is used to approximate the diode characteristic curve as a series of linear segments. The real diode is modelled as three components in series: an ideal diode, a voltage source and a resistor.

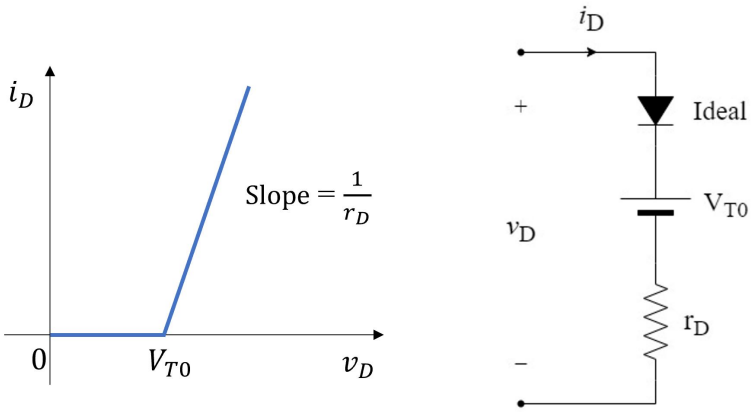

Figure 4.3.11: Piecewise linear model of the diode forward characteristic and its equivalent circuit representation.

Typically the sloped line segment would be chosen tangent to the diode curve at the working point (Q-point). Then the slope of this line is given by the reciprocal of the small-signal resistance of the diode at the Q-point.

The PWL modelling fully describes the forward characteristics from the knowledge of the threshold voltage V_{T0} and a dynamic resistance r_D. Such parameters are given by the device manufacturer in the STTH1210D diode datasheet: $V_{T0} = 1.3\,V$, $r_D = 33\,m\Omega$. The total voltage diode voltage is then represented by the following equation:

$$v_D(i_D) = V_{T0} + r_D \cdot i_D \tag{4.3.14}$$

The instantaneous conduction losses can therefore be computed as the product of voltage and current:

$$p_C(i_D) = v_D \cdot i_D = V_{T0} \cdot i_D + r_D \cdot i_D^2 \tag{4.3.15}$$

Finally, the integration of the instantaneous power losses over the switching cycle results in the average value of the diode conduction losses.

$$P_C = \frac{1}{T_S}\int_0^{T_S} p_C(t)\,dt = \frac{1}{T_S}\int_0^{T_S} V_{T0} \cdot i_D + r_D \cdot i_D^2\,dt = V_{T0} \cdot I_{D,av} + r_D \cdot I_{D,rms}^2 \tag{4.3.16}$$

where $I_{D,av}$ is the forward average current and $I_{D,rms}$ is the forward root mean square current flowing through the diode in a period interval.

At this point, of the discussion it in necessary to distinguish between the two circuit topologies. In fact, if on one hand V_{T0} and r_D are fixed with the diode, on the other the average and RMS value of the current through it depend on the considered topology.

In the case of the MOSFET implementation the computation proceeds as follows. Again, the current through the inductive load can be considered roughly constant and equal to I_L thanks to the reduced ripple because of high switching frequency compared to the load inductance (look at Subsection 3.3.1 for full explanation). Recalling the project specification of $6.5\,A$ inductive load current are obtained from $230\,Vrms$ auxiliary supply voltage by means of a PWM command duty cycle $d = 0.2$, the fraction of the period the diode is forward-biased will be $(1-d) = 0.8$. The switching period average and RMS value of the diode current results:

$$I^M_{D,av} = \frac{1}{T_S}\int_0^{T_S} i_D(t)\,dt = \frac{1}{T_S}\left(\int_0^{d\cdot T_S} 0\,dt + \int_{d\cdot T_S}^{T_S} I_L\,dt\right) = (1-d)\cdot I_L \tag{4.3.17}$$

$$I^M_{D,rms} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_D(t)^2 dt} = \sqrt{\frac{1}{T_S}\left(\int_0^{d\cdot T_S} 0\,dt + \int_{d\cdot T_S}^{T_S} I_L^2\,dt\right)} = \sqrt{1-d}\cdot I_L \tag{4.3.18}$$

Finally, the average value of the diode conduction losses in the MOSFET configuration results

$$\begin{aligned} P^M_C &= V_{T0}\cdot(1-d)\cdot I_L + r_D\cdot(1-d)\cdot I_L^2 = 1.3\,V\cdot 0.8\cdot 6.5\,A + 0.033\,\Omega\cdot 0.8\cdot(6.5\,A)^2 = \\ &= 7.8754\,W \end{aligned} \tag{4.3.19}$$

As a double check the manufacturer datasheet provides also a diagram showing the conduction losses as function of the average current $I_{D,av} = (1-d)\cdot I_L = 5.2\,A$ and the duty cycle related to the diode conduction time interval $(1-d) = 0.8$. It is possible to appreciate the resulting conduction losses match Eq. 4.3.3.

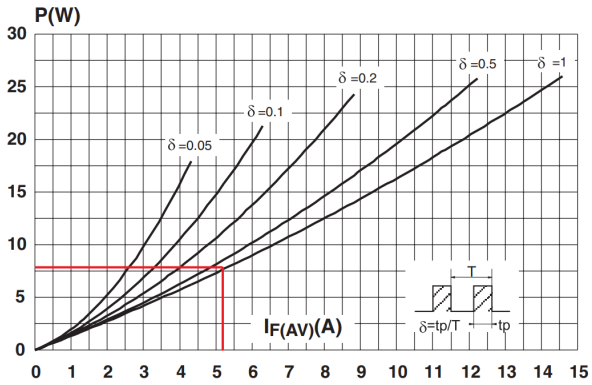

Figure 4.3.12: Conduction losses VS average current for MOSFET-based configuration [33].

Considering the thyristor-based implementation, similarly to what done for the thyristor conduction losses, it is necessary to consider the ripple to which the inductive load current is subject. Recalling from Fig. 2.2.6 the diode current trajectory, reported below for sake of simplicity, the average and RMS values of the diode current is then found.

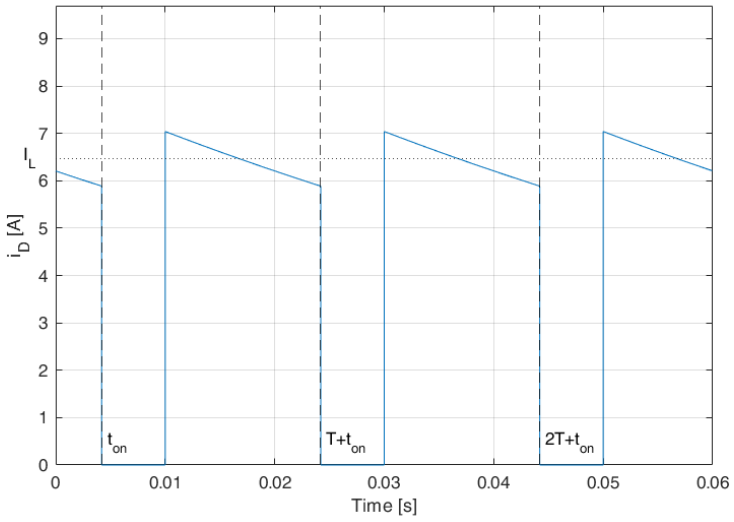

Figure 4.3.13: Freewheeling diode current in the thyristor-based implementation.

$$I_{D,av}^{T} = \frac{1}{T}\int_{0}^{T} i_D(t)\,dt = \frac{1}{360}\int_{180^\circ}^{360^\circ+\alpha} i_T(t)\,dt = \frac{360^\circ-\alpha}{360^\circ} I_L = \frac{255.6^\circ}{360^\circ} 6.5\,A = 4.615\,A \tag{4.3.20}$$

$$I_{D,rms}^{T} = \sqrt{\frac{1}{T}\int_0^T i_D(t)^2 dt} = \sqrt{\left(I_L^2 + \frac{\Delta I_L^2}{12}\right) \cdot \frac{360° - \alpha}{360°}} \tag{4.3.21}$$

where ΔI_L is the value of the current ripple. A way to compute its value has already been proposed in Subsection 3.3.1. Exploiting the same procedure the computation is performed looking at the off phase. The voltage across the inductor v_L results to be the reverse of sum of the voltage drop across the parasitic resistance $v_R = R_L \cdot I_L = 65\,V$ plus the voltage drop on the diode, negligible in comparison to the first term. With these assumptions the current is going to vary linearly in time, producing a current ripple of value

$$\Delta I_L = \frac{v_L}{L} t_{off} = \frac{R_L \cdot I_L}{L} \frac{360° - \alpha}{360°} \cdot T = \frac{10\,\Omega \cdot 6.5\,A}{0.8\,H} \frac{255.6°}{360°} \cdot 0.02\,s = 1.15375\,A \tag{4.3.22}$$

Finally, the average value of the diode conduction losses in the thyristor configuration results

$$P_C^T = V_{T0} \cdot I_{D,av} + r_D \cdot I_{D,rms}^2 = 1.3\,V \cdot 4.615\,A + 0.033\,\Omega \cdot (5.484\,A)^2 = 6.992\,W \tag{4.3.23}$$

that is slightly lower than the case of the MOSFET-based topology. Also in this case it is possible to double check by means of the datasheet diagram conduction losses VS average current. Inputs in this case are $I_{D,av}^T = 4.615\,A$ and $\delta = \frac{360° - \alpha}{360°} = \frac{255.6°}{360°} = 0.71$. The resulting value matches what computed in Eq. 4.3.23

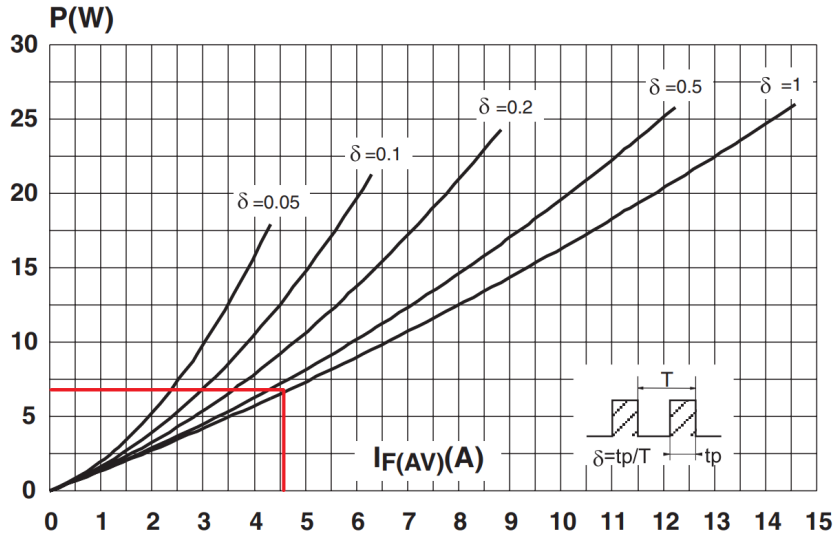

Figure 4.3.14: Conduction losses VS average current for thyristor-based configuration [33].

Switching losses It has already been said the freewheeling diode operates as a power switch acting in a complementary way with respect to the main switch. For this reason, it is interesting to investigate the losses related to its switching activity, as done for the MOSFET. The only 1 kHz switching frequency MOSFET-based topology will be discussed; the 50 Hz thyristor-based one results not to be relevant because of the much lower commutation frequency. It will be shown that even in the MOSFET-topology case the switching losses account for a negligible fraction with respect to the conduction ones. For this reason, in the thyristor-based one those will be even more negligible.

Turn-on losses of a power rectifier are typically not relevant. They are due to the voltage overshoot caused by the growth of the forward current, that encounters a high initial resistivity of the drift region because of the low-level carrier injection from p^+n^- and n^+n^- junctions. As the current increases the growth of the diode voltage slows and eventually turns over as the drift region becomes shorted out by the large amount of carrier injection into it. High injection level condition make conductivity modulation to occur: drift region resistivity and so forward voltage drop. The losses in this case would be due to the overlap between the voltage overshoot and the diode current increasing with a rate of change dictated by the main switch.

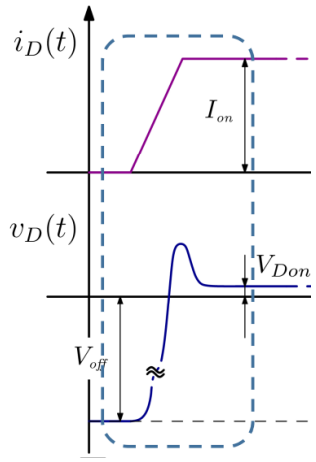

Figure 4.3.15: Diode Turn-on current and voltage trajectories [**4**].

However, the presence of the turn-off snubber makes this process to be extremely reduced in time. Recalling the MOSFET turn-off transient discussion, treated in Subsection 3.3.9, the diode current does not follow the same rate of change of the MOSFET, but instead it should, theoretically, instantly jump from zero to I_L as the drain-source voltage reaches V_d (that is when the voltage across the diode reaches zero). This trend is observable from the oscilloscope capture of v_{DS} and the snubber current i_{SN}.

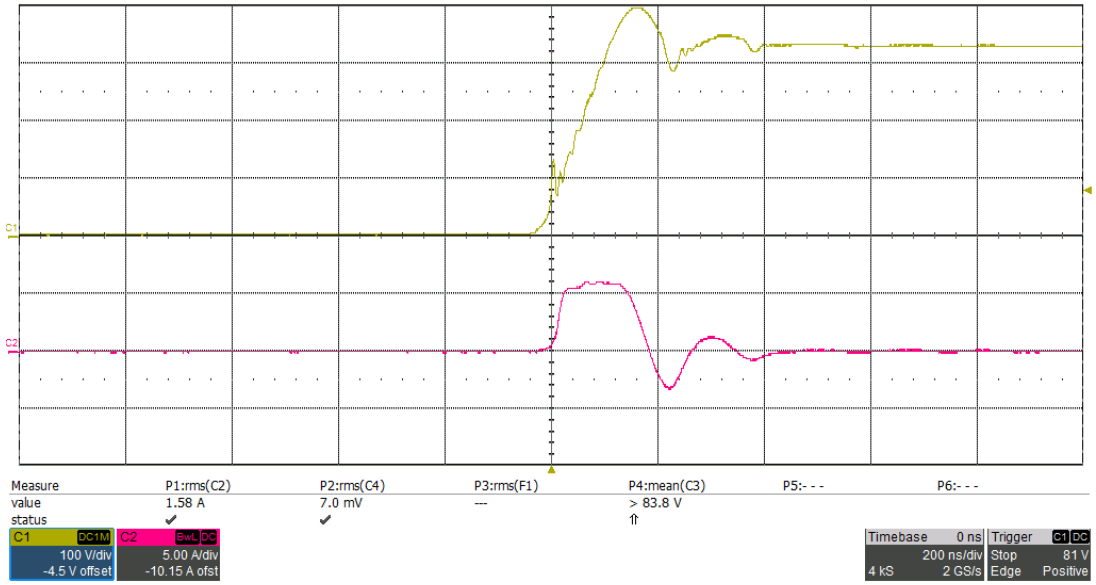

Figure 4.3.16: MOSFET turn-off transient. C1: v_{DS}; C2: i_{SN}.

The freewheeling diode current rises as the snubber current falls after being constant for a while. The relevant voltage overshoot observable in the figure is not actually due to the just cited phenomenon. Instead it's consequence of parasitic inductances distributed in the wiring connection between the MOSFET and the freewheeling diode. It is possible to assert this because the voltage overshoot peak verifies exactly when the diode current begins to grow, and not after, as expected if it was due to conductivity modulation phenomenon. The voltage overshoot for diode turn-on is actually present too, but completely surmounted by the other. For this reason, it is possible to neglect diode turn-on power losses.

A larger power consumption is instead related to the turn-off commutations. The reason is to be found in the diode reverse recovery process, occurring at every turn-off transition of the device. Since the physical phenomenon has already been discussed in Subsection 3.3.5, in this section the focus is on the quantification of the power losses caused by reverse recovery. Even if there is not availability of a direct oscilloscope measurement of the freewheeling diode voltage and current, it is possible to derive their trajectories from the MOSFET ones in Fig. 4.3.6 and the MOSFET snubber current i_{SN} ones here shown.

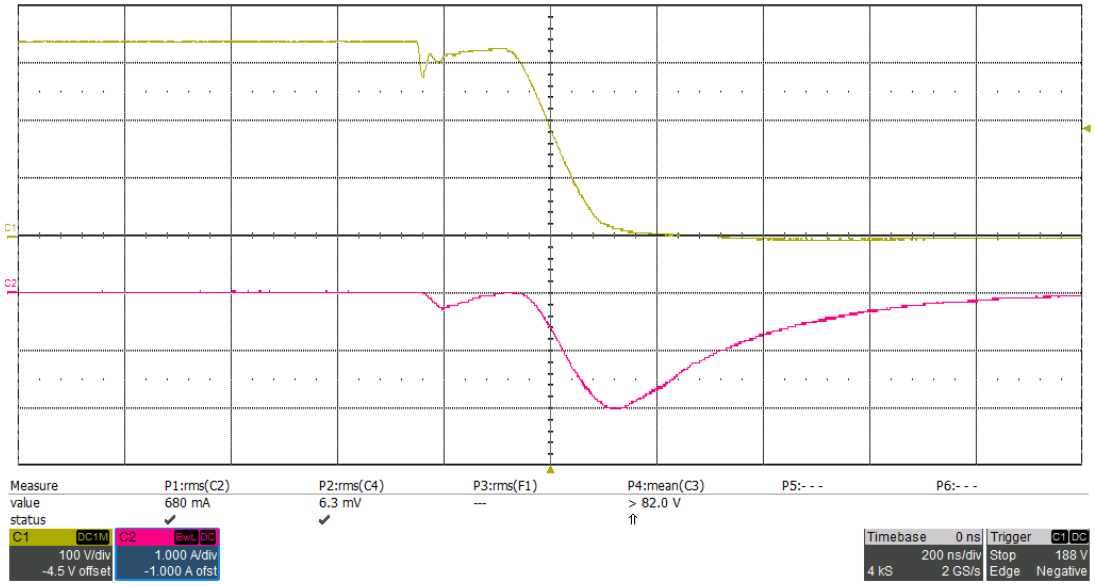

Figure 4.3.17: MOSFET turn-on transient. C1: v_{DS}; C2: i_{SN}.

In particular, the diode voltage can be expressed as $v_D = V_d - v_{DS} - L_\sigma \dfrac{di_D}{dt}$, where the last term being the voltage drop due to distributed stray inductance $L_\sigma$in the wiring connection between diode and power switch. On the other hand the current can be obtained from the trajectories of drain current and snubbers currents $i_D = I_L - i_S - i_{SN}$. As done for the MOSFET switching losses, even in this case the trajectories are modeled as piecewise linear functions, allowing a rough but simple computation.

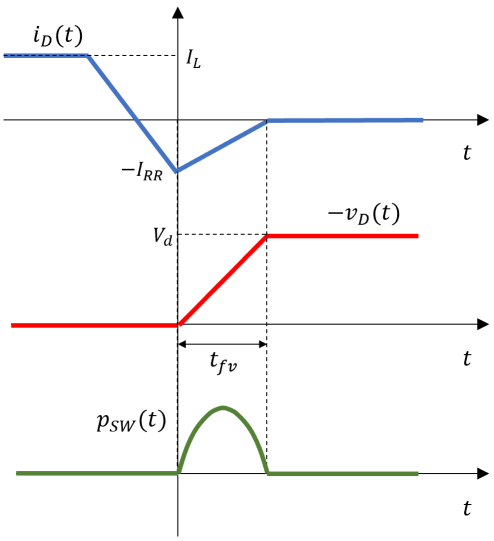

Figure 4.3.18: Freewheeling diode turn-off simplified trends of current, voltage and instantaneous power losses for switching losses computation.

During the interval t_{fv} in which power loss is manifested, it is possible to write the piecewise functions of current and voltage:

$$i_D(t) = I_{RR}\Big(\frac{t}{t_{fv}} - 1\Big) \tag{4.3.24}$$

$$v_D(t) = -\frac{V_d}{t_{fv}}t \tag{4.3.25}$$

With these assumptions the instantaneous power p_{SW}, being the product of linear current and voltage functions, is going to assume the quadratic trend:

$$p_{SW}(t) = v_D(t) \cdot i_D(t) = \frac{V_d \cdot I_{RR}}{t_{fv}}t\Big(1 - \frac{t}{t_{fv}}\Big) \tag{4.3.26}$$

With these assumptions the turn-off switching losses result:

$$P_{D,off} = \int_0^{t_{fv}} p_{sW}(t)\,dt \cdot f_S = \frac{V_d \cdot I_{RR} \cdot f_S}{t_{fv}} \int_0^{t_{fv}} \Big(t - \frac{t^2}{t_{fv}}\Big)\,dt = 0.046\,W \tag{4.3.27}$$

accounting for the 0.57% of the total diode losses in the MOSFET-based configuration. It is thus proven the switching losses are completely negligible compared to conduction losses in such topology. In the case of the thyristor-based one it is clear the switching losses related to the freewheeling diode are even smaller due to the 50 Hz switching frequency. A complete discussion and computation is not considered interesting in the thesis discussion because of the obvious outcome.

Below the results of the entire Section 4.3 are summed up: power losses for the current thyristor-based topology and the proposed MOSFET-based one are compared in the table. The reader has to notice MOSFET and freewheeling diode switching losses are neglected in the account of the total device dissipated power. As demonstred in this section the low 1kHz value of commutation frequency chosen to drive the inductive load allows to neglect the losses related to commutations, since they account for a minority part (less than 10%) of the entire losses.

	MOSFET-based topology	Thyristor-based topology
Main switch	7.605 W	2.5 W
Freewheeling diode	7.875 W	6.992 W

4.4 Heat sinks thermal resistance

Once completed the evaluation of the maximum dissipation losses for power devices in the circuit, it is finally possible to proceed with the needed heat sinks thermal resistances. The computation is going to be done for the MOSFET, the thyristor and the freewheeling diode in both the power switches configurations. The final outcome will allow to assert in which topology there is an advantage from the heat sink sizing point of view. In the industrial world an important interest is the cost reduction. For this reason, it is always preferable to try minimizing the cost for the company products. In this particular case this interest translated into the desire of small-size heat sinks, because of two reasons. The first is the direct consequence that a smaller heat sinks have lower price. The second is related to the space occupied by the heat sink itself over the printed circuit board: larger devices force the designer to arrange the various circuit components further each other, with the consequence of needing larger surfaces, directly related to the board cost. Since the heat sink size is inversely proportional to its thermal resistance, the best topology is going to be the one for which a larger thermal resistance is sufficient.

4.4.1 MOSFET heat sink thermal resistance

Being characterized by a time-varying periodic pulse dissipated power, the value of heat sink thermal resistance for the MOSFET can be computed by means of the procedure exposed in Section 4.2. The inputs for the calculation are exposed below. First of all from the STP13N80K5 MOSFET datasheet it is possible to read the maximum operating junction temperature is $150°C$. As anticipated in Section 4.3.1 keeping the junction temperature even below this maximum temperature level is a good design rule because it slows down the component degradation and aging process, resulting in a longer operating lifetime. For this reason, a 10% safety margin is kept, resulting in a design maximum junction temperature to $T_{Jmax} = 135°C$. Secondly, since the power dissipated by a device manifests as an increase in junction temperature, it is fundamental to know the ambient temperature the device is working at. This value has been provided by the company, being $T_A = 70°C$. It is due to the heating action of the generator itself, on which the regulator board is mounted on. Other required information consists in the junction-to-case thermal resistance, $R_{thJC} = 0.66\,K/W$ from the datasheet, and the case-to-heat sink thermal resistance R_{thCS}, not provided by the datasheet, but commonly considered to be $1\,K/W$. The value for the junction-to-case transient thermal impedance Z_{thJC} can be derived from the datasheet diagram reported

below knowing the power pulse peak period t_p and the related duty cycle.

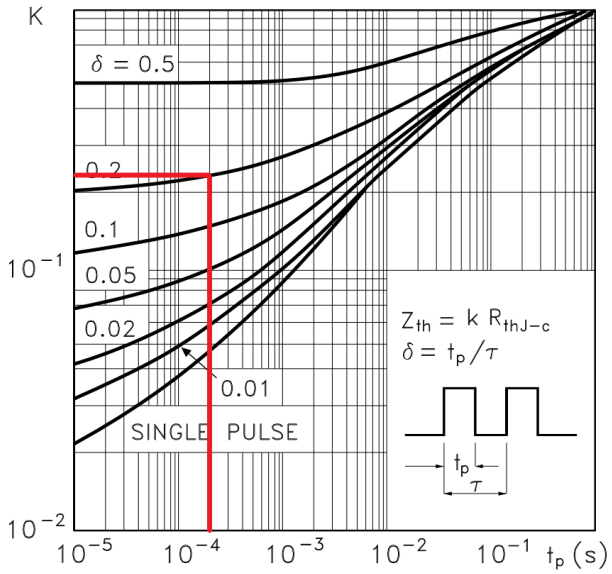

Figure 4.4.1: k multiplier for Junction-to-case transient thermal impedance computation in function of pulse duration and duty cycle **[32]**.

Recalling from Section 4.3.1 the duty cycle value is $d = 0.2$, thus $t_p = d \cdot T_S = 0.2 \cdot 1\,ms = 0.2\,ms$. It results a $k = 0.22$ multiplier factor, that allows to obtain the transient thermal impedance $Z_{thJC} = k \cdot R_{thJC} = 0.1452\,K/W$. At this point, the needed heat sink-to-ambient thermal resistance can be computed recalling the instantaneous and average values of the power dissipated by the MOSFET, computed in Section 4.3.1: $P_{DM} = 38.025\,W$ and $P_C = 7.605\,W$. The reader has to notice MOSFET switching losses are neglected in the account of the total device dissipated power. As demonstred in Subsection 4.3.1 the low $1kHz$ value of commutation frequency chosen to drive the inductive load allows to neglect the losses related to commutations, since they account for less than 10% of the total losses. Finally, from Eq. 4.2.2, heat sink-to-ambient thermal resistance is computed:

$$T_{Jmax} = T_C + P_{DM} \cdot Z_{thJC} = T_A + P_C \cdot (R_{thSA} + R_{thCS}) + P_{DM} \cdot Z_{thJC}$$

$$\begin{aligned} R_{thSA} &= \frac{T_{Jmax} - T_A - P_{DM} \cdot Z_{thJC}}{P_C} - R_{thCS} = \\ &= \frac{135°C - 70°C - 38.025\,W \cdot 0.1452\,K/W}{7.605\,W} - 1\,K/W = 6.821\,K/W \end{aligned} \tag{4.4.1}$$

4.4.2 Thyristor heat sink thermal resistance

Also the thyristor, like the MOSFET, is characterized by a time-varying periodic pulse dissipated power. However, the MCR8SN thyristor datasheet doesn't provide a diagram to assess the transient thermal impedance, but only information about thermal resistances. For this reason, the transient equivalent electrical network to model the heat dispersal described in Section 4.2 simplifies to its average version, in which the relevant variables (power and temperature) are considered only in terms of average values. The direct consequence of this simplification is the capacitive elements removal: for the ampere-second balance principle over one complete switching cycle the total ampere-seconds applied to a capacitor must be zero. For this reason, in the average equivalent electrical network the capacitors are replaced with open circuits.

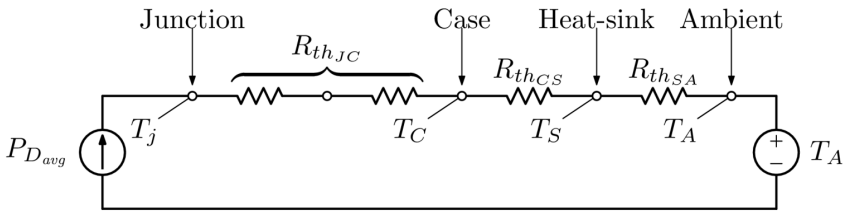

Figure 4.4.2: Average electrical equivalent model of the heat flux [**4**].

This model is characterized only by series of resistances, allowing a simple calculation of the junction temperature T_J knowing the ambient temperature T_A and the average dissipated power:

$$T_J = T_A + P_C \cdot (R_{thJC} + R_{thCS} + R_{thSA}) \tag{4.4.2}$$

As done for the MOSFET, the MCR8SN datasheet provides the inputs for the calculation. The maximum operating junction temperature is $110°C$ but, in a similar way to what done for the MOSFET, a 10% safety margin is kept, fixing the maximum temperature to about $100°C$. In order to make a fair comparison, the ambient temperature is fixed to the same value as the MOSFET, so $T_A = 70°C$. The junction-to-case thermal resistance is $R_{thJC} = 2.2\,K/W$, while the case-to-heat sink thermal resistance R_{thCS}, not provided by the datasheet, also in this case is considered to be $1\,K/W$. At this point, the needed heat sink-to-ambient thermal resistance can be computed recalling the average value of the power dissipated by the thyristor, computed in Section 4.3.2: $P_C = 2.5\,W$.

From Eq. 4.4.2 heat sink-to-ambient thermal resistance is computed:

$$R_{thSA} = \frac{T_{Jmax} - T_A}{P_C} - R_{thJC} - R_{thCS} = \frac{100°C - 70°C}{2.5\,W} - 2.2\,K/W - 1K/W = 8.800\,K/W \tag{4.4.3}$$

From the comparison of the results of Eq. 4.4.1 and 4.4.3 it is possible to evince that there is a small advantage in choosing the MCR8SN thyristor than the STP13N80K5 MOSFET. This advantage involves the necessity to a slightly larger heat sink to pull over the MOSFET. This is mainly due to the much higher power dissipation for the MOSFET, being strongly dependent on the junction temperature. No temperature dependence has been considered instead for the thyristor power loss computation because no information about this is provided.

4.4.3 Freewheeling diode heat sink thermal resistance

Since the same STTH1210D ultrafast recovery diode is considered to be used for both the configurations involving MOSFET and thyristor, after having computed its power losses in both the cases, it is possible at this point to compute the two heat sink-to-ambient thermal resistances needed to remove a sufficient amount of heat from the device die.

Like the MOSFET and the thyristor, it has already been expressed many times the freewheeling diode acts as a power switch in the circuit. For this reason, also this device is characterized by a time-varying periodic pulse dissipated power, that should be desirably modeled by means of the transient electrical equivalent model of the heat flux of Fig. 4.2.2. However, like in the case of the MCR8SN thyristor, even the STTH1210D datasheet does not provide any information to derive the transient thermal impedance in the case of a pulsed conduction behaviour. Only the case of a single pulse is presented, not useful for this thesis discussion. For this reason, the averaged version of the electrical equivalent model of the heat flux is exploited in this case too. Keeping into account the scheme of Fig. 4.4.2 the inputs for the computation are the here reported. The maximum operating junction temperature is $175°C$ but, as done for the MOSFET and the thyristor, a 10% safety margin is kept, fixing the maximum considered junction temperature to about $155°C$. $70°C$ is always the ambient temperature the regulator is considered to work at. The junction-to-case thermal resistance is $R_{thJC} = 1.9\,K/W$ and the case-to-heat sink thermal resistance is always considered to be $R_{thCS} = 1\,K/W$, in the lack of further datasheet indication. The last information needed is the average value of dissipated power by the diode in the MOSFET topology, $P_C^M = 7.8754\,W$, and in the thyristor topology, $P_C^T = 6.992\,W$. The reader has to notice power losses related

to switching activity are neglected even in the more critical case of the $1\,kHz$ commutation frequency of the MOSFET topology. As demonstrated in Subsection 4.3.3 such losses are negligible since accounting only for 0.57% of the total dissipation. Finally, from Eq. 4.4.2, heat sink-to-ambient thermal resistance is computed respectively for the MOSFET and thyristor topologies:

$$R^M_{thSA} = \frac{T_{Jmax} - T_A}{P^M_C} - R_{thJC} - R_{thCS} = \frac{155°C - 70°C}{7.8754\,W} - 1.9\,K/W - 1K/W = 7.893\,K/W \tag{4.4.4}$$

$$R^T_{thSA} = \frac{T_{Jmax} - T_A}{P^T_C} - R_{thJC} - R_{thCS} = \frac{155°C - 70°C}{6.992\,W} - 1.9\,K/W - 1K/W = 9.257\,K/W \tag{4.4.5}$$

Also in this case it results a slight advantage in favour of the thyristor topology. This occurs mainly because of the larger portion of the switching period the diode is forward polarized in the MOSFET circuit, being $(1 - d) = 0.8$, compared to the circuit with the thyristor, being $\frac{360° - \alpha}{360°} = 0.71$.

Below the results of the entire Section 4.4 are summed up: heat sink-to-ambient thermal resistances for the current thyristor-based topology and the proposed MOSFET-based one are compared in the table.

	MOSFET-based topology	Thyristor-based topology
Main switch	$6.821\,K/W$	$8.800\,K/W$
Freewheeling diode	$7.893\,K/W$	$9.257\,K/W$

Chapter 5

Experimental validation

This chapter intends to describe the tests performed on the developed circuit in order to observe, analyze and evaluate its actual operation on the field. The gathered measurements of the key parameters provide and show the results obtained in this thesis.

This chapter is structured into three paragraphs, each describing the progressive order by which the tests are performed on the proposed circuit. In a new engineering solution development, like the one of this thesis, it is a good practice not to test the prototype directly on a standard operational environment (in this instance, the closed-loop regulation of the output voltage in an operating generator), but progressively testing the circuit in order to check its functioning in every single detail. This way, it is possible to avoid unexpected behaviours which may endanger firstly people and secondly the system itself, due to the high voltages and currents involved.

5.1 Circuit test bench setup

Once realized a first prototype of the circuit the next step regards its test. In order to do so, it is considered appropriate not to operate directly on a real Mecc Alte generator, but instead to realize an on purpose test bench to verify the correct operation of the circuit. For this reason, as a first step the supply isn't provided by the auxiliary winding of a rotating generator, but instead by a variac. The variac is a variable autotransformer, that is a single-coil transformer in which two portions of the same coil are used as the primary and the secondary winding. The user can vary the output voltage acting on a knob attached to a wiper that makes contact with the transformer coil allowing the electricity to be "tapped" at any point along the winding for a specific voltage output. A variac is useful in this thesis application because it allows to control the amplitude of the input AC voltage, simulating the role of the auxiliary generator.

A very important aspect regards the simulation of the auxiliary winding parasitic inductive term. In this context the variac is well suited for this task. In fact, due to its realization, it inherently has an inductive nature. The single-coil transformer entails a parasitic inductance which has the same effect of the auxiliary winding inductance when the current through it is switched. This variac inductance, assessed in the same way of what done in Subsection 3.3.6, results to be $L_{variac} = 1.08\,mH$, not equal but the same order of magnitude of the considered auxiliary inductance $L_{AUX} = 0.5\,mH$.

Clearly, since the variac is supplied by the main grid, the output waveform is almost sinusoidal. This represents a difference compared to the auxiliary generator waveform having also third harmonic content. However, this difference does not represent a problem from the circuit operation point of view, since the aluminum electrolytic capacitor downstream of the diode bridge acts converting the input voltage to a roughly constant value equal to the input waveform peak. Actually the variac is not supplied directly by the main grid. Instead the utilization of a isolating transformed is considered a good safety precaution, in order to isolate the testing circuit from the grid.

On the other hand the inductive load consists of an exciter stator disassembled from the generator. Even if the exciter is not in operation, the exciter rotor metal core is inserted into the stator because it influences the exciter stator inductance. The inductance value is indirectly obtained from the measure, by means of digital multimeters, of RMS voltage and current applied. From the ratio between voltage and current, giving the impedance, and from the resistance (measured by the multimeter), the reactance and so inductance can be assessed.

It has to be explained the goal of this first setup is not to provide a closed-loop control of the generator output voltage (as it will be performed is Section 5.3), but instead being able to regulate the current flowing through the inductive load I_L acting on the power switch PWM duty cycle command. The PWM duty cycle is manually controlled by means of a simple circuit composed by a potentiometer and the Arduino Uno board. The potentiometer provides to an Arduino input analog pin a DC voltage between $0\,V$ and $5\,V$. This signal, converted to digital by the internal 10 bit ADC, is sent to the internal pulse width modulator, which provides a $5\,V$ rectangular pulse train having a duty cycle proportional to the input analog voltage.

Moreover, the goal of this first test step is to monitor the main voltages and currents in the circuit in order to detect possible unwanted behaviours. The whole test bench setup is shown below.

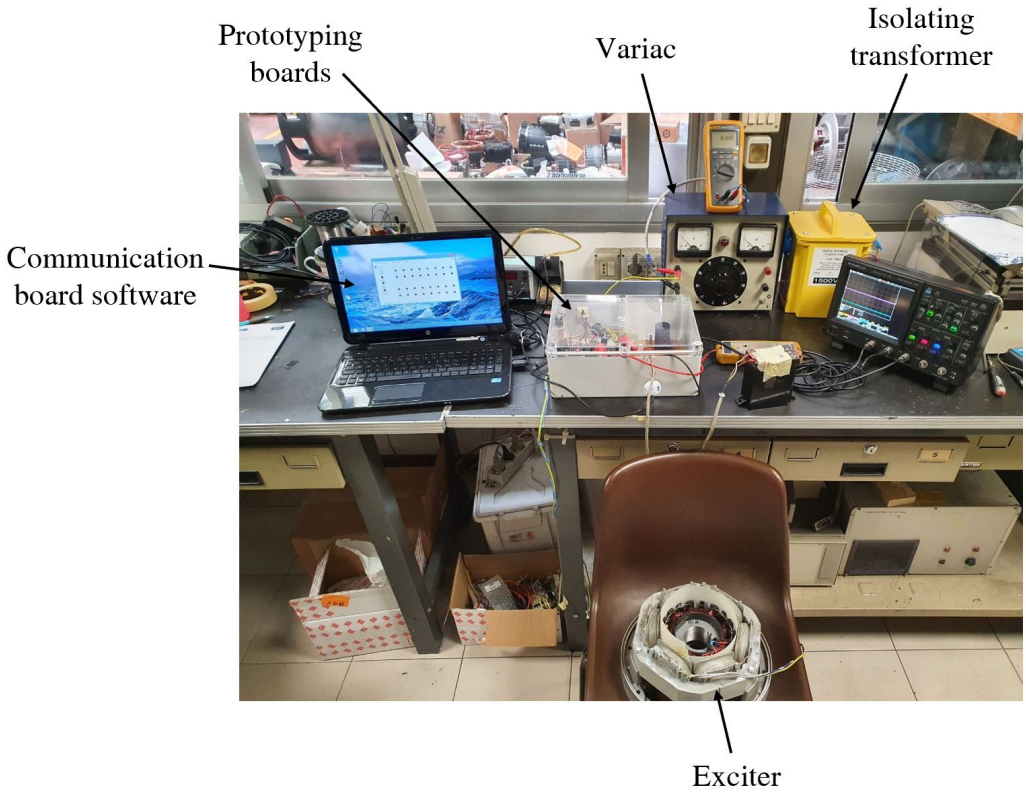

Figure 5.1.1: Test bench setup.

5.1.1 Results at project specification ratings

Thanks to the possibility to adjust the input voltage amplitude (acting on the variac) and the exciter stator current (acting on the potentiometer) the test bench created allows to be extremely flexible in evaluating the circuit performances under the desired solicitations. In fact, compared to the tests performed on real machines where operation in their nominal condition is assessed (see the next subsection), the test bench setup allows to perform the test at the worst-case projects specification ratings given by the company, listed in Section 3.2.

The following oscilloscopes acquisitions show the traces of the circuit key quantities at project specification nominal condition, that is 230 $Vrms$ input supply auxiliary voltage and maximum constant inductive load current $I_L = 6.5\,A$. In particular, the quantities acquired are: the input auxiliary voltage v_{AUX}, the bus rectified voltage across the electrolytic capacitor v_C, the exciter stator voltage v_{EXC}, the MOSFET drain-source voltage v_{DS} and the exciter stator current I_L.

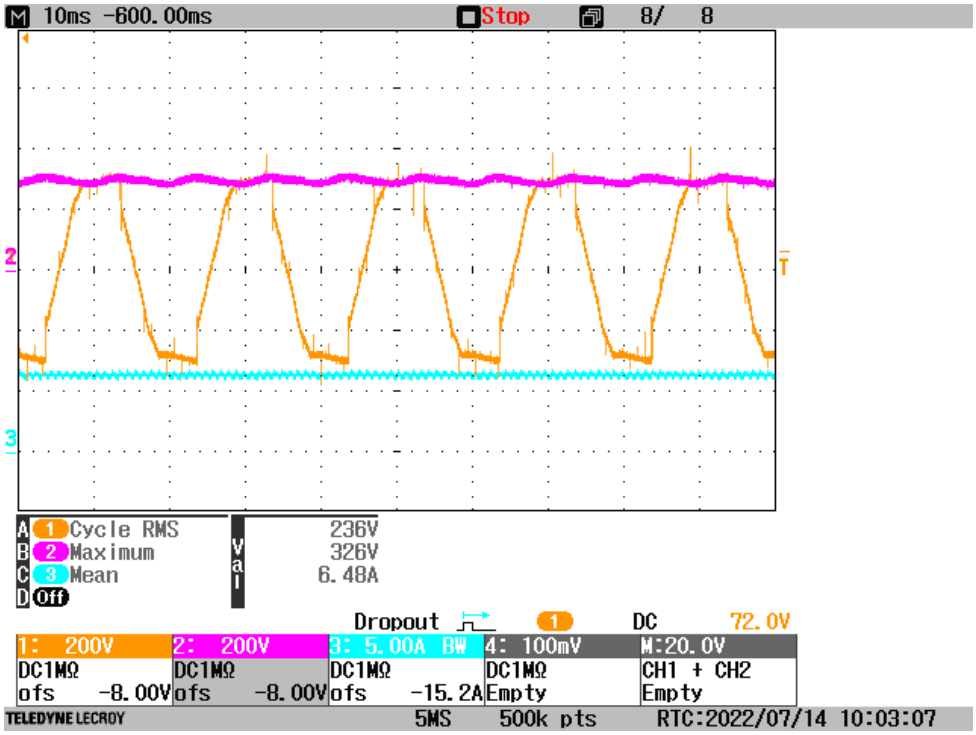

Figure 5.1.2: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

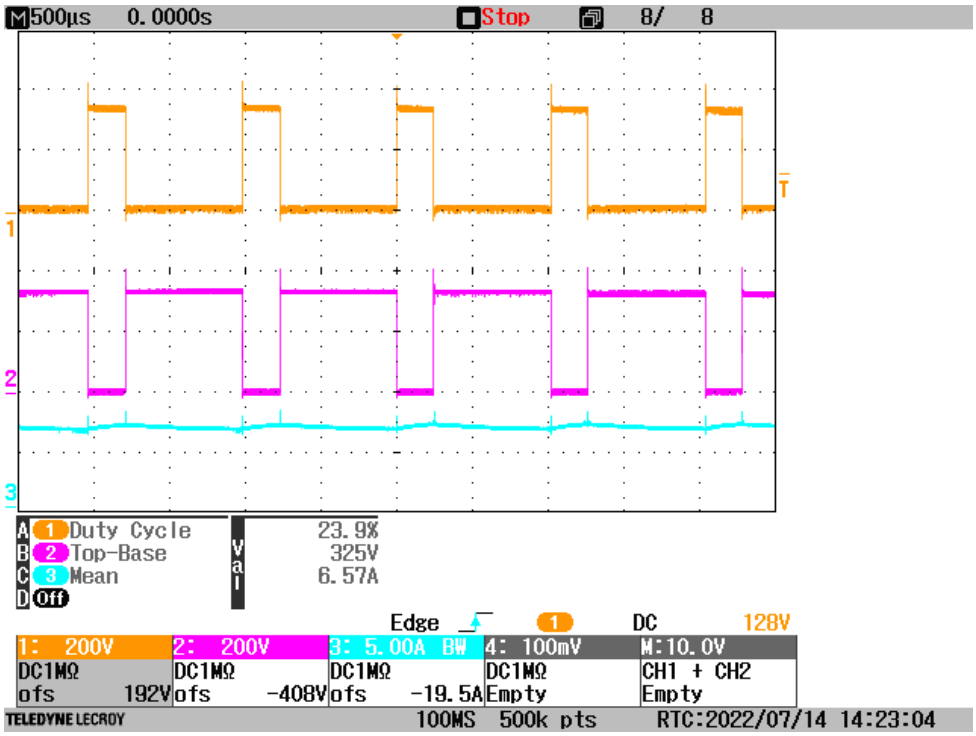

Figure 5.1.3: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

From the acquired waveforms it is possible to observe the correct circuit operation: the voltage pulses are "cut" from the input alternating voltage rectified by the electrolytic capacitor and applied to the exciter stator in a rectangular pulse train form defined by the 976 Hz PWM frequency.
One can notice the voltage spikes generated at the power switch turn-off are kept below maximum voltage ratings, thanks the presence of the turn-off snubber.
The absence of unexpected behaviours like voltage spikes exceeding devices ratings and projects specifications are the evidence of good excitation system operation.

It is possible to notice the desired 6.5 A inductive load current is achieved, from a 325 V peak sinewave ($\sqrt{2}V_{AUX}^{rms}$), applying a PWM duty cycle $d \simeq 0.24$. The reader can notice this duty cycle differs from the one theoretically computed during the MOSFET conduction losses discussion in Subsection 4.3.1, being 0.2. However, that computation was performed making a number of assumptions:

- ideal sinewave input waveform;
- no voltage drop on the diodes of the GBU4J silicon bridge rectifier;
- no MOSFET drain-source voltage drop during on phase;
- ideal voltage rectification to a constant value equal to the input sinewave peak;
- no stator exciter resistance increase due to Joule effect.

These aspects not accounted in the first theoretical duty cycle evaluation justify this difference. However, this gap is not critical because $d = 0.24$ keeps yet a large margin from the full $d = 1$ excitation system capability.

5.2 Test on real generators

Once checked the correct operation of the circuit on the test bench setup, the realized prototype is tested on real Mecc Alte generators. In particular, two models are chosen to perform such tests: the ECP4 2M4C[**35**] and the ECO38 1L [**34**] models. The reason is to be found in the willingness to check the circuit functioning on two very different machines from power generation, size and auxiliary voltage waveform points of view. In particular, the ECP4 model is a small 8 kVA power, 30 cm case diameter synchronous generator; the ECO38 14M C is instead a large 300 kVA power, 60 cm case diameter one. Since the proposed circuit should work on every generator model sold by the company, the demonstration of the correct circuit operation on machines which span almost the whole range of products power is a very important result to show in the thesis.

Even in this second test step the control of the output voltage is not performed by a closed-loop regulation. According to what said at the begin of this chapter, it is good practice to test a new developed solution one step at a time so to avoid potentially dangerous unexpected and undesired behaviours. For this reason, the regulation of the output voltage is yet performed acting on the potentiometer which controls the PWM duty cycle. The goal for these tests is to assess the correct operation of the machine and its excitation system in steady-state condition under different load situations. Independently if a load is connected to the generator or not, the voltage regulator objective should be the one to maintain the output phase-neutral voltage to $V_{PN}^{rms} = 230\,V$. For this reason, for each test the duty cycle is manually adjusted in order to achieve such voltage value. What is more an extra working situation is tested, that is the short circuit test.

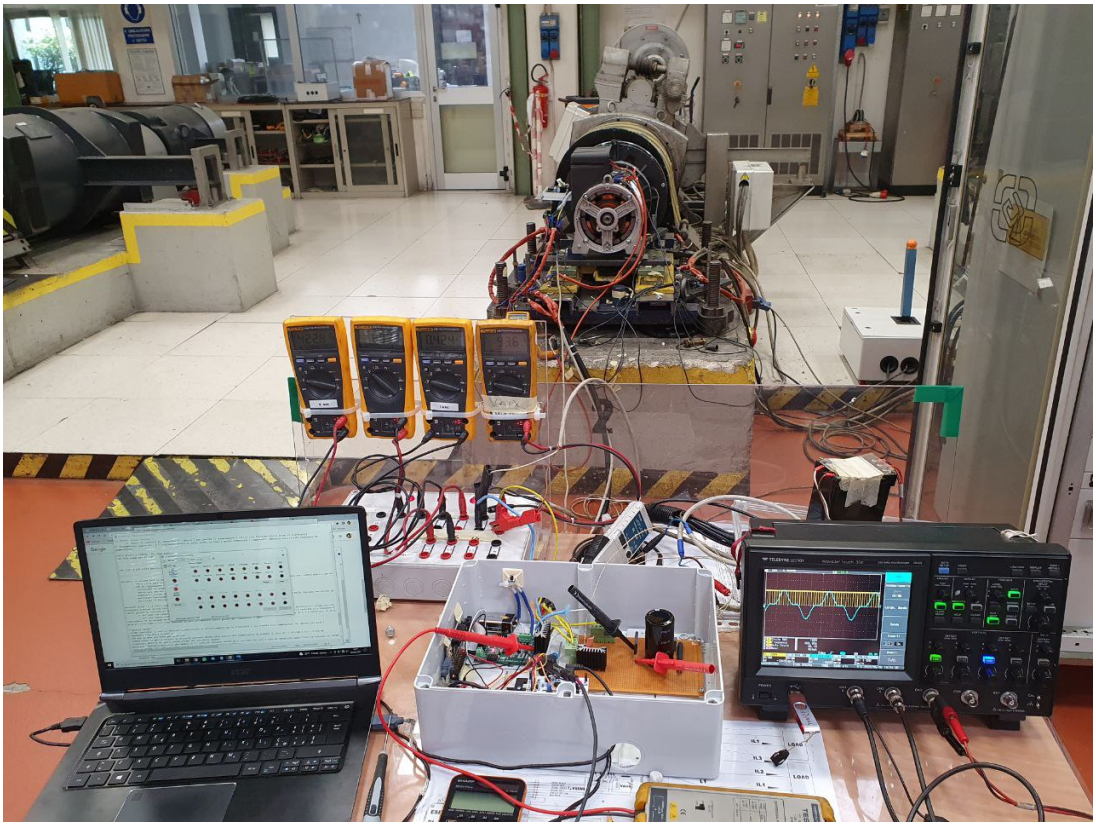

Figure 5.2.1: Setup for ECP4 2M4C model test.

Figure 5.2.2: ECO38 1L model tested.

5.2.1 Results on ECP4 model

Regarding the smaller machine, the tests are performed in five load situations: no load condition, purely resistive load ($cos\Phi = 1$), nominal load ($cos\Phi = 0.8$), purely inductive load ($cos\Phi = 0$) and short circuit.

No load From the measurement panel of the oscilloscope it is possible to notice the inductive load current required to achieve the nominal output voltage of 230 $Vrms$ is about 0.5 A, obtained by means of 5.2% duty cycle. For this small amount of current drawn by the inductive load the bus capacitor is able to rectify perfectly the auxiliary alternating voltage to a constant value equal to its peak. The non-ideal sinewave shape of the auxiliary voltage is due to the presence of third harmonic content.

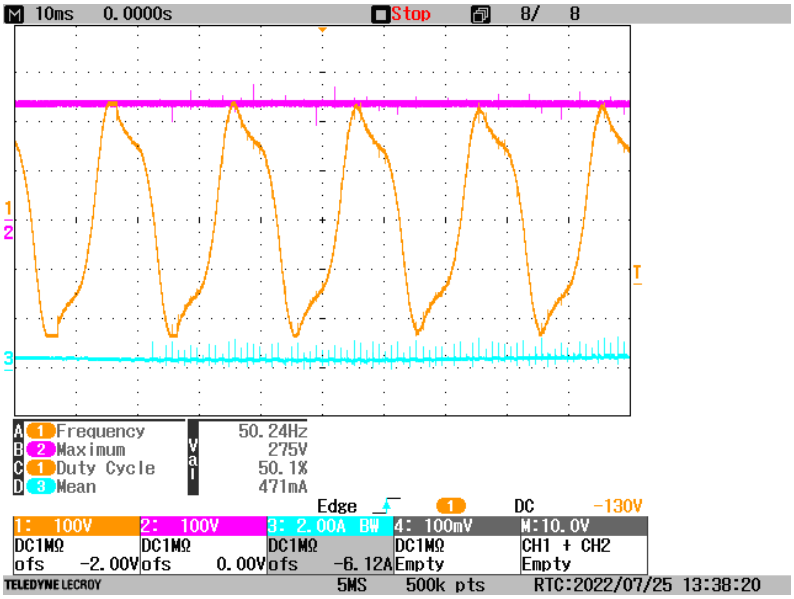

Figure 5.2.3: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

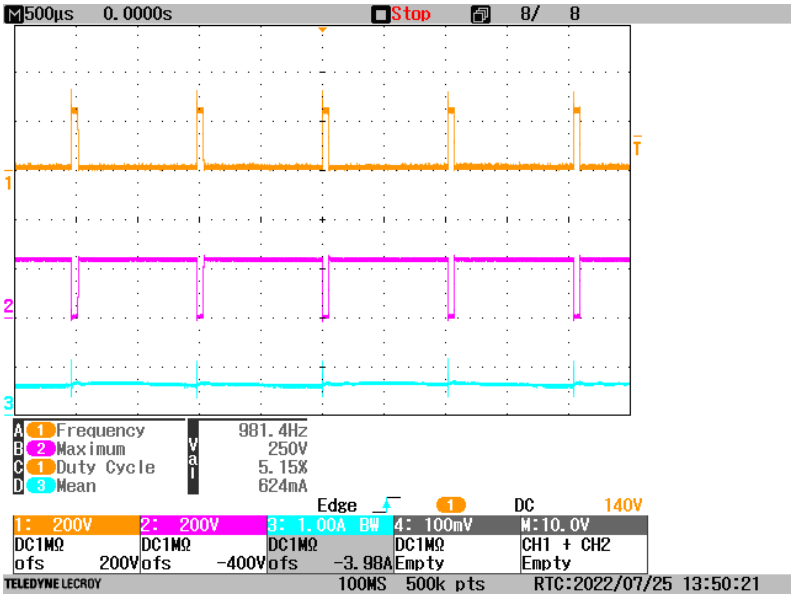

Figure 5.2.4: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Resistive load In these screenshots it is possible to appreciate the armature reaction effect: on one hand the resistive load has the effect to require more excitation current (consequently the inductive load current rises to about 1.2 A) to supply the load; on the other the auxiliary voltage gets distorted. The duty cycle, as expected, rises to about 6.3%.

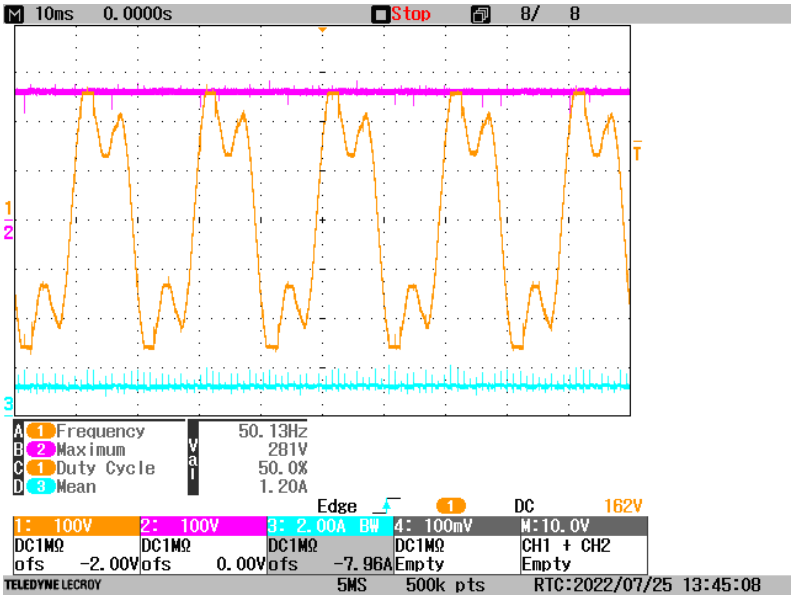

Figure 5.2.5: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

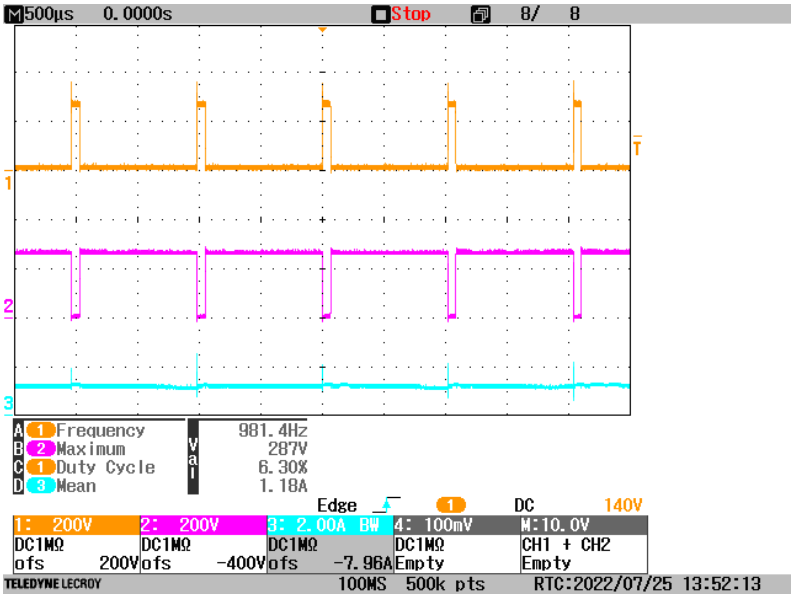

Figure 5.2.6: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Nominal load As regards the nominal load ($cos\Phi = 0.8$), like the purely resistive case, the effect of the load is to rise the required excitation current and distort the auxiliary voltage. As expected from armature reaction theory, the required current is higher than the purely resistive case (in fact it's about 1.7 A, obtained with 11.5% duty cycle).

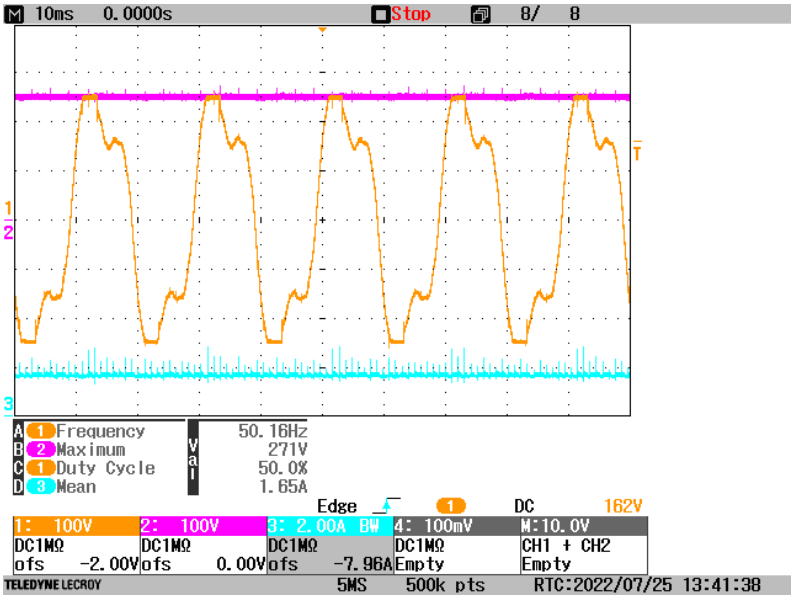

Figure 5.2.7: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

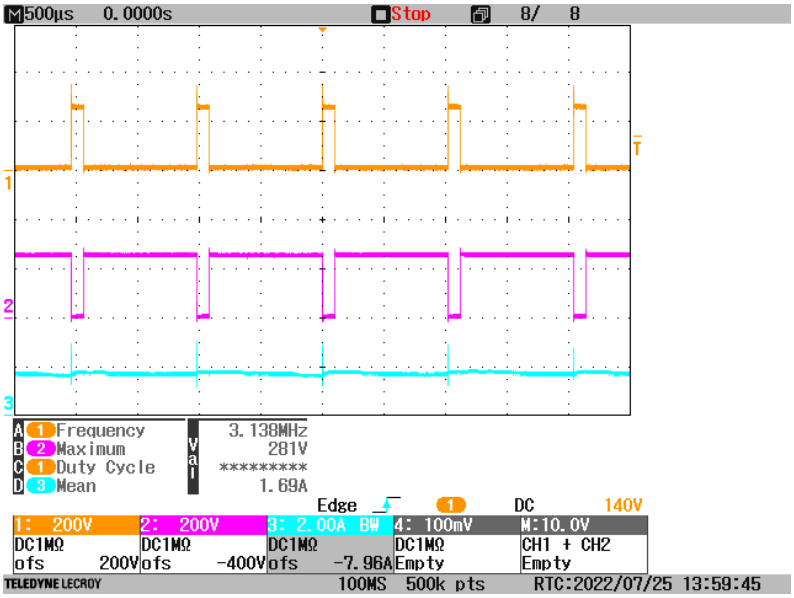

Figure 5.2.8: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Inductive load In testing the inductive load ($cos\Phi = 0$) situation, differently from previous loads, it is chosen not to reach the nominal current, but stop to $0.8 \cdot I_N$. This is a typical strategy used for inductive loads tests in order to avoid the exciter stator current to raise too much. For this reason, the levels of inductive load current ($1.3\,A$) and duty cycle (7.9%) are lower than the ones for nominal load. However, differently

from this strategy, the test of inductive load for the next model, in Subsection 5.2.2, is performed at 100% I_N.

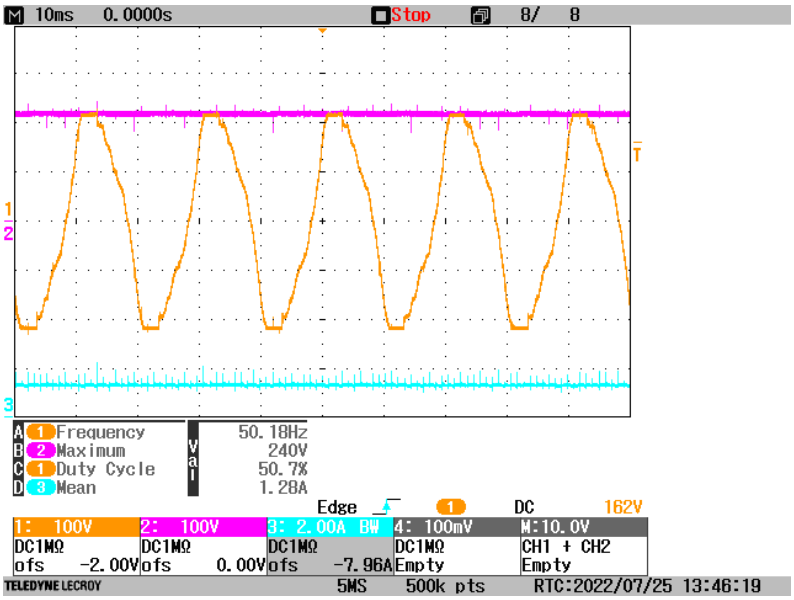

Figure 5.2.9: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

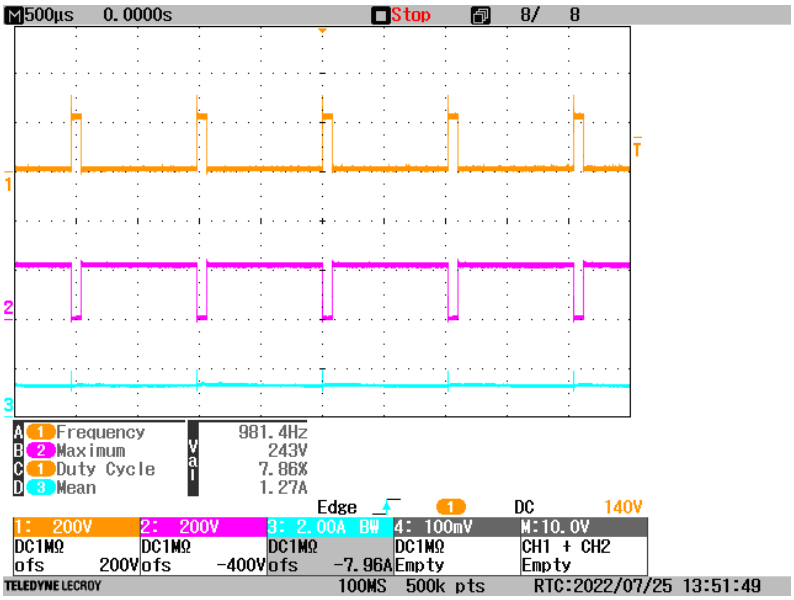

Figure 5.2.10: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Short circuit During short circuit test the goal is to check the excitation system capability to reach a short circuit current I_{SC} equal to at least three times the nominal current I_N. This test is performed on another model of the same ECP4 series, the 5M4C.

Knowing the nominal output power of the generator to be $P_o = 18\,kVA$, it is possible to obtain

$$I_N = \frac{P_o}{3 \cdot V_{PN}^{rms}} = \frac{18000\,VA}{3 \cdot 230\,V} \simeq 26\,A \tag{5.2.1}$$

During this test the PWM duty cycle frequency is adjusted acting on the potentiometer in order to gradually increase the short circuit current to reach $3I_N$ and beyond, up to the value obtained using 100% PWM duty cycle.

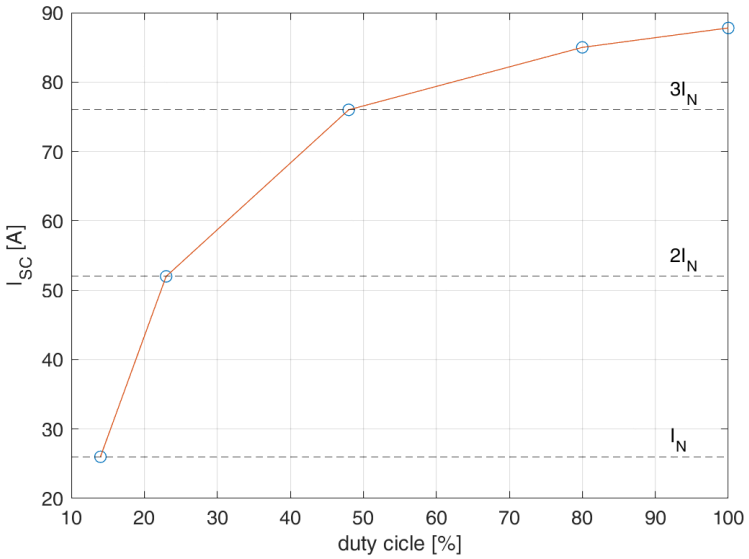

Figure 5.2.11: Short circuit I_{SC}-d characteristics.

The first noticeable peculiarity of this graph is its non-linearity. The short circuit current tends to stabilize as duty cycle is increased. This behaviour is due to the combination of two phenomena: the first is the magnetic saturation of the ferromagnetic core of the exciter generator; the second is the progressive bus electrolytic capacitor inability to keep a constant voltage at its terminals v_C due to the increase in the load current which discharge the capacitor faster.
From the above plot it is possible to observe the regulation required short circuit current $I_{SC} = 3I_N$ is obtained by means of 48% PWM duty cycle. At full duty cycle, which coincides with the always-on power switch condition, the maximum short circuit current is obtained, being $I_{SC,max} = 87.8\,A$ ($3.4I_N$).

A second interesting plot shows the exciter stator current vs duty cycle characteristics for the same key points considered in the previous plot. This way, it is possible to appreciate the required current through the exciter stator in order to reach output short circuit current levels of that order of magnitude.

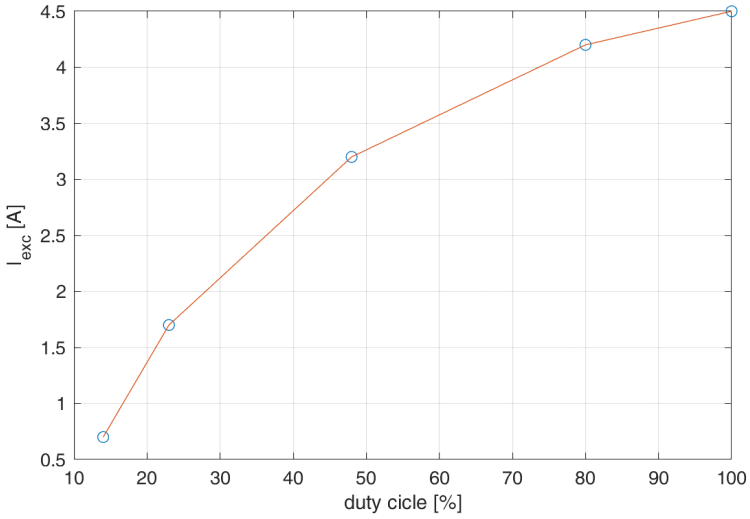

Figure 5.2.12: Short circuit I_{exc}-d characteristics.

It is possible to notice that, as expected, the short circuit test represents the most stressful situation for the operation of the designed circuit. In fact, the current through the inductive load is the highest achieved among all the possible working conditions the alternator can operate at.

5.2.2 Results on ECO38 model

On the larger machine the following tests are performed: no load condition, purely inductive load ($cos\Phi = 0$) and short circuit. Tests with other types of load are not performed because the much larger power involved in this machine would require the utilization of an energy recovery system. If on one hand this kind of system is actually available in the company lab, on the other hand a high voltage regulator stability is required. Because of the first prototyping stage of the circuit, the company considered better not to perform such kind of tests. However, the limited tests performed on this machine show the correct operation of the proposed circuit even on the ECO38 more powerful machine.

No load The no load nominal output voltage of $230\,Vrms$ is achieved from $I_{exc} \simeq 0.73\,A$, obtained from a duty cycle of about 3.6%. Even in this case it is possible to notice the rectified voltage v_C remains roughly constant due to the small amount of current through the inductive load.

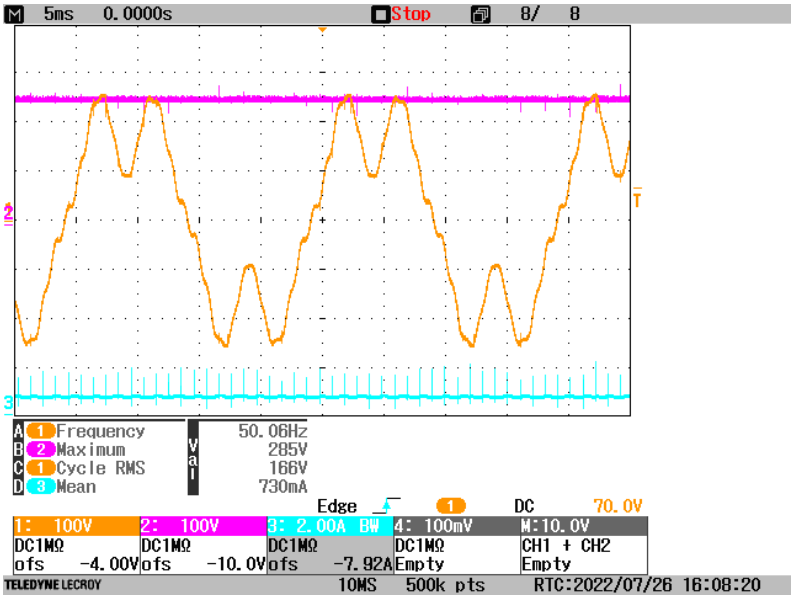

Figure 5.2.13: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

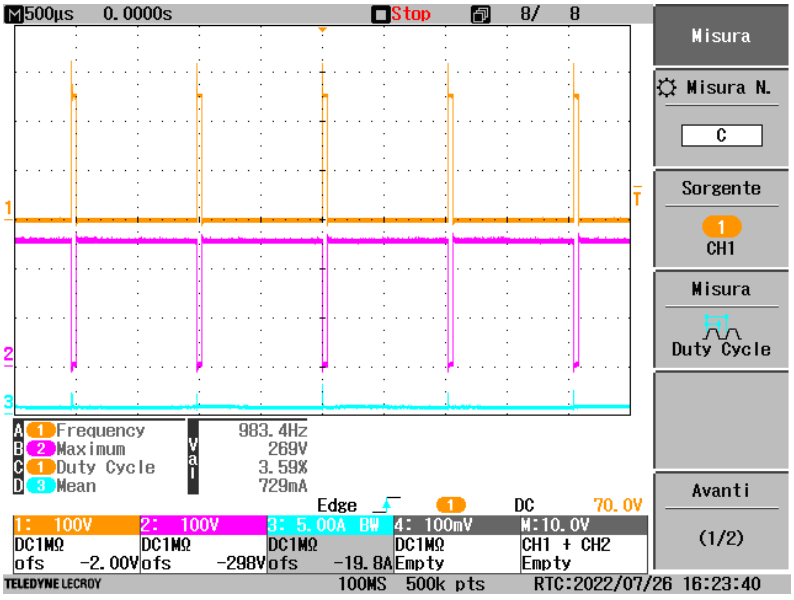

Figure 5.2.14: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Purely inductive load The purely inductive load test is interesting because many phenomena are observable simultaneously. First of all the distortion in the auxiliary winding due to armature reaction; secondly the raise in exciter stator current $I_{exc} \simeq 3.1\ A$, obtained by means of the larger $d \simeq 17\%$ PWM duty cycle; lastly the reader can observe a slight v_C oscillation, due to the charge and discharge of the bus electrolytic

capacitor, because of the higher level of inductive load current required.

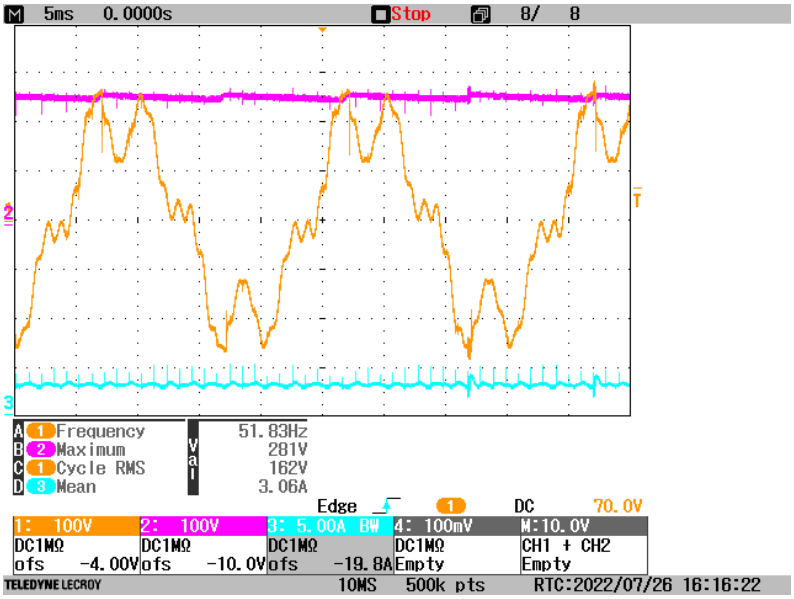

Figure 5.2.15: Oscilloscope screenshot. Ch.1: v_{AUX}; Ch.2: v_C; Ch.3: i_L.

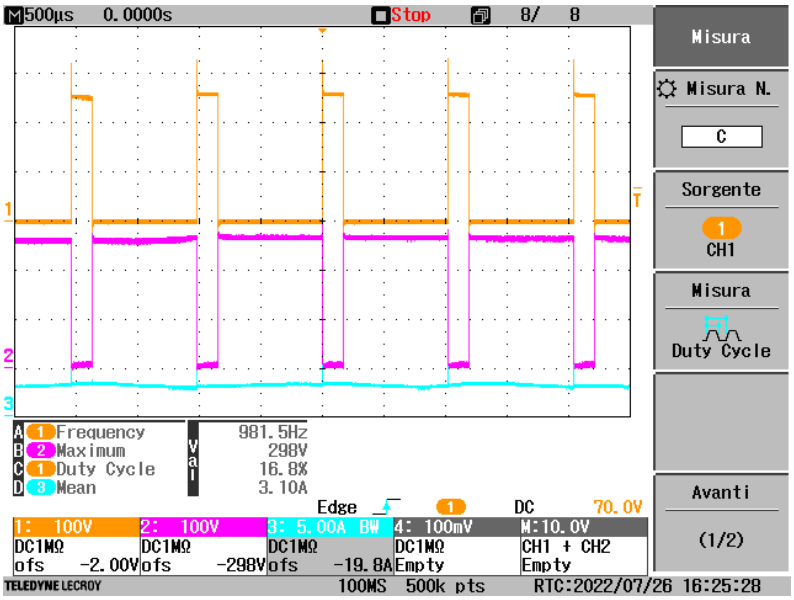

Figure 5.2.16: Oscilloscope screenshot. Ch.1: v_{EXC}; Ch.2: v_{DS}; Ch.3: i_L.

Short circuit As done for the previous model generator, the nominal value for the output current is firstly computed. From the nominal output power of the ECO38

1M4C, $P_o = 225\,kW$, the nominal current is

$$I_N = \frac{P_o}{3 \cdot V_{PN}^{rms}} = \frac{225000\,VA}{3 \cdot 230\,V} \simeq 325\,A \tag{5.2.2}$$

In the same way of the other generator model, the PWM duty cycle is adjusted in order to increase gradually the short circuit current. Let's recall this operation is done acting manually on the potentiometer. It's clear this operation takes some time, during which the flowing current heats up the stator windings. For this reason, in this test the achievement of $3I_N = 975\,A$ is avoided, since the time required to reach that value can result dangerously critical for the machine.

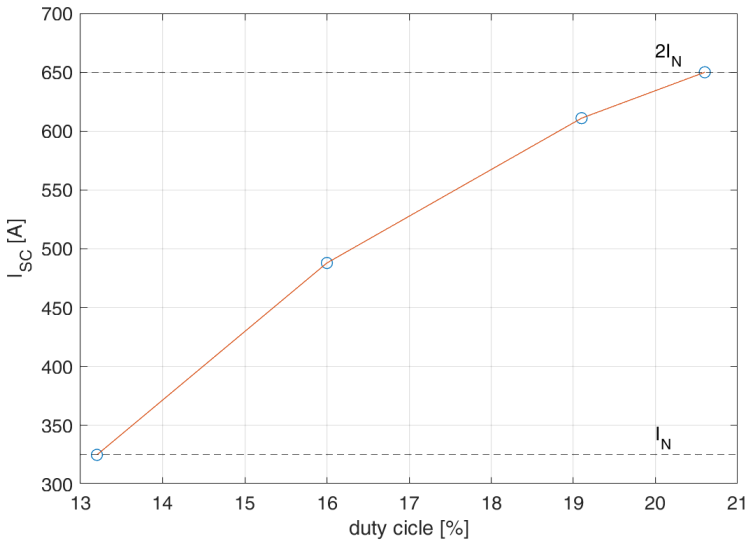

Figure 5.2.17: Short circuit I_{SC}-d characteristics.

In evaluating the short circuit characteristics of the machine stopping at $2I_N$ is considered appropriate not to overheat and damage the generator itself. However, it is already appreciable the same trend observed in the previously tested model: the short circuit current increases not proportionally with the duty cycle for the same reasons previously described.

In the same way as done for the ECP4 model, the relation between the exciter stator current and the duty cycle is plotted below.

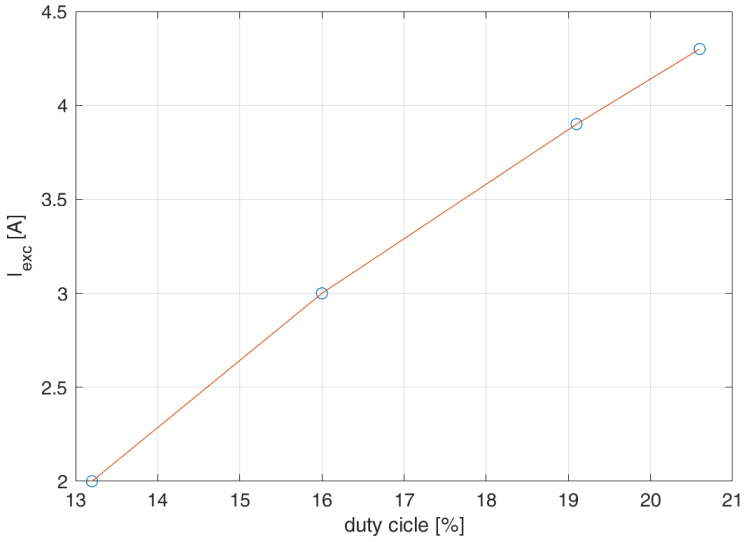

Figure 5.2.18: Short circuit I_{exc}-d characteristics.

Even in this case, as expected, the short circuit test represents the most stressful situation in which the designed circuit has to operate, due to the highest level of the inductive load current reached in this condition.

5.3 Test on generator excitation system dynamic response

The tests shown up to this point are focused on the assessment of the circuit correct behaviour under nominal and particular working conditions. For this purpose voltages and currents in the circuit are monitored in order to prove the correct operation of the proposed system by means of oscilloscope screenshots showing instant captures of different steady-state situations. These tests are performed in open-loop regulation: the output voltage is manually controlled acting on the power switch command PWM duty cycle in order to obtain the desired $V_{PN}^{rms} = 230\,V$.

At this point, after having proved the circuit is working properly, a step further can be done. Since the project developed is part of a voltage regulator, what would be actually interesting is to observe the circuit operating for what it is designed for. It is recalled a voltage regulator for an electrical generator has the purpose to maintain the output alternating voltage at a constant desired level, independently on the kind and amount of load connected to the machine. For this reason, it is interesting to observe the dynamic response of the excitation system obtained with the new designed circuit. Moreover, this section has also to be seen as a way to show the reader the designed

circuit is actually able to keep the output voltage to a constant level, aspect that up to now has been asserted, but not proven.

5.3.1 Closed-loop regulation

In order to observe the system dynamic response, a system which is responsible for automatically keeping the output voltage to the desired setpoint has to be implemented. In order to do so a closed-loop regulation is required. Here, the introduction of a negative feedback allows the output value to be continuously compared with the desired result; the control output to the process is modified and adjusted to reduce the deviation, thus forcing the response to follow the reference.

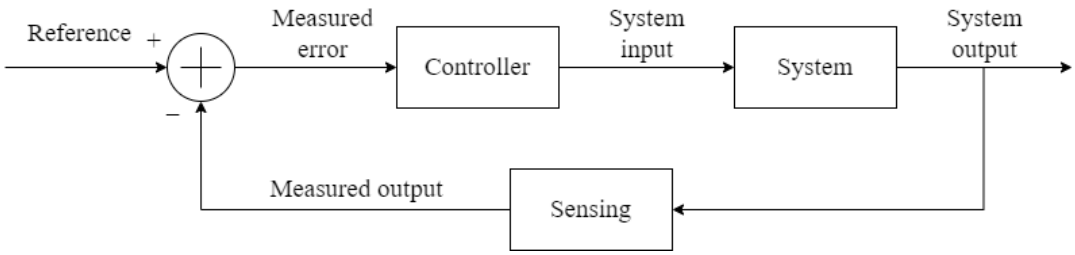

Figure 5.3.1: Block diagram of the negative feedback control system.

5.3.2 PID controller

The closed-loop regulation is implemented via a PID feedback control. The Proportional–Integral–Derivative (PID) controller is chosen because the most used in control systems, since simple and applicable even if a detailed model of the process is not known. Since even Mecc Alte itself uses this type of control in its regulators, it is considered appropriate to use the same kind of control loop feedback mechanism.

A PID controller calculates the error signal as the difference between the desired setpoint and the measured output variable and applies a correction based on the past control error (integral term), the present control error (proportional term) and the future control error (derivative term). If $u(t)$ is the control signal sent to the system, $y(t)$ is the measured output, $r(t)$ is the desired output and $e(t) = r(t) - y(t)$ is the tracking error, the PID controller algorithm has the form

$$u(t) = K_p\, e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{5.3.1}$$

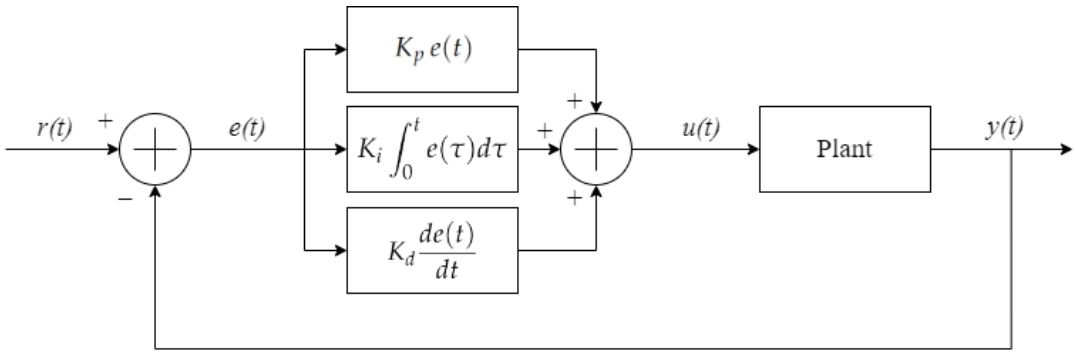

Figure 5.3.2: PID controller block diagram.

The desired closed-loop dynamics is obtained by adjusting the three parameters K_p, K_i and K_d. Qualitatively speaking stability can often be ensured using only the proportional term. The integral term allows disturbance rejection and the elimination of the steady-state error. The derivative term is used to improve stability providing damping or shaping of the response. In order to discuss how these parameters are found, a step back is needed.

As typically done nowadays, the regulation task is completely digital. A microcontroller is programmed to perform the output value sensing, the comparison with the setpoint, the run of control algorithm and the output signal generation. For this reason, a more accurate representation of the closed-loop system would be the sampled and quantized version of the block diagram shown in Fig. 5.3.1.

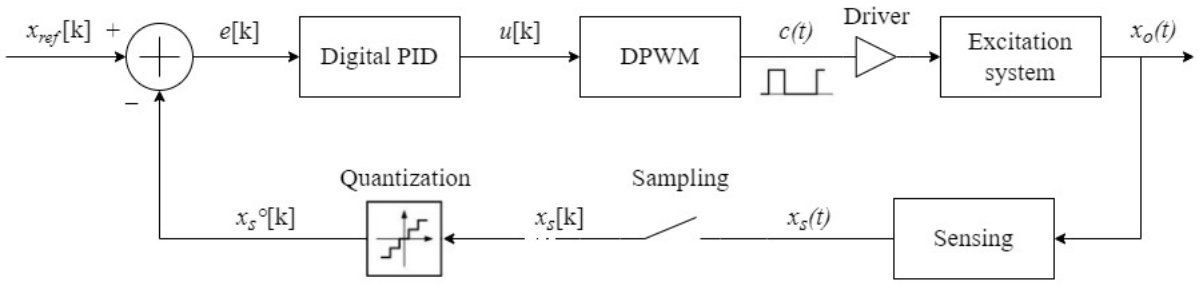

Figure 5.3.3: Block diagram of the digitally controlled excitation system.

In this thesis this task is again assigned to the Arduino Uno microcontroller board. For this reason, differently from the analogue case, control quantities are sampled and

quantized. The continuous sensed signal $x_s(t)$ is sampled and quantized by the Arduino ADC to generate the sequence $x_s^\circ[k]$. From the comparison with the setpoint variable internally generated in the Arduino, the error quantized sequence is the input for the digital PID compensator. The digital output signal is the input for the Arduino digital PWM generator, which produces a PWM signal having discrete duty cycle levels. This signal is eventually applied to the gate driver chip.

In typical academic exercises the three PID parameters are computed from the s-domain (or in this case z-domain) transfer function model of the open loop system. However, in this application the system is extremely complex and the transfer function of the excitation system is not simple to evaluate. For this reason, the PID controller is suitable for this application: K_p, K_i and K_d can be empirically set without specific knowledge of the system model, iteratively tuned on the base of experimental tests.

Sensing circuit In order to implement the closed-loop control the output regulated variable has to be read by the Arduino board. Clearly the output phase-neutral alternating 230 *Vrms* desired voltage has to be manipulated in order to be manageable by the Arduino board. This task is performed by a specific circuit.

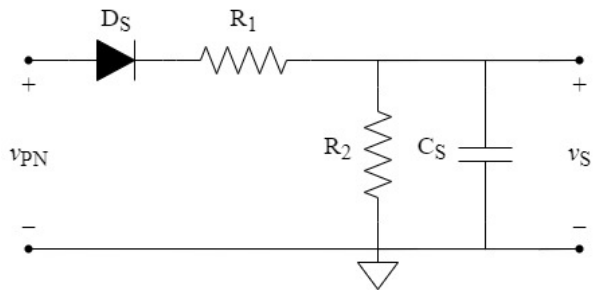

Figure 5.3.4: Sensing circuit.

The regulation is based on one phase voltage. In particular, the waveforms peaks are considered: the diode D_S filters only positive half-waves of phase-neutral voltage sinewave v_{PN} and the voltage divider R_1-R_2 scales down the voltage to manageable levels for the Arduino ADC. Assuming v_{PN} to be an ideal sinewave, the resistors are chosen so to match the desired peak $V_{PN} = \sqrt{2}V_{PN}^{rms} = \sqrt{2} \cdot 230\,V \simeq 325\,V$ with the half of the ADC input voltage $[0\,V,\, 5\,V]$, being $V_{S,half} = 2.5\,V$.

$$v_S = \frac{R_2}{R_1 + R_2} v_{PN}^+$$

$$V_{S,half} = \frac{R_2}{R_1 + R_2} V_{PN} \rightarrow R_1 = \left(\frac{V_{PN}}{V_{S,half}} - 1\right) R_2 \simeq 129 R_2 \tag{5.3.2}$$

It is convenient to select large resistance values so to minimize the current drawn by the sensing circuit. For this reason, $R_1 = 1\,k\Omega$ and $R_2 = 129\,k\Omega$ are chosen. Lastly a small $1\,nF$ ceramic capacitor is placed in parallel R_2 so to smooth potential noise in the sensed signal.

Controller algorithm At this point, the microcontroller algorithm performs a sampling at $10\,kHz$ rate of the handled output signal, thus providing 100 samples for each $10\,ms$ half-wave. For every time-window of $20\,ms$ the maximum sample value is selected and used as the measured output to be subtracted to the reference value to generate the error signal to be sent to the PID algorithm.

The proportional part is simply obtained as error $e[k]$ times the proportional constant:

$$u_P[k] = K_p \cdot e[k] \tag{5.3.3}$$

The integral part at iteration k is obtained as the sum of the error times the integral constant with the past iteration error:

$$u_I[k] = K_i \cdot e[k] + u_I[k-1] \tag{5.3.4}$$

The derivative part is computed as the product of the derivative constant with the rate of change of the error:

$$u_D[k] = K_d \cdot \frac{e[k] - e[k-1]}{t[k] - t[k-1]} \tag{5.3.5}$$

5.3.3 Results on dynamic response at generator load connection

The tests on the dynamic response of the excitation system, utilizing the MOSFET-based output stage of the voltage regulator and the PID control above described, are performed on the ECP4 generator model. The dynamic response wished to observe is the step response due to a load connection. As previously explained, the connection of a load to a generator, depending on its electrical nature (resistive, inductive, capacitive) and on its amount (the current involved) induces a variation on the generated voltage due to armature effect. The following acquisition shows the time evolution of the output RMS voltage and the error signal following to the connection and disconnection of a nominal resistive load, meaning the load is a resistor which absorbs the machine nominal current of 26 A.

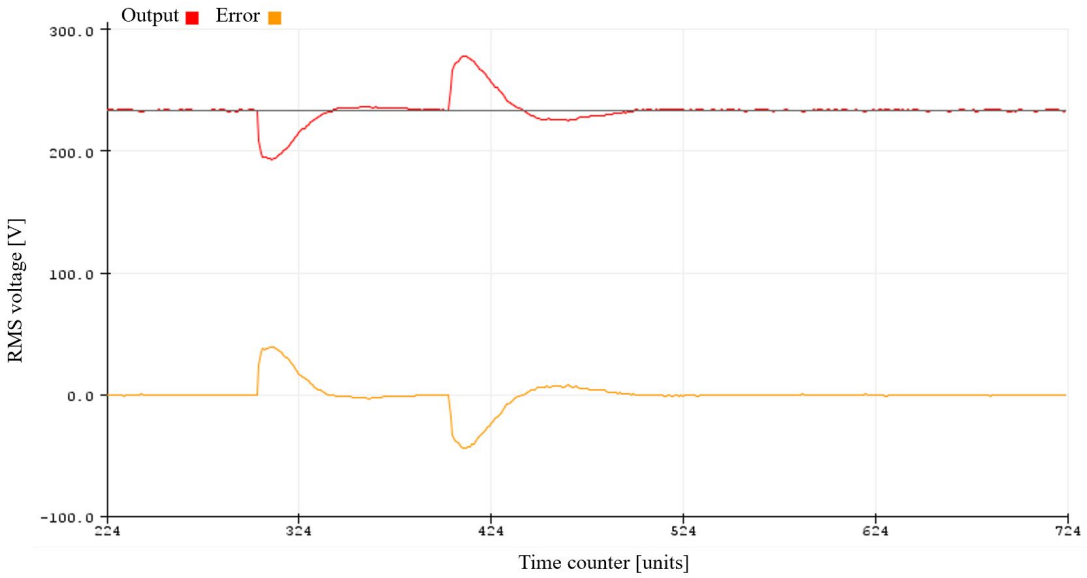

Figure 5.3.5: Time evolution of the output RMS voltage and error signal at load connection and disconnection.

This result is obtained after a series of attempts, in the choice of the three PID gains, which are aimed at reducing the maximum voltage variation at a connection/disconnection event, reducing the transient recovery time and avoiding excessive overshoots or oscillations in the regulated variable. In particular, the above results are obtained with the following parameters combination: $K_p = 0.095$, $K_i = 0.02$, $K_p = 0.04$.

Nevertheless, the reader should consider this thesis does not focus on the control side of the voltage regulator: the control algorithm and implementation of the closed-loop regulation represent a marginal topic in the thesis discussion, whose core and focus is instead the hardware power electronic design of the regulator stage which deals with the voltages and currents of the synchronous generator excitation system. The presence of this paragraph within the chapter regarding the thesis' results is due to the interest and curiosity in the realisation of a full-working voltage regulation: even if simple, the student and the reader may appreciate the operation of an overall regulator. Moreover, the development of the closed-loop regulation allows to prove the output voltage is actually kept at a constant desired level (in steady-state) using the developed circuit.

Despite the basic version of the control algorithm implemented, it is possible to assert the dynamical response results obtained are quite positive. In fact, the output voltage maximum variation at a load connection/disconnection event is kept within the limits of the legislation, which is the 20% of the nominal value. The minimum voltage value reached after the nominal load connection is about 195 V, correspondent to

a variation of the output voltage of 15.2%. The maximum voltage value reached after nominal load disconnection is about 275 V, correspondent to a variation of the output voltage of 19.6%.
Moreover, transient recovery time results quite low too. Considering the delay imposed in the *loop* function of the Arduino, a time division, composed of 100 units, corresponds to 4 seconds. Consequently, the transient recovery time observable for both events is about 1.5 s. Notice these results are obtained from the step response of a nominal load. For lower loads the maximum variation in the regulated variable and the transient recovery time are smaller.

Chapter 6

Conclusions

This thesis, result of the internship in the company Mecc Alte SpA, develops an investigation on the possibility to modify the output power stage of the voltage regulator used on the company products, synchronous generators. In particular, the company's desire is to develop a version of such output stage which relies on a both turn-on and turn-off controllable silicon power switch, like a power MOSFET or IGBT, instead of the currently used thyristor, because some advantages in the excitation system control are expected.

However, this power switch substitution brings some issues, the main one being related to the combination of the high switching capability of these devices with the inductive nature of the generator itself. For this reason, a long process of research, which starts from project requirements, passing through analytical study of the problem, components selection and sizing, software simulations, solution proposals and explanations of their criticisms, up to the final proposed solution, develops and illustrates the electronic design of the new output stage circuit of the voltage regulator. This circuit accomplishes the actual goal of the thesis.

Because of primary importance in power electronic design, an entire chapter was dedicated to power losses computation. This discussion led to a comparison between the old and new output stage versions regarding the needed heat sinks to pull over the power devices.

Once the circuit is defined and simulated, a real prototype is realized and tested. At a first stage a dedicated test bench is developed and exploited in order to assess the correct circuit operation. At a second stage the circuit is tested on two real Mecc Alte machines, before in open-loop and then in the closed-loop configuration. In order to perform the closed-loop regulation a simple microcontroller firmware is programmed and tested on a real generator.

The results outlined in Chapter 5 prove the developed circuit is able to perform the correct synchronous generator output voltage regulation. Consequently, it is possible to assert, at the end of this activity, the thesis's project goal's achievement.

In addition to this, perhaps the most important aspect the company is interested in is the performance/cost tradeoff comparison between the current circuit topology and the new proposed one. In order to provide a critical answer to this, a list of points summing up the advantages and disadvantages of the new proposed circuit is presented below.

Advantages

- The possibility to control also the turn-off transition of the power switch allows the utilization of a diode bridge to rectify the auxiliary supply waveform. This is a significant advantage because it is possible to avoid problems related to non-idealities in the auxiliary waveform. Extra zero-crossings and large third harmonic amplitude which downs the voltage below zero make the synchronization task, needed to use the thyristor, much more complex. On the contrary, both the turn-on and turn-off controllable power switch allow the simpler PWM control technique, which has the advantage that no syncronisation is no longer needed.

- The presence of the diode bridge allows to exploit also the energy contained in the negative half of the auxiliary supply alternating waveform. This way, it is possible to enhance the current made flown in the inductive load considering the same auxiliary voltage, or to obtain the same needed inductive load current from a lower amplitude auxiliary supply (more realistic scenario). In regards to this advantage, it is possible to imagine to design less demanding generators auxiliary winding in terms of voltage needed to be generated, an advantage for the company.

- The auxiliary voltage rectification, in combination with the power switch PWM command realizes a better regulator stability. In fact, in case of high load the auxiliary voltage rises. The enhancement of the voltage rate of change around zero crossings represents an issue for the thyristor-based topology. A very large current gain VS trigger angle presents. It is clear with this high slope of voltage a small variation in the command trigger angle results in a large voltage pulse amplitude variation and eventually a large inductive load current variation.

- The use of a power MOSFET gives the possibility to untie from the $50\,Hz$ auxiliary waveform frequency. The PWM control signal frequency can be chosen

higher so to have an improvement in the regulation velocity, in addition to reducing the inductive load current ripple, so as to have a more constant magnetic flux generated by the exciter stator.

Disadvantages

- The proposed circuit to achieve the output stage of the voltage regulator surely involves an higher cost. The power MOSFET is more expensive than the thyristor and the presence of additional circuit components like the diode bridge and the aluminum electrolytic capacitor represents the first and main disadvantage of this new circuit proposal.
- Regarding thermal considerations, it is evinced the proposed circuit involves the need of more performing heat sinks. More than the cost of the component itself, the main issue is the larger space occupied by a larger heat sink on the PCB. However, from calculations performed in Chapter 4, it has been shown there is not a significant difference in the needed heat sinks (roughly 20% of thermal resistance less in the case of the MOSFET-based circuit).

Finally, possible future developments of this project are presented below:

- The development of the output stage of the voltage regulator can proceed in the choice of a better suited gate driving circuit for this application. In fact, the circuit proposed in this thesis uses a galvanically isolated gate driver with advanced protection, configuration and diagnostic features. These properties are desired during the first development and prototyping stage, but not actually required in the ultimate product. In the gate driving circuit design, one should consider the use of either discrete components (like two BJTs in push-pull configuration) or specific integrated circuits. The choice depends both on operation considerations, like functionalities required, and on industrial considerations, like cost and suppliers availability.

  When it comes to the gate driving strategy, another possible solution for handling the auxiliary inductance current switch issue, not assessed in this thesis, could be to control appropriately the gate input signal to force the power switch to turn off slower than its maximum capability. If on one hand it is true switching capabilities of the power MOSFET or IGBT are not exploited at maximum level, on the other slowing down the device current drop at turn-off would induce a smaller and longer voltage spike on auxiliary inductance terminals (similar to

the thyristor case), more manageable by the power switch, avoiding the use of the large electrolytic capacitor. The main drawback of this strategy is switching losses enhancement, which could become equally as problematic as the auxiliary inductance issue: appropriate counter measures should be taken, for instance the use of much larger heat sinks. However, it is believed it's worth to investigate also this idea, because an optimum trade-off between turn-off rate and switching losses may be found.

- Following in the project development flow is the realization of a PCB for the proposed power stage of the voltage regulator, including on a single board the gate driver, the power switch, the diode bridge and so on. This allows to shorten as much as possible components connections, useful to minimize undesired non-idealities due to practical realization of the circuit, first of all stray and leakage inductances. In this way, by means of a second test session, some circuit components, whose purpose is to compensate for these non-idealities, could be possibly resized (for example the MOSFET snubber capacitor).

- An aspect not addressed in the design of the output stage of the voltage regulator is the circuit for regulator supply. A not obvious point for the reader is that power supply for regulator operation is not provided by the main grid like done in this thesis, but, on the contrary, by the generator produced energy itself. The reason is quite simple: one must remember Mecc Alte generators are mainly employed in gensets, so typically where main grid supply is not available. During genset start-up a residual voltage is induced on the main stator windings and in particular on the auxiliary winding (due to residual magnetization of the main rotor electromagnets according to magnetic hysteresis loop), accounting to roughly 15 $Vrms$ at engine speed. Starting from this low supply, the regulator must begin to operate as soon as possible. There are two strategies to perform this task. The first is to design the regulator so that the control stage is able to be supplied directly from the low residual voltage, not a easy task. The second is self-ignition: the residual voltage supplies a pure analog circuit which forces the power switch to conduct in an uncontrolled manner. This way, a positive feedback is established in the excitation system, which enhances quickly the excitation current and the output voltage. At this point, it is easier to supply the regulator, which however, is required to begin regulating very fast.

- Once the new power stage of the voltage regulator is designed, the focus can shift to the control stage. In this regards the microcontroller firmware including the

functional and protection features has to be developed. In particular, the most important part consists in programming an appropriate regulation algorithm, which typically is a PID regulator. As a matter of fact a simple well-working PID firmware has been implemented for this thesis. However, a better one, possibly able to exploit the higher switching frequency at which the power switch of operated, can be written.

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