UNIVERSITA' DEGLI STUDI DI PADOVA

FACOLTA' DI INGEGNERIA

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

Corso di Laurea Specialistica in Ingegneria Elettronica

TESI DI LAUREA

CHARACTERIZATION OF ESD PROTECTION STRUCTURES FOR 65 nm CMOS TECHNOLOGY

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Anno Accademico 2009-2010

To my parents

Abstract

ESD phenomena are well known to be extremely dangerous for microelectronic devices. This thesis deals with failures induced by ESD phenomena, starting from the description of main charging events up to the physics beyond the operation of different devices under high current regime. Novel implementations developed in the last years to increase the devices behavior under ESD event was introduced.

How to recreate in laboratory ESD-like events it is also shown, with the description of fundamental test models used to define the sensibility of electronics devices. Providing certain and repeatable results, these models permit to compare several devices under equal conditions and to design better devices in future, less dependent on ESD problems. In particular it was analyzed the TLP method that, in the last years, became the standard testing methodology in the semiconductor industry because, looking at the HBM qualification test of the product, a TLP pulse with a width of 75 ns equals the HBM typical pulse energy with decay time of 150 ns. For this method was described operational principle, fundamental implementations and issues.

ESD protection elements and metal lines of PCM for 65 *nm* CMOS technology are investigated with DC and TLP-TDR (in 100 ns TLP pulsed regime) measurements. About DC measures, it was realized a LabView program to automate the process with the parameter analyzer HP 4145B. For every kind of structure it was obtained current and voltage failure values and an analysis of extracted values was made. A measurement of leakage current for protection structures under TLP-TDR test allowed to evaluate their robustness and degradation, showing in some cases the presence of soft failure or continuous increase in leakage current value (sign of the device degradation).

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Introduction

Everybody has observed in his life an electrostatic discharge events as the lightning. This one is the most common and powerful ESD event in the world, but to many people static electricity is little more than the shock experienced when touching a metal doorknob after walking across a carpeted room or sliding across a car seat. The visible spark is the result of the ionization of the air gap between the charged human body and the zero-potential surface of the doorknob. Clearly a high voltage discharge takes place under these circumstances with highly visible (and sometimes tangible) effects. Historically the knowledge of electrostatic discharge (ESD) phenomena can be ascribed at the Greek empire, when Thales of Miletus noticed the attraction of strands of hay to amber, leading to the coining of the word ‘‘electron’’. Static electricity has been a problem for centuries. For example in the 1400s, in European and Caribbean forts were used static control procedures and devices to prevent electrostatic discharge ignition of black powder stores. Only in the 1700s the guiding of electrical discharge was of interest to Benjamin Franklin, with the invention of the lightning rod. The lightning rod was the first effort to guide the electrical discharge current of a lightning strike in a direction that would not harm structures. With the industrialization the ESD problems increased and some solution was created. For example, by the 1860s, paper mills throughout the U.S. employed basic grounding, flame ionization techniques, and steam drums to dissipate static electricity from the paper web as it travelled through the drying process. The age of electronics brought with it new problems associated with static electricity and electrostatic discharge. In particular, as electronic devices became faster and smaller, their sensitivity to ESD increased. So today, in semiconductor chips, ESD protection structures have the same role of lightning rod in 1700s: to guide the current through a semiconductor chip to prevent the failure of circuits and the semiconductor chip. Anyway, despite a great deal of effort during the last decades, ESD events still affect production yields, manufacturing costs, product quality, product reliability, and profitability.

After a brief introduction about ESD phenomena and fundamental models used to test devices under their effects, the most common devices operating as protection structures will be presented in Chapter 2 (diode, SCR and MOSFET). For each device will be shown some novel implementation developed in the last years to increase its behavior under ESD event. In Chapter 2 will be also analyzed failure mechanisms and their damages into integrated circuits.

In Chapter 3 will be introduced the most common measurement setup used to recreate in laboratory an ESD-like event: the Transmission Line Pulser. For this method will be also described the operational principle and issues related to its implementation and measure process. In particular, for their importance in characterization of ESD protection structures, it will be analyzed the measure of leakage current and the calibration of measure system. Furthermore it will be studied the correlation of TLP with other ESD test methods, in particular the HBM and CDM models.

In Chapter 4 it will be presented the LabView program realized to automate the measure process with the parameter analyzer HP 4145B, used to obtain DC measurement of protection structures studied. A brief description of other LabView VI used for TLP-TDR system will be made at the end of chapter.

In last chapter it will be shown the characterization activity carried on different protection structures (RF diodes, MOSSWI, SCR) and metal lines, for PCM in 65 nm CMOS technology. This work is related to the project “Characterization of ESD protection structures in NVM sub-micrometrical processes” between ST Microelectronics and the Microelectronic group of University of Padova, Department of Information Engineering.

Chapter 1

Electrostatic Discharge: Fundamentals and Models

Electrostatic discharge is defined as the rapid transfer of charge between bodies at different electrical potentials. It appears as a shock, result of discharging of a body accumulated charge through a conductive object (spontaneous high-current impulses with a duration in the range of 1 ns to 100 ns). The effect of this shock can induce different effects. In fact even if the discharge of our body capacitance at several kV via a low resistive path is recognized just as some discomfort, the voltage drop across a 2 Ω power bus of a 0.13 µm CMOS device (designed for an operation at 1.2 V) may well exceed 20 V, putting the ultra-thin gate oxides at severe risk [1]. Before thinking through this phenomenon in semiconductor devices, a brief review of static electricity is necessary.

1.1 Static Electricity: Creating Charge

Static electricity is the creation of electrical charge by an imbalance of electrons on the surface of a material which produces an electrical field. This imbalance of electrons produces an electric field that can be measured (according with Coulomb's law) and that can influence other objects at a distance. In particular the electrostatic voltage resulting from the separation of charge is the driving force for the discharge current.

Basic mechanisms to generate electrostatic voltages are triboelectric charging, ionic charging, direct charging, and field-induced charging. Differently to first two mechanisms, that are slow processes, the current impulses of the latter two depend on the impedance of the charge path. A brief description of these mechanisms is now presented, beginning with the most common case: triboelectric charging.

1.1.1 Triboelectric charging

This mechanism results from the mechanical contact and separation of two surfaces with different electron affinity. As shown in figure 1.1, before contact, the two materials consists of atoms with equal numbers of protons and electrons, so both materials are electrically neutral. When the two materials are placed in contact and then separated, negatively charged electrons are transferred, in first approximation, to the surface of the material with the higher affinity. Gains electrons will depend on the nature of the two materials, as shown in following table (*FIG. 1.2*) (named *triboelectric series table*) for some typical materials. In particular, in a triboelectric charging event, the object that is closer to the top of the table takes a positive charge and the other one takes a negative charge. In addition, materials that are further apart on the table generate higher charge than those that are closer.

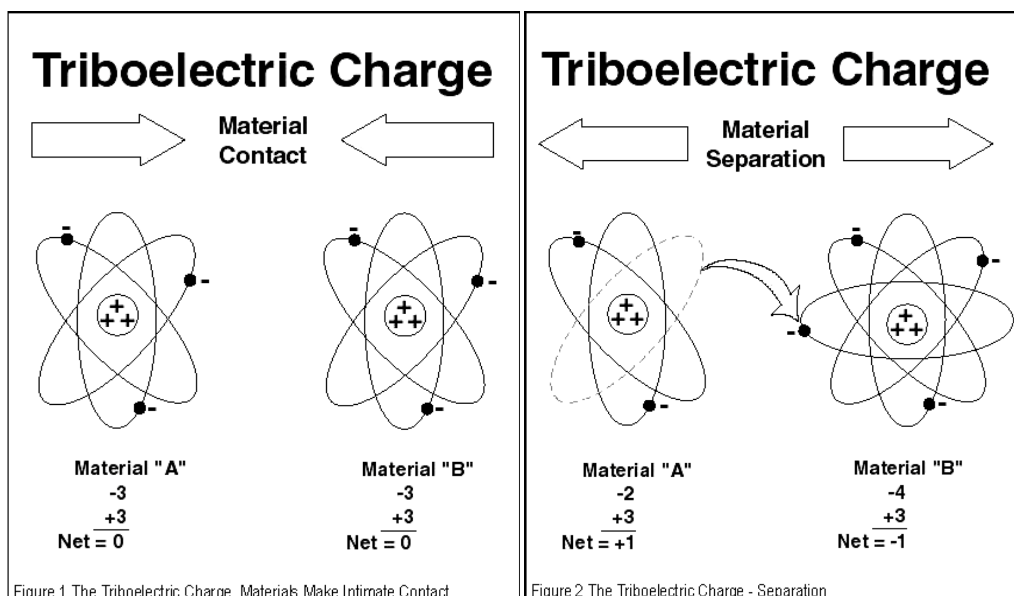


FIG. 1.1 Triboelectric Charge: contact and separation

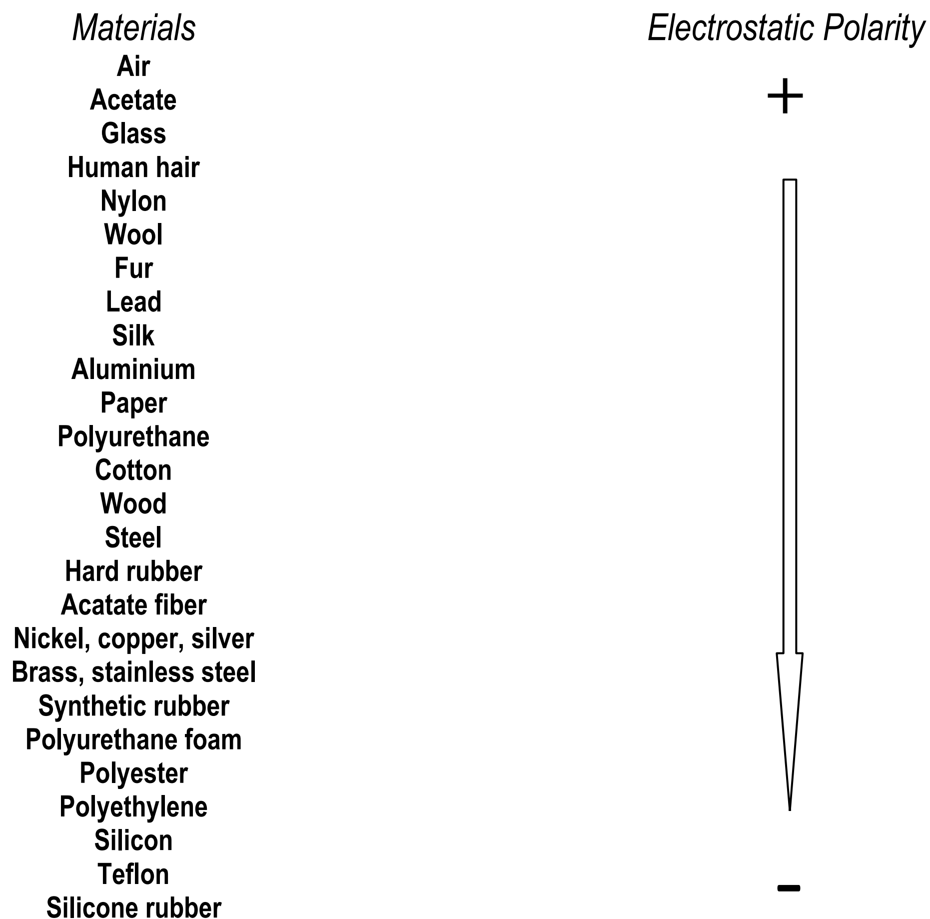


FIG. 1.2 A typical Triboelectric Series

If the charges cannot immediately recombine, additional instances of contact and separation increase the amount of charge, which builds up a higher voltage. More rapidly occurs the separation of the objects, less are the chances to have a recombination. Other factors that have a significant influence on the static charge are:

- Contamination of the surface
- Relative humidity
- Temperature of the surface contact
- Roughness of the surface contact
- Pressure of the surface contact
- Electrical characteristics of the material

Humidity, in particular, increases the surface conductivity, raising the rate of recombination. For example the data of electrostatic charge generation in workplace are shown [2].

Motion	Electrostatic potential at relative humidity	
	10%	55%
Walking across a carpet	35 KV	7.5 KV
Walking across a vinyl floor	12 KV	3 KV
Worker on bench	6 KV	0.4 KV
Removing dual-in-line parts from plastic tubes	2 KV	0.4 KV
Removing dual-in-line from vinyl trays	11.5 KV	2 KV
Removing dual-in-line from polystyrene foam	14.5 KV	3.5 KV

FIG. 1.3 Impact of relative humidity on electrostatic potential

Even if, based on the triboelectric series table, all materials can be electrically charged, the amount of generated charge and where and how fast the charge goes depend also on the material electrical characteristics. Insulators, due to their very high surface resistivity (generally greater than 1 x 10^{12} ohms/sq), are capable of storing a huge amount of electrostatic charge. Differently a conductive material, because of its low electrical resistance (generally less than 1 x 10^{5} ohms/sq), allows electrons to flow easily across its surface. When a conductive material charged makes contact with another conductive material, the electrons will transfer between the materials quite easily. If the second conductor is attached to an earth grounding point, the electrons will flow to ground and the excess charge on the conductor will be neutralized [3].

1.1.2 Ionic charging

Ionic charging, due to the use of air ionizers, is the other fundamental slow process to generate electrostatic voltage. It occurs when we try to neutralize immobile charge on insulating surfaces, in particular only if the flow of ionized gas molecules is not properly balanced or adjusted to the charging properties of the individual manufacturing process step. The resulting voltage can easily exceed some 100 V.

1.1.3 Direct charging

Direct charging occurs if mobile charge is directly transferred from a charged object, for example with a cable into an integrated circuit. So it may usually be associated with the insertion of a device into a test socket. A lot of parameters affect amplitude and duration of the current pulse, like

- Voltage difference
- Capacitance of the IC
- Voltage source
- Impedance of the charge path

1.1.4 Field-induced charging

To explain the *Field-induced charging* consider two objects in a space with homogeneous electromagnetic characteristics. The first one is a neutral conductor, the second one an insulator with negative charge. In this way the presence of charge into insulator induce an electrostatic field. Most often just triboelectric charging is the cause for the generation of this electrostatic field. Now bringing slowly a neutral object into electrostatic field causes the separation of mobile charge on the conductive parts of the body. In particular between

two conductors will develop an electric field and so an electric potential. In these conditions we can expect an ESD between the two conductors in case of right values for surfaces distance, quality and density of charge, characteristic of the separation medium.

1.2 Static Electricity : Discharge

An exhaustive description for the discharge mechanism applied to any spontaneous transfer of charge between two conductive objects at a different electrostatic voltage is too difficult to obtain because it is related to a very high number of parameter that we will list after. For simplification, we assume that the discharge takes place between two charged conductive objects at distance d. On its opposite surfaces there is an electrostatic charge, respectively $+Q_1$ and $–Q_2$, stored up with one of methods explained in previous section. This charge induces an electrostatic field E and potentials V_1 and V_2 between conductors and a ground point. The isolator between the two electrodes may either be air or a controlled gas atmosphere. The transition from isolation to conduction requires the breakdown of the isolator, in this way we can obtain an ESD. We know that electric field can induce a low current on charges in air (free electrons or ions). For high voltages (high charge value or low distance d), an air gap breaks down starting with a single electron that generates an avalanche, because the increase of the electric field result in an increase of kinetic energy for free electrons and ions on air gap. Finally, a plasma channel of ionized gas develops to a low resistance path. This phenomenon is named *avalanche discharge* or *electrostatic discharge* and the current amplitude can reach dozens of amps with rise time shorter than ns [4]. It is also accompanied by a visible and audible spark and emission of electromagnetic radiation. For low voltages the avalanche cannot develop easily. In this case the breakdown of the insulator can be reached only after a direct contact between the conductors. This mechanism is named *direct contact discharge* and is very common in practical experience. The recombination is obtained through a low impedance conductive way, so it results in transitions of few 10 ps. This value is one order less than the system rise time of the current oscilloscopes for single events and for this reason the measurement accuracy for such fast impulses is very limited [1]. In summary it is possible to say that the fundamentals parameters for discharge are:

- electrostatic voltage
- polarity and distance between electrodes

- shape, material, and surface layers of the electrodes
- speed of approach between electrodes
- illumination of the electrodes
- composition of the gas and its pressure
- external resistance
- capacitance and inductance of the discharge circuit

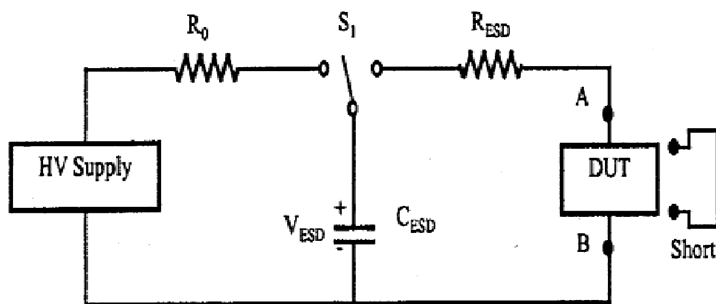
The interdependencies of these parameters are very complex and we will not improve this problem. However it is important to remember that the discharge current depends exponentially on the field strength. This fact constitutes the major influence on the reproducibility of a discharge across a closing air gap because, during the available time lag (named *statistical time lag)* elapsed between the moment when right electrical field required for breakdown is reached and the start of the avalanche, the closing of the gap continues and the electrical field strength increases further.

1.3 ESD test models

In this section we introduce some ESD stress models that permit to find and improve a protection for devices under ESD. These models define the sensibility of electronics devices and, providing certain and repeatable results, permit to compare several devices under equal conditions. This fact helps the design of better devices, less dependent on ESD problem. The ESD event can occur in different situations (into an equipment or because of handling by a person), so different models exist that envisage almost whole possible cases. Now we will introduce some fundamental models: Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM).

1.3.1 Human Body Model (HBM)

Human Body Model ESD testing is performed to evaluate the effectiveness of the protection circuitry in an integrated circuit in the case of the charged human body transfer that charge to a semiconductor device through normal handling or assembly operations. The device under test, at the time of the discharge, is assumed to be at a low potential. The ESD testing is used to determine the immunity or susceptibility level of a system or part to the HBM ESD event but does not exist only one kind of HBM. In particular exist several different standards with different ESD simulation circuits and pulse waveforms: Military Standard MIL-STD 883E (method 3015.7), JEDEC STANDARD and others. The first one, published in 1989, uses a simplified equivalent circuit (shown in next figure) to simulate an HBM ESD event [5].



Elements	*Specifications*
R_0	$10^6 - 10^7\ \Omega$
R_{ESD}	$1500\ \Omega$
C_{ESD}	$100pF \pm 1\%$
S_1	*HV relay*

FIG. 1.4 Equivalent circuit for HBM standard MIL-STD-883E

The event is simulated as an electrostatic discharge from a C_{ESD} via R_{ESD}. To ensure the reproducibility the standard define a short-circuit as output. Unfortunately this very simple model is not appropriate because it does not consider parasitic effects. A better model is presented in figure 1.5 [2].

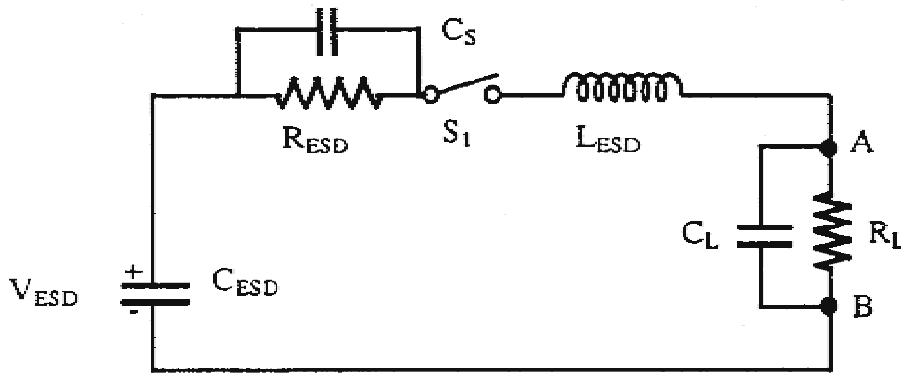


FIG. 1.5 A 4th-order HBM model circuit includes parasitic elements

This circuit introduces a parasitic inductance (typically 6 to 10 μH) in the discharge channel and two parasitic capacitances C_S and C_L (respectively for human body and test board). In this way it is possible to obtain a better analytical equation:

$$I_{ESD}(t)=V_{ESD}C_{ESD}\left\{\frac{\omega_0^2}{\sqrt{\alpha^2-\omega_0^2}}\right\}e^{-\alpha t}\sinh\left(\sqrt{\alpha^2-\omega_0^2}*t\right) \quad (1.1)$$

where i_{ESD} is the discharge current, V_{ESD} the potential and

$$\alpha=\frac{(R_{ESD}+R_L)}{2*L_{ESD}} \qquad \omega_0=\frac{1}{\sqrt{L_{ESD}C_s}} \qquad \alpha>\omega_0$$

So HBM ESD event can be modeled as a current source with the current waveform shown in figure 1.6. The current peak for HBM model is between 1.20 A and 1.48 A (for 2 kV HBM ESD stress), the rise time between 2 ns and 10 ns and the decay time is 130–170 ns. In particular we obtain that for a rise time of 10 ns L_{ESD} = 7.5 μH (in case of short-circuit load). The parasitic capacitances have two different effects on the waveform. The first one (C_S) creates an overshoot of current, so an increase of device stress on the first stage of discharge. The capacitance C_L increases the rise time and reduces the current peak;

further it can disturb the measure creating an additional peak of current not controlled by R_{ESD}.

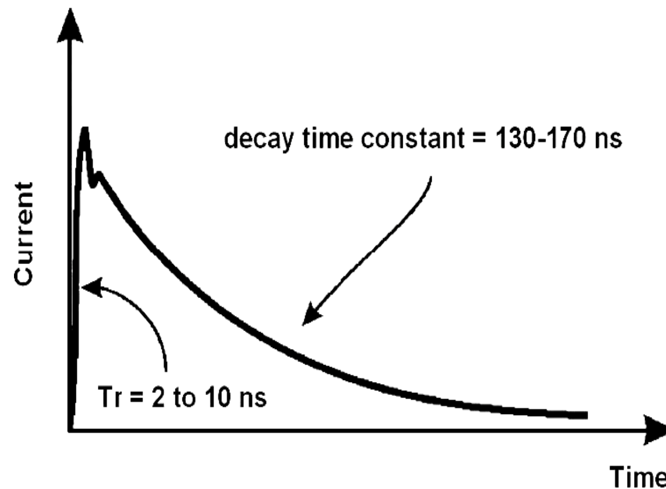


FIG. 1.6 Current waveform for HBM ESD event

Other standards, as JEDEC (JESD22-A114D) or AEC, have a main common modification in an extra tester verification step using a 500 Ω load in addition to short-circuit calibration [6]. In this way it is possible to take attention on parasitic effect of a generic C_{DUT} .

In order to minimize errors with environmental conditions, all testing must be performed in a controlled environment room which maintained temperature and humidity at relatively constant levels of 23 ± 4℃ and 32 ± 5% relative humidity. Furthermore in real world situations a person may have a resistance and capacitance that differ from this model.

Also the practice is defined for a standard. An example of specifications for HBM test is the next one (in accordance with the ESD association specification) [7]:

- Each I/O pin should be stressed against each power supply pin. It is permissible to short all the power supply pins together
- Each power supply should be stressed with respect to other power supplies
- Three repeated ESD zaps in sequence are required, and there should be at least a 300 ms interval between consecutive zaps

To allow easy comparison between components, the standards define their ESD protection level. For HBM model we have different classes, shown in this table.

Class	*Voltage range (V)*
Class 0	<250
Class 1A	250–500
Class 1B	500–1,000
Class 1C	1,000–2,000
Class 2	2,000–4,000
Class 3A	4,000–8,000
Class 3B	>8,000

FIG. 1.7 Human body model classes

1.3.2 Machine Model (MM)

The *Machine Model* is very similar to HBM. It was initially developed by the EIA in Japan as a particular case for HBM model. This model aims to represent the type of damage caused by equipment in manufacturing, including in-line inspection tests and automatic test equipment (ATE). As the resistance is very low for metallic machinery, peak current for ESD events is very high in this case (much higher than the HBM case). So MM was designed as a severe case for HBM. The model circuit is shown in next figure.

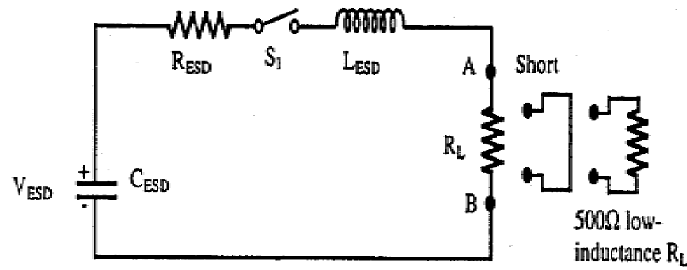


FIG. 1.8 MM ESD circuit including parasitic elements

It looks like HBM circuit with the substitution of the value for C_{ESD} = 200 pF and a resistance nominally of 0 Ω. An analytical model for MM ESD waveform can be obtained with next equations:

If $\alpha > \omega_0$

$$i_{MM}(t) = V_{ESD} C_{ESD} \left\{ \frac{\omega_0^2}{\sqrt{\alpha^2 - \omega_0^2}} \right\} e^{-\alpha t} \sinh\left(\sqrt{\alpha^2 - \omega_0^2} * t\right) \qquad (1.2)$$

where $\alpha = \frac{(R_{ESD} + R_L)}{2 * L_{ESD}}$ $\qquad \omega_0 = \frac{1}{\sqrt{L_{ESD} C_S}}$

If $\alpha < \omega_0$

$$i_{ESD}(t) = \frac{V_{ESD}}{L_{ESD}\omega_0} e^{-\frac{R}{2L_{ESD}}t} \sin(\omega_0 t) \qquad (1.3)$$

where $\omega_0 = \frac{1}{\sqrt{L_{ESD} C_{ESD}}}$, $R = R_{ESD} + R_L$

But this model with zero value for resistance is too affected by parasitic parameters from test board or ESD device. A solution defined by “ESD Association”, JEDEC and AEC is shown in figure 1.9 , where 1.5 kΩ resistor was replaced with a 750 nH inductor and there is an effective resistance of 10 Ω in the discharge path [8].

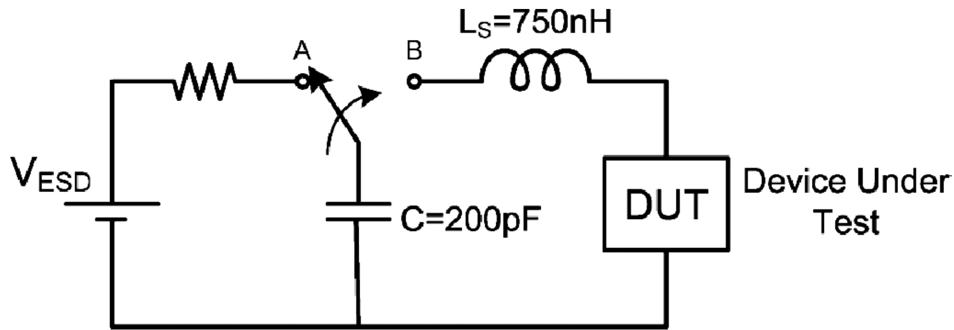
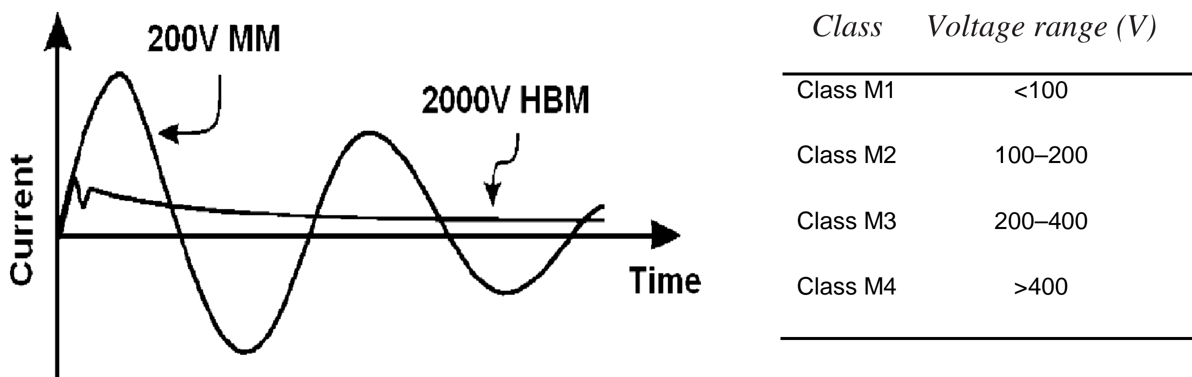


FIG. 1.9 MM ESD equivalent circuit with 750 nH inductor

However the inductance value is the most critical parameter in this model because it controls the rise time and also the waveform of current during the discharge. Further, it forces MM to have a low grade of correlation between different test boards. The typical voltage values range is from 100 V to 500 V, very lower respect HBM (see next graph).



Class	*Voltage range (V)*
Class M1	<100
Class M2	100–200
Class M3	200–400
Class M4	>400

FIG. 1.10 Machine Model: comparison with HBM and classes

The increased use of automatic handling equipment has resulted in a situation where the impact of CDM (shown later) and MM ESD events have surpassed HBM ESD events as the major contributor of ESD failures. Unfortunately, many automatic equipments have wrong ESD protection setups within itself. This problem is now under attention and we can find several studies that show possible solutions for it, analyzing equipment used in conventional semiconductor manufacturing processes [9]. For example we can talk about trim and form machines, that involves the use of lead frame material where the pins of ICs are shorted together up to the external lead finishing process. After individual ICs are separated from the lead frame and the pins of ICs are formed into different shapes and angles as per the respective package specification. The more critical process step is where there is a separation between the handling tool and the IC, because it involves a robotic arm picking up the ICs and placing it onto a metal chute. Since robotic arm is conductive and ICs package is an insulator, it is possible to have a hard discharge during the placement of the IC onto the metal chute. To understand better the problem, the voltage measured on the package is very high (300 V) and the clearance between the pins of the ICs and the metal chute is very small (only 0.1mm).

1.3.3 Charged Device Model (CDM)

As we have shown in previous section, the Charged Device Model has became (with Machine Model) the primary real world ESD event among rapid discharge events in automated handling, manufacturing and assembly of IC devices. Its importance has dramatically increased in the last few years as package feature sizes, capacitance and pin count have scaled upward. Differently from HMB type, where a charged IC part discharges when a pin contacts a conductive surface, CDM is a self-discharge procedure used to simulate the event that occurs from charged packaged ICs which subsequently discharging into a low impedance ground (as a grounded surface or a metal work table). So measures obtained with CDM are not comparable with HBM or MM.

Even if the CDM concept was introduced in 1974 by Speakman ("Human body model is not the only concern to semiconductor users"), it is very difficult to build up a good CDM ESD tester because of the tremendous influence of parasitic elements on the pulse generated (look at figure 1.11 where a parasitic inductance of only 50 nH gives the dashed curve, very different to the curve described by JEDEC standard).

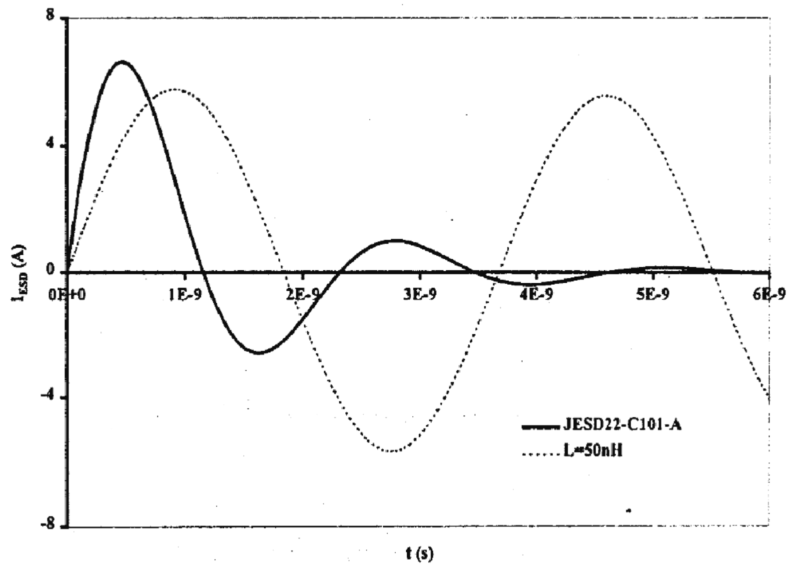


FIG. 1.11 CDM pulse waveform defined by JESD22-C101-A standard for V_{ESD}=500 V and C_{ESD}=6.8 pF. Parasitic inductance (50 nH) have strong impact on the pulse shape.

However there are two different types of apparatus: non-socketed and socketed. In the first one the device under test is tested directly, in the second the device is placed into a socket (shown in next figure in field-induced version, FCDM) and then it is charged and discharged via the socket. The socketed CDM test is more used, produces more severe damage and in some cases a different failure mode compared to the non-socketed test.

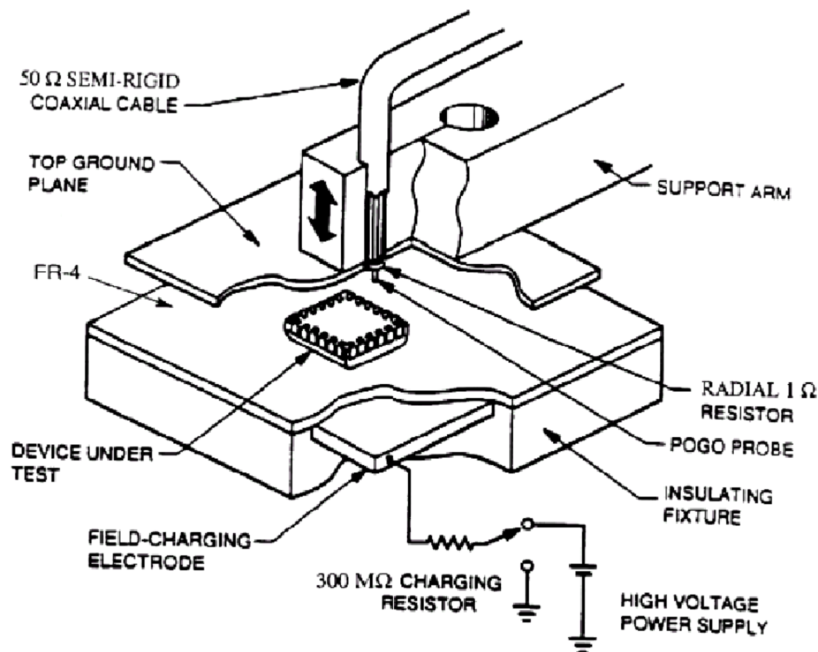


FIG. 1.12 FCDM test system

The simple equivalent circuit of the CDM, defined by different standards (JEDEC, AEC , ESD Association), is shown in figure 1.13 . C_{CDM} is the sum of all capacitances in the device and the package with respect to ground and R_{CDM} is the total resistance of discharge path. For 500 V CDM (considering standard JESD22-C101-A), the typical model parameters are C_{CDM} = 10 pF, R_{CDM} = 10 Ω, R_L = 10 Ω, and L_S = 10 nH (the discharge impedance in real life is close to zero, but it is finite and small in an ESD tester) [8].

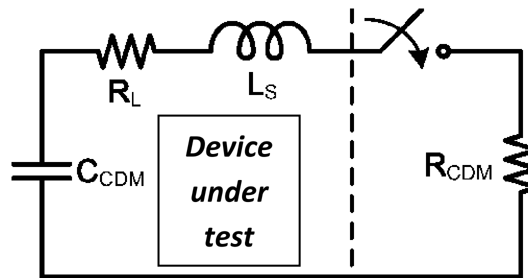


FIG. 1.13 CDM ESD equivalent circuit

The current waveform of a 500 V ESD event has a rise time of ~0.3 ns and a peak of ~10.4 A, so the peak current is much higher and rise time (as well as stress duration) is much shorter compared to the current in an HBM (look at next graph).

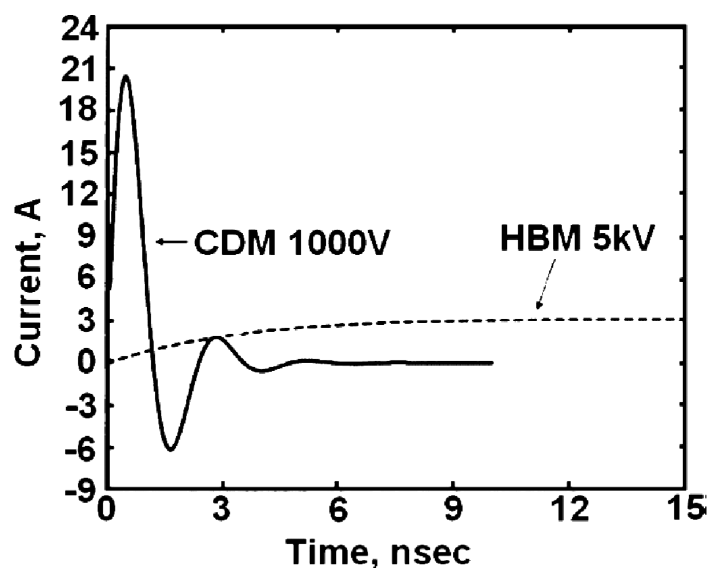


FIG. 1.14 Comparison between current waveforms of CDM and HBM ESD event

Figure 1.15 shows CDM classes. The protection level of 500 V for CDM stress is typically used to ensure the general-purpose chip reliability. Higher CDM classes are applied for special ICs used for automotive, aviation and other industries with high reliability requirements.

Class	*Voltage range (V)*
Class C1	<125
Class C2	125–250
Class C3	250–500
Class C4	500–1,000
Class C5	1,000–1,500
Class C6	1,500–2,000
Class C7	>2,000

FIG. 1.15 Charged device model classes

Nevertheless the rapid advancement of IC technology scaling, coupled with the increased demand for high speed circuit performance, are making it increasingly difficult to guarantee the commonly customer specified 500 V CDM specification [10]. In fact three trends have combined to greatly complicate the task of designing effective on-chip CDM protection circuits:

- The pin count and size range of IC components has grown significantly. This is a serious issue because the peak current produced during CDM testing at a given pre-charge voltage is a sensitive function especially of package size. To protect fragile circuits it is required a large increases in ESD layout area on the die, but in some cases this area becomes prohibitively large.

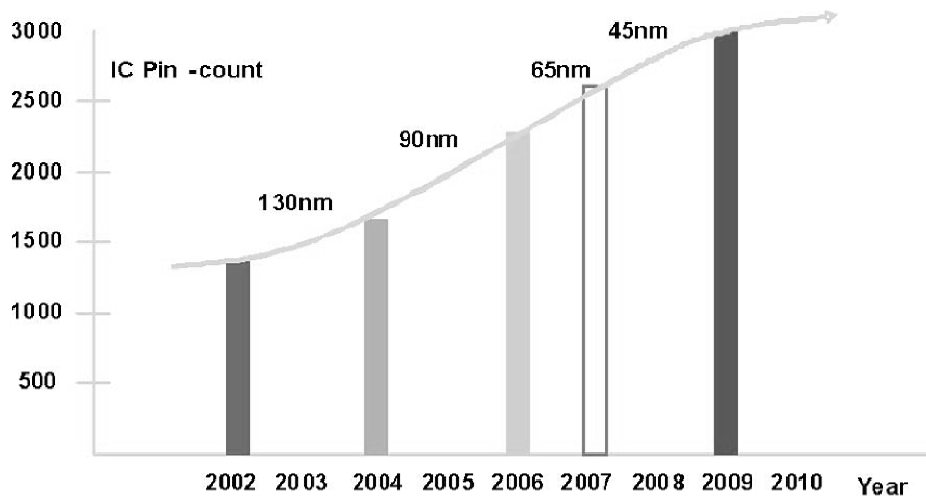


FIG. 1.16 Trend for high pin count BGA Packages

- Devices are smaller and more fragile as well as thinner and more resistive. This makes it more difficult to protect the component at a given CDM current level.

- Strict electrical performance limitations on mixed signal ICs with high speed digital, RF analog and other performance sensitive pins (much more prevalent) limit options for ESD protection, making impossible to reach typical CDM qualification criteria.

Those trends conducts to adopt at this time a general CDM qualification target of 250 V (according to JEDEC) as a reasonable compromise between on-chip design and a uniform manufacturing process control requirement for all IC products [11]. Anyway the implementation of a higher CDM robustness in cases where it does not degrade performance or delay time-to-market adds further margin and is always beneficial. In future, as silicon technologies advance further into the deep sub-50 nm regime towards the 22 nm node and beyond, even lower withstand voltages will be required to account for the scaling effects and the continued drive towards higher circuit speed performance at data rates reaching 40 Gb/sec or more. A roadmap based on this projection is shown in next figure.

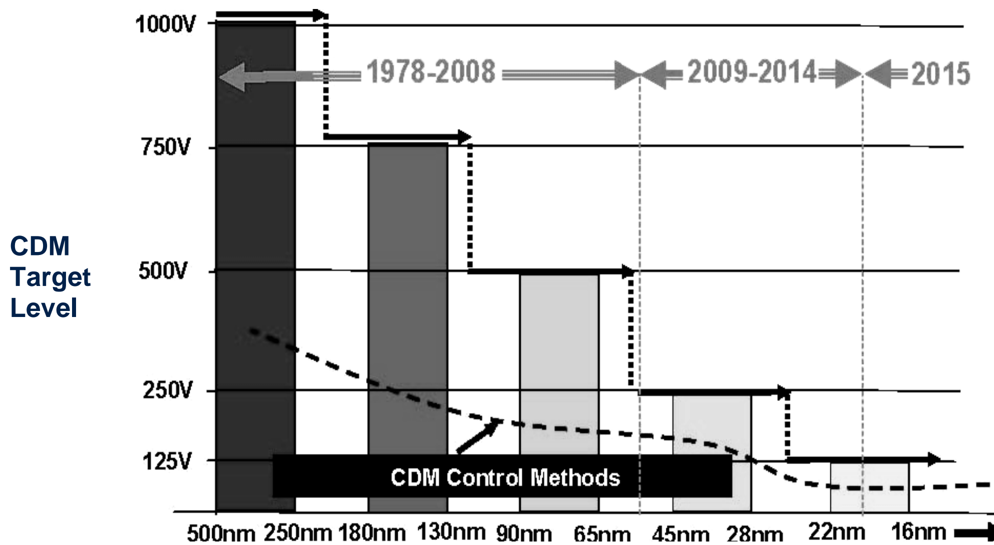


FIG. 1.17 CDM Roadmap. Technology scaling effects on practical CDM levels and the associated CDM control requirements

1.3.4 Other Models

There are other different models based on previous fundamental models. In this section we analyze the *Charged Board Model* (CBM) and the *Human Metal Model* (HMM). A particular attention will be given to *Transmission Line Pulse* (TLP) testing on Chapter 3.

The *Charged Board Model* is similar to CDM but it is used if components are mounted on a circuit board. This difference is very important because it was shown that ICs robust to HBM and CDM damage at the package level may be susceptible to CBM damage at the board level depending on the PCB design or board capacitance. The test simulator was developed by Bell Laboratories and is shown in next figure (in field-induced version, FCBM) [8].

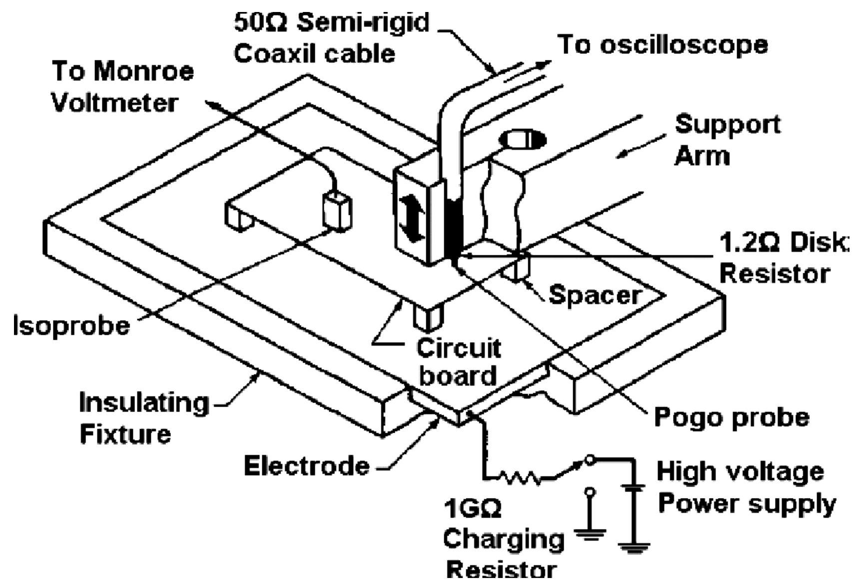


FIG. 1.18 Field-induced CBM test system

As we can see the system is very similar to CDM, but in this case the discharge has much higher energy and very faster rise time. The reason of this difference is due to a different value for capacitance at board level, very higher in comparison to the chip level (remember that $t_{rise}=\sqrt{L_{CBM}C_{CBM}}$ and $I_{peak}=V_{CBM}\sqrt{\frac{C_{CBM}}{L_{CBM}}}$).

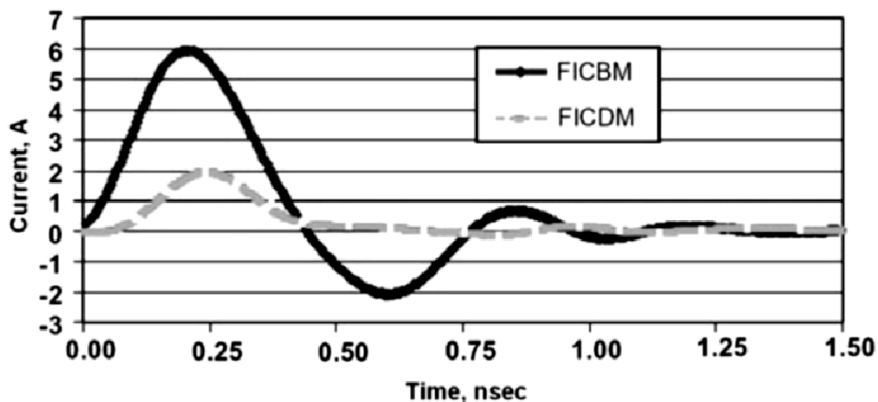


FIG. 1.19 Comparison of FICBM and FICDM current discharge waveforms of Dual Op. Amp. with a 375 V charge voltage

The *Human Metal Model* is a new model developed in last years to enable the IC manufacturer to predict the ESD performance of their products under system-level stress conditions. It was proposed by ESD Association in 2008 with work “Electrostatic Discharge Sensitivity Testing - Human Metal Model (HMM)”, published only in autumn 2009. All standardized method for testing components shown in previous sections was developed to test a component-level ESD stress. In this way an IC can fulfill the component-level ESD robustness requirements, while failing the ESD system-level tests carried out by the system vendor. So HMM reproduces an ESD discharge caused by a human touching a pin of a grounded electrical component using a metal tool.
The discharge circuit, shown in next figure, have a pre-charged capacitor of 150 pF and a resistor of 330 Ω to create the stress waveform, according to IEC 61000-4-2 standard for component-level testing. There are also some parasitic components to obtain desired waveform for discharge current (*FIG. 1.21*).

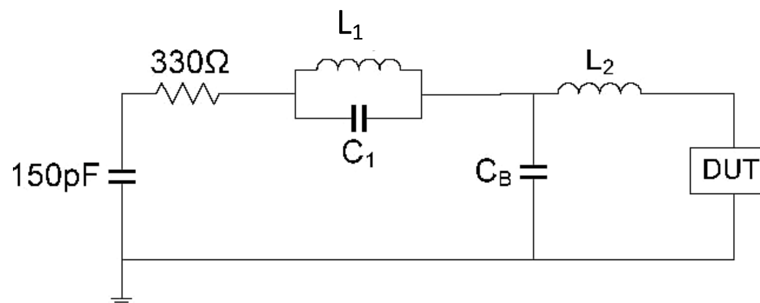


FIG. 1.20 Discharge circuit in HMM on-wafer tester: Ln, Cn – parasitic elements in test setup, CB – board capacitance, DUT – device under test

A recent study [12] has shown that a correlation among device responses on system-level ESD compared to component-level ESD stress (as HBM) depend strongly on the device type. Range of values is very high, from 1.5 for the high voltage ESD clamp up to 8.6 for the STI-SCR based power clamp.

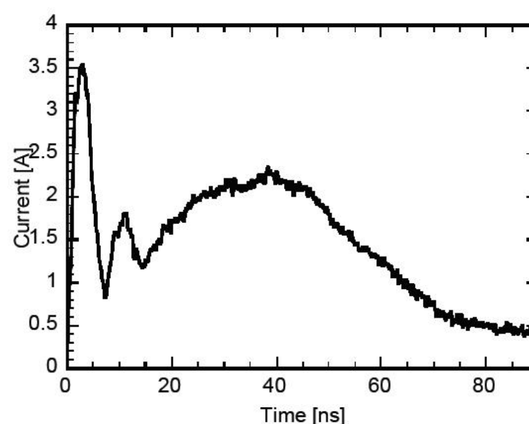


FIG. 1.21 HMM current waveform of a short on a wafer; precharge voltage of 1000V

Chapter 2

Electrostatic Discharge: Damages and Protection Structures

In this chapter it will be analyzed fundamental damage mechanisms for failures due to ESD in a semiconductor device and in main structures used to prevent it. First of all a brief introduction on failures due to an ESD event is necessary.

2.1 Failures for ESD events in ICs

ESD events affect integrated circuits (ICs) essentially in two stages during the product life: wafer-fabrication process and assembly operation. In the first case, as clean-rooms are good sources for charge-generating materials due to the extensive use of synthetic materials in containers and tools [13] , we can have

- the ESD event distorts the fine pattern defined on the mask for a photolithography operation, then each circuit will be printed with this damage [14]

- a direct discharge to the wafer that results for example in a gate oxide and junction damages [15]

In the other stage ESD hazards are present in all of these operations [16]

- wafers must be cut to yield individual dies
- dies are inspected and placed in packages
- wires are attached to allow signals to travel from the outside pins to the die
- package is formed around the die

ESD and EOS (electrical overstress) are the major cause for ICs failures. As it is shown in figure 2.1 ESD related failures can reach up to about 70% failure modes [17].

Percentage	**51%**	**72%**	**23%**	**38%**	**45%**	**43%**	**39%**
Author	Green	McAteer	Euzent	Merill	Wagner	Shumway	Brodbeck
Year	1988	1988	1991	1993	1993	1995	1997

FIG. 2.1 *The EOS/ESD failure percentage as total failure modes studied by different author over the years*

These failures are caused by at least one of three reasons:

- localized heat generation
- high current densities
- high electric field intensities

In particular the current densities implies high power dissipation, so thermal damages due to a growth in the lattice temperature. In fact, having silicon a negative resistance relationship with temperature coefficient, this power dissipation in a small volume will result in higher temperatures and thermal runaway (if the rate of heat generation becomes greater than the rate of heat removal). Moreover high current, combined with high electric field intensity, makes failure more likely across the dielectric and junctions in the circuit. In particular the gate oxide is the most vulnerable dielectric for its thinness and because structural defects and sharp corners in layouts aid to increase electric field and current values [8]. ESD induced failures can be divided in two categories: *soft* and *hard* failures. In the first case the device has a partial damage typically resulting in an increased leakage current that does not compromise the working operation of a defined circuit. Basic functionalities of the device are so operative but without any guarantee about potential latency effects. For hard failures, the basic functionalities of the device are completely destroyed during the ESD event. In next section we will analyze fundamental damage mechanisms capable to induce failures, now we focus on how it is possible the identification of failure locations [1]. This problem is very important to the process of designing ESD protection structures. There are different kind of failure analysis techniques but the easiest is maybe the Liquid Crystal Analysis, where a liquid crystal is applied to a wafer placed on a temperature-controlled chuck. When the temperature is raised to about 50 ˚C (depending on the type of liquid crystal used) and the device is powered up, it is possible to detect failures on the order of μA as shown in figure 2.2 . Major advantages of this technique are certainly its low cost and the nondestructive behavior but it is impossible to reveal the exact location of the failure because of its low resolution.

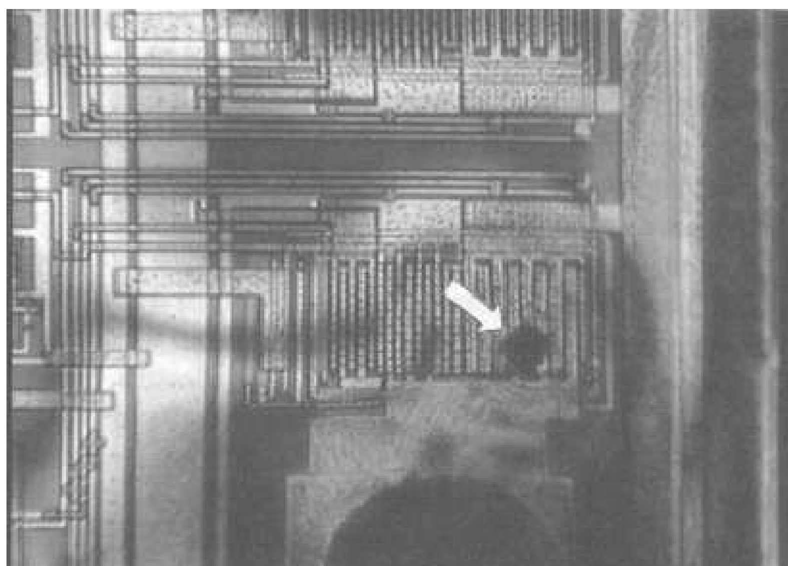


FIG 2.2 Liquid Crystal Analysis of ESD damage in a CMOS output buffer

To obtain a better resolution reducing analysis time is used Light Emission Microscopy. This technique identifies, thanks to a photon detector, regions of excessive light emission through the observation of emitted photons from a powered up device, because photoemission detects reverse-biased breakdown. Respect to previous technique occurs more expensive equipment but none thermal control is required, moreover recent improvements have made possible to observe infrared emission owing to thermal effects [1]. Once the failure location has been revealed (look at next figure) it is possible to examine the damage area through a Scanning Electron Microscopy (SEM) process.

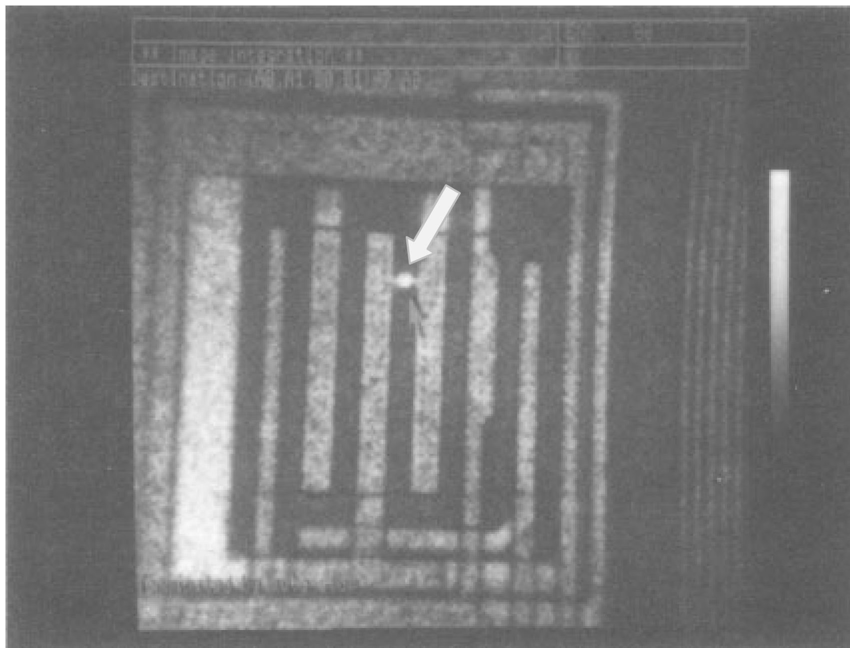


FIG 2.3 Photoemission analysis of ESD damage in a CMOS output buffer

Other essential parameter for ESD protection structure design is the failure threshold, determined by monitoring the leakage current at stressed pin of an IC. In fact it has been shown a close correlation between ESD failure threshold and change in leakage current ΔI_{leak} [18]. In particular ΔI_{leak} in circuits fabricated in an advanced CMOS process can be in one of five categories [19], each of that can be related to a fundamental damage mechanism shown in following section:

(a) No increase in leakage current, $\Delta I_{leak} = 0$

(b) $\Delta I_{leak} < 10$ μA

(c) 1 μA < ΔI_{leak} < 100 μA

(d) 100 μA < ΔI_{leak} < 1mA

(e) ΔI_{leak} > 1mA

Naturally in case (a) there is no effect on the behavior of the IC. In first approximation it is possible to consider cases (b) and (c) as soft failures, while for other cases we have an hard failure. That is easily to guess in examples shown in next SEM photographs. In first case an ESD stress voltage range up to 2 KV has induced a ΔI_{leak} < 10 μA, in second one has been observed a ΔI_{leak} ≈ 1mA.

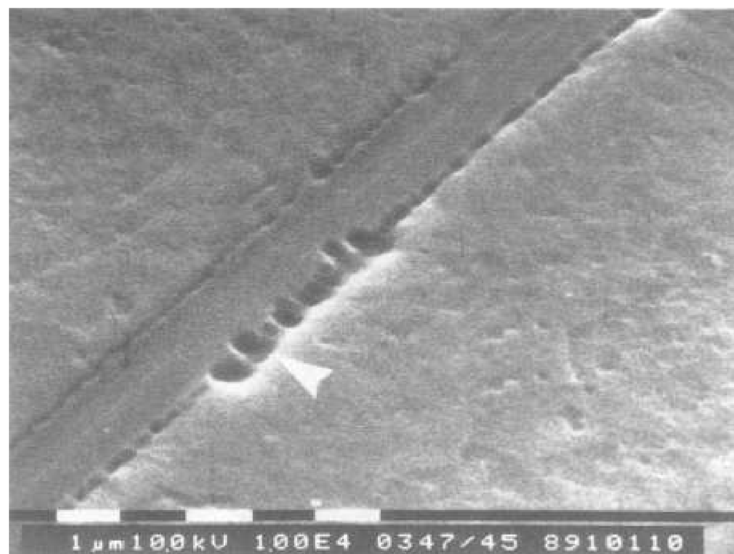


FIG. 2.4 SEM photograph of drain/gate diffusion edge damage

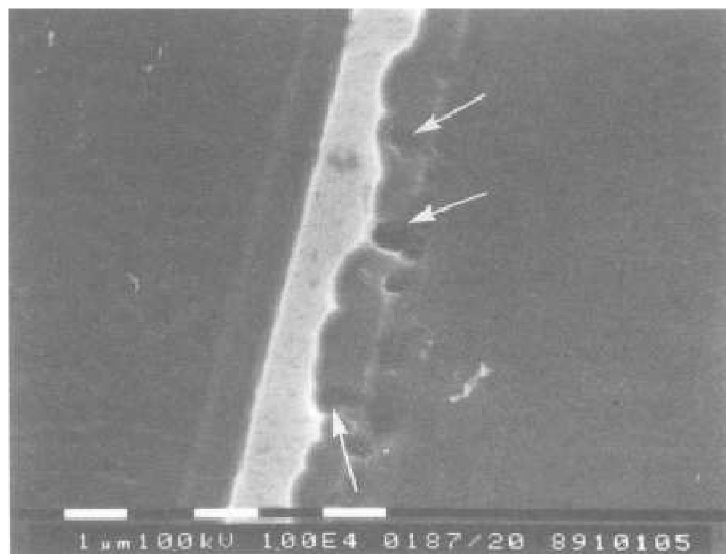


FIG. 2.5 SEM photograph of an nMOS transistor showing gate oxide damage

2.2 Damage mechanisms for failures due to ESD events

Even if ESD or EOS events can damage a semiconductor device into several modes, there are four fundamental mechanisms:

- Oxide Punch-through
- Junction Filamentation and Spiking
- Metallization and Polysilicon Burn-out
- Charge Injection

The first case is the principal mechanism for MOS circuits because it is related to an ESD event that causes a voltage pulse able to damage dielectric or oxide into a device. Typically, gate oxides can withstand an electric field of 6–10 MV/cm before it breaks down. But the maximum voltage across the device, due to the ESD event, can exceed the voltage to have gate oxide breakdown (V_{BD}), inducing oxide failures (*FIG. 2.6*). The gate oxide breakdown (V_{BD}) is also a critical function of its thickness, so with the scaling down of the device sizes, the gate oxide thickness is also reduced resulting in an increase of this failure mechanism. Summarizing, a typical dielectric punch-through process has following stages:

1. An high voltage spike causes a potential difference between two pins connected at opposite sides of a dielectric
2. Applied voltage exceeds dielectric breakdown voltage
3. Dielectric breaks and begins to conduct
4. The temperature of dielectric grows up in the conduction point
5. Conduction point melts making a short circuit between pins

So, in order to minimize failures due to oxide punch-through, it is essential to avoid the generation of voltage spikes into the circuit.

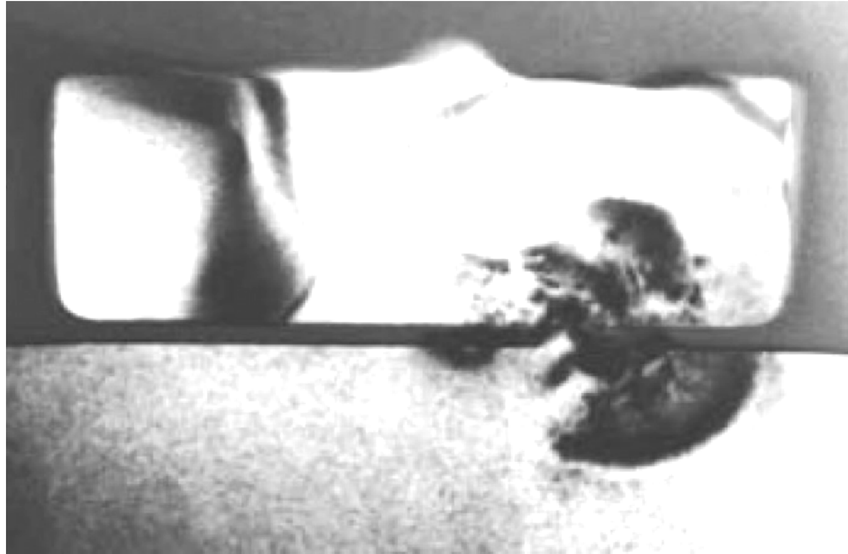


FIG. 2.6 Gate oxide damage in MOS transistor after the CDM stress

Junction filamentation and *spiking* are two similar phenomena related to an increase in the reverse bias leakage of a *p-n* junction. In *junction filamentation* the ESD event causes current to flow through the junction (in worst case shorted), inducing high power dissipation and an increase of the temperature until the junction. In this conditions silicon can melt, dropping its resistance by a factor of 30 or more [8]. This causes more of the current to flow in the narrow and melted region, leading to thermal runaway. The failure regions can be located close to the device surface, as in the gate to drain overlap region for MOSFET devices (*FIG. 2.7*), or deeper in the silicon (like BJT, SCR and Thick Field Oxide Device).

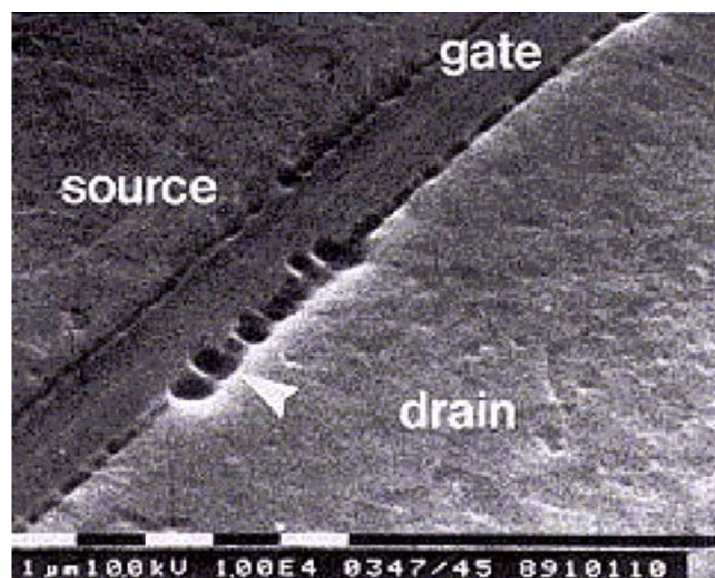


FIG. 2.7 Drain junction filamentation in MOS transistor due to the ESD stress

For *junction spiking* the melted region grows until it intercepts a metal contact, causing the degradation of metal and silicon. In this case the damage thresholds are lower for metal contacts because the metal-silicon alloy is formed at temperature lower than melting point of silicon.

The fundamental mechanism that can occur in a resistor or in metal lines, as in polysilicon interconnection and thin-films, is just *Metallization and Polysilicon Burn-out*. Practically the high temperatures induced by the ESD pulse can induce the melting of a metal or polysilicon line located close to the hot spot region in *p-n* junction, resulting for example in an interconnection opening (*FIG. 2.8*). However the melting of a resistor or a metal line can depend also on other types of mechanisms, as dielectric or oxide breakdown. During the chip design it is so essential making resistors and metal lines wide enough to handle an ESD current pulse for the desired level of protection.

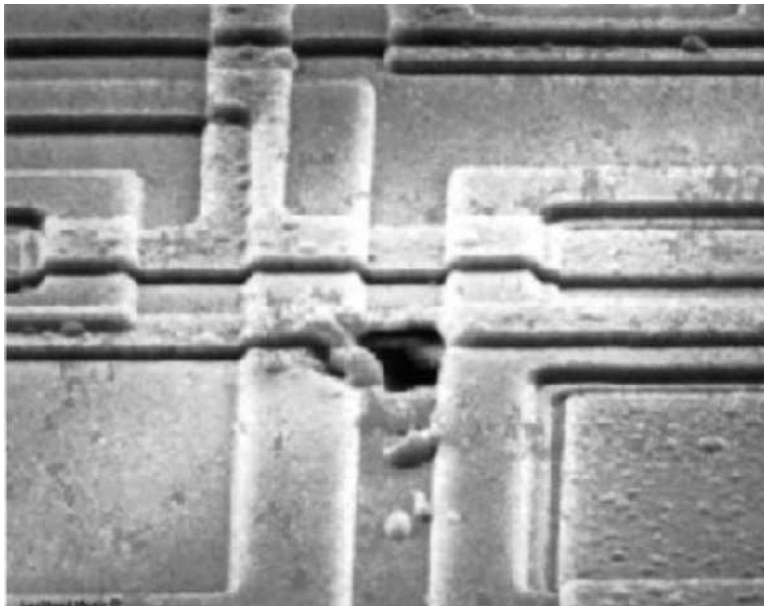


FIG. 2.8 Interconnects damage due to the ESD stress

Charge injection occurs into the gate oxide of *p-n* junction when an ESD event causes a reverse-biased junction able to conduct by avalanche multiplication. This induce the increasing of leakage current because some carriers, under ESD event effect, have enough energy to surmount the oxide-silicon energy barrier. The degree of degradation in oxide is related to the current density of the injected charge, but a localized charge injection during the drain junction avalanche breakdown at the ESD event causes more damage than the uniform charge injection from the gate to the body of a transistor during normal operating conditions [8].

2.3 ESD protection: structures and devices

We have described how much an ESD event can be detrimental to integrate circuits, so it is required to look for a solution to avoid or limit this phenomenon. Followed strategy can be divided in *active* and *passive* protections. The last ones are preventive measures aim at preventing the accumulation of static charge near the electronic circuit. These criteria are related essentially to productive processes or to device utilization. In particular there are control or check procedures for materials or equipments as:

- utilization of antistatic materials and ground bracelets to handle electronic circuits
- a correct grounding for equipment
- utilization of ionizers
- utilization of wrappings or containers against ESD

Active protections are founded on strategies processed in design stage to make integrate circuits more resistant to electrostatic discharges. For this reason each circuit has its protection structures with different performances, working and devices used to implement it. Generally this kind of protections are essentially auxiliary protection circuits as well as appropriate layout rules. The protection circuit has to exhibit dynamic characteristics suitable for the ESD event but, at the same time, it has not to affect the behavior of protected device under normal operating conditions. So, only during the ESD event, current related to it has to be sent towards ground, keeping the input voltage of the circuit under protection at a safety level for its working. The fundamental characteristics to design efficient protection structures are:

- dynamic impedance very high without ESD event, but very low in case of ESD event to assure a good discharge path
- high robustness

- threshold of intervention higher than voltage of normal operating conditions, but lower than voltage for device failure
- very fast time of intervention because ESD current reach its peak in about a ns
- transparency in case of no ESD event
- compatibility with technological process
- lowest occupation of area

Fundamental devices used into protection structures for CMOS technologies are diodes, silicon-controlled rectifiers (SCR) and MOSFETs. Based on the shape of the *I-V* characteristic of semiconductor devices, they are divided into two main categories: *non-snapback* devices and *snapback* devices. For diode, as other *non-snapback* devices, if the voltage across it is increased beyond a certain voltage, the current starts to increase rapidly while the voltage across it remains constant. *Snapback* devices (as SCR and MOSFET), similar to a reverse biased diode, go to the breakdown region as the voltage across them is increased. After breakdown, due to an internal positive feedback mechanism, the voltage across the device drops and the device moves from breakdown region to the holding region. Now a brief analysis of these devices under ESD effects is presented.

2.3.1 Diode

Diode has been a very important electrostatic discharge device in the past, as well as remaining an important ESD element in future technologies for its low capacitance and because it is scalable. In fact, diode designs have migrated from CMOS to silicon-on-insulator (SOI) and radio-frequency applications [20]. Our analysis of diode behavior under high current conditions (so under ESD effect) will be divided in forward-bias and reverse-bias conditions. In particular the first condition is important to understand why a diode can be a current discharge element in a forward-bias mode of operation.

For forward-bias condition the diode current equation is

$$I=qA\left\{\frac{D_p}{L_p}\nabla p_n+\frac{D_n}{L_n}\nabla n_p\right\} \qquad (2.1)$$

where the excess minority carrier population is (under high level injection)

$$\nabla p_n=\frac{p_n\left(e^{V_j/kT}-1\right)\left(1+\frac{n_n}{p_p}e^{q\left(V_j-\phi_i\right)/kT}\right)}{1-e^{2q\left(V_j-\phi_i\right)/kT}} \qquad (2.2)$$

$$\nabla n_p=\frac{n_p\left(e^{V_j/kT}-1\right)\left(1+\frac{p_p}{n_n}e^{q\left(V_j-\phi_i\right)/kT}\right)}{1-e^{2q\left(V_j-\phi_i\right)/kT}} \qquad (2.3)$$

From this expression, the diode current equation in high-level injection can be expressed as

$$I=I_s\frac{\left(e^{V_j/kT}-1\right)\left(1+\eta e^{q\left(V_j-\phi_i\right)/kT}\right)}{1-e^{2q\left(V_j-\phi_i\right)/kT}} \qquad (2.4)$$

where $I_s=qA\left\{\frac{D_p}{L_p}p_{n0}+\frac{D_n}{L_n}n_{p0}\right\}$, $\eta=\frac{N_a}{N_d}$ for a p+/n diode, $\eta=\frac{N_d}{N_a}$ for a n+/p diode

If the excess minority-carrier injection is small compared with the doping concentrations the (2.4) is expressed as

$$I=I_s\left(e^{qV_j/kT}-1\right) \tag{2.5}$$

So the value of on-voltage and on-resistance of the diode can be calculated as

$$V_{on}=\frac{kT}{q}\ln\frac{N_aN_d}{n_i^2} \tag{2.6}$$

$$R_{on}=\left[dI/dV_j\right]^{-1}=\frac{kT}{qI_s}e^{-\left(qV_j/kT\right)}\ , \quad V_j>V_{on} \tag{2.7}$$

These parameters are functions of the semiconductor doping and junction area but, due to low values, diode is able to carry a large current in forward bias. Furthermore, power dissipation and internal temperature of the diode remains low under high current conditions. It is possible to improve this model regarding the diode series resistance. During the ESD event next resistances are no more negligible and can be expressed as [20]

$$R_{anode}=R_M+R_C+(R_{sil})_{eff}+(R_d)_{eff} \tag{2.8}$$

where the anode resistance is the resistance of the interconnect, the contact, the salicide film, and the anode implant

$$R_{cathode}=R_M+R_C+(R_{sil})_{eff}+(R_d)_{eff}+R_{well} \tag{2.9}$$

where R_{well} is the well resistance.

Regarding the voltage drops across these resistances in (2.5), the series resistance, obtained from the derivative of the voltage with respect to current, can be express as

$$R_{series}=\frac{dV_D}{dI_D}-\frac{2kT}{q}\frac{1}{I_D} \qquad (2.10)$$

where I_D, V_D are respectively the current and the voltage across the diode.

Further improvement in diode model can be obtained regarding its self-heating [20]. In fact, during an ESD event the temperature of the diode increases, modulating its response. We can assume that the heating is expressed as the change of the junction temperature with time, without effects on the minority-carrier diffusion (significantly faster than the rise in temperature). The junction temperature increase can be expressed as

$$T_J=\Theta_{TH}P_D \qquad (2.11)$$

where $P_D= I_D V_D$ is the input power and Θ_{TH} is the thermal impedance of the diode structure.

Under reverse bias condition, the current is generated through the avalanche breakdown process. In this case the on-voltage equals to the avalanche breakdown voltage of the *p-n* junction. For an abrupt junction diode we obtain the equation

$$BV=3.25\times10^{6}\ \frac{N_a+N_d}{N_aN_d}\ E_{crit}^2 \qquad (2.12)$$

Typical values for the on-voltage and the on-resistance for a diode is in the range of 10–20 V, and 50–100 Ω respectively [8]. These high values induce high power dissipation and internal temperature of the reverse-biased diode under high current conditions, making it unsuitable for ESD protection applications. Differently in these conditions the diode shows small current when used in normal circuit operation. In conclusion, in order to obtain a suitable protection under ESD conditions the diode is biased in forward bias region, while under normal operating conditions it is biased in reverse bias region.

2.3.2 Silicon controlled rectifier

Silicon-controlled rectifier (SCR) structures (*FIG. 2.9*) are important semiconductor devices for electrostatic discharge because they can have transitions from a low-current/high-voltage to a high-current/ low-voltage state. Known as the Shockley diode, the SCR is a four-region device of alternating p- and n-doped regions with three physical p–n metallurgical junctions (*FIG. 2.9 (a)*), also an inherent parasitic structure in semiconductor technologies. The four region pnpn can be understood as a cross-coupled pnp and npn bipolar junction transistor (BJT) device, where the base of the pnp BJT device is the collector of the npn BJT device, and the base of the npn is the collector of the pnp BJT device (*FIG. 2.9 (b)*).

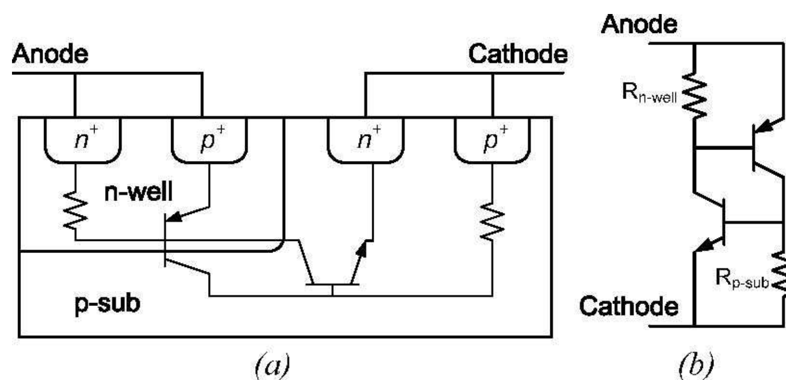


FIG. 2.9 Silicon controlled rectifier : (a) cross section (b) equivalent schematic

Application of a positive bias on the emitter of the pnp element and a ground potential on the emitter of the npn element establishes a voltage across the SCR. Maintaining the base–collector junction of the pnp (so the base–collector junction of the npn) in a reverse-biased state, it is impossible for current flow from the anode of the pnpn to the cathode. Only an increase in the applied voltage allows current to flow efficiently from the SCR anode to the cathode. This mode of operation is called the forward blocking state.

The current through the pnpn structure can be expressed as a function of the bipolar transistor current gain and the base–collector leakage current

$$I=\frac{I_{cp0}+I_{cn0}}{1-\left(\frac{\beta_n}{\beta_n+1}+\frac{\beta_p}{\beta_p+1}\right)} \quad (2.13)$$

From (2.13) the current magnitude in the SCR device can be large if the leakage current in the base–collector junction is large. This is possible due to impact ionization, punch-through, photons, or an external source of current.

The condition for triggering of the silicon controlled rectifier is a function of the currents through the feedback elements, influenced in particular by intrinsic resistances in the collector and base or emitter structure. It is possible to determine the bipolar current gain required to have a regenerative feedback condition and an expression for holding current as

$$\beta_n\beta_p \geq \frac{I+I_w\beta_p}{\left[I-I_{sx}\frac{(\beta_p+1)}{\beta_p}-I_w\right]} \quad (2.14)$$

$$I_H=\frac{\beta_p(\beta_n+1)I_w+(\beta_p+1)\beta_n I_{sx}}{\beta_p\beta_n-1} \quad (2.15)$$

where $$I_W=\frac{(V_{BE})_{pnp}}{R_w}=\frac{V_0}{R_w}\ln\left[\frac{I-I_w}{(I_0)_p}\right] \quad (2.16)$$

$$I_{sx}=\frac{(V_{BE})_{npn}}{R_{sx}}=\frac{V_0}{R_{sx}}\ln\left[\frac{I-I_{sx}}{(I_0)_n}\right] \quad (2.17)$$

are respectively the well and substrate current. In the case that both bipolar current gains are significantly larger than unity, the holding current relationship becomes the sum of the

base–emitter voltage of the pnp and npn transistor divided by the well, and substrate resistance, respectively. If the holding voltage is less than the supply voltage under normal operating conditions, a small current in the substrate can increase the SCR current beyond the holding current and trigger the SCR. This phenomenon is called latch-up and is one of drawbacks for SCR, as high trigger voltage or low turn-on speed. To reduce the trigger voltage of SCR device, it was invented a low-voltage-triggered SCR [21], while turn-on efficiency for ESD protection was improve with some circuit techniques (the gate-coupled [22], diode-triggered [23] and substrate-triggered [24]). Recent studies have been presented to find a solution for high holding voltage and latch-up concerns. The first one [25] is a protection concept realized with PMOS or NMOS triggered SCR devices with embedded MOS transistors (*FIG. 2.10*). In this case it is possible to have values of about 7 V for trigger voltage and 3 V for holding voltage.

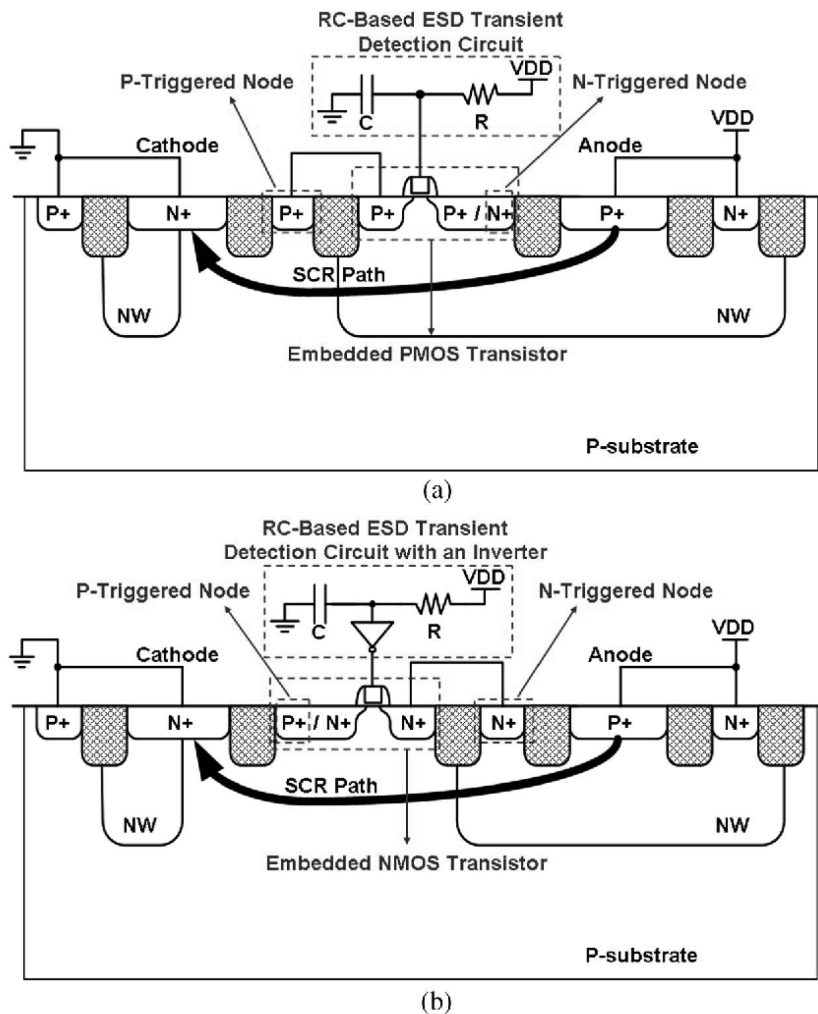


FIG. 2.10 Cross-sectional views of (a) the PMOS-triggered SCR device with RC-based ESD transient detection circuit and (b) the NMOS-triggered SCR device with RC-based ESD transient detection circuit and an inverter

A second solution [26] introduced a novel SCR based ESD protection device with high holding voltage (*FIG. 2.11*). In this case measured triggering voltage is 12.8V and holding voltage is 10V. Third solution proposed [27] is based on a novel dual SCR with triggering voltage of 7V and holding voltage of 4V.

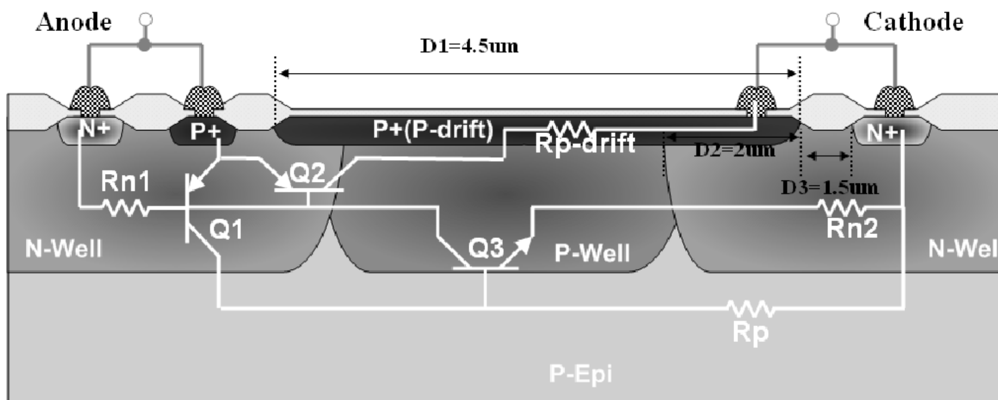


FIG. 2.11 Cross-sectional and equivalent circuit of proposed ESD protection device

2.3.3 MOSFET

MOSFET is maybe the most important snapback device in used CMOS technology. To understand its behavior we consider its simplest configuration in ESD protection applications, shown in next figure: the grounded gate configuration.

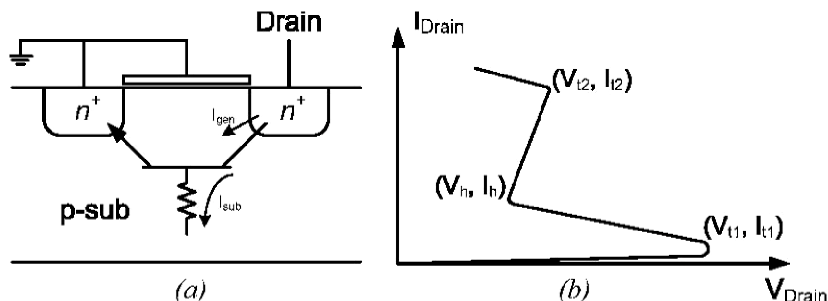


FIG. 2.12 Grounded-gate NMOS (a) cross section; (b) I-V characteristic

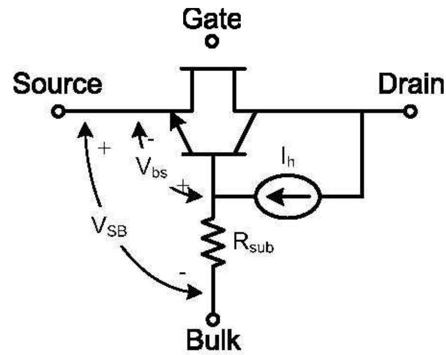


FIG. 2.13 Equivalent circuit for nMOS for high electric field

Under ESD stress conditions a parasitic bipolar transistor is formed in parallel with the drain and source diffusion. Therefore the collector is formed by the drain of the nMOS, the emitter is formed by the source, and the base is the substrate. As the drain current is increased the reverse-biased drain-substrate junction is initially in high impedance, then begins to gain to avalanche due to the high voltage across it. Practicaly there are generated electron-hole pairs, with electrons swept across the drain junction towards the drain contact and holes drift towards the substrate contact. So when the electric field increases in the transistor, avalanche multiplication increases leading to the generation term (I_G) in total current equation (2.18). In this expression, some of the hole generation current will serve as base current for the lateral bipolar element (I_B), while some of the holes generated will enter the substrate serving as substrate current (*FIG. 2.13*). The substrate current can then be expressed as in equation (2.19), as sum of a first term associated to avalanche multiplication and the base current:

$$I = I_{DS} + I_C + I_G \tag{2.18}$$

$$I_{sub} = (M-1)(I_{DS} + I_C) - I_B \tag{2.19}$$

In equation (2.19) the avalanche multiplication factor M can be related to the impact ionization coefficient integrated over the depletion width and can be expressed as

$$M=\frac{1}{1-\int \alpha dx} \tag{2.20}$$

Differently the avalanche multiplication factor M can be related to the avalanche breakdown voltage (2.21), showing that it can increase rapidly if the drain voltage approachs to this value.

$$M=\frac{1}{1-\left(\frac{V_D}{V_{AV}}\right)^n} \tag{2.21}$$

For ESD analysis, the substrate current is important because it is associated with the voltage drop that occurs locally in the MOSFET region under high current regime, due to the effective substrate resistance R_{sub}. As I_{sub} increases, the voltage drop equals the forward bias voltage of the p–n junction formed between the source and the substrate and MOSFET snapback occurs with the snapback condition.

$$V_{BE} \geq \left[(M-1)(I_{DS}+I_C)-I_B\right]R_{SUB} \tag{2.22}$$

Once the parasitic transistor turns on, the drain voltage decreases (changing from V_{t1} to V_h in *FIG. 2.12*) and a negative resistance region is observed because bipolar action generates more current and there is no need to keep the drain voltage at previous value to maintain the drain current. After snapback occurs the transistor is in a low impedance state and the voltage increases very little with current. The on-resistance of the parasitic transistor depends of:

- the increase of M (proportional to V_D) required to compensate a reduction in R_{sub} and β at high current
- the collector (drain) resistance
- the high-temperature effects on M, β, R_{sub} and the drain resistance.

The high increase of the current causes power dissipation with an increase in the temperature of the device. So a thermal breakdown, known as *second breakdown*, and silicon melting can occur when the thermally generated carriers become significant in comparison to the avalanche generated carriers. Analyzing MOSFET as an ESD protection device, under normal operating conditions the transistor is OFF and the current is very small. Under ESD conditions and when the voltage exceeds V_{t1}, the transistor will go into snapback mode and ESD current will be discharged through the device. In order to have an adequate level of protection are necessary the following requirements:

- V_{t1} must be less than the gate oxide breakdown voltage to protect the gate during an ESD event
- Voltage value for second breakdown must be greater than V_{t1} to ensure uniform triggering among fingers of GGNMOS. In fact the device is usually realized in a multi-finger configuration to reach the width of a few hundred microns required by ESD protection levels. This condition on voltage ensures that even if one finger triggers first, other fingers can be turned on before the first finger reaches the second breakdown region, degrading in any case the performance of the GGNMOS
- I_{t2} determines robustness of the ESD protection device and should be as high as possible
- V_h should be greater than V_{DD} to avoid that the device may turn on during normal operating conditions and lead to latch-up

About second requirement a recent study [28] have analyzed the influence of the positive and negative gate voltage for NMOS in ESD protection operation colcluding that, under appropriate gate bias, the ESD protection devices can obtain lower V_{tl} and higher V_{t2}.

Also HV MOS transistors have similar parasitic BJTs in their device structures. However they are difficult to use as protection devices in HV-MOS ICs due to the following difficulties:

- susceptibility to soft leakage degradation, that is a gradual increase in the drain leakage current caused by multiple ESD stresses, because of hot carrier trapping in the field oxide
- non-uniform current conduction

In the last years many studies have been realized to improve the MOSFET behavior, in particular to realize ESD-robust protection devices for HV-MOS ICs or to increase CMOS scaling. A solution for the first problem is a novel device with a shallow n^+ ballast region between the n drift region and the n^{++} drain region (shown in *FIG. 2.14*) that suppresses soft leakage degradation due to this ballast region [29]. In fact the avalanche generation occurs both in this ballast region and in the drain region, reducing current at the drain by splitting it into two parts.

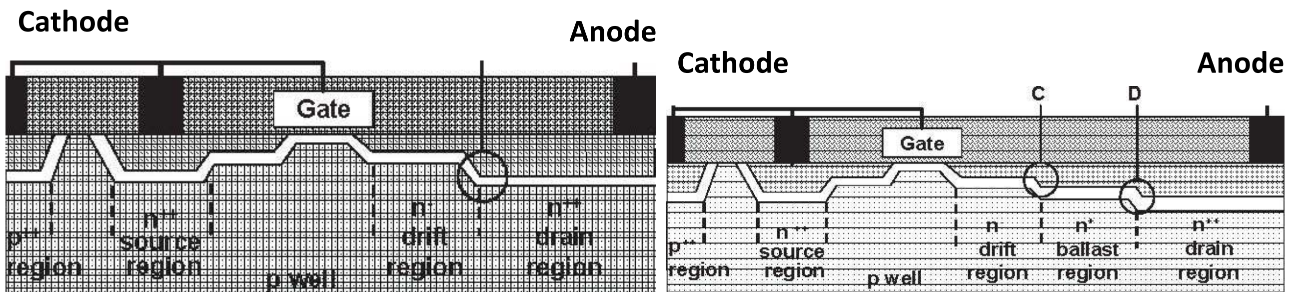


FIG. 2.14 A conventional HV MOS (left) ; proposed structure with ballast region (right)

2.3.4 Future

To improve the CMOS scaling below 22 nm node, in 2009 was presented first ESD result on FinFET devices implemented on bulk silicon wafers [30]. These devices, shown in figure 2.15 in comparison to devices fabricated on SOI substrate, have demonstrated to have an excellent robustness (a current for second breakdown of about 30 mA/µm for gate length of 22 nm, up to 9x compared to SOI device) and ESD-RF performances comparable to the best SOI FinFET diode.

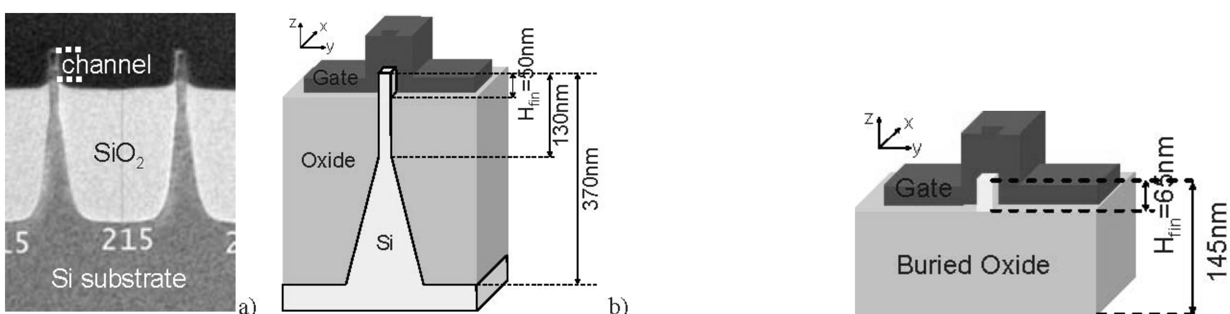


FIG. 2.15 On left: a) TEM and b) 3D schematic (not to scale) of a multi-fin bulk FinFET. On right: 3D schematic (not to scale) of a SOI FinFET.

Chapter 3

Transmission Line Pulser

Since 1985, when T. J. Maloney and N. Khurana discussed transmission line pulser (TLP) testing as a method for semiconductor I–V characterization and modeling, the interest in this test method is increased for its peculiarities. In 1997 J. Barth introduced the first commercial transmission line pulser (TLP) device simulator, leading to the acceptance of the TLP methodology for ESD sensitivity testing of semiconductors. In fact in 2004 ESD Association Device Testing Standards Committee initiated the transmission line pulser Standard Practice document, accepting TLP as a standard testing methodology in the semiconductor industry. Before speaking about fundamental implementations of TLP systems, a brief introduction on TLP operational principle and issues related to its implementation is necessary. It will be described as it is possible to measure leakage current and to calibrate the measurement system and, at the end of the chapter, the TLP-method correlation with others ESD models introduced in chapter 1, in particular the Human Body Model (HBM).

3.1 TLP : fundamentals and issues

The TLP-testing of integrated structures is based, as other test methods analyzed in chapter 1, on the generation of square pulses of selectable duration and amplitude to simulate ESD events. High voltages are necessary in order to generate current pulses of several Amperes, comparable with ESD events. The common method used to make it is based on the charging and discharging of the distributed capacitance, expressed in F/m, of a transmission line (TL). A transmission line is a waveguide with a characteristic impedance Z_0 that only depends on the material and the geometry of the conductors and the dielectric isolating them. Characteristic impedance can be obtained from equations (3.1) (3.2), known as telegraph equations, where l and c are the distributed inductance and capacitance respectively.

$$\frac{\partial V(x)}{\partial x} = -ZI(x) \quad , \quad Z = jwl \qquad (3.1)$$

$$\frac{\partial I(x)}{\partial x} = -YI(x) \quad , \quad Y = jwc \qquad (3.2)$$

Differentiating these equation we have equations (3.3) (3.4), with solutions (3.5) (3.6)

$$\frac{d^2V(x)}{dx^2} = ZYV(x) \qquad (3.3)$$

$$\frac{d^2I(x)}{dx^2} = ZYI(x) \qquad (3.4)$$

$$V(x) = V_+e^{-\Gamma x} + V_-e^{\Gamma x} \qquad (3.5)$$

$$I(x) = I_+e^{-\Gamma x} - I_-e^{\Gamma x} \qquad (3.6)$$

where $\Gamma = \sqrt{ZY}$.

Replacing (3.5) (3.6) in (3.1)(3.2) we obtain the equation $V_{+} = \sqrt{\frac{Z}{Y}} I_{+}$, so characteristic impedance is defined as $Z_0 = \sqrt{Z/_{Y}}$. Equations (3.5) (3.6) can be expressed now as

$$V(x) = V_{+}e^{-\Gamma x} + V_{-}e^{\Gamma x} \quad (3.7)$$

$$I(x) = \frac{V_{+}}{Z_0}e^{-\Gamma x} - \frac{V_{-}}{Z_0}e^{\Gamma x} \quad (3.8)$$

In this way it is possible to obtain the expression for impedance in the transmission line.

$$Z(x) = \frac{V(x)}{I(x)} = Z_0 \frac{V_{+}e^{-\Gamma x} + V_{-}e^{\Gamma x}}{V_{+}e^{-\Gamma x} - V_{-}e^{\Gamma x}} \quad (3.9)$$

For negligible losses, the electric and the magnetic field can be considered transversal to the direction of propagation. If a pulse travels along a transmission line, any discontinuity of the impedance $Z(x) \neq Z_0$ causes a partial reflection of the energy of the incident pulse. The reflection is of the same polarity as the incident pulse if the impedance difference $Z(x)$-$Z(x$-1) is positive and of opposite polarity else. In fact it is possible to find an expression for the incident pulse from (3.9) for x=0, shown in (3.10). Because (3.7) shows that the voltage value for each point of the transmission line is the addition of the amplitudes of incident and reflected pulses, it is possible to measure with a voltage probe these values (out of phase of a time t_{delay}). So it is possible to rewrite equations (3.7)(3.8)(3.10) as (3.11)(3.12)(3.13) respectively.

$$V_{-} = \frac{Z_L - Z_0}{Z_L + Z_0} V_{+} \quad (3.10)$$

$$V_L(t) = V_{incident}(t) + V_{reflected}(t - 2t_{delay}) \quad (3.11)$$

$$I_L(t)=\frac{V_{incident}-V_{reflected}(t-2t_{delay})}{Z_0} \quad (3.12)$$

$$V_{reflected}(t)=\frac{Z_L(t-t_{delay})-Z_0}{Z_L(t-t_{delay})+Z_0}V_{incident}(t-t_{delay}) \quad (3.13)$$

This effect is used for the characterization of unknown devices in the time domain reflectometer but must be minimized in the rest of the system. Each discontinuity in the impedance generates a reflected pulse that will continue to reflect itself throughout the line until it will be attenuated by losses. So, to obtain a better measure, the transmission line is adapted and the only discontinuity in the impedance is on the load. Principle shown in figure 3.1 is used to generate pulse (that simulate ESD event) for TLP-testing of integrated structures, in accord with transmission line theory.

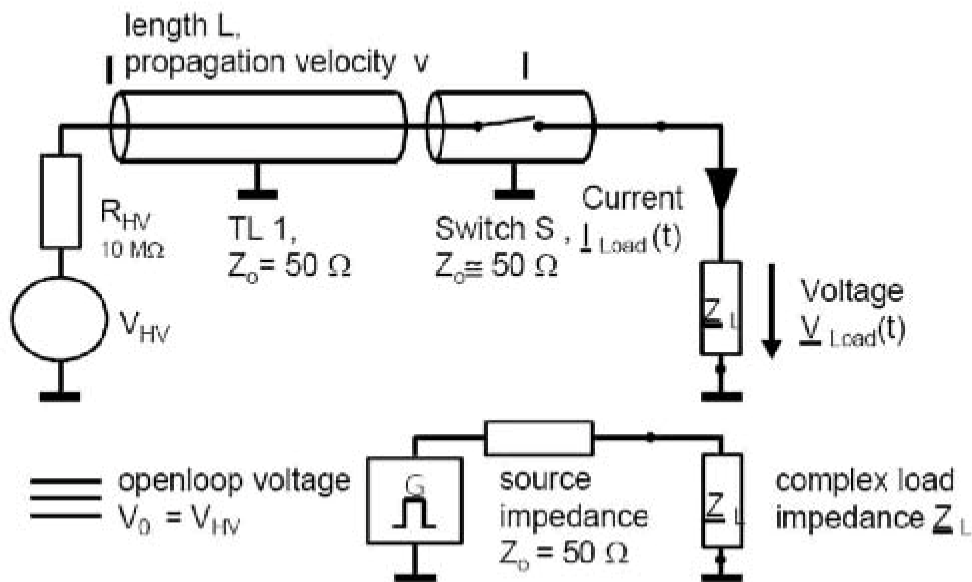


FIG. 3.1 Schematic of the TLP pulse generation section and its equivalent electrical model

An high-voltage source is used to charge the distributed capacitance of the transmission line TL1 via a high-ohmic resistor, while the coaxial switch S is in its open state. After the switch closes, the discharge of such a transmission line (TL1) into a resistive load or into TL2 produces a square pulse. The duration of the square pulse is equal to the length of the charged line divided by the velocity the signal propagates from the switch to the high-

ohmic end of this line and back to the switch (3.14). As an example, 10 m of the typical RG58 transmission line with a propagation velocity of 20 cm/ns generate a 100 ns long pulse [1].

$$\tau_p = \frac{2l}{s} \qquad (3.14)$$

The amplitude of the voltage pulse V is determined by the pre-charge voltage V_0 and the impedances of the source Z_s and the load Z_L:

$$V = V_0 \frac{Z_L}{Z_L + Z_S} \qquad (3.15)$$

For a matched impedance in the switch and the load, the amplitude of the voltage pulse would be half of the pre-charge voltage.

Regarding the measure process, when are obtained measurements for reflected pulse, it is possible to calculate (thanks to Ohm's law) the impedance of DUT by equations (3.11)(3.12). Furthermore, it is useful to make a measure of leakage current to evaluate device degradation. For this measure we can use a parameter analyzer to polarize the DUT with a defined voltage value, enabling TLP to evaluate the leakage current after each discharge. Necessary equipment for TLP measurement system are:

1. High-voltage generator (HV-DC)
2. Oscilloscope
3. Parameter Analyzer (Source Measure Unit for leakage measurement and for optional additional voltage bias of the DUT)
4. Controller
5. Current and voltage probes
6. Relay switch and its control
7. Probe station with needles to contact wafer

Software controls the equipment and extracts the actual current through a device I_{DUT} (t) and the voltage across the device V_{DUT} (t) and derives the various data from the measurement. In figure 3.2 is explained, for the example of a snapback protection element, the principle and terminology of the *quasi-static* pulsed device characterization.

Practically a series of increasing magnitude square pulses is generated and I-V values at every pulse are obtained by means of averaging a certain region in the second half of the transient waveform, where the TLP waveform is steady (usually at about 50~60 ns of 100 ns time pulse for TLP). A recent study [31] has found that it is very important to choose TLP-IV extraction timing for ESD parameter extraction, as shown in *FIG. 3.3* .

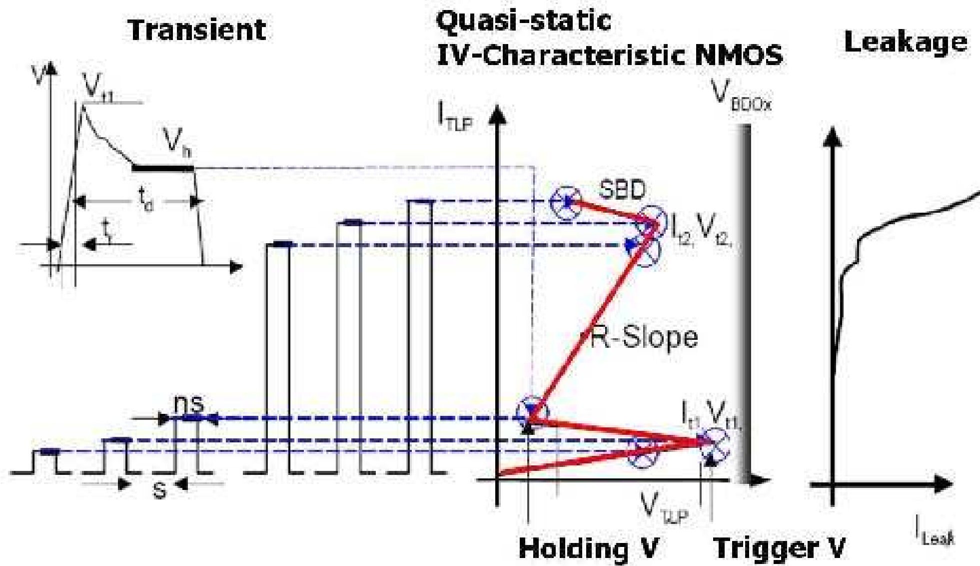


FIG. 3.2 Principle of the pulsed characterization with a series of increasing magnitude square pulses. I-V values at every pulse are obtained by means of averaging a certain region in the second half of the transient waveform

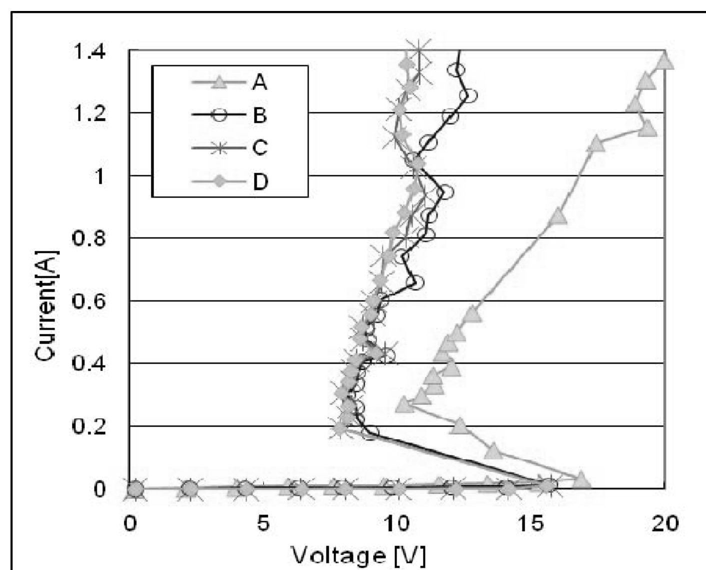


FIG. 3.3 ESD parameter location extraction of NMOS breakdown characteristic. Period after snapback: A 0~10ns , B 20~30ns , C 30~40ns , D 40~50ns

Then the software shows in real time an I-V graph (as in *FIG. 3.4*) with values, obtained increasing the device stress voltage, for leakage current and DUT parameters (voltage and current).

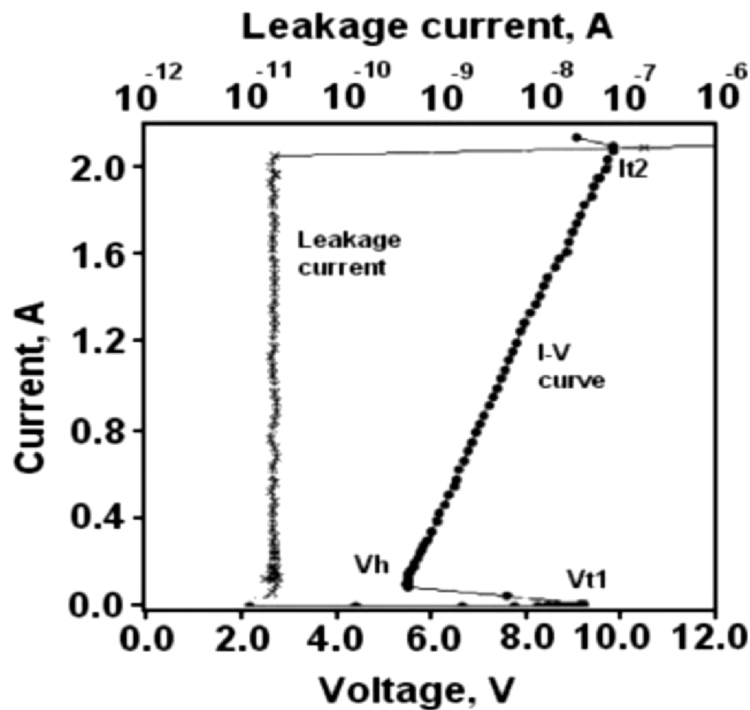


FIG. 3.4 Typical TLP breakdown I-V characteristics and leakage current curve

Fundamental issues that can occur in practical measure are:

- deviations from the ideal square shape of the pulse resulting from resistive and dielectric losses that are frequency-dependant as well as from variations in the impedance along the line through the whole system.
- the homogeneous turn-on of protection devices and consecutively their clamping and failure thresholds may depend on the rising edge.
- the repeatability of the switching relay over the full voltage range

To improve the first issue it is mandatory to employ cables and components that are well matched, as short as necessary, and with low losses throughout the whole system. Particular attention is necessary for the interconnection between the TLP-generator and both probe needles (which have no controlled impedance), that must be kept to a minimum of few centimeter and also be placed in place for calibration (analyzed in next section). Additional parasitics affect also the initial *dV/dt* at low currents, with effects on turn-on and snapback voltage of DUT [32]. Because a low series resistance by means of a metallic contact should be established instantaneously and be maintained for the full duration of the pulse and possible reflections, a lower amplitude with a trailing pulse of the same polarity or even steps on the top of the pulse can be found. Besides the shorter the pulses become, the more emphasis need to be put on the impedance of the signal path. However, a dedicated long transmission line may be employed to tailor the rise time in order to comply with HBM or MM test models.

The second issue could be the relay switch. Implementations with a Reed relay surrounded by a metal sleeve or cylinder are commonly in use, although with standard dimensions of commercially available Reed relays the impedance is in the order of 60 Ω. At least, for a significant pulse duration, for example 100 ns, the resulting degradation of the leading corner of the pulse top and after the falling edge is acceptable [1].

Third issue is related to choose of the rights relays, attenuators, and other components for TLP system. This choice is not always easy and cheap, in particular for coaxial components explicitly rated for high voltages.

Just before the fundamentals and different setups for the generation and measurement of the square pulses are compared, a brief analysis for the measure of leakage current and the calibration of measure system is necessary for their importance in characterization of ESD protection structures.

3.2 Measure of leakage current and calibration

As we have said, the measure of leakage current with a parameter analyzer after each discharge is very important to evaluate device degradation. The parameter analyzer makes a DC analysis on DUT forcing a dc voltage on it and recording current that flows through it. These values are saved by a control software with voltage values on DUT after each TLP pulse. So it is possible to graph these values together, appending the curve of leakage current on I-V characteristic (*FIG. 3.4*). The leakage current has very low values until the device breaks, then its value increases drastically. This increase is also related to a change in the I-V curve behavior, so in device impedance, showing a damage in the DUT. Other example is shown in *FIG. 3.5* where, for a I_{DUT} of about 3.72 A and a V_{DUT} of about 11.17 V, the leakage current pass from 9.06 nA to 1 mA, value defined as “compliance” for parameter analyzer. In this case the voltage value chosen to make the leakage current measure is 1.8 V, in accordance with a previous DC analysis of the device.

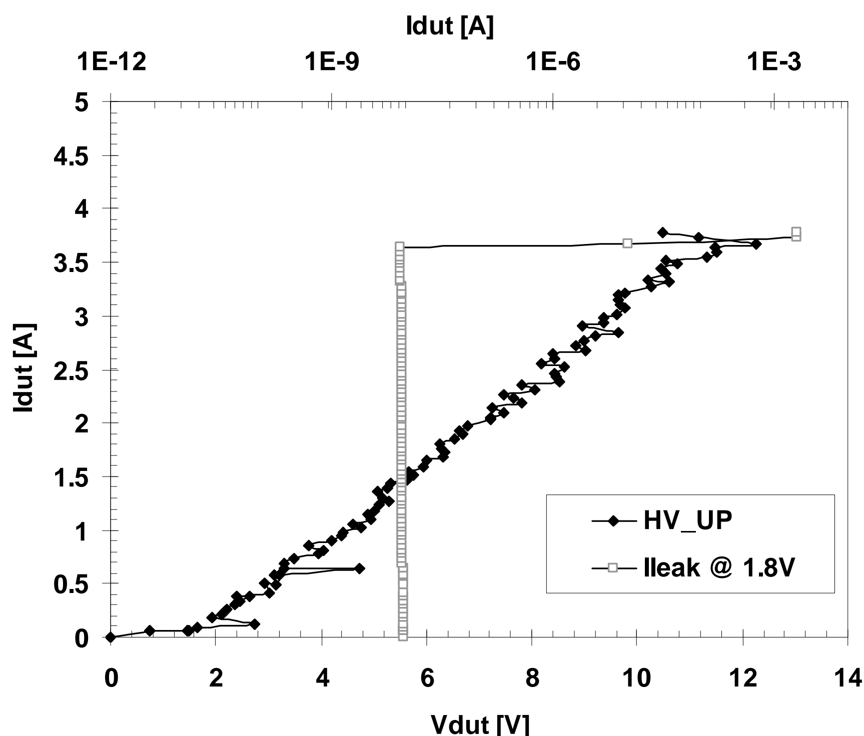


FIG. 3.5 Measure of leakage current and I-V characteristic for a MOSSWI

Observing the previous figure the measure of leakage current can seem unneeded to define the break point for DUT because of change in I-V behavior. Actually, as shown in *FIG. 3.6*, the change in I-V behavior is not always present, in particular for well balanced protection structures [33]. In this case the leakage current increase its value from about 9.7 nA to compliance value, even if for corresponding voltage and current values (about 9.8 V and 5.9 A respectively) it could not seem that DUT is broken (I-V characteristic do not show the second breakdown point).

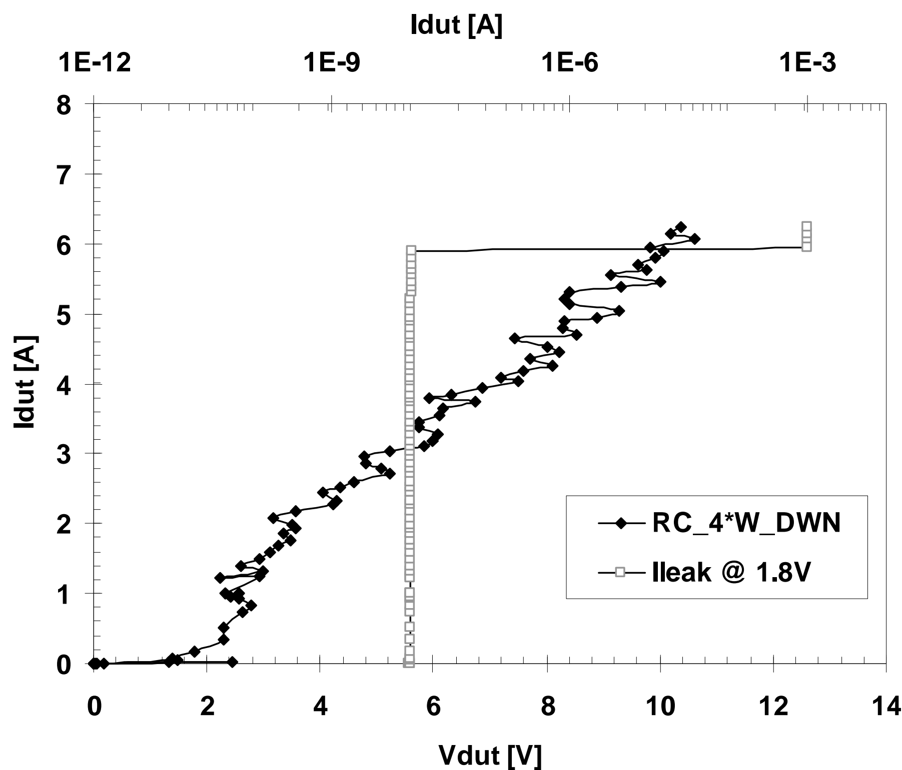


FIG. 3.6 I-V characteristic for a MOSSWI that don't show device's breaking point

In next example (*FIG. 3.7*) are shown two important phenomena that can occur in leakage current behavior. For very low values of I_{DUT} (about 0.15 A) we have a progression in the leakage curve typical of a "soft failure". The increase from about 1 nA to 24 nA signals a damage on protection structure, impossible to see in I-V behavior. So, without leakage current curve, it would be defined an incorrect value for device breaking point. In case of soft failure the structure design should be made on its voltage value, not on second breakdown voltage [34]. Another phenomenon impossible to see in I-V behavior is the continuous increase in leakage current value already for very low I_{DUT} values (about 0.2 A), indicative of a bad protection structure design.

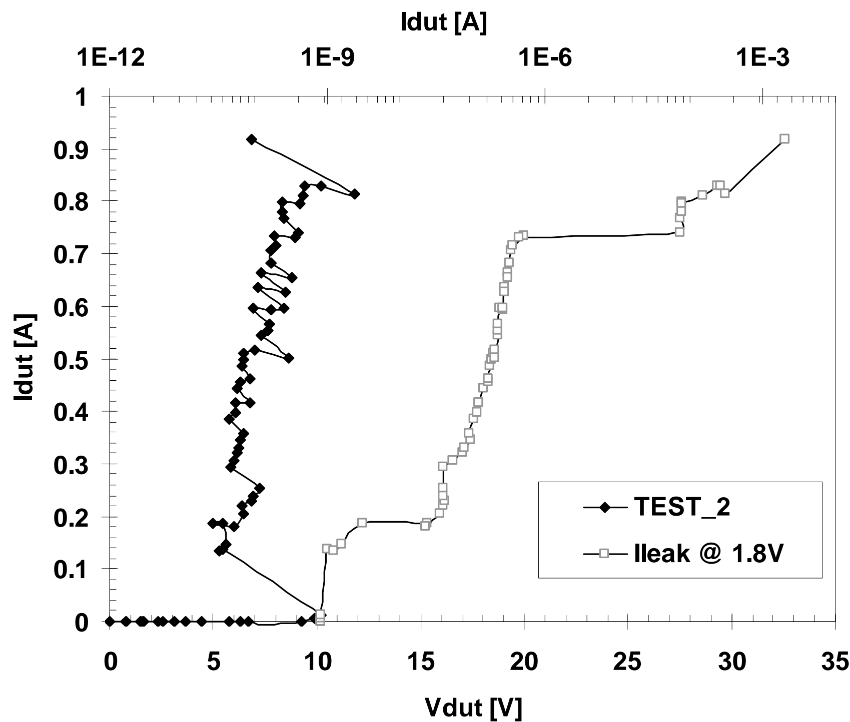


FIG. 3.7 Leakage current behavior : soft failure and device's degradation

Depending on the setup and the device to be stressed, electromagnetic interference between the stress terminals and control terminals of the DUT can become an issue. As we have said in previous section a first issue is the elimination or attenuation of multiple reflections, which may cause additional stress to the DUT. For each TLP type, the appropriate calibration technique must be applied in order to gain the correct attenuation factors of the system. An example to obtain a good calibration for a TLP test exact and repeatable is the SOL (short, open, load) method [33]. Practically three TLP measures are made on a short circuit, an open circuit, and a load of 5 Ω with a network analyzer. Measure values are corrected to obtain a characteristic without oscillations vertical (in case of short circuit), equal to zero for each voltage value (in case of open circuit), with an angular coefficient of 1/5 (in case of 5 Ω load). Testing on the wafer, also the *contact resistance* of the probe needles to the pads must be included in the calibration. On this resistance there is a voltage due to discharge current that can alter the result. The error can be very important for measurements of devices with impedance values from 1 to 5 Ω [33]. Furthermore the oxide that forms on wafer pads and on needles can modify measurements with time, so a frequent calibration of the equipment is required. The compensation of contact resistance used in this work provides for a subtraction of voltage due to discharge current across needles on voltage value measured by voltage probe (equation (3.16)).

$$V_{DUTreal}(t) = V_{DUTmeasured}(t) - R_{correction} * I_{DUT}(t) \qquad (3.16)$$

$R_{correction}$ is measured proceeding from *contact resistance* with the following process :

- probe needles are put on the same pad of the wafer under test, without direct contact between them
- with a parameter analyzer is made a DC measure for very low current and voltage value, avoiding to damage DUT
- from I-V characteristic obtained is possible to calculate a value of resistance, adopted as $R_{correction}$

Making a TLP measure we will expect an I-V characteristic coherent with short circuit condition. Really we will not obtain vertical characteristic due to another parasitic components not detected by parameter analyzer, in particular a resistance due to current probe, as shown in *FIG. 3.8* (before calibration). To obtain the correct calibration we can calculate the resistance in TLP measure (in this example 1 Ω), adding this value to previous correction for resistance measured with parameter analyzer ($R_{correction}$). A second TLP measure will show the good quality of calibration (*FIG. 3.8* - before calibration).

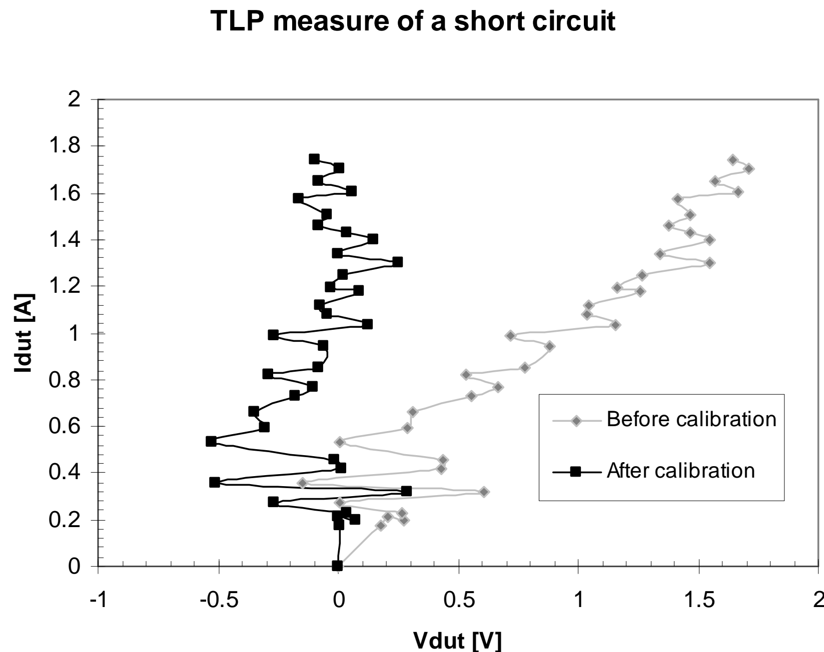


FIG. 3.8 Calibration of a TLP on needles system after DC correction with parameter analyzer

Even if this result seems to be not coherent with short circuit condition, really it is satisfactory because the shift from the vertical line is very contained. To improve this method (named linear compensation, because it uses only one resistance value to make calibration) we have used a sequential compensation, where the compensation is made with different values associated each one to a short current range [31]. The improvement in measure precision is shown in next figure.

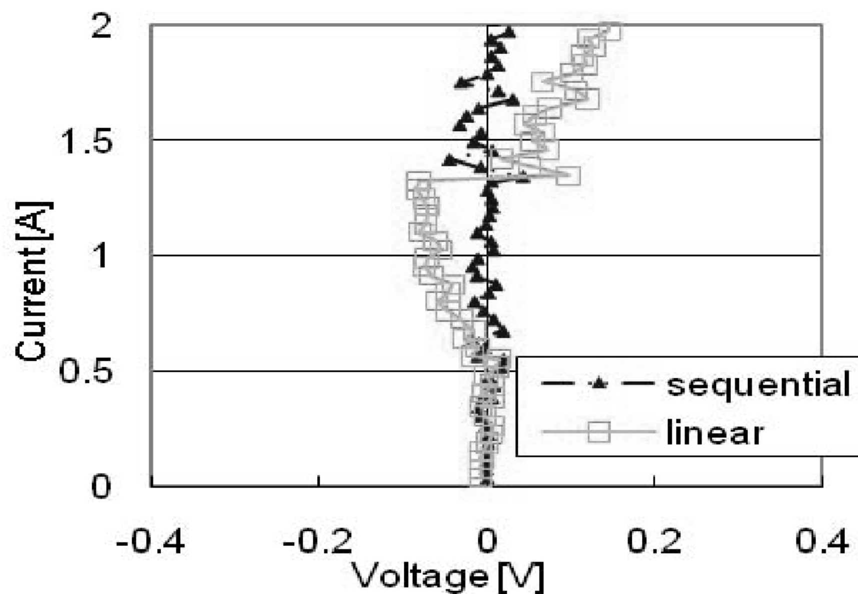


FIG. 3.9 The comparison data of the sequential and the linear compensation

In conclusion is important to observe that needles have also an inductive parasitic component that induce overshoots in rise front of voltage pulse. These overshoots can result in a more rapid failure or in a break at lower voltage value for DUT. Previous method are not able to attenuate effects of an inductive parasitic component. Only in presence of several samples for current and voltage waveform and an adequate band width for probes and oscilloscope (about 1 GHz) is possible to study these effects.

3.3 Implementations of TLP-system

In this paragraph we will analyze fundamental implementation of TLP-system described in previous sections. In particular we will discuss about schematics and operational principles of current source TLP, Time Domain Reflectometer TDR-TLP, Time Domain Transmission TDT-TLP and Time Domain Transmission TDT-TLP.

3.3.1 Current Source TLP

The *Current Source TLP* is mainly used to simulate HBM-stress by means of a 100 ns wide pulse at the package level. This kind of TLP, shown in *FIG. 3.10*, is characterized by the termination resistor and the source resistor that forces the current through a low ohmic DUT.

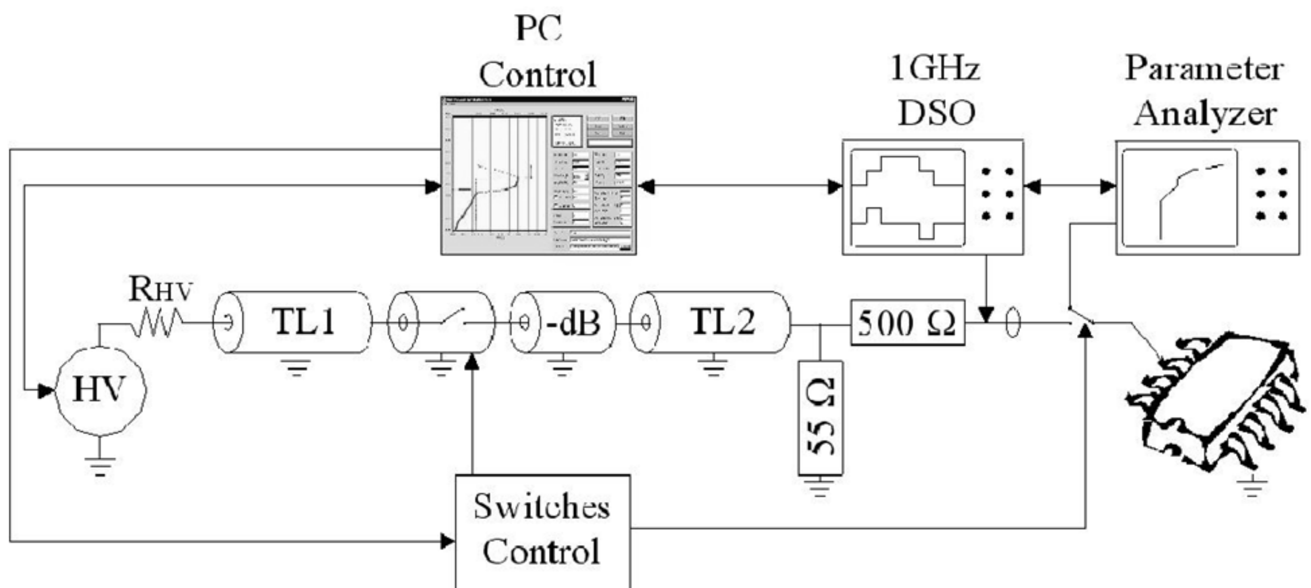


FIG. 3.10 Schematic of the current source TLP R_S = 500 Ω

Resistance R_s= 500 Ω generates current level to apply at DUT (because its resistance is very low), turning voltage in current pulse. In this way the transmission line is not adapted, so the insertion of resistance R = 55 Ω changes the equivalent resistance of the line in a value of about Z_0 , minimizing the reflection coefficient. Voltage and current are measured independently as close as possible at the DUT, making the method rather tolerant to pulse variations. An expression for voltage and current pulse amplitude is

$$V_P = \frac{HV}{2} \tag{3.17}$$

$$I_P = \frac{HV}{2\,(R_S + R_{DUT})} \cong \frac{HV}{2R_S} \tag{3.18}$$

Additional switches disconnect the DUT from the stress circuit and connect it to the DC-parameter analyzer. High parasitic elements at the DUT slow the achievable *dV/dt* and increase the probability for ringing. The matched termination eliminates multiple reflections between the open end of TL1 and the DUT. The oscilloscope and the probes determine the accuracy nearly independent from the load impedance Z_{DUT}. For low DUT voltages associated with low ohmic protection elements, the voltage probe should be placed between the current probe and the DUT. Otherwise, all measured and applied DUT-voltages require correction for the dynamic impedance of 1Ω in the ground path. Resistors with low inductance can be used to verify the system. Anyway this TLP system can generate current pulses up to 4 A, so other kind of implementation are necessary to analyze devices at higher current values.

3.3.2 Time Domain Reflectometer TDR-TLP

The *Time Domain Reflectometer* TLP is based on the fact that if an incident square pulse reaches the DUT at the end of a transmission line, it will be reflected depending on the impedance $Z_{DUT}(t)$ of the DUT relative to the impedance Z_0 of the transmission line (look at equation (3.13) rewritten next).

$$V_{reflected}(t)=\frac{Z_{DUT}(t\text{-}t_{delay})\text{-}Z_0}{Z_{DUT}(t\text{-}t_{delay})+Z_0} * V_{incident}(t\text{-}t_{delay}) \tag{3.19}$$

This setup can maintain the 50 Ω impedance from the generator to the device with minimum parasitic elements and pulse distortion. *FIG. 3.11* shows the schematic of the TDR-TLP, and in *FIG. 3.12* a detail of the behavior of the waveforms incident to and reflected from the DUT.

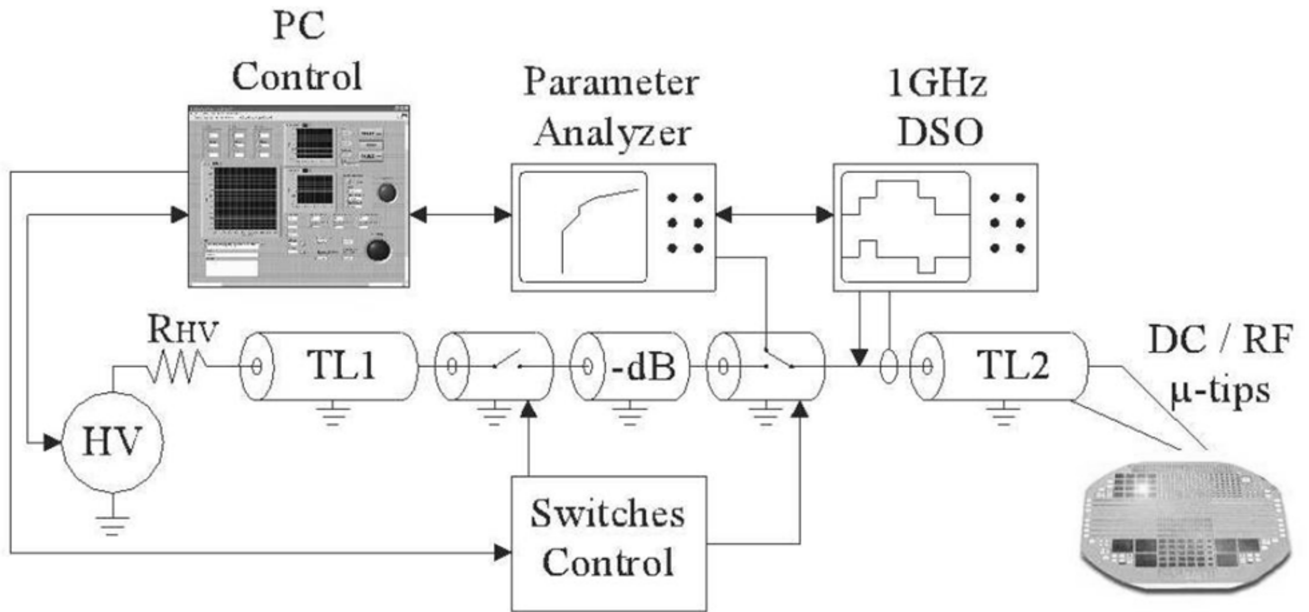


FIG. 3.11 Schematic of the Time Domain Transmission TLP

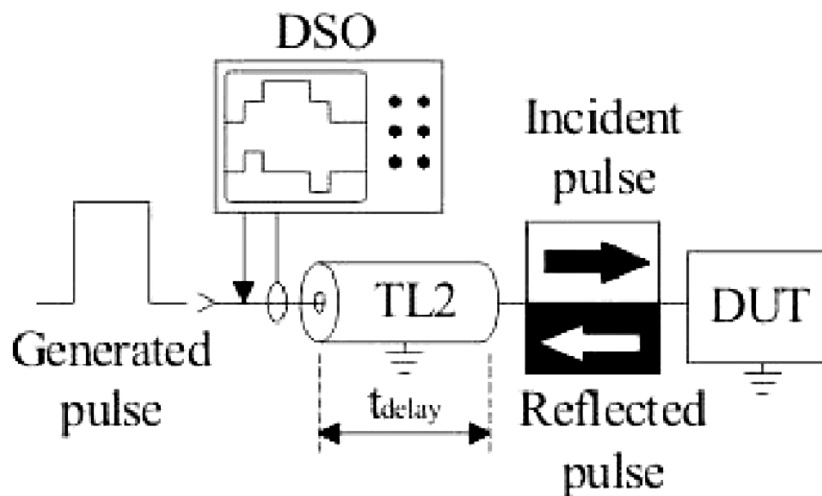


FIG. 3.12 Detail of the behavior of the waveforms incident to and reflected from the DUT

The *Time Domain Reflectometer* TLP can be realized also in a different configuration, with a current transformer (CT) in the signal path (*FIG. 3.13*). This system uses an oscilloscope with two channels and measures voltage and current reflected from the DUT independently with the accuracy provided by the probes and the oscilloscope after a calibration of the attenuation factors of the system. Alternatively, for a known impedance Z_0, the current I(t) can be calculated from the relations (3.20) (3.21), for incident and reflected pulse respectively.

$$I(t) = \frac{V_{incident}(t)}{Z_0} \tag{3.20}$$

$$I(t) = -\frac{V_{reflected}(t)}{Z_0} \tag{3.21}$$

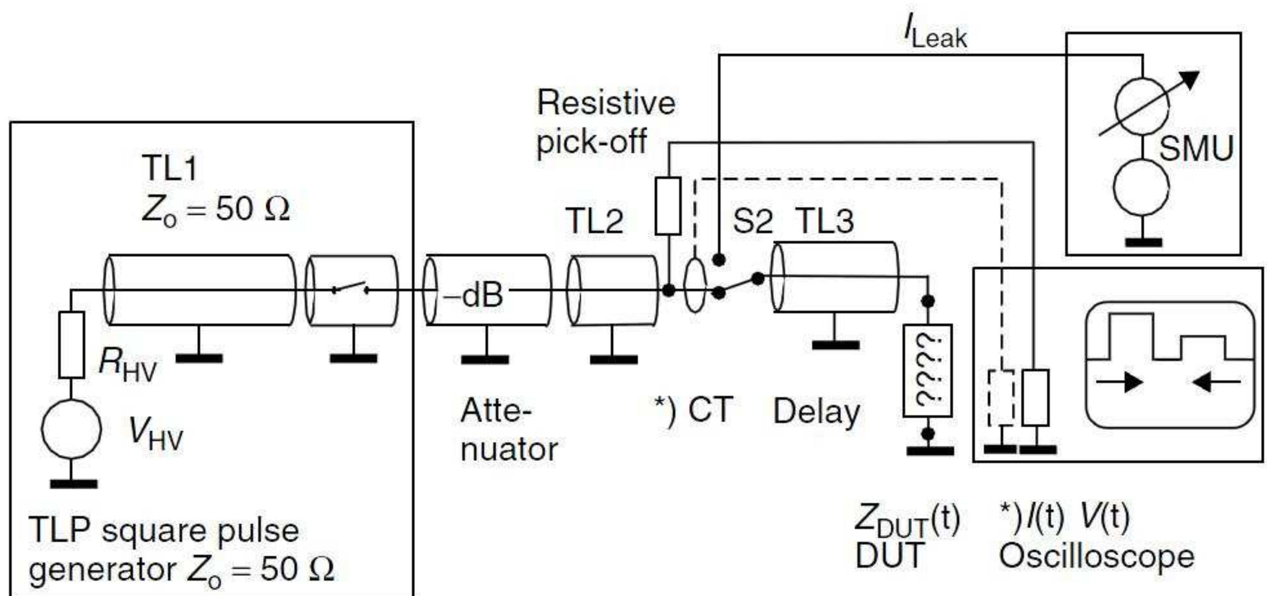


FIG. 3.13 Schematic of the Time Domain Transmission TLP with a current transformer (CT) in the signal path

The transmission line TL3 between the resistive pick-off and the DUT delays the reflected pulse with respect to the incident pulse. Voltage $V_{DUT}(t)$ and current $I_{DUT}(t)$ at the DUT are calculated from the measured incident and reflected voltage pulse after a shift of the

reflected pulse to the left by twice the one-way delay time t_{delay} and a correction for the attenuation of the resistive voltage pick-off and transmission lines, using the following equations:

$$V_{DUT}(t) = V_{incident}(t) + V_{reflected}(t - 2t_{delay}) \tag{3.22}$$

$$I_{DUT}(t) = \frac{V_{incident} - V_{reflected}(t - 2t_{delay})}{Z_0} \tag{3.23}$$

Some uncertainty results from numerical effects for DUT impedances close to open and short and from distortion on the delay line TL3 in the phase of transition. Calibration to 0 Ω and a resistor together with correction improves the accuracy. If the reflected pulse is not completely separated from the incident pulse, the incident pulse must be very repeatable and flat. An attenuator between the pulse generator and the DUT is recommended in order to reduce multiple stress caused by multiple reflections that depend on the DUT impedance. To reduce reflections from low-impedance devices is possible to employ a diode in series with a termination resistor at the open end of the transmission line. This termination, that may even be switched in order to generate bipolar pulses, depends on polarity and should not be used for the characterization of oxides. A coaxial relay in the delay line allows to connect a DC-parameter analyzer to the DUT.

3.3.3 Time Domain Transmission TDT-TLP

The *Time Domain Transmission* TLP avoids the uncertainties associated with the dispersion of the reflected pulse signal (see *FIG. 3.14*). However, it requires that first a reference voltage pulse $V_{chg}(t)$ is captured for every voltage step without a DUT in place. In this condition the voltage $V_{chg}(t)$ equals the measured voltage $V(t)$, considering the attenuation factor *a*. Then the device is inserted in the fixture and the resulting pulses $V_{DUT}(t)$ are captured for the same pre-charge voltage levels.

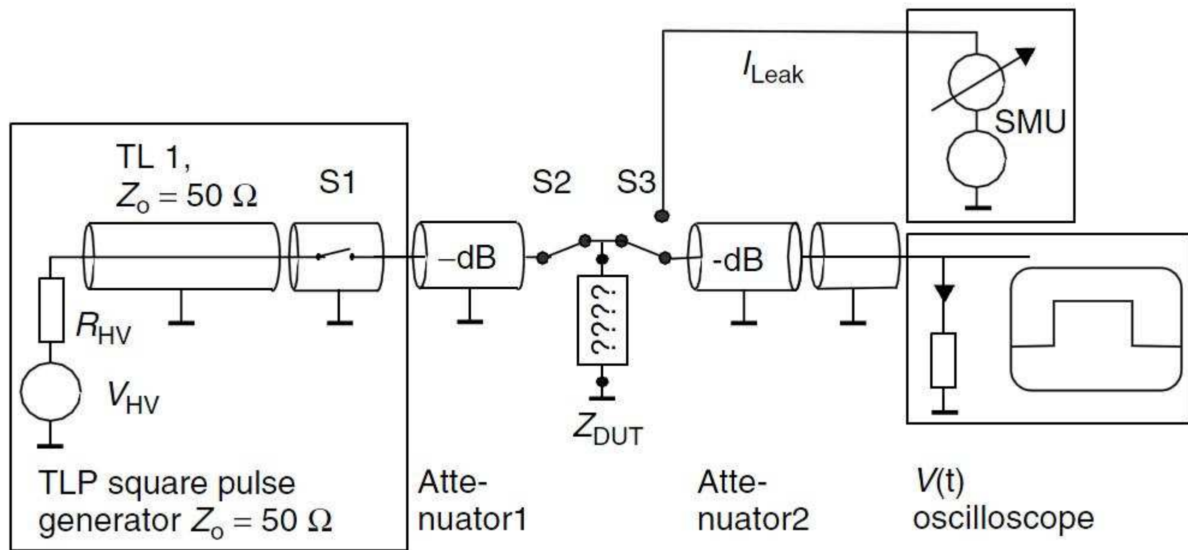


FIG. 3.14 Schematic of the Time Domain Transmission TLP

This method can also be implemented with minimum parasitic elements and in particular distortion. The impedance of the relay in the conductive stage is constant and repeatable, generating repeatable pulses in the full voltage range. An attenuator between the pulse source and the DUT reduces multiple reflections and stabilizes the source impedance Z_0. For the first pulse of a series of decaying reflections the following equations are used to calculate the current through the DUT from the directly measured voltage $V_{DUT}(t)$ attenuated to an amplitude safe for the oscilloscope:

$$Z_{DUT}(t) = \frac{V_{DUT}}{V_{chg}(t) - V_{DUT}(t)} * Z_0 \qquad (3.24)$$

$$I_{DUT}(t) = \frac{V_{DUT}(t)}{Z_{DUT}(t)} \qquad (3.25)$$

Two relays are necessary in order to isolate the DUT for leakage measurements between stress pulses.

3.3.4 Time Domain Transmission Reflectometer TDTR-TLP

The *Time Domain Transmission Reflectometer* TLP embeds the DUT between the center conductors of two transmission lines of equal length and requires a two-channel oscilloscope. A schematic of the TDTR-TLP is shown in *FIG. 3.15*.

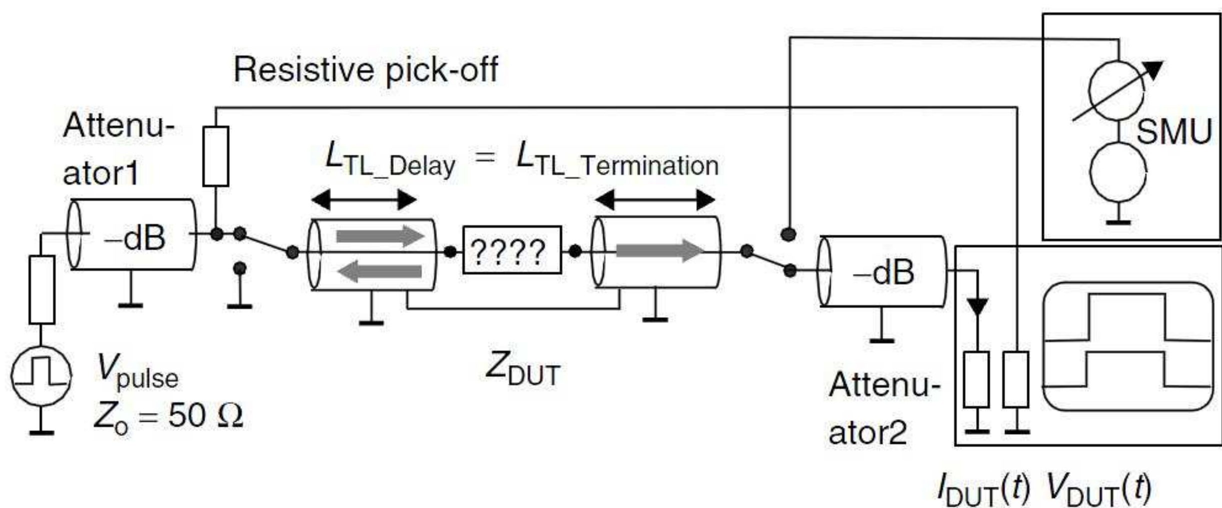


FIG. 3.15 Schematic of the Time Domain Transmission Reflectometer TLP

The grounded outer conductors of the two lines are connected to each other. The equal length of the lines is necessary in order to align the transmitted and the reflected signal on the screen of the oscilloscope. The length of the delay and termination line should exceed the length of the pulse generating TL1 in order to separate the reflected from the incident pulse at the pick-off. Employing equation (3.26), the voltage $V_{DUT}(t)$ is calculated from the reflected pulse considering the attenuation factor of the pick-off and the transmission lines. With equation (3.27) the current $I_{DUT}(t)$ is calculated from the transmitted pulse voltage at the 50 Ω input resistor of the oscilloscope.

$$V_{DUT}(t) = a * 2 * V_{reflDUT}(t) \qquad (3.26)$$

$$I_{DUT}(t) = \frac{V(t)}{Z_0(t)} * Z_0 \qquad (3.27)$$

Both signal may need some additional attenuation. This system has a source impedance of 100 Ω, as the DUT is in series with the 50 Ω line connected to the oscilloscope. Although even a short does not generate reflections of opposite polarity, an attenuator between the pulse generator and the pick-off is recommended. In order to test the leakage, additional coaxial relays may be necessary for DC insulation. The calibration of the system is done at least with a short. With the symmetrical outline of the controlled impedance paths, this TLP method has a high potential for an implementation in an automated multipin TLP-test system.

3.4 Correlation with other ESD test methods

TLP is nowadays the preferred test method to run ESD tests on semiconductor devices, so it is very important to know its features in order to correlate the test results to the different standard models. As we have said, it implements a square waveform with controlled amplitude and time length, expressed by equations (3.28) (3.29)

$$\tau_p = \frac{2l}{s} = l * 10\ [ns/m] \qquad (3.28)$$

$$V = V_0 \frac{Z_L}{Z_L + Z_S} \qquad (3.29)$$

where V_0 is the pre-charge voltage and Z_s, Z_L are respectively the impedances of the source and the load. This characteristic allows to equal the energy value among different models. In fact, even if could seem that there is no correlation among TLP and other ESD models looking at their waveforms (*FIG. 3.16*), is possible to obtain the charge voltage V_{Geq} that equals specific energies of several models to a defined model [35]. In following table is shown the comparison with HBM specific energy, obtained by equation (3.30).

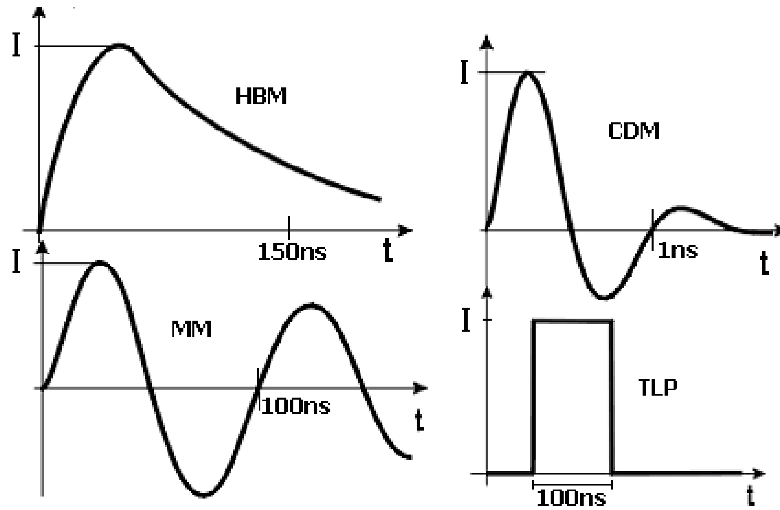


FIG. 3.16 Waveforms of some ESD models

$$V_{Geq} \cong \sqrt{\frac{E_{HBM}}{E_{model}}} * V_{Gmodel} \tag{3.30}$$

Model /Standard	E_{model} [μJ/Ω]	V_{Geq} (E_{HBM}) [KV]
HBM / MIL-STD-883G	0.13	2
HM-HBM / ANSI C63.16	2.12	0.5
HBM 4• / MIL-STD-883G	0.1	2.3
MM / EIA/JESD22-A115-A	1.07	0.14
CDM / ESD STMS 3.1	0.02	1.3
TLP	0.4	0.58

FIG. 3.17 Comparison of specific energies for ESD models

Looking at the HBM qualification test of the product, the TLP pulse must have a width of 75 ns to equal the HBM typical pulse energy with a decay time constant of 150 ns [36]. Measures on devices under ESD effect have shown that a good value for width of a rectangular TLP pulse is 100 ns, because of same damages and peak value in current waveform (as shown in *FIG. 3.18*). Moreover, values in *FIG. 3.19* show that TLP current for 100 ns pulse width provides a similar equivalent voltage of HBM model if it is multiplied by 1.5 KΩ (the HBM resistance value) [37].

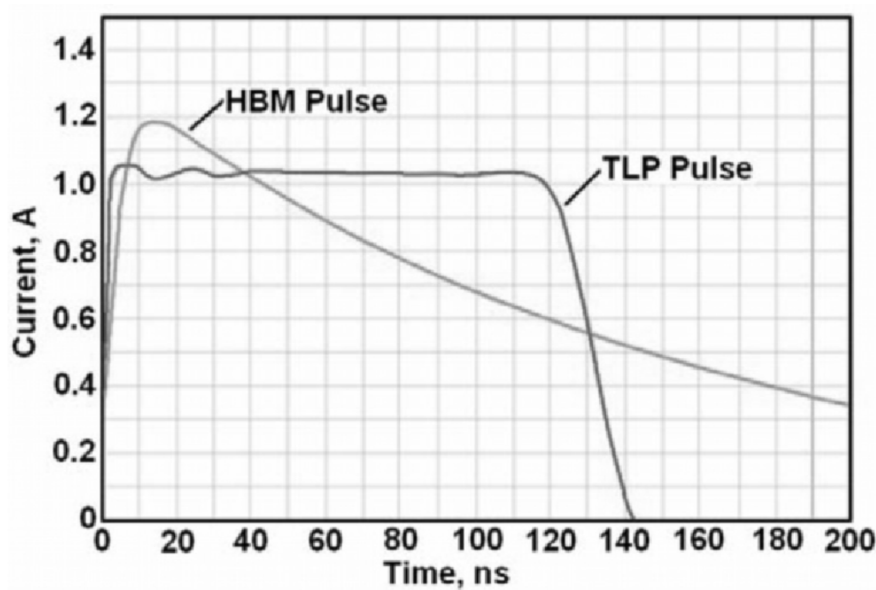


FIG. 3.18 HBM pulse vs. TLP pulse

	V (HBM) [KV]	*I (HBM) [A]*	*I (TLP) [A]*
Device #1	1.9 ± 0.3	1.2	1.25
Device #2	2.7 ± 0.4	1.8	2.25
Device #3	1.1 ± 0.2	0.7	0.7
Device #4	1.25 ± 0.3	0.8	0.7
Device #5	2.3 ± 0.25	1.5	1.2

FIG. 3.19 Correlation between HBM and TLP current values, for different HBM voltages and devices

Rise time of TLP pulses used in this correlation with HBM model can change from 2 ns to 10 ns, with also a possible variation of ±10% of the current peak. This parameter can strongly influence the correlation because modifying it the needed current to make same damages on DUT would change. For example the correlation factor (HBM/TLP) can pass from 0.21-0.27 to 1.43-1.71 (according to device dimensions), changing rise time from 0.2 ns to 10 ns (look at *FIG. 3.20*) [33]. In view of equivalent turn-on characteristics and energy-related failure mechanisms, TLP-pulse with a rise time in the order of 5 ns and a pulse duration of 100 ns are typically used. They translate 1 A into almost 1.5 kV HBM.

Device type / W	***HBM [KV]***	***TLP 0.2ns***		***TLP 10ns***	
		[A]	*HBM / TLP*	*[A]*	*HBM / TLP*
1 / 50µm	1.0	4.1	0.24	0.6	1.66
2 / 50µm	0.9	4.2	0.21	0.63	1.42
3 / 50µm	1.2	4.4	0.27	0.7	1.71
1 / 100µm	1.8	8.3	0.21	1.2	1.5
1 / 100µm	2.1	8.5	0.24	1.3	1.61

FIG. 3.20 Correlation's factor HBM / TLP changing rise time

A recent study [38] has compared HBM and TLP methods showing that pulsed measurement methods like TLP testing are not always a suitable tool to fully assess the ESD performance of devices or circuits. For many applications, it is needed to study the device behavior in an environment, which is much closer to the ESD events occurring in nature. In fact in nature there are no ESD environments which are terminated with the 50 Ω termination of TLP test systems. One of these more realistic ESD characterization methods is just HBM. The use of HBM on-wafer measurements allows a full characterization of a component under ESD stress conditions, including its quasi-static and transient behavior. The different setup of HBM testers simulates more realistic ESD events than a pulsed measurement method like TLP.

About correlation with other test methods, researchers have attempted to correlate the TLP measurement results with CDM testing that, due to the completely different current and time domain, does not correlate well with HBM and MM models. For example, the correlation coefficients between CDM-HBM and CDM-MM are respectively 0.28 and 0.42 [8]. But, given the fast rise and fall times, the TLP techniques should give to designers a

better understanding of the dynamic effects such as trigger speeds and transient currents under ESD CDM type conditions. However, there is the fundamental difference between these methods because CDM is a one pin test, while TLP requires the selection of two IC pins. Therefore, the ESD discharge path for both CDM and TLP are different within an IC. To deduce CDM relevant parameters of the ESD protection design, such as the transient voltage response, it is possible to use the very fast TLP (vf-TLP). This technique complies with necessities to apply equivalent conditions to the device under test and to have a high enough resolution to define the transient behavior of the device. In this system, a square pulse of short duration and rapid rise time, typically it is used a pulse width of 10 ns (but also other widths as 3.5 ns are used) with a rise time of 750 ps, is applied to the device under test by discharging a pre-charged transmission line into the load device. This incident pulse is reflected at the device under test. Typically, the average current and voltage over the time interval between 65% and 95% of the pulse width is used to determine a single IV data point at the vf-TLP IV characteristics. It was found that the failure voltage of CDM is between 6 and 8.5 times higher than the vf-TLP (3.5 ns pulses) failure voltages. The failure current threshold of vf-TLP is from 1.3 to 1.7 times higher than the CDM failure current [39]. Generally, the correlation of vf-TLP testing with the CDM testing is achieved in terms of the failure signature. The failure thresholds of vf-TLP and CDM do not correlate due to the different current paths.

Chapter 4

HP 4145B and TLP: LabView programs

In this chapter it will be discussed the LabView implementation of equipment and the process used to make measurements shown in next chapter. In particular a VI has been realized for HP 4145B parameter analyzer, to make DC measurements of devices under test. A brief description of other LabView VI for TLP system is made at the end of chapter.

4.1 DC measurements : HP 4145B

4.1.1 Instrument specifications

The instrument used to make DC measurements on wafer is an HP 4145B Semiconductor Parameter Analyzer. It is able to measure DC current through voltage-biased devices and DC voltage across current-biased devices. Its source and measurement units are:

- four SMU channels, each of that can be programmed to function as a variable or constant DC voltage source/current monitor or as a variable or constant DC current source/voltage monitor

- two voltage source (Vs) channels, each of that can be programmed to function as a variable or constant DC voltage source

- two voltage monitor (Vm) channels, each of that can measure DC voltage up to ±20V

In our measurements we have used Source/Monitor Units (SMU) channels. Their source ranges and resolutions are shown in next tables, for voltage and current mode respectively.

Voltage Range	Resolution	Max Current
± 20V	1 mV	100 mA
± 40V	2 mV	50 mA
± 100V	5 mV	20 mA

<table>
<tr><th>Current Range</th><th>Resolution</th><th>Max Voltage</th></tr>
<tr><td>± 100 mA</td><td>100 μA</td><td>20 V (>50 mA)
40 V (>20 mA)</td></tr>
<tr><td>± 10 mA</td><td>10 μA</td><td rowspan="8">100 V (≤20 mA)</td></tr>
<tr><td>± 1 mA</td><td>1 μA</td></tr>
<tr><td>± 100 μA</td><td>100 nA</td></tr>
<tr><td>± 10 μA</td><td>10 nA</td></tr>
<tr><td>± 1 μA</td><td>1 nA</td></tr>
<tr><td>± 100 nA</td><td>100 pA</td></tr>
<tr><td>± 10 nA</td><td>10 pA</td></tr>
<tr><td>± 1 nA</td><td>1 pA</td></tr>
</table>

FIG. 4.1 SMU channel specifications for HP 4145B

The instrument supports remote control with an IEEE-488 interface, so it has been connected to a computer with a GPIB cable to make measurements. Needles was connected to the parameter analyzer with a coaxial cable. Measurement process was automated, using the instrument remote control from pc, thanks to the LabView program realized and described in the next paragraph.

4.1.2 VI for DC measures

The program described in this paragraph allows to obtain I-V curves for DC measurements of devices under test, setting values for defined variables in the front panel of VI (shown in *FIG. 4.3*). When all values are chosen and the VI is started, the program begins a sequence of automated operations. In a first moment are linked together the control strings that will be sent to HP 4145B, thanks to local variables afterwards called again by VI during the command execution.

In the front panel it is possible to define five sections:

1. *Channel definition*
2. *Display*
3. *Source set up*
4. *Plot and save*
5. *Display mode set up*

In *Channel definition* section it is possible to set name, source function (CONST, VAR1, VAR2) and source mode (voltage or current) for every channel of the instrument. In particular it is possible to disable or enable each value with a button.

The *Display* allows to view the I-V characteristic of device under test, shown in front panel of HP 4145B. It shows also the resource name of instrument, controlled by "VISA" communication protocol.

In *Source set up* section is possible to set the following parameters:

- source mode (voltage or current) for each source function (with the possibility of disable or enable it)
- type of sweep (linear or logarithmic)
- start, stop and step values for sweep
- number of points: number of measures in defined voltage or current range
- compliance limit: limit for output variable sets to avoid, a damage of device due to an excessive value

In *Plot and save* section it is possible to set:

- file path
- a comment in saved file
- measure type: it is possible to make a single measure and repeat, append or stop it
- integration time: opening time of A/D converter of the instrument. This parameter influences the rapidity of the measure and its noise. Practically a low value allows a lower impact on the device, but a more noisy characteristic. Three selectable values are short, medium and long. In first case no digital integration is performed, in second case measurement result is the average value of 16 sample taken during one line frequency period. Third case considers 256 sample taken during sixteen line frequency periods

In *Display mode set up* section is possible to set the visualization mode. Possible options are graphics (always used in this work), list and matrix. For graphics option is possible to name axes and set ranges of visualization. It is also possible to disable or enable the visualization of each axis.

LabView program realized to control HP 4145B consists in a series of frames. First frames defined local variables for channels, then are defined measurement and visualization conditions. In particular the program start with a frame that enables channels and sets their name and function (*FIG. 4.2*).

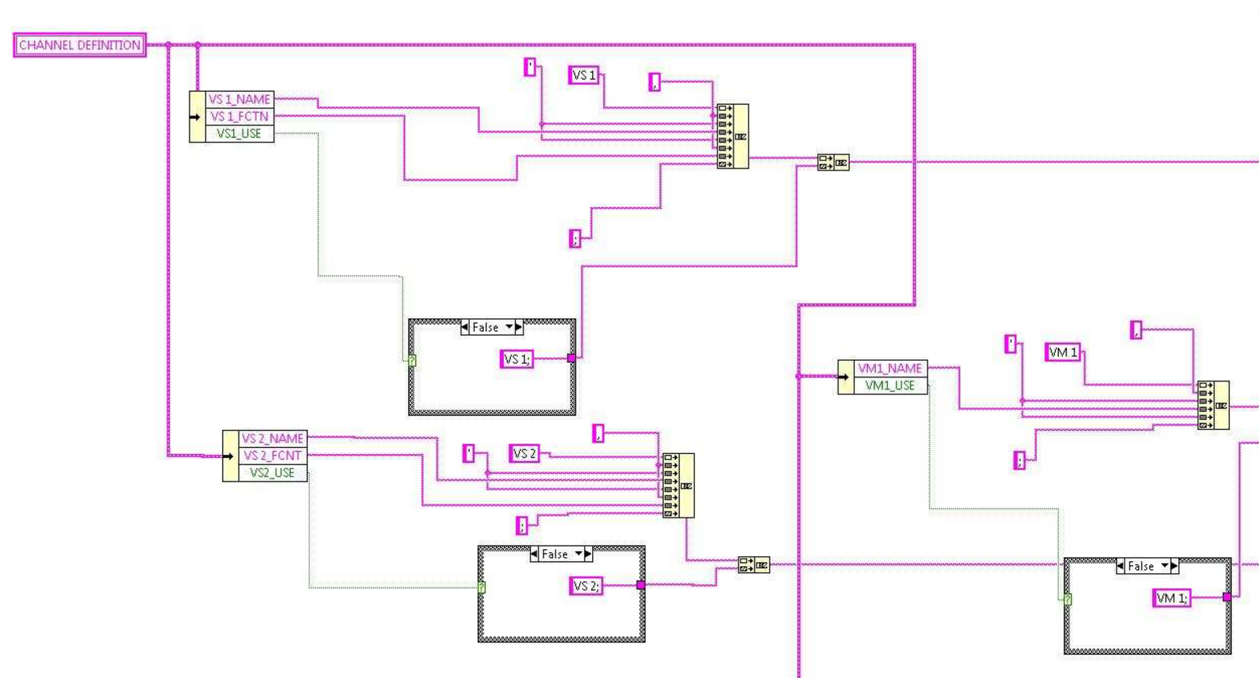


FIG. 4.2 Channels definition : name and function

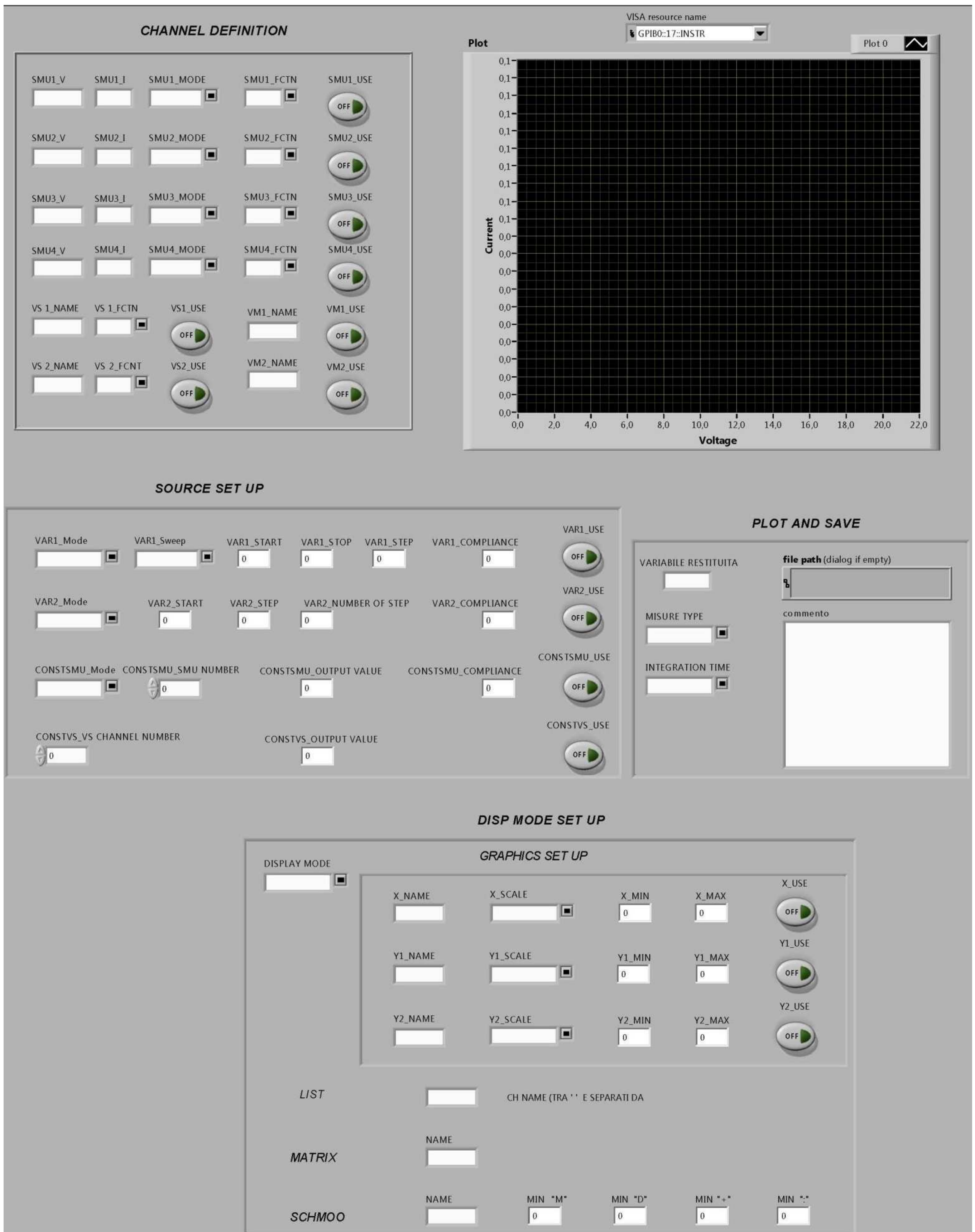


FIG. 4.3 Front panel of VI for DC measures with HP 4145B

Subsequently enable source functions are selected and for everyone are defined all parameter described in *Source set up* section of program interface (*FIG. 4.4*) (*FIG. 4.5*).

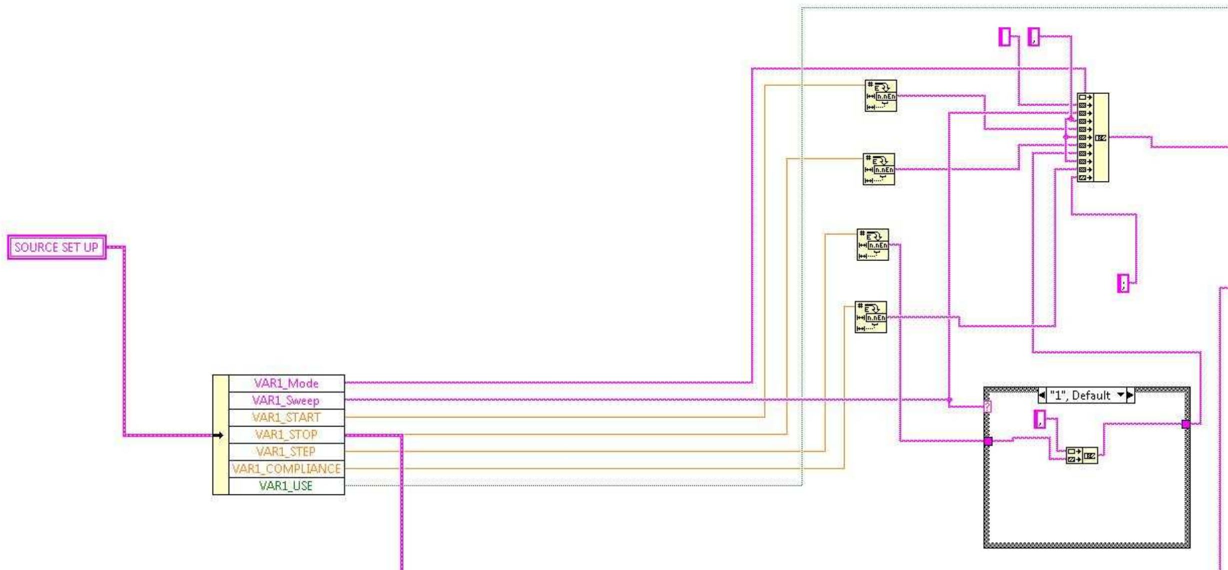


FIG. 4.4 Particular of Source set up frame: parameter definition for VAR1

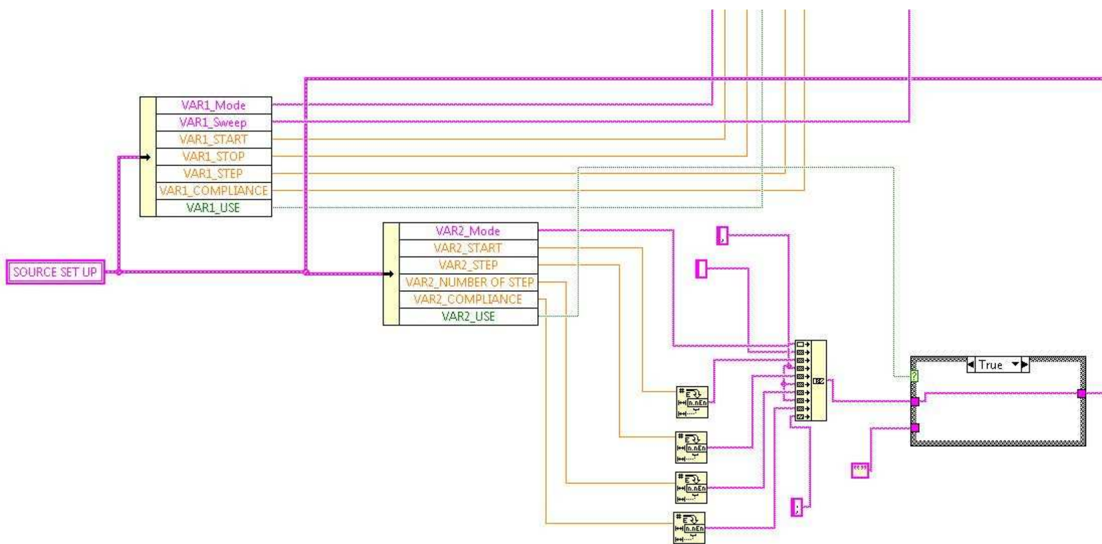


FIG. 4.5 Particular of Source set up frame: parameter definition VAR2

In third frame the name and range of visualization for axes (*FIG. 4.6*), measurement type (single, append, repeat) (*FIG. 4.7*) and integration time are defined.

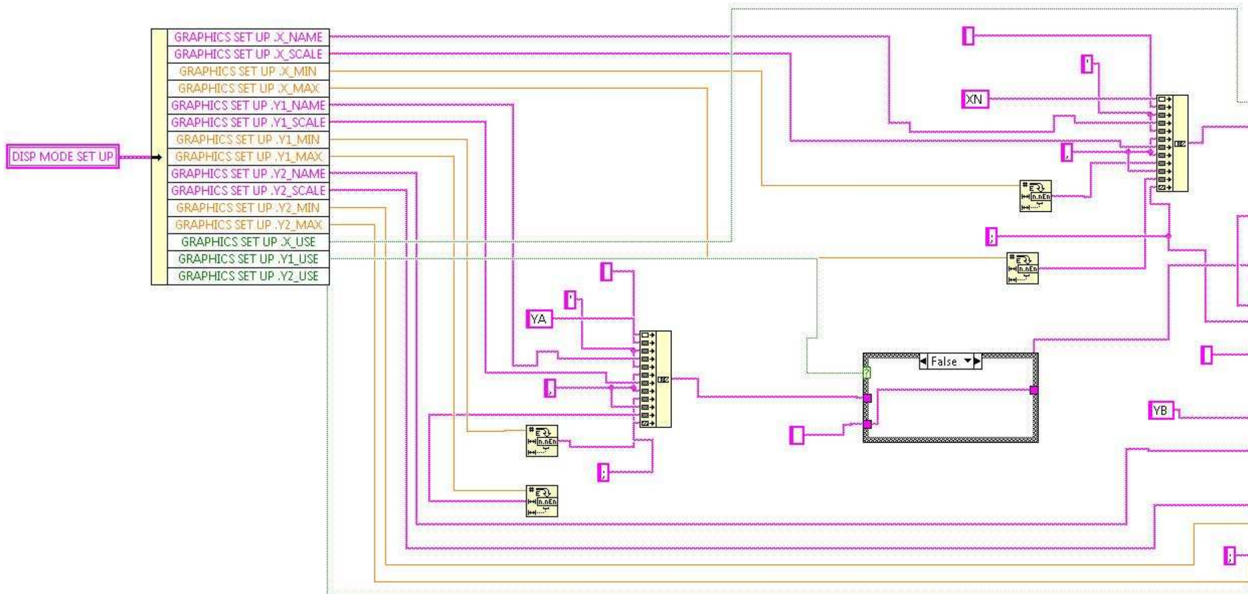


FIG. 4.6 Particular of Display set up frame: axes

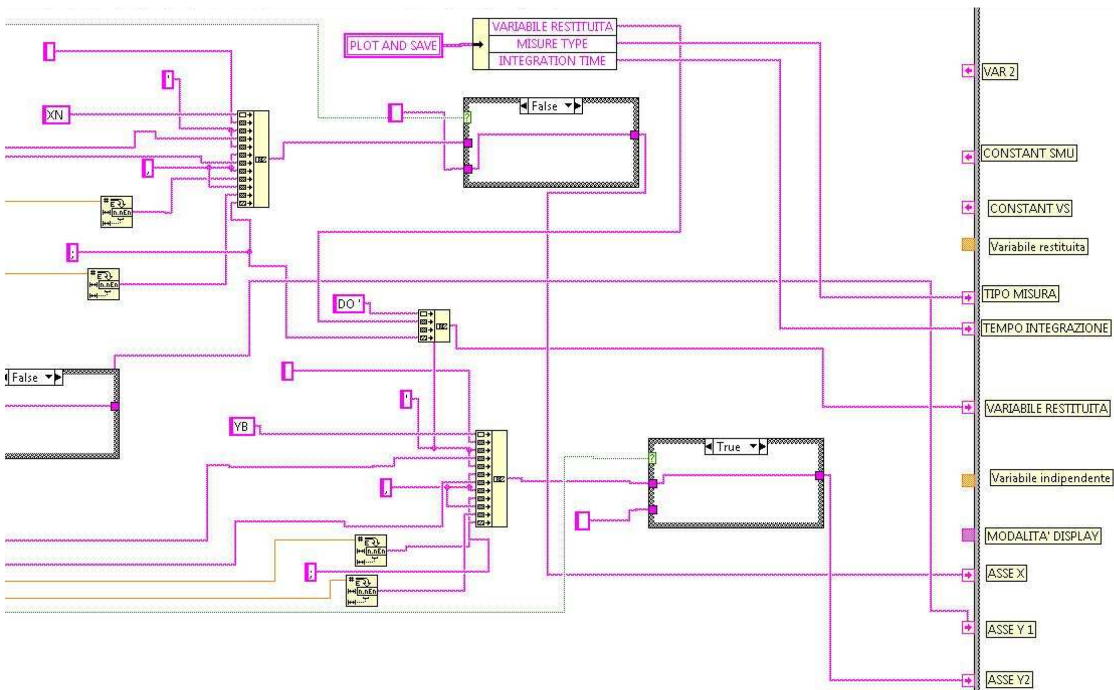


FIG. 4.7 Particular of Display set up frame: measure type

Next frame allows to select the display mode. It was realized for any possible case, even if in this thesis we have used only the graphic mode (*FIG. 4.8*) (*FIG. 4.9*).

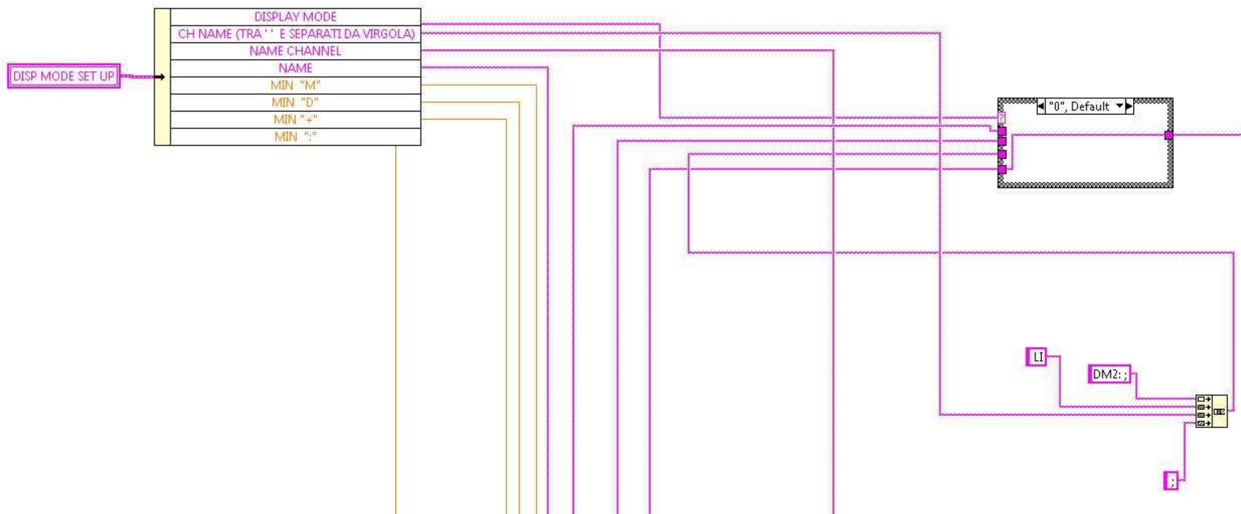


FIG. 4.8 Particular of Display mode set up frame: structure for selection of mode

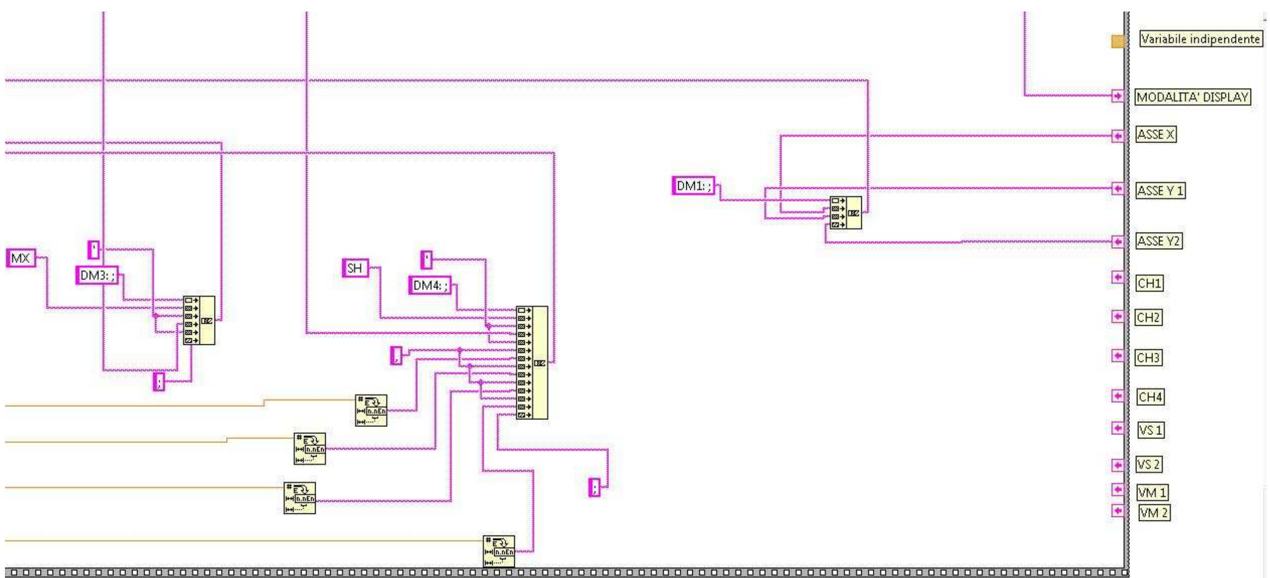


FIG. 4.9 Particular of Display mode set up frame: definition of MATRIX (DM3), GRAPHICS (DM1), SCHMOO (DM4) mode

In the fifth frame all defined parameters are passed to the parameter analyzer (*FIG. 4.10*). Subsequently the instrument is controlled (*FIG. 4.11*), measure is launched and result are read from the HP 4145B (*FIG. 4.12*).

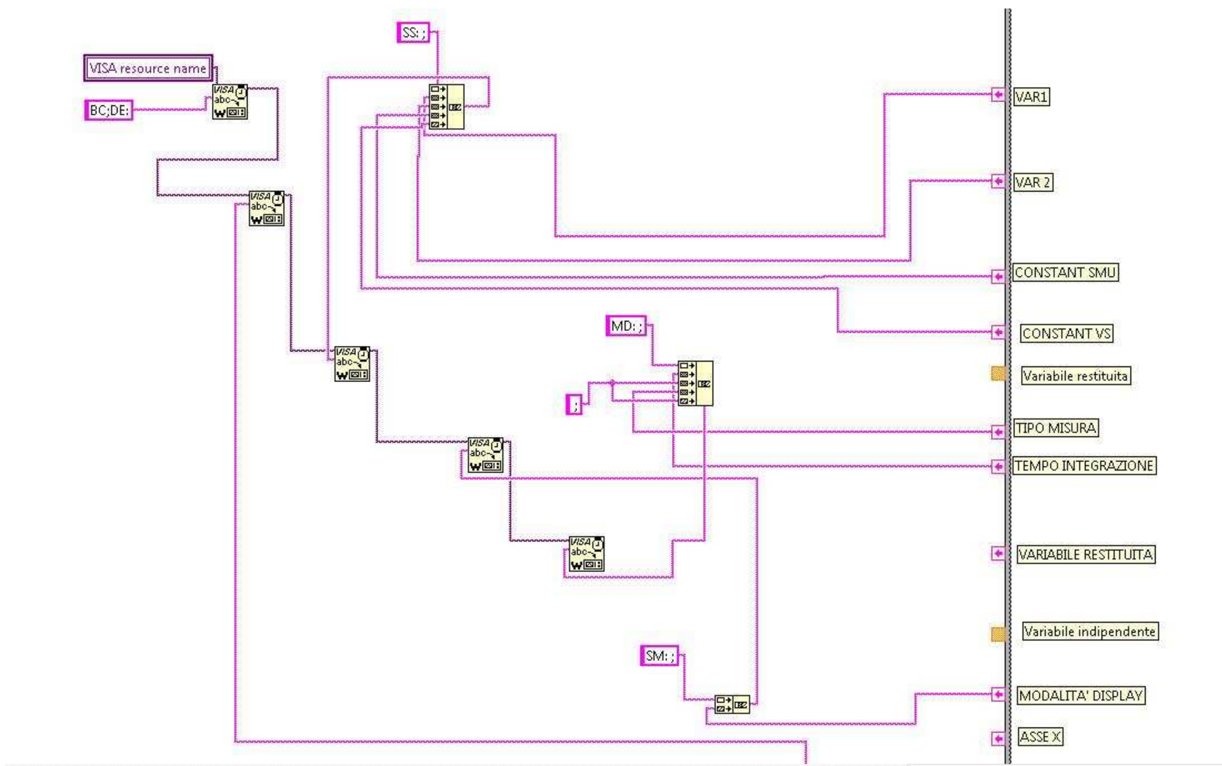
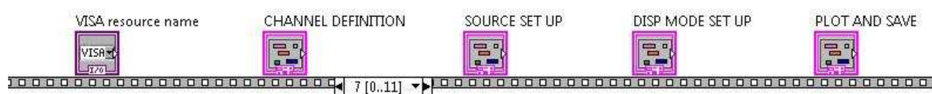


FIG. 4.10 Parameter defined in previous frames are passed to the parameter analyzer



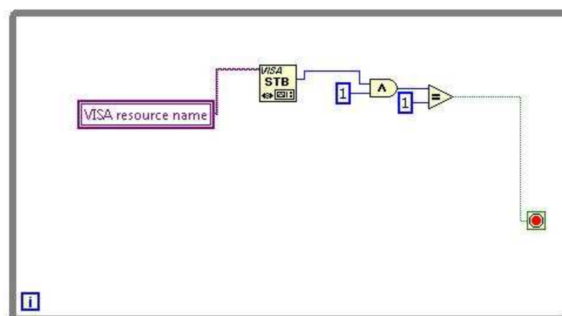


FIG. 4.11 Parameter analyzer control. On the top: global variable used in the program

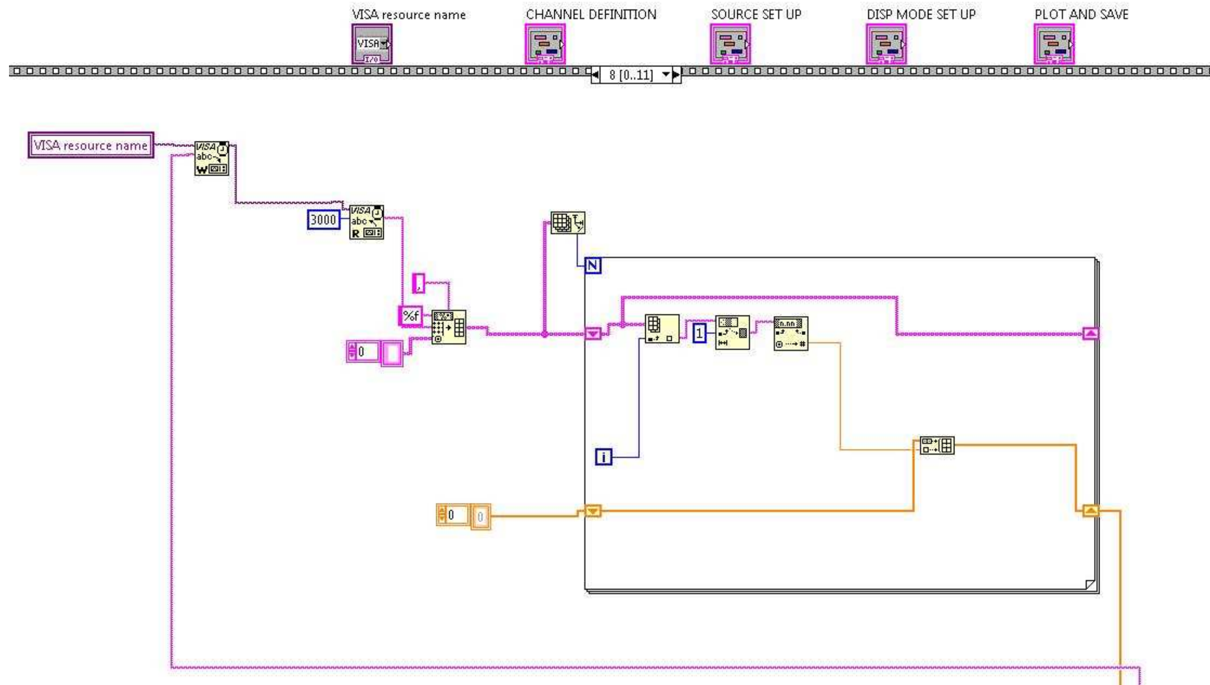


FIG. 4.12 Measure and data reading

In conclusion, before data saving (*FIG. 4.15*) and I-V characterization on interface display (*FIG. 4.16*), we have defined the y-axis scale for visualization (*FIG. 4.13*) (*FIG. 4.14*). According with selection in graphic display mode set up on interface, it can be linear or logarithmic (with 10, 25 or 50 points).

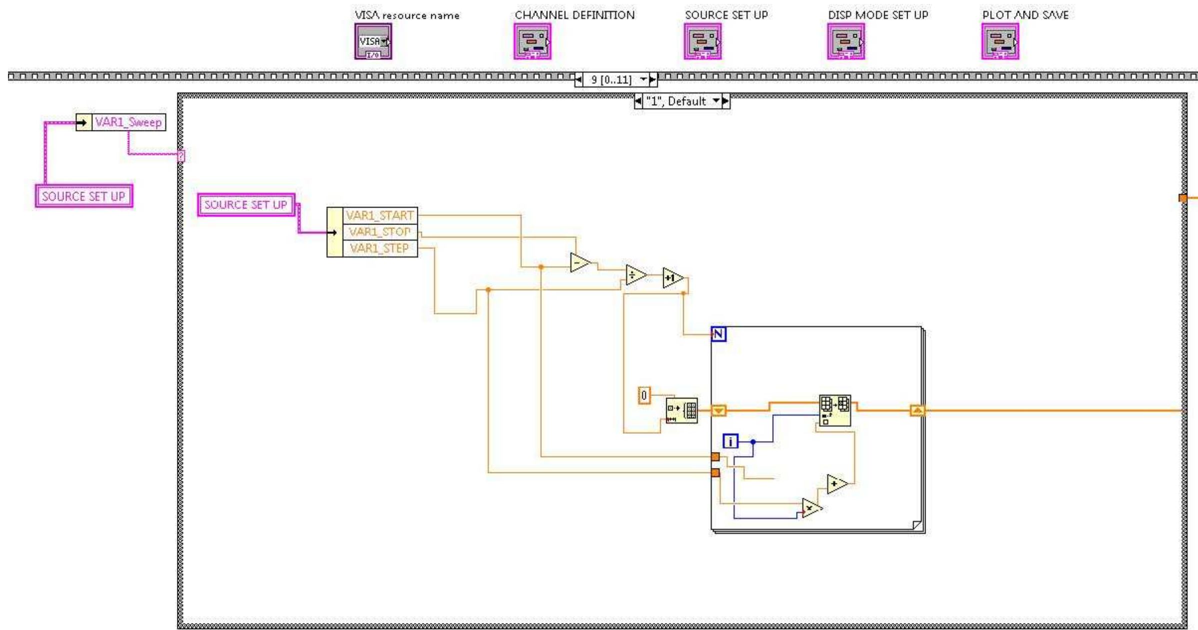


FIG. 4.13 Y-axis scale: linear case

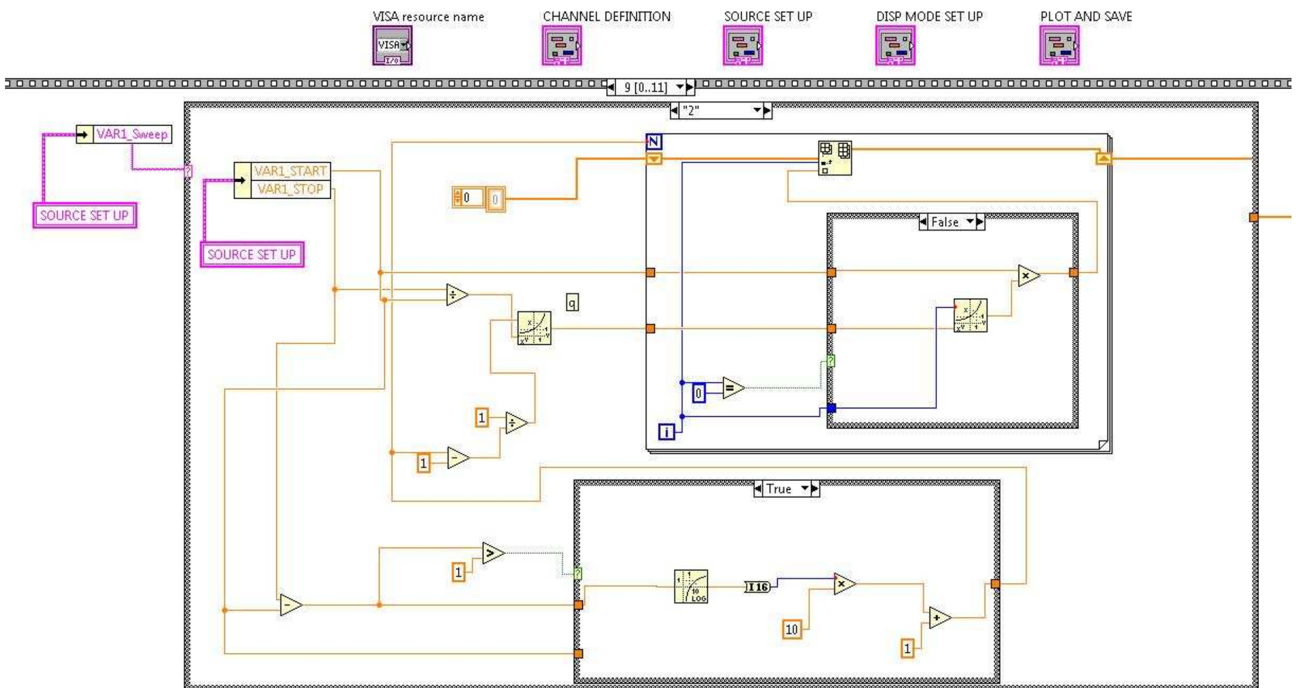


FIG. 4.14 Y-axis scale: logarithmic case (in this page for 10 points)

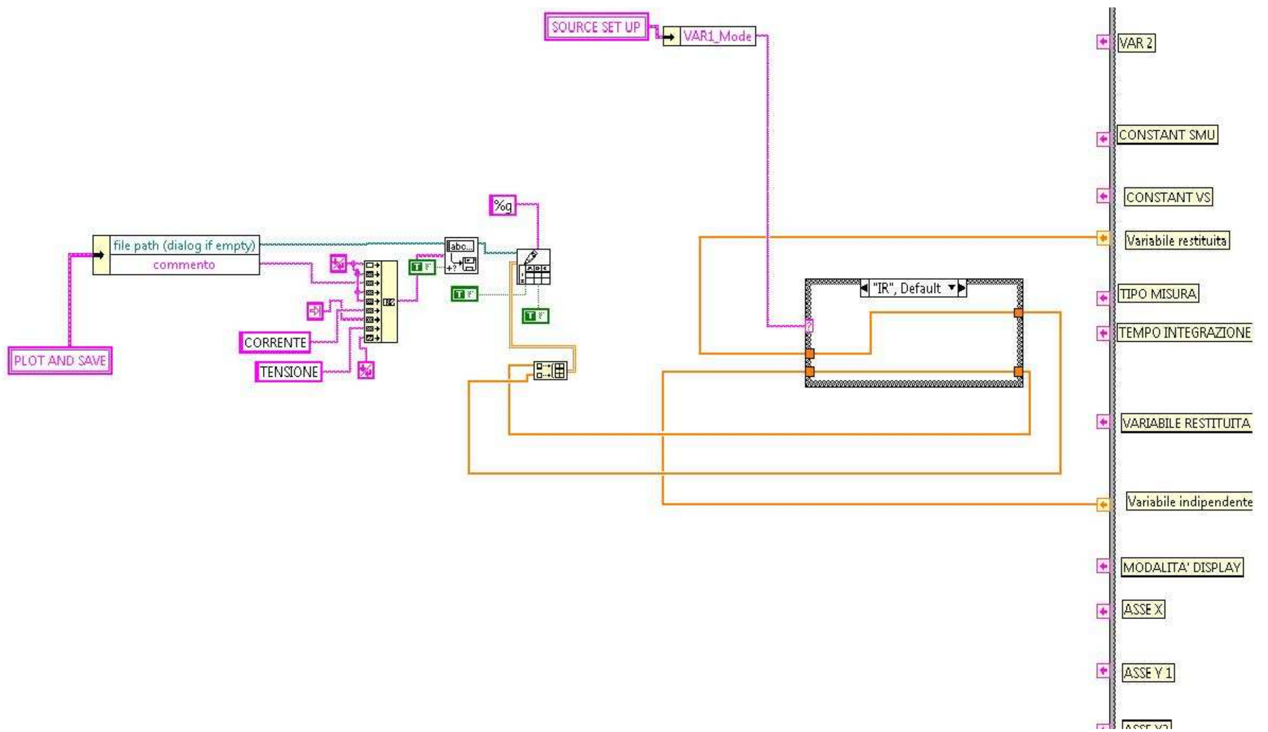


FIG. 4.15 Saving data

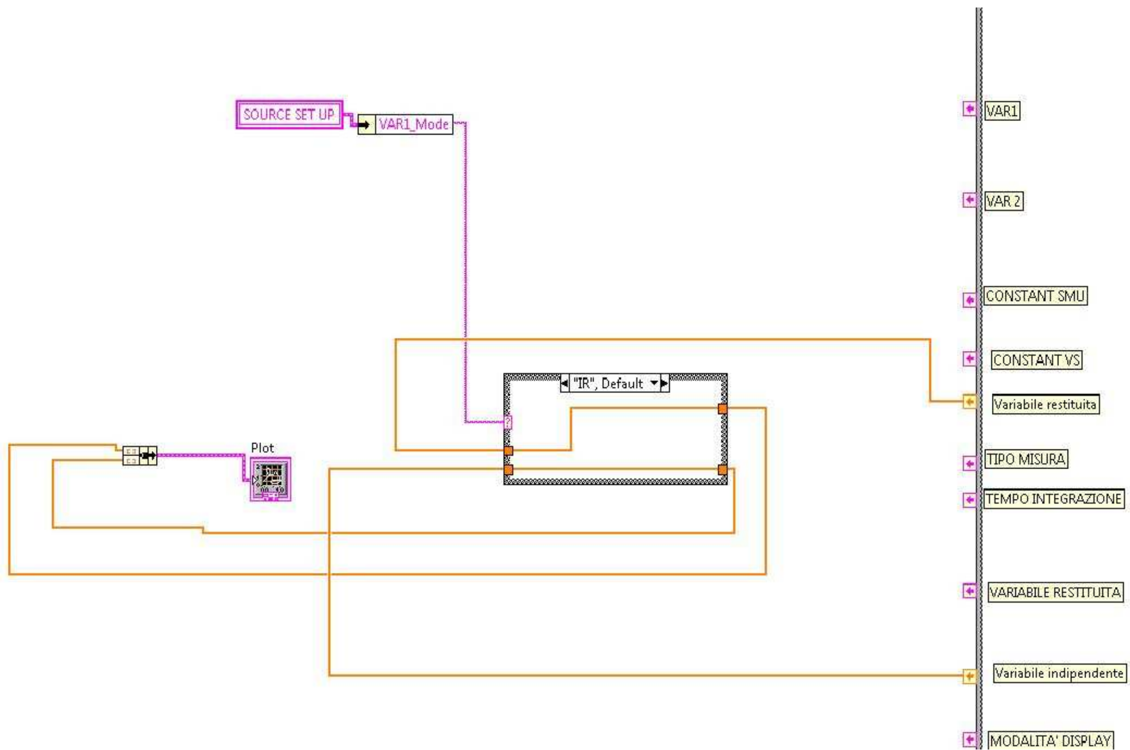


FIG. 4.16 I-V characteristic of data

4.2 TLP measurement : software LabView

In this paragraph is described the operation principle of LabView program used to make measurements shown in next chapter. It implies the interaction among typical elements of TLP on needles (described in previous chapter) and some instruments as an HV generator, an oscilloscope and a parameter analyzer. All instrument are used with a remote control, thanks to an IEEE-488.2 interface. A program synchronizes different operations necessary to make the measurement, avoiding overlaps. The front panel of implemented TLP system is shown in next figure.

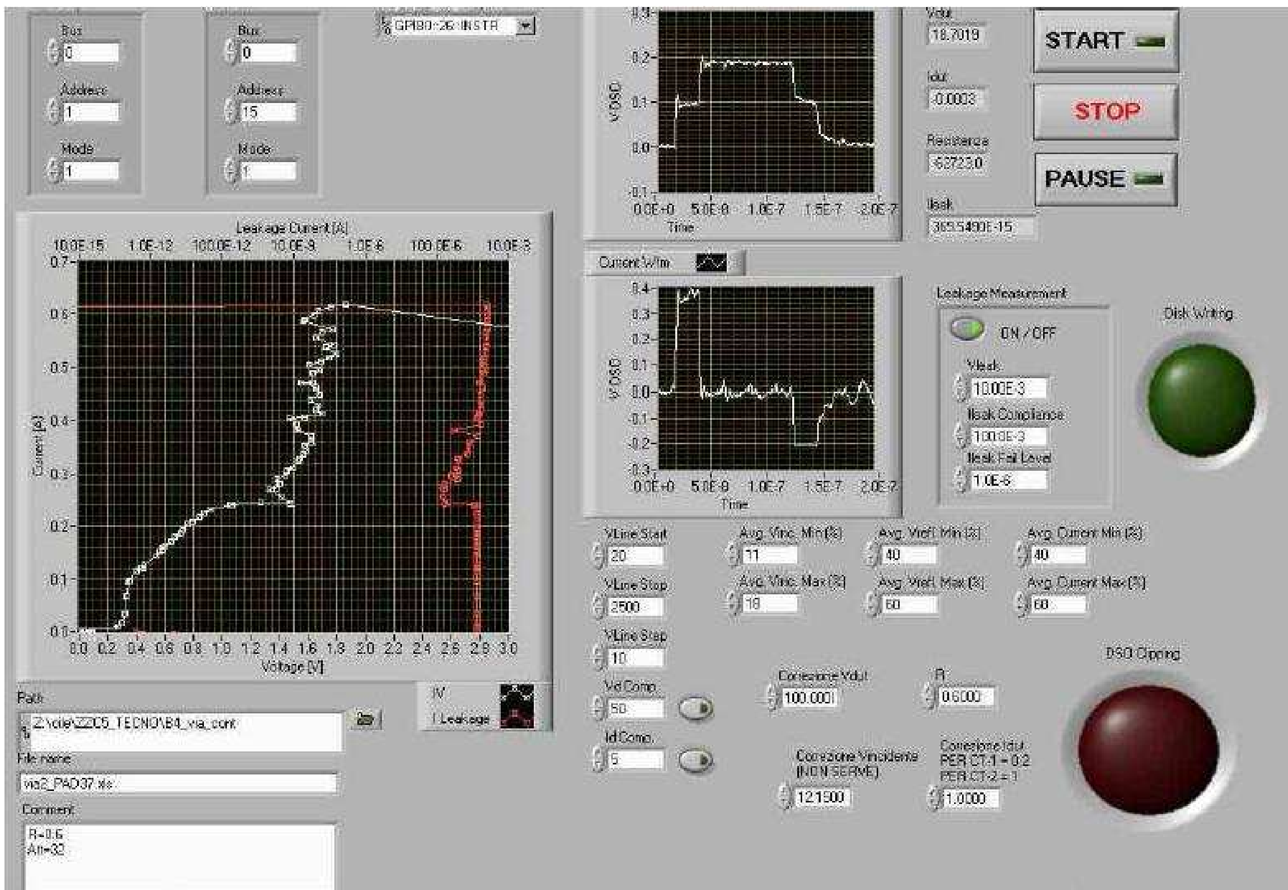


FIG. 4.13 : LabView interface of the Transmission Line Pulser implemented

In the panel is possible to see three graphic elements. They displays the I-V characteristic of DUT and the current and voltage pulses acquired by probes. On the right of current and voltage waveforms some indicators show their values, in addition to device impedance and leakage current at every measure cycle. Below leakage current indicators there are commands to set waveform range where we want to acquire current and voltage values on the device (as we have seen different range can induce different waveform values, so an incorrect evaluation of devices behavior). On the right of DUT I-V characteristic there are command to set voltage range for HV generator and the voltage increase at each measure cycle. Near these indicators there are controls to set voltage and current compliance for leakage measurement, compensation resistance and correction factors for probes. On I-V graph it is possible to set the GPIB bus and the address. Finally a section allows to set for saved measurements the file name and path, in addition to a comment.

LabView program working can be summarized in six fundamental passes:

1. *Start command waiting*: LabView program does not start until START button on interface is not pushed

2. *Initialization of HV generator (**Stanford Research System PS 350/5000V-25W**)*

3. *Initialization of DSO (**Tektronik 680 B, 2 channels, 1 GHz**)*: program sends data of selected channels to the oscilloscope, waiting for the start of measurement

4. *Initialization of **Keithley 2612***: are sent data for leakage current measurement to parameter analyzer

5. *Measurement cycle*:

    - Charge the transmission line with the HV generator. Voltage is increased at each cycle of the selected value in program interface

    - Prepare the oscilloscope to acquire voltage and current values

    - Enable and afterwards disable a relay to discharge the transmission line on DUT

    - Acquire voltage and current measurement from the oscilloscope

- Make leakage current measurement with *Keithley 2612*

- Disable all relays of system, displaying results on LabView program interface

- Wait for all instruments to be ready for a further cycle

6 *Data save*: I-V characteristic, leakage current and current and voltage pulses acquired by probes are saved in a file defined in program interface

Chapter 5

Measurements of metal lines and ESD protection structures for 65 nm PCM

In this chapter it will be shown DC and TLP measurements for metal lines and ESD protection structures made on a wafer given by ST Microelectronics. The work is related to the project "Characterization of ESD protection structures in NVM sub-micrometrical processes" between ST Microelectronics and the Microelectronic group of University of Padova, Department of Information Engineering. The activity regarded the characterization of metal lines, MOSSWI based protection structures and diodes from the P12_TC_ESD cell, shown in the next figure

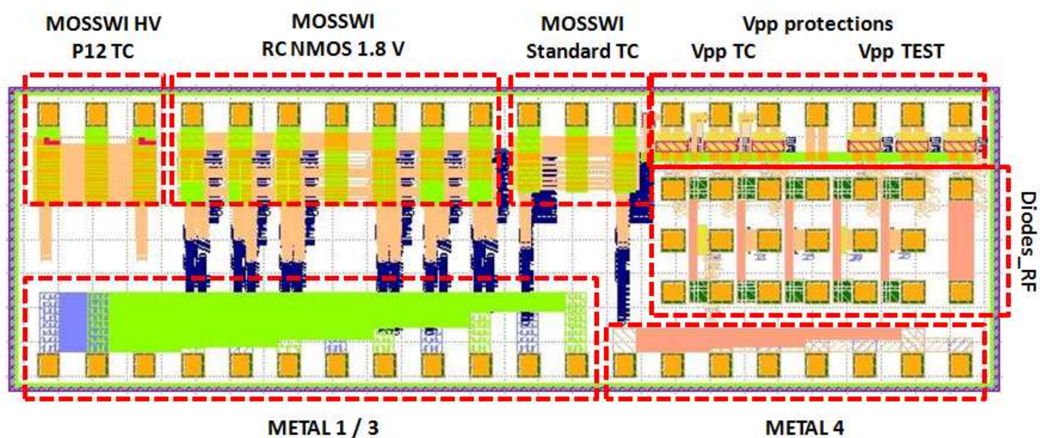


FIG. 5.1 Cell P12_TC_ESD : position of protection structures

Tested wafer ref. is A843768-16B0. All tested structures were characterized in DC and 100 ns TLP pulsed regime, and diodes were measured also in 200 us pulsed regime using the pulsing capabilities of a Keithley 2612 Source Meter.

5.1 Metal lines

The characterization activity of devices from P12_TC_ESD cell started measuring the electrical parameters of METAL structures in DC (Hp 4145B Semiconductor Parameter Analyzer) and 100 ns pulsed regime (100 ns - TLP). The layout of tested structures, with the numeration adopted to identify tested devices is reported in the next figure.

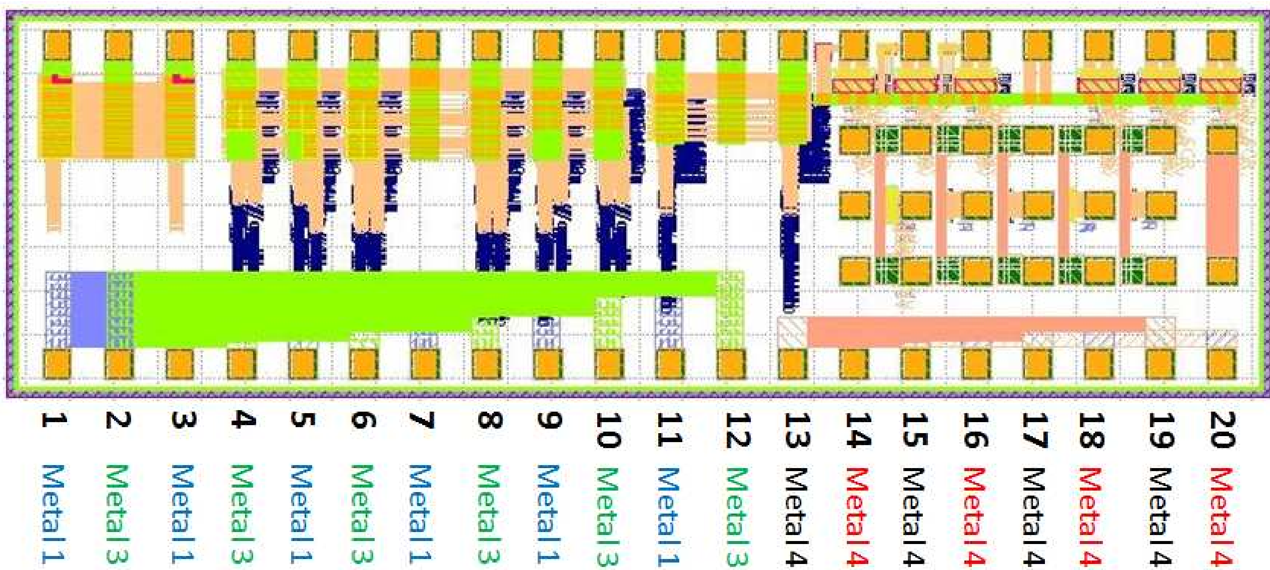


FIG. 5.2 Numeration adopted to identify pins for measures of metal lines

Dimensions of tested structures are summarized in the next table. Other dimensions (extracted from .GDS) are:

- pad size: 67*72 µm
- pad-to-pad distance: 73 µm

The right structure (METAL 4) is interdigitated with METAL 2, 40 µm width, connected to METAL 1 with a large number of VIAs.

METAL 1			METAL 3		
Pads	Length [um]	W [um]	Pads	Length [um]	W [um]
1 → 3	212.94	8	2 → 4	212.94	8
1 → 5	493	16	2 → 6	493	16
1 → 7	773.3	24	2 → 8	773.3	24
1 → 9	1053.46	32	2 → 10	1053.46	32
1 → 11	1333.08	40	2 → 12	1333.08	40
METAL 4			**METAL 4**		
Pads	Length [um]	W [um]	Pads	Length [um]	W [um]
13 → 15	212.94	8	14 → 16	212.94	8
13 → 17	493	16	14 → 18	493	16
13 → 19	773.3	24	14 → 20	773.3	24

The comparison of the measurements carried out in DC regime (current compliance set @ 20 mA) on different structures is reported in the next graphs. Measurement were repeated in several sectors of the wafer, obtaining similar data. All structures have shown, as expected, a resistance value increasing with the increase of the metal line length. This result is possible normalizing the value of current with the area because the presence of a different number of VIAs and metal width makes difficult a direct comparison of test structures.

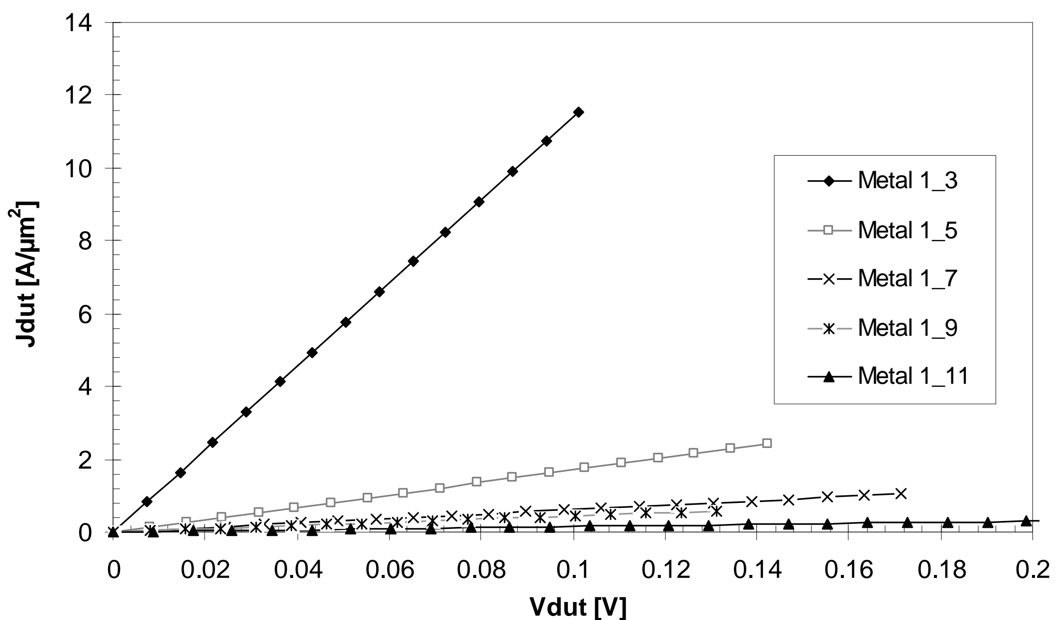


FIG. 5.3 Comparison of DC measures with HP 4145B for metal line #1

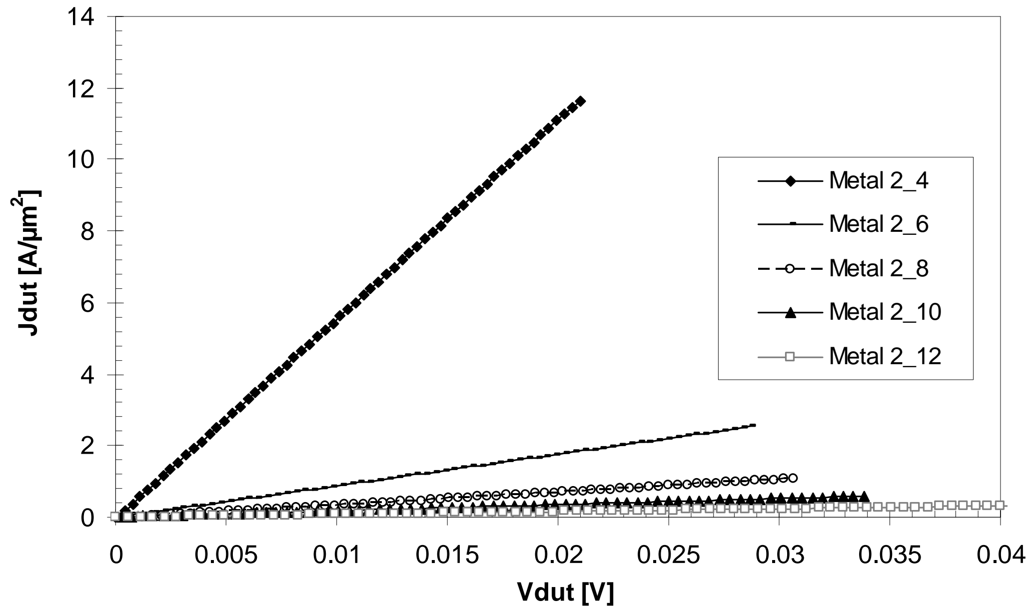


FIG. 5.4 Comparison of DC measures with HP 4145B for metal line #3

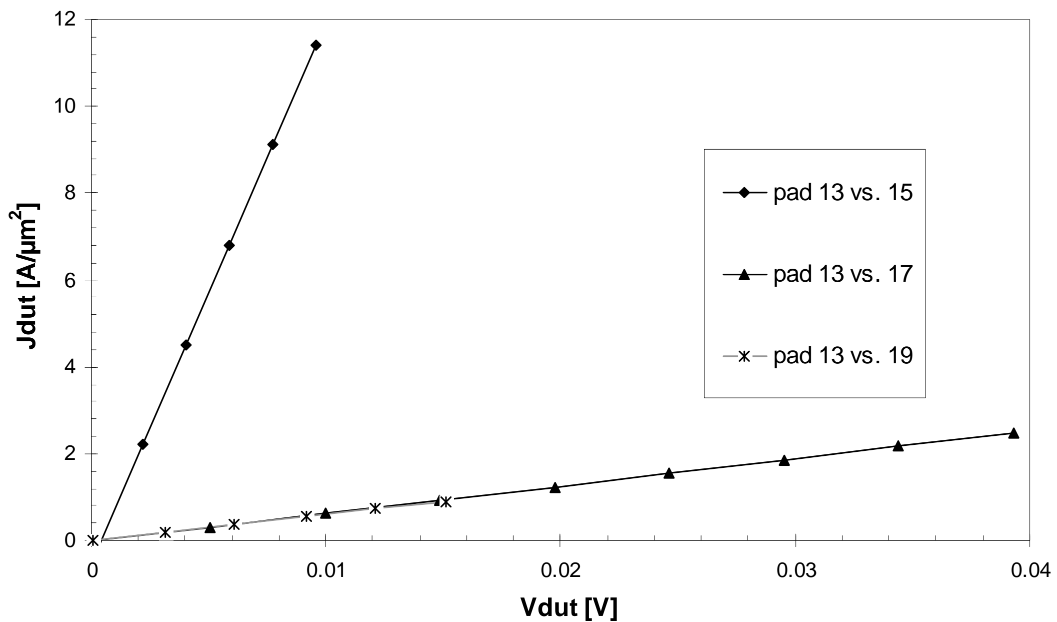


FIG. 5.5 Comparison of DC measures with HP 4145B for metal line #4

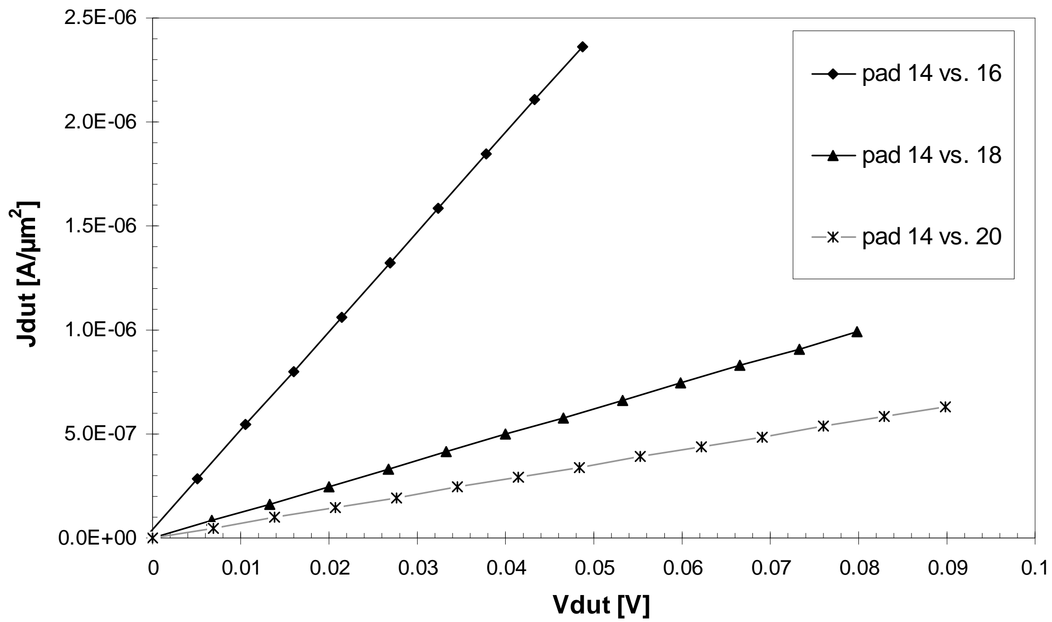


FIG. 5.6 Comparison of DC measures with HP 4145B for metal line #4

We have then proceeded with the characterization of the behavior shown by metal lines under 100 ns TLP regime. Because of the four type of metal lines share a common pad, each measurement was carried out on a fresh die, to avoid influences from previous measurements. The comparison of measured I-V curves are shown in the next graphs.

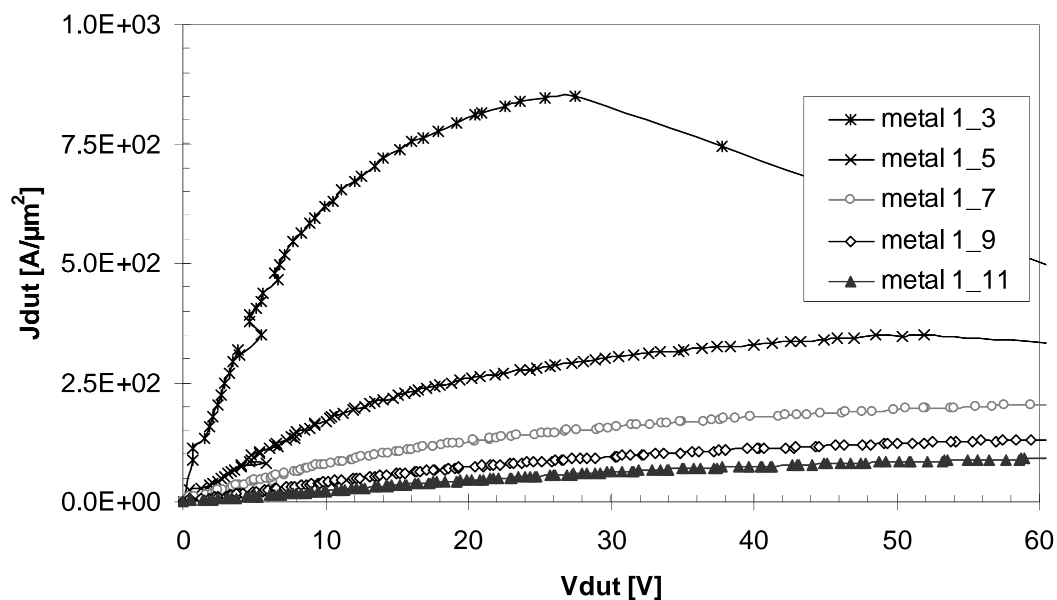


FIG. 5.7 Comparison of TDR-TLP measures for metal line #1

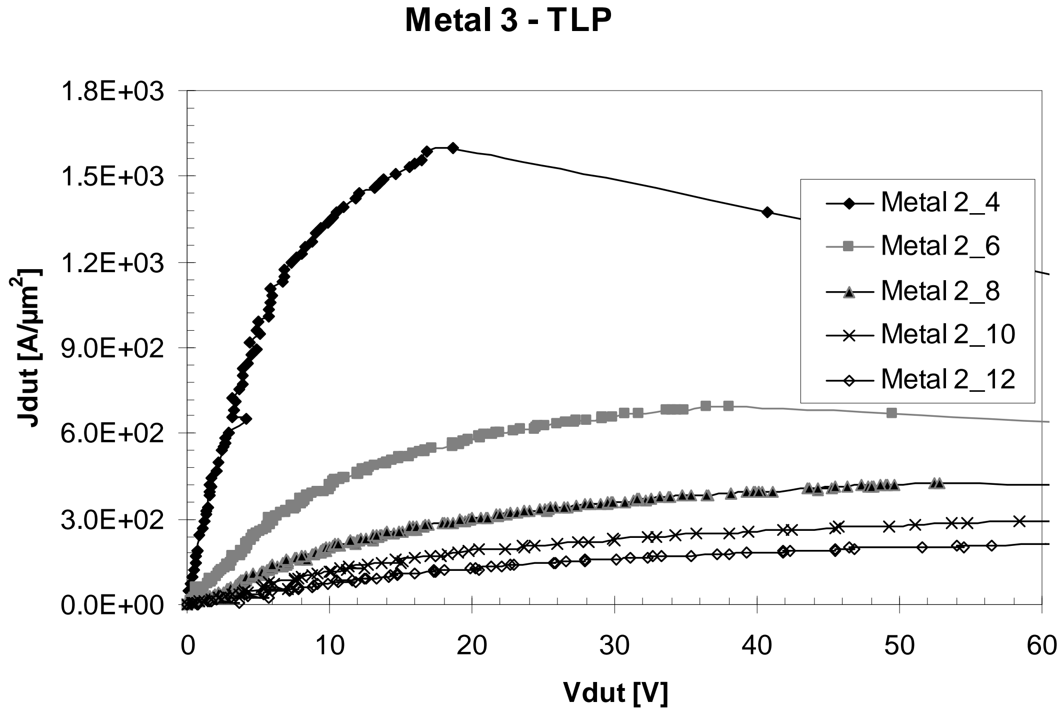


FIG. 5.8 Comparison of TDR-TLP measures for metal line #3

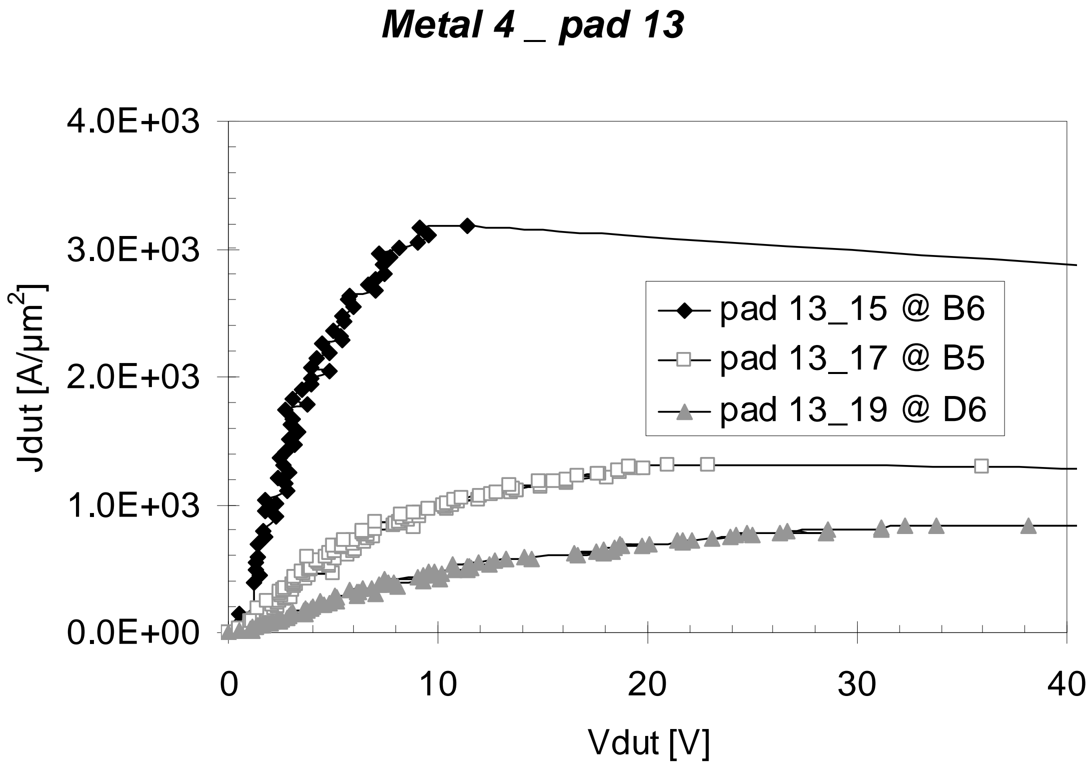


FIG. 5.9 Comparison of TDR-TLP measures for metal line #4

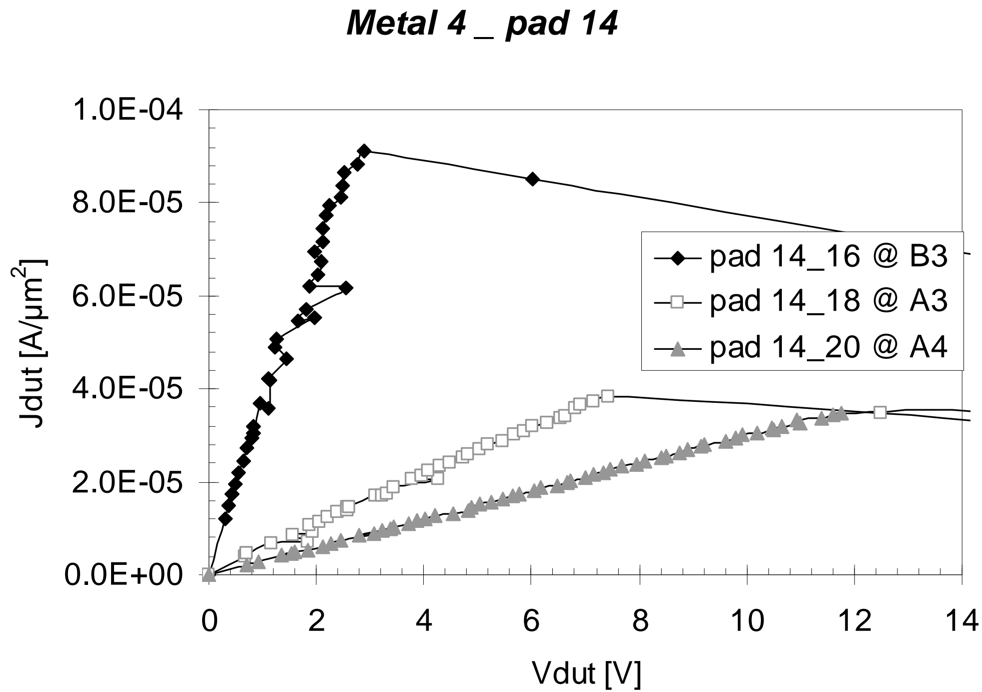


FIG. 5.10 Comparison of TDR-TLP measures for metal line #4

The following table summarizes the extracted values (metal line resistance in DC and TLP regimes, failure current, failure voltage). Resistance values were extracted by means of a linear regression of the linear region of the I-V curves, shown later.

DUT	Pads	Area (µm²)	R□_DC (Ω *µm²)	R□_TLP (Ω *µm²)	I_{fail} (A)	V_{fail} (V)
Metal 1	1-3	1.7 E-03	8.76 E-03	1.33 E-02	1.4	27.4
Metal 1	1-5	7.89 E-03	5.83 E-02	5.81 E-02	2.7	51.9
Metal 1	1-7	1.86 E-02	1.63 E-01	1.31 E-01	3.9	72.3
Metal 1	1-9	3.37 E-02	2.27 E-01	2.46 E-01	4.7	76.8
Metal 1	1-11	5.33 E-02	6.67 E-01	4.5 E-01	5.6	85.8
Metal 3	2-4	1.7 E-03	1.79 E-03	5.20 E-03	2.7	18.6
Metal 3	2-6	7.89 E-03	1.13 E-02	2.03 E-02	5.4	38.1
Metal 3	2-8	1.86 E-02	2.97 E-02	4.78 E-02	7.9	52.4
Metal 3	2-10	3.37 E-02	5.79 E-02	9.77 E-02	9.8	63.8
Metal 3	2-12	5.33 E-02	1.27 E-01	1.46 E-01	11.8	79.0
Metal 4	13-15	1.7 E-03	1.47 E-03	2.14 E-03	5.42	11.42
Metal 4	13-17	7.89 E-03	1.57 E-02	8.24 E-03	10.37	22.86
Metal 4	13-19	1.86 E-02	2.38 E-02	1.96 E-02	15.53	38.14
Metal 4	14-16	8.37 E+03	2.10 E+04	3.01 E+04	0.76	2.89
Metal 4	14-18	1.94 E+04	8.02 E+04	1.89 E+05	0.74	7.41
Metal 4	14-20	3.04 E+04	1.41 E+05	3.38 E+05	1.06	11.77

In the following pages we report the I-V graphs of metal lines measured in TLP regime, together with the indication of the linear regression used to extract the resistance value. Titles on the graphs indicates the pads of tested devices (subdivision of the wafer shown on next figure).

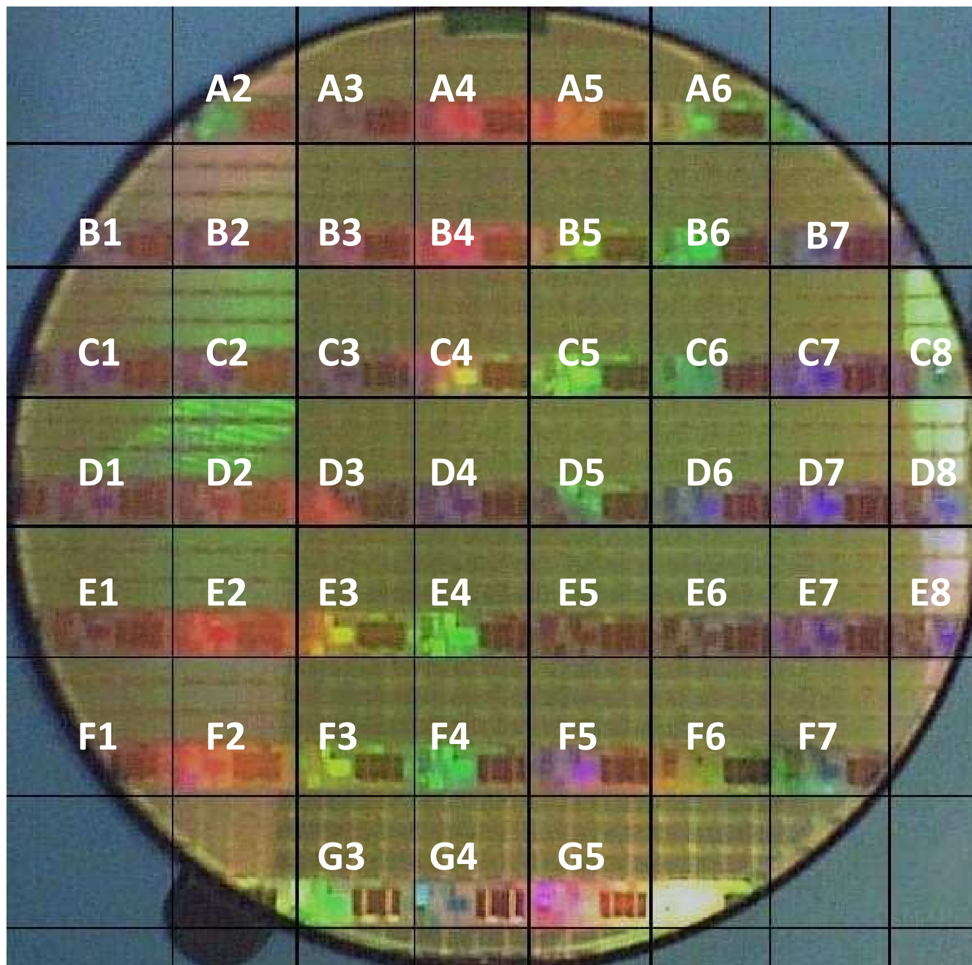


FIG. 5.11 Subdivision of tested wafer: every measure that will be shown indicates in graph's title the tested devices on wafer

METAL 1

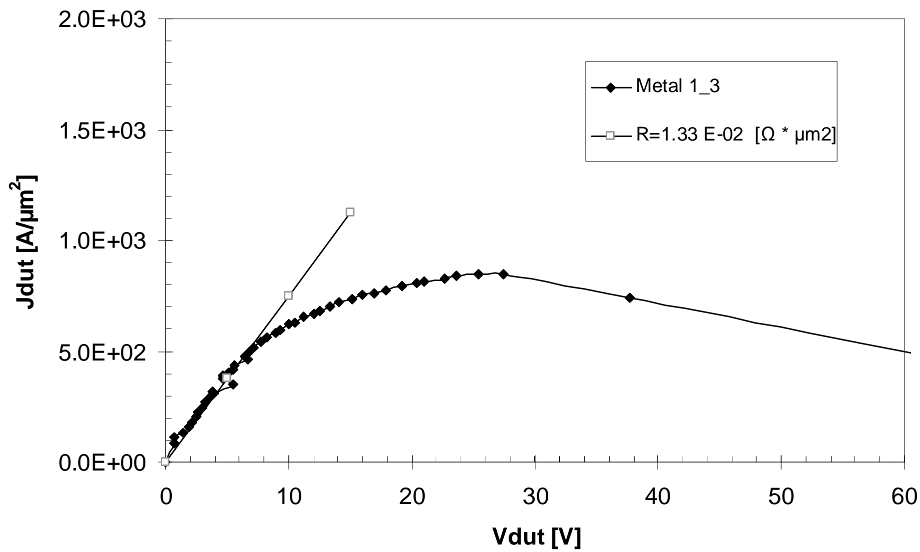


FIG. 5.12 TDR-TLP measure for pads 1 vs. 3

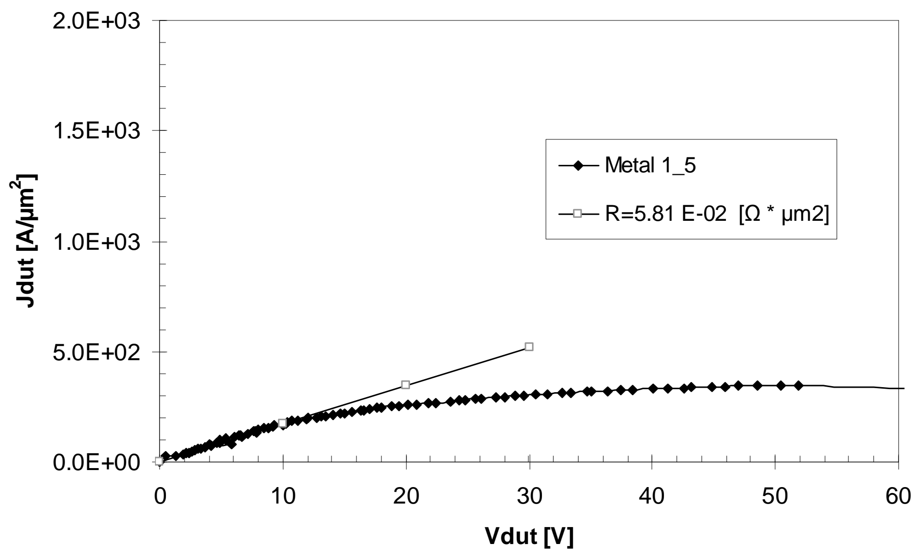


FIG. 5.13 TDR-TLP measure for pads 1 vs. 5

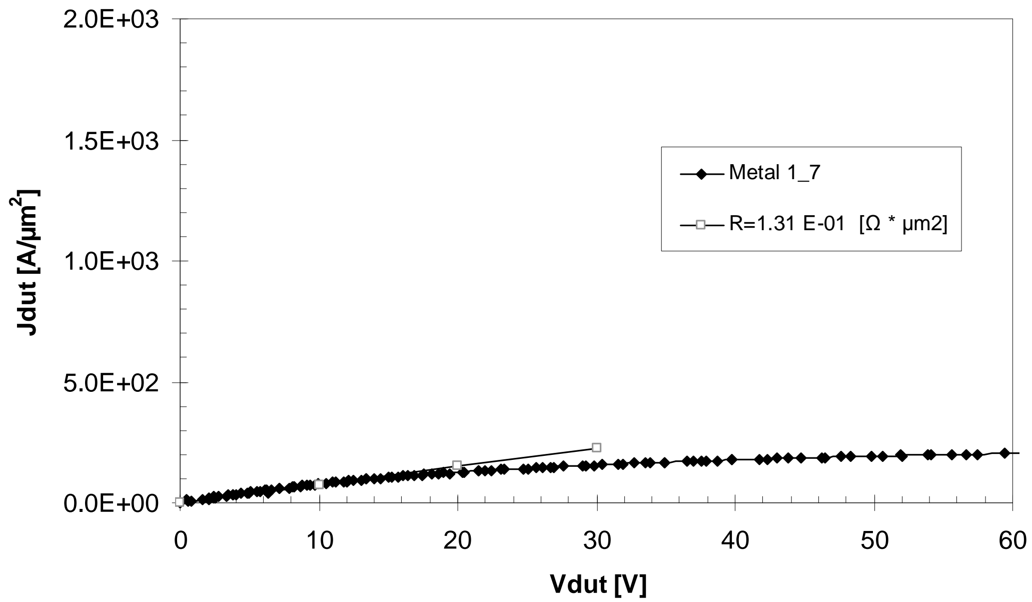


FIG. 5.14 TDR-TLP measure for pads 1 vs. 7

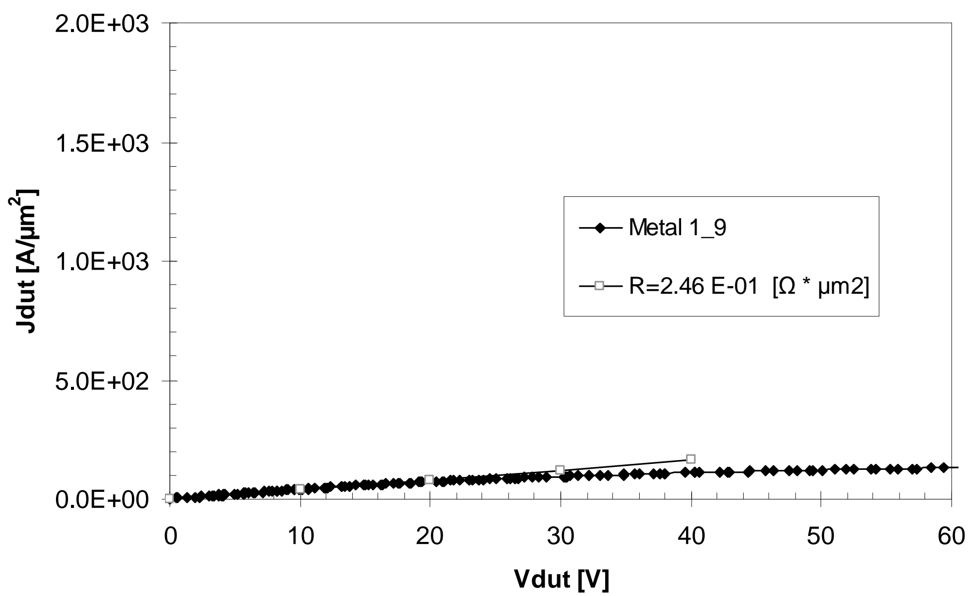


FIG. 5.15 TDR-TLP measure for pads 1 vs. 9

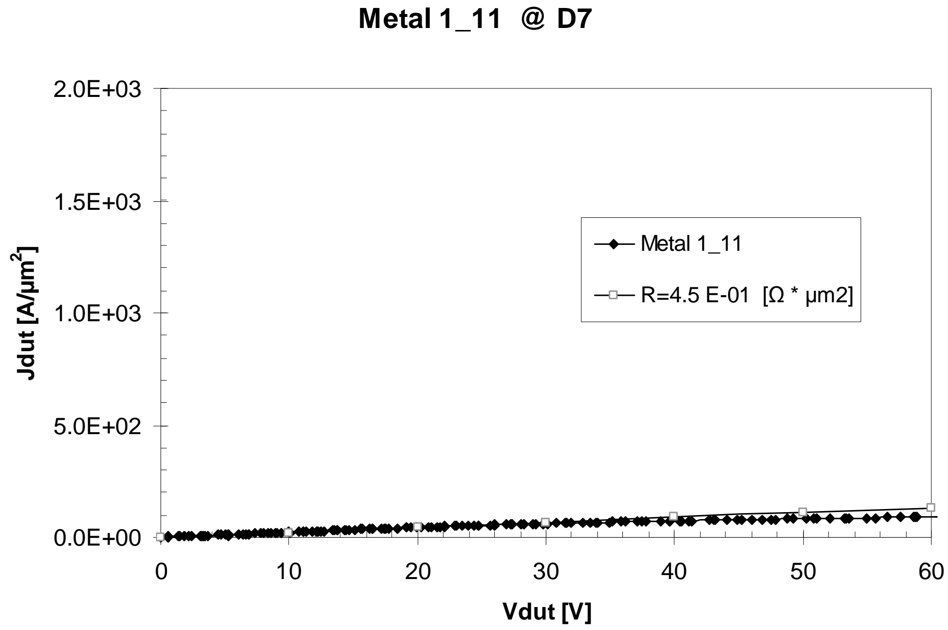


FIG. 5.16 TDR-TLP measure for pads 1 vs. 11

METAL 3

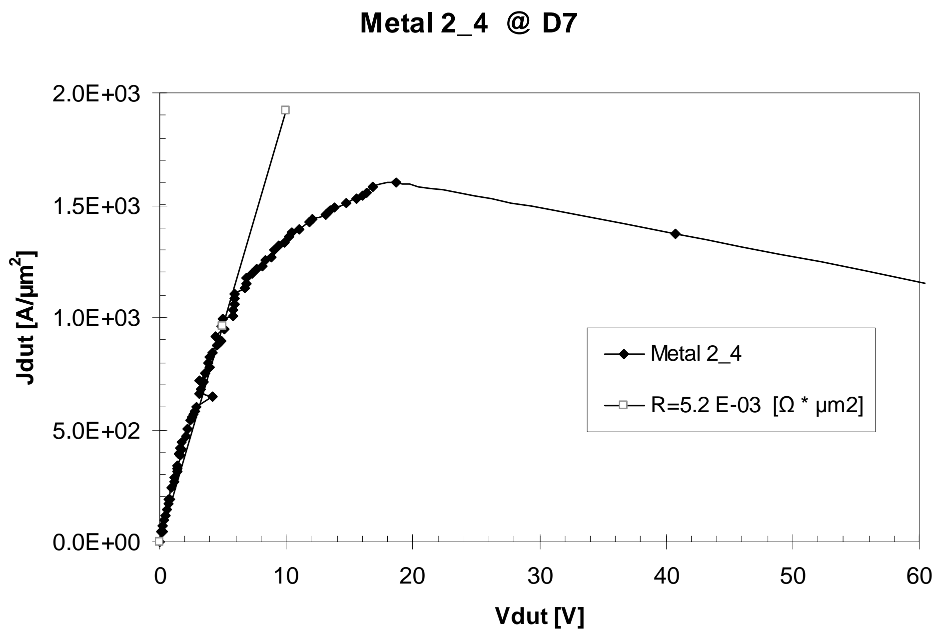


FIG. 5.17 TDR-TLP measure for pads 2 vs. 4

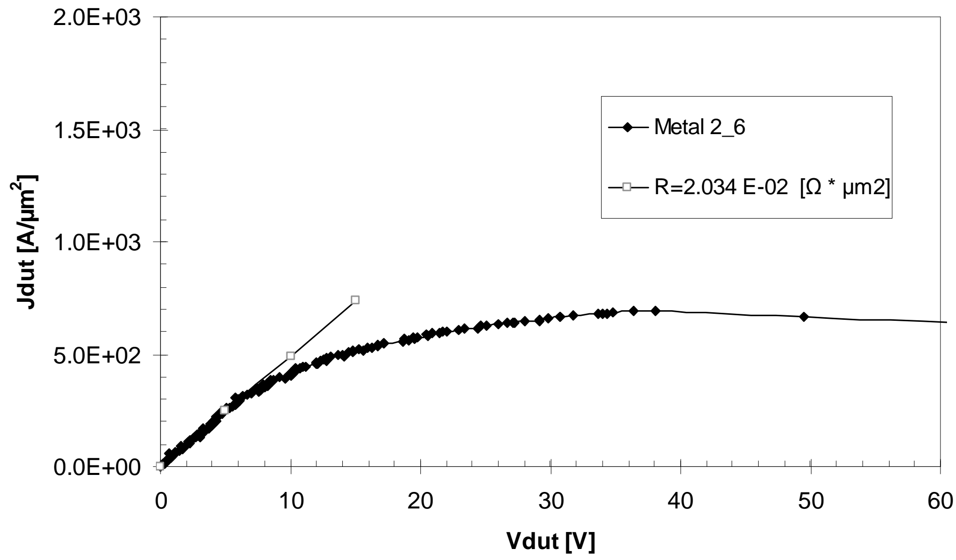


FIG. 5.18 TDR-TLP measure for pads 2 vs. 6

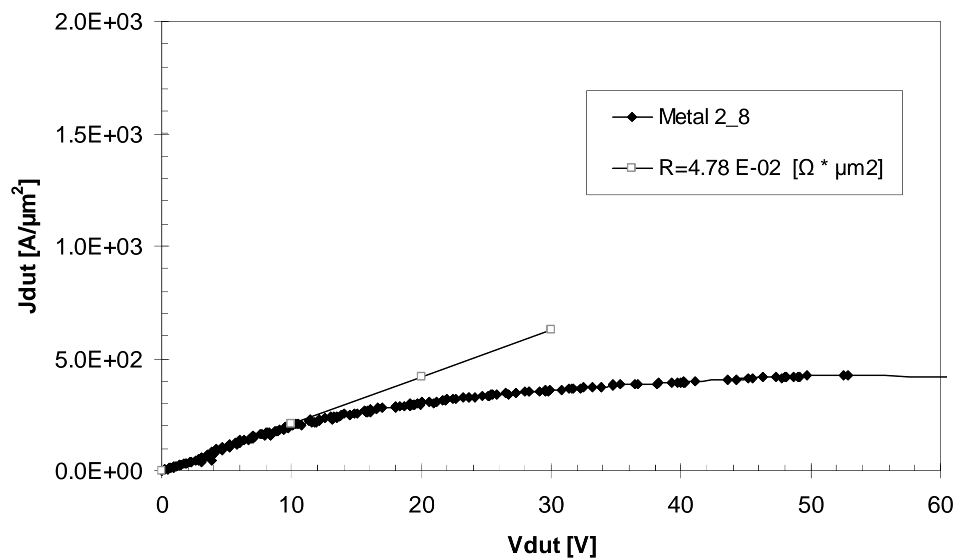


FIG. 5.19 TDR-TLP measure for pads 2 vs. 8

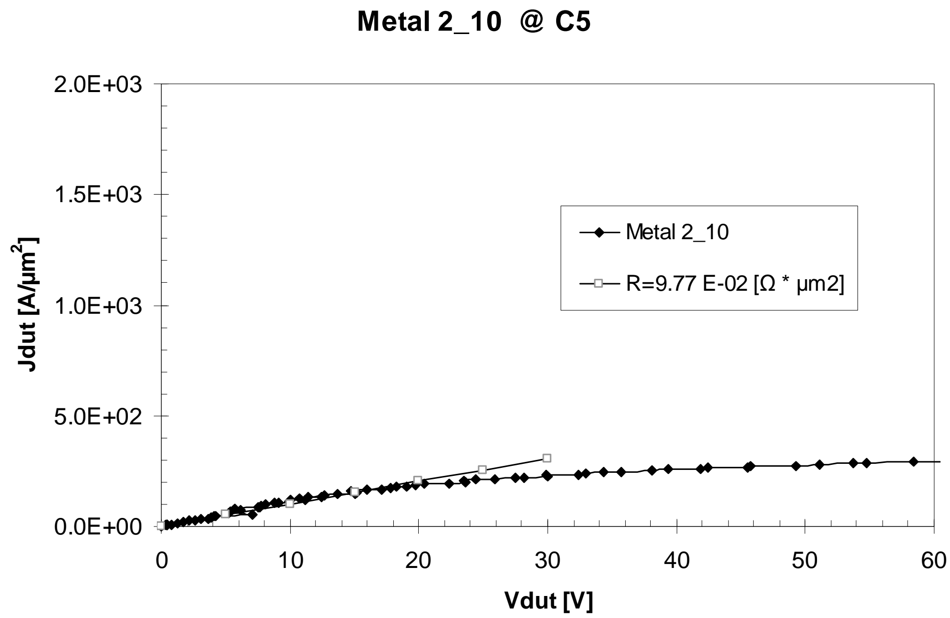


FIG. 5.20 TDR-TLP measure for pads 2 vs. 10

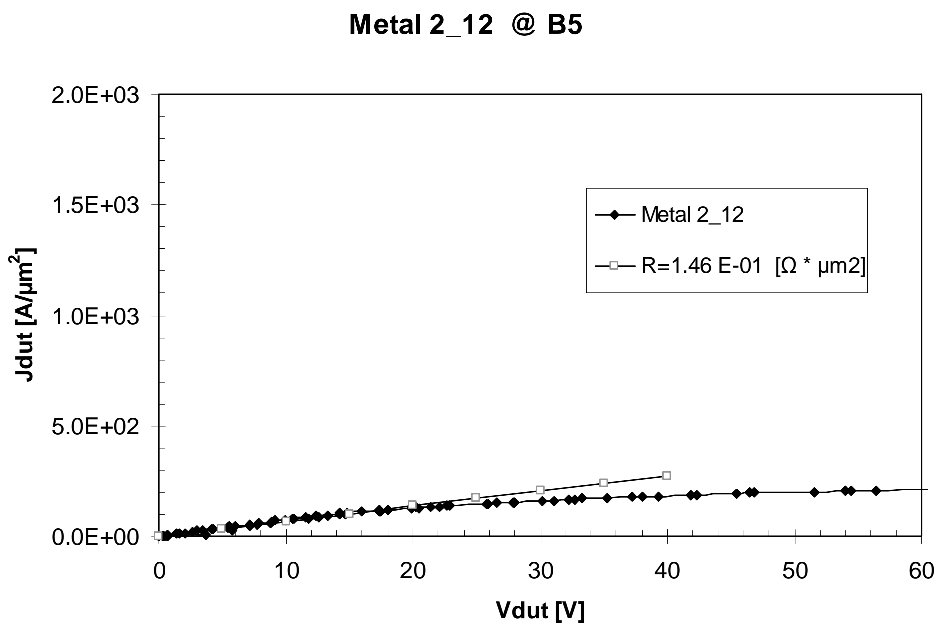


FIG. 5.21 TDR-TLP measure for pads 2 vs. 12

METAL 4

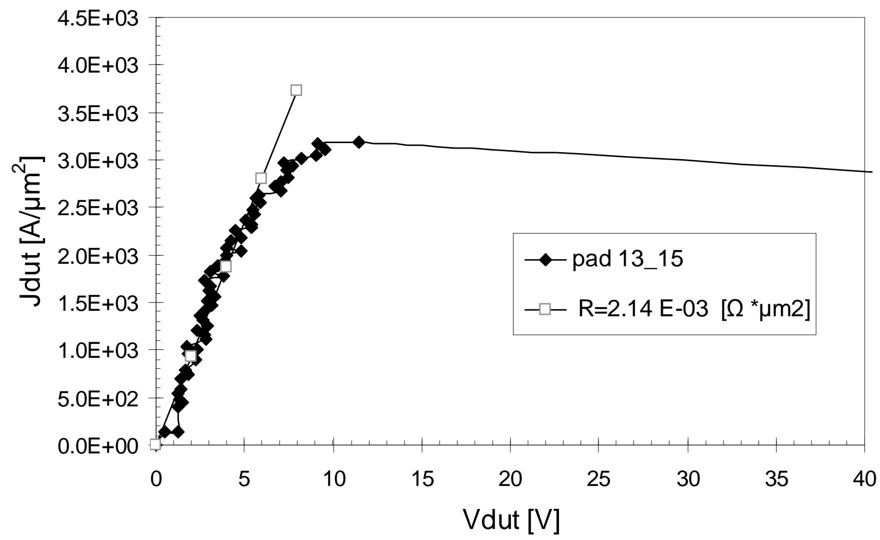


FIG. 5.22 TDR-TLP measure for pads 13 vs. 15

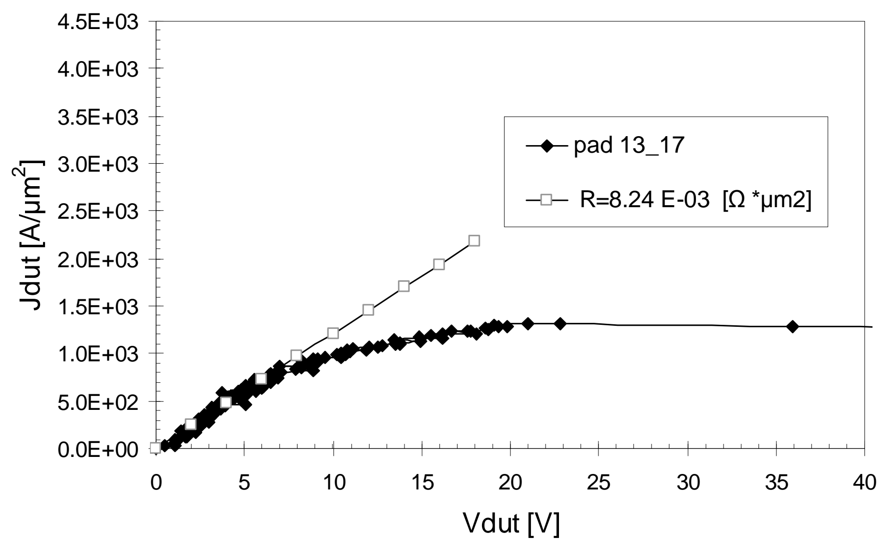


FIG. 5.23 TDR-TLP measure for pads 13 vs. 17

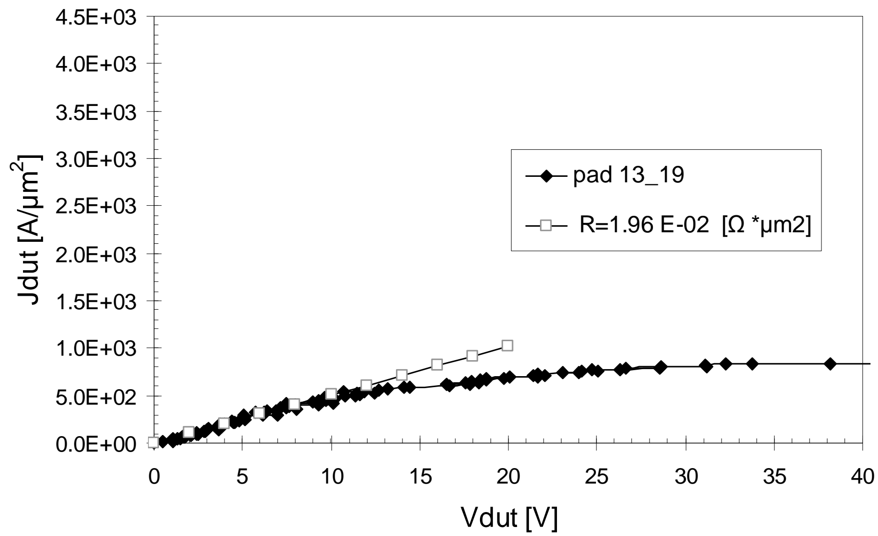


FIG. 5.24 TDR-TLP measure for pads 13 vs. 19

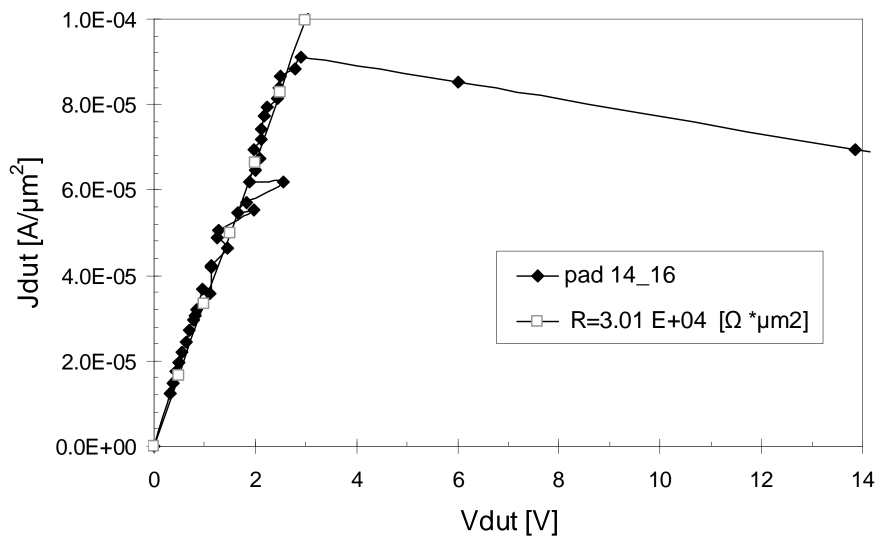


FIG. 5.25 TDR-TLP measure for pads 14 vs. 16

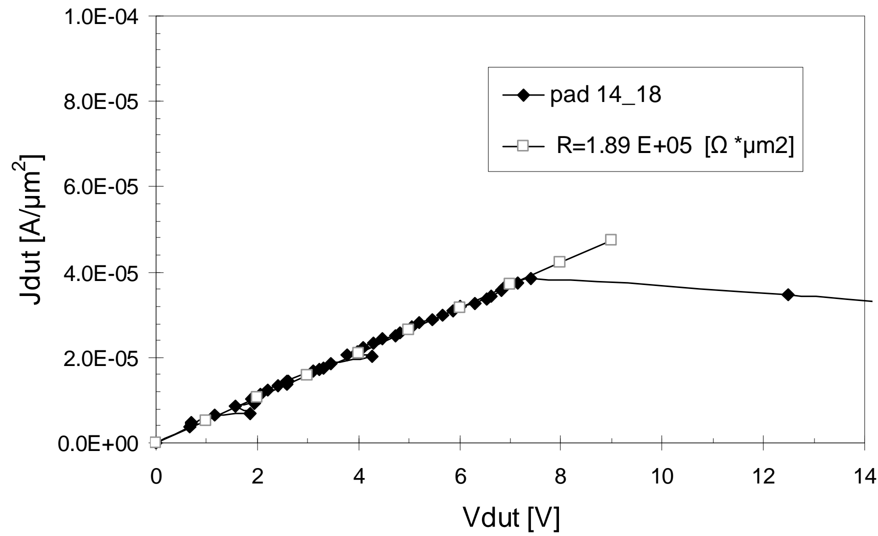


FIG. 5.26 TDR-TLP measure for pads 14 vs. 18

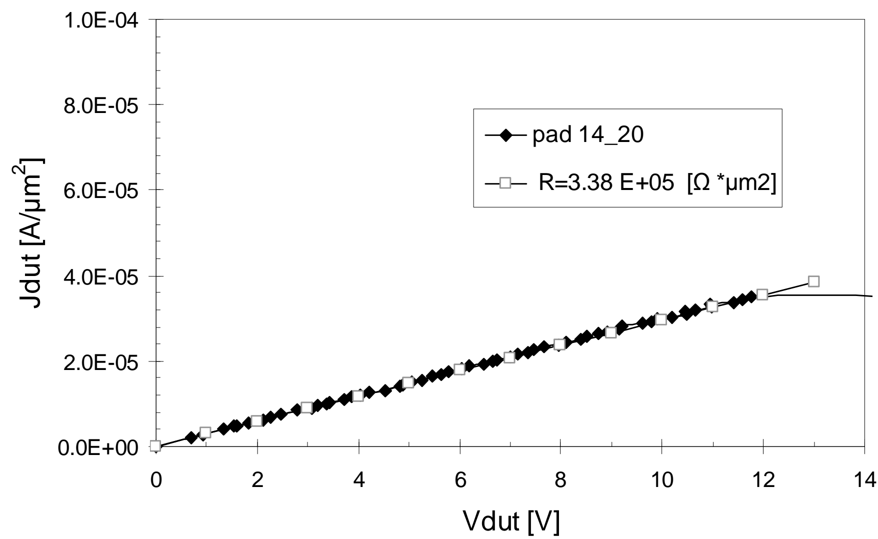


FIG. 5.27 TDR-TLP measure for pads 14 vs. 20

5.2 MOSSWI

The characterization activity continued with the characterization of MOSSWI ESD protection structures (MOSSWI Standard TC, MOSSWI RC NMOS 1.8 V, MOSSWI HV P12 TC). The position of tested structures in the die is shown in the next figure. Devices were named UP/DOWN, with respect of their position from the GND pad.

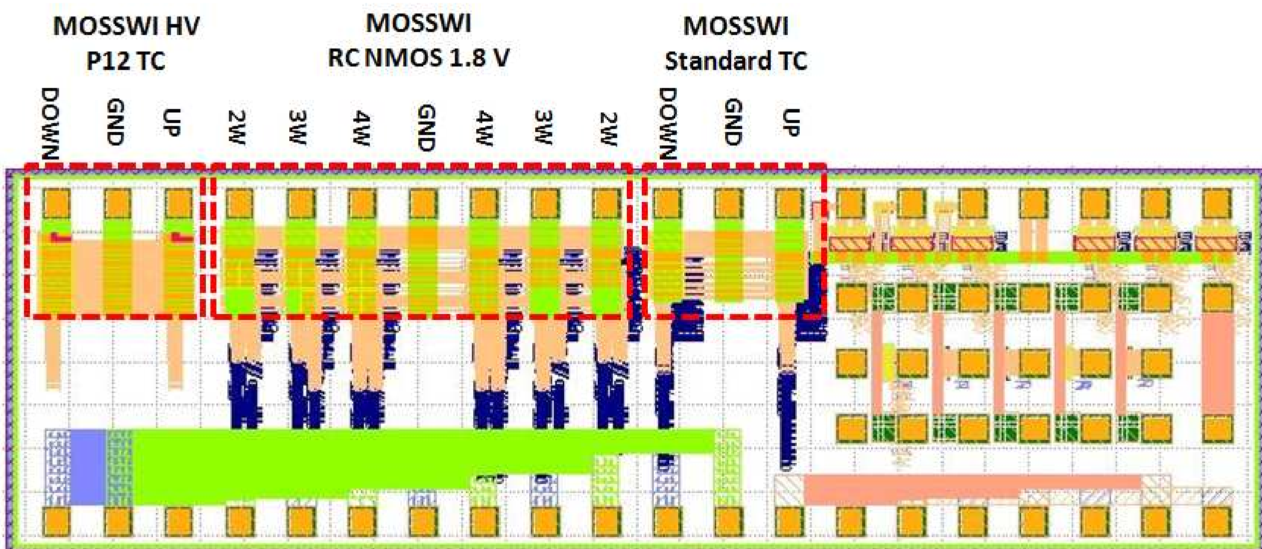


FIG. 5.28 Nomenclature of pads for measures of MOSSWI structures

During the preliminary measurements, devices “UP” showed an I-V behavior similar to a positive bias junction, that probably means that the structures were designed to protect “negative” pins. An example of the I-V curves shown by “UP” devices is reported in the next graph.

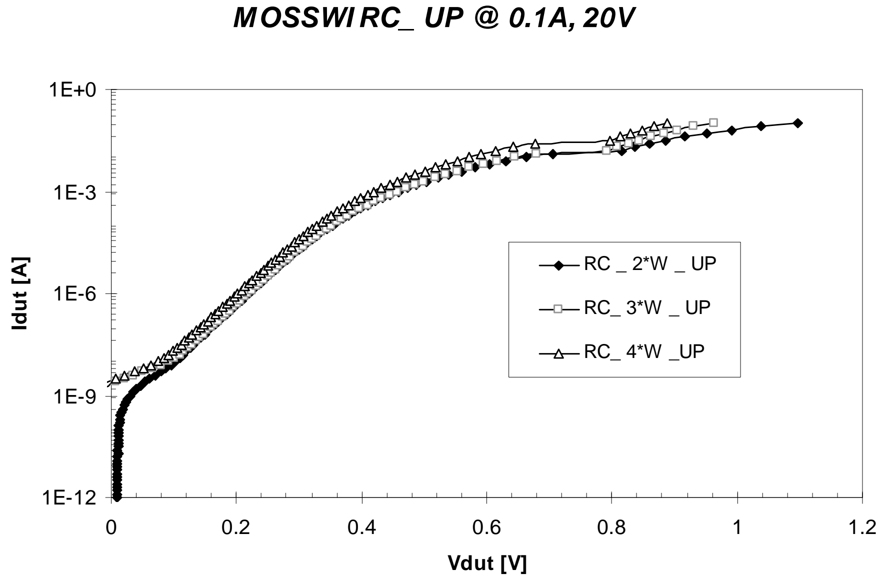


FIG. 5.29 Comparison of DC measures for MOSSWI RC_UP

A similar behavior is shown also by HV devices, as reported in the next graph.

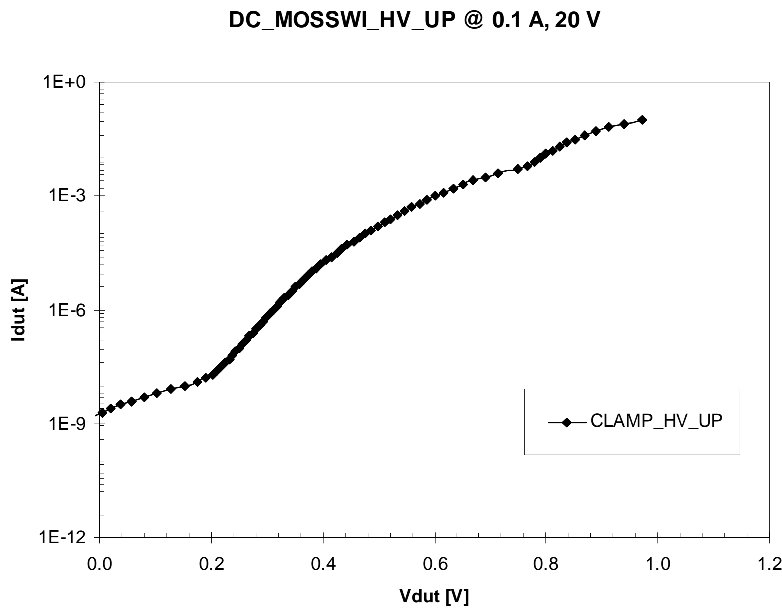


FIG. 5.30 DC measure for MOSSWI HV_UP

The I-V behavior of tested structures in DC regime is shown in the next graphs. Devices were biased in current mode, from 1 pA up to 100 mA, in a logarithmic scale. All tested MOSSWI_DWN structures showed a breakdown voltage of 4.6 V (DC), independently on the device size. Devices “UP” was studied for direct and reverse bias condition.

DIRECT BIAS CONDITION

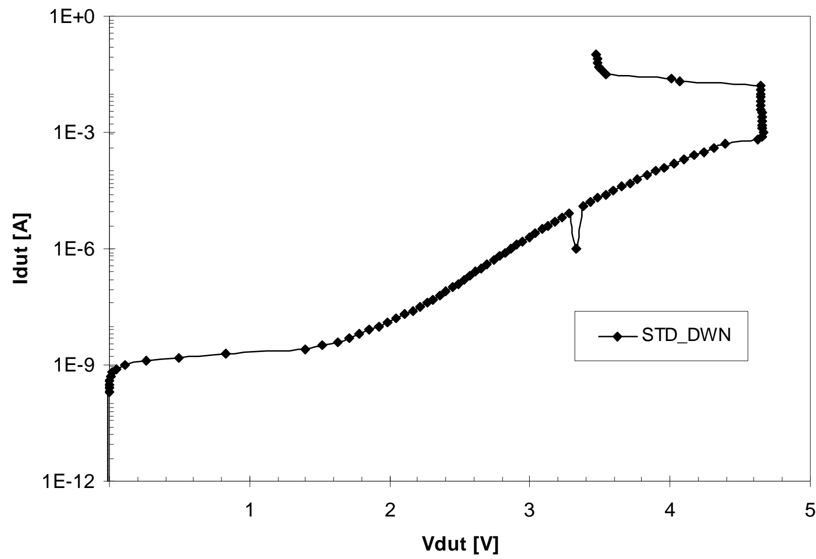


FIG. 5.31 DC measure for MOSSWI STD_DWN

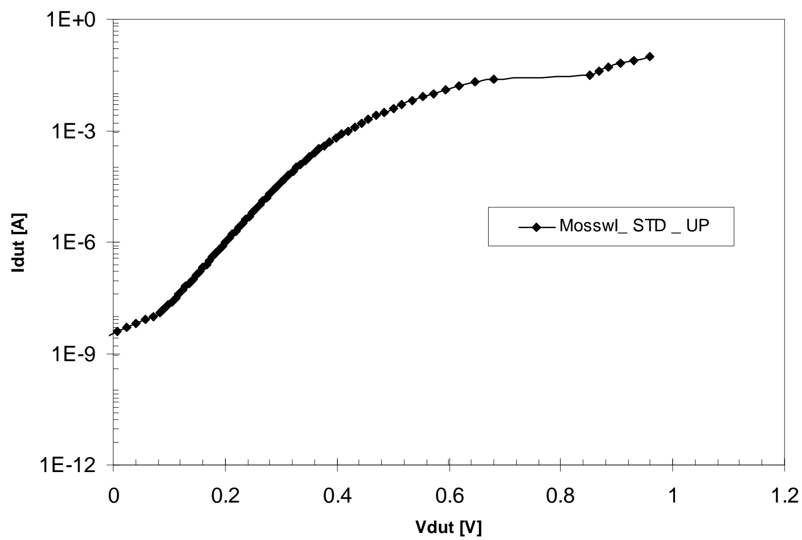


FIG. 5.32 DC measure for MOSSWI STD_UP

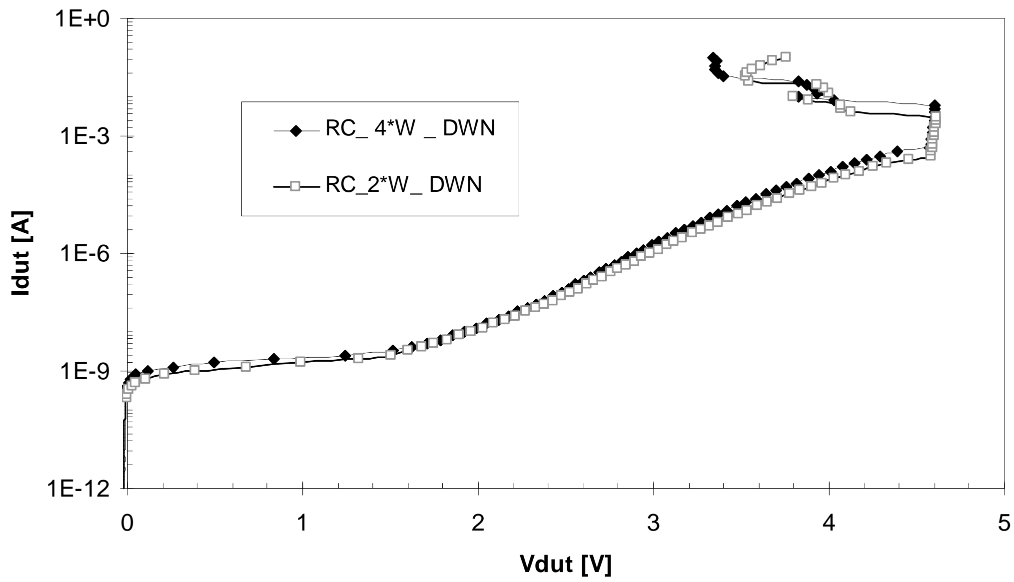


FIG. 5.33 Comparison of DC measures for MOSSWI RC_DWN

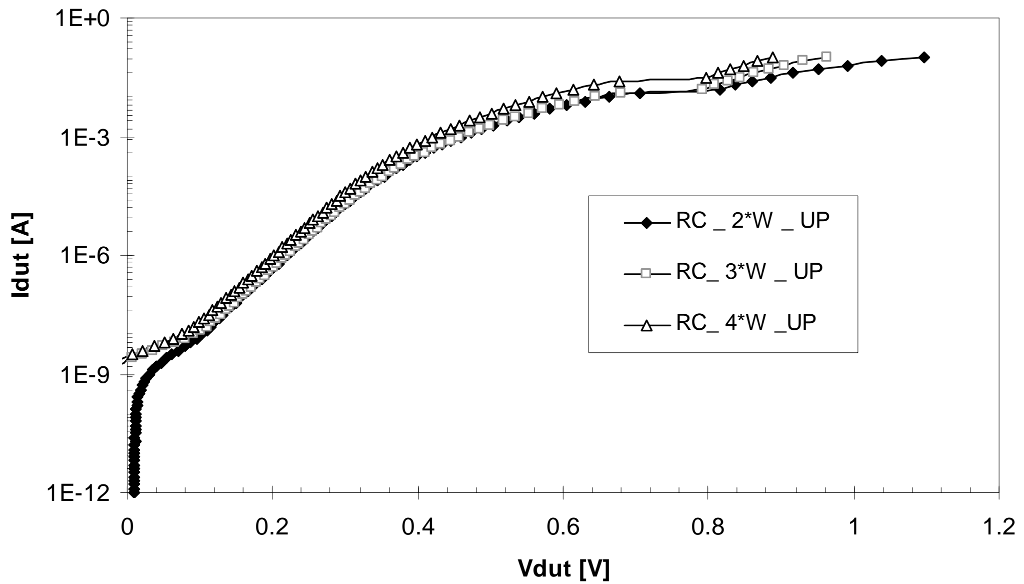


FIG. 5.34 Comparison of DC measures for MOSSWI RC_UP

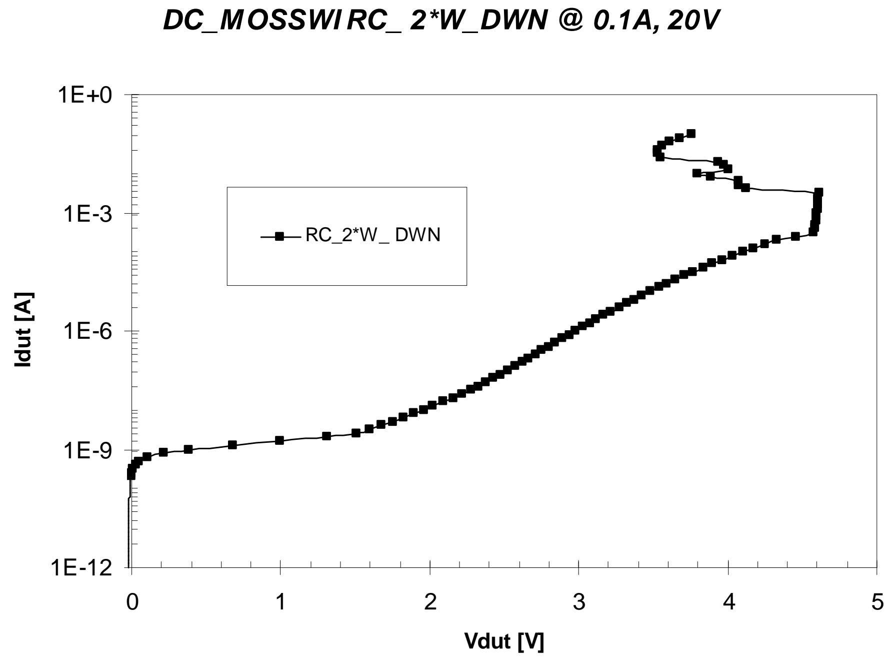


FIG. 5.35 DC measure for MOSSWI RC_DWN

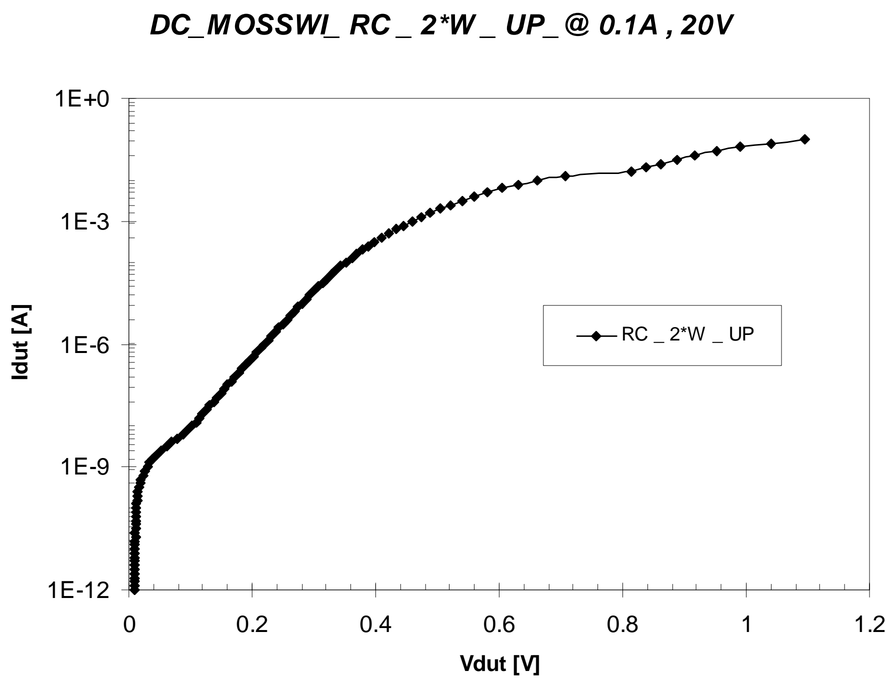


FIG. 5.36 DC measure for MOSSWI RC_UP

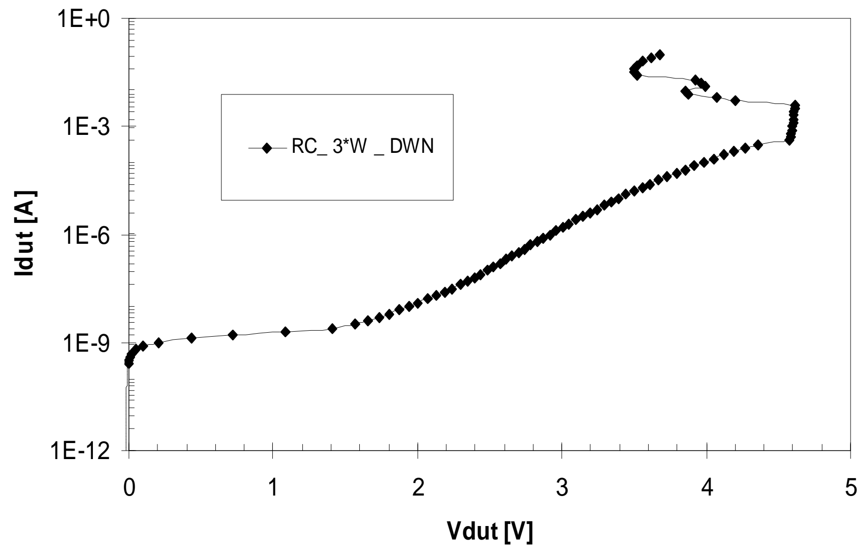


FIG. 5.37 DC measure for MOSSWI RC_DWN

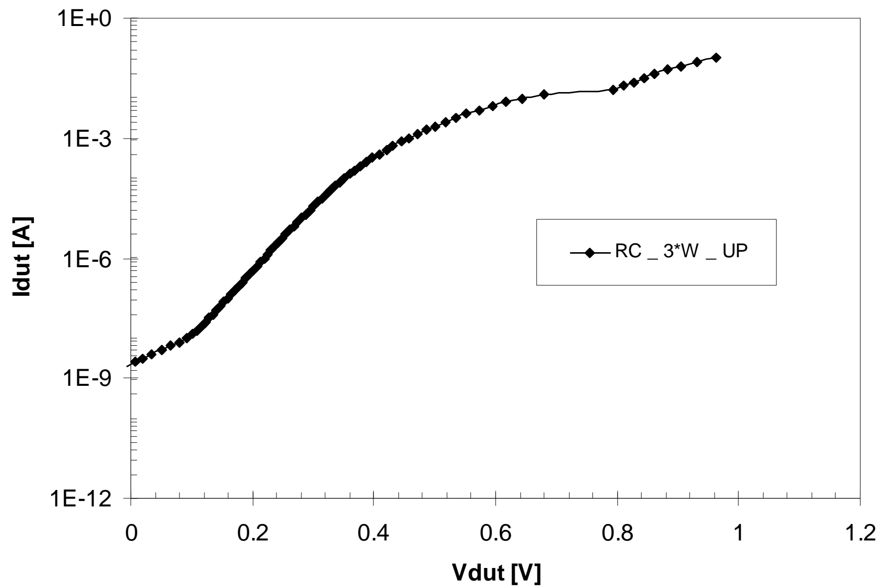


FIG. 5.38 DC measure for MOSSWI RC_UP

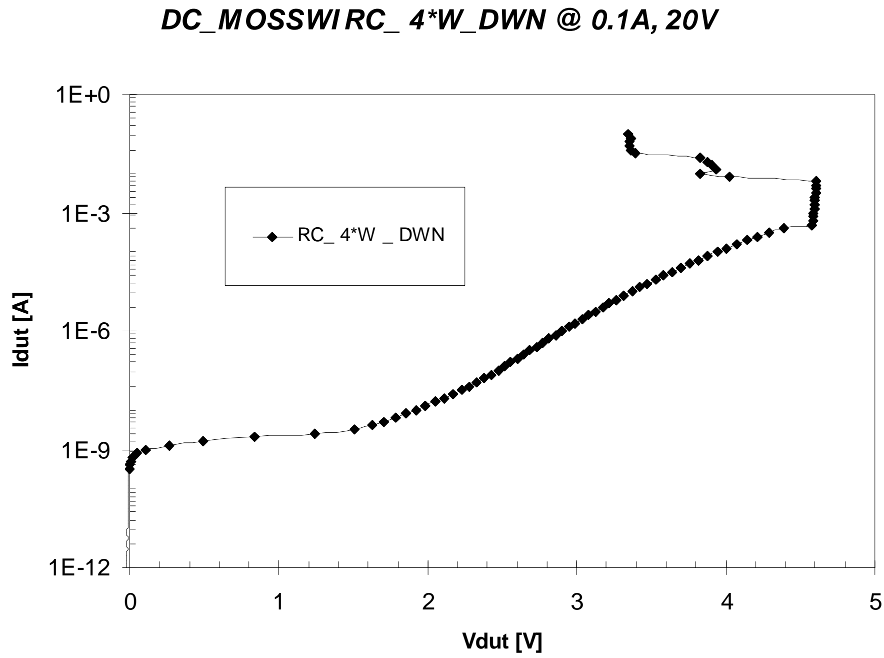


FIG. 5.39 DC measure for MOSSWI RC_DWN

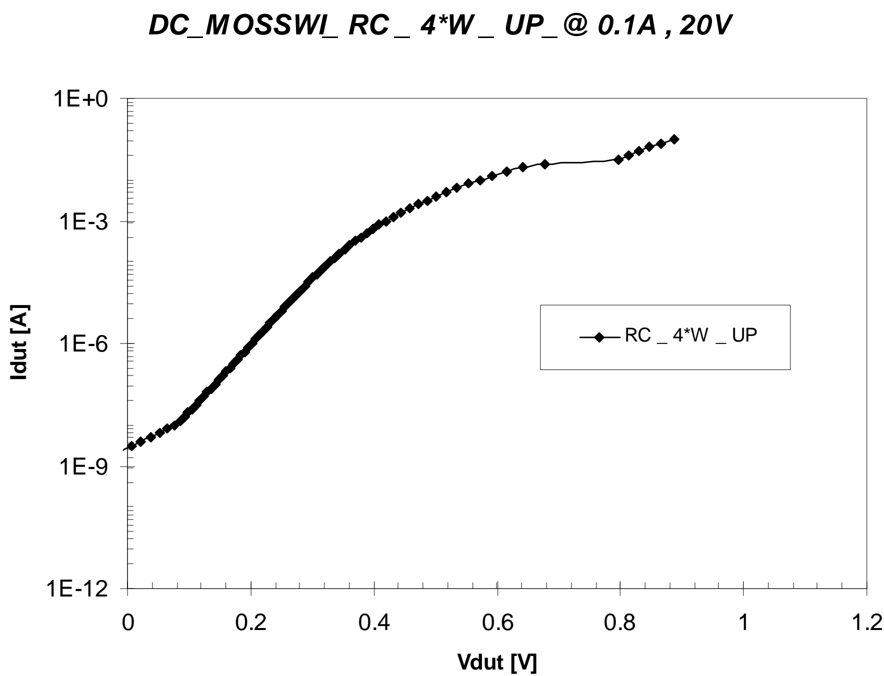


FIG. 5.40 DC measure for MOSSWI RC_UP

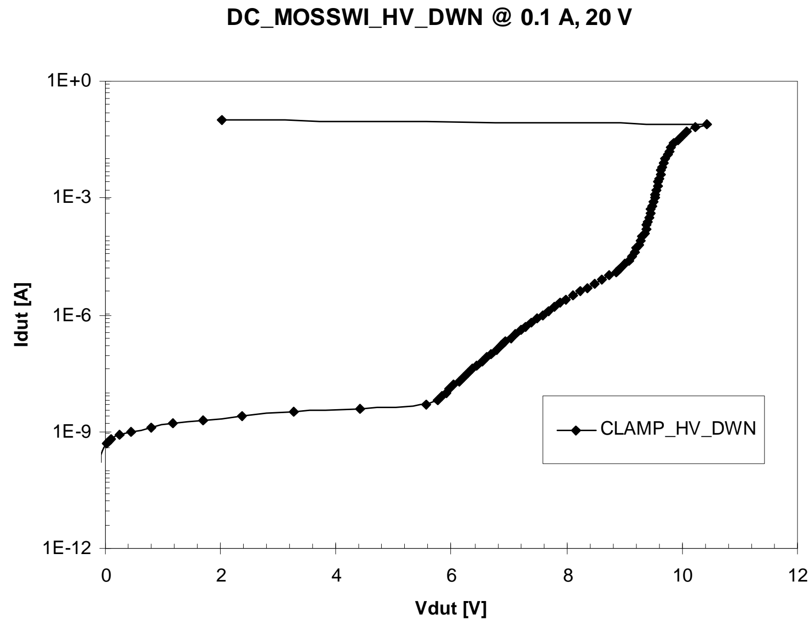


FIG. 5.41 DC measure for MOSSWI HV_DWN

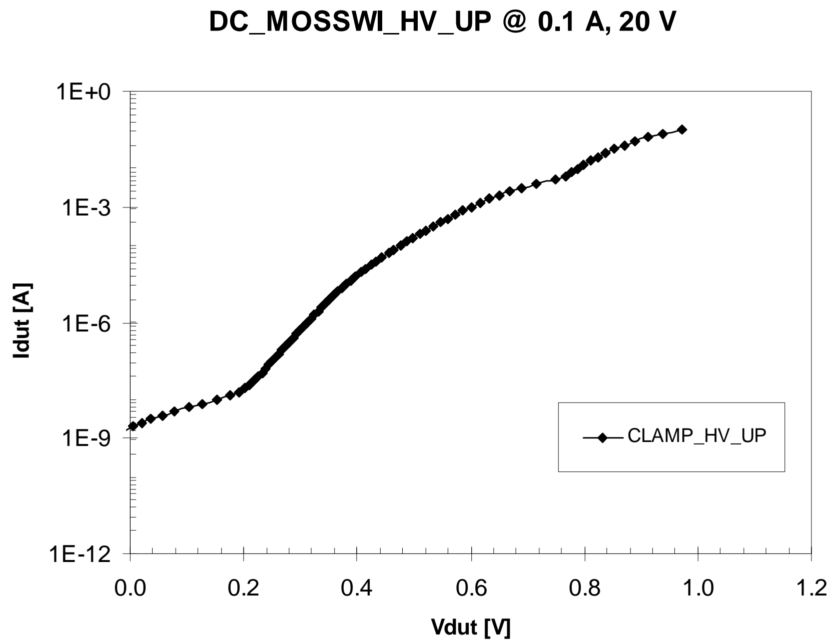


FIG. 5.42 DC measure for MOSSWI HV_UP

REVERSE BIAS CONDITION

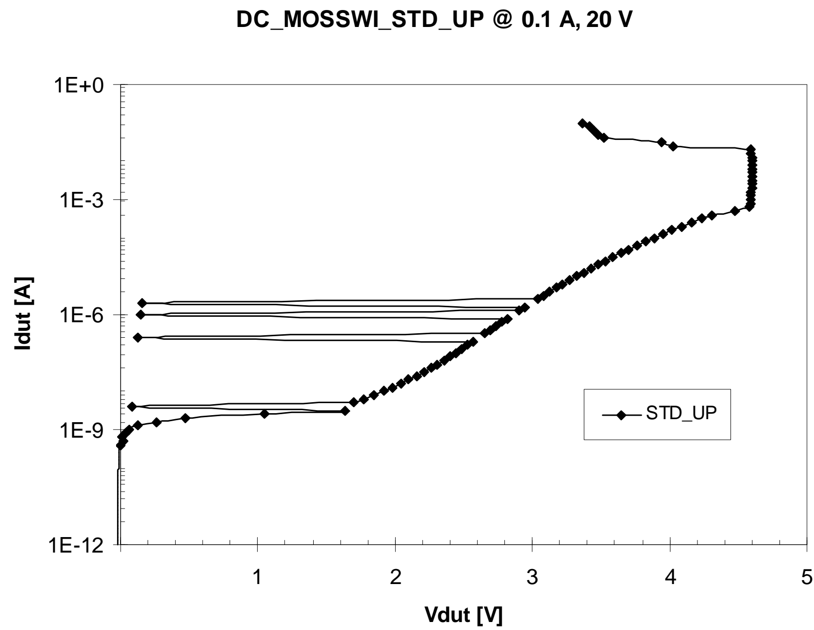


FIG. 5.43 DC measure for MOSSWI STD_UP under reverse bias condition

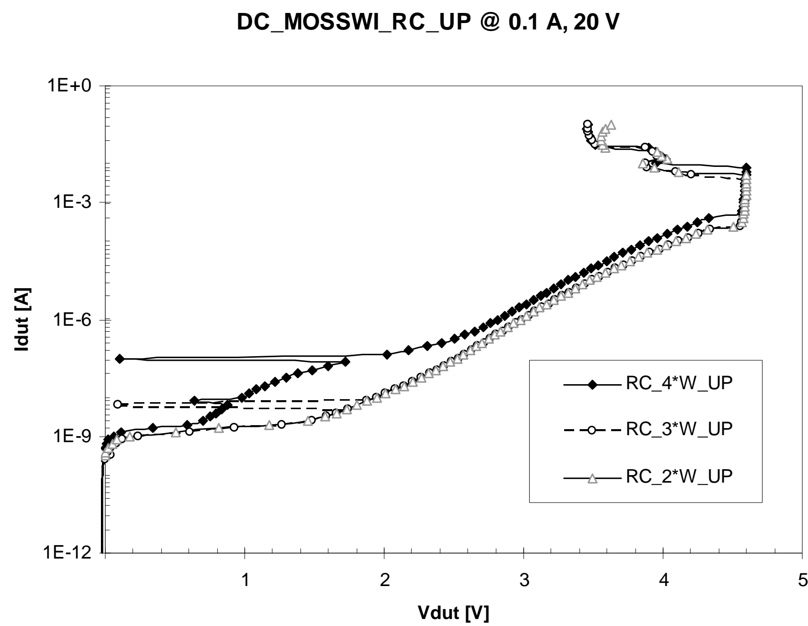


FIG. 5.44 Comparison of DC measures for MOSSWI RC_UP under reverse bias condition

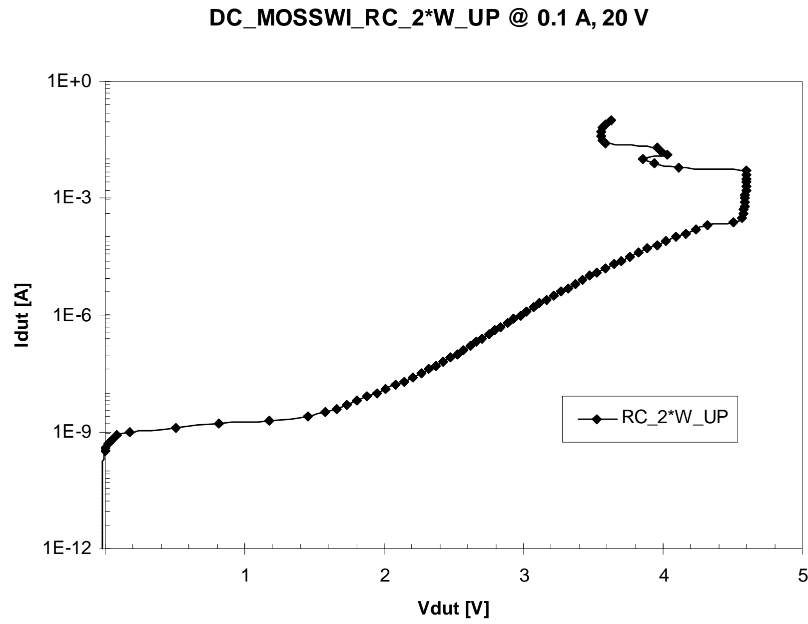


FIG. 5.45 DC measure for MOSSWI RC_UP under reverse bias condition

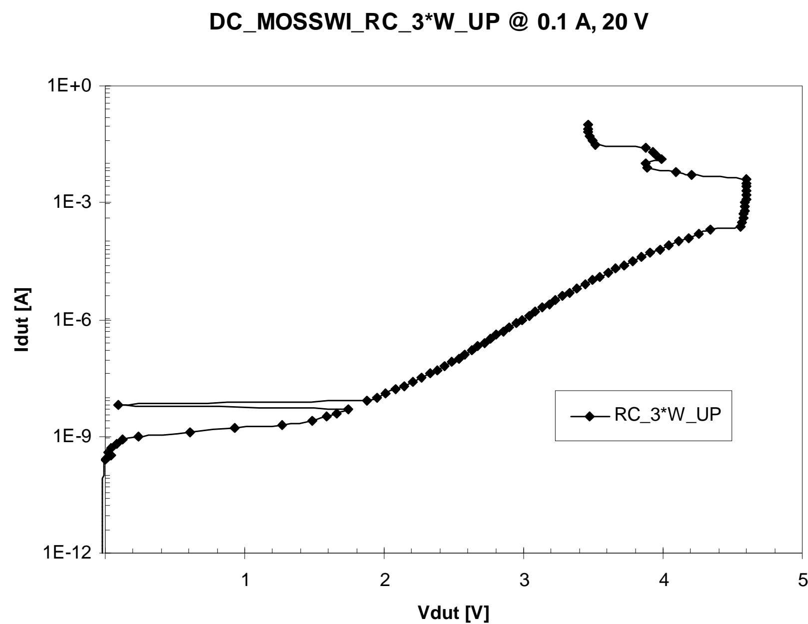


FIG. 5.46 DC measure for MOSSWI RC_UP under reverse bias condition

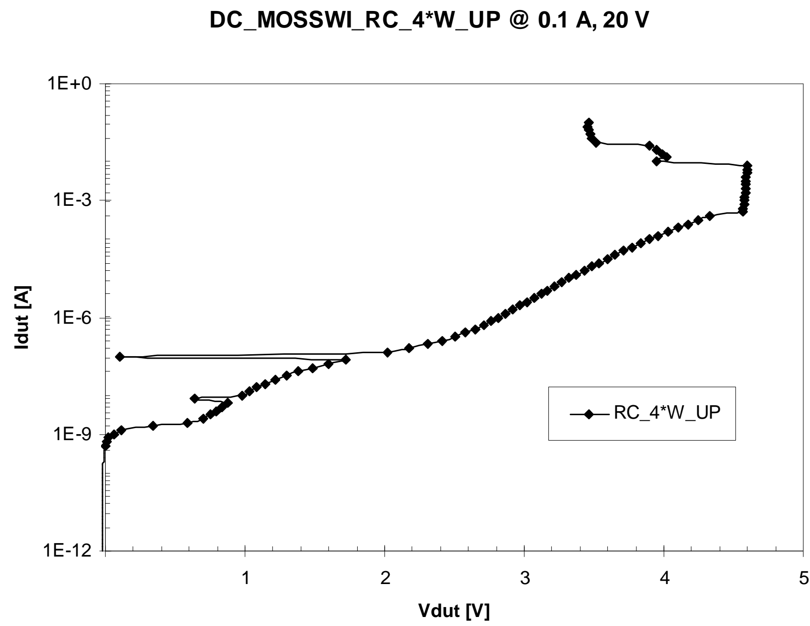


FIG. 5.47 DC measure for MOSSWI RC_UP under reverse bias condition

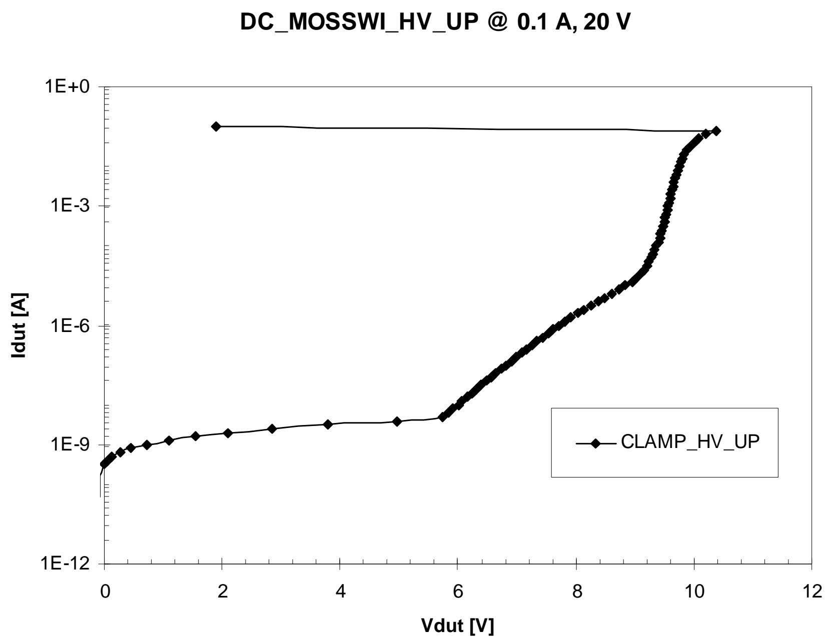


FIG. 5.48 DC measure for MOSSWI HV_UP under reverse bias condition

Devices have then been characterized in 100 ns TLP regime, extracting the main electrical parameters reported in the next table (leakage measured @ 1.8 V for all DWN devices and UP devices on reverse bias condition, @ 0.1V for UP devices on direct bias condition). Only HV_UP in direct bias condition has been measured @ 0.3V and @1V, because at lower value (like 0.1 V) the measures show an unexpected behavior (look at next graphs).

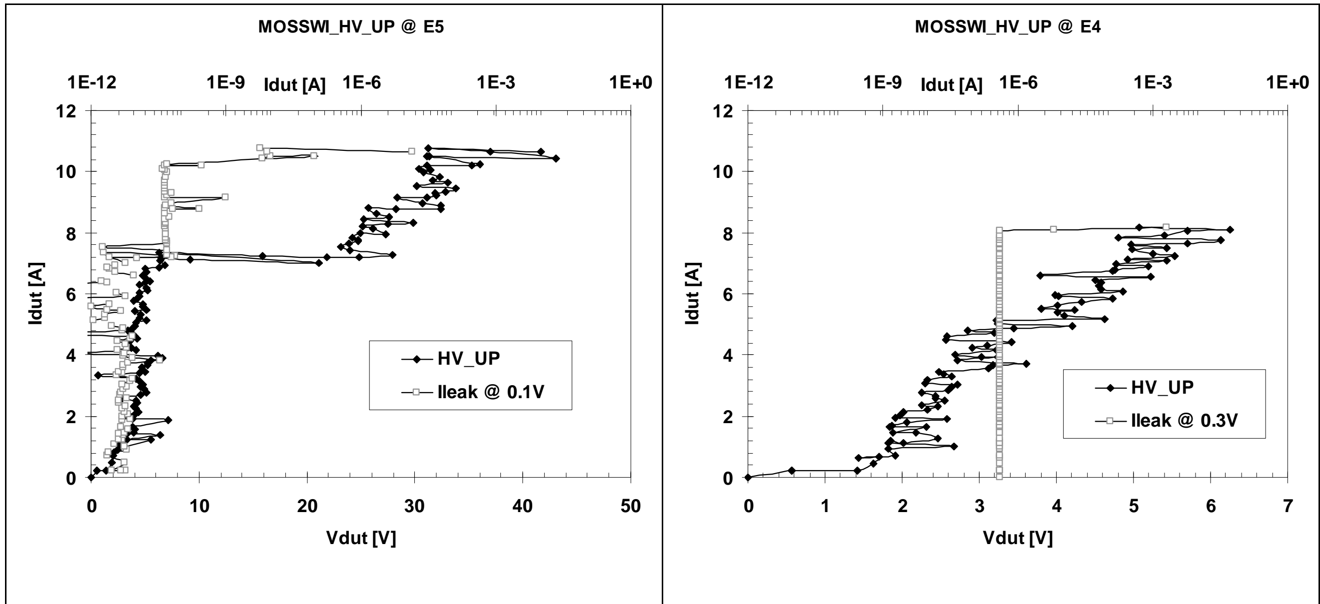


FIG. 5.49 TDR-TLP measures for MOSSWI HV_UP @ 0.3V and @1V under direct bias condition

MOSSWI	BIAS CONDITION	I_{fail} (A)	V_{fail} (V)	$I_{leakage}$ (nA)
RC_2*W_UP	DIRECT	4.49	19.00	8.32
RC_2*W_UP	REVERSE	2.70	12.3	6.10
RC_2*W_DWN	DIRECT	2.40	13.6	10.8
RC_3*W_UP	DIRECT	6.96	21.15	8.44
RC_3*W_UP	REVERSE	3.40	11.30	6.80
RC_3*W_DWN	DIRECT	4.60	11.10	10.5
RC_4*W_UP	DIRECT	9.01	15.22	17.1
RC_4*W_UP	REVERSE	7.40	9.60	7.30
RC_4*W_DWN	DIRECT	5.90	9.80	9.70
STD_UP	DIRECT	10.65	10.76	16.9
STD_UP	REVERSE	3.90	6.20	6.90
STD_DWN	DIRECT	4.90	11.10	11.90
HV_UP	DIRECT (@ 0.3V)	8.11	6.25	397.00
HV_UP	REVERSE	3.72	11.17	9.06
HV_DWN	DIRECT	3.28	10.05	19.07

I-V curves are shown in the next pages, for direct and reverse bias conditions.

DIRECT BIAS CONDITION

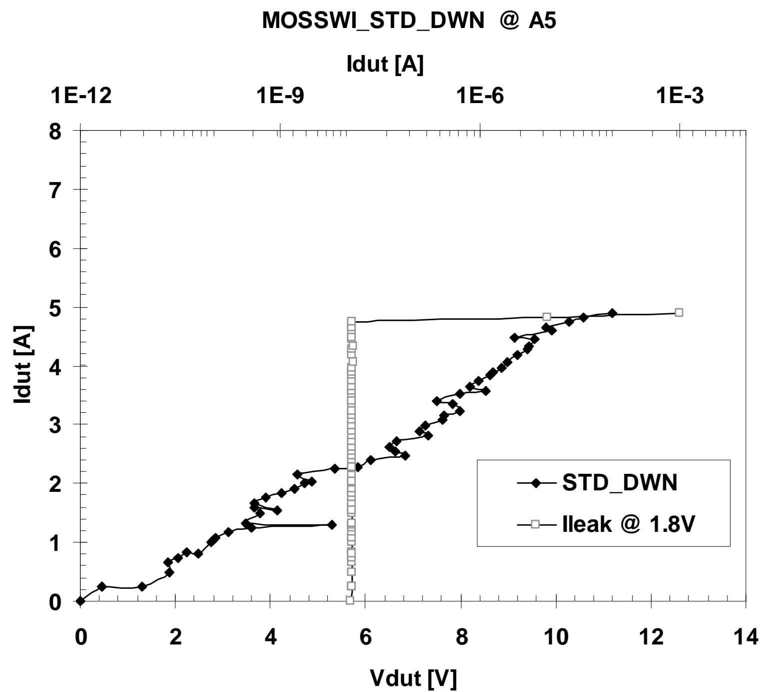


FIG. 5.50 TDR-TLP measure for MOSSWI STD_UP under direct bias condition

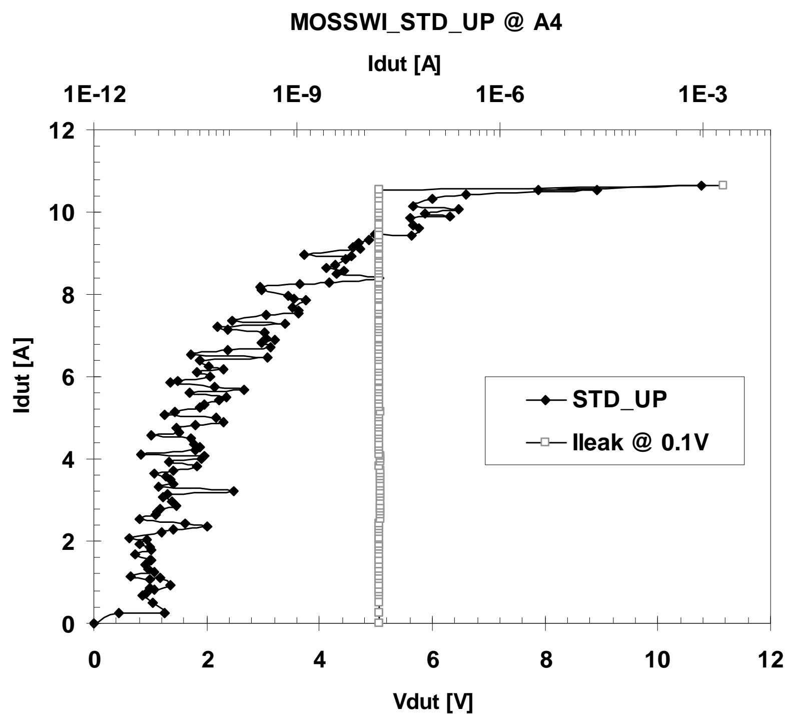


FIG. 5.51 TDR-TLP measure for MOSSWI STD_UP under direct bias condition

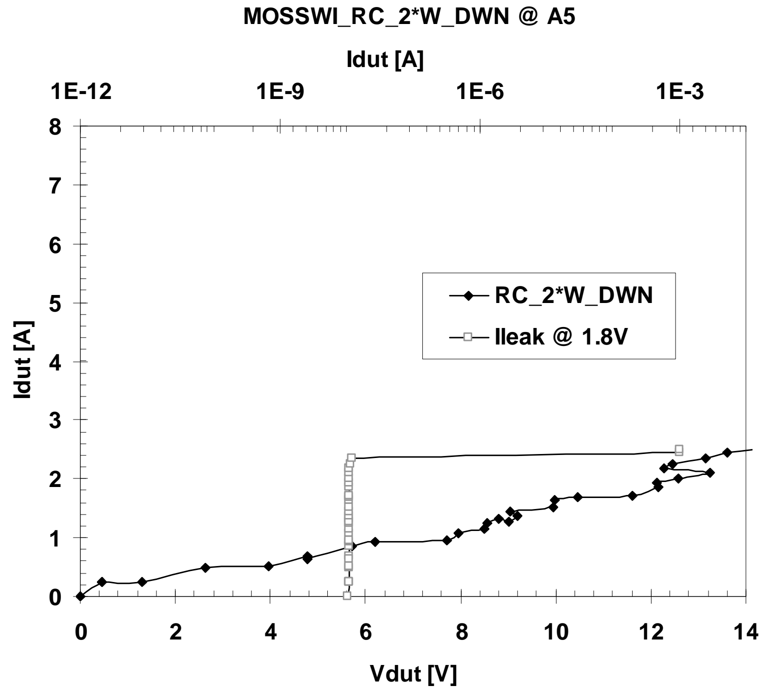


FIG. 5.52 TDR-TLP measure for MOSSWI RC_DWN under direct bias condition

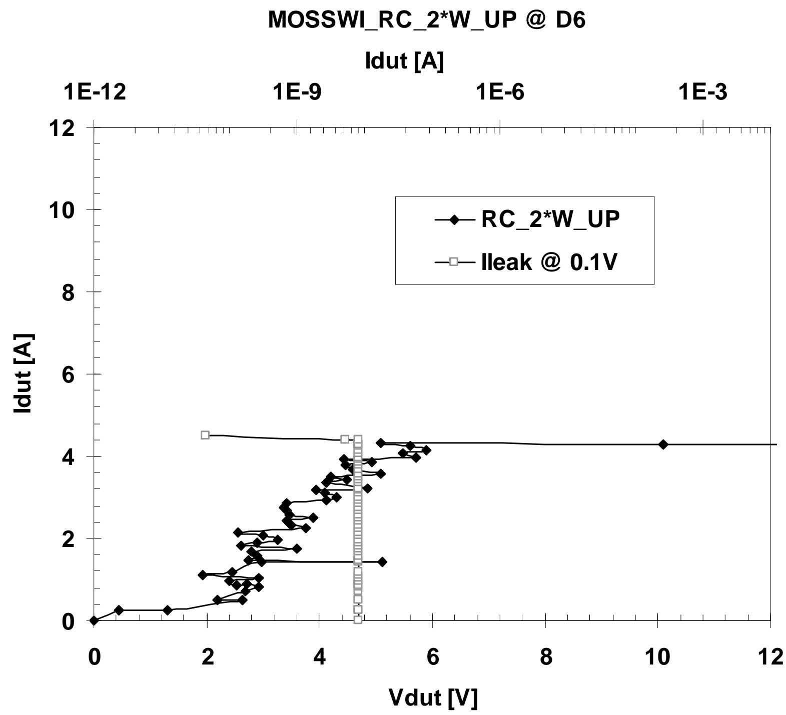


FIG. 5.53 TDR-TLP measure for MOSSWI RC_UP under direct bias condition

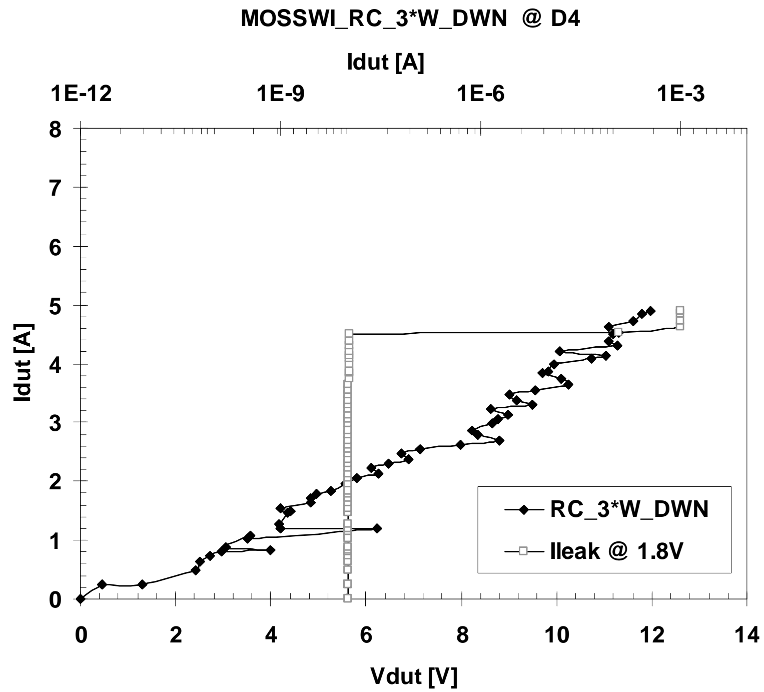


FIG. 5.54 TDR-TLP measure for MOSSWI RC_DWN under direct bias condition

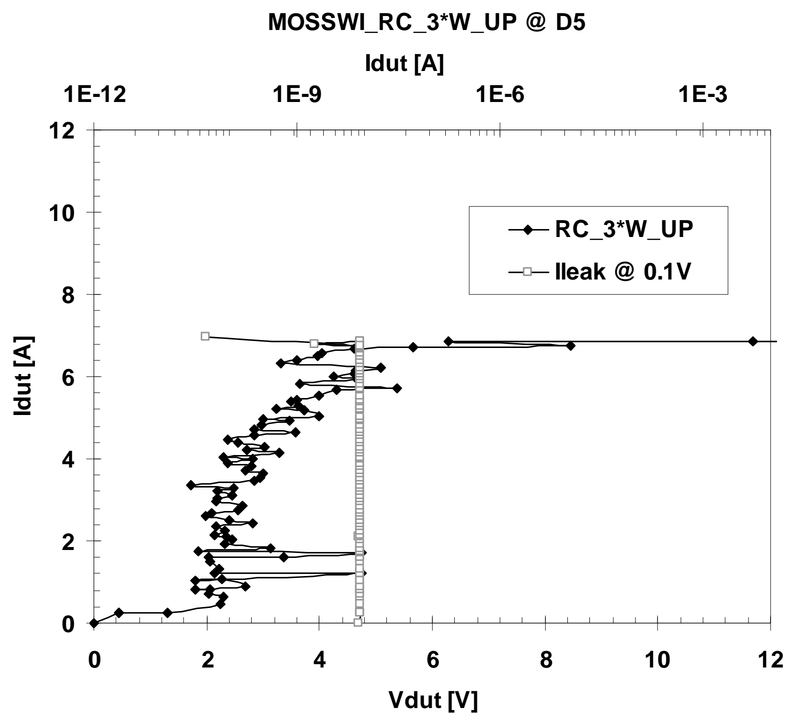


FIG. 5.55 TDR-TLP measure for MOSSWI RC_UP under direct bias condition

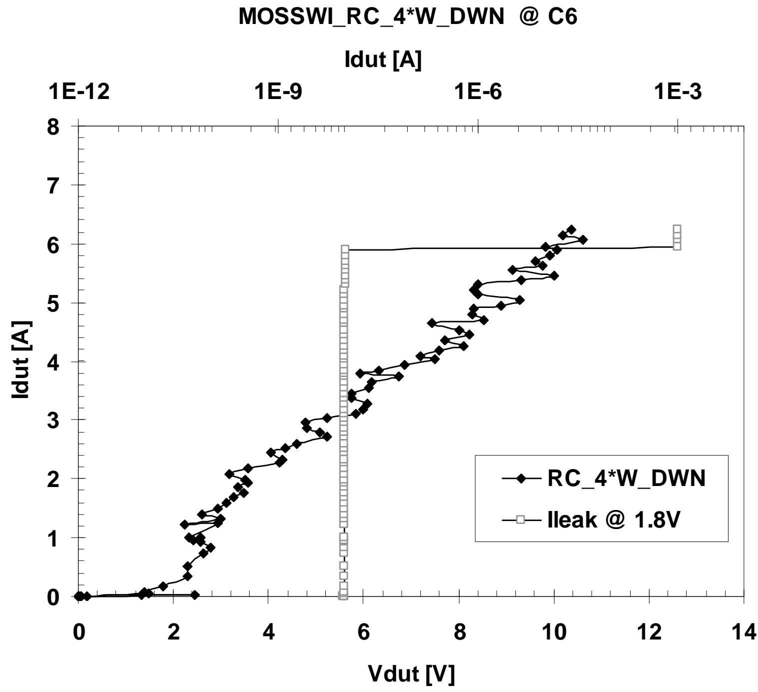


FIG. 5.56 TDR-TLP measure for MOSSWI RC_DWN under direct bias condition

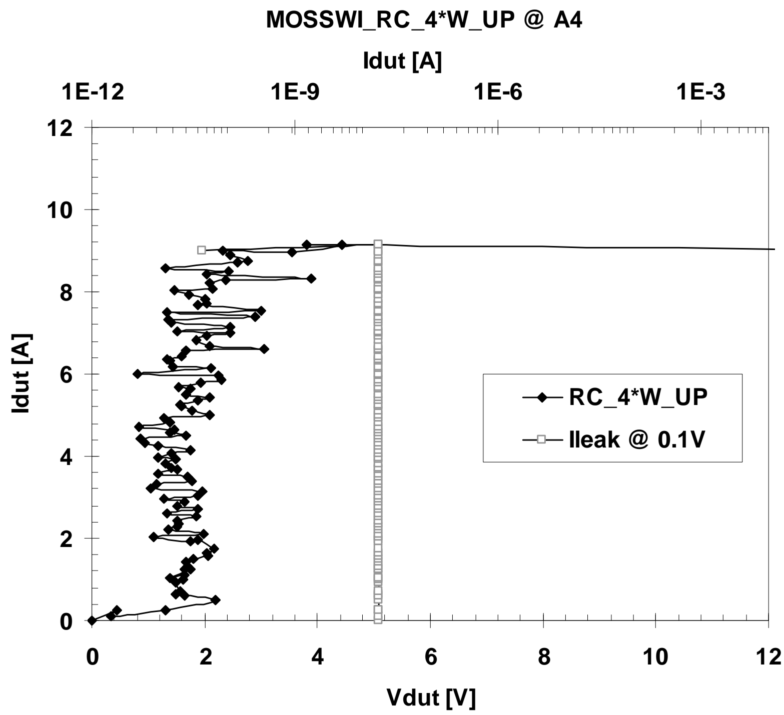


FIG. 5.57 TDR-TLP measure for MOSSWI RC_UP under direct bias condition

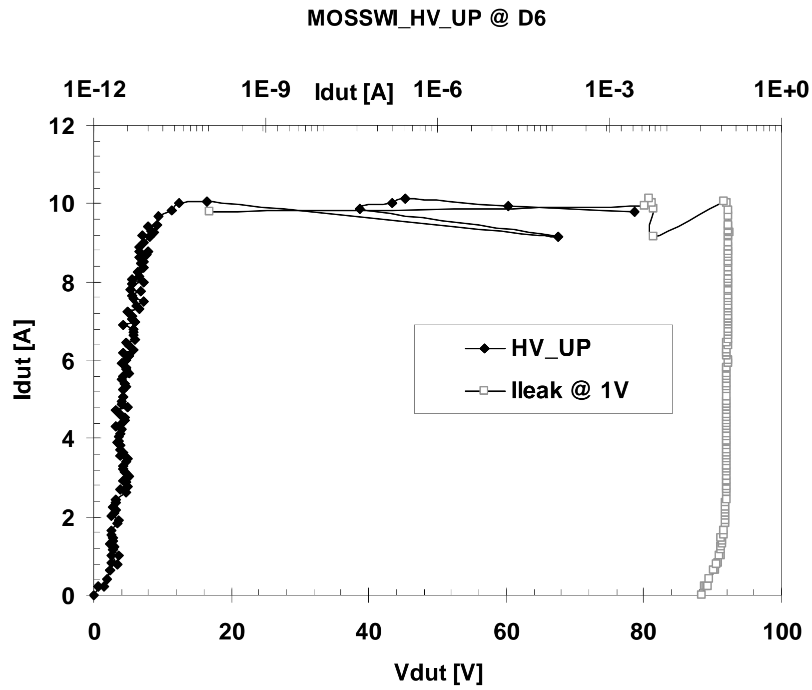


FIG. 5.58 TDR-TLP measure for MOSSWI HV_UP @1V

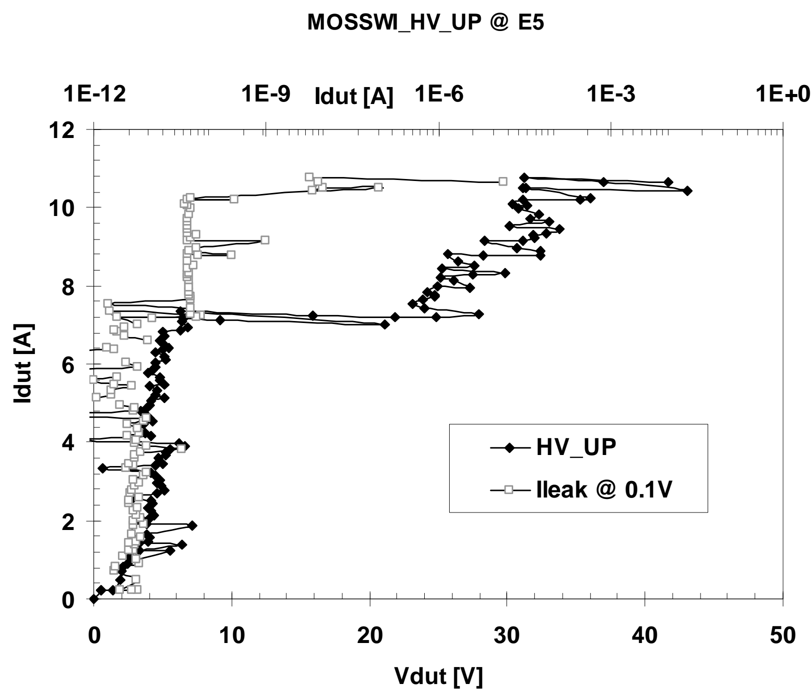


FIG. 5.59 TDR-TLP measure for MOSSWI HV_UP @0.1V

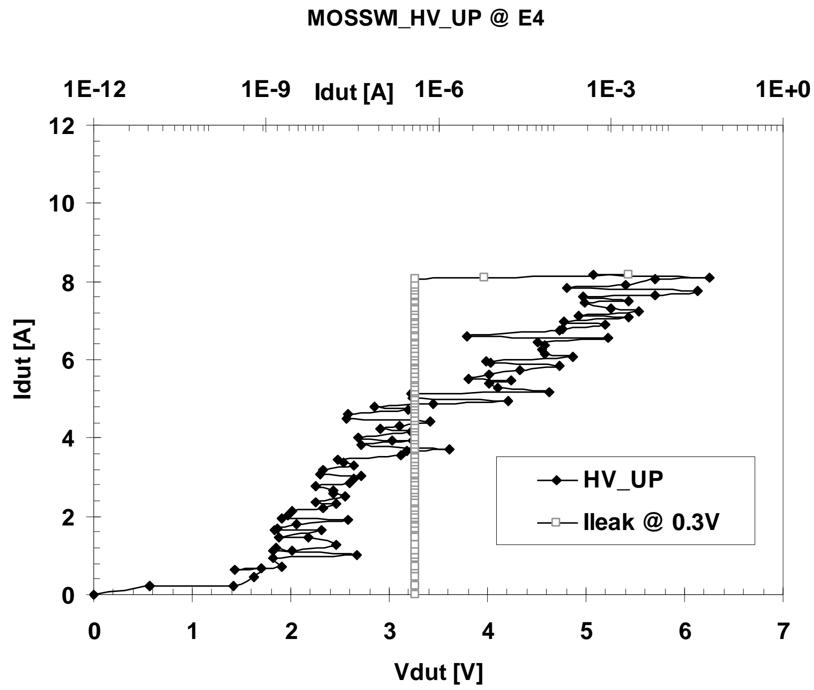


FIG. 5.60 TDR-TLP measure for MOSSWI HV_UP @0.3V

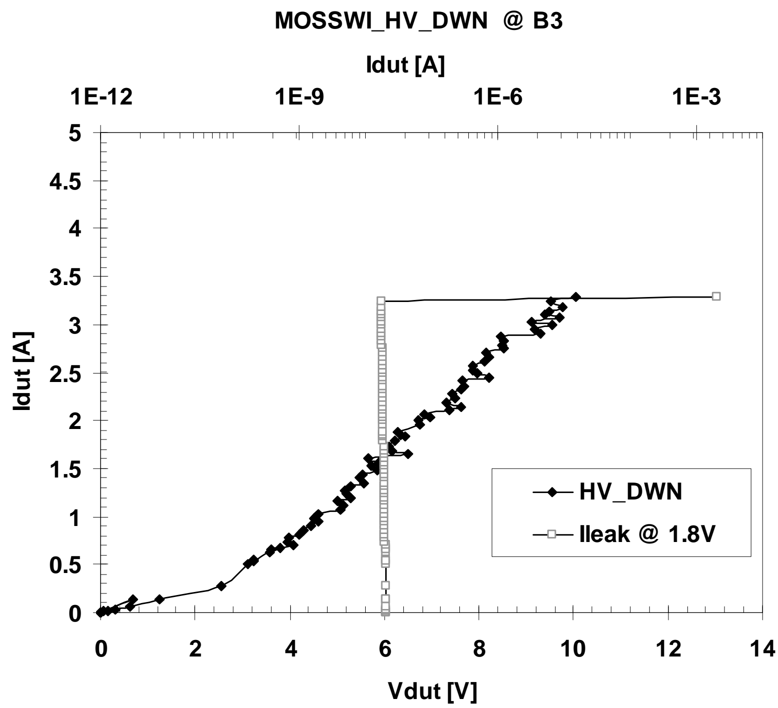


FIG. 5.61 TDR-TLP measure for MOSSWI HV_DWN under direct bias condition

REVERSE BIAS CONDITION

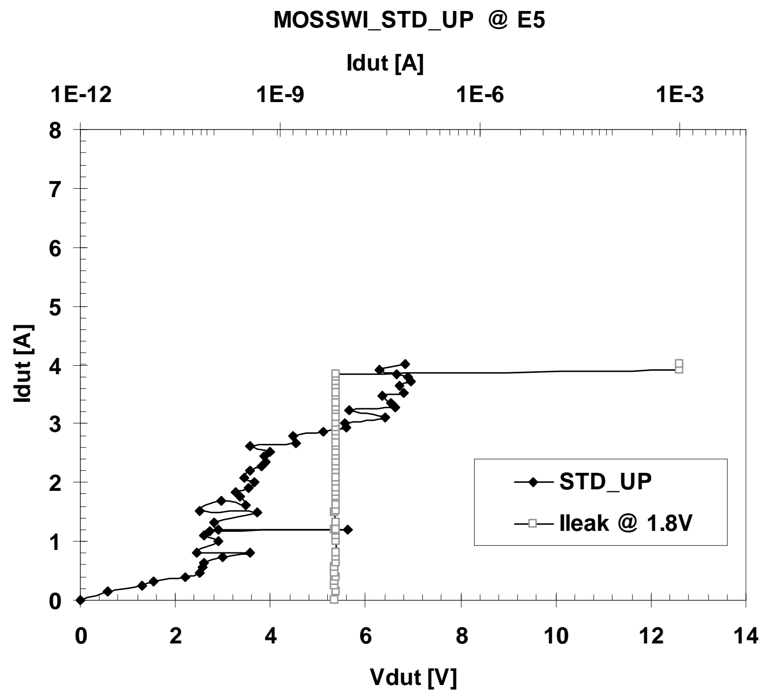


FIG. 5.62 TDR-TLP measure for MOSSWI STD_UP under reverse bias condition

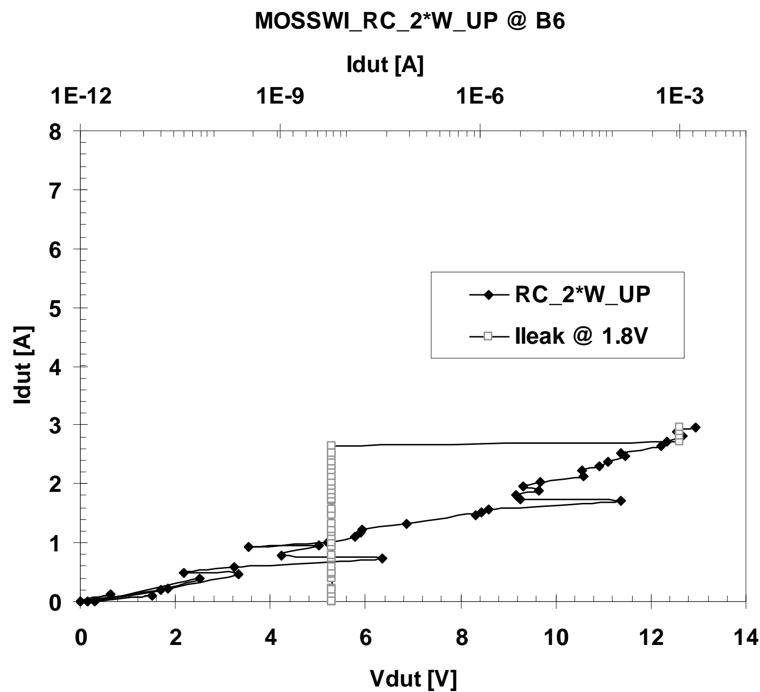


FIG. 5.63 TDR-TLP measure for MOSSWI RC_UP under reverse bias condition

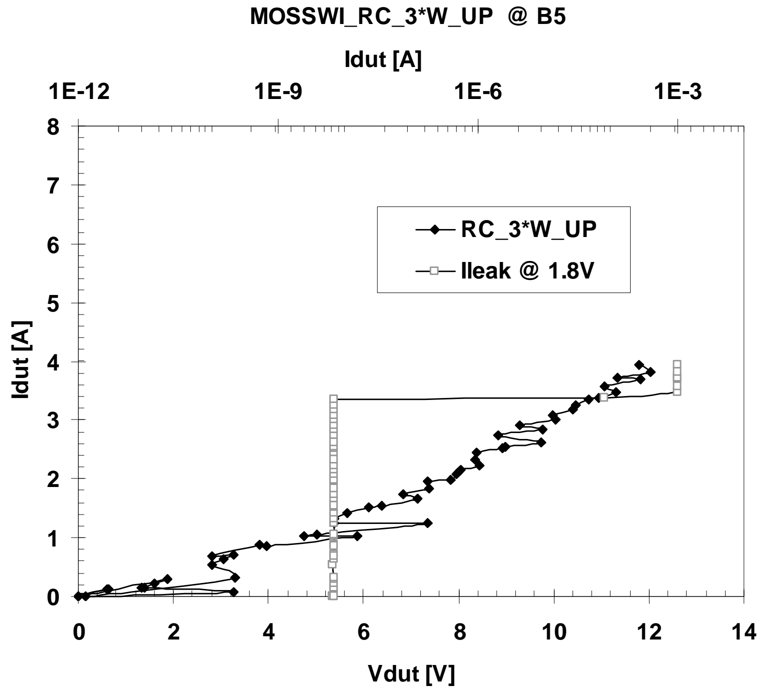


FIG. 5.64 TDR-TLP measure for MOSSWI RC_UP under reverse bias condition

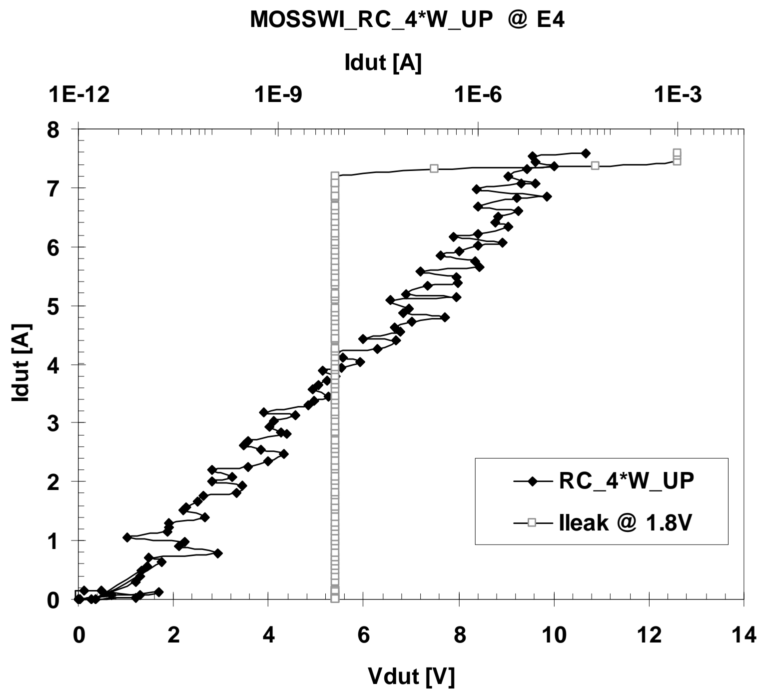


FIG. 5.65 TDR-TLP measure for MOSSWI RC_UP under reverse bias condition

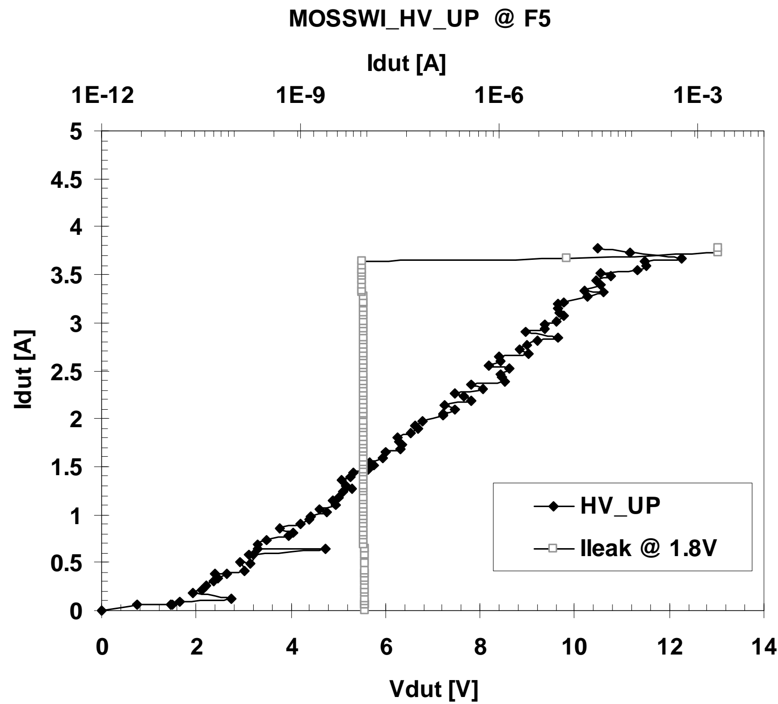


FIG. 5.66 TDR-TLP measure for MOSSWI HV_UP under reverse bias condition

5.3 Vpp Protections

The characterization activity continued with the characterization of Vpp protections structures (Vpp TC, and Vpp TEST). The position of tested structures in the die is shown in the next figure.

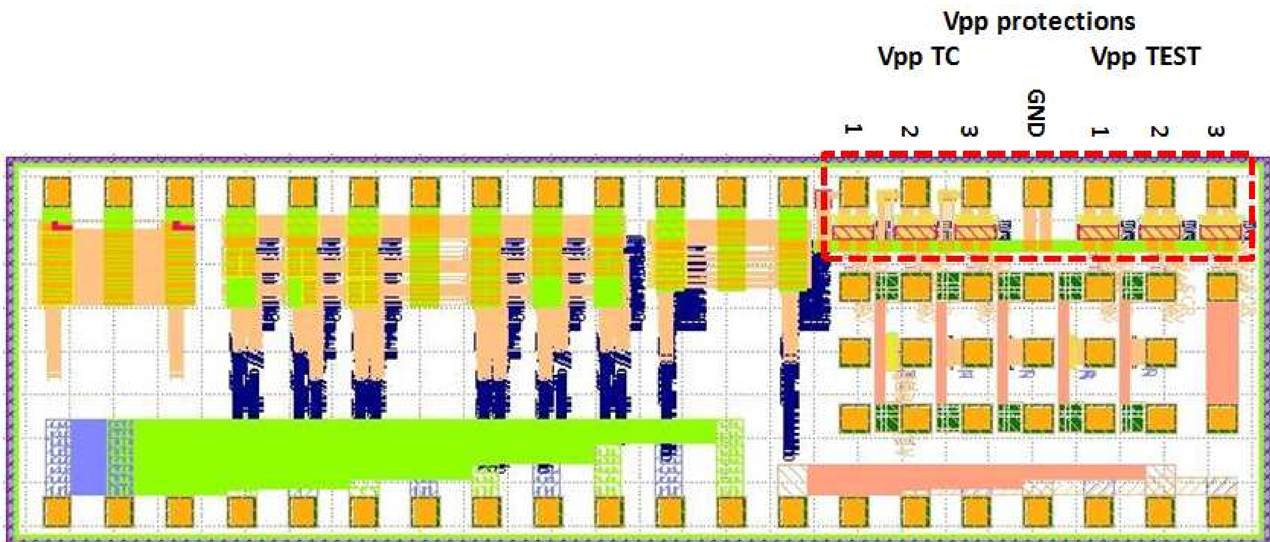


FIG. 5.67 Nomenclature of pads for measures of Vpp protection structures

The comparison of the behavior shown by TEST and TC Vpp Protection structures in DC regime is shown in the following graphs.

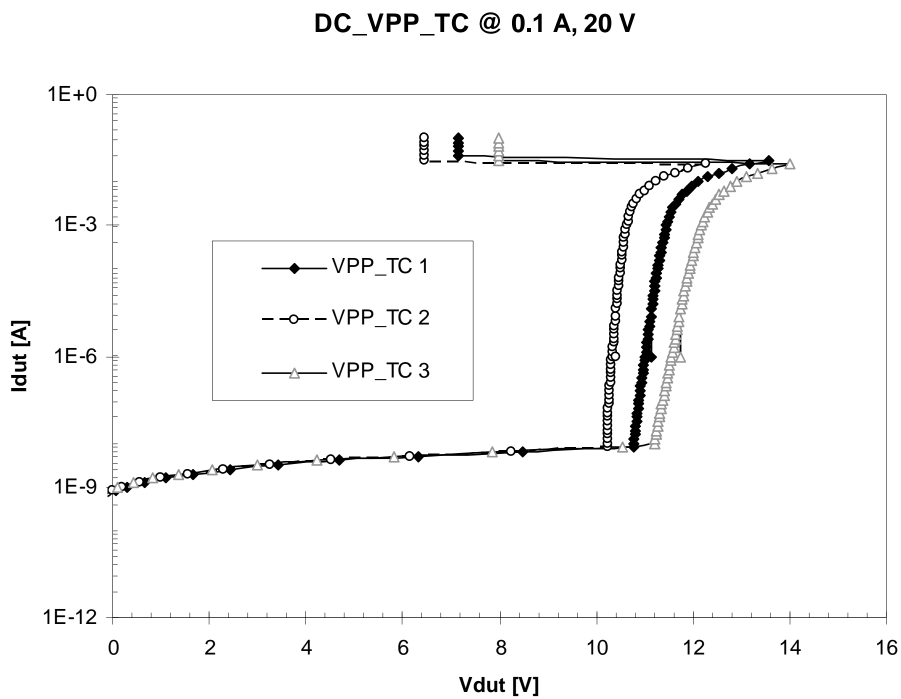


FIG. 5.68 Comparison of DC measures for VPP_TC

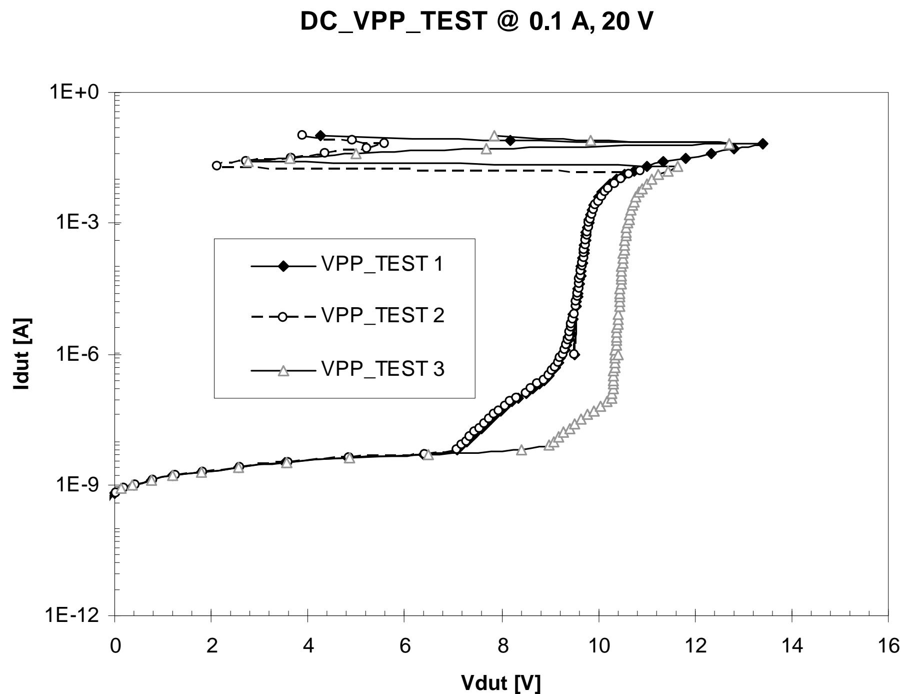


FIG. 5.69 Comparison of DC measures for VPP_TEST

Devices have then been characterized in 100 ns TLP regime, extracting the main electrical parameters reported in the next table (leakage measured @ 1.8 V). I-V curves are shown in the next pages.

Vpp Protections	I_{fail} (A)	V_{fail} (V)	$I_{leakage}$ (nA)	Res_(Ω) TLP
TC_1	5.75	26.01	0.42	2.81
TC_2	4.75	22.11	0.29	2.36
TC_3	5.79	28.70	0.32	2.93
TEST_1	5.58	28.92	0.157	3.44
TEST_2	0.92	7.56	180.00	11.00
TEST_3	0.35	9.28	15.7	22.43

As it is possible to see from the graphs, devices Vpp TEST 2 and TEST 3 have shown a strong degradation of the leakage curve during the TLP stress, almost after the turn-on of the protection structure. On the contrary, all other Vpp protection structures have shown an hard-breakdown, and quite high failure level (about ~5 A).

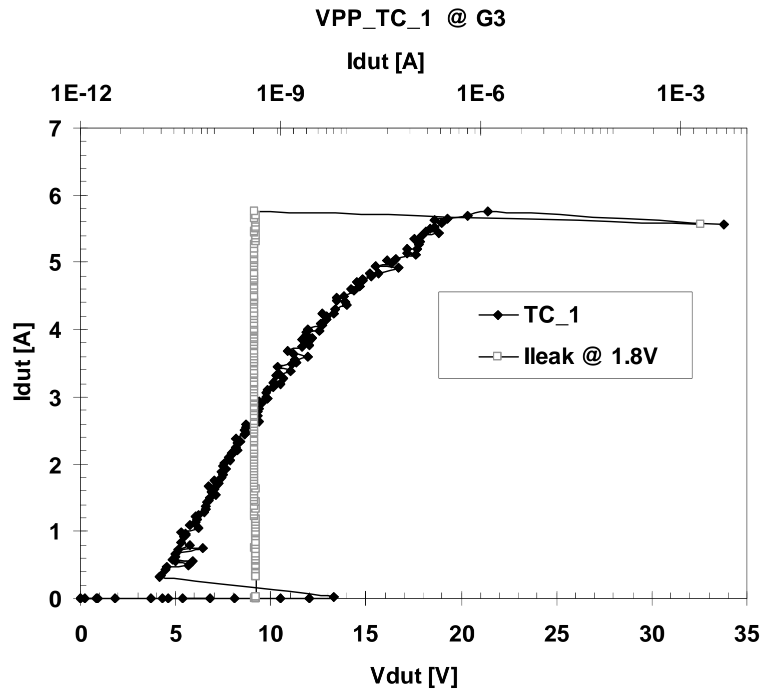


FIG. 5.70 DC measure for VPP_TC

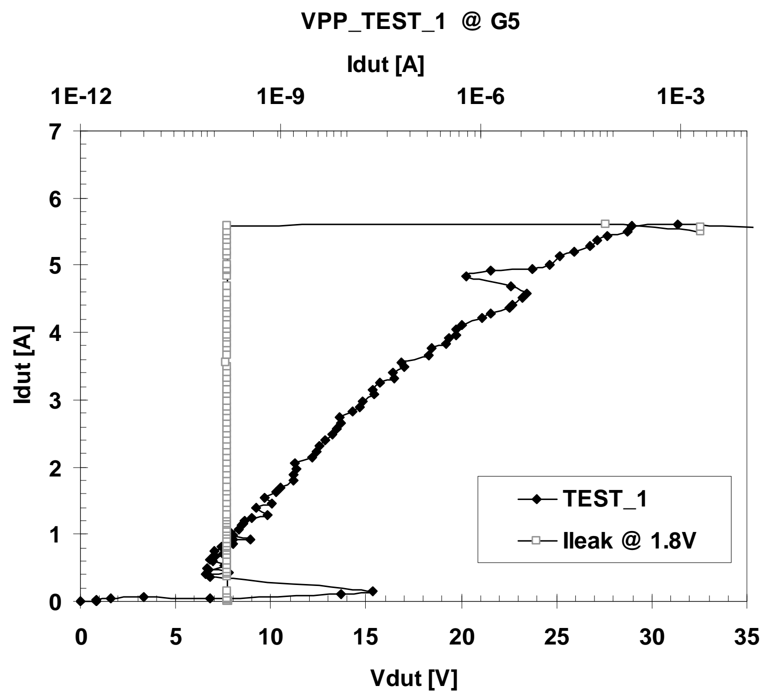


FIG. 5.71 DC measure for VPP_TEST

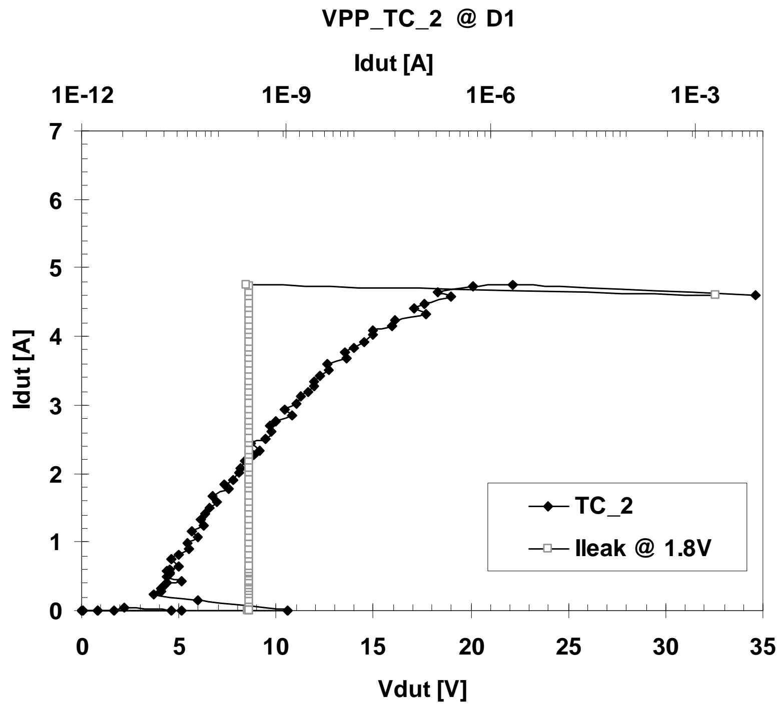


FIG. 5.72 DC measure for VPP_TC

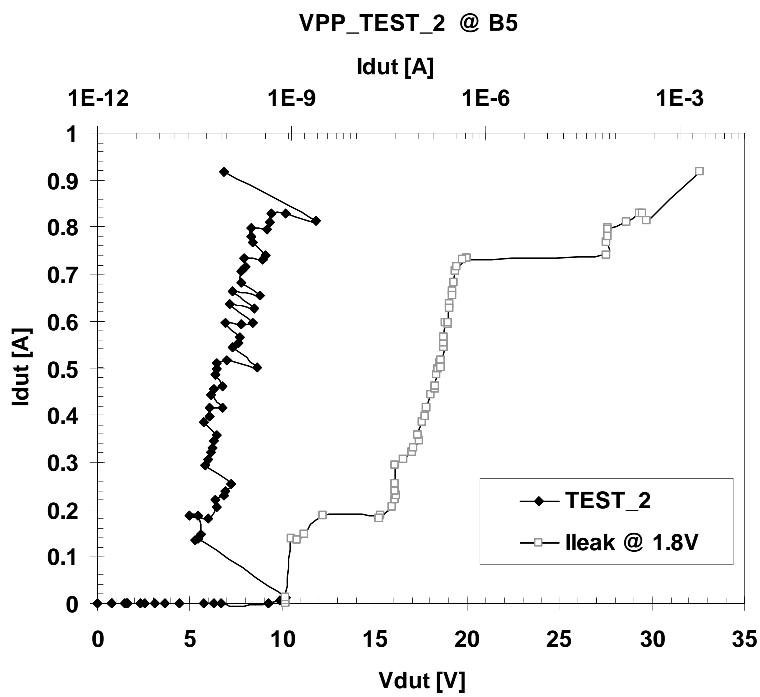


FIG. 5.73 DC measure for VPP_TEST

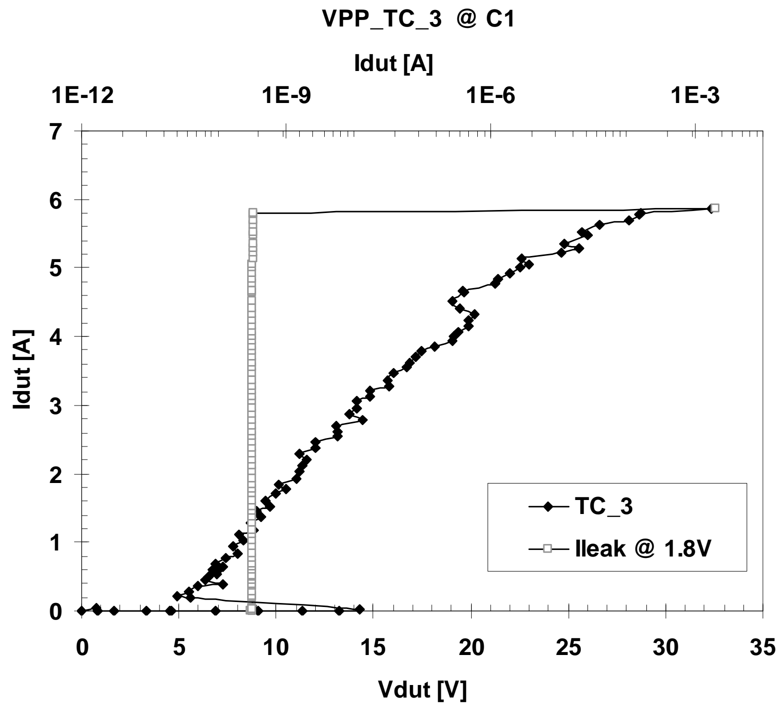


FIG. 5.74 DC measure for VPP_TC

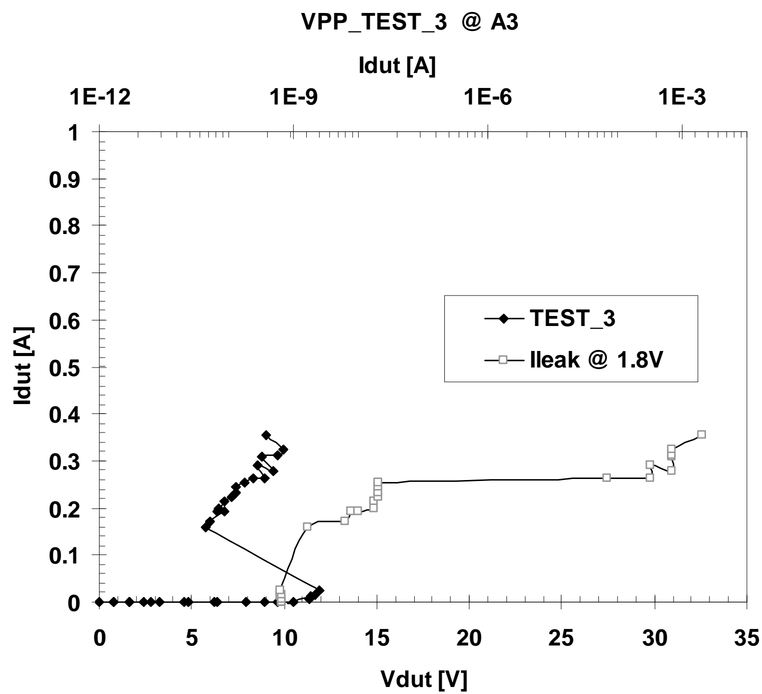


FIG. 5.75 DC measure for VPP_TEST

5.4 DIODES_RF

We have then characterized DIODES_RF devices. The position of tested structures in the die is shown in the next figure.

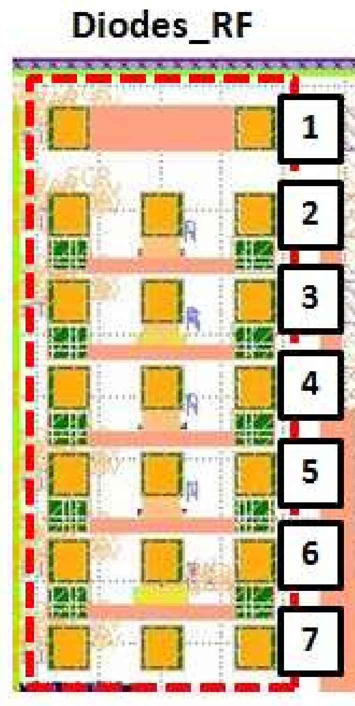
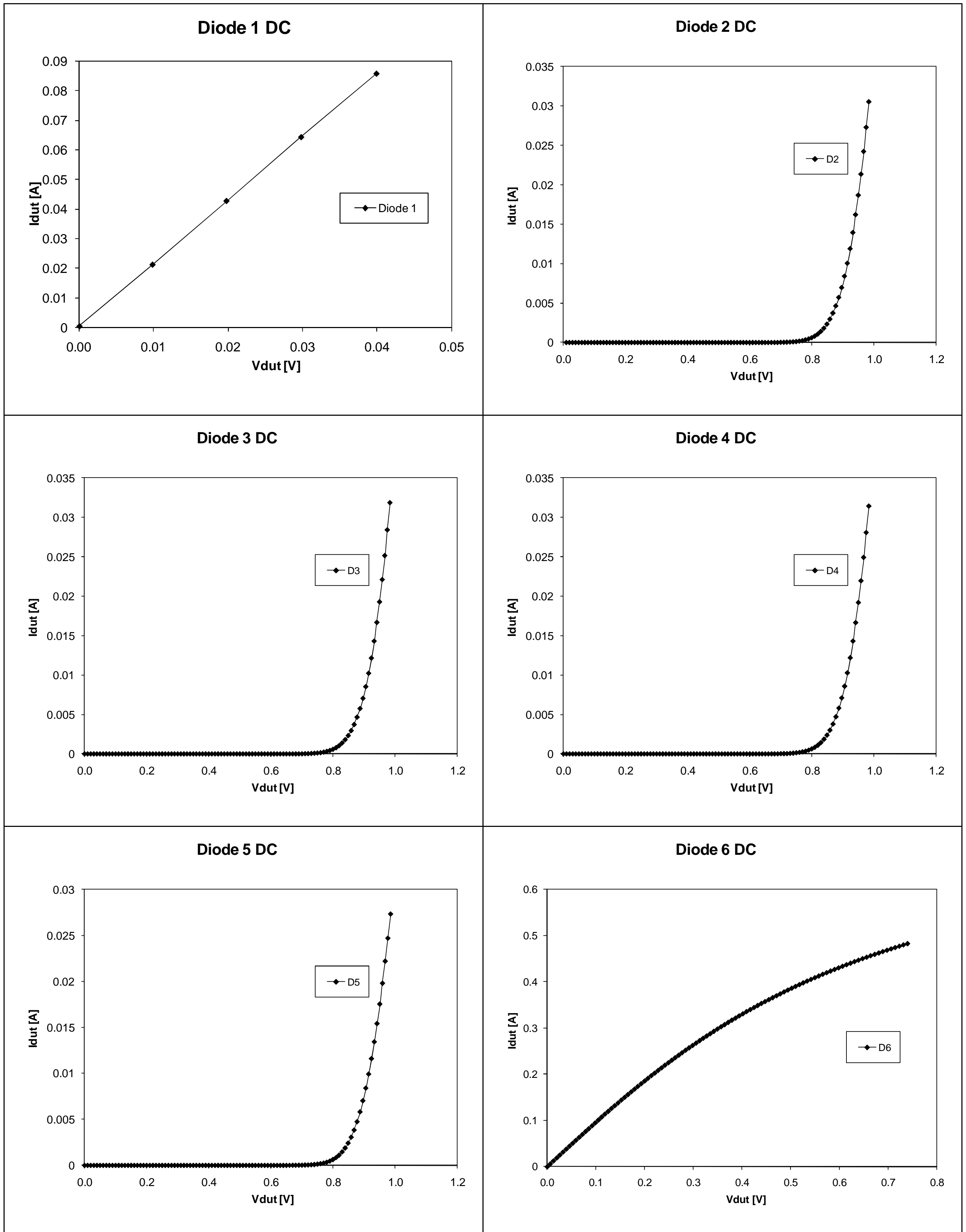


FIG. 5.76 Numeration adopted to identify pins for measures of diodes_RF

Diodes_RF devices have been characterized using rf-tips (150 um pitch) in a rf probe station. All measurements have been corrected subtracting the parasitic resistance coming from cables, tips, and contact points, using a calibration substrate typically used for the calibration of a Vector Network Analyzer (the short circuit structure). Measurements were then carried out using a Keithley 2612 Source Meter, both in DC and pulsed regime. As expected from the layout, structure n. 1 acts as a short circuit, and n. 7 as an open one.

The graphs of the I-V curves measured in DC regime are here reported.



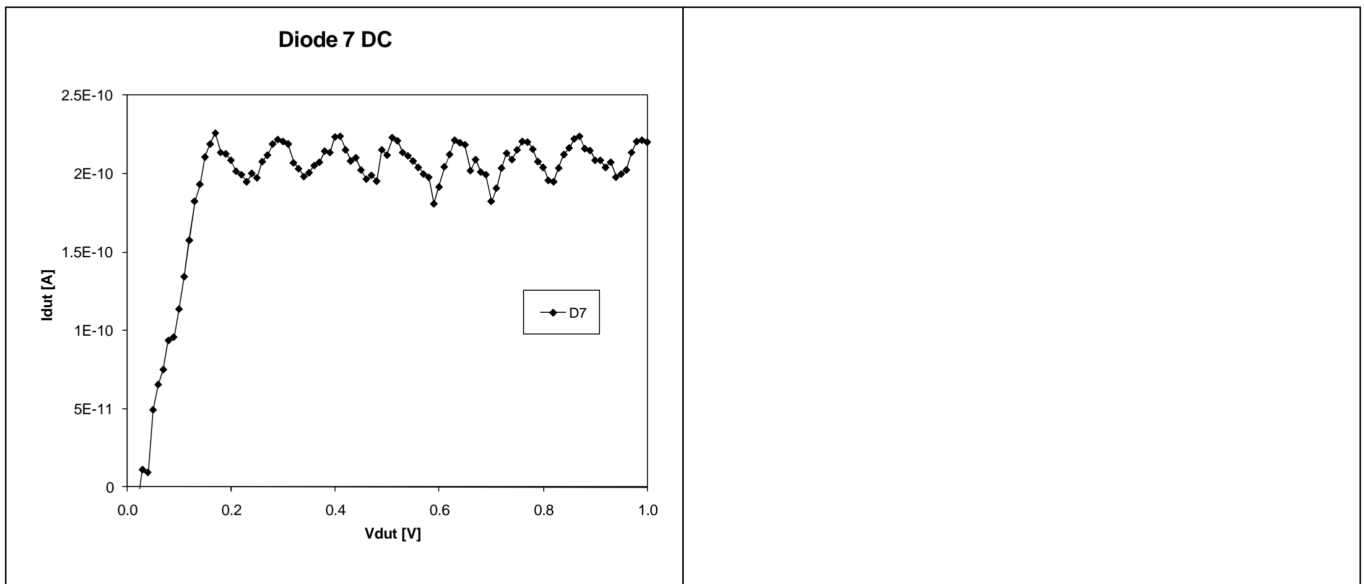
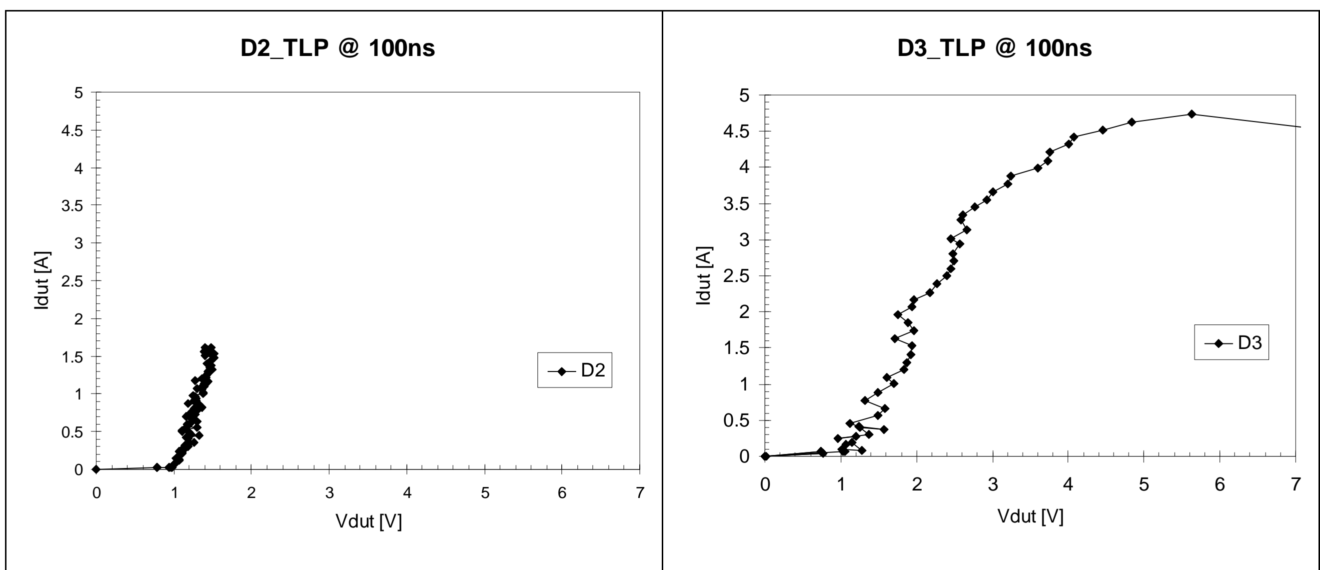


FIG. 5.77 DC measures for diodes_RF

We have then tried to characterize such devices with the 100 ns TLP system. Because of the inverse polarity of the layout of devices under test, we needed to generate negative pulses with the TLP setup (negative pulse applied to the central pad, with respect of the ground pads at left and right). Unfortunately, the inversion of the TLP pulse generated unwanted reflection on the line, probably caused by the ac current transformer. Because of that, we were not able to characterize under 100 ns TLP regime all the devices. Preliminary I-V curves in TLP regime are shown in the following figures.



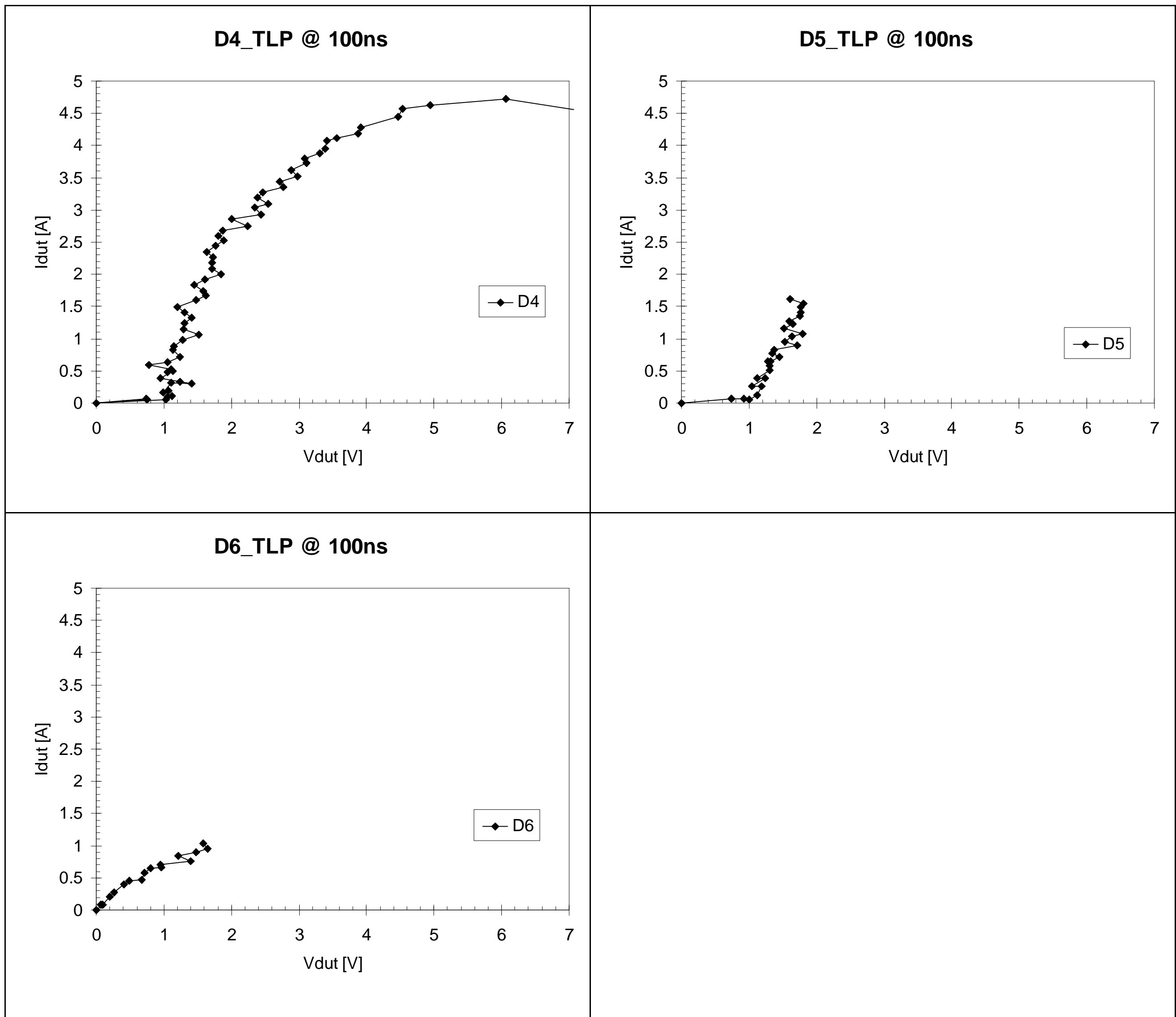


FIG. 5.78 Measures for diodes_RF under 100ns TLP regime

The following table reports the electrical parameters extracted from previous TLP measurements.

DIODES_RF_TLP	I_{fail} (A)	V_{fail} (V)	Res. DC (Ω)	Res. TLP (Ω)
D_2	---	---	2.95	0.55
D_3	-4.73	- 5.62	2.75	0.53
D_4	- 4.71	- 6.07	2.84	0.55
D_5	---	---	3.66	0.86
D_6	---	---	1.05	1.01

By the way, we used the pulsing capabilities of the Keithley 2612 (200 us, up to 10 A) in order to furnish a preliminary characterization of all diodes. Extracted I-V curves, together with the linear regression curve used to extract the on-resistance of the diodes, are shown in the next figures (open and short structures were not shown).

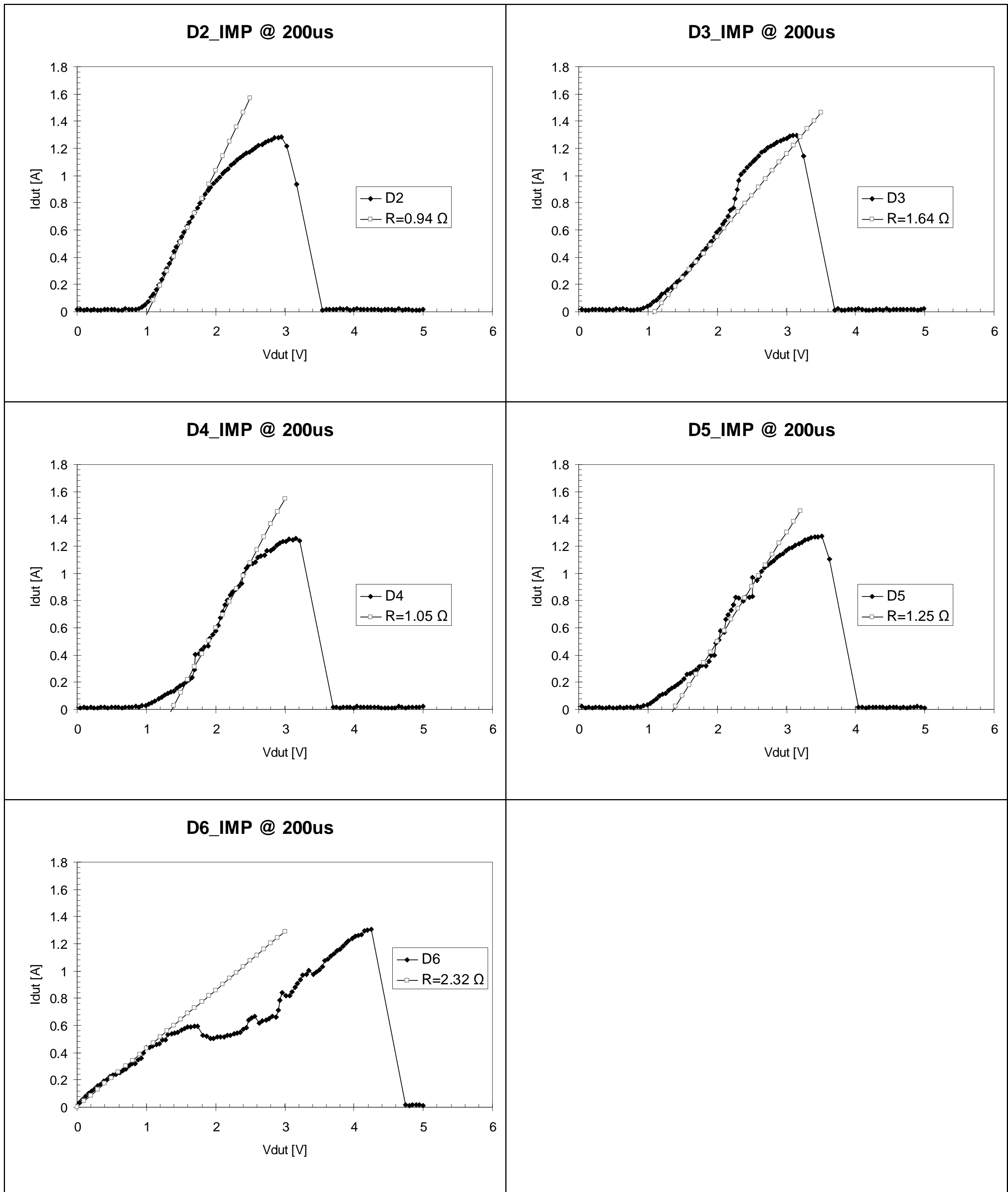


FIG. 5.79 Measures of diodes_RF with Keithley 2612

The comparison of the I-V curves shown by tested diodes under 200 us regime is reported in the next figure.

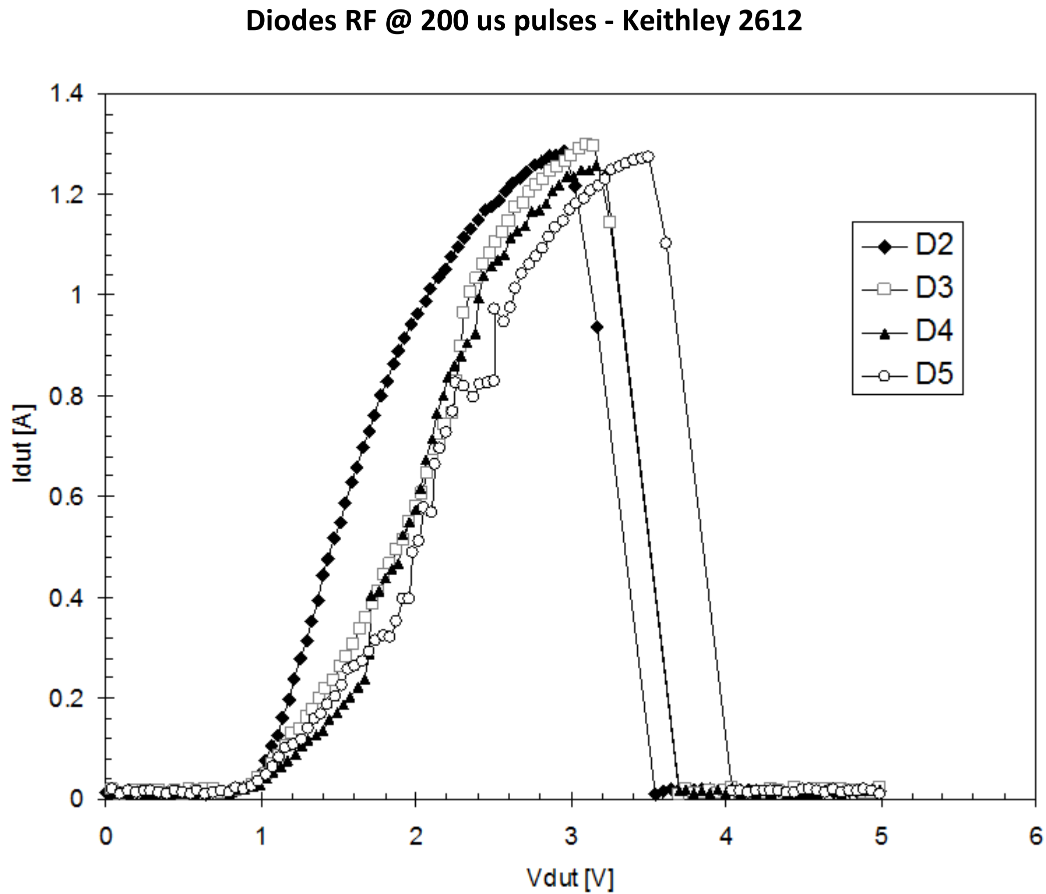


FIG. 5.80 Comparison of measures for diodes_RF with Keithley 2612

Finally, the following table reports the electrical parameters extracted from previous measurements.

DIODES_RF	I_{fail} (A)	V_{fail} (V)	Res. DC (Ω)	Res. (Ω) 200us
D_2	- 1.28	- 2.95	2.95	0.94
D_3	- 1.29	- 3.15	2.75	1.64
D_4	- 1.257	- 3.16	2.84	1.05
D_5	- 1.27	- 3.50	3.66	1.25
D_6	- 1.31	- 4.25	1.05	2.32

5.5 Main results

In conclusion we can try to sum up the fundamental results obtained in previous paragraphs. Each point is related to corresponding section number.

1. All METAL structures, as expected, present a resistance value increasing with the increase of the metal line length. It is possible to obtain this result for the resistance normalizing current values with the area, because the presence of a different number of VIAs and metal width make difficult a direct comparison of tested structures. The main electrical parameters extracted from METAL lines characterization are reported in the following table.

DUT	Pads	Area (μm²)	R□_DC (Ω *μm²)	R□_TLP (Ω *μm²)	I_{fail} (A)	V_{fail} (V)
Metal 1	1-3	1.7 E-03	8.76 E-03	1.33 E-02	1.4	27.4
Metal 1	1-5	7.89 E-03	5.83 E-02	5.81 E-02	2.7	51.9
Metal 1	1-7	1.86 E-02	1.63 E-01	1.31 E-01	3.9	72.3
Metal 1	1-9	3.37 E-02	2.27 E-01	2.46 E-01	4.7	76.8
Metal 1	1-11	5.33 E-02	6.67 E-01	4.5 E-01	5.6	85.8
Metal 3	2-4	1.7 E-03	1.79 E-03	5.2 E-03	2.7	18.6
Metal 3	2-6	7.89 E-03	1.13 E-02	2.03 E-02	5.4	38.1
Metal 3	2-8	1.86 E-02	2.97 E-02	4.78 E-02	7.9	52.4
Metal 3	2-10	3.37 E-02	5.79 E-02	9.77 E-02	9.8	63.8
Metal 3	2-12	5.33 E-02	1.27 E-01	1.46 E-01	11.8	79.0
Metal 4	13-15	1.7 E-03	1.47 E-03	2.14 E-03	5.42	11.42
Metal 4	13-17	7.89 E-03	1.57 E-02	8.24 E-03	10.37	22.86
Metal 4	13-19	1.86 E-02	2.38 E-02	1.96 E-02	15.53	38.14
Metal 4	14-16	8.37 E+03	2.1 E+04	3.01 E+04	0.76	2.89
Metal 4	14-18	1.94 E+04	8.02 E+04	1.89 E+05	0.74	7.41
Metal 4	14-20	3.04 E+04	1.41 E+05	3.38 E+05	1.06	11.77

2. MOSSWI devices failure levels are from 2.4 A (MOSSWI RC_2*W_Down), up to 10.65 A (MOSSWI_STD_Up on direct bias condition). All extracted values are reported in the next table.

MOSSWI	BIAS	I_{fail} (A)	V_{fail} (V)	$I_{leakage}$ (nA)	MOSSWI	BIAS	I_{fail} (A)	V_{fail} (V)	$I_{leakage}$ (nA)
RC_2*W_UP	DIRECT	4.49	19	8.32	STD_UP	DIRECT	10.65	10.76	16.9
RC_2*W_UP	REVERSE	2.7	12.3	6.1	STD_UP	REVERSE	3.9	6.2	6.9
RC_2*W_DWN	DIRECT	2.4	13.6	10.8	STD_DWN	DIRECT	4.9	11.1	11.9
RC_3*W_UP	DIRECT	6.96	21.15	8.44	HV_UP	DIRECT (@0.3V)	8.11	6.25	397
RC_3*W_UP	REVERSE	3.4	11.3	6.8	HV_UP	REVERSE	3.72	11.17	9.06
RC_3*W_DWN	DIRECT	4.6	11.1	10.5	HV_DWN	DIRECT	3.28	10.05	19.07
RC_4*W_UP	DIRECT	9.01	15.22	17.1					
RC_4*W_UP	REVERSE	7.4	9.6	7.3					
RC_4*W_DWN	DIRECT	5.9	9.8	9.7					

3. Vpp protection structures TC1, TC2, TC3 and TEST1 have shown a good robustness (failure level of about ~5 A) and an “hard breakdown” behavior. On the contrary, TEST 2 and TEST 3 have shown a strong degradation of the leakage curve during the TLP stress, almost after the turn-on of the protection structure. Measured values are shown in next table.

Vpp Protections	I_{fail} (A)	V_{fail} (V)	$I_{leakage}$ (nA)	Res_(Ω) TLP
TC_1	5.75	26.01	0.42	2.81
TC_2	4.75	22.11	0.29	2.36
TC_3	5.79	28.70	0.32	2.93
TEST_1	5.58	28.92	0.157	3.44
TEST_2	0.92	7.56	180.00	11.00
TEST_3	0.35	9.28	15.7	22.43

4. Diodes_RF devices have shown traditional I-V behaviors. Because of the inverse polarity of the design of such test structures, we have tried to test such devices with the negative TLP setup, but the presence of unwanted reflections limited the characterization under 100 ns TLP regime. By the way, a preliminary characterization was performed using a Keithley 2612. Extracted values are shown in next table.

DIODES_RF	I_{fail} (A)	V_{fail} (V)	Res. DC (Ω)	Res. (Ω) 200us	Res. TLP (Ω)
D_2	- 1.28	- 2.95	2.95	0.94	0.55
D_3	- 1.29	- 3.15	2.75	1.64	0.53
D_4	- 1.257	- 3.16	2.84	1.05	0.55
D_5	- 1.27	- 3.50	3.66	1.25	0.86
D_6	- 1.31	- 4.25	1.05	2.32	1.01

Conclusions

ESD events are phenomena very common in the real world and extremely dangerous for microelectronic devices. To avoid critical failures for devices introduced to the market, appropriate ESD protection structures must be developed and validated. This thesis has dealt with ESD phenomena, starting in chapter 1 from basic definitions and most common method of charging up to describe the fundamental test models used to define the sensibility of electronics devices under ESD events. In chapter 2 a brief description of the physics of the most common devices used as protection structures has been presented, pointing particular attention to the behavior of the devices under high current, short time, regimes and to novel implementations developed in the last years to increase their behavior under ESD event. Chapter 3 has dealt with the most common measurement setup used to recreate in laboratory an ESD-like event: the Transmission Line Pulser. It is based on the charging and fast discharging of the distributed capacitance of a transmission line. Most common implementations and relative issues have been presented and particular attention has been paid to the measure of leakage current and the calibration of measure system for their importance in characterization of ESD protection structures. Furthermore it has been studied the correlation of TLP with other ESD test methods, in particular the HBM and CDM models. In Chapter 4 it has been presented the LabView program realized to automate the measure process with the parameter analyzer HP 4145B, used to obtain DC measurement of protection structures studied, and a brief description of the implemented TLP used for measures under 100 ns pulsed regime, based on the Time-Domain-Reflectometer. In the last chapter it has been shown the measurements obtained in the characterization activity of protection structures and metal lines for PCM in 65 nm CMOS technology. Summarizing main results, all METAL structures, as expected, have been presented resistance and failure current values increasing with the increase of the metal line length. MOSSWI devices failure levels are from 2.4 A up to 10.65 A and a very similar behavior about failure values (current and

voltage) between pads with opposite position from the GND pad (only in case of opposite bias). Almost all the Vpp protection structures have shown a good robustness (failure level of about ~5 A) and an “hard breakdown” behavior; indeed only TEST 2 and TEST 3 structures have shown a strong degradation of the leakage curve during the TLP stress, almost after the turn-on of the protection structure. Diodes_RF devices have shown traditional I-V behaviors. Because of the inverse polarity of the design of such test structures, we have tried to test such devices with the negative TLP setup, but the presence of unwanted reflections limited the characterization under 100 ns TLP regime. By the way, a characterization has been performed using a Keithley 2612 in 200 μs pulsed regime. Measurements have been shown a similar behavior, with failure current of about –1.3 A .

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