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Design of a Phase and Amplitude Detector for a wideband phased array system in SiGe BiCMOS technology

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Abstract

Phased arrays nowadays are used in a wide variety of situations, ranging from consumer to military applications. Their diffusion is mainly due to the capability to electronically modify the radiation pattern, performing beam-steering in a much quicker way than any mechanical counterpart. On the other hand, this task can be accomplished effectively only if it is possible to rely on the accuracy of the transmit-receive modules, and due to the insufficient performances obtainable from the integrated modules, a test procedure is required, to be performed in a post-production phase. This work focuses on the task of realizing an integrated wide-band (4-12GHz) phase and amplitude detector, to be employed in the context of an on-chip test fixture with the aim of allowing quick and low-cost test set-ups, without the need for RF sockets and instrumentation. The device has the structure of a direct conversion receiver, employing two mixers in I-Q configuration, and provides the desired information through a couple of baseband outputs that can be easily sampled by an ADC. The simulation results highlight that the device can perform accurate detection, with a maximum phase error of less than 3° and a maximum amplitude error of 0.5dB.

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Chapter 1

Introduction

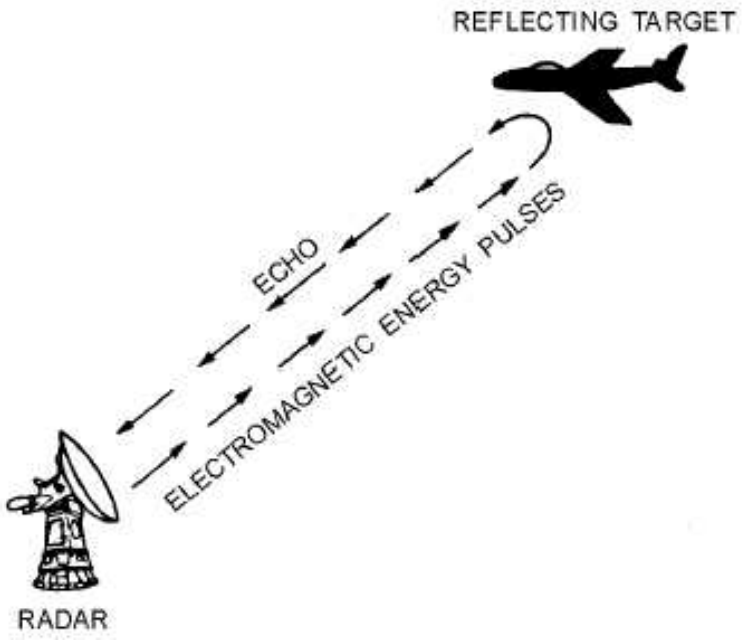
1.1 Radar systems and phased arrays

In this section it is given a brief overview on the principle of operation of a RADAR system (the denomination means *radio detection and ranging*).

Such devices have been used for decades to detect a target's position or velocity, basically through a transmitter emitting an electromagnetic signal and a receiver detecting the reflected one, as depicted in Fig.1.1. The usage of narrow-beam antennas, capable of bounding the transmitted and received power in particular directions allows to precisely detect the target's angular position, while the time taken by the wave to reach the target and come back gives the distance. These systems are used in a variety of applications, including airport surveillance, speed control, mapping and imaging and several more. Some of them employ a single antenna performing both transmission and reception, while others use separate antennas. Another distinction is based on the type of waveform emitted, mostly a train of pulses or a continuous waveform, depending on the application.

As stated, RADARs rely on very narrow-beam antennas or antenna systems to enhance performances. An antenna, indeed, never emits or receives in only one direction: a figure of merit often employed to characterize the antenna from this standpoint is the *gain*, that estimates how efficiently it emits and receives in the direction of maximum radiation. This behavior can be observed in Fig.1.2, showing a graph called *radiation diagram*, which depicts the magnitude of the electromagnetic field (that is proportional to the power density) in polar coordinates. The radiation diagram is characterized by a main radiation lobe, identifying the direction in which the antenna emits (or receives) most of the power, and several, usually unwanted, secondary lobes. The radar equation

Figure 1.1: Principle scheme



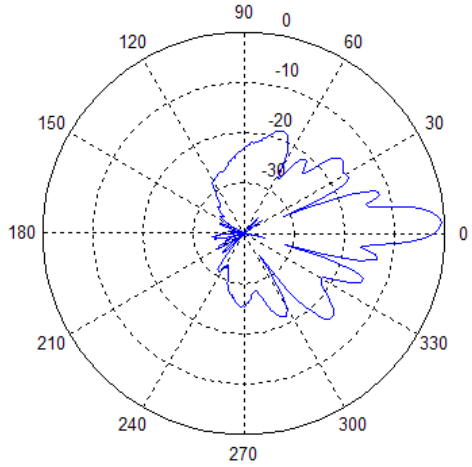
[1] gives an approximated indication on the received power, depending on the transmitted power P_t, the gain of the antenna G, the wavelength λ, the distance of the target R and the radar cross section σ[1]:

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4}$$

as can be observed, the received power falls very quickly with increasing distance, but also with increasing frequency. This equation is useful to estimate, for example the maximum range of detection, given the transmitted power, and the frequency of the transmitted signal. A narrow-beam antenna, as stated, emits only in a specific direction, hence scanning techniques, both mechanical and electronic, are employed to rotate the beam direction and perform detection in a wide space range. Mechanical rotation systems have been widely employed in the past to achieve such a result, with the obvious speed and reliability limitations. The electronic counterparts, though being known since long time ago, have been limited in their usage by the high costs or limited performance. However, the steady growth in silicon based processing technologies and the unprecedented performances are making these solutions more

[1]With *radar cross section* it is meant the ratio of the power scattered back to the incident power density.

Figure 1.2: An example of radiation diagram



and more attractive even for commercial, low-cost applications. Nowadays, electronically-scanned radar systems are capable of fine manipulation of the beam shape and direction, much more quickly than the mechanical solutions, allowing to locate and track multiple targets simultaneously.

A **phased array** is a group of antennas disposed at specific distances between each other, and fed by signals with particular phase shifts, in order to increase the equivalent gain and to scan quickly in azimuth or elevation, taking advantage of constructive and destructive interference. In order to understand the principle of operation, let's consider a set of equally spaced antennas fed through currents equal in magnitude, but with a constant phase shift between each other. Under these assumptions, the total electric field produced in a specific point Q, neglecting all coupling effects (an hypothesis usually reasonable), results to be the sum of the contributions from all the antennas:

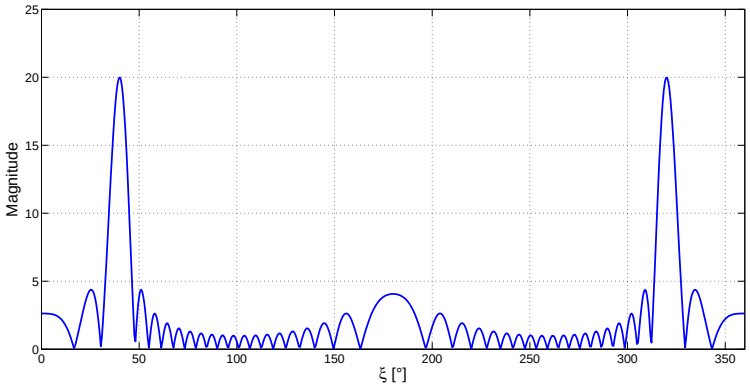
$$\vec{E}_{array}(Q) = \sum_{i=1}^{n} \vec{E}_i(Q) = M \cdot \vec{E}_0(Q)$$

where M is called *complex composition factor*, and $\vec{E}_0$ is the field produced by the antenna located at the reference point. It can be shown [2] that the magnitude of the composition factor results:

$$|M| = \frac{sin(n \cdot f(\xi))}{sin(f(\xi))} \tag{1.1}$$

ξ being the angle with respect to a reference direction. Such a function has a maximum value equal to n, and exhibits zeroes for $n \cdot f(\xi) = k\pi$, $k \neq 0$. Expression (1.1) is plotted in Fig.1.3 for an array composed by $n = 20$ antennas, designed to provide two main radiation lobes at $\xi = \pm 40°$. This clarifies that the effect of interference can be exploited to **add null directions** to the radiation diagram of the single antenna, thus controlling the number and width of the radiation lobes, as well as the radiated power.

Figure 1.3: Magnitude of the composition factor for a linear phased array

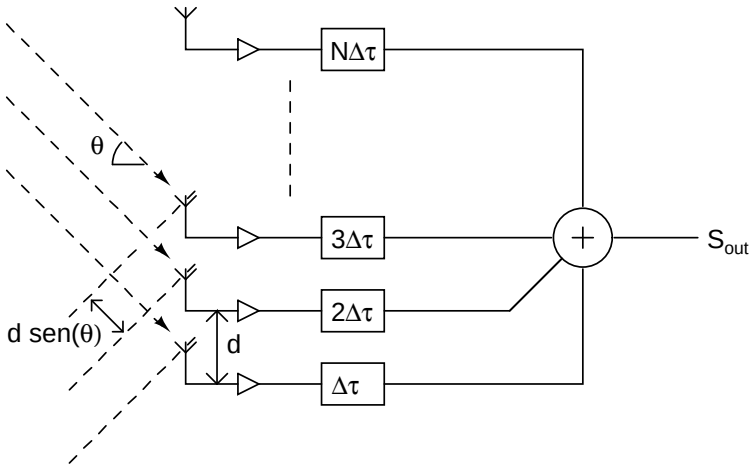


The number of antennas and their spacing allows to control the width of the main radiation lobes, and the maximum radiated power, while by modulating the phase shifts between the signals feeding the antennas it is possible to control the directions of the main lobes and perform electronic beam steering. Another degree of freedom can be obtained modulating also the magnitudes of the supply currents, which allows to get even more complex radiation patterns.

In the literature on phased array there exist a slightly different approach for these issues that allows to understand in a more intuitive way how the circuits have to drive each antenna of the array. Referring to Fig.1.4, which depicts an array receiving a plane wave, it is observed that the incident wave experiences a delay $\frac{d}{sin\theta c}$ in reaching successive antennas (d being the spacing between the antennas), therefore, to properly reconstruct the signal at the output, the processing blocks must compensate for such delays. The signal obtained by summing all the outputs exhibits a gain that is called *array factor*, and contains the same information as the composition factor magnitude defined earlier [3].

Each antenna is therefore supplied by a block containing at least a programmable gain amplifier (PGA) and a programmable delay line, which perform the desired amplification and phase shifting on the incoming or outgoing

Figure 1.4: Principle of operation of a phased array



signal. This block is usually referred to as a transmit-receive module (TRM). Phase shifting is a key aspect, and basically it is accomplished by two kind of devices:

1. phase shifters;

2. true time delay (TTD) phase shifters.

The former ideally provide constant phase shift over the frequency, and have been traditionally used for their simplicity. However, the constant phase shift traduces in non-constant time delay versus frequency, and this results in an unwanted change in the beam direction with different frequencies.

True time delays, on the contrary, provide constant time delay, which allows to maintain the same beam position with different frequencies, thus enabling wide band operation. A fixed TTD phase shifter can be built through a physical delay line, for example a microstrip line on circuit boards, though this solution is usually quite lossy. Other, more performing, solutions include MEMS and MMIC-based true time delays which can operate up to several tenths of GHz [4].

1.2 Built In Test Equipment

It has been clarified that the amplification and phase shifting tasks need to be performed in a very accurate way, so that the phased array operate properly. In fact, the unavoidable errors that the amplifiers and phase shifters

introduce, due to component mismatch, frequency depandance, and other non-idealities, can compromise the precision of the beam steering. For this reason, it is mandatory to provide an efficient way to test the array elements, after their production. The TRM elements are provided with digital inputs in order to set the desired amplitude and phase shift: the test purpose is to measure the deviation of the real amplitude and phase variations from the wanted behavior. It is important to point out that the quantities of interest are relative, since what strongly affects the radiation pattern is the variation of the phases and amplitudes referred to the initial condition. The impact of the mismatch among the reference amplitudes and phases for the different antennas, indeed, is a secondary concern.

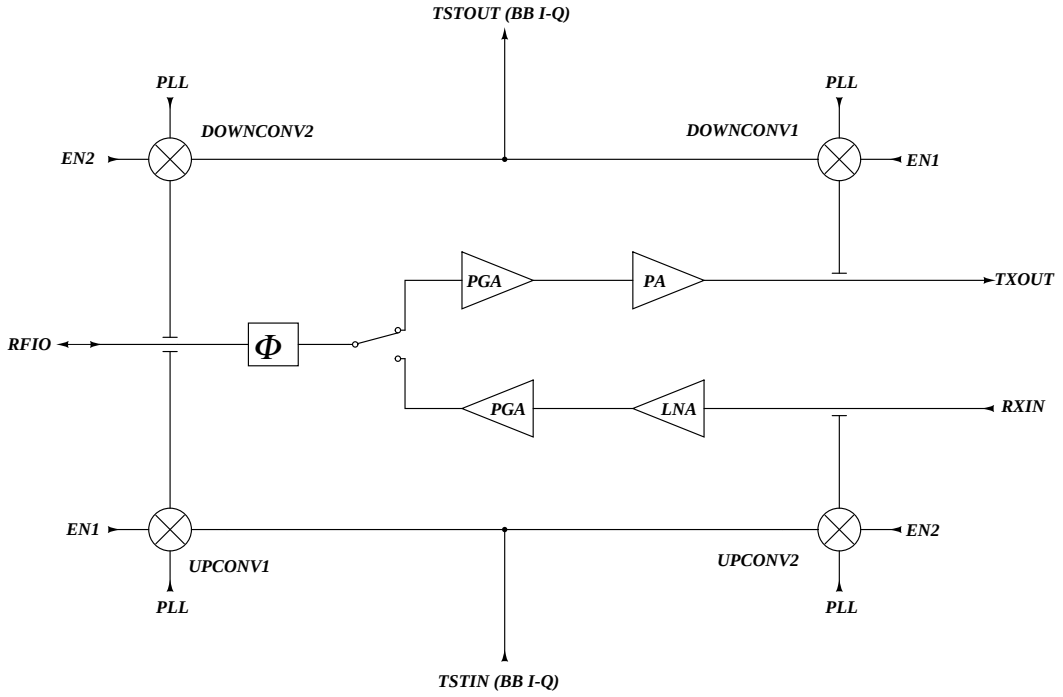
One option is the direct test at radio frequency. It has the advantage of providing the best coverage of the operating conditions and performances, but on the other hand it implies expensive RF and pick-and-place equipment, complex measurement set-ups, beside reproducibility and volume production issues.

Another solution is to provide the TRM with a so called *built in test equipment* (BITE), meaning additional circuitry capable of providing test facilities that relieve the mentioned issues, lowering the test costs, and allowing to implement simpler baseband test set-ups.

Regarding the context of this work, the principle scheme of the transmit-receive module provided with a BITE is reported in Fig.1.5, showing the system equipped with an additional test input and output at base band, where both the receiving and transmitting paths can be tested by turning on the proper devices through the enable inputs EN1 and EN2. The test signal, thus, is upconverted via the stage UPCONV1 or UPCONV2, it is processed by TRM, and then downconverted by means of DOWNCONV1 or DOWNCONV2. Being the input and output at base band, I-Q upconversion and downconversion stages are employed, as it is usual for these kind of tasks, hence there are two inputs to be processed by the upconverter, and two outputs, as well, to acquire from the downconverter. Both the stages, as it will be explained in the following chapter talking about the downconversion, need a reference signal to provide the frequency translation, that in this case comes from an integrated PLL, as highlighted in the picture. When both the enable signals are zero, of course, the BITE must not influence the operation of the module, despite being connected to it.

This work is focused on the downconversion side of the BITE. Specifically,

Figure 1.5: Principle scheme of a TRM equipped with built in test equipment.



the aim is to build a detector which provides, in the baseband I and Q outputs, the information on the amplitude and phase of the processed signal, so as to evaluate the performance of the module. Hence, the downconverter assumes the role of a vector analyzer for the RF module. Such an implementation is not unprecedented in the field of phased arrays: in [5] a similar configuration is described to provide buit-in self-test capabilities for a X-band phased array chip. In that work, the downconversion stage, particularly area-optimized, is realized using CMOS passive mixers whose outputs are amplified through an OpAmp stage.

1.3 Target specs

The quantities of interest in this work (amplitude and phase) are relative: this means that both the phase shift and the amplitude will be measured with respect to a reference.

The specifications for the object of this work are listed as follows:

- input frequency range: 4-12GHz;
- maximum standard deviation of the phase measurement error: $\sigma_{ph} = 1°$;

- maximum amplitude error: 0.5dB;
- input dynamic range: 20dB;
- operating temperatures: $0\,°\mathrm{C} - 85\,°\mathrm{C}$ (should be anyway functional in the range $-40\,°\mathrm{C} - 135\,°\mathrm{C}$);
- operating supply voltage: $3.3V \pm 5\%$.
- technology b11hfc SiGe BiCMOS 130nm.

The detector will be integrated in a test-chip to verify its performances. For this reason further specifications need to be met:

- inputs and outputs are differential;
- the RF inputs are fed by transmission lines with 100Ω (differential) characteristic impedance;
- the input RF blocks have to provide impedance matching.

Additionally, it is desirable to minimize the area occupation of the detector, thus the usage of inductors is to be avoided. Since the test equipment is not designed to operate continuously, power consumption is not an issue.

1.4 SiGe BiCMOS technology

As stated, the circuit has to be realized using the b11hfc SiGe BiCMOS technology of Infineon. BiCMOS technologies exploit the fact that low-voltage, high-speed bipolars can be isolated in the same way used for CMOS devices, allowing the fabrication of high-density chips provided with both the transistor types. This is a very attractive solution because it combines the possibility to integrate on the same die both low-power digital CMOS circuits and high-performance analog circuits, at the price of a more expensive fabrication process.

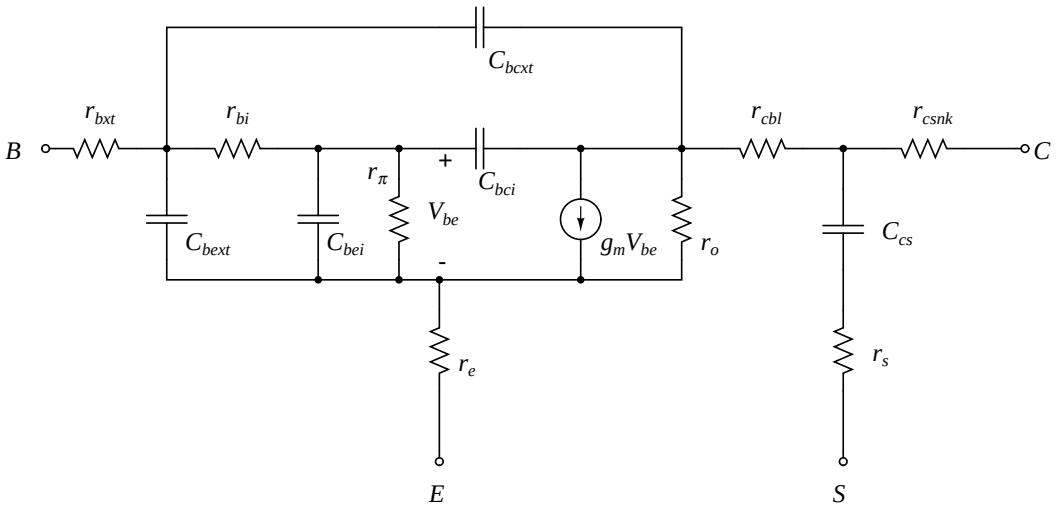
Since, for analog applications, bipolar transistors have very useful features, like high gain and low parasitic effects, they have been extensively employed in the described circuits. To use effectively these devices it is necessary to understand properly how they work. The DC characteristics of a bipolar operating in the active region are described by the equation

$$I_c = A_e J_s \left(e^{\frac{V_{be}}{nV_T}} - 1 \right) \left(1 + \frac{V_{ce}}{V_A} \right)$$

where A_e is the emitter area, J_s the collector saturation current, V_A the Early voltage. Note that this equation does not model the breakdown that occurs for high V_ce, and simulators, as well, do not take it into account. Therefore the device should be operated far from that condition, also to count on the reliability of the simulation results. The frequency response of a bipolar transistor is described by the small signal equivalent model shown in Fig.1.6, where both extrinsic and intrinsic parameters are highlighted. The most important parameters, from a RF standpoint, are:

- the transconductance $g_m = \frac{I_c}{nV_T}$, where n is a factor accounting for the intrinsic degeneration effect given by the emitter parasitic resistance r_e;
- the base-emitter capacitance, which is composed by a diffusion term $C_{be,diff} = g_m\tau_F$, proportional to the transconductance and usually dominant, and a junction term, related to the geometry of the transistor layout;
- the base-collector capacitance, also composed by an extrinsic and intrinsic component, and approximately proportional to the area below the emitter, $C_{bc} \simeq C_{jc} \cdot l_e \cdot w_e$;
- the collector-substrate junction capacitance, also related to the size of the transistors.

Figure 1.6: Small signal equivalent circuit of a bipolar transistor



A parameter often recalled to characterize the speed of such a device is the *transit frequency* f_T, that identifies the frequency at which the current gain

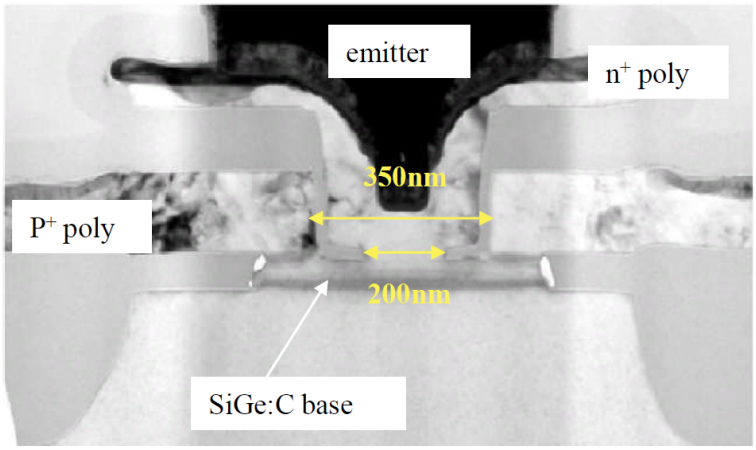
of the transistor, set in common-emitter configuration and loaded on a short-circuit, is unity. It is an indication of the high frequency capabilities of the device, which is usually operated at much lower frequencies, though this is not a strict rule. For a bipolar, it holds

$$f_T = \frac{g_m}{2\pi(C_{be} + C_{bc})}$$

highlighting how both the bias current and the capacitive parasitics influence this parameter.

In particular, the technology utilized in this work provides *heterojunction* bipolar transistors (HBTs), that are characterized by the use of different materials to build the base-emitter junction, specifically silicon (Si) and germanium (Ge).

Figure 1.7: Photograph of a HBT cross section [6]



In standard bipolar processes, the emitter doping is kept high with respect to the base, to achieve an emitter injection efficiency close to unity. High emitter doping, on the other hand, might lead to high base-emitter capacitance, thus to provide high f_T with unity efficiency it is necessary to lightly dope the base. In turn, low base doping means high base resistance r_b, that also limits the high frequency performance, because it cause a time constant with the input capacitance. This effect is amplified by the fact that, to boost f_T, it is necessary to make the base thinner to reduce the minority carriers transition time τ_F. Therefore it is apparent the existence of a tradeoff between the need for a high f_T, on one side, and a low r_b on the other, both limiting the device speed. The usage of a compound of silicon and germanium in the base of

a bipolar transistor overcomes this problem, because it lowers the band gap there, increasing the potential barrier that the holes face to be injected back to the emitter, thus relaxing the requirement for an emitter doping much higher than the base. In particular, a graded Ge base doping gives the following advantages over a standard bipolar homojunction transistor:

- it allows to significantly increase the base doping to reduce r_b;
- the possibility to reduce r_b in this way permits to reduce the base width to increase f_T;
- it allows to enhance β;
- it increases the Early voltage.

The HBTs in b11hfc are available in high-speed, medium-speed and high-voltage versions, that provide increasing operating voltage (the limit is usually specified referring to the collector-emitter breakdown voltage) but decreasing device speed. Regarding the circuits on which this work focuses, only high-speed devices have been employed, because the supply voltage allows to operate them with a V_{ce} safely below the breakdown limit. MOSFETs are available in two versions, featuring a different oxide thickness, and therefore different operating voltage limits. In the circuits where FETs have been employed like switches, the version with thinner oxide have been chosen, in order to enhance the conductance, taking care of the maximum voltage applied to the gate (sections 2.6.1,2.6.2). In other situations (section 3.6), MOSFETs have been used to enable or disable a circuit, driving them with gate-source voltages approaching the supply, and in such cases the FETs with thick oxide have been adopted.

The technology, additionally, offers the following components and features:

- MIM (metal-insulator-metal) capacitors;
- polysilicon resistors;
- precision tantalum resistors;
- multiple copper levels, with different thicknesses, current capacities, and parasitics, plus a top aluminum level.

1.5 Figures of merit

In analog circuits the performances of the various block are summarized by parameters called figures of merit, providing numerical indications that allow to understand the capabilities of the circuit, and to compare it with other potential solutions.

Each of these quantities evaluates a specific aspect of interest, such as:

- gain;
- linearity;
- relative amplitude and phase errors;
- noise figure;
- S-parameters;
- stability coefficients.

Therefore, the relevant parameters are described in the following.

1.5.1 Gain

The gain of a circuit, in the RF field, is usually defined as the output to input power ratio, since usually the ports are matched, and there is a well defined impedance to which the power is referred.

$$G_P = \frac{P_{out}}{P_{in}}.$$

In dB, the expression above becomes

$$G_{P,dB} = 10log_{10}\Big(\frac{P_{out}}{P_{in}}\Big) = 10log_{10}\Big(\frac{\frac{V_{in}^2}{2Z_{in}}}{\frac{V_{out}^2}{2Z_{out}}}\Big)$$

and, if $Z_{in} = Z_{out}$,

$$G_{P,dB} = 10log_{10}\Big(\frac{V_{out}^2}{V_{in}^2}\Big) = 20log_{10}\frac{V_{out}}{V_{in}} = G_{V,dB}$$

which is the voltage gain, in dB. However, in this work the circuits do not exhibit impedance matching at all the ports, since, for example, the output ports will carry the wanted information at DC. For this reason, the gain of

the involved circuits is more suitable to be expressed as a voltage gain, in a linear scale or in dBV. On the other hand, at the RF interfaces, that will all be matched to a characteristic impedance of 100Ω, the signal power will be considered, and expressed in dBm:

$$S_{P,dBm} = 10log_{10}\Big(\frac{V_{s,V}^2}{2Z}\Big) + 30 = S_{P,dBW} + 30$$

1.5.2 Linearity

One desirable property in an analog block is usually that it responds linearly over the whole input power range. This does not happen in practice due to the nonlinear behavior of the circuit or its different response over the frequency, whose effect on the signal is a modification of its time-domain waveform. This phenomenon is often more easily detectable looking at the spectrums, that, in the presence of distortion, highlight a modification of the relative amplitude of the signal harmonics, or even the appearance of completely new harmonics.

The sources of distortion are several (see [7] for an extensive coverage of the argument):

- a non-constant frequency response distorts a wide-band signal, even if the circuit is linear;
- the saturation of a transistor, for example in the output stage of an amplifier, might clamp the signal, causing a sharp edge that adds several spurious harmonics to the wanted spectrum (this is sometimes referred to as *hard distortion*);
- the intrinsic nonlinear characteristic of a semiconductor device causes distortion as well (*weak distortion*).

The first two sources can be avoided by selecting for the circuit proper DC operating point and bandwidth. Weak distortion, instead, causes a bit more trouble, as it is never completely canceled, and it usually rises with increasing powers, ultimately setting an upper bound for the dynamic range. The origin of the problem can be understood by calculating the Taylor series expansion of the input-output relationship around the operating point. Denoting with $x(t)$ and $y(t)$ the input and output signals, the result is

$$y(t) = a_0 + a_1x(t) + a_2x^2(t) + \dots$$

where a_0 is the bias contribution, a_1 the small signal gain, and the others are distortion coefficients. Indeed, applying a single-tone input signal $x(t) = A \cdot cos(\omega t)$, and recalling some trigonometry,

$$y(t) = \Big(a_0 + \frac{a_2}{2}\Big) + A\Big(a_1 + \frac{3a_3}{4}A^2\Big)cos(\omega t) + \frac{a_2}{2}A^2 cos(2\omega t) + \dots \qquad (1.2)$$

showing how distortion causes an alteration in the DC component, in the gain at the wanted frequency, and spurious harmonics at frequencies multiple of the input one.

To characterize the linearity performances of an analog circuit it is customary to stimulate the circuit with two tones at different frequencies ω_1 and ω_2, because this leads to parameters more easily measurable. In this case, using the same approach as in the single-tone case leads to discover that the second-order distortion causes intermodulation harmonics at $\omega_1 \pm \omega_2$, while the third-order one at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$. The latter are usually considered more important because they occur at frequencies close to the input tones. Parameters that characterizes this phenomenon, are the second and third-order intermodulation distortions, indicated with IM_2 and IM_3, and defined as the ratio of the intermodulation harmonic amplitude to the input one[2]. Referring to the third-order IM

$$IM_3 = \frac{3}{4}\frac{a_3}{a_1}A^2.$$

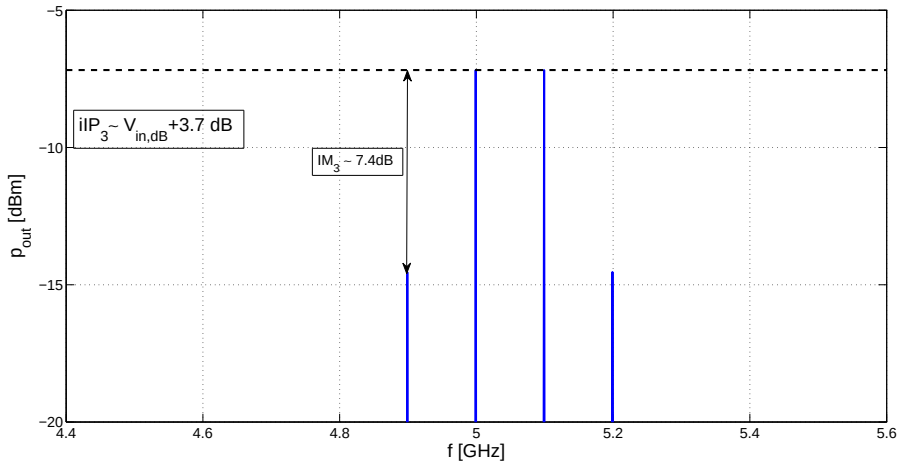
This coefficient, however, depends on the input power, and it is not clear how to handle it. A useful evaluation is given by the value of the input amplitude for which the extrapolated curves of the IM_3 components and the fundamental would coincide, that is called (input-referred) third-order intercept point IP_3. Such a coefficient is very popular because it gives a useful information on the circuit linearity (high IP_3 means that the third order distortion shows up at high input/output power) and it is easy to measure, since it holds

$$IP_{3,dB} = V_{in,dB} - \frac{1}{2}IM_{3,dB}.$$

Fig.1.8 depicts this simple evaluation in the case of input tones at $5GHz$ and $5.13GHz$ respectively: the IM_3 in this particular situation is -7.4dB, so the iIP_3 is equal, in dB, to the input voltage plus 3.4. Another parameter often employed to characterize the third-order distortion is the 1dB compression

[2]It is supposed the two input tones have the same amplitude, and it is neglected the compression effect at the frequency of the input tones, thus the measurement should be carried out with moderate input power.

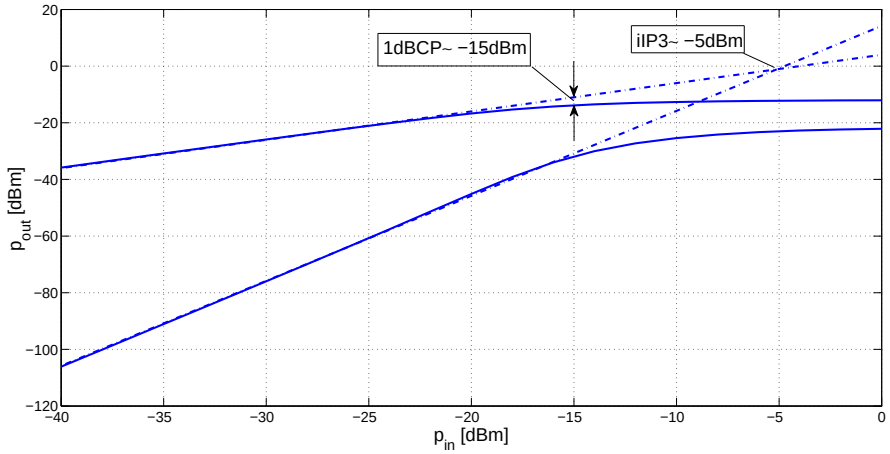
Figure 1.8: Evaluation of the input-referred IP_3



point (1dBCP), that is the value of A where the curve of the fundamental tone power is reduced of 1dB with respect to the extrapolated one, as displayed in Fig.1.9. It can be shown that $IP_{3,\mathrm{dB}}$ and $1\mathrm{dBCP}_{\mathrm{dB}}$ are linked by the following relationship

$$1dBCP_{dB} \simeq IP_{3,dB} - 9.64dB.$$

Figure 1.9: Input-referred 1 dB compression point and third order intercept



1.5.3 Relative amplitude and phase errors

The aim of the detector is to measure relative amplitudes and phases, as previously explained. A possible measurement procedure for the characterization of a TRM is therefore the following:

1. the amplitude and phase control inputs are set to the nominal, "zero" value;

2. the amplitude and phase are measured over the frequency range of interest, so as to build the references;

3. for each of the frequency points of step 2, the phase is measured with all the possible settings of the phase control input, and the procedure is repeated for each configuration of the amplitude control input. The references are subtracted to the obtained values to get the relative phases in all operating conditions;

4. the same procedure is repeated for the amplitude measurement, with the unique difference of taking the ratio of the measured amplitudes to the references.

This algorithm has to be applied to characterize the TRM of each antenna and provides a vector of relative phases and one of relative amplitudes for each operating condition.

The relative phase error, expressed in degrees, for each configuration of the control inputs and each considered frequency, is defined as the error between the real (relative) phase shift, and the one measured by the detector.

Similarly, the relative amplitude error, expressed in dB, in each condition, is defined as the error between the real (relative) amplitude, and the one measured by the detector.

1.5.4 Noise figure

Noise in electronic circuits refers to random interferences produced by the components or injected by the input-output lines, that superposes to wanted signal. A figure of merit widely employed to quantify the noise performance of a circuit is the noise figure, generally defined as follows:

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i/N_i}{S_o/N_o}$$

where S_i and S_o are the input and output signal power, while N_i and N_o are the noise power due to the source, and the total noise power at the output, including the contributions of the circuit. When mixers are involved, this issue becomes a little more complicate, because there are two input frequencies that generate the same output one, often referred to as sidebands: the frequency of the wanted signal and the image frequency. The noise figure calculation, thus, has to take into account that noise and signals belonging to both the sidebands mixes to the same output frequency [8], and for this reason different NF definitions exist to handle such situations. In this work the Single Side Band (SSB) noise figure is considered, which assumes that there is no signal at the image frequency except the source noise. Conversely, the Double-Side Band (DSB) refers to the case in which both the sidebands carry desired input signals, thus it results, normally, 3dB lower.

1.5.5 S-parameters

The scattering parameters, collected in the S-matrix, provide a complete description of a N-port network at radio frequency, relating the incident voltage waves at each port to the reflected ones.

$$\begin{pmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{pmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & S_{22} & \dots & S_{2N} \\ \vdots & \vdots & \ddots & \dots \\ \dots & \dots & \dots & S_{NN} \end{bmatrix} \cdot \begin{pmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{pmatrix}$$

where V_i^+ and V_i^- are, respectively, the amplitude of the incident and reflected wave at the i-th port. The S-parameters are calculated in the following way

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ = 0, k \neq j} .$$

In particular, thinking of a two port network, S_{11} is found to be the reflection coefficient at the input port, calculated when the output is closed on the matching impedance, that means $V_2^- = 0$.

The S-parameters are often employed, in the RF context, to define the high frequency behavior of the circuits, since they provide information on both the transmitted and reflected power on the ports. Regarding the circuit object of this work, they will be used mainly to understand if the reflection RF ports exhibit too much reflection, a condition that could be dangerous for the

interfaced devices.

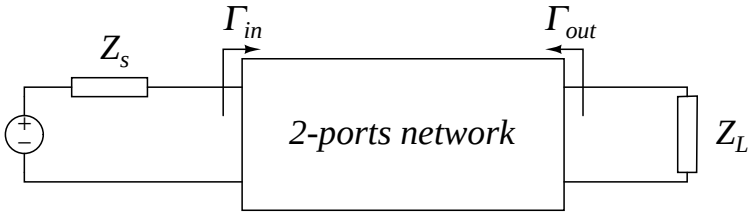
1.5.6 Stability coefficients

In the RF field the parasitic components are not negligible, so their effect has to be carefully taken into account especially at high frequencies. Consider Fig.1.10, showing a two port network with generic source and load impedances. The voltage divider applied at the input loop gives

$$V_{in} = V_S \cdot \frac{Z_{in}}{Z_S + Z_{in}} = V_S \cdot \frac{1}{1 + \frac{Z_S}{Z_{in}}}$$

where it is highlighted that the ratio $\frac{Z_S}{Z_{in}}$ assumes the role of a loop gain. If the involved impedances where passive, instability would not be possible, but Z_{in} depends on an active device, and might display a negative real part, which could potentially lead to oscillations. Note that Z_{in} and Z_{out} depend on, re-

Figure 1.10: Two port network considered for stability analysis



spectively, Z_L and Z_S, which are not clearly defined on a wide frequency range, for the mentioned reasons. Therefore, the common approach is to assure, if possible, that the impedances never show negative real part, that means guaranteeing input and output reflection coefficients whose magnitude is bounded to be less than one

$$|\Gamma_{in}| < 1 \quad , \quad |\Gamma_{out}| < 1. \tag{1.3}$$

The dependence on the source and load impedances is clarified by the following expressions

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right|$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right|.$$

If the inequalities (1.3) are satisfied for every pair of passive source and load impedances, then the circuit is said to be unconditionally stable. If they are not satisfied, the circuit is conditionally stable, meaning that, with some specific impedances, it might oscillate. Such cases can be studied on the Smith chart through the stability circles, that identify the sets of impedances for which the circuit is unstable [1]. However, in order to get a robust solution, this situation will be avoided, so the aim of the design is to have blocks which are all unconditionally stable.

The evaluation of the reflection coefficients for all the possible impedances is not practically feasible, but there exist a simple method to check the stability conditions (1.3), which makes use of a pair of coefficients easily obtained from a S-parameters analysis:

$$K(f) = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

$$b_1(f) = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

where $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$. It can be proven that the system results unconditionally stable if both of the following relations hold

$$\begin{aligned} K(f) &> 1 \\ b_1(f) &> 0. \end{aligned} \tag{1.4}$$

The former is known as *Rollet's condition* [9]. Finally, a few things need to be clearly stated:

- the previous conditions apply to the case of a two-port network. In the presence of more complex networks, stability should be checked between each pair of ports;
- the conditions (1.4) depend on frequency. Ideally, they should be checked over the whole frequency axis. Practically, the S-parameters analysis should be pushed up to the maximum frequency of oscillation of the devices of which the network is composed;
- the network needs to be stable itself, meaning that its transfer function must not exhibit poles in the right-half complex plane;
- the stability of the single circuit blocks does not imply the stability of the overall system, that needs to be checked as well, for example after the layout and the parasitics extraction.

Chapter 2

Detector structure

2.1 Overview

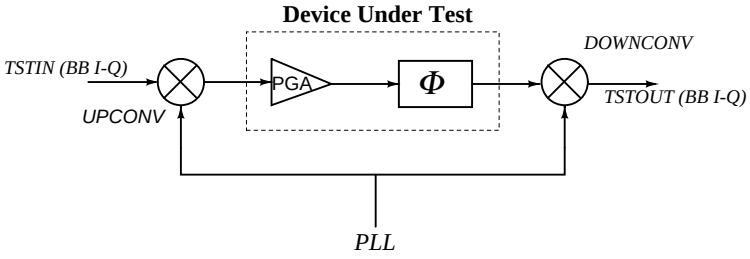
The purpose of this work is to design a system capable of measuring the amplitude and phase of the input RF signal. As explained in the previous chapter, we are interested in relative quantities, hence the phase will be measured with respect to a "zero" phase reference, while the amplitude, as well, will be measured referring to its ratio to a reference measurement. In this chapter it is given a top-level characterization of the system, and provided a description of all the blocks composing it, together with the main issues and the required performances.

2.2 Characterization of the Device Under Test (DUT)

As briefly mentioned in the introduction, each antenna of the phased array system, on the transmission side, has to be fed by a signal with proper amplitude and phase shift. When receiving, on the other hand, the different path traveled by the signal, with respect to the other elements of the array, has to be compensated through a phase shift as well, and of course the signal need to be amplified. This allows to understand that the basic block behind the antenna is always composed by the series of a programmable gain amplifier (PGA) (plus a power amplifier or a low noise amplifier, whether the transmitting or receiving path is considered) and a phase shifting element, like depicted in Fig.2.1. Both the gain and the phase shifting stages are provided with a digital control input that allow to set the desired amplitude and phase for the

processed signal in a discrete way.

Figure 2.1: Device under test



The poor tolerances that are usually available for the components in an integrated circuit, the always present mismatch issue, and the usual need for wide-band operation lead to an insufficient reliability of the gain-phase shift module. Indeed, the phase shifter, in its physical implementation, always introduce an attenuation beside the wanted phase shift, and the amplifier chain, as well, cannot provide gain without phase shifting over the whole frequency range of operation.

For these reasons, to accurately perform beam steering it is mandatory to *characterize* the DUT through a set of measurements provided by a Built In Test Equipment, that is the context in which takes place the object of this work.

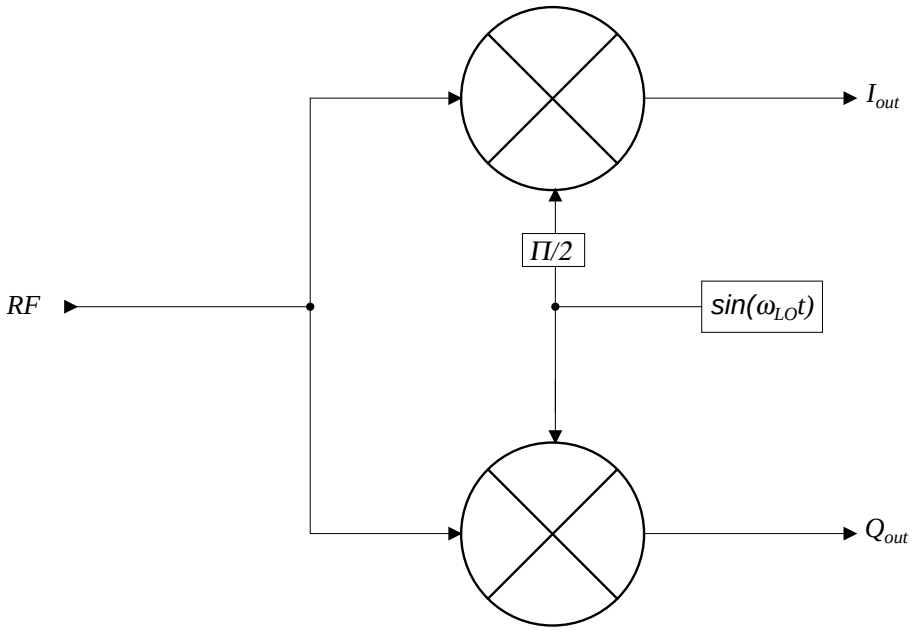
2.3 I-Q receivers

To reach the mentioned goal a RF receiver is employed. Such a device generally has the task of converting the incoming high-frequency signal to an intermediate frequency, more easily processable by the following stages (further downconversion stages, filters, amplifiers, ADCs, …). To perform the frequency conversion, it is needed a non-linear block called *mixer*, that can be modeled like a three-ports device: the RF input, the LO (local oscillator) input and the output. Basically, if the input frequencies are labeled f_{RF} and f_{LO} (with $f_{RF} > f_{LO}$), the output signal will be found at a frequency of $f_{RF} - f_{LO}$: this means that, for example, an RF signal at $10.1GHz$ mixed with an LO one at $10GHz$ will produce an output laying at $100MHz$. One common problem in this kind of circuits is that not only the frequency $f_{LO}+\Delta f$ is downconverted at Δf, but also the 'image' frequency' $f_{LO}-\Delta f$. This problem can be addressed employing image-rejection filters canceling the unwanted frequencies, which

can be very complex especially if $\frac{\Delta f}{f_{LO}}$ is very small. Receivers of this kind, employing a mixer, and one or more narrow band filters to select the desired range of frequencies are usually referred to as *etherodyne*.

A different architecture, shown in Fig.2.2, makes use of two mixers in I-Q configuration, meaning that they are fed by LO signals with a 90° phase shift between each other. This structure is often employed to achieve image rejection without any complex filter, and in direct conversion receivers [10].

Figure 2.2: Principle scheme



- Receivers belonging to the first of these two classes are used to downconvert the input signal to a finite intermediate frequency, and exploits the phases of the signals to cancel out the image frequency components, after properly shifting and summing the outputs. These kind of receivers have the advantage of needing just simple low-pass filters at the outputs of the mixers, to cancel out the unwanted frequency-sum components[11].

- Receivers belonging to the second class are instead employed because they avoids at all the problem of image components, since the conversion is performed to baseband (this structures are also called zero-IF receivers). However, other problems show up, because DC offsets and signal leakage in the mixers become sources of error that sum to the desired outputs [12].

2.3.1 Phase and amplitude detection

In this particular implementation, the presented structure is used as a direct conversion receiver to get at the outputs two DC voltages containing the desired information, which will be acquired through a pair of ADCs. This goal is achieved imposing the same frequency for the RF and LO signals, that will be drained by the same frequency reference.

Supposing the mixers perform pure multiplication with gain G, and indicating with A the amplitude of the RF signal, ϕ_{RF} and ϕ_{LO} the absolute phases of the signals, the DC component at one of the outputs results:

$$Vout = GAcos(\omega_{RF}t + \phi_{RF})cos(\omega_{LO}t + \phi_{LO}).$$

Since $\omega_{RF} = \omega_{LO}$,

$$Vout = \frac{GA}{2}cos(\phi_{RF} - \phi_{LO}) + \frac{GA}{2}cos(2\omega_{RF}t + \phi_{RF} + \phi_{LO})$$

and it is then easy to see that the DC outputs result

$$\begin{aligned} Vout_{I,DC} &= \frac{GA}{2}cos(\phi_{LO} - \phi_{RF}) = Iout \\ Vout_{Q,DC} &= \frac{GA}{2}sen(\phi_{LO} - \phi_{RF}) = Qout. \end{aligned} \tag{2.1}$$

These two components allow to reconstruct the signal amplitude and phase:

$$\sqrt{Vout_{I,DC}^2 + Vout_{Q,DC}^2} = \frac{GA}{2} = G_{mix}A \quad , \quad arctg\left(\frac{Vout_{Q,DC}}{Vout_{I,DC}}\right) = \phi_{LO} - \phi_{RF}$$

where G_{mix} is the effective voltage gain of the mixer.

2.4 Impact of non-idealities

The simple analysis conducted so far does not take into account any potential source of error that would show up depending on the particular hardware implementation. On the other hand, there are some effects that can be considered from a general standpoint, since they are common to all hardware structures:

1. since we are interested in the DC value of the outputs, any source of output offset is a potential source of error;

2. any kind of frequency divider is affected by quadrature error, due to mismatch between components and layout asymmetries;

3. the ADCs finite resolution produces a quantization error that degrades the phase and amplitude measurement.

In this section a brief analysis of the effects of these non-idealities on the measurements is carried out. These effects are particularly heavy on phase measurements, so the analysis is focused on this issue; amplitude measurement results to be more robust, and limited mainly by the compression that affects the stages with highest RF power.

2.4.1 DC offsets and quadrature error

The presence of an offset that sums to the wanted signal at the output is a particular concern, since especially with low input power it corrupts the measurement. Indicating with $V_{os,I}$ and $V_{os,Q}$ the offsets at the I and Q outputs, we get:

$$\phi_{meas} = arctg\left[\frac{sen(\phi_{RF} - \phi_{LO}) - 2V_{os,Q}/GA}{cos(\phi_{RF} - \phi_{LO}) + 2V_{os,I}/GA}\right]$$

Fig.2.3 shows a simulation result obtained setting two reasonable values for the I and Q offsets, considering mixers with $G_{mix} = 2$, and an RF input power of -20dBm, since this has resulted being the minimum managable power in most of the practical circuits: as can be observed, the error does not show any particular periodicity versus the input phase. Offset is mainly due to mismatch and process variations affecting structures that should be symmetrical, and to non linearities such as second order distortion, as seen in section 1.5.

If we suppose that a quadrature errore ε exists, than we might express one of the output components, let's say Qout, as a function of ε:

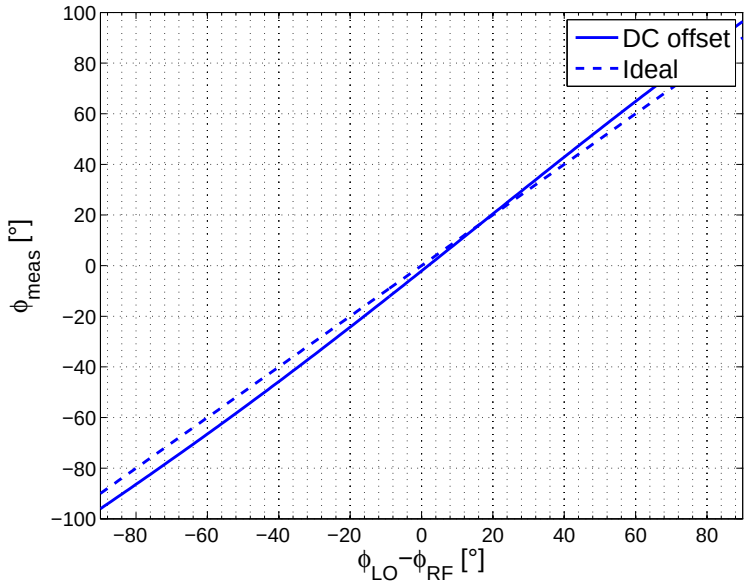
$$Qout = -\frac{GA}{2}sen(\phi_{RF} - \phi_{LO} - \varepsilon)$$

while Iout remains the same. In this situation the measured phase would become:

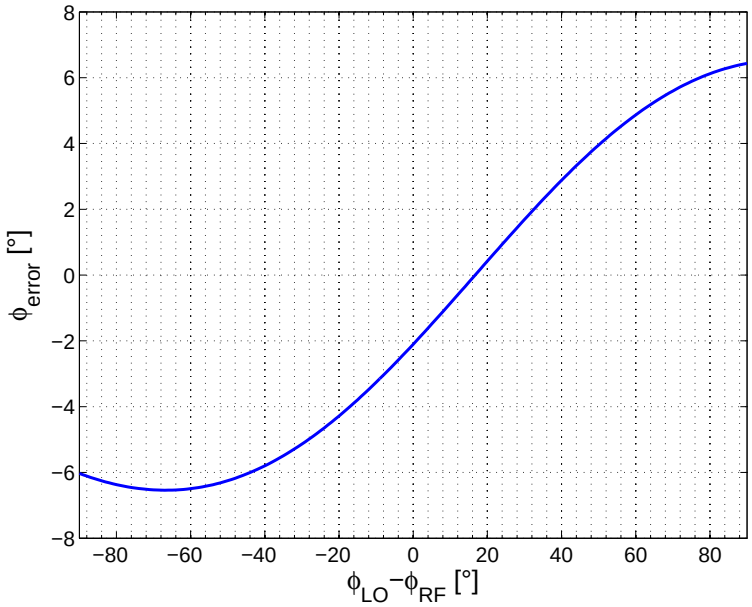
$$\phi_{meas} = arctg\Big[tg(\phi_{RF} - \phi_{LO})cos(\varepsilon) - sen(\varepsilon)\Big]$$

A plot of this function is reported in Fig.2.4 for $\varepsilon = 4°$ (setting the same G_{mix} and P_{RF} as in the simulation of Fig.2.3), showing how this results in a distortion of the phase characteristic. It should be noted that, in this case, the error is periodic with $\varepsilon = 180°$ period, and its magnitude reaches roughly the

Figure 2.3: Effect of mixer DC offsets



(a) Phase characteristics

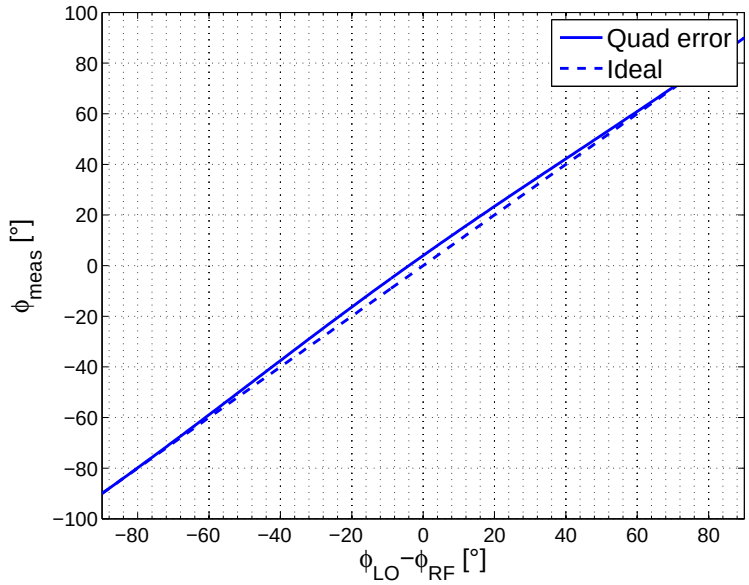


(b) Phase error

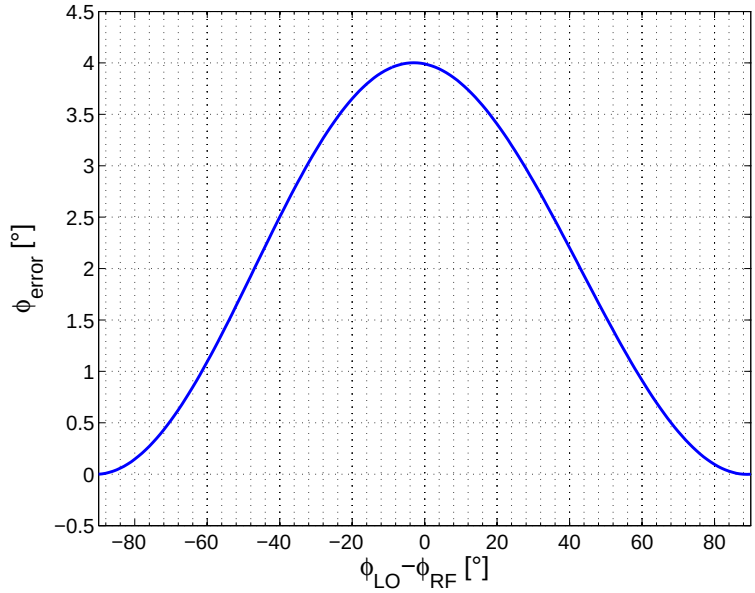
one of the quadrature error itself. This is easy to see considering the previous formula for $\phi_{RF} - \phi_{LO} = 0$: $\phi_{meas} = arctg\Big[-sen(\varepsilon)\Big] \simeq -\varepsilon$.

Let's consider, now, the effect of both these two non idealities combined together. To better understand what one should expect in this case, a statistical simulation has been carried out considering both DC offets and quadrature error to be uncorrelated random variables with normal distribution and zero mean: this is not a completely correct formulation of the problem, since, as

Figure 2.4: Effect of quadrature error



(a) Phase characteristics

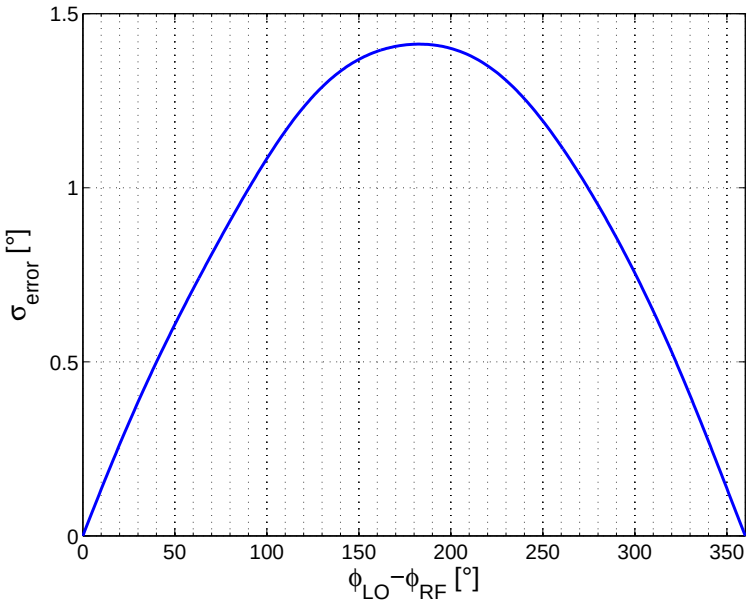


(b) Phase error

explained in the following chapters, the sources causing quadrature error are also responsible for output offset in some circuits, so it should be taken as an indication of the possible result, to be confirmed through more accurate simulations. Fig.2.5 shows the standard deviation of the overall phase error obtained in the described conditions versus the input phase. Obviously, the error drops to zero at $\Delta\phi = 0°$ and $\Delta\phi = 360°$, since we are considering a relative measurement. On the other hand, the maximum error is statistically

reached at $\Delta\phi = 180$.

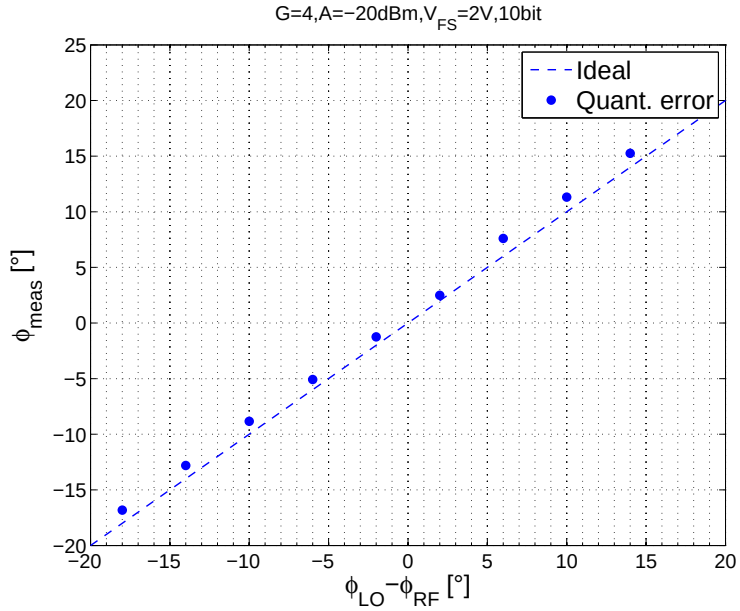
Figure 2.5: Std.dev. of the phase error with both LO quad. error and offsets



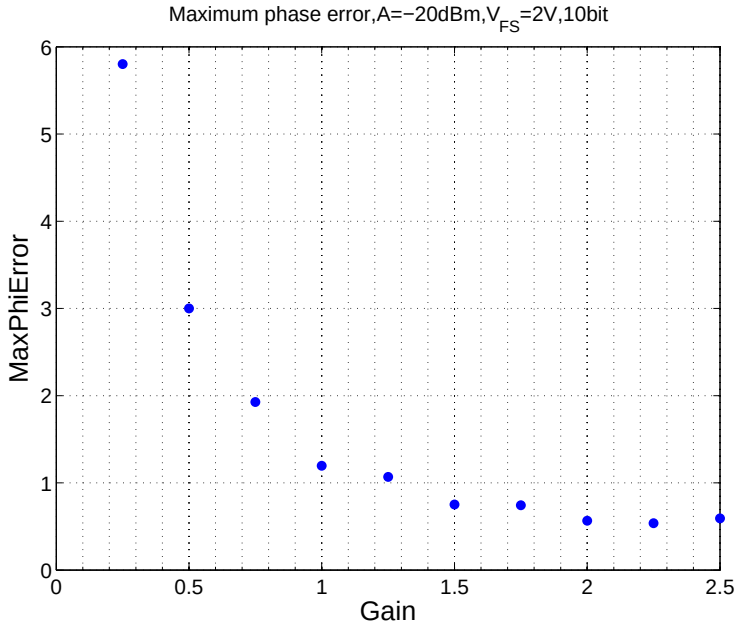
2.4.2 ADC quantization error

The DC voltages provided by the mixers are acquired through a pair of ADCs whose finite resolution contribute in degrading the performance of the detector. From this standpoint, the most critical situation in terms of phase measurement occurs when the voltage provided by the mixer is maximum, because for a wide range of input phases the same output code is kept. However, at the same time, the other mixer is providing a sine shifted by 90°, so its output is in the steepest region and the global error is somehow reduced. Basically, if we want to use an ADC with less bits, then we need more gain from the mixer, or higher RF power. Fig.2.6a shows the effect of quantization on measured phase for a 10 bits ADC with full-scale range of 2V (one of the available IP blocks), and again a mixer with $G_{mix} = 6dB$ fed by an RF signal of -20dBm, while Fig-2.6b shows the magnitude of the maximum error versus the gain of the mixers. This gives a first indication on the requirements of the mixing blocks, allowing to set a lower bound which could be of at least $G_{mix,min} = 1.5$ ($\simeq 3.5dB$), keeping a reasonable safety margin.

Figure 2.6: Effect of quantization error on phase characteristic



(a) Phase characteristics

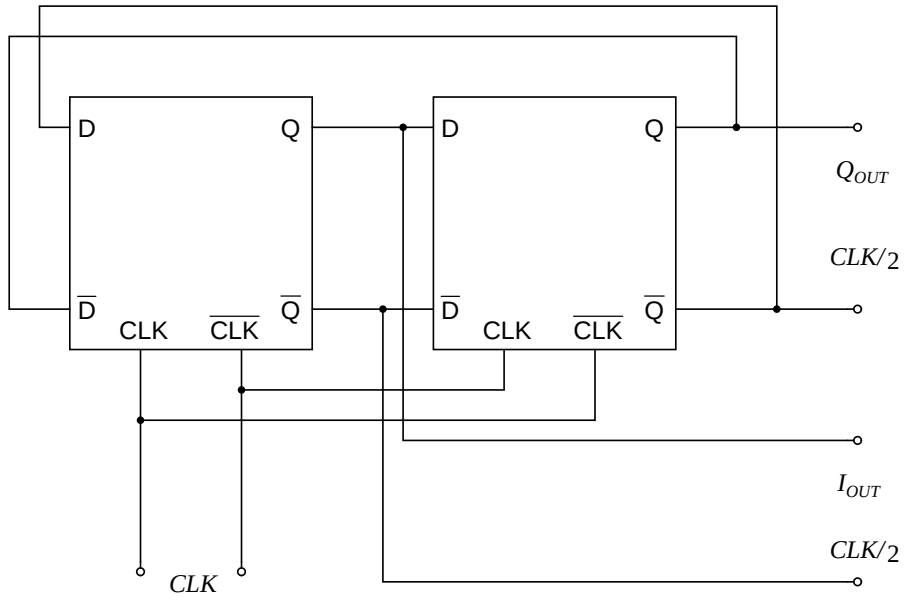


(b) Maximum phase error versus mixer gain G_{mix}

2.5 LO I-Q generation

As stated in the previous sections, this structure needs to work with two LO signals with a 90° phase shift between each other. There are different circuits performing this task: for example, a polyphase filter achieves the goal employing passive components; it is also possible to obtain the wanted signals

Figure 2.7: Principle scheme of the frequency divider

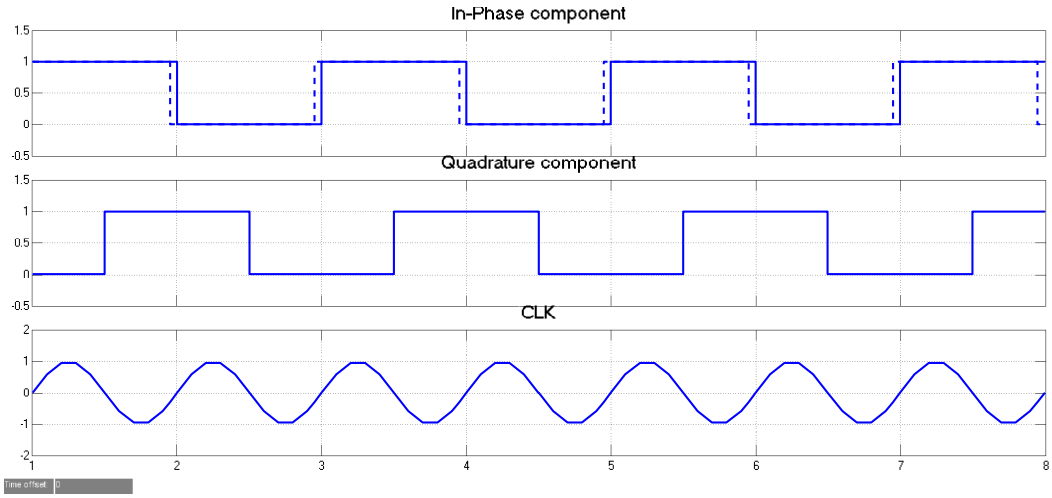


through a pair of VCOs locked to oscillate in quadrature. In this work, a different circuit has been employed, which uses two D-type flip flops connected in cascade with negative feedback, as shown in Fig.2.7: in this section the principle of operation and the issues related to this device are briefly described.

The structure implements a frequency divider halving the frequency of its input, and provides the quadrature signals at the outputs of the flip-flops. It has not been designed from scratch, but has been developed an existing solution in order to improve the performances in terms of output power and quadrature error. Fig.2.8 depicts the involved waveforms: when the clock signal is high, the second flip flop is latching its output and feeding it back, inverted, to the first one, that samples it; when the clock goes low, the same thing happens but with inverted roles, hence the second flip flop samples the output of the first, thus changing the state of its own. The result is the generation of two square waves with 90° phase shift between each other, and half the frequency with respect to the clock.

The adopted topology to realize the flip flops is the CML (*Current Mode Logic*) one. This denomination indicates a category of high-speed digital logic which operates through the commutation of currents to obtain the desired voltage signals, differently from the well-known CMOS paradigm. The main advantage in using these architectures lies in the operating frequencies they allow to reach, usually far higher than what is achievable in CMOS, while the

Figure 2.8: Waveforms provided by the divider (dashed line showing the quadrature error due to mismatch)



drawbacks with respect to CMOS are mainly:

1. the static power consumption, that makes CML circuits not suitable to the realization of low power, highly integrated systems;

2. the area occupation, since a CML logic gate usually results bigger than a CMOS one, due to the presence of resistors to convert the current signals in voltage ones, and big-sized transistors.

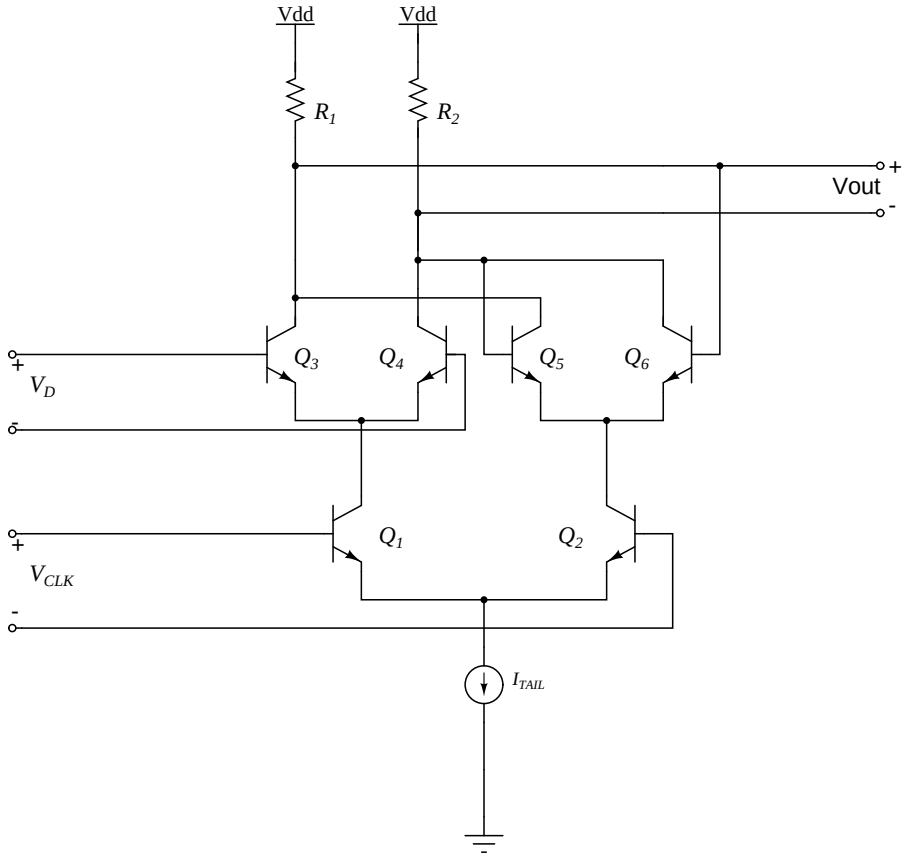
Fig.2.9 shows the schematic of a CML flip flop. Transistors Q_1 and Q_2 are responsible for the propagation of the clock signal, while Q_3-Q_4 and Q_5-Q_6 are respectively the sampling and latching pairs. To understand how the structure works, treat the transistor like ideal switches: when Q_1 is on, all the current flows through Q_3 and Q_4, so the input signal V_D propagates at the output (sampling state); when Q_1 turns off and Q_2 turns on, then I_{tail} flows entirely through the latching pair, that is already at the state previously sampled, and thus re-enforce it due to its feedback configuration (latching state).

Summarizing, the quadrature is guaranteed by the structure, while the frequency is imposed by the input. The size of the load resistors and the magnitude of the current set the output swing, thus the amplitude of the differential signal, given by:

$$\Delta V = R_L I_{tail}.$$

Then, both the value of R_L and the size of the transistors influence the band-

Figure 2.9: Simplified schematic of a CML flip flop



width of the system, which has to guarantee quick enough commutations, as explained with more detail in the next chapter. In this work it is important to optimize the quadrature error between the signals provided by the divider, so it is mandatory to understand properly which are the sources of error in this circuit and what they cause. First, recall that transistor mismatch is responsible for the arise of offset in differential pairs, which is usually modeled like a voltage generator in series with the differential input, and a current generator in shunt across the terminals. Since we consider the pairs composing the divider driven by low impedance sources, we are going to consider just the first case.

Let's suppose the divider to be perfect apart for the clock pair of one flip flop: if we insert a voltage offset generator in series with the clock input of that device, then the signal at the input of the ideal pair will be summed to a DC component and, consequently, all the commutations of that flip flop will be shifted in time by the same amount, thus leading to an error in the phase shift between the outputs (see Fig.2.8). Under these hypotesis and that (for

simplicity) of uniform base doping, the offset voltage results to be the one that must be imposed to the differential input to get a null differential current flowing through the collectors [13]:

$$V_{OS} = V_T ln\left(\frac{A_{e1}}{A_{e2}}\frac{Q_1}{Q_2}\right)$$

where the coefficients A_{ei} identify the emitter areas, and Q_i the total base doping per unit area. Setting $A_{e1} = A_e + \Delta A$, $A_{e2} = A_e - \Delta A$, $Q_1 = Q + \Delta Q$, $Q_2 = Q + \Delta Q$ to model small mismatches between these parameters, the previous relation becomes:

$$V_{OS} = V_T\left(-\frac{\Delta A_e}{A_e} - \frac{\Delta Q}{Q}\right)$$

making clear that one way to reduce the offset and thus the error is to increase the size of the transistors, without forgetting that this causes also an increase in the parasitics that must be taken into account.

Similarly, if we suppose the divider to be perfect apart for the sampling pair of one flip flop, it's easy to see that, again, the commutations will be shifted, but this time the sign of the shift will be opposite for the rising and falling edges: the result is an error in the duty cycle. The mismatch in the latching pair instead causes minor effects, since this pair is not involved commutations, but in this work it is sized the same way as the sampling pair to maintain the simmetry of the system. Finally, the mismatch in the load resistors is also a source of error, and it causes an offset in the output differential signal, leading to duty cycle errors, due to the interaction between the two flip flops, and possibly causing further errors in the mixer, if it's DC coupled.

2.6 Mixers

In section 2.3.1 it has been clarified that a key point in the down-conversion process is the frequency translation given by the multiplication of the RF and LO signals. To perform such a task it is not possible to employ linear time-invariant networks, since they can only apply a gain (or attenuation) and a phase shift to an incoming signal, without influencing its frequency. Hence, non-linear or time-variant elements are usually exploited:

- some mixers make use of the non-linear characteristic of semiconduc-

tor devices, like diodes and BJTs, that have exponential I-V relations: a strong LO voltage applied to a pn junction results in a non-linear conductance dependent on the LO itself, and a small RF perturbation applied to such a conductance leads to a current given by the multiplication of the two signals [14, pp. 556-559];

- the second cathegory of mixers exploit switches driven by the LO signal to periodically modifiy the topology of a linear network, thereby resulting in the multiplication of the RF signal by a time-variant quantity dependent on the LO.

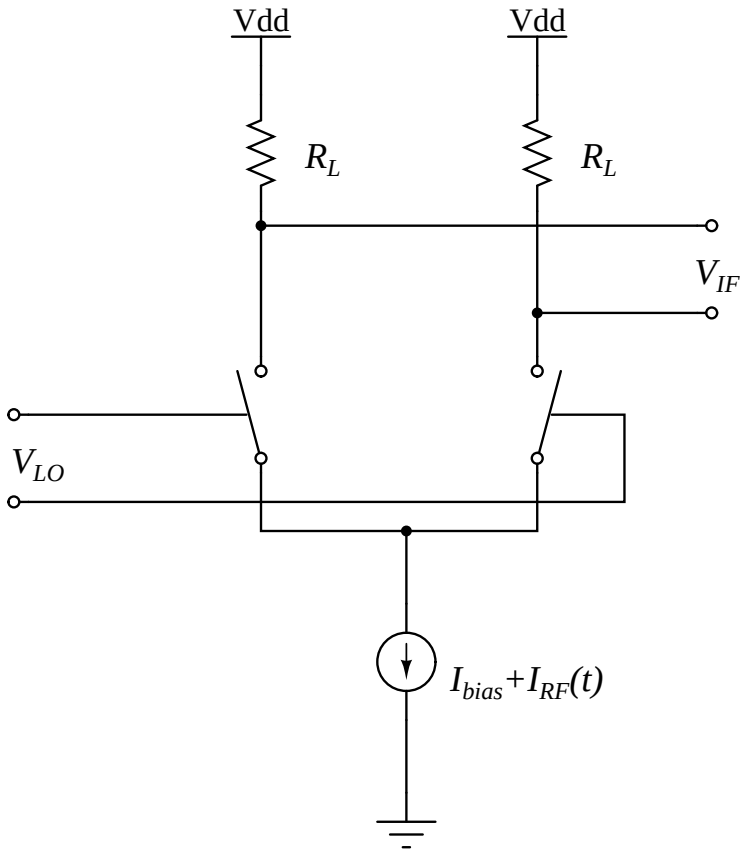
In this work, only mixers belonging to the second cathegory are considered. Mixers are often distinguished in active and passive ones depending on their capability to amplify the input signal. It should be noted that a mixer has always a gain lower than that of the equivalent linear amplifier (obtained turning off the LO signal) because of the power splitting between the sum and difference frequency components. Another fact that should be pointed out is that often mixers do not behave like ideal multipliers, although it is possible also to obtain this result [15], but produce an output signal with a much higher harmonic content, due to the strong non-linearity of the employed devices or to the sharp switching of the commutating block. This aspect is explained with more detail in the following section referring to the specific topologies.

2.6.1 Current commutating mixers

Gilbert mixers Mixers belonging to this cathegory perform the desired task by periodically modifying the topology of the circuit through a current-steering block driven by the LO signal[16]. The principle of operation is easy to understand reasoning on one of the simplest topologies of this type, the single-balanced Gilbert mixer, depicted in Fig.2.10. If we suppose the LO being a sinusoid $V_{LO}(t) = A_{LO}cos(\omega_{LO}t)$ with an amplitude sufficient to cause sharp switching, then the current drained by the tail generator is steered from one branch to the other at the LO frequency, and the output voltage results:

$$V_{out}(t) = R_L \cdot sign[cos(\omega_{LO}(t))] \cdot \Big(I_{bias} + i_{RF}(t)\Big) = R_L \cdot m(t) \cdot \Big(I_{bias} + i_{RF}(t)\Big) \tag{2.2}$$

Figure 2.10: Principle scheme of the Gilbert single balanced mixer



Since $m(t)$ is a periodic square wave, it is expressed by the Fourier series

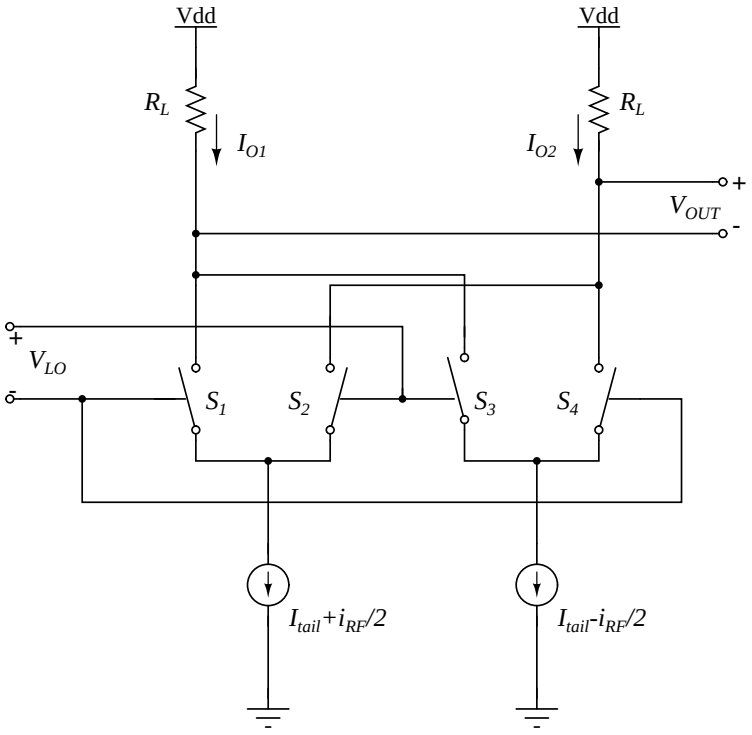
$$m(t) = \sum_{-\infty}^{+\infty} M(k)e^{-jk\omega_{LO}t} = M_0 + \sum_{0}^{+\infty} \frac{4}{(2n+1)\pi} cos\Big((2n+1)\omega_{LO}t\Big) \quad (2.3)$$

where $M_0 = 0$ in this case, since the square wave we are considering has zero mean. Comparing (2.2) and (2.3) highlights that the output spectrum is populated by several harmonics, and in particular the bias current being mixed with the LO cause all the LO harmonics to appear at the output, which may be a problem in some applications. another concern, considering the task performed by the mixer in this work, is the non-ideal isolation between the LO and RF ports, possibly causing the LO to transfer at the RF port and self-mix to DC: the isolation between the mentioned ports is guaranteed only as long as the switches are perfectly symmetrical.

The Gilbert double-balanced mixer combines two single-balanced cells exploiting the symmetry to prevent the LO components to propagate at the

output. The principle schematic is shown in Fig.2.11. In this configuration,

Figure 2.11: Principle scheme of the Gilbert double balanced mixer



when S_1 and S_4 are on the output currents result

$$I_{O1} = I_{bias} + \frac{i_{RF}}{2} \quad , \quad I_{O2} = I_{bias} - \frac{i_{RF}}{2}$$

while when S_2 and S_3 are on

$$I_{O1} = I_{bias} - \frac{i_{RF}}{2} \quad , \quad I_{O2} = I_{bias} + \frac{i_{RF}}{2}.$$

The output voltage thereby results:

$$V_{out} = R_L \cdot (I_{O1} - I_{O2}) = R_L \cdot \left(2 \cdot \frac{i_{RF}}{2} sign[cos(\omega_{LO} t)]\right) = R_L \cdot m(t) \cdot i_{RF}(t). \quad (2.4)$$

Comparing (2.2) and (2.4) allows to see that the LO harmonics no longer propagate to the output, since the term given by the bias current does not appear. Another useful property of this topology versus the single-balanced one, concerning the aims of this work, is that it has a differential input, thus not needing a differential-to-single ended conversion. The gain of both these mixers is found by substituting (2.3) in (2.4), and setting $i_{RF}(t) = G_m V_{RF} cos(\omega_{RF} t)$,

where G_m is the transconductance of the input voltage to current converter:

$$\begin{aligned} V_{out} &= G_m R_L V_{RF} cos(\omega_{RF} t) \cdot \left[M_0 + \sum_{0}^{+\infty} \frac{4}{(2n+1)\pi} cos\Big((2n+1)\omega_{LO} t\Big) \right] \\ &= G_m R_L V_{RF} \frac{2}{\pi} \left[cos\Big((\omega_{RF} - \omega_{LO})t\Big) + cos\Big((\omega_{RF} + \omega_{LO})t\Big) \right] + \dots \end{aligned} \tag{2.5}$$

thus

$$G_{mix} = \frac{2}{\pi} G_m R_L \tag{2.6}$$

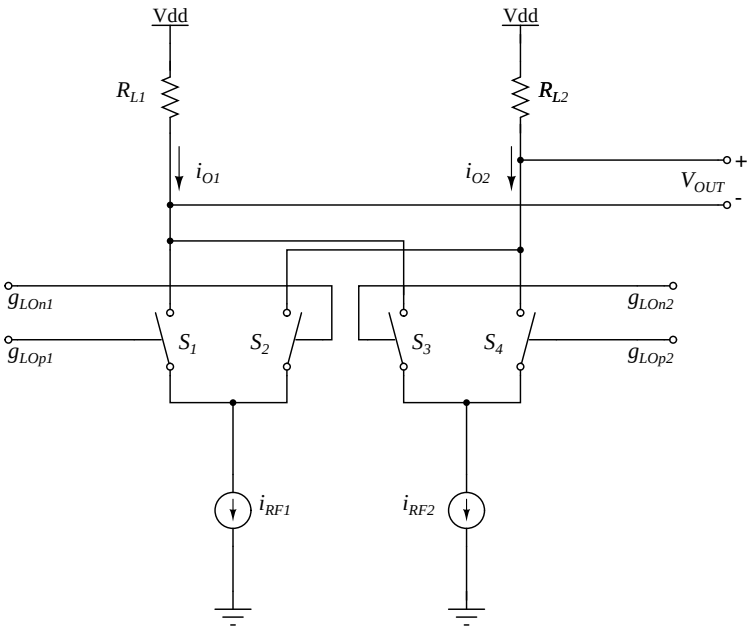
Taking into account the task performed by the mixers in this work, a particular concern is the non-ideal isolation between the LO and RF ports due to component mismatch, that may cause the LO to transfer at the RF port and self-mix to DC: the isolation between the mentioned ports is guaranteed only as long as the switches are perfectly symmetrical. It is therefore strongly important, to avoid this undesirable effect, that the adopted technology provides good matching performances. Both the single and the double-balanced Gilbert mixers can be realized employing bipolar or MOS transistors.

Output offset analysis in Gilbert double-balanced mixers In this paragraph it is provided a simplified analysis of the output offset in Gilbert double-balanced mixers, developed following the approach in [17]. The switching behavior is modeled through the functions g_{LOi} (refer to Fig.2.12), where η_i is the duty-cycle associated to each specific switch:

$$\begin{aligned} g_{LOp1/2}(t) &= \eta_{p1/2} - \frac{2}{\pi} \Big[sin(\eta_{p1/2}\pi) cos(\omega_{LO} t) \\ &\quad - \frac{1}{2} sin(2\eta_{p1/2}\pi) cos(2\omega_{LO} t) + \frac{1}{3} \dots \Big] \\ g_{LOn1/2}(t) &= \eta_{n1/2} + \frac{2}{\pi} \Big[sin((1-\eta_{p1/2})\pi) cos(\omega_{LO} t) \\ &\quad - \frac{1}{2} sin(2(1-\eta_{p1/2})\pi) cos(2\omega_{LO} t) + \frac{1}{3} \dots \Big] \end{aligned} \tag{2.7}$$

The nonlinearities due to the transconductor are also taken into account in the expressions of the single-ended currents i_{RF1} and i_{RF2}, supposing the

Figure 2.12: Scheme of the Gilbert double balanced mixer highlighting component mismatch



differential input port to be fed by a single tone $v_{RF}(t) = V_{RF}cos(\omega_{RF}t)$:

$$\begin{aligned} i_{RF1} &= g_{m1}\left[\frac{v_{RF}(t)}{2} + a_2'\Big(\frac{v_{RF}(t)}{2}\Big)^2 + a_3'\Big(\frac{v_{RF}(t)}{2}\Big)^3 + \dots\right] + I_{bias1} \\ &= I_{bias1} + \frac{a_2'}{2}g_{m1}\left(\frac{V_{RF}}{2}\right)^2 + g_{m1}\left[\frac{V_{RF}}{2} + \frac{3}{4}a_3'\left(\frac{V_{RF}}{2}\right)^3\right]cos(\omega_{RF}t) + \dots \end{aligned} \tag{2.8}$$

$$\begin{aligned} i_{RF2} &= g_{m2}\left[-\frac{v_{RF}(t)}{2} + a_2'\Big(\frac{v_{RF}(t)}{2}\Big)^2 - a_3'\Big(\frac{v_{RF}(t)}{2}\Big)^3 + \dots\right] + I_{bias2} \\ &= I_{bias2} + \frac{a_2'}{2}g_{m2}\left(\frac{V_{RF}}{2}\right)^2 - g_{m2}\left[\frac{V_{RF}}{2} + \frac{3}{4}a_3'\left(\frac{V_{RF}}{2}\right)^3\right]cos(\omega_{RF}t) + \dots \end{aligned} \tag{2.9}$$

where $g_{m1/2} = \frac{I_{bias1/2}}{nV_T}$, and a_2', a_3', …are the relative non-linear coefficients. The following expressions model the mismatches between the parameters:

$$\eta_{p1/2} = \eta_{nom} + \frac{\Delta\eta_{1/2}}{2} \quad , \quad \eta_{n1/2} = \eta_{nom} - \frac{\Delta\eta_{1/2}}{2}$$

$$R_{L1} = R_L + \frac{\Delta R_L}{2} \quad , \quad R_{L2} = R_L - \frac{\Delta R_L}{2}$$
$$I_{bias1} = I_{bias} + \frac{\Delta I_{bias}}{2} \quad , \quad I_{bias2} = I_{bias} - \frac{\Delta I_{bias}}{2}.$$

The output voltage is therefore given by

$$\begin{aligned} v_{out}(t) &= R_{L1} i_{o1}(t) - R_{L2} i_{o2}(t) \\ &= i_{RF1}(t)\Big[R_{L1} g_{LOp1}(t) - R_{L2} g_{LOn1}(t)\Big] \\ &+ i_{RF2}(t)\Big[R_{L1} g_{LOn2}(t) - R_{L2} g_{LOp2}(t)\Big] \end{aligned} \tag{2.10}$$

By plugging (2.7), (2.8) and (2.9) into (2.10) the following result is obtained for the output DC voltage:

$$\begin{aligned} V_{out,DC} &= \Big(I_{bias} + \frac{g_m a_2'}{2} V_{RF}^2\Big)\Big(R_L(\Delta\eta_1 - \Delta\eta_2) + \Delta R_L\Big) \\ &+ \frac{\Delta I_{bias}}{2}\Big(1 + \frac{a_2'}{2nV_T} V_{RF}^2\Big) R_L(\Delta\eta_1 + \Delta\eta_2) \\ &- \frac{2}{\pi} g_m R_L\Big(V_{RF} + \frac{3}{4} a_3' \frac{V_{RF}^3}{4}\Big) + g_m \frac{a_3'}{3\pi} R_L \frac{V_{RF}^3}{8} + \dots \end{aligned} \tag{2.11}$$

Looking at the previous result it is possible to note two contributions:

1. in the first line of (2.11) there appear all the contributions caused by component mismatch in the transconductor, switching cell and load resistors;

2. in the second line of (2.11) appears the gain of the stage, together with the compression coefficient a_3' due to the non-linearity of the transconductor, and all the other DC contributions caused by the harmonics from the transconductor mixing with the ones of the LO functions to DC.

Basing on what discussed in section 2.4.1, it is straightforward that component matching in the transconductor, switching cell and between the load resistors is a key aspect to guarantee accurate phase measurement. Moreover, distortion may result in DC errors as well, so especially at the highest input power it should be taken into account.

TIA loaded passive mixers Another topology belonging to the category of current-cummutating mixers is the one shown in Fig.2.13, employing again a transconductance amplifier, current-mode switches and a low-frequency TIA (transimpedance amplifier) to convert the output current back into a voltage.

TIAs are usually realized through differential amplifiers with resistive feedback, or other kinds of amplifier based on a common-base or common-gate input stage, with the purpose of keeping both a low input impedance and a proper conversion gain. These features make the signal current generated by the transconductor flow through the switches and then in the transimpedance stage, provided that its input impedance is negligible with respect to the one of the load resistors. Thereby, under the assumptions that all the signal current flows through the TIA and that the switching operation is ideal, the gain results:

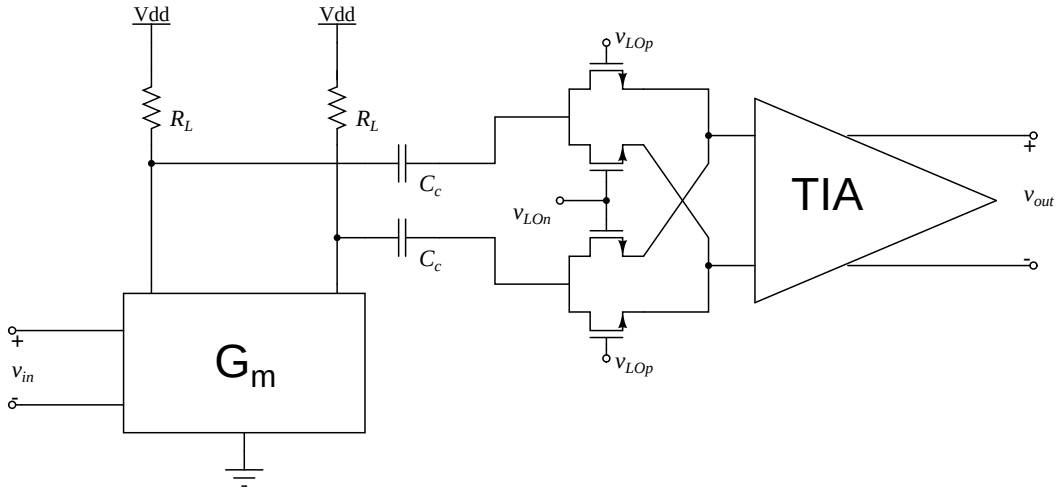
$$G_{mix,TIA} = \frac{2}{\pi} G_m R_{TIA}$$

R_{TIA} being the transimpedance of the TIA. This type of mixer has been effectively used to obtain high-linearity and low-noise performances[18]. A good feature, regarding the intended purpose, is the presence of capacitors decoupling the G_m stage and the switching cell, thus avoiding the offset from the transconductor to propagate towards the output. Note that this also imply that the switches do not dispose of a bias current, as it is in the Gilbert mixer, thus they are realized employing MOS transistors: this fact sets some bounds regarding the LO drive, which needs more swing (when compared to the bipolar Gilbert mixers) to get reliable switching, and about the input common mode of the TIA, that should be kept as low as possible. The offset in this mixer is ultimately set by the TIA stage, whose performance has to be sufficient not to compromise the accuracy of the measurement: since the wanted information lays at DC, it has to be designed in order to get the best matching between its components.

2.6.2 Passive voltage-mode mixers

Mixers discussed so far perform mixing in the current domain, making use of switches that steer the signal current between two branches in a square-wave fashion. There exist also mixers operating entirely in the voltage domain, skipping the previous V-I conversion usually performed by a transconductor. These devices are generally attractive because they can operate with very low power consumption, and are often realized in CMOS technology, since it naturally provides good switches. A very simple mixer belonging to this category is shown in Fig.2.14, and consists in a bridge built with four switches driven by the LO signal. As in the Gilbert mixer, one pair of switches at a time is turned on, while the other two are off: when M_1 and M_4 are on, $v_{out}(t) =$

Figure 2.13: Principle scheme of a mixer relying on a baseband TIA



$v_{RF}(t)$, while in the following half-period M_2 and M_3 are on, thus $v_{out}(t) = -v_{RF}(t)$. Ideally the output port sees the RF voltage multiplied by a unity-amplitude square wave, which as seen previously means the multiplication of the two signals plus several spurious harmonics. The ideal gain of this mixer, when driven by a square-wave like LO signal, is therefore:

$$G_{mix,passive} = \frac{2}{\pi}$$

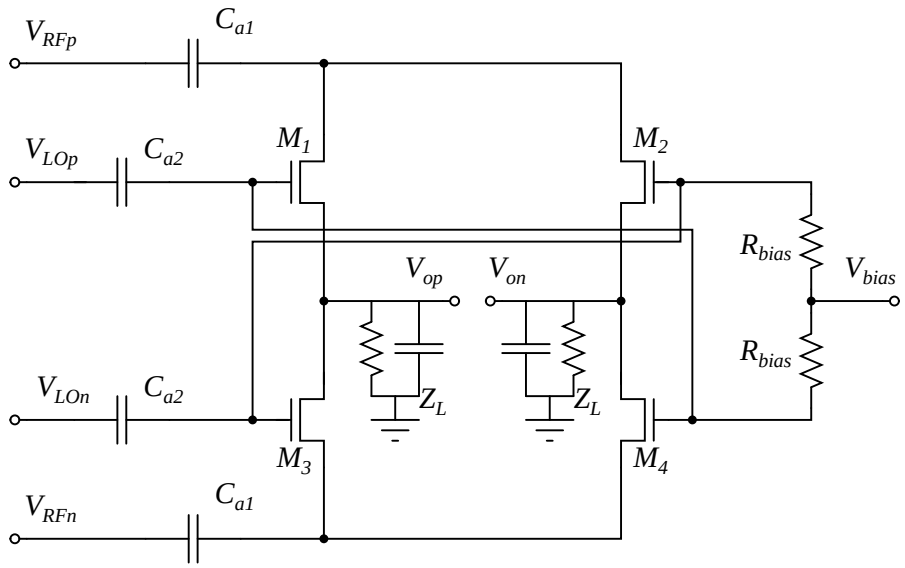
It has been demonstrated that this mixer version can theoretically achieve a unity gain when driven by a sinusoidal LO with particular properties [19]. Unfortunately, remembering the results reported in Fig.2.6, even such a conversion gain is too low, therefore an amplifier would be needed to enhance it. Moreover, as discussed when dealing with the TIA loaded mixer, a low output common mode is desirable for reliable switching operation, but at the same time such an output would be likely not suitable to feed an ADC, whose input is subjected to swing limitations. These considerations lead to the need for another stage, at least to perform the common-mode shifting, and again the offset performance would rely on this output stage. On the other hand, this topology is very interesting because it is very simple, and does not show offset sources itself, unlike the Gilbert mixer. Concerning the linearity performances, there are mainly two sources of distortion in this mixer:

1. the first source of distortion is due to the input current flowing through the non-linear conductances represented by the MOSFETs;

2. the second source of distortion is the modulation of the switching times due to the RF signal.

Both of this non-linearities can be attenuated be means of a strong gate drive, with very steep commutations, that keeps low conductances and makes negligible the effect of the RF signal.

Figure 2.14: An example of passive MOS mixer

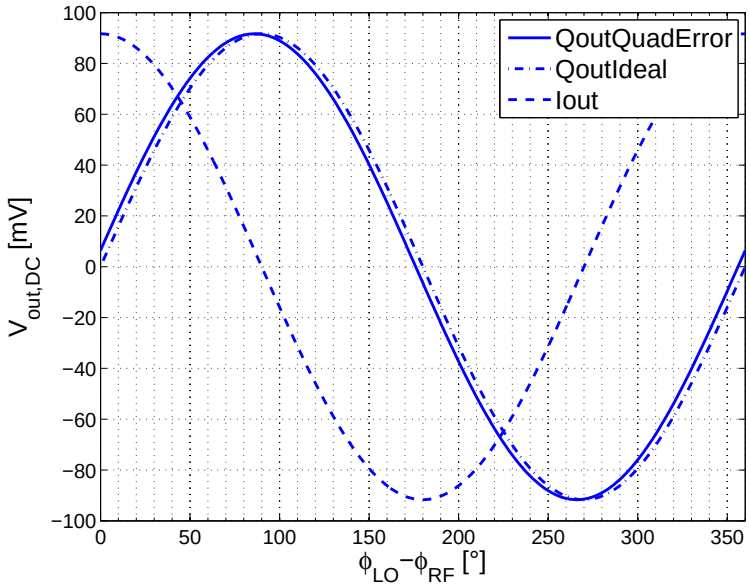


2.6.3 LO-swap functionality

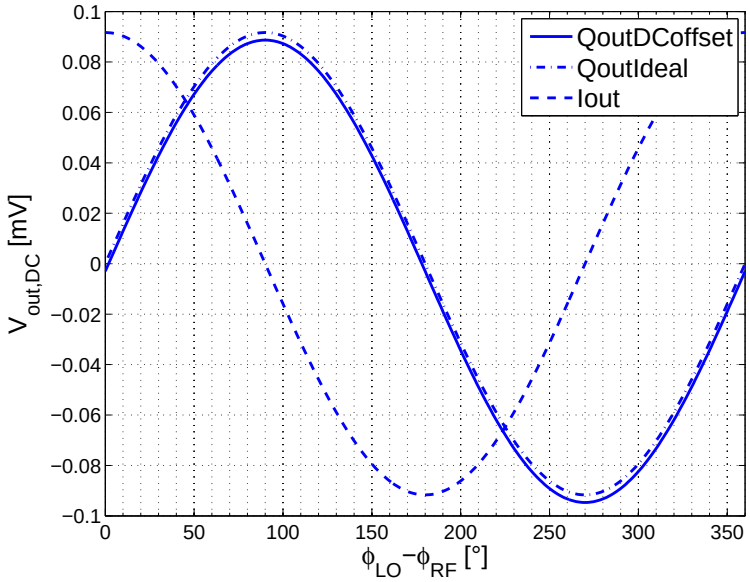
In section 2.4 the impact of mixer output offsets and quadrature error on the phase measurement has been discussed and indentified as the main causes of error. Here a simple calibration technique potentially capable of correcting both of these erros is described. To introduce this issue it is useful to observe what the I and Q output characteristics look like when affected by offset and quad error, compared to the ideal case. Fig.2.15a shows that an error in the phase shift between the LOs results in an *horizontal* shift of the output characteristics with respect to one another, while Fig.2.15b highlights that the presence of offsets produce *vertical* shifts of the waves. These observations introduce the issue of understanding if it is possible to compensate for these errors exploiting some kind of post-processing of the acquired values. Let's make some considerations:

- if the ADCs had infinite resolution, and if it was possible to change the RF phase with infinite resolution (without considering the possibly

Figure 2.15: I-Q characteristics



(a) Quadrature error



(b) DC offset

non-linear behavior of the phase shifter), the offsets could be directly measured, and the quad error could be estimated looking at the distance between the zeros of the I and Q characteristics;

- the phase shifter has finite resolution, thus it would be necessary to interpolate the measured points of the I-Q characteristics to find the zeroes, reducing the precision of the estimation.

- the limited resolution of the ADCs makes not possible to measure directly the offset. This makes even more difficult to have a good estimation of the quad error.

Therefore, it is not possible to perform these estimations by merely trying to post-process the acquired values. On the other hand, recalling the results of section 2.6.1 for the Gilbert mixer, it has been clarified that the output offset does not depend on the input signals, at least if the distortion is negligible. Such an approximation is satisfied in the considered conditions, because the worst-case effects of the non-idealities arise when the input power is minimum, hence with the mixers operating far from the compression point. This means that the offset can be considered a constant DC voltage superposed to the wanted DC signal.

If the LO signal is swapped, meaning that its phase is shifted by 180°, the I and Q wanted outputs change in sign. Recalling (2.1) the result of such an operation, taking into account the offsets, is the following:

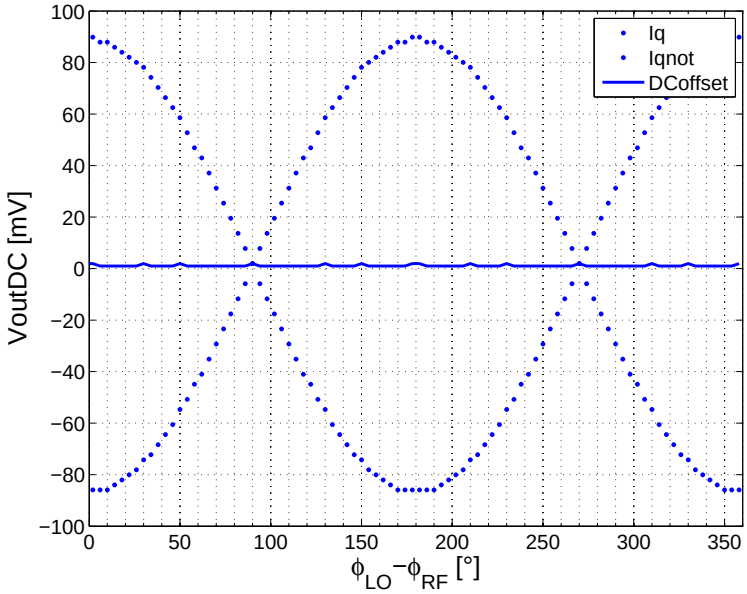
$$Iout(\phi_{LO} + \pi) + V_{OS,I} = -Iout(\phi_{LO}) + V_{OS,I}$$

$$Qout(\phi_{LO} + \pi) + V_{OS,Q} = -Qout(\phi_{LO}) + V_{OS,Q}.$$

It is therefore obvious that *averaging* the outputs obtained with the two configurations of the LO signals, the offsets can be estimated, since in this situation the measurement is performed on a signal detectable by the ADC. Still, considering the magnitude of the involved signals, this estimation is quite inaccurate. Looking at Fig.2.16 it is understood that, especially for very low offsets, the estimation varies with the input phase, and its characteristic resembles a square wave. In the specific case depicted in the figure, the offset is less than a LSB, so the estimated offset commutates between the LSB and half the LSB. Hence, it is intuitive that a way to improve the measurement is to average many estimations over the entire input phase sweep: the higher is the number of estimations the closer is the average to the real value. This artifice is not only useful for offset estimation, but also for quadrature error detection: in fact, the position of the zeroes of the real I and Q waves can be estimated in the crossings of the interpolated curves.

Summarizing, this technique potentially allows to compensate for both the discussed error sources, at the price of introducing a LO driver circuit capable of swapping the LO single-ended signals (thus inverting the differential LO drive) and doubling the measurements performed over the input phase range.

Figure 2.16: Offset estimation through LO swap

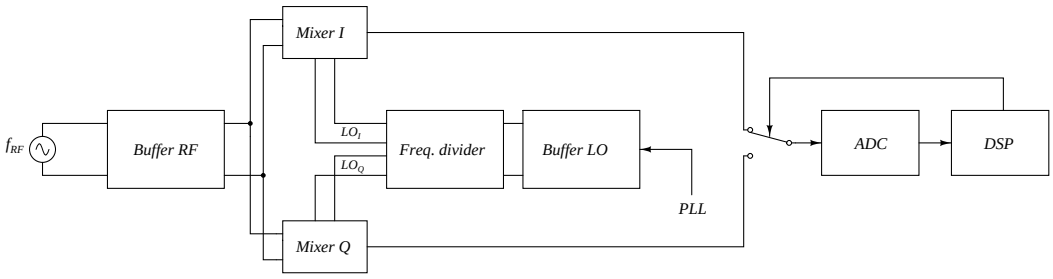


2.7 Detector top-level

So far the various blocks composing the system have been specified, analyzing their required characteristics and critical points. What remain to specify are the interfaces to the ports of the test chip: since the involved frequencies extend up to 12GHz (24GHz in the case of the divider input), the RF and LO input ports are fed by transmission lines, hence the input impedances of these blocks need to be matched to the characteristic impedance in order to keep a reasonable reflection coefficient. Since the input impedance of the divider and of the mixers, disregarding the employed topology, is not likely to be sufficiently high over the whole frequency range of interest, it has been decided to place in front of them a couple of high input impedance buffers preceded by impedance matching networks. These blocks are also needed to supply the following stages with the required currents, that for the mentioned reason are not negligible at the highest frequencies, without loading the input ports. The input buffers need also to be carefully layouted, because the parasitic capacitances on the input lines might worsen the impedance matching. Since the wanted output signals are at DC, instead, the mixer outputs will be directly connected to the relative port. The top-level architecture of the receiver is thereby shown in Fig.2.17.

Note that, if two ADCs are employed, also the impact of mismatch between

Figure 2.17: Top-level architecture of the phase and amplitude detector.



the converters should be considered. To avoid this further complication, only one ADC will be employed, and it will alternatively sample the two receiver outputs by means of a switch, like shown in the picture.

Chapter 3

Design

3.1 Overview

In this chapter the design of the presented circuit blocks is addressed. In section 3.3 it is described the optimization of the divider in order to improve the quadrature error without losing output power. In section 3.4 it is addressed the problem of which mixer topology to choose, and the design of the different solution is reported, together with the performances. The passive voltage-mode mixer and the current-mode, TIA loaded one have not been fully designed, but rather it has been conducted an investigation in order to understand if their performance are comparable to the Gilbert mixers'. The last section deals with the design of the buffers.

3.2 Active and passive devices: matching properties

The employed technology offers different types of components to build the circuits, which are characterized by different performances in terms of matching. Since this aspect is a particular concern in the context of this work, it is mandatory to understand which performance one might expect, and, if two types of components are available, which one is more reliable from this standpoint.

This is exactly the case of resistors, that are fabricated in two ways:

1. tantalum resistors;

2. polysilicon resistors.

The latter have a higher sheet resistance compared to the former, so they tend to occupy less area, but at the same time they exhibit a less precise absolute value and they can withstand a lower RMS current. The available data from lab measurements clarify that the matching properties of the polysilicon resistors are better than tantalum one: indeed, on equal area, the standard deviation of the $\frac{\Delta R}{R}$ in the tantalum case is 3 times the one measured for polysilicon. Hence, polysilicon resistors have been employed for the circuits described in this chapter.

Another comparison that can be done is between MOSFETs and HBTs, since the described mixer typologies employ them both as switches. In this case the issue is not as straightforward as in the previous case, since these two kinds of devices operate in a physically different way. Thinking of them like switches, the key parameter is the threshold voltage in one case, and the on-state base-emitter voltage, in the other. The available data predicts that, on equal area, the relative error of the threshold voltage has a standard deviation one order of magnitude higher than the $\frac{\Delta V_{be}}{V_{be}}$. This result advantages the bipolar option, even if it must be pointed out that FETs can be realized in a wider area range.

3.3 Frequency divider

Dividers are often among the most critical parts in high-frequency circuits. This block has been optimized starting from a previous version that does not have suitable performances concerning the purpose of this work. Fig.3.2 shows the full schematic of this circuit, composed of two CML flip-flops in cascade with negative feedback.

The first thing the should be pointed out is that, since this is a logic device, it has to be operated with signals capable of completely steer the differential pairs. This means that, taking into account the voltage drop on the emitter resistance, the output waveforms need to exhibit an amplitude satisfying

$$\Delta V > 4V_T + r_E I_{tail},$$

and since the thermal voltage and the emitter resistance both increase with temperature, this condition has to be checked at the maximum operating temperature. The differential amplitude ΔV coincides with the output swing of the latches: from this standpoint, care should be taken in avoiding the saturation of the HBTs, a condition that would slow down the commutation.

Regarding the input clock, it is driven by a sinusoidal wave provided by the transmission line, that needs to have an amplitude sufficient to get fast commutations, a concern especially a the low frequencies. To address this point another aspect typical of CML dividers needs to be clarified.

These systems are characterized by a self-oscillation frequency f_{so} due to the unstable equilibrium point they tend to assume: such a behavior stems from the presence of the cross-coupled pairs, which are elements widely used to build oscillators, since they exhibit a differential negative resistance. Thus, the divider operated without an input signal tends to show at the output an oscillation at f_{so}, while with a proper input signal it locks at half its frequency. This is a desirable property, since to produce an output signal at the self-oscillation frequency it is necessary a very low clock differential amplitude. Since the latch can be modeled (see [20]) like a system with no input, unity positive feedback, and open loop gain

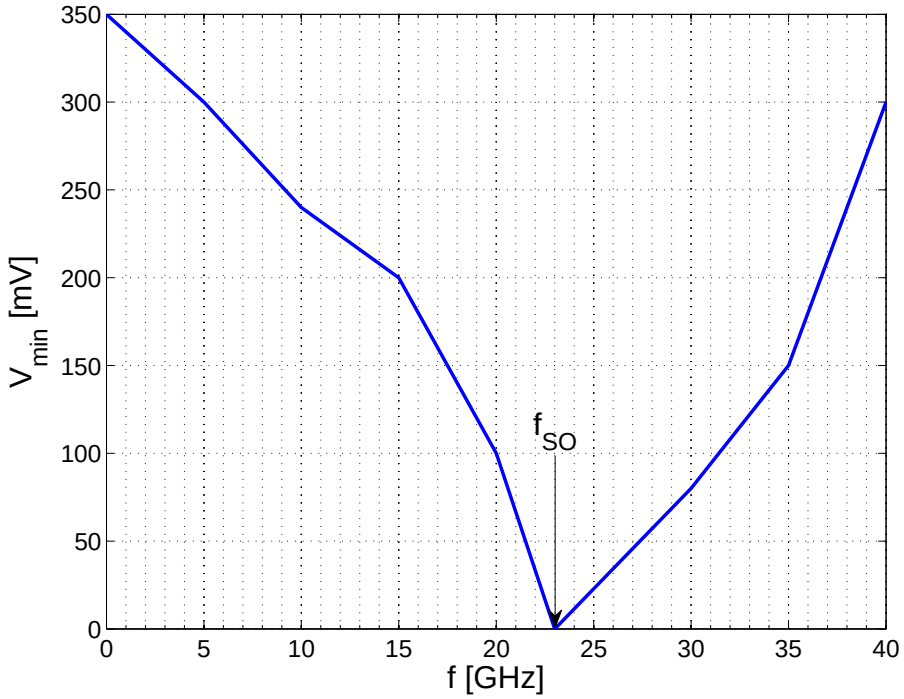
$$A_{OL} = \left(\frac{g_{mL} R_L}{1 + sR_L C} \right)^2$$

it is easy to see that a necessary and sufficient condition for the divider to self-oscillate is given by the bound

$$g_{mL} \cdot R_L > 1$$

where g_{mL} is the small signal transconductance of the latch HBTs. If such a condition is not met, the divider can still work, but it requires usually a higher clock amplitude, especially at low frequency. Usually, to give an intuitive interpretation of the phenomenon it is provided a graph called *sensitivity curve* relating the input frequency to the minimum input amplitude needed to achieve a reliable operation: an example of such a graph is reported in Fig.3.1, showing how the required amplitude drops practically to zero at $2f_{so}$. If the input signal has an amplitude less than the one specified by the sensitivity curve, the divider still operates, but the output spectrum is populated by further harmonics, because during the slow commutation of the clock differential pair enough time is left for the device to self-oscillate, resulting in bursts superposed to the wanted output [21].

Figure 3.1: Sensitivity curve of a CML frequency divider



3.3.1 Design

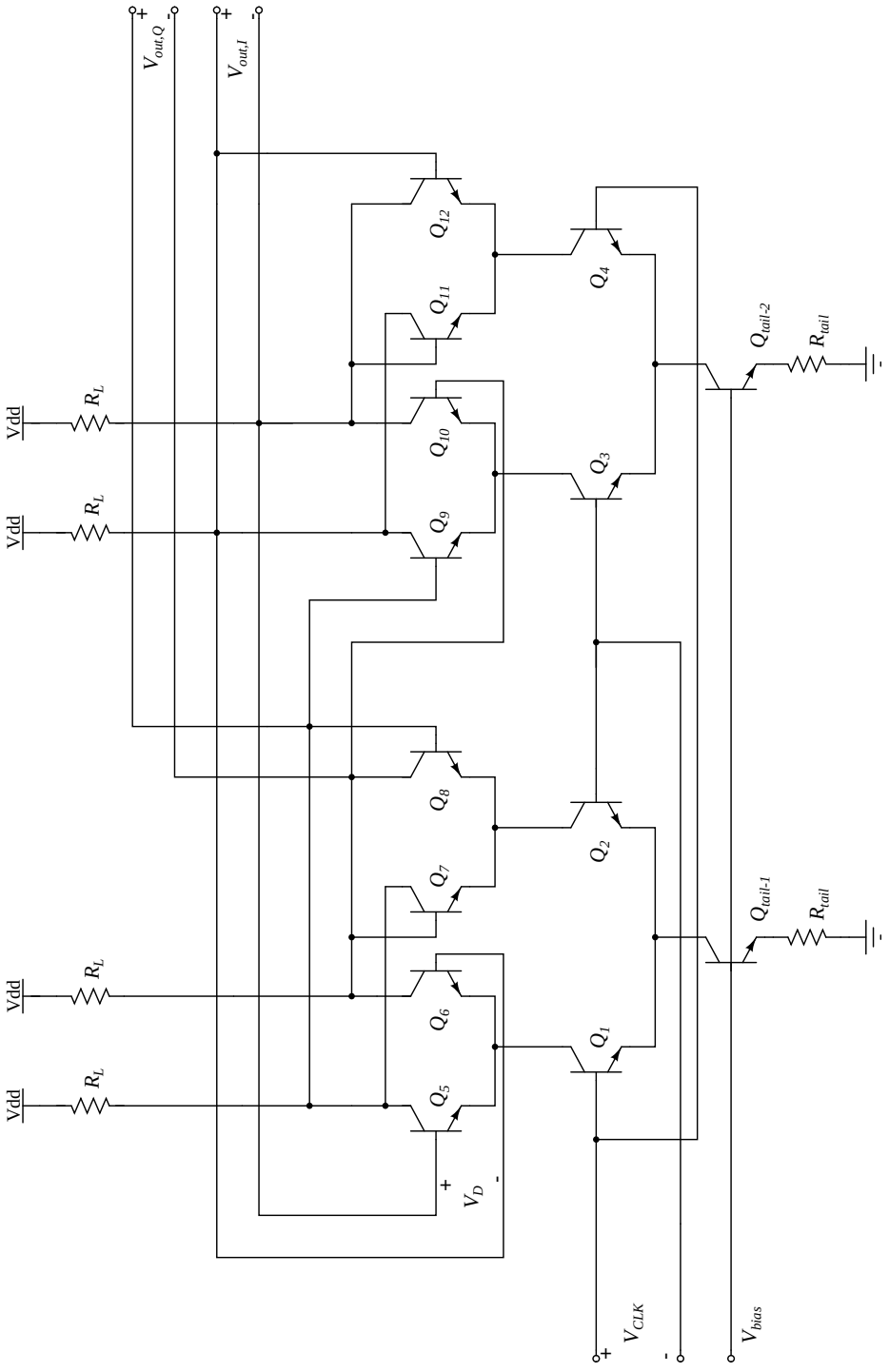
In this work, the goal is to obtain a better matching among the components, making the device at least functional (i.e. capable of dividing) up to 135 °C as a conservative rule. Therefore, the adopted approach has aimed to scale the transistor emitter lengths, meanwhile verifying the perfomances in terms of:

- commutation speed;
- output swing;
- standard deviation of the phase quadrature error, simulated through a Monte Carlo analysis.

The speed of the system is basically limited by the time constant found at the output node: when the device has to switch, indeed, it needs to charge the total output capacitance, given by the following expression (referring to the node connected at the collector of Q_1):

$$C_T = C_{cs1} + C_{bc1} + C_{cs7} + 2C_{bc7} + C_{be8} + 2C_{bc8} + C_{be9} + (1 - A_v)C_{bc9}$$

Figure 3.2: Schematic of the CML frequency divider



Considered this, the latch delay results $\tau_{latch} = R_L C_T$, and the maximum frequency of the clock signal is roughly bounded by two latch delays:

$$f_{max} = \frac{1}{2\tau_{latch}}$$

Other authors give a slightly different solution of this problem [20], whose accuracy depends also on the technology adopted (either CMOS or bipolar). Anyway, the result should be taken as an indication, because it cannot take into account the effect of the parasitics, and of the asymmetries introduced by the layout, that is a very critical aspect. Table 3.1 shows the performances of the first version of the divider, tested with an ideal input buffer, and driven by an input power $P_{in} = 3dBm$, which has resulted to be sufficient to guarantee correct operation over the whole frequency range. The parameter $\sigma_{\phi err}$ identifies the standard deviation of the quadrature error, and is evaluated at $f_{out} = 12GHz$, $T = 85\,°\text{C}$ and $V_{cc} = V_{cc,nom} + 5\%$, because this is the worst case condition. The parameter l_e refers to the emitter length of the transistors composing the clock, sampling and latching pairs, and it has been scaled up to 4 times the original size, decreasing at the same time the value of the load resistors, in order to keep the same output swing. How can be observed, the maximum frequency of operation increases with the size, because the total capacitance at the output node does not grow linearly meanwhile (due to the contributions of the base-collector and collector-substrate capacitances). Of

Table 3.1: Performances of the frequency divider.

l_e [μm]	I_{tail} [mA]	R_L [Ω]	f_{max} [GHz]	$\sigma_{\phi err}$ [°]
$l_{e,ref}$	1.7	140	65	0.43
$2l_{e,ref}$	3.4	70	78	0.3
$4l_{e,ref}$	6.8	35	89	0.26

course, this result is not reliable, since it has been tested the divider without a load and with an ideal input, but it gives an indication on the potential performances of the divider. The configuration finally chosen is the one with $l_e = 4l_{e,ref}$. Section 3.5 deals with the design of the EFs, and it gives an overlook on the performances in the practical configuration. It has been decided to buffer not only the input but also the outputs of the divider, mainly for two reasons:

- the switching cell of the mixers exhibits a capacitive input impedance at high frequency, that would add up to the other contributions, slowing

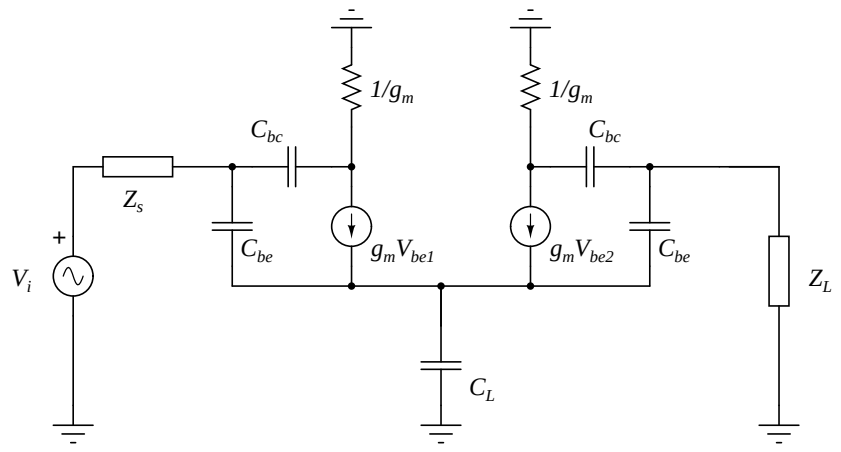
down the commutation;

- one of the versions of the Gilbert mixer has been designed with a DC coupling to the switching cell, and the buffer is useful as a level-shifter, providing a suitable DC operation point.

Finally, to achieve a reliable operation also at 135 °C the output swing has been increased, with respect to the original configuration, by setting the value of the load resistance at 45Ω, that gives $\Delta V = 0.3V$. This is useful because it guarantees correct switching even in the condition of reduced supply voltage ($V_{cc} = V_{cc,nom} - 5\%$), and it further speeds up the commutation without compromising the operation of the following stages. The self-oscillation frequency results to be $f_{so} = 21.8GHz$.

3.3.2 Stability

Figure 3.3: Small signal equivalent circuit for stability analysis



Since at the RF frequencies of operation the inductive and capacitive parasitics are absolutely not negligible, as explained in section 1.5.6, a common practice consists in make sure that the circuit interfaces are unconditionally stable, meaning that for every possible source and load impedance, the magnitude of the reflection coefficient at the input and output port keeps lower than one. A couple of conditions that are usually checked to ensure this safe behavior are the Rollet's one

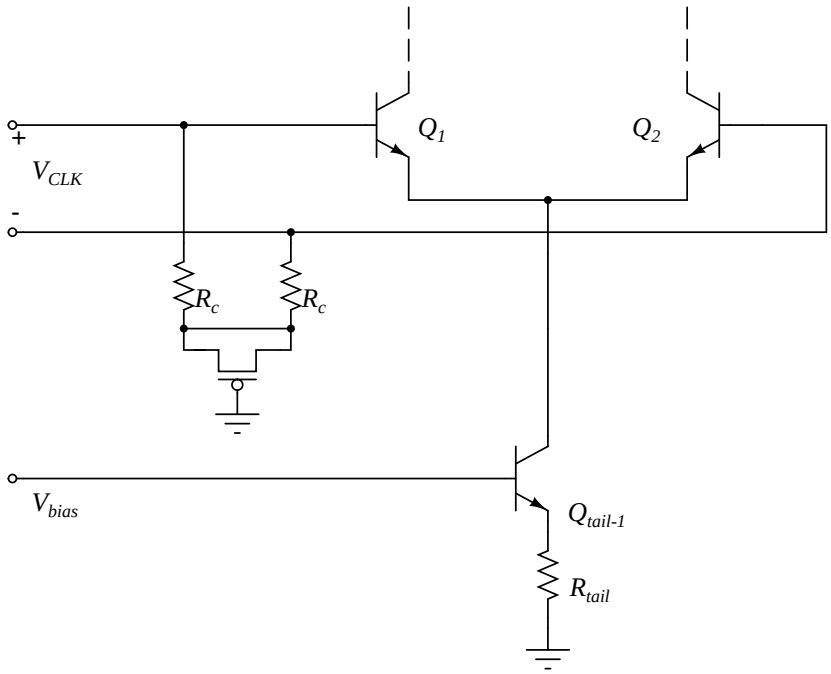
$$K_f > 1$$

along with the auxiliary condition

$$b_{1f} > 0.$$

These conditions need to be checked especially in the most critical conditions, which are usually at the minimum operating temperature and with the maximum supply voltage, because the transconductance of the HBTs is thereby maximized. Stability should be checked relatively to each pair of ports in the circuit, considering both single-ended and differential stimuli. In this case the differential ports are generally less critical than the single-ended ones: for example, if the input impedance of the clock differential pair is considered, it is easy to see that at high frequency it is essentially given by the base-emitter capacitance in series with the base resistance, since the Cascode level represented by the upper pairs does not produce a significant Miller effect, and this is true independently of the considered load impedance Thus, the input

Figure 3.4: Compensation network added to the clock input



reflection coefficient results

$$|\Gamma_{in}| = \left|\frac{Z_{in} - Z_0}{Z_{in} + Z_0}\right| = \left|\frac{r_b + \frac{1}{sC_{be}} - Z_0}{r_b + \frac{1}{sC_{be}} + Z_0}\right| < 1$$

and in this situation the circuit is unconditionally stable. If instead single-

endend impedances are considered, the situation is different: for example, suppose the input port to be connected to a terminal of the clock differential pair, while the output port is connected to the other one. This situation could happen in practice if a disturb was superposed to the wanted signal only on one input line, at the LO port. The equivalent small signal circuit is shown in Fig.3.3. It can be observed that the circuit in this configuration resembles an EF buffer, due to the low impedance seen at the emitters of the Cascode level. Neglecting the base-collector capacitances, the impedance seen by the input port, after Z_s is

$$Z_{in} = \frac{2}{sC_{be}} \cdot \frac{1 + s\left(\frac{Z_L C_{be}}{2} + \frac{C_L}{g_m}\right) + s^2 \frac{C_L C_{be}}{2g_m^2}}{1 + s(Z_L C_{be} + \frac{C_L}{g_m}) + s^2 \frac{C_L C_{be}}{g_m^2}}.$$

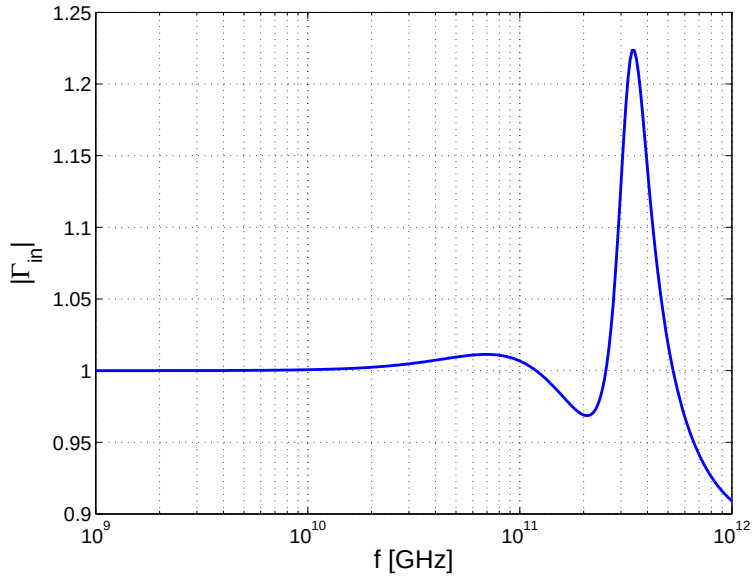
If an inductive output impedance is taken into account, which is realistic for an EF, the magnitude of the reflection coefficient results to be the one shown in Fig.3.5a, and it is clear that in this situation the system is conditionally stable. A way to fix this could be to put some series resistance in front of the bases of the HBTs composing the differential pair, but this solution has been found to be not suitable because it requires too high values of the resistors. An alternative solution, is the one shown in Fig.3.4, showing the compensation resistors in parallel with the input. From a differential signal standpoint, they consist in a further load of magnitude equal to $2R_c$. A single-ended signal, instead, sees only R_c if the MOS capacitor is suitably dimensioned. Remembering that the aim is to make the total impedance show a positive real part, let's see the effect of R_c at the frequencies for which, on the contrary, Z_{in} assumes a negative real part:

$$Z_{in}(j\omega_0) = -R(j\omega_0) + jX(j\omega_0)$$

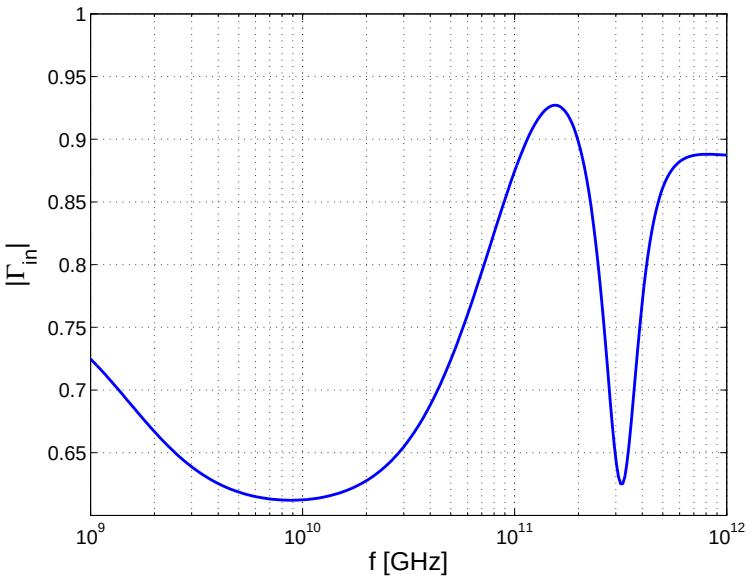
$$Z_{in,tot}(j\omega_0) = R_c//Z_{in}(j\omega_0) = \frac{R(j\omega_0)R_c(R(j\omega_0) - R_c) + R_c X^2 + j(R_c^2 X)}{(R_c - R)^2}.$$

It is therefore clear that a sufficiently low resistance should fix the problem. It has been verified experimentally that a $R_c = 400\Omega$ is sufficient to solve the problem and get unconditional stability. Fig.3.5b shows the input reflection coefficient with the compensation resistors added, considering the same inductive load used for Fig.3.5a.

Figure 3.5: Input reflection coefficients considerated in the stability analysis



(a) Non-compensated case



(b) Compensated case

3.4 Mixers

In this section it is faced the design of the mixers. Several solutions have been tested in order to understand which one is the most suitable. First, the design of the standard Gilbert double-balanced mixer is addressed, hence it is described the design of the Gilbert mixer with the LO-swap feature. Finally, also the mixers with MOS switching cell are presented.

3.4.1 Gilbert double-balanced mixer

This structure, probably the most used to build mixers, has been briefly discussed in section 2.6.1. It has been optimized in order to get the best possible matching, thus the lowest output offset and to reach this goal more than one configuration has been investigated.

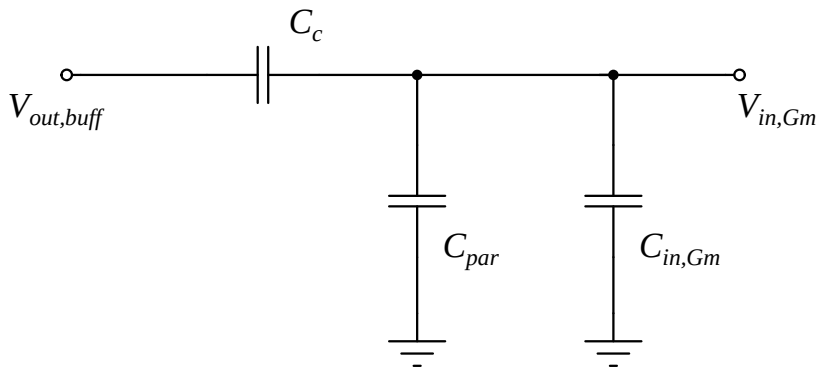
Input dynamic range As specified, the detector has to guarantee its performances on an input dynamic range of 20dBm. For all the Gilbert mixers that have been designed and tested, it has been verified that the minimum manageable input power is approximately -20dBm: below this bound, in fact, the effect of mismatch cause the phase error to exceed the specs. Thus, in the following discussion on Gilbert mixers it is assumed a minimum power level $P_{RF,MIN} = -20dBm$ and a maximum one $P_{RF,MIN} = 0dBm$.

Coupling The first question to answer has been how to couple the mixer to the RF buffer and to the frequency divider. This raises some considerations:

- coupling capacitors prevent the propagation of the DC offset between the connected stages, avoiding it to contribute to the overall output offset;
- coupling capacitors contribute to the capacitve loading of the driven stage through the parasitics, and this can be a problem if the absorbed current is high enough to cause distortion;
- coupling capacitors are further components that are affected by mismatch;
- coupling capacitors are typically area-consuming, so if possible it is better to avoid them.

Concerning the RF input, it has been verified by simulation that a fully matching-optimized input buffer does not contribute with an input offset sufficient to justify the insertion of capacitors to cancel it out. Moreover, at high frequency the input impedance of the transconductor is basically capacitive, hence the voltage signal at its input is determined by the equivalent capacitive divider: such a situation is graphically highlighted by Fig.3.6. This is a further reason to choose DC coupling at this input port, because, as clarified in section 2.4.2, the limited ADC resolution makes important to maintain the highest possible signal level. Regarding the switching cell, the issue is a bit tricky, because in this case the insertion of the capacitors *worsen* the output

Figure 3.6: Effect of coupling capacitors on input stage



offset, even with big, well-matched capacitors, exactly the contrary of what one might expect. The reason behind such a behavior is that the capacitive loading effect due to the parasitics slows down the commutation, enhancing the effect of the other offset sources. Therefore, the first version of the Gilbert mixer has been designed with DC coupling at both the RF and LO ports.

Transconductor Basically, a transconductor is a block providing conversion from the voltage domain to the current one with gain G_m, and in differential circuits it is usually realized employing an emitter (source) coupled pair. The transconductor is the main source of distortion in the Gilbert mixer, thus it must be carefully dimensioned in order to avoid nonlinearities, especially at the highest input power. There are two situations that must be avoided, in this sense:

- the transistors (the HBTs composing both the differential pair and the tail generator) must not saturate, otherwise their transconductance and output resistance would drop resulting in a non linearity;
- the tail current must not be completely steered by the input signal, a situation that would produce distortion as well.

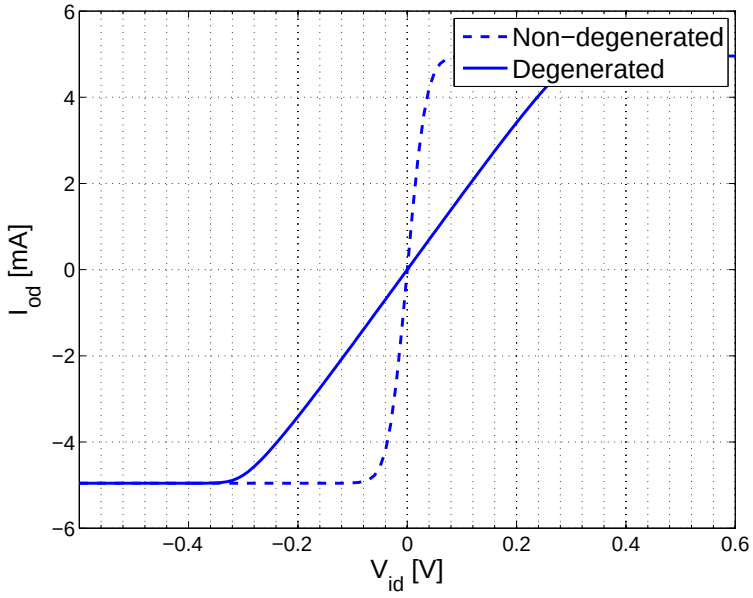
The DC transfer characteristic of an emitter-coupled pair is given by

$$I_{od} = I_{o1} - I_{o2} = I_{tail} \cdot tanh\Big(\frac{-V_{id}}{2V_T}\Big). \tag{3.1}$$

the previous result can be obtained by applying the KVL at the differential input, and recalling the exponential $i_c - V_{be}$ relationship typical of bipolars. This relationship is plotted in Fig.3.7, where it is highlighted that to completely

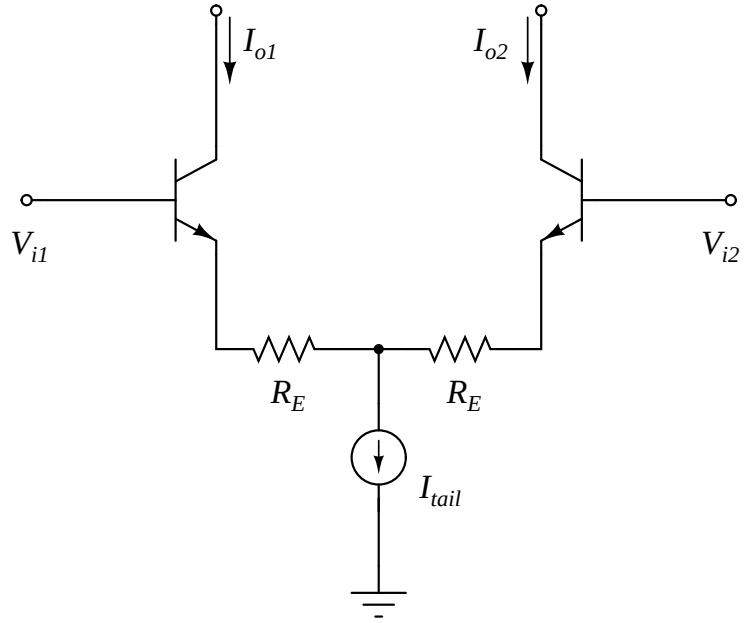
steer the tail current a voltage $V_{id} \simeq 4V_T$ is required, as pointed out also in section 3.3. To enhance the linearity of the differential pair, emitter degeneration

Figure 3.7: DC characteristic of a differential pair with $I_{tail} = 5mA$

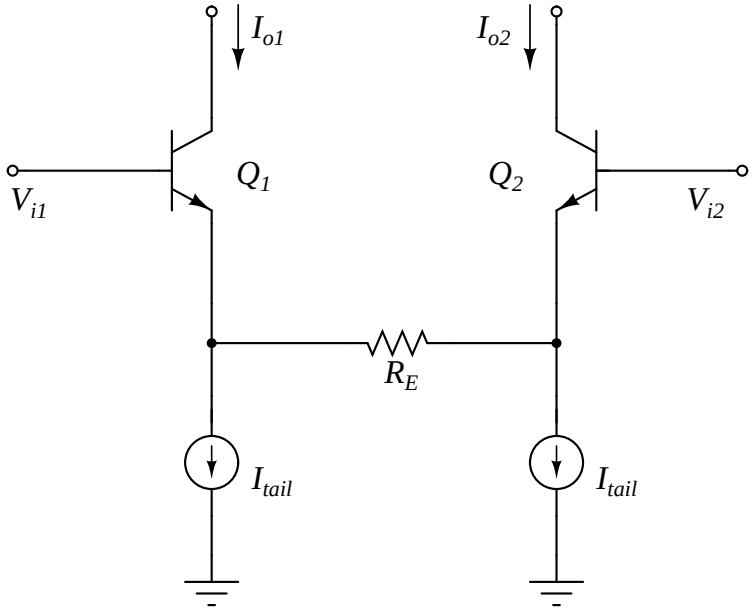


is usually exploited, which can be either resistive or inductive. In this work it is desirable to avoid the usage of inductors due to their area occupation, thus resistive degeneration has been employed. Its effect is easy to understand without employing further formulas: in the degenerated pair, when the current is completely steered, the voltage drop on the resistor connected to the transistor being on is $R_E I_{tail}$, while on the other resistor there is zero drop. This means that the input voltage needed to completely steer the current is roughly extended by $R_E I_{tail}$, with respect to the non-degenerated case. Fig.3.8 shows two examples of degenerated transconductors. To understand the reason behind the choice of the adopted solution it is useful a numerical example: considering that the divider outputs are biased at $V_{dd} - \Delta V/2 = 3.15V$, and that they are buffered, the switching cell is driven with a DC level $V_{b,switch} = V_{out,div} - V_{be} \simeq 2.3V$ (since the HBTs have a $V_{be} \simeq 800 - 900mV$), thus at the collectors of the HBTs belonging to the transconductor it is found DC level of approximately $V_c = V_{out,div} - 2V_{be} \simeq 1.5V$. Suppose that at the tail transistor collector is present a DC voltage level of $V_t \simeq 700mV$, in order to keep it safely in the active region. If the transconductor of Fig.3.8a is employed, and a voltage drop $R_E I_{tail}/2 \simeq 100 - 200mV$ is present on the degeneration resistors, as a

Figure 3.8: Resistive degeneration in differential pairs



(a)



(b)

result Q_1 and Q_2 would operate with a DC collector-emitter voltage

$$V_{ce,DC} = V_c - R_E I_{tail}/2 - V_t \simeq 500mV.$$

If the maximum input power $P_{RF,MAX} = 0dBm$ is applied, that means a differential amplitude of $V_{RF} \simeq 450mV$, then Q_1 and Q_2 would likely reach

the saturation. Following these simple considerations the transconductor of Fig.3.8b has been preferred, because it has the advantage of saving the voltage drop on R_E. Moreover, it has a single degeneration resistor, instead of two, that is better from a matching standpoint. On the other hand, it should be pointed out that common-mode signals, with this configuration, do not see the degeneration resistance, hence the CMRR of this stage relies on the output impedance of the tail current generators, that is mainly capacitive at high frequencies. The differential transconductance of this stage, easily obtained from the small-signal equivalent circuit, is

$$G_m \simeq \frac{g_m}{1 + g_m \frac{R_E}{2}} \cdot \frac{1 + s\frac{R_E}{2}C_L}{1 + s\frac{C_L + C_b e}{g_m}}. \tag{3.2}$$

The common-mode transconductance results

$$G_{m,cm} \simeq \frac{sC_L}{1 + s\frac{C_L + C_b e}{g_m}}$$

and thereby the CMRR is

$$CMRR = \frac{g_m}{sC_L(1 + g_m R_E)}(1 + sR_E C_L)$$

confirming that, at high frequency, the common-mode rejection is limited by the tail generators capacitance.

The complete schematic for this mixer core is reported in Fig.3.9.

Noise Noise is not among the specifications, in this work, but it is anyway good to make the devices the least possible noisy, without compromising the other performances.

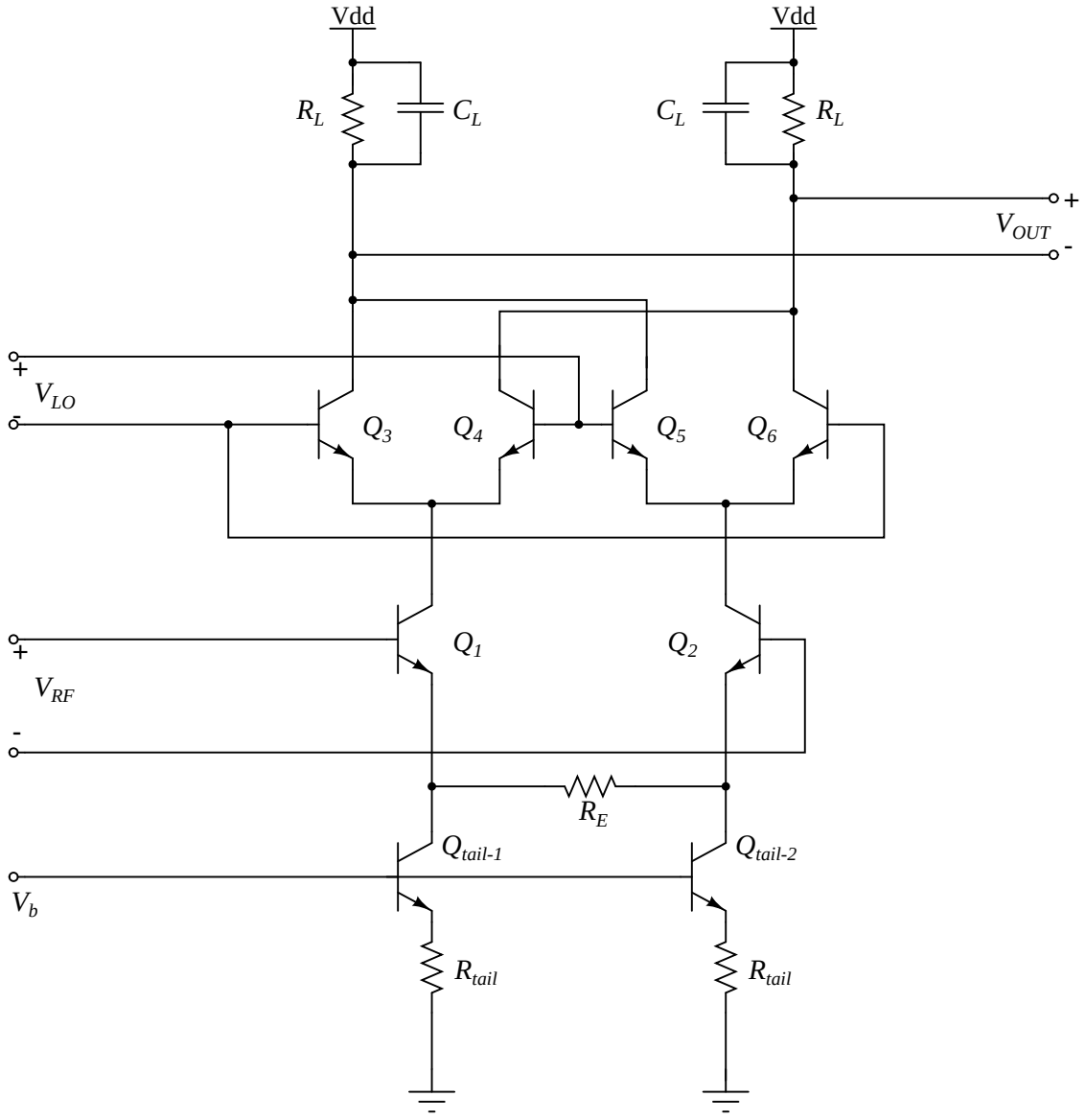
To understand which are the parameters to set in order to minimize the noise figure it is worth making some investigations on the contributions. The following analysis is referred to the approach extensively explained in [13, pp. 748-788]. Noise in bipolar transistors belongs to three categories:

1. thermal noise due to the resistive contribution, such as the base resistance;

2. shot noise, a kind of white noise typically found in junction devices, related to the flow of DC currents;

3. burst noise and flicker noise, that are both low-frequency noise with a

Figure 3.9: Schematic of the matching-optimized Gilbert mixer



PSD that decreases with frequency, and they are usually related to the base current.

It can be demonstrated that the noise sources in a bipolar can be modeled through an equivalent voltage noise generator placed in series to the base, and a current one connected in parallel. In particular, the equivalent voltage PSD is given by

$$\frac{\overline{v_{eq}}^2}{\Delta f} = 4kT\left(r_b + \frac{1}{2g_m}\right)$$

taking into account the thermal noise due to the base resistance and the shot

noise related to the collector current I_c. Similarly, the equivalent current PSD results

$$\frac{\overline{i_{eq}}^2}{\Delta f} = 2qI_b + K_1' \frac{{I_b}^a}{f} + \frac{I_c}{|\beta(j\omega)|^2}$$

where the last two terms represent the mentioned low frequency noise.

Now, these generators are used to find equivalent input-referred noise generators for the whole transconductor, taking into account also the degeneration, and the effect of the tail current generators. Generally, since the noise contribution of the transistors are independent, the transconductor from the noise standpoint cannot be simplified employing single-ended equivalent circuits. Anyway, the noise can be modeled using equivalent noise generators referred to each input, like shown in Fig.3.10a. In this context, only the voltage generators are calculated, since the transconductor is driven by a low impedance source, thus the current generators have no practical impact. Moreover, the fact that the transconductor has high CMRR, at least at low frequency, permits to further simplify the problem, because it is possible to move, without losing information, one of the voltage noise generators to the other input, thus leading to the schematic of Fig.3.10b.

The analysis to calculate the expression for the PSD of the input voltage noise generator is described in appendix A, whilst here it is reported the result:

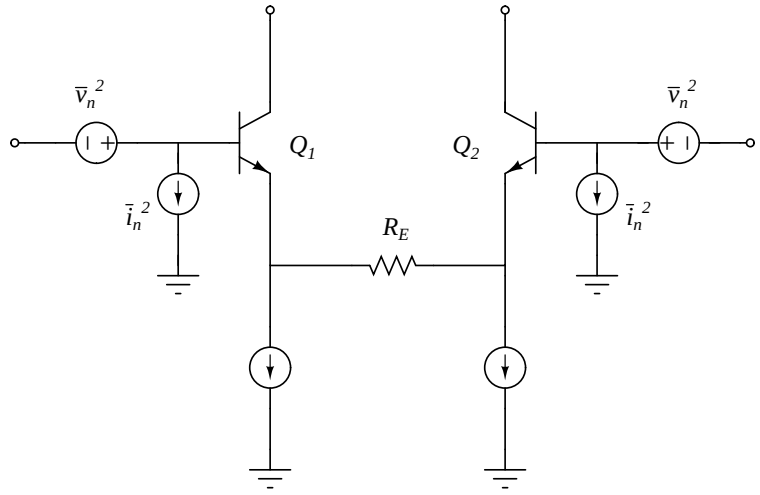
$$\begin{aligned}\frac{\overline{v_{eq}}^2}{\Delta f} &= 2 \cdot 4kT \left[r_{b1} + \frac{1}{2g_{m1}} + \left(r_{b,tail} + \frac{1}{2g_{m,tail}} + R_{deg} \right) \cdot \left(\frac{g_{m,tail} R_E}{1 + g_{m,tail} R_{deg}} \right)^2 \right] \\ &\quad + 4kTR_E \\ &= 4kTR_{eq}\end{aligned} \tag{3.3}$$

Noise is subjected to mixing as well as any other signal. This means that, at the output of the mixer it will be found a noise PSD which, at each frequency, is the sum of all the noise contributions resulting from the mixing with the LO signal and its harmonics[22]: for a given frequency f_0, thus, the terms of interest lay at the frequencies $f_{LO} \pm f_0$, $3f_{LO} \pm f_0$, $5f_{LO} \pm f_0$, and so on. To calculate the output noise, it is necessary to sum all these terms, that results in the multiplication by the factor

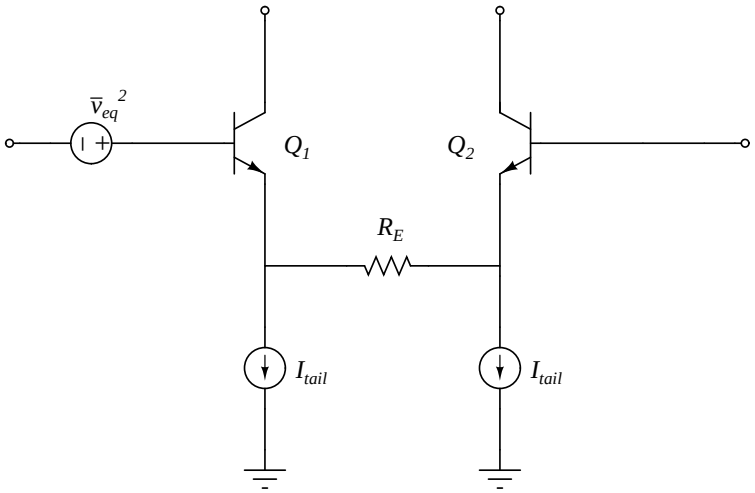
$$n = 2 \cdot \left(1 + \frac{1}{3^2} + \frac{1}{5^2} \dots \right) = \frac{\pi^2}{4}.$$

Supposing that the switching cell contributes in a negligible way, taking into

Figure 3.10: Representation of the transconductor with equivalent input noise generators



(a)



(b)

account the gain of the mixer and the contributions of the load resistors, the total output noise PSD results

$$\frac{\overline{v_{n,o}}^2}{\Delta f} = 8kTR_L + n \cdot \left(\frac{2}{\pi} G_m R_L\right)^2 \cdot 4kTR_{eq}.$$

The spot SSB (Single Side Band) noise figure is thereby calculated, referring

to an equivalent source noise taken into account through the resistor R_s:

$$\begin{aligned} NF_{SSB} &= \frac{SNR_{in}}{SNR_{out}} = \frac{P_{in}}{G_{mix}^2 P_{in}} \cdot \frac{v_{n,o}}{v_{n,i}} \\ &= \frac{8kTR_L + n \cdot \left(\frac{2}{\pi} G_m R_L\right)^2 \cdot 4kTR_{eq}}{\left(\frac{2}{\pi} G_m R_L\right)^2 \cdot 4kTR_s} \end{aligned} \tag{3.4}$$

This result highlights that, to reduce the noise figure, since the values of the physical resistors will be set by other requirements, it is useful to maximize the size of the transistors or employ multiple base configuration, where possible, to reduce the base resistances, meanwhile avoiding excessive biasing currents that would enhance the shot noise contribution.

Note that, for simplicity, the presented results do not take into account the filtering effects of the parasitic capacitances. The simulated noise figures, indeed, approximately matches the prediction provided by this analysis only setting quite low LO frequencies.

In the following sections, the noise figure is employed to provide a further comparison between the different types of mixers that have been investigated. All the results refer to a reference source noise resistance of 100Ω.

Bias current choice and components sizing In section 2.6 it has been derived the ideal gain of the Gilbert mixer, expressed by (2.6). Obviously this holds in the case of perfect, square-wave like, switching. In practice, due to the finite bandwitdh of the driver circuit, the cummutation takes some time, resulting in a certain reduction of this gain: recalling Fig.2.11, equation (3.1) and under the hypotesis of linear transconduction, the differential output current is:

$$\begin{aligned} \Delta I &= I_{o1} - I_{o2} = I_{S1} + I_{S3} - (I_{S2} + I_{S4}) \\ &= \left(I_{bias} + \frac{i_{RF}(t)}{2}\right) \cdot tanh\left(-\frac{v_{LO}(t)}{2V_T}\right) - \left(I_{bias} - \frac{i_{RF}(t)}{2}\right) \cdot tanh\left(\frac{v_{LO}(t)}{2V_T}\right) \end{aligned} \tag{3.5}$$

neglecting, thus, the bias terms, and imposing $\frac{i_{RF}(t)}{2} = G_m \frac{v_{RF}(t)}{2}$,

$$\Delta I = -G_m v_{RF}(t) \cdot tanh\left(\frac{v_{LO}(t)}{2V_T}\right).$$

By averaging this function over the RF period, the DC value of the output differential current is obtained.

A few considerations on the bias and resistor size choice are now discussed. The expression of the transconductance for a bipolar transistor is $g_m = \frac{I_c}{nV_T}$, where the factor $n \simeq 1.5 - 2$ takes into account the degeneration effect of the parasitic emitter resistance. Substituting (3.2) in (2.6) and expanding it is obtained:

$$G_{mix} = \frac{4}{\pi} \cdot \frac{R_L I_c}{2nV_T + R_E I_c}. \tag{3.6}$$

This equation identifies three quantities to work on:

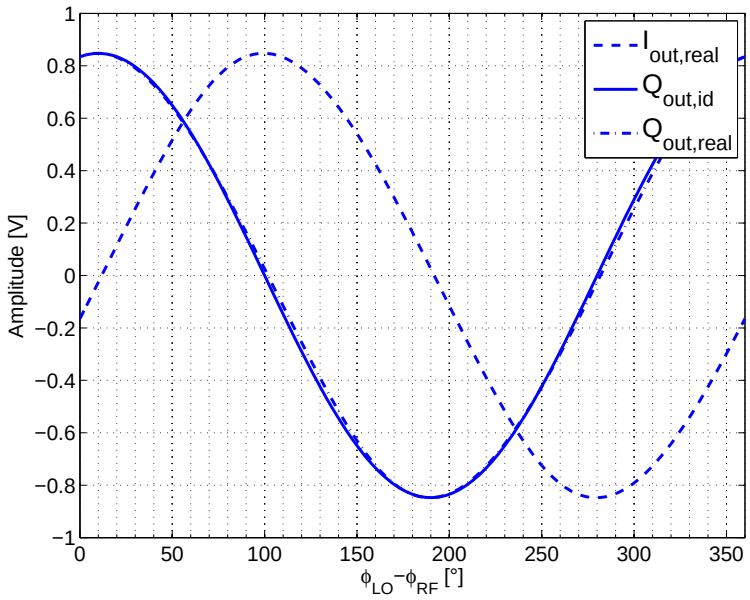
1. linearity, quantified by $R_E I_c$ (provided that all HBTs work in the active region);
2. gain G_{mix};
3. voltage drop on the load resistors $R_L I_c$.

In particular, the effect of the circuit parameters are:

- increasing the current enhances gain and linearity, but also decreases the DC output common mode, possibly leading to switches saturation;
- increasing R_E improves linearity but decreases G_{mix};
- increasing R_L enhances G_{mix}, but lowers the output common mode.

Before effectively sizing the components one last phenomenon has to be considered. Mixers are being used to provide a DC voltage proportional to the cosine of the phase difference between RF and LO. When this shift is 90°, the differential output at DC should be zero, even with the most powerful input, and in that particular situation the HBTs componsing the switching cell have to commutate when the current is at its absolute maximum value. The described switching condition is the worst-case one, because the base-emitter junction of the switch is flooded by diffusion charge due to the high corrent conduction, resulting in a big equivalent capacitance to discharge, that requires time. The practical effect of this phenomenon is a non-zero DC value for a 90° RF-LO phase shift. Fig.3.11 reports the result of a simulation which clarifies the behavior of the mixer over the whole phase range. As can be observed, the real characteristic is perfectly aligned to the ideal one near the top and bottom values, while tends to drift slightly around the zero values. This provokes of course a phase detection error, but the most critical effect regards

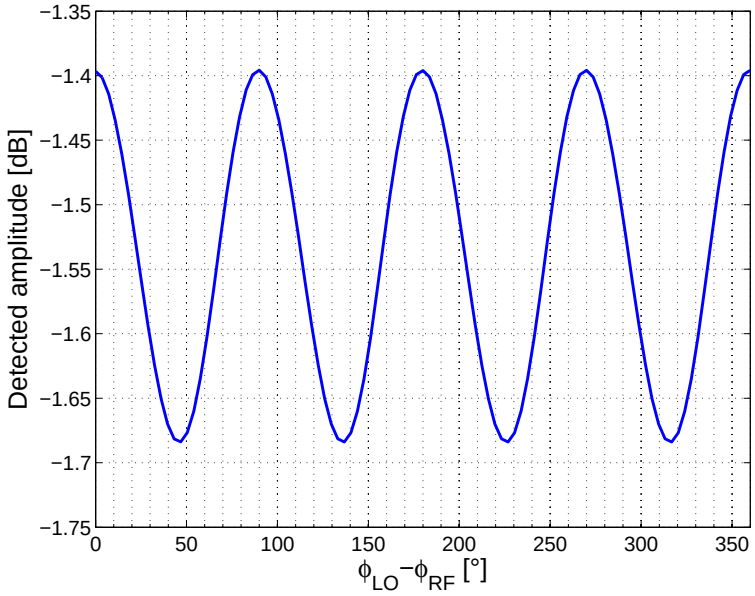
Figure 3.11: Effect of limited switch bandwidth with max RF power



the amplitude detection: indeed, the phase error consists in a deviation from the ideality which, as verified *a posteriori* simulating the optimized circuit, reaches up to 1°, but without a serious offset impact, because the amplitude considered is two to three orders higher. Regarding the amplitude, instead, the effect is depicted in Fig.3.12, where it is shown that the detected value is not constant over the phase shift, but exhibits an 'oscillation'. Remembering the specification bound of $0.5dB$, it is clear that this behavior could lead the detector to exceed the amplitude error bound in some very particular conditions, for example the combination of a reduced tail current and an 'unlucky' value of the RF-LO phase shift. For this reason, the linearity of the mixers needs to be carefully oversized, to keep some safety margin.

Regarding the transistors emitter lengths and configuration choice, the transconductor HBTs have been set at the maximum available size and in double-emitter configuration, exploiting the best possible matching to minimize their offset contribution, enhancing the transconductance, and minimizing the equivalent base resistances, thus the noise contribution. The switching cell HBTs have been sized in the same way, even if big transistors mean big capacitances to be driven by the LO, because it has been verified by simulation that this configuration leads to the minimum offset contribution, hence to the minimum phase error. The tail transistors, instead, have been kept as small as possible so as to minimize their base-collector and collector-substrate

Figure 3.12: Effect of limited switch bandwidth with max RF power



capacitances and obtain the best CMRR even at high frequnecy. Concerning the remaining parameters, the adopted solution has been the following:

- $I_{tail} = 4.7mA$;
- $R_L = 180\Omega$;
- $R_E = 80\Omega$.

The nominal performances thereby result:

- gain $G_{mix} = 6.9dBV$;
- input-referred 1dB compression point $1dBCP = 3dBm$;
- output common-mode DC voltage $2.45V$;
- $NF_{SSB} \simeq 10dB$ in the white, with a corner frequency $f_{co} \simeq 1kHz$.

Stability Being a circuit that operates at high frequency, the mixer has to provided with stable interfaces to make sure that no unwanted oscillations show up. The stability issue has been faced the same way as seen for the divider in section 3.3.2, because it also relies on differential pairs. The most critical interfaces to stabilize result to be the single-ended one, because the circuit tends to respond like an emitter follower, that is known to have an

high frequency input impedance with a potentially negative real part. The solution found to solve the problem matches again the one adopted for the divider, which is depicted in Fig.3.4. The stability checks have been carried out between all pairs of ports, both single-ended and differential, verifying that the stability conditions $K_f > 0$ and $B_{1f} > 0$ hold in all the cases.

3.4.2 Gilbert mixer with LO-swap functionality

In this section it is discussed the designed of the Gilbert double-balanced mixer featuring the LO-swap functionality which, as explained in section 2.6.3, provides the possibility of detecting both the DC offset and the quad error. It has been mainly an evolution of the design described in the previous section, hence the relevant differences are going to be explained. Since the offset is going to be compensated, it is not necessary to fully optimize this stage in terms of matching, then it is possible to improve other aspects. On the other hand, it is useful to get good matching where possible without compromising other performances.

LO driver circuit The complete schematic of this mixer is shown in Fig.3.13. The LO driver circuit, that must be capable of providing the LO inversion of phase, has been built exploiting the same structure of the basic mixer: the transconductor is driven directly by the divider, that makes it switch sharply, thus it needs no degeneration, while the block called 'switching cell' here is DC-driven by a logic gate, and is exploited to swap the currents generated by the transconductor, getting the desired inversion. When the circuit operates, only two of these four transistors are on, thus the circuit assumes the structure of a Cascode amplifier, that has the advantage of a reduced input capacitance.

The transistors belonging to the input differential pair have been set at maximum size because the input capacitance of the stage mainly depend on the $C_{be} \simeq g_m \tau_F$, that is proportional to the bias current. Maximizing the size, hence, does not affect the performances, and it has the advantages of

1. improved matching, that is anyway desirable;

2. reduced base resistance, thus reduced noise contribution.

Regarding the transistors responsible for the phase inversion (Q_{7-10}), they have to be sized together with the load resistors and the switching cell they are going to drive, because all these components affect the resulting switching

delay. The total capacitance connected to the output node results indeed

$$C_L = 2C_{cs,casc} + 2C_{bc,casc} + 2C_{be,switch} + 2C_{bc,switch} + C_{par}.$$

Note that the filtering capacitors at the output of the mixer practically shot-circuit the load resistances at high frequency, making negligible the Miller effect on the HBTs of the switching cell.The bandwidth of the LO driver circuit is therefore approximately

$$f_{LO,driver} = \frac{1}{2\pi R_L C_L}. \tag{3.7}$$

In this situation, since the output offset is going to be compensated through the calibration, it has been preferred to AC couple the driver to the switching cell, since this leaves the freedom to choose the input bias levels independently. The coupling capacitors have been sized in order to make their contribution negligible with respect to the input capacitance of the switching cell, meanwhile avoiding to oversize them, so as to keep as low as possible the parasitics. The contribution of Q_{7-10} to this time constant then results quite small, since the heaviest terms are the base-emitter capacitances and the parasitic ones. Note that the mismatch of these transistors is also quite negligible, because they do not work as differential pairs. At this point, C_L is fixed, so R_L has been chosen to achieve the wanted bandwitdh, and finally the tail current has been set so as to obtain the wanted swing.

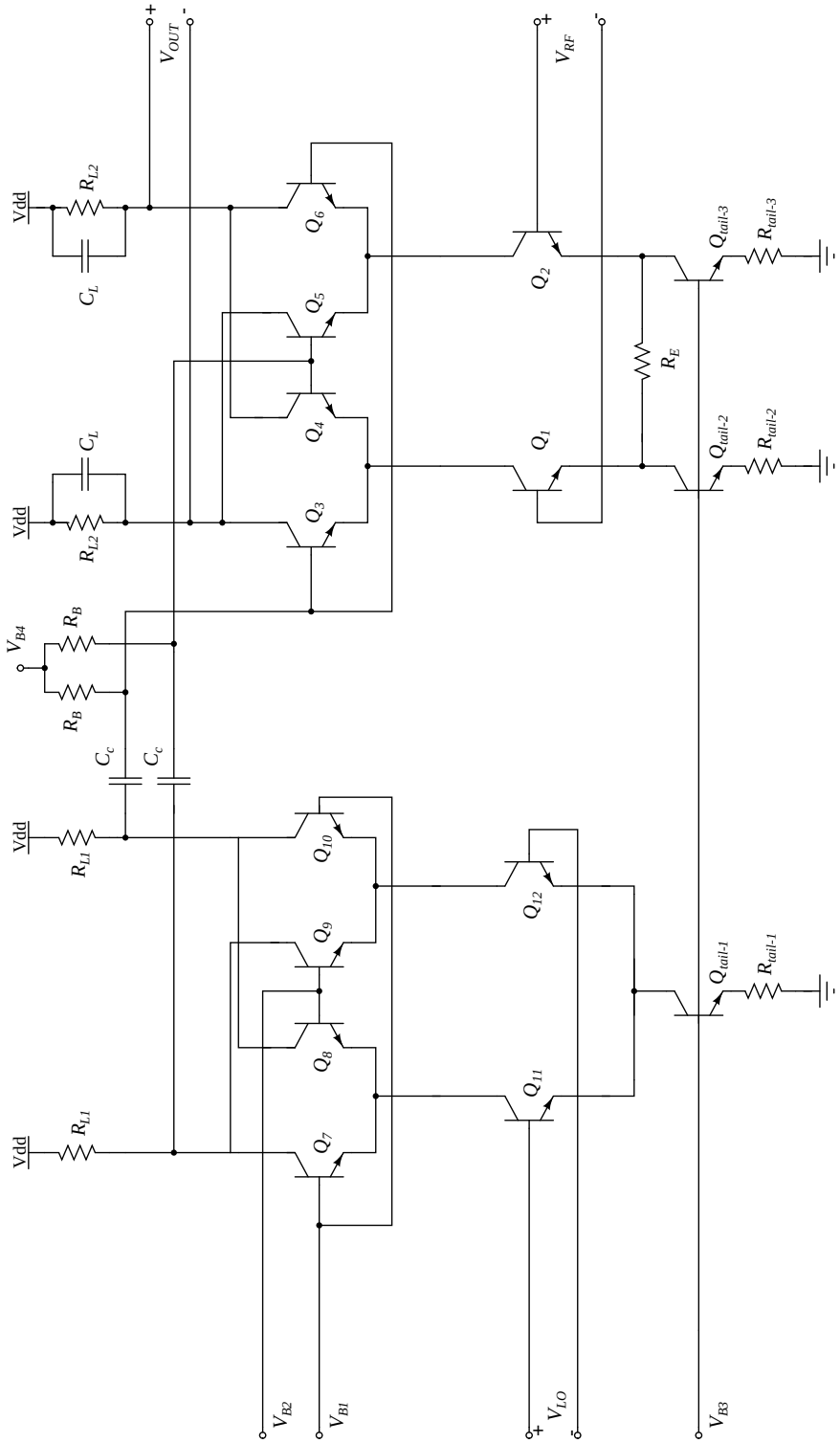
Mixer core The design of the mixer core has followed the same guidelines discussed in section 3.4.1, with some relevant exceptions:

1. the DC input bias of the switching cell can be set independently, thus there is more flexibility to exploit in choosing the DC output common mode;

2. there is no need to size the switching cell as in 3.4.1; in particular it can be avoided the double emitter configuration, which leads to multiple bases, thus to a heavier C_{bc} then the standard configuration.

Leaving apart the phase measurement performances of the LO-swap calibration technique, that will be described in chapter 5, the freedom given by the fact that it is possible to avoid concentrating mostly on the matching gives the possibiliy to optimize the amplitude measurement, whose critical aspect have been highlighted in section 3.4.1. This configuration indeed permits faster

Figure 3.13: Schematic of the Gilbert mixer with LO swap functionality



commutations, thus a behavior closer to ideality than the Gilbert mixer analyzed in the previous section, leading to a lower amplitude measurement error

at $P_{RF,MAX}$.

Tables 3.2 and 3.3 show the chosen component parameters for this version of the Gilbert mixer.

Table 3.2: HBT emitter lenghts.

$l_{E,Q_{1-2}}$ [μm]	$l_{E,Q_{3-6}}$ [μm]	$l_{E,Q_{7-10}}$ [μm]	$l_{E,Q_{11-12}}$ [μm]
$10l_{E,min}$	$4l_{E,min}$	$10l_{E,min}$	$10l_{E,min}$

Table 3.3: Component parameters.

R_{L1}	R_E	R_{L2}	I_{tail1} [mA]	I_{tail2} [mA]
30Ω	75Ω	175Ω	$12mA$	$6mA$

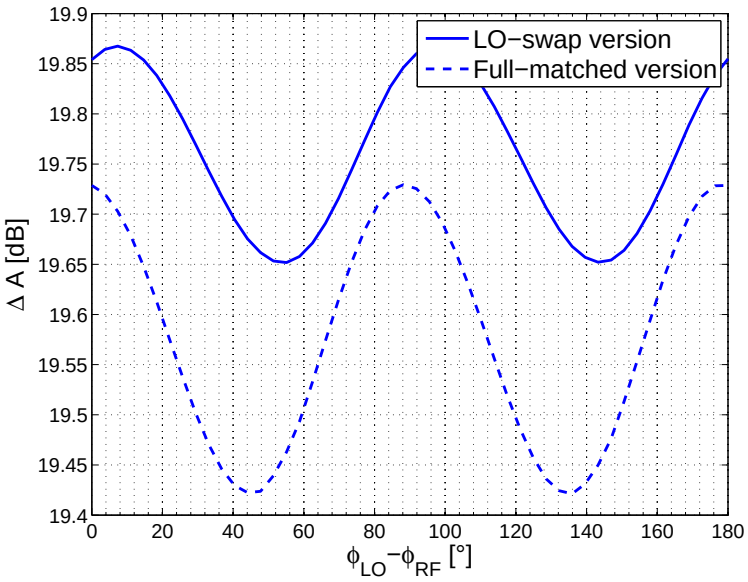
The performances result:

- gain $G_{mix} = 6.7dBV$;
- input-referred 1dB compression point $1dBCP = 5dBm$;
- output common-mode DC voltage $2.4V$;
- $NF_{SSB} < 13dB$ in the white, with a corner frequency $f_{co} \simeq 1kHz$.

As can be observed, with respect to previous version, the current have been boosted with the aim of providing a higher compression point, thus a reduced amplitude error, especially in the case of low supply voltage. The gain, instead, remains roughly the same, like the noise figure and the output common mode. Fig.3.14 shows the ratio of the amplitude measured at $P_{RF,MAX}$ to the one measured at $P_{RF,MIN}$ over the whole phase range, comparing the performance of this mixer and those of the full matching-optimized Gilbert mixer. The simulation has been carried out setting the situation that causes the lowest bias current, hence the lowest linearity for the transconductor. Note that in this situation the matching-optimized mixer displays both bigger error on average and wider deviation of the measured amplitude over the input phase range. Finally, all these advantages come at the price of a slightly increased noise figure, due to the higher currents and degeneration resistor.

Again the apporach to stability has been the one previously described, and the same adopted solutions.

Figure 3.14: Ratio of the ampltidue measured at $P_{RF,MAX}$ to the one at $P_{RF,MIN}$

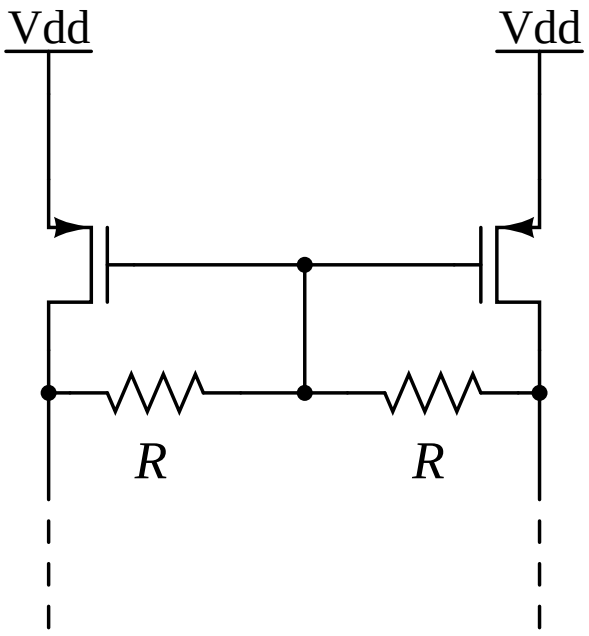


3.4.3 TIA loaded passive mixer

The design of this mixer, introduced in 2.6.1, is somehow more flexible than that of the Gilbert mixer, because it is partitioned into blocks (transconductor, switches and TIA), each with its own bias. It basically re-employs the transconductor discussed in the previous sections to provide voltage to current conversion. The signal current divides between the load of the transconductor and the low impedance offered by the series switches-TIA. For this reason, a high impedance load is desirable for the transconductor, but this cannot be achieved through physical resistors, because it would lead to an excessive voltage drop. A useful solution, in this sense, is the one described in [23], employing self-biased MOS active loads in the configuration shown in Fig.3.15 the bias current flows through the pMOS transistors, while the resistors connected between drain and gate set the load seen by a differential signal. Of course, the active loads need to be properly sized, because the parasitics C_{db} and C_{gd} are also found at the output node, and they could serioulsy compromise the gain at high frequency.

The switching cell is realized through the double-balanced bridge already discussed in the previous chapter, and depicted in Fig.2.13. The LO signal has been boosted through a driver circuit to achieve a swing higher than the one provided by the divider, thus enhancing the conductance provided by the

Figure 3.15: Self-biased active loads for the transconductor



switches. Making the FETs influence negligible is desirable, since their g_{ds} is a source of distortion. The expression of the switch conductance is the following

$$g_{ds} \simeq \mu_n C_{ox} \frac{W}{L} (\hat{V}_{LO} - V_{in,TIA} - V_{th}).$$

The previous formula points out that an increased conductance is possible at the price of

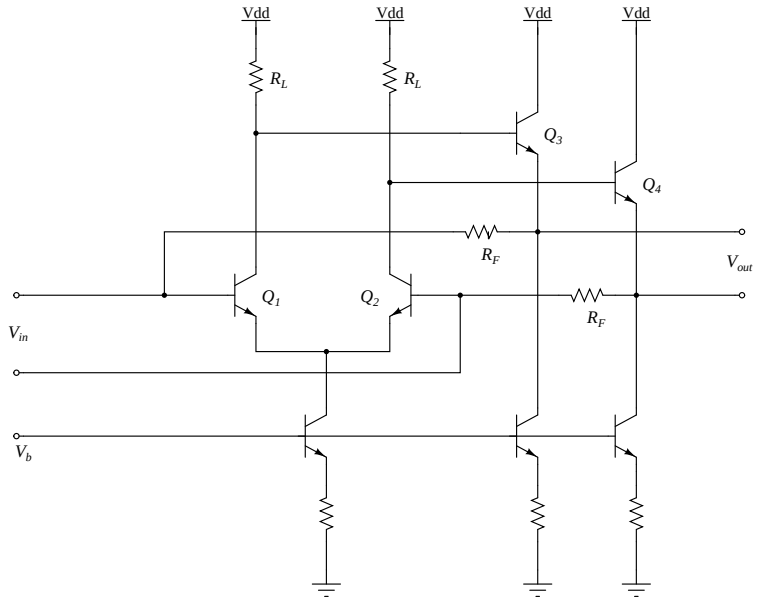
- a stronger LO drive;
- an increased W/L, that causes also an increase in the parasitics of the switches, and might reduce the bandwidth of the driver.

If the employed FETs have the body connected to ground, it is also desirable to provide the TIA with an input common mode as low as possible, to minimize the body effect. The employed driver circuit is very similar to the one presented for the Gilbert mixer with LO-swap functionality, and it is not going to be discussed again here. The main difference consists in the higher swing it needs to provide, that has been set to $\simeq 800mV$, while the switches has been biased very close to the threshold, in order to make them switch very readily.

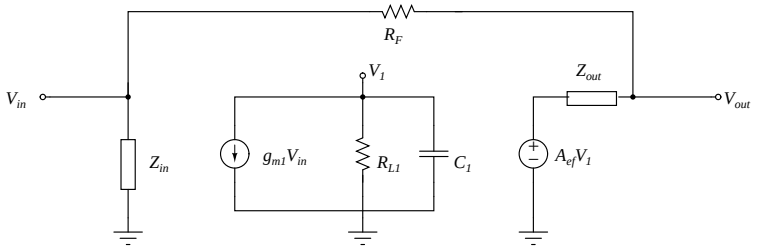
To carry out a comparison with the Gilbert mixer implementation, it has been designed a TIA fully optimized in terms of matching, since this stage is

the one that mainly influences the output offset. The TIA has been realized in a very simple form using a buffered differential amplifier as the gain stage, with a resistive feedback that allows to get a low input impedance. It is worth pointing out that this is not the best solution to get a low input common mode, but it has been adopted mainly for its simplicity, with the idea that a low number of well-matched components likely leads to an overall low offset. Such a configuration is shown in Fig.3.16a, with an output buffer that gives robustness with respect to loading effects, and help lowering the common mode input-output voltage. The single-ended small signal equivalent circuit is reported in Fig.3.16b, where A_{ef} represents the gain of the emitter-follower stage, and C_1 the capacitance at its input node. It represents an amplifier with shunt-shunt feedback, thus its loop gain needs to be analyzed to detect an eventual instability, and characterize its performances. The parameters of the feedback

Figure 3.16: Transimpedance amplifier



(a) Schematic



(b) Single-ended small signal circuit

result:

$$A_{OL} = -\frac{R_F//R_{in}}{1+sR_F//R_{in}C_{in}} \cdot \frac{g_m R_1}{1+sR_{L1}C_1} \cdot A_{ef}(s)$$

$$\beta = -\frac{1}{R_F}$$

where $A_{ef}(s)$ exhibits a (dominant) pole approximately at $\omega_{p,ef} = \frac{g_{m,ef}}{C_{be}+C_L}$. The input impedance and the transimpedance, at low frequency, are reported as follows:

$$Z_{in,TIA} \simeq \frac{R_F}{1+g_{m1}R_{L1}} \cdot \frac{1}{1+s\frac{C_{in}R_F}{1+g_{m1}R_{L1}}}$$

$$Z_{TIA} \simeq -R_F \frac{g_{m1}R_{L1}}{1+g_{m1}R_{L1}} \cdot \frac{1}{1+s\frac{R_F C_{in}}{1+g_{m1}R_{L1}}}.$$

To obtain performances comparable to the Gilbert mixers, R_F has been set to a value of 200Ω. The target gain for the amplifier is $20dB$, so as to achieve an input impedance of less than 20Ω. In this situation, the system is easily stable with a phase margin close to 90°, because the term $R_F C_{in}$ dominates over the other poles, also thanks to the Miller effect that enhances the input capacitance. The proposed circuit has been realized both with bipolars and MOSFETs to compare the offset statistics. Note that the offset error introduced by the buffer undergoes an attenuation equal to the loop gain, because it can be modeled like an error that sums to the signal after the gain element. On the contrary, the differential pair offset errors does not suffer such an attenuation, and in particular, the current offset is amplified by the transimpedance of the stage. The current offset can be calculated as the difference between the base currents when the input is left opened

$$I_{OS} = \frac{I_{C1}}{\beta_{F1}} - \frac{I_{C2}}{\beta_{F2}}$$

that, under the hypothesis of small deviations of the parameters from the ideality, leads to[1]

$$I_{OS} = \frac{I_C}{\beta_F} \cdot \Big(\frac{\Delta\beta_F}{\beta_F} + \frac{\Delta R}{R_C}\Big).$$

The previous result highlights that, for example, if the resistors and beta mismatch sum to a 20% overall deviation, the offset current would be approximately $0.2I_B$, and the output offset $V_{OS,out} \simeq 0.2R_F I_B$. To obtain good performances with this mixer, it is therefore convenient to employ well-matched differential pair and load resistors, possibly avoiding high biasing currents, or

[1] See [13] for the complete analysis.

skipping the problem using a FET pair.

The nominal performances for this mixer are result:

- gain $G_{mix} = 7.2dBV$;
- input-referred 1dB compression point $1dBCP = 3dBm$;
- input-output common-mode DC voltage $1.5V$;
- $NF_{SSB} \simeq 11dB$ in the white, with a corner frequency $f_{co} \simeq 10kHz$ (bipolar TIA version).

Therefore, this kind of mixer provides performances comparable to the Gilbert mixer, in terms of gain and linearity. The noise figure at high frequency assumes a comparable value as well, but the corner frequency results higher.

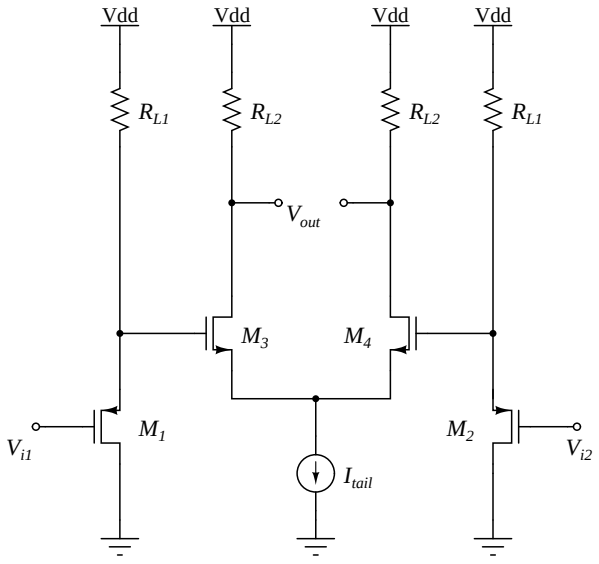
3.4.4 Passive voltage-mode mixer

As pointed out in the previous chapter, this mixer is not suitable to the aims of this work because of its attenuation. Employing a pre-amplifier, on the other hand, is not an effective solution, because the compression would bound the dynamic range preventing the structure to meet specifications. One possible solution, then, is to put an amplifier after the mixer, like the solution proposed in [5]. This is not a great idea in terms of noise, since the noise produced by the switches is amplified as well. However, noise is not a main concern in this situation, and it has been considered worth trying to investigate this solution, so as to have a further comparison with the Gilbert mixer performances.

The employed amplifier is composed of a couple of pMOS source followers that work with a zero input common mode, followed by a differential amplifier providing the desired gain, as shown in the principle schematic of Fig.3.17. Note that in this case the mismatch of both the source followers and the differential pair contribute to the output offset. On the other hand, the size of the MOSFETs composing this stage can be increased as long as the equivalent load capacitance cause negligible current absorption from the input buffer, because, as demonstrated in [19], the effect of load capacitance on the mixer gain is simply the one of a single-pole filter applied after mixing, hence it cause no effect on the gain of the structure. The switching cell, introduced in the previous chapter, has been designed in a way similar to the one of the TIA loaded mixer. To reduce the distortion arising from the non-linear conductance of the switches and the modulation of the switching times due to the RF

leakage, it has been re-used the LO driver circuit already mentioned, that provides a strong overdrive with steep commutations. The size of the switches, as well, has been chosen to enhance the conductance without compromising the bandwidth of the driver.

Figure 3.17: Amplifier with level shifter employed with the passive mixer



The nominal performances for this mixer, provided with the output amplifier result:

- gain $G_{mix} = 7.4dBV$;
- input-referred 1dB compression point $1dBCP \simeq 5dBm$;
- output common-mode DC voltage $1.12V$;
- $NF_{SSB} \simeq 19.5dB$ in the white, with a corner frequency $f_{co} > 10kHz$.

Again, gain and linearity are not an issue, being comparable to the performances of the other mixers. The noise figure, instead result much worse, as expected.

3.4.5 Output offset comparison

In this last section the performances in terms of offset between the different solutions are compared. The circuits have been simulated in a set of Monte Carlo analysis, with no RF input applied in order to take into account the

contributions to the offset of the output stages, where employed, and other possible sources of error, like self-mixing. The results of this test are reported in table 3.4 Clearly, the best performances are offered by the Gilbert mixers.

Table 3.4: Simulated std.dev. of the output offset in the different mixers.

Mixer version	$\sigma_{V_{OS}}[mV]$
Matching optimized Gilbert mixer	0.75
Gilbert mixer+LO-swap	1.4
TIA loaded mixer: bipolar TIA	1.7
TIA loaded mixer: MOS TIA	3.2
Passive mixer+amplifier	5.7

This is not surprising, since in that realization there is no output stage, and, recalling (2.11), a good matching between the switches and the load resistors provides a low offset even if the transconductor is mismatched, thanks to the double balanced topology. A further comment on the latter two types of mixers: the TIA loaded mixer is definitely not suitable to this kind of application, at least with this technology. Though it provides good performances with a well-matched TIA, this comes at the price of one more stage, with respect to Gilbert mixer, without any other advantage, nor in terms of power consumption, since it requires a transconductor and a LO driver circuit, nor about area, since, without accounting for the space occupied by the TIA, it employs one more pair of coupling capacitors to connect the transconductor to the switches. The passive voltage-mode mixer, instead, is being penalized by the output stage, that cannot be avoided because of its insufficient gain. On the other hand, it is a simple circuit, with few components, and few sources of error, which has a very low power consumption, if compared to the other ones, and it is likely not more area consuming. For these reasons, it should be taken into account in possible different realizations.

The bipolar Gilbert mixer provided with LO-swap functionality for offset compensation is the version chosen for layouting, since as will be clarified in the results chapter, it is the one providing the best results and meets all the specifications.

3.5 Buffers

This section deals with the design of the buffers, that are key blocks, not less important than the mixers and the divider. The design goals are different

depending on the function of the buffer. In particular:

- the RF buffer must not distort the input signal, and it needs to provide (ideally) no attenuation and impedance matching over the input wide band;
- the divider buffer does not need to be as linear as the RF buffer, but it needs enough bandwidth to drive the divider input up to twice the maximum RF frequency, meanwhile providing impedance matching;
- the divider output buffers (in the following discussion indicated as 'LO buffers') have to display a high input impedance so as to avoid loading effects on the divider, and they need a high bandwidth to provide quick commutations.

Each of these buffer stage, therefore, has been specifically designed to meet the mentioned requirements. The next paragraphs describe in detail the design flow and the related aspects.

3.5.1 Emitter follower buffers

It is customary to use these circuits to separate a low output impedance stage from the following, high input impedance one, because they effectively work like voltage buffers. The general schematic of an EF is reported in Fig.3.18, where it is shown that the bases of the EF HBTs are directly driven by the input signal, while the emitters are connected to the output.

Intuitively, due to the exponential characteristic of the bipolar transistor, that makes the base-emitter voltage practically constant with respect to large variations of the current, even if the buffer is driving a load, the potential at the emitter will follow the one applied to the base, just being shifted of V_{be}. Therefore, the differential output voltage should ideally replicate the differential input one.

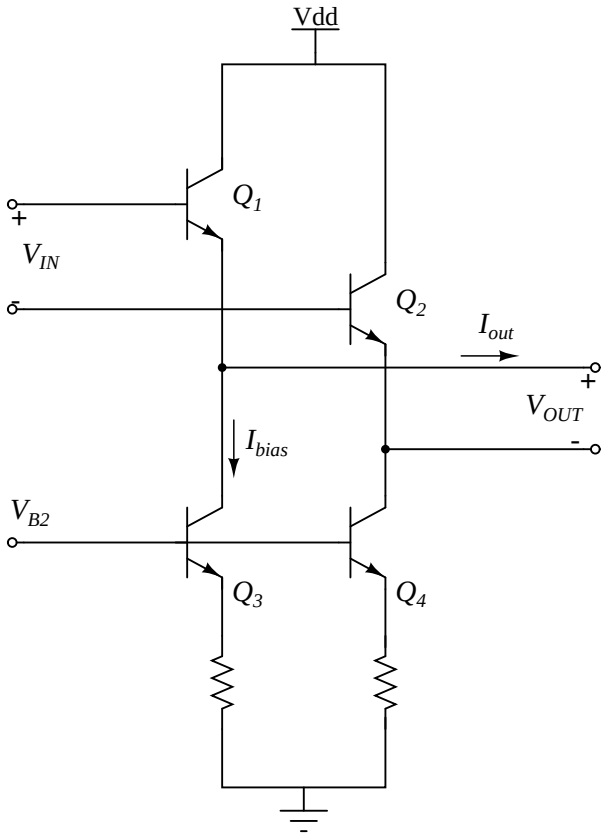
Of course, this is not true in practice, from more than one standpoint. First of all, considering just DC values, it is easy to characterize the effect of loading: labeling with I_{bias} the DC current provided by the mirrors, and i_{out} the output current, then

$$I_{bias} + i_{out} = I_S \cdot e^{\frac{V_{be}}{nV_T}}$$

which leads to

$$V_{be} = nV_T \cdot ln\Big(\frac{I_{bias} + i_{out}}{I_S}\Big).$$

Figure 3.18: Schematic of an EF buffer (biasing not shown).



Therefore, the input-output characteristic results

$$V_{out} = V_{in} - nV_T \cdot ln\Big(\frac{I_{bias} + i_{out}}{I_S}\Big) \tag{3.8}$$

that is a non-linear equation, and gives a first insight on the performances of such a device. Indeed, assuming i_{out} to be negligible with respect to the biasing term, then the relation is linear since the offset term is constant. Hence, to design an emitter follower with good linearity performances, it is necessary to know at least the order of magnitude of the load to be driven. Naturally, such an argument holds only if the transistors keep working in the active region, thus the operating point needs to be chosen carefully to make sure that even with the most powerful applied signal saturation does not occur.

The other features of this configuration can be better understood through a small-signal analysis, carried out considering a resistive-capacitive load. The

low-frequency behavior of the EF stage is described by its gain

$$A_V \simeq \frac{g_m R_L}{1 + g_m R_L} \cdot \frac{1 + s\frac{C_{be}}{g_m}}{1 + s\frac{C_L + C_{be}}{g_m}}.$$

The previous expression highlights that the bandwidth is set by term $\omega_{buffer} = \frac{g_m}{C_L + C_{be}}$, thus if the load to drive displays a strongly capacitive input impedance, a high bias current will be needed not only for linearity purposes, but also to make the buffer fast enough. From the same analysis other results need to be taken into account, first of all the input impedance

$$Z'_{in} \simeq r_b + g_m r_\pi R_L \cdot \frac{1 + s\frac{C_L + C_{be}}{g_m}}{1 + s(r_\pi C_{be}) + s^2 r_\pi R_L C_L C_{be}}$$

$$Z_{in} = r_b + Z'_{in} // \frac{1}{sC_{bc}}$$

r_b being the parasitic base resistance. A plot of this function using realistic values for the involved parameters is reported in Fig.3.19, where it can be observed that at high frequencies the magnitude of the impedance drops at values of few $k\Omega$, and the phase widely exceeds $-90°$, that means the buffer tends to show an input impedance with negative real part, in a certain range of frequencies. Indeed, neglecting the resistive components, the expression of Z'_{in} becomes

$$Z'_{in} = \frac{1}{sC_L} + \frac{1}{sC_{be}} + \frac{g_m}{s^2 C_L C_{be}}$$

where the term $\frac{g_m}{s^2 C_L C_{be}}$ accounts for the negative resistance. As already discussed, this condition is to be avoided to ensure the absence of oscillation in any case, thus some attention must be paid in the design.

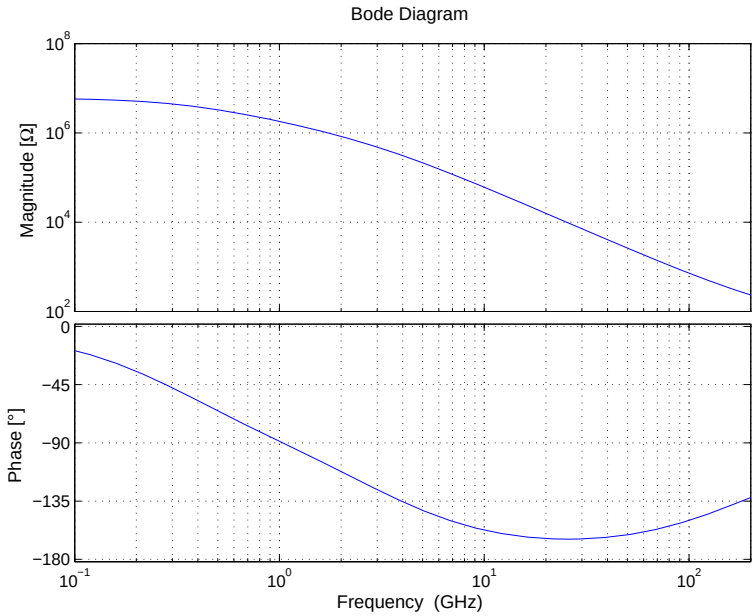
The output impedance, instead results

$$Z_{out} \simeq \frac{1 + s r_b C_{be}}{g_m + s C_{be}} \tag{3.9}$$

which is mainly inductive in a wide range of frequencies.

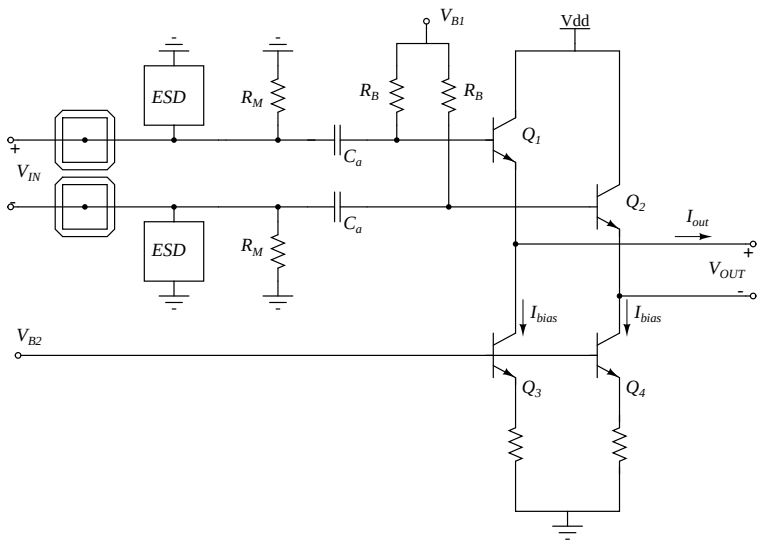
To obtain impedance matching, a configuration like the one depicted in Fig.3.20 is employed, with two matching resistors terminating to ground, that provides input matching for the common-mode signals also, and fixes the operating point of the inputs to ground. The picture highlights also the presence of the pads and the ESD (electrostatic discharge) protections, because these components introduce further capacitance that adds to the input, degrading

Figure 3.19: Magnitude and phase of the input impedance of an EF.



the reflection coefficient. As discussed in chapter 1, the upper bound usually

Figure 3.20: Schematic of a buffer providing impedance matching.



set for the $|S_{11}|$ desired at the interfaces of the circuit is $-10dB$.

Regarding the noise issue, in this case the main contribution are due to the emitter followers, the eventual input matching networks and the compensation resistors. Since the EF sizes are going to be maximized for matching reasons, what can be done to limit the noise produced by the buffer is avoiding excessive

biasing currents (recall the expressions derived in 3.4.1), that is also useful from other standpoints, as it is explained in the following sections.

3.5.2 RF buffer

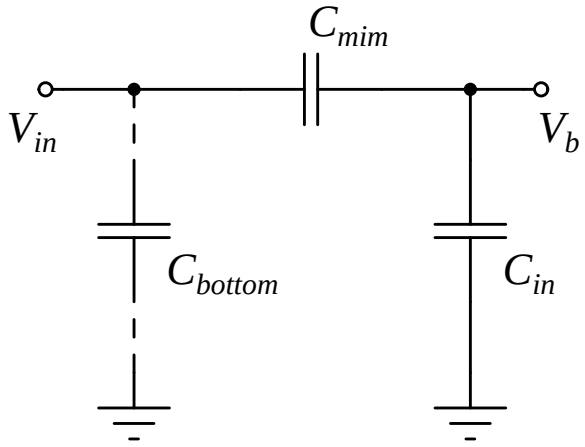
To match the objectives presented at the beginning of this section, the RF buffer needs a biasing sufficient to provide good linearity when the maximum input power is applied, and a suitable bandwidth. Moreover, the HBTs should not cause excessive input parasitic capacitance, because to minimize the impact on the S_{11}. From this perspective, care should be taken in the choice of the coupling capacitors, because they also add up input capacitance, and the ESD protection devices as well.

Taking into account the equivalent input capacitance exhibited at high frequency by the *two* transconductors the buffer drives, it is possible to estimate the maximum current absorbed, and thus, recalling (3.8) to set a lower bound for the bias current needed. Power consumption is not an issue in this work, but on the other hand, excessive biasing leads to the need for big transistors and large metal connections, that in turn means more parasitics due to the layout.

A compromise value has been found in the value of $I_{bias} = 6mA$, that provides a bandwidth of $BW \simeq 91GHz$, meanwhile guaranteeing a negligible distortion, even at $P_{RF,MAX}$.

The coupling capacitors have to be sized in order to be transparent to the signal, meanwhile avoiding to add excessive parasitic capacitance through the parasitics. The employed MIM (Metal-Insulator-Metal) capacitors, realized exploiting two adjacent levels of metal separated by an insulating film, are characterized mainly by a bottom parasitic towards the substrate that depends both on the area and the perimeter of the capacitor itself. To minimize this contribution it is convenient to set the capacitor so as it is composed of squared blocks, because this minimizes both the area and the perimeter contribution. Imagining that, at high frequency, the impedance displayed by the stage at the input is mainly given by the transistor parasitic, the input circuit becomes a capacitive divider, as displayed in Fig.3.21. It is straightforward that, to maximize the signal at the base, the best solution is to connect the top of the MIM capacitor at the base, so that the bottom parasitic does not get involved in the division. A suitable value for the MIM capacitor has been found to be $C_c = 1.5pF$, that in this configuration produce a negligible signal loss on the input divider circuit.

Figure 3.21: Simplified input circuit with the capacitor parasitic.



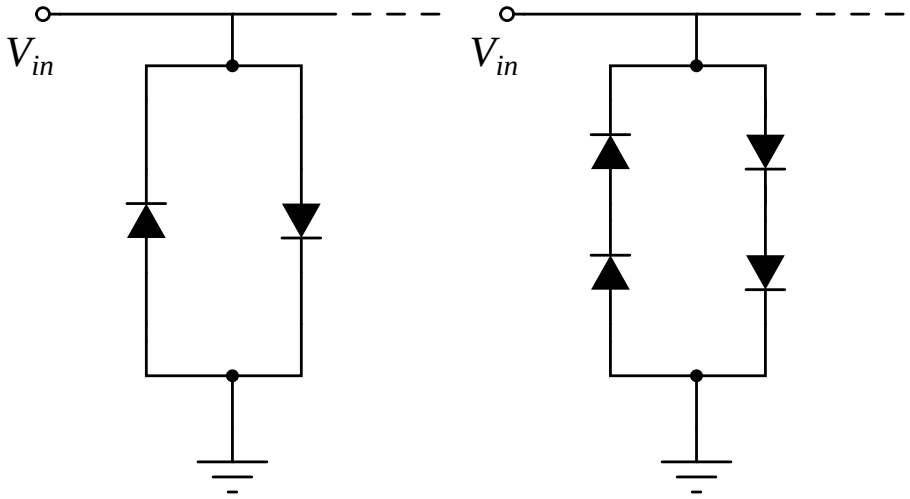
This buffer needs to provide impedance matching. The input impedance, at low frequency is set by the matching resistor terminated to ground, but as the frequency grow, the capacitive effect gain influence. This capacitance is given by the sum of the base-collector capacitance due to EFs, the MIM parasitic, and the ESD parasitic:

$$C_{in} = C_{bc} + C_{bottom} + C_{ESD}.$$

The ESD protection is usually realized through diodes that switch on if the input voltage goes over a certain value, shorting the line to the supply, or to ground. Since the input common-mode here is zero, a suitable solution is shown in Fig.3.22. In both of these cases the capacitance contribution is due to the junction capacitance associated to the depletion region in the diodes, and it is proportional to the size of the devices, so a good starting point is to choose the minimal one. If the parasitic is still excessive, then the configuration of Fig.3.22b helps reducing it, since the total capacitance is the series of the parasitics from the two diodes.

Regarding the stability issue, as anticipated the EF buffer in particular situations might oscillate, and also in this case the aim is to obtain unconditional stability. To achieve this goal, there exist different techniques, some of which rely on particular choices of the collector current densities (see [14] p.715), but in this case the size of the HBTs will be maximized to obtain the best matching, so the current density is going to be quite low. In the particular case of the RF buffer, the input impedance is matched, and tends to

Figure 3.22: ESD diode configurations.



become capacitive at high frequency, due to the parasitic loading at the input, and independently from the load impedance. The output impedance, recalling (3.9), might exhibit negative real part for example in the presence of an inductive source impedance, that is likely the case of a long input line. A simple way to overcome the problem is to simply put a few resistance in front of the bases, which push to higher frequencies the inductive effect, helping to keep the wanted output impedance up to some hundreds of GHz. It is also useful to add some resistance in series to the output lines, for the same reason, paying attention to its effect on the gain.

3.5.3 Divider buffer

The design of this block has focused on the need for good matching, to feed the divider with the smallest possible offset, meanwhile providing a suitable impedance matching up to *twice* the maximum RF frequency.

First of all, the matching issue is addressed. To properly design the buffer for this purpose it is necessary to understand how the various parameters affect the performances. Recalling the structure of Fig.3.20, and labeling with R_{B1} and R_{B2} the resistors biasing respectively Q_1 and Q_2, the KVL applied at the input loop gives

$$V_{OS} = -V_{be1} - R_{B1}I_{b1} + R_{B2}I_{b2} + V_{be2}$$

that, supposing small deviations of the parameters from the nominal values,

becomes

$$\begin{aligned} V_{OS} =& nV_T\left(\frac{1-\frac{\Delta I_c}{2I_c}}{1+\frac{\Delta I_c}{2I_c}}\cdot\frac{1-\frac{\Delta A_e}{2A_e}}{1+\frac{\Delta A_e}{2A_e}}\cdot\frac{1+\frac{\Delta Q_B}{2Q_B}}{1-\frac{\Delta Q_B}{2Q_B}}\right) \\ &+ R_B\frac{I_c}{\beta}\left[\frac{1+\frac{\Delta I_c}{2I_c}}{1+\frac{\Delta\beta}{2\beta}}-\frac{1-\frac{\Delta I_c}{2I_c}}{1-\frac{\Delta\beta}{2\beta}}\right] \\ &+ \frac{\Delta R_B}{2}\left[\frac{1+\frac{\Delta I_c}{2I_c}}{1+\frac{\Delta\beta}{2\beta}}+\frac{1-\frac{\Delta I_c}{2I_c}}{1-\frac{\Delta\beta}{2\beta}}\right] \end{aligned} \tag{3.10}$$

and, neglecting the higher order terms finally gives

$$V_{OS} = nV_T\Big(-\frac{\Delta I_c}{I_c}-\frac{\Delta A_e}{A_e}+\frac{\Delta Q_B}{Q_B}\Big)+\frac{I_c}{\beta}\Big[R_B\Big(\frac{\Delta I_c}{I_c}-\frac{\Delta\beta}{\beta}\Big)+\Delta R_B\Big]. \tag{3.11}$$

This result rises two considerations:

1. the offset of the buffer is enhanced by the mismatch between the emitter followers, through the mismatch of emitter areas and current gains. The β mismatch is emphasized by the drop on the biasing resistors;

2. the offset is also influenced by the collector currents mismatch, but while increasing the collector current helps reducing the mismatch between the base-emitter voltages, on the other hand it increases the weight of biasing resistors and beta mismatch.

Taking into account these reasons, the following design guidelines have been adopted:

1. the emitter followers give the best performances when the maximum size is chosen;

2. the collector current should not exceed the value needed to obtain the desired bandwidth;

3. the biasing resistors can be oversized for improved matching, as long as the parasitics are not a concern.

4. the size of the tail generators does not need to be maximized, because their local feedback attenuates the effect of the mismatch, thus they weakly contribute to the overall offset.

Table 3.5 summarizes the results for the buffer offset and the corresponding quadrature error, obtained by sweeping the size of the EFs and the magnitude

of the bias current. It has been used the optimized divider, as explained in section 3.3, and the tests have been conducted imposing nominal supply voltage and maximum operating temperature (the worst case for the divider). As predicted, by increasing the current both offset and quad error worsen, even if the latter increases less dramatically, because current enhancement leads to bandwidth enhancement, hence steeper commutations and reduced effect of the mismatches. The choice of $I_{bias} = 6mA$ also in this case has been

Table 3.5: Simulated std.dev. of the output offset in the different mixers.

$I_c[mA]$	l_e	$\sigma_{V_{OS}}[mV]$	$\sigma_{\phi err}[^\circ]$
2	$4l_{e,min}$	1.63	0.55
	$6l_{e,min}$	1.3	0.43
	$8l_{e,min}$	1.09	0.4
	$10l_{e,min}$	0.96	0.38
4	$4l_{e,min}$	2.47	0.65
	$6l_{e,min}$	1.7	0.48
	$8l_{e,min}$	1.38	0.41
	$10l_{e,min}$	1.18	0.38
6	$4l_{e,min}$	4.3	1.09
	$6l_{e,min}$	2.69	0.71
	$8l_{e,min}$	2	0.56
	$10l_{e,min}$	1.62	0.42
8	$4l_{e,min}$	6.92	1.61
	$6l_{e,min}$	4.24	0.99
	$8l_{e,min}$	3.08	0.73
	$10l_{e,min}$	2.45	0.6

considered an acceptable compromise, while the size of the EFs has been set to the maximum $l_e = 10l_{e,min}$.

The impedance matching issue, in this case, has to be evaluated more carefully, considered the high frequency of operation this block has to reach. The coupling capacitors do not need to be sized to maximize the signal transferred to the bases, on the contrary they have to provide the least possible parasitic capacitance. It has been found that, for this buffer, a value of $C_c = 300fF$ is suitable. In conjunction, the ESD configuration of Fig.3.22b is employed, and following the same idea, the single-base configuration is chosen for the EFs, to minimize the contribution of the base-collector capacitances.

The buffer has been provided with series resistor on the input and output lines, like the RF one, to make the interfaces of this block unconditionally stable.

3.5.4 LO buffers

As anticipated in section 3.3, these buffers decouple the divider from the switching cell, or the LO driver of the mixer, to provide less loading capacitance, and level shifting in the case of the DC coupled mixer.

These buffers need a high bandwidth and a good matching, to provide fast commutations and avoiding introduce further errors. Indeed, ideally the only capacitive contribution they add is due to the base-collector capacitances, that are usually much lower than the input capacitance of a differential pair. Note that, recalling (3.11), and since the bases of the EFs are directly connected to the outputs of the divider, in this case the impact of the terms R_B is much lighter, because they are represented by the load resistors of the divider $R_L = 45\Omega$, differently from the other buffers, where high biasing resistances are employed, in order to make them negligible from the input signal standpoint. These load resistors are naturally well-matched, because they need to stand a high current, so their sizing is bounded by the Joule heating. Therefore the matching issue for these EFs is less critical, and to provide the best performances they have been sized with maximum emitter length, while the double emitter configuration has been chosen.

The others issues have been faced in a way similar to the other buffer stages, in particular:

1. the tail current generators, have been set at the minimum possible size to avoid unuseful capacitive loading;
2. the bias current has been set at $I_{bias} = 6mA$, because this provides enough bandwidth for quick switching;
3. series resistors have been provided at the outputs to get unconditional stability at every operating condition.

3.6 Bias and Enable circuits

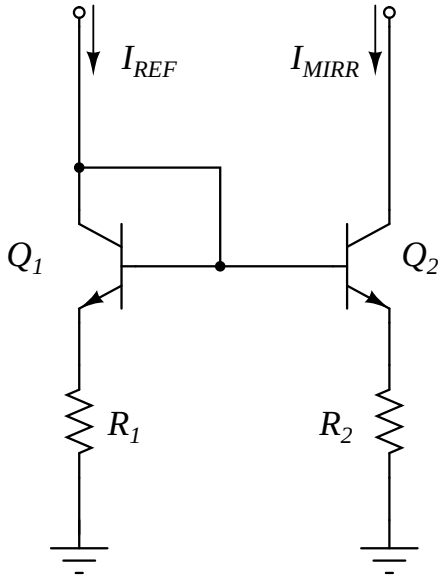
All the described stages are current-biased, and since the performances of the HBTs depend mainly on their collector current, it is important to design a reliable biasing circuit. Basically, the simplest way to accomplish this task, is to generate a reference current and replicate it where needed through current mirrors. A current mirror in bipolar technology usually looks like the one depicted in Fig. 3.23, where the reference current flows through a diode-connected transistor that shares its base voltage with the HBT of the mirrored

branch. Applying the KVL to the loop composed by the base-emitter and the degeneration resistors, it is readily found the following relation:

$$I_{MIRR} = \frac{1}{R_2} \cdot \left[R_1 I_{REF} + nV_T ln\left(\frac{I_{REF}}{I_{MIRR}} \cdot \frac{I_{S2}}{I_{S1}} \right) \right]. \tag{3.12}$$

This is a transcendental equation that does not have a closed form solution,

Figure 3.23: Schematic of a bipolar current mirror.



but it is easy to understand what happens. If the desired mirrored current is N times I_{REF}, then the emitter areas of the HBTs should be set in order to match $A_{e2} = NA_{e1}$, and the resistors $R_2 = \frac{R_1}{N}$. In this situation, if the ratio $\frac{I_{MIRR}}{I_{REF}}$ exceeds N, then equation (3.12) gives that the logarithmic term will subtract to the other one, reducing thereby I_{MIRR}, and if the ratio is less than N the logarithmic term will increase the current. It is intuitive that, at the equilibrium, $I_{MIRR} = \frac{R_1}{R_2} \cdot I_{REF} = N \cdot I_{REF}$.

The degeneration resistors at a first look do not seem necessary, as they are usually not employed in MOS current mirrors, but they provide some desirable properties that are listed as follows:

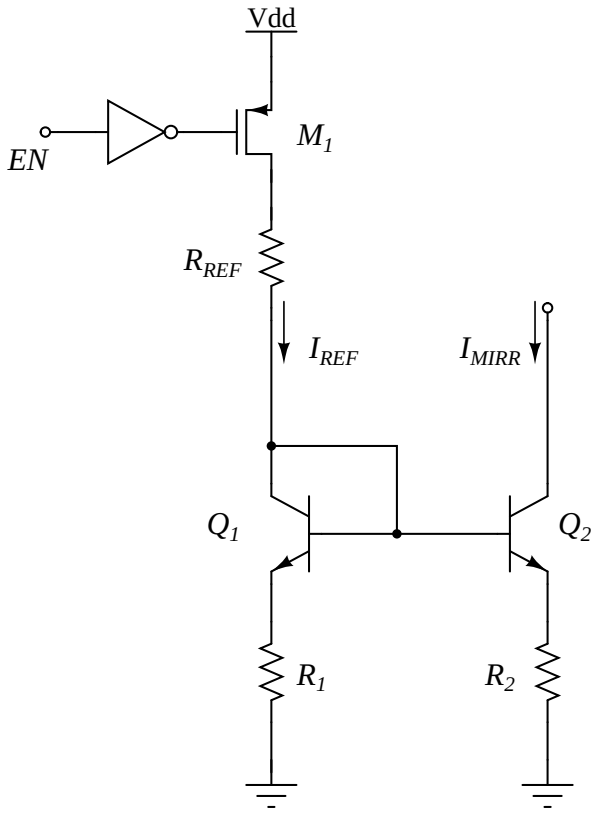
1. they introduce a local series-shunt feedback, that improves the output resistance of a factor equal to the loop gain;

2. they reduce the system sensitivity to errors such as mismatch, again thanks to the feedback;

3. they help making the mirror unconditionally stable, which can be verified looking at the small-signal input-output impedances in the two cases.

4. they reduce the sensitivity to layout parasitics wiring both emitters.

Figure 3.24: Schematic of a bipolar current mirror complete with the enable feature.



All of these advantages come at the price of a reduced output swing, since the mirror behaves as an ideal current generator as long as the potential at the output node keeps higher than $R_2 I_{MIRR} + V_{ce,sat}$. If this bound is not acceptable, a MOS current mirror can be employed, since the minimum voltage thereby reachable can be much lower. In this work, anyway, it has not been necessary to employ FET mirrors.

The detector is a device that has to be employed for test purposes, and during the normal operation of the overall system it is switched off. Hence, the different blocks composing the detector need to be provided with an enable circuit that allows to turn them on when the device is employed. Such a circuit must be able to perform this task being driven by a logic input, here indicated as EN.

To get this functionality, a pMOS transistor driven by an inverter is plugged between the power supply and the reference branch of each current mirror, as shown in Fig.3.24. This way, when the EN input is low, the gate of the pMOS is pulled at V_{dd}, thus turning it off, and when EN is low, the pMOS is turned, allowing the reference current to flow. Of course, the FET has to be sized so as it works in deep triode region, displaying the smallest possible drain-source resistance.

Chapter 4

Layout

This chapter describes the guidelines followed to produce the layout of the circuit blocks, and finally of the test chip. The layout is a very delicate step in the design flow, mostly regarding the RF circuits. In fact the physical realization of the circuit introduces resistive, capacitive and inductive parasitic components, that influence the circuit in different ways: in the worst cases, the performances could be seriously degraded, or the circuit could even become unstable. For these reasons, it is important to rely on a robust design, and it is useful to take into account the possible effects of the parasitics even before reaching the layout phase. Of course, this is also a matter of experience. Sometimes, layout problems lead to step back to the design phase, because unexpected issues show up. Regarding this work, this has happened in the case of the divider buffer, where the parasitic input capacitance due to the metal connections, the pads, an the ESD protections, forced a review of the design of this block, in order to guarantee a proper impedance matching up to the wanted frequencies.

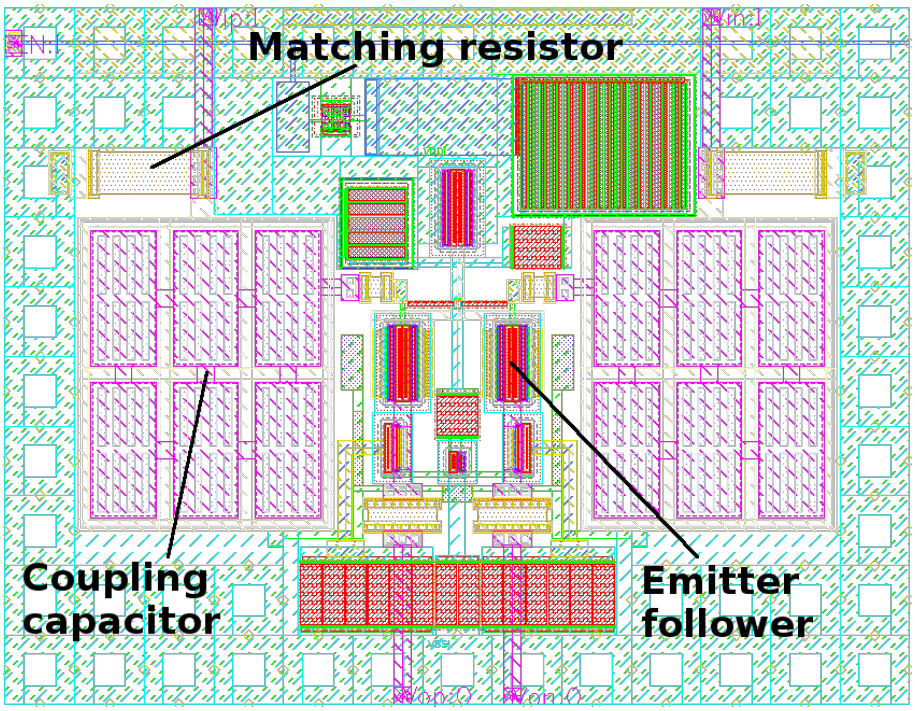
Generally speaking, the following ”rules” should be considered when realizing a layout:

- metal paths and vias, like transistors and resistors, are subjected to DC and RMS current limitations, and must be properly sized as well;
- long metal paths imply considerable inductive parasitics;
- metal layers are subjected to parasitic capacitance towards the substrate: the usage of metal levels close to the substrate implies higher parasitic capacitance than the upper levels;
- crossings between two paths involve parasitic capacitances between them,

related to the area of the metals facing each other. When needed, shields connected to ground can be employed to relieve this effect;

- thin metal connections involve smaller capacitive parasitics, but higher resistance: depending on the situation it has to be decided which contribution is heavier and should be reduced;
- in the paths through which the RF signal travels, 90° bends should be avoided whenever possible;
- differential circuits should be as symmetrical as possible;
- for the reason just mentioned, in differential circuits, signals should travel through similar paths, and loading contributions due to parasitics should be as symmetrical as possible;
- to get more simmetry, dummy components and metal strips are effectively used to intentionally introduce symmetrical parasitics.

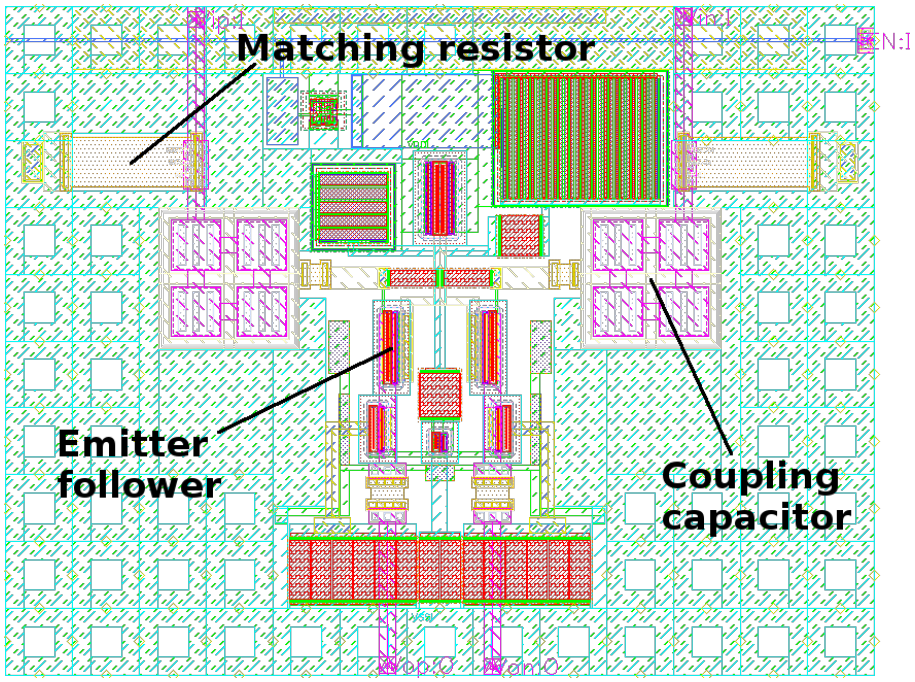
Figure 4.1: Layout of the RF buffer (130μm x 100μm).



RF buffer Fig.4.1 shows the layout of this circuit, where it is evident the presence of the big coupling capacitors (1.5pF), the matching resistors and

the enable pMOS. After the EFs, the path towards the output has been realized through a straight metal strip, to make the path as short as possible, and employing the thinnest possible metal strip, to reduce the capacitance. The layout has been realized to enhance the symmetry, employing mirrored branches, with the bias circuit in the middle.

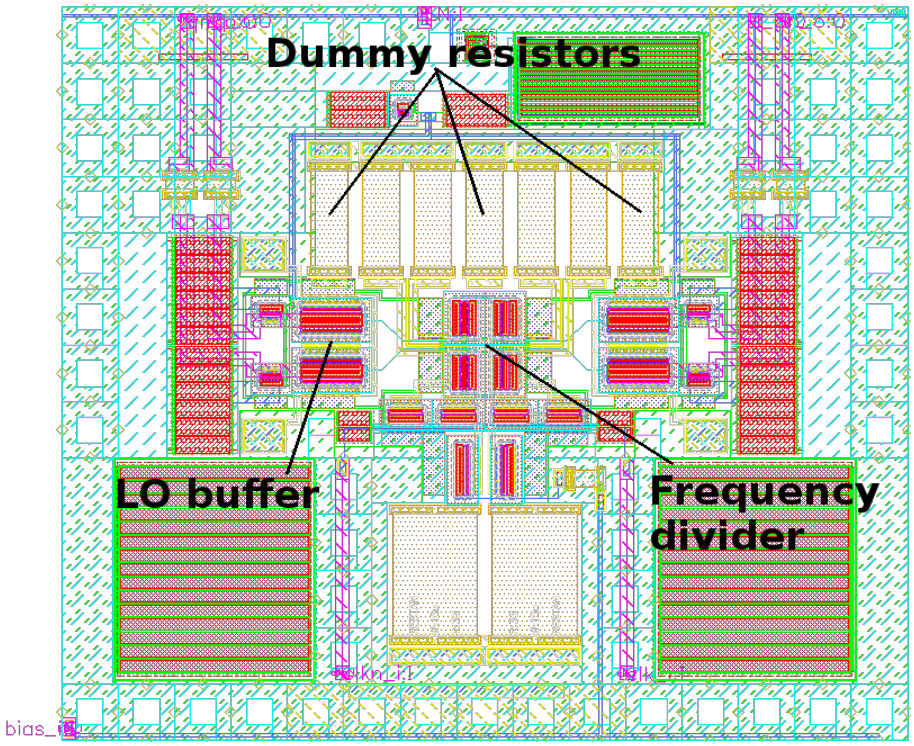
Figure 4.2: Layout of the divider buffer (130μm x 100μm).



Divider buffer This block is very similar to the previous one, and has the same size. Smaller coupling capacitors have been employed, compared to the RF buffer, to reduce the input parasitic capacitance, and smaller EF transistors as well.

Frequency divider and LO buffers The layout of this circuit is very important, because it strongly influences its performance: indeed, the sampling and latching pairs of the flip-flops, that ideally should be symmetrical, in practice very hardly meet this target, because of the need for a simple and compact layout, with short connections between the components. To reach the goal, dummy components, like the copies of the load resistors highlighted in Fig.4.3, dummy metal connections and vias have been employed to equalize the strips' parasitics and resistances.

Figure 4.3: Layout of the frequency divider ($150\mu m$ x $130\mu m$).



Mixer This is the core of the device. In Fig.4.4 the driver circuit and the mixer core are highlighted. The following guidelines have been followed:

- the paths traveled by the LO signal are realized with straight metal paths, avoiding crossings with other metal layers if possible, or making the crossings at least symmetrical from a differential standpoint;
- the same rule is followed to realize the transconductor;
- the connections carrying DC voltages, on the contrary, can be realized with large metals, since capacitive parasitics are not a concern, and can be crossed over other connections of the same type (an example are the mixer output lines).

The input of the LO driver is located at the bottom left side, while the RF input is at the bottom right one: this has been chosen in order to minimize the distance traveled by the signals. The outputs, instead, are located at the top, after the MIM filtering capacitors.

Test chip top-level Fig.4.5 shows the top level layout of the chip. On the border, the aluminum pads providing a connection to the external environment

are present, along with the ESD protections, and the clamp circuits. The divider buffer is fed through transmission lines, approximately 230μm long, while the RF buffer has been placed very close to the input pads, so as to enhance the impedance matching. The output lines are connected to the respective pads at the top and bottom of the layout. Being the information in the outputs at baseband, the involved metal paths have been placed as needed, without care for eventual intersections with lines on adjacent metal layers. The other pads carry the swap signals, that allow to invert independently the LO signals in the two mixers, the enable, and the supplies. Note that the circuit have been surrounded with big capacitor matrixes, to keep the voltage stable, filter the disturbs coming from the input supply lines, and provide a short path for the eventual high frequency current absorbed from the supply.

Figure 4.4: Layout of the mixer (150μm x 150μm).

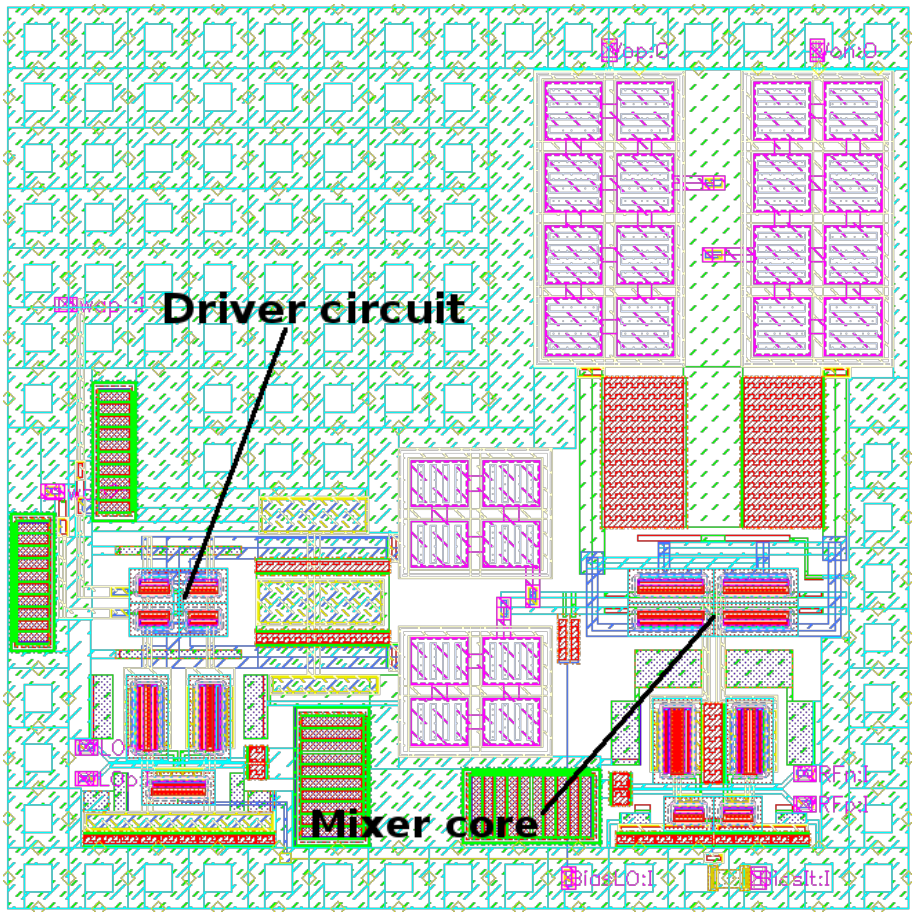
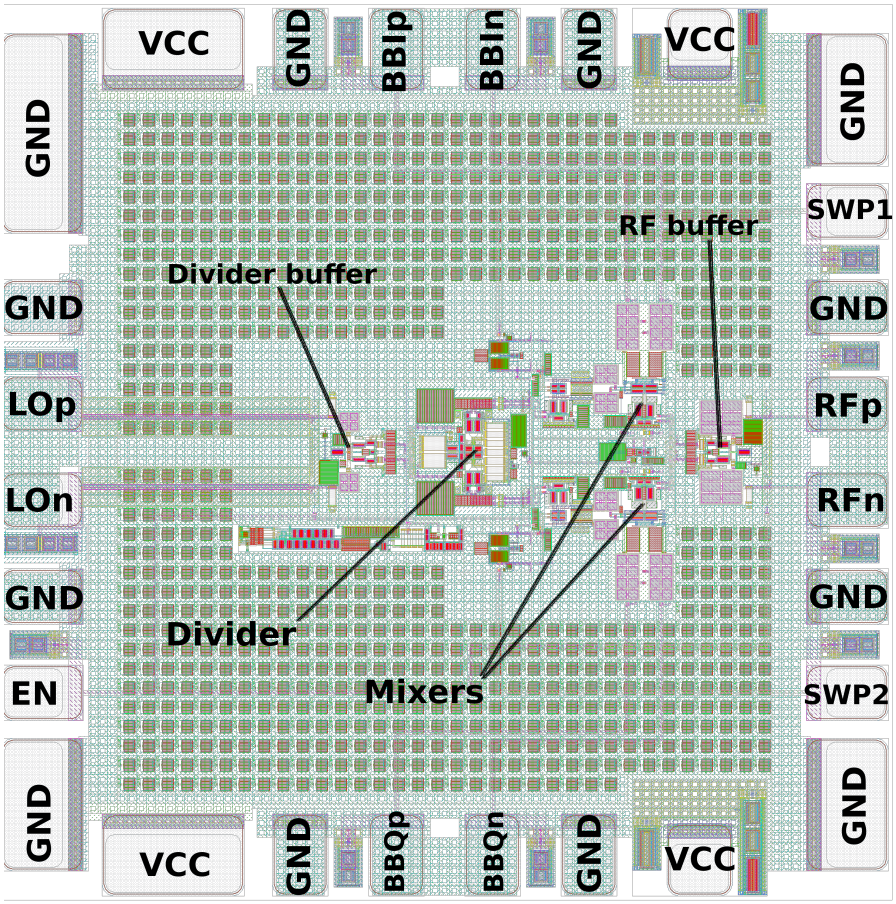


Figure 4.5: Top level of the test chip (930μm x 930μm).



Chapter 5

Results

This chapter presents the results of the simulations for the blocks previously described, finally analyzing the performances of the whole detector. The results about the stability factors have not been included, to avoid enlarging too much this chapter: it is implied that all the circuits have been fully tested and result unconditionally stable.

5.1 Buffers

In this section the performances of the buffers are presented. The results have been obtained from simulations carried out with both the R-C extracted of the circuit and the schematic provided with approximated R-L-C parasitics. The inductive contributions have been roughly estimated using the rule of the thumb which specifies that a connection $x\mu m$ long introduces a parasitic inductance $L_{par} \simeq \frac{x}{2} pH$.

5.1.1 RF buffer

The performances of this buffer have been evaluated in terms of:

- bandwidth;
- impedance matching;
- linearity;
- output offset.

Bandwidth As shown in the figures, over the target supply and temperature range, the RF buffer keeps a bandwidth aligned with the design requirements. Fig.5.1 shows the simulations results obtained from the extracted view, the worst-case result being at the temperature of 85 °C, in which case the -3dB bandwidth results $f_{-3dB} \simeq 65GHz$. Fig.5.2 shows the same simulations carried out employing the schematic with R-L-C parasitics added on the input and

Figure 5.1: Freq. resp., varying supply voltage and temperature (extracted)

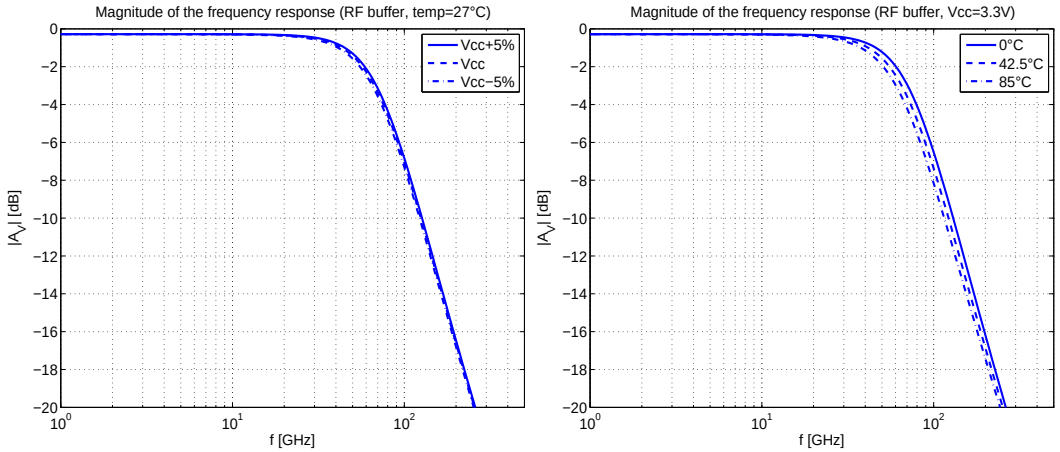
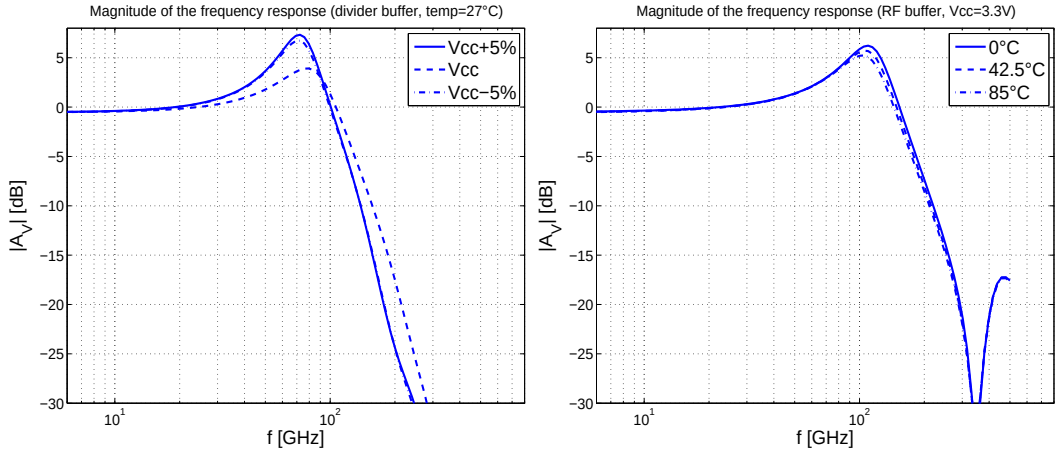


Figure 5.2: Freq. resp., varying supply voltage and temperature (schematic)

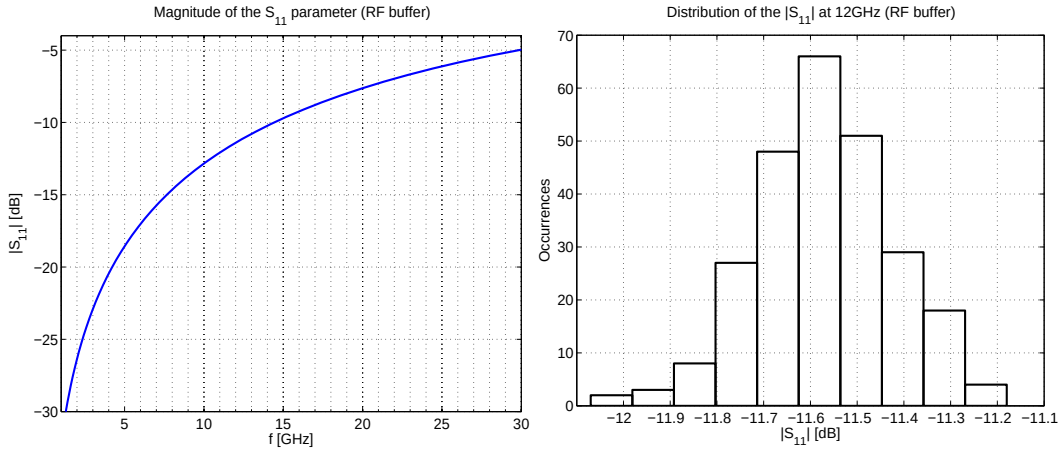


output lines: the effect is evident, since the bandwidth is increased, and the frequency response becomes a second order one with $Q > 1$, that means the system exhibits oscillatory convergent modes. This is not a concern, since the measurement is performed in steady-state operation.

Impedance matching Impedance matching is quantified by the magnitude of the coefficient $|S_{11}|$, which has to keep below -10dB. In this case it has been verified that variations of supply voltage and temperature weakly influence the matching: the main contributions, indeed, come from the variations of the matching resistance. Fig.5.3 reports a simulations carried out at 27 °C, showing that the condition is guaranteed up to 15GHz, together with the statistics of $|S_{11}|$ at 12GHz, due to mismatch and process variations.

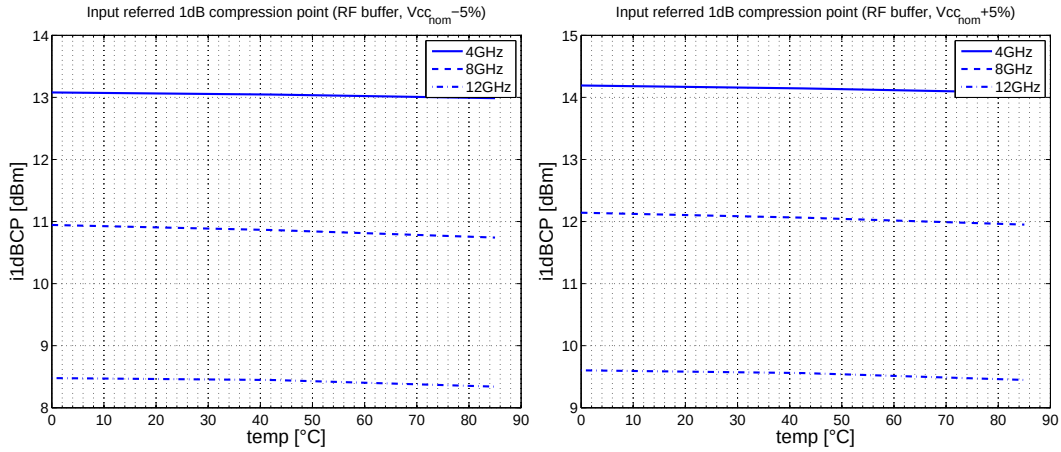
Linearity As explained in section 1.5.2, a figure of merit often employed to characterize linearity is the third-order intercept point (IP3). In this case, on the other hand, calculating the IP3 is not completely appropriate, because the circuit must work with a single-tone input, therefore it has been preferred

Figure 5.3: Magnitude of $|S_{11}|$ (extracted)



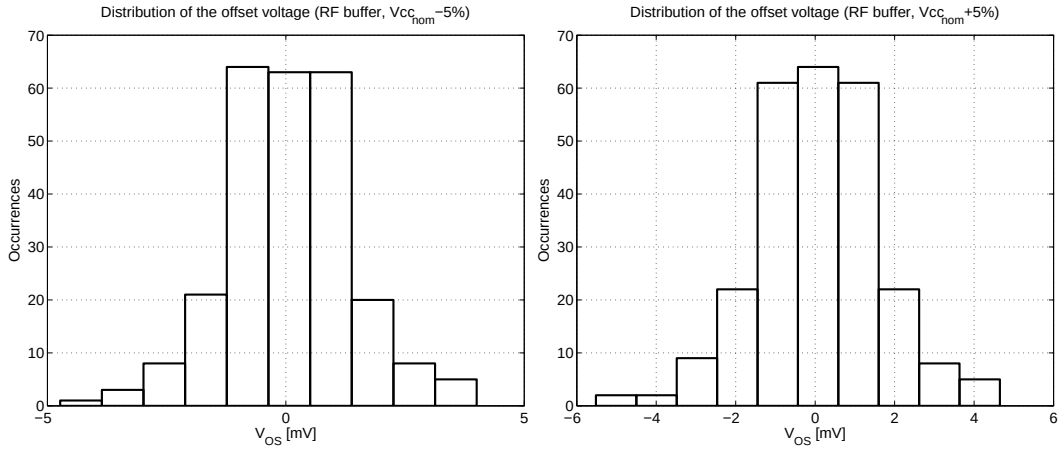
to look at the 1dB compression point (1dBCP), that gives a direct indication about the drop of the gain for high input power. Fig.5.4 shows this parameter, as it results from simulations conducted at the edges of the operating voltage range. The worst-case condition is individuated at maximum frequency and minimum supply voltage, since this means also minimum bias current (remember that the reference currents are obtained from simple circuits like the one in Fig.3.24). The minimum simulated i1dBCP is of 8.5dBm, which is enough, considered that the maximum input power is $P_{RF,MAX} = 0dBm$.

Figure 5.4: Input-referred 1dB compression point (RF buffer)



Output offset The offset due to mismatch and process variations has been simulated through Monte Carlo analysis. The worst-case results have been found at 85 °C: Fig.5.5 reports the histograms of the results with minimum and maximum supply voltages. The standard deviations result respectively $\sigma_{Vos,Vccmin} = 1.33mV$ and $\sigma_{Vos,Vccmax} = 1.56mV$.

Figure 5.5: Output offset (RF buffer)



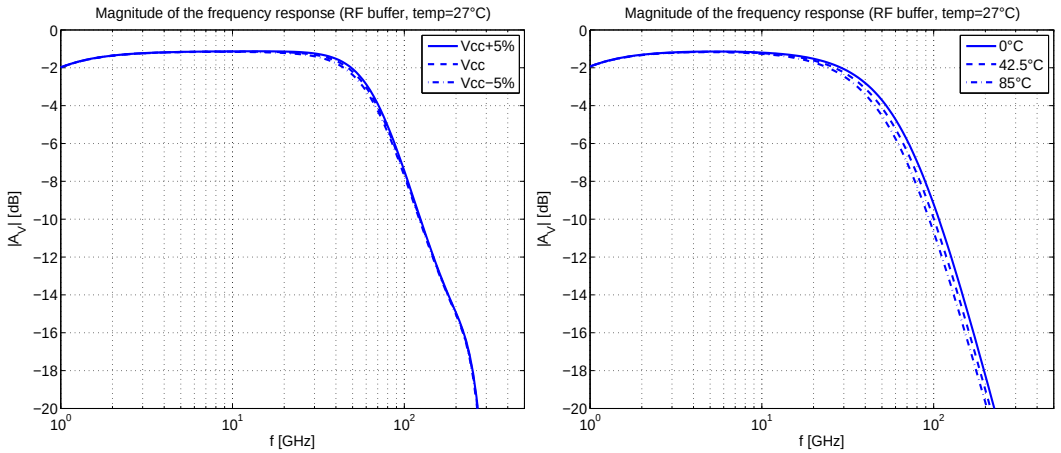
5.1.2 Divider buffer

The performances of this buffer have been evaluated in terms of:

- bandwidth;
- impedance matching;
- output offset.

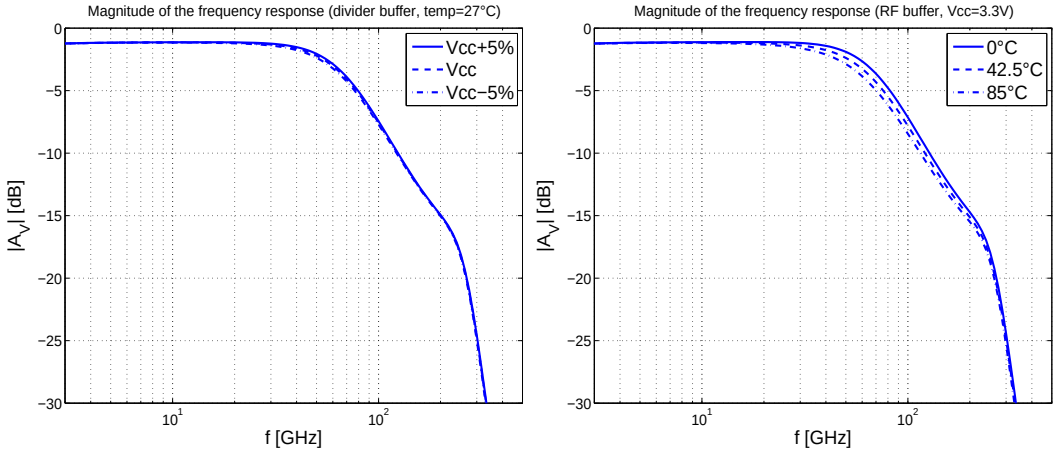
Unlike the previous case, linearity here is not a concern, since this buffer simply needs to steer the differential pairs of the divider.

Figure 5.6: Freq. resp., varying supply voltage and temperature (extracted)



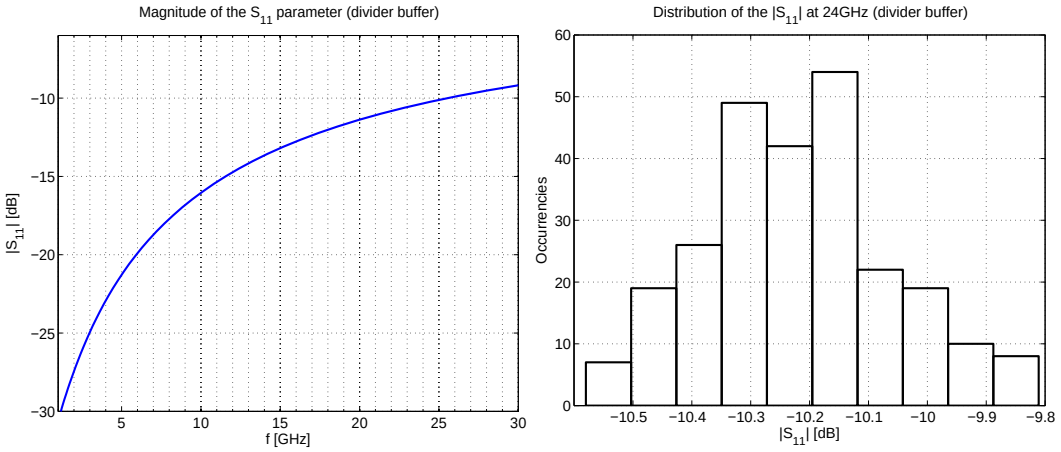
Bandwidth Fig.5.6 and 5.7 show the results, in the same way as done in the previous section. It can be observed that, with respect to the RF buffer, in this case the bandwidth is reduced to 55-60GHz. This means the input signal is going to be quite attenuated especially at highest frequency, however, if an input power of 3dBm is guaranteed, the output signal keeps an amplitude largely sufficient to drive the frequency divider.

Figure 5.7: Freq. resp., varying supply voltage and temperature (schematic)



Impedance matching Fig.5.8 shows the results for the impedance matching. As depicted, the target $|S_{11}| < -10dB$ is guaranteed up to 25GHz. The Monte Carlo analysis highlights that mismatch and process variations may lead to exceed this bound at the maximum operating frequency, but this is considered acceptable, since it happens in the worst-case condition, and in less than 10% of the cases.

Figure 5.8: Magnitude of $|S_{11}|$ (extracted)

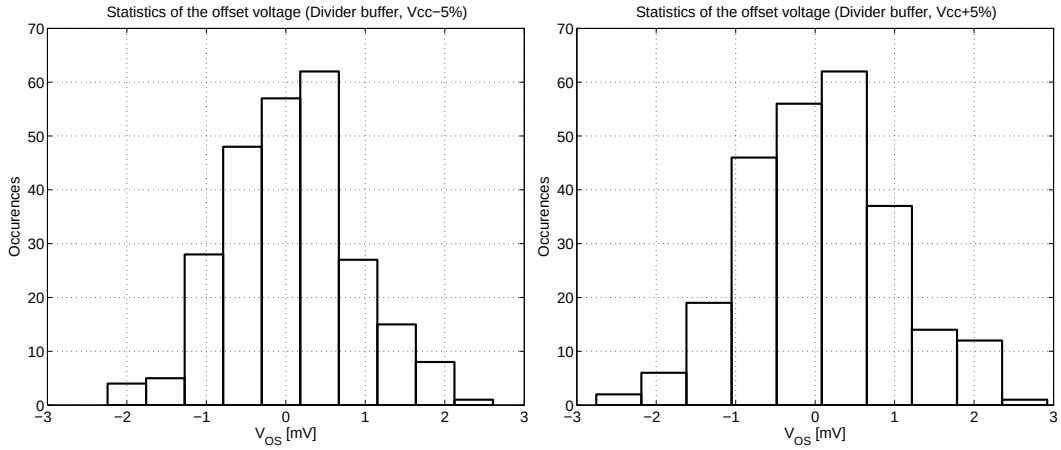


Output offset The distribution of the output offset for the divider buffer is depicted in Fig.5.9, again at 85 °C and in the two cases of Vcc-5% and Vcc+5%. The standard deviation results $\sigma_{Vos,Vccmin} = 0.79mV$ and $\sigma_{Vos,Vccmax} = 0.92mV$, a slightly better result, with respect to the RF buffer, mainly thanks to the oversizing of the biasing resistors.

5.1.3 LO buffers

The LO buffers need to provide:

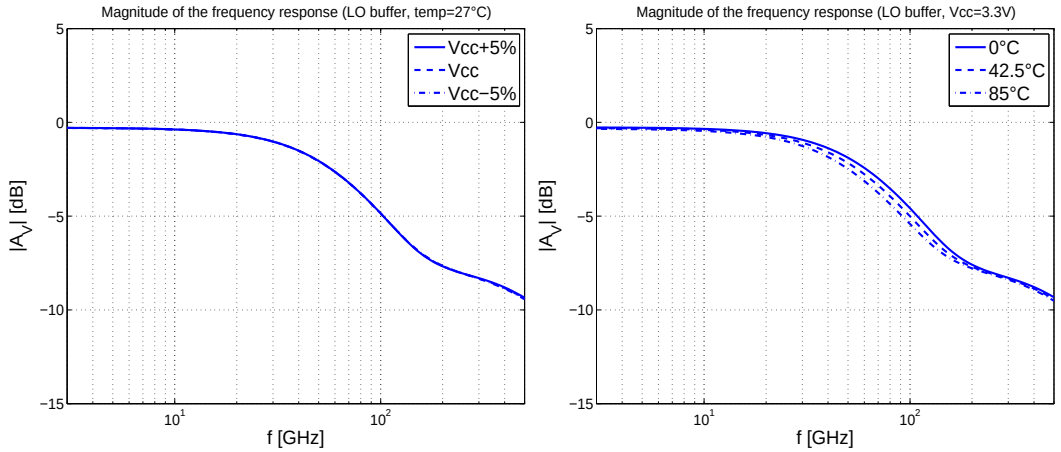
Figure 5.9: Output offset (divider buffer)



- adequate bandwidth;
- high input impedance, to reduce the loading effect on the divider;
- low output offset.

Therefore, the listed performances have been evaluated. The following simulations rely on the R-C extracted circuits, while it has been considered unnecessary to include inductive parasitics, since the lengths of the connections between the divider, the buffers and the mixers are small compared to the cases of the input buffers.

Figure 5.10: Freq. resp., varying supply voltage and temperature (LO buffer)

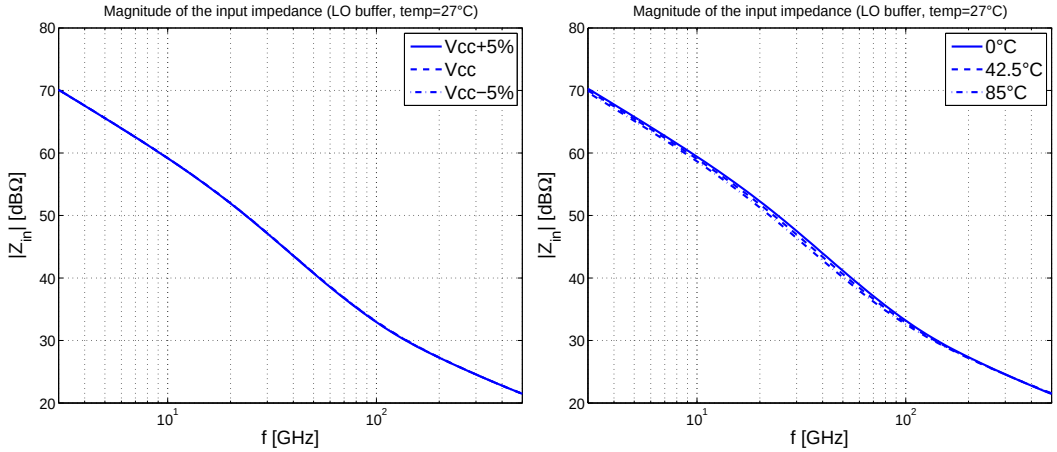


Bandwidth Fig.5.10 displays the frequency response of these buffers with varying temperature and supply voltage, the -3dB bandwidth resulting $f_{-3dB} > 65GHz$. A wider bandwidth would be desirable for faster switching: note that, at maximum frequency $f_{LO} = 12GHz$, and supposing the divider to provide an ideal square wave, the fifth harmonic is found approximately at the cut-off, so it is attenuated by 3dB, meaning that the buffer severely attenuates the

higher order harmonics. On the other hand, this is an ideal situation, because the divider does not provide infinite-slope edges: recalling the analysis carried out in section 3.3.1, it is easy to see that the time constant limiting the speed of the divider is much higher than the one of the buffer, ultimately limiting the speed of the system. Therefore, such performance is acceptable.

Input impedance Fig.5.11 shows the magnitude of the input impedance for the LO buffer in the conditions mentioned above. As it can be observed, in the frequency range of interest, the graph has a -20dB/decade slope, indicating a capacitive contribution. However, the magnitude results $|Z_{in}|_{dB} > 55-60dB\Omega$, meaning an equivalent capacitive loading of roughly 20fF, essentially due to the base-collector capacitances of the EFs. Note that, directly connecting the divider to the LO driver circuit, the equivalent high-frequency capacitive loading would have been easily 5 times bigger, proving that the EFs effectively contribute in speeding-up the switching.

Figure 5.11: Input impedance, varying supply voltage and temperature (LO buffer)

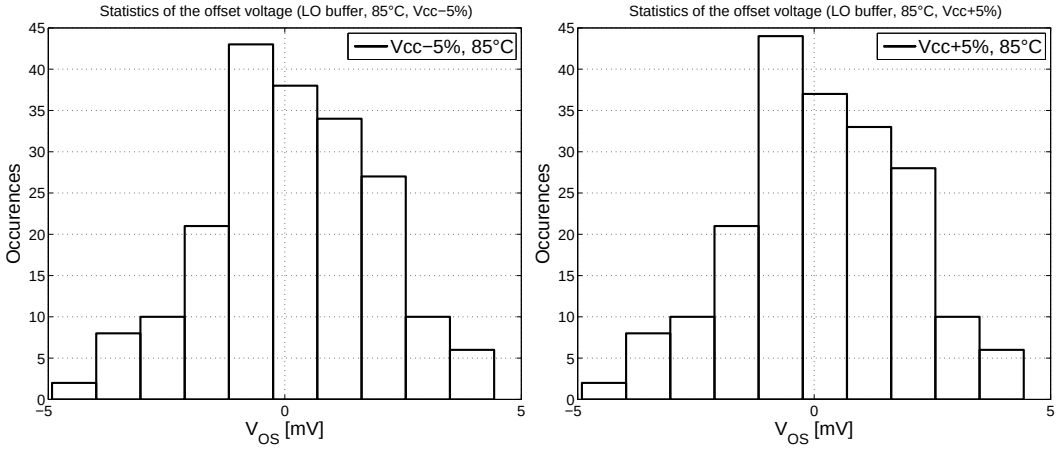


Output offset Like done for the input buffers, Fig.5.12 reports the distribution of the output offset, simulated through Monte Carlo analysis. The standard deviation results higher than what seen for the input buffers, due to the divider offset contribution.

5.2 Frequency divider

Regarding the divider, the considered parameters are the quadrature phase error, measured like the phase shift between the fundamental components of the two outputs of the divider, and the amplitude of the fundamental, because they are essential for efficient mixing. Concerning the phase quadrature error, the worst-case condition has been found at maximum operating frequency, temperature of 85 °C and maximum supply voltage. Fig.5.13 and Fig.5.14 show

Figure 5.12: Output offset (LO buffer)



the distribution of the quad error at the mentioned temperature, minimum and maximum supply voltage, respectively at 4GHz and 12GHz. The standard deviations in the different cases are:

- $\sigma_{\phi err}|_{3GHz,V_{ccmin}} = 0.23°$;
- $\sigma_{\phi err}|_{3GHz,V_{ccmax}} = 0.25°$;
- $\sigma_{\phi err}|_{12GHz,V_{ccmin}} = 0.33°$;
- $\sigma_{\phi err}|_{12GHz,V_{ccmax}} = 0.36°$.

This situation is better highlighted in Fig.5.15, where the standard deviation of the quad error is plotted versus the temperature for different frequencies and supply voltages. Fig.5.16 and 5.17 instead show the statistics of the fundamental harmonic amplitude in the same conditions discussed for the quad error. In all the considered conditions the standard deviation keeps below 0.2dB, assuring robust switching in each condition.

Figure 5.13: Distribution of the quad error (f=3GHz)

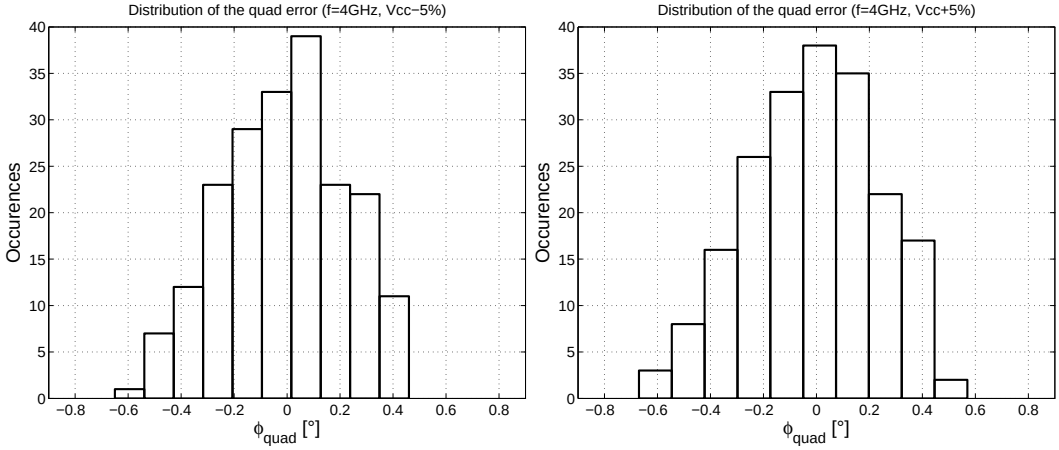


Figure 5.14: Distribution of the quad error (f=12GHz)

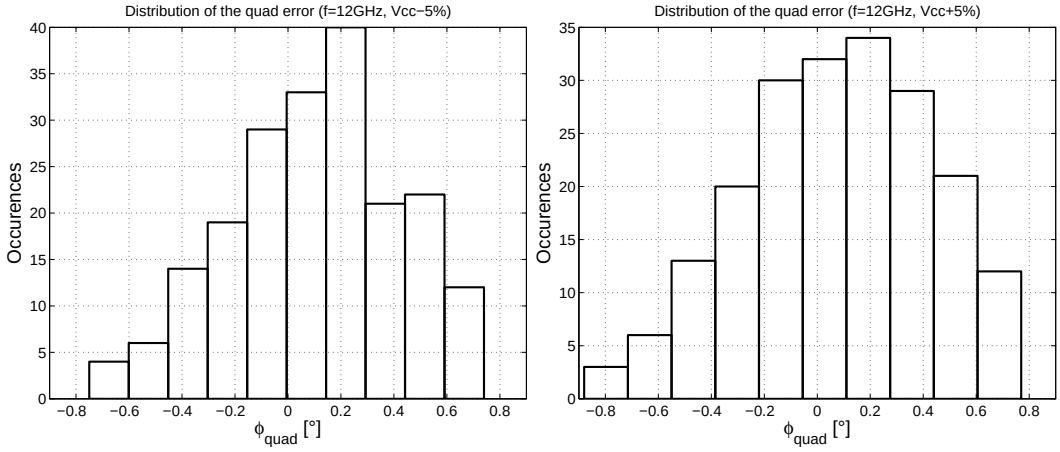


Figure 5.15: Std.dev. of the quad error vs temperature, frequency and Vcc

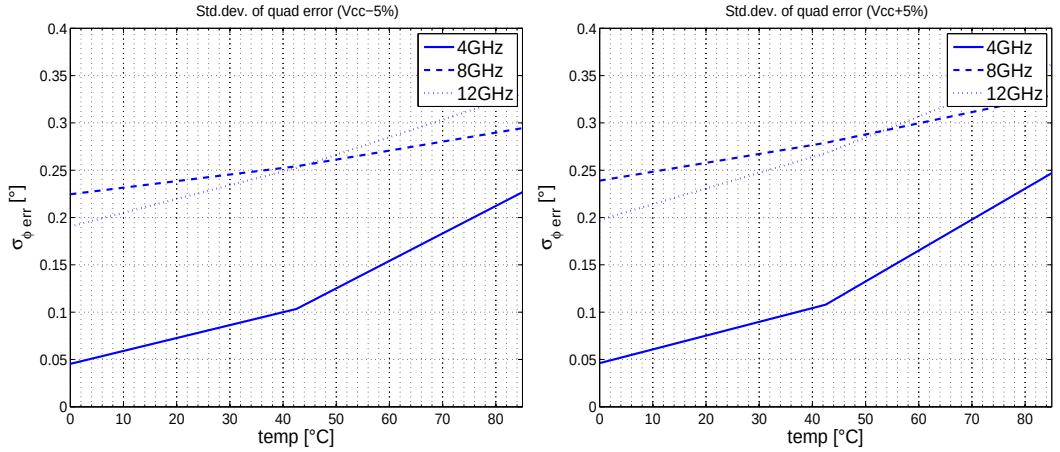


Figure 5.16: Distribution of the fund. harmonic amplitude (f=3GHz)

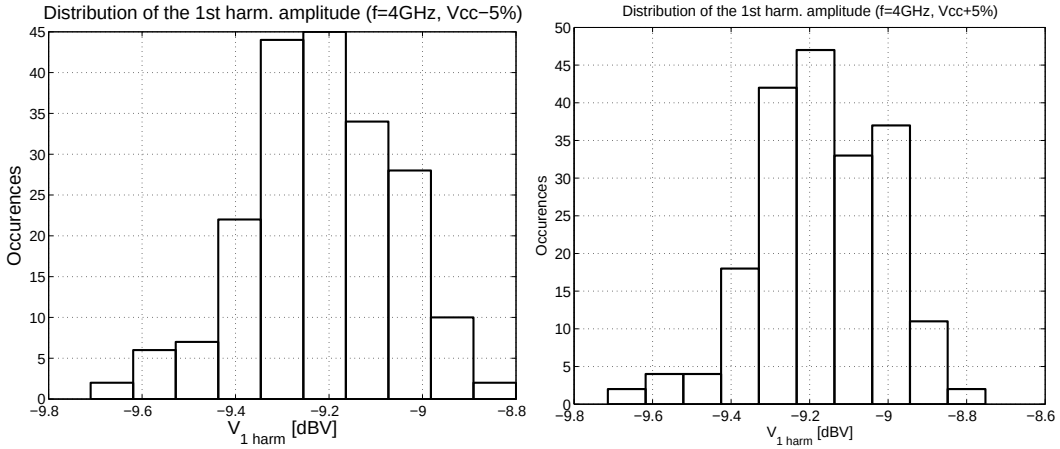
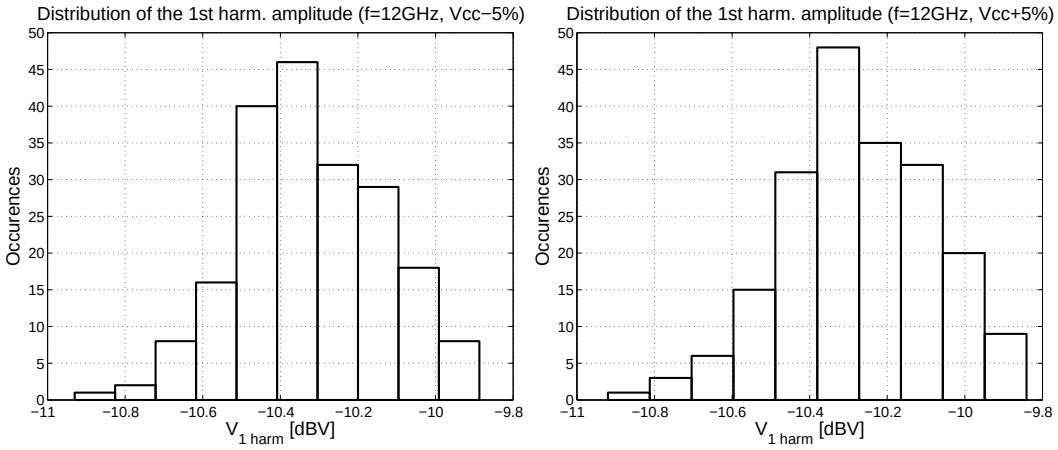


Figure 5.17: Distribution of the fund. harmonic amplitude (f=12GHz)



5.3 Mixer

For the mixer circuit, the evaluated parameters are:

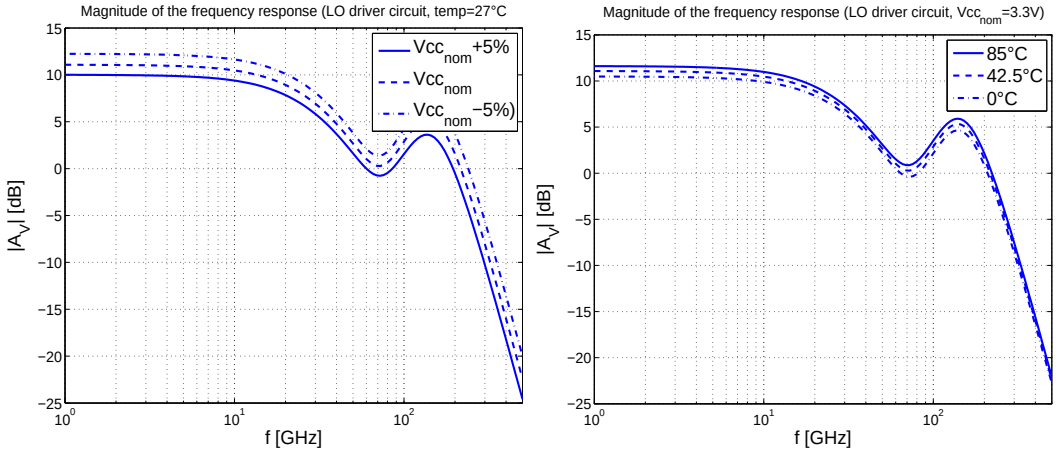
- LO driver bandwidth;
- voltage gain;
- linearity;
- output offset.

The first is important to guarantee the switching closest to ideality, thus the highest gain and lowest output offset. Voltage gain should be kept as high as possible to minimize the degradation of the measurements due to offsets, if the LO-swap feature is not exploited, and to allow the best offset estimation, if, on the contrary, it is employed. Linearity, that depends mainly on the transconductor block, needs to be, in terms of compression point, high enough to guarantee low amplitude measurement error at maximum input power, while output offset, of course, needs to be as low as possible.

LO driver bandwidth Fig.5.18 depicts the frequency response of the LO driver circuit. The bandwidth results relatively low, being approximately 25-30GHz in all cases, because it is dominated by the time constant at the output node, given by (3.7). The main contributions to the loading capacitances are given by the base-emitter junctions of the switches, the bottom parasitics of the MIM coupling capacitors, and the parasitics due to the layout, being the connections between the transconductor and the load resistors realized in a metal layer that is not capable of withstanding high current densities, that has resulted in the usage of large metal strips. An optimized layout, therefore, can lead to better performances, but the improvement margin is quite reduced, because the other capacitances are dominant. Trying to lower the resistance,

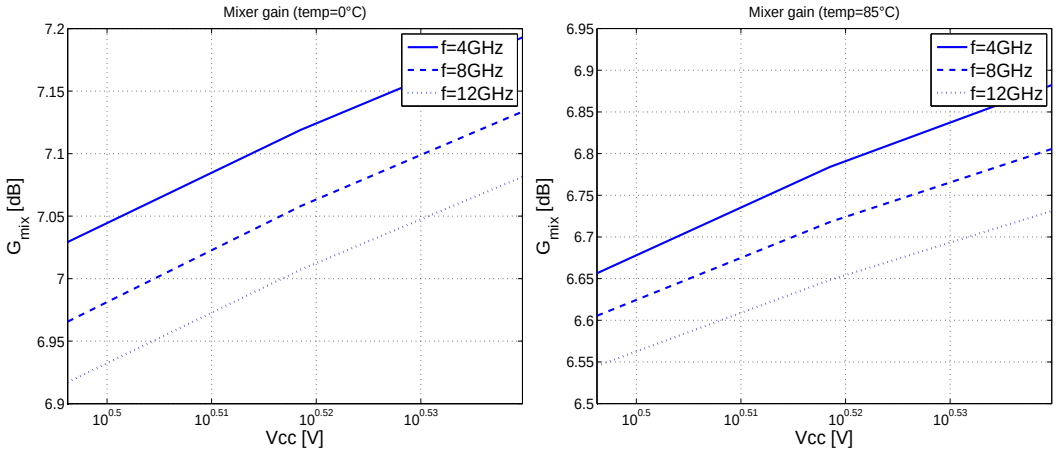
on the other hand, would lead to a even higher current, to maintain the same swing, and the need for larger metal strips, thus this solution is considered acceptable, keeping in mind that it is the bottleneck of the system, in terms of commutation speed.

Figure 5.18: Freq. resp. of the LO driver circuit, varying supply and temperature



Voltage gain The target voltage gain for this mixer is approximately 7dB and, as highlighted by Fig.5.19, the goal is reached, even if in the upper part of the frequency range it is registered a slight decrease.

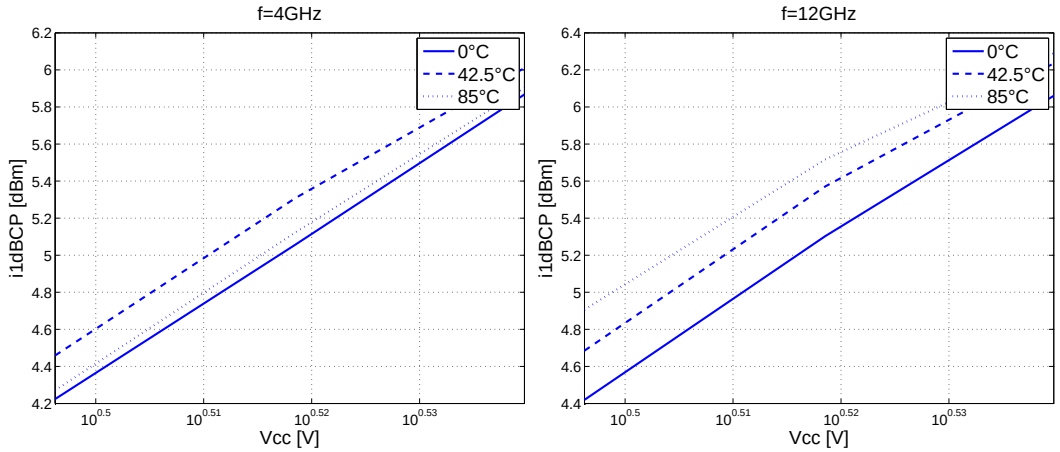
Figure 5.19: Voltage gain of the mixer with varying frequency, temperature and supply voltage



Linearity Like in the case of the RF buffer, the linearity is best quantified by the 1dB compression point, because the circuit is going to be fed with a single-tone input signal. It is necessary to point out a particularity, from this standpoint: normally the compression point and the intercept points are not related to the phases of the signals; in this case, instead, they must be considered, because if the RF and LO signals are in quadrature, the output is

naturally close to zero, and the evaluation of the mentioned parameters loses any meaning. Therefore, in this paragraph the compression point, by convention, is evaluated imposing the RF and LO signals to be in phase or in phase opposition. Fig.5.20 shows the simulation results, evidencing values between 4.2dBm and 6.3dBm. The compression is naturally more evident at low temperatures, and it results higher at 12GHz simply because of the bandwidth limitations of the circuits. This highlights that the amplitude measurement performances of the detector are limited by the linearity of the mixers, being the RF buffer compression point higher in all conditions.

Figure 5.20: Input referred 1dB compression point, evaluated at 4GHz, and 12GHz

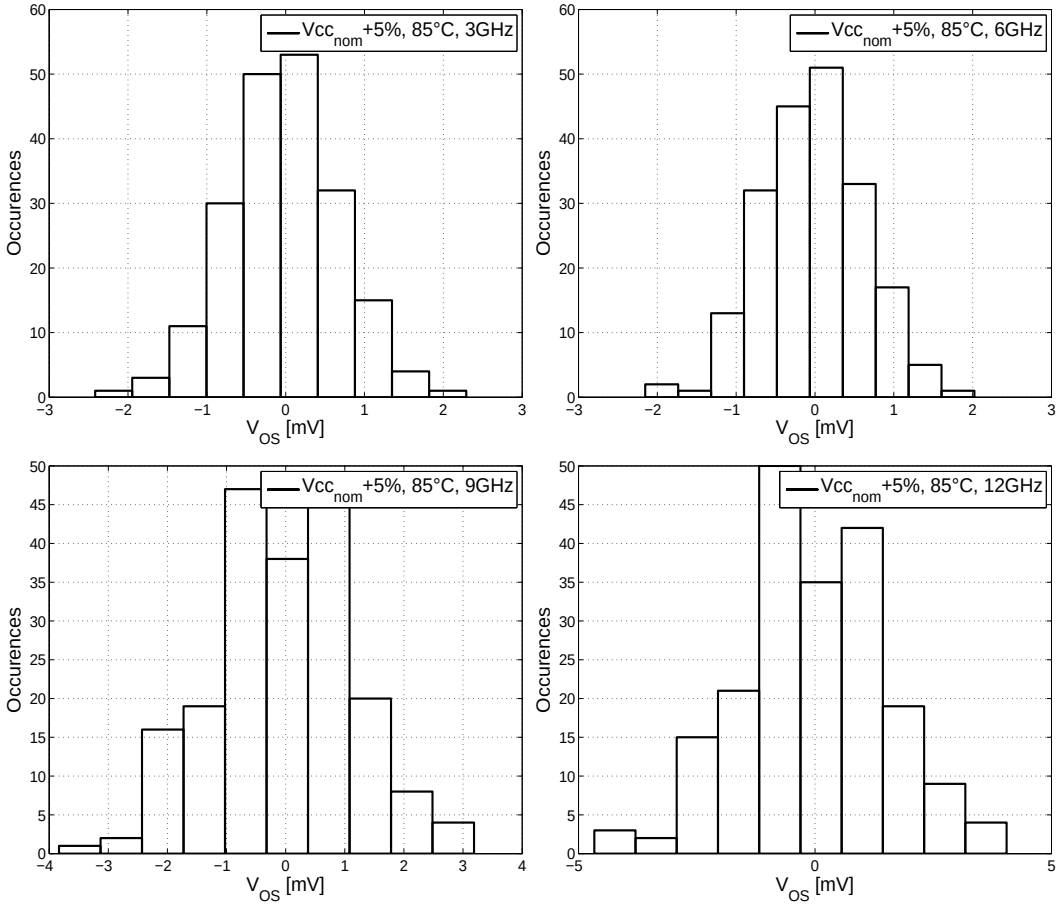


Output offset This paragraph presents the output offset distribution obtained from the simulations of the mixer, carried out with maximum temperature and supply voltage, because these are the worst-case conditions. Fig.5.21 reports the distributions at 3GHz, 6GHz, 9GHz and 12GHz. The maximum standard deviation, as can be observed, is reached at 12GHz, and its value is $\sigma_{V_{OS,max}} = 1.4mV$.

5.4 Detector

In this last section the performances of the detector are presented. First, the amplitude measurement performances are described: since in this case the error is due mainly to compression, the device has been tested reporting the ratio of the measured amplitude at $P_{RF,MAX}$ to the one at $P_{RF,MIN}$, which evidences the maximum error, comparing the results obtained at different temperatures and supply voltages. The phase measurement has been simulated both at $P_{RF,MAX}$, where the involved magnitudes make unnecessary the offset compensation and at $P_{RF,MIN}$, where the performances with and without compensation have been compared.

Figure 5.21: Distributions of the mixer output offset



5.4.1 Amplitude measurement

The amplitude measurement has been checked via Monte Carlo simulations at the frequencies of 3GHz, 6GHz, 9GHz, and 12GHz. For each of these frequencies, the performances have been evaluated at different supply voltages and operating temperatures, and with the worst-case input phases, so as to evaluate the device in its most critical conditions. Since the relative measurement is performed at $P_{RF,MAX}$ and referred to the reference obtained at $P_{RF,MIN}$, the target result is 20dB, with a maximum error of 0.5dB. This means that, due to the compression, the aim is to get measurements over 19.5dB.

Figure 5.22: Distributions of the relative amplitude measurement (f=4GHz, worst-case RF phase)

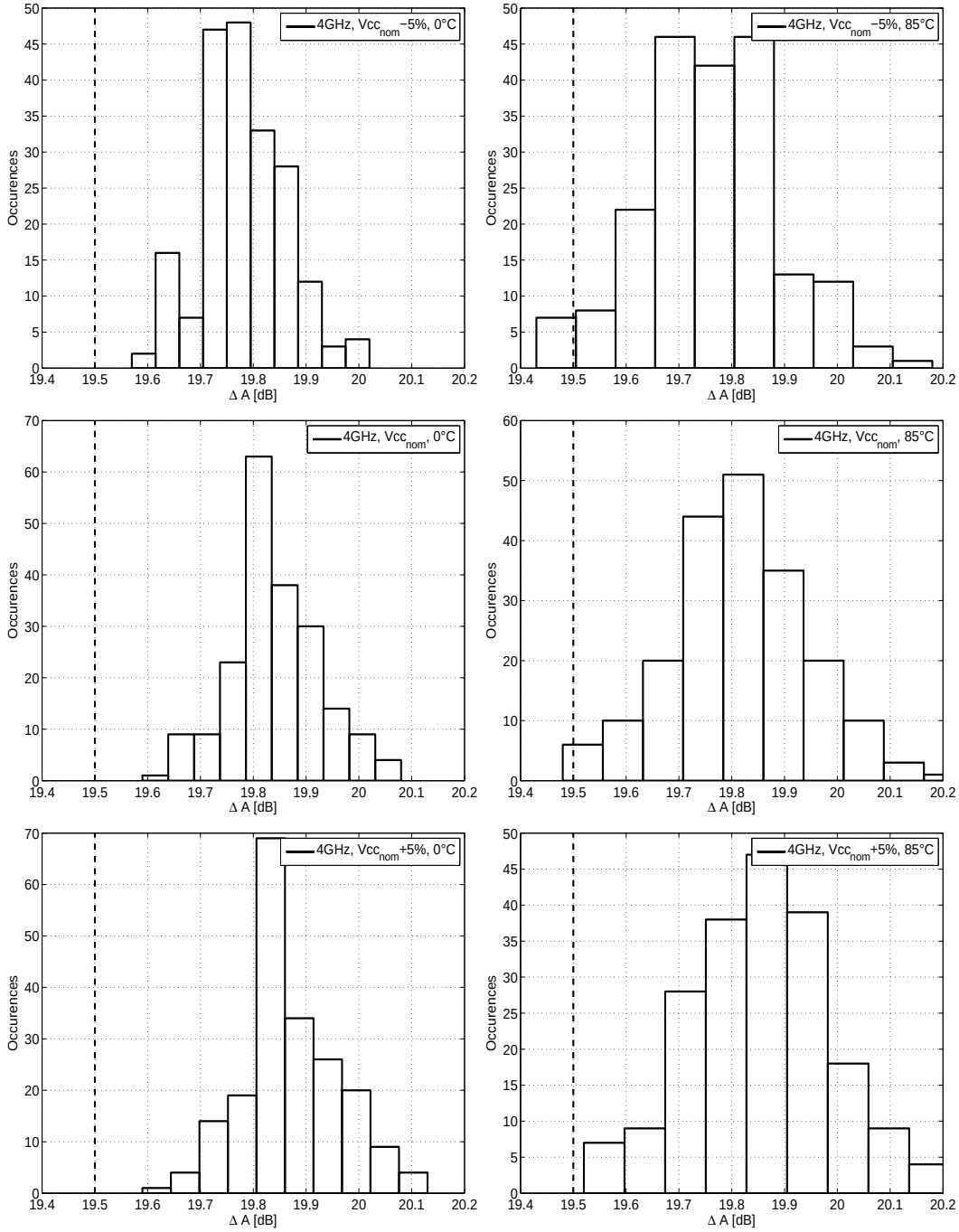


Figure 5.23: Distributions of the relative amplitude measurement (f=8GHz, worst-case RF phase)

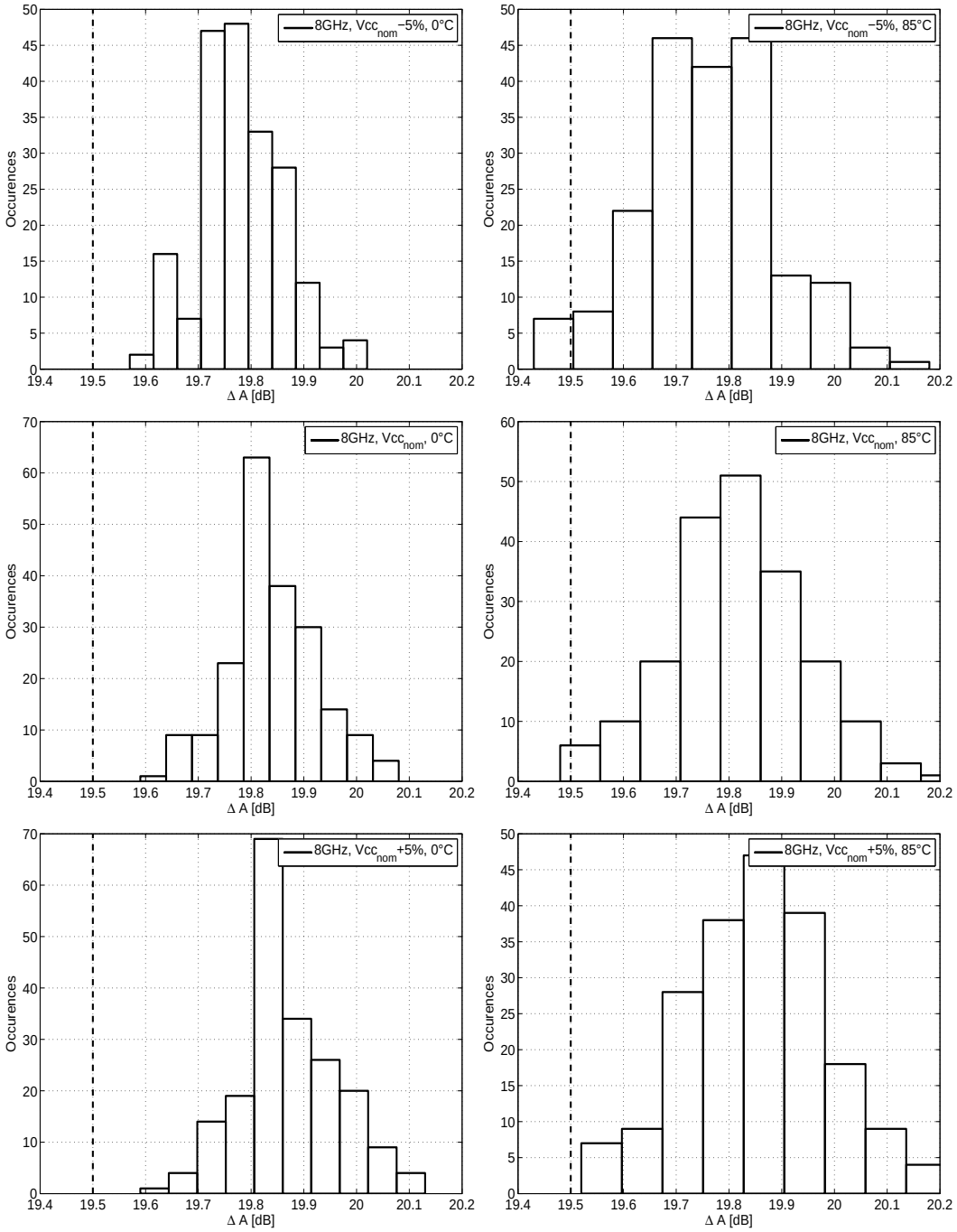
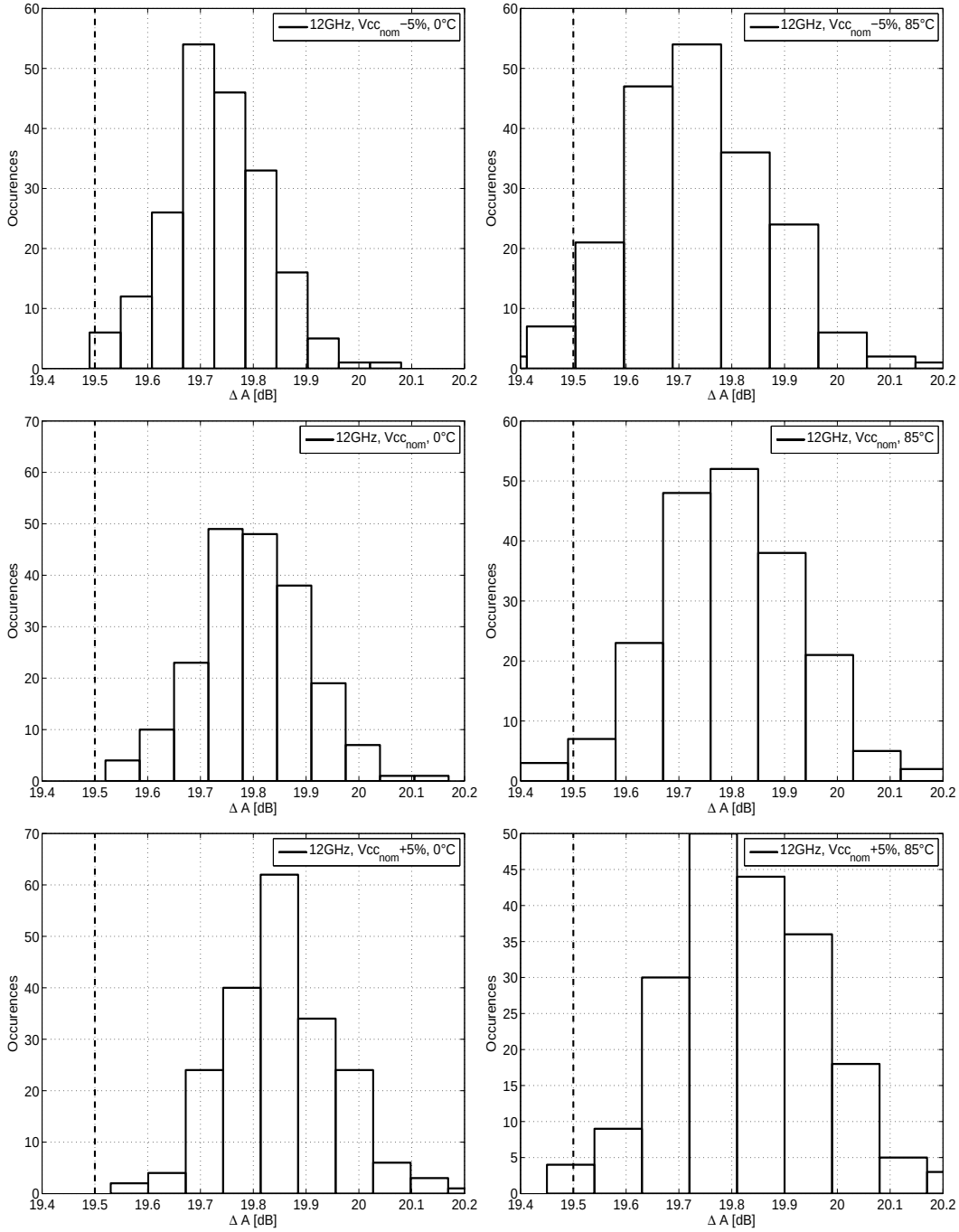


Figure 5.24: Distributions of the relative amplitude measurement (f=12GHz, worst-case RF phase)



As can be observed in the graphs, the error tends to worsen with increasing frequency, increasing temperature, and decreasing supply voltage. The highest error is reached in the following conditions:

- RF frequency $f = 12GHz$;
- temperature 85 °C;
- supply voltage $Vcc_{nom} - 5\%$;

- worst-case input phase.

In the listed conditions, the measured relative amplitude results on average 19.7dB, and the distribution highlights that 95% of the samples falls within the desired range. Considered the wide range of operating conditions that the device has to deal with, this performance has been evaluated suitable to the purpose of this work. If this was not sufficient, anyway it is possible to perform the measurement only for those input phase ranges where the error is bounded even more robustly below 0.5dB, and then extract the amplitude measurement over the whole range through interpolation.

5.4.2 Phase measurement

In this subsection the phase measurement performances are presented. The evaluations have been carried out both at minimum and maximum input power, and, in particular, the performances at minimum input power are compared in the cases of compensated and non-compensated operation.

Performances at $P_{RF,MAX}$ Fig.5.25 to 5.28 show the behavior of the relative phase error with $f = 12GHz$, and varying temperature and supply voltage. As highlighted, the magnitude of the error keeps always below 2°, thus largely meeting the target, and of course, reducing the frequency, the performance further improves. Note that the average value of the error is not zero, because of the distortion mechanism discussed in section 3.4.1.

Figure 5.25: Phase error performances at $P_{RF,MAX}$, f=12GHz, temp=85°C, supply Vcc_{nom}+5%

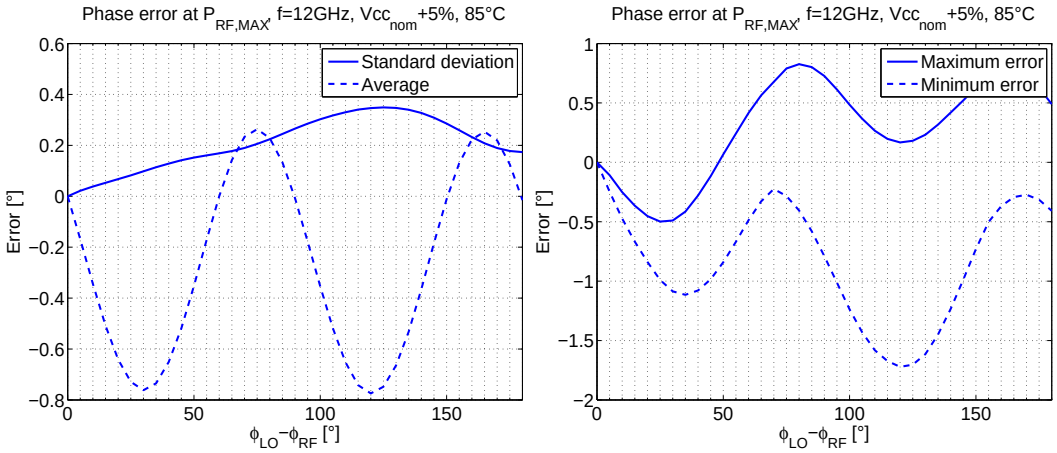


Figure 5.26: Phase error performances at $P_{RF,MAX}$, f=12GHz, temp=0°C, supply Vcc_{nom}+5%

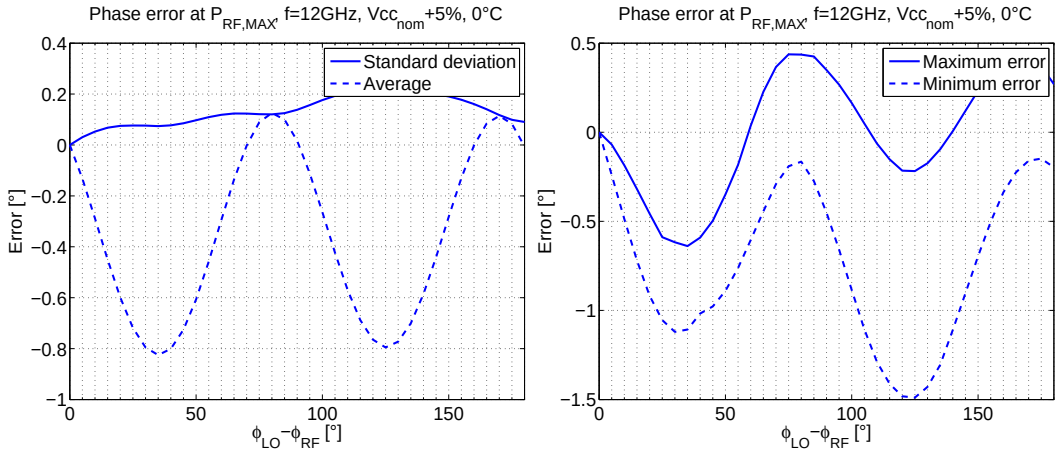


Figure 5.27: Phase error performances at $P_{RF,MAX}$, f=12GHz, temp=85°C, supply Vcc_{nom}-5%

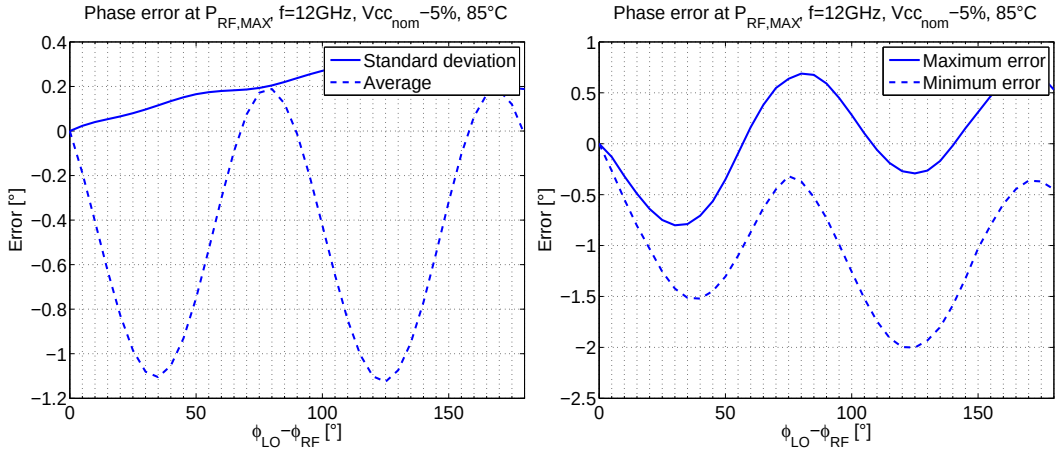
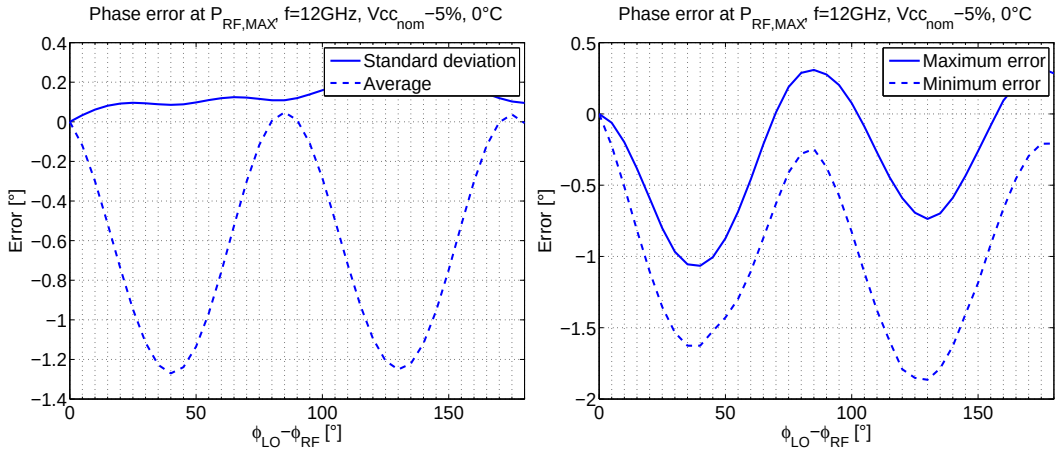


Figure 5.28: Phase error performances at $P_{RF,MAX}$, f=12GHz, temp=0°C, supply Vcc_{nom}-5%



Performances at $P_{RF,MIN}$ In this last paragraph, the phase measurement issue at minimum input power is presented. Performances with and without offset error compensation have been compared at different frequencies and supply voltages, keeping the maximum operating temperature, since this condition causes the worst error. Unlike the previous paragraph, the ADC quantization error introduced by an ideal converter with 2V full-scale range and 10 bits (thus a quantization step of roughly 2mV) is taken into account, observing the effect of this further error on the measurement: such an evaluation is needed to get realistic results, since at $P_{RF,MIN}$ the output voltage produced by the mixer stimulates only a few codes of the ADC, if compared to the result obtained with $P_{RF,MAX}$. The simulations have been carried out by sweeping, in each condition, the RF phase over a range of 180°, with 7.5° steps, which is a reasonable value at all the frequencies, considered the available phased shifters. At each input phase, then:

1. it has been acquired the mixers outputs with both a one and a zero value applied to the SWAP input;
2. the acquired voltages have been quantized;
3. an estimation of the offset has been derived.

Completed the described process, it has been simulated the operation of the DSP, calculating the average of the offset estimations, employing the obtained values to correct the acquired voltages, and calculating both the compensated and uncompensated measured phase. Fig.5.29 to 5.31 display the results, evidencing how the standard deviation of the measured relative phase meets the target $\sigma_\phi < 1°$ in all the situations.

Figure 5.29: Phase error performances at $P_{RF,MIN}$, f=12GHz, temp=85°C

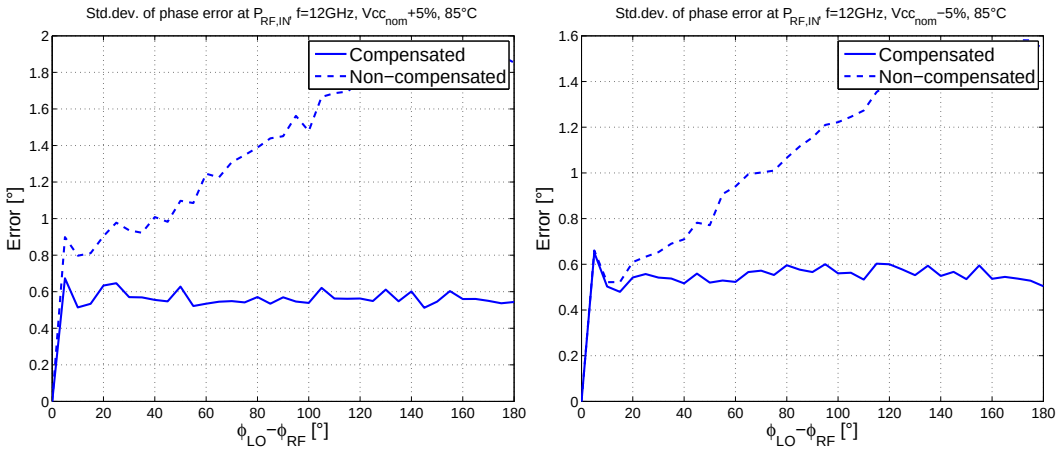


Figure 5.30: Phase error performances at $P_{RF,MIN}$, f=8GHz, temp=85°C

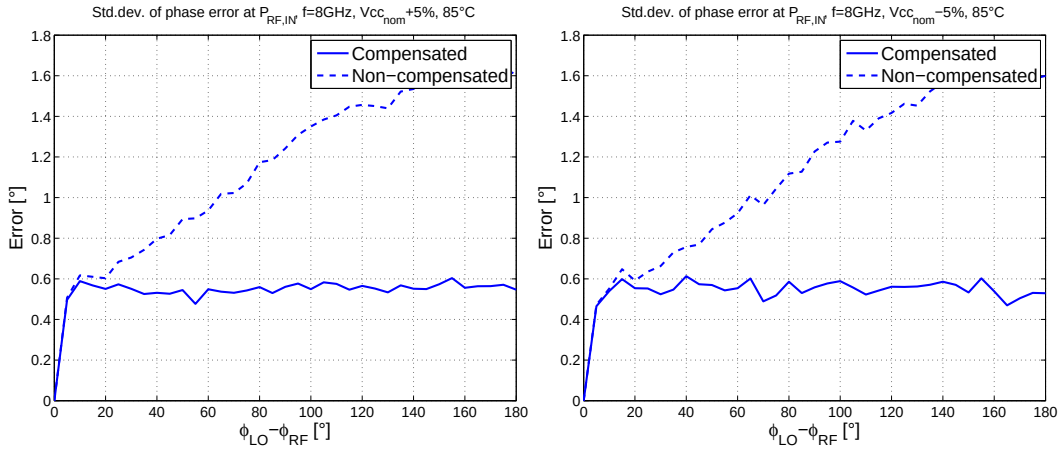
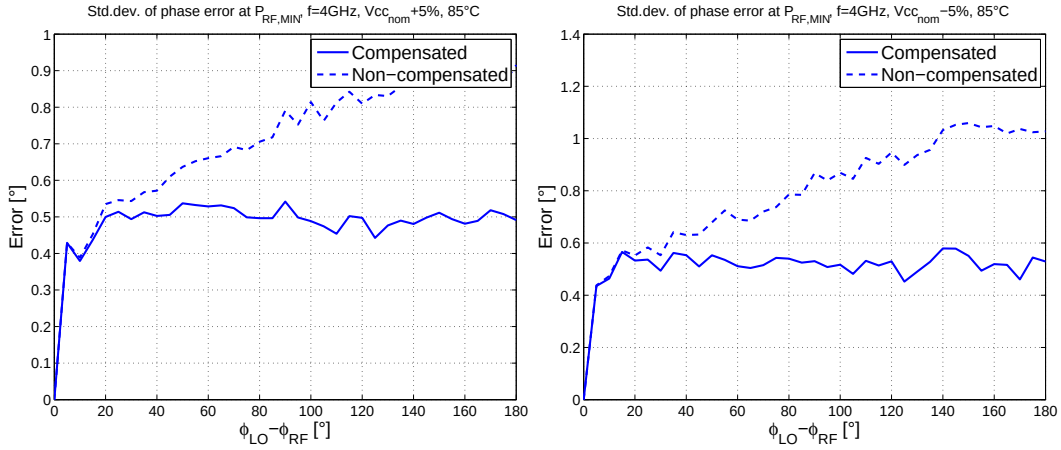


Figure 5.31: Phase error performances at $P_{RF,MIN}$, f=4GHz, temp=85°C



Chapter 6

Conclusions

This work has dealt with the design and simulation of a phase and amplitude detector to be used in a Built-In Test Equipment (BITE) for phased array transmit-receive modules (TRMs). In the introduction chapter, the issues related to the phased array systems have been investigated, leading to explain why it is necessary to provide a reliable and low-cost post-production test procedure for the TRMs, and the advantages of an on-chip solution that handles baseband test signals versus the direct testing at radio frequency. In this context takes place the circuit object of this work, which has to acquire a RF input and extract the information on its relative amplitude and phase, providing them through the baseband outputs. The second chapter describes the top-level structure of the device, investigating the possible circuit topologies to be employed for the realization of the various blocks, and the main issues related to the phase and amplitude measurement. Thus, the design flow is faced in the third chapter, that explains the reasons and the trade-offs behind the main choices taken to reach the target specifications, and compares the different investigated circuits for the realization of each top-level block, leading to the choice of the best solutions: simple EF buffers with input impedance matching networks allow to interface the divider and the mixers to the RF and LO ports, a matching optimized CML frequency divider provides the quadrature LO signals, and double-balanced Gilbert mixers equipped with LO-swap driver circuits are employed to perform the frequency conversion to baseband. In the design chapter the layout issues are also taken into account, pointing out the effect of the parasitics, and the precautionary solutions that need do be adopted, in order to make the design more robust. Chapter 4 deals with the layout procedure, and briefly presents the blocks and their main features, along with the test chip top-level. Finally, chapter 5 presents the results, showing how the target specifications regarding the amplitude and phase measurements are robustly reached by the circuit, over the whole frequency range (4-12GHz), operating temperature range (0 °C-85 °C) and supply voltage range ($Vcc_{nom} \pm 5\%$).

In conclusion, the presented amplitude and phase detector is a good candidate to be employed effectively in a BITE for phased array transmit-receive

front ends. The performances are achieved at the expense of a total area occupation of approximately $0.09mm^2$, and a nominal power consumption of 385mW.

Appendices

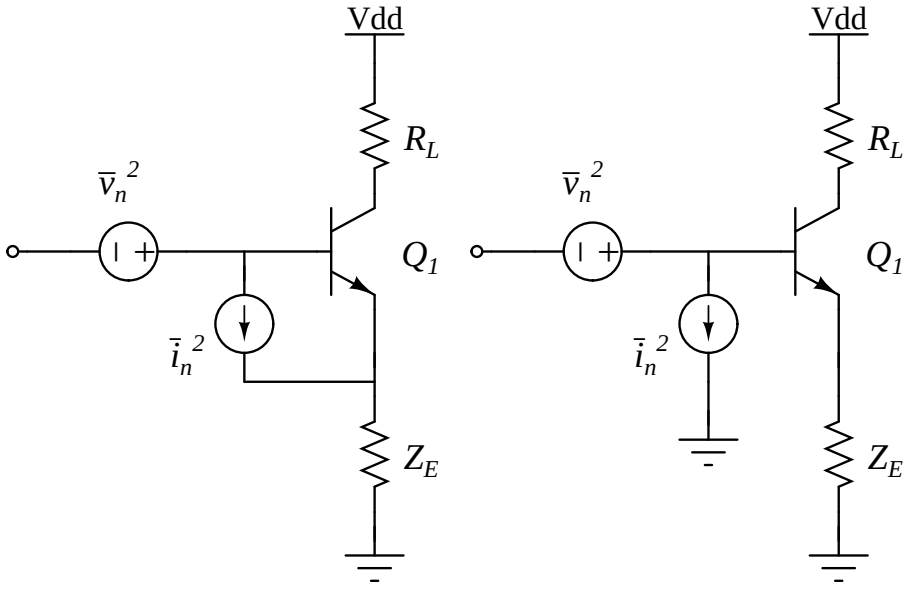
Appendix A

Transconductor noise

In this section the steps to reach the result reported in (3.3) are described.

Recall Fig.3.10 and consider only the noise from Q_1: the circuit can be seen as a common emitter stage with a degeneration impedance Z_E given by the resistor R_E plus the impedance seen looking into the emitter of Q_2. As known from the theory, even in the presence of such a feedback, the noise generators of Q_1 can be moved unchanged to the input, and the same can be done thinking about Q_2, like depicted in FigA.1.

Figure A.1: Effect of feedback on transistor noise generators.

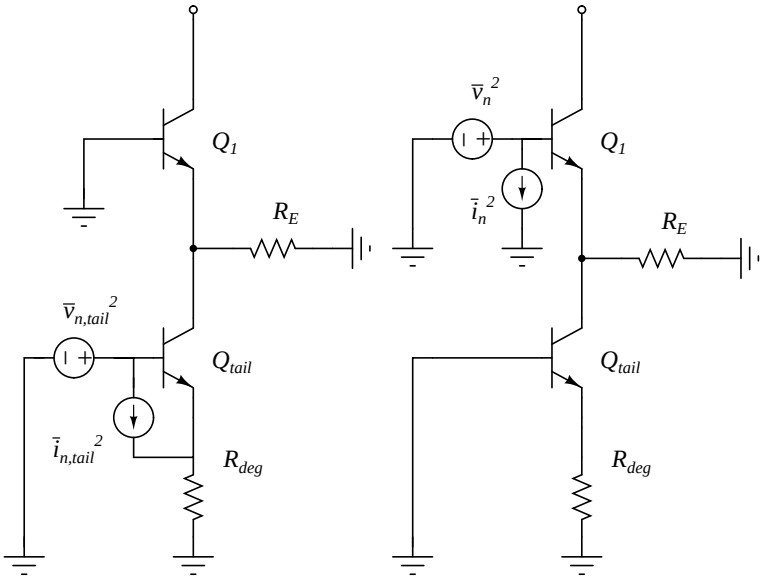


(a) (b)

Consider now the effect of the tail generators: the equivalent input noise can be found by comparing the circuits of Fig.A.2, and equating the output currents. It is clear that the current generator has no effect, due to the input short circuit, instead the voltage generator (which comprises also the noise of R_{deg}) is referred to the input through the following steps. The output current

from the schematic of Fig.A.2a (note that the resistance seen from the emitter of Q_1 has been approximated with R_E, neglecting the contribution due to the transconductor) is

Figure A.2: Effect of feedback on transistor noise generators.



$$i_o \simeq v_{n,tail} \cdot \frac{g_{m,tail}}{1 + g_{m,tail} R_{deg}} \cdot \frac{g_{m1} R_E}{1 + g_{m1} R_E}$$

while the one from Fig.A.2b is

$$i_o \simeq v_n \cdot \frac{g_{m1}}{1 + g_{m1} R_E}.$$

Equating the results it is found

$$v_n \simeq v_{n,tail} \frac{g_{m1} R_E}{1 + g_{m,tail} R_{deg}}$$

thus

$$\frac{\overline{v_n}^2}{\Delta f} = 4kT\left(r_b + \frac{1}{2g_{m1}}\right)\left(\frac{g_{m1} R_E}{1 + g_{m,tail} R_{deg}}\right)^2$$

A similar result is obtained for the noise coming from the degeneration resistor of the tail transistor, R_{deg}, expressing its equivalent current noise generator:

$$v_n \simeq i_{n,Rdeg} \frac{g_{m1} R_E R_{deg}}{1 + g_{m1} R_{deg}}.$$

that leads to the result

$$\frac{\overline{v_n}^2}{\Delta f} = 4kTR_{deg}\left(\frac{g_{m1}R_E}{1+g_{m,tail}R_{deg}}\right)^2$$

Before considering the degeneration resistor R_E, let's make another observation: since the differential pair, at least at low frequency, has high CMRR, it is of interest the differential noise signal at the input. Under this hypotesis, it is possible to move one of the input voltage generators to the other side, which results in one single voltage generator with doubled PSD as in Fig.3.10b.

Finally, it is the turn of the degeneration resistor R_E. It is not hard to imagine that this resistor contributes only to the output differential noise current, and, thanks to the mentioned high CMRR, it is referred to the input voltage noise generator. The method is the same: the circuits must be compared short circuiting the inputs and equating the output (differential, in this case) currents. The result is that the noise voltage generator of the resistor can be moved unchanged to the input, thus its power summed to the other terms. Another way to see this could be to break the resistor in two halves, considering for each one the noise generator, and referring it, unchanged, to the input: these generators are not independent, because under this hypothesis their phase is correlated, so, after moving them to the same input side, they sum in amplitude, leading to the same equivalent input generator.

List of Figures

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