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CORSO DI LAUREA MAGISTRALE IN
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"Device physics and failure mechanisms of deep submicron gate GaN HEMTs for microwave and millimeter-wave applications"

Relatore: Ch.mo Prof. Enrico Zanoni

Laureando: Andrea Carlotto

ANNO ACCADEMICO 2022 – 2023

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Contents

Abstract

This thesis presents the findings of a comprehensive characterization study on GaN-based, gate-scaled HEMTs for RF applications. The samples considered in the study are Ga-polar devices which differentiate for: (1) the adoption of substrates produced by different device supplier, (2) the presence of a back-barrier, and (3) the aluminum concentration in the back-barrier. The investigation considers performance, stability, and reliability aspects; more in detail, the analysis was focused on the investigation of the deep levels presents in the different epitaxial structures, with the aim of evaluating how the presence of a back-barrier with different Al concentration affected them. For each technology, static and dynamic measurements were conducted on the devices under test; this involved double-pulse, and V_{TH} transient measurements performed stressing the devices both in OFF- and semi-ON-state. The observed results were compared with those reported in the literature to determine the nature and location of the traps responsible for performance variations and identify them. In the end, the results obtained showed that the devices without a back-barrier presented a greater dispersion due to the interaction with the buffer trap states (carbon and iron). On contrary, the devices with a back-barrier were able to effectively screen the traps in buffer, even though other traps were found. Further analysis are required in order to discover the nature of those traps but they seems related to the presence of interface states between the back-barrier and the GaN channel interface. This research provided the first systematic study of the impact of back-barriers on the deep levels in a HEMT devices, providing valuable insight for the optimization of the technology.

Introduction

The progress in semiconductor materials and device development has been remarkable, with a profound impact on society. At the forefront of this advancement has been the continuous integration and development of silicon-based MOSFET devices guided by Moore's law, which predicts a doubling of device density every 18 months. This has been achieved through advanced lithographic tools that enable the production of few-nanometre gate-length transistors, the increase of silicon wafer diameter, and the implementation of innovative device designs to maintain charge control and minimise gate leakage (double-gate FET[1], super-halo ion implantations[2], strain engineering and orientation effects[3]). Looking at the future development of semiconductor devices, there are challenges to overcome in scaling conventional CMOS circuits. Additionally, power dissipation poses a thermal limitation on the size and speed of future processors. Thus, while Si-based CMOS architecture has dominated the industry in terms of chip size and dollar volume, other semiconductor technologies have also made critical advancements. The ability to grow epitaxial layers in a controlled manner, initially through Liquid Phase Epitaxy (LPE) and Vapor Phase Epitaxy (VPE), and then through Metalorganic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE), has played a crucial role in the maturation of the compound semiconductor industry. This development has had a significant impact on both photonics and electronics.

In addition, in recent decades, the growing demand for digital data has driven scientists to seek innovative solutions to enhance the transmission capacity of existing data communication and telecommunication links. In the realm of wireless communication systems, the utilization of micrometer and millimeter-wave spectrum has made possible to attain larger bandwidth communications resulting in communication rates in the range of 30-300 GHz. This can be achieved thanks to the union of Gallium Nitride (GaN), a Wide Band Gap (WBG) material, and High Electron Mobility Transistor (HEMT) structure, that with respect to traditional silicon-based transistor can lead to several advantages in terms of high voltage (high power) and high frequency applications. Research is now going in the direction of scaling the dimensions of such devices to enhance their switching frequency operations. However, when small aspect ratio (ratio

between gate width and gate length) are reached, parasitic effects named as short-channel effects can manifest: they can result in lowering the controllability of the gate contact over the channel, making the carrier velocity saturates due to increasing lateral electric field, reducing the efficiency of the device due to the formation of leakage paths under the channel region, and more [4]. To mitigate such problems, innovative structures has been adopted like back barriers, and doped buffer layers. The aim is to maintain the carriers focused in the channel region and reduce the buffer leakage. However, the implementation of such structures may also introduce traps that can limit the performance of the device and cause the insurgence of stability and reliability issues. For these reasons, significant research efforts are needed. The aim of this thesis is to evaluate the characteristics, and the stability, issues concerning GaN HEMTs with back-barrier. This has been accomplished by utilizing the data gathered during the research activity. The devices provided come from the US company QORVO, which is a partner of the University within the ONR project. On these samples, several tests have been conducted. In particular, they underwent to a series of static and dynamic measurements. This encompassed first of all a preliminary DC analysis and then double-pulse and Vth transient measurements, subjecting the devices to stress conditions in both OFF and semi-ON states. By comparing the outcomes with data from existing literature, we aimed to determine the origin and the placement of the traps contributing to performance degrading and subsequently classify them. Ultimately, the key findings are as follows: CONTROL devices, that are those lacking of a back-barrier, exhibit higher dispersion due to their interaction with trap states within the buffer. Conversely, devices equipped with a back-barrier are successful in isolating these defects, although they may introduce alternative trapping mechanisms, potentially involving interface states. The thesis will be organised as follows:

Chapter 1: A comprehensive review of gallium nitride (GaN), which includes its chemical and electrical properties, highlighting its advantages with respect to traditional semiconductors.

Chapter 2: An in-depth examination of the structure of high-electron mobility transistors (HEMTs) based on gallium nitride, demonstrating how the material properties are leveraged in the operation of these devices.

Chapter 3: An overview of the stability and reliability issues that impact GaN HEMT devices, including an analysis of short-channel effects and proposed structural enhancements.

Chapter 4: Detailed explanations of the structure of the devices used in the experiments followed by a description of the experimental setup adopted to perform the measurements.

Chapter 5: A comprehensive discussion of the experimental results obtained for QORVO devices, covering various aspects such as DC characteristics, double pulse and transient characteristics, and temperature-induced stress.

Chapter 6: The conclusions are traced and the main results obtained discussed.

Chapter 1: Gallium Nitride

Gallium Nitride (GaN) has emerged as a game-changing material for microelectronics applications, revolutionising fields such as optoelectronics, power electronics, and wireless communication due to its unique combination of exceptional properties and superior device performance. In this chapter, we explore the potential of GaN in microelectronics, showcasing its chemical and electrical properties and examining its advantages over traditional semiconductors.

1.1 Beyond the limits of silicon: gallium nitride

From the invention of the first transistor in December 1947, silicon has been the backbone of electronic industry. The progress in microelectronics has led to a better comprehension of the properties of semiconductor materials, and, as a consequence, to an improvement of every electronic device. Indeed, without a deep knowledge of the semiconductor properties, it would not have been possible to manufacture the integrated circuits, the memories, and all the other components, which have allowed the realisation of advanced electronic devices such as computers, smartphones, tablets and televisions. The development of a new technological solution in the electronic field was also crucial for the development and realisation of advanced communication technologies and telecommunications networks.

Silicon has been and still is the semiconductor of choice for the electronic industries; However, even silicon shows certain limitations [5], especially in the field where efficient light emission, high frequency, and high-power operation are required.

These and other constraints prevent Silicon from being a suitable material for the realization of devices for optoelectronic, high frequency and high-power applications. As a consequence, the microelectronics industry has started looking at other materials that offer higher performances, specifically compound semiconductors and Wide Bandgap materials (WBG). What has been done is to move from the IV group of the periodic table where we can find simple semiconductors as Silicon (Si) and Germanium (Ge) to elements of group III and V that can be bond together and form a unique structure,

showing promising properties. Gallium nitride (GaN) and silicon carbide (SiC) are two main examples of WBG. From the performance point of view, respect to traditional semiconductors, they offer several advantages, as reported in the following Figure 1.1:

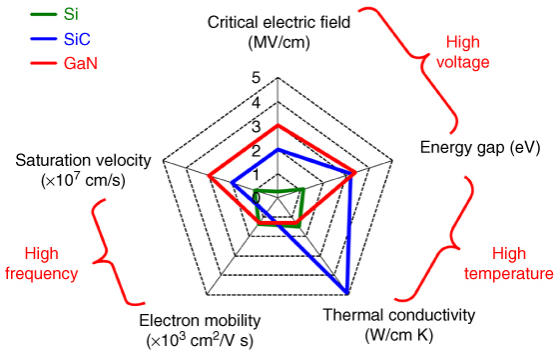


Figure 1.7 Spider plot of the physical and electronic properties of GaN compared with those of Si and SiC.[6]

Gallium Nitride (GaN) is one of the most promising binary compounds at the moment, composed by Gallium (Ga) and Nitrogen (N). In the following a comparison between GaN and Si will make clear the choice of this innovative material.

1.1.1 Optical Properties

First of all, Silicon is an indirect bandgap semiconductor. This can be determined by solving Schroedinger equation for a periodic potential knowing the crystal structure of silicon and in this way finding the relation between energy and momentum which is the Band diagram of the semiconductor, an essential tool that allows to understand the physical properties of the material. The term 'indirect' refers to the fact that in the E-k diagram, as shown in Figure 1.2, the minima of Conduction Band is not aligned with the maxima of Valence Band. For this reason, it is complicated to have a photon emission. Indeed, in order to have a radiative recombination process the energy must be conserved during the transition. Since the maximum and the minimum of the valence and covalence band are not aligned, the momentum change; thus, it is essential that a carrier collides with the crystal lattice, generating a phonon (quanta of crystal lattice vibration) in order to allow the radiative recombination to occurs.

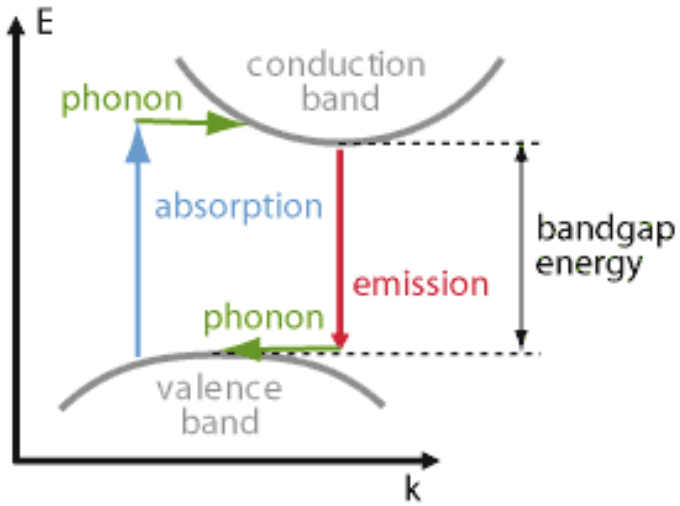


Figure 1.2 Indirect bandgap diagram: in this case additional phonons need to be involved in absorption and emission processes in order to provide the required momentum change of electrons.[7]

On the other hand, thanks to its crystalline structure and its chemical composition, GaN is a direct bandgap semiconductor having the maxima of Valence Band aligned with the minima of Conduction Band as reported in figure 1.3:

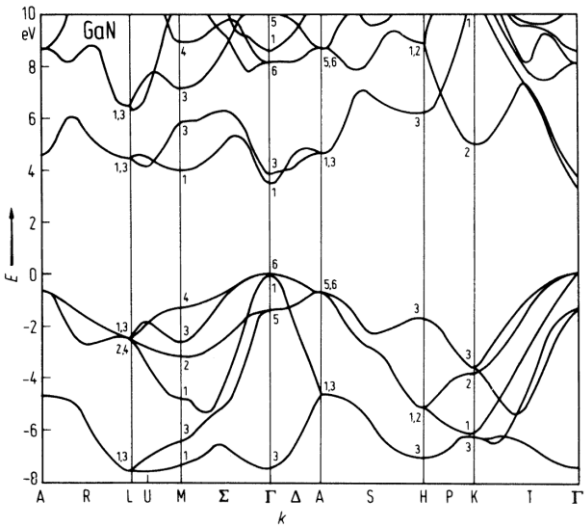


Figure 1.3 Band Structure of GaN (direct-bandgap). Eg = 3.39 eV [8]

The direct-bandgap configuration allows to have recombination between carriers in a more efficient way compared to Silicon; indeed, when a carrier passes from the valence band to the conduction band both energy and momentum are conservated, resulting in a

high probability of having a phenomenon of radiative recombination. This property allows the realization of devices with high efficiency in light emission applications. From the figure 1.3 we can also see, as already anticipated, that the difference between the maxima and minima of the two bands, that is the energy gap, is 3.39 eV. This is a wider bandgap compared to Silicon and this was one of the best advantages that were studied from GaN discovery. There is a relation expressed by the equation 1.1 based on De Broglie hypothesis, that links the Energy Gap with the emission wavelength of the photons emitted by the devices:

$$\lambda = \frac{hc}{\Delta E} \cong \frac{hc}{E_G} \quad (1.1)$$

From this equation we can compare the results obtained for Silicon and GaN:

- $\lambda_{Si} \cong 1107\ nm$ (IR spectra)
- $\lambda_{GaN} \cong 365\ nm$ (UV spectra)

Just comparing the region of the spectrum at which Silicon and GaN emits, we can understand that there is an important difference. With GaN it is possible to access to the most energetic portion of the electromagnetic spectrum in the visible (violet and blue), a region that would have been inaccessible just by utilizing Silicon. This result is important in the realization of white LEDs. There are several strategies to produce white light, but one of the more exploited technique is phosphorus conversion, which entails in coating a GaN-based blue LED with a phosphorus layer. When the GaN LED is activated, it emits high energetic photons that are absorbed by the phosphorus, generating electron-hole pairs. These pairs subsequently recombine, emitting photons predominantly in the yellow region of the visible spectrum, displaying a wide dispersion of colors. The resulting spectrum closely resembles the reference spectrum for white light. [9]

Gallium nitride is commonly alloyed with other elements such as indium or aluminium to form ternary and quaternary alloys. In the case of ternary alloys, where no crystallographic phase change occurs with varying composition, Vegard's law can be applied to predict the semiconductor's properties:

$$a(A_xB_{1-x}C) = x \cdot a\,(AC) + (1-x)\,a(BC) \quad (1.2)$$

This equation represents a weighted average of the lattice constants of the binary compounds involved, and it proves to be valuable in assessing the bandgap of the resulting ternary alloy. By carefully selecting the appropriate materials, and precisely controlling the constituent concentrations, it becomes feasible to create materials that possess an energy bandgap positioned between those of the constituent binary alloys. This technique is also known as bandgap engineering. For instance, when gallium nitride is combined with aluminium nitride, a ternary alloy called AlGaN can be formed, exhibiting a bandgap that falls within the range of 3.4 eV to 6.24 eV. Considering equation 1.2, it becomes evident that, in theory, adopting ternary alloys become possible the creation of LEDs capable of emitting photons at various frequencies, thereby producing different colours of light.

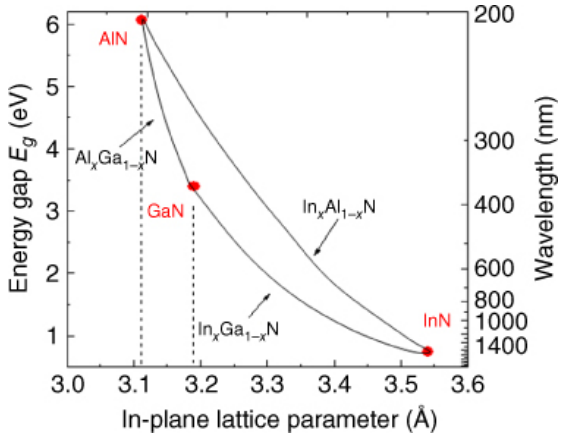


Figure 1.4 Energy band gap of nitride semiconductors (AlN, GaN, InN, and their ternary alloys) as a function on the in-plane lattice parameter. The corresponding wavelength is reported on the right axis. [6]

1.1.2 High-Power behaviour

Furthermore, the maximum electric field that a silicon device can sustain before breaking is only 0.3 $\frac{MV}{cm}$, which means that building high-voltage components (>500-1000 V) requires a larger amount of material resulting in thick components. This is due to the relatively small bandgap of silicon which is E_g = 1.12 eV. As the thickness of the material increases, so does the resistance. Therefore, the applications that require devices able to operate at high power (e.g. power converters) are negatively affected, since it could lead to a reduction in the circuit efficiency. In the recent years, improving the efficiency of

electronic circuit is becoming increasingly important, not only for reducing losses and costs, but also to help in reducing the carbon emissions.

On the other hand, not only the direct bandgap structure of GaN had allowed it to be extensively used in the field of illumination but numerous other important properties had enabled it to excel in various electronic application fields, such as high-power operations. In fact, the wide bandgap (WBG) of the material (E_g = 3.4 eV) results in a high critical electric field (E_{CR} = 3 - 3.75 MV/cm), representing the maximum-field-strength the material can endure without experiencing breakdown. As mentioned before, this high critical field plays a pivotal role in enabling the creation of electronic devices designed to operate at high voltages, while maintaining low on-resistance. These advantages allow WBG to be the best candidate for power conversion applications.

For this and also other purposes, also the impact of temperature on semiconductors must be considered, as it significantly influences carrier generation and, consequently, the electrical properties of devices as well as the ability to operate reliably in stressful environment such as the high-power one. In general, WBG allows to realize devices able to sustain higher temperature than silicon. This is due to the fact that with their bigger bandgap WBG have a smaller intrinsic carrier concentration, because the distance between Valence and Conduction band is higher. As a consequence, the quantity of minority carrier necessary to make the material degenerative is increased and happens at higher temperature respect to traditional semiconductors. This quantity of carriers is referred to as the intrinsic carrier concentration (n_i), and it exhibits an exponential dependence on temperature (T), as shown in the equation 1.3:

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_G}{2kT}} \quad (1.3)$$

Here, k denotes the Boltzmann constant, while N_C and N_V represent, respectively, the density of states in the conduction, and valence bands.

In the following figure 1.5, it is reported a comparison of intrinsic carrier concentration as a function of Temperature for Silicon, Silicon Carbide (SiC) and

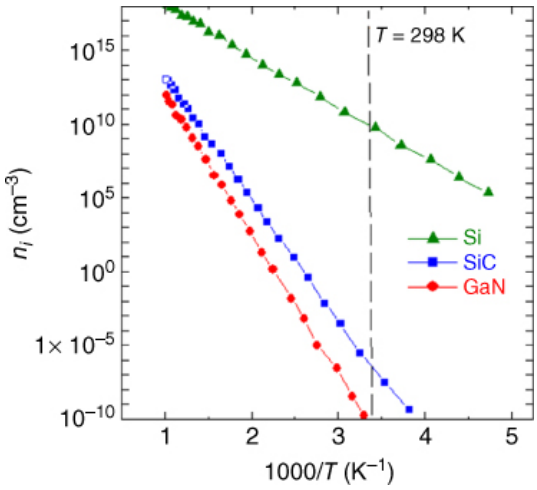


Figure 1.5 Calculated intrinsic carrier concentration ni as a function of reverse of the temperature (1000/T) for GaN. For comparison, the curves of ni for Si and SiC are also reported. The dashed line indicates the room temperature (T = 298 K). [10]

As previously said the intrinsic carrier concentration in Si at temperatures above 300 °C can become comparable to or even exceed intentional dopant concentrations, making the material degenerative. In contrast, SiC and GaN exhibit much lower intrinsic carrier concentrations, making them less susceptible to issues caused by an excessive intrinsic carrier concentration even at elevated temperatures, such as 600 °C. Especially, GaN stands out with an extremely low intrinsic carrier concentration, about 19 orders of magnitude lower than Si at room temperature (T = 298 K).

1.1.4 High-frequency operation

In addition, Silicon exhibits a moderate mobility of 1350 $\frac{cm^2}{V\,s}$ and a relatively low saturation velocity of 700 $\frac{cm}{s}$. These factors limit the maximum frequency at which silicon-based transistors can work (few GHz); Nevertheless, the requirement of some emerging applications in industry, like 5G and 6G telecommunication systems, will need devices able to operate at higher frequencies. Consequently, new materials with higher electron mobility and higher saturation velocity are necessary for the next generation of high-speed electronics.

Another aspect to consider concerning the electrical properties of GaN is undoubtedly the carrier saturation velocity and their mobility within the crystal lattice of

the material. Mobility represents the ability of carriers to move within the material, while saturation velocity is the maximum speed they can attain under the influence of high electric fields. Gallium nitride exhibits a saturation velocity of approximately $2.5 \cdot 10^7 \frac{cm}{s}$, which is nearly three times higher than that of silicon. In general, carriers don't travel at their saturation velocity. When low electric fields are applied the dependence of the saturation velocity on the electric fields can be expressed, in first approximation, by the equation 1.4:

$$v = \mu \cdot E \quad (1.4)$$

However, the dependence between v and E is more complex, as we can see in figure 1.6:

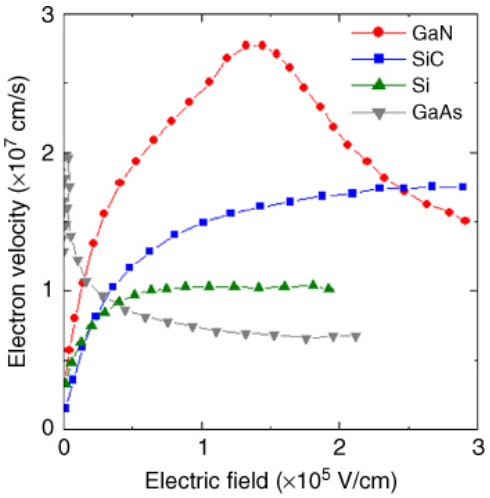


Figure 1.6 Electron velocity as a function of the electric field for GaN. For comparison, the values of the electron velocity of GaAs, Si, and SiC are also reported. [11]

We can see that at first, as the electric field increases, the carrier velocity also increases as carriers are accelerated, showing a linear behaviour. However, beyond a critical electric field, the carrier velocity starts to decrease due to a reduction in the material's mobility, which becomes dominant at high electric field values. This is attributed to the band structure of GaN, where carriers, under very high electric fields, move to higher-energy states in the conduction band. Therefore, the effective mass increases causing a reduction in the carrier mobility, as can be seen from equation 1.5:

$$\mu = \frac{q\,\tau}{m^*} \qquad (1.5)$$

q is the electron charge, τ is the average scattering time, and m* is the effective mass of the carriers. The electron mobility, in GaN, at room temperature is around $1000\ \frac{cm^2}{V \cdot s}$, which is comparable to silicon. However, doping significantly influences mobility, as it increases the concentration of ions and impurities. Therefore, a higher concentration of defects increases the probability of collisions, leading to a reduction in scattering time; thus, to a reduction in the carrier mobility. Scattering time refers to the average time between two electron scattering events. This aspect will be discussed more in detail in the following chapter of the thesis.

1.2 Spontaneous and Piezoelectric polarizations

As already discussed in the previous sections, one of the most promising binary compounds at the moment is Gallium Nitride (GaN), composed by Gallium (Ga) and Nitrogen (N). The two elements are linked through covalent bonds that allow each atom to be tetrahedrally bonded to four atoms of the other type. In addition, an ionic contribution is also present because Ga and N have a large difference in electronegativity, which is a measure of the ability of an atom to attract electrons on its side of the bond. Since Nitrogen has a higher electronegativity than gallium, Ga and N atoms exhibit anionic (+) and cationic (−) characteristics, respectively; this results in a spontaneous polarization oriented along the growth-axis. In fact, while the internal polarization is balanced within the material, an asymmetry emerges at the cut face, resulting in a specific polarization along the growth-axis, known as spontaneous polarization. In III-N materials, the spontaneous polarization values have been reported as $P_{sp,InN} = 0.032\ \frac{C}{m^2}$, $P_{sp,GaN} = 0.029\ \frac{C}{m^2}$ 0.029 and $P_{sp,AlN} = 0.081\ \frac{C}{m^2}$ for InN, GaN, and AlN, respectively, all directed from column III atoms to Nitrogen (see figure 1.7). In addition, the ionicity causes significant changes in the semiconductor properties: it increases the Coulomb interaction between the ions , and the energy of the fundamental gap in the electronic band structure, resulting in a high energy gap of $E_G = 3.39\ eV$ (larger than Silicon: $E_G =$

1.12 eV). Moreover, the enhancement in crystal's cohesive energy owing to the Coulombic interaction between the ions promotes the rock-salt structure comprising atoms with six-fold coordination instead of tetrahedral bonds. In fact, Gallium Nitride, as well as other III-nitride materials such as AlN and InN, possess a stable crystal structure with a high melting point due to the small covalent radius and the strong bonding energy. Generally, they adopt a wurtzite crystal structure which comprises of two hexagonal close-packed sub-lattices interpenetrating each other and shifted along the c-axis (the growth-axis) by 3/8 of the cell height. The wurtzite structure possesses an ABABAB stacking sequence in the <0001> direction, as shown in Figure 1.7. [6]

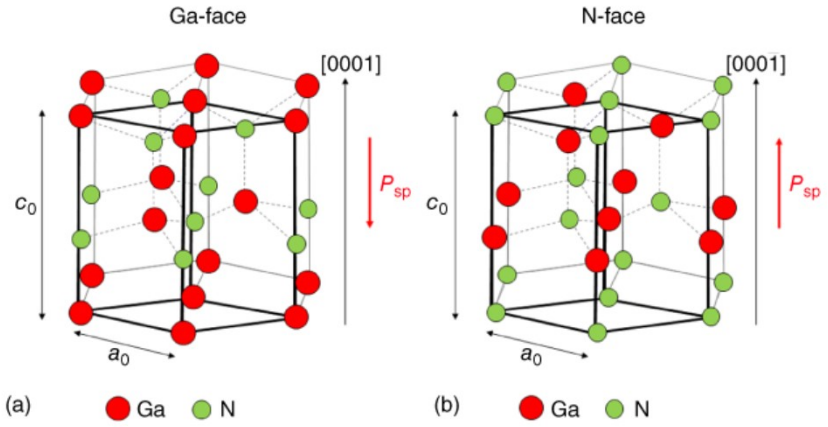


Figure 1.7 Hexagonal crystal structure of GaN (wurtzite) for the Ga-face (a) and for the N-face (b). The bold lines highlight the unit cell, while the dashed lines indicate the GaN bonds. The spontaneous polarization vectors (PSP) are also drawn for the two cases. [6]

Another type of polarization occurs mostly in GaN based heterostructures, where another material like AlGaN or InAlGaN is grown or placed in contact with a GaN substrate. The presence of a mismatch in the lattice constants, between two epitaxial layer generates a new type of polarization known as piezoelectric polarization. Figure 1.8 illustrates how this polarization occurs in nitride semiconductors. In the left figure, the combined internal polarization vectors ($P_1 + P_2 + P_3 + P_4$) cancel out, resulting in zero polarization in a freestanding tetrahedral structure due to the crystal symmetry. However, in the right-hand side of the figure, when the crystal experiences deformation due to lattice mismatch, the angle θ widens under tensile stress, (or the opposite if a compressive stress is applied). As a consequence, the internal electric field becomes unbalanced, leading to the appearance of the piezoelectric field (P_{PE}) according to equation 1.6:

$$P_1 + P_2 + P_3 + P_4 = P_{PE} \qquad (1.6)$$

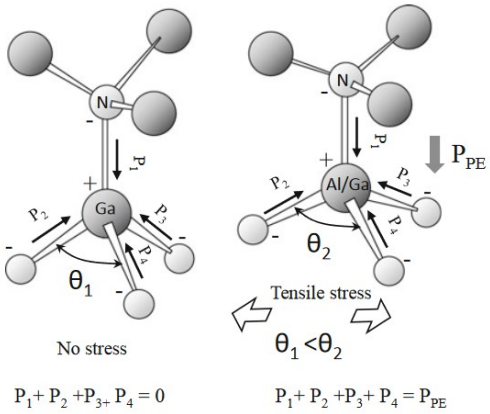


Figure 1.8 The balanced polarization of ionic bonds in the tetrahedron shape (left) cause the unbalance of polarization field under the stress originated to the difference of lattice constant of underlying material. The resultant electric field is called piezo electric one, shown as Ep in the figure (right) [6]

The most remarkable characteristic of Gallium Nitride and nitride semiconductors is the capacity of accumulating free carriers (electrons) at the heterointerface to counterbalance the fixed spontaneous and piezoelectric polarizations, when two WBG semiconductors with different lattice constants are putted together. In Figure 1.9, the theoretically calculated 2DEG (2-Dimensional Electron Gas) density for three types of ternary semiconductor layers coherently grown over GaN is shown.

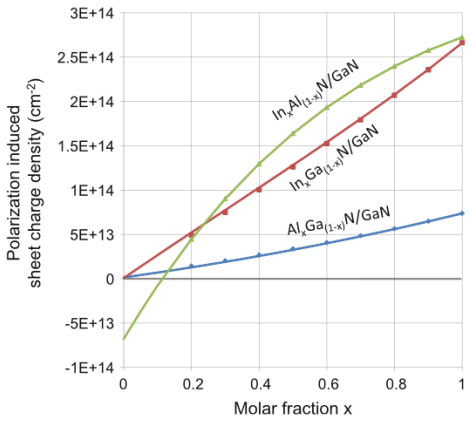


Figure 1.9 Theoretically calculated carrier densities at the heterostructure are calculated caused by spontaneous and piezoelectric polarizations for three ternary alloys of $Al_xGa_{(1-x)}N$, $In_xGa_{(1-x)}N$, and $Al_xIn_{(1-x)}N$, as a function of the their molar fraction x grown over GaN [6]

This high-density 2DEG is extensively utilized in typical nitride-based High Electron Mobility Transistors (HEMTs) since it allows the creation of an electron channel in an undoped material, by exploiting the polarization mechanisms. This feature stands as the most significant advantage of GaN-based Field-Effect Transistors (FETs). [12]

In the second chapter it will be discussed more in detail how these polarization mechanisms, that differentiate GaN from other materials, are exploited for the realization of the High Electron Mobility Transistor (HEMT)

Chapter 2: GaN-based High Electron Mobility Transistor (HEMT)

After presenting the remarkable properties of semiconductor material, and especially Si and GaN, in this chapter the advantages of using HEMT structure based on GaN, are going to be described. These novel types of devices are able to achieve remarkable properties making the devices optimal candidates for high-frequency and high-power applications.

2.1 Introduction to traditional FET devices

The MOSFET is not the only device that can be realized using semiconductor materials for microelectronic applications. In fact, there are numerous variants generally referred to as advanced FET (Field-Effect Transistor) devices. These variants typically involve the use of materials different from Silicon to achieve advanced performance, such as high switching speed, low resistance to improve the efficiency, and high reliability for long-term operation. The basic concept for any FET device is rather straightforward: The device features an active channel, allowing the flow of electrons (or holes) from the source to the drain, which are realized by creating two ohmic contacts. Then there is a third contact which is called gate. By applying a potential to the gate, the conductivity of the channel can be controlled as we can see in Figure 2.1:

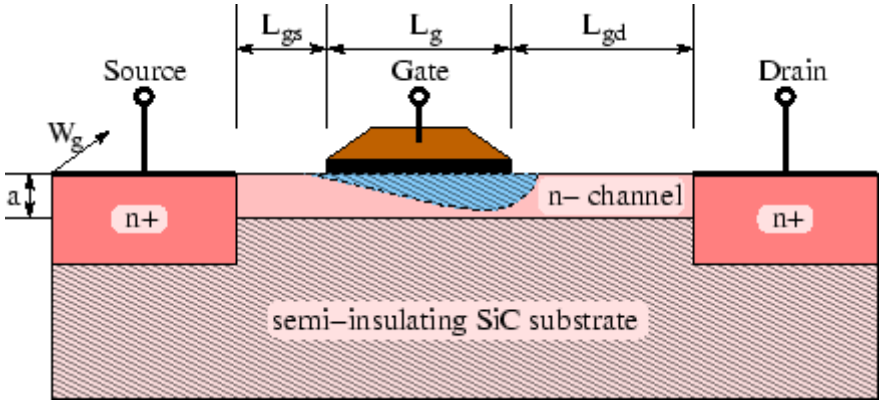


Figure 1.1 Example FET's working principle. In this example it is shown a n-MESFET. The gate metal creates a Shottcky junction. The bias applied to the gate controls the conductivity of the channel, modulating the depth of the space charge region. [13]

It is essential to isolate the gate contact from the channel to prevent current leakage to/from the gate. Various strategies for gate isolation exist; for example, in MOSFET an oxide layer is grown for this purpose.

Other strategies include:

- Schottky barrier (MESFET)
- Reverse-bias pn junction (JFET)
- Heterojunction (HFET)

However, not all structures possess the same characteristics. For this reason, there are quantities called figures of merit used to characterize the performance of devices and quantify their suitability for a particular application.

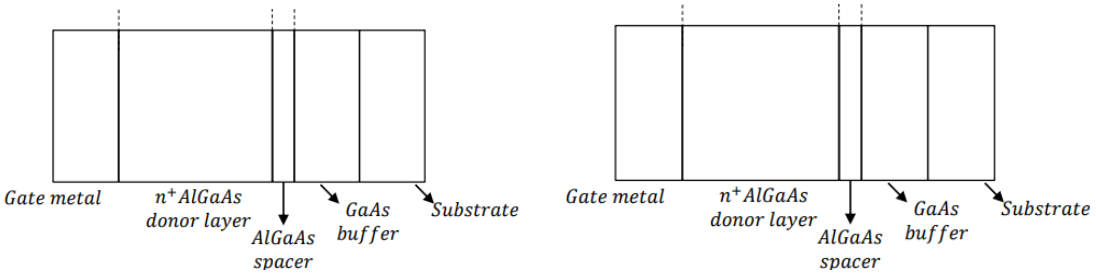
2.2 Advanced FET devices: GaAs HEMTs

In traditional device structure such as, MOSFETs, MESFETs, and JFETs, the active (channel) region consists of a doped semiconductor layer. However, the adoption of doping introduces certain issues. The most important are:

- Transport takes place within the doped semiconductor, leading to scattering with ionized impurities that lower the mobility.
- Not all wide bandgap semiconductors have shallow dopants, potentially resulting in a relatively low carrier density.

In order to avoid the adoption of doping, while maintaining an elevated carrier density, new device structure have been developed such as the Heterostructure FET (HFET) also called High Electron Mobility Transistor (HEMT).

By employing this approach, the doped region (if present) and the channel region are intentionally separated in space. As result, it is possible to create a channel of free electrons with a high concentration of charges without the necessity of introducing dopant; Thus, the elevated mobility of the material is preserved. To better understand the operational principle of HEMT it is better to consider a device based on GaAs. A heterojunction is formed by growing a doped AlGaAs layer above a GaAs film. Two doping strategies can be employed: uniformly doping the entire AlGaAs layer except for a thin film or doping only a thin region of the layer while leaving the rest undoped. Electrons from the doped AlGaAs donor layer migrate into the GaAs layer, creating a dipole layer. As a result, the conduction band bends, generating a quantum well where electrons are trapped, forming the channel, also referred to as the 2DEG (two-dimensional electron gas). The band diagrams of the two approaches are reported in figure 2.2:



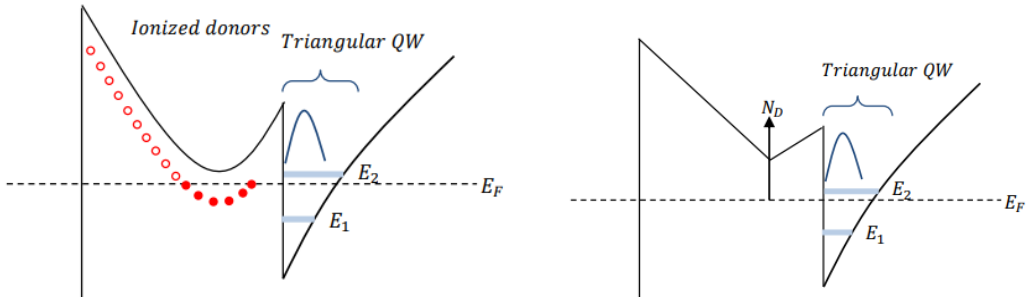


Figure 2.2 at the left the uniform doping approach: this scheme is easier to implement but the amount of charge introduced in the 2DEG is lower. At the right the delta-doping scheme: it introduces a much higher charge in the 2DEG and reduces the risk of introducing a parasitic channel within the barrier [14]

The key advantage of this kind of structure is the suppression of ionized impurity scattering in the channel region since, the dopants are physically separated from the free electrons. Moreover, in contrast with the devices with a doped channel, that suffer from dopant freeze-out at low temperatures, HEMTs maintain a high carrier density even in such conditions, ensuring reliable operation at colder temperatures. In the end, superior materials for the channel can be exploited. Usually, this kind of materials are challenging to process in thick layers; however, HEMTs' reduced channel layer thickness allows their use, further improving device capabilities.

2.3 Advanced FET devices: GaN HEMTs

First of all, an AlxGa1-xN alloy is an hexagonal crystal, as GaN, that can be obtained by replacing a portion of Ga-atoms with Al-atoms in the GaN crystal. The lattice parameter and energy gap of AlxGa1-xN alloys can be customized by varying the Al concentration, according to Vegard's Law, yet presented in section 1.1.

AlGaN/GaN heterostructures are then formed by growing a thin AlxGa1-xN barrier layer on a GaN substrate. The different energy gaps between the materials create an energy discontinuity in the band diagram, while the lattice mismatch induces a tensile strain in the AlxGa1-xN layer to compensate [15]. This strain leads to a piezoelectric polarization along the c-axis, as reported in the following Figure 2.3, to visualize better this mechanism:

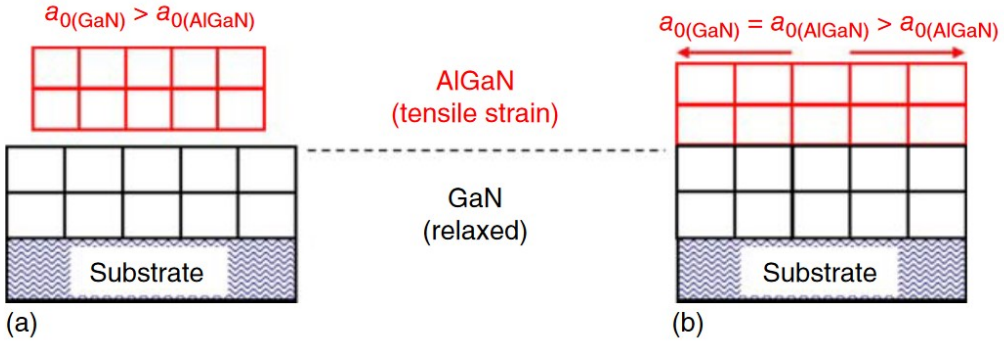


Figure 2.3 Illustrates the schematic of isolated AlGaN and GaN crystals (a) and the resulting AlGaN/GaN heterostructure (b). After the growth of the AlGaN layer on GaN, a tensile strain is induced to compensate for the lattice mismatch between the two materials. [6]

In the strained AlGaN/GaN heterostructure, an induced piezoelectric polarization PPE along the c-axis is given by Equation 2.1:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \qquad (2.1)$$

Here, e_{33} and e_{31} are the piezoelectric coefficients, ε_z represents the strain along the c-axis ($\varepsilon_z = \frac{(c - c_0)}{c_0}$), and $\varepsilon_x = \varepsilon_y = \frac{(a - a_0)}{a_0}$ denote the isotropic in-plane strains. Additionally, a_0 and c_0 represent the equilibrium lattice constants. By the way, the piezoelectric polarization along the c-axis can also be expressed as in equation 2.2:

$$P_{PE} = 2\frac{(a - a_0)}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (2.2)$$

where $C_{13}$and C_{33}represent the elastic constants of the material. The term $\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$ is negative within the entire Al-concentration range commonly used in AlxGa1-xN alloys. Consequently, the piezoelectric polarization will be negative for tensile strain ($a^{AlGaN} > a_0^{AlGaN}$) and positive for compressive strain ($a^{AlGaN} < a_0^{AlGaN}$). For a Ga-face AlGaN/GaN heterostructure with the AlGaN barrier layer under tensile strain, the piezoelectric polarization P_{PE} will be negative and aligned with the spontaneous polarization P_{SP} (directed towards the GaN substrate). The polarization

gradient at the AlGaN/GaN interface results in a polarization-induced charge density as reported in Equation 2.3, which depends on the Al-concentration x:

$$|\sigma\,(x)| = |[P_{SP}(Al_xGa_{1-x}N) + P_{PE}(Al_xGa_{1-x}N) - P_{SP}(GaN)]| \quad (2.3)$$

To maintain charge neutrality, free electrons migrate in order to compensate for the polarization-induced charge density at the AlGaN/GaN interface, leading to the generation of a 2D electron gas (2DEG). This 2DEG accumulates in the potential well formed at the AlGaN/GaN interface as can be seen in Figure 2.4:

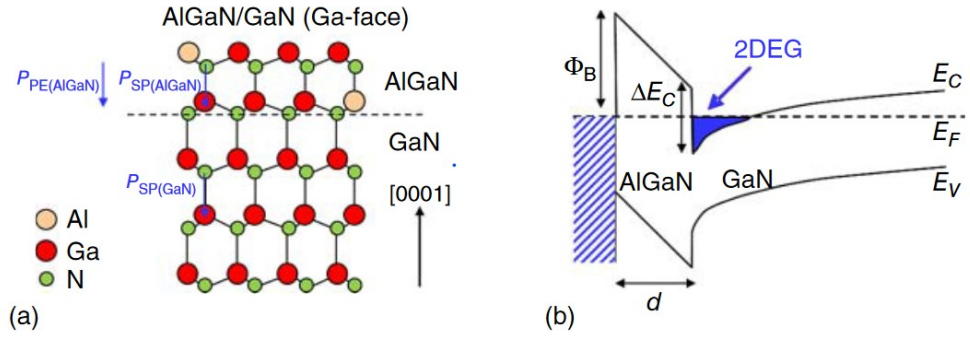


Figure 2.4 (a) This diagram illustrates an AlGaN/GaN heterostructure with the spontaneous and piezoelectric polarization vectors. (b) The schematic band diagram of the AlGaN/GaN heterostructure is shown, with an arrow indicating the presence of a 2DEG (two-dimensional electron gas) in the quantum well at the interface. [6]

Specifically, in an AlGaN/GaN device, a Schottky metal electrode forms on the AlGaN surface, and a bias is applied to modulate the sheet carrier density of the 2DEG, denoted as n_s. In the presence of the Schottky metal, the maximum sheet carrier density of the 2DEG can be expressed as in Equation 2.4:

$$n_s(x) = \frac{\sigma(x)}{q} - \left[\frac{\varepsilon_0\varepsilon_{AlGaN}(x)}{d_{AlGaN}\,q^2}\right] \cdot [q\Phi_B(x) + E_F(x) - \Delta E_c(x)] \quad (2.4)$$

where $d_{AlGaN}$is the thickness of the AlxGa1-xN barrier layer, ε_{AlGaN} is its permittivity, $q\Phi_B$ is the Schottky barrier height of the metal contact, E_F represents the position of the Fermi level with respect to the GaN conduction band edge energy, and ΔE_c is the conduction band offset at the AlGaN/GaN interface. Usually, the 2DEG formed in

AlGaN/GaN heterostructures exhibits sheet carrier density values on the order of $10^{13} cm^{-2}$ and a mobility within the range of $1000 - 2000 \frac{cm^2}{V \cdot s}$ [16].

The HEMT operations are based on the presence of the 2DEG at the AlGaN/GaN heterostructure interface. In Figure 2.5, a schematic cross-section of a device is shown. In a conventional AlGaN/GaN HEMT, the current flows through the 2DEG channel between a source and a drain Ohmic electrode. The current is controlled by applying a negative bias to a Schottky contact serving as the gate electrode of the transistor.

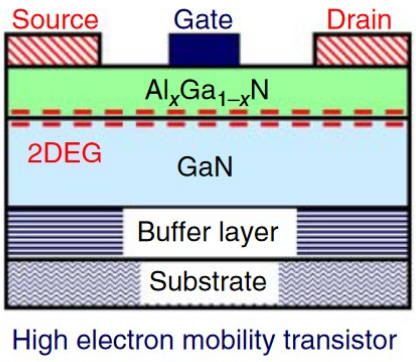


Figure 2.5 Schematic cross-section of a typical AlGaN/GaN HEMT [6]

Since the 2DEG is inherently present in the AlGaN/GaN heterostructure, and the Fermi level at the interface is above the conduction band minimum (as can be seen in figure Figure 2.4 b), this device is considered "normally-on." It means that current flows between the source and drain even when the gate bias is zero (Vg = 0). A typical output IDS−VDS characteristic is illustrated in Figure 2.6:

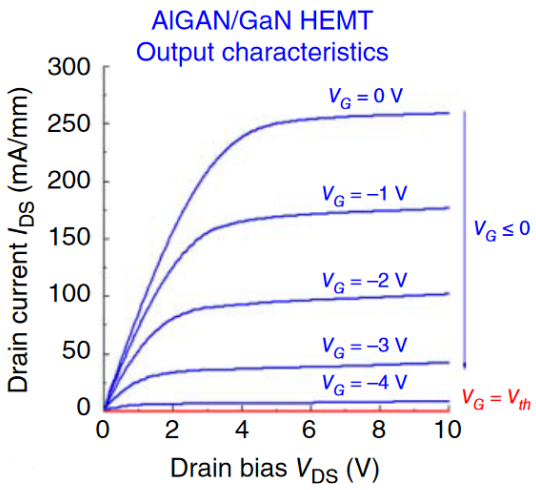


Figure 2.6 typical output IDS-VDS characteristic of a normally-on GaN HEMT [6]

Specifically, The HEMT's output current can be regulated by applying a negative bias to the gate, gradually reducing the current until it reaches the "threshold voltage" (V_{th}). At this point, the Fermi level is pushed below the conduction band edge of the AlGaN, depleting the 2DEG channel. The threshold voltage of an AlGaN/GaN HEMT relies on the heterostructure properties, including AlGaN thickness, doping, and Al concentration. It can be expressed through Equation 2.8:

$$V_{th}(x) = \Phi_B(x) + E_F(x) - \Delta E_c(x) - \left[\frac{qN_D {d_{AlGaN}}^2}{2\varepsilon_0 \varepsilon_{AlGaN}(x)}\right] - \frac{\sigma(x)}{\varepsilon_0 \varepsilon_{AlGaN}(x)} d_{AlGaN} \quad (2.5)$$

Here, N_D represents the doping density of the AlGaN barrier layer expressed in atoms/cm³. The high saturation velocity and mobility of the 2DEG in AlGaN/GaN heterostructures enable rapid switching frequencies in HEMTs.

As we can see from the following equation, valid in general for all the FET devices:

$$f_T = \frac{v_s}{\pi L} = \frac{1}{\pi \tau} \quad (2.6)$$

where v_s is the saturation velocity of electrons, and $\tau = \frac{L}{v_s}$ represents the transit time for electrons to travel the gate's length at saturation velocity, to achieve high-

frequency operation, the transit time (τ) between the source-drain spacing (L_{SD}) must be minimized. The cutoff frequency (f_T) expressed by Equation 2.6 can be rewritten in terms of transconductance (g_m) and gate capacitance (C_g) as in Equation 2.7:

$$f_T = \frac{g_m}{2\pi C_g} \qquad (2.7)$$

Utilizing the saturation electron velocity of GaN, Equation 2.6 indicates that submicron gate HEMTs are capable of operating in the millimeter-wave (mmW) frequency range and that are suitable for Radio-frequency (RF) and telecommunication applications.

2.4 Johnson's figures of merit

In microwave transistors for telecommunication applications, one of the key figures of merit is the unity gain cutoff frequency, that is the frequency at which current gain becomes unity (fT). Its expression is reported by Equation 2.6. This equation demonstrates that to maintain high-frequency operation, it is essential to minimize the transit time, and one way this could be done is by properly scaling the device's dimension (reduce gate length). In practical cases, the unity gain cutoff frequency is typically lower with respect to the one predicted by the above equation due to parasitic capacitances (such as gate fringing capacitance, interelectrode capacitances, etc.) and other parasitic effects.

In addition, each semiconductor material has a critical electric field ($Ecrit$), that represent the maximum field the material can withstand before experiencing breakdown. Therefore, there is a maximum value for VDS (drain-source voltage), denoted as $V_{DS,max}$, which is given by Equation 2.8:

$$V_{DS,max} = E_{crit} \cdot L_{DS} \qquad (2.8)$$

Where L_{DS} is the physical distance between Drain and Source.

In the end, the Johnson figure of merit ($JFoM$) is the product of the maximum transit frequency and the maximum voltage for a given drain-source distance. It can be expressed as in the following Equation 2.9:

$$JFoM = f_T \cdot V_{DS,max} = \frac{v_s}{2\pi L_{DS}} E_{crit} \cdot L_{DS} = \frac{E_{crit} \cdot v_s}{2\pi} \qquad (2.9)$$

The Johnson figure of merit offers valuable insights and considerations: it relies on material parameters, making it ideal for identifying novel semiconductors suitable for high-frequency operation. It is clear also that there exists an inverse relationship between breakdown voltage and cutoff frequency: High-frequency devices have lower breakdown voltages compared to transistors operating at lower frequencies. In the end, JFoM effectively facilitates the comparison of different material systems for high-power and high-frequency applications. It aids in determining the best material to achieve specific performance requirements [17].

In the following table 2.1 a comparison is made between various materials in order to see the advantages in terms of JFoM. The elevated JFOM and the remarkable electrical properties makes GaN an excellent material for the realization of high-power high frequency FET devices.

Material	E_G(eV)	ε_r	μ (cm²/Vs)	$\mathcal{E}_{crit}$ (MV/cm)	v_s (x10^7 cm/s)	κ_{th} (W/cmK)
Si	1.12	11.7	1440	0.3	1	1.3
GaAs	1.42	12.9	9400	0.4	0.9	0.55
GaN	3.4	8.9	1400	3.75	2.4	2.5
4H-SiC	3.23	9.66	950	2.5	2	3.7
AlN	6.2	8.5	450	15	1.4	2.85
Diamond	5.5	5.7	4500	10	2.3	23
β-Ga_2O_3	4.9	10	250	8	1.1	0.1-0.3

Table 2.1 The table presents the key electrical properties of silicon, wide bandgap semiconductors, and ultra-wide bandgap semiconductors. It is evident that the significant improvement in the Johnson figure of merit (JFoM) for wide bandgap semiconductors mainly relies on E_crit (critical electric field). However, even ultra-wide bandgap materials achieve a JFoM that is only marginally greater than three times that of GaN, indicating that field engineering alone is approaching its limits in enhancing power performances [12].

2.5 Epitaxial Structure Implementations

The epitaxial structures of GaN HEMTs, usually, are composed of several layers, that are substrate, nucleation layer, buffer layer, barrier layer and cap layer. These layers are grown sequentially on top of a substrate using either metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) techniques. MOCVD and MBE are two popular epitaxial growth techniques used to deposit thin films of crystalline materials on a substrate with precise control over the atomic arrangement and thickness. These techniques are extensively employed in the fabrication of advanced semiconductor devices, including GaN-based transistors. MOCVD uses metal organic precursors transported by a carrier gas, while MBE operates in ultra-high vacuum conditions, depositing atoms or molecules on a heated substrate thanks to atomic and molecular beams.

Thanks to these two and other techniques, several structures are implemented in the HEMT, starting form a substrate till reach the core of the HEMT structure which is the GaN/AlGaN heterojunction. The growth sequence from bottom to top typically includes:

2.5.1 Substrate

The substrate is a crucial component in the fabrication of semiconductor-based devices, as it serves as the foundation for all other layers. The choice of substrate significantly impacts production costs and the overall device quality. Four common materials are used as substrates for GaN HEMTs:

- Silicon: Suitable for cost-effective devices due to its large area capacity (up to 12”). However, it has a significant lattice mismatch with GaN, leading to dislocation concentration and potential cracking. Strain management techniques are necessary for silicon substrates.

- Sapphire: Another cost-effective option, with a significant lattice mismatch to GaN. It introduces compressive strain and requires dislocation mitigation techniques similar to silicon. Sapphire also has an extremely low thermal

expansion coefficient and may benefit from flip-chip bonding for better heat transfer.

- Silicon carbide (SiC): A highly desirable substrate due to its high thermal conductivity, allowing efficient heat transfer and reducing the need for elaborate cooling systems. This enables smaller electronic devices and minimizes electromagnetic interference (EMI) issues. However, SiC substrates are expensive, and current fabrication techniques limit the achievable area.

- Gallium nitride (GaN): Offers the least amount of dislocation, (no lattice mismatch), making it the preferred substrate for high-quality GaN devices. However, GaN substrates have high production costs and limited achievable area, leading to very expensive devices. Despite this, they offer superior performance.

The choice of the appropriate substrate depends on device architecture and desired performance, with each material having distinct advantages and limitations as reported in the following table 3.1[18]:

Material	Crystalline structure	Typical surface orientation	In-plane lattice constant (nm)	In-plane thermal expansion coefficient (K^{-1})
GaN	Hexagonal	*c*-Plane	0.3189 [62]	5.6×10^{-6}
Sapphire	Rhombohedral	*c*-Plane	0.476 [62]	7.3×10^{-6} [61]
SiC	Hexagonal	*c*-Plane	0.308 [62]	4.5×10^{-6} [61]
Si	Cubic	{111}	0.384	3.6×10^{-6}

Table 3.1 Crystalline data of sapphire, SiC, and Si which are important for epitaxial growth.

2.5.2 Nucleation layer

The nucleation layer is a thin initial layer that is grown on the substrate before the deposition of other GaN-based layers. The main purpose of the nucleation layer is to facilitate the heteroepitaxial growth of subsequent layers and improve the overall crystal quality of the device. The choice of the nucleation layer material is critical because it

needs to accommodate the lattice mismatch between the substrate and the GaN layers. GaN has a significantly different lattice constant compared to common substrate materials like sapphire, silicon, and silicon carbide. This lattice mismatch can lead to defects and dislocations at the interface if not properly managed. In this way, by carefully selecting the nucleation layer material and its thickness, it is possible to minimize lattice mismatch between the substrate and GaN layers, helping in stress relaxation during growth, preventing the propagation of defects and improving the structural integrity of the device. Common materials used as nucleation layers in GaN HEMTs include AlN (aluminum nitride) and low-temperature GaN. Both materials have similar lattice constants to GaN, making them suitable choices to minimize lattice mismatch.

2.5.3 Buffer layer

The buffer layer is realised by growing a thick film of high-quality GaN, on top of the nucleation layer. This is done to enhances the performance and reliability of the GaN-based devices by providing a higher-quality platform for the growth of the active layers, preventing the propagation of dislocations from the nucleation layer to the active layer. In addition, to improve the carrier confinement, the buffer layer can also be engineered to control the electron confinement in the device channel. This can be achieved by incorporating acceptor-type dopants like carbon (C) or iron (Fe) to increase resistivity or by introducing a back-barrier structure to further enhance electron confinement [19]. Usually part of the buffer is dedicated to the channel. GaN channel is an undoped film where 2DEG form. It is left undoped in order to preserve the high mobility of GaN. , the channel thickness involves a trade-off between electron confinement and trapping effects.

2.5.4 Barrier layer and cap layer

For AlGaN-based devices, using ultrathin Al-rich materials in the millimiterwave (mmW) range is preferred to avoid gate recess, which can impact device reliability. The thickness and alloy composition influence mechanical strain, piezoelectric polarization, and the density of the two-dimensional electron gas (2DEG). Usually, an additional final layer is used: the cap layer that often is made of aluminum nitride (AlN). It is applied to

prevent stress relaxation at the heterointerface of the Al-rich barrier/GaN channel and passivate surface states, reducing dispersion.

To better visualize the structure, an example is reported in Figure 3.1, comparing the theoretical cross-section and the one imaged by a real Transmission Electron Microscope:

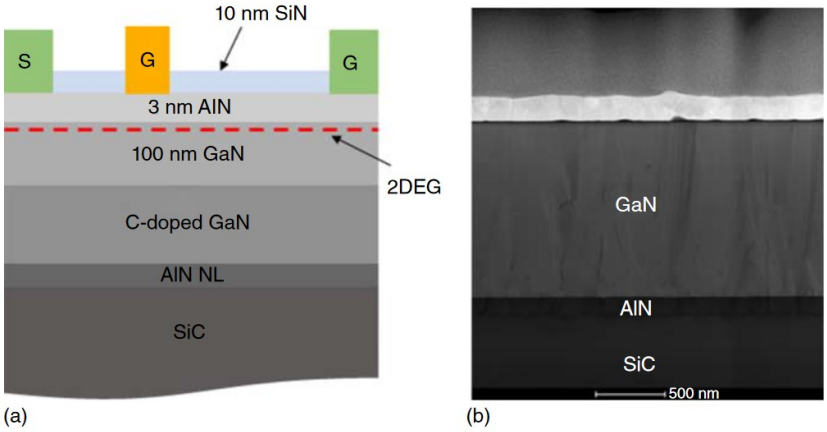


Figure 3.1 Cross section (a) and transmission electron microscopy (TEM) of the MOCVD [6]

Chapter 3: Stability and Reliability issues

This chapter starts with a detailed description of the main issues affecting the technology is presented: this involves stability and reliability issues as well as short channel effects. The latter are parasitic effects that manifest with a reduction in controllability of the channel, the saturation of the carrier velocity due to the lateral electric field, the presence of leakage paths below the channel, and the drain-induced barrier lowering (DIBL).

In order to mitigate stability and reliability issues, and short channel effects research is now focusing on the development of new innovative structures. In particular, to diminish short channel effect the following strategies has been considered: growth of N-polar GaN structures, use of novel materials (AlN, ScAlN, InAlN, and InAlGaN) for the barrier layer, use of doping in the buffer, usually C and/or Fe, and implementations of back barriers to obtain a better carrier confinement in the channel region. Hower, these promising structures are not able to completely eliminate the stability (temporary) and reliability (permanent) issues which degrade the device performances. In order to have a real development in the technology it is essential to understand the presence and the root causes of this problems.

3.2 Stability and Reliability Issues

GaN-based electronic devices have revolutionized power, frequency, and efficiency, outperforming Si- and GaAs-based devices. Ensuring successful commercialization requires reliable operation alongside enhanced performance and cost-effectiveness. Stability and reliability issues have been major concerns in GaN electronics, leading to extensive research to understand and mitigate them, achieving short-term and long-term operational success. The presence of defects that may act as traps in GaN heterostructures are mainly caused by: foreign substrates, that introduces dislocations; caused by the lattice mismatch between the layers; addition of element as

dopant, that may act as traps sites; and epitaxial structures that can introduces new failure mechanisms. For example, Iron and Carbon doping in the buffer layer can from one side enhance the electron confinement in the channel but at the same time they increase the trapping activity, as well as the increasing concentration of aluminum in the barrier layer can from one hand improve the confinement and on the other enhance the presence of surface states. Nevertheless, significant research efforts have improved the reliability of RF GaN HEMTs and monolithic microwave-integrated circuits (MMICs), providing a better understanding of dispersion effects, failure modes, electric field concentration, and heat distribution. This stability and reliability studies relies on monitoring the device failure rate under application-specific conditions and environment. Stability issues refers to recoverable changes in the device electrical characteristics primarily due to trapping effects, while reliability refers to unrecoverable device failure that can occur through two modes gradual changes in electrical parameters over time and sudden catastrophic failure or burnout.

3.2.1 Stability issues, related to trapping effects

Initially, also due to the immature growth technology, stability issues emerged as a significant concern in AlGaN/GaN HEMTs. The most common effects are referred to the temporal variation of electrical parameters such as the drain current I_D (current collapse), threshold voltage V_{th}(threshold voltage shift), transconductance g_m, and ON-resistance R_{ON}. Another common reliability issue consists in the presence of kink, which correspond to a sudden increment in the drain current. All these effects result from the capture and emission of carriers by electrically active defects (traps), that are present in different regions of the device. During the capture process, a free carrier loses its energy and becomes localized by the defect site, characterized by its density, energy level in the semiconductor bandgap, and capture cross-section. On contrary, in the emission process, the carrier needs to acquire sufficient energy to overcome the energy barrier defined by the defect level, and the minimum of the conduction band, for electrons, or the maximum of the valence band for holes. As a result, the emission process and the associated emission time constant are typically much longer than the capture process, as the latter mainly depends on the availability of free carriers. Despite significant improvements in

growth quality, III-N heterostructures still exhibit relatively high densities of bulk defects and surface/interface states. These defects include intentionally or unintentionally introduced impurities like C or Fe in the buffer layers, extended crystallographic defects like dislocations, and point defects such as interstitials, vacancies, or antisites. For what concerns the location, the presence of traps under the gate region typically leads to changes in the threshold voltage that results in a reduction of the drain current (current collapse), whereas variations in the transconductance and on resistance are often associated with traps in the gate-to-drain access region [20].

In general, HEMT have a low concentration of holes; thus, the stability issues are mainly related to trapping or detrapping of electrons. Considering trapping of electrons under the gate region, the trapping of electrons directly influences the threshold voltage of the device. Indeed, if acceptor-like-traps are considered, the trapping activity lead a to the formation of a small depletion region that disperses charges. As a result, the negative voltage required at the gate to fully deplete the channel is reduced causing a variation in the voltage shift called threshold voltage shift. The voltage at which the channel is fully depleted is the threshold voltage V_{th} which for GaN HEMT devices is usually negative (normally-on devices, as discussed in section 2.2. If we consider traps located between the gate and drain regions, what primary can be observed is a variation in the ON-resistance of the device, while the threshold voltage remains almost constant. This happens because of a mechanism called “virtual gate”. To better explain it lets analyse the case where we have only surface defects.

The degradation of drain current that occurs is also known as frequency dispersion effect because the reduction of the current is higher as the switching frequency from the OFF to the ON-state is increased. In this case, the surface traps located in the gate to drain access region are considered primarily responsible for this phenomenon. When the gate voltage experiences high-frequency excursions, the surface levels fail to follow the imposed variations, resulting in a decrease in current of the device. The theorized explanation is as follows: in the off-state bias condition, a high gate-to-drain voltage induces the injection of electrons into surface states from the gate edge. The high density of surface traps allows for electron redistribution through hopping towards the drain, causing negative charge to extend over a long region from the gate edge until a steady-state condition is achieved due to electrostatic feedback of the accumulated negative

charge. These electrons create the "virtual gate" effect, expanding the depletion region of the two-dimensional electron gas (2DEG) channel. In fact, the phenomenon can be modelled with a second gate, called a virtual gate, in series with the real gate. It can be understood that the potential of the real gate is controlled by the applied voltage, while the potential of the virtual gate is controlled by the level of trapped charge. When the gate bias is switched to the on-state, the trapped electrons cannot be immediately removed (the channel formation speed is greater than the de-trapping speed), and the extended virtual gate section of the channel remains depleted for a period determined by the characteristic emission time constant. The dynamic emission of electrons from surface/interface states, leads to a transient change in drain current, resulting in a dynamic variation in ON-resistance that increases and a consequent diminishing in peak transconductance [21]. In this way the output current is reduced since the slope of the characteristic goes as $\sim \frac{1}{R_{ON}}$.

The last effect related to trapping is called kink effect. The term "kink" refers to the phenomenon which manifests with a sudden increase in drain current under DC conditions resulting from the application of high Drain-Source voltages. In fact, increasing the sweep of the voltage V_{DS} creates a distortion in the initial part of the saturation region of the output characteristic, caused by the drop in current, which would not occur with a smaller sweep. This happen because, when the sweep of the voltage V_{DS} increase, from a certain point there is an immediate liberation of charges that were trapped by defects. This degradation of the DC characteristics is considered to be related to the presence of traps, for example in the buffer layer, that when activated by the high electric field, capture electrons, resulting in a decrease in current. This leads to a decrease in charge carriers in the channel and, therefore, a reduction in current until a certain voltage is reached. Under that condition there is a sudden release of the trapped electrons. Another interpretation from Meneghesso et al., proposed that the kink could be caused by intra-band impact ionization in the buffer layer, involving electrons trapped in acceptor-like deep levels with energies 0.9 eV above the valence band of GaN. Nevertheless, in RF devices, the electric field is usually not sufficient to induce impact ionization; thus, the most accredited hypothesis associates the kink with trapping and detrapping of electrons The trapping behavior of GaN-based HEMTs can be rapidly assessed using pulsed $I_D - V_D$ and $I_D - V_G$ characterization[22], also known as pulsed IV or double pulse measurements, where the I–V characteristics are measured in gate and drain-pulsed mode

and compared to DC characteristics. An example is shown in Figure 3.2 b,c, which displays the output and transfer characteristics of an RF AlGaN/GaN HEMT before and after off-state stressing. While stress-induced positive V_{th} shift was observed from DC measurements (Figure 3.2c), indicating trap generation under the gate, pulsed gate-lag measurement (inset of the left panel) clearly depicts dynamic $R_{DS,ON}$ degradation, suggesting trap generation in the gate-to-drain access region. To gain a more comprehensive understanding of trapping effects, a dual-channel pulsing system with different sets of quiescent bias conditions, known as drain-lag measurement, can be employed [23]. Despite the effectiveness of pulsed I–V characterization, these techniques do not provide specific information about the properties of traps responsible for device degradation under stressing.

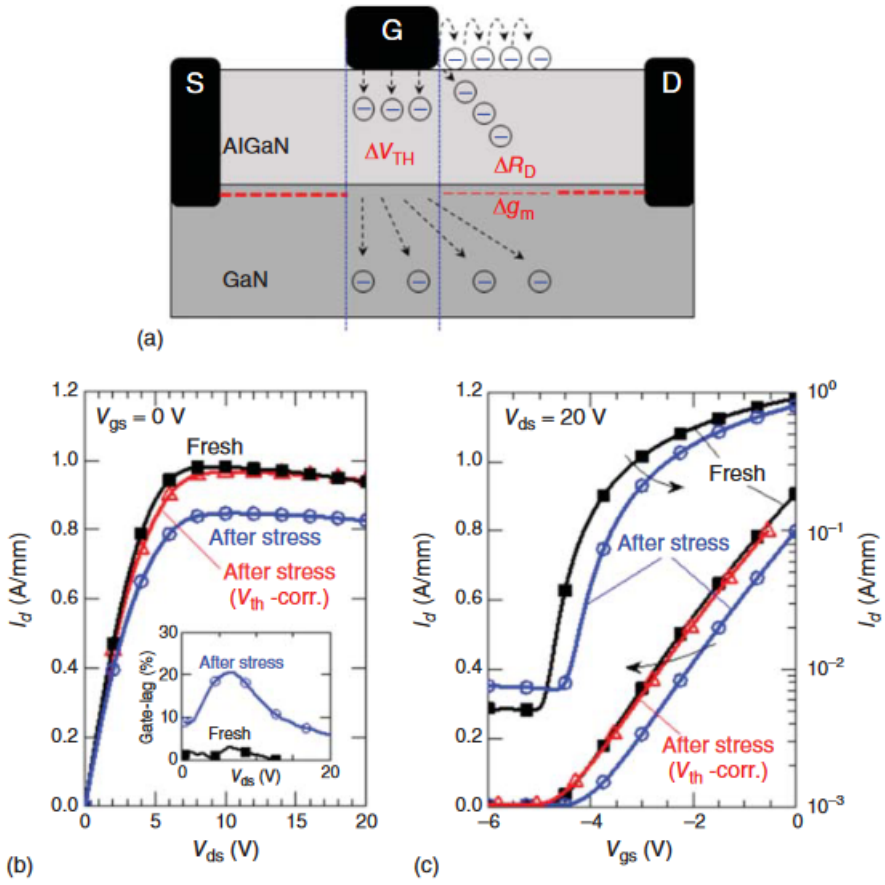


Figure 3.2 (a) A diagram illustrating surface and bulk traps in the AlGaN barrier and GaN buffer layers, affecting Vth, RD, and gm. (b) Output characteristics of an AlGaN/GaN HEMT before and after off-state stress.(c) Transfer characteristics of the same AlGaN/GaN HEMT before and after the off-state stress. After correcting the I–V characteristics for Vth shift, significant degradation of R_{ON} is evident in the linear part of the ID–VD characteristic. Furthermore, a much stronger degradation of dynamic R_{ON} is observed from the gate-lag measurement before and after OFF-state stress (inset)[24]

To mitigate trap-related phenomena, particularly the frequency dispersion caused by surface traps, various solutions can be employed. The most commonly used approach is passivation, which involves depositing an insulating film, typically Silicon Nitride (Si_3N_4). This creates a nearly optimal dielectric/semiconductor interface that neutralizes surface charge arising from dangling bonds, surface defects, and residual charges generated by lattice disruptions. However, uniform results are not always guaranteed, making the deposition process and the quality of materials and surfaces crucial for the device's proper functioning. Nevertheless, improvements in final characteristics are typically achieved, depending on the frequency.

Another technique employed is the use of a field plate, a gate shaped like a T or Γ that partially covers the gate-drain region. This redistributes the electric field between the gate and drain, which is the primary cause of charge migration from the gate to traps. This improvement in the metallization helps in limiting the peak field above the gate and distributes it, to a lesser extent, across the entire extension of the field plate. A third method to mitigate surface effects is gate recess, a technique that involves moving the barrier layer deeper by inserting additional layers of AlGaN or GaN. This effectively distances the surface from the channel [25].

3.2.2 Stability issue and device degradation mechanisms

In addition to charge trapping, there are permanent degradation mechanisms in devices fabricated in GaN, primarily attributed to the high electric fields that can be developped between the gate and drain. These fields can lead to the deterioration of the crystalline structure of the materials, with negative consequences for the device operations. Specifically, the elevated electric fields achievable due to the small device dimensions can give rise to degradation mechanisms related to the presence of a strong inverse piezoelectric effect (gate edge degradation) and hot electrons (degradation due to hot electrons).

An important degradation mechanism known as “gate-edge degradation” was identified through tests conducted on GaN HEMT devices by applying high negative voltages to the gate, maintaining the device in the OFF-state (avoiding the formation of a carrier-conducting channel) [26]. Specifically, this degradation involves a catastrophic,

sudden, and irreversible increase in gate leakage currents (I_G), accompanied by a slight and more gradual degradation of DC characteristics such as a decrease in drain currents (I_D), transconductance (g_m), and an increase in drain resistance (R_D). The voltage value at which degradation begins is generally referred to as the critical voltage ($V_{critical}$). Electroluminescence measurements have evidenced that the sudden increase in leakage current happens simultaneously with an increment of electroluminescence emission. This increment in the number of photons emitted is caused by the formation of hot spots, which are localized regions emitting an elevated number of photons, along the gate edges, these emission spots are attributed to localized defects formed during reverse bias step-stress tests in the crystalline lattice. Their origin is attributed to the inverse piezoelectric effect (IPE), which manifests when an intense longitudinal electric field is applied to the device (usually, there is an elevated potential difference between gate and drain). According to this hypothesis the inverse piezoelectric effect introduces additional tensile stress to the AlGaN barrier with respect to the one already presents due to the lattice mismatch between the strained AlGaN, and the relaxed GaN layer. Thus, the elastic energy of the barrier increases, and if it surpasses a critical value, crystallographic defects can form. Therefore, an increase in the leakage facilitating tunnelling between the gate and the channel through the AlGaN barrier, and these defects can become traps for electrons (degrading the DC characteristics). The defects formed in the lattice provide a path for carriers and have the equivalent effect of lowering the Schottky barrier height of the gate (percolative paths).

From environmental studies it was also noticed the environment contribute into enhancing the gate edge degradation. Pits were found to contain gallium and aluminum oxides in the form of oxygen (O), probably introduced in the device structure as part of the epitaxial fabrication process. However, moisture's role, rather than O, was found to be pivotal in the degradation process. Experiments showed that moisture clearly enhanced pit formation, leading to the hypothesis of moisture-induced electrochemical oxidation causing pits at the gate's edge. Connections were also drawn between pit formation and material quality. Pits were observed to nucleate at threading dislocations with a screw component in AlGaN/GaN HEMTs on Si, characterized by a relatively high density of dislocations due to the great lattice mismatch. Under high reverse gate bias conditions, threading dislocations migrated toward the gate edges, resulting in higher pit density and

hastened device degradation. Mitigating this failure mode involves effective electric field management through proper field plate design, addressing material quality to manage traps and dislocations, minimizing residual moisture, and ensuring a highly hermetic passivation [27]. Another common degradation phenomenon affecting HEMT is named “hot electrons” degradation. Early on, the degradation pattern in the ON -state closely matched that of the OFF -state. However, detailed ON -state studies were complicated by device self-heating. Increasing structural degradation was observed along the gate finger's edge toward the device's center, where the temperature is highest and studies on nominally identical devices under closely matched junction temperature and electric field conditions showed increased I_D change under ON -state stress compared to OFF -state stress, suggesting a different mechanism of degradation.

In fact, by biasing a device in the saturation region of operation (ON state) and subjecting it to high drain-source voltages, the resulting strong electric field can give rise to the formation of hot electrons in the channel. Hot electrons are highly accelerated electrons that interact with the lattice, causing deformation and generating trap states. Their presence can be detrimental to the device, leading to degradation and the formation of traps and defects in the lattice. The high energies attained by these electrons, strongly accelerated by the electric field, enable them to generate electron-hole pairs through impact ionization upon interacting with the lattice. This phenomenon is also known as avalanche multiplication, as the electrons and holes generated from one collision are accelerated by the electric field and can acquire enough energy to ionize other atoms. The secondary carriers thus created are collected at the drain alongside the primary carriers, while the holes are accelerated toward the source and the gate. Given that impact ionization occurs in the region where the electric field is highest, near the Drain-side of the Gate, the majority of the produced holes are drawn toward the Gate by the electric field. Hot electrons can generate traps, consequently increasing current collapse and frequency dispersion. They can also become trapped in the surface, GaN, or AlGaN due to pre-existing traps, modifying the internal electric field and altering performance.

3.3 Short Channel Effects

Even from section 2.1 it was possible to understand that the unity gain cut-off frequency becomes greater when device dimensions are reduced, enlarging the bandwidth and the switching frequency operation of the device. To enhance HEMT frequency performance through transistor scaling, it's essential to maintain the aspect ratio $\frac{L_G}{d}$, where gate length (L_G) to gate-to-channel distance (d), while reducing resistances, capacitances and conductance (Figure 3.4).

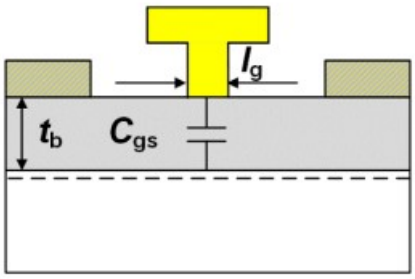


Figure 3.4 Guiding principle of transistor scaling [28]

In fact, considering the following equations:

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{v}{2\pi L_G} \qquad (3.1)$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_i + R_G + R_S)g_{ds} + 2\pi f_T C_{gd} R_G}} \qquad (3.2)$$

$$C_{gs} \sim \frac{\varepsilon}{t_B} L_G \qquad (3.3) \qquad g_{ds} = \frac{q\mu n_s(t_B)}{L_G} \qquad (3.4) \qquad g_m = \frac{\varepsilon}{t_B} v \qquad (3.5)$$

It is possible to understand that high frequency optimization involves [28]:

- Down-scaling the gate length (to reduce C_{gs})
- Down-scaling the barrier thickness (to reduce g_{ds} and increase g_m)
- Improve the electron confinement (to reduce g_{ds})
- Improve electron transport properties (to increase f_T and g_m)

In simple terms, doubling the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) requires halving the lateral and vertical dimensions while reducing resistances per unit gate width (in Ω·mm) by half and doubling conductances per unit gate width (in $\frac{S}{mm}$). This scaling approach ensures that the electrostatic potential profile (and consequently the behaviour of electrons) within the transistor remains consistent. The channel aspect ratio, represented as the ratio of gate length (L_G) to gate-to-channel distance (d), i.e., $\frac{L_G}{d}$, serves as a structural parameter to gauge transistor scaling behavior. A small channel aspect ratio compromises the gate's control over drain current due to incomplete electrostatic isolation between the source and drain. This results in reduced transconductance (g_m), negative threshold voltage (Vth) shifts, increased drain-induced barrier lowering (DIBL), and amplified output conductance (g_d). These phenomena collectively termed "short-channel effects" are notably observed in ultrashort gate HEMTs with gate lengths below 100 nm. The requirement to avert severe short-channel effects has been both theoretically (Awano et al., 1989) and experimentally (Jessen et al., 2007) confirmed. It's been shown that an aspect ratio of Lg/d ≥ 5 is necessary to mitigate these effects. Short-channel effects pose significant constraints on high-frequency transistor scaling as the reduction in g_m and increase in g_d directly impact both f_T and f_{max}, as indicated in the equations above.

These effects are mainly caused by the reduction of the potential barrier formed beneath the gate during the off-state due to an applied V_{DS}. In HEMTs with long channels, the reduction in energy barrier height on the source side of the gate usually has minor consequences, leading to a small drain-source leakage current. However, with a sufficiently short gate length, the voltage applied at the drain contact can influence the barrier height on the source side of the gate. Consequently, thermal excitations enable electrons to surpass the energy barrier, causing an increase in the drain-source leakage current. This phenomenon is termed Drain-Induced Barrier Lowering (DIBL), resulting

in a negative shift of V_{th} in the device's transfer characteristics. Due to Short Channel Effects, the gate's capacity to modulate the electron concentration in the channel is compromised, leading to a reduction in g_m. Furthermore, as the dependence of V_{th} on V_{DS} strengthens, R_{DS} decreases, leading to a reduction in f_{max}.. In GaN-based HEMTs, DIBL can also be triggered by a high leakage current through the buffer beneath the depleted gate region (punch-through), rather than at the AlGaN/GaN interface. Thus, increasing resistivity in the buffer layer is essential to confine the electron distribution to the vicinity of the III-nitride interface. Alternate approaches involve enhancing electron confinement in the quantum well by incorporating a back-barrier with a larger bandgap, such as AlGaN. This improved confinement allows for better gate control, thus mitigating DIBL. Implementing a lattice-matched InAlN can further enhance gate modulation by reducing the barrier thickness while maintaining a high sheet carrier concentration. This permits additional L_G reduction in GaN HEMTs.

These techniques allows to reconfigurate the HEMT structure in the so named Nitrogen-polar epitaxial structures, where the GaN channel resides on top and the AlGaN layer beneath inherently serves as a back barrier. This configuration enables the achievement of low ohmic contact resistance on GaN and significantly enhances scalability. As a result, Nitrogen-polar HEMTs have achieved remarkable benchmarks in power density and power added efficiency (PAE)[29].

Chapter 4: Laboratory activity

This chapter describes the experimental activity carried out in the laboratories of the department of information engineering (DEI) of the University of Padua, with the supervision of the members of the ACME group (Advanced Characterization and Modeling of Electronics devices). More in detail, the structure of the devices under examination will be analysed, as well as the experimental set-ups adopted to carry out the characterization activity. The set-ups were developed internally by the members of the group and have allowed the investigation of the deep levels present in the devices helping the comprehension of the origin of the stability issue.

4.1 Device Under test: QORVO

Through partnerships with academia, industry and government, Office of Naval Research (ONR) coordinates and sponsors scientific research and technology development for the U.S. Navy and Marine Corps. Thanks to this project, the University of Padua has started a collaboration with the U.S. company QORVO, multinational colossus specialized in products for wireless, wired and power markets. For my thesis project, the company has provided us with a variety of state-of-the-art GaN HEMT devices (for a total amount of 40 devices) intended for RF applications. Thanks to this experimental study, a stability analysis was conducted to investigate the issues affecting the analysed technology and contributing in this way to its development through a better knowledge of the sources of the stability issue.

Initially, the components that were entrusted to us came as single transistors from the lot with identifier 2125360. Since the devices would have been difficult to handle due to the small dimensions, they were preliminarily deposited on top of an aluminum sheets and subsequently welded on thanks to a two-component paste. This paste consists of a silver-filled epoxy system[30] which, when heated to high temperatures, solidifies and blocks the device in position. The resin therefore acts as a conductive glue, thus allowing easier handling during the device analysis. In the Figure 4.1 is reported a picture taken

with a Dino-lite microscope where we can see the final result of the deposition of 5 transistors (belonging to the same wafer) on a single aluminum plate.

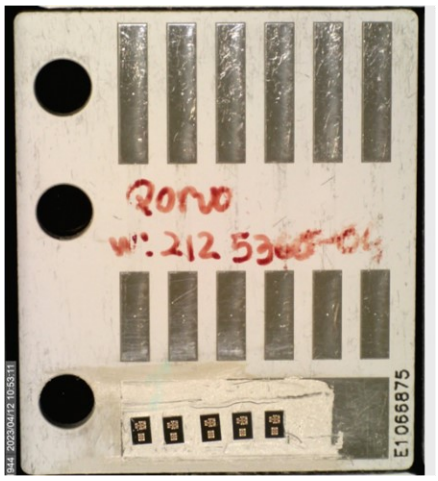


Figure 2.1 Example of a chip under test with 5 GaN HEMT transistor from QORVO on it. The picture has been taken with Dino lite microscope camera.

Ultimately, the 40 single transistors that have been assigned to us, belonged to 8 wafers from which have been cut 5 transistors each. The eight wafers differ for the epitaxial stack; More in detail, they differentiate for (i) the presence of a back-barrier (ii) the concentration of aluminium in the back-barrier, and (iii) the substrate producer. The detailed info are reported in Table 4.1 where are reported the information provided by the producer about the 8 wafers from which the transistor came:

Product	Lot	Wafer	Material	Epi-Vendor	Substrate
EG3745	2125360	1	Control	IQE	II-VI
EG3745	2125360	2	1.5%BB	IQE	CREE
EG3745	2125360	3	0.5%BB	IQE	CREE
EG3745	2125360	4	1%BB	IQE	CREE
EG3745	2125360	5	Control	IQE	II-VI
EG3745	2125360	6	1.5%BB	IQE	II-VI
EG3745	2125360	7	0.5%BB	IQE	II-VI
EG3745	2125360	8	1%BB	IQE	II-VI

Table 4.1 Information provided by the customer

In order to distinguish the device and easily identify them, the wafers were numbered from 1 to 8, while the single transistor were named Ax, where x is a number is between 1 and 5. In this way for example, if we are referring to the third device of the fifth chip of wafer (abbreviated from now on as chip) we can name it chip5_A03. The epitaxial vendor is common to every wafer and is IQE, a British semiconductor company which manufacture advanced epitaxial wafers, while the substrate is done by two different companies that are CREE (also named Wolfspeed) and II-VI. As previously mentioned the first difference between the devices consists in the presence or not of a back-barrier (i): chip 1 and 5 are the wafers defined as CONTROL and they are the only wafers that have not a back-barrier in their structure. These devices were considered as the reference devices for the analysis, and they are both grown on top of a substrate developed by II-VI.

The second difference (ii) consist in the different concentration of Al in the back-barrier Chip 2 and 6 have a concentration of Al in the back-barrier equal to 1.5 % Chip 3 and 7 have a concentration of Al in the back-barrier equal to 0.5% In the end, Chip 4 and 8 have a concentration of Al in the back-barrier equal to 1 %

The third and latter difference consist in the substrate which were producted by two different companies (iii). Chips 2, 3, and 4 are grown on top of a substrate developed by CREE (wolfspeed), while all the other chip are grown on top of a substrate made by II-VI.

The reason why there are two CONTROL devices from the same substrate is that the CONTROL is a released technology. Though on the control, there is no difference in performance between CREE and II-VI, there is a small difference in yield (Wolfspeeds 150mm substrates edges has more uncracks than II-VI) but this is a yield issue not a performance difference.

About the geometry these devices come from the GaN45 3rd generation technology on which QORVO is working, and they present a gate length of 0.45 µm, a gate width of 0.4 µm, consisting of four fingers of 0.1 µm each with standard gate and gate-source

field plates. In the following Table 4.2 a summary is done and in Figure 4.2 a picture with dino-lite microscope of the single device is reported:

QORVO GaN45 3rd generation technology	dimension
Gate length L_G	0.45 µm
Gate width W_G	4 x 0.1 µm

Table 4.2 Summary of devices dimension for QORVO GaN45 3rd generation technology

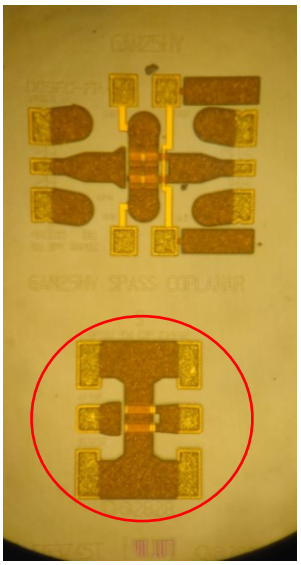


Figure 4.2 Of the two devices in the picture, the one that has been analysed is the lower ones. It presents a typical RF structure. The up and down contacts are the Source contacts while the two central ones are the gate (on the left) and) the drain (on the right).

Ultimately the epitaxial structure of the devices is analysed. The architecture from bottom to top comprises:

1. Silicon Carbide (SiC) substrate
2. Nucleation layer
3. Carbon (C) and Iron (Fe) doped GaN buffer
4. AlGaN back-barrier with different alluminum concentration:0 %, 0.5 %, 1 %, 1.5 %
5. GaN (unintentional impurity doping uid)
6. AlGaN barrier layer
7. Passivation layer

8. Ohmic contacts
9. Gate and Gate-Source field plates

These devices are therefore grown on a Silicon Carbide substrate, one of the top-quality types of substrate that allows for a great heat dissipation and isolation. In addiction this material respect to Silicon allows for a better match in lattice constant with the following layers, reducing in this way the defect density [31]. Thus, a nucleation layer is present in order to mitigate the difference with other layers structure and make more accompanied the change in the crystal structure. Moreover, there are two layers with the same purpose, of improving the carrier confinement (for further detail see chapter 3…): the GaN buffer with Carbon and Iron intentionally introduced, and the AlGaN barrier layer functioning as a back-barrier. The adoption of both aims to enhance the charge confinement in the 2DEG. In fact, since percolative and parasitic paths of carriers are almost always present in the standard AlGaN/GaN architecture, iron and carbon doping in a lower layer allows to generate trap defects through impurity doping that can capture the carriers outside the channel that would result into leakage current [32][33]. At the same time, the introduction of an AlGaN layer immediately above the GaN channel, act as a back-barrier in a sense that there is an increase in the electron's confinement in the channel thanks to the enhanced bending in the band diagram on the substrate side which reduce the leakage current toward the buffer. Then there is the core of the polar architecture, the layer of undoped GaN and the AlGaN barrier layer that thanks to the polarization effects enable the formation of a channel of electron with an elevated density of carriers (2-DEG) (see chapter 2 for further information about the 2-DEG formation and the properties of HEMTs) . The passivation layer is present to reduce the impact of surface defects, as mentioned in the previous chapter. In the end are present ohmic contacts that allows injection of carriers at the drain and source of the devices and field plates, that thanks to their presence can improve the uniformity of the electric field on top of the structure, reducing the stability issues and enhancing the performances of the device.

4.2 Characterization of the devices

In the period of the research training, several characterizations were performed on the devices provided by QORVO. The aim was to analyze the stability issues associated with trapping. The standard approach of the group to the characterization of HEMT devices starts with a complete static DC characterization. The main curves of the transistor were derived: $I_{DS} - V_{DS}$ (output characteristic), $I_{GS} - V_{GS}$ (input characteristic), $I_{DS} - V_{GS}$ (transfer characteristic), $g_m - V_{GS}$ (transconductance characteristic), $g_d - V_{DS}$ (conductance characteristic). The importance of these curves Is related to the possibility of extracting the main DC parameter that in a first analysis can give an indication of the performance of the device. Moreover, it is possible to study the distribution of those indicator in order to have a comparison between different devices [34]. A subset of the typical DC parameters extracted from the DC curves are: the threshold voltage (V_{th}) that can be calculated from the $I_{DS} - V_{GS}$ graph, by fixing a value of current close to zero to avoid the presence of the ON-resistance and then extrapolating the corresponding voltage (usually a value of current of $I_{DS} = 0.005\ \frac{A}{mm}$ is used), the peak of transconductance ($g_{m,peak}$) which is derived as the maximum of the $g_m - V_{GS}$ curve, the ON-resistance (R_{ON}) of the device which is the inverse of the slope of the linear region of the characteristic $I_{DS} - V_{DS}$. After the DC measurement was completed, double-pulse (or pulsed I-V) measurements were performed. They consist in measuring $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ characteristics, obtained pulsing the drain and the gate voltage during the measurements. These types of curves are derived by giving fixed pulses in order to measure the device and between those, a specific bias is given to the transistor in order to stress it. This is done in order to estimate the functioning of the trapping mechanisms inside of the devices, especially if there is or not presence of memory effect, if the major trap's contribute is due to traps located under the gate stack or on the drain side. Note that this characterization is only quantitative and gives a response only to the presence or not of the traps but doesn't communicate anything on the trap's nature and origins. In fact, what is possible to observe from these curves is the variation of some parameters as the stress performed is increased: generally, the rule is that if the $I_{DS} - V_{GS}$ characteristic are rigidly shifted to the right or left a threshold voltage variation is happening which in turn says that the traps are mainly located under the gate stack. On the contrary, if the slope of the $I_{DS} - V_{DS}$ curves is changing, we are registering a variation in the ON-resistance of

the devices, which in turn says that the traps are mainly located between the gate and the drain regions.

The parameters aimed to prove these observations are the following:

- Current collapse (CC): it represents the variation of the saturation current after stress. It is calculated as:

$$CC = 1 - \frac{I_{DS}\left[V_{GS,stress} \neq 0\ V, V_{DS,stress} \neq 0\ V\right]}{I_{DS}\left[V_{GS,stress} = 0\ V, V_{DS,stress} = 0\ V\right]} \qquad (4.1)$$

- Threshold voltage shift (ΔV_{th}): it is the variation of the threshold voltage after stress. It can be calculated as [36]:

$$\Delta V_{th} = V_{th,stress} - V_{th,no-stress} \qquad (4.2)$$

- The variation of ON-resistance as previously mentioned.
- The variation of the transconductance which can be expressed as a rigid shift of the characteristic or as a variation in its peak

After the pulsed I-V characterization, a second DC analysis has been carried out, this time aimed to confirm the behaviour observed during the pulsed stress, This was done performing DC measurements, and extracting the $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ in going and back conditions. This means that V_{GS} (in the case of $I_{DS} - V_{GS}$) and V_{DS} (in the case of $I_{DS} - V_{DS}$) are varied from a value A to a value B (with B>A) during the go measurement and viceversa, from B to A, during the back measurement. This technique allow to understand if the device can trap or detrap during the measurement and if this happen how the DC characteristics are changed, in order to understand better trap's behaviour.

In the end a qualitative analysis of the traps has been performed: this was achieved by performing Vth-transient measurement. The impact of the traps has been analysed with stressing the devices at different bias condition, and at different temperatures. Thanks to these plots it is possible to monitor the evolution of the drain current during the stress and recovery phase. The transients so obtained are then fitted with stretched exponential functions in order to extract the corresponding time constant at various temperatures. In

the end from these time-constants it is possible to build the Arrhenius plot, from which it is possible to obtain the trap capture cross-section and the activation energy. [37]. Then the Arrhenius plot of the trap present in the devices, were compared with the Arrhenius plot of other traps known in the literature. In such a way, it becomes possible to estimate the nature of the traps, for example iron related traps or carbon related traps, and subsequently, estimate the position and the physical origin of the trap: for example, traps associated with the doping of the device, dislocations, surface state and more. The majority of the Vth-transient analysis has been conducted stressing the device in OFF-state; Nevertheless, measurements, stressing the device in SEMI-ON were performed, this stress condition differentiate from the off state since the device is in saturation and there is a current flowing during the stress. The adoption of different type of stress has allowed a better comprehension of the trapping mechanisms

4.3 Laboratory instruments

The laboratory activity has been carried out in the laboratory of the University of Padua, where custom set-up has been built in order to characterize the devices. IN this paragraph the instrumentation adopted and the experimental setups are going to be explained.

Probe stations and general equipment

The probe station appears as a cubic metal box where in the inside we can found several tools needed for every kind of measurements. First of all, the probe station acts as a Faraday cage, that allows to reduce the influence of the outside interference on the measurements. Moreover, it is equipped with pneumatic suspension lo lower the vibrations that can obstacle the goodness of the contact between the tips and the device under test. Inside of a probe station we can find a metal chuck, movable in the planar cartesian directions (x,y) thanks to dedicated handles typically placed below it. The metal chuck is a metal plate where the devices are places in order to be analysed. The chuck can be either simple or thermal, in the last case meaning that thanks to a specific controller it can be raised up in temperature for specific tests. In addiction it is generally provided

with a series of holes on the surface connected to a vacuum pump in order to maintain the device under test attached to the plate. Above the chuck there is a microscope. This tool is essential because the devices, as well as the tips to contact them, are too small to be clearly visible to human eyes. In the following Figure 4.3 a picture has been taken of one of the probe stations used during the laboratory activity:

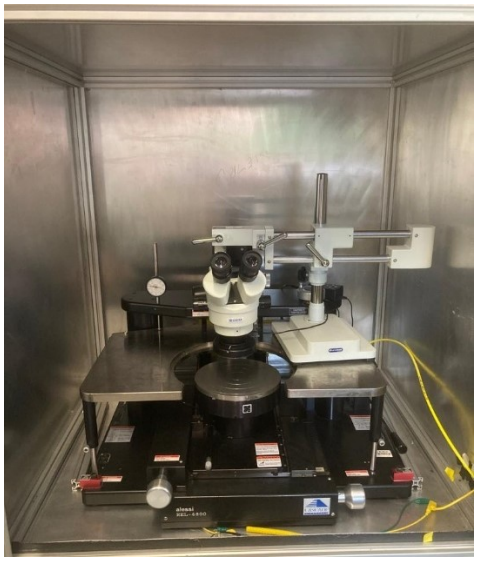


Figure 4.3 Probe station, without tips and manipulators. It is possible to observe the metal chuck under the microscope.

For what concern the tips, they are metallic tools used to contact the terminals of the device under test, that are Source, Drain and Gate. There are two main types of tips: the DC and RF ones. The DC tips are usually single needle, mostly used to contact power devices. The major drawback of this tips is that are not suitable to contact scaled devices such as the RF ones since they introduce not negligible parasitic element (capacitor and inductances) that may result in remarkable oscillation of the electrical parameters during the measurements. The RF tips are the ones used during the characterization activity. They have a shape which resemble the one of a tridents. The external fingers are connected to ground and are used to contact the Source. The central one carries the electrical signal that are applied to the gate and the drain terminals. The design allows to minimize the parasitic elements such capacitances and inductances of the tips themselves. Since these tips are used for high-frequency test signals, the design allows to minimize the parasitic elements such capacitances and inductances of the tips. In this way the impact of the tips

on the device operation is lowered, optimizing the quality of the measurement. The tips used with the set of devices to test are present in Figure 4.4:

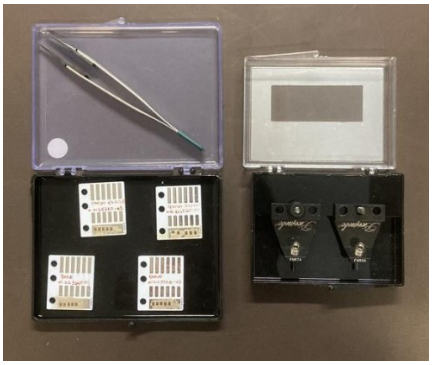


Figure 4.4 on the left: a set of 4 chip (with 5 transistors on each). At the right: the two RF-tips used to analyse the transistors

Finally the tips are mounted on manipulators which act as a solid support, able to make the tips move, with precision, and be adjusted in all cartesian directions (x,y,z). The manipulators are usually kept on two magnetic metal planes on the sides of the metal chuck in order to maintain them fixed.

Parameter analyzers

The parameter analyzer is essential to do the DC characterization. There is a great variety of parameters, which differentiate for the number of Source Monitor Unit (SMU) and their characteristics. The model used is the Keysight E5263A reported in the following Figure 4.5:

Figure 4.5 Parameter Analyzer Keysight E5263A

This parameter is provided with two SMUs, one designed as high-speed and medium power and the other high-speed and high-power. In the following table it is reported the main differences between the two:

SMU	Maximum V-I ratings	Minimum V-I resolution
High-speed/medium-power	-100 ÷ 100 V ; -200 ÷ 200 mA	100 µV ; 5 pA
High-speed/high-power	-200 ÷ 200 V ; -1 ÷ 1 A	100 µV ; 5 pA

Table 4.3 SMUs maximum ratings and minimum resolution for the Keysight E5263A parameter analyzer

At the end of the SMUs there are two output connectors, one dedicated only to measurement (measure connector) and another able to impose an output voltage and register the output current (force connector). For our activity, this instrument was used to perform the DC measurements. In order to carry on the measurements two triaxial to coaxial connector were linked to the force terminals of the two smu. Then with two wire were used to connect the terminal to the tips connected at the drain and gate terminal of the device. Lastly, the parameter can be directly linked to an external computer thanks to a General-Purpose Input Unit (GPIB) which open the communication between the two tools. By doing this, it is possible to control remotely the parameter through the external computer by mean of a Labview software.

Current Probes

Current probes are essential in order to measure the current flowing in the devices without altering the measurement. The probe used during the laboratory activity was a Hioki probe which is a type of Hall Effect Current probe. In the following Figure 4.6 the current probe used is reported.

Figure 4.6 Hioki Current Probe based on Hall-effect

This instrument is able to measure the current thanks to the presence of a magnetic field. When charges flow inside a conductor, if a magnetic field is present, Lorentz's Force act on the charges that are flowing in the semiconductor, making them deviating their trajectory towards one of the two extremities of the conductor. The Lorentz's Force is given by the expression reported in the Equation 4.3:

$$\vec{F} = q\vec{v}\, x\, \vec{B} \qquad (4.3)$$

In this way, after the charges has been deflected, there is an accumulation of positive and negative charge on the opposite sides of the semiconductor that in turn produce a voltage drop. Measuring the induced voltage drop it is possible to determine the current flowing in the device.

Arbitrary Waveform Generator

The Arbitrary Waveform Generator (AWG) is the instrument able to produce the electrical signal needed during the measurement. Despite the different types of AWG, the most common employed are the digitalized one. In a digital AWG, the internal memory is capable to store different signals shapes. Since they are programmable, each custom waveform can be generated for each specific measurements. In the following Figure 4.7 the AWG used during the characterization is reported:

Figure 4.7 AWG Keysight 33600 A

The model Keysight 33600 A is a dual channel AWG with three output connectors: the yellow one is named channel 1 and it is usually connected to the gate of the device under test. The green one is called channel 2 and it is usually connected to the drain. In the end the third connector is a trigger port. The trigger port is used to generate a triggered signal which align AWG operations with the ones of other instruments. The AWG is finally connected via USB to the external computer.

Power Amplifiers

Power amplifiers (PA) are a common instrument used in the laboratory. Their principal objective is to enhance the amplitude of the input signal while maintaining all other characteristics unaltered. This tool is generally placed between an AWG and the DUT (device under test), in order to overcome the intrinsic limitations in term of maximum voltage and current of the AWG (V_{max} = 10 V; I_{max} = 1 mA). Even if they are essential in order to correctly measure the principal characteristic of the devices, often they can also introduce noise, amplifying the input noise at low frequencies. For this and other reasons, several adjustments need to be considered during the measure. In the following Figure 4.8 a standard 10 x Power Amplifier is illustrated:

Figure 4.8 10 x Power Amplifier

As the depicted figure reports, at the left we have the input connector and at the right the output connector. In the middle there is a knob able to change the gain of the amplifier, in this case the maximum reachable is an amplification of 10 times. The input impedance is 500 Ω.

Oscilloscopes

Oscilloscopes are essential tools in laboratory activity, whose principal objective is to measure the electrical signals of the device under test. The oscilloscope that has been used during the experiments is the Tektronix MS044, reported in the Figure 4.9.

Figure 4.9 Oscilloscope Tektronix MS044

This instrument presents four input channels which are used during the measurement to read the voltages at the terminal of the tested device. Usually, two terminals are employed to read the voltages at drain and gate, one of them is connected to a current probe to sense the current and the last channel is the trigger port, that can be connected to the one of AWG, for example, to allow the synchronism between the two instruments. Another port is present on the side of the oscilloscope to connect the internal mass of the instrument with a banana cable. This allows to connect the mass of different instrument, avoiding errors correlated to different ground reference. In the end, even this model of oscilloscope can be linked to an external computer via USB, allowing the transfer of data acquired during the measurement.

Clamp Circuit

The clamp circuit is a PCB with resistors, capacitors, one Operation Amplifier (Op-Amp), one MOSFET and a set of three Zener Diodes with different blocking voltages. One of the three Zener can be selected, based on the desired blocking voltage. In the following a schematic of the circuit is reported:

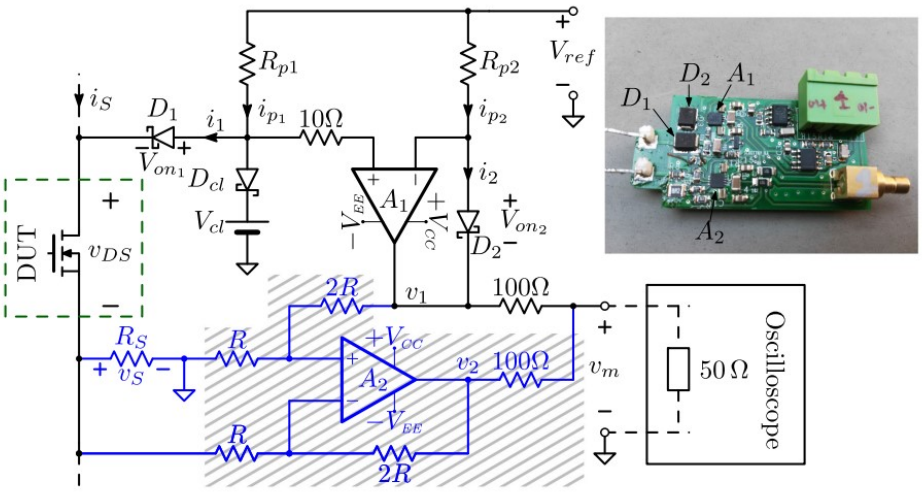


Figure 4.10 Generic schematic of a clamp circuit [38]

The clamp circuit has to be put in a specific position of the set-up, specifically between the output of the power amplifier and the input of the oscilloscope. The working principle of the circuit is the following: when an input as a ramp or step signal arrive, the

circuit starts initially to follow the signal, producing an equal output waveform. Then, the circuit make the voltage saturate to the lowest voltage between the power supply one and the blocking voltage of the selected Zener diode. In this way, even if we are operating at very high voltages, and consequently diminishing oscilloscope resolution (same number of divisions for a greater span of voltage), the clamp circuit allow to saturate the high voltage value to a smaller one dictated by the Zener or the power supply, in this way contributing to enhance the oscilloscope resolution. In the following, a picture of the clamp circuit and of the power supply used during the laboratory activity is reported:

Figure 4.11 at the left: Clamp circuit. At the right: power supply

4.4 Experimental set-up

In the following section, the experimental set-ups used during the laboratory activity are presented in detail in order to explain better how the characterization of the assigned devices was carried out. The set-ups are mainly custom-type set-ups, in the sense that they were developed internally by the members of the ACME group, and are based on the measuring instruments described previously.

4.4.1 DC Analysis

The main goal of the DC or static analysis is to evaluate the performances of the device under test in static conditions, as a starting point. From this characterization, that involves the acquisition of several I-V curves, the most describing parameters of the

transistor were derived, and used to have a comparison in the population of the devices that have to be analysed.

The tools required in order to carry out the DC analysis are:

- Probe station
- Manipulators and RF tips
- Parameter Analyzer
- DC Labview Program

The parameter analyzer was taken and placed near the probe station. As previously described, the parameter, has two SMUs, a high-power and medium-speed and a high-power and high-speed one. These pieces of equipment allow to impose a voltage at the terminals of the DUT and to measure the current flowing in the terminals of the devices for this activity, the force connector was chosen from the ones present on the SMUs, since it allows only to measure the current or voltage (amplitude and sign), but also to impose, respectively, a voltage or a current.

To realize the connections between the parameter analyzer and the device under test, a triaxial to coaxial adapter is placed on the two force connectors. Then, two coaxial cables are attached from the measuring instruments to the measuring RF tips and finally placed in contact with the terminals of the device under test. The high- speed and medium-power force connector is linked to the gate of the device, since neither high voltage nor high current are expected at this terminal. Instead, at the drain of the device is contacted with the high-speed and high-power connector of the SMU, since at this terminal higher currents and voltages, with respect to the gate, are expected. In the end, thanks to a GPIB interconnection, the parameter analyzer is directly interfaced with the DC Labview program form the external computer, that coordinate the characterization and allows to extrapolate the data during the measurement. In the following Figure 4.11, a schematic of the set-up is reported:

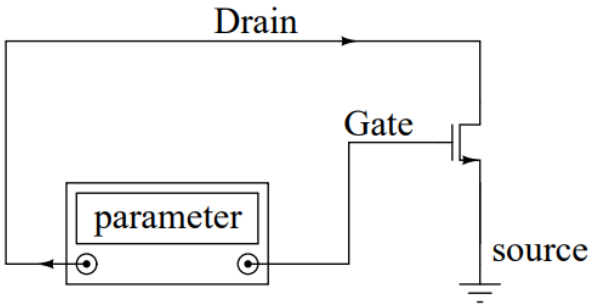


Figure 4.12 DC measurement experimental set-up

Thanks to this set-up it was possible to extract the data to realize several I-V curves, by appropriately choosing the measurement conditions from the DC-Labview program, as reported in the following Figure 4.12:

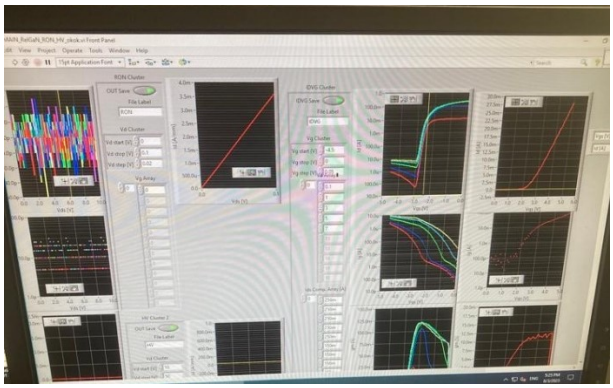


Figure 4.13 Frames of the DC-Labview program

The curves extracted are:

- The input characteristic or gate-to-drain diode characteristic $I_{GS} - V_{GS}$
- The input characteristic or gate-to-source diode characteristic $I_{GD} - V_{GS}$
- The transfer characteristic $I_{DS} - V_{GS}$
- The output characteristic $I_{DS} - V_{DS}$

From these curves, realized starting from empirical I-V data, several parameters of interest can be derived, as follows:

- Gate-leakage current and Drain-leakage current ($I_{GS,leak}\ and\ I_{D,leak}$): the first leakage contribute is extracted considering the $I_{GS} - V_{GS}$ characteristic, when the transistor is in the OFF-state. To extrapolate it, a fixed value of gate voltage is considered, and then the corresponding value of current is extrapolated. In a similar way, from the $I_{DS} - V_{GS}$ curve, a value of voltage, when the device is in the OFF-state, is chosen as a reference, and then it is possible to extract the value of current at that voltage level.
- Threshold Voltage (V_{th}): the threshold voltage of the device is the minimum voltage at which the device is considered able to conduct a current. This parameter is extracted from the transfer characteristic $I_{DS} - V_{GS}$, choosing a fixed value of current, and extrapolating the voltage that corresponds at that current level.- In order to provide a better comparison between devices with different gate width, the measured current is usually normalized with respect to the gate width in order to eliminate its influence., The current value at which the threshold voltage was evaluated was $I_D = 0.005\ \frac{A}{mm}$,
- Drain Induced Barrier Lowering (DIBL): it is one of the manifestations of short-channel effects. Because of the reduced gate length and the increased lateral field, drain contact can influence the barrier height on the source side of the gate. Consequently, thermal excitations enable electrons to surpass the energy barrier, causing an increase in the drain-source leakage current. To quantify the dependence of the threshold voltage on the drain current the DIBL can be calculated as:

$$DIBL = \frac{V_{th}\left(V_{DS.high}\right) - V_{th}\left(V_{DS.low}\right)}{V_{DS.high} - V_{DS.low}} \qquad (4.4)$$

- Transconductance peak ($g_{m,peak}$): The transconductance is the derivative with respect to V_{GS} of the drain-source current, that is the derivative of the transfer-characteristic as reported by the following equation:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \qquad (4.5)$$

The peak of the transconductance is linked with the threshold voltage, and it can be useful to track its variation. For this reason, once the g_m curve has been extracted from the transfer characteristic, the peak is found by searching the

maximum in the corresponding array of data, and th voltage at which the gm peak is found is tracked.

- Subthreshold slope (SS): when the transfer characteristic is plotted in logarithmic scale, it is easier to study the subthreshold behaviour: typically this behaviour is governed by an exponential and express how fast the device is able to switch from an On to an OFF condition. The S.S. is evaluated considering the magnitude of the slope of the I_D current from the I_DV_G characteristic in the subthreshold region. If the slope is high, the device is able to switch is status faster, enabling high frequency operations; on the contrary, if the slope is small the device is slow and starts to conduct after more time (it requires more time to switch from ON to OFF state). The SS is usually extracted fitting the I_DV_G curves in logarithmic scale with a linear exponential and it is given by the expression reported below:
- ON-resistance (R_{ON}): from the output characteristic it is possible to extract the ON-resistance as the inverse of the slope evaluated in the linear region of the characteristic. This is achievable thanks to a linear fit and then through the following equation:

$$R_{ON} = \frac{1}{\frac{\delta IDS}{\Delta VDS}} \qquad (4.6)$$

- Saturation current (I_{DSS}): the saturation current is the value of the drain current when the device operates in saturation region. This parameter is extracted from the I_DV_D characteristics of the device, in a similar way to threshold voltage derivation: in this case, a fixed value of drain voltage is chosen, like V_{DS} = 7 V, where it is sure that the device is in saturation. At this point the corresponding current is derived through an extrapolation operation.
-

4.4.2 Double-Pulse Analysis

The objective of the double pulse or pulsed IV analysis measurements is to perform a measure of the current of the device avoiding any contribution due to the self-heating. In order to do so the voltages at the gate and the drain terminal are imposed for a short time. As a consequence, the current results pulsed too. The pulse duration is usually

shorter than the average life time of the hypothetical traps present in the structure, in order to avoid any influence of the traps during the measuring pulses. This measurement is performed by imposing a bias condition on the gate and drain terminal of the device under test and subsequently, two pulses are simultaneously applied in order to build the I-V curve. In this way, by changing the amplitude of the pulses that are sent to the drain and gate of the device, the $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ curves can be constructed. The first is derived by keeping the amplitude of the drain pulse constant and by varying that of the gate pulse. On contrary, the second one, is obtained by changing the drain pulse while the gate pulse is kept constant. In the Figure 4.13 and 4.14, the typical measurement waveform applied at the drain and gate terminals are reported:

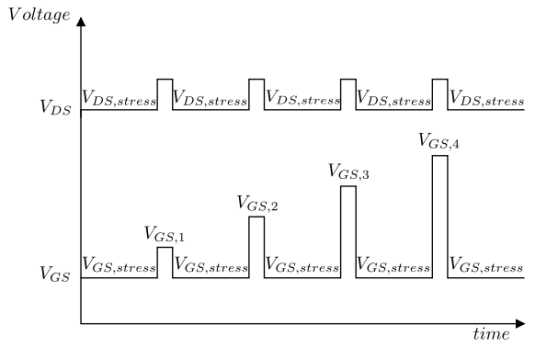


Figure 4.14 Waveforms to be applied at the gate and drain terminal in order to build the $I_{DS} - V_{GS}$

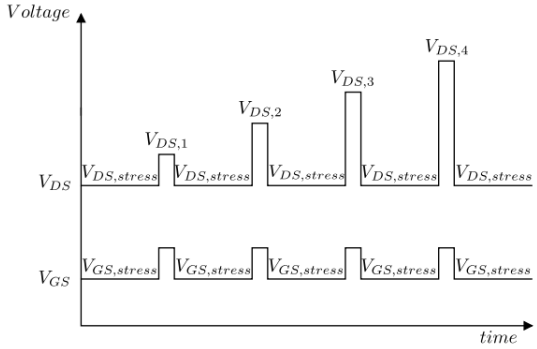


Figure 4.15 Waveforms to be applied at the gate and drain terminal in order to build the $I_{DS} - V_{DS}$

In addition, there are numerous parameters to consider during the measurements, that have to be chosen appropriately before the start of it:

- Duty-cycle: about the duty cycle must be chosen properly since it is the sum of the pulse duration, the number of pulses (if more measuring pulses are done subsequently) and the stress phase. The pulse duration is usually kept as short as possible in order to minimize self-heating effects, and avoiding any trapping during the measure. Usually it is comprised between 1 μs and 10 μs. The custom setup allows to choose between two acquisition mode: sample mode and average mode. In the first case the current is calculated from a single measuring pulse, while in the second mode a train of measuring pulse is generated and then the current is evaluated as the average of current measured during each pulse. In the end the quiescent phase corresponds to the time during which the device is stressed, and it allows to determine the minimum duty-cycle achievable.
- Stress bias condition: Consists in the electrical condition applied to the terminals of the device. Its importance resides in the fact that choosing the appropriate state (OFF, semi-ON and ON) in which the device is stressed, has an impact in the activation of the traps inside of it. Generally, during OFF-state stress, when there are high negative V_{GS} and low positive V_{DS} the expected trapping mechanism is associated to bulk traps under the gate region, while with high negative V_{GS} and high positive V_{DS}, the traps are expected to be located mainly in the gate-to-drain access region. With semi-ON state stress, with increasing V_{DS}, the trapping mechanism associated to the drain access region is enhanced. In the end, during ON-state stress, the effect of hot electrons is enhanced respect to OFF-state stress where the channel hasn't formed yet. The higher are the voltages applied, the more energetic become the electrons in the channel and consequently able to escape the channel or produce other traps by impact ionization.

In the end, the I-V characteristics built starting from the pulsed measurements, are quantitively describing the trapping mechanisms affecting the device. In fact, the influence of traps can be detected, monitoring the rigid shift of threshold voltage, the variation in transconductance peak, the variation in the ON-resistance and the modification of saturation current. Finally, as reported during chapter 3, in the section

related to stability issues and trapping mechanisms, an association with the literature can be done: shifts in the threshold voltage and variation in transconductance peak can be associated respectively to traps mainly under the gate or mainly in the gate-to drain access region. In the same way variation of saturation current and change in the ON-resistance can be reconducted to traps presence respectively in the gate stack or in the access region. In the following Figure 4.15 a frame of the Labview program utilized to make the characterization is reported:

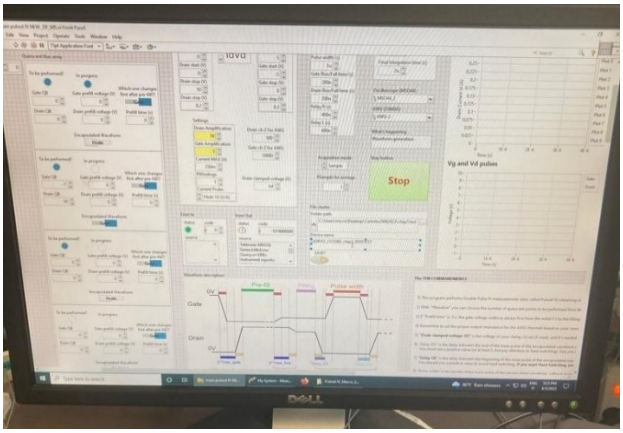


Figure 4.16 Pulsed IV Labview program: at the left the baseline with the bias stress conditions, in the up-central panel the possibility to set the duty-cicle parameters while in the down-center part an example of the pulses at drain and gate. In the end the plots of the transfer and output characteristic are reported at the right

Despite the existence of a dedicated instrument to such analysis, the so-called DIVA (Dynamic I-V Analyzer), in the laboratory, a custom set-up to perform pulsed IV measurement was developed. The instruments employed are reported in the list:

- Probe station, where the device under test were placed
- RF tips and manipulators to properly contact the device
- AWG to generate the pulses and to impose the bias condition during the quiescent phase at both terminals, gate and drain.
- Oscilloscope, that with its four channel it was used to read the waveform generated at the drain and the gate and also to measure the current at the drain thanks to a current probe connected to it
- Current probe, to measure the current at the drain

- Power Amplifier, to amplify the waveform at the drain (10x)

In the Figure 4.16 is reported the schematic of the set-up, highlighting the interconnections between the various instruments. To remotely control the tools, both AWG and oscilloscope were connected via USB to an external computer. From this one, a Labview program dedicated to pulsed IV measurement were used to set the various parameters.

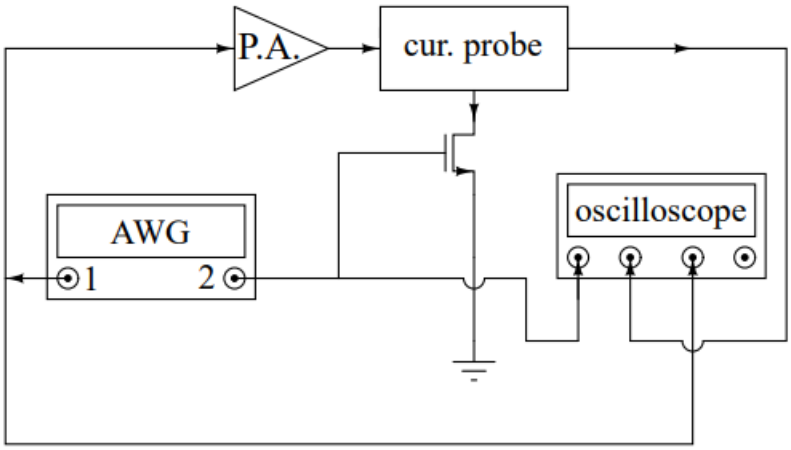


Figure 4.17 Schematic of the Pulsed-IV set up

Finally, in our case, also a clamp circuit was introduced in the set-up, placed between the amplifier output and the drain-connector of the oscilloscope. This was done in order to increase the oscilloscope resolution, since a remarkable level of noise was found during the previous measurements and in this way its impact was limited. In addition, a link between the AWG and the Oscilloscope is done, using the trigger-port in order to synchronize them during the operation.

4.4.3 Vth-transient measurements

The aim of Vth-transient measurements is to evaluate the trapping mechanism affecting the device, in order to collect enough information to understand their origin and root causes. The quantities that are kept under observation are the drain current and the threshold voltage, whose values are periodically collected. The standard procedure

consists of a stress and a recovery phase where appropriate bias conditions are imposed to the device under test. In particular, during the stress phase, a specific bias condition is chosen in order to enhance the trapping mechanism that hypothetically affects the device. The possibility are then OFF-state stress to investigate the presence of traps under gate and in the gate drain access regions, or semi-ON and ON state stress where the role of hot-electrons becomes dominant. In the recovery phase there is usually no imposed bias, in order to avoid to stress the device and measure if the current, previously affected by traps during the stress phase, is able to return to its original value. By the way, even during the recovery phase a bias condition can be imposed in order to observe if the recovery was influenced by the bias, and have a better understanding of the causes generating a specific trapping mechanism. In addition, the time instants in which the data about the current are collected, are logarithmically spaced. This is done because trap levels usually have a behaviour that can be modelled with a stretched exponential function. In this way, the logarithmic scale of the time axis allows in the $I_{DS} - time$ curve a better and faster recognition of the transients due to trapping phenomena. By fitting the transients associated with a specific trap it is possible to derive the time-constant related to the trapping mechanism, and subsequently derive the activation energy of the trap. This is possible by inserting the time constant in the Arrhenius plot and performing a linear fit. The general function describing the behaviour of the current through time is the following:

$$I_{DS}(t) = I_{DS,final} - \sum_{i=1}^{N} A_i \exp\left(-\frac{t}{\tau_i}\right)^{\beta_i} \qquad (4.7)$$

Here, $I_{DS,final}$ is the final value of the current after the recovery phase, N is the number of different stretched exponential transients, the coefficients A_i represents the amplitude of each transients, and it corresponds to the current collapse induced by that trap as well as the type of charge emitted ($A_i > 0\ for\ holes,\ A_i < 0\ for\ electrons$). τ_i are the time-constants associated to each transient and β_i are the ideality factor, that is a measure of how much the transient show an ideal exponential behaviour ($0 < \beta_i < 1$) [39]. It is interesting to notice that even if the measurement is named Vth-transient, what is monitored through time is the behaviour of the current. The reason is the following: a

value of V_{GS} is preliminary fixed and take the name of interpolating voltage. In fact, by interpolating it at each measuring time, the corresponding current is derived. In this way it is possible to monitor the evolution of current through time.

The measurement can be performed at fixed temperature with different stress bias condition, in order to investigate in which, state the trapping phenomena are accentuated, or even with variable temperature, to see if the trapping or detrapping mechanism are thermally activated, (accelerated). In the end, once the time constants are known by fitting the transients, the Arrhenius plot can be built, and the activation energy of the traps can be extracted. The vertical axis of it is represented by $\ln(\tau_i T^2)$ where T is the temperature in kelvin, while the horizontal axis is q/kT. In the case that the trapping process is thermally activated the following relation is valid:

$$\ln(\tau_i T^2) = \frac{E_a}{kT} + \ln\left(\frac{h^3}{2\sqrt{3}(2\pi)^{\frac{3}{2}} m_r m_o k^2 g \sigma_c}\right) \qquad (4.8)$$

Where: E_a is the activation energy of the trap, k and h are the Boltzmann and Planck constant respectively, $m_r m_o$ is the effective mass of electrons, g is the degeneracy factor (usually equals to 1) and in the end σ_c is the capture cross section related to the considered trap. From the equation is clear to see that after the Arrhenius plot have been plotted, a linear fit can easily extract the activation energy (eV) of the trap [40].

In the end the experimental set-up used to perform Vth-transient analysis involves the use of:

- Probe station, where the device under test were placed
- RF tips and manipulators to properly contact the device
- AWG to generate the pulses and to impose the bias condition during the quiescent phase at both terminals, gate and drain.
- Oscilloscope, that with its four channel it was used to read the waveform generated at the drain and the gate and also to measure the current at the drain thanks to a current probe connected to it

- Current probe, to measure the current at the drain
- Power Amplifier (10x), to amplify the waveform at the drain side
- Thermal chuck, to modify the temperature

The schematic is the same of Figure 4.16. The AWG, and the oscilloscope are linked together thanks to the trigger port to synchronize their operation. They are also both connected to an external computer via USB. Thanks to a dedicated Labview Program, Vth transient measurements are performed remotely. In the following figures a picture of the Labview program used is reported.

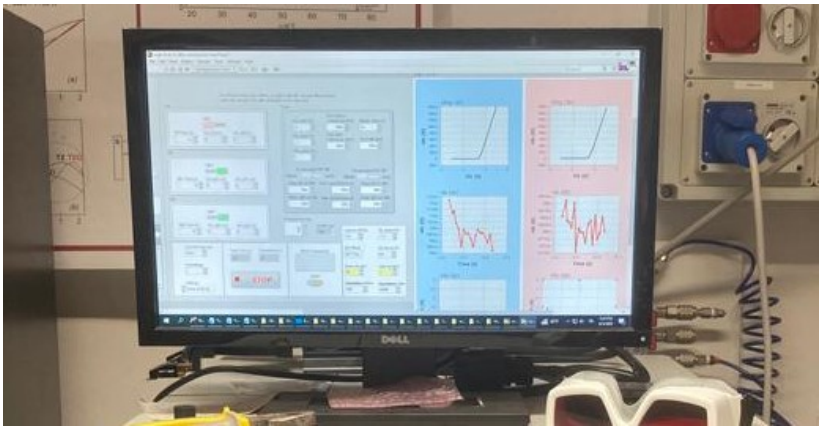


Figure 4.18 frame of the Vth-transient Labview program. In the left panel the stress and recovery bias condition can be settled. In the central panel, the waveform settings are present. In the right panel the data are directly plotted after the measurement.

Chapter 5: QORVO devices

In this chapter, the main results obtained during the laboratory activity conducted on QORVO devices, are reported. The research activity had as focus the comprehension of the stability issues affecting the devices. For that reason, after a preliminary DC characterization, the following measurements were performed to investigate the deep levels in the device: double pulse measurements, DC go and back measurement, and Vth-transient, performed at different temperature and stress conditions. The analysis is aimed to investigate the stability performance focusing on: (i) the influence of the presence, or absence, of the back-barrier in the devices, (ii) the influence of the percentage of Al in the back-barrier, and (iii) the influence of the substrate.

5.1 DC analysis

The DC characterization was done in order to extract the main parameters of the devices. Then, the parameter collected were compared, to identify the differences, if presents, among the devices. In this characterization the most significative curves have been derived from the experimental data collected through the measurement. More in detail, the curves considered are reported in the list:

- $I_{GS} - V_{GS}$
- $g_m - V_{GS}$
- $I_{DS} - V_{GS}$
- $I_{DS} - V_{DS}$
- $g_d - V_{DS}$

All the devices present in the population were tested, and among the 40 devices tested the most representative transistors were chosen for each wafer. This mean that the devices with the parameters more similar to the average parameters were chosen as reference. This was done in order to avoid errors during the characterization caused by an

erroneous choice of the device to compare. In the following table, a recap of the devices chosen and their wafer provenience is reported:

chip	Control	0.5%	1%	1.5%	Control	0.5%	1%	1.5%
Substrate	II-VI	CREE	CREE	CREE	II-VI	II-VI	II-VI	II-VI
Device chosen	A03	A04	A05	A02	A03	A03	A02	A05

Table 5.1 Recap of the most representative device for all the stability analysis: the first raw describe the wafer composition where CONTROL means absence of aluminum back-barrier, while the percentages 0.5%,1% and 1.5% are the concentration of aluminum in the back-barrier layer. In the second raw the Substrate vendor is reported: we have two CONTROL from II-VI, three wafers from CREE with increasing percentage of Al in the back-barrier and three wafers from II-VI, always with increasing Al in the back-barrier. In the end, in the third raw the nominative of the device chosen is reported, with prefix A0. This mean that from the 5 devices available for every wafer, just the most representative has been chosen for the analysis.

These representative devices were chosen after all other were tested, and a statistic has been made: in this way the present trend could be investigated and the devices with average characteristic could have been selected.

5.1.1 DC statistics

In the following section, the statistical analysis of all the parameters obtained from the DC characterization has been reported. In order to extract the parameters, the procedure explained in the chapter 4 was followed. The parameters considered are the ones reported in the list:

- gate and drain leakage current $I_{GS,leak}$ and $I_{D,leak}$
- Peak of transconductance $g_{m,peak}$
- Subthreshold slope SS
- Threshold voltage V_{th}
- Drain Induced Barrier Lowering DIBL
- Saturation current I_{DSS}
- ON-resistance R_{ON}

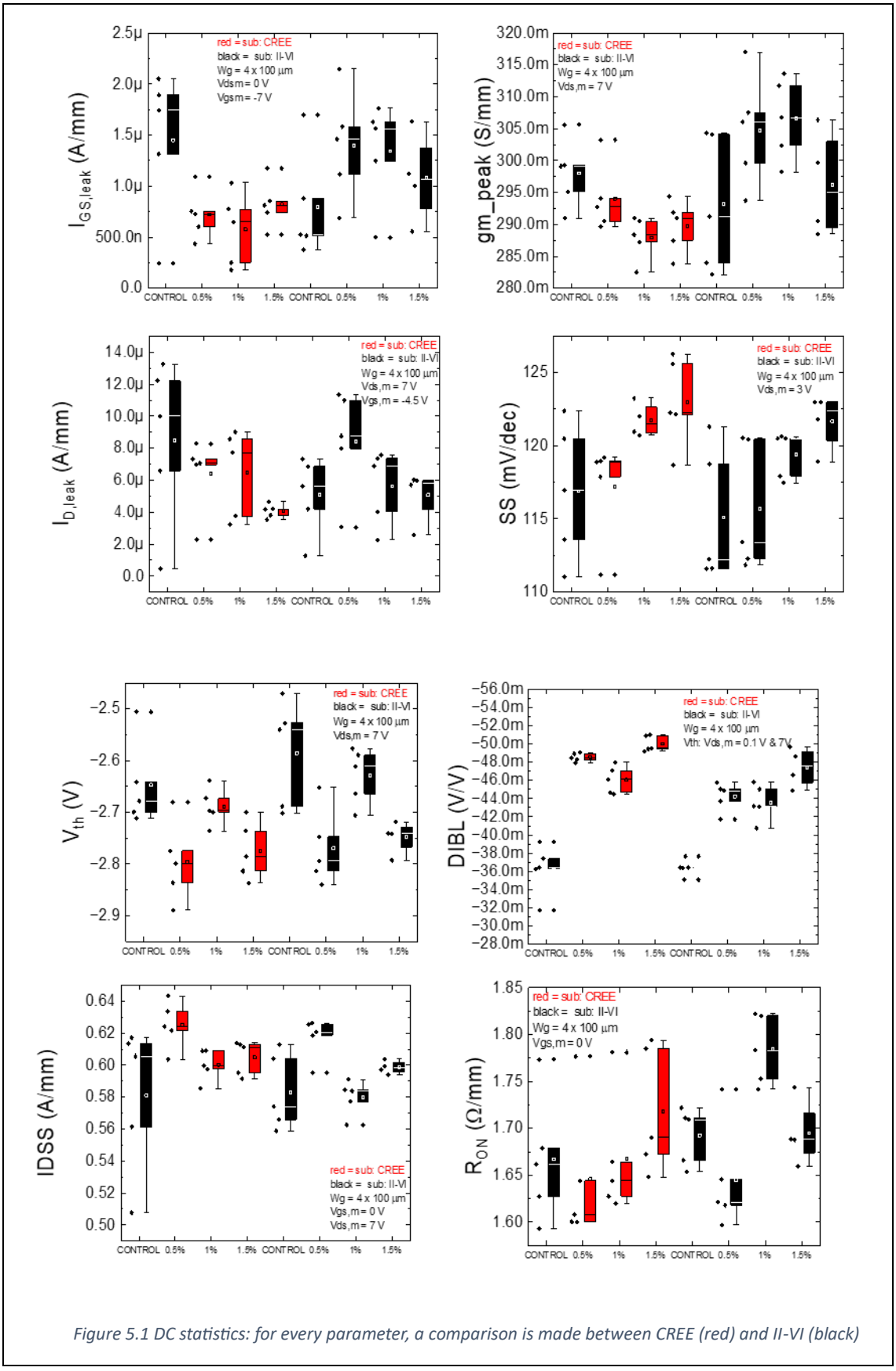


Figure 5.1 DC statistics: for every parameter, a comparison is made between CREE (red) and II-VI (black)

Then, the same parameter, for all the different wafers, were plotted using a box chart plot. This was done, in order to visualize more easily the dependences of the parameters on the different epitaxial structures

In the end, some dependences were found, and are summarized in the list which follows. To better comprehend the dependences of the parameters on the wafers structure, a comparison was done between devices with different substrate, and between devices with different back-barriers (presence of the back-barrier, and Al concentration):

- CREE vs II-VI substrate: With respect to devices grown on II-VI substrates, the others grown on CREE substrate showed a lower two-terminal gate-leakage current ($I_{GS,leak}$), while they shows similar value of drain leakage current ($I_{D,leak}$). For what concerns the $g_{m,peak}$, the V_{th} and the DIBL (in modulus) they were found to be smaller, on average, for CREE devices. As a consequence, the smaller DIBL of devices grown on CREE substrate proved that those devices are less dependent on short-channel effects. The SS and the I_{DSS} are slightly higher for the devices grown on CREE substrate, meaning that these devices are slower in turning on, but show a higher saturation current (regime value of current is higher). In the end R_{ON} seems to be smaller. However, the differences between the two substrates, even if found, were not that high to show a concrete dissimilarity. The only parameter which can be evaluated effectively diverse is the two-terminal gate-leakage current ($I_{GS,leak}$) that for CREE substrate devices appears smaller.

- CONTROL vs Back-Barrier: the presence of the back-barrier allows to reduce the possible leakage paths in the architecture: in fact both $I_{GS,leak}$ and $I_{D,leak}$ decrease as well as I_{DSS} in the devices where a back-barrier is present respect to the control one, which are the reference devices without back-barrier. Then $g_{m,peak}$ shows a different trend depending on the substrate: for CREE it seems decreasing while on the contrary for II-VI it increases. The change in transconductance peak is associated in the literature to the presence of trap state in the gate-to-drain access region, as reported in chapter 3, so probably a different mechanism of trapping in such region affects the two different substrate-based population of devices.

- Increasing concentration of aluminum Back-Barrier: It is registered that when aluminum concentration in the back-barrier layer is increased, for both substrates, V_{th} becomes more negative and consequently DIBL increases (in modulus) and then R_{ON} tends to become bigger too. Moreover, subthreshold slope (SS) tends to increase if a back-barrier is present in the device architecture. This means that the device is less able to turning on and off quickly, so a longer transient is required to pass from one state to the other. This is probably due to the fact that the insertion of aluminum causes the enhancement of strain stress due to to the differences in crystal lattice that could generate surface defects present in the structure, that in turn affect the device stability performances.

5.1.2 DC characteristics:

In the following pages, the characteristics of the most representative devices are reported. The characteristics were divided in two groups, to avoid the comparison between devices with different substrate. For this reason, the first four chips are analysed together (II-VI CONTROL and the CREE devices) and then the other (four II-VI devices).

$I_{GS} - V_{GS}$ characteristic

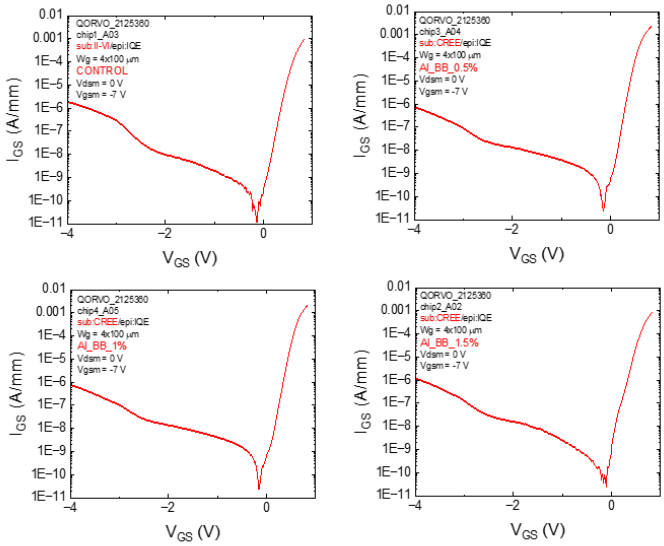


Figure 5.2 Comparison between CREE devices: I_GS- V_GS characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement condition are V_DS=0 V and V_GS=-7 V

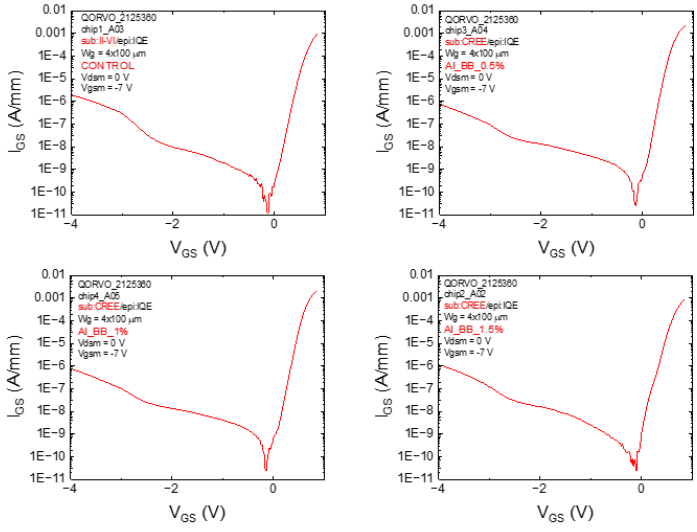


Figure 5.3 Comparison between II-VI devices: I_GS- V_GS characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement condition are V_DS=0 V and V_GS=-7 V

$g_m - V_{GS}$ characteristic

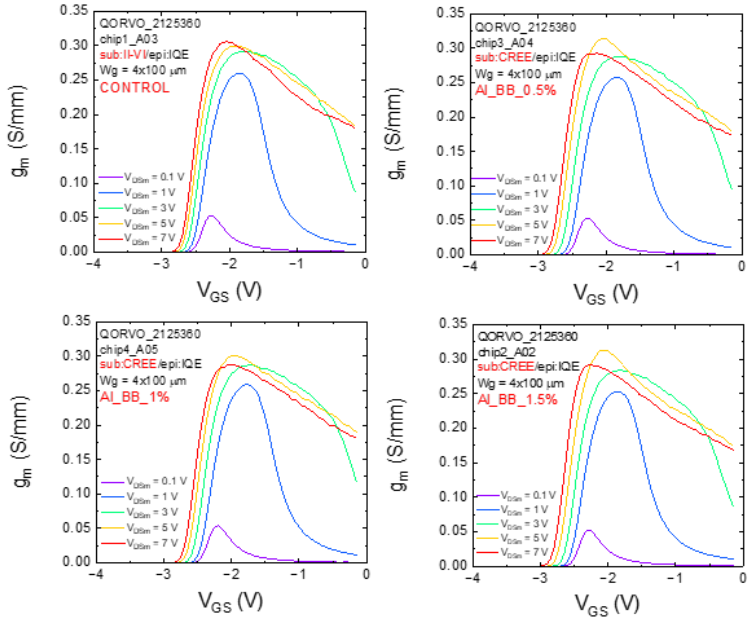


Figure 5.4 Comparison between CREE devices: $g_m - V_{GS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{DS} = 0.1,1,3,5,7\ V$

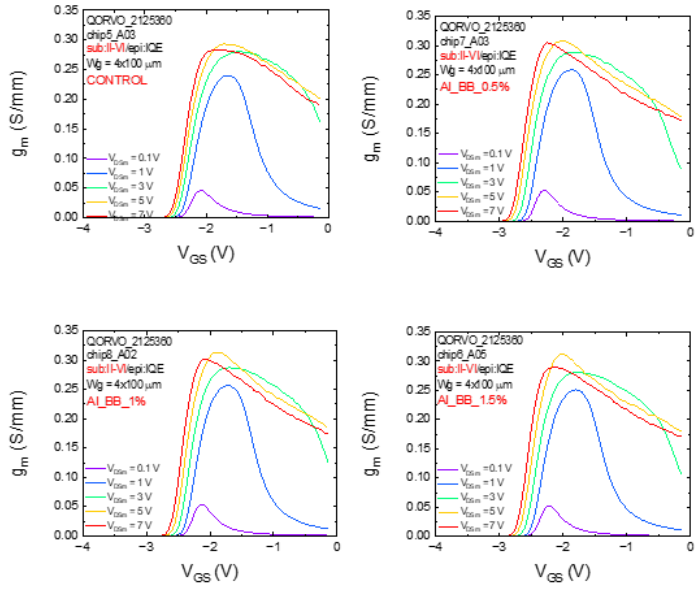


Figure 5.5 Comparison between II-VI devices: $g_m - V_{GS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{DS} = 0.1,1,3,5,7\ V$

$I_{DS} - V_{GS}$ characteristic

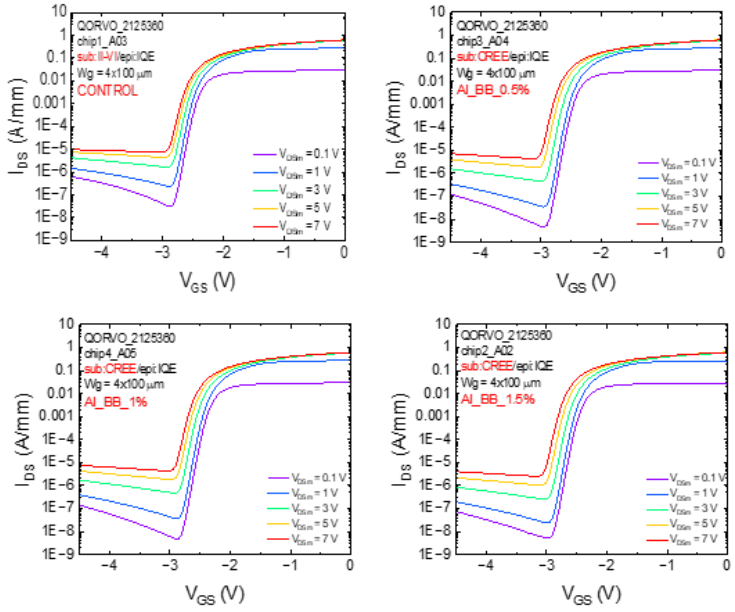


Figure 5.6 Comparison between CREE devices: $I_{DS} - V_{GS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{DS} = 0.1,1,3,5,7\ V$

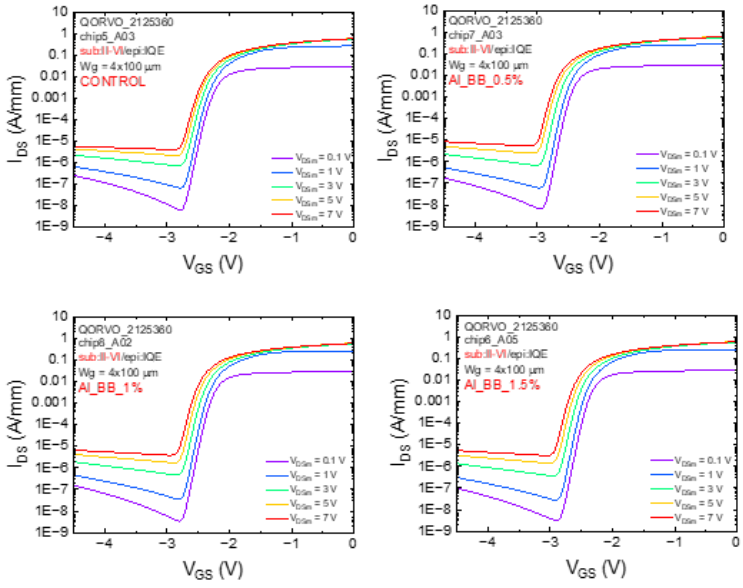


Figure 5.7 Comparison between II-VI devices: $I_{DS} - V_{GS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{DS} = 0.1,1,3,5,7\ V$

$I_{DS} - V_{DS}$ characteristic

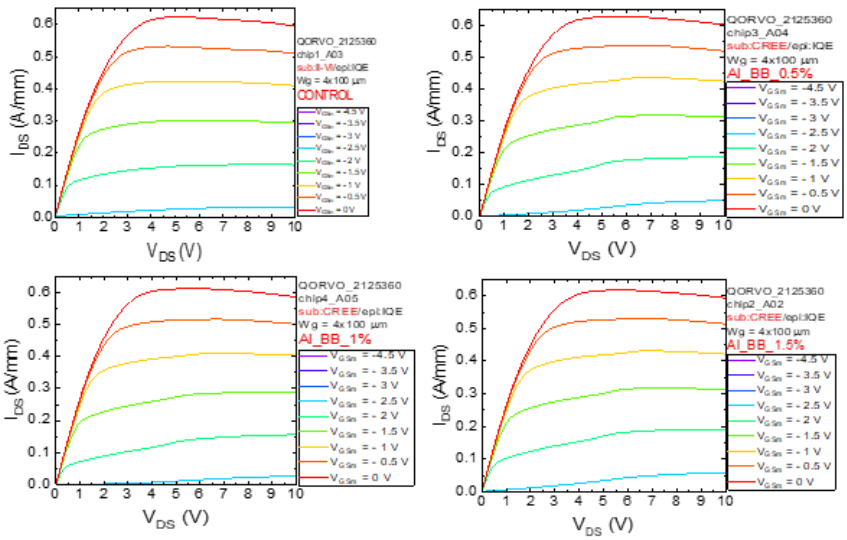


Figure 5.8 Comparison between CREE devices: $I_{DS} - V_{DS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{GS} = -4.5, -4, -3.5, -3, -2.5, -2, -1.5, -1, -0.5, 0\ V$

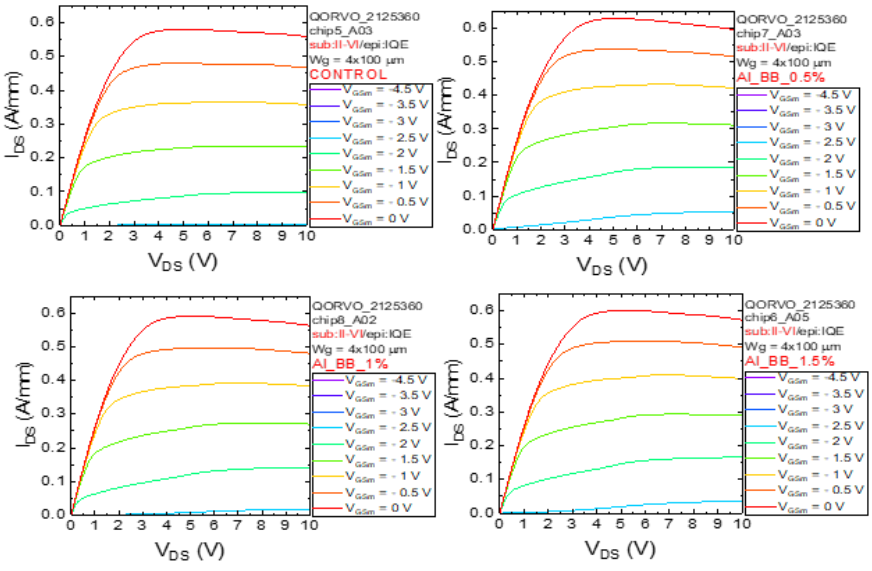


Figure 5.9 Comparison between II-VI devices: $I_{DS} - V_{DS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{GS} = -4.5, -4, -3.5, -3, -2.5, -2, -1.5, -1, -0.5, 0\ V$

$g_d - V_{DS}$ characteristic

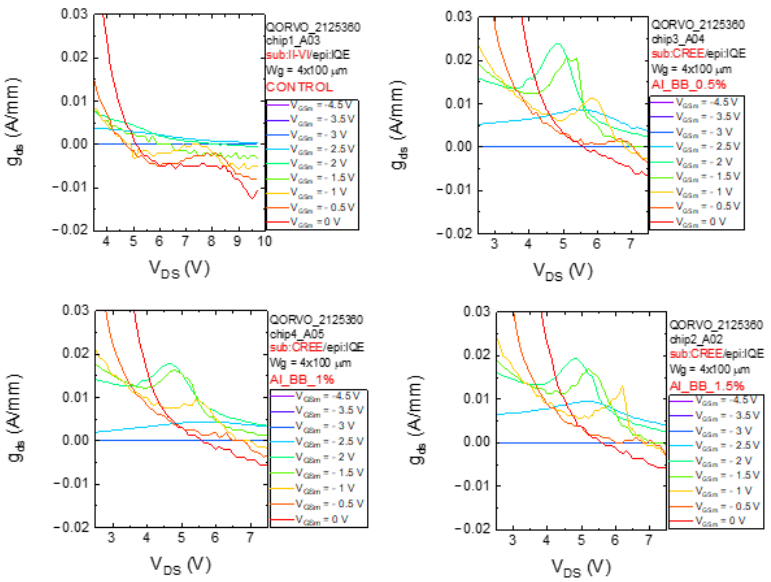


Figure 5.10 Comparison between CREE devices: $g_d - V_{DS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{GS} = -4.5, -4, -3.5, -3, -2.5, -2, -1.5, -1, -0.5, 0\ V$

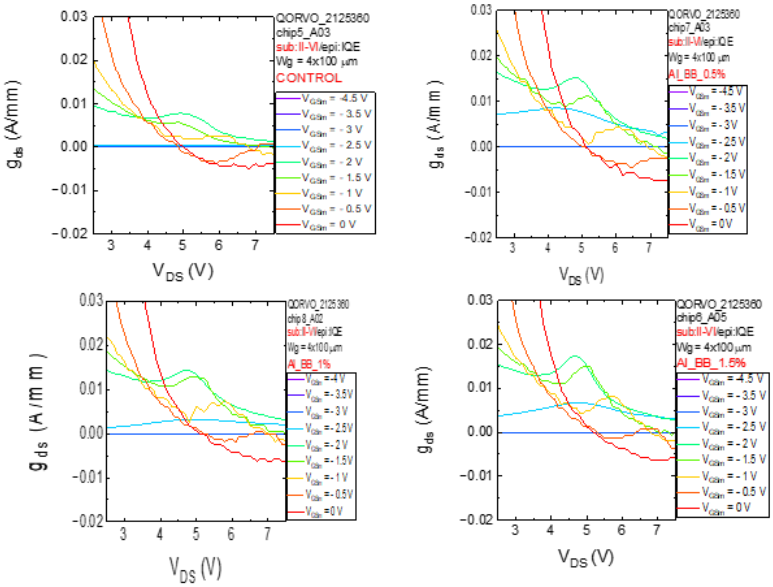


Figure 5.11 Comparison between II-VI devices: $g_d - V_{DS}$ characteristic. Starting from top left the CONTROL device, following the 0.5%,1% and 1.5% of aluminum back-barrier. The measurement conditions are $V_{GS} = -4.5, -4, -3.5, -3, -2.5, -2, -1.5, -1, -0.5, 0\ V$

Another intriguing observation stemming from the DC characterization pertains to the emergence of a distinctive feature within the $I_{DS} - V_{DS}$ characteristic. Evidently showcased in Figure 5.8 and 5.9, a noteworthy phenomenon unfolds during the transition of the device's operational states – from ON to semi-ON and OFF. Particularly when the V_{DS} voltage reaches relatively elevated levels, a discernible upsurge in drain current becomes evident. This peculiar behavior finds its explanation in what is known as the "kink effect." This phenomenon highlights that the process of detrapping, wherein charge carriers are released, is selectively activated solely at specific V_{DS} voltages. This activation is contingent upon the electric field's ability to efficiently facilitate the detrapment of previously captured charge carriers. This fact is emerging also as the presence of a moving peak from $g_d - V_{DS}$ characteristics. Based on those results, in section 5.3 it will be treated a deeper DC analysis, aimed to investigate more in detail the difference between trapping and detrapping mechanisms.

5.2 Double pulse analysis

Within this paragraph, the results of the double-pulse measurements are reported. The measurements were executed under room temperature conditions, and they required a careful choice of the stress bias conditions. As previously indicated in chapter 4, the choice of the bias holds great importance, since different biases can enhance the activation of different type of traps, potentially present in distinct segments of the structure. Through the application of a negative voltage bias at the gate contact, and a neutral bias at the drain terminal ($V_{GS,stress} < 0\ V, V_{DS,stress} = 0\ V$), trapping events associated with traps in the gate region are enhanced. On contrary, the impact on the other sections of the device is minimal. The traps positioned below the gate region produced a variation in the threshold voltage and consequently in the saturation current. In HEMT devices, trapping predominantly involves electron capture due to the limited availability of holes. For this reason, what is commonly observed is a shift toward right of the threshold voltage followed by a reduction in the saturation current. Alternatively, by applying a negative voltage bias to the gate terminal coupled with a positive bias to the drain ($V_{GS,stress} < 0\ V, V_{DS,stress} > 0\ V$), the trapping in the gate-to-drain regions is improved. The cumulative effect of these two voltages amplifies trapping events underneath the gate and within the gate-to-drain portion of the device, since the electric field is more intense, Traps situated between the gate and drain junction typically lead to a decrement in the transconductance peak and an increase in device on-resistance. The performed measurements encompassed the following bias configurations:

1. $V_{GS,stress} = -5\ V, V_{DS,stress} = 0\ V$
2. $V_{GS,stress} = -6\ V, V_{DS,stress} = 0\ V$
3. $V_{GS,stress} = -7\ V, V_{DS,stress} = 0\ V$
4. $V_{GS,stress} = -8\ V, V_{DS,stress} = 0\ V$
5. $V_{GS,stress} = -7\ V, V_{DS,stress} = 5\ V$
6. $V_{GS,stress} = -7\ V, V_{DS,stress} = 10\ V$
7. $V_{GS,stress} = -7\ V, V_{DS,stress} = 20\ V$
8. $V_{GS,stress} = -7\ V, V_{DS,stress} = 30\ V$

9. $V_{GS,stress} = -7\ V, V_{DS,stress} = 40\ V$
10. $V_{GS,stress} = -7\ V, V_{DS,stress} = 50\ V$

Between every baseline, a measurement performed without applying any stress bias ($V_{GS,stress} = 0\ V, V_{DS,stress} = 0\ V$) has been performed. In this way it was possible to see if the device, after the stress, has completely recover or not. Since in the initial experiments this negative effect, named as "memory effect", has been recognized, certain strategies were used to limit it. Initially after every measurement, a time of 5 minutes was waited between one stress and the other to see if the reset of the devices was sufficient. Unfortunately, this didn't happen. So, in order to have a complete recovery and empty the traps the devices were illuminated for 10 minutes with the light of the microscope. This was done, since the photon present in the light are able to give sufficient energy to the trapped carrier, to allow them to overcome the potential barrier and being detrapped. Then the device was left for 5 minutes in a dark place in order to allow the generated electrons and holes pairs to recombine. With this procedure, it was possible to completely eliminate the memory effect. Regarding the stress, the first four baseline were used to evaluate the presence of traps under the gate region only. The last six instead, were used to investigate on the presence of defects in the gate-to-drain access region. The results of the double pulse measurements are reported. Even in this case, the results were compared considering the effect of: (i) different substrate producer, (ii) presence or not of a back-barrier (iii) concentration of Al in the back barrier.

The measurement conditions used were the following: a fill time of 100 seconds, a pulse width of 1 microsecond. The delay used was 400 nanoseconds, while the integration interval ranged from 1.8 microseconds tio 2 microseconds. In the end the drain/gate raise and fall time were set at 200 nanoseconds. Instead, in the following are summarized the main measurement conditions used for both the type of characteristic:

The $I_{DS} - V_{GS}$ conditions are the following: the drain measure voltage is kept at 5 V ($V_{D,M} = 5\ V$), while the voltage at the gate starts at -5 V ($V_{G,start} = -5\ V$) ends at 0 V ($V_{G,stop} = 0\ V$) with a step of 0.2 V ($V_{G,step} = 0.2\ V$

The $I_{DS} - V_{DS}$ conditions are the following: the gate stops at 0 V with a step of 0.2 V ($V_{G,stop} = 0\ V, V_{G,step} = 0.2\ V$) while the drain voltage starts at 0 V ($V_{D,start} = 0\ V$) and ends at 10 V($V_{D,stop} = 10\ V$)

After all the data have been extracted and processed, the characteristics were derived. The plots of them are reported for completeness at the end of the paragraph. In order to get deeper in the analysis, the threshold voltage variation from the $I_{DS} - V_{GS}$ curves and the current collapse from the $I_{DS} - V_{DS}$ curves are studied. In the following, the trend observed are reported:

Threshold voltage variation CREE

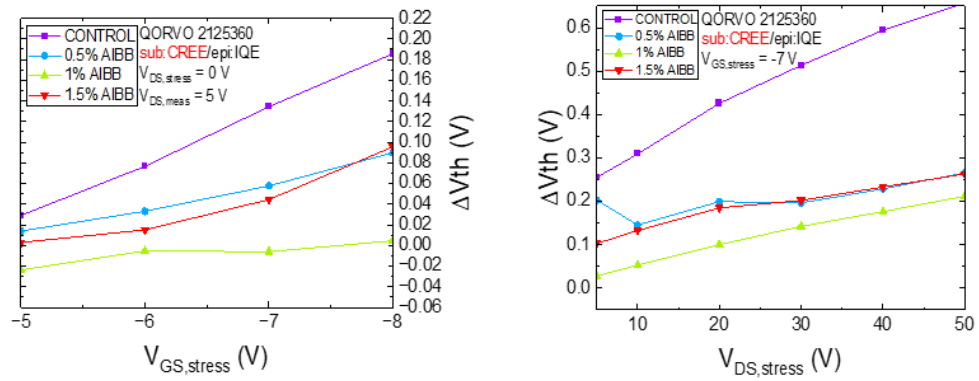


Figure 5.12 Threshold voltage variation: at the left when the drain voltage is fixed at zero while the gate voltage increases (stress only at the gate). At the right when the gate voltage is fixed at -7 V while the drain voltage increases (stress in the gate-to-drain region)

Current Collapse CREE

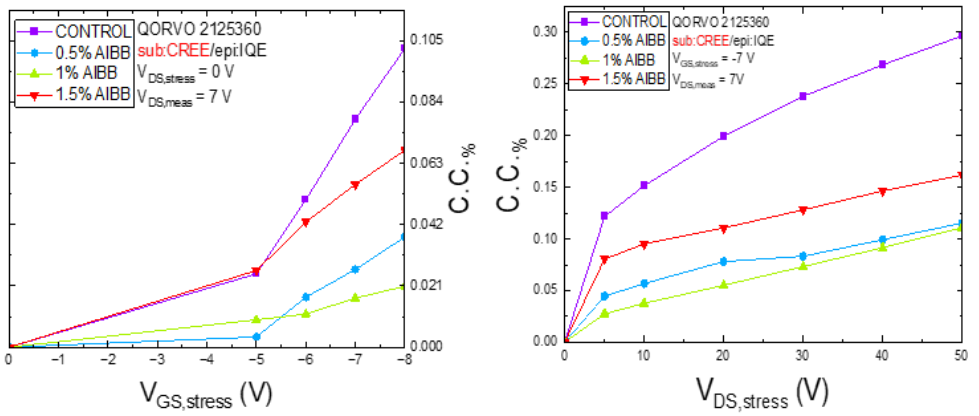


Figure 5.13 Current collapse: at the left when the drain voltage is fixed at zero while the gate voltage increases (stress only at the gate). At the right when the gate voltage is fixed at -7 V while the drain voltage increases (stress in the gate-to-drain region)

Thresold voltage variation II-VI

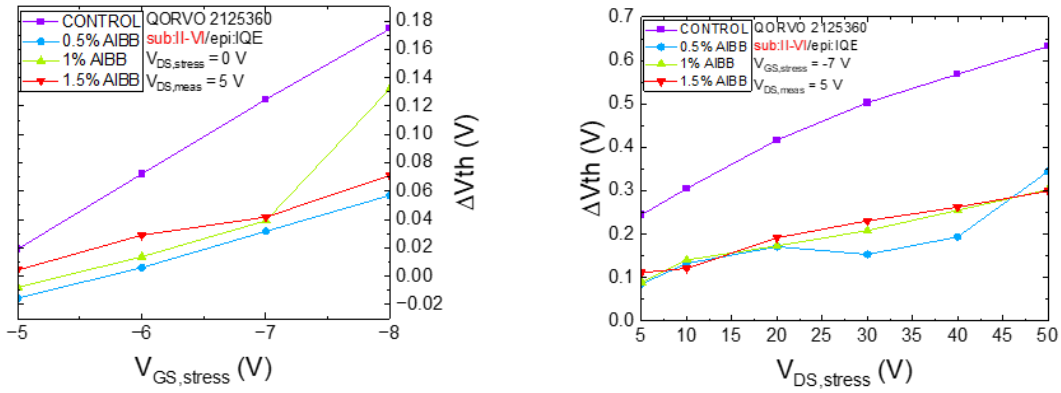


Figure 5.14 Threshold voltage variation: at the left when the drain voltage is fixed at zero while the gate voltage increases (stress only at the gate). At the right when the gate voltage is fixed at -7 V while the drain voltage increases (stress in the gate-to-drain region)

Current Collapse II-VI

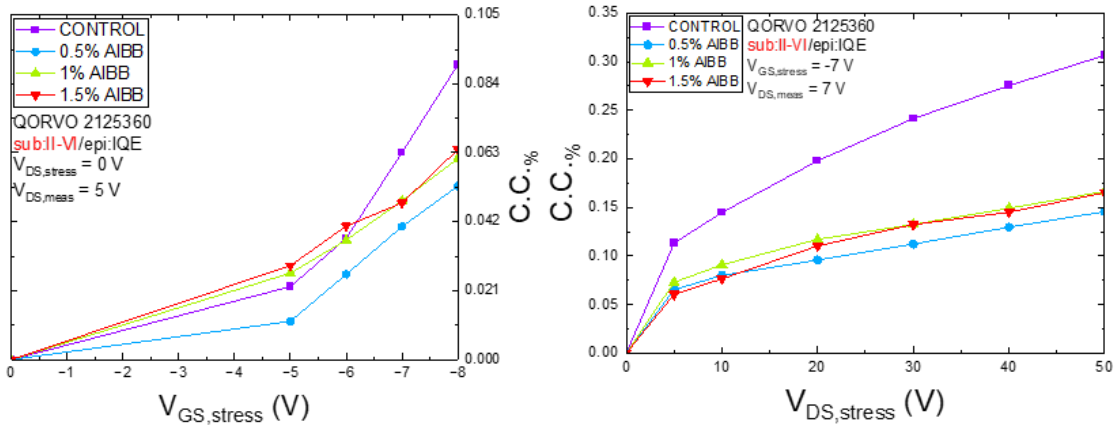


Figure 5.15 Current collapse: at the left when the drain voltage is fixed at zero while the gate voltage increases (stress only at the gate). At the right when the gate voltage is fixed at -7 V while the drain voltage increases (stress in the gate-to-drain region)

From the Double Pulse analysis emerges that first of all memory effect was recognized during the measurements. Its presence was detected observing the difference between the measure done after the stress, without imposing stresses ($V_{GS,stress} = 0\ V, V_{DS,stress} = 0\ V$) with the reference one executed before stressing the device . This means that the detrapping was slower than the time between two subsequent measurements; thus, the effects were cumulating. This was solve illuminating the device as previously explained.

Then both threshold voltage variation, which is the change in the threshold voltage when the stress is increased, and current collapse, which is the variation in drain current are analysed. They're formula are reported here:

$$\Delta Vth = Vth, stress - Vth, 0{,}0 \qquad (5.1)$$

$$C.C. = \frac{I_{DS,0,0} - I_{DS,stress}}{I_{DS,0,0}} \qquad (5.2)$$

The change in threshold voltage that is registered after the stress is a finite value coming from the comparison with the initial value of threshold voltage $Vth, 0{,}0$ before the stress. The variation of drain current is in percentage, extrapolated from the comparison with its original value $I_{DS,0,0}$. From these parameters, the following results are observed:

- CREE vs II-VI substrates: In both substrate cases, a monotone trend has been recognized both for threshold voltage variation and current collapse. This means that increasing the stress condition enhances the dispersion and the variation of parameters. In fact, by keeping the drain voltage fixed it is clear that increasing the voltage at the gate contributes to a larger variation of the threshold voltage and of the current collapse from their original value. This is also observed when the gate voltage is fixed and the drain voltage is increased. As a result, no significant differences are observed between the two substrates, which show a similar behaviour.

- CONTROL vs back-barrier: Another point that emerges is that the CONTROL devices in both substrate cases show a larger variation, while with the presence of back-barrier the change in threshold voltage and current collapse is reduced. This confirms the fact that the introduction of a back-barrier contributes to have a better confinement of carriers in the channel, contributing to reduce the dispersion inside of the devices.

- Increasing concentration of Aluminum Back-Barrier: no particular trend has been found that links the increasing concentration of aluminum in the back-barrier and the threshold voltage variation. However, it is found for current collapse: for CREE and II-VI the observed trend are the following (going from the device with most dispersion to that with the lowest level of dispersion encountered):

  -CREE: CONTROL →1.5% Al_BB → 0.5% Al_BB → 1% Al_BB

  -II-VI: CONTROL →1% Al_BB → 1.5% Al_BB → 0.5% Al_BB

  In particular, a hypothesis has been made for the trend related to II-VI devices: in a first approximation, the presence of back-barrier is able to strengthen the electron confinement in the channel. However, when the concentration of aluminum is increased, also the strain stress is enhanced, due to the increasing lattice mismatch of the two layers. In this way, it is probable that surface defects have been generated, leading to a greater dispersion and contributing to reduce the level of current.

In the end, considering the experimental data is possible to summarize the results as follow. An increase in the stress voltages causes an enhancement in current collapse, and threshold voltage variation, and confirm the presence of traps inside the structure. When an higher stress voltage is applied the electric field inside the device is enhances; Therefore, the trapping centers are reached with a bigger fluence of carriers resulting in

an enhanced trapping activity. The presence of a back-barrier in the device has proven to be able to reduce the trapping activity. This is probably related to the better isolation between the 2-DEG, and the doped GaN buffer. Therefore, iterations between the carriers and the trapping centers in the buffer are significantly reduces. Considering the trend observed for the current collapse, the devices grown on II-VI substrate showed a similar behaviour to the ones grown on CREE substrates proving that the substrate has a minimum impact on the stability issues. In both cases the worse current collapse for devices with a higher Al concentration in the back barrier was hypothesise to be related to the introduction of interface traps. The higher density of interface traps was associated with the higher Al concentration. The main reason is that by increasing the Al percentage in the back-barrier, as stated by the Vegard's law, there is a wider lattice mismatch between the two materials. In order to verify this hypothesis further experiments are required.

In the following, the curves obtained during the characterization are reported for completeness.

I_DS - V_GS CREE

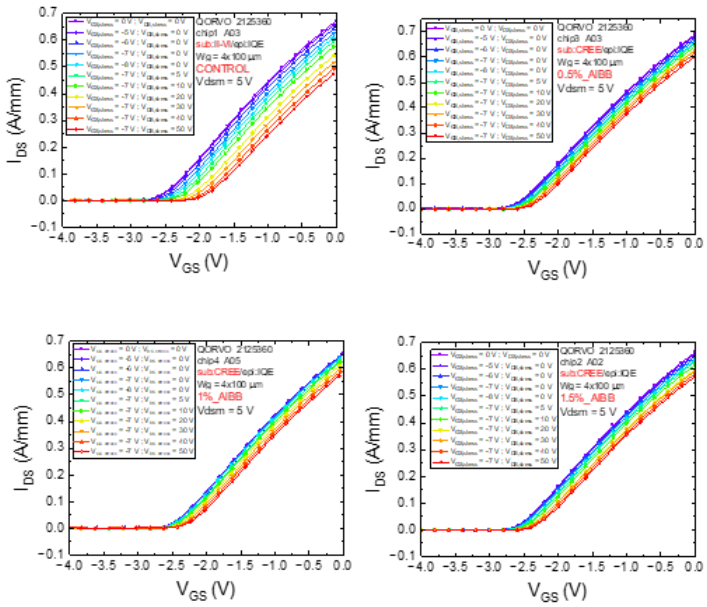


Figure 5.16 IDVG curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

g_m – V_GS CREE

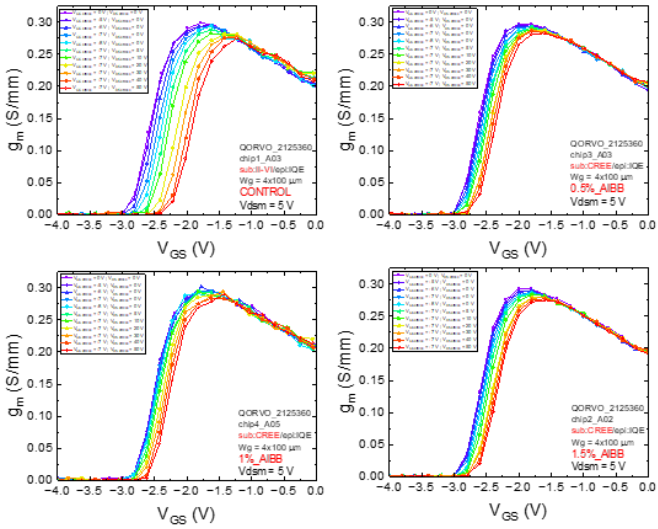


Figure 5.16 transconductance curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

I_DS – V_DS CREE

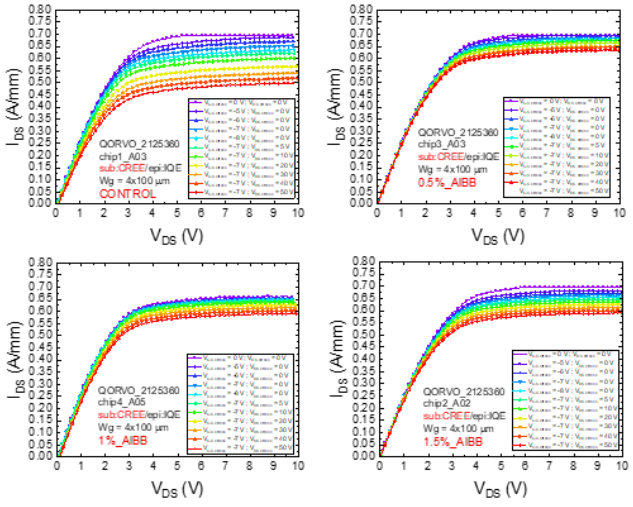


Figure 5.17 transconductance curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

I_DS – V_GS II-VI

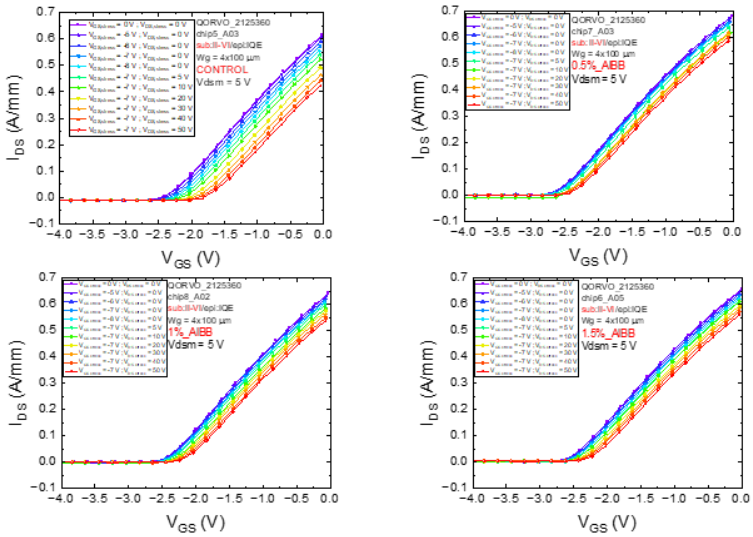


Figure 5.18 IDVG curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

g_m – V_GS II-VI

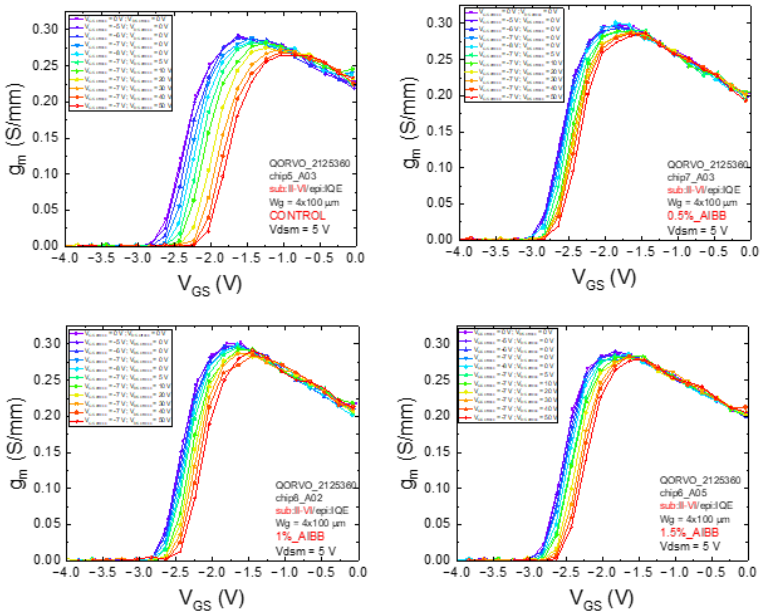


Figure 5.19 transconductance curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

I_DS – V_DS II-VI

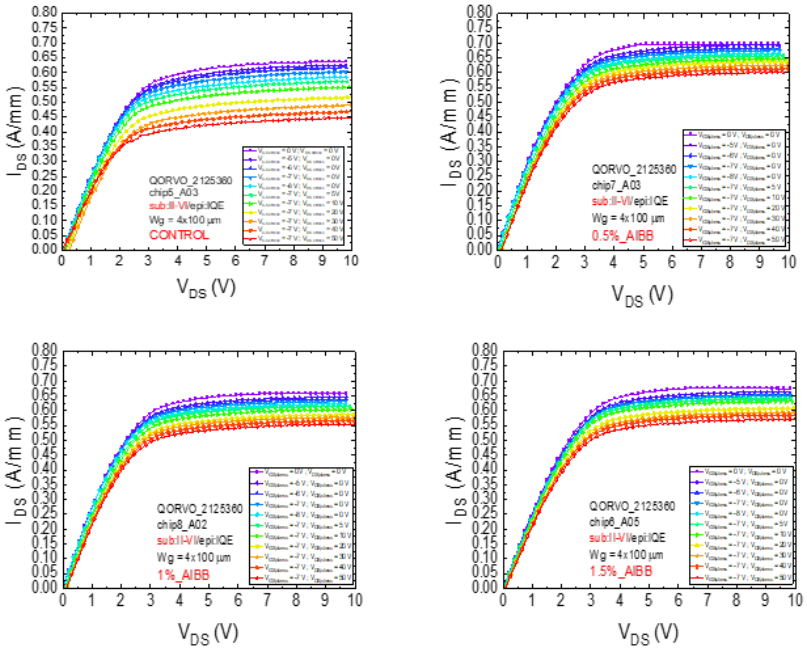


Figure 5.20 IDVD curves obtained from Double pulse measurement at different voltage stress. At the top-left there is the CONTROL device, and then the percentage of aluminum in the back-barrier increases.

5.3 DC go and back analysis

Another thing that was interesting to notice from the already discussed DC characterization was the presence of a kink in the I_DV_D characteristic: in fact, as it can be seen from Figure 5.7 and 5.8, as soon as the device passes from the ON to the semi-ON and OFF state, when the V_{DS} voltage is relatively high, an increase of the drain current is detected. This can be attributed to the so-called kink effect, meaning that the detrapping mechanism is activated only at certain V_{DS} , because only at this voltage the electric field can effectively detrap the charge carriers previously captured. From this observation the idea to study if the trapping and detrapping mechanisms behave differently emerged. In order to do that, a DC go and back analysis was performed. This type of measurements consists in stressing the device, usually in OFF-state, and then perform a two DC measurement (Go and BACK), at first executing a sweep of the voltage from a low value to a high value and vice versa. Considering the case of the I_DV_D measurements the Go measure is done imposing a fixed gate voltage and the by increasing the drain current from 0 V to $V_{DS,MAX}$. On contrary, the BACK measure is done imposing a fixed gate voltage, and then decreasing the drain voltage from $V_{DS,MAX}$ to 0 V. As first step, the bias conditions were chosen, considering the results of the double pulse measurements, and selecting the most stressful ones. Than the study proceeded, performing at the same stress $I_{DS} - V_{GS}$ characteristics. These curves where performed first increasing V_{GS} and then decreasing it. This was done in order to see which kind of differences arose. Considering I_DV_G, I_DV_D, and g_mV_G characteristics, many information can be estracted from them, for example, if there are variation in the R_{ON}, V_{TH}. . In addition, to eliminate memory effect between different stresses, illumination with microscope for 10 minutes plus 5 minutes of dark where used as reset. For each device, the set of bias condition were:

- $V_{GS,stress}$= 0 V, $V_{DS,stress}$ = 0 V, stress time = 1 s
- $V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V, stress time = 100 s
- $V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 50 V , stress time = 100 s

Then at each measure, $g_m - V_{GS}$ characteristics were extrapolated with the following conditions, resumed by table 5.3:

	$g_m - V_{GS}$
GO measure	$V_{G,start} = -5\ V$ $V_{G,stop} = 0\ V$
BACK measure	$V_{G,start} = 0\ V$ $V_{G,stop} = -5\ V$

Table 5.3 DC go and back conditions for gm-VGS and IDS-VDS curves

In the following are reported the curves obtained during the analysis:

CREE GO

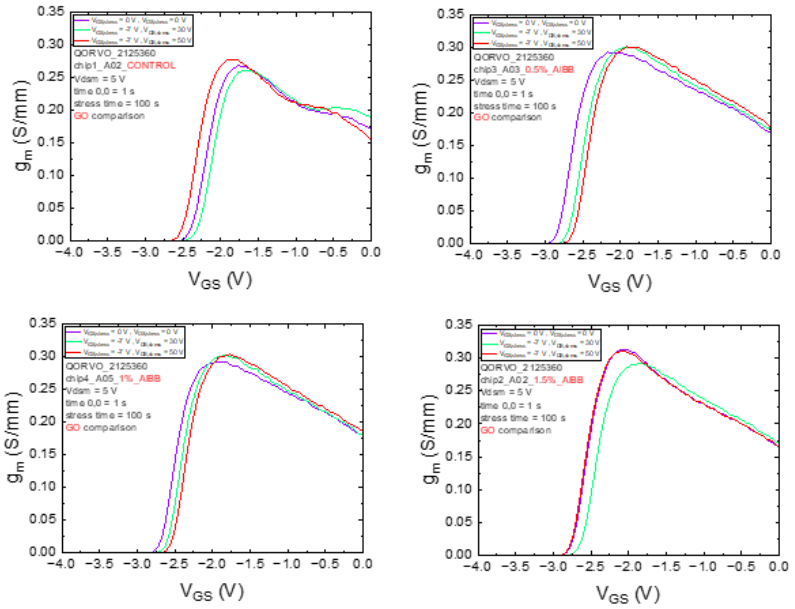


Figure 5.21 DC go and back: gm-VGS comparison between CREE during the GO conditions

CREE BACK

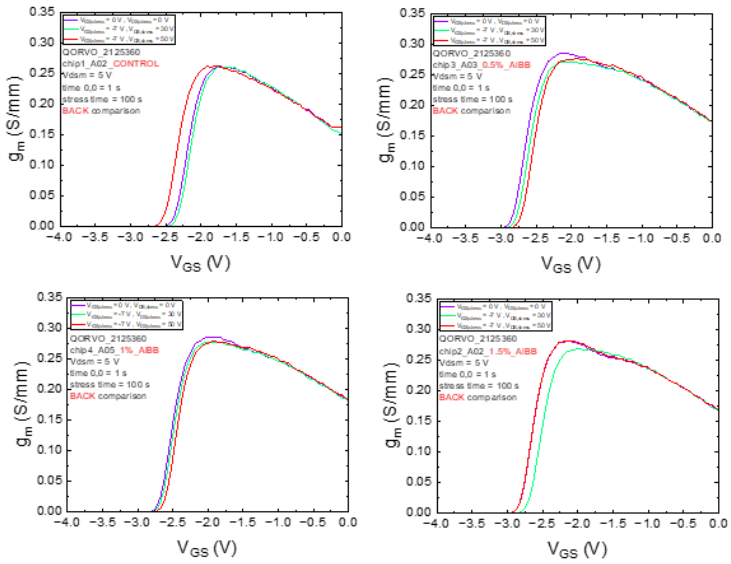


Figure 5.22 DC go and back: gm-VGS comparison between CREE during the BACK conditions

CREE GO and BACK

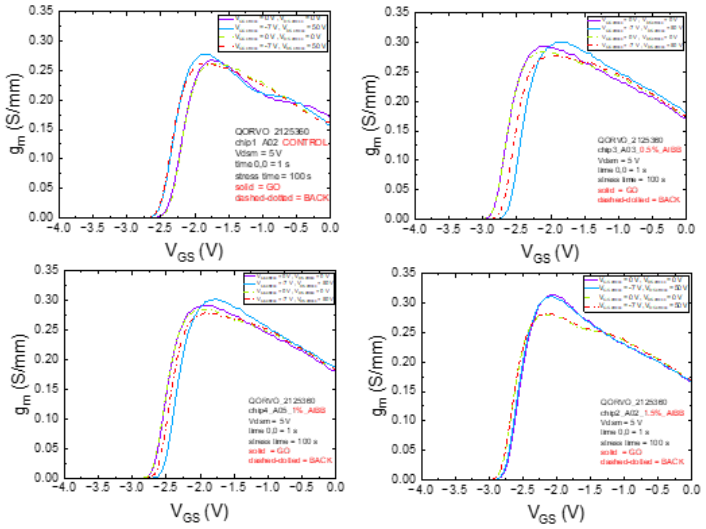


Figure 5.23 DC go and back: gm-VGS comparison between CREE

II-VI GO

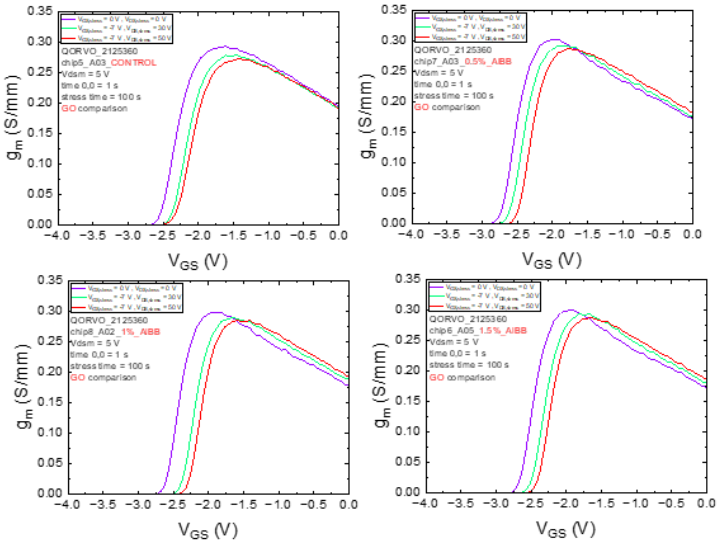


Figure 5.24 DC go and back: gm-VGS comparison between II-VI during the GO conditions

II-VI BACK

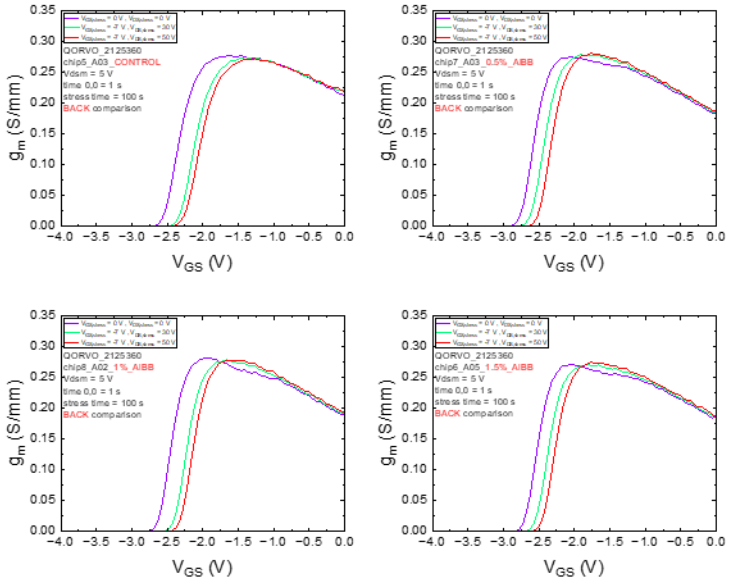


Figure 5.25 DC go and back: gm-VGS comparison between II-VI during the BACK conditions

II-VI GO and BACK

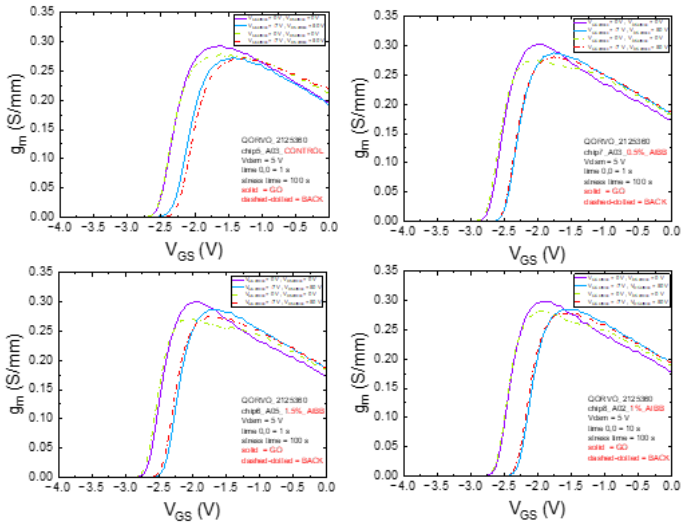


Figure 5.26 DC go and back: gm-VGS comparison between II-VI

The main results obtained from this analysis are the following: for both set of devices, the main difference between go and back measurement is that the peak of transconductance is higher during the go phase and lower during the Go one. This suggest that detrapping related phenomena are activated during the Go measurement. There is also present an asymmetry between CREE and II-VI: while in CREE with increasing stress the curves shift to the left, with II-VI the characteristics shift to the right.

5.4 Vth transient

In this section, the results of the Vth transient measurements are reported. As already anticipated in the previous chapter, while the I-V characteristics obtained from the prior double pulse measurements allowed us to explore certain aspects like the presence of traps and estimate their location, it lacked of the capability of provide insights of the dynamics of trapping and detrapping mechanisms. To address this gap, Vth transient measurements were conducted. This measurement's technique involves the observation of the drain current's evolution, extrapolated considering a fixed voltage at which the I_DV_G curves are interpolated. Unlike previous measurements, Vth transient measurements offers a means to derive the Arrhenius plot, aiding in the identification of associated traps. The main results obtained are the ones which follows. First of all, a preliminary characterization was conducted, maintaining the temperature fixed at 25°C and using different stress conditions both in OFF-state and semi-ON state in order to estimate the better bias conditions. For that characterization the CONTROL wafers and the chip with 1.5% Al_BB with II-VI substrate were chosen as sample. This preliminary part gave us the thrust to proceed with a full comparison of the OFF-state stress for all the chips, both from CREE and II-VI. This allowed us to compare if the results obtained from double pulse measurements about current collapse, and VTH shift were confirmed or not by VTH transient measurements. Then, in order to investigate the root causes of the trapping mechanisms, the CONTROL device was chosen and it was analysed in temperature. The analysis in temperature allow the extraction of the time constants associated to the defect, at different temperatures, and subsequently it allows to build the Arrhenius plot. In this way, the activation energy of the traps could be determined and then it could be compared with the activation energies of the traps known in literature. Finally, a hypothesis on the traps origin and nature can be done. In the end for the 1.5% Al_BB with a II-VI substrate, another analysis was conducted: maintaining the temperature fixed at 25°C, a semi-ON stress was performed. This was done in order to discriminate if the degradation phenomena due by trapping was mainly caused by hot-electrons or self-heating effects.

Here, the conditions used for each of the step of the analysis are reported: as stress time it has been chosen 100 seconds, while for the recovery phase 1000 seconds were

decided. For the (0,0) measurements stress and recovery time have been set at 10 seconds. The voltage that as be monitored at which the current was extrapolated was chose at -1.5 V (VGS,interp = -1.5 V). The pulse that has been used for VDS was 5 V (VDS,impulse = 5 V). In the end, the pinch-off current was decided to be 1 mA (I_pinch-off = 1 mA).

In the following, the main results as well as the specific conditions used for every part of the analysis are reported:

Preliminary OFF and semi-ON state stress

The CONTROL and the 1.5 % Al_BB from II-VI were analyed. Between every stress, as during the Double Pulse characterization, the device was placed under the microscope light for 10 minutes and then the device was kept in dark condition for other 5 minutes. In this way the device was able to completely recover between to consecutive measurements, and the memory effect was eliminated. The stress and measurement conditions used were:

-OFF-state stress:

- $V_{GS,stress}$= 0 V, $V_{DS,stress}$ = 0 V
- $V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 0 V
- $V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V

-semi-ON state stress:

- $V_{GS,stress}$= 0 V, $V_{DS,stress}$ = 0 V
- $V_{GS,stress}$= -1.5 V, $V_{DS,stress}$ = 3 V
- $V_{GS,stress}$= -2 V, $V_{DS,stress}$ = 7 V

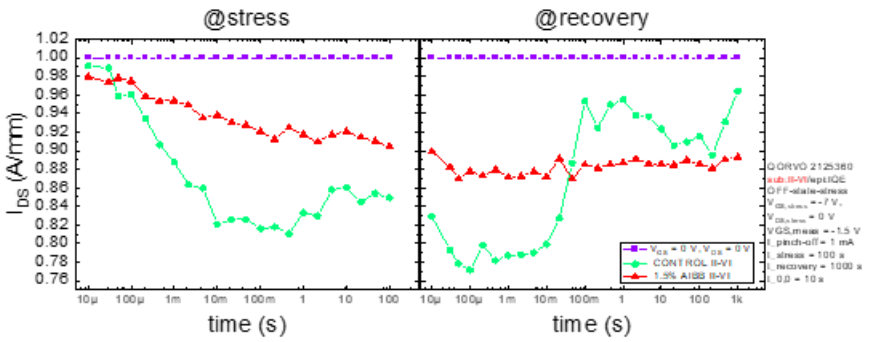


Figure 5.27 Vth transient: OFF-state stress (VGS = -7 V, VDS = 0 V) , CONTROL and 1.5% Al_BB

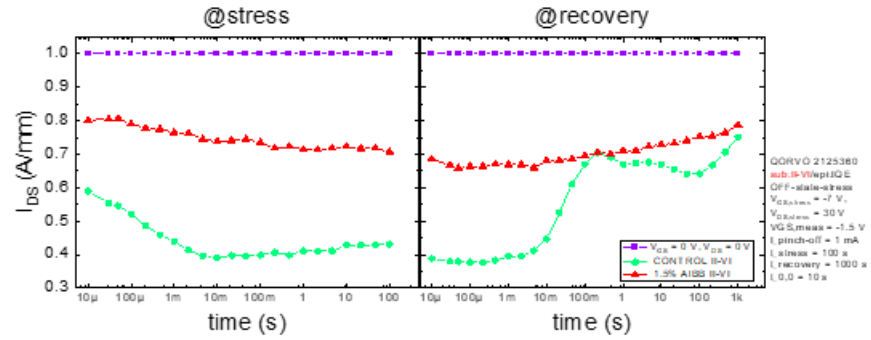


Figure 5.28 Vth transient: OFF-state stress (VGS = -7 V, VDS = 30 V) , CONTROL and 1.5% Al_BB

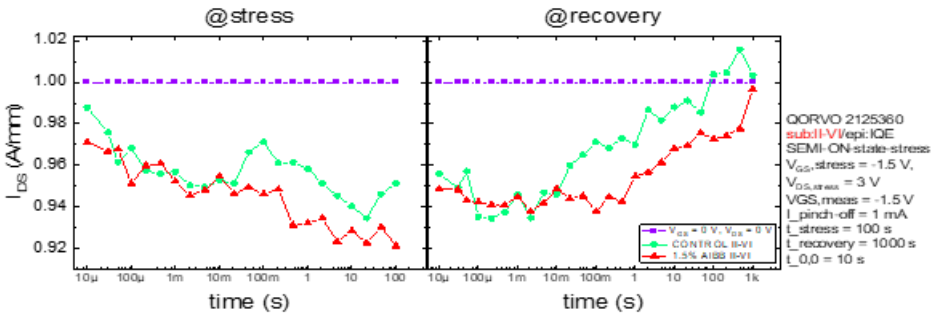


Figure 5.29 Vth transient: semi-ON-state stress (VGS = -1.5 V, VDS = 3 V) , CONTROL and 1.5% Al_BB

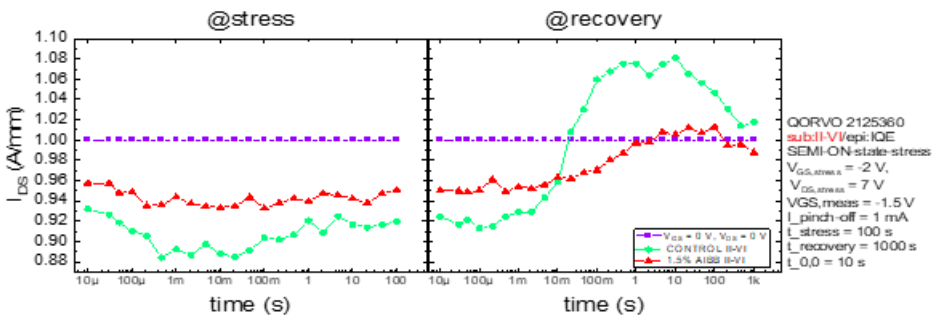


Figure 5.30 Vth transient: semi-ON-state stress (VGS = -2 V, VDS = 7 V) , CONTROL and 1.5% Al_BB

After this step, a complete characterization adopting an OFF-state stress with the following bias conditions ($V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V) was done for the devices with both substrates.

Off-state stress

Both CREE and II-VI substrate were analysed, studying all chips' behaviour. The analysis were conducted at room temperature (25°C) and with the off-state bias condition ($V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V).

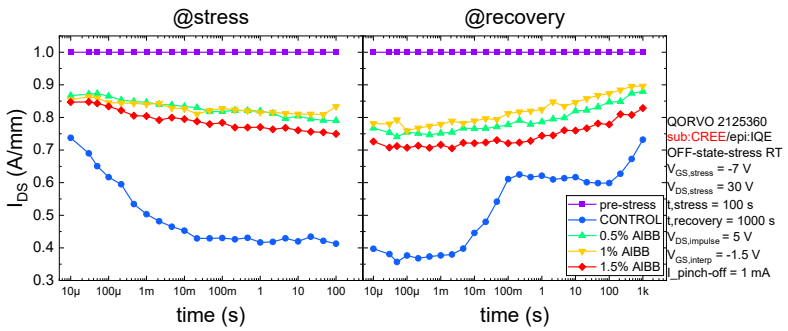


Figure 5.31 Vth transient: OFF-state stress at VGS = - 7 V, VDS = 30 V for CREE substrate devices

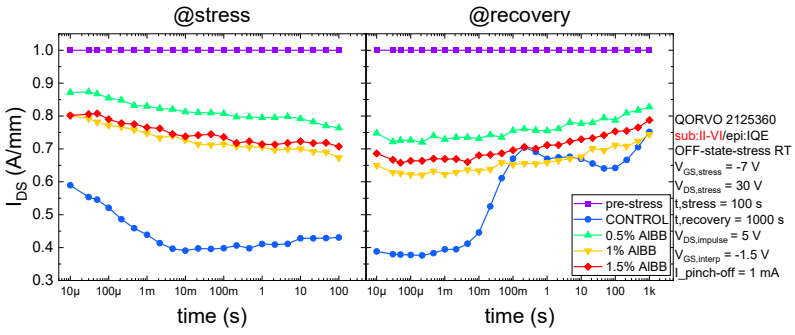


Figure 5.32 Vth transient: OFF-state stress at VGS = - 7 V, VDS = 30 V for II-VI substrate devices

From this step, some results were obtained: first of all, the control device showed a greater dispersion with respect to the devices with a back-barrier Those results confirms the findings of the double pulse measurements concerning the current collapse. Moreover, It is also possible to see that the devices can't return to the original pre-stress value after the recovery phase: this proved the presence of a memory effect for this devices. If the processes are thermally activated, repeating the measurements with the same bias condition, but at higher temperature, the processes can be accelerated enough to allow a complete recovery in 1000s. In the end, two trends are extracted, one for each substrate type set of devices, where the dispersion for the different concentration of aluminum in the back barrier is compared (starting with the device with the greater dispersion):

-CREE: CONTROL →1.5% Al_BB → 0.5% Al_BB → 1% Al_BB

-II-VI: CONTROL →1% Al_BB → 1.5% Al_BB → 0.5% Al_BB

Comparing these two trends with the ones obtained during the Double Pulse analysis, a perfect matching is found. This probably confirm the hypothesis that the introduction of a back-barrier can better isolate the buffer, contributing to lower the leakages due to the iteraction between the carrier and the buffer traps, but when the concentration of aluminum in the back/barrier is enhanced, the stress due to the strain and to the mismatch in lattice constant can produce other defects (that may act as traps) such surface defects.

Vth-transient in Temperature

In order to see the impact of temperature, and if the trapping mechanisms are thermally activated, VTH transient measurements were executed on Control devices the bias condition used to stress the device was kept constant and equal to ($V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V). The temperatures at which VTH transient measurements were executed are the following ones:

- T = 25°C

- T = 50°C
- T = 75°C
- T = 100°C
- T = 125°C
- T = 150°C

This is done thanks to a thermal chuck powered by an external controller. Between every temperature stress, as during the Double Pulse characterization, a "reset" was done using the microscope light for 10 minutes and keeping the device in dark condition for other 5 minutes. In this way memory effect was eliminated.

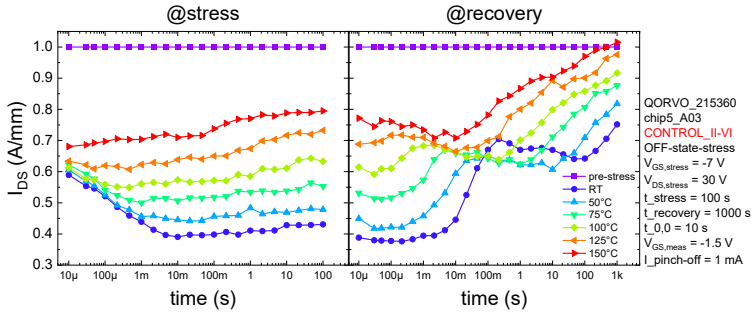


Figure 5.33 Vth transient: CONTROL II-VI; VGS = -7 V, VDS = 30 V; with increasing temperature

As can be noted the process is thermally activated. By increasing the temperature, the device is able to recover totally (may be also over recovery) reaching the initial pre-stress conditions. In addition, it can be seen that transients are present only during the recovery phase: all the transients were associated to double stretched exponential but only for the first three temperature (25°C, 50°C, 75°C) it was possible to make a correct fit. By fitting them the following time constants were found:

Temperature	25 °C	50°C	75°C
Time-constant τ_1	0.03 s	0.0066 s	0.0011 s
Time-constant τ_2	4629.7 s	954.44 s	220.26 s

Table 5.2 From figure 5.22, in the recovery phase, it was possible to recognize a double-stretch exponential behaviour for the first three temperature associated curves. In this table the two-time constants associated to each of the two part of the double-stretched exponential are extracted by fitting for every temperature related curve.

Inserting the time constants into the Arrhenius plot the following signatures were found:

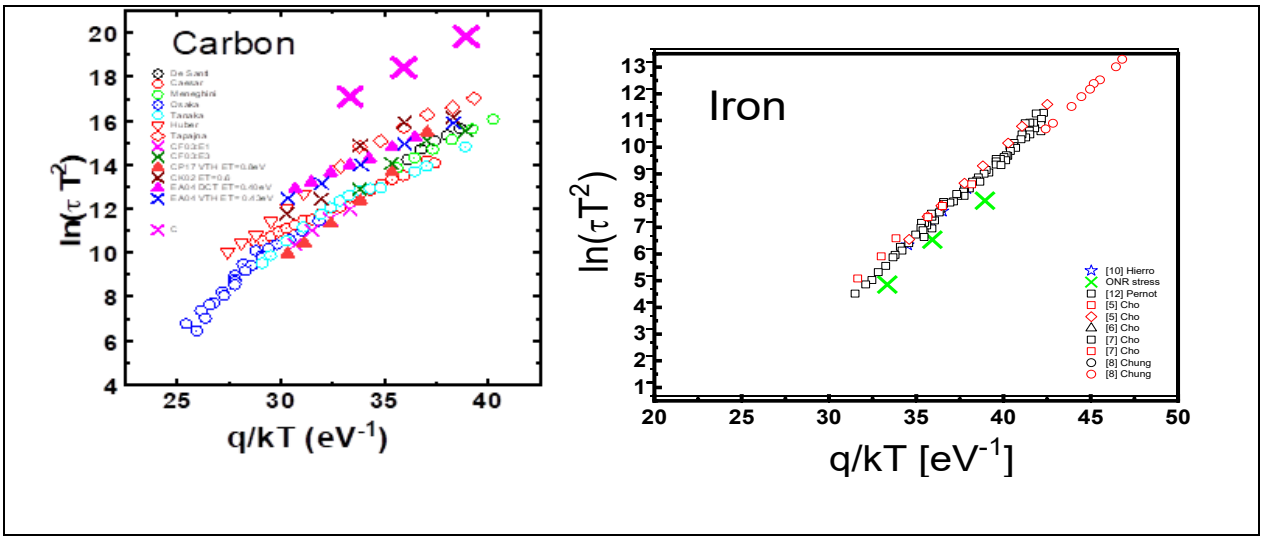


Figure 5.23 At the left: the three-time constant τ_1 associated to the first part of the double exponential gives a result compatible to Iron doping. At the right: the three-time constant τ_2 associated to the second part of the double exponential gives a result compatible to Carbon doping [41]-[45].

In the end, by comparing the results obtained with the Arrhenius plot, it was possible to determine that the trapping mechanisms associated with the exponential transients in the recovery phase of the current analysis are mainly due to the presence of iron and Carbon doping in the buffer layer. In fact, although this technique allows one to reduce the leakage path of electrons under the channel and improve their confinement, at the same time it introduces trap states able to lower the current flowing.

Vth transient: Variable recovery in semi-ON state

In the end, in order to discriminate if the trapping events associated with the transients found in the previous sections were mainly caused by hot-electrons or self-heating effects, an ultimate step has been made: it was chosen the 1.5 % Al_BB II-VI as a reference device. The stress phase was fixed in OFF-state: ($V_{GS,stress}$= -7 V, $V_{DS,stress}$ = 30 V) for all the measurements while the bias imposed during the recovery was changed. To avoid the insurgence of the memory effect, after every measurement the device was placed 10 minutes under the microscope light and 5 minutes in the dark. The bias conditions used for the recovery phase were:

- $V_{GS,recovery}$= 0 V, $V_{DS,recovery}$ = 0 V
- $V_{GS,recovery}$= -1.5 V, $V_{DS,recovery}$ = 0 V
- $V_{GS,recovery}$= -1.5 V, $V_{DS,recovery}$ = 1 V
- $V_{GS,recovery}$= -1.5 V, $V_{DS,recovery}$ = 5 V

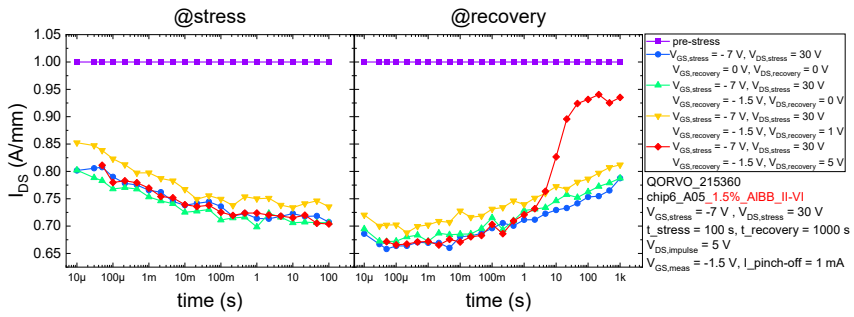


Figura 5.34 Vth transient: device 1.5% Al_BB II-VI; OFF state stress condition at VGS = -7 V, VDS = 30 V; semi-ON variable recovery conditions.

As can be noted with the ($V_{GS,recovery}$= -1.5 V , $V_{DS,recovery}$ = 5 V) recovery bias condition, a left shift is achieved and this confirms the presence of hot electrons: in fact the detrapping process is accelerated during semi-ON state, meaning that when the channel is almost formed, the influence of hot electrons is enhanced.

Chapter 6: Conclusions

During the thesis activity, different HEMTs have been analyzed, to investigate the influence of different epitaxial structure strategies on the reliability issues. More in detail, it was investigated the influence of: (i) difference substrate producer, (ii) the presence of a back-barrier, and (iii) different concentrations of Al in the back-barrier. At first a preliminary DC characterization was performed to extract the devices' main parameters. Then Double Pulse measurements were performed in order to study the presence of trapping mechanisms, estimate their location, and compare the stability performance of the different technologies. Subsequently, DC go and back measurements were conducted to investigate how the trapping (and the kink) influence the devices characteristics. In the end, Vth transient measurements were performed to investigate the nature of the traps and identified them.

a. DC analysis

- CREE vs II-VI: from the statics of the DC measurements, it emerged that in comparison to devices grown on II-VI substrates, those developed on CREE substrates exhibited a discernibly reduced two-terminal gate-leakage current ($I_{GS,leak}$), while their drain leakage current ($I_{D,leak}$). values remained comparable. Regarding $g_{m,peak}$, the V_{th} and the modulus of DIBL, CREE devices displayed smaller average values. This led to the revelation that devices grown on the CREE substrate exhibited a lesser reliance on short-channel effects, as indicated by their diminished DIBL. Although the subthreshold slope (SS) and the saturation current (I_{DSS}) registered slightly higher values for devices originating from the CREE substrate, (slower turn-on times and heightened saturation current) the differences were not significant enough to denote a substantial distinction. ON resistance (R_{ON}), on the other hand, appeared to be somewhat smaller

in this context. However, the distinctions between the two substrates, while present, did not manifest in such a pronounced manner as to imply a definitive dissimilarity. The only parameter that exhibited a notable divergence was the two-terminal gate-leakage current, which appeared noticeably smaller for devices associated with the CREE substrate.

- CONTROL vs Back-Barrier: the analysis revealed that the inclusion of the back-barrier introduces a notable reduction in potential leakage pathways within the architecture. Notably, for both substrates $I_{GS,leak}$, $I_{DS,leak}$ and I_{DSS} diminished in the devices featuring the back-barrier, in contrast to the reference devices (CONTROL) that lacked this additional layer. However, an interesting disparity stood in the behaviour of $g_{m,peak}$ depending on the substrate. For devices grown on CREE substrate, there appeared to be a decline, while conversely, for those on II-VI substrate, they exhibited an increase. This suggests that probably distinct mechanisms of trapping within this region might exert influence upon the divergent populations of devices rooted in the two different substrates. Finally, for the devices with a back-barrier, the presence of kink was registered in the $I_D V_D$ characteristics.

- Increasing concentration of aluminum in the Back-Barrier: it was evident that with the enhancement of aluminum concentration within the back-barrier layer, a sequence of effects unfolded for both substrates. Notably, the threshold voltage became more negative, consequently leading to an increase in the modulus of DIBL and subsequently causing a tendency for the ON-resistance to increase as well. Furthermore, in the presence of a back-barrier within the device architecture, the subthreshold slope demonstrated a propensity to escalate. This indicates a reduced capacity of the device to transition swiftly between on and off states. Prolonged transients are required to pass from one state to the other.
-

b. Double pulse analysis

The main results obtained during the double pulse characterization are the following:

- CREE vs II-VI: for both substrates, memory effect between the measurements was present and it was possible to eliminate it by illuminating the devices for 10 minutes and then waiting 5 minutes under dark conditions. The main parameters observed during the analysis were the variation of threshold voltage and the current collapse. For each of them a monotonic trend was observed for both substrates, showcasing an increasing variation as the stress condition were enhanced. However, no particular differences were found between the two substrates.

- CONTROL vs Back-Barrier: in the analysis it was observed a larger variation exhibited by the devices without a back-barrier in both considering current collapse and threshold voltage variation. However, with the incorporation of the back-barrier, this alteration in threshold voltage and current collapse experienced a reduction. This confirms the notion that the introduction of a back-barrier contributes to enhance the confinement of carriers within the channel. This, in turn, aids in mitigating the dispersion phenomenon within the devices.

- Increasing concentration of aluminum in back-barrier: for threshold voltage variation no particular trend in dependence on aluminum concentration in the back-barrier was found. The trend observed for current collapse, were the following, (going from the device with most dispersion to that with the lowest level of dispersion encountered):

  -CREE: CONTROL → 1.5% Al_BB → 0.5% Al_BB → 1% Al_BB

  -II-VI: CONTROL → 1% Al_BB → 1.5% Al_BB → 0.5% Al_BB

This result led to the following hypothesis: back barrier limits leakage paths and reduces dispersion, but higher aluminum concentrations might enhance trapping due to the increasing presence of surface defects that are generated by the increasing lattice mismatch.

c. DC go and back

The aim of the DC go and back measurements was to determine how the trapping influenced the device characteristics. To do this, stressful conditions were applied to the devices and measured both with increasing (go measurement) and with decreasing (back measurement) voltage. The main results obtained are reported below:

- For all the devices, there is a remarkable distinction between the forward and reverse measurements: The transconductance peak was elevated during the forward phase and reduced during the reverse phase. This discrepancy implies the activation of detrapping-related events during forward measurement (kink).
- Additionally, an asymmetry was observed between CREE and II-VI: as stress increased, the curves shifted leftward for CREE, while they shifted rightward for II-VI. This confirms what suggested from the DC analysis so that different trapping mechanisms affect the two wafers.
- In the end, neither the substrate type nor the concentration of aluminum had shown particular variations in the results obtained

d. Vth transient

The main results obtained are the following:

- During Vth transients in OFF-state stress, the same trend obtained with double pulse measurement was found (going from the device with most dispersion to that with the lowest level of dispersion encountered):

-CREE: CONTROL →1.5% Al_BB → 0.5% Al_BB → 1% Al_BB

-II-VI: CONTROL →1% Al_BB → 1.5% Al_BB → 0.5% Al_BB

This enforced the previous hypothesis.

- Due to the increasing temperature, the transients of the II-VI device without a back-barrier (Control) in the off state were thermally activated. By comparison of the time constants in the Arrhenius plot, Iron (Fe) and carbon (C) doping where found as the main origin of traps in the device. This was confirmed by the device supplier.
- Due to variable recovery conditions, the transients of the 1.5% back barrier II-VI device shifted leftward as soon as a semi-ON bias was applied during the recovery phase. This suggested that the introduction of higher concentrations of aluminium in the device may led to an increment of interface trap state. Then by applying a semi-on bias during the recovery phase, the recovery was accelerated. It was assumed that the hot-electrons impact ionized the surface state traps helping in freeing the charge. Nevertheless, further experiments are required in order to prove this hypothesis.

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