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MASTER'S DEGREE IN ELECTRONIC ENGINEERING

BIDIRECTIONAL HALF-DUPLEX NEAR FIELD DATA COMMUNICATION SYSTEM FOR BIOMEDICAL IMPLANTABLE DEVICES

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Abstract

This work aims at designing a bidirectional half-duplex near field data communication system for biomedical implantable devices (IMDs) in the category of retinal prostheses, starting from the system realized in [19].

The purpose of IMDs is to substitute sensory or motor functionalities that have been lost due to an injury or a disease and, therefore, they require reliable transfer of a large volume of data either from external artificial sensors to the implant or in the opposite direction.

The system's architecture is based on LSK (load-shift keying) modulated inductively coupled resonators and it is strongly biased towards downlink transmission, from the external unit to the implant. Moreover it is designed to work at a carrier frequency allocated inside the ISM radio band, preferably at $f_0 = 13.56\,\mathrm{MHz}$.

The implementation and simulation of the designed system, carried out with the aid of *Cadence Virtuoso* software, displays the limitations introduced by load-shift keying techniques in applications which require high data rate. Indeed, while LSK proves to be a reasonable choice for uplink transmission, minimizing power consumption in a direction of transmission for which data rate requirements are not that stringent, it becomes rapidly disadvantageous for downlink communication, since it evidently struggles to achieve the challenging data rate specification of $5\,\mathrm{Mb/s}$.

This result suggests that exploring alternative modulation techniques, at least for downlink transmission, may lead to enhancing the performance of the system in terms of data rate requirements.

Sommario

Lo scopo di questa tesi è la progettazione di un sistema di trasmissione di dati in tecnologia bidirezionale alternata da utilizzare per impianti biomedicali ed in particolare per l'implementazione di una retina artificiale.

I dispositivi medicali impiantabili hanno la finalità di sostituire funzioni motorie e sensoriali danneggiate a causa di infortuni o malattie e, di conseguenza, necessitano di elevata affidabilità nel trasferimento di grandi volumi di dati da sensori esterni all'impianto e nella direzione opposta.

L'architettura del sistema, progettato partendo dai risultati riportati in [19], è basata su una coppia di risonatori ad accoppiamento induttivo. La trasmissione dei dati è realizzata tramite modulazione di impedenza in tecnologia load-shift keying (LSK) ed è fortemente sbilanciata verso il downlink, ovvero la comunicazione dall'unità esterna all'impianto. Inoltre, il sistema è progettato per funzionare ad una frequenza compresa all'interno della banda ISM, preferibilmente a 13.56 MHz.

L'implementazione del sistema e le successive simulazioni, realizzate tramite l'utilizzo del software *Cadence Virtuoso*, mettono in luce le limitazioni introdotte dalla modulazione di impedenza in applicazioni, come questa, che richiedono un data rate elevato. Infatti, nonostante la modulazione LSK si configuri come una scelta ragionevole nella trasmissione in uplink, in quanto capace di minimizzare il consumo energetico in una direzione in cui le specifiche sul data rate sono alquanto lasche, essa diventa rapidamente svantaggiosa nella comunicazione in downlink, in quanto fatica a raggiungere la specifica stringente di 5 Mb/s.

Questo risultato suggerisce l'idea che approfondire tecniche di modulazione alternative, almeno per quanto riguarda la trasmissione in downlink, possa introdurre miglioramenti nella performance del sistema in termini di velocità di trasmissione dati.

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I extend my heartfelt gratitude to all the friends who shared a moment with me in South Korea. Good times turn into good memories and each one of them made Seoul feel like a second home to me.

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Contents

List of Acronyms

ASK	Amplitude-shift Keying 9, 10
BER	Bit Error Rate 11, 12
BFSK	Binary Frequency-shift Keying 9
BIBO	Bounded-input Bounded-output 27
BPSK	Binary Phase-shift Keying 10
CAGR	Compound Annual Growth Rate 1
FSK	Frequency-shift Keying 9, 10
IBC	Intra-body Communication 6
IMD	Implantable Medical Device 12, 13
IoT	Internet Of Things 14
ISI	Intersymbol Interference 11, 12
ISM	Industrial, Scientifical And Medical 3, 25, 58, 69
LFO	Low-frequency Oscillator 26
LSK	Load-shift Keying 10, 11, 18, 22, 25, 38, 46, 51, 64, 69, 70
NFC	Near Field Communication 5, 13, 14, 15
OOK	On-off Keying 9
PDM	Pulse Delay Modulation 12, 13, 71
PHM	Pulse Harmonic Modulation 11, 12, 71
PSK	Phase-shift Keying 10
PTE	Power Transfer Efficiency 11, 12
RF	Radio Frequency 16, 26

RFID Radio Frequency Identification 5, 13, 14, 15
RHP Right Half Plane 27, 29, 31

SIR Signal-to-interference Ratio 12

WPT Wireless Power Transfer 5, 13, 16

List of Figures

List of Tables

Chapter 1

Introduction

This introductory chapter details the motivations for this work, dwelling on a general explanation of the field of application considered for the designed system. The focus is then shifted to the actual system to be designed, the objectives to be pursued are listed and the required specifications discussed. Finally, the structure of the document is introduced.

1.1 Motivation

The first record of implantation of a medical device in the human body dates back to 1958 at the Karolinska Institute in Solna, Sweden, with the first fully implantable pacemaker, designed by Rune Elmqvist and Åke Senning.

Since then, the development of the industry of implantable medical devices has been continuously proceeding at a considerably fast rate. Several factors foster the need to further expand this industry, such as the coming of the so-called super-aged society[1] and the rising incidence of cardiovascular and neurological illnesses. [7]

Indeed, according to a 2018 Transparency Market Research's[2] report, the global implantable medical devices market, which was valued at US$ 37,700.8 Mn in 2018, is anticipated to expand at a compound annual growth rate (CAGR) of 4.6% from 2019 to 2027.

This recent and on-going proliferation of implantable medical devices, such as cochlear implants, neuro, and visual prostheses is pushing the technological research towards efficient and power saving solutions for short-range wireless data communication. A technology that has proved to be suitable to meet these requirements is inductive coupling, which is, indeed, useful to realize a reliable transfer of data between two devices placed in proximity.

[1] According to the United Nations, the term *super-aged society* refers to a society where more than 20% of the total population is aged 65 years and older.

[2] https://www.transparencymarketresearch.com/

The benefits introduced by inductively-based data links are particularly attractive, not only for biomedical implants, but also for other emerging technologies, such as contact-less payments and domotics applications. Nevertheless, implantable devices play, by themselves, a very central role in the demand for technological advance in this field due to their remarkable potential applications in health-care.

The main requirements driving technological research in this field are high reliability, longevity of the device and efficiency of the transfer of data and, eventually, power. Indeed, many of these links have been used to transmit wireless power to the implanted device in addition to carrying information.

It is, in fact, not feasible to rely on batteries in order to power up the device, since it would unavoidably lead to the deployment of invasive methods, such as surgical remove of the implant, for the process of recharge of the latter.

Unfortunately, the development of implantable medical devices is also facing several challenges and limitations. First and foremost, the main challenge to be faced resides in the limited available physical space, both in terms of volume and shape. Moreover, some limitations that are worth mentioning concern the materials to be deployed, the level of power consumption, bio-compatibility and the realizable functionalities.

Some other factors are also expected to be hindering the expansion of the industry, such as the high cost of the devices and the increased demand for non-invasive treatments.

Taking the aforementioned challenges into account, the design of a bidirectional half-duplex inductive data link for an artificial retina is proposed as the work for this thesis. The idea behind the artificial retina is to restore sight to the blind by transmitting digital images collected by a camera to an implant on the eye, producing artificial vision.

The system to be designed in this work relies on the technology introduced in [19], which serves as an inspiration for the work to be realized, and extends the use of load-shift keying also to the downlink direction of transmission, while adapting the system to the desired use-case. The deployed mechanism of communication leads to a system that is strongly biased towards downlink transmission, from the external device to the implant, with stringent requirements on the data rate to be achieved, which inevitably expose the main limitations of the deployed modulation technique.

1.2 Objectives

As previously introduced, the main objective of this thesis is to design a bidirectional half-duplex near field data communication system for a retinal prosthesis.

The system is designed based on the work reported in [19], deploying

load-shift keying modulation over a pair of inductively coupled resonators driven by an oscillator, that is working at their common resonant frequency.

The following specifications are set for the project.

First and foremost, some stringent constraints on the feasible dimensions of the coils must be respected. More specifically, the diameter of the implanted coil d_2 must be smaller than 15 mm. This constraint can be slightly relaxed on the external device, with a maximum value for the coil diameter d_1 equal to 30 mm.

The range of distance between the coils over which reliable communication is required varies from 30 mm to 50 mm.

Moreover, the system is designed to work inside the industrial, scientifical and medical (ISM) band, preferably at a carrier frequency of 13.56 MHz or, if not feasible, at multiples: 27.12 MHz or 40.68 MHz.

The main objective in the design of the system is to achieve a sufficiently high data rate while maintaining the carrier frequency at the lowest possible value due to the significant electro-magnetic field absorption, which increases at a rate of the carrier frequency squared.

Since the transfer of data occurs mainly from the external device to the implant (downlink), it is required to achieve a larger data rate for this direction of communication. Indeed, reliable transfer of data over a challenging data rate of at least 5 Mb/s is required for the downlink communication.

Conversely, regarding the uplink transmission, from the implant to the external device, a data rate of few kb/s, which is quite easily achieved, is required.

1.3 Thesis Outline

This thesis is divided in 5 chapters and the content is organized as follows.

Following this brief introduction, Chapter 2 presents an overview of the current state-of-the-art on near field data communication systems. More specifically, after generally introducing the characteristics of near field communication, the focus is placed on inductive data links. Their basic functioning is carefully explained, while the main parameters to be kept in mind during the design are defined. The focus is then shifted on the actual transfer of information, with a thorough review of some frequently deployed modulation techniques, supported by practical examples of realization. Last, some other applications beyond medical implantable devices are mentioned.

Chapter 3 gets into the heart of the work by accurately explaining the whole design process for the circuit. First the theory behind RLC resonators is introduced in order to prepare the reader for the actual design of the parallel RLC tanks constituting the link. Then, the LC oscillator is designed, after a brief introduction to the theory behind this category of circuits. The design of the modulating circuit is then completed by the analysis of the

working principles characterizing the LSK modulation and by the design of the switch that is physically realizing the transfer of data. Last, the design process for the envelope detector is briefly discussed.

The results of the simulations performed on the designed circuit are then collected and discussed in Chapter 4. The focus is placed on the flaws exhibited by the circuit, in particular regarding the demanding specifications on data rate. An additional section explores briefly an alternative design approach.

Finally, the work is closed by Chapter 5 which contains a summary of the obtained results and drawn conclusions and discusses some useful suggestions for future work on the matter.

Chapter 2

Theory and State of the Art

This section covers the state-of-the-art on near field data communication systems. The focus is placed in particular on a sub-category of this class of systems, represented by inductive links. The theory behind the operation of inductive links is carefully explained and some frequently deployed modulation techniques are revised, both with their limits and their potentials. Last, a review of some other applications beyond the ones pertaining to the sphere of medical implants is reported, lingering on Near Field Communication (NFC) protocols, Radio Frequency Identification (RFID) technologies and Wireless Power Transfer (WPT).

2.1 Near Field Communication Systems

Over the last few years, the demand for short-range communication technologies has been increasing significantly, with several emerging applications requiring an efficient and reliable transfer of data and power between two or more devices. Among this class of systems, near field technologies based on magnetic and electric coupling have been profiling themselves as competitive strategies for data transmission both in biomedical applications and in general in the world of mobile electronics.

In order to present an exhaustive review of this category of systems, it is useful to start by revising the theory behind near and far field communication.

The electromagnetic field generated around any electromagnetic-radiation source, such as an antenna or scattering object, can be in general divided into two regions, the near field and far field. As the term suggests, the near field dominates in proximity of the electromagnetic-radiation source, while the far field radiation dominates at greater distance from the source.

The amount of distance between the region and the source induces different properties in how the electromagnetic field reacts and propagates in the two regions. In the far field region of the antenna, the radiated power

decreases proportionally to the square of the distance and absorption of radiation does not affect the transmitter. Moreover, inside this region the electric and magnetic fields are strongly intertwined as the propagation of each of the two is associated to a change in the other one.

Conversely, in the near field region, the electric and magnetic fields exist independently of each other and in different sub-regions one of the two can dominate over the other, leading to a sub-division of the near field into magnetic and electric coupling regions. Furthermore, due to proximity, the receiving antenna does affect also the transmitting one, and the radiated power decreases more rapidly with distance with respect to what happens in the far field.

This rapid drop in power ensures that the effects of the near field vanish a few wavelengths away from the radiation source. In between these two regions, a third area can be defined, namely the transition zone, which combines properties of both the near and far fields based on the distance from the source.

The sub-division of the near field into regions where either the magnetic or the electric field dominates over the other leads to the identification of two major categories of near field communication systems, i.e., inductively coupled and capacitively coupled links. [5]

Among the two, inductive links are in general more common and they represent the best choice for biomedical applications, since the magnetic field causes less adverse effects on the human body with respect to the electric one. [15]

It's worth mentioning that several other approaches for short-range data (and power) transmission have been explored in the literature, such as ultrasonic based communication methods [17], optical links [3], intra-body communication (IBC) [20], and so on. Nevertheless, this work focuses on inductive coupling, which proved to be the most suitable strategy for both wireless power and data transmission for implantable medical devices. [12]

2.2 Inductive Links

In order to provide the reader with a complete understanding of the working principle of inductive links, some useful concepts should be briefly introduced. A good starting point is the definition of self and mutual inductances, which are two of the main parameters regulating the operation of inductive links.

The term *inductance* refers to the tendency of an electrical conductor to oppose a change in the electric current flowing through it. The flow of electric current in a conductor generates, indeed, a magnetic field around the conductor itself, whose intensity is proportional to the magnitude of the current and which is varying following the changes of the latter. The afore-

mentioned variation in the magnetic field induces a voltage in the conductor, due to a process called *electromagnetic induction*. This induced voltage, generated by the changing current, has, in fact, the effect of opposing the initial change in current.

Inductance is quantified as the ratio of this induced voltage to the rate of change of the current causing it. More precisely, the quantity describing the effect of a conductor on itself is called self-inductance, while the term mutual inductance describes the effects of the conductor on nearby conductors.

Therefore, assuming a sinusoidal excitation current i at a frequency f, the amplitude of the sinusoidal voltage induced by the current flowing in the conductor on the conductor itself is given by $v = 2\pi fiL$, where L is indeed called *self-inductance*.

If a second conductor is placed in proximity of the first one, a varying voltage $v = 2\pi fiM$ is induced across the second conductor as well and the parameter M accounts, indeed, for the *mutual inductance*.

Thanks to the superposition principle, the total voltage across each of the two conductors is given by the sum of their self-induced and mutually induced voltages.

As it can be noted from the general schematic of an inductively coupled link reported in Fig. 2.1, the core of the inductive link is represented by a pair of mutually coupled inductors, which are basically two coils storing energy in the magnetic field when electric current flows through them.

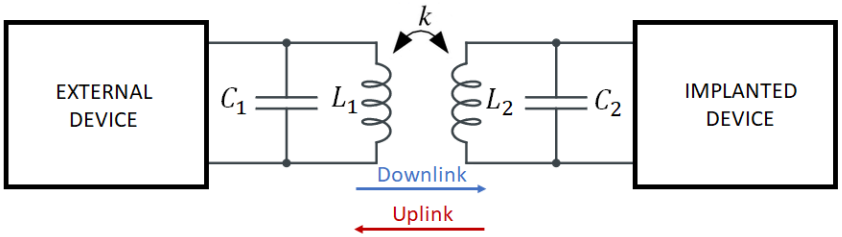


Figure 2.1: Inductive link: general schematic.

From the definitions of self and mutual inductance, it is possible to derive the main parameter modeling the relation between the pair of coils constituting the inductive link, namely the *coupling coefficient*,

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{2.1}$$

with M accounting for the mutual inductance and L_1 and L_2 representing the self-inductances of each of the two coils.

As it can be noted straightforwardly from the definition, given that it's always true that $M^2 \leq L_1 L_2$, the modulus of the coupling coefficient k varies between 0 and 1 and its value expresses the strength of the coupling between

the two coils. When $k = 0$, the current in the first inductor doesn't affect the second one at all. Conversely, when $k = 1$, the first coil affects the second one as much as it affects itself.

The coupling coefficient k is proportional to the geometrical characteristics of the coils, such as their diameter, distance, orientation and alignment.

Starting from the approximated expression reported in [16] and modifying it to obey reciprocity, it is possible to derive the following simple expression for the coupling coefficient:

$$k \approx \left(\frac{d_1 d_2}{4r^2 + d_1^2 + d_2^2} \right)^{3/2} \cos\theta \tag{2.2}$$

where d_1 and d_2 are the diameters of the two coils, r is the distance between the coils and θ accounts for the angle between the planes of the coils.

As reported in [19] this expression, even though an approximation, proves to fit well with measurements. From it, it is then possible to estimate the range of values acquired by the coupling coefficient, which is going to be the starting point for the inductive link design procedure.

2.3 Data Transmission

The main function of the inductive link to be designed in this work is to transmit information. In this work, the flow of data is bidirectional and realized as half-duplex, i.e., transmission occurs from the external device to the implant and backwards, but at two different time instants.

In this biomedical application the major focus is placed on the downlink, i.e., the transfer of data from the external unit to the eye implant, with a stringent constraint on the minimum data rate to be achieved.

Nevertheless, several other applications based on inductive links may require similar data rate in both directions of transmission or, more frequently, they may be biased towards the uplink communication.

In order to transfer data through the inductive link some modulation techniques must be deployed both concerning the uplink and downlink transmissions. In general, two different strategies can be deployed for the two directions of transmission but, in this application, load-shift keying is applied to both.

Before dwelling on the principles behind load impedance modulation, it is useful to spend some words on a more extensive revision of the main modulation techniques available in the literature, introducing both their potentials and limitations.

First and foremost, it's worth noting that all the modulation strategies introduced hereinafter relapse into either one of the two major categories, namely carrier-based and carrier-less modulation techniques. Therefore, two different sections of this chapter are dedicated to the review of some of the

most common examples of carrier-based and carrier-less modulation schemes. Moreover, some practical examples of systems deploying each of these techniques, which were encountered during the review of the state of the art on near field communication systems, are briefly referenced.

2.3.1 Carrier-based Modulation Techniques

Most modulation techniques that have been devised for inductively coupled data links are carrier-based, i.e., they convey information by modifying either the amplitude, frequency, or phase of a sinusoidal carrier signal based on the data to be transferred. The popularity of this category of modulation techniques relies on the ease of their implementation, which is usually based on simple circuitry and consequently allows to satisfy stringent size constraints. Nevertheless, they don't always represent the most appropriate choice, mostly due to the low maximum value of data rate they can achieve, which can be significantly enhanced by deploying some other (carrier-less) modulation schemes.

Amplitude-Shift Keying

The most common form of carrier-based modulation is amplitude-shift keying (ASK). The basic principle behind its functioning is to represent data as variations in the amplitude of the carrier signal, while frequency and phase of the carrier are kept constant.

With this kind of techniques it is possible to achieve a very large index of modulation, in principle up to 100%, since the amplitude of the wave can be switched straightforwardly between its full-scale value and nearly zero.

The simplest realization of this modulation scheme is called on-off keying (OOK). This specific strategy refers to the case in which the modulation index is equal to 100% and the data transmission relies on the use of a carrier wave to indicate a binary one and on its absence to indicate a binary zero.

In the system introduced in article [1] ASK modulation is deployed due to its simple architecture, relatively low power consumption and affordable cost. The designed system can support power and data transfer with data rate approaching 1 Mb/s and modulation index equal to 11.1%.

Frequency-Shift Keying

An alternative approach is to keep the amplitude constant and convey digital information through discrete frequency variations of the carrier signal, implementing what is called frequency-shift keying (FSK). The simplest technique among this class of modulations is binary frequency-shift keying (BFSK), which only uses a pair of discrete frequencies to transmit binary information.

As explained in [2], FSK achieves better noise performance compared to ASK schemes while keeping the design complexity low, but at the price of consuming more power. Nevertheless, in some applications such as the inductive link realized in [2], FSK appears to be a superior choice. In the aforementioned article an inductive link-based wireless power transfer system for biomedical applications is designed, additionally provided with a FSK modulated backward data transmission path achieving reliable communication up to a data rate of 10 kb/s.

Phase-Shift Keying

With phase-shift keying (PSK) data is sent by changing the phase of a constant frequency carrier signal. More precisely, sine and cosine inputs are varied at specific time instants. Similarly to frequency-shift keying, the simplest, and more robust, strategy among this class of techniques is binary phase-shift keying (BPSK), which relies on the use of two different phases separated by 180°.

The attractiveness of PSK (and FSK) modulation schemes is related to their ability to provide an ideally constant power envelope during data transmission and consequently achieve higher power throughput. Nevertheless, their main limitation resides in the limited data rate they can achieve. Article [8] provides an example of a realized inductive link for power and data transfer which can achieve good performances by deploying an enhanced version of PSK modulation.

Load-Shift Keying

In several applications a paramount objective in the realization of the link is to keep the power consumption as low as possible. This is particularly significant in the case of biomedical implantable devices, where an excessive power dissipation could lead to serious damages to the body of the patient.

Under these circumstances, it can be beneficial to rely on a modulation technique called load-shift keying (LSK), which indeed displays simple system's architecture while keeping the level of power consumption minimal. Given that any inductive link is basically a transformer made up of two inductive coils, as it is evident from the schematic in Fig. 2.1, it is possible to exploit on the following property to realize LSK modulation: a change in the secondary load is reflected onto the primary coil as a variation of the equivalent impedance.

Therefore, by switching a resistor at the load, the value of the impedance can be set to different values and this change in impedance can be directly reflected into a variation of the output voltage amplitude.

It is then straightforward to recognize load-shift keying as a special, less power-consuming, form of amplitude-shift keying.

Articles [14] and [19] report two examples of LSK modulated inductive links achieving low power consumption.

2.3.2 Carrier-less Modulation Techniques

The carrier-based methods are particularly attractive because the same low-frequency data carrier can be used also to power the implanted device. However, in high-performance devices that require wider bandwidth a great improvement is obtained by separating the power carrier from the data carrier.

Indeed, aiming for high power transfer efficiency (PTE) and high data transmission bandwidth leads to conflicting requirements. To increase the data rate, a high frequency carrier is required, but to achieve a high PTE the power carrier frequency should be kept low due to the increase of loss at higher frequencies in media such as biological tissues.

As a result the use of two separated carrier signals for power and data has been introduced. A further improvement was made, as reported in articles [6] and [11], by substituting the data carrier with a series of sharp and narrow pulses, in order to reduce even more the power consumption and increase the data rate.

The two techniques introduced in the aforementioned articles are called respectively pulse harmonic and pulse delay modulation and the principles behind their operation, along with some implementation examples, are briefly explained in the following dedicated sections.

Pulse Harmonic Modulation

In article [10] a low-power transceiver for wideband near-field data transmission across inductive telemetry links is designed. Communication in the aforementioned link is achieved through the deployment of a pulse-based data transmission technique called pulse harmonic modulation (PHM), which allows to increase the data rate while lowering the power consumption.

The main goal is, therefore, to suppress the carrier signal thanks to the use of sharp and narrow pulses, reducing significantly the power consumption and transferring data across an inductive link with low self-resonance frequency. The two main parameters to be aware of are the bit error rate (BER) and the intersymbol interference (ISI) which should be kept as low as possible.

The solution introduced in article [6], where PHM is first introduced, is to "utilize a pattern of two or more pulses with specific time delays and amplitudes for transferring each bit". The key harmonic components of the so-called *initiation pulse*, at the beginning of each bit, are modulated on the receiver side by adjusting the delay time (t_d) and amplitude ratio (P) of one or more additional pulses, called *suppression pulses*, which are transmitted within every bit period (T) following the initiation pulse. The obtained signal

is an amplitude modulated oscillation pattern which allows to minimize the ISI across the receiver coil and facilitate robust data demodulation with low BER.

Therefore, in PHM the oscillation pattern is modulated by sending one or more narrow pulses within the same bit period to rapidly suppress oscillation before T. Figure 2.2 shows the basic functioning of PHM, where in every "1" bit only one suppression pulse with the same width (t_{pw}) is used.

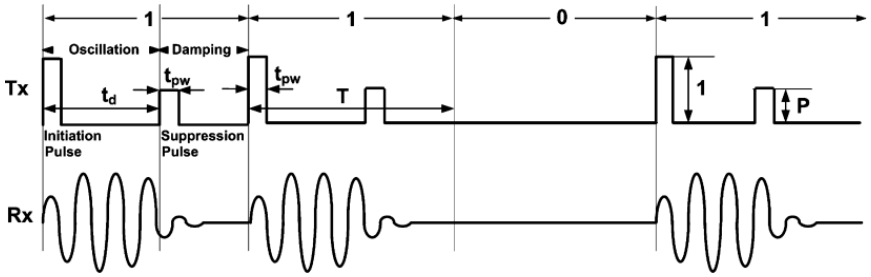


Figure 2.2: PHM conceptual waveforms. [6]

In conclusion, the PHM-based transceiver designed in [10] achieves a high data rate of 20 Mb/s across a 10-mm inductive link, while minimizing the ISI at the receiver input.

Pulse Delay Modulation

Even though PHM allows to achieve overall satisfactory performances both in terms of data rate and power consumption, it is unfortunately not very robust with respect to strong power carrier interference, meaning that it operates properly only when the signal-to-interference ratio (SIR) at the receiver is high enough. Therefore, PHM becomes impractical in all the applications requiring a low-power, wideband, low BER data link that can withstand simultaneous power transmission inside the implantable medical device (IMD). [9]

To overcome this issue, another carrier-less modulation technique, called pulse delay modulation (PDM), is introduced in [11]. The main novelty introduced by PDM with respect to PHM technique is to exploit the undesired power carrier interference on the wireless data link, due to the proximity between power and data coils, to deliver information.

Figure 2.3 shows the operation and key waveforms of PDM for an inductive data and power transmission link where two separate links are used for power ($L_1 - L_2$) and data ($L_3 - L_4$) to keep bandwidth and PTE as large as possible.

As explained in [11], in order to send a bit "1" two narrow pulses spaced by half a power carrier cycle ($\frac{T_p}{2}$) are transmitted. The first pulse is applied after a specific delay t_d chosen as to introduce a shift with respect to the

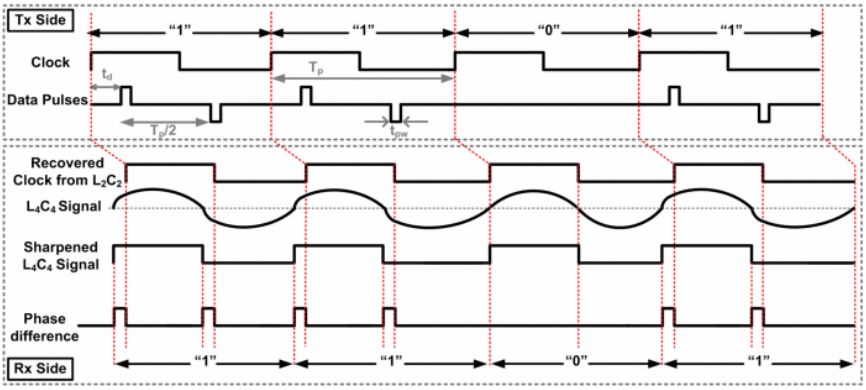


Figure 2.3: PDM conceptual waveforms. [11]

interfering power carrier zero-crossing time. After $\frac{T_p}{2}$ a second pulse with opposite amplitude is applied to introduce a similar time shift.

No pulses are transmitted for a bit "0" and, therefore, any delay between the L_2C_2 and L_4C_4 recovered waveforms can be easily detected as a bit "1".

In [9] a 13.56 MHz PDM-based transceiver for simultaneous power and data transmission was designed, achieving a data rate of 13.56 Mb/s across a 10-mm inductive link, while delivering 42 mW of regulated power to the load.

2.4 Other Applications

Even though the main focus of this work is on near field data communication systems for biomedical implantable devices, it should be noted that IMD's don't represent the only field of application for this category of circuits. Indeed, there are several other emerging applications requiring an efficient and reliable transfer of data, and eventually power, over short distances.

Some of these applications are particularly remarkable, due to their pervasiveness in our daily life. The dramatic development of mobile electronics has indeed introduced the need to deploy various magnetic-based near field technologies such as RFID, NFC and WPT. These technologies are briefly introduced in the following dedicated sections.

2.4.1 Radio Frequency Identification

Radio frequency identification (RFID) leverages on the use of the electromagnetic field to automatically identify and track tags attached to objects from a distance, without requiring them to be in the line of sight.

This key property of RFID represents its main advantage over earlier bar-code technologies, together with its ability to discern multiple different tags located inside the same area without the need for human intervention.

At a first, higher, level RFID devices can be categorized into two classes: active and passive tags. Active devices are in general more expensive and cumbersome due to their need for a power source. An example of active tags is the transponder attached to an aircraft identifying its national origin. [18]

Conversely, passive tags are characterized by considerably smaller size, much longer operational life and they don't require maintenance or batteries. They are made up of an antenna, a semiconductor chip attached to it and encapsulation. The chip coordinates the process of energy capture and transfer from the antenna, while the encapsulation protects both the antenna and the chip from external contamination.

Powering and communication with the tag is carried out by the tag reader and, in most cases, it relies on magnetic coupling between the reader and the tag. In these scenarios data is sent back from the tag to the reader through the deployment of load modulation techniques. The mechanism of near field power and data transfer for RFID tags operating at less than 100 MHz is illustrated in Figure 2.4.

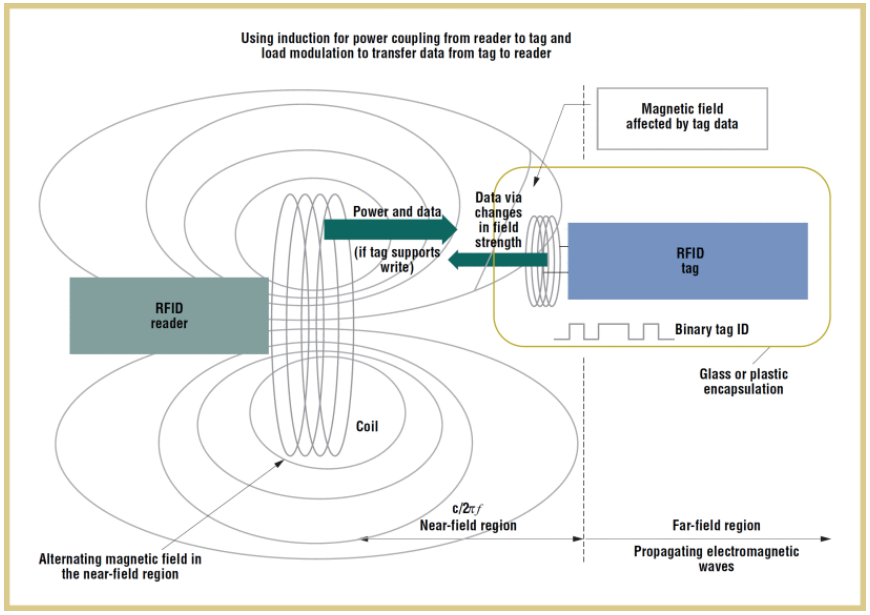


Figure 2.4: Passive RFID tags: near field power and data transfer mechanism. [18]

RFID is becoming more and more widespread due to its applications in traceability, access control and more in general as a key technology in the expanding field of Internet of Things (IoT). Nevertheless, this technology is unable to support peer-to-peer communication, since this standard requires initialization of communication at both ends. This standard of communication is, instead, realized by relying on the use of NFC protocols.

2.4.2 Near Field Communication

NFC is a short-range half-duplex communication protocol relying on inductive coupling to provide data transfer between two close and compatible devices at a working frequency of 13.56 MHz. It was developed in late 2002 by Philips and Sony. [4]

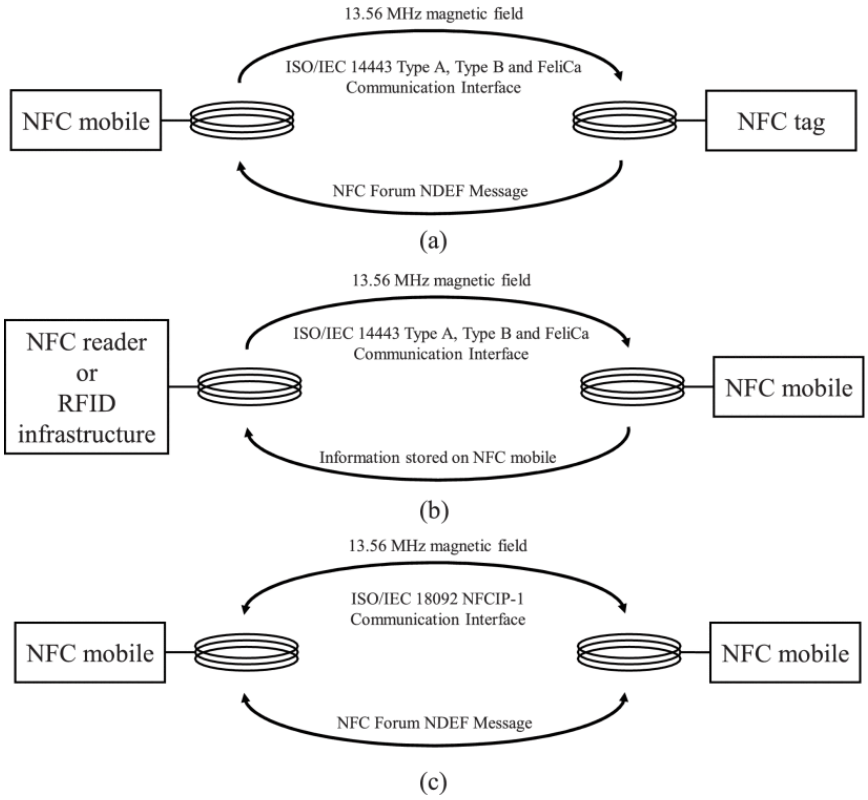


Figure 2.5: NFC operating modes. [12]

As reported in Figure 2.5 NFC technologies include three different operating modes: the reader/writer mode where an active NFC device is able to read and write the data stored in the NFC tag, the card-emulation mode which only allows contact-less reading in a fashion similar to RFID and the peer-to-peer mode which allows exchange of information in both directions. [12]

The peer-to-peer mode of operation is the main novelty introduced by NFC protocols with respect to RFID schemes, where the roles of reader device and readable tag were distinctly defined and non-interchangeable.

The development of NFC technology is contributing to the enhancement in safety, speed and user-friendliness of mobile phones, by integrating daily-use loyalty and credit cards into it and enabling easy communication between nearby devices.

2.4.3 Wireless Power Transfer

Another field of application of inductive links, which is actually closely related to biomedical implants, is represented by wireless power transfer (WPT) technologies.

Indeed, it is not feasible to rely on batteries to power up the implanted devices, due to the risks associated to the process of change or recharge of the battery which would require an invasive surgical remove of the implant. Therefore many of the links that are used to carry data signals are in addition used to transmit wireless power to the implant.

Moreover, wireless charging can introduce several other advantages with respect to traditional charging in a wider range of applications, such as improving user-friendliness by allowing different models of devices to rely on the same charger, achieving smaller dimensions due to the absence of the battery, providing better product durability and implementing more flexible and energy-efficient charging solutions. [13]

It's worth mentioning that inductive links, based on the deliver of electrical energy between two magnetically coupled coils, don't represent the only feasible option to implement efficient and reliable power transfer. Indeed, several wireless charging technologies rely on alternative techniques as illustrated in Figure 2.6.

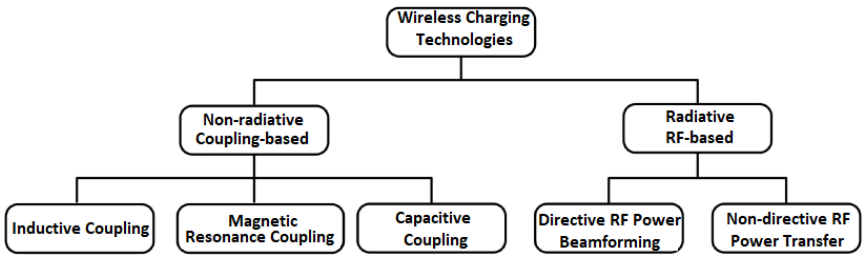


Figure 2.6: WPT technologies classification. [13]

First of all, these technologies can be classified into non-radiative coupling-based charging and radiative RF-based charging. Among the former category, besides inductive coupling, also magnetic resonance coupling, based on evanescent-wave coupling, and capacitive coupling can be found.

The latter category, instead, comprehends directive radio frequency (RF) power beamforming and non-directive RF power transfer.

Thanks to the multiple benefits they introduce and to the several different possible realizations, WPT systems are nowadays among the most widespread technologies not only with the aim of recharging implantable devices but successfully applied to various mobile devices, and deployed to operate small home appliances and to energize electric cars.

Chapter 3

Circuit Design

The system designed in this work is a bidirectional half-duplex near field data communication system for biomedical implantable devices in the category of retinal prostheses.

The idea behind the functioning of the retinal prosthesis is to have an external camera collecting videos and images and sending them directly to the eye of the patient. Therefore, two transceivers must be realized: a first one to be implanted on the eye of the patient, and a second one to be mounted on a special pair of glasses.

Clearly, most of the data exchange happens from the external transceiver towards the implant, in what is referred to as *downlink* direction of communication, but some control signals must also be sent in the opposite, *uplink*, direction.

The block diagram of the link, whose design is based on the system realized in [19], is reported in Figure 3.1.

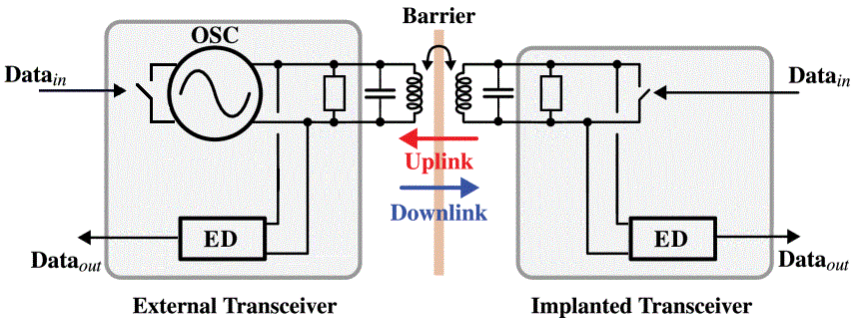


Figure 3.1: Block diagram of the system.

As it is visible from the block diagram, the core of the link is represented by two coupled inductors placed in close proximity. These inductors make part of two parallel RLC resonators, which are tuning an oscillator to their

common resonant frequency.

The left half of the circuit, composed by the oscillator and one of the two resonators, represents the external transceiver while the other resonator accounts for the implanted device.

In order to limit as much as possible the power consumption of the system, data is transmitted through the deployment of load-shift keying.

Both the external and the implanted transceiver include a block realizing the *envelope detector* whose purpose is to demodulate the received data.

In this work the system is designed only with the aim of exchanging data and no power transfer mechanism is realized. Nevertheless, in a practical realization of the link some power supply for the implanted device, alternative to rechargeable batteries, would be essential.

The objectives and specifications for the system, which were introduced in Section 1.2, are summarized in Table 3.1.

Parameter	Value
External coil diameter d_1	30 mm
Implanted coil diameter d_2	15 mm
Coils distance r	[30, 50] mm
Carrier frequency f_0	13.56/27.12/40.68 MHz
Uplink data rate D_{up}	few kb/s
Downlink data rate D_{dn}	$>$ 5 Mb/s

Table 3.1: System specifications.

The design of the subsystems realizing the communication system is carried out in the following sections. In particular, after introducing the basic principles behind the functioning of resonators, Section 3.1 focuses on the design of the two parallel RLC tanks constituting the core of the data link.

Section 3.2 presents an introduction to oscillators and describes the design of the CMOS LC oscillator that is driving the inductive link.

Last, Section 3.3 is dedicated to the practical implementation of the LSK modulation, while Section 3.4 dwells on the design of the circuit used for envelope detection both at the implant and at the external device.

3.1 Resonators

As briefly anticipated in the previous section, the core of the inductive link-based system designed in this work is represented by a pair of mutually coupled inductors. These two inductors are part of two RLC resonators tuning an oscillator to their common resonant frequency.

Consequently, the starting point for the design of the system is the design of the resonators. In the following subsections a general introduction to the

theory behind the functioning of resonators and their purposes is reported, dwelling both on the category deployed in this work, namely parallel RLC tanks, and on its dual, i.e., series RLC tanks. Afterwards, the design procedure followed in this work is discussed and the final sizing of the components of the resonating network is reported.

3.1.1 Introduction to RLC Resonators

An RLC resonator is a circuit made up of a resistor, an inductor and a capacitor connected in series or in parallel. This category of elementary circuits is useful for different purposes, such as the realization of matching networks, i.e., passive networks realizing an impedance transformation, to achieve high frequency gain by cancelling transistor's parasitic elements and to filter signals over a range of frequencies.

The main property of these circuits lies in their ability to resonate at the so-called *resonant frequency* f_0. This resonant frequency is defined as the frequency at which the impedance of the resonator is purely resistive (purely real).

In order to provide the reader with more accurate knowledge on RLC networks, the following sections focus respectively on series and parallel RLC resonators. Moreover, an additional mention of how to trace back other generic RLC networks to one of the two main categories introduced above is reported.

Series RLC Tank

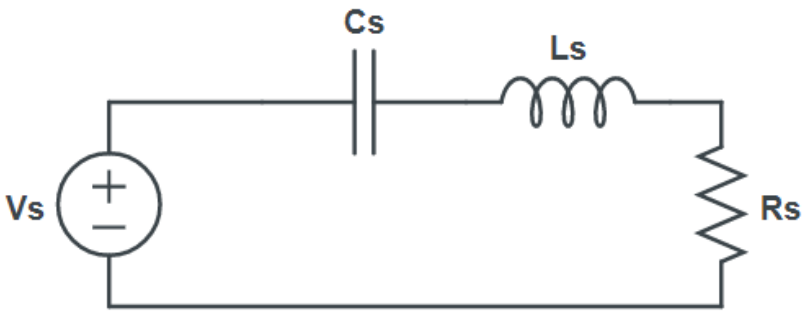


Figure 3.2: Series RLC tank.

This first section deals with series RLC tanks as the one reported in Figure 3.2. First of all, it's useful to retrieve the complex impedance of the tank, which is

$$Z_s = R_s + sL_s + \frac{1}{sC_s} = \frac{1 + sR_sC_s + s^2L_sC_s}{sC_s} \tag{3.1}$$

From the expression of the impedance it is possible to derive the expression of the frequency response of the system, which is given by

$$Z_s(j\omega) = R_s + \frac{j}{\omega C_s}(\omega^2 L_s C_s - 1) \tag{3.2}$$

It is then evident that $|Z_s(j\omega)| \to \infty$ both as $\omega \to 0$ and as $\omega \to \infty$. Therefore, both at very low (DC) and at very large frequencies the resonant network is equivalent to an open circuit.

Moreover, the resonant frequency f_0 can be derived as the frequency at which the inductive and capacitive reactances cancel out and the impedance is purely resistive:

$$|Z_s(j\omega_0)| = R_s \quad \text{at } \omega = \omega_0 = \frac{1}{\sqrt{L_s C_s}} \tag{3.3}$$

A key property of any resonator lies in its ability to store energy. More specifically, a good resonator is able to store a significant amount of energy while dissipating as little power as possible.

A measurement of the quality of the resonator is provided by the *quality factor* Q, which is a dimensionless figure of merit that is only defined at resonance as:

$$Q = \omega \frac{W_t}{P_l} \tag{3.4}$$

where $W_t = \frac{1}{2} L_s I_{pk}^2$ is the total energy stored in the resonator at resonance, while $P_l = \frac{1}{2} R_s I_{pk}^2$ is the average dissipated power.

Therefore, for a series RLC tank $Q = \sqrt{\frac{L_s}{C_s}} \frac{1}{R_s}$, where $\sqrt{\frac{L_s}{C_s}}$ is called the *characteristic impedance* of the resonator.

It's worth noting that, from the definition of $3\,dB$ bandwidth, the following relation can be retrieved:

$$Q = \frac{\omega_0}{\omega_{-3dB}} \tag{3.5}$$

This relation implies that the higher the quality factor Q is, the smaller the bandwidth would be, meaning that a resonator with very high Q is a very frequency selective resonator. This statement is one of the main rules guiding the design of the system realized in this work.

Parallel RLC Tank

The parallel tank reported in Figure 3.3 is the dual circuit of the series RLC resonator. Therefore, the properties of the parallel RLC tank can be retrieved in a very similar fashion.

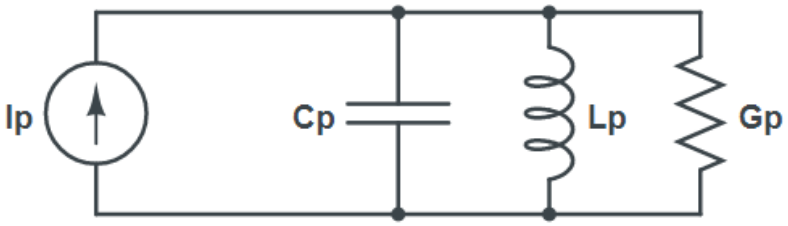


Figure 3.3: Parallel RLC tank.

By duality the admittance of the circuit is given by:

$$Y_p(j\omega) = \frac{1}{R_p} + \frac{j}{\omega L_p}(\omega^2 L_p C_p - 1) \tag{3.6}$$

In this case, both at very low (DC) and very large frequency the resonant network is equivalent to a short circuit. Moreover, the resonant frequency and the quality factor of the RLC parallel tank are given by:

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} \quad \text{and} \quad Q = R_p\sqrt{\frac{C_p}{L_p}} \tag{3.7}$$

Once again, a very high Q leads to a very frequency selective resonator.

Other RLC Resonators

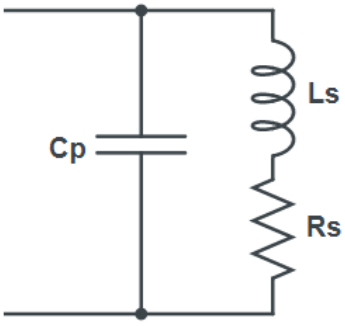


Figure 3.4: Generic RLC tank: example.

In practical situations most resonant networks are neither purely series nor purely parallel tanks, but they may instead present a configuration similar to the one reported in Figure 3.4. It is then paramount to derive a set of formulas allowing to trace back this kind of configurations to one of the two studied in the previous sections. It is useful to start from a general case as the one reported in Figure 3.5.

Figure 3.5: Series to parallel transformation.

By equating the impedances of both networks it is retrieved:

$$R_s + jX_s = \frac{1}{\frac{1}{R_p} + \frac{1}{jX_p}} \tag{3.8}$$

It is then useful to define the *impedance transformation factor* M as $M(\omega) = \frac{X_s}{R_s} = \frac{R_p}{X_p}$ and, by separating the real and imaginary components in Equation 3.8, the following formulas for series-to-parallel transformation are obtained:

$$\begin{aligned} R_p &= R_s(1 + M^2(\omega)) \\ X_p &= X_s(1 + M^{-2}(\omega)) \end{aligned} \tag{3.9}$$

The parallel-to-series transformation, instead, is achieved by simply inverting the above equations. It's worth noting that at resonance, if X_s and X_p are either purely inductive or purely capacitive, the impedance transformation factor $M(\omega_0)$ coincides with the quality factor Q of the resonator.

3.1.2 Resonators Design

Now that the general theory behind RLC resonators has been introduced, the focus can shift on the actual circuit to be designed. In this work, the couple of RLC resonators making up the core of the inductive link are realized as parallel RLC tanks. As introduced in [19], this topology choice allows to achieve better responsiveness of the circuit to changes in the load, meaning that a better LSK modulation can be obtained. Moreover, "a parallel resonator straightforwardly tunes a differential LC oscillator" [19], which is one of the main components of the designed circuit.

Once the topology for the resonators is chosen, the first step is to accurately size the components, i.e., inductors, capacitors and resistors. The

starting point is represented by the inductors, which coincide indeed with the core element realizing the inductive link.

The sizing of the inductors is carried out starting from the specifications on the maximum diameter of the coils. An online inductance calculator [1] is deployed to retrieve an estimate of the maximum feasible values for inductances L_1 and L_2 realizing the link.

This online tool provides both an estimate of the maximum achievable inductance and an estimate of the quality factor of the considered inductor. Since the calculator is not perfectly accurate, some margin is kept on the actual chosen values with respect to the maximum values retrieved.

From the value for the quality factor retrieved from the online calculator it is possible to derive an estimate of the parasitic series resistance of each inductor. Indeed, to each coil is associated some finite resistivity which can be modelled by simulating the behavior of the actual inductor through the series combination of an ideal inductor and of an explicit resistance accounting for this parasitic component.

The parasitic series resistance of the inductor can be estimated from the quality factor as $R_L = \dfrac{2\pi f_0 L}{Q}$, where f_0 is the operative frequency of the circuit.

From Equations 3.7 for the general parallel RLC tank it is then straightforward to retrieve the values for capacitors C_1 and C_2, allowing to have the system resonating at f_0, as $C = \dfrac{1}{L\omega_0^2}$.

One important thing to note is that at the desired frequency of operation ($f_0 = 13.56$ MHz and multiples) the quality factors of the obtained capacitors are significantly larger than the ones of the corresponding (large) inductors. Therefore, throughout the whole design procedure that is following, the capacitors are considered ideal.

The schematic for the couple of parallel RLC resonators realized in *Cadence Virtuoso* is reported in Figure 3.6. In the reported schematic the upper half of the circuit represents the implanted circuit while the lower half accounts for the external device.

[1] https://spok.ca/index.php/resources/tools/102-circularinductorcalc

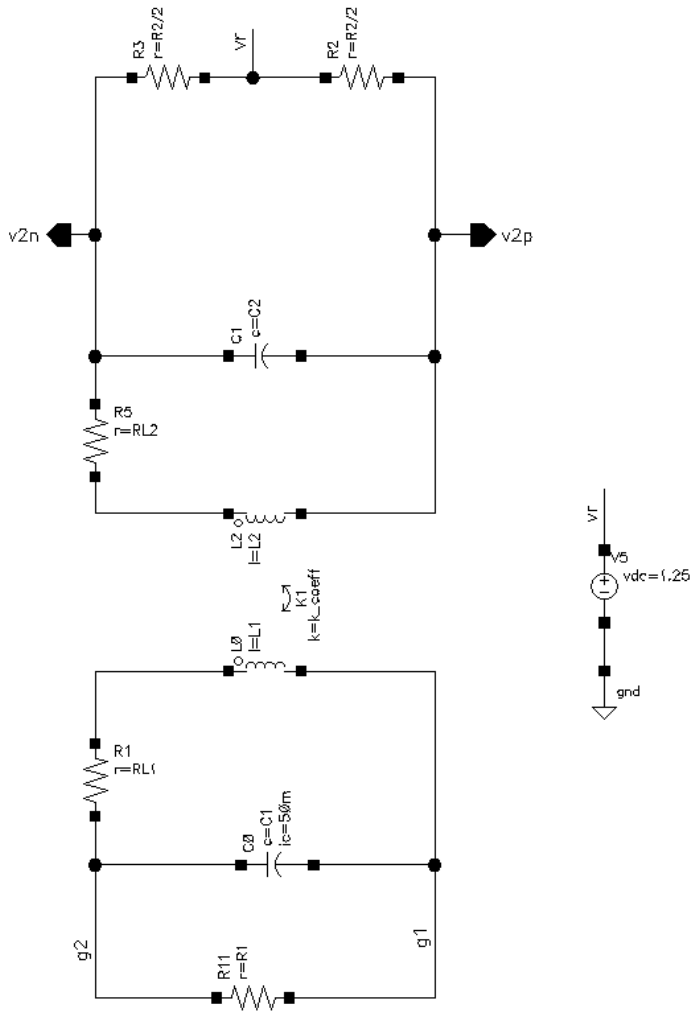


Figure 3.6: Cadence schematic of RLC resonators.

As introduced in Chapter 2, the main parameter that is modeling the interaction between the coils constituting the inductive link is the coupling coefficient k. From the specifications reported in Table 3.1 and considering two coils with maximum diameter lying on the same plane with the same orientation, the coupling coefficient k is found to be comprised between 0.008 and 0.029. It is visible from Figure 3.7, reporting the variations of the coupling coefficient as the distance between the coils varies between 30 and 50 mm, that the coupling is much weaker as the distance between the coils increases.

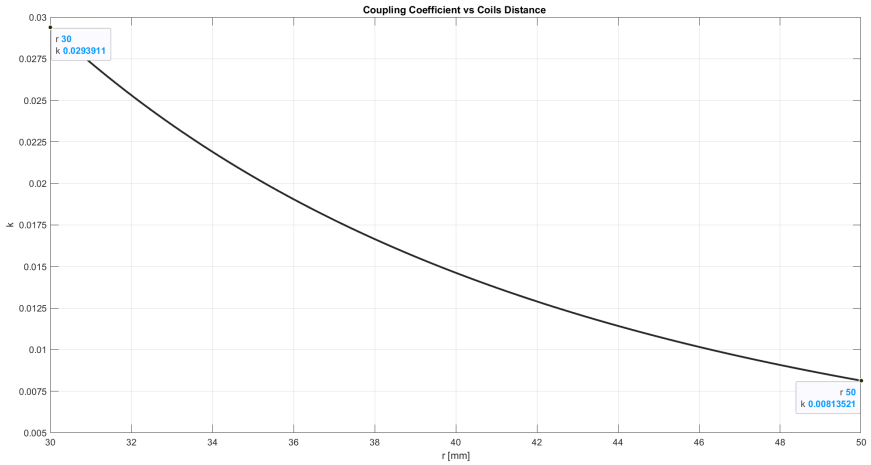


Figure 3.7: Coupling coefficient k as function of distance r between the coils.

The dramatically low values acquired by the coupling coefficient represent a significant issue in the design of the link since, due to the weak coupling, variations in one of the two sides of the circuit reflect very poorly on the other one. This strongly limits the quality of the LSK modulated circuit, since the main idea behind this modulation strategy is to achieve large variations in the output voltage amplitude by setting the load to different values of resistance.

As it is apparent from the schematic of the system the two inductively coupled coils basically form a transformer with ratio $1 : nk$ where k is, indeed, the coupling coefficient, while $n = \sqrt{\frac{L_2}{L_1}}$ represents the so-called *turn ratio*.

A first, simple, choice to make in the design of the system is to consider unitary turn ratio and therefore two coils with the same value of inductance $L_1 = L_2$. In this work, as an alternative approach, also the case of an asymmetric pair of inductors with $n = 3$ is considered.

At a first glance, increasing the value of the turn ratio above one may introduce some advantages in the modulation, since it practically allows to compensate the extremely low values of the coupling coefficient. Nevertheless, this solution proves to be unsuitable for the system, since, along with this reduced benefit, it introduces several disadvantages, such as a significant increase in the value of the supply current.

This is more thoroughly explained in the following chapters, where the LSK modulation is analyzed more carefully.

The calculated values for the main components constituting the links are reported in Table 3.2. The values of the inductors with their parasitic series resistances and of the capacitors needed to resonate the network are calculated at three different working frequencies inside the ISM band: 13.56 MHz, 27.12 MHz and 40.68 MHz.

The inductors are sized in order to respect the constraint on the maximum diameter and to have the self-resonant frequency of each inductor being

at least three times the operating frequency of the circuit.

The sizing of the explicit resistors R_1 and R_2 that complete the RLC resonators is carried out in Section 3.3 since it's strongly related to the load impedance modulation.

Parameter	13.56 MHz	27.12 MHz	40.68 MHz
L_1	1.5 μH	700 nH	400 nH
L_2	1.5 μH	700 nH	400 nH
C_1	91.84 pF	49.2 pF	38.27 pF
C_2	91.84 pF	49.2 pF	38.27 pF
Q_{L1}	200	340	400
Q_{L2}	140	200	240
R_{L_1}	639 mΩ	351 mΩ	256 mΩ
R_{L_2}	913 mΩ	596 mΩ	426 mΩ

Table 3.2: RLC resonators components for n=1.

3.2 Oscillator

The two parallel RLC resonators designed in Section 3.1.2 tune an oscillator to their common resonant frequency. Therefore, the next step in the design of the system is represented by the design of the oscillator.

In the following subsections a brief introduction to electronic oscillators is reported and, subsequently, greater focus is placed on LC differential oscillators, such as the one implemented in this work. The last subsection focuses on the design procedure followed to realize the oscillator together with its bias circuit and displays the final schematic with chosen sizing for each component.

3.2.1 Introduction to Oscillators

An electronic oscillator is an autonomous circuit converting DC power into a periodic signal. Indeed, an oscillator produces as output a periodic, oscillating signal which is often a sine wave, a square wave or a triangle wave.

Electronic oscillators are characterized by the frequency of the output signal. For example, a low-frequency oscillator (LFO) generates a signal at a frequency generally below 20 Hz, an audio oscillator in the audio range (between 16 Hz and 20 kHz) and an RF oscillator in the RF range (between 100 kHz and 100 GHz).

A relevant category of oscillators is represented by the so-called *harmonic oscillators* which produce a sinusoidal output.

An harmonic oscillator can be easily modeled as a feedback system, like the one reported in Figure 3.8.

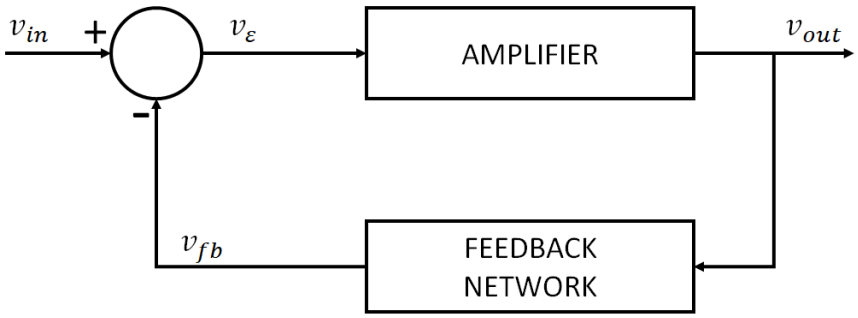


Figure 3.8: Oscillator as a feedback system.

The feedback system reported in Figure 3.8 is characterized by the transfer function

$$H(s) = \frac{v_{out}}{v_{in}} \tag{3.10}$$

In general, an oscillating circuit can be easily realized through the deployment of a BIBO[2] unstable system. Since the necessary (and sufficient) condition for the BIBO stability of a system is to have no poles of the system's transfer function lying on the right half plane (RHP), one condition needed to realize an oscillator is to have some poles lying on the RHP.

For simplicity it can be assumed to start from a simple system with $H(s) = \frac{k}{(s-s_1)(s-s_2)}$. Since an oscillator is a self sustaining circuit, it is able to produce an output without needing any signal at the input. Therefore, it must be assumed $v_{in}(t) = 0$.

Consequently, the output of the system is given by the *natural response* of the system:

$$v_{out}(t) = a_1 e^{s_1 t} + a_2 e^{s_2 t} \tag{3.11}$$

where a_1 and a_2 are two complex numbers depending on the initial conditions of the system.

Assuming s_1 and s_2 to be a pair of complex conjugate poles with positive real part:

$$\begin{aligned} s_1 &= \sigma + j\omega_0' = s_2^* \\ s_2 &= \sigma - j\omega_0' \end{aligned} \tag{3.12}$$

and $a_1 = a_2^*$, the output signal becomes

$$v_{out}(t) = 2|a_1|e^{\sigma t} cos(\omega_0' t + \angle a_1) \tag{3.13}$$

Therefore, the signal that is obtained at the output is an oscillating waveform with amplitude increasing over time, such as the one reported in Figure 3.9.

[2]In control theory a bounded-input bounded-output (BIBO) stable system is a system in which the output is bounded for every input that is bounded.

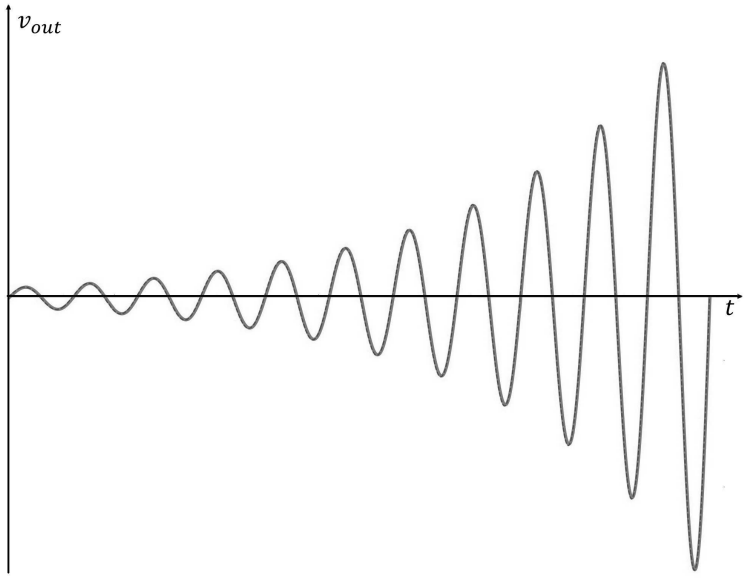


Figure 3.9: Ideal oscillator's output.

This is an accurate representation of the output sinusoid only in the ideal case. In fact, in the case of a real circuit, the non-linearities of the circuit stabilize the amplitude of oscillation which settles to a maximum value $\hat{V}_{LO}$. The corresponding output waveform is reported in Figure 3.10.

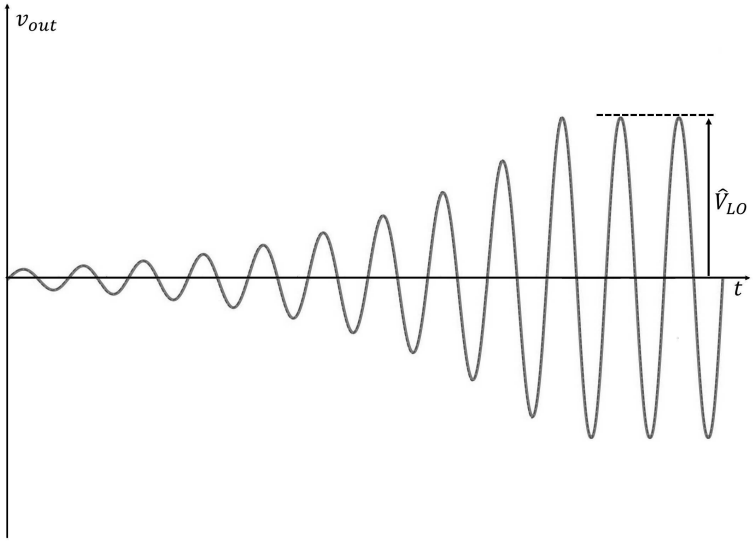


Figure 3.10: Real oscillator's output.

In conclusion, to realize an oscillator a feedback system which is able to generate a natural response with the following characteristics is needed:

- a pair of complex conjugate poles
- poles lying in the RHP ($\sigma > 0$)

One simple, yet effective, example of a circuit realizing an oscillator is the so-called *Colpitts oscillator*. This circuit is made up of a common gate tuned amplifier and a capacitive voltage divider realizing the feedback network. The general schematic of the Colpitts oscillator is reported in Figure 3.11.

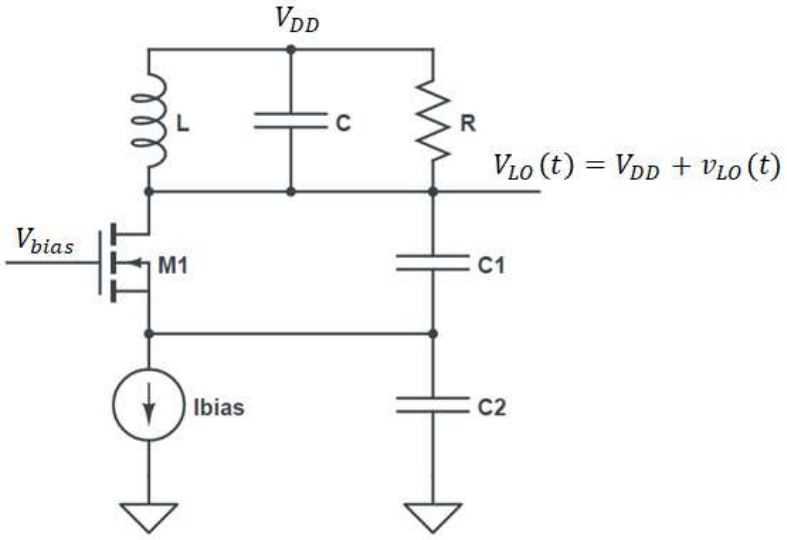


Figure 3.11: General schematic of Colpitts oscillator.

The analysis of the Colpitts oscillator can be easily carried out by treating it as a feedback system and focusing on the loop gain of the system to find the conditions needed for the oscillation start-up.

However, for several other topologies of oscillators it may be difficult to identify the feedback and it is, therefore, needed to carry out the analysis in a different fashion. This is, for example, the case of the LC differential oscillator, which is the topology chosen in this work.

It becomes then essential, before introducing this topology of circuits, to dwell on explaining a different methodology that is particularly suited for the analysis of this category of oscillators. This approach is referred to as the *negative resistance method*.

3.2.2 Negative Resistance Method

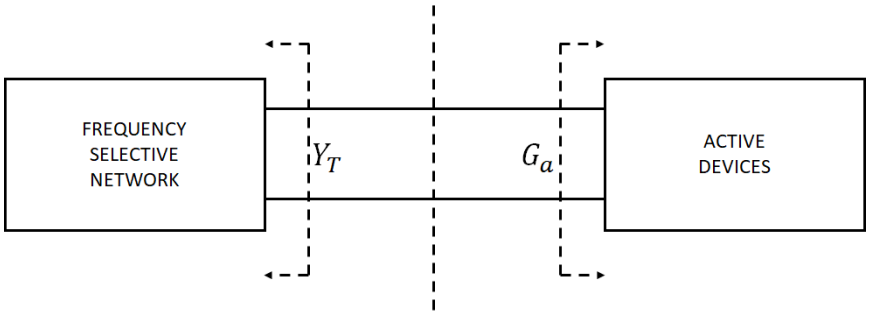


Figure 3.12: Negative resistance method: circuit's partition.

The main idea behind this approach to analyze oscillating circuits is to find an electrical port partitioning the circuit in two distinct parts (as reported in Figure 3.12): the frequency selective network comprising all the reactive components of the circuit and identified by the admittance Y_T and the active devices summarized by the parameter G_a.

First of all, the frequency selective network can be modelled as a resonant tank with overall admittance Y_T. In this case a parallel RLC tank is considered, but the same analysis can be carried out in a very similar fashion for a series RLC tank. This tank includes not only the explicit inductance, conductance and capacitance but also all the parasitic elements coming from the active devices.

On the opposite side, the active devices are modelled by conductance G_a and the voltage across the port is represented by voltage $v_{LO}(t)$, as reported in Figure 3.13.

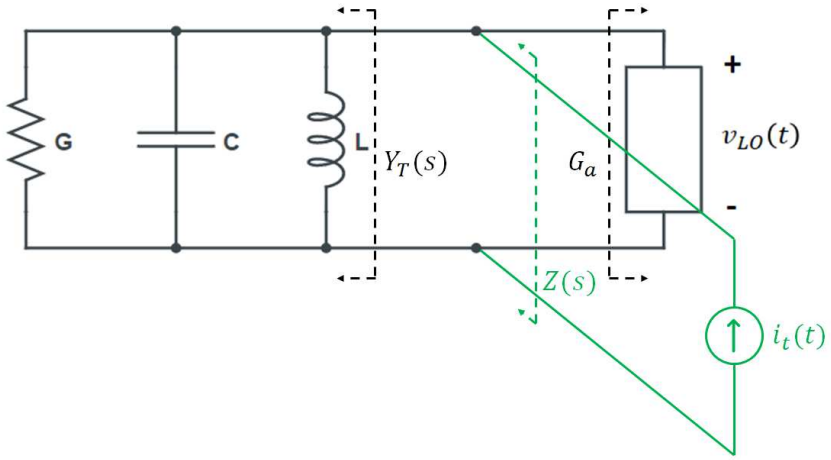


Figure 3.13: Negative resistance method: equivalent circuit.

In order to assess the stability of the circuit and identify the conditions needed for the oscillation start-up the small-signal analysis of the circuit is carried out.

The next step is to compute the small signal impedance $Z(s)$ that is seen by looking into the aforementioned electrical port. This is practically done by injecting a test signal $i_t(t)$ into the port and evaluating the impedance as the ratio between the voltage $v_{LO}(t)$ and the current $i_t(t)$.

Moving to the Laplace domain:

$$V_{LO}(s) = \frac{sL}{1 + sL(G + G_a) + s^2LC} = Z(s)I_t(s) \tag{3.14}$$

In this situation $I_t(s)$ accounts for the input signal while $V_{LO}(s)$ for the output. Therefore $Z(s)$ represents the closed-loop transfer function of the oscillator and in order to assess the stability of the system, the location of the poles of $Z(s)$ must be checked.

Indeed, the system is unstable if and only if the poles of $Z(s)$ lie in the RHP. Therefore, the equation to be solved is:

$$1 + sL(G + G_a) + s^2LC = 0 \tag{3.15}$$

which leads to a pair of complex conjugate poles if the tank's quality factor is large enough.

By imposing the needed condition on the real part of the poles of the system the following start-up condition for oscillation is retrieved:

$$Re\{s_{1,2}\} = -\frac{G + G_a}{2C} > 0 \quad \Leftrightarrow \quad \boxed{G_a < -G} \tag{3.16}$$

Since G accounts for the conductance of the tank, it has to be positive. Therefore, G_a has to be a negative conductance as suggested by the name of the method deployed in the analysis.

Once the start-up condition is verified, the frequency of the oscillation is set to:

$$\boxed{\omega_0 = \frac{1}{\sqrt{LC}}} \tag{3.17}$$

In conclusion, the paramount element needed to realize an oscillating circuit is a negative conductance (or equivalently, resistance) which is easily provided by a cross-coupled differential pair. The cross-coupled pair represents, indeed, the core of the LC differential oscillator, whose functioning is more thoroughly explained in the following section.

3.2.3 LC Differential Oscillator

The general schematic of an LC differential oscillator is reported in Figure 3.14. In this example, the cross-coupled differential pair is realized by two

n-channel MOSFETs but the analysis can be carried out in a similar fashion also in the case of p-channel MOSFETs.

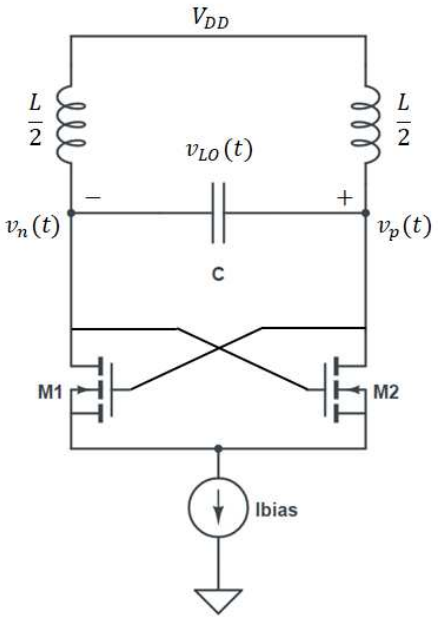


Figure 3.14: LC differential oscillator (nMOS).

First, a small signal equivalent model for the cross-coupled pair can be derived, in order to more easily trace back the system to the schematic reported in Figure 3.12. Figure 3.15 reports the schematic of the cross-coupled pair together with its small signal model.

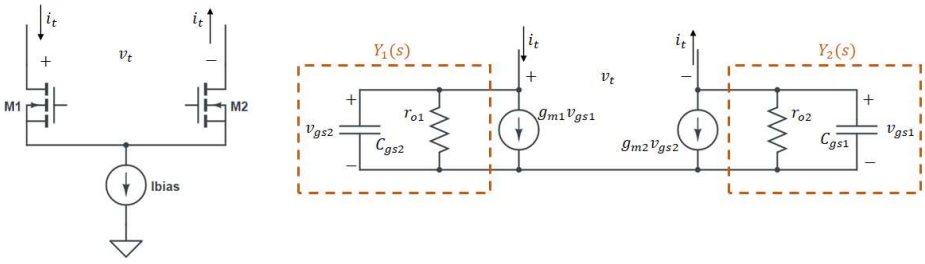


Figure 3.15: nMOS cross-coupled pair: circuit (left) and small signal model (right).

From the circuit the following set of equations can be retrieved:

$$\begin{cases} i_t &= g_{m1}v_{gs1} + Y_1 v_{gs2} = -g_{m2}v_{gs2} - Y_2 v_{gs1} \\ v_t &= v_{gs2} - v_{gs1} \end{cases} \tag{3.18}$$

where

$$Y_1(s) = sC_{gs2} + \frac{1}{r_{o1}} \quad \text{and} \quad Y_2(s) = sC_{gs1} + \frac{1}{r_{o2}}$$

Since M_1 and M_2 form a differential pair, they are identical and biased with the same current:

$$\begin{aligned} g_{m1} &= g_{m2} = g_m \\ Y_1 &= Y_2 = Y \end{aligned} \tag{3.19}$$

Recasting the first equation in 3.18 as

$$(g_{m1} + Y_2)v_{gs1} = -(g_{m2} + Y_1)v_{gs2} \tag{3.20}$$

and exploiting the relations highlighted in 3.19 the following results are retrieved:

$$\begin{cases} v_{gs1} = -v_{gs2} = -\dfrac{v_t}{2} \\ i_t = -\dfrac{g_m}{2}v_t + \dfrac{Y}{2}v_t \end{cases} \tag{3.21}$$

To sum up the overall equivalent admittance is given by

$$\frac{i(t)}{v(t)} = -\frac{g_m}{2} + \frac{Y}{2} = -\frac{gm}{2} + \frac{sC_{gs}}{2} + \frac{1}{2r_o} \tag{3.22}$$

leading to the equivalent circuit reported in Figure 3.16.

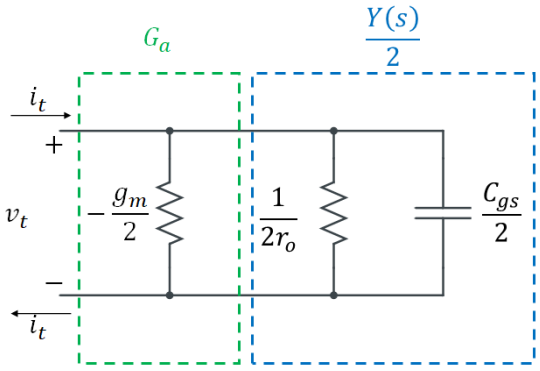


Figure 3.16: Small signal equivalent model for cross-coupled pair.

This result can be leveraged to derive the overall small signal equivalent circuit for the LC differential oscillator of Figure 3.14.

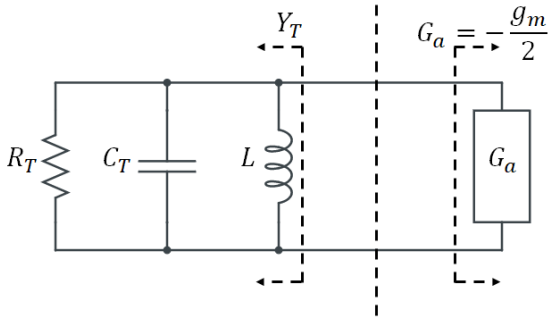


Figure 3.17: LC differential oscillator: small signal model.

In the circuit, which is displayed in Figure 3.17, R_T accounts both for the intrinsic losses of the tank and for the loading effect of the cross-coupled pair, while C_T includes the explicit capacitance C together with the parasitic capacitances of the differential pair:

$$\begin{aligned} G_T &= \frac{1}{R_T} = G + \frac{1}{2r_o} \\ C_T &= C + \frac{C_{gs}}{2} + 2C_{gd} + \frac{C_{db}}{2} \end{aligned} \tag{3.23}$$

As it is evident from the circuit of Figure 3.17, it is appropriate to apply the negative resistance method. Therefore, the condition for the oscillation start-up becomes:

$$G_a < -G_T \quad \Leftrightarrow \quad -\frac{g_m}{2} < -\frac{1}{R_T} \quad \Leftrightarrow \quad \frac{g_m R_T}{2} > 1 \tag{3.24}$$

After the oscillations start at frequency $\omega_0 = \frac{1}{\sqrt{LC_T}}$, the amplitude of oscillation $v_{LO}(t)$ increases exponentially until M_1 and M_2 operate in a condition called *hard-switching*, meaning that at any instant only either M_1 or M_2 is on. Once this condition is achieved, the amplitude of oscillation reaches the steady-state value

$$\hat{V}_{LO} = \frac{2}{\pi} R_T I_{bias} \tag{3.25}$$

3.2.4 Oscillator Design

All the analysis carried out in the previous sections represents a valuable starting point for the design procedure of the oscillator to be realized in this work. The oscillator is realized as an LC differential oscillator using a cross-coupled CMOS pair, as reported in the schematic of Figure 3.18. In this case, the frequency selective network is made up by the resonators and, eventually, the parasitic elements introduced by the MOSFETs constituting the differential pair.

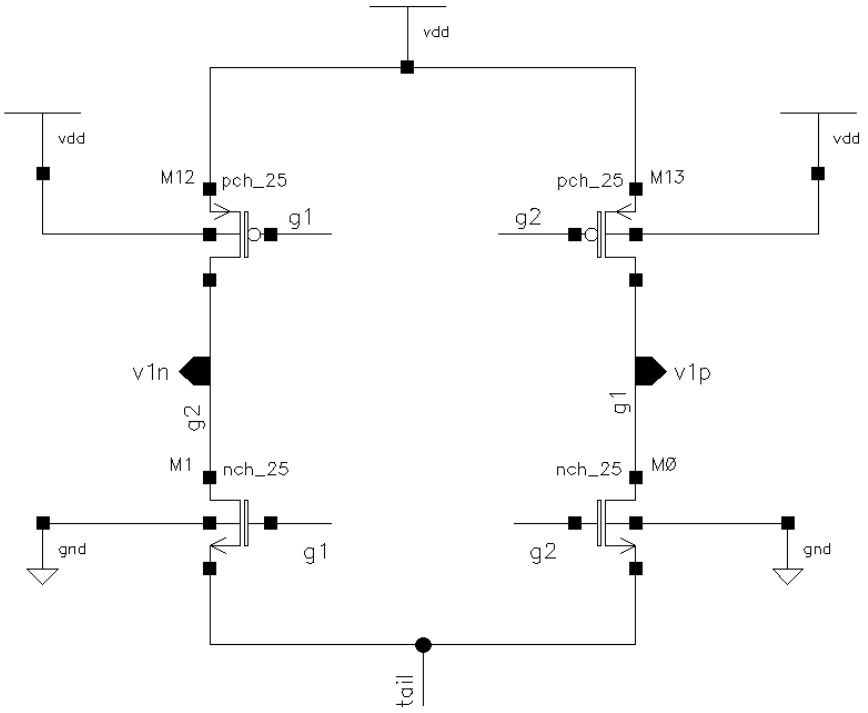


Figure 3.18: Cadence schematic of LC differential oscillator.

In practice, the values chosen for the explicit capacitances C_1 and C_2 (and reported in Table 3.2) for all three different operating frequencies strongly dominate over any parasitic capacitance introduced by the MOSFETs, being in the order of the pF. Therefore, there's no need to take those parasitic components into consideration.

The transistors making up the differential pair are *nch_25* and *pch_25* from the *65nm technology* by TSMC[3] with a nominal I/O voltage of $2.5\,V$.

Since the transistors are supposed to be working in the hard-switching condition in order for the circuit to oscillate properly, they need to be able to sustain the flow of the whole tail current through them. The tail current is varied in between $100\,\mu$A and $500\,\mu$A for the different configurations of the circuit and, therefore, the transistors are sized in order to be able to sustain these values of current, while satisfying the oscillation start-up condition at all three different operating frequencies.

As found in Section 3.2.3 the start-up condition for oscillation is $\frac{g_m R_T}{2} > 1$. However, it's worth noting that for the CMOS configuration of the circuit the transconductance g_m is given by the parallel of the transconductances of

[3]https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_65nm

the nMOS and pMOS, $g_m = g_{mn}||g_{mp}$.

The aimed value for the oscillation at any configuration is chosen to be around $2\,V$ with some margin accepted, as long as it's below the supply voltage of $2.5\,V$ and it is able to provide a good modulation, as it is more appropriately discussed in Section 3.3.

From the aforementioned values for I_{tail} and $\hat{V}_{LO} = 2\,V$, R_T is found from Equation 3.25 to be comprised between a few $k\Omega$ and $35\,k\Omega$[4].

From the start-up condition and keeping some margin to make sure the oscillations actually start, the minimum value for g_m is found to be $g_m \geq 500\,\mu$S, meaning that, choosing the same trasconductance for nMOS and pMOS devices, this has to be at least $g_{mn} = g_{mp} = 1\,$mS.

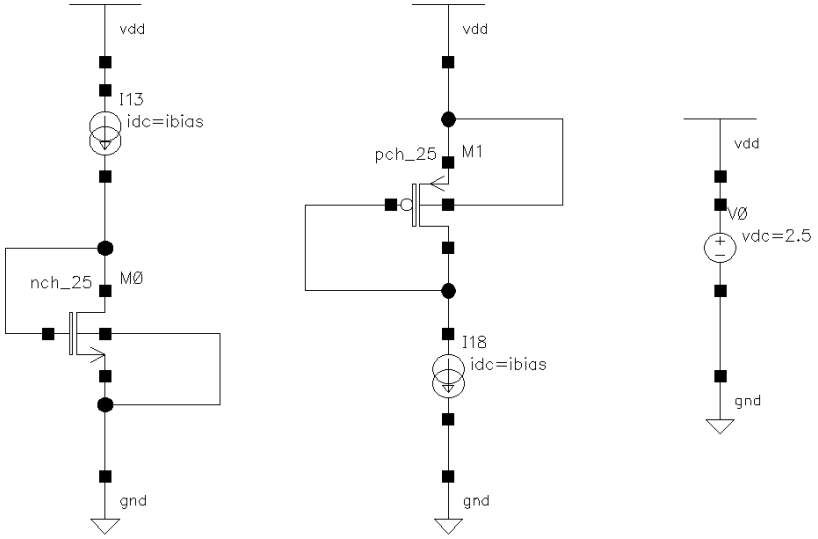


Figure 3.19: Test circuit for MOS sizing.

The sizing for the transistors is then found from simulation, using the circuit reported in Figure 3.19. This circuit performs a parametric simulation (varying the current injected by the current generator) for a nMOS or pMOS transistor of fixed size. Then a plot of the parameter $\frac{g_m}{I_d}$ versus the drain current normalized with respect to the width of the transistor $\frac{I_d}{W}$ is extracted, as in Figure 3.20 for the nMOS. In Figure 3.20 the test transistor has a length $L = 280\,$nm and a width $W = 100\,\mu$m, and the aimed value for g_m is $1\,$mS.

[4]This range for R_T proves to be in accordance with the sizing for the resistances R_1 and R_2 that is reported in Section 3.3 with the aim of achieving a satisfactory impedance modulation.

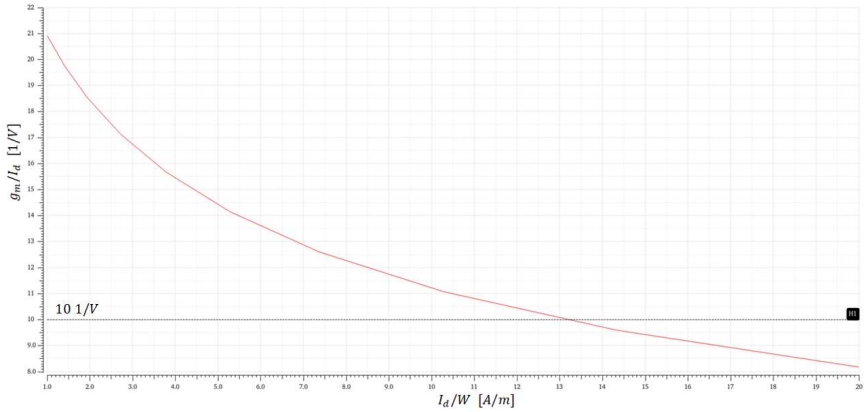


Figure 3.20: nMOS sizing: $\frac{g_m}{I_d}$ vs $\frac{I_d}{W}$.

By choosing the desired value for g_m it is then possible to derive the actual width of the transistor able to sustain the desired drain current. This method provides a good starting point for the sizing of the transistors but, through simulation it is found that it is actually necessary to aim for a larger value in order for the oscillations to start at every working frequency.

In conclusion, in order to satisfy the required constraints, the p-MOSFETs are realized with width $W_p = 110\,\mu$m, while the n-MOSFETs have shorter width $W_n = 40\,\mu$m. Both the p-MOSFETs and n-MOSFETs are realized with length $L = 280\,$nm.

The tail current is provided by the bias circuit reported in Figure 3.21 together with the CMOS LC differential oscillator.

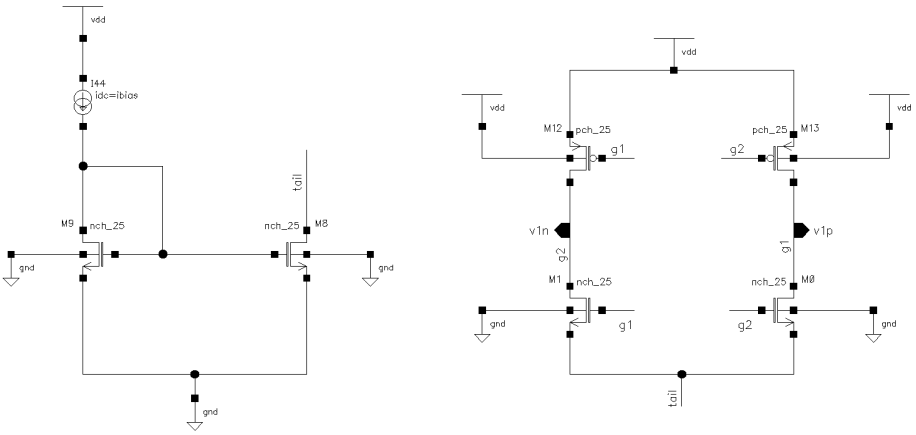


Figure 3.21: Cadence schematic of CMOS oscillator with bias circuit.

The bias circuit is realized as a basic current mirror with ratio 1:1. In order to minimize the mismatches in the bias circuit due to the short-channel

effect, the nch_25 MOSFETs realizing the mirror have double the length of the ones making up the differential pair. Indeed, the nch_25 transistors of the mirror have $W = 100\,\mu$m and $L = 560\,$nm.

3.3 LSK Modulation

Once the basic blocks making up the inductive link are designed, the focus can shift on the actual transfer of information. Communication between the external and the implanted devices, as introduced before, is realized through the deployment of LSK modulation.

This modulation technique is particularly advantageous in the case of biomedical applications, since it reduces the power consumption while displaying simple system's architecture. Indeed, since the application considered in this work is an artificial retina, a modulation technique resulting in an excessive power dissipation could lead to inflicting serious damages to the eye of the patient.

The main principles behind the functioning of LSK modulation were already introduced in Section 2.3.1, but the topic is more thoroughly discussed in the following section, leading to the sizing of the last components making up the link, namely resistors R_1 and R_2, both for the uplink and downlink directions of transmission.

Section 3.3.2 focuses, instead, on the actual design of the CMOS switches realizing the modulation at a practical level.

3.3.1 Working principle

As introduced in Section 2.3.1, the main idea behind LSK modulation is to treat the couple of inductive coils as a transformer and exploit the fact that a change in the secondary load reflects onto the primary coil as a variation of the overall impedance.

Therefore, modulation is realized by setting the value of the load impedance to two different values in order to obtain a consequent variation in the output voltage amplitude. The change in impedance can be produced by simply switching a resistor at the load according to the data flow to be transmitted.

Clearly, the major factor determining the quality of the modulation is represented by the difference between the two values of voltage amplitude obtained at the output. The larger this difference is, the higher the quality of modulation will be.

Since the output voltage is in general proportional to the impedance at the output, it is first needed to derive a set of equations linking the change in the output impedance to the variation introduced mechanically via the deployment of the switch.

In order to do so, it is useful to derive an equivalent model for the couple of resonators both in the case of the uplink and downlink transmissions.

These models are retrieved in the following subsections, which are dedicated to the completion of the design of the link to achieve the actual data transmission in both directions of communication.

Figure 3.22 reports the overall Cadence schematic of the data link comprising the oscillator with its bias circuit and the pair of parallel RLC resonators.

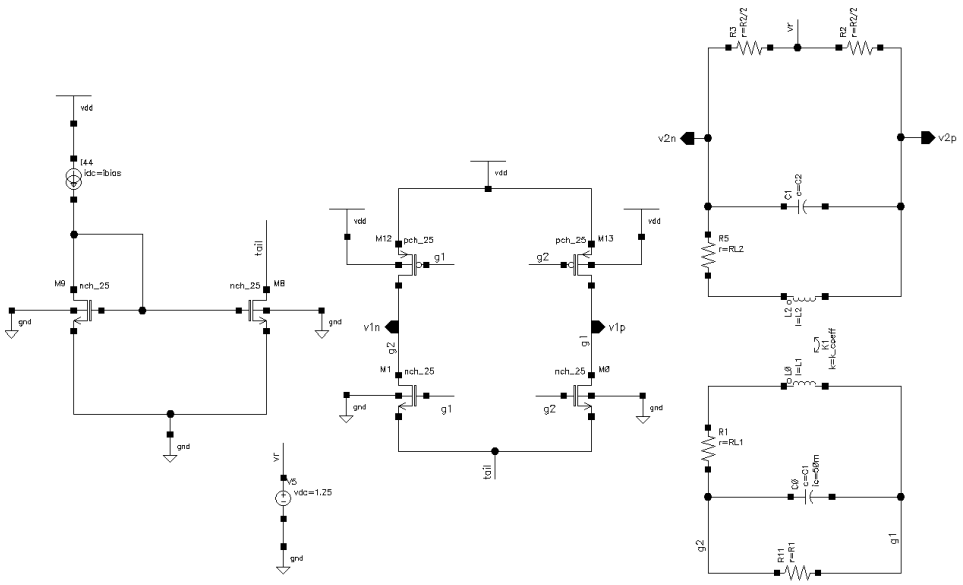
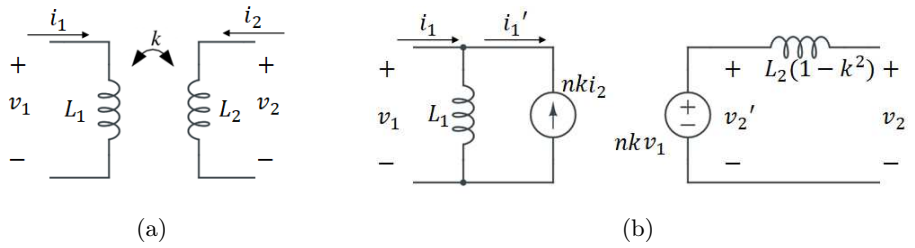


Figure 3.22: Cadence schematic of the data link (resonators, oscillator and bias circuit).

Uplink

The first step in order to retrieve an equivalent model for the pair of RLC resonators is to derive an equivalent circuit for the inductively coupled coils, exploiting once again their similarity to a transformer. Starting from the coupled coils reported on the left of Figure 3.23a, it is possible to derive a set of equations leading to the equivalent circuit of Figure 3.23b.



(a) (b)

Figure 3.23: Coupled coils: equivalent model derivation.

First, the coupled coils can be described as a two-port network ruled by the two following equations in the Laplace domain:

$$\begin{cases} V_1 = sL_1I_1 + sMI_2 \\ V_2 = sMI_1 + sL_2I_2 \end{cases} \tag{3.26}$$

where M is the mutual inductance, while L_1 and L_2 account for the self-inductances of each of the two coils.

From these two equations and exploiting the fact that $M = k\sqrt{L_1L_2}$ the voltage at the secondary can be expressed as:

$$V_2 = k\sqrt{\frac{L_2}{L_1}}V_1 + sL_2(1-k^2)I_2 \tag{3.27}$$

An auxiliary current term can be defined as:

$$I_1' = I_1 - \frac{V_1}{sL_1} = -k\sqrt{\frac{L_2}{L_1}}I_2 \tag{3.28}$$

given that $\dfrac{V_1}{sL_1}$ is the current at the primary when there's no current at the secondary ($I_2 = 0$). In the same situation, from Equation 3.27, the voltage at the secondary is given by $V_2' = k\sqrt{\dfrac{L_2}{L_1}}V_1$.

Remembering that the turn ratio is defined as $n = \sqrt{\frac{L_2}{L_1}}$, from Equations 3.27 and 3.28 the following set of equations can be retrieved:

$$\begin{cases} V_2 = knV_1 + sL_2(1-k^2)I_2 = V_2' + sL_2(1-k^2)I_2 \\ I_2 = -\dfrac{I_1'}{kn} \end{cases} \tag{3.29}$$

Since voltages V_1 and V_2' and currents I_1' and I_2 are related by:

$$\frac{V_2'}{V_1} = nk = -\frac{I_1'}{I_2} \tag{3.30}$$

the core of the equivalent model is an ideal transformer with ratio $1 : nk$ and the equivalent circuit for the coupled coils coincides with the one reported in Figure 3.23b.

Substituting this model to the coils in the couple of RLC resonators, the equivalent circuit of Figure 3.24 is retrieved.

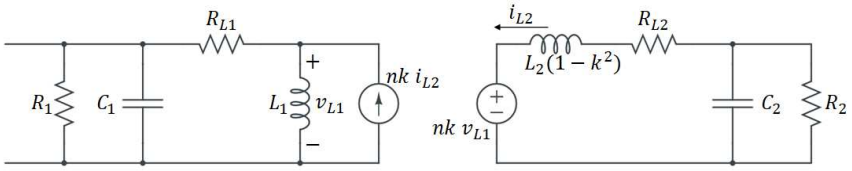


Figure 3.24: First equivalent model for uplink.

From this model and through several manipulations a final, much simpler, equivalent circuit can be obtained. First and foremost, two observations must be made:

1. Given that $k < 0.1$, as derived in Section 3.1.2, the leakage inductance $L_2(1-k^2)$ can be approximated to L_2 with relative error lower than 1%.

2. In series-to-parallel and parallel-to-series impedance transformations the value of the reactive element (L or C) can be considered practically unchanged with very small relative error if the quality factor of the transformation is large enough.

Keeping these observations in mind, it is possible to apply a first parallel-to-series transformation to C_2 and R_2, leading to the circuit of Figure 3.25, where $R_{2s} = \frac{R_2}{1+Q_{C2}^2}$ and $C_{2s} \simeq C_2$, given that $Q_{C2} = \omega_0 R_2 C_2$ is large enough.

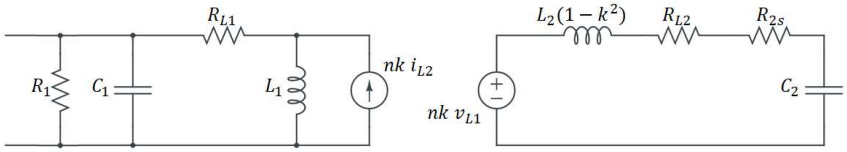


Figure 3.25: Uplink equivalent model derivation: step 1.

Moreover, given that $L_2(1-k^2) \simeq L_2$, $C_{2s} \simeq C_2$ and $\omega_0 = \frac{1}{\sqrt{L_2 C_2}}$, $L_2(1-k^2)$ and C_{2s} are very close to resonance at ω_0 and therefore they cancel out, leading to Figure 3.26.

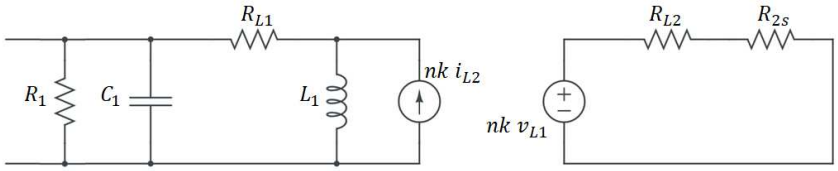


Figure 3.26: Uplink equivalent model derivation: step 2.

The next manipulation on the circuit consists into transferring R_{L2} and R_{2s} to the primary, obtaining the circuit reported in Figure 3.27 where $R_2' = \frac{R_{L2}+R_{2s}}{(nk)^2}$.

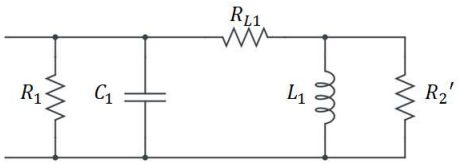


Figure 3.27: Uplink equivalent model derivation: step 3.

Then, a parallel-to-series transformation can be applied to L_1 and R'_2 leading to $R'_{2s} = \frac{R'_2}{(1+Q_{12}^2)}$ and $L_{1s} \simeq L_1$ if $Q_{12} = \frac{R'_2}{\omega_0 L_1}$ is large enough, as displayed in Figure 3.28.

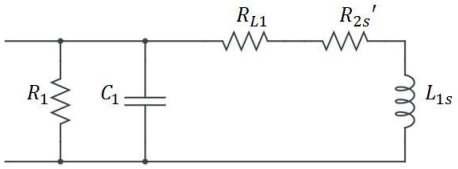


Figure 3.28: Uplink equivalent model derivation: step 4.

Applying a series-to-parallel transformation to L_{1s} and $R_{L1} + R'_{2s}$, the circuit of Figure 3.29 is obtained, where $R''_2 = (R_{L1} + R'_{2s})(1 + Q_{1s}^2)$ and $L_{1p} \simeq L_{1s} \simeq L_1$ as long as $Q_{1s} = \frac{\omega_0 L_{1s}}{R_{L1}+R'_{2s}}$ is large enough.

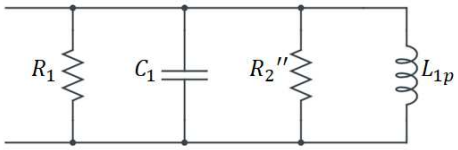


Figure 3.29: Uplink equivalent model derivation: step 5.

Last, given that $L_{1p} \simeq L_{1s} \simeq L_1$ and $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$, L_{1p} and C_1 are very close to resonance at ω_0 and therefore they cancel out, leading to the final equivalent circuit of Figure 3.30.

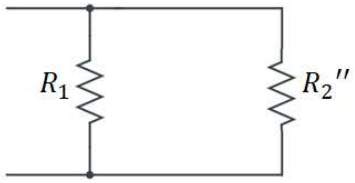


Figure 3.30: Final uplink equivalent model.

In the uplink direction of transmission, from the implant to the external device, the switch is placed at the secondary in parallel to resistor R_2, while the differential output voltage is exactly the voltage read at the primary between the gates of the transistors of the cross-coupled pair.

Since the equivalent resistance seen at the output is $R_{out1} = R_1||R_2''$ as displayed in Figure 3.30 and R_2'' depends on the value of R_2, the presence of the switch at the secondary clearly induces a variation in the value of R_{out1}.

In order to more easily explain this variation, it is useful to define two fictitious resistances $R_{2_{off}}$ and $R_{2_{on}}$ explicitly expressing the changes introduced by the switch. Indeed, while the switch is off the explicit resistance at the secondary is simply $R_{2_{off}} = R_2$, but when the switch is turned on, the ON resistance of the switch lowers the explicit resistance to $R_{2_{on}} = R_2||R_{ON}$.

Therefore, the values of $R_{2_{off}}$ and $R_{2_{on}}$ should be chosen accurately in order to maximize the difference between the corresponding $R_{out_{1off}}$ and $R_{out_{1on}}$ and consequently the modulation index.

It is worth noting that, as introduced above, the quality factors of each transformation should be large enough so that the values of the reactive elements don't change significantly. This choice helps making sure that at $f = f_0$ both the primary and the secondary circuits are very close to resonance.

Nevertheless, a too large value of the quality factors contributes to slowing down the step response of the circuit. This is a significant issue, since the main effect of a large transient and, therefore, of a slow step response is to reduce dramatically the maximum achievable data rate. Therefore, both in uplink and downlink transmission, an appropriate trade-off should be found between a large quality factor not to vary too much the resonant frequency and a small one to speed up the response.

This trade-off leads in the case of the uplink to the sizing reported in Table 3.3. As verified through simulation, this allows to sufficiently reduce the transient while keeping the relative error in frequency with respect to the carrier frequency f_0 below 1%.

More specifically, the value of $R_{2_{off}} = R_2$ is chosen in order to obtain sufficiently (but not overly) large quality factors and an amplitude of oscillation of around $2\,V$, while the value of $R_{2_{on}} = R_2||R_{ON}$ is chosen in order to have a sufficiently large difference between the two amplitude values.

Since $R_{out1} = R_1||R_2''$, if R_1 is chosen to be much larger with respect to the maximum value acquired by R_2'', the latter dominates in the parallel combination maximizing the index of modulation. Moreover, the choice of R_1 is strongly intertwined with the choice of I_{tail} in order to keep the output voltage, which is proportional to both, below the supply voltage $V_{DD} = 2.5\,V$.

Parameter	13.56 MHz	27.12 MHz	40.68 MHz
$R_{2_{off}}$	6390 Ω	5964 Ω	5112 Ω
$R_{2_{on}}$	511 Ω	477 Ω	409 Ω
R_1	50 kΩ	50 kΩ	30 kΩ
I_{tail}	150 μA	100 μA	100 μA

Table 3.3: Uplink: circuit parameters.

Downlink

The analysis of the downlink transmission can be carried out in a similar fashion. More specifically the equivalent model reported in Figure 3.24 can be adapted to the opposite data flow by deriving the dual circuit as reported in Figure 3.31.

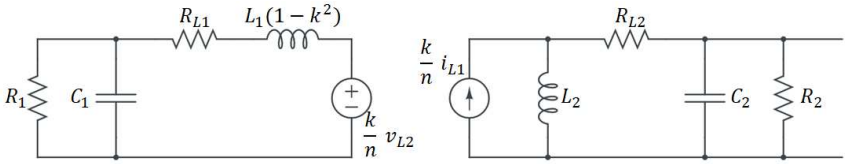


Figure 3.31: First equivalent model for downlink.

Then, a similar set of manipulations can be carried out for this new circuit.

First of all, a parallel-to-series transformation applied to R_1 and C_1 leads to the circuit of Figure 3.32, where $R_{1s} = \frac{R_1}{1+Q_{C1}^2}$ and $C_{1s} \simeq C_1$ if $Q_{C1} = \omega_0 R_1 C_1$ is large enough.

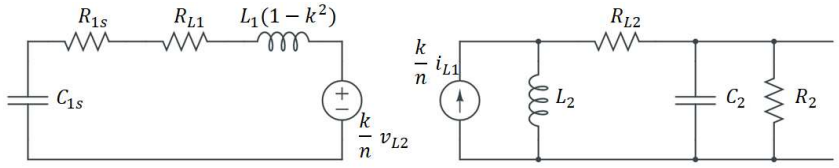


Figure 3.32: Downlink equivalent model derivation: step 1.

Next, given that $L_1(1-k^2) \simeq L_1$, $C_{1s} \simeq C_1$ and $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$, $L_1(1-k^2)$ and C_{1s} are very close to resonance at ω_0 and they cancel out, leading to Figure 3.33.

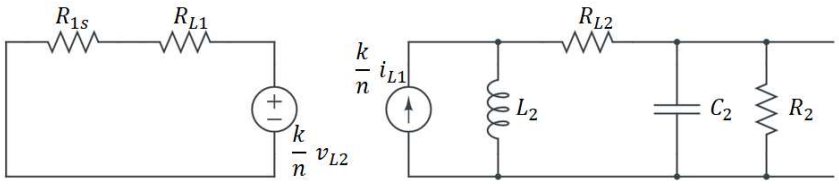


Figure 3.33: Downlink equivalent model derivation: step 2.

The resistances R_{L1} and R_{1s} can then be transferred to the secondary circuit as reported in Figure 3.34 where $R_1' = \frac{(R_{L1}+R_{1s})}{k^2} n^2$.

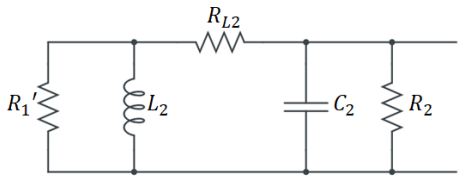


Figure 3.34: Downlink equivalent model derivation: step 3.

Subsequently, it is possible to apply another parallel-to-series transformation, this time on L_2 and R_1', so as to obtain the circuit of Figure 3.35, with $R_{1s}' = \frac{R_1'}{1+Q_{21}^2}$ and $L_{2s} \simeq L_2$ given that $Q_{21} = \frac{R_1'}{\omega_0 L_2}$ is sufficiently large.

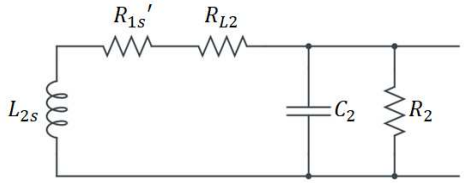


Figure 3.35: Downlink equivalent model derivation: step 4.

A last series-to-parallel transformation can then be applied to L_{2s} and $R_{L2} + R_{1s}'$ leading to $R_1'' = (R_{L2} + R_{1s}')(1 + Q_{2s}^2)$ and $L_{2p} \simeq L_{2s}$ given that $Q_{2s} = \frac{\omega_0 L_{2s}}{R_{L2}+R_{1s'}}$ is large enough, as reported in Figure 3.36.

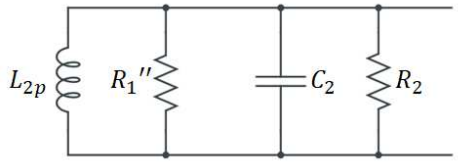


Figure 3.36: Downlink equivalent model derivation: step 5.

Last, the final equivalent circuit reported in Figure 3.37 is obtained by resonating C_2 with $L_{2p} \simeq L_2$ at $\omega_0 = \frac{1}{\sqrt{L_2 C_2}}$.

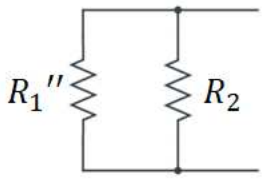


Figure 3.37: Final downlink equivalent model.

In the downlink direction, from the external device to the implanted one, the switch is placed at the primary in parallel to resistor R_1, while the differential output voltage is read at the secondary.

Therefore, the equivalent resistance seen at the output is $R_{out2} = R_2||R_1''$ and the presence of the switch at the primary induces a variation in the value of R_{out2}.

Once again two fictitious resistances $R_{1_{off}}$ and $R_{1_{on}}$ can be defined, explicitly expressing the changes introduced by the switch. While the switch is kept off the explicit resistance at the primary is simply $R_{1_{off}} = R_1$, but when the switch is turned on, the explicit resistance becomes $R_{1_{on}} = R_1||R_{ON}$.

The values of $R_{1_{off}}$ and $R_{1_{on}}$ are then chosen in order to maximize the modulation index.

The observations made for the uplink direction of transmission regarding the quality factors and the speed of the step response of the circuit still hold.

Nevertheless, in this situation, R_2 is not chosen to be much larger than R_1''. This choice relates to the ambitious target data rate that is desired for downlink communication.

Indeed, it is evident from simulation that reducing the value of R_2 doesn't compromise significantly the quality of the modulation while it strongly speeds up the step response of the system, allowing to achieve a larger data rate.

Moreover, in this case, extra care should be used when choosing the value of R_1 and of the tail current I_{tail} in order to make sure that the maximum amplitude of oscillation at the primary is once again around $2\,V$ and doesn't exceed the supply voltage of 2.5 V.

The sizing of the circuit for the downlink direction of transmission is reported in Table 3.4.

3.3.2 CMOS Switch Design

The main physical component regulating the LSK modulation is the switch. At a first approximation and in order to obtain some qualitative results, the

Parameter	13.56 MHz	27.12 MHz	40.68 MHz
$R_{1_{off}}$	6390 Ω	5964 Ω	5112 Ω
$R_{1_{on}}$	511 Ω	477 Ω	409 Ω
R_2	3 kΩ	3 kΩ	3 kΩ
I_{tail}	500 μA	400 μA	500 μA

Table 3.4: Downlink: circuit parameters.

switch behaviour can be easily modeled using the ideal component *switch* taken from the library *analogLib* in *Cadence Virtuoso*.

The required value for the ON resistance can, then, be retrieved respectively from $R_{2_{on}} = R_2||R_{ON}$ for the uplink and $R_{1_{on}} = R_1||R_{ON}$ for the downlink, substituting the values reported in the above tables.

This parameter can then be explicitly inserted into the circuit as a series resistance or specified as the parameter *close switch resistance* in the *switch* component (see Figure 3.38).

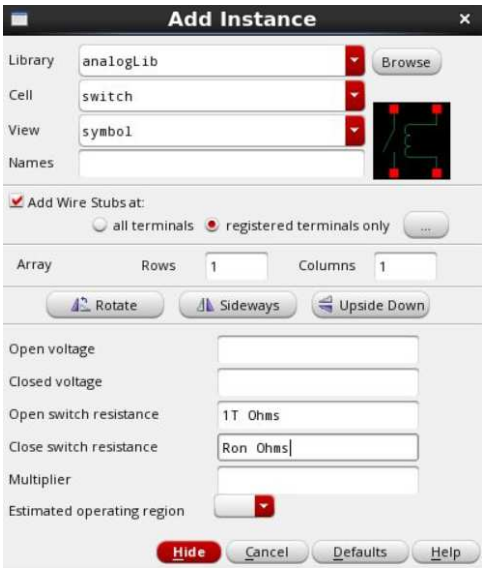


Figure 3.38: AnalogLib switch component: parameter window.

As a second step, the aforementioned model can be substituted by the actual implementation of the switch, realized as a CMOS transmission gate as it is reported in Figure 3.39. The appropriate sizing for the MOSFETs making up the switch, in order to obtain the desired R_{ON}, is retrieved through simulation and reported in Table 3.5[5].

[5]All the MOSFETs making up the switch have length $L = 280\,\text{nm}$.

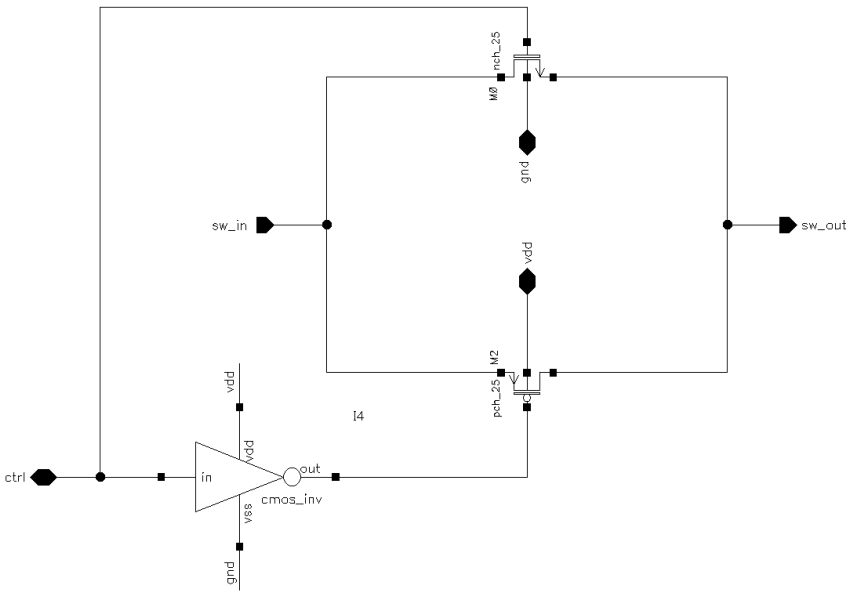


Figure 3.39: Cadence schematic of CMOS switch.

$R_{1/2_{on}}$	511 Ω	477 Ω	409 Ω
R_{ON}	555 Ω	518 Ω	445 Ω
W_n	3 μm	3 μm	3.5 μm
W_p	6 μm	6 μm	7 μm

Table 3.5: CMOS switch sizing.

3.4 Envelope Detector

After the design of the modulating circuit is completed, the last step is to design the circuit for envelope detection and slicing. The schematic of the aforementioned circuit, which is based on the circuit reported in [19], is reported in Figure 3.40.

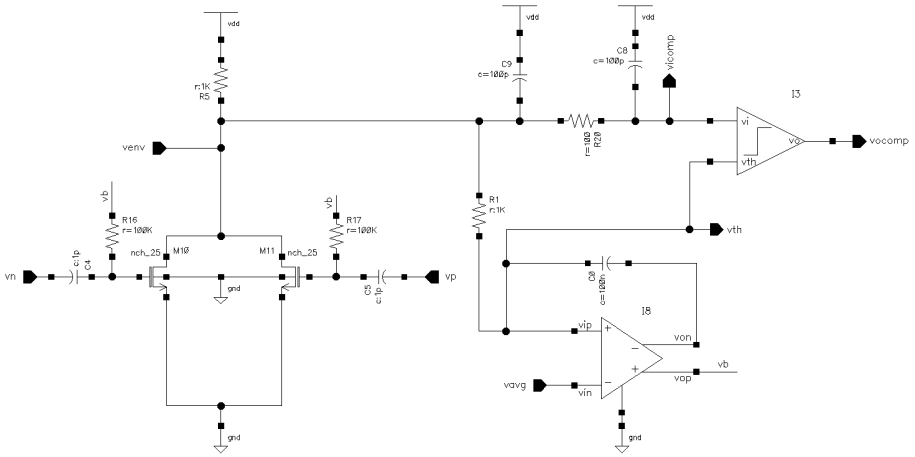


Figure 3.40: Cadence schematic of envelope detector.

The modulated differential voltage is applied to a full-wave rectifier made up by two nch_25 transistors. The rectified output voltage V_{env} is then filtered through a second-order low pass RC section, in order to remove the oscillations at the carrier frequency, and applied to an integrator block that controls the voltage V_B needed to bias the gates of transistors M_{10} and M_{11}.

This configuration forces the mean value of the rectified waveform to the externally supplied voltage V_{avg}. The filtered voltage is then applied to a comparator which slices the modulated envelope against the constant threshold $V_{th} = V_{avg}$, producing the output waveform varying in between zero (binary "0"), when the voltage is lower than the threshold, and the supply voltage (binary "1"), when it overcomes V_{th}.

Chapter 4

Simulations and Results

Once the design of the circuit has been completed, it is possible to start performing simulations. The environment used to perform the simulations is *Cadence Virtuoso ADE Assembler*.

This chapter dwells on the simulation results and on the discussion of the main flaws experienced by the designed system. The first section (4.1) introduces the simulation setup and the deployed test benches. Subsequently, Section 4.2 focuses on the results obtained from the simulations, both for the modulating circuit and for the whole circuit comprising the envelope detector. The section discusses the main weaknesses found in the performance of the circuit, focusing in particular on the maximum achievable data rate and providing some suggestions regarding how to improve it. Last, Section 4.3 introduces the results obtained by simulating a circuit designed following an alternative approach. More specifically, it dwells on the case in which the coils are realized asymmetrically with turn ratio $n = \sqrt{\frac{L_2}{L_1}} = 3$.

4.1 Simulation Setup

The performance of the circuit is analyzed by performing a transient simulation and plotting the differential output voltage as a function of time. Being the designed system a bidirectional half-duplex data link, the success of data transmission must be checked in both directions of communication, i.e. for uplink and downlink.

Therefore, the test bench must be configured differently according to the direction of transmission to be analyzed.

Starting from the uplink, the test bench to be deployed for simulation is reported in Figure 4.1.

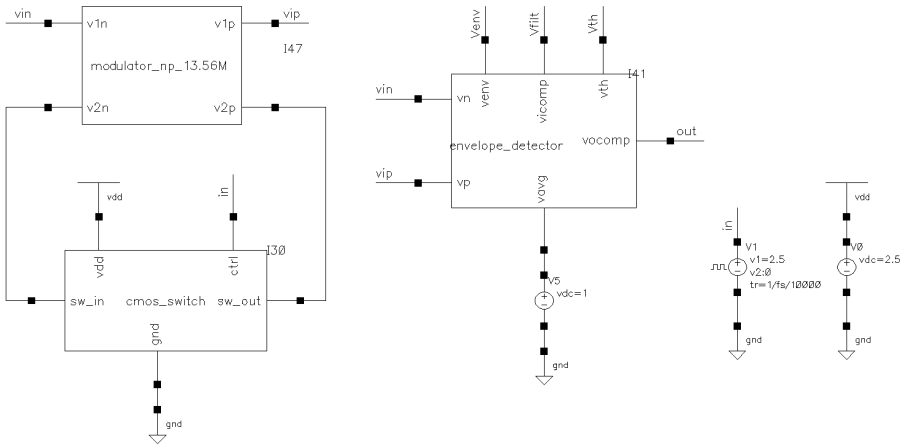


Figure 4.1: Test bench configuration for uplink transmission.

On the left of the schematic the modulating circuit is reported. The upper block accounts for the modulating circuit reported in Figure 3.22, with the four terminals identifying the positive and negative output voltage nodes at the primary and at the secondary circuit.

The lower block represents, instead, the CMOS switch of Figure 3.39 realizing the transfer of information. In the uplink direction, the switch is connected at the secondary between nodes v_{2n} and v_{2p} while the differential output voltage is retrieved at the primary between v_{1n} and v_{1p}.

The last block, on the right, accounts for the envelope detector of Figure 3.40. The two terminals on the left feed the circuit with the differential output voltage, while the reference voltage V_{avg} is fed directly from the lower terminal. The waveform representing collected and demodulated output data varying in between binary "0" and "1" is retrieved from terminal *out* on the right.

Last, the three terminals on top of the block collect the intermediate outputs of the envelope detector, such as the output of the full-wave rectifier V_{env}, the filtered version V_{filt} and the threshold voltage V_{th}, which should ideally coincide with V_{avg}.

The supply voltage, provided from the voltage generator on the extreme right, is fixed to $V_{DD} = 2.5\,V$.

In order to simulate the data transfer, the switch regulating the LSK modulation is driven by the signal *in*, accounting, indeed, for the data to be transfered. In this set of simulations, the signal *in* is a square wave varying between $0\,V$ and $V_{DD} = 2.5\,V$, with fundamental frequency f_s. Exploiting this configuration, by varying the frequency f_s of the square wave, it is possible to simulate the system's performance at different data rates.

More specifically, since a period of the square wave includes both a binary "0" and a binary "1" and therefore two bits, the data rate coincides with

twice the fundamental frequency f_s.

The rise and fall times of the square wave are chosen to be significantly small, fixed at 0.01% of the period.

Since the coupling coefficient k varies, as retrieved from the specifications of the system, in between 0.008 and 0.029 according to the distance between the coils, each simulation is carried out for the two limit values $k = 0.008$ and $k = 0.029$.

The quality of the modulation is expected to be in general worse for $k = 0.008$ since this value implies weaker coupling between the two sides of the circuit and therefore a worse reflection of the changes in one of the two sides on the other side.

Since the circuit was designed to operate at three different frequencies, also the simulations are carried out for all the three different configurations.

The test bench deployed for the analysis of the circuit's performance in the dowlink direction of transmission is, instead, reported in Figure 4.2.

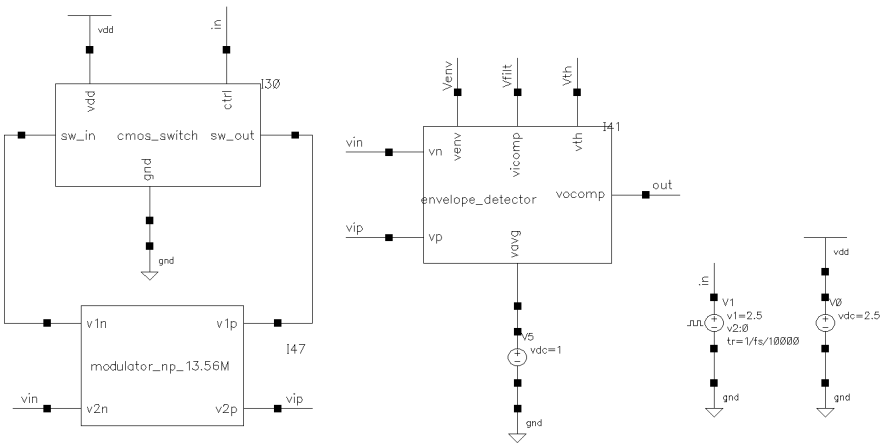


Figure 4.2: Test bench configuration for downlink transmission.

As visible from the schematic, the only difference with respect to the uplink test bench lies in the different connection between the data link block and the switch. Indeed, in this configuration, the switch is connected at the primary in between v_{1n} and v_{1p}, while the output voltage to be fed to the envelope detector is collected at the secondary between v_{2n} and v_{2p}.

4.2 Simulation Results

Ideally, the system is designed to work at a carrier frequency $f_0 = 13.56\,\text{MHz}$ and, therefore, the first simulations are performed at this frequency.

In the uplink direction, only a data rate of few kb/s is required and, therefore, f_s is chosen equal to 20 kHz, leading to a simulated data rate of 40 kb/s. Figure 4.3 reports the differential output voltage at the primary between terminals v_{1p} and v_{1n}, both for $k = 0.008$ (green) and for $k = 0.029$ (red).

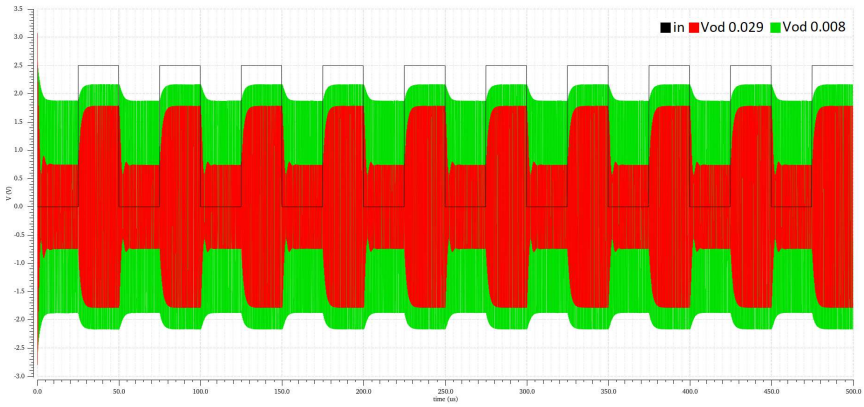


Figure 4.3: Uplink at 13.56MHz: modulated output voltage at 40 kb/s.

It is visible from the plot that the circuit is realizing a satisfactory modulation with a pronounced difference between the two output voltage amplitudes of around $1\,V$ for $k = 0.029$ and a more limited one of around $300\,mV$ for $k = 0.008$.

The aforementioned differential voltage is then fed to the envelope detector, producing the output plot reported in Figure 4.4. More specifically, Figure 4.4 is split into three sub-windows. The upper plot reports the differential output voltage at the primary, as reported in Figure 4.3. The middle sub-window collects the intermediate outputs of the envelope detector, such as the output of the full-wave rectifier V_{env}, its filtered version V_{filt} and the threshold voltage V_{th}. Last, the bottom sub-window collects the data flow recovered at the output *out* and compares it to the input signal *in*.

All these plots are, once again, collected for the two limit values of the coupling coefficient: $k = 0.008$ and $k = 0.029$.

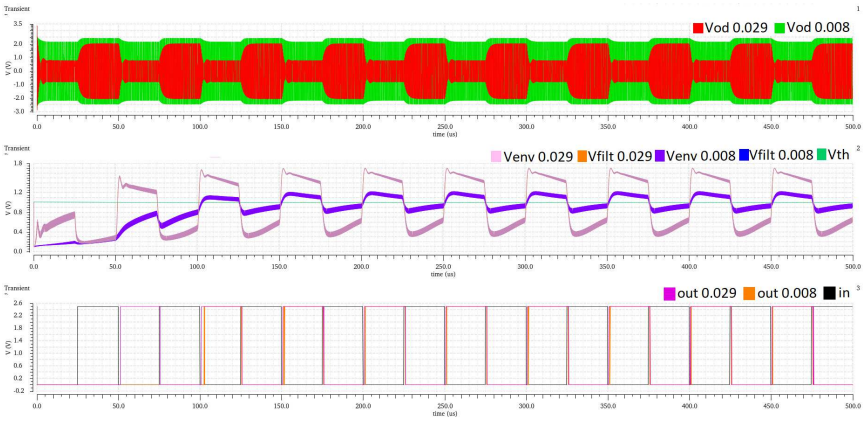


Figure 4.4: Uplink at 40 kb/s with $f_0 = 13.56\,\text{MHz}$.

It is visible from the plot of the output waveform that some post-processing should be applied in order to accurately compare the output to the input data. Indeed, Figure 4.5 reports the input signal together with a properly shifted version of the waveform recovered at the output, as to have the rising edges of the two waveforms aligned.

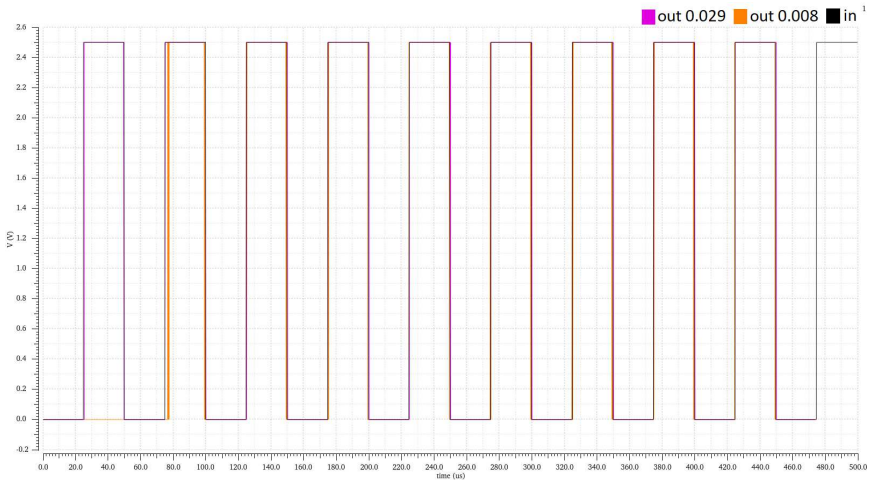


Figure 4.5: Uplink at 40 kb/s with $f_0 = 13.56\,\text{MHz}$: *out* aligned to *in*.

From this result, it is then easier to accurately evaluate the quality of the system's performance. Indeed, it is noticeable that after a transient of around 100 μs has extinguished, the output signal resembles quite accurately the input, satisfying the specifications.

Conversely, in the downlink direction of transmission the circuit is not able to achieve the required data rate of 5 Mb/s. Several simulations were carried out for different data rates in order to estimate the maximum feasible data rate for downlink at 13.56 MHz.

Figure 4.6 reports the differential output voltage at the secondary between terminals v_{2p} and v_{2n}, both for $k = 0.008$ (green) and for $k = 0.029$ (red) at $f_s = 50\,\text{kHz}$ and therefore at a starting data rate of $100\,\text{kb/s}$.

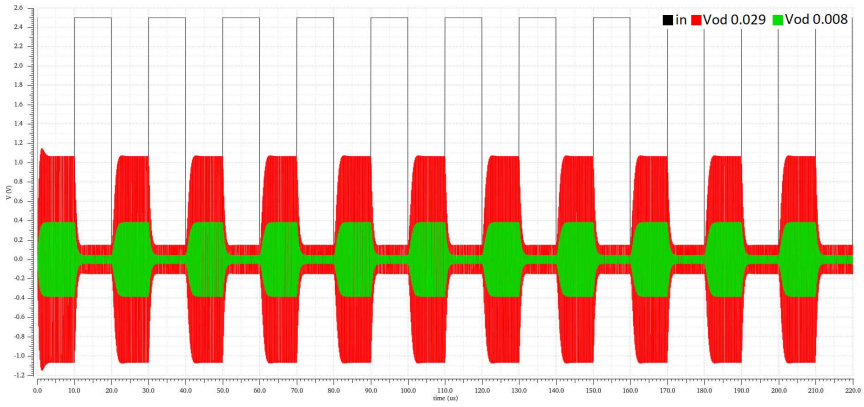


Figure 4.6: Downlink at 13.56MHz: modulated output voltage at 100 kb/s.

From a first glance at this figure, it is clearly noticeable that the quality of the modulation is increased with respect to the uplink transmission (Figure 4.3). This result suggests that, in principle, a larger data rate can be achieved for the downlink direction of transmission with respect to the uplink. This is in accordance with the desired behaviour for the system, since the main flow of information is supposed to go from the external device to the implant.

Nevertheless, as explored in the following, even though the downlink achieves better modulation than the uplink, it still struggles significantly to achieve a data rate even remotely close to the very demanding specifications.

Figure 4.7: Downlink at $100\,\text{kb/s}$ with $f_0 = 13.56\,\text{MHz}$.

Figure 4.7, similarly to Figure 4.4 for the uplink, collects the intermediate and the final output of the envelope detector and compares it to the input

data flow.

Once again, the output appears to be shifted by a constant amount with respect to the input and therefore, some necessary post-processing allows to obtain the plot of Figure 4.8.

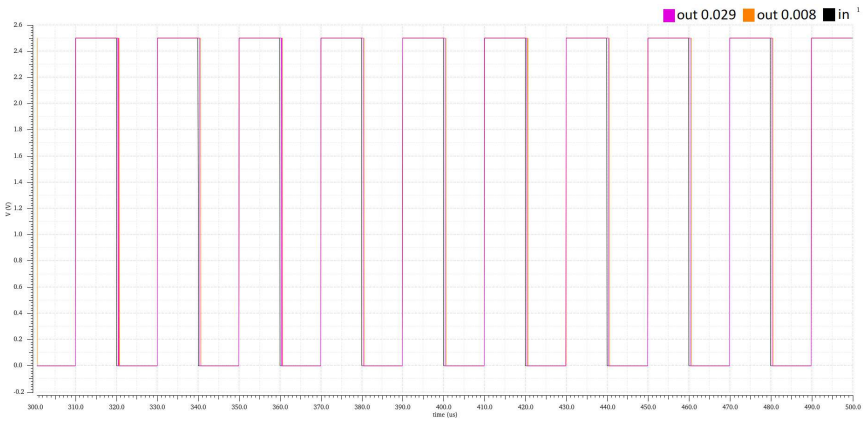


Figure 4.8: Downlink at 100 kb/s with $f_0 = 13.56$ MHz: *out* aligned to *in*.

The result is, also in this case, satisfactory enough. Indeed, aligning the rising edge of input and output, the output slightly departs from input in the falling edge with a relative error that is always below 5%. The result is slightly better for the larger value of the coupling coefficient.

For the sake of brevity and to avoid unnecessary repetition, for all the other simulations at different data rates only the collection of the output waveforms of the envelope detector and their post-processed versions are reported.

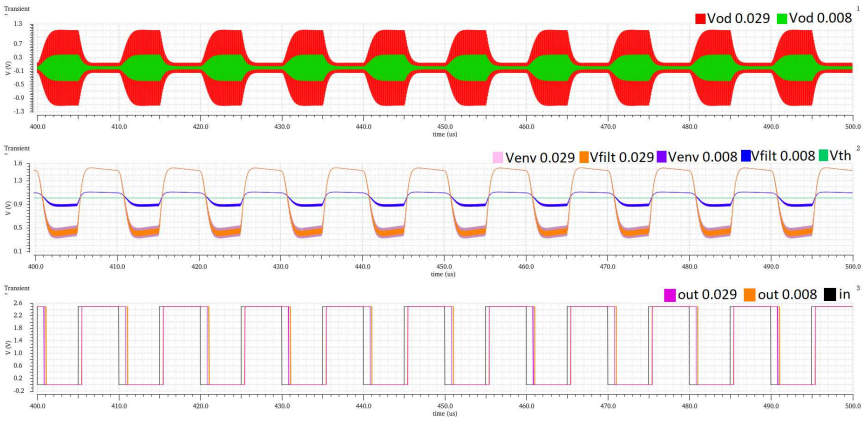


Figure 4.9: Downlink at 200 kb/s with $f_0 = 13.56$ MHz.

Figure 4.9 reports the output waveforms for $f_s = 100$ kHz and, therefore,

at a data rate equal to 200 kb/s, while the properly aligned output waveforms are reported in Figure 4.10.

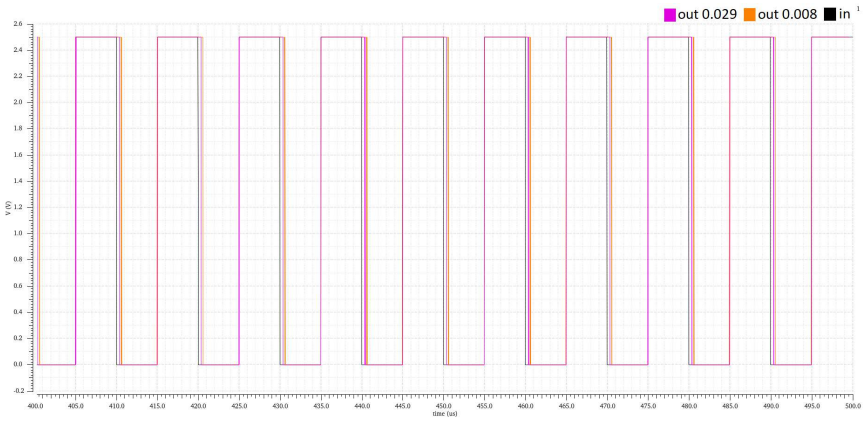


Figure 4.10: Downlink at 200 kb/s with $f_0 = 13.56$ MHz: *out* aligned to *in*.

At this data rate, the circuit operation is still reliable enough, but as the data rate is increased the quality of the performance drops very rapidly.

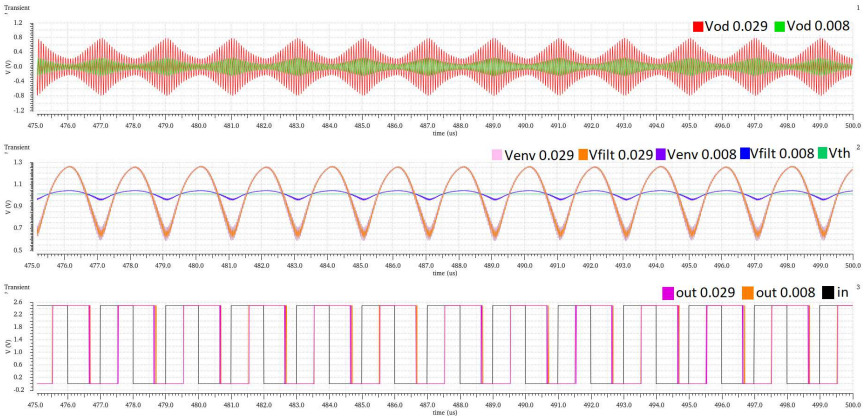


Figure 4.11: Downlink at 1 Mb/s with $f_0 = 13.56$ MHz.

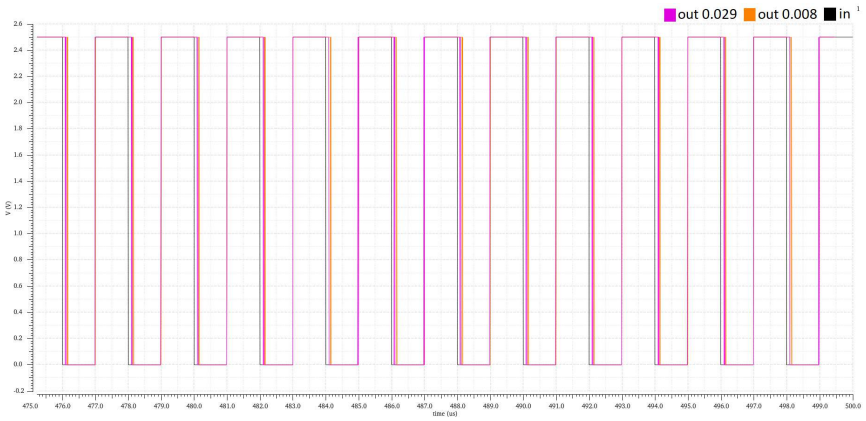


Figure 4.12: Downlink at 1 Mb/s with $f_0 = 13.56$ MHz: *out* aligned to *in*.

Already from a 1 Mb/s data rate, as reported in Figures 4.11 and 4.12, a first decline in performance is visible. This is even more evident in Figure 4.13, comparing the input square wave to the properly shifted output signal for a data rate of 2 Mb/s ($f_s = 1$ MHz).

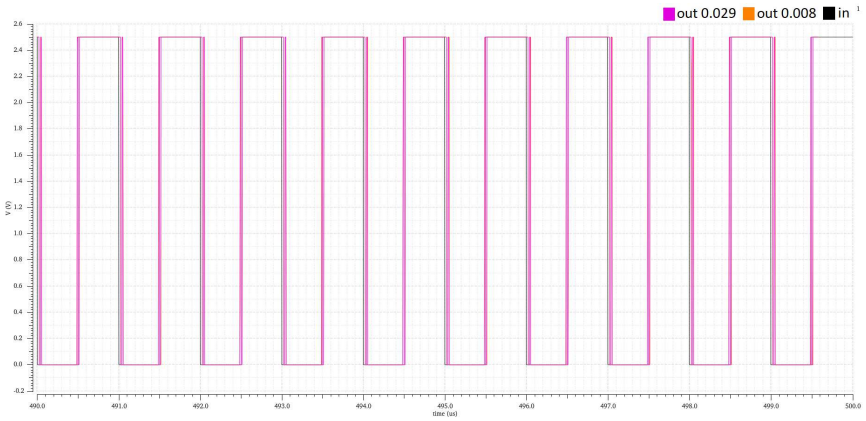


Figure 4.13: Downlink at 2 Mb/s with $f_0 = 13.56$ MHz: *out* aligned to *in*.

Clearly, as the data rate is increased at 2 Mb/s or above, the system is no more able to achieve a satisfactory result. This result suggests that some alternative configurations should be explored in order to achieve reliable downlink communication at a larger data rate, in order to meet the demanding specification requiring a data rate of 5 Mb/s.

The most intuitive strategy to speed up the system and achieve a larger data rate is to move to a higher operating frequency, by working at multiples of 13.56 MHz, while remaining within the ISM band to meet the requirements.

Indeed, by increasing the working frequency of the system, the impact

of the transient time before the oscillation settles to the maximum value becomes less relevant. This represents the main reason why the system was designed to work at three different carrier frequencies: 13.56 MHz, 27.12 MHz and 40.68 MHz.

First, the system working at 27.12 MHz is considered, in order to evaluate whether the increase in frequency is enough to meet the specifications. Starting from the uplink direction of transmission, Figure 4.14 reports the output waveforms at a data rate of 40 kb/s, while Figure 4.15 eases the performance evaluation by aligning the output to the input as explained before.

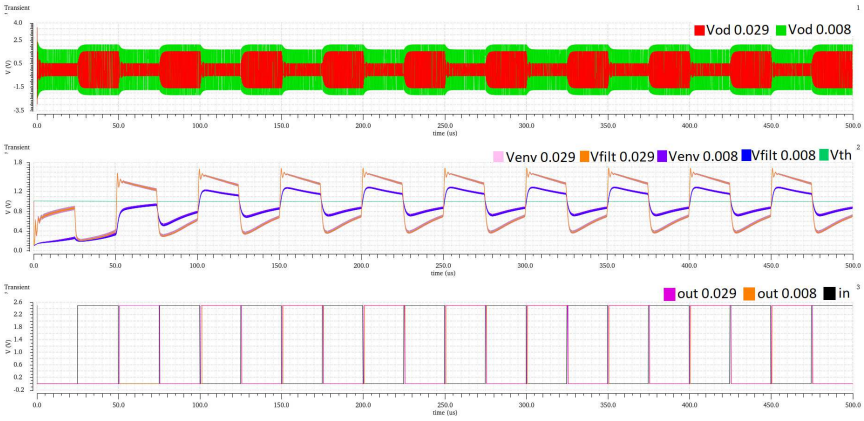


Figure 4.14: Uplink at 40 kb/s with $f_0 = 27.12$ MHz.

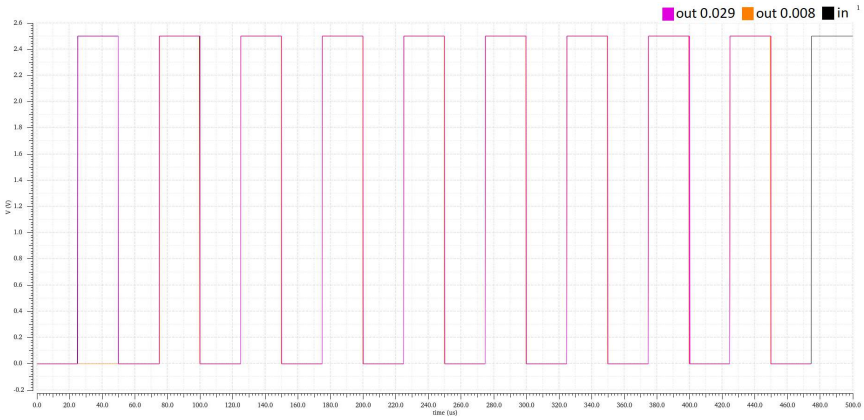


Figure 4.15: Uplink at 40 kb/s with $f_0 = 27.12$ MHz: *out* aligned to *in*.

No significant improvement is introduced in the uplink direction of transmission, since the system had already achieved a satisfactory performance at the required data rate with $f_0 = 13.56$ MHz. Conversely, operating at 27.12 MHz allows to increase the maximum achievable data rate in downlink, accomplishing reliable transmission at up to 2 Mb/s, as reported in Figures

4.16 and 4.17. Indeed, by comparing Figure 4.13 and Figure 4.17, it is apparent that the increase in carrier frequency significantly benefits the system's performance since at this data rate the performance of the 13.56 MHz circuit had already become insufficient.

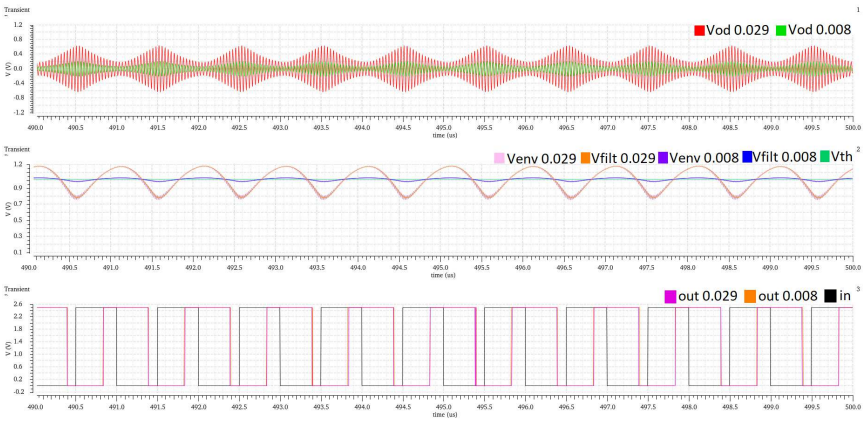


Figure 4.16: Downlink at 2 Mb/s with $f_0 = 27.12$ MHz.

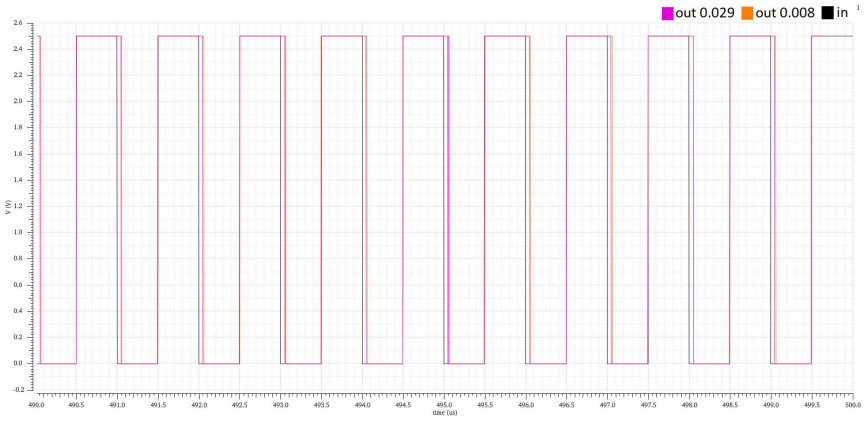


Figure 4.17: Downlink at 2 Mb/s with $f_0 = 27.12$ MHz: *out* aligned to *in*.

Nevertheless, as the data rate is further increased to 4 Mb/s, the quality of the data transfer is no more acceptable, as it is visible from Figures 4.18 and 4.19.

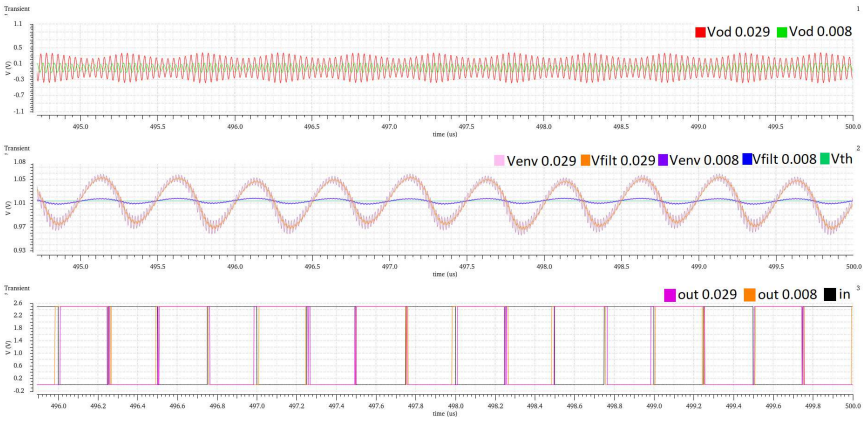


Figure 4.18: Downlink at 4 Mb/s with $f_0 = 27.12\,\text{MHz}$.

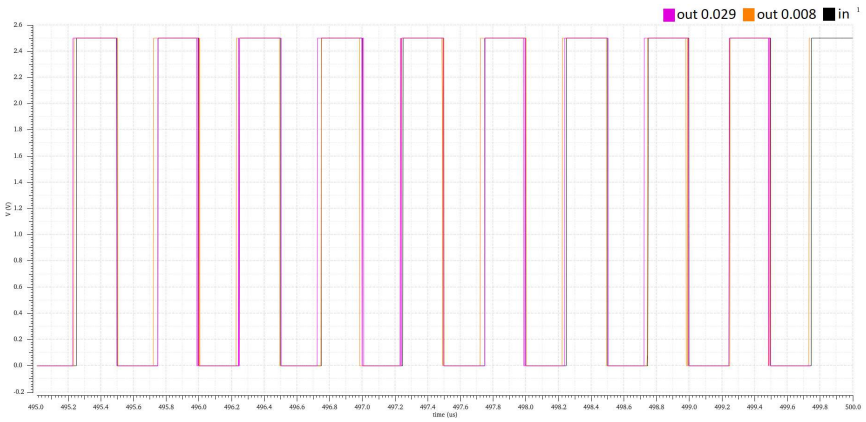


Figure 4.19: Downlink at 4 Mb/s with $f_0 = 27.12\,\text{MHz}$: *out* aligned to *in*.

Consequently, it becomes necessary to analyze the behavior of the system at a further increased carrier frequency $f_0 = 40.68\,\text{MHz}$, in order to evaluate whether this third system is able to meet the specifications. First, once again, the uplink waveforms at 40 kb/s are reported in Figures 4.20 and 4.21. No significant improvement is visible for the plot but, once more, the system fully meets the requirements in uplink.

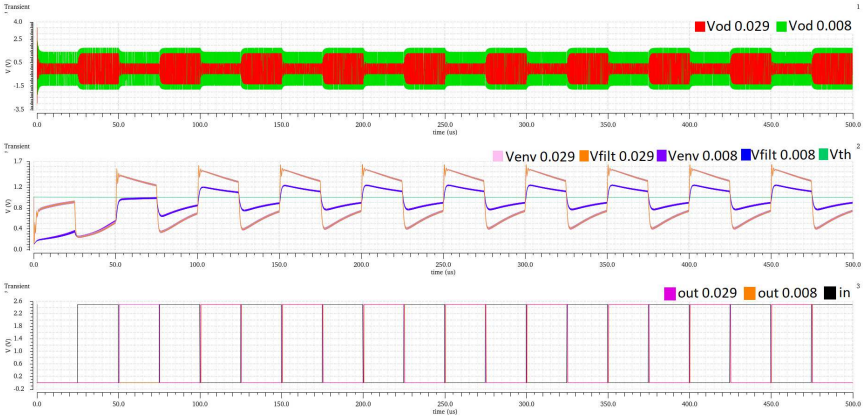


Figure 4.20: Uplink at 40 kb/s with $f_0 = 40.68$ MHz.

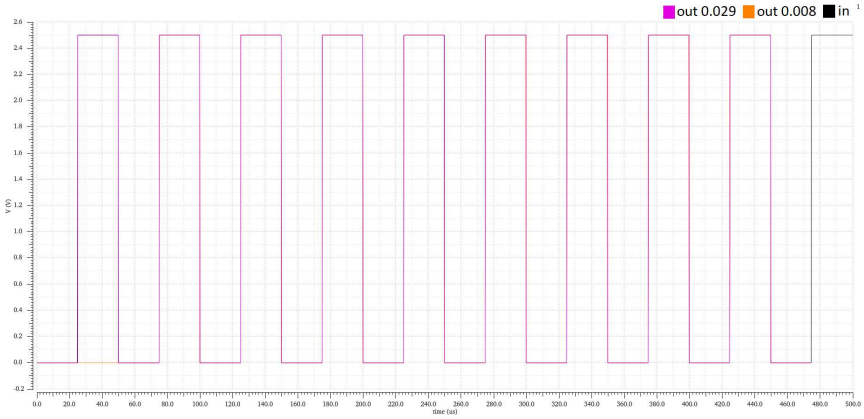


Figure 4.21: Uplink at 40 kb/s with $f_0 = 40.68$ MHz: *out* aligned to *in*.

Downlink specifications are, again, far more challenging. Figures 4.22 and 4.23 display high quality performance at 4 Mb/s, showing the superiority of this design with respect to the previous ones.

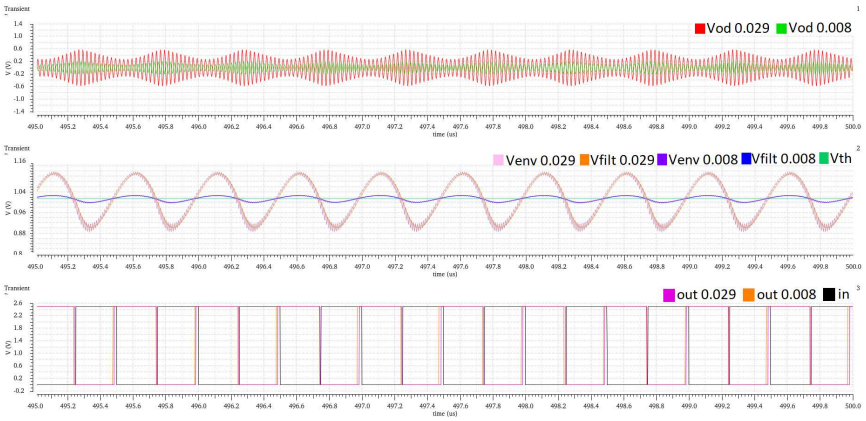


Figure 4.22: Downlink at 4 Mb/s with $f_0 = 40.68$ MHz.

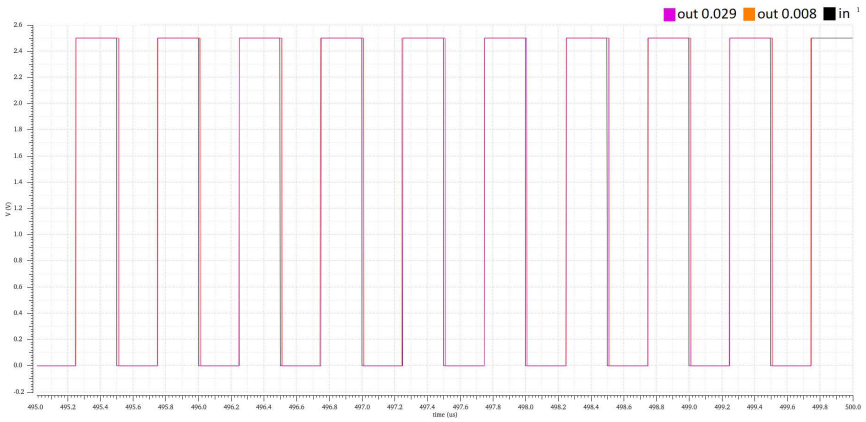


Figure 4.23: Downlink at 4 Mb/s with $f_0 = 40.68$ MHz: *out* aligned to *in*.

Unfortunately, even with this configuration, communication at the required data rate of 5 Mb/s is not fully reliable. Indeed, Figures 4.24 and 4.25 show worsened performances. Nevertheless, the error between the input and output data, even if more visible, is always below 10%.

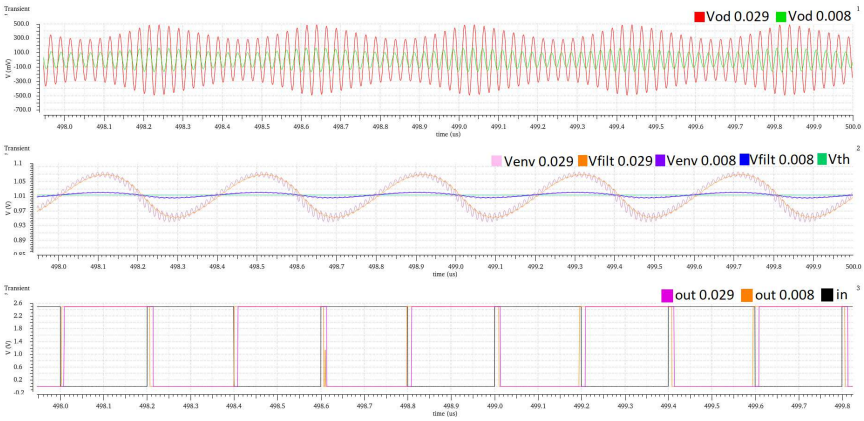


Figure 4.24: Downlink at 5 Mb/s with $f_0 = 40.68$ MHz.

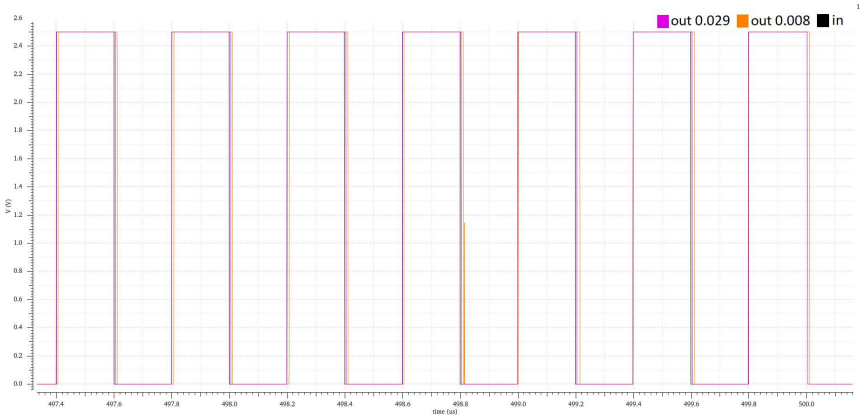


Figure 4.25: Downlink at 5 Mb/s with $f_0 = 40.68$ MHz: *out* aligned to *in*.

In conclusion, relying on the first design of the system at a carrier frequency of 13.56 MHz proves, very rapidly, to be an inadequate choice due to the very demanding specifications on the data rate for the downlink direction of transmission. It becomes then necessary to explore two different designs at an increased value of the carrier frequency f_0 but, unfortunately, also these configurations become soon flawed with errors varying between 5% and 10%.

These results suggest the idea that LSK techniques are unsuitable in applications requiring high data rate, such as the one considered in this work.

Nevertheless, another possible design approach, still based on LSK modulation is investigated in the last section of this chapter.

4.3 Alternative Design: n = 3

This section explores an alternative design for the inductive link. In this configuration the two coils composing the link are realized with different values of inductance. In particular in this case the turn ratio is fixed to $n = \sqrt{\frac{L_2}{L_1}} = 3$ and, therefore, $L_2 = 9L_1$.

The idea behind this design approach is to leverage on $n > 1$ in order to compensate for the low value of the coupling coefficient k. Indeed, as previously appointed, the pair of coils basically forms a transformer with ratio $1 : nk$. If $n = 1$, being k very small, the coupling between the primary and the secondary circuits will be in general very weak.

However, by increasing the value of the product nk, the coupling can be strengthened. This would in principle bring benefits to the quality of the modulation, since a stronger coupling between the coils leads to variations in one of the two sides of the circuit (due to the presence of the switch) reflecting more strongly on the other side.

Unfortunately, the results reported in this section show that this approach actually proves to be unfavourable. Table 4.1 reports the values for the main components constituting the data link at the working frequency of 13.56 MHz both for $n = 1$ and $n = 3$.

Parameter	13.56 MHz (n=1)	13.56 MHz (n=3)
L_1	1.5 μH	166.67 nH
L_2	1.5 μH	1.5 μH
C_1	91.84 pF	826.56 pF
C_2	91.84 pF	91.84 pF
Q_{L1}	200	110
Q_{L2}	140	140
R_{L_1}	639 mΩ	129 mΩ
R_{L_2}	913 mΩ	913 mΩ

Table 4.1: RLC resonators components at 13.56 MHz for $n = 1$ and $n = 3$.

The design of the system is then completed by following the procedure explained in Section 3.3, leading to the components sizing reported respectively in Table 4.2 for the uplink and Table 4.3 for the downlink.

Parameter	13.56 MHz (n=1)	13.56 MHz (n=3)
$R_{2_o}ff$	6390 Ω	6390 Ω
$R_{2_o}ff$	511 Ω	511 Ω
R_1	50 kΩ	10 kΩ
I_{tail}	150 μA	1.5 mA

Table 4.2: Uplink n=3: circuit parameters.

Parameter	13.56 MHz (n=1)	13.56 MHz (n=3)
$R_{1_o}ff$	6390 Ω	710 Ω
$R_{1_o}ff$	511 Ω	142 Ω
R_2	3 kΩ	5 kΩ
I_{tail}	500 μA	7 mA

Table 4.3: Downlink n=3: circuit parameters.

Focusing first on the uplink, Figure 4.26 reports the output of the envelope detector with $n = 3$ at 40 kb/s.

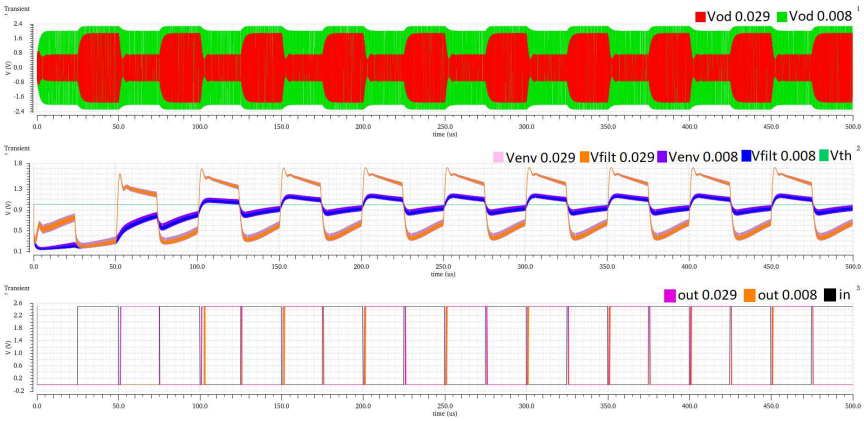


Figure 4.26: Uplink at 40 kb/s with $f_0 = 13.56$ MHz (n=3).

The result, that is made more evident from the comparison with the $n = 1$ case reported in Figure 4.27, is that increasing the turn ratio n proves not to bring significant advantages to the quality of the uplink transmission, which was already good enough for $n = 1$. Conversely, choosing $n = 3$ leads to dealing with a larger tail current of about 1.5 mA which increases significantly the power consumption of the system and is therefore undesirable.

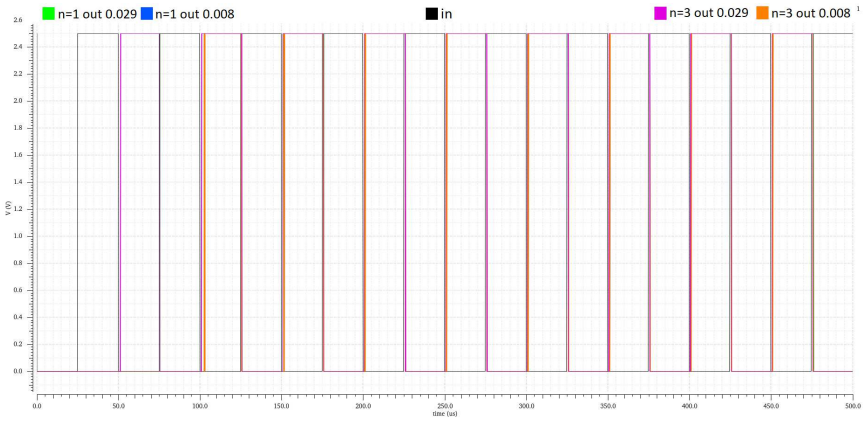


Figure 4.27: Uplink at 40 kb/s: $n = 1$ vs $n = 3$.

Similar conclusions can be drawn also concerning the downlink transmission. Indeed, Figure 4.28 and Figure 4.29 report the output waveforms in the case $n = 3$ respectively at 1 Mb/s and 2 Mb/s.

From the comparison with the corresponding plots for $n = 1$ it can be noticed that increasing the turn ratio doesn't improve the behavior of the system which at a data rate of 2 Mb/s becomes, actually, even worse than what was obtained with $n = 1$.

Moreover, this configuration requires a dramatically large current of about 7 mA which, compared to the 400 μA needed for $n = 1$, is clearly increasing significantly the power consumption of the overall system.

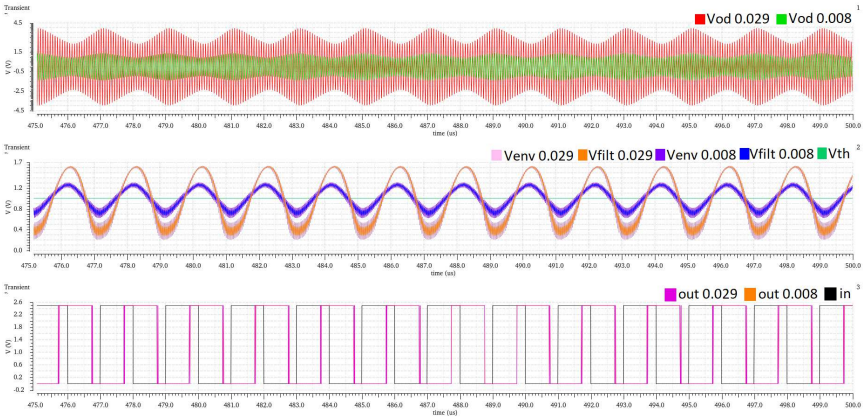


Figure 4.28: Downlink at 1 Mb/s with $f_0 = 13.56$ MHz (n=3).

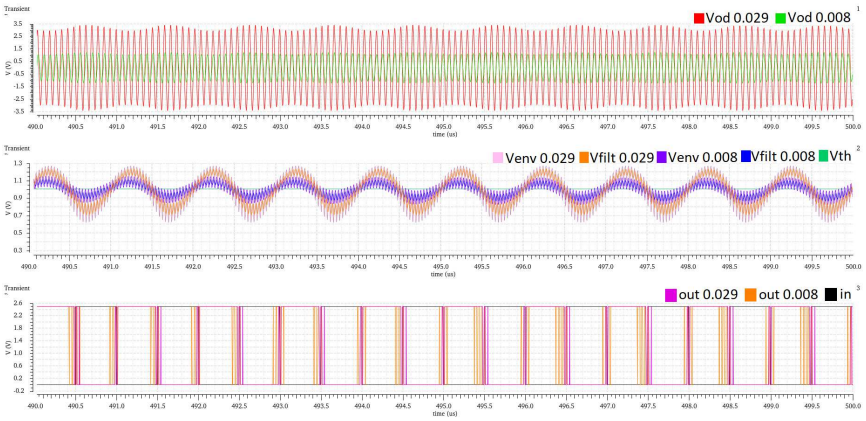


Figure 4.29: Downlink at 2 Mb/s with $f_0 = 13.56$ MHz (n=3).

For the sake of comparison, Figure 4.30 reports the input and output data for downlink transmission at 100 kb/s. Even at a low data rate, the unitary turn ratio design proves to be a better choice for the realization of the coils constituting the link.

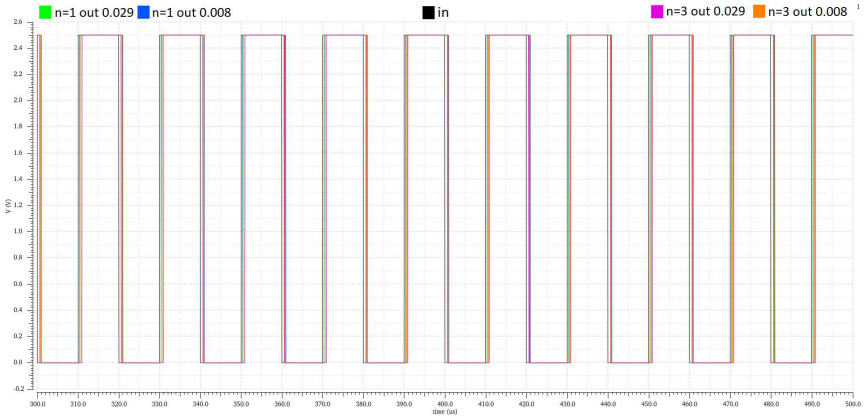


Figure 4.30: Downlink at 100 kb/s: $n = 1$ vs $n = 3$.

In conclusion, due to the proven inadequacy of this design for 13.56 MHz, it is considered pointless to overload the discussion by dwelling on the $n = 3$ designs and simulations at higher carrier frequencies.

Chapter 5

Conclusions and Future Work

This last chapter summarizes the main conclusions drawn from this thesis work, before discussing some possible improvements to be made to the designed circuit and providing some useful suggestions for future work on the topic.

5.1 Conclusions

In this work a bidirectional half-duplex near field data communication system for an artificial retina was designed at three different carrier frequencies inside the ISM band: 13.56 MHz, 27.12 MHz and 40.68 MHz.

The data was transmitted by leveraging on LSK modulation both in the uplink and in the downlink directions, aiming to satisfy far more stringent constraints on the downlink side. Indeed, while for the uplink a data rate of only few kb/s was required, the downlink data transfer aimed at achieving reliable transmission at a speed of at least 5 Mb/s.

After the desired specifications were introduced and the basic principles behind the functioning of the system and of the artificial retina were discussed, the link was designed according to the procedure reported in Chapter 3.

Subsequently, several simulations were performed on the designed system, mainly targeting the evaluation of the maximum achievable data rate in each realized configuration. The results of the transient simulations showing the recovered and demodulated output data and comparing it to the input data flow were reported in Chapter 4.

The designed system proved to be reliable enough in the uplink transmission for each of the three carrier frequencies at which it was designed. Indeed, as reported in Figures 4.5, 4.15 and 4.21, the recovered data at the output resembled accurately the input data stream, with very low relative error. In this situation, given the obtained results, it would be preferable to deploy the system working at the lowest carrier frequency in order to reduce

as much as possible the power absorption and consequently also limit the possible health hazards associated to the implant.

Unfortunately, transmission in the dowlink direction was not able to fully meet the specifications. The analysis of the performance of the system during the downlink transmission started at the lowest value of the carrier frequency since, as previously explained, it is preferable to work at the lowest possible frequency, but the 13.56 MHz system rapidly proved its inadequacy.

In fact, the 13.56 MHz data link was able to achieve acceptable communication only up to a data rate of 1 Mb/s. The 27.12 MHz system was, instead, able to extend the transmission up to 2 Mb/s and finally the 40.68 MHz system was the best choice in order to approach the demanding specifications.

Indeed, it was able to achieve quite a satisfactory result at 4 Mb/s and to approach an almost acceptable data transfer at 5 Mb/s, displaying a relative error between the input and the recovered output stream of around 10%.

The main conclusion that can be drawn from these results is that load-shift keying techniques prove to be unsuitable in applications that require a large data rate. Indeed, while these techniques may be appealing since they allow to minimize the power consumption of the system, they strongly limit the maximum achievable data rate.

Unfortunately, in the target system both the power consumption level and the speed of data transfer represent paramount specifications, on which little compromise can be accepted. Indeed, while the power consumption must be kept low in order to minimize the possible risks associated to the implantation of the device on the human body, also the large volume of data collected from the external unit must be rapidly, reliably and efficiently sent to the implant to accurately implement artificial vision.

Subsequently, these results already suggest some directions to be further explored in the future work on the matter.

5.2 Future Work

First and foremost, some small improvements to the designed circuit could in principle enhance the quality of the modulation, while allowing to deploy the LSK technique in both directions of transmission.

In fact, a more sophisticated envelope detector could be designed, relying for example on the use of an active filter instead of a passive one. The implementation of this kind of filter would bring significant benefits, allowing to compensate for the reduction in the amplitude of the envelope introduced by the envelope detector, with the consequence of achieving a larger index of modulation.

In the eventuality that the resulting modulation is still far from satisfactory, a more drastic solution can be evaluated.

Indeed, as mentioned in the previous section, significant improvements

to the system could be made by deploying a different modulation technique in the dowlink direction of transmission. More specifically, the deployment of carrier-less modulation techniques such as pulse harmonic (PHM) and pulse delay (PDM) modulations could strongly enhance the quality of the modulation, since they can, in principle, achieve reliable transmission at significantly larger data rates, as discussed in Section 2.3.2.

Even though the main focus in this work is placed on the fulfillment of the requirements related to the speed of the system, there are several other enhancements that could be applied to the designed system in order to make it more suitable for the application taken into consideration.

The analysis carried out in this work was, in fact, limited to the case of two coils lying on the same plane and presenting the same relative orientation. This hypothesis limits significantly the accuracy of the actual system in practical situations. Indeed, in visual prostheses such as the artificial retina to be realized, the orientation of the coils varies continuously following the movements of the eyes of the patient.

Therefore, robustness of communication is required not only against variations in the distance between the coils but also against changes in their relative orientation. Starting from the analysis carried out in this work, it is then straightforward to notice that taking into account the variations of the angle θ between the planes of the coils will lead to dealing with even lower values of the coupling coefficient k, limiting far more significantly the achievable quality for the data transmission.

As an alternative approach also capacitive coupling could be considered to realize the data link. Even though the superiority of inductive coupling in biomedical applications, due to the reduced health hazards associated to these technologies, was already mentioned in Section 2.1, the capacitive realization could be more accurately analyzed in order to establish whether it is able to achieve a more fast and reliable transfer of data.

Lastly, a significant topic that was not explored in this work regards the need to integrate a mechanism of power transfer into the system. As it was mentioned multiple times in this document, the implanted device will require some sort of power supply in order to work and it is clearly unfeasible to rely on batteries to realize the power-up of the implant. Indeed, the invasiveness of the process of recharging or replacement of the battery, which would require the surgical removal of the implant, makes it strongly unsuitable.

Therefore, besides the path for data transmission, a second path for wireless power transfer should be designed for the system. This could be done in practice by deploying a second pair of coils working at a different, much lower, frequency to minimize interference [11] or, once again, by relying on carrier-less modulation schemes. [9]

In conclusion, this work has shed light on several details to be further investigated and suggested a variety of directions in which this research could

and should proceed, highlighting the key role played by inductively-based near field technologies in biomedical applications.

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