Università degli studi di Padova

Laurea Magistrale in Ingegneria Elettronica

WideBand Upconverting IQ Modulator Design in BiCMOS Technology

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Ai miei genitori
Riccardo e Mirna

Contents

Acknowledgments

Ringrazio per la grande opportunità offertami in questi ultimi sette mesi, il prof. Andrea Bevilacqua e il Dott. Marc Tiebout.

Un caloroso grazie è rivolto ai miei colleghi e amici Stefan e Daniele, che hanno condiviso con me quest'ultima esperienza a Villach.

D'altra parte voglio esprimere la mia immensa gratitudine per chi mi aspetta a casa in Italia, coloro i quali mi hanno sempre sostenuto su ogni mia scelta, grazie di cuore ai miei genitori Mirna e Riccardo, mia sorella Monia e mio cognato Luca.

Fortunatamente sono circodanto da molti amici, che non mi hanno mai fatto mancare un motivo per sorridere, sarebbe impossibile scrivere tutti i loro nomi, quello che mi resta da fare è dire grazie a voi amici e amiche di ZV, siete una famiglia.

Concludo con chi da un anno a questa parte ha radicalmente cambiato la mia vita, teşekkürler Özgün.

Abstract

The presented work

Mixers and frequency translation are key processes in the wireless systems who have increasingly stringent requirements for transmission of a clean signal with a low noise floor and low intermodulation and harmonic distortion.

The desired upconverting IQ modulator has to translate a baseband starting at DC ending at 500 MHz, to a radio frequency range between 1 to 15 GHz, fed by a 2 to 30 GHz LO frequency, since the IQ LO signals are provided by a frequency divider driven at the double of the output rate.

The core of the system is implemented by a couple of active mixers based on the Gilbert cell structure. All the system terminations are differential and have to be matched to the standard 100Ω equipment lab characterization. The design is oriented to reach a wide output dynamic range, reducing the total noise and ensuring a high linearity. These specifications are pursued taking advantage of the features provided by the SiGe BiCMOS technology. Since the baseband fits with the frequency response of the available CMOS devices, there is the opportunity to use them as linear transconductor of the active mixers. The larger range of linearity held by these devices, improves the intercept point reached by the modulator even without any degenerative topology. The trade-off represented in terms of noise performances, can be reduced by several solutions and the noise cancellation technique is a good candidate [4, 5] . By creating a highly linear and low noise transconductor cell, based on a CMOS noise canceling topology, and merging it with the performances of the

SiGe fast speed bipolar transistors, the designed structure achieves the single side band mixing with a output third order interception point greater than +10 dBm over the complete RF band, while the DSB noise figure is held below 12 dBm . The designed structures have a differential matched termination for all the input and output port, confirmed by a reflection coefficient kept lower than -10 dB. The design is supplied by a 3.3V single voltage and all signal pads are protected by ESD diodes. All the chip is analyzed and checked using Spectre and ADS tools. Hence, the modulator is implemented in a full-custom layout and the parasitic extraction is done. The problem of spurs deriving by the application of a square waveform as LO signal, which consequentially generates an unwanted higher order mixing, is investigated and a Multi-path Polyphase Mixer system is analyzed and simulated in order to indicate a way to suppress this distortion.

Chapter 1

Introduction

Nowadays the life has the aspect that we see thanks to the evolution of communications had within the last 20 years. The birth of the information era comes from the opportunity to communicate boundlessly, surpassing the concept of space distance. The exploit had by wireless communication networks, have contributed to the large diffusion of the radio frequency circuit design, which finds application in several areas as Voice and Data Telecommunication (Cellular System, WiFi, WPAN and UWB), identification/security systems(Transponders, security scanners) and object identification and positioning (GPSs and Radars).

In a day by day more digital world, the analog radio frequency design is an undeniable segment of the communication industry since what we hear and perceive are analogs. But this reality now is assuming a new form, the manufacturers are trying to make digital the most of the signal processing during the communication, limiting the analog circuitry just to the interface with the antenna. Indeed digital circuits are more scalable than the analog counterparts, limiting costs and increasing the integration. Radio Frequency circuits include passive components which are difficult to shrink causing a slower scaling and raising the total chip cost. The research done to enhance the analog design, suppressing its deficiencies, is directed toward the development of new topology able to reduce the area effort and the total cost.

Technologies act a fundamental role for the circuit optimization, providing new approaches to solve the aforementioned issues. The SiGe BiCMOS technology merges the proprieties of bipolar and CMOS into a single chip, combining the bipolar high-speed for the analog radio frequency operation with the low power consumption and the robustness of CMOS technology.

The developed modulator has to provide the upconverting translation in a Wideband Continuos-Wave Radar system. In this chapter is presented a first approach to these kind of systems, discussing the main applications and architectures available and analyzing their behaviors.

1.1 Radar Systems

Radar is an acronym for Radio Detection and Ranging, the term radio is referred to the use of EM waves to detect the position and the velocity of a specific target.

Radars can be employed into different applications:

- **Air Traffic and Maritime Navigation monitoring:** The tracking and the positioning of aircraft and ships can be detected by the use of radar systems.
- **Automotive**: To reduce traffic fatalities, radar system employ active safety systems as adaptive cruise control, collision warning systems, blind spot detection.
- **Military**: The radar is applied in a manifold of defence and surveillance systems applications.

  Two are the macro-typology of a radar system transmission:

  - **Pulse Radar :** Pulses of energy are irradiated in the space. The detection and ranging part are accomplished by timing the delay between transmission of a pulse of radio energy and its subsequent return

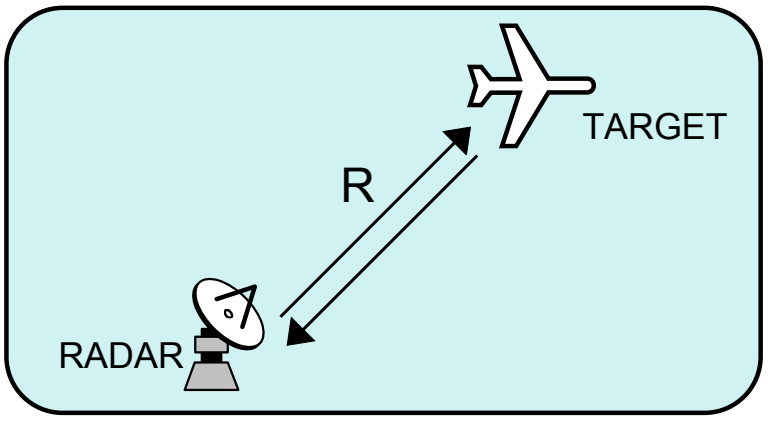

Figure 1.1: Radar ranging

– **Continuous-Wave radar :** emits electromagnetic radiation at all times, irradiating continuous sine wave. CW radar can measure the instantaneous rate-of-change of target's range. This is accomplished by a direct measurement of the Doppler shift of the returned signal. The Doppler shift is a change in the frequency of the electromagnetic wave caused by motion of the transmitter, target or both. For example, if the transmitter is moving, the wavelength is reduced by a fraction proportional to the speed it is moving in the direction of propagation. Since the speed of propagation is a constant, the frequency must increase as the wavelength shortens.

The CW radars provide a greater flexibility than pulse radar, furthermore, it is also possible to use a CW radar system to measure the position instead of the velocity, by frequency modulation, the systematic variation of the transmitted frequency. The simplest way to modulate the wave is to linearly increase the frequency. In other words, the transmitted frequency will change at a constant rate. Frequency Modulated CW Radars (FMCW) measure the frequency of the return signal, compute the differences of the transmitted and received frequency, then the period of the difference is directly proportional to the time delay between transmission and reception, hence the position can be extracted.

If R is the distance to detect, by transmitting a signal of frequency f_{tx}, modulated in a range $f_1 < f_{tx} < f_2$, and receiving a signal with frequency f_{rx}, the time delay between the two waveform is $\tau = T\frac{f_{tx}-f_{rx}}{f_2-f_1}$, where T is the period of sweep from f_1 to f_2.

The wanted distance is simply computed as $R = c \cdot \tau/2$.

1.2 Monostatic Phased Array Radars

The proprieties to have a steerable beam to direct in a defined and narrow direction during the transmission and the reception of an EM wave in a radar system, is reachable without using further mechanical parts, but just installing an array of antennas and controlling it electronically. A linear phased array antenna is a series of equidistant antennas whose effective (summed) radiation pattern can be altered by phasing the signals of the individual elements. By choosing the difference of phase of the signals injected for each antenna, the irradiated beam can be steered providing a fast and programmable antenna target pointing.

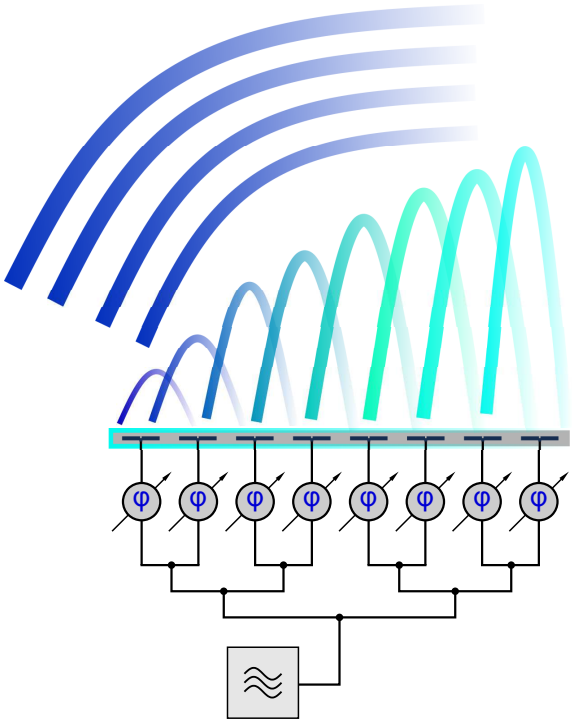

Figure 1.2: Model of a phased array antenna

A phased array radar implementing the transmission and the reception of EM waves sharing the antennas in both directions, belongs in the category of monostatic radar, hence the transmitter and the receiver have a common antenna.

1.3 WideBand upconverter for tracking radars

The objective in the design of communication module is to bring digital domain closer to the antenna at the receiving and transmitting ends using software defined radio. The phase shifting in digital beamforming is performed in the digital domain inside the digital signal processing. The module shown here (Fig. 1.3), illustrates how is implemented the signal path in a generic transmission module, which can deliver the phase shifted signal to the antenna array.

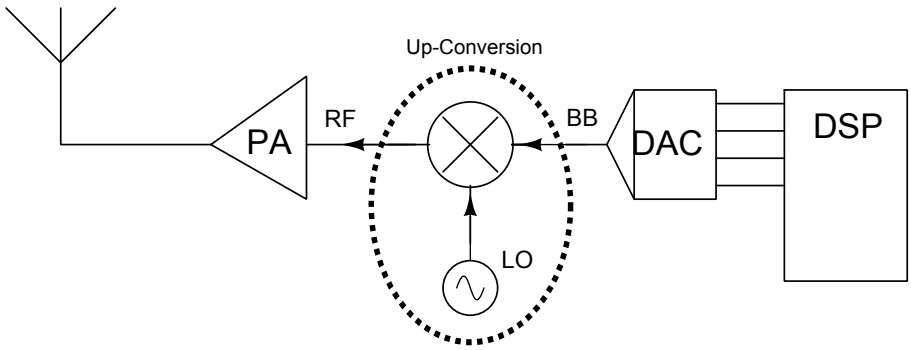

Figure 1.3: Model of a transmission module suitable for phased array antenna

The transmitting signal has to be translated in the transmission radio frequency range, by a mixer, this components is commonly followed by a power amplifier which properly boost the signal in order to make it suitable for the wanted transmission.

Due to that the modulation of the signal has to perform an important bridge between baseband and radio frequencies processing, ensuring a robust conversion. An available efficient implementation of a modulator is named single side band (SSB) mixer (see Fig. 2.1). The SSB mixer is the aim of this work.

The baseband signals are produced in the digital domain by a couple of DACs, which perform the initial phased delay to provide two IQ baseband signals. The LO signal feeds a frequency divider which generates the two IQ signals driving the couples of mixers employing the SSB upconverting modulation.

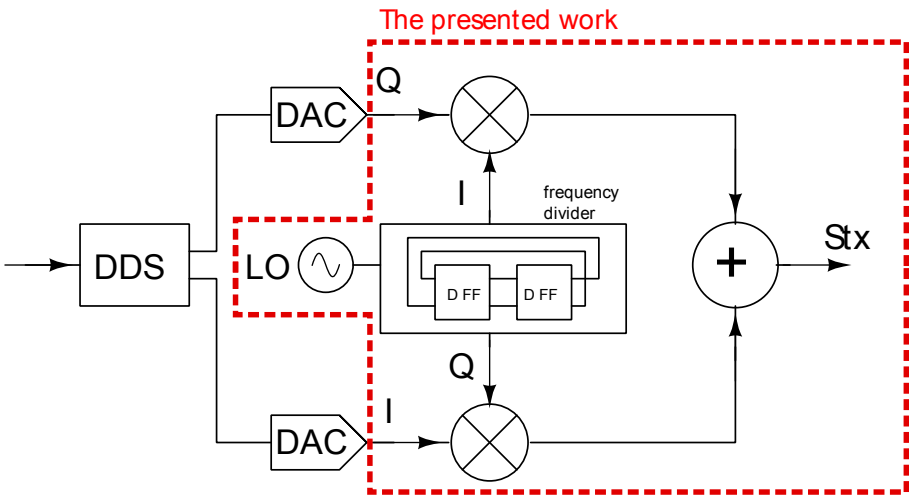

Figure 1.4: Model of a frequency Modulated CW Radar

1.4 Target Specifications

Upconversion mixers are fundamental modules in communication and radar systems converting the low frequency baseband (BB) signal to RF band. The noise figure which identifies the sensistivity of the circuit is a key of permonces of the upconversion mixer, delimiting the lower value of output power deliverable by the system. The compression point determines the maximum signal that the mixer can handle. The desired upconversion mixer has to guarantee a low NF and an high IIP3, describing a large dynamic range. Moreover, as discussed in the next chapter, applying an active mixer structure the focus of the design can not omit to verify an high image rejection and LO suppression.

All the performances for all the input and LO frequencies, have to be satisfied in a range of temperature from 0° to 85° and the a supply voltage variation of the 5%. Moreover, variations due process and mismatch have to be taken into account.

Parameters	Target Value
RF Output Frequencies	1 ... 15GHz
Baseband Input Frequencies	0..500 MHz
OIP3	$>$ 10dBm
SSB NF	$<$ 12dB
IRR	$>$ 30dBc
LO Feedthrough	$<$ 30dBc
Technology	b11hfc
Supply voltage	Single 3.3V
Area effort	Minimal (coils-less)

Table 1.1: Design Specifications

1.5 Infineon BiCMOS technology

The available technology is a SiGe BiCMOS provided by Infineon Technologies [16] , which makes possible to place on the same chip bipolar and CMOS devices. The enhancement is clearly understandable in the analog design when an application, as the wideband modulator is, requires processing of baseband signals and high radio frequencies signal in the same chip. The cost of a BiCMOS process is significantly higher than a normal full bipolar or CMOS technology.

SiGe homojunction bipolar transistor

The performance advantages of SiGe over pure silicon for RFIC applications are mainly the extremely high cutoff frequencies, f_{max} and extremely low current-mode logic gate delay. Furthermore, improved power-added efficiency (PAE) at low DC voltages makes SiGe HBTs a good choice for power amplifier applications. SiGe bipolar transistors are bipolar transistors with the presence of germanium in the base region, which reduces the band gap of the SiGe material.

The normal design of a bipolar transistor, presents an higher emitter doping if compared to the base decreasing the emitter junction efficiency, that is the ratio of the

electron current in the emitter, to the sum of the electron and hole diffusing across the base-emitter junction.

$$\gamma = \frac{I_{E_n}}{I_{E_n} + I_{E_p}} = \frac{1}{1 + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \tag{1.1}$$

In order to increase the efficiency mentioned above, this technology does not give the opportunity to decrease the base at the doping without getting lower the transition frequency. Even decreasing the base width maintaining constant the dope density the efficiency cannot be enhanced not increasing the base resistance.

By using the germanium as the base of the bipolar transistor, the doping density at the emitter is decreased, whereas the base doping got lower. This causes an higher transition frequency allowed to the bipolars.

The available bipolars belonging to the SiGe HBT technology have different performances depending on the application which are designed for. High voltage HBT offers an higher collector-emitter drop voltage causing the breakdown at the bipolar junction, on the other hand, low voltage HBT provides an higher speed .

Seven are the available levels of metallization, six of cupper and one of alluminium. The metal stack allows to have short and small connection to the lower levels, being more resistive compared with the top levels. On the other hand, the upper level are used to carry high currents and to implement high Q inductor.

1.6 Figures of Merit

This chapter explains the basic figures of merit used during the design to better describe the system performances.

1.6.1 Gain and Conversion gain

In a common linear system, the gain referred to the voltage or to the power is the ratio between input and output signal, describing the processing employed by the block to its stimulus.

The gain of mixers and modulator must be carefullly defined to avoid misunderstanding. In transmitter it is desiderable to raise the gain and hence the output swings of upconverter mixers.

The voltage conversion gain is the ratio of the rms voltage of the output modulated signal, to the rms voltage of the input modulating signal. The two waveform have different frequency, and it can be computed by applying, for istance in a upconversion mixer, a input cosine at ω_{BB} and finding the amplitude of the upconverted component at the desired ω_{RF}.

$$A_V = \frac{V_{RF}}{V_{BB}} \tag{1.2}$$

$$A_{V_{[dB]}} = 20log(A_V) \tag{1.3}$$

Traditionally the RF design, is characterized by a "power conversion gain", where the ratio is done on the output and input power signals.

$$G_P = \frac{P_{RF}}{P_{BB}} \tag{1.4}$$

$$G_{P_{[dB]}} = 10log(G_P) \tag{1.5}$$

1.6.2 Distortion

The distortion analysis is a topic of high interest in matter of telecommunication circuits, being the cause of spurious frequencies. Every difference between the shape of the output waveform in the time domain and the input, net after a scaling factor, is a distortion effect. Distortion has as straight forward consequence the phenom of the compression, describing the upper limit of the signals which a system can generate.

The distortion here analyzed is the weak distortion, where the harmonics gradually disappear when the signal amplitude becomes smaller, then, the analysis is limited at the low distortion region where only second and third order distortion components are considered.

The most important case of distortion related to this design, is the nonlinear distortion caused by a system which has a nonlinear characteristic:

$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 \tag{1.6}$$

If a_0 represents the dc component and a_1 the linear gain of the nonlinear system, the remaining coefficients reproduces the system distortion. An analytic expression of the output y, can give the a_i coefficients as:

$$a_i = \frac{1}{n!}\frac{\partial^i y}{\partial u^i}\Big|_{u=0} \tag{1.7}$$

By applying a cosine waveform $u = U\cos(\omega t)$, the output becomes :

$$y = \left(a_0 + \frac{a_2}{2}U^2\right) + \left(a_1 + \frac{3}{4}a_3 U^2\right)U\cos(\omega t) + \frac{a_2}{2}U^2\cos(2\omega t) + \frac{a_3}{4}U^3\cos(3\omega t) + .. \tag{1.8}$$

All the combinations of coefficients deriving from the cosine multiplication proprieties

are part of the distortion.

It is important to understand how much the linear response is compromised by the upper harmonics, thus, how is modified the signal component at the fundamental frequency. The Harmonic Distortion is defined as the ratio of the component of frequency multiple of ω to the one at the fundamental.

$$HD_2 = \frac{1}{2}\frac{a_2}{a_1}U \tag{1.9}$$

$$HD_3 = \frac{1}{4}\frac{a_3}{a_1}U^2 \tag{1.10}$$

It is important to note that HD_2 is proportional to the amplitude of the input signal, on the other hand the HD_3 to the amplitude squared. This point spot the higher relevance of the third harmonic distortion in the most of the case.

Intermodulation

It is important to take into account the issue of two close harmonics as input, reproducing the case of a disturb at the input of the transmission system. Under low-distortion conditions, with two cosine waveforms of frequencies ω_1 and ω_2 injected at the input, then thee output signal contains all the combinations of these harmonics and their multiples: $k\omega_1 + m\omega_2$.

The second-order intermodulation distortion IM_2 is defined by the ratio of the component at frequency $\omega_1 \pm \omega_2$. Its third order version IM_3 is detected at the the frequencies $2\omega_2 \pm \omega_1$ and $2\omega_1 \pm \omega_2$.

$$IM_3 = \frac{3}{4}\frac{a_3}{a_1}U^2 = 3HD_3 \tag{1.11}$$

$$IM_2 = \frac{a_2}{a_1}U = 2HD_2 \tag{1.12}$$

The correspondence between third harmonic and intermodulation distortion is a reason why they are more important than the HD_3, in fact the value of IM_3 is three times larger than the one of HD_3 and this gets it easily measurable. Generally, a further characteristic that makes this distortion attractive in matter of design, is the close occurrence of the tone at $2\omega_{1,2} - \omega_{1,2}$ to the fundamental tone. In a case of wideband response, this consideration is partially true: from Fig.(1.5) is easily understandable that, more IM_3 takes a more important role if the range of frequencies taken in account is wider. In place of design, is necessary to limit these components and shaping it by the active mixer frequency response.

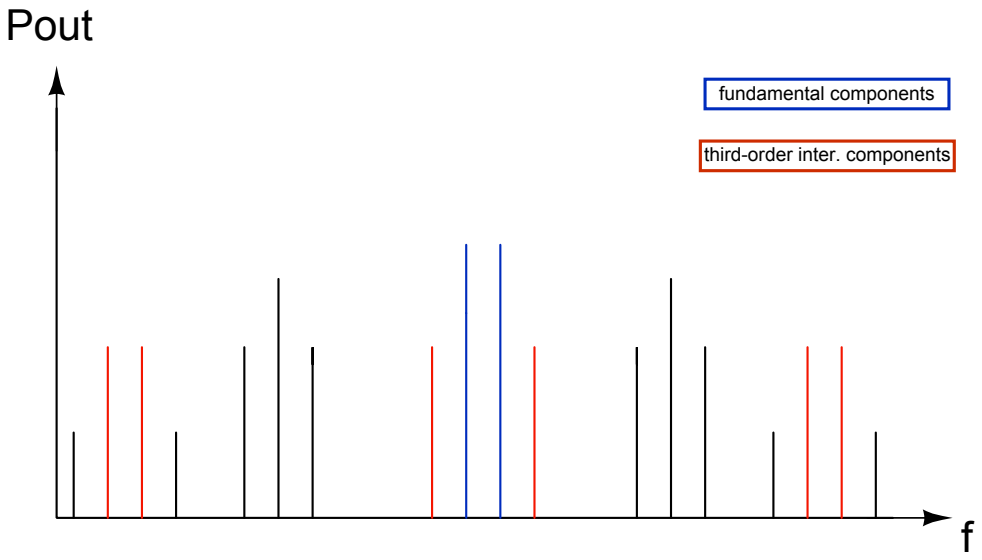

Figure 1.5: Fundamental harmonics and third order intermodulation components [9].

Third order intercept point

The point where both components coincide is the IP3, which has multiple correspondences with IM_3, making easier its computation.

$$IP_3 = \sqrt{\frac{4}{3}\frac{a_1}{a_3}} = V_{IN_{dB}} - \frac{1}{2}IM_{3_{dB}} \tag{1.13}$$

Compression point

An alternative, less accurate way to characterize distortion is the -1 dB compression point, the input/output referred power when the output voltage is compressed by 1 dB. This value can be approximately calculated from (1.3), indeed the compression is caused by the a_3 coefficient. Remembering that 1 dB of reduction is linearly a reduction to 0.122 :

$$V_{in,1dBc} = \sqrt{0.122\frac{4}{3}\frac{a_1}{a_3}} = \sqrt{0.122}IP_3 \tag{1.14}$$

In a dB scale the difference between IP3 and 1dB compression point is estimable of almost 10 dB, defining a wide used rule of the thumb.

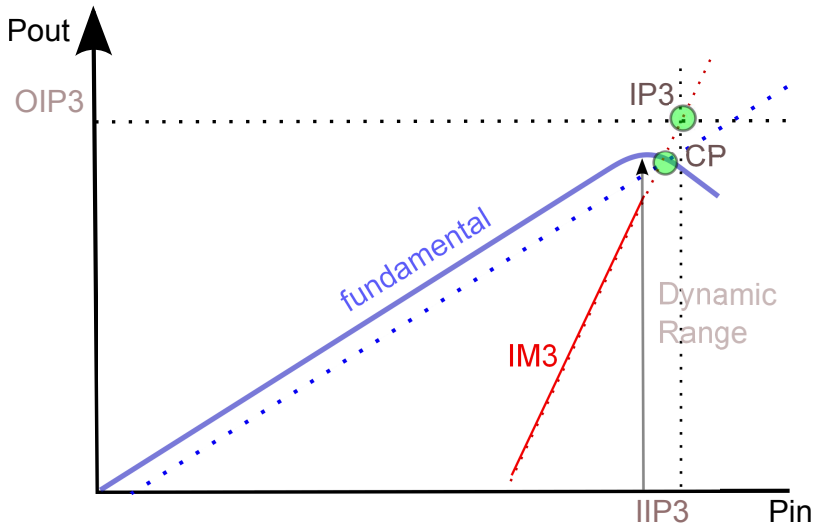

Figure 1.6: Fundamental curves explaining the intermodulation distortion.

1.6.3 Noise Figure and SNR

The noise is unavoidable, having a intrinsic nature related to the system physic. It is just predictable by using statistics, and it can be reduced and minimized refer-

ring to the signal carrying the information. For the reception, elaboration and the transmission of the signal, it is important to measure the relative weight of the noise in comparison with the information carrier, in fact an important figure of merit is the Signal to Noise Ratio, the ratio between the power of the signal carrying the information and the overall power of the noise.

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{1.15}$$

Noise in the time domain

Generally, the noise in the time domain can be described as statistic distribution of the instantaneous amplitude, since the noise derives from the superposition of an high number of elementary processes, in first approximation, uncorrelated, the distribution belonging to most of the case of the noise is the Gaussian distribution. The noise so has no first moment (equals to zero) and it is described just by the second moment, so by the root-main-square value and variance.

Noise in the frequency domain

Since the noise has to be referred with squared term in the time domain, the same has to be done in the frequency domain. Thanks to the Parseval theorem, the variance has to correspond the spectral power density of the noise:

$$\overline{x(t)^2_{\Delta f}} = \int_0^\infty S(f)df \tag{1.16}$$

The spectral power density is the Fourier transform of the auto-correlation function.

So for a small range of frequencies, $\Delta f \longmapsto 0$, it is possible to do an acceptable error considering:

$$S(f) = \frac{\overline{x(t)^2_{\Delta f}}}{\Delta f} \tag{1.17}$$

In the most of the cases of interest the spectral density of the noise power has a slope dependent on the frequency.

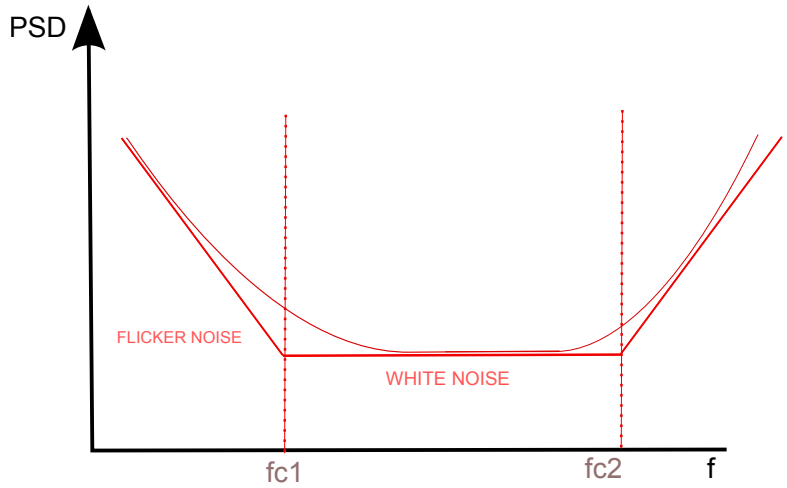

Figure 1.7: Usual power noise density spectre

At lower frequency the PSD has an $\frac{1}{f}$ behavior, then a flat slope and then it raises again directly proportional with the frequency.

The flat part, called white noise is delimited by the two noise corner frequencies.

Noise response in a linear network

Describing a circuit with the two ports model it is possible to determine the output power spectral density generated by the two ports.

$$S_{out}(f) = \left|G\right|^2 S_i(f) \tag{1.18}$$

Where S_{out} is the output spectral density power of noise. When the circuits has more than one source , if every source is uncorrelated with the other (assumption applicable with a small error to the most of the cases), the total spectral density is derived by:

$$S_{out}(f) = \Sigma_i S_i(f) \tag{1.19}$$

The Noise factor

The most common representation of the magnitude with which the system degrades the signal during the elaboration, is the Noise Factor and the related Noise Figure. This two figures of merit are based on the comparison between the total output noise due to a noisy input termination and the total output noise due to a noise-less input termination. This input termination can not be whatever the designer wants, but has to be a simply and general termination suitable for the case of interest. For the radio frequency systems the common termination is purely resistive with a resistance of 50Ω (75Ω for the Television applications).

Hence, the Noise Factor is defined as:

$$F = \frac{\text{Total output power}}{\text{Output Power due to the input termination}} = \frac{SNR_i}{SNR_{out}} \tag{1.20}$$

Finally, the Noise Figure is the conversion of F in a dB scale.

$$NF = 10log_{10}F \tag{1.21}$$

Noise sources

The physical noise sources assumed within the design noise analysis are:

- The thermal noise for resistors and MOSFETs, direct consequence of the fundamental mechanisms due to the energy state of a system.
- The flicker noise generated by the MOSFET, due the trapping-detrapping model describing the carrier fluctuation.
- The shot noise due to the flattening of the charge carriers, strictly related to its granular nature, acting a principal role in the bipolar transitors.

The thermal noise descends from the fundamental equations of the thermodynamic and from the energy quantization.

The resistive thermal noise source is observed as the flattening of the voltage among its terminal or the current flowing through it and it can be represented by:

$$\overline{V_n^2} = 4kTR \tag{1.22}$$

$$\overline{I_n^2} = 4KTG \tag{1.23}$$

A MOSFET transistor at the thermal equilibrium is, by its nature, a resistive device and its dissipation is associated to a correspondent thermal noise source between the drain-source channel, modeled as:

$$\overline{I_n^2} = 4kT\gamma g_m \tag{1.24}$$

The coefficient γ takes in account the relation among conductance of the channel and transconductance, dependent of the geometry and the structure of the device. In a real device with short channel that coefficient assumes, in first approximation, values between 1 and 2.

In terms of thermal noise a bipolar transistor comprehends a noise sources for each parasitic resistor at its terminal, dominant is the source due to the base resistor. Further, this kind of device has a shot noise current source between its collector emitter terminations due to the base current:

$$\overline{I_n^2} = 2qI_B \tag{1.25}$$

At low frequencies the flicker noise is the most dominant contribution generated by a MOSFET transistor. The equation governing the flicker noise is given by:

$$\overline{V_n^2} = \frac{k}{C_{ox}WLf} \tag{1.26}$$

The complete bipolar shot noise comprehends a factor of proportionality $\Gamma(f)$, describing the transmission time of the charge carrier on the collector and the emitter region, which typically $\Gamma(f) < 1$. For the analysis it is simply taken into account as white noise.

1.6.4 Scattering Parameters

Microwave are preferable measured in term of power quantities than voltage and current, because the measurement of high-frequency voltage and currents in the laboratory are difficult, when a power measure is straightforward [1].

The scattering parameters can be obtained through the measurement of power quantities. A general two-port network can be fully described by the ratio of the incident and reflected waves at the input and output port with different of termination.

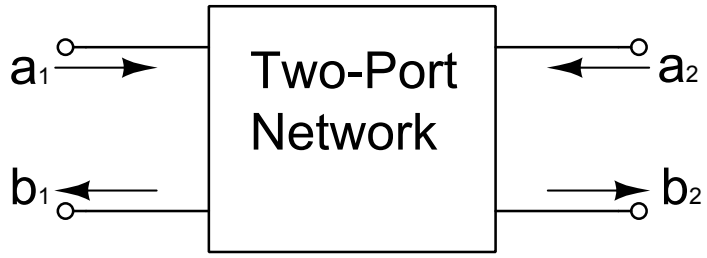

Figure 1.8: Two-port network model

The scattering matrix gives a relation the input and output waveform is given by:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1.27}$$

Where the scattering parameters are defined as:

$$S_{ij} = \frac{b_i}{a_j}\Big|_{a_2=0} \tag{1.28}$$

The parameter S_{11} is the ratio of the reflected and incident waves of the input port, thus it represents the quality of the input matching being the reflection coefficient of the input port.

Equally, the parameter S_{22} measures the accuracy of the output matching and it is the output port reflection coefficient.

The s-parameters are frequency dependent and they assume complex values, for the overall project they are expressed in units of dB.

$$S_{m,n_{dB}} = 20log|S_{m,n}| \tag{1.29}$$

In microwave designs these parameters gives important information about a two-port behavior as matching, gain, isolation and even stability.

Since one requirement of the specifications asks to ensure the opportunity to test the chip once in the laboratory with instruments providing a 100Ω differential termination, the input and output port of the system have to limit the reflection coefficient measured by S_{11} and S_{22} below of $-10dBm$, for the frequency range of interest.

$$S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} \tag{1.30}$$

$$S_{22} = \frac{Z_{out} - R_S}{Z_{out} + R_S} \tag{1.31}$$

1.6.5 Unconditional Stability

For baseband and radio frequency circuits a must to follow during the design is the stability control, no oscillations have to be propagated along the circuit, since they can deteriorate the performances of the system or even compromising the total behavior.

By observing into a wide range of frequencies, in the microwave circuits some topology that in a first approximation do not include feedback path, at high frequency when parasitic components introduce further signal branches, can bring back part of the signal to the input, becoming a feedback system potentially unstable.

Several are the method to check the stability of a system, and by using the scattering parameters an intuitive way to explain and define the stable condition is made by observing the output and input reflection coefficients system.

In fact, a system is assumed unconditionally stable if $S_{11} < 1$ and $S_{22} < 1$, for all passive load and source impedances.

A common measure of the unconditional stability can be made by using the Rollet's stability factor, which adds two useful scalar parameters:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{12}S_{21}} \tag{1.32}$$

$$B_1 = 1 + |S_{11}^2 - |S_{22}|^2 - |\Delta|^2 \tag{1.33}$$

Where $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$, and both parameters are frequency dependent, since they derive from the s-parameters.

The Rollet's stability factors confirm the stability when is verified that $K > 1$ and $B_1 > 0$.

Chapter 2

System Blocks

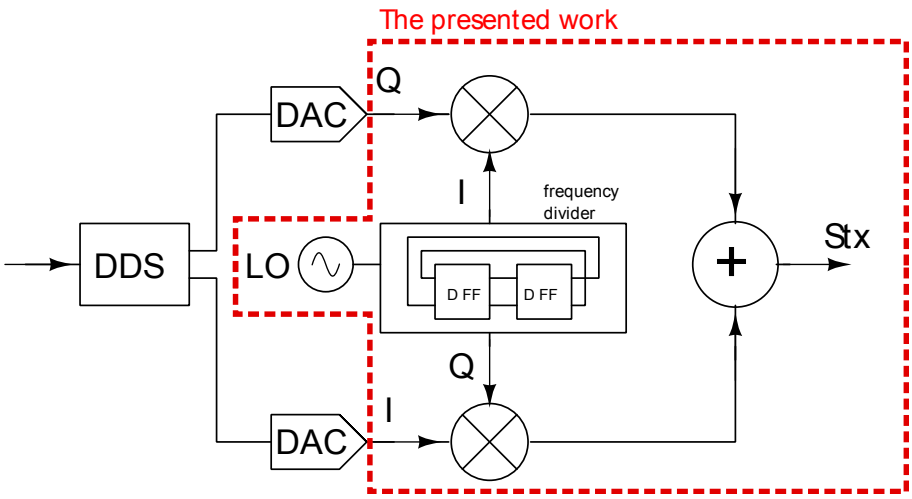

Figure 2.1: Wideband Upconverting IQ Modulator

2.1 IQ Modulator

Single Side Band (SSB) Mixer or also called sideband rejection mixer plays a key role in the modern RF communication systems. SSB mixers reduce system cost and

complexity avoiding the need for expensive extra filtering blocks, do not adding more stage to the mixer to perform the filtering, preserving the complexity of the whole system.

These mixers simplify up-converting modulation by separating the up-converted lower sideband (LSB) from the upconverted upper sideband (USB). This separation is made by a phase cancelation technique. Dually, the same is done by the Image Rejection Mixers performing the down-conversion and suppressing the unwanted image band.

The Sideband Rejection

The SSBM provides a single-sideband suppressed carrier output. The input of the system consists in a pair of LO signals and of BB signals. The requirements for the input stimulus, the two keys for a good sideband suppression in a IQ modulator are:

- Balanced IQ baseband inputs: equal amplitude and quadrature phase
- Balanced IQ LO signals feeding the two mixers composing the modulator.

No design is perfect, and a certain amount of imbalance of LO and baseband paths is expected.

A conventional double balanced mixer has, as core, a multiplication between two signals in the time domain. If the two signals can be represented as two sines:

$$s_1(t) = A\cos(\omega_1 t + \phi_1) \tag{2.1}$$

$$s_2(t) = A\sin(\omega_2 t + \phi_2) \tag{2.2}$$

The output produced will contains two harmonics: one at the sum of the two frequencies and the other at the difference of them.

$$p(t) = \frac{AB}{2}\Big[\cos(\omega_1 - \omega_2 + \phi_1 - \phi_2)t + \cos(\omega_1 + \omega_2 + \phi_1 + \phi_2)t\Big] \tag{2.3}$$

If two mixers are connected to each other, due to the difference of phase among the two paths, a LSB or USB output can be selected by choosing which in-phase port to drive with the base-band signal.

In fact, under ideal balanced conditions, the system work as follows:

- At the top mixer a $\sin(\omega_{BB}t)$ baseband signal and a $\sin(\omega_{LO}t)$ LO signal are mixed.
- The output of the top mixer consists of two terms:
  1. $\frac{1}{2}A\cos(\omega_{LO} - \omega_{BB})t$ in the lower sideband.
  2. $-\frac{1}{2}A\cos(\omega_{LO} + \omega_{BB})t$ in the upper sideband with 180 degrees of shift.
- If the bottom mixer is fed with a LO signal in quadrature of phase referenced to the previous, and a quadrature signal even for the baseband, the mixing result will consist in:
  1. $\frac{1}{2}A\cos(\omega_{LO} - \omega_{BB})t$ in the lower sideband.
  2. $\frac{1}{2}A\cos(\omega_{LO} + \omega_{BB})t$ in the upper sideband with no shift of phase.
- Hence, if the output of the two mixers is summed:
  1. The two lower sideband terms are added in-phase and produce the desired low-side output signal
  2. The two upper components are summed in out-of-phase and canceled.
- If the I and Q components are swapped, the upper sideband terms add in-phase, and the lower sideband terms are canceled.

2.2 Current Commutating Mixers

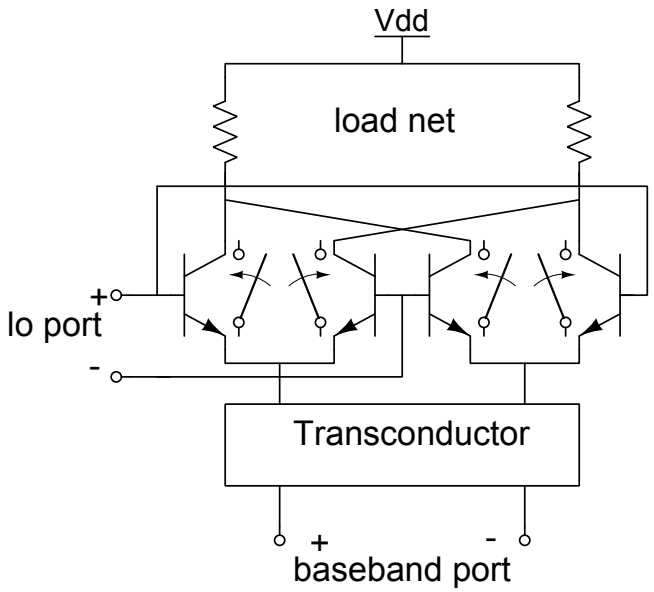

Figure 2.2: Model of a Gilbert Mixer [13]

To achieve high port isolation, gain conversion and low noise an active mixer topology is preferable than a passive mixer, despite it could achieve a better linearity. The double balance active mixer [13] here shown is based on a double crossed differential structure . It is composed by a switching cell driven by the LO signal and acts the modulation by steering the current provided by the driver transconductor stage, performing the conversion of the input voltage signal into a proportional current.

The switching cell is called also Gilbert Cell by the name of the creator of this structure. This topology is born to execute a precision multiplication of the currents flowing through it. Half of a Gilbert Mixer, called single balanced mixer, is here presented in the full CMOS version. The transistor M1 converts the input BB voltage to a current the upper differential pair M2-M3 steers this current to the left and to the right.

Then, this current flows reaching the output network composed by two resistors, converting it in the final modulated output voltage. With the complete structure the

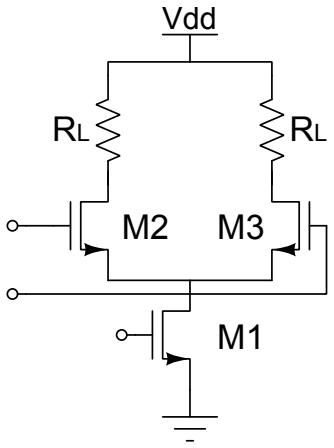

Figure 2.3: CMOS single balanced mixer

BB signal is available in differential form, if the transconductor provides differential output then the active mixer must be modified accordingly. The differential structure implies the advantage of the LO feedthrough suppression.

2.2.1 The Conversion Gain

In Fig.2.3 half a mixer is visible. M1 produces a small-signal drain current equal to $I_{ds_1} = g_{m1}V_{BB}$, if we assume the presence of an abrupt LO switching, the switching cell acts the multiplication of i_{BB} by a square wave commuting between 0 and 1, called $S(t)$.

$$I_1 = I_{RF}S(t)I_2 = I_{RF}S\Big(t - \frac{T_{LO}}{2}\Big) \tag{2.4}$$

By resolving the DC path starting and closing on the supply voltage comprehending the output voltage:

$$V_{out} = V_{DD} - I_1R_1 - V_{DD} + I_2R_2 \tag{2.5}$$

And ensuring the balance with $R_1 = R_2 = R_{out}$, the output voltage can be written

as:

$$V_{out} = I_{BB} R_D \Big[S\Big(t - \frac{T_{LO}}{2}\Big) - S(t) \Big] \tag{2.6}$$

The multiplication of a square wave toggling between 0 and 1 and I_{BB}, can be represented expanding the square wave by the Fourier series:

$$V_{out} = I_{BB}(t) R_{out} \Big[\frac{4}{\pi} \cos \omega_{LO} t .... \Big] \tag{2.7}$$

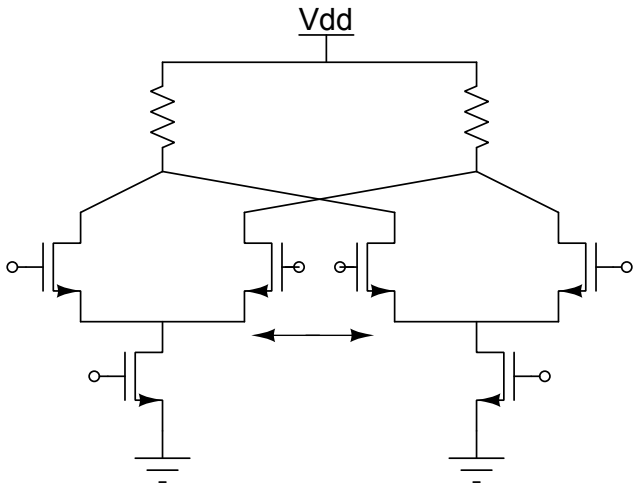

Figure 2.4: Interconnecting two single balance mixer it is possible to obtain the full differential network

Referring now, to the full differential version, the double active mixer if the baseband input signal is a sinusoidal wave form at the frequency ω_{BB}, the output signal, in first approximation, will be :

$$V_{RF} \simeq \frac{2}{\pi} g_m R_{out} V_{BB} \Big[cos(\omega_{LO} - \omega_{BB})t + cos(\omega_{LO} + \omega_{BB})t \Big] \tag{2.8}$$

So the voltage conversion gain is therefore equal to:

$$A_V = \frac{V_{RF_p}}{V_{BB_p}} = \frac{2}{\pi} g_{m1} R_{out} \tag{2.9}$$

The conversion gain is reduced by the non-ideal toggling computed by the switching cell. If the single-ended Lo waveform during ΔT is switching the state the total conversion gain is equal to :

$$A_V = \frac{2}{\pi} g_{m1} R_{out} \Big(1 - \frac{2\Delta T}{T_{LO}}\Big) \tag{2.10}$$

A bipolar double active mixer presents the same behavior and the analysis aforementioned can be applied even to it.

LO Feed-through Suppression

As seen previously, analyzing the single balanced mixer, the switching cell behavior has the consequences of to modulate the transconductor output current by a square wave. Being single-balanced, this topology has the defect to multiply the signal $V_{LO}\cos(\omega_{LO}T)$ to the current $i_{BB}(t)$, which contains even a DC component. The unwanted mixing carries out from the mixer a component at the same frequency of the LO, disturbing the overall transmission. This unexpected output, called LO Feed-through, can be avoided just using a useful feature provided by the double-balanced Gilbert Cell. In fact this topology has the advantage to provide as output the differences between the resistor voltages, which are equal to :

$$V_{p,n} = \pm\frac{2}{\pi}[\cos(\omega_{LO}t)]\Big[I_{DC} + g_m V_{BBp,n} cos(\omega_{BB}t)\Big] \tag{2.11}$$

The DC component is transported by both branches to the output, as their difference, comes out without LO component.

It is important to clarify that this condition is verified, just when a perfect balancing of the circuit is guarantee.

Port isolation

Ideal double-balanced mixer means the circuit is perfectly symmetrical without any parasitic effects. In fact the even harmonics of the baseband port are canceled due to the symmetry of the circuit. In this case the LO leakage is in the noise level so it is concluded that there is no LO feedthrough for an ideal double balanced mixer. In the real circumstance, there are no ideal conductors and connections, and they must be considered as resistors and capacitors. Parasitics and non-ideal effects, are the causes of the presence of unexpected components into the output when a real circuit is implemented.

2.2.2 Noise analysis

The main target of this project is to ensure the widest dynamic range (D.R.) achievable for the signal transmitted. The lower bound of the D.R. is bounded by the floor noise, thus, referring to the output, the smallest signal at the output generated by amplifying the noise. So the noise gives the limits to the sensitivity of the system, in fact a signal with an amplitude lower than the noise floor can not be distinguished and the system can carry information just having signals with higher amplitudes.

The enhancement of the noise floor and consequentially, of the D.R. could be done, principally by two ways:

- Using noise-less components or low noise architecture
- Using a post-process elaboration of the signal called optimum filtering.

In this up-converter system no inductors are inserted, to save the area of the circuit and further, no additional filtering will be implemented for this full-analog up converting block.

Noise in frequency translator systems

A frequency translator system is inherently noisy because noise is transferred from idler frequencies to the output. The input at base-band frequencies, carry an unwanted amount of noise and the frequency shifting, since spreads the input to multiple frequencies, will fold even the input signal PSD into multiple side-bands. The noise figure in a mixer is defined as the SNR at the baseband port (input) divided by the SNR at the RF port (output). In a typical mixer the output signal stands over over two output sidebands. The existence of a double sideband increases the difficulty of the noise figure computation, and this fact in the most of the case lead to defines two different NF definitions.

- When just one side-band carries the useful signal and the other side-band contains just the noise the noise figure computed over the output frequencies is called Single Side Band NF (SSB).
- When the signal exists on both side band frequencies, the NF is called Double Side Band (DSB).

If both sidebands have the same conversion gain through the system the DSB NF is 3 dB lower than the SSB NF.

Noise in Current-Commutating CMOS Mixers

Since frequency conversion means not a linear time invariant behavior, its noise could not be analyzed with conventional circuit techniques. Fast estimation of the noise performances is preferable because this capability facilitates design optimization and accelerated the design steps. The Gilbert cell contains a transconductance stage, which is, in the most of the cases, reported as a differential pair biased at a fixed operating point, anyway this analysis comprehends even more sophisticated kind of transconductors. The Gm-Cell is connected to feed with an output current the switching pairs driven by the LO signal.

It is easier and useful to consider half a Gilbert cell, shown in Fig.2.5. The noise

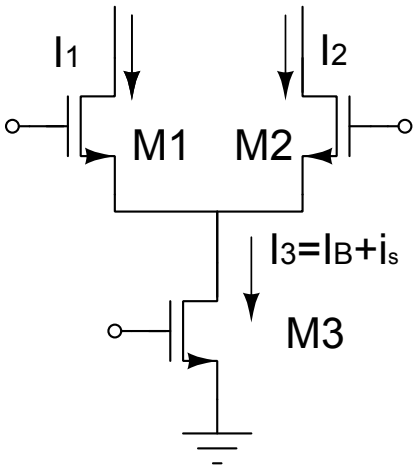

Figure 2.5: Single balance noise analysis

generated by the mixer has a periodically time-varying statistics, because the operating point changes periodically in the time domain and a random process whose statistics are periodic functions of time is called cyclostationary. In this case, the power spectral density is not just function of the frequency but being time variant is function even of the time.

A good approach to understand the mixer noise behavior is to compute the time average PSD and then evaluate the noise figure.

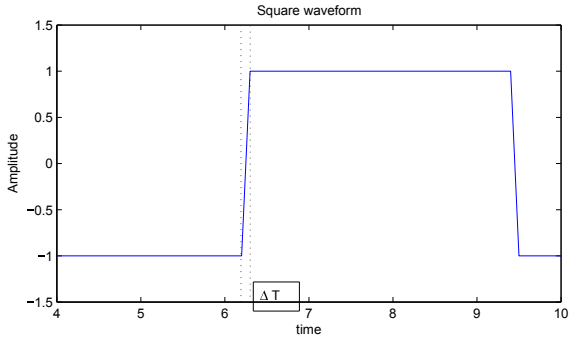

Figure 2.6: LO square waveform driving the switching cell

Considering the thermal noise generated in M1 and M2 assuming that they remain in saturation during the part of the period they are on. Neglecting capacitive effects when M1 or M2 is off the output current is determined by the transconductor output current and the switching block doesn't contribute on the output noise.

During the time interval ΔT, which bounds the commutation mode, both M1 and M2 are on and they contribute to the output noise.

IF the LO amplitude V_{LO} is high during the commutation, $\Delta \to 0$ this output noise added by the switches is negligible. The flicker noise generated by the switching cell is translated and folded around the DC but not around f_{LO} [8].

It is important to underline that the same analysis can be applied to a switching cell composed by bipolar.

Referring to (2.5), the transconductor delivers its noise current $i_n(t)$ to the output, modulated by the effects of the switches driven by the LO voltage.

$$i_{out_n} = i_s(t) \cdot p(t) \tag{2.12}$$

The time average PSD is:

$$S_{out}(f) = \Sigma_{n=-\infty}^{\infty} |p_n|^2 S_{N3}(f - nf_{LO}) \tag{2.13}$$

Considering the noise source as white for the whole baseband and if the LO has a large amplitude, the modulating signal can be expressed as a square wave form, hence :

$$\Sigma_{n=-\infty}^{\infty} |p_n|^2 = 1$$

$$N_{N3} = \Sigma_{n=-\infty}^{\infty} S_{N3}(f - nf_{LO})$$

Thus $S_{out}(f) = N_{N3}$.

The contribution of the different sidebands in the case of the square-wave form

approximation comes for the most percentage from the frequencies between $f_{LO} \pm f_{out}$, where f_{out} is the output frequency.

Finally, a large LO amplitude increases the conversion gain and reduces the noise contribution of the switching pair and the LO port. After a certain value, the conversion gain of the switching pair reaches its maximum value $\frac{2}{\pi}$ and the noise contribution of the switching pair reaches its minimum. Further, the PSD of the total mixer can be calculated with linear circuit techniques and the total SSB noise figure can be easily computed.

Finally, in an upconverting mixer the flicker noise related to the devices composing the transconductor is up-converted and translated at the beginning of the side-band of interest [23] .

2.2.3 Linearity assumption

Linearity is a very important issue because it brings many problems as gain compression or intermodulation distortion, phenoms measured by the second-order intercept point (IP2), third-order intercept point (IP3), and 1-dB compression point (P1dB). Therefore, it is a great challenge to achieve high linearity at low power and low voltage [9].

Into the implemented IQ Modulator the two main blocks consist of two mixers, which will act the phase canceling to provide the single sideband signal. It is clear that, these two blocks will limit the overall linearity of the system, and their design will set significantly the performances of the whole circuit.

Any mixer working as frequency converter bases its operation on a generic nonlinearity, consequently the output consists of a large quantity of components and only one is the desired compromising linearity performances and the quality of the mixing.

The employed double balanced active mixer offers as benefit the opportunity to preserve the linearity in terms of LO feed-through which, in case of a perfect bal-

ance of the structure, is totally supressed. The linearity is mostly dominant by the transconductance stage, therefore, it is very important to have a linear voltage to current transformation.

A common topology, acting a suitable V-I conversion in the active mixer can be, as widely seen, the differential pair (2.5).

This topology being differential does not present second-order distiortion. The differential output current $i_{od} = i_1 - i_2$ is twice the ac current of each transistor, and the relative current swing is given by:

$$i = \frac{i_{od}}{I_3} = \frac{v_{id}}{V_{GS} - V_T}\sqrt{1 - \frac{1}{4}\Big(\frac{v_{id}}{V_{GS} - V_T}\Big)^2}$$

For small value of $v_{id} < (V_{GS} - V_T)$, the square root can expanded as a power series:

$$\sqrt{1-x} = 1 - \frac{x}{2} - \frac{x^2}{8} - \frac{x^3}{16}$$

and limiting to the first term the differential output current becomes:

$$I_{odp} = \frac{I_3}{v_{GS} - V_T} \cdot V_{id} = gm_1 \cdot V_{Id} \tag{2.14}$$

Assuming the $\frac{V_{idp}}{V_{GS_3} - V_T}$ and i_p as output the coefficients of the nonlinear response are: $a_3 = -\frac{1}{8}$ and $a_1 = 1$.

Finally, the IM3 can be expressed as:

$$IM_3 = 3HD_3 = \frac{3}{32}\Big(\frac{V_{idp}}{V_{GS_3} - V_T}\Big)^2 \tag{2.15}$$

and

$$IP_3 = 4\sqrt{\frac{2}{3}}(V_{GS3} - V_T) \tag{2.16}$$

The IP3 of a common-source transistor rises with the overdrive, eventually reaching a relatively constant value.

2.3 Frequency division

The static frequency divider is a fundamental block for various applications, within mobile or satellite communication systems and multiple optic fiver systems. The high speed needed to achieve this duties is released by the Current Mode Logic frequency dividers, that unfortunately exhibits an high static power consumption.

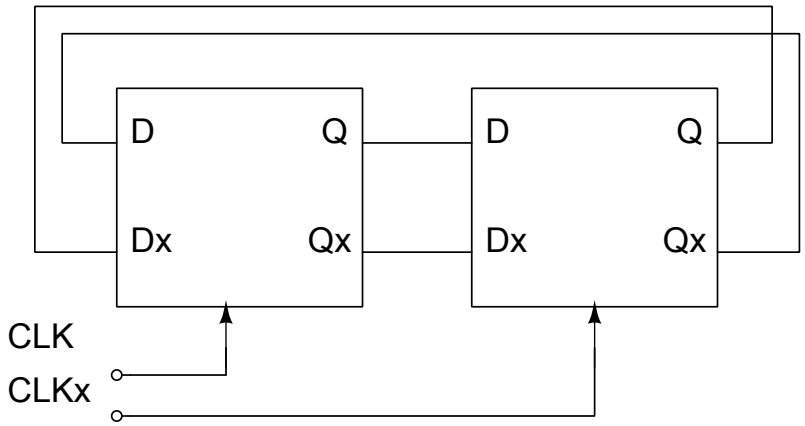

Figure 2.7: The frequency divider implemented by a master slave flip-flop topology

The common frequency divider is based on a flip-flop circuit architecture implementing a counter, as shown in Fig.2.7. This architecture is primarily a master-slave flip flop with a negative feedback. This circuit works by continually toggling the output state per each clock cycle. The mechanism effectively causes the output to commute between one and zero at the rate of half the input clock. In this way frequency division is achieved. The Fig.2.8 shows the clock pulses and the output from each of the latches explaining the circuit action. In high speed master-slave configurations the slave behaves as the dual of the master so that they can be both driven by a single clock. To do that, the divider utilizes two identical latches that are driven by complementary clocks CLK and CLKx.

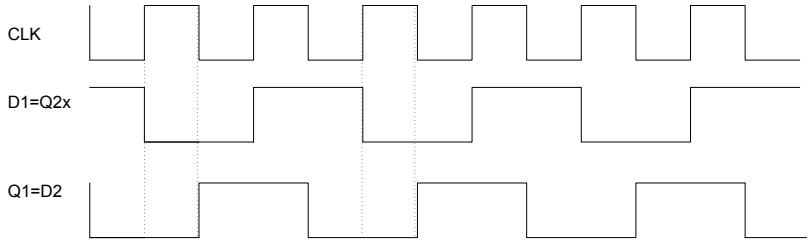

Figure 2.8: Clock and Flip Flop based divider operation

The high speed D flip flop are designed using current-mode logic circuits Fig. 2.9 . In the conventional CML latch topology, the track and the latch modes are determined by the clock signal, driving a second differential pair. When the signal CLK is 1, the circuit operates in the tracking mode, where the current from T7 flows entirely through the tracking differential pair T1 and T2, thereby allowing V_{out} to track V_{in}. During the latch-mode, the signal V_{CLK} is held low and the tracking stage is disabled. Further, the latch pair is enabled storing the logic state at the output. This topology is suitable to work at frequencies of various GHz.

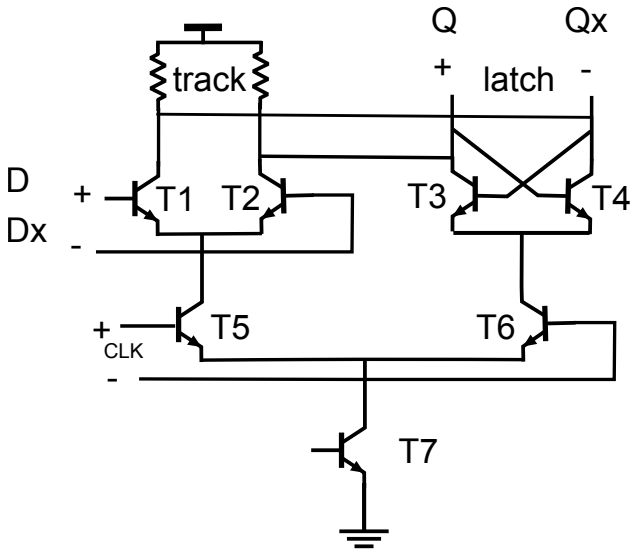

Figure 2.9: CML D Flip Flop

2.4 WideBand spurs issues

As repeatedly observed in the previous sections, the Gilbert Mixer can be used as a flexible tool to achieve the frequency translation, thanks to some assumptions making it easily analyzable, even if it is strictly based on a nonlinear time variant system. If noise and linearity designs are closely related to the transconductor behavior, neglecting further parts of the topology, is direct consequence of the hard switching acted by the Gilbert cell. An hard driven commutation is verified if the LO signal assumes a square waveform, with negligible toggling time. By observing the system performances in a wideband range, it is important to take into account the spectre belonging to the square waveform. In fact, it is composed by an infinite series of odd harmonics, responsible of a related series of wanted and unwanted mixing, with the baseband signals. The unwanted mixing, even if has a lower harmonic amplitude, degrades the linearity of the IQ Modulator, adding spurs upon the output band of interest with the lower LO signal frequencies: for instance, it is clear how a 3GHz LO signal, can produce a further mixing close to the 9GHz harmonic disturbing the overall transmission. So it is useful to fix these further spurs, avoiding the addition of extra components but rather reusing blocks already available. A filterless polyphase modulator can be performed by a parallel wideband mixers interconnection.

2.5 Multipath Polyphase Filtering

As mentioned , unwanted spectral components can be canceled by a polyphase multipath technique. The basic idea is to split an input signal into N paths [10] . Each branch contains a phase shifter followed by a nonlinear circuit and an additional phase shifter. The nonlinear circuits are identical, on the other hand, the phase shifts differs for every path. All the output of the different branches are added to get the output signal.

This structure allows a constructively addition of the wanted signal if the desired

signal paths have equal phases before the summing node. The undesired signals (results of various distortion products) should have a different phase at the end of every path and the phase differences between the paths should be chosen in such a way that the unwanted signals are canceled.

Harmonics suppression technique

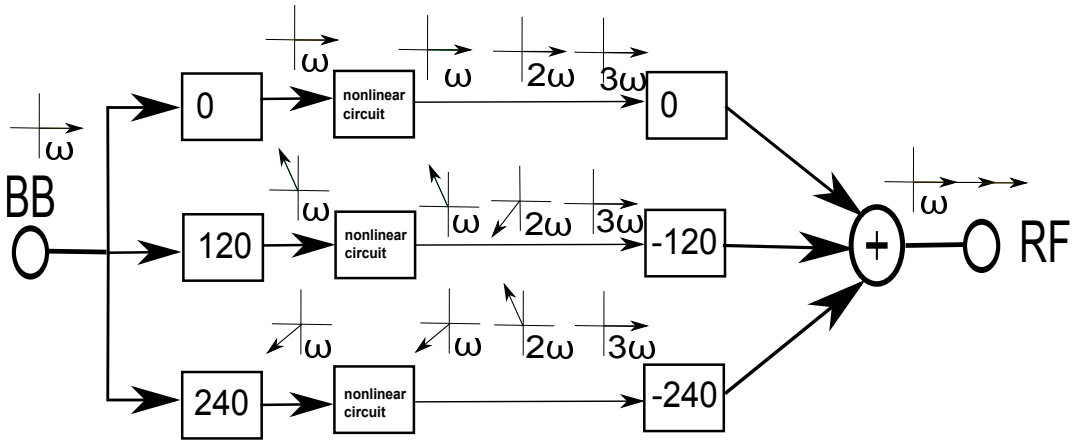

Figure 2.10: Multipath Polyphase harmonics suppression technique [10] .

By combining the phase shifts of all the phase shifters into the vector:

$$\underline{\varphi} = [\varphi_1, \varphi_2, ..., \varphi_N] \tag{2.17}$$

All the phase of the signals after the first phase shifters are $\underline{\varphi}$, and the nonlinear circuits generates harmonics of these signals.

By assuming that the circuits are weakly nonlinear, and if all the nonlinear circuit input can be represented as $x_i(t) = \cos(\omega t + \varphi_i)$. It is easily demonstrable [10] how the fundamental harmonic component, before the last phase shifter, is a scaled version with the same phase of the input $x_i(t)$, but the unwanted components cause by the nonlinear circuit, having a frequency multiple of the fundamental, have phases following the relation:

$$\underline{\varphi}_{nonlinear_n} = n\underline{\varphi} \tag{2.18}$$

The phase shifters after the nonlinear circuits set the phase of the desired signal back to zero, consenting the constructive addition. The higher harmonics take the same phase shifting, and their phases before the adder become:

$$\underline{\varphi}_{s,n} = (n-1)\underline{\varphi} \tag{2.19}$$

These components can be canceled. Indeed, by setting the first phase shifting equidistant between each paths:

$$\underline{\varphi} = [0 \cdot 360/N, 1 \cdot 360/N, ..., (N-1) \cdot 360/N] \tag{2.20}$$

then the (2.19) can be rewritten as:

$$\underline{\varphi}_{s,n} = \frac{n-1}{N}[0 \cdot 360/N, 1 \cdot 360/N, ..., (N-1) \cdot 360/N] \tag{2.21}$$

This equation shows that whenever $n = p \cdot N + 1$, the phase in every path will be a multiple of 360° leading to constructive addition. It can be shown that in all cases when $n \neq p \cdot N + 1$, the phases are distributed equidistantly over 360°, leading to cancellation.

Phase of $\underline{s}$ N	$\underline{0}$	$\underline{\pm\varphi}$	$\underline{\pm 2\varphi}$	$\underline{\pm 3\varphi}$	$\underline{\pm 4\varphi}$	$\underline{\pm 5\varphi}$	$\underline{\pm 6\varphi}$	$\underline{\pm 7\varphi}$
2		C		C		C		C
3		C	C		C	C		C
4		C	C	C		C	C	C
5		C	C	C			C	C

Table 2.1: Table indicates whether harmonics are canceled ("C") or not (blank), depending on their phase from eq. (2.19) (columns) and number of path rows(N)

Table (2.1) can be used to see if a harmonic with this phase is canceled or not by a certain number of paths.

Canceling of Intermodulation Products

The canceling of intermodulation products can be analyzed in the same way as the canceling of the harmonics. It can be shown [10], that an intermodulation product at $k\omega_1 + m\omega_2$, with k and m positive or negative, will have a phase of $(k+m)\cdot\underline{\varphi}$, after the nonlinear circuits and a phase of $(k+m-1)\varphi$ before the adder. Therefore, if the n^{th} harmonic is canceled, even the intermodulation products at $k\omega_1 + m\omega_2$ with $k+m=n$ will be canceled.

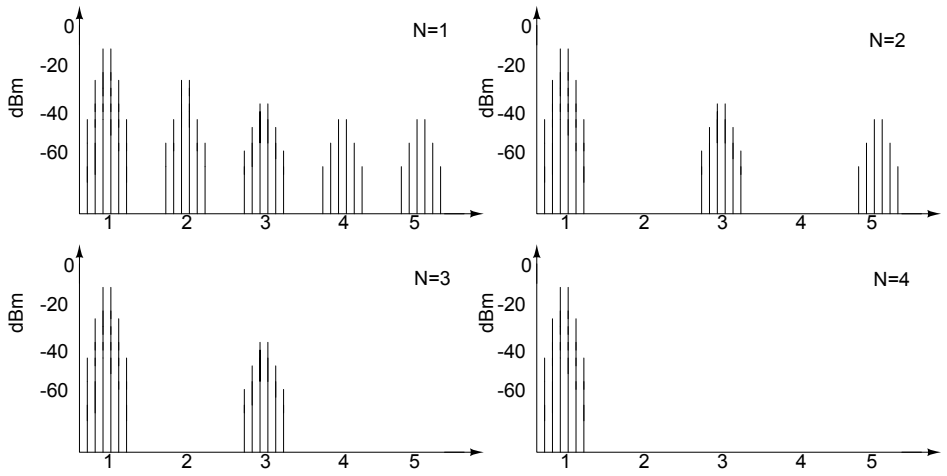

Figure 2.11: Output spectra of a polyphase multipath circuits several paths (two-tone test) [10] .

2.6 Multipath Polyphase Mixer

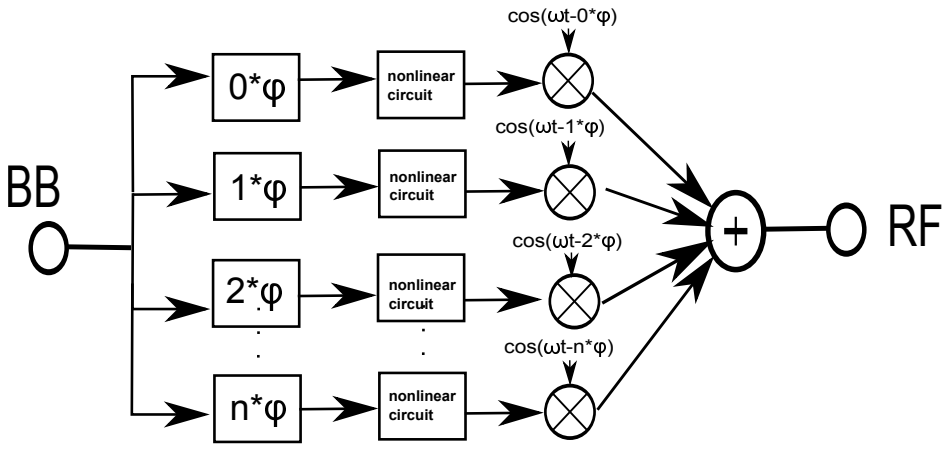

Figure 2.12: Multipath Polyphase Mixer [10] .

An important point to guarantee a wideband perfomance, is to ensure a constant phase shifting over all band. After the nonlinear circuit the band of interest is greater than before it.

RLC filters, often implemented as phase shifters, but present difficulties in order to work over a wide band spectre with a constant phase shift.

The already discussed Gilbert Mixers, can in principle implement the needed phase shifters, making an active wideband filtering. The mixer will introduce even the required frequency shifting, completing the IQ Modulator with polyphase path structure.

Finally, the harmonics of the LO signal will also be mixed, as previously anticipated, gives an extra spectral components that can be included to the undesired harmonics to delete.

It is possible to create a straight forward correspondence of what already seen in matter of delectable harmonics with all spurs that an active mixer can produce. If the desired signal is in the upper sideband, while a positive n means that the n^{th} harmonic is in the upper sideband and a negative n means the the n^{th} harmonic is

in the lower sideband, (2.19) changes to :

$$\underline{\varphi}_{s,j,n} = \begin{cases} (n-j)\cdot\underline{\varphi}, & n \geq 0 \\ (-n+j)\cdot\underline{\varphi}, & n < 0 \end{cases} \tag{2.22}$$

So, to delete a spectral component at $j\omega_{LO} + n\omega_{BB}$ with at ω_{BB} the input baseband signal and $j\omega_{LO}$ an undesired LO harmonic component, is necessary to create a polyphase multipath mixer of N paths, with N verifying:

$$n = j + p \cdot N \tag{2.23}$$

n / j	**-5**	**-4**	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**	**4**	**5**
0	$5\underline{\varphi}$	$4\underline{\varphi}$	$3\underline{\varphi}$	$2\underline{\varphi}$	$1\underline{\varphi}$	0	$1\underline{\varphi}$	$2\underline{\varphi}$	$3\underline{\varphi}$	$4\underline{\varphi}$	$5\underline{\varphi}$
1	$6\underline{\varphi}$	$5\underline{\varphi}$	$4\underline{\varphi}$	$3\underline{\varphi}$	$2\underline{\varphi}$	$-\underline{\varphi}$	0	$1\underline{\varphi}$	$2\underline{\varphi}$	$3\underline{\varphi}$	$4\underline{\varphi}$
2	$7\underline{\varphi}$	$6\underline{\varphi}$	$5\underline{\varphi}$	$4\underline{\varphi}$	$3\underline{\varphi}$	$-2\underline{\varphi}$	$-\underline{\varphi}$	0	$1\underline{\varphi}$	$2\underline{\varphi}$	$3\underline{\varphi}$
3	$8\underline{\varphi}$	$7\underline{\varphi}$	6	$5\underline{\varphi}$	$4\underline{\varphi}$	$-3\underline{\varphi}$	$-2\underline{\varphi}$	$-\underline{\varphi}$	0	$1\underline{\varphi}$	$2\underline{\varphi}$
4	$9\underline{\varphi}$	$8\underline{\varphi}$	$7\underline{\varphi}$	$6\underline{\varphi}$	$5\underline{\varphi}$	$-4\underline{\varphi}$	$-3\underline{\varphi}$	$-2\underline{\varphi}$	$-\underline{\varphi}$	0	$1\underline{\varphi}$
5	$10\underline{\varphi}$	$9\underline{\varphi}$	$8\underline{\varphi}$	$7\underline{\varphi}$	$6\underline{\varphi}$	$-5\underline{\varphi}$	$-4\underline{\varphi}$	$-3\underline{\varphi}$	$-2\underline{\varphi}$	$-\underline{\varphi}$	0

Table 2.2: Phase of the n^{th} harmonic of input signal mixed with j^{th} harmonic of LO signal just before addition in a polyphase multipath circuit with mixers as second phase shifters

As before, the intermodulation distortion products, can be deleted including them in the previous equation as $k + m = n$.

Chapter 3

Design

3.1 Design Overview

The targets of this project (See table 1.1) are directed to achieve a dynamic range as wide as possible for the upconverting IQ Modulator, hence the noise generated by the system, degrading the sensitivity of the mixing at lower output and input powers, has to be properly limited. The output referred interception point and the relative compression point needs to be increased, allowing an high output power to be produced meanwhile the input and output voltage follow a linear trend defined by the conversion gain.

The degradation of the signal to noise ratio strongly depend on the noise produced by the input port, represented by the transconductor stage of the two mixers implemented. The design of them has to be conveyed toward the lower possible noise generation. Equally the voltage to current conversion employed by the same stage, needs to reduce the production of distortion, which has the straight forward consequence to generate and spread spurs over the output frequency range getting worse the linearity of the transmission. Moreover, the mixer are followed by an output buffer, which has to conserve the linearity of the mixing avoiding additional spurs

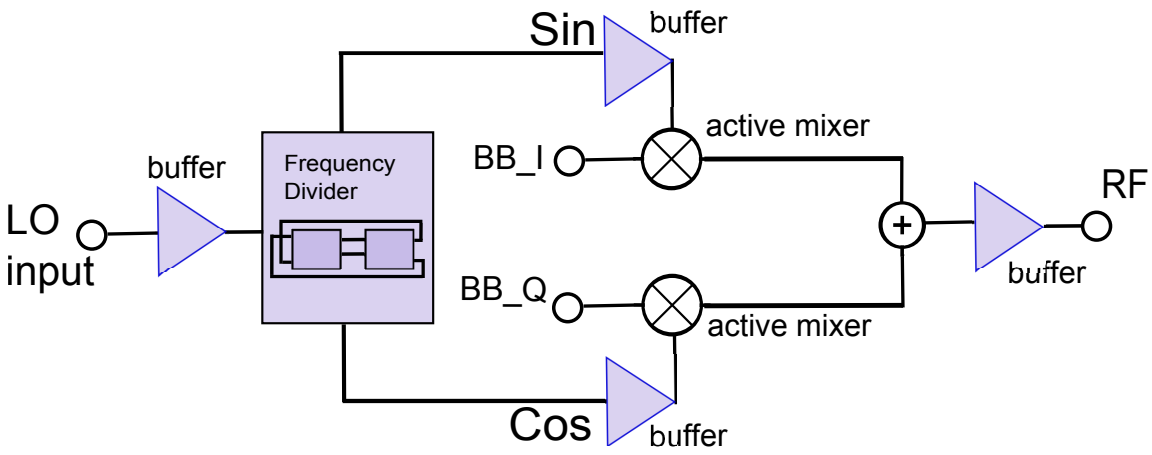

Figure 3.1: The complete IQ Modulator block chain

injection, but not decreasing the third order intercept point referred at the output port.

The active mixer of the upconverter needs to be interfaced with DACs, delivering a quadrature baseband signal in the current domain, a 50Ω input impedance provided by the transconductor can avoid to add an extra DAC interface to match the two blocks.

At the output port a differential 100Ω impedance needs to be provided, allowing measures with the standard radio-frequency laboratory equipment.

The core of the system is the active mixer, defining most of the proprieties aforementioned. Having the opportunity to use a SiGe BiCMOS technology two macro-topology of mixers can be considered:

- **Active mixer with bipolar transconductor** : The presented mixer, is composed by a bipolar transconductor simpled made by a differential pair.
  - **Pros:**
    - A bipolar transconductor can achieve an high transconductance.
    - The thermal noise produced by these devices is smaller than the MOS-

FET counterpart.

  - **Cons:**
    * A bipolar device offers a linearity directly proportional to the current flowing trhough it. To enhance the linearity of a bipolar differential pair is possible to place degeneration resistors, but decreasing their gain, increasing the noise and spending an higher current to bias it [15].

- **Active mixer with CMOS transconductor** : Since the frequency translation to assolve is the upconverting, the input signal is located at the baseband frequency range and so even no high speed devices can employ the voltage to current conversion. Due to that a MOSFET transconductor is taken into account
  - **Pros:**
    * A MOSFET transistor is a device with a greater intrinsic linearity than a bipolar, proportional to the overdrive voltage instead of the biasing current.
    * A MOSFET differential pair provides an higher IP3 than the bipolar counter part even without degeneration [21] .
  - **Cons:** MOSFETs are more noisy than bipolar.

In both solutions here shown, the switching cell is composed by two cross coupled differential pair implemented by bipolar technology, indeed the bipolar switching cell fits with the input LO frequency request ensuring , furthermore, a really high port isolation.

If a technique to reduce the noise figure is implemented the MOSFET transconductor

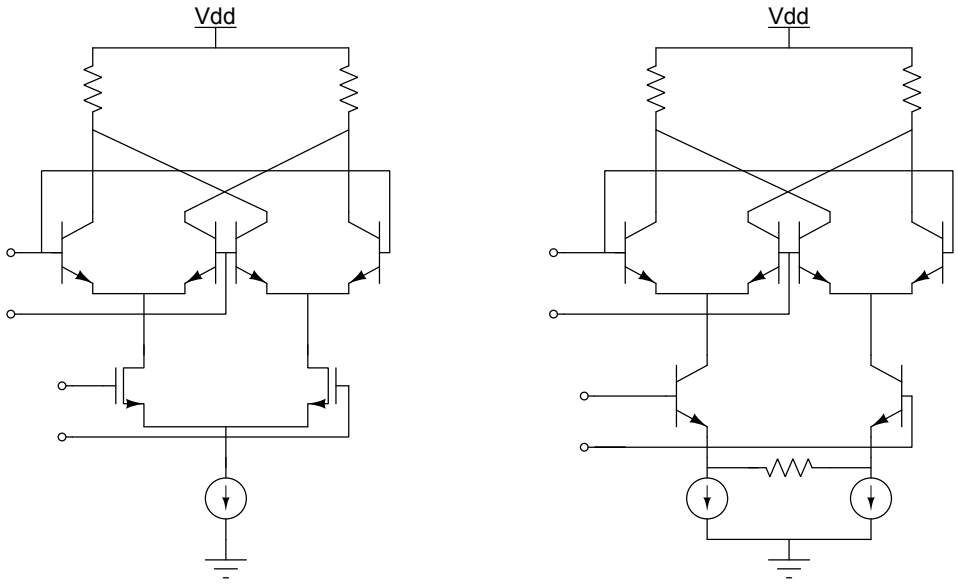

Figure 3.2: Compared structures

version becomes the most attractive solution, by taking in advantage of their intrinsic linearity proprieties. Due to that the presented design is based on full BiCMOS mixing topology directed to ensure the specified target performances.

3.2 The buffers

3.2.1 The input buffer

The input buffer, has to interface the local oscillator with the frequency divider. The input port of this stage is AC coupled, placing two coupling capacitors in series to the input termination. Moreover, to avoid any kind of reflection and oscillation to its port, ensuring the maximum power transfer from the input source to the stage, the input matching has to be achieved. The input voltage source provides frequencies in a wideband, so the match needs to be verified for the whole band.

At the input a couple of bias resistor are placed in parallel to the common collector

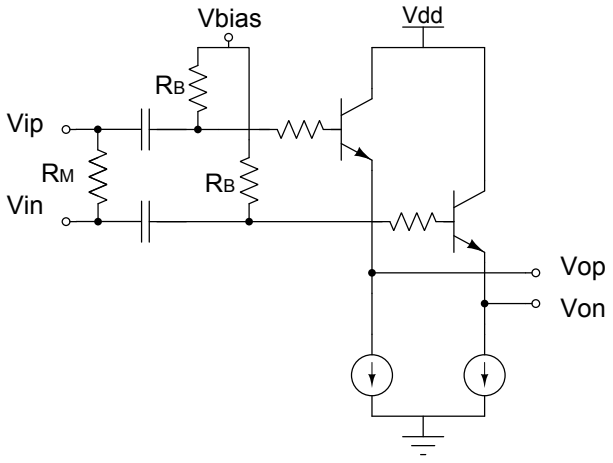

Figure 3.3: Emitter Follower

amplifiers and biased at the proper voltage V_{bias}. R_M is the matching resistor, in fact being in parallel with the input impedance of the common-collector amplifier $r_\pi(1 + g_m R_{out_{mirror}})$ and the biasing resistors R_B, having both couples an high resistance value, it is the predominant and describe the input impedance. Due to that, the differential port is matched when $R_M = 100\Omega$. The couple of series capacitors connected at the input, complete the ac biasing. On the other hand the intrinsic output buffer resistance is given at low frequencies by:

$$R_{OUT} = \frac{1}{g_m}$$

.

The biasing network is implemented by a couple of current tail mirrors, that offers a stable current and an high output resistance seen from its collector. This impedance is higher, when these current mirrors contain a degeneration resistance which increases the r_o by a factor equals to the loop gain $T = (1 + g_m R_E)$.

The output load of this circuit is the input impedance of the frequency divider. At the frequencies of interest it has a resistive predominant value slightly below $1k\Omega$. The input signal applied has a differential 3dB power ($\simeq 600mV$). Due to this values

not an high current is needed to bias the stage, and this and it is set to $2mA$ for each branch.

3.2.2 Wideband Input Matching

The input matching has to be guaranteed over a range of frequencies up to $f_{MAX} = 2f_{LO_{MAX}} = 30GHz$, since the local oscillator driving the frequency divider, works at the double of the RF frequency commuting the active mixer.

This limit is strictly correlate with the parasitic components nested in the couple of emitter followers. At high frequencies the input impedance becomes:

$$Z_{in} = \frac{r_\pi}{1 + sr_\pi C_\pi}(1 + gmR_L) \tag{3.1}$$

C_π is the principal contributor of the degradation of the input impedance seen at the base of the emitter follower. Indeed, at higher frequency the impedance becomes purely capacitive, and its low value, connected in parallel with input impedance, increases the total reflection at the input port. By limiting the geometry size of the transistor it is possible to get lower parasitic effects due to C_π, achieving the required S_{11} even at high frequencies.

Stability check

The emitter follower topology, having the output taken from the emitter of the common collector amplifier and the input applied to its base, suffers of a tendency to oscillate. Carefully watching its structure, considering layout parasitic including load capacitors and series inductors, its structure reclaims the widely known topology named Colpitts Oscillator.

The parasitic inductance is negligible when the wire connecting the input to the base of the bipolar amplifier is shorter. The capacitive divider composed by C_π and

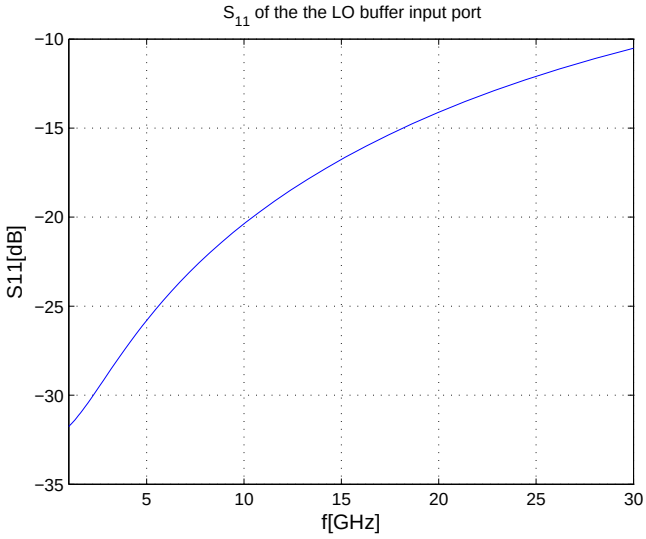

Figure 3.4: The S_{11} seen at the input port of the buffer

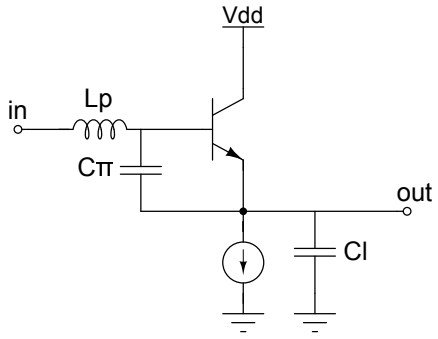

Figure 3.5: Intrinsic Colpitts oscillator

the sum of the capacitors nested to the output node C_L, if preceded by an inductor generates an unwanted oscillation.

All these parasitic components, get the input buffer oscillating close to the frequency :

$$f_o = \frac{1}{2\pi\sqrt{L_p \frac{C_\pi C_L}{C_\pi + C_L}}}$$

The unconditional stability is checked up to 200GHz, a wide band range including even f_o.

The design has to consider and fix this issue, indeed to reduce it, it is possible during the layout, to decrease the input track connecting the local oscillator to the input of this buffer, reducing the parasitic inductor, but this solution is not always available and does not ensure the unconditionally stability robustness.

A more efficient way to the avoid this problem is represented connecting in series at the base of the buffer a resistor, suppressing the Q of the inner tank.

Furthermore, by observing the stability of the circuit even without inductors, oscillations can occur even not including any parasitic tank. An additional analysis can explain how it is possible, concerning the relation between instability and S-parameters. In a two-port by considering the reflection coefficients, seen from the input and the output port and represented by S_{11} and S_{22}, if they assume an absolute value greater than one, the injection of a signal in the relative port can cause an unstable behavior of the circuit. This situation is verified when:

$$\frac{Z_S - Z_{IN}}{Z_S + Z_{IN}} > 1$$

If $Z_S = R_S$ this expression can be verified when the input impedance assumes negative values. Indeed by considering the parasitic capacitance, already objects of discussion, the input resistance seen looking at the base of the common-collector transistor can assume negative value [3].

As already seen, this negative resistor can get positive just with an additional resistor

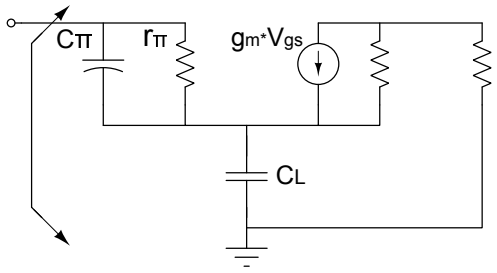

Figure 3.6: Input impedance small signal model

connected in series at the base increasing R_b.

The trade-off of a supplementary series resistor, is represented in additional losses, but the magnitude of this leakages cause negligible consequences for the overall performances of the system, reminding that the input power of the local oscillator is set at the standard of 3dBm, largely sufficient to drive the frequency divider.

3.2.3 The output buffer

The summation of the current signals, produced by the two active mixers has to be delivered to the external environment through a buffer interface. Most likely the output buffer will be connected to a further power amplifier, then connected to a transmitter antenna. So, the output buffer has to deliver the modulated signal providing a matched output impedance of 50Ω.

On the other hand this circuitry has an important role for the linearity issue. In fact, the OIP3 can be computed as follows:

$$OIP3 = P_{out_{[dBm]}} - IM3_{[dB]}\frac{1}{2} = P_{in_{[dBm]}} + Gain_{[dBm]} - \frac{1}{2}IM3_{[dB]} \qquad (3.2)$$

To set an high OIP3, it is important to guarantee along the system, an adequate gain to the fundamental output harmonics. Moreover, the specification to ensure the output impedance matching causes an unavoidable loss of 3dB. On the other hand, increasing its voltage gain, means to introduce distortion decreasing the linearity of

the whole Modulator.

Two solution are here compared:

- An emitter follower topology.
  - **Pros:**
    - By definition a voltage buffer, it provides high input impedance and low output impedance, thanks to the inner feedback composed by the emitter resistance.
    - The same feedback decrease the distortion.
  - **Cons:**
    - It attenuates the input signal: indeed, due to its effective transconductance.
    - The bipolar technology provides an huge transconductance, its output impedance is :$\frac{1}{g_m}$ and is averagely lower than the required matching impedance: 50Ω.

      A further series resistance has to be added to the output terminal increasing the losses, degrading the output third order intercept point
- A degenerated differential pair:
  - **Pros:**
    - Partially degenerated, it can a quite high input impedance and a and a good linearity, depending on the degeneration resistor .
    - The load resistor connected at the collectors, when assumes a low resistance, it is the output impedance. This topology easily provides the required matched output
    - The moderate degeneration allows the opportunity to achieve a voltage gain.

- **Cons:**
  - Setting an high linearity means to provide an higher biasing current flowing through the transistors

The current budget does not suffer of strict limitations, hence to preserve linearity at the cost of current and additional design steps, a differential pair with degenerated emitter is implemented. To achieve an OIP3 greater than 0 dBm, it is fundamental to ensure the suitable output swing of the amplifier. The compression has to appear when the output has already reached the 0 dBm, thus, almost a differential 440mV zero-peak voltage on a 100Ω load resistor. In a single ended point of view, the output amplifier has to guarantee a linear behavior producing signals with $\simeq 225mV$ of amplitude. Due to the output matching, the attenuation has to be counterbalanced with a linear gain of 2. All these conditions can be satisfied, as said, with the cost of an higher biasing current, furthermore, increasing the I_B the layout scales proportionally. The gain of this stage is given by:

$$\frac{v_{out}}{v_{in}} = -R_L \cdot g_{m_{eff}} = -R_L \cdot \frac{g_m}{1 + g_m \frac{R_D}{2}} \tag{3.3}$$

If the previous equation is set equal 2 and the output resistance is 50Ω, the effective transconductance is :

$$g_{m_eff} = 2/50\Omega = 40mS$$

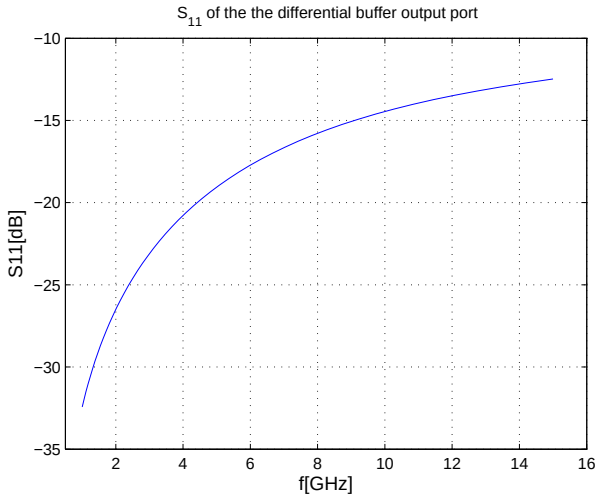

Figure 3.7: The S_{11} computed by injecting a signal to the output port of the buffer with a 100Ω differential termination

The rule of thumb which says that the linear span of linear operation is increased of an amount equals to $I_B R_D$, hence, if the current it is chosen $10mA$, the degeneration resistor has to be : $R_D = 44\Omega$. Hence, the left transconductance can be defined as: $g_m \simeq 210mS$.

Stability check

The analysis done concerning the stability of the input buffer, can be here applied with the proper changes. By observing the small signal model of the buffer, the input impedance can suffer of the presence of a negative input resistor considering the capacitance added by the current tail mirror to the emitter of the transistor employing the buffer. As already discussed, this issue can be fixed with an additional series resistor placed at the base of the amplifier, bringing the input resistor to a positive value. On the other hand, the series resistor causes losses, and a further decreasing of the signal at the output port can strongly degrade the output IP3. To limit these losses it is preferable to reduce as possible this further resistor. One solution to preserve stability and the integrity of the signal is by placing an additional

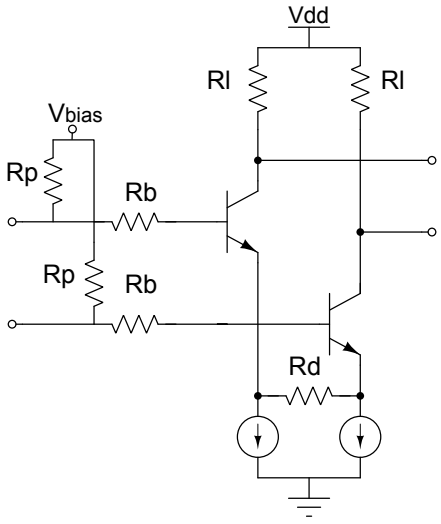

Figure 3.8: Output Buffer

parallel resistor to the input port.

A further parallel resistor interfacing an impedance with negative real part [3]:

$$Z_{IN} = \frac{r_\pi}{1 + sC_\pi r_\pi} + (1 + g_m \frac{r_\pi}{1 + sC_\pi r_\pi})(R_E + \frac{1}{j\omega C_L})$$

At high frequencies the input impedance can be represented as the series of a negative resistor $R_N = \frac{g_m}{-\omega^2 C_L C_\pi}$ followed by a series capacitor.

Considering $Z_{IN} = R_N + jX_N$ where both R_N and X_N have a negative sign, by placing a parallel resistor to the net the value of the input impedance seen at input terminal becomes:

$$R_P||(R_N + jX_N) = (...) = \frac{R_P(R_N + jX)(R_P + R_N + jX)}{(R + R_N)^2 + X_N^2} \tag{3.4}$$

The previous equation assumes a positive value when:

$$R_P(R_P R_N^2 + R_N^2 - X^2) > 0 \tag{3.5}$$

Hence, the input impedance is represented by a parabola with negative concavity assuming positive values when the parallel resistor is $0 < R_P < X_N^2 - R_N(R_N - 1) = R_P^*$.

So in this range of resistance even just placing a parallel resistor is possible to make positive the total resistance and to avoid the instability. By the help of a small series resistor the parallel auxiliar resistance can be set to preserve the total input impedance, that in the case of a buffer has to high, and even the stability. In this case R_P has been set to $1k\Omega$,

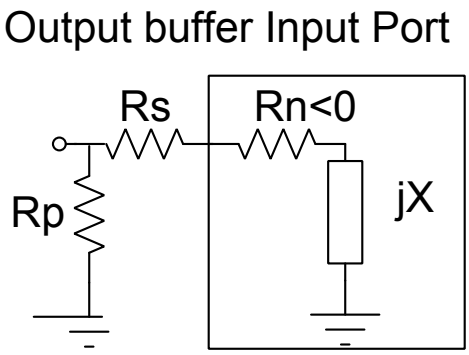

Figure 3.9: Output Buffer

3.3 The mixer

In this section is analyzed and designed the active mixer, core of the system. Its design is directed to enhance the dynamic range of the output signal, in order to have a clean transmission as good as possible.

3.3.1 The transconductor

The implemented transconductor is based on a differential version of a noise canceling topology of a wideband low noise amplifier [4]. This circuit, being a inductorless-topology, achieves a low area effort furthermore, the provided technology ensure the

wide bandwidth. A further feature is needed: the input impedance has to be matched overall the base-band frequencies, making sure the possibility of testing the chip with 50Ω standard equipment.

An inductorless low noise amplifier with a flexible input impedance could be implemented using a shunt feedback amplifier [22] .

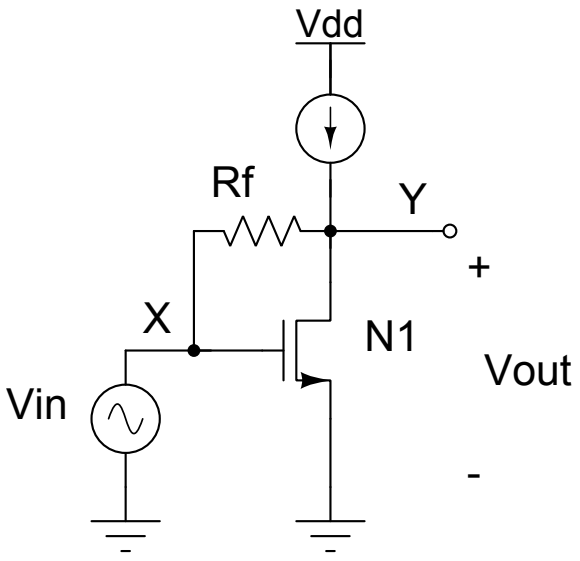

Figure 3.10: Shunt feedback amplifier

The Shunt Feedback Amplifier

The resistive feedback renders wideband input impedance matching without reducing the signal with a noisy attenuator before amplification.

In fact, at low frequencies and by applying the KCL at the output node when an input voltage v_{in} is connected to the gate of the transistor:

$$\frac{v_O}{r_O} + g_m v_{in} = \frac{v_{in} - v_o}{R_F} \tag{3.6}$$

Assuming a lower value of the resistor R_F in comparison with r_o, in first approximation is possible to determine the input impedance merely as $1/g_{m_{N1}}$ and the unloaded

gain by:

$$\frac{v_{in}}{v_{out}} = -(g_{m_{N1}} R_F - 1) \tag{3.7}$$

If the feedback resistor approached the same magnitude as r_o the small signal current will no longer completely flow through R_F and the input match will be degraded.

Considering these secondary effects, gain and input impedance equations change its expressions, as follow:

$$A_{V_{SF}} = (1 - g_{m_{N1}} R_F) \frac{r_o}{R_F + r_o} \tag{3.8}$$

$$R_{IN} = \frac{R_F}{1 - A_{V_{SF}}} \tag{3.9}$$

A further source of input impedance degradation comes at higher frequencies, since the parasitic capacitor C_{gs} of N1 is located in parallel with the input resistor:

$$Z_{IN} = \frac{1}{sC_{gs_1}} || R_{IN} \tag{3.10}$$

This capacitor contributes to worse the input matching.

The stage provides an output impedance that can be computed shorting v_S to the ground and computing the impedance of the resistive network under the same hypothesis previously assumed.

Placing a test voltage v_T on the output and dividing by the resulting output current i_T the output may be found (Note that input matching is assumed).

$$i_T = g_{m_{N1}} v_{in} + \frac{v_T}{r_o || (R_F + R_S)} \tag{3.11}$$

$$v_{in} = \frac{v_T R_S}{R_F + R_S} \tag{3.12}$$

Hence, a low frequency approximation of the output resistor can be obtained as follow:

$$\frac{v_T}{i_T} = ro||\frac{(RF + R_S)}{2} \tag{3.13}$$

The shunt feedback amplifier is frequently use as first stage of a low noise amplifier due to its feature relating a flexible input impedance with a low noise generation. Feedback renders wideband input impedance matching without reducing the signal with a noisy attenuator before amplification, its NF is much better than that of common source with resistive termination.

The noise analysis is here presented, considering the drain-source noise generation of N1, the biasing source current mirror and the shunt feedback resistor as noise sources.

Being i_{n_1} the thermal noise current generator due to the n-channel of N1, by applying the KCL at the output node:

$$i_{n_1} = \frac{v_{out}}{r_o||(R_F + R_S)} + g_{m_{N1}} v_{gs} \tag{3.14}$$

But $v_{gs} = v_{out}\frac{R_S}{R_F+R_S}$ applying a voltage division, and substituting back into the previous equation:

$$i_{N1} = \frac{v_{out}}{r_o||(R_F + R_S)} + g_{m_{N1}} v_{out}\frac{R_S}{R_F + R_S} \Longrightarrow v_{out} = i_{N1}\frac{1}{\frac{1}{r_o||(R_F+R_S)} + \frac{g_{m_{N1}}R_S}{R_F+R_S}} \tag{3.15}$$

If $R_S = 1/g_{m_{N1}}$ and $R_S + R_F << r_o$, the precedent equation simplifies to :

$$v_{out} = i_{N1}\frac{R_F + R_S}{2} \tag{3.16}$$

So, the input referred power noise follows the next equation:

$$\overline{V_{in_{N_1}}^2} = \frac{\overline{I_{N1}^2}(R_F + R_S)^2}{4(-g_{m_{N1}}R_F + 1)^2} \tag{3.17}$$

An other source of noise, to complete the noise analysis of the shunt feedback amplifier is the its biasing net, consisting in the current mirror used to get biased the whole amplifier. This current mirror is made by the pMOS P1, further adder of thermal noise starting from its current source. Its current noise generator is connected directly to the shunt feedback output impedance and its analysis follows the same steps done with the current noise generator of N1. Hence:

$$\overline{V_{in_{P1}}^2} = \frac{\overline{I_{P1}^2}(R_F + R_S)^2}{4(-g_{m_{P1}}R_F + 1)^2} \tag{3.18}$$

The total input referred noise is the sum of the last extracted expressions, and this sum is used to compute the total noise factor, as follows:

$$F = 1 + \frac{R_S}{R_F} + \frac{\gamma R_S}{4}(g_{m_{N1}} + g_{m_{P1}}) \tag{3.19}$$

The first term reduces increasing the resistance R_F, to decrease the last two terms could be made the choice to decrease both transconductances, this means to increase the overdrive voltage of the two transistors, with the trade-off to reduce the maximum voltage swing achievable and affecting the linearity of the amplifier.

Wideband low noise transconductor

It is clear that the disadvantages of the shunt feedback common emitter amplifier include the lack of design freedom degree to provide gain, 50Ω output impedance, input impedance and linearity [4] .

To decouple the input impedance, output impedance and the gain between each

other, is useful to add a second stage with particular characteristics:

- A second stage adding devices, adds noise, but using an active noise canceling topology which erases the noise sources from the first stage (the most noise contributor), this further noise is negligible.
- If this ulterior stage increases the signal gain, the noise will be reduced in a higher rate.

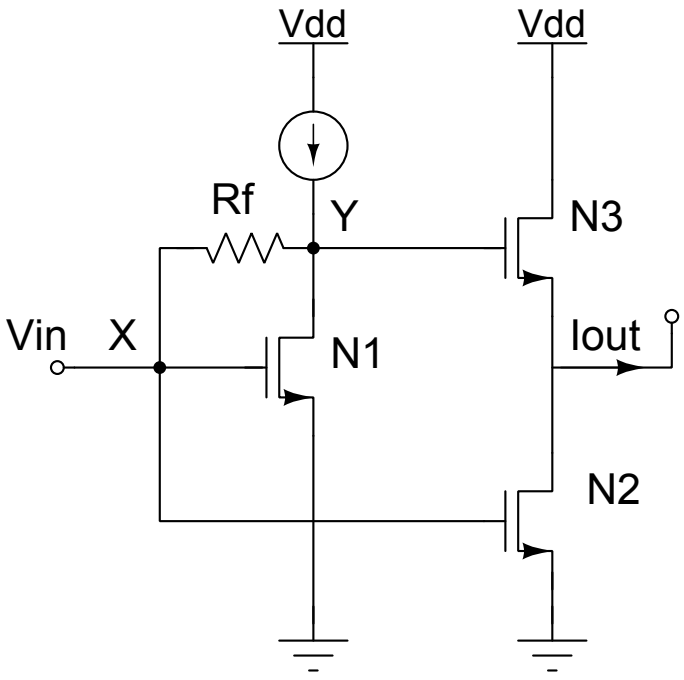

Figure 3.11: Single ended transconductor

A Gm-Cell by definition has an output current, so in order to provide the maximum rate of signal to the switching cell of the active mixer, this block should have an higher output impedance in comparison with input impedance seen at the emitter of the BJTs belonging to the two cross-coupled pairs.

Having a BiCMOS active mixer this problem can be avoided. In fact the current provided by the CS's drain terminal, will flow in a high rate to the switches instead of into the CD's source, since the BJTs transconductances, by their nature, have a

value largely greater than MOSFETs one.

The CD amplifier, from its source pin, sees the high impedance from the drain of the CS amplifier and taking into account the lower impedance seen from emitters of the switching cell connected to the same node, the current will flow completely toward the BJTs, completing its configuration with the mixer load resistor R_L.

The noise canceling takes in advantage of the resistive feedback deleting the thermal noise due to the nMOS's channel of the first stage. In fact, this feedback path, causes the noise from drain-source channel to appear at v_{IN}, after a voltage division comprehending the series of R_S and R_F.

$$v_{in} = v_{out_n} \frac{R_S}{R_F + R_S} \tag{3.20}$$

Where v_{out_n} is the voltage due to the MOSFET noise channel current. This means that the voltage noise at the output of the first stage (node X) and at the input node (Y) are in phase, while the signal path produces two out-of-phase signals among these nodes (i.e. negative voltage gain). This different difference of phase between signal and thermal noise can be useful to decrease the first stage noise contribution. The voltage of node Y, will be transformed into an in-phase-current by the transistor N3, in the other hand, N2 will produce an out-of-phase current in comparison with the input signal phase. But, remembering that the node voltage signal on Y is in out-of-phase with voltage in X, this configuration act as a signal adder. By observing the non-difference of phase among the two nodes for the thermal noise voltage, and repeating the previous steps, the second stage is easily definable as a noise subtractor.

The overall G_m and the Conversion Gain.

A first look has to be taken, over the trasconductor first stage, this stage composed by the shunt feedback amplifier, occupying the first position on the block chain, assumes an important value in terms of noise performances, so, fundamental is its analysis.

The second stage contributes in order to decrease the noise as discussed in the next section, but, in the other hand, it has a non-neglectful value even in the total transconductance of the Gm-Cell. The voltage at the input node, its converted in current, by two different paths:

- Node X is directly connected to the gate of the transistor N2, this nMOS contributes to the output current as following:

$$\imath_{out_X} = v_X \cdot g_{m_2} \tag{3.21}$$

- The shunt feedback amplifier, multiplies v_X by its gm, then, this voltage is converted in a current by N3, located at the second stage, contributing to the output with its effective trasconductance:

$$\imath_{out_Y} = v_Y \cdot \frac{g_{m_3}}{1 + g_{m_3} R_L} = v_X \cdot A_{v_{SF}} \cdot g_{m_{3eff}} \tag{3.22}$$

Then, the total output current follows the equation:

$$\imath_{out} = i_{out_X} + i_{out_Y} = v_X \cdot g_{m_2} + v_X \cdot A_{v_{SF}} \cdot A_{CD_{N3}} = v_X \cdot (-g_{m_2} + \frac{g_{m_3}}{1 + g_{m_3} R_L}(1 - g_{m_{N1}} R_F)\frac{r_o}{R_F + r_o}) \tag{3.23}$$

Finally, is possible to detect the overall trasconductance of the topology here presented:

$$G_m = \frac{i_{out}}{v_X} = -g_{m_2} + (1 - g_{m_{N1}} R_F)\frac{g_{m_3}}{1 + g_{m_3} R_L}\frac{r_o}{R_F + r_o} = (1 - g_{m_{N1}} R_F) g_{m_{3eff}} \frac{r_o}{R_F + r_o} - g_{m_2} \tag{3.24}$$

Having extracted the total trasconductance of the Gm-Cell, is possible to determine the final conversion gain for each active mixer implemented into the IQ Modulator. In fact, as seen before, the total conversion gain is:

$$G = \frac{V_{RF}}{V_{BB}} = G_m R_L (\frac{2}{\pi}) = \Big[(1 - g_{m_{N1}} R_F) g_{m_{3eff}} \frac{r_o}{R_F + r_o} - g_{m_2}\Big] R_L (\frac{2}{\pi}) \tag{3.25}$$

The noise analysis

As discussed in the second chapter, assuming an hard LO switching with negligible transition time, the principles contributors to the total noise figure of the Gilbert mixer are limited to the Gm-Cell and the load resistors.

To get easier the design steps, the topology analyzed will be half the mixer, in fact, analyzing the single-balanced counter part [1] . In fact, the output noise current of a single-balanced topology is half of the double balanced circuit $2\overline{I^2_{n,out_{sing}}} = \overline{I^2_{n,out_{double}}}$, but the load resistor follow the equation: $R_{L_{sing}} = 2 * R_{L_{double}}$. Then the output noise voltages:

$$\overline{V^2_{n,out,sing}} = \overline{I^2_{n,sing}} R^2_D \tag{3.26}$$

$$\overline{V^2_{n,out,doub}} = \overline{I^2_{n,doub}} \frac{R_D}{2}^2 \tag{3.27}$$

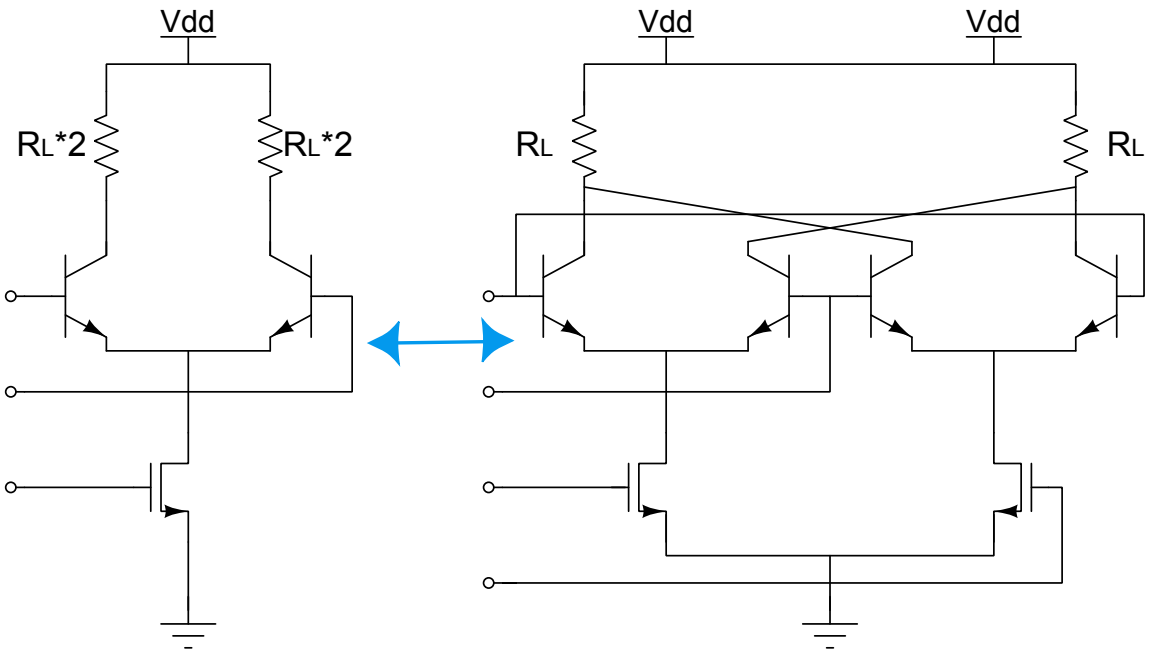

Figure 3.12: Double active mixer and the single balance counterpart

The voltage conversion gain of the double-balanced mixer is half of that of the single-balanced topology. Thus, the input-referred noise voltages of the two circuits are related by:

$$\overline{V_{n,out,sing}^2} = \frac{1}{2}\overline{V_{n,out,doub}^2} \tag{3.28}$$

This equation, still valid if the load resistors are take into account, underlines how the double balanced mixer is 3 dB more noisy than its equivalent single balanced version.

To estimate the input referred noise voltage, it is necessary to use this procedure:

1. Determining the conversion gain from the noise source to the RF output
2. Sum all magnitude noise multiplied with their related gain
3. Divide the output noise by the overall conversion gain of the mixer

As initial hypothesis the LO signal is considered a square waveform with 50% of duty cicle and all MOSFETs are considered in saturation region with the channel noise characterized with the spectral density $\overline{I_n^2} = 4kT\gamma g_m \Delta f$.

By superposition each noise source contributes independently to the toal circuit noise. Referring these noise sources back to the input as noise voltages we may calculate the ratio of the noise added by the circuit compared with the noise incident to the circuit from the 50Ω termination (Noise Factor).

Various components contribute to the total noise factor, describing the SNR degradation of the transconductor, hence, of the active mixer and the IQ Modulator.

The noise current of the transistor's channel, converted to a small signal i_{n_1}, flows back to the shunt feedback amplifier instead of the second stage, since the first stage provides a lower output impedance.

The noise current path, pass through resistors R_F and R_S, in a portion presentable as α depending on the relation between the input impedance $1/g_m$ and R_S. This current generates two instantaneous correlated noise voltages, at nodes X and Y,

with the same phase.

$$v_X = I_{n_1} R_F \tag{3.29}$$

$$v_Y = I_{n_1}(R_F + R_S) \tag{3.30}$$

The voltage at node Y, is translated to the output passing through the CD, composed by N3 and the mixer load resistor R_L. The node voltage X, is inverted and amplified, to the output by the CS configuration of N2 with R_L as drain resistor.

$$v_{out_n} = v_Y \frac{g_{m_3} R_L}{1 + g_{m_3} \cdot R_L} - v_X g_{m_2} R_L \Rightarrow v_{out_n} = (I_{n_1}(R_F + R_S)) \frac{g_{m_3} R_L}{1 + g_{m_3} \cdot R_L} - (I_{n_1} R_S)(g_{m_2} R_L) \tag{3.31}$$

The noise factor, is obtained by dividing the input power noise by the noise power due to the input termination. Then, the transistor's noise factor contribution has the following form:

$$F_{n1} = \frac{4kT\gamma g_{m_1}[(R_F + R_S)\frac{g_{m_3} R_L}{1 + g m_3 \cdot R_L} - R_S(g_{m_2} R_L)]^2}{(G_m R_L \frac{2}{\pi})^2} \tag{3.32}$$

The last equation shows how this transconductor has the possibility to delete completely the noise contribution of the first stage, while simultaneously adding the signal contribution constructively. This is done by the difference in sign for noise and signal through the Gm-Cell. The noise canceling is reached when:

$$(1 + \frac{R_F}{R_S}) \frac{g_{m_3} R_L}{1 + g_{m_3} \cdot R_L} = g_{m_2} R_L \tag{3.33}$$

The current noise source related to the pMOS P1, is connected as the N1 noise source, so its analysis mirrors perfectly the procedure already done with the same results and conclusions: the noise generated from this tail current source could be canceled if the same equation, previously discussed, is verified. The noise factor related to

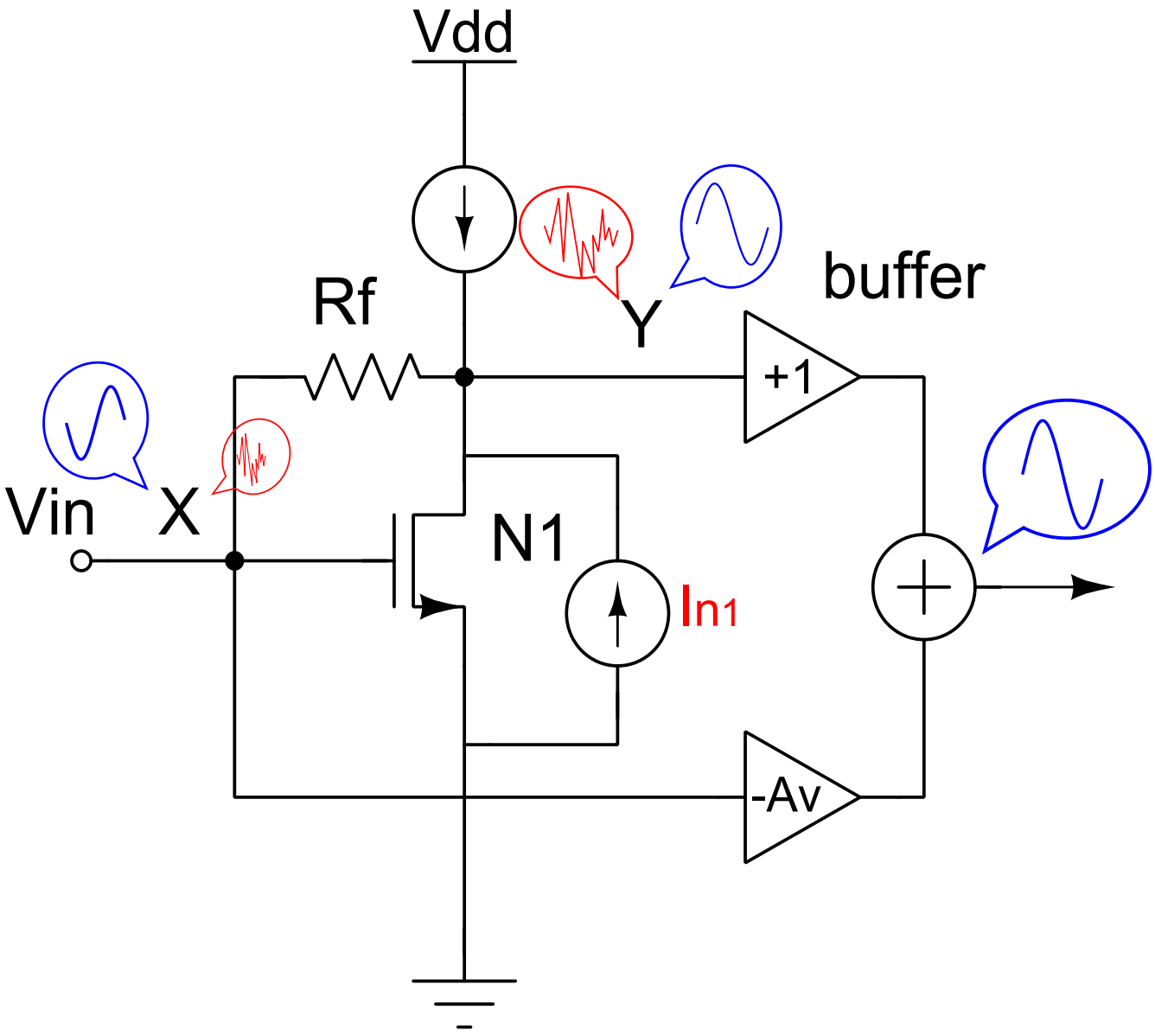

Figure 3.13: Noise canceling topology [4]

P1, is given by:

$$F_{P1} = \frac{4kT\gamma g_{m_{p1}}[(R_F + R_S)\frac{g_{m_3}R_L}{1+g_{m_3}\cdot R_L} - R_S(g_{m_2}R_L)]^2}{(G_m R_L \frac{2}{\pi})^2} \tag{3.34}$$

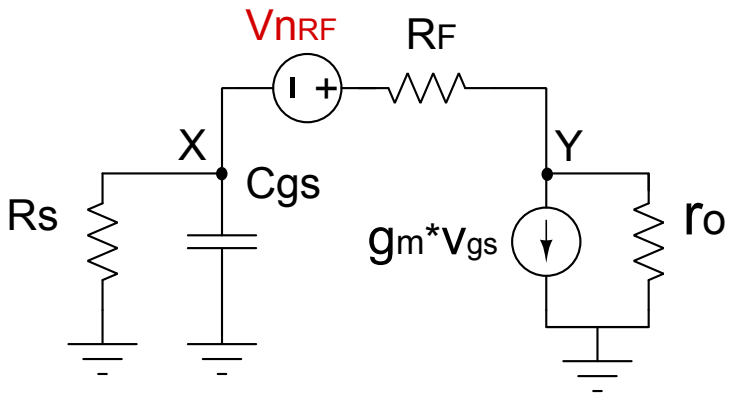

Figure 3.14: Small signal representation of the noise generated by R_F

Referring to the circuit, the shunt feedback resistor R_F is analyzed, neglecting the other noise sources. Its noise source $\overline{V_{nRF}^2}$ is changed in a small signal source: v_{nRF}.

By Applying the KCL at the output node:

$$g_{m_{N1}}v_{gs} + \frac{v_{out}}{r_o} + \frac{v_{out} - v_{nRF}}{R_F + R_S} = 0 \tag{3.35}$$

At the input node, the KCL may help to find out v_{gs}:

$$\frac{v_{in}}{R_S} = \frac{(v_{out} - v_{nRF} - v_{in})}{R_F} \tag{3.36}$$

Obtaining $v_{in} = \frac{v_{out}-v_{nRF}}{R_F/R_S+1}$. Substituting back into the KCL output's equation:

$$g_{m_{N1}}\frac{R_S}{R_S + R_F}(v_{out} - v_{nRF}) + \frac{v_{out}}{r_o} + \frac{v_{out} - v_{nRF}}{R_S + R_F} = 0$$

$$v_{out}\left(g_{m_{N1}}\frac{R_S}{R_S + R_F} + \frac{1}{r_o} + \frac{1}{R_F + R_S}\right) = v_{nRF}\left(g_{m_{N1}}\frac{R_S}{R_S + R_F} + \frac{1}{R_F + R_S}\right)$$

In first approximation, assuming $r_o >> (R_F + R_S)$ and reminding $1/g_{m_{N1}} = R_S$, the equation simplifies further to $v_{out} = v_{nRF}$. Thus, the power noise referred to the output is $\overline{V^2_{out_{RF}}} = \overline{V^2_{nRF}}$.

The thermal noise spectral density of R_F is $4kTR_F$, further, the noise passes through the nMOS N3 reaching the mixer load resistor R_L.

So the gain seen from this noise source is $A_{CD} = \frac{v_{out_{CD}}}{v_{nRF}} = \frac{g_{m3}R_L}{1+g_{m3}R_L}$, so the input referred noise power due to the feedback resistor is:

$$\overline{V^2_{in_{RF}}} = \frac{\overline{V^2_{nRF}} \cdot A^2_{CD}}{(G_m R_L(\frac{2}{\pi}))^2} \tag{3.37}$$

Hence, the contribute provides by the resistor R_F to the total noise factor is:

$$F_{R_F} = \frac{4kTR_F \cdot A^2_{CD}}{4kTR_S(G_m R_L(\frac{2}{\pi}))^2} \tag{3.38}$$

Assuming $R_F >> R_S$, $1/g_{m_{N1}} = R_S$ and if the noise canceling equation is verified, then:

$$F_{R_F} \simeq \frac{R_S}{R_F} \tag{3.39}$$

Thus, a contribution inversely proportional to the shunt feedback resistor.

Capacitive effect

The noise path belonging to the current noise source of the pMOS current tail and the nMOS N1, could be degraded in a second order analysis considering the effect due to the capacitor nested on the node Y.

That node, in a small signal analysis, sees the presences of severals capacitor coming from all transistor junctions connected to it. The main contribution is provided by the gate-source capacitor of the transistor N3, further, this capacitor is connected

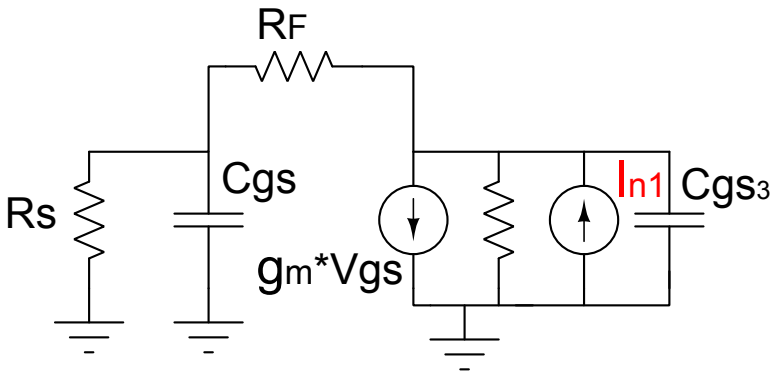

Figure 3.15: Small signal noise with the additional parasitic capacitor

in parallel, so increasing the total capacitance by the gate-drain capacitance due to transistor N3 and P1.

As consequential effect is division of the current noise source from the drain source channels of N1 and P1 splitter among the resistor R_F and the total capacitor at the node Y.

Thus, the amount of current flowing through the total capacitor at this terminal will pass through the CD amplifier and then to the load. This noise contribution at the load will be not erased by the noise cancelling technique adding a term at the total noise factor, degrading the total SNR of the Gm-Cell.

If β is the portion of noise current flowing through the total capacitor at the node Y, the further term to the total noise current has the following form:

$$F_{n'} = \frac{4kT\alpha g_{d0}(g_{m_{3eff}}R_L)^2}{(GmR_L\frac{2}{\pi})^2} \tag{3.40}$$

On the other hand the amount of erasable noise of the two amplifiers decreases of α.

To neglect this additional noise factor the size of the transistors has to be limited, paying attention principally to the size of the transistor N3 and its gate-source parasitic capacitor.

Second Stage noise analysis

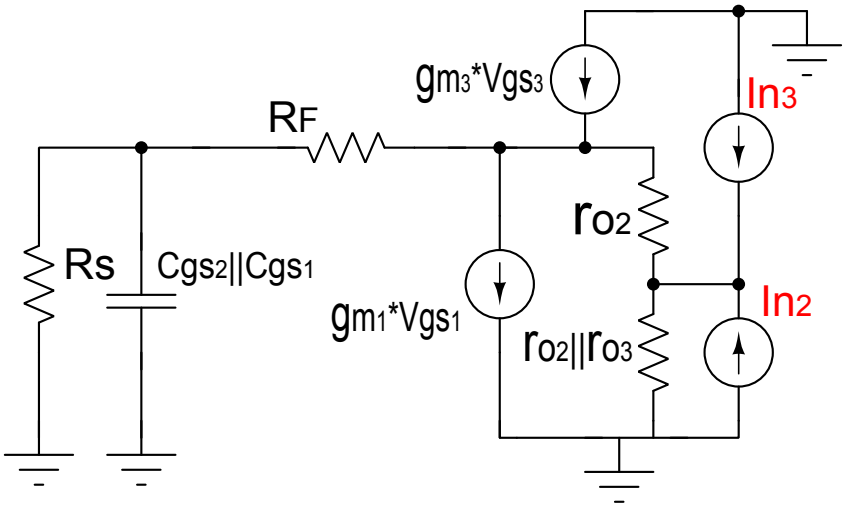

Figure 3.16: Second stage noise analysis

To minimize the noise added by the second stage, as introduced before, the resistive feedback creates a different path between noise and signals making possible to decrease the noise and to increase the gain.

The small signal model considering the noise sources of the two amplifiers placed into the output branch, is shown in Fig. 3.16.

The small signal transistor noise sources $i_{n_N 2}$ and $i_{n_{N3}}$ are located in parallel to each other and both the analysis to find the transfer function from the noise source to the output voltage are identical. Hereafter $i_{n_{2S}}$ represents a small signal noise current source from the output node to AC ground that can represent any transistor small signal noise sources.

Switching off the input voltage, the noise source current sees as impedance from its terminal, the parallel of the output resistor of both of the transistors with the load resistor. Since $R_L << r_{o_2}||r_{o_3}$ the total parallel resistor is $r_{o_2}||r_{o_3}||R_L \simeq R_L$. Further, taking a look over the the drop voltages through the terminals of N2: $v_{gs_2} = 0$, thus, N2 dependent current source is off.

The branch connecting the source of N3 with the correspondent gate is in parallel within the small signal model with the output load resistor R_L, due to the presence of C_{gs_3} at low frequencies its contribute is negligible, hence:

$$\frac{v_{out_n}}{i_{n_2S}}\bigg|_{low} = R_L \tag{3.41}$$

But increasing the frequencies this branch will add a pole and a zero to the previous transfer function. In fact, by applying the KCL to the output node:

$$\frac{v_{out_n}}{R_L} Z_{gs_3} = i_{n_{2S}} - v_{out_n} \frac{g_{m_3}}{Z_S} \tag{3.42}$$

If the gate-source impedance is the combination of the shunt feedback output resistor in series with the gate-source capacitor : $Z_{gs_3} = \frac{1+sR_{out_{N1}}C_{gs_3}}{sC_{gs_3}}$, the final transfer function becomes:

$$\frac{v_{out_n}}{i_{n_{2S}}} = (R_L||Z_S||\frac{Z_S}{g_{m_3}}) = R_L||\frac{Z_S}{1+g_{m_3}} = \frac{R_L(1+sC_{gs_3}R_{out_{1S}})}{1+sC_{gs_3}(R_{out_{1S}}+(1+g_{m_3})R_L)} \tag{3.43}$$

With a first look, at higher frequencies the gate-source branch could contribute stealing noise current from the load resistor, but in the worst case when the gate-source capacitor is shorted, R_L will be connected in parallel with the output resistor of the shunt feedback amplifier, which has a resistance value one order of magnitude higher than the load resistance, rending negligible its effect.

Now to find out the input referred noise power the previous transfer function has to be divided by the total transconductor gain:

$$\overline{V_{ni_{N2}}} = \overline{V_{ni_{N3}}} = \frac{\overline{V_{no}^2}}{(G_m R_L \frac{2}{\pi})^2} = \frac{\overline{I_n^2}}{(G_m R_L \frac{2}{\pi})^2} \tag{3.44}$$

and the related noise factor is:

$$F_{N_{1,2}} = \frac{g_{m_{1,2}}}{R_S} \tag{3.45}$$

Final noise considerations

The last term to add to the Noise Factors found above, is the contribution of the output resistors, that can be easily obtained as:

$$F_{R_L} = \pi^2 \frac{2}{G_m^2 R_S R_L} \tag{3.46}$$

To find the total noise factor all the input referred noise sources are summed. Using the equation above for the input referred noise of N2 and N3, and the previous equations , the noise factor is shown below.

$$F_{tot} = 1 + F_{R_F} + F_{N1} + F_{P1} + F_{N2} + FN_3 + F_{R_L} \tag{3.47}$$

If the noise canceling is verified, the first stage noise contribution is highly decreased. By increasing of the resistance of the shunt feedback resistor F_{R_F} can be strongly limited confining the noise contribution to the second stage devices. Is important even, to restrict the size of the transistors, avoiding, the already discussed, capacitor effects.

If g_{m_1} has to be set to $20mS$ to achieve the input matching required by the design goals, on the other hand, no straight-forward assumptions can be taken to size R_f, g_{m_2} and g_{m3}. These parameters has to weight the obtainable enhancement to the noise figure by curing even the linearity and the compression point of the overall system.

Equally, g_{m_2} and R_L if increased, limit the total noise figure, but a very high gain mixer reaches the compression point earlier due to the clipping of the transistors composing the whole system.

Increasing the shunt feedback resistance R_F, the noise decrease linearly but, as discussed in the next section the linearity suffers of the incremental gain reached by the shunt feedback amplifier.

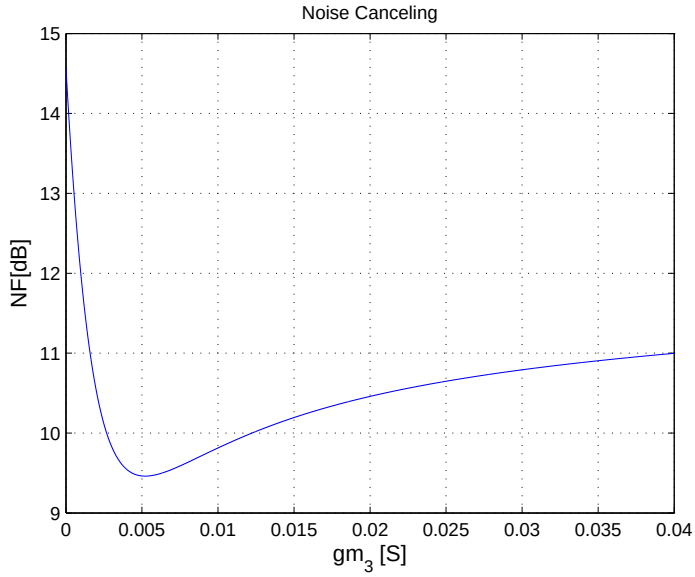

Figure 3.17: Noise figure sweeping the value of g_{m_3}, when $g_{m_2} = 50mS$, $g_{m_1} = 20mS$, $R_F = 800\Omega$ and $R_L = 130\Omega$. The minimum is reached when the noise canceling equation is totally verified.

Linearity

Moving the focus to the upper limit of the dynamic range, linear assumptions are needed. The linearity of a mixer, depends on three main factors:

1. The transconductance stage

2. The LO overdrive

3. The clipping of the output signal

The trasconductor being based on a MOSFET structure, can achieve high linearity proportionally to the overdrive voltages provided to the transistors composing it.

$$IP3 \propto (V_{GS} - V_{TH})$$

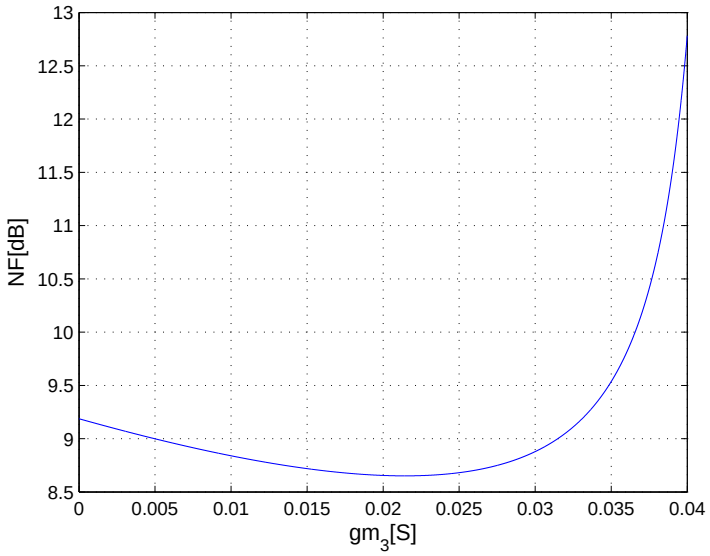

Figure 3.18: Noise figure sweeping the value of g_{m_2}, when $g_{m_3} = 5mS$, $g_{m_1} = 20mS$, $R_F = 800\Omega$ and $R_L = 130\Omega$. The minimum is reached, again, when the noise canceling equation is totally verified.

A straight forward tradeoff of this relation, is in term of noise figure [1] :

$$\overline{V_{n,in}^2} = 4kT\gamma\frac{V_{GS} - T_{TH}}{2I_D}$$

To ensure the wider dynamic range some compromises have to be taken.

A first step to achieve such a good linearity, is to guarantee for each transistor composing the Gm-Cell, the best biasing. Is also important to establish the bounder working conditions of the circuits.

The IQ mixer will be placed in a chip $930x930\ \mu m^2$, this chip will be tested by applying coupling capacitor to the baseband ports of the mixers. Consequentially, the transconductance stage has to set its common mode, by itself.

On the other hand, it is fundamental to ensure a usage flexibility for the Modulator implemented. This system has to be one of the last blocks of the transmission

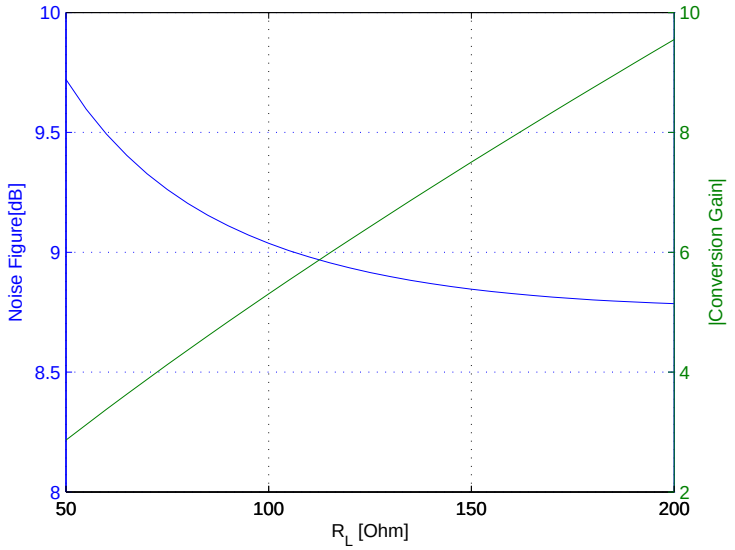

Figure 3.19: Noise figure and Conversion Gain, sweeping the value of R_L, when $g_{m_3} = 5mS$, $g_{m_1} = 20mS$, $R_F = 800\Omega$ and $g_{m_2} = 50mS$.

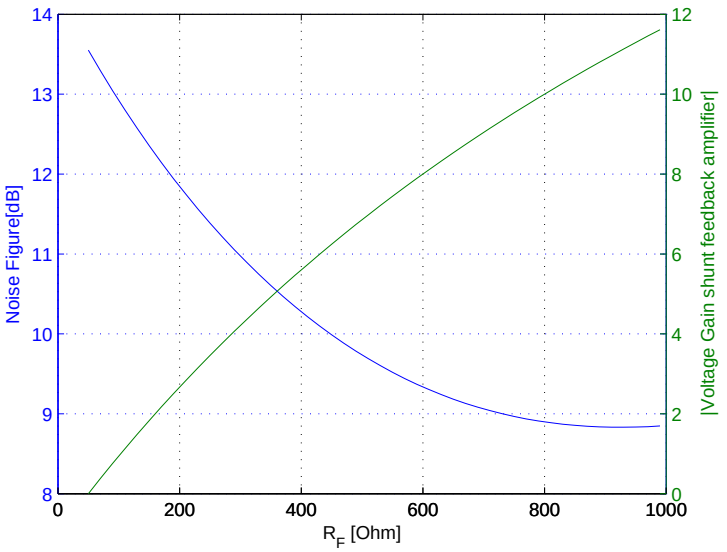

Figure 3.20: Noise figure and $A_{V_{SF}}$, sweeping the value of R_F, when $g_{m_3} = 5mS$, $g_{m_1} = 20mS$, $R_L = 130\Omega$ and $g_{m_2} = 50mS$.

chains, the source for this upconverter tipically is a couple of DACs, which most likely provide an high output resistance being a current generator. Due to that and reminding that the common lab equipment termination have a 100Ω differential impedance, the input resistor provided by the stage has to be shaped to 50Ω. This condition, can be described as the needed to limit the S_{11} factor below $-10dB$ for the whole the baseband frequencies range.

Moreover during the design of the transconductor the low area effort has to be ensured. The common biasing circuit suitable with the discussed transconductor presents coupling capacitors in order to bias the second stage independently. This assumption cannot be applied to this case. The aim of the design needs to let pass all baseband frequency from 0 to 500 MHz, forbidding the use of AC biasing within the driver stage of the active mixer.

Furthermore an AC bias for low frequencies means high capacitance, next, in place of layout, a big area effort.

The second stage, composed by a CD and CS amplifier, needs to be fed with a suitable common mode by the first stage, in fact, if the voltage nodes, V_Y and V_X, presents a dc component to feed N3 and N2 respectively, this feature requires a dc current flowing the shunt feedback resistor creating, consequentially, a drop voltage through the passive components, large enough to force in saturation region both the final n-MOSFETs preserving the linearity of the signal addition.

This additional DC current component, needs to flow to the resistor R_F and close it path through an other component, do not disturbing a possible precedent stage connected to the transconductor in terms of current and so, of linearity.

Placing a further current mirror, with the output toward the gate terminal of the first transistor this operation can be implemented. Indeed, an additional current tail mirror steels the extra current flowing through the resistor, just adding an high resistance in parallel to the first stage do not degrading the input impedance, important as specification. This current tail mirror adds as tradeoff, a contribution of noise current, but if its output resistance is enough high and its transconductance quite

low, its additional noise term is negligible.

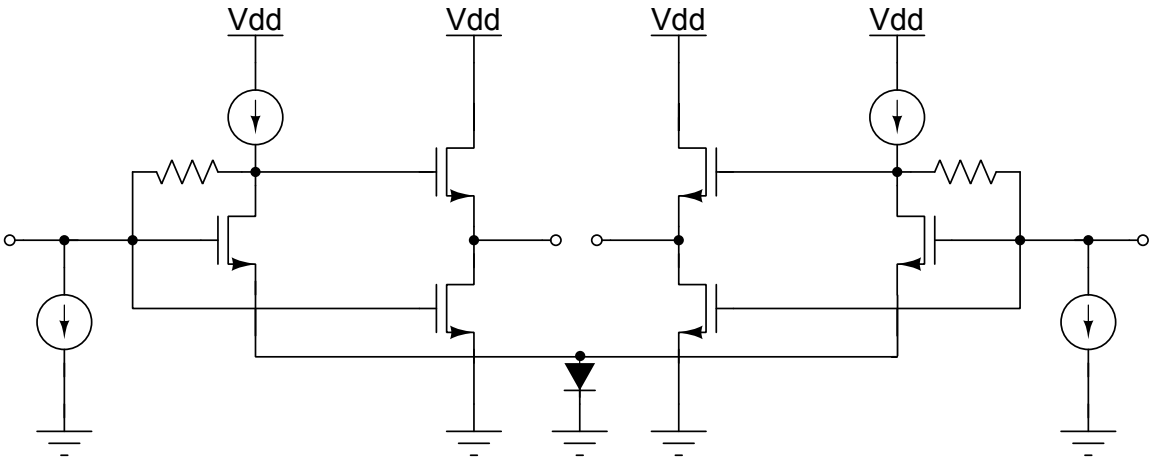

Figure 3.21: Differential transconductor

The left term of current, $I_{N1} = I_{P1} - I_{aux}$ flow through the shunt feedback amplifier. This component will set up the input impedance, shaping the transconductance of N1 (indeed at low frequencies $1/g_{m1} = Z_{IN}$). The source terminal of N1 in the final differential topology is coupled with the complementary transistor driven by $V_{BB,n}$. This node Z, has the opportunity to set up all the bias voltage of the circuit. If an ideal diode is there connected, it leaves passing any current, fixing the source voltage of the shunt feedback transistors to its drop voltage, and consequentially the node voltage V_X and V_Y. This device can be implement by a MOSFET diode connected, leaving to the design the freedom degree in matter of drop voltage, proportional to its size. It is clear how this diode does not decrease any small signal performance of the transconductor, since it is placed at an AC-ground node.

An higher output current resistance provided by the transistors, acting as current tail mirror, has the consequence to ensure a constant output current even in presence of drain-source voltage flattening, in fact, the robustness of the transconductor depends on this parameter. In a ideal case, with all current mirrors source having an infinite output resistance, the common mode voltage V_X can be moved from its equilibrium value (defined by the diode in Z), do not disturbing the biasing currents of the

entire circuit, the only consequently fact is the linear relative voltage translation of the node Y. In other terms, V_X and V_Y move together with a span of voltage: $I_{R_F} \cdot R_F$, consenting the transconductor to be driven even by a voltage input stage with different common voltage, preserving its performances as input impedance and linearity, if this input common mode does not differs with a big spread from the original value.

As discusses before, the trasconductor presents a mechanism leading the cancellation of the noise generated by the shunt feedback amplifier. This same technique is exploited to achieve a distortion cancellation.

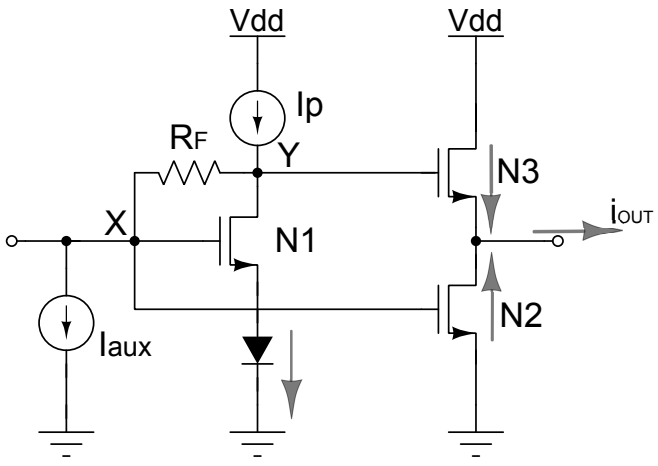

Figure 3.22: Single-ended transconductor

The small-signal linearity perfomances of a MOSFET and generally of an amplifier are degrade by the nonlinearity of its V-I conversion, that can be expainded by the Taylor series :

$$I_{out} = I_{dc} + g_m v_{in} + g_{m_2} v_{in}^2 + g_{m_3} v_{in}^3 \tag{3.48}$$

where the first, second and the third order transconductance are defined as:

$$g_{m_i} = \frac{\partial^i i_{ds}}{\partial v_{gs}^i} \tag{3.49}$$

The third order coefficient g_{m_3} performs an important role because it controls the third-order intermodulation distortion (IMD3) at a low signal level and, thus, determines IP3. In fact, the IP3 of gate voltage amplitude is given as follows:

$$IP3 = \sqrt{\frac{4g_m}{g_{m_3}}} \tag{3.50}$$

Using the Taylor approximation is possible to express the drain source current of the shunt feedback amplifier as follows:

$$I_{n1} = gm_1 V_X + I_{NL} \tag{3.51}$$

With I_{NL} denoting all the nonlinear high-order terms. Then, the signal voltage at nodes X and Y can now be written as:

$$V_X = V_{in} - R_S(I_{n1}) \tag{3.52}$$

$$V_Y = V_{in} - (R_S + R_F)(I_{n1}) \tag{3.53}$$

The distortion voltage at node Y has $1 + \frac{R_F}{R_S}$ times higher amplitude than at node X, and has equal sign: the same characteristics assumed for the noise current source. So the noise canceling equation if verified, cause the canceling of the distortion due to the transistor N1. Therefore, the linearity analysis is strictly related to the stage composed by the CD coupled with the CS amplifier [4] . Since, this stage, implies a signal sum as current, the total output current will suffer of the sum of the distortion of the two amplifiers.

The small signal output currents assume the form:

$$\begin{aligned} i_{out} = i_{n2} + i_{n3} = -(g_{m_{1,n2}} v_x + g_{m_{2,n2}} v_x + g_{m_{3,n2}} v_x) + \\ + g_{m_{1,n3}} v_y + g_{m_{2,n3}} v_y + g_{m_{3,n3}} v_y = \\ = v_x[(-g_{m_{1,n2}} v_x - g_{m_{2,n2}} v_x - g_{m_{3,n2}} v_x) + \\ + (2 - g_{m_{1,n1}} R_F)(g_{m_{1eff,n3}} v_x + g_{m_{2eff,n3}} v_x + g_{m_{3eff,n3}} v_y)] \end{aligned} \tag{3.54}$$

The current signals are summed, as already seen, with the same sign, thus, the distortion of the two amplifiers are summed. The CD stage, is the cascade stage after the shunt feedback amplifier, assuming a negligible distortion offered by N1 (discussed above), N3 convert an already amplified voltage, this fact could increase the intrinsic distortion of this amplifier, but the exiting feedback inner the CD configuration, decreases the resulting distortion by a factor of $(1 + g_{m_{1,N3}} R_L)$ counterbalancing the pre-amplification. In place of noise analysis, has been discussed the need to limit the size of the transistor N3, to avoid capacitive effects degrading the noise canceling, this assumption can fit even from a linearity point of view, limiting even the its distortion contribution.

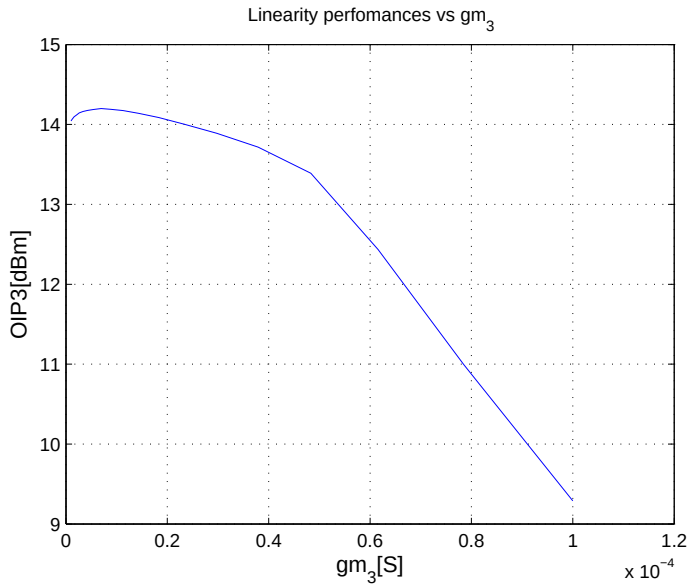

Figure 3.23: The weight of the transconductance g_{m_3} in terms of output IP3. In this case $g_{m_2} = 50mS$ and $R_L = 130\Omega$.

Increasing the gm_3 as aforementioned creates increase the distortion due the sum of the two currents on the output transconductor branch.

It is clear how at high frequency the contribution by the parasitic capacitors becomes stronger increasing the reflection coefficient.

3.3.2 The switching cell and the output load

The load of the upconverter is made by a couple of resistor, not having any needs in term of filtering, since a wideband upconvertion has to be implemented. Conversion gain and output resistor are related to each other, having a not negligible role in terms of compression point of the mixer and of the overall system.

The value of the load resistor is limited by the maximum allowable dc voltage across it. Indeed, the maximum voltage resistor has to be set as compromise among gain and output swing, since the increasing of the Gain in linear region increases, in turn, the

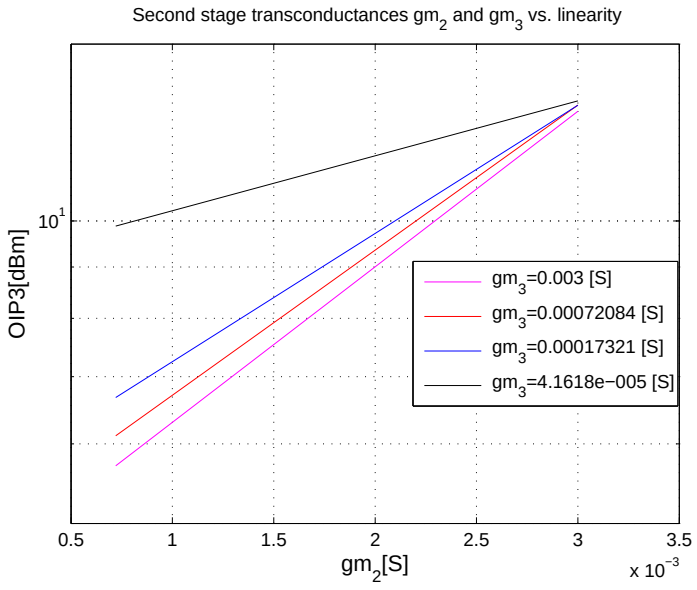

Figure 3.24: In this case $R_L = 130\Omega$.

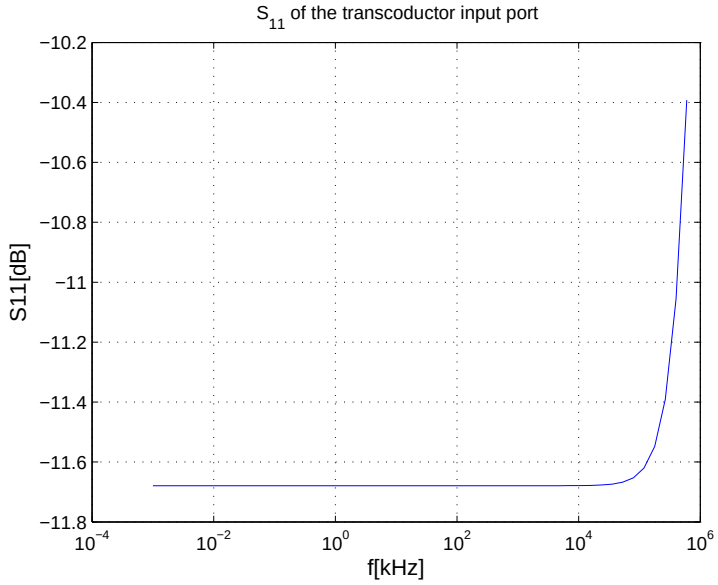

Figure 3.25: S_{11} seen looking at the input baseband mixer port.

output referred IP3 if the active device are kept in saturation mode for the MOSFET and active zone for the bipolar transistors, avoiding to cause the compression.

Too much gain conversion can put in triode region the switches of one branch when on the other branch, the transistors are in saturation.This phenom causes a signal dependent current division of I_{BB} generated by the Gm-Cell [1], between the two output path degrading the linearity of the system (Fig. 3.26).

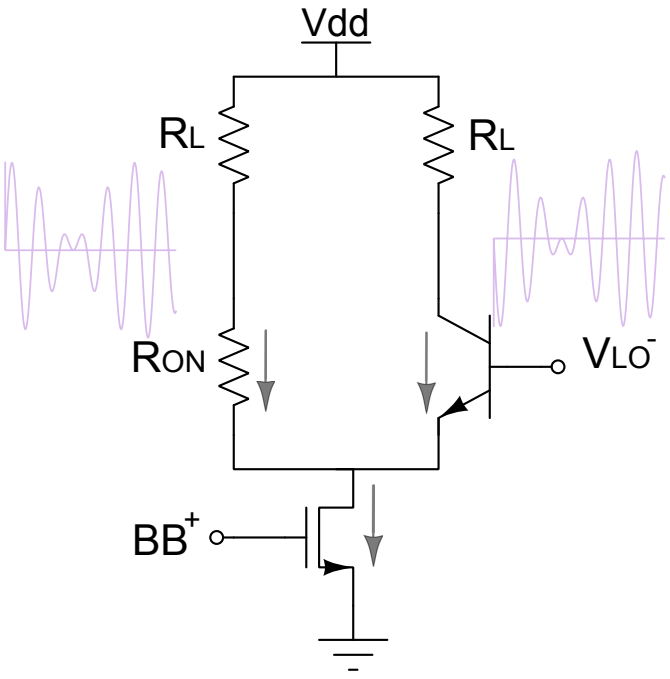

Figure 3.26: Switches in triode region produce further distortions

It is clear how the collector emitter voltage at rest V_{DS_0} has to be set an at optimal biasing to allow the transconductor to manage input power as great as possible meanwhile the mixers are working in a linear mode increasing as much as possible the compression point and dynamic range as well. This common mode configuration takes in account even the amplitude and the dc component of the LO signal, acting a main role in this design step. The switches transistor are biased at the common mode of the LO waveform $V_{CM,LO}$, and its peak of amplitude is $\hat{V_{LO}}$.The emitter of a switch composing the Gilbert cell, fluctuates according to the shape of the square

waveform of the LO. The common mode voltage at the emitter of all transistors of the switching cell is named as : V_E, and it has to guarantee the saturation zone for all MOSFETs connected through the path starting at the output of the transconductor ending at the ground. The shape of v_E is given by:

$$v_E = V_E \pm \hat{V_{LO}} = V_{CM,LO} - V_{BE} \pm \hat{V_{LO}} \tag{3.55}$$

By contrast, the collector of the switching cell changes its value according to the current i_{BB}, coming from the Gm-Cell, multiplied to the resistor. So its peaks are given by:

$$\hat{v_C} = V_C \pm G_m R_L \frac{2}{\pi} \tag{3.56}$$

The difference between the voltage of the collectors and emitters:

$$v_C - v_E = \left(V_C \pm G_m R_L \frac{2}{\pi}\right) - \left(V_{CM,LO} - V_{BE} \pm \hat{V_{LO}}\right) \tag{3.57}$$

It is fundamental to keep a linear behavior for the transconductor, especially the collector-emitter voltage has to be greater than the minimum threshold voltage to ensure the active zone for the bipolar transistors $V_{CE_{min}}$.

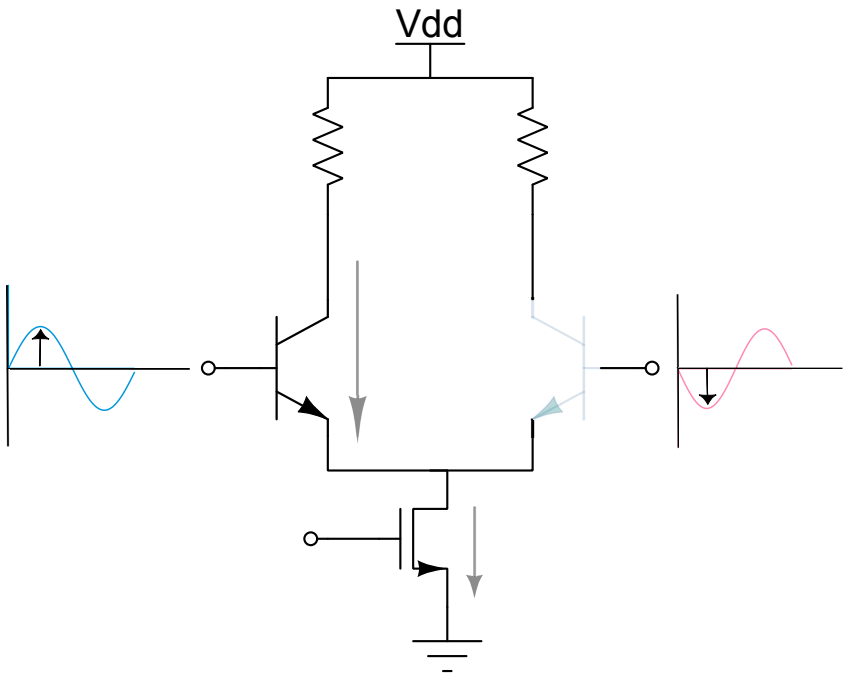

Figure 3.27: Large Signal analysis on a single balance mixer

This condition involves the load resistors, the overall G_m of the transconductor and the LO amplitude, all these parameters are set to guarantee an high gain and linearity at the same time.

Computing the output 1dB compression point while increasing the load resistors, it is possible to underline how until the increasing of the Conversion Gain do not clip the transistors the linearity of the overall can benefits. Instead when the transistors leave from the active zone the output compression point and the output intercept point come down.

3.3.3 LO port buffer

Several assumptions and hypothesis were applied to reduce the overall complexity of the active mixer analysis, based on the shape and behavior of the local oscillator voltage source applied to the switching cell. Indeed, noise and linearity performances

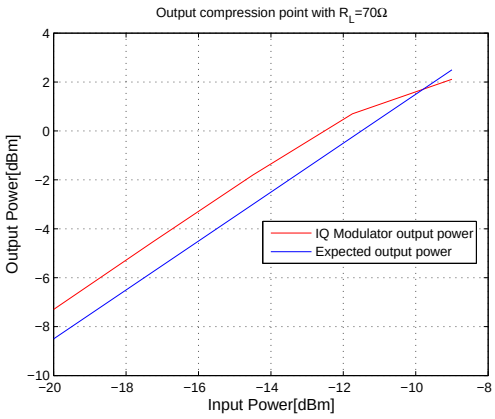

Figure 3.28: $R_L = 130\Omega$, $f_{BB} = 500MHz$ and $f_{LO} = 10GHz$

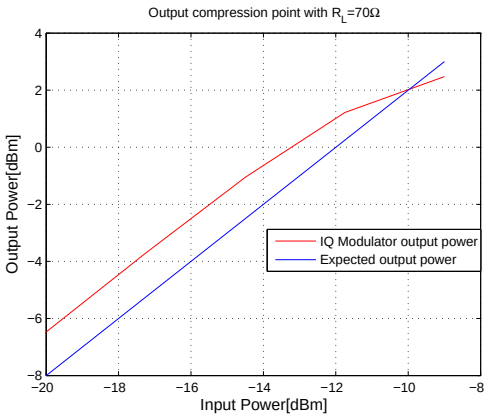

Figure 3.29: $R_L = 160\Omega$, $f_{BB} = 500MHz$ and $f_{LO} = 10GHz$

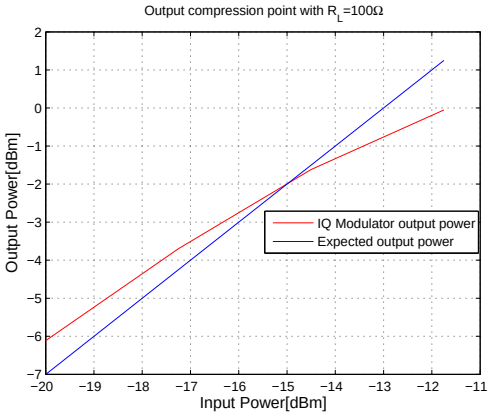

Figure 3.30: $R_L = 200\Omega$, $f_{BB} = 500MHz$ and $f_{LO} = 10GHz$.

of the mixers and consequentially of the whole structure, have a common starting point related to the hard switching of the Gilbert Cell driven by a quasi-ideal square waveform, especially the toggling periods have to be set as short as possible. By contrast, the unconditionally stability has to be verified even on this stage, and being not a two-port the mixer requires a bit more complex analysis. All the three ports has to be checked, by considering two ports at time, with differential and

single ended termination, and verifying that $K_f > 1$ and $b_{1,f} > 0$. By observing the trasconductor port, stability is not an issue, since it is implemented by a feedforward topology. This is not true looking at the switching cell port. The previous stability analysis, has shown how the parasitic capacitors and inductors, can inject unwanted oscillation at such port. This fact assumes more importance, when the stability is controlled by applying a single ended termination, cause several ac ground nodes lose their proprieties allowing the signal and thus the oscillation, to flows through it from one port to the other.

The solution, as widely discussed, is to place series resistor at the input termination of the port suppress oscillation. Losses helps stability but referring to the switching port it can compromise the quality of the wanted mixing, increasing the noise added by the switches and degrading the LO signal, distancing from the square-wave ideal behavior.

To preserve the LO signal integrity and to carry out the required specifications, a further block acting as buffer has been placed among the LO input port and the switching cell.

The buffer is implemented by using a simple emitter coupled circuit driven by the output squarewave provided by the frequency divider. The input impedance which takes an important role for the stability issue, becomes the input impedance of the differential amplifier. The considerations made by analyzing the input and output system buffers can be re-applied, but in this case the additional series resistors and the losses due to it, are counterbalanced by the possibility to set a voltage gain of the buffer and furthermore avoiding to increase the noise of the switching cell. Thanks to this stage the robustness of the frequency divider receives benefits do not overloading further its output port. The trade-off present in this cell are mainly deriving from the additional parasitic capacitors nested into the differential coupled pair, decreasing the slewrate and enlarging so the time of commutation, taken by the current to flow one branch to the other, following the input differential voltage. To reduce the effect of the transient needed to discharge the parasitic capacitors, is possible to increase the amplitude of the LO signal properly setting the load resistor connected to the

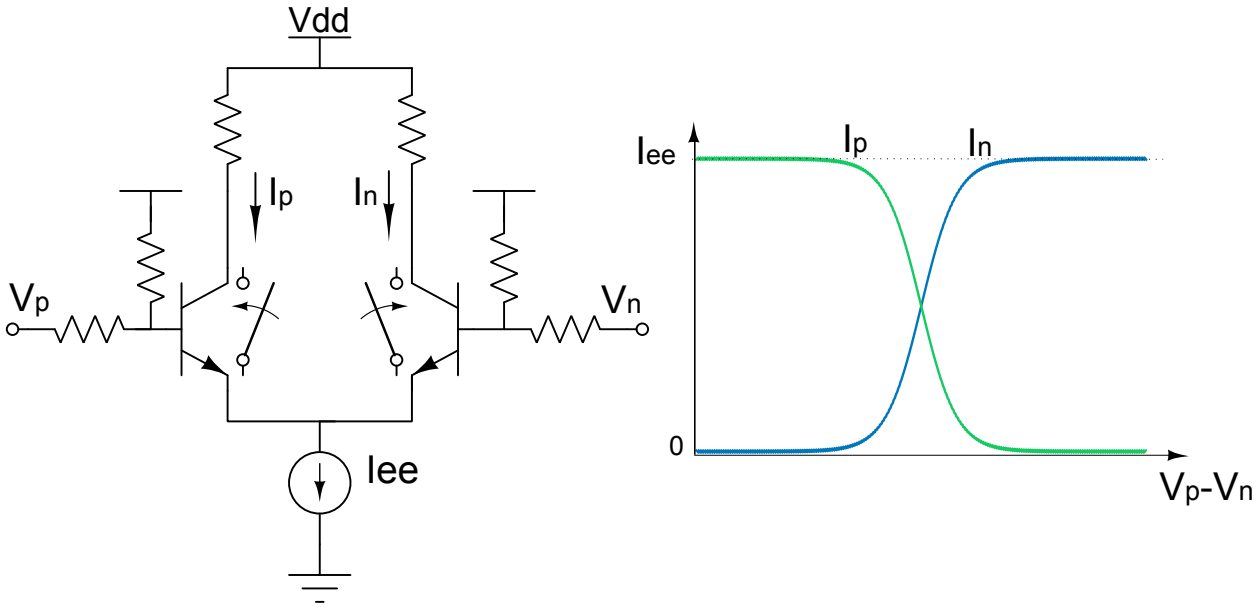

Figure 3.31: LO pre-amplifier

collectors of the transistors. Furthermore, the slewrate can be raised enhancing even the biasing current of the overall buffer.

3.3.4 Mixer Design Summary

Noise and linearity are strictly dependent on the transconductor performances, but this is true just when switching cell works in a quasi-ideal behavior, thanks to the fast toggling squarewave coming from the LO buffer, finally the load resistor describes the maximum conversion gain available to preserve a linear gain even sweeping the input power at the baseband port. All the block here quoted are dependent on each other, not facilitating the design of the block. A step by step procedure has to be made carefully.

1. As introduced, the S_{11} seen by injecting signal to the input port of the transconductor, has to stand below the -10dB referred to a 50Ω termination, the transconductance $g_{m_{N1}}$ is set to $\frac{1}{50\Omega} = 20mS$. The current passing through

it is set to $2mA$.

2. By raising the resistance R_F, the noise figure decreases linearly, but from (3.8) the gain raises consequentially. The output voltage of the shunt feedback amplifier drives N3, decreasing the total linearity (3.54). Then, $R_F = 800\Omega$.

3. Not including an AC biasing interfacing the switching cell to the LO pre-amplifier, the common mode of the output transconductor node is set by the biasing of the pre-ampliflier. This node is set as $V_E = 1.5V$ allowing enough headroom to bias N1 and its complementary source coupled transistor, and the current tail mirror generating the bias current.

4. Then the overdrive voltages applied to all the transconductor transistors, is completed setting up I_{aux}, the current flowing from the node Y to the node X, in fact :$\Delta V_{YX} = R_F * I_{aux}$. For the second stage amplifiers:

$$V_{OV_3} = V_Y - V_E - V_{th_3} \tag{3.58}$$
$$V_{OV_2} = V_X - V_E - V_{th_2} \tag{3.59}$$

   I_{aux} is established to a value of $1mA$.

5. The transconductances of N3 and N2, have an heavy weight being the transistors composing the output branch of the Gm-Cell. As discussed into the precedents sections, the sizes of both are important to reach an high gain and the noise canceling. On the other hand the CD amplifier N3, adds parasitic capacitance to the noise path and add distortion to the output current, since it is the follower of the amplified node voltage V_Y. So it is important to limit g_{m_3}, and the best compromise between noise and linearity is setting $g_{m_2} = 50mS$ and $g_{m_3} = 2mS$, with a biasing current $I_{BB} = 7.5mA$. The most of I_{BB} flows to the switching cell, due to the current division among switches and CD amplifiers, completely dominated by the bipolar g_m . The noise canceling is not completely verified but a large amount of noise is subtracted even with this configuration, conserving such a good linearity. Consequentially by (3.24), the

total transconductance $G_m \simeq 57mS$.

6. Choosing the best suitable load resistor values, is possible to ensure an high linearity even raising the input power applied to the baseband port. The LO buffer signal decided to drive the switches has to counterbalance the losses and the delay, added to the square waveform provided by the frequency divider, deriving by stability resistor and parasitic capacitors. By choosing a biasing current flowing through the LO buffer of $I_{B_{buff}} = 6mA$, the buffer load resistor of 30Ω, the amplitude voltage driving the switching cell is $\hat{V_{LO}} \simeq 400mV$. By (3.57)the load resistor is $R_L = 130\Omega$.

With this configuration the noise figure of a single mixer stands slightly below the 7dB, the OIP3 reaches averagely the +14dBm and the compression point is almost +2dBm in the variety of combination of LO and baseband frequencies at the input. The S_{11} seen at the input port of the Gm-Cell increases with the frequency, due to the parasitic input capacitor effect (3.10), however its highest values stands below the target of $-10dBm$.

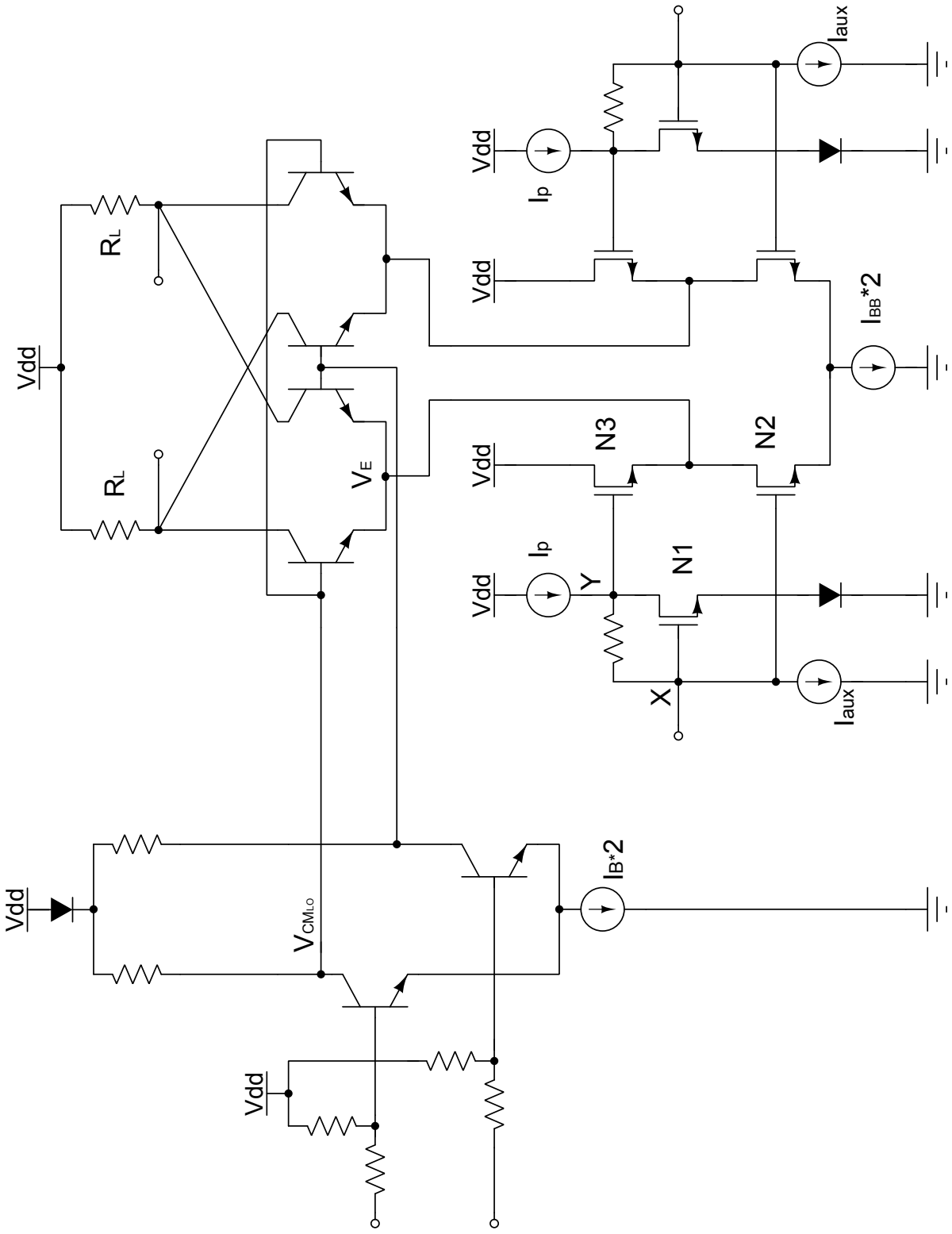

Figure 3.32: The implemented double balance active mixer

3.4 Biasing circuits

3.4.1 BiCMOS current mirrors

The current mirrors find a wide employment into the integrated circuits. During the whole design and implementation of this project they have been used biasing the several branches composing the modulator. By using current generators as biasing element can enhance the insensitivity of the system to the temperature and power supply variations. Furthermore, is possible to restrict the area of the chip using biasing circuit made by current sources instead of simply resistors. The BJTs current mirror differs to the MOSFET counterpart, by the systematic presence of a degeneration resistor saving its stability and increasing the output resistor by a factor $(1 + g_m R_E)$. Several are the kind of biasing mirror here implemented to feed the overall circuit.

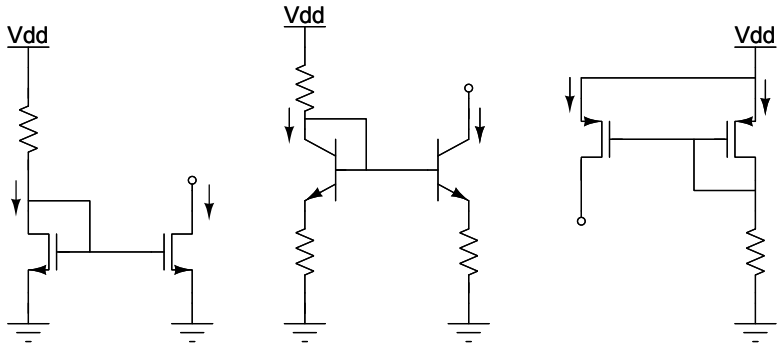

Figure 3.33: Current mirrors

When the headroom is enough to bias more then one device, the current mirroring is employed by connecting two transistor in a cascode current mirror topology, saving area and increasing the output resistance provided by the source. Within the mixer transconductor is placed even a kind of BiCMOS cascode current mirror implemented by the cascade of one MOSFET and one BJT, since the available headroom better suites with the combination of a collector-emitter and drain-source voltages.

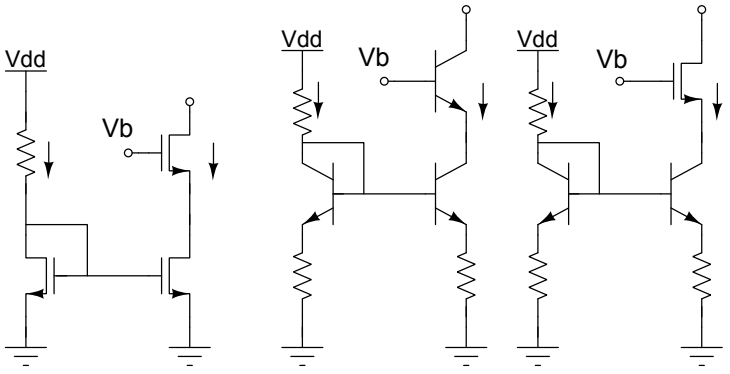

Figure 3.34: Cascode current mirrors

3.4.2 Enable circuits

The overall IQ Modulator during production test has to not draw any current when is switched off. This general chip building block requirement, requires to arrange a enable and disable external pin interfacing with all the blocks composing the IQ Mixer.

A pMOS interconnected among the supply voltage and the components of a current mirror source can employ the required duty. It is important to properly size the transistor allowing through all the current needed by the current source.

Fig. 3.35 shows a complete emitter follower topology. The biasing branch is composed by the enable pMOS transistor driven by a not logic port, in order to let pass the current through it when the enable pin is at the high logic state.The implemented current mirror is made by a cascode topology, in fact the available headroom in this stage, allows the connection of two bipolar with a degeneration resistor. This architecture permits to provide an high output resistance and to decrease the area consumption of the block. Finally, the current flowing through the driver branch is set by the resistance of R_B.

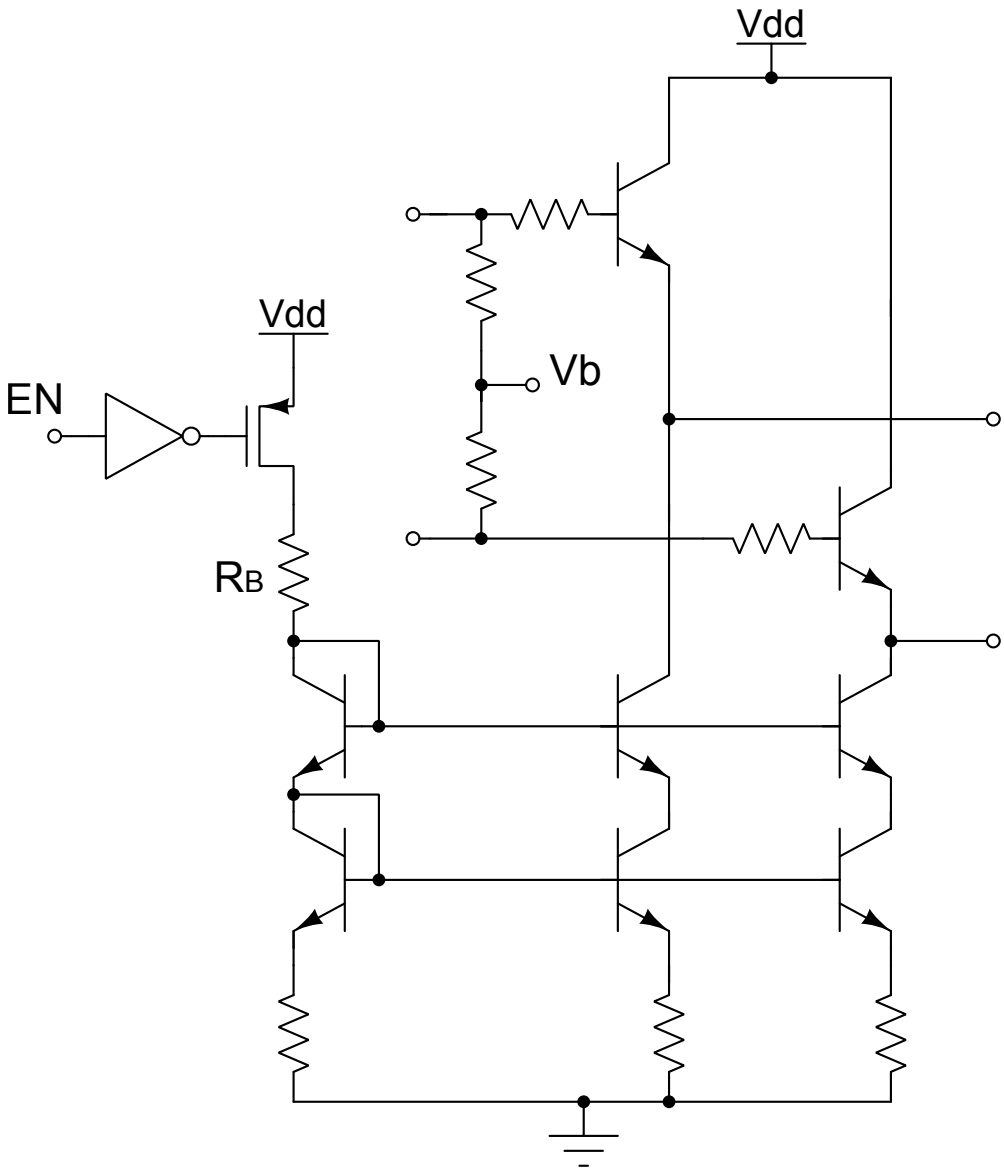

Figure 3.35: An examble of complete biasing circuit for the IQ Modulator input buffer, including the enable circuit.

3.4.3 ESD Protections

All the connections to the pad, are integrated of an additional circuitry employing the electrostatic discharge protection. Since the birth of the ICs, the electrostatic discharge issue has increased its importance year by year due to the increasing of the achievable chip speed and the decreasing of their size. During the manufacturing process the chips, having different contacts with several devices, can suffer of electrostatic discharges generating small transients more dangerous when the devices geometry is smaller. This unwanted currents can damage or totally destroy junctions, gate oxide and metallizations in a IC. The most common ESD protection for the integrated circuits are net of diodes. When two diodes are connected to the pads, and if they are forward biased, they allow the discharge through themself connecting V_{DD} or V_{SS}.

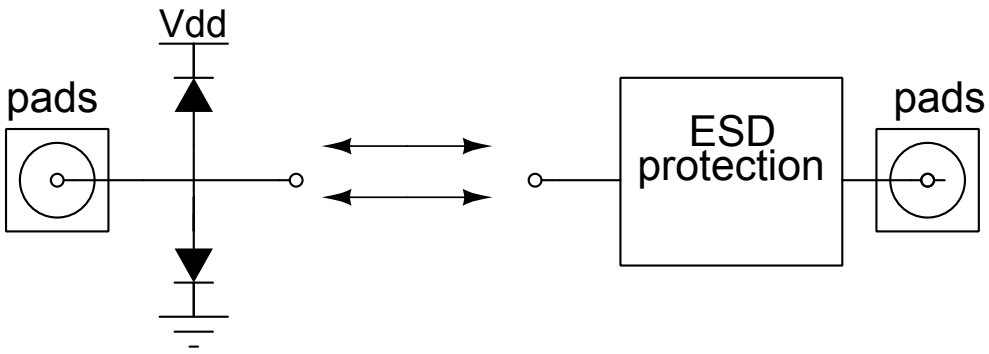

Figure 3.36: ESD protections connected to all pads connecting the chip.

This is not the only available topology to implement ESD, at the RF port of the chip a more suitable solution can be applied. In fact, the electrostatic protections add parasitic capacitors due the depletion region of the diodes. These parasitic components degrade the signal injecting to the input radio frequency port and the output modulated signal. To reduce this effect, one solution is show in Fig. 3.37 , which reduces the overall parasitic capacitance exploiting series connection of capacitors.

The trade-off is in term of devices number .

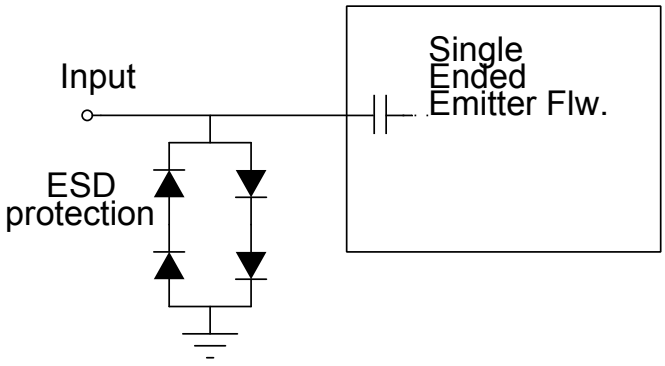

Figure 3.37: Emitter Follower ESD connection

3.5 The Frequency divider

Studying a single D Flip Flop of the Current Mode Logic frequency divider is possible to derive the maximum toggle frequency. Assuming at time $t = 0^-$, the output Q was low, which means the capacitances C_1 and C_2 were high and low respectively. At t=0, the clock goes high and the input D goes high, this switches the whole of the current I_{ss} through the transistor T1 and T5. The capacitor C_1 discharges with this current, until its drop voltage reaches $V_{dd} - I_{ss}R_L$, on the other hand, C_2 charges via $I_c(t)$ until its potential arrives to V_{dd}. If the whole current at $t = 0^+$ passes through T1 and T5, therefore, for $0 < t < T/2$ using the KCL in A:

$$\frac{V_{dd} - V_1}{R} - C_1 \frac{dV_1}{dt} = I_{ss} \tag{3.60}$$

Solving this differential equation with the condition of $V_1(0) = 0$, then the voltage at node A is given by $V_1(t) = V_{dd} - I_{ss}R(1 - e^{\frac{-t}{RC_1}})$. Dually,s following the same steps the $V_2 = V_{dd} - I_{ss}Re^{\frac{-t}{RC_2}}$.

The time variation of the output voltages in the sensing phase is shown in (3.39), which clearly shows that half the clock period has to be greater than T_{cr} [19] , allowing the verifying of the condition:

$$V_2(T/2) > V_1(T/2) \rightarrow e^{\frac{-T/2}{RC_1}} + e^{\frac{-T/2}{RC_2}} < 1 \tag{3.61}$$

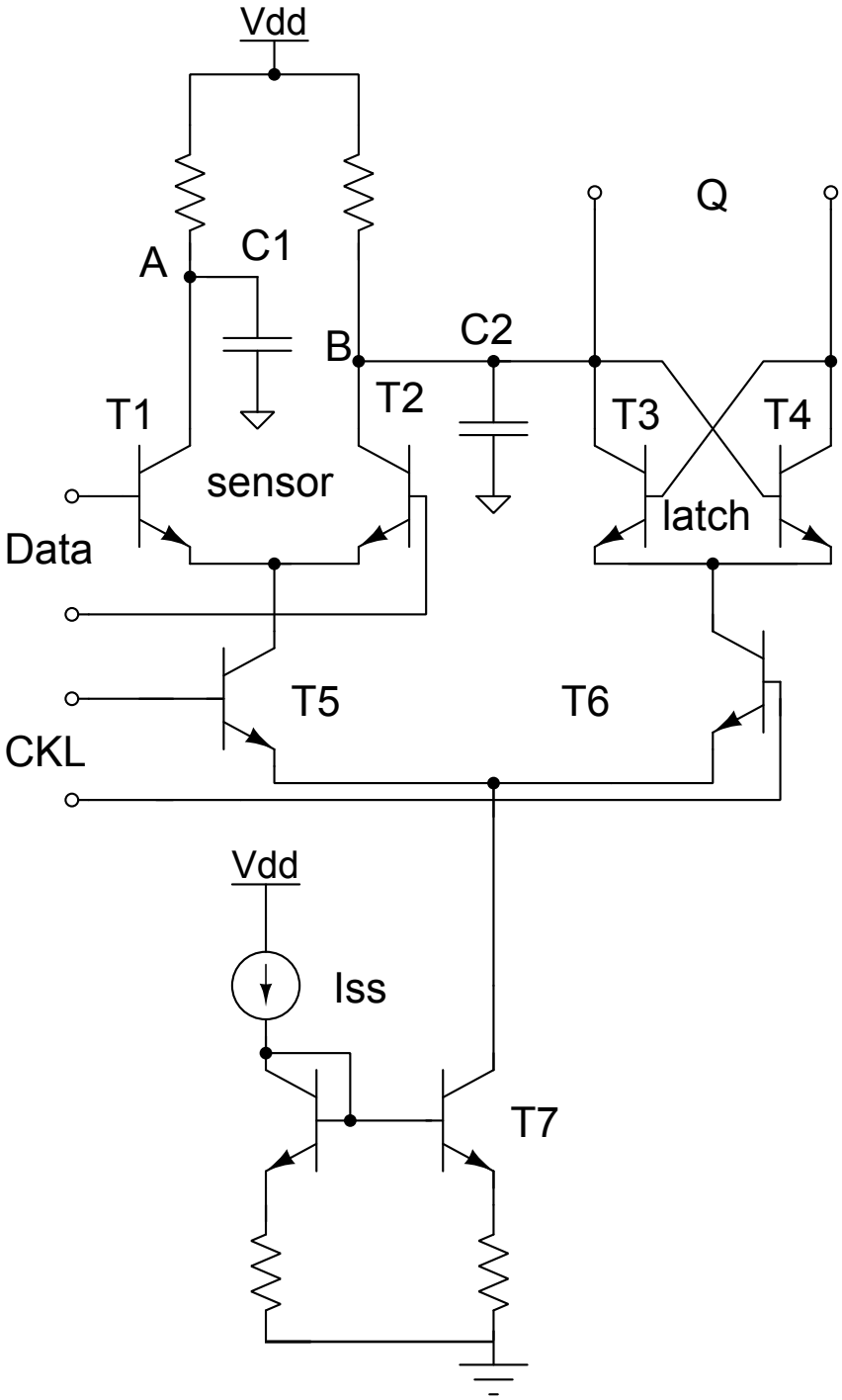

Figure 3.38: D Flip Flop implemented in Current Mode Logic

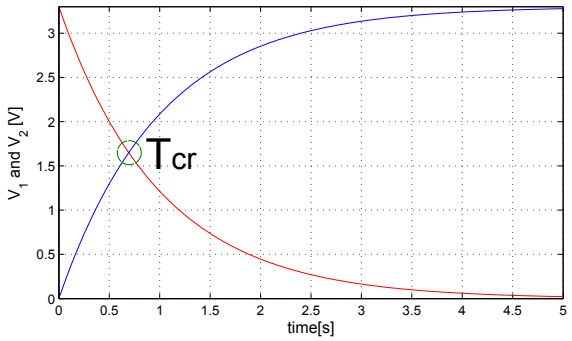

Figure 3.39: Typical transient of V_2 and V_1 due to the presence of C_2 and C_1, respectively.

If the two capacitors are equals, the previous expressions is verified if:

$$T/2 > ln(2)RC \Rightarrow f_{clk} < \frac{1}{2ln(2)RC} \tag{3.62}$$

Hence, decreasing the load resistor can increase the maximum frequency operable. However, decreasing R reduces the output swing proportionately and therefore the drivig capacity, degrading the overall robustness.

To limit the quadrature error the device mismatch has to be managed and decreased, this is done by increasing the size of the transistors. The tradeoff is represented in terms of parasitic capacitances nested in the BJTs, so a decreasing of the load resistance is needed to balance this lost of velocity. The output swing of the frequency divider has been fixed increasing the biasing current of the whole block.

To accomplish a DC bias, interfacing the frequency divier output port and the RF input port of the active mixer, the output common mode can be properly managed by using a couple of voltage shifters connected to the in phase and quadrature outputs of the circuit. Moreover an additional features added by this solution is found analyzing the input port of the mixer. In fact, the generated squarewave toggles the two emitter coupled transistors connected to the switching cell. This transistors suffers of Miller effects, that can degrade the quality of the LO voltage and then of the

overall system, by the excessive overloading. Interconnecting a voltage shifter this effect is suppressed, conserving the robustness of the commutation.

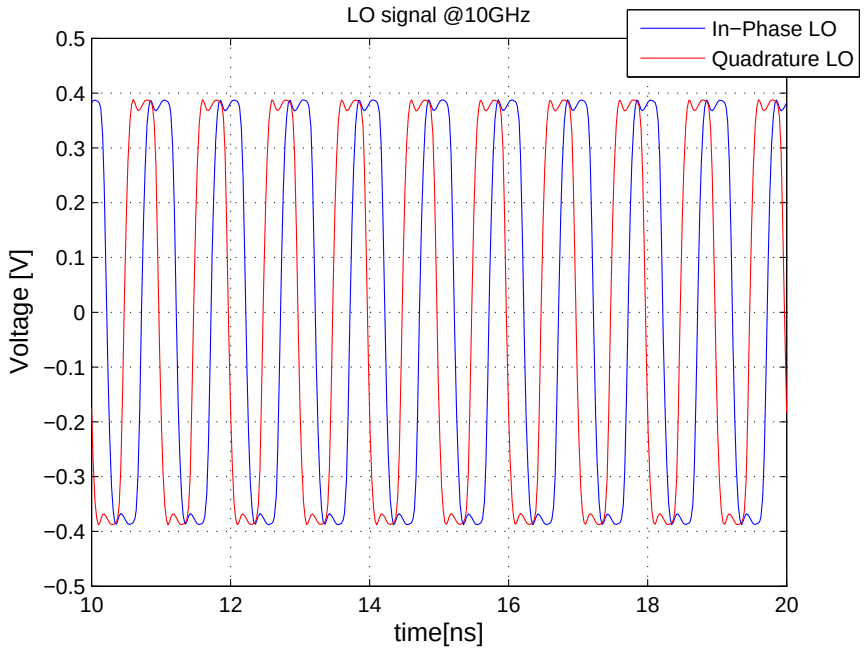

Figure 3.40: Transient of the output quasi-square wave provided by the frequency divider at $f_{LO} = 10GHz$.

Stability check

Even being a frequency divider, with an unstable characteristic by nature, the unconditional stability has been checked for all the ports of the block in order to suppress any form of additional oscillation that could disturb the quasi-squarewave produced by the block itself. Due to that, series resistor are placed in series at the input clock port and at the biasing port.

3.6 The Multipath Polyphase structure

A MutiPath PolyPhase Mixer is here designed, to delete the spurs representing the third order intermodulation distortion around the third LO harmonic. By using the table (2.1) and (2.2) and the equation (2.19), it is straightforward how 4 Mixers and so, 4 differential paths have to be employed on the new IQ Modulator system [10] . The LO signal has to be applied to two frequency dividers connected in cascade, providing 4 differential RF signals with a difference of phase between each other of 45° degrees equi-distant in the phase constellation. The same has to be applied to the baseband signals, in this case the frequency shifting can be acted in the digital domain, or remaining in the time continue domain the signal could be processed by an all pass filter or even called equalizer over the required baseband [20] .

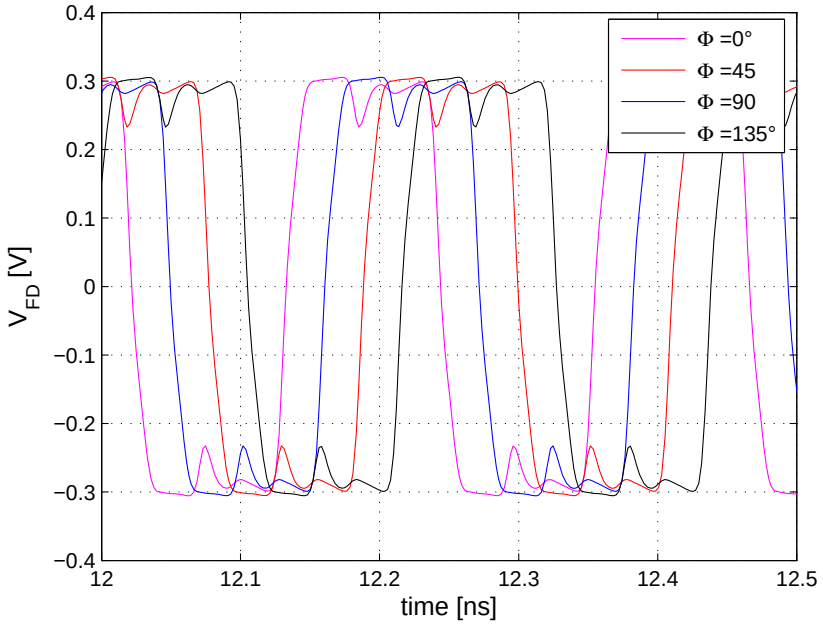

Figure 3.41: Frequency dividers output voltages.
With a 45 degree difference of phase among each one
Frequency at 4GHz.

Noise, Power and Area considerations

The desired signals in every path are in phase before they are added. In this way no signal power is lost due to the addition. This addition is done by summing the currents for every path. By not changing the biasing current for each mixer, to keep the same conversion gain is needed to reduce the load resistance by a factor of N (N=4 in this case) to avoid the clipping zone for the transistors and maintaining the linearity. But letting flow a N times higher currents to the load, the noise performance of the system suffers of additional power contributors coming from each input port of the system. It is easily understandable, in order to limits the noise figure as much as possible, that is required to design the multipath system with the same output power at the load. Thus, the current per path in a system with N paths can be N times smaller than the current in a system with one path . When the current per path is N times smaller, then in general the noise power per path can also be N times smaller. Therefore, the total noise power after the addition node is not deteriorated by the polyphase technique. In terms of area decreasing the signal currents to achieve the same performances an amount of area can be saved during the layout. On the other hand, the LO signal generation needs two frequency dividers, and two buffers for each one, which are difficult to dwindle. Due to that the dimension of the modulator of N differential paths in comparison with a single modulator, gets close to multiply the area effort by N.

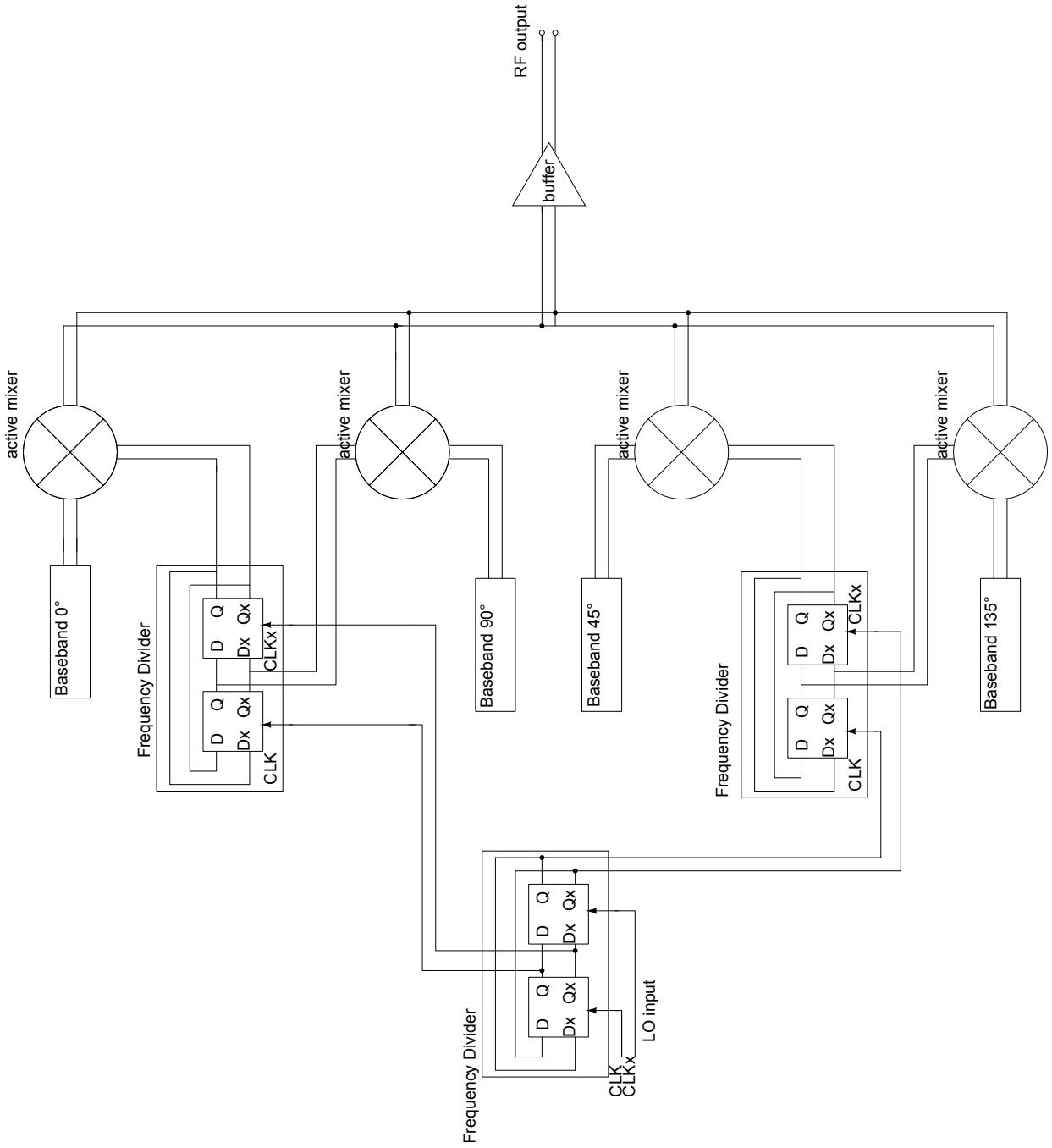

Figure 3.42: The simulated Multipath Polyphase Mixer

Chapter 4

Layout

This chapter is organized in order to discuss the considerations and the choices taken during the layout of the complete modulator.

4.1 Layout considerations

At high frequencies parasitic components start to be effective and their contributions can highly deteriorate the quality of the implemented mixing. Parasitics as inductor, capacitors and resistors are nested on every track, causing several unexpected effects. It is important to reduce the number of issues due to these parasitic components to follow some easy rules within the layout, especially in case of radio frequencies design. All the input and output are provided in a differential termination, and several assumptions taken during the design are strictly correlated to the differential nature of the signals, to do not compromise the system behavior is opportune to guarantee the symmetry of the system as far as possible. As tradeoff an unbalanced circuit increases the LO feedthrough and decreases the image rejection ratio. The connections have to be as short as possible, long connections increases the parasitic inductance causing, as discussed in the previous chapter, possible oscillations along the system.

The overlapping of two metals has to be avoided, to do not create not expected capacitance between two points of the circuit, establishing a "media" between them. Moreover, enlarging the width of a line increases the capacitor between the line and the below metal, by contrast, the reducing of the width increases the parasitic resistor. It is important to understand which is the better choice to take during the layout in order to conserve the system performances.

Finally, long transistor need to be folded, using the parallel interconnection of smaller devices, this has the effect to half the source/drain parasitic capacitance and the gate resistor of the transistor.

4.2 Input buffers

For the input buffer, since it is an emitter follower unbalancing effects do not cause strong effects in terms of final performances. The most of the area is spent to place the coupling MIM-capacitors. Being a circuit managing the highest frequencies of the chip the connection line lengths have to be limited to avoid the parasitic inductor, sources of possible parasitic oscillations.

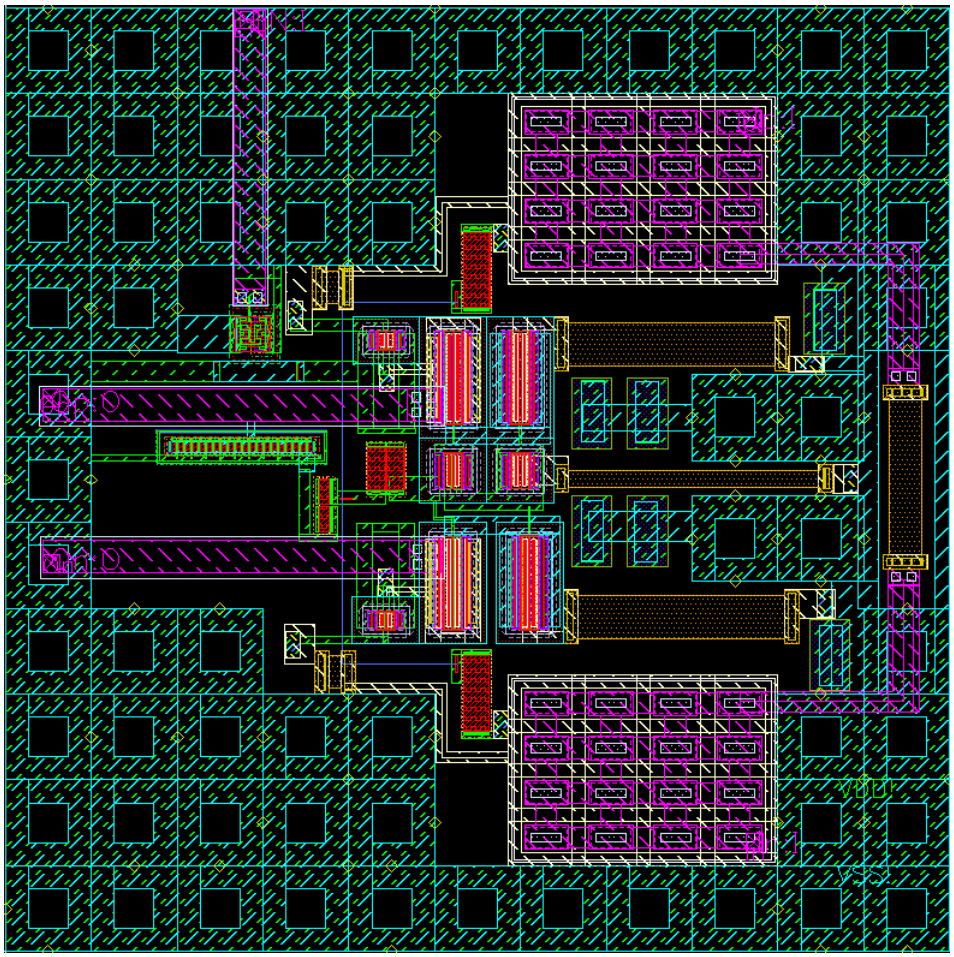

Figure 4.1: Layout of the emitter follower.
Area: $110x110\mu m^2$

4.3 Output buffers

The layout of the output buffer has to be as symmetrical as possible being a differential pair with degeneration resistor. Since the chosen biasing current to $10mA$, the layout has to be done with low resistive connection at the higher level of metal, to avoid big parasitic capacitors. Dually, the DC part of the circuit where no high frequency signal is managed, the width of the lines if do not overlap other paths, can be enlarged to let pass all the current and to decrease the overall metal resistance, conserving the biasing point.

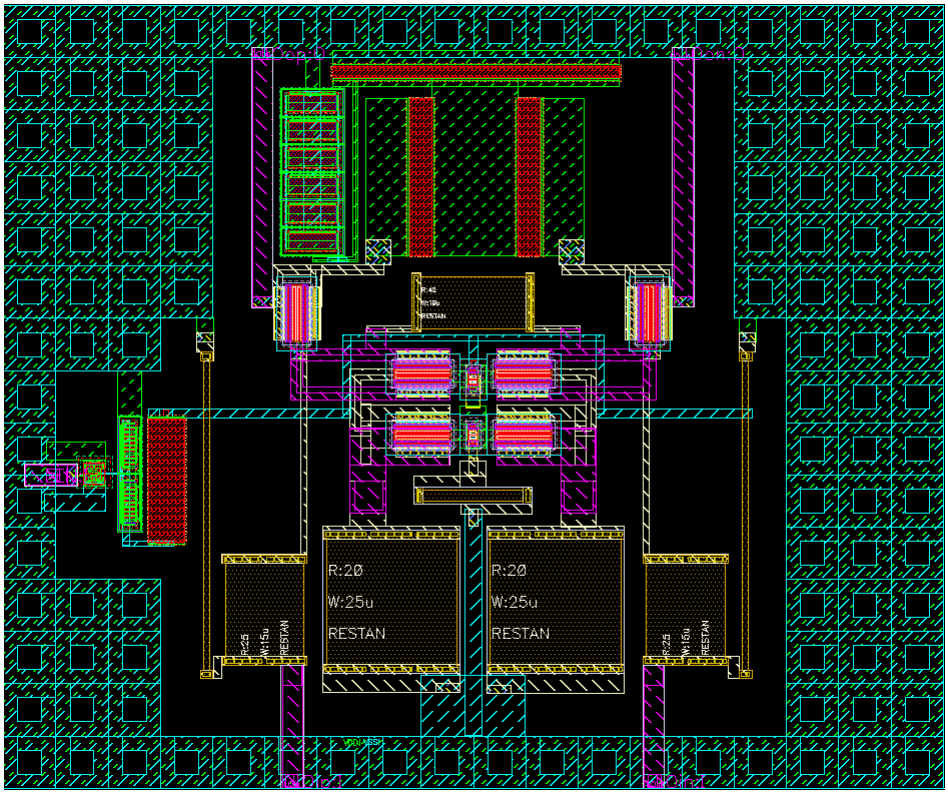

Figure 4.2: Layout of the differential output buffer.
Area: $150x180\mu m^2$

4.4 Mixer

The largest and most complex block to be implemented in phase of Layout is certainly the active double balanced mixer. The LO signal passes, first of all, through the pre-amplifier composed by the pair of emitter coupled transistors. Since high frequency signals flows through this block, the better choice is to decrease as far as possible the total unbalancing into the signal path, by using high level metals and the overlaps between connections. The transcodunctor implemented by CMOS technology is the core of the mixer, and consequentially the most important block of the system, making fundamental a good layout implementation.

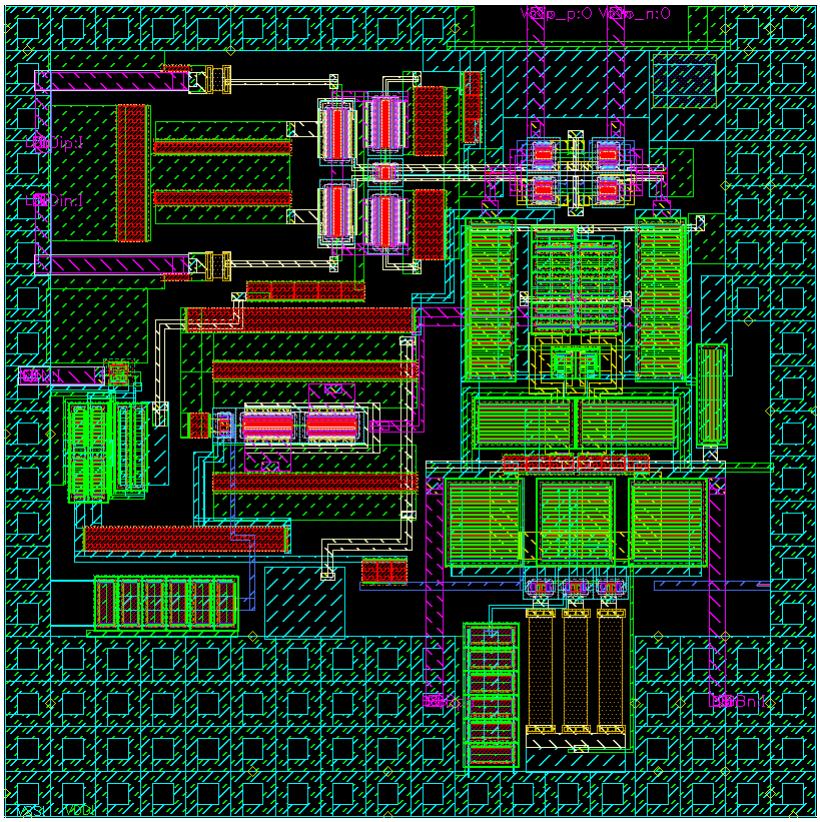

Figure 4.3: Layout of the active mixers.
Area: $180x180\mu m^2$

For the widest MOSFETs, in order to reduce their inner parasitic gate resistance, it is required to fold them. Furthermore, the noise figure strictly depends to the magnitude of the gate resistance provided by the input MOSFETs. MOSFETs are significantly larger than bipolar counter and the most percentage of the total mixer area is spent to place the MOSFET's transconductor.

4.5 Frequency Divider

The frequency divider being drived and generating high frequency signals, needs to be balanced as much as possible limiting the error of phase between the two IQ square waveforms. As previously discussed, the parasitic capacitors found connected to the output resistance can significantly enlarge the transient of the commutation state into a signle D flip flop. Limiting the width of the metallization can help to reduce this delay.

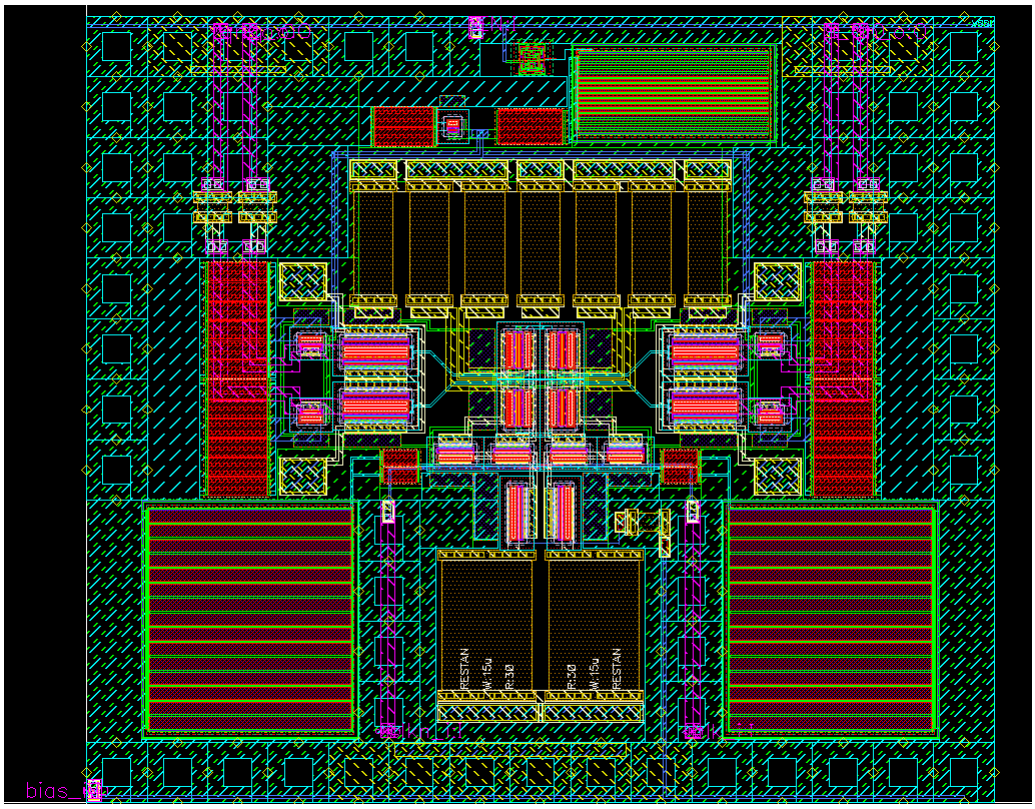

Figure 4.4: Layout of the CML static frequency divider.
Area: $140x120\mu m^2$

4.6 Top Level

The complete layout of the WideBand Upconverting IQ Modulator is here shown.

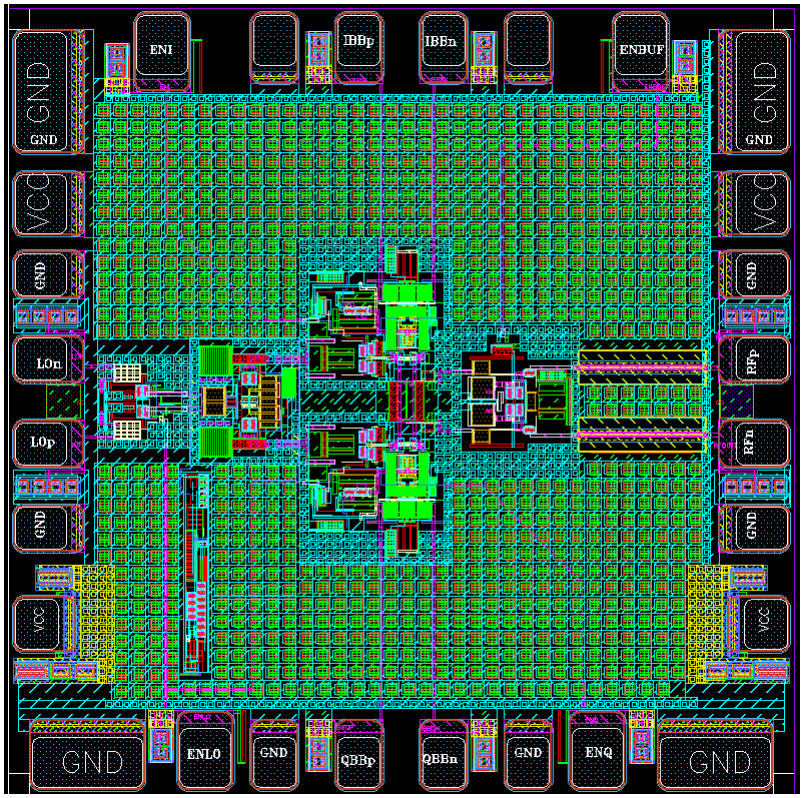

Figure 4.5: Top level
Area = $930x930\mu m$

All the blocks of the chip are surrounded by a matrix of power supply decoupling capacitors. All the differential inputs are placed with two extra pads which are connected to ground within the test.A number of 4 pads are available to connect the ground, and 2 to connect V_{dd}. As visible, surrounding the chip are placed 4 enables pads. These pads, permits during the testing, to switch on/off independently the various blocks, doing it, various configuration of the chip, as for instance a single mixer test, can be made. To enhance the matching between the two load resistor

nets present one per each mixer, are merged to a unique couple of resistors with half of the resistance. Finally, a 50Ω transmission line is connected between the output pad and the RF signal delivered by the output differential buffer.

Chapter 5

Simulations

5.1 Waveforms in the time domain

Input baseband voltage

Baseband input voltage, injecting two tone at 501MHz and 503MHz at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$ and a $f_{LO} = 10GHz$.

Fig. 5.2 shows the presence of the intermodulation distortion upon the waveform.

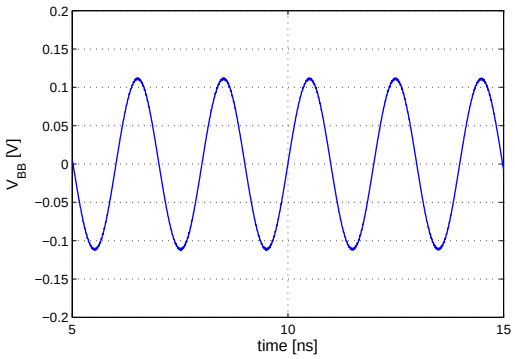

Figure 5.1: $V_{bb}(t)$

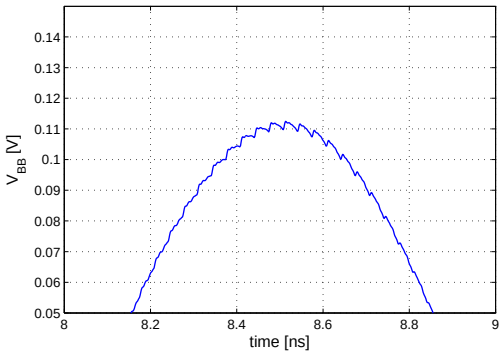

Figure 5.2: $V_{bb}(t)$

Output RF voltage

The voltages here shown are produced by sweeping the LO frequencies and injecting a 500MHz baseband voltage at the input port at the nominal conditions of $T = 27°$ and $V_{dd} = 3.3V$

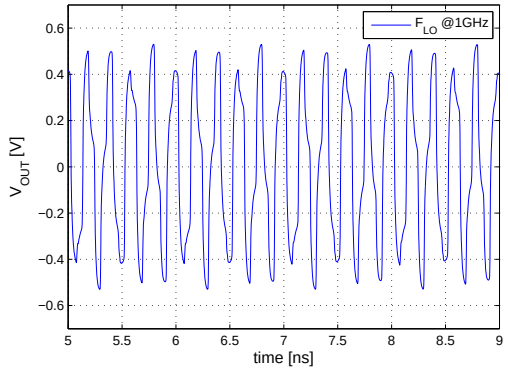

Figure 5.3: $f_{LO} = 1GHz$.

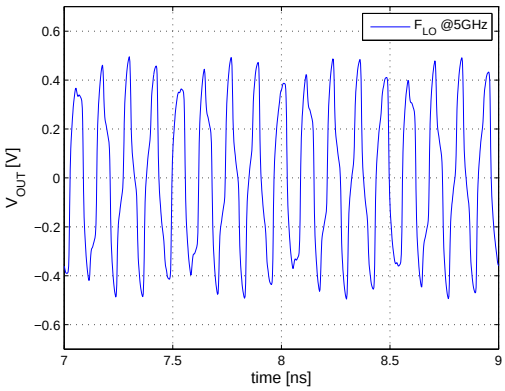

Figure 5.4: $f_{LO} = 5GHz$

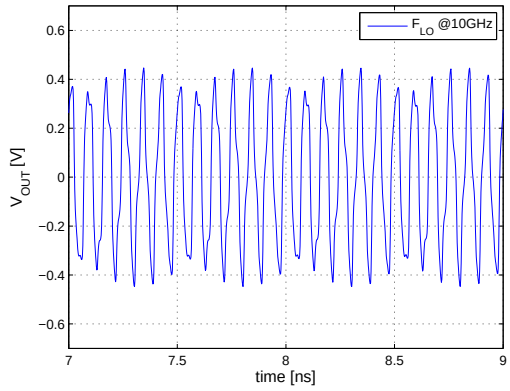

Figure 5.5: $f_{LO} = 10GHz$.

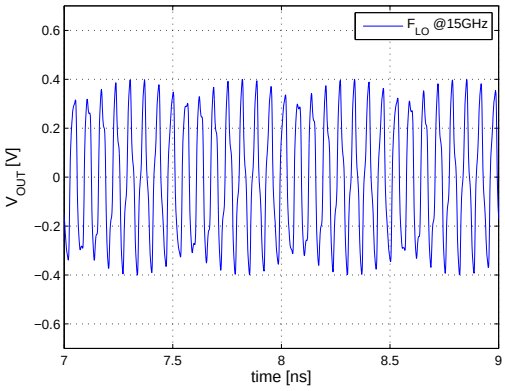

Figure 5.6: $f_{LO} = 15GHz$

Frequency Divider output voltage

The frequency divider output waveforms are here shown. The simulation is performed at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$.

At higher frequencies the produced quasi-square waveform assumes a more sinusoidal shape, since the third-order harmonics stands even more at higher frequencies, and the frequency response of the total system reduces its amplitude.

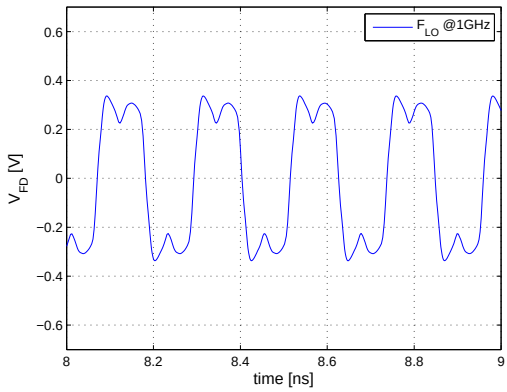

Figure 5.7: V_{FD} with $f_{LO} = 1GHz$.

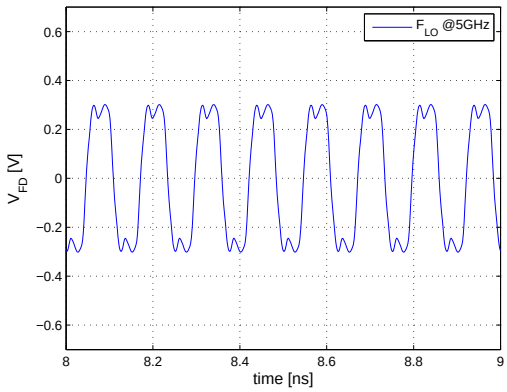

Figure 5.8: V_{FD} with $f_{LO} = 5GHz$

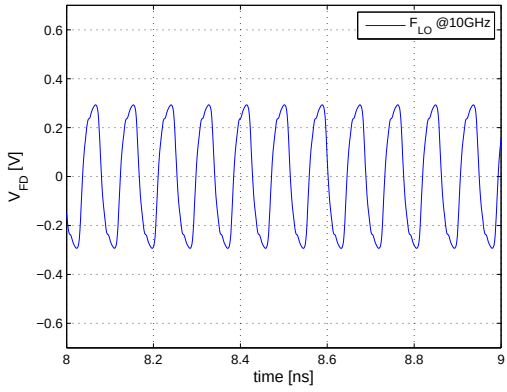

Figure 5.9: V_{FD} with $f_{LO} = 10GHz$.

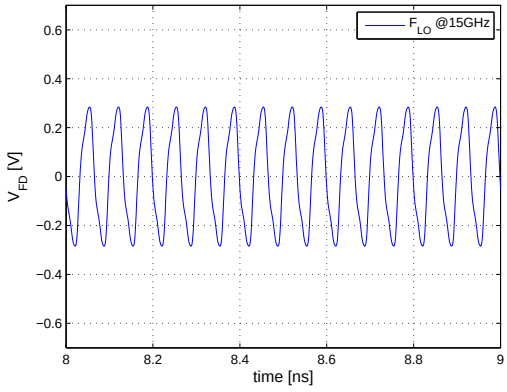

Figure 5.10: V_{FD} with $f_{LO} = 15GHz$

Waveforms produced by the emitter coupled pair before the switching cell

The boosting employed by the emitter coupled pair placed before the switching cell, is illustrated here below.

The simulations are performed at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$.

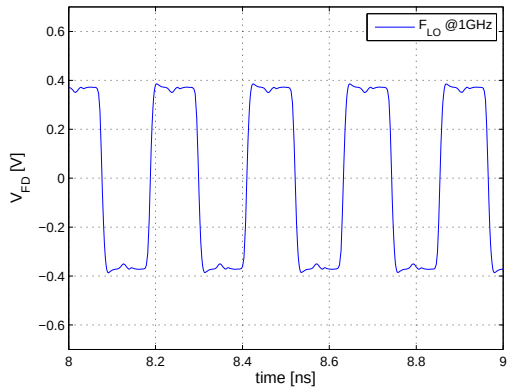

Figure 5.11: V_{em} with $f_{LO} = 1GHz$.

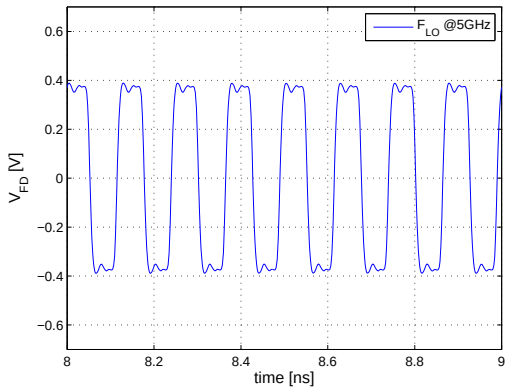

Figure 5.12: V_{em} with $f_{LO} = 5GHz$

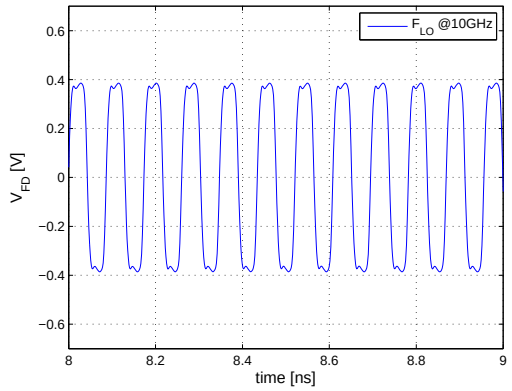

Figure 5.13: V_{em} with $f_{LO} = 10GHz$.

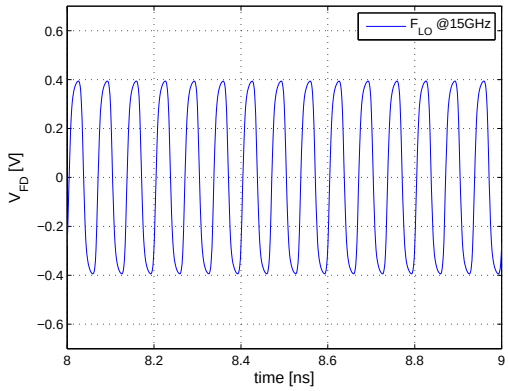

Figure 5.14: V_{em} with $f_{LO} = 15GHz$

5.2 Reflection coefficients

Input LO buffer

The input reflection coefficients are shown here.

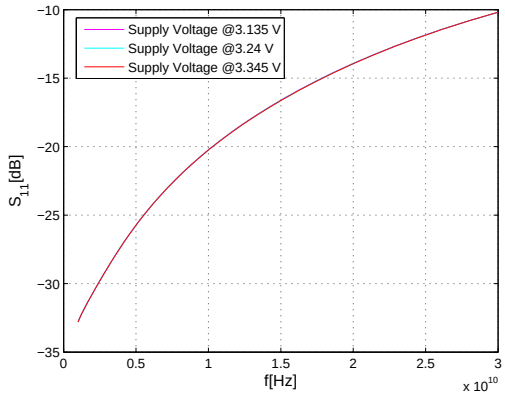

Figure 5.15: S_{11} with $T = 0°C$

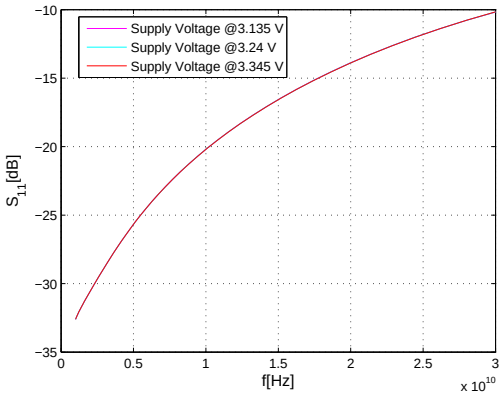

Figure 5.16: S_{11} with $T = 21.25°C$

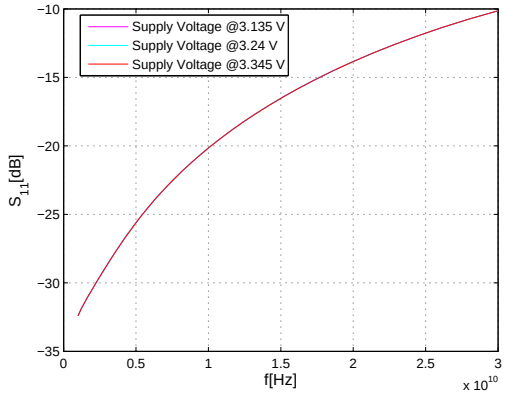

Figure 5.17: S_{11} with $T = 63.75°C$

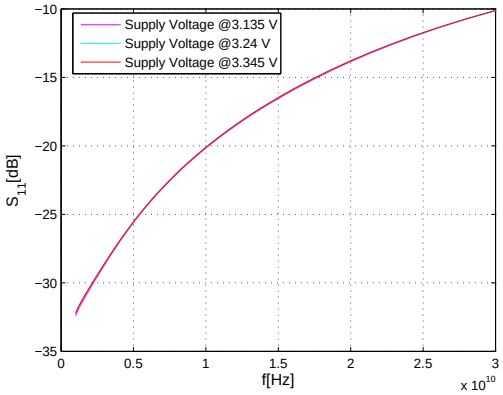

Figure 5.18: S_{11} with $T = 85°C$

Input baseband port

The input reflection coefficients are shown here.

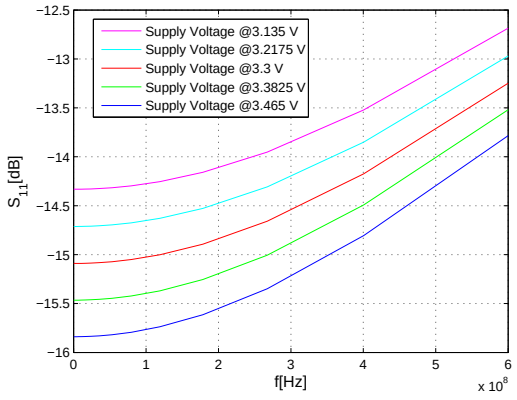

Figure 5.19: S_{11} with $T = 0°C$

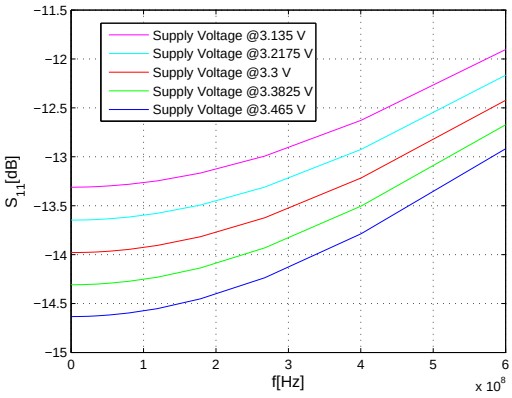

Figure 5.20: S_{11} with $T = 21.25°C$

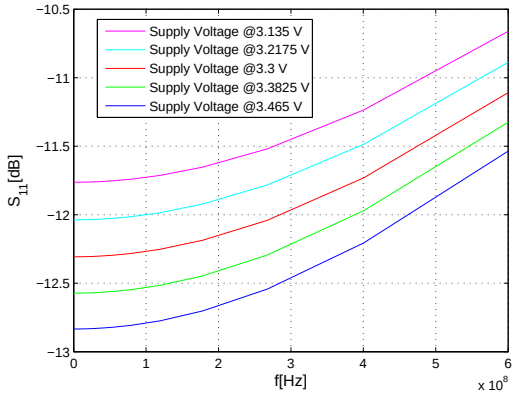

Figure 5.21: S_{11} with $T = 63.75°C$

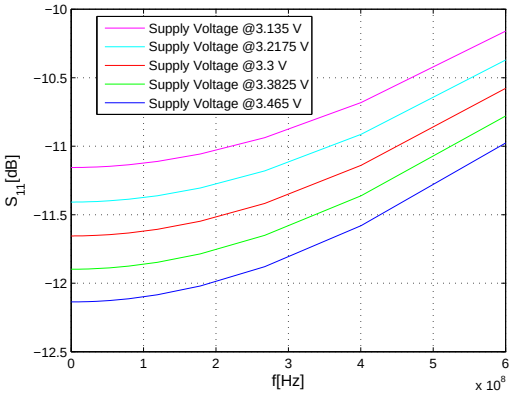

Figure 5.22: S_{11} with $T = 85°C$

Output buffer

The output reflection coefficients are shown here.

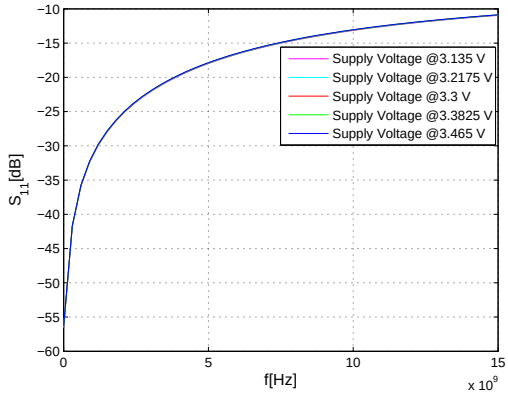

Figure 5.23: S_{11} with $T = 0°C$

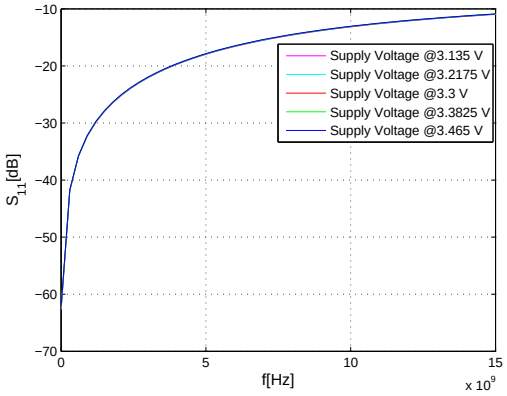

Figure 5.24: S_{11} with $T = 21.25°C$

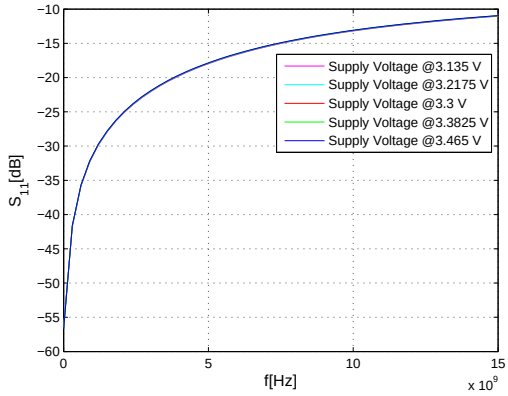

Figure 5.25: S_{11} with $T = 63.75°C$

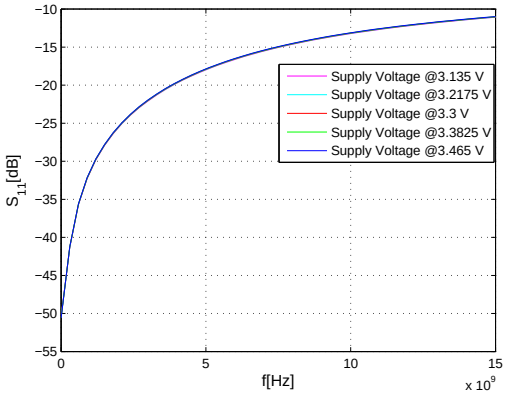

Figure 5.26: S_{11} with $T = 85°C$

5.3 Noise Figure

Noise Figure at various LO frequencies

These noise figures are collected by sweeping the LO frequency at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$. The noise figure point extracted is the median in the band of interest.

The noise figure gets its minimum in the middle of the LO band, at lower value of f_{LO} the noise figure increases due to the higher rate of noise folding from others frequencies, on the other hand at higher frequencies the LO voltage waveform features, as previously underlined, a more sinusoidal shape, consequentially the toggling produced by the waveform is less abrupt increasing the noise contribution by the switching cell.

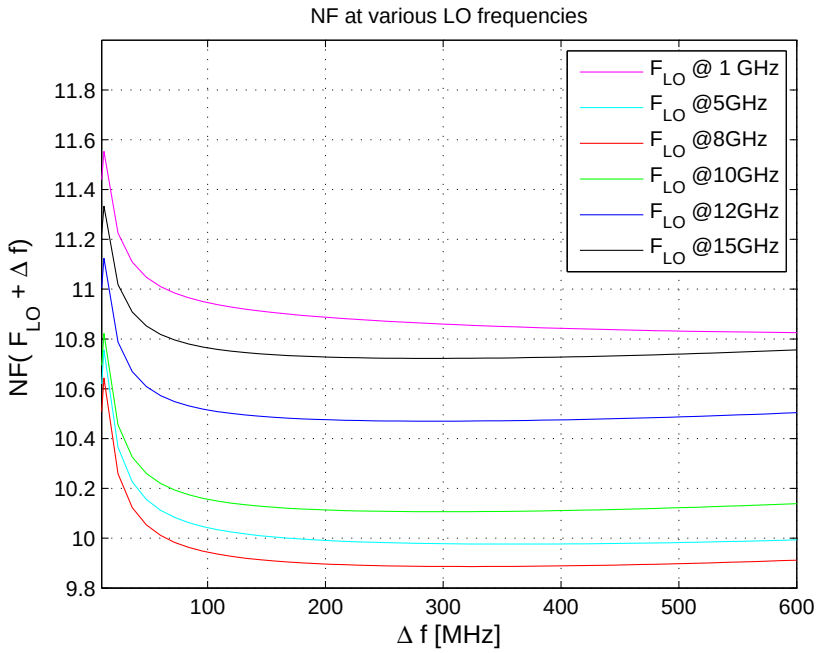

Figure 5.27: Noise figures obtained by sweeping the local oscillator frequency .

Noise Figure versus temperature

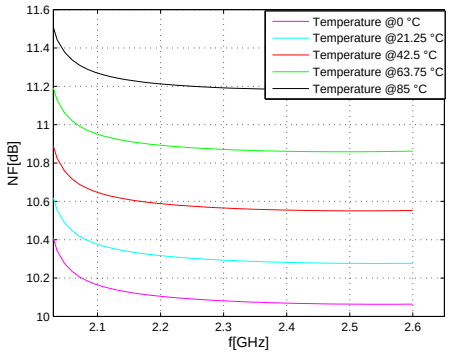

Figure 5.28: Noise figure with $f_{LO} = 2GHz$

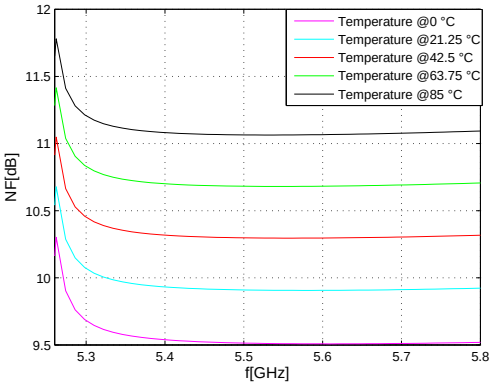

Figure 5.29: Noise figure with $f_{LO} = 5.25GHz$

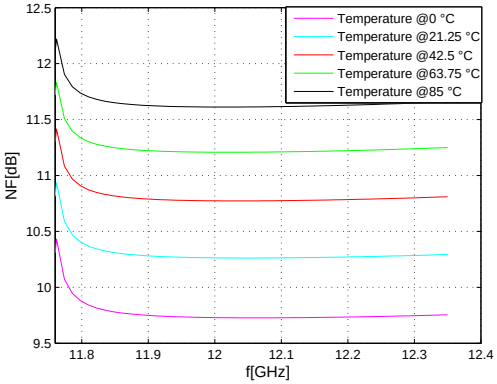

Figure 5.30: Noise figure with $f_{LO} = 11.75GHz$

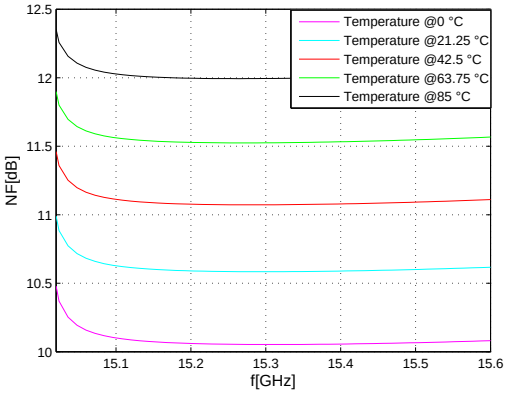

Figure 5.31: Noise figure with $f_{LO} = 15GHz$

Noise Figure versus voltage

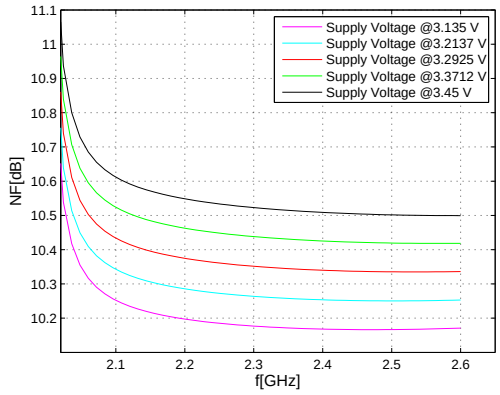

Figure 5.32: Noise figure with $f_{LO} = 2GHz$

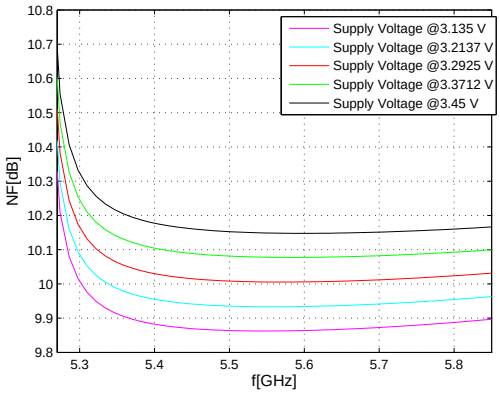

Figure 5.33: Noise figure with $f_{LO} = 5.25GHz$

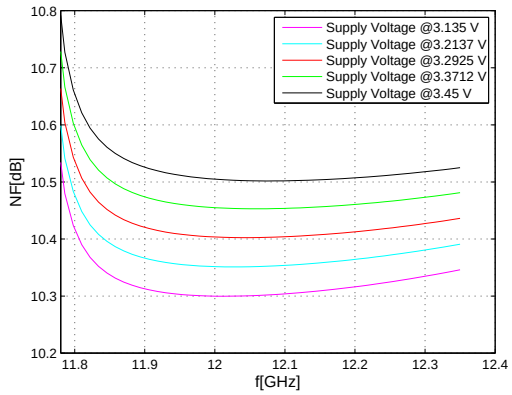

Figure 5.34: Noise figure with $f_{LO} = 11.75GHz$

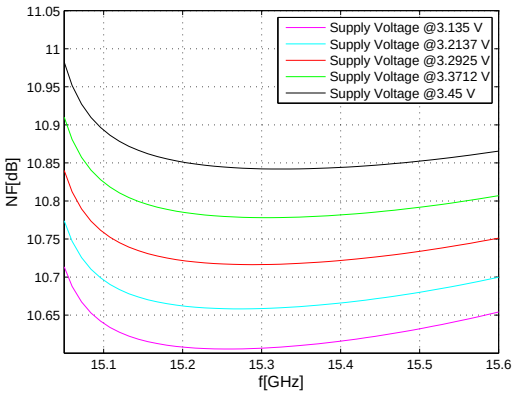

Figure 5.35: Noise figure with $f_{LO} = 15GHz$

Noise Figure obtained from MonteCarlo simulation

The following graphics represent the noise figure values obtained considering mismatch and process variations.

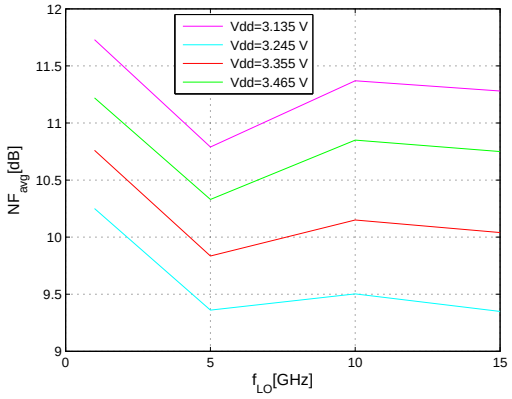

Figure 5.36: Noise Figure Average value

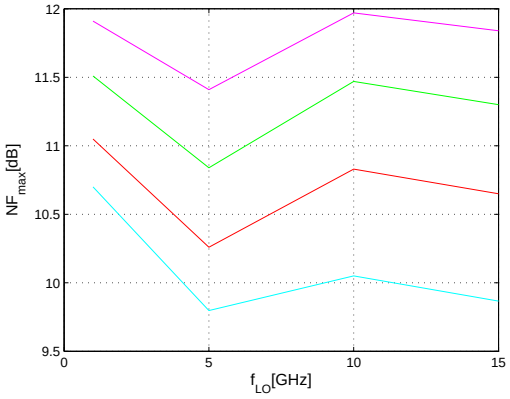

Figure 5.37: Noise Figure Worst case

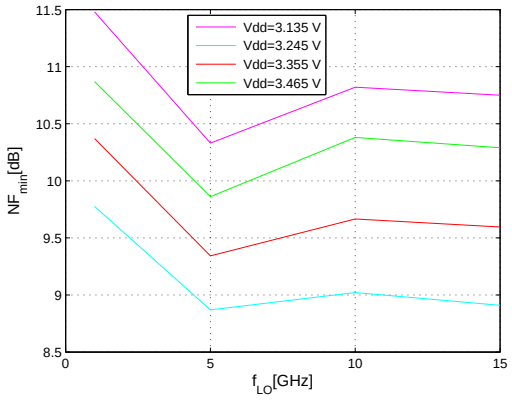

Figure 5.38: Noise Figure Best case

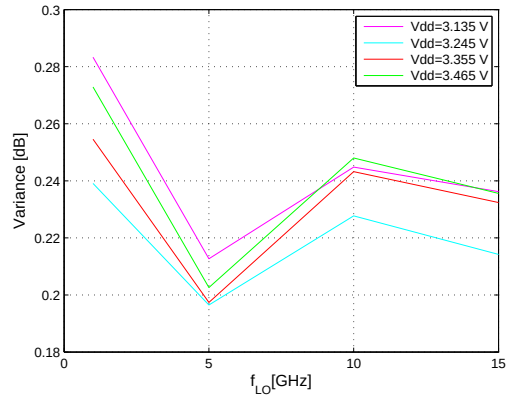

Figure 5.39: Noise Figure Std.Deviation

Conditions	$NF_{Min_{[dB]}}$	$NF_{Max_{[dB]}}$	$NF_{Mean_{[dB]}}$	$NF_{\sigma_{[dB]}}$
$f_{LO} = 1Ghz$				
$V_{dd} = 3.135V$	11.48	11.91	11.73	0.283
$V_{dd} = 3.245V$	9.76	10.70	10.25	0.240
$V_{dd} = 3.335V$	10.37	11.05	10.76	0.255
$V_{dd} = 3.465V$	10.87	11.51	11.22	0.273
$f_{LO} = 5Ghz$				
$V_{dd} = 3.135V$	10.33	11.41	10.79	0.212
$V_{dd} = 3.245V$	8.87	9.79	9.36	0.196
$V_{dd} = 3.335V$	9.34	10.26	9.83	0.198
$V_{dd} = 3.465V$	10.38	11.47	10.85	0.244
$f_{LO} = 10Ghz$				
$V_{dd} = 3.135V$	10.82	11.97	11.37	0.248
$V_{dd} = 3.245V$	9.02	10.05	9.503	0.23
$V_{dd} = 3.335V$	9.66	10.83	10.15	0.243
$V_{dd} = 3.465V$	10.38	11.47	10.85	0.244
$f_{LO} = 15Ghz$				
$V_{dd} = 3.135V$	10.75	11.84	11.28	0.244
$V_{dd} = 3.245V$	8.909	9.866	9.349	0.214
$V_{dd} = 3.335V$	9.596	10.65	10.04	0.232
$V_{dd} = 3.465V$	10.29	11.3	10.75	0.235

Table 5.1: MonteCarlo Table results.

5.4 Linearity

Conversion Gain

By sweeping LO frequency and the baseband input frequency the various conversion gain are here collected. At lower LO frequencies having a lower abrupt commutation the conversion gain is decreased. At higher LO frequencies the conversion gain suffers of the attenuation due to the frequency response of the whole mixer. The simulations are performed at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$.

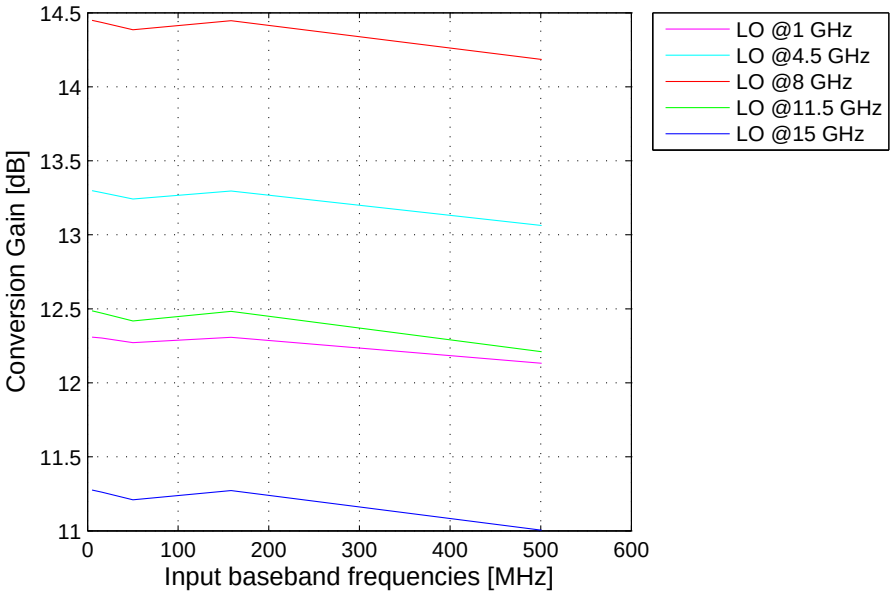

Figure 5.40: Conversion gains.

Compression Points

The compression point here presented at various LO frequencies by injecting a single baseband tone at $f_{bb} = 500MHz$. The simulations are performed at the nominal conditions of $T = 27°C$ and $V_{dd} = 3.3V$.

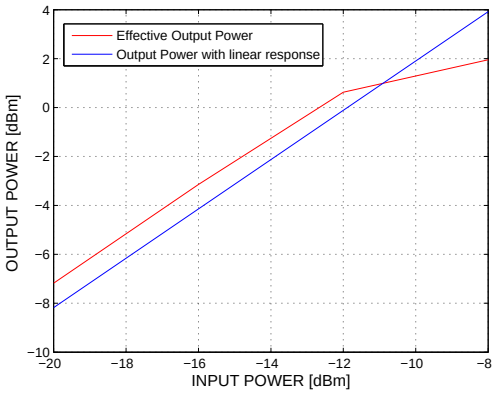

Figure 5.41: C.P. obtained with $f_{LO} = 1GHz$

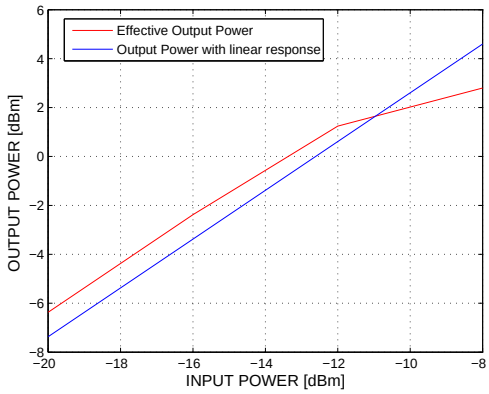

Figure 5.42: C.P. obtained with $f_{LO} = 5GHz$

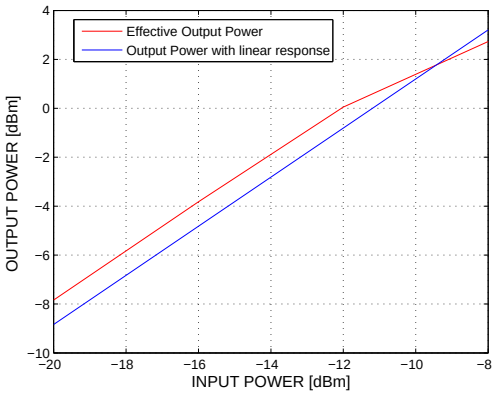

Figure 5.43: C.P. obtained with $f_{LO} = 10GHz$

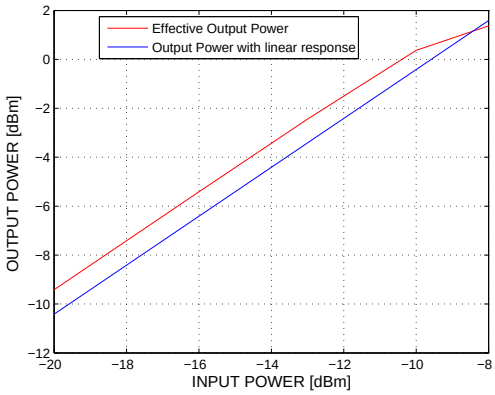

Figure 5.44: C.P. obtained with $f_{LO} = 15GHz$

OIP3

The OIP3 here collected are simulated by applying two tones at f_{bb_1} and $f_{bb_2} = f_{bb_1} + 1MHz$. The simulations are performed with $V_{dd} = 3.3V$ and $T = 27°C$. By sweeping the input frequency, the maximum of the linearity is reached when the input signal stands in the lower side of the baseband, when the linearity of the transconductor does not suffer of capacitor effects. On the other hand, when the local oscillator stands in the middle of its band is the optimal condition to achieve better linearity, in fact the conversion gain does not suffer of any attenuation due to the slower rise and fall time of the commutation driving the switching cell and the frequency response of the mixer does not inject any distortion over the harmonics of the output spectre.

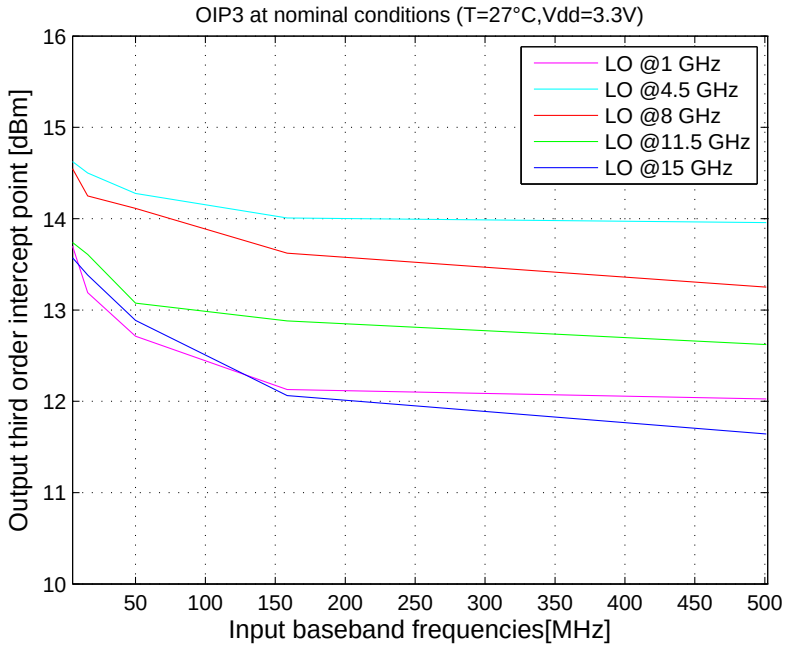

Figure 5.45: OIP3

OIP3 versus temperature and Supply Voltage

The OIP3 here collected are simulated by applying two tones at $f_{bb_1} = 501MHz$ and $f_{bb_1} = 503MHz$. By changing the LO frequency commuting the switching cell of both mixers, a simulation with temperature and voltage sweeping is run in order to detect the OIP3 of the system within various working conditions.

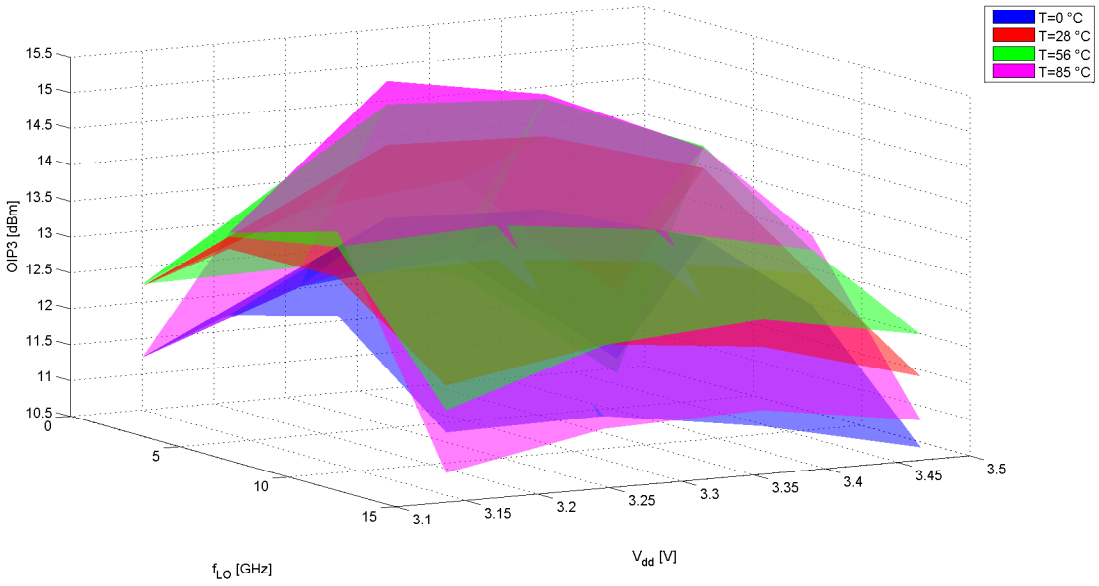

Figure 5.46: For all the executed configurations the OIP3 stands into the design targets.

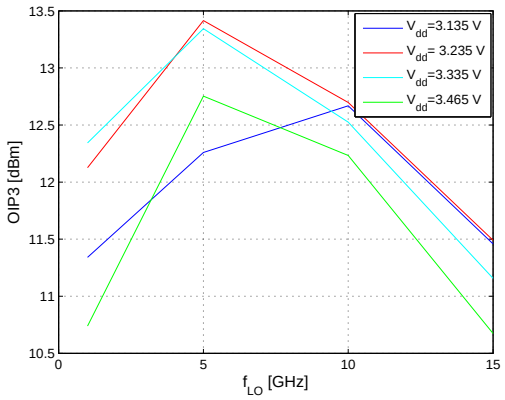

Figure 5.47: OIP3 obtained with $T = 0°C$

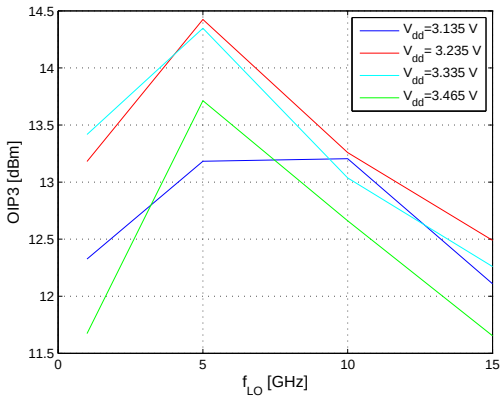

Figure 5.48: OIP3 obtained with $T = 28°C$

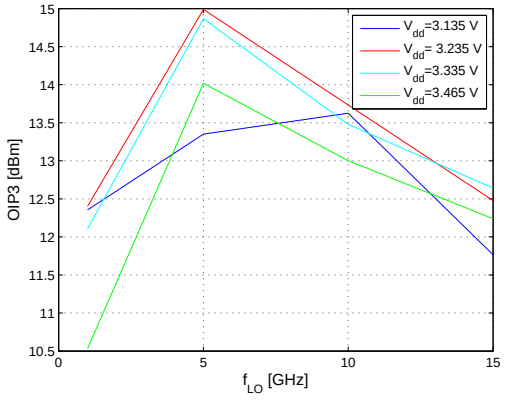

Figure 5.49: OIP3 obtained with $T = 56°C$

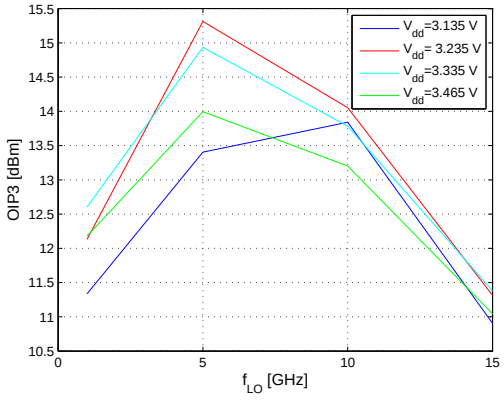

Figure 5.50: OIP3 obtained with $T = 85°C$

OIP3 Monte Carlo simulation with voltage and temperature sweeping

The OIP3s for various f_{LO} are extracted via Monte Carlo simulations. At the input of the the baseband ports are injected two tones at $f_{bb_2} = 501MHz$ and $f_{bb_2} = 503MHz$. The simulations are performed by sweeping of temperature and voltage.

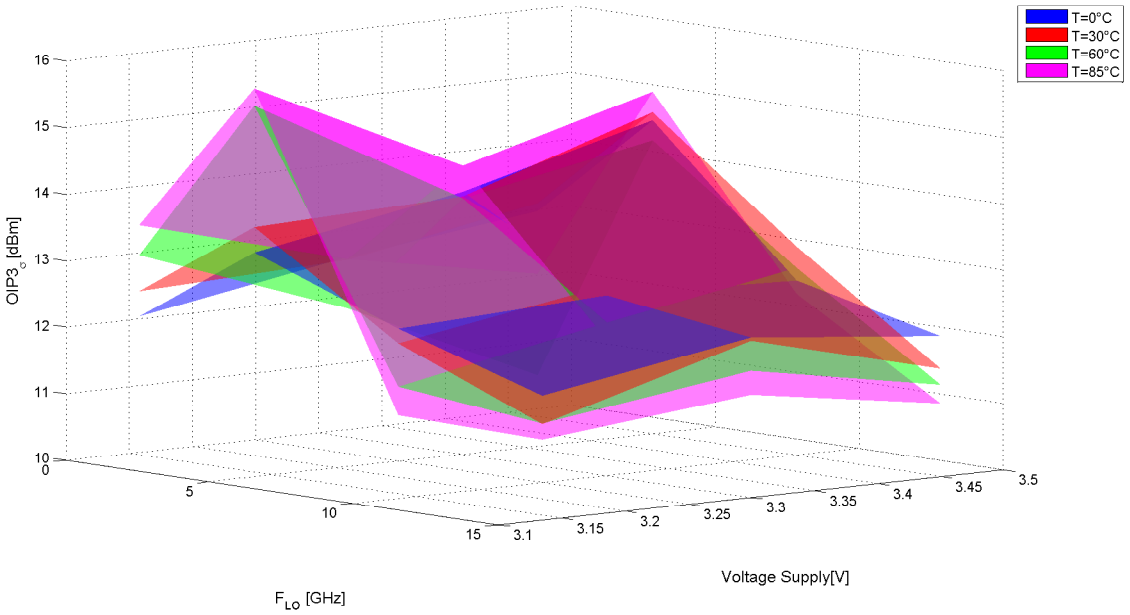

Figure 5.51: Average value of OIP3 obtained via Monte Carlo Simulation

As visible from Fig. 5.51 the minimum is reached at higher frequencies of assumed by the local oscillator driving the two mixers, and the maximum in the middle of the f_{LO} band.

The next figures represents the parameters describing the distribution assumed by the samples: minimum, maximum, mean value and standard deviation.

The reported parameters are simulated at the nominal voltage supply of 3.3V.

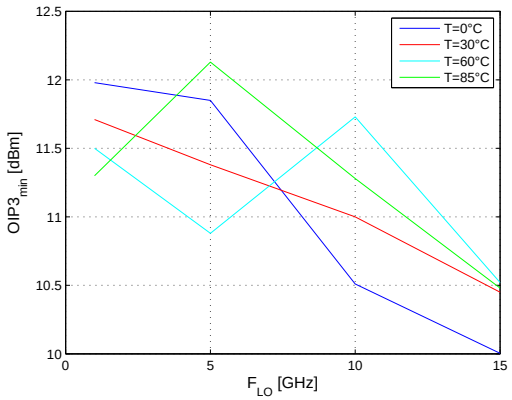

Figure 5.52: OIP3 Worst case

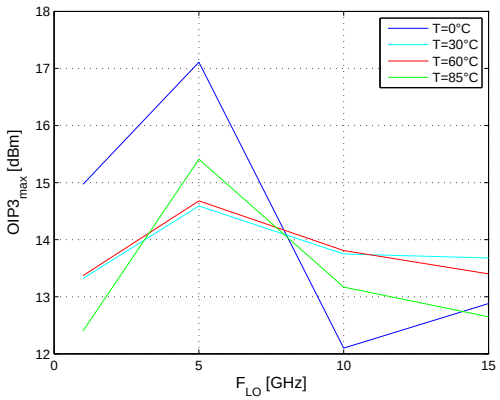

Figure 5.53: OIP3 Best case

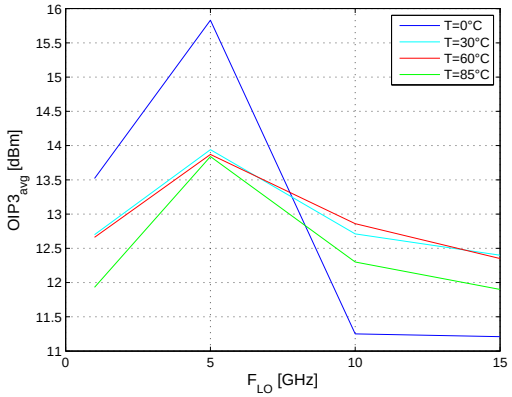

Figure 5.54: OIP3 Mean value

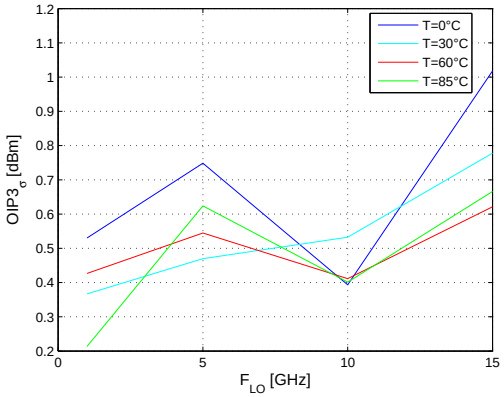

Figure 5.55: OIP3 σ value

The reported parameters are simulated at the nominal temperature of $30°C$.

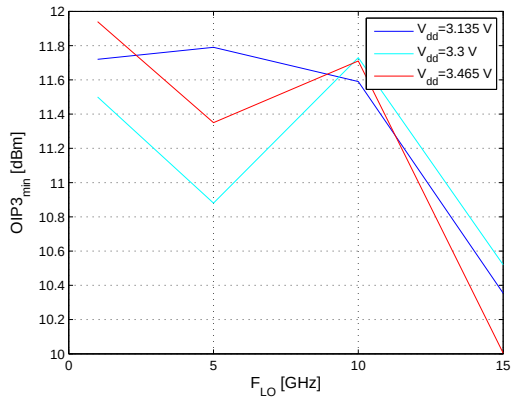

Figure 5.56: OIP3 Worst case

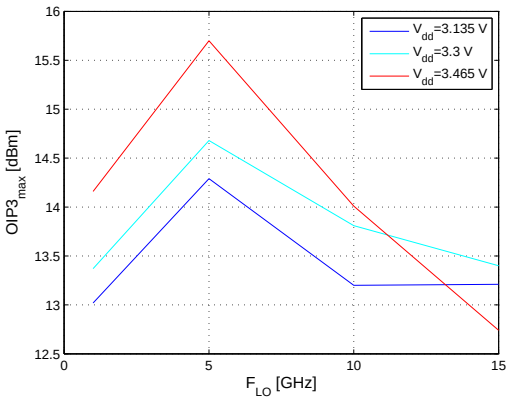

Figure 5.57: OIP3 Best case

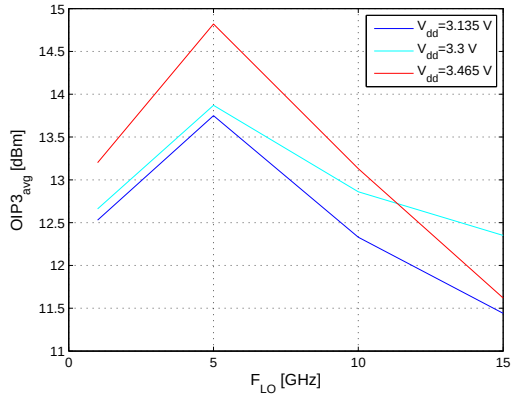

Figure 5.58: OIP3 Mean value

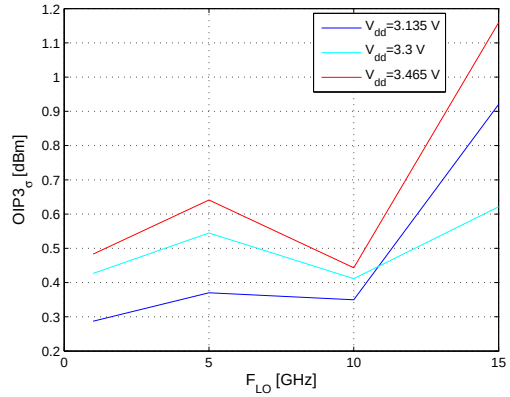

Figure 5.59: $OIP3_{\sigma}$ value

5.5 LO feedthrough and Image Reject Ratio

By theory if the system is perfectly balanced the LO feedthrough and Image Reject Ratio will assume $-\infty$ and $+\infty$ dBc value respectively. But taking into account the mismatches of the devices composing the system, the balancing condition is not still verified. So into the output signal spectre appears a component at f_{LO} and at the image harmonic $f_{LO} + f_{bb}$, where f_{bb} is the input tone injected at the input port.

Considering the device mismatches, and the variation of process the Image Reject Ratio and the Local Oscillator Feedthrough are measured. The Monte Carlo simulations are executed at various f_{LO}, applying at the input one tone at $f_{bb_1} = 500MHz$. The simulation collected are extracted by sweeping the temperature into a 0 to 85° C range, while the applied voltage supply sweeps into the ±5% variation of its nominal value (3.3V).

The reported parameters are simulated at the nominal voltage supply of 3.3V.

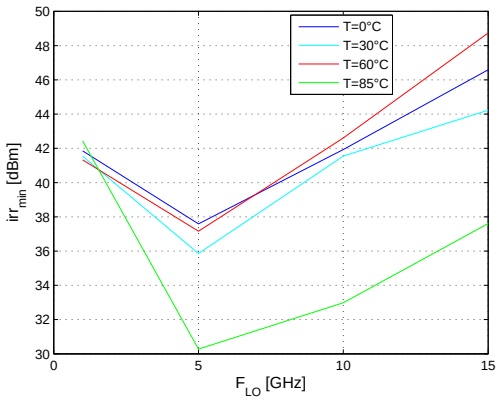

Figure 5.60: Image Reject Ratio Worst case

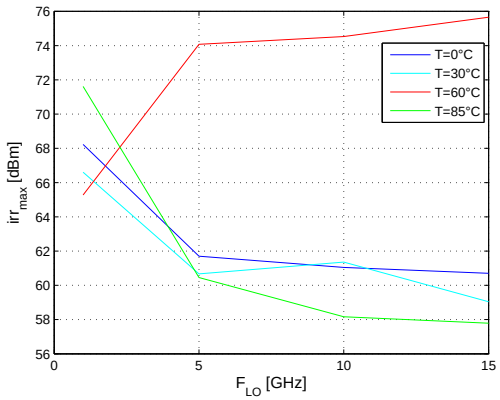

Figure 5.61: Image Reject Ratio Best case

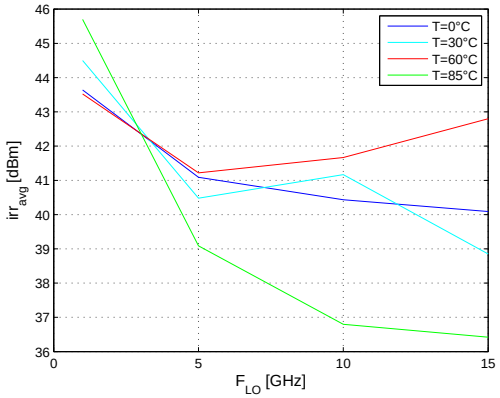

Figure 5.62: Image Reject Ratio Mean value

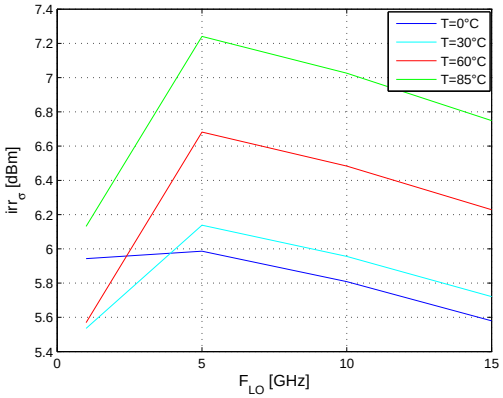

Figure 5.63: Image Reject Ratio σ value

The reported parameters are simulated at the nominal temperature of $30°C$.

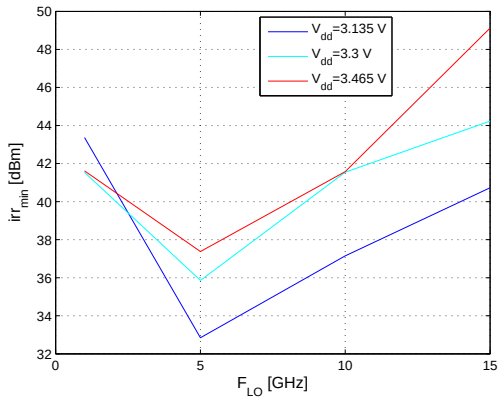

Figure 5.64: Image Reject Ratio Worst case

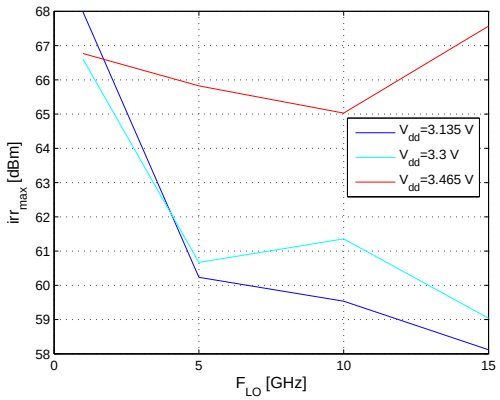

Figure 5.65: Image Reject Ratio Best case

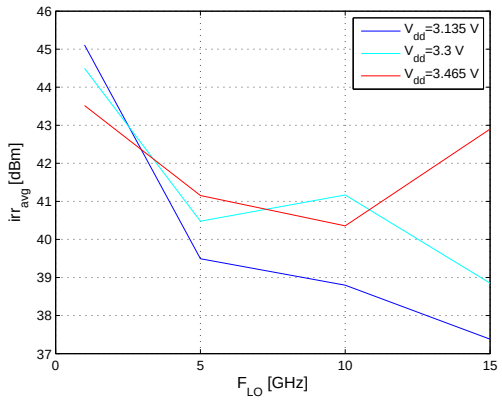

Figure 5.66: Image Reject Ratio Mean value

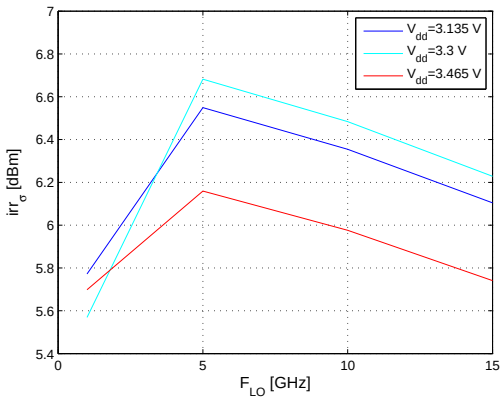

Figure 5.67: Image Reject Ratio σ value

The reported parameters are simulated at the nominal Voltage supply $V_{dd} = 3.3V$.

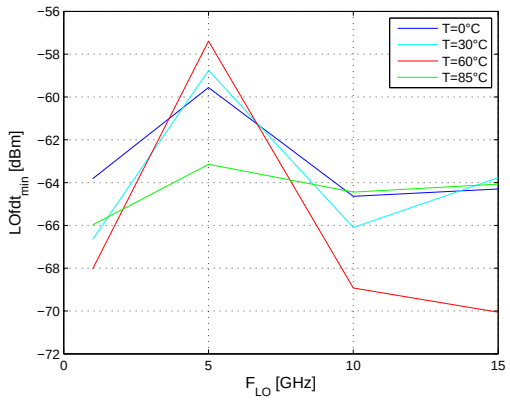

Figure 5.68: LO feedthrough Best case

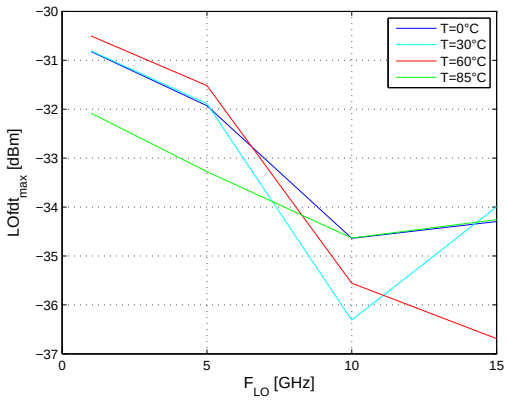

Figure 5.69: LO feedthrough Worst case

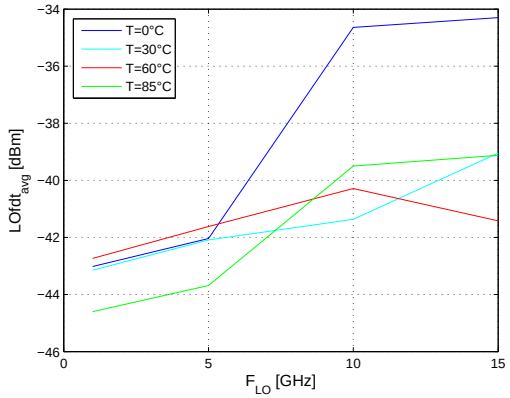

Figure 5.70: LO feedthrough Mean Value

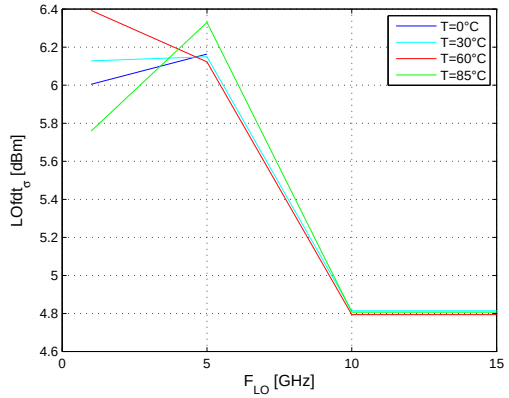

Figure 5.71: LO feedthrough σ Value

The reported parameters are simulated at the nominal temperature $T = 30°C$.

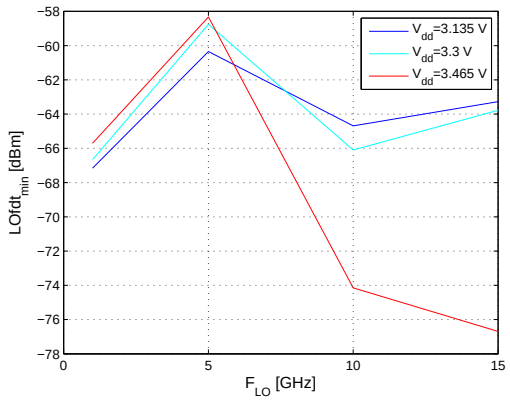

Figure 5.72: LO feedthrough Best value

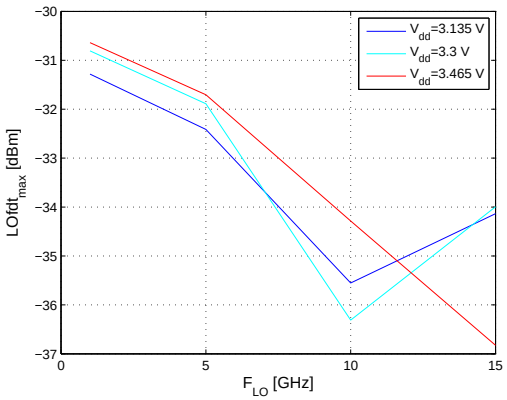

Figure 5.73: LO feedthrough Worst value

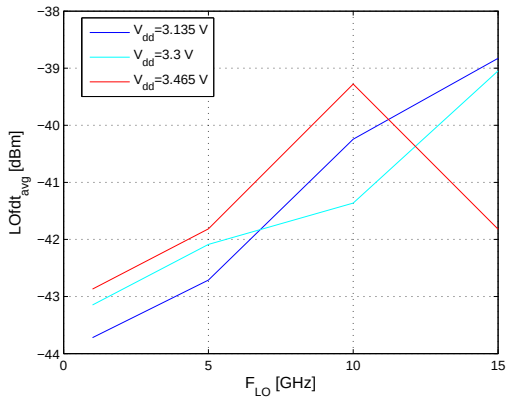

Figure 5.74: LO feedthrough Mean value

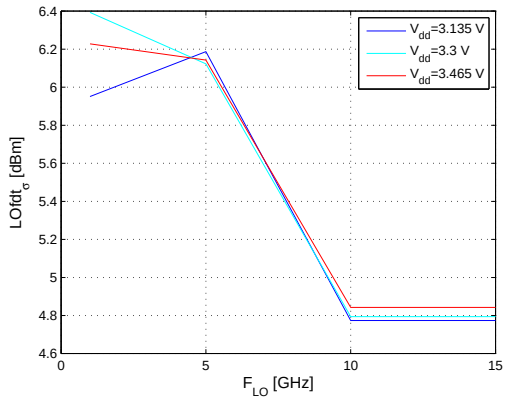

Figure 5.75: LO feedthrough σ value

5.6 MultiPath Polyphase Mixer simulation results

To find out, a suitable solution to suppress the spurs produced by the higher odd harmonics contained into the spectra of the local oscillator signal, which generates unwanted mixing, disturbing the transmission here are shown the simulation done by using the Multipath Polyphase Mixer previously discussed. The simulations employed to extract the output RF spectre of the Multipath Polyphase Mixer are set with two tone at the input $f_{bb_1} = 501MHz$ and $f_{bb_2} = 503MHz$ with the frequency of the quasi-square wave toggling at the switching port of both mixers at $f_{lo} = 4.1GHz$.

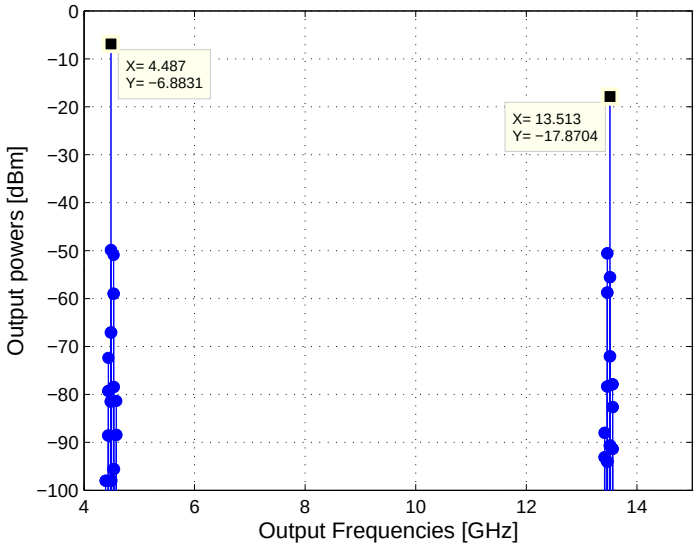

Figure 5.76: The spurs produced by a IQ modulator without polyphase harmonics suppression.

By following the design considerations assumed, the noise can be reduced by biasing all the mixer with a lower current, here is presented how the noise figure decreases consequentially. The trade-off is present in terms of linearity, as widely already discussed in the previous chapters.

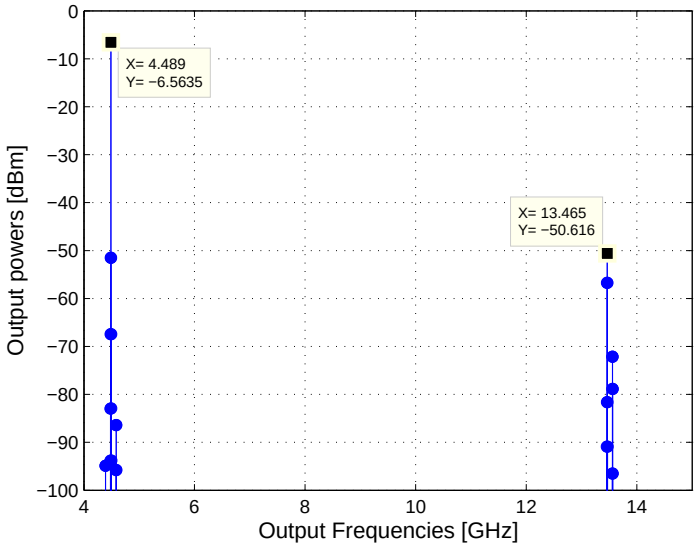

Figure 5.77: The harmonics suppression employed by the Multipath Polyphase Mixer (Fig. 3.42). In this case $OIP3 \simeq 15dBm$.

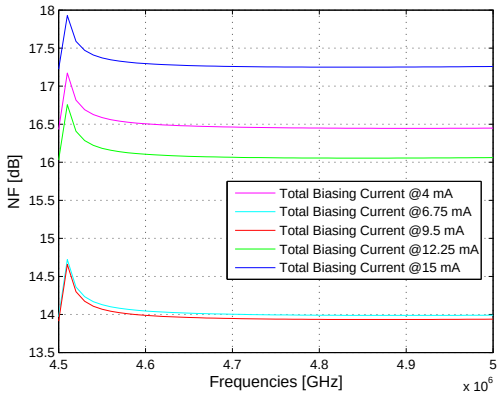

Figure 5.78: Noise figures obtained sweeping the biasing current

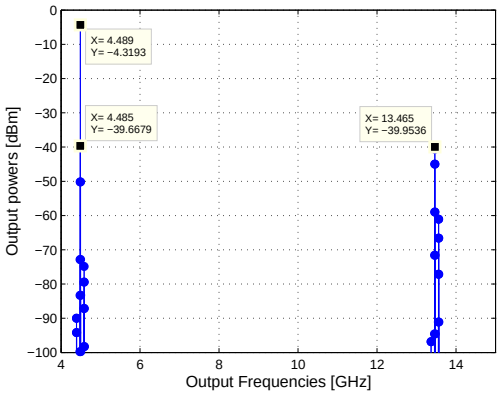

Figure 5.79: In this case $OIP3 \simeq 12dBm$.

Chapter 6

Summary

The presented work, underlines the various aspects of the design of a Wideband Upconverting IQ Modulator. The first chapter recalls the basic concept of the T/R modules employed in the most of transmission devices, which in the most of the case require a frequency translation, such describing a common application for the realized mixer structure. During the second chapter all the blocks composing the modulator are discussed from a theoretical point of view, analyzing their structures and features. Furthermore, the problem of the presence of spurs coming from unwanted mixing at higher harmonics is analyzed and the Multipath Polyphase Mixers are introduced. The third chapter concerns the design choices made in order to achieve the better dynamic range for the system. The input and output buffers are the first blocks discussed, then the active mixer and all its sub-blocks are analyzed, proposing a a noise canceling transconductor designed to maintain under limits the noise figure for all the frequencies of interest and by taking advantage of the low distortion nature of the available CMOS technology.

The obtained performances are here resumed.

	OIP3				***Noise Figure***
	1MHz	*50MHz*	*100MHz*	*500MHz*	
F_{LO}					
1GHz	13.7dBm	12.7dBm	12.3dBm	12.1dBm	10.8dB
5GHz	14.7dBm	14.5dBm	14.3dBm	14.3dBm	9.8dB
10GHz	13.7dBm	13.1dBm	12.9dBm	12.6dBm	10.1dB
15GHz	13.5dBm	12.6dBm	12.4dBm	11.8dBm	10.7dB

Table 6.1: Performances obtained at the nominal condition of $T = 27°C$ and $V_{dd} = 3.3V$

The wanted frequency translation, since it is performed in a wide band, does not present a costant shape and behavior in terms of dynamic range. It is clear, how the frequency conversion reaches is best quality for low frequencies baseband input signal and lo signals whose stand with frequencies around $5 \div 8GHz$, where the conversion gain does not suffer of slow raising/fall commutations and the frequency response of the overall system does not add further distortions to the produced signal.

When the LO signal toggles at low LO frequencies($\simeq 1GHz$) the system works at its noisiest configuration, also at the end of the LO band ($\simeq 15GHz$) the noise contribution is significantly since the frequency divider can not generate a quasi-ideal squarewave as at lower frequencies, due low-pass filtering performed by the inner parasitic capacitors found in the CML static frequency divider.

The total static power consumption of the Wideband IQ Modulator is of 439mW and chip area is of 930x930 μm^2.

By simulating the variation of process and mismatches, goals as LO feedthrough and Image reject ratio are verified (Fig. 6.2).

	LO Feedthrough [dBc]				***Image Reject Ratio [dBc]***			
F_{LO}	*Mean*	*Min*	*Max*	σ	Mean	Min	Max	σ
1GHz	-42	-70	-31	6.1	44	41	66	5.6
5GHz	-42	-58	-32	6.1	40	36	61	6.6
10GHz	-41	-66	-36	4.8	41	41	62	6.4
15GHz	-37	-62	-32	4.9	38	44	59	6.2

Table 6.2: Values extracted by the Monte Carlo simulation at the nominal condition of $T = 30°C$ and $V_{dd} = 3.3V$

At low frequencies to suppress the spurs produced by the hard driven switching cell, the filterless technique named Mulipath Polyphase Mixing is a flexible and suitable tools, which can implement a cleaner frequency upconversion within a wide dynamic range, with a further cost in terms of area effort and power consumption.

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