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Study and design of an inverters series configuration composed by three-phase and single-phase multilevel units for high power applications

(Studio e progettazione di una configurazione di inverter in serie composta da unità multilivello trifase e monofase per applicazioni a elevata potenza)

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Abstract

Many multilevel topologies have been proposed to overcome the power switches limitations. The purpose of this thesis is to study a multilevel configuration that couples two three-phase three-levels converters and three single-phase three-levels converters with the possibility to use different power sources guaranteeing a reliable operation and an high efficiency. The general control problem, interleaving benefits, balancing issues and magnetic component sizing have been studied and a solution has been proposed. The control strategy uses four classical PI (proportional integral) regulators considering the capacitor voltage controlled by external regulators. Interleaving has been applied obtaining in a certain optimal power condition an apparent switching frequency four times higher than the real one. A three-phase RLC circuit and a modified switching pattern are used for the three-phase and single-phase capacitors balancing. The structure stability have been proven with a stochastic simulation and the efficiency is estimated. Finally the non-conventional magnetic components have been studied and an example of design is reported.

Varie topologie multilivello sono state proposte per superare le limitazioni imposte dagli interruttori di potenza. Lo scopo di questa tesi è quello di studiare una configurazione che utilizza due unità a tre livelli trifase e tre unità a tre livelli monofase con la possibilità di sfruttare sorgenti diversificate garantendo un'operazione affidabile ed efficiente. Il problema generale del controllo, i benefici dovuti all'interleaving, i problemi di bilanciamento e il dimensionamento dei componenti magnetici sono stati studiati ed una soluzione è stata proposta. La strategia di controllo utilizza quattro classici regolatori PI (proporzionale integrale) considerando che la tensione dei condensatori sia controllata esternamente. L'interleaving è stato applicato ottenendo in una certa condizione di potenza generata una frequenza di commtazione apparente quattro volta maggiore di quella reale. Un ramo RLC trifase e un switching-pattern modificato sono utilizzati per il bilanciamento dei condensatori trifase e monofase. La stabilità della struttura è stata provata tramite simulazioni stocastiche e una stima dell'efficienza è stata riportata. Infine gli elementi magnetici non convenzionali sono stati studiati ed un esempio di progettazione è stato riportato.

Chapter 1

Introduction

Nowadays power electronics is diffused in many applications, covering a wide power range. Electronic converters are commercialized in standard and customized products as compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro-pumped storage, wind energy conversion, and railway traction, to name a few [1].
The multiple degrees of freedom in the control of the electrical parameters allows an electronic converter to optimally regulate voltages and currents that flow through a load, controlling at the same time active and reactive power fluxes and also other parameters depending on the application.
In renewable applications like solar and wind power plans the static converters are essential: in the former case the inverter allows the maximum power point tracking (MPPT) and obviously the conversion DC/AC, in the latter case grid-connected converters are widely used as essential power electronics devices, especially in wind power generation systems with variable speed constant frequency generators. With the PWM (pulse width modulation) strategies the grid power factor in the grid side can be controlled providing sinusoidal currents with low total harmonic distortion (THD) and bidirectional power transfer.
As regards the wind power situation, today the most popular large variable-speed wind turbines are rated around $1.5 - 3\ MW$. Neverthless larger wind turbines of $10\ MW$ are under development in order to reduce the wind power generations costs[3].
In the wind offshore case and in many other applications an high power converter is required, but the semiconductor technology has limited capability. The maximum current and voltage values tolerated by the most common commercial switches are shown in figure 1.1. The solution to increase the overall power produced by the static converter is to connect many converters together. Various connection schemes have been proposed in literature such:

- series and multilevel topologies;
- parallel topologies;

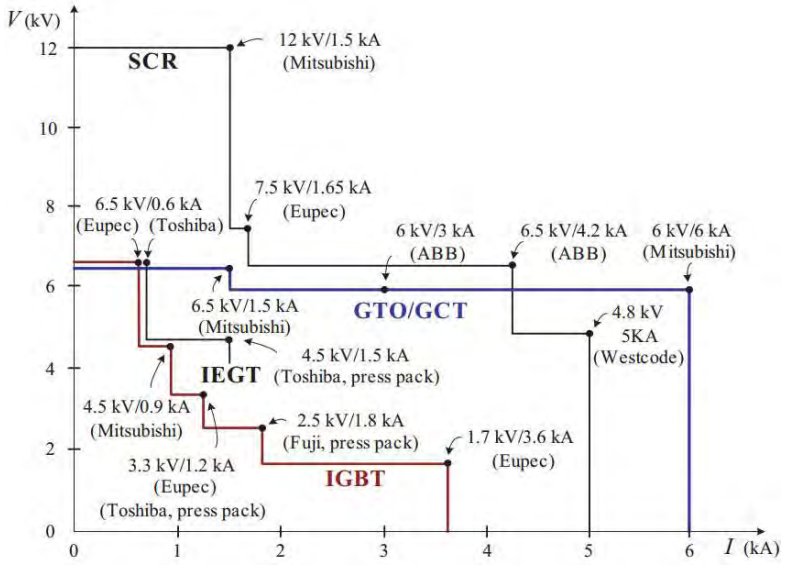


Figure 1.1: Switches limit performance [2].

- hybrid topologies.

The series topologies connect in series many converters generating multiple voltage levels with controllable amplitude, frequency and phase. In this way the voltage of each cell can be kept low while the total converter can reach high voltage levels.
In the parallel topologies two or more converters are paralleled increasing the total current produced by the inverter keeping the voltage value constant.
In the hybrid topologies both series and parallel connections are used in order to combine the advantages.
To obtain a comparison between the topologies many parameters have to be evaluated: THD, redundancy and fault tolerance, reliability, costs, weight and volume of the converter, dynamical behaviour, output power, output voltage, switching frequency.
Since in high power application ($P > 5\ MW$) the electrical inductors and transformers are designed for high currents and voltages, it becomes really important to minimize the filtering inductances and when it is possible, to remove the transformers. These goals have to be reached not only because of the costs of the electrical machines, but also because in applications like offshore wind power plants the reduction of the total weight of the structure is desirable.
The challenge is to find the optimal solution that addresses all these requirements. In this thesis the solution proposed in literature by *Laka et al.* is deeply studied to understand his potentiality and his limits.
The hypothesis on the grid parameters are discussed and a study case is chosen. All the parameters of the magnetic elements are discussed and estimated in order to understand if the studied case is feasible first, then when the economical and technical feasibility are

proven the effective detailed design is studied and the previous estimations are verified.
Regarding the *research and methodology* description, the main database that have been used to support the work is *IEEE Xplore* together with many doctoral thesis and on-line books provided by the *NTNU: Norges teknisk-naturvitenskapelige universitet* institution.
In chapter 2 the literature review analysis is reported with a brief explanation of the converter parallel concept, the most diffused multilevel topologies on the market and the modulation techniques.
Chapter 3 presents the studied topology focusing on the most important aspects and possibilities that this configuration offers in comparison to the conventional ones.
In chapter 4 the resistances and inductances associated to each component are estimated keeping a certain safety margin for the resistances.
An optimization algorithm is reported in chapter 5: through this process the reference values of deliverable power for all the DC sources is calculated considering all the technical and topological constraints and the optimal three-dimensional matrix of values is stored in look up tables.
In chapter 6 the general control structure is designed and simulated; two additional blocks to avoid high in-rush currents and to limit dynamically the direct and quadrature current are designed and discussed.
In chapter 7 the interleaving benefits are proven with a comparison between the with-interleaving simulations and without-interleaving simulations.
In chapter 8 the source models are discussed and the converter waveforms are studied; the first hypothesis of constant voltage sources generators is removed and the DC capacitors are designed. The capacitor balancing problem are studied and then different solutions are implemented in single-phase and three-phase converters and the circuit reliability is proven through initially unbalanced simulations. The converter then is simulated with stochastic sources in order to prove the stable operation and control robustness.
In chapter 9 the power transformer, zero sequence blocking transformer and filtering impedance are effectively designed and therefore the real electrical parameters are calculated.
In chapter 10 the total converter efficiency and harmonic spectrum are studied and the requirements according to the most common commercial standards are analyzed. Some ideas are also proposed to increase the converter efficiency.

Chapter 2

High power topologies

Series and parallel topologies are the basis to built hybrid converters. While in the parallel connection the circuit topology is well established, in the series connection many solutions have been proposed in literature with different drawbacks, thus the choice is weighted on the application. In this chapter the parallel concept will be firstly discussed, reporting the related issues and the solutions that have been proposed in literature. After that the classical multilevel topologies are shown comparing advantages and drawbacks. Finally the most diffused hybrid topologies are presented.

2.1 Converters paralleling

2.1.1 Parallel concept

The easiest idea to connect many converters in order to increase the output power is to built a parallel topology: this solution could be obtained either connecting multiple power switches or multiple converters in parallel. According to [3] in the former solution the biggest challenge is to guarantee equal voltage or current sharing, while in the latter interleaving techniques are usually used in order to improve the output waveforms. In

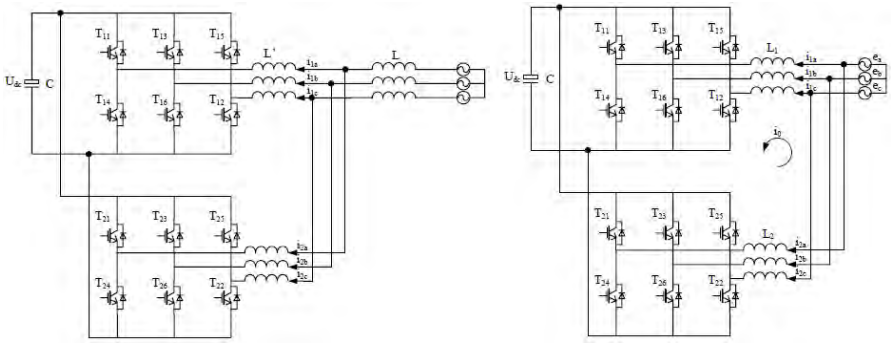


Figure 2.1: Typical parallel scheme with shared DC capacitor [3].

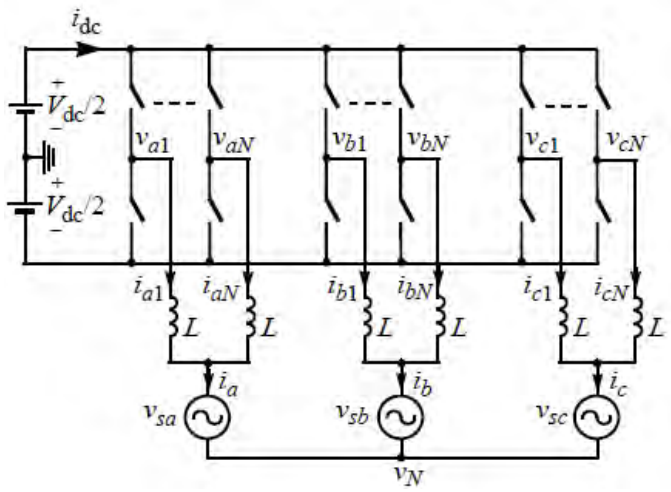


Figure 2.2: General parallel of N converters [6].

figure 2.1 a typical converter parallel connection is depicted. It is easy to understand that the power rating might be extended by adding a new converter unit; this modular configuration ensures a reliable system because of the redundancies.
When two or more converters are connected in parallel a closed path is created for a zero sequence circulating current. This current is harmful because it increases the switches stress and may lead to low harmonics if the passive components like the filter inductances are slightly different. The easiest way to avoid this current is to use separated DC sources or multi-windings transformer in the AC side, but this solution is expensive and also increase the weight of the system. Many other solutions have been proposed in literature to mitigate this current: the most diffused use a modified PWM scheme especially when the space vector modulation is applied [4]. Other methods propose a PI controller that has the role to reduce the low frequency zero sequence current [3] shifting the modulation wave vertically. Asiminoaiei proposed in [5] to use common mode inductors to reduce the circulating current between parallel converters. These coupled inductors are three-phase inductors wounded on the same magnetic core, also referred as zero sequence blocking transformers: the positive and negative sequence produce a null flux inside the magnetic core and therefore the impedance seen is low because is only due to the leakage fluxes. The zero sequence component produce a net flux inside the magnetic core with a limited value because the zero sequence current is only a low percentage of the positive sequence current. This means that the impedance seen by the zero sequence is high and the size of the magnetic element remains small.

2.1.2 Interleaving

When many converters are connected in parallel, the first idea could be to apply to all the converters the same modulation strategy at the same time; in this case the equivalent

converter is exactly the same of one converter with the current multiplied by the number of converters. Even if a current close path is produced (neglecting eventual asymmetries) there is no current that flows between the converters. Interleaving is often applied in order to improve the output waveform: the main concept is to shift the carriers of each converter in order to eliminate $N-1$ output harmonics. The interleaving theory and its effects have been widely explained in literature and the considerations made in [6] are reported to understand how interleaving affects the output waveforms.
Using the double Fourier series method and considering the PWM modulation for the phase a of the k^t converter the voltage referred to the ground is:

$$v_{ak}(t) = \frac{V_{dc}}{2} M \cos(\omega_1 t + \phi_1) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} C(m,n) \cos[m(\omega_c t + \phi_{ck}) + n(\omega_1 t + \phi_1)] \quad (2.1)$$

where the function $C(m,n)$ is calculated as:

$$C(m,n) = \frac{2V_{dc}}{\pi m} J_n\left(m\frac{\pi}{2}M\right) \cdot \sin\left[(m+n)\frac{\pi}{2}\right] \quad (2.2)$$

and V_{dc} is the DC link voltage, ϕ_1 is the initial phase angle of the reference voltage, M is the modulation index, N is the number of paralleled converters, ω_c is the switching frequency, m is the multiplier of the fundamental frequency, J_n is the Bessel function of the first kind [6]. The optimal interleaving angle will be demonstrate to be $1/N$ and therefore considering the first carrier phase angle $\phi_{c0} = 0$:

$$\phi_{c(k+1)} = \phi_{ck} + \frac{2\pi}{N} \;\rightarrow\; \phi_{ck} = \frac{2\pi}{N}(k-1). \quad (2.3)$$

The common mode voltage in the time-domain can be computed:

$$v_{cm}(t) = \frac{1}{N} \sum_{k=1}^{N} \frac{v_{ak} t + v_{bk}(t) + v_{ck}(t)}{3}. \quad (2.4)$$

Rewriting equation 2.4 using equation 2.1 with the phase shift angle defined in 2.3 each summation over k is non-zero only if m is a N multiple. Therefore the common mode voltage can be written as:

$$v_{cm} = \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} C(Nm, 3n) \cos[Nm\omega_c t + 3n(\omega_1 t + \phi_1)]. \quad (2.5)$$

From the equation above the harmonics components in the common mode voltage appear in bands centred at N multiples of the carrier frequency. Interleaving eliminates (N-1) carrier sidebands every N carrier sidebands.
Considering the source neutral floating the common mode voltage appears as the neutral voltage v_n. The harmonic components of the phase current are determined by the difference between the phase harmonic and the common mode voltage; this voltage difference is:

$$\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} C(Nm, n) \cos[Nm\omega_c t + n(\omega_1 t + \phi_1)], \quad (2.6)$$

and considering $i = \int \frac{v}{L} dt$ the expression becomes:

$$\sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0,\pm 3..}}^{\infty} \frac{C(Nm,n)N}{(nM\omega_c + n\omega_1)L} \sin[Nm\omega_c t + n(\omega_1 t + \phi_1)] \tag{2.7}$$

As shown in equation 2.7 the harmonic content of the phase current is similar to the one obtained for the common mode voltage: with N interleaved modules the harmonics in each phase current are centred at the N multiples of the carrier frequency.
Interleaving is particularly desirable in high power applications where the switching frequency is limited because of the power losses connected to high values of currents and voltages. However applying this technique each converter operates asynchronously in relation to the others and therefore a circulation current raises between the converters.

2.1.3 Circulating current

Considering two paralleled converters and considering s_{1x} and s_{2x} to be the switching functions and $L1$ and $L2$ the inductances of converter 1 and 2 respectively, according to Kirchoff's law the equations are:

$$\begin{cases} L1\frac{di_{1a}}{dt} + s_{1a}\frac{Udc}{2} - L_2\frac{di_{2a}}{dt} - s_{2a}\frac{U_{dc}}{2} = 0 \\ L1\frac{di_{1b}}{dt} + s_{1b}\frac{Udc}{2} - L_2\frac{di_{2b}}{dt} - s_{2b}\frac{U_{dc}}{2} = 0 \\ L1\frac{di_{1c}}{dt} + s_{1c}\frac{Udc}{2} - L_2\frac{di_{2c}}{dt} - s_{2c}\frac{U_{dc}}{2} = 0 \end{cases} \tag{2.8}$$

Summing these equations and defining the zero sequence current and zero sequence switching function as follows:

$$\begin{cases} i_0 = \frac{(i_{ia}+i_{ib}+i_{ic})}{3} = -\frac{i_{2a}+i_{2b}+i_{2c}}{3} \\ s_{10} = \frac{(s_{1a}+s_{1b}+s_{1c})}{3} \\ s_{20} = \frac{(s_{2a}+s_{2b}+s_{2c})}{3} \end{cases} \tag{2.9}$$

the zero sequence equation can be written:

$$(L1 + L2)\frac{di_0}{dt} = (s_{20} - s_{10})\frac{U_{dc}}{2}. \tag{2.10}$$

In figure 2.3 the zero sequence voltage difference represented by equation 2.10 is depicted when two converters are used with the optimal interleaving of 180°. This voltage difference is periodic with period Ts and therefore a circulating current with the switching frequency is produced, increasing the switching stress. If a low zero sequence impedance load is connected, as a three-phase three limbs transformer, these zero sequence currents may be large. Methods like the selective harmonic elimination (SHE) could be used to delete the triplen harmonics, but it is worth to reduce the 5^{th} and 7^{th} while the triplen should be reduced in other ways. An useful device for this purpose is the zero sequence blocking transformer ($ZSBT$) also called common mode inductor.

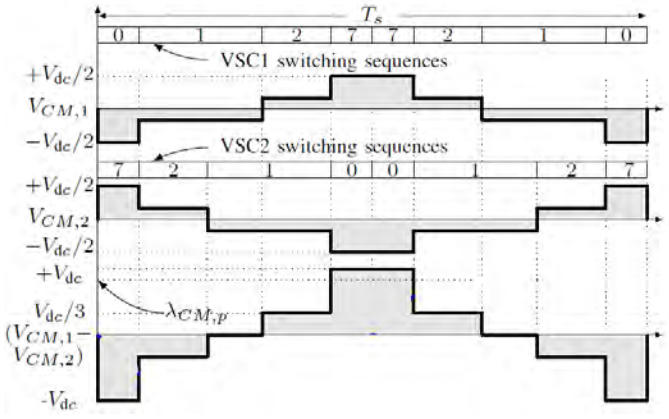


Figure 2.3: Zero sequence voltage difference when SVM with two interleaved converters is applied [4].

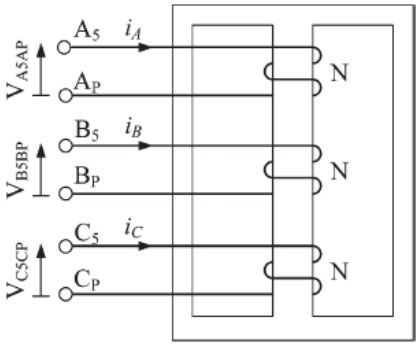


Figure 2.4: Zero sequence blocking transformer simplified scheme [7].

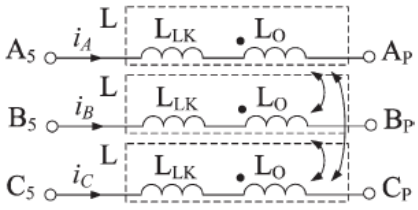


Figure 2.5: ZSBT equivalent scheme [7].

2.1.4 Zero Sequence Blocking Transformer (ZSBT)

The zero sequence blocking transformer is formed by three closely coupled coils that are wounded on the same magnetic limb, as shown in figure 2.4. According to [7] neglecting the core losses the equivalent model is represented in figure 2.5. Considering the mutual inductance to be $M = k \cdot L$ where k is the coupling coefficient, L is the single winding inductance and the leakage inductance becomes $L_0 = (1 - k) \cdot L$. The matrix equation is:

$$\begin{bmatrix} v_{A5-AP} \\ v_{B5-BP} \\ v_{C5-CP} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \cdot \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + \begin{bmatrix} L_0 + M & M & M \\ M & L_0 + M & M \\ M & M & L_0 + M \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{2.11}$$

Considering the positive and negative sequence, the sum $i_A + i_B + i_C$ is equal to zero and therefore the ZSBT offer a low impedance since all the mutual contributes cancel each other out and the only term that remains is the one associated to the copper losses and the leakage inductance. The matrix notation in the differential mode is:

$$\begin{bmatrix} v_{A5-AP} \\ v_{B5-BP} \\ v_{C5-CP} \end{bmatrix}_{dm} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \cdot \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + \begin{bmatrix} L_0 & 0 & 0 \\ 0 & L_0 & 0 \\ 0 & 0 & L_0 \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{2.12}$$

Considering the zero sequence component, the relation that rules the currents is $i_A + i_B + i_C = 3 \cdot I_0$, where I_0 is the zero sequence current. The equivalent impedance presented for the zero sequence is $3 \cdot M \approx 3 \cdot L$. It is important to achieve a good symmetry of the ZSBT in order to obtain a good cancellation of the fundamental flux. The magnetizing impedance is chosen to be high in comparison to the one imposed by the load (three limbs transformer). To guarantee that the zero sequence is not injected into the grid side if the wye connection is necessary, a tertiary winding on the power transformer could be used in order to create a short circuit for the zero sequence current.

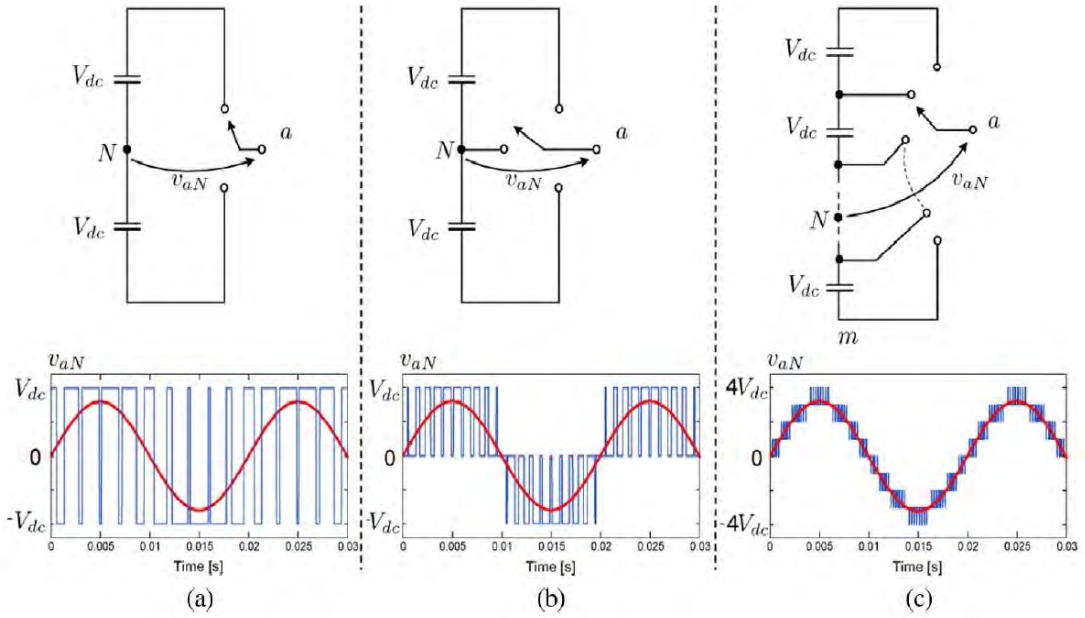


Figure 2.6: Phase-neutral output voltage of the converter: a) 2 levels, b) 3 levels, c) 9 levels [1].

2.2 Classic multilevel topologies

To better understand the advantages in the multilevel technology, it is necessary to report the basic multilevel topologies. The first multilevel converter was the CHB (Cascaded H-bridge), introduced in the late 1960s. The follower was the FC (Flying Capacitor) and the last the three levels NPC (Neutral Point Clamped). The three basic topologies are shown in figure 2.7.

The concept of the multilevel technology can be easily understood starting from the well known two-level inverters. In the classical two-level converter only two switches for each leg are used (six switches with three phase inverter). To create a specific waveform the switches have to be turned on and off many times in each period, according to the modulation strategy used. As shown in figure 2.6 *a*, the real output voltage is a rectangular wave with two possible values: $(+Vdc, -Vdc)$. Developing this waveform (periodic) with the Fourier's series all the harmonics component will be found. The closer to a single frequency spectrum the waveform is, the better operational behaviour the converter has. The currents have low harmonic distortion because of the inductive filtering elements and the inductive loads. According to [8], the multilevel topology follows the same principle of the simple two-level inverter, but has the advantage to provide an high-quality power achieved by generating several voltage levels. In figure 2.6 *b* and *c*, the power semiconductors are depicted with a three-state and a multi-state

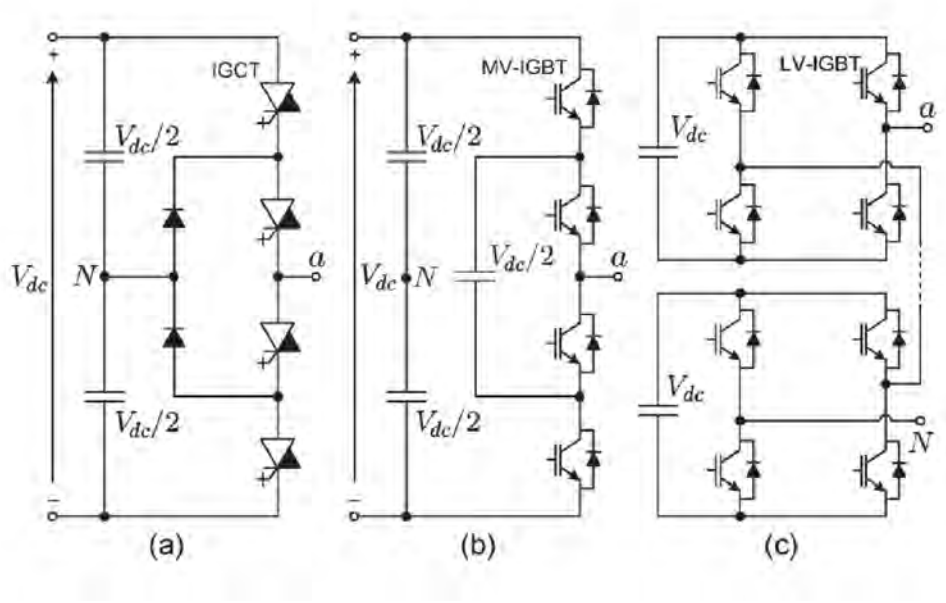


Figure 2.7: Basic multilevel converter topology. (a) 3L-NPC; (b) 3-L FC; (c) 5 level CHB [1]

.

switch: the output waveform is composed by steps with amplitude equal to Vdc. With multiple levels produced, the output fits better the pure sinusoidal wave; this leads to a reduction of THD, of the voltage derivative (dv/dt) and of the size of the output filters (in the two-level case). As always happens in technical applications, the converter number of levels have to be optimized: if more levels are chosen the THD is reduced while the costs and the complexity are increased.
Each of this topologies has advantages and disadvantages, here briefly presented.

2.2.1 3L-NPC: neutral point clamped

According to [8] the 3L-NPC converter consists in two traditional two level converters connected together: as in figure 2.8, the negative bus of the upper converter coincides with the positive bus of the lower converter while the original output phases are connected to the neutral point using two clamping diodes, dividing the DC-link voltage in two parts. Each power converter must be able to block only half DC-voltage, allowing the doubling of the total power keeping the same semiconductor technology. As shown in figure 2.9, the neutral point enables the generation of the "zero voltage level" obtaining three voltage levels (considering the phase to neutral voltage) using a defined switching state combination. Only two gate signals for each converter leg are necessary while the other switches receive the opposite gate signal to avoid short-circuits. The state $(S_{a1}, S_{a2}) = (1, 0)$ is not used since no current path for the load is generated in this case.

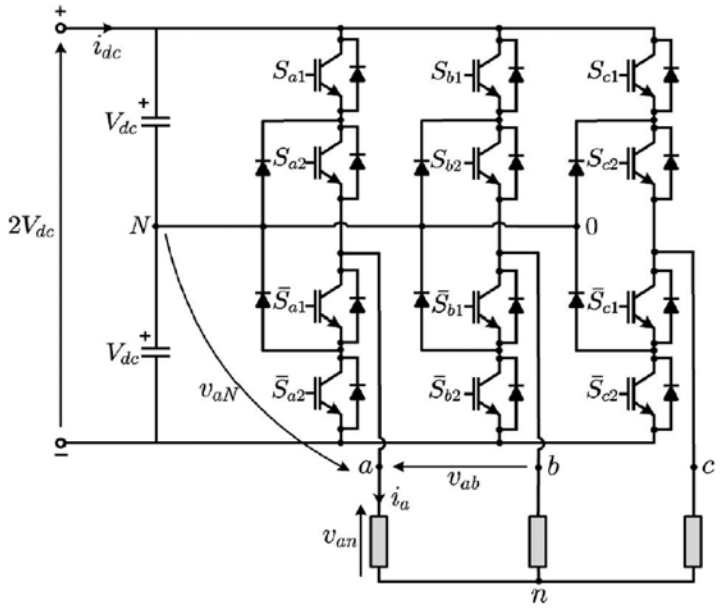


Figure 2.8: 3 level NPC circuit [8].

The DC unbalance issue is worth to be mentioned: when the load is connected to the neutral, the load current flows trough one capacitor, creating an unbalanced circuit. The DC-balancing must be controlled for a good operational behaviour.
Theoretically using this connection scheme an high number of levels can be reached, increasing the number of diodes to support higher voltages. Figure 2.10 shows that the number of devices increase dramatically: this means higher costs and a more complicated scheme to control the voltage unbalance on the capacitors. Because of these reasons only the three level NPC topology is quite diffused. A common example could be the ABB AC-DC-AC converter for wind power plants that uses IGCT switches and reach a power of 9 $[MVA]$ with 3.3 $[kV]$ AC voltage without converter paralleling [12].

A brief summary of the NPC features is here presented, as reported in [1] and [8]:

Advantages

- High voltages can be reached;
- low THD and dv/dt;
- simple rectifier system required.

Disadvantages

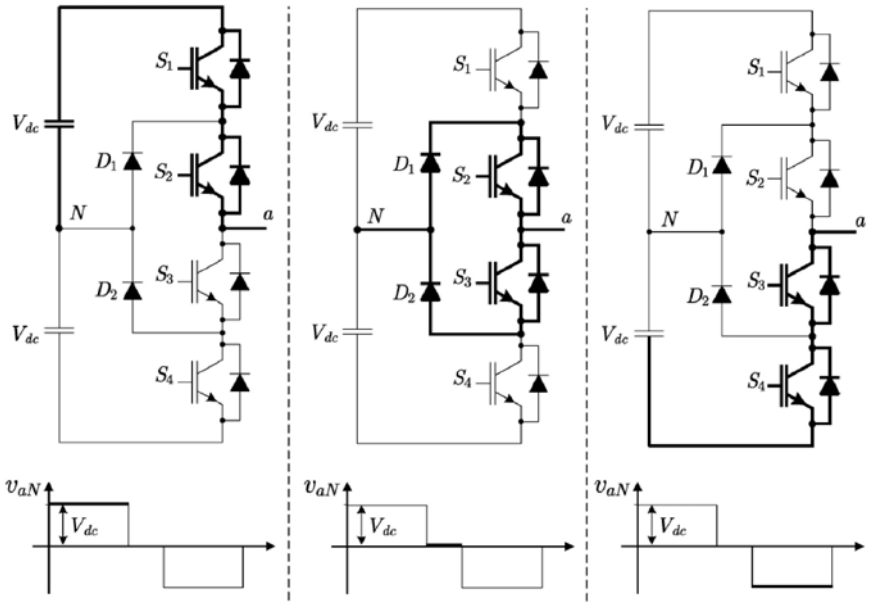


Figure 2.9: Switches states for 3L-NPC [8].

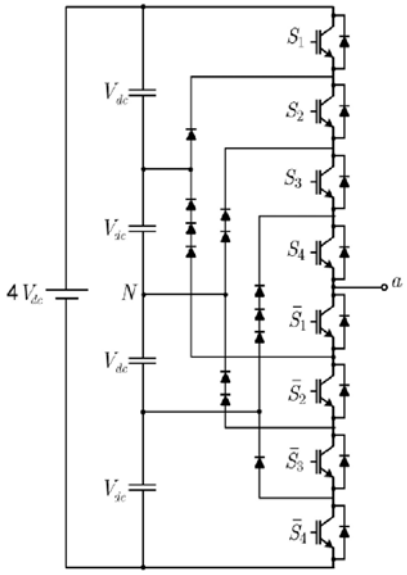


Figure 2.10: 5 level NPC scheme [8].

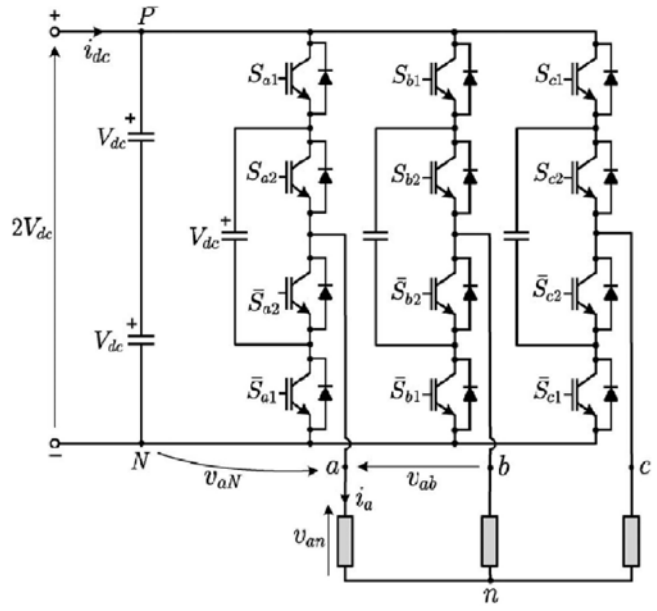


Figure 2.11: 3 levels FC scheme [8].

- Increasing the number of levels the number of components increases dramatically;
- High conduction losses (due to high number of devices);
- Uneven losses distribution and unequal voltage stresses due to the current that flows trough the neutral (avoided with special voltage balancing techniques);
- DC capacitors limit the maximum voltage level achievable;
- Scheme is not redundant (a failure in one switch will affect the overall converter operation).

2.2.2 3L-FC: Flying capacitor

In [8] the authors explain that the scheme of the flying capacitor (FC) is similar to the NPC structure, with the clamping diodes replaced by capacitors: in this topology the zero state is created indirectly connecting the load arms with the positive or negative DC bus trough a capacitor charged with an opposite voltage. Like the NPC, only two gate signals are necessary to command the switches of one arm while the others switches receive the opposite signal to avoid short-circuits. In this topology the state $(S_{a1}, Sa2) = (1, 0)$ is used in order to control the voltage balance of the flying capacitor. An higher switching frequency (e.g. higher than $1200Hz$) compared to the NPC and CHB schemes is required, thus self-balancing or control-assisted balancing modulation strategies can be applied to actively control the capacitors voltages. Due to the more complex control strategy and

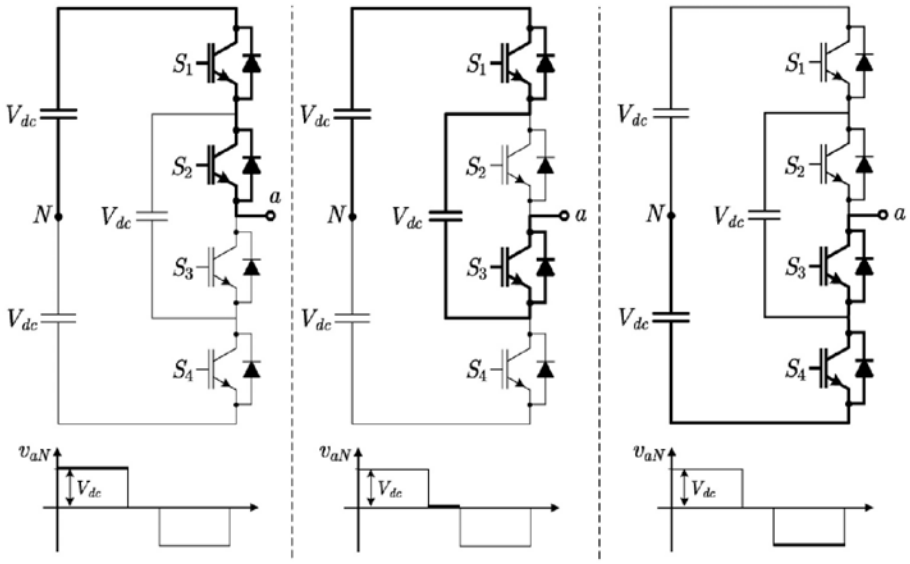


Figure 2.12: Switches states for 3 levels FC [8].

the capacitor voltage initialization this topology is less diffused than the NPC and the CHB and the power reached is limited ($2.24MW$ for 4L-FC [1]).

The advantages of this multilevel scheme are the modularity construction as shown in figure 2.13: it is easy to obtain more voltages levels adding new cells based on one capacitor and two switches. Developing special switching patterns it is also possible to get an asymmetrical multilevel system (with asymmetrical voltage levels): in this configuration the redundancies are reduced (and also the modularity) but the output voltage quality is increased keeping constant the number of semiconductors used.

The summary of advantages and disadvantages is presented, according to [1] and [8]:

Advantages

- Reduced number of devices;
- modular configuration;
- good performance with high and low modulation index.

Disadvantages

- Many capacitors required;
- capacitor voltage balancing systems required;

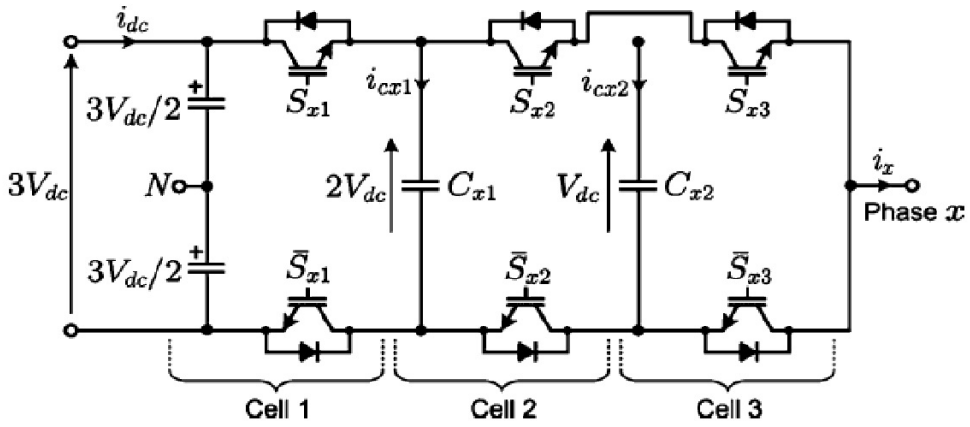


Figure 2.13: 4 levels FC: modular structure [8].

- capacitor voltage initialization systems required;
- high switching frequency increases the losses (model not suitable for high power).

2.2.3 CHB: Cascaded H-bridge

Referring to [8] the cascaded H-bridge configuration is obtained connecting in series more single phase H-bridge cells as shown in figure 2.15; the line to line voltage is the converter output. With four switches for each cell, four combinations are possible but only three levels can be achieved by every cell: this means that two combinations are redundant. The devices of every leg must be driven with opposite signals to avoid short-circuit (see figure 2.15). The major advantage of this topology is the high number of levels reached: with k H-bridges series connected, $2k+1$ levels are obtained. This scheme also introduce an higher level of redundancy since every converter has one redundant state and others are added due to the series connection. This means high fault-through operation, together with modularity. The big disadvantage is the requirement of isolated DC sources that implies bulky and complex transformers.
The cascaded configuration allows to use different voltages for the capacitors (in analogy with the FC topology), reducing the total number of redundant states but increasing the voltage levels with the same number of devices. (see figure 2.16). The characteristics may be summarized:

Advantages

- Modular structure;

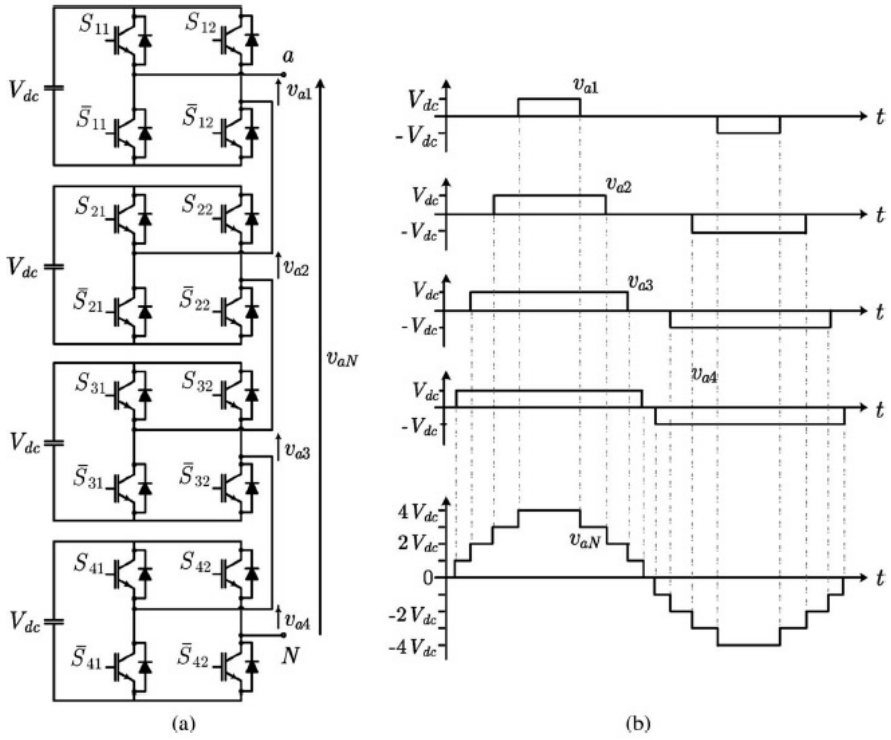


Figure 2.14: 9 levels H-bridge [8].

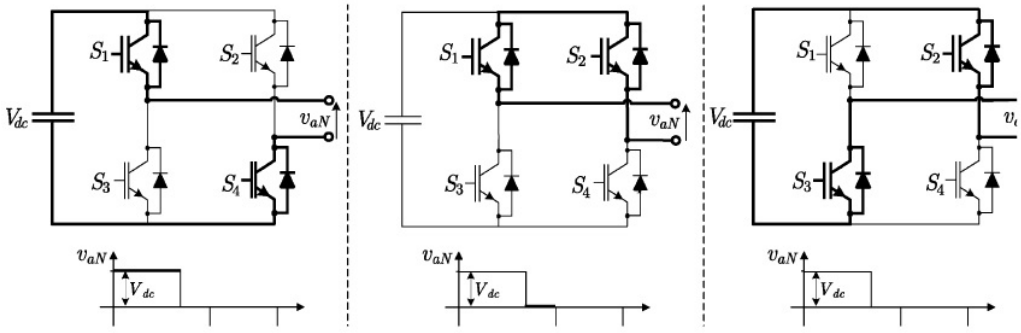


Figure 2.15: H-bridge switching pattern [8].

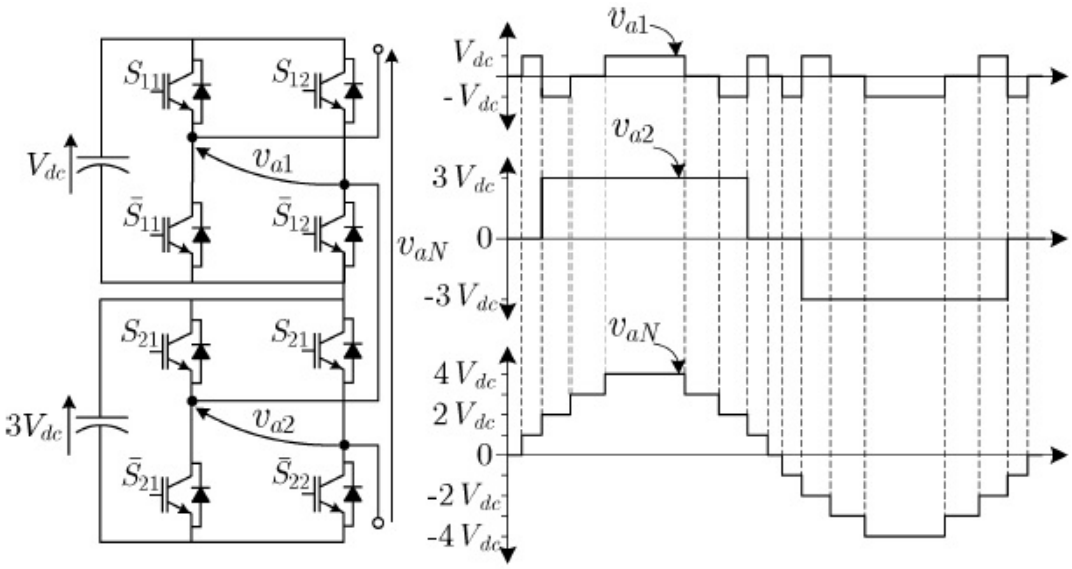


Figure 2.16: 9 level H-bridge with 4 cells [8].

- fault-tolerant operation capability (e.g. using bypass switches);
- high voltages reached with low switching rating;
- higher power than NPC is reached;
- configuration suitable for asymmetric operation.

Disadvantages

- Large DC capacitors are required to suppress the voltage ripple;
- many insulated sources are required (bulky and expensive transformers).

2.2.4 Modulation strategies for multilevel converters

The PWM (pulse width modulation) and the SVM (space vector modulation) are the most common techniques used in the DC-AC converters field. Starting from the basic principle of PWM and SVM many other modulation strategies have been developed to achieve different goals as for example THD reduction, converter losses reduction, circulating current reduction (with parallel converters). A simple and complete explanation of the most diffused PWM techniques and the mathematical model of switching losses and current ripple is reported in [9].
In the multilevel converters field the same basic principles have been used and adapted

to the different structure. The most diffused multilevel modulation techniques according to [8] are:

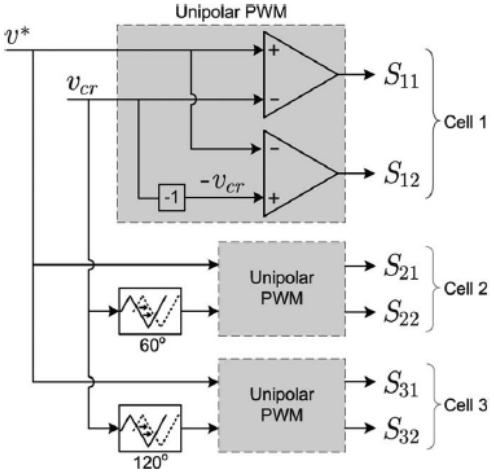
- PS-PWM: phase shifted pulse width modulation;
- LS-PWM: level shifted pulse width modulation;
- SVM: space vector modulation for multilevel converters.

According to [8], the PS-PWM is a natural extension of the PWM strategy suitable for converters with a modular structure, like the FC and cascaded H-Bridge. As shown in figure 2.17a and 2.18b the PS-PWM is dual to the interleaving applied with paralleled converters, using the analogy reported in [6]. The phase shift between the carriers cause the phase shift between each H-bridge or FC cell output and therefore the overall voltage has many levels as figure 2.18a shows. This modulation scheme is especially suitable for FC and CHB topologies because it allows an equal power sharing between each cell and therefore there is no needing to keep the capacitors balanced in the FC structure.
The LS-PWM is the generalization of the bipolar PWM that use the comparison between many carrier signals and the reference voltage to choose the output voltage level. With m levels, $m-1$ carrier signals are needed. Each carrier signal is associated to two voltage levels and the group of all the carriers spans the entire voltage amplitude range. In figure 2.17b the circuit is implemented for a three level converter. As shown in figure 2.18b the carriers may be chosen to have different phase disposition that will be related to the output waveform and THD.
This modulation strategy is especially useful with NPC converters since each carrier can be associated to two power switches [8].
Another strategy is worth to be presented is the space vector modulation (SVM). The switching times are computed using the vectorial representation of the reference voltage and of the inverter states, as shown in figure 2.19. Considering the three-phase system, the $\alpha - \beta$ transform is applied obtaining a vector in the complex plane. The equation obtained is:

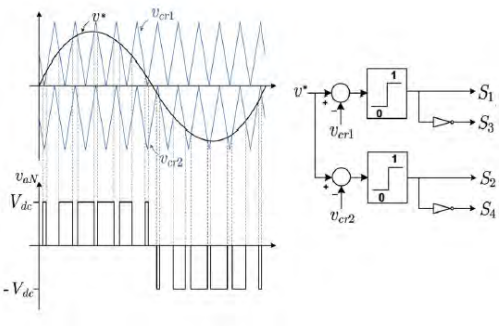
$$v_s = \frac{2}{3} \cdot [v_a + \alpha v_b + \alpha^2 v_c] \tag{2.13}$$

where $\alpha = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$. Substituting all the converter output voltage combinations the regular hexagons shown in figure 2.19 are obtained. According to this figure 19 of the 27 combinations produce a new state while the remaining 8 states are a redundant combinations. These redundancies are important because nothing changes from the load point of view in terms of applied voltage but the switches states are different and therefore this property is used to keep the capacitors balanced.
The equation 2.13 may also be applied to the reference voltage that is a rotating vector with angular speed ω. The output voltage level is generated from the comparison between the reference voltage and the triangular meshed hexagon. When the triangle where the reference voltage lays is identified the three voltage phasors associated to the three triangle corners are applied with a certain dwelling time. The voltage results:

$$v_{out} = \frac{1}{\tau}(t_1 \cdot v_1 + t_2 \cdot v_2 + t_3 \cdot v_3) \tag{2.14}$$

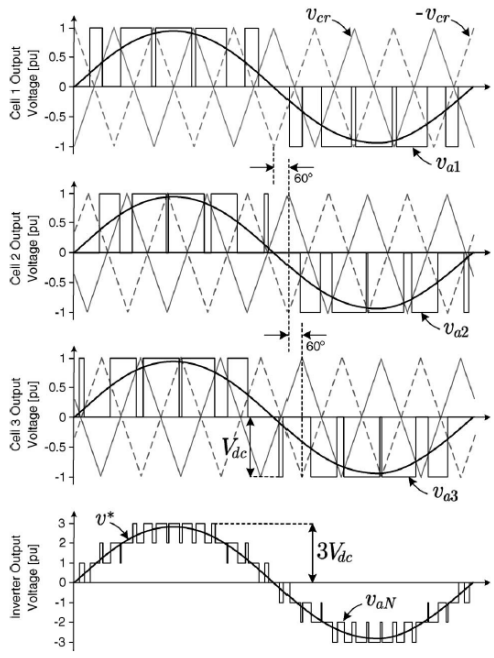


(a) PS-PWM circuital implementation [8].

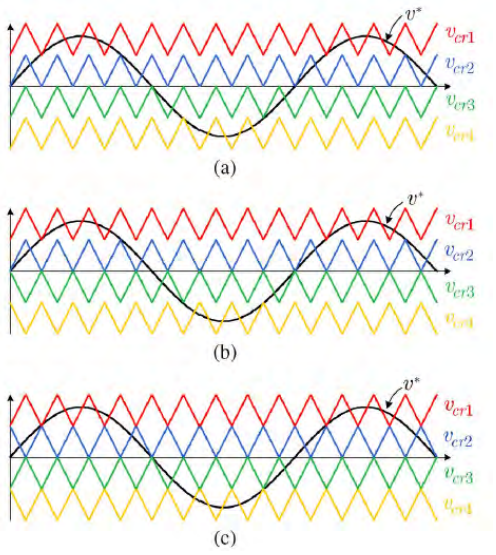


(b) LS-PWM circuital implementation [8].

Figure 2.17: Multilevel modulation schemes.



(a) PS-PWM seven level waveform CHB [8].



(b) LS-PWM different carrier position: a)phase disposition, b) phase opposition disposition, c) alternate phase opposition disposition [8].

Figure 2.18: Multilevel converters PWM modulation waveforms.

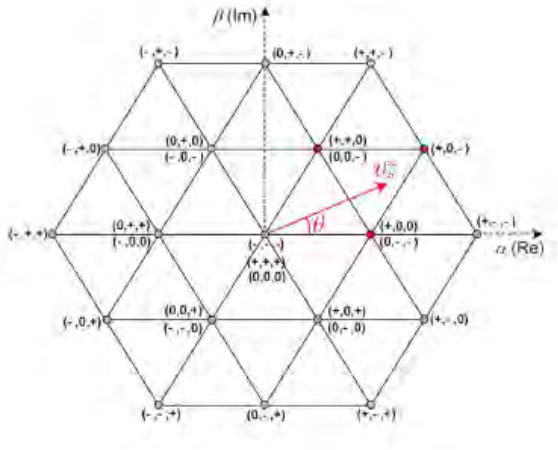


Figure 2.19: SVM with 3-levels converter [8].

where $\tau = t_1 + t_2 + t_3$ is a fixed modulation period and v_1, v_2, v_3 are the triangle corner vectors. The dwelling time for each vector is variable during the converter operation. Many SVM techniques have been designed in order to reduce the switching losses or to achieve the capacitor balancing; they differ in the calculation of the dwelling time of each vector. A clear example is reported in [10].
When the system is three-phase plus neutral, 3D-SVM techniques are used and therefore the $\alpha - \beta - \gamma$ transformation is used and the geometry of figure 2.19 becomes 3-D.

2.3 Hybrid and other series configurations

Starting from the classical topologies other improved configurations grew trying to put together the advantages. The most famous are: 3 levels active NPC (3L-ANPC), modular multilevel converter (MMC), asymmetrical CHB and FC. Some of these topologies are effectively hybrid topologies that combine different basic structures while others only use different semiconductors.

2.3.1 ANPC structure

In [1] it is shown that the ANPC structure is equivalent to the conventional NPC but uses an active neutral point clamping. The diodes are replaced with power switches as shown in figure 2.20 *a* and the current path is forced. In this way the power losses sharing can be optimized saving costs on the cooling systems, while in the classical NPC structure the freewheeling current trough the upper or lower clamping diodes depends on the current polarity. The result is an increased power limit for the converter.
The 5L-ANPC is obtained as an hybrid starting from the ANPC and FC schemes. Ob-

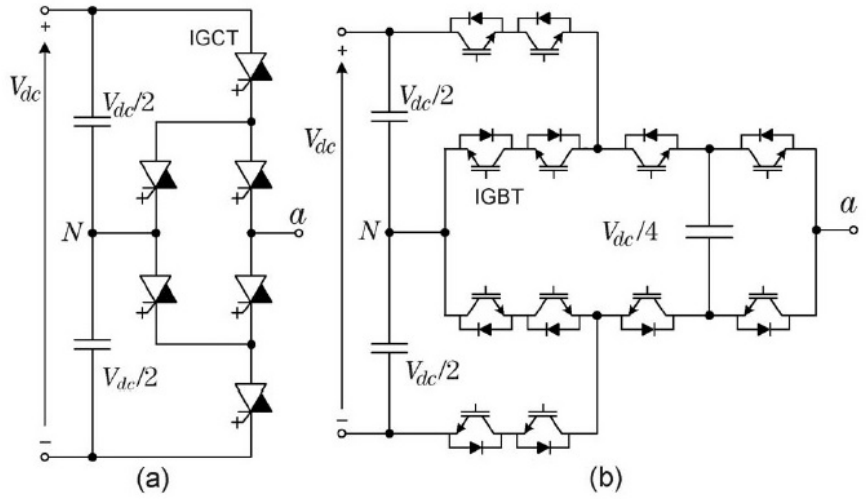


Figure 2.20: Active NPC schemes: a)3L-ANPC; b) 5L-ANPC (hybrid with 3L-ANPC + 3L-FC [1].

viously the control of this converter is more complex since the capacitor voltage must be constant. The FC stadium only adds new levels to the converter without increasing the power rating. Available configurations cover the range $0.4 - 1MVA$ according to [1].

2.3.2 MMC structure

According to [1], the MMC topology has found industrial applications recently, in the HVDC systems. The MMC is composed of single-phase two levels units, known as half bridges and connected in series. Each phase leg is divided in two parts with an even number of cells to generate an equal number of positive and negative levels. Inductors are used to prevent transitory short circuits. The switches are controlled in a complementary mode producing two active states: the capacitor of each cell can be inserted or bypassed generating the multilevel waveform. Like the FC structure, the voltage of each capacitor must be controlled and kept constant.
The interesting feature of this solution is the scalability and modularity, together with a fault-trough operation if an additional switch for each cell is used. In addition there is no needing of high voltage capacitors because this task is performed by the low voltage cells capacitor. This topology is suitable for HVDC systems: a back to back project has been proposed with $Vdc = \pm 320kV$ and nominal power $Pn = 1GW$ [13].

2.3.3 Asymmetrical CHB and FC

The asymmetrical CHB or FC uses the same scheme of the classical topologies but each cell is fed with different DC voltages ([11], [1]). In this way some or even all the redundant states can be eliminated, maximizing the number of different voltage levels

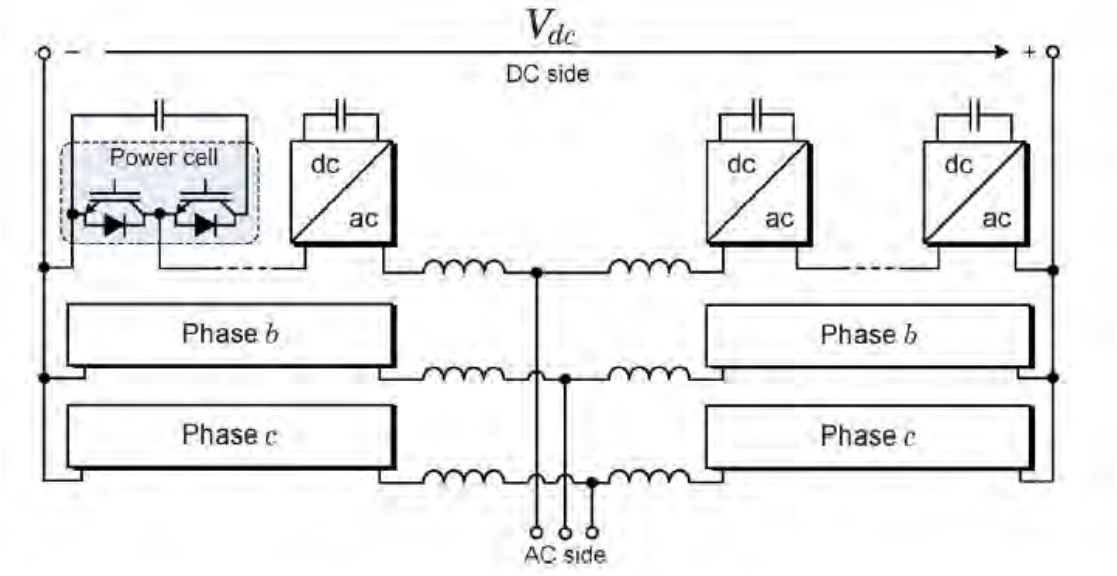


Figure 2.21: MMC converter [1].

generated. As reported in [1], many voltage asymmetry ratios has been introduced such as $(1 : 2 : \cdots 2^{n-1})$ and $(1 : 3 : \cdots 3^{n-1})$, while further ratios are introduced in [11] when the converter is used to fed a motor without open-end winding configuration: in this case the number of voltage levels in each motor winding is maximized instead of in each converter phase, obtaining a *new optimal* strategy and an *extreme* strategy under certain conditions. Aside from the strategy used, according to [1] and [11] this proposed methods allows to use different switching frequency for each cell. The one with higher power rating will use the fundamental frequency limiting the switching losses, while the others will be controlled with higher frequencies.
The biggest drawback is the uneven power sharing between the cells that means unequal cooling requirements, families of different used semiconductors, higher current harmonics due to the suppression of the input transformer.

Chapter 3

Selected topology

3.1 Introduction

The configuration studied in this thesis is a serial connection between two three phase converters and three single-phase H-bridges. This system has been proposed in [14]. The studied topology is derived from the classical cascaded H-bridges shown in figure 3.1, based on six NPC cells fed by separated DC sources. The solution presented in figure 3.1 like many others based on cascaded converters has the big advantage to utilize conventional semiconductors to reach high power levels; great flexibility and fault tolerance are also guaranteed. However the insulation between every DC cell must be ensured in order to avoid short circuits between the capacitors; this condition may be respected using different sources or for example multi-windings generators. Moreover since every cell is a single-phase cell if a constant power is delivered to the grid the power oscillation in the DC side is twice the fundamental frequency ($120Hz$ if the fundamental frequency is $60Hz$). The capacitors are chosen to fulfil the requirements on the voltage ripple; in the hypothesis of small ripple V_c and considering the steady state the operation, the ripple equation can be written [14],[15]:

$$I_c = C \cdot \frac{dV_c}{dt} = \frac{V_m \cdot \sin(\omega t) \cdot I_m \cdot \sin(\omega t + \phi)}{E} = \frac{1}{2} \cdot \frac{V_m \cdot I_m \cdot \sin(2\omega t)}{E} \tag{3.1}$$

$$V_c = \frac{\int I_c \, dt}{C} = V_{DC} + \frac{V_m \cdot I_m}{4 \cdot E \cdot \omega \cdot C} \cdot \cos(2\omega t) \tag{3.2}$$

where V_m and I_m are the AC side maximum voltage and current, ω is the angular speed of the output voltage and C is the capacitor size. The equation 3.1 is valid in the hypothesis of small DC ripple, sinusoidal voltage V_m and considering that the filter always used to connect an inverter with a grid is mostly inductive. For a fixed set of parameters in 3.1, the voltage ripple obtained in the DC capacitor is inversely proportional to the capacitance that must be high in order to compensate the $2 \cdot fundamental$ frequency effect.

In figure 3.2 the studied configuration is presented: two three phase converters share the same DC bus and they are connected in series with three single-phase H-bridges cells

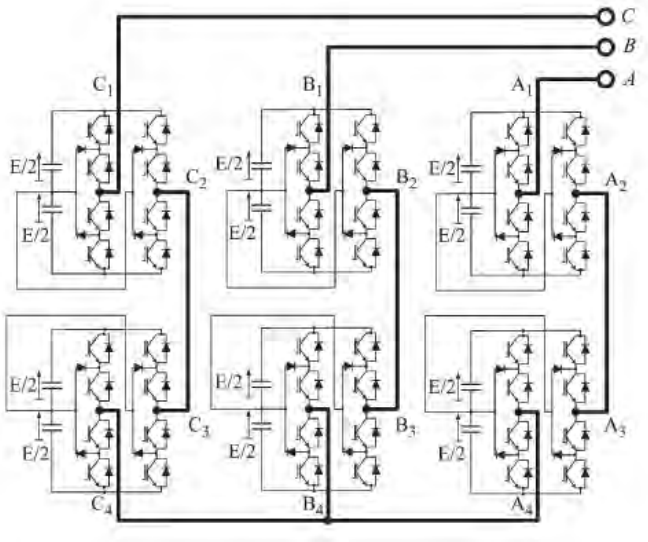


Figure 3.1: Cascaded H-bridge VSC with 3L-NPC [14].

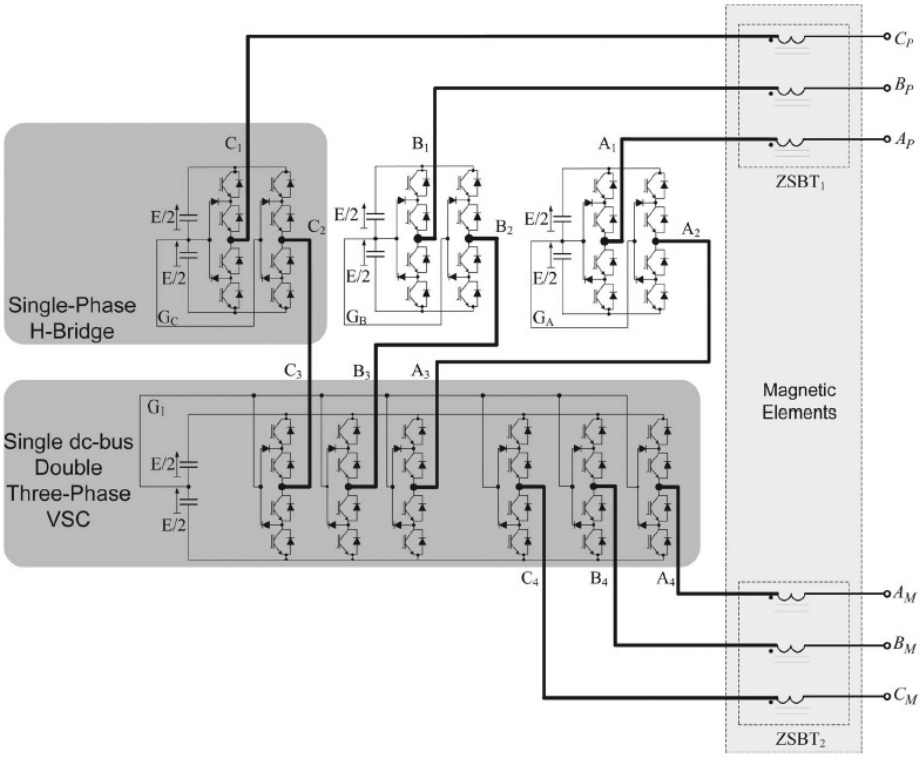


Figure 3.2: Studied topology proposed in [14].

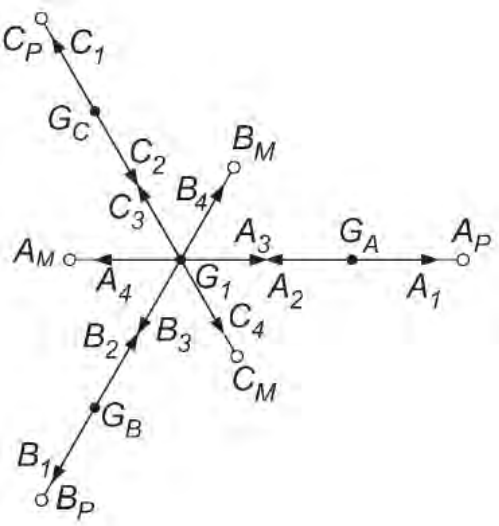


Figure 3.3: Vector diagram proposed in [14].

instead of using six cells. According to [14] this connection is allowed because of the open-end winding configuration; without this solution a close path for the current would be created if a special modulation strategy is not developed and the capacitors would be short-circuited. This means that the open-end winding allows to use only 4 separated bus instead of 6.
The used converters are NPCs, the most diffused multilevel topology already described in chapter 2.
It is known that in a three-phase converter where the phases that share the same DC bus, the summation of the instantaneous powers is constant in the case of balanced load. This means that the power oscillation at twice the fundamental frequency is not generated and the ripple associated to the three-phase bus is only due to the switches commutation [14]. Thus the size of the capacitors for the three-phase converters can be reduced, obtaining a cheaper solution.
According to [14], since the open-end winding configuration is adopted, the load imposes the zero sequence impedance: if this impedance is low, the zero sequence blocking transformers (ZSBT) must be used to avoid over-currents. For example if a three-phase three limbs transformer is adopted the zero sequence impedance obtained will be low and the ZSBTs are necessary. If this topology is grid connected through three single-phase transformers, the zero sequence is automatically blocked.
In figure 3.3 the voltage vectors combination adopted in [14] is shown: considering the phase a, V_{A1GA} and V_{A2GA} imposed by the mono-phase converter are in phase opposition as V_{A3G1} and V_{A4G1}.This means that the total voltage phasor applied to the load is 4 times the single phasor in the hypothesis of equal voltage phasors impressed by the converters.

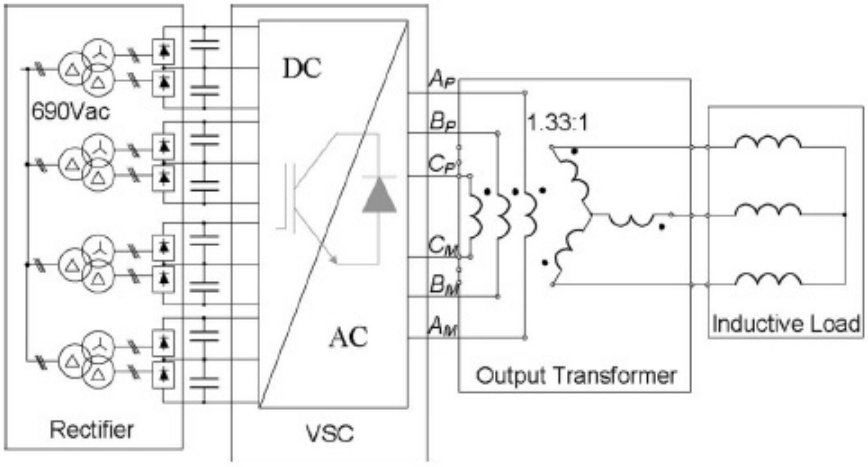


Figure 3.4: Electrical diagram of the experiment executed in [14].

3.2 Properties of this configuration

As mentioned in the previous chapter, in [14] the main advantages like high reliability, fault-tolerant operation and reduction of the number of isolated sources together with the three-phase capacitors size reduction are discussed. In this section an overview about other interesting aspects of this topology is presented.

3.2.1 Voltage level

Since the multi-levels converters were born to increase the power ratings and the output voltage of the conventional converters, this topology easily fit with *medium voltage applications*. However recently a low voltage application of three-level converters appeared on the market of wind power plants [16]. The advantages are the reduction of filter size, a better harmonic spectrum and the usage of low voltage components that in applications like off-shore wind power plant are desirable.
As shown in [16], this topology may be applied in low voltage range: in this thesis the reference value for low voltage will be considered $V_{rms} = 1000[V]$ with frequency $f = 60\ [Hz]$. The same configuration shown in figure 3.4 is adopted to connect the whole converter to the grid because of the open-end winding configuration; if the load is a single electrical machine, the transformer is not necessary. This interconnection transformer allows to adjust the voltages between the converter side and the grid side. This means that there are no restrictions on the choose of the semiconductors; the optimal solution matches the good compromise between the power losses (related to the square value of the current) and the insulation requirements (related to phase-phase and phase-ground voltages). Let us consider the parameters in table 3.1: the selected semiconductor is an

Data	Parameter	Symbol	Value	Unit
Grid	$V_{line-line}$	V_{rms}	1	$[kVrms]$
	Frequency	f	60	$[Hz]$
IGBT FZ3600R17KE3	*DC collector current*	$Ic\ nom$	3.6	$[kA]$
	Collector emitter voltage	V_{CES}	1.7	$[kVpeak]$
	Delays time	td	3.15	$[\mu sec]$
GCT FGC6000AX120DS	*RMS on state current*	$Ic\ nom$	3.1	$[kA\ rms]$
	Collector emitter voltage	V_{CES}	6	$[kVpeak]$
	Delays time	td	6	$[\mu sec]$
GTO 5SGA 40L4501	*RMS on state current*	$Ic\ nom$	1.57	$[kA\ rms]$
	Collector emitter voltage	V_{CES}	4.5	$[kVpeak]$
	Delays time	td	35.5	$[\mu sec]$
SCR FT1500AU-240	*RMS on state current*	$Ic\ nom$	2.36	$[kA\ rms]$
	Collector emitter voltage	V_{CES}	12	$[kVpeak]$
	Delays time	td	1214	$[\mu sec]$

Table 3.1: Typical devices for high power application [2].

$IGBT$ thus the switching frequency can reach high values but the devices performances in terms of maximum voltage and current are reduced in comparison with other technologies. Considering a fault case in the worst working condition, only one converter will produce power while the others will be switched off. For example it can be considered that only one three-phase converter or three half single-phase units are working which is the minimum to guarantee balanced voltages. Considering the voltage drop on the filter negligible, the voltage produced by a single converter must be sufficient to reach the grid voltage value to guarantee a fault-tolerant operation. The voltage equation is:

$$V_{conv} = \frac{1}{\sqrt{2}} \cdot \frac{V_{dc}}{2} = \frac{2 \cdot 1700}{2 \cdot \sqrt{2}} = 1202\ [V\ rms] \tag{3.3}$$

where V_{conv} is the reached voltage referred to the neutral point, Vdc is the total DC voltage set to $Vdc = 2 \cdot Vmax$ because in the NPC topology the switches have only to block half of the DC bus voltage. Using a delta connection on the grid side the transformer ratio becomes:

$$k_{transformer} = \frac{V_{grid}}{V_{conv}} = \frac{1000}{1202} = 0.832. \tag{3.4}$$

The maximum rms current delivered in the grid and the power are therefore computed considering the switches current limit $Imax = 3600\ [A\ peak]$:

$$I_{grid} = \frac{I_{max}}{\sqrt{2} \cdot k_{transformer}} = \frac{3600}{\sqrt{2} \cdot 0.832} = 3060\ [A\ rms] \tag{3.5}$$

$$P = \sqrt{3} \cdot V_{grid} \cdot I_{grid} = \sqrt{3} \cdot 1000 \cdot 3060 = 5.3\ [MW] \tag{3.6}$$

This solution with IGBTs presents the maximum fault-through operation and high switching frequency (compared with GTO and GCT) but the total power is low and the switches have a low utilization factor.
Because of the series connection the current in all the converters is the same, while the voltage produced by each converter will be proportional to the power available in the DC side. This means that in this topology the voltage reachable in each converter is fixed (once the considerations on the fault operation are made) while the current will be limited by the switches. It is obvious that in a normal operation in the full power condition the current will be near to the devices limit, while the voltage will be lower than the maximum: this means that the semiconductors have normally a low utilization factor, defined as the ratio between the power delivered and the power limit of the switch. Considering to operate in a fault condition with minimum a couple of operative converters (2 three-phase or 3 double single-phase), using the same devices of the previous case the total power can be doubled reducing the fault-tolerant capability.

$$V_{conv} = 2 \cdot \frac{1}{\sqrt{2}} \cdot \frac{V_{dc}}{2} = 2 \cdot \frac{2 \cdot 1700}{2 \cdot \sqrt{2}} = 2404 \ [V \ rms] \tag{3.7}$$

$$k_{transformer} = \frac{V_{grid}}{V_{conv}} = \frac{1000}{2404} = 0.416 \tag{3.8}$$

$$I_{grid} = \frac{I_{max}}{\sqrt{2} \cdot k_{transformer}} = \frac{1700}{\sqrt{2} \cdot 0.416} = 6119 \ [A \ rms] \tag{3.9}$$

$$P = \sqrt{3} \cdot V_{grid} \cdot I_{grid} = \sqrt{3} \cdot 1000 \cdot 2890 = 10.598 \ [MW] \tag{3.10}$$

If instead of IGBTs GCTs are used, the results are the following:

$$V_{conv} = \frac{1}{\sqrt{2}} \cdot \frac{V_{dc}}{2} = \cdot \frac{2 \cdot 6000}{2 \cdot \sqrt{2}} = 4243 \ [V \ rms] \tag{3.11}$$

$$k_{transformer} = \frac{V_{grid}}{V_{conv}} = \frac{1000}{4243} = 0.2357 \tag{3.12}$$

$$I_{grid} = \frac{I_{max}}{k_{transformer}} = \frac{6000}{0.2357} = 13.15 \ [kA \ rms] \tag{3.13}$$

$$P = \sqrt{3} \cdot V_{grid} \cdot I_{grid} = \sqrt{3} \cdot 1000 \cdot 18000 = 22.78 \ [MW]. \tag{3.14}$$

The power is increased but a lower switching frequency must be adopted because GCTs are slower than IGBTs.
If the power rating must be extended using IGBTs and keeping the maximum fault-tolerant operation other solutions can be adopted. For example the transformer may be designed as an *on-load tap changer* (OLTC) as figure 3.5 shows: only few levels are sufficient to guarantee the operation below the voltage limits in whatever fault condition.

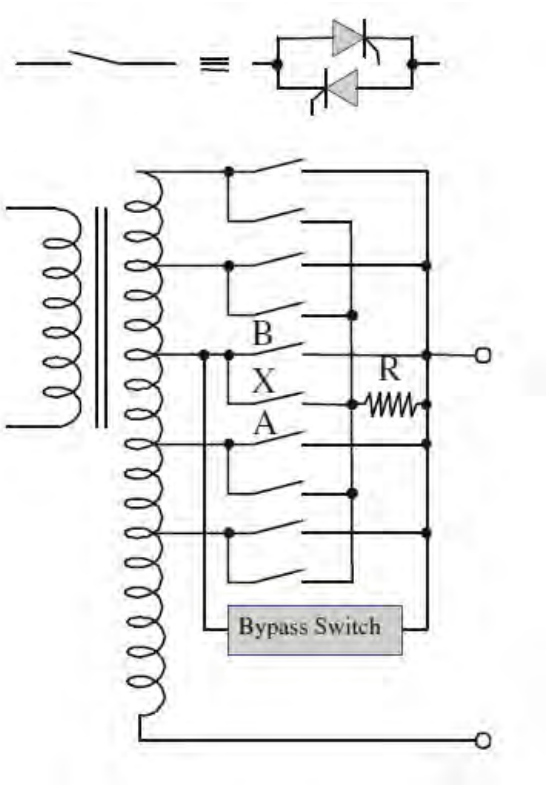


Figure 3.5: Full electronic OLTC [17].

The price that must be paid is the increased complexity of the system that require to control automatically the changer. In addition the internal impedance of the transformer varies with different tap positions and this observation must be taken into account when the interconnection filter is designed. Anyway this solution is feasible and may be used to increase the total power delivered and the switches utilization.

3.2.2 Power plant

In [14] the sources were considered equal and were modelled with constant voltage sources with equal values. In this thesis this hypothesis is removed, considering the case of different power sources that can deliver different amount of power at each instant. Therefore this topology can be considered as an hybrid topology, connecting for example photovoltaic cells to the single-phase converters and wind power plants to the three-phase converters.
Considering to have different sources is also a limitation: in this topology the power delivered is proportional to the voltage applied by each converter and in the single-phase converters this voltage must be the same to avoid voltage unbalances in the triple of phasors. Thus in the case of failure of one single-phase converter or if null power produced

the others must adapt to this value, even if they're able to produce. This drawback can be deleted in two ways:

- Using conform generation plants in the same region;
- Using three phase insulated windings stators.

In the former solution the power is produced by homologous separated sources located in the same region so that the sources will deliver approximatively the same amount of power: considering for example the photovoltaic case, the solar irradiation will be the same in the near areas. If this hypothesis is removed, the plants must be able to regulate the power delivered such as with a pitch control in order to obtain always the same amount of power in the single-phase converters.
The latter solution is obvious: a unique three-phase plant is split in three separated single-phase sources and the power delivered will be different only in case of failure. Using a more sophisticated control if the voltage triple of the grid is unbalanced the system could apply an unbalance triple of phasors in order to reduce the negative sequence current.

3.2.3 Interleaving

Since four converters are serialized, with a proper use of the modulation strategy the first harmonics band in the voltage output waveform can be shifted by a factor of 4 obtaining an apparent switching frequency $f = 4 \cdot f_{switching}$ according to the interleaving theory. The modulation strategy chosen is the level shifted carrier pulse width modulation ($LSCPW$) with the carriers shifted by 90°. Because of the opposite connection of the two single-phase converters and the two three-phase converters the carriers of the three-phase converters must be in phase with each other and shifted relatively to the carries of the single-phase converters, again in phase with each other.The result is shown in figure 3.6.

This is valid considering that all the sources have the same DC voltage. Because of the serial connection the current is the same, and the condition on the power become $Psingle_{tot} = Pthree_{tot}$, and this means that the power produced by a single single-phase DC source must be $\frac{1}{3} \cdot Pttot$. If this link is removed the harmonic cancellation won't be perfect because the voltage phasors applied by three-phases and single-phases converters will be different. This means that generally the switching frequency band appears in the voltage waveform centred at $2 * fswitching$; changing the power ratios the reduction of the harmonic band at $2 * fswitching$ will be variable and a theoretical a perfect elimination will be possible with the power ratios nearly equal to 1.

3.2.4 Unbalanced grid

According to [18], power converters are affected by power oscillations and over-currents when the AC source becomes unbalanced and many methods that control the positive and negative sequence have been proposed. In case of distorted AC source due to faults or disturbances, the unbalanced AC voltages have been proven to be one of the greatest challenges for the converters control in order to keep them normally operating and connected to the source.

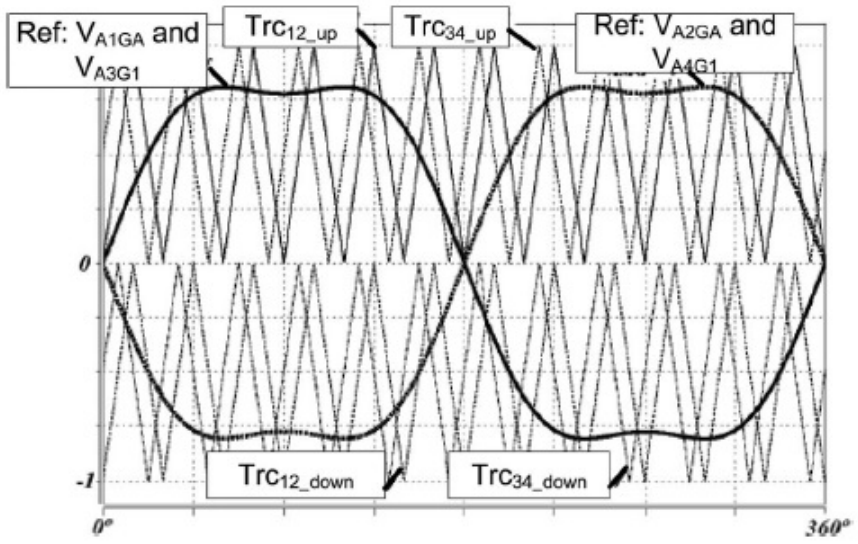


Figure 3.6: Modulation strategy used in [14].

Since in the selected topology a closed path for the zero current is produced, this current can be controlled in order to obtain specific objectives when an unbalanced fault appears on the grid side. Figure 3.7 shows the control adopted in [18] where positive, negative and zero sequence currents are produced. The current reference equations for the three sequences have been computed in [18] in order to:

- Eliminate the negative sequence current;
- Eliminate the active and reactive power oscillation;
- Eliminate the active power oscillation and negative sequence current.

The use of a single converter in order to control $i_d^+, i_d^-, i_q^+, i_q^-, i_{re}^0, i_{im}^0$ needs an high switching frequency that limits the application of this solution to the low power converters field (in the experiment in [18] a frequency $f = 20\ [kHz]$ was used). For example in the studied topology depicted in figure 3.2), the control of the negative and zero sequence can be activated, when an unbalance fault is detected, on the single-phase converters while the three-phase converters deliver active power. When the unbalance is removed, the control of the single-phase converters can be changed again to the positive sequence. Obviously according to [18] the power expression in case of fault becomes more complex:

$$\begin{bmatrix} p_{3\phi} \\ q_{3\phi} \end{bmatrix} = \begin{bmatrix} P + P0 \\ Q \end{bmatrix} + \begin{bmatrix} P_{c2} + P_{0c2} \\ Q_{c2} \end{bmatrix} \cdot \cos(2\omega t) + \begin{bmatrix} P_{s2} + P_{0s2} \\ Q_{s2} \end{bmatrix} \cdot \sin(2\omega t) \tag{3.15}$$

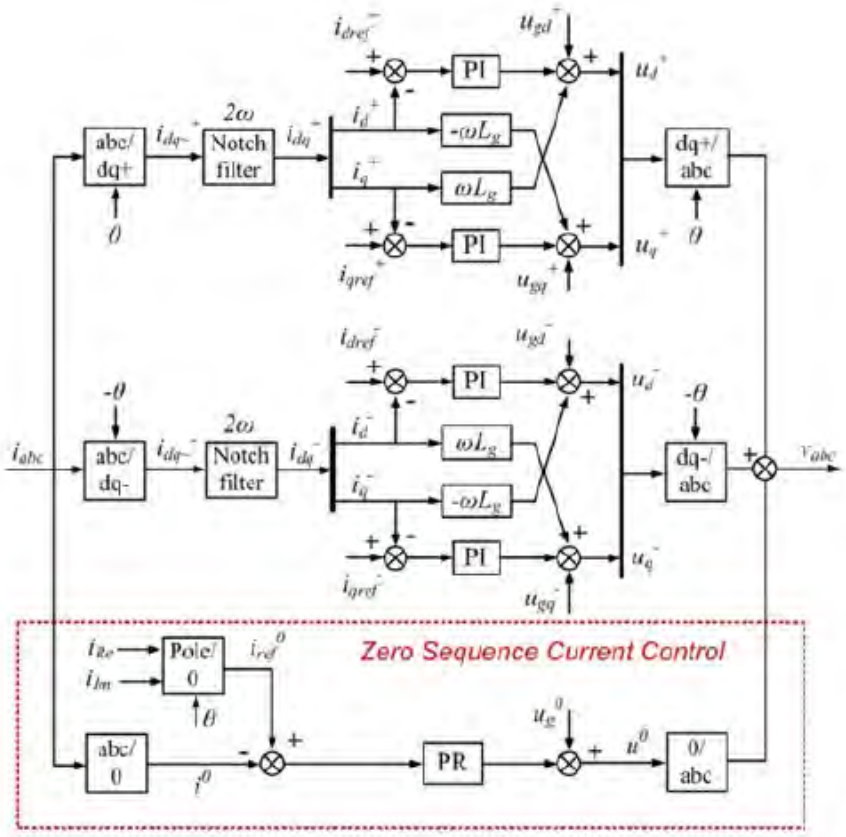


Figure 3.7: Control structure with zero sequence control used in [18].

where $p_{3\phi}, q_{3\phi}$ are the instantaneous active and reactive power and the other components are calculated as follows in a rotating dq reference system:

$$\begin{bmatrix} P+P0 \\ Q \\ P_{c2}+P_{0c2} \\ Q_{c2} \\ Q_{s2} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_d^+ & v_q^+ & v_d^- & v_q^- & v_{re}^0 & v_{im}^0 \\ v_d^- & v_q^- & v_d^+ & v_q^- & v_{re}^0 & -v_{im}^0 \\ v_q^- & -v_d^- & -v_q^+ & v_d^+ & -v_{im}^0 & -v_{re}^0 \\ v_q^+ & -v_d^- & v_q^- & -v_d^- & 0 & 0 \\ v_q^- & -v_d^- & v_q^+ & -v_d^+ & 0 & 0 \\ -v_d^- & -v_q^- & v_d^+ & v_q^+ & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \\ i_{re}^0 \\ i_{im}^0 \end{bmatrix} \tag{3.16}$$

As shown in the equations 3.15 and 3.16 with an unbalanced condition the active and reactive power are oscillating and all the sequences contribute to active and reactive instantaneous power.

3.3 General control problem

3.3.1 System configuration

In this section the general control problem will be discussed. Even if the studied topology is built with many converters connected in series, an equivalent model can be derived using the Thevenin's principle: considering that the phasors applied by the three-phase converters and the single-phase converters are aligned, the result will be a generator with 4 times the voltage applied by a single converter. In figure 3.8 the classical connection scheme using a simple inductive filter is shown: typically the L filter is placed on the inverter side with the lower voltage and higher current because the transformer is usually a step up transformer. This choice is reasonable because if the inductance is placed on the grid side considering k to be the transformer amp-turn ratio ($k > 1$), the value required will be $L_{grid} = k^2 \cdot L_{inv}$ while the nominal current is proportional to $\frac{1}{k}$. Considering an inductor without magnetic core, the inductance is:

$$L = \frac{N^2}{\Re} = \frac{N^2 \cdot \pi \cdot Dm^2 \cdot \mu_0}{4 \cdot h} \tag{3.17}$$

where N is the number of turns, $\Re$ is the reluctance, Dm is the medium coil diameter and h is the the coil length. Decreasing the current a proportional decrease is obtained for the wire section, thus it is generally preferred to connect the inductance in the high current side in order to keep the diameter and the number of turns low, even if the losses are higher ($P_{loss} = R \cdot I^2$). Also another factor must be considered: the transformer obviously uses a magnetic core, where the losses are given by Steinmetz formula (even if the modified Steinmetz equation should be used in non-sinusoidal problems):

$$P_{losses} = C_1 \cdot f^{\alpha} \cdot B^{\beta} + C_2 \cdot f^2 \cdot B^2 \tag{3.18}$$

where C_1, C_2 are material coefficients, B is the magnetic induction and f is the fundamental frequency. If the filter is used in the grid side all the voltage harmonics are applied directly to the transformer, giving an higher value for the iron losses.

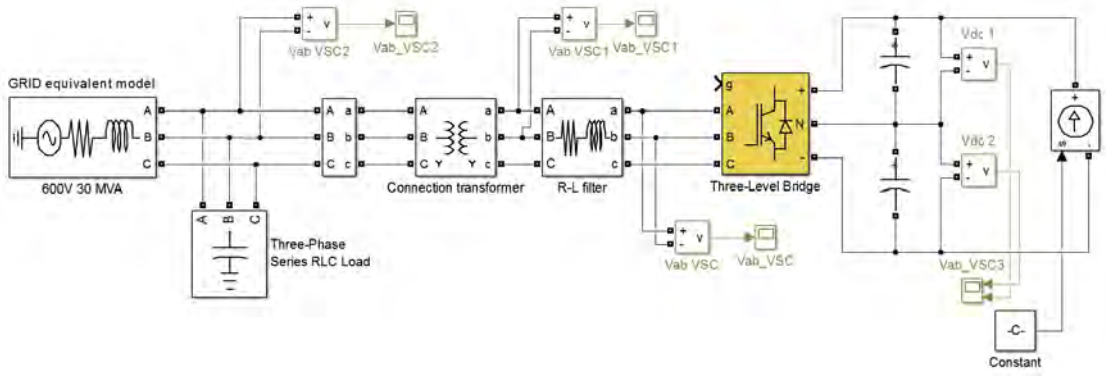


Figure 3.8: Typical connection scheme with an inductive filter.

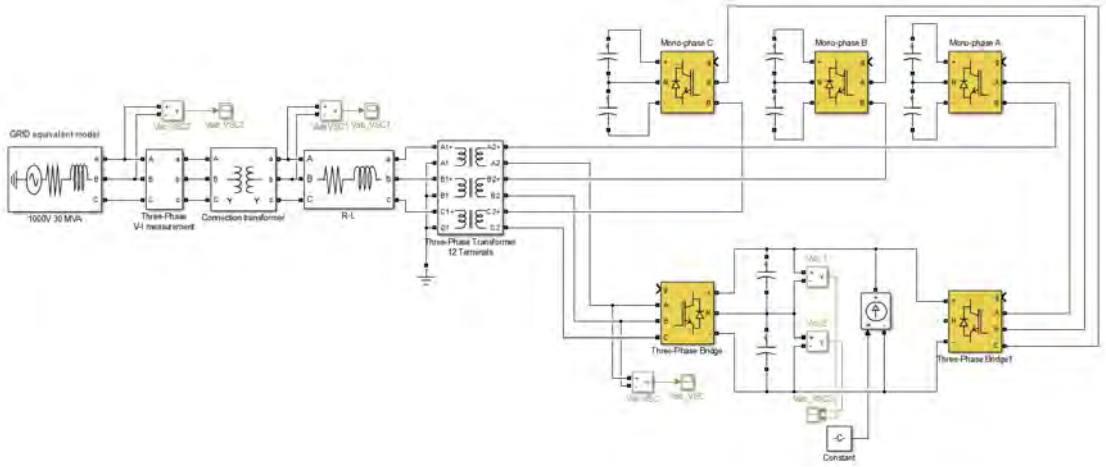


Figure 3.9: Simplified representation of the studied configuration.

The configuration studied in this thesis is represented in 3.9 with a model built is Simulink ®. The open end winding transformer is represented as a three-phase transformer with twelve terminals (in figure 3.9 with Y-Y connection) and the inductive filter is placed on the grid side. The filter may be also an LC filter or an LCL filter, but for now the simple case of a first order filter is considered. Other considerations relatively to the efficiency and the losses calculation will be made in the next chapters.

The electrical equivalent circuit is represented in 3.10 where also two ZSBTs are modelled. The windings in the grid side are connected in wye configuration that should be changed in delta if a zero sequence current is produced by the converters. The zero sequence current can circulate because of the neutral connection, due to the configuration with shared DC capacitor for the three-phase converters.

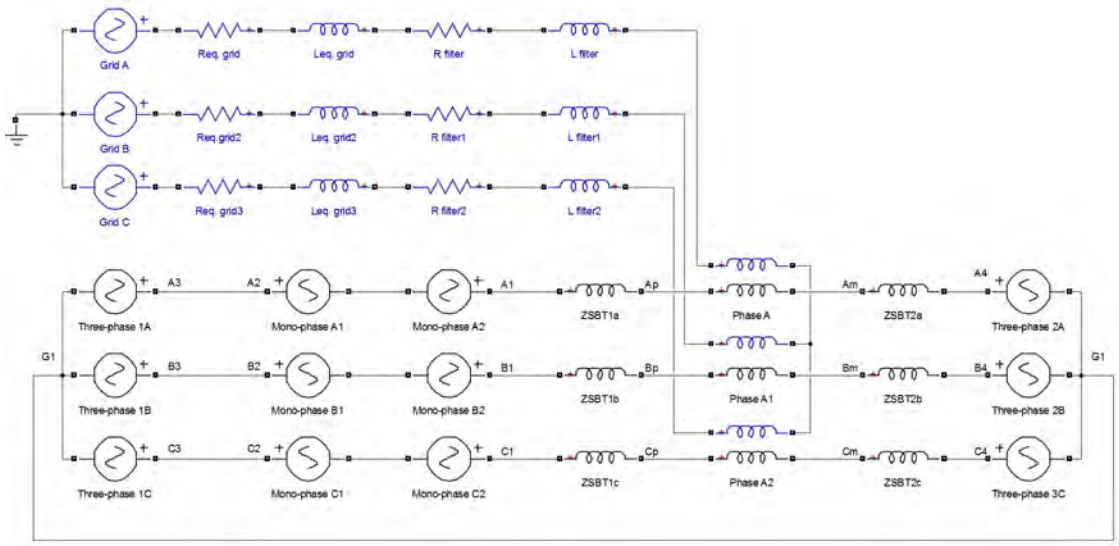


Figure 3.10: Electrical equivalent scheme of the topology with ZSBTs.

3.3.2 Theoric control

The system given by the connection of all the converters may be modelled with a voltage generator applying the Thevenin's theorem (also an internal impedance should be added) as shown in figure 3.11. The equivalent voltage phasor (phase-ground) can be expressed as:

$$V = \frac{m \cdot U_{DC} \cdot \sin(\omega t + \delta)}{2\sqrt{2}} \tag{3.19}$$

where V is calculated in RMS value, UDC is the DC voltage m is the adopted modulation index, ω is the the fundamental angular speed and δ is the angle between the inverter phasor and the grid phasor. In the hypothesis of negligible resistance, the well known expressions for the power can be found:

$$P = \frac{3 \cdot V \cdot V_{grid} \sin(\delta)}{X} \tag{3.20}$$

$$Q = \frac{3 \cdot V_{grid} \cdot (V_{grid} - V \cdot \cos(\delta))}{X}. \tag{3.21}$$

Controlling separately the modulation index m and the angle δ, the voltage drop on the filter inductance is fixed: in this way the active and the reactive powers delivered to the grid are controlled. Obviously some constraints in the regulation must be taken into account such as the switches maximum voltage and current together with other limitations related to: the maximum power capability of the transformer, the grid stability, the power-frequency drop function. The more constraints are added,the more complicated the system becomes.

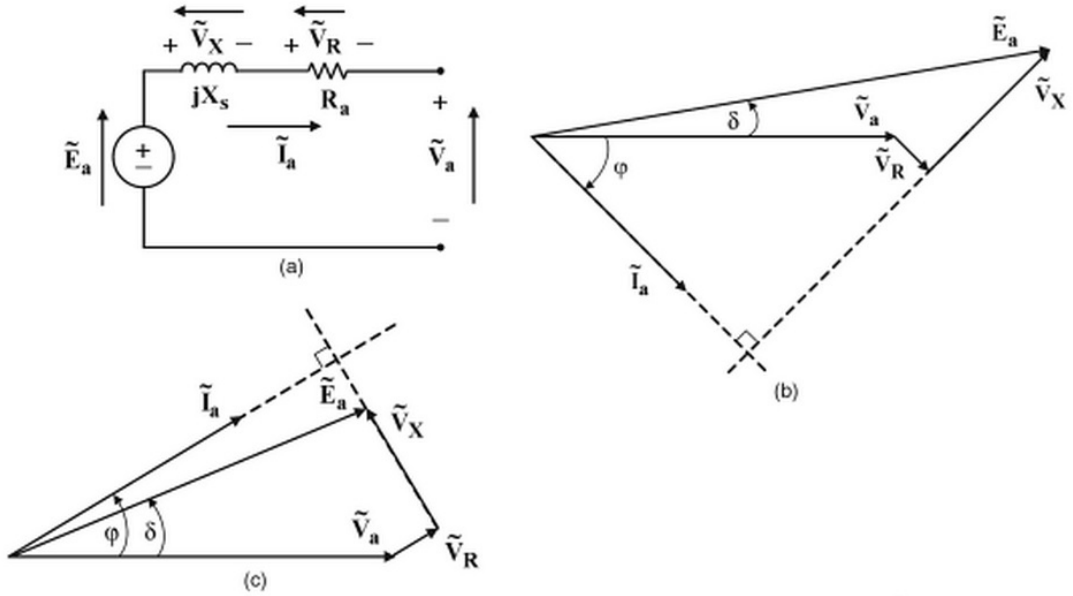


Figure 3.11: Phasors diagram for a RL impedance: a)circuit considered; b)inductive load c)capacitive load.

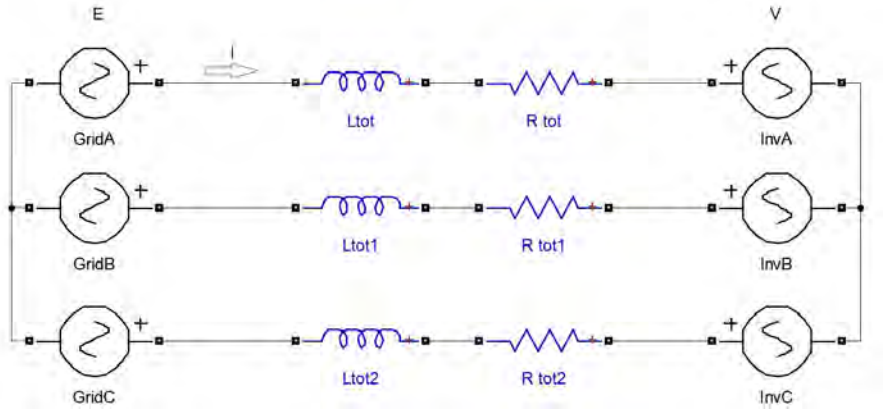


Figure 3.12: Equivalent grid-filter-converter model.

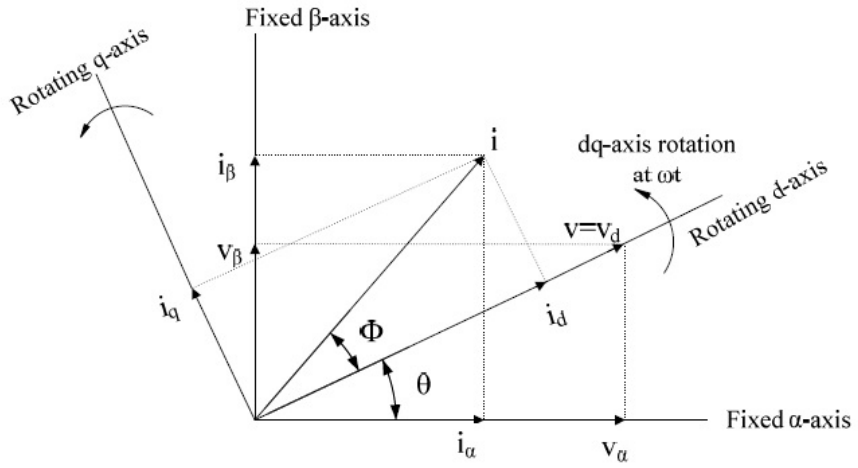


Figure 3.13: Stationary-rotating transformation [19].

To understand how to control the overall system, the first step is to analyze the equivalent circuit shown in figure 3.12, where the converters are substituted with voltage sources V. Also the grid is modelled with voltage sources with value E. The current convention is considered to be positive in the direction shown in figure 3.12. The equations of this system written in vectorial form in *abc* frame are:

$$\begin{bmatrix} Ea \\ Eb \\ Ec \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} + \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \tag{3.22}$$

The equation 3.22 uses a stationary coordinate system. In order to control the three-phase system with classical PIDs, the reference system must be changed into a rotating *dq* coordinate system as shown in figure 3.13. The equations become:

$$\begin{bmatrix} Ed \\ Eq \\ E\gamma \end{bmatrix} = \begin{bmatrix} R & -\omega \cdot L & 0 \\ \omega \cdot L & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} + \begin{bmatrix} Vd \\ Vq \\ V\gamma \end{bmatrix} \tag{3.23}$$

where ω is the angular speed of the rotating coordinate system equal to $\omega = 2\pi freqency$.

According to [19], the reference value for the active power can be produced controlling directly the active power that must be delivered to the grid or controlling the DC side voltage; the power that can be delivered is different from the power produced because of the losses. The same happens to the reactive power reference that can be produced to fulfil directly the reactive requirement or to control the AC side voltage amplitude in order to help the grid for voltage regulation purposes.
As shown in figure 3.11, the reactive power injection influences on the converter voltage

phasor, but the more reactive current flows through the switches the lower is the active power that can be delivered (for economical reasons, the best choice would be to inject all the active power).
In this thesis the first hypothesis considered is to have a *DC input voltage regulated by controllers outside of this topology*: for example in case of wind power production plants or when generally the production is in AC, the rectifier can be set to control the DC voltage. If a direct DC source is used, the DC voltage can be regulated using a DC-DC chopper. In this way active and reactive power exchanged with the grid are controlled directly.
Using a dq reference with an orthogonal transformation with the d axis aligned with grid voltage phasor, the power expressions become:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_d \cdot i_d + v_q \cdot i_q \\ j \cdot (v_q \cdot id - v_d \cdot i_q) \end{bmatrix} = \begin{bmatrix} v_d \cdot i_d \\ -j \cdot v_d \cdot i_q \end{bmatrix}. \tag{3.24}$$

The converters are connected in series: this means that i_d and i_q will have the same value while the voltage will depend on the power delivered. The power equation can be re-written as:

$$P = (v_{d1} + v_{d2} + v_{d3} + v_{d4}) \cdot i_d \tag{3.25}$$

$$Q = -(v_{d1} + v_{d2} + v_{d3} + v_{d4}) \cdot i_q. \tag{3.26}$$

Four voltage terms are used because four converters are serialized (two single-phase and two three-phase). Normally i_d and i_q references are produced starting from this equation since the sum of all the voltages is equal to the grid voltage.
The first idea could be to design separated controls for the single-phase system and the three-phase system, knowing for example the amount of power that each DC source is able to deliver. The problem is that the current components i_d and i_q are the result of the interaction between the total applied voltage phasor and the grid voltage phasor and equations 3.25 and 3.26 can't be used to find a reference voltage that should be applied to each converter. To avoid this problem, an expression for the current as a voltage function must be found. Assuming to be in steady state operation, the time derivative in 3.23 can be neglected and the equation becomes:

$$\begin{bmatrix} Ed - Vd \\ Eq - Vq \\ E\gamma - V\gamma \end{bmatrix} = \begin{bmatrix} R & -\omega \cdot L & 0 \\ \omega \cdot L & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} \tag{3.27}$$

Starting from the previous expression the following equation can be written:

$$\begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} = \begin{bmatrix} R & -\omega \cdot L & 0 \\ \omega \cdot L & R & 0 \\ 0 & 0 & R \end{bmatrix}^{-1} \begin{bmatrix} Ed - Vd \\ Eq - Vq \\ E\gamma - V\gamma \end{bmatrix} \tag{3.28}$$

Computing the inverse matrix the expression becomes:

$$\begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} = \frac{1}{R^2 + \omega^2 L^2} \cdot \begin{bmatrix} R & \omega \cdot L & 0 \\ -\omega \cdot L & R & 0 \\ 0 & 0 & \frac{R^2 + \omega^2 L^2}{R} \end{bmatrix} \begin{bmatrix} Ed - Vd \\ Eq - Vq \\ E\gamma - V\gamma \end{bmatrix} \tag{3.29}$$

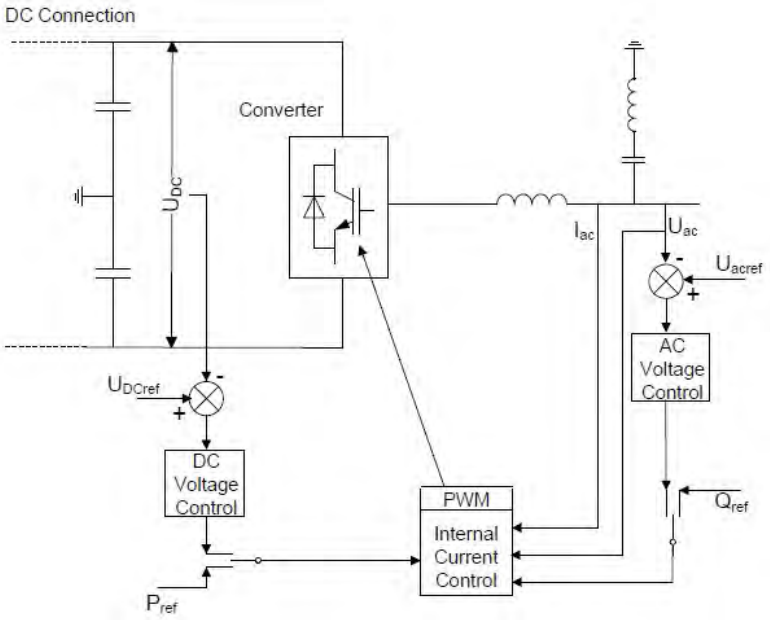


Figure 3.14: General control principle adopted [19].

Finally computing the active power contribute the following expression is found considering that the zero current is negligible:

$$\begin{aligned} P &= vd \cdot id + vq \cdot iq \\ &= \frac{R(vd(ed - vd) + vq(eq - vq)) + \omega L(vd(eq - vq) - vq(eq - vq))}{R^2 + \omega^2 L^2} \\ &= \frac{R(vd(ed - vd) - vq^2)) + \omega L(-vd \cdot vq - vq^2))}{R^2 + \omega^2 L^2} \end{aligned} \tag{3.30}$$

where the quadrature voltage is considered $vq = 0$, condition guaranteed by the PLL (phase looked loop). A similar result can be obtained for the reactive power, again function of the quantities vd and vq. The idea of separated controls for the converter would be feasible knowing the values for active and reactive power that each converter should deliver to the grid. The instantaneous power values should be subtracted from the reference values, producing an error that through two PI controllers produces the reference value for the vd and vq voltages. As equation 3.30 shows the expression of the power is quite complicated and non-linear because square values and products between variables are present. This means more complex loops and difficulties in the controllers tuning.
To avoid these problems, another approach has been followed. Trough measurements dependent on the power plant the active power that can be delivered by single-phase converters and three-phase converters is known. Through an optimization the solution that optimize the power delivered to the grid is found counting all the constraints given

by the switches and additional constraints. This solution consists in the single-phase and three-phase voltage phasors that should be applied and also the power itself that may be different from the power produced by the DC sources. In this way the general control structure can be used: from the optimization the reference values of the total active and reactive power are known. According to equation 3.24 the reference values for id and iq are computed using one PI for the active power and another for the reactive power. The current values are used in two separate current loops that produce as a result the values of the overall converter voltage phasor given by the sum of the single-phases and three-phases contributes. The phasor module and angle δ referred to the grid phasor are therefore known. In order to divide the contributes of the single-phases and three-phases phasors contributes the result of the optimization is used: obviously since the optimization gives the values for the steady state operation, the relative percentage referred to the total phasor is used.
This solution allows to use only four controllers with linear transfer functions. The weakness is that the system has to rely on the optimizer algorithm that may not have convergence or can estimate quantities based on wrong inputs if for example the total impedance change because of a grid failure.

Chapter 4

Grid model and filter impedance

The first step in order to obtain some parameters to work with is the grid equivalent model definition and the filter impedance design. With some hypothesis and considering the normal practice rules adopted in the existing systems it is possible to define some feasible values for the resistances and inductances.

4.1 Per unit system

The per unit (p.u.) adopted system uses the following parameters:

- General parameters:
  $P_{base} = 7\ [MVA]$;
  $\omega_{base} = 2 \cdot \pi \cdot f = 2 \cdot \pi \cdot 60 = 376.99\ [rad/sec]$;

- Grid side parameters:
  $V_{base} = \sqrt{\frac{2}{3}} \cdot V_{grid} = \sqrt{\frac{2}{3}} \cdot 1000 = 816.5\ [V]$;
  $I_{base} = \frac{2 \cdot P_{base}}{3 \cdot V_{base}} = \frac{2 \cdot 7 \cdot 10^6}{3 \cdot 816.5} = 5.716\ [kA]$;
  $Z_{base} = \frac{V_{base}}{I_{base}} = \frac{816.5}{5716} = 0.1429\ [\Omega]$;
  $L_{base} = \frac{Z_{base}}{\omega_{base}} = \frac{0.1429}{376.99} = 378.94\ [\mu H]$;
  $C_{base} = \frac{1}{\omega_{base} \cdot Z_{base}} = \frac{1}{376.99 \cdot 0.1429} = 18.6\ [mF]$;

- Simulink p.u. default system:
  $Ps_{base} = \frac{P_{base}}{3}$;
  $Vs_{base} = \frac{V_{base}}{\sqrt{2}}$;
  $Is_{base} = \frac{I_{base}}{\sqrt{2}}$
  $Zs_{base} = \frac{Vs_{base}}{Is_{base}} = Z_{base}$;

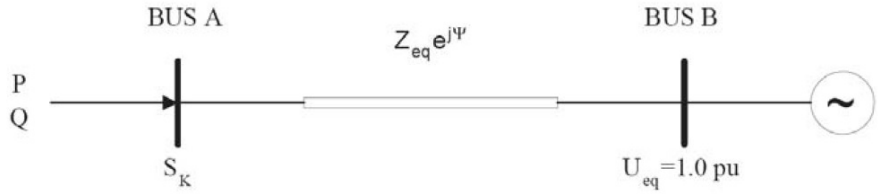


Figure 4.1: Grid equivalent model [24].

4.2 Grid model

Using the Thevenin's equivalent circuit for the grid as shown in figure 3.10, the parameters to be defined are the grid voltage, the frequency, the resistance and the inductance. These parameters are usually given in an implicit way using a concatenate RMS voltage V_{eq}, a frequency f, a three-phase short circuit apparent power S_{cc} and a power factor of the grid impedance ψ. Obviously the relations are the following:

$$S_{cc} = \frac{V_{eq}}{\sqrt{R_{eq}^2 + X_{eq}^2}} \tag{4.1}$$

$$\psi = \arctan\left(\frac{X_{eq}}{R_{eq}}\right) \tag{4.2}$$

$$Z_{eq} = R_{eq} + j \cdot X_{eq} = Z_{eq} \cdot e^{j \cdot \psi}. \tag{4.3}$$

An important concept to discuss when a grid connected inverter is studied is the "weak" or "strong" grid behaviour. Considering a power plant grid connected with a nominal power Pn the ratio $\frac{S_{cc}}{Pn}$ is the index that gives an idea of the grid strength. According to [24], a grid is generally said to be weak when changes in the active and reactive power flows of the connected converters will cause a significant change in the voltage amplitude in the connection point and in neighbouring points on the network. The networks are generally weaker in rural areas than industrial and urban areas. The meaning of weak grid written in terms of short-circuit ratio may be: $\frac{S_{cc}}{Pn} < 25$ for weak grids, $\frac{S_{cc}}{Pn} > 25$ for strong grids.
The grid impedance angle also depends on the type of network: while the transmission lines offer mostly an inductive contribute with angles between $55 - 85°$, the distribution grids are more resistive ranging between $25 - 55°$.
In the studied case the power plant can be set to $Pn = 7\ [MW]$ and the grid concatenate voltage may be assumed to be $V = 1\ [kVrms]$ with frequency $f = 60\ [Hz]$.
A good choice for the grid parameters in the hypothesis of "weak grid" could be:

- $\frac{S_{cc}}{Pn} = 20$, weak grid when the maximum power is delivered;
- $\frac{R}{X} = k_{gr} = 0.3$, reasonable for this voltage level.

In this hypothesis the grid impedance is calculated as:

$$Z_{eq} = \frac{V_{eq}^2}{S_{cc}} = \frac{1000^2}{20 \cdot 7} = 0.0071 \ [\Omega] \tag{4.4}$$

$$L_{grid} = \frac{Z_{eq}}{\sqrt{1 + k_{gr}^2} \cdot \omega} = 18.41 \ [\mu H] \tag{4.5}$$

$$R_{grid} = k_{gr} \cdot L.\omega = 2.1 \ [m\Omega] \tag{4.6}$$

With these parameters the grid is strong for low power produced by the converter and becomes weak near the nominal power operation.

4.3 Filter impedance

The filter impedance is necessary to allows the inverter connection with the grid. As shown in the previous chapter this impedance appears in the voltages-currents relations. The effect of this impedance is a reduction of the voltage harmonics injected into the grid and a reduction of the current distortion.
Many filter configurations have been proposed:

- L filter: simple first order filter with an attenuation factor of $-20dB/dec$; the switching frequency should be high in order to attenuate the inverter harmonics.
- LC filter: second order filter giving $-40dB/dec$ attenuation factor. The capacitor is added to suppress the high frequency harmonics while it should provide an high impedance in the control frequency range. The resonant frequency must be evaluated in order to avoid resonances with voltage harmonics produced by the inverter.
- LCL filter: third-order filter with an attenuation factor of $-60dB/dec$. This filter provides a low grid current distortion and reactive power and it's suggested when low switching frequencies are used. The price to be paid is the higher complexity due to the introduced resonance.

The filter impedance optimal value is found as the good compromise counting many factors: weight, cost and time response of the circuit are decreased with low values of the inductance while the current ripple becomes higher.
Using the equation 3.21 here reported:

$$P = \frac{3 \cdot V \cdot V_{grid} \sin(\delta)}{X} \tag{4.7}$$

in the hypothesis of negligible resistance the power delivered to the grid is inversely proportional to the inductive reactance. Therefore for a given power target that must be delivered the choice on the inductance is directly related to the DC bus voltage that must

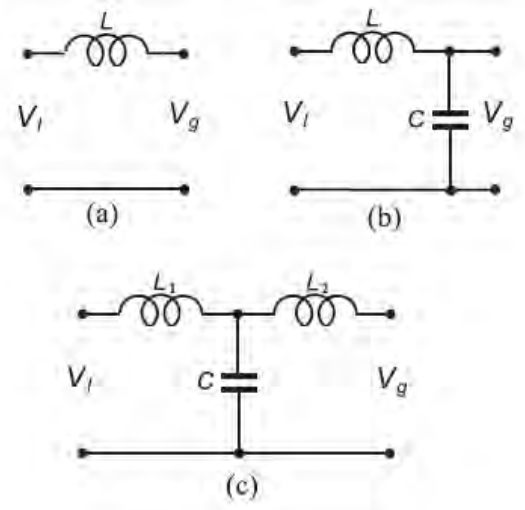


Figure 4.2: L, LC, LCL filters.

be used. Considering that the current phasor is aligned with the grid voltage phasor, this expression can be used:

$$P = \frac{3 \cdot V_{grid}}{X} \cdot \sqrt{V^2 - V_{grid}^2} \tag{4.8}$$

and therefore:

$$V_{dc} = V \cdot 2 \cdot \sqrt{2} = 2 \cdot \sqrt{2} \cdot \sqrt{\frac{-V_{grid} + \sqrt{V_{grid}^2 + 4 \cdot \left(\frac{P \cdot X}{3}\right)^2}}{2}} \tag{4.9}$$

The obtained result is shown in figure 4.3 for a unitary transformer ratio and considering the maximum modulation index used in the converters. The DC voltage V_{dc} in the selected topology is the sum of the voltages of three-phase converters and single-phase converters reported to the grid side.

In the circuit scheme presented in 3.10 many components give a contribute for the filter impedance. The total impedance is given by:

$$R_{pu} = Rpu_{filter} + Rpu_{T1} + Rpu_{T2} + 2 \cdot Rpu_{ZSBT} \tag{4.10}$$

$$L_{pu} = Lpu_{filter} + Lpu_{T1} + Lpu_{T2} + 2 \cdot Lpu_{ZSBT} \tag{4.11}$$

In this thesis the parameters in table 4.1 have been considered. The filter reactive inductance has been set to $L_{pu} = 0.157$, but this value can be changed in order to fulfil the harmonics and THD requirements for currents and voltages that must be verified with the interleaving technique. Zero sequence blocking transformers are considered to obtain low positive sequence impedances.

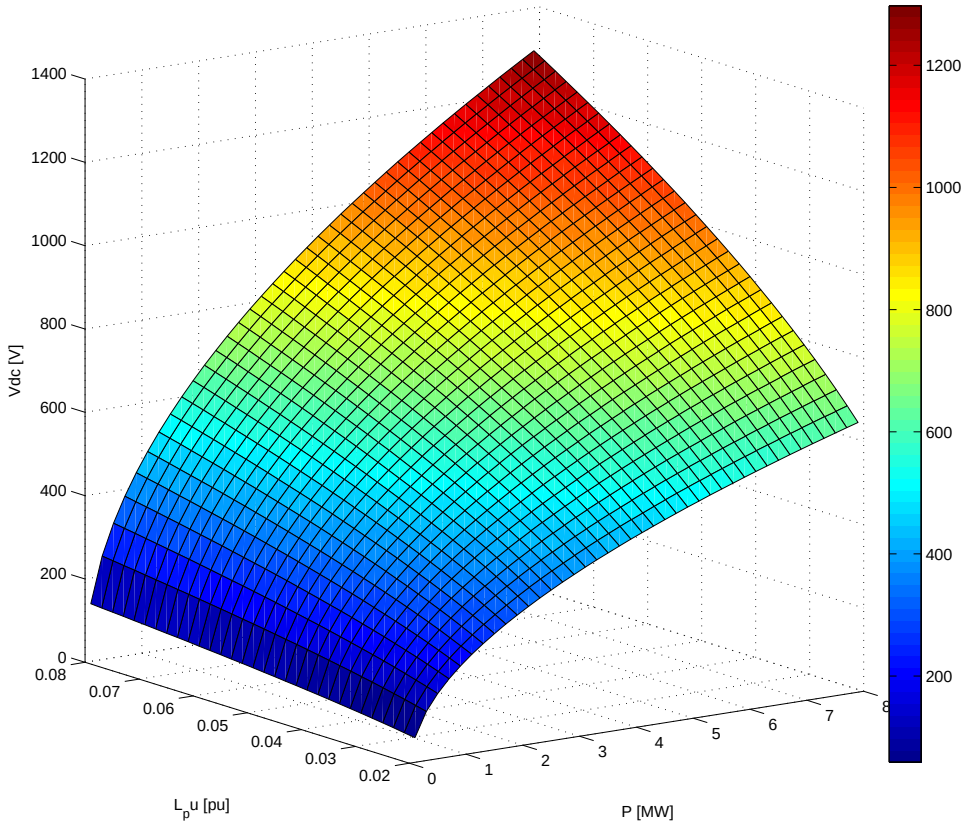


Figure 4.3: V_{dc} obtained considering unitary the transformer ratio.

Component	Parameter	Value
Grid	R_{pu}	0.0144 pu
	L_{pu}	0.0479 pu
Transformer	R_{pu}	0.013 pu
	L_{pu}	0.06 pu
2 ZSBT	R_{pu}	0.005 pu
	L_{pu}	$6.6 \cdot 10^{-4}$ pu
Filter impedance	R_{pu}	0.01 pu
	L_{pu}	0.157 pu
Total	R_{pu}	0.0424 pu
	L_{pu}	0.2593 pu

Table 4.1: Used parameters in per unit system.

Chapter 5

Optimization

Depending on the nature of the power plant, different measurements can be implemented to find the value of power that is possible to extract; for example considering photovoltaic cells some measurements based on the assessment of the solar irradiation can be used or the wind speed should be evaluated for a wind power plant. When the power that can be delivered by each source is known the reference power value must be found for all the converters.
In a simple case the problem could be solved analytically: the minimum value of the single-phase powers is taken as single-phase reference, then this value is added to the three-phase reference and the total power is found. To deliver the maximum power to the grid the reactive component of the current that flows through the switches should be null, equivalent to the condition $\cos(\phi) = 1$. Therefore the following expression can be used:

$$I = \frac{3 \cdot 2 \cdot P_m + 2P_t}{\sqrt{3} \cdot V_{grid} \cdot \cos(\phi)} \tag{5.1}$$

where P_m and P_t are the single and three-phase power associated to only one converter (one arm of the mono-phases and one three-phase converter). Considering that the connection impedance parameters are known, the total voltage drop phasor on this impedance can be calculated and finally the components of the converter voltage (phase δ and amplitude) are known. In the final step the voltage values for each converter can be calculated as:

$$Vm = \frac{P_m}{I \cdot \cos(\phi)} \qquad Vt = \frac{P_t}{\sqrt{3} \cdot I \cdot \cos(\phi)}. \tag{5.2}$$

The result of this solution is depicted in figure 5.1. This analytical approach effectively works and gives the exact result with a low computational cost and it's possible to implement it in Simulink ®. The biggest drawback is that it's only possible to solve easy configurations and if many constraints are added the problem becomes difficult to be solved analytically and also the implementation complexity is increased because many if checks must be implemented. For example if the switches limits (currents and voltages) and other restrictions on the grid side such as: $\cos(\phi) \neq 1$, current limits in failure cases, THD of the voltage waveform, power drop functions and more complicated

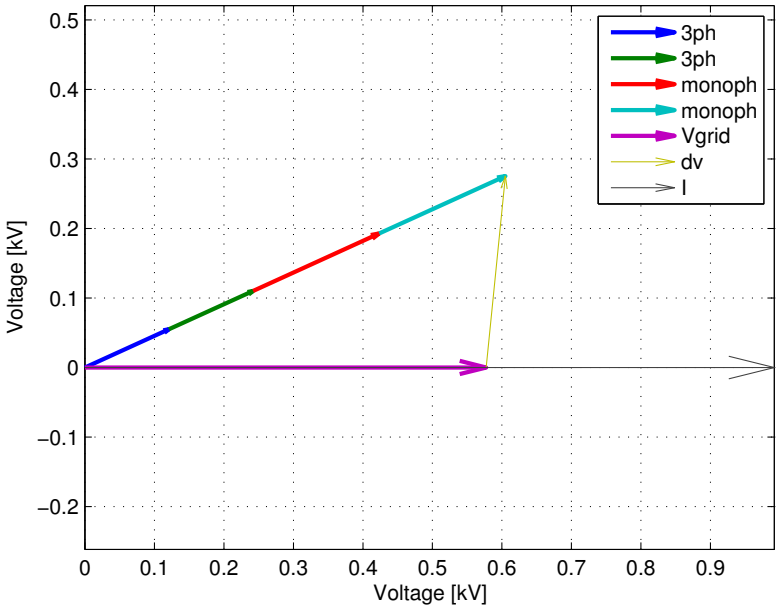


Figure 5.1: Analitycal solution of the optimal problem.

controls must be implemented, the analytical solution becomes infeasible. To overcome all these limitations an optimization script has been used to solve this single-objective problem, that may also become a multi-objective problem depending on the formulation.

5.1 Problem definition

The objective function that the optimizer must maximize in the first simple case is:

$$obj = 6 \cdot P_m + 2 \cdot P_t - 3 \cdot R \cdot I^2 \tag{5.3}$$

where the variables of the optimization are:

$$x = (V_m, V_t, I, \phi, \delta, Pm, Pt) \tag{5.4}$$

V_m and V_t are the single and three-phase voltage phasor amplitudes, I is the current module, ϕ is the angle between the grid voltage and current phasors considered positive in the clockwise direction, δ is the angle between the converter voltage phasor and grid voltage phasor considered positive in the anti-clockwise direction, Pm and Pt are the active powers delivered by each converter. The angle ϕ is kept as variable in order to allows the converter to help the grid voltage regulation. For this function additional conditions must be considered and for now to keep the problem simple ψ is fixed equal

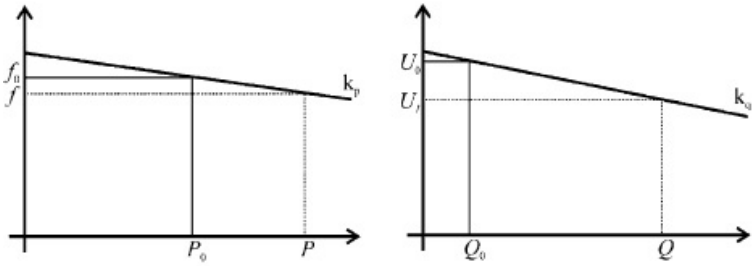


Figure 5.2: Typical frequency and voltage droop when X»R [20].

to 0 (condition that has to be removed obviously if $\phi \neq 0$). The constraints that the solver must take into account are divided in equality and inequality constraints:

$$\begin{cases} Pm = Vm \cdot I \cdot \cos(\phi + \delta) \\ Pt = 3 \cdot Vt \cdot I \cdot \cos(\phi + \delta) \\ 2 \cdot (Vt + Vm) \cdot \cos(\delta) - \frac{V_{grid}}{k_{transformer}} - R \cdot I \cos(\phi) - \omega L \cdot I \cdot \sin(\phi) = 0 \\ 2 \cdot (Vt + Vm) \cdot \sin(\delta) - \omega L \cdot I \cos(\phi) - R \cdot I \cdot \sin(\phi) = 0 \\ \phi = 0 \end{cases} \tag{5.5}$$

$$\begin{cases} 0 \leq Pm \leq Pm_{lim} \\ 0 \leq Pt \leq Pt_{lim} \\ 0 \leq I \leq I_{lim} \\ \phi_{min} \leq \phi \leq \phi_{max} \\ 0 \leq \delta \leq \delta_{lim} \\ 0 \leq Vm \leq V_{lim} \\ 0 \leq Vt \leq V_{lim} \end{cases} \tag{5.6}$$

Pm_{lim} and Pt_{lim} are power limits known by environmental measurements; I_{lim}, V_{lim} are the switches limits and the grid voltage is reported to the converter side through the turns ratio of the transformer. δ obviously must be positive and the conditions on ϕ is dependent on the system: if a frequency and voltage droop function must be implemented, the standard limits on power factor can be chosen according to $IEEE$ standards (for example $\cos(\phi) > 0.85$ lagging or leading for solar PV systems, $IEEE$ 929). A typical example of voltage and frequency droop functions is depicted in 5.2 when $X >> R$. Since this configuration is suitable for low and medium voltage applications, this condition might not be respected and in some weak low voltage grids $R >> X$. In this case a good solution that uses fictitious P and Q is proposed in [20].

5.2 Lookup table concept

The parameters Pm and Pt changes according to the irradiation, wind condition or others factors. In this way the optimization should be run in each instant to match the right set of parameters. The solution of a time-running optimization would have an high computational cost and the drawback of the convergence: if in some cases the solution is not found the control of the system will be lost; a typical example could be the initial point choice. For this purpose in this work the look-up tables were used: the input parameters for the algorithm are Pm and Pt, variable in a certain range in order to cover all the combinations. The same approach has been used in [21] for offshore wind parks with wind turbines serialized in the DC side. The optimization is run before the converter operation and the results are stored in look-up tables that ensure a fast response. The advantage of this method is that if one optimization operation fails, the output function can be easily re-shaped with a smoothing. The drawback is related to the quantity of data that should be stored and many inputs are also required for the look-up tables if the problem is complex (with many inputs).

5.3 Results

5.3.1 Pgenerated<Plim

The optimizer that has been used is the function $fmincon$ of the Matlab ® *Optimization toolbox*^{TM}, a deterministic optimizer able to solve non linear constrained problems. The range chosen for single and three phase powers and the other data are:

- $Pm = [0 : 0.8]MW$
- $Pt = [0.5 : 1]MW$
- $Imax = 2\ kArms$
- $Vmax = 600\ Vrms$
- $ratio_{transformer} = 1 : 2;\ V_{grid} = 1\ [kVconc]$
- $R_{pu} = 0.0315\ pu,\ L_{pu} = 0.2593\ pu$

With these parameters the expected maximum power is:

$$Plim = \sqrt{3} \cdot V_{grid} \cdot ratio_{transformer} \cdot Ilim = \sqrt{3} \cdot 2000 \cdot 2000 = 6.928\ [MW] \tag{5.7}$$

while the top combination of generated powers gives:

$$Pmax = 6 \cdot Pm + 2 \cdot Pt = 6.8\ [MW]. \tag{5.8}$$

The converter has the capability to deliver the maximum power generated by the sources. This could be a scenario when the peak of the produced power must be completely exploit, thus when the probability to work near this maximum power point is high.

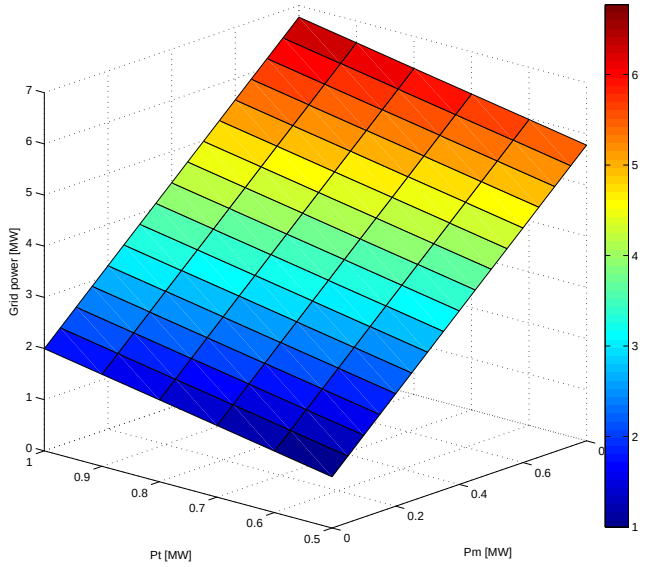


Figure 5.3: Power delivered to the grid in [MW].

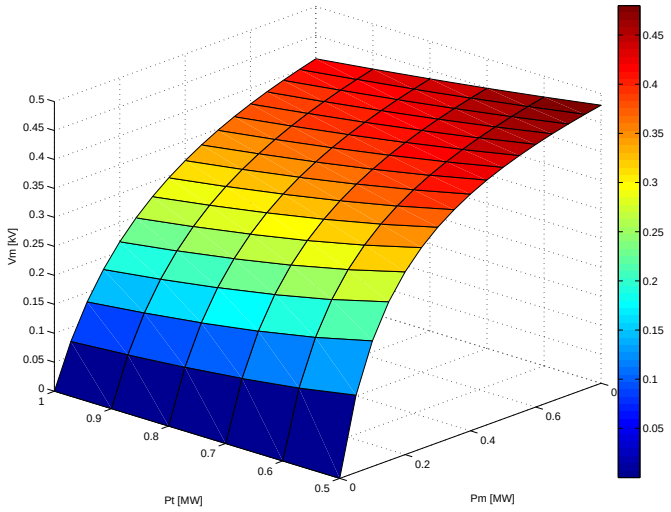


Figure 5.4: Voltage phasor of the single-phase converter.

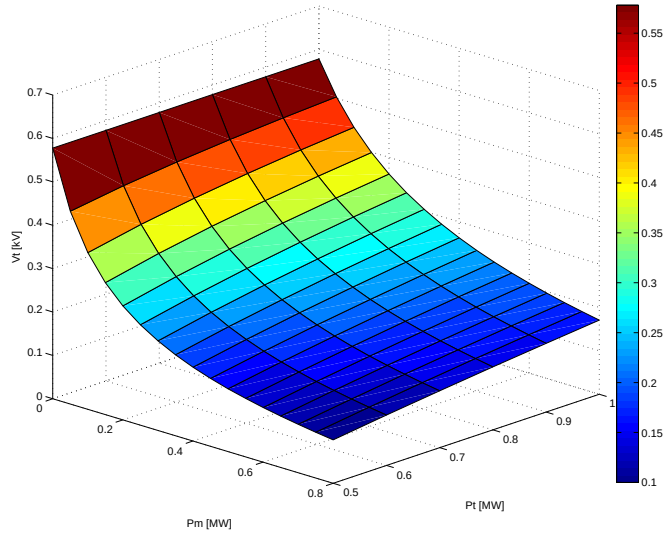


Figure 5.5: Voltage phasor of the three-phase converter.

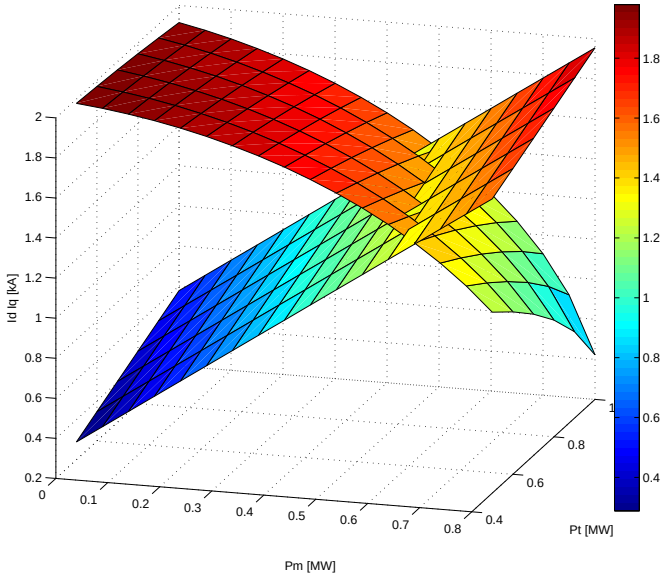


Figure 5.6: Required Id and Iq limit surface.

The voltage phasor of the single-phase converter is zero in case of NULL power delivered by the DC source. This case could represent effectively the non production state or the single-phase converter failure. In the hypothesis of failure of one single-phase converter all the others must be switched off and the only converters still active are the three-phases. In this case the current will flow through the clamping diodes of the single-phase converters. Considering the case of failure of only one leg of the single-phase converter (half converter), the optimizer algorithm can still be used modifying the objective and the non-linear constraints.
Figures 5.3,5.4,5.5 5.6 show the optimization result for the set of parameters given at the beginning of the chapter. As discussed before the reactive power is kept to zero and figure 5.6 shows the Iq current limit that the converter is able to deliver for each power condition. This curve will be useful if a dynamic control on Id and Iq is required to limit the current in case of three-phase fault on the grid side.
From figures 5.4 and 5.5 as discussed in 3.3.2 the ratios $\frac{Vm}{2 \cdot Vt + 2 \cdot Vm}$ and $\frac{Vt}{2 \cdot Vt + 2 \cdot Vm}$ must be calculated.

5.3.2 Pgenerated>Plim

An interesting choice cold be to design the power plants in order to obtain a maximum power peak higher than the deliverable power. This case is interesting for example when the probability to have single-phases and three-phase DC sources working at the highest power point at the same time is low. In this hypothesis another constraint condition should be added to the optimizer to keep uniformity on the solution when the limit current is reached. In fact when $I = Ilim$, the solver find a feasible solution but without constraints on the power that must be limited and as a result both the single and three phase powers are limited. A better solution could be to limit only the single-phase power when the current limit is reached because a power limiting system is already present if the single-phase converters have different DC sources. This means that the three-phase converter power can reach his limit without limitations to be implemented while some limitation mechanism must be used for the single-phases sources, such as the pith regulation for example. This set has been used:

- $Pm = [0 : 1] MW$
- $Pt = [0.5 : 1] MW$
- $Imax = 2\ kArms$
- $Vmax = 600\ Vrms$
- $ratio_{transformer} = 1 : 2;\ V_{grid} = 1\ [kVconc]$
- $R = 2.4 m\Omega,\ X = 0.788 \mu H$

With these parameters the expected maximum power is:

$$Plim = \sqrt{3} \cdot V_{grid} \cdot ratio_{transformer} \cdot Ilim = \sqrt{3} \cdot 2000 \cdot 2000 = 6.928\ [MW] \quad (5.9)$$

while the top combination of generated powers gives:

$$Pmax = 6 \cdot Pm + 2 \cdot Pt = 8\ [MW] \quad (5.10)$$

The converter is not able to deliver the maximum generated power.
In figure 5.7 the power limit is visible corresponding to the current limit shown in figure 5.10. In figure 5.11 the generated powers for single-phase and three-phase sources are shown: as explained the three-phase source reach the source power limit while the single-phase power is limited to avoid over-currents.

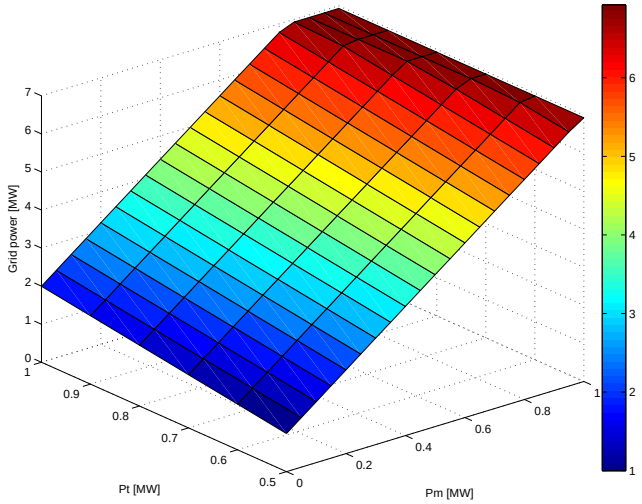


Figure 5.7: Power delivered to the grid in [MW].

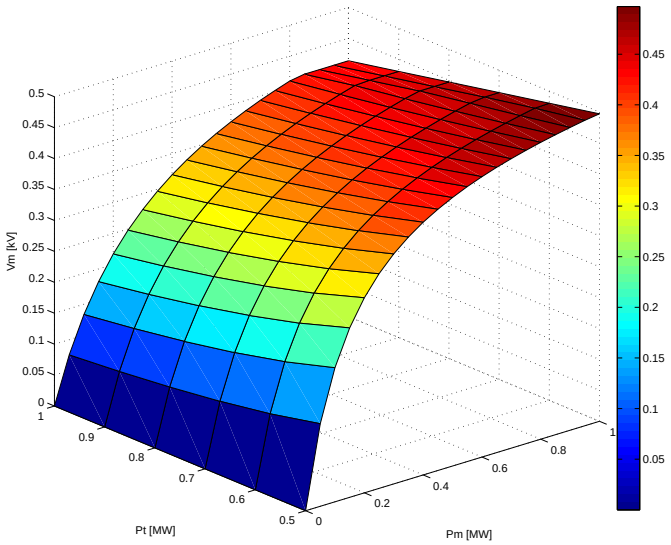


Figure 5.8: Voltage phasor of the single-phase converter.

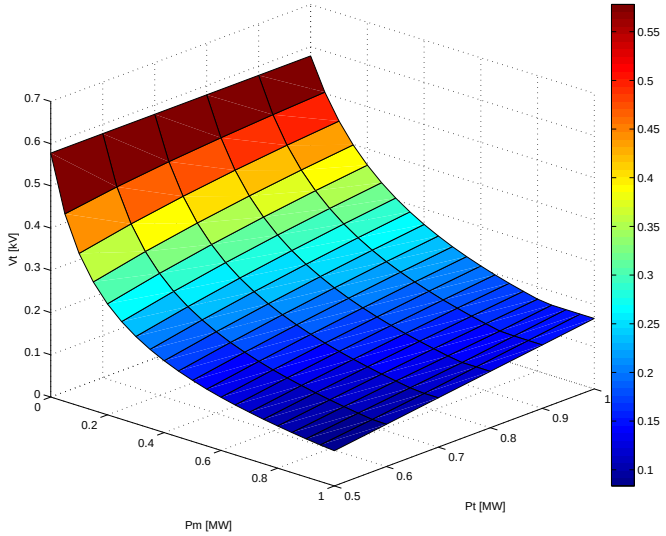


Figure 5.9: Voltage phasor of the three-phase converter.

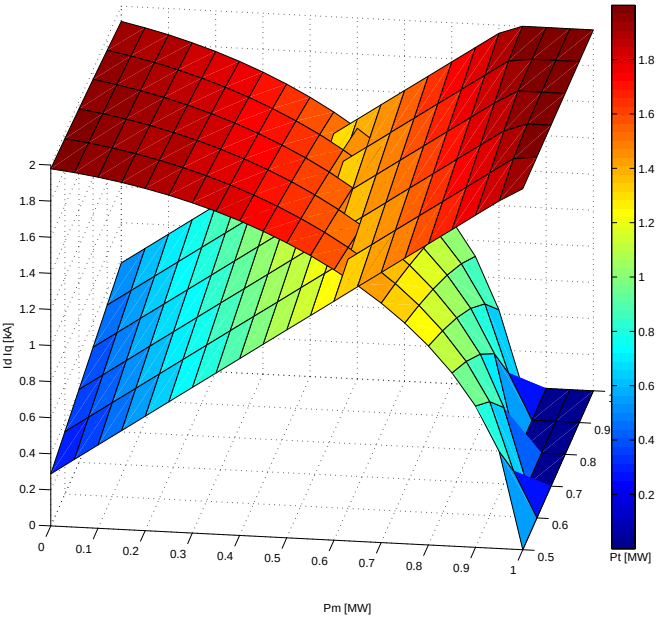


Figure 5.10: Required Id and Iq limit surface.

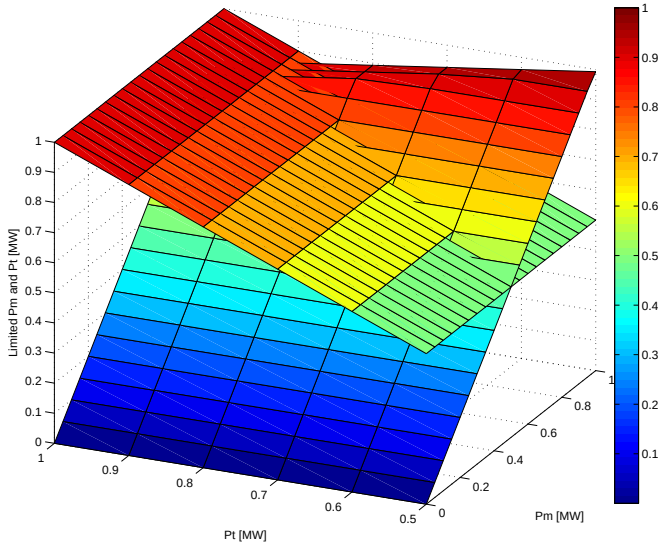


Figure 5.11: single-phase and three-phase power.

Chapter 6

Control structure

Starting from the considerations in 3.3.2, the control scheme structure can be built. The loop control consist of PI controllers implemented in the rotating coordinate system dq. Totally four loops are built: two internal current loops and two external power loops.
The use of a rotating coordinate system requires obviously a device that allows the control to work synchronously with the grid voltage triple of phasors. This device is a three phase PLL (phase locked loop). As shown in figure 6.1, the PLL uses an internal oscillator that is controlled in order to keep the phase difference referred to the input zero. In this way the grid phasors are tracked in phase and amplitude, and the signal ωt can be applied in the $\alpha\beta - dq$ transform that in steady state operation and considering a balanced grid gives: $(Ed \neq 0; Eq = 0)$.

6.1 Internal loops

Figure 6.2 shows the general control scheme adopted for current loops. In the topology studied in this thesis the controller works on the overall system as explained in 6.2 and the voltage reference V_{CONV} is split in single-phase and three-phase reference values through the ratios calculated in the optimization script and stored in look-up tables. Considering that the time required for the memory reading operation is negligible in comparison with the other time constants of the system, the loop scheme remain valid in first approximation.
Using equation 3.23 here reported the transfer functions that regulate the system can be found.

$$\begin{bmatrix} Ed - Vd \\ Eq - Vq \\ E\gamma - V\gamma \end{bmatrix} = \begin{bmatrix} R & -\omega \cdot L & 0 \\ \omega \cdot L & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} \tag{6.1}$$

As shown in the equation and in the open loop scheme presented in 6.3, the off-diagonal terms of the $3x3$ matrix cause a cross-coupling between the d and q axes that must be removed in order to keep simple the tuning of the PI parameters. This cross-coupling will be removed using the usual ωI feed-forward.
The inverter introduces a delay that together with the used sampling time must be

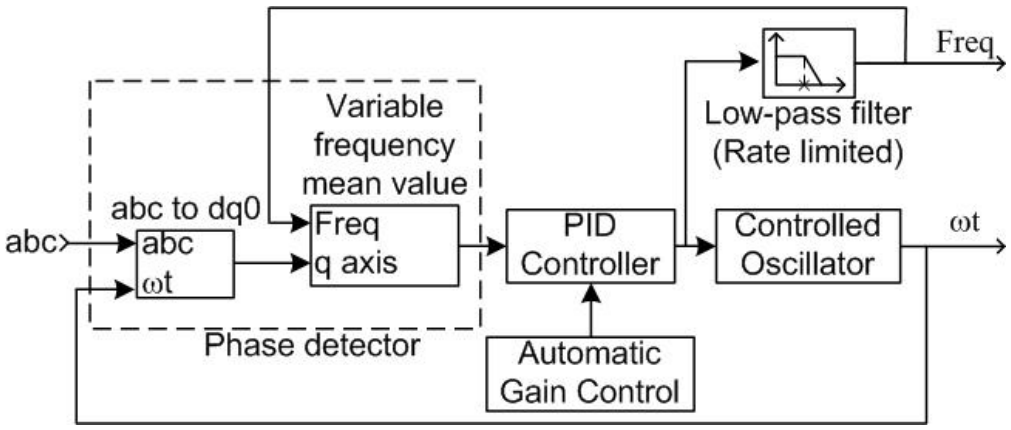


Figure 6.1: Three phase PLL block diagram [22].

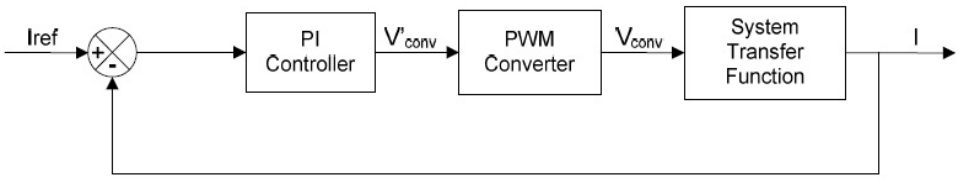


Figure 6.2: Id and Iq general loop [19].

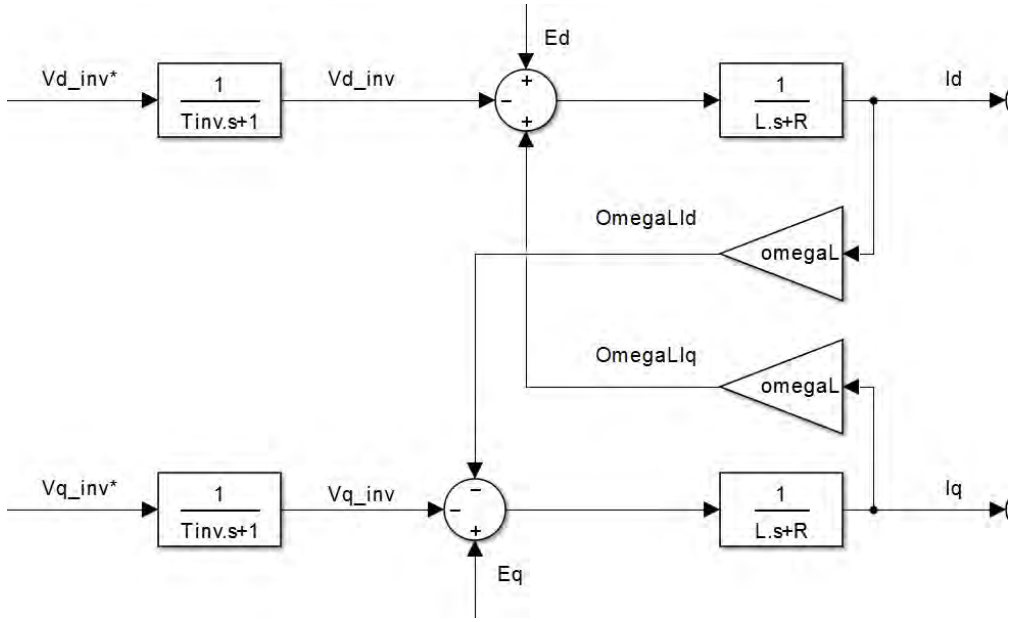


Figure 6.3: Transfer function scheme with the adopted convections (open loop).

taken into account since the real model works in discrete-time domain. The general approximation uses as a delay time half triangular carrier time period, thus the inverter transfer function becomes:

$$G_{INV}(s) = \frac{1}{1 + Tinv \cdot s} = \frac{1}{1 + \frac{1}{2 \cdot f_{sw}} \cdot s} \tag{6.2}$$

The inverter is therefore modelled with a simple stable pole. In order to consider the time delay introduced by the sampling operation, a similar transfer function is used:

$$G_{SAMPL}(s) = \frac{1}{1 + Tsample \cdot s} \tag{6.3}$$

where $Tsample$ is the sample time and also the lowest time constant of the system. According to figure 6.2 the voltage Vd_{inv} and Vq_{inv} produced by the inverter must be proportional to the current error expressed as a difference between $(I_{REF} - I_{measured})$. Moreover as shown in figure 6.4 and in equation 6.5, the decoupling contributes and feed forward must be included. The voltages become:

$$\begin{cases} Vd_{inv} = (-(Id_{ref} - Id) \cdot G_{PI} + Ed + \omega LIq) \cdot \frac{1}{Tsampl \cdot s + 1} \cdot \frac{1}{Tinv \cdot s + 1} \\ Vq_{inv} = (-(Iq_{ref} - Iq) \cdot G_{PI} + Eq - \omega LIq) \cdot \frac{1}{Tsampl \cdot s + 1} \cdot \frac{1}{Tinv \cdot s + 1} \end{cases} \tag{6.4}$$

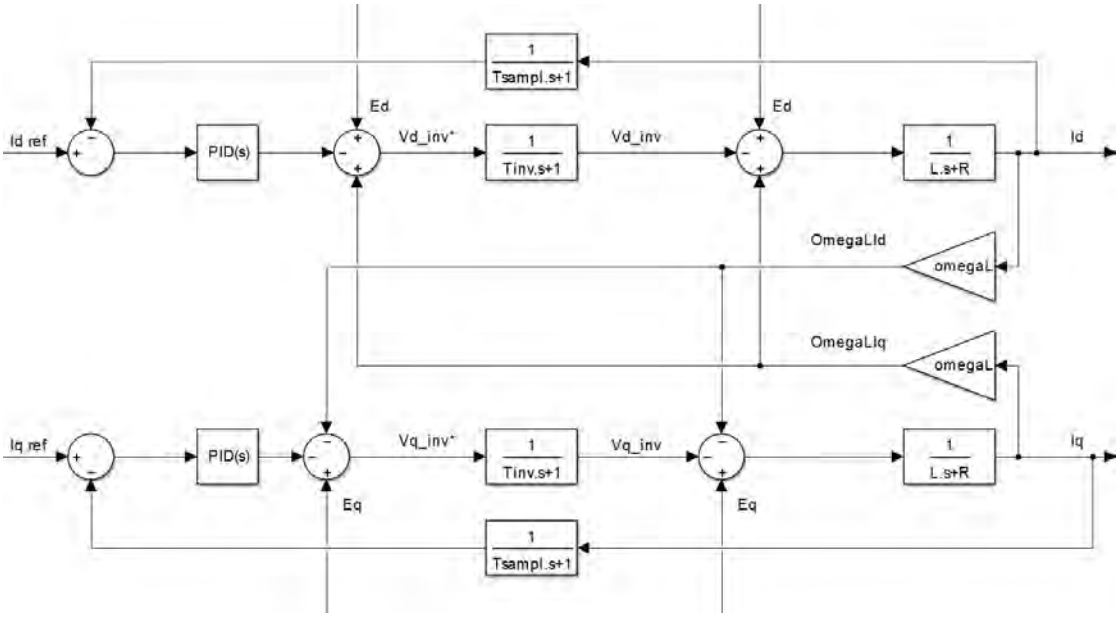


Figure 6.4: Transfer function scheme with the adopted convections (closed loop).

To verify the decoupling action, substituting equation 6.4 in equation 6.5 and considering $Tsample$ and $Tinv$ negligible, the result is a decoupled system of equations:

$$\begin{bmatrix} (Id_{ref} - Id) \cdot G_{PI} \\ (Iq_{ref} - Iq) \cdot G_{PI} \\ E\gamma - V\gamma \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} Id \\ Iq \\ I\gamma \end{bmatrix} \tag{6.5}$$

As equation 6.4 shows, in systems with this structure the dynamical response can generally be improved using a feed forward weighted by the reciprocal of the transfer function $\frac{1}{Tinv \cdot s+1}$. In this specific case when the PLL tracks the grid reference $Eq = 0$ and $Ed = constant$ considering only the positive sequence voltage and considering to track directly the voltage equivalent generators (valid in the hypothesis of strong grid with high PCC). With these assumptions the feed forward compensation is not necessary; the neglected term is:

$$G_{feed} = \frac{(1 + T_{inv} \cdot s)}{(1 + T_{pole} \cdot s)} \tag{6.6}$$

where a pole with $T_{pole} < T_{sample}$ have been added in order to obtain a finite gain with $s \to \infty$.

6.2 Current loop PI tuning

The equation that represents the PI transfer function is:

$$G_{PI} = K_P + \frac{K_i}{s} = K_P \cdot \left(\frac{1 + T_i \cdot s}{T_i \cdot s} \right) \tag{6.7}$$

where the proportional term K_P and the time constant $T_i = \frac{K_P}{K_i}$ are the result of the tuning process.
The most used tuning technique that guarantee a fast response for the inner system is the *modulus optimum*: for a given transfer function where many time constants appear, the slowest pole is deleted with the PI zero and the gain is chosen in order to keep the bandwidth of the system as high as possible, satisfying the requirements on the phase margin. This method is quite diffused because it's really simple and it guarantees fast response [19].
Looking at figure 6.4 the global transfer function of the Id and Iq loops may be found :

$$G_{OL} = \frac{1}{Tsample \cdot s + 1} \cdot \frac{1}{Tinv \cdot s + 1} \cdot \frac{1}{R(T_{LR} \cdot s + 1)} \tag{6.8}$$

where T_{LR} is the time constant of the RL filter used to connect the converter with the grid; this time constant is the slowest of the system because it's related to electrical processes. The pole with $Tsample$ time constant quantifies the additional delays introduced by the sampling operation of Id and Iq.
Introducing also the PI transfer function, the following equation is obtained:

$$\begin{aligned} G_{OL+PI} &= K_P \cdot \left(\frac{1 + T_i \cdot s}{T_i \cdot s} \right) \cdot \frac{1}{Tsample \cdot s + 1} \cdot \frac{1}{Tinv \cdot s + 1} \cdot \frac{1}{R(T_{LR} \cdot s + 1)} \\ &= \frac{K_P}{R \cdot T_{RL} \cdot s \cdot (Tsample \cdot s + 1) \cdot (Tinv \cdot s + 1)} \end{aligned} \tag{6.9}$$

Approximating the transfer function and neglecting T_{sample} in comparison with the others time constants of the systems, the expression of the closed loop function has two poles and it is possible to find the damping coefficient and natural frequency [19]:

$$G_{CLO} = \frac{G_{OL+PI}}{1 + G_{OL+PI}} = \frac{K_P}{T_{RL} \cdot R \cdot Tinv \cdot \left(s^2 + \frac{1}{Tinv} \cdot s + \frac{K_P}{T_{RL} \cdot R \cdot Tinv} \right)} \tag{6.10}$$

where using $s^2 + 2\xi\omega_n \cdot s + \omega_n^2$ the equations become:

$$\omega_n = \sqrt{\frac{K_P}{T_{RL} \cdot R \cdot Tinv}} \tag{6.11}$$

$$\xi = \frac{1}{2} \cdot \sqrt{\frac{T_{RL} \cdot R}{K_P \cdot Tinv}} \tag{6.12}$$

Model of controlled plant	K_P	T_I	T_D
$\frac{k}{(T_1 s+1)(T_2 s+1)(T_3 s+1)}$ $T_1 \geq T_2 \geq T_3$	$\frac{T_i}{2kT_3}$	T_1+T_2	$\frac{T_1 T_2}{T_1+T_2}$

Figure 6.5: General choose for PID parameter.

Imposing the absolute value to be 1, the parameter K_P according to modulus optimum criteria is found [19]:

$$\begin{cases} K_P = \frac{T_{RL} \cdot R}{2 \cdot Tinv} \\ Ti = T_{RL} \end{cases} \tag{6.13}$$

obtaining the following values for natural frequency, damping factor and transfer function in closed loop:

$$\begin{cases} \omega_n = \frac{1}{2 \cdot Tinv} \\ \xi = \frac{1}{\sqrt{2}} \end{cases} \tag{6.14}$$

$$G_{CL} = \frac{1}{2 \cdot Tinv^2 \cdot s + 2 \cdot Tinv \cdot s + 1} \tag{6.15}$$

The system bandwidth should be maximized keeping a certain margin from the carrier angular speed: in fact if the current loop is faster than the switching frequency the stability of the system could be compromised because the general law of "outer controller slower" is violated. The bandwidth condition is verified if the criteria above is used but it must be checked if a different choice for the parameter K_P is considered. In fact the bandwidth can be chosen to be equal to a desired crossover frequency in accordance with the condition just discussed.
If the phase margin must be increased in order to obtain a more robust response with reduced overshoot and settling time and improved stability the derivative action can be implemented and the general tuning criteria is found in [23] and reported in figure 6.5.

6.2.1 Results

This set of parameters has been considered in the studied case:

- $f = 60\ [Hz]$
- $f_{switching} = 25 \cdot 60 = 1500\ [Hz]$
- $Tsample = 10\mu s$
- $R_{pu} = 0.0424$
- $L_{pu} = 0.2656$

Parameter	Symbol	Value	Unit
$RLtimeconstant$	T_{RL}	0.0166	$[s]$
Inverter delay	$Tinv$	333	$[\mu s]$
Sampling time	$Tsample$	10	$[\mu s]$

Table 6.1: Id and Iq loops parameters.

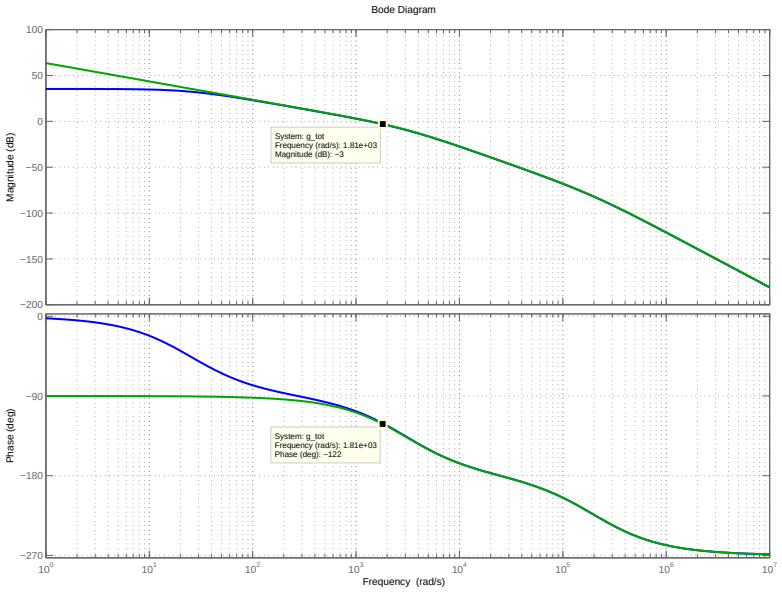


Figure 6.6: Bode's diagram of Id and Iq open loops with PI (green) and without PI(blue).

The useful parameters for the analysis are therefore reported in table 6.1.
The Bode's diagrams have been depicted in 6.6. The gain in steady state ($s \to 0$) tend to be infinite so the error is zero and only the integral part provide the reference value. The bandwidth is approximatively $1.8 \cdot 10^3$ $[rad/sec]$ and the phase margin is near to $P_{margin} = 60°$. The transfer function obtained for Id and Iq using again the approximation of negligible Ts can be written as:

$$\begin{aligned} G_{CL} &= \frac{1}{2 \cdot Tinv^2 \cdot s + 2 \cdot Tinv \cdot s + 1} = \frac{1}{1 + 2 \cdot Tinv \cdot s \cdot (1 + Tinv \cdot s)} \\ &\simeq \frac{1}{1 + \cdot 2 \cdot Tinv \cdot s} \end{aligned} \tag{6.16}$$

This approximation is valid for low frequencies but the difference is visible after the cross-over frequency in figure 6.7. The phase diagram obtained using the real transfer functions

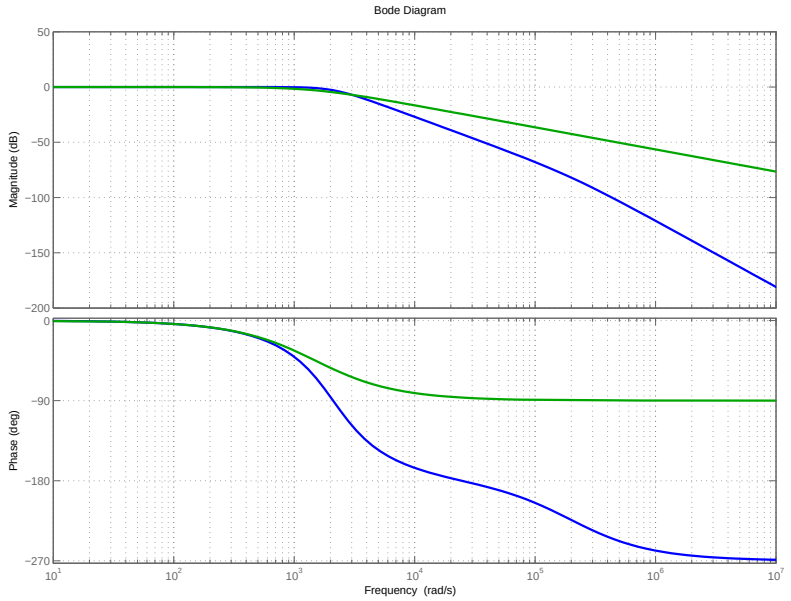


Figure 6.7: Id closed loop Bode's diagram analytical (blue) and with the approximation in 6.16.

reaches $Ph = -270°$ because of the double pole neglected in the approximation.

6.3 PQ loops

The external power loops use a structure similar to the internal current loops because the action of capacitor voltage control is demanded to an external control as explained in 3.3.2. Rewriting the power equation 3.24:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_d \cdot i_d + v_q \cdot i_q \\ j \cdot (v_q \cdot id - v_d \cdot i_q) \end{bmatrix} = \begin{bmatrix} v_d \cdot i_d \\ -j \cdot v_d \cdot i_q \end{bmatrix}. \tag{6.17}$$

the active and reactive power loops can be built as shown in figure 6.8. For simplicity the internal current loops are here modelled with a pole with a Tid time constant that is equal for both the current loops because of the system symmetry. Considering again the approximation introduced in equation 6.16, the obtained system for the power loop is the following:

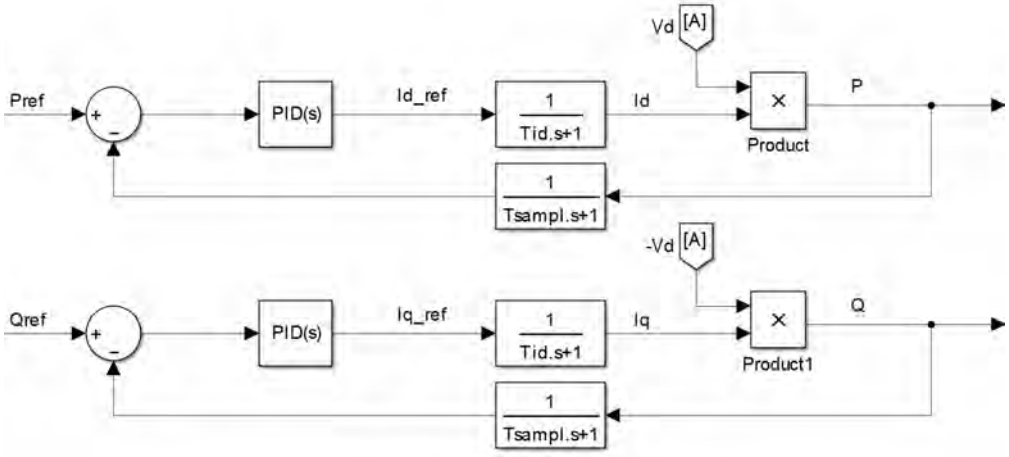


Figure 6.8: Power loops schemes.

$$\begin{aligned} G_{OL+PI} &= K_P \cdot \left(\frac{1+T_i \cdot s}{T_i \cdot s}\right) \cdot \frac{1}{Tsample \cdot s+1} \cdot \frac{1}{2 \cdot Tinv \cdot s+1} \cdot ed \\ &\simeq K_P \cdot \left(\frac{1+T_i \cdot s}{T_i \cdot s}\right) \cdot \frac{1}{2 \cdot Tinv \cdot s+1} \cdot ed \end{aligned} \tag{6.18}$$

neglecting again the time constant $Tsample$ in comparison with the others of the systems. For a system with a transfer function:

$$G = \frac{K}{1+T \cdot s} \tag{6.19}$$

the PI controller should have the parameters $T_i = T$ and $K_P = \frac{T \cdot \omega_p}{K}$, where ω_p is the desired bandwidth for the power loop. In this case the obtained equation is :
$K_P = \frac{2 \cdot Tinv \cdot \omega}{ed}$ and $T_i = 2 \cdot Tinv$.
The amplitude of ed given by the $abc \rightarrow dq$ transformation is always 1 $p.u.$ and the bandwidth of the power loops should be chosen to be lower than the one of the inner loops. According to equation 6.16 and to figure 6.6 the bandwidth of the inner loop is $\frac{1}{2 \cdot Tinv}$, therefore a reasonable choice could be: $\omega_p = \left(\frac{1}{5} - \frac{1}{10}\right) \cdot \omega_i$.

6.3.1 Results

Starting from the results obtained for the $Id - Iq$ loops the results for the power loops are here depicted. In figure 6.9 Bode's diagrams of the power loop with the exact transfer functions (without approximations) are shown. The bandwidth obtained is $\omega_p = 309$ $[rad/sec]$ in accordance with $\omega_c = 1800$ $[rad/sec]$ and the phase margin is $Ph = 90°$.

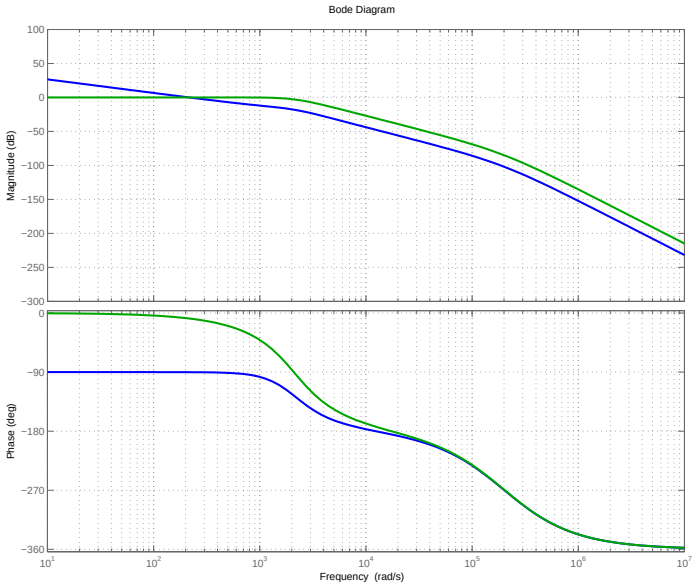


Figure 6.9: Power open loops with PI (blue) and without (green)

6.4 Soft starter

6.4.1 Start-up transient and solution

In the first instants of operation of the converter, an important factor is to ensure that the PLL is tracking the grid reference before applying the power reference signals. If this condition is not verified, in the worst case the converter stability would be compromised especially if the used modulation index is near the maximum. Another disadvantage is the reached current peak: when the inverter is started the power produced by the DC sources is near to the maximum (with the maximum current), the initial transient could result in an over-current that can destroy the switches or reduce their average lifetime. This over-current effect is particularly severe when small inductances are used, which is the goal of the multi-megawatt power plants in order to reduce costs and volumes.
A classical approach used with the induction motors is shown in figure 6.10, where SCR with opposite connection are used. This solution limits the voltage applied to the motor winding during the start-up transient and a similar configuration can be used to limit the current using for example inductances with bypass circuits. Obviously the idea of add an additional inductance is not feasible and therefore a simple power reference limit has been implemented in the control scheme.
Limiting the power reference value there are no limitations on the real current amplitude that may differ from the reference especially during the initial transient when the PLL

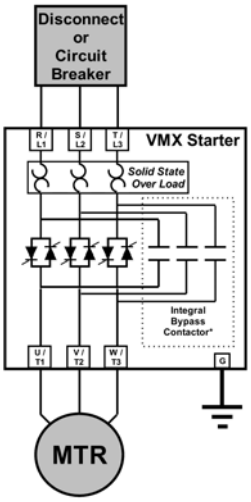


Figure 6.10: Classical soft start used fot induction motors.

is still not tracking the grid signal. In this study the initial current peak is considered to be below the maximum current.
A really simple circuit has been used in this application as depicted in figure 6.11, while the connection scheme is presented in 6.12 with the transfer function block. A certain time is set to keep the power errors equal to zero. During this time the reference value of Id and Iq is fixed to zero that correspond to the lower current condition. The power errors have been selected instead of the power references in order to avoid the integration effect of the PI controllers. When the initial transient time is finished the real reference value is applied and the PIs start their normal operation. An external error reset has been implemented if the control architecture need to avoid the wind condition up of the PIs.

6.4.2 Results

In figure 6.13 the results for the initial operation of the converter are depicted. The power delivered is near the maximum and the modulation index is kept high in order to maximize the switches utilization and to minimize the required DC voltage. The parameters are: $P = 6 \cdot Pm + 2 \cdot Pt = 6.8\ [MW]$, modulation index $= 0.95$, $Imax = \frac{Imax_{switches}}{k_{transformer}} = 4\ [kA]$.

As shown in figure 6.13 the P power loop output saturates to -1 during the start-up and causes the current overshoot. This is clearly visible in figures 6.14 and 6.15. The delay visible in the plots is due to the delays introduced by the control structure (sampling effect). According to the adopted conventions, the power is negative if the converter works as an inverter.

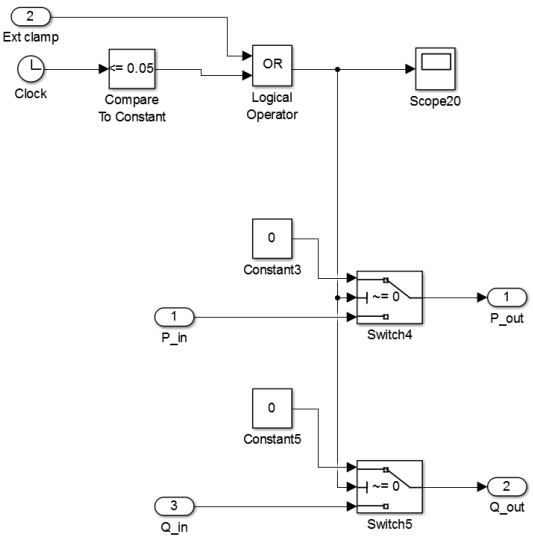


Figure 6.11: Classical soft start used for induction motors.

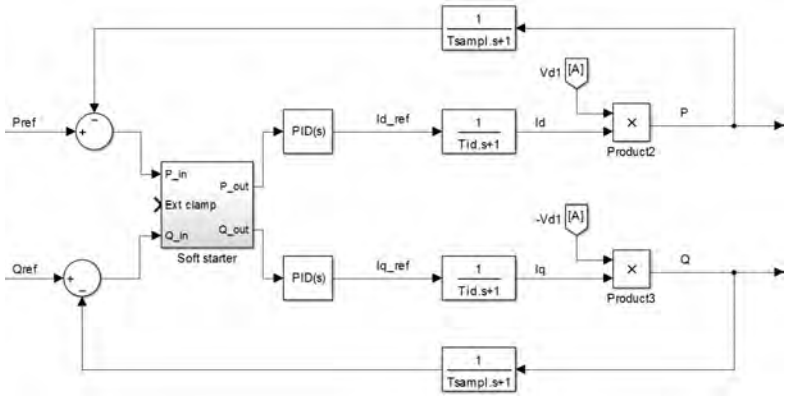


Figure 6.12: Connection scheme of the soft start circuit.

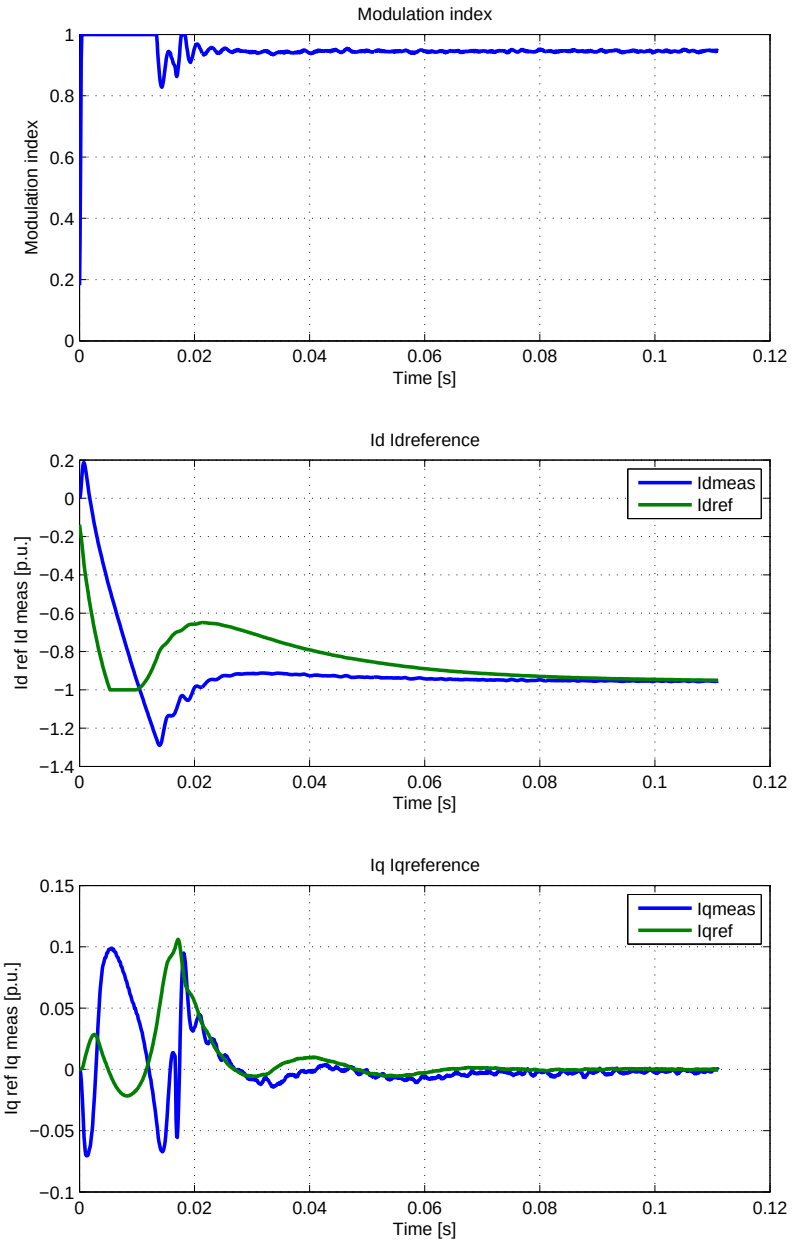


Figure 6.13: Control signals without soft starter.

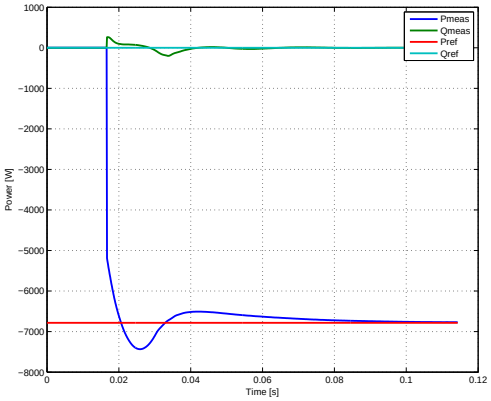


Figure 6.14: Active and reactive powers [W] without soft starter.

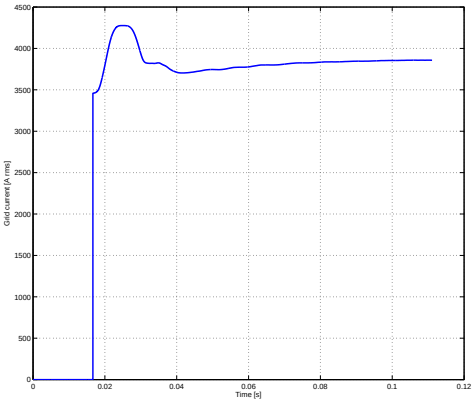


Figure 6.15: RMS grid current without soft starter.

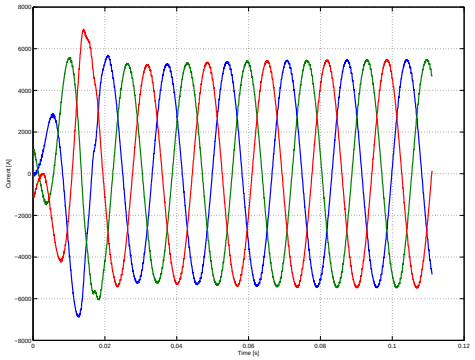


Figure 6.16: RMS grid current without soft starter.

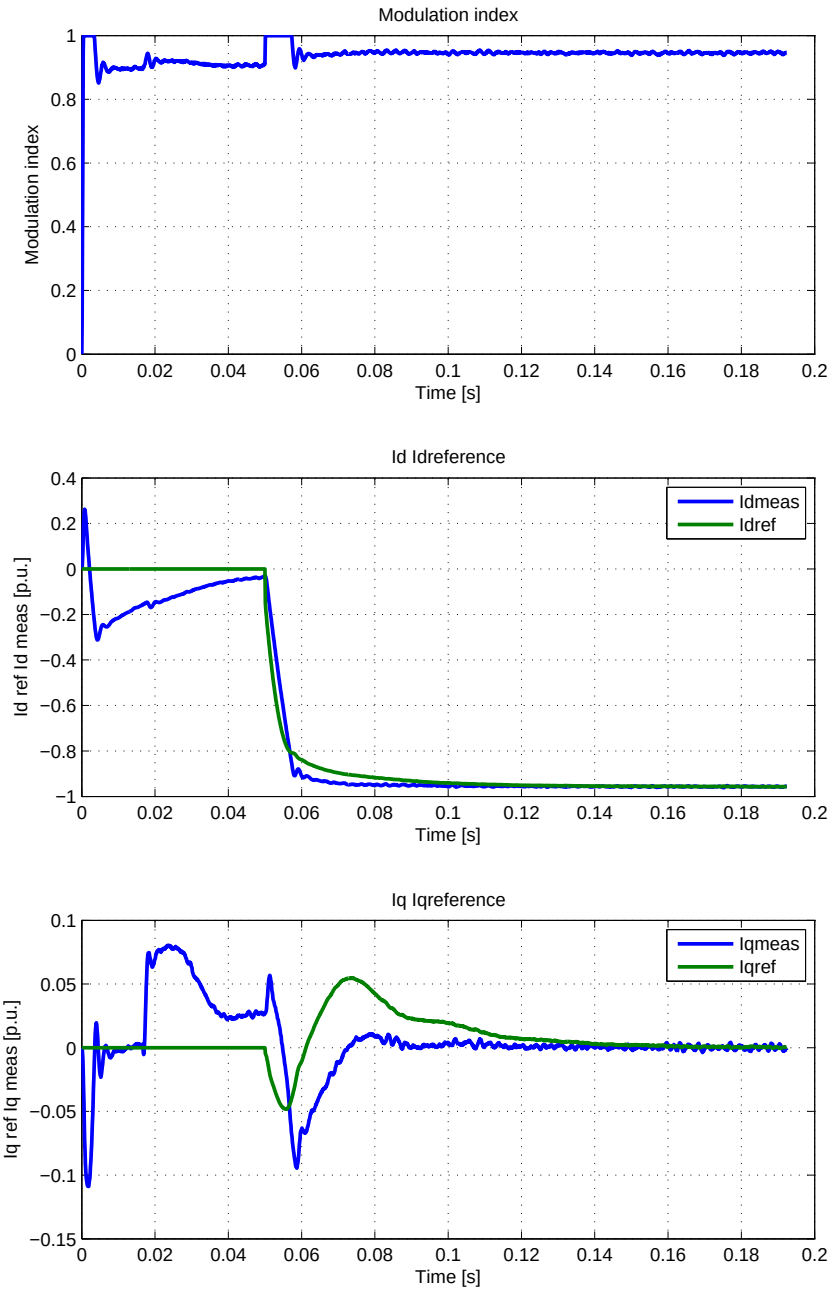


Figure 6.17: Control signals with soft starter.

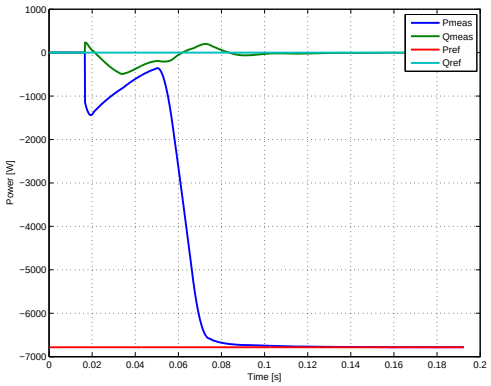


Figure 6.18: Active and reactive powers with soft starter.

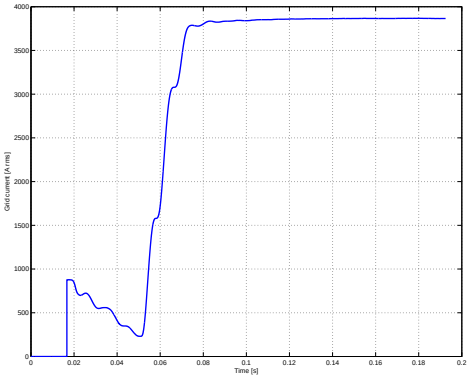


Figure 6.19: RMS grid current with soft starter.

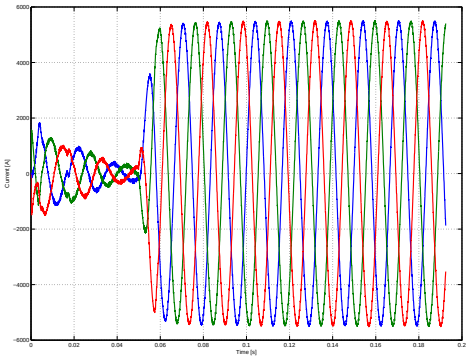


Figure 6.20: Grid current with soft starter.

If the circuit presented in figures 6.11 and 6.12 is used with the same parameters, the results shown in figures 6.17,6.18,6.19,6.20 are obtained.
As the plots show the current spike is now deleted using the simple presented technique. The initial transient due to the PLL is visible in $Idreference$ in figure 6.17 and has a limited current amplitude (lower than the maximum), therefore the previous hypothesis is verified. Figure 6.20 shows the current waveforms using the soft starter technique.

6.5 Dynamic current limiting

6.5.1 Fault operation

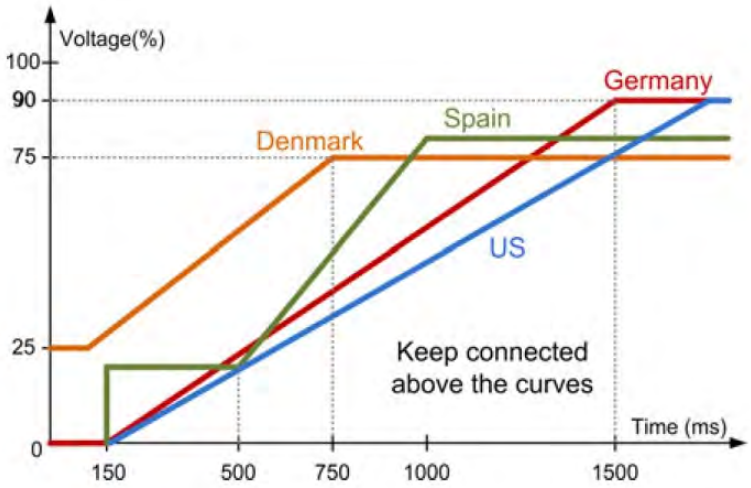


Figure 6.21: Grid codes of wind turbine under grid voltage dip in different countries [18].

Because of the control structure adopted with two external power loops that produce the current reference values, some considerations are worth to be made about faults and generally on voltage dips that can occur in the grid. According to [18] since the power electronics is getting so widely used and renewable power plants have a size that increases year after year, the failure or shot-down of these DC-AC converters may result in serious problems. Therefore the power converters should be reliable to withstand some grid-failure or disturbances. In figure 6.21 for example the grid codes adopted for high power wind power plants are shown. Since the sudden disconnection of power converters may cause issues to the grid (even blackout in the worst case) the converters should be able to remain attached to the grid in order to avoid problems concerning the grid stability. As shown in figure 6.21, the requirements are strict and the converters should be able to work in fault operation for a long time [18].
Obviously the key issue during a fault operation of a converter is to guarantee the protec-

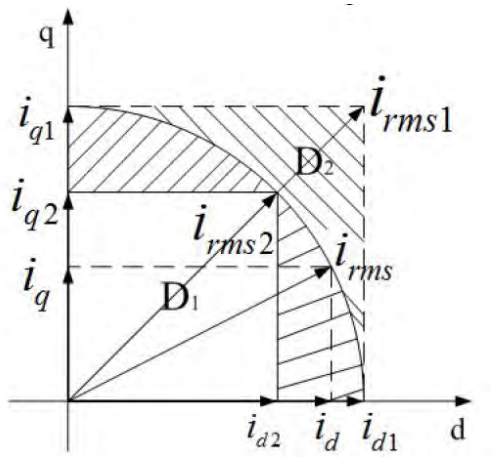


Figure 6.22: $Id1$ and $Iq1$ satisfy the limit current condition but $Irms1$ exceed this limit [26].

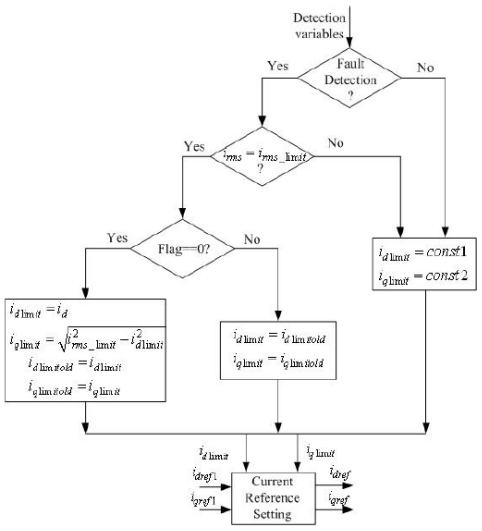


Figure 6.23: Dynamic current limiting blocks diagram proposed in [26].

tion of the converter itself. With the control structure adopted if a three-phase fault or a voltage dip occurs, if the look-up tables are two-dimensional (input Pm and Pt without V_{grid}) the power loops are not able to see the equivalent impedance change or the grid voltage dip and the power reference will remain the same. Since the impedance during a fault is lower than the normal operation one, the power reference can be reached with a current increasing. The solution would be a simple saturation block of the Id and Iq reference values to $1p.u.$, but in this hypothesis if the inverter is injecting both active and reactive currents the limit will be reached satisfying the single condition on Id and Iq, as shown in figure 6.22. As well explained in [26], this problem can be solved using a dynamic current limiting control.

In figure 6.23 the solution adopted in [26] is shown. In the normal operation the current limits are $Id = 1$ and $Iq = 1$. When a fault is detected on the grid (voltage dip, three-phase short circuit or other disturbances) a script is run. If the total current $Irms$ is bigger than the limit, the instantaneous Id value is memorized and $Iq = \sqrt{Ilim^2 - Id^2}$. These two parameters are set as new saturation limits and they will remain unchanged till the fault is removed. When the disturb action ends, the initial limits are restored. In this way if the converter was injecting the current Id and the reactive current Iq to give voltage assist to the grid before the fault, after the fault the values of Id and Iq will remain unchanged (if the transient is neglected), while the powers will change according to the impedance change (or voltage dip).

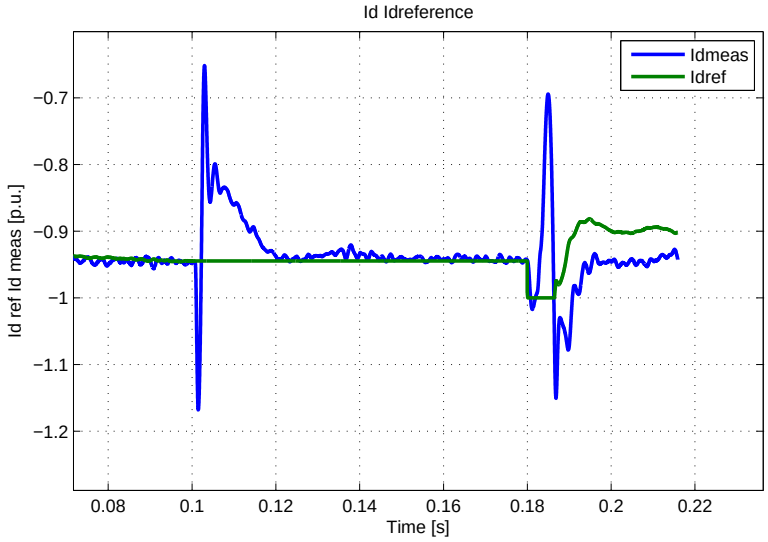


Figure 6.24: Dynamic limiter operation without delay.

6.5.2 Implementation and results

In figure 6.25 the scheme used in the Simulink ® model is presented: the list of checks that have to be verified is executed inside a *Matlab function* and the saturation limits *Idlim* and *Iqlim* are applied to dynamic saturators. Because of the *Matlab function* concept, the data storage is implemented with a feedback between the new and old values; an unit delay block must be added in order to avoid the direct algebraic loop. When the fault is detected if the current loops saturate the power loop integral part grows rapidly and when the fault is removed the current reference goes to -1, affecting the operation during the transient. The reference current remains -1 till the integral value is reset, showing a wind-up behaviour. To avoid the integration during the fault condition, the soft-starter block is activated and the current PIs keep a constant power input. A *Transport delay* block is introduced in order to keep the current limit when the power regulators start their operation again. The operation without the delay is depicted in figure 6.24: when the fault is removed the reference current saturates.

The simulations have been run with different combinations of parameters in order to understand the response of the system in different conditions. The used impedances are the same reported in table 4.1. The total impedance of the circuit is:

$$Z = (R_{pu} + j \cdot L_{pu}) \cdot Zb = (0.0315 + j0.2593) \cdot 0.1429 = 0.0373\ \Omega < 83.08^{\circ} \qquad (6.20)$$

A three-phase fault can be modelled with three-resistances wye connected. To obtain a fault condition the short-circuit impedance must be at least comparable or lower than the circuit impedance. The impedance is chosen equal to:

$$Z_{fault} = R_{fault} + j\omega L_{fault} = 0.011 + j\omega 5 \cdot 10^{-6}\ [\Omega] \qquad (6.21)$$

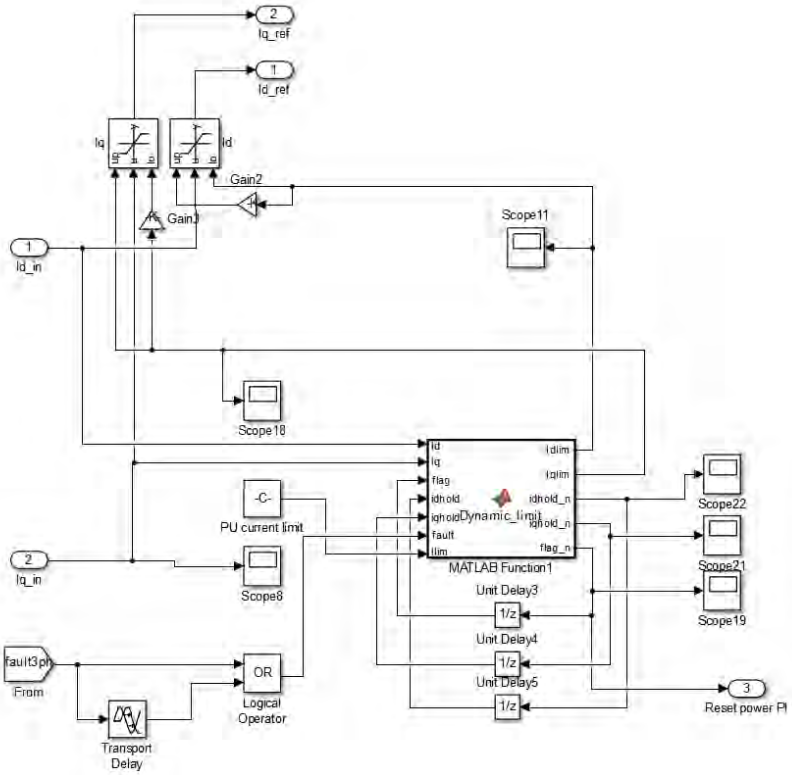


Figure 6.25: Implementation of dynamic current limiting.

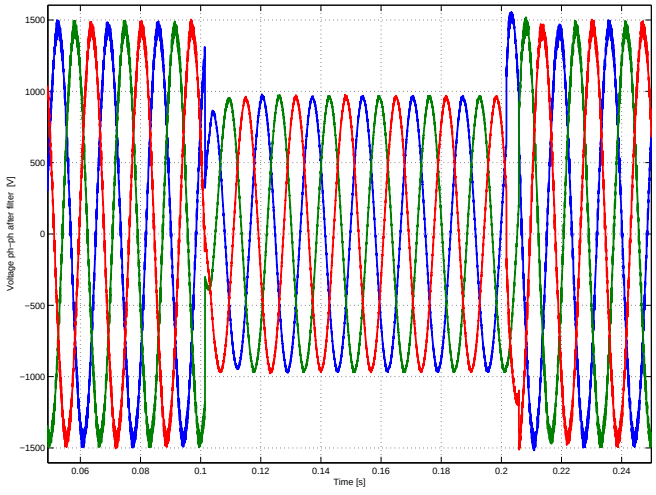


Figure 6.26: Voltage dip considered in the simulation.

The first fault simulation considers the following power production of the DC sources:

$$\begin{cases} Pm = 0.8\ [MW] \\ Pt = 1\ [MW] \end{cases} \tag{6.22}$$

Therefore the total delivered power is:

$$P = 6 \cot Pm + 2 \cdot Pt = 6.8\ [MW] \tag{6.23}$$

The converter is also consider to inject reactive power in order to contribute to the voltage regulation (when the line is not too resistive, otherwise the reactive power injection will affect the line frequency). This reactive power is fixed to be equal to $Q = 0.5[MVar\ ind]$. The considered case is near to the worst condition, because the converter is around his power limit and a voltage dip or an electric fault that may occur would cause a rising of the current above the switches limits.
As presented in figure 6.26, when the three-phase fault is present the voltage has a dip and reaches an amplitude of 62% in comparison with the previous value. The three-phase fault is activated starting from $t = 0.1$ $[sec]$ and removed at $t = 0.2$ $[sec]$.
In the operation without the dynamic current limit, figure 6.27 shows that the Id current loop saturates because the power reference with the new circuit require a current higher than 4 $[kA]$. The reactive power loop after the transient due to the sudden fault still works as the previous condition (without fault). This means that the current is higher than the switches limit, and depending on the temporal length of the voltage dip, the switches may be destroyed.

In figure 6.28 the delivered power is depicted: during the voltage dip the active power is lower, because of the current loop saturation. The transients due to the sudden connection and disconnection are more visible in the reactive power since the resistance is low and therefore the reactive power is related to the voltage. In figure 6.29 the RMS value of the current in the phase a is depicted: nothing can be done to suppress the peaks during the transient condition, but when the circuit is stable during the dip, the current is higher than the limit ($I_lim = 4$ $[kA]$ looking at the grid side).
The same plots are depicted again with the dynamic current limit implemented. In figure 6.30 the RMS current is reduced remaining below the limit (if the transient are not considered). This is obtained because the Id value when the fault is detected is limited at the previous value assumed before the fault.
As shown in figure 6.25 the time delay introduced keep the dynamic limiter in operation even after the fault.

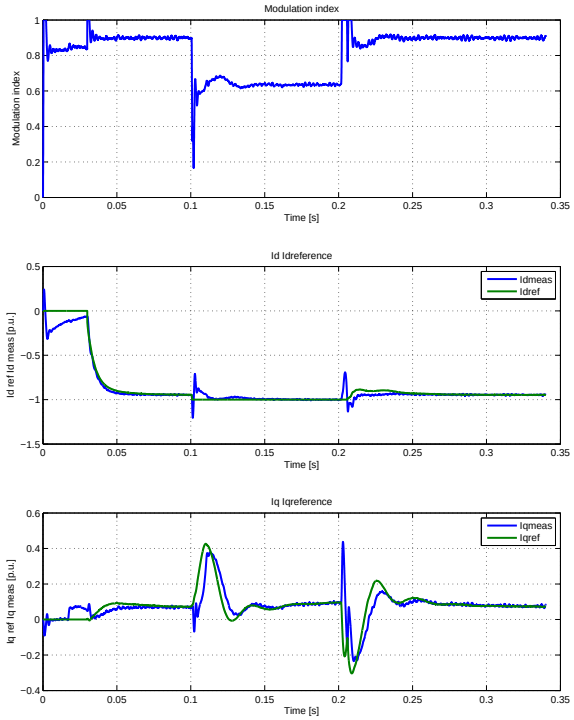


Figure 6.27: Control signals: three-phase modulation index, Id and Iq without dynamic limit.

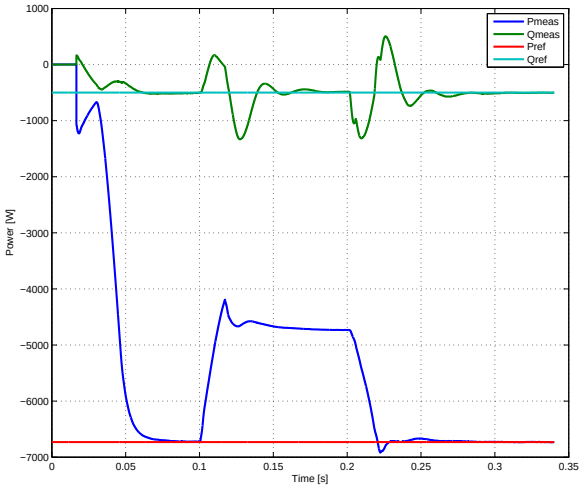


Figure 6.28: Active and reactive power without dynamic limit.

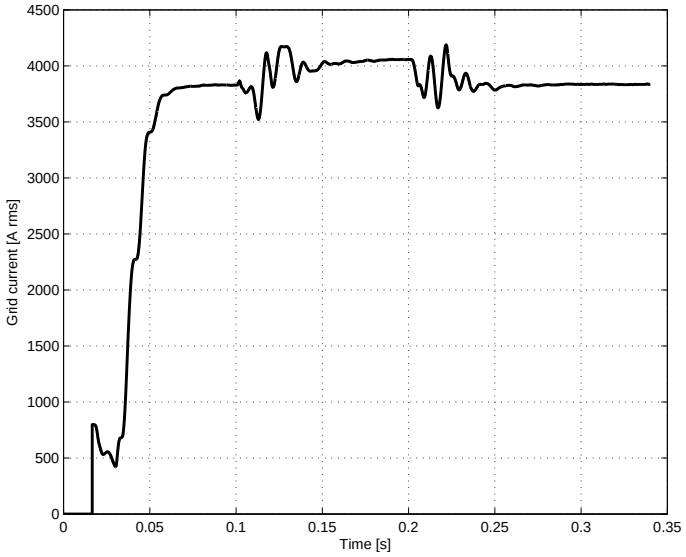


Figure 6.29: RMS current in the phase a without dynamic limit.

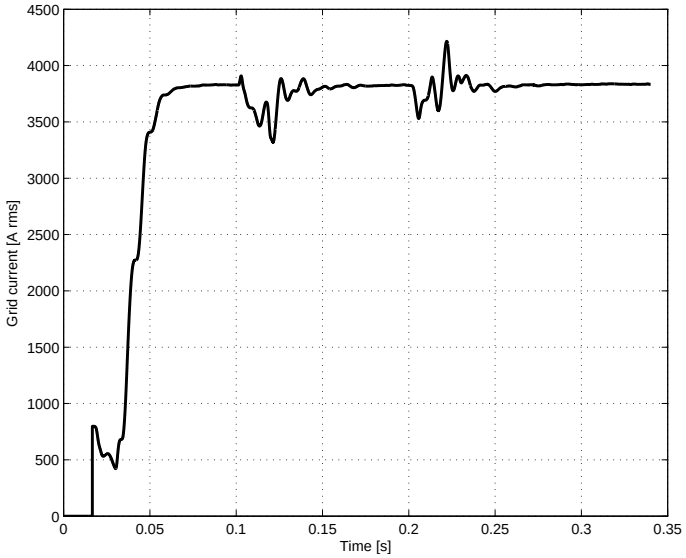


Figure 6.30: RMS current in the phase a with dynamic limit.

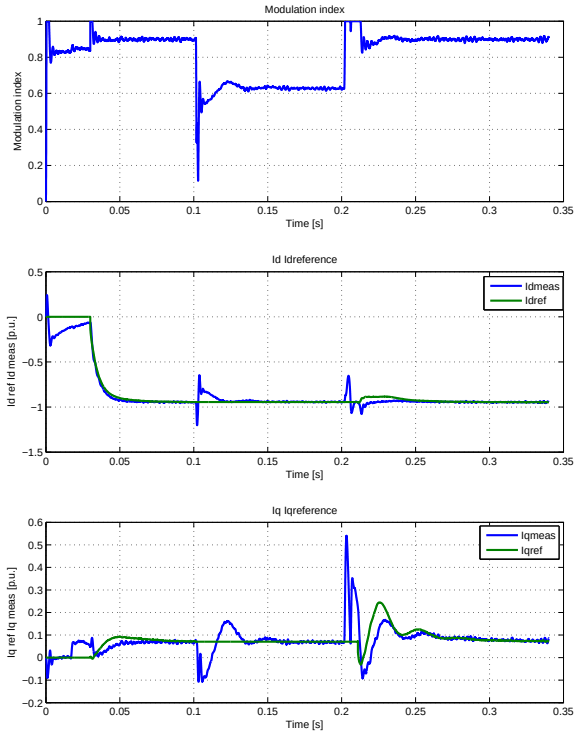


Figure 6.31: Control signals: three-phase modulation index, Id and Iq with dynamic limit.

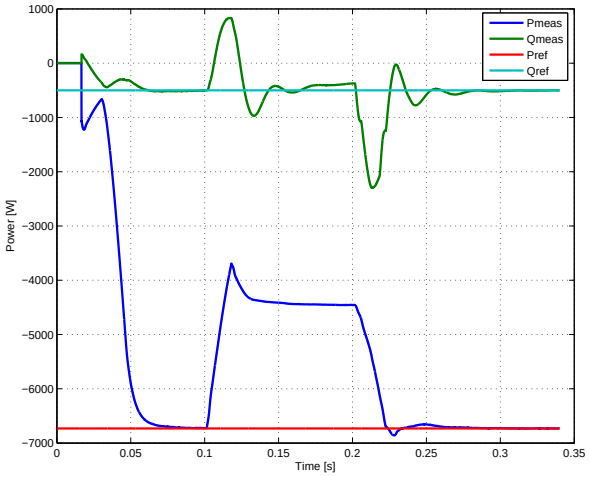


Figure 6.32: Active and reactive power with dynamic limit.

Chapter 7

Interleaving

7.1 Theory

The interleaving principle has already been explained in chapter 2.1.2 in the two-levels converters case. In [6] the analogy between the parallel two-level VSC (voltage source converter) and the FC multilevel topology has been presented, showing that N parallel two-level VSC models are equivalent to $(N + 1)$-level FC converters as far as PWM control and harmonic characteristic are concerned. This is true because of the modularity structure of FC and CHB, as explained in [8]. With the NPC topology the single switch gate signal is defined by the *Level shifted PWM* that is the most used modulation strategy for NPC converters. Since totally four converters for each phase are used (two one-arm single-phase and two one-arm three-phase), the interleaving can be applied between these carrier signals using the analogy principle reported in [6]. The series of converters may be seen as the converters parallel with opposite fundamental applied voltages; in figure 7.1 two parallel arms are shown, but the same scheme would be used to represent one single-phase converter (neglecting the three-phase) if $2 \cdot L$ is the equivalent single-phase inductance.

Firstly the operation without interleaving will be presented in chapter 7.2 and then interleaving will be applied in chapter 7.3.

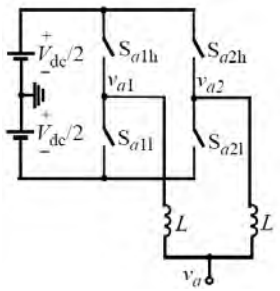


Figure 7.1: Parallel of 2-levels converter [6].

7.2 Without interleaving

In this section the simulation results without applying interleaving are shown. All the carrier are in phase for three-phase and single-phase converters. In fact keeping the carriers in phase in this topology is like to apply interleaving between half single-phase converters and between the three-phase converters. This fact can be seen looking at the phasor diagram reported in figure 7.2. The two half single-phase converters and the two three-phase converters apply phasor in phase opposition and therefore the first harmonic band is centred at $2 * f_{sw}$ because the first band is deleted.
The idea of using the same carriers for all the converters is desirable because to produce shifted carrier signals synchronization and computations are required as explained in [25]. Anyway the best solution is to reach a further reduction applying interleaving also between the single-phase and three-phase converters as it will be discussed in the next chapter.
In figure 7.3 the power block is shown with the measurement blocks that should be used in order to observe the interleaving effect.
Figure 7.4 shows the voltage waveform between the transformer and the RL filter referred to ground. The filtering action is due solely to the transformer and the ZSBTs (with a low contribute). Figure 7.5 shows the FFT analysis with the harmonics that have been depicted. The switching frequency with order 25 does not appear while the first harmonic family is centred around the $50th$. As the waveform with 5 levels shows, all the switches of the inverters are used and the modulation index is near to 1.
In figures 7.6 and 7.7 the voltage waveform and the FFT analysis after the filter are depicted: the harmonic content is the same of figure 7.4 but the amplitude is scaled. In figure 7.8 and 7.9 the current waveform and harmonic spectrum is shown.

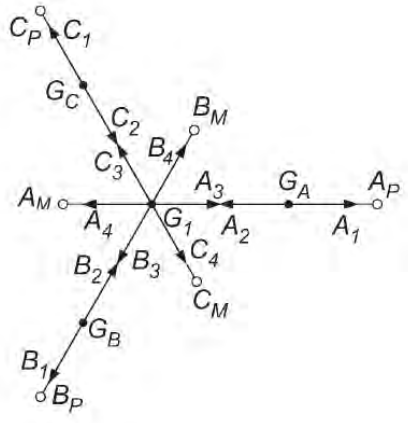


Figure 7.2: Vector diagram proposed in [14].

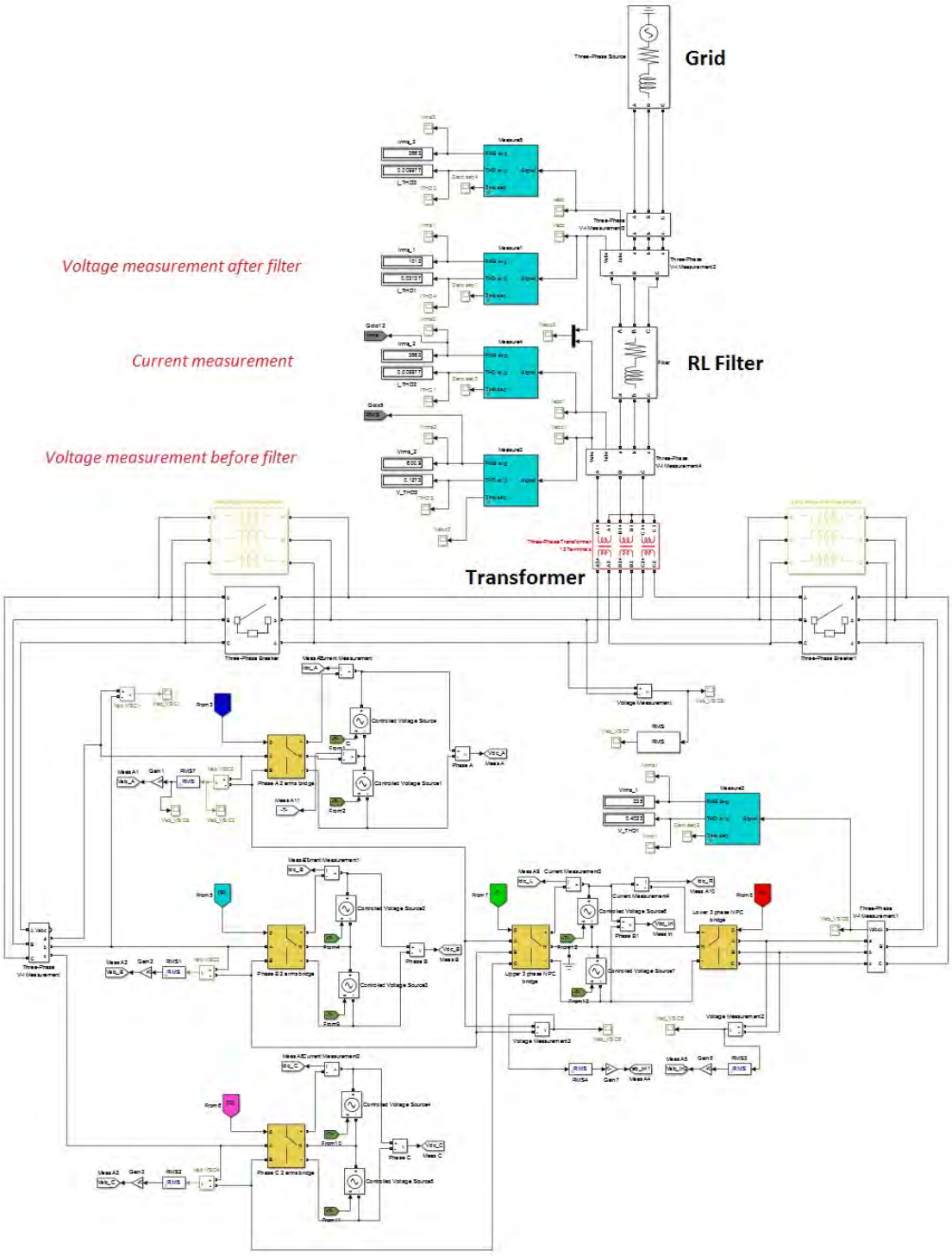


Figure 7.3: Simulink ® model with scopes.

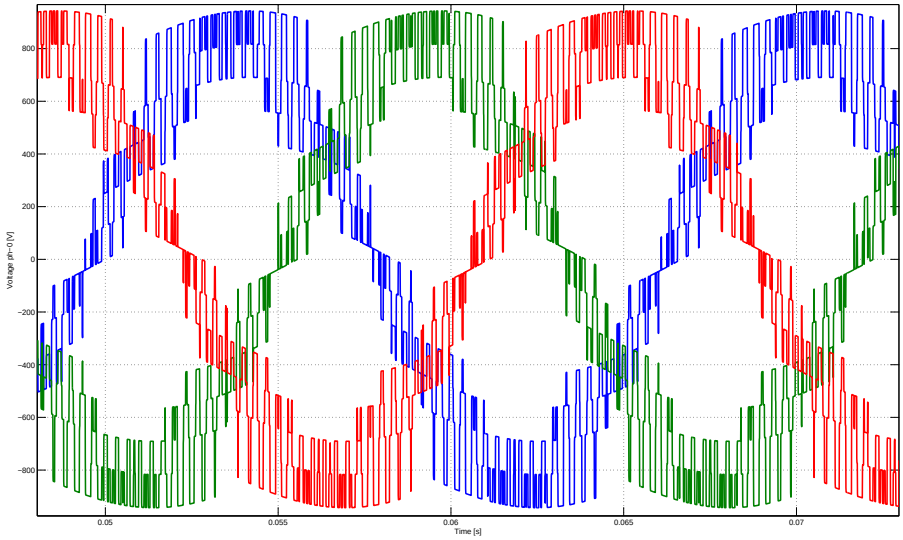


Figure 7.4: Phase to ground voltages before the filter without interleaving; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

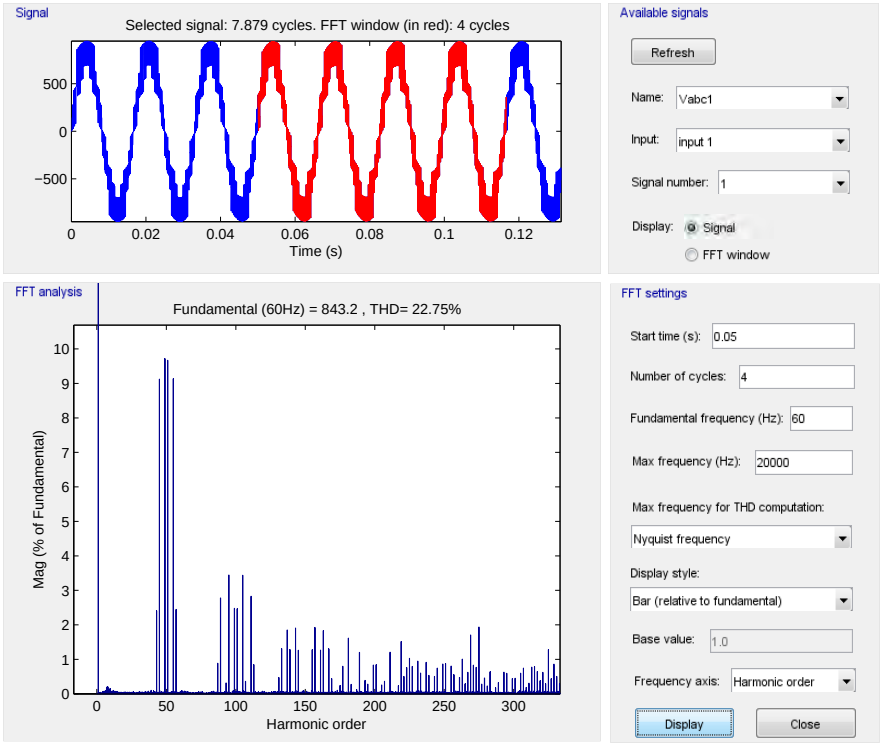


Figure 7.5: FFT of phase to ground voltage; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

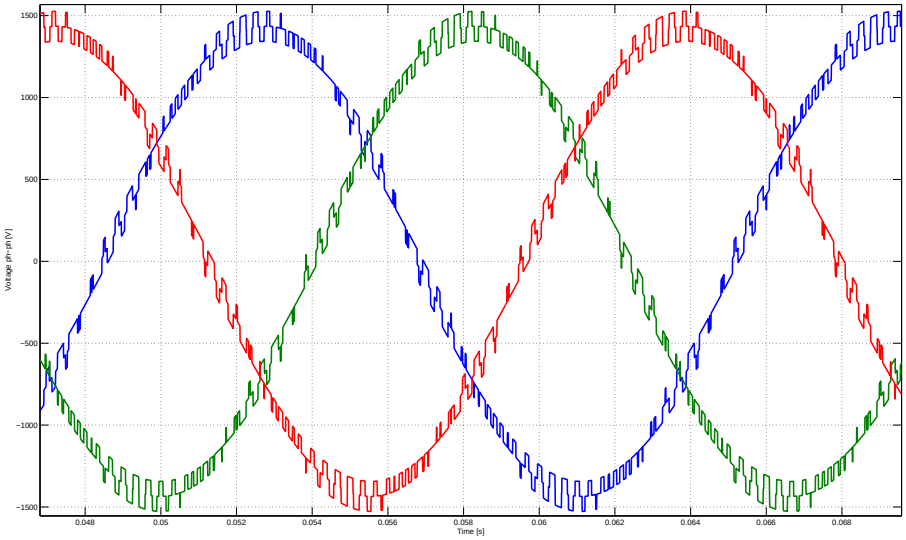


Figure 7.6: Phase to phase voltage after filter without interleaving; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

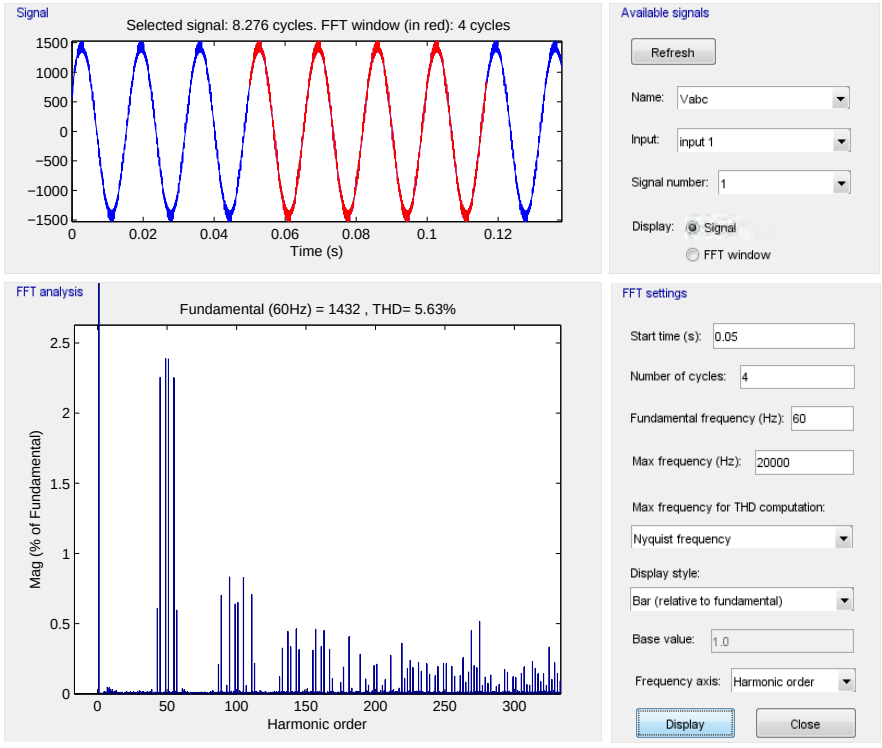


Figure 7.7: FFT of phase to phase voltage after filter; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

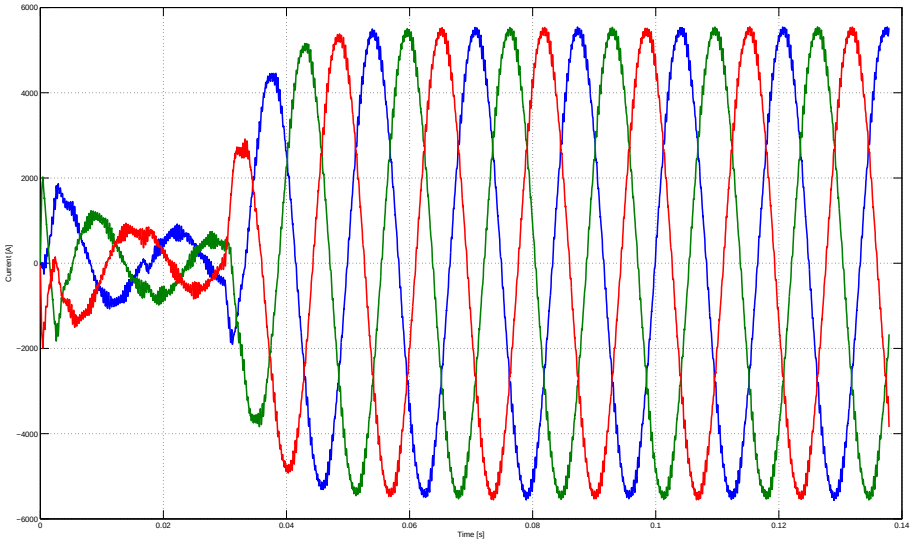


Figure 7.8: Current without interleaving; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

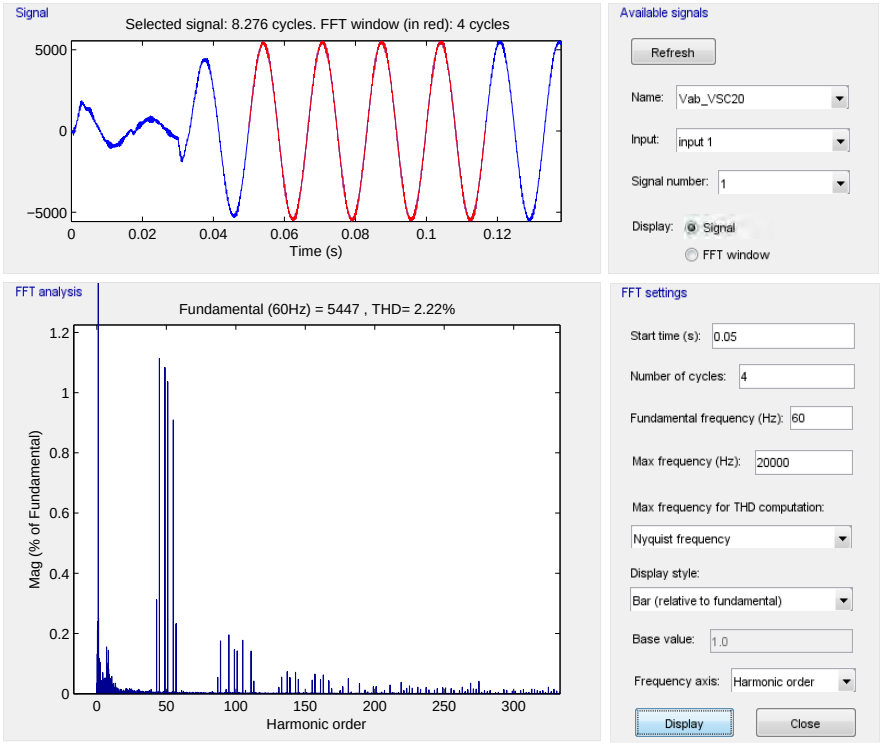


Figure 7.9: FFT of phase current; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

7.3 With interleaving

In this section the carriers of the three-phase converters are phase shifted of 90° referring to the single-phase converters. The comparison with the results obtained for the previous case shows a reduction of the amplitude of the harmonics band centred at $2 * fswitching$ instead of a complete elimination. This is due to the gap between the powers delivered by single-phase converters and three-phase converters. The total power delivered neglecting the losses is:

$$P = 3 \cdot \underbrace{(2 \cdot Et \cdot I \cdot cos\phi)}_{\text{Psingle-phase}} + \underbrace{2 \cdot (3 \cdot Et \cdot I \cdot cos\phi)}_{\text{Pthree-phase}} \tag{7.1}$$

with clear meaning of the symbols. If the power delivered by the converter obey to this law:

$$Pm_{DC} = \frac{1}{3} \cdot Pt_{DC} \tag{7.2}$$

where Pm_{DC} is the power delivered by the single-phase sources in DC side and Pt_{DC} is the one delivered by the three-phase DC source, the voltage applied by each converter is the same because the current is the same. In this condition the bandwidth around $2 \cdot f_{switching}$ is also deleted and the first harmonics appear around $4 \cdot f_{switching}$.
Figures 7.10, 7.12, 7.14 show the voltage before the filter, the voltage after the filter, the current waveforms with the respective FFT analysis. The interleaving improves the waveforms as seen in the comparison with the previous results. As already discussed if the power condition 7.2 is not respected the $2/cdotf_{switching}$ band is not completely deleted, while in figures 7.16, 7.18, 7.20 the first harmonics appear around $4 \cdot f_{switching}$.

7.4 THD vs power

Since the harmonics cancellation depends on the power of three-phase and single-phase generators, with a maximum when $Pt = 3Pm$, an interesting factor to evaluate is the THD variation changing the ratio between powers delivered by each converter. In figure 7.22 Pt is kept constant equal to 1 $[MW]$ while the single-phase power is changed in a range $[0 : 0.9]MW$. The minimum point is reached when the power condition is satisfied and the THD functions grow in a steeper way on the left side of this minimum than the right side.

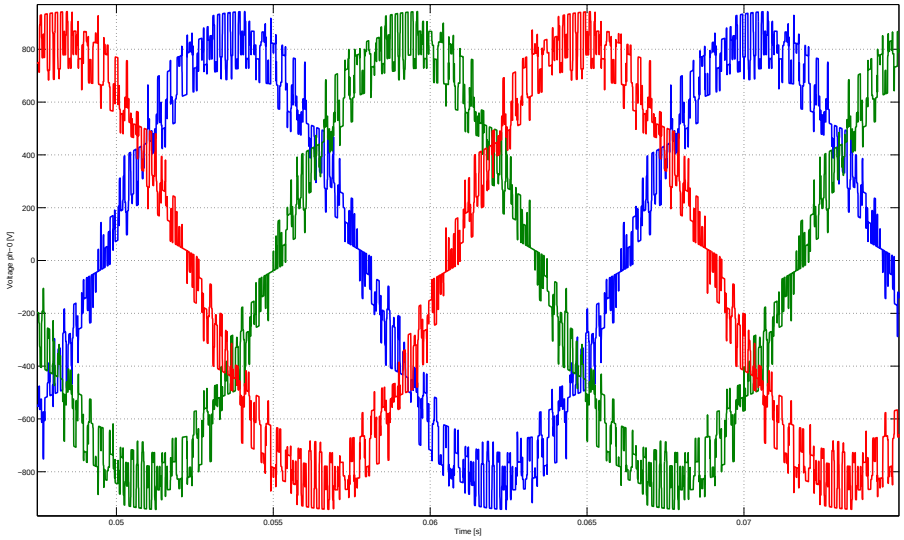


Figure 7.10: Phase to ground voltages before the filter with interleaving; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

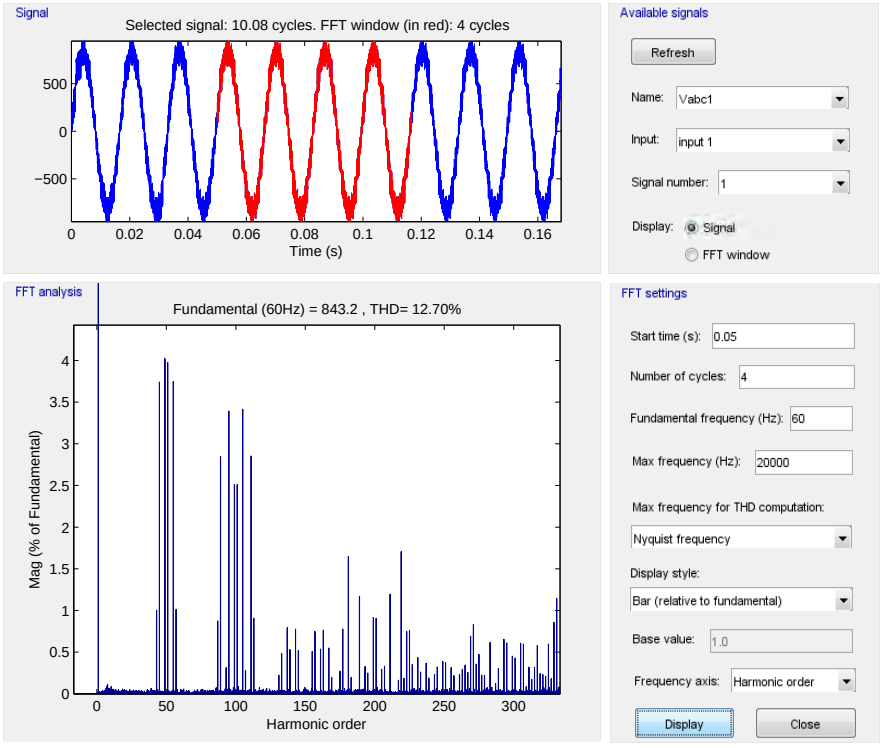


Figure 7.11: FFT of phase to ground voltage; $Pm = 0.8\ [MW]$, $Pt = 1\ [MW]$.

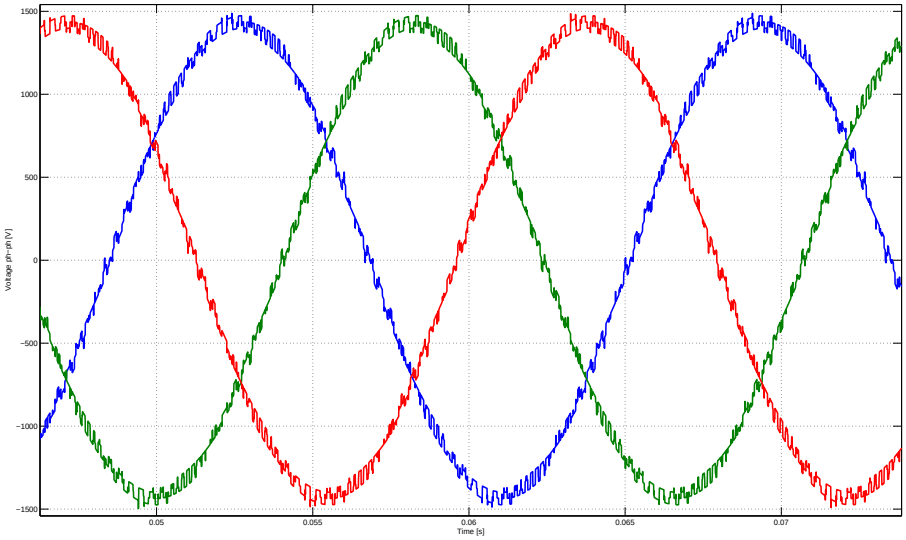


Figure 7.12: Phase to phase voltage after filter with interleaving; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

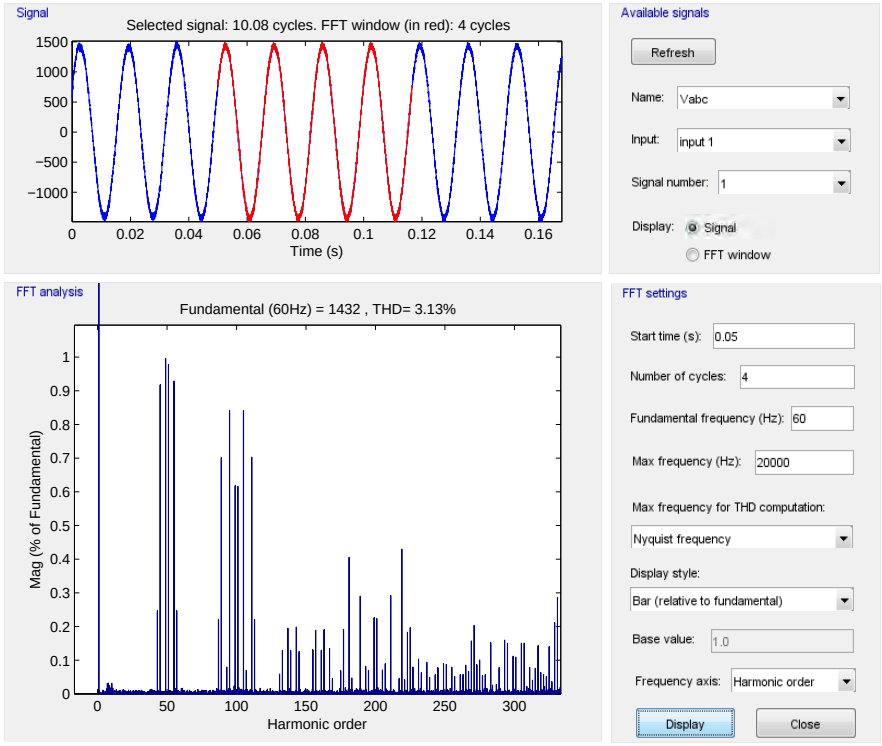


Figure 7.13: FFT of phase to phase voltage after the filter; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

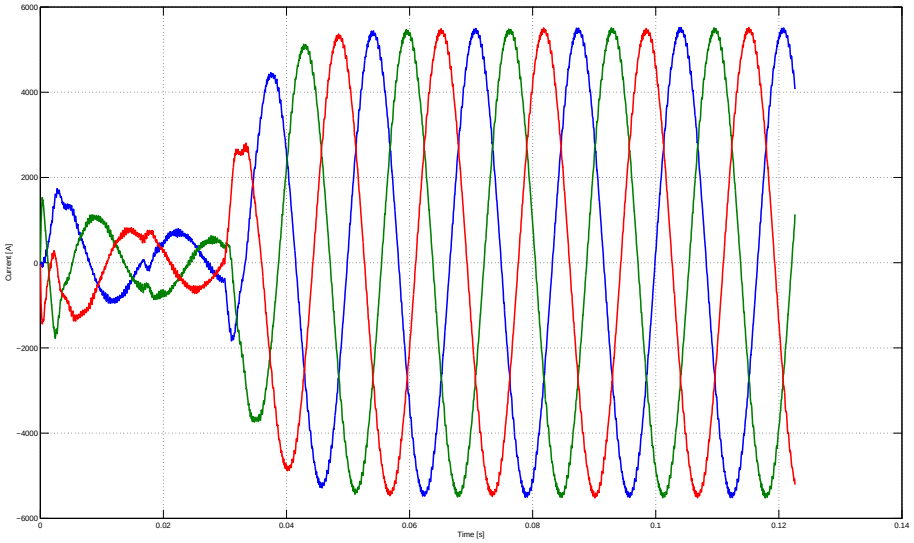


Figure 7.14: Current with interleaving; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

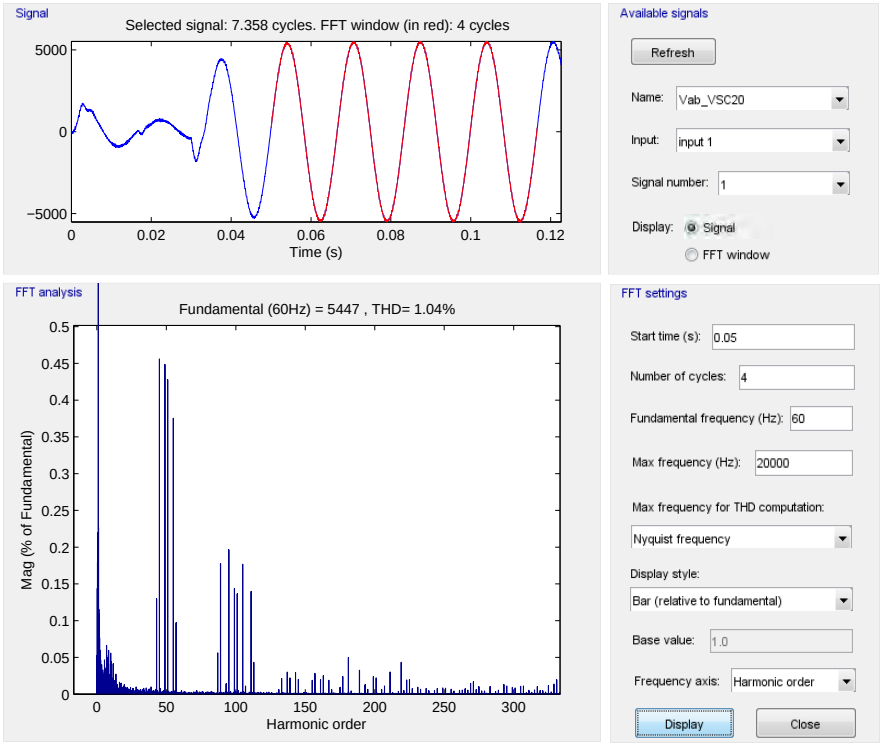


Figure 7.15: FFT of the phase current; $Pm = 0.8$ $[MW]$, $Pt = 1$ $[MW]$.

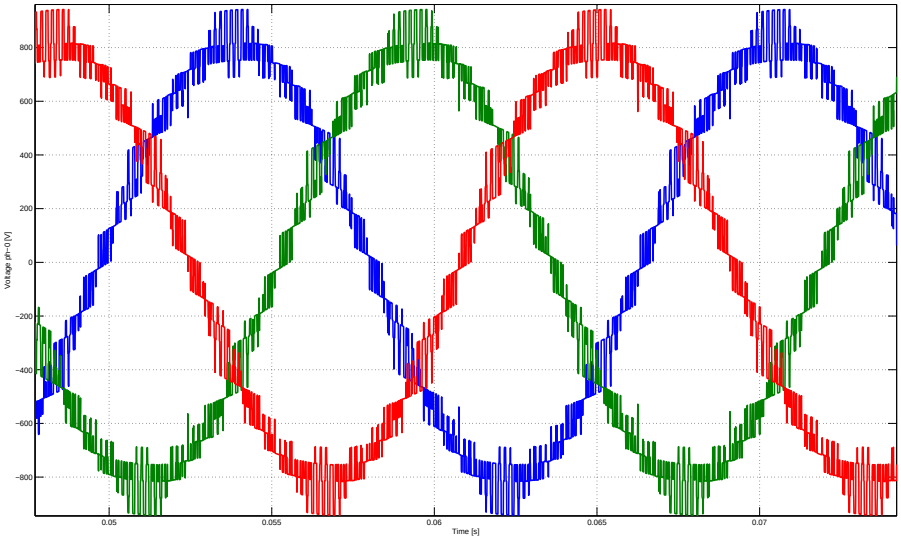


Figure 7.16: Phase to ground voltages before the filter with optimal power condition: $Pm = 0.33$ $[MW]$; $Pt = 1$ $[MW]$.

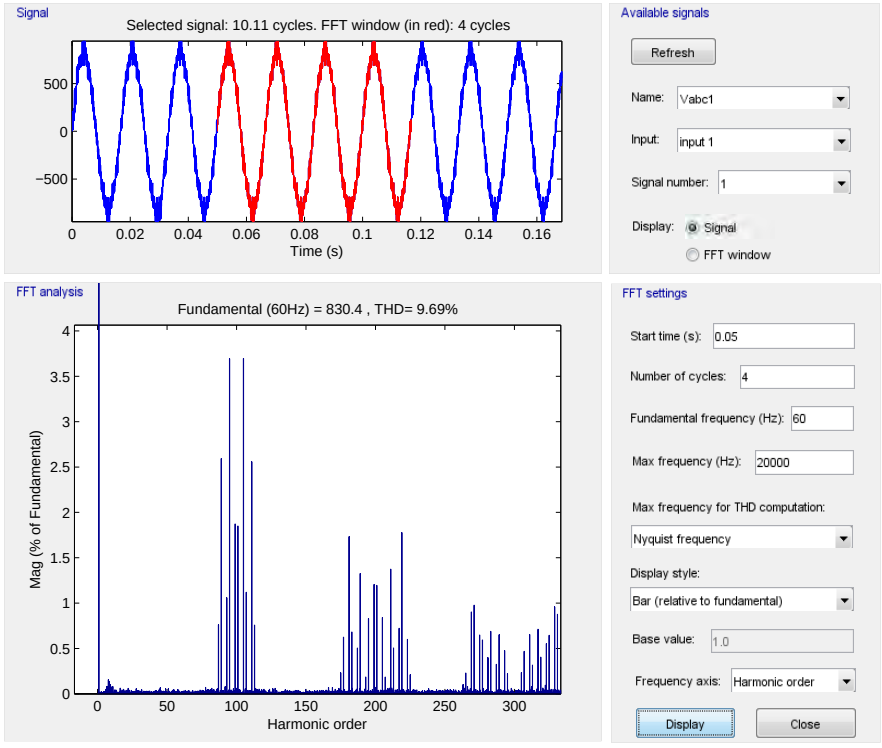


Figure 7.17: FFT of the phase to ground voltage with optimal power condition: $Pm = 0.33$ $[MW]$; $Pt = 1$ $[MW]$.

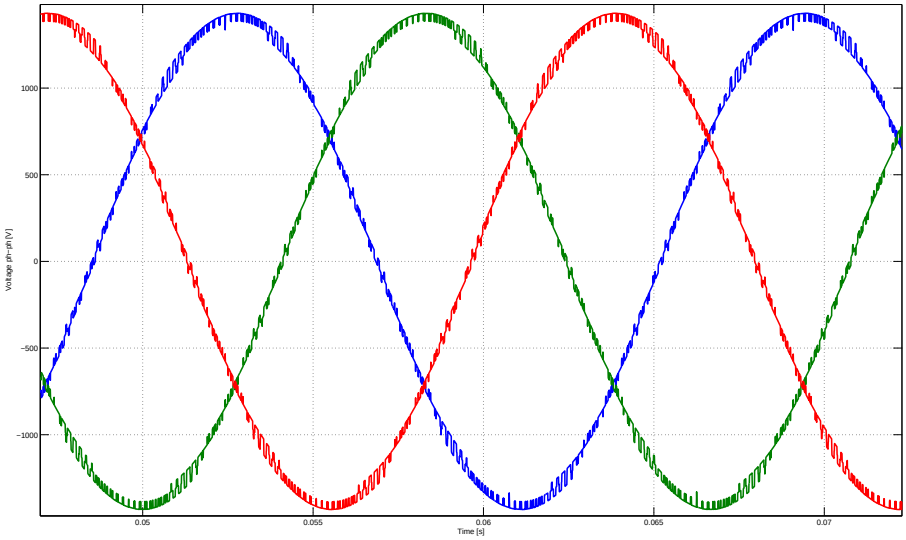


Figure 7.18: Phase to phase voltage after filter with optimal power condition: $Pm = 0.33\ [MW]$; $Pt = 1\ [MW]$.

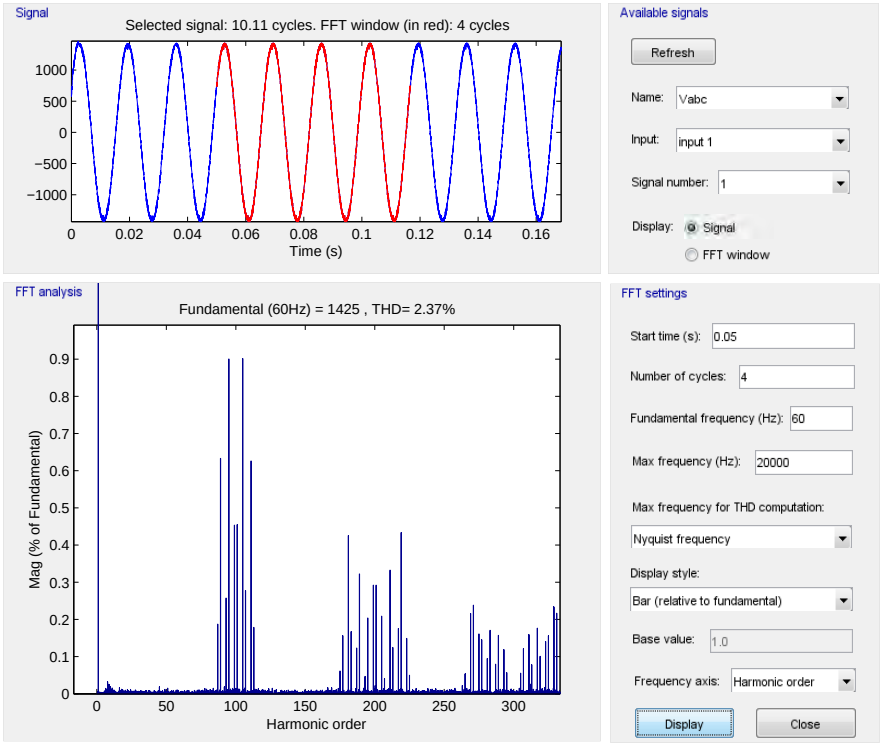


Figure 7.19: FFT of the phase to phase voltage after the filter with optimal power condition: $Pm = 0.33\ [MW]$; $Pt = 1\ [MW]$.

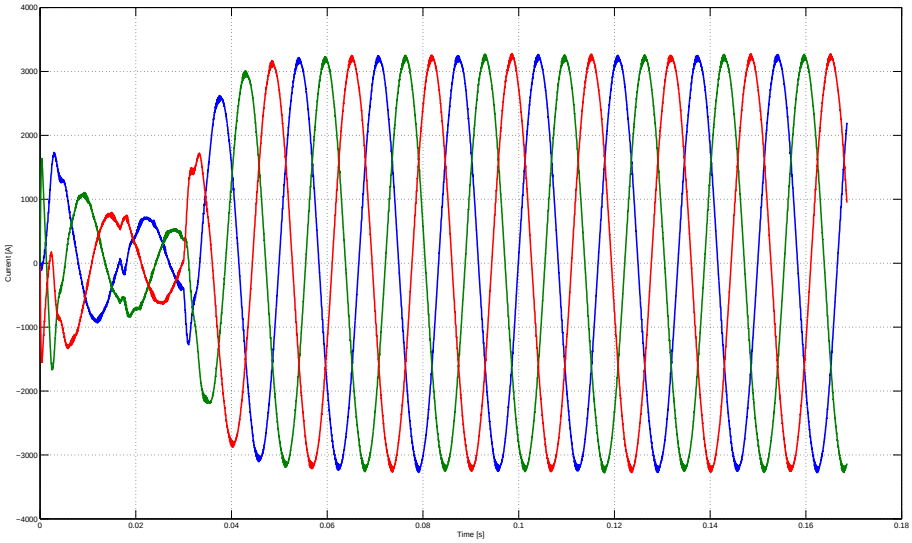


Figure 7.20: Current without interleaving with optimal power condition: $Pm = 0.33\ [MW]$; $Pt = 1\ [MW]$.

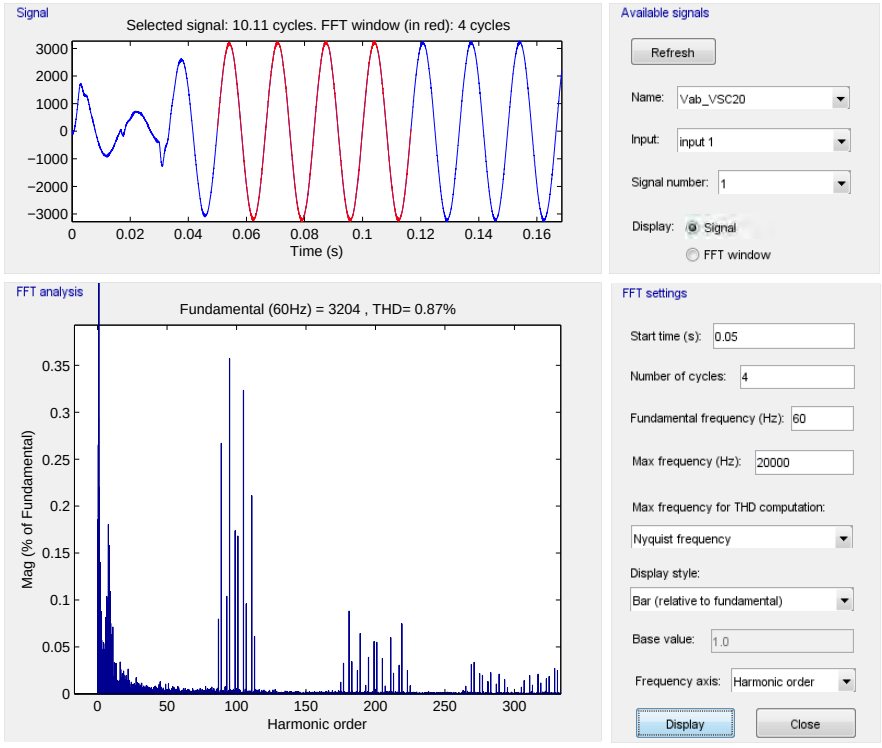


Figure 7.21: FFT of phase current with optimal power condition: $Pm = 0.33\ [MW]$; $Pt = 1\ [MW]$.

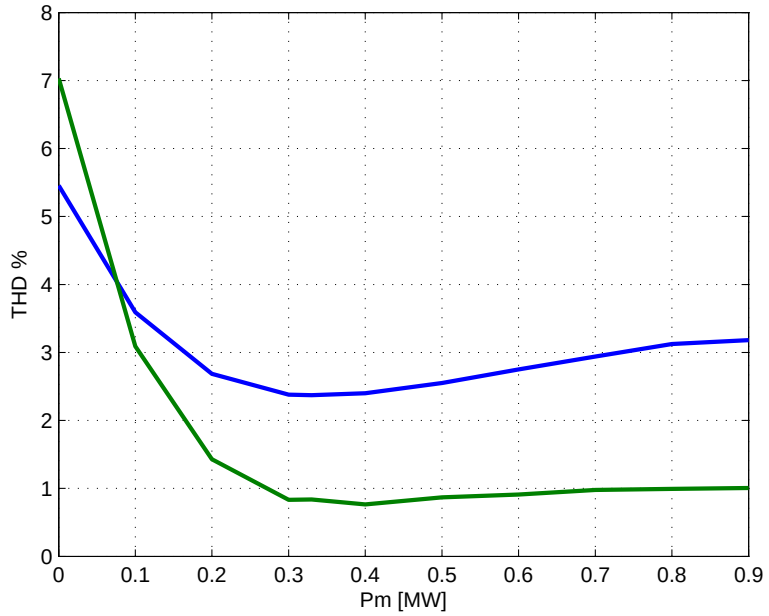


Figure 7.22: THD percentual for voltage measured after the filter (blue) and the current (green) with $Pt = 1$ $[MW]$.

Chapter 8

Sources models

8.1 DC voltage sources

8.1.1 DC voltage reference

In this chapter the simulation results using DC voltage sources are presented. The used circuit is the same of chapter7 here reported in figure 8.2. The use of voltage sources is obviously an idealization of the converter operation because in practise the DC side of each converter has two capacitors to reduce the voltage ripple and the total DC voltage must be controlled. In this thesis an external control has been considered to adjust the power delivered controlling each DC voltage source. The block diagram of a DC voltage controller is shown in 8.1.

The first consideration that is worth to discuss is about the DC voltage impressed by the converters. As explained in 3.2.1, the choice of this maximum voltage affects the operation capability under failure of the converter: the higher the maximum DC voltage is, the more reliable the topology becomes. Since this voltage must be regulated by external controllers that produce an Id reference value as shown in 8.1, a voltage reference value must be given. If the maximum DC voltage is chosen to be the reference for any working condition, the result will be unsatisfactory in terms of THD and voltage stress on the switches. The current in fact is the same for all the converters therefore the power is injected by a single converter adjusting the voltage applied; if the power

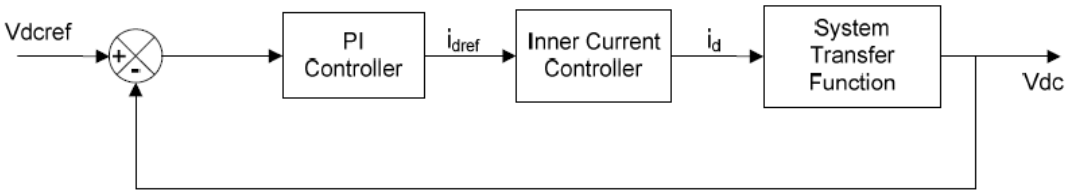


Figure 8.1: Classical scheme used to control the DC capacitor voltage [19].

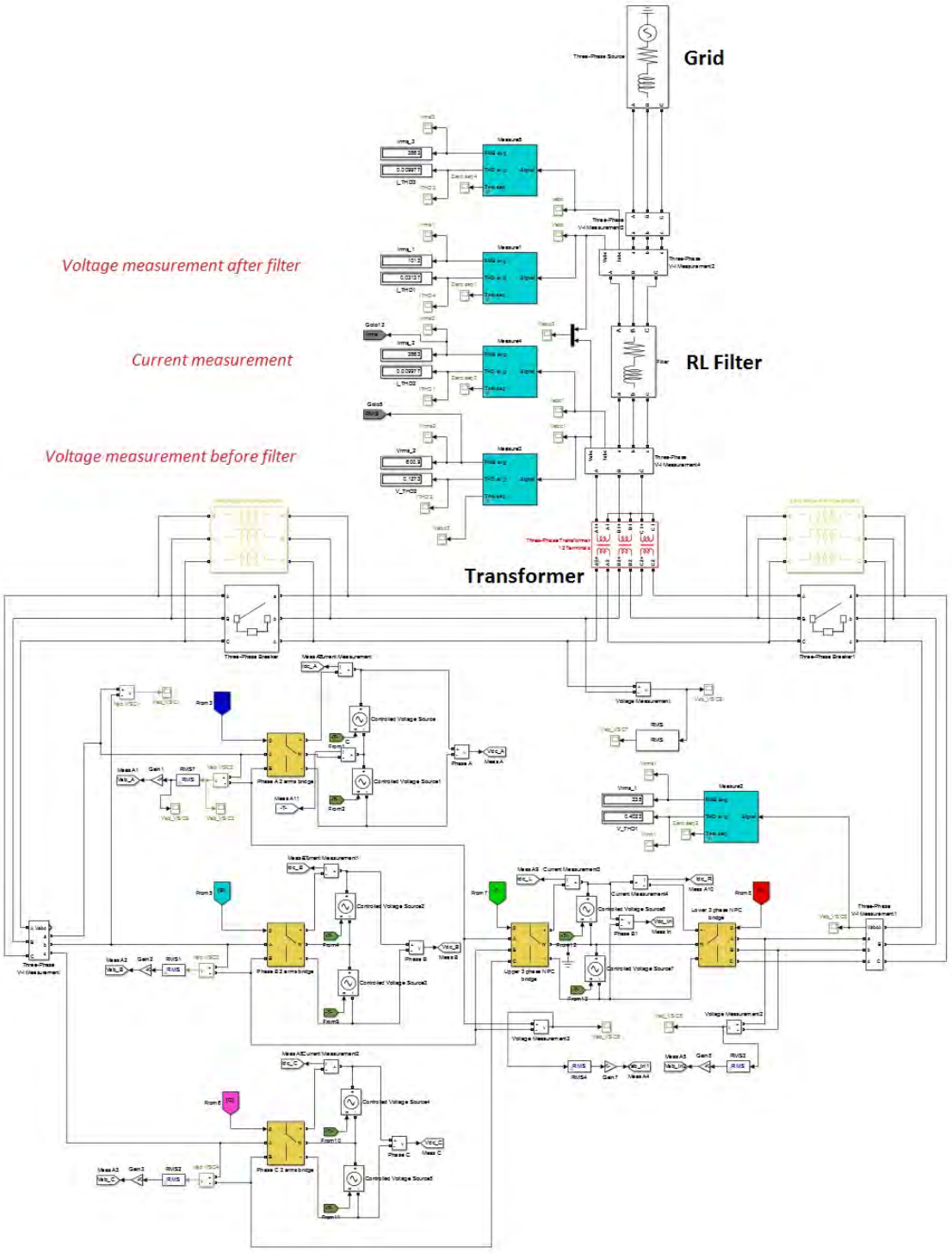


Figure 8.2: Simulink ® model with scopes.

available from a DC source is low, keeping fixed to Vdc_{max} the DC side voltage the modulation index will be low. This means an increasing of the total harmonic distortion with the level shifted PWM technique using two carriers in phase. This is shown in figures 8.3,8.4,8.5, where the chosen modulation index is $m = 0.35$ and the analyzed converter is the single-phase A (the upper in figure 8.2).
In figure 8.3 the used carrier signals are depicted for the adopted control strategy level shifted PWM. The reference voltage signals produced by the internal loops are also represented and they are in phase opposition in order to double the voltage applied by the converter. The result of the comparison between references and carriers is shown in figure 8.4. An important factor to be noticed is that when the result of one comparison is $+1$ or -1, the other signal is always zero. Therefore the difference between these two signals that gives the total phase to phase voltage Vab can assume these values: $[-V_{DC}, 0, +V_{DC}]$. This is effectively the obtained result, shown in figure 8.5. It would be desirable to obtain a five levels output in phase-phase voltages for an NPC three-level converter to maximize the benefits on the waveform.
The obtained results for the overall voltage after the filter are depicted in figures 8.6 and 8.7.
In figures 8.8, 8.9, 8.10 the results with high modulation index $m = 0.9$ are depicted. It is clearly visible that the output has a five-levels waveform, giving an improved result in terms of THD for the voltages after filter, as shown in figures 8.11 and 8.12. The result with an higher modulation index would be even better, but choosing $m \simeq 1$ the control structure becomes weak during transients because the working point is near to the saturation.
In these hypothesis, given an optimal modulation index that should be used, the reference DC voltage value applied by each external controller should be calculated in each power condition. Therefore the DC voltage reference changes according to the power that the source has to deliver. Since the optimization algorithm presented in chapter 5 returns the RMS voltage phasor amplitude that three-phase and single-phase converters should apply, through look-up tables the DC reference value can be computed and stored:

$$V = \frac{m \cdot U_{DC}}{2\sqrt{2}} \tag{8.1}$$

$$U_{DC} = \frac{2\sqrt{2} \cdot V}{m}. \tag{8.2}$$

Anyway a lower limit for the DC voltage must be fixed in order to avoid the voltage reversion that may occur approaching the 0 $[V]$ condition. This limit may be implemented in the optimizer algorithm. If a third harmonic injection system is used, an increase till $+15\%$ may be obtained for V, with a more complex control structure and a better usage of the DC capacitors.

8.1.2 Power and current waveforms

In this section a simple simulation with constant power is run, in order to analyze the DC power waveforms and the current waveforms in the converter side. These parameters

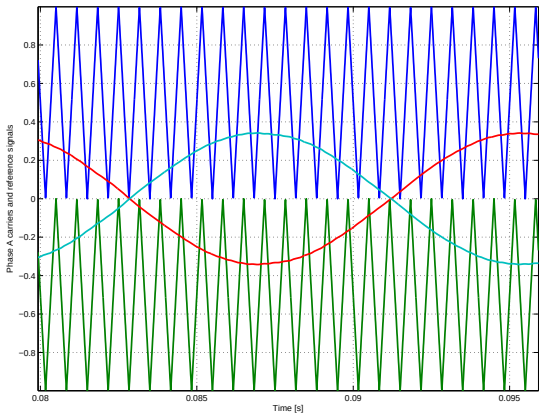


Figure 8.3: LSPWM carriers and reference signals with a low modulation index.

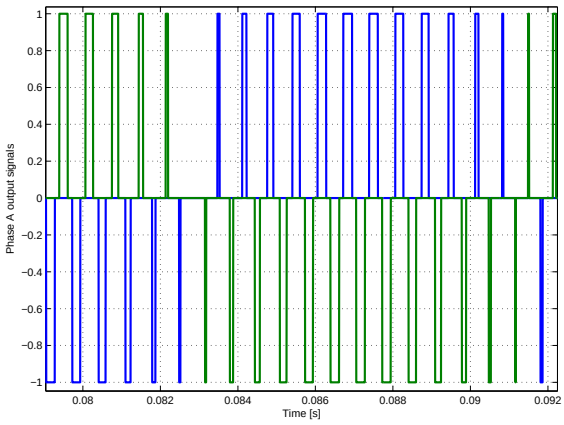


Figure 8.4: LSPWM signals for the upper and lower switches.

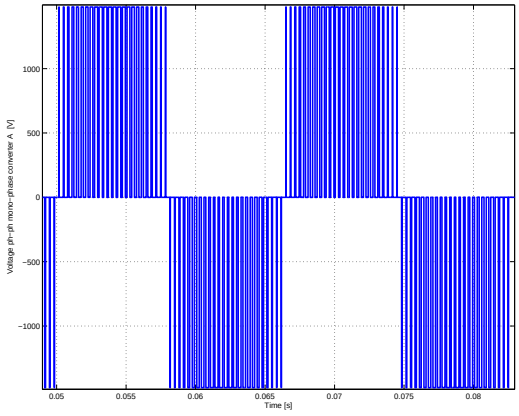


Figure 8.5: Phase to phase voltage waveform with a low modulation index.

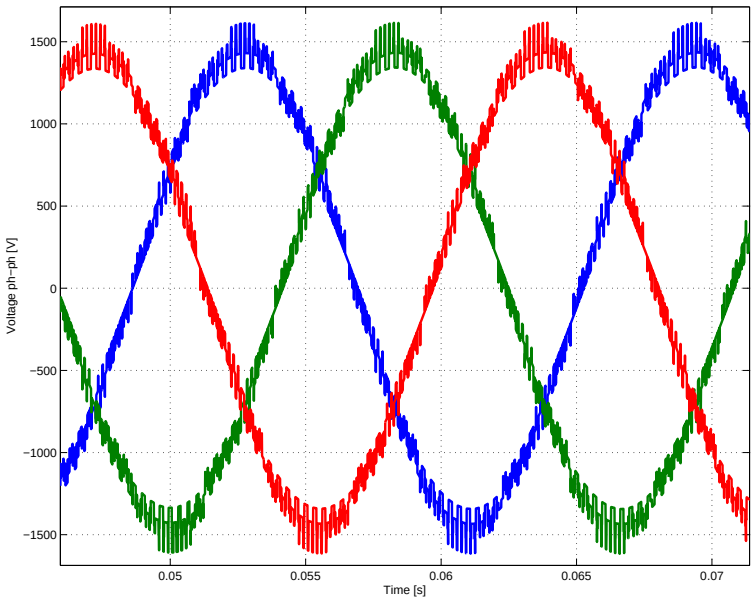


Figure 8.6: Voltages obtained after filter with low modulation index.

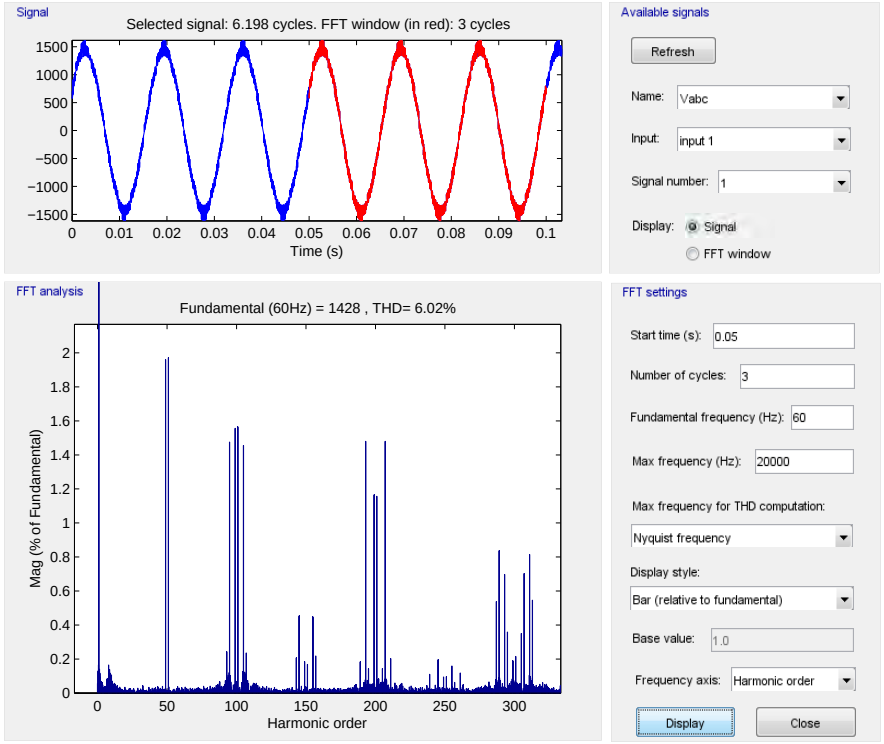


Figure 8.7: Voltege FFT after filter.

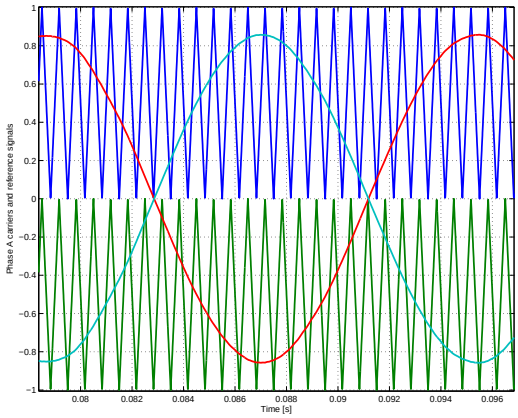


Figure 8.8: LSPWM carriers and reference signals with high modulation index.

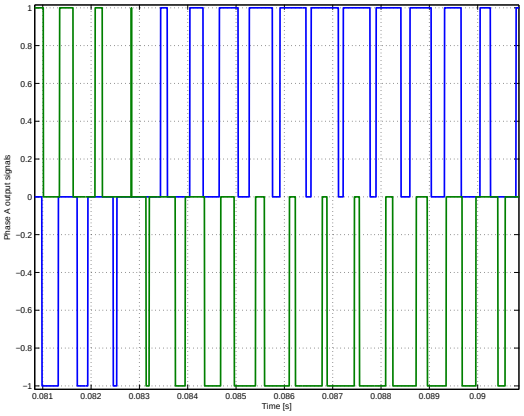


Figure 8.9: LSPWM signals for the upper and lower switches.

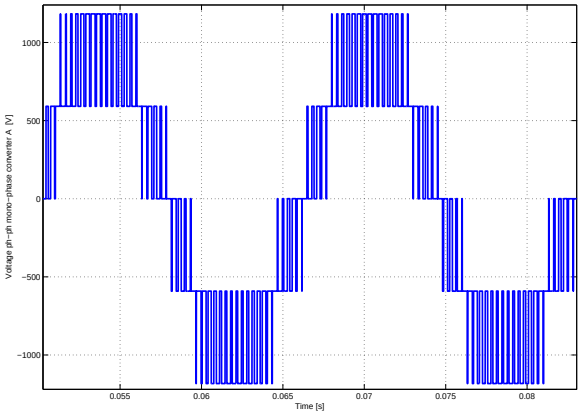


Figure 8.10: Phase to phase voltage waveform with high modulation index.

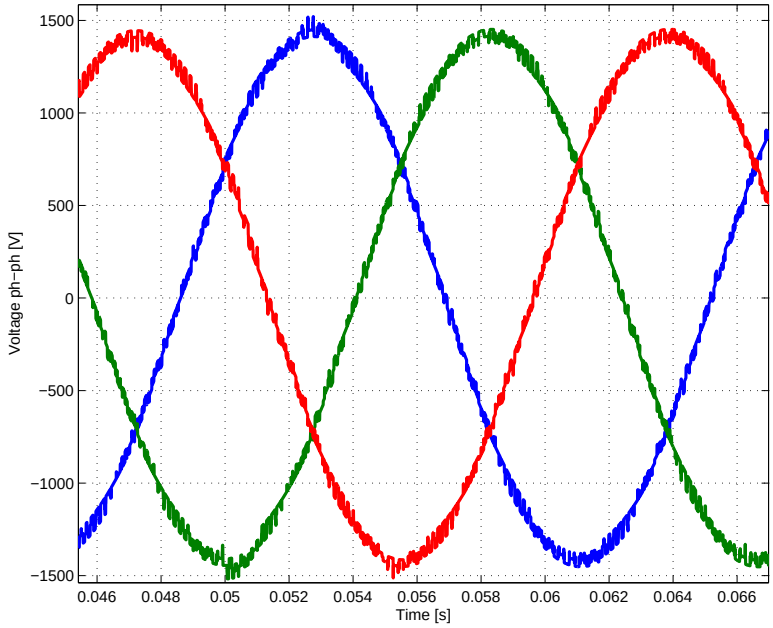


Figure 8.11: Voltages measured after the filter with an high modulation index.

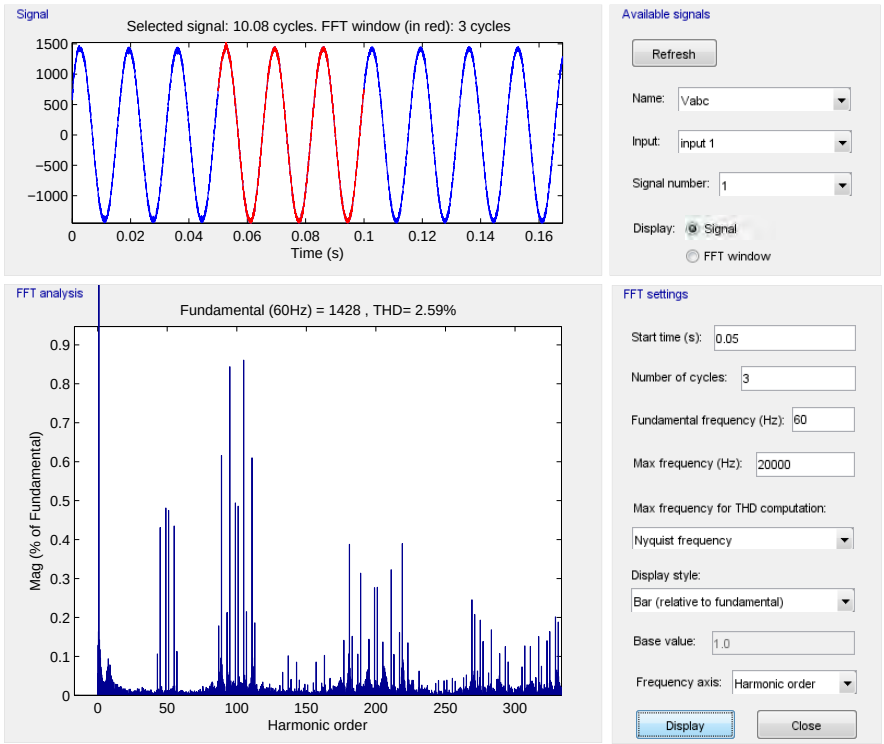


Figure 8.12: Voltege FFT measured after the filter.

have been used:

- $Pm = 0.5$ $[MW]$;
- $Pt = 1$ $[MW]$;
- Interleaving: used;
- $mod.index = 0.85$.

The other parameters are the same used in chapter 4 and chapter 5. In figure 8.23 the power delivered by each DC source is depicted. Remembering the scheme shown in figure 8.2, A is the upper single-phase converter, the converter C is the lower, and the three-phases converters are on the right connected to the same DC source.
According to the analysis presented in chapter 3.1 and considering a sinusoidal phase to neutral voltage V, a sinusoidal current I shifted by ϕ and considering $Ineutral$ negligible, the power in AC side delivered by one leg of the single-phase converter is:

$$P(t) = v(t) \cdot i(t) = \sqrt{2} \cdot V \sin(\omega \cdot t) \cdot \sqrt{2} \cdot I \cdot \sin(\omega \cdot t - \phi) \tag{8.3}$$

The DC side voltage V_{DC} is the voltage impressed by one voltage source and it is kept constant, therefore the current becomes:

$$Id = \frac{V \cdot I}{V_{DC}} \cdot \cos(\phi) - \frac{V \cdot I}{V_{DC}} \cdot \cos(2 \cdot \omega t - \phi) \tag{8.4}$$

The single-phase power spectrum with a constant DC source contains a DC value and a component with frequency $f = 120$ $[Hz]$, twice in comparison with the fundamental. As shown in figure 8.13 in the plots of the DC currents relative to the upper and lower converter, the currents follow exactly the equation 8.4; the upper and lower currents are phase-shifted looking at the switching frequency component because of the neutral current, neglected using equation 8.4. In the FFT analysis the expected voltage is a DC component with the same value of the second order harmonic (considering $\cos\phi \simeq 1$) plus the harmonic bands centred around the multiples of the switching frequency. The result is the same of a single-phase converter that uses an unipolar PWM. The simulations validate this hypothesis as shown in figure 8.14 where the fundamental is $f = 120$ $[Hz]$ and the switching frequency has an order equal to $\frac{25}{2} = 12.5$.
Only a small delay is introduced because of the angle ϕ between currents and voltages. Since in this case the voltage of each source is kept constant, the current waveform is exactly proportional to the power waveform for each half DC source. The total power of the DC source is given by the sum of the two half powers and the shape obtained is shown in figure 8.13. This waveform is obtained because the equation:

$$Id = \frac{V_{ph-ph} \cdot I}{V_{DC}} \cdot \cos(\phi) - \frac{V_{ph-ph} \cdot I}{V_{DC}} \cdot \cos(2 \cdot \omega t - \phi) \tag{8.5}$$

is still valid with V_{ph-ph} that is the RMS voltage output of the converter A considering that the average neutral current adsorbed by the converter is zero. Since V_{ph-ph} is a three-level voltage in half period (five-levels in full period), the global power has three different

"levels" in one power period (half voltage period). The expected FFT analysis should show again a DC component with the same amplitude of the second order harmonic considering $\cos\phi \simeq 1$ and then harmonic bands centred around the multiples of the switching frequency: remembering that the interleaving is applied, looking at the global power the switching should appear doubled. The expected results are verified in figure 8.15 that shows the harmonic content of the DC total power: the fixed fundamental frequency is $f = 120\ [Hz]$ and the first harmonic that appears has an order $25 \cdot 2 = 50$ because of the interleaving.
In figures 8.13 and 8.16 the waveform of the neutral current adsorbed by the single-phase converter A is also depicted. This current is due to the load current inertia when the zero state is applied in one of the two legs of the single-phase converter. This current is the difference between the lower and the upper DC current. Therefore the contributes with the second order harmonic and the DC component are theoretically deleted, while the first frequency visible in the FFT analysis should be the switching frequency. This is in accordance with the obtained results in figure 8.17 where the fundamental $f = 25 \cdot 50$ is considered. The DC value is zero and the first important family of harmonics is centred around the switching frequency.

The same line of reasoning may be developed for the three-phase converters. If only one converter is considered, in the hypothesis of sinusoidal AC voltages and currents and neglecting again the neutral current, the power expression gives according to [27]:

$$P(t) = E_a(t) \cdot I_a(t) + E_b(t) \cdot I_b(t) + E_c(t) \cdot I_c(t) \tag{8.6}$$

$$\begin{aligned} I_{DC} = \frac{2 \cdot E \cdot I}{V_{DC}} \cdot [&\cos\omega t \cos(\omega t - \phi) + \cos(\omega t - 120^\circ)\cos(\omega t - 120^\circ - \phi) \\ &+ \cos(\omega t - 240^\circ)\cos(\omega t - 240^\circ - \phi)] = \frac{3 \cdot E \cdot I \cdot \cos\phi}{V_{DC}} \end{aligned} \tag{8.7}$$

therefore the current should contain only a continuous component plus the harmonic content due to the switching frequency.
In figure 8.18 the simulation results are depicted. The upper and lower DC current is due to both the three-phase converters. As expected according to equation 8.7 these currents do not contain low harmonics of the switching frequency and the first harmonics that appear are centred around the switching frequency, as shown in figure 8.19.
Both the three-phase converters contribute to the neutral current, again obtained as a difference between the lower DC current and the upper DC current. The average is again equal to 0 and the first expected harmonic is the switching frequency, in accordance with figure 8.21.
Finally the total DC power is due to the sum of the upper and lower contributes, directly proportional to the current values; remembering that the interleaving is applied, the expected first harmonic should be two times the switching frequency; this is in accordance with figure 8.20.

Figure 8.22 shows the zero sequence component on the converter side, limited by the action of the zero sequence blocking transformers. In this simulation the transformer has

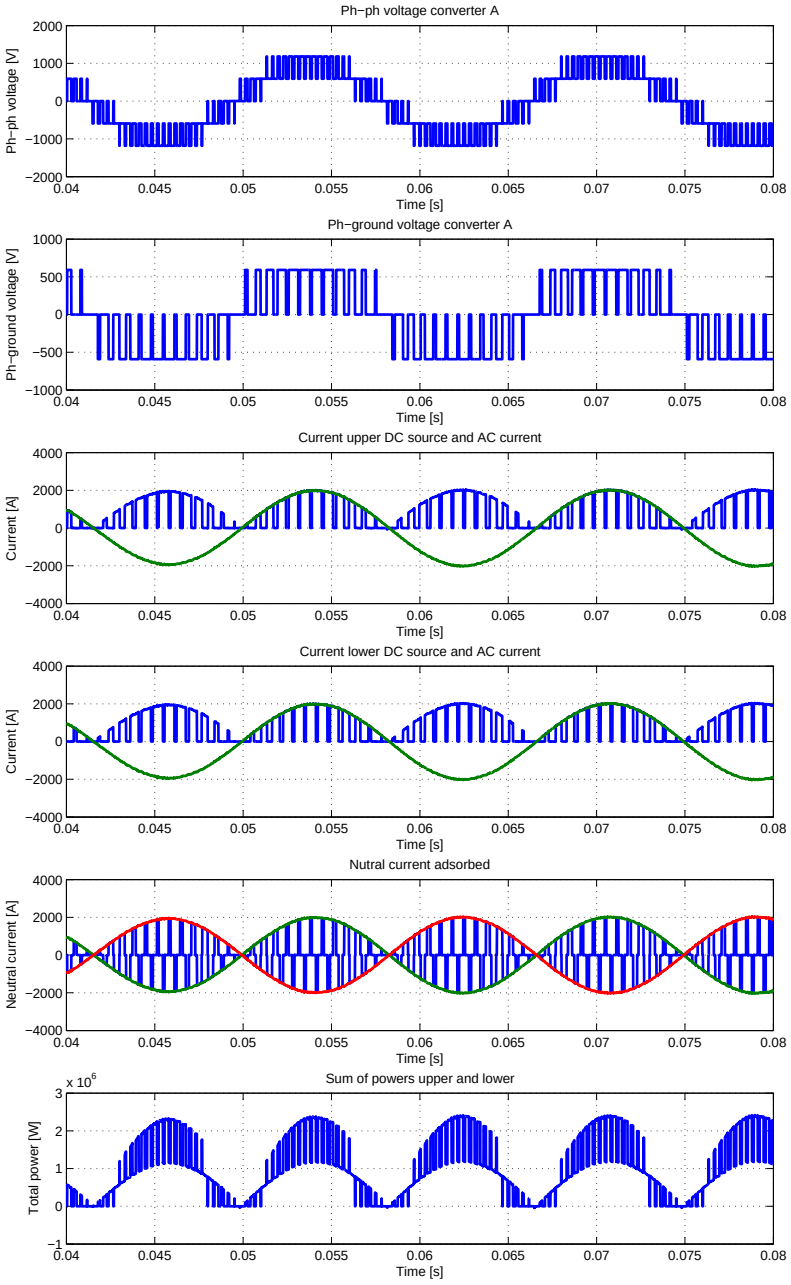


Figure 8.13: Single-phase converter A waveforms.

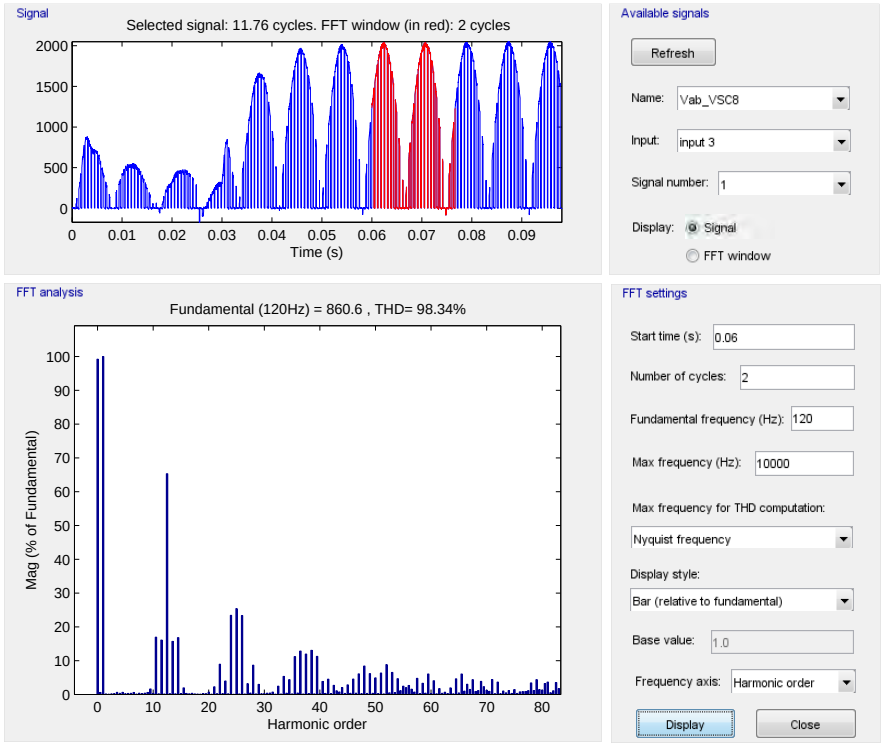


Figure 8.14: FFT analysis of I_{DC}: current in the upper DC source of the converter A.

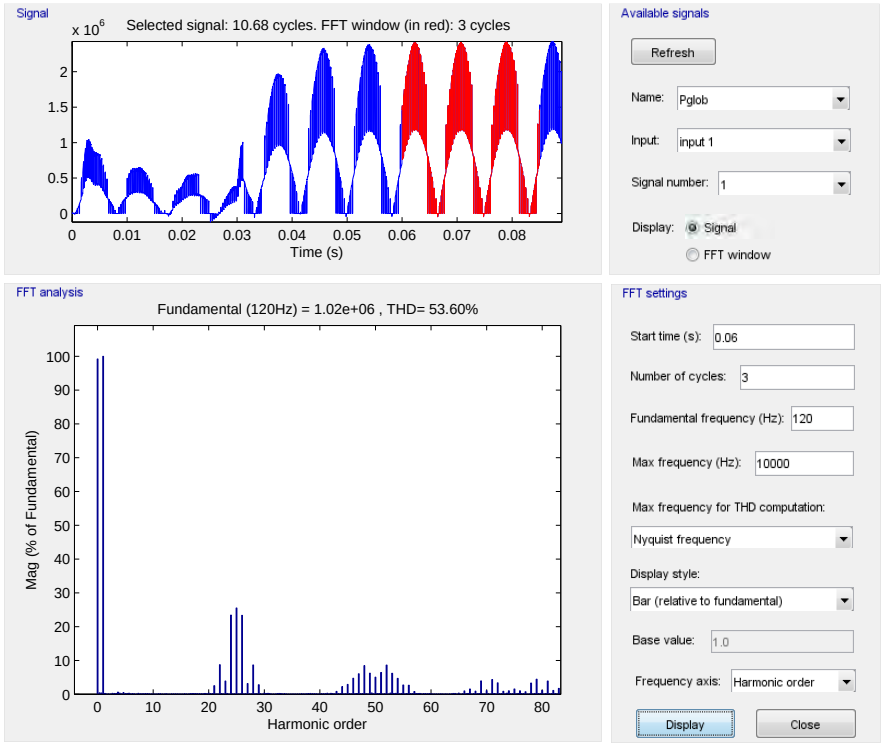


Figure 8.15: FFT analysis of P_{DC}: total DC power of the converter A (sum of upper and lower powers).

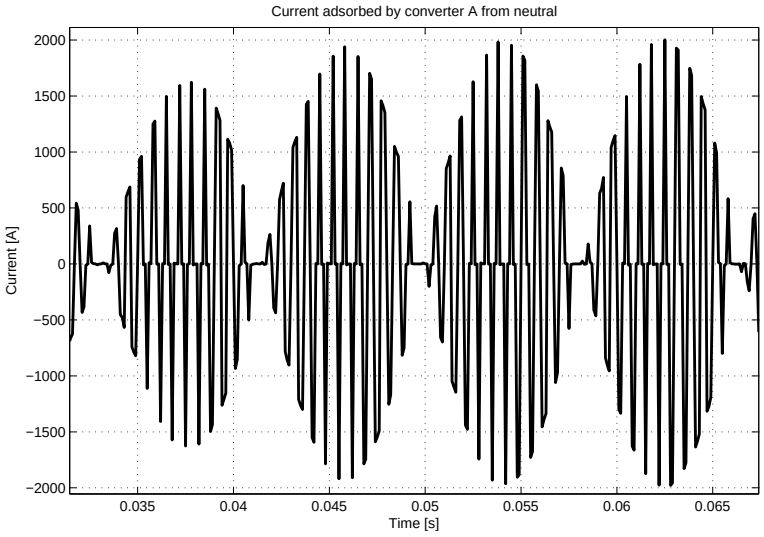


Figure 8.16: Neutral current adsorbed by the converter A (zoom of figure 8.13.

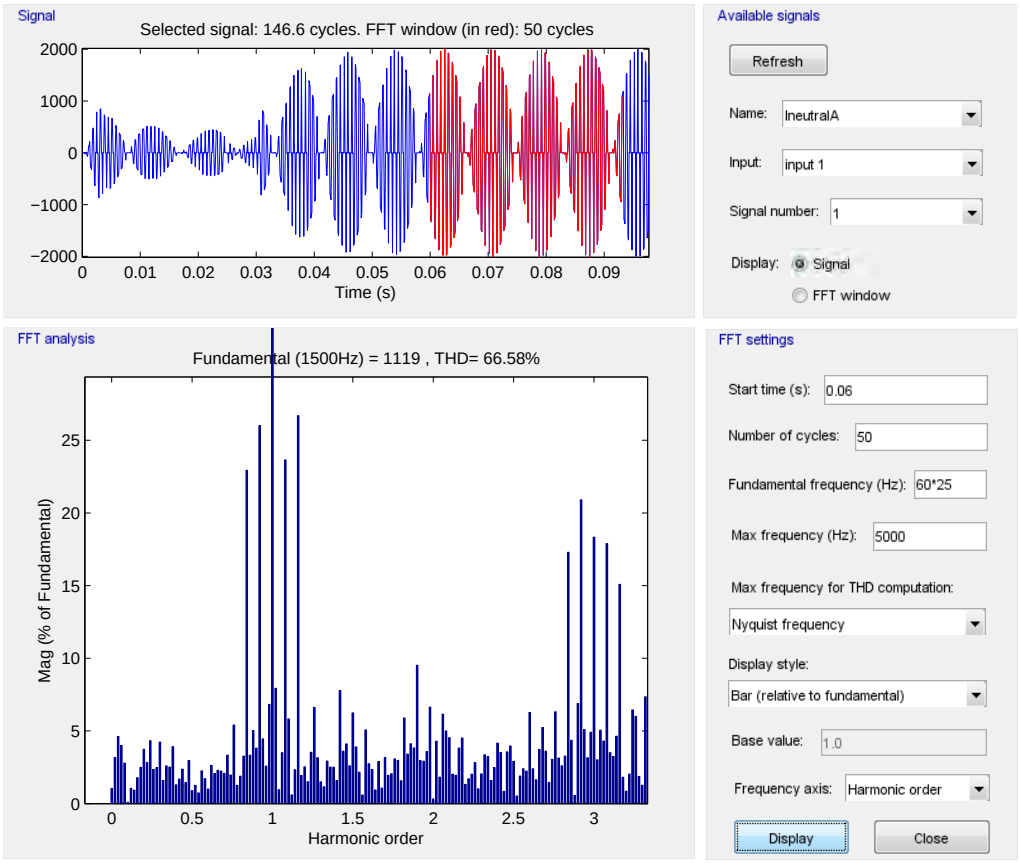


Figure 8.17: Neutral current FFT of a single-phase converter.

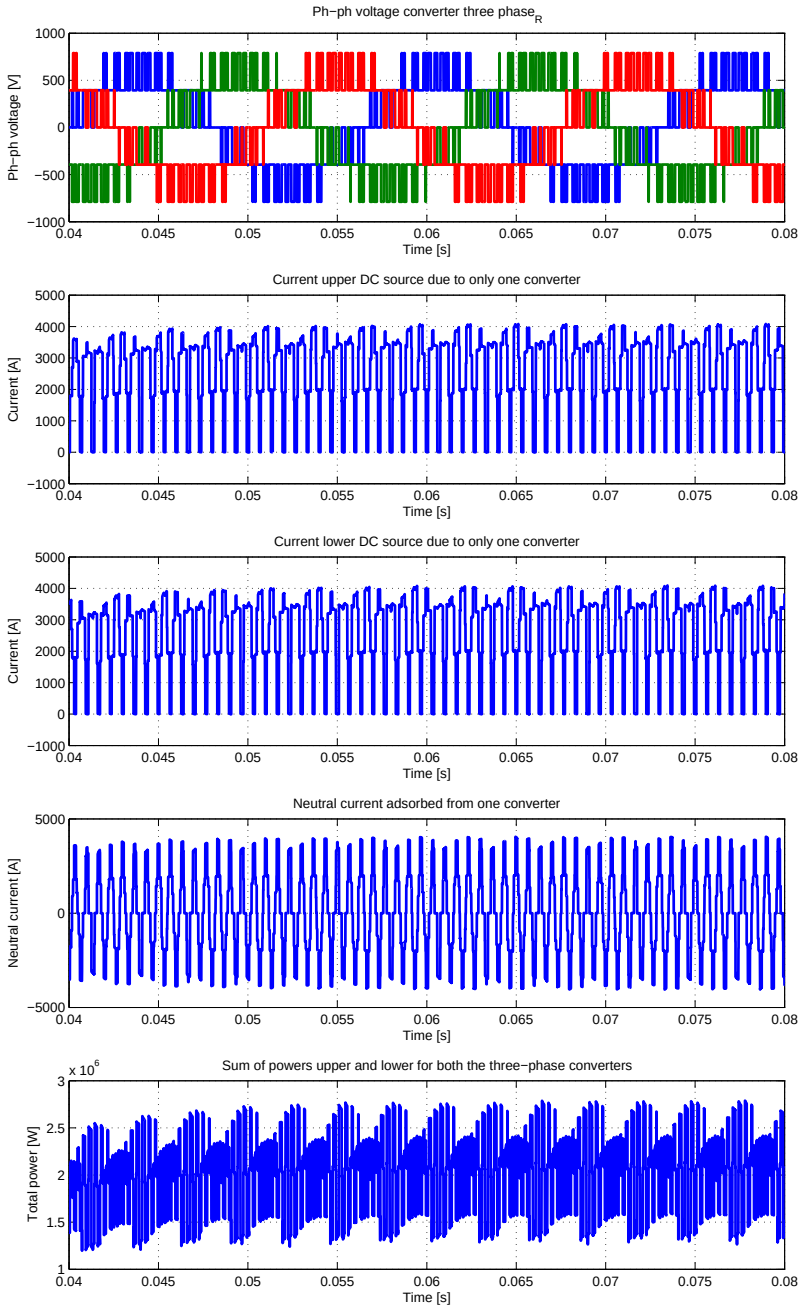


Figure 8.18: A single three-phase converter waveforms.

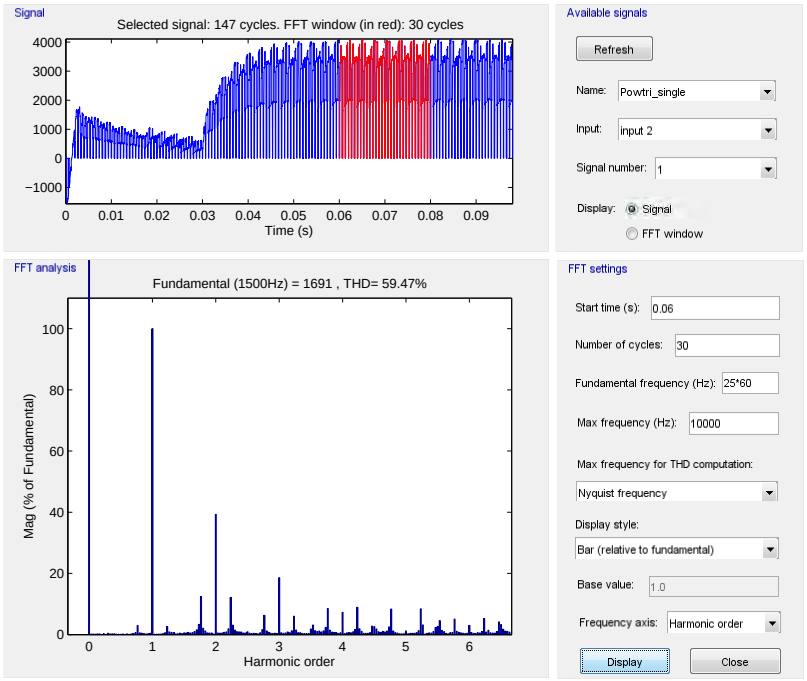


Figure 8.19: FFT analysis of I_{DC}: current in the upper DC source three-phase converter.

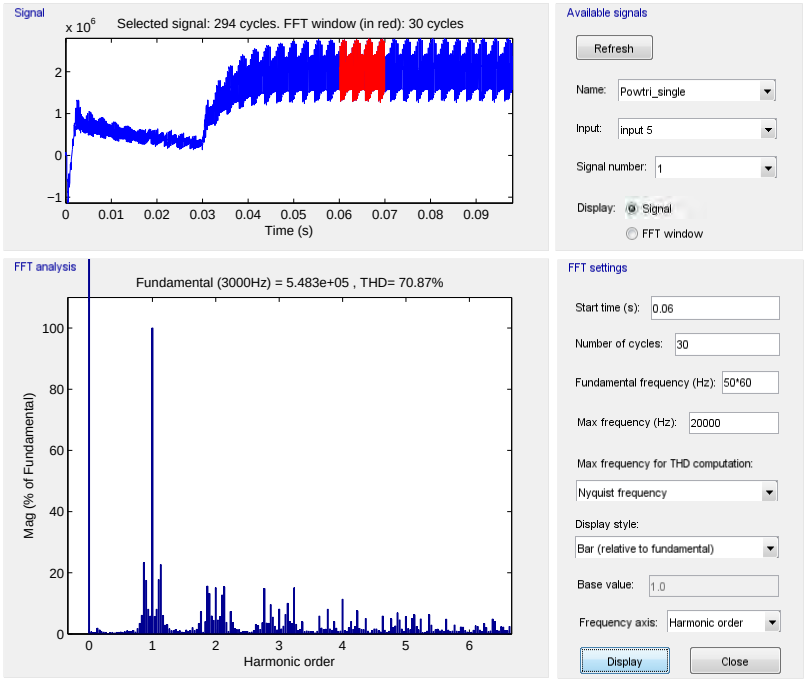


Figure 8.20: FFT analysis of P_{DC}: total DC power of three-phase converters (sum of the upper and lower powers)

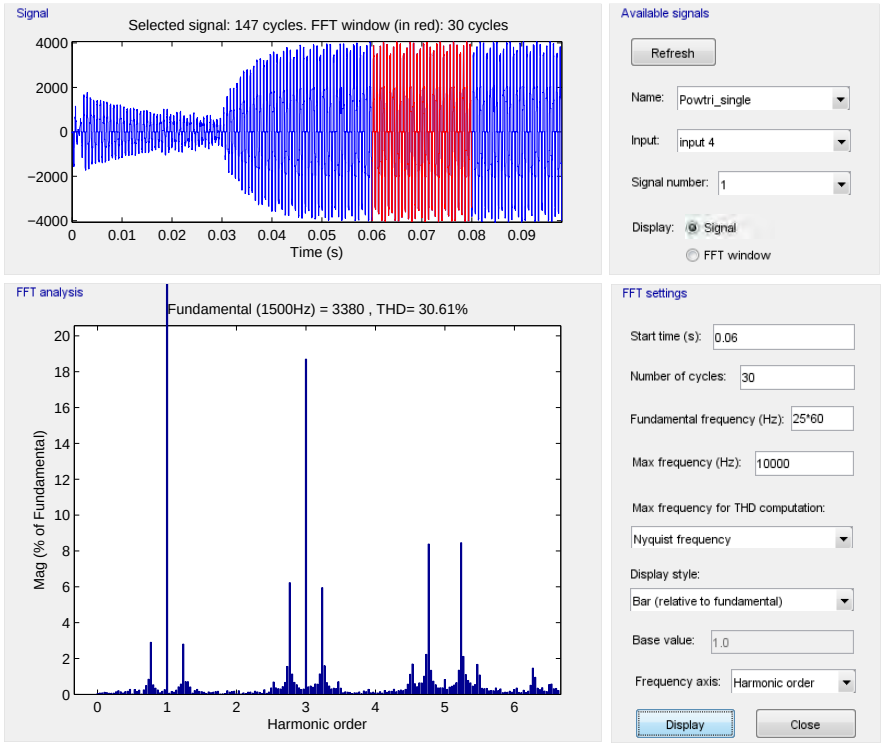


Figure 8.21: FFT of the neutral current of three-phase DC link.

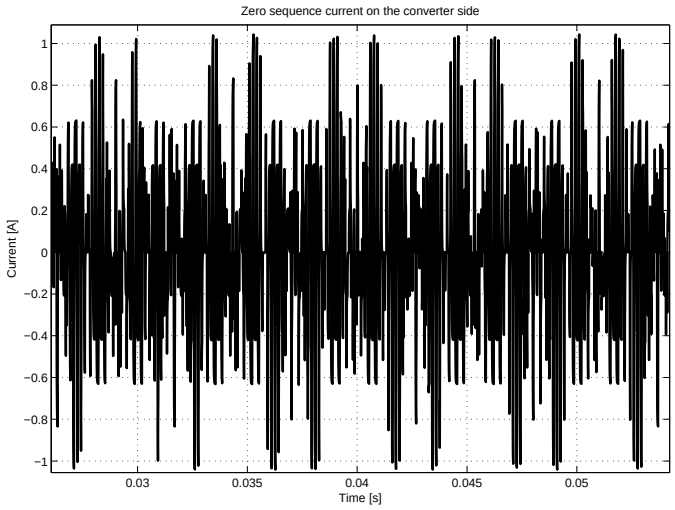


Figure 8.22: Zero sequence current on the converter side: value obtained neglecting the trnasformer zero sequence impedance and considering a constant ZSBTs impedance.

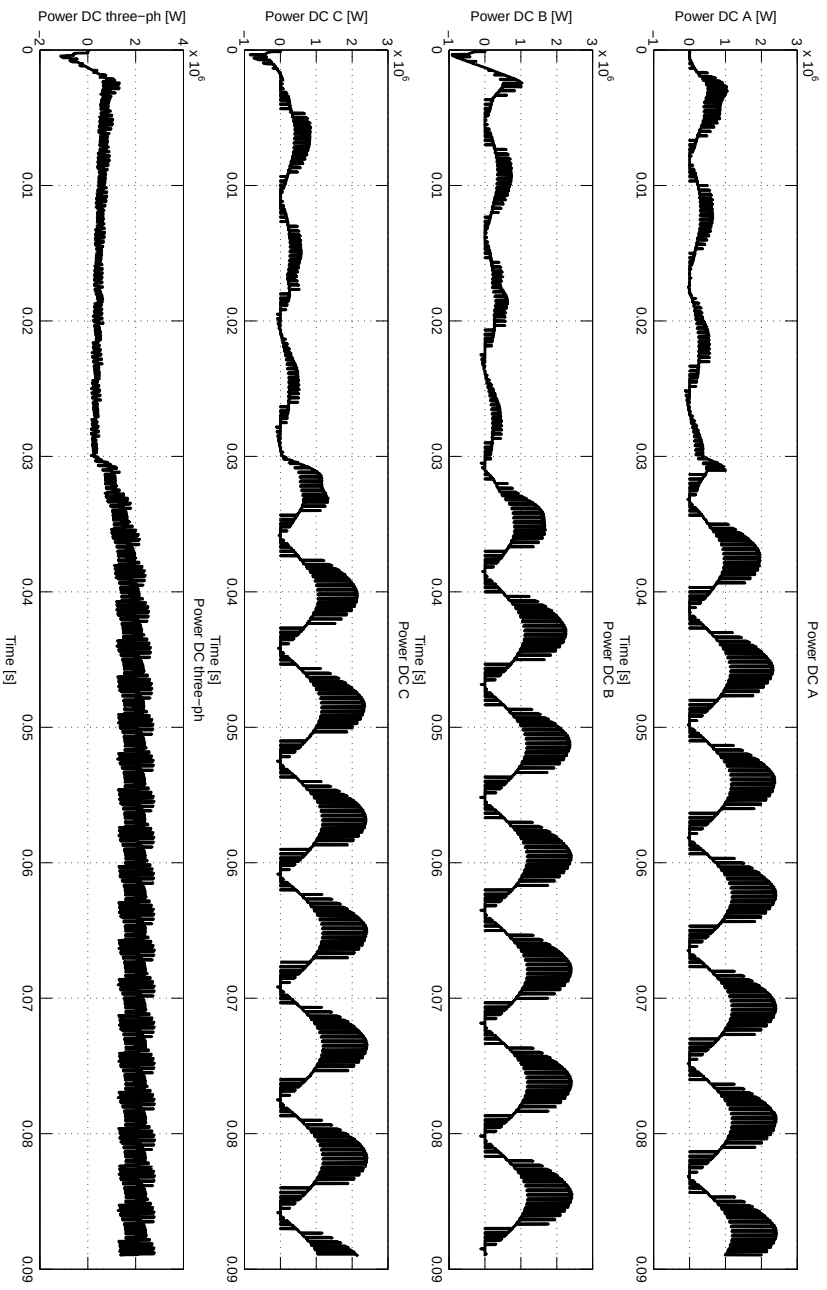


Figure 8.23: Power waveforms in all the DC sides.

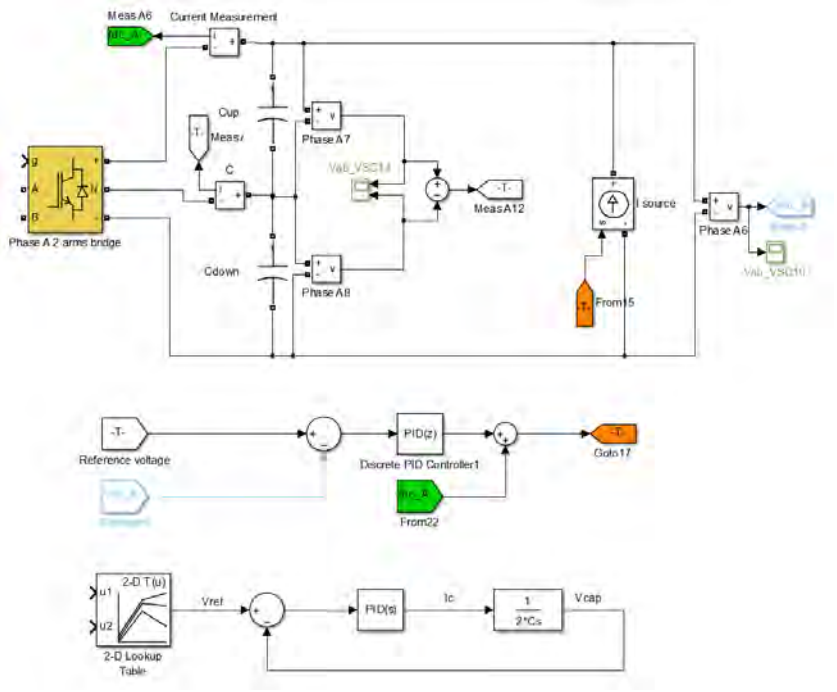


Figure 8.24: DC capacitor circuit and voltage controller transfer function.

a wye-open end configuration, therefore if the neutral point of the transformer and of the grid model is grounded, the zero sequence impedance offered by the grid will not be an open circuit and a zero current will be injected into the grid. Some computational issues must be overcame to simulate the circuit with positive and zero sequence as it will be explained in chapter 9.2. Since in this simulations the interest is focused on the positive sequence, the zero sequence current is considered to remain limited by the ZSBTs and therefore the zero sequence impedance of the transformer is neglected, obtaining a negligible current in comparison with the fundamental one as shown in figure 8.22. The real zero sequence current will be studied in chapter 9.2; if the zero sequence current will be intolerable from the grid and the delta connection cannot be used, the only solution will be to increase the ZSBTs impedance.
Finally in figure 8.23 all the DC powers are shown. Clearly the three-phase converter DC source will require a lower capacitance to filter the harmonics in comparison to the single-phase DC sources.

8.2 DC capacitors

8.2.1 Capacitors design

In the previous chapter the simulations have been run using two voltage sources for each DC source. An interesting point would be to understand what will happen if two capacitors are applied in the DC side of each converter and the DC power is injected using a driven current source with a controller based on the overall DC voltage (that is the sum of the voltage in each capacitor). This solution for one single-phase converter is represented in figure 8.24. The presented circuit is not able to balance the voltage difference between the upper and lower capacitors and the hypothesis beyond the model is to consider negligible the current derived by the neutral connection. Therefore the current source has to provide the current Idc_A adsorbed by the converter and the current to balance the total voltage Vdc_A. The loop obtained without PI is stable (single pole), adjusting the PI parameters the delay that the DC source introduce regulating the DC voltage may be simulated. Since the regulation involves the active power delivered by the power plant, when a voltage reference step is applied the power produced by the source must be adjusted. This process may have an high time constant depending on the type of used power sources: if for example a wind power plant is considered the time constant involves the pitch regulation.
The first step is the capacitor design for the single-phase converters. Using equation 3.2 proposed in [14] here reported:

$$V_c = \frac{\int I_c \, dt}{C} = V_{DC} + \frac{V_m \cdot I_m}{4 \cdot V_{DC} \cdot \omega \cdot C} \cdot \cos(2\omega t) \tag{8.8}$$

and considering the results obtained in the previous chapter it is easy to see that the first current harmonic with frequency $2 \cdot f = 2 \cdot 60 = 120\ [Hz]$ requires a capacitor to limit the ripple to 10%:

$$\Delta v_{\%} = \frac{V_c - V_{DC}}{V_{DC}} \cdot 100 = \frac{V_m \cdot I_m}{4 \cdot \omega \cdot C \cdot V_{DC}^2} = \frac{m \cdot I_m}{4 \cdot \omega \cdot C \cdot V_{DC}} \tag{8.9}$$

$$C_m = \frac{m \cdot I_m}{4 \cdot \omega \cdot \Delta v_{\%} \cdot V_{DC}} = \frac{1 \cdot \sqrt{2} \cdot 2000}{4 \cdot 2\pi \cdot 60 \cdot 1000 \cdot 0.1} = \ 18.76\ [mF]. \tag{8.10}$$

In equations 8.9 and 8.10 the modulation index has been fixed to 1, the RMS current in the AC side is $I = 2\ [kA]$ (the maximum), the DC voltage has been fixed to $V_{DC} = 1\ [kV]$ and the current derived by the neutral point is neglected (reasonable looking only at the frequency $f = 120\ [Hz]$). The resultant capacitance is the series of upper and lower capacitance. One of the hypothesis behind equation 8.8 was $\phi \simeq 90°$ that is verified if the converter injects mostly reactive power. Therefore the singles capacity will be: $C_{m-single} = 2 \cdot C_m = 37.52\ [mF]$.
The same reasoning can be applied for the three-phase converters, remembering that the first harmonic in this case is the switching frequency that appears in each capacitor according to figure 8.20 where also the current harmonic value will be found. With the

three-phase converters the single capacity is studied because the neutral current is not negligible (the switching frequency is involved).

$$\Delta V_c = \frac{\int I_c\, dt}{C} = \frac{I_m}{C \cdot \omega_{hf}} \cdot \frac{2}{\pi} \int_0^{\pi} \sin(\omega t) d(\omega_{hf} t) = \frac{I_m \cdot 4}{C \cdot \omega_{hf} \cdot \pi} \tag{8.11}$$

$$C_{t-single} = \frac{\sqrt{2} I_m \cdot 4}{\omega_{hf} \cdot \Delta V c_{\%} \cdot \frac{V_{DC}}{2} \cdot \pi} = \frac{2000 \cdot \sqrt{2} \cdot 4}{2\pi \cdot 25 \cdot 60 \cdot 0.1 \cdot 400 \cdot \pi} = 9.5[mF]. \tag{8.12}$$

where I_m is the RMS value of the current harmonic with the switching frequency, ω_{hf} is the angular speed associated to the switching frequency and $\frac{V_{DC}}{2}$ and $C_{t-single}$ are the voltage and the capacitance of a single capacitor. These parameters has been fixed to: $I_m = \sqrt{2} \cdot 2$ $[kA]$ (see figure 8.19) and the voltage has been fixed to $V_{DC} = 400$ $[V]$ (see chapter 5). It is possible to understand that the effective ripple depends on the DC voltage: the lower the DC voltage is, the higher ripple is obtained. This is a limitation of the scheme proposed in 8.1.1 where in order to keep the modulation index high the regulation on the DC voltage were proposed. Therefore *an additional condition must be added to the optimizer algorithm* once the ripple limit and the capacitors have been fixed. The feasibility of the adopted solution must also be discussed: in fact the capacitors are crucial components in terms of costs and failure. Volumes, weights and the life-time expectancy must be evaluated in order to obtain an optimal compromise. To evaluate approximatively the volume of the capacitors without using any specific manufacturer data-sheet, this considerations can be made:

$$W_{stored} = \frac{1}{2} \cdot \epsilon_0 \cdot \epsilon_r \cdot E^2 \tag{8.13}$$

where W_{stored} is the energy density stored inside the capacitor, ϵ_r depends on the used dielectric material and E is the maximum electric field reached inside the dielectric. Considering a normal electrolytic capacitor, the parameter can be fixed to $E = 100$ $[\frac{kV}{mm}]$ and $\epsilon_r = 4$. Considering also a packaging factor that takes into account that the dielectric volume is part of the total volume (metallic plates and other insulating materials are present) $k_{pack} = 0.2$ an average energy density can be calculated:

$$W = \frac{1}{2} \epsilon_0 \epsilon_r E^2 \cdot k_{pack} = \frac{1}{2} \cdot 8.85 \cdot 10^{-12} \cdot 4 \cdot (100 \cdot 10^6)^2 \cdot 0.2 = 36\ [\frac{kJ}{m^3}] \tag{8.14}$$

and this means for the single-phase capacitors:

$$W = \frac{1}{2} C V^2 \ \rightarrow\ Vol = \frac{W}{W_{stored}} = \frac{0.5 \cdot 37.5 \cdot 10^{-3} \cdot 500^2}{36 \cdot 10^3} = 0.13\ [m^3]. \tag{8.15}$$

Another parameter that should be checked is the current that the capacitor is able to provide: in the single-phase converters this limit might be strict according to formula 8.4.

Also the economical term must be carefully evaluated: as seen in the previous process, the single-phase capacity is higher than the three-phase because of the 120 $[Hz]$ harmonic and this value may be economically infeasible. In order to reduce the capacity and the current adsorbed by these passive elements, many considerations can be done:

- The DC voltage can be increased and the AC current can be decreased changing the ratio of the transformer and changing the switches according to the new voltage requirements. This solution reduces the capacitor size and the current;
- the DC ripple of the converter can be increased without heavily affecting the AC side and the control of the whole system. This solution must be evaluated carefully because it implies a life-time reduction of the passive components;
- schemes with an active DC filter can be used.

The last solution seems to be attractive and many papers have been proposed to overcome the $2 \cdot fundamental$ frequency issue especially regarding the high power fuel cells field. According to [29] the basic idea of the active filters is to divert the power ripple into another capacitor or inductor that can withstand to heavy currents and voltage fluctuation and therefore it can be reduced in size with longer lifetime. In [29] a scheme with two additional switches and an LC branch is proposed to mitigate the DC ripple in high power applications with low switching frequencies. This solution is depicted in figure 8.26, where also an high frequency insulating transformer is used.
Another solution is the one presented in [30] here depicted in figure 8.27, where a special insulating transformer with a central tap is used with a lower number of devices in comparison with figure 8.26.
A different system is presented in [31] and reported in figure 8.28. This scheme uses again an insulating HF (high frequency) transformer with an higher number of devices but without using the LC branch.
The optimal solution must therefore be evaluated carefully because many factors are involved. The price that must be paid is a more complex structure with an higher number of switches but that may have a crucial role in terms of capacitor size reduction and passive components life expectancy.

8.2.2 DC sources dynamic model

Now that the order of the capacitor size is defined, some considerations can be made on on the PI tuning. The link between the PI parameters and the step response has to be found in order to correctly model the DC source. In figure 8.24 the transfer function block diagram for the current generator loop was presented. The expression in open loop including the PI regulator is:

$$G_{dc-model} = K \cdot \frac{1+sT}{sT} \cdot \frac{1}{sC} \tag{8.16}$$

and the expression in closed loop becomes:

$$G_{dc-model-clo} = \frac{K\dfrac{1+sTC}{s^2TC}}{1+K\dfrac{1+sTC}{s^2TC}} \tag{8.17}$$

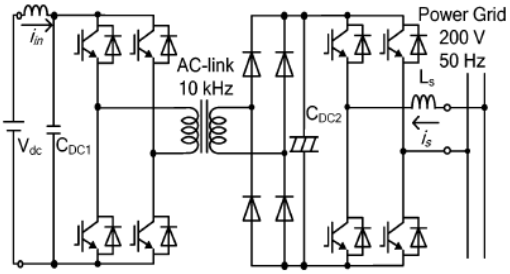


Figure 8.25: Classical configuration with HF insulating transformer.

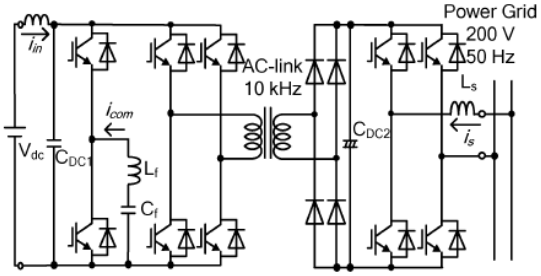


Figure 8.26: DC active power filter proposed in [29] plus HF transformer.

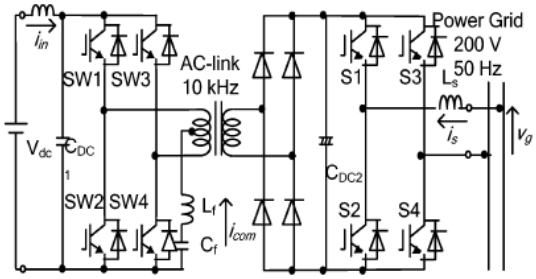


Figure 8.27: Active power filter proposed in [30].

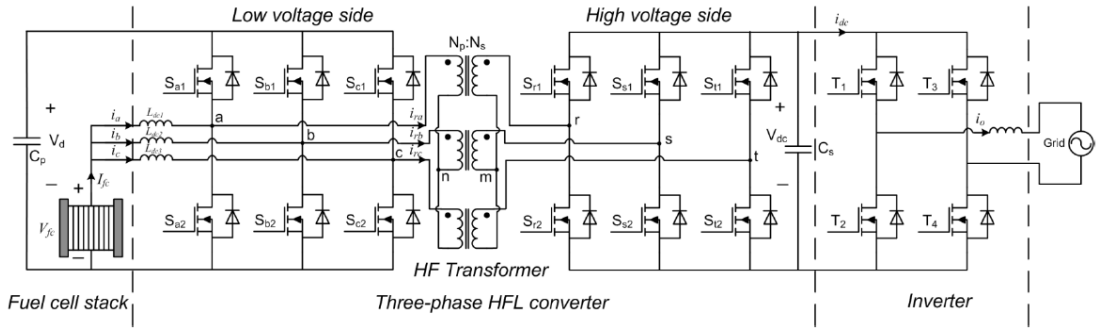


Figure 8.28: Active power filter proposed in [30].

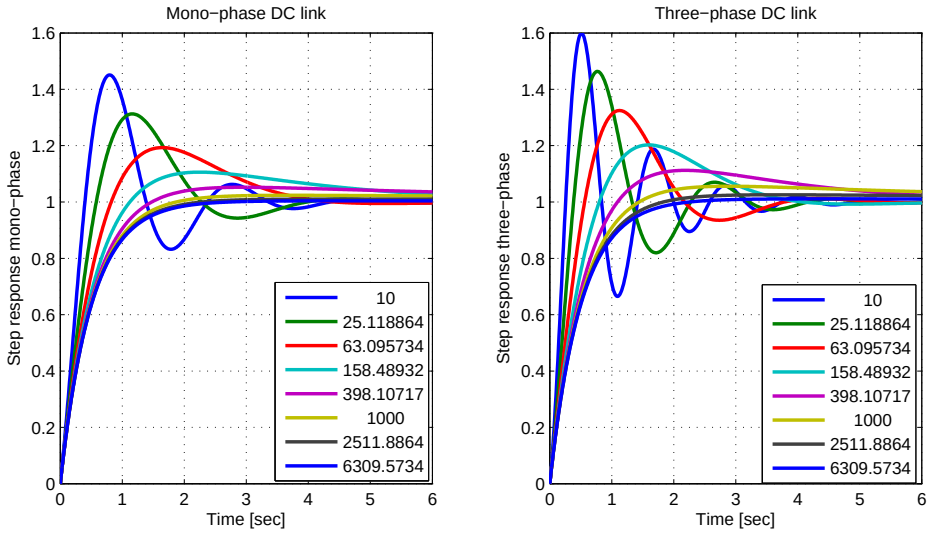


Figure 8.29: Step response with $K = 2$ and variable T.

where K is the PI proportional term, T is the PI time constant, C is the total capacitance (sum of upper and lower). The time response applying an unitary step to the voltage reference is found with the Laplace anti-transform:

$$f = \mathcal{L}^{-1}\left(G_{dc-model-clo} \cdot \frac{1}{s}\right) = 1 - e^{-\frac{K \cdot t}{2}} \left(\cosh\left(\frac{t \cdot \sqrt{\frac{CTK^2}{4} - K}}{\sqrt{CT}} \right) - \right.$$
$$\left. - \left(K \cdot \sinh\left(\frac{t \cdot \sqrt{\frac{CTK^2}{4} - K}}{\sqrt{CT}} \right) \cdot \frac{\sqrt{CT}}{2 \cdot \sqrt{\frac{CTK^2}{4} - K}} \right) \right). \tag{8.18}$$

The proportional gain is inversely related to the time constant of the power regulation, where $\tau = \frac{2}{K}$. If the power regulation is related to a mechanical process, this time constant will be low; $\tau = 1$ $[s]$ and $\tau = 0.667$ $[s]$ for example can be chosen, correspondent to $K = 2$ and $K = 3$. The second parameter to be designed is the time constant T of the PI, using the capacitance values found in equations 8.10 and 8.12.

Figure 8.29 shows the results obtained for the step response for single-phase DC link and three-phase DC link. With a lower capacity the overshoot and the settling time using the same parameters K and T is higher. The characteristic chosen may be different for the DC links according to the type of power plant used. The case $T_{single} = 400$ and $T_{three} = 7500$ is considered in this thesis. The PI parameters are reported in table 8.1.

Since the dynamic for the DC sources is quite slow, the voltage on the capacitors may decrease during fast power changing. This fact is visible also in the modulation index that will increase in this case. When the DC source responds the modulation index will return at the set value.

single-phase DC	K_p	2
	K_i	0.005
Three-phase DC	K_p	2
	K_i	0.0004

Table 8.1: PI parameters of the DC sources models.

8.2.3 Balancing issues

It is well known that the NPC topology suffer of DC voltage unbalancing problems. While the sum of the voltages of the capacitors is controlled by the external source (current generator loops) nothing guarantees the equal distribution of voltages between each component. This cause asymmetries on the voltage output in AC side and leads to unstable operation. According to [28] the different voltage values can also lead to premature failure of the switching devices and the THD of the output current increases because low-order harmonics appear and become dominant. In figures 8.13 and 8.18 the waveform of the neutral current is depicted. This current as already explained appears when the zero state is applied and this current affects the voltage balance of the capacitors. A simple example is given in figure 8.30 that is valid for three-phase converters. The switching modulation scheme in this case is space vector modulation; the small vectors have influence on v_z. Normally the neutral current has a null average value and therefore the balancing problem shouldn't be solved looking at one fundamental period (an unbalance waveform expected with harmonics around the switching frequency with zero average value). According to [2] the neutral point voltage deviations may depend on many factors in addition to the influence of the small and medium voltage vectors including: unbalanced DC capacitor size due to manufacturing tolerances, inconsistency in switching devices characteristics and unbalanced three-phase operation. Therefore the capacitor balancing of each converter must be controlled. An example of unbalanced condition is shown in figures 8.31, 8.32, 8.33, 8.34. The capacity values used are the ones expressed in 8.10 and 8.12. In figure 8.31 the voltage unbalance is depicted, calculated as a difference between V_{upper} and V_{lower}. Due to the big value of the DC capacity the unbalance for the single-phase converters remains limited in amplitude. The frequency that appears in the DC unbalance for the single-phase converters is the switching frequency and there is also the sum of two opposite waves with the fundamental frequency according to the results obtained in 8.16 for the neutral current. With this value of capacity the average unbalance remains limited to 5 $[V]$, but as discussed before this value can increase dramatically if the capacitor size is reduced.
In the three-phase DC link the result is unacceptable. The unbalance has peaks of 200 $[V]$ with a DC average voltage of 700 $[V]$. The frequency that appears in the unbalance waveform is the switching frequency, according to 8.21. When the current injected by the inverter grows, the unbalance becomes higher and after $t = 0.08$ $[s]$ the converter has an unstable operation as shown in figures 8.34 and 8.32. Therefore a balancing tech-

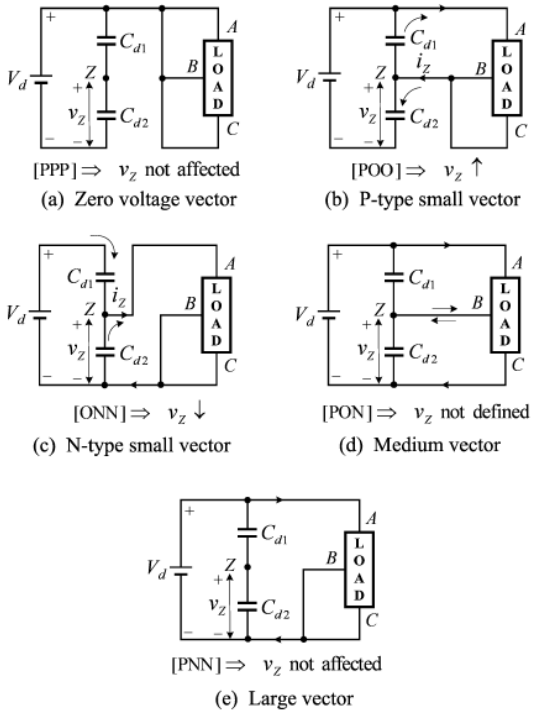


Figure 8.30: SVM effect on the neutral point voltage [2].

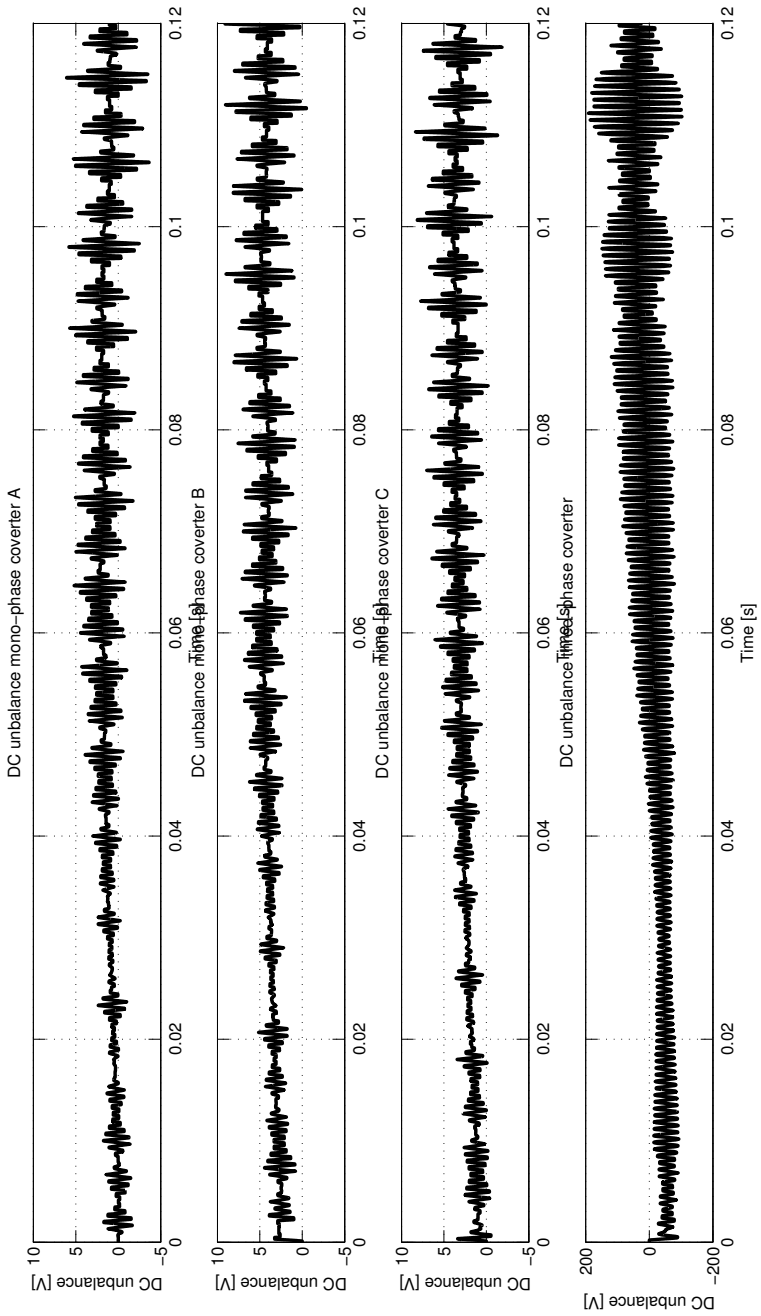


Figure 8.31: Voltage unbalance in all the DC links.

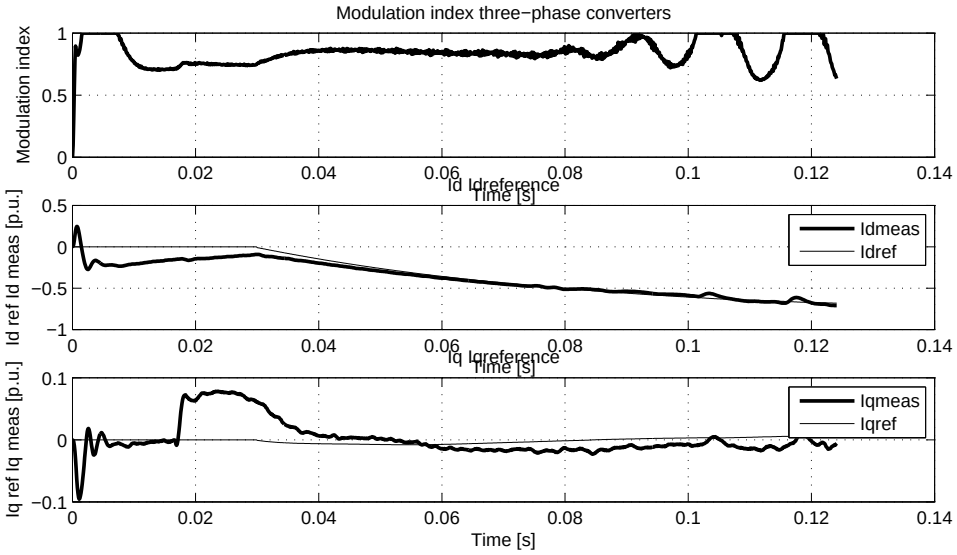


Figure 8.32: Control signals in the unbalanced operation.

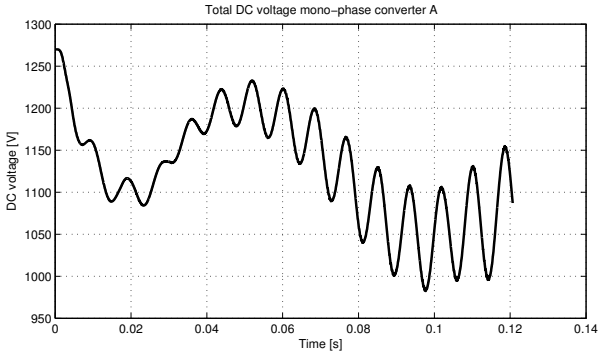


Figure 8.33: DC link voltage of the single-phase converter A in unbalanced operation.

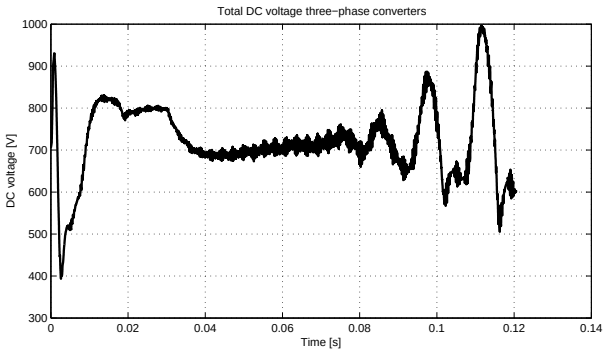


Figure 8.34: DC link voltage of the three-phase converters in unbalanced operation.

nique for all the DC buses must be implemented. From figures 8.33 and 8.34 it is possible to validate the capacity values obtained setting the ripple to 10% in the operation with a current lower than the maximum one.
Many techniques have been proposed in literature to deal with the unbalance operational behaviour. Some techniques use a modified switching pattern in order to use the states resonances to control the voltage sharing between the capacitors. Other techniques use an additional external circuit with additional switches and components to control the voltage balance. Obviously a balancing algorithm without adding other components to the topology is desirable, however the modified switching pattern must be studied carefully to obtain a low impact on the THD and harmonic content of the output waveform. Many articles are focused on the three-phase converter balancing system using an SVM modulation where the dwelling time of the redundant vectors is changed in order to keep the neutral point voltage control. In the studied topology the adopted modulation scheme is carrier based in order to apply interleaving between the converters.

In [32] a really suitable balancing method is proposed. This technique is based on voltage injection for single phase three-level converters when the carrier based modulation is used. This paper firstly explains that when an unbalance occurs, the carrier based PWM algorithm is powerless. The used converter model is presented in figure 8.35 and four general cases are depicted in figure 8.36. Two vectors are defined as "redundant" if applying one or the other nothing changes from the point of view of the voltage applied to the load. The redundant vectors that have influence on the neutral point voltage are: $(1,0)$ and $(0,-1)$ when $u_a > 0$; $(0,1)$ and $(-1,0)$ when $u_a < 0$. In a switching period Ts the duty time of redundant states may be calculated as:

$$\begin{cases} T_{(1\ 0)} = (1+u_b)T_s \\ T_{(0\ -1)} = (1-u_a)T_s \end{cases} \tag{8.19}$$

where $u_a = -u_b$ because of the modulation strategy. The voltage unbalance is computed as:

$$u_{diff}(t+Ts) = u_{diff}(t) + \frac{i_s}{C}[d_{(1,0)} + d_{(-1,0)} - d_{(0,1)} - d_{(0,-1)}]T_s \tag{8.20}$$

where d represents the duty ratio of each combination and i_s is the AC current. As explained in [32], the voltage unbalance substituting equation 8.20 in 8.19 can be obtained:

$$\Delta u_{diff} = \frac{1}{C} \cdot (T_{(1,0)} - T_{(0,-1)})i_s = 0. \tag{8.21}$$

This equation is obtained for each of the four cases presented in 8.36 and therefore when an unbalance phenomenon occurs the algorithm is powerless. This fact can be easily validated if different initial pre-charge voltages on the capacitors are supposed. In figure 8.37 an initial unbalance of $+65$ $[V]$ is used in the single-phase converter A. As shown, this initial offset remains unchanged and the unbalance develops in the same way of the other single-phase converters.

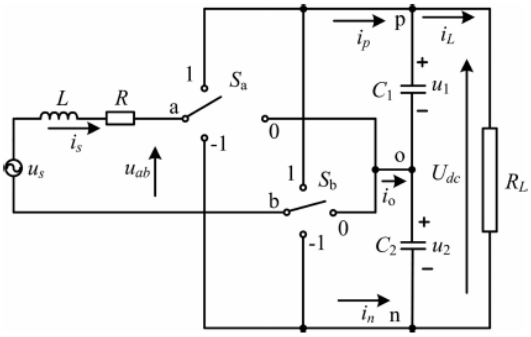


Figure 8.35: Single-phase converter model used in [32].

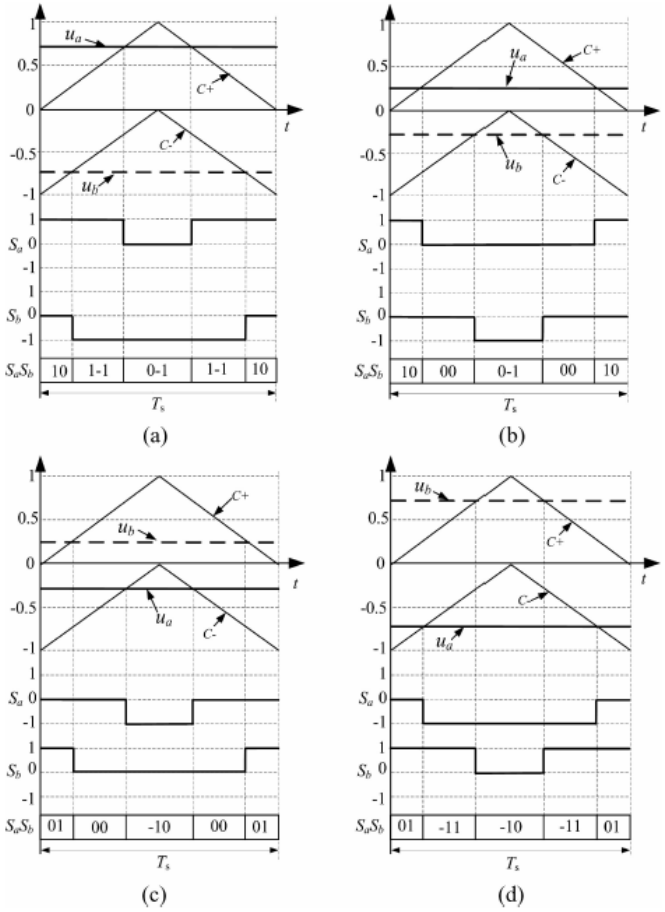


Figure 8.36: Unipolar three-levels CBPWM shown in [32] for different reference signal states.

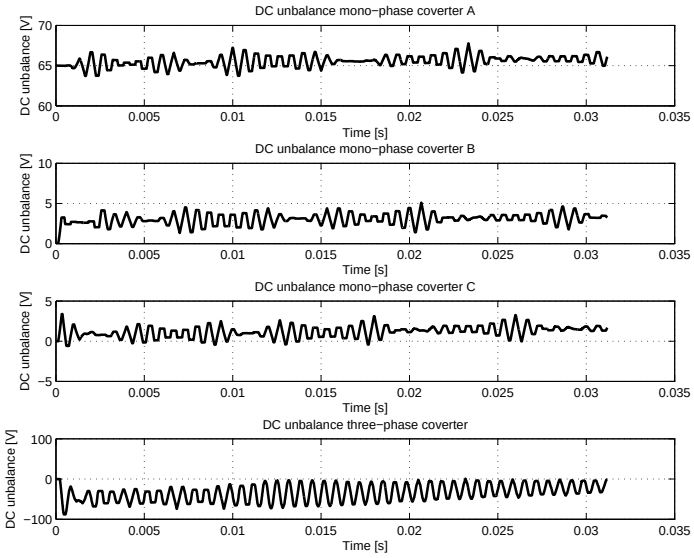


Figure 8.37: DC voltage unbalance with different pre-charge voltage in single-phase converter A.

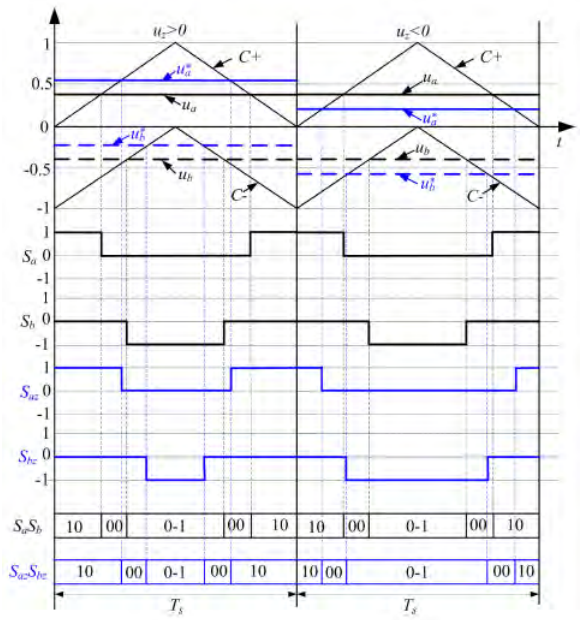


Figure 8.38: CBPWM-OVI with $u_a < 0.5$ [32].

8.2.4 Single-phase balancing system

The balancing circuit for the single-phase converter is the one described in [32]. In this paper two methods of voltage injection are proposed: the former is the CBPWM-OVI (output voltage injection) and the latter is CBPWM-MOVI (maximum OVI), where the offset voltage is maximized. The OVI method has been chosen for this study because it guarantee an harmonic content of the line current centred around $2 \cdot f_s$ in comparison with the MOVI strategy that introduces harmonics around the switching frequency. The price to pay is a response slower than MOVI and an higher number of switching commutations each period.
In figure 8.37 the CBPWM-OVI strategy is depicted: in the first period the offset voltage v_z is positive while in the second period negative. Because of the offset the redundant vectors time is changed:

$$\begin{cases} T_{(1\ 0)} = (u_a + u_z)T_s \\ T_{(0\ -1)} = -(u_b + u_z)T_s \end{cases} \tag{8.22}$$

and therefore with a good choice of the offset the neutral unbalance may be adjusted. In [32] the voltage unbalance follows the law:

$$u_{diff} \cdot \frac{du_{diff}}{dt} \leq 0 \tag{8.23}$$

in order to achieve a reduction. Two solutions to compute the offset voltage are proposed in [32]:

$$uz = -sgn(u_{diff} \cdot sgn(i_s) \cdot sgn(u_a) \frac{k|u_{diff}| \cdot (1 - |u_a|))}{U_{dc}} \tag{8.24}$$

$$uz = \frac{-sgn(i_s) \cdot sgn(u_a) \cdot k \cdot u_{diff} \cdot (1 - |u_a|)}{U_{dc}} \tag{8.25}$$

where k is a coefficient greater than zero and V_{dc} is the total DC voltage on the DC bus. Equation 8.25 has been chosen because of the linear dependence on the voltage unbalance that makes the balancing action stronger when the voltage difference is high. To keep the regulator in the linear modulation region uZ has been limited to:

$$u_z = \begin{cases} u_z & if\ |u_z| < |u_{ZL} \\ u_{ZL} & if\ |u_z| \geq |u_{ZL}, \end{cases} \tag{8.26}$$

where:

$$|u_{ZL}| = \begin{cases} |u_a| & if\ |u_a| \leq |0.5 \\ 1 - |u_a| & if\ |u_a| > 0.5. \end{cases} \tag{8.27}$$

Another condition on u_z has also been implemented as suggested in [32] in order to limit the maximum voltage step, based on the comparison between the previous and the running u_a. The algorithm has been implemented through Matlab ® functions, as shown in figure 8.39.
In figure 8.40 an initial unbalance equal to $u_{diff} = +65\ [V]$ is set in the DC link of

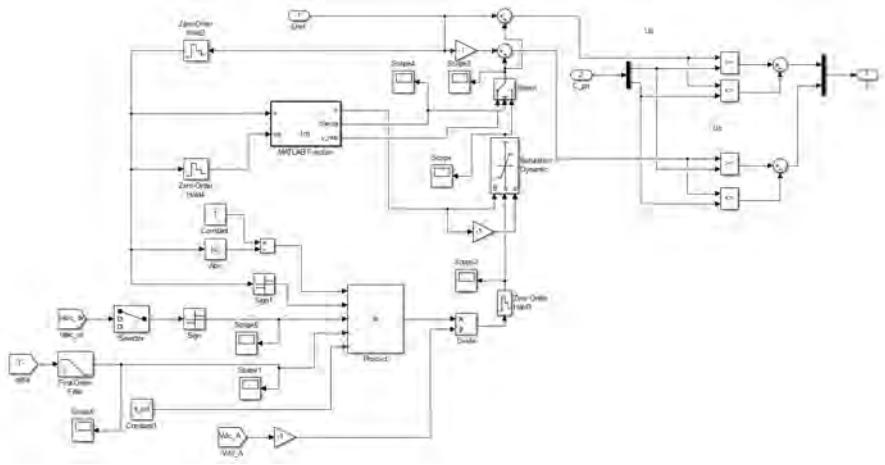


Figure 8.39: Balancing circuit implementation.

the converter A. As it can be noticed the unbalance is deleted at $t = 15$ $[ms]$ thanks to the balancing algorithm. In figure 8.41 and 8.42 the same simulation presented in section 8.2.3 is run with the single-phase balancing algorithms. The total DC ripple is reduced using the balancing circuit and also the oscillations in the unbalancing waveform with high frequency result reduced in comparison with figure 8.31. The coefficient k in the balancing algorithm has been set to $k = 100$. The higher k the faster response is obtained. However a certain limit from the offset voltage saturation must be ensured to keep the regulator in the linear modulation region.

In figure 8.43 the output voltage of the single-phase converter with the balancing operation is shown. The DC voltage ripple affects the waveform but the balancing algorithm has low impact on the frequency spectrum (also because the capacitors are big) as shown in figure 8.44. An important observation that is worth to be discussed is the influence of the single-phase balancing system on the three-phase unbalance waveform in comparison with the operation in figure 8.31. When the inverters are used a zero sequence voltage is always present due to the modulation scheme and because of the closed path also a zero sequence current is generated and limited by the zero sequence blocking transformers. An interesting aspect is to understand if the proposed balancing system for the single-phase converters affects the zero sequence voltage, since one method to balance the DC capacitors of the three-phase converters could rely to zero sequence voltage or current injection. As shown in figure 8.45, the zero sequence voltage impressed by the single-phase converters with or without balancing strategy is approximatively equal when the unbalance is kept low since only a slight difference is present. In figure 8.46 when the unbalance is high the waveforms are different, while when the unbalance is removed the waveforms coincide as visible in figure 8.40. Therefore the zero sequence voltage can be assumed to be independent from the capacitor balance state in the hypothesis of small unbalance and some methods based on the zero sequence can be tried in order to keep

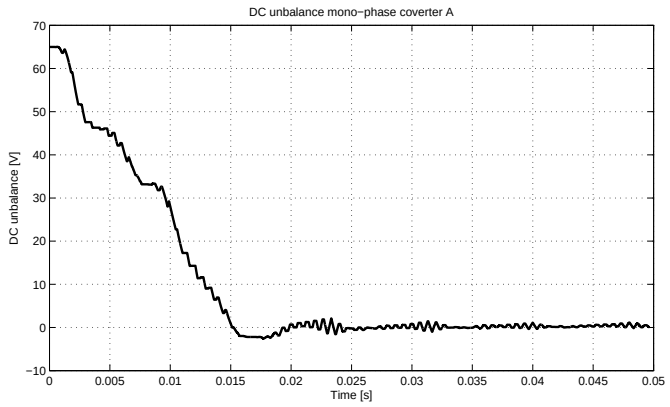


Figure 8.40: Result waveform with an initial unbalance set to +65 $[V]$.

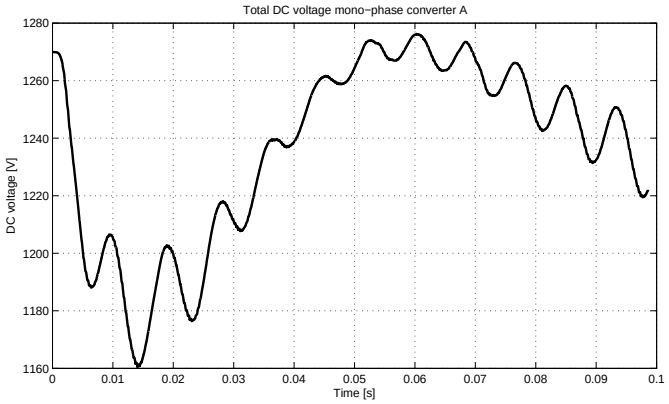


Figure 8.41: DC ripple with balanced single-phase converters.

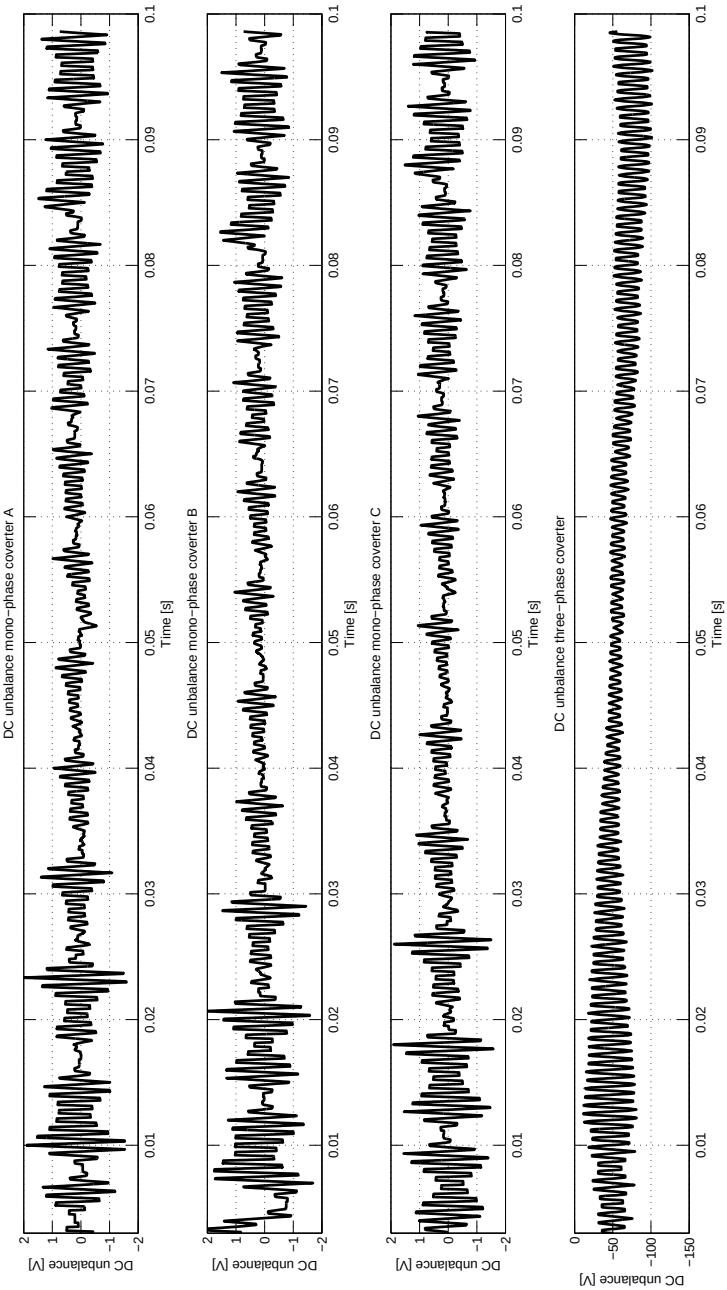


Figure 8.42: Voltage unbalance in all the DC links with balanced single-phase conveters.

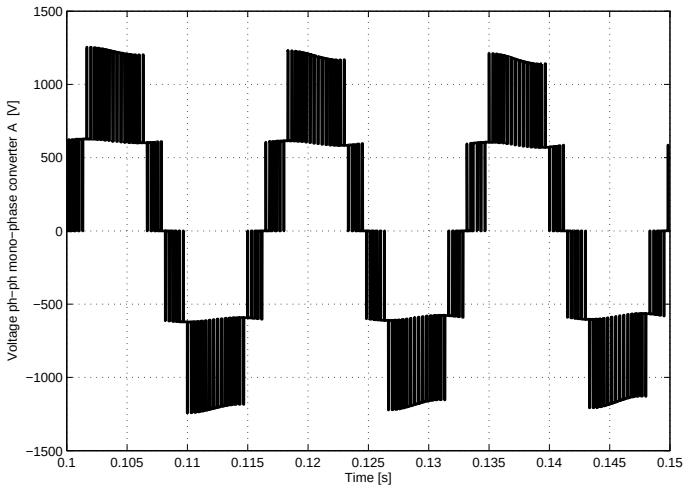


Figure 8.43: Single-phase output phase to phase voltage with balancing algorithm.

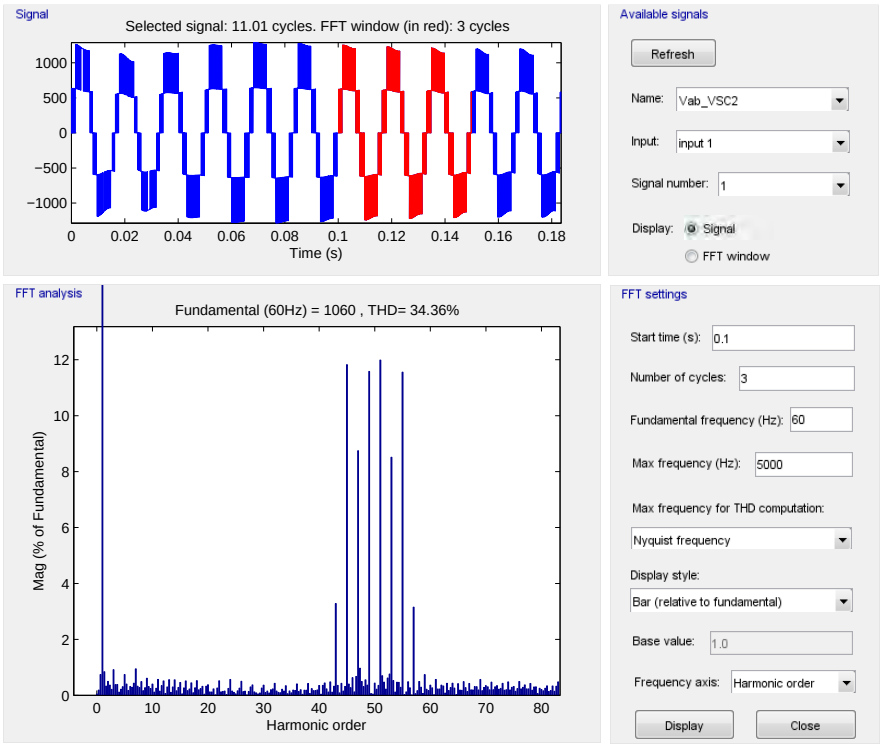


Figure 8.44: FFT analysis of the single-phase output voltage with active balancing.

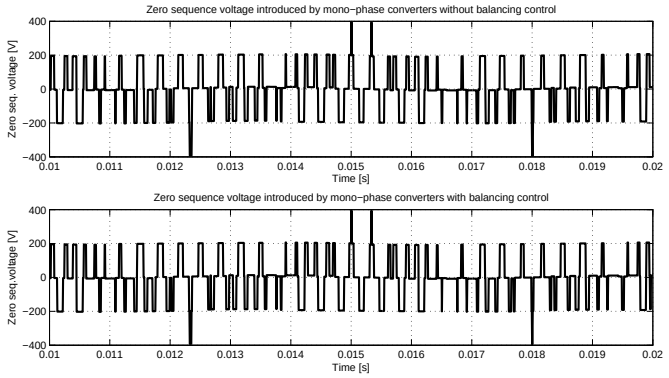


Figure 8.45: Zero sequence voltage introduced by single-phase converters with initially balanced capacitors.

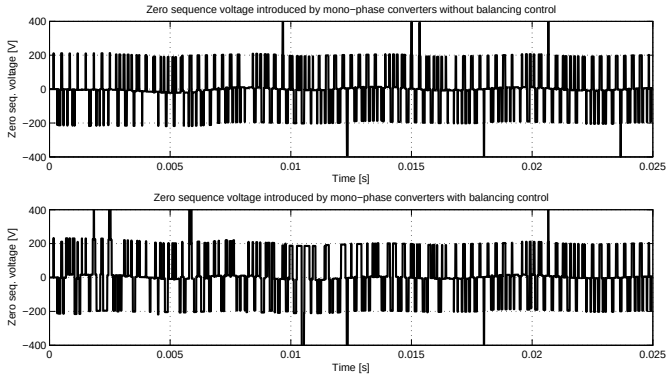


Figure 8.46: Zero sequence voltage introduced by single-phase converters with initial unbalance +65 $[V]$ on the DC link of one converter.

the three-phase DC link balanced.

8.2.5 Three-phase balancing system

The biggest problem to be solved is the one related to the three-phase balance. Because of the small capacity used, the balance system has to be fast enough to guarantee the good operation of the control system. In fact one solution that seems to be potentially suitable for this application could be the one proposed in [33]: an interesting analogy is reported there between the SVM and CBPWM modulation strategies and the balancing circuit is built computing each instant a zero voltage vector that should be added to the reference systems. This method would work if only one converter would be connected to the DC capacitors. Since the three-phase converters share the same DC link, the operation of one converter interferes with the balancing circuit used in the other. Moreover a zero current circulation path is present and the single-phase converters introduce a zero sequence

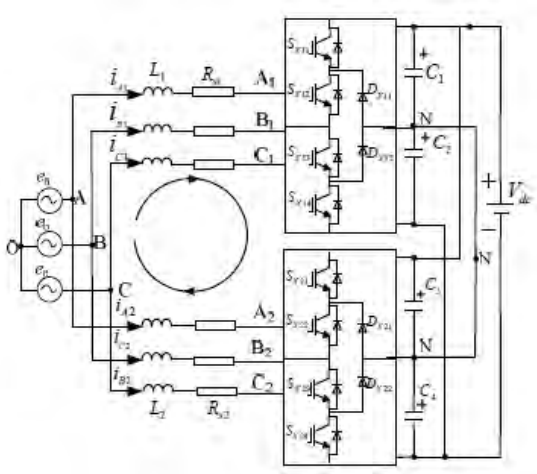


Figure 8.47: Parallel configuration of three-level NPC converters [34].

voltage and the implementation of this method is not simple.

Neglecting the single-phase converters, the topology is similar to the one presented in figure 8.47 where two three-phase three-level converters are connected in parallel. The difference is that the converters apply voltage phasors in phase opposition and the voltage sources that model the grid are connected in series in the studied topology. In [34] another algorithm based on the zero sequence voltage injection where also the zero sequence current is controlled is presented. However this scheme in the studied topology should take into account the zero sequence voltage applied by the single-phase converters, centred around $2 \cdot f_{switching}$ and this high frequency voltage would saturate the PI of the proposed scheme.
Because of this reasons it seems easier to use an external balancing circuit, keeping the possibility to control the zero sequence current using a zero sequence voltage injection. An interesting solution is proposed by [35] for parallel configurations, where the voltage balancing is obtained through a resonant RLC circuit. In this paper the author explains that when a voltage unbalance occurs the output voltage waveform change his harmonic spectrum because the switching frequency appears while normally it should be deleted because of the unipolar operation, seen as interleaving. This solution can be applied here because of the analogy with a pure parallel circuit, shown in figure 8.47.
The circuit proposed in [35] and the schematic explanation of the harmonic spectrum is reported in figure 8.48; it uses a modified PWM scheme in order to let the switching frequency appears in the output voltage if an unbalance occurs. The RLC circuit is used as a filter tuned on this frequency providing the balancing effect.

In figure 8.49 the voltage difference between the same phases of two converters is depicted when the balancing of the DC bus is not controlled. According to [35] a component with the switching frequency appears as shown in figure 8.50. This component is the one

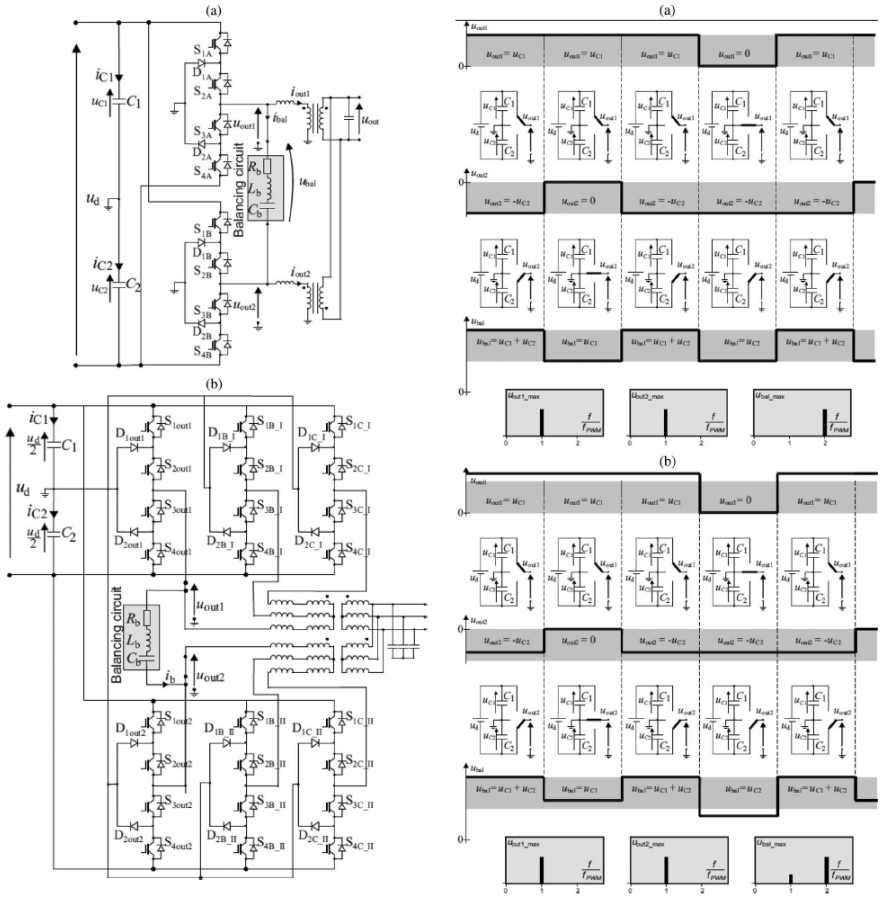


Figure 8.48: Balancing circuit proposed in [35].

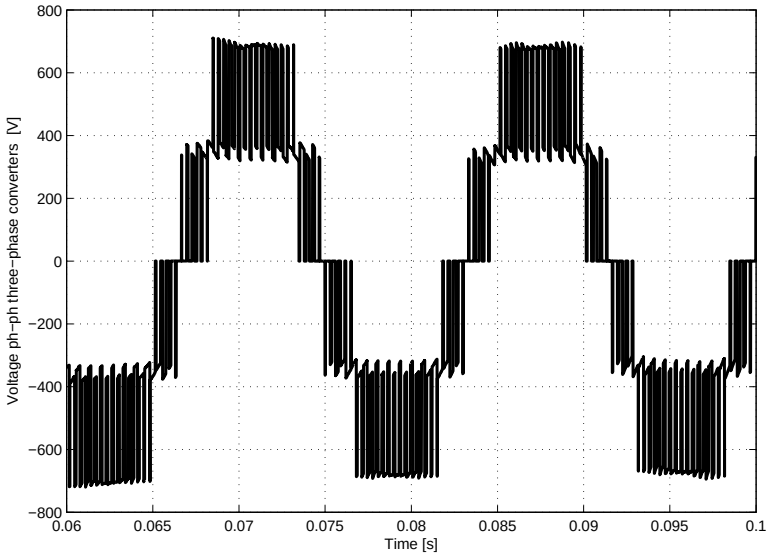


Figure 8.49: Voltage difference between the same phases of the three-phase converters u_{bal} in figure 8.48.

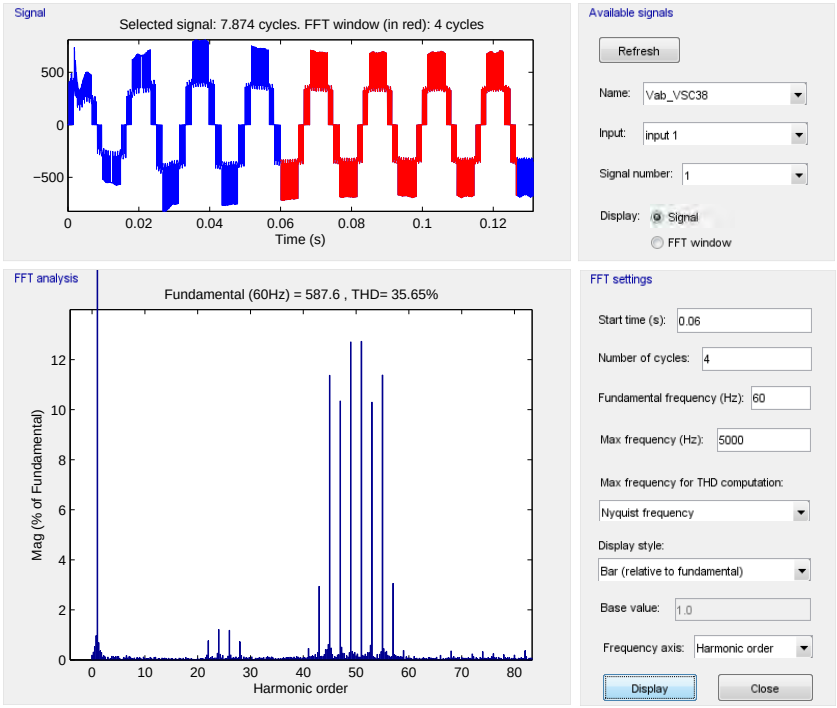


Figure 8.50: FFT analysis of the waveform shown in 8.49.

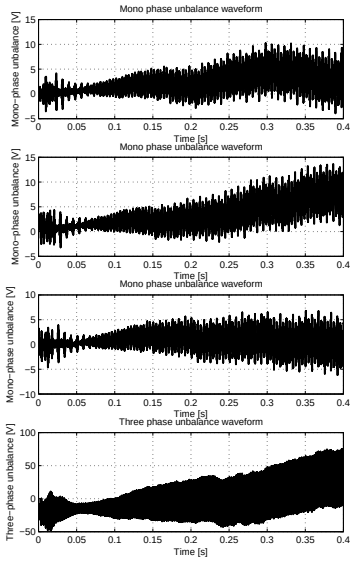


Figure 8.51: Unbalance waveform without balancing circuits and with an initial balanced state.

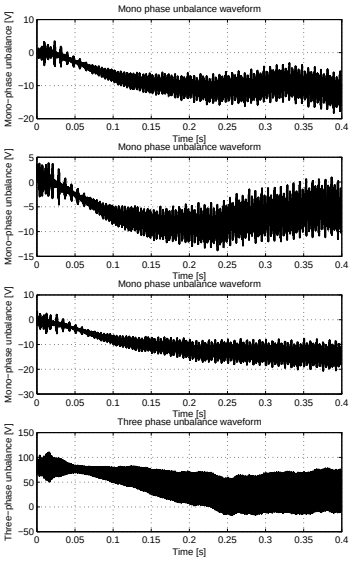


Figure 8.52: Unbalance waveform without balancing circuits and with an initial unbalanced state $V = +100$ $[V]$.

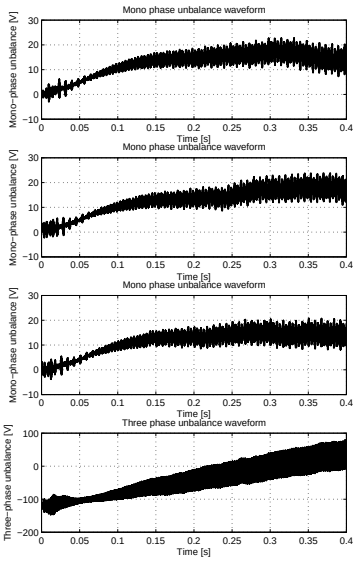


Figure 8.53: Unbalance waveform without balancing circuits and with an initial unbalanced state $V = -100$ $[V]$.

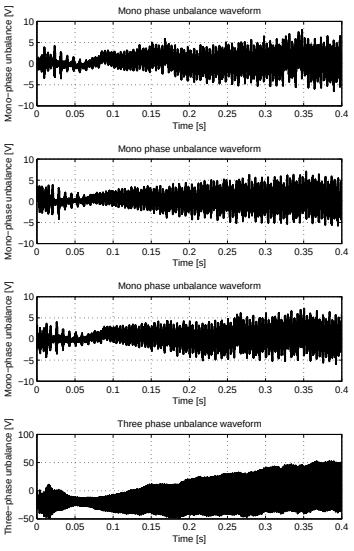


Figure 8.54: Unbalance waveform with single-phase balancing circuits and with an initial balanced state.

that should be used for balancing proposals with the RLC circuit. The other frequencies, centred around the fundamental and twice the switching frequency, only contribute to increment the losses and therefore they should be eliminated.
An initial consideration on the single-phase and three-phase balancing systems interaction must be done. In figures 8.51, 8.52, 8.53 the unbalance waveforms are depicted for all the DC buses without any implemented balancing system. The operating conditions for these simulations are: $Pm = 0.6$ $[MW]$, $Pt = 1$ $[MW]$, $Ptot = 5.6$ $[MW]$, $Vdc_{single} = 1270$ $[V]$, $Vdc_{three} = 764$ $[V]$. Analyzing these simulations the single-phase unbalance is clearly affected by the three-phase unbalance. The result is that the system normally seems to provide a little compensation of the three-phase unbalance, even if this compensation is slow, dependent on the power value and with a big overshoot. The three-phase unbalance leads to the single-phase unbalance that remains limited because of the big capacity used to suppress the low frequency harmonic. As proposed in the previous chapter an interesting solution would be to implement some methods to achieve the ripple reduction in order to reduce the DC capacitor size. With reduced capacitors the unbalance waveform would result increased in amplitude and the balancing algorithm would work in an harsher condition.
In figure 8.54 the single-phase balancing systems work. As discussed before these balancing algorithms help the three-phase balancing even if the result must be improved.
The parameters that have to be chosen are the resistance, the inductance and the capacitance of the series resonant circuit with the constraint of the resonant frequency. The equations are:

$$f_{resonant} = \frac{1}{2\pi \cdot \sqrt{Lb \cdot Cb}} = f_{switching} \tag{8.28}$$

$$\rho = \sqrt{\frac{Lb}{Cb}} \tag{8.29}$$

where Lb,Cb are the inductor and the capacitor of the balancing circuit and ρ is the circuit characteristic impedance. According to [35] the resistance and the characteristic impedance affect the system bandwidth and therefore the circuit selectivity: in a solution with wider bandwidth the variation of the balancing parameters has a lower impact on the balancing capability. In [35] a decrease in ρ has little impact on the speed of the balancing process but cause an increasing in the currents that flow into the RLC circuit; for a bigger ρ the balancing process occurs with higher voltages on the inductor and the capacitor.
Another factor that should be considered is the possibility to use three resonant circuits, one connected to each phase: while the losses in this solution are increased by a factor 3, the obtained overall circuit is equilibrated and every arm contributes to the capacitor balancing action.

In figures 8.55 and 8.56 only one RLC arm is used, while in figures 8.57 and 8.58 a three-phase balancing circuit is used. The values of the resonant circuit have been fixed to: $R = 1$ $[\Omega]$, $\rho = 1$. As expected the balancing response with a three-phase circuit is better than the single-phase solution even if the losses are tripled.

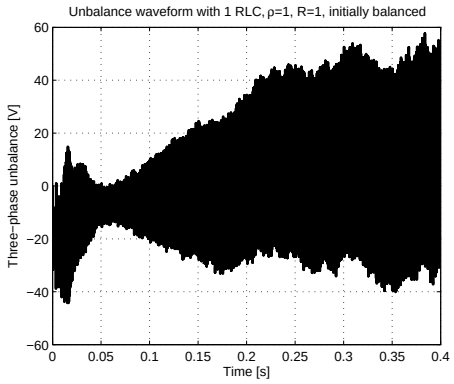


Figure 8.55: Unbalance waveform.

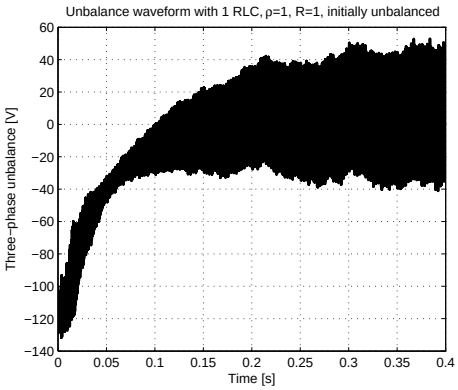


Figure 8.56: Unbalance waveform.

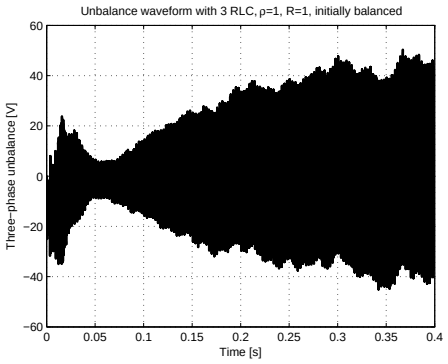


Figure 8.57: Unbalance waveform.

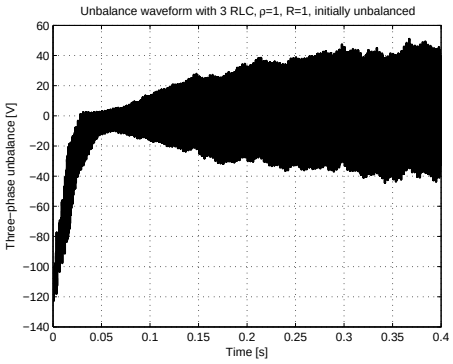


Figure 8.58: Unbalance waveform.

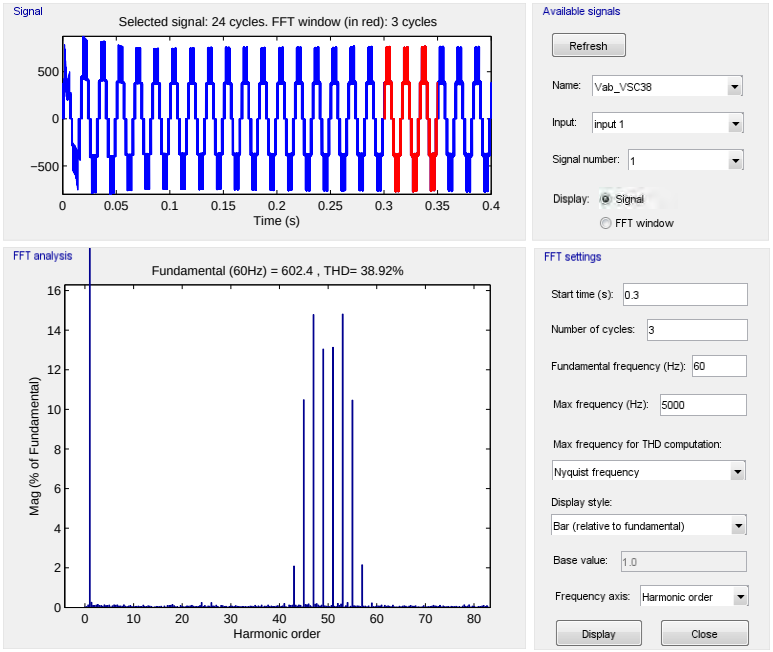


Figure 8.59: FFT analysis of the balancing voltage with the RLC filter.

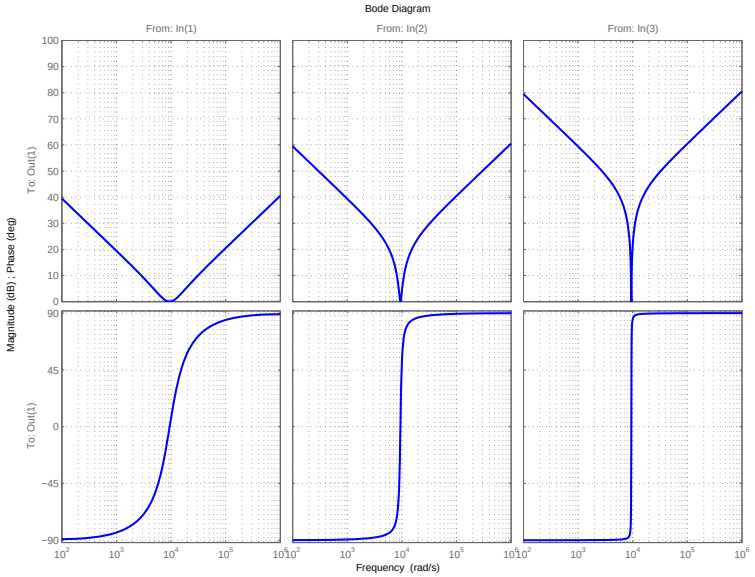


Figure 8.60: Bode's diagrams with $R = 1$ [Ω] and $\rho = [1, 10, 100]$.

ρ []	f [kHz]	R [Ω]	L [mH]	C [μF]	Bandwith[Hz]
1	15	1	0.106	106	1500
10	15	1	1.06	10.6	150
100	15	1	10.6	1.06	15

Table 8.2: Used parameters in per unit system.

In figure 8.59 the harmonic spectrum of the balancing waveform is depicted: the switching frequency harmonic is reduced because of the resonant impedance.
In figure 8.60 the Bode's diagrams of the resonant impedance are depicted for a constant resistance $R = 1$ [Ω] and $\rho = [1, 10, 100]$. Clearly with low values of ρ the bandwidth is higher and the circuit is less selective, while with higher ρ the opposite situation is obtained. The parameters have to be optimally chosen because while a lower selectivity is desirable also to reduce the harmonics around the switching frequency, the impedance at $2 \cdot f_{sw}$ becomes low and higher currents and power losses are obtained. On the other side with an high selectivity a low current is obtained whit a performance nearer to the the one without balancing circuit. The used parameters in each case are reported in table 8.2.
In figures 8.61,8.68 the simulation results are depicted using the same global parameters relatively to the control system and the power delivered. In figures 8.61 and 8.62 the situation without balancing control and with only a single-phase balancing control are depicted respectively. Figures 8.63, 8.65, 8.67 show the three-phase DC unbalance waveform with different ρ, while on the right side in figures 8.64, 8.66, 8.68 the respective current and powers (related to only one arm) are represented. Since the power is due to multiple frequencies, the numerical integration has been used:

$$P = \frac{1}{T} \int_0^T R \cdot i(t)^2 dt. \tag{8.30}$$

This equation computes an average power that can be used for the components sizing; obviously if an high initial unbalance is present, the currents will be higher and the average power should be computed with shorter time steps. Another important parameter that is worth to be considered during the components design is the reached maximum voltage:

$$V_{peak} = \frac{I_{max}}{\omega \cdot C} = I_{max} \cdot \omega L. \tag{8.31}$$

It can be considered that the current depicted in figures 8.64, 8.66, 8.68 has only a component at the switching frequency as a simple hypothesis. The result is therefore represented in table 8.3. Looking at the simulation results the best response is obtained with $\rho = 1$, but the current that circulates in the RLC resonant circuit is high as the power losses. This means higher requirements for the cooling system of the RLC circuit and lower efficiency.

In [35] a solution with a transformer is proposed in order to delete the fundamental frequency current. This transformer introduces a phase shift of 180° in the output voltage

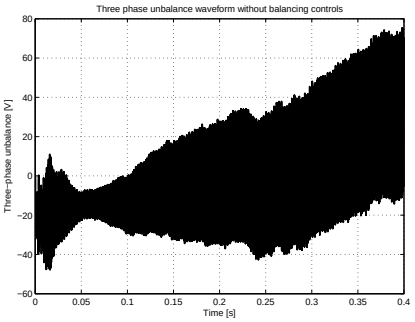


Figure 8.61: Unbalance waveform.

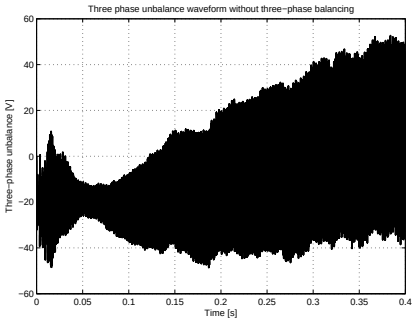


Figure 8.62: Unbalance waveform.

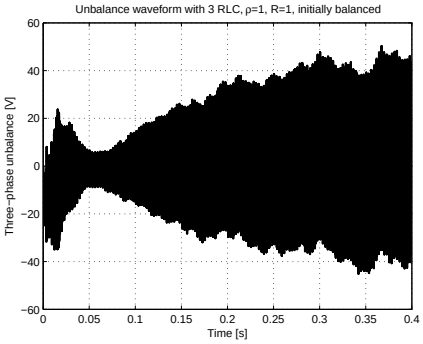


Figure 8.63: Unbalance waveform.

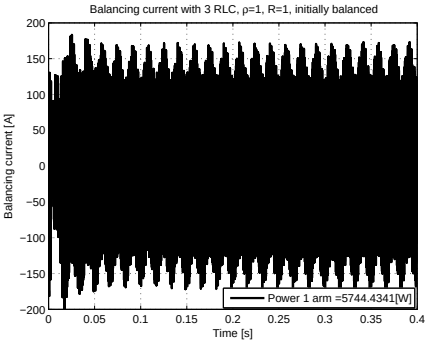


Figure 8.64: Balancing current.

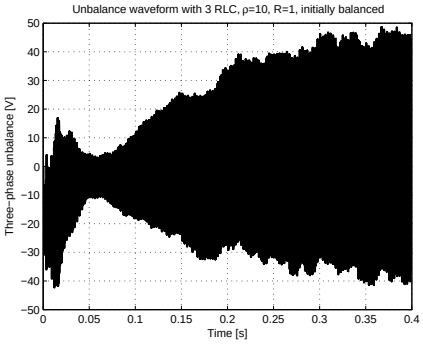


Figure 8.65: Unbalance waveform.

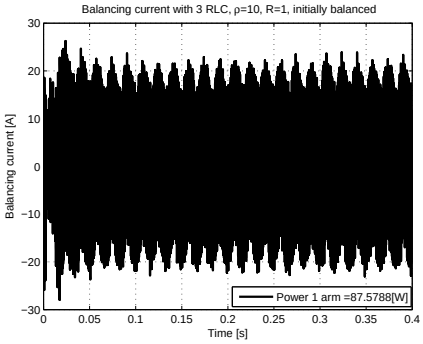


Figure 8.66: Balancing current.

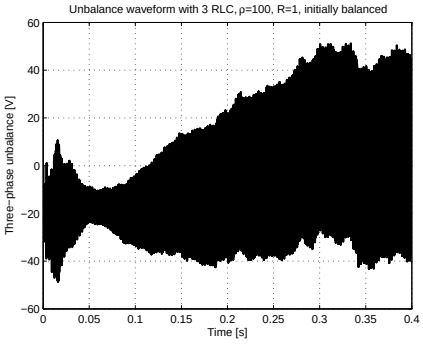


Figure 8.67: Unbalance waveform.

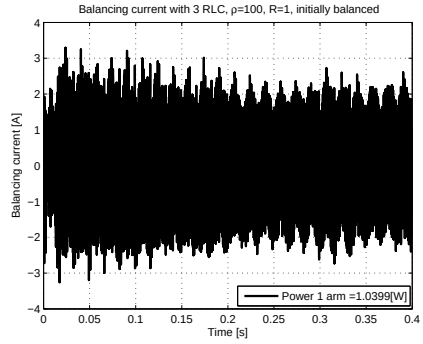


Figure 8.68: Balancing current.

ρ []	R [Ω]	$I_{max}[A]$	$V_{max}[V]$	$Ploss$ [W]
1	1	170	106	$5745 \cdot 3 = 17235$
10	1	25	250	$87.75 \cdot 3 = 263$
100	1	3	300	$1.04 \cdot 3 = 3.12$

Table 8.3: Currents voltages and power losses of the RLC circuit.

of one converter and therefore the fundamental waves are in phase and does not affect the RLC filter behaviour; the disadvantage of using the coupled inductors is the influence of the dispersion flux on the RLC impedance that must be carefully taken into account: the inductance of the resonant RLC is low (100 [mH] with $\rho = 1$) and therefore the transformer should be designed with an high coupling factor and relatively low mutual inductance, that cause an increase of the shunt current. Since the power loss value is acceptable compared to the global power rating and because of the discussed problems, the chosen configuration is the one without transformer. It must be noticed that with this method the current that flows through the RLC circuit is related to the voltage applied (combination of modulation index and DC voltage of the three-phase converter). The parameters that should be used in this case are:

- $\rho = 3$, compromise between the previous results (impedance related to logarithmic scale);
- $R = 1$ [Ω], with $R < 2 \cdot \rho$ that according to [35] guarantees the oscillatory operation of the balancing circuit;
- $f_{resonant} = 1500$ [Hz]
- three-phase RLC, that guarantees the system symmetry.

With these parameters, the simulation results are depicted in figures 8.69,8.72. The power losses are $3 \cdot 902.6 = 2.708$ [kW], the RLC parameters are $R = 1$ [Ω], $L = 318.3$ [μH], $C = 35.37$ [μF] and the maximum voltage is $I_{max} \cdot 2 \cdot \pi \cdot f_{sw} \cdot L = 70 \cdot 2 \cdot pi \cdot 1500 \cdot 318.3 \cdot 10^{-6} = 210$ [V].
In figure 8.73 the currents that appear in the three-phase resonant circuit are depicted; many frequencies appears around $60, 1500, 3000$ [Hz]. Figure 8.74 shows the capacitor voltage on the three-phase DC link. The choice of the capacity is justified by the total voltage ripple, around 10%.
In figure 8.75 the controls signals are represented: the modulation index for the three-phase converter has a certain margin from 1 in order to avoid the unbalanced phenomena found in figure 8.32. An interesting observation is to notice that in the graph of $Iq_{reference}$ the quadrature current measured has some spikes, related to the operation with the single-phase balancing circuits.
The presented solution is suitable when the voltage of the three-phase DC link is low ($Vdc = 765$ [V]). Considering an higher voltage the set of used parameters should be closer to the case $\rho = 1$, depending if it is more important to reduce the power losses or the voltage unbalances.

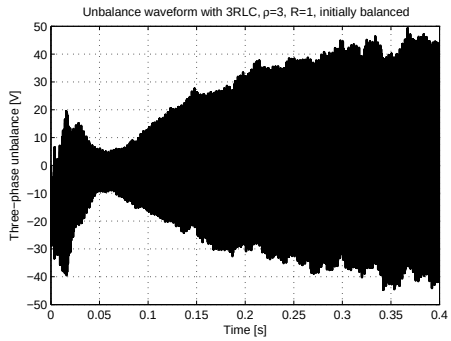


Figure 8.69: Unbalance waveform.

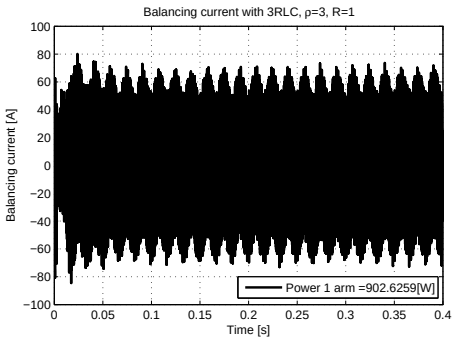


Figure 8.70: Balancing current.

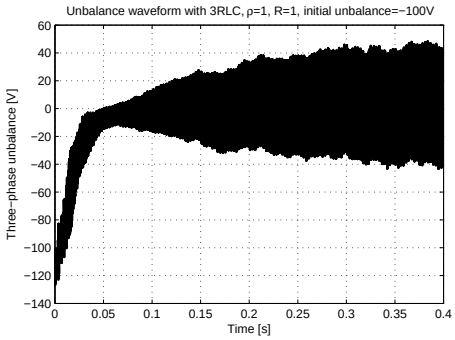


Figure 8.71: Unbalance waveform.

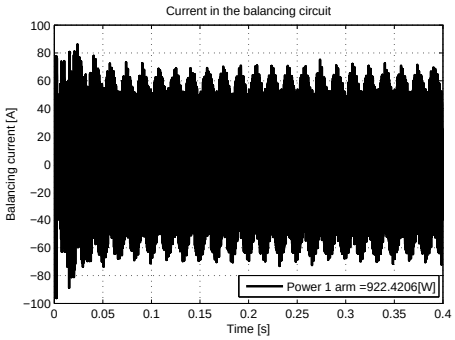


Figure 8.72: Balancing current.

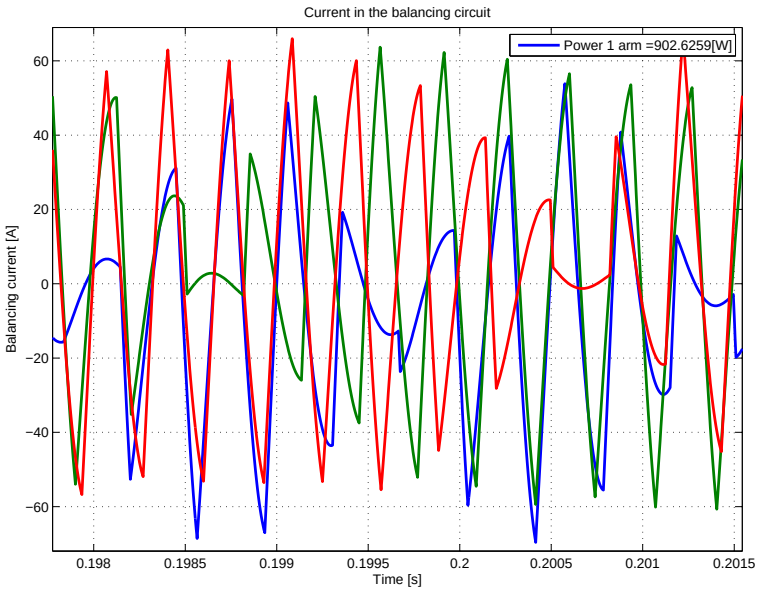


Figure 8.73: Zoom of the balancing currents.

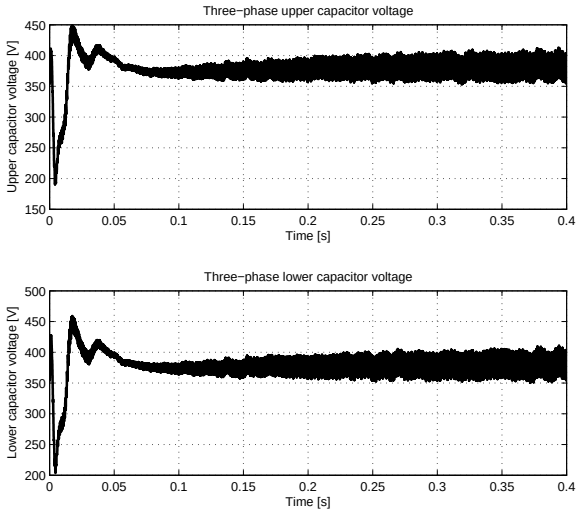


Figure 8.74: DC capacitors voltage of the three-phase converter.

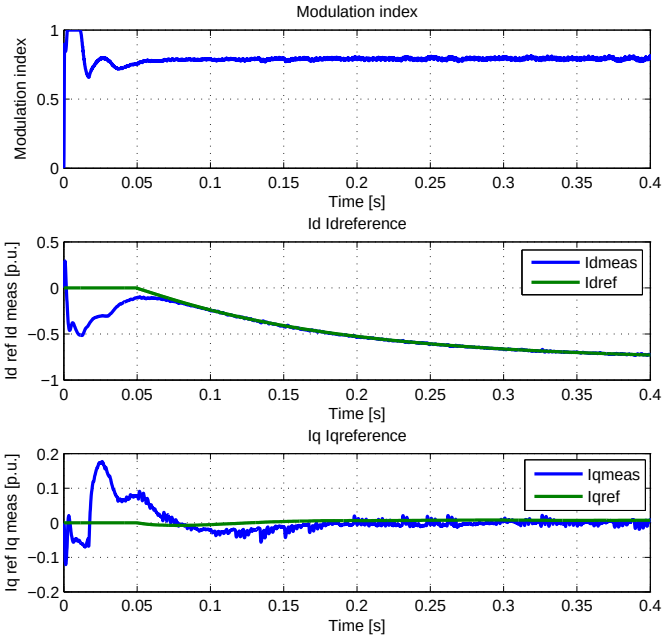


Figure 8.75: Three-phase modulation index, control signals Id and Iq.

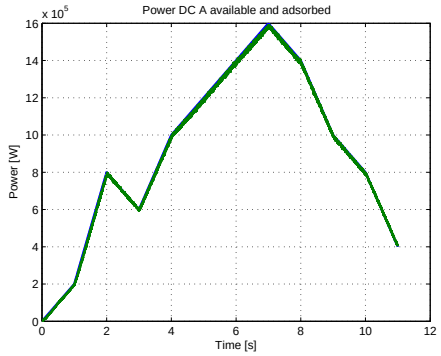


Figure 8.76: Single-phase converter DC available power and adsorbed power.

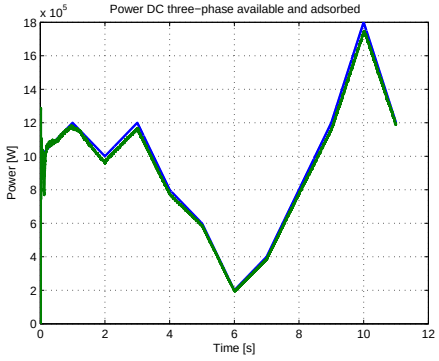


Figure 8.77: Three-phase converter DC available power and adsorbed power.

8.3 Variable sources

An interesting test could be to evaluate the control response when a general input variable source is applied. From the discussion made in the previous chapters, the source controls have the role to control the voltage on the series of the two capacitors; another consideration is that the voltage reference that the source should follow is variable and dependent on the results of the optimization, as explained in 8.1.1. The main reason was related to the output waveform: with low modulation indexes implementing a carrier based modulation the NPC converter is not efficiently used and the output harmonics become high (filter impedance must be increased). The lower voltage limit is fixed to $Vdc_{low} = 500$ in order to keep a certain margin from the voltage reversion on the capacitor that may occur approaching 0 $[V]$: if the capacitors are electrolytic this phenomena causes the failure of the component with possibility of explosions because of the high energy released by electrochemical reduction. Some hypothesis on the sources have to be made: in this thesis it has been considered that the voltage regulation occurs with a known time constant, settling time and overshoot according to chapter 8.2.2. The power that each source is able to deliver is known from measurements on the environment (like wind speed or solar irradiation or other factors). This power signal is now considered to be stochastic for the single-phase and three-phase converters. This is obviously dependent on the considered system, but in order to run a simulation with reasonable computational time a variation of $0.5[MW/s]$ is considered possible while theoretically it would be too high for rotating systems with an high inertia. The available power spectrum considered is depicted in figures 8.76 and 8.77. The three single-phase sources are considered to have: the same power available, a sampling time of 1 second and a signal noise-free.

In this simulation the capacitors value is the same of the previous chapter while the bandwidth of the Id and Iq loops has been decreased to $750[rad/sec]$ in order to avoid possible unstable operations considering that the voltage balancing operation is due to the DC source. The sampling time has been fixed to $1e-5[sec]$ (lower than the one used

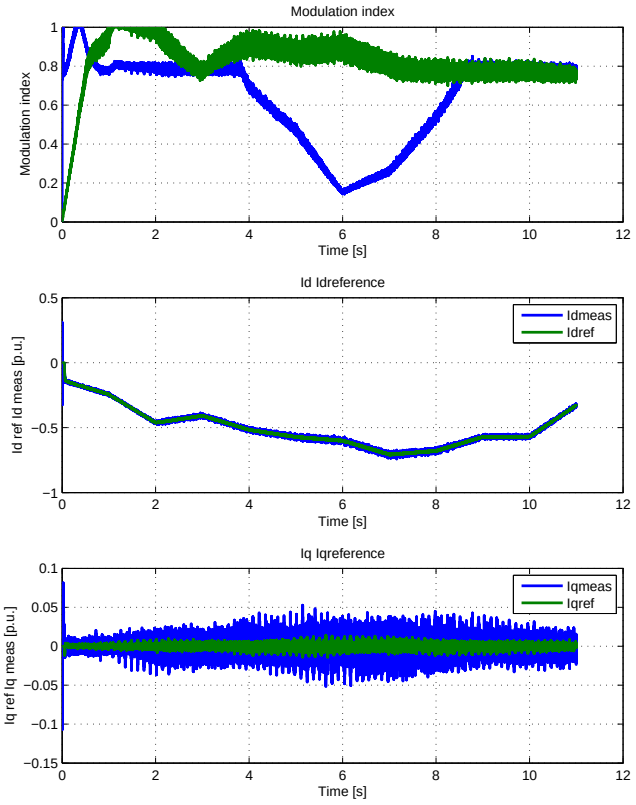


Figure 8.78: Control signals: three-phase modulation index, Id and Iq.

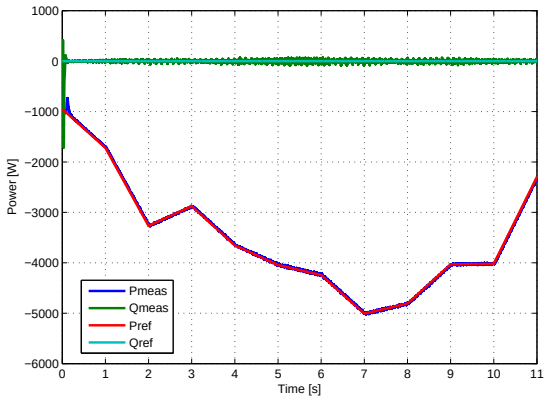


Figure 8.79: Active and reactive powers delivered to the grid.

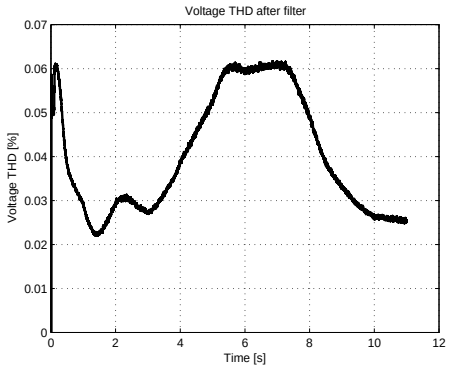


Figure 8.80: Voltage THD after filter.

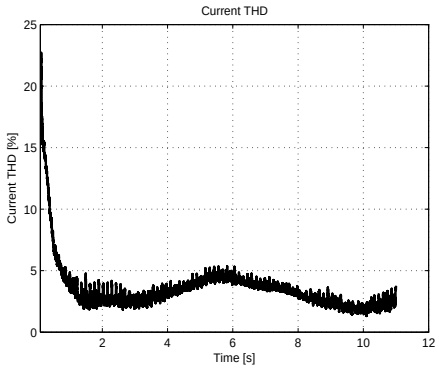


Figure 8.81: Grid-side current THD.

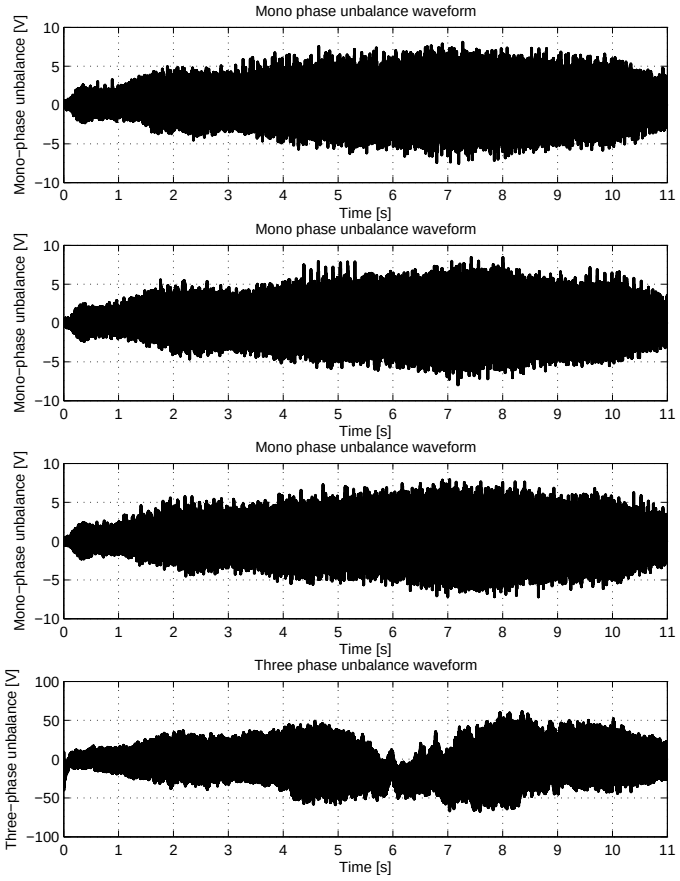


Figure 8.82: Unbalance waveform of the single and three-phase DC buses.

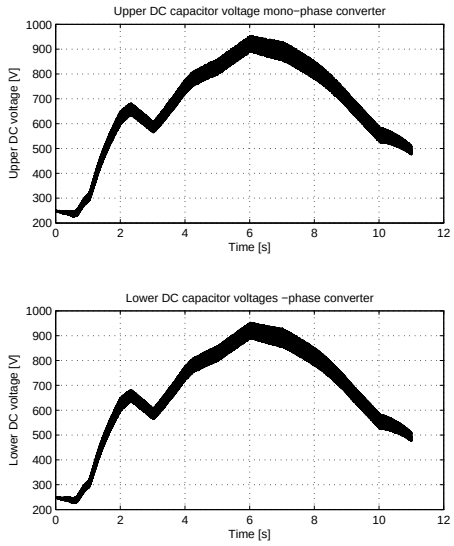


Figure 8.83: Single-phase converter DC upper and lower capacitor voltage.

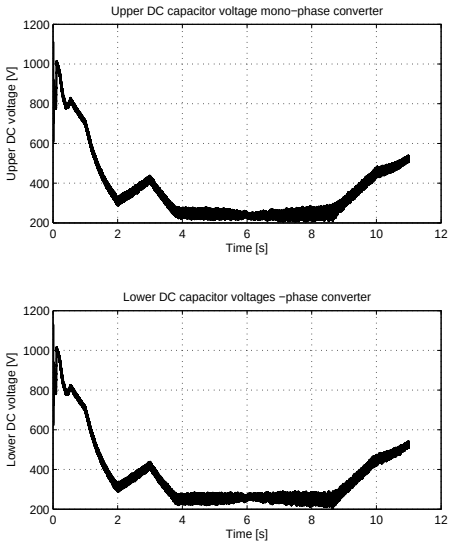


Figure 8.84: Three-phase converter DC upper and lower capacitor voltage.

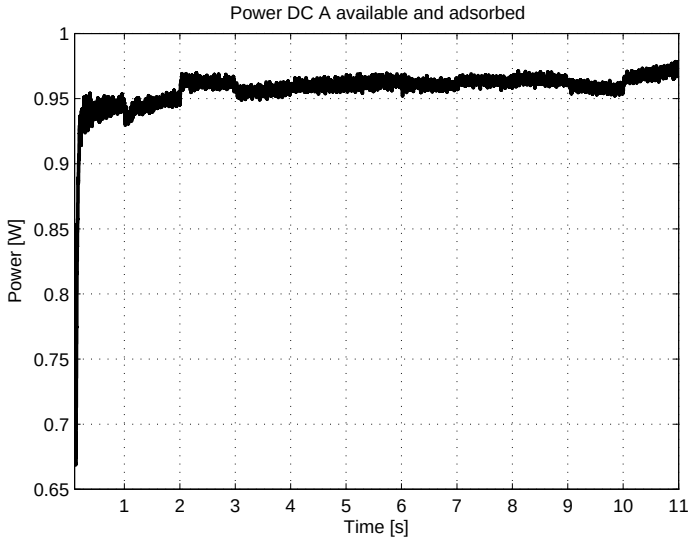


Figure 8.85: Efficiency calculated as ratio between the power delivered to the grid and the power adsorbed by the DC link.

with the previous simulations) in order to reduce computational costs and simulation time. In figure 8.76 and 8.77 the available powers and the adsorbed powers are depicted. There is a slight gap between these values; this is due to the power losses associated to the harmonics that have not been considered in the optimizer algorithm. These power losses are higher when only one converter is operating (three-phase). To keep into account these losses the power reference must be decreased, otherwise the capacitor voltage will decrease even if the DC source is delivering the maximum power. In this first simulation a coefficient 0.96 has been used to keep into account these additional losses. The disadvantage is a reduction of the efficiency when the THD becomes low (and the power associated to the harmonics becomes high). A better solution could be to use a PI that decrease the power reference: even if the loop is non-linear, this regulator only contributes with a low percentage ($< 5\%$ for example) and therefore the loop stability shouldn't affect the operation of the converter. In figure 8.78 the three-phase modulation index, Id and Iq reference are depicted. Figure 8.79 shows the total active and reactive power delivered to the grid. Figure 8.80 shows the voltage THD measured after the filter impedance: apart from the initial transient, it is visible that when the power produced by the three-phase converter is low in comparison with the one produced by the single-phases converters the THD becomes high. This is obtained because the converters are working far from the optimal condition introduced in chapter 7. The current THD waveform in figure 8.81 has the same shape.
In figure 8.82 the balancing waveforms are depicted: the single-phase DC links remain well balanced as the three-phase. A small unbalance is shown when the power produced by the three-phase source is low: in fact in this case the output voltage is also low and therefore the balancing algorithm is weaker.
In figures 8.83 and 8.84 the DC voltages for single and three-phase sources are depicted: the reference value changes according to the output voltage that the converter has to apply in order to keep the modulation index high. The lower value of 500 $[V]$ is reached by the three-phase converter when the power produced is low. Finally the conversion efficiency is depicted, calculated as the ratio between the global power delivered to the grid and the power that all the DC sources are able to deliver. Thus this efficiency considers all the resistive elements and the used coefficient to take into account the reductive effect due to the harmonics power losses, but it neglects the power electronic losses.
The introduction of a reduction coefficient is a method that works but introduces limitations on the efficiency, especially when both the converters are operating and the THD is low. A more precise solution is obtained measuring in each instant the power losses associated to the harmonics different from the fundamental; this process requires a more complex measuring system but the efficiency would be higher. The losses due to the harmonics when the current and voltage harmonics are known are:

$$P_{harm} = 3 \cdot R_{pu} \cdot Z_{base} \cdot \sum_{n=2}^{\infty} I_n^2 \tag{8.32}$$

where I_n is the n^{th} harmonic. If this calculation is executed in the grid side, the zero sequence losses should be taken into account because there is no zero sequence current

in the DC side with the adopted network model:

$$P_{zero} = 3 \cdot (2 \cdot R_{ZSBT} + R_0) \cdot I_0^2 = 3 \cdot (2 \cdot R_{ZSBT} + R_0) \cdot \sum_{n=3,9,15...}^{\infty} I_n^2 \tag{8.33}$$

where R_0 is the zero sequence resistance offered by the transformer and R_{ZSBT} the resistance offered by the zero sequence blocking transformer. The last contribute that must be considered is due to the harmonic injection into the line:

$$P_{line} = 3 \cdot \sum_{n=2}^{\infty} V_n \cdot I_n \cdot \cos(\phi_n) \tag{8.34}$$

where V_n and I_n are the measured phase to ground voltage harmonics and current harmonics and ϕ_n is the n^{th} power factor. Additional losses should be considered because high frequency harmonics introduce losses into the magnetic elements with an iron core as the power transformer and the ZSBTs. Because of the complexity of the measurements an easier choice is to use the method based on the adjustment of the power reference value already presented. The control variable is the DC capacitor voltage: if this voltage is decreasing in comparison with the reference value, the power coefficient should be decreased and vice-versa. Since the delay of the source has been modelled, these regulators help the capacitor voltage regulation, reducing the power reference when the capacitor should be charged. The chosen controller is a simple proportional with limited output in the range $(+0.01\% \ -0.05\%)$. As already explained the variation of the power is kept low because the power reference result by the optimizer is near to the right one, neglecting the harmonic and balancing losses and therefore the system stability is not compromised by the action of this regulator (the transfer function would be difficult to be studied).
In figures 8.86 and 8.87 the modulation indexes are depicted for the simulation with constant reduction coefficient and with regulated reduction coefficient. From the plots the PI regulation helps the voltage regulation action controlled by the source. The efficiency is also affected as shown in figures 8.88 and 8.89; the conversion efficiency considers the resistive losses in the transformer, ZSBTs and filter impedance neglecting the power electronic losses; the real efficiency keep into account the ratio between the power delivered and the deliverable power, known from envirormental measurements. Because of the capacitive storage the real efficiency could be higher than the conversion efficiency.

In figures 8.90 and 8.91 the power reduction coefficients are depicted: as shown the single-phase controller saturates to the lower limit since a simple proportional has been used. The PI should be tuned when the typical power production curve of the DC sources is known. Setting the integral part and the output limits of this regulator the converter operation can be optimized.

8.4 Power electronics efficiency estimation

It is interesting to evaluate the conversion efficiency due to the power electronics conversion. In order to compute this efficiency through the simulations the PWM block must

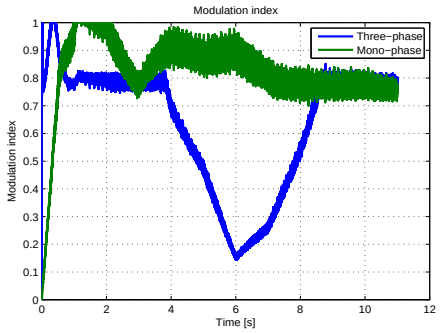


Figure 8.86: Modulation indexes with power reduction coefficient.

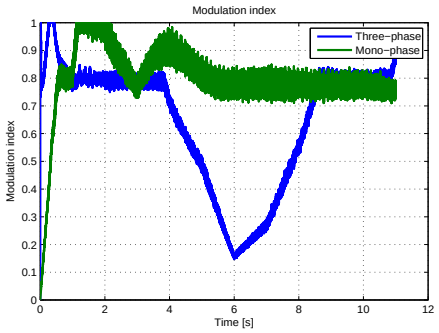


Figure 8.87: Modulation indexes with controlled power reduction.

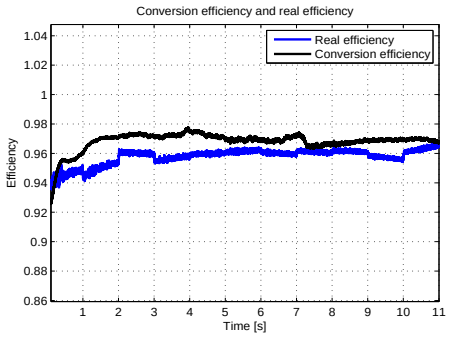


Figure 8.88: Efficiency with power reduction coefficient.

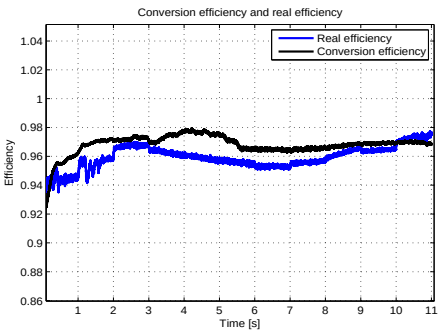


Figure 8.89: Efficiency with controlled power reduction.

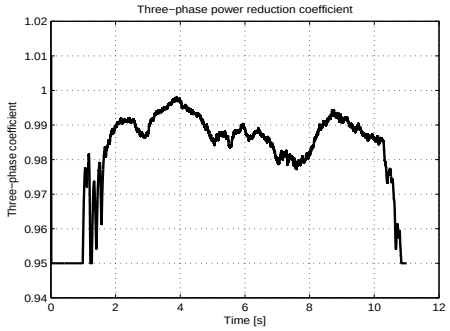


Figure 8.90: Three-phase power reduction coefficient with the PI controller.

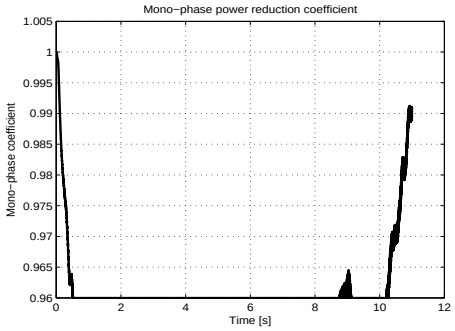


Figure 8.91: single-phase power reduction coefficient with the PI controller.

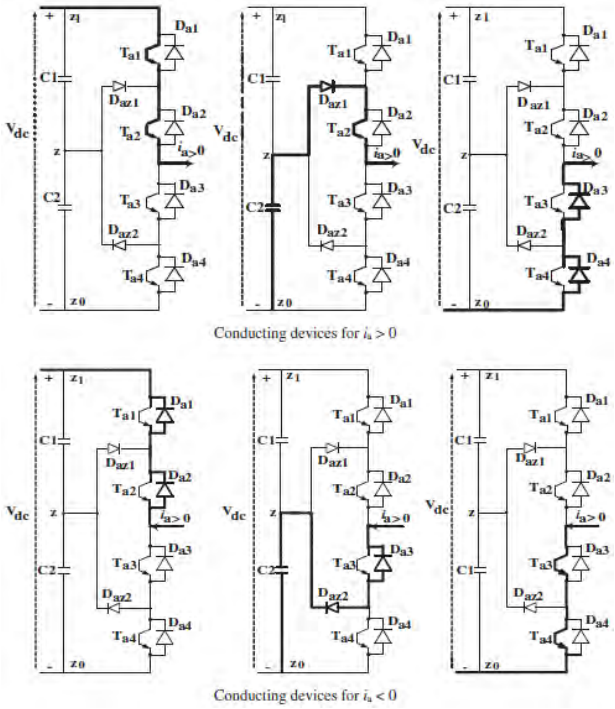


Figure 8.92: Current direction in one leg of three-level converter.

be modified because the $IGBT$ block fails the switch-on operation of the converter (this will be part of the future work to be developed). The solution is therefore to compute analytically the converters losses knowing that this result won't be far from the real one. In [36] an analytical method is proposed to compute the efficiency of two-levels and three-levels NPC converters that is useful in the studied case. The forward voltage V_f of each switch is:

$$V_f = V_{f0} + r_f \cdot i \tag{8.35}$$

where V_{f0} is the collector-emitter voltage, r_f is the conduction resistance and i is the current that flows through the device. The losses are computed as:

$$Pc = V_f \cdot I_{avg} + r_f \cdot I_{rms1}^2 \tag{8.36}$$

where I_{avg} and I_{rms} are the average and RMS currents flowing through the device. In figure 8.92 the current path is shown in one leg of the three-level NPC converter; as explained in [36] with some considerations on the duty cycles of the switches the expressions of average and RMS current for each IGBT and diode are computed and here reported:

$$I_{Ta1,avg} = I_{Ta4,avg} = \frac{M \cdot Im}{4\pi}[(\pi - \theta)\cos\theta + \sin\theta] \tag{8.37}$$

$$I_{Ta2,avg} = I_{Ta3,avg} = \frac{Im}{4\pi}[4 + \theta \cdot M \cdot \cos\theta - M\sin\theta] \tag{8.38}$$

$Switch$	$Iavg\ [A]$	$Irms^2\ [A^2]$
$T1, T4$	556.8	$1.336 \cdot 10^6$
$T2, T3$	900	$2 \cdot 10^6$
$D1, D2, D3, D4$	0.35	266
$Daz1, Daz2$	343	$663 \cdot 10^3$

Table 8.4: Devices currents.

$Parameter$	$Value$	$Unit$
$V_{CE,igbt}$	1.6	$[V]$
$R_{CE,igbt}$	0.555	$[m\Omega]$
$E_{on+off,igbt}$	1.5	$[J]$
$V_{CE,diode}$	1.2	$[V]$
$R_{CE,diode}$	0.42	$[m\Omega]$

Table 8.5: Data-sheet parameters.

$$I^2_{Ta1,rms} = I^2_{Ta4,rms} = \frac{M \cdot Im^2}{12\pi}[3 + 4\cos\theta + \cos(2\theta)] \tag{8.39}$$

$$I^2_{Ta2,rms} = I^2_{Ta3,rms} = \frac{Im^2}{12\pi}[3(\pi - M) + 4M\cos\theta - M\cos(2\theta)] \tag{8.40}$$

$$I_{Da1,avg} = I_{Da2,avg} = I_{Da3,avg} = I_{Da4,avg} = \frac{M \cdot Im}{4\pi}[\theta \cdot \cos\theta - \sin\theta] \tag{8.41}$$

$$I^2_{Da1,rms} = I^2_{Da2,rms} = I^2_{Da3,rms} = I^2_{Da4,rms} = \frac{M \cdot Im^2}{4\pi}[3 - 4\cos\theta + \cos(2\theta)] \tag{8.42}$$

$$I_{Daz1,avg} = I_{Daz2,avg} = \frac{Im}{\pi} - \frac{M \cdot Im}{4\pi}[(\pi - 2\theta)\cos\theta + 2\sin\theta] \tag{8.43}$$

$$I^2_{Daz1,rms} = I^2_{Daz2,rms} = \frac{Im^2}{12\pi}[3\pi - 6M - 2M\cos(2\theta)] \tag{8.44}$$

where M is the modulation index, Im is the peak current, θ is the power factor. Assuming a constant $M = 0.8$ and $\phi = 0.18\ [rad]$ near to the condition $\cos\phi = 1$ an estimation the converters efficiency is possible. The first condition that is worth to be considered is the maximum power point, where the converters should present the highest power losses. The current that flows trough the devices is $Im = \sqrt{2} \cdot 2000 = 2828\ [A]$. The average and RMS currents in the switches are reported in table 8.4.

To estimate the converter efficiency the devices must be chosen in order to extract the needed data from the data-sheet. The components that have been selected are the IGBT $FZ3600R17KE3_B2$ and the diodes $FD5000AV - 100DA$. The data-sheets can be found in [37, 38] respectively. The parameters reported in 8.5 are found considering $Im = 2828\ [A]$ and a low junction temperature ($25°\ C$). The devices losses are represented in

Device	*Powerlosses*	*Unit*
$T1, T4$	1.63	$[kW]$
$T2, T3$	2.55	$[kW]$
$D1...D4$	0.53	$[W]$
$Daz1, Daz2$	690	$[W]$

Table 8.6: Devices losses.

8.6.

The total power losses due to conduction in each leg are:

$$P_{cond} = 2 \cdot P_{T1} + 2 \cdot P_{T2} + 4 \cdot P_{D1} = 9.74 \ [kW]. \tag{8.45}$$

The total power losses due to the switching operation in the hypothesis of equal sharing between the devices are:

$$P_{sw} = f \cdot E_{on+off} \cdot 4 = 9 \ [kW] \tag{8.46}$$

Considering that globally the converter is built with twelve legs, the total power losses are:

$$P_{tot} = 12 \cdot (P_{cond} + P_{sw}) = 12 \cdot (9 + 9.74) = 224.88 \ [kW]. \tag{8.47}$$

This power value is important because it is the reference value that should be used to design the converters cooling system since it is also the maximum value that can be obtained with these parameters. The efficiency approximating the delivered power to 7 $[MW]$ is:

$$\eta_{converter} = \frac{7000}{7000 + 224.88} = 96.89\%. \tag{8.48}$$

In figures 8.88 and 8.89 the conversion efficiency and real efficiency were depicted considering the switches to be ideal. The conversion efficiency was approximatively $\eta = 0.97$ and therefore a rough estimation could consider $\eta_{converter}$ to be constant and an overall efficiency of $\eta_{tot} = \eta \cdot \eta_{converter} = 0.94$. These results have been computed starting from the initial over-estimation of the parameters of the magnetic elements (filter, transformer and ZSBTs) and therefore it must also be validated with the effective component sizing. Practically this efficiency estimation is a lower under-estimated limit since the effective resistances will be lower than the ones used in the simulation and also an high switching frequency has been chosen.

Chapter 9

Magnetic components sizing

9.1 Power transformer

9.1.1 Design

In this chapter some consideration on the power transformer design are made. Since the zero sequence impedance of the transformer depends on how it is built and especially on the external tank, a simplified design of the machine is presented in order to study the positive sequence impedance and to verify if the assumptions made in chapter 4 are correct or need to be fixed.
As already explained the secondary three-phase winding of the transformer is connected with wye with accessible neutral configuration, in order to allow the grounding of the neutral point if the distribution system require it. In this case the zero sequence current that flows in the primary winding is reported to the secondary since no delta winding are present. Some considerations are also worth to be done on the power losses of this transformer and the possibility to build a tertiary winding if the star connection in the grid side is adopted in order to stabilize the neutral point voltage if single-phase loads on the grid are present and to avoid the zero sequence current injection in the grid side [39].
In this thesis the transformer with the parameters depicted in table 9.1 will be considered. This is obviously an example, these parameters have to be adapted to the studied case and

$Parameter$	$Value$	$Unit$
$V1$	2000	$[V]$
$V2$	1000	$[V]$
S_n	7	$[MVA]$
f	60	$[Hz]$
$Connection$	$open - Yn$	[]

Table 9.1: Transformer parameters.

the design procedure may be the same adopted in this chapter. The first consideration concerns the voltage level: this topology would work in a better way if the grid side is at medium voltage level (10 $[kV]$ for example) decreasing the size of the conductors and the power losses even if the higher voltage level require more expensive systems. Even if in this case the transformer ratio is low the solution of using an auto-transformer (with 50% of the total power transferred by the magnetic coupling) is not feasible because the primary winding must be in an open end configuration and because it would present a lower inductance. Therefore the electric machine type that have been chosen is an oil cooled three-phase transformer.
The design starts with the magnetic flux:

$$\Phi = 1.35 \cdot 10^{-2} \cdot \sqrt{\frac{S_n[kVA]}{f}} = 0.146\ [Wb] \tag{9.1}$$

The magnetic field in the iron core is fixed to 1.8 $[T]$. The iron core section is:

$$A_{fe} = 1.2 \cdot \frac{\Phi}{B} = 1.2 \cdot \frac{0.146}{1.8} \simeq 97333\ [mm^2] \tag{9.2}$$

and the voltage induced in each turn is:

$$E_t = \sqrt{2} \cdot \pi \cdot f \cdot \Phi = 4.44 \cdot 60 \cdot 0.146 = 38.89\ [V]. \tag{9.3}$$

The number of turns required in the secondary winding is:

$$N_2 = \frac{1000}{\sqrt{3} \cdot E_t} = \frac{1000}{\sqrt{3} \cdot 38.89} = 14.86. \tag{9.4}$$

The selected number of turns is 15 and the updated flux becomes:

$$\Phi = \frac{E_t'}{4.44 \cdot \Phi} = \frac{1000}{\sqrt{3} \cdot 15 \cdot 4.44 \cdot 60} = 0.1445\ [Wb]. \tag{9.5}$$

The updated iron section is therefore $A_{fe} = 96300\ [mm^2]$, the turn-voltage is $E_t' = 38.49\ [V]$ and the diameter of the iron core is:

$$D = \sqrt{\frac{4 \cdot A_{fe}}{\pi}} = \sqrt{\frac{4 \cdot 96300}{\pi}} = 350\ [mm]. \tag{9.6}$$

The first designed winding is the low voltage coil that will be internally placed:

$$I = \frac{S_n}{\sqrt{3} \cdot V1} = \frac{7000}{\sqrt{3} \cdot 1000} = 4041.5\ [A] \tag{9.7}$$

and using a current density of $J = 3.3\ [A/mm^2]$ the required copper section is:

$$Scu_2 = \frac{I_2}{J} = \frac{4041.5}{3.3} = 1225\ [mm^2]. \tag{9.8}$$

The "electric load" defined for transformer uses the following expression for an oil cooled transformer:

$$k_2 = \frac{N_2 \cdot I_2}{h} = (200 \div 250) \cdot 10^3 \sqrt{\Phi} = 250 \cdot 10^3 \cdot \sqrt{0.1445} = 95000 \ [A/m] \tag{9.9}$$

where h is the height of the coil that results $h = 640$ $[mm]$. A disposition of the conductors in four columns is chosen and therefore each turn has an height $h_t = 160$ $[mm]$ and an approximated width $w_t = \frac{1225}{160} = 7.65$ $[mm]$. The conductor chosen is made of 16×2 smaller conductors with rectangular shape 10×4 $[mm^2]$. Considering a paper insulation of 0.2 $[mm]$, the overall size of one turn is 166.4×8.8 $[mm^2]$. The total copper winding column has a size equal to 678×8.8 $[mm^2]$ considering also to wound the coil with conductor transposition.
The single conductor copper section is $S_{cu} = 39.14$ $[mm^2]$ and therefore the total copper section of one turn is $S_{tot} = 16 \cdot 2 \cdot 39.14 = 1252.5$ $[mm^2]$. The real current density obtained is $J_{real} = \frac{I_{tot}}{S_{tot}} = 3.23$ $[\frac{A}{mm^2}]$.
Because of the heat exchange the coil is placed 6 $[mm]$ above the iron core, in order to leave enough space for the oil circulation. An illustration of the winding is reported in appendix B in figures B.1 and B.2.
The lower voltage coil has been completely defined; the weight and the losses may therefore be computed:

$$G_{cu} = \gamma\pi \cdot Dm \cdot S_{tot} \cdot N2 = 8900\pi(350+(6+8.8+3)\cdot 2)\cdot 1252.5 \cdot 15 \cdot 10^{-9} = 218.1 \ [kg] \tag{9.10}$$

considering the specific copper weight to be $\gamma = 8900$ $[kg/m^3]$. Since the conductors are immersed in a magnetic field the current distribution will be non-uniform and with an empirical formula the increasing coefficient has been estimated $k_r = 1.2$. The total power loss is therefore:

$$P_{cu} = \frac{\rho}{\gamma} \cdot J^2 \cdot G_{cu} \cdot k_r = 2.35 \cdot 3.23^2 \cdot 218.1 \cdot 1.2 = 6417 \ [W] \tag{9.11}$$

The total resistance of the winding is $R1 = P_{cu}/I^2 = 0.393$ $[m\Omega]$. To verify thermally the coil a simplified formula may be used considering that the oil heat exchange coefficient is $\alpha_o = 80$ $[W/m^2K]$:

$$\theta = \frac{P_{cu}}{\alpha \cdot \pi \cdot Dm \cdot 8 \cdot h \cdot \xi} = \frac{6417}{\pi 80 \cdot 415.2 \cdot 8 \cdot 678 \cdot 0.75 \cdot 10^{-6}} = 15.35 \ [^\circ C] \tag{9.12}$$

where ξ considers the reduced convection surface because of the coil sustaining cardboard. θ represents the copper-oil temperature gap, that should be less than 20 $[K]$.
The same procedure can be followed for the higher voltage coil. The voltage applied by the converters with the open end-winding configuration is applied on the entire winding and therefore it is the same to have a wye connected primary winding. The number of turns is:

$$N1 = \frac{V1}{\sqrt{3} \cdot Es'} = \frac{2000}{\sqrt{3} \cdot 38.49} = 30. \tag{9.13}$$

The selected number of turns is 29 because for design reasons it is easier to built a coil with an odd number of turns. The real voltage is $V1 = E_t \cdot N1 = 1933$ $[V]$ and the current is:

$$I = \frac{S_n}{\sqrt{3} \cdot V1} = \frac{7000}{\sqrt{3} \cdot 1933} = 2090.4 \ [A]. \tag{9.14}$$

The current density is chosen $J = 3.88$ $[A/mm^2]$, higher than the one used in the inner coils because the heat exchange is better for the external coil. In these hypothesis the required copper section becomes $S_{cu} = 538.76$ $[mm^2]$. This time the conductors are displaced in three columns because of the simplicity of this pattern; all the six terminals must be accessible from outside.
The height of each wire turn is $h_t = 678/10 = 67.8$ $[mm]$ and the width is $s_t = 7.95$ $[mm]$. In this case the conductor is chosen to be composed of 8×2 rectangular conductors in parallel with size $8.5 \times 4[mm]$. Considering the same paper insulation, the global size of one column becomes $712 \times 8.8[mm^2]$.
The copper section is $33.14 \cdot 16 = 530.24$ $[mm^2]$ and the real current density is therefore $J = 3.94$ $[A/mm^2]$.
Regarding the coil positioning, a certain gap must be considered between the low and high voltage coil; the length of this gap will affect the leakage inductance of the transformer. Since a filter impedance must be used the higher leakage inductance the lower filter need to be used. A gap of $15[mm]$ is considered, enough for thermal exchange purposes. The distance between the coils is fixed to be 6 $[mm]$, the minimum required for a good thermal exchange. In appendixes B.1 and B.2 the structure is depicted.
The medium diameter of the high voltage coil is:

$$Dm = 350 + (6 + 53.2 + 15 + 8.8 + 6 + 8.8/2) \cdot 2 = 536.8 \ [mm] \tag{9.15}$$

The copper weight is:

$$G_{cu} = \gamma\pi \cdot Dm \cdot S_{tot} \cdot N2 = 8900\pi(536.8) \cdot 530.24 \cdot 29 \cdot 10^{-9} = 231 \ [kg] \tag{9.16}$$

and the power losses considering the same coefficient for the unequal current distribution are:

$$P_{cu} = \frac{\rho}{\gamma} \cdot J^2 \cdot G_{cu} \cdot k_r = 2.35 \cdot 3.88^2 \cdot 231 \cdot 1.2 = 9806 \ [W]. \tag{9.17}$$

The phase resistance is $R = P_{cu}/I^2 = 2.24$ $[m\Omega]$. Again the thermal check may be verified:

$$\theta = \frac{P_{cu}}{\alpha \cdot \pi \cdot Dm \cdot 8 \cdot h \cdot \xi} = \frac{9806}{\pi 80 \cdot 536.8 \cdot 6 \cdot 712 \cdot 0.85 \cdot 10^{-6}} = 20 \ [^\circ C] \tag{9.18}$$

where $\xi = 0.85$ is bigger than the one used for the inner coil because the outer coil has one free surface that means an improved thermal exchange. The temperature is equal to

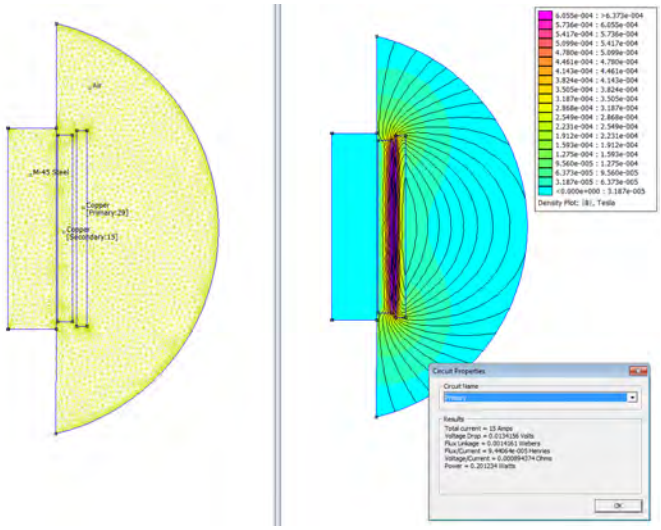


Figure 9.1: Leakage inductance calculation through FEM software.

the limit of 20 [$°C$]. The leakage impedance is evaluated with the following formula:

$$\begin{aligned} X &= 1.06 \cdot \omega \cdot \mu_0 \cdot N1^2 \cdot \frac{\pi \cdot Dm}{h} \cdot \left(\frac{s1}{3} + s2 + \frac{s3}{3} \right) \\ &= 1.06 \cdot 4 \cdot \pi \cdot 10^{-6} \cdot 2 \cdot \pi \cdot 60 \cdot \frac{29 \cdot \pi \cdot 0.483}{0.712} \cdot \left(\frac{53.2}{3} + 15 + \frac{38.4}{3} \right) \\ &= 41.02 \ [m\Omega] \end{aligned} \tag{9.19}$$

To verify this calculated inductance a FEMM axisymmetric model of one transformer phase can be built. From figure 9.1 the inductance results $L = 9.44 \cdot 10^{-}5$ $[H]$ and therefore the impedance is: $X = \omega L = 2 \cdot \pi \cdot 60 = 36.6$ $[m\Omega]$, similar to the one theoretically calculated.

The percentage quantities are:

$$Xcc_{\%} = X \cdot \frac{I1}{V1} = 41.02 \cdot \frac{2090.4}{1933} = 4.44 \ \% \tag{9.20}$$

$$Rcc_{\%} = \cdot \frac{P_{cu}}{S_n} = \frac{3 \cdot (6.417 + 9.806)}{7000} = 0.695 \ \% \tag{9.21}$$

All the parameters are known now and therefore the dimensions of the magnetic core and of the external tank may be found.
The distance between two high voltage windings is fixed to 20 $[mm]$. The external diameter of each winding is $D = 575.2$ $[mm]$, therefore the distance between each phase axis is $i = 592.5$ $[mm]$. A distance of 10 $[mm]$ between the coils and the horizontal yokes is also considered. The height of the central column is $hc = 712 + 20 = 732$ $[mm]$,

while the length of the two lateral columns is $hl = hc + 2 \cdot i + 350 = 2272.4$ $[mm]$. The total height of the core is $h_{tot} = 1432$ $[mm]$ while the width is $l_{gg} = 1540.4$ $[mm]$. The magnetic core is depicted in appendix B.3.
The total volume and weight of the magnetic core is:

$$Vol_{fe} = 3 \cdot h_c \cdot A_{fe} + 2 \cdot l_{gg} \cdot A_{fe} = (3 \cdot 732 \cdot 96300 + 2 \cdot 1540.4 \cdot 96300) \cdot 10^{-9} = 0.5082 \ [m^3] \tag{9.22}$$

$$G_{fe} = \gamma_{fe} \cdot Vol_{fe} = 7650 \cdot 0.5082 = 3890 \ [kg] \tag{9.23}$$

considering the specific iron weight equal to $\gamma = 7650$ $[kg/m^3]$. The magnetic field inside the core was fixed to 1.8 $[T]$. Considering grain-oriented steels, the power losses at $60[Hz]$ with a lamination thickness of 0.3 $[mm]$ is 1.45 $[W/kg]$ considering $30JGH110$ steel with $f = 60$ $[Hz]$ and $B = 1.8$ $[T]$. Considering an increasing coefficient due to the material manufacturing and cutting $k = 1.2$, the total iron losses are:

$$P_{fe} = k \cdot 1.45 \cdot G_{fe} = 1.45 \cdot 1.2 \cdot 3890 = 6770 \ [W] \tag{9.24}$$

The total efficiency without considering the effect of the harmonics at the maximum current is:

$$\eta = \frac{S_n}{S_n + 3 \cdot (Pcu1 + Pcu2) + P_{fe}} = \frac{7000}{7000 + 6.77 + 3 \cdot (9.806 + 6.417)} = 0.992. \tag{9.25}$$

The magnetizing current may be computed since all the informations on the transformer are known: the last parameter to consider is the thickness of the air gap between the iron yokes. An equivalent length $t = 0.04$ $[mm]$ is considered. The required magneto-motive force for these gaps is:

$$H \cdot t_{eq} = \frac{B}{\mu_0} = \frac{1.8}{\mu_0} \cdot 0.04 \cdot 10^{-3} = 57.3 \ [A] \tag{9.26}$$

while the magneto-motive force required to magnetize the iron core is:

$$H_{fe} \cdot hl = 120 \cdot 2.272 = 273 \ [A]. \tag{9.27}$$

The overall reactive current required to magnetize the core is (with H found in the material data-sheet):

$$I_\mu = \frac{H_{fe} \cdot t_{eq} + 2 \cdot H \cdot t}{N1} = \frac{273 + 2 \cdot 57.3}{29} = 13.37 \ [A] \tag{9.28}$$

while the active component can be found:

$$Ia = \frac{P_{fe}}{3 \cdot E1} = \frac{6770}{\sqrt{3} \cdot 2000} = 1.95 \ [A]. \tag{9.29}$$

The total magnetizing current is therefore:

$$I0 = \sqrt{Ia^2 + I_\mu^2} = \sqrt{1.95^2 + 13.37^2} = 13.51 \ [A] \tag{9.30}$$

$Parameter$	$Value$	$Unit$
R_{pu}	1.3%	$[p.u.]$
X_{pu}	6%	$[p.u.]$
$R0$	200	$[p.u.]$
$X0$	200	$[p.u]$

Table 9.2: Transformer parameters used in the simulations.

with $I0\% = 0.64\%$. The percentage shunt parameters are therefore:

$$R0 + jX0 = \frac{E}{Ia} + j \cdot \frac{E}{I_\mu} = \frac{2000}{\sqrt{3} \cdot 1.95} + j\frac{2000}{\sqrt{3} \cdot 13.37} = 592 + j86.36 \ [\Omega] \tag{9.31}$$

The base impedance calculated in chapter 4 was $Z_b = 0.1429$ $[\Omega]$ on the grid side and $Z_b' = 4 \cdot Z_b = 4 \cdot 0.1429 = 0.5714$ $[\Omega]$ on the converter side. It is therefore possible to compute the p.u. values of $Rcc, Xcc, R0, X0$ that have been previously estimated.

$$R_{p.u.} = Rcc_{\%} = 0.695\% \ p.u. \tag{9.32}$$

$$X_{p.u.} = Xcc_{\%} = 4.44\% \ p.u. \tag{9.33}$$

$$R0_{p.u.} = \frac{R0}{Z_b} = 1036 \ p.u. \tag{9.34}$$

$$X0_{p.u.} = \frac{X0}{Z_b} = 151.1 \ p.u. \tag{9.35}$$

The parameters used in the simulations are reported in table 9.2. All the parameters were overestimated, especially the resistances and therefore the efficiency obtained in the simulations is lower than the expected one. In order to obtain the same THD resulted in the simulations the inductance of the filter impedance should be increased till the same total reactive impedance is obtained.

The external tank can be simply modelled with a rectangular shape; the chosen height is $h = 1762$ $[mm]$, keeping the transformer 30 $[cm]$ above the bottom of the tank (for sedimentation deposit) and 300 $[mm]$ below the top of the tank. The width is $w = 1685$ $[mm]$ and the depth is $d = 685$ $[mm]$. The material used for the oil tank is mild steel non laminated with a thickness of 6 $[mm]$. The tank is depicted in appendix B.4.

9.1.2 Additional losses

The design of the transformer in the previous chapter is simple and only considers the case of sinusoidal quantities. The voltage harmonics according to [40] affect the no load power losses and the no load current waveform (which is distorted already distorted because of the magnetic core saturation). The additional losses introduced are normally neglected when the voltage THD is below 5%. In the studied case the filter is placed

after the transformer and therefore the THD seen by the transformer is only limited by the $ZSBTs$. As shown in figures 9.2 and 9.3 the THD of the voltage applied to the primary phase transformer is grater than 5% and is variable during the simulation because the interleaving is more effective when the optimal power condition is reached. The power losses without load may be expressed with Steinmez's relation:

$$P = k_{hysteresis} \cdot \left(\frac{f}{60}\right)\left(\frac{B}{B_{ref}}\right)^2 + k_{eddy} \cdot \left(\frac{f}{60}\right)^2\left(\frac{B}{B_{ref}}\right)^2 \tag{9.36}$$

where the coefficients are normally:

$$\begin{cases} k_{hysteresis} = 70\% \cdot P_{specific} = 0.7 \cdot 1.45 = 1.015\ [\frac{W}{kg}] \\ k_{eddy} = 30\% \cdot P_{specific} = 0.3 \cdot 1.45 = 0.435\ [\frac{W}{kg}]. \end{cases} \tag{9.37}$$

Writing the inductor equation the link between the voltage and the flux is known:

$$v = \frac{d\Phi_T}{dt} = \frac{N \cdot d\Phi}{dt} = N \cdot \omega \cdot \Phi \ \rightarrow \ \Phi = \frac{v}{N \cdot \omega} \tag{9.38}$$

assuming that the effects overlapping principle may be applied. The additional power losses due to the voltage harmonics may be estimated approximatively as:

$$\begin{aligned} P = \sum_{n=2}^{n=\infty} k_{hysteresis} \cdot \left(\frac{1}{60}\right)\left(\frac{v_n}{N \cdot 2 \cdot \pi \cdot n \cdot f \cdot S \cdot 1.8}\right)^2 + \\ + k_{eddy} \cdot \left(\frac{1}{60}\right)^2\left(\frac{v_n}{N \cdot 2 \cdot \pi \cdot S \cdot 1.8}\right)^2 \end{aligned} \tag{9.39}$$

where S is the iron core surface offered for the flux. It must be considered that increasing the frequency this section decreases because the penetration depth becomes lower. The penetration depth at a certain frequency is:

$$\delta = \sqrt{\frac{2}{\mu \cdot \mu_0 \cdot \omega \cdot \sigma}} \tag{9.40}$$

and therefore if the flux is considered to flow only in one penetration depth, the available surface S is:

$$S = \begin{cases} S & if\ d > \delta \\ S \cdot \frac{\delta}{d} & if\ d < \delta \end{cases} . \tag{9.41}$$

Applying equation 9.39 limiting the summation to the first harmonic family (see figure 9.2) the results in table 9.3 are obtained.

Considering the same core material of the previous chapter, the specific losses given by the manufacturer were quantified in $P_{specific} = 1.45\ [\frac{W}{kg}]$. The percentage increment of the losses due to the voltage harmonics is:

$$Padd_{\%} = \frac{P_{add}}{P_{specific}} \cdot 100 = +22.76\% \tag{9.42}$$

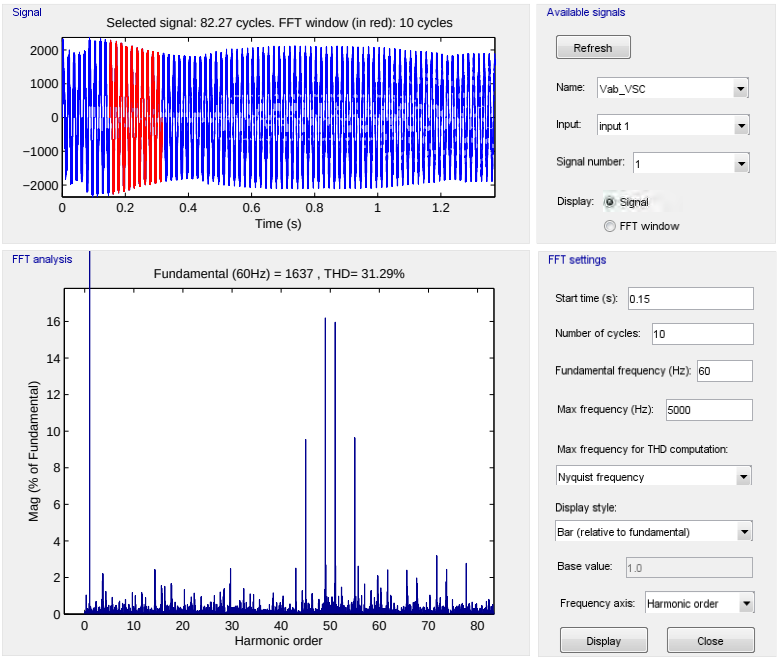


Figure 9.2: FFT analisys of primary winding voltage at $t = 0.15$ $[s]$.

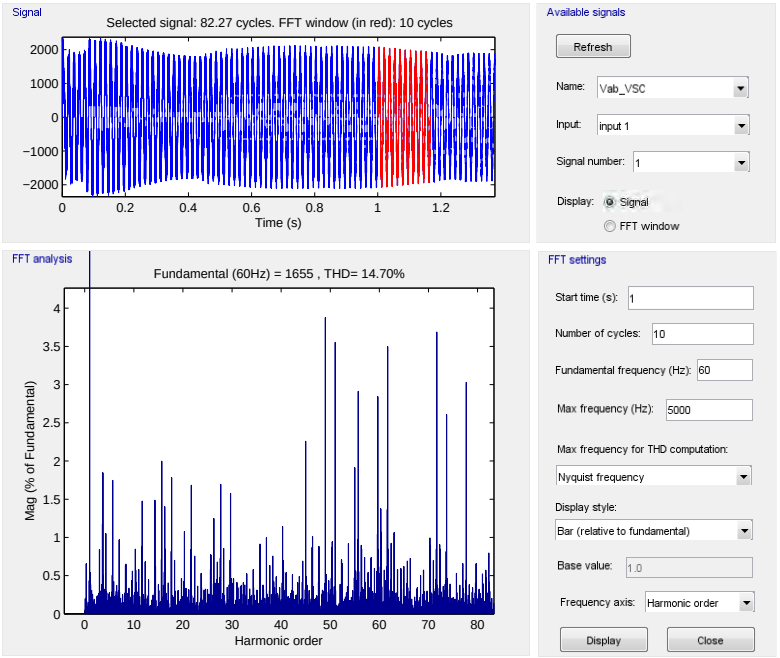


Figure 9.3: FFT analisys of primary winding voltage at $t = 1$ $[s]$.

$Parameter$	$Value$	$Unit$
$P_{hysteresis}$	$5,69 \cdot 10^{-6}$	$[\frac{W}{kg}]$
P_{eddy}	0.33	$[\frac{W}{kg}]$

Table 9.3: Transformer parameters.

The iron power losses, $R0$ and the efficiency of the transformer are therefore:

$$P_{fe} = k \cdot (1.45 + 0.33) \cdot G_{fe} = 1.78 \cdot 1.2 \cdot 3890 = 8310\ [W] \tag{9.43}$$

$$R0'_{p.u.} = \frac{V^2}{P_{fe} \cdot Zb} = \frac{2000^2}{8310 \cdot 0.5714} = \ 842[p.u.] \tag{9.44}$$

$$\eta' = \frac{7000}{7000 + 8.31 + 3 \cdot (9.806 + 6.417} = 0.99 \tag{9.45}$$

The resistance is still higher than the one used in the simulations; this means an higher efficiency with respect to the simulation.

9.1.3 Zero sequence impedance

Since the transformer used in the simulations has the wye-wye configuration the zero sequence current sees the impedance due to the external tank because all the flux lines are closed outside the magnetic core. An estimation of the zero sequence impedance has been done in order to model this transformer (and to run the simulations) and it would be interesting to verify if the value assumed is feasible. A temperature distribution evaluation inside the tank would also be interesting because the zero sequence current cause an increasing of the shell temperature that might be intolerable. If the temperature reached is too high it is necessary to modify the cooling system or to use a tertiary winding delta connected; it is worth to be discussed that the ZSBTs are useful to reduce the zero sequence current on the converter side but if a single-phase fault occurs on the grid side the zero sequence current is free to circulate into the transformer. Therefore an evaluation of the fault conditions is also necessary to choose if the tertiary winding is required.

9.2 ZSBTs

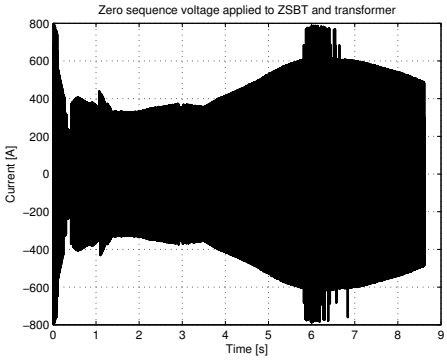
9.2.1 Introduction

As with the power transformer, in the simulations the parameters of the ZSBTs have been hypothesized and in this chapter these magnetic components will be designed in order to understand if the size and the weight obtained are excessive or acceptable.
In Simulink ® the *zero sequence coupled inductor module* has been used; the positive sequence and zero sequence values have been defined according to table 9.4. The zero

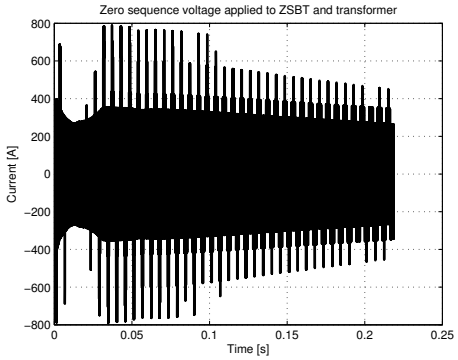
$Parameter$	$Value$	$Unit$
$R0$	1.4	$[m\Omega]$
$L0$	2.5	$[mH]$
$R_{+,-}$	1.4	$[m\Omega]$
$L_{+,-}$	$5 \cdot 10^{-7}$	$[H]$

Table 9.4: ZSBTs parameters.

sequence impedance is seen when a set of three zero sequence voltage sources is connected to the transformers; as explained in chapter 2.1.4 this impedance is related to the mutual coupling between the windings while the leakage inductance is related to the positive and negative sequence impedances. If ideally the coupling coefficient was $k = 1$, the positive and negative sequence inductance would be zero and the zero sequence inductance would be equal to the auto-inductance of one winding.
Theoretically it is enough to provide mutual coupling between the windings to obtain a ZSBT; practically the role of leakage inductances and the saturation of the magnetic circuits must be considered and the design problem becomes more complex.
An important consideration is worth to be reported: in the simulations that have been run all the parameters regarding the zero sequence impedance have been hypothesized and they are considered to be constant. In particular the saturation behaviour could be modelled through look-up tables and expressing the mathematical model of the inductor, but the frequency dependence cannot be included. Since all the magnetic elements like the transformer and the ZSBTs have a magnetic core with a certain thickness the model with constant parameters is no longer valid when the frequency becomes high and the penetration depth decreases below the sheets thickness. In order to obtain a reliable model of the entire system (positive,negative and zero sequences) it would be necessary to couple Simulink ® with finite element method (FEM) programs where the magnetic components are designed. At each time step the main circuit should be solved computing the resistances and inductances of the ZSBTs through the FEM software starting from the previous result with an iterative process. The computational cost would be therefore really high. The ZSBTs have the role to reduce the zero sequence currents and these currents will be low in comparison with the positive sequence currents and even if the parameters of the ZSBTs are considered to be constant the error committed will be negligible again in comparison with the positive sequence. When the ZSBTs must be designed a different way to proceed should be used because the positive and negative sequence are ideally exactly deleted, while the zero sequence current produces the flux. In the simulation with constant parameters the information that may be extract is the zero sequence voltage applied to the series ZSBT-transformer-ZSBT, depicted in figures 9.4a and 9.4b. Another circuit separated from the main circuit can be built and the voltage extracted from the main simulation can be implemented in order to study the zero sequence current with a smaller approximation considering that the inductances and resistances are frequency dependent. To obtain a light simulation the fast Fourier



(a) Result for the simulation presented in 8.3.



(b) Zoom of the initial zero sequence voltage waveform.

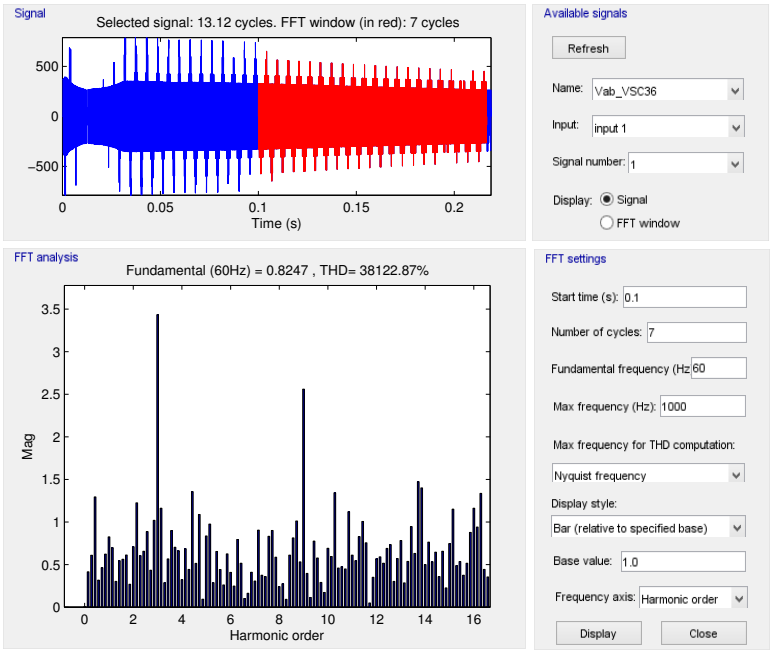
Figure 9.4: Zero sequence voltage waveform

transform (FFT) may be applied to the zero sequence voltage, as shown in figure 9.5; the highest contributes will then be applied to the FEM model finding the current at each frequency. Finally all the current phasors obtained will be reported in time domain and added up, giving the total zero sequence current. This process is valid if the saturation of the ZSBT is not reached.
This is an approximated approach since the problem to be solved is complex (electric parameters are frequency and current dependent).

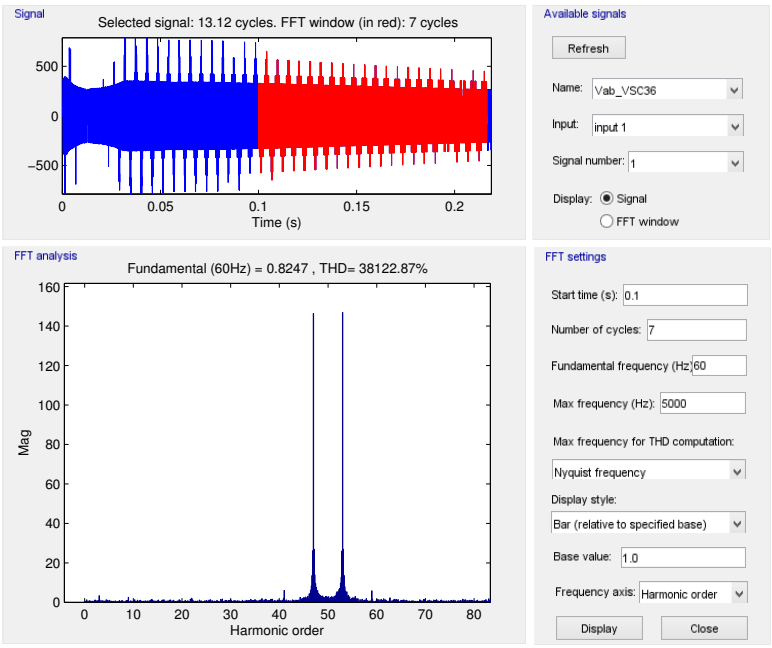
9.2.2 Design

The first interesting step is to understand the effects due to the positive current on the ZSBT and to validate the positive sequence impedances used for these components. For this purpose a general design methodology will be followed while a multi-objective optimization should be run to find the best geometry.
A low number of turns $N = 12$ is considered for each winding and the target inductance is $L0 = 3\ [m\Omega]$; according to chapter 2.1.4 the auto-inductance L should be $L = 1\ [mH]$. The magnetic core is chosen to have a $C + I$ shape to simplify the problem and it is built with silicon steel $M - 45$ with a relative permeability $\mu = 4700$. The air gap is necessary to built the windings: with the CI magnetic core two air gaps are realized with $t_{air} = 0.04\ [mm]$ in order to obtain a high inductance. The parameters that still have to be fixed are the iron section S_{fe} and the length of the magnetic core l_{core}. An initial zero sequence current must be chosen for the circuit design and then the design follows an iterative process: this parameters is fixed to $I0_d = 14\ [A\ peak]$. The magnetic circuit expression can be written:

$$3 \cdot N \cdot I0_d = \Re \cdot \Phi = \left(\frac{l_{core} + \mu \cdot t_{air}}{\mu_0 \cdot \mu \cdot S_{fe}} \right) = B \cdot \left(\frac{l_{core} + \mu \cdot t_{air}}{\mu \cdot \mu_0} \right) \tag{9.46}$$



(a) Low frequencies components.



(b) High frequencies components.

Figure 9.5: FFT analysis of the zero sequence voltage: the triplen harmonics are visible in the spectrum, even if the predominant components are centred at $2 \cdot switching frequency$.

where B is the magnetic flux density and it can be fixed equal to $B = 1.2$ $[T]$. The length of the circuit becomes:

$$l_{core} = \frac{3N \cdot I0_d \cdot \mu \cdot \mu_0}{B} - \mu \cdot t_{air} = 2.17 \ [m]. \tag{9.47}$$

The iron section required to obtain the target self-inductance can be calculated from the inductance expression:

$$L = \frac{N^2}{\Re} = \frac{N^2 \cdot \mu_0 \cdot \mu \cdot S_{fe}}{l_{core} + t \cdot \mu} \tag{9.48}$$

$$S_{fe} = \frac{L \cdot (l_{core} + t \cdot \mu)}{N^2 \cdot \mu_0 \cdot \mu} = \frac{1 \cdot 10^{-3} \cdot (2.17 + 0.08 \cdot 10^{-3} \cdot 4689}{12^2 \cdot \mu_0 \cdot 4689} = 3000 \ [mm^2] \tag{9.49}$$

The core weight would be approximatively:

$$W_{fe} = \gamma \cdot S_{fe} \cdot l_{gap} = 7700 \cdot 3000 \cdot 10^{-6} \cdot 2.17 = 50 \ [kg] \tag{9.50}$$

where γ is the magnetic iron specific weight. This solution is feasible because the iron weight is low referred to the transformer; to find the core dimensions the windings must be designed. In order to keep the resistance low as in the transformer, the conductors should be divided in smaller copper strips. The chosen format is the same used in the power transformer and therefore the single conductor size is 10×4 $[mm^2]$, with a copper section $S_{single} = 39.14$ $[mm^2]$. The insulation used is *nomex* with thickness $t_i = 0.125$ $[mm]$. One wire turn is composed by an array of 10×3 conductors and the global dimensions are: 102.5×12.75 $[mm^2]$. To obtain $N = 12$ turns an array with dimensions 2×6 might be used and the result is shown in figure 9.6. The medium turn length is:

$$lm = 2 \cdot (136.5 + 50 + 136.5 + 60) \cdot 1.3 \cdot 10^{-3} = 1 \ [m] \tag{9.51}$$

with a safety coefficient $k = 1.3$ and therefore the winding resistance is:

$$R = k_{corr} \cdot \rho \cdot \frac{N \cdot lm}{S_{cu}} = 1.2 \cdot 0.018 \cdot \frac{12 \cdot 1}{1174.2} = 0.221 \ [m\Omega]. \tag{9.52}$$

where $k_{corr} = 1.2$ is the same used with the power transformer and considers the uneven current distribution in the wire section. The value used in the simulation for the positive sequence resistance was $R = 1.4$ $[m\Omega]$, therefore there is still a margin to increase the number of turns eventually.
All the parameters are reported in table 9.5.
The geometry has been defined; to study the inductances and the effect of the positive sequence currents a 2-D FEM software has been used.
Since the nominal current in the primary winding of the transformer was $I1 = 2090$ $[A]$, this current has been used also in these simulations (and the current density will be higher).

In figure 9.7a the set of current applied is:

$$\begin{cases} Ia = \sqrt{2} \cdot I \cdot \sin(\omega t + \phi) = \sqrt{2} \cdot 2090 \cdot \sin(0) == 2955.7 \ [A] \\ Ib = \sqrt{2} \cdot I \cdot \sin(\omega t + \phi) = \sqrt{2} \cdot 2090 \cdot \sin(-120) = -1477.8 \ [A] \\ Ic = \sqrt{2} \cdot I \cdot \sin(\omega t + \phi) = \sqrt{2} \cdot 2090 \cdot \sin(-240) = -1477.8 \ [A]. \end{cases} \tag{9.53}$$

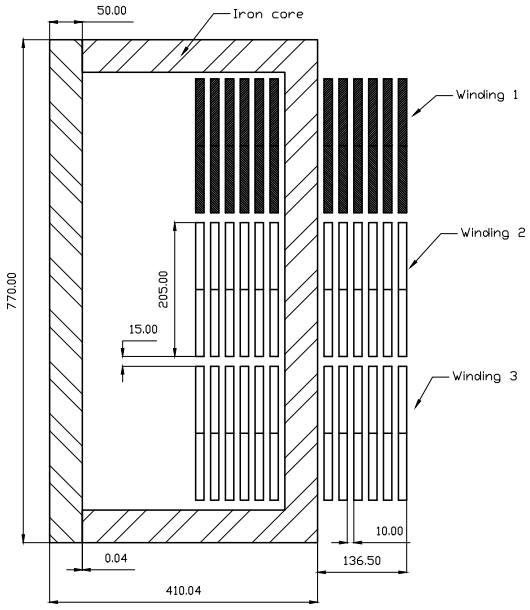
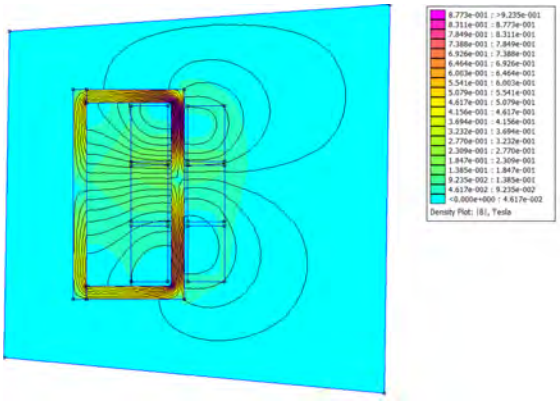


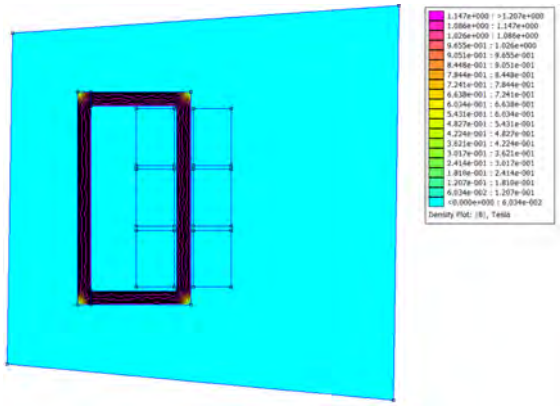
Figure 9.6: ZSBT dimensions.

Parameter	*Symbol*	*Value*	*Unit*
Number of turns	N	12	$[turns]$
Target inductance	$L0$	3	$[mH]$
Magnetic sheets thickness	t_s	0.5	$[mm]$
Magnetic core premeability	μ	4689	$[/]$
Design current	I	2	$[kA]$
Design zero seq. current	$I0_d$	14	$[A\ peak]$
Current density	J	1.8	$[A/mm^2]$
Copper section	S_{cu}	1161.1	$[mm^2]$
Copper real section	S_{fe-r}	1174.2	$[mm^2]$
Air gap	t_{air}	0.4	$[mm]$
Core length	l_{core}	2.17	$[m]$
Iron coresection	S_{fe}	3000	$[mm^2]$
Iron coresize	lxd	50×60	$[mm^2]$
Core weight	W_{fe}	50	$[kg]$
Windingresistnce	R	0.22	$[m\Omega]$

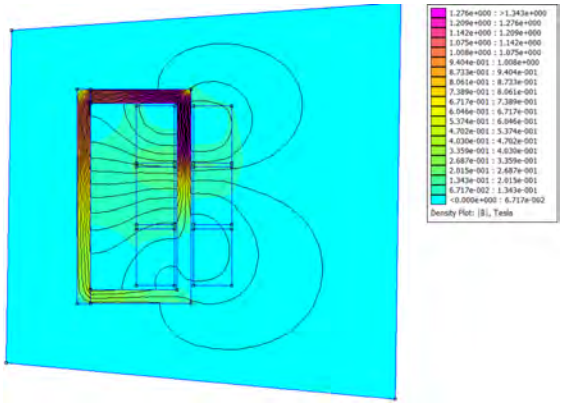
Table 9.5: ZSBTs parameters.



(a) Positive sequence simulation.



(b) Zero sequence simulation.



(c) Positive+zero sequence simulation.

Figure 9.7: FEM simulations with concentrated windings.

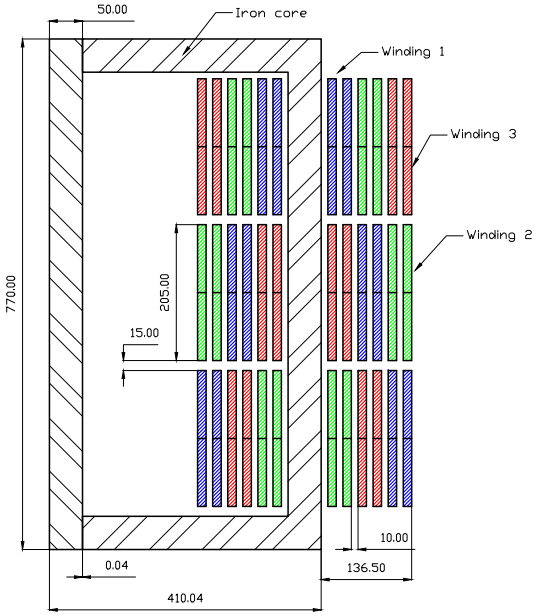


Figure 9.8: ZSBT dimensions.

With this set of currents the magnetic flux density should be theoretically zero inside the magnetic core. The flux lines have a path in either air and iron while there are no flux lines entirely closed in the iron core. Because of these flux lines closed in air associated to flux leakage, the magnetic flux density inside the core reaches a value similar to the one used in the component design where the current is maximum. The coupling coefficient is expected to be low and different in each winding since different saturation conditions have been reached in the points of the magnetic core and the flux lines are concentrated around the central winding. The leakage inductances result: $L0_a = 8.96\ [\mu H]$; $L0_b = 4.72\ [\mu H]$; $L0_c = 16.1\ [\mu H]$, where the inductance of the central winding is one forth of the inductance of phase A. This ratio should be kept near to 1 in order to avoid impedances asymmetries.
In figure 9.7b only a zero sequence current $I0 = 14\ [A]$ is applied to the windings; naturally all the flux lines are closed into the magnetic core, the inductances result $L_a = 3.118\ [mH]$,$L_b = 3.121\ [mH]$, $L_a = 3.118\ [mH]$. These parameters represent the zero sequence inductance according to the observations in chapter 2.1.4.
In figure 9.7c the currents applied on the previous two cases are added; the leakage inductance heavily affects the fluxes distribution. The magnetic flux density is uneven distributed and this cause also a zero sequence impedance unbalance.

In order to obtain a more efficient design, the windings may be distributed as shown in figure 9.8. In this way a better coupling between the windings is achieved and the leakage inductance will be reduced. In figure 9.9a the same currents shown in equation

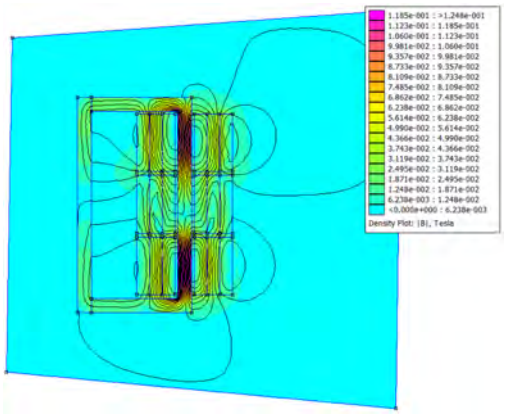
9.53 are applied to the new winding configuration. As it can be noticed, the maximum magnetic flux density reached is here $B = 0.12$ $[T]$, while in the previous case it was $B = 0.92$ $[T]$. This implies a better symmetry in the positive sequence impedance and a reduced impact of the leakage inductances, that in this simulation result: $L0_a = 0.559$ $[\mu H]$; $L0_b = 0.53$ $[\mu H]$; $L0_c = 0.521$ $[\mu H]$.
In figure 9.9b the simulation is practically equal to the previous in figure 9.7b. The zero sequence impedances result: $L_a = 3.16$ $[mH]$,$L_b = 3.16$ $[mH]$, $L_c = 3.16$ $[mH]$.
In figure 9.9c the sum of positive and zero sequence is reported: the positive sequence slightly affects the ZSBT behaviour in comparison with the pure zero sequence case. The coupling coefficient will be therefore higher than the previous case and the blocking effect will be better according to chapter 2.1.4 without any design modification.

Using the distributed model of the ZSBT with the hypothesis of circuit linearity (therefore neglecting the saturation),the FEM simulations can be run at the most relevant frequencies that appear in the zero sequence voltage spectrum, obtaining informations on the impedance function of the frequency $z = f(frequency)$. Supposing that the ZSBTs zero sequence impedance is much bigger than the power transformer zero sequence impedance (true especially if a tertiary winding delta connected is used), the power transformer effect can be neglected and therefore the zero sequence voltage may be applied directly to the series of two ZSBTs. All the current phasors must then be reported to the time domain and summed, giving the overall periodic zero sequence current.
From figure 9.5 the highest voltage frequencies are extracted and reported in table 9.6. The penetration depth δ relatively to each frequency is also reported in order to make a comparison with the iron sheet thickness. δ is calculated as:

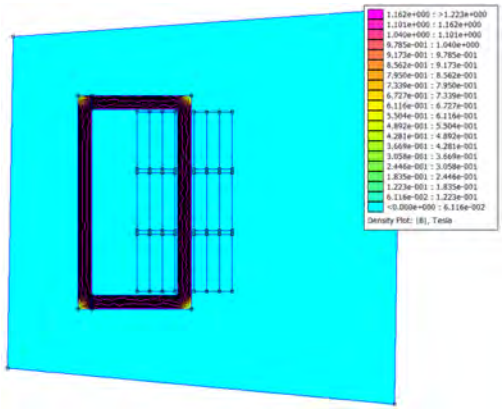
$$\delta = \sqrt{\frac{2}{\mu_r \cdot \mu_0 \cdot \omega \cdot \sigma}} \tag{9.54}$$

where μ_r and σ are the relative permeability and the conductivity of the iron used for the magnetic core. If $M - 45steel$ is used (non laminated steel for rotating machines), $\mu_r = 4700$ and $\sigma = 2.9$ $[\frac{MS}{m}]$.

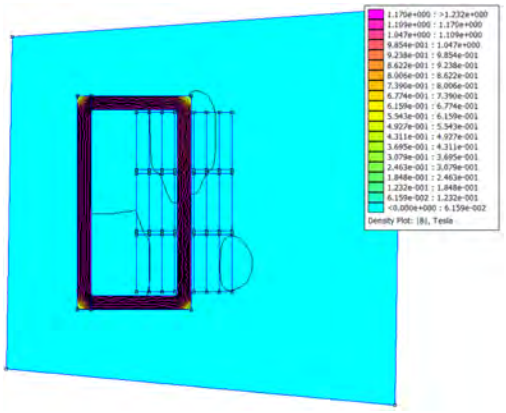
Before starting with the simulations some consideration are worth to be made about the influence of the ratio between iron sheet thickness and penetration depth on the zero sequence impedance. If the ZSBTs cores were not laminated the penetration depth calculated at the fundamental frequency would be smaller than the core thickness causing the flux lines to be external to the magnetic core and the leakage inductance would be increased. A solution would be to keep the penetration depth high or to use thin iron sheets. Since $\delta = \propto \frac{1}{\sqrt{\mu \cdot \sigma}}$ the product $\sigma \cdot \mu$ should be kept low. Again μ is also related to the quantity of flux lines closed outside the magnetic core and therefore it should be chosen high to keep the good coupling between the windings. If the zero sequence impedance was not enough, the solution would be to increase the core resistivity or to reduce the sheets thickness.
Through FEM simulations the impedance presented by the inductor has been calculated considering the skin concentration of the currents in the iron core but neglecting the



(a) Positive sequence simulation.



(b) Zero sequence simulation.



(c) Positive+zero sequence simulation.

Figure 9.9: FEM simulations with distributed windings.

$Frequency\ [Hz]$	$Harmonic\ order$	$Value\ [V\ peak]$	$P.\ depth\ [mm]$
180	3	3.5	0.32
360	6	2.29	0.227
540	9	3.09	0.186
720	12	1.41	0.186
900	15	1.1	0.144
2460	41	4.79	86.9
2820	47	241.7	81.2
3180	53	241.2	76.5
3540	59	4.14	72.5

Table 9.6: Voltage zero sequence analysis.

$Frequency\ [Hz]$	$Inductance\ [mH]$	$Resistance\ [\Omega]$	$Impedance\ [\Omega]$	$Current\ [A]$
180	3.27	1.57	4.012	0.436
360	2.27	3.62	6.28	0.182
540	1.74	4.85	7.64	0.202
720	1.45	5.75	8.72	0.081
900	1.28	6.36	9.64	0.057
2460	0.767	10.5	15.85	0.151
2820	0.719	11.3	17.03	7.096
3180	0.678	12.1	18.13	6.652
3540	0.645	12.74	19.19	0.108

Table 9.7: Single ZSBTs simulation result.

uneven current distribution in the windings section. The results are reported in table 9.7. The inductance becomes lower increasing the frequency because the equivalent section for the magnetic flux density is decreased. The resistance becomes higher for the same reason and the total impedance grows with the frequency. The current is therefore calculated considering the impedance of two $ZSBT$.

In figure 9.10 the total current is depicted considering the worst hypothesis of signals in phase between each other. The maximum current reached is approximatively $Imax = 15\ [A]$ therefore the design limit used $I0_d = 14\ [A]$ is respected.
Decreasing the sheet thickness the impedance will become higher and the zero sequence current will decrease. With these considerations the length of the magnetic core might be reduced according to equation 9.47 and in order to keep the same zero sequence impedance also the iron section S_{fe} should be decreased. This leads to weight reduction even if the thermal problem has also to be considered. A good design solution would be found with an optimization, that can be part of the future work. Many variables are involved, some of these variables are integers and the optimization is multi-objective (weight and

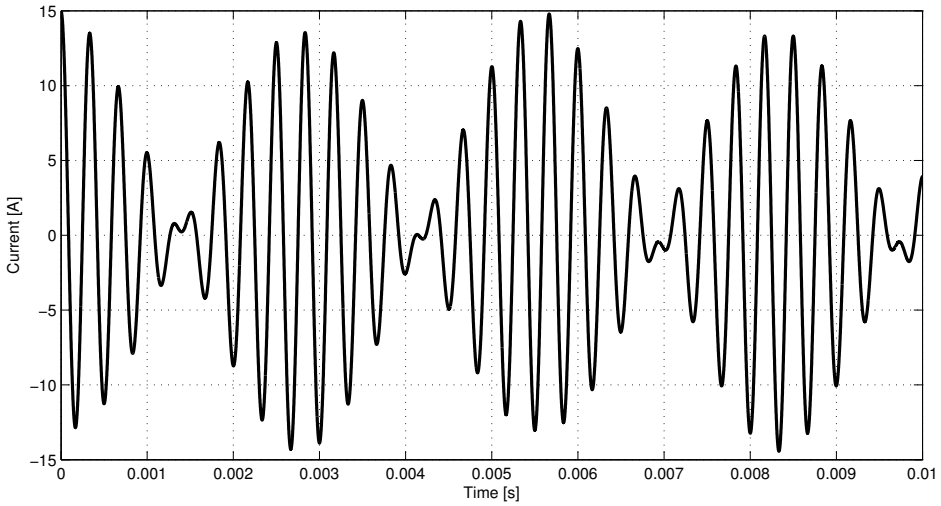


Figure 9.10: Zero sequence current in the worst condition.

Parameter	*Value*	*Unit*
Rf	1.4	$[m\Omega]$
Lf	60	$[\mu H]$

Table 9.8: Filter impedance parameters.

inductance have to be optimized); the optimization should be studied carefully starting from the choice of the algorithm.

9.3 Filtering impedance

The last element that should be designed is the filtering inductance. In the simulations the parameters shown in table 9.8 have been used. This parameters have been estimated, especially the resistance has been chosen with a safety factor. In order to compute the real efficiency and to find the size of the inductors in this chapter the filtering components will be designed. The nominal current in the grid side is $In = 4040\ [A]$ and therefore the inductor should be designed for this value. Depending on the construction of the inductors, the weight and size obtained are different. In this work a three-phase inductor water cooled will be designed, in order to reduce the component size. In the hypothesis of forced water circulation, a convective coefficient $\alpha = 100\ [\frac{W}{m^2 \cdot K}]$ could be considered. The current can be considered to be divided in $k = 4$ parallel paths and therefore in each turn the current is approximatively $Ip = 1.01\ [kA]$. The current density can be kept high since the number of turns will be limited and the water cooling system is used. Using

$j = 4\ \frac{A}{mm^2}$, the wire section becomes:

$$S_{cu} = \frac{I}{j} = \frac{1010}{4} = 250\ mm^2. \tag{9.55}$$

The section is big and in order to reduce the skin effect losses many conductors in each turn have to be used. With a fill factor equal to $k_{fill} = 0.75$ that considers the insulation between the conductors, the effective section becomes:

$$S = \frac{S_c u}{k_{fill}} = \frac{250}{0.75} = 330\ mm^2. \tag{9.56}$$

The diameter associated to the wire section S is:

$$dc = \sqrt{\frac{4 \cdot S}{\pi}} = \frac{4 \cdot 330}{\pi} = 20\ [mm]. \tag{9.57}$$

The distance between each turn is fixed to $d = 5\ [mm]$ and the inductor medium diameter is fixed to $Dm = 0.5\ [m]$ ($Dm > 15 \cdot dc$). Considering the thermal equation:

$$P_{loss} = \alpha \cdot \xi \cdot \pi \cdot Dm \cdot N \cdot \theta \tag{9.58}$$

where α is the water convective coefficient, $\xi = 0.7$ is a coefficient that keep into account the surface reduction due to the insulating supports between each turn and θ indicates the winding over-temperature referring to the water temperature. The power loss can be calculated as:

$$P_{loss} = \rho \cdot \frac{\pi \cdot Dm \cdot I^2}{\pi \cdot \frac{dc^2}{4}} \tag{9.59}$$

where rho is the copper resistivity calculated at the working temperature. Assuming an over-temperature of 10 [$^\circ K$], considering the coefficient $\alpha_c = 4 \cdot 10^{-3}$ and considering the water temperature equal to $T_w = 30\ [^\circ C]$, the resistivity becomes:

$$\rho_{40} = \rho_{20} \cdot (1 + \alpha_c \Delta T) = 0.0178 \cdot (1 + 4 \cdot 10^{-3} \cdot 20) = 0.0192\ [\Omega \frac{mm^2}{m}] \tag{9.60}$$

Substituting equation 9.59 into equation 9.58 the over-temperature results:

$$\theta = \frac{4 \cdot \rho \cdot I^2}{\pi^2 \cdot \alpha \cdot \xi \cdot k_{fill} \cdot dc^3} = \frac{0.02 \cdot 4 \cdot 1010^2}{\pi^2 \cdot 200 \cdot 0.7 \cdot 0.75 \cdot 0.02^3} = 9.85\ [^\circ K] \tag{9.61}$$

in accordance with the resistivity used. The inductor is considered to be built with $k = 4$ parallel circuits disposed along the inductor axis. The axial length of the entire circuit inductor h depends on the number of axial turns Na:

$$h = Na \cdot dc + (Na - 1) \cdot d \simeq Na \cdot (dc + d) \tag{9.62}$$

Considering to use a number of radial turns $Nr = 2$, the total number of turns of one circuit $N = Na \cdot Nr$. The global inductance will be the parallel of k circuits and therefore

each circuit should have an inductance equal to $L = k \cdot L_{target} = 4 \cdot 60 = 240$ $[\mu H]$. The global inductor may be designed as an inductor with fictitious inductance:

$$L_{TOT} = \frac{\Phi_c}{I} = \frac{k^2 \cdot N^2 \cdot I \cdot \mu_0 \cdot \pi Dm^2}{4 \cdot h} = k \cdot L_{target} = 4 \cdot 240 = 960 \ [\mu H]. \tag{9.63}$$

The inductance expressed using equation 9.62 becomes:

$$L_{TOT} = \mu_0 \frac{\pi}{4} \cdot N^2 \cdot \frac{Dm^2}{Na \cdot (dc + d)} \tag{9.64}$$

and therefore the total number of turns N is:

$$N = \frac{4}{\pi} \cdot \frac{L_{TOT}}{\mu_0} \cdot \frac{dc + d}{Nr \cdot Dm^2} = \frac{4}{\pi} \cdot \frac{960 \cdot 10^{-6}}{\mu_0} \cdot \frac{0.02 + 0.005}{2 \cdot 0.5^2} = 48. \tag{9.65}$$

The number of axial turns $Na = \frac{N}{Nr} = 24$ is multiple of the number of circuits k. The inductor height h is:

$$h = Na \cdot dc + (Na - 1) \cdot d = 24 \cdot 0.02 + 23 \cdot 0.005 = 0.595 \ [m] \tag{9.66}$$

while the winding radial length r is:

$$r = Nr \cdot dc + (Nr - 1) \cdot d = 2 \cdot 0.02 + 0.005 = 0.045 \ [m]. \tag{9.67}$$

Considering that the inductor is short, the inductance may be approximated with this empirical formula that avoid the use of Nagaoka's coefficients:

$$\begin{aligned} L_{TOT} &= 1.044 \cdot \frac{\pi}{4} \cdot \mu_0 \cdot N^2 \cdot Dm \cdot \left(\frac{Dm}{h + r} \right)^{0.5} \\ &= 1.044 \cdot \frac{\pi}{4} \cdot \mu_0 \cdot 48^2 \cdot 0.5 \cdot \left(\frac{0.5}{0.595 + 0.045} \right)^{0.5} = 1.049 \ [mH] \end{aligned} \tag{9.68}$$

and therefore the parallel inductance will be:

$$L = \frac{L_{TOT}}{k^2} = \frac{L_{TOT}}{16} = 65.57 \ [\mu H] \tag{9.69}$$

The medium length of one inductor circuit is:

$$lm = \frac{N}{4} \cdot \pi \cdot Dm = 12 \cdot \pi \cdot 0.5 = 18.85 \ [m] \tag{9.70}$$

and the resistance considering the resistivity calculated in 9.60 becomes:

$$R = \rho \frac{lm}{k \cdot S_c u} = 0.0192 \cdot \frac{18.85}{4 \cdot 250} = 0.362 \ [m\Omega] \tag{9.71}$$

This resistance value is 4 times smaller than the one chosen in the simulations. The efficiency therefore will be higher. The simplified inductor section is depicted in figure 9.11. The real inductor should reserve some space for the winding connections and the external water container should be designed considering the the thermal analysis and the power that should be extracted.

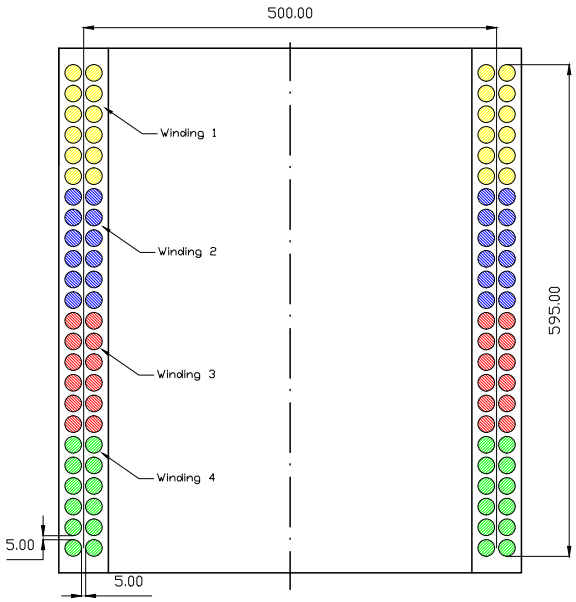


Figure 9.11: Filter inductor design.

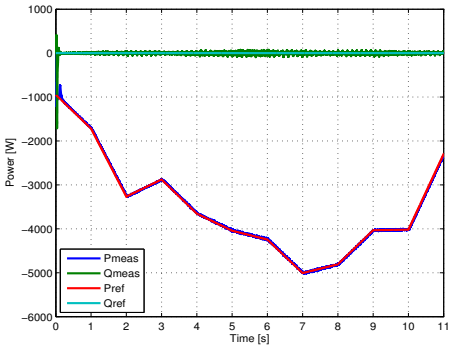
Chapter 10

Efficiency and thermal considerations

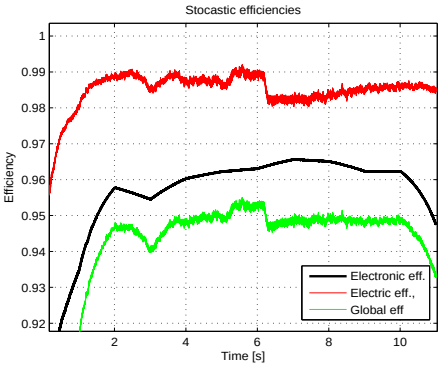
10.1 Efficiency and harmonics standards

In this chapter the real efficiency substituting the components designed in chapter 9 will be simulated. The new set of used parameters is reported in table 10.1 and the switching frequency used is $f_{switching} = 1.5\ [kHz]$. The expected efficiency should be higher than the one found in the previous chapters since the resistance was over-estimated in order to keep a certain safety margin.
The same simulation reported in chapter 8.3 with the new set of parameters is represented in figure 10.1. In figure 10.2 the same *p.u.* parameters are used but the base power has been increased to $Pb = 12\ [MW]$, while in figure 10.3 the transformer ratio has been changed: in this way the power deliverable $Pb = 16\ [MW]$ is higher while the fault-through operational capability is reduced. As shown in the efficiency plots the high number of devices limits the electronic efficiency giving an overall efficiency in the full load condition near to $\eta = 0.953\%$. As shown in figure 10.3 an higher value is obviously obtained changing the transformer ratio but in this way the converter is less reliable considering the faults probability. During the normal operation the voltage applied on each switch is far from the voltage limit and this leads to a lower electronic utilization factor.
In figure 10.4 the THD waveforms are depicted for the simulations with base power $Pb = 10\ [MW]$ and $Pb = 16\ [MW]$.
In order to increase the total efficiency the switching frequency must be reduced obtaining a proportional reduction of the switching losses, while the THD and the harmonics injected into the grid will have an higher impact on the power quality. The harmonics level is also related to the filtering inductance and therefore the optimal switching frequency must be found satisfying the power quality requirements and fixing a limit for the inductor size and weight.

The problem of the optimal switching frequency choice has been discussed in [41], where high voltage $IGBTs$ has been replaced with the series of lower voltages compon-

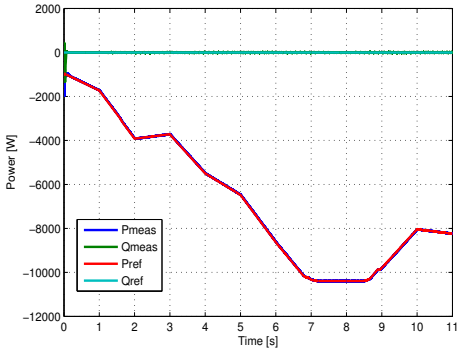


(a) Global active and reactive powers.

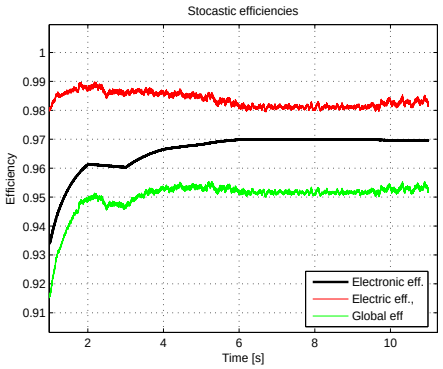


(b) Efficiencies waveforms.

Figure 10.1: Efficiency with: $k_{transformer} = 0.5$, $Pbase = 7\ [MW]$, $f_{sw} = 1.5\ [kHz]$.

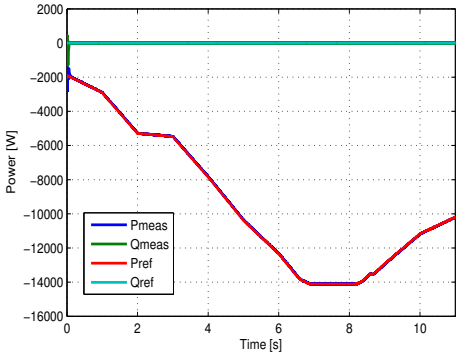


(a) Global active and reactive powers.

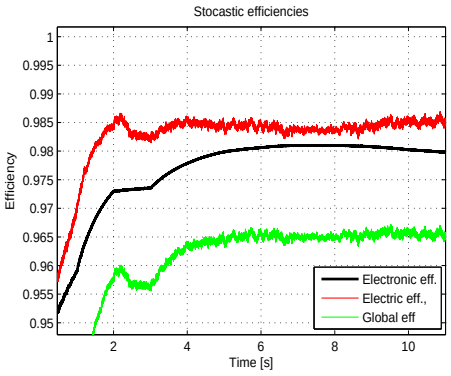


(b) Efficiencies waveforms.

Figure 10.2: Efficiency with: $k_{transformer} = 0.5$, $Pbase = 12\ [MW]$, $f_{sw} = 1.5\ [kHz]$.



(a) Global active and reactive powers.

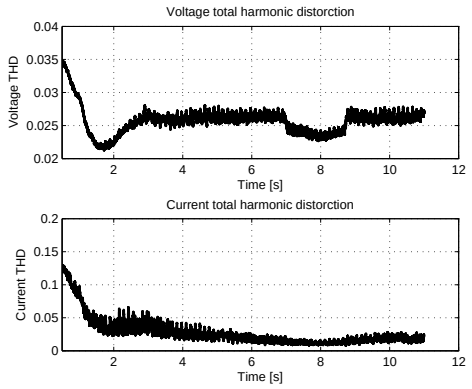


(b) Efficiencies waveforms.

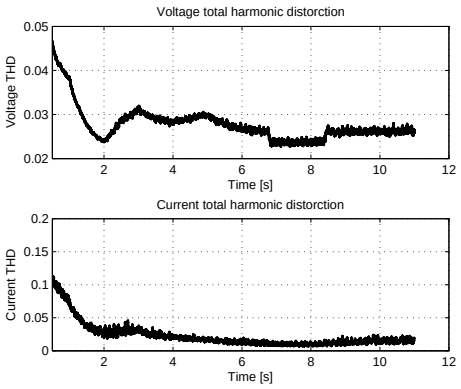
Figure 10.3: Efficiency with: $k_{transformer} = 0.3$, $Pbase = 16\ [MW]$, $f_{sw} = 1.5\ [kHz]$

Component	Parameter	Value
Grid	R_{pu}	0.0144 pu
	L_{pu}	0.0479 pu
Transformer	R_{pu}	0.00695 pu
	L_{pu}	0.06 pu
2 ZSBT	R_{pu}	$4.42 \cdot 10^{-4}$ pu
	L_{pu}	$6.6 \cdot 10^{-4}$ pu
Filter impedance	R_{pu}	0.0025 pu
	L_{pu}	0.157 pu
Total	R_{pu}	0.0243 pu
	L_{pu}	0.2656 pu

Table 10.1: Simulation parameters based on chapter 9.



(a) THD of the simulation in figure 10.2.



(b) THD of the simulation in figure 10.3.

Figure 10.4: Voltage and current global THD of the simulations of figures 10.2, 10.3.

Maximum harmonic current distortion I_ν^* and *TDD* in % of I_L for distribution systems 0.12-69 kV						
	Individual harmonic order ν (odd harmonics) [1]					
I_{SC}/I_L	< 11	$11 \leq \nu < 17$	$17 \leq \nu < 23$	$23 \leq \nu < 35$	$35 \leq \nu$	*TDD*
≤ 20 [2]	4.0	2.0	1.5	0.6	0.3	5.0
(20, 50]	7.0	3.5	2.5	1.0	0.5	8.0
(50, 100]	10.0	4.5	4.0	1.5	0.7	12.0
(100, 1000]	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

[1] Even harmonics are limited to 25 % of the odd harmonic limits.

[2] All power generation equipment is limited to these values of current distortion regardless of I_{SC}/I_L.

For distribution systems in the voltage range 69-161 kV the above limits reduced by 50 % apply.

Figure 10.5: IEEE 1547 current harmonics requirements [44].

ents allowing a power loss reduction and a switching frequency increasing. The same optimization considering the switches data-sheets should be considered in this topology finding the best compromise in terms of reliability and efficiency.
The most common standards for the converter-grid connection are the IEEE 1547 [42] and the BDEW[43]; these standards have an important role to evaluate the converter performances: if the harmonics and THD requirements are satisfied by the inverter, the switching frequency or the filtering inductor may be decreased. In this work the IEEE standard will be considered; the standards use different definitions and a comparative analysis has been studied in [44].

In figure 10.5 the maximum harmonic current distortion limit is reported according to [42]. The current I_{SC} reported is the short circuit current at the grid common coupling point an it is calculated as:

$$I_{sc} = \frac{U}{\sqrt{3} \cdot 2\pi \cdot f \cdot L_{grid}} = \frac{1000}{\sqrt{3} \cdot 2\pi \cdot 60 \cdot 1.27 \cdot 10^{-5}} = 120.6 \ [kA] \tag{10.1}$$

where U is the concatenated grid voltage. According to [42] and [44], when a power generation equipment is considered the limits to consider are the ones with $SCR < 20$ and independent from the short circuit current.
The standard [45] also introduces limits on the voltage harmonics as reported in figure 10.6 and for the voltage sub-harmonics with systems with a voltage lower than $V = 1 \ [kV]$ to limit the flicker effect as shown in figures 10.7 and 10.8. The voltage is exactly $V = 1 \ [kV[$ and therefore only the lowest limits should be applied; to consider a certain safety margin the limits for $1 \ [kV] < V \leq 69 \ [kV]$ will be considered.

Taking as example the simulation with $Pb = 12 \ [MW]$, the FFT analysis of the current waveform is reported in figure 10.9 where a medium power level value is taken as a reference. The FFT analysis of the sub-harmonic voltage is reported in figure 10.10.

Concerning the current analysis, the harmonic levels are far below the limits proposed by the standard considering the harmonics with order $\ni < 35$, while around the switching frequency the levels are slightly above the limit. Since the harmonics to be reduced

Bus voltage V at PCC	Individual harmonic (%)	Total harmonic distortion THD (%)
$V \leq 1.0$ kV	5.0	8.0
1 kV $< V \leq 69$ kV	3.0	5.0
69 kV $< V \leq 161$ kV	1.5	2.5
161 kV $< V$	1.0	1.5[a]

[a]High-voltage systems can have up to 2.0% THD where the cause is an HVDC terminal whose effects will have attenuated at points in the network where future users may be connected.

Figure 10.6: Voltage limits according to [45].

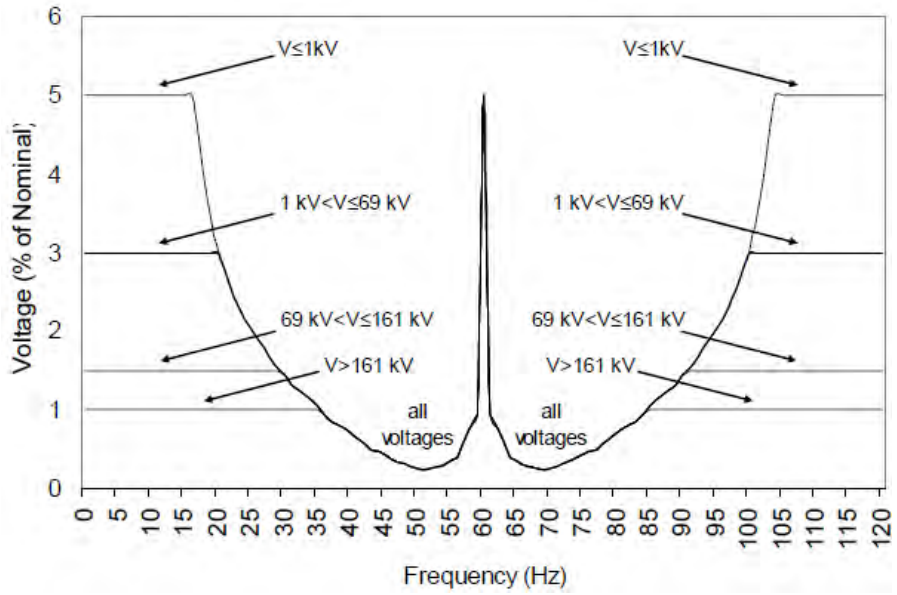


Figure 10.7: Sub-harmonics voltage limits based on flicker for $f = 60$ $[Hz]$ systems [45].

Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)	Frequency (Hz)	Magnitude (%)
16	5.00	27	1.78	38	0.81	49	0.28
17	4.50	28	1.64	39	0.78	50	0.25
18	3.90	29	1.54	40	0.71	51	0.23
19	3.45	30	1.43	41	0.64	52	0.25
20	3.00	31	1.33	42	0.57	53	0.27
21	2.77	32	1.26	43	0.50	54	0.29
22	2.53	33	1.20	44	0.48	55	0.35
23	2.30	34	1.13	45	0.43	56	0.40
24	2.15	35	1.05	46	0.38	57	0.58
25	2.03	36	0.95	47	0.34	58	0.77
26	1.90	37	0.85	48	0.31	59	0.95

Figure 10.8: Sub-harmonics voltage limits based on flicker for $f = 60$ $[Hz]$ systems [45].

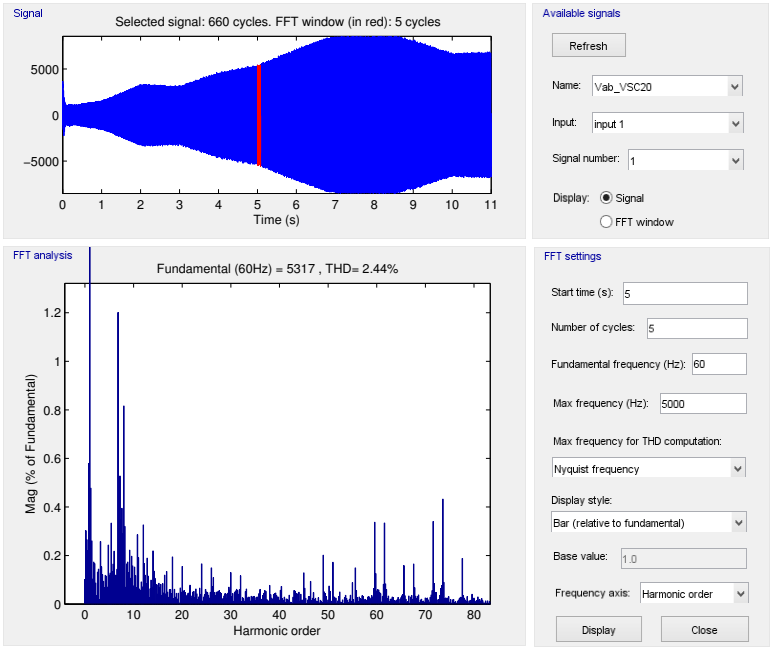


Figure 10.9: Current FFT with: $k_{transformer} = 0.5$, $Pbase = 12\ [MW]$, $f_{sw} = 1.5\ [kHz]$.

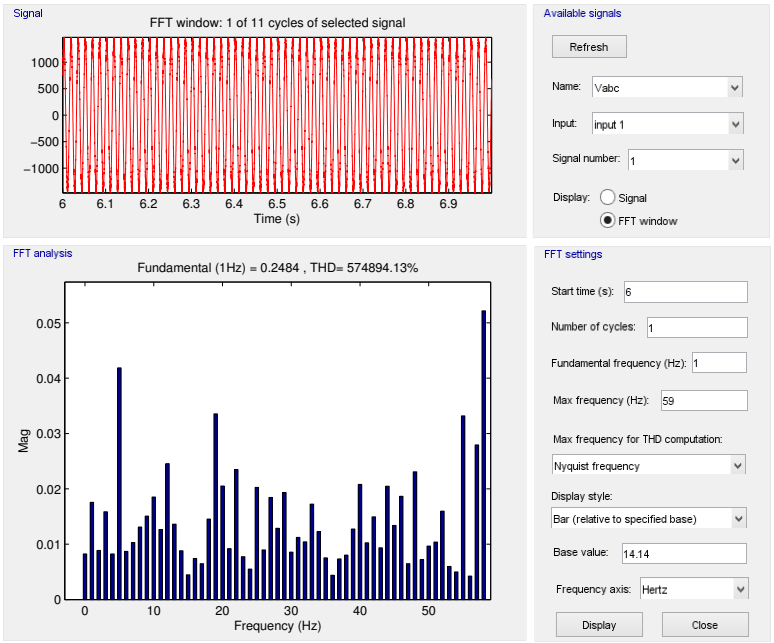
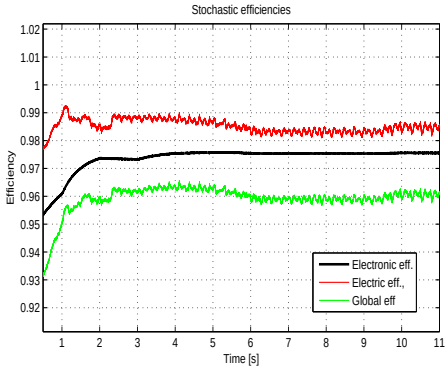
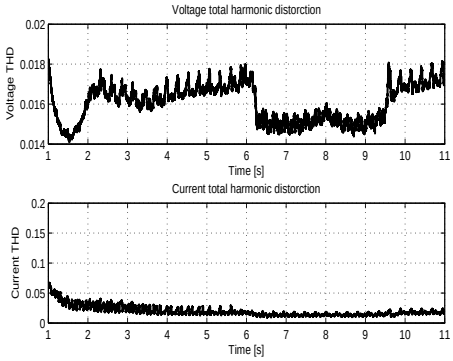


Figure 10.10: Voltage sub-harmonic FFT with: $k_{transformer} = 0.5$, $Pbase = 12\ [MW]$, $f_{sw} = 1.5\ [kHz]$. Harmonic magnitude expressed in % with respect to the fundamental $V = \sqrt{2} \cdot 1000 = 1414\ [V]$.



(a) Efficiencies plots.



(b) Voltage and current THD.

Figure 10.11: Converter simulation with the stochastic power depicted in figure 10.2, $f_{sw} = 780\ [Hz]$ and $L = 120\ \mu H$.

have high frequency, a slight increasing in the filtering inductance value will allows the converter to operate according to the specified standards. The reduced low harmonic amplitude is a characteristic of the multilevel converters and therefore the filter impedance must be designed in order to satisfy the high frequency limits. The structure of the filter may also be changed to an L-C or L-C-L topology depending on the requirements on space and weight.
Regarding the sub-harmonics voltage FFT analysis, the values obtained are again far below the limits reported in figure 10.7 and 10.8.
With an increased filtering inductance the switching frequency of the converter may be reduced with a proportional reduction of the switching losses. For example using again $k_{transformer} = 0.5$ $Pbase = 12\ [MW]$, the switching frequency is changed to $f_{sw} = 780\ [Hz]$ and the filtering inductance is doubled obtaining $L = 120\ [\mu H]$. The switching losses from equation 8.46 become:

$$P = f \cdot E_{on+off} \cdot 4 = \frac{780}{1500} \cdot 9 \cdot 12 = 56.16\ [kW] \tag{10.2}$$

The simulation results in these conditions have been represented in figure 10.11: the global efficiency is higher, reaching $\eta = 96\%$ and the current and voltage THD remain low.

10.2 Thermal considerations

In all the high-power applications a special issue is the temperature control in each component of the converter. The electronic switches must work with a junction temperature normally lower than $T_j = 150\ [°C]$, the refrigerant oil used for the power transformer cooling has a limited working temperature and also the filtering inductor require an appropriate cooling system. Taking as a reference the power value $P = 10\ [MW]$ and

considering the converter efficiency to be $\eta = 0.96\%$, the total thermal power that must be extract is $P_{th} = 10 \cdot (1 - 0.96) \simeq 400\ [kW]$. Since the high power switches are normally liquid-cooled and also the filtering inductors have been designed to be water-cooled, depending on the converter application a possibility could be to recover this low temperature heat. If the converter is installed on-shore a solution could be to use the heat in industrial processes or in buildings heating applications. If the converter is installed off-shore one possibility could be to use an organic Rankine cycle (ORC) that is able to extract power even with ultra-low thermal sources. The fluid of the cycle is chosen with an optimization algorithm considering that many factors such as the boiling point depend on the specific application; more constraints would be added to the general problem since the fluid must also suitable for the electronic cooling application. Since the power in this cycle is produced by a turbine with variable rotating speed, normally a rectifier-inverter stadium is required. The inverter stadium can be avoided and the produced *DC* power could directly assist the optimal *DC* bus in order to maximize the power delivered to the grid. For example this power could assist the single-phase converter with the instantaneous smallest power produced or the three-phase converters if in this case the power ratio between single and three-phase converters is nearer to the optimal one.

10.3 DC power redistribution

As already discussed in chapter 6, when the available power in the DC sides of the single-phase converters is different, the power converted must be fixed to the lowest one. This can be economically acceptable if the power miss-match occurs only for a limited transient. If this condition persists for a long time term or in the worst case if one single-phase converter fails, the potential available power cannot be exploited. One solution could be to use additional switches that will redistribute the DC power on the operative converters; these switches would not normally operate and therefore they would not contribute to the power losses. With a smart design of the DC power plants the converter may also operate near to the optimal power condition: using for example many paralleled strings in the solar case, the power may be distributed between the single-phase and three-phase DC buses. To allow this operation another optimization algorithm to control the additional switches may be used and the general connection scheme has to be designed (using DC-DC choppers if the sources voltage is different).

Conclusions

In this thesis the converter topology based on three single-phase units and two three-phase units proposed in [14] has been studied considering different power sources that can deliver different amount of power. The grid voltage has been fixed to 1 $[kV]$ in order to use low voltage insulation components on the grid side.
The converter is designed in order to guarantee the good operational behaviour even when only one converter is working. A control strategy has been developed and a solution for the issues of initial current overshoot, dynamic current limiting and capacitors voltage balancing has been proposed. The simulations prove the converter stable operation, the benefits given by the balancing circuits and the interleaving effect on the current and voltage THD that remain low with low filtering requirements.
The magnetic elements have been designed in order to obtain simulations results based on real parameters and also to understand the effect of non-conventional components as the ZSBTs.
In a further study the possibility of energy recovery may be explored depending on the converter application, adopting for example a power redistribution scheme or designing an ORC cycle for low temperature heat recovery. Another aspect that is worth to be studied is the filtering inductance scheme that can adopt the $L-C$ or $L-C-L$ solution instead of the simple series inductance.

In questa tesi la topologia di convertitore composta da tre unità monofase e due unità trifase presentata in [14] è stata studiata considerando sorgenti diversificate che possono erogare potenze variabili. La tensione di rete è stata fissata ad 1 $[kV]$ in modo da utilizzare componenti a bassa tensione di isolamento.
Il convertitorè è progettato in modo da garantire l'operazione anche se un solo convertitore è in funzione. La stategia di controllo è stata sviluppata e una soluzione per i problemi di overshoot iniziale di corrente, limitazione dinamica delle correnti e bilanciamento delle tensioni dei condensatori è stata proposta. Le simulazioni provano la stabilità operazionale del convertitore, il funzionamento dei circuiti di bilanciamento e l'effetto dell' interleaving sul THD di correnti e tensioni che rimane limitato con contenuti requisiti per le induttanze di filtro.
Gli elementi magnetici sono stati progettati per ottenere simulazioni basate su parametri reali e per capire gli effetti di componenti non-convenzionali come gli ZSBTs.
In uno studio futuro la possibilità del recupero di energia può essere esplorata in dipen-

denza dall'applicazione del convertitore, utilizzando ad esempio uno schema di redistribuzione della potenza oppure progettando un ciclo ORC per recupero di calore a bassa temperatura. Un ulteriore aspetto che vale la pena di essere studiato è lo schema dell'induttanza di filtro che può utilizzare una soluzione di tipo $L-C$ o $L-C-L$ rispetto alla singola induttanza serie.

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Appendix A

Simulink model

A.1 Id Iq current loops

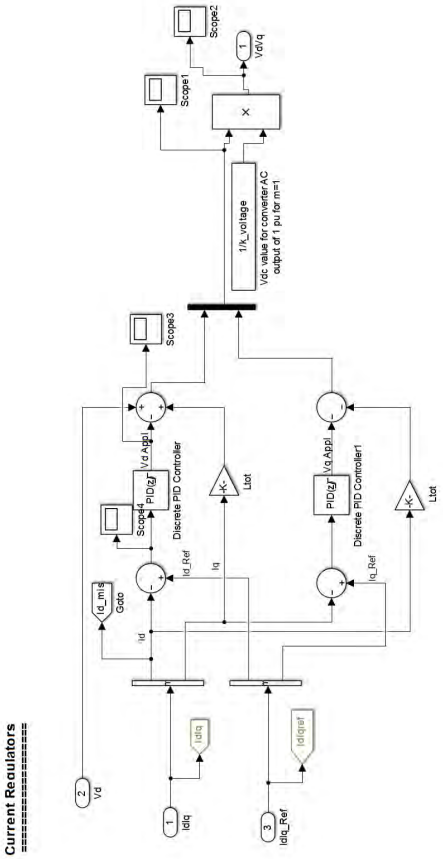

Figure A.1: Id and Iq current loops

A.2 Power loops

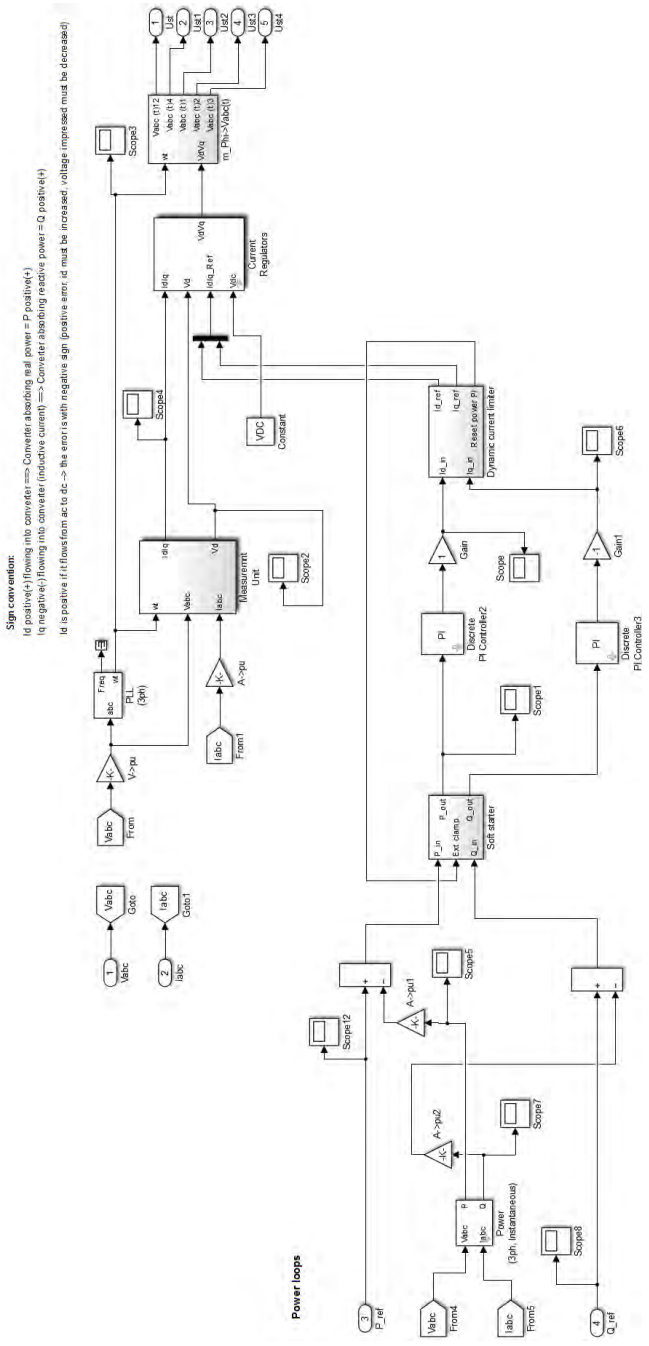

Figure A.2: Active and reactive power loops

A.3 Id Iq dynamic limit

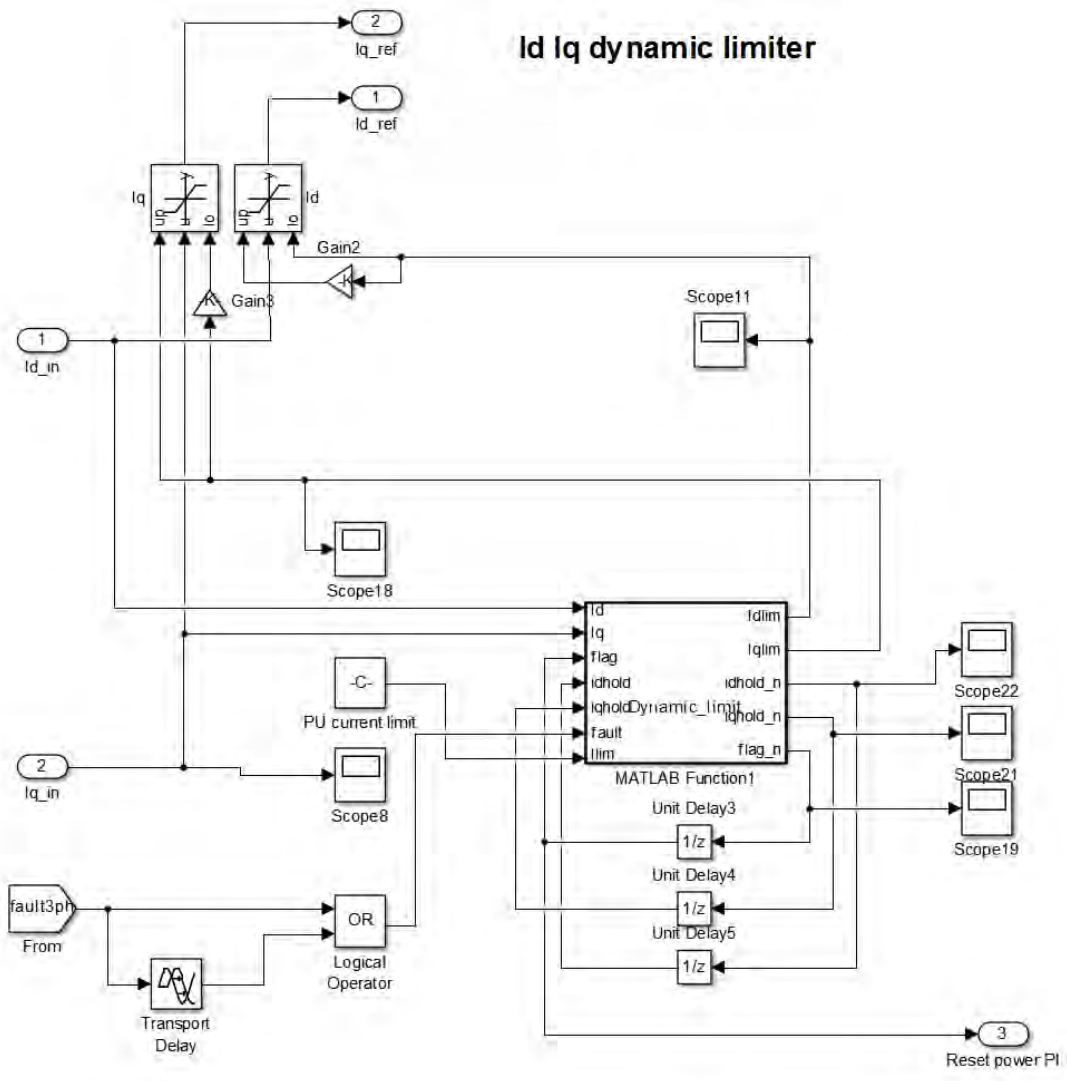

Figure A.3: Active and reactive power loops

A.4 Power splitter and dq to abc conversion

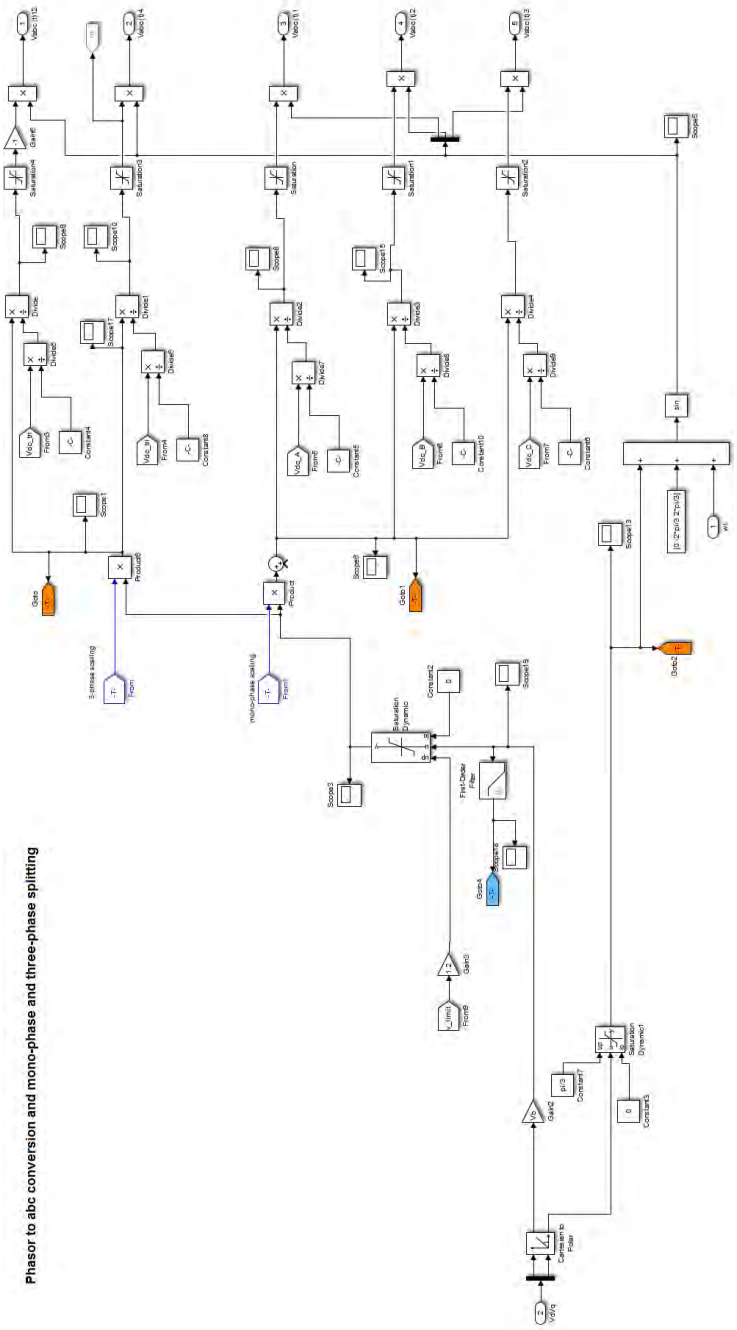

Figure A.4: Active and reactive power loops

A.5 Lookup tables

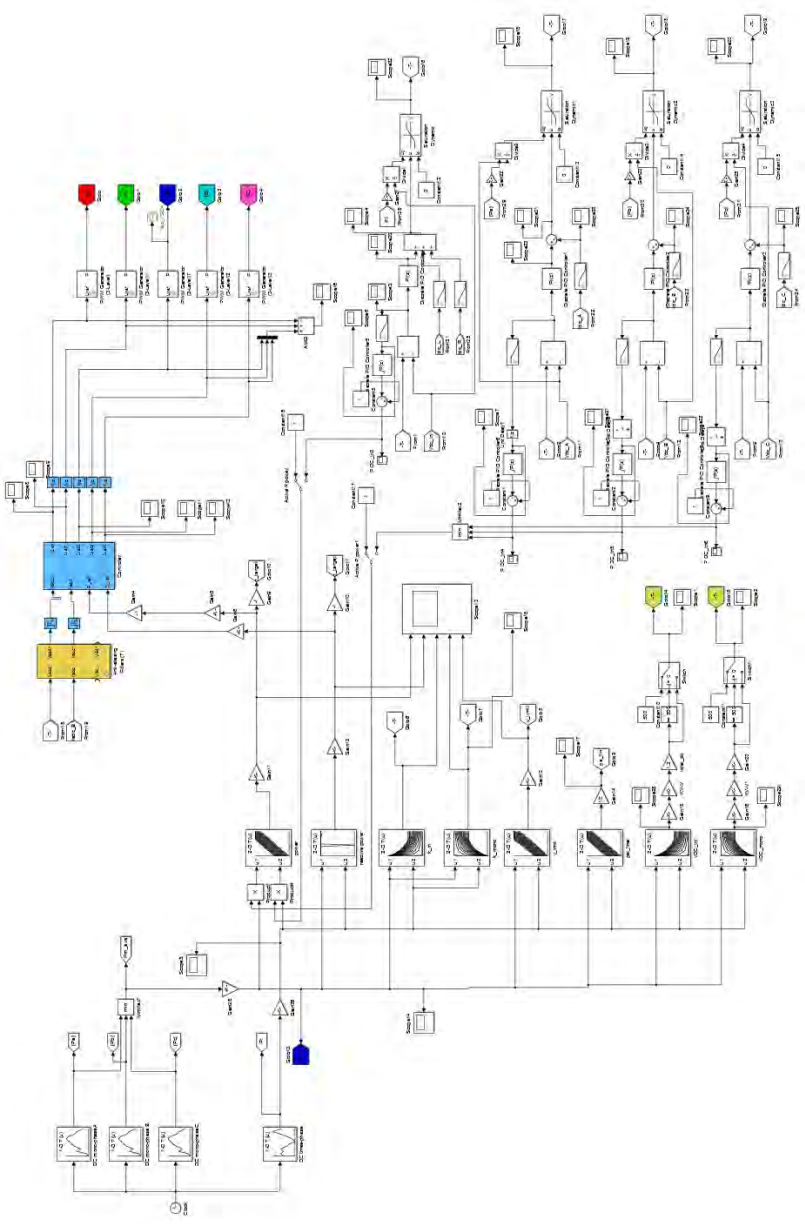

Figure A.5: Active and reactive power loops

A.6 DC source model

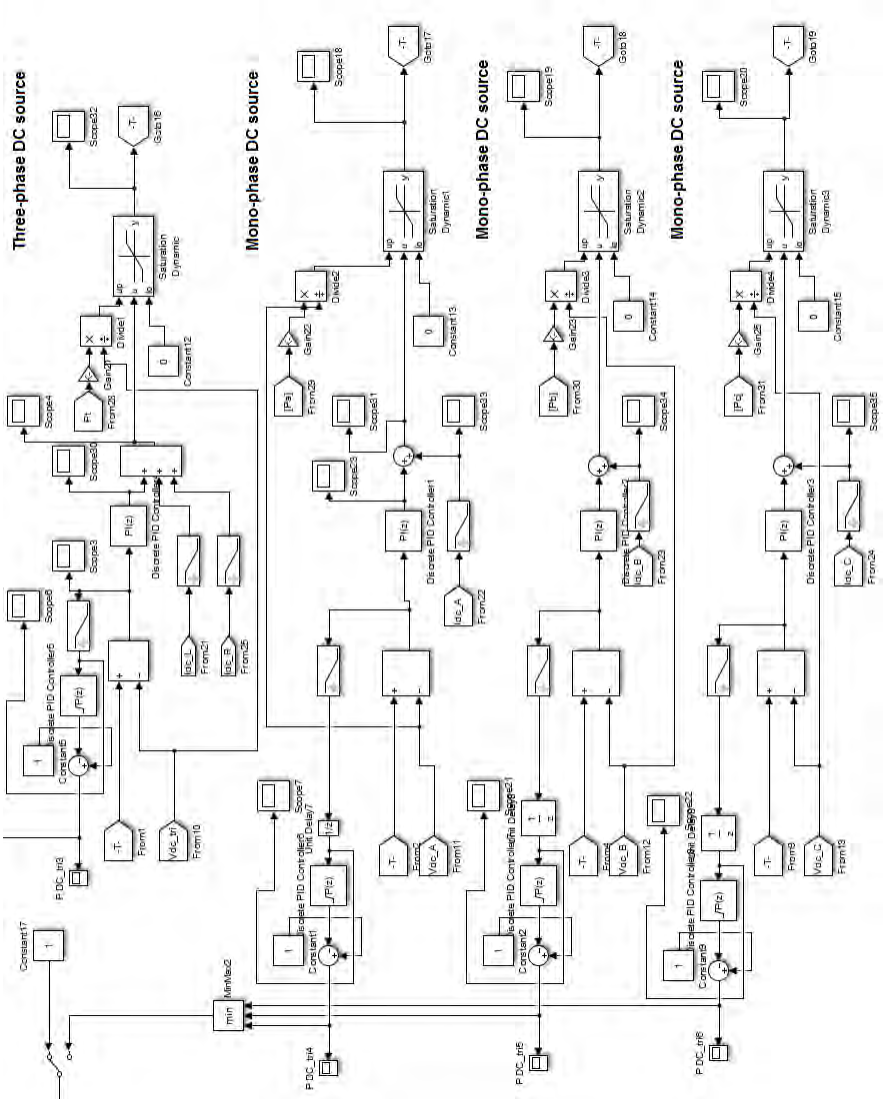

Figure A.6: Active and reactive power loops

A.7 Power circuit

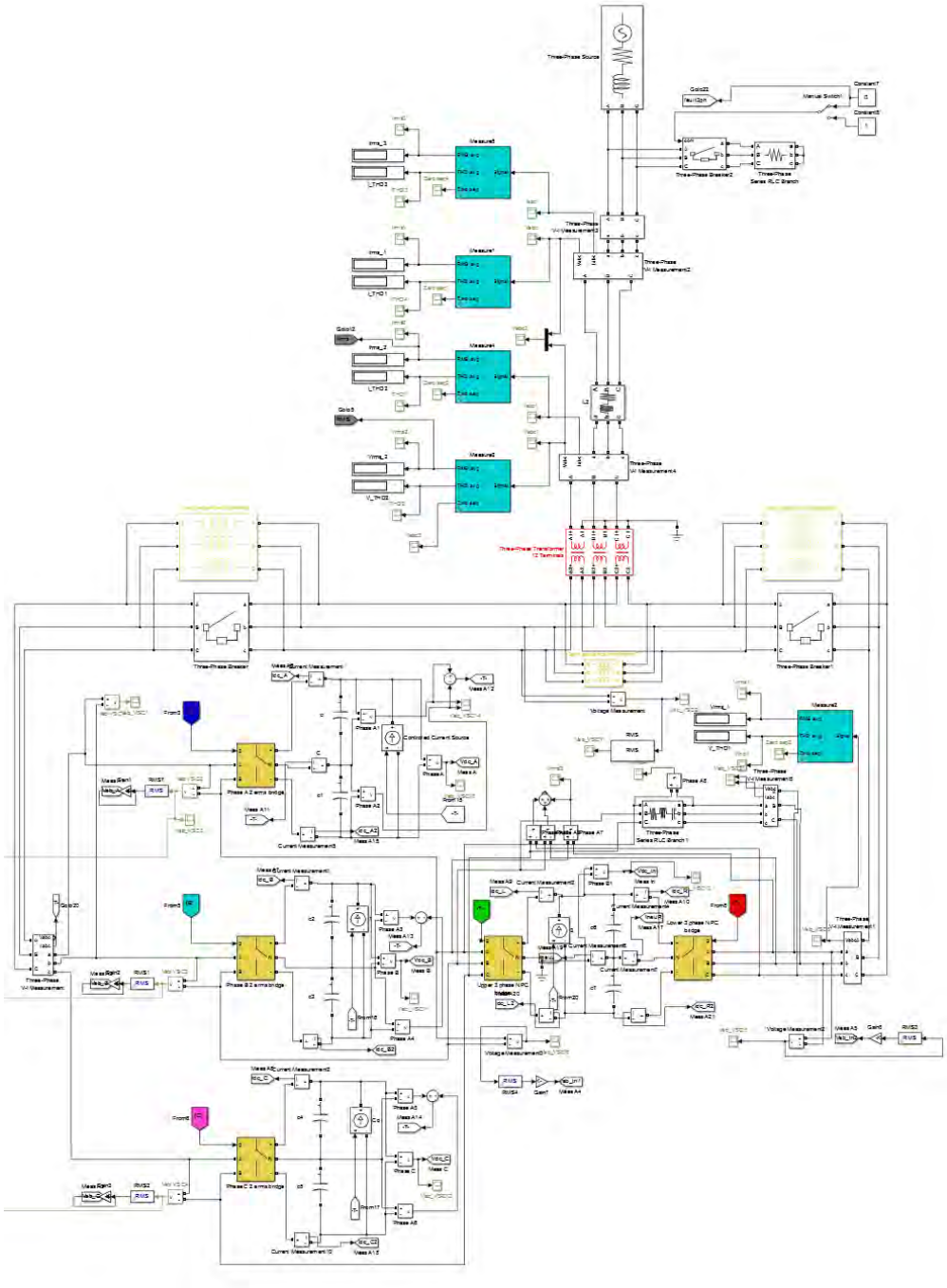

Figure A.7: Active and reactive power loops

A.8 Three-phase balancing circuit

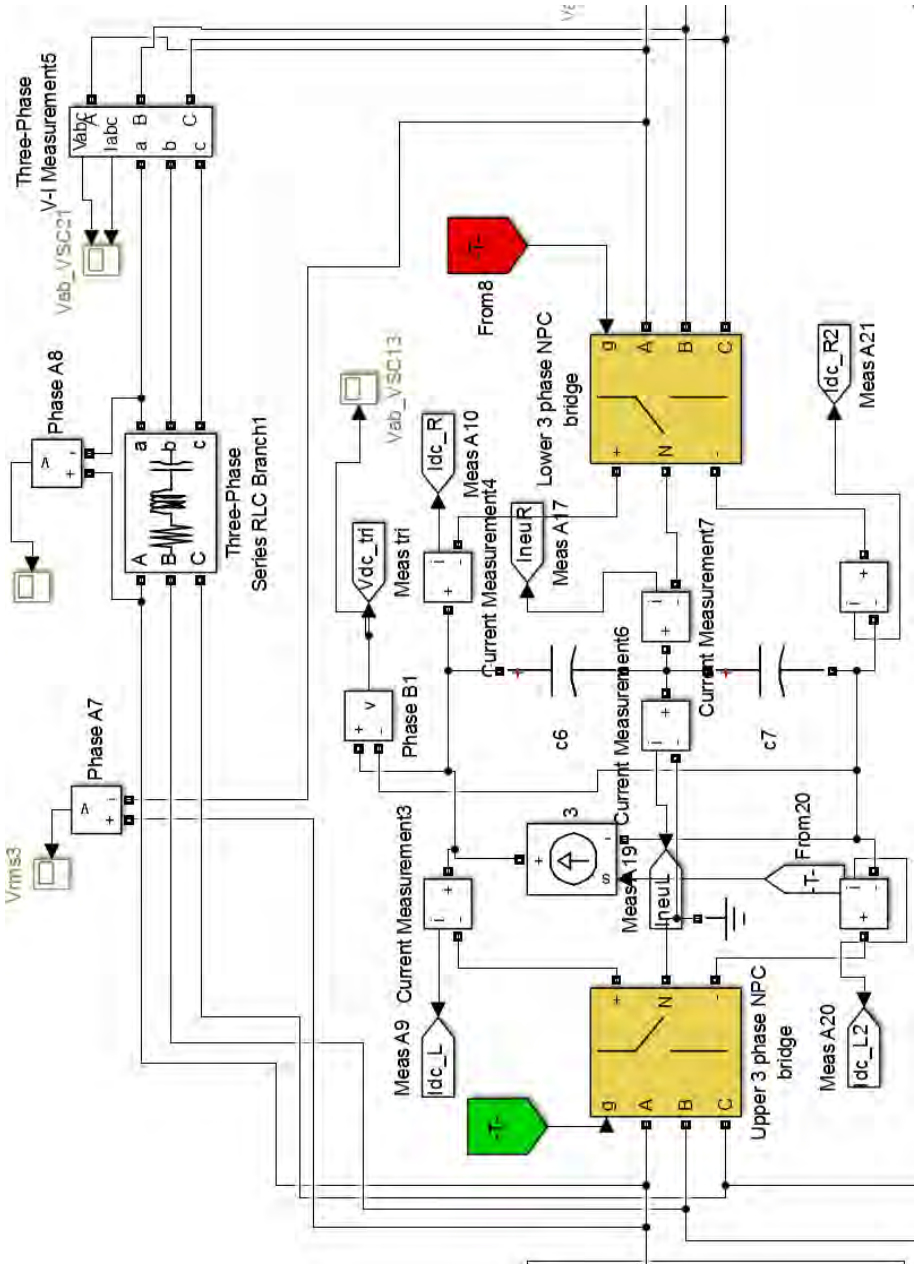

Figure A.8: Active and reactive power loops

A.9 single-phase balancing circuit

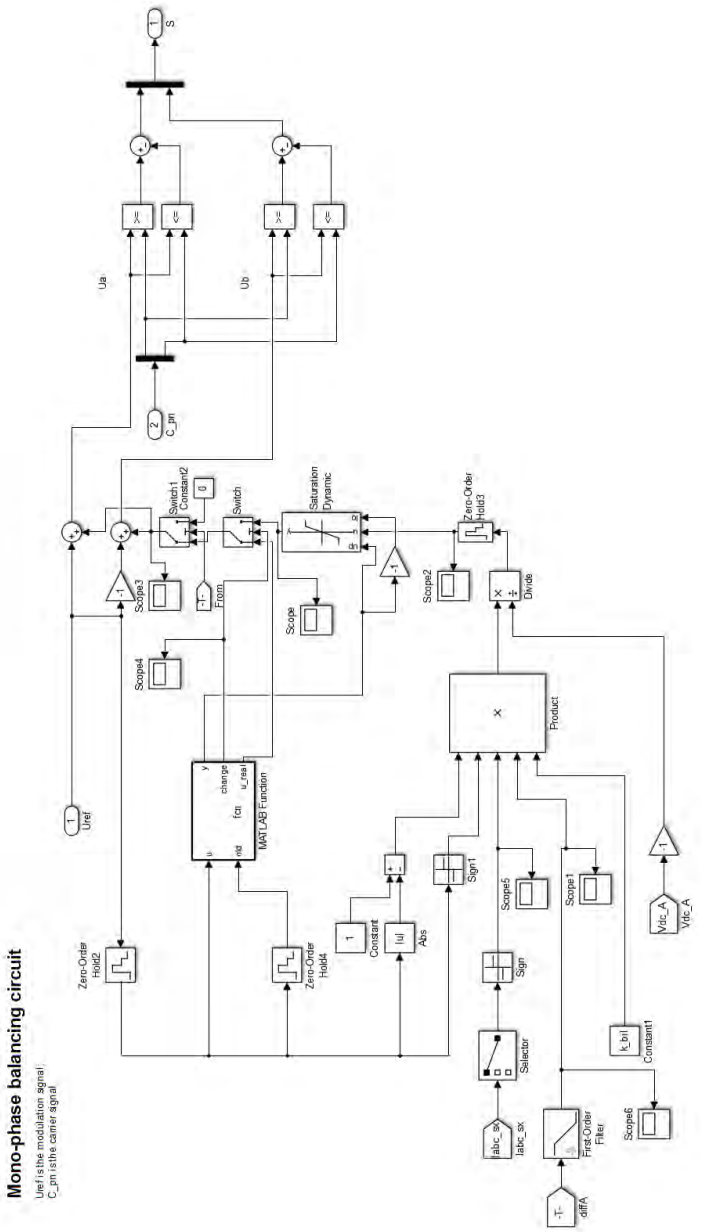

Figure A.9: Active and reactive power loops

Appendix B

Power transformer design

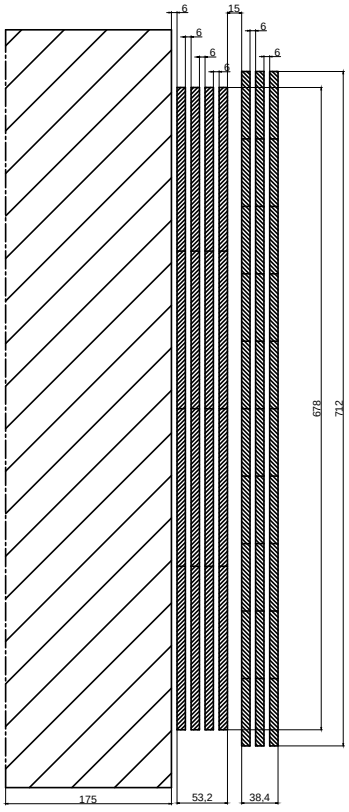

Figure B.1: AT and BT windings

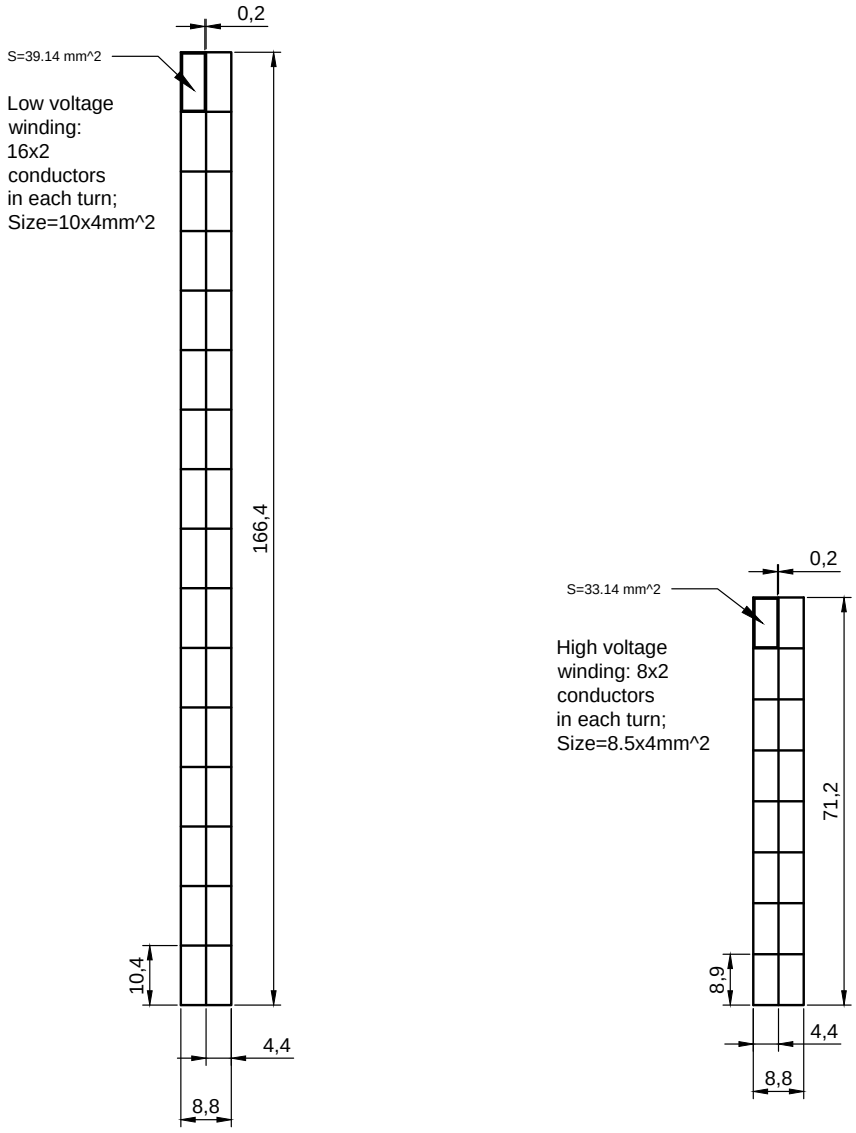

Figure B.2: AT and BT single turn section

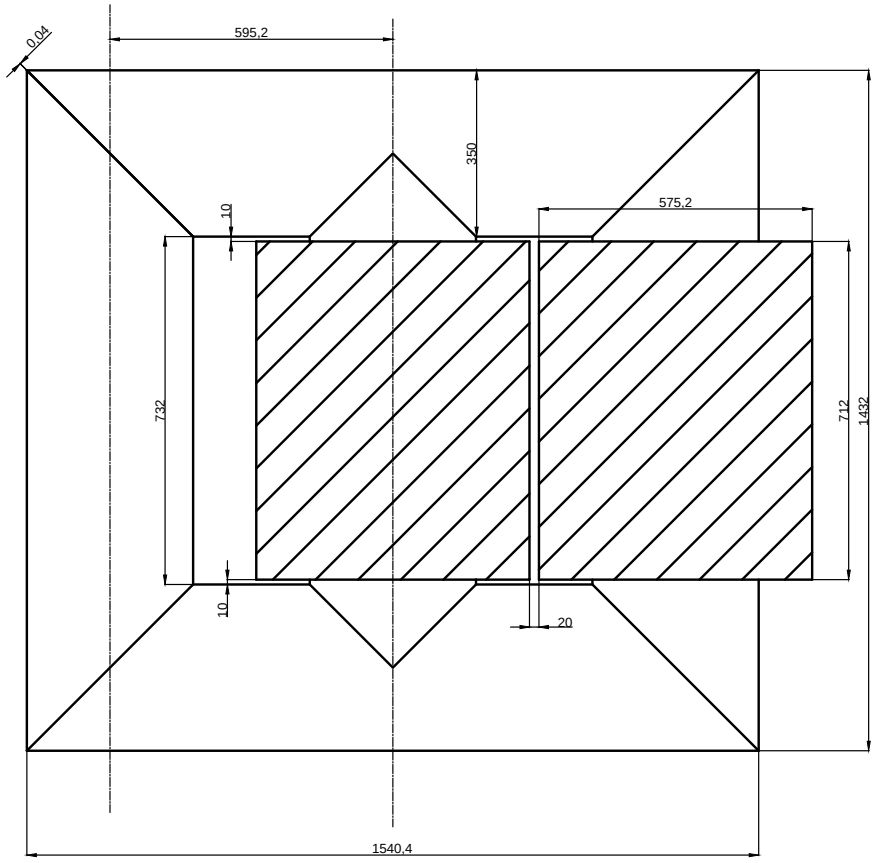

Figure B.3: Iron core design

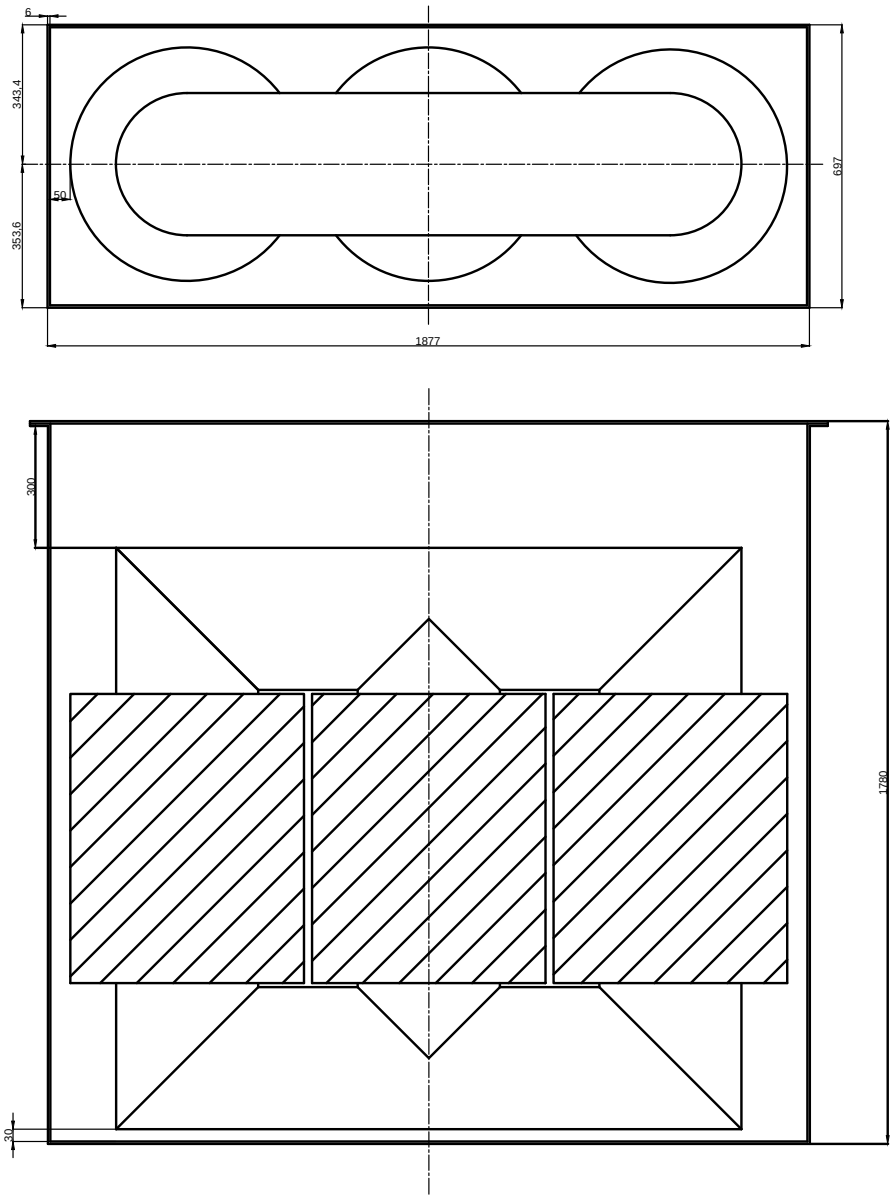

Figure B.4: External tank design