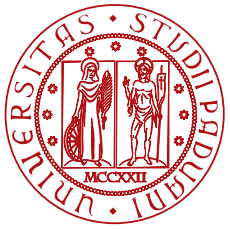

Università degli Studi di Padova

Dipartimento di Ingegneria dell'Informazione

Master Thesis in Electronic Engineering

Analysis and Simulation of the Vienna Rectifier Input Stage for American Market UPS: Overmodulation Control Technique

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Abstract (english version)

The purpose of this thesis is to present, step by step, the stages of research and development that took place during the realisation of a peculiar input stage, belonging to a UPS for the North American market, developed by Riello UPS s.p.a.
The system will be realised by exploiting the "Vienna Rectifier" circuit configuration, appropriately modified in order to realise a three-phase PFC without neutral, digitally controlled by means of an overmodulation control technique with third harmonic injection.
Starting from the project objectives, it will be reported the logic flux followed during the entire development of the system, analysing the performance generated by different types of digital controllers such as PI, PR and PIR through an analytical, simulation and experimental approach.
Different techniques that can be applied to implement the required overmodulation control will also be analysed, presenting progressively more optimal solutions.

Abstract (versione italiana)

Lo scopo di questa tesi è quello di presentare, passo passo, le fasi di ricerca e sviluppo susseguitesi durante la realizzazione di un peculiare stadio d'ingresso, appartenente ad un UPS destinato al mercato Nord americano, sviluppato da parte dell'azienda Riello UPS s.p.a.
Il sistema in questione verrà realizzato sfruttando la configurazione circuitale "Vienna Rectifier", appositamente modificata al fine di realizzare un PFC trifase senza neutro, controllato digitalmente tramite la tecnica di controllo in sovramodulazione con iniezione di terza armonica.
Partendo dagli obiettivi di progetto verrà presentato il flusso logico seguito durante l'intero sviluppo del sistema, analizzando le prestazioni generate da diversi tipi di controllori digitali quali PI, PR e PIR tramite un approccio analitico, simulativo e sperimentale.
Verranno analizzate, inoltre, diverse tecniche applicabili al fine di implementare il controllo in sovramodulazione richiesto, presentando soluzioni via via più ottimali.

Contents

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1 Introduction

In the run-up to the conclusion of my university course I had the opportunity to spend a period as a trainee at RIELLO UPS s.p.a, a company belonging to the Riello Elettronica group, located near Legnago (VR). Leader in its sector in Italy, the company is permanently placed among the top 4 companies worldwide in technological research, production, sales and service of UPS (Uninterruptible Power Supply) systems. During my time as a trainee I had the opportunity to support the work carried out by numerous engineers on the realisation of a rather innovative project, within the Research and Development department. My contribution was based on the analysis, study and simulation of an input stage for a three-phase UPS without neutral, realised using the Vienna Rectifier configuration, digitally controlled via overmodulation control. The machine, which will have to ensure an output power of up to 67 $[kW]$, will then be destined for use and sale in North America territory.

What follows is intended to represent a method of approaching the problem, starting from the analysis of the objectives up to the realisation of the entire machine in the company's own laboratory, supporting the entire work through the realisation of a simulative model capable of predicting the operation of the machine, supported of course by the usual analytical approach.
The aim of this experience was therefore to study the feasibility of the project, to build a simulative model on which to test different types of digital voltage and current controls like PI, PR and PIR, and then to verify the performance offered by an overmodulation control, realised through the injection of a third

harmonic of current into the system.
The purpose of the simulation will also be to support the theoretical study of the system's behaviour when subjected to non-ideal grid conditions, according to North American standards, such as the presence of unbalanced and distorted grid voltages. The system will have to be supplied by the North American three-phase grid at 480 $[V_{RMS}]$ concatenated, producing a DC voltage of 760 $[V]$ and capable of supplying up to 67 $[kW]$ of output power.
The employment of an overmodulation control would let the company exploit the same hardware already used for other UPS machines, destined for the European market, thus allowing optimal operation even at higher line voltages, such as North American ones; the alternative would involve modifying the existing hardware, requiring the use of some capacitors with such high capacitance and working voltages that they would be too expensive, as well as being practically unavailable on the market.
Having thus defined the project objectives, a brief summary of the contents covered in each chapter will now be provided.

Leaving aside this brief introductory section, **Chapter 2** will initially present the main issues that can affect a generic electrical power supply network, drawing some conclusions about the protections that each UPS must have. This will be followed by a general discussion of UPS systems, in order to take a closer look at the system under consideration, and then conclude the section with an analysis focused on the standards and characteristics that distinguish North American power supply systems, in order to make initial design choices.

Chapter 3 will present the discussion on the choice of the most suitable simulator to use, then presenting the main advantages offered and the major strengths that distinguish it.

Chapter 4 deals instead with the analytical/design study concerning the analogue typology under consideration Vienna Rectifier, suitably modified in order to allow overmodulation control. Finally, some transfer functions inherent to the circuit will be derived, thanks to the study using average models, which will be used in the next chapter.

Chapter 5 essentially reports the discussion related to digital control: after

introducing some study techniques, the performances offered by different types of controls such as PI, PR and PIR are tested through simulation. Two solutions inherent to the application of overmodulation are then advanced and tested: they will then be compared, finally making the respective design choices.

Chapter 6 conducts the analysis of the system when the latter is powered by a distorted line network: after presenting a theoretical study method, a proposed optimisation algorithm for implementing overmodulation is tested by simulation.

Chapter 7 shows instead some experimental results obtained in the laboratory. After presenting the test station, the trends of voltages and currents actually present in the machine during certain test conditions are shown, verifying the correctness of what has been obtained by means of theoretical and simulation models; conclusions and bibliography then follow.

2

Generalities about UPS

2.1 Power Quality

As is well known, the quality of the mains voltage supplied by power distribution centers can be far from optimal: waveforms, frequency and RMS value of the electrical voltage present on our electrical power sockets may depend not only on the reliability of the distribution systems used by the power suppliers themselves, but also on the use to which the individual user may put it.
The term "Power Quality", coined for this purpose, is intended precisely to refer to the degree to which the power supply present at the various grid access points conforms to well-defined standard specifications.
The quality of the electrical voltage supplied may depend, as just mentioned, on very different factors, causing quite a few problems for those who connect to the network in case the latter is not optimal. Hostile environmental conditions, vandalism, malfunctions and failures concerning network circuit breakers or transformers, accidental breakage of power cables during the performance of civil works, local overloads, or simply possible failures of switchboards and equipment already connected to the public grid can greatly affect the quality of the voltage supply present, introducing harmonics into the network and generating dangerous distortions, sometimes even causing temporary interruption of the power supply.

As already mentioned, the individual user also has a certain responsibility regarding maintaining high power quality of the network. An example of misuse

of the public network could be provided by the intention to power a small load by connecting it directly to the home network, for example using a simple diode bridge as a voltage rectifier. The number of harmonics introduced into the network by the latter would become a problem, since the rectifier certainly cannot be considered ideal, thus generating non-sinusoidal voltage drops along the line due to the absorption of impulsive current provided by the simple voltage rectifier, and thus distorting the voltage present in the various network access points.

A conscious use of public power supply is not only mandatory, but also well regulated by specific laws regarding the injection of harmonics (and not only) into it. Despite this, a conscious use of the network does not ensure correct maintenance of good power quality: starting of three-phase and single-phase motors, major load changes, switching on and off of industrial and office machinery such as refrigerators, coolers, elevators, medical equipment etc. can temporarily introduce serious reductions in the quality of the public network, making it almost impossible to keep the latter unchanged when used.

Clearly, the use of a variable and distorted electricity grid, therefore suffering from low power quality, can lead to serious problems including:

- Malfunctions and data loss;
- Damage to sensitive electronic equipment;
- Service and production interruptions;
- Overheating of cables and components (caused, for example, by circulation of harmonics in neutral cables in three-phase systems);
- Reduction in estimated life time, degradation and breakage of powered electrical components and systems;
- Higher maintenance costs and reduced reliability in grid-powered electrical systems.

Suffice it to say that, according to a study conducted in 2008 by the global community for professional sustainable energy "Leonardo Energy", the average industrial cost attributable to the low power quality of the grids was estimated to be around 4% of turnover, costing the European economy up to 150 billion euros per year. Currently, thanks to the introduction of more stringent laws, the situation seems to have improved slightly; however, no new studies have been

conducted in this regard.

It is therefore clear why it is so important to set up a reliable power grid, which presents the highest possible power quality. It is essential to know how to recognize and catalog the effects that contribute to lowering the quality of the grid, in order to be able to find a reliable solution in the case of poor power quality.

Standard 1159-1995 provided by the IEEE has made some clarity regarding the proper nomenclature to be used to refer to various power quality issues. These are categorized into 7 macrocategories, including:

- Transient;
- Short duration variations;
- Long duration variations;
- Voltage imbalance;
- Waveform distortion;
- Voltage fluctuations;
- Power frequency variations.

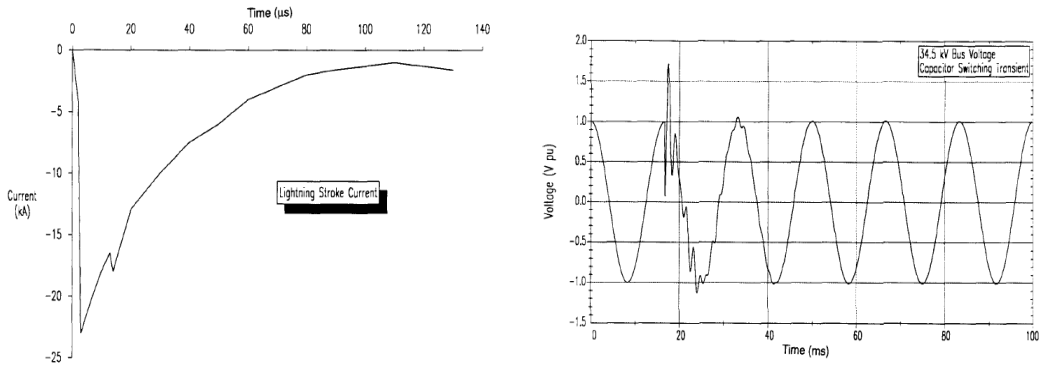
Each macrocategory is divided into further subcategories according to the duration, amplitude and harmonic content related to each electromagnetic phenomenon, as visible in the table shown in Figure 2.1. For completeness, some examples relating to the most common electromagnetic phenomena listed in this table have been reported below.

Categories	Typical spectral content	Typical duration	Typical voltage magnitude
1.0 Transients			
1.1 Impulsive			
1.1.1 Nanosecond	5 ns rise	< 50 ns	
1.1.2 Microsecond	1 μs rise	50 ns–1 ms	
1.1.3 Millisecond	0.1 ms rise	> 1 ms	
1.2 Oscillatory			
1.2.1 Low frequency	< 5 kHz	0.3–50 ms	0–4 pu
1.2.2 Medium frequency	5–500 kHz	20 μs	0–8 pu
1.2.3 High frequency	0.5–5 MHz	5 μs	0–4 pu
2.0 Short duration variations			
2.1 Instantaneous			
2.1.1 Sag		0.5–30 cycles	0.1–0.9 pu
2.1.2 Swell		0.5–30 cycles	1.1–1.8 pu
2.2 Momentary			
2.2.1 Interruption		0.5 cycles–3 s	< 0.1 pu
2.2.2 Sag		30 cycles–3 s	0.1–0.9 pu
2.2.3 Swell		30 cycles–3 s	1.1–1.4 pu
2.3 Temporary			
2.3.1 Interruption		3 s–1 min	< 0.1 pu
2.3.2 Sag		3 s–1 min	0.1–0.9 pu
2.3.3 Swell		3 s–1 min	1.1–1.2 pu
3.0 Long duration variations			
3.1 Interruption, sustained		> 1 min	0.0 pu
3.2 Undervoltages		> 1 min	0.8–0.9 pu
3.3 Overvoltages		> 1 min	1.1–1.2 pu
4.0 Voltage imbalance		steady state	0.5–2%
5.0 Waveform distortion			
5.1 DC offset		steady state	0–0.1%
5.2 Harmonics	0–100th H	steady state	0–20%
5.3 Interharmonics	0–6 kHz	steady state	0–2%
5.4 Notching		steady state	
5.5 Noise	broad-band	steady state	0–1%
6.0 Voltage fluctuations	< 25 Hz	intermittent	0.1–7%
7.0 Power frequency variations		< 10 s	

Figure 2.1: Categories and typical characteristics of power system electromagnetic phenomena.

Transients

Transients are probably the most dangerous type of electromagnetic disturbance we can encounter, and can be subdivided into impulsive and oscillatory. The former can be subcatalogued according to the duration of the transient, while the latter are subcatalogued according to the frequency of oscillation involved.
Impulsive phenomena are usually characterized by very short and huge increases in amplitude of the affected signal, both in current and voltage.
The most common causes capable of generating such transients are lightning strikes, use of poor grounding systems, switching of inductive loads and electrostatic discharges; Figure 2.2 (a) shows a typical impulse current induced on a conducting structure due to the electromagnetic field generated by a lightning strike.
Oscillatory phenomena, instead, can occur when turning off an inductive or capacitive load, such as a motor or capacitor bank, obviously as a result of a resonance phenomenon; we can alternatively also find them within distribution lines as a result of ferroresonances or transformer energization.
In Figure 2.2 (b), for example, a low frequency oscillatory transient caused by capacitor-bank energization is shown.

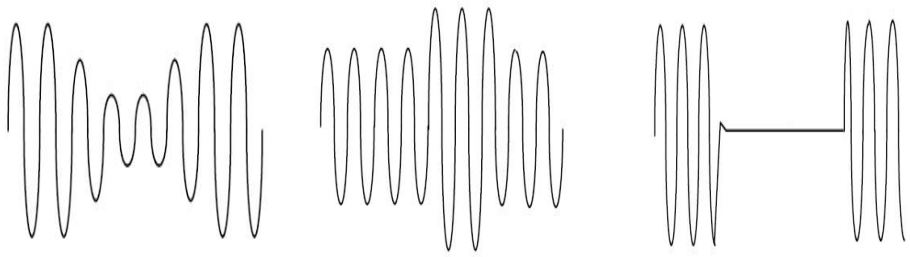


(a) (b)

Figure 2.2: Lightning strike current (a); low frequency oscillatory transient caused by capacitor-bank energization (b).

Short duration variations

This type of interference is characterized by a temporary lowering (sag) or raising (swell) of voltage or current levels, usually of relatively short duration (maximum 1 minute). Major load changes or single line-to-ground-fault can cause this type of interference.
Also included within this category are temporary interruptions, also lasting up to 1 minute, characterized by a total absence of voltage from the grid.
Temporary interruptions can occur as a result of system or equipment failures, or control malfunctions; we find a few examples in Figure 2.3.

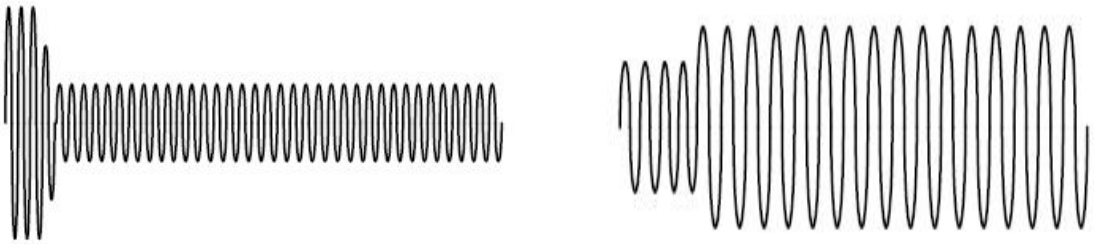


(a) (b) (c)

Figure 2.3: Example of instantaneous sag (a), instantaneous swell (b) ed instantaneous interruption (c), according to the summary table.

Long duration variations

This category of interference contains the same types of disturbances found in the previous point, whose durations, instead, persist beyond a single minute. The "sag" and "swell" phenomena that persist beyond a minute are called, relatively, "undervoltage" and "overvoltage" (fig. 2.4). In this same category we also find the "permanent interruptions," known vulgarly by the term "blackouts" which can generate, of course, incalculable damage, if not properly handled, to all systems that for one reason or another can never be turned off.
Often, these kinds of problems are permanent and require manual intervention designed to solve the problem; they can occur as a result of serious damage sustained by the power grid and the causes of which can be determined by lightning, animals, generical faults or whatever else.



(a) (b)

Figure 2.4: Example of undervoltage; unlike the electromagnetic phenomenon "sag", this type of interference lasts longer than a minute (a); example of overvoltage (b).

Voltage Unbalance

This type of interference is characteristic of three-phase systems and represents the degree of imbalance between the three mains voltage lines, often caused by unbalanced single-phase loads connected along a three-phase power grid, supply of unbalanced three-phase loads, or the presence of different mains impedances along the power distribution system.
Working with unbalanced triplet causes quite a few problems for the equipment that needs this type of power supply: these network non-idealities should therefore be predicted and managed optimally.
This type of interference can be expressed and estimated in percentage form, as visible in the general table in Figure 2.1, through two different formulations, both used in the industrial world; the first exploits the definition provided by the American NEMA (National Equipment Manufacturers Association) given below:

$$\text{Voltage imbalance } \% = 100 \cdot \left(\frac{\text{max deviation from average voltage}}{\text{average voltage}} \right) \tag{2.1}$$

where "average voltage" represents the arithmetic mean obtained from the peak values (or RMS) of the three voltage (or current) phases, obtained following a temporal analysis performed on the three-phase network. However, the proposed equation is not optimal as it does not take into account the phase shift between the three voltage lines.
The second formulation, instead, which is more complete and more generic, requires carrying out some more calculations; below it is reported the so-called

"true definition" of Voltage imbalance:

$$\text{Voltage imbalance} = 100 \cdot \frac{|V_{inverseSequence}|}{|V_{directSequence}|} \tag{2.2}$$

the two terms present are calculated as the magnitude of the phasor sum of the three components belonging to the direct (or inverse) sequence, calculated by exploiting Fortescue's theorem applied to the phasor triplet of line voltage; the latter relationship will become clearer after discussing Fortescue's theorem within chapter 6.

Waveform distortion

In this category we can include all the cases where the line voltage waveform has a more extensive harmonic content than the single main harmonic. Taking the usual table shown in Figure 2.1 as a reference, we can divide this macrocategory into 5 microcategories, based on the type of distortion present:

- **DC offset**: the harmonic spectrum contains a zero frequency component in addition to the fundamental one;
- **Harmonics**: the harmonic spectrum contains harmonics at multiple frequencies of the fundamental;
- **Interharmonics**: the harmonic spectrum contains harmonics at frequencies that are not multiples of the fundamental;
- **Notching**: the main harmonic is superimposed by a periodic impulsive transient; the harmonic spectrum will have at least one harmonic more than the fundamental;
- **Noise**: the fundamental harmonic is superimposed on a random fluctuation of signals spanning the entire harmonic spectrum of interest.

This type of phenomena can have very different origins, including powering nonlinear loads, powering devices having nonlinear characteristics, powering inductive motors or using both three-phase and non-three-phase power converters. A particular characteristic of these disturbances is that they do not possess short durations, as they are usually generated by the operation of certain electrical machines connected to the grid; therefore, these disturbances can persist over

time, lowering the quality of the public power supply network for an indefinite period.

(a) (b)

Figure 2.5: Example of notching superimposed on the main harmonic (a); example of harmonic distortion: being a purely periodic signal, it cannot be associated with distortion via interharmonics, as the spectrum will only be composed of whole harmonic multiples of the fundamental (b).

Voltage fluctuations

A voltage fluctuation is a systematic variation of the voltage waveform or a series of random voltage changes, of small dimensions, namely 95 to 105% of nominal at a low frequency (fig. 2.6). To quantify the fluctuation present, one can express the RMS value of the disturbance component as a percentage of the RMS value of the fundamental; arc furnaces connected to the grid are the main generators of this type of grid non-ideality.

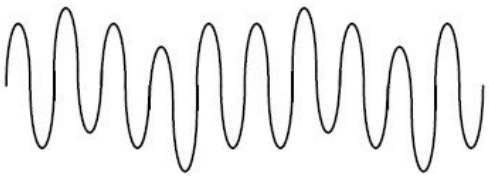


Figure 2.6: Example of Voltage fluctuation.

Power frequency variations

Frequency variation (fig. 2.6) is extremely rare in stable utility power systems, especially systems interconnected via a power grid; by using an isolated voltage generator the chance of running into this kind of problem may become slightly higher. This type of disturbance is quite rare to encounter since frequency variations generally occur as a result of momentary changes in the rotational speed

of power generation systems, but thanks to new generation of transmission systems the possibility of this happening is drastically reduced.
However, this possibility must be taken into account and handled appropriately: problems of this type can generate any kind of malfunctions since the timing naturally marked by the supply voltage waveform is altered.

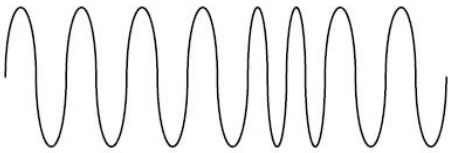


Figure 2.7: Example of frequency variation.

2.2 What is an UPS

As a result of what was reported in Section 2.1, it becomes clear that the power supply line carries with it some disadvantages in terms of reliability and quality. The quantity and vastness of power quality problems that can affect the network, being so various from each other, make it difficult to find a simplistic solution capable of ensuring safe and reliable operation for whatever type of load we want to supply. Thus, an ingenious, purpose-built solution was born: the **UPS**.

A UPS (Uninterruptible Power Supply) is an electrical equipment that acts as an interface between the mains power supply and a generic load that is to be powered: its job is to provide a clean, stable and well-regulated power supply, reducing as much as possible the effects resulting from electromagnetic disturbances from the grid, while trying not to affect the quality of the mains voltage to which it is connected.
Different types of UPSs have been made, according to the requirements of various users; in general, these machines constantly ensure a continuous source of power, even in the event of interruptions from the grid (a role from which the machine takes its name), eliminating totally or partially the remaining electromagnetic disturbances that may affect the Power Quality of the grid. The capability of filtering or not filtering out all the disturbances on the grid depends on the purpose of the machine itself.

In accordance with EN/IEC 62040-3 we can classify UPS, among other possibilities, according to the performance they are able to offer by drawing up three different categories:

- Voltage and Frequency Dependent (VFD);
- Voltage Indipendent (VI);
- Voltage and Frequency Indipendent (VFI).

Following will briefly explain the characteristics of each type before delving into the one we are concerned with.
VFD UPSs (fig. 2.8) are the worst performing, being incapable of stabilizing either the voltage or the output frequency: they simply filter the line voltage

and protect the load from possible overvoltages, by connecting the latter to the grid through a dedicated EMI/RFI filter.
Like all UPSs, in the occurrence of power interruption, it ensures a continuous supply to the load through the use of an internal inverter powered by a battery, also internal, which is charged by a dedicated voltage rectifier; this type of UPS is clearly not suitable for particularly problematic networks.

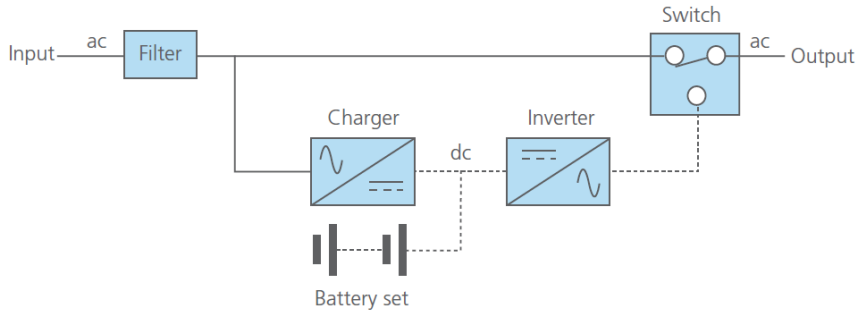


Figure 2.8: Basic structure of a VFD UPS, also called "OFF-Line" UPS.

VI UPSs (fig. 2.9), in contrast, offer a few more advantages over the previous category, allowing instantaneous regulation of the output voltage by means of an AVS[1]. The latter constantly monitors the supply voltage present on the load, going on to compensate it through the use of a battery-powered inverter, as in the previous case. Again, there is no possibility of adjusting the frequency of the output voltage since it is set by the grid itself.

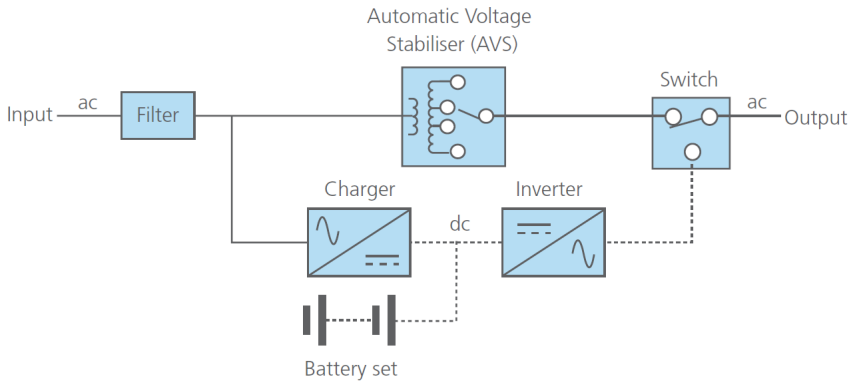


Figure 2.9: Basic structure of a VI UPS, also called "Line-Interactive" UPS.

[1]Automatic Voltage Stabiliser.

VFI UPSs (fig. 2.10), by contrast, are the most complex and the most reliable: by using an input voltage rectifier, they continuously supply power to an internal inverter which, in turn, supplies power to the load. If the mains voltage drops out of some well-defined standard, the UPS will switch from "normal" to "stand-alone" mode of operation, powering the output inverter via the usual internal battery, rather than through the rectified mains voltage, keeping the load constantly supplied.
This type of UPS allows three major advantages in contrast to the previous two cases:

1. It allows both voltage and output frequency to be adjusted, being able to function as a frequency converter as well;
2. It continuously reconstructs the output voltage waveform rather than filtering the line voltage waveform through the use of input filtering: this ensures the total absence of disturbances conducted from the line to the load;
3. Its internal structure allows for *instantaneous* switching when passing from inverter to battery, unlike the previous two types which require a few milliseconds to switch from one operation to the other: it maintains, therefore, a very high quality of power supply against any type of load.

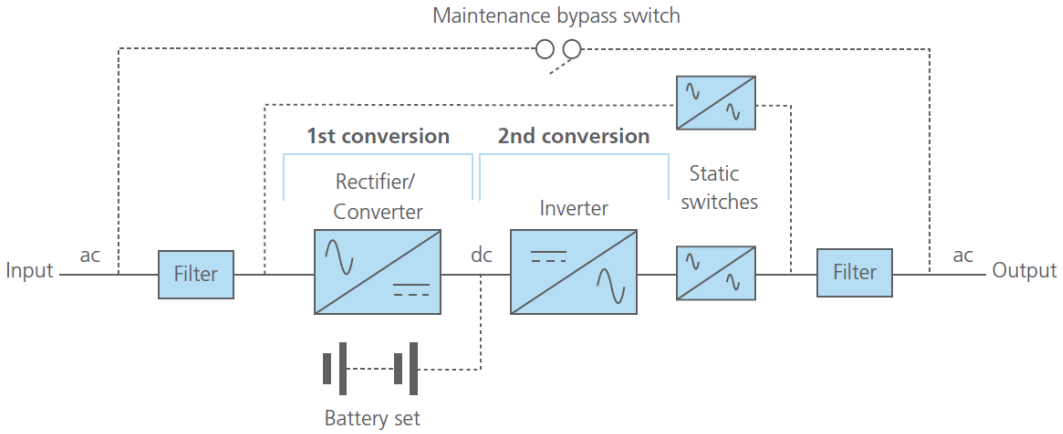


Figure 2.10: Basic structure of a VFD UPS, also called "On-Line" UPS.

It is interesting to analyze, in more detail, the essential blocks that make up UPSs belonging to the latter type: the machine we are going to develop during this study falls right into the category of VFI (On-Line UPS).
The three main blocks that make up a UPS are, undoubtedly, the input AC/DC converter, the battery set and the output inverter. The remaining blocks shown

in Figure 2.10 represent the input filters and the various overcurrent protections, the switches used to shift from one mode to another and the bypass switch, used to perform various types of maintenance without having to forcely disconnect the load from the grid, before being able to act on the UPS itself.

Input AC/DC converter

The input stage is undoubtedly a fundamental part of the UPS: it, regardless of whether it is contained within a single-phase or three-phase UPS, is realized through some type of PFC[2] chosen specifically.
As mentioned earlier, numerous norms regulate the amount of harmonics and electromagnetic disturbances that any device connected to the grid can inject into it, in order not to further degrade the power quality of the grid to which it is connected. UPSs must obviously also comply with these norms: the choice of using a PFC as an input stage becomes, therefore, mandatory.
A PFC is a particular type of AC/DC converter usually composed of a rectifier block, such as a diode bridge, followed by a power converter (buck, boost, flyback, etc.); the input stage of UPSs usually exploits a boost topology.
The peculiarity of PFCs is to force, through a certain type of current/voltage control, a current draw that is as proportional as possible to the voltage present at the input to the rectifier block, instant by instant, even if the latter should be distorted. This allows the PFC to operate as a voltage rectifier, while generating and injecting as few harmonics as possible within the network, behaving as much as possible as a linear load.
The latter is an obvious, but at the same time fundamental concept, and needs to be emphasized in order to be able to produce a high-quality product: if the supply voltage is distorted, the current drawn must also be distorted. This not only allows it to behave as a purely resistive load and therefore not distorting the grid itself, but at the same time avoids requiring obviously unused reactive power from the load, reducing the net amount of current that has to flow in the grid.
The PFC was created precisely to optimize these last two concepts: as a result, the apparent power recalled by the load is minimized, resulting almost only composed by active power; this concept can be expressed mathematically by

[2]Power Factor Corrector.

referring to the concept of *Power Factor* (PF), from which the PFC itself takes its name.

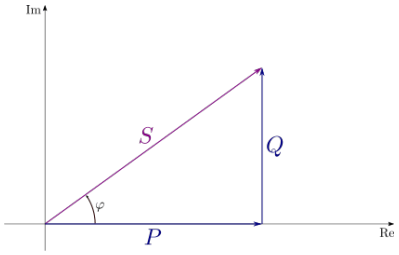


Figure 2.11: The triangle of powers.

The power factor is a dimensionless figure of merit, apt to measure how efficiently electrical energy is transmitted between a source and load connected to the grid itself. From another point of view, it quantifies the degree of proportionality that exists between the voltage and current waveforms feeding a given load, by using a numerical value between 0 and 1.
We can, in this regard, refer to the "triangle of powers" shown in Figure 2.11: denoting the amount of electrical power actually circulating in the network by the name of apparent power, we can exploit phasor theory in order to represent the latter by means of the modulus of a complex vector, having as its real part the active power absorbed by the resistive component of the load, using instead the reactive power, stored in the reactive components of the load, as its complex component, thus enabling us to write the relationship:

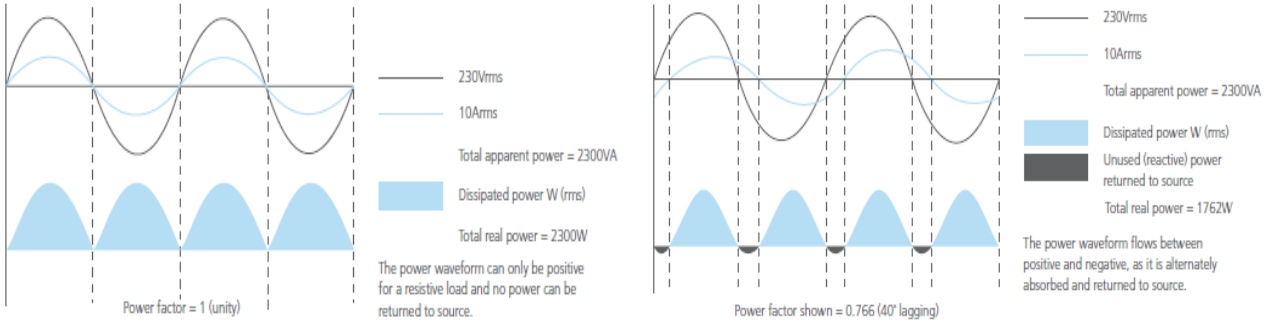
$$\dot{S}\ [\text{VA}] = \text{P}\ [\text{W}] + j\ \text{Q}\ [\text{VAR}]$$

Taking this into account we can then express the concept of Power Factor, associated with a given load, by means of the following relation[3] :

$$\text{PF} = \frac{P}{|\dot{S}|} = \frac{P}{S} = \frac{\text{average power}}{(\text{rms voltage}) \cdot (\text{rms current})} \tag{2.3}$$

Figure 2.12 makes the concept easier to understand: in both images shown there are the voltage and current waveforms powering a 2300 [VA] load; the first has a unity PF, the second has $PF = 0,766$.

[3]Mathematically speaking, it is correct to distinguish complex power $\dot{S}$ from apparent power S: the former is rappresented through a complex vector, while the latter represents its magnitude.



(a) (b)

Figure 2.12: Example of purely resistive load: the PF, in this case, is unitary (a); example of partially inductive load: by absorbing reactive power as well as active power, the PF becomes less than unity (b).

Looking at the preceding figures it is clear that PF is intrinsically related to the phase shift present between voltage and circulating current; denoting the latter by ϕ $[rad]$, in the case of a non distorting load, we can write:

$$\mathrm{PF} = \frac{P}{S} = \frac{V_{1_{RMS}} \cdot I_{1_{RMS}} \cdot \cos(\phi)}{V_{1_{RMS}} \cdot I_{1_{RMS}}} = \cos(\phi)$$

In the case of a distorting load, instead, assuming we have a perfectly sinusoidal voltage to feed the latter with, we can write:

$$\mathrm{PF} = \frac{P}{S} = \frac{V_{1_{RMS}} \cdot I_{1_{RMS}} \cdot \cos(\phi)}{V_{1_{RMS}} \cdot \sqrt{I_{1_{RMS}}^2 + \sum_{k=1}^{\infty} I_{k_{RMS}}^2}} = \frac{\cos(\phi)}{\sqrt{1 + THD^2}}$$

the summation present in the denominator obviously represents the sum of the square RMS current values, belonging to the various current harmonics generated by the load itself.
This last relationship is a proof of what was said earlier: the fact that voltage and current are not proportional to each other (i.e. current contains harmonics that voltage does not contain) lowers the PF of the load itself. If the supply voltage contained the same harmonics as the current, i.e. if the load were perfectly linear, the PF would return to being unity.

The previous relationship also allows us to introduce an additional figure of merit that is essential regarding the characterization of a good PFC: this is the Total Harmonic Distortion (THD).

This fundamental dimensionless parameter is used, in this case, to express the degree of harmonic distortion generated by a generic electrical device under analysis. Feeding the latter by a perfectly sinusoidal voltage waveform, in fact, the degree of non linearity of its input characteristic will generate a certain number of current harmonics; obviously, if the load were supposed to be perfectly linear, only the first current harmonic will be generated.
It is then possible to define this parameter, which will be useful later, as follows:

$$\mathrm{THD} = \sqrt{\frac{\sum_{k=1}^{\infty} I_{k_{RMS}}^2}{I_{1_{RMS}}^2}} \tag{2.4}$$

also expressible in other forms such as the following, expressed in [dB]:

$$THD_{dB} = 20 \cdot \log \sqrt{\frac{\sum_{k=1}^{\infty} I_{k_{RMS}}^2}{I_{1_{RMS}}^2}} \; [dB] \tag{2.5}$$

Output inverter

The output inverter is certainly another fundamental block for any UPS: in On-Line UPSs, unlike the other two types, the inverter works continuously generating the sinusoidal waveform required to power the load. This operation is digitally controlled by PWM, appropriately driving the various IGBTs that make the inverter leg itself (or the branches, in the case of three-phase inverters), thus generating a voltage signal that is subsequently filtered, in order to obtain the required sinusoidal voltage waveform at the output.
In addition, as already mentioned, On-Line UPSs have the possibility of exploiting the output inverter as a frequency converter: this feature gives them great versatility, allowing them to operate even in countries with grid standards different from those in Europe.

Battery set

The battery set certainly represents the third fundamental block of any UPS: the latter keeps the output inverter active in case of a lack of power from the mains, in case of particularly distorted and/or unreliable line voltage. A battery set may comprise of a single or multiple battery strings connected in parallel;

their autonomy depends on the type of UPS in which they will be installed.
One of the ways in which a UPS design can protect its battery set is to ensure the rectifier, or battery charger, presents a very low AC ripple. This is an AC component superimposed onto the DC output waveform of a rectifier, or battery charger, and designs strive to reduce this to the minimum. For a battery set, a high AC ripple can lead to increased battery temperature, speed up of corrosion of the positive plate and reduced battery working life.
Although the old machines had their batteries connected directly to the output of the input stage, thus forcing the use of very high capacitor banks in order to stabilise the output voltages as much as possible, nowadays a battery charger is practically always connected between the output bank and the batteries themselves. In this way, it is possible to avoid the use of capacitors with extremely high capacitance, while at the same time ensuring an excellent life expectancy for the battery set used.

2.3 UPS and North American grids

Having reported in some detail on the issues that can affect the quality of a generic electrical distribution network and illustrated how UPSs should behave, both normally and in the wake of unpleasant network mishaps, it is now appropriate to focus on the network standards present in the area of our interest and the various related issues, in order to be able to fix from the beginning the network specifications to which our product will have to submit.
The American electrical distribution system is quite peculiar: it presents network voltages and frequencies found almost only in the same American country, unlike almost all the rest of the distribution systems present in the world. Some network configurations present are found exclusively in certain areas of the territory, being subject to certain local standards that may, in turn, be different as one travels the entire American continent.
For this reason we will focus, below, on the network peculiarities present on North American soil, in view of the project we will have to carry out, focusing more on standards applied in the U.S.A., since the latter will be the main sales territory of interest for us. However, the discussion will also be extended to the major neighbouring countries, so that we can compare some standards similar to each other.

North America also presents a multitude of different distribution systems and standards: the motivation must be sought in historical aspects, in the breadth and vastness of the territory itself and in the great distance usually present between energy generation centers electricity and the major consumption centers of the same.
Numerous electrical standards have been presented throughout history in order to standardize the North American territory as much as possible. In view of our project we can find useful information by referring to the legislation ANSI C84.1-2011 "American National Standard for Electric Power Systems and Equipment - Voltage ratings (60 Hertz)", valid specifically for the U.S.A. territory, the CSA CAN3-C235-83 regulation, valid specifically for the Canadian territory and the NOM-001-SEDE regulation, valid specifically for the Mexican territory. These establish the power supply voltage values present in the relevant electrical distribution systems, presenting the operating ranges and related power quality problems that may be encountered in this regard.

It should be stressed, however, that although each American country uses very specific standards in this regard, often the differences present between one and the other are not as clear-cut as one might think: clearly, aligning one's own standards with international ones brings many advantages, ensuring for example the compatibility of imported electrical equipment and facilitating trade with neighboring countries.

Focusing on the low-voltage power systems referred to in the previous standards we can mention, expressed in RMS value, some of the most commonly used voltage standards in major North American countries:

- 120 $[V]$ for single phase grid (127 $[V]$ for Mexico);
- 208 $[V]$ for large power consumers (three-phase);
- 240 $[V]$ for industry (bi-phase);
- 480 $[V]$ for industry (three-phase);
- 600 $[V]$ for industry (three-phase, mainly present in Canada and Mexico).

In view of the project to be carried out, we are clearly interested in the use of the 480Δ $[V_{RMS}]$.
Another main feature which characterizes, however, almost all the countries in the American territory is the use of 60 $[Hz]$ in all grid power systems, unlike most of the rest of the countries of the world, which use the typical 50 $[Hz]$; this choice results from a combination of historical factors, pioneering decisions and technical considerations.
Having thus introduced the main frequency and voltage values used in the most common electrical distribution networks, found in the North American territory, it is worthwhile to investigate the operating ranges and the various tolerances provided by the same standards.
In this regard, the whole of North America allows the use of different tolerances regarding the rated voltage present on power cables, depending on the physical point of the network where we are going to make the voltage measurement.

We can distinguish, using the same definitions found in ANSI C84.1-2011 itself:

- **Service Voltage**: The voltage at the point where the electrical system of the supplier and the electrical system of the user are connected;
- **Utilization Voltage**: The voltage at the line terminals of utilization equipment.

We can right now define two different types of tolerances, belonging to two different types of ranges:

- **Ideal Range**: the tolerances within it must be applied to the average voltage level that we can encounter along the distribution lines;
- **Tollerable Range**: the tolerances within it must be applied to rare and exceptional cases, limited in time and not long-lasting, arising for example due to large voltage drops or heavy load fluctuations, which can occur due to lightly meshed networks combined with long transmission lines.

According to the limits set by each country within their own ideal Range we can conclude that, in the worst cases, the Service Voltage must be between 95% and 105% of the nominal voltage in question, while the Utilization Voltage can vary between 90% and 104%.
Clearly, the difference between the minimum value of one compared to the minimum value of the other depends on the voltage drops allowed along the conductors, which are also defined by specific standards.
Regarding the tolerable Range, instead, we can find a range of voltage values between 92% and 105.8% of the nominal voltage regarding the Service Voltage, while for the utilization Voltage we find values between 87% and 105.8% of the same.
The table shown in Figure 2.13 summarizes for simplicity what has been said.
In addition to the tolerances relative to the voltage amplitude values, that can be found at the various network access points, it is important to consider other non-ideality parameters; one of these is certainly the Voltage Unbalance parameter, the non-ideality factor presented in the previous chapter.
In this regard, using the equation 2.1 the U.S.A. and Canadian standard imposes a maximum value of Voltage Unbalance equal to 3 % when measured in a no-load condition.
According to research carried out by EPRI[4] on the Voltage Unbalance percentages present in the Canadian and U.S.A. distribution networks, the regulations

[4]Electric Power Research Istitute.

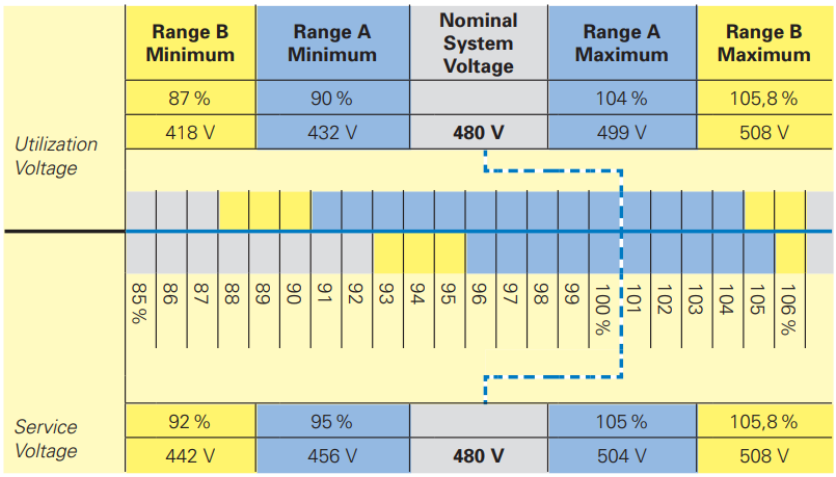


Figure 2.13: Service Voltage and Utilization Voltage tolerances, using as a reference the industrial voltage 480 $[V]$ at 60 $[Hz]$.

would seem to be almost totally respected: the data show that about 98% of the electricity distribution lines taken into consideration show a value of less than 3%, while about 66% of the same samples show a value of less than 1%.
Regarding, instead, the Voltage Fluctuation values encountered at the various points of access to the network, the situation is rather problematic: although the majority of users report a value lower than 3% (value calculated following the explanation given in the specific paragraph), about 10% of them report Voltage Fluctuation values higher than 7%, even going beyond the tolerable ranges presented above.
The harmonic content present in the network must also be clearly regulated; the 519-2014 standard provided by the IEEE, recognised in all three of the countries examined, clearly defines the methods used to measure the harmonic content present on a generic power line, also establishing the relative limits. Analysing the same document we find the two tables shown in Figure 2.14 which list the accepted limits of harmonic distortion: focusing on the power systems of interest, having nominal voltage less than 1 $[kV]$, the voltage THD measured at the PCC[5] must be less than 8%, on condition that each voltage harmonic present has a maximum amplitude equal to 5% of the amplitude of the main harmonic. As regards the number of current harmonics that can be injected into the network by the individual user, reference can be made to the table 2.14 (b): in this

[5]Point of Common Coupling: represents the point at which the single electrical equipment is connects to the public distribution network.

Table 1—Voltage distortion limits

Bus voltage V at PCC	Individual harmonic (%)	Total harmonic distortion THD (%)
$V \leq 1.0$ kV	5.0	8.0
1 kV $< V \leq 69$ kV	3.0	5.0
69 kV $< V \leq 161$ kV	1.5	2.5
161 kV $< V$	1.0	1.5[a]

[a]High-voltage systems can have up to 2.0% THD where the cause is an HVDC terminal whose effects will have attenuated at points in the network where future users may be connected.

(a)

Table 2—Current distortion limits for systems rated 120 V through 69 kV

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)[a, b]						
I_{SC}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
< 20[c]	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

[a]Even harmonics are limited to 25% of the odd harmonic limits above.

[b]Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

[c]All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.

where

I_{sc} = maximum short-circuit current at PCC

I_L = maximum demand load current (fundamental frequency component) at the PCC under normal load operating conditions

(b)

Figure 2.14: Measurable harmonic distortion limits at PCC, defined by the 519-2014 standard provided by the IEEE.

way each harmonic is cataloged within a well-defined category, with clearly defined limits. An interesting peculiarity that characterises North America is the disproportionate number of power supply networks, each different from the other, present within the same territory. Some of these configurations can only be encountered, among other things, in the North American territory: the various types that can be encountered are shown in Figure 2.15. Nowadays, the majority of the systems present are earthed; however, it is very common to use local earthing rather than a single distributed earthing system: this leads to the presence of different earthing potentials that can be found between the various locally realised points.

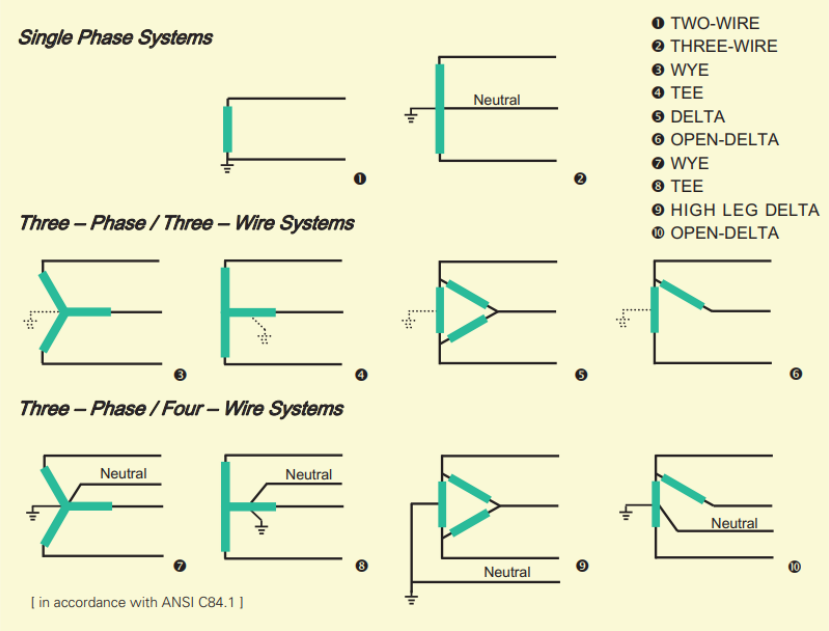
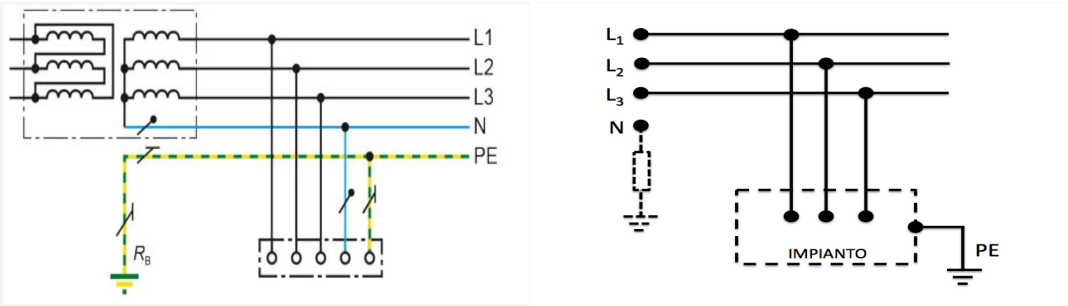


Figure 2.15: Supply networks encountered in North America, only the transformer supply secondary winding configurations are pictured. In connections (5) and (6) the ground may be connected to the midpoint of one winding as shown (if available), to one phase conductor ("corner" grounded), or omitted entirely (ungrounded). Single phase loads can be connected to single phase systems, or phase to phase in polyphase systems or, when available, between phase and neutral.

Clearly, the use of power systems with an earthing connection simplifies the use of protection systems, even though, as just mentioned, the use of IT-type distribution systems is not absent in North America, which do not provide any earthing conductor from the distribution system. This type of network has all active conductors separated from earth; alternatively a single point is connected to earth via high impedance. This clearly favours continuity of service, ensuring that the protection device does not respond in the presence of a first earth fault: the latter will be detected, signalled and handled as soon as possible, without interrupting the continuity of the electrical service.
For the sake of completeness, Fig. 2.16 shows some examples taken from three-phase IT-type systems, with and without neutral. Based on what we have seen so far, it is clear that the machine to be built will have to be able to operate by connecting to electrical networks with the characteristics just presented, while respecting certain limits, including those imposed by the number of current harmonics that can be injected into the network by the user.



(a) (b)

Figure 2.16: IT type system: three-phase power system with neutral, without connection to earth by the secondary transformer (a); three-phase power system without neutral, provided with connection to earth by means of a high impedance (b).

Observing Figure 2.15 it is clear that, since a three-phase system without neutral is to be realised, our machine will have to be able to connect to network number 5, called Delta, which will present 480 $[V_{RMS}]$ concatenated.
As already announced, an overmodulation control technique will also be used in order to be able to physically control the PFC placed at the input, so as to be able to generate 760 $[V_{dc}]$ that can subsequently be used by the battery and the inverter. This technique, if rendered optimal, will allow us to work with distorted and/or unbalanced networks without losing control of the PFC itself, ensuring a certain margin of operation despite the fact that the network itself may be affected by possible power quality problems, according to the tolerances presented previously.
To achieve this we will rely on the use of a simulator, which will be presented in the next chapter, in order to develop and test the operation of the entire input stage of the commissioned UPS.

3

QSPICE: a new powerful simulator

The theoretical study that will be carried out on the system under consideration will have to be flanked and supported by some experimental results, which can be easily obtained through the use of an appropriate simulator. The choice of the most suitable simulator to be used must be made following a careful analysis of the objectives set during the project, in order to obtain satisfactory results that are consistent with our aims in the simplest possible way.
Among the various classes of existing simulators it is in fact possible to find:

- *Circuit simulators*: these are simulation environments dedicated explicitly to the resolution of electrical and electronic circuits, each of which may be particularly suited to the analysis of a particular branch of electrical systems such as integrated circuits, SMPS systems, purely digital systems, etc;

- *Numerical simulators*: these are software tools dedicated to scientific calculation that can also be used to create models of electrical and electronic circuits, easily reproducible through arbitrarily definable behavioral blocks or by exploiting classic matrix calculation; an example is provided by the scientific software Matlab, produced by the MathWorks company, which provides the Simulink package;

- *HIL simulators*[1]: these are tools that integrate the numerical simulation of circuit models, carried out in real time, with physical control systems of the analogue and/or digital type, making it possible to simulate certain parts of the electrical system without having to forcibly realise them.

[1]Hardware In the Loop

In our case we wanted to create a simulation model act to verify what the theoretical models predicted, obtaining a system capable of faithfully reproducing both the analogue and digital parts dedicated to control, showing in detail the trend of the quantities in play such as voltages, currents and digital signals. After careful analysis we chose to use the QSPICE circuit simulator, a powerful successor to the famous LTspice simulator, a decision supported by the numerous advantages it offers which will be illustrated below.

QSPICE is an analog and mixed-signal circuit simulator characterized by high simulation speed, accuracy and reliability developed by Qorvo, an American multinational company specializing in products for wireless, wired, and power markets. Based on the SPICE[2] engine, turns out to be particularly suitable for the simulation of not only integrated or purely analog circuits, but also power circuits such as the SMPS system of our interest, thanks to a series of interesting peculiarities and measures introduced in this new version.
In this regard, three main features determined the choice to use QSPICE, which will be discussed in more detail below:

1. Presence of digital blocks programmable in C++/Verilog language;
2. Use of the computer's internal GPU to accelerate simulations;
3. Improved simulation robustness compared to previous SPICE versions.

The presence of programmable digital blocks allows, in fact, to program the entire digital control of an SMPS system through a specific programming language: the simulator, in this regard, implements the Digital Mars C++ Compiler, offering the possibility of creating and programming the respective blocks digital in C++ language; alternatively it is possible to use a modified version of Snyder's Verilator, giving to the user the possibility to program the latter using the Verilog language.
Figure 3.1 shows an example of application provided by a test circuit present as a DEMO inside the simulator: the possibility of creating digital blocks capable of simulating logical parts and/or entire microcontrollers through a basic language programming makes it possible to create a project composed of mixed

[2]Simulation Program with Integrated Circuit Emphasis.

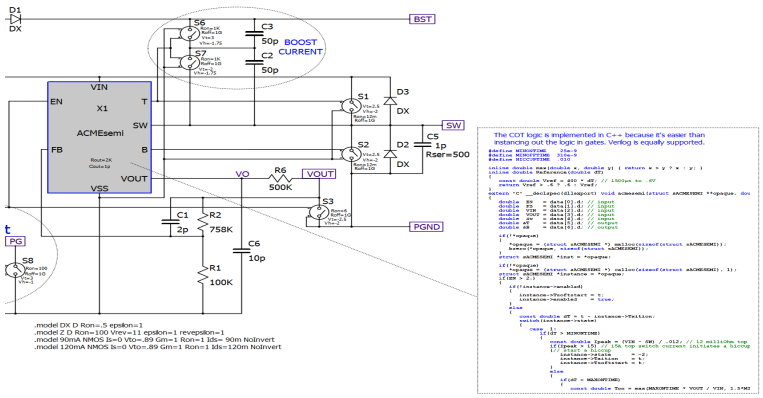


Figure 3.1: DEMO circuit contained within the simulator's test library: in addition to the possibility of drawing and inserting images on the schematic there is also the option of creating programmable digital logic blocks, which can be interfaced with an external analogue circuit.

signals like ours; the development of the assigned project will in any case take place using the C++ language rather than the Verilog language.
The use of the GPU as support for the simulation makes the simulator extremely fast compared to most previous SPICE versions, which only use the CPU to carry out the entire simulation. In general, circuit simulators make it possible to analyse the operation of a circuit through the resolution of countless equations, defined by the topology and the typology of the circuit under examination. Clearly, the required timing is also variable, among other reasons, depending on the number of operations the CPU has to perform, both those inherent to the simulator and those in the background.
On the contrary, the QSPICE simulator exploits, in parallel to the CPU, the performance offered by the GPU inside the computer: the latter, specialized in parallel calculation, excels in the execution of intensive numerical calculations, such as those required by simulations. This involves in a substantial increment of the performance offered by the simulator, managing to speed up the process dozens of times compared to conventional SPICE simulators.
In contrast, with regard to the increase in simulation robustness compared to previous versions it is possible to name, among many new features:

1. Elimination of discontinuities in the equations that describe the behavior of components and devices;

2. Updating of the numerical methods used;

3. Optimized timestep control;

4. Improvement of the accuracy of the results provided by some critical operations.

The elimination of the discontinuities, present in the I-V curves used to describe the electrical behavior of the various components, has certainly brought numerous advantages from different points of view.
Firstly, eliminating discontinuities makes the models obtained more realistic as, in the real world, there are no physical behaviors presenting abrupt discontinuities, as the latter can only be the result of mathematical approximations. Secondly, a higher computational efficiency was achieved, as any discontinuity requires a greater number of numerical iterations by the simulator before it can generate an accurate result.
It should also not be forgotten how discontinuities can be a source of numerical instability: eliminating them means increasing the robustness of the system by ensuring better numerical convergence, especially in the case of an SMPS system such as the one under consideration.
As regards, instead, of the numerical methods used by the simulator we can mention:

1. Trapezoidal integration (default);

2. Gear integration;

3. Backward Euler integration.

In this regard, the simulator uses, by default, a trapezoidal integration method based on the approximation of the integral calculus through the use of infinitesimal trapezoidal areas, a method closely linked to the Tustin approximation which will be introduced in the chapter 5.
The simulator then provides two further integration techniques that can be used: although the previous technique practically always generates reliable results it can, in certain cases, run into numerical oscillations, thus causing the famous "trapezoidal ringing", superimposing non-real oscillations on some signals while maintaining the correct mathematical calculation by means of their infinitesimal areas.
Using then alternative techniques, such as Gear integration, it is possible to mitigate these purely visual distortions through the insertion of artificial dissipative

elements within the calculation, in order to decrease parasitic ringing; however, for this reason, this technique provides less accurate results than the previous case. In any case, the simulator features an intelligent control of the timestep used in the simulations, which is skilfully exploited in order to reduce possible visual ringing effects when the trapezoidal integration method is used.
The possibility of using different integration methods at the user's discretion is however very useful, since if all three integration methods were to provide the same results this would mean that the latter could be considered reliable, as they are not affected by numerical errors or by artificial distortions.

As just mentioned, QSPICE incorporates a redesigned time step control system with respect to traditional SPICE simulators, thus providing accurate and efficient simulations. This is due to the fact that, through the use of rather complex algorithms, it is able to modify the measurement of the time step used during the simulation, reducing the discretization errors that can be generated at the most critical points and speeding up the simulation process in slower and monotonous processes. This makes the results produced more reliable, eliminates most of the artificial oscillations that can be generated and makes the simulation system faster and more efficient.
The improvement of the mechanisms used to manage and minimize the numerical errors, produced during the simulations, has then made the system even more reliable: for example, by modifying the integration methods and additional parameters used during the simulations, by merging the results obtained, using thresholds for the detection of errors and thus making the simulation system more elastic, with respect to the various events that can be analysed.
The simulator also offers a series of commands uniquely created for the study of SMPS systems, such as the ".bode" instruction, which allows to extract the open loop frequency domain response of a SMPS, operating in closed loop in the time domain via multiple disturbances; this is usable, for example, to study the stability of the system.

As a result of what has been presented we can expect very good performance from the QSPICE simulator, both in terms of reliability and processing speed. We are, then, finally ready to introduce the study of the system under consideration from the next chapter, being able to count on an excellent simulation system.

4 Vienna Rectifier

After a long introduction, the circuit topology called "Vienna Rectifier" will now be presented: this chapter will focus almost exclusively on the analysis of its electrical operation, going into greater depth on the control theory used in the following chapters.

4.1 Overview of Circuit operation

The Vienna Rectifier is a three-phase three-level unidirectional rectifier managed by PWM control, proposed for the first time by Professor Johann W. Kolar between 1993 and 1994, whose electrical configuration is shown in Figure 4.1. To better understand what it is about, it is convenient to derive its typology starting from a simple single-phase PFC boost, shown as an example in Figure 4.2 (a). The latter shows the electrical diagram belonging to a PFC boost, realized by means of a diode bridge and a classic boost converter connected in cascade. Clearly, the diode bridge rectifies the supply voltage, placing a pulsating voltage at the input to the boost stage: at this point, via a suitable driver connected to the gate of the MOSFET, a control network drives the latter via PWM control, by generating an average inductor current proportional to the shape of the input pulsating voltage, as mentioned in previous chapters.
In this type of circuit, therefore, the single boost converter operates by exploiting the contribution of both input voltage half-waves, positive and negative, where the latter is obviously rectified.
An alternative is shown instead in the figure 4.2 (b), which represents the single-

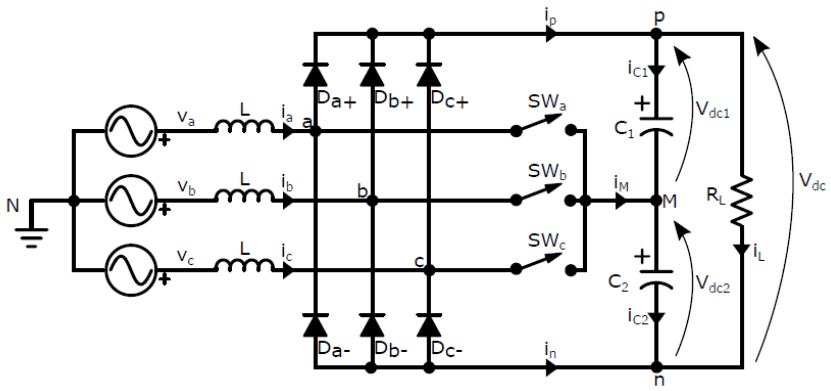
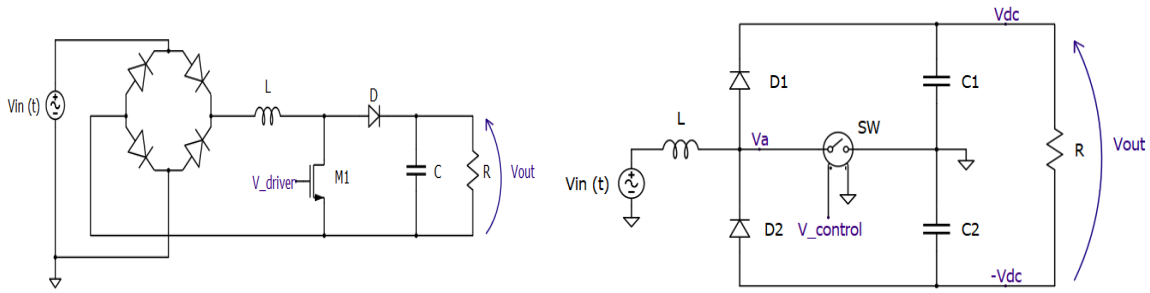


Figure 4.1: Vienna Rectifier: basic configuration.



(a) (b)

Figure 4.2: Single-phase PFC with rectified input voltage (a); Vienna Rectifier single phase (b).

phase counterpart of the same Vienna rectifier: the latter is realized using two boost converters, whose components have been rearranged in such a way as to use a single coil for both. Unlike the previous type, the first boost converter works only with the positive input voltage half-wave, while the second works only with the negative input voltage half-wave, avoiding the need to take advantage of a rectifier bridge. A single bidirectional switch used to control both boost converters is also shown in the relative image (we will see later how this can be realized); clearly, the general operation of the boost converters remains unchanged, which charge the inductor via the switch and discharge it through the diodes, powering the output and in turn charging the relative bank capacitances.

The main difference between the two types just proposed lies in the voltage stress to which the various components are subjected: at the same output voltage, the last proposed solution makes it possible to reduce by half the voltage

stress imposed on the various power components such as diodes and capacitors, thanks to the use of two separate output half-banks, one positive and one negative. This certainly implies the possibility of working with higher output voltages than other types, thus optimizing the power-volume ratio[1] of the same converter.

It is interesting to note that the latter type represents a three-level converter, unlike the former which has only two levels: this means that the voltage potential "Va", visible in the figure 4.2 (b), can take on *ideally* three different voltage values (V_{dc} $[V]$, 0 $[V]$, $-V_{dc}$ $[V]$) in order to control the inductor current. Clearly, unlike other types of two-level converters, this feature gives the latter a greater ability to shape the input current waveform[2]; at this point it is easy to understand how the three-phase version of the Vienna Rectifier works.

Taking Figure 4.2 (b) as a reference, two additional input voltage phases can be added: two boost converters are added for each phase, which operate in the same way for each voltage line, loading the two capacitances already present at the output.

We can ultimately consider the three-phase Vienna rectifier shown in Figure 4.1 as the fusion of six boost converters, two for each phase, which load the same output capacitances in groups of three: this makes it possible to reduce the current demand by each individual phase, due to the fact that the active power called up by the load will be shared and generated by the three input current phases.

Furthermore, to work with a three-phase rectifier brings with it an essential advantage, along with those already mentioned, over the simple single-phase configuration. Referring again to the figure 4.1, it is clear that there is no need for any connection between node M (machine center) and node N (network center): this allows, in fact, to function as a three-phase rectifier *without neutral*. In fact, observing the single-phase configuration of Vienna Rectifier, it is clear that during the inductor loading phase the current must pass through the switch and then close on the same voltage generator: the two ground references present in Figure 4.2 (b) can in fact be replaced by a single connection.

[1] Low powers imply the use of smaller components, allowing for more compact boards.

[2] This reasoning cannot be applied to the model in the figure 4.2 (a) because the input voltage is rectified, reducing its swing by half and therefore simplifying the control of the inductor current.

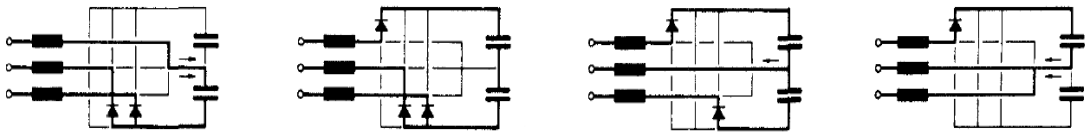


Figure 4.3: Paths followed by currents during different moments of operation.

This is not the case in the three-phase configuration in which, if the system is properly functioning and the line voltages represent a balanced tern, it can be assumed that the tern of current that must circulate through each phase is also balanced. We can then assume that instant by instant the following equation is valid, which links the three currents circulating in the three input inductors:

$$i_a(t) + i_b(t) + i_c(t) = 0\ [A] \tag{4.1}$$

Therefore, being purely differential currents, which do not present any common component between them, they automatically make the previous equation valid also in the center of the machine, without having to impose the Kirchhoff equation on the currents at that point: this clearly imposes an average voltage equal to 0 $[V]$ in the center of the machine, obviously already present at the center of the network tern; a hypothetical neutral cable connected between these two points would, in fact, be useless. We must also not forget that any balanced three-phase network possesses, instant by instant, two voltage lines with positive instantaneous value and one with negative value (or vice versa): the case in which all three voltage lines have the same sign can never occur.
The Vienna Rectifier, having to operate as a three-phase PFC, ensures the fact that all three currents have the sign of the relative line voltage: this ensures that, instant by instant, the charging current of a certain coil becomes the discharging current of the remaining two coils, or vice versa, keeping the previous equation valid and allowing the current to flow from one phase to the other. The image shown in Figure 4.3 makes this fact easier to understand, showing the path followed by the currents in the circuit during different operating states of the system.
It is interesting to observe this type of operation in a little more detail, showing the direction assumed by the currents in the various cases of system control. To do this it is convenient to divide the network period into six different regions, according to the polarity assumed by the three supply voltages: each region is

characterised by a specific direction of circulation to be followed by the various currents, clearly concordant with their corresponding line voltages. After having defined the direction of flow of the currents within a certain sector, we only need to observe the state of the various switches to understand the physical path that the currents will actually take.

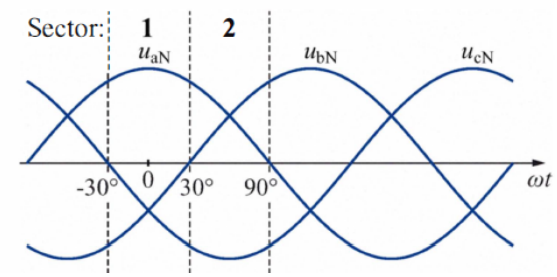


Figure 4.4: Partition of the network period into six sectors of 60° each.

Let's start by taking Figure 4.4 as a reference, which shows the subdivision into sectors carried out over a network period, expressed in degrees rather than seconds. We then build a table in which to report the physical path followed by the currents, depending on the logic state present on the various switches, focusing on the first sector; in the same way it will be possible to obtain the corresponding characteristics of each section.

SW_a	SW_b	SW_c	state L_1	state L_2	state L_3	i_M $[A]$
0	0	0	D	D	D	0
0	0	1	D	D	C	$-i_c$
0	1	0	D	C	D	$-i_b$
0	1	1	D	C	C	$i_c + i_b = -i_a$
1	0	0	C	D	D	i_a
1	0	1	C	D	C	$i_a + i_c = -i_b$
1	1	0	C	C	D	$i_a + i_b = -i_c$
1	1	1	C	C	C	$i_a + i_b + i_c = 0$

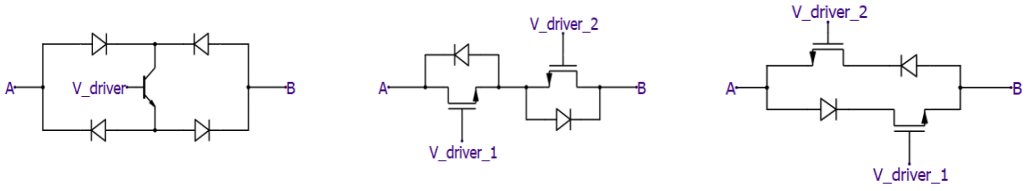
Table 4.1: Summary table of the direction assumed by the various currents in the first operating sector, as a function of the logical states of the switches.

Using the conventions shown in Fig. 4.1 it can be observed that the following statement is valid in the first sector: $V_a > 0,\ V_b < 0,\ V_c < 0$ so the assumed direction of the currents will be the same, setting $i_a \geqslant 0,\ i_b \leqslant 0,\ i_c \leqslant 0$.
By then indicating with '1' the logical "on" state and with '0' the "off" state of each switch, further indicating with C the fact that a certain current is flowing

through the corresponding switch by charging the corresponding inductor (C = Charge), and at the same time using D to represent the fact that a certain current is flowing through the diodes by implementing the discharge process of the corresponding inductor (D = Discharge), we can represent the value assumed by the current i_M within the table 4.1. Clearly, observing the latter it can be verified that the condition $i_a(t) + i_b(t) + i_c(t) = 0\ [A]$ remains valid in any case.

Bidirectional switch

It is interesting to observe in greater detail how the bidirectional switches presented previously are implemented. In principle, a bidirectional switch can be implemented through the use of multiple unidirectional switches such as BJT, MOSFET or IGBT, combined for example with some diodes, which can be internal or external to the same components. Some examples are shown in Figure 4.5: figure (b) shows, for example, a configuration that can be achieved by exploiting the antiparallel diodes present internally in the power MOSFETs, without having to connect them externally; on the contrary, using IGBTs instead of MOSFETs, it becomes necessary to use external diodes (c).



(a) (b) (c)

Figure 4.5: Examples of bidirectional switches. Single undirectional switch inserted in a diode bridge (a); opposite series of two bidirectional current devices (b); antiparallel connection of two bidirectional devices (c).

Independently of the choices made by the factory, we choose to use the configuration shown in Figure 4.5 (b) within the simulation that will be carried out during the development of the project. The image shows the possibility of using two different control signals for the two switches, although nothing prevents the use of the same signal for both; in fact, since the direction of the currents is already defined by the relative input voltage, there is no substantial difference between operating the two switches simultaneously or not, at least as regards

the general functioning of the system.
Some difference can be seen, however, when dealing with the subject of switching losses and the safety of the system itself: operating the two switches at the same time increases losses, as the parasitic capacitances present in the gates of the various switches used are unnecessarily charged and discharged, and also generates a potential drop on the diode as the latter conducts, which is certainly greater than if the MOSFET itself were used. Clearly, this type of control increases the general safety of the system since, in the event of errors on the part of the system, both switches can be instantly turned off by acting on the same signal, thus preventing any current flowing through them.
Another possibility, opposite to the previous one, suggests instead modulating only the state of the switch that regulates the operation of the system; the second switch can instead be kept always on as its contribution is null for control purposes. This helps reduce losses, because the voltage drop will be much smaller than it would be if the diode were used in antiparallel, avoiding as just mentioned the switching losses.
This solution involves less safety for the system itself: in the event in which the input voltage undergoes an unforeseen change of sign, for example as a result of a dangerous transient or notching, we could find ourselves momentarily operating in the wrong quadrant of the system's V-I characteristic, thus momentarily generating uncontrolled and dangerous currents.
The safest and at the same time less efficient alternative is, instead, to control only one of the two one-way switches, leaving the second one switched off at all times.

Faced with this trade-off we choose an intermediate solution: during the simulation, a single signal will be used to control both switches.

Necessary hardware modifications: the three input capacitances

The configuration shown in the Figure 4.1, although representing the classical configuration of the Vienna Rectifier, requires some modification in order to allow the achievement of the set objectives. In fact, in order to realise an overmodulation control, it is necessary to have an extra current harmonic circulating with a frequency three times higher than the mains frequency; the latter will be able to model the voltage present on the machine centre point (M), in order to extend the control capability of the entire structure for higher mains values,

compared to the case in which no overmodulation is applied. Since it is a boost rectifier, there is no possibility of maintaining control in the event that, even for an instant, one of the three voltage input phases should assume a higher value than that held by a single half-bank[3].
Clearly, the triple-frequency harmonic component that is to be injected into the system needs a special mesh in which it can circulate: as it is not part of any three-phase tern, it cannot exploit any relation similar to the equation 4.1 to circulate.
It is then convenient to split the overmodulation harmonic component into three common components, making them flow through the relative input coils and then summing up in the machine centre node, allowing the path to be reclosed by inserting three impedances, as equal to each other as possible, in order to maintain the symmetry of the circuit. We have thus realised three new meshes in which any homopolar component, generated by the circuit itself, may flow, including the third current harmonic.

Therefore we modify the figure 4.1 by adding three input capacitors which will be connected between the network and the coils as just mentioned, finally connecting them to the machine centre node. These capacitors will have a dual purpose:

- **Permit overmodulation control**; the newly added capacitances allow the third-harmonic current homopolar components to circulate in the network, taking advantage of the voltage drop they generate on the input capacitors, in order to permit overmodulation control;

- **Filtering high frequency ripple**; using a PWM control will certainly generate some high frequency component which can be split into a common ripple component and differential: the former will circulate on the capacitors because it is homopolar, while the latter will do so as long as the capacitors have a much lower impedance than the one introduced by the power line[4]. The capacitors will then act as a high-frequency filter, allowing as little high-frequency disturbances as possible to be injected into the network, assuming the respective capacitance values are carefully chosen.

[3] Any boost configuration can work if and only if $V_{in} \leqslant V_{out}$, regardless of whether it is used within a three-phase, single-phase or DC voltage system.

[4] Redrawing the power line using Thévenin's theorem and considering the three capacitors as short-circuited this statement becomes obvious, being at high frequencies, exploiting the voltage divider rule.

Overmodulation operation will be discussed in more detail in the following section; for now we can however assume that, in the case of control by injection of a third harmonic current, the equation 4.1 must be modified as shown below, according to what has been said:

$$i_a(t) + i_b(t) + i_c(t) = i_{3\text{rd harm}}(t)\ [A] \tag{4.2}$$

Necessary hardware modifications: the banks regulator

In order to achieve correct operation of the Vienna Rectifier it is not only necessary to ensure that the output voltage is as required and that the inductor currents flow as intended, but it is also necessary to ensure that the voltages present at the two output capacitances are the same. This fact is in effect not ensured during the classical operation of the Vienna Rectifier, since the voltage control usually implemented only handles the output voltage of the entire stage of value $V_{out} = V_{dc} - (-V_{dc}) = 2 \cdot V_{dc}\ [V]$.
Since there is in fact no control over the individual voltages of the half-banks, but only over the total output voltage, there is a risk that one of the two capacitances may be loaded more than the other, altering the potential at the machine centre and affecting the efficiency of the modulation technique implemented. This issue would, however, affect other factors including the possible increase in switching losses by the control switches, as the voltage at their terminals would be modified, or by increasing the voltage stress to which the most charged capacitor would be subjected, which could even explode if the voltage at its terminals were to exceed the limit allowed by its dielectric rigidity.
An easily implementable hardware solution can be seen in Figure 4.6 which shows, among other things, the overall circuit diagram that will be used for this project[5]. The proposed solution is based on the use of a bidirectional buck-boost converter, which utilises the individual voltages present on the output half-benches as the voltage values on which to operate. By controlling this type of converter, in such a way as to balance the amount of charge present on both capacitors, it is possible to shift this charge from one capacitor to the other, in

[5]Once again the presence of diodes placed in antiparallel to the various unidirectional switches, present in the figure, is highlighted; these diodes are clearly not necessary if MOSFETs, which have internal diodes placed in antiparallel, are used, becoming instead necessary when exploiting, for example, IGBTs.

case of imbalance, thus keeping the voltage present on each output half-bench constantly balanced, even when operating with unbalanced loads.

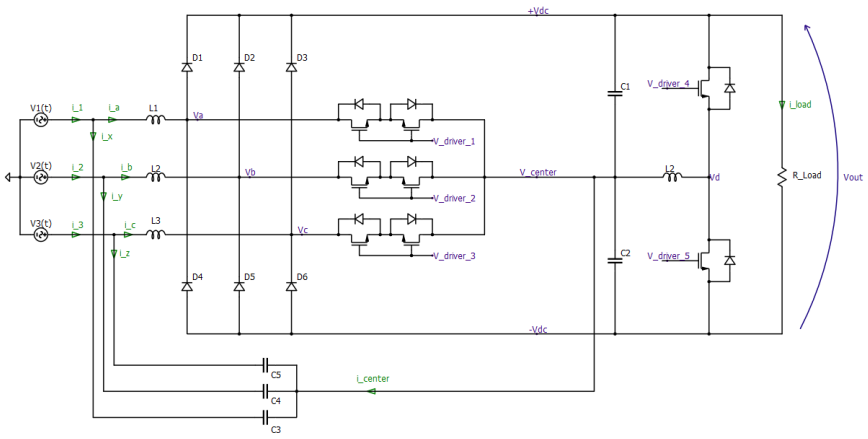


Figure 4.6: Ideal final circuit configuration of the Vienna Rectifier, necessary for the development of the project.

Clearly, the negative half-bank is loaded by the positive half-bank using the switch driven by the signal "$V_{\text{driver }4}$" and the diode placed between V_{dc} and $-V_{dc}$. The positive half-bank can instead be charged via the negative half-bank, using the unidirectional switch and the diode opposite to those just mentioned. There can be several different control techniques that can be implemented for this type of converter, both open and closed loop, which will be mentioned in the chapter specifically dedicated to machine control.
Although this type of solution has been chosen to be implemented, this does not imply that there are no others. In fact, the introduction of this hardware configuration is not mandatory, since the problem of voltage unbalances on the half-banks can be handled by acting directly on the inductor currents.
By acting on the current control, we could temporarily unbalance the inductor current absorption, further charging the output capacitor which is less charged than the other, thus avoiding the need to insert an additional controller. Clearly, each solution brings with it its own strengths and weaknesses, which is why it was chosen to continue as previously reported.

The proposed circuit solution is therefore the definitive one; now, adding the major non-idealities that can affect the real circuit, such as line impedances or parasitic impedances, we can obtain the model to be used within the simulation. Figure 4.7 shows the circuit diagram that will be used to carry out the project

simulations; MOSFETs and their respective diodes can, in this case, be replaced by bidirectional switches with the addition of corresponding non-idealities. On the right-hand side of the same picture there are also programmable generators acting on bidirectional switches: the latter can be used to simulate load changes by short-circuiting or connecting additional resistors, placed either in series or parallel to the one already present.

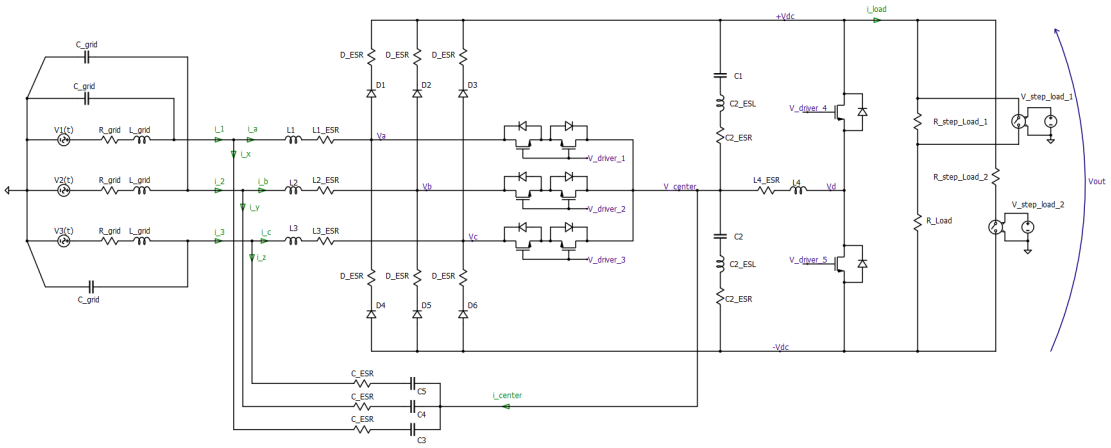


Figure 4.7: Circuital model of the Vienna Rectifier that can be implemented on the simulator, including the major non-idealities present in the real circuit.

4.2 Analytical Approach to Circuit Design

Having defined the final circuit diagram, it is now convenient to analyse in more detail the entire electrical operation of the system, in order to be able to define the correct values to be assigned to the various components in view of the design constraints, to estimate the value of the electrical quantities, assumed during operation, and to predict the performance of the system itself. In the following paragraphs the steady state operation of the overall system will be analysed, followed by the analysis of the average models which will allow us to derive the different transfer functions necessary to analyse the stability of the system.

4.2.1 Steady state operation

We can start by trying to estimate the input current that should be circulated in the three phases during steady state operation, having a certain well-defined load to supply; as usual, we should initially refer to the single-phase model shown in the figure 4.8.
The picture just reported, in addition to showing the classic model of the single-phase Vienna Rectifier, gives us the opportunity to observe how the components contained within the shear surface S can be considered, at least in a first approximation, non-dissipative: it can therefore be easily concluded that the active power P_{out} recalled by the load is practically approximable to the active power P_{in} delivered by the input generator. We are then justified to write:

$$P_{in} \simeq P_{out} \quad \Longrightarrow \quad V_{in_{RMS}} \cdot I_{in_{RMS}} \simeq \frac{V_{out}^2}{R_{load}} \; [W]$$

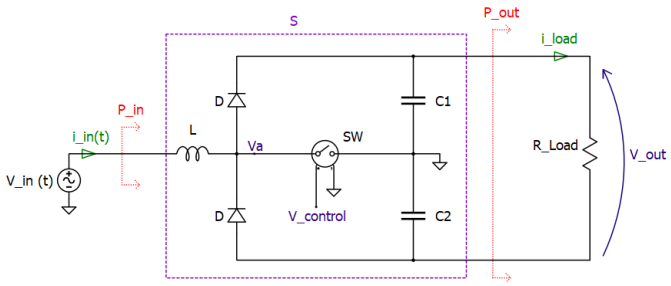


Figure 4.8: Single-phase model of the Vienna Rectifier.

Clearly, the concept does not change in the three-phase context: observing the circuit in the figure 4.6 it is clear that the only dissipative element present is once again the load resistance, which can only be powered through the contribution of the inductor currents. The only difference compared to the previous case is that the input power is delivered identically by the three current phases, rather than by a single one. We can then write, using the same references used in the previous case for each single current:

$$3{\cdot}P_{in} \simeq P_{out} \quad \Longrightarrow \quad 3{\cdot}V_{in_{RMS}}{\cdot}I_{in_{RMS}} \simeq \frac{V_{out}^2}{R_{load}} \quad \Longrightarrow \quad I_{in_{RMS}} \simeq \frac{V_{out}^2}{3 \cdot R_{load} \cdot V_{in_{RMS}}}\ [A]$$

The previous equation can be rewritten as a function of the peak values in the case of a perfectly sinusoidal input voltage[6]:

$$I_{in_{peak}} \simeq \frac{2}{3} \cdot \frac{V_{out}^2}{R_{load} \cdot V_{in_{peak}}}\ [A] \tag{4.3}$$

where clearly $I_{1_{peak}} = I_{2_{peak}} = I_{3_{peak}} = I_{in_{peak}}$; as already repeated more than once, the phase possessed by each input current will be the same as its phase voltage.

Under the same assumptions it is also possible to calculate the current circulating through the three input capacitors. Using the references present in fig. 4.6 and defining $v_{center}(t) \equiv v_c(t)$ for brevity we can write, using the user convention for each passive component:

$$v_{C3}(t){+}v_{C4}(t){+}v_{C5}(t) = \big[V_1(t){-}v_c(t)\big]{+}\big[V_2(t){-}v_c(t)\big]{+}\big[V_3(t){-}v_c(t)\big] = -3{\cdot}v_c(t)\ [V]$$

under the hypothesis $C3 = C4 = C5 = C$ we can than write:

$$i_x(t) + i_y(t) + i_z(t) = C \cdot \left[\frac{d}{dt}v_{C3}(t) + \frac{d}{dt}v_{C4}(t) + \frac{d}{dt}v_{C5}(t)\right]\ [A]$$

by now exploiting the linearity of the derivative operator, in conjunction with the equation derived earlier, we obtain:

$$i_x(t) + i_y(t) + i_z(t) = -3 \cdot C \cdot \frac{d}{dt}v_{center}(t)\ [A] \tag{4.4}$$

[6]For any sinusoidal waveform is clearly valid $V_{RMS} = \frac{V_{peak}}{\sqrt{2}}$

This last relationship turns out to be of fundamental importance, allowing us to make two important considerations:

1. The relationship shows how the machine centre voltage, in the absence of homopolar components, flowing through the input capacitances such as the third current harmonic, must necessarily assume a constant value;
2. The relationship makes it possible to calculate the amplitude that the third current harmonic will have to assume, depending on the type of overmodulation we want to obtain.

The first consideration comes from the fact that

$$i_x(t) + i_y(t) + i_z(t) = -i_{center}(t) = 0\ [A]$$

by construction; the centre current can in fact be expressed as the sum of the three inductor currents, which is equal to $0\ [A]$ instant by instant as seen previously. This implies, therefore:

$$i_{center}(t) = 3 \cdot C \cdot \frac{d}{dt} v_{center}(t) = 0\ [A] \quad \Longrightarrow \quad v_{center}(t) = \text{const.}\ [V] \tag{4.5}$$

The second consideration comes from the fact that, in the case in which overmodulation control is present, the relationship ideally holds:

$$i_{center}(t) = i_{3\text{rd harm}}(t) = 3 \cdot C \cdot \frac{d}{dt} v_{center}(t)\ [A] \tag{4.6}$$

validated by the equation 4.2 presented previously. The equation 4.6 just calculated will be useful later, since, knowing the shape that the machine centre voltage must take in order to overmodulate, we will also be able to predict the shape that the third harmonic current must assume.
As a result of these observations it is in any way possible to calculate the currents flowing into the input capacitors, as mentioned above. Assuming we have no overmodulation we can try to calculate the current $i_x(t)$, knowing that $v_1(t) = V_{1peak} \cdot \sin(\omega t + \phi_1)\ [V]$:

$$i_x(t) = C \cdot \frac{d}{dt}\big(v_1(t) - v_{center}(t)\big) = C \cdot \frac{d}{dt} v_1(t) = \big(\omega \cdot C \cdot V_{1peak}\big) \cos(\omega t + \phi_1)\ [A]$$

Clearly the further two currents i_y and i_z will only differ from the latter in terms of phase shifting, being also part of a three-phase triplet.

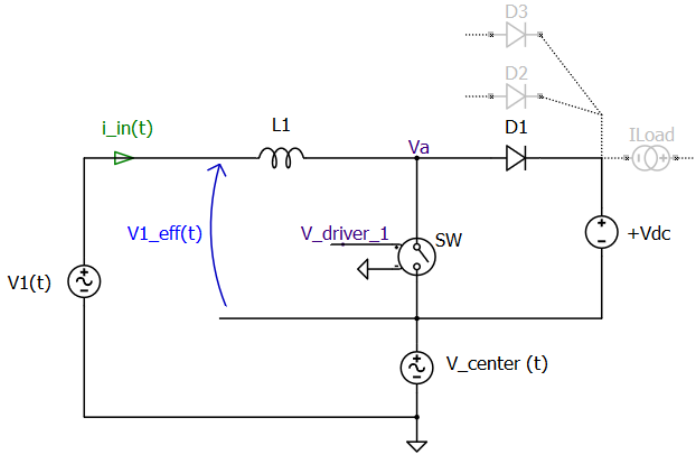


Figure 4.9: Ideal circuit for studying one of the six individual boost converters belonging to the three-phase Vienna rectifier configuration.

Conversion index

Certain figures of merit characteristic of static operation can be calculated independently of the fact that the system on which one is operating is single-phase or three-phase; one of these is the *conversion index*, that links the output voltage with the input voltage.
Knowing that the overall system comprises 6 boost configurations, it is interesting to demonstrate what has been said by calculating which should be the conversion index affecting each phase. We can start by making a few assumptions:

1. The system is ideal;
2. The output voltage ripple is absent[7].

We can focus, for the moment, only on the boost configuration dedicated to working with the positive half-wave of the first input phase: we can then model the system as shown in Figure 4.9, in which the capacitor belonging to the positive half-bank has been replaced by a constant voltage generator[8]. Diodes belonging to the remaining two input branches are also shown, as well as an output current generator that simulates the presence of a load to be supplied. If one looks closely at the figure it is possible to clearly recognise the classic

[7]This last assumption is correct and will be demonstrated later.
[8]approximation valid under the hypothesis $C_1 \rightarrow \infty$ $[F]$.

boost configuration and the role played by overmodulation. It is clear, in fact, that the circuit represented can be studied as a boost converter with an input voltage equal to $v_{1\text{eff}}(t) = v_1(t) - v_{center}(t)$ $[V]$, and output voltage equal to V_{dc}; the presence of the other phases merely reduces the current recalled by the load on each phase by a factor 3. We are therefore allowed to study the single stage in an isolated way as if the actually connected output load were 3 times larger. The desired relationship can easily be obtained by considering the Volt Second Balance relation, valid under the hypothesis of using a switching frequency f_s $[Hz]$ much higher than the mains frequency f_o $[Hz]$.
We can then write:

$$\begin{cases} V_{L1}^{on} \simeq v_{1\text{eff}}(t) & \text{if } t \in t_{on} \\ V_{L1}^{off} \simeq v_{1\text{eff}}(t) - v_{center}(t) & \text{if } t \in t_{off} \\ V_{L1}^{on} \cdot T_{on} = |V_{L1}^{off}| \cdot T_{off} & \text{(from the VSB law)} \end{cases}$$

from which we easily derive the following relationship, valid in CCM $\forall t \mid v_{1\text{eff}}(t) > 0$ $[V]$, which represents the conversion index desired:

$$M_+(t) = \frac{V_{dc}}{v_{1\text{eff}}(t)} = \frac{1}{1 - d_1(t)}$$

where clearly $d_1(t) = \frac{t_{on}}{T_{sw}}$ represents the duty cicle.
It is clear that the relationship just derived is the same for any boost converter working in CCM; we can also extend the relationship just derived to the relative boost converter operating with negative voltages, obtaining the following equation:

$$M(t) = \frac{V_{dc}}{|v_{1\text{eff}}(t)|} = \frac{1}{1 - d_1(t)} \tag{4.7}$$

The latter relationship is valid assuming the use of a single bidirectional switch for each control branch so as to impose a single modulating signal, as mentioned above. Although the input voltage changes sign, the three-phase structure allows automatic circulation of currents in such a way that positive half-wave operation does not have to be distinguished from negative half-wave operation; clearly, the previous relationship can be extended to each phase.

One could therefore theoretically control the entire three-phase structure by

means of an open loop control, imposing a duty cycle of the type:

$$\delta_i(t) = 1 - \frac{|v_{i\text{eff}}(t)|}{v_{dc}}$$

if the load would allow exclusively CCM operation for all three phases. In the absence of overmodulation there would be $v_{i\text{eff}}(t) = v_i(t)$, which would lead to writing, in the case of an undistorted line:

$$d_i(t) = 1 - \frac{V_{i\text{peak}}}{V_{dc}} \cdot |\sin(\omega t + \phi_i)| = 1 - k \cdot |\sin(\omega t + \phi_i)|$$

con $k \leq 1$.
The same type of procedure can be followed to calculate the $d_i(t)$ generated in DCM, which is identical to that of any single-phase boost converter.

Modulation index

Before continuing it is also necessary to deal with the operating case in which overmodulation is applied, as in the case of our interest. We can then refer to figure 4.10, which clearly shows the benefits introduced by the overmodulation technique that we want to exploit. Using a normalised scale the image shows one of the three line voltages (in red), the machine centre voltage generated by the flow of the third harmonic of current through the capacitors introduced earlier (in green) and the respective voltage difference present between the two (in blue), which represents the voltage $v_{i\text{eff}}(t)$ present at the input of each boost stage, excluding the relative phase shifts.

It can be mathematically demonstrated that the effect of overmodulation becomes optimal when the machine centre voltage results to be a sine wave with an amplitude equal to 15.5% of the peak voltage of the three lines (assumed balanced), shows a frequency equal to three times that of the grid, and is in phase with the three voltage lines.
We can then define, assuming we exploit the optimal overmodulation case:

$$v_{i\text{eff}}(t) = V_{i\text{peak}} \cdot \sin(\omega_o t + \phi_i) - 0.155 \cdot V_{i\text{peak}} \cdot \sin(3\omega_o t + \phi_i)\ [V]$$

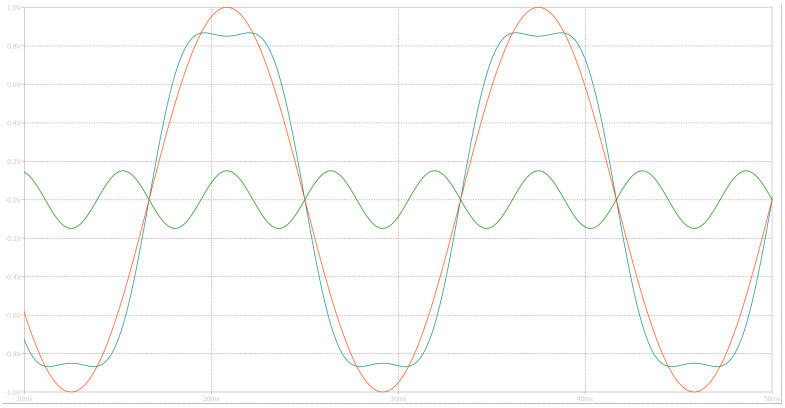


Figure 4.10: Example of overmodulation desired to be implemented: it is shown, for simplicity, its application only on the first voltage phase.

from which we obtain the generalisation of the previously sought relationship, valid in the case where overmodulation is applied:

$$d_i(t) = 1 - \frac{V_{i\text{peak}}}{v_{dc}} \cdot |\sin(\omega t + \phi_i) - 0.155 \cdot \sin(3\omega t + \phi_i)|$$

In order to mathematically quantify the benefit obtained from the introduction of the third current harmonic, it is convenient to introduce an additional parameter, called *modulation index*, which can be defined appropriately for each power converter:

$$m_a = \frac{V_{i\text{peak}}}{V_{out}/2} \tag{4.8}$$

The parameter just introduced, valid for each boost configuration belonging to the overall network, represents by means of a numerical value the operating state of the boosts through the ratio performed between the peak value that the line voltage can reach, which represents the input voltage of the boost converter in the case of absence of overmodulation, and the DC voltage present on each half-bank, which represents the output voltage of each boost stage as represented in the figure 4.9.
Obviously, in the case where there is no overmodulation, the maximum modulation index is reached when $V_{i\text{peak}} = V_{out}/2 = V_{dc}$ $[V]$ as a generic boost stage is not able to generate output voltages that are lower than the input voltages, as previously pointed out.
With the introduction of overmodulation, instead, it becomes possible to maintain control of the various boost converters as long as the relationship $V_{i\text{eff}} \leq$

V_{dc} $[V]$ remains valid, from which we can derive the limiting case in the form $V_{i\text{eff max}} = V_{i\text{peak}} + 0.155 \cdot V_{i\text{peak}} = V_{dc}$ $[V]$, thus allowing the input line voltage to reach peaks equal to $V_{i\text{peak max}} = 1.155 \cdot V_{dc}$ $[V]$ before losing control of the system. We can then, in case in which overmodulation is applied, reach[9] the case where $m_{\text{a max}} = 1.155 > 1$.

Current ripple and input inductors

Continuing with the theoretical study of the operation of the system at steady state it is possible to affirm that, as in the previous case, the current ripple equation is also independent of the number of phases used. As already pointed out, it is in fact the average inductor current to be influenced by the number of phases used, unlike the current ripple, which is a simple oscillation superimposed on the latter. We can then expect to obtain the same classical current ripple equation, valid for any single-phase boost, regardless of the number of phases used. Let us then assume:

$$\Delta i_{L_{pp}} = \frac{1}{L} \cdot \int_{t_o}^{t_o+T_{on}} |v_{i\text{eff}}(t)| dt \simeq \frac{|v_i(t) - v_{center}(t)| \cdot d_i(t) \cdot T_s}{L} \; [A]$$

from which:

$$\Delta i_{L_{pp}} \simeq \frac{V_{dc} \cdot \big(1 - d_i(t)\big) \cdot d_i(t) \cdot T_s}{L} \; [A] \tag{4.9}$$

It is possible to exploit this last relationship to choose an appropriate value to assign to the various inductances, considering the worst-case scenario, setting the maximum acceptable amplitude for the current ripple according to our design specifications. By then assuming $\delta_{i\text{worst case}} = \frac{1}{2}$ we obtain:

$$L_{min} = \frac{V_{dc}}{4 \cdot f_s \cdot \Delta i_{L_{pp}}} = \frac{V_{out}}{8 \cdot f_s \cdot \Delta i_{L_{pp}}} \; [H] \tag{4.10}$$

demonstrating that the equation obtained reflects the same as for any boost stage. Clearly, by L_{min} we mean the minimum inductance value that the coil can reach during its operation within the circuit, since the latter cannot be considered constant. Each inductor, in fact, depending on the intensity of the current flowing through, it presents a certain value of inductance depending on

[9] This last observation is valid in the ideal case; in reality, due to voltage drops and losses, a slightly higher maximum modulation index can be achieved.

the type of air gap present within it, generating saturation phenomena and thus modifying the value of its inductance instant by instant.

Voltage ripple and output capacitors

Having obtained an equation which can be used to estimate the inductors, we must now concentrate on estimating the value to be associated with the two large output capacitances. Unlike single-phase systems, however, the value of these capacitances is not to be sought as a function of a certain voltage ripple that may be presented superimposed on the voltage V_{out}. In the latter, in fact, the capacitors play the role of energy storers, charging and discharging themselves continuously as a function of the fluctuating power component coming from the input network. In fact, the instantaneous power called up by a single-phase converter can be mathematically considered as the superposition of a constant component, defined by the active power delivered, and a periodic component, formed by the fluctuating power, where the contribution of the latter becomes zero every T_o $[s]$.
Three-phase systems, regardless of whether they have a neutral connection or not, are characterised by a fundamental property in contrast to single-phase systems: they carry instantaneous power having a constant value.
More precisely, although each phase carries both active and fluctuating power,the contribution from the latter elides with the one from the other phases:

$$p_i(t) = \big(P_{A_1} + p_{f_1}(t)\big) + \big(P_{A_2} + p_{f_2}(t)\big) + \big(P_{A_3} + p_{f_3}(t)\big) = 3 \cdot P_A + \sum_{n=1}^{3} p_{f_n}(t) = 3 \cdot P_A \ [W]$$

It then results that, theoretically, capacitors play no role in stabilizing the output voltage, as they do not act as energy storages. We can therefore expect to find a output voltage with *no ripple component*.
The reality of the facts is actually more complicated than what explained, since our assumptions are based on the fact that a resistive load of constant value is linked at the output. In reality, we will find a three-phase inverter which can work asynchronously with the input rectifier stage, or in an unbalanced way, thus absorbing energy from the capacitors and generating superimposed ripple to the output voltage.
Considering negligible the contribution generated by the latter, it is possible to size the output capacitance according to how slowly you want the output bank to

discharge, in the event that the system should instantly find itself without mains power. If a UPS is to be realized, in the event of a hypothetical blackout the bank will start to discharge slowly, providing the necessary time for the battery to connect. We can then determine a time constant associated with the discharge time of the capacitors: knowing that the latter will be totally discharged in a given time interval $\overline{T}$ we can define the latter as:

$$\overline{T} \simeq 5 \cdot \tau \simeq 5 \cdot (C_1 // C_2) \cdot R_{Load_{min}} \; [s]$$

Using then the usual discharge equation for a capacitor we can determine the minimum discharge time t_{min} required by the specifications, thus ensuring a hold-up time necessary for the machine to function properly:

$$V(t_{min}) \simeq V_{out} \cdot e^{-\frac{t_{min}}{\tau}} \; [V] \quad \Longrightarrow \quad t_{min} \simeq \tau \cdot \ln\left[\frac{V_{out}}{V(t_{min})}\right] [s]$$

Choice of diodes and switches: stress and conduction losses

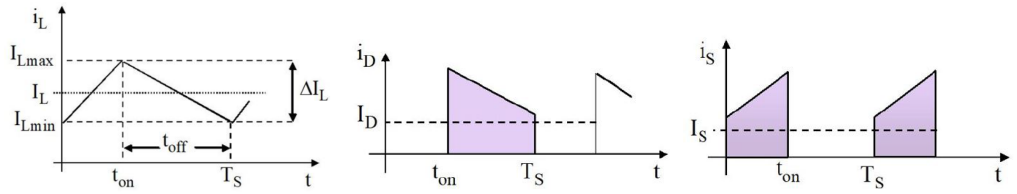
The sizing of the components must certainly also be carried out as a function of the conduction losses and the voltage and current stress to which they will be subjected during normal system operation. In this regard, the estimation of conduction losses can easily be carried out as a function of the entity of the average and RMS currents flowing through the various components, where the latter are slightly more complex to obtain. The estimation of losses can then be applied in order to design the most appropriate heat sink to be used.
In this regard, it is interesting to quantify the entity of currents that may flow through the diodes and MOSFET (or whatever type of electrical switch one wishes to use) in the circuit during usual operation; one may therefore proceed as illustrated below.
By observing the figure 4.9 it becomes immediate to derive the usual ideal current waveforms characteristic of each boost stage, shown in Figure 4.11. These represent the trend of the currents flowing through the inductor, diode and switch of each boost converter referring to a generic instant of operation.
In fact, although the actual waveforms have an average sinusoidal pattern, when considered within a single switching period they can be regarded as having a constant average value. The quantities shown in the figures are then to be considered as average current values calculated over a single switching period,

and not over an entire network period.
It is then convenient to proceed by calculating the current values, averaged over a switching period, which flows through the diode and the switch; it is easy to demonstrate that:

$$\overline{i_s}(t) = \frac{1}{T_s}\int_0^{T_s} i_s(t)\,dt = \overline{i_L}(t)\cdot d_i(t)\;[A]$$

$$\overline{i_D}(t) = \frac{1}{T_s}\int_0^{T_s} i_D(t)\,dt = \overline{i_L}(t)\cdot (1-d_i(t))\;[A]$$

where the quantities $\overline{i_s}(t)$, $\overline{i_D}(t)$ and $\overline{i_L}(t)$ represent the average quantities calculated over a switching period, which are however not constant in value when considered over an entire network period.
We now proceed by averaging these currents over an entire network period, this time referring to the complete circuit shown in Figure 4.6. Assuming that we are working in CCM operation, for the moment without any overmodulation, we calculate the average current flowing on diode $D1$ and through the respective MOSFET during the positive half-wave current coming from inductor $L1$ as follows.



(a) (b) (c)

Figure 4.11: Trend of the current flowing through the inductor (a), diode (b) and switch (c) on a generic boost stage, relative to a single switching period.

We can first rewrite the equation 4.7 as shown:

$$1-d_1(t) = \frac{V_1(t)}{V_{dc}} = \left(\frac{\hat{V}_1}{V_{dc}}\right)\sin(\omega_o t) = m_a\cdot\sin(\omega_o t) \implies d_1(t) = 1-m_a\cdot\sin(\omega_o t)$$

where clearly the use of modules has been avoided, since we are only interested

in considering the time interval $[0,\ T_o/2]$. We now pose:

$$\overline{i_D} = \frac{1}{T_o}\int_0^{T_o} \overline{i_D}(t)\ dt = \frac{1}{T_o}\int_0^{\frac{T_o}{2}} \overline{i_L}(t)\cdot(1-d_1(t))\ dt\ [A]$$

Rewriting now $\overline{i_L}(t) = \hat{i_L}\sin(\omega_o t)$, where $\hat{i_L}$ has been calculated by means of the equation 4.3, we finally obtain:

$$\overline{i_D} = \frac{1}{T_o}\int_0^{\frac{T_o}{2}} \hat{i_L}\cdot\sin(\omega_o t)\cdot m_a\cdot\sin(\omega_o t)\ dt = \frac{\hat{i_L}\cdot m_a}{T_o}\int_0^{\frac{T_o}{2}} \sin^2(\omega_o t)\ dt = \frac{\hat{i_L}\cdot m_a}{4}\ [A]$$

The same can be done for the MOSFET used for positive current conduction:

$$\overline{i_s} = \frac{1}{T_o}\int_0^{T_o} \overline{i_s}(t)\ dt = \frac{1}{T_o}\int_0^{\frac{T_o}{2}} \overline{i_L}(t)\cdot d_1(t)\ dt = \hat{i_L}\cdot\left(\frac{1}{\pi}+\frac{m_a}{4}\right)[A]$$

The same RMS values can be easily calculated using the same procedure just shown:

$$i_{s_{RMS}} = \sqrt{\frac{1}{T_o}\int_0^{T_o} \overline{i_s}(t)^2\ dt} = \hat{i_L}\sqrt{\left(\frac{1}{4}-\frac{2m_a}{3\pi}\right)}\ [A]$$

$$i_{D_{RMS}} = \sqrt{\frac{1}{T_o}\int_0^{T_o} \overline{i_D}(t)^2\ dt} = \hat{i_L}\sqrt{\left(\frac{2m_a}{3\pi}\right)}\ [A]$$

The values just calculated were derived under the assumption of the absence of overmodulation. In the case in which it is present, it suffices to slightly modify the previous equations; we then proceed by defining:

$$d_1(t) = 1 - \frac{\hat{V_1}\cdot\sin(\omega_o t) - 0.155\cdot\hat{V_1}\cdot\sin(3\omega_o t)}{V_{dc}} \qquad \forall t\in[0,T_o/2]$$

from which:

$$d_1(t) = 1 - m_a\cdot\frac{\sin(\omega_o t) - 0.155\cdot\sin(3\omega_o t)}{V_{dc}} \qquad \forall t\in[0,T_o/2]$$

At this point, the expression of the average current must also be modified, as there will be a third harmonic superimposed on the main one. Using then the

equations 4.2 , 4.3 and 4.4, by assuming CCM behavior we can write:

$$\overline{i_L}(t) = \hat{i_L} \sin(\omega_o t) + \frac{i_{3\,\text{arm}}(t)}{3} = \hat{i_L} \sin(\omega_o t) + \frac{3 \cdot C_{in} \cdot \frac{d}{dt}\left[0.155 \cdot \hat{V_1} \sin(3\omega_o t)\right]}{3}\ [A]$$

from which:

$$\overline{i_L}(t) = \hat{i_L} \sin(\omega_o t) + \left[0.465 \cdot C_{in} \cdot \hat{V_1} \cdot \omega_o\right] \cos(3\omega_o t)\ [A]$$

At this point, by repeating the calculations presented earlier using these latest definitions, it becomes immediate to evaluate the current stress values affecting the switches, even under the hypothesis of overmodulation. The third harmonic component, in fact, not being able to circulate on the diodes since it does not transport active power to the load, does not alter the conduction losses suffered by the latter: the only ones to be affected are the switches, which must undergo the effect of a single phase current superimposed on a third harmonic current.

The sizing of diodes and switches also depends, as already mentioned, on the voltage and current stress to which they are subjected during the usual operation of the system; by the term "stress" we refer to the instantaneous peak values, of both voltage and current, to which the various components are subjected. It is, however, easy to observe how these can be considered identical for both components under consideration: the voltage stress to which both are subjected can be easily approximated by the half-bank voltage V_{dc}, while the current stress can be approximated by the average peak current of the inductor $\hat{i_L}$ mentioned above. The latter assumption can be considered acceptable since the current ripple, ignored in this case, affects no more than $20 - 30\%$ of the previous one: its contribution can thus be neglected assuming the use of typical design safety margins, which usually involve a factor 2.

FINAL CHOICES

According to what has just been presented it is then necessary to make some design choices, in order to define the values to be assigned to the various components used in the simulation. Regardless of the choices made by the factory, which will not be reported for reasons of company secrecy, we can consider the values given in the table 4.2 to be acceptable in order to realise a simulation that is fairly in accordance with reality.

components	Values	components	values
L_1, L_2, L_3	100 $[\mu H]$	$L_{1_{\text{ESR}}}$,$L_{2_{\text{ESR}}}$,$L_{3_{\text{ESR}}}$	0.1 $[\Omega]$
L_4	250 $[\mu H]$	$L_{4_{\text{ESR}}}$	0.2 $[\Omega]$
C_1, C_2	12 $[mF]$	$C_{1_{\text{ESR}}}$,$C_{2_{\text{ESR}}}$	0.02 $[\Omega]$
C_3, C_4, C_5	66 $[\mu H]$	$R_{C_{\text{ESR}}}$	$\sim$ 0.005 $[\Omega]$
R_{grid}	$\sim$ 0.1 $[\Omega]$	D_{ESR}	0.02 $[\Omega]$
L_{grid}	$\sim$ 5 $[\mu H]$	$C_{1_{\text{ESL}}}$,$C_{2_{\text{ESL}}}$	$\sim$ 1 $[nF]$
C_{grid}	$\sim$ 10 $[nF]$		

Table 4.2: Values assigned to the different components used in the simulation.

Clearly, the capacitances used can be physically realized through the use of entire banks of capacitors, connected in parallel with each other, allowing for the realisation of equivalent capacitors of 12 $[mF]$ as shown in the table 4.2.

All that remains to be defined, at this point, is the switching and sampling frequency to be used: the latter is set at f_{sw} = 18 $[kHz]$ as a result of certain considerations regarding the typical digital control structure, which will be briefly presented in the following chapter; the network frequency, instead, remains clearly fixed at f_{sw} = 60 $[Hz]$ according to North American standards.

4.2.2 Average Model

Before proceeding with the realisation of the control system it is worth taking a final look at the circuit structure of the Vienna Rectifer, trying to derive some transfer functions that will be useful in the study of the system's stability. Mathematically speaking, it is only possible to define a certain transfer function (t.f.) for LTI[10] systems. Clearly, our overall system cannot be considered linear as some components with non-linear characteristics, such as diodes and MOSFETs, are used. At the same time, the system cannot be considered time invariant either, as there is a continuous change of state by the various electrical switches during operation of the system, a common feature of every SMPS circuit.
As in all cases of power converters we are dealing with a *Variable Structure System*, which the solution by perfect analytical methods is unnecessarily complex to obtain. However, there are some mathematical techniques that can be used to study the average behaviour of the whole system, which are presented below:

1. "Time Averaging" (T.A.) : makes it possible to obtain, from a Variable Structure System, a continuous system capable of describing its average operation while maintaining the non-linear characteristics of the starting system;

2. "Steady State & Small Signal Analysis" : this technique consists, starting from a continuous non-linear system, in defining an operating point of the circuit of particular interest and then linearizing the trend of the real characteristic around the point just defined.

The characteristic linearised around the system's operating point can thus be considered as belonging to an LTI system equivalent to the starting system, thus allowing us to exploit it in order to derive the transfer function sought.
In the following pages we will attempt to exploit these methods, in order to derive some essential transfer functions for the study of system stability.
In order to understand which transfer functions will be useful, it is necessary to immediately define the control structure of the system to be used. As is usual for any type of power converter, it is advisable to use both a current control and a voltage control, one inside the other, in order to simplify the research of a stability point, while keeping both the output voltages and the inductor currents

[10]Linear and Time Invariant.

controlled; in this case we will use an average current control.

The type of control that will be implemented will then require the following transfer functions, in order to be represented correctly:

- $G_{d-i_L}(s) = \frac{\hat{i_L}(s)}{\hat{d}(s)}$: links the small variations conducted on the duty cycle to small variations relating to the inductor current that we want to control, a necessary relationship in order to create a Current Mode Control;

- $G_{G_{eq}-V_{out}}(s) = \frac{\hat{V_{out}}(s)}{\hat{G_{eq}}(s)}$: it allows us to convert a small variation in active input power into a small variation in output current, in order to keep the output voltage V_{out} constant.

We can immediately study the system by focusing on only one of the three current phases, using the single-phase model.
In fact, it is always possible to study a three-phase system, even without neutral, by considering the three current phases as independent, as long as the machine centre voltage is approximately constant and the voltages present on the half-banks can be considered equal. Clearly, the machine centre voltage cannot be considered to be constant if the overmodulation technique is used. Since, however, the machine centre voltage can at most assume a value equal to $\sim 15\%$ of $V_{in}(t)$ it is possible to consider it negligible, committing a small error, but being able to carry out the entire analysis.
We can also consider the models, obtained in the following pages, for the AC and DC sides to be decoupled. This is ensured by the different frequencies at which they work: the current control works at the switching frequency, which is much higher than the line frequency at which the voltage control works; this means that the variations imposed by the latter are completely irrelevant within a single switching period, in which the current control works.
This fact is ensured by realising a voltage control which is much slower than the current control, thus presenting clearly different control bandwidths[11].

[11]The internal current control is usually made much more performing than the voltage control: this allows to keep controlled a quantity affected by a high rate of variation in a very short time interval, as the current is. This choice also allows the stability of the voltage loop to be practically unaffected: the internal current loop, in fact, sets its poles at frequencies which are too high compared to the classic crossing frequencies common to classic voltage loops.

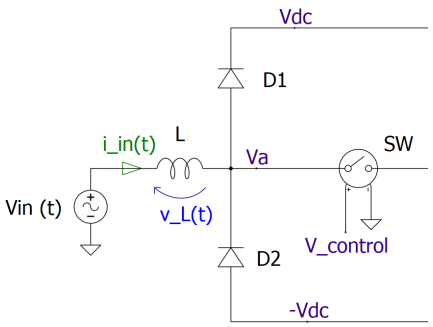


Figure 4.12: Portion of Vienna Rectifier Single Phase.

Research of $G_{d-i_L}(s)$

We can start, according to what was said earlier, by referring to the figure 4.12; we start by defining a variable $q(t)$ which we call *switching function* in such a way that it takes on different values, depending on the state of the SW switch and the sign possessed by the current $i_{in}(t)$:

$$q(t) = \begin{cases} 1 & SW \text{ is open with } i_{in}(t) > 0 \\ 0 & SW \text{ is closed} \\ -1 & SW \text{ is open with } i_{in}(t) < 0 \end{cases}$$

Using this function it is now possible to define the potential at which the node V_a can be found, during operation of the circuit, both as a function of the state owned by SW and the direction possessed by the current $i_{in}(t)$, under the assumption of work in CCM operation:

$$V_a(t) = \begin{cases} V_{dc} \simeq \frac{V_{out}}{2} \; [V] & q(t) = 1 \\ V_{\text{center}} \simeq 0 \; [V] & q(t) = 0 \\ -V_{dc} \simeq -\frac{V_{out}}{2} \; [V] & q(t) = -1 \end{cases}$$

At this point it becomes immediate to write:

$$v_L(t) = v_{in}(t) - v_a(t) \quad \Longrightarrow \quad L \cdot \frac{d}{dt}\big(i_{in}(t)\big) = v_{in}(t) - V_{dc} \cdot q(t) \; [V]$$

In order to obtain a time invariant system it is therefore possible to exploit the previously mentioned Time Averaging technique, based on averaging both parts contained in the previous equation within a single switching period. We then

get:

$$\overline{L \cdot \frac{d}{dt}\big(i_{in}(t)\big)} = \overline{v_{in}(t) - V_{dc}\big(1 - q(t)\big)} \quad \Longrightarrow \quad L \cdot \frac{d}{dt}\big(\overline{i_{in}(t)}\big) = \overline{v_{in}(t)} - \overline{V_{dc}} \cdot \overline{q(t)}\ [V]$$

It is now possible to write each variable $\overline{x}(t)$ as the sum of a certain operating point X and a small signal $\tilde{x}$, using the second mathematical method introduced above. Before proceeding, it is possible to assume, without loss of generality, $\overline{V_{dc}} = V_{dc} = \text{const.}$, effectively eliminating the dependence of the latter on the inductor current. This becomes possible from the fact that the output capacitances have such large values that the voltage present at their ends can practically always be considered constant.

Before proceeding, it is necessary to make a few observations regarding the variable $\overline{q(t)}$, as it is dependent on the type of modulator we are going to use: the choice of the latter is essential for this type of analysis, as it determines the shape to be taken by the modulating signal produced by the control itself, thus affecting the performance of the final result.

Although the choice of modulator will be adequately discussed in the next chapter, we can for now suggest that the use of a modulating signal that is proportional to the signal to be tracked brings several advantages to the control itself; one of these is undoubtedly the linearity introduced into the equation we are developing, which will make the t.f. sought independent of any operating point.

We then proceed by imposing $\overline{q(t)} = \delta(t)$, where $\delta(t)$ represents the modulating signal that will be compared with the PWM comparator[12]. Clearly, with respect to the duty-cycle $d(t)$, the relation $\delta(t) = 1 - d(t)$ must hold in order to keep valid the expressions obtained in the previous section.

As mentioned earlier, it is convenient to consider the effects resulting from the presence of the third current harmonic as negligible: its presence can be considered as a small variation superimposed on the operating point of the system itself, independently of the method by which it is generated.

Proceeding as described we obtain:

$$L \cdot \frac{d}{dt}\big(\hat{i_{in}}\big) = V_{IN}(t) + \hat{v_{in}} - V_{dc}\big(1 - D(t) - \hat{d}\big)\ [V]$$

[12]It was assumed that the modulator exploits a triangular signal with unity amplitude

from which we obtain:

$$L \cdot \frac{d}{dt}\left(\hat{i_{in}}\right) = V_{IN}(t) + \hat{v_{in}} - V_{dc}\left[1 - \left(1 - \frac{V_{IN}(t)}{V_{dc}}\right) - \hat{d}\right] [V]$$

from which:

$$L \cdot \frac{d}{dt}\left(\hat{i_{in}}\right) = V_{IN}(t) + \hat{v_{in}} - V_{IN}(t) + \hat{d} \cdot V_{dc} [V]$$

At this point we can apply the Laplace transform on both sides, also imposing $\hat{v_{in}} = 0\ [V]$ as it is useless for our purposes, thus obtaining the required ideal transfer function:

$$sL \cdot \hat{i_{in}} = \hat{\delta} \cdot V_{dc} \quad \Longrightarrow \quad G_{d-i_L}(s) \simeq \frac{\hat{i_{in}}(s)}{\hat{d}(s)} = \frac{V_{out}/2}{sL} \tag{4.11}$$

This relationship was obtained by making some implicit assumptions:

1. The inductor L was considered ideal;
2. At frequencies similar to the switching frequency, the line impedance is negligible compared to the impedance imposed by the relative input capacitance.

To make the equation just reported more realistic we could then:

1. Possibly add the parasitic resistance R_{ESL} in series with the inductor, resulting in an expression such as $G_{d-i_L}(s) = \frac{V_{out}/2}{sL+R_{ESL}}$;
2. Consider the voltage $V_{in}(t)$ as a function of line impedance, exploiting for example an equivalent representation developed using Thevenin or Norton. In this way we can easily consider the fact that there is a line impedance connected between the inductor and the line itself in addition to the input capacitor placed between the inductor and the earth potential, supported by the assumption $V_{center} \simeq 0\ [V]$.

Research of $G_{G_{eq}-V_{out}}(s)$

Differently from classical DC-DC converters, which work by maintaining a constant operating point for both inductor currents and output voltages, our system does not show similar characteristics: having to realise a PFC, in fact, the three inductor currents must exhibit a sinusoidal trend, which entails a continuous change of the system's operating point. For this reason, it is clear that the stability analysis of the system cannot be entirely conducted by means of the classical double-loop representation, realised exclusively by means of transfer functions, since there is certainly a variable quantity within the control structure which prevents the fixing of the classical operating point required for linearisation, thus impeding the separation of the latter from the small-signal model.
As will be shown later, this fact makes it impossible to stabilise the outer voltage loop using the classical theoretical approach. It is possible, however, to exploit the power conservation theorem, which clearly exhibits a constant operating point, thus allowing an equivalent transfer function to be derived between the active power required by the system and the power delivered at the output; this allows the operating point of the system to be separated from the small-signal contribution.

It is possible, at this point, to make the following assumptions:

1. The input current I_{in}, belonging to a certain phase, is proportional to the relative voltage line according to the relation $I_{in}(t) = G_{eq} \cdot V_{in}(t)\ [A]$;
2. The voltage regulator, implemented in the outer loop of the control system, will generate at steady state the constant contribution G_{eq} which, multiplied by the reference from the specifically scaled line voltage, will generate the sinusoidal current reference used for current control.

We then apply the power conservation theorem, exploiting the relationship just introduced:

$$3 \cdot V_{in_{RMS}} I_{in_{RMS}} = V_{out} \cdot I_{DC} \quad \Longrightarrow \quad 3 \cdot V_{in_{RMS}}^2 G_{eq} = V_{out} \cdot I_{DC}$$

Since the latter relationship is time invariant, it is already possible to apply the decomposition between operating point and small signal as follows:

$$3 \cdot V_{in_{RMS}}^2 \left(G_{EQ} + \hat{G_{eq}}\right) = \left(V_{OUT} + \hat{v_{out}}\right)\left(I_{DC} + \hat{i_{DC}}\right)$$

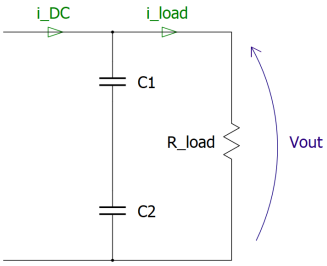


Figure 4.13: Model used to derive the transfer function between $\hat{i_{DC}}(s)$ and $\hat{v_{out}}(s)$.

We thus obtain the small-signal equation desired[13]:

$$3 \cdot V_{in_{RMS}}^2 \cdot \hat{G_{eq}} = V_{OUT} \cdot \hat{i_{DC}} + I_{DC} \cdot \hat{v_{out}}$$

From which:

$$\hat{i_{DC}} = 3 \cdot \frac{V_{in_{RMS}}^2}{V_{OUT}} \cdot \hat{G_{eq}} - \frac{I_{DC}}{V_{OUT}} \cdot \hat{v_{out}} = 3 \cdot \frac{V_{in_{RMS}}^2}{V_{OUT}} \cdot \hat{G_{eq}} - \frac{1}{R_{load}} \cdot \hat{v_{out}} \tag{4.12}$$

in which is visible the negative dynamic resistance present at the DC port, which is the opposite of the load resistance. It is also possible to interpret the previous relationship from the following point of view: if the input power does not change, the increase of $\hat{i_{DC}}$ must correspond to a decrease of $\hat{v_{out}}$.
It is possible, at this point, to search for a relationship between $\hat{i_{DC}}$ and $\hat{v_{out}}$. The transfer function that links the three-phase rectified current with the output voltage can be easily derived using the classical current divider formula: using average models we can avoid considering the presence of the machine centre node, effectively making the two output capacitances in series with each other. Defining then $C_{eq} = C_1 // C_2$ $[F]$ we can derive the required equation by modelling the system as shown in Fig. 4.13, from which:

$$\hat{v_{out}} = R_{load} \cdot \hat{i_{load}} = \frac{R_{load} \cdot \frac{1}{sC_{eq}}}{R_{load} + \frac{1}{sC_{eq}}} \cdot \hat{i_{DC}} \implies \frac{\hat{v_{out}}(s)}{\hat{i_{DC}}(s)} = \frac{R_{load}}{1 + s \cdot R_{load} C_{eq}} \ [\Omega] \tag{4.13}$$

By substituting, therefore, the equation 4.13 within the equation 4.12, the re-

[13] We can consider all products containing two variables at the small signals to be negligible, imposing $\hat{x} \cdot \hat{y} \simeq 0$.

quired relation is obtained:

$$G_{\text{Geq - Vout}}(s) = \frac{v_{out}(s)}{G_{eq}(s)} = \left(3 \cdot \frac{V_{in_{RMS}}^2}{V_{OUT}} \cdot \frac{R_{load}}{2}\right) \cdot \frac{1}{1 + s \cdot (C1//C2) \cdot (R_{load}/2)} \quad (4.14)$$

The pole of the system depends, therefore, on the serial capacity $C_{eq} = C_1//C_2$ $[F]$ and half of the load resistance R_{load}.

At this point, all the circuit-dependent transfer functions necessary for the study of system stability were derived. In the next chapter they will be used appropriately, after a brief introduction to the modelling of digitally controlled systems.

5

Exploration of Control Techniques

After having analized the electrical operation of the entire configuration under examination, we can now proceed to the control theory.
In this chapter, we will first present the main characteristics common to any digital control technique, followed by a discussion of the stability analysis for the system that will be implemented. We will then continue with the analysis of some digital controllers that can be implemented, initially focusing on the development of a functioning system without overmodulation. Finally, we will conclude by examining some implementable overmodulation techniques.

5.1 Digital control structure and stability theory

Digital control represents a branch of control theory based essentially on the management of analog dynamic systems through the use of digital electronic devices, such as microcontrollers or computers, exploiting a proper interface that allows the conversion of an analog signal into a digital signal and vice versa. Figure 5.1 illustrates the concept by showing the block diagram of a classic digitally controlled analog system: the digital controller generates the control signal $\hat{u_k}$ which is then converted into an analog signal by the actuator. This actuator includes a digital-to-analog converter (DAC) that converts $\hat{u_k}$ into a discrete amplitude analog signal, followed by an interpolator that transforms it into the continuous analog signal $u(t)$; the latter represents the control signal that is used to control the analog system concerned.

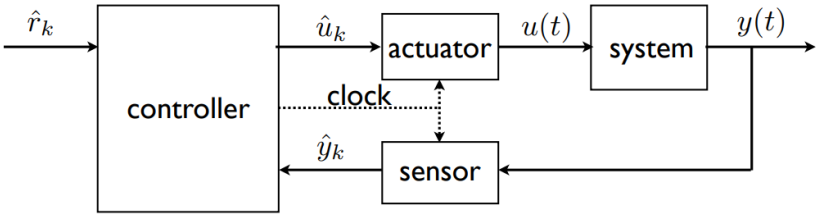


Figure 5.1: Generic structure of a classic digital control.

In order to implement feedback control, the quantity $y(t)$ to be controlled is measured, sampled, quantized, and discretized by the sensor shown in the same figure. This block represents an analog sensor, typically followed by an anti-aliasing filter, which is in turn followed by a sampler to convert the measured continuous analog signal into a discrete signal. An analog-to-digital converter (ADC) then provides the digital quantized signal $\hat{y}_k$ to the controller. This signal is finally compared with the reference digital signal $\hat{r}_k$ to generate an error signal, which is processed by the implemented digital controller and so producing the initial control signal $\hat{u}_k$.
Digital control technology undoubtedly offers numerous advantages over classic analog control; in the following there are some of them:

- **Reduced costs**: a cheap microprocessor can often easily replace the work done by an entire analog control system consisting of countless discrete components;

- **Flexibility**: any modification can be simply implemented by modifying the instructions used in the control software;

- **Simplicity of controller realisation**: unlike an analog controller, any necessary transfer function can be easily implemented by inserting a simple instruction within the realized code; an analog control must instead be implemented by suitably connecting various electrical components together, trying to obtain a transfer function equivalent to that required;

- **Reliability**: the various parameters used in the control are not dependent on any external conditions such as temperature, humidity, ageing, etc. as all the information required for control is stored within the digital system itself.

However, there are certainly some disadvantages that do not arise when using a traditional analog control:

- **Intrinsic control delays**: a digitally controlled system needs an internal clock to manage the sequence of operations. This creates a constant delay that can affect the control's performance;

- **Use of conversion blocks**: unlike in a generic analog control, ADC, DAC, samplers, interpolators and anti-aliasing filters must also be implemented. Fortunately, most of these conditioning blocks are often already included within any microcontroller or DSP that can be purchased;
- **Loss of accuracy**: unlike digital-analog-digital conversion, analog-digital-analog conversion cannot be carried out in an ideal way: the anti-aliasing filter can modify the real form of the signal to be discretized, the quantization introduced by ADC inexorably leads to partial loss of information, the interpolator used in a real-time control must necessarily represent a causal system, ineluctably introducing delay in the loop control, also altering the quality of the converted signal as a function of the interpolator used[1].

In order to realize an optimal digital control it is therefore necessary to take into account what has just been presented; in our case, we can make some simplifications within the simulation that will be realized:

- The on-board ADC present on the microcontroller used by the company turns out to be a 12-bit SAR ADC: since we are not interested in studying the quantisation effects on the overall system, it is possible to avoid including this block within the simulation program. This choice is supported by two important observations:
  - 12 bits turn out to be more than enough for our purposes, allowing us to overlook the presence of this block;
  - The ADC can be modelled as a unitary block to which a certain quantisation error with uniform probability density is added; since we can consider the quantisation error as a disturbance, its influence is clearly reduced by the fact that we are working on a feedback system.

- Regardless of the company's design choices, the insertion of anti-aliasing filters can be avoided within the simulation: working in an almost ideal world, there is no risk of operating with signals having frequencies higher than the switching frequencies, except during transients.
  Current sampling will also be made synchronous with the PWM, thus enabling sampling in the middle of the modulation period, automatically excluding the higher harmonics that make up the ripple itself: this technique will allow the ripple to be automatically filtered, avoiding aliasing phenomena by the ripple itself. However, it is possible to insert an equivalent block in order to obtain a simulation more faithful to reality.

[1]From the theory of digital control, it can be demonstrated that the optimal interpolator is the Shannon interpolator, which offers an impulsive response of the type $h(t) = sinc(t)$; however, possessing unlimited support and not representing a causal system, it clearly cannot be physically realised, forcing us to use different, non-ideal interpolators.

- Within the simulation it is also possible to neglect the presence of real probes, which have a limited bandwidth: an equivalent block can in any case be added in order to make the simulation more faithful to the real world.

Let us now analyze in more detail the main design choices that can be made regarding what has just been reported.

CHOICE OF INTERPOLATOR

The interpolator is clearly a block of fundamental importance within a digitally controlled system.
There are various types, both represented by LTI and non-LTI systems; limiting ourselves to LTI interpolators we can mention:

- Impulsive interpolator, having impulsive response of the type $h(t) = \delta(t)$;
- Zero-Holder, having an impulse response of the type $h(t) = \text{rect}_T(t) = \begin{cases} 1 & 0 \leq t < T \\ 0 & otherwise \end{cases}$
- One-Holder, having an impulsive response of the type $h(t) = \text{triang}_T(t)$
- Shannon interpolator, having an impulse response of the type $h(t) = sinc_T(t)$

Clearly, in order to realize real-time control, it is necessary to use a causal interpolator presenting a response of the type $h(t) = 0 \ \forall t < 0$, obviously with limited support. It is always possible, however, to truncate and to shift any impulsive response in order to make any of the interpolators just presented usable. In order to choose an interpolator with an acceptable delay and that can be easily implemented, so as not to overload the processor itself, it is better to choose the *One-Holder* which is the most commonly used interpolator in digital systems.
Referring again to Figure 5.1 we can then mathematically consider its contribution as follows.
The digital signal $\hat{u_k}$ is converted into a discrete analogue signal $u(kT)$ which is put as input to the interpolator, which generates the signal $u(t)$ through the convolution operation $u(t) = u(kT) * h(t) = \sum_{k=-\infty}^{+\infty} u(kT) \cdot h(t - kT)$.
Observing Fig. 5.2, the effect introduced by the same within the control loop becomes clear: the image shows a generic continuous signal $u(t)$ which has been discretized and made analogue again through the use of a holder, represented

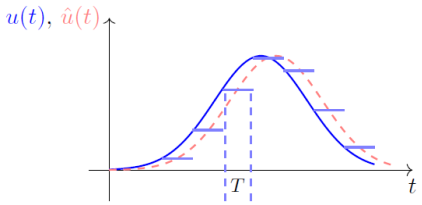


Figure 5.2: Effect of the delay introduced by the One Holder.

by the advancing blue bars within the same image. We can then consider that the equivalent generated signal is approximately represented by the pink signal $u\hat{(}t)$, which represents the shifted version of the original signal $u(t)$.

We can then approximately represent, within any block diagram, the interpolator just presented as a simple unitary block capable of introducing a delay equal to $\frac{T}{2}[s]$. Assuming then that we must place a One-Holder downstream of a generic continuous-time system, represented by the transfer function $P(s)$, we can treat the equivalent system formed by both as:

$$P_{eq}(s) \simeq P(s) \cdot e^{-s \cdot \frac{T}{2}}$$

It entails a loss of phase margin with respect to the use of the original single system $P(s)$; we can easily estimate the portion of phase margin subtracted due to the use of the One-Holder by knowing the crossing frequency f_c of the entire Bode diagram of the open loop system[2]:

$$\angle e^{-j \cdot 2\pi f_c \cdot \frac{T}{2}} = -2\pi f_c \cdot \frac{T}{2} = -\omega_c \cdot \frac{T}{2} \, [rad]$$

So, if a certain phase margin m_ϕ is to be ensured for the overall system, the existence of the Holder within the feedback loop can be neglected as long as a contribution is added to the phase margin required by the specification, knowing that this contribution will be lost due to the Holder being used, thus defining a new fictitious phase margin m'_ϕ:

$$m'_\phi = m_\phi + \omega_c \cdot \frac{T}{2} \, [rad]$$

[2]The holder, being represented by a t.f. having unitary modulus, only affects the phase trend of the system.

In our control system we can consider the presence of two Holders, one for the voltage controller and one for each current controller since, for implementation purposes, the sampling period implemented cannot be the same for all types of controllers. While the current loops require a fast control and at the same time a short sampling time, the voltage loop does not require the same speed of action, thus allowing us to set its sampling time at 4 times that of the current loop. This is due to the fact that, in order to exploit and improve the shared resources of the microcontroller used, the ADC used for voltage control is used in rotation to process additional signals within the UPS itself by means of a dedicated multiplexer, which only allows the output voltage to be sampled once every four clock periods. This clearly affects the delay introduced by the voltage Holder.
Knowing then that $T_{s_v} = 4 \cdot T_{s_i}$, we can assume that the delay introduced by the voltage Holder is:

$$\text{delay Holder}_v = \frac{T_{s_v}}{2} = 2 \cdot T_{s_i} \ [s]$$

The bandwidth of the voltage regulator will, however, be so tight that the delay introduced by the voltage Holder, at the frequencies of interest, can be neglected. Differently, the current holder will introduce a delay equal to:

$$\text{delay Holder}_i = \frac{T_{s_i}}{2} \ [s]$$

The discussion just carried out is, clearly, valid for a system that uses a Holder in order to generate a continuous signal to be compared with a carrier signal, which is also continuous, within the PWM modulator. In our case, in reality, the function of the Holder is realised implicitly within the PWM modulator: the comparison between modulating signal and carrier signal takes place, in fact, by digital way. As will be shown later, the PWM modulator will use a carrier signal of symmetrical triangular form; it can be shown that, a modulator of this type, introduces a delay equal to that introduced by a One-Holder followed by a PWM modulator: the treatment just presented is then correctly applicable also in our case, allowing us to model the system as if it really presents the Holders just described.

ANTI-ALIASING FILTER AND PROBES USED

Anti-aliasing filters are usually implemented in every digitally controlled system: they too, just like the Holder, influence and reduce the total phase margin of the overall loop; their influence clearly depends on the order of the filter to which they belong and the frequency range they attenuate. Regardless of the choices made by the company, we can, as a first approximation, assume the use of a simple first-order filter for both currents and voltages, since harmonics of a higher frequency, with respect to the sampling frequency, will practically never be introduced into the simulation itself, as will be demonstrated below.
We know, from Shannon's theorem, that only harmonics having a frequency greater than the sampling frequency f_s are subject to aliasing. Leaving aside a few possible transients we can easily state that the frequencies involved are much lower than f_s, also due to the fact that the same sampling will be carried out at strategic points in the period in such a way as not to include the influence of the current ripple in the various measurements, which is the only component consisting of frequencies higher than the sampling frequency. It is however possible to take into account the presence of an anti-aliasing filter by slightly increasing the phase margin required by specification, as done for the holder.
As for the probes used to measure, for example, currents, we can also assume them to be negligible since their contribution will only occur at very high frequencies compared to the crossing frequency. We can, however, introduce their contribution into the stability analysis by assuming we model them as:

$$H_{probe}(s) \simeq \frac{1}{1 + s \cdot \tau_{probe}}$$

This contribution is clearly negligible in the case where $\omega_c << \frac{1}{\tau_{probe}}\ [rad]$.

CHOICE OF SAMPLING PERIOD T_s

The choice of sampling period falls on multiple factors and is one of the fundamental parameters characterizing any digitally controlled system. As shown above, its value influences the phase margin subtracted by Holder and anti-aliasing filters, but not only; some examples follow:

- The microcontroller used needs a certain amount of time to be able to analyse the various sampled data, calculate the control signal and complete

the various active tasks. A criterion for choosing T_s can then be as follows: $T_s \geq \sum_{i=1}^{N} T_i \ [s]$, where T_i represents the computation time of the task "i";

- Another criterion of choice is based on the delay introduced in the sampling of rising or falling edges of any sampled signal; in the case where a certain signal changes, this will be sampled with a certain delay $\Delta \leq T_s$. Assuming then that the maximum variation can occur in a time t_r we can make the sampling delay negligible if the latter is at least one tenth of the variation time t_r, imposing $T_s \leq \frac{t_r}{10} \ [s]$;
- The choice of period T_s also affects, for example, the effect of the quantisation introduced by ADC on the computation of the discrete derivative. To give an example, it can be mathematically demonstrated that the error committed in the estimation of the discrete derivative through Euler is equal to err $\leq |\frac{\pm\Delta}{T_s}|$ where Δ represents the extension of an average quantisation step introduced by the ADC; in this case, the error is reduced by choosing a longer T_s.

Keeping this in mind it is important to recall that, in the context of converter control, the sampling period is determined principally as a function of the modulation period: the sampling period is usually set at a value equal to the modulation period itself or equal to half of it, sometimes even equal to an integer multiple of the latter when undersampling is desired. The modulation period is, among other things, defined by the performance required by the power circuit and cannot, therefore, be modified to much.

Following what has been reported, therefore, it is possible to choose an appropriate sampling period that takes into account the various aspects just presented. Following the company's choices we can then choose $T_{s_i} = 55 \ [us]$, by rounding the sampling frequency to the value of $f_s = \frac{1}{T_s} \simeq 18 \ [kHz]$ as already mentioned in the previous chapter.

METHOD OF STUDY: CONTROLLER DERIVATION

Before proceeding with the analysis of the entire feedback loop it is advisable to define from the outset the most suitable technique to be used to study the system, which comprises both a digital and an analogue part.
The literature offers numerous possibilities and different techniques to be used in order to consider a certain analogue t.f. in its equivalent digital counterpart or vice versa, thus obtaining a fully analogue or fully digital equivalent system. In our case, having to introduce some digital controllers inside a purely analogue

system, it is convenient to consider these controllers as analogue controllers and then derive their equivalent digital counterpart.
The analysis of the stability of the loop will then take place considering the overall system as purely analogue, exploiting the Laplace transform and the various Bode diagrams in order to study the stability of the system. The controllers $C_i(s)$ necessarily obtained will then be transformed into the equivalent digital configuration, thus obtaining an equivalent transfer function based on the Zeta transform, discrete counterpart of the Laplace transform. From the latter, we will obtain the mathematical expression to be inserted within the various instructions used by the control programme.

Among the various methods that can be used to approximate a certain $P(s)$ to a corresponding $P(z)$ we can mention the Invariance Method, the Matched Pole/Zero Method and the method based on the approximation of the derivative; based on the company's choices, the latter method will be used.
This type of derivation is based on the approximation of the derivative function to its equivalent discrete representation, thus allowing an approximate link to be found between the complex Laplace variable s and the complex variable z by the fact that the derivative itself can be rewritten within the Laplace domain, if continuous, or with the Z transform, if discrete. Among the methods that will be exploited we find *Backward Euler Method*" and the "*Tustin method*", both derived from this typology of study.
As an example, we can derive the "Backward Euler Method" as follows, looking for an equivalent discrete representation of the derivative function and then performing the Laplace transform on both sides:

$$L\left[\frac{d}{dt}x(t)\right] \sim L\left[\frac{x(t) - x(t - T_s)}{T_s}\right]$$

whence:

$$s \cdot X(s) \sim X(s) \cdot \frac{1 - e^{-s \cdot T_s}}{T_s}$$

where clearly the term $e^{-s \cdot T_s}$ represents the unitary delay function within the Laplace domain. Knowing that the same delay function can be described within the domain of the Z-transform as z^{-1} we can assume these two as equivalent, being able to substitute one for the other. By eliminating the terms in common

then we obtain:

$$s \sim \frac{1 - z^{-1}}{T_s} \tag{5.1}$$

which represents the discrete approximation based on the Backward Euler Method.
The Tustin Method, instead, uses a more precise approximation of the derivative function, based on the trapezoidal approximation of the result of an integral function that equivalently describes the discrete derivative function. The treatment is more complicated than the previous one, so only the result of the latter is given:

$$s \sim \frac{2}{T_s} \cdot \frac{z - 1}{z + 1} \tag{5.2}$$

Clearly, the Tustin approximation generates a discrete transfer function that is more accurate than using the Backward Euler Method, but it makes its calculation more complex and increases the calculation time required by the control. Depending on the level of precision required, therefore, we will decide whether to use one type of approximation rather than another.

CHOICE OF MODULATOR

As mentioned earlier, the choice of modulator influences the shape of the modulating signal to be generated by the control itself. Its characteristic affects the dynamic performance of the resulting system since the controller itself, being unable to possess infinite bandwidth, may struggle to generate signals with discontinuities or rising and falling edges that are too steep.
The fact of being able to use a modulator that allows the controller itself to generate a modulating signal proportional to the input voltage, as in this case, not only enables the latter to generate easily reproducible sinusoidal signals, but also ensures that a linear relationship is present between output voltage, input voltage and modulating signal itself.
This characteristic makes the operating point of the circuit independent of the stability of the system itself, as demonstrated for the transfer function of the Current Mode Control.
This fact can be easily explained by considering that although our system is composed by six boost converters, the type of modulation used allows the entire system to be controlled by exploiting a modulation characteristic of Buck converters which present the linear relationship $V_{out} = D(t) \cdot V_{in}(t)\ [V]$ between

input and output, in contrast to a generic boost stage where the non-linear relationship $V_{out} = \frac{1}{1-D(t)} \cdot V_{in}(t)\ [V]$ applies: it is, in fact, the linearity present in the control relation that makes operation independent of the operating point, since it obviously does not require any linearisation.
We then choose to use a PWM modulator consisting of an analogue comparator able to compare the modulating signal $\delta(t)$ with a carrier signal $w(t)$ generated by a series of analogue counters. $w(t)$ represents, in our case, a unitary triangular wave signal as $\delta(t) \in [-1, 1]$, subsequently rectified in order to obtain a modulating signal $\delta(t) \in [0, 1]$ so as to control the two switches of each phase with the same drive signal[3].
The modulator must then respond as follows:

$$\text{out}(t) = \begin{cases} 1 & |\delta(t)| \leq w(t) \\ 0 & otherwise \end{cases} \tag{5.3}$$

As a result of what has been said we can then derive the last transfer function needed to complete the study of the control loop, i.e. that relating to the PWM modulator.
Knowing in fact that $d(t) = 1 - |\delta(t)|$ and that $w(t) \in [0, 1]\ [V]$ we can now perform the usual small-signal analysis, obtaining:

$$D(t) + \hat{d} = 1 - |\Delta(t)| - \hat{\delta} \quad \Longrightarrow \quad D(t) + |\Delta(t)| + \hat{d} = 1 - \hat{\delta}$$

where clearly $D(t) + |\Delta(t)| = 1\ \forall t$; we then obtain the relation:

$$\hat{d} = -\hat{\delta} \quad \Longrightarrow \quad K_{PWM} = \frac{d(s)}{\delta(s)} = -1 \tag{5.4}$$

[3]The modulating signal $\delta(t)$ has a positive and a negative portion as $\delta(t) \in [-1, 1]$, where each portion controls in principle a different switch; rather than making two different modulators it is better to rectify the negative portion of $\delta(t)$ and drive the corresponding switch with it, using a single modulator. As explained in the previous chapter, however, there is no difference in commanding both switches with the same rectified signal since the direction of the current is defined by the polarity of the same input voltage. The introduction of the absolute value does not change the mathematical analysis carried out so far, as the control itself will continue to act as if nothing had happened.

STABILITY ANALYSIS

We are now finally ready to analyse the control loop of the entire system; Figure 5.3 represents the block diagram of the entire control structure, referring to a single current phase.
Starting from the left, it is possible to observe the voltage comparison block, the relative digital controller $C_V(z)$ followed by its Holder: its output is indicated with $\hat{G}_{eq}(s)$ and represents, expressed in Siemens [S], the single-phase RMS inductor current value to be assigned to each phase. The latter is then multiplied by the specifically scaled line voltage V_N in order to generate the sinusoidal current reference to be used within the current loop[4].
Neglecting for the moment the summing block, next we find the current loop, which also has its own digital controller $C_I(z)$ followed by the transfer functions previously derived. Within the same loop we also find a summing block that introduces the error variable $E_i(s)$: the latter simulates the presence of an ADC, which introduces an error represented by an aleatory variable $E_i(s)$ having a uniform probability density, with a value relative to the error that can be introduced by it. Inside the loop we then find the block $M_i(s)$ which represents the current probe used and the hypothetical anti-aliasing filter used.
It is also interesting to note that the current comparison block is inverted with respect to the voltage one: this ensures operation in negative feedback, reversing the sign previously inverted by the block[5] $K_{PWM}(s)$.
The output voltage V_{out} is then extracted from the block representing the circuit structure of the Vienna Rectifier, subsequently sampled by the corresponding ADC which introduces the error $E_v(s)$.
Within the same control structure there are two summing rings that have not yet been named, which introduce two different signals:

1. $ff(s)$: represents the feed-forward signal, which may be introduced into the control; the introduction of the latter may be justified by:

    - Necessity to help the controller to realise the required modulating signal. If the shape that the latter must take is known from the outset,

[4]in fact, the signal $\hat{G}_{eq}(s)$ uses conductance as the unit of measurement because, when multiplied by the voltage $V_N(t)$, it results in the reference current expressed in $[A]$.

[5]The same result could be obtained by transforming the summing ring used to inject $ff(s)$ into a comparison block; the choice turns out to be indifferent as long as the negative feedback is maintained.

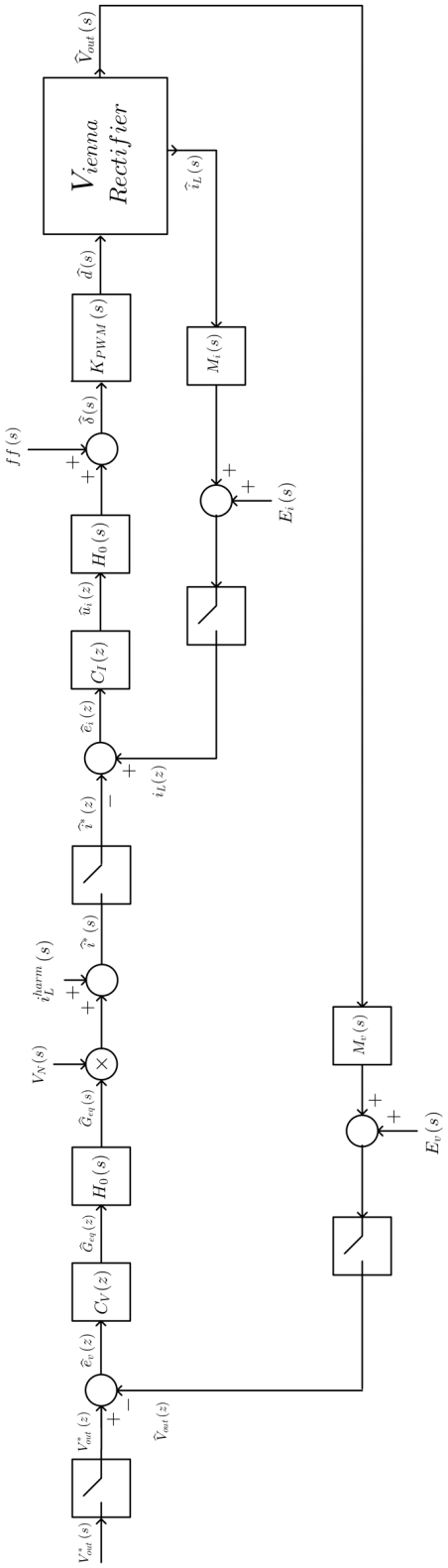


Figure 5.3: Block diagram of the entire control structure.

the feed-forward signal can be injected directly after the controller: the latter, already having a pre-calculated form at its output, will limit its contribution in correcting the small variations that the latter signal does not take into account; this allows the controller to work with more precision, thus generating a more accurate result;

- Implement the modulating component relating to third harmonic injection. In fact, in the chapter dedicated to the injection of the third harmonic, two different implementation possibilities will be analysed: one relating to the introduction of the pre-calculated modulating signal, relative to the third harmonic of current, directly at the output of the regulator and one based on the addition of a third harmonic directly into the reference signal.

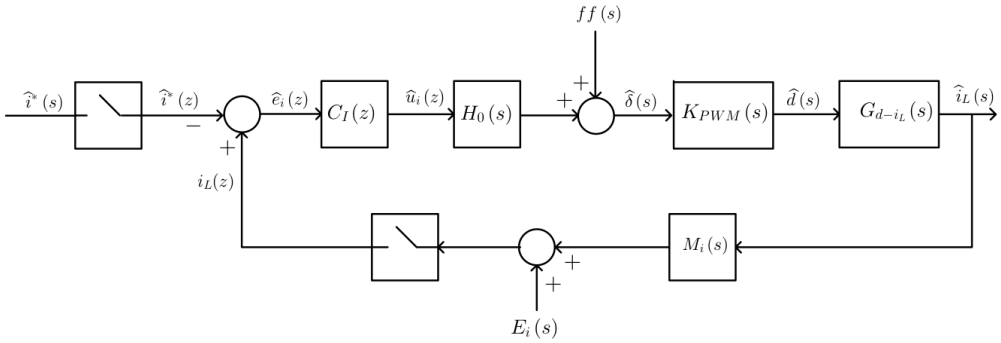
2. i_L^{harm}(s): represents the possible third harmonic reference that can be used in the case in which we want to inject the third harmonic directly into the current control reference; the block diagram just presented is designed to be as generic as possible, and therefore includes all working possibilities; however, this solution will be analysed in the appropriate chapter.

In order to derive the information required to realise a good controller $C_I(z)$ it is clearly worth starting with the internal current loop, shown in Figure 5.4(a); within the latter there is also the transfer function $G_{d-i_L}(s)$ derived in the previous chapter. As previously reported, we can neglect the error contribution $E_i(s)$, as we are not interested in studying its influence in the system; using the study method previously reported it is then possible to redraw the block diagram of the entire current loop as shown in Figure 5.4 (b), in which the presence of the equivalent controller $C_I(s)$ is emphasised.

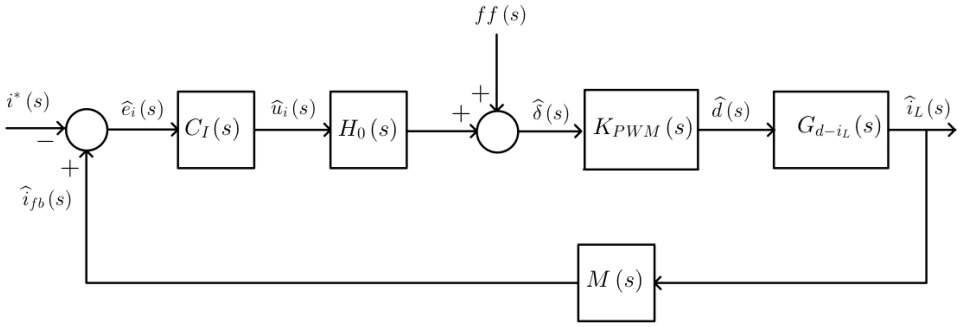
We can now make one last assumption: the signal $ff(s)$, independently of what information it carries, can be considered as a disturbance since it is injected at an intermediate point in the loop itself and therefore its contribution can be neglected, since it is inserted within a feedback system[6]. This last statement is, in reality, the result of an approximation which allows us to study the loop in a simplified way: the signal $ff(s)$ has, indeed, an influence on the signal V_N used as an oscillating reference, since the presence of the line impedance shapes the form of the voltage used as a reference in the corresponding current control. The

[6]Feedback, among its various advantages, presents a strong rejection of disturbances: this can be considered valid, to a first approximation, for both the signal $ff(s)$ and the signal $E_i(S)$.

overall system should actually be studied using an additional feedback loop, in this case clearly negligible.



(a)



(b)

Figure 5.4: Small-signal model of the entire current loop (a); suitable model for current controller derivation (b).

Following these observations, we can finally calculate the open loop current gain $L_I(s)$, which can be derived by analysing the structure of the overall loop. Basing ourselves on the Figure 5.4 (b) we can denote by $A(s)$ the whole of the blocks present in the upper branch and by $B(s)$ the block present in the lower branch; it is then immediate to prove that:

$$\frac{\hat{i_L}(s)}{i^*(s)} = \frac{-A(s)}{1 - A(s)B(s)}$$

where clearly the presence of the block $K_{PWM}(s) \in A(s) = -1$ re-establishes the order of the signs, as anticipated above, obtaining the classical expression of a feedback system.

We can then describe the open loop current gain as:

$$L_I(s) = -1 \cdot C_I(s) \cdot H_o(s) \cdot K_{PWM}(s) \cdot G_{\text{d-iL}}(s) \cdot M_i(s)$$

from which we obtain, simplifying:

$$L'_I(s) = C_I(s) \cdot H_o(s) \cdot G_{\text{d-iL}}(s) \cdot M_i(s) \tag{5.5}$$

At this point it is clear that, depending on the type of controller $C_I(s)$ we want to realise, it may be easier to study the system by graphical or analytical way. Assuming, however, that we require a certain crossing frequency $\omega_c^* = 2 \cdot \pi \cdot f_c^*$, in which the phase margin of the system should be m_ϕ, we can impose the following design conditions, removing the term $H_o(s)$ from the expression 5.5 in accordance with the study method previously described:

$$\begin{cases} |C_I(j\omega_c^*)| \cdot |G_{\text{d-iL}}(j\omega_c^*)| \cdot |M_i(j\omega_c^*)| = 1 + j0 \\ \pi + \left[\angle C_I(j\omega_c^*) + \angle G_{\text{d-iL}}(j\omega_c^*) + \angle M_i(j\omega_c^*) \right] \geq m_\phi^* = m_\phi + \omega_c^* \cdot \frac{T_s}{2} \ [rad] \end{cases}$$

from which we get:

$$\begin{cases} |C_I(j\omega_c^*)| = \frac{1}{|G_{\text{d-iL}}(j\omega_c^*)| \cdot |M_i(j\omega_c^*)|} \\ \angle C_I(j\omega_c^*) \geq m_\phi^* - \angle G_{\text{d-iL}}(j\omega_c^*) - \angle M_i(j\omega_c^*) - \pi \ [rad] \end{cases} \tag{5.6}$$

The system of equations 5.6 just derived will be used in the following paragraphs in order to design suitable current controllers according to their typology; in fact, the number of parameters contained within the same controller suggests the most suitable design method to be applied.
Clearly, after having derived the final expression of $C_I(s)$, it becomes immediate to obtain the equivalent digital controller $C_I(z)$ using the approximations derived from the *Backward Euler Method* or the *Tustin method* previously described.

At this point all that remains is to derive the voltage controller $C_V(z)$; we can then redraw the entire system as we did previously for the current loop, keeping the same assumptions valid, obtaining the scheme shown in Figure 5.5. Inside it, the current loop has been replaced by the equivalent block $T_i(s)$: knowing that the bandwidth of the current control is certainly much higher with respect

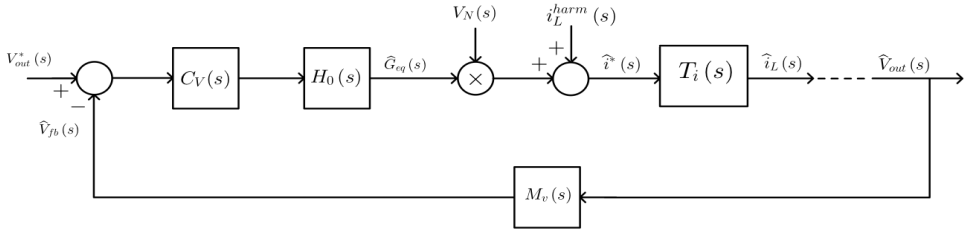


Figure 5.5: Small-signal model referring to the voltage loop, remodelled as one continuous-time system.

to that of the voltage control, it is possible to assert that:

$$T_i(s) \simeq 1$$

which allows us to assume the presence of perfect phase current control, as well as total decoupling between voltage and current control, greatly simplifies the study of the system.

As shown in Section 4.2.2, the presence of the variable contribution $V_N(s)$ makes it impossible to perform the stability analysis of the voltage loop using only the transfer functions shown in Figure 5.1, since the system's operating point varies instant by instant: the discussion must therefore be extended by exploiting the theorem of conservation of power, in order to derive the transfer function $G_{\text{Geq - Vout}}(s)$ previously derived, thus allowing us to fix the system's operating point from the point of view of the active power called up at the input, which is clearly a constant value.
Therefore, taking the equation 4.14 and substituting the term $V_{in_{RMS}}\ [V]$ with $V_N = \frac{V_{in_{RMS}}}{K}\ [V]$, where K represents the normalisation factor used, it is possible to define the open-loop function related to the voltage loop as:

$$L_V(s) = C_V(s) \cdot H_o(s) \cdot G_{\text{Geq - Vout}}(s) \cdot M_v(s) \tag{5.7}$$

At this point it is easy to derive the complete expression of $C_V(s)$, proceeding as shown for the current loop; we then obtain:

$$\begin{cases} |C_V(j\omega^*_{cv})| = \frac{1}{|G_{\text{Geq - Vout}}(j\omega^*_{cv})| \cdot |M_v(j\omega^*_{cv})|} \\ \angle C_V(j\omega^*_{cv}) \geq m^*_\phi - \angle G_{\text{Geq - Vout}}(j\omega^*_{cv}) - \angle M_v(j\omega^*_{cv}) - \pi\ [rad] \end{cases} \tag{5.8}$$

where ω^*_{cv} $[rad/s]$ represents the relative crossing frequency, and $m^*_\phi = m_\phi + \omega^*_{cv} \cdot 2 \cdot T_s$ $[rad]$. It is important to set ω^*_{cv} $[rad/s]$ at a frequency lower than the line frequency, thus preventing the voltage loop from following the generated contribution of the fluctuating power conducted by each phase, by only tracking the active power required by the load.
Clearly, additional scaling factors were to be used within the real system or simulation, e.g. to adapt the current and voltage values to the respective ADCs and probes, they must also be considered in the analysis just conducted.

Bank balancer: typology of control used

Having studied the entire system by means of small-signal analysis, it now remains to evaluate the control possibilities of the previously introduced bank balancer. The first control hypothesis is based on an open-loop operation with duty cycle set at 50% for each switch present: referring again to Fig. 4.6 it is in fact possible to use a logic of the type $V_{\text{driver 4}} = \overline{V_{\text{driver 5}}}$ such that each half-bank imposes the same voltage on the opposite half-bank, being a bidirectional buck-boost converter.
This type of control implies constant CCM operation, by flowing the classical triangular current with constant mean value through the respective inductor; being in CCM operation is valid, for each stage, the relation $M = \frac{D}{1-D} = 1$ where $D = \frac{1}{2}$. This solution does not require any kind of feedback control, making it easier to handle the overall system; however, forcing continuous operation in CCM results in higher losses than those introduced by other solutions, caused by the non-ideality of the coil and capacitors, present on each half-bank.

An alternative solution could be based on the feedback control of the bidirectional converter by means of two control loops, one of current and one of voltage. In fact, an additional comparison block could be inserted to control the voltage present on the two buck-boosts, calculating the difference between the two and trying to follow the null reference value.
In this case the system would track the reference 0 $[V]$ through small continuous adjustments, performed on the output voltages, working sporadically and only in DCM. Wanting to realise a similar system we could conduct a small-signal analysis similar to the one presented above, deriving the transfer function rela-

tive to a bidirectional buck-boost working in DCM and stabilising it as shown. This solution obviously involves a more impressive use of resources as it requires two additional controllers, while gaining on the losses generated as its operation would be sporadic and not continuous.

A third solution, already mentioned above, consists in avoiding the insertion of a bidirectional converter on the condition that the output unbalances are controlled directly by acting on the inductor currents via an additional control loop: the same comparison block presented in the previous solution can be implemented in order to generate an extra current contribution to be added to the current phases, so as to influence the charge of the most discharged capacitor.
This solution minimises conducted losses as it avoids the insertion of an extra converter but makes the realisation of the total control more complex, as the contribution of an extra control loop within the current loop shown above would be added. In the two previous solutions, on the other hand, the insertion of the dedicated converter made it possible to separate the two controls, simplifying the realisation of each one.
Regardless of what is done in the factory, we can choose to use the first solution proposed within the simulation program, in order to speed up the simulation itself and avoid burdening it with controls that are not strictly necessary.

5.2 Control without overmodulation

Having finally defined the entire control structure we can now proceed to the research phase for the most optimal controller to be used, both for current and voltage control; the next sections will present the different types of controllers developed and tested during the system study phase. For the moment we will only discuss control without overmodulation: third harmonic injection will be dealt with at the end of the chapter.

5.2.1 PI control: analysis and considerations

The first type of controller implemented was the classic PI, for both current and voltage loop.
This type of controller, which is used in a multitude of different fields, allows excellent performance in different contexts depending on the type of reference signal to be tracked.
As is well known, the ideal PI controller can be defined by the following relationship:

$$u(t) = K_p \cdot e(t) + K_i \int_{-\infty}^{t} e(\tau)\, d\tau$$

which clearly can be represented in Laplace's domain as:

$$G_{PI}(s) = \frac{U(s)}{E(s)} = K_p + \frac{K_i}{s} \tag{5.9}$$

The principle of the internal model, derived from control theory, demonstrates how the pole in zero introduced by the PI itself allows a hypothetical step reference to be tracked with zero error, assuming that the open-loop gain $L(s)$, which contains the same t.f. of the PI, contains no further poles in zero. In the event that the expression $L(s)$ contained one or more poles in zero, the type of reference chaseable with zero error would become a ramp, a parabola, a cubic etc., respectively, but never a sinusoid.
This characteristic is easily demonstrated by the fact that these types of references present multiple poles in zero when considered within Laplace's domain, unlike a sinusoid which is represented by means of a rational fractional function with a complex conjugate denominator, thus translated in s. The fact that the latter is translated does not permit perfect tracking by this type of control, regardless of the number of poles in zero introduced.

It becomes interesting to analyse this phenomenon mathematically, which will be more useful later on. The use of a PI, in accordance with the principle of the internal model, is perfect for tracking signals of the type $r(t) = k \cdot t^n$ where $k = \frac{r_o}{(n-1)!}$, whose Laplace transform turns out to be $R(s) = \frac{r_o}{s^{n+1}}$. We can now highlight the number of poles in zero contained in the loop gain $L(s)$, in which the same PI is contained, exploiting the form $L(s) = \frac{L_o(s)}{s^k}$; exploiting the final value theorem we can then calculate the error $e(t)$ present at steady state, exploiting for simplicity a system having a unity feedback loop:

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} s \cdot E(s) = \lim_{s\to 0} s \cdot \frac{1}{1+L(s)} \cdot R(s) = \lim_{s\to 0} s \cdot \frac{s^k}{s^k + L_o(s)} \cdot \frac{r_o}{s^{n+1}}$$

from which it is clear that:

$$\lim_{t\to\infty} e(t) = 0 \iff k > n$$

We can take advantage of this type of analysis by concluding that, for the voltage controller, the use of a PI is perfect as it allows zero-error tracking of the step reference to which it is subjected. On the contrary, a PI will not be able to ensure zero error at steady state for any current sine wave, as the latter does not fall within the cases considered above.
Although the PI cannot ensure zero error for the desired current reference, this does not mean that it cannot make the latter so small as to be considered negligible.
Consider, for simplicity's sake, an $H(s)$ LTI system consisting of a unity feedback loop, at the input of which is placed the reference sinusoid $x(t) = A \cdot \sin(\omega_o t + \phi)$. We now consider steady-state operation by imposing $t \to \infty$, which allows to consider any transient to be concluded, allowing us to study the system's steady-state operation by Fourier Transform rather than Laplace, thus posing $s = \sigma + j\omega \sim j\omega$. We can then mathematically demonstrate the following relationship:

$$Y(j\omega) = H(j\omega) \cdot X(j\omega) \implies y(t) = A \cdot |H(j\omega_o)| \cdot \sin[\omega_o t + \phi + \angle H(j\omega_o)]$$

it is then clear that, leaving aside the phase shift introduced by the system, the two input and output sinusoids tend to assume the same amplitude value if is valid the approximation $|H(j\omega_o)| = |\frac{L(j\omega_o)}{1+L(j\omega_o)}| \sim 1$.

This means that if the Bode diagram relating to $L(j\omega)$ has a sufficiently high magnitude value at the point $\omega = \omega_o$, the approximation just presented becomes valid, allowing the system to track the input sinusoid with negligible error at the cost of a slight phase shift.
This assertion leads us to the conclusion that a feedback system $H(s)$ allows excellent amplitude tracking for each sinusoidal input, as long as its loop gain $L(s = j\omega)$ has a sufficiently high modulus gain for each frequency concerned.
In this regard, a PI can be used to increase the magnitude of the loop gain $L(j\omega)$ at the pulsation $\omega = \omega_o$ enough to allow a good tracking by the system; its bandwidth can therefore be extended enough to greatly increase the tracking performance of the system itself.
By rearranging the equation 5.9 we can obtain the form:

$$G_{PI}(s) = \frac{K_i}{s} \cdot \left(1 + \frac{K_p}{K_i} \cdot s\right)$$

which allows us to make two observations:

1. The integral part allows the value of $|G_{PI}(s)|$ to be greatly increased at relatively low frequencies;

2. The proportional part introduces a zero which cancels the phase shift introduced by the PI itself at high frequencies.

Having to work with relatively low frequencies, the PI can then also be used within the current loop, exploiting the integral part to reduce the steady-state error and the proportional part to stabilise the system itself; clearly, the proportional part introduces a limit to the level of attenuation provided by the PI at high frequencies.
Having to realise a PFC, the delay introduced by the overall system can clearly be a problem: although the PI allows for improved tracking of the reference itself, it unfortunately introduces phase delay, which is certainly mitigated by the presence of a feedback loop but still present in the overall system.
As mentioned above, an implementable solution to mitigate the problem could be to exploit the feed-forward signal by injecting a pre-calculated contribution, having the same form as the required modulating signal, into the output of the current PI. It is possible in this way to slightly increase the parameters of the PI itself with respect to those calculated by means of the small-signal analysis, since the signal $ff(s)$ does most of the work that the controller itself should do;

the latter will simply carry out small corrections with respect to what the signal $ff(s)$ does, reducing the effect of the phase delay introduced by the controller itself.

It is convenient to carry out a few tests by means of simulation, in order to evaluate the effects introduced by the delay: first of all, we have to obtain the discrete PI expression to be inserted in the form of an instruction into the control program. Since the latter is not particularly sensitive, it can be discretised without any problems using the Backward Euler Method in order to minimise the impact introduced on the performance of the microcontroller used.
Basing on the equation 5.9 we can apply the approximation 5.1, obtaining:

$$G_{PI}(z) = \frac{U(z)}{E(z)} = K_p + \frac{K_i \cdot T_s}{1 - z^{-1}}$$

from which:

$$U(z) = K_p \cdot E(z) + \frac{K_i \cdot T_s}{1 - z^{-1}} \cdot E(z) \implies U(z) = U_p(z) + U_i(z)$$

Using the anti-transform Z it is then obvious to obtain:

$$\begin{cases} U(z) = U_p(z) + U_i(z) \\ U_p(z) = K_p \cdot E(z) \\ U_i(z) = \frac{K_i \cdot T_s}{1 - z^{-1}} \cdot E(z) \end{cases} \implies \begin{cases} u(k) = u_p(k) + u_i(k) \\ u_p(k) = K_p \cdot e(k) \\ u_i(k) = K_i T_s \cdot e(k) + u_i(k-1) \end{cases}$$

It is then possible to realise a digital PI using the previous equations, clearly written in the form of instructions; the integral memory $u_i(k-1)$ must obviously be updated at each cycle, imposing $u_i(k-1) = u_i(k)$ before dealing with a new calculation of $u_i(k)$. Obviously, using an integral component will require the addition of a digital anti-windup filter.

In order to try out and test the various controllers realised, it was necessary to take advantage of a simpler and gaunt simulation model with respect to the three-phase model. Figure 5.6 shows the respective mono-phase circuit of the Vienna Rectifier, provided with all the necessary blocks for simulation, which was realised specifically for this case study.
Starting from the left, we find the conditioning block in which the various

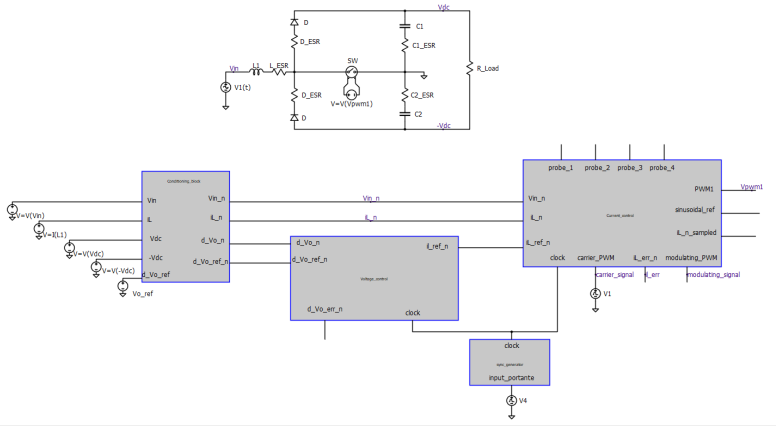


Figure 5.6: Simulation model relating to the single-phase configuration of the Vienna Rectifier, used to test the performance offered by different types of digital controls within a simplified model.

scaling factors are applied to the signals measured by the probes, which are implemented via controlled voltage generators. Continuing to the right, we find the digital block that simulates voltage control and that which simulates current control, while the smallest digital block represents a synchronism generator which generates the clock signal. The switch in the circuit is obviously controlled by the "PWM1" signal, provided as output by the current controller. The content of the various digital blocks, each of them programmed in C language, will be subsequently readjusted in order to create the control system of the complete three-phase network: we will focus later on the content of these blocks, currently only shown for completeness.

After having correctly calibrated the various blocks, it is possible to carry out a few tests: Figure 5.7 shows the performance achieved by a current control based on a classical PI, without the addition of feed-forward or other strategies, which shows the modulating signal generated by the PI itself (in red) and the inductor current (in blue). The delay introduced by the PI becomes visible as the modulating signal produced remains out of phase with respect to the reference input voltage: when the latter changes polarity it forces the current to do the same, inexorably generating current peaks, since the modulating signal, being delayed, has polarity opposite to that which it should have. The latter is thus forced to deal with sharper peaks in order to eliminate the introduced error as quickly as possible, never being able to correct it, due to the fact that the delay

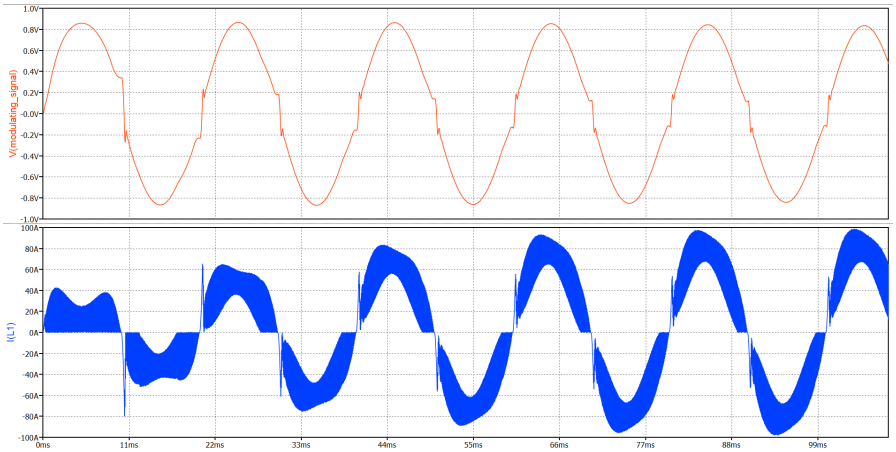


Figure 5.7: Performance of a current PI controller tested on a single-phase system without using Feed-Forward. The signal in red represents the modulating signal, the one in blue represents the inductor current; test conditions: $R_{Load} = 50\ [\Omega]$, $V_{out} = 760\ [V]$, $V_{\text{i peak}} = 325\ [V]$.

is intrinsic to the control itself; this obviously generates distortion.
In order to improve the performance obtained, it is possible to inject a feed-forward signal as previously mentioned; it is also possible to add some expedients in order to further reduce the distortion produced by the control, for example by acting on the memory of the integral part at the most critical points of the period.
Figure 5.8 shows the result generated by the implementation of what has just been presented: the modulating signal (in red) and the inductor current (in blue) have this time a sinusoidal and practically distortion-free shape. The signal in green, instead, represents the contribution generated by the PI controller, isolated with respect to the feed-forward signal, which clearly generates a limited contribution compared to the latter.

At this point, having achieved excellent results with the single-phase model, we are ready to implement the equivalent control for the three-phase system.
The implementation will be very similar to that used for the single-phase control, which however includes three current controllers rather than just one.
By exploiting the circuit previously shown in Figure 4.7, it is then possible to realise a suitable digital control, such as the one shown in Figure 5.9. Starting from the left, we find two digital blocks which operate as a conditioning block, kept separate for simplicity. We then find the voltage controller, the synchronism

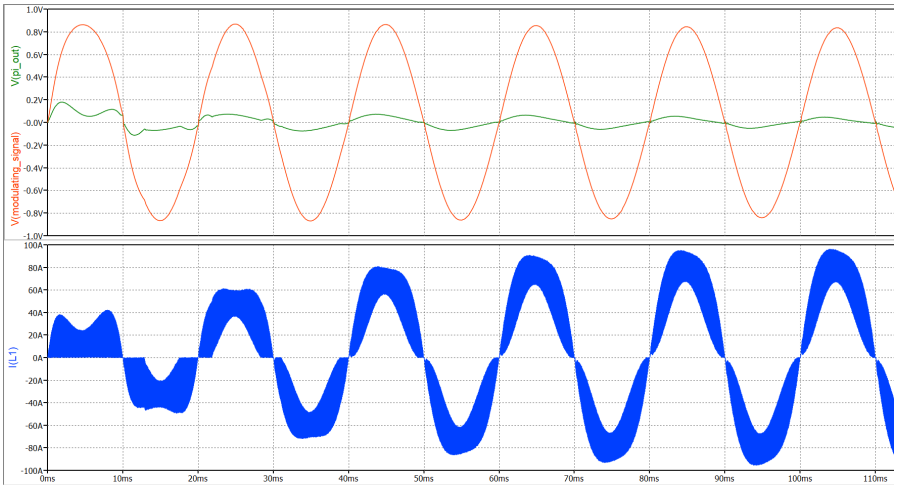


Figure 5.8: Performance of a current PI controller tested on a single-phase system, with the aid of the feed-forward: the modulating signal is shown in red, the coil current in blue and the contribution generated by the integral/proportional part in green. $R_{Load} = 50\ [\Omega]$, $V_{out} = 760\ [V]$, $V_{\text{i peak}} = 325\ [V]$.

generator and the three current controllers, one for each phase; these clearly control the relative switches located in the overall circuit system.
The contents of these digital blocks will be discussed at the end of the chapter, after having added the necessary controls for handling overmodulation, in order to avoid redundancy of content.

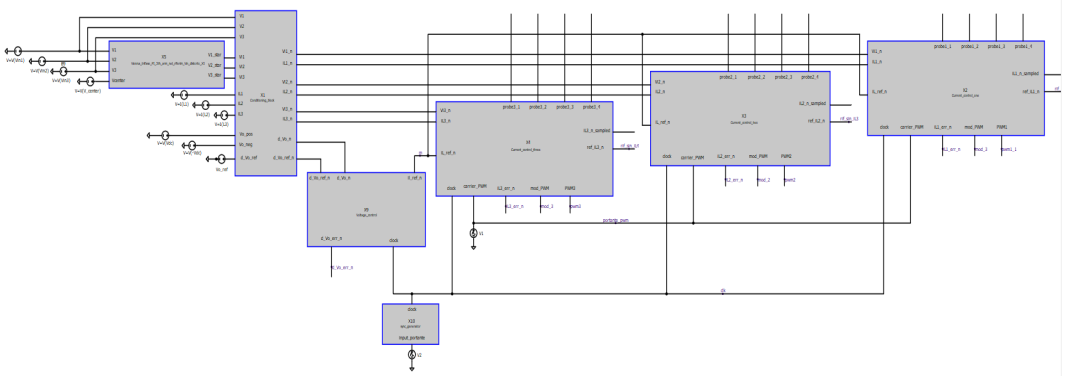


Figure 5.9: Simulation component related to digital control, implemented in order to control the full three-phase network of the Vienna Rectifier.

The only conceptual difference in this control scheme, compared to the one used for the single-phase system, is the presence of the double conditioning block: the purpose of the additional block is to mathematically calculate the voltage value present on the neutral cable, which is accessible in simulation,

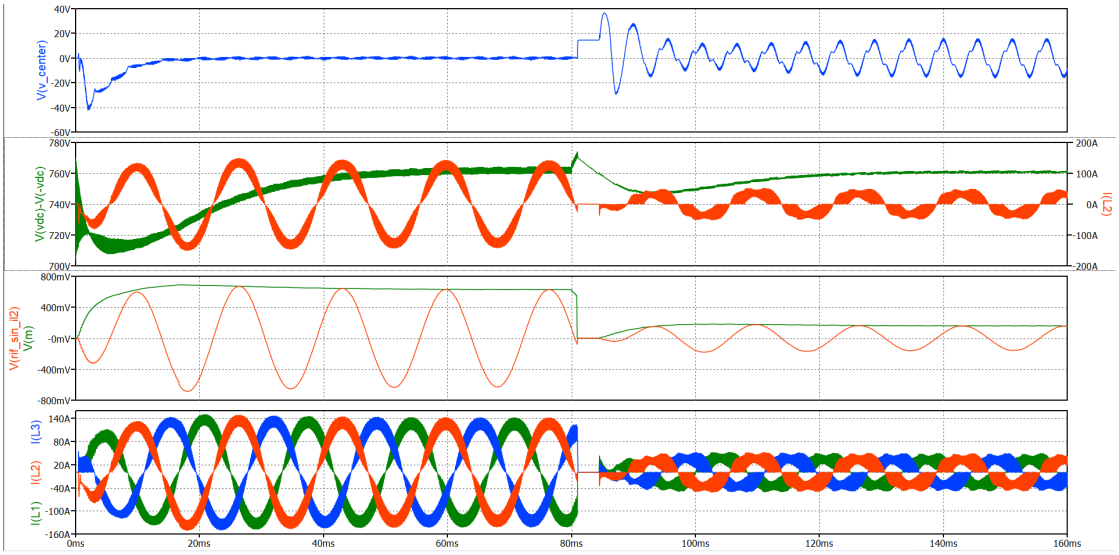


Figure 5.10: Main waveforms generated during the simulation, inherent to the complete three-phase system, realised with three current PI controllers and one voltage controller.

but not in the real machine. As there is no access to the neutral cable, all measurements taken by the probes are referred to the voltage at the centre of the machine, which may be at a different potential to the neutral potential; this block therefore acts as a neutral potential calculator, thus being able to refer all measurements performed to a constant reference potential, calculated mathematically.

The functioning of this block will be slightly mentioned at the end of the chapter: for now it can be neglected as, in our conditions, it is not able to introduce any error component[7]. As a test phase, it is advisable to use a line voltage lower than the actual one: as no overmodulation technique is currently implemented, it becomes impossible to handle a voltage bank of 760 $[V]$. We will then use the following test conditions: $V_{out} = 760\ [V]$, $V_{\text{i peak}} = 325\ [V]$, $R_{Load} = 10\ [\Omega] \rightarrow 40\ [\Omega]$ in order to simulate a load change; the result obtained is visible in Figure 5.10.

The image shows some of the more interesting waveforms produced by the simulation performed: the first quadrant shows the machine centre voltage (in

[7]It will later be emphasised that this conditioning block cannot introduce any error component unless there are parasitic harmonics within the line voltage, which are not included in this test phase.

blue), the second shows one of the three inductor currents (in red) together with the output voltage V_{out} (in green). The third contains the output signal generated by the voltage PI (in green) together with the normalised current reference, relative to the inductor current, present in the previous quadrant (in red), while the last quadrant shows the tri-phase current generated.
We can make, in this regard, some interesting observations:

- During the initial transient, the voltage V_{out} reaches a minimum voltage of 710 $[V]$; this is the result of the slow dynamics of the voltage PI, which is designed in such a way that it does not introduce overshoot, but at the same time does not allow higher performance response without incurring into stability problems[8]. Not being able to act further on the parameters of the voltage PI, it is possible to modify the structure of the latter in order to obtain a dynamic variation of the parameters K_i and K_p, during the operation of the system, realising a PI with a non-linear response. it is in fact possible to define dynamic parameters, thus increasing the response speed of the controller when strictly necessary: Figure 5.11 shows a simplified example, in which the parameter K_p becomes $K'_p = K_p + U_v(e_v(t))$ where $U_v(e_v(t)) \in [U_{min}, U_{max}]$ as a function of the voltage error present;

- A similar precaution was introduced during load change, forcing the current control to switch off if the voltage V_{out} should rise above a certain range, with respect to the nominal output voltage;

- Using a load of 10 [Ω] the inductor currents seem to exhibit practically zero distortion; as the output resistance is increased, the shape assumed by them appear to become slightly distorted, becoming more and more pronounced as the load resistance is increased. Clearly, with the load equal to 40 [Ω] we bring the inductor currents to work in both DCM and CCM, in contrast to the former case in which the working zone practically always remains in CCM operation;

- The machine centre voltage is, in some way, influenced by the shape assumed by the inductor currents, presenting an oscillation with frequency $f_{CM} = 3 \cdot f_o$ $[Hz]$ and variable amplitude, negligible in the first case but not in the second. We will discuss this topic later, in the chapter dedicated to the movement of the machine centre voltage.

In order to achieve better waveforms it is possible to exploit more complex controls, or for example to implement a feed-forward signal that takes into account the fact that we are working in CCM or DCM. In any case we can be

[8]Clearly, this kind of slow dynamic is a source of many problems since, below a certain voltage threshold, it is necessary to switch to the UPS's internal battery.

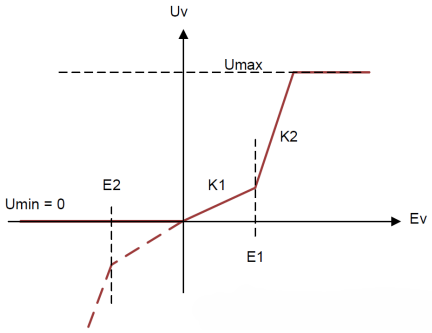


Figure 5.11: Non-linear parametric structure exploitable within a PI with variable gain.

temporarily satisfied as the system seems to work without any problems: the controls developed allow optimal operation at high loads, introducing slight distortion at lower loads.

Before changing topic, moving on to the analysis of a different type of controller, it is interesting to observe the performance generated by a current PI slightly different from the one just presented, which has been tested but never mentioned so far. During the various tests conducted, various combinations of modulators and comparison blocks were actually tested, with regard to the current PI; a solution that provided good results was obtained by exploiting the same structure presented so far, with two major modifications:

- The comparison block of current has two absolute values, performing the comparison between $|i_L^*|$ and $|i_{fb}|$ rather than between i_L^* and i_{fb};
- There is no necessity to introduce a feed-forward signal.

This type of modification makes the use of the PI more appropriate, as the current reference to be tracked would become a pulsating signal rather than a sine wave, presenting a mean value different from 0 $[V]$ which the PI itself can track with zero error. This leaves the remaining pulsating component, with a zero mean value, which the PI could track more easily with respect to what has been presented so far, as the actual signal to be tracked will have a smaller amplitude than ours.
This solution introduces pros and cons compared to the previous case:

- Better tracking of the average current value at low loads: the average current signal has less distortion compared to the case under consideration;

- The modulating signal must track a pulsating reference, ideally responding at certain instants with cusps, which represent points of non-derivability; the control will certainly not be able to generate them easily, distorting significantly at the crossing point;

- The non-linearity of the response seems to affect the machine centre voltage, which rises noticeably to peaks of $\sim 60\ [V]$, in contrast to the $\sim 20\ [V]$ reported in the previous case;

- In DCM operation, the shape held by the modulating signal appears to be totally different from the classical rectified sine wave: this makes it difficult to add a pre-calculated feed-forward signal.

Figure 5.12 shows some of the waveforms generated by the simulation in which the modifications just presented were made, carried out under the same conditions and working points as the previous one: the first box shows the machine centre voltage produced, while the second shows the perfect tracking present between one of the three current reference signals (in green) and the sampled average of the same (in red).

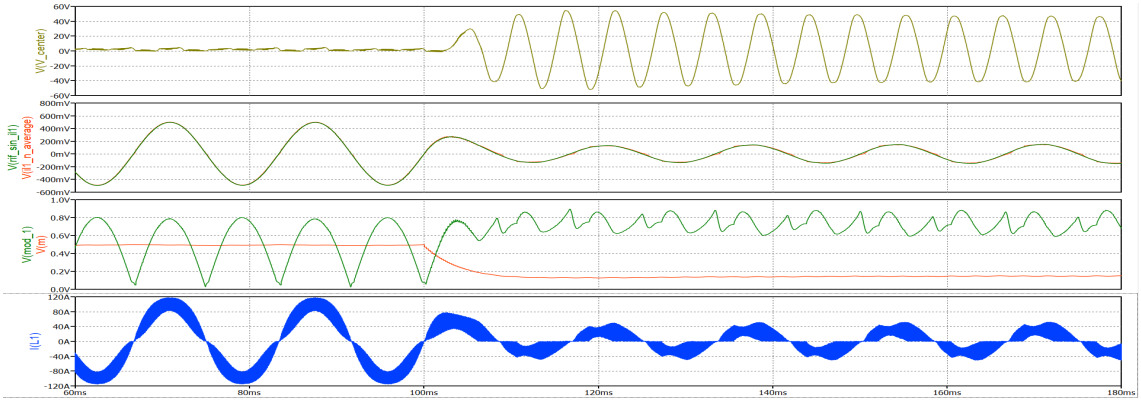


Figure 5.12: Main waveforms generated during a test simulation of the complete three-phase system, carried out with three PI controllers with slightly modified comparison blocks, compared to those presented above.

The third box shows the modulating signal produced by the previous PI of current (in green) and the output of the PI of voltage (in red), while the last box shows the actual inductor current.
The fact that a variety of not indifferent problems have been encountered, in exchange for a slightly better tracking of the average current reference, leads to the conclusion that the use of a different controller could result in a better trade-off between the various required specifications; the fact that the centre voltage

moves uncontrollably, despite the fact that there is no active overmodulation technique, means nothing good.
It should in fact be emphasised that working with a linear modulating signal with no non-derivability points leads to fewer problems in terms of managing the machine centre voltage, which is why this type of solution has been temporarily shelved.

5.2.2 PR CONTROL: ANALYSIS AND CONSIDERATIONS

Analysing the PI controller presented in the previous section, it was shown how it is not possible to obtain, using a sinusoidal reference, a tracking by the system with zero error at steady state.
We can then ask what would happen if we tried to translate the PI transfer function in frequency, clearly placing it on both frequency f_o and frequency $-f_o$, since the required t.f. must clearly exhibit Hermitian symmetry. We then calculate the two contributions separately:

$$G_{PI}(s - s_o) = K'_P + \frac{K'_i}{s + s_o}$$

$$G_{PI}(s + s_o) = K'_P + \frac{K'_i}{s - s_o}$$

Let us now put the two contributions together, thus obtaining the desired generic expression:

$$G_{\text{shifted PI}}(s) = G_{PI}(s - s_o) + G_{PI}(s + s_o) = 2K'_P + 2K'_i \cdot \frac{s}{s^2 - s_o^2}$$

By now considering $s_o = j\omega_o$ and assigning two different names to the variables obtained, we derive the final expression of a new type of controller, which has the usual proportional part and a new contribution that we will call *resonant*:

$$G_{PR}(s) = K_p + K_r \cdot \frac{s}{s^2 + \omega_o^2} \tag{5.10}$$

The previous equation can be rewritten in classical Bode form as:

$$G_{PR}(s) = K_p \cdot \frac{\left(1 + \frac{K_r}{K_p \omega_o^2} s + \frac{s^2}{\omega_o^2}\right)}{\left(1 + \frac{s^2}{\omega_o^2}\right)} \iff G(s) = K_{gain} \cdot \frac{\left(1 + \frac{2 \cdot \xi_N}{\omega_o} s + \frac{s^2}{\omega_o^2}\right)}{\left(1 + \frac{2 \cdot \xi_D}{\omega_o} s + \frac{s^2}{\omega_o^2}\right)}$$

where clearly $\xi_D = 0$ e $\xi_N = \frac{K_r}{2 \cdot K_p \cdot \omega_o}$.
It is now easy to draw the Bode diagram of the previous transfer function: Figure 5.13 shows several graphs obtained by exploiting different constants K_p and K_r. Clearly, the fact that $\xi_D = 0$ imposes an infinite gain on the frequency f_o, leaving at the numerator the task of smoothing the narrow band placed in f_o. The t.f.

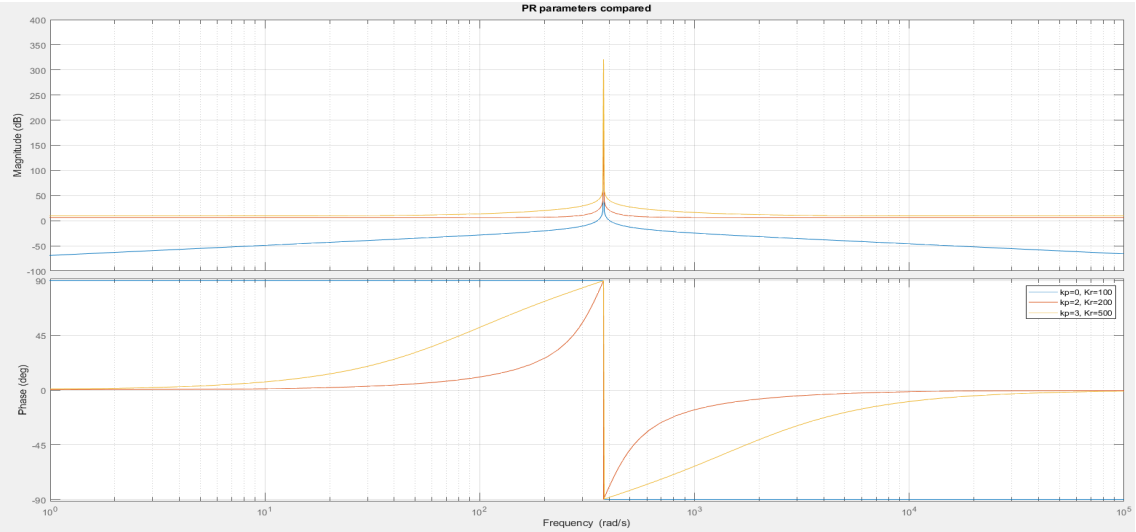


Figure 5.13: Bode diagram of the PR controller, as a function of the values of the constants K_p and K_r.

just obtained shows two excellent properties:

1. It imposes infinite gain at frequency f_o, thus being able to track a sinusoidal input with zero error when used as a controller;

2. The fact of using a proportional contribution, together with the resonant one, makes the presence of the latter component completely independent with respect to the stability of the system: in the absence of a proportional component, a loss of 90° is generated for $f >> f_o$, while adding a generic K_p produces a zero and a pole, both complex conjugates, which elide their contributions at high frequencies, thus generating a phase shift of 0° at higher frequencies.

It is possible to prove mathematically that this type of controller is able to track with zero error any sinusoidal input having frequency f_o, making it the equivalent of a PI controller for frequencies different from 0 $[Hz]$. In fact, by placing $\omega_o = 0$ $[rad/s]$ within the equation 5.10, we obtain the exact expression of the classic PI controller.
We start by observing that a generic input sine wave can be represented, using the Unilateral Laplace transform, as:

$$X(s) = L_u\left[A \cdot \sin(\omega_o t)\right] = A \cdot \frac{\omega_o^2}{s^2 + \omega_o^2}$$

Assuming then that a PR controller is used within a generic system with a unitary feedback, the following relationship can be obtained by exploiting the

Final Value theorem:

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} s \cdot E(s) = \lim_{s\to 0} s \cdot A \cdot \frac{\omega_o^2}{s^2+\omega_o^2} \cdot \frac{L_D(s)}{L_D(s)+L_N(s)}$$

where clearly $E(s) = X(s) \cdot \frac{1}{1+L(s)}$ ed $L(s) = \frac{L_N(s)}{L_D(s)}$.

The above expression imposes $\lim_{t\to\infty} e(t) = 0$ if and only if the following conditions are satisfied:

$$\begin{cases} L_D(s) = s^2 + \omega_o^2 \iff \text{ensured by the presence of the PR} \\ L_D(s) + L_N(s) \neq s \iff \text{true if } \omega \neq 0\ [rad/s] \end{cases}$$

The controller we have just derived, although appearing at first sight to be perfect for our purposes, suffers a serious problem when applied in a real context: the infinite gain, imposed at a given frequency, decreases infinitely by moving infinitesimally away from the set frequency; this generates two enormous problems:

1. If the network frequency could vary by an infinitesimal df $[Hz]$, the performance generated by the control would be dramatically reduced;

2. Discretizing such a precise model would introduce discretization errors that would cause, among other things, variations of the actual position of f_o.

An interesting compromise is then found by introducing a damping factor $\xi_D \neq 0$ within the denominator, which allows the bandwidth of the spike to be extended, thus increasing the gain in the vicinity of the frequency f_o and greatly reducing the influence of possible discretabilisation errors.
Knowing that, for a second-order resonant system, it is possible to define $\xi = \frac{1}{2\cdot Q}$, where Q represents the Quality Factor of the resonator itself, it is also possible to define $\omega_{-3dB} = \frac{\omega_o}{Q}$ $[rad/s]$ where ω_{-3dB} represents the normalised bandwidth of the resonator at $-3dB$. It then becomes convenient to rewrite the equation 5.10 in the form:

$$G_{PR}(s) = K_p + K_r \cdot \frac{2 \cdot \omega_c \cdot s}{s^2 + 2 \cdot \omega_c \cdot s + \omega_o^2} \tag{5.11}$$

where $\omega_c = \frac{\omega_{-3dB}}{2}$ $[rad/s]$ represents the half-bandwidth at $-3dB$.
This form is useful as it allows an easier relationship with the parameters of the

resonator itself, as it is possible to write:

$$\frac{\omega_c}{\omega_o} = \xi = \frac{1}{2 \cdot Q} \iff 2 \cdot \omega_c = \frac{\omega_o}{Q} = \omega_{-3dB}$$

The term present in the numerator is clearly introduced to normalise the expression; in fact, it is possible to rewrite the contribution of the resonant part as:

$$G_R(s) = K_r \cdot \frac{2 \cdot \frac{\omega_c}{\omega_o^2} \cdot s}{1 + 2 \cdot \frac{\omega_c}{\omega_o^2} \cdot s + \frac{s^2}{\omega_o^2}} = K_r \cdot \frac{\frac{s}{2 \cdot Q}}{1 + \frac{s}{2 \cdot Q} + \frac{s^2}{\omega_o^2}}$$

and so, calculating the magnitude of $G_R(s)$ at the point $s = j\omega_o$ we obtain:

$$|G_R(j\omega_o)| = K_r$$

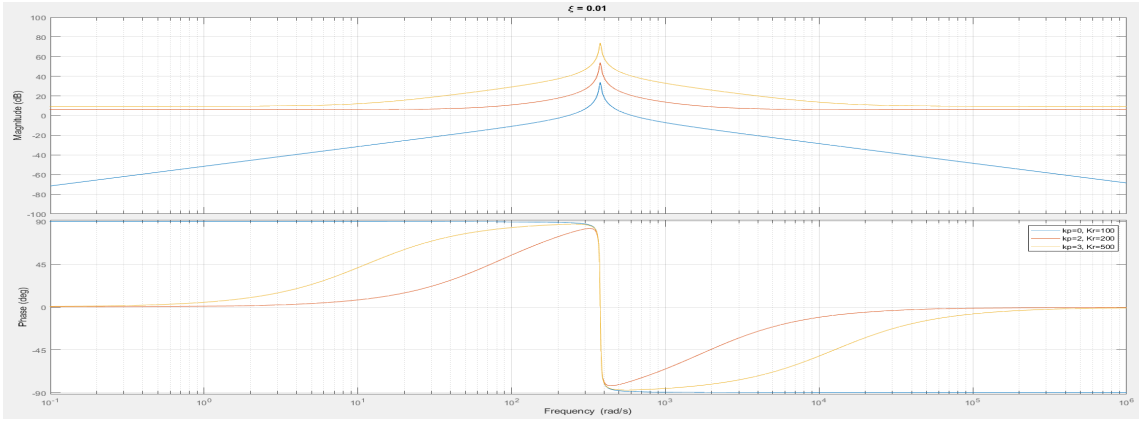
We have now normalised the entire resonator equation, obtaining three different variables to define while designing a PR controller:

- K_p : proportional contribution, on which the stability of the system depends;
- K_r : resonant contribution, which defines the maximum height reached by the narrow-band peak in $f = f_o$;
- w_c : normalized half-bandwidth at -3_{dB}.

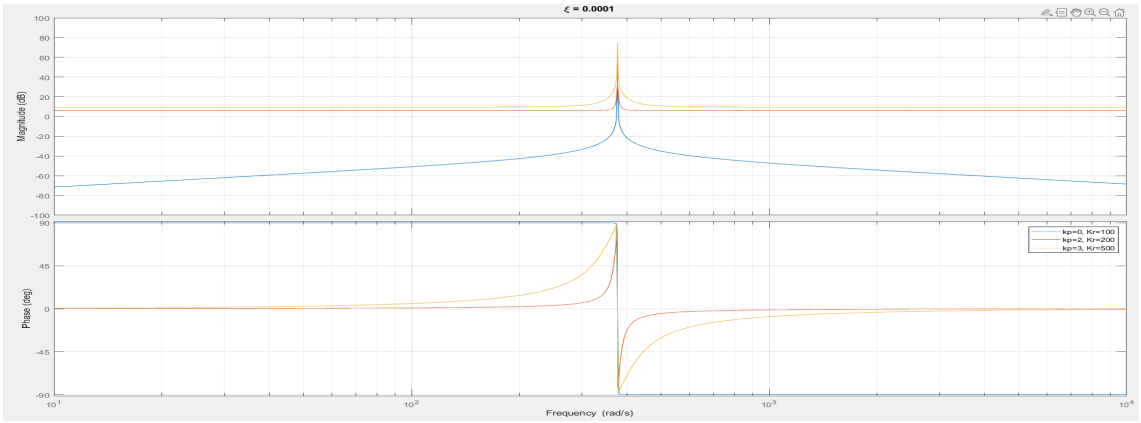
The introduction of the damping factor clearly invalidates the condition $L_D(s) = s^2 + \omega_o^2$ derived earlier, thus producing a minimum of error at steady state; however, compared to a simple PI, we can obtain two enormous advantages:

1. The steady-state error can be considered practically zero if we set the peak centred in f_o at a very high value; the possibility of acting directly on its height therefore makes the error introduced easily manageable. Increasing the parameter K_r thus reduces the steady-state error more and more, without the risk of altering the stability of the system;
2. The stability of the system depends practically only by K_p if the controller is well designed, which avoids to introduce phase delay within the system, except at frequencies close to f_o: thus, if the open-loop cut-off frequency turns out to be $f_{cut} >> f_o$, the presence of the resonant controller will not alter the phase margin of the system.

We can then observe how the Bode diagram of the PR controller changes as its three parameters change; Fig. 5.14 (a) shows some shapes obtained by setting $\xi_D = 0.01 \iff \omega_c \simeq 3.77\ [rad/s]$, while Fig. 5.14 (b) uses the same parameters except ξ_D, which is set $\xi_D = 0.0001 \iff \omega_c \simeq 0.0377\ [rad/s]$.



(a)



(b)

Figure 5.14: PR with dumping factor: various tests carried out with $\omega_c \simeq 3.77\ [rad/s]$ (a) and $\omega_c \simeq 0.0377\ [rad/s]$ (b).

At this point, it is possible to discretize the controller we have just created, in order to test it on the simulation system; since we have to work with an apparently sensitive controller it is advisable to use a sufficiently precise discretisation technique, in order to not introduce excessive discretisation errors which could modify the shape of the narrow-band used in frequency.

We then use Tustin's appossimation rather than Euler's, obtaining:

$$\begin{cases} U(z) = U_p(z) + U_r(z) \\ U_p(z) = K_P \cdot E(z) \\ \\ U_r(z) = \frac{a_o \cdot (1 - z^{-2})}{b_o + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}} \cdot E(z) \quad \text{where} \begin{cases} a_o = 4 \cdot K_r \cdot T_s \cdot \omega_c \\ b_o = T_s^2 \cdot \omega_o^2 + 4 \cdot T_s \cdot \omega_c + 4 \\ b_1 = 2 \cdot T_s^2 \cdot \omega_o^2 - 8 \\ b_2 = T_s^2 \cdot \omega_o^2 - 4 \cdot T_s \cdot \omega_c + 4 \end{cases} \end{cases}$$

By antitransforming, we then obtain the required system of difference equations:

$$\begin{cases} u(k) = K_p \cdot e(k) + u_r(k) \\ u_r(k) = \{a_o \cdot \big[e(k) - e(k-2)\big] - \big[b_1 \cdot u_r(k-1) + b_2 \cdot u_r(k-2)\big]\} \cdot \frac{1}{b_o} \end{cases} \tag{5.12}$$

It is now possible to do some tests on the simulation program, initially using the single-phase model to make some calibration tests; theoretically, by using a sufficiently narrow ω_c it is possible to stabilise the loop by acting only on K_p.
Figure 5.15 shows the result of steady state operation obtained via the single-phase model, in which a load change is also carried out.
The controller used seems to offer very high performance without even the use of the feed-forward signal: in the first box we can see the superposition of the sinusoidal reference signal (in red) with the average sampled current (in green). In the second box we can see the inductor current (in blue) and the current feeding the output load (in red), shown in order to make visible the exact moment when the load change takes place.

From the first tests it becomes clear how this type of controller can offer sensational performance in steady state operation, even outperforming a PI control with an accompanying feed-forward signal; testing its behaviour during the most critical transients, such as start-up and shutdown, instead, reveals the true sensitivity of the PR control. Fig. 5.16 shows in fact a series of transients realised ad hoc, in order to study the performance of the controller during dynamic control operations: the image shows in the first quadrant the modulating signal produced by the PR control (in red) and the component generated by the

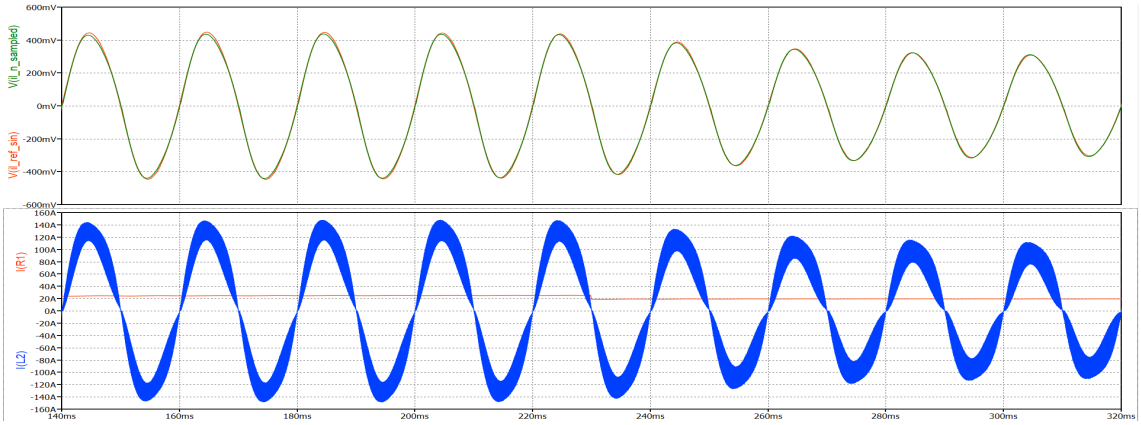


Figure 5.15: Steady state performance generated by a PR current controller, used in the single-phase model; the calibration was carried out with $K_p = 1$, $K_r = 500$, $\omega_c = 0.1$.

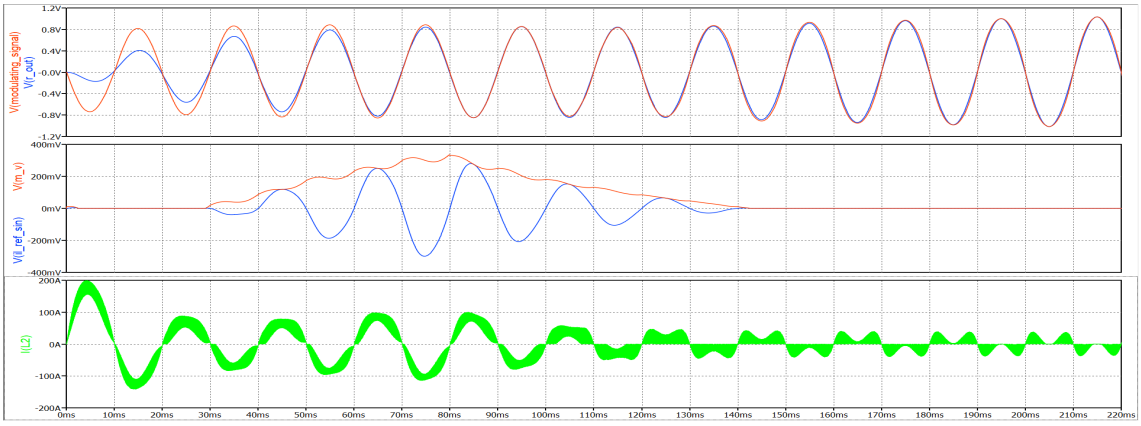


Figure 5.16: Performance generated during transients using a PR current controller, used in the single-phase model; the calibration was carried out with $K_p = 1$, $K_r = 500$, $\omega_c = 0.1$.

resonant contribution alone (in blue); in the second quadrant is visible the reference generated by the voltage controller (in red) which generates the sinusoidal current reference (in blue), while the last quadrant shows the trend of the real inductor current.

It is therefore possible to make the following observations:

1. During the first operating cycles the inductor current reaches enormous peaks, despite the current reference is zero. The explanation for this comes from the first quadrant, in which it can be seen that the resonant contribution takes a few network cycles before it reaches the steady state: the first operating cycles are then managed by the proportional contribution alone;

2. The resonant contribution, after reaching steady state, seems to act correctly even during the switch-off transient;

3. When the current reference returns to zero, the inductor current continues to circulate for a few more cycles, gradually becoming more and more damped.

Clearly, the choice of controller parameters affects its dynamic performance; after a series of various analyses, we can make the following conclusions:

1. The narrower the half-band ω_c is, the more the controller will tend to respond with a purely sinusoidal modulant: narrowing the bandwidth, in fact, limits the range of frequencies to which the controller can respond, generating less distortion at steady state, but presenting many problems during transients, since it is forced to respond with purely sinusoidal modulants, when it would be useful to exploit a whole spectrum of frequencies. The narrow bandwidth causes the harmonics produced during the transient to be almost all filtered out, unlike those around the f_o frequency, which prevents the controller from functioning correctly;

2. The wider the half-band ω_c, the less time the controller takes to stop; in this respect, an analogy can be made between the resonant control and an RLC network, since both have a t.f. of the same kind. In fact, we can say that the higher the resistance R, the wider the band of the resonator, settling more quickly the oscillations generated by a step input; in the same way, the half-band width defined by ω_c affects the time required by the controller to settle its contribution;

3. The higher the K_r value, the more aggressive the control is: in the case of significant load changes, the controller will tend to reduce the generated error as soon as possible, thus causing higher distortions during transients. In even more critical cases, a too high K_r and a too narrow ω_c make the controller so aggressive that it loses entire network cycles during start-up, before settling down correctly.

A correct controller calibration then becomes seemingly impossible to achieve if optimum performance is to be achieved in any context: the choice of parameters is a function of a continuous trade-off between lower distortion and greater controllability of transient dynamics, between lower steady-state error and lower operating safety at critical control points.
In the previous chapter, the use of feed-forward and intelligent memory management was added to the current PI; even with the PR controller it is then possible to use special techniques outside of it, in order to properly manage the overall set of issues related to its dynamic performance.
By appropriately exploiting feed-forward signals, implementing dynamic parameter management together with intelligent management of the relevant

memories, it is then possible to achieve an overall better performance of the controller under consideration, as can be observed in Fig. 5.17.

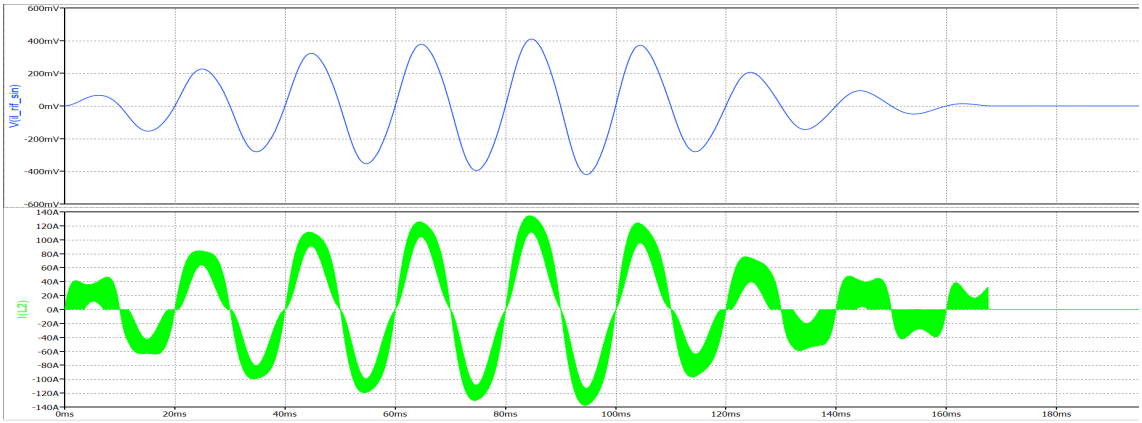


Figure 5.17: Dynamic performance offered by a current PR controller correctly implemented, in a single-phase Vienna network.

It is interesting to observe the starting instant: as soon as the output voltage V_{out} falls below a limit value, the non-linear voltage PI increases the gain offered, generating a higher current reference, so as to reach the target operating voltage more quickly. The same dynamics can be seen during the load-switching instant, in which the voltage PI drastically lowers the generated current reference, so as to prevent the output voltage from rising above the preset operating point. The performance offered by the current control appears to be excellent, being practically comparable with the performance offered by the PI controller with the addition of the feed-forward.
The machine centre voltage shows a very similar trend to that obtained with the previous controller, showing in this case a slightly lower maximum peak than that obtained in the previous case: this clearly depends on the parameters used by the PR controller, specially chosen to obtain an excellent compromise between good operation and performance at steady state.

It is then possible to implement this type of controller on the three-phase simulation model. Fig. 5.18 shows the results obtained: the first quadrant shows the machine centre voltage, while the second shows the output voltage V_{out}; the third quadrant shows the current reference, used by the first inductor current (in red), generated by the output of the voltage controller (in blue), while the last quadrant shows the trend of the three current phases.

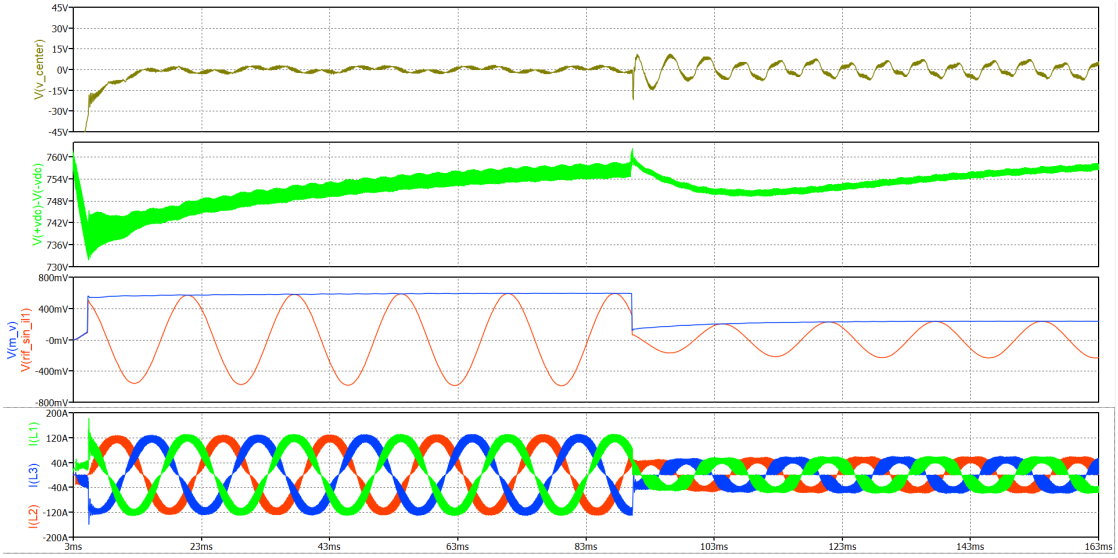


Figure 5.18: Dynamic performance obtained by using three PR current controllers, within the three-phase Vienna Rectifier network. Same test conditions used for the previous three-phase simulation; load change conditions: 10 [Ω] → 25 [Ω].

5.2.3 PIR CONTROL: ANALYSIS AND CONSIDERATIONS

In the two previous sections, two different types of controllers were analyzed, each with strengths and weaknesses:

- The PI control: presenting an enormously wider bandwidth than that offered by a PR controller, it does not present any dynamic problems during transients. However, it does introduce a phase delay, which can only be corrected by the use of a feed-forward signal and intelligent memory management;

- PR control: presenting a very narrow band, it responds naturally by means of almost sinusoidal signals, greatly reducing the distortion produced, but showing quite a few problems during transients; it becomes controllable only through the use of certain specially designed techniques.

At first view, the two controllers seem to possess such opposing qualities that they compensate for each other. It is then legitimate to wonder whether the union of the two can generate an equivalent control, with optimal performance in all the cases analysed, which also does not require complex techniques to manage it: thus, the PIR controller is born.
This type of controller exploits a resonant component capable of tracking the first current harmonic producing very little distortion, while exploiting an integral component in order to track the harmonics produced during transients: the two contributions can thus handle different instants of operation, without unnecessarily burdening the control code, which would force the operation of a single contribution in all cases through complex techniques. We can then define a generic PIR controller by means of the following transfer function:

$$G_{PIR}(s) = K_p + \frac{K_i}{s} + K_r \cdot \frac{2 \cdot \omega_c \cdot s}{s^2 + 2 \cdot \omega_c \cdot s + \omega_o^2} \tag{5.13}$$

with which it is possible, as usual, to draw the corresponding Bode diagram as a function of the values K_p, K_i, k_r and ω_c shown in Figure 5.19; it is possible to make a few observations in this respect:

- The graph in red exploits the integral and proportional part in order to increase gain at frequencies $f < f_o$: the resonant part will follow the reference relative to the fundamental current harmonic, exploiting instead the integral contribution to handle the most critical transients such as start-up. At steady state, the integral contribution will tend to cancel out, thus avoiding the use of any feed-forward signal;

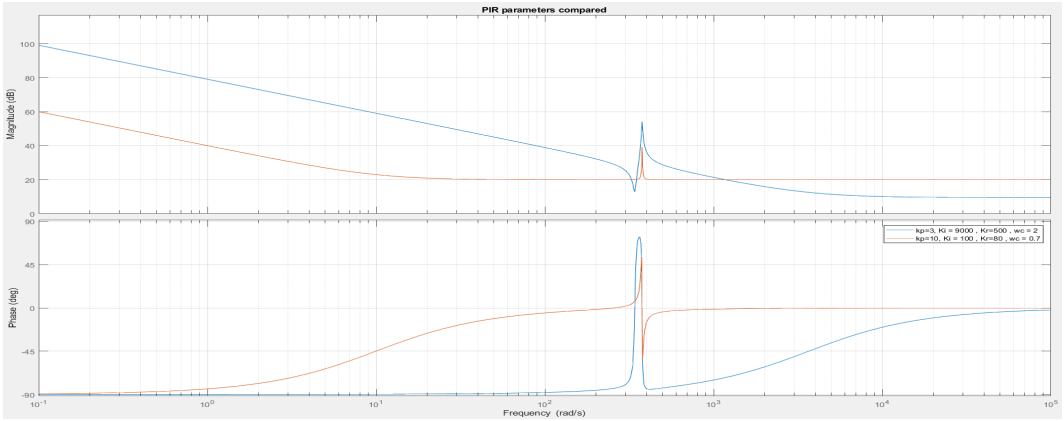


Figure 5.19: Bode diagram of some t.f. relative to PIR controls, as a function of their parameter values; note how the use of such a high K_i is not so absurd, since the respective digital constant turns out to be $K_i' = K_i * T_s < 1$.

- The graph in blue, instead, exploits the integral and proportional part to increase the loop gain for frequencies even higher than f_o: this technique can be used in order to track, although with less precision, harmonics at frequencies higher than f_o, while the resonant contribution will perfectly track the fundamental current harmonic.
  In the case of tracking harmonics other than the first, the use of a feed-forward signal is recommended as the task will be performed exclusively by the PI part.
- It is also interesting to observe how the integral part, used in the blue graph, is so high as to generate a complex conjugate zero with a frequency no longer approximated to $f \sim f_o$. Around the latter, two peaks are in fact generated, one positive and one negative, breaking down the phase variation introduced into a $+180°$ peak and a $-180°$ peak, unlike the graph in red.

Clearly the resonant component will only track the fundamental harmonic component, completely cancelling out the steady-state error if K_r is high enough. This means that, regardless of how high the value K_i is, the integrator will naturally tend to damp itself at steady state if there are no further harmonics to chase; this then emphasises the fact that, in addition to gaining a better transient with respect to the use of the PR alone, the steady state performance will be the same as that obtained with the single PR.
The advantage we have obtained comes not only from the possibility of tracking the fundamental harmonic with perfect precision, correctly managing the various transients, but also from the possibility of tracking even higher harmonics by means of the integral contribution, in case the latter should be high enough. This solution will be applied in order to study the behaviour of the system when

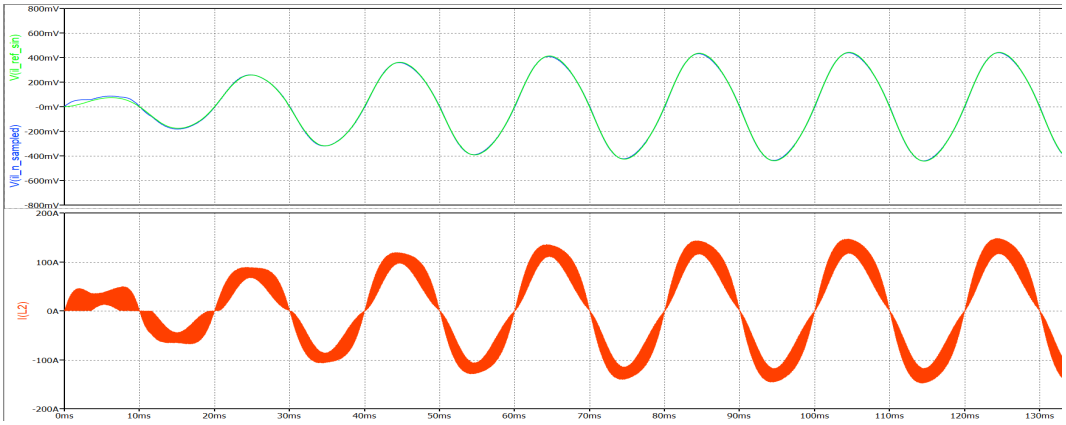


Figure 5.20: Dynamic performance provided by a current PIR controller: simulation model of the single-phase Vienna Rectifier.

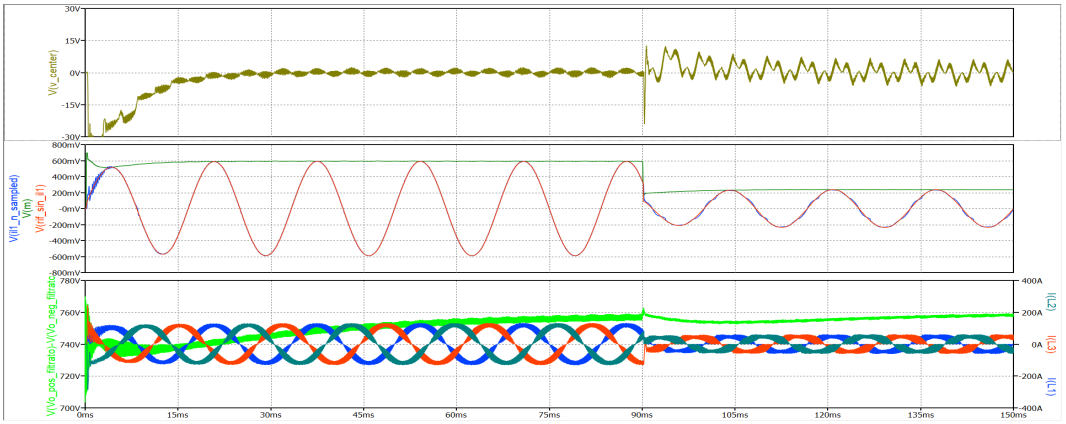


Figure 5.21: Dynamic performance obtained using three current PIR controllers within the three-phase network of the Vienna Rectifier. Same test conditions used for the previous three-phase simulation; load change conditions: 10 [Ω] → 25 [Ω].

it is subjected to a distorted power supply network, thus being able to track multiple harmonics, and also reducing the use of processor resources with respect to the implementation of more complex solutions, such as the use of multiple resonators at different frequencies.

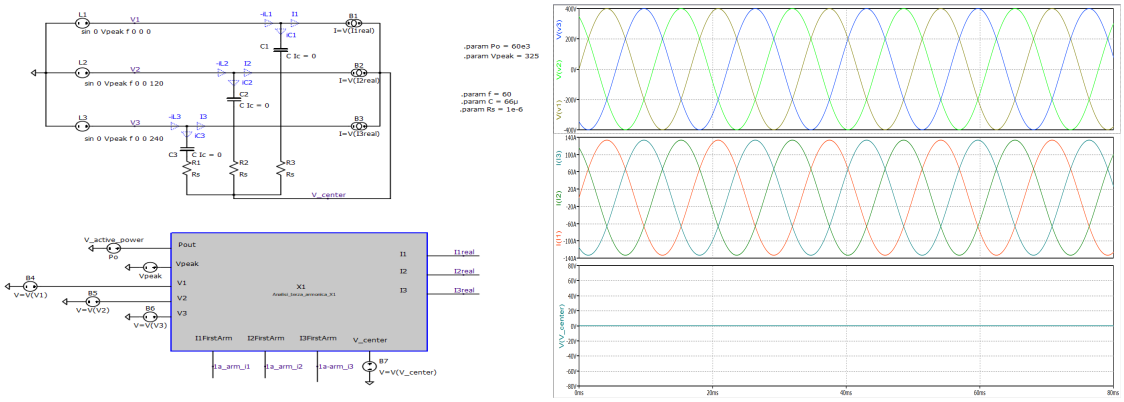
Doing the usual tests with the single-phase and three-phase model, we obtain performance that is practically comparable with the previous ones: as just mentioned, we will benefit later about the performance generated by this type of control.

The relative images are shown in Fig. 5.20 and Fig. 5.21: the first shows the inductor current (in red) and the corresponding current reference (in green)

superimposed on the sampled average (in blue); the second shows the machine centre voltage (in yellow), the reference of the first inductor current (in red) superimposed on the respective sampled current (in blue) and the output of the voltage controller (in green). The last quadrant shows the three inductor currents and the output voltage V_{out}; the non-linear voltage PI is also active here.

5.3 Influence of control on center bank voltage: introduction to the simplified model

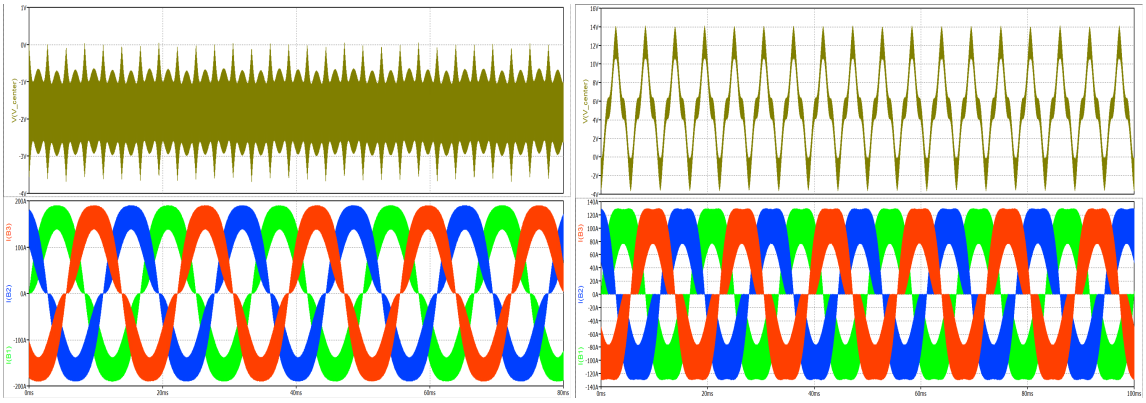
Regardless of the type of control used in the three-phase model it was observed that, from the first tests with the PI of current, the machine centre voltage tends to move with amplitude apparently depending on the load, clearly in contradiction with what was shown by the equation 4.5.
In order to analyse the problem, a simpler simulation model should be realised, as there are too many parameters and controls to be taken into account in the complete simulation. It is then possible to realise the simulation model shown in Figure 5.22(a): the latter represents the essence of the Vienna rectifier, comprising the line voltage generators, the three input capacitors and three current generators driven by the digital system, which can simulate the behaviour of the inductor currents; the latter are connected to the input capacitors via a machine centre connection.



(a) (b)

Figure 5.22: Simplified three-phase Vienna Rectifier simulation (a); test on average operation in the absence of overmodulation (b).

This type of simplified model makes it possible to eliminate any type of control, PWM operation and bank balancer: it is in fact possible to use the simulated digital controller in order to generate, in open loop, the required currents, as a function of a certain pre-set output power. Using the formulas obtained in Chapter 4 it becomes simple to construct the digital block, greatly simplifying the analysis of the problem.
It is then possible to make the first tests assuming to let some currents circulate



(a) (b)

Figure 5.23: Simulation model simplified: addition of a ripple superimposed on the inductor currents. Full load operation (a) and at 50 $[kW]$ (b).

in the three simulated coils, represented only by their average value; by setting a certain output power, it is then possible to exploit the equation 4.3, obtaining the behaviour shown in Figure 5.22(b). The image shows the three input voltages in the first quadrant, while the second shows the three simulated currents, represented only by their average value; the last quadrant shows instead the machine centre voltage. The latter appears to be, in this case, of constant value, in accordance with the equation 4.5, confirming that there is nothing abnormal in the theory developed.
Having provided currents with a null sum, instant by instant, it is obvious that the centre bank cannot move: whatever made it move in the complete simulation certainly represented a parasitic element, which for some reason imposed the sum $i_{L1}(t) + i_{L2}(t) + i_{L3}(t)$ $[A]$ no longer null at each instant, thus causing a current component to circulate on the input capacitors, generating a certain movement of the machine centre voltage.
It is then convenient to add non-ideal elements that would normally be introduced by the control, in order to obtain the same behaviour expected: for example, it is possible to add a superimposed ripple to each average current, making it as similar as possible to that generated in the complete simulation. Exploiting the equation 4.9, imposing a current direction concordant and limited to that of the voltage, and assuming the use of an ideal duty-cycle, we obtain the results shown in Figure 5.23.
What we obtain is the proof we were looking for. Figure 5.23 (a) shows the three simulated inductor currents together with the machine centre voltage, this time

no longer constant, generated assuming a full load operation; as there is no bank regulator, the latter holds non-zero averages, also showing some movement with an amplitude of a few volts as observed in the complete model.
Figure 5.23 (b) shows, instead, what happens when we impose an output power equal to 50 $[kW]$, generating an amplitude of oscillation of the machine centre voltage equal to ~ 9 $[V]$.
The explanation becomes thus clear: in full-load operation, the three inductor currents are practically always operating in CCM, making the equation $i_{L1}(t) + i_{L2}(t) + i_{L3}(t) = 0$ $[A]$ always true. Lowering the load instead causes the three currents to operate in both CCM and DCM: although the three average current components result in a zero sum, this is not true for the ripple components superimposed on the latter; the component that remains excluded from the sum, having to somehow circulate, tends to flow in the input capacitors, generating the centre-machine oscillation.
It is then possible to decompose the ripple, superimposed on each inductor current, as the sum of a differential ripple component and a common component, considered with the same convention as the signs of the inductor currents, defined as follows:

$$i_{Lj}(t) = i_{\text{Lj average}} + i_{\text{ripple diff j}}(t) + \frac{1}{3} \cdot i_{\text{ripple com}}(t) \ [A]$$

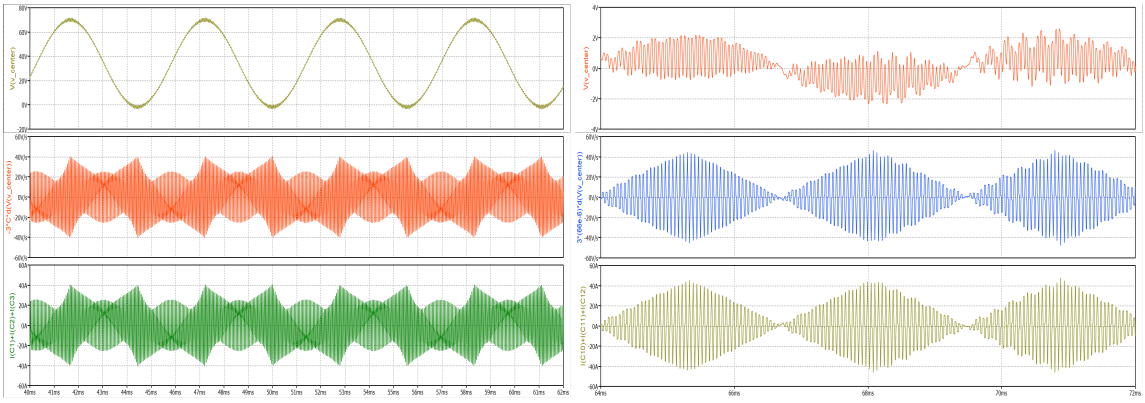
in this way, by adding the three inductor currents we obtain:

$$\sum_{j=1}^{3} i_{Lj}(t) = \sum_{j=1}^{3} i_{\text{Lj average}} + \sum_{j=1}^{3} i_{\text{ripple diff j}}(t) + \frac{1}{3} \sum_{j=1}^{3} i_{\text{ripple com}}(t) = i_{\text{ripple com}}(t) \ [A]$$

where clearly both the average and differential ripple components cancel out as their sum is null; the $i_{\text{ripple com}}(t)$ component, instead, turns out to be the cause of the centre bank movement, mathematically defined by the equation 4.6 previously derived, thus asserting that in the absence of the third harmonic of current it holds:

$$i_{\text{ripple com}}(t) = i_{center}(t) = 3 \cdot C_{in} \cdot \frac{d}{dt} V_{center}(t) \ [A]$$

Clearly, the common ripple component is the same for all three phases and follows the same planned path for the third harmonic; in contrast, the differential ripple component would come from the grid, along with the average first



(a) (b)

Figure 5.24: Machine centre voltage and common-mode ripple component, derived within the simplified model (a) and within the complete three-phase model (b).

harmonic current, if there were no line impedance. Since the latter is present, in fact, only the fundamental current component can come from the network, forcing also the differential component to flow through the capacitors, since the latter is a high-frequency contribution; the latter will clearly not contribute to the movement of the machine centre voltage.
Figure 5.24 (a) makes what has been said obvious: by lowering the simulated load further, it can be seen in the first quadrant how the machine centre voltage has increased even further. Applying the derivative function to the latter and multiplying it by $3 \cdot C_{in}$ $[F]$ we obtain what is shown in the second quadrant; adding now the three currents present in the input capacitors we obtain the current shown in the last quadrant. These last two results represent the same function and are perfectly superimposable, demonstrating the equation just obtained: these last two currents therefore represent the common component of the ripple responsible for the movement of the machine centre voltage, in the absence of the third current harmonic.

It is now possible to perform the same test with the complete three-phase model, obtaining the same results even if a high load is used; these results are shown in Figure 5.24 (b), carried out simulating operation with a load of 10 [Ω]. As can be seen, the machine centre voltage has a non-zero mean value that changes in value each time the envelope of the component $i_{\text{ripple com}}(t)$ concludes and begins a new rhombic pattern. Taking a closer look at the exact instant of transition, it

can be observed that the current $i_{\text{ripple com}}(t)$ maintains the same polarity for an instant, which is enough to vary the mean value of the machine centre voltage, which represents the integral of the current $i_{\text{ripple com}}(t)$ except for multiplicative constants.
Although the inductor currents practically always work in CCM, at the instant they change polarity they enter into DCM operation, generating the phenomenon just depicted. If we try to lower the load we obtain, as seen from the tests carried out on the various controllers, a machine centre voltage with an increased amplitude of oscillation: this is due to the fact that the currents more frequently make the CCM-DCM transition, generating this type of distortion more frequently.
This type of problem turns out to be non-existent for the control itself, as the sampling of the various currents is strategically done in the middle of the T_{on} period, precisely where the contribution of the ripple turns out to be zero. The current control will therefore only have access to the average currents, ignoring the fact that there is a superimposed ripple. By the way, although it may be assumed that in CCM operation this technique allows the actual average current to be sampled, this is not true in DCM, as the inductor current turns out to be zero for a certain period of time, introducing an estimation error in the average current itself.

Therefore, *the estimation error of the average introduced in DCM and the presence of a superimposed ripple completely invisible to the control itself generate this type of problem*. Although there may be elaboration techniques that allow the actual average current to be estimated more accurately during DCM operation, this type of non-ideality can never be completely compensated for, at least by maintaining this type of control system.
This could impose a major limitation on the operation of our machine: at low loads, the third harmonic of current that will be circulated may have to take into account the presence of a parasitic movement of the machine centre voltage, independent of it; on the contrary, during burst mode operation the inductor current assumes such low values that it practically keeps the centre bank fixed.

In order to predict the parasitic trend of the machine centre voltage, it is possible to try to derive an analytical form describing the ripple component of the various phases; it is then possible to define $i_{\text{r j}}(t) = i_{\text{ripple diff j}}(t) + \frac{1}{3} \cdot i_{\text{ripple com}}(t)$

by deriving the following equation:

$$i_{\mathbf{rj}}(t) \simeq \begin{cases} \frac{|v_{\text{in j}}(t)-v_c(t)|\cdot d_i(t)}{2\cdot f_s\cdot L_j}\cdot \text{triang}\big(\omega_s t+\phi_j\big) & \text{if } \left(\frac{\Delta I_{\text{Lj}}}{2}\cdot \text{triang}\big(\omega_s t+\phi_j\big)\right)\cdot \sin\left(\omega_o t+\phi_j\right)>0 \\ 0 & \text{otherwise} \end{cases}$$

where clearly $v_c(t) = v_{center}(t)$ is linked, as is well known, to the common mode ripple component.
Imposing then the sum $\sum_{j=1}^{3} i_{\mathbf{rj}}(t) = i_{\text{ripple com}}(t)$ and writing the latter as a function of $v_{center}(t)$ it is possible to predict the trend of the latter as a function of all the factors just shown.
Clearly, what has been obtained represents a differential equation with non-linear variables defined at intervals, which is practically unsolvable.
However, it is possible to impose the following assumptions:

- Perfectly sinusoidal duty-cycle;
- Exclusive CCM operation: we have eliminated the cause of oscillation;
- Current ripple approximated to a sinusoid.

It then becomes possible to rewrite the previous equation as:

$$3\cdot C_{in}\cdot\frac{d}{dt}v_c(t) \simeq \sum_{j=1}^{3}\frac{|v_{\text{in j}}(t)-v_c(t)|\cdot\left(1-\frac{|v_{\text{in j}}(t)-v_c(t)|}{V_{out}/2}\right)}{2\cdot f_s\cdot L_j}\cdot\sin\left(\omega_s t+\phi_j\right)$$

which, after some simplification, can be solved by an online calculator, showing that the function $v_{center}(t)$ has zero mean value and does not exhibit the typical oscillatory trend observed previously.
This demonstrates analytically what has been said above, also underlining the fact that it is practically impossible to calculate in real-time the waveform assumed by the machine centre voltage in order to predict it, since it is dependent on:

- Shape of the modulating signal; it is therefore a function of the type of control used (PI, PR, PIR etc.) as well as the parameters used (K_p, K_i, K_r etc..);

- Value and type of load to be supplied;
- Presence of a third harmonic current that flows or not;
- Symmetry of the grid voltage and the system itself.

This type of non-ideality will then have to be considered and handled appropriately, although it cannot be predicted in real-time: in the next section we will observe what happens when the contribution generated by an overmodulation control is superimposed on it.

5.4 Control with overmodulation

At this point we are finally ready to analyse the techniques that can be used to realise the required overmodulation control.
We can first make some tests using the simplified simulation model, in order to obtain some images of the expected average operation, regardless of the type of control to be realised.As mentioned earlier, in order to realise the optimal overmodulation control, known as flat-top modulation, it is necessary to generate a sinusoidal machine centre voltage oscillating at three times the grid frequency, having the maximum peak equal to 15.5% of the peak voltage of each phase.
By observing Figure 5.22 it is clear that the three controlled current generators must generate the same homopolar component so that these can circulate independently on the three phases, only summing up at the machine centre point. The sum of these three identical components will produce the current previously called $i_{center}(t)$, which turns out to be directly related to the machine centre voltage by the equation 4.6; we then define:

$$3 \cdot i_{\text{L third arm}}(t) = i_{center}(t)\ [A]$$

Knowing then that the equivalent input voltage of each boost stage, present in the three-phase configuration, is $\Delta v_j(t) = v_{\text{in j}}(t) - v_{center}(t)$ it is possible to calculate the current component that each control must generate in order to realise overmodulation, taking any of the three input phases as a reference. Considering then the first voltage line, which has phase equal to 0 $[rad]$, we can define:

$$\Delta v_{1\text{ optimal}}(t) = V_{1\text{ peak}} \cdot \sin(\omega_o t) - 0.155 \cdot V_{1\text{ peak}} \cdot \sin(3\omega_o t + \pi)\ [V]$$

from which we can write:

$$i_{center}(t) = 3 \cdot C_{in} \cdot \frac{d}{dt} v_{center}(t) \implies i_{\text{L third arm}}(t) = C_{in} \cdot \frac{d}{dt}\left[0.155 \cdot V_{1\text{ peak}} \cdot \sin(3\omega_o t + \pi)\right]$$

from which we obtain:

$$i_{\text{L third arm}}(t) = 3 \cdot \omega_o \cdot C_{in} \cdot 0.155 \cdot V_{1\text{ peak}} \cdot \cos(3\omega_o t + \pi)\ [A]$$

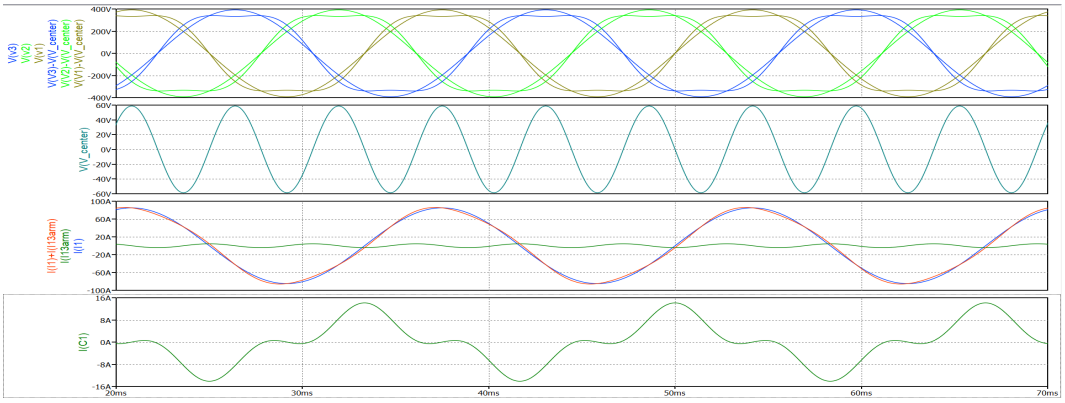


Figure 5.25: Overmodulation effects observable within the simplified simulation model.

from which we obtain, through the relations of the associated angles:

$$i_{\text{L third arm}}(t) = \left(3 \cdot \omega_o \cdot C_{in} \cdot 0.155 \cdot V_{1\,\text{peak}}\right) \cdot \sin\left(3\omega_o t - \frac{\pi}{2}\right) [A] \tag{5.14}$$

We have thus derived the equation for the third harmonic of current that *each* current controller must generate. Adding this latter contribution to all three controlled current generators, shown in Figure 5.22, we observe what is reported in Fig. 5.25: the first box compares the various line voltages with the same voltages measured with respect to the machine centre voltage, where the latter is visible in the box displayed below.
The third box instead compares the average currents circulating in the simulated coil (in red), showing the two current contributions that make up the latter (blue and green); the last box finally shows the average current flowing through the first input capacitor, visibly composed by two different components, respectively of first and third harmonic.
What is illustrated represents the effects of overmodulation, which will be realised in the next sections by means of methods that are progressively more in accordance with the achievement of the project's objectives.

5.4.1 Feed-forward third harmonic injection

One technique that can be used in order to realise overmodulation is to add a certain pre-calculated contribution, relative to the third harmonic current, directly onto the modulating signal generated by each current controller.
This technique is therefore based on an open-loop control of the third harmonic current, independent of the control itself. This gives rise to the name "feed-forward third harmonic injection": the pre-calculated contribution must be injected in the form of a feed-forward, adding it to other contributions already used to control the fundamental current harmonic.
This technique clearly brings with it advantages and disadvantages, which are outlined below.

- Being an open-loop control, it has no dynamics or transients; for the same reason it cannot generate instability problems;
- The control must not be able to track harmonics having a frequency equal to $3 \cdot f_o$ $[Hz]$: the latter would otherwise treat the input as a disturbance, tending to cancel it out;
- For the same reason, the control cannot track any third harmonic components present on the line voltage;
- Unless other techniques are implemented, in the case of a distorted network line, the contribution injected at open loop may be excessive as some harmonic contribution may already be present in the grid.

The facility of handling this solution brings with it, therefore, a major limitation: not intending to exploit a closed-loop control, it becomes impossible to use the PIR controller previously presented in order to track harmonics higher than the first. A good implementation choice would come, for example, from the use of a PR, or a PIR having an integral bandwidth less than f_o, not allowing in conclusion to minimise the reactive power generated in the case of a distorted voltage line. However, it is possible to analyse its performance: this type of solution could be optimal in the case in which one does not want to track harmonics higher than the first.
The implementation is quite simple: wanting to act directly on the modulating signal it is necessary to introduce the signal relative to the voltage modulation we want to realise, rather than relative to the third harmonic current we want to circulate, since the modulating signal itself generates a certain duty-cycle referred to the voltages rather than to the circulating currents.

It is then sufficient to add to the modulating signal the component:

$$\delta'(t) = V_{\text{in peak norm}} \cdot 0.155 \cdot \sin(3\omega_o t) \tag{5.15}$$

clearly in phase with the three line voltages, being a voltage reference. The factor $V_{\text{in peak norm}}$ represents the peak voltage of one of the three voltage lines, all assumed to be identical, normalised[9]. The delay introduced by the control could introduce a phase shift of a few degrees with respect to the required ideal form; it is then sufficient to add into the equation 5.15 a small phase shift within the sine function, in order to obtain an optimal result.
Figure 5.26 shows the result obtained, showing what happens during the usual load change under the usual test conditions; in this case, a current PR controller was used to track the first harmonic of current, so as not to interfere with the injection of the third harmonic. The first quadrant shows the input voltages, measured with respect to the grid centre and with respect to the machine centre voltage; the latter is also visible in the same box.

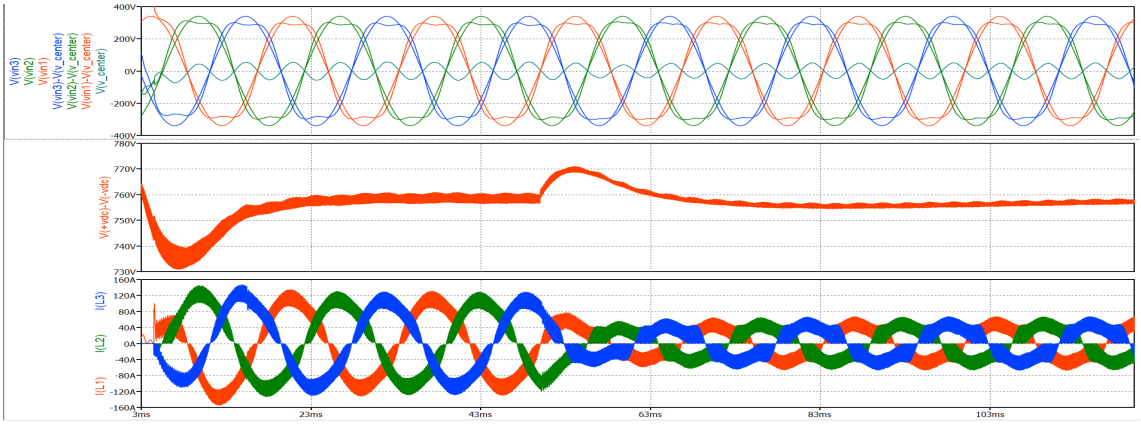


Figure 5.26: Performance obtained by the application of overmodulation, generated by feed-forward signal, using three current PR controllers. Usual test conditions.

In the second quadrant is shown the output voltage V_{out}, while in the third are visible the three inductor currents: these appear slightly distorted by the fact that, superimposed on each of them, there is a third harmonic of current defined by the equation 5.14.

[9]Each sampled quantity has a certain normalisation value since they are usually discretized through an ADC, which works with much lower voltages than those present in the circuit.

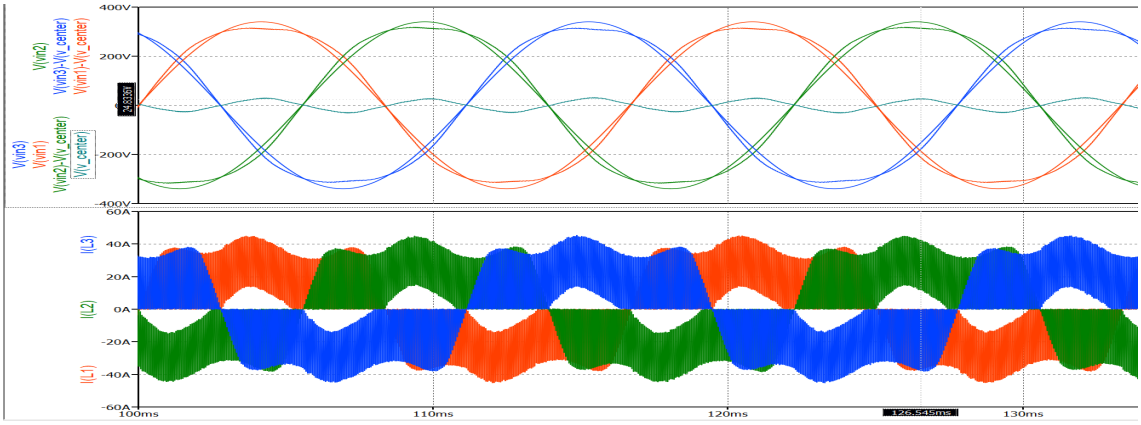


Figure 5.27: Performance obtained by applying overmodulation, under the same conditions described before, at low loads (10 $[kW]$).

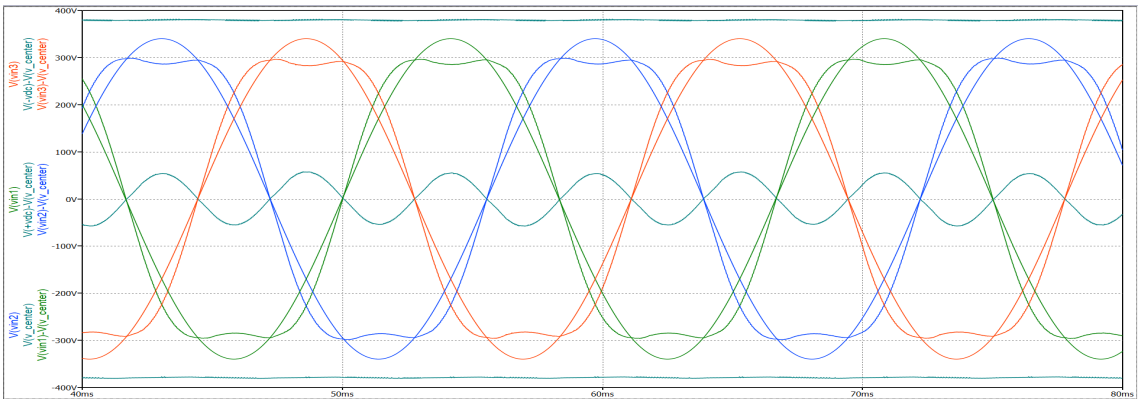


Figure 5.28: Zoom of the main signals present in the overmodulation control; test performed at full load.

As shown previously, the machine's centre voltage tends to move easier at lower loads even if there is no overmodulation applied: the oscillation generated, compared with the overmodulation carried out in Fig. 5.26, turns out to be negligible. In fact, looking at the same image, we can observe slight variations with respect to the behaviour at full load shown on the left-hand side of the image.

In Fig. 5.27 the behaviour at even lower loads is shown, generating in this case an output power equal to 10 $[kW]$: the third harmonic current tends to switch off automatically since there is no possibility for it to circulate, being the inductor current too low. In fact, by observing the cursor positioned on the voltage peak reached by the machine centre voltage, we can notice that it shows a value of

$\simeq 25\ [V]$, unlike the $\simeq 50\ [V]$ reached at steady state[10].
Looking at the line voltages it is clear that, under these conditions, the effect of overmodulation is automatically reduced until it disappears completely in burst mode operation.
Figure 5.28 shows instead a zoom of the full-load operation: here are shown, in cyan, the two voltages $v_{dc}(t)$ and $-v_{dc}(t)$ measured with respect to $v_{center}(t)$, in addition to the three line voltages measured with respect to the usual two reference voltages introduced previously. Thus, the effectiveness of the overmodulation technique used can be appreciated, which allows to extend the operating range of the system by 15.5%.

[10]In order to obtain comparable behaviour with the previous simulations, the usual test conditions were maintained, imposing $V_{\text{in peak}} = 325\ [V]$: the peak reached at full load by the machine centre voltage will then be $V_{\text{center peak}} \simeq 0.155 \cdot V_{\text{in peak}} \simeq 50\ [V]$.

5.4.2 Third harmonic injection into the current reference

A different overmodulation technique can be realised by exploiting feedback, unlike the previous case, in which the third harmonic of current was controlled with an open loop control.
In this case it is necessary to modify the various current references, adding the one relative to the third harmonic to each controller: by then exploiting the equation 5.14, correctly scaled by the full-scale factor used for currents, it is possible to realise the reference relative to overmodulation. Clearly we need a controller capable of tracking harmonics higher than the fundamental: the PIR controller analysed above will then be implemented.
We can then expect that the resonant component follows the fundamental harmonics while introducing as little distortion as possible, while the integral component, adequately supported by an appropriate feed-forward signal, tracks the higher harmonics, such as the one designated to realise the overmodulation technique.
We can then expect the following characteristics:

- Being a closed-loop control, it can present dynamics and transients; for the same reason, instability problems can arise;
- Compared to the previous case, we can expect more distortion as an integral control component is introduced: this will certainly generate delay within the loop, which can be reduced by adding a feed-forward signal;
- By using a current reference, we are able to track additional harmonics present in the network, including contributions at $f = 3 \cdot f_o$ $[Hz]$ unlike in the previous case: this will allow us to increase the power factor of the entire system, while simultaneously reducing the reactive power drawn from the network.

Using a suitably calibrated PIR controller it is then possible to carry out the usual performance test: Fig. 5.29 shows the results provided by conducting the same type of test carried out for the previous control technique.
Two observations can be made immediately with respect to the open loop control technique:

1. The few degrees of phase shift previously introduced in the feedfoward signal, in order to correct possible actuation delays, are not necessary in this case, at least not at full load: the use of feedback made the resulting

signal perfectly symmetrical;

2. In contrast to the previous case, at lower loads there is a slight distortion of the shape of the machine centre voltage signal: it is visible, in fact, that the overmodulation does not show the same performance generated at full load after the load change.

This last observation is easily explained by the fact that the distortion generated by the previous method came only from the operation of the resonant control at low loads. In this case, on the other hand, the latter must be added to the distortion component generated by the integral control during the tracking of the third harmonic reference: the sum of these contributions alters the shape of the machine centre voltage in a no longer negligible manner, generating what is shown in the same figure.

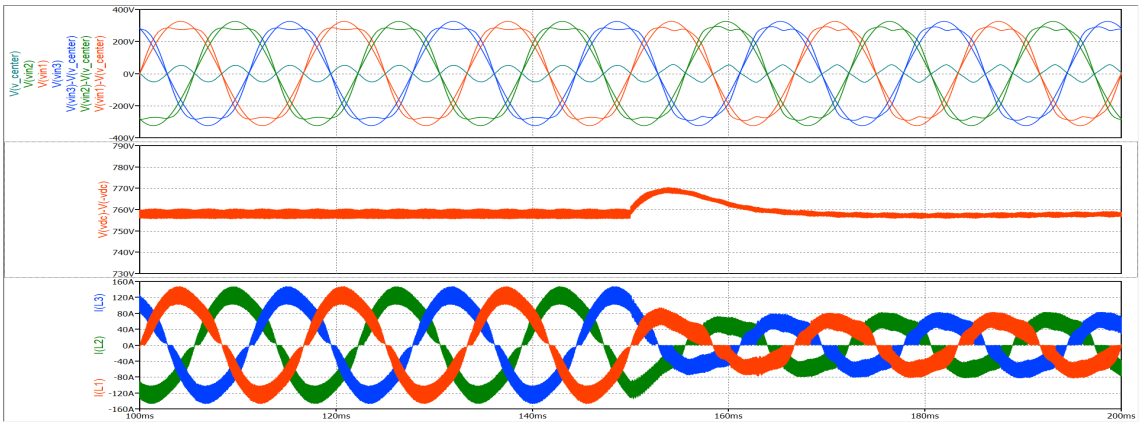


Figure 5.29: Zoom of main quantities generated by overmodulation control; test carried out at full load, then reduced by half (30 $[kW]$).

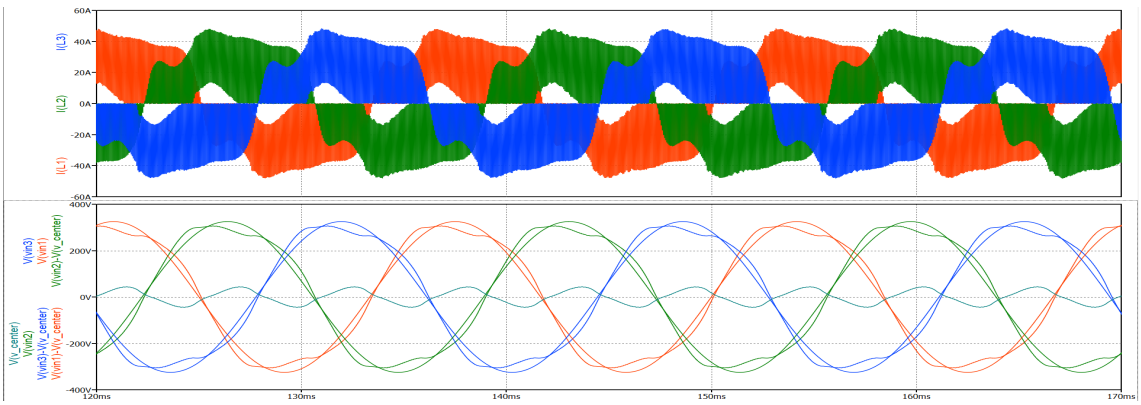


Figure 5.30: Performance obtained from the application of overmodulation, under the same previous conditions, at low loads (10 $[kW]$).

Fig. 5.30 shows instead the machine's behaviour at much lower loads (10 $[kW]$): as in the previous case, distortion increases by reducing the magnitude of the generated currents; reducing the load even more prevents the circulation of the third harmonic, until the effect of overmodulation is completely eliminated.
Fig. 5.31 shows instead a zoom relative to operation at full load: as can be seen, the performance obtained turns out to be excellent, gaining again 15.5% more than the operating range achievable without overmodulation.

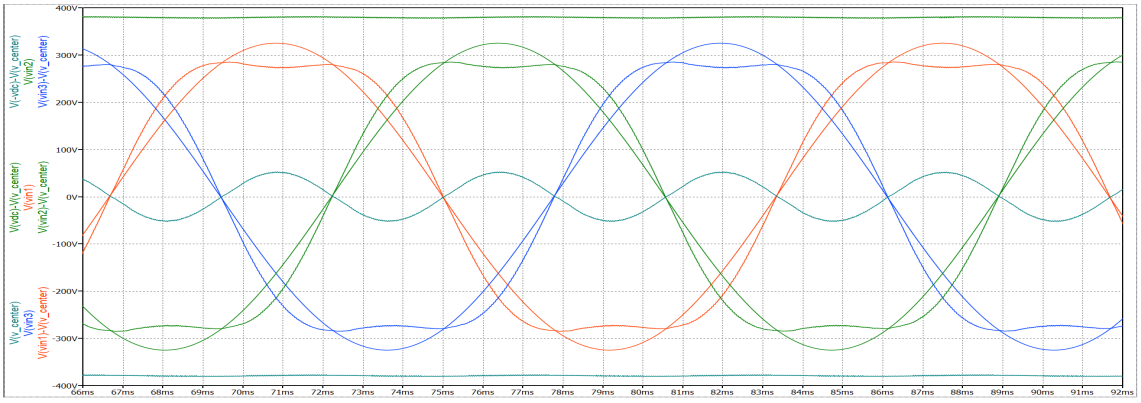


Figure 5.31: Zoom of the major waveforms obtained from the application of overmodulation at full load.

Final considerations about control

So far we have analysed different applicable control solutions, each with its own advantages and disadvantages. The two overmodulation techniques proposed allow for excellent operation, which can be further improved. They can be applied in two different contexts: applying a third harmonic injection directly on the modulating signal certainly allows one to work with less distortion, accepting to limit the Power Factor according to the distortion present in the line. Instead, injecting the third harmonic by applying a feedback control implies a slightly more distorting operation of the machine's centre voltage, but allows the system's PF to be further increased.
At this point we are ready to analyse the non-ideal operation of the machine, introducing distortions and imbalances in the line: a solution will then be proposed to improve the performance obtained with the closed-loop overmodulation method, which can also be used in the presence of non-ideal network conditions. Before continuing, it will be shown some code used to implement

the closed-loop overmodulation, without going into too much detail, in order to respect the company's secrecy. The code reported is related to the inductor current controller $n°1$, which has the same structure as the other two current controllers. Within the code, the values used for the calibration of the PIR have been omitted, together with the contents of some particularly sensitive functions.

```
double e_k = 0;       // error e(k)
double e_k1 = 0;      // error e(k-1)
double e_k2 = 0;      // error e(k-2)
double u_P = 0;       // P(k) out
double u_R_k = 0;     // R(k) out
double u_R_k1 = 0;    // R(k-1)
double u_R_k2 = 0;    // R(k-2)
double m_PI = 0;      // PI(k) out
double m_PIR = 0;     // PIR(k) out
double m_pwm = 1;     // modulating signal
double sin_ref = 0;   // first armonic current reference
double third_ref = 0;// third armonic current reference
bool clock_kI = 0;    //clock(k-1)
bool temp = 0;        //temporary variable
double intI_k = 0;    // intI(k)
double intI_k1 = 0;   //intI(k-1)
double FFthird = 0;   //feed_forward third armonic
const double Ki = xxx;
const double Kp = xxx;

#include <cmath>

//////////////////CALCULATION OF RESONANT CONTROL COEFFICIENTS//////////////////////////

const double Kr = xxx;
const double wc = xxx;

const double wo = 120 * M_PI;                          //2*pi*60 [rad/s]
const double Ts = 55e-6;                               //sampling period [s]
const double ao = 4 * Kr * wc * Ts;                    //Coefficient for R control
const double bo = (wo*wo*Ts*Ts) + 4 * wc * Ts + 4;     //Coefficient for R control
const double b1 = (2*wo*wo*Ts*Ts) - 8;                 //Coefficient for R control
const double b2 = (wo*wo*Ts*Ts) - 4 * wc * Ts + 4;     //Coefficient for R control
const double Ipeak_3_arm = (3 * wo * 0.155 * V_in_peak * C_in) / (I_fs); //third-arm_peak

////////////////////////// FUNCTION DEFINITION/////////////////////////////////////////

//Corrects integral memory as a function of input voltage
void PI_low_distortion (double Vin_sampled, double* mem_PI);

//Corrects the shape of the modulating signal at low loads
void DCM_low_distortion (double Vref, double* mod_signal, bool* var);

//Detects and corrects the state of the switch in critics cases,
//returning a value representing the action performed
bool operation_no_load(bool* PWM1, bool* temp);

////////////////////////////////////////////////////////////////////////////////////

union uData
{
   bool b;
   char c;
   unsigned char uc;
   short s;
   unsigned short us;
   int i;
   unsigned int ui;
   float f;
   double d;
   long long int i64;
   unsigned long long int ui64;
   char *str;
   unsigned char *bytes;
};
```

Figure 5.32: Current control, part 1; starting from the top we find the definition of the variables in use, the definition of the parameters used by the PR, the definition of certain functions whose contents will not be shown and the automatic definition of variable types.

```
// int DllMain() must exist and return 1 for a process to load the .DLL
int __stdcall DllMain(void *module, unsigned int reason, void *reserved) { return 1; }

// pins definition

#undef Vi1_n
#undef iL1_n
#undef iL_ref_n
#undef clock
#undef carrier_PWM
#undef PWM1
#undef iL1_err_n
#undef mod_PWM
#undef ref_iL1_n
#undef iL1_n_sampled
#undef third_arm
#undef PLL_third_arm
#undef probe1_1
#undef probe1_2
#undef probe1_3
#undef probe1_4

extern "C" __declspec(dllexport) void current_control_one(void **opaque, double t, union uData *data)
{
   double  Vi1_n            = data[ 0].d; // input
   double  iL1_n            = data[ 1].d; // input
   double  iL_ref_n         = data[ 2].d; // input
   bool    clock            = data[ 3].b; // input
   double  carrier_PWM      = data[ 4].d; // input
   double  PLL_third_arm    = data[ 5].d; // input
   double &PWM1             = data[6].d;  // output
   double &iL1_err_n        = data[7].d;  // output
   double &mod_PWM          = data[8].d;  // output
   double &ref_iL1_n        = data[9].d;  // output
   double &iL1_n_sampled    = data[10].d; // output
   double &third_arm        = data[11].d; // output
   double &probe1_1         = data[12].d; // output
   double &probe1_2         = data[13].d; // output
   double &probe1_3         = data[14].d; // output
   double &probe1_4         = data[15].d; // output


if((clock ^ clock_k1) & clock) //sampling istant
   {

    ////////////////////////////// UPDATING MEMORIES ////////////////////////////////////////////

     intI_k1 = intI_k;
     u_R_k2 = u_R_k1;
     u_R_k1 = u_R_k;
     e_k2 = e_k1;
     e_k1 = e_k;


     ////////////////////////////////// SAMPLING ////////////////////////////////////////////////

     iL1_n_sampled = iL1_n;                    // current sampling
     sin_ref = iL_ref_n * Vi1_n;               // calculation of the current reference without overmodulation
     third_ref = PLL_third_arm * Ipeak_3_arm;  // calculation of the overmodulation current reference
     e_k =  -((sin_ref + third_ref) - iL1_n);  // calcolo l'errore e_k in ingresso al PI

     ////////////////////////////////// PIR CONTROL /////////////////////////////////////////////
```

Figure 5.33: Current control, part 2; starting from the top we find the automatic definition of the various pins available on the digital block, subsequently associated with the type of variable for which they have been defined. This is followed by a clock signal rising edge detector with which the controller's memories are updated, performed the sampling and calculation of the various references used in the comparison block, as well as the calculation of certain variables used as visual output.

```
    ////////////////////////////// PIR CONTROL ////////////////////////////////////////////

    FFthird = xxx;

    u_P =  Kp * e_k;                                                    // discrete P control
    intI_k = intI_k1 + Ki * e_k;                                        // discrete I control
    u_R_k = (ao *(e_k - e_k2) - (b1 * u_R_k1 + b2 * u_R_k2))/bo ; // discrete R control

    m_PI = u_P + intI_k ;                                               // discrete PI control
    m_PIR = m_PI + u_R_k;                                               // discrete PIR control


    ////////////////////// ANTI WIND-UP for PI contribution ////////////////////////////////

    //higher thresholds to avoid intersection with the carrier
    if (m_PI >= 1.05)
    {
       m_PI  = 1.05;                //saturator
       intI_k = intI_k1 - Ki * e_k; //anti wind-up filter
    }
    else if (m_PI <= -1.05)
    {
       m_PI  = -1.05;               //saturator
       intI_k = intI_k1 + Ki * e_k; // anti wind-up filter
    }

     PI_low_distortion (Vi1_n, & intI_k1) //Function to reduce the distortion introduced by the PI
}


    ////////////////////////////////// EXECUTION ///////////////////////////////////////

    if((clock ^ clock_k1) & clock_k1)              //update instant
    {
      m_pwm = m_PIR + FFthird;                    //modulating signal with FF update
      DCM_low_distortion (iL_ref_n, &m_pwm, &temp) //Reduce the distortion introduced by the DCM operation
    }


   clock_k1 = clock; //clock(k-1) update

   ////////////////////////////// OUTPUT PROBE ////////////////////////////7////////

   probe1_1 = m_PI;     // print PI contribution
   probe1_2 = u_R_k;    // print R contribution
   probe1_3 = m_PIR;    // print PIR contribution
   probe1_4 = FFthird;  // print feedforward signal
   mod_PWM = m_pwm;     // print modulating signal
   ref_iL1_n = sin_ref; // print sinusoidal reference
   iL1_err_n = e_k;     // print e(k)


   ////////////////////////////////// MODULATOR ///////////////////////////////////////

   if (operation_no_load(&PWM1, &temp)==0) //dynamical management
   {
     if (fabs(m_pwm) <= carrier_PWM ) //comparison between modulating & carrier signal
     { PWM1 = 10; }//closed switch

      else
     { PWM1 = 0; } //open switch
   }

}
```

Figure 5.34: Current control, part 3; starting from the top, we find the code used by the PIR controller together with the wind-up filter, used for the integral component; this is followed by the execution block, acting half a period after the sampling instant, in which the modulating signal is produced; this is followed by a block for managing the visual outputs, followed by the final modulator.

Clearly, in order to realise an open-loop overmodulation control, it would have sufficed to eliminate the reference relative to the third harmonic shown in Fig. 5.33, also switching off the integral contribution by setting $K_i = 0$ in Fig. 5.32.

The code for the PI voltage controller is even simpler than the one just shown, as

it realises a simple PI control with a wind-up filter; as it is not possible to show the non-linear parameter handling used dynamically, the code contained in the relevant control block will be avoided.

The only block which we have not yet examined in detail turns out to be that concerning the virtual calculation of the ground reference, a voltage to which the machine clearly has no access as it has no neutral connection, so that the various measurements made with the probes can be referred to the grid centre, rather than to the machine centre. Although it is not possible to explicate the content of the block, it is nevertheless possible to mention that by means of a vector analysis, based on the voltages measured with respect to the machine centre, it is possible to accurately calculate the potential present at the grid centre, assuming an undistorted network is used.
In the case of a distorted network, the previous reasoning requires some corrections, implying the use of some specific signal processing techniques; we can therefore conclude that the error introduced by the calculation performed is definitely negligible.
Another important role played by this block is that of eliminating from the voltage reference, calculated with respect to the grid centre, any homopolar components present on the line. As we will see in the next chapter, this fact plays a fundamental role, since the system would clearly not be able to absorb any homopolar components from the network; by using this digital block, the system will not notice their presence on the network, thus avoiding to insert them within its current references unnecessarily.

6

Distorted and unbalanced power line

6.1 Fortescue's theorem: theory and applications

Having tested the operation of the overall system under ideal conditions, it is now necessary to analyse the performance provided by the system in the event on which the input voltage line would present distortions and imbalances. To analyse the operation of a system supplied by unbalanced voltages is clearly complex, as it is not clear how the system will respond, how much the machine centre voltage will be affected, or which currents will actually flow.
In order to study, predict and test the operation of the system under these conditions, it is therefore necessary to exploit a solid and efficient mathematical theory: the powerful Fortescue theorem.
First, however, it is worthwhile to provide some useful definitions in order to use a correct and cohesive language:

- We define a *"phasorial symmetrical ternary"* as a set of three isofrequential phasors characterised by:
  1. Same RMS value;
  2. Reciprocal phase shift of 120°.

- We then define a generic phasorial symmetrical ternary as a function of its cyclic direction of rotation, subdividing it into:
  1. Direct symmetrical ternary: possesses a clockwise cyclic direction of rotation;

2. Reverse symmetrical ternary: possesses a counter-clockwise cyclic direction of rotation.

- In contrast to the phasor symmetrical ternary, we can define *"phasor homopolar ternary"* as a set of three isofrequential phasors characterised by:

  1. Same RMS value;
  2. Null reciprocal phase shift.

- One last important distinction can be made in this regard:

  1. A ternary of isofrequential rotating vectors is called "pure" when the sum of the three components results to be zero: this is the case for the direct and inverse ternary;
  2. A ternary of isofrequential rotating vectors is called "spurious" when their sum is non-zero: this is the case for the homopolar ternary.

Figure 6.1 makes clearer the definitions just given.

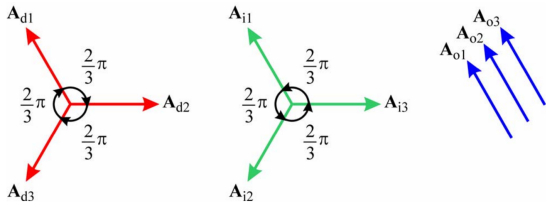


Figure 6.1: Starting from the left we observe a direct ternary, an inverse ternary and a homopolar ternary.

We can explain the enunciation of Fortescue's theorem as follows, looking at Fig. 6.2 to make the concept clearer:

"*Any ternary of isofrequency phasors is always uniquely decomposable into three further ternaries: one of direct sequence, one of inverse sequence and one of homopolar sequence.*"

The mathematical theory on which this fundamental theorem is based is not too complex, for which one may refer to any electrical engineering textbook. However, it is possible to outline its fundamentals by observing that any phasor multiplied by the phasor operator $\dot{\alpha} = e^{j\frac{2}{3}\pi}$ gives the phasor itself rotated anti-clockwise by 120°.

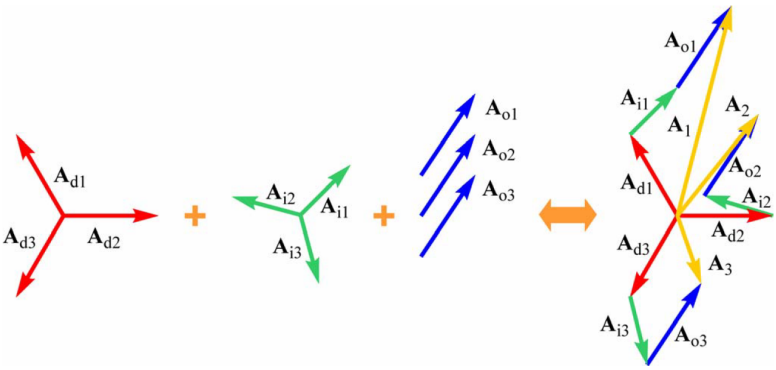


Figure 6.2: Unbalanced ternary decomposed by using Fortescue's theorem.

By defining then $\dot{\alpha}$ as a phasorial rotation operator, it is then possible to define:

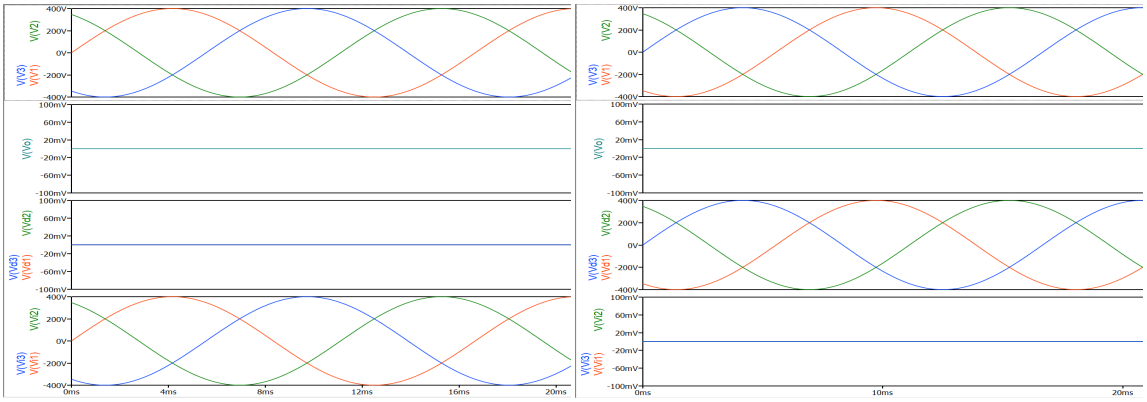
- A direct ternary, by taking a generic phasor and multiplying it by the vector $(1, \dot{\alpha}^2, \dot{\alpha})$;
- An inverse ternary, by taking a generic phasor and multiplying it by the vector $(1, \dot{\alpha}, \dot{\alpha}^2)$;
- A homopolar ternary, by taking a generic phasor and multiplying it by the vector $(1, 1, 1)$.

It is then possible to consider any unbalanced triplet of phasors and perform a base change, defining an appropriate transformation matrix $\|S\|$ with its inverse $\|S^{-1}\|$ as follows:

$$\overrightarrow{V_{orig}} = \begin{bmatrix} \overline{V_1} \\ \overline{V_2} \\ \overline{V_3} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \dot{\alpha}^2 & \dot{\alpha} \\ 1 & \dot{\alpha} & \dot{\alpha}^2 \end{bmatrix} \cdot \begin{bmatrix} \overline{V_o} \\ \overline{V_d} \\ \overline{V_i} \end{bmatrix} = \|S\| \cdot \overrightarrow{V_{fort}}$$

$$\overrightarrow{V_{fort}} = \begin{bmatrix} \overline{V_o} \\ \overline{V_d} \\ \overline{V_i} \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \dot{\alpha} & \dot{\alpha}^2 \\ 1 & \dot{\alpha}^2 & \dot{\alpha} \end{bmatrix} \cdot \begin{bmatrix} \overline{V_1} \\ \overline{V_2} \\ \overline{V_3} \end{bmatrix} = \|S^{-1}\| \cdot \overrightarrow{V_{orig}}$$

where $\overrightarrow{V_{orig}}$ represents the original ternary of phasors to be decomposed, while $\overrightarrow{V_{fort}}$ represents the ternary composed by the first phasors belonging to the homopolar ternary $\overline{V_o}$, direct $\overline{V_d}$ and inverse $\overline{V_i}$.
The matrices $\|S\|$ and $\|S^{-1}\|$ clearly contain the coefficients belonging to a linear system with three known variables and three equations: it is therefore always



(a) (b)

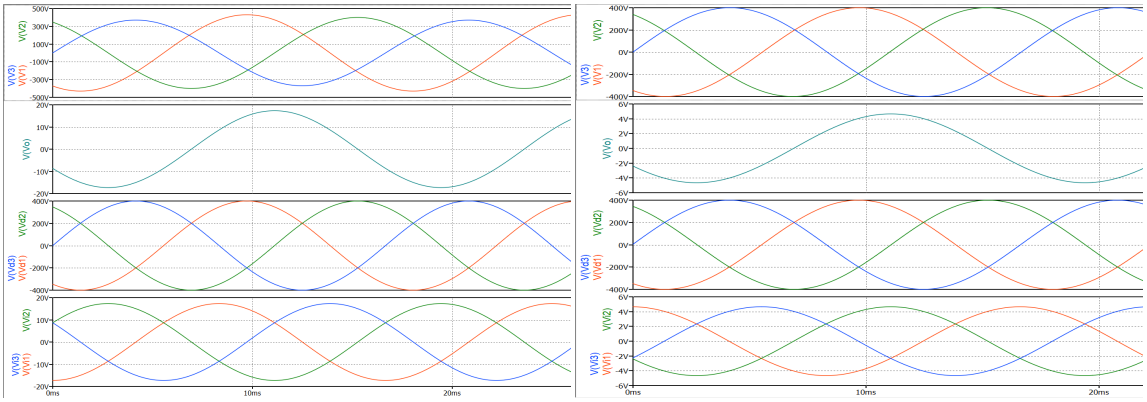
Figure 6.3: Decomposition of sequences; balanced ternaries realised by phasors: $\overline{V_1} = 400 \cdot e^{j0}[V]$, $\overline{V_2} = 400 \cdot e^{j\frac{\pi}{3}}[V]$, $\overline{V_3} = 400 \cdot e^{j\frac{2\pi}{3}}[V]$ (a); $\overline{V_1} = 400 \cdot e^{j\frac{2\pi}{3}}[V]$, $\overline{V_2} = 400 \cdot e^{j\frac{\pi}{3}}[V]$, $\overline{V_3} = 400 \cdot e^{j0}[V]$ (b). In the first boxes, the original symmetrical ternaries are visible; moving down we find, respectively, the homopolar, direct and inverse components.

possible to obtain an univocal solution to the problem.

Before continuing, it appears important to reduce the number of operations to be carried out each time we wish to perform a decomposition of sequences by means of Fortescue's theorem: it may be a good choice to create a simple program in order to automate the matrix calculation between phasors, since the theorem just presented will turn out to be of fundamental importance during the analysis of the system.
Recalling then that a generic sinusoidal signal can be transformed into its corresponding phasor by means of the relation 6.1, it becomes immediate to realise the automated file so as to know from the outset which sequences will compose the test signals, which will be inserted on the power supply lines within the complete simulation.

$$x(t) = A \cdot \sin(\omega t + \phi) = \mathrm{Im}\left[Ae^{j\phi} \cdot e^{j\omega t}\right] = \mathrm{Im}\left[\overline{X} \cdot e^{j\omega t}\right] \tag{6.1}$$

Doing some tests we can initially observe that, as shown in Figure 6.3, trying to decompose a pure symmetrical ternary we obtain either only direct components or only inverse components, as a function of the fact that a certain phase results out of phase with respect to another by $+120°$ or $-120°$. Trying instead to unbalance the original ternary, while maintaining the $120°$ phase-to-phase



(a) (b)

Figure 6.4: Decomposition of sequences; original balanced ternary with phasors: $\overline{V_1} = 430 \cdot e^{j\frac{2\pi}{3}}[V]$, $\overline{V_2} = 400 \cdot e^{j\frac{\pi}{3}}[V]$, $\overline{V_3} = 370 \cdot e^{j0}[V]$ (a); $\overline{V_1} = 400 \cdot e^{j\frac{2\pi}{3}}[V]$, $\overline{V_2} = 400 \cdot e^{j\frac{61\pi}{90}}[V]$, $\overline{V_3} = 400 \cdot e^{j0}[V]$ (b).

displacement, we obtain what is shown in Figure 6.4 (a): in the latter we have imposed $\overline{V_1} = 430 \cdot e^{j\frac{2\pi}{3}}[V]$, $\overline{V_2} = 400 \cdot e^{j\frac{\pi}{3}}[V]$, $\overline{V_3} = 370 \cdot e^{j0}[V]$.

It is interesting to observe how the decomposition of the sequences places most of the contribution on the direct sequence, generating a three-phase ternary with 400 $[V_{peak}]$ for each phase. The inverse sequence, on the other hand, maintains an oscillation amplitude of 15 $[V_{peak}]$, as does the homopolar component: the latter, added to the contribution of the inverse sequence, will generate the missing contributions of 30 $[V_{peak}]$, 0 $[V_{peak}]$ end -30 $[V_{peak}]$ in order to correctly decompose the original ternary. We can perform a final test by repeating the analysis performed in Figure 6.3 (b), this time imposing the phase of the second phasor equal to 122° instead of 120°; we then obtain what is shown in Figure 6.4 (b), observing how both an inverse and a homopolar component is again generated, both having amplitude ~ 5 $[V_{peak}]$.

In view of the analysis we have to conduct we can then make an important observation: *any homopolar component present in the grid cannot generate current contribution within the system realized, as it is not possible to absorb from the grid any current component that does not represent a pure balanced ternary*.
Trying however to track this component, it would generate in the system a triplet of homopolar current superimposed on the overmodulation component, with no possibility of absorbing it from the grid. However, as already reported at the end of the previous chapter, the digital algorithm developed in order to refer the

measured voltages to the grid centre, rather than to the machine centre, does not allow the system itself to notice the presence of any homopolar component in the grid.
In view of this, we can then conclude that a voltage line represented by an undistorted and unbalanced ternary introduces:

- A direct and reverse symmetrical ternary, which can generate current components circulating in the circuit without ideally affecting the machine centre voltage;
- A homopolar ternary that cannot be detected by the system; its contribution will then be placed directly on the machine centre voltage, thus preventing the circulation of any homopolar current component, superimposing itself on any other voltage contribution present on the machine centre.

In the case in which the power supply network also exhibits harmonic distortion, it is possible to repeat the same analysis as presented earlier: any distorting component, which cannot be represented by a balanced symmetrical ternary, will introduce a symmetrical direct and inverse voltage ternary into the network, adding instead to the machine centre voltage the corresponding homopolar component that cannot be detected by the system.

We then try to verify how the system behaves by inserting unbalance and distortion into the grid, taking advantage of what is reported in the chapter regarding American grids in order to simulate a real power line.
Knowing first of all that we are using a three-phase network at 480 $[V_{RMS}]$ concatenated, we can expect to find a star voltage equal to $V_{star} = \frac{480}{\sqrt{3}}\ [V_{RMS}] = 277\ [V_{RMS}]$, from which $V_{star} = 392\ [V_{peak}]$. In order to simulate an unbalanced network we can now assume that there is 3% of Voltage Unbalance, measured according to the equation 2.1, which represents the worst case of unbalance that can be encountered, according to the norms given above.
Assuming then that the three concatenated phases possess value $V_{L1} = 480\ [V_{RMS}]$, $V_{L2} = 480 + \Delta\ [V_{RMS}]$ end $V_{L3} = 480 - \Delta\ [V_{RMS}]$ we can simplify the actual calculation, obtaining an imbalance of $\Delta = 14.4\ [V] \sim 14\ [V]$.
By posing then $V_{L1} = 480\ [V_{RMS}]$, $V_{L2} = 494\ [V_{RMS}]$ e $V_{L3} = 466\ [V_{RMS}]$ it is now convenient to calculate Fermat's point[1] belonging to the realised phasorial trian-

[1]Having to perform the triangle-star conversion through a non-equilateral triangle such as

gle, in order to perform the triangle-star conversion while maintaining the 120° phaseshift present between phase and phase. By performing an iterative calculation, we can approximate the result with $V_{\text{star }1} = 396\ [V_{peak}]$, $V_{\text{star }2} = 368\ [V_{peak}]$ and $V_{\text{star }3} = 417\ [V_{peak}]$: these will be the peak values used in the star voltage generators used in the simulation[2].
It is also possible to add a distorting harmonic contribution to the line voltage by placing a third harmonic voltage equal to $V_{\text{3rd peak}} \sim 16\ [V_{peak}]$ and a fifth harmonic having $V_{\text{5rd peak}} \sim 5\ [V_{peak}]$, as stated in the chapter concerning American networks.
We can thus evaluate the behaviour of the system in the presence of strong unbalance and distortion, studying a case very far from the ideal one.

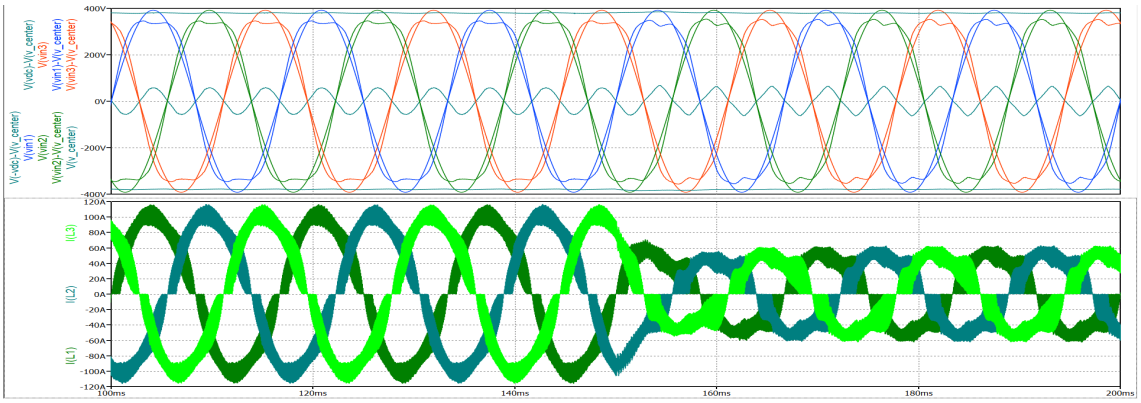


Figure 6.5: Overmodulation performance realised in closed loop; the simulated system is fed through an ideal North American network.

We will now clearly focus on the overmodulation technique with injection of the third harmonic in the reference, since it is the only one that allows the harmonics present in the network to be tracked, as required by the specification; the latter is also the most complex solution, since it presents more distortion generated and more management difficulties.
Two figures are then shown: Fig. 6.5 shows, for the first time, the operation of

ours, it is necessary to calculate the point inside the triangle representing the grid centre of the system, which maintains a phase shift equal to 120° among the segments constructed between each angle of the triangle and the point sought; the latter, in our case, is called Fermat's point.

[2]This conversion was necessary because, for simplicity's sake, star voltage generators were used in the simulation rather than concatenated voltages, exploiting the appropriate star-delta conversion.

the system with the American grid voltage at 480 [V_{RMS}] concatenated, without unbalance and distortion. The voltage V_{dc}, as can be seen, is lower than the peak voltage of the three phases: it is then clear that overmodulation is essential in order to manage the entire system without losing control.

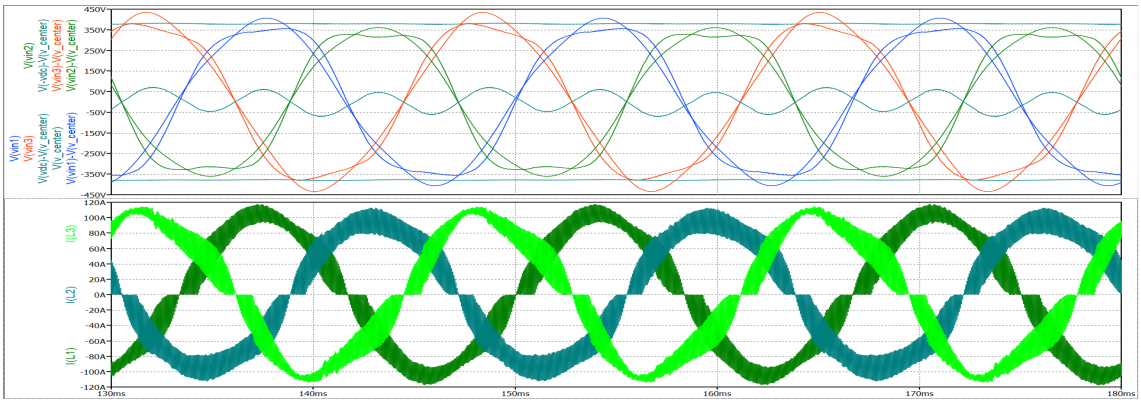


Figure 6.6: Effects of a strongly unbalanced and distorted three-phase network connected to the Vienna Rectifier with overmodulation control; most significant waveforms.

Figure 6.6 shows instead the case of strong distortions and imbalances presented above. For the test, phase shifts equal to 120° were maintained only for the fundamental line harmonics: random phase shifts were imposed for the higher harmonics, in order to simulate a critical case of unbalanced and out-of-phase harmonics. The following table summarises the values set for the various harmonics:

	Amplitude [V_{peak}]	Phase [deg]
$V_{1\ 1st\ harm}$	396	0
$V_{2\ 1st\ harm}$	368	-120
$V_{3\ 1st\ harm}$	417	-240
$V_{1\ 3rd\ harm}$	16	105
$V_{2\ 3rd\ harm}$	16	34
$V_{3\ 3rd\ harm}$	16	220
$V_{1\ 5rd\ harm}$	5	15
$V_{2\ 5rd\ harm}$	5	123
$V_{3\ 5th\ harm}$	5	292

Table 6.1: Values assigned to the various voltage harmonics used as tests within the simulated line.

Fig. 6.6 also shows how the operating range gained through overmodulation turns out to be much reduced due to the non-idealities of the network. Generally

speaking, the direct and inverse harmonic components, present in the grid, model in a non-symmetrical pattern the various phase voltages of the circuit; instead, the circulating common ripple components add their contribution to the machine centre voltage, thus altering the sinusoidal waveform generated by the third harmonic injection.
This results in non-optimal overmodulation, as both the amplitude and the phase of the injected third harmonic do not take into account the non-idealities present both in the network and in the system: in the next section, a suitable optimisation method will be presented, in order to gain as much operating range as possible through overmodulation.

6.2 "Disturb and Observe" algorithm

The impossibility of performing a real-time FFT of the network, by means of the board's internal processor, makes it impossible to calculate the exact amplitude and phase relative to the third harmonic of current to be injected.
Not being able to predict, then, the direct and inverse components present in the network, it is possible to develop an algorithm called "*Perturb and Observe*", capable of performing an autonomous research of optimal phase and amplitude to be associated to the circulating third current harmonic[3].
The idea is to analyse the result obtained by overmodulation, then varying the phase and amplitude of the third harmonic in order to obtain a better result than the previous one. Proceeding iteratively, the optimal overmodulation conditions are thus found, without having access to the information on the harmonic content present in the grid.

In simulation I have then realised an algorithm that carries out what has been said, which performs the following 4 steps:

1. *Approximately* research for an optimal value for the phase:

   (a) Maintain the usual amplitude and phase of overmodulation: sample the three voltage lines for a period, then calculate the following value:
   $$\text{maximum} = \max_T \{|V_{\text{in } 1(t)}|, |V_{\text{in } 2(t)}|, |V_{\text{in } 3(t)}|\}$$

   (b) Increase the phase by 15° and repeat the calculation, comparing the maximum found with that calculated in the previous cycle; if a lower value is obtained, the phase found is better than the previous one: starting from the latter phase found, proceed iteratively. If, on the other hand, a higher value is found than the previous one, go back to the phase used previously and subtract 15°, repeating the process again iteratively, reducing the value of the phase used rather than increasing it;

   (c) If by increasing and decreasing the phase by 15° it continues to find larger values than previously found, it means that the phase found is close to the optimal phase sought: move on to the next step.

2. *Accurate* research for an optimal value for the phase:

[3]Among the various alternatives, the *P&O* algorithm appears to be a valid solution to the problem.

   (a) Repeat the previous algorithm doing steps of 3° rather than 15°, starting from the phase found approximately in the previous step;

   (b) If by increasing and decreasing the phase by 3° it continues to find values larger than those found previously, it means that the phase found is the optimal phase sought: move on to the next phase, keeping the phase found in memory.

3. *Approximately* research for an optimal value for the amplitude:

   (a) Repeat the first step of the algorithm maintaining the phase found and varying, this time, the amplitude of the third current harmonic, making amplitude variations equal to 3% of the maximum value reached by the three voltage lines;

   (b) If increasing and decreasing the amplitude it continues to find higher values than those found previously, it means that the amplitude found is close to the optimum amplitude sought: move on to the next step.

4. *Accurate* research for an optimal value for the amplitude:

   (a) Repeat the previous algorithm by making amplitude variations equal to 1% of the maximum value reached by the three voltage lines, starting from the amplitude found approximately in the previous step;

   (b) If by increasing and decreasing the amplitude it continues to find larger values than those found previously, it means that the amplitude found is the optimum amplitude sought: by then setting optimum phase and amplitude we have optimised the effect of overmodulation.

The algorithm just proposed makes it possible to obtain, in less than a few seconds, a significantly wider working range with respect to its non-application. The multi-step search makes it possible to find the conditions for optimal application of the third harmonic without having to test all combinations, including the worst case, and also to avoid making small variations from the outset, which would lead to a longer time required. Working with absolute values also makes it possible to obtain signals perfectly centred in 0 $[V]$: by trying to lower the maximum and minimum values reached as much as possible, the equilibrium condition will be obtained when $V_{max} = |V_{min}|$.

It is possible to analyse the performance provided by the algorithm just proposed by looking at Figs. 6.7, 6.8 and 6.9. The first image shows the unbalanced and distorted network used for the test, measured with respect to the machine

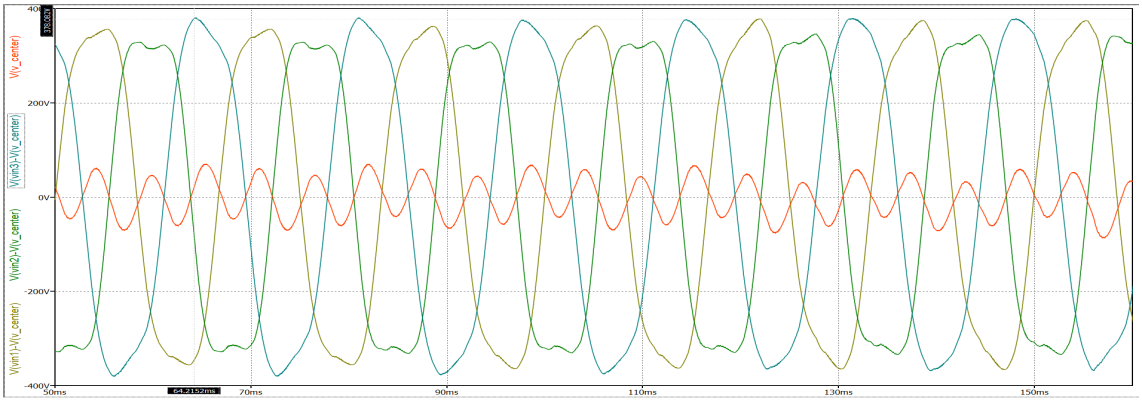


Figure 6.7: Strongly distorted and unbalanced line voltage, measured with respect to the machine centre voltage, where the signal in red represents the machine centre voltage measured with respect to the network centre; in the second half of the image, small variations in the signals can be seen as the previously proposed $P\&O$ algorithm has just been activated.

centre, with parameters summarised in Table 6.1. As can be seen, a cursor positioned on the maximum peak indicates that the voltage peak is reached at $\sim 378\ [V]$: knowing that each output half-bank presents 380 $[V]$ at its terminals, we come to the conclusion that there is an operating range of only 2 $[V]$ before the system loses control.

As can be seen, the peak reached by the signal in blue has decreased, while that reached by the signal in yellow has increased; the algorithm has stopped at the moment when the peak reached by the higher signal has decreased to the point where it reaches one of the peaks belonging to the other two signals.

When the algorithm has concluded, the cursor allows us to demonstrate that the maximum peak reached by the system is 369 $[V]$, allowing us to extend the operating range by $\sim 18[V]$ with respect to the previous case, obtaining an operating margin of 11 $[V]$ on both the positive and negative banks, compared to the 2 $[V]$ declared previously.

Fig. 6.9 instead shows the algorithm in action, allowing us to observe the phase and amplitude trends applied to the third current harmonic during the optimisation phase. The first to be subjected to variations is the phase, represented by the signal in red, which undergoes high step variations (first step) and then reduced (second step) until it finds the optimum value at which it will be stabilised; at this point the perturbation of the amplitude begins, represented by the signal in blue, which also undergoes high step variations and then reduced.

As can be seen, the optimum values obtained under these test conditions are:

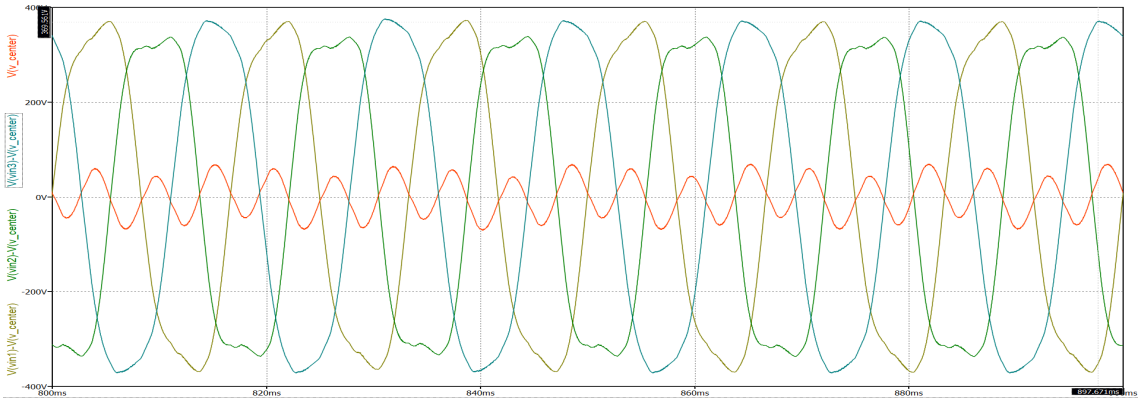


Figure 6.8: Highly distorted and unbalanced line voltage, measured with respect to the machine centre voltage, where the latter was optimised using the previously proposed *P&O* algorithm.

- Third harmonic current phase equal to $-65°$ instead of $-90°$;
- Amplitude of third harmonic current increased by $\sim$ 13% compared to the usual.

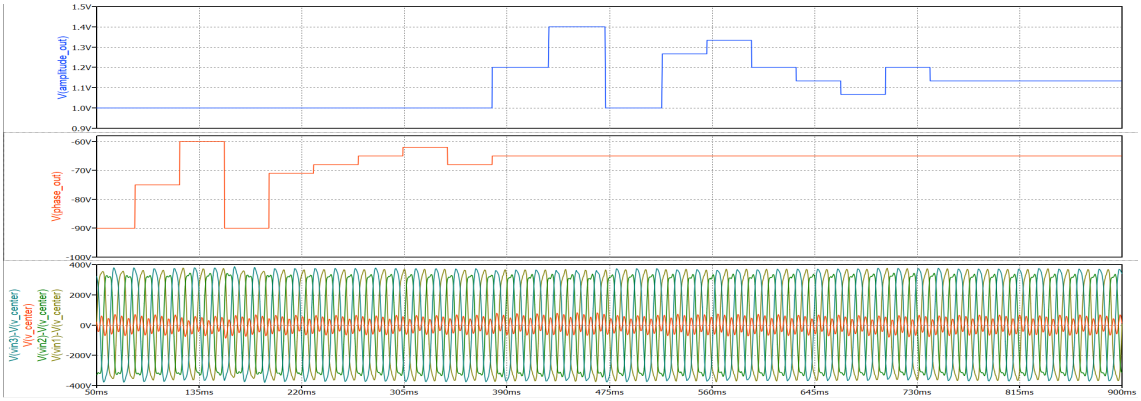


Figure 6.9: Algorithm *P&O* in action: the first box shows the normalised amplitude trend relative to the third harmonic current, while the second represents the corresponding phase trend, expressed in degrees; the last box shows the trend of the line voltages, measured with respect to the machine centre voltage during the application of the proposed algorithm.

However, it is quite easy to demonstrate graphically how this algorithm cannot always find the optimal operating point; with a simple online graphical tool, it can be observed that:

- The system can admit, depending on the grid distortion, one or more points of relative minimum in addition to an absolute minimum: the algorithm is clearly not able to distinguish one from the other, since it was

developed in such a way as to avoid analysing all possible combinations of phase and amplitude, so as to avoid having to necessarily test even the worst operating point;

- In certain cases, optimum conditions can be found by searching for the absolute minimum, through amplitude variations, using a phase from a relative minimum wrongly exchanged for an absolute minimum.

Various techniques can then be implemented in order to further optimise the proposed algorithm; one solution might be to repeat the same algorithm several times in the event in which the result obtained does not satisfy certain predefined standards, proceeding with the research of further relative minimums of phase or amplitude.

Before concluding, we can observe what would happen supposing we were working under even worse conditions than the limit case analysed above: trying to double the amplitude owned by the multiple harmonics present in the network we obtain, even before activating the algorithm $P\&O$, what is shown in Figure 6.10.

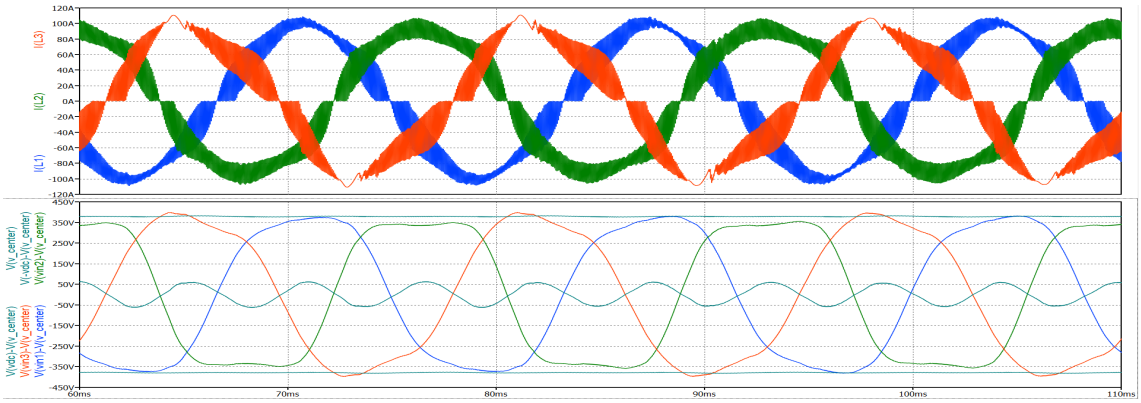


Figure 6.10: Performance of the system connected to a highly distorted and unbalanced network, beyond the permitted North American legal limits: as can be seen, temporarily exceeding the operational limits does not lead to any stability problems, despite having temporarily lost the control of the system.

In this last image we can observe the three phase currents and the three input voltages, measured with respect to the machine centre voltage, placed in conditions of unbalance and distortion outside all permitted limits. It is interesting to observe how the input voltage, represented by the signal in red, exceeds the output voltage of the two half-banks for a certain time, forcing the respective

diodes to conduct and thus generating a momentarily ripple-free inductor current.
This last observation proves that even if the control of the system were to be momentarily lost, the system would be able to recover as soon as the absolute value of the input voltage returns to a value less than the half-bank voltage.
Assuming then that the system has to be operated within a completely unbalanced and distorted network, such as the one just proposed, we can ensure a momentary operation also outside the operating limits, at least until the proposed algorithm optimises the chosen operating point by further lowering the equivalent input voltage.

7

Experimental tests: comparison with theoretical results

In parallel with the simulation program, a test board was created in the company's laboratory in order to carry out some practical tests; during the internship period it was therefore possible to directly observe the operation of the machine, although in a partial way compared to what previously presented. Fig. 7.1 shows the test station in the laboratory; the board used is instead shown in more detail in Figure 7.2, after having hidden the sensitive information reported on the various components on it.
Looking at the latter it is possible to observe, on the left-hand side, the input stage on which the entire study was focused, dedicating the right-hand side of the board to the output inverter; the batteries inside the UPS are not shown as they require a dedicated space.
Among the various components included in the input stage board, the following can be observed:

- 12 coils; 6 are used for filtering, while the remaining ones represent the 3 input inductances in pairs of two. As can be seen, the current probe shown in the image has only been connected to one of the two coils representing an input inductance: this information will come useful later on, as some images, captured using the oscilloscope, will be reported;

- 12 capacitors interspersed with some heatsinks: the latter represent a single half-bank capacitance. The second capacitance is realised with the same components, shown on the right-hand side of the board;

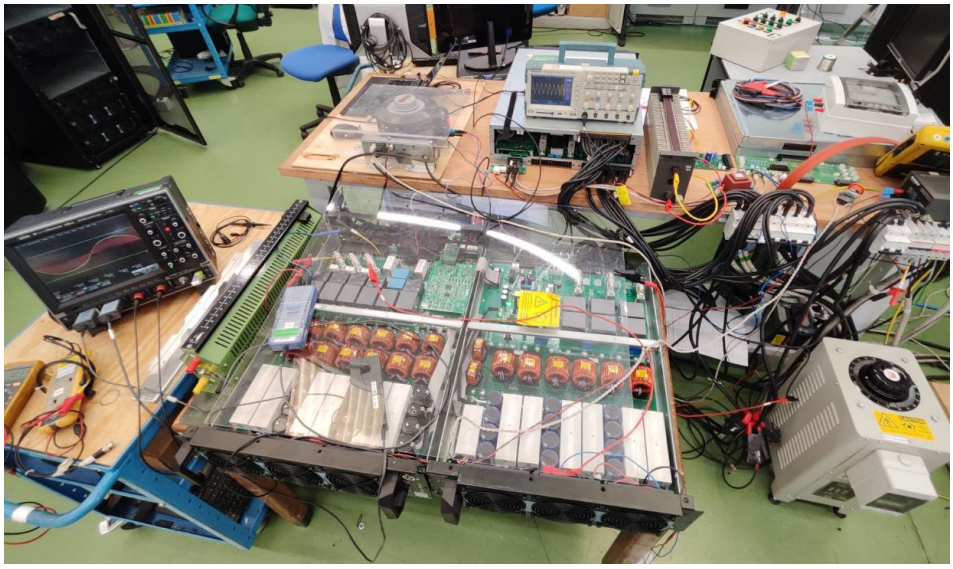


Figure 7.1: Test station in the laboratory.

- Further types of capacitors, visible in the upper part of the picture, where 6 of them realise the three input capacitances; several types of protection, formed by relays and various fuses, are also visible.

It is also interesting to note that the communication between the board and the computer, used to test the different types of controls presented, takes place using an opto-isolation system: this allows us to protect the control instrumentation from disturbances and faults, providing safety for both the latter and the staff that use it. Using a JTAG protocol it is also possible to directly access the variables present in the several memory cells during machine operation, being able to observe in real-time what is happening inside the processor used.
In order to perform all the necessary tests, the following devices can also be observed within Fig. 7.1:

- Various probes and oscilloscopes;
- An UPS capable of generating up to 200 $[kVA]$: this makes it possible to supply the machine with any type of line voltage needed, simulating both balanced and unbalanced voltages.
- A variac: the latter represents a transformer with a variable centre-tap, used in order to carry out initial tests with much lower voltages than those that would be present at normal operation: in this way it is possible to carry out the first tests safely;
- A variable load of up to 200 $[kW]$;

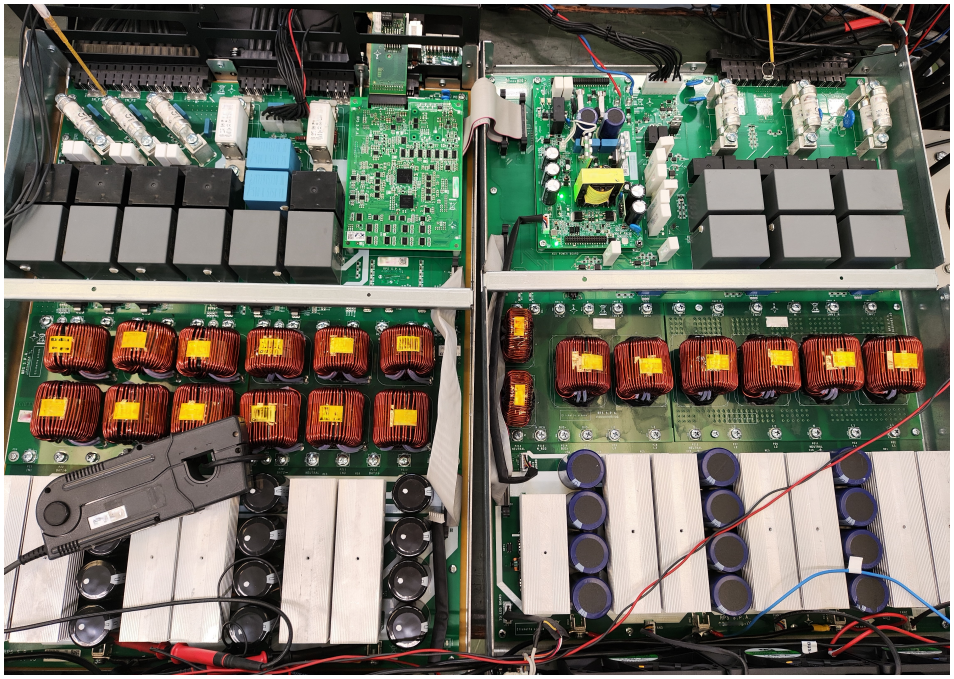
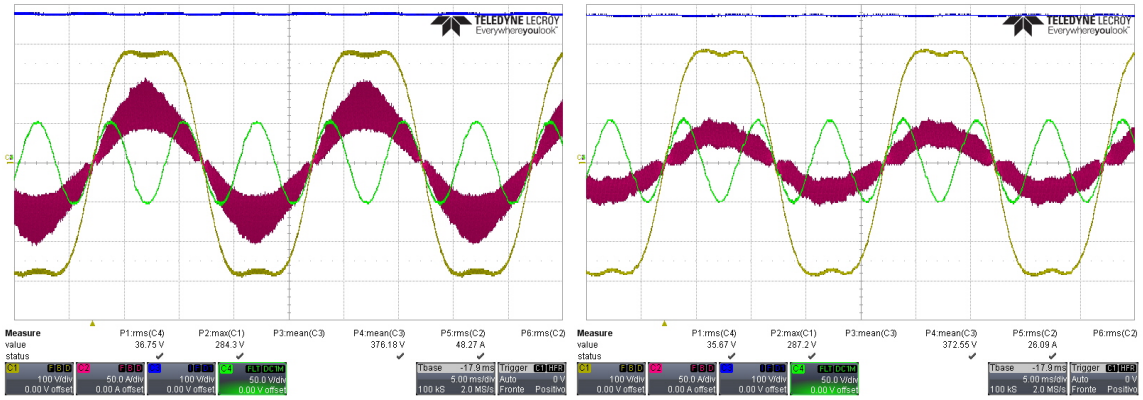


Figure 7.2: Board under consideration; on the left we find the input stage, on the right the output inverter.

After having followed various safety rules and having equipped oneself with the necessary PPE[1], we are then ready to carry out some tests in the laboratory; some examples of machine operation are given below, obtained during several tests carried out in the laboratory.

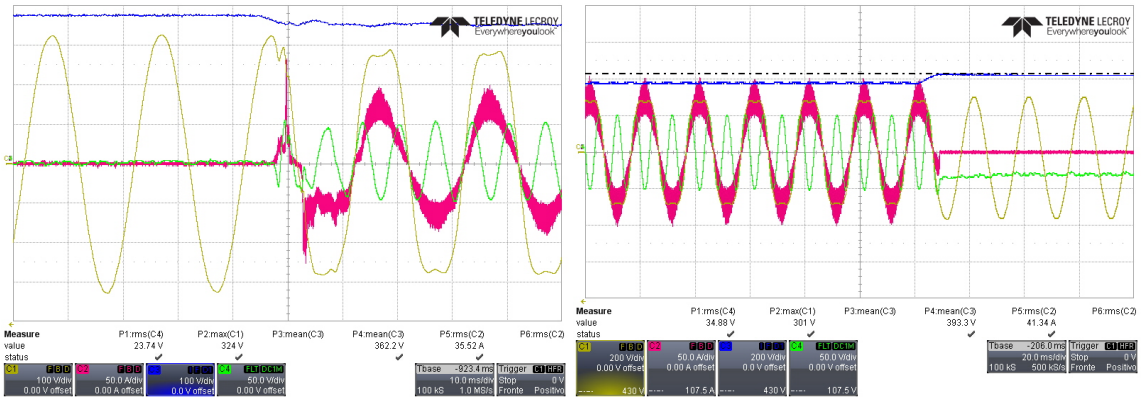


(a) (b)

Figure 7.3: Laboratory test: operation at steady state (a) and with halved load (b).

[1]Personal Protective Equipment.

Fig. 7.3 represents, for example, the operation of the machine under the same test conditions used to carry out the simulation shown in Figure 5.26, thus exploiting the overmodulation obtained through open loop control. In the picture we can observe the voltage of the positive half-bank (in blue), the voltage of the first supply line measured with respect to the machine centre (in yellow), the corresponding inductor current (in red) and the machine centre voltage (in green); as already mentioned above, the current shown represents only half of the inductor current actually present on the entire input coil.
Comparing the result obtained from the simulation with that obtained through the real machine, it is possible to state that what is shown by the simulation model can be considered more than valid: as already demonstrated through the simulator, this type of overmodulation greatly reduces the distortion generated by its application, allowing excellent performance to be achieved even at operation other than at full load.

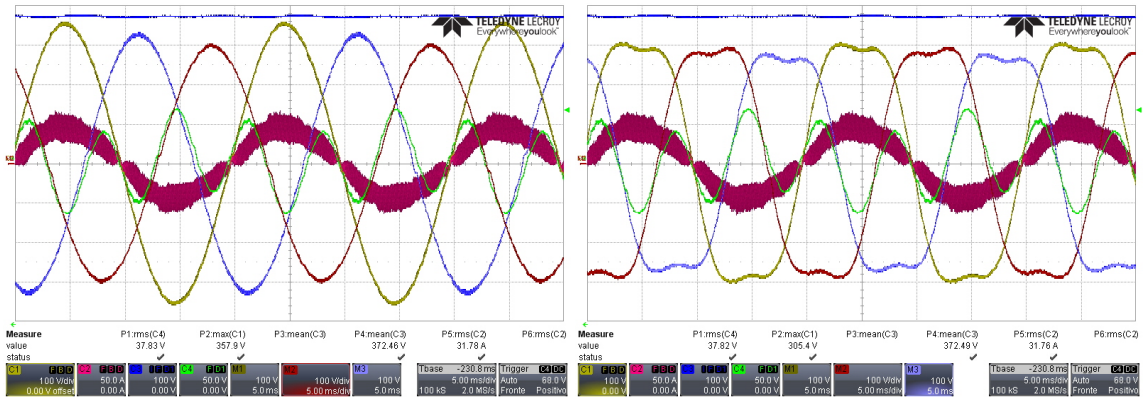


(a) (b)

Figure 7.4: Laboratory test: switching from burst-mode → full load operation (a) and vice versa (b).

Fig. 7.4 allows instead to verify certain characteristics of the machine in particular states of operation. Figure 7.4 (a) allows us to observe how, during burst-mode operation, the machine centre voltage is practically stationary, despite the overmodulation required by the control being applied: as previously explained, since no current can circulate, there is no way for the third harmonic to circulate; this latter fact ensures that the machine centre voltage is stationary, as demonstrated by the equation 4.5.
Fig. 7.4 (b) shows instead what happens when we pass from full-load operation to burst-mode operation, occurring at an instant which is not a multiple of the

period of the machine centre voltage: the overmodulation, abruptly interrupted, loses all possibility of controlling the machine centre voltage, leaving the latter at a random value $\neq 0$ $[V]$. The latter will then be slowly returned to the voltage of 0 $[V]$ thanks to the bank regulator, as visible in the same image.



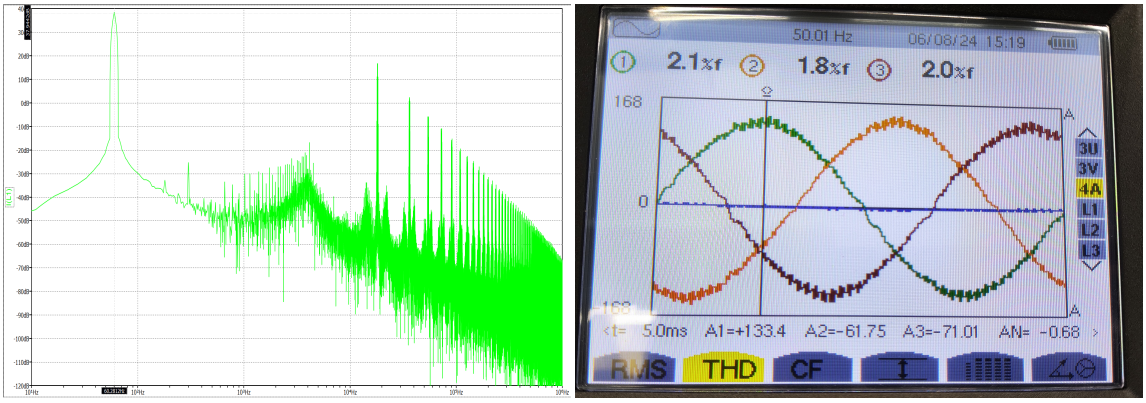
(a) (b)

Figure 7.5: Laboratory test carried out with unbalanced voltages: 255 $[V_{RMS}]$, 230 $[V_{RMS}]$, 215 $[V_{RMS}]$.

It was also possible to observe the behaviour of the system when subjected to unbalanced line voltages, using a 200 $[kVA]$ UPS as mentioned above in order to realise a specific unbalanced line voltage, such as the one shown in Figure 7.5 (a). Fig. 7.5 (b) shows instead the operation of the system after the application of a different algorithm from the P&O previously presented, based fundamentally on the generation of a first harmonic voltage superimposed on those already present on the machine centre voltage. This latter solution results to be particularly sensitive to the company, reason why it will not be explored further.

Finally, it is possible to verify whether the performance offered by certain controllers, tested by simulation, actually performs better than others. In fact, QSPICE simulator allows us to perform certain intensive operations such as the FFT of specific signals: we can, in this way, quantify the current THD value generated by the system under test, comparing the performance obtained through the implementation of the PI, PR and PIR controllers.
The following test conditions were then set, repeated for all three controllers, temporarily eliminating the effect of overmodulation:

- Full load operation: simulations were carried out assuming a load of



(a) (b)

Figure 7.6: FFT applied to an inductor current within the complete three-phase model, which uses PI controllers with feed-forward (a); THD measured in the laboratory using PR controllers (b).

10 [Ω], drawing an output power equal to 57.560 [kW];

- The power supply used is undistorted and unbalanced. The peak voltage of each line was set to 325 [V_{peak}] in order to avoid overmodulation;
- The FFT was applied to a one-phase current only, using an observation window of 11 line periods so that no temporal leakage problems could occur, and also to avoid the phenomenon of Scalopping Loss by the DFT used;
- The windowing was realised using the usual rectangle function: the latter ensures the best possible frequency separation.

Fig. 7.6 (a) shows, as an example, the result obtained with regard to the PI control with feed-forward signal included. Leaving aside the high-frequency harmonics, which make up the superimposed ripple, it is possible to calculate the THD value by means of the equation 2.4, using the current harmonics comprised from the first to the fifteenth. However, the result obtained turns out to be completely unrealistic: the calculated THD is found to be -61.57 [dB], which corresponds to a percentage equal to 0.0000692% of distortion.
Carrying out the same test with the remaining two controllers we obtain practically comparable performances, coming to the conclusion that the simulation realised is still too ideal to be able to analyse the performance that can really be generated by the developed controllers. The THDs obtained, having practically zero values, are however a sign of excellent operation on the part of the controllers, giving us the possibility of at least ideally obtaining more than optimal

operation on the part of all three cases analysed.
Fig. 7.6(b) shows instead the result obtained in the laboratory, through the use of a network analyser, regarding the performance generated by a PR controller: as can be seen, the THD reported was, respectively, equal to 2.1%, 1.8% and 2.0% for the various current phases.
The performance obtained, on the other hand, by means of a PI controller, showed THD values in the region of 3%, thus showing a slight improvement in the performance offered by the PR controller with respect to the classic PI controller.

8

Conclusions and future developments

What has been observed so far leads us to conclude that the realisation of the project is more than feasible: the forced flow of a third harmonic current, within the network, makes the realised overmodulation a solid and robust operating technique, as it is based on the electrical properties of the network. The developed *P&O* algorithm also ensures an optimal operation, even under conditions of strong distortion and unbalance by the grid, according to American non-ideality standards. It has also been demonstrated how, even in conditions of unbalance and distortion outside the established limits, the machine is able to operate without problems, always finding an optimal operating point; the presence of the banks regulator also allows the system to operate even when supplying unbalanced loads.

The analysis based on the performance of the implemented controls also suggested that a current PIR control could be an excellent solution to the problem, as it allows to merge together the excellent steady-state performance provided by a purely resonant control with the simplicity of control that characterises any PI controller.

The two overmodulation techniques tested show how the injection of the third harmonic, carried out in the current references, further increases the Power Factor of the system developed, while minimising the reactive power recalled from the grid. On the other hand, the centre bank voltage turns out to be more difficult to control, compared to the open loop injection method, as it is more sensitive to distortion phenomena, making it necessary to use a *P&O* system capable of optimising the required operating point.

As an alternative, it is possible to review the design objectives, avoiding tracking the main harmonics present in the network and accepting a decrease in the value owned by the Power Factor of the system, thus allowing the use of the open-loop overmodulation technique. This would greatly reduce some of the visible distortion effects on the machine centre voltage, achieving even at lower loads an optimal overmodulation operation.
The QSPICE simulator, which was used in the development of the project, has proved to be a valid working tool, allowing the realisation of a complex simulation project and at the same time generating excellent results that accurately reflect the reality.

Anyway, the project is not to be considered complete yet; further complex control techniques can be implemented and tested, such as the possibility of exploiting several resonant controllers, in order to track higher harmonics present in the network. This would thus make it possible to reduce the distortion generated by the PIR control, which exploits the integral and proportional part in order to track harmonics at higher frequencies, compared to the fundamental, thus introducing delay in the loop. In contrast, resonant components could track higher harmonics with less distortion, further increasing the system's Power Factor.
Further control techniques could be further tested, such as the Space Vector Modulation. The latter, by implementing an implicit overmodulation technique through the presence of phase interference, could considerably reduce the distortion generated on the machine centre voltage, even at lower loads, as it does not represent a technique based on the comparison between modulating and carrier unlike the PWM control technique. On the other hand, the challenge would become more complex as both three-phase operation and overmodulation would be merged into a single control system, making it more difficult to manage them separately.
Further improvements can also be made to the simulation, e.g. by introducing additional non-idealities not taken into account at this stage of the study.

9

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