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# Characterization and optimization of a fast converter to control plasma instabilities in JT-60SA

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# Riassunto

L'obiettivo finale di questo lavoro di tesi è di studiare il comportamento di un convertitore veloce, progettato per alimentare gli avvolgimenti per il controllo dei cosiddetti Resistive Wall Modes (RWM) in JT-60SA. La macchina oggetto degli studi è stata progettata dall'azienda Equipaggiamenti Elettronici Industriali EEI s.p.a. e un suo prototipo è già stato prodotto e testato. Durante suddetti tests sono emerse varie problematiche che l'Autore ha analizzato e risolto durante il lavoro di tesi. Quindi, durante il lavoro, l'Autore ha ottenuto un buon livello di esperienza sul campo ed ha avuto la possibilità di sviluppare alcune idee e soluzioni originali, grazie anche alla solida preparazione teorica ottenuta durante gli studi universitari.

JT-60SA è una macchina per fusione nucleare dotata di magneti superconduttori, sviluppata grazie ad una collaborazione tra Europa e Giappone, che inizierà ad operare all'inizio del 2019. Uno dei suoi scopi principali è studiare la stabilizzazione attiva degli RWM. Essi sono instabilità magneto-idrodinamiche che tendono a distorcere velocemente la colonna di plasma. Tuttavia, esse possono essere rallentate, grazie a delle pareti conduttive stabilizzanti, e, quindi, controllate attivamente. Una delle possibilità di controllo è proprio quella di utilizzare delle bobine in rame stabilizzatrici: ne saranno, infatti, posti 18, 6 nella direzione toroidale per 3 in quella poloidale. Per produrre i campi necessari alla stabilizzazione sono richiesti 300 A e 240 V di picco.

Per ottenere la massima flessibilità nel controllo degli RWM, ogni avvolgimento avrà un proprio convertitore indipendente. Sono, quindi, previsti 18 convertitori monofase a quattro quadranti e ponte intero da 72 kVA ciascuno. Inoltre, essi dovranno avere una dinamica molto veloce, infatti le specifiche prevedono  $50 \mu\text{s}$  di massima latenza e 3 kHz di banda passante. Di conseguenza sono richieste alte frequenze di commutazione con modulazione unipolare, raggiungibili, nella configurazione a ponte ad H, solo grazie alle moderne tecnologie di IGBT ibridi in Carburo di Silicio (SiC), dove solo il diodo in antiparallelo è effettivamente prodotto in SiC. Grazie a ciò le perdite di commutazione vengono fortemente ridotte e si possono raggiungere 30 kHz di frequenza di commutazione, che diventano 60 kHz equivalenti sul carico. Infine, ogni convertitore sarà dotato di una scheda di controllo molto veloce, basata su DSP e FPGA. A causa della bassa impedenza di carico e delle alte frequenze di commutazione, è stato, infine, necessario introdurre un filtro in uscita di tipo LC, abbinato ad un ramo trasversale RC smorzatore.

Poiché il carico ha resistenza ed induttanza variabile con la frequenza, a causa di effetti pelle, di prossimità e schermatura, è stato necessario procedere con un'ottimizzazione del controllore PI dell'anello di corrente tramite l'uso di un modello numerico del carico. Due modelli, quindi, sono stati sviluppati: il primo, sviluppato dalla EEI, è basato sulle celle Cauer, ossia reti di dipoli RL, che ricreano con precisione l'impedenza del carico fino a frequenze superiori ai 3 kHz; il secondo, basato su un'idea dell'ing. Ferro, prevede la convoluzione tra la forzante (la tensione imposta sul carico) e la risposta impulsiva del carico (l'anti-trasformata di Fourier dell'ammettenza). Quest'ultimo modello, come mostrato dall'Autore, funziona poiché, per ogni sistema lineare tempo-invariante (LTI), una sua evoluzione particolare può essere trovata facendo la convoluzione nel tempo tra la forzante e la risposta impulsiva del sistema stesso.

Quindi, l'Autore, utilizzando come base un codice pre-esistente, ha sviluppato un codice di ottimizzazione stocastico multi-obiettivo basato sulla teoria della Particle Swarm Optimization (PSO) ed il Fronte di Pareto. Utilizzando il modello a convoluzione, la procedura di ottimizzazione ha messo in evidenza alcuni limiti del controllore PI usato. Dunque, l'Autore ha sviluppato due possibili soluzioni originali che consentono di migliorare le prestazioni dinamiche: la prima e più promettente prevede l'aggiunta di un

ulteriore ramo integrale al controllore PI, che include un certo ritardo regolabile rispetto al PI originale; la seconda è, invece, una soluzione "predittiva" basata sul modello a convoluzione, che utilizza, in realtà, la deconvoluzione. Essa cerca di ricavare la tensione necessaria a rispettare il riferimento di corrente sul carico deconvolvendo la risposta impulsiva e la tensione stessa (calcolata nei passi precedenti).

Dopodiché è stata fatta la validazione del modello a convoluzione tramite i primi test sperimentali. Due tipi di prove sono state eseguite: nella prima è stata misurata la risposta di corrente sul carico ad un gradino di tensione. Lo stesso test, con proprio lo stesso input di tensione, è stato poi replicato nel modello, ottenendo una quasi perfetta sovrapposizione dei risultati. Nella seconda prova, invece, è stata fatta una caratterizzazione in frequenza del controllo di corrente e i risultati ottenuti hanno evidenziato una buona sovrapposizione con il modello per frequenze fino ad oltre 1 kHz.

Fatto ciò, si è passati all'analisi degli overshoot di tensione dovuti alla dinamica del filtro d'uscita, i quali possono raggiungere picchi di 550 V. Una volta replicato il fenomeno sul prototipo, l'Autore ha eseguito degli studi per modifiche del filtro che permettessero di ridurre il picco di tensione, sviluppando una soluzione originale al problema, basata su un ramo risonante posto al posto del ramo RC smorzatore. Questa nuova topologia, inoltre ha permesso una buona riduzione delle derivate di tensione sul carico.

Inoltre è stata approntata un'approfondita analisi del sistema di correzione dei tempi morti (Dead Times, DT). Ciò ha portato allo sviluppo da parte dell'Autore di un modello che è riuscito a ricreare con sufficiente precisione delle anomale oscillazioni di corrente, le quali erano state effettivamente misurate durante i tests. Grazie a questo lavoro, l'Autore è riuscito ad identificare dettagliatamente la dinamica e la causa delle suddette oscillazioni ed, inoltre, ha elaborato delle possibili soluzioni al problema.

L'ultima parte del lavoro è consistita nella caratterizzazione di alcune anomale oscillazioni di tensione, osservate soprattutto ad alte correnti (300 A) e basse frequenze (100 Hz). Dopo vari test sperimentali, è risultato che queste oscillazioni sono dovute a brevi, ma comunque dannosi, cortocircuiti in una gamba del ponte ad H. L'Autore, analizzando i dati ottenuti, ha quindi cercato di chiarirne le cause, escludendo eventuali effetti parassiti.



# Abstract

The final and primary aim of this work is to study the behavior of a fast mono-phase converter, designed to feed the Resistive Wall Modes Control Coils (RWM-CC) in JT-60SA, and, eventually, to find possible solutions to the main issues that came out during initial testing of its prototype. The main points to be investigated were: the optimization of the frequency response of the current closed loop control, current oscillations due to a voltage errors compensation algorithm, high voltage overshoots and derivatives on the load due to the output filter behavior and, lastly, some anomalous voltage oscillations. With this aim, a deep analysis of a the system has been pursued with the help of advanced numerical models and tools. Then, the obtained model results were tested experimentally on the real prototype. Thank to this procedure, the Author slightly improved the frequency response with a controller modification, based on a original idea. Then, he understood the causes of the current and voltage oscillations problems. Lastly, the Author found a possible solution to improve the filter behavior. Therefore, during this work, the Author gained a certain level of experience on complex system analysis and debugging. Then, he managed, thanks to his theoretical framework obtained during his University studies, to develop some valid and original solutions to such problems, as will be further explained in the subsequent paragraphs.



# Chapter 1

## JT-60SA

### 1.1 Introduction

JT-60SA, (Fig. 1.1 <sup>1</sup>), is a new superconducting tokamak that is being built in Naka, Japan and it will start to operate in 2019. It is a combined project of the JA-EU Satellite Tokamak Programme, that will support the exploitation of ITER and research towards DEMO [1, 2].

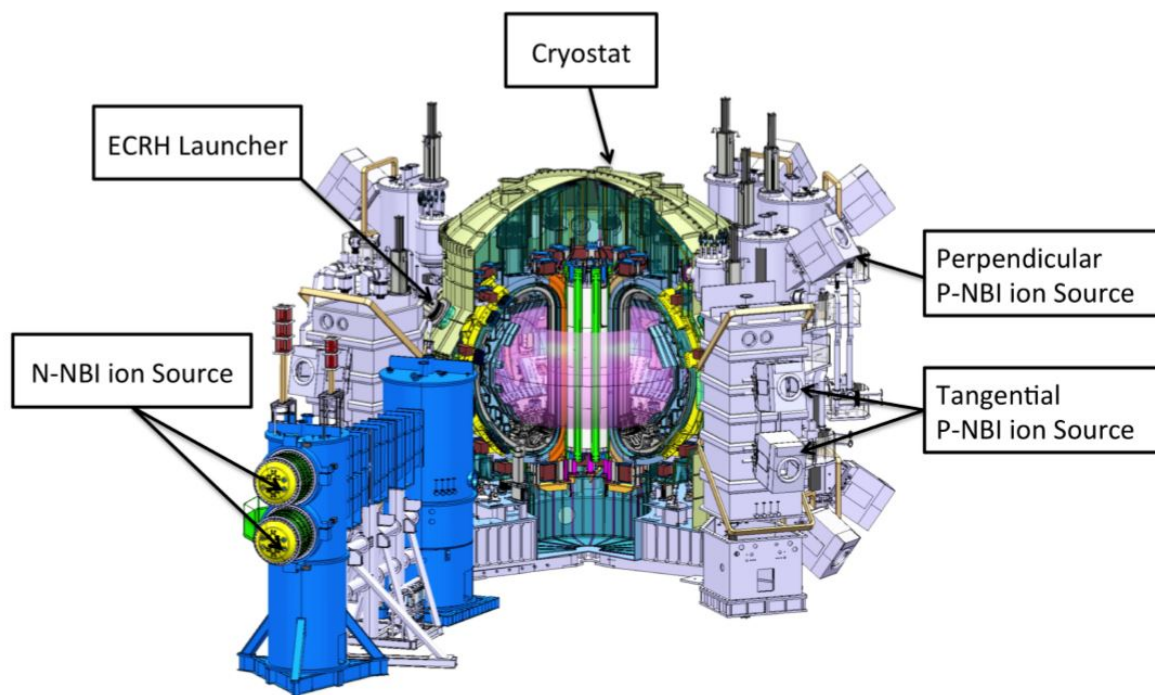


Figure 1.1: An overview of the tokamak JT-60SA.

Its main aim is to study:

1. Operation regimes;
2. MHD stability and control;
3. Transport and confinement;
4. High energy particle behavior;

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<sup>1</sup>All the figures in this chapter are taken from [1]

5. Pedestal and edge physics;
6. Divertor and plasma-wall interaction;
7. Fusion engineering;
8. Theoretical model and simulation codes validation.

One of the most important goal is to contribute to a practically acceptable DEMO plasma design. In-fact one of the most important feature of JT60-SA will be its steady-state regime performance and its real time control capability.

## 1.2 JT-60SA main parameters

JT-60SA is expected to produce a break-even equivalent class high temperature deuterium plasma and to maintain it for a typical time of 100s. The plasma will have a maximum current  $I_p = 5.5$  MA with high density of the order of  $10^{20} \text{ m}^{-3}$ .

To achieve these results, the machine will have a plasma volume of 120-130  $\text{m}^3$  contained in a torus with a major radius of 2.95 m and a minor one of 1.15 m circa. The plasma will be confined by a toroidal magnetic field of about 2.2-2.3 T.

The plasma will be heated by both positive (24 MW) and negative (10 MW) neutral beam injectors (NBI) and by electron cyclotron resonance heating (ECRH, 110 GHz and 138 GHz, 7 MW total), producing up to 41 MW of total input power.

Another important component of the tokamak is the divertor. The JT60-SA divertor has to handle up to 15 MW/ $\text{m}^2$  for the entire plasma pulse length.

The active feedback control system will include:

- two independently controllable coils for position control: Fast Plasma Position Control Coils (FP-PCC);
- 18 Resistive Wall Mode Control Coils (RWM-CC);
- 18 Error Field Control Coils (EFCC);
- high power heating, current-drive and momentum-input systems.

All these systems are coupled with 26 plasma diagnostics with high spacial and time resolution, needed not only by the control system, but also for conducting all the physics research.

## 1.3 Magnet systems

**Toroidal Field coils.** These are 18 NbTi superconducting coils cooled by supercritical Helium at 4.4 K. They will produce a 5.65 T B-field at the conductor surface, while absorbing 25.7 kA.

**Central Solenoid System (CS).** It uses a  $\text{Nb}_3\text{Sn}$  superconductor, always cooled at 4.4 K by supercritical Helium. They will sustain a maximum coil current of 11 MAturns while having an operating current of 20 kA and a nominal peak B-field of 8.9 T. The CS system will be composed by 4 modules with a total number of turns of 549.

**Equilibrium Field coils (EF).** Located, as shown in Fig. 1.2, just outside the TF coils, they will be composed of NbTi superconductors and they will be rated for 20 kA nominal current. They will produce peak B-field between 4.8 and 6.2 T, depending on their position. In total there will be 6 EF coils.

**Fast Plasma Position Control coils (FPPCC).** This system is composed by two copper coil sets that provide independent control of vertical and horizontal fields. They will sustain 80 kAturns for each set, but the number of turns has not yet been specified.

**Error Field Correction coils (EFCC).** There will be 18 coils: 6 will form the upper coil set, 6

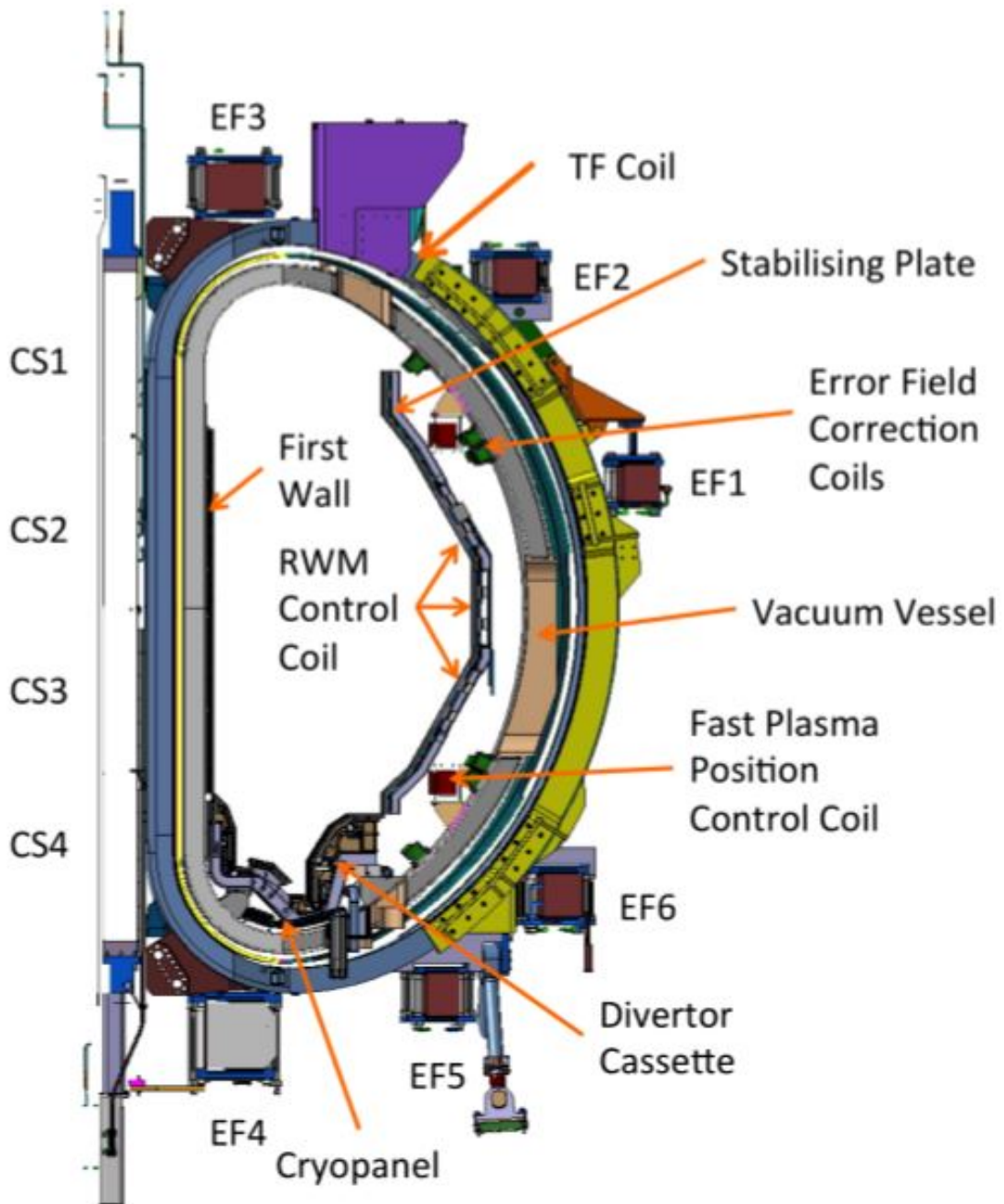


Figure 1.2: The JT-60SA magnet system.

the lower set and the last 6 the middle set. Each coil will be rated for 30 kAturns, with 35 turns per coil.

**RWM Control coils (RWM-CC).** These are 18 coils divided in 6 groups, distributed symmetrically along the toroidal direction, each group being composed of 3 coils along the poloidal one. Each coil will have 8 turns, leading to a 2.2 kAturns current. FPPCC, EFCC and RWM-CC are positioned as shown in Fig. 1.2 and 1.3.

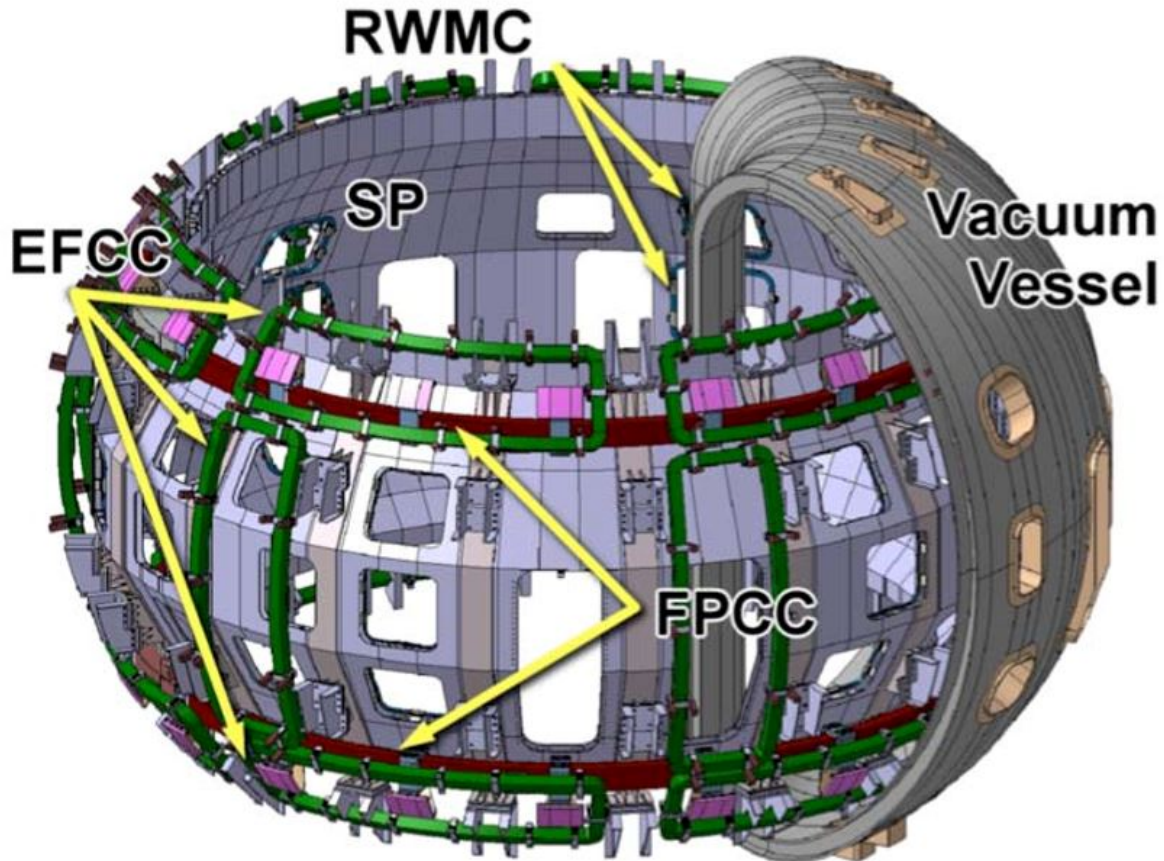


Figure 1.3: Layout of JT-60SA EFCC, RWM-CC, FPPCC and stabilizing plate.

## 1.4 Heating systems

JT-60SA will have both ECRH and NBI plasma heating systems, with a total peak requested power from the power supplies (PS) of 128 MW.

**ECRH system.** This system, pictured in Fig. 1.4, is mainly composed by: high voltage PS, high power gyrotron sets, transmission lines and launcher (antenna) systems. In the initial research phase there will be two sets that will inject 3 MW of heating power for less than 5 s in order to help the plasma start-up, then there will be other two sets that will inject 1.5 MW for all the plasma pulse duration (100 s). During the subsequent integrated research phase, other 5 sets will be added, taking the final input power up to 7 MW. All the sets will work at 110 GHz gyrotron frequency, but also a dual frequency gyrotron at 138 GHz is under intensive R&D.

**NBI system.** During the extended research phase, the injected power will be 34 MW for 100 s. Before it will be 20 MW and 30 MW for the integrated research phase I and II. There will be 12 positive-ion-based NBI (P-NBI) at 2 MW each and one negative-ion-based NBI (N-NBI) rated at 10 MW. All the NBI

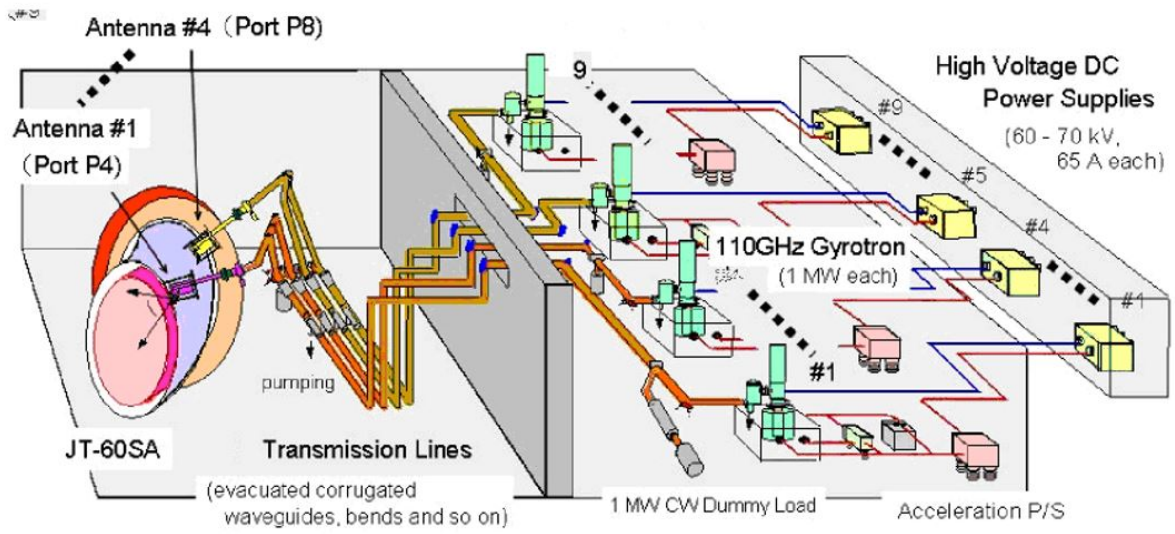


Figure 1.4: A schematic view of th ECRF heating systems.

systems will be an upgraded version of the ones used by JT-60U, where the main upgrade will be made on the PS systems and, only on the N-NBI, on the voltage handling capability.

## 1.5 Electric systems

**Pulsed power electrical network.** The pulsed loads, as displayed in Fig. 1.5, will be fed by the 275kV commercial power grid. The voltage will be lowered by step-down transformer. The ECRH heating system will be directly fed by a 275/18 kV transformer, while the other system (NBI,PF and TF coils) will have a first step-down to 66 kV and then three different transformers will bring the voltage to 11 kV. In addition, two motor generator will be connected to the 11 kV stage: the T-MG will be a 215 MVA synchronous machine that will provide the requested active and reactive power to one of the P-NBI and to the N-NBI, while the H-MG will be a 400 MVA synchronous machine, driven also by an induction machine, and it will feed the last P-NBI, all the PF coils and the fast plasma position control coils (FPPCC).

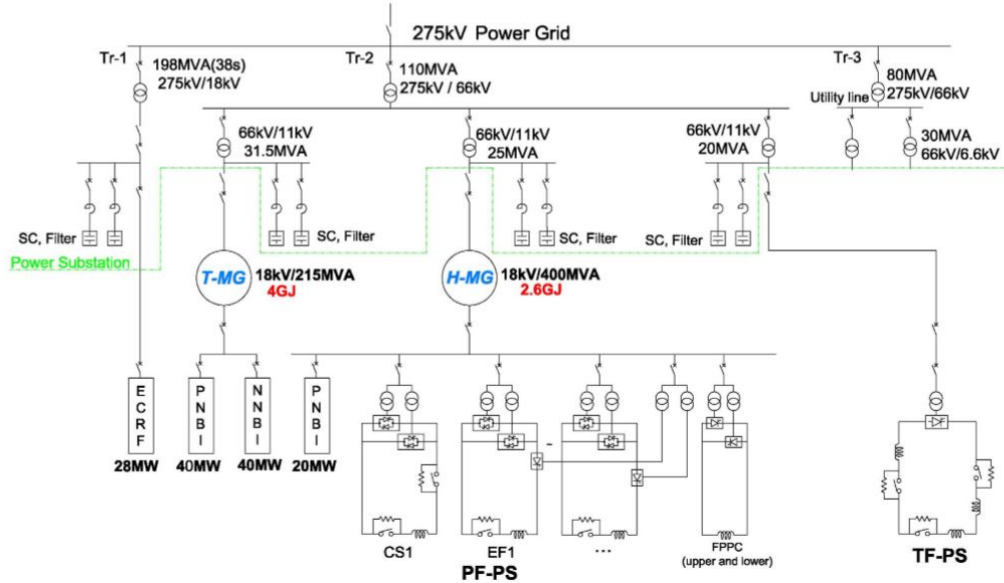


Figure 1.5: The JT-60SA pulsed power electrical network.

**TF coils power supply.** These coils will be fed by a water cooled two quadrants AC/DC thyristor converter, that will feed the 25.7 kA DC current continuously. The converter AC stage will be connected to a dedicated 11 kV line. Finally, the converter will be able to charge and discharge the full magnet current in about 25 minutes, operations that will be made only once a day. The TF PS circuit is shown in Fig. 1.6.

**PF coils power supplies.** There will be three series-connected basic components for each PF system: a "Base power supply (PS)", a "Booster PS" or a Switching Network Unit (SNU) and a quench protection circuit (QPC). Each CS module will have a separate PS that will feed the module with the requested 20 kA. The EF coils will also feature separate PS for each coil, also because EF1, EF2, EF5 and EF6 will have asymmetric current ratings (-20 kA to 10 kA), due to expected operational space. The SNU will be used to induce high plasma voltage to obtain its break-down. It will consist of a DC current interrupter and a tunable resistor added into each CS PS and EF3 and EF4 PS. The PF and EF circuits are displayed in Fig. 1.7.

**Quench protection circuit (QPC).** In case of superconducting coil quench or a failure inside the PS, a system that can extract rapidly all the magnet stored energy is required in order to protect the coils and shut-down the plasma operation. The QPC is composed by a DC current interrupter, a current dump resistor and a pyro-breaker. In particular, the DC interrupter is composed by both a mechanical switch and a static one: the first conduct the continuous current, while the other is needed for circuit interruption.

**FPPC coils power supply.** These copper coils will have the function of control vertical and hori-



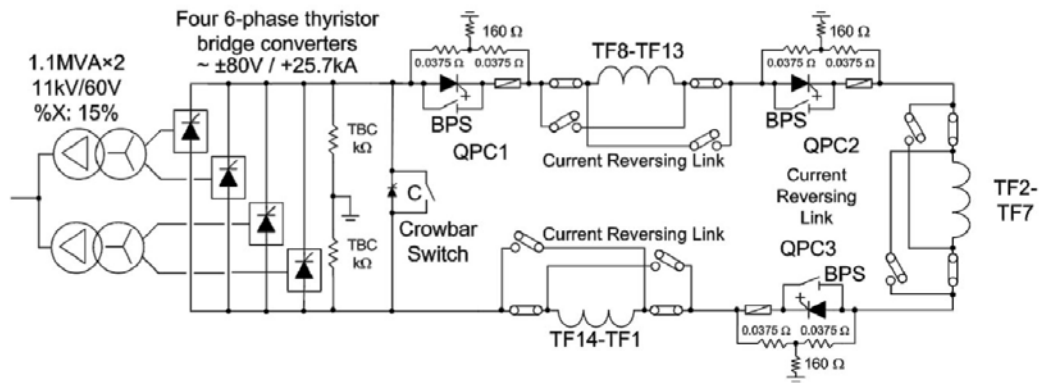


Figure 1.6: The JT-60SA TF power supply circuit.

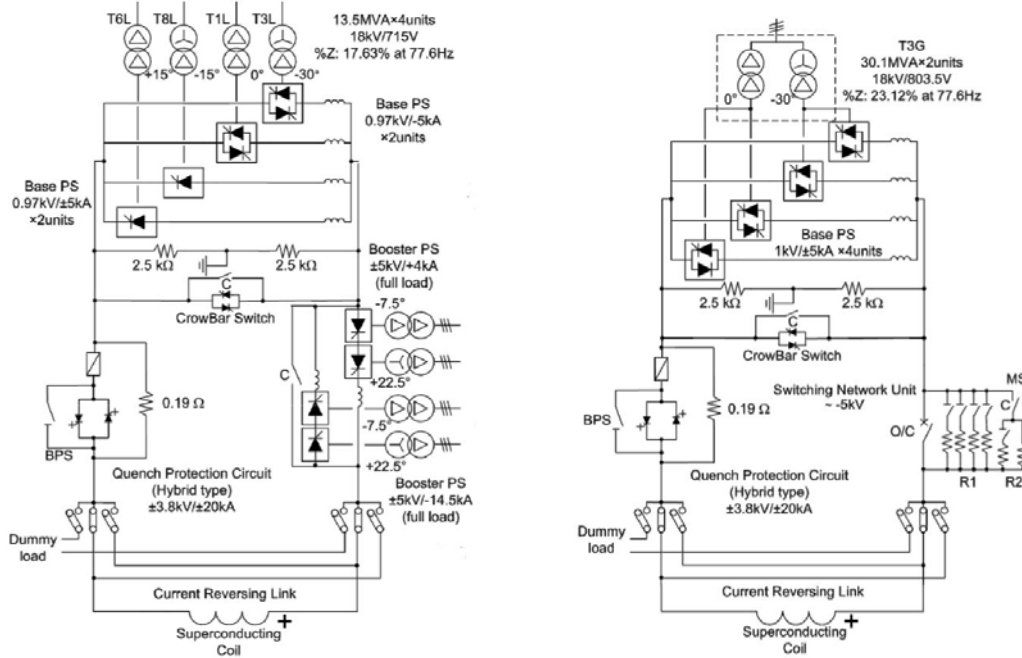


Figure 1.7: The JT-60SA EF (left) and CS (right) power supply.

zontal position of the plasma against small perturbation. The PS will consist of a 4 quadrant thyristor converter for each coil with small delay time .

**RWM control coils power supply (RWM-PS).** It consist of 18 independents voltage source converters, rated for  $\pm 300$  A and  $\pm 240$  V with low latency and fast current dynamics.

**Error Field correction coils power supply.** It has been proposed to use multi-phase PWM inverters, but the case is currently under study.

## 1.6 Supervisory control system and data acquisition system

The Supervisory control system and data acquisition system (SCSDAS) has the following roles:

1. plant monitoring and machine state management;
2. discharge sequence management;
3. real-time plasma control;
4. device protection and human safety;
5. discharge result data management;
6. remote experimentation.

The discharge sequence can be divided, as in Fig. 1.8, in three main time steps:

1. discharge preparation period;
2. plasma discharge period;
3. discharge completion period;

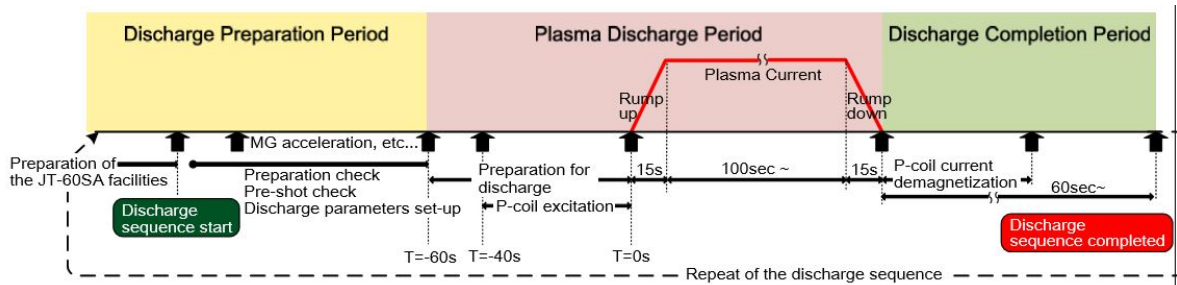


Figure 1.8: The main time steps of the discharge sequence.

During the first phase SCSDAS collects, and in case edits all the discharge condition data and feeds the compiled results to each sub-system. Then it performs a sub-systems condition check.

After all, SCSDAS starts the discharge period: firstly it controls the magnetization of all the PF coils (the TF ones are magnetized only once a day) and it will take up to 60 s, then there will be the plasma current rump-up (15 s), followed by the steady-state operation (up to 100 s), at the end of this there will be the plasma current rump down period (about 15 s).

Then the last phase begins the discharge completion period. During this step SCSDAS commands the PF coils demagnetization and saves all the experimental data.

In addition, during the plasma discharge period the real-time control system takes a primary role. It makes the reconstruction of the plasma shape from magnetic sensor data, calculates the coil currents/voltages necessary to keep the plasma in the reference shapes, generates the control commands for all the actuators. Critical to the operation of the real-time control is the data exchange between all the subsystems: this will be managed by a reflective memory network, that will distribute all the commands, actuator status, measured and processed data.

The real-time control system will have a main control cycle duration of about 10 ms.

## 1.7 Research phases

Three main research phases are foreseen for JT-60SA:

1. initial research;
2. integrated research;
3. extended research.

**Initial research phase.** Firstly only hydrogen plasmas will be produced, as needed to prepare deuterium operations and for the integrated commissioning of the machine. Then there will be the deuterium phase, in which neutron production, nuclear heating and radiation safety will be commissioned. This will lead to the characterization of operational boundaries and experimental flexibilities, by producing only relatively short pulse discharges. The injected heating power will be 10 MW from N-NBI, 20 MW from P-NBI and max 3 MW from ECRF at 110-138 GHz.

**Integrated research phase.** In this phase long plasma pulses of up to 100s will be finally produced. Due to the higher neutron production (up to  $10^{21}$  neutrons/year), the remote handling system must have completed its commissioning before this phase. The total NB injected power will be 20 MW for 100 s or 30 MW for 60 s, while the ECRF injected power will be increased to 7 MW for 100 s. Also, the divertor will work at its nominal full load of 15 MW/m<sup>2</sup>.

**Extended research phase.** In this phase the heating power will be increased to 41 MW, but this is currently under investigation. Also, the divertor will be upgraded to a metallic one with an advanced shape, based on the progress of tokamak research worldwide.

So, JT-60SA will, hopefully, produce its first plasma in the first half of 2019. Then, as shown in Fig.1.9, every single research phase will last about 2 to 3 years, so that the integrated research phase will end somewhere between 2027 and 2030.

It is to be noted how JT-60SA will start its operations well before ITER, which will produce its first hydrogen plasma maybe in 2025 (the ITER schedule is presently under review). In addition, the ITER Q=10 long pulse D-T operation will not start before 2035, because it requires sufficient exploration of the key physics issues and operational techniques in satellite devices, such as JT-60SA.



Figure 1.9: The two possible time schedules for JT-60SA exploitation.



## Chapter 2

# The Resistive Wall Mode control in JT-60SA

### 2.1 Introduction

Resistive Wall Modes (RWM) are magneto-hydro-dynamic (MHD) instabilities that arise from the interaction between plasma and the mechanical boundaries, i.e. the first wall. Because these structures are usually made with conductive materials, plasma current or B-field variations could induce asymmetrical eddy currents inside them, with a pattern similar to the one shown in Fig. 2.1. As is it well known, each induced current in turn will create a counter-induced magnetic field that will oppose the variation in the inducing field. This effect, then, will highly reduce the growing rate of external kink modes, i.e. the expansion of the external magnetic field towards the confinement wall. Being these structures resistive, this expansion is not stopped, but only slowed down, making RWM an unstable mode.

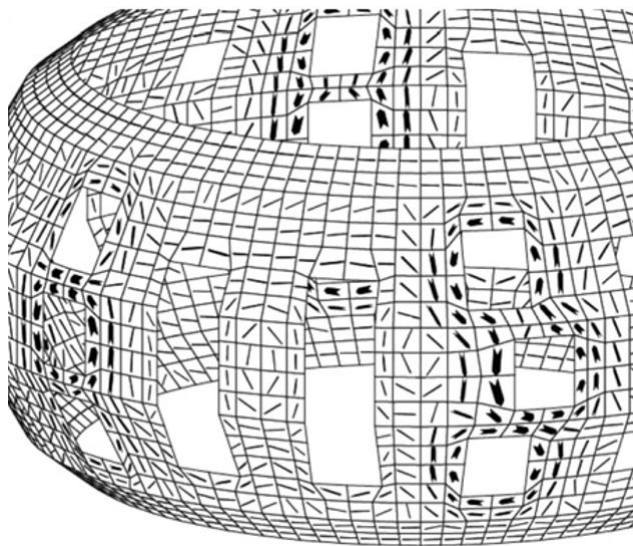


Figure 2.1: Eddy-current pattern on the stabilizing plate of JT-60SA [3].

RWMs occur especially at high-pressure ( $\beta_N$ ) plasmas. Therefore RWMs set, also, a limit on the achievable  $\beta_N$  in tokamak advanced scenarios.

## 2.2 Control of RWM

**Ideal wall.** One theoretical possibility, that should control RWM, is to have a perfectly conducting wall near the plasma boundary. In-fact the penetration of the B-field variation is fully stopped by the skin effect of an ideal conductive material and so the mode cannot expand. Obviously this is unfeasible and other control techniques have to be implemented.

**Stabilizing plate (SP).** While a superconducting wall is not feasible, it is possible, however, to place inside the vacuum vessel a conducting wall: the so called stabilizing plate. It cannot totally contain the B-field expansions, but, at least, it can slow them down to acceptable grow rate, making them much easily controllable. In JT-60SA, the SP, made of SS316LI, will be covered with composite carbon fiber (CFC), positioned over copper heat sinks, that are water cooled. So, the SP can slow down the growth time till 1 to 10 ms, making possible to control RWMs through active feedback control.

**Active control.** The active control, typically, needs a set of coil, positioned near the plasma, each one controlled independently by its own PS. JT-60SA, in-fact, will feature 18 RWM copper control coils (RWM-CC0), distributed symmetrically along the torus [1, 2]. The feed-back system needs pick-up coils in order to detect the magnetic flux. The MHD controller will take the feed-back signal from the sensors and then calculates in real-time the current that the correction coil must apply in order to suppress the kink expansion. Simulations, made with VALEN code [4], show that in JT-60SA the active control allows achieving a  $\beta$  limit near to the ideal-wall  $\beta$ . By the way, a strong coupling between plasma and coils is needed in order to obtain higher control efficiency, i.e. to minimize the current required to effectively suppress RWMs.

**Plasma rotation.** In DEMO, due to the high neutron production, it is not convenient to put coils inside the vacuum vessel, such as RWMCC. So, another control technique has been developed: rotational stabilization. In-fact, a rotational plasma can increase the shielding effectiveness of the SP. Typically, a toroidal plasma rotation of the first spatial harmonic is induced thanks to the NBIs and a 100 krad/s pulsation is reached [5]. This translates to an equivalent frequency of the B-field seen by the SP of 15 kHz. Hypothesizing that the SP is only made of copper, a 0.5 mm of depth of penetration is obtained. This method will be further tested in JT-60SA.

## 2.3 Coils design and characterization

At the present configuration of the system each coil will be placed on the inner side of the stabilizing plate (SP), as pictured in Fig. 2.2, so that each coil will require only 2.2 kAturns maximum because they will be close to the plasma and far less shielded by the SP. Each coil will have 8 turns, leading to a total absorbed current of 275 A. The square conductors will be disposed on 2 layers, each one containing 4 turns. They will be made of copper and they will be water cooled [6]. The insulator will be organic and must withstands the high temperatures. The coil will have a mean dimension of its sides of 0.85 m [7]. The coil can be seen as an ohmic-inductive load, in which the resistance and the inductance vary with frequency. In particular, the resistance increases with frequency due to skin and proximity effects, but also due to eddy current in passive surrounding structures. Instead, the inductance decreases with frequency due to the shielding effects. The coils will be connected to the respective power supply with coaxial cables (max length 88 m) and vacuum feeders (across and inside the vacuum vessel). The impedance of the load (including also cable and feeder) is shown in Table 2.1. The estimation has been obtained with FEM analysis (for coils and feeders) and from data-sheet (for cable).

As it can be noted, the load impedance is low. This is critical for the current ripple and control. In-fact with low impedance loads, the current tends to go out of control easily.

## 2.4 Cables

The converter is connected to the RWM-CC using a single coaxial cable, that is seen from the converter itself as part of the load. In order to minimize the voltage drop on the cable a  $100\text{mm}^2$  will be adopted. The length of the cable will be between 55 to 88m [9], different for each RWM-CC.

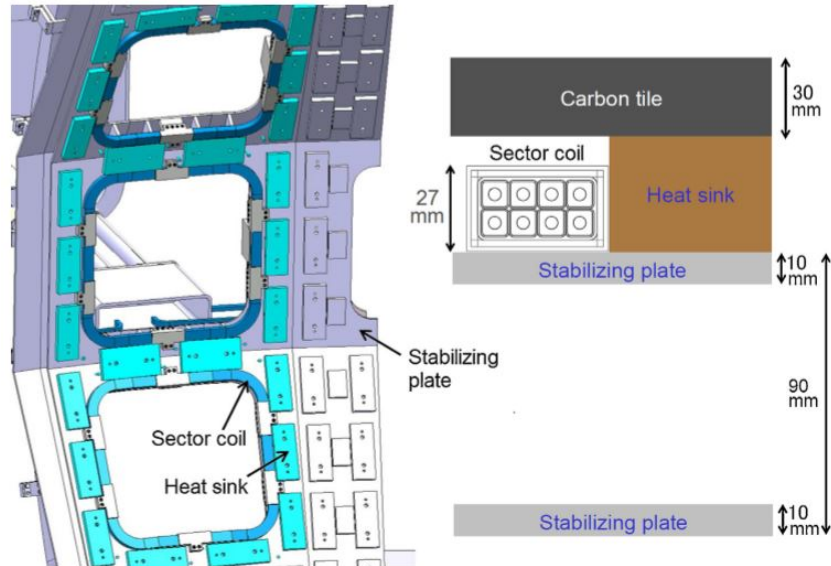


Figure 2.2: The design of RWM-CC of JT-60SA [8].

Freq [Hz]	R [m $\Omega$ ]	L [ $\mu$ H]	Impedance [m $\Omega$ ]	Phase [degrees]
1	52.6	143	52.6	1.0
3	52.7	143	52.8	2.9
10	53.3	140	54.0	9.4
30	56.6	130	61.7	23.4
100	72.4	107	98.8	42.9
300	117	80.2	191	52.3
1000	221	50.7	388	55.2
3000	397	35.1	772	59.0
10000	824	22.7	1650	60.0

Table 2.1: RWMCC system main characteristics.

The main characteristics of the coaxial cable are listed in Table 2.2, while the estimated resistance and inductance as a function of frequency are listed in Table 2.3, considering the maximum length of 88m [10].

Parameters	Values
Rated Voltage	600v
Rated Current	320A at 1kHz 295A at 5kHz 165A at 10kHz
Cross-section (for conductor)	100mm <sup>2</sup>
Outside diameter (for conductor)	15.4mm
Insulator thickness	2.0mm
Sheath thickness	30mm
Outside diameter (for cable)	30mm
Approximate wight	2200 kg/km
Test voltage	AC3000V, 1 min

Table 2.2: Main characteristics of the cable.

Frequency (Hz)	AC loop resistance ( $\Omega$ /km) at 90°C	Inductance (mH/km)	Impedance ( $\Omega$ /km)
1	0.476	0.1143	0.476
3	0.476	0.1143	0.476
10	0.476	0.1143	0.476
30	0.476	0.1143	0.476
100	0.476	0.1143	0.481
300	0.476	0.1143	0.523
1000	0.460	0.0957	0.757
3000	0.486	0.0824	1.63
10000	0.670	0.0721	4.58

Table 2.3: Frequency characterization of the cable.

## 2.5 PS and control main requirements

RWM will be controlled at frequencies up to 1 kHz [4], so the 3dB bandwidth of the control system has to be at least 3 kHz. Also, the system will have a very low allowable latency, less than 50  $\mu$ s. The 1 kHz limit is given by the need not to increase excessively the mode exponential growth, so that the required current is limited too. At that frequencies, the induced field is not so shielded by the surrounding structures, thanks to the position of the RWM-CC, towards the plasma.

Considering that 275 A are required in order to produce the stabilizing magnetic field and considering a certain margin, the PS should be able to feed the coil with a 300 A current. By the way, at 3 kHz there is a 3 dB attenuation, resulting in a 212.4 A peak current. In order to achieve this current value at 3 kHz, taking the load impedance, the voltage requested is 226 V. So, considering some voltage attenuation and physics uncertainties, the inverter should be rated for 240 V [6].

## 2.6 Plasma induced back-EMF

Then, we have to take in account the possible back-electromotive force (back-EMF) induced on the load by plasma current variation. The worst scenarios are plasma disruptions and vertical displacement events (VDE) happening when the plasma initially has the nominal current of 5.5 MA and with the minimum current decay time during disruptions of 4 ms. Simulations gave a resulting induced voltage, as shown in Fig. 2.3. With some margin,  $\pm 170$  V for 15 ms has been considered for the design of the system. When this back-EMF appears, the fast converter has to limit the possible consequent over-current below



30% of 300 A: this requires applying in few  $\mu\text{s}$  a counter voltage higher than the induced one, through a dedicated fast over-current protection [6].

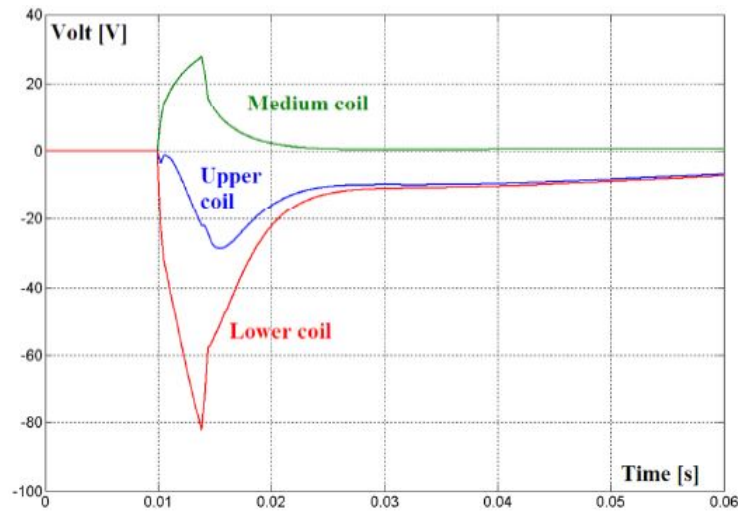


Figure 2.3: Induced voltage in the sector coils during plasma disruption [6].

Table 2.4 summarizes the main specifications of the fast converters for RWM control [9].

Description	Value
Nominal output voltage at the inverter output terminals	240V
Maximum peak of a sinusoidal output current	300A, continuously
Nominal output current in dc operation	>100A
Maximum output current ripple	$\pm 30\text{A}$
Max. pulsed voltage induced into the load	$\pm 170\text{V}$ for 15 ms
Bandwidth of the current at -3 dB (with current control loop)	3kHz
Maximum operation duty	100s/1800s
Maximum latency (between step reference and output voltage change)	50 $\mu\text{s}$
Type of reference	Arbitrary, range $\pm 100\%$
Accuracy of the load current in steady-state, up to 100 Hz	$\pm 2\%$ of full scale
Max. voltage/current overshoot with step variation of the reference	$\pm 15\%$
Max. current overshoot during induced voltage pulse	$\pm 30\%$
Dc-link operational range	50 $\div$ 100%
Maximum dc-link voltage variations in normal transient conditions	-15% $\div$ +10%
Dc-link overcurrent during induced voltage pulse	+30%
Max ambient temperature	40°C
Max instantaneous differential voltage at the coil terminals	$\pm 550\text{V}$
Max $dV/dt$ at the coil terminals	<20 MV/s

Table 2.4: Main specifications of the fast converters for RWM control.



## Chapter 3

# RWM power supply

### 3.1 Introduction

The RWM-PS system is now under construction and it will be delivered in 2018. The system will be provided by EEI Equipaggiamenti Elettronici Industriali S.p.a.

Every RWM-CC will be fed by its own four quadrant converter (full H-bridge topology). All the 18 fast converters are then connected to the same DC-link, as shown in Fig. 3.1, which will be supplied by a single three-phase AC/DC thyristor converter. This converter will be lastly connected to a step-down 50 Hz transformer. The transformer will be a 6.6kV/290V Dyn11, rated for 100 kVA nominal continuous power and a 200 kVA peak power (at least maintained for 100 s) [9]. The 6.6 kV three phase line will be provided by the existing electrical network in Naka.

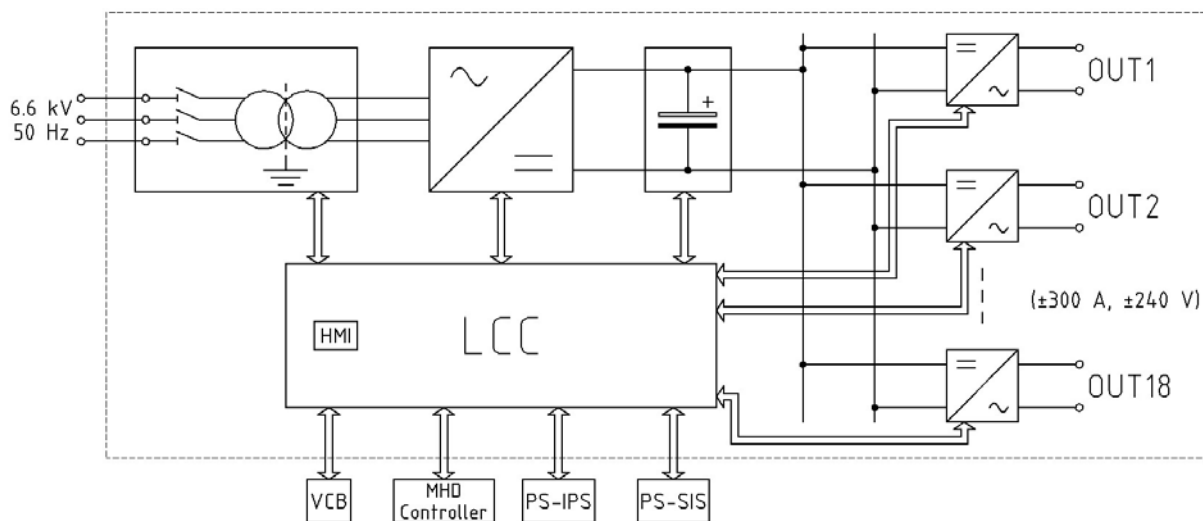


Figure 3.1: Overview of the overall RWM-PS electrical scheme (courtesy of EEI).

Note that the 290 V secondary voltage is due to the DC-link chosen voltage, rated for 300 V. Furthermore, upstream the transformer there will be a manually-operated AC disconnector, provided by EEI, and a vacuum circuit breaker, provided by the customer.

### 3.2 AC/DC front-end

The aim of the AC/DC front-end is to convert the 290 V three phase AC voltage to a 300 V DC one. This will be made with a full bridge rectifier that, also, will have the capability to compensate voltage fluctuations within  $\pm 10\%$  of the nominal voltage. Because the energy regeneration towards the AC grid is

not requested, a thyristor based converter has been chosen, as the most economical and simple solution. Due to the needed 670A DC-current and 550 A AC-current, the rectifier topology will be the 6-pulse one, with 2 thyristor per branch, as pictured in Fig. 3.2. A smoothing choke will be placed at the converter downstream.

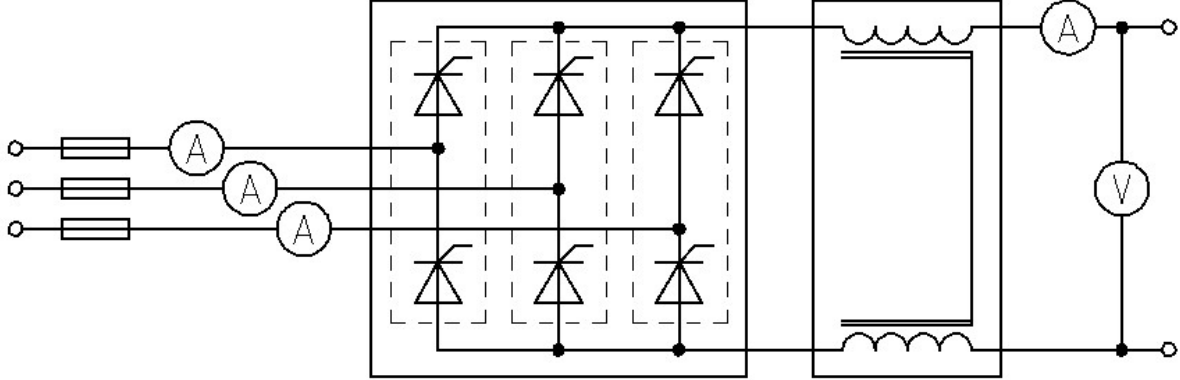


Figure 3.2: The AC/DC converter topology (courtesy of EEI).

The main specifications of the rectifier are listed in Table 3.1.

Description	Value
Nominal AC voltage (RMS)	290 V
Nominal DC voltage	300 V
Nominal AC current (RMS)	670 A
Nominal DC current	550A
Output power	200 kW
Range of operation of the voltage reference	$60 \div 100\%$ of $V_{DC,n}$
Maximum error between average dc-link voltage and reference voltage	$\pm 3\%$
Maximum rise time	5 s
Maximum dc-link voltage variations in normal transient conditions	$-15\% \div +10\%$
Maximum dc-link overvoltage in case of pulsed electromotive force induced into the load	$+20\%$

Table 3.1: Main specifications of the rectifier.

### 3.3 DC-link nominal voltage

The nominal DC-link voltage ( $V_{DC,n}$ ) has to be chosen so that at 85% of  $V_{DC,n}$ , the required current control bandwidth (-3 dB at 3 kHz) can still be achieved. Knowing that the load impedance at 3 kHz is 397 m $\Omega$  and 35.1  $\mu$ H with 212.4 A<sub>pk</sub> (considering also the attenuation), the load peak voltage is 163.4 V. Then, adding the voltage drops on the output filter and on the fast converter switches (around 4V), it results a minimum DC-link voltage of 261V. So, taking some margin, the nominal DC-link voltage is set to 300 V by EEI [9].

### 3.4 DC-link capacitor bank

The capacitor bank is needed to aid the rectifier to regulate the DC-link voltage. Because the most demanding design criteria is the maximum DC-link over-voltage (20%) during plasma induced back-EMF, it has been identified the maximum energy fed back to the DC-link. This happens when each of the 18 inverters are feeding their RWMCC with the nominal 300A current and then a 170V back-EMF voltage appears on the load. So a  $170 \cdot 300 \cdot 18 = 918$  kW of power is fed back for 15ms, leading to a energy of 13.5kJ.

Imposing that all this energy goes in the capacitors, then a 0.68F total capacitance is required in order to

limit the over-voltage within the  $\pm 20\%$  of 300V. In the end, considering a certain margin, a 1F electrolytic capacitor bank has been chosen by EEI [9].

### **3.5 Fast converter**

Downstream the capacitor bank there is, finally, the fast converter. It is basically composed by 3 stages: input filter, H-bridge, output filter. It will be discussed in the next chapters.



# Chapter 4

## The dummy load

### 4.1 Introduction

Because the real load to which the converter will be connected is not available yet, in order to test the prototype, a dummy load (DL) was provided by OST with a frequency characteristic as far as possible similar to the real one. In particular it is important that the dummy load will have the same impedance of the real one at 1 kHz and 3 kHz.

### 4.2 Dummy load characterization

The dummy load is made of a massive copper coil, without any ferromagnetic core, that is wrapped around a stainless steel cylinder. The cylinder is necessary in order to reproduce the impedance characteristic of the real RWM-CC as function of frequency. By the way, the coil itself didn't match the requested specification so three series inductances have been added downstream the dummy load, that have 16.9  $\mu\text{H}$  and 3.5 m $\Omega$ .

So, the final characteristic is as illustrated in the subsequent Table 4.1 and graphs in Fig. 4.1 and 4.2. However the resistance and phase at 1 kHz are different from the real RWM-CC, so its current response at those frequencies is different in CCM.

Frequency [Hz]	R dummy [ $\Omega$ ]	L dummy [ $\mu\text{H}$ ]	Impedance [ $\Omega$ ]	Phase [ $^\circ$ ]
1	2.69E-02	167.1	2.69E-02	2.2
10	2.69E-02	167.0	2.89E-02	21.3
30	2.85E-02	168.0	4.26E-02	48.0
100	4.6E-02	162.0	1.12E-01	65.7
300	0.144	122.8	2.73E-01	58.0
1000	0.3167	56.7	4.77E-01	48.4
3000	0.3728	40.0	8.41E-01	63.7
10000	0.459	36.9	2.37	78.9
20000	0.596	35.9	4.56	82.48
30000	0.751	35.2	6.68	83.55
40000	0.891	34.7	8.78	84.17
50000	1.00	34.3	10.83	84.69
60000	1.11	34.1	12.92	85.07
70000	1.20	33.8	14.93	85.38
80000	1.29	33.6	16.96	85.65
90000	1.36	33.5	19.02	85.89
100000	1.43	33.4	21.06	86.11

Table 4.1: The measured R and L with the addition of the external inductance.

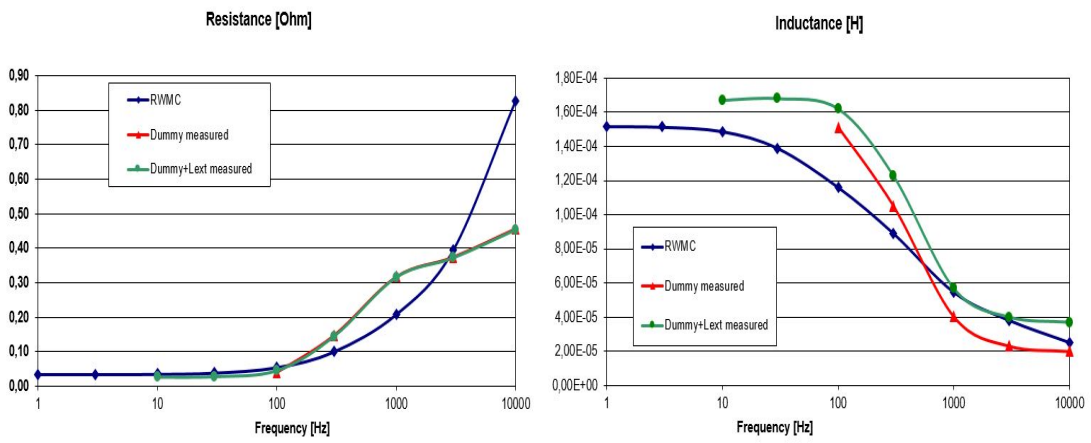


Figure 4.1: The DL resistance and inductance.

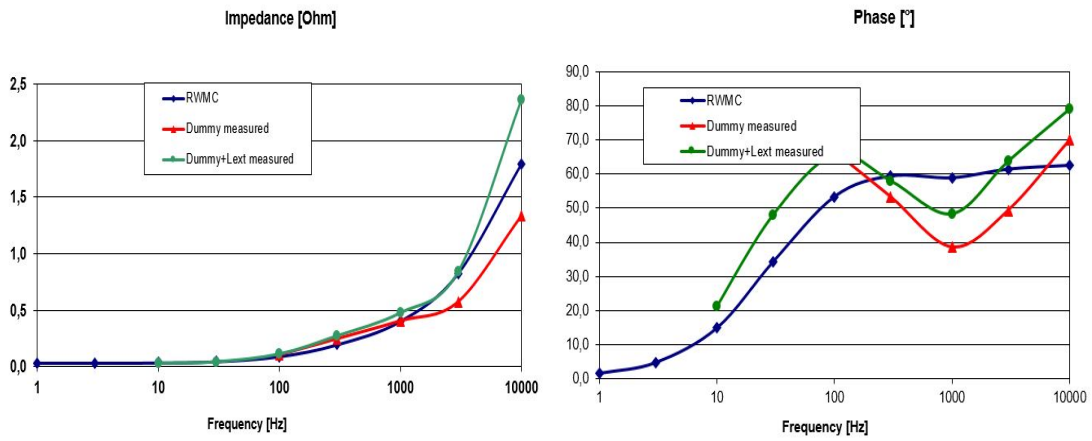


Figure 4.2: The DL impedance and phase.



Figure 4.3: The dummy load.



# Chapter 5

## The fast converter

### 5.1 Introduction

The RWM-PS system will include 18 identical four quadrant fast converters. The topology is the one shown in Fig.5.2. Each converter will have its own control board. A PWM unipolar modulation is adopted, due to its capability to double the output frequency.

Furthermore, a prototype has been built in order to verify the feasibility of the dynamic requirements by using commercially available components with reasonable prices.

### 5.2 Power semiconductors

Considering the 3 kHz bandwidth, an output frequency between 40 to 60 kHz is needed, that means a switching frequency of 20 to 30 kHz, too high for Si-based IGBT modules, using the H-bridge topology. Anyway, such frequencies can be achieved with hybrid Si-SiC IGBTs modules, where only the anti-parallel diodes are made of SiC. These diodes have a lower reverse recovery current than Si diodes, thus reducing commutation losses.

An Infineon FF600R12IS4F IGBT module is used for each leg has been chosen by EEI [9]. The module is composed of two Si IGBTs (Infineon fast IGBT2 technology, 600 A, 1200 V) and two antiparallel SiC diodes (360 A, 1200 V) and it is suitable for high switching frequency applications.

With these components a 30kHz switching frequency has been reached on the prototype, thus an output frequency of 60kHz.

In addition, in order to reduce commutation stresses on the IGBT, RC parallel snubbers ( $R_s = 1.65 \Omega$ ,  $C_s = 20 \text{ nF}$ ) have been adopted by EEI for each switch. The composition of the H-bridge with the snubbers can be seen in Fig. 5.1.

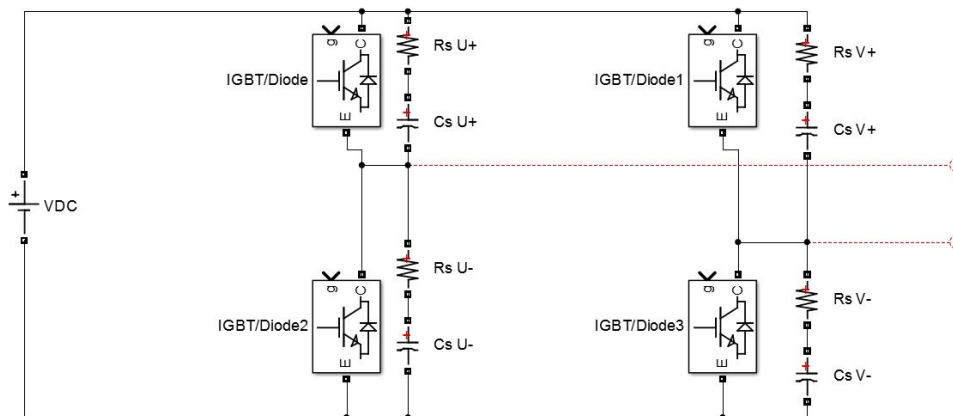


Figure 5.1: The topology of the H-bridge with the snubbers.

### 5.3 Input capacitor bank

Film capacitors are installed close to the H-bridge at input side. In combination with a couple of differential-mode inductance, they form an input filter against the high-frequency components of the input current. The most critical requirements are their current rating and high frequency performance, required to filter out the current harmonics (60kHz and multiples). Also, they are subjected to a current frequency that is twice the fundamental load current frequency.

6 off DUCATI energia DC85C series (650  $\mu$ F each, 900 Vdc) have been chosen by EEI for the prototype because readily available. They are characterized by reasonably low self inductance (<60 nH each) and series resistance (3.5 m $\Omega$  each), and sufficient rated rms current (40 A each).

### 5.4 Output filter

An output filter is required in order to:

1. reduce the current ripple;
2. avoid overvoltages on the coaxial cable,
3. uniform the load impedance, that may vary due to different cable lengths;
4. reduce electro-magnetic-interference (EMI) produced by voltage rising/falling fronts.

About the cable overvoltage problem, one must consider that the rise/fall  $\tau_r$  time of the voltage at the switches end is about 100 ns: so the propagation effects along the cable must be considered. Firstly the dielectric constant of the cable must be calculated using the formula:

$$\varepsilon_r = \frac{\ln(D/d) \cdot C}{2\pi\varepsilon_0 \cdot l} \quad (5.1)$$

where D is the return shield diameters, d is the internal core diameter, C/l is the cable capacitance and it results  $\varepsilon_r = 4$ . Then it is possible to calculate the critical length, defined as the cable length at which voltages up to twice the DC-link voltage can be expected at load terminals:

$$l_c = \frac{\pi \cdot c \cdot \tau_r}{4\sqrt{\varepsilon_r}} \quad (5.2)$$

which yields a critical length of 12m. The use of PWM with high carrier frequencies in association to cable length higher than the critical length may lead to overvoltage up to two to three times the DC-Link voltage at the load terminals [9, 11].

From the requirements, a maximum  $\pm 30$ A of current ripple is imposed, that is 10% of the nominal 300A current. Considering that the ripple frequency is at 60kHz and choosing an LC filter, that give a -40 dB/dec attenuation after the resonance frequency, it should be placed 0.5 decades before the switching frequency, leading to a 20kHz resonance frequency.

The filter inductance has been chosen by EEI keeping in mind that the higher the inductance, the lower the filter current ripple, but the higher the required DC-Link rated voltage to provide the required performance. So, from the requirements, the current on the inductance should not increase more than 60A during the time interval in which the full DC-link voltage (300 V) is applied on the load. Assuming to have the nominal voltage on the capacitance (240V), when the H-bridge applies 300 V at the output, 60 V are applied on the inductance. Because in order to maintain 240V on the load the required duty cycle is 0.8, the full 300V voltage is maintained for  $\Delta t = 0.8/60000 = 13.33 \mu$ s. So, from the formula:

$$\Delta I = \frac{V_L}{L} \cdot \Delta t \quad (5.3)$$

Imposing  $\Delta I = 60$ A and  $V_L = 60$ V, it is  $L = 13.3 \mu$ H. Given the sizes available in the market, 2 inductances of 6  $\mu$ H have been chosen by EEI.

To obtain the chosen resonance frequency a 5  $\mu$ F capacitance is then required. By the way, a damping RC branch is needed to reduce the resonance peak of the transfer function and it is made with a 4.7  $\Omega$  resistor and a 2  $\mu$ F capacitance. That results in two parallel branches: one with the RC series and one

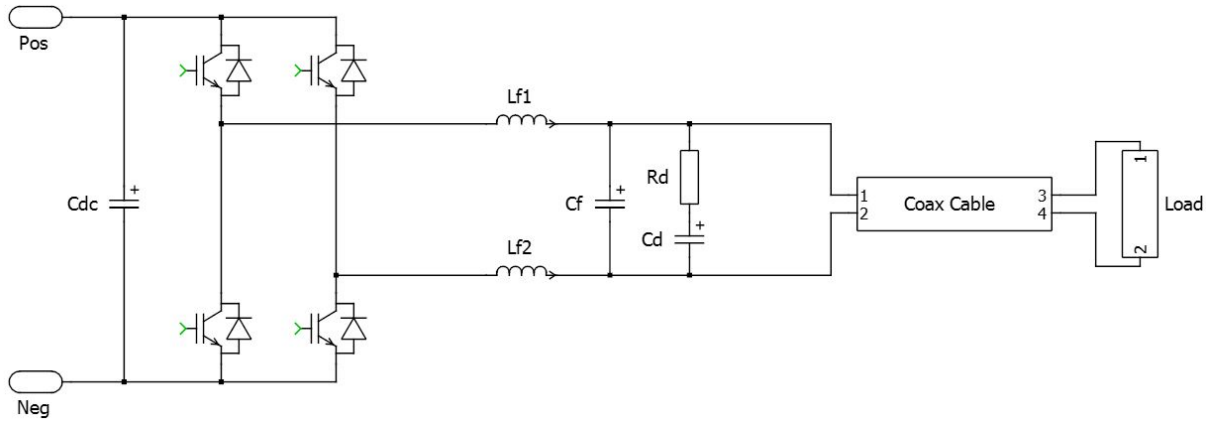


Figure 5.2: The fast converter and output filter topology (courtesy of EEI), where  $L_{f1}=L_{f2}= 6 \mu\text{H}$ ,  $C_f=4 \mu\text{F}$ ,  $C_d=2 \mu\text{F}$ ,  $R=4.7 \Omega$ .

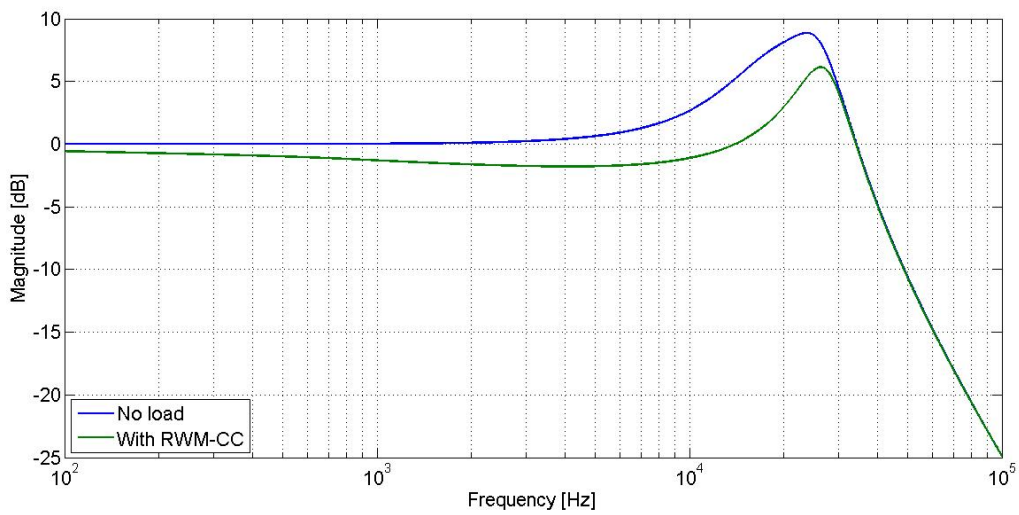


Figure 5.3: Attenuation of the filter with the RWM-CC connected (green) and without it (blue).

with a 4  $\mu\text{F}$  capacitance, as shown in Fig. 5.2. Fig. 5.3 shows the voltage attenuation of the filter; note how with the RWM-CC connected the resonance peak is lower and, also, there is a certain attenuation of the voltage at lower frequencies, while without the load the filter is virtually transparent to the voltage.

## 5.5 Control board

The converter control system has to be very fast in order to satisfy the dynamic requirements, such as the low latency. In addition to that the control boards will feature a complete set of communication ports, which include Ethernet ports, digital and analog ports. These are needed in order to communicate with the SCSDAS, through the local control cubicle (LCC). Also, all the I/O signals have to be safely galvanic insulated from the power section.

So, the control boards of the prototype have a master/slave configuration, in which:

- a slave control board (SCAB) is designed with an Altera Cyclon V FPGA, with a 4ns resolution (245 MHz clock), that manages all the feedback measurements and can actively modify the PWM gate pulses;
- a master control board (MCB) is made with a Texas Instruments (TI) 32-bit 60MHz ARM micro-controller that supervises and controls the operation of the entire converter.

All the acquired signals are in the analog ( $\pm 10\text{ V}$ ) form, while parameters (alarms and values) exchange between the converter control boards and the LCC are made via Ethernet.

So, the SCAB acquires both the load current and voltage with two fast (3 Msps) 12-bit ADCs with SPI interface. Then it averages them with a 16-sample or 32-sample per each half PWM period average and it sends these signals to the MCB by converting the obtained digital signals to analog ones. Then the MCB samples the feed-back signals and executes the main control routine. A qualitative scheme of the control system can be seen in Fig. 5.4.

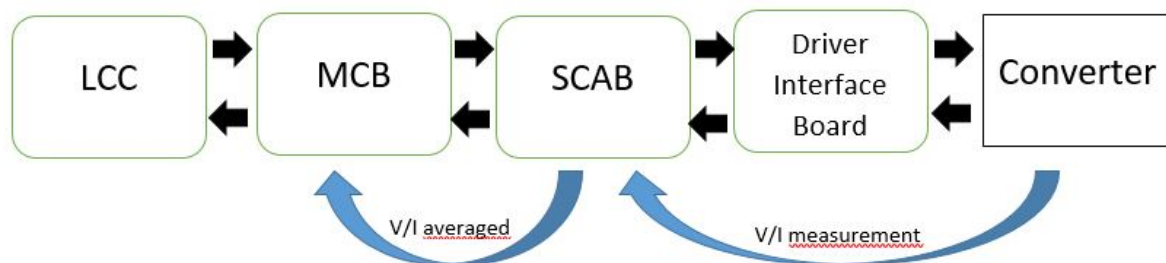


Figure 5.4: A simple scheme of the control board.

Two control schemes are available:

1. Mode 1: Current Control Mode (CCM), that is a closed-loop scheme;
2. Mode 2: Voltage Control Mode (VCM), that is an open-loop and a faster control scheme.

In CCM the current is regulated by a simple PI controller with anti-windup function, that is executed with a 60kHz rate (around every 16.67  $\mu\text{s}$ ). It receives the averaged feed-back current by the SCAB, then it executes the PI algorithm and generates the unipolar PWM switching pattern. The chosen execution rate and PWM frequency yield a worst-case latency between reference step and duty-cycle variation of less than 50  $\mu\text{s}$  as required.

In VCM, voltage drops both on the switches and the output filter inductances have to be compensated. For the switches, a numerical characteristic is implemented, while, for the inductances, the voltage drops are compensated by calculating the derivative of the current at each PWM cycle. Both these compensations are directly implemented in the main control routine. The resulting control scheme can be seen in Fig. 5.5.

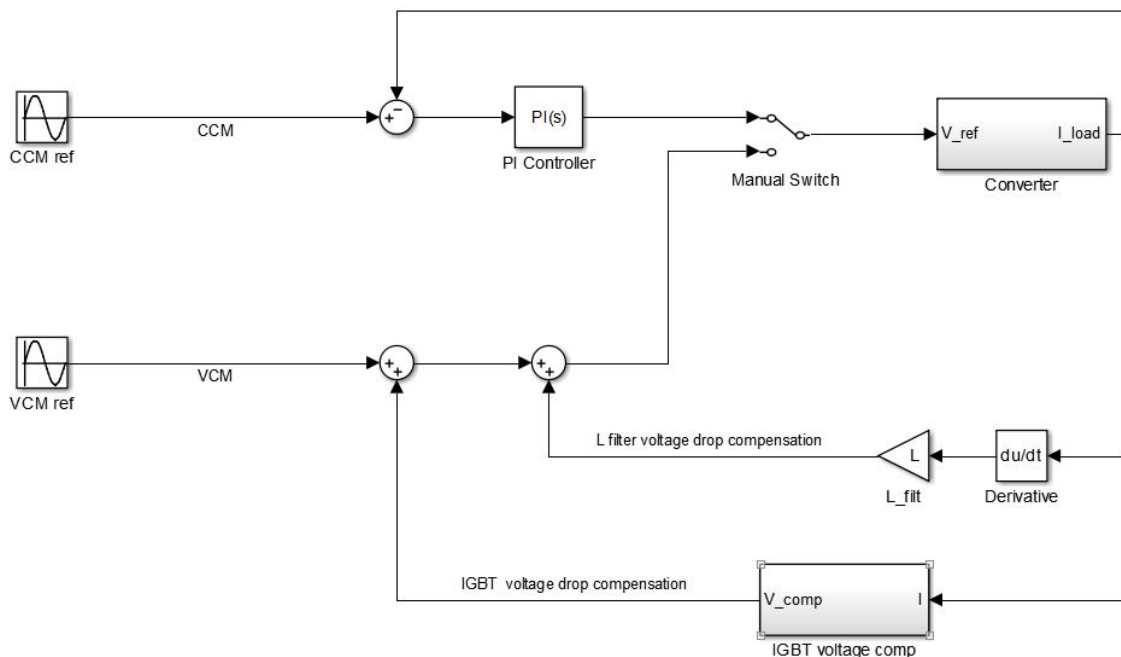


Figure 5.5: A scheme that shows the main control blocks.

## 5.6 Voltage slope limits

The nominal  $dV/dt$  limit is 20 MV/s, but it would be better if the effective voltage slope on the load was reduced toward 10 MV/s to improve the voltage distribution among coil turns against capacitive effects. The voltage slope strictly depends on the output filter. In the prototype, the filter guarantees a maximum  $dV/dt$  that is between 15 and 20 MV/s. So, additional analysis have been started out by the Author in order to further reduce the voltage slope.

## 5.7 Thermal limits

Firstly it is to be noted that the actual prototype is only air-cooled, while the final product will be water-cooled. This is because the air cooling is sufficient in order to reach the objectives the prototype is meant for. In particular, the maximum pulse length for the prototype has been set to 2 s.

From the IGBTs data-sheets, 1.9kW losses have been calculated by EEI with 300 A peak at 500Hz, with a worst-case junction temperature of 125°C. In DC operation, due to the fixed current sign, on each switch only the IGBT or the diode conduct. This lead to a worsening of the operating condition: in-fact simulations show greater losses on the switches, up to 2.76kW with 300A<sub>DC</sub>. By the way, the converter prototype was able to run safely and indefinitely with a load current of at least 100 A<sub>DC</sub>. In addition, the water-cooled converter will exceed the performance of the prototype and will be able to provide a 300 A peak sinusoidal waveform indefinitely. In any case, the converter has to be capable to provide 300 A<sub>DC</sub> until the switch junctions are in thermal regime with the respective case, without damages. It is acceptable that, after some time, the thermal protection, based on the NTC sensor embedded with the case, intervenes.



## Chapter 6

# The converter model

### 6.1 Introduction

In order to optimize and study the PS behavior, a mathematical model of the system is needed. The model has been implemented both with PSIM<sup>®</sup> and Matlab Simulink<sup>®</sup>. The load, with its particular impedance, was initially modeled with Cauer cells by EEI using PLECS<sup>®</sup>, then researchers at Consorzio RFX ported the model in the PSIM<sup>®</sup> platform and also they modeled it with a convolution-based one. While the Cauer model replicates the quasi-exact impedance of the load for frequency up to 3 kHz, the convolution-based one could replicate the behavior also at much higher frequencies, also beyond the switching frequency, allowing to see the effects on the load of PWM frequency. By the way, this model needs further validations of its results, that is one of the objectives of this thesis. Note that the original convolution-based model developed by Consorzio RFX is made with the SimCoupler S-function: a Simulink<sup>®</sup> block that interfaces Simulink<sup>®</sup> itself and PSIM<sup>®</sup>. In-fact, the whole H-bridge and control section was originally developed on the PSIM<sup>®</sup> platform by Consorzio RFX. Then the Author made the porting of the whole power and control section in Simulink<sup>®</sup> obtaining a half of the initial simulation time. The final model is shown in Fig. 6.1.

### 6.2 The Simulink<sup>®</sup> fast converter model

The model of the converter power section has been implemented by the Author in a dedicated block, shown in Fig. 6.2, which takes as input the duty-cycle values generated by the control section and gives as output the voltages at the negative and positive output terminals downstream the filter. The DC-link, actually, is an ideal one implemented inside this subsystem, but it could be modeled with more details in a dedicated block.

The input duty-cycle signal is sampled with a 60kHz rate by using a sample and holder. Then the sampled signal is duplicated: one is directly compared with a 30kHz triangular wave, the other is firstly inverted and then sent to the comparator. By doing this, we obtain the unipolar control.

Then the so created PWM signals are fed to the ideal IGBT switches: at this level, in case, a dead time (DT) compensation and insertion block can be implemented, as shown in subsequent chapters. Downstream the IGBT section is lastly placed the output LC filter.

The snubbers are not implemented in this model for simplicity. They will be included only for the analyses of sections 13 and 14, were they can influence the results.

### 6.3 The Simulink<sup>®</sup> control model

A discrete PI controller has been implemented which takes as input the difference between the reference and the feed-back current and gives as output the duty-cycle signal. The anti-windup feature is implemented with a saturation block, placed inside the discrete integrator.

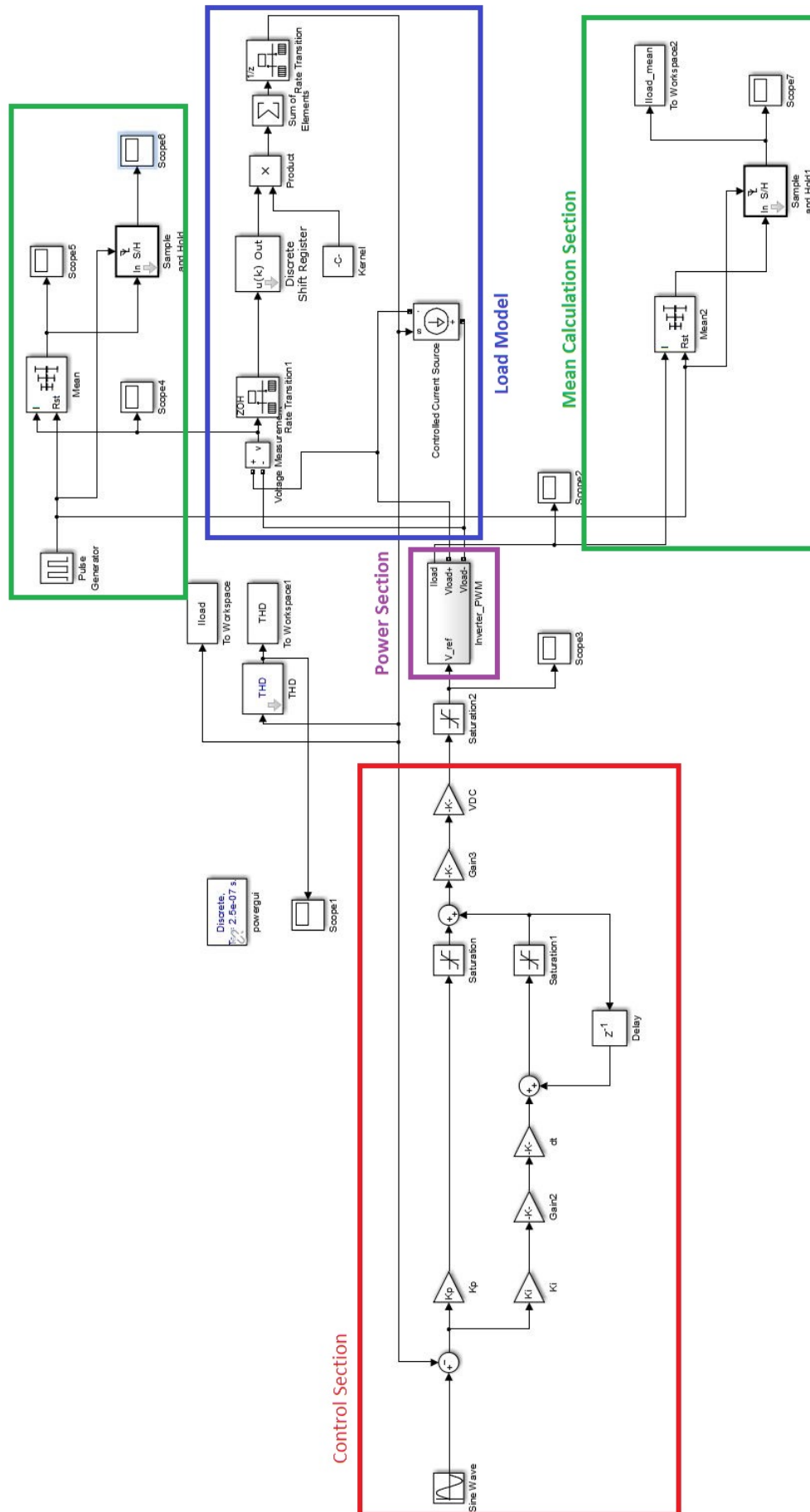


Figure 6.1: Overview of the Simulink® model, with the convolution-based model of the load.



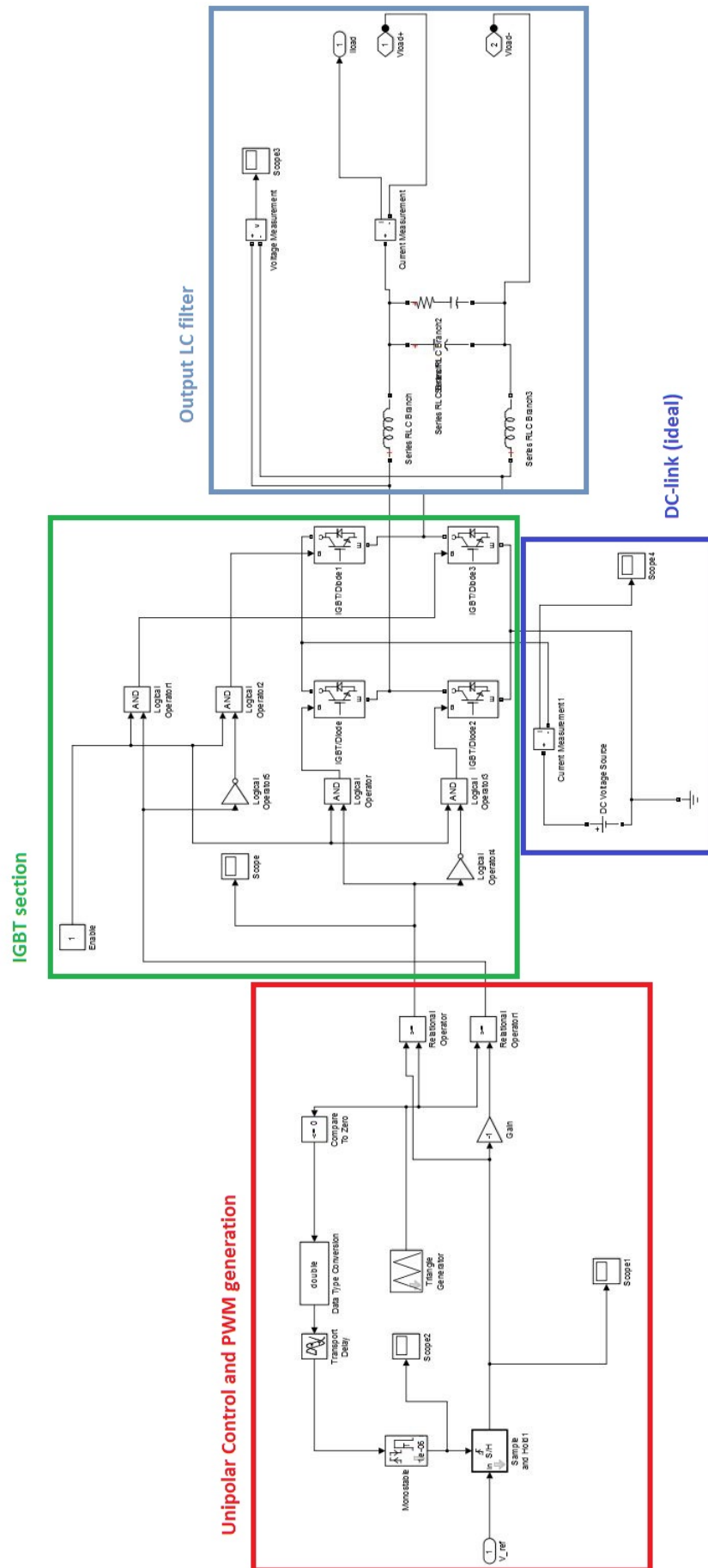


Figure 6.2: Simulink® model of the power section.

## 6.4 The load model based on Cauer cells

The Cauer-cells model is based on the creation of a network of multiple RL dipoles. The resistances and inductances values of the dipoles are chosen in order to recreate approximately the same frequency response of the real load.

EEl empirically found the correct values of the RL dipoles such to replicate the real frequency response for frequencies up to 3 kHz. These values substantially recreate poles and zeros of the transfer function of the load.

As result in Fig. 6.3 is shown the load impedance and phase of the obtained model compared with the RWM-CC one.

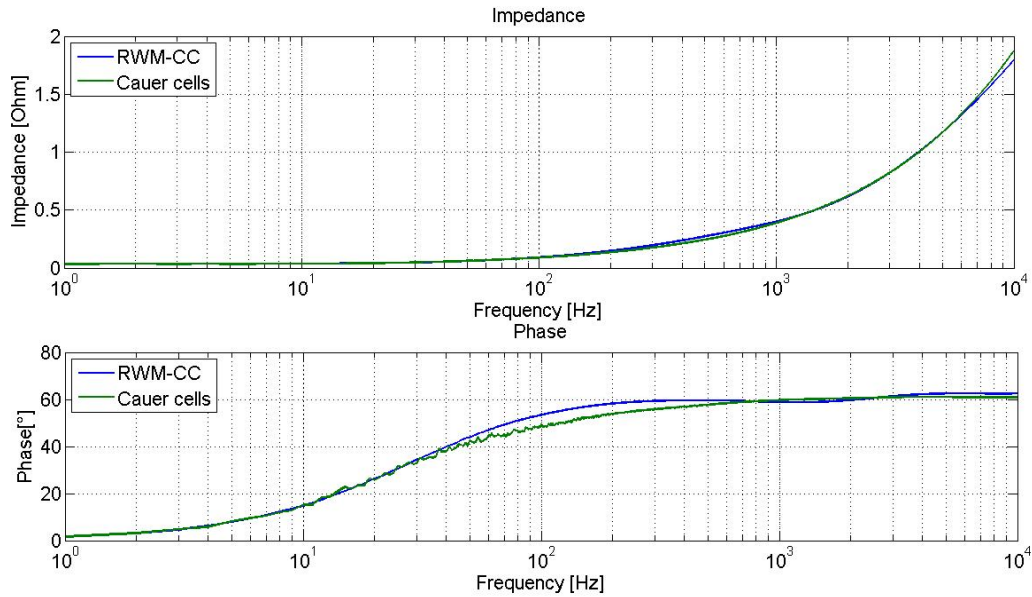


Figure 6.3: The Cauer cell characteristic up to 10 kHz compared with the RWM-CC one.

It can be noted how the resulting load follows quasi-exactly the real characteristic up to more than 3 kHz. In Fig. 6.4 is shown also the electrical scheme of the model.

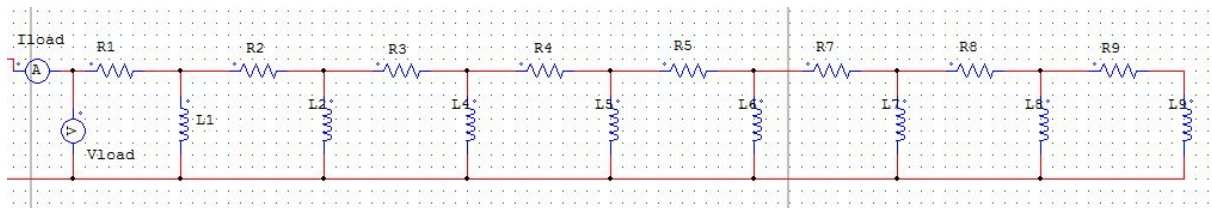


Figure 6.4: The Cauer cell electrical scheme, downstream the output filter.

## 6.5 The load model based on convolution

The convolution model, originally developed by ing. A. Ferro [12], is based on the assumption that a particular solution of an ordinary differential equation can be defined as:

$$i_p(t) = v(t) * h(t) \quad (6.1)$$

Where:

- $i_p(t)$  is the particular solution;

- $v(t)$  is the input forcing voltage signal;
- $h(t)$  is the system impulse response in the time domain.

We can consider, for example, the classical RL model:

$$v(t) = R \cdot i(t) + L \cdot \frac{di}{dt}(t) \quad (6.2)$$

The definition impulsive response  $h(t)$  is, by definition, the solution of the RL equation with a Dirac's impulse as input and null initial condition:

$$\delta(t) = R \cdot h(t) + L \cdot \frac{dh}{dt}(t) \quad (6.3)$$

Convolving each term with  $v(t)$  and using the derivative property of the convolution:

$$v(t) * \frac{dh}{dt}(t) = \frac{d}{dt}[v(t) * h(t)] \quad (6.4)$$

We get:

$$v(t) * \delta(t) = R \cdot (v(t) * h(t)) + L \cdot \frac{d}{dt}(v(t) * h(t)) \quad (6.5)$$

But the Dirac's delta is the neutral element of the convolution, so they get:

$$v(t) = R \cdot (v(t) * h(t)) + L \cdot \frac{d}{dt}(v(t) * h(t)) \quad (6.6)$$

Comparing (6.6) with (6.2), they get that  $v(t) * h(t)$  is actually the particular solution  $i_p$ , because initially we didn't consider the initial conditions. Finally, this demonstration can be generalized for all linear ordinary equations and linear-time-invariant (LTI) systems.

The actual load can be characterized with a frequency response, that, however, cannot be defined with a single resistance and inductance. So, the system cannot be described with the RL first order differential equation, but with a greater grade one. In-fact, in principle, as it has been described in the previous paragraph, it is possible to recreate approximatively the frequency response of the load with a finite network made of constant resistances and inductances. This is because the local properties of the system, such as the dielectric constant, conductivity and permeability, are all constant in time. So, this possibility and the fact that an unique frequency response can be defined makes the load a LTI system, where the assumption in (6.1) is still valid.

## 6.6 The Simulink® implementation of the load model

The discrete convolution has been implemented in the past by ing. A. Ferro in Simulink® by using a shift register and some rate transition blocks.

In-fact, in order to compute the impulsive response, a fixed frequency step  $f_{step}$  is defined and the interval of frequencies of our interest, that goes up to  $f_{max}$ , is so discretized in  $N = \frac{f_{max}}{f_{step}}$  frequency values. So, the load admittance has to be characterized up to  $f_{max}$ , but then the values are extended also up to  $2f_{max}$  in order to obtain a function that is symmetric conjugate. By doing so, we end up with a function that has Hermitian symmetry with respect to  $f_{max}$ , with  $2N$  samples. Now it is possible to do the inverse-fft, by using the Matlab command `ifft()`, and we obtain a real impulse response  $h(t)$  that extends from 0 to  $1/f_{step}$ , with a time step of  $1/2f_{max}$  and  $N$  samples. This is also called the kernel of the admittance. Hence, the discrete convolution can be obtained by implementing the subsequent formula:

$$i(t) = i_{(m \cdot t_{step})} = (v * h)_{(m \cdot t_{step})} = \sum_{n=0}^{\min(N-1, m)} h_{(n \cdot t_{step})} \cdot v_{((m-n) \cdot t_{step})} \quad (6.7)$$

Note that  $t_{step}$  used in the convolution is, in general, different from the simulation time step, so rate transition blocks are needed. Also, the number of samples of the voltage must be equal to  $N$ : this can be achieved by using a discrete shift register, that always selects a running  $N$ -samples window of the voltage. The resulting system is hence pictured in Fig. 6.5.

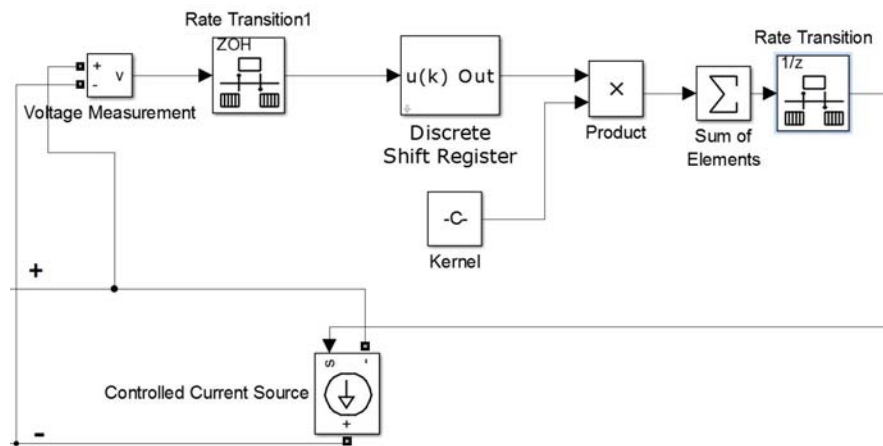


Figure 6.5: The load model.

## 6.7 The load characterization

Starting from the measurements done on the dummy load for frequencies up to 100 kHz (Tab. 4.1) and from the results of simulations done by using a FEM model of the RWM-CC up to 10 kHz (Tab. 2.1), we both interpolate the existing data and extrapolate it, if necessary, toward 100 kHz by using a spline interpolation. The results are shown in Fig. 6.6.

Then, we duplicate the results up to 200 kHz, in order to obtain the Hermitian symmetry of the Fourier transform, and we make the inverse Fourier transform. By doing this we finally obtain the kernel of the admittance, as shown in Fig. 6.7.

This process has been initially implemented by ing. A. Ferro on a Matlab code, then the Author optimized the code in order to suppress the numerical noise created by the `ifft()` function by using a running mean. The final code can be found in the Appendix.

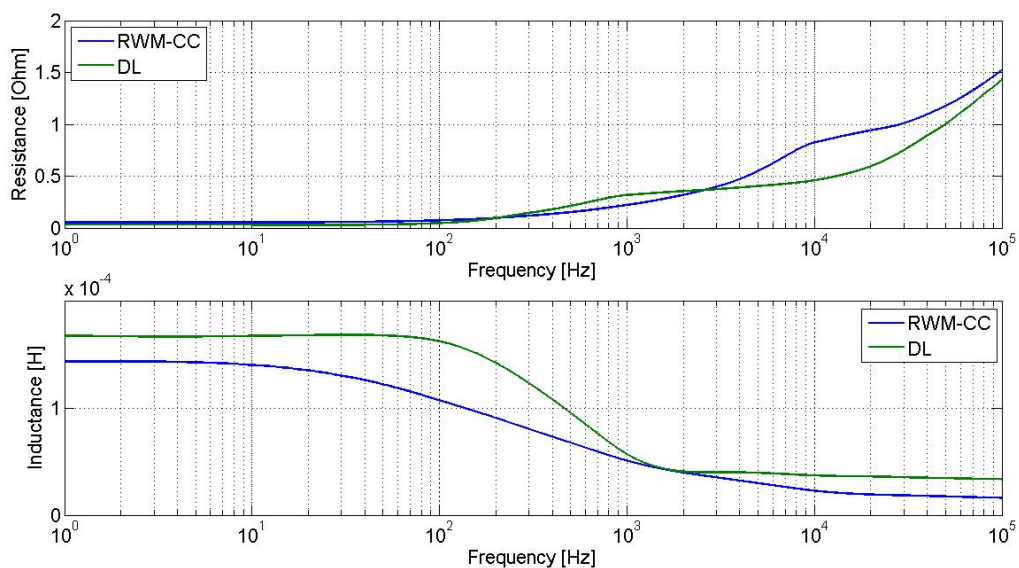


Figure 6.6: The interpolation of the resistance and inductance of both DL and RWM-CC.

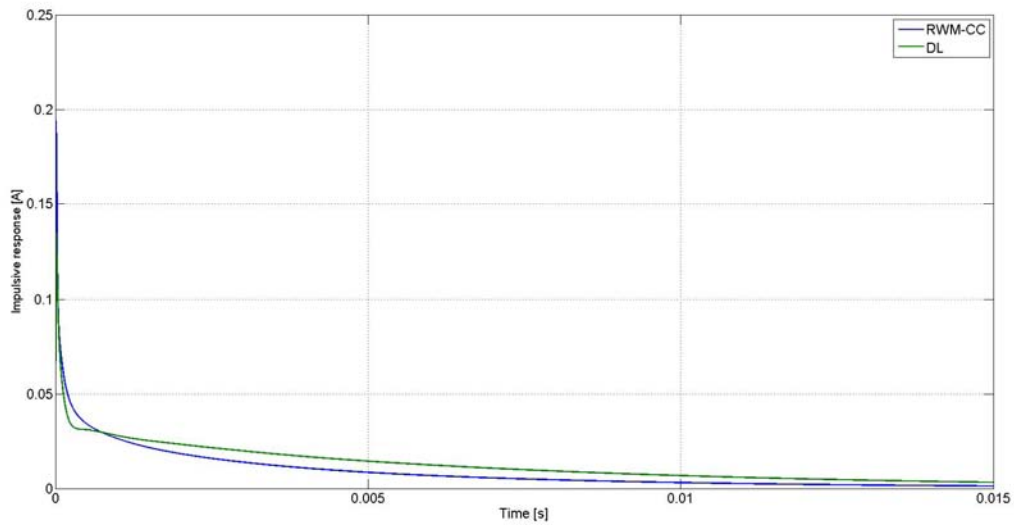


Figure 6.7: The impulsive response of the DL and the RWM-CC.

## 6.8 Precision of the convolution-based model

In order to evaluate the precision of the model it is possible to re-estimate the dummy load (frequency of which characteristic has been measured up to 100 kHz) admittance and impedance by using the model itself. Then, the obtained results can be compared with the measured data on the real load. The obtained results are shown in Fig. 6.8 and 6.9.

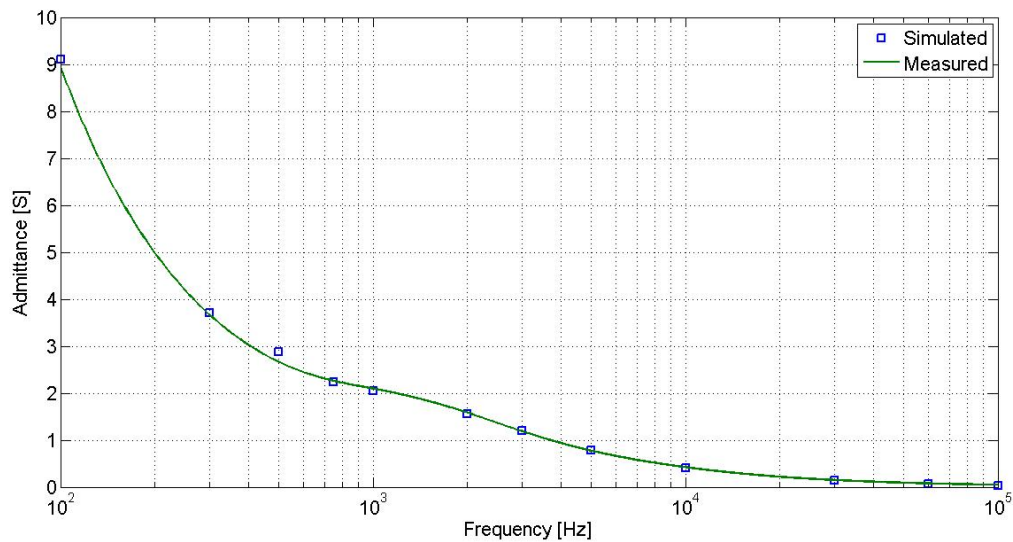


Figure 6.8: The comparison between the simulated admittance and the measured one.

As can be noted, in particular on the impedance graph, the model is precise up to 20 kHz. Then there is a certain deviation from measurements for higher frequencies. Infact, approaching gradually the 100 kHz threshold, higher harmonics start to influence the system behavior. However, the model does not have any information about the real system behavior at those frequencies, causing the observed errors to appear.

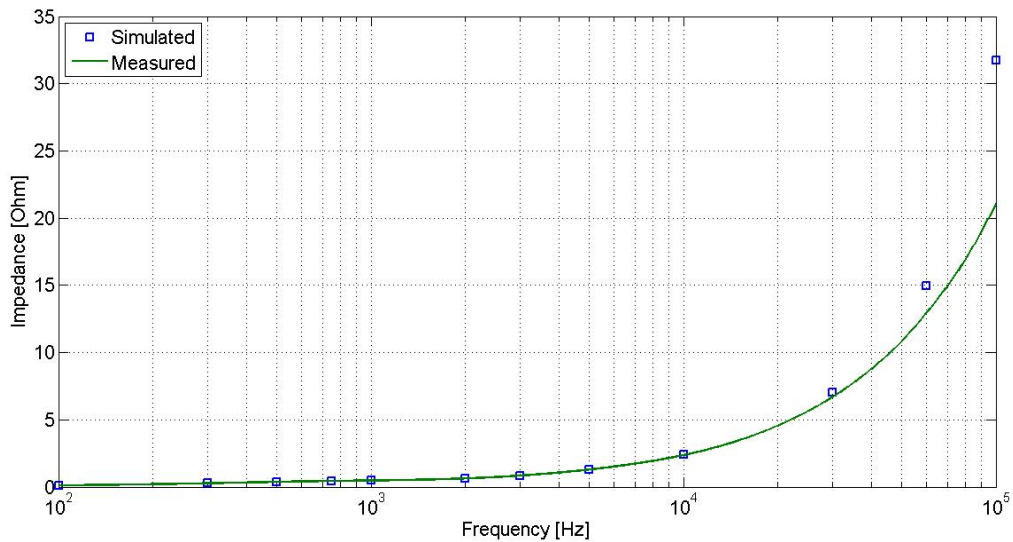


Figure 6.9: The comparison between the simulated impedance and the measured one.

## 6.9 Cauer cell vs convolution model comparison

The admittance and the impedance of the RWM-CC with the convolution and with the Cauer cell has been estimated and compared. The results can be seen in Fig. 6.10 and 6.11.

It came out that:

- at low frequencies the convolution-based model should be more precise, maybe because it can better describe the rapid variation of R and L that happens at those frequencies;
- at higher frequencies (more than 20 kHz), the Cauer cells model behaves better than the convolution-based one, due to the approximation described in the previous paragraph.

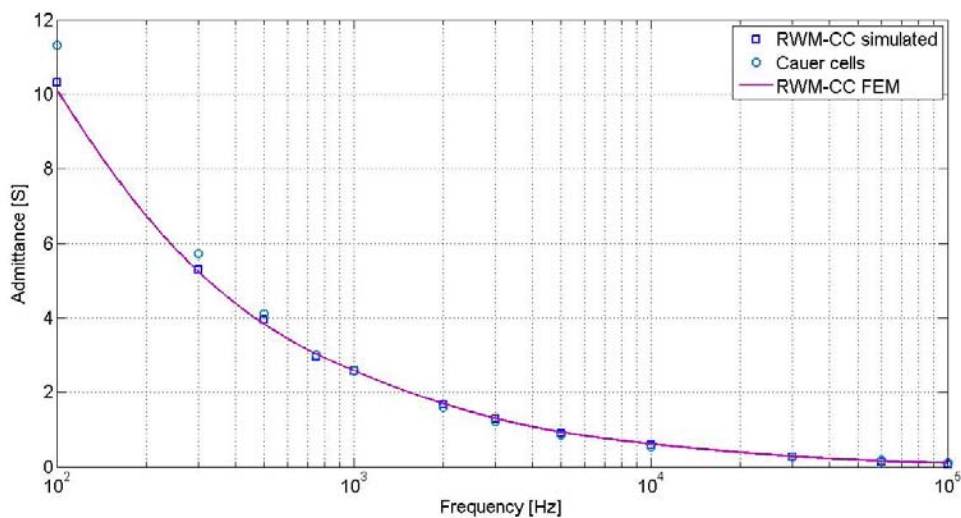


Figure 6.10: The comparison between the simulated admittance and the measured one.

In addition, a comparison between the two models has been made with the full converter model in CCM. The results are shown in Fig. 6.12, all calculated with the RWM-CC as load and  $K_i = 0.3$  and  $K_p = 1.35$  for the PI controller. The results are similar up to 1 kHz. For higher frequencies the Cauer cells model

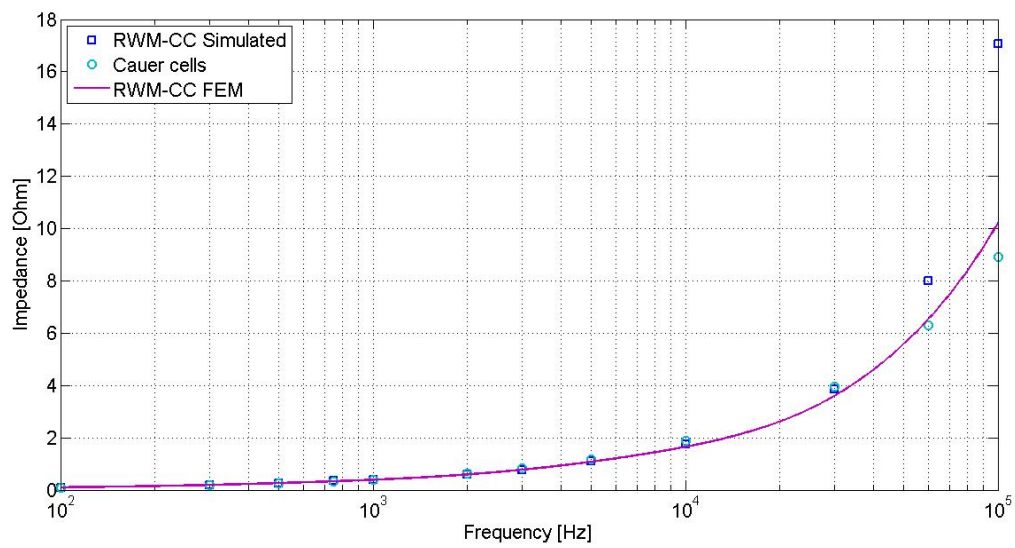


Figure 6.11: The comparison between the simulated admittance and the measured one.

shows lower currents, this maybe due to the controller capabilities which increasingly affects the system's behavior.

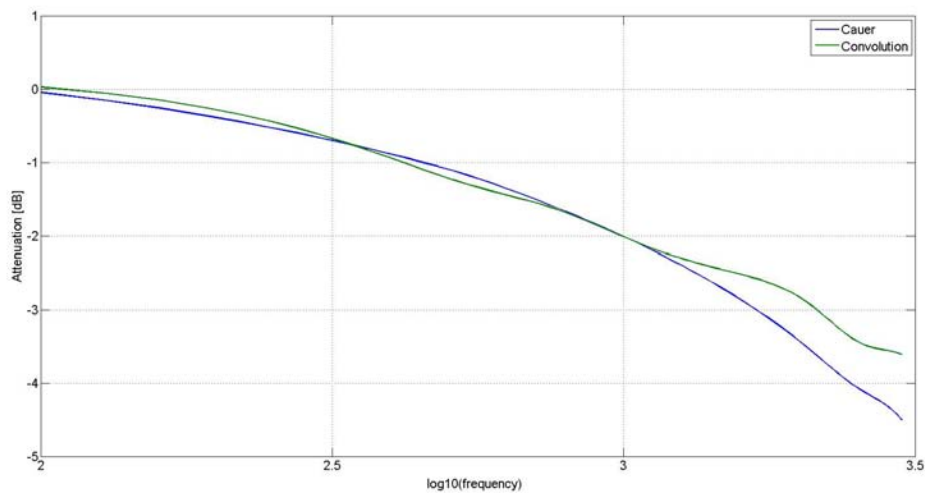


Figure 6.12: The current attenuation over frequency.

In conclusion, it has to be noted that the convolution model is much more flexible than the Cauer cell one. In-fact obtaining the impulsive response of a given system is simpler than tentatively trying to replicate its load impedance with a finite network of resistances and inductances.

## 6.10 The discrete shift register

The Matlab® built-in discrete shift register is limited to only 32000 vector points. This limits the maximum time resolution of the whole simulation. In-fact, with 32000 vector points, it is possible to refresh the load current only once every 1  $\mu$ s, because the impulsive response is 32 ms long, in-fact it results  $0.032/1E-06=32000$ . So, in order to decrease the time step the Author had to build a new shift

register.

The shift register has a first-in-first-out (FIFO) logic, so at every time step of the simulation it is needed to delete the last element of the vector and insert as first element the new voltage evaluation. It is possible to do this using vector concatenate and vector de-mux blocks, as shown in Fig. 6.13.

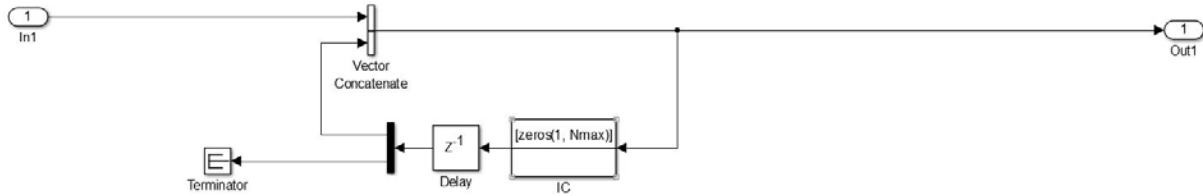


Figure 6.13: The shift register implementation.

So, the output vector is fed-back with a one step delay and while doing this its last element is deleted with a vector de-mux. Then the new voltage evaluation is inserted as first element with a vector concatenate block.

Obviously, in order to increment the time resolution the number of elements of the vector have to be increased. For example, if a 250 ns time step is wanted,  $0.03/250E-9=120000$  elements are needed. So the computational time of the convolution is greatly increased. Also the load characterization script had to be improved in order to manage the increased time step of the evaluation of the kernel.



# Chapter 7

## DT compensation

### 7.1 Introduction

Taking into account a single branch of the inverter, a dead time (DT) between the switch-off of one of the IGBTs and the switch-on of the other one is necessary to prevent possible short circuit, due to non-instantaneous turn-off/turn-on.

So, a  $t_{DT} = 1.6 \mu s$  DT has been adopted by EEI in the converter. Assuming an equivalent switching frequency  $f_S = 60 \text{ kHz}$  and a DC-link voltage  $V_{DC} = 300 \text{ V}$ , using the formula:

$$\Delta V = \pm t_{DT} \cdot f_S \cdot V_{DC} \quad (7.1)$$

we get  $\Delta V = \pm 18 \text{ V}$ , where the  $\Delta V$  is positive when the branch current is negative (entering the load) and vice-versa (exiting the load), due to the activation of the anti-parallel diodes. Note that this formula is valid only when the turn on/off time of the IGBTs are negligible in comparison with the DT itself. In particular this approximation is not valid when the current is near zero and the  $\Delta V$  result somewhere between 0 and 18 V.

In conclusion, the DT voltage error is not negligible: in-fact, due to the very low resistance of the load, in steady-state condition it can give rise to current errors over 300 A on the load [9], in-fact the subsequent formula is valid:

$$\frac{18V}{R_{\text{load,DC}}} = \frac{18V}{52.6\text{m}\Omega} = 342\text{A} \quad (7.2)$$

So, it has to be compensated. The compensation method adopted by EEI in the prototype is based on the one illustrated in [13]. So, in the following paragraph the functioning of the compensation method and how the Author implemented it in Matlab Simulink® is illustrated.

### 7.2 DT compensation method

Since the inverter must follow an arbitrary current reference which doesn't have a specific predefined shape, a feed-back type DT compensation method is needed [9]. In a first explanation, it works as follows:

1. the measured branch voltage (terminal-to-ground voltage) is converted to a logical (boolean type) signal, which is 1 when the voltage is equal to  $V_{DC}$ , creating the feed-back signal (F);
2. the feed-back is then compared with the reference PWM signal (R), which is 1 when the branch voltage is +300 V, giving as a output a compensated one (C);
3. the obtained signal then is given as input to the IGBT driver that will add the DT.

The compensation is mainly based on an integrator, called error counter (EC), that will integrate, considering a time step equal to 1, positively when R is 1 and F is still 0 (turn-on delay), and negatively when R is 0 and F is still 1 (turn-off delay). By doing this, the EC will count all the delay between the reference and the effective actuation of the command by the switches.

So now, using the EC, the compensated signal C can be generated. Firstly we define two threshold values  $T_1$  and  $T_2$  (typically 0 and 1, but they can be tuned in order to get the best performance) and we get the following cases:

- $EC > T_2$  : C is immediately changed (if needed) and maintained to 1;
- $EC < T_1$  : C is immediately changed (if needed) and maintained to 0;
- $T_1 < EC < T_2$  : C is kept equal to R, i.e. the reference signal pass through the compensator without being touched.

This basically works thanks to the EC, that always remembers and sums all the delays and advances between R and F. Also, note that the branch current is not considered, in-fact, neglecting the commutation delays given by the switches:

- if F has some turn-on delay with respect to R, it means that the current is positive and make the bottom diode conducting and keeping the voltage to zero;
- if F has, instead, some turn off delay from R, it means that the current is negative and the upper diode of the leg is conducting, keeping the voltage to  $V_{DC}$ .

Finally, if we further analyze the threshold mechanism, we get:

- positive branch current: we get  $EC \geq T_2$ . Starting with  $EC = T_2$  at the time when R becomes 1: because of the positive current, F becomes 1 with a delay DT and EC starts to grow, making, instead, C equal to 1 immediately with R. When R becomes 0, we have  $EC > T_2$ . So, in order to have C=0, we have to wait the EC to get back to  $T_2$ ; in this way, the C goes to 0 with an artificial delay, compensating the DT;
- negative branch current: we get  $EC \leq T_2$  and it operates in an opposite way than before;
- zero-crossing branch current: we get  $T_1 \leq EC \leq T_2$ . As a consequence, R is sent untouched to the IGBT driver: in-fact, theoretically, none of the diodes switch on.

### 7.3 MatLab Simulink® implementation.

In MatLab Simulink® the DT compensation algorithm has been implemented in a subsystem which takes as input the measured output voltage of the converter branch and the reference PWM signal. As output it produces the compensated signal, as shown in Fig.7.1. The output then passes through the DT inserting block, which in the Figure is here modeled as a simple "On Delay" block.

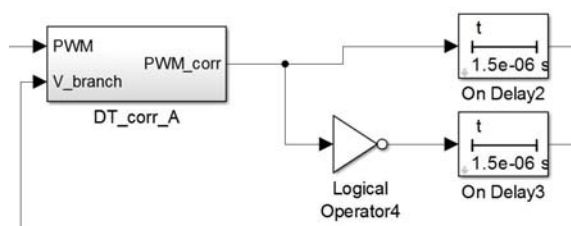


Figure 7.1: Schematic view of the DT compensation system. Actually the real DT is  $1.6 \mu\text{s}$ , but due to the 250 ns simulation time step, a  $1.5 \mu\text{s}$  DT is here imposed.

Inside the subsystem shown in Fig.7.2, it is possible to recognize an input stage and an output one. In the input stage there are the following components:

1. Relay: it converts the voltage in a logical signal; the hysteresis is necessary due to possible oscillations of the voltage;
2. XOR port: its output is TRUE only when the two inputs are different;

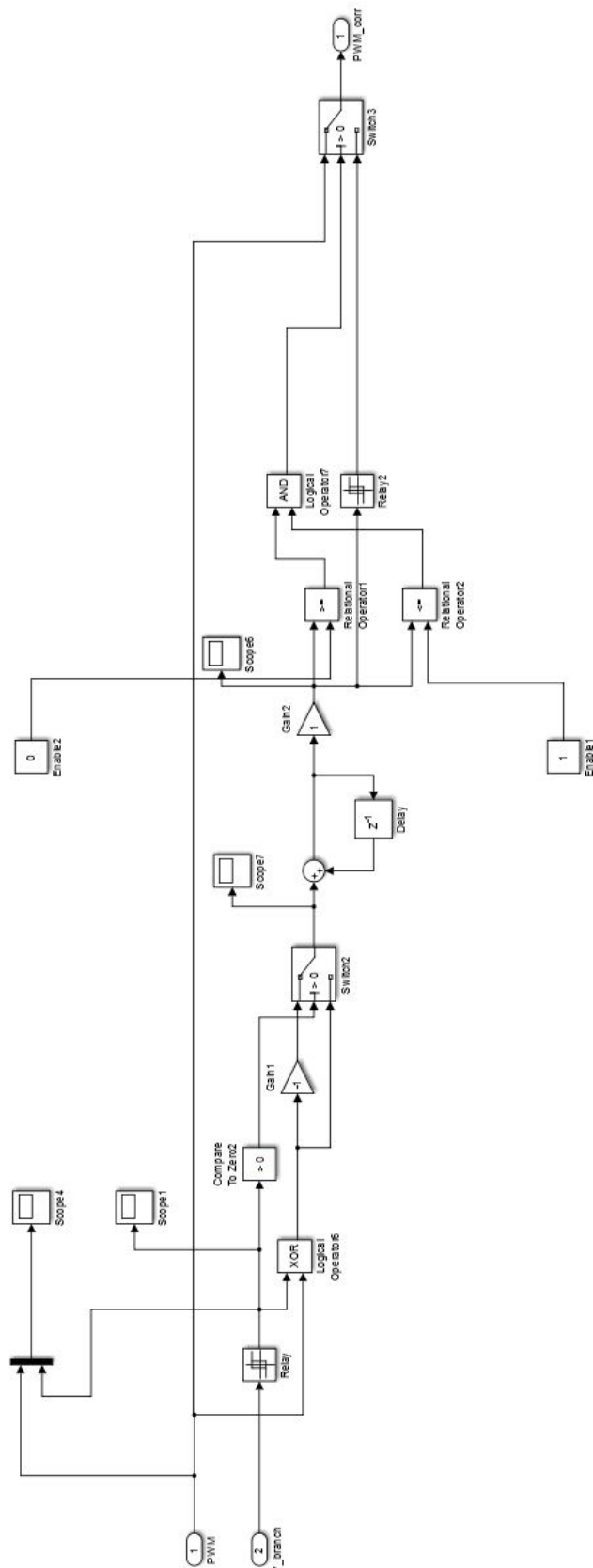


Figure 7.2: Schematic view of the DT sub-system.

3. logical switch: it selects the negative output when R is 0 and F is 1 (turn-off delay): in this way the integrator can decrease.

In the output stage we can recognize:

1. Discrete integrator: simply implemented with a one step delay, it creates the EC;
2. Relay: it recognizes when the EC do not belongs to the  $[T_1, T_2]$  interval;
3. Comparators and AND port: this system recognizes when the EC belongs to the  $[T_1, T_2]$  interval;
4. Logical switch: if the EC belongs to the  $[T_1, T_2]$  interval, then the R signal passes through the subsystem without being modified.

## 7.4 MatLab Simulink® results.

Simulating the system for 20 ms with a 100 A (peak) sinusoidal current at 100 Hz and CCM ( $K_i = K_p = 1.7$ ), which is the most demanding case for the DT compensation algorithm, we get the result displayed in Fig. 7.3.

The current is about the same result obtained without any dead time and there is a slightly improvement on the current waveform. The only thing that has to be noted is a little deformation of the sinusoidal shape, just after the current zero-crossing. This effect can give rise to high frequency current oscillations and it has been observed also in the measured data. The causes of this phenomena will be explained in a dedicated chapter.

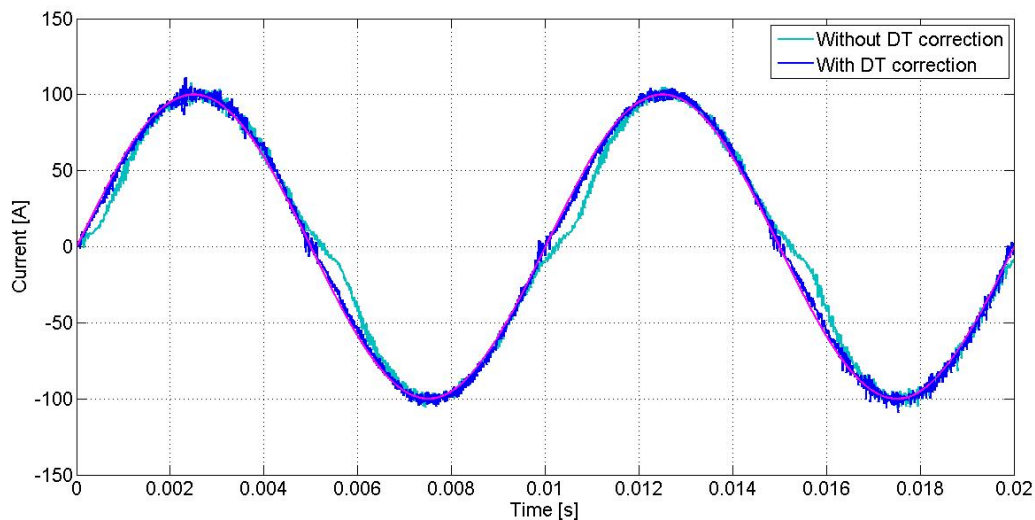


Figure 7.3: Current waveforms obtained with the Simulink® model, in CCM with  $K_i = K_p = 1.7$ , 100 A peak, 100 Hz.

# Chapter 8

## PI optimization

### 8.1 Introduction.

In a proportional integral (PI) controller it is possible to tune the integral constant ( $K_i$ ) and the proportional one ( $K_p$ ) in order to optimize the system dynamics.

Three specifications have to be fulfilled on the fast converter of RWM-PS connected to the SC:

- Attenuation at 1 kHz:  $A_{dB,1kHz} \leq 1$  dB;
- Attenuation at 3 kHz:  $A_{dB,3kHz} \leq 3$  dB;
- $\pm 4\%$  of current error for frequencies up to 100 Hz.

Furthermore, even if it is not requested on the specification, a limit on the THD at 3 kHz has been imposed in order to filter only the results that make sense.

With the  $K_i = 0.3$  and  $K_p = 1.35$  chosen by EEI for the prototype the inverter didn't fulfill all the requested specifications, in particular an attenuation at 1 kHz of 3 dB circa was measured with the dummy load, while, according to the convolution-based model, an attenuation of 2 dB is observable at 1 kHz with the RWM-CC load, as can be seen in Fig. 8.1. So it is needed to go through a further optimization process. The Author adopted a Particle Swarm Optimization (PSO) algorithm [14]. By the way, PSO is a single objective algorithm, so we need to make it Multi-Objective (MO).

To make the PSO algorithm a MO one, we will use the Pareto approach: we will find all the possible points in the objective space (the space where every point is defined by the values of the objective parameters), that dominate all the other points in, at least, one of those parameters. The group of points we will find determines the so called Pareto front. It is to be said that not all the Pareto front points will satisfy all the specification given above.

All the codes described in this chapter are based on a original PSO code written by prof. Alotto from University of Padova.

### 8.2 Particle Swarm Optimization.

The PSO algorithm is classified as a stochastic optimizer in which a "swarm" of particles (i.e. evaluation points) is randomly launched inside our domain with an initial velocity, with which each particle moves across the domain that contains all the possible  $K_i$  and  $K_p$  couples. Starting from these points, we will make an initial evaluation of our objective function by simulating the inverter, with its load, with Simulink®.

After the initial evaluation, the global best  $p_g$  and every personal best of each particle  $p_i$  are found. So now the algorithm will enter the main iterative cycle where we will calculate, at every step, the new velocity of each particle. In-fact each evaluation point can be treated as a particle with mass (inertia) and velocity, with which the particle moves around the imposed domain. So it is possible to calculate the new particle speeds by using the formula:

$$v_i(t+1) = w * v_i(t) + c_1 * [p_i(t) - x_i] + c_2 * [p_g(t) - x_i] \quad (8.1)$$

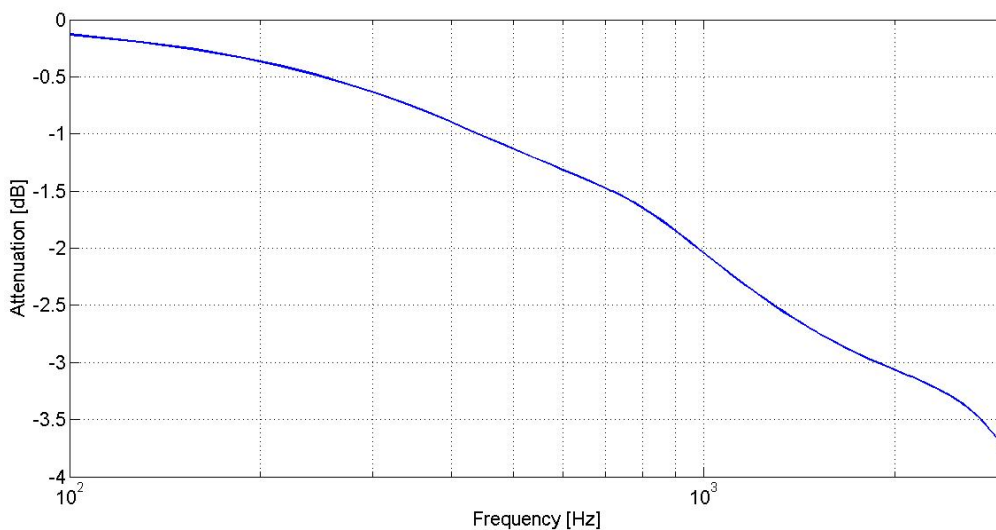


Figure 8.1: Attenuation of the system with the parameters chosen by EEI, according to the convolution-based model.

Where three components can be identified:

1. Inertia: where  $w$  is a mass-like parameter and, typically, it is linearly lessened from 1 to 0.3 at every step;
2. Cognitive:  $p_i$  is the personal best of one particle and this component lets the particle stays near his personal best;
3. Social:  $p_g$  is the global best and this component forces all the particles to move toward the  $p_g$ ;

The last two components are multiplied by a constant and typically it is set:  $c_1 = c_2 = 1.05$ .

Then each velocity will be integrated in order to find every new position:

$$x_i(t+1) = x_i(t) + v_i(t) \cdot \Delta t \quad (8.2)$$

Where  $x_i(t+1)$  corresponds to a new  $(K_i, K_p)$  couple. After this, a new objective function evaluation will begin. The iteration will stop when the max iteration number will be reached.

The so written PSO algorithm will then find the  $(K_i, K_p)$  couple that will produce, let's say, the minimum attenuation at 1 kHz, but this does not guarantee that the other specifications will be fulfilled.

So now we have to make the PSO a multi-objective algorithm.

### 8.3 Multi Objective PSO

Firstly, it is necessary to introduce two main concepts: domination and Pareto front.

We can say that one point dominates another point when all the objective parameters of the first are better than the parameters of the latter. For example, we have two points with  $P_1$  having an  $A_{db1kHz} = 0.75dB$ , an  $A_{db3kHz} = 2.9dB$  and a  $THD_{3kHz} = 0.01$  and  $P_2$  having an  $A_{db1kHz} = 1dB$ , an  $A_{db3kHz} = 3.2dB$  and a  $THD_{3kHz} = 0.015$ . It is clear that  $P_1$  dominates  $P_2$ , in-fact all the parameters of the first point are better than the parameters of the other point. By the way, if even one parameter of  $P_2$  had been better than the corresponding one from  $P_1$ , then the two points would be equal and no one would dominate (non-dominated points).

So, all the non-dominated points will be part of the Pareto front.

Starting from the PSO algorithm, once all the objective function are evaluated for the first time, it is possible to extract all the dominant point and compose the first Pareto front. So it is necessary to compare each point with all the others: if a chosen point is never dominated by the others, then it will

enter the Pareto front. On subsequent iterations the new front extraction will take in account both the new evaluations and the old front: every point will be compared with all the points of the new evaluation and, also, with all the previously extracted front points.

After the front extraction, we have to chose the global best and every personal best. For the global best we will proceed as follows:

1. firstly the point in the front with the minimum THD at 3 kHz is chosen: because, firstly, it is necessary to select output that makes sense and if the THD of all these points is, for example, more than 0.012 (that value can be tuned, keeping in mind that the fundamental harmonic to calculate the THD shall corresponds to the frequency of the reference signal), the point with minimum THD is set as global best;
2. if the minimum THD of these points is less than 0.012, all the points in the front with a THD less than 0.012 are found;
3. then from this set of points the attenuation at 3 kHz is analyzed;
4. if the minimum attenuation of these points is over 3 dB, the point with the minimum attenuation will be made the global best;
5. else if the minimum attenuation is less than 2.5 dB, then it is needed to find all the points with an attenuation less than 2.5 dB and to take as global best the one with the maximum attenuation among them, in order to facilitate the particles to go towards the 2.5-3 dB interval;
6. if the minimum attenuation is between 2.5 and 3 dB all the points that have an attenuation between 2.5 and 3 are found and the algorithm starts looking at what happen at 1 kHz;
7. so it finally choses the global best from this last set of points as the one which has the minimum attenuation at 1kHz;

Note that if the attenuation at 3 kHz is between 2.5 dB and 3 dB, then there are more possibilities to get a current error up to 100 Hz within  $\pm 4\%$ . In order to clarify these steps, Fig. 8.2 show the Matlab® code that does it. Where:

- **archivef**: array that contains all the Pareto-front values of the objective function;
- **igbest**: array that contains all the indexes of the possible new best set;
- **fgbest**: array that contains the new values of the objective function of the new global best points;
- **gbest**: array that contains the new values of  $K_i$  and  $K_p$  of the new global best points.

Note that, in these algorithm the lower frequencies are not analyzed, this is because the Pareto front extraction does it by itself and the choice of the global best is needed only to better redirect all the particles across the  $K_i$ - $K_p$  domain.

Then, for every personal best, we have to see if the new evaluation belongs to the Pareto front or not: if it belongs to the front, then we update the personal best.

## 8.4 Results

Being the RWM-CC not available for the experimental tests, the PSO-MO algorithm has been run for the first time with the dummy load, in order to test the so found PI parameters during the experimental campaign.

We obtained that with  $K_i = 4$  and  $K_p = 1.13$  all the specification could be fulfilled with the dummy load. In-fact we get less than 0.1 dB at 1 kHz and circa 3 dB of attenuation at 3 kHz. Anyway, with this result we will get an amplification of about 1 dB at 500 Hz.

Further adjustments of the parameters could be carries out to lower this amplification, however the Author put more effort in the optimization with the RWM-CC, which is the final goal of this work.

For that case, at the end of each simulation we chose the best  $K_i$ - $K_p$  couple and we took it as starting point for the next run. By doing this, we observed that some couples always survived until the last run we made. That couples are:

```

if THDmin>=0.012
    igbest=find(archivef(:,5)==THDmin);
    fgbest=archivef(igbest,:);
    gbest=archivex(igbest,:);
else
    a=find(archivef(:,5)<=0.012);
    Adb3min=min(archivef(a,4));
    if Adb3min>=3
        igbest=find(archivef(:,4)==Adb3min);
        fgbest=archivef(igbest,:);
        gbest=archivex(igbest,:);
    elseif Adb3min<3 && Adb3min>=2.5
        c=find(archivef(a,4)<=3 & archivef(a,4)>=2.5);
        b=a(c);
        bc=find(archives(b,3)>0);
        if isempty(bc)
            Adb1min=min(archivef(b,3));
        else
            Adb1min=min(archivef(bc,3));
        end;
        igbest=find(archivef(:,3)==Adb1min);
        fgbest=archivef(igbest,:);
        gbest=archivex(igbest,:);
    else
        c=find(archivef(a,4)<=2.5);
        d=max(archivef(c,4));
        igbest=find(archivef(:,4)==d);
        fgbest=archivef(igbest,:);
        gbest=archivex(igbest,:);
    end;
end;
end;

```

Figure 8.2: The Matlab code.



1.  $K_i = 2.3462$ ,  $K_p = 1.5721$ ;
2.  $K_i = 1.5362$ ,  $K_p = 1.791$ ;
3.  $K_i = 1.1877$ ,  $K_p = 1.7204$ ;
4.  $K_i = K_p = 1.7$ ;

The resulting attenuations are shown in the graphic in Fig. 8.3.

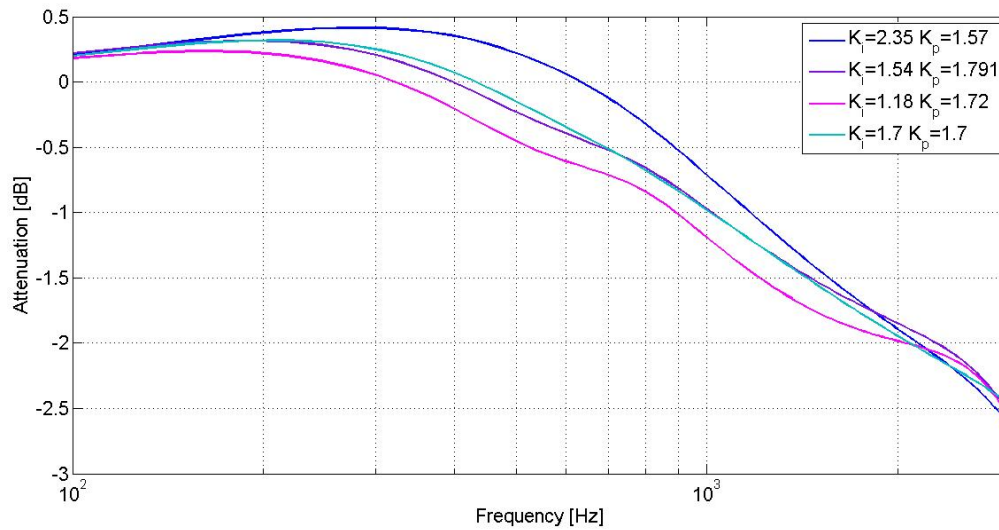


Figure 8.3: Attenuation of the system obtained with the Simulink<sup>®</sup> with the chosen parameters.



# Chapter 9

## Controller modifications

### 9.1 Controller modification

With the actual controller, that is a simple PI type, it is difficult to match the given specifications. After some optimization code runs, it came out that the controller can have 1 dB of attenuation at 1 kHz and less than 3 dB of attenuation at 3 kHz together, but with the main downside of having a peak of amplification at lower frequency, typically at 250-300 Hz, with values up to 0.5 dB. This peak of amplification influences, also, the behavior at 100 Hz, where the amplification shall be lower than 4% (0.34 dB).

Due to this limitation of the simple PI controller, some other controller topologies have been investigated, avoiding major modification of the control code of the DSP, if possible.

### 9.2 Delayed integral branch

The first possible modification is to implement the full PID controller, however this type of controller didn't show significant improvements. Also, the derivative branch probably cannot be implemented in the present controller, due to limited computational capacity.

By the way, it is possible to add to the PI controller another integral branch, which, instead, will be fed with a delayed error signal. In-fact, going deeper in the theory, it is possible to define how a delay can be modeled in the frequency domain. So, using Fourier transform formula, we get:

$$\int_{-\infty}^{+\infty} x_{(t-\beta)} \cdot e^{-j\omega t} dt \quad (9.1)$$

Where  $x_{(t-\beta)}$  is the delayed input function and  $\beta$  is the actual delay. Substituting  $\tau = t - \beta$ , because the interval of integration is  $\pm\infty$ , we get:

$$\int_{-\infty}^{+\infty} x_{(\tau)} \cdot e^{-j\omega(\tau+\beta)} d\tau = X_{(j\omega)} \cdot e^{-j\omega\beta} \quad (9.2)$$

where  $e^{-j\omega\beta}$  is the Fourier transform of the imposed delay  $\beta$ .

So this result can be added to the original PI transfer function and it results, in the Laplacian domain:

$$G_{C(s)} = K_p + \frac{K_i}{s} + \frac{K_{i,del}}{s} \cdot e^{-s\beta} \quad (9.3)$$

where  $K_{i,del}$ , in our case, should be negative.

Then, defining the total load admittance  $Y_{(j\omega)}$ , which must take in account the filter, and calculating the total closed loop transfer function, it results:

$$W_{(s)} = \frac{G_{C(s)} \cdot Y_{(s)}}{1 + G_{C(s)} \cdot Y_{(s)}} \quad (9.4)$$

So, making a comparison between the original PI topology and the new one, by using a Matlab® code (based on an previously developed Excel paper by ing. A. Ferro) which implements equation (9.4), the

results, shown in Fig. 9.1, have been obtained. They are close to the Simulink® results, in particular for frequencies up to 1 kHz. However, at higher frequencies the results are slightly different from the Simulink® results, as can be seen in Fig. 9.3.

As can be clearly seen in Fig. 9.1, the delay component  $e^{-j\omega\beta}$  creates an oscillation of the transfer function around the original one, that mitigates the resonance peak and, also, it raises up the gain at about 1 kHz.

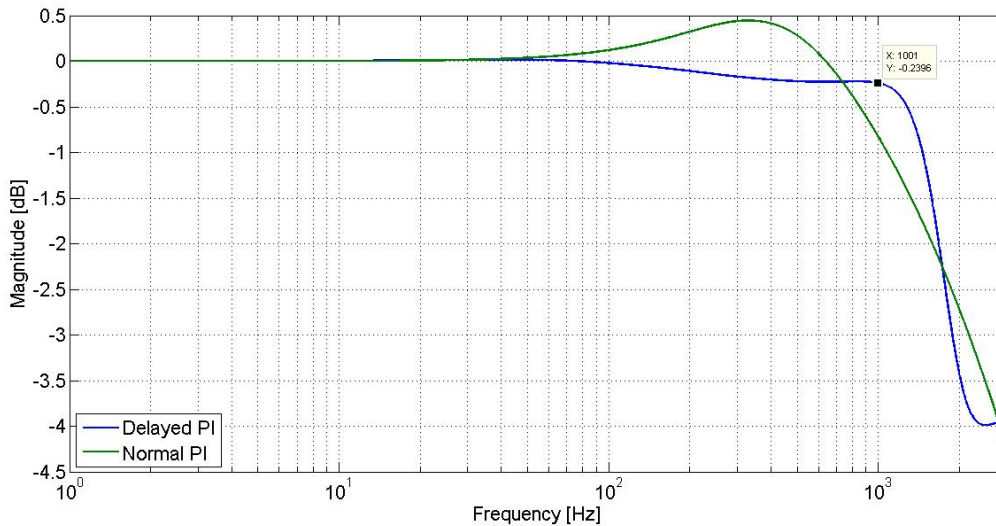


Figure 9.1: The comparison between the normal PI and the delayed one, using the transfer function estimator code.

This preliminary results were obtained by fixing the delay at  $400 \mu\text{s}$  and  $K_{i,del}$  at  $-1.8$ , while the normal PI parameter were fixed at  $K_i = 2.35$  and  $K_p = 1.57$ . These parameters were chosen because with these values the PI nearly matched the specification at 1 kHz and 3 kHz, while not having a too high resonance peak. In particular, if a delay  $\beta$  is chosen, the oscillating component of the newly obtained transfer function will have a period, on the frequency domain, of  $1/\beta$  Hz. However, the phase of the load admittance varies with frequency, so the period of the oscillation it is not exactly  $1/\beta$  Hz and, also, it will vary along the curve. This happens, in particular, because the transfer function of the delayed branch has to be multiplied with the load admittance, as shown in (9.4). So,  $400 \mu\text{s}$  correspond, theoretically, to a period of 2.5 kHz, so the oscillating component would be null at 1250 Hz and 2.5 kHz and it would have a peak at 625 Hz and a minimum at 1875 Hz. So, if the amplitude ( $K_{i,del}$ ) is negative as it is, it would cut out the resonance peak that is between 100 Hz and 1 kHz, while not really affecting the behavior at 1kHz.

Another way to choose the delay is to try to adjust the current step reference response, so that the overshoot would be canceled out. As it can be seen in the simulations made with the simple PI, typically the current reach the 300 A threshold in about  $400 \mu\text{s}$ . So, setting the delay at  $400 \mu\text{s}$  mostly cut out the current overshoot. It is to be noted that the current overshoot cut out happens only if the delayed branch component decreases the normal integral one: this can happen only with a negative  $K_{i,del}$ . In order to set the  $K_{i,del}$  parameter, it is possible to make some attempt in order to find the best transfer function. Simulations confirmed what has been found in theory and their results are shown in Fig. 9.2 and 9.3.

### 9.3 C code implementation

In the present DSP code, the PI is executed in a dedicated function, which is called by the main program at each switching period. So, the delayed integral branch has to be implemented inside this function.

A simple method to build up a delay is to create an array with a number of elements equal to the ratio between the wanted delay and the execution step-time: in our case result  $400/16.667=24$  elements. This array has to be initialized with all null elements, which can be made with a for loop. Furthermore, it can

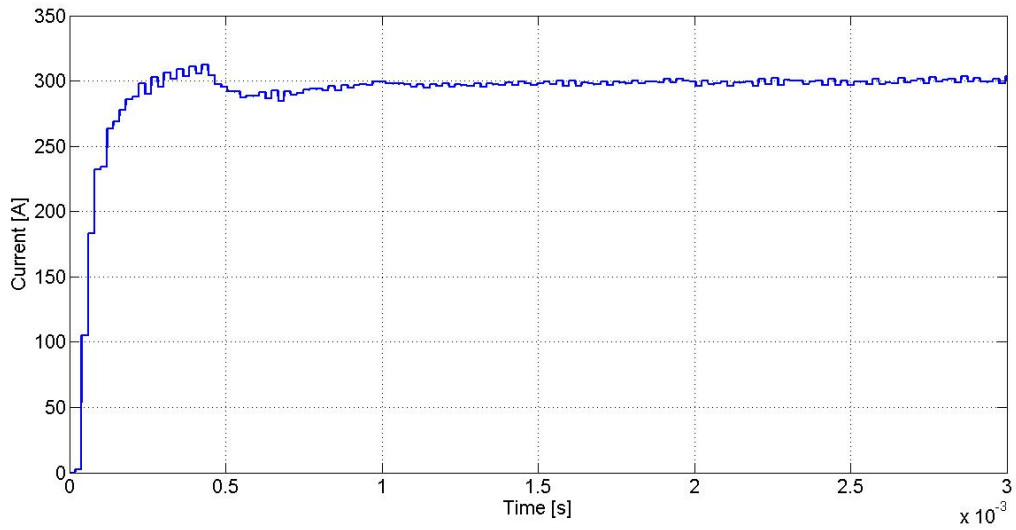


Figure 9.2: The step response with the delayed integral branch.

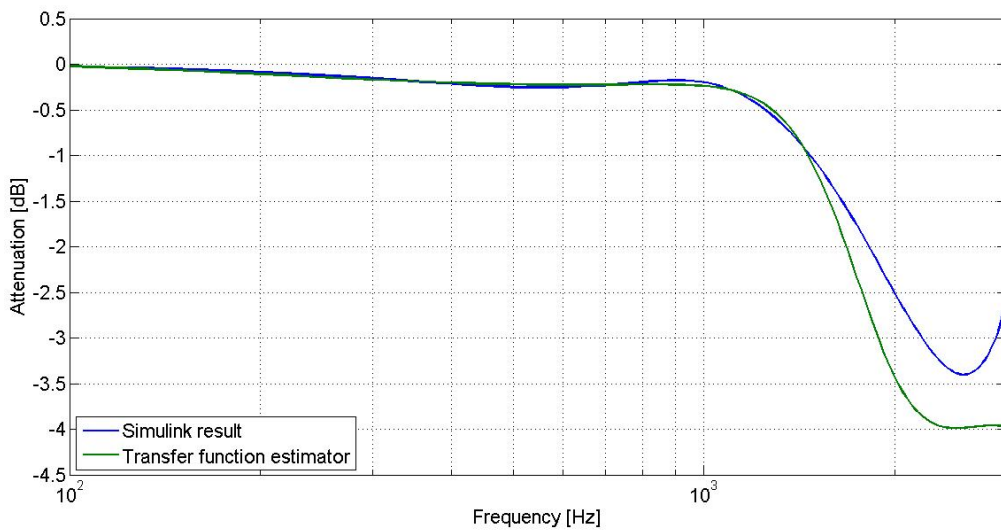


Figure 9.3: The attenuation over frequency with the delayed integral branch: a comparison with the Simulink model results and the transfer function estimation.

be reset only if a reset command is sent, so it has to be initialized outside the PI function. The delayed branch has to see the error values that has been calculated 24 steps before the real-time one. So, at each function call the real-time error sample overwrite the oldest one, leading to a first-in-first-out logic. However, the overwrite command must be executed only after the new reference evaluation. The correct management of the error samples can be done with an index that memorizes which is the next sample to be used for the reference evaluation and then overwritten. It has to be noted that this index must be reset in order to avoid its overflow and that it must be initialized outside the function. So, in the end, the delayed PI only needs little modifications to the original code, which aren't computationally expensive. A guideline example is shown in Fig. 9.4.

```

1  int step_delay=24; // the needed delay is 24 steps;
2  long shift_reg[step_delay]; // shift register;
3  int shift_idx=0; // shift register index;
4  long IntPart=0;
5  long IntPart_del=0;
6
7  //null initialization
8  for(int i=0; i<step_delay; i++) {
9      shift_reg[i]=0;
10 }
11
12 // PI function
13 int PI_delayed(long shift_reg, int err, int step_delay, int shift_idx, int Ki_del ,<other PI parameters such Ki, Kp...> )
14 {
15     long PropPart,Out;
16
17     //proportional and integral computation:
18     PropPart=err*Kp;
19     IntPart+=err*Ki;
20
21     //index overflow control
22     if (shift_idx==step_delay) {
23         shift_idx=0;
24     }
25     //dalayed integral computation
26     IntPart_del += Ki_del*shift_reg[shift_idx];
27     //new error overwrite
28     shift_reg[shift_idx]=(long)err;
29     shift_idx=shift_idx+1;
30     //final output computation
31     Out = PropPart + IntPart + IntPar_del ;
32     return(Out)
33 }

```

Figure 9.4: A guideline example of the needed C code.

# Chapter 10

## Open loop current control

### 10.1 Introduction

As has been shown in previous chapters, the convolution-based model can be used in order to control the system with a sort of predictive controller. Thanks to its precision, it should be able to run the system with an open loop control. So, it is possible to feed the controller only with the current reference signal and then calculate the needed voltage. The main problem of this system is that, theoretically, the anti-Fourier transform of the load impedance is needed. Anyhow, this operation leads to an impulsive response full of numerical errors and noises, that make it useless.

In order to overcome this problem, it is possible to implement a deconvolution algorithm in the model. This solution showed very interesting and promising results, which utilizes the less noisy anti-Fourier transform of the load admittance.

### 10.2 The deconvolution algorithm

As explained before, the discrete convolution is basically a scalar product between two vectors: the forcing term (the voltage in our case) and the impulsive response (multiplied with the time-step  $dt$ ). However, now the known terms are the reference current and the impulsive response. So, the voltage is the unknown term of the equation and the inversion of the scalar product is, therefore needed.

In order to invert the scalar product, one can define the scalar product as:

$$\mathbf{v} \cdot \mathbf{h} = \sum_{j=1}^N v_j h_j \quad (10.1)$$

Where  $N$  is the number of elements contained in the two vectors.

So, defining the voltage at the  $k$ -th step as  $\mathbf{v}_k$  and its elements as  $v_k^j$ , it is possible to write:

$$\mathbf{v}_k \cdot \mathbf{h} = \sum_{j=1}^N v_k^j h^j = i_k \quad (10.2)$$

Where  $\mathbf{h}$  can be the discrete impulsive response with the integration step  $dt$ : by doing this the written scalar product is a discrete integral, i.e. it can be the discrete convolution.

In addition, the voltage vector must be flipped left to right in order to have a discrete convolution:

$$v_k^j = v_k^{N-j} \quad (10.3)$$

In-fact the first element of the vector is the last evaluated voltage. Hence, inside the  $\mathbf{v}_k$  vector the only unknown is its first element  $v_k^1$ . So, the following formula:

$$v_k^1 h^1 = i_k - \sum_{j=2}^N v_k^j h^j \quad (10.4)$$





in order to avoid discontinuities on the reference signal. However, the results showed the presence of a low frequency harmonic (tens of Hz), that makes the amplitudes oscillate: this can be due to numerical noises of the model.

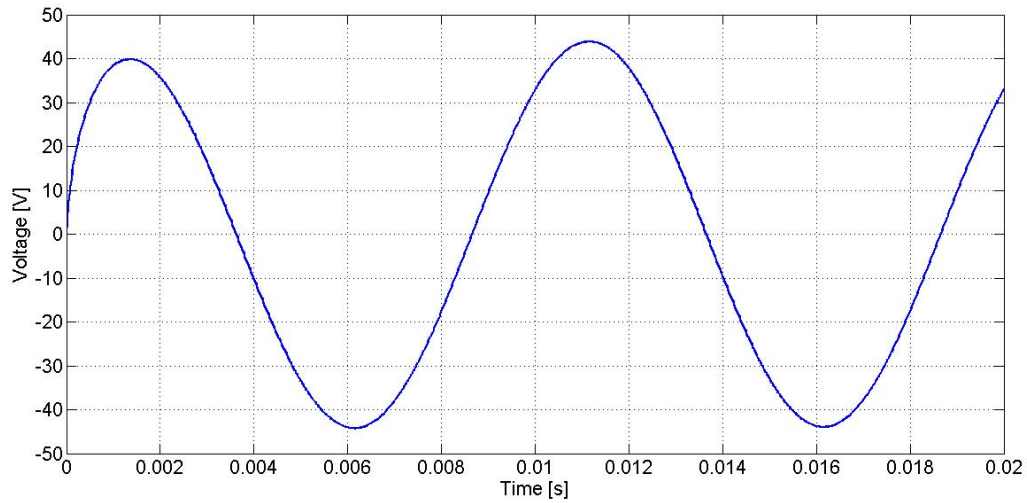


Figure 10.2: The calculated voltage reference, i.e. the output of the deconvolution, with a 300 A and 100 Hz current reference.

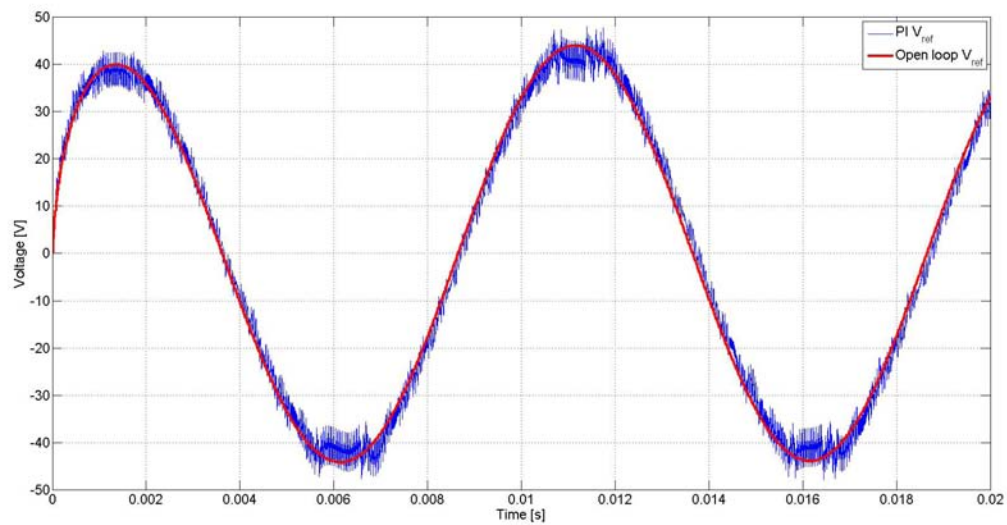


Figure 10.3: The comparison between the voltage reference output from the PI controller ( $K_i = 0.3$ ,  $K_p = 1.35$ ) and the deconvolution output.

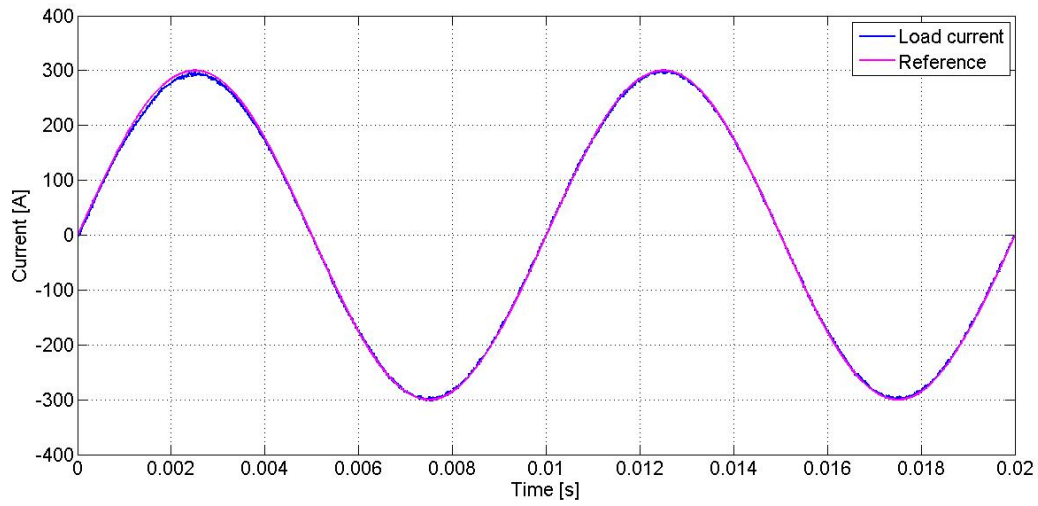


Figure 10.4: Comparison between load current and 100 Hz reference with the proposed open loop control based on deconvolution. The reference and the measured current are nearly perfectly coincident at 100 Hz.

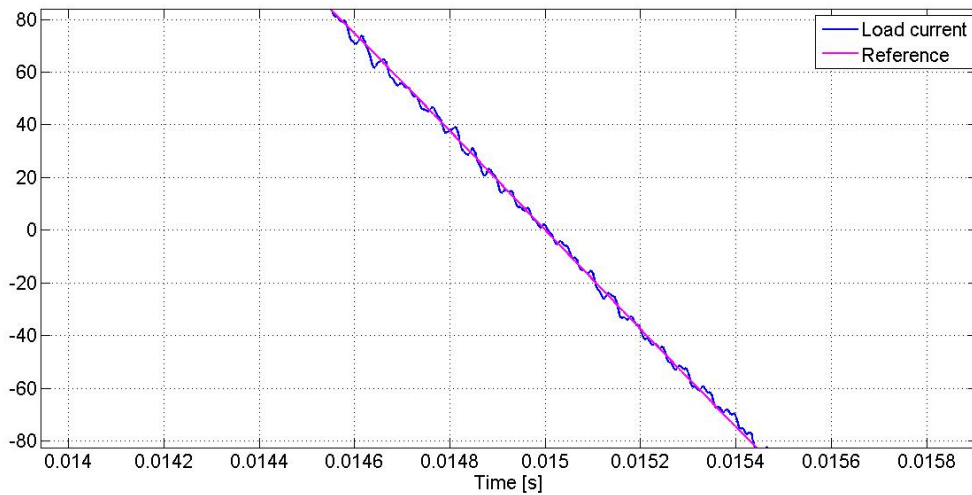


Figure 10.5: A zoom-in of the above figure, during current zero-crossing.

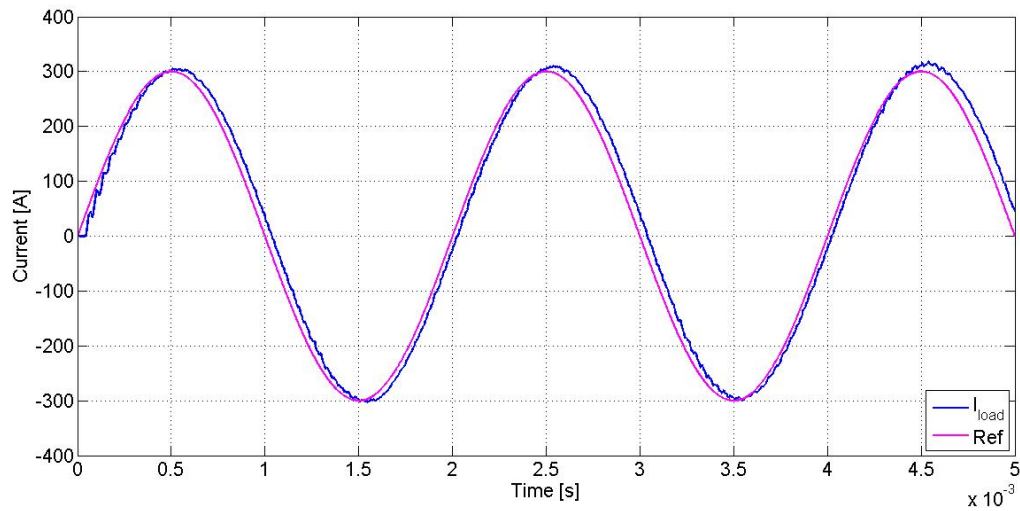


Figure 10.6: Comparison between load current and 500 Hz reference with the proposed open loop control based on deconvolution.

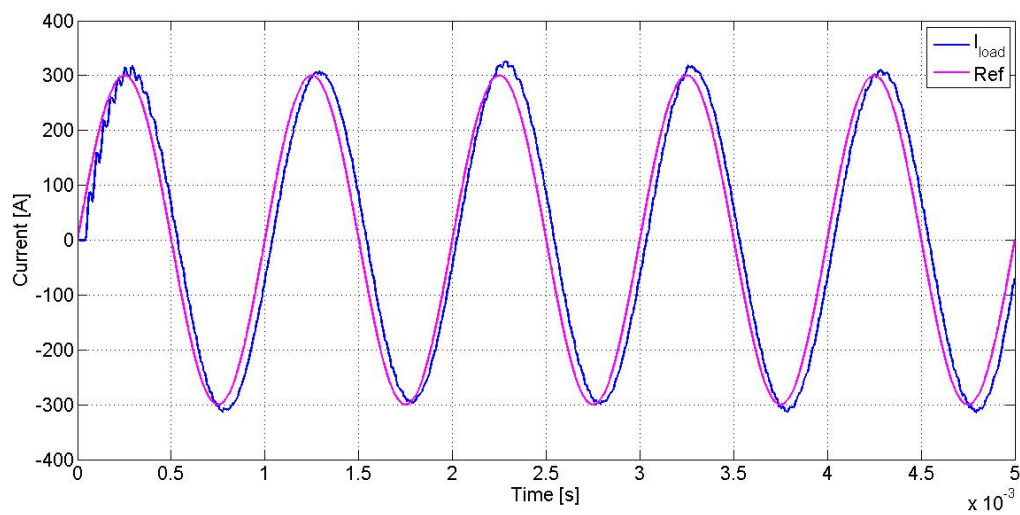


Figure 10.7: Comparison between load current and 1 kHz reference with the proposed open loop control based on deconvolution.

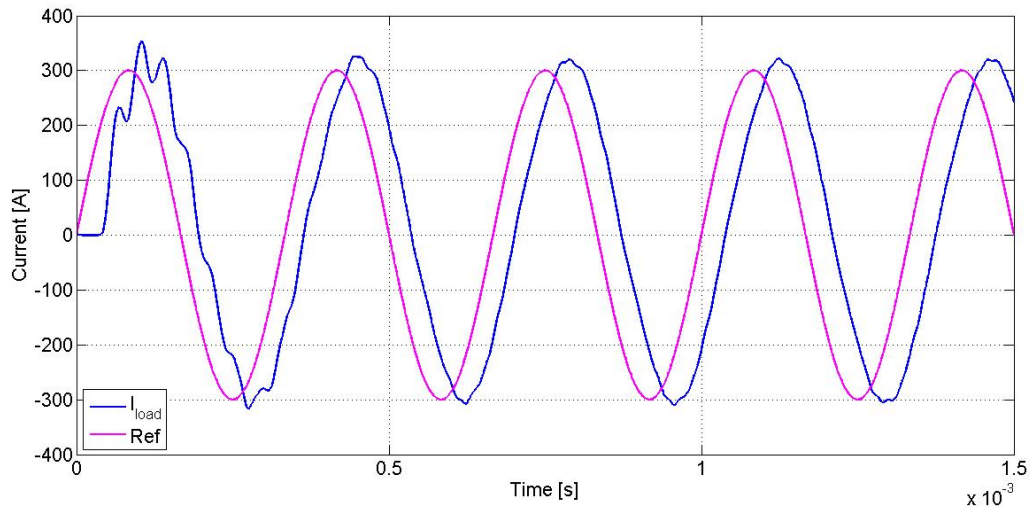


Figure 10.8: Comparison between load current and 3 kHz reference with the proposed open loop control based on deconvolution.

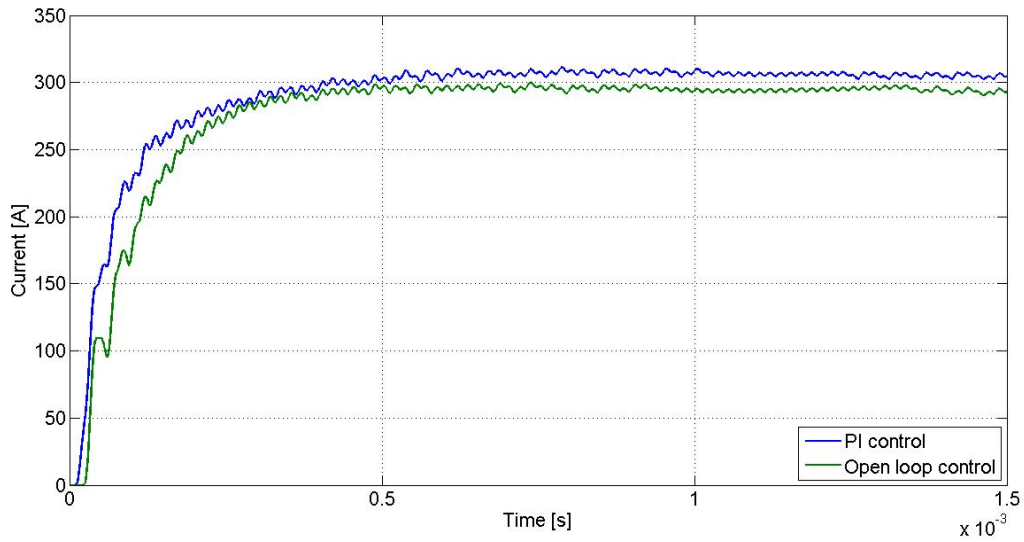


Figure 10.9: The obtained load current with step reference, both with PI control ( $K_i = K_p = 1.7$ ) and the open loop control. The result are very similar, as expected.

## 10.4 Conclusion

In conclusion, further experimental tests, but also analytical studies, should be done. Moreover, it is to be underlined that this is a totally open loop control, which does not know how the system is actually behaving, but it can achieve, or even also exceed, the performances of the closed loop PI controller. However, this control scheme, due to its open-loop nature, may suffer the presence of non-idealities inside the converter itself, such as voltage drops on the switches and the presence of DT; however, probably, these phenomena can be corrected and compensated.

Finally, the deconvolution method can be used in a closed loop controller, which could be able to control precisely also non-linear time-variant systems. Infact, the deconvolution can be used in order to reconstruct iteratively (step-by-step) the impulsive response of the system starting from the measured current and voltage on the load, thus overcoming non-linear and non-predictable effects on the controlled system.



# Chapter 11

## Experimental setup

### 11.1 Introduction

All the experimental tests on the prototype were executed at Consorzio RFX. The objective of this experimental campaign was to validate the convolution model of the dummy load, to verify the performances of the controller with the previously found  $K_i$  and  $K_p$  parameters, to measure the output filter performance and to study other issues of the control system, such as the DT compensation and residual V/I oscillations occurring in some conditions.

In order to do this, we did not need to run the system for long time: short-pulse operations were enough to do all the needed measurements.

### 11.2 Power supply

The DC power supply we used is rated for 500 V and 1 A. So it cannot directly feed the fast converter. So, the power supply charges a capacitor bank at 1 A rate. Then this bank feeds the current needed by the converter.

Obviously, the energy stored in the capacitor bank is limited, so the inverter can work for only few ms. In-fact, the most demanding case is at a 3 kHz, 300 A sinusoidal reference current with an attenuation of 3 dB, that results in 212 A peak. At this frequency the dummy load has a resistance of 372.8 m $\Omega$  and an inductance of 40.0  $\mu$ H, from which results a 8.4 kW absorbed active power, while exchanging 17 kVar of reactive power.

The capacitor bank, shown in Fig. 11.1, is composed by 6 parallel branch, each one having two 15 mF capacitors in series. It results a total capacitance of 45 mF. If they are charged at 300 V (the nominal DC-link voltage), they will accumulate a total energy of 2 kJ. Assuming to discharge the capacitor until 80% of the rated voltage (240 V), the available energy is 730 J, that leads to a maximum pulse duration of 87 ms, which is sufficient for the tests to be performed.

### 11.3 Capacitor discharge circuit

The discharge circuit, as shown in the schematic in Fig. 11.2, is made up of a fixed slow discharge branch and a fast discharge branch inserted by a relay contact. The first is composed by the series of two 1 k $\Omega$  resistors, the second by five 150  $\Omega$  parallel resistor, that make up a total 30  $\Omega$  resistance.

The first branch is able to totally discharge the capacitor bank in 450 s (7' and 30"), while the second in 6.75 s. This setup leads to a peak power on the first branch of 45 W, that is less than the 200 W nominal power of the resistor, and 3 kW on the second one. Note that in the second branch the power is divided on the five resistances, so we have 600 W for each one and only for a brief pulse. The resulting system is pictured in Fig. 11.3.

The test of this setup went ok, without any overheating of the system, even at 300 V.

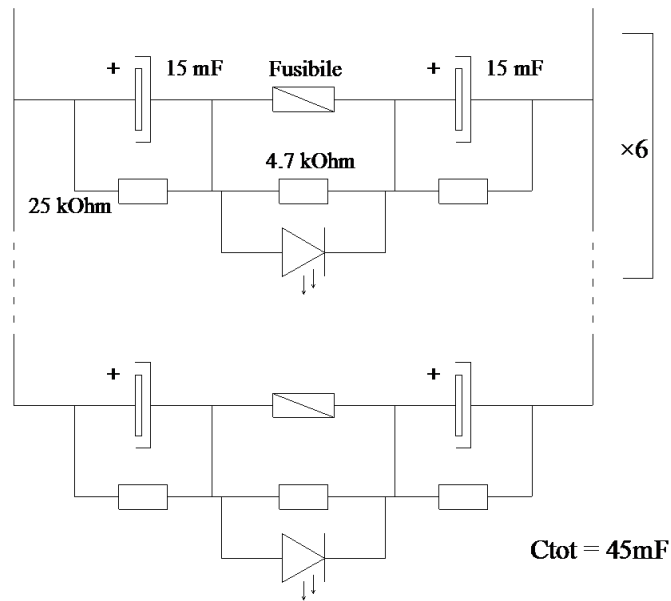


Figure 11.1: The scheme of the capacitor bank used in the test bench.

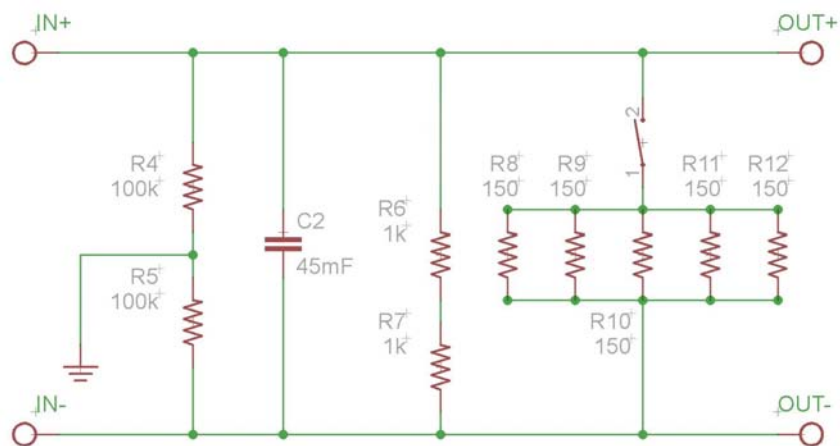


Figure 11.2: The scheme of the discharge circuit for the capacitor bank used in the test bench.



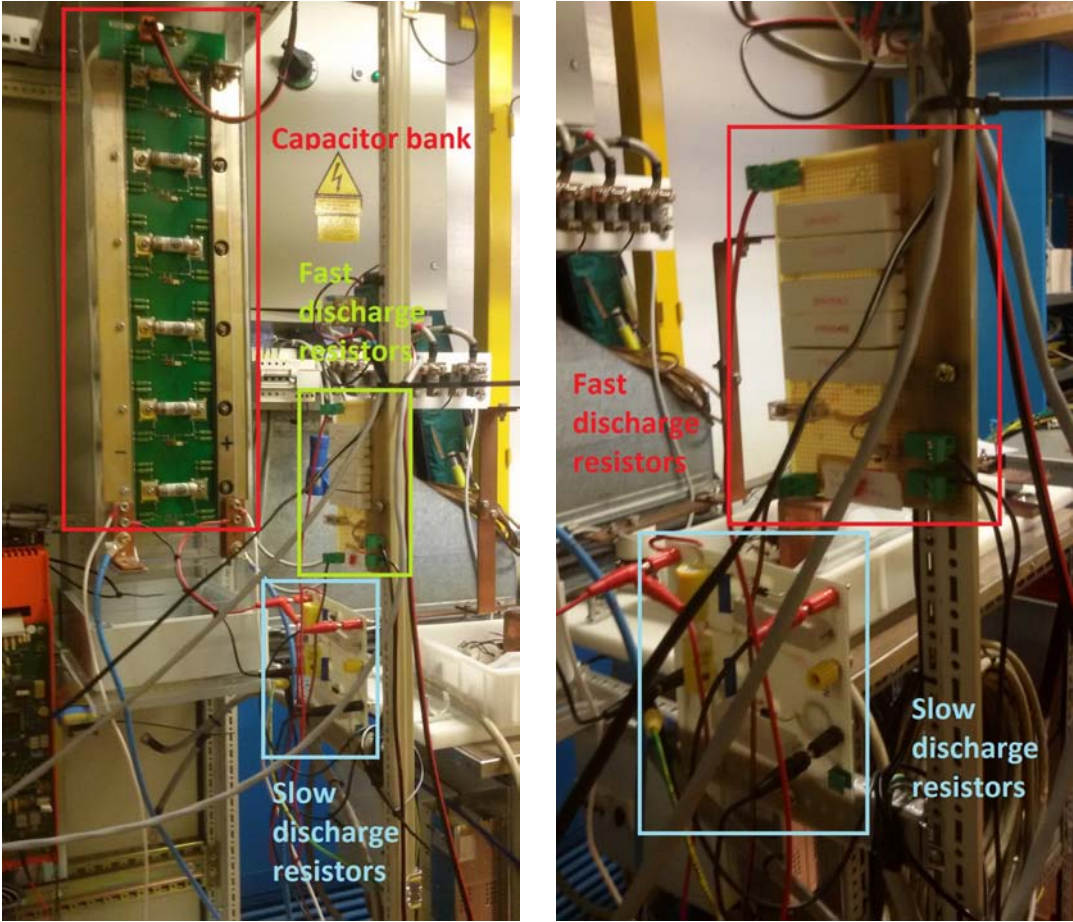


Figure 11.3: The DC-link setup at Consorzio RFX, with all the main parts underlined.

## 11.4 Grounding

The grounding system has been developed in order to half the potential of the two DC bars with respect to ground. So, the grounded clamp is positioned between two 100 k $\Omega$  resistors in a transversal branch. In this way we have the positive bar at +150 V and the negative one at -150 V, with respect to ground. The grounded clamp is connected to the plant ground network at which also all the auxiliaries of the inverter and the power source are connected.

The load and the output side of the converter are, instead, left floating.

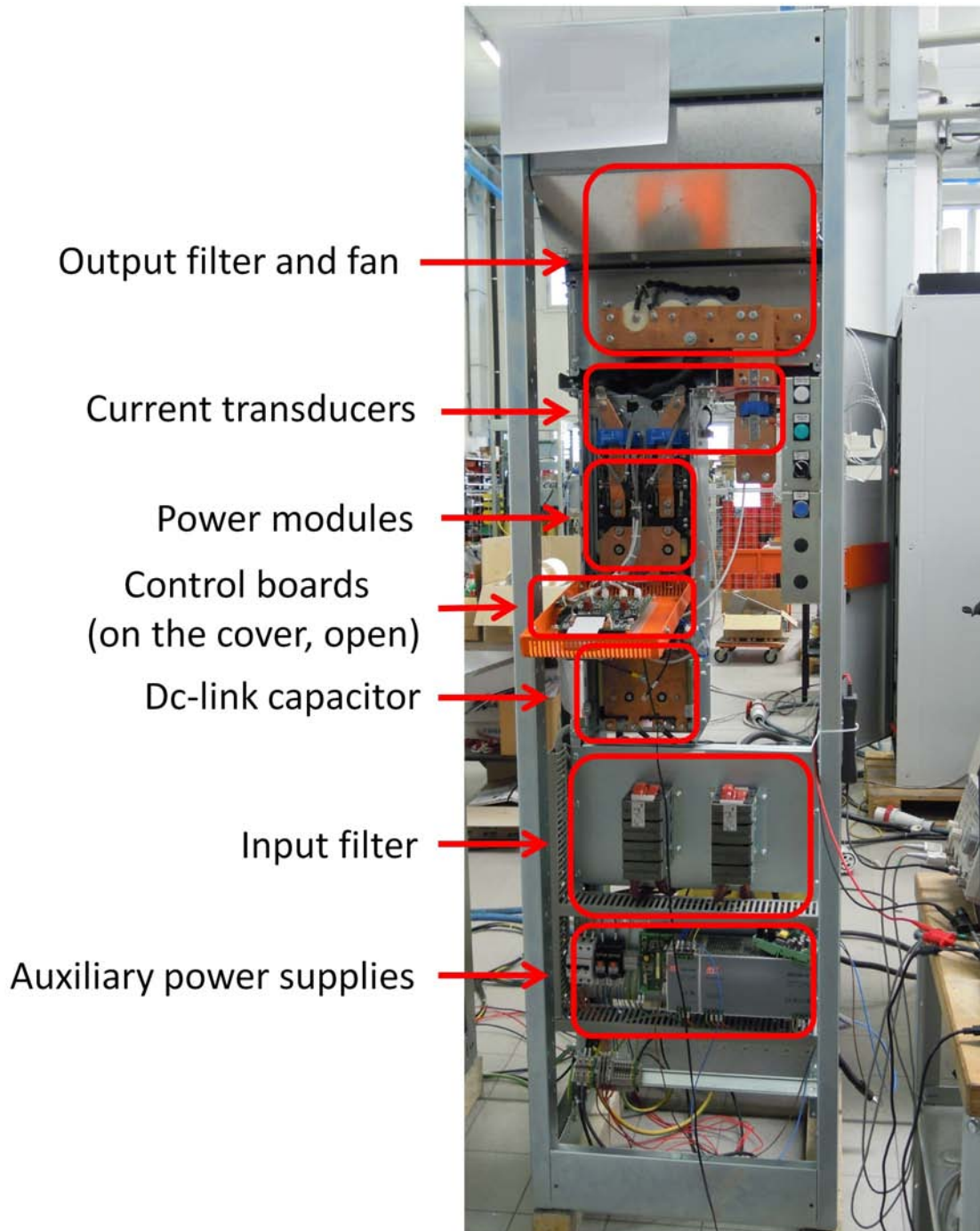


Figure 11.4: A photo of the used prototype, where its main parts are well underlined.

# Chapter 12

## Model validation with experiments

### 12.1 Introduction

All the experimental tests were performed with the setup described in the previous chapter and with the dummy load connected.

The first objective of the experimental campaign is to validate the simulation results obtained with the convolution-based model. Two tests have been carried out:

1. voltage step response in VCM;
2. frequency characterization in CCM;

The first one is necessary in order to validate the load model. The second one, instead, is needed in order to validate the controller model. In evaluating the frequency responses, it has to be taken into account that the dummy load has a different behavior from the real RWM-CC load, although similar.

### 12.2 Voltage step response

The experimental data were taken setting the converter to VCM and then applying a 1 kHz square wave as reference with a 100 V amplitude, in order to avoid high current on the load. Also, all the possible compensations, such as voltage drops on the switches and on filter inductances, were disabled. Then we measured the applied load voltage and the load current, both averaged with a  $16.67 \mu\text{s}$  step. The measurement are shown in Fig. 12.1.

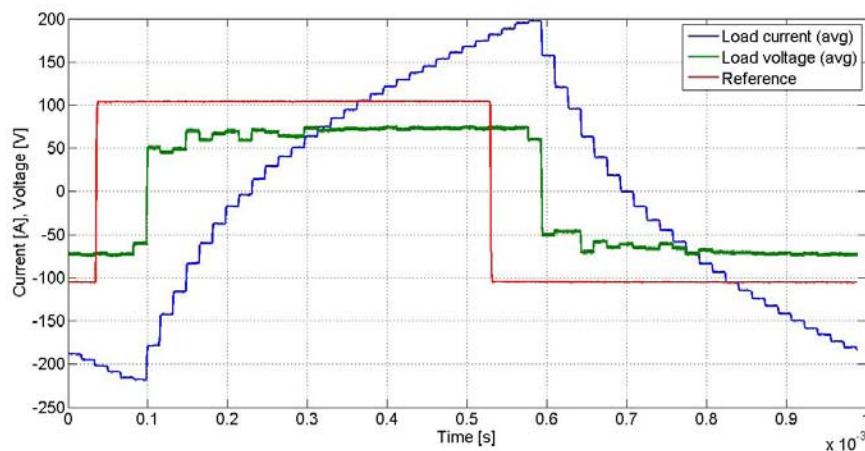


Figure 12.1: The measured measured voltages and currents with voltage step reference and dummy load connected, in VCM.

Then, the measured load voltage has been used to run a Simulink® model, shown in Fig. 12.2, which is composed by a controlled voltage source and the convolution-based model, all run with a 250 ns time-step. Apart from a certain off-set on the current, due to some transient component, the model shows really satisfactory results, as can be seen in Fig. 12.3, where a comparison between the two current waveforms has been made.

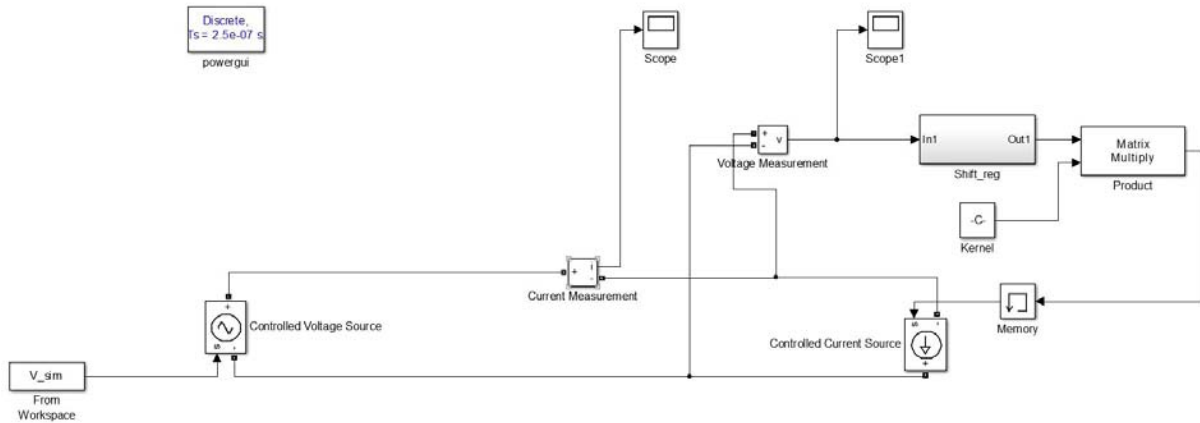


Figure 12.2: The used model.

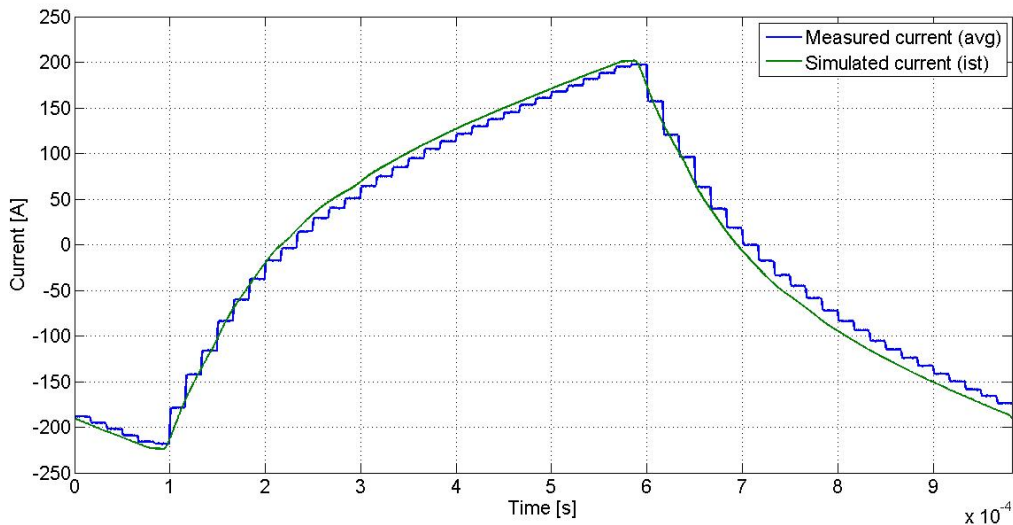


Figure 12.3: The comparison between the measured current and the simulated one, with voltage step reference and dummy load connected.

### 12.3 Frequency characterization

All the subsequent tests had been done in CCM with 100 A current peak with 50, 100, 300, 500, 1000, 3000, 5000, 7000 Hz sinusoidal references. The 100 A amplitude has been chosen due to energy limitations of the DC-link and also in order to avoid over-temperature on the switches (the cooling system is air based, while the final cooling system will be water based).

Three  $K_i - K_p$  couples have been chosen:

1.  $K_i = 0.3$ ,  $K_p = 1.35$  (EEI parameters);
2.  $K_i = 4$ ,  $K_p = 1.13$ ;
3.  $K_i = 1.7$ ,  $K_p = 1.7$ .

The last two couples showed promising results in simulations: the second one has been chosen due to the behavior at 1 kHz and 3 kHz with the dummy load connected, while the third one has been chosen because showed the best results with the real RWM-CC load. The three obtained characteristics are shown in Fig. 12.4.

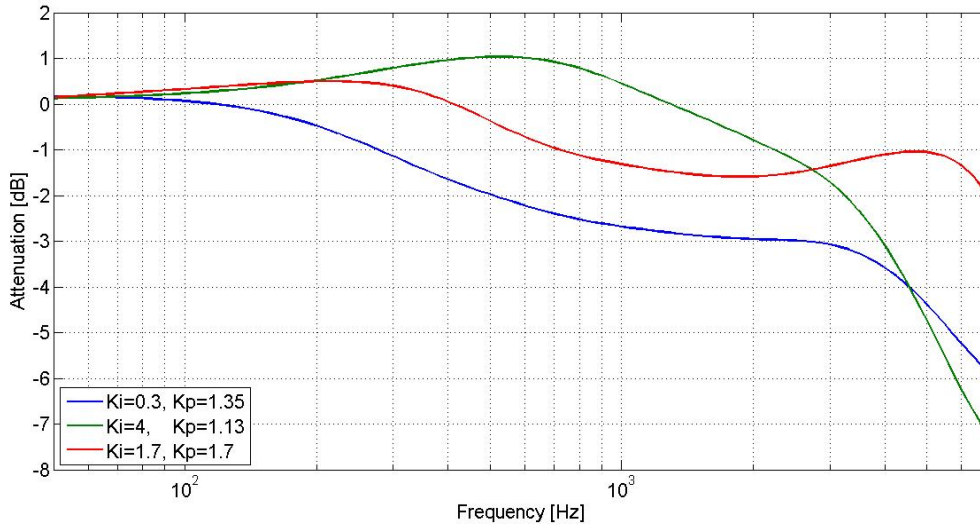


Figure 12.4: The comparison between three experimental frequency characteristics, in CCM, 100 A peak, with dummy load connected, from 50 Hz to 7 kHz.

The first thing that has to be noted is that the hardware itself can certainly match all the given dynamic specifications, that are 1 dB of attenuation at 1 kHz and 3 dB at 3 kHz. So, the compliance with the specifications is just a matter of controller optimization. The second thing that can be noted is that increasing the  $K_i$  parameter also the resonance peak seems to increase and shift to higher frequencies.

## 12.4 Comparison with the model

The model used for the comparison is the convolution-based one, where the impulsive response is sampled at 1  $\mu$ s time-step, while the rest of the model runs at 250 ns time-step : this set has been chosen in order to speed up the simulation time, while it does not impact significantly the results. In Fig. 12.5 the results are shown.

Firstly, at high frequencies (more than 1 kHz) the model tends to underestimate the load current: in-fact three things must be taken into account:

1. in the used model there is not any DT and DT compensation system;
2. in the model the control section runs at the simulation step time (250 ns), while in the real system it runs with a 60 kHz rate;
3. in the real system the controller has as input an averaged current, while in the model it has the instantaneous one.

In-fact, using the model with the DT compensation algorithm, the results are better, as shown in Fig. 12.6, with lower current error at high frequencies, depending on the  $K_i$  and  $K_p$  couples used. In-fact, the characteristic made with lowest  $K_i$  shows an over-estimation of the current from 200 to 2000 Hz, while the one with the highest  $K_i$  showed an under-estimation of the current in the same frequency interval. So,

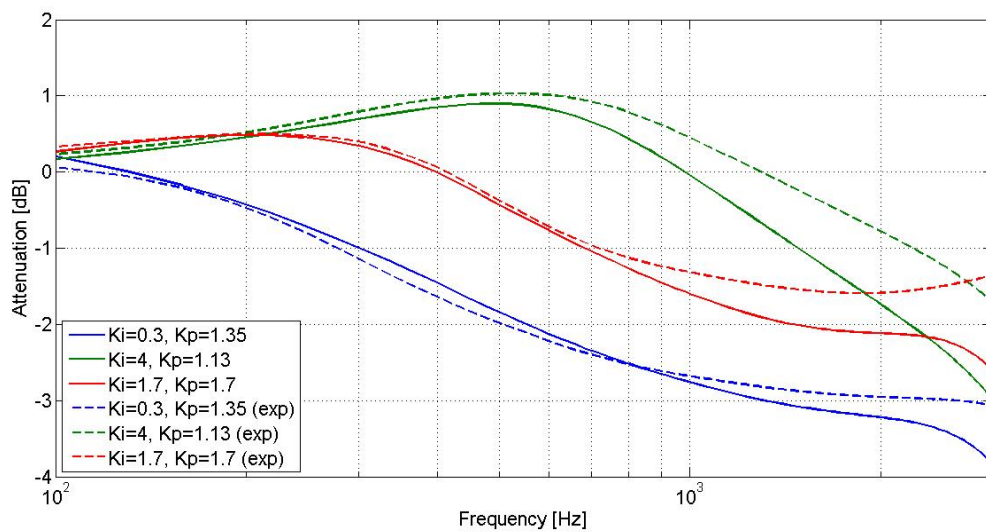


Figure 12.5: The comparison between the convolution-based model and the measurements in CCM with the previously cited PI parameters and dummy load connected.

the choice of control parameters influences the accuracy of the model. However, the experimental results showed anyway a behavior similar to the simulated ones, confirming the effectiveness of the PSO-MO algorithm.

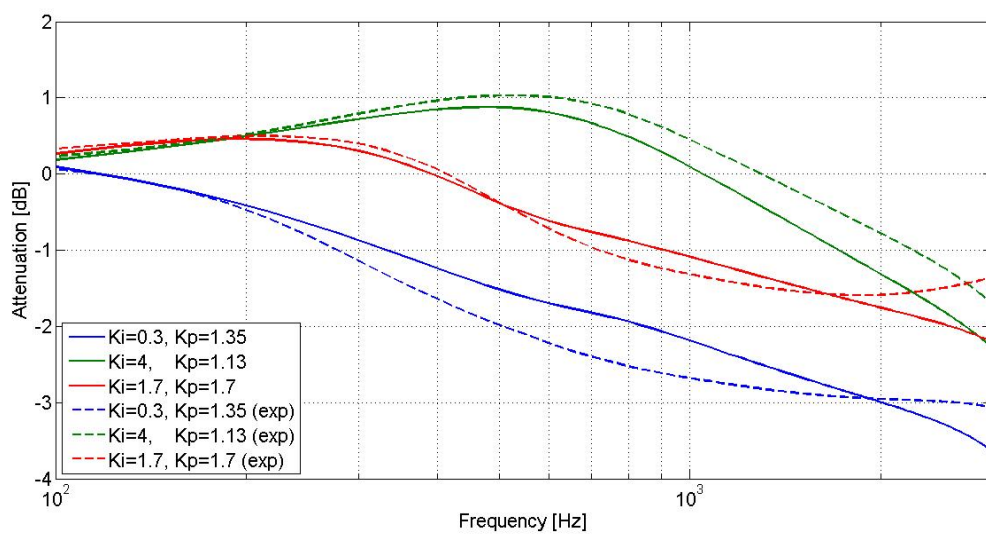


Figure 12.6: The comparison between the model and the measurements with the DT correction algorithm.

# Chapter 13

## Filter optimizations

### 13.1 Introduction

As described in chapter 5 the filter was designed in order to be transparent at low frequencies, however a certain voltage overshoot occurs in the step response. In addition, smaller voltage derivatives than those found experimentally would be preferred. The highest voltage overshoots would occur if, for whatever reason, the gates of the switches are cut-off while the converter is applying full voltage. So, some hardware modifications of the filter will be proposed in order to solve such issues .

### 13.2 Measurements

In order to better characterize the filter, some measurements of the instantaneous load voltage have been done. In particular, the overshoot phenomena has been put in evidence by tuning the load current limit in the FPGA: in-fact, if the current exceeds such limit, the FPGA suddenly cut-off all the gates signals. So, the current limit has been set so that the protection is activated when the load voltage is about 300 V, with, also, high current (close to 300 A). The result is shown in Fig. 13.1.

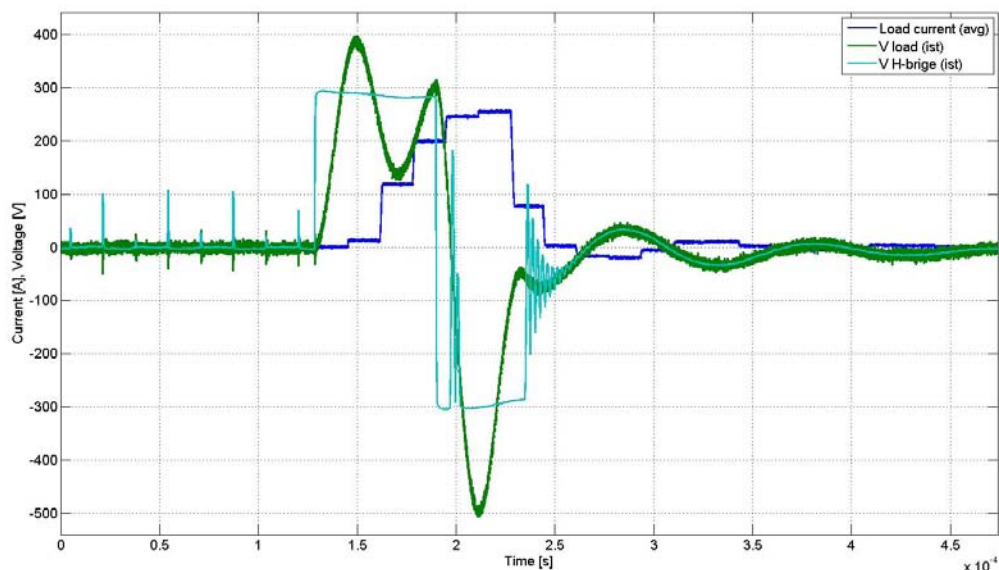


Figure 13.1: The measured voltage oscillations at gate cut-off, in VCM.

It can be seen how the voltage peak reaches and may exceeds 500 V, thus remaining under the requested

maximum voltage peak of 550 V. In addition, a voltage derivative with a peak of about 63 MV/s has been measured. So, it would be desirable to reduce the voltage stresses on the load.

### 13.3 Test models

Two models have been used, which both simulate the load with the convolution-based model. The first one has been used in order to replicate the measured data. So, a controlled voltage source is used in order to feed the system with the measured voltage itself, obtaining the results shown in Fig. 13.2.

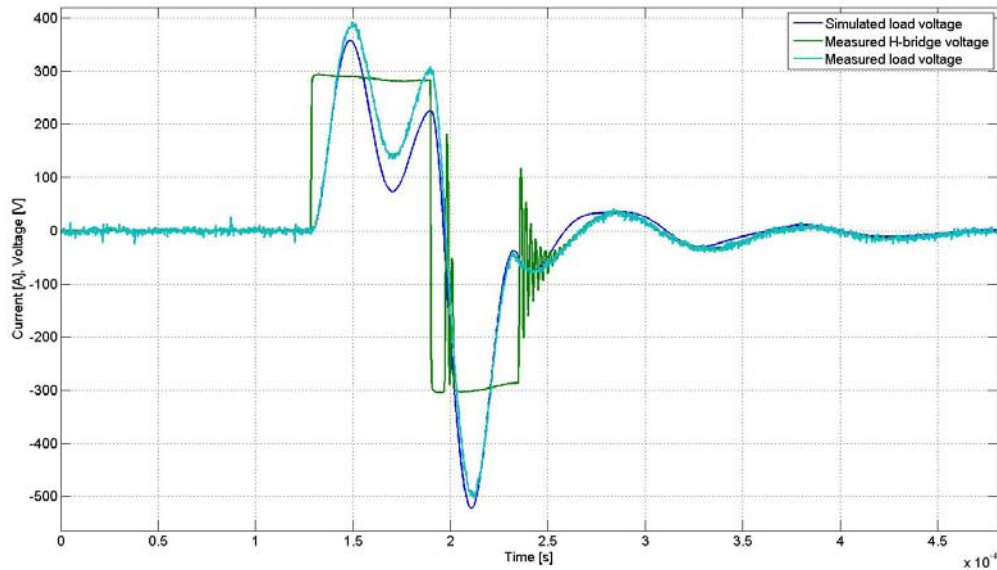


Figure 13.2: The comparison between the measured load voltage and the simulated one at gate cut-off.

As it can be noted, the simulated voltage has some difference from the measured one in particular during the initial phase, probably due to some parasitic effects on the filter (as the inductance resistance) and due to the fact that the voltage source is ideal and it can feed the system with whatever current, while the real system includes also an input filter and shows other voltage drops on the switches. However, the model replicate with great precision the voltage peak, even if the 20 kHz oscillations are not well replicated, due to the reduced precision of the model at high frequencies.

The second model, instead, is used as a benchmark, thanks to its ability to replicate the worst case, i.e. a voltage step from +300 V to -300 V with an initial 300 A current and the subsequent H-bridge voltage oscillation caused by the current zero-crossing. The system, which is quite complicated, is pictured in Fig. 13.3.

Substantially, in this model there are three main parts:

1. the power section: the load with the filter and the controlled voltage source;
2. a Matlab® function which, basically, replicate the behavior of the diodes of the H-bridge while the IGBTs are off: it impose +300 V when the filter inductance current is negative and -300 V with positive current;
3. a system (i.e. all the remaining blocks) which recognizes when both the load voltage and the load current are near 300 V and the 300 A threshold, respectively needed to trigger the gate cut-off dynamics.

With this model good results have been obtained, as shown in Fig. 13.4, where, in particular, the initial dynamics and the voltage peaks are well replicated, obtaining a voltage peak of about 550 V and a maximum voltage derivative of 64.4 MV/s with the original filter.



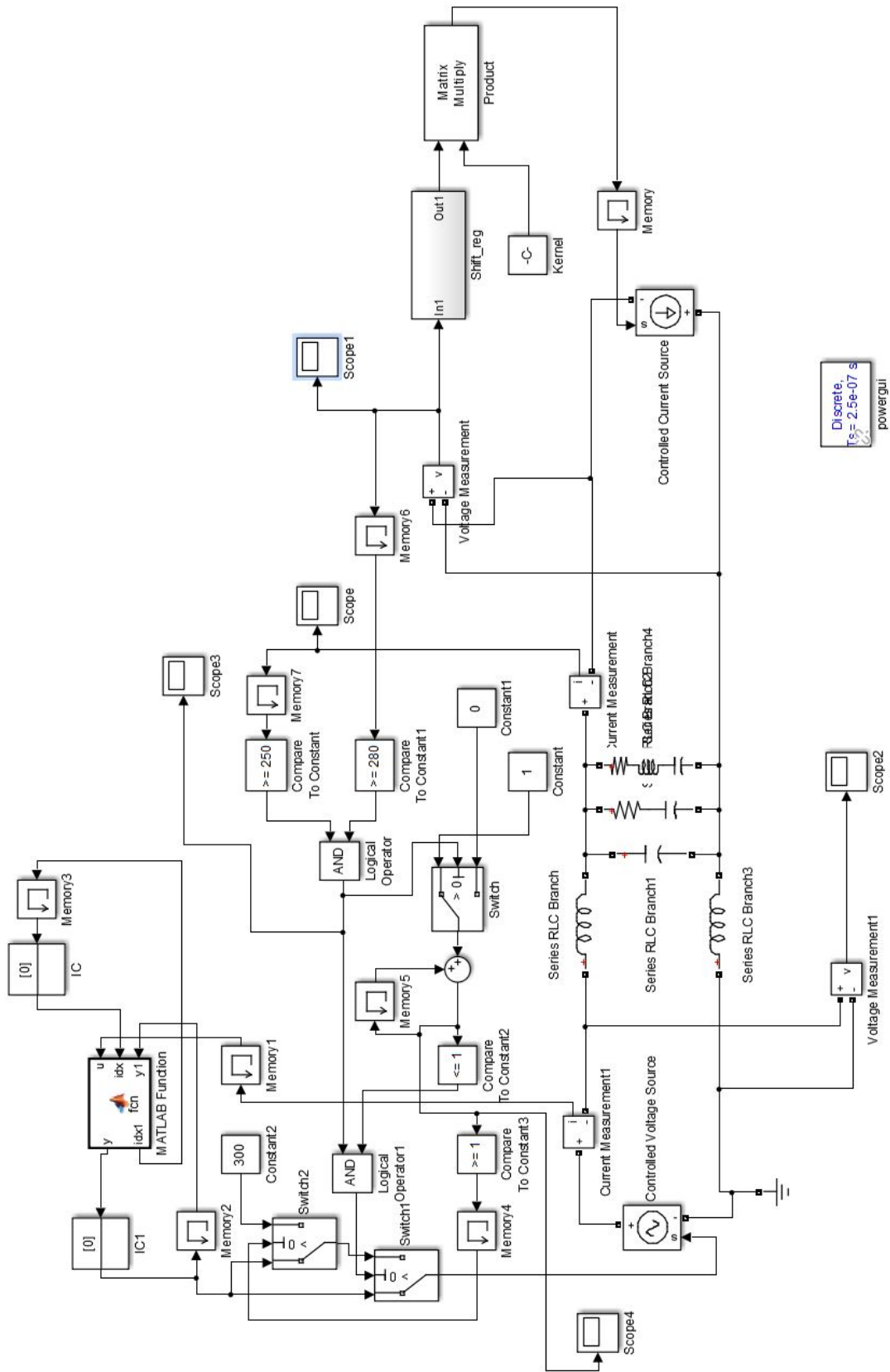


Figure 13.3: The benchmark model of fast converter and output filter, used to find the highest voltage overshoot.

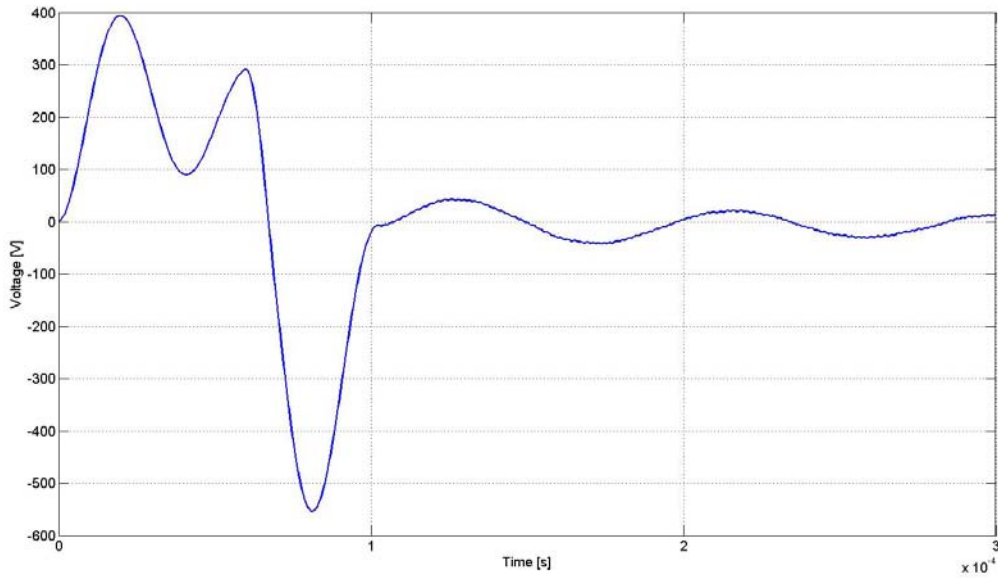


Figure 13.4: The benchmark model results with the present filter of the prototype.

### 13.4 RLC damping branch

Firstly, in order to lower the voltage derivatives, it is possible to increase the value of the transversal capacitance. From the convolution-based model of the converter with RWM-CC (Fig. 6.1), it resulted that just a little increase of the capacitance value would reduce the voltage derivative. In-fact with a  $5 \mu\text{F}$  capacitance the maximum voltage derivatives decreased from  $20 \text{ MV/s}$  to about  $15 \text{ MV/s}$  with a  $3 \text{ kHz}$  sinusoidal current reference, as can be noted in Fig. 13.6.

By the way this change has led to a little worsening of the overshoot in the current step response. Furthermore, simulations showed an increased value of the  $20 \text{ kHz}$  voltage harmonic of the step response, that is about the resonant frequency of the filter. In order to correct this effect, a resonant LRC transversal branch has been studied. In-fact, starting from the existing damping branch, it is possible to add a series inductance to the branch, making it resonates at  $20 \text{ kHz}$ . Considering the existing  $2 \mu\text{F}$  capacitance and a resonance frequency of the modified LC dipole of  $20.5 \text{ kHz}$ , it results a  $30 \mu\text{H}$  inductance. The so obtained filter topology is pictured in Fig.13.5.

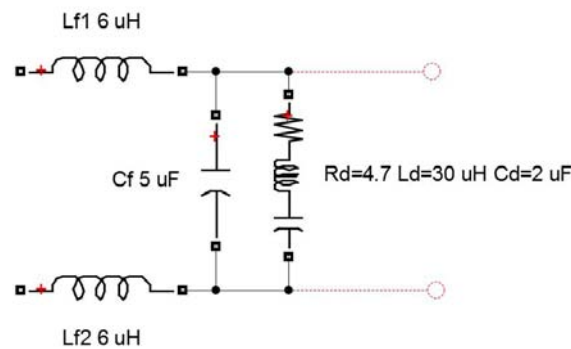


Figure 13.5: The proposed filter with increased capacitance  $C_f$  and with additional inductance  $L_d$ .

In the end, the described hardware modification lead to:

- reduced voltage derivative at  $3 \text{ kHz}$  to  $10\text{-}15 \text{ MV/s}$ ;

- limited current overshoot at step response: circa 10-12 A;
- performance at other frequencies untouched in CCM: no modifications of the controller parameters are needed.

The only drawback of this modification is the large inductance that has to be added to the system, that also increases the overall losses. By the way, if an ideal damping inductance is assumed, on the damping resistor  $R_d$  a lower current is obtained with a 3 kHz sinusoidal 300 A current reference: in-fact a 9 A peak current is detected on the resistance, instead of a 12 A peak with the original filter topology.

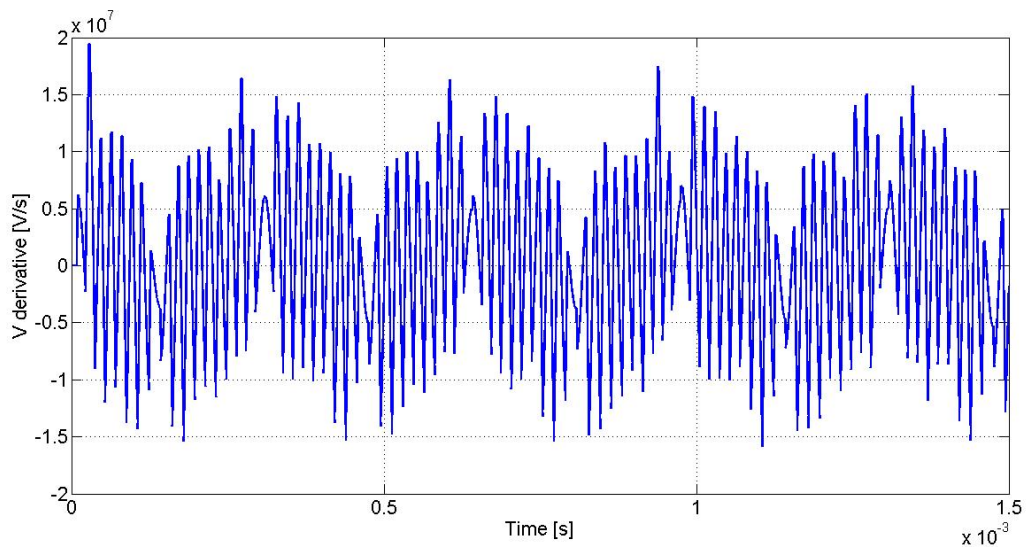


Figure 13.6: The derivative of the voltage at 3 kHz, 300 A, in CCM and  $K_i = K_p = 1.7$ .

In the gate cut-off event simulation, the new filter obtained interesting results, with a reduction of the voltage peak of about 50 V and a maximum voltage derivative of 60.6 MV/s, as can be seen in Fig. 13.7.

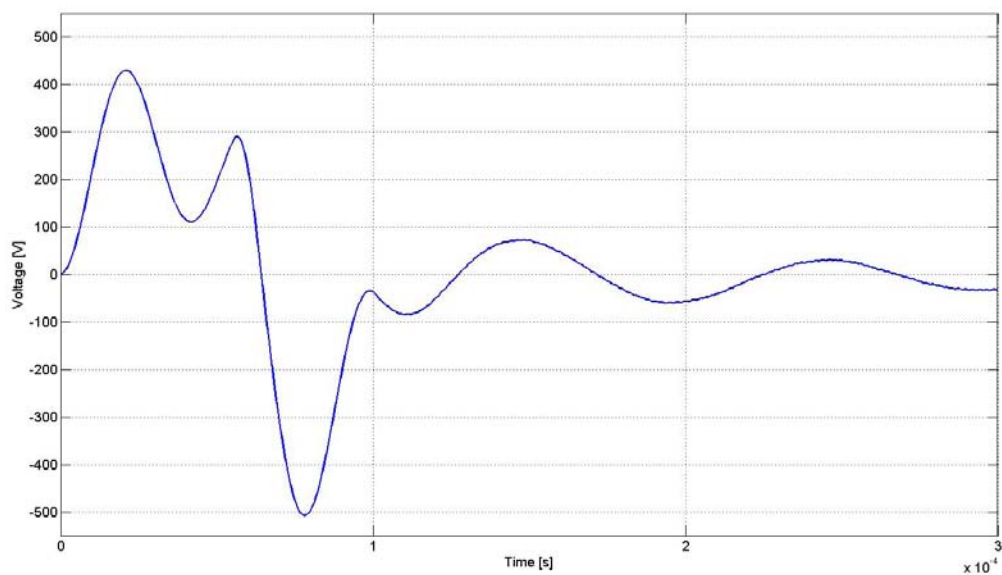


Figure 13.7: The result obtained the model in of Fig. 13.3, with the filter proposed in Fig. 13.5.

### 13.5 RLC resonant branch

Another possible solution is to add to the actual filter, with only the filter capacitance upgraded to a  $5\ \mu\text{F}$  one, another RLC resonant branch in parallel, as shown in Fig. 13.8. This resonant branch has been originally proposed by ing. A. Ferro.

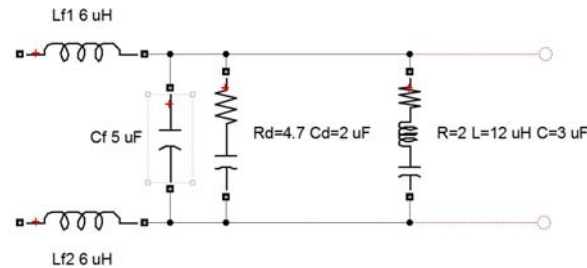


Figure 13.8: The proposed filter with increased capacitance  $C_f$  and with additional resonant branch.

Also this filter has been designed with a resonant frequency similar to the one of the original filter and it does not require to modify the controller parameters.

In the gate cut-off simulation this filter showed a further improvements over the above solution, as shown in Fig. 13.9.

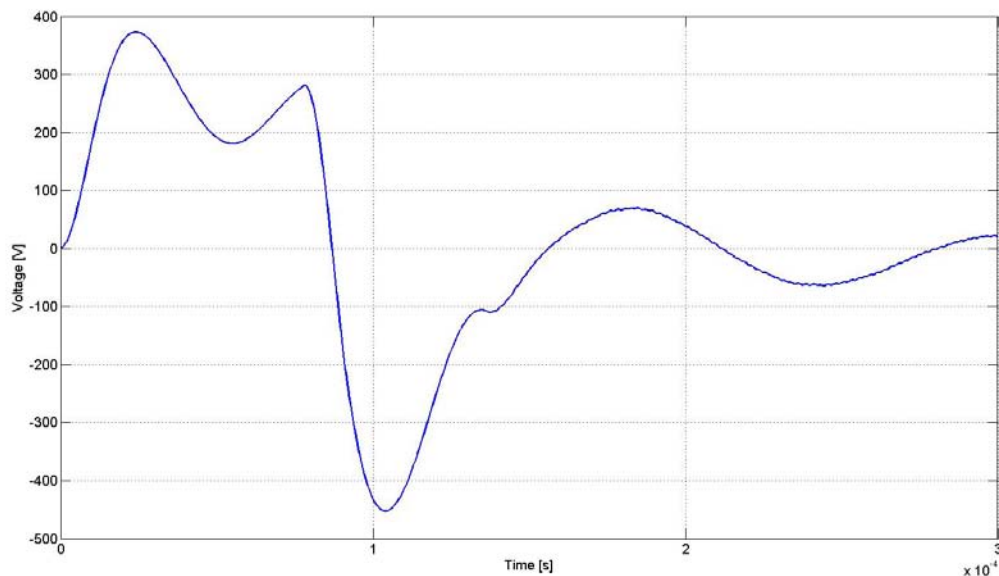


Figure 13.9: The result obtained with the model of Fig. 13.3, with the filter of Fig. 13.8

Note how the voltage peak is reduced to about 450 V and the maximum voltage derivative is 51.2 MV/s. However, in simulations with CCM and a 300 A and 3 kHz current reference made with the model pictured in Fig. 6.1, it has been found on the resonant branch resistance a repetitive current peak of more than 20 A, which can lead to more than 800 W power peak on the resistance, which may be difficult to manage. In-fact, these losses have to be added to the ones on the original damping resistance.

A cumulative graph with all the simulated losses on the filter resistance can be seen in Fig. 13.10 and 13.11.

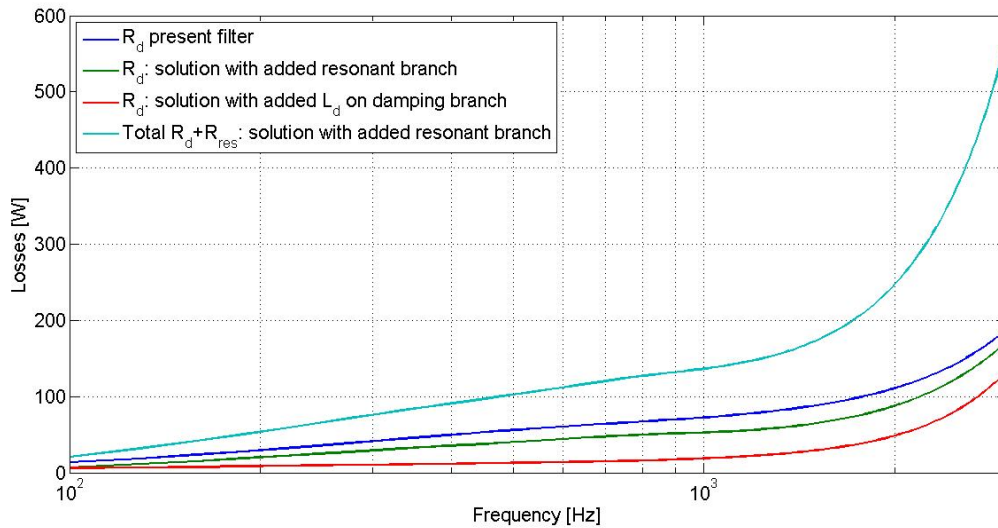


Figure 13.10: The estimated losses on the filter resistances. In particular, for the filter with the additional RLC resonant branch also the sum of the losses on the two resistances are shown.

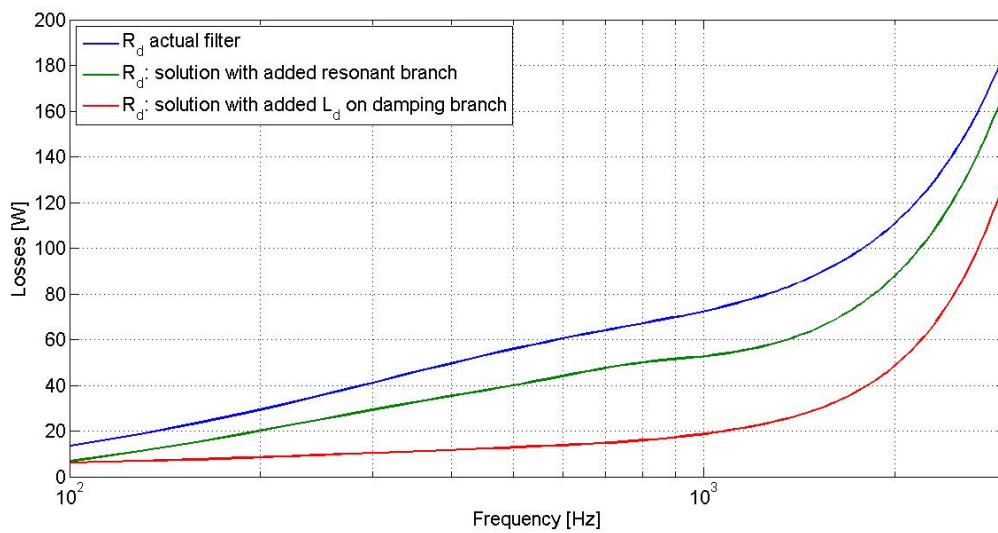


Figure 13.11: The estimated losses on the damping resistance  $R_d$  only.

## 13.6 Filter on analog reference

In order to reduce the load voltage overshoot at VCM step reference, one way is to filter up the reference. In this way the inverter do not impose immediately the nominal 240 V voltage on the load, thus reducing voltage oscillation. The filter on the reference is necessary also to cut-out possible harmonic components of the reference above 3 kHz and to limit the power dissipated on the damping resistance of the output filter. The reference is filtered by a first order low-pass filter, which has been implemented in the converter master control board with the analog circuit shown in Fig. 13.12. In the Simulink® model, instead, it has been inserted with the subsystem shown in Fig. 13.13. The resulting reference is shown in Fig. 13.14.

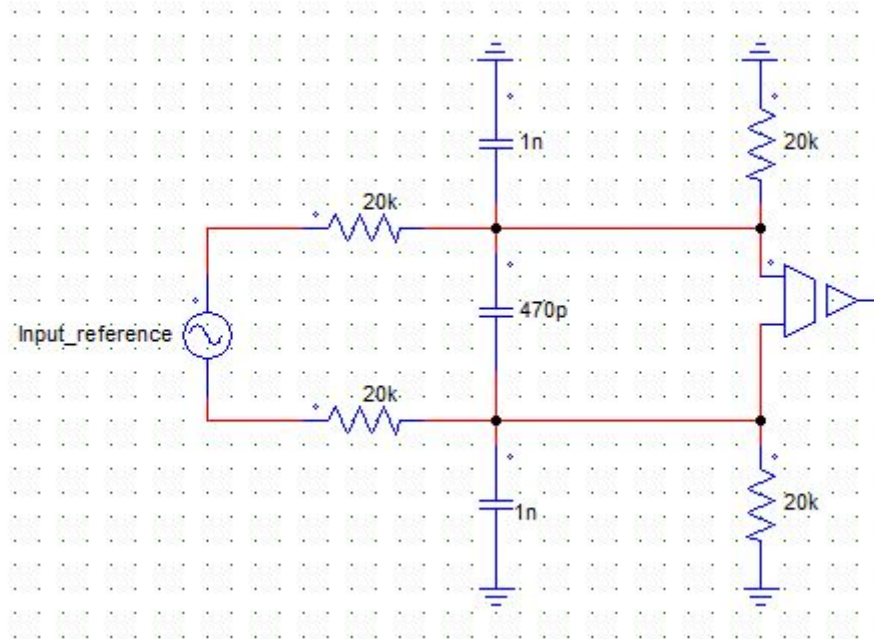


Figure 13.12: The low pass filter as implemented by EEI in the MCB.

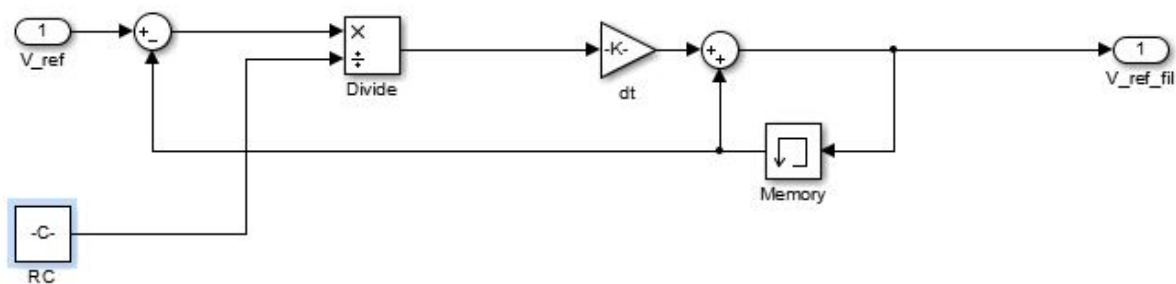


Figure 13.13: The low pass filter as implemented in Simulink®.

The subsystem time constant has been chosen keeping in mind that:

1. the low pass filter can slow down the overall system dynamics;
2. if the time constant is too low, the voltage overshoots and the power dissipated on damping resistors are not reduced;

A  $18.8 \mu\text{s}$  time constant has been chosen by EEI.

Simulations, made with the convolution-based model, show that the overshoot is mainly canceled, even

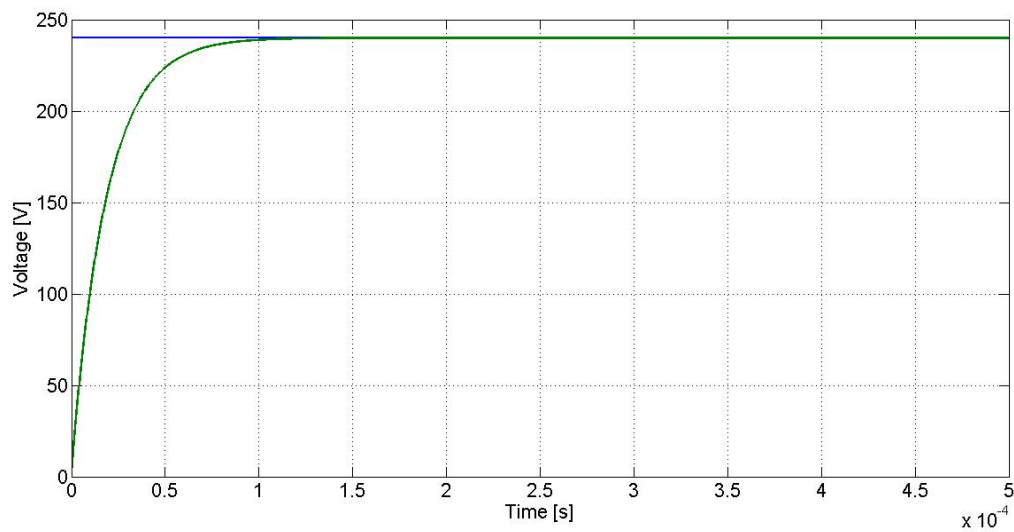


Figure 13.14: The obtained filtered reference.

without any filter modification, as can be noted in Fig. 13.15. Obviously, this filter can not do anything in the case of gate commands interruption. For this case only a modified filter topology can reduce the overvoltage.

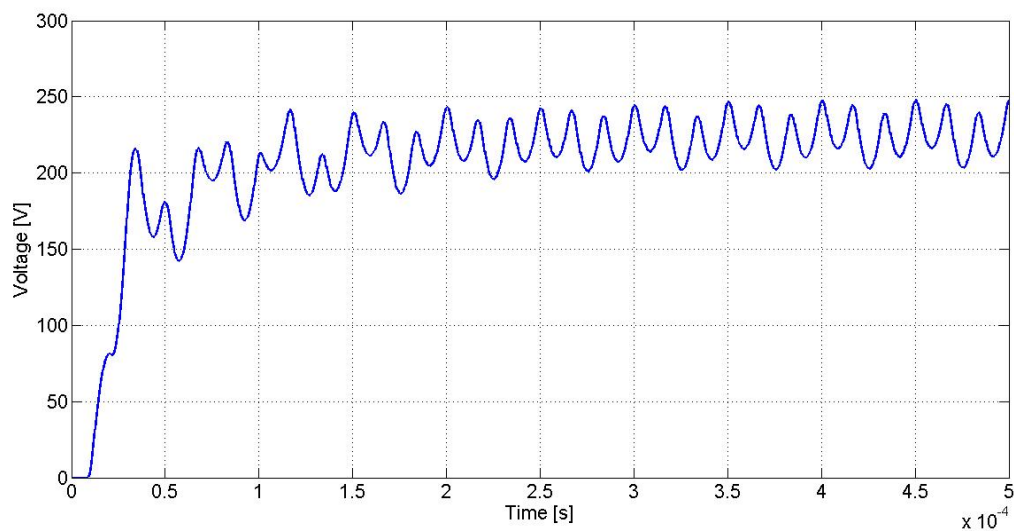


Figure 13.15: The obtained voltage step response on the load, in VCM with a 240 V step reference.

In addition, in all the studied filter modifications, the voltage derivatives on the load were always much more higher than what has been requested in the specifications. So, maybe, another type of protection should be investigate, if possible, which cuts off the voltage on the load in a controlled way.





# Chapter 14

## DT correction effects

### 14.1 Introduction

As it has been described in previous chapter, a misbehaving of the DT correction algorithm has been detected during current zero-crossing, both in the Simulink® model and in measured data, leading to a little current distortion. In order to further investigate such phenomenon, which can be seen in Fig. 14.1 and 14.2, the model has been improved implementing also the RC snubbers ( $R_s = 1.65 \Omega$ ,  $C_s = 20 \text{ nF}$ ) of the switches, because they have an impact in the current waveform close to zero-crossing. .

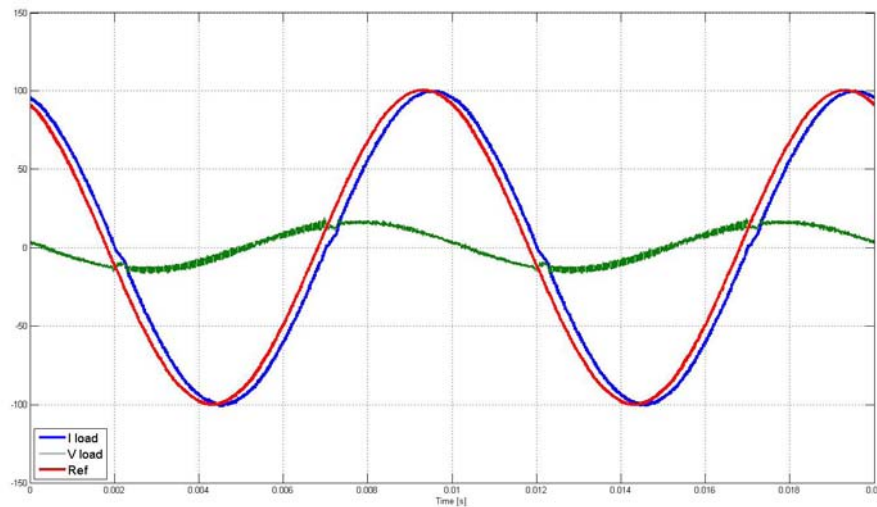


Figure 14.1: The measured load current, in CCM with sinusoidal 100 A (peak) current reference,  $V_{DC} = 300 \text{ V}$ ,  $K_i = 0.3$ ,  $K_p = 1.35$ .

### 14.2 Model results with snubber

With the implementation of the snubbers, the results are similar to the measured data. However, it is to be noted that during the experimental tests it was only possible to measure the averaged current with  $16.67 \mu\text{s}$  steps. But the averaged current can not show the rapid oscillations of the instantaneous one. In-fact, while the averaged simulated current shows a similar behavior of the measured one, the instantaneous simulated current shows greater oscillation at zero-crossing. This can be clearly seen comparing Fig. 14.3 with Fig. 14.4.

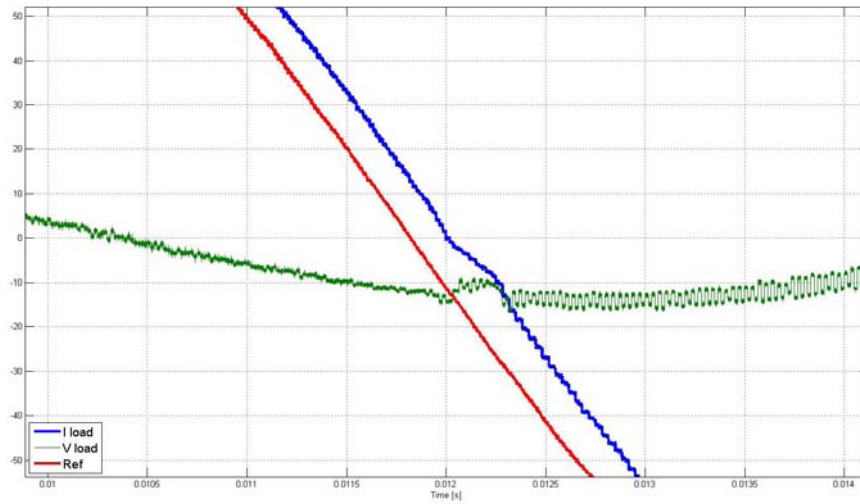


Figure 14.2: A zoom-in of the previous graph.

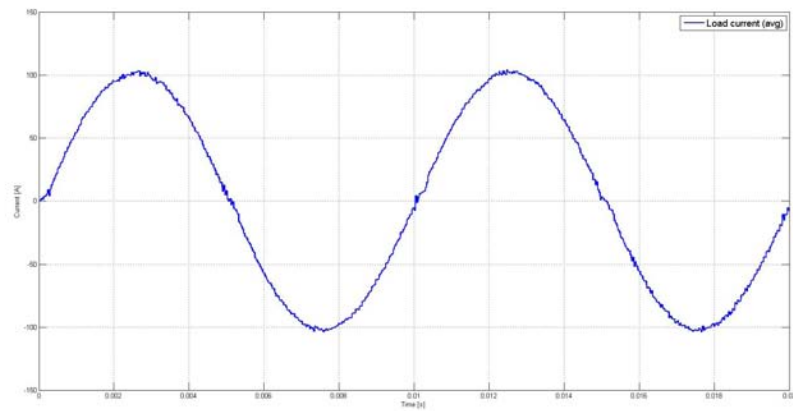


Figure 14.3: The simulated averaged load current in CCM, with sinusoidal 100 A (peak) current reference,  $V_{DC} = 300$  V,  $K_i = 0.3$ ,  $K_p = 1.35$ .

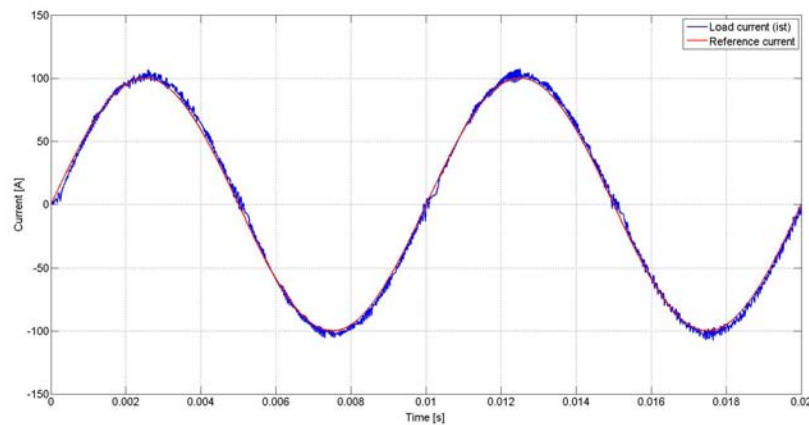


Figure 14.4: The simulated instantaneous load current compared with the reference current in CCM, with sinusoidal 100 A (peak) current reference,  $V_{DC} = 300$  V,  $K_i = 0.3$ ,  $K_p = 1.35$ .

### 14.3 Causes

The current distortion happens only at very low current and low voltages. In this condition three main causes are involved:

1. very low current on filter inductances: these inductances feed the current needed by the snubber to charge or discharge themselves. If this current are low, also the snubber dynamics are greatly slowed down;
2. low voltage reference: this leads to a certain overlap between the DT of the two converter legs, so there are some time intervals in which there is totally no control on the voltage applied to the H-bridge terminals, which become imposed firstly by the snubbers dynamics;
3. inductance current zero-crossings: because the current change sign during snubbers charge/discharge time intervals, this may lead to an oscillation of their voltage and a further slow down of their dynamics.

All this three causes end up with:

1. applying an H-bridge differential voltage that has the opposite sign of the desired one, due to the DT compensation system;
2. making the voltage pulses not reaching the full DC-link voltage, mainly due to the slowed down dynamics;

This two effects can be clearly seen in Fig. 14.5.

### 14.4 Dynamics of the phenomena

Firstly it is hypothesized that the reference voltage needed during current zero-crossing is positive, so that the H-bridge should apply to the filter only positive voltage pulses (+300 V) during the PWM cycle. What results from Simulink® simulations, made with the convolution-based model and a 250 ns time step, is that, effectively, during the current zero-crossing, some negative voltage pulses are detected, as it is clearly shown in Fig. 14.6.

So, in this time interval the subsequent phenomena happen:

1. initially there is positive current on the filter inductances;

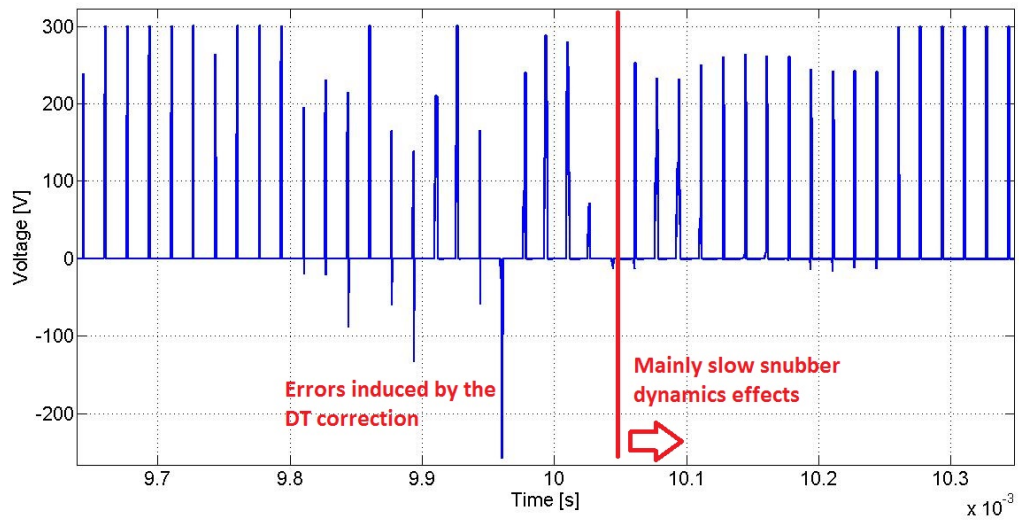


Figure 14.5: An overview of the voltage errors that occur during current zero-crossing.

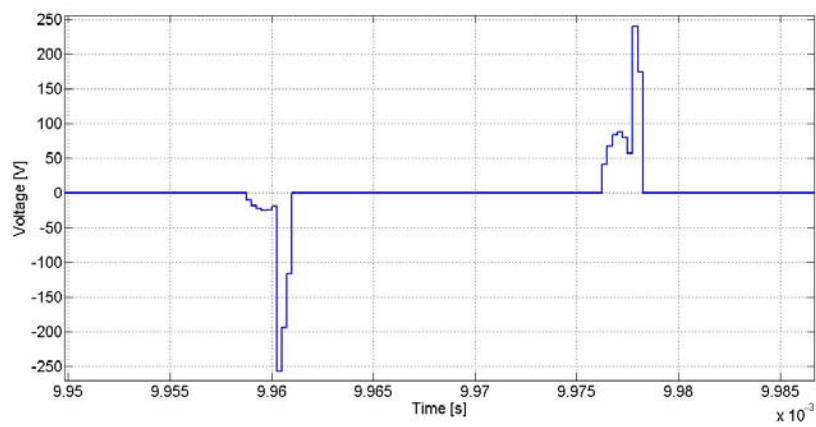


Figure 14.6: The instantaneous H-bridge voltage, note the anomalous negative pulse at 9.96 ms.

2. the U-branch lower switch is initially in the on state, but, due to the positive current, the lower free-wheeling diode conduct and the DT effects do not appear in this branch;
3. the V-branch lower switch is in the on-state and it is carrying the inductance current;
4. then, the V-branch lower IGBT is turned off and the DT starts: the lower snubber starts to charge itself, while the upper one starts to discharge, both absorbing the inductance current, which decreases;
5. after some time the inductance current reaches zero, while the snubbers have not ended their transient, so that the V-branch voltage stops to grow and, instead, starts to decrease slowly;
6. at this time the U-branch lower diode is forced to turn-off, which triggers the snubbers transient;
7. shortly after, the V-branch DT ends and the upper IGBT is switched on: immediately (i.e. with fast dynamics) the V-branch potential is clamped to the positive DC-link one (+300 V);
8. however the U-branch is still undergoing the snubbers transient and its terminal potential is still low, so the voltage applied to the filter become negative and near to the DC-link voltage (a little more than -300 V).

This sequence can be clearly seen in Fig. 14.7 and 14.8, where the described events happen at around 9.96 ms.

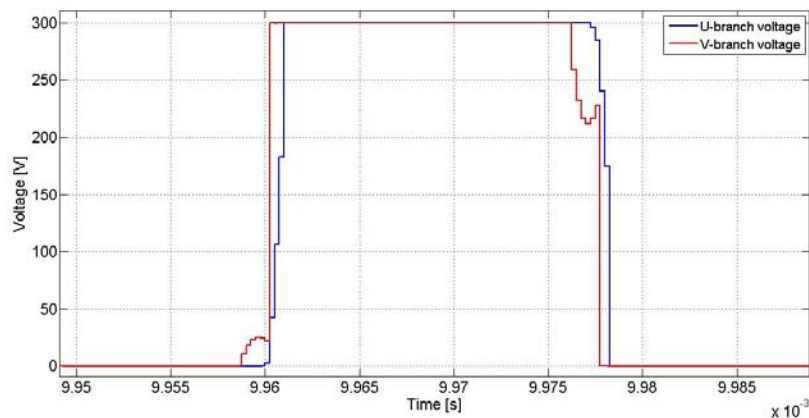


Figure 14.7: The instantaneous terminals potential referred to ground.

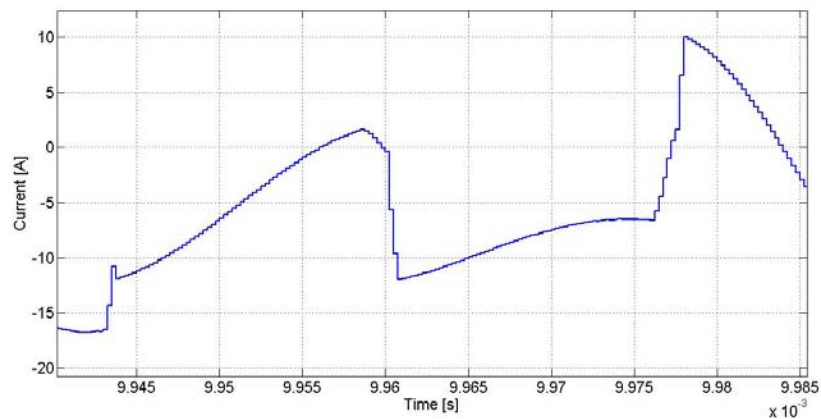


Figure 14.8: The instantaneous filter inductance current.

However, it has to be noted that the used IGBT model does not take in account of the rise/fall times of the switch, which, also, are dependent on the IGBT current. Furthermore, the current near zero-crossing is imposed by the snubber discharge on the IGBT itself, which gives rise to current greater than 50 A.

## 14.5 Possible solution

Some possible solutions can be found, keeping in mind that:

1. the problem does not heavily disturb the load current, which is only affected by a little deviation from the reference;
2. the current DT algorithm should not be highly modified, due to its correct and good behavior in other situations;

Software solutions should take in account the interaction between the two branches of the converter that happen during the DT. So, a way to take into account the effective voltage applied to the load should be found. In particular, in the example given above, the phenomena can be corrected avoiding the initial commutation of the V-branch, i.e. delaying its commutation after the end of the DT to the U-branch. This could be done by adding, downstream the DT correction algorithm, a supervisor controller that can recognize, by analyzing the DT correction output PWM signals and the sign of the current, if the resulting H-bridge voltage is the desired one.

## 14.6 The supervisor controller

The aim of this paragraph is only to show the way to develop such a system and to underline the possible instabilities that can rise with its implementation. The final system that the Author developed can be seen in Fig.14.9, where the most important sections are well underlined.

So, there are three main parts:

1. the DT simulation section;
2. the error recognition section;
3. the switching section;

**The DT simulation section.** This part of the algorithm simply predicts the delay effects imposed by the DT. In-fact, it needs to know the sign of the current on the inverter outputs. However, in order to simplify the system, only the reference current is considered, which anyway gave good results.

So, now the system is able to understand when the DT effect can afflict the converter branch. In-fact, by using a set of logical switches, the turn-on or turn-off delay can be bypassed, if necessary.

**The error recognition section.** This segment, then, recognizes, by using a simple logical circuit, if the voltage pulse will have the correct sign. If not, the algorithm will exchange the signal between the two legs.

In-fact, there are three logical ports:

1. XOR (one): this port recognizes if the two signals are different, however it does not tell which of the two is in the ON (1, +300 V branch voltage) or OFF (0, 0 V branch voltage) state;
2. AND: this is needed to recognize which of the two legs is actually in the OFF state, in-fact one of the two inputs comes from a comparator that is 1 when the U-branch is OFF. So, as output, we get 1 only when the U-branch is in the OFF state and the V-branch is in the ON state, resulting in a -300 V at the converter terminals;
3. XOR (two): then the obtained signal has to be compared with the needed sign of the H-bridge voltage pulse. So, this port gives 1 as output when the needed sign and the predicted one are the same, if not the XOR port gives 0 as result and a switch of the two signals is then requested.

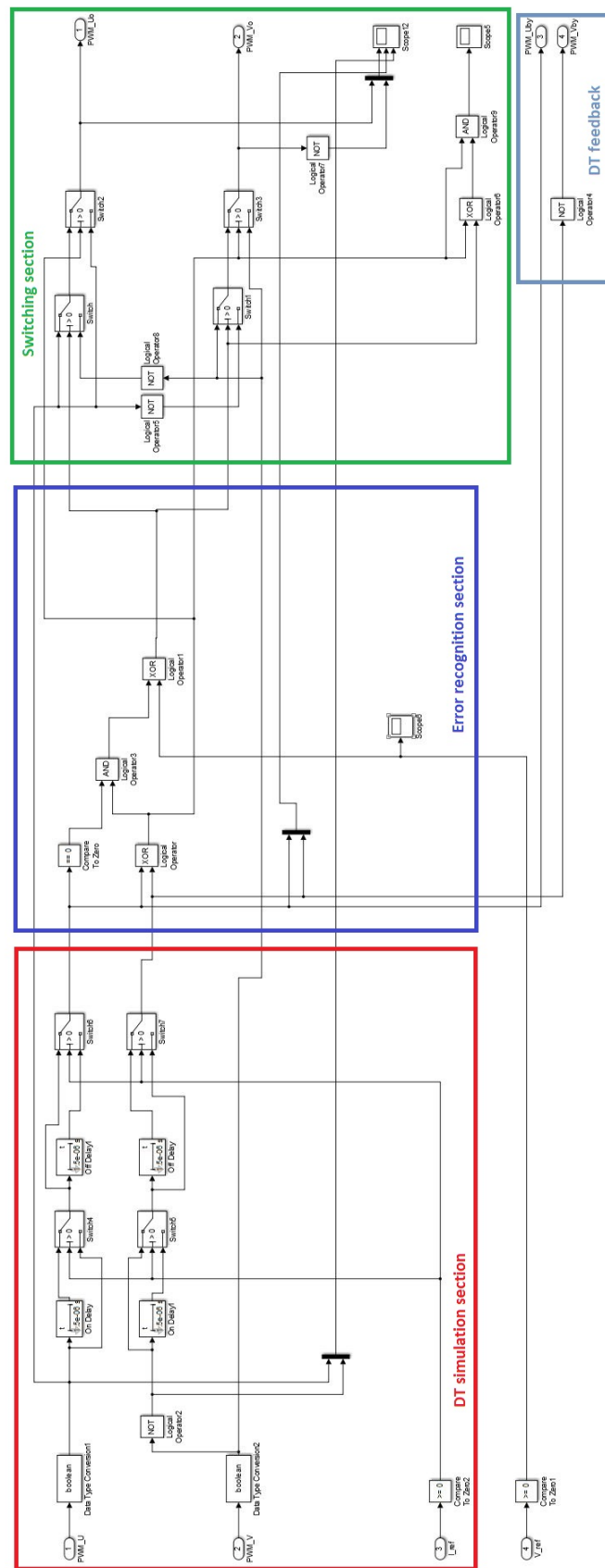


Figure 14.9: The resulting supervisory system.

**The switching section.** So, in this part, if requested, the two signal of the branches can be exchanged. A NOT port applied to the two switching signal is needed just because the PWM signal of the U-branch commands the upper switch, while the other commands the lower one. Then, a further logical switch system is needed. In-fact, the two PWM signals must bypass the whole system if the needed voltage is 0 V: i.e. when the XOR1 output is 0.

So, the obtained system its just a logical network that can be implemented efficiently in the FPGA. However, this supervisory controller highly destabilize the DT correction system. So, it must be invisible to the DT correction system. This can be actually achieved simply by feeding back the correction system with the simulated delay obtained as output from the first section.

The obtained results are, so, pictured in Fig. 14.10. While not being optimal, they underline how this system can be the right path to follow in order to achieve the total correction of these undesired effects.

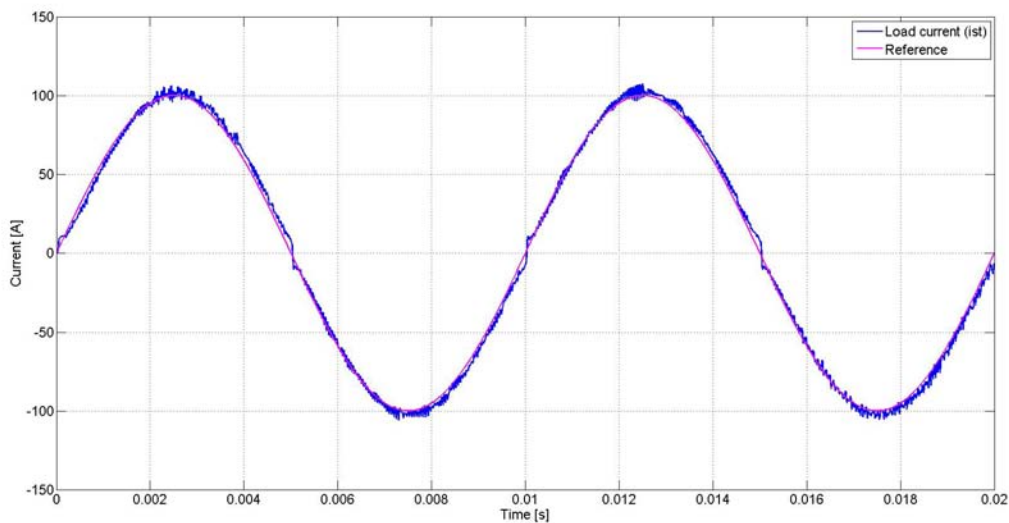


Figure 14.10: The results of the supervisory system with 100 A amplitude in CCM, with sinusoidal 100 A (peak) current reference,  $V_{DC} = 300$  V,  $K_i = 0.3$ ,  $K_p = 1.35$ .

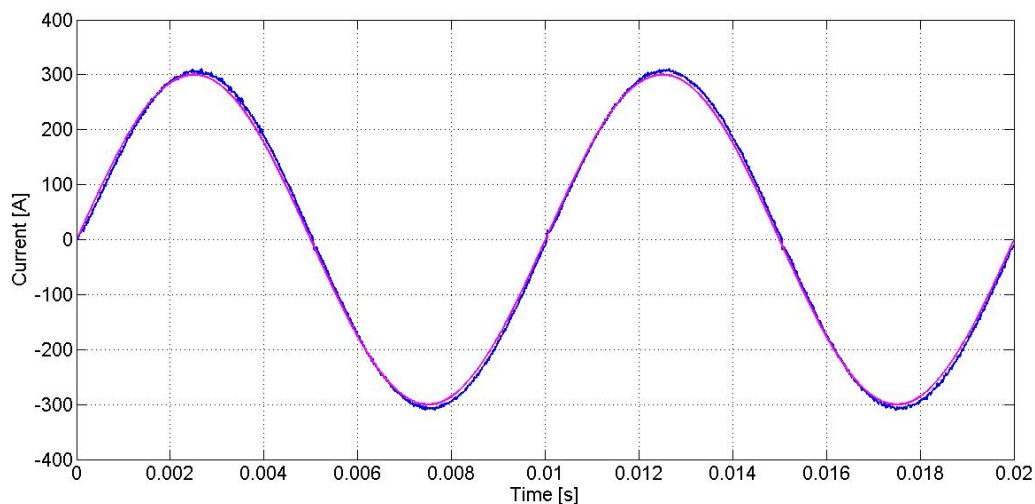


Figure 14.11: The results of the supervisory system with 300 A amplitude in CCM, with sinusoidal 100 A (peak) current reference,  $V_{DC} = 300$  V,  $K_i = 0.3$ ,  $K_p = 1.35$ .



# Chapter 15

## Anomalous voltage oscillations

### 15.1 Introduction

During experiment runs, some unwanted voltage oscillations have been observed, especially at high positive currents (300 A) and low voltages, as shown in Fig. 15.1.

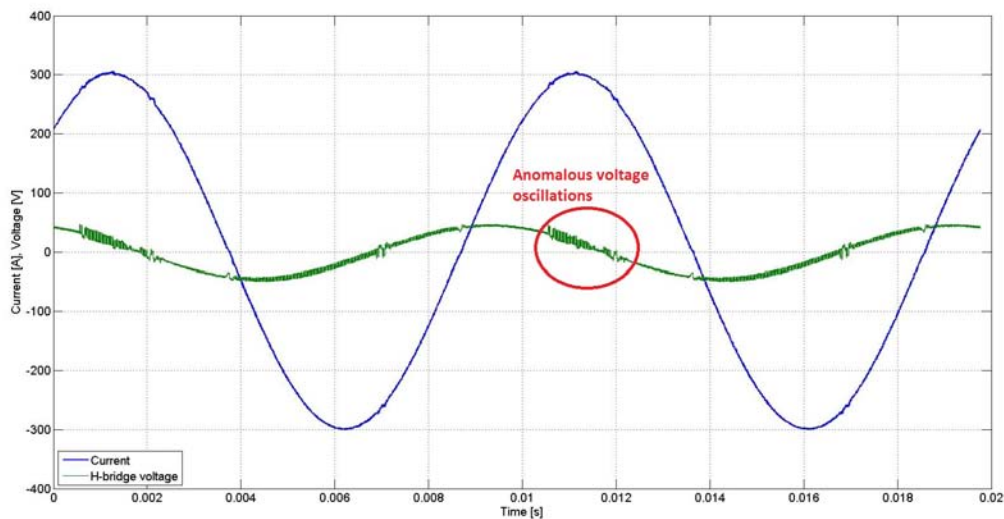


Figure 15.1: Average load current and H-bridge voltage in CCM, with 300 Apk, 100 Hz reference,  $K_i=0.3$ ,  $K_p=1.35$ ,  $V_{DC} = 300$  V.

Further measurements showed that:

1. the DSP PWM signals are OK;
2. there is a sort of random shift of the time interval in which the converter apply the full DC voltage, which causes oscillations of the H-bridge average voltage and the load voltage.

Other analysis with the help of some Matlab® code, showed that the random shift was of about 600 ns, while the averaged voltage oscillations had an amplitude of about 7 to 10 V.

### 15.2 Initial measurements

In order to better characterize the problem, firstly feedback logicals signal coming from the switches have been measured: each of this two signals is TRUE when the low switch is ON, i.e. with a null drain-source

voltage  $V_{DS}$ , and is FALSE when the low switch is off, i.e. with  $V_{DS} = V_{DClink}$  V. What came out was a strange behavior of the feedback of the U branch, which is the positive terminal of the converter, as can be seen in Fig. 15.2 and 15.3.

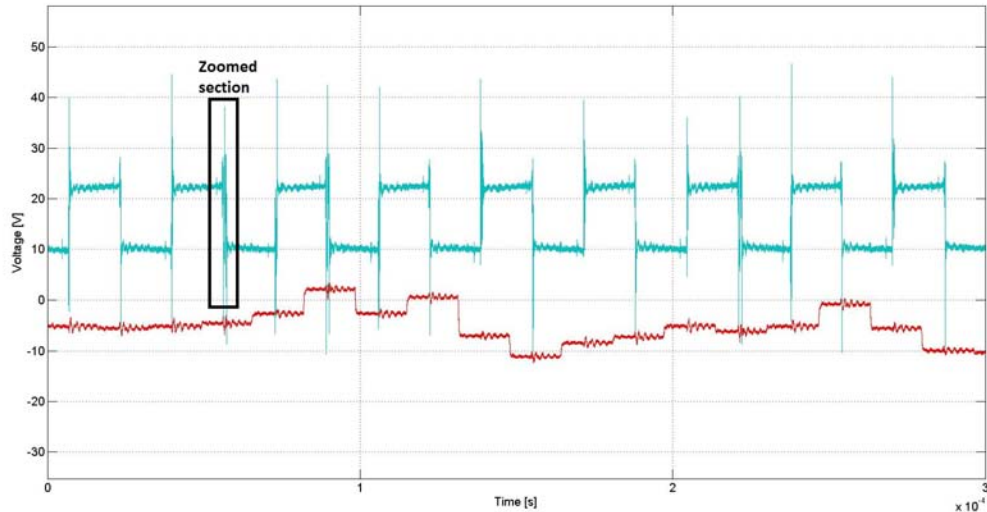


Figure 15.2: The feedback signal of the U-branch (blue) and the H-bridge averaged voltage (red), during an anomalous voltage oscillation.

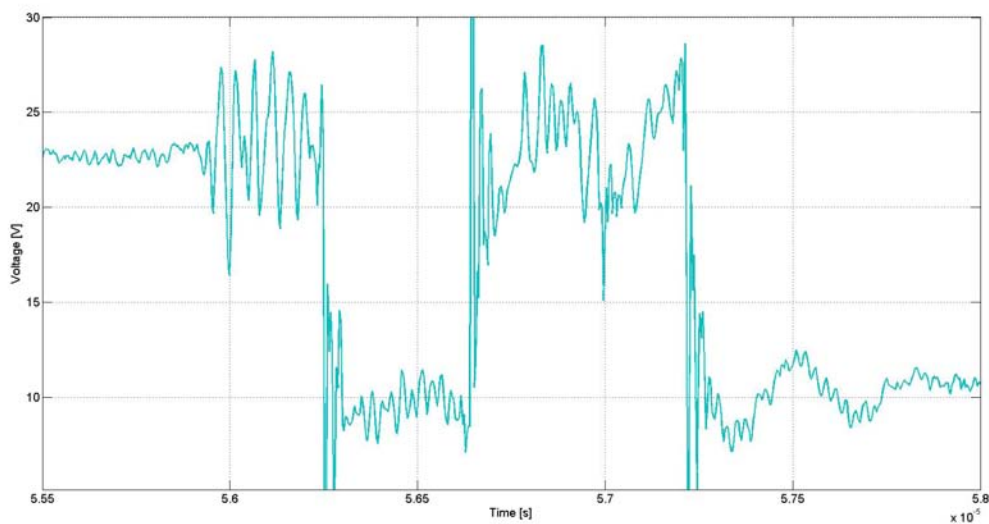


Figure 15.3: A zoom-in of the previous graph, where the anomalous feedback behavior can be better observed.

Here, in-fact, it can be seen how sometimes the feedback signal, after a turn off, suddenly return for a certain period in the TRUE-state. So, this phenomena is actually what triggers the observed voltage oscillations.

Measuring also directly the  $V_{DS}$  of the two U-branch switches, four phases can be highlighted (keeping in mind that the phenomena is observed with positive high load current):

1. zero U-branch voltage: the low switch is on and the anti-parallel diode conduct;

2. the low switch is turned off: the system behave correctly, the lower diode continues to conduct and the branch enters the DT interval;
3. the upper switch is turned on at DT end: the system behave as expected, the lower diode turn off and the current is now led by the upper IGBT; also the U-branch voltage rise toward the DC-link one (300 V);
4. after about 300 to 400 ns the U-branch voltage starts to fall down, while the two  $V_{DS}$  of the switches change going towards an intermediate values of about 100 V: this phenomena lasts about 100 to 200 ns and then the system returns to a normal state.

These dynamics are well pictured in Fig. 15.4.

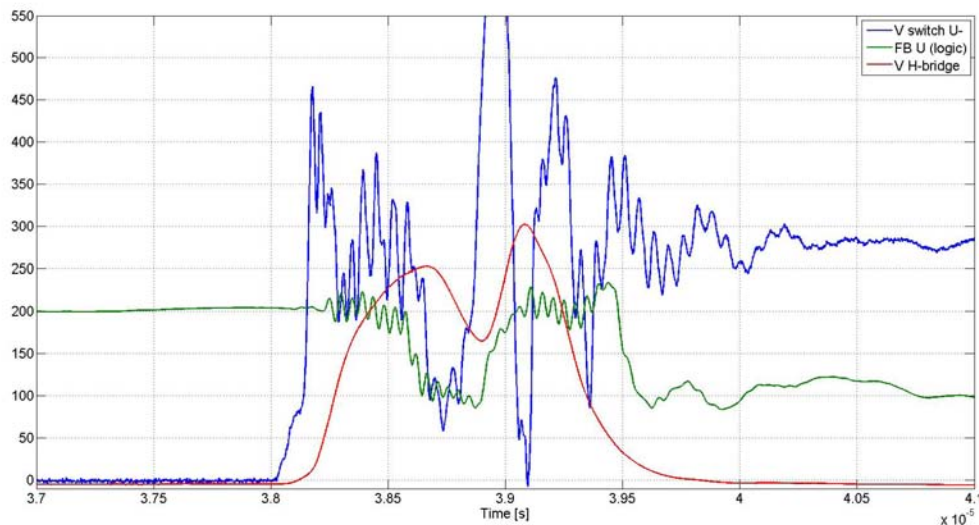


Figure 15.4: U-branch voltage, feed-back signal and H-bridge voltage during the U-branch commutation.

### 15.3 Shoot-through phenomena

Then, also the U-branch gate voltages  $V_{GS}$  have been monitored. By doing so, it resulted that the upper switch behaves correctly, while the lower one not.

In-fact, as shown in Fig. 15.5, about 350 ns after the correct turn on of the upper switch, the lower switch is turned on by a gate pulse, whose cause is still unknown. This unexpected turn-on of the switch causes a dangerous shoot-through condition, that could seriously damage the IGBT itself. In-fact, after all these test, in such anomalous condition, a fatal fault of the switch occurred. Also, the shoot-through phenomenon has not been observed on the V-branch.

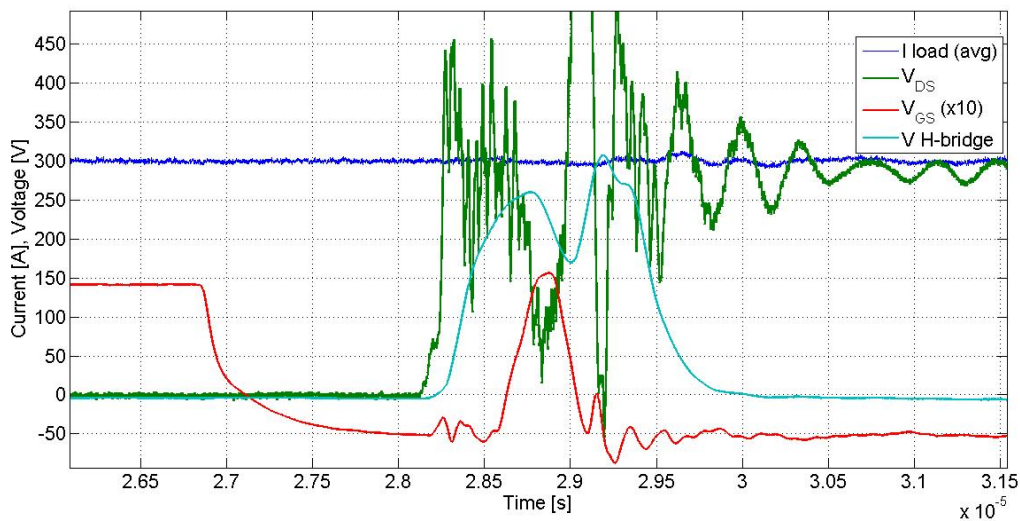


Figure 15.5: Load current, drain-source and gate-source voltages of the lower switch and H-bridge voltage during a shoot-through phenomenon on the U-branch: note how it happens well after the DT interval and the turn-on of the upper switch.

## 15.4 Parasitic turn-on phenomena

Parasite turn-on phenomena are well known problems that may happen due to the high voltage and current derivatives that can occur during commutations. In the studied case, two are the possible causes that can trigger this parasitic turn on:

1. voltage spikes induced by the Miller capacitance;
2. voltage spikes created by stray inductances.

**Miller capacitance effects.** The "Miller capacitance" is an equivalent parasitic element that connects the drain and gate terminals and it is created by the module geometry itself, as can be seen in Fig. 15.6. While its value is usually under 1 nF, if an high  $dV/dt$  is applied to it, a non negligible current will start to pass through it. This current, then, will close its path through the gate resistor, creating voltage drops that could greatly step-up the gate potential itself, possibly making the  $V_{GS}$  crossing the IGBT threshold voltage and leading to an unwanted turn-on of the switch. This phenomenon can be triggered on the lower switch of the branch when it is off, with its anti-parallel diode conducting, and, then, the upper switch is subsequently turned on.

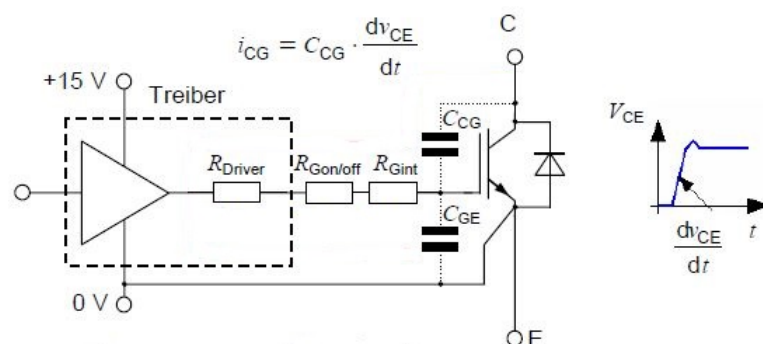


Figure 15.6: The electrical scheme that shows the Miller capacitance [15].

**Stray inductances effects.** Stray inductances are equivalent components that sum up the behavior of all the connections that are around the switch itself. In particular, they are placed downstream the source terminal, as shown in FIG. 15.7, and they have a typical values of about 15 to 20 nH. Voltage drops across them can be noted when high  $di/dt$  are applied. This can happen, in particular, during the decay of the reverse recovery current of the anti-parallel diode. In-fact, during this time interval a rapidly decaying current flow trough the stray inductance of the switch, leading to a decrease of the source terminal potential. This phenomena can be noisy on the low switch when it is off, with the diode conducting, and the upper switch is then turned on. In-fact, at this time, the diode stops conducting and, during the commutation phase, the rapidly decaying reverse recovery current starts to flow through the stray inductance, lowering the source potential and leading to an increase of the  $V_{GS}$ , that can trigger a parasite turn-on of the IGBT itself.

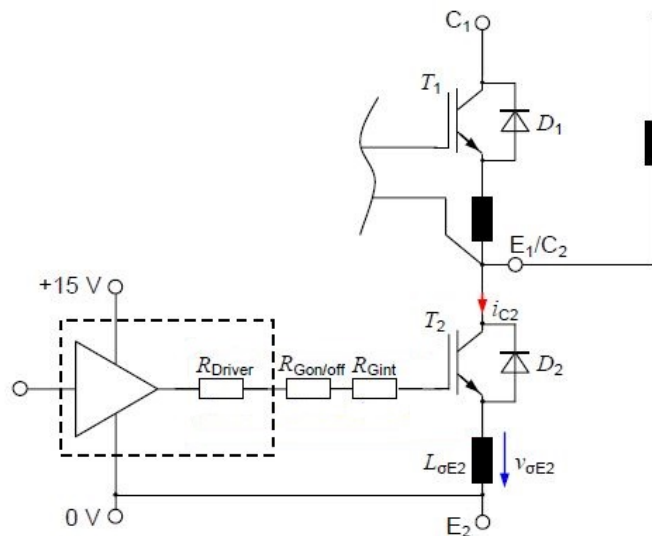


Figure 15.7: The electrical scheme that shows where the stray inductance  $L_{\sigma E2}$  is placed [15].

However, these phenomena can be compensated in various modes and measurements done on the  $V_{GS}$  show that they may not to be the cause of the gate restrike. In-fact, damped oscillations of the  $V_{GS}$  can be observed at every commutation of the bridge, as shown in Fig. 15.8, but they do not reach the gate thresholds. Furthermore, these phenomena should happen on the lower switch contemporary with the commutation of the upper switch, which is not the case. So, parasitic turn-on should not be the cause of the previously described shoot-through phenomena.

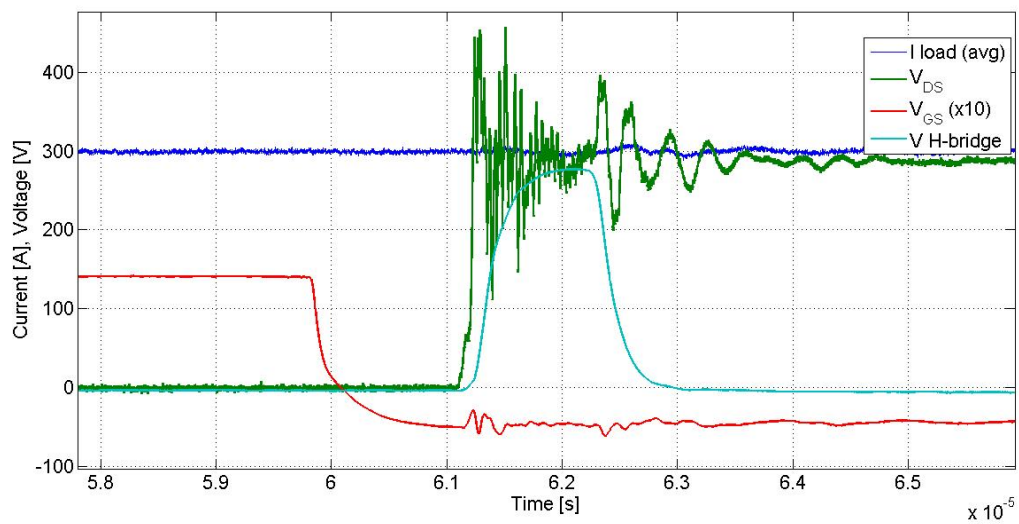


Figure 15.8: Load current, drain-source and gate-source voltages of the lower switch and H-bridge voltage during a correct U-branch commutation: note the oscillations that happen on the  $V_{GS}$  just after the  $V_{DS}$  rise.

# Chapter 16

## Conclusions

### 16.1 Main results

In conclusion, a detailed characterization of the converter prototype and its load has been achieved. This has led to the development of a set of various Simulink models in which, in particular, the control section is very accurate. Thanks to these models, an optimization process of the control parameters has been initiated by the Author with a Multi-objective optimization code. In addition, promising alternatives to the simple PI controller have been found. As it has been shown by simulations, these solutions have beneficial effects on the dynamic response of the system.

Also, the voltage overshoots phenomenon due to the output filter has been well characterized and, then, the Author found a possible solution to this, with a upgraded filter scheme. The Author quantified also the power dissipated by the damping resistance, which is not so different in comparison with the original filter.

Further, the Author identified some possible improvements of the Dead Times compensation algorithm, that can be implemented in the converter firmware. Such upgrade would reduce the current distortion observed at zero-crossing both on simulations and experimental results.

Finally, the author studied the anomalous voltage oscillations occurring in the prototype at certain condition, and discovered its cause, i.e. occasional shoot-through events, much dangerous for the power switches.

### 16.2 Future developments

Firstly, a further characterization of the IGBTs dynamics during commutation would be useful, as future work, in order to improve even more the precision of the model and the control section.

Also, the analyzed improvements of the output filter to limit voltage derivatives and peaks, found by the Author, should be tested on the prototype.

In addition, the newly found controller would need further studies and a solid validation with experimental data, requiring the update of the firmware with the support of the Supplier. Moreover, it would be interesting to develop further and study the deconvolution-based controller presented in this work, which, also, will certainly require an optimization and parallelization of the code that makes the convolution, which could be implemented in some FPGA chipset.

Further upgrades, which also consider the waveform of the drain-source voltage across the power switches during commutations, would increase the voltage accuracy at low current levels and it would be worthwhile to dedicated analyses and experimental tests.





# Appendix A

## Matlab® codes

### A.1 Code to find the impulsive response

```
1 clear all;
2
3 %use RWM-CC data
4 load('fRX 8 turns no Cstray_da specifica_matlab_estrap100kHz.mat');
5 %use DL data
6 %load('fRX DL JAEA_matlab.mat');
7
8
9 fint=1:1:100000; % The frequency response is sampled with 1 Hz step
   from 1 Hz to 100 kHz
10 %for RWM-CC only
11 Rinterpol = interp1(data(:,1),data(:,2),fint,'cubic','extrap');
12 Xinterpol = interp1(data(:,1),data(:,3),fint,'spline','extrap');
13 %for DL only
14 % Rinterpol = interp1(dataDL(:,1),dataDL(:,2),fint,'cubic','extrap');
15 % Xinterpol = interp1(dataDL(:,1),dataDL(:,3),fint,'spline','extrap');
16
17 figure(1);
18 plot(log10(fint), Rinterpol);
19 ylabel('Resistance [Ohm]');
20 xlabel('log10(Frequency)');
21 grid on;
22 figure(2);
23 plot(log10(fint), Xinterpol./(fint*2*pi));
24 ylabel('Inductance [H]');
25 xlabel('log10(Frequency)');
26 grid on;
27
28 %computation of the admittance
29 Zinterpol = complex(Rinterpol,Xinterpol);
30 Yinterpol=zeros(1,100000);
31
32 for i=1:100000
33
34     Yinterpol(i)=Rinterpol(i)/(abs(Zinterpol(i))^2)-1i*Xinterpol(i)
   /(abs(Zinterpol(i))^2);
35
36 end;
```

```

37
38 Ysimm=zeros(1,200000);
39
40 for i=1:100000
41     Ysimm(i)=Yinterpol(i);
42
43
44 end;
45
46
47 for i=100001:200000
48     Ysimm(i)=conj(Ysimm(mod(200000-i+1,200000)+1));
49
50
51 end;
52
53 %computation of the impulsive response
54 Responsesduplice = real(ifft(Ysimm,200000,'symmetric')); %The ifft is
    real because Ysimm is symmetric conjugate
55 Responsecut=Responsesduplice(1:100000); %Only 1 half of the time
    response is taken, corresponding to 1/2 = 0.5 s
56 t = linspace(0,0.5,100000); %The time response length is 0.5 s and
    spaced with 5 us steps (0.5s/100000)
57
58 Responsetot(1,:)=t(1,:); %Time base
59 Responsetot(2,:)=Responsecut(1,:); %Time response
60
61 N=15000 %Only a part of the time response is taken, N is the number
    of samples, corresponding to N*5us duration
62
63 Response5usDL(:,:)=Responsetot(:,(1:N));
64
65 %running mean (optional)
66 n_media=4;
67 media_I(1,N)=0;
68 for i=5:N
69     media_I(1,i)=(Response5usDL(2,i)+Response5usDL(2,i-1)+Response5usDL(2,i
        -2)+Response5usDL(2,i-3))/4;
70 end;
71 media_I(1,1:2)=Response5usDL(2,1:2);
72 media_I(1,3)=(Response5usDL(2,2)+Response5usDL(2,3))/2;
73 media_I(1,4)=(Response5usDL(2,2)+Response5usDL(2,3)+Response5usDL(2,4))
    /3;
74 media_I(1,1)=0;
75 media_I(1,2)=(Response5usDL(2,1)+Response5usDL(2,2))/2;
76
77 figure(3);
78 plot(Response5usDL(1,:), Response5usDL(2,:), Response5usDL(1,:),media_I)
    ;
79 ylabel('Current [A]');
80 xlabel('Time [s]');
81
82 %time step reduction to 1 us
83 Response5us(:,:)=Responsetot(:,(1:N));
84 Response5us(2,:)=media_I(:);
85 Response1us(1,:)=linspace(0,0.03,120000); %Time base

```

```

86 Response1us(2,:) = interp1(Response5us(1,:),Response5us(2,:),Response1us
    (1,:),'spline','extrap')/20;
87
88 figure(5);
89 plot(Response1us(1,:), Response1us(2,:));
90 ylabel('Impulsive response [A]');
91 xlabel('Time [s]');
92 grid on;
93 axis([0 0.015 0 0.04]);

```

## A.2 PSO-MO Matlab® code

```

1 clear all;
2
3 %load the needed impulsive response
4 time_response_RWMC;
5
6 %particle swarm optimization
7
8 %initial parameters
9 Tstep=250e-9; %simulation time step
10 D=2;
11 Nobj=5; %objectives number
12 N=10; %particle number
13 itmax=10; %iteration number
14 c1=1.05;
15 c2=1.05;
16 wmin=0.3;
17 wmax=1;
18 w=linspace(wmin,wmax,itmax); %decreasing mass parameter
19
20 %domain borders
21 lim_min(1:N,1)=0; %lim Ki
22 lim_min(1:N,2)=0; %lim Kp
23 lim_max(1:N,1)=50; %lim Ki
24 lim_max(1:N,2)=10; %lim Kp
25 b=lim_max;
26 a=lim_min;
27
28 %nitial velocities
29 q=(b-a)/4;
30 v=q.*rand(N,D);
31
32 %ititial positions
33 x=a+(b-a).*rand(N,D);
34 %some previously obtained results:
35 %needed for validation
36 x(1,:)=[4, 1.13];
37 x(2,:)=[0.3, 1.35];
38 x(3,:)=[2.3462, 1.5721];
39 x(4,:)=[1.5362, 1.791];
40 x(5,:)=[1.1877, 1.7204];
41
42 tic

```

```

43 %initial evaluation
44 for i=1:N
45     Ki=x(i,1);
46     Kp=x(i,2);
47     f=100;
48     T=20e-3;
49     Nval=T/(2*Tstep);
50     sim('inverter_conv');
51     Imax=max(Iload.signals.values);
52     Adb100(i,1)=abs(20*log10(300/abs(Imax)));
53     fun(i,1)=Adb100(i,1);
54     funs(i,1)=sign(20*log10(300/Imax));
55     f=500;
56     T=5e-3;
57     Nval=8000;
58     sim('inverter_conv');
59     Imax=max(Iload.signals.values);
60     Adb500(i,1)=abs(20*log10(300/abs(Imax)));
61     fun(i,2)=Adb500(i,1);
62     funs(i,2)=sign(20*log10(300/Imax));
63     f=1000;
64     T=1.5e-3;
65     Nval=1750;
66     sim('inverter_conv');
67     n=length(THD.signals.values);
68     Imax=max(Iload.signals.values);
69     Adb1(i,1)=abs(20*log10(300/abs(Imax)));
70     fun(i,3)=Adb1(i,1);
71     funs(i,3)=sign(20*log10(300/Imax));
72     f=3000;
73     sim('inverter_conv');
74     n=length(THD.signals.values);
75     Imax3=max(Iload.signals.values);
76     THD_I3(i,1)=THD.signals.values(n);
77     Adb3(i,1)=abs(20*log10(300/Imax3));
78     fun(i,4)=Adb3(i,1);
79     fun(i,5)=THD_I3(i,1);
80     funs(i,4)=sign(20*log10(300/Imax3));
81 end;
82 toc
83
84 %pareto front extraction
85 pbest=x;
86 fpbest=fun;
87 idxp=findpareto(fun);
88 archives=funs(idxp,:); %sign archive
89 archivef=fun(idxp,:); %eval archive
90 archivex=x(idxp,:); %position archive
91 %if Adb1khz<0 the point is not interesting and
92 %must be erased from the archive
93 neg=find(archives(:,3)<0);
94 if length(neg)~=size(archives,1)
95     archivef(neg,:)=[];
96     archivex(neg,:)=[];
97     archives(neg,:)=[];
98 end;

```

```

99
100 %global best points choice
101 %THD criterion
102 THDmin=min(archivef(:,5));
103 if THDmin>=0.012 %this values can be higher
104     igbest=find(archivef(:,5)==THDmin);
105     fgbest=archivef(igbest,:);
106     gbest=archivex(igbest,:);
107 else
108     %3 kHz behavior analysis
109     a=find(archivef(:,5)<=0.012);
110     Adb3min=min(archivef(a,4));
111     if Adb3min>=3
112         igbest=find(archivef(:,4)==Adb3min);
113         fgbest=archivef(igbest,:);
114         gbest=archivex(igbest,:);
115     elseif Adb3min<3 && Adb3min>=2.5
116         %1 kHz behavior analysis
117         c=find(archivef(a,4)<=3 & archivef(a,4)>=2.5);
118         b=a(c);
119         %select only positive attenuations
120         bc=find(archives(b,3)>0);
121         if isempty(bc)
122             Adb1min=min(archivef(b,3));
123         else
124             Adb1min=min(archivef(bc,3));
125         end;
126         igbest=find(archivef(:,3)==Adb1min);
127         fgbest=archivef(igbest,:);
128         gbest=archivex(igbest,:);
129     else
130         %Adb min at 3 kHz <2.5 dB
131         c=find(archivef(a,4)<=2.5);
132         d=max(archivef(c,4));
133         igbest=find(archivef(:,4)==d);
134         fgbest=archivef(igbest,:);
135         gbest=archivex(igbest,:);
136     end;
137 end;
138 gbest=gbest(1,:);
139
140 %personal best choice
141
142 for i=1:N
143     if(find(idxp==i))
144         if(domination(fun(i,:),fpbest(i,:))==1)
145             fpbest(i,:)=fun(i,:);
146             pbest(i,:)=x(i,:);
147         end;
148     end;
149 end;
150
151
152 %main iteration cycle
153 tic
154 for it=1:itmax

```

```

155     v(1:N,1:D)=w(it)*v(1:N,1:D)+c1*rand*(pbest(1:N,1:D)-x(1:N,1:D))+c2*
        rand*( repmat(gbest,N,1)-x(1:N,1:D));
156     x(1:N,1:D)=x(1:N,1:D)+v(1:N,1:D);
157     %new evaluation
158     for i=1:N
159         Ki=x(i,1);
160         Kp=x(i,2);
161         f=100;
162         T=20e-3;
163         Nval=T/(2*Tstep);
164         sim('inverter_conv');
165         Imax=max(Iload.signals.values);
166         Adb100(i,1)=abs(20*log10(300/abs(Imax)));
167         fun(i,1)=Adb100(i,1);
168         funs(i,1)=sign(20*log10(300/Imax));
169         f=500;
170         T=5e-3;
171         Nval=8000;
172         sim('inverter_conv');
173         Imax=max(Iload.signals.values);
174         Adb500(i,1)=abs(20*log10(300/abs(Imax)));
175         fun(i,2)=Adb500(i,1);
176         funs(i,2)=sign(20*log10(300/Imax));
177         f=1000;
178         T=1.5e-3;
179         Nval=1750;
180         sim('inverter_conv');
181         n=length(THD.signals.values);
182         Imax=max(Iload.signals.values);
183         Adb1(i,1)=abs(20*log10(300/abs(Imax)));
184         fun(i,3)=Adb1(i,1);
185         funs(i,3)=sign(20*log10(300/Imax));
186         f=3000;
187         sim('inverter_conv');
188         n=length(THD.signals.values);
189         Imax3=max(Iload.signals.values);
190         THD_I3(i,1)=THD.signals.values(n);
191         Adb3(i,1)=abs(20*log10(300/Imax3));
192         fun(i,4)=Adb3(i,1);
193         fun(i,5)=THD_I3(i,1);
194         funs(i,4)=sign(20*log10(300/Imax3));
195     end;
196     it
197     idxp=findpareto(fun);
198     [archivex, archivef, idx]=putarchive(archivex,archivef,x,fun);
199     archives=[funs; archives];
200     archives=archives(idx,:);
201     %if Adb1khz<0 the point is not interesting and
202     %must be erased from the archive
203     neg=find(archives(:,3)<0);
204     if length(neg)~=size(archives,1)
205         archivef(neg,:)=[];
206         archivex(neg,:)=[];
207         archives(neg,:)=[];
208     end;
209

```

```

210 %global best points choice
211 %THD criterion
212 THDmin=min(archivef(:,5));
213 if THDmin>=0.012 %this values can be higher
214     igbest=find(archivef(:,5)==THDmin);
215     fgbest=archivef(igbest,:);
216     gbest=archivex(igbest,:);
217 else
218     %3 kHz behavior analysis
219     a=find(archivef(:,5)<=0.012);
220     Adb3min=min(archivef(a,4));
221     if Adb3min>=3
222         igbest=find(archivef(:,4)==Adb3min);
223         fgbest=archivef(igbest,:);
224         gbest=archivex(igbest,:);
225     elseif Adb3min<3 && Adb3min>=2.5
226         %1 kHz behavior analysis
227         c=find(archivef(a,4)<=3 & archivef(a,4)>=2.5);
228         b=a(c);
229         %select only positive attenuations
230         bc=find(archives(b,3)>0);
231         if isempty(bc)
232             Adb1min=min(archivef(b,3));
233         else
234             Adb1min=min(archivef(bc,3));
235         end;
236         igbest=find(archivef(:,3)==Adb1min);
237         fgbest=archivef(igbest,:);
238         gbest=archivex(igbest,:);
239     else
240         %Adb min at 3 kHz <2.5 dB
241         c=find(archivef(a,4)<=2.5);
242         d=max(archivef(c,4));
243         igbest=find(archivef(:,4)==d);
244         fgbest=archivef(igbest,:);
245         gbest=archivex(igbest,:);
246     end;
247 end;
248 gbest=gbest(1,:);
249
250 %personal best choice
251
252 for i=1:N
253     if(find(idxp==i))
254         if(domination(fun(i,:),fpbest(i,:))==1)
255             fpbest(i,:)=fun(i,:);
256             pbest(i,:)=x(i,:);
257         end;
258     end;
259 end;
260 end;
261 toc
262
263 %show the last pareto front
264 gbest
265 fgbest

```





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