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ANALYSIS AND DESIGN OF A HIGH FREQUENCY DRIVER FOR CASCODE POWER STAGES SUITABLE FOR AUTOMOTIVE DCDC CONVERSION

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Chapter 1

Introduction

1.1 Infineon® Technologies

This thesis has been developed in collaboration with *Infineon® Technologies* which is a world leader in semiconductor solutions founded in 1999. Its mission is to make like easier, safer and greener with semiconductors that can link the real and digital world resulting in efficient energy management, smart mobility and seamless communications. The company has more than fifty thousand employees who work in 56 R&D centers and 20 manufacturing locations worldwide.

Its business growth in the semiconductor market is driven by four areas [11]:

- **Energy Efficiency:** Due to the rising demand for energy, the growing depletion of fossil resources and climate change, smarter and more efficient ways of generating, transmitting, storing, and using energy must be found. The Industrial Power Control (IPC) division makes this possible thanks to advanced IGBT and SIC modules, discrete power devices, industrial power supplies, trains, Intelligent Power Modules (IPM), ICs drivers and MCUs.

- **Mobility:** Society's mobility challenges need to be addressed while also mitigating the environment impact. Infineon's mobility services range from eBikes and eScooters to hybrid and fully electric vehicles to underground and high-speed trains. Developed by the Automotive (ATV) division, some major Infineon products in this area are modules for electromobility, sensors, radars, and connectivity solutions for automated driving and lighting.

- **Security:** In the digital world we live in, being able to communicate while protecting our data is an increasing concern. Infineon secures electronic devices and infrastructure by providing embedded security solutions for electronic devices, computer systems, network components, and industrial facilities.

- **IoT and Big Data:** IoT devices need to be smart, easy, and efficient to link the real with the digital world. Infineon makes the IoT work thanks to its Power & Sensor Systems (PSS) which deliver a wide range of technologies for smart cars, homes, and factories.

The company is a top player in Automotive Semiconductors, Power Discretes and Modules, Microcontroller Suppliers, and about 13 % of its annual revenue are invested into R&D allowing it to continuously expand the patents portfolio, showing a high level of innovative strength.

1.2 Infineon Italy

At Infineon Italy more than 250 professionals create and market leading edge semiconductor for Industrial and Automotive applications in three different sites:

- Milan: Sales team and staff functions,
- Padua: Research and Development Center focused on Automotive products,
- Pavia: Research and Development Center focused on Industrial products.

The Padua site is divided in three internal departments:

- PS & PD: Power Integration Supply and Product Development,
- BP: Body Power,
- MC: Microcontroller.

In particular, this thesis has been developed in the Analog Design team of the PS & PD department, which is focused on PMIC for automotive applications.

1.3 Overview of the Work

The current automotive market trends push toward an ever-increasing integration of electronic devices such as microcontrollers, sensors and radars in modern cars which impose specific characteristics to the supply systems. In particular, radars require to avoid the introduction of disturbances in the base-band range below a given frequency threshold. Such a threshold, in the considered applications, is fixed at 25 MHz and it is destined to further increase.

This work of thesis is collocated in the wake of a research project aimed at developing high-frequency and low-noise dc-dc converters for automotive applications. More specifically, the focus is put on the analysis and the development of a buck Power Stage optimized for the switching frequency of 100 MHz, in the face of the range between 1 MHz and 2.5 MHz typically targeted by Infineon® products.

The thesis will be structured in the following way:

- Chapter 2 introduces the dc-dc conversion topic and provides a simple steady-state analysis of the buck converter operation in *Continuous Conduction Mode*. An overview of some of the most important loss sources in the converter will be given as well;
- Chapter 3 presents and describes the Power Stage of the high-frequency converter to develop and provide an analysis based on simulation results. Some important criticalities of the original design are pointed out.
- Chapter 4 presents an analysis of the switching transients of the *power switches* in the *Commutation Cell*. First, the classic scenario of the switches realized to single MOSFET will be considered, and then an interpretation of the innovative cascode configuration behavior will be given;
- Chapter 5 illustrates an alternative design for the *Internal Supply Generator* in the power stage and carries out a comparison with the original circuit;
- Chapter 6 proposes a possible implementation of the *OL Driving Chain*, which is a driving mechanism inside the new design, which had been kept ideal in Chapter 5;
- Chapter 7 provides some final considerations and depicts a perspective on future possible developments.

Chapter 2

Buck Converter Basics

Power electronics deals with the processing of electrical power by means of electronic devices. A system of particular interest in this field is the *switching converter*. In general, a switching converter presents power input and control input ports, and a power output port. The input control specifies how to process the raw input power which is converted into the conditioned output power. Several basic functions can be performed, and in this thesis, the focus is put on dc-dc conversion where the dc input voltage is converted to a dc output voltage having a larger or smaller magnitude, eventually with opposite polarity or with isolation of the input and output ground references.

It is nearly always desired to produce a well-regulated output voltage, even in presence of variations in the input voltage and load current, hence control is invariably required. Then, an essential feature in any power electronic system, and specifically in dc-dc converters, is *high efficiency*. Surely this is true in order to reduce costs associated with energy consumption and in general to save energy, but the main reason for which high efficiency is often a fundamental requirement lies in market feasibility constraints. To better present this idea let us consider the following definition for the efficiency η of a converter having output power P_{out} and input power P_{in}:

$$\eta \triangleq \frac{P_{out}}{P_{in}}. \tag{2.1}$$

The power lost in the converter is:

$$P_{loss} = P_{in} - P_{out} = P_{out}(\frac{1}{\eta} - 1) \tag{2.2}$$

Equation (2.2) shows that, if the efficiency is low and the output power is substantial, then so is the loss power. The latter is converted into heat from dissipative elements along the power path, and causes the electronic elements within the converter to operate at high temperature, leading to a reduced reliability. Hence, a large and expensive cooling system becomes needed or, at high output power, it may be impossible to adequately cool the converter elements[8].

Then it is clear that increasing the efficiency is the key to reach and work with higher output power. For example, if the converter efficiency is 90%, then the converter loss power is equal to only 11% of the output power, and since very little power is lost the converter element can be packaged with high density, leading to a converter of small size, and less exposed to temperature rise.

But how is it possible to realize converters dissipating negligible power? The basic idea is to employ elements that, at least ideally, do not dissipate energy. For this reason, capacitor and magnetic devices, which meet this requirement, are important elements in switching converters, while they are usually avoided wherever possible in conventional signal processing applications, because of their large size and the difficulty of incorporating them into integrated circuits. Instead, it is the resistive element as well as the linear-mode semiconductor device to be avoided in dc-dc converters realization. Switched-mode semiconductor devices are also employed. A semiconductor device operating in the off-state does not conduct current, hence its power dissipation is zero. Similarly, when the semiconductor device operates in the on (saturated) state, its voltage drop is small and hence its power dissipation is also small. In both cases the power consumption of semiconductor device is low. In conclusion, capacitive and inductive elements, as well as switched mode semiconductor devices are suitable for synthesis of high efficiency converters[15].

Let us consider now the commutation cell showed in Fig 2.1, where the switches S_1 and S_2 operate in a periodic fashion with period T_s, and coordinated so that when S_1 is ON S_2 is OFF, and vice versa. Let's call t_{on} the time subinterval in which S_1 is ON, and t_{off} the time subinterval in which S_1 is OFF. Then let's define as *duty cycle* D the fraction of the period in which S_1 is ON:

$$D \triangleq \frac{t_{ON}}{T_s}.$$

Notice that, as a proper fraction, the duty cycle takes value in the interval $[0, 1]$.

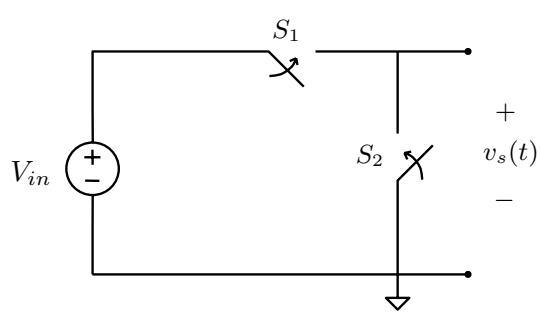


Figure 2.1: Commutation Cell

The output voltage $v_s(t)$ of such a commutation cell is equal to the converter input voltage V_{in} during t_{on}, and it is equal to 0 during t_{off}. The output $v_s(t)$ is then a rectangular waveform having period T_s and frequency $f_s = 1/T_s$, as shown in Fig. 2.2.

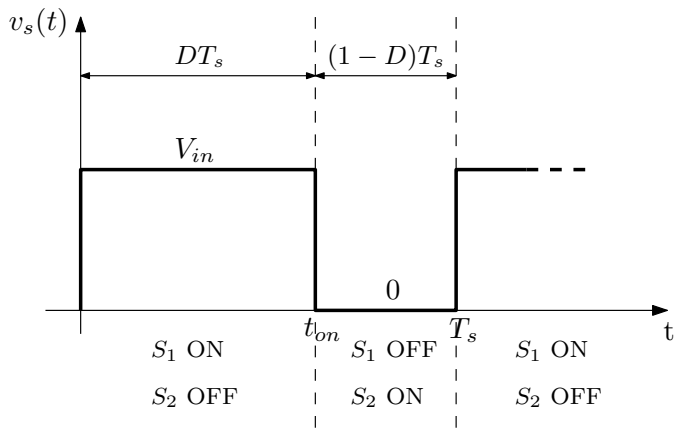


Figure 2.2: Commutation Cell Rectangular Output Voltage

The balance between the subintervals t_{on} and t_{off} determines the dc component of the output voltage. In fact from Fourier analysis we know that the dc component of a periodic waveform is equal to its average value. Hence, the dc component of $v_s(t)$ is

$$V_s = \frac{1}{T_s}\int_t^{t+T_s} v_s(t)\ dt = DV_{in} \tag{2.3}$$

Thus, it is possible to select the desired dc component of the output of the commutation cell by choosing the appropriate duty cycle. For example, if $V_{in} = 10\ V$ and we want a $v_s(t)$ with a dc component of $8\ V$, we will have to select $D = 0.8$.

Anyway, as it has already been pointed out, the switch output voltage waveform $v_s(t)$ is a rectangular waveform and, together with the desired dc component V_s, it also contains harmonics at frequencies which are integer multiples of the fundamental switching frequency f_s. In most applications these harmonics must be removed, such that the output voltage is essentially equal to the dc component, $V_o = V_s$. A LC low-pass filter may be used for this purpose as it is shown in figure Fig. 2.3.

If the filter corner frequency f_0 is sufficiently less than the switching frequency f_s, then the filter heavily attenuates the harmonics and essentially passes only the dc component of $v_s(t)$. The example of the converter shown Fig. 2.3 is called *buck converter* because it reduces the dc voltage. Let us notice that, as long as the switches, the inductor and the capacitor are ideal, the efficiency of those dc-dc converter approaches 100%. In order to perform other power processing functions other kinds of converters can be constructed, but this work of thesis revolves around the analysis and the development of a buck converter, whose generic steady-state behavior will be treated in the next paragraph.

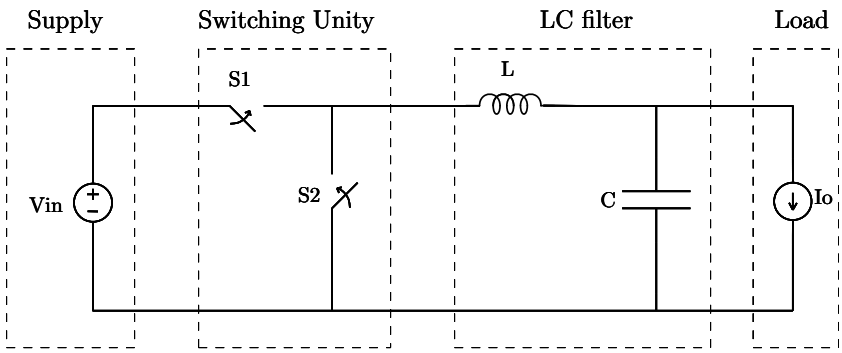


Figure 2.3: Buck Converter Topology

2.1 Steady State Operation: Continuous Conduction Mode

In the previous section, an introductory description of the buck converter as a means of reducing a dc voltage using only ideal non dissipative elements has been given. Now, a brief treatment of the operation of the buck converter will be carried out under the condition of *Steady-State*. This condition is characterized by the assumption that the voltage and current waveforms in the circuit repeat themselves periodically with period T_s. In particular:

$$i_L(t + kT_s) = i_L(t),$$

and

$$v_c(t + kT_s) = v_c(t)$$

For every natural number k and for every real t in the range $[0, T_s]$, where $i_L(t)$ and $v_c(t)$ are the current throughout the filter inductor and the voltage across the filter capacitor respectively, with the polarities showed in Fig. 2.3. Plus, this analysis will be referred to the *Continuous Conducting Mode* (CCM) *operation*, which consists in assuming that the inductor conducts positive current all the time:

$$i_l(t) > 0, \ \forall t.$$

Let us now introduce two principles and an approximation which will turn to be useful in order to present a more compact and simple analysis of the buck converter operation:

Small Ripple Approximation

As it has already been pointed out in the previous section, a filter is needed in order to pass the dc component of $v_s(t)$ but to reject the harmonics at frequency multiple of f_s. Nevertheless it is impossible to build a perfect low-pass filter to

accomplish such a task. So the low-pass filter must allow to reach the output at least some small amount of the high frequency harmonics generated by the switch cell. Hence, the output voltage waveform $v_o(t)$, will be actually made by the sum of a dominant desired dc component Vo and a very small ripple $v_{ripple}(t)$:

$$v_o(t) = V_o + v_{ripple}(t)$$

as illustrated in Fig. 2.4.

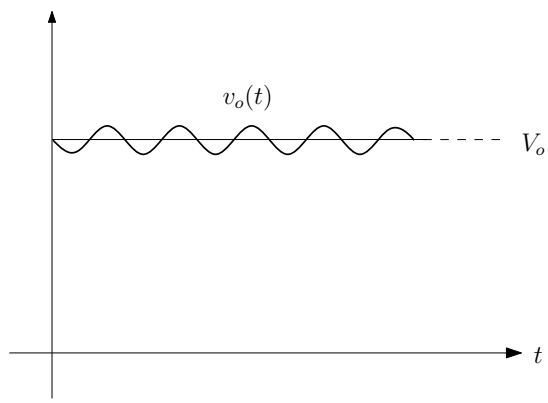


Figure 2.4: Output Voltage Ripple

Since the purpose is to produce a dc output, the voltage switching ripple should be small in any well designed converter (typically less than 1% compared to the dc level). So we can assume:

$$|v_{ripple}| << V_o$$

Therefore, it is possible to neglect the small ripple term $v_{ripple}(t)$ and to consider the output voltage well approximated by its dc component:

$$v_o(t) \approx V_o$$

Throughout the following sections this approximation, known as *small ripple approximation*, will be adopted, in that it allows to greatly simplify the analysis of the converter waveforms.

Inductor Volt-Second Balance Principle

The *Inductor Volt-Second Balance Principle* states that the time integral over a period of the voltage across an inductor in a periodic steady-state regime is always zero:

$$\int_t^{t+T_s} v_L(t)dt = 0, \ \forall t > 0. \tag{2.4}$$

The inductor volt-second balance principle may even be rephrased in the following equivalent way: the average value of the voltage across an inductor operating in steady-state periodic regime is null:

$$V_L = \frac{1}{T_s}\int_t^{t+T_s} v_L(t)dt = 0,\ \forall t > 0. \tag{2.5}$$

This principle statement can be easily proved by combining the concept of steady-state, for which:

$$i_L(t) = i_L(t+T_s),\ \forall t > 0,$$

and the voltage-current relation imposed by an ideal inductor:

$$v_L(t) = L\frac{di_L(t)}{dt}$$

In particular, integrating in time both members of this equation over a period we find:

$$\int_t^{t+T_s} v_L(t)dt = L[i_L(t+T_s) - i_L(t)] = 0$$

Capacitor Ampere-Second Balance Principle

Similarly, the *Capacitor Amp-Second Balance Principle*, or *Charge Balance Principle*, states that the time integral over a period of the current through a capacitor in a periodic steady-state regime is always zero:

$$\int_t^{t+T_s} i_C(t)dt = 0,\ \forall t > 0. \tag{2.6}$$

The capacitor amp-second balance principle may even be rephrased in the following equivalent way: the average value of the current through a capacitor operating in steady-state periodic regime is null:

$$I_C = \frac{1}{T_s}\int_t^{t+T_s} i_C(t)dt = 0,\ \forall t > 0. \tag{2.7}$$

This principle statement can be easily proved by combining the concept of steady-state, for which:

$$v_C(t) = v_C(t+T_s),\ \forall t > 0,$$

and the voltage-current relation imposed by an ideal inductor:

$$i_C(t) = C\frac{dv_C(t)}{dt}$$

In particular, integrating in time both members of this equation over a period we find:

$$\int_{t}^{t+T_s} i_C(t)dt = C[v_L(t+T_s) - v_L(t)] = 0$$

2.1.1 Buck Waveforms Analysis

Inductor Voltage

Let us consider now the waveform of the voltage across the inductor during a switching period. We have:

$$v_L(t) = \begin{cases} V_{in} - v_o(t), & \text{when } 0 \leq t \leq DT_s \\ -v_o(t), & \text{when } DT_s \leq t \leq T_s \end{cases}$$

And using the small ripple approximation it becomes:

$$v_L(t) = \begin{cases} V_{in} - V_o, & \text{when } 0 \leq t \leq DT_s \\ -V_o, & \text{when } DT_s \leq t \leq T_s \end{cases} \tag{2.8}$$

as illustrated in Fig. 2.5.

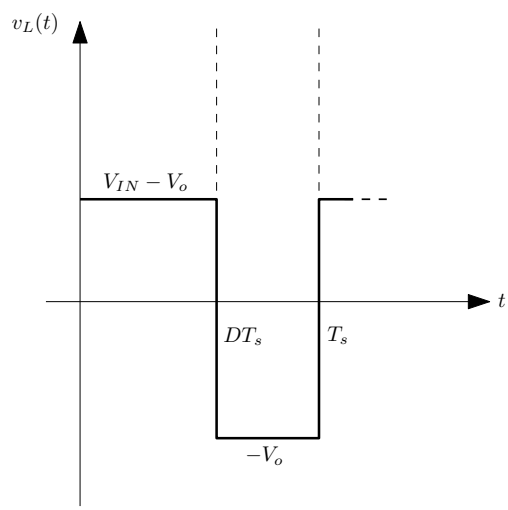


Figure 2.5: Inductor Voltage

Voltage Conversion Ratio

Let us define the *Voltage Conversion Ratio M* of a dc-dc converter as the ratio between the output and the input voltage:

$$M \triangleq \frac{V_o}{V_{in}} \tag{2.9}$$

Let us focus now on the case of a buck converter in Continuous Conduction Mode. Consider the inductor voltage shown in Fig. 2.5. From the inductor Volt-Second balance principle, we have:

$$\int_0^{T_s} v_L(t)dt = 0$$

from which:

$$(V_{in} - V_o)t_{on} - V_o t_{off} = 0,$$

And dividing both the members for the switching period T_s:

$$(V_{in} - V_o)D - V_o(1 - D) = 0$$

From which we get the voltage conversion ratio:

$$\frac{V_o}{V_{in}} = M = D \tag{2.10}$$

And we can conclude that the voltage conversion ratio of a buck converter in steady-state operating in CCM is equal to the duty cycle.

Inductor Current

Let us now consider the current through the inductor. From the Kirchhof Current Law (KCL) we have:

$$i_L(t) = i_C(t) + i_o(t)$$

From the linearity of the average function, the same relation stands for the average values:

$$I_L = I_C + I_o.$$

For the Charge Balance Principle, in steady-state the average current through the capacitor is null, so we have:

$$I_L = I_o. \tag{2.11}$$

Let's now consider the Current-Voltage relation for the ideal inductor:

$$v_L(t) = L\frac{di_L(t)}{dt}$$

According to (2.8), the voltage across the inductor $v_L(t)$ is a periodic step function that oscillates between two different constant values, and so is $\frac{di_L(t)}{dt}$ as a consequence. In particular we have:

$$\frac{di_L(t)}{dt} = \begin{cases} \frac{V_{in}-V_o}{L}, & \text{when } 0 \leq t \leq DT_s \\ -\frac{V_o}{L}, & \text{when } DT_s \leq t \leq T_s \end{cases} \tag{2.12}$$

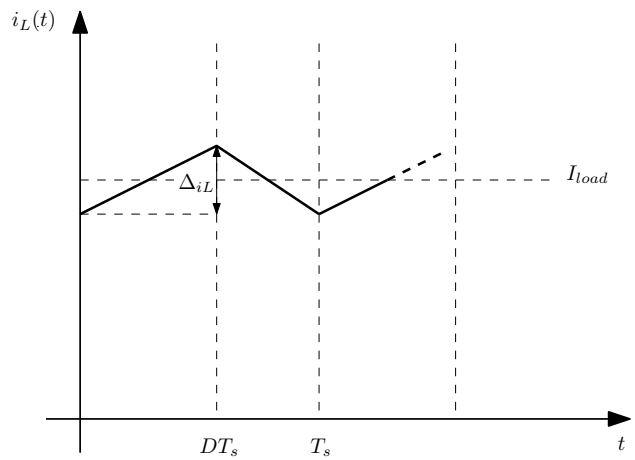


Figure 2.6: Inductor Current

A sketch of the current inductor is shown in Fig. 2.6.

It is possible to have two alternative expressions for the current ripple Δ_{iL} by integrating the current over the interval $[0, t_{on}]$ or $[t_{on}, T_s]$, and what we get is:

$$\Delta_{iL} = \frac{V_{in} - V_o}{L} DT_s = \frac{V_{in}}{f_s L}(1 - M)M \tag{2.13}$$

$$\Delta_{iL} = \frac{V_o}{L}(1 - D)T_s = \frac{V_o}{f_s L}(1 - M) \tag{2.14}$$

(**??**), which assumes V_{in} to be constant and independent from M, is shown graphically in Fig. 2.7, while (2.14), which assumes V_o to be constant and independent on M is shown graphically in Fig. 2.8.

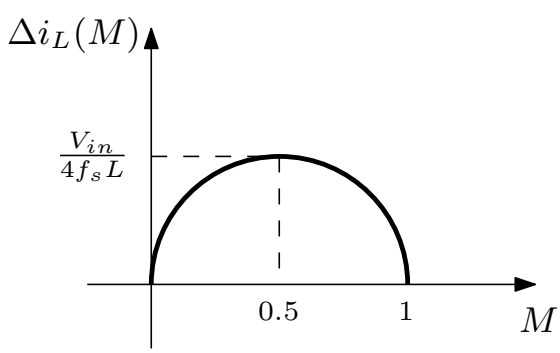


Figure 2.7: Current Ripple, V_{in} Fixed

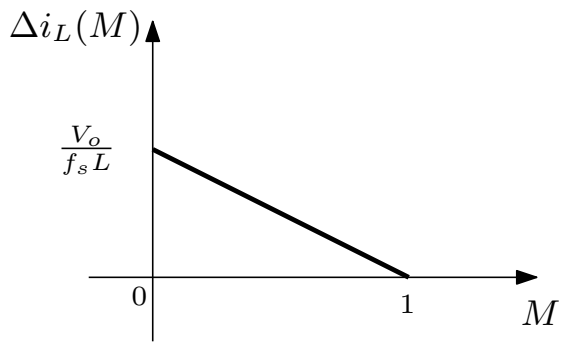


Figure 2.8: Current Ripple, V_o Fixed

Output Voltage Ripple

Now we want to estimate the peak-to-peak variation (ripple) of the output voltage. We have:

$$i_C(t) = i_L(t) - I_o$$

assuming a constant output load current. Fig. 2.9 gives a representation of the capacitor current. The peak-to-peak variation of the output voltage $v_o(t) = v_C(t)$ is given by double the charge Q entering in the capacitor during the time sub-interval in which $i_C(t) > 0$ and the capacitance value C:

$$\Delta_{Vo} = \frac{Q}{C} = \frac{\Delta_{iL}}{8 f_s C} \tag{2.15}$$

and by Δ_{iL} with the expression given by (2.14), the output voltage ripple Δ_{Vo} may be rewritten as follows:

$$\Delta_{Vo} = \frac{V_o}{8 f_s^2 LC}(1 - M) \tag{2.16}$$

2.1.2 Design Considerations

From (2.13) we get:

$$L = \frac{V_{in}}{f_s \Delta_{iL}}(1 - M)M \tag{2.17}$$

From (2.17), it is particularly evident that is possible to fix a maximum limit $\Delta_{iL,max}$ for the current ripple by selecting a sufficiently big inductor, as showed respecting the following inequality:

$$L_{min} \geq \frac{V_{in}}{f_s \Delta_{iL,max}}(1 - M)M \tag{2.18}$$

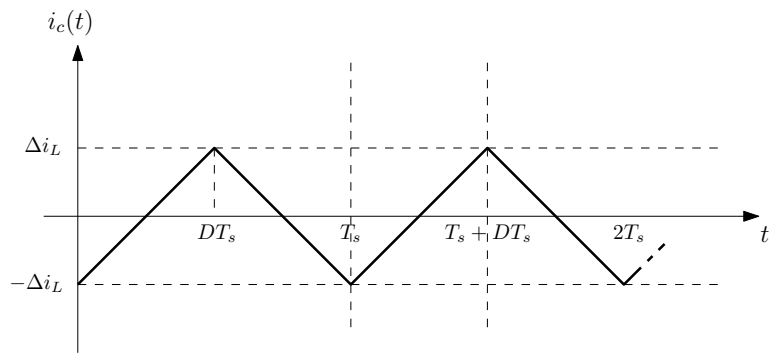


Figure 2.9: Capacitor Current

Then, once the inductance value has been fixed, it is theoretically possible to obtain an arbitrary small output voltage ripple by selecting a sufficiently big capacitance value, according to the following inequality:

$$C_{min} \geq \frac{\Delta_{iL}}{8 f_s \Delta_{Vo,max}} \tag{2.19}$$

which has been obtained by reversing (2.15).

Looking at (2.13) and (2.16) it is possible to notice that the current and voltage ripples are inversely proportional to the switching frequency and to its square respectively. Dc-dc converters are typically very expensive and bulky, and this is typically due to the presence of capacitors and inductors, which by themselves occupy more area and cost than the entire chip. Previous consideration show that it is theoretically possible to employ smaller values of filter capacitance and inductance, and still get the target ripples by operating at a higher switching frequency. This observation suggests that high frequency operation opens the possibility for the integration of the inductor, thus saving a lot of area and cost to the manufacturer.

2.2 Sources of Losses in DC-DC Buck Converters

The treatment developed so far leads to associate the dc-dc buck converter with a 100 % efficiency in that, as mentioned, it has been built with ideal lossless components. Nevertheless, in order to implement the switches and the passive LC filter, real components are employed, which introduce intrinsic and parasitic dissipative effects, leading to a degradation of the ideal efficiency.

In this section, an overview of three of the most important energy losses in a dc-dc converter will be given. In particular, those associated with the switches' operation will be considered:

- Conduction losses;

- Switching losses;
- Driving losses.

2.2.1 Conduction Losses

During the ON phase, the MOSFETs implementing the power switches S_1 and S_2 work in the triode region and conduct approximately the load current I_{load}. According to the model presented in [13], the MOSFET drain current in the triode region is given by:

$$I_D = k'_n \frac{W}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.20}$$

where the case of an nMOSFET has been described. Recall that the triode region is characterized by the following condition:

$$0 < V_{DS} < V_{GS} - V_{th} \triangleq V_{ov}.$$

In particular, if $|V_{DS}| << |V_{GS} - V_{th}|$, then (2.20) can be approximated as:

$$I_D \approx k'_n \frac{W}{L} V_{ov} V_{DS}. \tag{2.21}$$

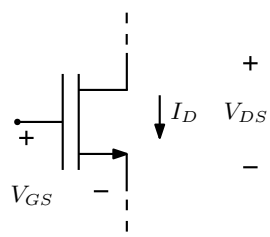


Figure 2.10: nMOSFET

Let us notice that (2.21) depicts a proportional relation between the current I_D and the voltage V_{DS}. For this reason, the triode region is even called *linear region*, and the behavior transistor channel can be modeled as an equivalent resistance:

$$R_{DS,ON} \triangleq \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{k'_n \frac{W}{L} V_{ov}}. \tag{2.22}$$

Since MOSFETs that implement the power switches work in linear region during the ON phase, in this condition they give place to losses associated to this equivalent resistance, and such losses, namely *Conduction Losses*, can be approximated with:

$$P_{cond} = R_{DS,ON} \cdot I_{D,s}^2, \tag{2.23}$$

where $I_{D,s}$ is the RMS value of the drain current conducted by the switch. It is clear from (2.23) that conduction losses are particularly relevant at high output currents. They can be minimized by minimizing $R_{DS,ON}$, and this result is typically achieved by maximizing the width of the transistors. It is worth mentioning that the inductor's *Equivalent Series Resistor* causes an increase in conduction losses as well, as it is placed in series with the $R_{DS,ON}$ of the switches.

Notice that, for given duty cycle, input voltage and output current, the voltage drops across these equivalent resistances decrease the output voltage, the output active power, and the power efficiency as a consequence.

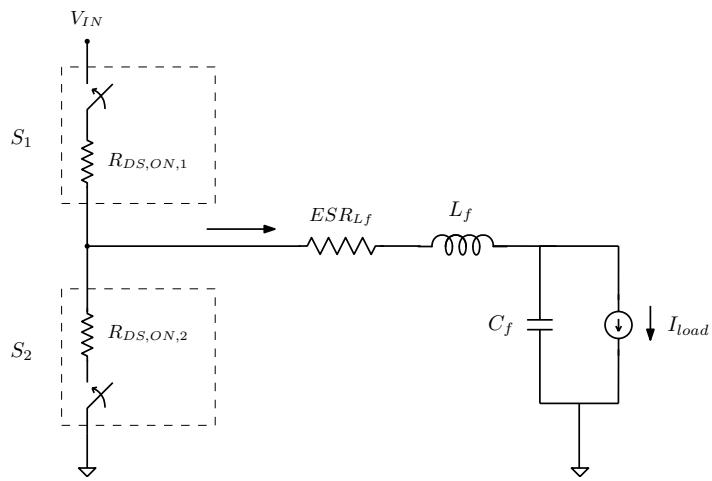


Figure 2.11: Conduction Losses

2.2.2 Switching Losses

These losses are associated with the fact that in real switches the commutations are not instantaneous, like it happened in the ideal case, but they require finite non-zero time, namely the *switching time*. During these time intervals, the switches experiment a transient (that will be better analyzed in Chapter 4) during which both the current through the MOSFET channel and the voltage across it are not null and not negligible. Such a situation is sketched in a simplified form in Fig. 2.12.

By looking at the device instantaneous power dissipation shown in Fig. 2.12, and by using a piece-wise linear approximation, the switching losses can be easily inferred:

$$\begin{cases} P_{sw,on,1} \approx \frac{V_{IN} I_L}{2}(t_{ri} + t_{fv}) f_s, & \text{considering the } S_1 \text{ turn-on intervals} \\ P_{sw,off,1} \approx \frac{V_{IN} I_L}{2}(t_{rv} + t_{fi}) f_s, & \text{considering the } S_1 \text{ turn-off intervals} \end{cases}. \tag{2.24}$$

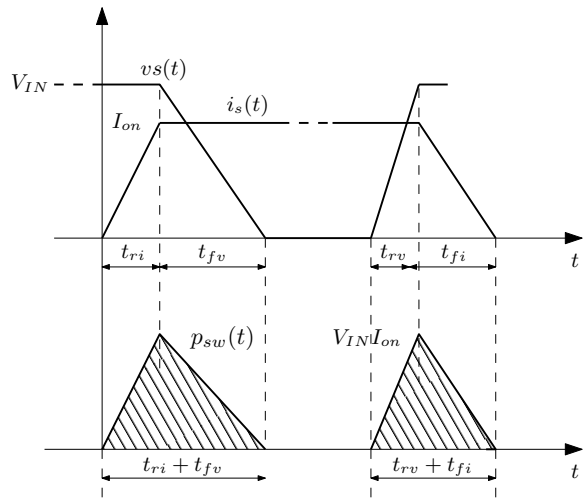


Figure 2.12: Switching Losses

where I_L represents the constant inductor current under the assumption that the inductor peak-to-peak current ripple Δi_{Lpp} can be neglected. Nevertheless, it is important to observe that, if the inductor current ripple cannot be neglected, the above analysis remains valid provided that the switching current is substituted by the peak or valley inductor current at turn-off and turn-on, respectively. In fact, being the total turn-on and turn-off switching intervals much smaller than the switching period, the inductor current can still be considered constant during these intervals, thus justifying the substitution of the inductor with a current generator. In this case, the total average switching losses are

$$P_{sw,1} \approx \frac{V_{IN}I_L}{2}(t_{ri}+t_{fv}+t_{rv}+t_{fi})f_s + \frac{V_{IN}I_L}{4}\frac{\Delta i_{Lpp}}{I_L}(-t_{ri}+t_{fv}-t_{rv}+t_{fi})f_s. \tag{2.25}$$

Notice that from (2.25) it is clear that increasing the switching frequency f_s has a negative impact on the switching losses.

2.2.3 Driving losses

The last contribution to the degradation of the efficiency that will be presented here comes from the driving losses[5]. Driving losses refer to the power that is needed to turn on the transistor that realizes the power switches. From the model in [10], they can be approximately quantified by the following expression:

$$P_{drv} = C_G \cdot V_{drv}^2 \cdot f_s, \tag{2.26}$$

where C_G is the gate capacitance of the MOSFET that realizes the switch and V_{drv} is the voltage imposed at the gate-source port to turn the switch on. Notice

that, minimizing the width of the transistor, the gate capacitance is reduced and the driving losses as well, as oppose to what happened to the conduction losses. Therefore, optimal sizing of the power switches should be calculated keeping all these loss contributions into account. Notice even that, similarly to what happened for the switching losses, the driving losses increase for higher switching frequencies.

Chapter 3

VHF Buck Converter: Analysis

One of the major trends that nowadays is animating the automotive power supply market is the transition to Pre/Post regulation architecture. The traditional approach to supply all the electronic devices of a car is direct conversion: each block has its own dedicated dc-dc converter that scales down the voltage delivered by the battery to the desired level. Instead, in the Pre/Post regulation approach, the battery voltage is initially scaled down to an intermediate level from a so-called pre-regulator. This intermediate voltage represents the input of successive dc-dc conversion stages, called post-regulators, that provide the different needed input voltages to all the devices to supply. In face of an increased complexity of the architecture of the supply system, the transition towards Pre/Post regulation solutions offers two clear advantages: the energetic efficiency of the system is improved, and it simplifies the thermal design, since it is easier to thermally isolate circuits which are referred to different voltage domains.

3.1 Testbench

The battery of a car typically provides a 12 V voltage that, as previously explained, is stepped down from a pre-regulation stage at an intermediate level which, in general, may belong to the range between 3 V and 8 V. This voltage, as mentioned earlier, represents the input voltage for the dc-dc converters of the following post-regulation stage.

In particular, the buck converter that will be analyzed in this thesis has been designed in order to operate in the post-regulation domain and to sustain input voltages up to 4 V. Moreover, it is supposed to work with load currents up to 2 A and it is optimized for a load current of 1 A, which are typical conditions in automotive applications.

In this thesis the focus has been put on the analysis and the development of

the power stage of the converter, which performs the basic power conversion from the input voltage to the output voltage. For this reason, all the considerations and all the simulations will be referred to testbenches of the power stage in open loop, neglecting all the aspects inherent in the control problem. Fig. 3.1 features the scheme of such a testbench, where the commutation cell of the power stage has been included together with a set of blocks whose task is the functional processing of the control input. In the following section a brief overview of each block functionality will be given. Notice that the power stage is operated in open loop, and that the control input signal is provided by an ideal voltage waveform generator which models a *Pulse Width Modulator* (PWM). Notice even that, since the control aspects are being neglected, the duty cycle may be arbitrary fixed depending on the desired output voltage. For example, considering that $V_{in} = 3.6V$, and referring to equation (2.10), if an output voltage $V_o = 1.8V$ is desired, then a duty cycle of about 0.5 will have to be selected.

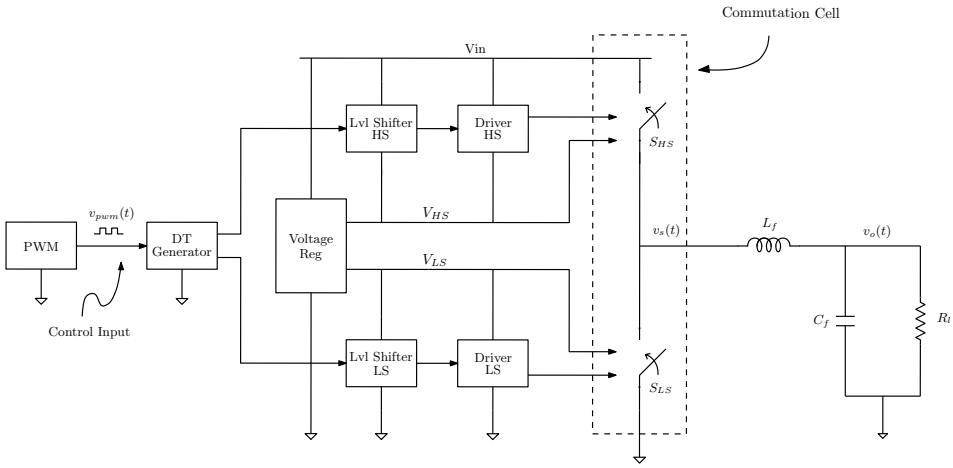


Figure 3.1: Testbench Concept

3.2 Blocks Overview

Commutation Cell

The *Commutation Cell* contains the power switches and represents the core of the converter power stage. It performs the conversion from the input dc voltage V_{in} to the rectangular voltage $v_s(t)$ whose dc component corresponds to the output dc level V_o.

In the design process of a converter, particular attention has to be dedicated to this block. It is necessary to properly select a topology and a typology capable of according reliability in the typical operation conditions of the target application, and at the same time, high performances have to be pursued both

in terms of efficiency and area occupation in order to grant the desirable thermal behavior, energy saving, and acceptable costs[16].

When it comes to the converter object of this thesis, it is supposed to operate in the automotive power supply environment, under the typical post-regulation domain conditions. Therefore, it is desirable to manage input voltages up to 5 V and load currents up to 2 A. Another important specification is to target the very high switching frequency of 100 MHz. According competitive performances and a reliable operation with such a set of specifications is not trivial and offers some interesting challenges to the designer.

For instance, the traditional configuration for an integrated buck DC-DC converter Commutation Cell exploits a pMOS and a nMOS to implement the high-side power switch and the low-side power switch respectively, both driven with a tapered chain of inverters. This solution is widely used as it is simple, well known, and potentially able to offer high efficiency. Nevertheless, it presents some important intrinsic limitations as well.

For example, assuming to adopt a given technology, whichever MOSFET is limited by the maximum drain-to source voltage (V_{ds}) it can sustain. In this approach, if this value is not high enough for the target application, it will be needed to adopt a different model with a higher maximum V_{ds}. The new model, though, will most likely be characterized by a bigger minimum channel length, and consequently by a bigger gate capacitance, which will increase the switching time of the transistor. This corresponds to an increasing in the energy loss during a single commutation of the switching cell as well, and most likely to a worse power efficiency of the converter. This scenario, given a fixed technology, opens the problem of selecting the topology for the power switches able to offer the better trade-off between metrics such as maximum voltage stresses sustainable, frequency characteristics, power efficiency, circuit complexity, and area occupation.

In [6], a study has been carried out in order to compare the four different topologies sketched in Fig. 3.2 and to verify which one works best to implement the switching cell. In this study, a technology for automotive application has been adopted, which features several MOS transistors, each with different minimum sizes, maximum sustainable drain-source voltage, threshold voltage, and capacitance. In particular, three types of MOSFET have been considered, each characterized by a different Vds sustainable: a "high voltage" (HV) MOSFET with minimum channel length of approximately 1 μm, a "medium voltage" (MV) MOSFET with minimum channel length of approximately 400 nm, and a "low voltage" (LV) MOSFET with a minimum channel length of approximately 120 nm. The maximum V_{ds} nominally sustainable is, obviously, higher for the HV MOSFET (5 V), intermediate for the MV MOSFET (2.5 V), and lower for the LV MOSFET (1.5 V).

The study underlines that the most attractive topology is the fourth, which is obtained by cascading a LV transistor, used for switching, and a cascaded MV transistor used as protection. In fact, under the typical operating conditions previously mentioned, it potentially allows to reach higher efficiency and to reduce the area occupation. Nevertheless, this solution presents an important

intrinsic disadvantage, which is the maximum sustainable V_{in}, limited to 4 V (V_{ds}(LV) + V_{ds}(MV)).

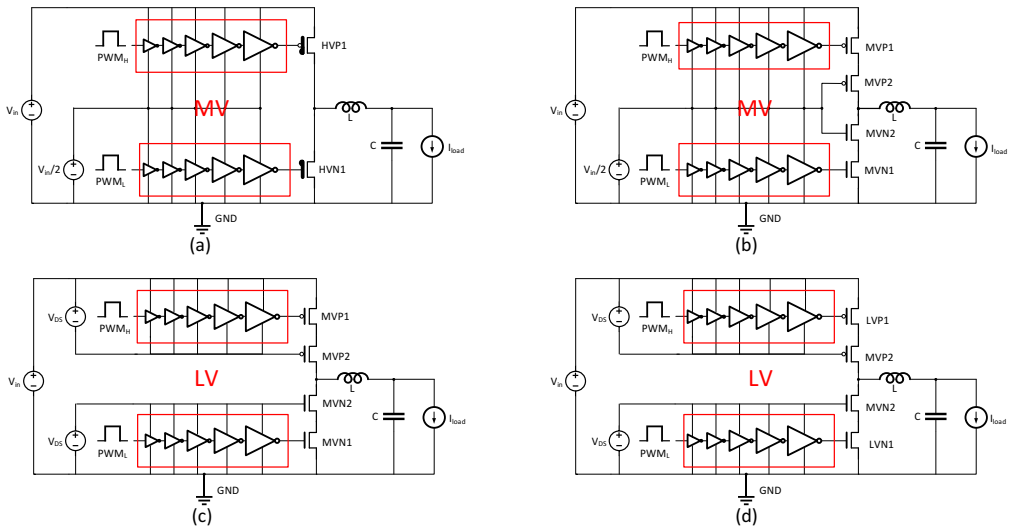


Figure 3.2: Four proposed schematics: (a) HV, (b) MV, (c) MV with LV driving, (d) Hybrid LV+MV.

Driving Buffers

In order to drive each of the transistors of the Commutation Cell with the shortest possible delay and optimizing the energetic behavior, a suitably sized tapered buffer of five inverters, made with LV MOSFET, has been employed. Recall that a CMOS tapered buffer is a chain of CMOS inverters, where every stage needs to be strong enough to effectively drive the following one without loading too much the previous one, and where the last stage drives the load capacitance providing large charging and discharging currents acting as a source/sink resistance.

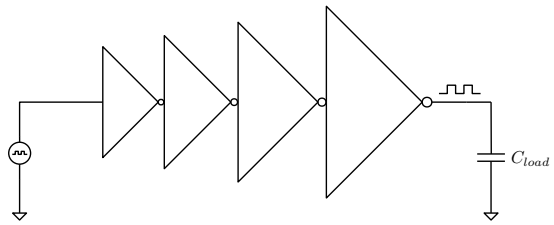


Figure 3.3: Tapered Buffer Principle Scheme

Level Shifters

In general, a level shifter (or level translator) is a circuit used to translate voltage from a logic level, or domain, to another one, allowing compatibility between different blocks.

As an example, referring to Fig. 3.1, let's consider the high-side level shifter. The purpose of the driving chain is to exploit the input control signal delivered by the pulse width modulator to drive the high-side switch. Nevertheless, the PWM signal is a rectangular waveform whose low and high logic levels corresponds to 0 V (ground) and 1.5 V respectively while, in order to drive the high-side switch with a 1.5 volt amplitude signal, it is necessary to have a rectangular waveform between 2.1 V and 3.6 V (which is the supply level). The conversion between these two different voltage domains is exactly the task of the level shifter, as sketched in Fig. 3.4.

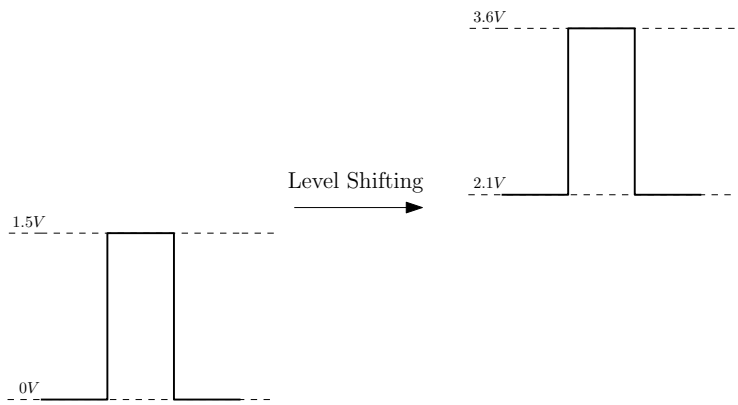


Figure 3.4: Voltage Level Shifting

Dead Time Generator

Ideal switches have zero commutation time, thus, the two switches of the power stage may ideally switch simultaneously. Nevertheless, the real power switches of the commutation cell have finite non-zero commutation time, and so it is important to pay particular attention to avoid short-circuits between them in order to prevent dangerous stresses to the devices and to limit as much as possible losses associated with cross-conduction phenomena. For this reason, a short interval time, namely a *dead time*, is inserted by a specific circuit between the switch-off phase of the high-side switch and the switch-on phase of the low-side switch and vice versa, between the switch-off phase of the low-side switch and the switch-on phase of the high-side switch. In particular, in the converter under analysis, a traditional circuit solution sketched in Fig. 3.5 has been employed to implement this function, and specifically to introduce a dead time of around 300 ps.

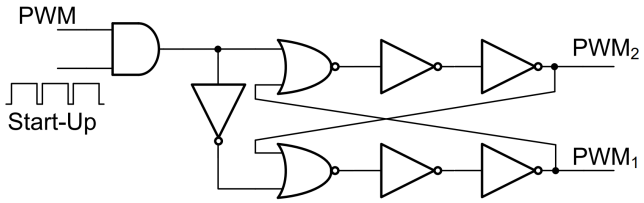


Figure 3.5: Dead Time Generator

Internal Voltage Generator

From Fig. 3.2(d) it is possible to notice that the low supply of the high-side driving chain and the high supply of the low-side driving chain cannot be both set at $V_{in}/2$; instead, they have to be set at a higher and at a lower value respectively in order to prevent the breakdown of the LV drivers. Notice that these two internal supplies have two different functions: firstly, as just mentioned, they set a logic level for the signal used to drive LV transistors of the power switches and, secondly, they are used to bias the cascode MV transistors of the power switches.

The voltage levels in these two internal rails should be set to 1.5 V ("low-side internal supply") and to 2.1 V ("high-side internal supply") in order to produce driving signals with 1.5 V amplitude, which is the maximum that can be used without exceeding the nominal tolerance of the LV transistors of the drivers and of the switching cell. Ideally this may be done by two ideal dc voltage generators as shown in Fig. 3.2(d). This way the two internal supplies are perfectly regulated and constant in time, since the ideal generators are able to source and sink an infinite amount of current instantly.

Nevertheless, when the voltage regulation is not ideal, the need for charging and discharging the intermediate nodes in the drivers and the parasitic capacitances in the power switches gives place to a high-peak impulsive current that has to be sourced/sink by the real regulator, causing some periodic perturbations in the two rails. These perturbations in the internal supplies may cause a drop in the expected efficiency, and risk to damage the transistor in the driver chains.

The scheme of the circuit initially used to implement the voltage regulator is shown in Fig. 3.6.

In this solution, the two voltages are obtained with a stack of diodes per rail (the two pMOS D_1 and D_2 for the high-side, and the two nMOS D_3 and D_4 for the low-side) with the bias resistor R in the middle. In order to mitigate as much as possible, the mentioned perturbations in the voltage rails, capacitors C_1 and C_2 have been added, and their capacitance value need to be as high as possible according to:

$$\Delta V = Q/C \tag{3.1}$$

where ΔV is the voltage variation that takes place in the rail when the charge

package Q arrives.

In the original design, 300 pF capacitance for each side have been integrated.

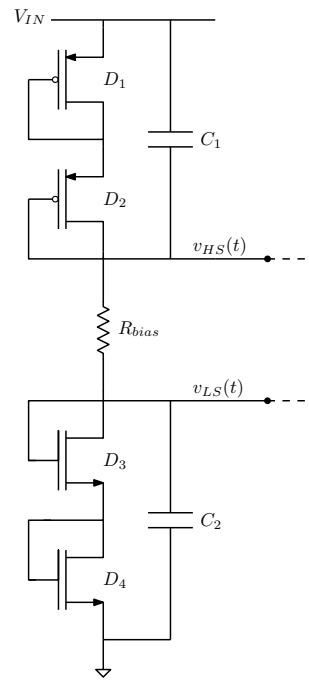


Figure 3.6: Original Internal Supplies Generator

3.3 Main Waveforms from Simulation

In this section, some meaningful waveforms will be showed and commented in order to describe the overall behavior of the converter under analysis. The waveforms are taken from a transient simulation ran on an open loop testbench for the power stage, under the following operating conditions:

- $V_{in} = 3.6\ V$: it is a typical value for the input voltage in automotive post-regulation domain, and it is close to the superior sustainable limit for the designed commutation cell;
- $I_{load} \approx 1\ A$ (around 935 mA): the maximum load current required given as a specification is 2 A, but assuming that the power stage will rarely have to work at maximum load current, this represents a more representative condition (half of the maximum value);
- $f_s = 100\ MHz$: this is the target switching frequency for this converter;
- $D = 0.5$: as an arbitrary choice, a voltage close to 1.8 V is targeted;

Output Voltage: $v_{out}(t)$

Fig. 3.7 shows the voltage $v_{out}(t)$ at the output of the converter.

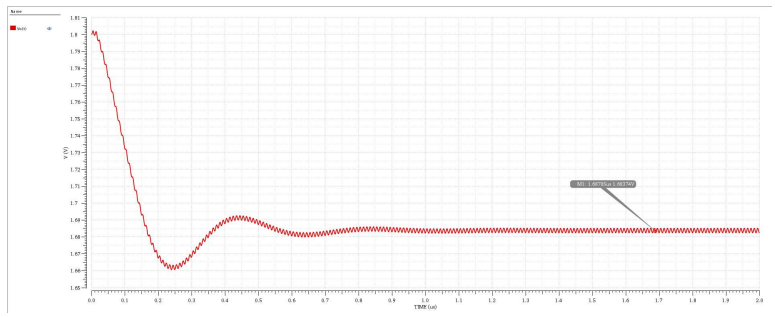


Figure 3.7: Converter Output Voltage

According to (2.10) a voltage of 1.8 V is expected. Instead, notice that the dc component $v_{out}(t)$ is slightly smaller:

$$V_{out} \approx 1.68\ V$$

The explanation of this mismatch lies on the fact that (2.10) has been derived analyzing an ideal model of the converter, in which no losses have been considered. Instead, taking into account loss sources, and in particular the conduction losses in the power switches, leads to a lower estimation of the conversion ratio of the converter, and consequently, given a fixed V_{in}, to a lower V_{out} expected. This idea may be easily caught even by inspecting the voltage waveform $v_s(t)$ at the output of the commutation cell, which is showed in Fig. 3.8. According to the ideal lossless model this should be a periodic rectangular waveform:

$$v_s(t) = \begin{cases} V_{in}, & \text{when } 0 \leq t \leq DT_s \\ 0, & \text{when } DT_s \leq t \leq T_S \end{cases}$$

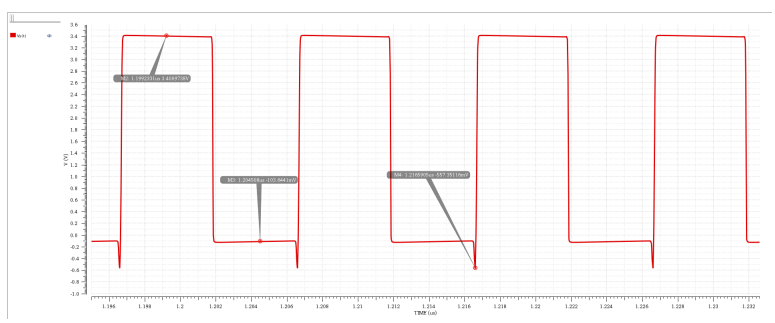


Figure 3.8: Converter Switching Node Voltage

Instead, it is evident that the high value is not V_{in}, but it is about 200 mV lower. This reduction corresponds to the voltage drop across the high-side switch during its on-phase. In fact, when the transistors that implement the switch are on, they work in the triode region, can be modeled with a resistor R_{on}, and are crossed by a current approximately equal to the load current. In order to minimize the equivalent resistance value, and the conduction losses as a consequence, a very large width has been selected for the power switches ($W \approx 40mm$).

Other two qualitative interesting observations can be carried out about the $v_s(t)$ waveform:

- During the t_2 subinterval, the voltage level across the low-side transistor is negative (around –110 mV) and not zero as expected from the ideal model. This corresponds to the voltage drop that appears across the channel and the body diode when the low-side power switch is ON, and when it is crossed by a current approximately equal to Iload. Notice that this effect contributes as well to lower the dc voltage of $v_s(t)$, and hence to explain the mismatch between the ideal and the real output V_o.

- During the dead time before the turning on of the high-side power switch, there is a very brief voltage negative peak in $v_s(t)$, the reaches down to about -550 mV. This is a consequence of the turning-off of the low side switch. In fact, by setting $v_{gs}(t)$ to zero, the channel disappears, and the conductive path is then represented only by the body diode which is much less conductive than the channel, leading to a significantly bigger voltage drop.

Let's focus now on the ripple in the output voltage, featured in Fig. 3.9. Notice that its peak-to-peak amplitude (about 2.71 mV) is very close to that expected from the theory presented in Chapter 2. In fact, from (2.16) we have:

$$\Delta v_{o,exp} = 2.625 \ mV$$

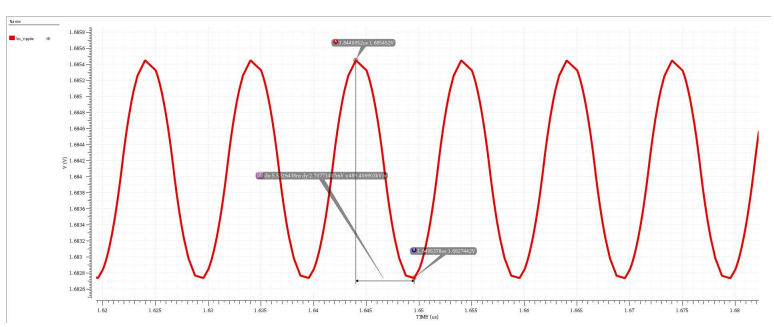


Figure 3.9: Output Voltage Ripple

As a final consideration, notice that with the selected filter, the peak-to-peak

ripple on the output voltage is relatively small, limited to less than 0.2 % of the dc level.

Inductor Current

Fig. 3.10 shows a view of the inductor current and the load current after the converter has entered steady-state. As expected from the theory, once the converter is working in the steady-state condition, the load current I_{load} essentially corresponds to the dc level of the inductor current. In the testbench we are referring to, the load has been modeled by a 1.8 Ω resistor, and being $V_o \approx 1.68$ V, it can actually be observed that:

$$I_{load} \approx \frac{V_o}{R_l} = 934mA,$$

as shown in the figure.

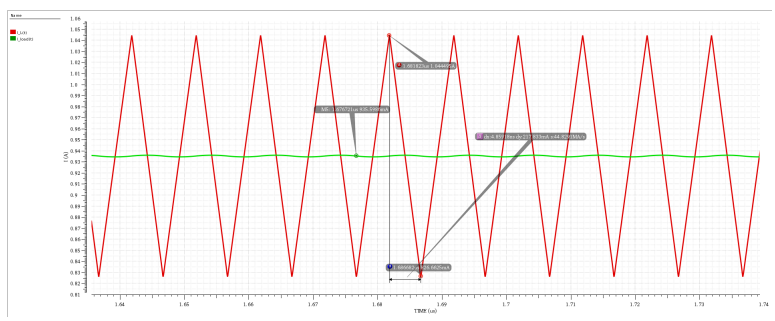


Figure 3.10: Load and Inductor Currents

The inductor current peak-to-peak ripple observed is $\Delta_{iL} = 217\ mA$. While, according to (2.13), the expected peak-to-peak current ripple in the inductor should be $\Delta_{iL,exp} = 224\ mA$.

Again, (2.13) is an estimation based on a simple ideal model, thus the indication taken from it is not expected to be exact. Nevertheless, as we can notice, it is accurate enough, and it actually can be used to set a first-hand sizing of the output filter inductor. Let us also notice that the dc level of the current inductor, which is imposed by the load, is much larger than the amplitude of the current ripple Δ_{iL}, and so the converter works in CCM with an important margin before the arise of the DCM. Notice that in this converter the secondary switch is implemented by a current-bidirectional structure made by two stacked nMOSFETs. For this reason, it is anyway supposed to stay in CCM along its operation.

Control Signal

The red curve of Fig. 3.11 represents the control input of the converter delivered by the pulse width modulator after having being processed by the control

system. Nonetheless, as previously mentioned, this is a testbench referred to the power stage in open-loop, and so the control input signal is directly delivered by an ideal waveform generator. Let us notice that it is a periodic rectangular waveform, whose low and high levels are 0 V and 1.5 V respectively, and whose duty cycle has been arbitrarily fixed to 0.5:

$$v_{pwm}(t) = \begin{cases} 1.5V, & \text{when } 0 \leq t \leq DT_s \\ 0V, & \text{when } DT_s \leq t \leq T_s \end{cases}$$

where $T_s = 1/f_s$ is the switching period. On the other side, the green curve of Fig. 3.11 represents the control input of the high-side power switch downstream of the driving chain. In other words, it is the pwm signal after having being processed by the dead-time generator, the level shifter and the tapered buffer. Let us observe that due to the level shifting, it belongs to another voltage domain with respect to the pwm signal in order to effectively drive the high-side pMOS switch. Nonetheless, it is possible to notice that, if the high level is approximately 3.6 V as expected, the low level is instead a bit higher than expected: it is not 2.1 V, but it varies around 2.25 V. This is a consequence of the disturbances in the internal supply voltages produced by the internal generator, as already discussed in the previous section. In fact, the high-side rail at the output of this block has actually the task of setting the low level of the driving signal for the high-side power switch.

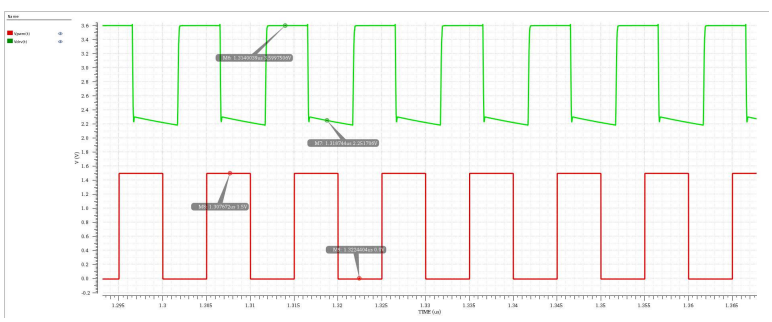


Figure 3.11: Signals Throughout the Driving Chain

Internal Supplies

Fig. 3.12 shows the voltage associated with the high-side rail at the output of the internal voltage generator. As previously discussed, this voltage is ideally supposed to be constant to 2.1 V or, more precisely, 1.5 V under the supply level which in the target applications is set at 3.6 V. Nevertheless, we can observe that the simulation highlights a mismatch between the ideal specification and the actual shape of the internal supply signal. In particular, the real signal varies in a range between 1.85 V and 2.3 V. More specifically, we notice that the signal stays around the upper bound of this range approximately for half

of the switching period, and around the lower bound for the other half. There are mainly two potential problems associated with this behavior. When the signal level is superior than the target of 2.1 V, it happens that the amplitude of the driving signal of the high-side power switched is reduced. This may slow down the turning-on phase, and consequently, increase the switching losses with a potential deterioration of the efficiency. On the other hand, having an internal supply at a level that is inferior to the target of 2.1 V results in an increase of the amplitude of the driving signal at some points of the driving chain, leading to voltage stresses in the transistors of the buffer which exceed those nominally tolerable. In other words, a not satisfying behavior in the internal supply generation might lead to problems inherent in both the efficiency and the reliability of the converter.

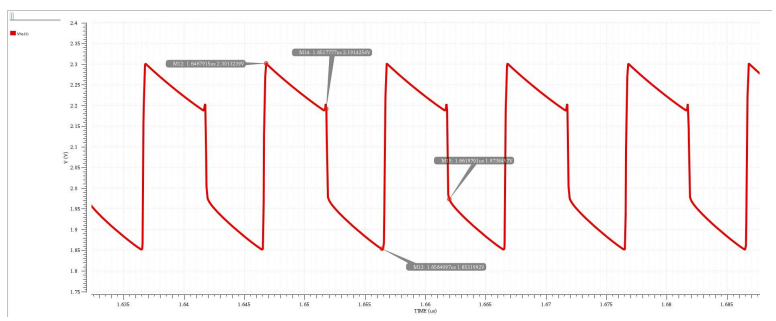


Figure 3.12: Original High-Side Internal Supply

3.4 Criticalities and Development Perspective

From the analysis of the converter and of his behavior, some important criticalities emerge. They represent the stimulus for the development work which is the core of this thesis.

There are two important aspects:

- Several violations of the Safety Operation Area (SOA) are reported, especially by transistors of the level shifters and of the buffers, which are forced to work under excessive voltage stresses for noticeable portions of the switching period;
- High values of capacitance are integrated in different parts of the circuit, mainly to mitigate undesired voltage perturbations.

Actually, no violations in Safety Operation Area of level shifters and buffers happen while simulating the power stage replacing the internal voltage generator circuit with an ideal one. This suggests, but it may even be easily accepted having a basic understanding of the system, that the source of these excessive voltage stresses is the generator of the internal supplies. Plus, as it is shown in

Fig. 3.13, an important portion of the integrated capacitance, namely 600 pF over ..., is allocated right in this circuit block with the intention, as mentioned, to mitigate the voltage surges associated to charge/discharge of the parasitic capacitances at the gate of the cascode MV transistors of the power switches, and at the internal nodes of the buffer, happening during the commutations.

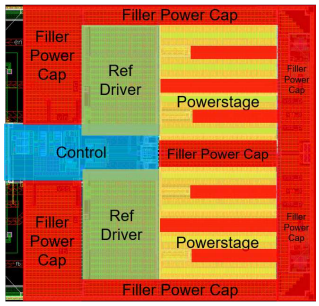


Figure 3.13: Test-Chip Area Occupation

More precisely, at every switching of the commutation cell, a charge Q is sunk or sourced in the internal supply. This charge flows through the output Internal Supplies Generator capacitor with capacitance C_{out} resulting in a voltage drop across it according to (3.1).

From (3.1), it is clear that the larger the capacitance value is, the smaller the voltage surge will be. This explains the need for a big capacitor in order to limit voltage perturbations and to have a robust approximately constant internal supply. For this reason, a big capacitance of 300 pF has been integrated in each of the sides of the internal generator. Nevertheless, being the power switch transistors large, a relevant amount of charge Q is sourced/sunk at every commutation, and the voltage surges observed are still substantial and sufficient to significantly reduce the efficiency and especially the reliability of the converter, as previously discussed.

This scenario strongly suggests to strive for improving the internal supply function by developing a new circuit solution that is more effective in managing the charge sourced and sunk by the driving buffers and by the power switches. Fig. 3.14 shows the current entering in the internal voltage generator through the high-side rail and the current crossing the capacitor, resulting in the undesired voltage drop. We can notice that the two waveforms are approximately coincident, that is, the task of managing the passage of charge is completely delegated to the capacitor; as a result, given a fixed value of capacitance C_{out}, the supply net will experiment the worse (largest) possible voltage drop.

The thesis work has then been oriented to find an alternative solution for the internal supply generator, featuring a more effective charge management

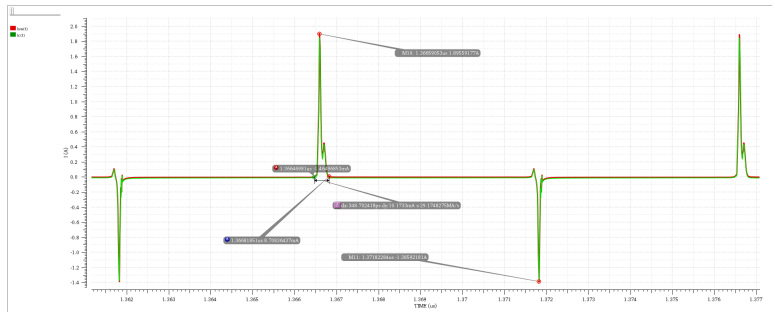


Figure 3.14: Load Impulsive Current

or, in other words, providing a lower impedance path for the sourced/sunk charge. As anticipated, the main goal of this project is reducing the voltage stresses in the driving chain, and at the same time significantly decreasing the amount of capacitance employed in the internal supply generation in order to reduce the area occupation. Since the energetic efficiency is a metric of primary importance for an integrated converter, it has been quantified and kept under control during the development activity. Notice that, in order to simplify the problem, the focus will be put on developing an alternative internal voltage generator for the high-side portion of the converter. Instead, an ideal internal supply of 1.5 V will be kept for the low-side. In further development stages an integrated solution to realize both the supplies may be pursued, implementing charge recycling principles to improve the efficiency, as well.

Chapter 4

Switching Transient Insight

In the last section of Chapter 3 the decision to re-design the *Internal Supply Generator* (ISG) has been taken in order to overcome some criticalities in the power stage, such as excessive voltage stresses in the high-side driving chain and very important area occupation due to the large integrated capacitance value. The problem that has been pointed out about this circuit block is that, despite the usage of such a high value output capacitance, the voltage actually imposed at the output rail, $v_{HS}(t)$, is not close to the target constant of 2.1 V, but still experiments large variations due to a not ideal rejection of the disturbances introduced by its load. In particular, the load of the Internal (high-side) Supply generator is represented by the well-known tapered buffer and, especially, by the innovative cascode high-side power switch of the commutation cell. Let us notice that the undesired voltage variations in the output rail of the ISG occur as a consequence of some current peaks injected and absorbed by the load contextually to the commutations of the power switches. These peaks can be observed through the simulation and are shown in Fig.3.14.

In order to develop a better understanding of the load to manage, Chapter 4 is dedicated to the analysis of the commutation transients of the power switches. Firstly the simpler and classic case where the high-side power switch is implemented by a single MOSFET will be treated, and then some considerations and observations, even based on simulations, will be carried out about the commutation transients of the cascode power switches.

4.1 Classic Switching Transients Analysis

The basic switching cell that can be extracted by a buck converter topology is shown in Fig. 4.1(a), where the secondary switch is implemented by a diode. Neglecting the inductor current ripple for simplicity, the inductor in the switching cell can be substituted by a current generator, as illustrated in Fig. 4.1(b).

Current I_o and voltage V_{in} represent simply the average inductor current and the input voltage of the converter respectively. Let us notice that in Fig.

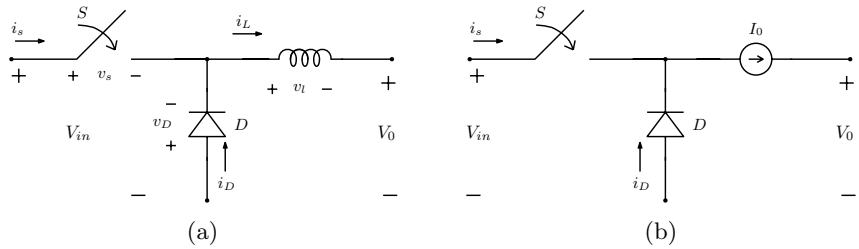


Figure 4.1: Buck Converter Switching Cell: (a) Inductive Load and (b) Simplified Version

4.1(b) the voltage V_o at the output port appears in series with an ideal current generator. Hence, its value is irrelevant for the operation of both the switch and the diode. For this reason, in this analysis such an output voltage can be arbitrarily set to zero for simplicity, and the simple equivalent model shown in Fig. 4.2 can be used to analyze the device switching process.

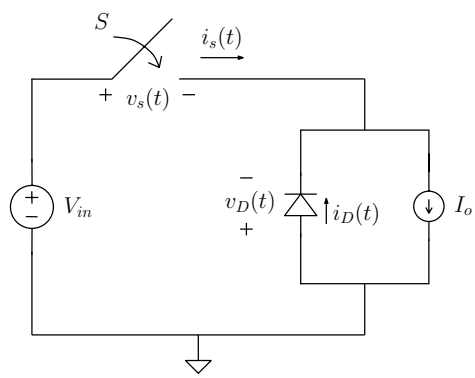


Figure 4.2: Simplified Model for Switching Analysis

In particular, the main goal of the analysis proposed in this section is describing the switching transients and highlighting the parameters that affect the interval times t_{ri}, t_{fv}, t_{rv} and t_{fi} shown in Fig. 2.12. Besides the obvious dependence on device model, the major contribution comes from the driver circuit, which has been included in Fig. 4.3, that has the task of charge and discharge the MOSFET's input capacitance in a very short time (a few hundreds of picoseconds in the target applications of the converter presented in Chapter 3).

As already discussed in section 3.2, the output stage of the driving circuit is an inverter that includes a pull-up pMOSFET, connecting the switch's gate to the external power supply V_{in} through an equivalent resistor R_1, and a pull-down nMOSFET, connecting the switch's gate to the voltage level $V_{in} - |V_{DRV}|$ through an equivalent resistor R_2. This output inverter is driven by a control signal $v_{ctrl}(t)$ derived from the PWM signal. Thus, the driving signal can be

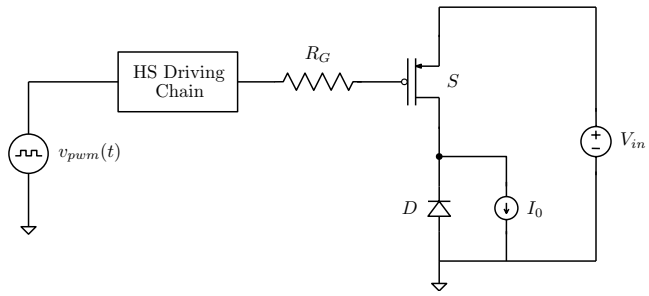


Figure 4.3: Scheme for Switching Analysis Including the Driving Circuit

represented through an equivalent source as sketched in Fig. 4.4 where $R_{on} = R_1 + R_G$ and $R_{off} = R_2 + R_G$.

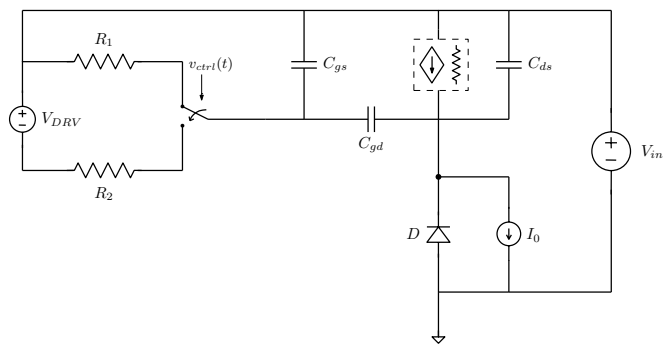


Figure 4.4: Switching Scheme with an Equivalent Representation of the Driving Circuit

Moreover in Fig. 4.4 the MOSFET is replaced by a simplified equivalent model that highlights the three capacitances C_{gs}, C_{gd} and C_{ds}, and that models the channel behavior as a control current generator or a simple resistor $R_{DS,on}$ dependently if the transistor is working in active or in linear zone respectively. Notice that typically datasheets refer MOSFET parasitic capacitance values of C_{iss}, C_{rss} and C_{oss}, defined as follow:

- $C_{iss} \triangleq C_{gs} + C_{gd}$;
- $C_{rss} \triangleq C_{gd}$;
- $C_{oss} \triangleq C_{ds} + C_{gd}$.

In general, MOSFET's capacitances are nonlinear with respect to the applied voltages, and they experiment quite abrupt variation when v_{DS} is close to zero. This suggests the idea of easily model this non-linearity by adopting a piece wise-constant approximation: for each capacitance, two different values will be

considering depending on the MOSFET status being ON or OFF. To discern the two possible values a single or a double quotation mark will be used respectively. Furthermore, in the following analysis the diode will be considered ideal.

4.1.1 Turn-on Transient

The turn-on transient consists in a sequence of five phases, each characterized by a specific topological state:

PHASE 1: interval $0 \leq t \leq t_1$

At the beginning of the turn-on phase the MOSFET is OFF and the current I_o is completely conducted by the diode D. The equivalent circuit is sketched in Fig. 4.5.

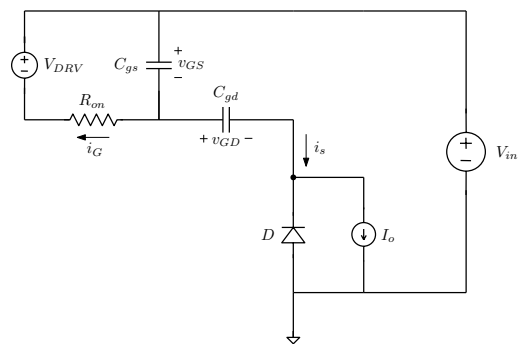


Figure 4.5: Turn-on Transient, Equivalent Circuit, Phase 1

Since the ideal diode is conducting, the voltage across it is zero, and the $|v_{DS}|$ voltage is clamped at V_{in}. Thus, the C_{ds} capacitive current is null. For this reason, the gate current i_G is divided between the other two capacitances C_{gs} and C_{gd} as they were connected in parallel, and its total values is given by:

$$i_G = C''_{gs}\frac{d|v_{GS}|}{dt} + C''_{gd}\frac{d(|v_{GS}| - V_{in})}{dt} = (C''_{gs} + C''_{gd})\frac{d|v_{GS}|}{dt} = C''_{iss}\frac{d|v_{GS}|}{dt} \quad (4.1)$$

where, as mentioned, the double quotation mark represents the values of capacitances with the MOSFET in OFF state. Therefore, the input MOSFET capacitance is simply charging through the resistor R_{on}, according to:

$$\begin{cases} |v_{GS}(t)| = V_{DRV}(1 - e^{-\frac{t}{\tau''}}) \\ i_G(t) = \frac{V_{DRV}}{R_{on}} e^{-\frac{t}{\tau''}} \end{cases} \quad (4.2)$$

being $\tau'' \triangleq R_{on}C''_{iss}$.

This phase ends when $|v_{GS}(t)|$ reaches the absolute value of the threshold volatage $|V_{th}|$. Let us call "t_1" this time instant:

$$t_1 = \tau'' \ln \frac{V_{DRV}}{V_{DRV} - |V_{th}|}. \quad (4.3)$$

PHASE 2: interval $t_1 \leq t \leq t_2$

When v_{GS} reaches the threshold voltage, the MOSFET turns on and starts to conduct the current i_{SD}. Since the ideal diode is still conducting current, v_{SD} is still clamped at V_{in}. Hence, the MOSFET turns on in *saturation region* and channel current i_{SD} follows a quadratic law. Fig. 4.6 shows an equivalent circuit describing this topological state.

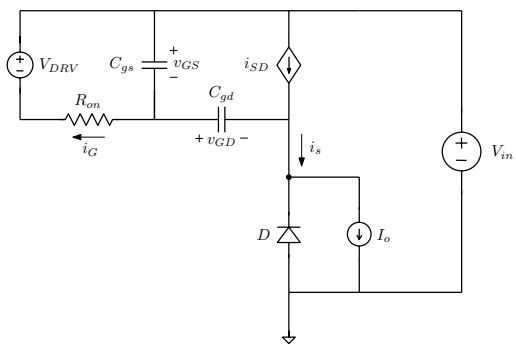


Figure 4.6: Turn-on Transient, Equivalent Circuit, Phase 2

The source-to-gate voltage goes on increasing according to (4.2), causing the source current to increase until i_S becomes equal to I_o, with the consequent turning off of the diode. This event characterizes the instant t_2:

$$i_S(t_2) = i_{SD}(t_2) - i_{dg}(t_2) = I_o. \tag{4.4}$$

From which, by selecting a model for the controlled current generator, it would be possible to derive an expression for t_2.

PHASE 3: interval $t_2 \leq t \leq t_3$

At the instant t_2 the diode turns off, and the v_{SD} voltage is no more clamped at V_{in}. Hence, the difference $i_{SD}(t) - I_o$ has to be delivered by the drain-to-source capacitance, which starts to be progressively discharged. Furthermore, since $i_{SD}(t) - I_o$ is increasing in time, the rate C_{ds} is getting discharged increases as well. This leads to an increase of $i_{dg}(t)$ in the face of a decrease of $|i_G(t)|$. At the instant t_3 these two currents become equal and their difference, $i_{gs}(t)$, zeros:

$$I_{G,pl} \triangleq i_G(t_3) = \frac{V_{DRV} - |V_{GS,pl}|}{R_{on}} = -C''_{gd}\frac{dv_{GD}}{dt} = C''_{gd}\frac{dv_{DS}}{dt} = constant. \tag{4.5}$$

The drain current is also constant:

$$I_{SD,pl} \triangleq i_{SD}(t_3) = I_o + I_{G_pl} - C''_{ds}\frac{dv_{SD}}{dt}. \tag{4.6}$$

Fig. 4.7 shows the equivalent circuit representing the described situation in this phase.

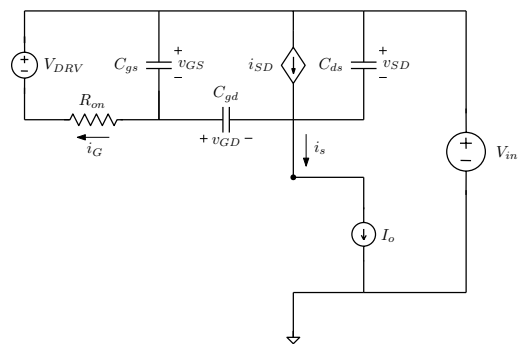


Figure 4.7: Turn-on Transient, Equivalent Circuit, Phase 3

PHASE 4: interval $t_3 \leq t \leq t_4$

The phase beginning in the t_3 instant is called *plateau* region, and it is characterized by null gate-to-source capacitive current, and as a consequence, by a constant $|V_{GS}|$. Fig. 4.8 sketches the equivalent circuit in this phase. The current discharging the drain-to-source capacitance:

$$i_{Cds} = C''_{ds} \frac{dv_{SD}}{dt}$$

is constant, and so the V_{SD} drops at a constant rate given by:

$$\frac{dv_{SD}}{dt} = -\frac{I_{G,pl}}{C''_{gd}} = \frac{V_{DRV} - |V_{GS,pl}|}{R_{on} C''_{gd}}. \tag{4.7}$$

In particular, (4.7) highlights the way the turn-on transient is dependent on the driver parameters: the R_{on} value has a clear role in determining the turn-on transient duration and the associated losses. When $|v_{DS}|$ reaches low levels and approaches $|V_{GS,pl}|$, C_{gd} starts increasing quite rapidly, and v_{SD} slopes decreases. Furthermore, the MOSFET exits saturation, entering its linear region in instant t_4.

PHASE 5: interval $t \geq t_4$

Once the MOSFET entered in the linear region its channel behavior can be modeled by an equivalent resistor $R_{DS,on}$, as shown in Fig. 4.9. The v_{SD} voltage is established at the value:

$$V_{SD,on} = R_{DS,on} \cdot I_o, \tag{4.8}$$

and the $|v_{GS}|$ voltage restarts to increase exponentially, virtually asymptotically approaching V_{DRV}:

$$|v_{GS}(t)| = |V_{GS,pl}| + (V_{DRV} - |V_{GS,pl}|)(1 - e^{-\frac{t-t_4}{\tau'}}), \tag{4.9}$$

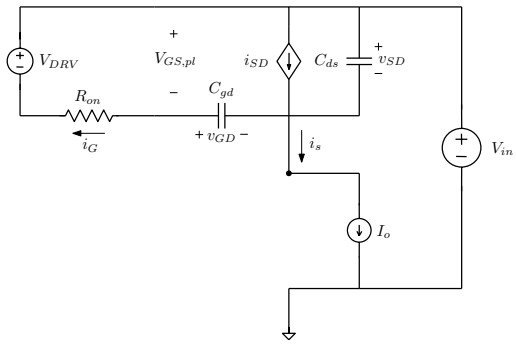


Figure 4.8: Turn-on Transient, Equivalent Circuit, Phase 4

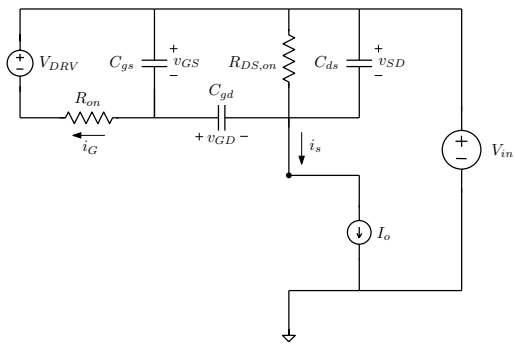


Figure 4.9: Turn-on Transient, Equivalent Circuit, Phase 5

Being τ' the time constant $\tau' \triangleq R_{on}C'_{iss}$, now higher than τ''.

The main turn-on transient waveforms are sketched in Fig. 4.10.

4.1.2 Turn-off Transient

In this section a description of the turn-off transient will be provided. In general terms the turn-off transient is similar to the turn-on one, with a reversed order of the topological states. Notice that now even the considered gate current i_G has been reversed, so that it still can be considered positive for the sake of a simpler explanation.

PHASE 1: interval $0 \leq t \leq t_1$

The turn-off transient starts when the pull-up transistor of the output stage of the driver connects the gate of the MOSFET to the external supply. Fig. 4.11 shows the equivalent circuit in this phase.

At the beginning of the process the MOSFET input capacitance is exponen-

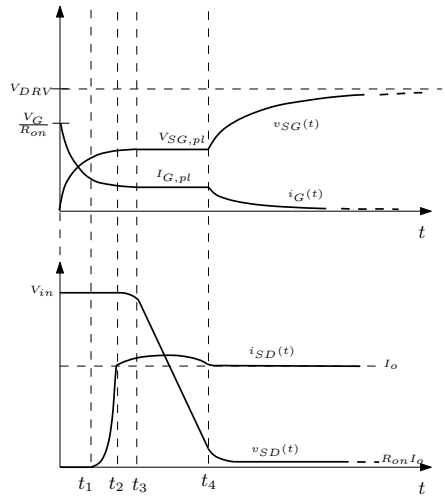


Figure 4.10: Turn-on Transient: Main Waveforms

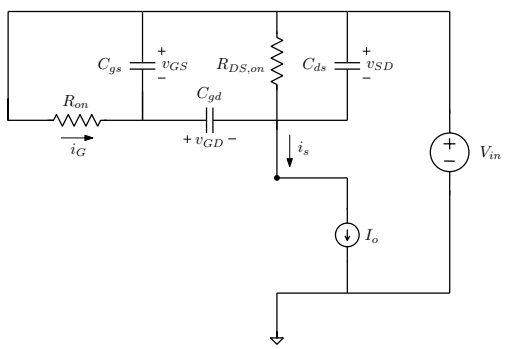


Figure 4.11: Turn-off Transient, Equivalent Circuit, Phase 1

tially discharged:

$$|v_{GS}(t)| = V_{DRV} e^{-\frac{t}{\tau'}}, \tag{4.10}$$

where τ' is now referred to the turn-off transient: $\tau' \triangleq R_{off} C'_{iss}$. The gate current follows the some trend, being:

$$i_G(t) = \frac{|v_{GS}(t)|}{R_{off}}. \tag{4.11}$$

Notice that during this interval the channel current i_{SD} is lower than I_o, since:

$$I_o = i_{SD} + i_{gd} = i_{SD} + \frac{C'_{gd}}{C'_{gs} + C'_{gd}} i_G. \tag{4.12}$$

The discharge process goes on until, at instant t_1, the MOSFET enters in saturation region when $v_{SD}(t_1) = |V_{GS}(t_1)| - |V_{th}|$.

PHASE 2: interval $t_1 \leq t \leq t_2$

Once the MOSFET is in saturation region, the channel behavior can be modeled with a controlled current source as shown in Fig. 4.12, and a further reduction of $|v_{GS}|$ translates into a decrease of both i_G and i_{SD}. Hence, the residual current $I_o - i_{SD} - \frac{C'_{gd}}{C'_{gs}+C'_{gd}} i_G$ starts charging the drain-to-source capacitance C_{ds}. As a consequence, the rate of change of v_{GD} increases, and $i_{gd}(t)$ increases as well, while $i_G(t)$ is decreasing according to (4.11). At time instant t_2 these two currents become equal and their difference, $i_{gs}(t)$, zeros, leading to the beginning of a *plateau* region.

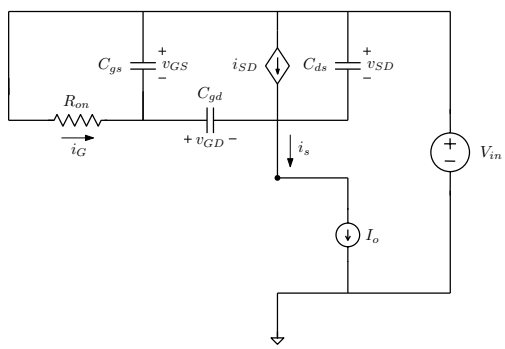


Figure 4.12: Turn-off Transient, Equivalent Circuit, Phase 2

PHASE 3: interval $t_2 \leq t \leq t_3$

As mentioned, when $i_{gs}(t)$ zeros in $t = t_2$ the source-to gate voltage remains constant at the value $|V_{GS,pl}| \triangleq |v_{GS}(t_2)|$, and the correspondent topological situation is represented in Fig. 4.13. The following equation hold:

$$I_{G,pl} \triangleq i_G(t_2) = \frac{V_{DRV} - |V_{GS,pl}|}{R_{off}} = C'_{gd}\frac{dv_{GD}}{dt} = C'_{gd}\frac{dv_{SD}}{dt} = constant. \quad (4.13)$$

Notice that, assuming capacitances' values constant, the v_{SD} rise is characterized by a linear behavior, whose slop is given by (4.13):

$$\frac{dv_{SD}}{dt} = \frac{I_{G,pl}}{C'_{gd}} = \frac{V_{DRV} - |V_{GS,pl}|}{R_{off}C'_{gd}}. \quad (4.14)$$

The channel current is also constant and equal to:

$$I_{SD,pl} \triangleq i_{SD}(t_2) = I_o - I_{G,pl} - C'_{ds}\frac{dv_{SD}}{dt}. \quad (4.15)$$

This phase ends when the value of v_{SD} reaches V_{in} in $t = t_3$, turning on the ideal diode D.

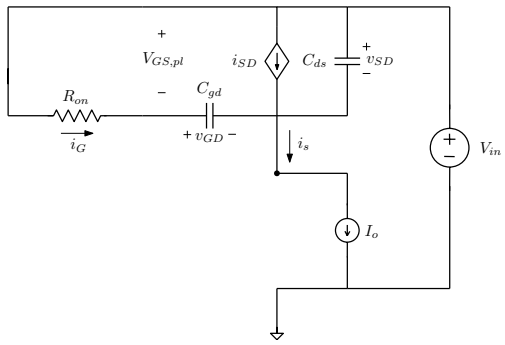


Figure 4.13: Turn-off Transient, Equivalent Circuit, Phase 3

PHASE 4: interval $t_3 \leq t \leq t_4$

Since the diode starts conducting, in this phase the v_{SD} is clamped at V_{in}, and C_{gs} experiments a further exponential discharge:

$$|v_{GS}(t)| = |V_{GS,pl}|e^{-\frac{t-t_3}{\tau''}}. \tag{4.16}$$

As a consequence, being the MOSFET in active zone, the channel current decreases until it zeros when $v_{GS}(t)$ reaches V_{th} in $t = t_4$. From (4.16), the duration of this phase is given by:

$$t_4 - t_3 = \tau'' ln \frac{V_{GS,pl}}{V_{th}}. \tag{4.17}$$

The equivalent topology characterizing this interval is shown in Fig. 4.14.

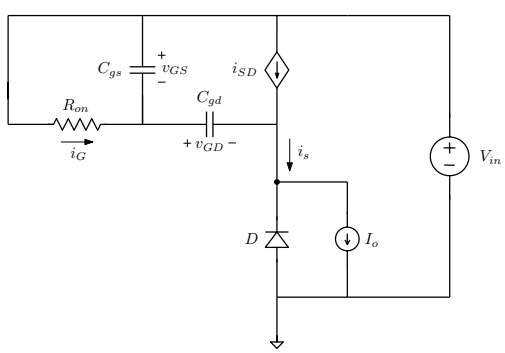


Figure 4.14: Turn-off Transient, Equivalent Circuit, Phase 4

PHASE 5: interval $t \geq t_4$

After the MOSFET turns-off, the gate-to-source absolute value voltage tends virtually and asymptotically to V_{DRV} according to (4.16). The equivalent circuit is sketched in Fig. 4.15.

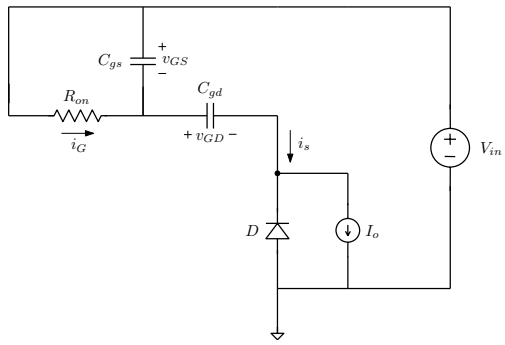


Figure 4.15: Turn-off Transient, Equivalent Circuit, Phase 5

The main waveforms relative to the turn-off transient are shown in Fig. 4.16.

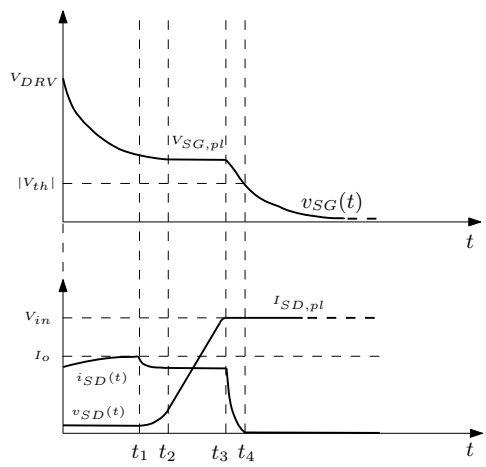


Figure 4.16: Turn-off Transient: Main Waveforms

4.2 Cascode Configuration Switching Transients

The aim of this section is to provide a qualitative interpretation of the switching transients of the cascode power switches shown in Fig. 3.2(d), which have been employed in the commutation cell of the high-frequency converter described in Chapter 3. In fact, an analysis similar to the one carried out in the previous section about the classic switch configuration would be much more complicated in that the system to analyze is now more complex and the sequence of the topological states is much more dependent on the operation conditions and on the models' parameters.

In order to carry out carry out some considerations about the switching transients of the high-side cascode-configuration switch, a conceptual scheme is sketched in Fig. 4.17.

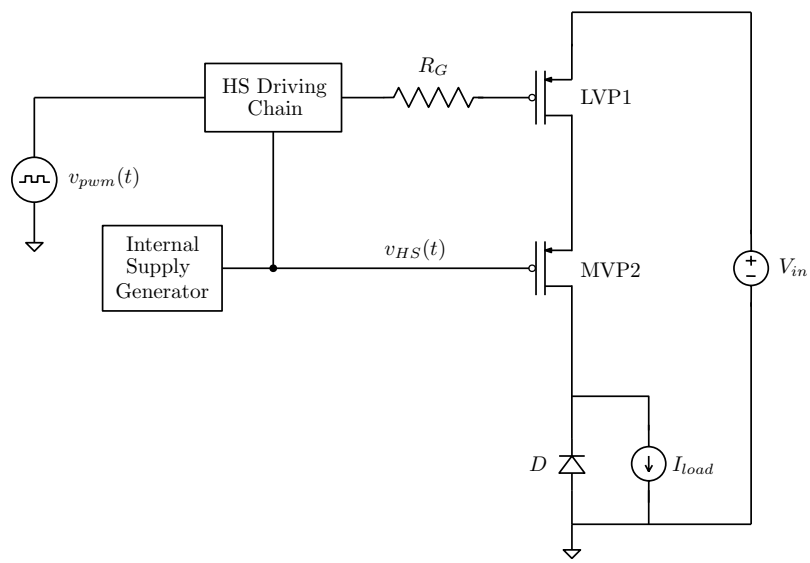


Figure 4.17: Scheme for Cascode Configuration's Switching Transients Simulation

4.2.1 Turn-on Transient

Qualitatively, the turn-on transient can be described by the sequence of the following events:

- When the driving signal experiments a falling edge and assumes its low level ($= V_{in} - V_{DRV}$), the charge process of the gate capacitance of the MOSFET LVP1 in Fig. 3.2 starts, as shown in Fig. 4.18.

- When the gate-to-source voltage of LVP1 reaches the threshold voltage, it enters in saturation region and starts sinking current through its channel. The primary effect of such a current is that it starts charging the source-to-gate capacitance of the cascoded device MVP2. Fig.4.19 shows the charging of the source-to-gate capacitance of MVP2 as a consequence of the charging of the source-to-gate capacitance of MVP1.

  Let us notice that the current charging the source-to-gate capacitance of MVP2 is injected through the gate of MVP2 in the internal supply net, which is the output rail of the *Internal Supply Generator* that will be redesigned in Chapter 5 and Chapter 6. In other words, the charge process of the source-to-gate capacitance of MVP2 is a phenomenon, together with

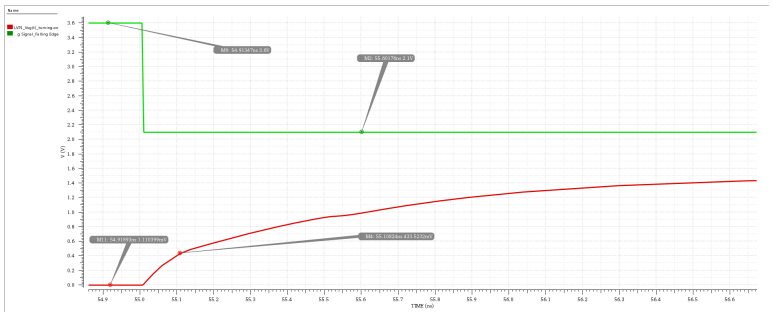


Figure 4.18: Trigger of the Turn-on Transient

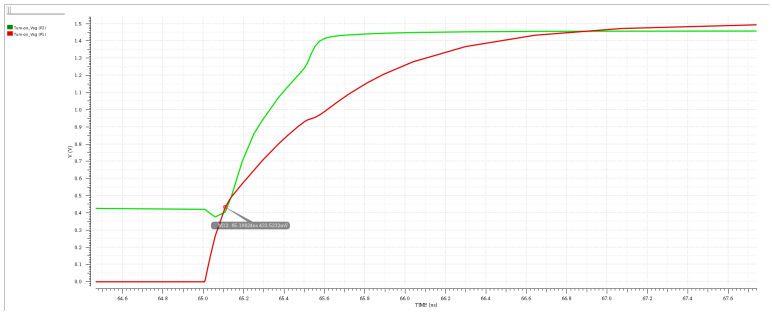


Figure 4.19: Source-to-Gate Capacitances' Charging

the discharge of the intermediate nodes of the tapered buffer, responsible for the injected current peaks that disturb the internal supply, shown in Fig. 4.20.

- Once the MVP2 device enters in saturation as well, the current through the cascode switch grows until it reaches the load current level I_{load}. Then, a further increasing in the switch current produces a discharge of the source-to-drain capacitances of LVP1 and of MVP1, and the consequent drop of $v_{SD,P1}$ and of $v_{SD,P2}$. Such a drop can be observed in Fig. 4.21.

  Notice that, contextually to the discharge of the source-to-drain capacitances there is even the discharge of the gate-to-drain capacitance of MVP2. This phenomenon is responsible for the second and highest peak of the current injected in the internal supply through the gate of MVP2, as shown in Fig. 4.20;

- This drop ends when the two MOSFETs enter in linear region conducting a current equal to I_{load}. The switch-on transient is extinguished and the drop across the channels is:

$$V_{SD,on} = R_{DS,on} \cdot I_{load} \tag{4.18}$$

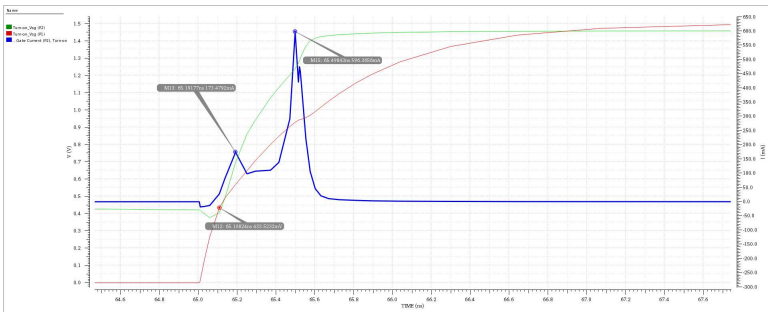


Figure 4.20: Injected Gate Current

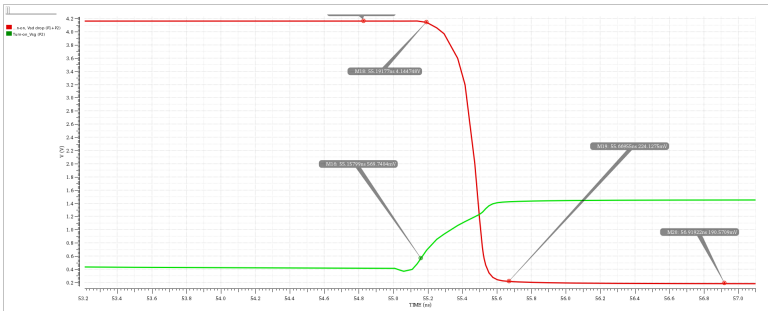


Figure 4.21: Switch Voltage Drop

Fig. 4.22 shows the current through the switch and the source-to-drain voltage of LVP1 after the turn-on transient is extinguished. Notice that the current is actually very close to the load current, which in the simulated system had been set at 1 A.

Fig. 4.23 represents the evolution of the source-to-gate voltage of LVP1 throughout the turn-on transient for several values of the output resistance of the driver. As a final observation, notice that higher values of such resistance produce a slow-down of the transient and a consequent increase of the associated losses. Notice even that, if the transient is sufficiently slow, it is still possible to well observe a *plateau* region, which represents the core of the turn-on transient.

4.2.2 Turn-off Transient

Here a sequence of steps that qualitatively describe the switch-off transient of the high-side cascode switch will be listed:

- When the driving signal experiments a rising edge and assumes its high level, which corresponds to the external supply V_{in}, the discharge exponential process of the gate capacitance of the MOSFET LVP1 in Fig. 3.2 starts, A shown in Fig. 4.24.

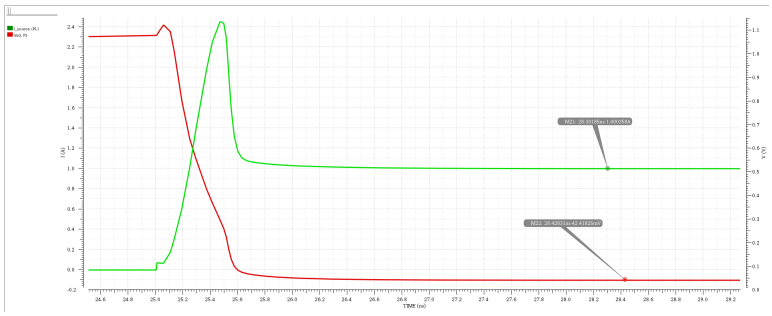


Figure 4.22: Switch's ON-Current and Voltage Drop

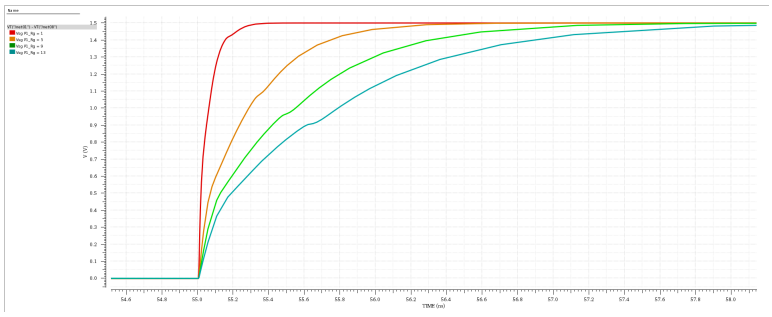


Figure 4.23: Impact of the Driver Resistor in the Turn-on Transient

- This discharge process goes on until the LVP1 exits the linear region and enters the saturation one. At this point, its channel current becomes dependent on the ongoing reduction of the source-to-gate voltage, and it starts decreasing as a consequence;

- The current difference I_{load}–$i_{SD,P1}$ has now to be provided especially through the gate-to-source capacitance of MVP2, causing reduction of the source-to-gate voltage of MVP2, as shown in Fig. 4.25. In such a way, the reduction of the source-to-gate voltage of MVP1 has been propagated to MVP2.

  Notice that the current through the gate-to-source capacitance in this phase is absorbed by the internal supply through the gate of MVP2. In other words, a contribution to the absorbed current peaks disturbing the internal supply comes from this phenomenon associated with the turn-off transient of the high-side cascode switch. Fig. 4.26 shows the current absorbed by the gate of MVP2 during the turn-off transient. Notice that such a current origins from the charge process of the gate-to-source capacitance of MVP2;

- At this point even MVP2 enters in saturation, and a further reduction of the source-to-gate voltages translates into a gradual reduction of the

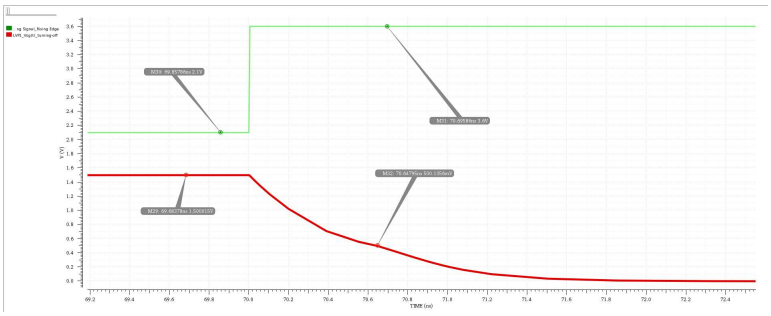


Figure 4.24: Trigger of the Turn-off Transient

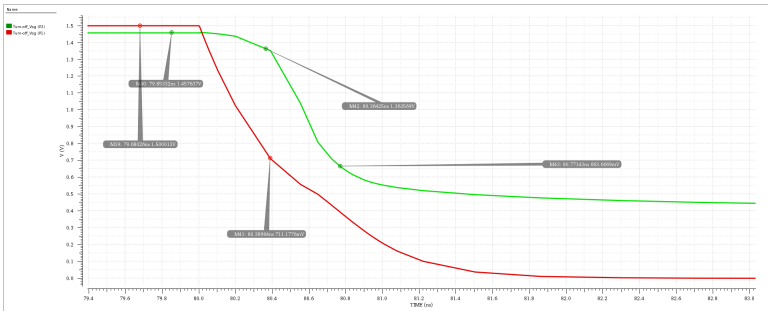


Figure 4.25: Source-to-Gate Capacitances' Discharging

switch current. Nevertheless, the diode is still inversely biased, and so it cannot conduct current. Thus, the current difference $I_{load} - I_S$ is provided by the source-to-drain capacitances of LVP1 and of MVP2 and by the gate-to-drain capacitance of MVP2. This process leads to a progressive increase of the voltage drop across the switch, which goes on until this voltage drop almost reaches V_{in}. Notice that the current through the gate-to-drain capacitance of MVP2 in this phase represents the second and last contribution to the current peaks absorbed through the gate of MVP2 and disturbing the internal supply rail.

Fig. 4.27 shows the rise up to about V_{in} of the voltage across the switch as a consequent of the switching-off of MVP2.

- Now the diode is no more inversely biased, so it starts conducting the load current. In the meanwhile, the switch current decreases until it zeros when the source-to-gate voltages of the two cascoded MOSFETs go down under their threshold voltages;

- As the last step, the source-to-gate voltage of LVP1 goes on exponentially decreasing until it approaches zero, and the turn-off transient is finally extinguished.

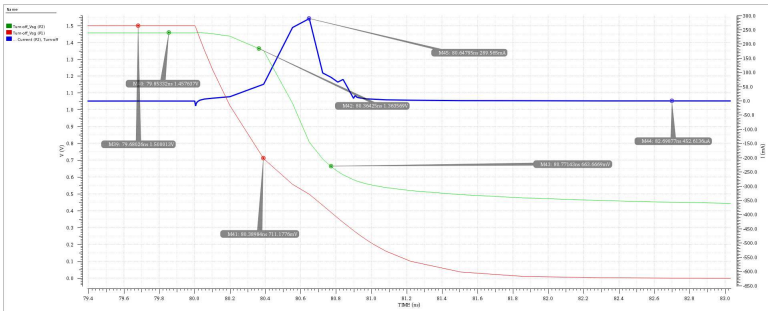


Figure 4.26: Absorbed Gate Current

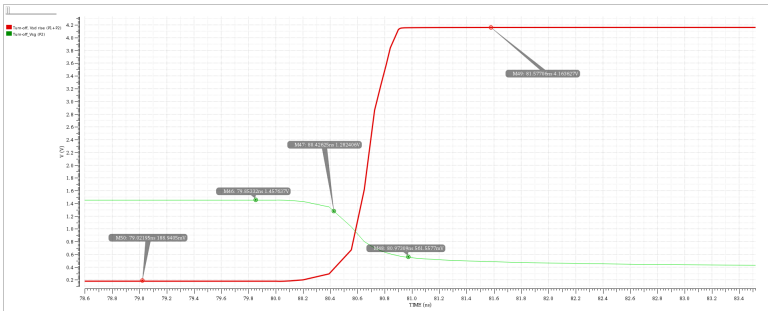


Figure 4.27: Source-to-Drain Voltage Rise at the End of the Turn-off Transient

As a final consideration let us point out that the main interactions between the *Internal Supply Generator* and the *Commutation Cell* consist in some very short and high-amplitude current peaks injected and absorbed by the commutation cell in the internal supply rail. Such peaks correspond respectively to the charge and discharge processes of the parasitic gate-to-source and gate-to-drain capacitances of the cascaded device MVP2. In addition, other contributions to the injected peaks of current in the internal supply rail are given by the charge of the gate capacitance of LVP1 and by the discharge of the intermediate nodes of the tapered buffer in the driving chain. Notice that all this phenomena happen contextually to the switching transients.

Chapter 5

Internal Supply Generator Design

5.1 Introduction

The problem of generating internal supplies in order to shape the driving signals and to bias the cascode transistors of the commutation cell has been introduced in Chapter 3. The original circuit integrated in the converter to realize this function, showed in Fig. 3.6, has been described as well. As previously discussed, the purpose of this block is to provide rails at a voltage which is approximately constant to a fixed level, and as robust as possible with respect to the perturbations introduced by the load (which is here represented by the drivers and the commutation cell). In particular, in the following treatment, the problem of generating and regulating the internal supply for the high-side driving chain will be considered while, in the global testbench simulations, the low-side internal supply will be set by an ideal generator. The high-side internal supply has to be set at a voltage level which is 1.5 V lower with respect to the external supply in order to get the most effective driving signal without over-stressing the LV transistors of the driving chain and of the power switch. Since for the target applications the external supply is given at the level $V_{in} = 3.6\ V$, assuming it to be constant, the internal supply will have to be generated and regulated at the target value of $V_{HS} = 2.1\ V$.

Other than improving the precision of the regulation, another key aspect that will be considered in the design of the new circuit solution is the area occupation. The dominant contribution in the footprint of the original voltage generator is given by the 300 pF capacitor integrated in it. For this reason, the value of the capacitance used will be adopted as a representative indicator of the overall area occupation, and efforts will be put in order to significantly reduce this capacitance value. To do that, the new solution should provide alternative paths to manage the sourced/sunk output current peaks in order to decrease the output impedance seen by the load.

In the development process several ideas have been considered. Many of these had some intrinsic limitations based or on an incomplete understanding of the converter environment, or on the incompatibility with the operation conditions, or they were simply too complicated to implement, without granting a sufficiently accurate behavior. On the other hand, each one of them had the merit to underline some important aspects of the problem, leading to a better understanding of the system. The outcome of the selection process is the final solution which is going to be presented in the following sections. In particular, it is obtained by combining three stages that are going to be progressively introduced and described:

- The **Common Drain** (CD) **stage**: it is basically used to impose the dc point of the voltage in the high-side output rail of the internal supply generator;

- The **Open Loop** (OL) **stage**: it represents the core of the regulation function. It has the task to aid the output capacitor to effectively manage the impulsive current introduced by the load, providing an alternative low-impedance path;

- The **Common Source** (CS) **stage**: its primary task is to stabilize the behavior of the internal regulator whenever a not optimal synchrony between the load and the OL stage occurs.

Notice that in the context of this chapter, some blocks such as error amplifiers and driving signal generators are represented and modeled by means of ideal components. This is true even for the simulation results that will be shown. This approach allows to separate different problems by the introduction of a hierarchy, and leads to simplifications in the design process. In particular, the realization of a chain to drive the OL stage, and to make its operating synchronized with the load will be carried out in Chapter 6.

5.2 Common-Drain Stage

The Common-Drain stage, inserted in a testbench designed to assess its correct functioning, is illustrated in Fig. 5.1. The figure shows that this circuit is obtained by connecting in cascade two different sub-stages: the "Biasing Stage" with the fundamental task of imposing the target dc point at the output rail of the internal supply generator, and the "Common-Drain (CD) Push-Pull Output Stage" that gives the name to this block.

5.2.1 Sizing and General Considerations

The biasing stage operation is very simple. It is sufficient to size the transistors M_1, M_2, M_3 and M_4, and to correctly select the input V_{bias1} and V_{bias2} in order

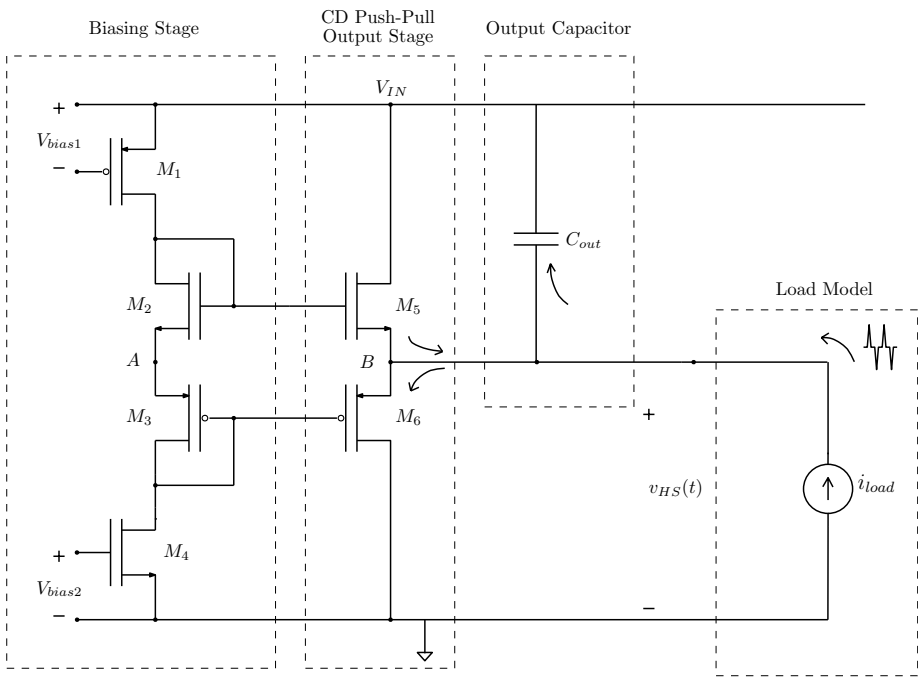


Figure 5.1: CD Generator Testbench

to bias the structure in such a way to have the desired dc output voltage at node A. Specifically, we want:

$$V_A = V_{in} – 1.5\ V = 3.6\ V – 1.5\ V = 2.1\ V$$

Now, let us face the issue to size the transistors M_1 and M_2 in order to have $V_B = V_A$ by carrying out the following analysis:

From KVL,

$$V_{GS,2} + V_{SG,3} = V_{GS,5} + V_{SG,6} \tag{5.1}$$

Ignoring the body effect, $V_{GS,2} + V_{SG,3}$ is constant if the bias current from M_3 is constant. Under these condition, increasing $V_{GS,5}$ decreases V_{SG_6} and vice versa.

For simplicity, assume at first that a short circuit is connected from the drain of M_2 to the drain of M_3. Then $V_{GS,2} + V_{SG,3} = 0$ and $V_{GS,5} = V_{SG_6}$ from (5.1). For M_5 to conduct nonzero drain current, $V_{gs,5} > V_{t,5}$ is required. Similarly, $V_{gs_6} < V_{t,6}$ is required for M_6 to conduct nonzero drain current. Since the adopted technology features enhanced-mode devices, $V_{t,5} > 0$ and $V_{t,6} < 0$. Therefore, M_5 and M_6 do not both conduct simultaneously under these conditions, which is characteristic of a Class B output stage[9].

In the situation represented in Fig. 5.1, however, $V_{GS,2}+V_{SG,3} > 0$ and both M_5 and M_6 are biased to conduct nonzero drain current when $v_{HS}(t) \equiv 2.1\ V$,

which is a characteristic of a class AB output stage. Recall that the basic theory for MOSFETs in saturation region states that, in first approximation:

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_t)^2 \tag{5.2}$$

Now, assuming $V_{t,5} = V_{t,2}$ and $V_{t,6} = V_{t,3}$, and observing that $I_{D,3} = -I_{D,2}$, using (5.2) in (5.1) gives:

$$\sqrt{\frac{2I_{D,2}}{k'_n(W/L)_2}} + \sqrt{\frac{2I_{D,2}}{k'_p(W/L)_3}} = \sqrt{\frac{2I_{D,5}}{k'_n(W/L)_2}} + \sqrt{\frac{-2I_{D,6}}{k'_p(W/L)_3}} \tag{5.3}$$

If the load does not absorb current, then $I_{D,6} = -I_{D,5}$, and (5.3) can be rearranged to give:

$$I_{D,5} = I_{D,2}\frac{(\sqrt{\frac{1}{k'_n(W/L)_2}} + \sqrt{\frac{1}{k'_n(W/L)_1}})^2}{(\sqrt{\frac{1}{k'_n(W/L)_2}} + \sqrt{\frac{1}{k'_n(W/L)_2}})^2} \tag{5.4}$$

where $I_{D,5} = I_{d,5}$ when $v_{HS}(t) \equiv 2.1\ V$. The key point in this equation is that the quiescient current in the transistors of the Push-Pull Output Stage is well controlled with respect to the bias current that flows in the diode-conneted transistors of the Biasing Stage.

It has already been mentioned that by suitably choosing V_{bias1} and V_{bias2}, it is possible to set V_A at the desired voltage of 2.1 V. Nonetheless, 2.1 V is the desired voltage at the output of this circuit block, and not just at the intermediate node A. Thus, now a sizing principle useful to get $V_{HS} \equiv V_B = V_A = 2.1\ V$ will be illustrated.

From KVL,

$$V_{HS} \equiv V_B = V_A + V_{gs,2} - V_{gs,5}$$

Assuming $V_{t,2} = V_{t,5}$, this equation can be rewritten as

$$V_{hs} \equiv V_B = V_A + V_{ov,2} - V_{ov,5}$$

Therefore, when V_i is adjusted so that $V_A = 2.1\ V$, this structure forces $V_B = 2.1$ V as well, if $V_{ov,2} = V_{ov,5}$ Recalling that $V_{ov} \triangleq V_{gs} - V_t$, from (5.2) $V_{ov,2} = V_{ov,5}$ if

$$\frac{I_{D,5}}{(W/L)_5} = \frac{I_{D,2}}{(W/L)_2} \tag{5.5}$$

Substituting (5.4) in (5.5) and rearranging shows that $V_{ov,2} = V_{ov,5}$ if

$$\frac{(W/L)_5}{(W/L)_6} = \frac{(W/L)_2}{(W/L)_3} \tag{5.6}$$

Let us now illustrate the design choices and results for the CD stage employed in the Internal Supply Generator of the very high frequency buck converter. First of all, the following choices about the sizing of the transistors have been taken:

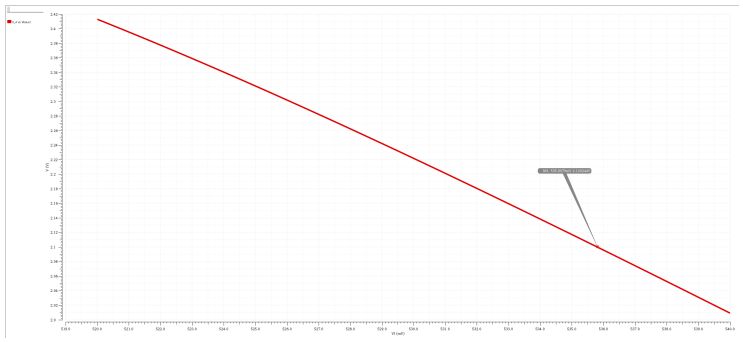
- $W_2 = 20\ \mu m$;
- $W_5 = 1.1\ mm$;
- $\frac{(W/L)_5}{(W/L)_6} = \frac{(W/L)_2}{(W/L)_3} = \frac{1}{3}$;

Then, V_{bias1} has been set to 600 mV and $V_{bias2} = 535.8\ mV$ has been selected in order to get $V_A = 2.1\ V$. To do this, a parametric dc simulation has been exploited, as shown in Fig. 5.2(a). Notice that now a situation in which the load showed in Fig. 5.1 is disactivated is being taken in consideration, that is, there is no current absorbed or sourced from the load. With the choices done, we have actually $V_A \approx 2.1\ V$ with a very good approximation. On the other hand, we have $V_B = 2.088\ V$. Notice that $V_B \approx V_A$ as it was expected from the theoretical analysis just carried out. Nevertheless, there still is a bit of difference between the two. This is related to the fact that, under the bias conditions in the circuit $V_{t,2}(= 727.1\ mV)$ is slightly different from $V_{t,5}(= 721.3\ mV)$, while in the analysis they were supposed to be exactly the same. More importantly, the (5.2), on which the analysis is based, represents a model with a particularly limited accuracy. In particular, the *channel length modulation* effect and the *short channel* effects have not been considered. Since we are interested in having a constant voltage of 2.1 V at the node B, it is possible to adjust the bias input voltage V_{bias2} at 535.2 mV as shown in Fig. 5.2(b). This allows to actually reach $V_B = 2.1\ V$.

About the sizing of the transistors, some interesting observations can be done:

- The length channel has been set at the minimum value allowed by the technology, which for these MV devices is $L = 400\ nm$. This choice is done in order to reduce the area occupation of the devices and, more importantly to minimize the channel resistance and the static consumptions;
- The widths W of the transistors of the Biasing Stage has been chosen relatively small. Again, this is done in order to limit the area occupation, and especially to limit the static current and, as a consequence, the static power consumptions. A different choice has been done for the transistors M_5 and M_6 of the Output Push-Pull Stage. In this case, much larger width values have been selected (but still much less with respect to those that implement the power switches of the commutation cell), mainly to reduce the overall impedance seen by the load when the current peaks occur. In fact, a larger W contributes in two ways to this sense: firstly, it is associated with higher parasitic capacitances (especially a higher gate-source capacitance, C_{gs}) which increase the overall capacitance value connected to the output node. Secondly, because a larger width corresponds to a lower channel resistance, it allows the passage of more charge when the load current peaks occur.

Now let us refer to the testbench represented in Fig. 5.1 when the load modeled by the current generator is activated. Fig. 5.3 represents the current



(a)

(b)

Figure 5.2: Parametric Analysis: (a) V_A vs V_{bias2} and (b) V_B vs V_{bias2}

conducted by the transistor M_6 (red waveform) when a positive peak of current is injected by the load compared with the current conducted by the branch made by R_{bias}, D_3 and D_4 of the original Internal Supply Generator showed in Fig. 3.6 in the same circumstance (green waveform).

Notice that the activation of the CD output stage is much higher, being able to conduct up to about 30 mA in correspondence to the peak, against the 13 mA of the previous solution. In this terms, the improvement of the performance is more than 200 %. Notice that the activation of the new circuit solution is higher even in the following half-period, contributing to recharge the output capacitor and to re-establish the desired 2.1 V at the output rail in a more effective way. Something analogous happens when a current peak is absorbed by the load.

Fig. 5.4 shows the trend of the voltage $v_{HS}(t)$ at the output rail of the Internal Supply Generator.

Again, the behaviour obtained by the CD-stage implementation (red waveform) is compared with the original one (green waveform). Notice that, despite the previous encouraging observations, there is not a substantial improvement: the generated waveform is still relatively far to be constant at the target of 2.1

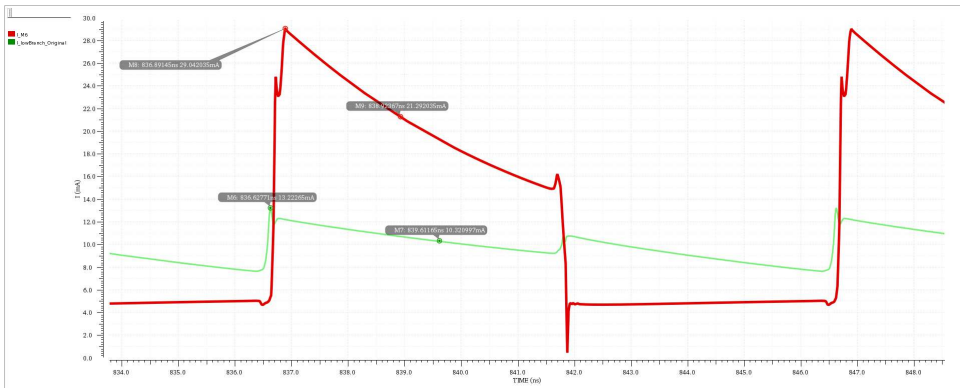


Figure 5.3: Original and CD-Stage Current Management: Comparison

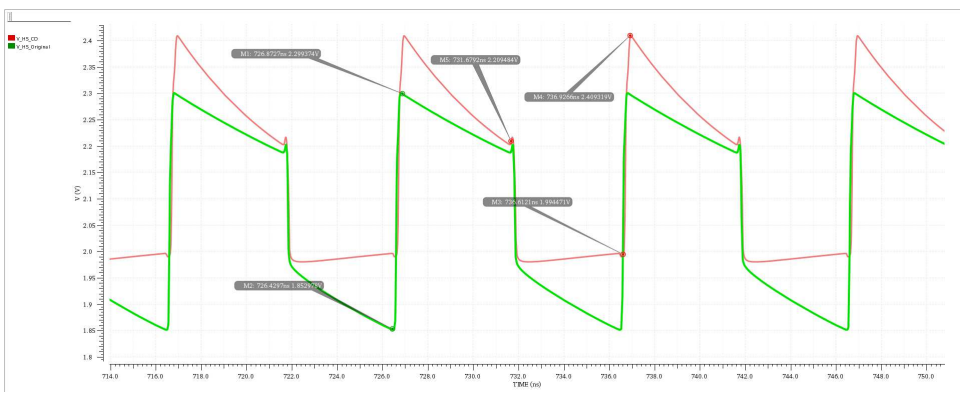


Figure 5.4: Output Voltage Comparison: CD Stage vs Original

V, and the deviations from it are similar in the two cases. This situation has two main reasons:

- When considering the amplitude of the load current peaks and the charge stored and taken from the output capacitor, the improvement actually reached are very poor, despite, as previously pointed out, the current management having a noticeably improvement in absolute terms. Fig. 5.5 shows the two currents shown in Fig. 5.3 compared to the peak of current inject by the load, and to the current managed by the output capacitor. Notice that, in both cases, the percentage of the current managed by the output capacitor approaches 100 %, and this translates in a similar output voltage perturbations. Nevertheless the small improvement in the current management can still be observed: when a positive current peak occurs the output voltage variation is about 450 mV in the original circuit, while it is about 415 mV with the CD realization. Notice even that, after the peak, the output voltage waveform goes back around 2.1 V quicker.

- The two compared generators work with a different principle. The one based on the CD-stage establishes the DC point of the output voltage, and then try to mitigate the deviations from it by an effective managing the current perturbations introduced by the load. This principle is in general adopted and developed throughout this thesis. On the other hand, the original generators establishes a dynamic equilibrium around the target 2.1 V. In other words, the target output is centered at the middle of the charging and discharging process od the output capacitor. In such a way, the actual deviation from the target is represent approximately by the half of the voltage variations observed as a consequence of the current perturbations introduced by the load.

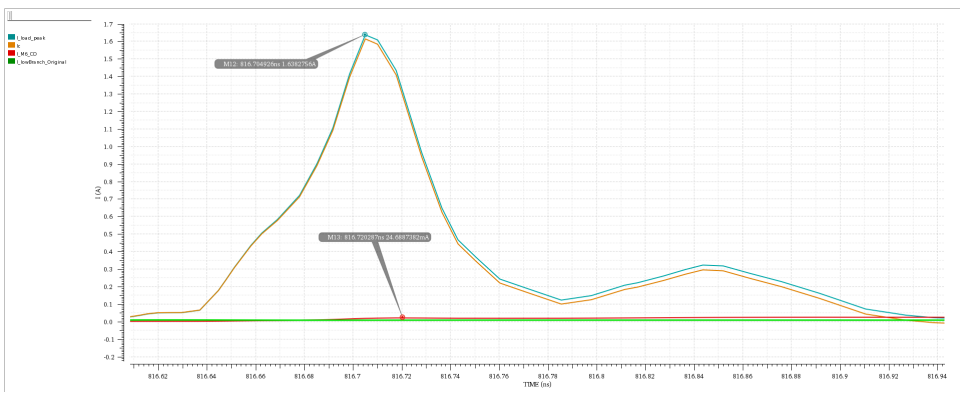


Figure 5.5: CD and Original: Current Management Relative Comparison

As a conclusion of this section, let us notice that the presented CD-stage is actually effective in setting the desired DC point of the output voltage. Moreover, it shows a better capability in managing the load perturbations. Nevertheless, it is intrinsically disadvantaged in a comparison with the original realization of the Internal Supply generator, and it does not give place to a substantial improvement to the overall behaviour of the circuit.

5.3 Open-Loop Stage

As pointed out in the previous section, the CD-stage is not effective enough in managing the current sourced and sank by the load. In fact, when an impulse of the load current arrives, almost all the charge is kept by the output capacitor while a minimal part is driven to ground through the Push-Pull structure of the CD-stage. Thus, most of the load current contributes to charge/discharge the output node, similarly to what happened with the original version of the Internal Supply Generator, leading to a voltage perturbation in the output rail, according to 3.1.

These observations highlight the need for an alternative solution, much more incisive, for the management of the impulse current injected and absorbed by the load at every commutation. The response to this need suggested in this thesis is the introduction of an additive stage, here called Open-Loop Stage, sketched in Fig. 5.6.

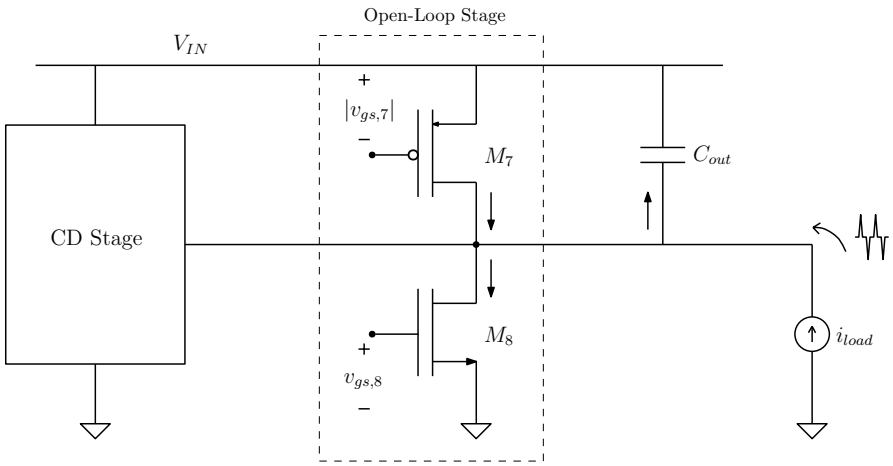


Figure 5.6: Open-Loop Stage Regulator

The basic idea behind the introduction of this new stage is very simple: whenever a current pulse is injected in the output node of the Internal generator by the load, the pMOS M_7 is turned on in order to conduct a significative portion of this pulse to ground, representing, in this way, an alternative path for the current that decreases the overall impedance seen by the load; similarly, when a current pulse is absorbed through the output rail, the pMOS M_8 is turned on and helps the capacitor deliver the charge required by the load. Finally, when the current pulses are extinguished, and when no current is sourced or sank by the load, the two transistors of the OL-stage are off, and the output voltage is effectively fixed to the target 2.1 V by the CD-stage. Notice that, in such a way, there is no static power consumption introduced by the OL-stage. On the other hand, an energy loss associated with the switching activity is expected.

More specifically, the transistors of the OL-stage are driven by a signal applied to their gates. In particular, the amplitude of the $|v_{gs}(t)|$ signal has to exceed the magnitude of the threshold voltage ($|V_t|$) in correspondence of the current peaks imposed by the load. Obviously, the contribution in managing the load current offered by these transistors will be determined by their size, by the amplitude of the driven signal, and by the quality of the synchronization between such a driven signal and the load current peaks. In this design, $W_7 = 3\ mm$ and $W_8 = 1.8\ mm$ have been selected for the width of the transistors M_7 and M_8 respectively. Notice that these widths are relatively large, because these transistors have to be able to conduct a noticeable current (several hundreds of mA) with a limited overdrive voltage (they are MV devices

that tolerate a maximum V_{gs} of 2.5 V and with a minimum channel length of 400 nm). Nevertheless, they are still significantly smaller than the power switch transistors (whose width is of 40 mm.

Fig. 5.7 represents the idea of the synchronization between the load current peaks and the activation of the OL-stage.

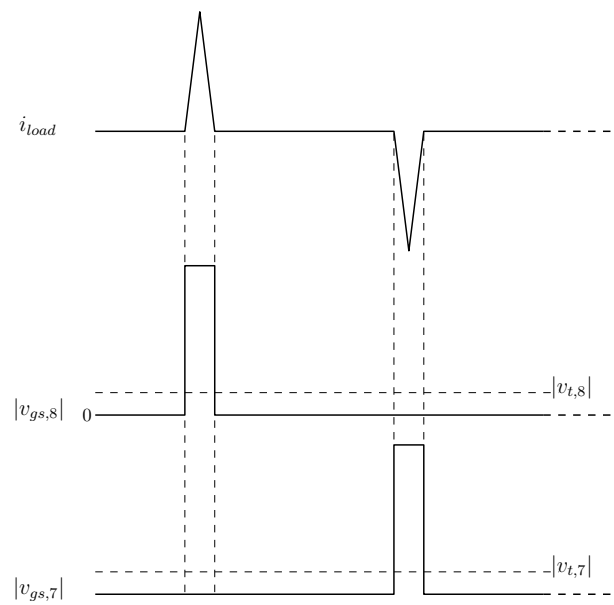


Figure 5.7: OL-Stage Synchronized Activation

At this point the issue of generating the driver signals for the OL transistors has to be faced. Two main ways have been considered: feedback driving and open-loop driving (as suggested by the name of the stage we are describing, the second way to drive the transistors has been adopted in the final solution).

5.3.1 Feedback Driving

This approach involves the generation of the driving signal on the base of information about the output voltage $v_{HS}(t)$ sensed and processed by means of a feedback mechanism. Let us consider the conceptual circuit realization sketched in Fig. 5.8.

Here a simplified version is represented, where the load injects a unipolar (positive only) impulsive current that has to be managed by the transistor M_8. The management of negative pulse of currents is treated in an analogous way by the transistor M_7, and so it is not here represented. Notice that, when there are no perturbations introduced by the load, M_8 is biased with $V_{GS,8} < V_{t,8}$. Also, the output voltage $v_{HS}(t)$ is set at 2.1 V by the common drain stage, and so the error processed by the error amplifier is zero. Hence M_8 is off and does not conduct current. On the other hand, the incoming of positive peaks

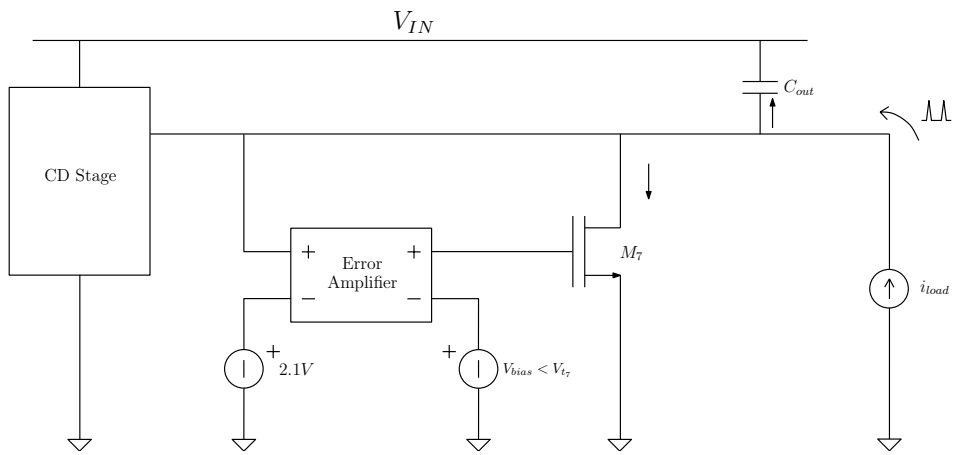


Figure 5.8: Feedback Driving Principle

of currents from the load tends to generate an increasing in the output rail voltage by discharging the capacitor C_{out}. $v_{HS}(t)$ is then compared with a constant reference of 2.1 V, and the positive difference (error) is amplified by the error amplifier. This amplified signal is summed to the DC biasing voltage, and causes $V_{gs}(t)$ to exceed $V_{t,8}$ and M_8 to turn on consequently. This way, M_8 finally conducts current and contributes to manage the charge injected by the load, limiting the voltage fluctuation as desired.

This method is interesting and attractive because it theoretically allows to reach a stable system in which the activity of the OL-stage transistors (here this name is not proper..) is linked to the evolution of the voltage to regulate itself by means of a negative feedback mechanism. Nevertheless, it presents some limitation that make it impossible to implement practically. Since the load current is impulsive, the voltage disturbances introduced in the output voltage of the Internal Supply general has an impulsive character as well. A circuit realization of the system sketched in Fig 5.6, where both M_7 and M_8 are driven through a feedback mechanism has been simulated, and Fig 5.9 shows the frequency spectrum of the output voltage.

Notice that a 2.1 V dc component is present, as expected. Also, it is interesting to observe that the signal is uniformly distributed over frequency component allocated at multiple frequencies of f_s. Such a frequency spectrum is actually typical of impulsive signals. Notice that the presented signal, deprived of his 2.1 V dc component is essentially the error signal at the input of error amplifier. Therefore, in order to correctly amplify its input signal, the error amplifier should present a huge bandwidth, still offering a gain sufficient to effectively turning on the transistors. The problem of this solution stems from here: such an amplifier is not available. In other words, the feedback mechanism is not fast enough to adequately compensate such a high frequency disturbance, and an alternative solution to drive the transistors M_7 and M_8 has to be found.

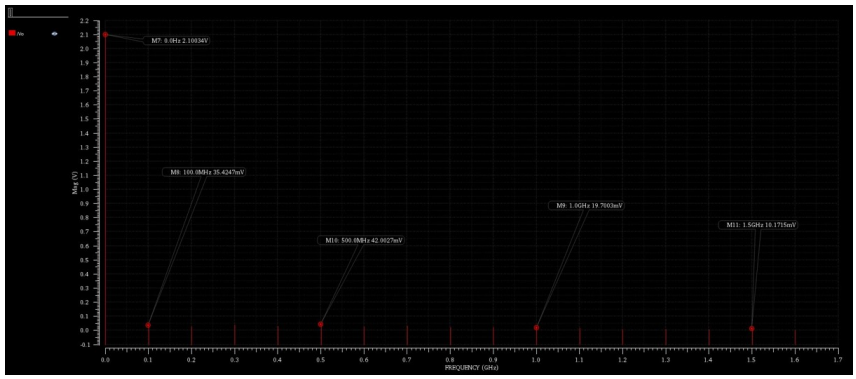


Figure 5.9: Output Voltage Frequency Spectrum

Fig. 5.10 graphically illustrates this idea. Here the error amplifiers have been endowed with a first order transfer function characterized by a gain of 10 (in the band) and a bandwidth of 1000 GHz, 1 GHz and 20 MHz alternatively. In particular, Fig. 5.10 shows the comparison between the managements of a load current peak in the three cases. Notice that in the case with a 1 GHz BW, the system is already too slow to activate the transistors during the current peaks effectively, and with a 20 MHz BW, the activation of the transistors is nearly null.

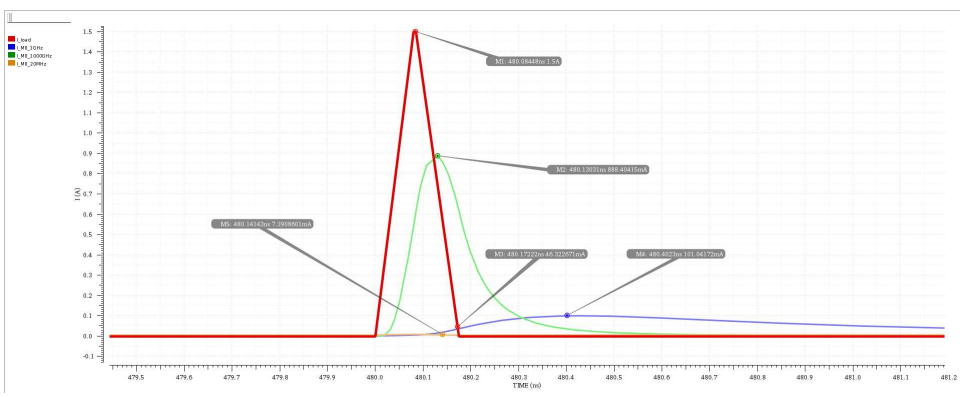


Figure 5.10: Limited Bandwidth Activation Comparison

5.3.2 Open-Loop Driving

An alternative solution to drive the transistors M_7 and M_8 involves exploiting a-priori information about the converter's power stage rather than a direct information about the voltage to regulate. In fact, it is known that the current peaks at the output rail of the Internal Supply Generator are associated with

the charging/discharging processes of the intermediate nodes of the buffer, and of the parasitic capacitances of the cascode power switches. For this reason, these current peaks occur immediately after the edges of the driver signal which trigger the switching activity of the commutation cell. Thus, starting from the mentioned driver signal edges, it is possible to synchronize the activation of the M_7 and M_8 transistors. The stage obtained in this way is driven by an open-loop mechanism, and this motivates the name chosen for it. A conceptual representation of the Internal Voltage Regulator presented so far is given in Fig. 5.11. A possible solution to realize the synchronization between the current peaks and the activity of the OL transistors will be treated in Chapter 6. Instead, in the next sections, we will refer to testbenches in which the driving signals are delivered by ideal generator in order to explore the potential and the limitations of this new stage.

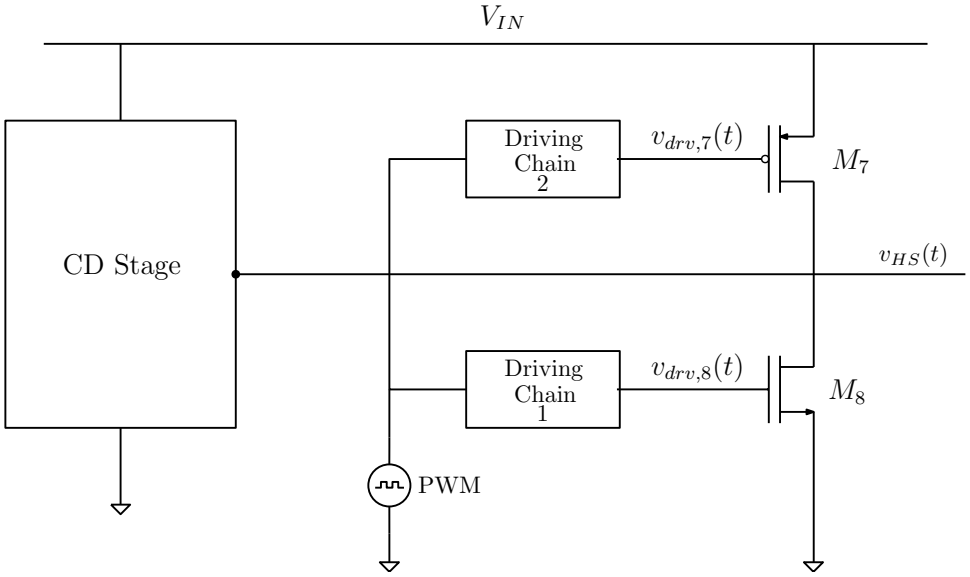


Figure 5.11: OL Drived Transistors Stage

Ideal Driving: Simulation Results

In the situation considered in this section, a nearly perfect synchronization will be implemented by an ideal generator to underline the potential of the OL-stage. Fig 5.12 shows the current peaks coming from the load and the M_7 and M_8 driving signals.

Notice that, despite the two transistors of the OL-stage being able to nominally tolerate voltage stresses of 2.5 V (they are what we previously called "MV" devices), the driving signals have still been shaped with an amplitude of 2.1 V. This choice has been done in order to simplify their practical implementation,

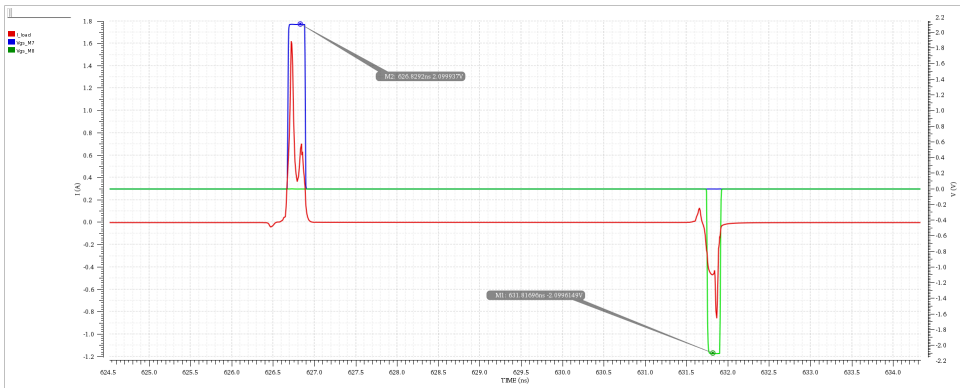


Figure 5.12: OL-Stage Perfect Activation

treated in Chapter 6. In fact, in such a way they can be generated by using the already available supplies at 1.5 V, 2.1 V and 3.6 V. Notice even that, as mentioned, the activation of transistors is here nearly perfect, in that the voltage and current pulses happen at the same time and have, approximately, the same duration. This nearly perfect activation translates into the current management showed in Fig. 5.13. Here, a positive current peak injected by the load is represented (red). For the KCL, this current is divided into the available paths: it may enter in the drain of M8 (blue), in the capacitor (green), and in the drain of M6 (orange).

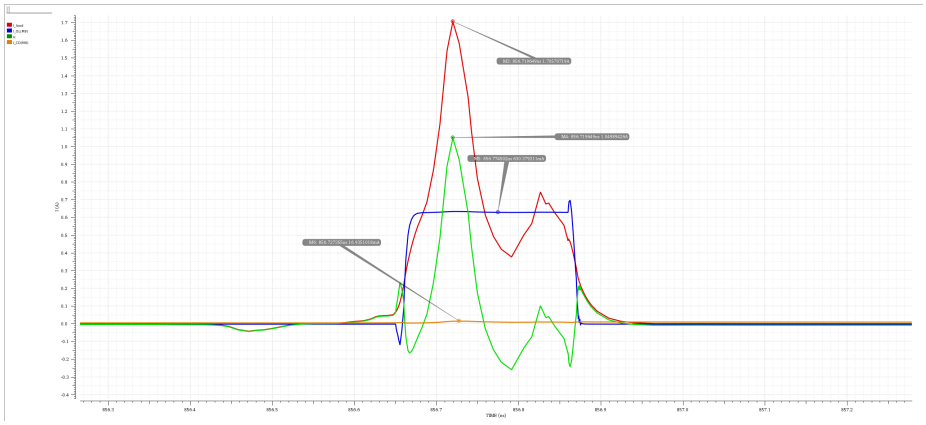


Figure 5.13: OL-Stage Perfect Activation: Current Management

Notice that, as opposed to the pure CD-generator and the original one where nearly all the charge was taken by the capacitor, here a very significant aid to the management of the charge is offered by the OL-stage. This desirable behavior corresponds to the situation depicted in Fig. 5.14, where the output voltage

waveform $v_{HS}(t)$ obtained with the introduction of the OL-stage is compared with the original one.

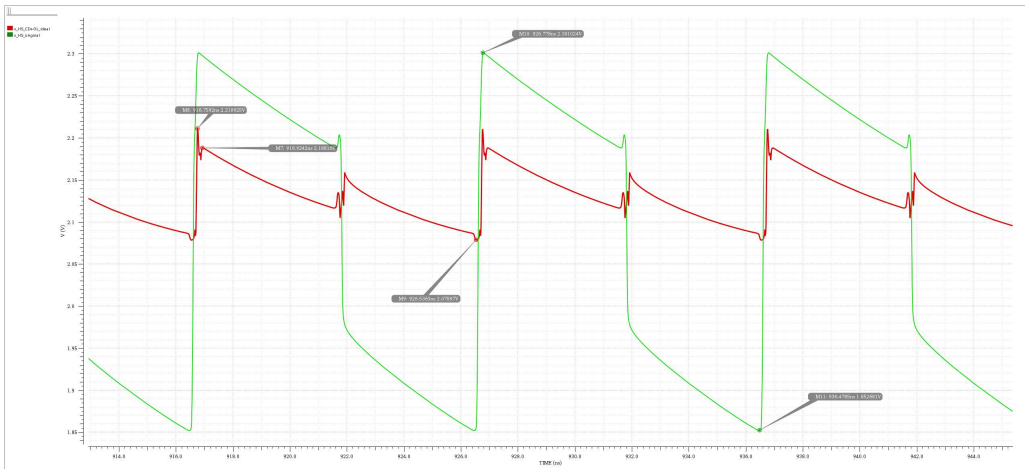


Figure 5.14: Output Voltage Comparison: Original vs CD&OL

This comparison highlights the very good potential improvement that may be targeted with the implementation of the new regulator. In fact, now the output voltage is essentially confined in the range between 2.08 V and 2.2 V, and it is much closer to the ideal target constant voltage of 2.1 V.

This situation has two interesting implications:

- There are no more excessive voltage stresses in the driving chain: no more SOA violations are reported. As an example, Fig. 5.15 shows the comparison between the v_{gs} voltage of a transistor of the high-side buffer. Notice that the new situation features a voltage level always inferior to 1.5 V. On the other side, with the original regulator, the voltage stress exceeds the threshold of 1.65 V for about one third of the period. This may potentially lead to a more reliable operation of the converter;

- There is a large margin to reduce the output capacitance and still get an improved output voltage. An example is given with Fig. 5.16, where the original output behavior (green) is compared with the output voltage imposed by the new solution employing an output capacitance C_{out} reduced by 66.7% (100 pF in place of 300 pF) (red). Notice that in face of a really significant reduction of the area occupation, still an important improvement is exhibited in the output voltage regulation.

Errors in the Driving Signal Generation

In the last section, the attractive potential improvements introduced by a well driven OL-stage have been pointed out. Now, let us try to investigate what

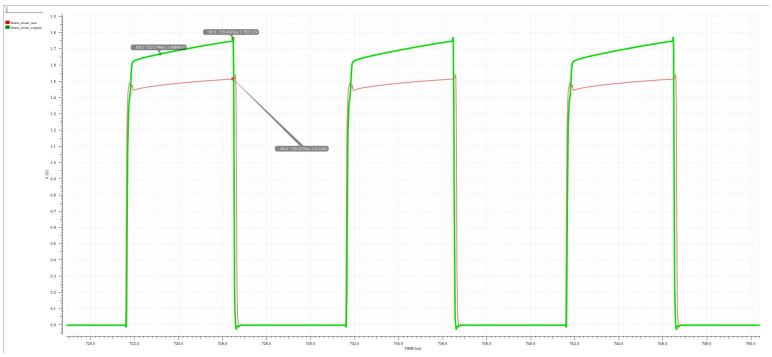


Figure 5.15: Voltage Stresses Comparison: Original vs CD&OL

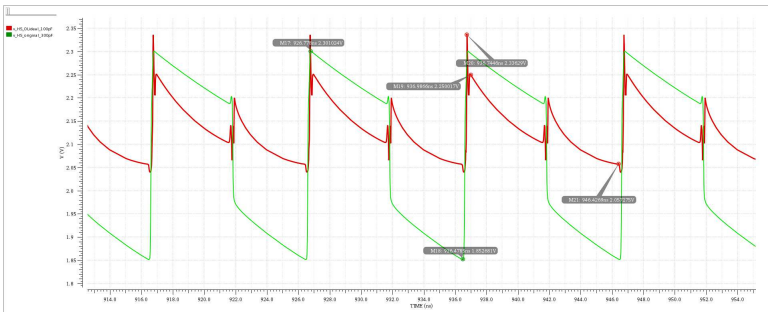


Figure 5.16: Output Voltage Improvement and Area Saving

happens if the driver signal is not perfectly adherent with the time span of the current peak to manage. In particular, we will consider two situations that represent respectively a "small deviation" and a "drastic deviation" with respect to the ideal driving behavior.

Small Deviation

Here the same system as before has been simulated, with the difference that the driving signal of M_8 has now been shaped with double the time duration as before, as shown in Fig. 5.17. In other words, a not-perfect OL activation of M_8 is introducing a "small" perturbation in the output rail. In practice, after the load current peak is extinguished, M_8 goes on conducting for a while (about 150 ps), causing the output capacitor to charge and, consequently, inducing a voltage drop at the output rail.

Such a voltage drop can be observed in Fig. 5.18. The perturbation is followed by a major activation of the CD-stage, which tries to reestablish the 2.1 V at the output. Nevertheless, the overall behavior is characterized by a slight reduction in the dc voltage, and by larger output voltage variations. Moreover, a deterioration of the power efficiency is expected, especially as a

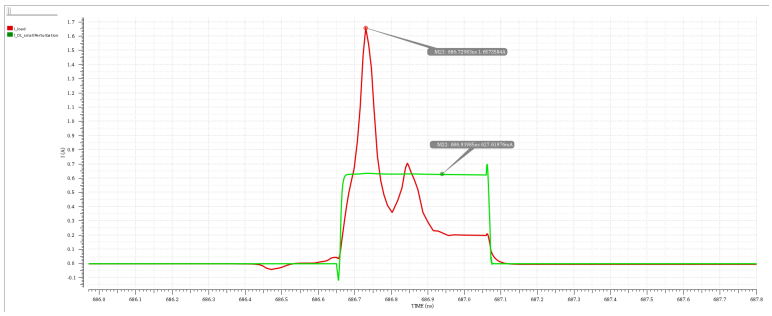


Figure 5.17: OL-Stage Introducing a Small Perturbation in the Output Rail

consequence of the conduction losses associated with the M_8 undesired activity.

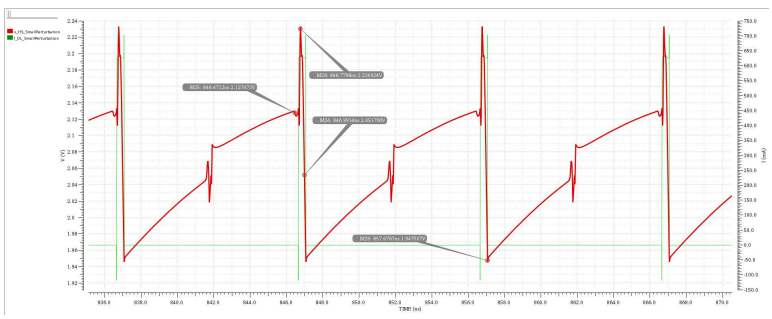


Figure 5.18: Output Voltage Perturbation due to a Small Variation from the Ideal Activation of the OL-Stage

Drastic Deviation

Now a more drastic scenario is considered to represent an almost compromised functioning of the OL- stage driving mechanism: it is assumed that the activation time of M_8 is about ten times the load current peak duration. Fig. 5.19 shows the trend of the most significant currents in the Internal Supply Generator when a positive current peak is injected by the load while Fig. 5.20 shows the trend of the output voltage $v_{HS}(t)$. Notice that, during the huge time in which M_8 is on (about 2 ns every period), the output node is discharged and its potential drops down to about 510 mV. In fact, during this interval, the M_8 current essentially charges the output capacitor. Then, it is possible to observe an extraordinary activation of the transistor M_5 of the CD-stage, trying to re-establish its equilibrium point characterized by the 2.1 V at the output. Nevertheless, this intervention is slow, and more than half period is required before approaching the desired output voltage again. In such a situation, the voltage stress on the transistors of the driving chain of the power switches is inadmissible, and the overall operation of the power stage is compromised.

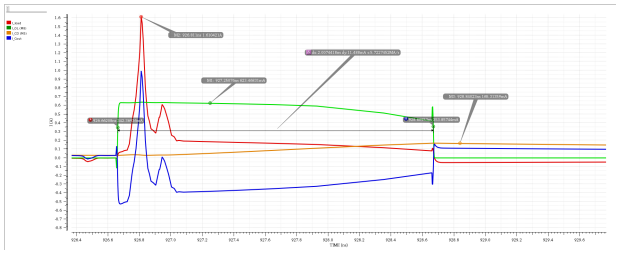


Figure 5.19: Drastic Perturbation Management

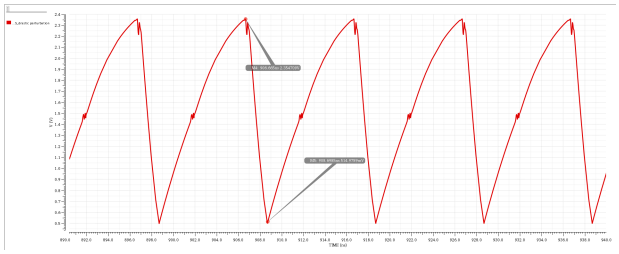


Figure 5.20: Output Voltage Drastic Perturbation

5.4 Common-Source Stage

There are two aspects that need to be underlined:

- Recall that one of the reasons for which the Internal Supply Generator should impose at its output a constant voltage is to limit the voltage stress on the LV transistors of the driving chain of the power switches. In order to do that it is surely important to limit the voltage variations associated with the peaks of current injected and absorbed by the load; this is the main purpose of the OL-stage just described. In fact, a big voltage variation in the output rail may be associated with a big overstress. Nonetheless, not only the amplitude of the overstress is important in order to prevent the breakdown of the transistors, but even the amount of time these are exposed to the excessive voltage stresses. For this reason, it is important that, once a voltage variation occurs in the internal supplies, the target equilibrium point is soon restored. The OL-stage does not help in this sense and, as showed in the previous sections, the CD-stage is very limited in doing this as well.

- In general, the problem of perfectly synchronizing the very short load current peaks with the activation of the OL-stage transistors is not trivial. Dealing with longer driving signals may lead to a simplification of the problem. Plus, when it comes to driving large transistors, generating a longer impulse is easier itself because it is less demanding on the buffer structure necessary to make the signal strong enough. Nonetheless, in the

previous section it has been pointed out that the internal supply delivered by the generator developed so far is very sensible to variation in the duration of the driving signals and, if such a variation is large enough, the overall behavior of the generator may be compromised.

In order to overcome these problems an additive stage may be added to the Internal Supply Generator. Similarly to the OL-stage, even the core of this new stage which will be referred as Common-Source (CS) Stage, is made by a nMOS and a pMOS connected to the output node of the generator, as sketched in Fig. 5.21.

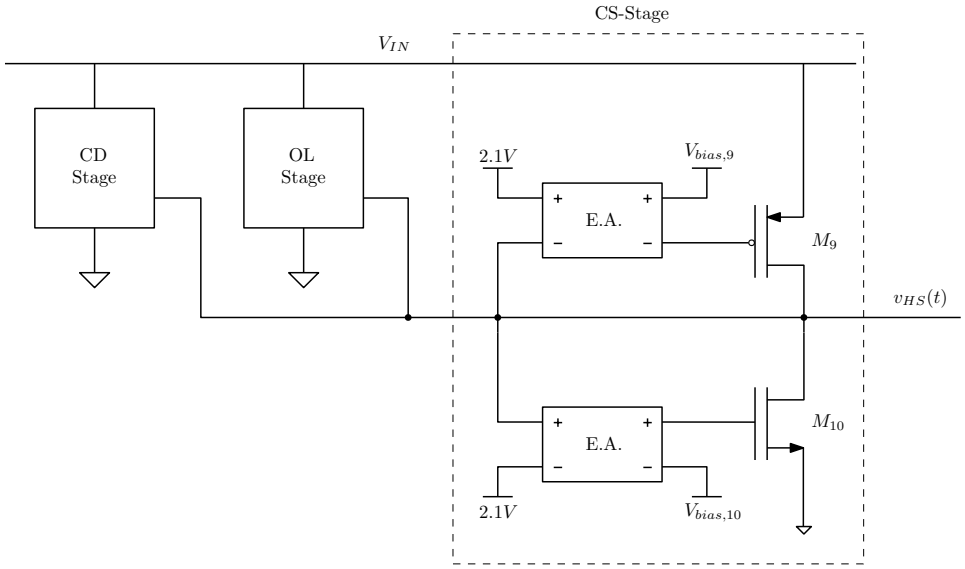


Figure 5.21: Common Source Stage Added to the Internal Supply Generator

The difference is that, in this new stage, these transistors are not driven by an open loop chain, but by a feedback mechanism. Such a solution, which in Section 5.3.1 has been discarded, is now a possibility and represents a convenient choice. In fact, the CS-stage, as opposed to what happened to the OL one, does not have the purpose of instantly managing the very fast disturbances introduced by the load, which would require a huge non-implementable bandwidth. Instead, its tasks are:

- Contributing to re-establish the target voltage in the output rail of the Internal Supply Generator as fast as possible after a variation occurs as a consequence of the current peaks injected and absorbed by the load;
- Rejecting the disturbances in the output rail associated with an excessive activation of the OL-stage transistors. These disturbances may still be current pulses, but longer, and with a lower amplitude with respect to

those introduced by the load. Thus, they can be rejected even through a feedback stage with a limited BW.

In order to compensate in a satisfactory manner the excessive activation of the OL-stage, if it occurs, the CS-stage transistors and the OL-stage ones should have similar sizes.

Notice that, to limit the power dissipation, the CS-transistors are biased in such a way that, when the output voltage is set at the target value, both of them are off. Nevertheless, if the OL-stage activation is excessive, then the disturbances in the output rail are noticeable, and the activation of the CS-stage is noticeable as well. This leads to significant losses and, contextually, to a degradation of the overall power efficiency of the converter. For this reason, a well calibrated and synchronized activation of the OL-stage is still absolutely advisable.

5.5 Simulation Results

In this section, some simulation results about the developed Internal Supply Generator will be shown and commented. Moreover, a comparison with the original circuit will be carried out. Particular attention will be put in the internal supply voltage level, in the voltage stresses in the driving chain, in the area occupation (roughly represented by the output capacitance value), and in the overall power efficiency of the converter, which are the most significant metrics in this design process.

Notice that this system here simulated is characterized by some ideal blocks and mechanism. In particular, the OL-stage driving chains are modeled by ideal voltage generator well synchronized with the load current peaks. Furthermore, the error amplifiers in the CS-stage are blocks with a low-pass first order transfer function characterized by an in-band gain of 10 and by a bandwidth of 20 MHz.

In fact, the results showed here aim to represent the potential of the proposed solution after certifying its feasibility, and not the actual behavior of the new developed system. Some degradation in the performances is expected after the implementation, especially due to the delicate task of synchronizing the load disturbances with the OL-stage activation.

Output Voltage

Fig. 5.22 represents a comparison between the high-side internal supply voltage delivered by the developed generator and that delivered by the original one.

It is possible to notice that the new Internal Supply Generator shows a noticeably improved performance. In particular, the perturbations introduced by the load result in a much smaller variations in the output voltage $v_{HS}(t)$ (the maximum surge decreases from more than 450 mV to less than 150 mV). Thus, the output waveform is much closer to the target constant value of 2.1 V.

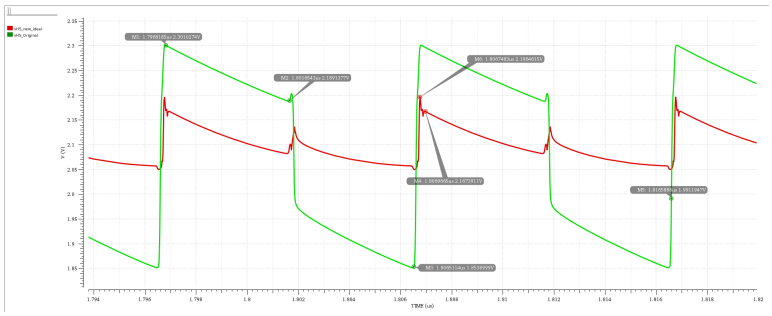


Figure 5.22: New and Original Generators: Output Voltage Comparison

Voltage Stresses

Fig. 5.23 shows the gate-to-source voltage in a transistor of the tapered buffer of the high-side driving chain in two different cases. In particular, the case where the Internal Supply Generator is implemented with the just developed design (red waveform) is compared to the case where it is implemented by the original one (green waveform). Notice that the gate-to-source and the drain-to-source voltages waveforms of all the transistors in the tapered buffer are very similar to each other, therefore this comparison is representative of the voltage stresses in all the high-side driving chain.

The devices that implement the buffer can nominally tolerate voltages up to 1.5 V, and SOA violations are reported when the stresses exceed this limit of more than 10 %. Let us notice that in the original system this last situation characterizes a very significant portion of the period (with a duty cycle of 0.5 around one third of it), leading to a deterioration of the reliability. Instead, with the new Internal Supply Generator the SOA is never violated, and the stresses are confined under 1.55 V.

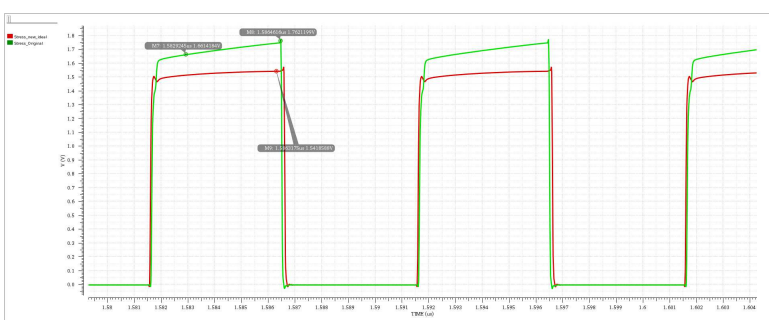


Figure 5.23: New and Original Generators: Voltage Stresses Comparison

Improved Behavior and Area Saving

One of the most critical aspects of the converter under analysis is the excessive usage of integrated capacitance, that is the main contributor in the area occupation in the test-chip, as shown in Fig. 3.13. A noticeable portion of this capacitance is allocated in the Internal Supply Generator and, as already mentioned, one of the purposes of the new design is to reduce the overall capacitance employed. Fig. 5.24 and 5.25 show a comparison between the performances of the original Internal Supply Generator (which exploits an output capacitance of 300 pF for the high-side rail), and the new design employing an output capacitance of 100 pF (reduced by 66.7 % with respect to the original circuit). In particular Fig. 5.24 shows a comparison between the output voltage $v_{HS}(t)$ in the two cases, while Fig. 5.25 confronts the voltage stresses on the high-side driving chain.

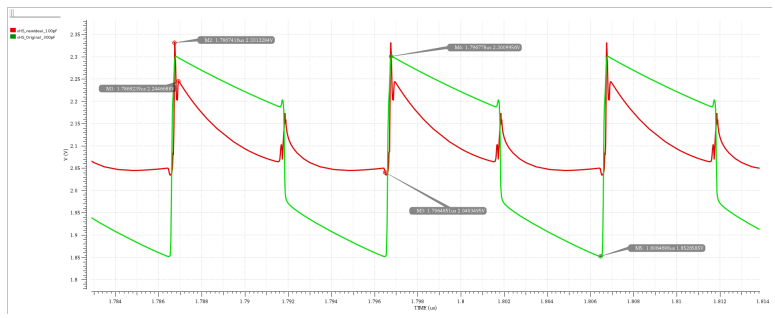


Figure 5.24: Output Voltage Comparison with Reduced Output Capacitance

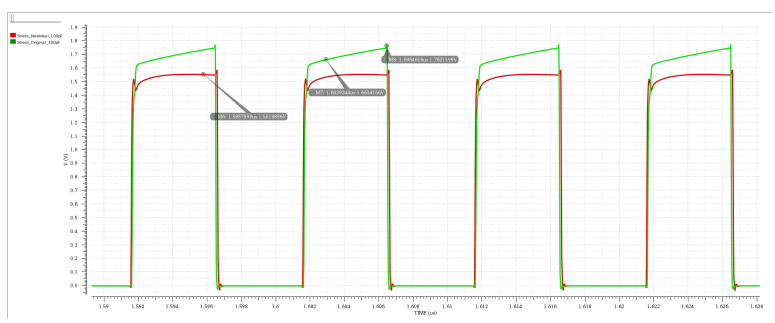


Figure 5.25: Voltage Stresses Comparison with Reduced Output Capacitance

Let us notice that, despite the very important reduction in the output capacitance value, the voltage in the output rail is still significantly improved, in that the perturbations induced by the load are smaller and the waveform is still visibly closer to the target constant 2.1 V. Moreover, even the voltage stresses are improved being constantly under the SOA violation threshold.

5.5.1 Bonding Wires

The connections between the supply voltage (V_{in}) and the chip that realizes the converter introduce some undesired parasitic effects[17] which so far has not been considered. Despite some more sophisticated (and more expensive) solutions that allow to limit these parasitic effects exist (e.g. pillars), in the realized test-chip of the converter under analysis these connections are realized through bonding wires. In particular, the parasitic effects, that may introduce noticeable alterations in the behavior of the system, can be modeled with the series of a resistor R_b and an inductor L_b inserted between the external supply and the power stage. Fig. 5.26 represents the Internal Supply Generator connected to the external supply through the bonding wires. Some measurements have been carried out on the available test-chip of the converter, that led to the estimations of the parasitic effects related to the bonding wires shown in Fig. 5.27.

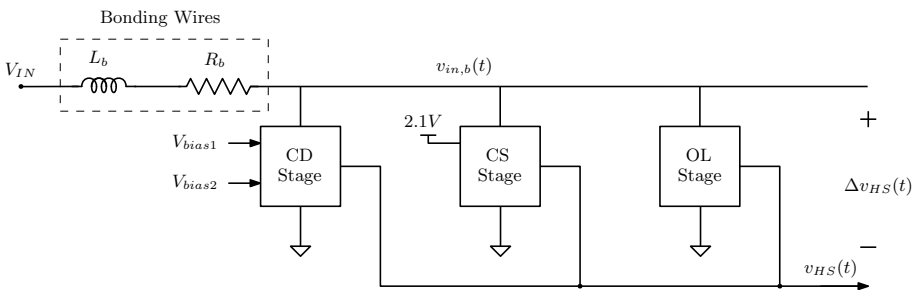


Figure 5.26: Internal Supply Generator Connected to External Supply through Bonding Wires

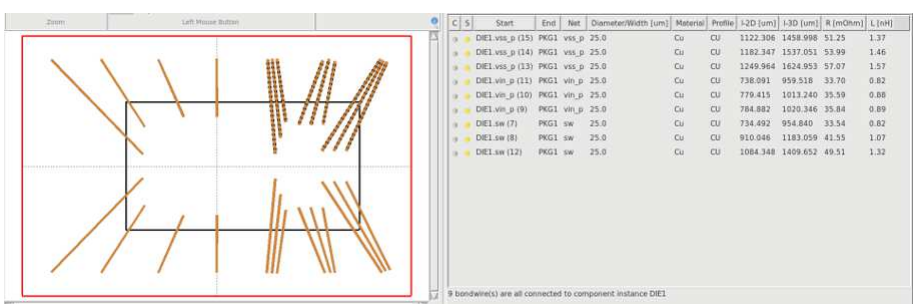


Figure 5.27: Estimated Bonding Wires Parasitic Effects

In particular, in the simulations carried out in this work of thesis, the following values have been adopted:

- $R_b = 12\ m\Omega$;
- $L_b = 300\ pH$.

Thus, in the following paragraphs some simulation results including the bonding wire parasitic effects as just described will be illustrated.

Output Voltage and Voltage Stresses

Now that the parasitic components associated with the bonding wires have been included in the system to simulate, the following clarification about the external supply should be done. Referring to Fig. 5.28, let us discern the two following voltage supplies:

- V_{IN} is the external supply constant to 3.6 V;
- $v_{in,b}(t)$ is the supply actually perceived by the power stage, downstream of the bonding wires. It is not constant, but it varies in time as a consequence of the parasitic effects.

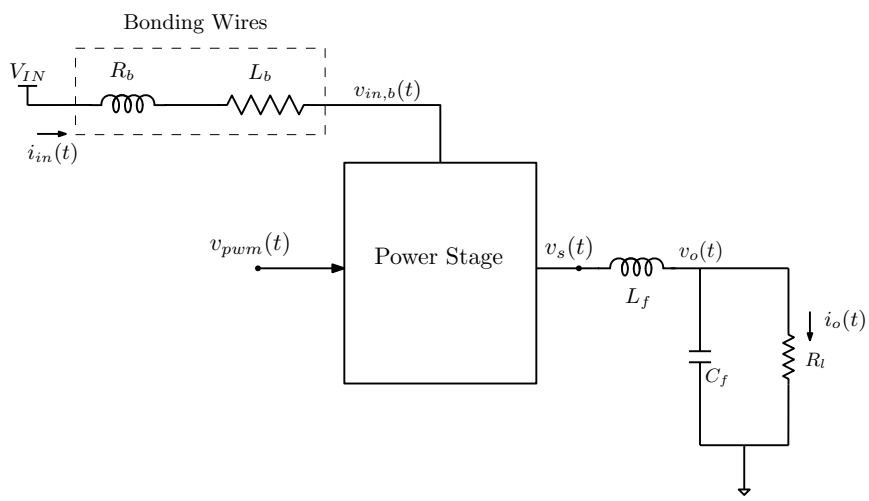


Figure 5.28: Connection to the External Supply Through Bonding Wires

Recall that the main purpose of the Internal Supply Generator is to deliver an ideally constant voltage at 1.5 V under the supply $v_{in,b}(t)$ perceived by the power stage. But since $v_{in,b}(t)$ is variable in time (and not constant at 3.6 V), it is appropriate to change the output voltage of the Internal Supply Generator from $v_{HS}(t)$ (which is no more representative of the functionality of the circuit block) to $\Delta v_{HS}(t)$, defined as:

$$\Delta v_{HS}(t) \triangleq v_{in,b}(t) - v_{HS}(t) \tag{5.7}$$

In other words, the task of the Internal Supply Generator is to deliver a $\Delta v_{HS}(t)$ as close as possible to the target constant value of 1.5 V. With this said, Fig. 5.29 shows a comparison between $\Delta v_{HS}(t)$ in the two cases in which

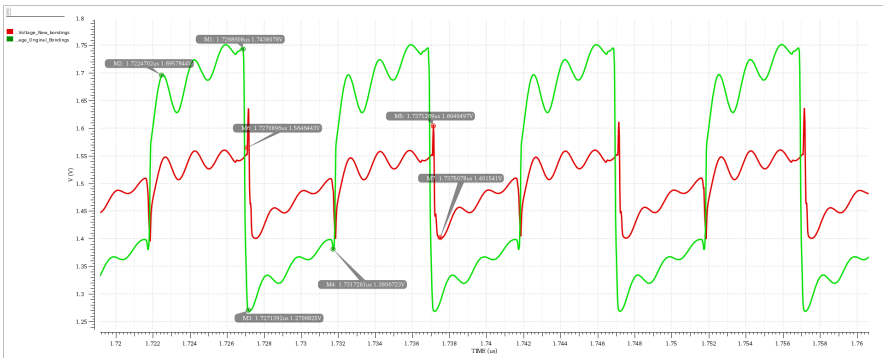


Figure 5.29: Comparison of Output Voltage Including Bonding Wires Parasitic Effects

the Internal Supply Generator is realized with the new design (red curve) and with the old one (green curve), including the bonding wires parasitic effects.

Let us notice that, even considering these parasitic effects, the new generator exhibits a better performance delivering an output voltage $\Delta v_{HS}(t)$ much closer to the constant target of 1.5 V for the entire period. This translates into an improved profile of the voltage stresses in the high-side driving chain as well, as shown in the Fig. 5.30. Again, with the solution developed in this chapter, the voltage stresses stay constantly under the SOA violation threshold, even considering the bonding wires, leading to an improved feasibility.

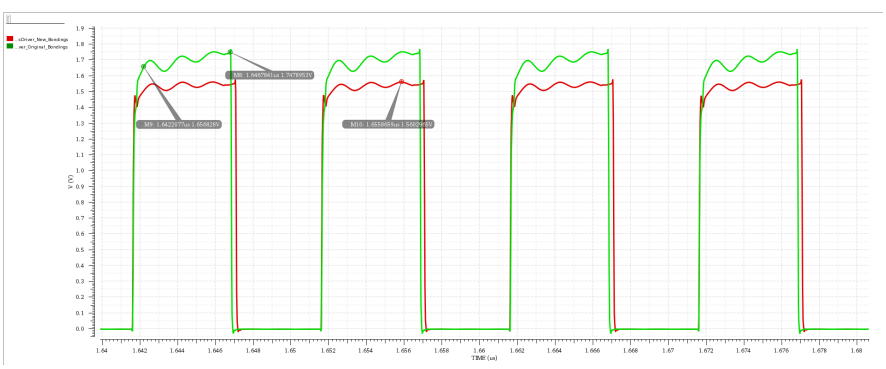


Figure 5.30: Comparison of Voltage Stresses Including Bonding Wires Parasitic Effects

Output Voltage, Voltage Stresses and Area Saving

Again, since one of the main purposes of the re-design of the Internal Supply Generator is to allow area saving in the chip, and since the integrated output capacitor in this block is one of the main contributors in area occupation, we

want now to asses if it is possible to significantly reduce its capacitance value and still get an improvement in the overall behavior even after having included the bonding wires in the model. Fig. 5.31 and Fig. 5.32 shows the behaviors of the Internal Supply Generator realized with the original design and employing an output capacitance of 300 pF (green curves), compared with the behavior obtained with the new design and employing an output capacitance of 100 pF (reduced by 66.7 %).

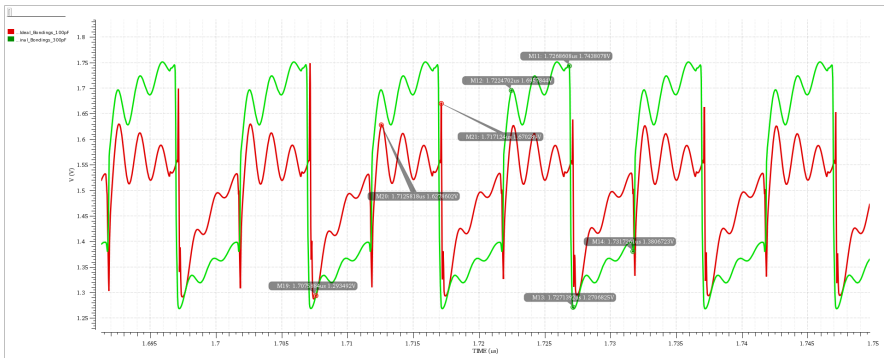


Figure 5.31: Output Voltage Comparison with a Reduced Output Capacitance

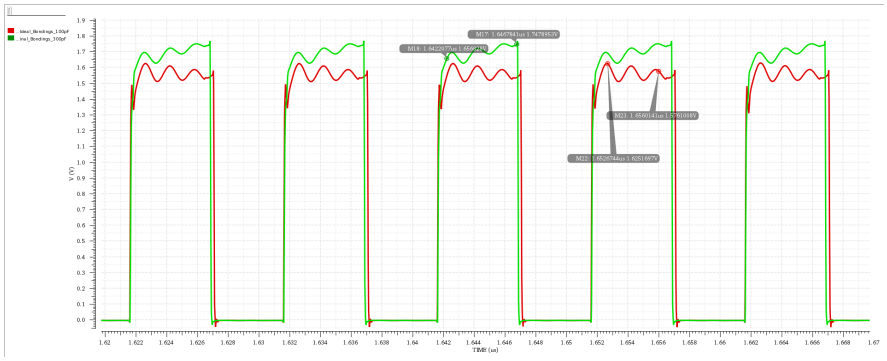


Figure 5.32: Voltage Stresses Comparison with a Reduced Output Capacitance

Despite a very important reduction in the integrated capacitance value, which leads to a significant reduction in the area occupation, it is possible to notice a net overall improvement of the performances. In particular, Fig. 5.31 shows a better a $\Delta v_{HS}(t)$, which stay closer to the target constant of 1.5 V for all the period, while Fig. 5.32 shows a reduced voltage stress profile in the high-side driving chain: with the new design, even integrating much less capacitance, the SOA is never violated, while with the old design violations occur for a very significant portion of the period (about one third with a duty cycle of 0.5).

5.5.2 Power Efficiency

The overall *Power Efficiency* of the power stage of the converter has been assessed through the simulation tool. In particular, the active input and output powers, P_{in} and P_{out} respectively, have been estimated, and then (2.1) have been used to calculate the efficiency.

Recall that:

$$\begin{cases} P_{in} = \frac{1}{T_s}\int_t^{t+T_s}(V_{in}\cdot i_{in}(t))dt, \\ P_{out} = \frac{1}{T_s}\int_t^{t+T_s}(v_o(t)\cdot i_o(t))dt, \end{cases} \tag{5.8}$$

where V_{in},$i_{in}(t)$, $v_{out}(t)$ and $i_{out}(t)$ are those shown in Fig. 5.31.

Table 5.1 shows a comparison between the energetic behavior of the converter power stage in the two cases in which the Internal Supply Generator has been implemented with the original design or with the one proposed in this chapter:

	Original	**New**
No Bonding Wires	83.45 %	76.24 %
With Bonding Wires	86.88 %	79.31 %

Table 5.1

It is possible to observe that, from the energetic point of view, the new design exhibits a worse behavior, showing an efficiency of 79.3 % which is a reduction of about 7 % with respect to the original case. This phenomenon is connected to the fact that, in order to manage the charge injected in the output rail by the load, with the new design relatively large MOSFETs are turned on and dissipate energy conducting current through their resistive channels.

5.6 Final Considerations

In this chapter, an alternative design for the Internal Supply generator has been proposed and its attractive potential have been illustrated. In particular, it allows to reach a net improvement in the voltage imposed at the output port, associated with a diminished stress in the high-side driving chain. It has also been shown that such an improvement can be accompanied by a reduction of the integrated output capacitance up until 70 % of the original employed value, leading to a significant area saving. On the other side, it has been shown that by adopting the new design, a reduction of about 7 % in the power efficiency is expected.

Nevertheless, as already mentioned, these performances are subordinate to the realization of some ideal blocks and mechanisms. In particular, Chapter 6 will be dedicated to present and treat the problem of driving the OL-stage transistors, synchronizing their activity with the peaks of current alternatively injected and absorbed by the load.

Chapter 6

Open Loop Stage Driving Chain

6.1 Introduction

This chapter is dedicated to present the problem of synchronizing the activation of the OL-stage transistors with the perturbations introduced by the load in the output rail of the Internal Supply Generator described in Chapter 5. Then, a possible solution of this problem will be proposed and described. In particular, a driving chain for the transistor M_8 will be developed while, in the simulations, the driving of M_7 will be kept ideal. Let us specify, anyway, that an analog solution of the one given for M_8 could be adopted even for M_7, with some adaptations.

It has been already observed that the load alternatively absorbs and injects some current peaks in the output rail of the Internal Supply Generator. As already explained in Section 5.3, the transistor M_8 has the task of managing the injected peaks by turning on when these occur, providing in this way an additive path for the current and lowering the overall impedance at the output node. In order to do this, and to avoid useless power loss, M_8 is supposed to stay off during all the period and turning on for the only last of the entering current peak. This behavior can be realized by generating a driving signal $v_{drv,8}(t)$ for M_8 as represented in Fig. 6.1.

Despite employing an nMOS for the transistor M_8 in the scheme presented in Chapter 5, in the design that is going to be developed, a pMOS will be used instead, as shown in Fig. 6.2. This choice has been done in order to implement a *charge recycling* principle [7], [1], [12],[2]. In fact, in such a way, the parasitic gate-to-source capacitance $C_{gs,8}$ of M_8 is connected directly to the output node. This produce two desirable effects:

- It concurs to manage the entering (and the exiting as well) current peaks, lowering the overall output impedance;

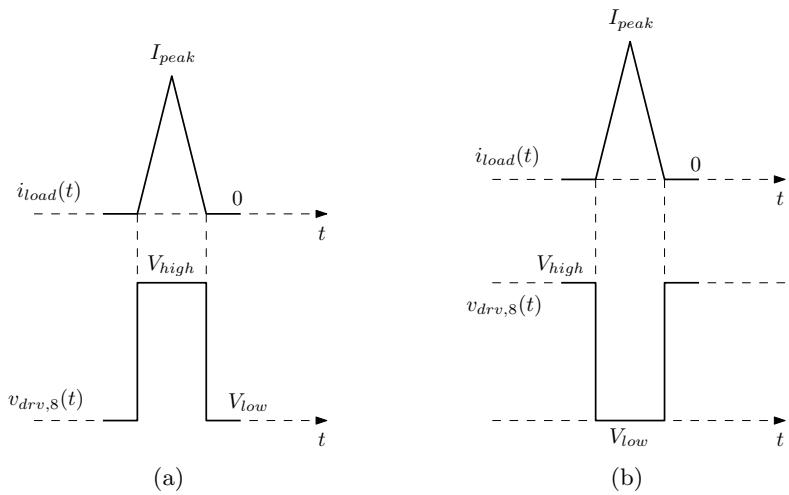


Figure 6.1: (a) M_8 Driving Signal nMOS (b) M_8 Driving Signal pMOS

- The minor part of the arriving charge that enters in this parasitic capacitor when a current peak occurs contributes to generate the driving signal at the gate of M_8, thus simplifying the task of the driving circuit.

With this said, notice that Fig. 6.1(a) shows the desired driving signal when M_8 is a nMOS, while Fig. 6.1(b) shows the desired driving signal when M_8 is a pMOS.

6.1.1 Idea for Driving

As already discussed, and as the name suggests, the OL-stage transistors are not controlled through a feedback mechanism based on the sensing of the voltage to regulate. In fact, for such a functionality, a feedback mechanism would require an excessive not-implementable bandwidth. Rather, they are driven in open loop, on the base of some indirect available information about the system. In fact, by the analysis of the power stage operation, it is known that the entering current peaks injected by the load occur immediately after the rising edge of the PWM signal $v_{pwm}(t)$. Actually, the entering current peaks are associated with the discharge of some intermediate nodes of the tapered buffer and of the gate capacitances of the two transistors (LV and MV) that implement the high-side power switch in the commutation cell. Analogously, the exiting current peaks absorbed by the load are associated with the charge of the gate-to-source and gate-to-drain parasitic capacitances of the cascode MV transistor of the high-side power switch in the commutation cell. Notice that these discharge and charge processes correspond with the switching-on and the switching-off of the high side power switch, and therefore, they happen as a consequence of the edges of the control signal $v_{pwm}(t)$, as said.

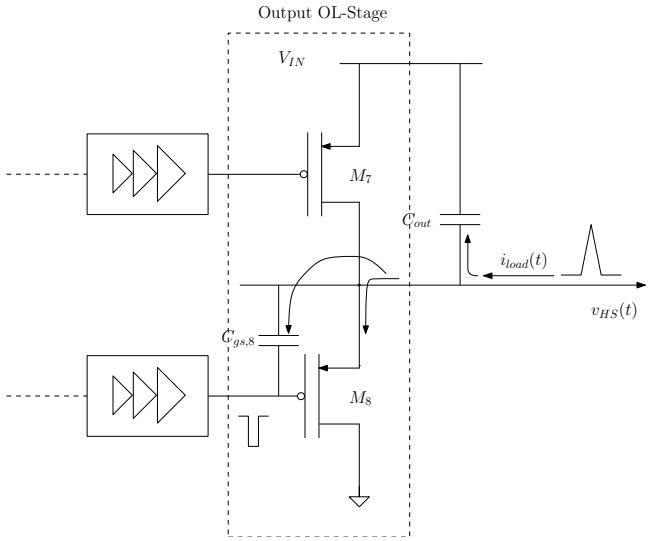


Figure 6.2: Charge Recycling

In other words, it is known that the current peaks injected by the load occur consequently to the rising edges of the control signal. Hence, it is possible to take the control signal in one intermediate node of the high-side driving chain, and exploit it to drive the OL-stage transistors. At this point there are two issues to deal with:

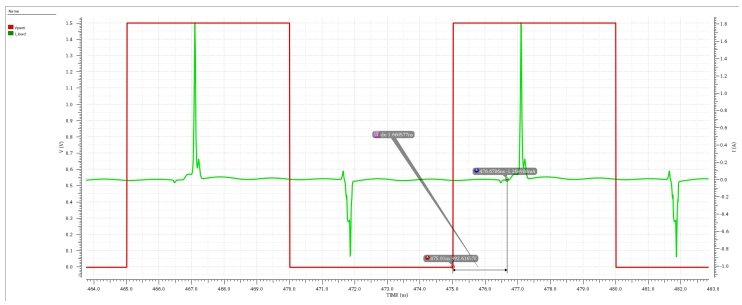
- The control signal itself is not suited to adequately drive the transistor M_8 of the OL-stage. In fact, its shape is different from the desired one showed in Fig. 6.1(b). Furthermore, the transistor M_8 is relatively large ($W_8 = 3$ mm), and the parasitic capacitance at its gate also is. Thus, the output stage of the driving signal has to be "strong" enough to adequately shape the short impulsive signal $v_{drv,8}(t)$. These points lead to the need for a driving chain that processes the control signal and delivers the driving one.

- As it will be pointed out, the OL-driving chain requires some time to process the control signal (several hundreds of ps). Let us call this time T_{drv}. Obviously the time interval between the considered rising edge of the control signal and the injected current peak, $T_{ctrl,load}$, must exceed T_{drv}:

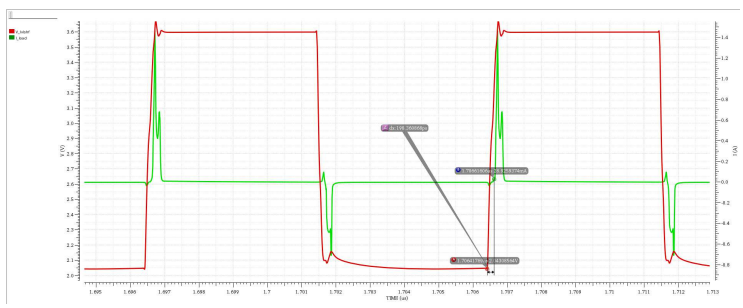
$$T_{ctrl,load} > T_{drv}, \tag{6.1}$$

  otherwise the transistor M_8 would be activated too late, when the current peak is already extinguished and when the undesired voltage variation in the output rail of the Internal Supply Generator already happened.

Therefore, the point in the high-side driving chain where the control signal is taken has to be appropriately chosen in order to satisfy this bound. For example, Fig. 6.3(a) and Fig. 6.3(b) highlight the time $T_{ctrl-load}$ in the two cases where the control signal is taken downstream of the high-side level shifter and directly from the PWM respectively.



(a)



(b)

Figure 6.3: OL Driving Chain Input Signal: (a) $v_{pwm}(t)$, (b) $v_{lvlshf}(t)$

Let us notice that in the first case the bound is not satisfied, and there is not enough time to process the signal in order to correctly drive M_8. Hence, in the implementation proposed in the following sections, the control signal will be taken directly from the PWM.

Now, since the inequality (6.1) stands, a delay cell has to be introduced in order to match the activation of M_8 with the current peaks injected by the load. For this reason, once T_{drv} has been estimated, it is possible to roughly get:

$$T_{delay} = T_{ctrl,load} - T_{drv}. \tag{6.2}$$

Fig. 6.4 furnishes a conceptual representation in the circuit of the just defined time intervals T_{drv}, $T_{ctrl,load}$ and T_{delay} and of the relation between them.

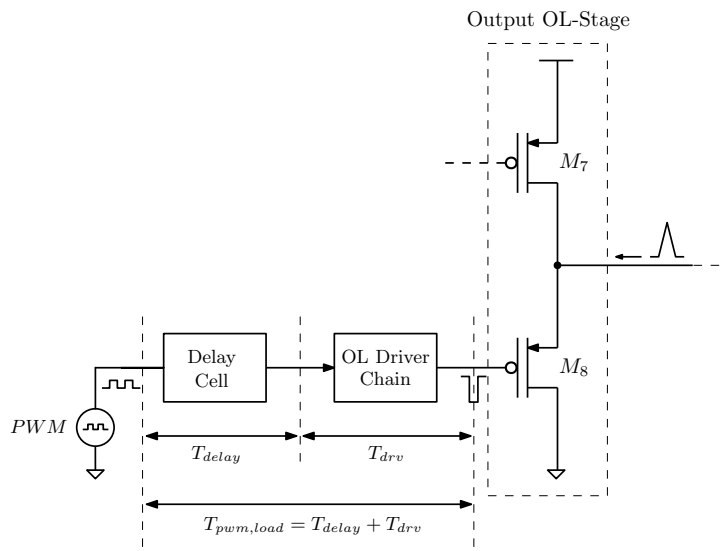


Figure 6.4: M_8Synchronization

6.2 Driving Chain

As mentioned, in order to get an appropriate driving of M_8 the input control signal $v_{pwm}(t)$ has to be taken, delayed of T_{delay} by a *delay cell*, and then processed by a circuit block that will be here referred to as *OL Driving Chain*. In particular, such a circuit block has to perform a sequence of three main operations in the input control signal in order to produce the desired driving signal $v_{drv,8}(t)$:

- Level shifting, to allocate the driving signal in the target voltage domain;
- Logic processing, to shape the driving signal in order to activate M_8 for the right time lapse, as shown in Fig. 6.1(b);
- Buffering, in order to make the driving signal "strong" enough to drive the large gate capacitance of M_8.

A block diagram representing the driving chain is sketched in Fig. 6.5, where the input $v_{pwm,d}(t)$ is a delayed version of the PWM signal $v_{pwm}(t)$.

6.2.1 Level Shifting

The input signal of the OL Driving Chain is the pwm signal, which is a periodic signal with period T_s, described by:

$$v_{pwm}(t) = \begin{cases} 1.5\ V, & \text{when } 0 \leq t \leq DT_s \\ 0\ V, & \text{when } DT_s \leq t \leq T_S \end{cases}$$

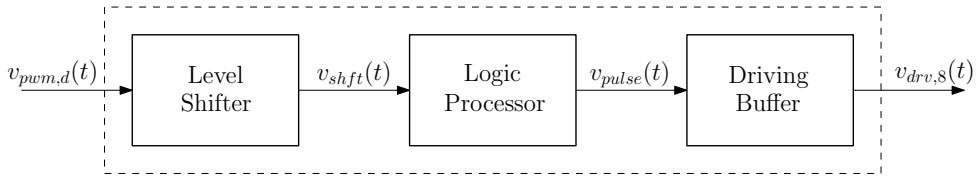


Figure 6.5: Driving Chain

Notice that it has a rectangular waveform with duty cycle D and whose low and high values are 0 V (ground) and 1.5 V respectively. Nonetheless, the transistor M_8 to be driven is a MV device and so it can sustain a gate-to-source voltage up to 2.5 V. Thus, ideally a driving signal with 2.5 V is desired. Since a constant 2.5 V is not available in the converter, it is convenient to exploit the high-side internal supply at 2.1 V instead. Hence the driving signal, for which a shape as represented in Fig. 6.1(b) is desired, should be allocated in the voltage domain between 0 V (low level) and 2.1 V (high level). To accomplish such a task, graphically represented in Fig. 6.6, a level shifter is employed.

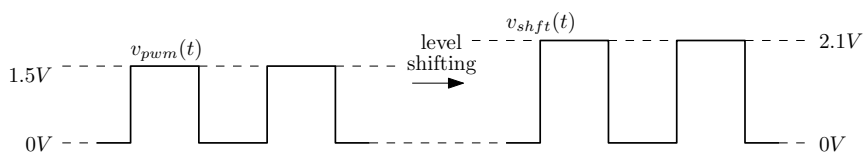


Figure 6.6: Level Shifting

The circuit scheme of the level shifter of the OL Driving Chain is represented in Fig. 6.7, while a simulation result featuring the signal at the input and at the output of the level shifter os shown in Fig. 6.8. Notice that this simulation is referred to a testbench for the driving chain where the 2.1 V constant level is delivered by an ideal generator, and not by the Internal Supply Generator in the Power Stage of the converter.

6.2.2 Logic Processing

After having moved the driving signal in target voltage domain, it is necessary to give it the desired shape, as shown in Fig. 6.9.

To reach this result, some steps has to be taken involving even logic operations. For this reason the circuit block dedicated to this task is here referred to as *Logic Processor*. Firstly, the signal $v_{shft}(t)$ at the output of the level shifter has to be delayed of a time interval t_{pulse} equal to the desired time lapse of the pulse of the target driving signal (such a time lapse should be approximately coincident with the time lapse of the load current peaks, and so about 200 ps). Then, this delayed signal $v_{shft,d}(t)$ has to be inverted. Finally, this inverted signal $\overline{v_{shft}(t)}$ has to be processed by a nand gate together with $v_{shft}(t)$. A

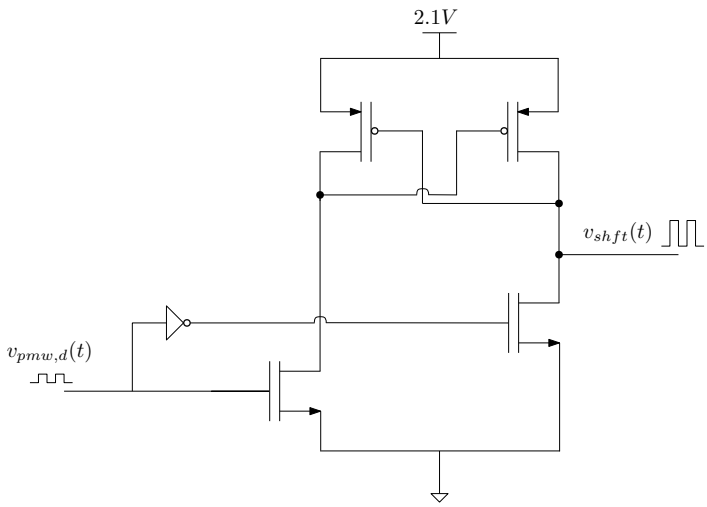


Figure 6.7: Level Shifter Circuit

schematic signal-representation of these steps is sketched in Fig. 6.10, while a logic scheme of the overall *Logic Processing* function is given in Fig. 6.11.

To conclude, a simulation result that represents the input and the output signals of this block is shown in Fig.6.12. In particular, the red curve represents the output signal $v_{pulse}(t)$. Notice that its shape is actually similar to the target one represented in Fig.6.9.

6.2.3 Buffering

The transistors at the output port of the nand gate employed in the Logic Processor have a width of 3 μm, while the transistor to drive, M_8, has a width of 3 mm, which is one thousand times superior. Thus, the gate of M_8 represents a huge capacitive load, impossible for the Logic Processor to drive. In fact, the too small transistors of the nand gate are not able to shape the target driving signal sinking and sourcing charge fast enough to discharge and charge the gate capacitance of M_8. In order to overcome this problem and to lower the charge and discharge time constant at the gate of M_8, a buffer circuit (a string of inverters) has to be inserted between the Logic Processing block and the capacitive load. Recall that something similar has been employed even to drive the power switches of the Commutation Cell in the Power Stage, as discussed in the Section 3.2. The conceptual scheme of a buffer circuit is sketched in Fig. 3.3.

When designing a buffer circuit there are two parameters particularly relevant to wisely consider: the number of inverter stages, N, and the aspect ratio between the transistors of an inverter and those of the previous one, A. In particular, the two parameter values have to be carefully selected in order to reach two desirable results:

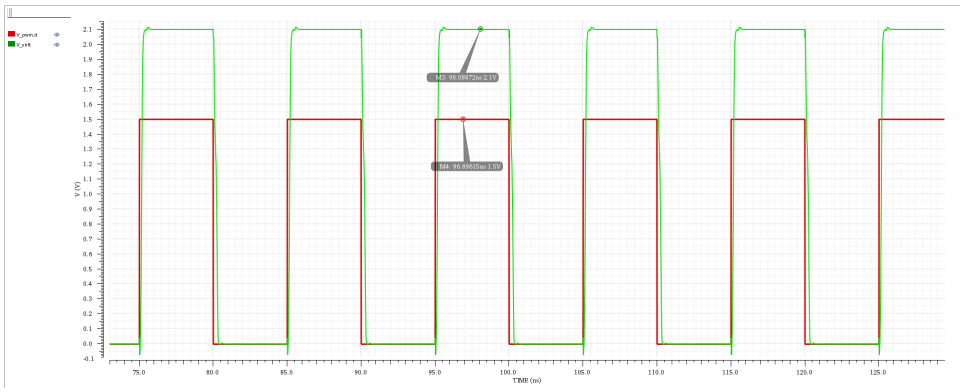


Figure 6.8: Level Shifting: Input-Output Transformation

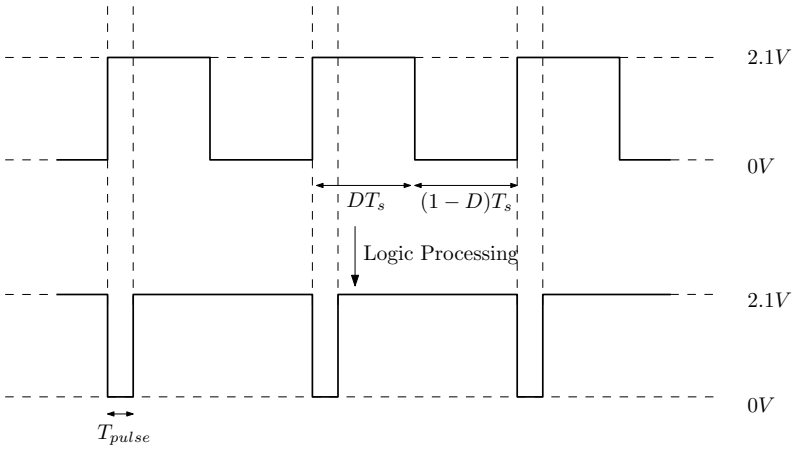


Figure 6.9: Shaping of the Driving Signal

- Reproducing correctly at the output the shape of the input signal. In fact, if the selected aspect ratio A is too large, one inverter stage may not be able to accurately reproduce at its output a steep edge present in the input signal. This leads to a distortion, eventually unacceptable, of the signal while propagating through the inverter stages.

- Minimize the propagation delay of the signal through the buffer. By selecting a small aspect ratio A it is possible to reduce the delay introduced by the single inverter stage. On the other hand, given a fixed capacitive load C_L to drive, selecting a small A requires to increase the number N of inverter stages needed, leading to an increasing of the propagation time. With the analysis carried out in [18] and in [4] it is possible to point out some formulas that allow to select A and N in order to minimize the overall propagation delay introduced by the buffer circuit. In particular we

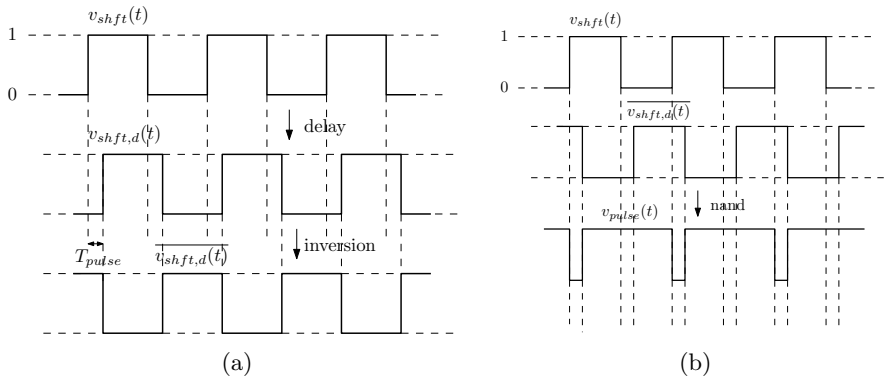


Figure 6.10: Logic Processing Steps

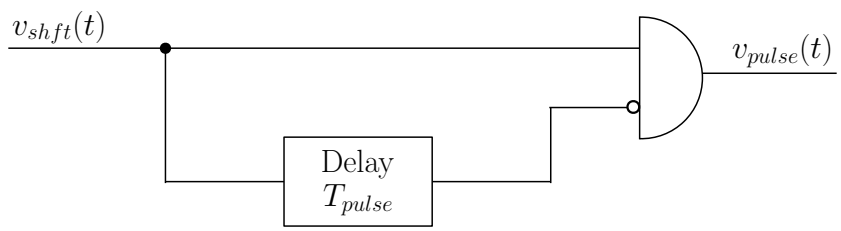


Figure 6.11: Logic Processing Logic Scheme

have:

$$N = \ln\left(\frac{C_{load}}{C_{in}}\right), \tag{6.3}$$

and

$$A = \left(\frac{C_{load}}{C_{in}}\right)^{\frac{1}{N}}, \tag{6.4}$$

where C_{in} represents the capacitance at the input node of the first inverter stage of the driving buffer.

Notice that in this application the propagation delay does not represent a problem as long as $T_{ctrl,load} > T_{drv}$. And since the buffer propagation delay is small compared to the difference $T_{ctrl,load} - T_{drv}$ we can conclude that minimizing it is not a requirement in this design. On the other hand, it is very important to design a buffer capable to reproduce accurately the input signal $v_{pulse}(t)$ which is not a trivial task to accomplish since the pulse to reproduce is very short ($\approx 200\ ps$) and the ratio $\frac{C_{load}}{C_{in}}$ is very large.

Let us now roughly estimate the ratio $\frac{C_{load}}{C_{in}}$ through a simple hand analysis. The transistors $M_{b,n1}$ and $M_{b,p1}$ of the first inverter of the buffer have a size similar to the transistor of the nand gate: $W_{b,n1} = 2\ \mu m$ and $W_{b,p1} = 5.4\ \mu m$. Instead, the transistor to be driven by the buffer is M_8, and its width is $W_8 = 3$

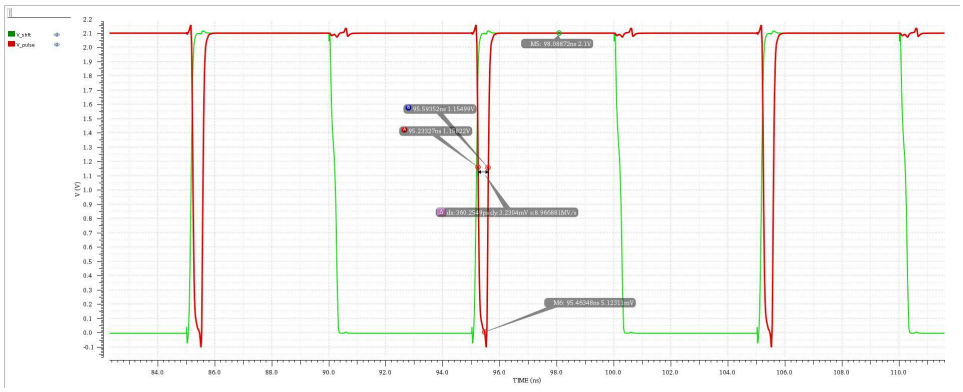


Figure 6.12: Level Processing: Input-Output Transformation

mm. In first approximation the gate capacitance of a MOSFET working in triode region, like $M_{b,n1}$ and $M_{b,p1}$ is given by:

$$C_{G,lin} \approx C_{ox} W L. \tag{6.5}$$

Hence, the C_{in} capacitance can be roughly quantified as:

$$C_{in} \approx C_{ox}(W_{b,n1} + W_{b,p1}) L_{min}. \tag{6.6}$$

Instead, the gate capacitance of a MOSFET operating in active zone, as M_8 when it turns on, can be roughly estimated as:

$$C_{G,act} \approx \frac{2}{3} C_{ox} W L. \tag{6.7}$$

Hence, the C_{load} capacitance can be roughly quantified as:

$$C_{load} \approx \frac{2}{3} C_{ox} W_8 L_{min}. \tag{6.8}$$

Therefore, since the transistors in the buffer and the OL-stage transistor M_8 are of the same kind, and since they both employ the minimum possible channel length (400 nm for MV devices realized with the available technology), we get:

$$\frac{C_{load}}{C_{in}} \approx \frac{W_8}{1.5 * (W_{b,n1} + W_{b,p1})} = 370 \tag{6.9}$$

Now, with (6.3) and (6.4) we obtain:

$$\begin{cases} N = 6 \\ A = 2.7. \end{cases}$$

Since simulations highlight that a driving buffer sized in such a way is not able to accurately reproduce the shape of the input signal $v_{pulse}(t)$, the final design

choice is:

$$N = 8,$$

And (6.4) gives:

$$A \approx 2.1.$$

Again, after observing the behavior obtained through simulations, it is appropriate to slightly adjust the value of the buffer aspect ratio A:

$$A = 1.9.$$

The structure of the driving buffer is sketched in Fig. 6.13, where the capacitances C_{in} and C_{load} and the roles of the parameter A and N have been pointed out.

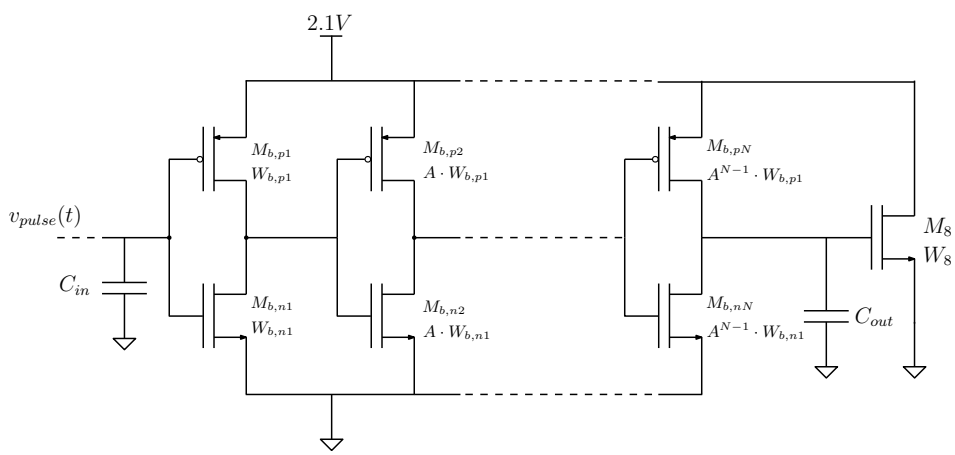


Figure 6.13: Driving Buffer Structure

Fig. 6.14 shows the signal delivered by the Logic Processor $v_{pulse}(t)$ and entering in the buffer (red curve) and the signal $v_{drv}(t)$ at the output of the buffer. Instead, Fig. 6.15 collects the M_8 driving signal after each of the processing steps in the OL Driving Chain.

6.2.4 Delay Cell

As discussed in the Section 6.1.1, the interval time from the rising edge of the PWM signal to the arriving of the consequent current peak injected by the load in the output rail of the Internal Supply Genertor, $T_{ctrl,load}$, is larger that the time employed by the OL Driving Chain to process the M_8 driving impulse, T_{drv}, according to (6.1). For this reason, in order to match the entering load current peaks with the activation of the OL-stage transistor M_8, it is necessary to introduce an appropriate time delay between the aforementioned rising edge and the start of the signal processing carried out by the OL Driving Chain:

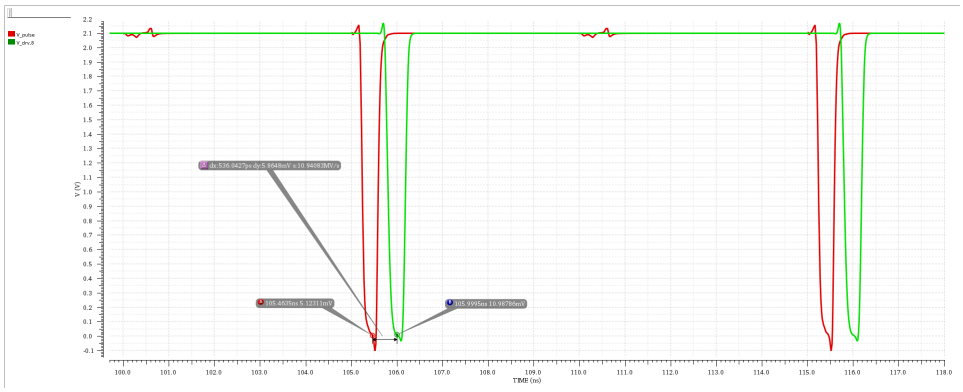


Figure 6.14: Driving Buffering: Input Output Transformation

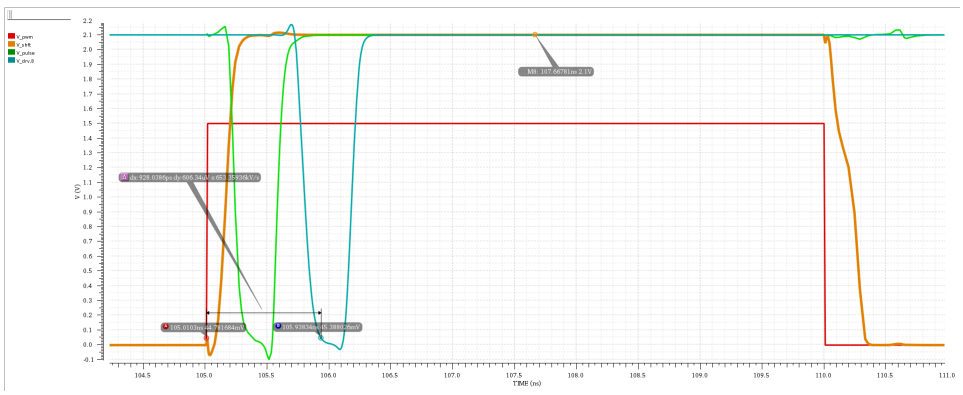


Figure 6.15: Signal Propagation through the Driving Chain

$$T_{delay} = T_{ctrl,load} – T_{drv}.$$

Fig. 6.15 highlights an estimation, based on simulation, of T_{drv}, while Fig. 6.3(a) highlights an estimation of $T_{ctrl,load}$. In such a way we get a first indication of the required delay time:

$$T_{delay} \approx 720ps.$$

This functionality is delegated to a specific *Delay Cell*, as sketched in Fig. 6.16.

Such a delay cell is once again obtained as a string of inverters. In this case the purpose of the cell is not to "enforce" its output signal, but rather to delay it of the given interval time T_{delay}. Therefore, there is no need to strive for minimizing the output delay or to appropriately select the best scale factor between an inverter stage and the following one. In particular, this Delay Cell has been obtained by connecting in series three equal modules, made with two

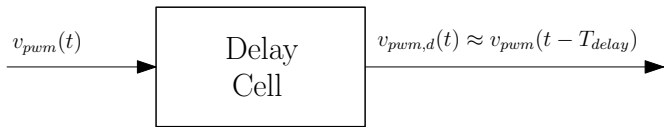


Figure 6.16: Delay Cell

inverters, each one introducing approximately 240 ps delay, as shown in Fig. 6.17. Instead, the circuit scheme of the delay cell is illustrated in Fig. 6.18.

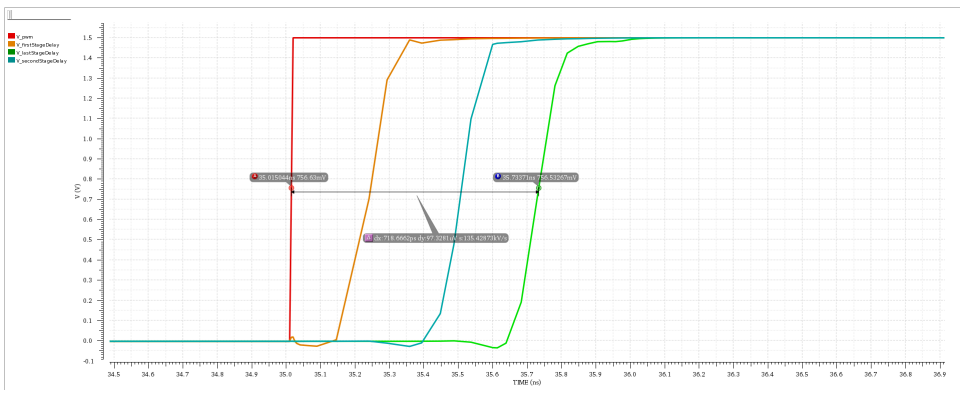


Figure 6.17: Delayed Input Signal

6.3 Simulation Results

Now some simulation results will be shown and commented. The purpose of these simulations is to compare the behavior exhibited by the Internal Supply Generator when it is implemented by the original design showed in Fig. 3.6 with respect to the case in which it is implemented by the new design. A similar comparison has already been carried out in Section 5.5, with an important difference: this time the chain driving the OL-stage transistor M_8 is not considered ideal like it has been done in the previous chapter, but it is realized like described in the previous section of this chapter, as sketched in Fig. 6.19.

Again, the behaviors of the two designs will be compared on the basis of the most relevant metrics for this circuit block: a voltage $\Delta v_{HS}(t)$ as close as possible to the constant value of 1.5 V is targeted, and the voltage stresses on the high-side driving chain of the Power Stage should be ideally kept under the nominal tolerance of 1.5 V, and anyway it should not exceed the SOA violation threshold of 1.66 V.

Notice that in this comparison a very large 300 pF integrated output capacitance has been used by the original design to produce and make more robust the high-side internal supply. Instead, in order to accord a significant saving in

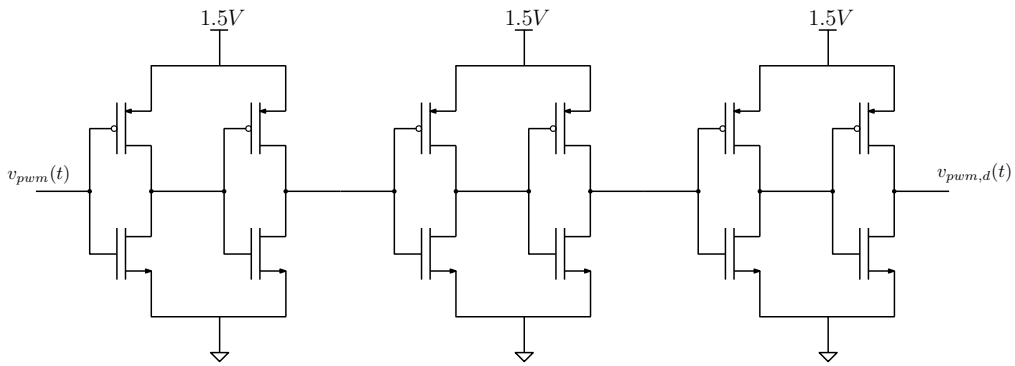


Figure 6.18: Delay Cell Structure

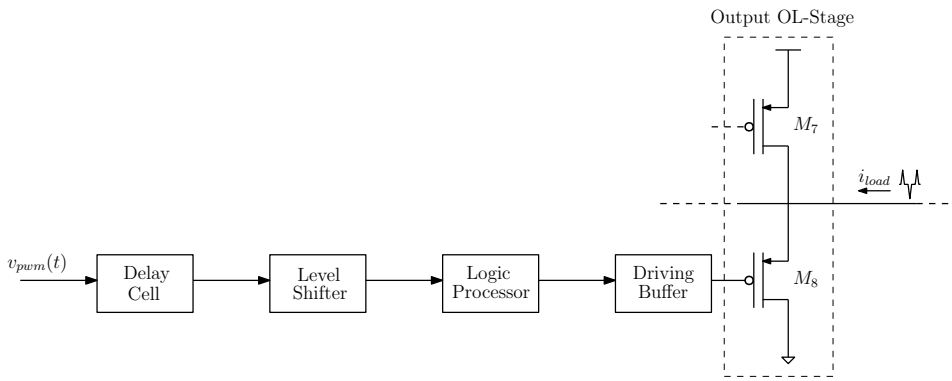


Figure 6.19: Real Driving of OL-Stage Transistors

area occupation, the new design employs a value of output capacitance reduced by 50 %, 150 pF.

6.3.1 Nominal Simulation Without Bonding Wires

The first important check is to verify that the OL Driving Chain developed in the previous section properly works even when inserted in the global system of the Power Stage of the converter. Fig. 6.20 shows, in the context of such a global situation, the propagation of the input signal $v_{pwm(t)}$ after each processing step along the OL Driving Chain. Let us notice that, with good approximation, the waveforms at the different nodes are the desired ones, and the overall behavior is in line with expectations.

Current Managing

Fig. 6.21 represents a current peak injected by the load in the high-side output rail of the Internal Supply Generator (red curve). It shows how it is managed

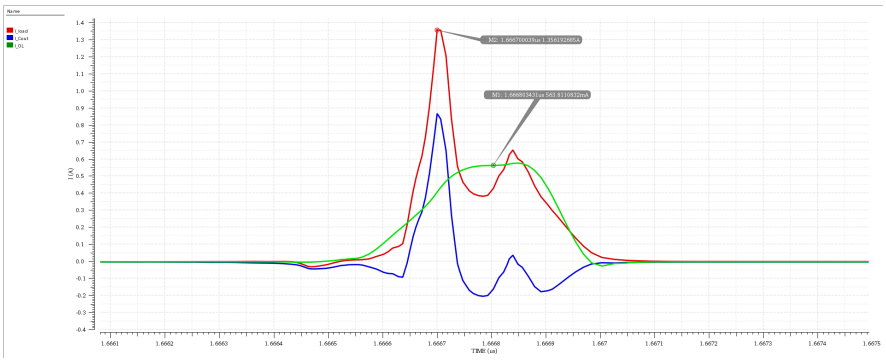


Figure 6.20: Propagation of the Driving Signal

by the OL-stage transistor M_8 (green curve), and by the output capacitor (blue curve). The first important observation is that actually, even with the real OL driving, the OL-stage transistor's activation is well synchronized with the arrival of the current peak. Moreover, it is possible to notice that its activation is substantial and covers the whole time lapse of the load peak, as desired. For this reason, the charge that actually enters in the output capacitor generating a voltage variation according to (3.1) is limited, and a significant improvement is expected in the output-port behavior with respect to the original Internal Supply Generator design.

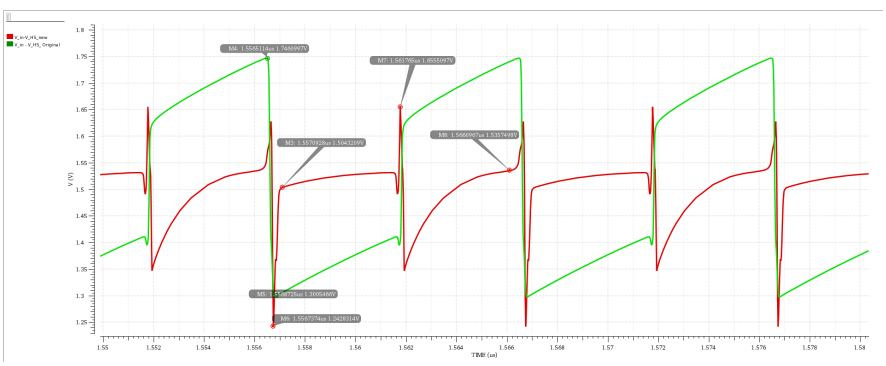


Figure 6.21: Current Management (No Bonding Wires)

Output Voltage

The output voltage $\Delta v_{HS}(t)$ imposed by the new internal generator is compared with that imposed by the original one in Fig.6.22. It is possible to notice that, despite the important reduction of 50 % in the output capacitance, the output behavior is still noticeably improved. In fact, with the new design, the voltage $\Delta v_{HS}(t)$ is much closer to the target constant 1.5 V for nearly the whole

switching period. In particular, with the new current management, the maximum voltage surge decreases from about 450 mV to about 300 mV. Let us even notice that, thanks to the CD and CS stages, after the surges the target output voltage is re-established much more effectively.

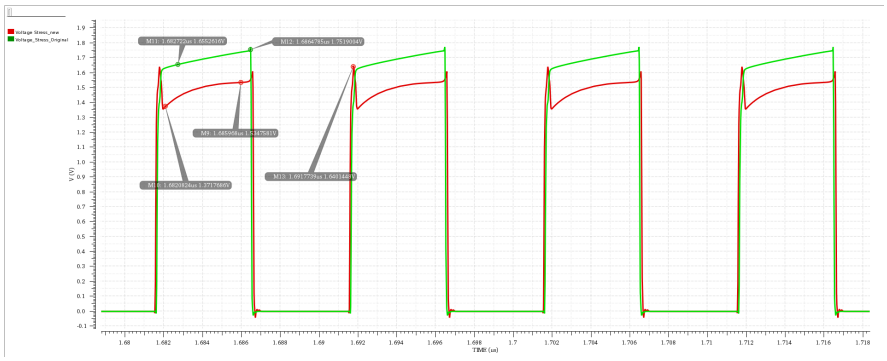


Figure 6.22: Output Voltage Comparison (No Bonding Wires)

Voltage Stresses

Finally, Fig. 6.23 features a comparison between the voltage stresses in the high-side driving chain of the Power Stage obtained with the two designs. Once again, the improvement reached by the new design is net: the stresses almost never reach the SOA violation threshold, while with the original design such a threshold is violated for a very significant portion of the switching period (about 33 % with a duty cycle of 0.5).

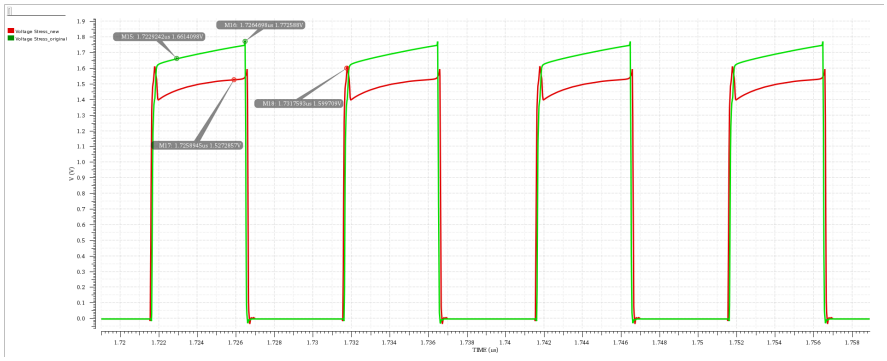


Figure 6.23: Voltage Stresses Comparison (No Bonding Wires)

The simulation results presented in the following sections take into account the parasitic effects introduced by the bonding wires that connect the Power Stage of the converter with the external supply, as discussed in Section 5.5.1.

Furthermore, the system will be tested and the comparison will be carried out in three different situations in order to assess the actual functioning of the circuit in a wide range of possible operation conditions:

- $T = 27\ °C$ and *nominal corner*;
- $T = -20\ °C$ and *fast corner*;
- $T = 150\ °C$ and *slow corner*;

where the different "corners" correspond to take in considerations that, once the circuit is physically realized, the parameters of the employed devices may differ from the nominal parameters of the respective model[14]. Thus, "fast" and "slow" corners allow to evaluate the behavior of the system when the models' parameters are at the two possible extremes of the possible range.

6.3.2 Nominal Simulation With Bonding Wires

The results presented in this section are referred to the operation of the system at the environmental temperature of 27 $°C$ and considering the nominal values of the models' parameters (e.g. nominal corner).

Current Management

Fig. 6.24 represents a current peak injected by the load in the high-side output rail of the Internal Supply Generator (red curve), and it shows how it is managed by the OL-stage transistor M_8 (green curve), and by the output capacitor (blue curve). It is possible to notice that, after the introduction of the bonding wires effects, the synchronization between the activation of the OL-stage transistor and the load disturbances is no more perfect. In particular, the transistor M_8 turns on slightly in advance. For this reason, after further observations, a re-design of the delay cell oriented to increase the introduced delay of a few tens of *ps* should be considered. Nevertheless, even if not optimized, there still is a significant contribution of the OL-stage transistor in the current management, and so an overall improvement in the output voltage is still expected.

Output Voltage

Fig. 6.25 compares, in the same conditions, the output voltage $\Delta v_{HS}(t)$ delivered by the Internal Supply Generator realized with the two different designs. It is possible to observe that, despite using a halved output capacitance, even after the realization of the OL Driving Chain, and even after considering the parasitic effects associated with the bonding wires, the new generator exhibits an improved behavior. In fact, for nearly the whole period, the voltage established at the output port is significantly closer to the target constant 1.5 V. It is still possible to observe, just in close proximity of the arrival of the load current peaks, that the new design output voltage experiments a slightly larger variation due to the aforementioned not perfect synchronization, relying on a significantly smaller output capacitance.

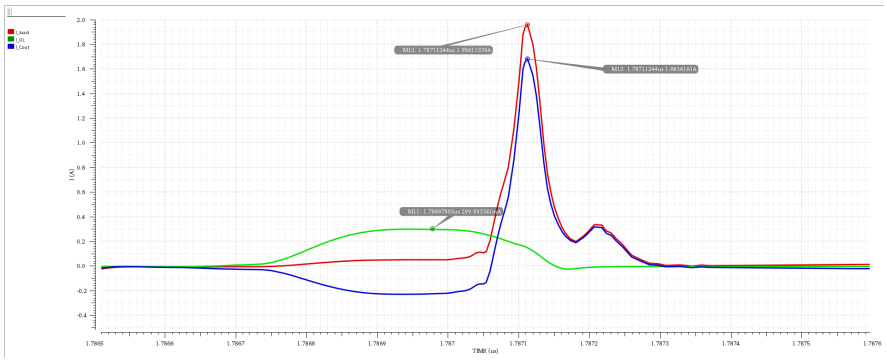


Figure 6.24: Current Management (Bonding Wires, Nominal)

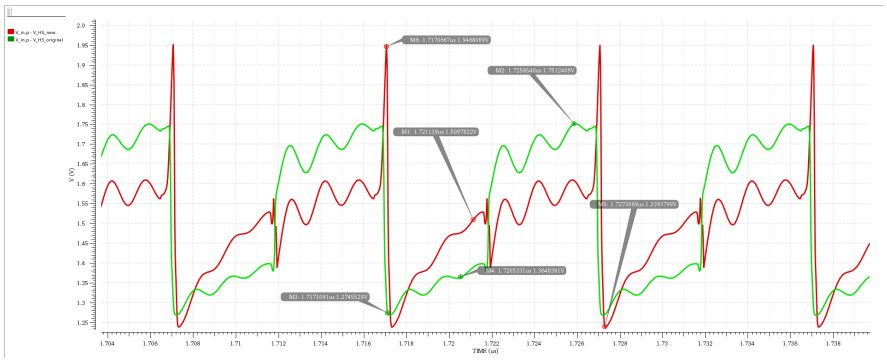


Figure 6.25: Output Voltage Comparison (Bonding Wires, Nominal)

Voltage Stresses

The improved output voltage delivered by the Internal Supply Generator realized with the new design translates into an improved voltage stress profile in the high-side driving chain as well, as shown in Fig.6.26. In fact, even after the introduction of the bonding wires, the voltage stressing the transistors of the tapered buffer stay still around 200 mV under the stresses observed with the original design. Nevertheless, after considering the bonding wires parasitic effects, such voltage stresses still slightly violate the SOA. However, the amplitudes and the time lapses of such violations are still much inferior than those produced by the original Internal Supply Generator.

6.3.3 Simulation with Bonding Wires: Fast Corner

The results presented in this paragraph are referred to the operation of the system working at the temperature of $-20\ °C$ and using a *fast corner* to set the models' parameters in the simulation.

Fig. 6.27 represents a current peak injected by the load in the high-side

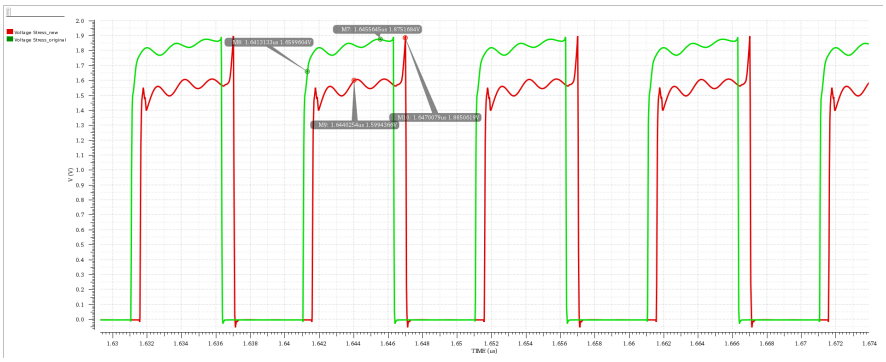


Figure 6.26: Voltage Stresses Comparison (Bonding Wires, Nominal)

output rail of the Internal Supply Generator (red curve), and it shows how it is managed by the OL-stage transistor M_8 (green curve), and by the output capacitor (blue curve).

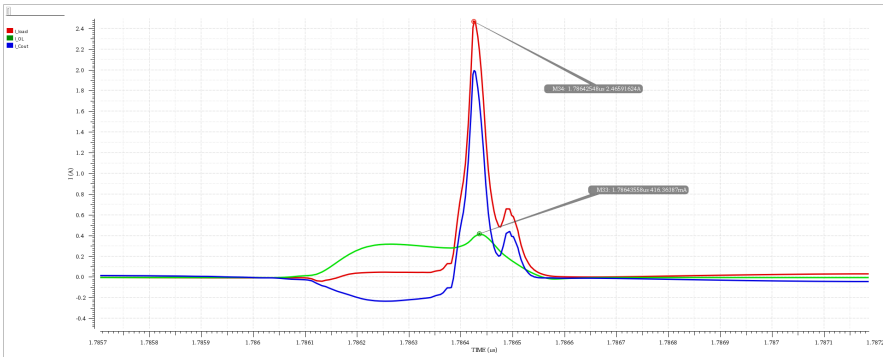


Figure 6.27: Current Management (Bonding Wires, Fast)

Again, even in these conditions the simulation highlights a not-perfect synchronization between the activation of the OL-stage transistor and the load disturbances. Similarly to what happened with the nominal corner, the transistor M_8 turns on slightly in advance. This observation enforces the need for a re-design of the delay cell oriented to increase the introduced delay of a few tens of ps. Nevertheless, even if not optimized, there still is a significant contribution of the OL-stage transistor in the current management, and so an overall improvement in the output voltage is still expected. In particular, Fig 6.28 shows a comparison between the output voltage $\Delta v_{HS}(t)$ delivered by the two different designs.

Even with fast corner and very low temperatures the new behavior is still globally improved, with some exceptions in the immediate proximity of the disturbances. Once again, this turns into an improved profile of the stresses in

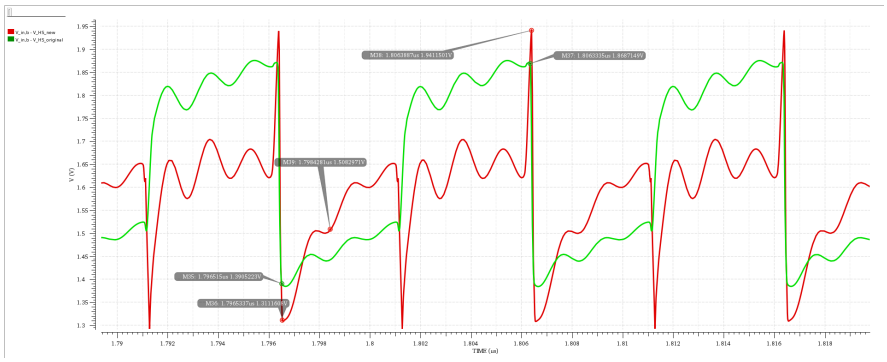


Figure 6.28: Output Voltage Comparison (Bonding Wires, Fast)

the high-side driving chain, as shown in Fig. 6.29. Such stresses approach the SOA violation limit of 1.66 V, but are still significantly lower (about 200 mV) of those experienced with the original design.

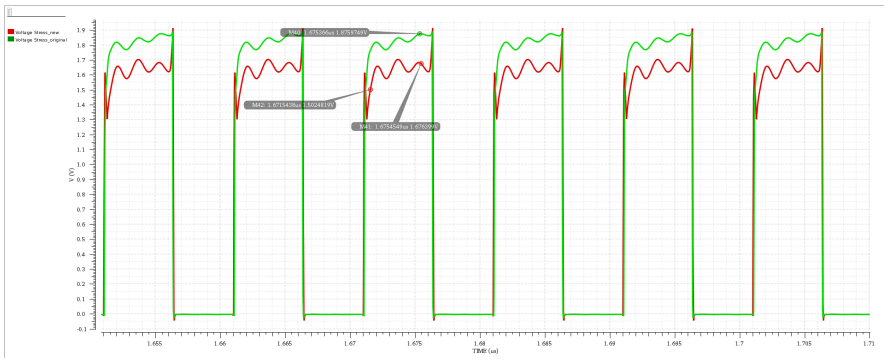


Figure 6.29: Voltage Stresses Comparison (Bonding Wires, Fast)

6.3.4 Simulation with Bonding Wires: Slow Corner

The results presented in this paragraph are referred to the operation of the system working at the temperature of 150 $°C$ and using a *slow corner* to set the models' parameters in the simulation.

Fig. 6.30 represents the OL-stage transistor's and the output capacitor's management of the current peak injected by the load in the high-side output rail of the Internal Supply Generator.

Let us notice that in these conditions there still is a partial synchronization between the OL-transistor's activation and the arrival of the load current peak but, as oppose to the previous cases, this time the activation occurs with a slight delay. For this reason, the idea of re-designing the *Delay Cell* in order to slightly increase the introduced delay would most likely degrade the performances at

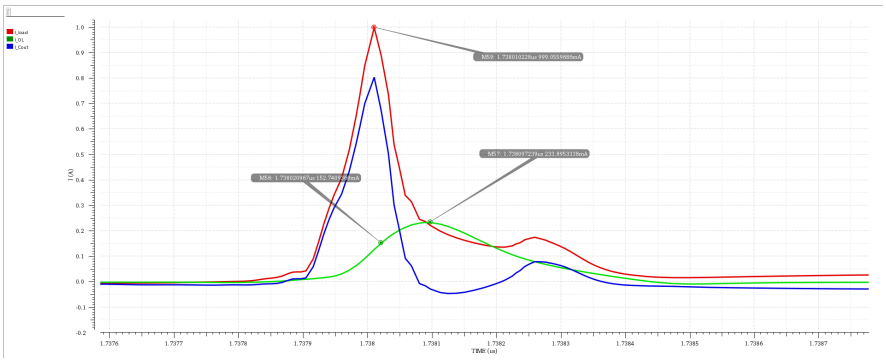


Figure 6.30: Current Management (Bonding Wires, Slow)

high temperatures with a slow corner. Fig 6.31 shows a comparison between the output voltage $\Delta v_{HS}(t)$ delivered by the two different designs. The behavior is comparable with the one offered by the original design, but recall that in the new one a halved output capacitance is being employed, still leading to significant save in area occupation. The voltage stresses in the high-side driving chain are in this case slightly larger for the new design case, but still always under the SOA violation threshold. In fact, it is possible to notice that, from this point of view, the high temperature and the *slow corner* lead to an improvement of the behavior showed by the original design.

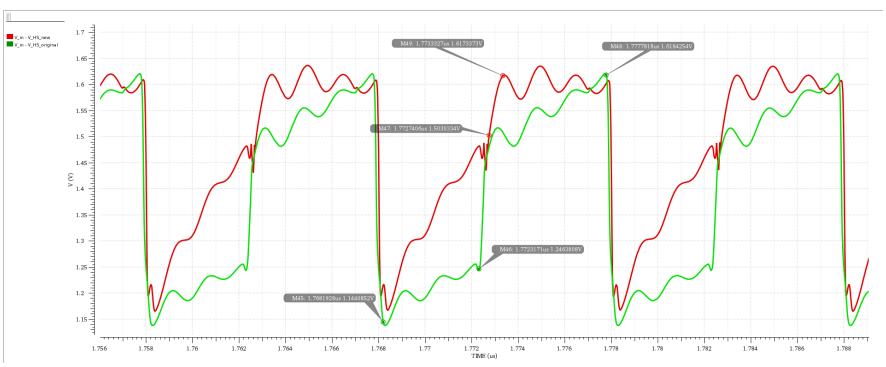


Figure 6.31: Output Voltage Comparison (Bonding Wires, Slow)

6.4 Efficiency Considerations

The input and output active powers have been assessed through the simulation tool in the several situations described, and then the energetic efficiency of the power stage has been calculated according to (2.1).

Table 6.1 shows a comparison between the energetic behavior obtained with

the new design of the Internal Supply Generator in two different cases: with the OL-stage transistor M_8 driving chain kept ideal, or realized as illustrated in this chapter.

	Ideal Driving	**Real Driving**
No Bonding Wires	76.24 %	76.23 %
With Bonding Wires	79.31 %	79.66 %

Table 6.1

The reported efficiency values show that there is no substantial difference between the two cases. This may be explained by noticing that, if in the second case the transistors in the driving chain dissipate energy, on the other hand the ideal driving of the first case leads to a more important activation of the large OL-stage transistor M_8, which actually results in a better behavior at the output port. Moreover, even with the ideal driving, a resistive effect associated with the ideal generator (1 Ω) has still been inserted in the simulated circuit, representing another source of energy loss.

Table 6.2 instead reports a comparison between the power stage energy efficiency achieved by employing the new design of the Internal Supply Generator with the real OL Drive Chain and by adopting the original version.

	Original	**New**
Normal, $T = 27°C$	79.66 %	86.88 %
Fast, $T = -20°C$	79.79 %	86.88 %
Slow, $T = 150°C$	72.60 %	86.88 %

Table 6.2

Notice that, again, a reduction of about 7 % is expected with the new design in nominal conditions. Something very similar is expected at low temperatures (-20 $°C$) and with a *Fast Corner*, while a further deterioration of efficiency is expected at high temperatures (150 $°C$) and with a *Slow Corner*, where an efficiency of 72.8 % is reached, 14 % less than the efficiency reached with the original design.

6.5 Final Considerations

In this chapter, a possible solution for the problem of appropriately driving the OL-stage transistors has been given and discussed. Since the high-amplitude current peaks injected by the load in the output rail of the Internal Supply Generator are very short in time (they last about 200 ps), the problem of synchronizing the turning on of the relatively large OL-stage transistors is particularly delicate. Nevertheless, such a synchronization has been reached, leading

to an overall improvement of the voltage established at the output port and of the voltage stresses in the high-side driving chain, even in the face of a sensible reduction (50 %) of the employed integrated capacitance which accord area saving. However, by testing the system operation over a wide range of temperatures and by considering the possible spread in the devices models parameters, it is possible to notice that, despite the synchronized activation of the OL-stage being able to accord an improvement of the behavior, this synchronization is no more perfect, sometimes leading to a significant reduction in the overall energy efficiency.

Chapter 7

Conclusions

This thesis, developed in collaboration with *Infineon® Technologies*, is inserted in the context of a new research line aimed at developing very high frequency dc-dc converters for automotive applications.

In general terms, the first problem to face consists in selecting a topology for the Commutation Cell of the power stage able to sustain the input voltages and the load currents typical of the target applications, and at the same time able to switch at a very high frequency (at least several tens of MHz) while still granting a good level of power efficiency. This step had already been accomplished in a previous stage of this research process, leading to the selection of a cascode topology. Then, a full buck converter had been developed, and a test-chip had been produced.

The main aim of this thesis, instead, was to analyze the already existing converter power stage, and to optimize the driving of the innovative cascode topology used to implement the commutation cell, making it more accurate and leading to area saving by reducing the overall integrated capacitance originally employed. In order to do this, the focus has been put in developing one of the functional blocks in the power stage of the converter, namely the *Internal Supply Generator*, which has the task of delivering an internal supply useful to appropriately shape the driving signal and to bias the cascode transistor in the power switch.

The design here developed and proposed, based on an improved rejection of the disturbances introduced by the switching activity of the Commutation Cell, actually allows to reach a more robust output behavior, delivering an internal supply globally closer to the target constant of 2.1 V. Contextually, even a better voltage stresses profile in the driving chain of the power switches has been reached, which represented a criticality with the original design since many SOA violations were reported during the operation of the power stage. Furthermore, this behavior is achieved still allowing a reduction of the capacitance integrated in the Internal Supply Generator up to 50 % (it has been decreased from 300 pF to 150 pF)

On the other hand, the solution proposed presents two main drawbacks.

Firstly, the design is based on the synchronization of the load disturbances with the activation of some MOSFETs. Since these disturbances consist in very short ($\approx 200\ ps$) and high-amplitude ($\approx 1.5\ A$) current peaks, such a synchronization is pretty delicate, and the solution obtained is not much robust with respect to temperature and models' parameters variations. Secondly, the activation of the aforementioned MOSFETs introduce some dissipative effects leading to a degradation of the power efficiency, which drops from about 86 % to about 79 %.

This work of thesis represented an opportunity to improve the understanding of this topic in view of further developments. In fact, the high-frequency dc-dc energy conversion is particularly attractive both for specific automotive applications, when it is up to supply devices that impose particular specifications to the supply system, and because it allows to reduce the size of the very bulky output filter passive components[3] resulting in an advantage in area saving and in the reduction of the chip cost.

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