Operation and Control Strategies of Solid State Transformer for a Stable MV-LV Interaction

Strategie di Funzionamento e Controllo di Trasformatori a Stato Solido per un interfacciamento stabile tra reti MT e BT

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Master Thesis

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Abstract

The electrical grid is facing a radical change, with renewable distributed generation(DG) as a central key. The future grid paradigm brings new challenges, such as low inertia grids operation and unpredictability of the generation. More and more generators and loads are interfaced to the grid through power electronics devices (PED), with the consequence that the physical inertia of the grid is going to decrease. In order to guarantee a stable and reliable grid operation, there is the need of defining a new set of devices that can contribute to the grid regulation. In order to be able to exploit all the generated power produced by intermittent DG, such as wind and photovoltaic (PV), the grid needs to have a buffer in terms of energy storage. Since most of the storage technologies are based on direct current (DC) technology it is expected the possibility to interface the storage to the grid directly in DC. The solid-state transformer (SST), also called smart transformer or electronic transformer in the literature is expected to play an essential role in the future grid. Unlike the traditional magnetic transformer, it provides accessible DC buses and can regulate the AC ports voltages independently. It can regulate the active and reactive power at the point of common coupling (PCC) without the need for flexible AC transmission systems. Furthermore, it can be controlled as a virtual synchronous machine (VSM) in such a way that the LV grid behaves, from the point of view of the MV grid, as a synchronous generator or motor.
This thesis aims to study a control framework based on the interconnection and damping assignment (IDA) passivity based control (PBC) and on the VSM theory for three single module topologies of SSTs. Both two-levels and three-levels topologies are considered. In particular a detailed comparison between single-phase, three-phase and three-phase neutral point clamped (NPC) DABs is done. The derived IDA-PBC and VSM controllers are implemented for each SST topology and finally simulated in Matlab Simulink.

Keywords: SST, Smart Grid, Energy, Virtual Inertia, Dual Active Bridge, Power electronics

Contents

1 Introduction

1.1 Motivation

The actual grid, based on a radial topology, is designed to transmit the power from big central generators one way to the peripheral nodes. The increasing penetration of small scale renewable energy plants, mostly connected through power electronic devices to the peripheral nodes of the grid, is going to change drastically the actual grid paradigm.

The passive low voltage grid is becoming more and more active, enhancing the vision of a microgrid based distribution grid. A microgrid is a portion of the grid able to generate locally its own power demand and to operate both in grid-connect and in island mode. The surplus power generated can be stored or transmitted to other portions of the grid. This would be efficient when many microgrids operate simultaneously to optimise the consumed and generated power, for example minimising the total cost or minimising the total carbon footprint. The better the microgrids are connected one with each other and the better optimised the power flow can be. Nowadays the LV grid is radial and that implies that to transmit a power flow from an LV feeder to another, the power should flow through a higher-level grid, causing the so-called reverse power flow, for which the actual grid is not designed for.

In order to be able to exploit all the generated power produced by intermittent DG, such as wind and photovoltaic (PV), the grid needs to have a buffer in terms of energy storage. Since most of the storage technologies are based on direct current (DC) technology it is expected the possibility to interface the storage to the grid directly in DC.

The fact that most of the DGs are interfaced through the grid with power electronic devices causes the physical inertia of the grid to decrease. Since the stability of the grid is strictly related to its inertia, alternative inertia providers have to be defined. A promising solution is virtual synchronous machines (VSMs) that can provide virtual inertia to the grid.

1.2 Solutions

The solid-state transformer (SST), also called smart transformer or electronic transformer in the literature is expected to play an essential role in the transition to a fully renewable-based grid. Unlike the traditional magnetic transformer, it provides accessible DC buses and it can regulate the AC ports voltages independently. The main application for the SST is to connect the medium voltage (MV) and the low

voltage (LV) grids. Solid State Transformer (SST) enables the integration of several novel features to the actual power grid, and it is a key element of the futuristic grid, envisioned in [1],[2].

The main features of the SST are the following:

- Frequency decoupling between the two ports: It permits to operate the medium voltage (MV) and low voltage (LV) grids with a different frequency, or, more realistically, with a different threshold for the frequency control.
- Accessible DC links: Enhance the possibility of connecting the energy storage without the need of a DC/AC converter and the development of DC lines that permit to mesh the low voltage grid at a lower cost [3].
- Bidirectional power flow: The direction of the current can be changed in very short time
- Independent voltage control on the two ports: the voltage on the MV side doesn't affect the voltage on the LV side, therefore both the voltages can be regulated independently.

It can regulate the active and reactive power at the point of common coupling (PCC) without the need for flexible AC transmission systems. Furthermore, it can be controlled as a virtual synchronous machine (VSM) in such a way that the LV grid behaves, from the MV grid, as a synchronous generator or motor, depending on the power flow direction.

1.3 Outline

Chapter 2

This chapter deals with the definition of basic concepts. Firstly the literature is reviewed, then fundamentals on the passivity based control (PBC) theory are presented and finally, some possible roses of the SST in the future grid are considered.

Chapter 3

In this chapter, the design of three SST topologies is presented. Power quality requirements are defined. Two-level and three-level dual active bride topologies are analysed and the DC bus ripple is derived in detail through switching function in order to properly design the DC side capacitor. The AC grid filter design is described in detail referring to the state of the art literature.

Chapter 4

This chapter is dedicated to the derivation of the Interconnection and Damping assignment (IDA) - PBC for all the converter constituting the SST. IDA-PBC is

applied for the first time to three-level neutral point clamped DAB. IDA-PBC is applied to grid forming and grid feeding converters as well as to the rectifiers.

Chapter 5

This chapter deals with the virtual synchronous machine (VSM) theory. A state of the art control approach is studied and presented.

Chapter 6

This chapter presents the simulations of the topologies and control approaches defined in chapter 3, chapter 4 and chapter 5. A comparison between the analysed topologies is performed. Three possible scenarios are presented, SST operated with LV grid off-nominal conditions, SST feeding constant power load (CPL) and SST supports the MV grid in terms of voltage and frequency regulation.

2 Basics

2.1 Solid State Transformer Concept

The Solid State Transformer is a three stages controllable power electronics device composed of a AC-DC converter, a DC-DC converter and a DC-AC converter, which connects two different voltage levels. The AC input voltage is firstly rectified, than it is converted to a desired level through a DC-DC converter and finally it is converted back to the desired AC voltage. The SST is a bidirectional converter, it can work in step-down mode when the power flows from the MV to the LV or in step-up mode to provide power to the MV grid. DC-DC converter topologies that have inherent valvanic isolation are best suited for SSTs. It provide an accessible DC bus that can be used to power a DC line or to host energy storage. The MV grid and the LV grid when connected through an SST are decoupled in sense of voltage and frequency. It means that a variation of frequency or voltage in one side is not reflected to the other.

The SST offers fast control of the output voltage and a bidirectional power flow, for this reason it is well suited for the smart grid applications.

2.2 Topology

One of the main challenges in the SST construction is how to connect it to the MV grid. Basically there are two different paths: the first is to use a multi-cellular topology based on modules of a fraction of the rated power that are connected in series at the input side, the second is to use single module topologies using high rated switching device. In this thesis the attention is mostly focus on the control of the SST, therefore a single module topology is selected to simplify the control implementation. Anyway the results of this thesis can be applied also to multi modular topology.

In Fig. 2.1 and in Fig. 2.2 an example of modular and single-module topology are presented.

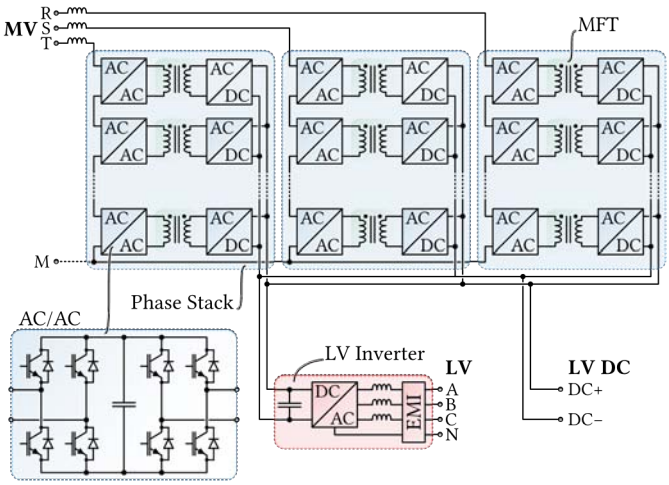


Figure 2.1: Multi-cellular based SST topology [4]

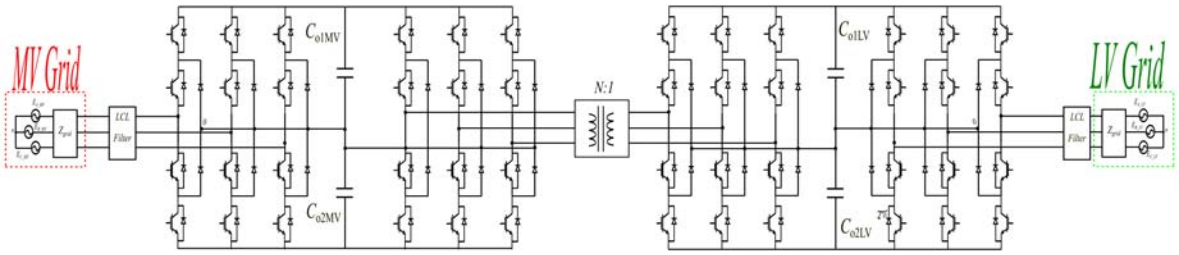


Figure 2.2: Single module SST topology based on three-level converters

For further reading about the topology refer to [5] [6] for single module and to [4] [7] for multi modular topologies.

2.3 Passivity Based Control

Passivity based control (PBC) was firstly introduced by Ortega and Spong [8] as a design methodology that achieves stabilization by controlling passivation. It can be applied only to Euler-Lagrange (EL) systems. The stabilization is achieved controlling the total energy of the system that can be seen as the difference between the stored and the supplied energy. The control works as an energy-balancing process that sets a minimum of the potential energy function in the desired equilibrium point. Since this control acts only on the potential energy it can not be applied to systems where the kinetic energy should be controlled, because in this case the closed-loop is no longer an EL system.

2.3.1 Port controlled hamiltonian

PBC can be extended to a broader class of systems by considering Port-controlled Hamiltonian (PCH). PCH results from the network modelling of lumped-parameter physical systems with independed storage elements. The system model takes the form of

$$\Sigma : \begin{cases} \dot{x} &= [J(x) - R(x)] \frac{dH}{dx}(x) + g(x)u \\ y &= g^T(x) \frac{dH}{dx}(x) \end{cases} \tag{2.1}$$

where $x \in \Re^n$ are the energy variables, the function

$$H(x) : \Re^n \to \Re \tag{2.2}$$

represents the total stored energy and $u, y \in \Re^m$ are the port power variables. The port power variables are conjugated, meaning that their product defines the power flow with the environment of the system. In the case of electrical circuits the port power variables are voltages and currents. The topology structure of the system is represented by the $n \times n$ skew-symmetric interconnection matrix $J(x) = -J^T(x)$ and by the $n \times m$ function $g(x)$. The matrix $R(x) = R^T(x) \geq 0$ is the dissipation matrix. By evaluating the energy rate of the system it is possible to obtain the following equation

$$\dot{H} = -\nabla H^T(x) R(x) \nabla H(x) + u^T y \tag{2.3}$$

stating that the difference between the output power and the dissipated power is equal to the total power. By integrating each component of eq. 2.3 results the energy-balance equation

$$\int_0^t u^T(s) y(s) ds = H\left[x(t)\right] - H[x(0)] + \int_0^t \left[\nabla H\left[x(s)\right]\right]^T R\left[x(s)\right] \nabla H\left[x(s)\right] ds \tag{2.4}$$

from which it is possible to see that for an uncontrolled system ($u(t) = 0$) the storage energy can not increase. Furthermore the stored energy would decrease with the presance of dissipation and reach a point where the energy is minimal. The aim of the PBC is to introduce a function that moves the open loop equilibrium point to the desired one x_*. In the next subsection the PBC with Interconnection damping assignment is presented.

2.3.2 IDA-PBC

The design of the controller is achieved with a minimization problem that can be solved with the Interconnection and Damping Assignment PBC (IDA-PBC) methodology, presented in this subsection. Firstly the damping and interconnection matrices are fixed in order to represent the internal energy exchanges of the analysed system. In the case of electrical circuits the interconnection and damping matrix represent respectively the Kirchoff laws and the resistive elements. Then a PDE system that represents all the possible energy function of the system is derived from

the PCH model. Finally the PDE is solved in order to select a function that satisfies the required minimum and the control is computed.

IDA-PBC is a methodology that has the objective to define a control function $u = \beta(x)$ such that the closed-loop dynamics is a PCH system with a dissipation function of the form

$$\dot{x} = [J_d(x) - R_d(x)] \nabla H_d(x) \tag{2.5}$$

where the closed loop energy function $H_d(x)$ has a local minimum at the desired equilibrium point x_* and $J_d(x) = -J_d^T(x)$, $R_d(x) = R_d^T(x) \geq 0$ represent the closed loop interconnection and damping matrices.
In the following proposition the design methodology proposed by Ortega [8] ortega is presented.

Given $J(x), R(X), H(x), g(x)$ and the desired equilibrium point $x_* \in \Re^n$. Assume we can find functions $\beta(x), J_a(x), R_a(x)$ and a vector function $K(x)$ that satisfy the matching equation

$$[(J(x) + J_a(x)) - (R(x) + R_a(x))] K(x) = -[J_a(x) - R_a(x)] \nabla H(x) + g(x) \tag{2.6}$$

and the following four conditions:

1. Structure preservation:

$$J_d(x) := J(x) + J_a(x) = [J(x) + J_a(x)] \tag{2.7}$$

$$R_d(x) := R(x) + R_a(x) = [R(x) + R_a(x)] \geq 0$$

(2.8)

2. Integrability: $K(x)$ is the gradient of a scalar function. Meaning

$$\nabla(x) = [\nabla(x)]^T \tag{2.9}$$

3. Equilibrium assignment: $K(x_*)$ verifies

$$K(x_*) = -\nabla H(x_*) \tag{2.10}$$

4. Lyapunov stability: The Jacobian of $K(x_*)$ satisfies the bound

$$\nabla K((x_*) > -\nabla^2(x_*) \tag{2.11}$$

Under these conditions, the closed loop system $u = \beta(x)$ will be a PCH system of the form 2.5 with

$$H_d(x) := H(x) + H_a(x) \tag{2.12}$$

and

$$\nabla(H_a(x)) = K(x). \tag{2.13}$$

In chapter 4 the IDA-PBC control approach is derived for the DAB1, the DAB3, the NPC-DAB, the grid forming LV-inverter, the grid feeding MV inverter and the rectifiers.

2.4 Roles of SST

In this section the roles that the SST could have in the future distribution grid are presented. The transition to renewable energies implies that the most part of the power sources are interfaced to the grid through a power electronic converter. The ancillary services that traditionally are provided by synchronous generators, as voltage and frequency control, shall find some substitute candidate. In particular there will be the need for devices that that could contribute to the voltage and frequency regulation. The SST, thanks to its multi stage topology and flexibility, is a good candidate for this purpose.

The services that can be offered by the SST to the grid are a key factor for its diffusion and success. The three stage topology of the SST provide many degrees of freedom in the operation of the device. The frequency and voltage of the MV and LV side can be regulated in an independent way. This permits many services to be handled at the same time, such as:

- Voltage and Frequency regulation on the MV side
- Load control in the LV grid
- Accessible DC link both at MV and LV levels (storage, DC feeder)

2.4.1 Frequency and voltage regulation

In the vision proposed by Zhong in [9] all the converters connected to the grid are controlled as a virtual synchronous machine (VSM), providing frequency and voltage support in terms of virtual inertia and reactive power. Having power electronics converters that act like a virtual synchronous machine can be positive for the system. Indeed the synchronous machine has a self stabilizing behaviour based on the swing equations that guaranties the stability of the converter with the grid. This approach, applied universally to all the devices, guarantees frequency and voltage stability following the concept of distributed generation and regulation.

The energy needed for providing virtual inertia is naturally stored in the power electronic devices as electromagnetic and electrostatic energy. If this energy is not sufficient a dedicated storage can be added to the DC link. In this case the storage is called power intensive, meaning that it has to supply a very high power for a short amount of time.

In the actual grid the voltage is regulated in basically three main ways:

- Generators side, by injection of reactive power,
- Load side, compensating the inductive reactive power of the load using capacitor banks, STATCOM and so on,
- In the transformation nodes, by modifying the transformation ratio of the transformers, on load or off load.

The latter one is not a proper solution, but just a palliative, because it takes the reactive power needed for the regulation from the upstream grid and therefore it gives the burden of the reactive power generation to the synchronous generators. In the case of an SST the regulation of the low voltage amplitude doesn't have an effect on the the MV side power factor because the reactive power is provided by the DC link capacitors. The solid state transformer can be seen as an OLTC operated in parallel with a Static Var Compensator. With the difference that the SST can change continuously the voltage and the reactive power, while the OLTC and the VSC have a step regulation.

The grid codes already incentives a distributed voltage regulation approach, mainly by means of capacitor banks on the load side, and set a limit on the lower admissible $cos\varphi$ of the load. A VSI can provide reactive power to the grid, like the already employed Static Synchronous Compensator (STATCOM). All the VSI can be controlled for providing voltage regulation.

In the normal operation of the SST the active power transfer is not affected by the VAR compensation. If the voltage regulation service is offered to the MV grid there will be a change in the apparent power of the MV converter but the LV one will not change, and also the contrary.

2.4.2 Reverse power flow

The increment of power generated in the LV grid cause that more and more often the instantaneous power injected is higher than the one consumed. In this condition the power flows from the LV to the MV grid causing the so called reverse power flow. This fact changes the paradigm of the actual distribution grid, where the voltage decreases when moving to the peripheral loads and introduce a new challenge for the voltage control, requiring a flexible regulation of the voltage at the nodes. The

solid state transformer, providing a controllable voltage level to the LV grid, can enhance a more efficient reverse power flow.

Sometimes a reverse power flow can be a problem and a strategy for avoiding it can be to store the extra power produced.[10] The SST, providing two accessible DC buses, can host energy storage that can work as a buffer between the MV and the LV grids.

3 SST Topologies: Design and Size

This chapter presents the design procedure of a 5MW solid state transformer (SST). The adopted switching frequencies are 1kHz for the DAB is 1kHz and 5kHz for the AC/DC, DC/AC converters. Three possible solutions are presented. The first is composed by two level AC-DC converters and by a single stage DAB (2L-1ϕ), the second differs from the first one due to the use of a three phase DAB (2L-3ϕ) and the third is based on the NPC topology, using three level NPC AC-DC converters and a three phase NPC DAB (3L-3ϕ).

The design of the SST transformer stages has to take in account the strong interconnection between all the dynamics of the system. In particular, the DC ripple on both the LV and the MV side have an impact on the AC grid voltage and current quality. Furthermore, the ripple on one DC bus is transmitted to the other by the high frequency transformer. For this reasons the design objectives are the following:

- Provide a stable DC bus voltage with a certain maximum voltage ripple
- Limit the total harmonic distortion (THD) injected in the AC grid to an acceptable level.

The power quality requirements are taken from the actual standards and are described in the next section.

3.1 Power quality requirements

3.1.1 AC power quality requirements

The standardization for the AC power quality is well defined. The total harmonic distortion limits for current and voltage can be found in IEEE [11]. The maximum THD indicated is of 5% for the voltage and of 5% for the current. Both measured at the common coupled point (PCC).

3.1.2 DC power quality requirements

The standardisation of terrestrial DC grids is ongoing. IEC sets a boundary between LVDC and MVDC at 1.5kV. What is important for the purpose of this work is to define a range of tolerance for the voltage variation of the DC links.

The topologies of SST proposed in this thesis offer a MV DC link of $30kV$ and a LV DC link of $\pm 400V$.

•	Max range	Min range
800 V	$+20\%, -40\%$	$\pm 10\%$

Table 3.1: Range of admitted voltage variations for the LV DC grids *as per* [12]

LVDC Link

A technology report from IEC [12] indicates the maximum and minimum proposed voltage variation range, showed in Tab.3.1. In order to be conservative and to be compliant with the most strict standard the design of the LVDC link capacitor will be done in order to achieve the minimum range fluctuations, i.e. $\pm 10\%$.

MVDC Link

MVDC micro grid are already used in electric ships. [13] indicates the main prescriptions for DC grids between 1 and 35 kV. The indicated voltage variation range in steady state is $\pm 3 - 5\%$.

3.2 Capacitor Design

In the SST the capacitor has to deal with switched currents both in the input and in the output. The aim of the design of the capacitor is to limit the voltage ripple in a tolerance zone that guarantees the proper operation of the device.In this section the approach to the design of the capacitors is discussed. The problem can be studied using the superposition principle, saying that the total effect of n sources on a linear circuit is equal to the sum of the contributions of each source. It is possible to say that the total voltage ripple is given by the sum of the ripple caused by the DAB and by the AC/DC Converter. By setting a peak value for the ripple of each converter a capacitor for both the ripple sources is designed. Finally, applying the superposition principle, it is possible to say that the total average ripple is given by the sum of the two ripples, when the capacitor size is chosen as the sum of the two.

In Fig.3.1 it is shown the DC bus circuit, where the two connected converters are modelled as current sources in terms of their harmonics.

In the following equations the DAB current and the DC/AC converter current are expressed in harmonic terms:

$$i_{DAB}(t) = I^0_{DAB} + i^1_{DAB}(t) + i^2_{DAB}(t) + ... + i^k_{DAB}(t) + ... + i^\infty_{DAB}(t) \tag{3.1}$$

$$i_{DC/AC}(t) = I^0_{DC/AC} + i^1_{DC/AC}(t) + i^2_{DC/AC}(t) + ... + i^k_{DC/AC}(t) + ... + i^\infty_{DC/AC}(t) \tag{3.2}$$

The apex number indicates the harmonic order. The k-th harmonic is defined as:

$$i^k(t) = \hat{I}^k \sin(k\omega t) \tag{3.3}$$

where $\hat{I}^k$ is the peak value of the k-th harmonic.

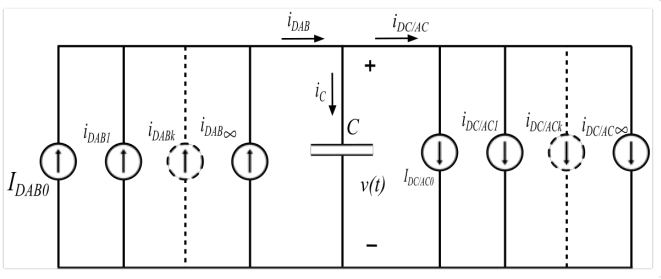


Figure 3.1: Schematic of the DC bus modelling the converters as current sources. Each converter current signal can be decomposed as the sum of its harmonics.

The superposition theorem can be applied by turning on one current generator per time, while all the others are substituted with an open circuit, and calculating the corresponding ripple on the capacitor voltage. The capacitor ripple caused from each harmonic is calculated as follows.

The Kirchoff current low applied to the DC bus node when just the k-th harmonic of the converter current is considered is:

$$C\frac{dv^k}{dt} = \hat{I}^k \sin(k\omega t) \tag{3.4}$$

The k-th harmonic ripple can be calculate as the sum of the integral of the capacitor voltage between the intervals $\left[0\ \frac{\pi}{4}\right]$ and $\left[\pi; \frac{3\pi}{4}\right]$. Since the sin function is symmetrical the same result can be found by taking two times the integral in the first interval, as follows:

$$\Delta v^k = 2\frac{\hat{I}^k}{C}\int_0^{\frac{1}{4kf_s}} \sin\left(k\omega_s t\right)\ \mathrm{d}t = 2\frac{\hat{I}^k}{2\pi f_s k C} \tag{3.5}$$

$$\Delta v^k = 2\frac{\hat{I}^k}{2\pi f_s k C} \tag{3.6}$$

where f_s is the switching equation of the converter (it may differ for the DAB and for the DC/AC converter), k is the harmonic order and $\hat{I}$ is the peak value of the sinusoidal harmonic signal. Repeating this procedure for each harmonic of the two converters and performing a summation of all the calculated voltage ripples brings to the total ripple on the DC bus. The current of the DC bus can be calculated in terms of its harmonics through the switching function of the converter. This is feasible for the DAB that has a relatively simple switching function, while is very tricky for the SVPWM controlled DC/AC converter. Therefore this method is applied to the DAB capacitor design, while for the DC/AC converter a DC capacitor design method from the literature [14] is adopted.

3.3 Converters Overview

In this section the converters adopted in this thesis for the design of the three topologies are presented.

3.3.1 MV Converter

The MV converter works both as rectifier and inverter depending on the power flow direction. It is connected to the grid through an LCL filter, which design is presented in chapter 3, and to the MV DC link. In this thesis two topologies for the MV converter are proposed: a two level and a three level neutral point clamped three phase converter.

Two level converter

The topology of the two level converter is shown in Fig. 3.2.

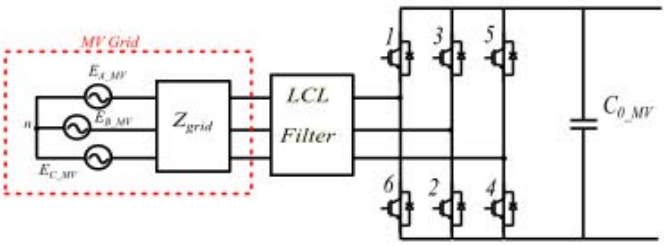


Figure 3.2: MV converter schematics

The relation between the grid line to line voltage and the dc bus voltage is expressed by eq. 3.7

$$V_{LL} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_{dc} \tag{3.7}$$

From it, by setting the desired nominal modulation index, the nominal MV dc bus voltage can be defined as

$$V_{MVdc} = \frac{2\sqrt{2}}{\sqrt{3}} \frac{V_{LL}}{m_a}. \tag{3.8}$$

Three level NPC converter

The neutral point clamped (NPC) three level converter was first introduced by [15] in 1981. The topology of the NPC converter is presented in Fig.3.3.

With this design the voltage applied on each power switching device is half respect to the one of conventional two level converter. It has lower line to line voltage steps and a higher number of steps in a carrier cycle, resulting in a lower ripple in the

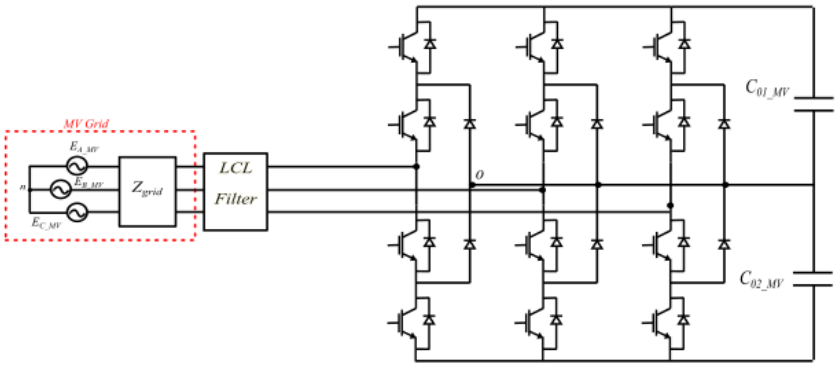


Figure 3.3: 3L NPC schematic

output voltage. Eq. 3.7 is valid also for this topology, since the DC bus voltage level is not affected by the converter type.

3.3.2 Dual Active Bridge

Dual Active Bridge was proposed in 1991 by [16]. It is a DC/DC bidirectional converter composed by two DC/AC converters connected through a medium frequency transformer. The power flow is controlled by phase shifting the secondary voltage wave form respect to the primary one. Depending on the power flow direction one of the two converters acts as inverter and the other as rectifier. The presence of the transformer provides a galvanic insulation between the primary and the secondary side of the DAB. In this thesis three different topologies for the DAB are considered .

Single Phase DAB

It is composed by two H-Bridges and a single phase transformer. The schematic of a DAB1 DC/DC converter is shown in Fig.3.4.

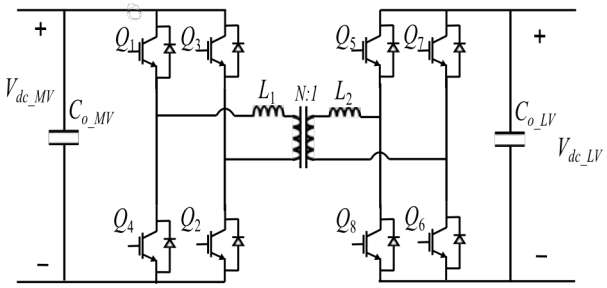


Figure 3.4: DAB1 schematics

The transformer voltage and current are shown in Fig.3.5. The duty cycle of the H-bridges is set to 0.5. The transformer voltage is a square wave and the current

has a trapezoidal shape.

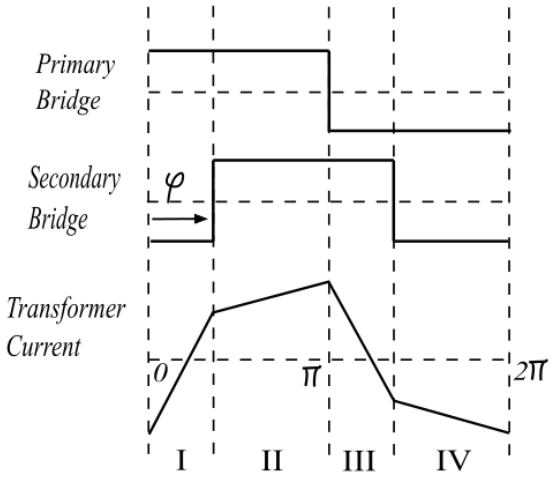


Figure 3.5: DAB1 bridge voltages and current

The power transferred by the DAB1 can be defined both from the DC output and from the AC side. In [16] it is used the first approach that leads to eq. 3.9.

$$P_t = \frac{V_{\text{in}}\, v\, \delta, \text{n}_\text{T}}{\omega L'} \left(1 - \frac{\delta}{\pi}\right) \tag{3.9}$$

The fundamental voltage on the primary and the secondary side written in time domain and referred to the primary are shown in eq. 3.10

$$\begin{aligned} V_{1n}(t) &= \frac{4V_{MVdc}}{\pi} sin(\omega_{sw} t), \\ V_{2n}(t) &= \frac{4V_{LVdc}}{\pi n_t} sin(\omega_{sw} t - \varphi). \end{aligned} \tag{3.10}$$

where φ, n_t are respectively the phase shift angle and the transformation ratio.

From eqs. 3.10 can be defined the RMS values that are respectively

$\overline{V}_{1n} = 2\sqrt{2}\frac{V_{MVdc}}{\pi}$ and $\overline{V}_{2n} = 2\sqrt{2}\frac{V_{LVdc}}{\pi}$.

Considering that in a transformer $r_t \ll L_t$ the following power flow equation can be written.

$$P_t = \frac{8V_{MVdc}V_{LVdc}}{\pi^2 n_t \omega_{sw} L_t} \sin(\varphi) \tag{3.11}$$

Equations 3.9 and 3.11 are slightly different because the first considers all the harmonics while the second considers only the fundamental harmonic of the voltage.

DAB3

The three phase DAB is composed by two three phase converters connected through a three phase transformer. The schematic of the DAB3 is shown in Fig.3.6

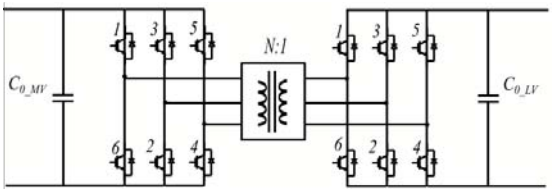


Figure 3.6: Three phase DAB schematics

As for the single phase DAB the primary and secondary three phase bridges are phase shifted by an angle φ in order to control the power.

In Fig 3.7 are shown the AC phase a primary and secondary voltages and the respective phase current. Both the voltages are referred to the primary side.

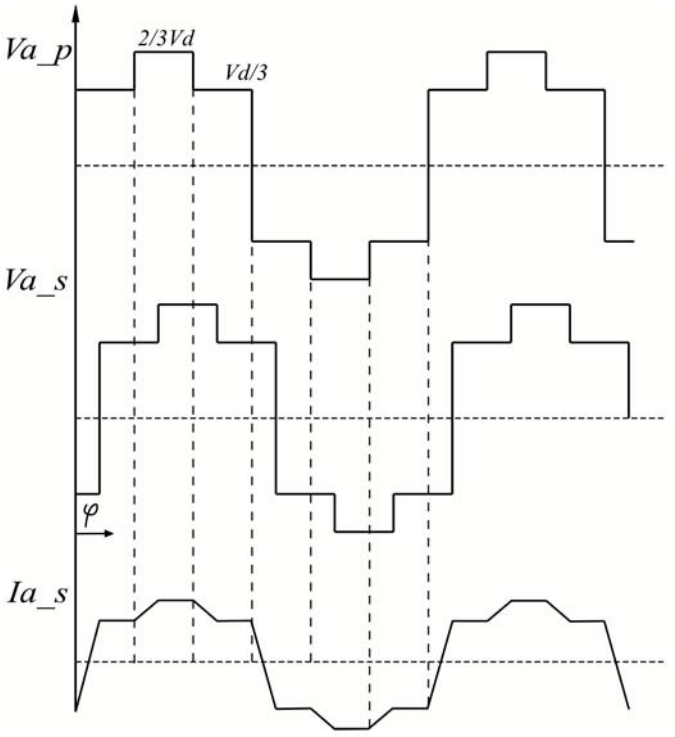


Figure 3.7: Three phase DAB phase voltages and current

The fundamental of the primary and of the secondary side voltage referred to the primary are expressed by

$$V_{1an}(t) = \frac{2V_{MVdc}}{\pi} sin(\omega_{sw} t)$$
$$V_{2an}(t) = \frac{2V_{LVdc}}{n_t \pi} sin(\omega_{sw} t - \varphi)$$

The active power results

$$P_t = \frac{6V_{MVdc}V_{LVdc}}{\pi^2 n_t \omega_{sw} L_t} sin(\varphi) \tag{3.12}$$

In [16] it is calculated the average output power shown in the following equation

$$P_t = \frac{V_{MVdc}V_{LVdc}\varphi}{\omega_{sw} n_t L_t} \left(\frac{2}{3} - \frac{\varphi}{2\pi} \right) \tag{3.13}$$

For the same reason explained the precedent subsection eqs. 3.12 and 3.53 are not perfectly equivalent.

DAB3 NPC

The neutral point clamped three phase DAB is composed by two NPC three phase converters operated with a fixed internal phase shift and controlled by PSM. This topology was first presented in [17]. In the same paper a solution for stabilizing the capacitors voltage is presented.

The topology of the DAB3 NPC is shown in Fig.3.8.

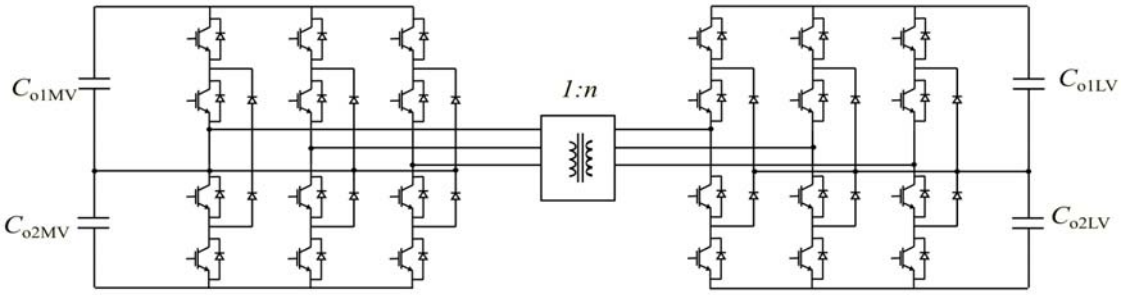


Figure 3.8: DAB3 NPC topology

In Fig. 3.10 are shown the voltages that characterize this topology. The internal phase shift of the NPC converter is a variable that acts on the phase angle between the external and internal switches of a leg. It modifies the shape of the voltage wave form affecting its THD.

Fig.3.9 shows the THD of the transformer current corresponding to the different internal phase shift values. As it can be seen the lowest THD is achieved with an internal phase shift $\phi_{int} = \frac{\pi}{6}$.

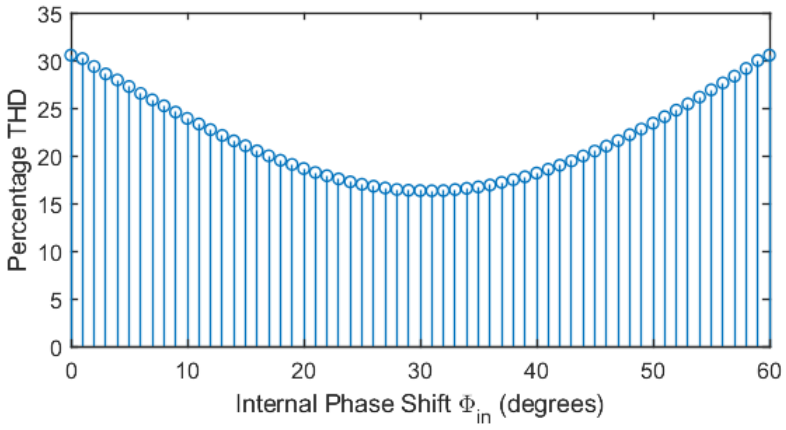


Figure 3.9: THD vs IPS

When the internal phase shift is set to zero, $\phi_{int} = 0$, the converter acts as a DAB3. Since the to upper and lower couple of switches are operated together and acts as a unique switch.

The waveforms of the primary bridge voltages are shown in Fig.3.10.

The switching function of the primary bridge phase to neutral voltage of the DAB3 NPC can be written as:

$$\langle V_{1,an} \rangle = \frac{V_1}{3\pi k} \sin\left(\frac{\pi k}{2}\right) \sin\left(\frac{\pi k}{6}\right) \sin\left(k\varphi_{in} + k\pi\right) - sin\left(k\varphi_{in}\right) + \jmath\left(\sin\frac{\pi k}{2} \sin\frac{\pi k}{6} \left(\cos\left(k\varphi_{in} + k\pi\right) - 1\right) - 1 - \cos\left(k\varphi_{in}\right)\right) \quad (3.14)$$

And the switching function of secondary side voltage when referred to primary side is

$$\langle V_{2,an} \rangle' = \frac{V_2}{3\pi k n_t} (\sin\left(\frac{\pi k}{2}\right) \sin\left(\frac{\pi k}{6}\right) \sin\left(k\varphi_{in} + k\pi\right) - sin\left(k\varphi_{in}\right) + \jmath\left(\sin\frac{\pi k}{2} \sin\frac{\pi k}{6} \left(\cos\left(k\varphi_{in} + k\pi\right) - 1\right) - 1 - \cos\left(k\varphi_{in}\right)\right) e^{-\jmath k\delta} \quad (3.15)$$

The average power transferred at 1st harmonic can be obtained by using k=1 in the above equations , and then taking RMS values of voltages in the power flow equation between two AC buses.

$$\langle V_{1,an} \rangle_1 = \frac{V_1}{3\pi} \left(\frac{1}{2} - \sin\left(\varphi_{in}\right) - sin\left(\varphi_{in}\right) + \jmath\left(\frac{1}{2}\left(-\cos\left(\varphi_{in}\right) - 1\right) - 1 - \cos\left(\varphi_{in}\right)\right) \quad (3.16)$$

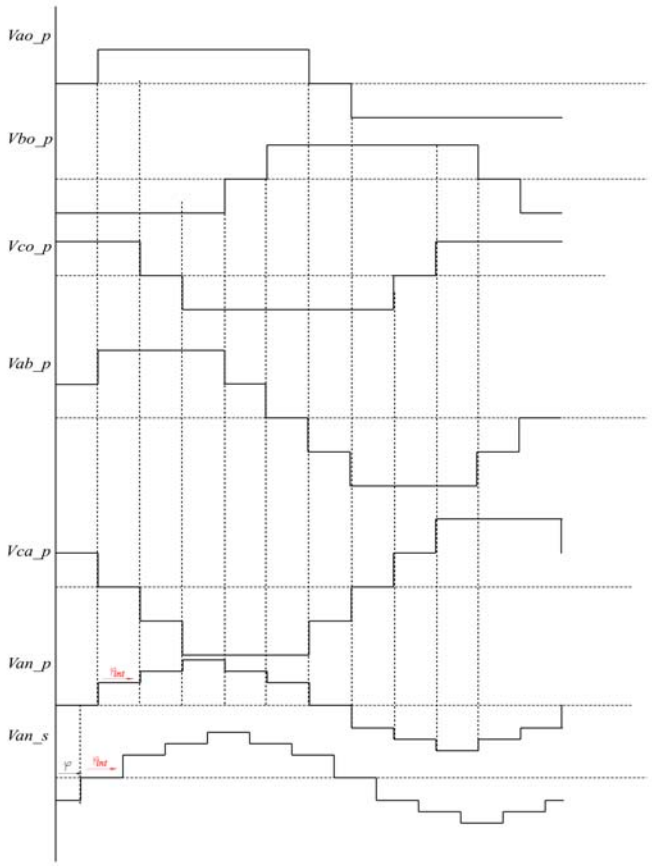


Figure 3.10: DAB3 NPC voltages. $\varphi_{int} = \frac{\pi}{6}$

Further reducing

$$\langle V_{1,an} \rangle_1 = \frac{-V_1}{2\pi} \left(\sin\left(\varphi_{in}\right) + \jmath \left(\cos\left(\varphi_{in}\right) + 1 \right) \right) \quad (3.17)$$

Converting eq.3.17 to time domain using inverse Fourier transform

$$V_{1,an}\left(t\right) = \langle V_{1,an} \rangle_1 e^{\jmath \omega_{sw} t} + \langle V_{1,an} \rangle_{-1} e^{-j\omega_{sw} t} \quad (3.18)$$

Peak value of the time domain signal can be written as,

$$\widehat{V}_{1,an} = 2|\langle V_{1,an} \rangle_1| = \frac{V_1}{\pi} \sqrt{2} \sqrt{1 + \cos\left(\varphi_{in}\right)} \quad (3.19)$$

RMS value of the signal is :

$$\overline{V}_{1,an} = \frac{V_1}{\pi}\sqrt{1+\cos\left(\varphi_{in}\right)} \tag{3.20}$$

Similarly the RMS value of secondary side voltage referred to primary side is:

$$\overline{V}'_{2,an} = \frac{V_2}{\pi n_t}\sqrt{1+\cos\left(\varphi_{in}\right)} \tag{3.21}$$

The secondary side and primary side are phase shifted by angle δ .
The average power flow is given by :

$$P_t = \frac{3\overline{V}_{1,an}\overline{V}'_{2,an}}{\omega_{sw}L_t}\sin\delta \tag{3.22}$$

Using the expressions of RMS voltages in the above expression, we get the power flow of the 3L-NPC-DAB in terms of the DC voltages.

$$P_t = \frac{3V_1V_2.\left(1+\cos\left(\varphi_{in}\right)\right)}{\pi^2 n_t\omega_{sw}L_t}\sin\delta \tag{3.23}$$

By using Bhaskara I sine approximation formula, sine function can be written down as a second order quadratic function:

$$\sin\delta = \frac{16\delta\left(\pi-\delta\right)}{5\pi^2-4\delta\left(\pi-\delta\right)} \tag{3.24}$$

Using the above approximation, power transferred can be approximated to:

$$P_t = \frac{48V_1V_2.\left(1+\cos\left(\varphi_{in}\right)\right)}{\pi^2 n_t\omega_{sw}L_t}\frac{\delta\left(\pi-\delta\right)}{5\pi^2-4\delta\left(\pi-\delta\right)} \tag{3.25}$$

3.3.3 LV Converter

For the low voltage converter are adopted the same topologies of the MV converter, therefore a two level and a three level NPC converters.

In Fig.3.11 are shown the two topologies.
The LV grid has a line to line voltage of 400V. By applying eq. 3.26 and setting the desired modulation factor can be defined the LV DC link voltage.

$$V_{LVdc} = \frac{2\sqrt{2}}{\sqrt{3}}\frac{V_{LL}}{m_a} \tag{3.26}$$

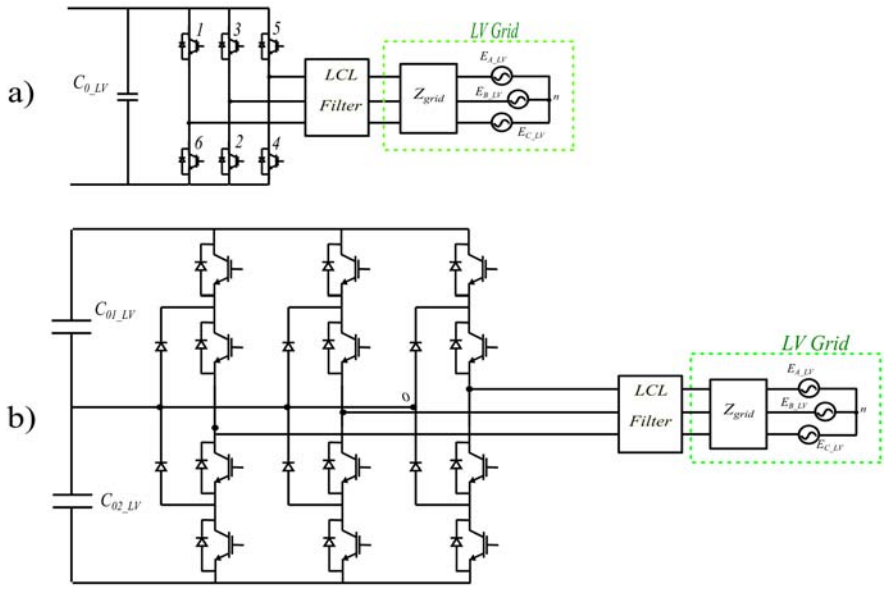


Figure 3.11: a) Two level converter topology b) Three level NPC topology

3.4 $T_1 \rightarrow 2L - 1\phi$

In this section the first topology composed of 2-Level AC/DC, DC/AC converters and single phase DAB is presented

This section is organised as follows:

- The low voltage AC/DC converter AC side filter and DC side filter are designed
- The DAB1 leakage inductance and DC capacitor are designed
- The medium voltage AC/DC converter AC side filter and DC side filter are designed

3.4.1 LV Conversion Stage

The low voltage converter is a three phase switching device. It has the DC bus connected to the LV side of the dab. The two converters are coupled by a capacitor. It has the AC side connected to the LV grid through an LCL filter.

3.4.2 LCL filter design

In order to limit the harmonics injected to the LV grid it is used an LCL filter. LCL filters are high-order filters widely used to interconnect power electronic converters to the grid. Usually a damping resistor is put in series with the capacitor in order to reduce the circulation of resonant currents in the filter. In order to reduce the

damping losses it can be employed a shunt damping resistance R_c in series with a capacitor C_d. This solution offer also the advantage of increasing the high-frequencies attenuation of the filter. [18]

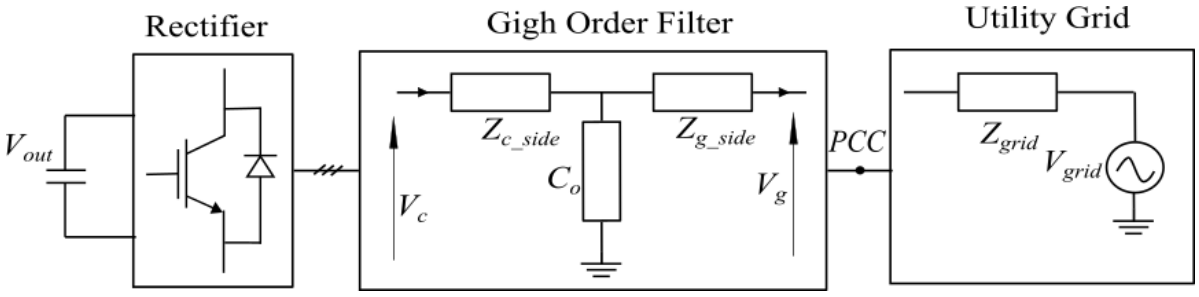


Figure 3.12: LCL Filter scheme

The design of the filter is based on the paper [18]. The schematic of the high-order filter used is shown in Fig.**??**. The corresponding state space model is expressed in equation 3.27.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = -\begin{bmatrix} Y_{11} \\ Y_{21} \end{bmatrix} V_1 - \begin{bmatrix} Y_{12} \\ Y_{22} \end{bmatrix} V_2 \tag{3.27}$$

Where the output variable is the grid side current i_2. The transfer function of the forward transadmittance (mutual admittance) is shown in eq.3.28 for the general case and in eq.3.30 for the LCL filter, where $Y_o = \frac{1}{s(L_1+L_2)}$.

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = \frac{Z_{3f}}{Z_{1f}Z_2 + Z_{1f}Z_{3f} + Z_2Z_{3f}} \tag{3.28}$$

$$Y_{21(LCL)}(s) = \left.\frac{I_2(s)}{V_1(s)}\right|_{V_2=0} = Y_0 \frac{1}{\frac{s^2}{\omega_0^2} + 1} \tag{3.29}$$

$$Y_{21(LCL)}(s) = Y_\infty \frac{1}{\frac{\omega_0^2}{s^2} + 1}. \tag{3.30}$$

As said before a shunt damping resistance R_d in series with a capacitor C_d is employed. In this way the damping is more selective, acting only around the resonance frequency of the filter and resulting to be more effective. Furthermore adding a series resistor in the LCL filter reduce of $20\frac{dB}{decade}$ the attenuation slope at high frequencies, while adding a shunt damping resistor only shift the attenuation slope of a factor $\frac{1}{n+1}$, where n is the number of the shunt damping branches. This kind of damping present a design problem regarding how the filter capacitance should be split between the two capacitors. For the shunt damping LCL filter the transadmittance becomes equation3.31

$$Y_{21(LCL+RC)} = Y_0 \frac{\frac{nQ}{n+1}\frac{s}{\omega_0} + 1}{\frac{nQs^3}{(n+1)^2\omega_0^3} + \frac{s^2}{\omega_0^2} + \frac{nQ}{n+1}\frac{s}{\omega_0} + 1} \tag{3.31}$$

where $Q = \frac{R_d}{R_o}$ is the quality factor. $R_o = \sqrt{\frac{L_{eq}}{C_o}}$ is the characteristic impedance of the filter.

The proper design of the filter is done in the following points:

1. The first step is to calculate the ripple of current from which can be calculated the converter side inductance. Assuming an unity power factor the current at nominal power can be determined from eq.3.32

$$I_{L1(rms)max} = \frac{S_{base}}{\frac{3V_{llMV}cos\phi}{\sqrt{3}}} \tag{3.32}$$

   Assuming a current ripple of 15% it results eq.3.33

$$\Delta I_1 = 10\% I_{1rmsmax} \tag{3.33}$$

   from which is possible to determine the peak output current of the converter, eq.3.34

$$\widehat{I}_{L1} = \sqrt{2} I_{L1(rms)max} + \Delta I_1 \tag{3.34}$$

   From eq.3.33 can be calculated L_1. Defining the base impedance of the converter $z_b = \frac{V_{ll}}{S_{base}}$ the inductance L_1 is expressed in percentage respect to z_b.

2. The total filter capacitance is designed to be 15% of the base capacitance, defined as $C_b = \frac{1}{\omega z_b}$. Therefore

$$C_o = \frac{15}{100} C_b \tag{3.35}$$

3. The grid inductance L_2 is defined imposing that the total percentage inductance $L_{1(\%)} + L_{2(\%)} \leq C_{o\%}$. The value of L_2 is chosen in order to move the resonance frequency to a value that is sufficiently far away both from the switching and the grid frequencies. In Fig.3.13 it is shown the Bode plot of both the LCL and the LCL with shunt damping.

4. The damping resistance is defined starting from the characteristic impedance of the filter, considered fully resistive, and multiplying it for the quality factor.

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2}$$

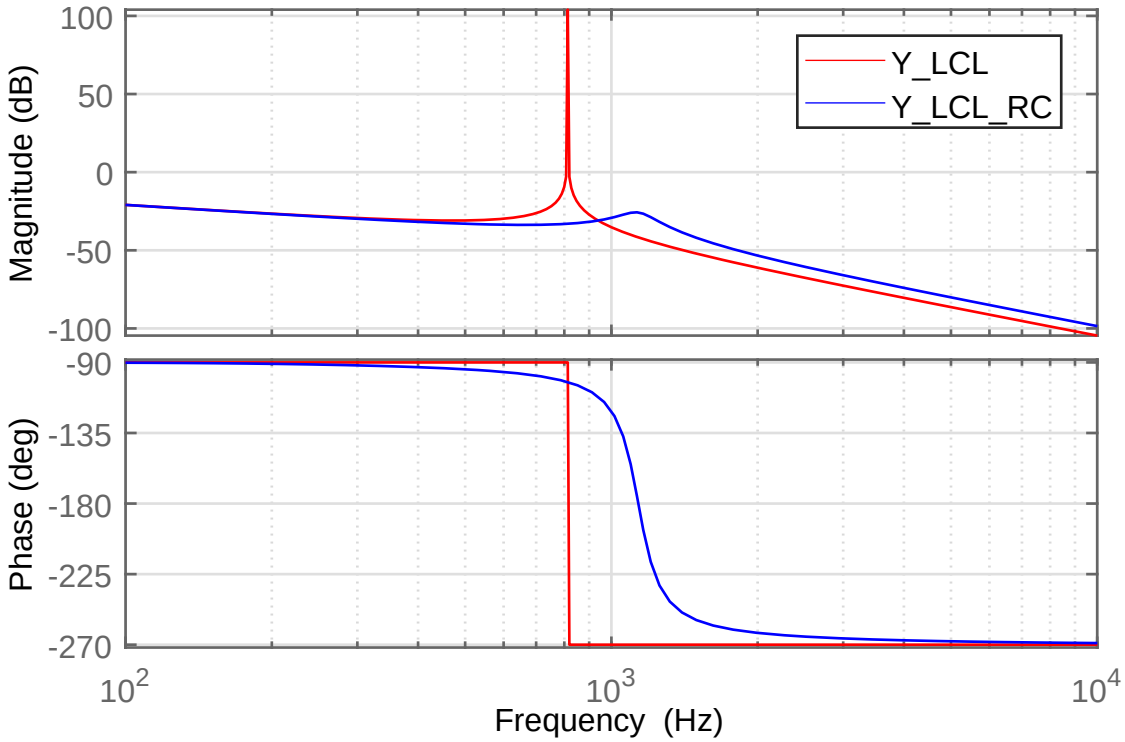


Figure 3.13: bodeplot of the MV LCL filter

(3.36)

$$Z_o = R_o = \sqrt{\frac{L_{eq}}{C_o}} \tag{3.37}$$

$$R_d = R_0 Q \tag{3.38}$$

5. The total filter capacitance is split between the two capacitors in equal parts.

$$C_f = C_d = \frac{C_o}{2} \tag{3.39}$$

3.4.3 LV AC/DC Converter Capacitor design

The design of the AC/DC converter capacitor is done accordingly to the approach proposed in [14]. In a three phase converter operating in steady state and with a balanced load, the current $i\,(t)$ on the DC link is composed only of two terms

$$i(t) = I_{dc} + \Delta i(t) \tag{3.40}$$

where I_{dc} is the direct current component and $\Delta i(t)$ is the is the current associated to the switching frequency. It is worth to note that in the case of unbalanced load there is also an alternating second fundamental frequency harmonic term. It is assumed that all the ripple current $\Delta i(t)$ is absorbed by the capacitor. Therefore the peak to peak variation of the dc voltage can be expressed as

$$\Delta v_{pp} = \left| \frac{1}{C} \int_0^{t_{pp}} \Delta i dt \right| \tag{3.41}$$

where t_{pp} is a specific time interval during which the capacitor get the maximum voltage variation. Considering the SVPWM switching function and the corresponding currents and applying equation 3.41, the maximum voltage variation results

$$\Delta v_{pp} = \frac{I_o T_s}{C} r_{pp}(m, \vartheta, \varphi) \tag{3.42}$$

where $r_{pp}(m, \vartheta, \varphi)$ represents the normalized maximum peak to peak ripple in function of the modulation index, the grid phase angle φ and the SVPWM reference angle ϑ.

Considering $\varphi = 0$ it can be found out that the normalized maximum peak to peak ripple $r_{pp}^{max} \approx \frac{1}{8}$, from which it is possible to determine the actual peak to peak dc-link voltage ripple amplitude

$$r_{pp}^{\max} \approx \frac{1}{8} \rightarrow \tilde{v}_{pp}^{\max} = \frac{1}{8} \frac{I_o T_s}{C} \tag{3.43}$$

.

Once the maximum voltage ripple $v_{pp}^{\max}$ is assigned, the corresponding capacitance C_{conv} can be calculated as

$$C_{conv} = \frac{1}{8 f_s} \frac{I_o}{\tilde{v}_{pp}^{\max}} \tag{3.44}$$

where $f_s = \frac{1}{T_s}$ is the switching frequency.

As explained the total DC bus ripple is given by the sum of the ripples produced by the AC/DC converter and by the DAB. It is assumed that each of the two converters is responsible for half of the ripple. The maximum ripple at full load is $\pm 10\%$ meaning a peak to peak value of 160V.
Therefore the AC/DC capacitor is designed in order to achieve a DC voltage ripple with a peak to peak value of 80V.

The capacitor size results $C_{0AC/DCLV} = 2.3mF$.

3.4.4 DC-DC Conversion stage

The design of the DAB consists mainly in the design of the leakage inductance and of the LV and MV capacitors.

Leakage inductance design

The leakage inductance value has a vital role in the power transfer of the DAB. It can be calculated from the power equation once the phase shift angle at nominal power is defined.

Eq. 3.45 describes the average power output of the DAB1, without considering the losses in the inner circuit and the power transferred through inner harmonics.

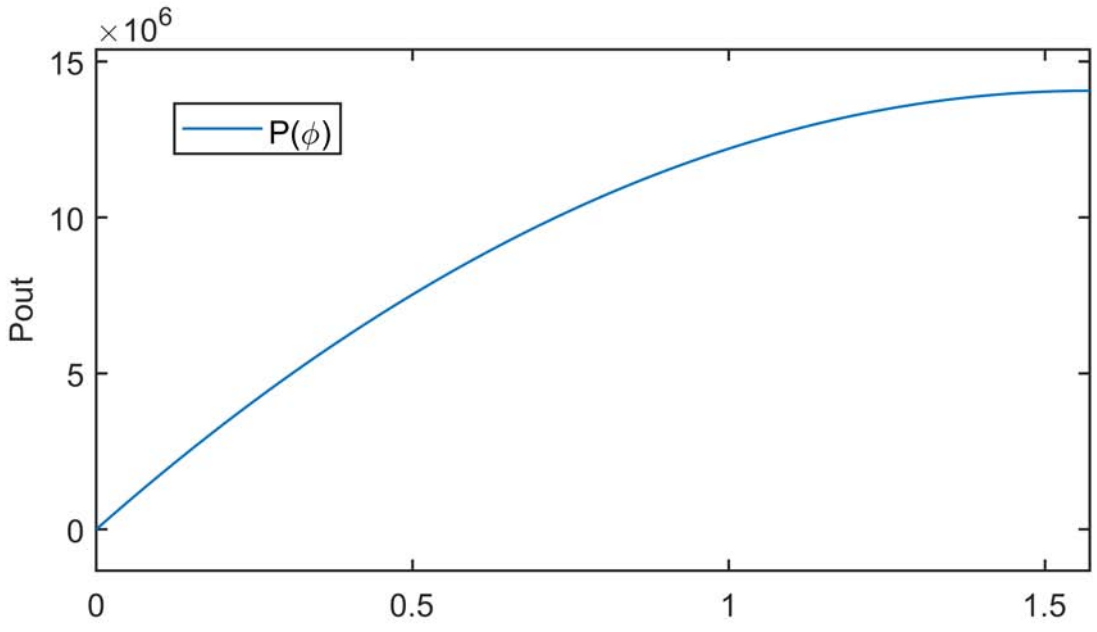
$$P_t = \frac{V_{\text{in}}\, v\, \delta, \text{n}_\text{T}}{\omega L'} \left(1 - \frac{\delta}{\pi}\right) \tag{3.45}$$

Where $n_t = \frac{N_p}{N_s}$ is the transformer ratio referred to the primary and $L' = L_1 + \frac{L_2}{n_t}^2$ is the total leakage inductance referred to the primary.
In step-down mode the phase shift angle is positive while in step-up mode it is negative.

Leakage inductance design The total leakage inductance is calculated using the average power function shown in eq.3.45. It can be written as eq.3.46

$$L' = \frac{V_{\text{in}}\, v\, \delta, \text{n}_\text{T}}{\omega P_t} \left(1 - \frac{\delta}{\pi}\right) \tag{3.46}$$

At this stage it is possible do define the desired phase shift angle at the nominal power. The output power expressed in function of the phase shift is shonwn in Fig.**??**. The maximum power is obtainable with a phase shift of $\pm\phi$ of $\frac{\pi}{2} rad$. The



reactive power absorbed by the transformer increase with the phase shift and it

reduces the utilization factor of the transformer given by $\frac{outputpower}{apparentpower}$. In order to maintain a low $cos\,(\phi)$ a phase shift of 40 deg at nominal power is adopted. By applying the phase shift the square wave of the secondary is shifted forward in order to enhance the power transfer. The secondary voltage phasor anticipates the primary voltage phasor.

DAB1 Capacitor Design

In order to properly design the DAB1 DC link capacitor, the current that flows in the dc link should be determined. It is possible to see this current as the rectified transformer current obtained in the Fourier domain by doing the convolution of the transformer current with the secondary H-bridge switching function.

The voltage on the primary side of the transformer is a square wave of magnitude V_d and it's Fourier transform equation is the following, where k is the harmonic order

$$\langle v_{ab} \rangle_k = \frac{jV_d}{k\pi}\Big(cos(k\pi) - 1\Big) \tag{3.47}$$

The secondary side transformer voltage is equal to the primary voltage divided by the transformation factor and phase shifted by an angle $k\phi$

$$\langle v_{cd} \rangle_k = \langle \frac{v_{ab}}{n_t} \rangle_k e^{-j\phi k} = \langle \frac{v_{ab}}{n_t} \rangle_k (cos(\phi k) - jsin(\phi k)) \tag{3.48}$$

Knowing the primary and secondary voltages it is possible to calculate the transformer current in the Fourier domain.

$$\langle i(t) \rangle_k = \frac{\langle v_{ab} \rangle_k - \langle v_{cd} \rangle_k}{jk\omega L} \tag{3.49}$$

The dc link current harmonics are obtained by doing the convolution of the secondary side current $\langle i(t) \rangle_k$ with the secondary H-bridge switching function $\langle s_2 \rangle_k$

$$\langle s_2 \rangle_k = \frac{j}{k\pi}\Big(cos(kpi) - 1\Big) \tag{3.50}$$

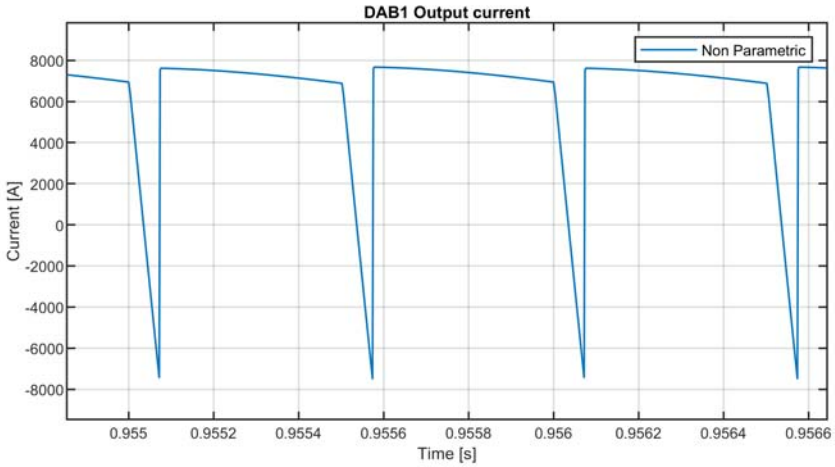
$$\langle i_s \rangle_k = \langle i(t) s_2 \rangle_k = \sum_{-\infty}^{\infty} \langle i(t) \rangle_k \langle s_2 \rangle_i \tag{3.51}$$

With equation 3.51 it is possible to calculate each harmonic of the dc-link current. The DC link voltage ripple corresponding to each harmonic can be found using equation 3.52

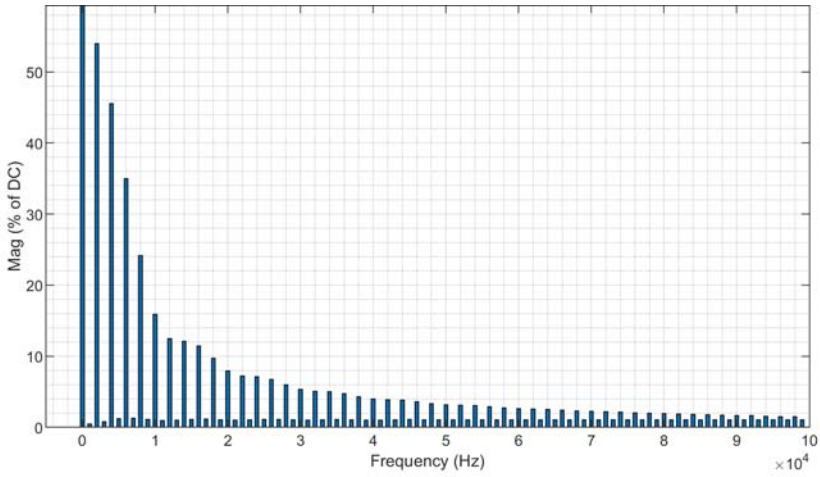
$$\Delta v_k^{pp} = 2 | \frac{\langle i_s \rangle_k}{2 f_s k C} | \tag{3.52}$$

The DAB1 capacitor size can be finally defined with eq. 3.52 once the peak to peak ripple voltage is chosed.

Using this approach both the LV and the MV DAB capacitors values can be calculated. The output current of the DAB1 is the transformer current rectified. It has a trapezoidal shape as shown in Fig.**??**.



The harmonic components of the output current are shown in Fig.**??**. The har-



monic order would be $2Km_f$ with a square wave form. Due to the fact that the shape is trapezoidal there is also the presence of odd terms.

Adopting a maximum voltage ripple of $\pm 10\%$ both for the MV and the LV DC bus the capacitor values result as follow:

- LV DC bus DAB1 capacitor 25.3 mF
- MV DC bus DAB1 capacitor 18μF

3.4.5 Low Voltage AC/DC Capacitor

The design of the low voltage capacitor relative to the AC/DC converter is done following the same procedure of the MV side.

The capacitor size in order to limit the voltage ripple to half of ±10

3.5 $T_2 \rightarrow 2L - 3\phi$

For this topology the single phase DAB is substituted with the three phase DAB. The grid LCL filters and DC capacitors relative to the AC/DC converter are the same of the $2L - 1\phi$ topology.

In this section the DAB3 leakage inductance and DC capacitor are designed.

3.5.1 DAB3 Leakage inductance

In the following equations the leakage inductance is the total inductance of the transformer referred to the primary side.
From the power equation

$$P_t = \frac{V_{MVdc} V_{LVdc} \varphi}{\omega_{sw} n_t L_t} \left(\frac{2}{3} - \frac{\varphi}{2\pi} \right) \tag{3.53}$$

can be calculated the leakage inductance L_t

$$L_t = \frac{V_{MVdc} V_{LVdc} \varphi}{\omega_{sw} n_t P_t} \left(\frac{2}{3} - \frac{\varphi}{2\pi} \right) \tag{3.54}$$

From eq. 3.54, setting $P_t = 5MW$ and $\varphi_n = 40^{\check{r}}$, L_t results $L_t = 11.1mH$.

3.5.2 DAB3 DC link Capacitor

In this subsection it is presented the design of the DC capacitor of the DAB3 topology, following the same approach shown in the previous one.

In order to calculate the capacitor it is required to know the dc-link current, composed of a constant term and harmonics. The dc-link current can be defined in time domain as

$$i_s(t) = i_a(t)s_a(t) + i_b(t)s_b(t) + i_c(t)s_c(t) \tag{3.55}$$

where s_a, s_b, s_c are the switching functions of the secondary legs and i_a, i_b, i_c are the phase currents on the secondary side of the transformer.

The current of eq. 3.55 can be expressed in terms of its Fourier coefficients, becoming

$$\langle i_s(t) \rangle_k = \langle i_a(t)s_a(t) \rangle_k + \langle i_b(t)s_b(t) \rangle_k + \langle i_c(t)s_c(t) \rangle_k \tag{3.56}$$

The product of two functions in the time domain becomes the convolution product of the two functions in the Fourier domain. In the following equation it is shown the convolution product applied to the first term of equation 3.56

$$\langle i_a(t)s_a(t)\rangle_k = \sum_{i=-\infty}^{+\infty} \langle i_a\rangle_{k-i}\langle s_a\rangle_i \tag{3.57}$$

The switching function of the a leg of the primary bridge is, in time domain

$$s_a^s(t) = \begin{cases} 1 & 0 < \theta < \pi \\ 0 & \pi < \theta < 2\pi \end{cases} \tag{3.58}$$

and its Fourier transform results as

$$\langle s_a^p\rangle_k = \frac{j}{2k\pi}(cos(k\pi) - 1) \tag{3.59}$$

.

Knowing that the secondary side converter is controlled with a lagging phase φ , the switching function of the a-leg of the secondary side s_a^s results

$$\langle s_a^s\rangle_k = \langle s_a^p\rangle_k e^{-j\varphi} = \frac{j}{2k\pi}\Big(cos(k\pi) - 1\Big)e^{-j\varphi} \tag{3.60}$$

.

The voltage of the first phase on the primary side of the transformer, shown in Fig 3.7, has the following Fourier coefficients

$$\langle v_{an}^p\rangle_k = \frac{jVd}{3k\pi}\left(cos\left(\pi k\right) - 1 + 2sin\left(\frac{\pi k}{6}sin\left(\frac{\pi k}{2}cos\left(\pi k\right)\right)\right.\right. \tag{3.61}$$

The corresponding secondary side voltage is v_{an}^p phase shifted by an angle φ and multiplied by the transformation factor n_t

$$\langle v_{an}^s\rangle_k = v_{an}^p e^{-j\phi} \tag{3.62}$$

Knowing the primary and secondary voltages, the secondary transformer current can be determined using the KVL

$$\langle i_a^s\rangle_k = \frac{\langle v_{an}^p\rangle_k n_t - \langle v_{an}^s\rangle_k}{\omega_{sw}kL} \tag{3.63}$$

The same logic can be applied to phases b and c, resulting in the formulation of the Fourier coefficients of all the three secondary transformer currents $\langle i_a^s\rangle_k, \langle i_b^s\rangle_k, \langle i_c^s\rangle_k$.

In order to find the DC-link current $\langle i_s\rangle_k$ the convolution of the phase currents with the corresponding leg switching function has to be performed, applying equation 3.57 to each element of equation 3.56 .

The capacitor size is calculated by applying the approach presented in 3.5.2. The tolerance for the voltage fluctuation is set to $\pm 10\%$ of the nominal voltage

for both the buses. The output current of the DAB is affected by multiple of $6km_f$ order harmonics, i.e $6kHz, 12kHz$ and so on. The capacitance calculations takes in account only the 6^{th} harmonic, that is the one with the highest magnitude. In Fig.?? it is shown the harmonic components of the DAB3 output current. The harmonic values are expressed in percentage respect to the DC component. In Fig.?? it is

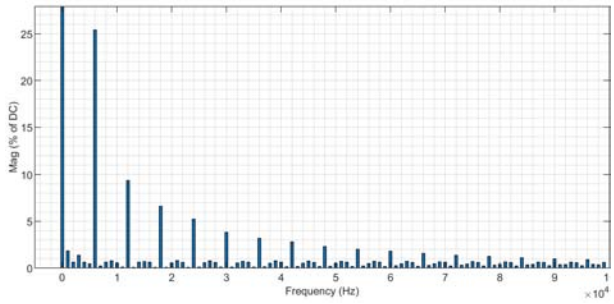


Figure 3.14: THD of the DAB3 output current

shown the output current of the DAB3 when supplying a 5 MW load on the low voltage DC bus. It can be seen that in this case the current is not negative and has a much lower ripple compared to the DAB1 output current.

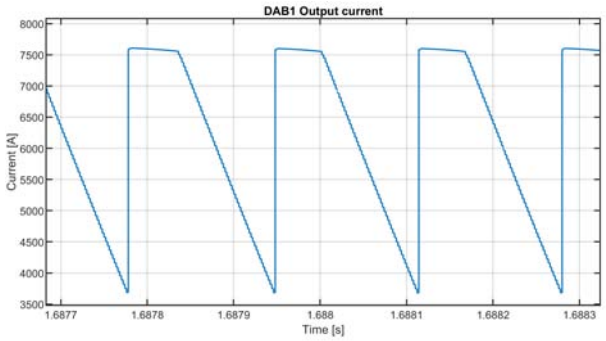


Figure 3.15: Waveform of the DAB3 output current when feeding a resistive load of 5MW at 800V

The capacitance value results as follows:

- MV DC bus $2.16\mu F$
- LV DC bus 1.8 mF

3.6 $T_3 \rightarrow 3L - 3\phi$

In this section it is presented the third topology of SST discussed in this thesis. Firstly an overview of the design choices is given and then the design of the DAB3 NPC Leakage inductance and capacitor is performed.

The proposed topology is composed by two Neutral Point Clamped (NPC) three level converters working as rectifier and inverter and by a NPC three phase DAB.

Even though the NPC topology offers lower DC side ripple and AC THD, and therefore to achieve the same power quality requirements the dimension of the filters can be lower, the design approach of the AC side and DC side filters of the NPC AC/DC converters is the same used for the two level converters. This has been made both for a question of time saving and both to be able to compare the performance of this topology with the other two without having to take into account the different filter performances.

3.6.1 DAB3 NPC Leakage iductance design

In the following equations the leakage inductance is the total inductance of the transformer referred to the primary side.
From the power equation

$$P_t = \frac{3V_1V_2\left(1+\cos\left(\varphi_{in}right\right)\right)}{\pi^2 n_t \omega_{sw} L_t}\sin\delta \tag{3.64}$$

can be calculated the leakage inductance L_t

$$\mathrm{L}_t = \frac{3V_1V_2(1+\cos(\varphi_{in}))}{\pi^2 n_t \omega_{sw} P_t}\sin\delta \tag{3.65}$$

From eq. 3.65, setting $P_t = 5MW$ and $\delta = 40^{\check{\mathrm{r}}}$, $\varphi_{in} = 30^{\check{\mathrm{r}}}$ L_t results $L_t = 8mH$.

3.6.2 DAB3 NPC Capacitor Design

The voltage functions of the NPC three phase DAB are shown in Fig.3.10. The internal phase shift angle is set to $\frac{\pi}{6}$ on order to minimize the HD of the output current.

The Fourier transform is applied to the voltage signals of the primary side. The voltage v_{an}^p in terms of its Fourier coefficients becomes

$$\begin{aligned}\langle v_{an}\rangle_k^p =& \frac{Vd}{3\pi k}\Big(\Big(\sin\left(\frac{\pi k}{2}\right)\sin\left(\frac{\pi k}{6}\right)\sin\left(k\phi_{in}+\pi-\sin\left(k\phi_{in}\right)\right)\Big) \\ &+ \jmath\Big(\sin\left(\frac{\pi k}{2}\right)\sin\left(\frac{\pi k}{6}\right)\left(\cos\left(k\phi_{in}+\pi\right)-1\right)-1-\cos\left(k\phi_{in}\right)\Big)\Big)\end{aligned} \tag{3.66}$$

From it it is possible to get the secondary side voltage signal referred to the primary side, by changing the magnitude and phase shifting it by an angle φ. The secondary voltage v_{an}^{s} can be defined as

$$\langle v_{an} \rangle_k^s = \langle v_{an} \rangle_k^p n_t e^{-j\varphi} \tag{3.67}$$

The transformer secondary current can be calculated as

$$\langle i_{ta}^s \rangle_k = \frac{n_t \langle v_{an} \rangle_k^p - \langle v_{an} \rangle_k^s}{jk\omega L}. \tag{3.68}$$

The current on the dc-bus is given by the superposition of three different currents i_p, i_m and i_n. As it can be seen in Fig.3.16 i_p is different from zero only when both the upper switches are on, i_m when the central switches are on and i_n when the bottom switches are on.

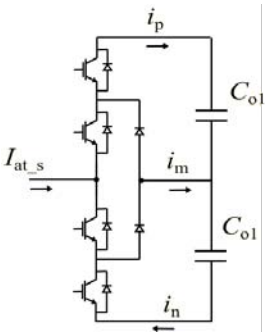


Figure 3.16: DAB3 NPC DC current components

In Fig.3.17 are shown the switching functions that cause the three different currents. It is worth to note that only two of this currents are independent from the others, therefore it is enough to calculate two of them.

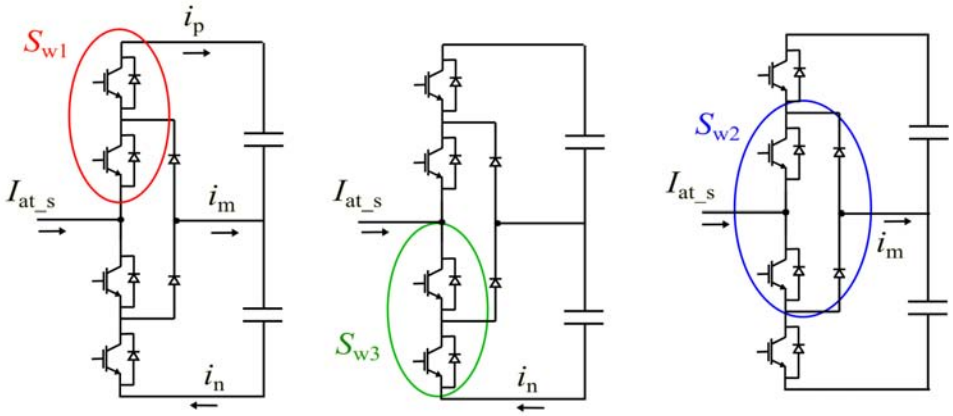


Figure 3.17: DAB3 NPC Switching functions

The dc-currents i_p and i_m are calculated by doing the convolution product between the switching functions of each leg with the corresponding secondary side transformer current, as indicated in the next equation.

$$\langle i_p \rangle_k = \sum_{i=-\infty}^{+\infty} \langle i_{ta}^s \rangle_{k-1} \langle Sw_a^1 \rangle_i + \sum_{i=-\infty}^{+\infty} \langle i_{tb}^s \rangle_{k-1} \langle Sw_b^1 \rangle_i + \sum_{i=-\infty}^{+\infty} \langle i_{tc}^s \rangle_{k-1} \langle Sw_c^1 \rangle_i$$

$$\langle i_m \rangle_k = \sum_{i=-\infty}^{+\infty} \langle i_{ta}^s \rangle_{k-1} \langle Sw_a^2 \rangle_i + \sum_{i=-\infty}^{+\infty} \langle i_{tb}^s \rangle_{k-1} \langle Sw_b^2 \rangle_i + \sum_{i=-\infty}^{+\infty} \langle i_{tc}^s \rangle_{k-1} \langle Sw_c^2 \rangle_i$$

$$\langle i_n \rangle_k = \langle i_p \rangle_k + \langle i_m \rangle_k$$

The capacitor currents can be calculated knowing i_p and i_m

$$\langle i_{Co1} \rangle_k = \langle i_p \rangle_k$$
$$\langle i_{Co2} \rangle_k = \langle i_p \rangle_k + \langle i_m \rangle_k$$

(3.69)

From equation 3.6.2 the voltage ripple on each capacitor can be defined,

$$\Delta v_{Co1}^{pp} = 2 \left| \frac{\langle i_p \rangle_k}{2 f_{sw} k C_{o1}} \right|$$

$$\Delta v_{Co2}^{pp} = 2 \left| \frac{\langle i_p \rangle_k + \langle i_m \rangle_k}{2 f_{sw} k C_{o2}} \right|$$

(3.70)

Assuming that $C_{o1} = C_{o2}$ the DC-bus ripple results

$$\Delta v_{Ceq}^{pp} = 2 \left| \frac{2\langle i_p \rangle_k + \langle i_m \rangle_k}{2 f_{sw} k C_{eq}} \right|$$

(3.71)

where $C_{eq} = 2C_o$ is the the DC-bus equivalent capacitance.

Once the peak to peak voltage ripple is set the corresponding capacitance can be calculated by equation 3.71.

The output current of the DAB3 NPC when feeding a 5MW load is shown in Fig.3.18

The THD of the DAB3 NPC output current is presented in in Fig.3.19

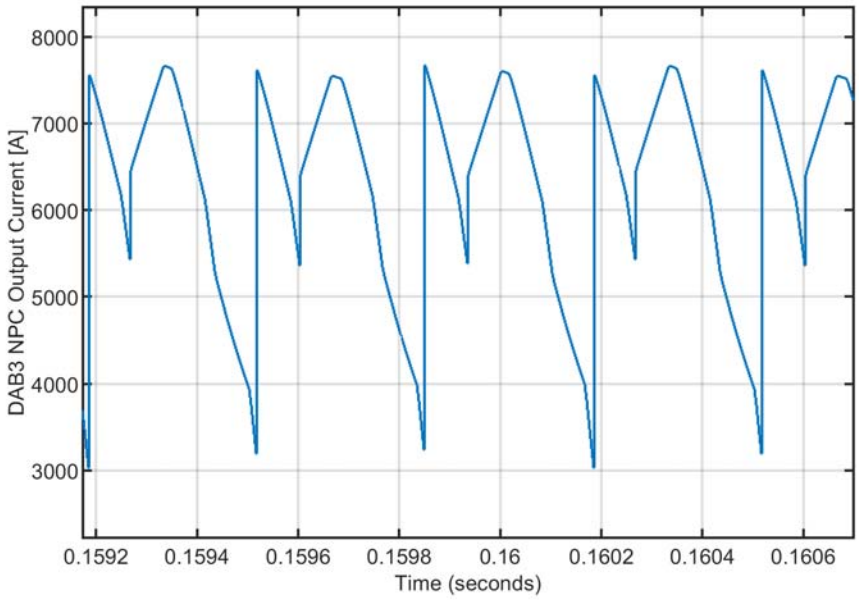


Figure 3.18: DAB3 NPC output current when feeding a 5MW on the LV side

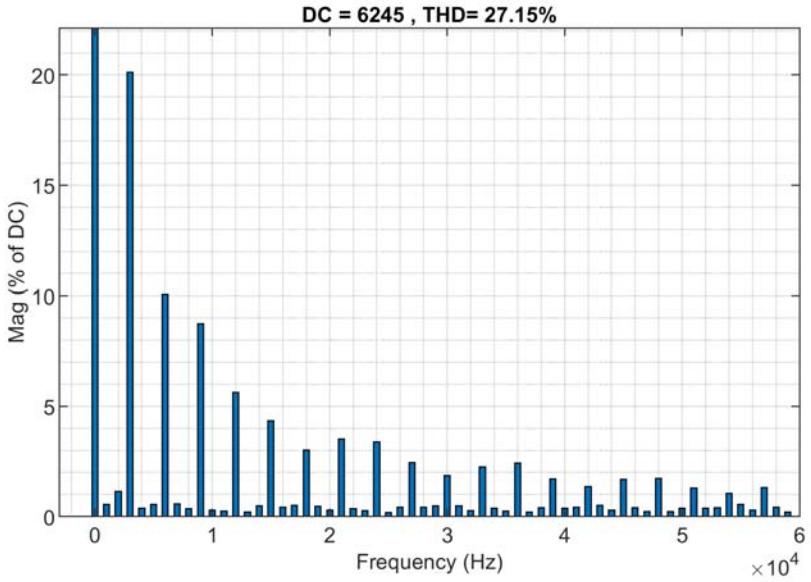


Figure 3.19: THD of the DAB3 NPC output current when feeding a 5MW on the LV side

4 Control Approach

From the control point of view the converters considered in this thesis can be divided in three families:

- Dual active bridge, controlled through phase shift modulation
- Grid forming converter, used for creating the LV grid
- Grid feeding converter, used as rectifier both in LV and MV and as inverter in the medium voltage side.

In this chapter the IDA-PBC control approach, presented in Section 2.3.2, is applied to all the converters.

The reason of adopting a non linear control approach instead of using PI controllers, is that every converter stage of the SST appears as a constant power load (CPL) to every preceding converter stage. This could bring to instability. IDA-PBC is a robust by design control that ensures stability.

4.1 Dual Active Bridge Control

In this section the design of the IDA-PBC controller of DAB1, DAB3 and DAB3 NPC are presented. There are two main approach for the design of the DAB controller. The first [19] consider the detailed state space model of the DAB which involves both the transformer current and the output capacitor voltage as state variables, the second [20] considers only the capacitor output voltage. The transformer current dynamics are captured by both of the models, in the simplified one trough the transformer power equation. The derivation of the IDA-PBC control for the simplified model is much easier but since it is based on the power transfer equation of the DAB it is valid only in ideal conditions, i.e. when the transformer losses are negligible. The losses of the non ideal transformer brings to a steady state error on the output voltage. This can be overcome both by introducing a damping factor that simulate a virtual loss and by adding an additional integrator control that suppress the steady state error. The addition of an integrator doesn't modifies the passivity of the system and doesn't affect its stability.[21]

The IDA-PBC approach has already been applied to DAB1 and DAB3 in the master Thesis [22].

Anyway the approach presented in this section is slightly different, in particular on how the port Hamiltonian system is formed. In [22] the load current is defined

in terms of the capacitor voltage by mean of a resistive load and a constant power load, and then included in the damping matrix. Differently, in this work the load current is considered as a disturbance, bringing to a different control function.

Therefore, the contribution of this section are:

- IDA-PBC applied to DAB1, DAB3, DAB3 NPC

4.1.1 IDA-PBC 1ϕ Design

The simplified state space model of the DAB1, applying Kirchoff current load to the DC node, is

$$C\frac{dv_{dc}}{dt} = i_L - i_s \tag{4.1}$$

where i_L is the load current and i_s is the DAB1 output current. The DAB output power P_t is

$$P_t = \frac{V_{in}\ v\ \delta\ n_t}{\omega L}\left(1 - \frac{\delta}{\pi}\right) \tag{4.2}$$

From power balance, knowing that the output power can be expressed also by $P_t = i_s v_{dc}$ the output current results

$$i_s = \frac{V_{in}\ \delta\ n_t}{\omega L}\left(1 - \frac{\delta}{\pi}\right) \tag{4.3}$$

Substituting 4.3 in 4.1 we get the following state space equation

$$C\frac{dv_{dc}}{dt} = i_L - \frac{n_t V_{in}\delta}{\omega L}\left(1 - \frac{\delta}{\pi}\right) \tag{4.4}$$

that can be expressed in port Hamiltonian form

$$\dot{\mathbf{x}} = [\mathbf{J}(\mathbf{x},\mathbf{u}) - \mathbf{R}(\mathbf{x})]\frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} + g\left(\delta\right)u\left(\delta\right) + \zeta \tag{4.5}$$

with the following elements

$x = Cv_{dc}$	$H\left(\mathbf{x}\right) = \frac{1}{2}Cv_{dc}^2$	$\frac{\partial H(\mathbf{x})}{\partial x} = v_{dc}$
$J = -J^{'} = 0$	$R = R^{'} = 0$	$u = \delta$
$g(u) = \frac{nV_{in}}{\omega L}\left(\frac{\delta}{\pi} - 1\right)$	$\zeta = -i_L$	

The desired energy function and its partial derivative are chosen as

$\mathrm{H}_d\left(x\right) = \left(x - x^*\right)^2 C = \frac{1}{2}C\left(v_{dc} - v_{dc}^2\right)\ \frac{\partial H_d(\mathbf{x})}{\partial x} = v_{dc} - v_{dc}^*$

H_d satisfies the equilibrium assingment condition 2.10 and Lyapunov stability 2.11. From 2.12 and 2.13, K can be defined as follows:

$$\frac{\partial H_a}{\partial x} = K = -\frac{x^*}{C} \tag{4.6}$$

where K satisfies the integrability condition 2.9.

The assigned interconnection matrix are chosen as $J_a = 0$ and $R_a = R_1$. The closed loop system can be written as

$$\dot{x} = (J_d - R_d) \frac{\partial H_d(\mathbf{x})}{\partial x} \tag{4.7}$$

where $J_d = J + J_a$ and $R_d = R + R_a$.

By equating eq.4.7 and eq.4.5 and substituting the defined elements it is possible to get the following equation

$$i_L + \delta \frac{nV_{in}}{\omega L} \left(\frac{\delta}{\pi} - 1 \right) + R_1 (v_{dc} - v_{dc}^*) = 0 \tag{4.8}$$

from which the following two solutions can be derived

$$\delta_{1,2} = \frac{\pi}{2} \pm \sqrt{\left(\frac{\pi}{2}\right)^2 - \frac{\omega L \pi}{n_t V_{in}} (i_L - R_1 (v_{dc} - v_{dc}^*))} \tag{4.9}$$

The smaller solution is the only with a stable operation point, and therefore is taken for the control.

4.1.2 IDA-PBC 3ϕ Design

In this subsection the IDA-PBC is designed for the DAB3. Fig.**??** shows the circuit diagram of a DAB3. It is operated with phase shift modulation with the power flowing from the leading bridge to the lagging bridge. Depending on the desired power flow the phase shift angle can be positive or negative.
The control defined in this subsection is written in a general form and can be applied to both the operation modes considering that:

- The inductance L is the total leakage inductance of the transformer referred to the input voltage side
- The transformation ratio n_t is calculated as the ratio between the output voltage v_{dc} and the input voltage V_{in}.

As for the DAB1 the average state space equation of the output DC terminal is

$$C \frac{dv_{dc}}{dt} = i_s - i_L \tag{4.10}$$

and the output power is

$$P_t = \frac{n_t V_d v_{dc} \phi}{\omega L} \left(\frac{2}{3} - \frac{\phi}{2\pi} \right) \tag{4.11}$$

The winding resistance of the transformer are neglected.
From power balance the output current can be written

$$i_s = \frac{n_t V_d \phi}{\omega L} \left(\frac{2}{3} - \frac{\phi}{2\pi} \right) \tag{4.12}$$

and substituting it in eq.4.10 the following system can be derived

$$C \frac{dv_{dc}}{dt} = \frac{n_t V_d \phi}{\omega L} \left(\frac{2}{3} - \frac{\phi}{2\pi} \right) - i_L \tag{4.13}$$

As per DAB1 it can be written in port Hamiltonian form

$$\dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}] \frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} + g(\phi) u + \zeta$$

equation
by considering the following quantities

$x = C v_{dc}$	$H(x) = \frac{1}{2} C v_{dc}^2$	$\frac{\partial H(x)}{\partial x} = v_{dc}$
$J = -J^{'} = 0$	$R = R^{'} = 0$	$u = \phi$
$g(\phi) = \frac{u V_{in}}{\omega L} \left(\frac{2}{3} - \frac{\phi}{2\pi} \right)$	$\zeta = -i_L$	

The desired energy function H_d is set up in order to fulfil the Lyapunov stability condition 2.11

$$H_d(x) = \frac{1}{2} C (v_{dc} - v_{dc}^*)^2 \tag{4.15}$$

From 2.12 and 2.13, K can be defined as follows:

$$\frac{\partial H_a}{\partial x} = K = -\frac{x^*}{C} \tag{4.16}$$

where K satisfies the integrability condition 2.9.

The assigned interconnection and damping matrices are chosen as $J_a = 0$ and $R_a = R_1$. The closed loop system can be written as

$$\dot{x} = (J_d - R_d) \frac{\partial H_d(\mathbf{x})}{\partial x} \tag{4.17}$$

where $J_d = J + J_a$ and $R_d = R + R_a$.

By equating the original port Hamiltonian system with the closed loop equation and substituting all the defined quantities the following expression can be found,

$$\phi^2 - \frac{4\pi}{3}\phi - \frac{2\pi\omega L}{n_t V_{in}}\left(R_1\left(v_{dc} - v_{dc}^*\right) - i_L\right) = 0 \tag{4.18}$$

and two solutions for the control phase shift can be derived

$$\phi_{1,2} = \frac{2\pi}{3} \pm \sqrt{\left(\frac{2\pi}{3}\right)^2 + \frac{2\pi\omega L}{n_t V_{in}}\left(R_1\left(v_{dc} - v_{dc}^*\right) - i_L\right)} \tag{4.19}$$

The smaller solution is the only with a stable operating point, and therefore is taken for the control.

4.1.3 IDA-PBC 3ϕ NPC Design

In this section the control function of the three-phase NPC DAB is derived following the IDA-PBC method described in subsection 2.3.

The average system equation on the DC link are

$$C\frac{dv_{dc}}{dt} = i_s - i_L \tag{4.20}$$

where i_s and i_L are the output current and the load current respectively. The DC link capacitors are connected in series and C is the corresponding equivalent capacitor.

The output power corresponding to the first harmonic of the transformer current, defined in 3.3.2, is given by

$$P_t = \frac{3V_{in}v_{dc}\left(1 + \cos\left(\varphi_i n\right)\right)}{\pi^2 n_t \omega_{sw} L_t}\sin\left(\delta\right) \tag{4.21}$$

.

From power balance the output current i_s results

$$i_s = \frac{P_t}{v_{dc}} = \frac{3V_{in}\left(1 + \cos\left(\varphi_i n\right)\right)}{\pi^2 n_t \omega_{sw} L_t}\sin\left(\delta\right) \tag{4.22}$$

In order to express the system in Port Hamiltonian form it is needed to avoid the use of trigonometric functions, therefore the $\sin\delta$ is expressed in its approximated form using the Bhaskara sine approximation formula:

$$\sin\delta = \frac{16\delta\left(\pi - \delta\right)}{5\pi^2 - 4\delta\left(\pi - \delta\right)}. \tag{4.23}$$

The Hamiltonian form of the model is

$$\dot{x} = \left[J - R\right]\frac{\partial H\left(x\right)}{\partial x} + g\left(\delta\right)u\left(\delta\right) + \zeta \tag{4.24}$$

where the following quantities are defined

$x = Cv_{dc}$	$H(x) = \frac{1}{2}Cv_{dc}^2$	$\frac{\partial H(x)}{\partial x} = v_{dc}$
$J = -J^{'} = 0$	$R = R^{'} = 0$	$u(\delta) = \delta$
$g(\delta) = \frac{3V_{in}(1+\cos(\varphi_i n))}{\pi^2 n_t \omega_{sw} L_t} \frac{16(\pi-\delta)}{5\pi^2-4\delta(\pi-\delta)}$	$\zeta = -i_L$	

The the desired energy function of the system is defined in order to stabilise the system to its reference point v_{dc}^*:

$$H_d(x) = \frac{1}{2}C\left(v_{dc} - v_{dc}^*\right)^2 \tag{4.25}$$

The assigned energy function, $H_a(x) = H(x) - H_d(x)$ results

$$H_a(x) = \frac{1}{2}\ C\ {v_{dc}^*}^2 \tag{4.26}$$

From 4.26, 2.12 and 2.13, K can be defined as follows:

$$\frac{\partial H_a}{\partial x} = K = -\frac{x^*}{C} \tag{4.27}$$

Choosing $J_a = 0$ and $R_a = R_1$ brings to the following closed loop equation

$$\dot{x} = -R_1\left(v_{dc} - v_{dc}^*\right). \tag{4.28}$$

By equating eq.4.28 with eq.4.24 the following to equations can be derived:

$$\begin{cases} \delta^2 - \delta + \frac{5k\pi^2}{4\,4+k)t} = 0 \\ k = \frac{\pi^2 n_t \omega_{sw} L_t}{3V_{in}(1+\cos\varphi_{in})}\left(i_L - R_1\left(v_{dc} - v_{dc}^*\right)\right) \end{cases} \tag{4.29}$$

and solving for δ it is possible to get the following control equations

$$\delta_{1,2} = \frac{\pi}{2} \pm \sqrt{\left(\frac{\pi}{2}\right)^2 - \frac{5}{4}\left(\frac{k\pi^2}{k+4}\right)} \tag{4.30}$$

where the smallest solution is the one with physical meaning.
Finally, by substituting k we get

$$\delta = \frac{\pi}{2} - \sqrt{\frac{\pi^2}{4} - \frac{5L_t n_t \pi^4 w_{sw}(i_L - R_1(v_{dc} - v_{dc}^*))}{12V_{in}(\cos\phi_{in}+1)\left(\frac{L_t n_t \pi^2 \omega_{sw}\left(i_L - R_1\left(v_{dc} - v_{dc}^*\right)\right)}{3V_{in}(\cos\phi_{in}+1)+4}\right)}}. \tag{4.31}$$

4.2 Voltage Source Inverter

4.2.1 VSI-IDA PBC

In this subsection the control approach of the voltage source (VS) LV grid forming inverter is presented. The simplified model used for the design of the IDA-PBC control is shown in Fig.**??**. The following assumptions are made:

- The shunt damping resistance of the filter is neglected
- The grid inductance is considered as part of the load and therefore is not taken into account in the model
- The case of study is setted in a LV smart grid where the SST set the reference angle θ that is followed by the other generators in the LV grid. Therefore the $50Hz$ reference angle is defined simply with a saw tooth generator. The DC voltage is assumed ripple free and slow varying.

The average model of the VS inverter can be written, in the d, q frame, as:

$$\begin{cases} L\dot{i}_{ld} & = -R_L i_{ld} - \omega_{dq} L i_{lq} + m_d v_{dc} - v_{od}, \\ L\dot{i}_{lq} & = -R_L i_{lq} + \omega_{dq} L i_{ld} + m_q v_{dc} - v_{oq}, \\ C\dot{v}_{od} & = i_{1d} - i_{od} + \omega C v_{oq}, \\ C\dot{v}_{oq} & = i_{1q} - i_{oq} - \omega C v_{od} \end{cases} \tag{4.32}$$

In order to apply the IDA-PBC approach to the VSI the system should be re-ordered in its port Hamiltonian (pH) form

$$\dot{\mathbf{x}} = [\mathbf{J}(\mathbf{x}, \mathbf{u}) - \mathbf{R}(\mathbf{x})] \frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} + \zeta(\mathbf{u}), \tag{4.33}$$

Comparing 4.33 and 4.52 the following elements can be defined

$$\mathbf{x} = \begin{bmatrix} L i_{ld} & L i_{lq} & C v_{od} & C v_{oq} \end{bmatrix}^{\mathbf{T}} \tag{4.34}$$

$$\mathbf{J} = \begin{bmatrix} 0 & \omega L & -1 & 0 \\ -\omega L & 0 & 0 & -1 \\ 1 & 0 & 0 & \omega C \\ 0 & 1 & -\omega C & 0 \end{bmatrix} \tag{4.35}$$

$$\mathbf{R} = \begin{bmatrix} R & 0 & 0 & 0 \\ 0 & R & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.36}$$

$$H(\mathbf{x}) = \frac{1}{2} L i_{ld}^2 + \frac{1}{2} L i_{lq}^2 + \frac{1}{2} C v_{od}^2 + \frac{1}{2} C v_{oq}^2 \tag{4.37}$$

$$\zeta(\mathbf{u}) = \begin{bmatrix} \frac{v_{dc}}{\sqrt{3}} m_d & \frac{v_{dc}}{\sqrt{3}} m_q & -i_{od} & -i_{oq} \end{bmatrix}^{\mathbf{T}} \tag{4.38}$$

$$\mathbf{u} = \begin{bmatrix} m_d & m_q \end{bmatrix}^{\mathbf{T}} \tag{4.39}$$

The control objective is that the control variables track their reference i_{ld}^*, i_{lq}^* and v_{od}^*, v_{oq}^*. A possible candidate desired energy function can be

$$H_d(\mathbf{x}, \mathbf{x}^*) = \frac{1}{2} L (i_{ld} - i_{ld}^*)^2 + \frac{1}{2} L \left(i_{lq} - i_{lq}^*\right)^2 + \frac{1}{2} C (v_{od} - v_{od}^*)^2 + \frac{1}{2} C \left(v_{oq} - v_{oq}^*\right)^2 \tag{4.40}$$

that can be written in compact form as

$$H_d(\mathbf{x}, \mathbf{x}^*) = \frac{1}{2} \epsilon^T \mathbf{P} \epsilon \tag{4.41}$$

where

$$\mathbf{P} = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C \end{bmatrix} \tag{4.42}$$

and ϵ is the tracking error vector

$$\epsilon = \mathbf{x} - \mathbf{x}^* = \begin{bmatrix} L (i_{ld} - i_{ld}^*) \\ L \left(i_{lq} - i_{lq}^*\right) \\ C (v_{od} - v_{od}^*) \\ C \left(v_{oq} - v_{oq}^*\right) \end{bmatrix} \tag{4.43}$$

$H_d(x)$ has its minimum in the reference point x^*.

The approach in this control is to put some virtual damping in parallel with the filter capacitance and in series with the filter inductance, therefore the assigned damping matrix is chosen as

$$\mathbf{R_a} = \begin{bmatrix} R_1 & 0 & 0 & 0 \\ 0 & R_1 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \tag{4.44}$$

where R_1 and $G_2 = \frac{1}{R_2}$ are the damping respectively in series with the filter inductance and in parallel with the filter capacitance. In order to keep a physical correlation between the virtual parameters and the real model the shunt damping factor is indicated with the admittance symbol for the reason that will be clear in the next lines.

The assigned interconnection matrix is chosen in order to decouple the control of the d and q axis, as follows

$$\mathbf{J_a} = \begin{bmatrix} 0 & -\omega L & -1 & 0 \\ \omega L & 0 & 0 & -1 \\ 0 & 0 & 0 & -\omega C \\ 0 & 0 & \omega C & 0 \end{bmatrix} \tag{4.45}$$

The desired interconnection and damping matrices result

$$\mathbf{R_d} = \mathbf{R} + \mathbf{R_a} = \begin{bmatrix} R + R_1 & 0 & 0 & 0 \\ 0 & R + R_1 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \tag{4.46}$$

$$\mathbf{J_d} = \mathbf{J} + \mathbf{J_a} = \mathbf{0} \tag{4.47}$$

Now the closed loop system can be written in terms of J_d, R_d and $\frac{\partial H_d}{\partial x}$

$$\dot{\mathbf{x}} = [\mathbf{J_d}(\mathbf{x}, \mathbf{u}) - \mathbf{R_d}(\mathbf{x})] \frac{\partial H_d(\mathbf{x})}{\partial \mathbf{x}} \tag{4.48}$$

By equating eq.4.48 and eq.4.33 the following set of equation can be derived, defining the control functions m_d, m_q and the current references i^*_{ld}, i^*_{lq}

$$\begin{cases} m_d = \frac{\sqrt{3}}{v_{dc}} \left(v_{od} - \omega L i_{lq} - R_1 \left(i_{ld} - i^*_{ld} \right) + R i^*_{ld} \right), \\ m_q = \frac{\sqrt{3}}{v_{dc}} \left(v_{oq} + \omega L i_{ld} - R_1 \left(i_{lq} - i^*_{lq} \right) + R i^*_{ld} \right), \\ i^*_{ld} = i_{od} - C\omega v_{oq} - G_2 \left(v_{od} - v^*_{od} \right), \\ i^*_{lq} = i_{oq} + C\omega v_{od} - G_2 \left(v_{oq} - v^*_{oq} \right) \end{cases} \tag{4.49}$$

The reason of the use of damping admittance can be seen in equations 3 and 4 of eq.4.49 where the physical unit of the equation is Ampere.

4.3 Current Source Converter

4.3.1 Front end converter IDA-PBC

In this subsection the design procedure for the control of the current source front end converter (FED) is presented. The proposed control is applied both to the MV converter, when working as inverter or rectifier, and to the LV converter when working as rectifier.

For the design of the controller a low order model of the filter is considered. This assumption is solid because this control, by virtually damping the circuit, modifies the filter response and cuts the frequency response of the capacitor.

The control objectives for this converter are:

1. Maintain a constant and stable voltage on the DC side when working as rectifier
2. Have a unitary power factor
3. Maintain the THD injected to the grid below the power quality limit

The equations describing the front end converter in dq frame are the following

$$\begin{cases} L\dot{i}_d & = -R_L i_d - \omega_{dq} L i_q + m_d v_{dc} - e_d, \\ L\dot{i}_q & = -R_L i_q + \omega_{dq} L i_d + m_q v_{dc} - e_q, \\ C\dot{v}_{dc} & = i_s - m_d i_d - m_q i_q \end{cases} \quad (4.50)$$

and can be expressend in matrix form as follows

.

$$\begin{bmatrix} L\dot{i}_d \\ L\dot{i}_q \\ C\dot{v}_{dc} \end{bmatrix} = \begin{bmatrix} -R_L & -\omega_{dq} L & m_d \\ \omega_{dq} L & -R_L & m_q \\ -m_d & -m_q & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} + \begin{bmatrix} -e_d \\ -e_q \\ i_s \end{bmatrix} \quad (4.51)$$

In order to apply the IDA-PBC method the system should be written in his Port Hamiltonian form, i.e.

$$\dot{\mathbf{x}} = [\mathbf{J}(\mathbf{x}, \mathbf{u}) - \mathbf{R}(\mathbf{x})] \frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} + \zeta, \quad (4.52)$$

where $\mathbf{x}$ is the state vector, $\mathbf{J}(\mathbf{x}, \mathbf{u})$ is the interconnection matrix, $\mathbf{R}(\mathbf{x})$ is the damping matrix, $H(\mathbf{x})$ is the energy function of the system and ζ is a vector containing the external perturbations.

Comparing eq 4.52 and eq. 4.51 the matrices $\mathbf{R}, \mathbf{J}$ and the vectors $\dot{\mathbf{x}}$ and ζ can be defined

$$\mathbf{x} = [x_1,\ x_2,\ x_3]^T = [Li_d,\ Li_q,\ Cv_{dc}]^T \quad (4.53)$$

$$\mathbf{u} = \left[m_d,\ m_q\right]^T \quad (4.54)$$

$$\mathbf{J(u)} = \begin{bmatrix} 0 & -\omega_{dq}L & m_d \\ \omega_{dq}L & 0 & m_q \\ -m_d & -m_q & 0 \end{bmatrix} \tag{4.55}$$

$$\mathbf{R} = \begin{bmatrix} R_L & 0 & 0 \\ 0 & R_L & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{4.56}$$

$$\zeta = [-\mathbf{e_d} - \mathbf{e_q i_s}]^{\mathbf{T}} \tag{4.57}$$

The energy function $H(\mathbf{x})$ of the system can be determined as the energy stored in the filter inductance and in the DC capacitance

$$H(\mathbf{x}) = \frac{1}{2}\left(\frac{x_1^2}{L} + \frac{x_2^2}{L} + \frac{x_3^2}{C}\right) = \frac{Li_d^2}{2} + \frac{Li_q^2}{2} + \frac{Cv_{dc}^2}{2} \tag{4.58}$$

and the corresponding partial derivatives vector is

$$\frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} = [i_d,\ i_q,\ v_{dc}]^T \tag{4.59}$$

The aim of the IDA-PBC control is to design a control law $\mathbf{u}$ that, by acting on the i_d and i_q currents, brings the state vector to its equilibrium point defined as

$$\mathbf{x}^* = \left[\mathbf{Li_d^*},\ \mathbf{Li_q^*},\ \mathbf{Cv_{dc}^*}\right]^{\mathbf{T}} \tag{4.60}$$

.

The closed loop dynamics of the system can be defined as

$$\dot{\mathbf{x}} = [\mathbf{J_d}(\mathbf{x}, \mathbf{u}) - \mathbf{R_d}(\mathbf{x})]\frac{\partial H_d(\mathbf{x})}{\partial \mathbf{x}} \tag{4.61}$$

where $\mathbf{J_d}, \mathbf{R_d}, \mathbf{H_d}(\mathbf{x})$ should be chosen in order to satisfy the following proposition

$$\left.\frac{\partial H_d(\mathbf{x})}{\partial \mathrm{x}}\right|_{\mathbf{x}=\mathbf{x}^*} = 0 \tag{4.62}$$

.

$\mathbf{J_d}, \mathbf{R_d}, \mathbf{H_d}(\mathbf{x})$ are respectively the desired interconnection matrix, damping matrix and energy function. This quantities are defined as follows

$$\mathbf{R_d}\left(\mathbf{x}\right) = \mathbf{R}\left(\mathbf{x}\right) + \mathbf{R_a}\left(\mathbf{x}\right) \tag{4.63}$$

$$\mathbf{J_d}\left(\mathbf{x},\mathbf{u}\right) = \mathbf{J}\left(\mathbf{x},\mathbf{u}\right) + \mathbf{J_a}\left(\mathbf{x},\mathbf{u}\right) \tag{4.64}$$

where $\mathbf{J_a}(\mathbf{x})$ and $\mathbf{R_a}(\mathbf{x})$ are matrices used to synthesize the control strategy. They can be selected in a wide range of matrices.

In this case the assigned interconnection matrix is used to decouple the d and q axis control equations by eliminating the existing coupling between the state variables

$$\mathbf{J_a}(\mathbf{u}) = -\mathbf{J_a^T}(\mathbf{u}) = \begin{bmatrix} 0 & \omega_{dq}L & -m_d \\ -\omega_{dq}L & 0 & -m_q \\ m_d & m_q & 0 \end{bmatrix} \tag{4.65}$$

and the assigned damping matrix is used to introduce some damping R_1 and R_2 respectively in series with the filter inductance and in parallel with the DC capacitor

$$\mathbf{R_a} = \mathbf{R_a^T} = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_1 & 0 \\ 0 & 0 & 1/R_2 \end{bmatrix} \tag{4.66}$$

.

The choice of $H_d(\mathbf{x})$ is made in order to fulfil its equilibrium point in $\mathbf{x}$. Defining

$$\mathbf{P} = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & C \end{bmatrix} \tag{4.67}$$

and $\epsilon = \mathbf{x} - \mathbf{x}^*$

the desired energy function can be defined as

$$H_d(\mathbf{x}) = \frac{\mathbf{1}}{\mathbf{2}}\left(\epsilon^{\mathbf{T}}\mathbf{P^{-1}}\epsilon\right). \tag{4.68}$$

By equating 4.61 and 4.52 the following equation can be written

$$[\mathbf{J}(\mathbf{x},\mathbf{u}) - \mathbf{R}(\mathbf{x})]\frac{\partial H(\mathbf{x})}{\partial \mathbf{x}} + \zeta = \dot{\mathbf{x}} = [\mathbf{J_d}(\mathbf{x},\mathbf{u}) - \mathbf{R_d}(\mathbf{x})]\frac{\partial H_d(\mathbf{x})}{\partial \mathbf{x}} \tag{4.69}$$

and rearranging the terms and substituting the actual parameters we get:

$$\begin{bmatrix} R_1 & -\omega_{dq}L & m_d \\ \omega_{dq}L & R_1 & m_q \\ -m_d & -m_q & \frac{1}{R_2} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} + \begin{bmatrix} -e_d \\ -e_q \\ i_s \end{bmatrix} = \begin{bmatrix} R_L R_1 & 0 & 0 \\ 0 & R_L R_1 & 0 \\ 0 & 0 & 1/R_2 \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \\ v_{dc}^* \end{bmatrix} \tag{4.70}$$

that have as solution the following set of equations.
The first two equations express the control laws while the third express i_s in terms of the control function $\mathbf{u}$.

$$\begin{cases} m_d = \frac{1}{v_{dc}} \left(R_L i_d^* + \omega_{dq} L i_q - R_1 (i_d - i_d^*) + e_d \right), \\ m_q = \frac{1}{v_{dc}} \left(R_L i_q^* - \omega_{dq} L i_d - R_1 (i_q - i_q^*) + e_q \right), \\ i_s = m_d i_d + m_q i_q - \frac{1}{R_2} \left(v_{dc} - v_{dc}^* \right) \end{cases} \tag{4.71}$$

The control reference value is the inductance reference current.

When the converter works as inverter the reference current is used to control the active and reactive power injected to the grid by setting the actual current value in the control equations.

When the converter works as rectifier, the reference current is calculated in order to maintain a constant voltage on the DC bus. The reference current is defined as follows.

By substituting the first two equations of 4.71 in the third one, assuming that the system is in steady state tracking the reference values $i_d = i_d^*, i_q = i_q^*$ and considering that the grid voltage has a unitary power factor $PF = 1 \rightarrow e_q = 0$, the following equation defining i_d^* can be defined:

$$i_d^{*2} + \frac{e_d}{R_L} i_d^* + i_q^* - \frac{v_{dc}}{R_L} \left(i_s + \frac{1}{R_2} \left(v_{dc} - v_{dc}^* \right) \right) = 0 \tag{4.72}$$

The following two solutions can be calculated:

$$i_{d_{1,2}}^* = \frac{1}{2} \left[-\frac{e_s}{R_L} \pm \sqrt{\frac{e_d}{R_L}^2 - 4 i_q^{*2} + 4 \frac{v_{dc}}{R_L} \left(i_s + \frac{1}{R_2} \left(v_{dc} - v_{dc}^* \right) \right)} \right] \tag{4.73}$$

Both the solutions are physically meaningful, meaning that are two actual operating points. Since a smaller current leads to smaller losses the root with positive sign is chosen.

5 New Roles of SST

5.1 Synchronverter

The Synchronverter is defined as a power electronic converter that behaves like a synchronous machine, generator or motor. This means that the converter follows the highly non linear SG dynamics equation, both from the electrical and the mechanical point of view, reacting with a active and reactive power droop in case of a grid frequency or voltage variation. In this way the converter participate to the grid frequency and voltage primary control without the need of any communication systems. In order to model the converter as a SG the following correspondences are assumed:

- The back emf $M_f i_f$ of the SG corresponds to the converter side voltage
- The synchronous reactance of the SG corresponds to the converter side filter inductance
-

A model and a control approach have been proposed in [23] and upgraded in [24], where the synchronisation is achieved without the use of a PLL. In this section it is presented the application of this control to the medium voltage converter of the proposed SST. For the mathematical derivation of the model the reader is invited to refer to [23]. The model of a round-rotor synchronous machine can be described by eqs. 5.1 - 5.4

$$J\frac{d^2\theta_m}{dt^2} = T_m - T_e - D_p\frac{d\theta}{dt} \tag{5.1}$$

$$T_e = M_f i_f \langle i, \sin\theta \rangle \tag{5.2}$$

$$e = \frac{d\theta}{dt} M_f i_f \sin\theta \tag{5.3}$$

$$Q = -\frac{d\theta}{dt} M_f i_f \langle i, \cos\theta \rangle \tag{5.4}$$

Where eq. 5.1 rapresents the swing equations of the machines, eq. 5.2 express the electromagnetic torque, eq. 5.3 defines the back emf due to the rotor movement and eq. 5.4 defines the reactive power delivered by the machine. Where:

- T_e is the electromagnetic torque
- T_m is the mechanical torque applied to the rotor
- D_p is the damping coefficient of the rotor
- $\frac{d\theta}{dt}$ is the virtual angular speed of the machine
- $M_f i_f$ is the back electromotive force
- $\langle ., . \rangle$ is the inner product in $\Re^3$
- $\sin\theta = \left[\sin\theta,\ \sin\left(\theta - \frac{\mathbf{2}}{\mathbf{3}\pi}\right),\ \sin\left(\theta + \frac{\mathbf{2}}{\mathbf{3}\pi}\right)\right]^{\mathbf{T}}$
- $\cos\theta = \left[\cos\theta,\ \cos\left(\theta - \frac{2}{3\pi}\right),\ \cos\left(\theta + \frac{2}{3\pi}\right)\right]^{T}$
- $i = [i_a,\ i_b\ , i_c]$ are the stator currents

The SG is assumed to have one pole per phase, therefore the mechanical angle coincides with the electrical angle.

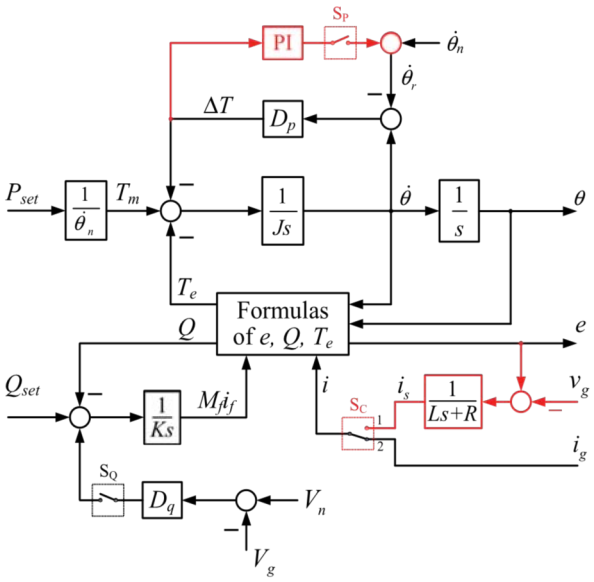


Figure 5.1: Control scheme of the self-synchronised Synchronverter [24]

The control, shown in Fig.5.1, is composed by two channels, one controlling the active power and the other controlling the reactive power.

Assuming that the SG is connected to an infinite power grid, as shown in Fig.**??** the following equations can be written,

$$P = \frac{3V_g E}{2X_s} \sin(\theta - \theta_g) \tag{5.5}$$

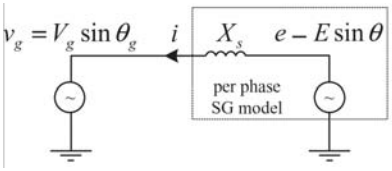


Figure 5.2: Single phase equivalent circuit of synchronverter connected to an infinite power bus [24]

$$Q = \frac{3V_g}{2X_s}\left[E\cos\left(\theta - \theta_g\right) - V_g\right] \tag{5.6}$$

where V_g is the amplitude of the grid voltage, E is the amplitude of the converter voltage that can be controlled by $M_f i_f$, X_s is the synchronous reactance and θ , θ_g are respectively the inverter and the grid phase.

The active power can be controlled by means of the difference between the grid phase and the converter phase

$$\delta = \theta - \theta_g \tag{5.7}$$

called power angle and can be controlled by the mechanical torque T_m. In order to have a stable working point $|\delta|$ must be lower than $\frac{\pi}{2}$.

The reactive power can be regulated by controlling E, that is proportional to $M_f i_f$.

In the next subsections the main operations of the Synchronverter are presented:

- Synchronisation
- Active and reactive power feeding
- Frequency regulation
- Voltage regulation

5.1.1 Synchronisation

In order to connect the converter to the grid without causing huge transitory currents the following two conditions must be satisfied

$$\begin{cases} E = V_g \\ \theta = \theta_g \end{cases} \tag{5.8}$$

meaning that both the active 5.5 and reactive power 5.6 are equal to zero. Therefore the synchronization of the Synchronverter consists in regulating the control signals $M_f i_f$ and $\dot{\theta}$ so that eq. 6.16 is satisfied.

This is achieved in the following way. A three phase virtual current i_s is generated from the voltage error between e, the voltage control signal, and the grid voltage v_g.

$$i_s = \frac{1}{Ls + R}(e - v_g) \tag{5.9}$$

This current acts both in the active power channel and in the reactive power channel.

In the active power channel the electrical torque calculated in eq. 5.2 is proportional to the current. A ΔT is produced in the frequency droop loop with droop coefficient D_p when the angular speed of the machine $\dot{\theta}$ is different from the reference angular speed θ_r. A PI controller is introduced to eliminate the error between the grid and the converter angular speed.

In the reactive power channel eq. 5.4 is proportional to the virtual current. The term $M_f i_f$ is the output of a feedback loop that controls the reactive power to be zero.

Since the virtual inductance L and resistence R are not physical, they can be chosen in a wide range. Small values lead to a fast transient with high virtual current, while big values lead to a softer transient. To small values lead to oscillations in the frequency estimated.

5.1.2 Active power control channel

The active power control channel is organised as a nested loop where the inner loop is the frequency droop control and the outer loop is the active power control. The feedback of the inner loop is the converter virtual angular speed. The outer loop feedback comes from the current i via the torque T_e. The time constant of the frequency droop loop is $\tau_f = \frac{J}{D_p}$. Since there is no delay involved τ_f can be chosen much smaller than for a real SG.

The active power is regulated by a virtual torque T_m that acts on the power angle δ. It can be calculated from the power command P_{set} as

$$T_m = \frac{P_{set}}{\dot{\theta}} \approx \frac{P_{set}}{\dot{\theta}_n} \tag{5.10}$$

where $\dot{\theta}$ is the machine angular speed and $\dot{\theta_n}$ is the nominal grid angular frequency.

Depending on the state of the Switch S_P the active power is controlled in the following two ways

- **P set mode** If the switch S_P is ON ΔT is controlled to be zero through the PI controller and hence the synchronverter electromechanical torque is equal to the virtual mechanical torque. The converter virtual angular speed is controlled as

  $$\dot{\theta} = \dot{\theta_r} = \dot{\theta_n} + \Delta\dot{\theta} \tag{5.11}$$

  where $\Delta\dot{\theta}$ is the output of the PI control and corresponds to the difference between the grid reference and actual angular speed. In this case the power

angle settles down to a constant value that corresponds to the set reference power.

- **Frequency support mode** If the switch S_P is off the PI controller does not participate to the control. The converter is operated in the frequency droop mode. The actual active power P is deviated from P_{set} according to the droop coefficient defined as

$$D_p = -\frac{\Delta T}{\Delta \dot{\theta}} \tag{5.12}$$

where $\Delta\dot{\theta}$ is the deviation between the converter angular speed and the nominal one. The synchronverter angular frequency become

$$\dot{\theta} = \Delta\dot{\theta} + \dot{\theta_n} \tag{5.13}$$

that is equal to the corresponding one in the P set mode but with a different $\Delta\theta$.

In both the functioning modes the converter virtual angular speed converges to the grid angular speed if $|\delta| < \frac{\pi}{2}$. In fact, considering that the dynamics of the frequency loop are way faster than the voltage loop ones, the $M_f i_f$ term can be considered constant. The delivered active power and the electromechanical torque T_e are proportional to $\sin\delta$. When the grid frequency $\dot{\theta_g}$ decreases delta increases and the power angle δ increases, consequently T_e increases making the term that goes to the integrator smaller. This reduces the converter virtual angular speed. This process continues until $\dot{\theta} = \dot{\theta_g}$. The same process happens when the frequency of the grid increases. This result make the synchronverter intrinsically stable and permits to avoid the need of a grid phase reference as input.

5.1.3 Reactive power control channel

The control of the reactive power flowing out of the converter is done with a nested loop where the internal control is the voltage droop with the grid voltage amplitude V_g as feedback. Note that neglecting the LC filter the amplitude of the grid voltage is

$$V_g = \dot{\theta} M_f i_f. \tag{5.14}$$

The outer loop is the reactive power control with the calculated reactive power from eq.5.4 as feedback.

The voltage tracking error is multiplied by the voltage drooping coefficient D_q defined as

$$D_q = -\frac{\Delta Q}{\Delta v}. \tag{5.15}$$

The output signal is then added to the tracking error between Q_{set} and Q and integrated with gain $1/K$ to create the signal $M_f i_f$.

The time constant of the voltage loop can be estimated as

$$\tau \approx \frac{k}{\dot{\theta} D_q}. \tag{5.16}$$

Depending on the state of the switch S_q the voltage droop loop can be activated and deactivated and the following two operations mode are achieved:

- **Q set mode** With S_q off the $M_f i_f$ term is generated by the integration, with gain $1/K$, of the term $Q_{set} - Q$. In this case the reactive power generated follows the set value without any error.
- **Voltage support mode** If the voltage droop is activated the reference reactive power becomes $Q_{set} + (V_n - V_g) D_q$. Hence the the reactive power Q does not track Q_{set} but takes in account the variation of the grid voltage from its reference value.

6 Simulations

In this chapter the simulation results of the three topologies of SST studied in this thesis are presented. Firstly voltage levels adopted for the different stages of the SSTs are presented, then a comparison based on the DC ripple and the AC THD is done and finally, three different possible scenarios are presented: namely, SST operating with LV AC grid working in off-nominal conditions, feeding a DC CPL and MV grid supporting.

In the simulations SSTs are always controlled with IDA-PBC apart the MV converter in the grid supporting scenario, that is controlled using the synchronverter approach.

6.1 Voltage Levels

For this case of study the MV and LV grids line to line voltages are assumed to be respectively 15kV and 400V.

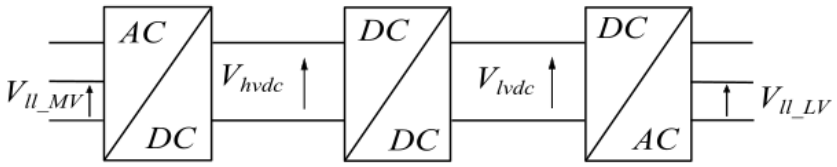


Figure 6.1: SST Topology

•	V_{llMV}	V_{MVDC}	V_{LVDC}	V_{llLV}
Voltage [V]	15000	30000	800	400

Table 6.1: voltage values

The converter should work in the linear zone, meaning that the modulation index (MI) m_a should be lower than 1. Choosing a MI of 0.8 and knowing that the LV grid has a $V_{ll} = 400V$ the LVDC voltage can be determined with eq. 6.1.

$$V_{LVDC} = \frac{2\sqrt{2}}{\sqrt{3}} \frac{V_{ll}}{m_a} \tag{6.1}$$

The resulting voltage is $V_{LVDC} \simeq 816V$, approximate to the standardised 800 V.

By applying the same procedure to the MV side converter, the adopted MV DC bus voltage is 30kV.

The switching frequency is 1kHz for the DABa and 5kHz for the AC/DC converters.

6.2 Comparison between the LV DC bus dynamics of T1, T2 and T3

In Fig.6.2 are shown the LV DC bus voltages of the three topologies presented in this thesis when a step load of 1MW is performed on the LV AC side. The SSTs are operating in step-Down mode. All the three topologies have the same virtual damping resistance of 10Ω for the DAB control and the LV DC link capacitors shown in Tab.6.2. The lowpass filter used for the voltage and current signals is a Butterwoth second order low-pass filter with a passband edge frequency of 3000 rad/s and is the same for the three DC/DC converters. As expected the dynamics are faster for T3, because the DC capacitance is the smallest.

The steady state error that is present after the transient is eliminated by an integrator term that has a much lower dynamics respect to the IDA-PBC DAB and therefore its effect is not visible in the proposed graph.

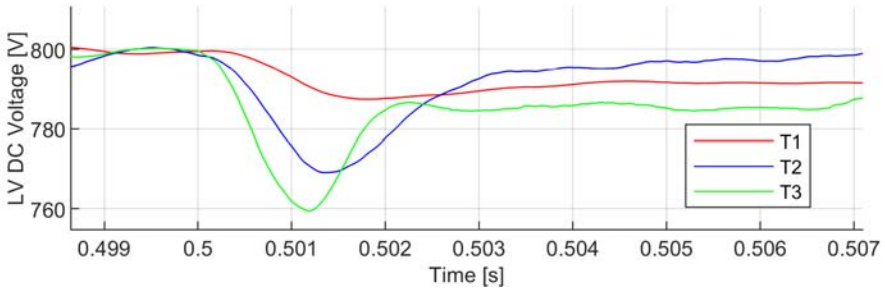


Figure 6.2: LV DC Bus of T1, T2 and T3 when a 1MW load step is performed on the LV AC side. r=10

6.3 Comparison between the three different topologies using IDA-PBC 5MW SST

All the three topologies are tested both in step-Up and in step-Down mode. The simulation is performed with a series of five load steps of 1MW, in order to get the nominal power of 5MW. The capacitor size is chosen in order to guarantee a max voltage ripple of 3% on MV side and 10% on LV side.

In table 6.2 are shown the values of the capacitors calculated with the method presented in section 3.2.

Topology	MV Cap [μF]	LV Cap [mF]
T_1	90	38
T_2	35	10
T_3	20	5

Table 6.2: Theoretical Capacitance values for the three different topologies

This capacitor values satisfies the equations when the converters are simulated alone, feeding a grid or a CPL, but are not when two converters work together sharing the same DC bus, as will be clear from the next subsections. This is caused mainly by slow oscillations, at grid frequency, caused by the LV rectifier. It is possible therefore to divide the ripple components in two parts, one caused by the switching operation and one related to the control uncertainties. This is the reason why the same topology, depending on the operation mode, in step up or step down mode, shows different DC voltage ripple. In the following simulations the capacitor sizes differs in step-Up and step-Down mode, in order to achieve always a compatible ripple and to emphasise the contribution of the control on the DC ripple. In particular the IDA-PBC control of the rectifier is very delicate. The reference current is calculated through a non linear equation with a root square term. The square root limits the range of the damping factor R_3 that, if chosen to big, does not guarantee a real solution.

6.3.1 T1

In this subsection the first topology T1 is simulated both in step-Up and step-Down mode. In Tab.6.3 are shown the parameters used in the simulations.

Parameter	Value
L_t	5 mH
fs_{DAB}	1 kHz
$fs_{AC/DC}$	5 kHz

Table 6.3: Parameters of SST 1

Step Down

In Fig.6.3 are presented the simulation results of the SST T1 operating in step down mode. A step load is made every 50s starting at t=0.2s. The LV converter is controlled as grid forming inverter and the MV converter works as rectifier. The capacitor size needed to achieve a voltage ripple compatible with the design power DC quality constrains, i.e. 900V oon the MV side and 80V on the LV side, are $C_{MV} = 80\mu F$ $C_{LV} = 30F$. Comparing it with the theoretical calculated values, $C_{MV_{calculated}} = 90F$ and $C_{LV_{calculated}} = 38F$ it can be seen that the values are coherent

with mathematical model. The THD injected in the MV and LV AC grid are respectively 2.78% and 1.71%, respecting the power quality requirements.

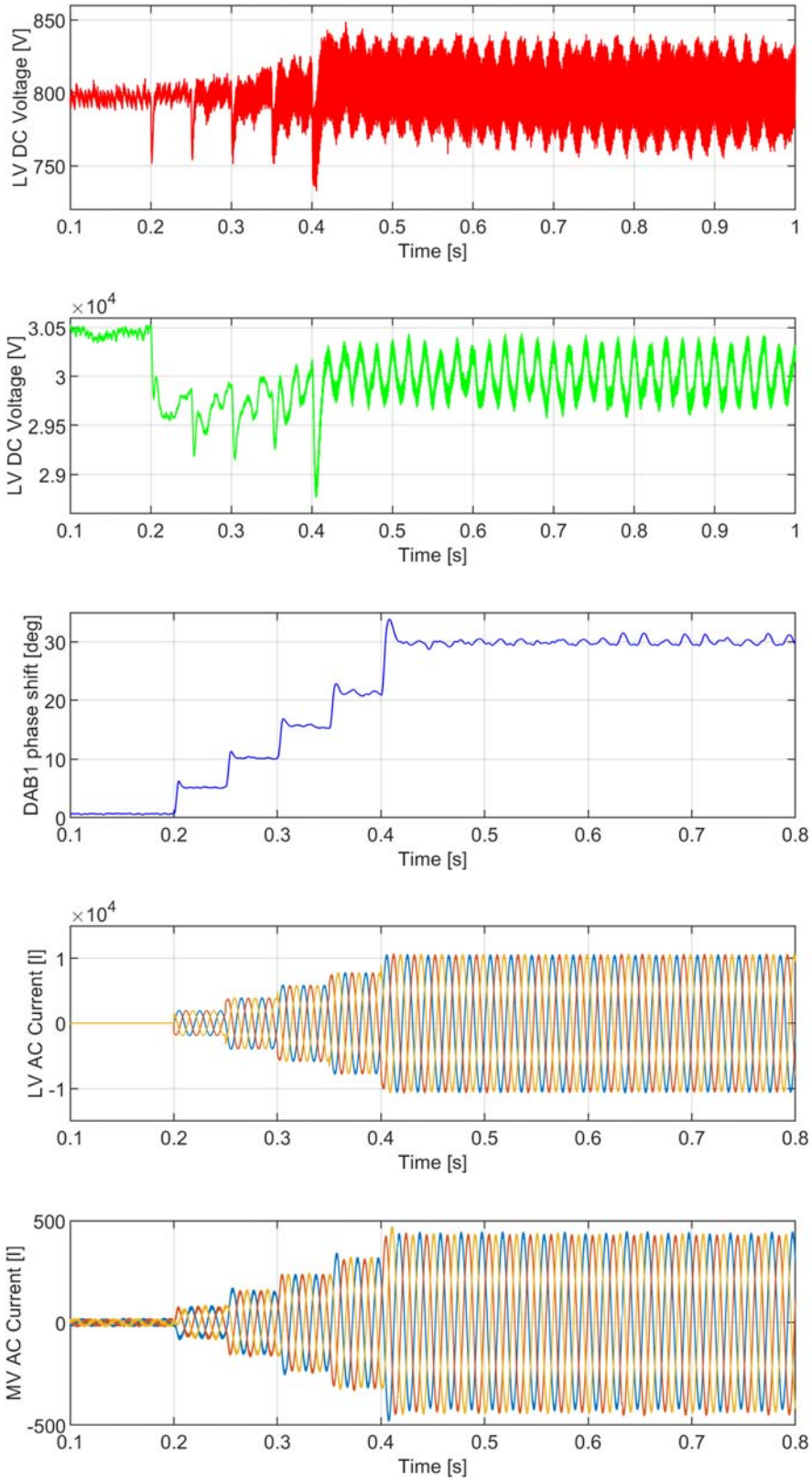


Figure 6.3: Simulation results of T1 SST controlled with IDA-PBC working in step down mode. ($MV_{Cap} = 80\mu F$, $LV_{cap} = 30mF$, $MV_{THD} = 2.78\%$, $LV_{THD} = 1.71\%$)

Step Up

In Fig.6.4 are presented the simulation results of the SST T1 operating in step-Up mode. A step load of 1MW is made at $t = 0.3, t = 0.5, t = 0.6, t = 0.7$ and $t = 0.8$. The MV converter is controlled as grid feeding inverter and the power regulated through the inductor current channel. Thr LV converter works as rectifier. The capacitor size needed to achieve a voltage ripple compatible with the design power DC quality constrains, i.e. 900V oon the MV side and 80V on the LV side, are $C_{MV} = 180\mu F$ $C_{LV} = 90F$. Comparing it with the theoretical calculated values, $C_{MV_{calculated}} = 90F$ and $C_{LV_{calculated}} = 38F$ it can be seen that the values are almost double the theoretical values. Among others, the LV rectifier is the principal cause. As said before, big values of the damping coefficient R3 brings to a negative square root term. This limits the tuning possibilities of the control and brings to a bigger steady state error. Therefore an integrator is added to the control to reach the reference voltage. The THD injected in the MV and LV AC grid are respectively 1.83% and 11%. The power quality requirements are not respected on the LV side.

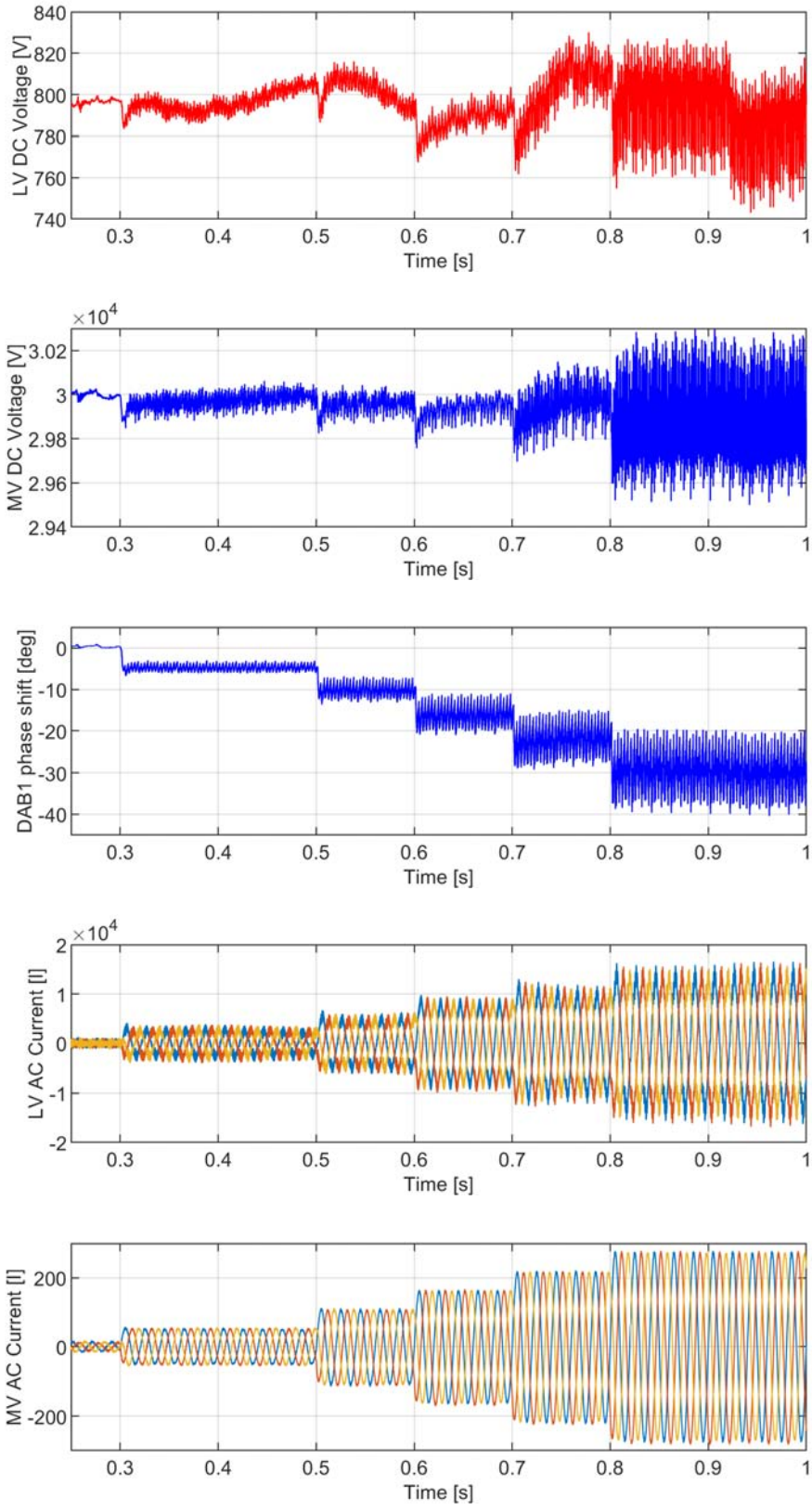


Figure 6.4: Simulation results of T1 SST controlled with IDA-PBC working in step up mode. ($MV_{Cap} = 180\mu F$, $LV_{cap} = 90mF$, $MV_{THD} = 1.83\%$, $LV_{THD} = \%11$)

6.3.2 T2

In this subsection the simulation result of the second topology T2 is presented. The same approach of the previous subsection is adopted.

The design parameters of T2 are shown in Tab.6.4.

Parameter	Value
L_t	7.5 mH
fs_{DAB}	1 kHz
$fs_{AC/DC}$	5 kHz

Table 6.4: Parameters of SST 1

Step Down

In fig.6.5 the simulation results of T2 operating in step down mode are shown. The capacitance needed to maintain the DC ripple within the limits are $C_{MVDC} = 60\mu F$ and $C_{LVDC} = 10F$. The theoretical capacitance values are $C_{DCMV} = 35\mu F$ and $C_{DC}LV = 10F$. The LV side capacitor perfectly matched the theoretical one, while the MV side capacitor is almost two times its theoretical value. The THD injected in the MV and LV AC grid are respectively 2.70% and 1.66%, respecting the power quality requirements.

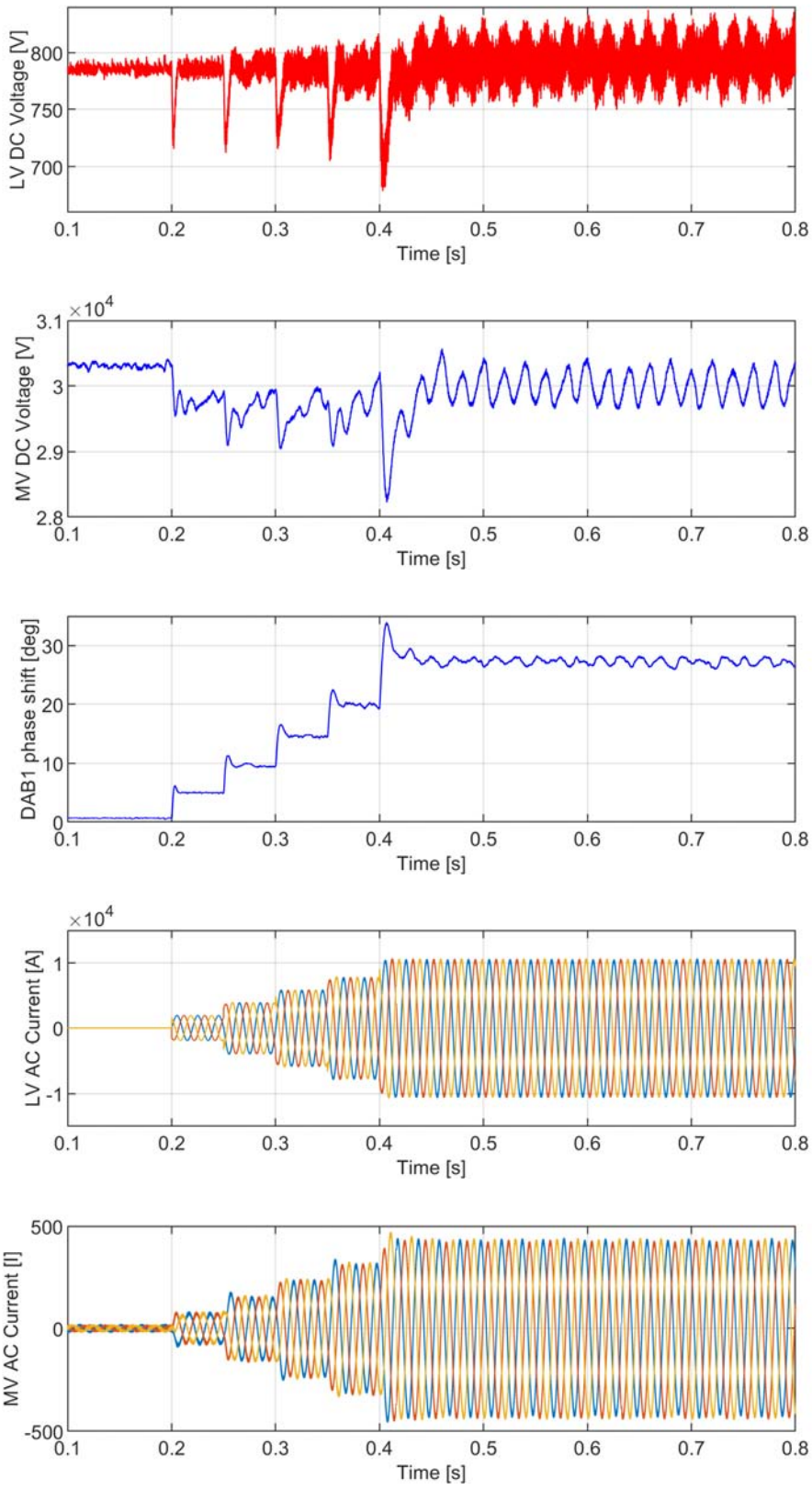


Figure 6.5: Simulation results of T2 SST controlled with IDA-PBC working in step down mode. ($MV_{Cap} = 60\mu F$, $LV_{cap} = 10mF$, $MV_{THD} = 2.70\%$, $LV_{THD} = 1.66\%$)

Step Up

In Fig. 6.6 the simulation results of T2 operating in step up mode are shown. The capacitance needed to maintain the DC ripple within the limits are $C_{MVDC} = 35\mu F$ and $C_{LVDC} = 10F$. The theoretical capacitance values are $C_{DCMV} = 35\mu F$ and $C_{DCLV=15F}$. This time the MV side capacitor perfectly matched the theoretical one, while the LV side capacitor need to be bigger than its theoretical value. The THD injected in the MV and LV AC grid are respectively 1.74% and 6%. Also for this topology the LV side rectifier controlled with IDA-PBC can not guarantee the power quality requirements.

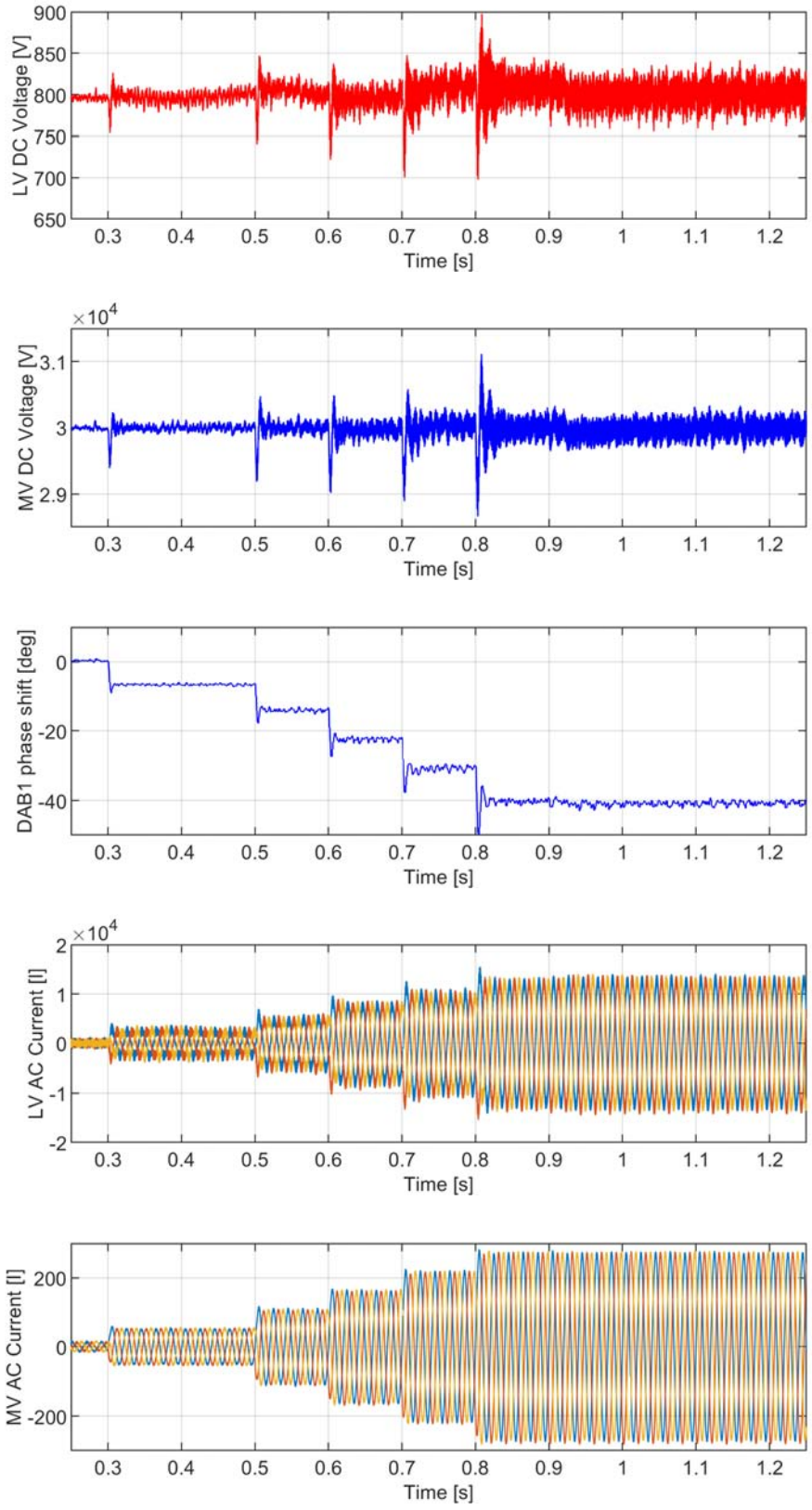


Figure 6.6: Simulation results of T2 SST controlled with IDA-PBC working in step up mode. ($MV_{Cap} = 35\mu F$, $LV_{cap} = 15mF$, $MV_{THD} = 1.74\%$, $LV_{THD} = 6\%$)

6.3.3 T3

In this subsection the simulation results of the third topology T3 are presented. The load is the same of the other two topologies. The design parameters of T3 are shown in Tab.6.5.

Parameter	Value
L_t	$7\ mH$
fs_{DAB}	$1\ kHz$
$fs_{AC/DC}$	$5\ kHz$

Table 6.5: Parameters of SST 1

Step Down

In fig.6.7 the simulation results of T3 operating in step down mode are presented. The capacitance needed to maintain the DC ripple within the limits are $C_{MVDC} = 40\mu F$ and $C_{LVDC} = 9.5F$. The theoretical capacitance values are $C_{DCMV} = 20\mu F$ and $C_{DCLV=5F}$. Both the adopted capacitors have a value that is two times its theoretical value. The THD injected in the MV and LV AC grid are respectively 1.88% and 1.25%, respecting the power quality requirements.

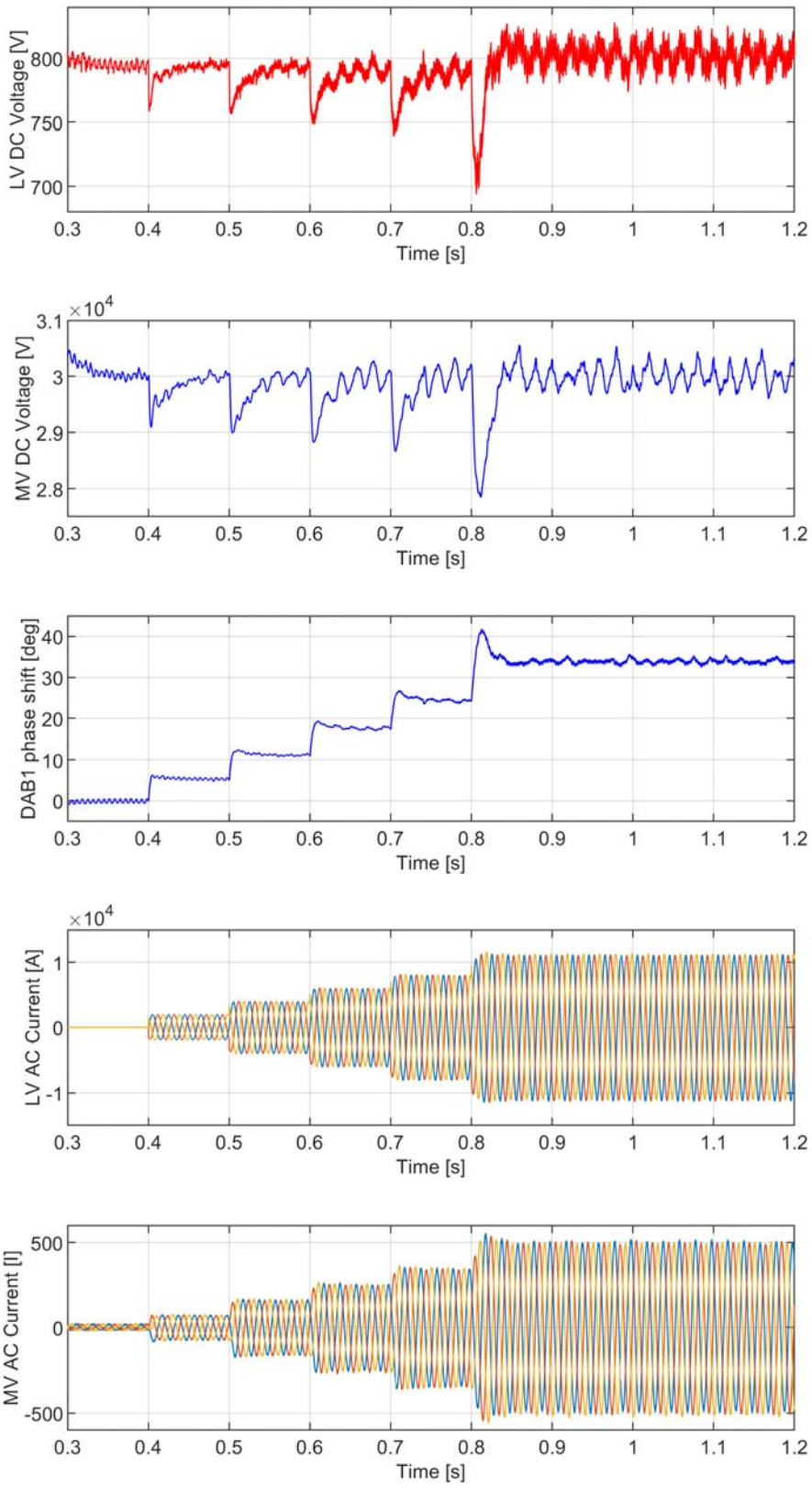


Figure 6.7: Simulation results of T3 SST controlled with IDA-PBC working in step down mode. ($MV_{Cap} = 40\mu F$, $LV_{cap} = 9.5mF$, $MV_{THD} = 1.88\%$, $LV_{THD} = 1.25\%$)

Step Up

In fig.6.8 the simulation results of T3 operating in step up mode are presented. The capacitance needed to maintain the DC ripple within the limits are $C_{MVDC} = 40\mu F$ and $C_{LVDC} = 7F$. The theoretical capacitance values are $C_{DCMV} = 20\mu F$ and $C_{DCLV=5F}$. As for the step-Down simulation the theoretical capacitance underestimate the ripple both for LV and MV. The THD injected in the MV and LV AC grid are respectively 1.4% and 4.96%. Also for this topology the LV side rectifier controlled with IDA-PBC can not guarantee the power quality requirements. As it is said at the beginning of this section, the LV rectifier control could not be optimized since the damping factor R3 need to be bounded to a low value. The same control applied to the MV rectifier was implemented with good results.

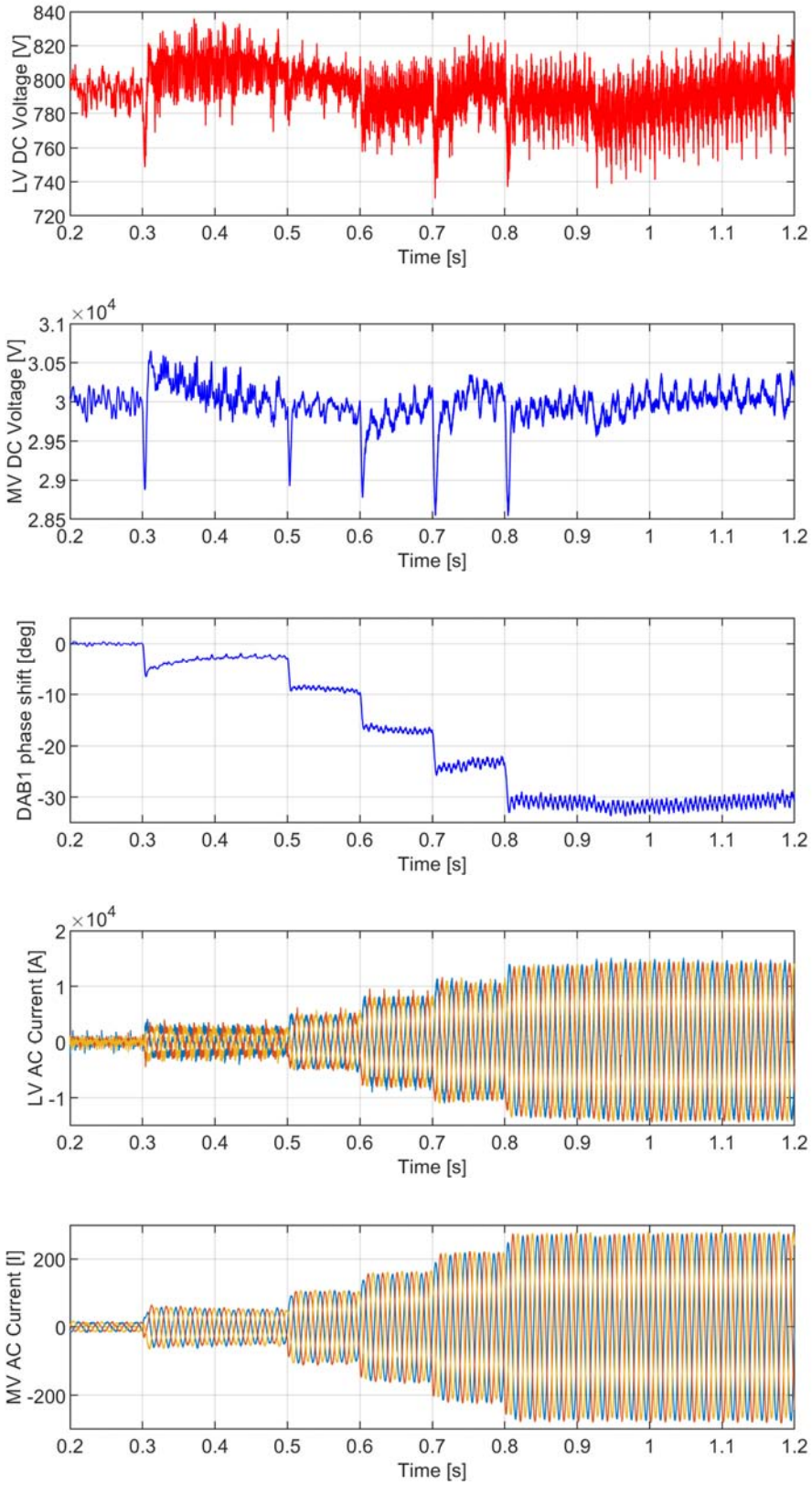


Figure 6.8: Simulation results of T3 SST controlled with IDA-PBC working in step up mode. ($MV_{Cap} = 40\mu F$, $LV_{cap} = 7mF$, $MV_{THD} = 1.4\%$, $LV_{THD} = 4.96\%$)

6.3.4 Conclusions

In this section the three topology have been compared. In Tab.6.6 are shown the capacitance values and the THD of the three topologies when operating both in step-up and step-down mode. Both the THD and the capacitance required decrease passing from T1 to T2 and T3. The biggest difference is between T1 and T2 where the capacitors size needed is more than a half.

While all the step down topologies where able to operate with a THD under the 3%, none of the step up topologies could guarantee a proper power quality to the LV AC grid. This is due to the behaviour of the LV rectifier control and in particular to the reference current formula where the damping factor R3 acts through a square root term that must be positive to have a real solution. For this reason, applying the control with the LV parameters, the choice of R3 needed to be bounded to very low values that led to a noisy signal. On the contrary, to small R3 should corresponds high R1 and R2, meaning that the noise of the reference current is amplified. As a result wasn't possible to get a good result for the LV THD when the SST is working in step up mode. This can be solved as future work by changing the interconnection and damping matrix in order to get a different formulation for the reference current.

Since the third topology results to be the most performing one, in terms of THD and capacitor size, it is adopted for the scenarios presented in the next two sections.

Topology	Operation Mode	C MV DC [μF]	C LV DC [mF]	MV THD [%]	LV THD [%]
T1	step down	80	30	2.78	1.71
T1	step up	180	90	1.83	11
T2	step down	60	10	2.70	1.66
T2	step up	35	15	1.74	6
T3	step down	40	9.5	1.88	1.25
T3	step up	40	7	1.4	4.96

Table 6.6: Comparison between T1, T2,T3.

6.4 Scenario 1: SST T3 operating with off nominal LV conditions

6.4.1 Voltage magnitude step

One of the advantages offered by using a SST instead of a traditional transformer is that it decouples the grids at the two sides completely, both from a voltage point of view and from a frequency point of view. This has the advantage that a disturbance on one side is not transmitted to the other side. In this section a scenario where the T3 SST is operated in step up mode and the LV grid is in off-nominal conditions is analysed. Four simulations are performed, with a positive and negative step in

the voltage magnitude and in the frequency. The maximum variation admitted in the actual European grid is $\pm 10\%$ for the voltage magnitude and $\pm 0.25 Hz$ for the frequency. For the magnitude a step of $\pm 30\%$, even if it is way to large for a steady state situation, it could happen during a start up of a big electrical machine, especially in the case of micro LV grids.

Positive step

In this subsection a positive step of the LV grid magnitude is performed when the SST T3 feeds a 5MW resistive load. A positive step of $0.3 p.u.$ is done through a simscape programmable voltage source block between $t = 1.5s$ and $t = 3.5s$. The simulation results are reported in Fig. 6.9. As it can be seen both the DC buses reacts to the magnitude step with an over voltage, of 12.5%for the LV DC bus and 3.3% for the MV DC bus. The overshoot can be reduced by adopting bigger capacitors. On the MV AC side the current has an overshoot smaller than 1%.

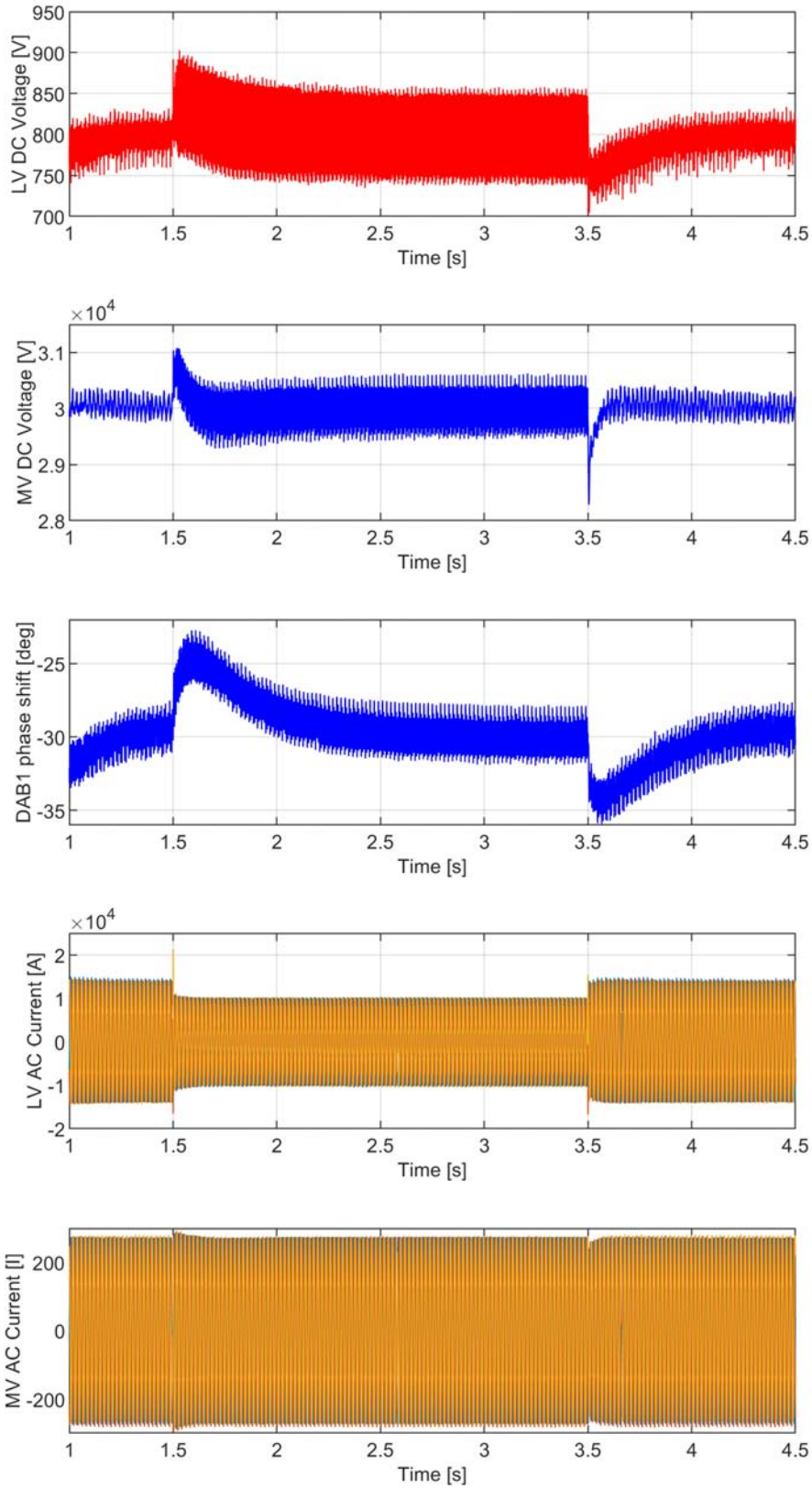


Figure 6.9: Simulation results of T3 SST controlled with IDA-PBC working in step up mode. A LV magnitude step of +0.3pu is performed between 1.5s and 3.5 s ($MV_{Cap} = 40\mu F$, $LV_{cap} = 7mF$, $MV_{THD} = 1.4\%$, $LV_{THD} = 4.96\%$)

Negative step

In this subsection a negative step of the LV grid magnitude is performed when the SST T3 feeds a 5MW resistive load. A negative step of $0.3p.u.$ is done through a simscape programmable voltage source block between $t = 1.5s$ and $t = 3.5s$. The simulation results are reported in Fig. 6.10. As it can be seen both the DC buses reacts to the magnitude step with an under voltage, of 22.5% for the LV DC bus and 7% for the MV DC bus. When the LV grid magnitude is stepped back to the nominal value an overshoot of 10% takes place both on the MV and LV DC bus.

On the MV AC side the current has an undershoot and an overshoot smaller than 1%.

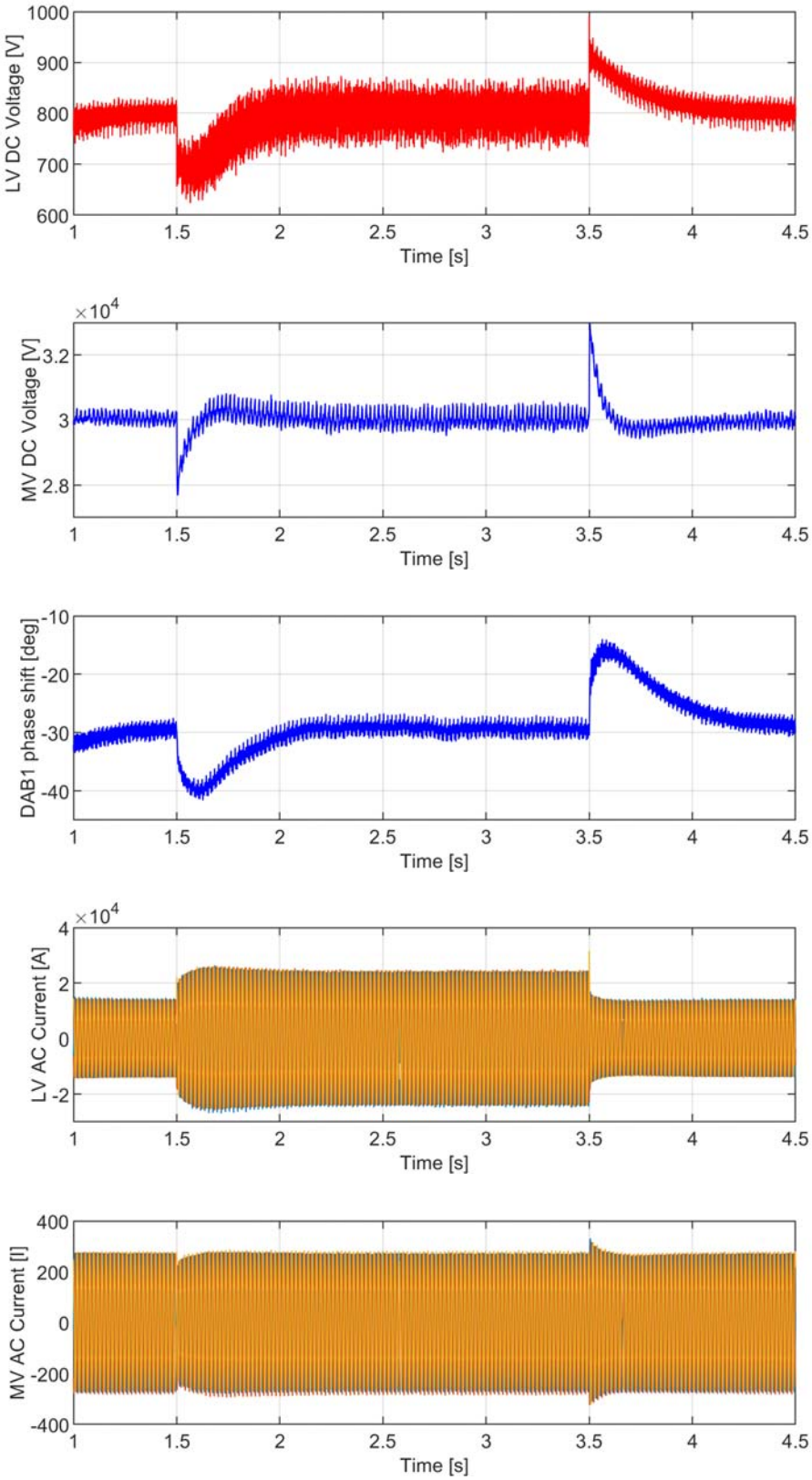


Figure 6.10: Simulation results of T3 SST controlled with IDA-PBC working in step up mode. A LV magnitude step of -0.3pu is performed between 1.5s and 3.5 s ($MV_{Cap} = 40\mu F$, $LV_{cap} = 7mF$, $MV_{THD} = 1.4\%$, $LV_{THD} = 4.96\%$)

6.4.2 Frequency step

In this subsection the simulation results of a positive and negative step of the LV grid frequency are presented.

Positive step

In this simulation the LV grid frequency is stepped up by $0.25Hz$, from $t = 1.5s$ to $t = 4s$. How it can be seen from Fig.6.11 after the frequency variation the LV rectifier input current oscillates. This reflects in to an oscillation both on the LV DC bus and on the MV DC bus. The oscillation is not damped and seems to continue also in steady state.

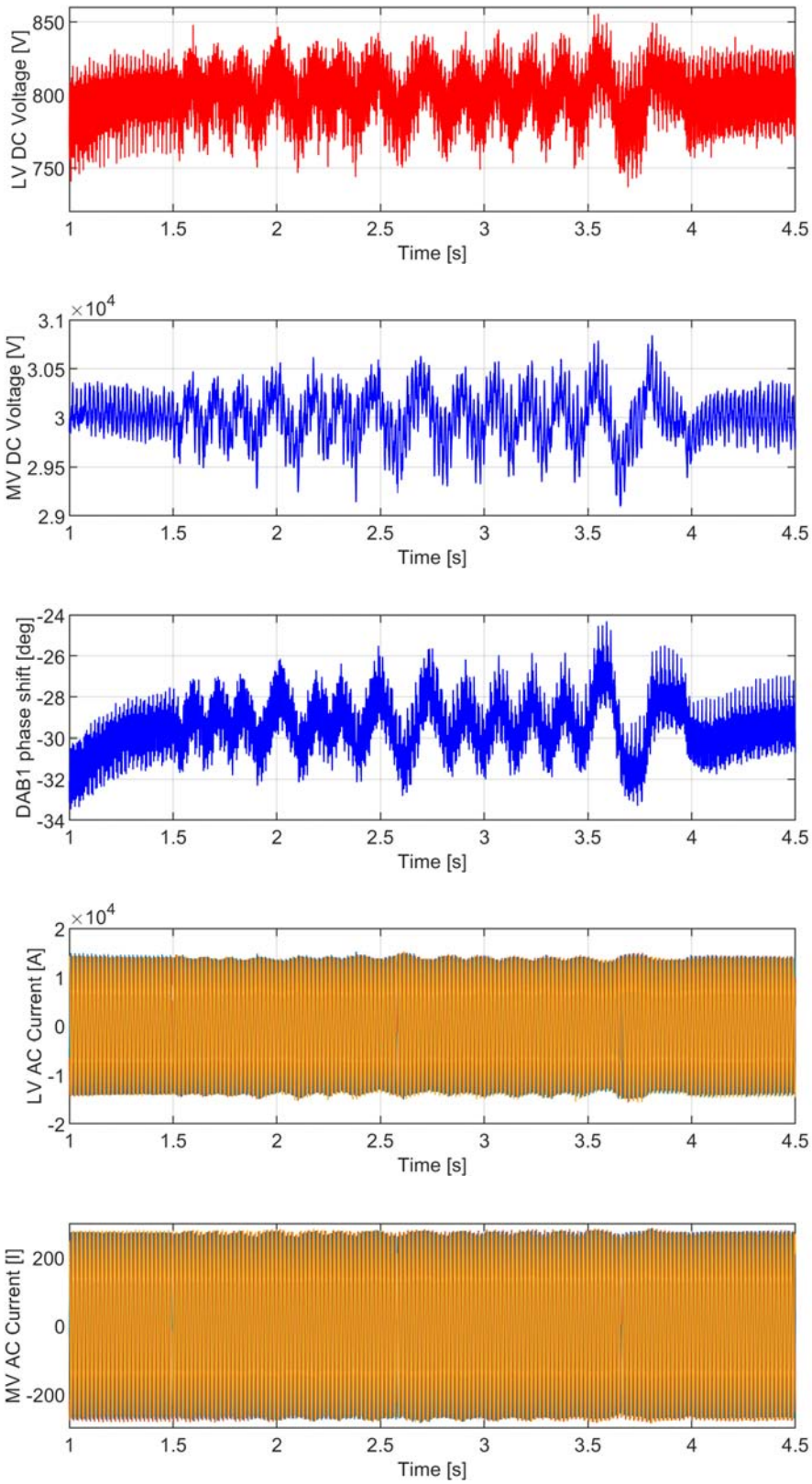


Figure 6.11: Simulation results of T3 SST controlled with IDA-PBC working in step up mode. The LV frequency is varied with a positive step of +0.25Hz,between 1.5s and 3.5 s ($MV_{Cap} = 40\mu F$, $LV_{cap} = 7mF$, $MV_{THD} = 1.4\%$, $LV_{THD} = 4.96\%$)

Negative step

In this simulation the LV grid frequency is stepped down by $-0.25Hz$, from $t = 1.5s$ to $t = 4s$. How it can be seen from Fig.6.11 after the frequency variation the LV rectifier input current oscillates. This reflects in to an oscillation both on the LV DC bus and on the MV DC bus. In this case the current oscillation decrease and become very low in steady state ($t = 3s$).

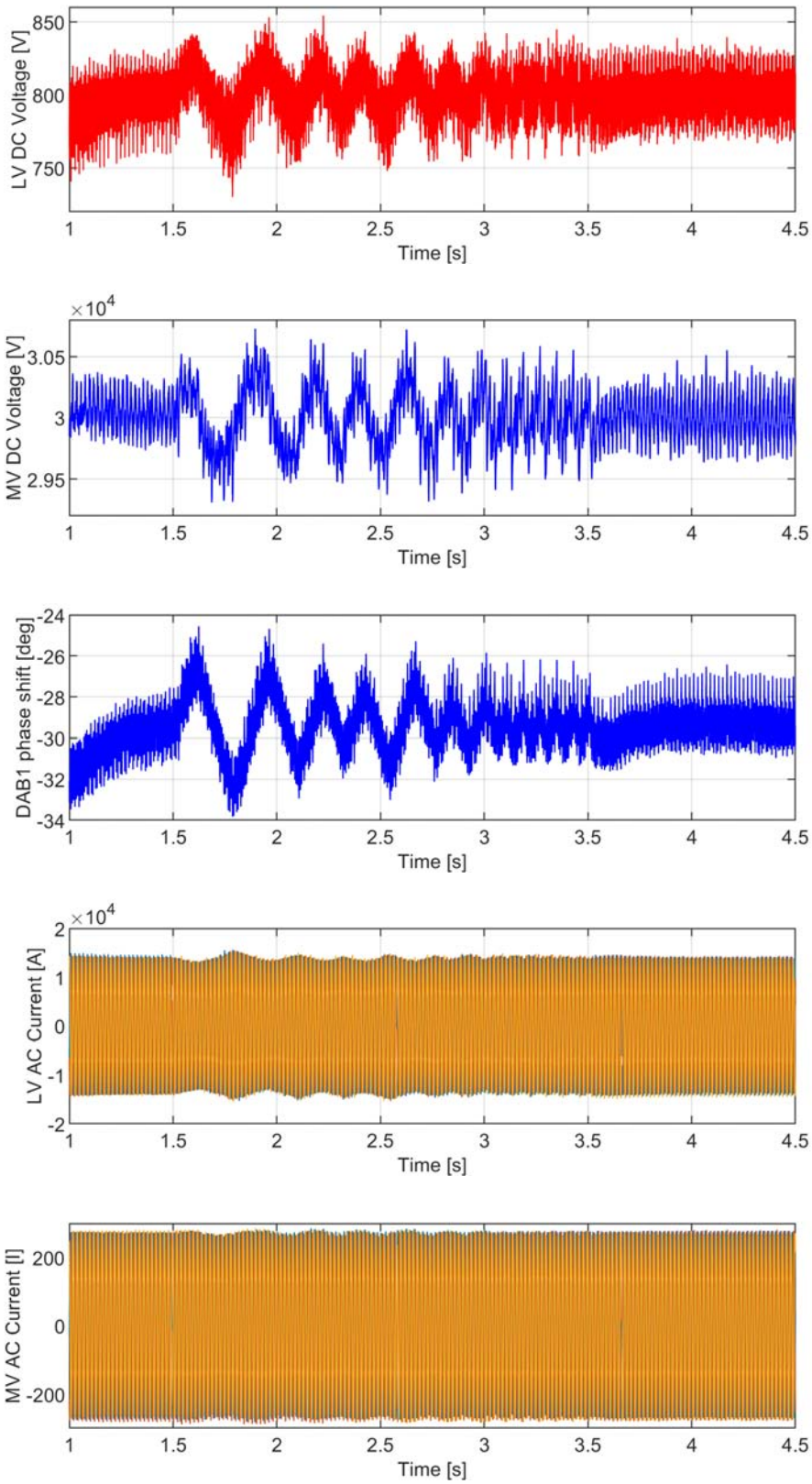


Figure 6.12: Simulation results of T3 SST controlled with IDA-PBC working in step up mode. The LV frequency is varied with a negative step of -0.25Hz,between 1.5s and 3.5 s ($MV_{Cap} = 40\mu F$, $LV_{cap} = 7mF$, $MV_{THD} = 1.4\%$, $LV_{THD} = 4.96\%$)

6.5 Scenario 2: DC bus power supply

In this Scenario it is analysed the behaviour of the SST T3 when feeding at the same time the LV AC grid and a DC constant power load (CPL) connected to the MV and LV DC bus. The CPL can be an energy storage unit or a DC connecting another substation. Since the T£ toology naturally offers a neutral point on the DC buses, the CPL are connected with a bipolar scheme. Therefore two CPLs are connected to each DC bus, between the positive and neutral point and between the negative and neutral point offered by the three level topology.

The simulation is performed as follows:

- At t=0.3 , t=0.5 and t=0.7 a 1MW resistive load is added on the LV AC side (3MW in total).

- Between t=1.5 and t=3 a 2MW CPL is fed through the LV DC bus

- Between t=3.5s and t=4.5s a 2MW CPL is fed through the MV DC bus

6.5.1 2MW CPL LV

In Fig.6.13 the simulation results of the SST feeding a bipolar CPL on the LV side is presented. The SST present a stable operation and the power quality requirements are guarantee.

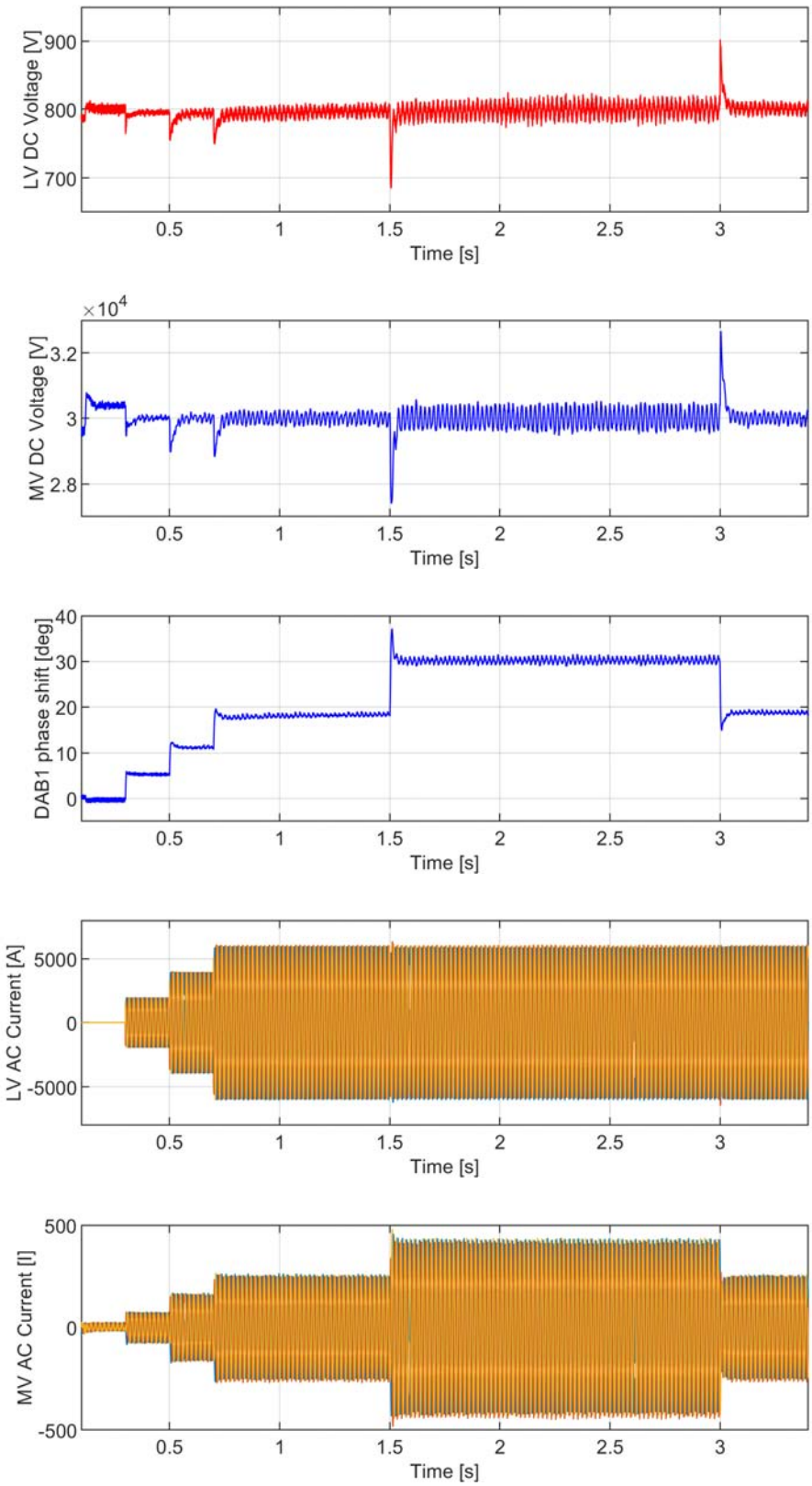


Figure 6.13: Simulation results of T3 SST controlled with IDA-PBC working in step down mode. A 3MW LV AC resistive load is fed. At 1.5s a 2MW CPL is connected to the LV DC bus. ($MV_{Cap} = 40\mu F$, $LV_{cap} = 9.5mF$)

6.5.2 2MW CPL MV

In Fig.6.14 the simulation results of the SST feeding a bipolar CPL on the MV side is presented. The SST present a stable operation and the power quality requirements are guarantee.

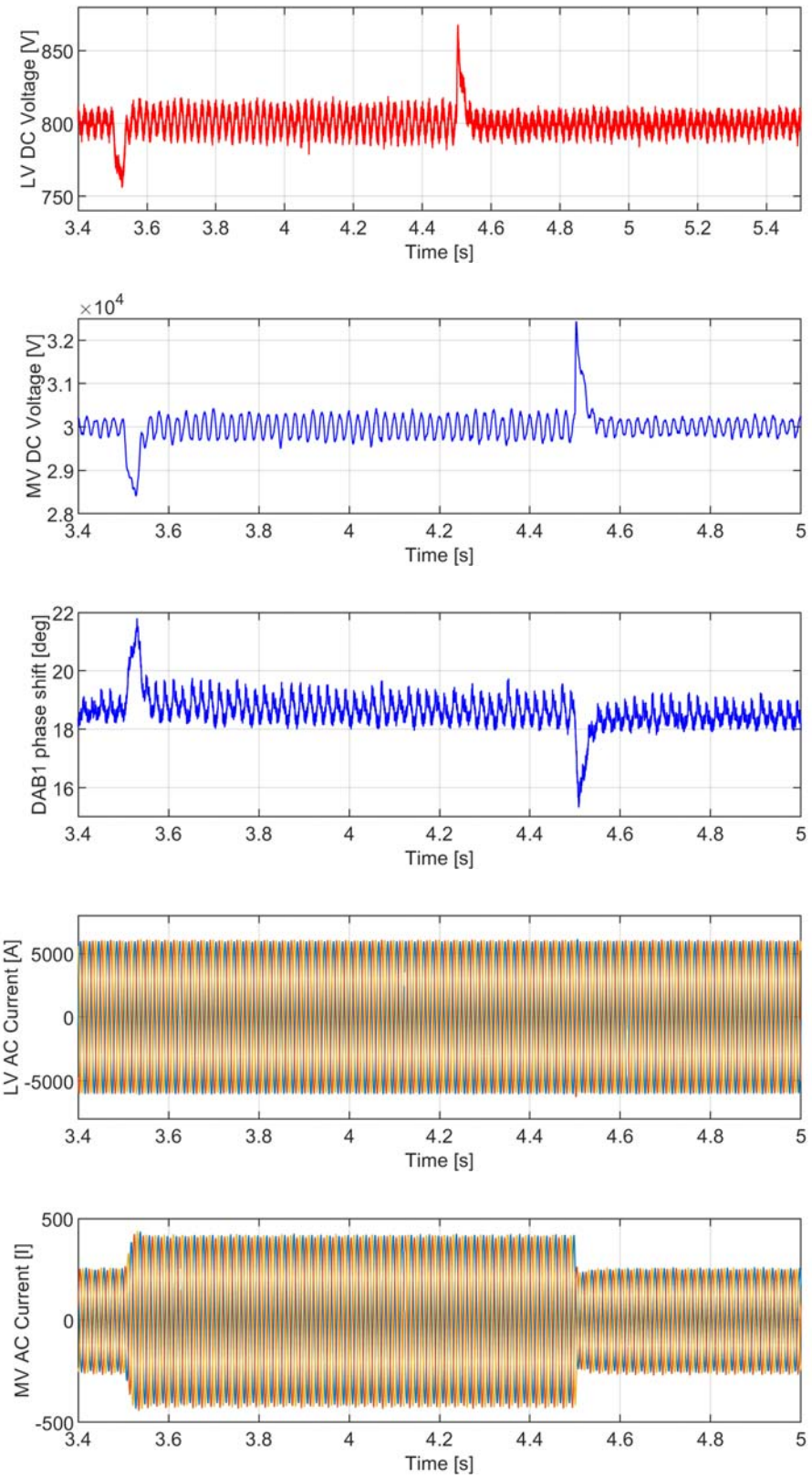


Figure 6.14: Simulation results of T3 SST controlled with IDA-PBC working in step down mode. A 3MW LV AC resistive load is fed. At 3.5s a 2MW CPL is connected to the MV DC bus. ($MV_{Cap} = 45\mu F$, $LV_{cap} = 12.5mF$)

6.6 Scenario 3: MV grid supporting

In this section a scenario where the Synchronverter described in section5.1 is substituted to the MV converter is presented. This solution permit to operate the SST in a way that supports the MV grid both through voltage and frequency regulation. The model is presented for the Step-up mode. The same approach can be applied also to the Step-down mode, making the MV converter behave like a synchronous motor. For lack of time this application is left as future work.

The T3 SST showed grid current unbalance and therefore was not used for this application. The T1 of SST is used instead. The cause of the current unbalances could not be defined and is also left as future work.

In Tab.6.7

Parameter	Value
D_p	2026
J	3.3
τ_f	0.002
D_q	796
K	50000
τ_v	0.2
P	$1e^{-6}$
I	0.005

Table 6.7: Parameters of Synchronverter

The electrical torque T_e and the back electromotive force $M_f i_f$ are both filtered with a eight order filter. This limits the oscillations of the angular speed of the machine.

The simulation is performed in order to test all the functioning modes (synchronisation, power set mode, frequency regulation and voltage regulation), accordingly to the following schedule:

- **Pset, Qset mode** Dq switch is off and Dp is on. Grid side breaker is open. Grid voltage frequency and magnitude are nominal
- **t=0** Synchronisation starts
- **t=2** Closure of the grid breaker
- **t=2.3** Active Power set to 5MW
- **t=3.5** Active power set to 3MW
- **Frequency regulation mode** Dq and Dq switches are off
- **t=4** Grid frequency step of -0.25Hz

- **t=5** Grid frequency step back to nominal
- **Voltage regulation mode** Dp switch is on and Dq switch is off
- **t=5.5** Amplitude of grid voltage step of -10%
- **t=6.5** Amplitude of grid voltage step back to nominal
- **t=7** Stop of the simulation

In Fig.6.15 both the active and reactive output power of the SST controlled as a Synchronverter are shown.

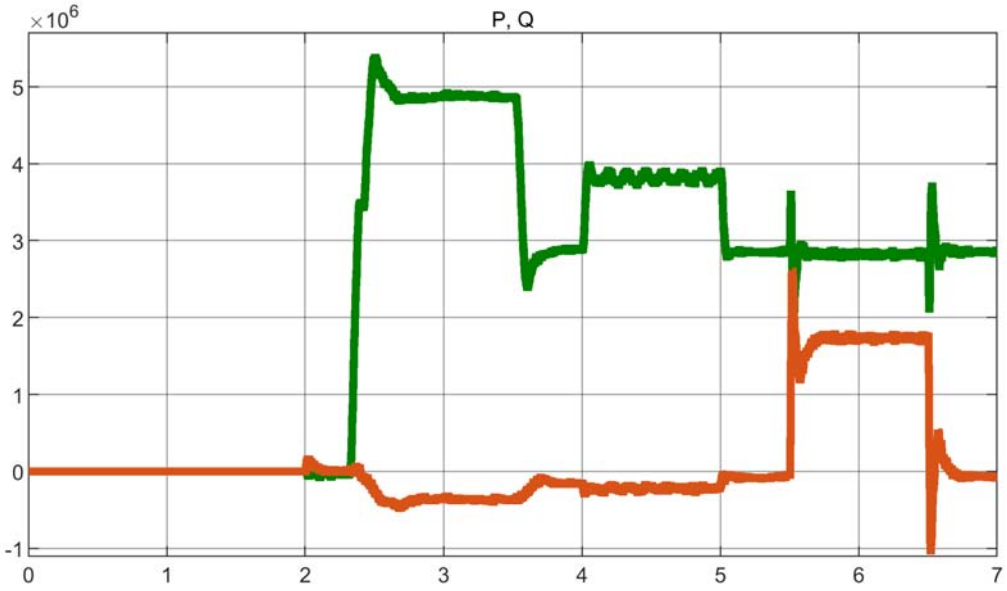
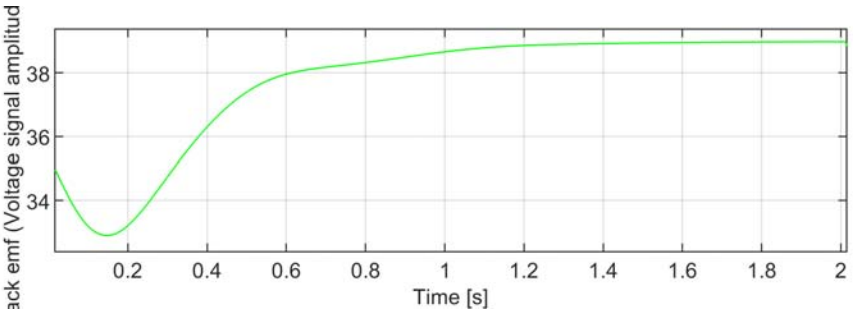


Figure 6.15: Active and reactive power generated from the synchronverter during the simulation

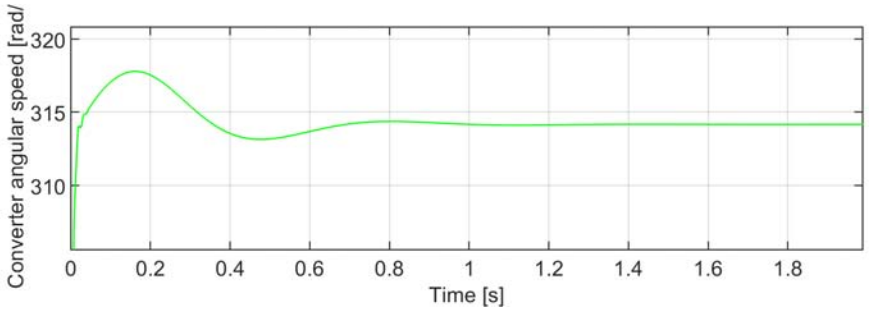
6.6.1 Synchronisation

Before to be connected to the grid the Synchronverter must be synchronised with the MV grid. It is done creating a virtual current that get minimised through the active and reactive control loops. When the virtual current goes to zero the back electromotive force approach the nominal value, equal to the peak value of the phase voltage of the grid divided by the angular rotor speed, and the angular speed approaches the grid angular speed. Depending on the virtual impedance parameters chosen the virtual current magnitude can be changed, making the process faster or slower. In this case the parameters chosen are $R_{virtual} = 10\omega$ and $L_{virtual} = 0.1H$.

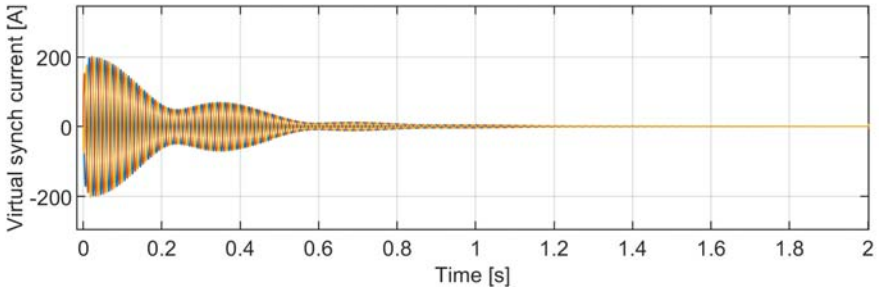
In Fig.6.16 the more significant signals are presented. In sub-figure (d) a detail on the phase synchronisation is shown. The grid phase is calculated with a phase lock loop (PLL).



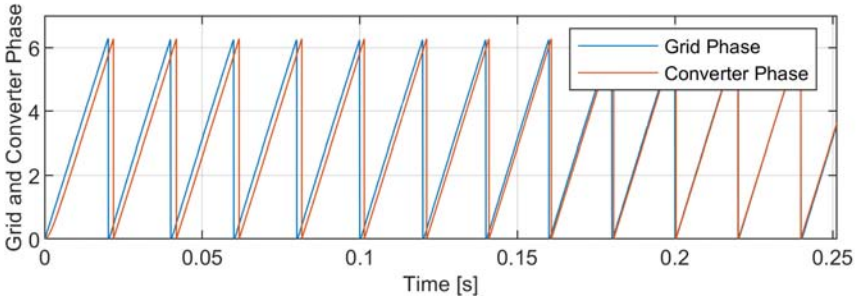
(a) Back emf



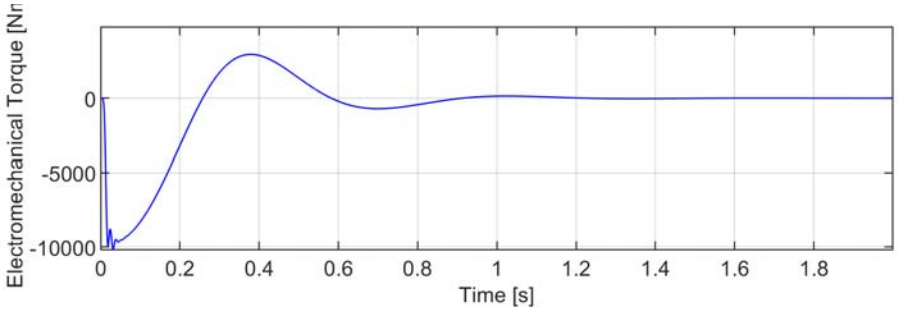
(b) Converter Angular Speed



(c) Synchronisation virtual current



(d) Converter and grid phase

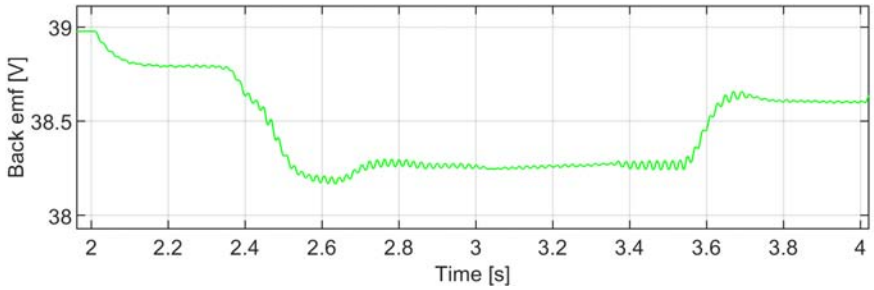


(e) Elechtromecanical Torque

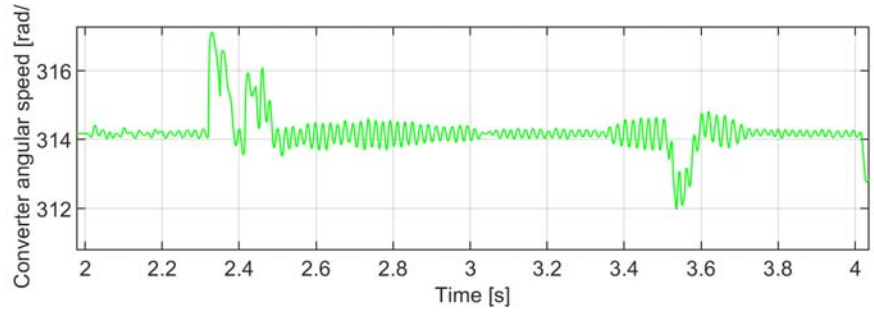
Figure 6.16: Simulation results of the synchronisation of the synchronverter with the grid

6.6.2 Pset, Qset mode

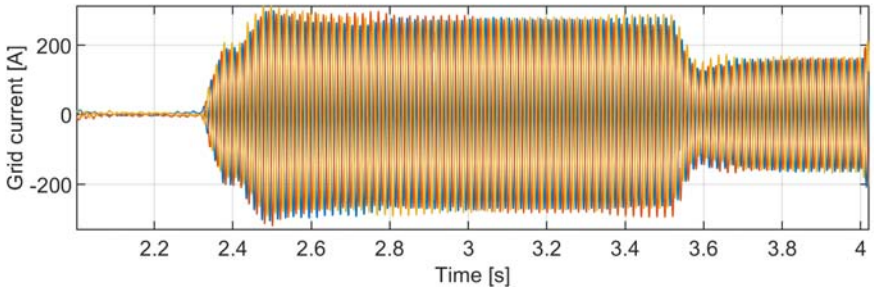
Active power is set to 5MW at $T = 2.3s$ and to 3MW at $t = 3.5s$. The reactive power reference is let to zero in order to have a unitary power factor. In this operation mode the synchronous machine does not react to off nominal voltage and frequency values but just follows the grid parameters. In Fig.6.17 the simulation results of the PQ set mode are presented. In sub-figure (d) a detail of the converter and grid phases is shown. The difference between the two angles is the synchronous generator power angle δ, through which the active power is controlled. The power angle has a vital role for the stability of the synchronverter. Its oscillations brings to current unbalances, as it can be seen from sub-figure (c,e). Since the oscillations of the angular speed are feed-forwarded to the loop through the electromechanical torque signal, it is difficult to damp this oscillations.



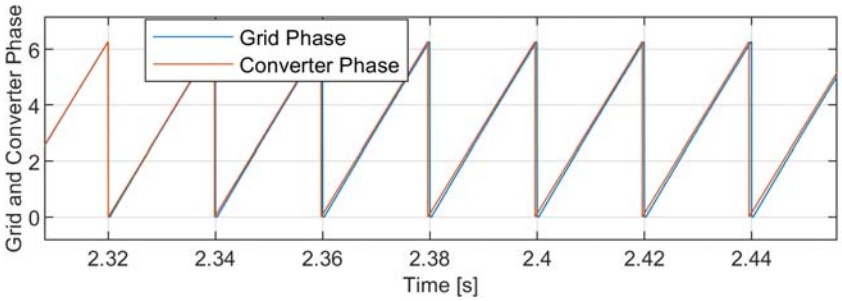
(a) Back emf



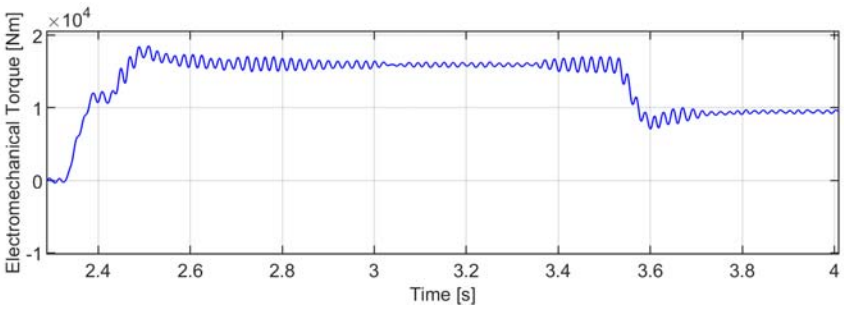
(b) Converter Angular Speed



(c) Grid current



(d) Converter and grid phase



(e) Elechtromecanical Torque

Figure 6.17: Simulation results of the synchronverter operating in Pset, Qset mode. The Active power reference is set to 5MW at t=2.3s and to 3MW at t=3.5s. The reactive power is set to 0.

6.6.3 Frequency regulation

The switch S_p is set to OFF. A step in the grid frequency is performed. The synchronverter reacts following its frequency droop characteristic that is governed by the parameter D_p through the following equation

$$D_p = -\frac{\Delta P}{\omega^* \Delta\omega} \tag{6.2}$$

expressing the frequency droop mechanism shown in Fig.6.18.

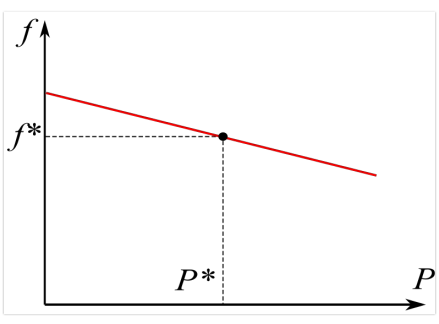
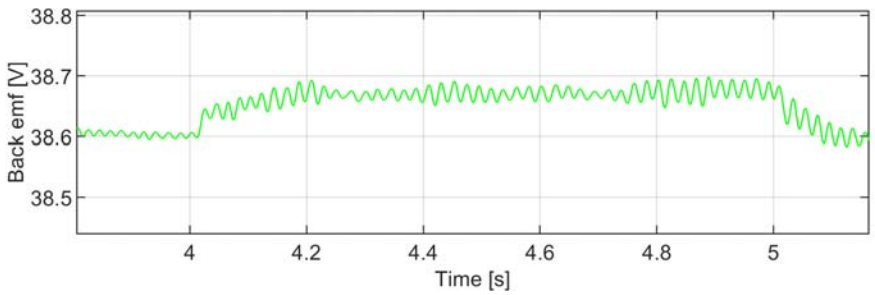


Figure 6.18: Frequency regulation droop

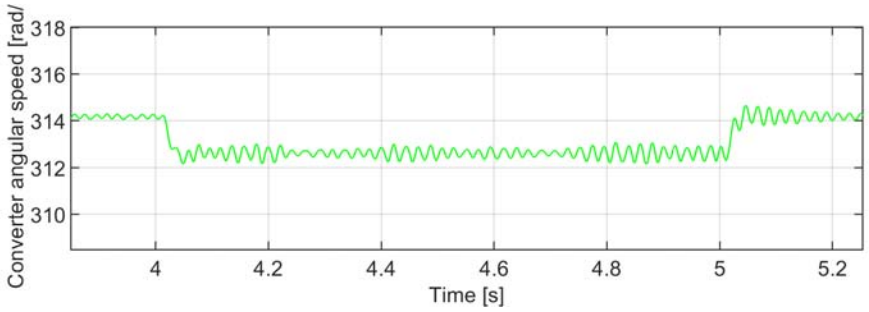
When the frequency of the grid decrease the output power increases. D_p is chosen in order to provide a regulating power ofd 1MW to a frequency variation of 0.25 Hz.

In Fig.6.19 the simulation results of the synchronverter operated in frequency support mode are shown. The grid frequency is stepped down by 0.25Hz and, according to eq.6.2, the active output power increases by 1MW.

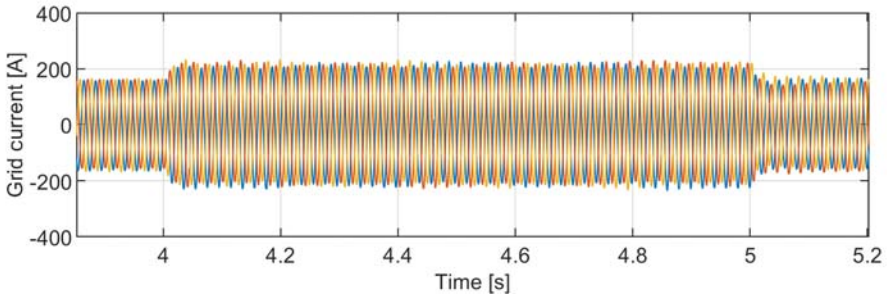
It is important to note that after the transient the machine virtual angular speed follows the grid angular speed (312.58 rad/s) maintaining the synchronisation. The regulating torque is produced by the gain D_p that multiplies the error between the actual and the nominal grid angular speed. This operating mode provides that the regulating power is provided instantaneously when the frequency is off-nominal without an output initialising signal.



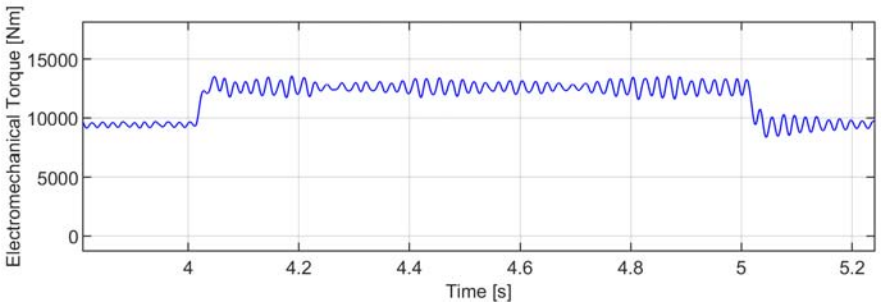
(a) Back emf



(b) Converter Angular Speed



(c) Grid current



(d) Elechtromecanical Torque

Figure 6.19: Simulation results of synchronverter in frequency support mode. A step of $-0.25Hz$ of the grid frequency is performed. The synchronverter reacts with a active power step of 1MW

6.6.4 Voltage regulation

In this subsection it is simulated the SST supporting the MV grid voltage. Both the switches S_p and S_q are turned on. The synchronverter reacts to a voltage magnitude variation with a reactive power injection or absorption from the grid, depending on the sign of the voltage variation. In this simulation is performed an under voltage condition, therefore the Synchronverter need to inject reactive power to the grid. In order to inject reactive power to the grid the machine should be over excited. It can be verified in sub-fig (a) of Fig.6.21 that the value of the electromotive force is $M_f i_f = \frac{=}{3}7.3V$ to which corresponds a converter side phase to ground peak voltage amplitude of $\hat{V}_{converterao} = 11718V$ that is higher than the the off nominal phase to ground grid voltage $\hat{V}_{gridao} = 11022V$.

The voltage support is regulated following the voltage droop control shown in Fig.6.20

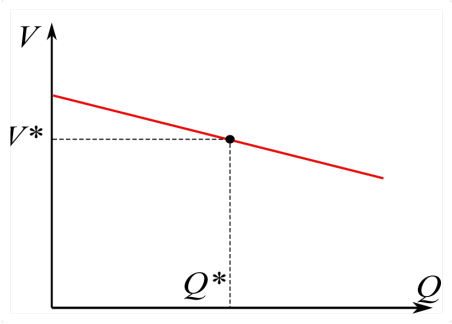
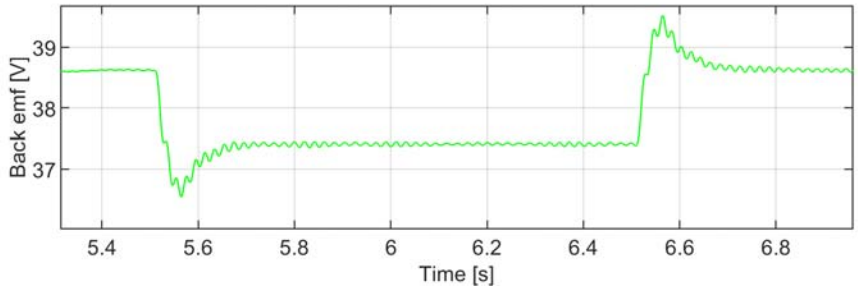


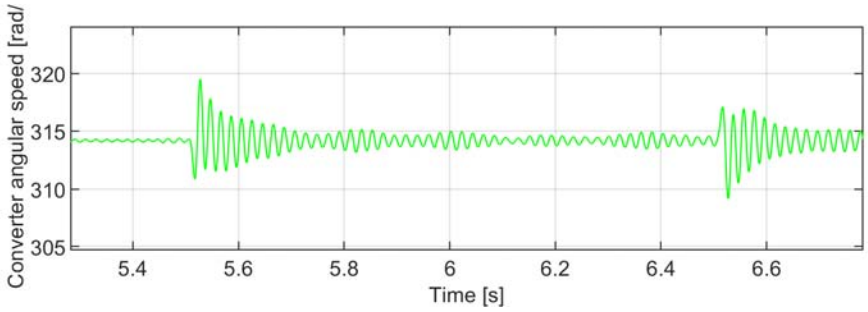
Figure 6.20: Voltage regulation droop

The voltage droop gain K is choosen in order to have a reactive power of 2MVar when the voltage magnitude varies of 10%.

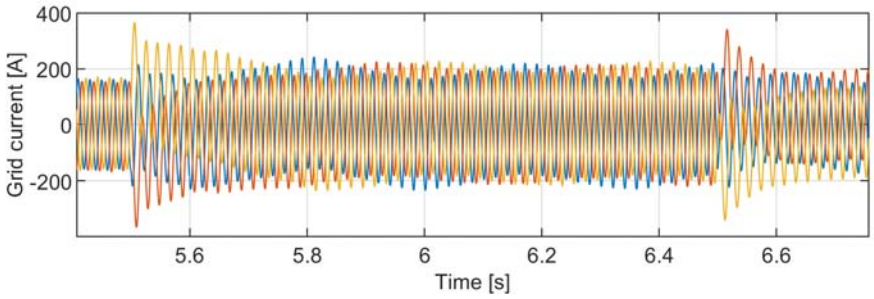
As it can be seem from Fig. 6.21 both the virtual angular speed and the back electromotive force signals have a strong oscillation during the voltage regulation operation.



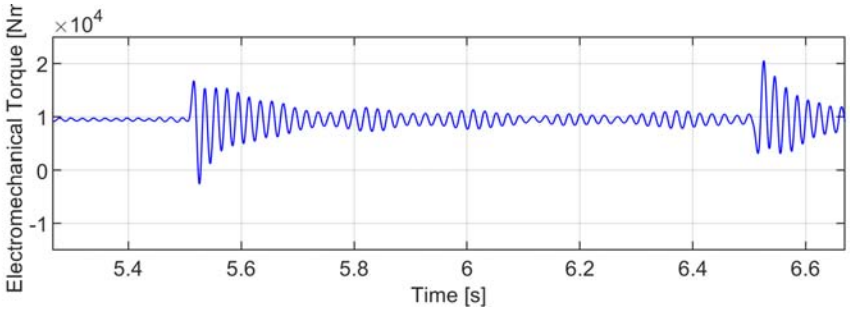
(a) Back emf



(b) Converter Angular Speed



(c) Grid current



(d) Elechtromecanical Torque

Figure 6.21: Simulation results of synchronverter in voltage support mode. A step of −10% of the grid voltage amplitude is performed. The synchronverter reacts with a reactive power step of 1MVAR

7 Conclusions and Future Work

7.1 Conclusion

In this thesis, detailed studies have been done on single module SST to investigate the performances of IDA-PBC control applied to three different topologies.

For each topology, the role of the DC bus capacitor has been analysed in detail. It has been designed considering the DAB and the AC/DC converter effects separately and then applying the superposition of the effects principle to find the total capacitance needed. Since the superposition principle is valid only for linear systems and power electronics is not linear, the simulation results didn't match with the theoretical values, being on average underestimated by the 50

As expected the DC bus capacitance, needed to ensure the same DC Bus voltage power quality, changes depending on the topology. Substituting the single-phase DAB with the three-phase DAB made the capacitance decrease by three time, and moving from the two-level topology to the three-level one the capacitance decreases by two. A smaller capacitance makes the dynamics of the DC buses faster. Meaning that the voltage level comes back quickly to the reference value after a disturbance. The stability analysis of the whole SST system is left as future work.

IDA-PBC control has been applied to all the converters constituting the SST. No knowledge of the load power is required making this control suitable for grid applications. The control showed good disturbances rejection both when operating in off-nominal LV grid conditions and when feeding a CPL on the DC buses. The THD measured in the simulations always satisfied the power quality requirements apart in the case of the LV rectifier. The upgrade of the LV rectifier control to ensure a lower THD is left as future work.

Finally, the new roles of virtual inertia provision for the SST have been analysed and the synchronverter control has been applied to the MV AC/DC converter with the SST working in Step-up mode.

7.2 Future work

VSM control

The synchronverter control designed in this thesis has given good results but has also shown some weakness. In particular, the power angle δ oscillations, present in the physical synchronous machines, causes unbalance in the output power (current) and in some conditions create instability. It has been noted that the two-level three-

phase converter was not very sensitive to this oscillations while the three-level NPC converter was very sensitive reacting with huge unbalance in the currents.

In this thesis, the VSM control has been applied to the MV side converter with the SST working in a step-Up mode, hence operated as an inverter. The same approach could be applied also to the MV converter working as a rectifier, corresponding to a synchronous motor. In this case, the control should regulate the DC voltage to the reference value. It has been tried to use a PI controller to stabilise the DC voltage by regulating the active reference power but due to the slow dynamics of the control, it has not worked.

An idea on how to proceed to derive a more robust control is to use the IDA-PBC approach that can guarantee robustness and stability. In [9] a port Hamiltonian model of the VSM is reported. This could be a starting point for further the research in this direction.

IDA-PBC rectifier control

The IDA-PBC approach applied to the LV rectifier has not been able to guarantee the AC power quality requirements. This is because the reference current is calculated through eq.4.73 where a square root limits the R2 damping to low values to have positive solutions. For this reason, the other damping coefficient R1 needs to be increased, causing a higher noise in the control signal. The same control applied to the MV rectifier guarantees power quality requirements.

As future work, it should be tried to re-define the reference current equation, for example by modifying the interconnection matrix J.

Appendix

List of Figures

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List of Listings

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