UNIVERSITÀ
DEGLI STUDI
DI PADOVA

DIPARTIMENTO
DI INGEGNERIA
DELL'INFORMAZIONE

DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

CORSO DI LAUREA MAGISTRALE IN
INGEGNERIA ELETTRONICA

DESIGN OF A 15kW NON-ISOLATED DC-DC CONVERTER FOR A FUEL-CELL TO BATTERY AUTOMOTIVE APPLICATION WITH WIDE INPUT AND OUTPUT VOLTAGE RANGES

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ANNO ACCADEMICO 2022-2023

Data di laurea 20/04/2023

Thanks to my friends.

Abstract

In recent years the automotive industry is increasingly shifting towards green power, as a clean and sustainable alternative to traditional gasoline-powered vehicles. The leading technologies in the shifting towards green power are the electric and hydrogen fuel cell vehicles. The fuel cell vehicles generate electricity through the chemical reaction of hydrogen and oxygen, taking place in the fuel cell, emitting only water or water vapor. The electric vehicles use the chemical energy stored into batteries to generate the motion of the vehicle, creating no emissions at all. Under the assumption that the energy stored into the battery of the electric vehicle, and the hydrogen consumed by the fuel-cell vehicle are green generated, both technologies provide motion power with near-zero emissions.

The combination of the two technology leads to the use of hydrogen fuel cells as a range extender for electric vehicles. Fuel cell range extenders can provide a longer driving range and faster refueling times compared to traditional battery-only electric vehicles, making them more practical for long-distance travel. For instance, every fuel-cell vehicle is equipped with a battery to manage the impulsive power request of the motor, against the slow dynamic of the fuel cell. If the average motion power is fully provided by the fuel-cell, then the vehicle is fully hydrogen powered. On the other side, if the fuel cell provides only a fraction of the total motion power, it operates as range extender for the electric vehicle. In both cases, the interfacing between the fuel cell generation and the vehicle battery is a relevant aspect in the powertrain of the vehicle.

In this thesis has been designed a DC-DC converter to interface the fuel cell to the battery of the vehicle. During normal operation, the fuel cell generates electric power and the converter controls the current injected into the battery to meet the power generation of the fuel cell. The output voltage is also controlled, to manage the condition of unconnected battery. The challenging aspect of the design are the wide range of the input and the output voltages, that complicates the control of the stages and the efficiency optimization of the converter. The topology is selected in such a way to obtain good efficiency in every operating condition. The project industrialization also takes crucial role in the decision process carried out in the design phase. The design of the converter have been first validated by simulation, and finally validated and optimized by experimental measurements.

Sommario

Negli ultimi anni l'industria automobilistica si sta spostando sempre più verso l'energia pulita, come alternativa sostenibile ai tradizionali veicoli a combustione. Le tecnologie leader nella transizione verso l'energia pulita sono i veicoli elettrici ed i veicoli ad idrogeno con fuel cell (cella a combustibile). I veicoli a fuel cell generano potenza elettrica mediante una reazione chimica tra idrogeno e ossigeno, che avviene nella fuel cell, emettendo solo acqua o vapore acqueo. I veicoli elettrici utilizzano l'energia chimica immagazzinata nelle batterie per generare la forza di trazione del veicolo, senza creare alcuna emissione. Partendo dal presupposto che l'energia immagazzinata nella batteria del veicolo elettrico e l'idrogeno consumato dal veicolo a fuel cell siano generati in modo sostenibile, entrambe le tecnologie forniscono potenza di trazione con emissioni prossime allo zero.

La combinazione delle due tecnologie consiste nell'utilizzare le fuel cells come range extender per i veicoli elettrici, fornendo un'autonomia di guida più lunga e tempi di rifornimento più rapidi rispetto ai tradizionali veicoli elettrici solo a batteria, rendendoli più pratici per i viaggi a lunga distanza. In ogni caso, ogni veicolo a fuel cell è dotato di una batteria per gestire la richiesta di potenza impulsiva del motore, data la dinamica lenta della fuel cell. Se la potenza di trazione media è completamente fornita dalla cella a combustibile, allora il veicolo è completamente alimentato a idrogeno. D'altra parte, se la cella a combustibile fornisce solo una frazione della potenza totale di trazione, la fuel cell funziona come un range extender per il veicolo elettrico. In entrambi i casi, l'interfacciamento tra la fuel cell e la batteria del veicolo rappresenta un aspetto di prim'ordine nella catena di generazione del veicolo.

In questa tesi è stato progettato un convertitore DC-DC per interfacciare la fuel cell alla batteria del veicolo. Durante il normale funzionamento, la cella a combustibile genera potenza elettrica ed il convertitore controlla la corrente iniettata in batteria al fine di iniettare in batteria la potenza generata dalla fuel cell. Viene controllata anche la tensione di uscita, per gestire la condizione in cui la batteria non sia collegata al convertitore. L'aspetto impegnativo del progetto consiste nell'ampia escursione delle tensioni di ingresso e di uscita, che complica il controllo degli stadi e l'ottimizzazione dell'efficienza del convertitore. La topologia è stata selezionata per ottenere una buona efficienza in ogni condizione operativa. L'industrializzazione del progetto ricopre un ruolo cruciale nel processo decisionale svolto durante la progettazione. Il progetto del convertitore è stato da prima convalidato in simulazione, ed infine convalidato ed ottimizzato con misure sperimentali.

Contents

List of Figures

List of Tables

1 Introduction

The fuel-cell power generation is gaining increasing interest in the green mobility field. Hydrogen electric vehicle (HEV) overcome the limitations of the traditional electric vehicles (EV), such as the limited distance range and the long charging time. In this scenario, the use of hydrogen in a *fuel-cell power extraction system* becomes an attractive solution, in fact: the refill of the hydrogen thank is extremely faster than the EV battery charge, and the range of the vehicle can be extended charging the motion battery by means of the fuel cell, while the vehicle is moving.
In figure 1 is depicted the block diagram of a standard fuel-cell (FC) power extraction system, for automotive application. The system core is the fuel-cell stack, it combines the hydrogen stored in the thank and the oxygen naturally present in the air to produce an electric current flow. Also water is generated, as product of the chemical reaction taking place in the cell. The hydrogen contained in the water can be extracted back by electrolysis, using green generated electric energy. In this way the circle is closed around the hydrogen consumption and production. In HEVs the battery is relatively small, in fact the average traction power is fully produced by the fuel cell and not provided by the battery. By the way the dynamic of the power generated by the cell is quite low, the battery is intended to power the traction motors during the power request variations, while the FC is reaching the new operating point with its slow dynamics.

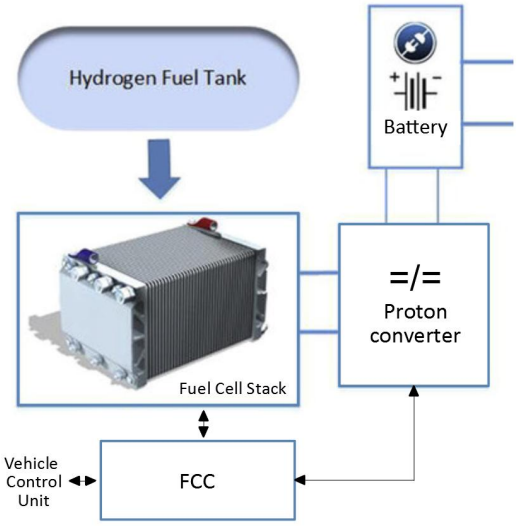


Figure 1: Schematic diagram of the fuel-cell generation system

The fuel-cell is well modeled as a current generator: the magnitude of the chemical reaction is directly proportional to the magnitude of the output current, while the voltage out of the cell is variable and unstable. The battery of the vehicle, instead,

resembles the more a voltage generator in the sense that its voltage is, in general, quite stable. Moreover FC stacks typically have voltage below $200\,V$, while traction battery reaches up to $800\,V$. The different electric behavior of the FC stack and the accumulator, as well as the voltage mismatch, highlights the necessity to introduce a power converter, to interface the fuel-cell and the battery. The converter needs to extracts the power generated by the cell, convert and control voltage and current to properly charge the battery of the vehicle. Current and voltage of the FC are DC quantities, and so is the battery voltage, the converter then is a DC/DC converter. The converter rises the cell voltage, typically lower than $200V$, up to the battery voltage that, depending on the vehicle, could range from $200V$ to $800V$.
The fuel-cell power extraction system could also be integrated into an EV as a "range extender", the topology of this implementation is depicted in figure 2[1].

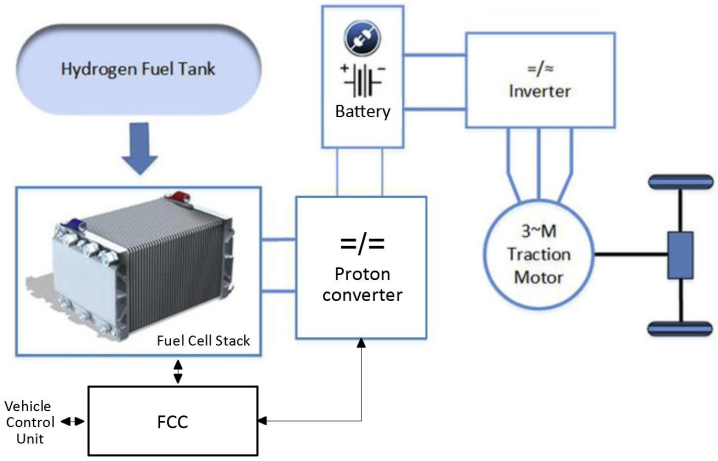


Figure 2: Schematic diagram of a fuel-cell implementation into an EV

The power extraction from the fuel-cell, as well as the full operation of the cell, is governed by the fuel-cell controller (FCC). The FCC, itself, receive from the vehicle ECU the information regarding how much power should be generated by the fuel-cell. Then the FCC modulates the flux and pressure of hydrogen and oxygen injected into the cell, in order to meet the power generation request. Due to the current generator behavior of the fuel cell, the operating point set by the FCC corresponds to a certain amount of current generated by the cell. The information of how much current is being generated is transmitted by the FCC to the power converter, that will use this information as a set-point to regulate its input current. A schematic of the power generation control is depicted in the following figure 3. In this thesis will be designed the DC/DC converter that interfaces the fuel cell and the vehicle battery. The design is committed by a fuel cell manufacturer, looking for a wide application converter to connect its fuel cell stacks to the most common EV architectures. The main challenging aspects of the design of the power converter

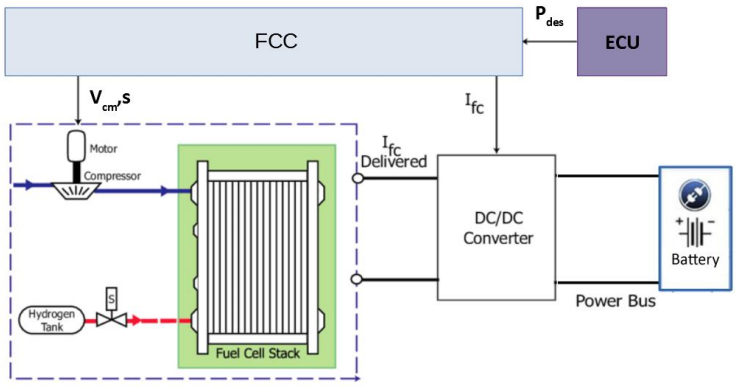


Figure 3: Control signals of a Fuel cell power generation system.

are:

- The high conversion power: the maximum power of the converter is $75kW$
- The wide input voltage range: input voltage spaces from $46\,V$ to $275\,V$
- The wide output voltage range: output voltage spaces from $200\,V$ to $800\,V$
- The industrialization of the product: the product will be manufactured and commercialized, then industrialization considerations take crucial relevance.
- High power density: reduced space occupation.

The converter requirements will be analyzed in sections 2, then in section 3 is developed the project of the converter based on those specifications.

2 Converter specifications analysis

The converter developed later on in this thesis has been commissioned by a fuel cell manufacturer to interface its FC to the most used battery voltage of $200-800\,V$. The application has discussed with the costumer, and came out the specifications for the power converter, that are presented and analyzed in this section. This specifications represent the objectives for the design of the converter carried out in the following section 3.

2.1 Input specifications

The DC/DC power converter is connected to the output of the FC. The converter input electrical parameters ,then, must rely on the FC output capability in terms of voltage and current. The converter is intended to fit the most wide range of fuel-cell stacks, so that the analysis first considers the electrical parameters of the fuel cell stacks manufactured by the customer, shown in figure 4.

Type PM 400	48	72	96	120	144	168	192	216	240
Electrical Output									
Power Range* [kW]	2.1–14.2	3.1–21.3	4.1–28.4	5.1–35.5	6.2–42.6	7.2–49.7	8.2–56.8	9.2–64.0	10.3–71.0
Current Range [A]	0–500								
Voltage Range [V DC]	28–55	42–83	56–110	71–137	85–165	99–193	113–220	127–248	142–275
El. System Efficiency* [%]	47–67								

Figure 4: Electrical parameters of the fuel cell stacks manufactured by the customer

The converter is intended to fit the most powerful stacks of the series from 96 to 240 cells. Then, from figure 4, the constraints on the input voltage of the converter are straightforward and results in table 1.

Table 1: Input voltage specifications

Input Voltage	**Range DC**
V_{IN}	46-275 V

The minimum input voltage of the converter is little lower than the minimum voltage of the 96-cells stack to accounts for voltage losses in the connections. Every fuel cell stack, regardless of the number of cells, outputs a current up to $500\,A$. The input current of the converter, that corresponds to the output of the FC, ranges itself within the $0-500\,A$, as listed in table 2.

Table 2: Input Current specifications

Input Current	**Range DC**
I_{IN}^{tot}	0-500 A

When the load current of the fuel cell is not purely DC, but a current ripple is superimposed, the hydrogen consumption increases and the output power of the fuel cell decreases. The magnitude of this efficiency decrease is a function of the frequency of the ripple current: low frequency ripple reduces the cell efficiency more than the high current ripple[2]. In this application the current ripple of the fuel cell equals the input current ripple of the converter, so considerations needs top be done to keep it at low value. The maximum input current ripple is set, by the customer, to the equation (1), using the maximum input current value $I_{in,max}^{tot} = 500\,A$.

$$\begin{aligned} \Delta I_{in,max}^{tot} &\leq 6\% \cdot I_{in,max}^{tot} \\ &\leq 30A \end{aligned} \tag{1}$$

The DC/DC converter must handle a nominal input power of $P_{nom} = 75\,kW$, generated by the FC. Since the power to be converted is considerably high, a common solution to realize the converter is to realize a certain number k of identical modules, and then realize a parallel connection between them. This solution move the converter design to a lower power level, since the power to be handled by a single module is P_{nom}/k. Of course, some complexity is added in terms of manage the parallel connection of the modules. The number of module k has chosen as a trade off between power reduction and complexity control increase: $k = 5$ has selected. With the total converter made up of 5 modules in parallel connection, every module is designed to handle a power of $15\,kw$. With the parallel connection of more modules, the converter design reduces to the design of a single module out of the k ones.
From this point, the specifications following in this section and the converter design of section 3 refers to a single module of size $15\,kW$. The maximum input current of the single module results in equation (2) as well as the maximum input current ripple in equation (3).

$$I_{in,max} = I_{in,max}^{tot}/k = 100A \tag{2}$$

$$\Delta I_{in,max} = 6\% \cdot I_{in,max} = 6\,A \tag{3}$$

For the maximum input current ripple of the single module, the worst case condition is considered: the modules are supposed to be synchronized, and no current ripple cancellation occurs due to interleaving effect between modules. Clearly, the input voltage specification don't change even if the converter is modular, due to

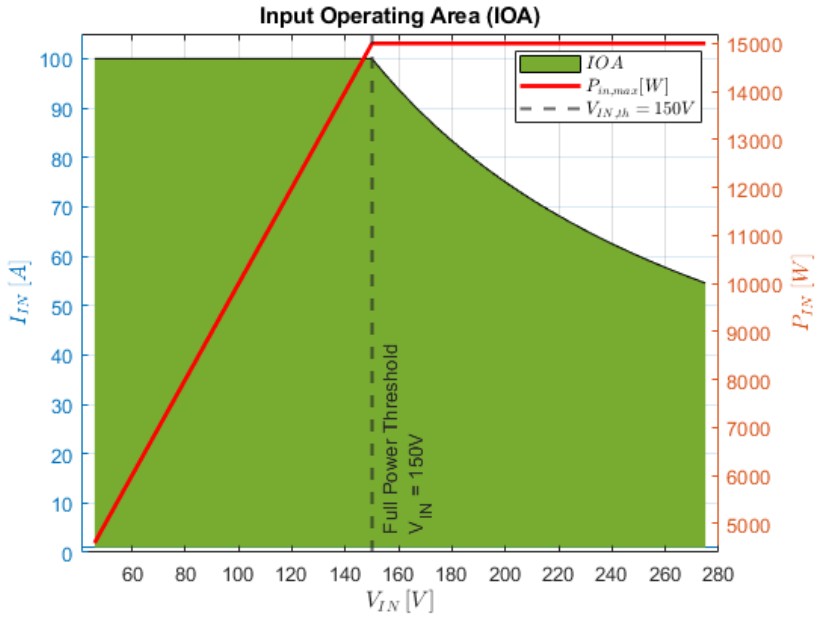


Figure 5: Input Operating Area and input power of a single converter module

the definition of the parallel connection. Based on the input specification of the single module, it is useful to defined the input operating area, IOA, showing all the possible input operating points of the converter. The IOA is shown in figure 5 as well as the maximum input power over the input voltage. Two main regions can be identified in the IOA:

- *Constant input current region:* $I_{IN,max}$ limits the input power. This is the left region of the green area, for input voltage lower than $V_{IN,th} = 150\,V$ no full power can be injected into the converter due to the limitation on the maximum input current
- *Constant input power region:* P_{nom} limits the input current. This is the right region of the green area for $V_{IN} > V_{IN,th}$. The maximum input power constraint limits the maximum input current to satisfy equation $I_{IN} \leq P_{nom}/V_{IN}$.

2.2 Output specifications

The goal of this fuel-cell power generation system is to be a flexible-application product, able to fit different hydrogen vehicles typologies and cover the largest possible market share. The power converter then needs to interface to the widest range of EV batteries. Current battery systems for hybrid and electric vehicles typically have operating voltages of $200 - 800\,V$ [3], makes sense this is also the range of the Output voltage of the converter as in table 3.

Table 3: Specification range of the output voltage of the converter

Output Voltage	**Range DC**
V_o	$200V - 800\,V$

When the converter operates at high power applications, around P_{nom}, its output voltage will probably experience the upper portion of the specification ranges, $400V - 800V$, since the high-power vehicles usually have the higher battery voltage. On he other side, for lower power applications the output voltage typically will be in the $200V - 400V$ range.
As for the input current, also the output current of the converter is limited in its maximum value. The constraint on the maximum output current has introduced to limit the conduction losses in the output stage of the converter, and to properly design the current rating of the active and passive devices. Output current range is defined for a single module in the following table 4.

Output Current	**Range DC**
I_o	$0 - 46\,A$

Table 4: Specification range of the output current, for a single module

As a side effect of the maximum output current limitation, is that the minimum output voltage is higher than $200\,V$ in some operating conditions: when the input power is greater than the threshold value $P_{fc,th}$ thrn the minimum output voltage must rise, to not exceed the maximum output current $I_{o,max} = 46\,A$.
Supposing the converter efficiency to be unitary, $P_o = P_{fc}$, then for $V_{o,min}^{nom} = 200V$ the treshold FC power results

$$\begin{aligned} P_{fc,th} &= V_{o,min}^{nom} * I_{o,max} \\ &= 200V * 46A \\ &= 9.2\,kW. \end{aligned} \tag{4}$$

For input power higher than $P_{fc,th}$ the minimum output voltage $V_{o,min}$ is strictly greater than $V_{o,min}^{nom}$: the minimum output voltage rises for output power $P_o \geq 62\% \cdot P_{nom}$. The area of figure 6 shows all the output operating points, for input power from $0W$ to the nominal power P_{nom}. Efficiency is supposed unitary.
The customer also specifies another constraint on the output voltage: the output voltage must be at least 12% greater than the input voltage, in every working condition.

$$V_o \geq V_{in} + V_{in} \cdot 12\% \tag{5}$$

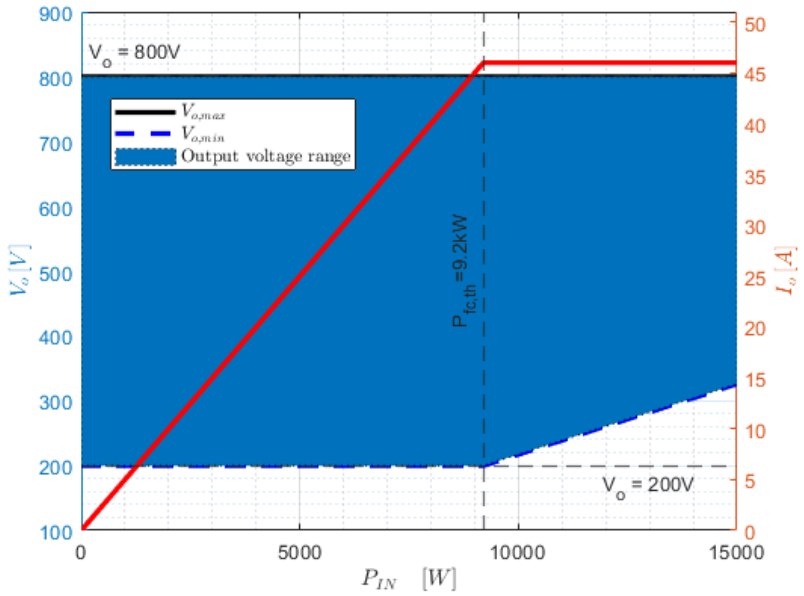


Figure 6: Output voltage range vs input power, the output current limitation effect is noticeable

In other words, the voltage transfer ratio of the converter $M = V_o/V_i$ results to be always greater than 1.12, as shown in equation 6, and the converter always behaves as a **step-up** converter.

$$M_{min} = \frac{V_o}{V_{in}} = \frac{V_{in} \cdot (1 + 0.12)}{V_{in}} = 1.12 \tag{6}$$

This information will play a leading role in the topology selection carried out in section 3. To facilitate the following design process, the voltage conversion ratio M is deeply investigated. Two relevant values can be determined:

- The maximum voltage conversion ratio, at nominal power

$$M_{max}^{nom} = \frac{V_{O,max}}{V_{IN,th}} \simeq 5.3 \tag{7}$$

- The absolute maximum voltage conversion ratio, at power lower than nominal

$$M_{max} = \frac{V_{O,max}}{V_{IN,min}} \simeq 17.4 \tag{8}$$

Then from figure 7 can be found the *maximum input power* experianciable for every voltage conversion ratio M. This information will be relevant during the design phase.

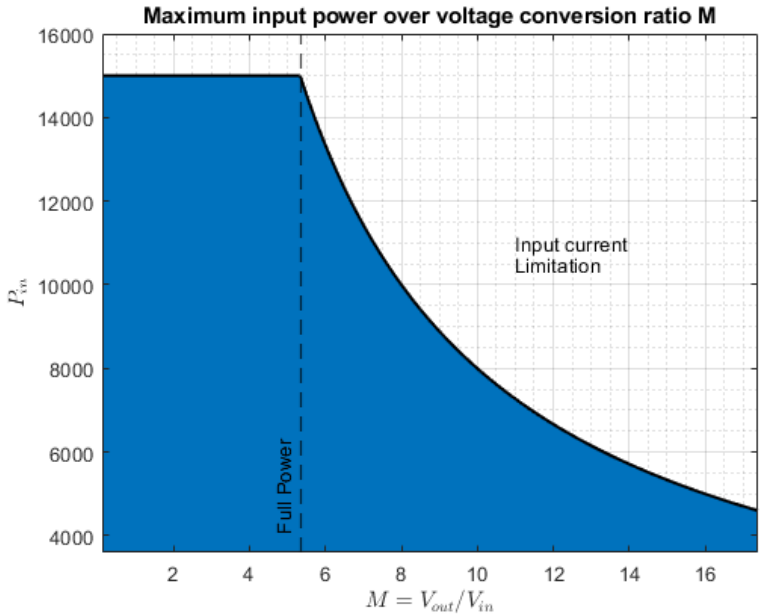


Figure 7: Input power over voltage conversion ratio M

2.3 Efficiency specifications

The efficiency of the converter is set by the customer as minimum values at specified operating points. Two standard fuel-cell stacks (96-Cells and 168-Cells) are considered as input operating conditions. The efficiency requirements are listed in table 5.

Table 5: Efficiency specifications, for a single module

	$I_{in}\,[A]$	$V_{in}\,V_{DC}$	$V_o\,V_{DC}$	$M = V_o/V_i$	η_{min}	η_{target}
96-Cell	100	46	200	4.3	95	96.5
EOL			800	17.3	92	93.5
168-Cell	100	133	216	1.6	97	98
SOL	100	105	216	2	96	97

The table sets two columns for different efficiency parameter: the η_{min} specifies the minimum efficiency to be reached, while η_{target} is a desired efficiency target that is desirable but not mandatory to reach. All the input operation points of table 5 are out of the full-power input range, so that efficiency specifications set by the customer are for power lower than the nominal one.
It is defined P_{loss} the power dissipated by the entire converter, then power losses

and efficiency η are related by the following equation

$$P_{loss} = P_{IN}(1 - \eta) \tag{9}$$

The efficiencies listed in table 6 results in the power losses of table 6. From the table can be noticed that the cooling system need to be able to extract and dissipate at least $P_{loss} \simeq 2\,kW$ from the converter.The entire converter made up of the $k = 5$ modules is considered.

Table 6: Power losses at specified efficiency points

M	η_{min}	P_{IN}	P_{loss}
1.6	97	66.5 kW	1995
2	96	52.5 kW	1575
4.3	95	23 kW	1150
17.3	92	23 kW	1840

To evaluate the maximum power that can be dissipated by the cooling system, a thermal analysis has been request to the TRE-S company. The company is specialized in the project and construction of heatsink for the electronics industry. They have performed finite element simulations to best design the liquid path into the baseplate, as well as determine the maximum dissipated power $P_{loss,max}$ to keep the plate temperature under the critical threshold of $T_{h,max} = 80°C$. The figure 8a shows the simulated plate temperature for a dissipated power of $3\,kW$. Then the simulation is repeated with $P_{diss} = 4\,kW$, and the baseplate temperature hits the threshold value $T_{h,max} = 80°C$. This power can be considered as the maximum power that can be dissipated by the converter. When the converter operates at full-power the maximum power dissipation $P_{loss,max} = 4\,kW$ corresponds to a minimum efficiency of

$$\eta_{nom,min} = 1 - \frac{P_{loss,max}}{P_{in,max}} \simeq 94.7\% \tag{10}$$

If the power dissipated by the converter exceed the maximum threshold of $P_{loss,max}$ the baseplate temperature increases too much and the converter will damage. Based on this result, can be defined a minimum efficiency that is strictly necessary to realize in order to avoid converter damage. The area of figure 9 depicts all the efficiency values that causes no thermal damage to the converter (i.e. $P_{loss} \leq P_{loss,max}$). Of course, the lower trace in figure 9 just represents a minimum value for the converter functionality, but the efficiency of the converter is expected to be higher than that values.

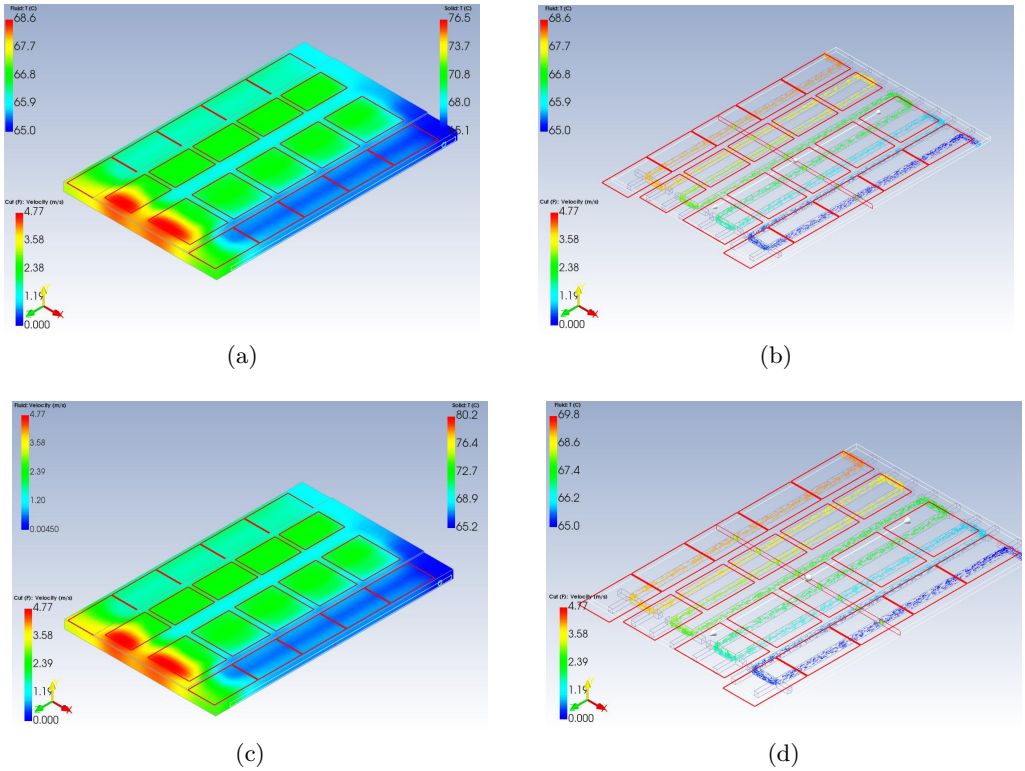


Figure 8: Thermal simulation results: $P_{loss} = 3\,kW$ plate temperature (a) and liquid temperature(b), $P_{loss} = 4\,kW$ plate temperature (c) and liquid temperature (d)

2.4 Physical dimension

Physical dimension is one of the challenging aspects in the converter design. The converter is intended for automotive application, so that both reduced size and reduced weight are fundamental aspects of the project. Since the power handled by the cooling system is considerably, and since the converter needs to be as compact as possible, a liquid cooling system will be used. This solution allows to mount the converter on an aluminum baseplate, just $2.5\,cm$ thick, and move the dissipating radiator outside the converter. The heat generated by the converter will transfer to the baseplate, then to the cooling liquid and finally to the ambient air through the radiator. The customer has specified the maximum physical dimension of the converter, follows the baseplate dimension of figure 10a. For the single module the physical dimensions are depicted in figure 10b, instead. The physical dimensions are an inviolable design constraint, other aspects, such as efficiency, could be little sacrificed in order to satisfy the size request.

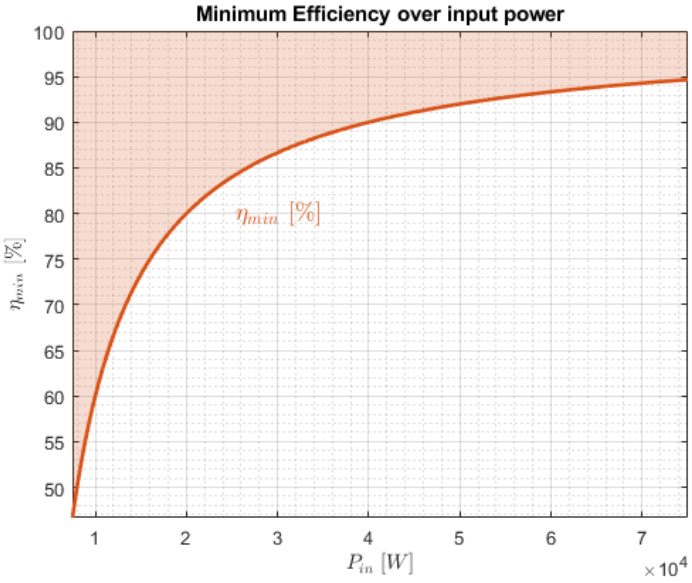
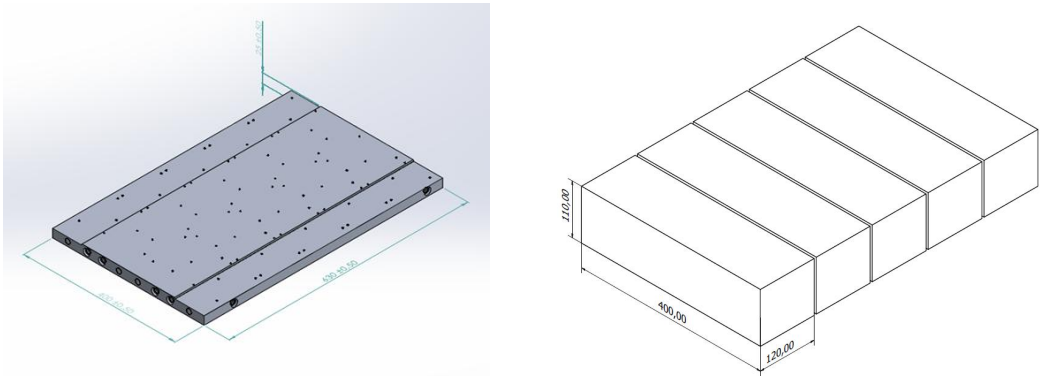


Figure 9: Absolute minimum efficiency of the converter, due to thermal limitation



(a) (b)

Figure 10: Physical dimensions of the baseplate (a) and of the single module (b)

3 Power converter design

In the previews section 2 have been analyzed the specifications for the power converter. Based on these specifications, in this section will be designed the power converter itself. The project consists of three distinct phases: first different topologies are analyzed, to find the one that best suits the converter specifications. Once the topology has determined, active and passive components are selected or designed. The last phase of the project consists in the compensation of the stage, or stages, and the realization of the control of the average input current of the converter.

First remind the field of application of the converter: as depicted in figure 11, the

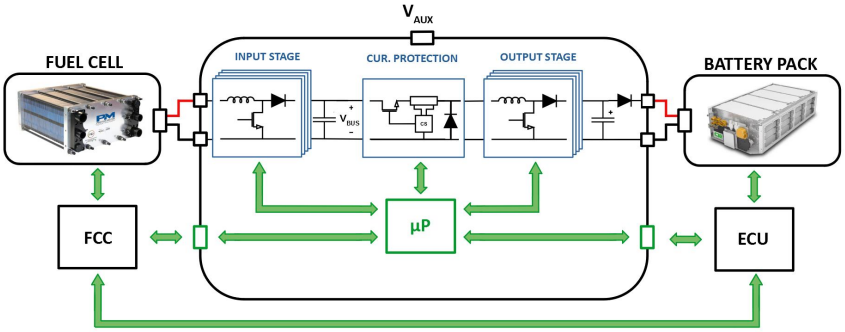


Figure 11: Schematic application of the converter

converter extracts power from a fuel cell and injects it into the battery pack of the vehicle, to increase its distance range over a purely electric vehicle topology.

Considering this scenario, in the previous section 2 were derived the main specifications for one out of the five modules of the power converter, that are summarized in table 7.

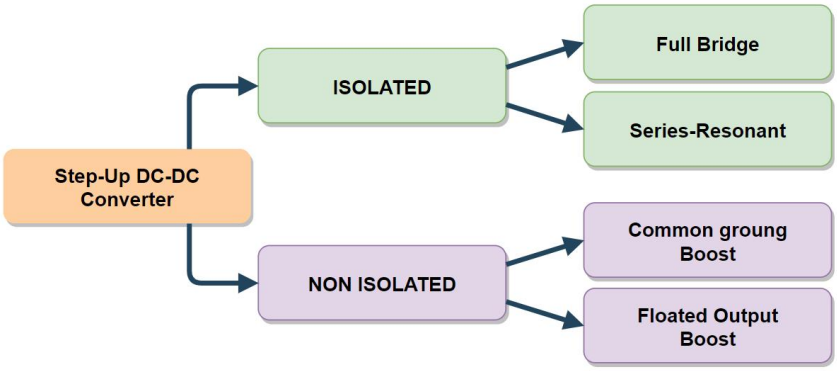


Figure 12: Diagram for the selection of the unidirectional converter topology

Table 7: Design specifications for a single module of the power converter

Parameter	**Symbol**	**Value**
Input voltage	V_{in}	$46 - 275\,V$
Input current	I_{in}	$0 - 100\,A$
Output voltage	V_o	$200 - 800\,V$
Output current	I_o	$0 - 46\,A$
Nominal power	P_{nom}	$15\,kW$
Voltage gain, $P_{in} = P_{nom}$	M^{nom}	$1.12 - 5.3$
Voltage gain, $P_{in} < P_{nom}$	M^{nom}	$5.3 - 17.4$
Physical dimension	$WxLxH$	$400x120x110\,mm$
Electrical isolation		Not required
Power transfer directions		Unidirectional

The literature has reported on a large number of topologies for boosting DC-DC converters. A first fundamental difference comes from the presence or not of the electrical isolation between the input and the output of the topology. The diagram of figure 12 divides the converters into isolated and non isolated topologies, and proposes some noticeable configurations for both the two categories[4].

A basic method for stepping-up a dc voltage is to use a PWM boost converter, figure 13a, which comprises only three components: an inductor, a switch, and a diode (or another switch in case of synchronous boost). A PWM boost converter is a simple, low cost, and efficient nonisolated step-up converter suitable for many dc applications. Among the most important required characteristics in a fuel cell application, is the current ripples reduction to avoid a lifetime shorting of the fuel

cell itself. The following equation gives current ripples of basic boost converter (11)

$$\Delta I_{in} = \frac{V_{in} \cdot D}{2 \cdot f_s \cdot L} \tag{11}$$

where V_{in} is the input voltage, D the duty cycle, f_s the switching frequency and L the inductance value. From this equation can be seen that small current ripples require large value inductance, and consequently a large inductor volume, making the total volume of the conventional boost converter quite large. Another parameter that plays an important role in the current ripples is the switching frequency. The introduction of wide bandgap devices such as SiC and GaN semiconductors helps in keeping the commutation losses at a relatively low values, by the way, the switching frequency can't be increased too much because the switching losses are proportional to the switching frequency.
The advantages and the drawbacks of basic boost converters are presented in the Table 8.

Advantages	**Drawbacks**
Simple converter	Low efficiency form high M
Low cost	Low voltage gain
Simple control	High inductor value for low input current ripple

Table 8: Advantages and drawbacks of basic boost converter.

When the converter is expected to achieve high conversion ratio, floating and non -floating boost topologies may be combined. The basic floating boost is shown in figure 13b. An example of combination of the basic boost in its floating and non-floating realization is the *Floating Double Bridge (FDB)*[5] of figure 13c: it brings to several advantages, including interleaving and higher voltage-gain of the entire converter. In particular the interleaving aspects is extremely relevant in this application: for high power applications, a single converter requires several devices in parallel to handle high currents. Instead of realizing a single converter with multiple parallel switches, it is desirable to have several identical converters connected in parallel with a phase-shifted control. This concept is called "interleaving", and every one of converters forming the interleaved structure can be referred as a "phase". Interleaving connection leads to a substantial reduction in the magnitude of the total input current ripple, due to the interaction of the input currents between the phases[6]. This aspect is so beneficial for the application of the converter that the choice is made to adopt an interleaving structure at the input of the converter.
In the FDB, the concept of interleaving is guaranteed by the parallel connection of the floating and non-floating version at the input and by the phase shifted control of the two switches (S1,S2). With the concept of interleaving, the total current

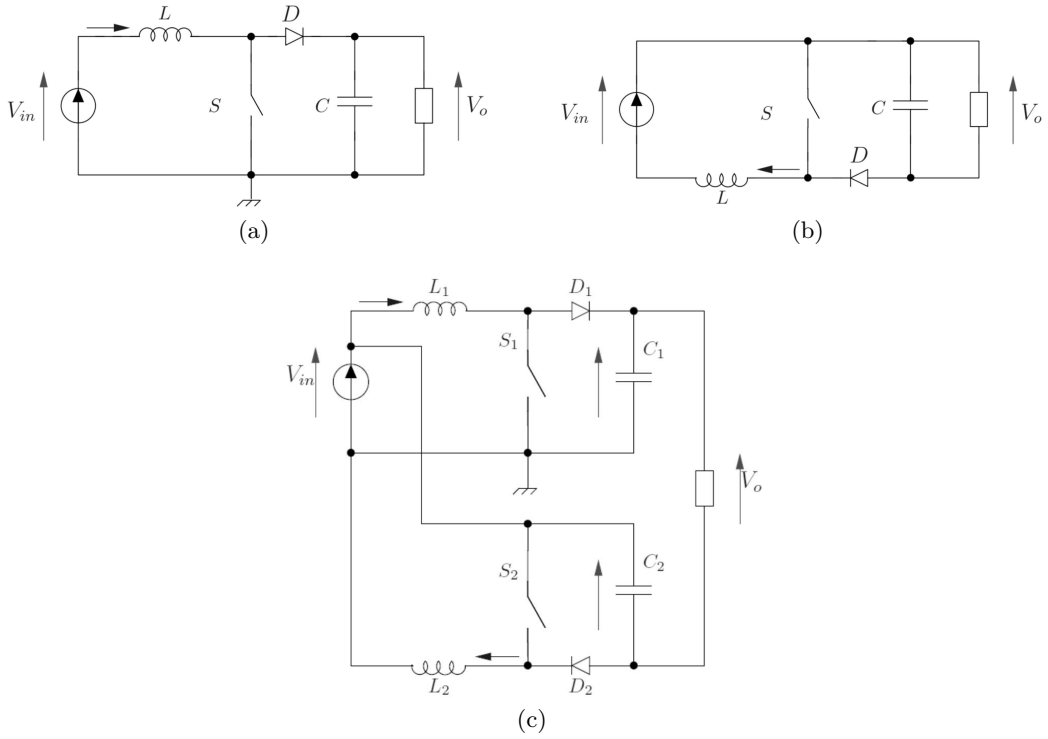


Figure 13: Basic shared ground boost topology (a), non shared ground boost (b) and FDB topology (c)

ripples are sufficiently low to allow a significant reduction in the volume of magnetic components. Then, since the volume of the converter is mainly determined by the volume of magnetic components, there will be a significant reduction in the volume of the converter and consequently higher power density.The relationship between the volume of the inductor and the number of phases is given in the following equation:

$$V_{tot,ind} = \left(\frac{I}{k}\right)^2 \cdot L \cdot k \tag{12}$$

where I is the current through the inductor, N the number of phases and L the inductance value. From this equation, the volume of the inductor is found to be reduced by a factor of k[5].
A fundamental aspect for the converter design is the capability to boost voltage, from input to output, known as *voltage transfer ratio "M"*. In the previous section 2.2, Figure 7 clarifies the range of "M" as well as the maximum input power for every M value. As we can see from table 7, the converter operates in full-power condition for relatively low voltage amplification values ($1.12 \leq M \leq 5.3$), but must be able to achieve higher voltage gain up to the maximum value $M_{max} = 17.4$, even if with reduced power transfer capability.
In high-power systems,if high voltage gain is required it is often beneficial to utilize magnetic coupling, and doing so can improve both efficiency and reliability. Typical ZVS an ZCS can be achieved with isolated-derived topology, and this helps to increase the efficiency of the conversion. Both the transformer in its nonisolated form (built-in) and the coupled inductor can be employed in nonisolated dc–dc structures. The coupled inductor will store energy in one cycle and then power the load in the other cycles; such converters usually operate at high frequency in order to reduce the size of the magnetic components. In a high-frequency transformer, instead, the voltage of an input dc source is converted to an ac voltage, often a square/quasi-square wave voltage, and then passed through the transformer to the output of the converter after a rectifying stage. The basic topology for unidirectional isolated-derived high-power transfer is the full bridge, depicted in figure 14a. The series-resonant is a full bridge topology with the addition of a series-resonant cell and is shown in figure 14b. The series-resonant converter is extremely attractive from a point of view of the conversion efficiency, due to near ZCS commutations of the bridge. Proper operation of these converters is highly dependent on the operating point, when the input and the output voltages drift from the nominal values then the resonance is no longer achieved and the efficiency quickly degrades. This prevents this topology to be used in wide input and output voltages application, then this topology is definitely not suited for this project.

The full-bridge circuit represents an improvement over the half-bridge circuit for high-power converters, the voltage seen by the transformer is doubled and so the current is split in half. The main challenge of the full bridge, as well as the other

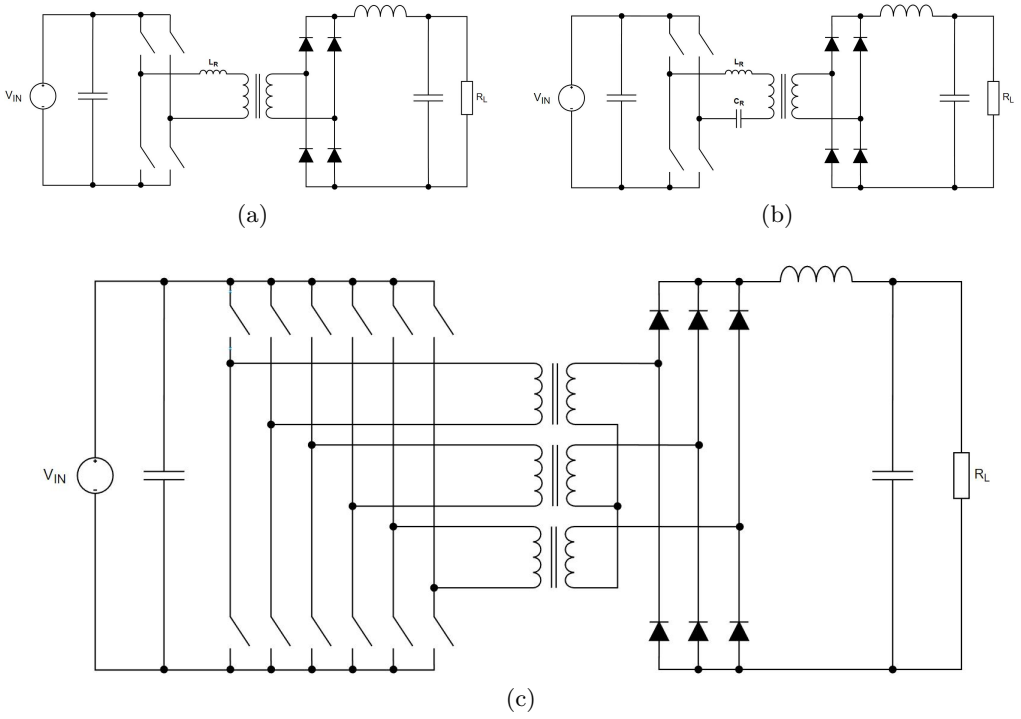


Figure 14: Full bridge (a), Resonant converter (b) and three-phase V_6 converter(c)

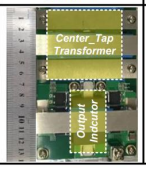
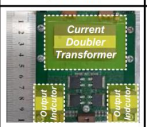
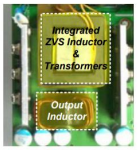
Structure	Proposed	PSFB_CT	PSFB_CD	[24]	[25], [26]
Transformer Type	PCB Printed Planar Transformer				Wire Winding Transformer
Power density of Magnetics	15 W/cm^3	12 W/cm^3	11.9 W/cm^3	11 W/cm^3	11.6 W/cm^3
Maximum Efficiency	95.1%	93.8%	94.1%	94.8%	95.0%
Prototype Magnetics					

Figure 15: Power density for different transformer technologies

isolated topology, is the transformer industrialization. In fact the transformer is:

- The most expansive component of the converter: the manufacturing requires many producing stages.
- A special process: requires hand-made operation during the mounting phase of the converter. This increases the manufacturing price of the converter.
- The bulkiest component of the converter.
- Difficult to dissipate: in non ventilated converters, as the one in this thesis, the transformer must be drowned into dissipating resin and screwed to the dissipating plate. By the way the inner windings can't be dissipated properly, since they are not reached by the resin.

The transformer represent the bottle-neck in the use of the isolated-topology in this project, than some rough calculations are computed to clarify if that choice is worth or not. In the paper [7] are compared three different arrangements for the full bridge converter, and compares different constructive technologies as well. The paper rely on the project of a $2kW$ full bridge converter operating at a switching frequency of $80kHz$. An interesting outcome of this study comes in the power density of the magnetic components, shown in figure 15.

The value of power density of figure 15 can be used as a starting point for a rough evaluation of the volume occupied by a $15kW$ transformer. The experience of the company in the design of power transformer suggests to lower the power density of such transformer to $PD = 9\,W/cm^3$, that is a more feasible value both for PCB printed planar transformer and wire winding transformer with a reasonable temperature increase. Then the fraction of the total volume occupied by the transformer results in equation 13

$$Occ\,[\%] = \frac{PD/P_{nom}}{V_{tot}} \simeq 32\% \tag{13}$$

Some points of percentage needs to be added because of the resin and dissipating case, that is mandatory in ordetr to dissipate the transformer in a non ventilated

Table 9: Advantages and drawbacks of V_6 converter over interleaved boost converter.

Advantages	**Drawbacks**
Soft switching over a wide load range	Much more expansive
High voltage gain	Bulkier
Higher efficiency for high M	Low efficiency for M away from nominal
	Higher conduction losses
	Control complexity increased

converter as the one of this project.
By the way, the input current of the converter reaches up to $100A$, and such a current is nontrivial to handle for a single transformer and practically too high for any MOSFET. In addition, interconnect and parasitic inductances will further induce significant i^2R and $Li2$ losses. It is necessary to parallel many MOSFETs to conduct the input current through the bridge without exceeding the maximum power dissipation of the active devices. The necessities to have more MOSFETs in parallel, together with the request of a low input current ripple forces to interleaving configurations such as the one of figure 14c, known as V_6 converter[8]. Different variations exist based on different connection of the transformer windings, strongly reduces the input current ripple but causes an increase in the volume occupied by the transformer. In fact, the number of windings are increased by a factor equal to the number of phases of the interleaved structure. This configuration, indeed, complicates the control of the converter. The advantages and drawbacks of using in this project the isolated topology of figure 14c, over a non isolated interleaved-boost are listed in table 9.

The drawbacks of using the V_6 solution over an interleaved boost converter makes the choice of the last one much more attractive. It is not explicitly required an electrical isolation between the input and the output of the converter, so an isolated topology would only be selected if its advantages are incontestably greater than drawbacks. This is not the case of this project, in fact:

- The transformer turns ratio in a phase-shift full bridge is selected considering the minimum input voltage and the maximum output voltage, so $N \simeq M_{max} = 17.3$. In this operating condition, the conduction angle is maximum and the full-bridge converter operates at its maximum efficiency. Out of this optimal point, the conduction angle decreases and the efficiency decreases itself due to increased conduction losses caused by higher rms value of the current flowing in the stage. The full bridge topology has an efficiency that is maximum at its maximum voltage gain, then decreases for lower voltage gains. The plot of figure 7 depicts the power over voltage gain of the converter to be designed,

it easy to see that the behavior of the desired efficiency is opposite to the one of a full bridge: the efficiency must be high at low voltage gains, where the transfer power is maximum, than can decrease for higher voltage gains since transfer power decreases itself.

- A transformer employed by isolated topology can be even ten times more expansive than an inductor used by a non isolated boost, with the same power capability. The design of an isolated topology strongly increases the production and development costs. Since the electrical isolation is not required, that increase in cost doesn't find direct match in a specification accomplishment.

This argumentation leads to set aside the isolated topology, in favor of the non isolated topologies like the boost or boost-derived converters. Using non isolated boost topologies keeps the design simple and the cost low but some solution needs to be found in order to overcome the weakness of the boost topology. In particular using the the boost topology:

- High voltage gains are not easy to achieve, due to parasitic resistance of the components
- Efficiency decreases for high voltage gains. Higher input current increases conduction losses, higher current and output voltage both increases commutation losses.

It is necessary to find a configuration with high efficiency at low voltage gains, but that is capable of high voltage gains when necessary. Efficiency degradation is tolerated at high voltage gains, since the power to be converter decreases with voltage gain. A consolidated structure to realize such behavior is the cascade of two boost stages. This allows to operate one single stage when low voltage gain and high efficiency is required, as well as to operate both stages in cascade to reach higher voltage gains. For these reasons, the input interleaved boost will be followed by a second interleaved boost stage, that comes into play only when the required voltage gain is too high for a single boost stage. The strategy of management of the two stages can be adjust on-the-fly to increase the overall efficiency of the converter at the specific operating point.
Two boost stages can be cascaded, leading to the *Double Stage Boost* of figure 16a, or integrated in the FDB topology, leading to the *Floating Double Boost Double Stage Boost* converter (FDBDSB) of figure 16b.

The theoretical voltage gain of the configurations under analysis are compared in the graph of figure 17 with the maximum voltage gain M_{max}. Can be noticed that the FDB is theoretically capable of reaching the maximum voltage gain $Mmax$ by itself. This is not the practical case due to the parasitic resistance of the components and the maximum t_{on} of the controller. Then it is reasonable to predict that FDB by itself is not capable of reaching M_{max} with good efficiency. Both the

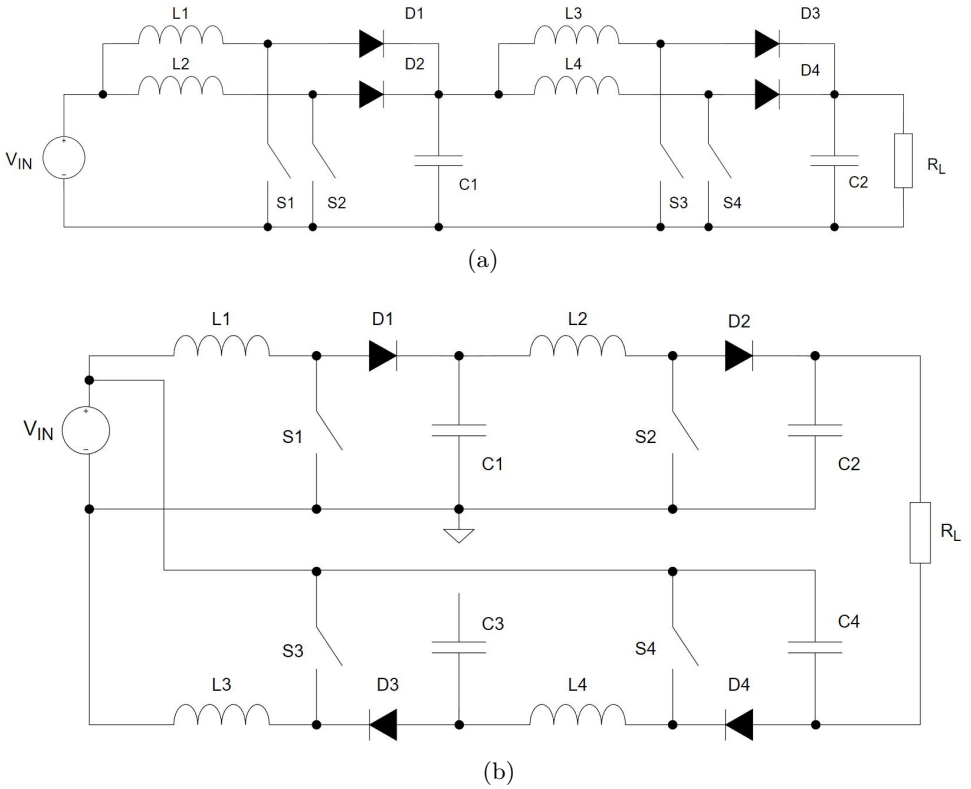


Figure 16: *Double Stage Boost* topology (DSB) (a), and *Floating Double Boost Double Stage Boost* (FDBDSB) (b)

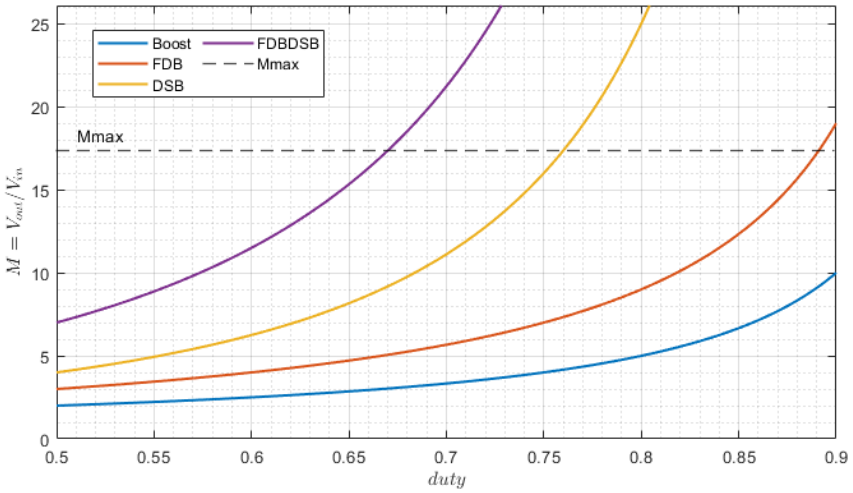


Figure 17: Voltage gain for different configurations: Boost, Floating double boost (FDB), Dual stage boost (DSB) and Floating double boost double stage boost (FDBDSB)

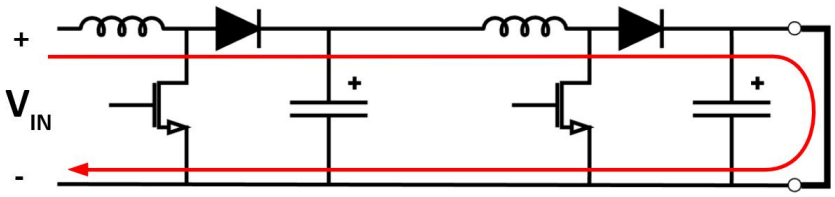


Figure 18: Current loop when the output is shorted

two cascaded configurations ,instead, reach the maximum voltage gain M_{max} with reasonable low values of duty cycle, so they both hit the voltage gain target. The configuration employing two basic boost stage in cascade is finally preferred over the FDBDSB topology, in terms of simplicity and since the ground connection can be shared between the input and output of the converter. The choosen topology is then presented in Figure 18.

The series of two boost stages has an intrinsic weakness: analyzing the condition of short circuit on the output, we can get rid of this potential issue. In figure 18 a short circuit is put at the converter output, the red line shows the path of the current flowing through the short circuit. When a short circuit occurs at the output, the output boost as well as the input boost has no chance to limit the current flowing through the short. In fact, the output voltage V_{out} becomes lower than the bus voltage V_{bus}. As a consequence, the freewilling diode of the output stage turns on. The same happens for the freewilling diode of the first stage. An uncontrolled

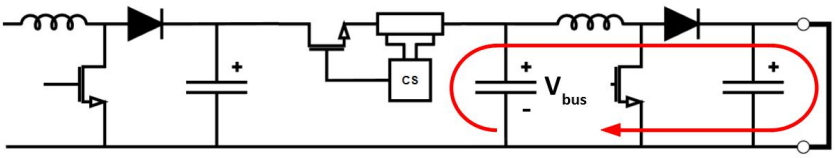


Figure 19: Current loop when the protection opens, one phase

current path is then established and the current is only limited by the short circuit resistance that is, by definition, very small. Please note that this loop exists even if the buck structure is synchronous, because of the body diode of the upper MOSFET. This potentially destructive condition, highlights the necessity of an intermediate stage capable of blocking the current flowing in the path of figure 18. Therefore the current flowing in the loop is measured, and a MOSFET is put in series to the current path. When the sensed current exceeds its threshold value, then the series MOSFET opens and the current loop is interrupted. The MOSFET is connected to have its body diode reversed in respect to the current flow.
This protection stage can be placed at any point of the current loop of figure 18, and the protection purpose is maintained. By the way, some consideration can be done to find the best placing point.

- At the input of the converter, the current is maximum. Then, if the protection stage would be placed at the input of the converter, this would reflect in high power dissipation in the series MOSFET due to the high input current.
- At the output of the converter, the voltage is maximum. This forces the selection of the MOSFET in the $1200\,V$ range, that has considerably higher on-resistance RDS_{on} than the $600\,V$ series. If the protecting stage would be placed at the output of the converter, the power dissipation on the series MOSFET would be high due to the high RDS_{ON}.

Make sense to place the protection stage in between the input and the output boosts, across the bus voltage V_bus. This allows to use the MOSFETs in the $600\,V$ series and, at the same time, the current is not as high as at the input.

When the protection circuit comes into play the inductor resonates with the bus capacitance, causes high voltage spikes across the switch. The protection circuit is completed by adding a freewilling diode to clamp the bus voltage to zero when until the entire magnetic energy of the output boost inductors is fully discharged. Figure 20 depicts the final configuration of the converter stages, as well as the current loop when the short-circuit protection comes into play. If look closely to the protection stage topology, can be recognized the configuration of a buck stage. A different management of the short circuit condition can be used: instead of abruptly interrupt the output current when a short circuit is detected, the average output current can

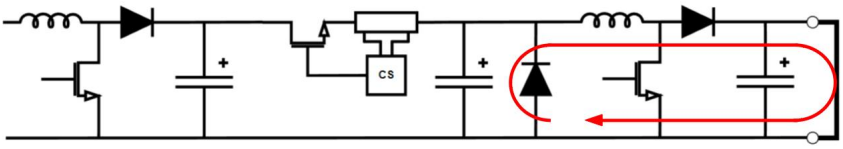


Figure 20: Current loop when the protection opens, freewilling diode

be controlled by operating the protection stage as a buck stage. If considered that this converter will be permanently mounted on the vehicle, and no accidental short circuit can occur, then the short circuit condition represents a fault in the battery system, and a rapid disconnection of the converter is expected. For this reason the protection stage is designed to act quickly at the overcurrent detection, and no buck operation of the stage will be developed.

The schematic overview of the converter is depicted in the Figure 21, the interleaved structure of the two boost stages is highlighted. The control strategy of the converter is highlighted with green arrows: a microcontroller sets the reference point for the control loops of the stages. The microprocessor also communicates withe the FCC and ECU to get the operating point data and to transmit functional parameters such as currents,voltages and temperatures.

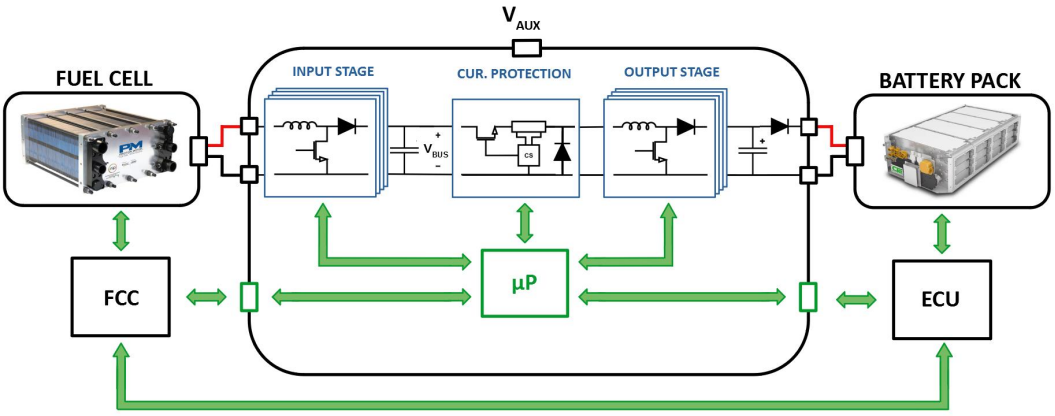


Figure 21: Total block diagram of converter in its intended application

3.1 Input Stage

The input stage of the converter is an interleaved boost stage, as shown in previews Figure 21. The input port is characterized by high current, up to $100\,A$, while the output voltage of the stage V_{bus} reaches a nominal value of $200\,V$ and a maximum value around $250\,V$. In this context of increased current and reduced voltage, a

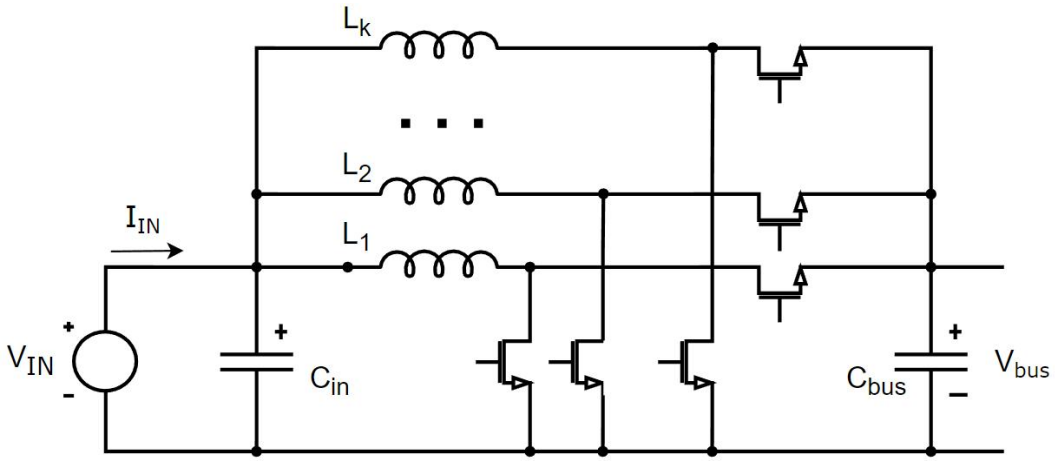


Figure 22: Starting schematic of the input interleaved boost stage

synchronous boost is preferred to the standard one (with diode) since the conduction power losses are strongly reduced. In the next section is developed the design of the stage.

3.1.1 MOSFET selection

In the past, converters in electric vehicle were conventionally implemented by silicon active devices and p-i-n diodes. Transiting from silicon MOSFET to fast switching wide bandgap technologies is expected to improve the performance and efficiency of EVs. Using GaN or SiC power MOSFETs instead of traditional Silicon (Si) power MOSFETs offers several benefits in terms of performance and efficiency. GaN devices offer faster switching speeds, lower power losses, and better high-frequency performance, while SiC devices handle higher voltage applications and are more robust and reliable. Both GaN and SiC offer lower thermal resistance, allowing for higher power density and improved thermal management. In the paper [9], 600V power Si,SiC and Gan devices have been compared. The SiC and GaN devices show superior on-state as well as switching behavior compared to Si unipolar and bipolar devices, as reported in figure 23 Choosing Silicon Carbide (SiC) over Gallium Nitride (GaN) power MOSFETs can be a suitable option in certain high-voltage applications. SiC devices have a higher breakdown voltage, up to ten times higher than Silicon (Si) power MOSFETs, and can operate at high voltage levels up to 1.2kV and beyond, making them suitable for high voltage applications. Additionally, the higher thermal conductivity of SiC, compared to GaN and Si, results in better heat dissipation, allowing for higher power density and improved thermal management. SiC power MOSFETs also offer lower on-resistance, reducing the power losses and increasing the efficiency compared to Si and GaN devices. The lower on-resistance allows for higher current handling capability and higher switching frequencies, which are crit-

Device	$R_{on,sp}$ (mΩ cm^2)		Switching simulations (300 V, 5A, R_g = 0, T = 150 °C)		Total loss (Duty cycle = 50%, f= 25kHz)
	25 °C	150 °C	Eoff (µJ)	Eon (µJ)	(µJ)
Si FS-IGBT	7.8	8.1	770	480	1371
Si SJ-MOSFET	8.6	18.6	18	0.5	205
SiC UMOSFET	1.1	1.6	1	0.1	17
GaN HEMT	0.7	0.9	0.6	0.1	10

Figure 23: Si SiC and GaN 600V power devices comparison

ical in high-power applications. Furthermore, SiC MOSFETs are more established technology and have a longer history of use compared to GaN, making them a more reliable option in terms of long-term stability. Another important advantage of SiC over GaN technology is the SiC capability to withstand overvoltage events without intrinsic damages. When V_{DS} increases over the BV_{DS} (Drain-Source breakdown voltage) the drain-gate diode of the SiC JFET turns-on causing a current in the gate driving circuit, the MOSFET turns on blocking the overvoltage event.
These benefits of SiC over GaN devices makes them the most suitable choice for this project. The best SiC power MOSFET part number is selected over many parameters, the ones considered in the selection are listed in the Table 10. By the way, the actual extreme lack of electronic components on the market forces the availability to be one fundamental parameter to consider in the power MOSFET device selection. A research on the market has point out the most suitable parts for this application, only the available components have been considered. The comparison between the MOSFETs is made easy to visualize in the spider-net diagram of figure 24: every part number represents a closed broken line, the closer to the origin the line intercept the axis the best suited that MOSFET is. The overall best trade-off is represented by the part-number **MSC015SMA070B4**, it exhibits the lowest area in the graph and its parameters are the lowest or closer to the lowest in every axis. It is not the cheapest transistor in the set, but it is a reasonable price to pay for its performances.

3.1.2 Number of phases

The number of phases of the input interleaving boost is set to operate the MOSFETs below the critical junction temperature of $T_{j,crit}$. In fact, the more the number of phases, the less the current flowing in each phase. The consequent reduction in the phase current leads to the reduction of the conduction and commutation losses of every MOSFET. Of course, the higher the number of phases the higher the cost and complexity of the stage: oversize the number of phases is not a good choice in this project.
The critical junction temperature has set to $T_{j,crit} = 125\,°C$ to keep some degrees

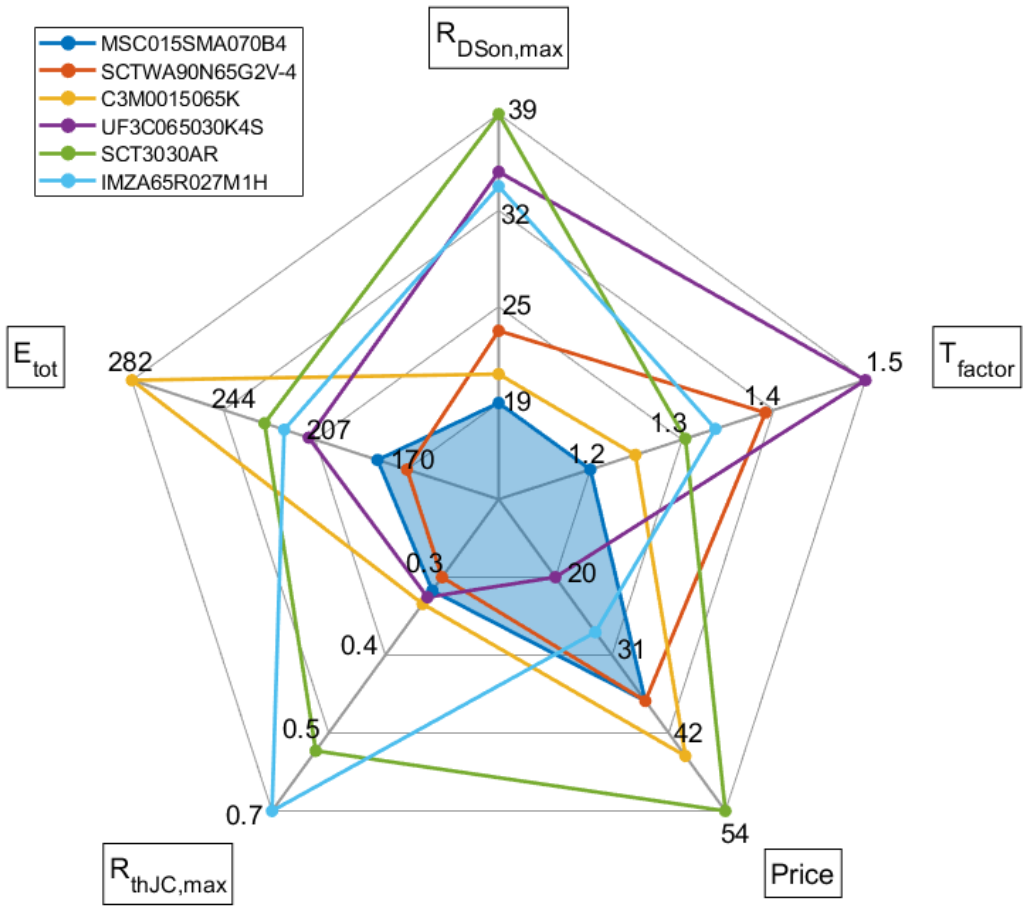


Figure 24: Spider-net diagram for the selection of the power MOSFET for the input boost stage

Table 10: Description of the parameters considered for the selection of the MOSFET part-number of the input stage

Parameter	[*unit*]	**Description**
$R_{SDon,max}$	$m\Omega$	Is the maximum on-state channel resistance, when the junction temperature is 25°.
T_{factor}	*none*	This parameter accounts for the variation of the on-state resistance due to the junction temperature increasing. Multiplying this coefficient to the parameter $R_{DCon,max}$ returns the channel resistance at a junction temperature of 150°.
Price	€	It is the average commercial price for one piece.
R_{thJC}	K/W	Thermal resistance from junction to case. The maximum value (worst case) is considered.
E_{tot}	μJ	Energy dissipated during one inductive commutation with $V_{DS} = 400V$ and $I_D = 25A$. It is proportional to the commutation losses of the component.

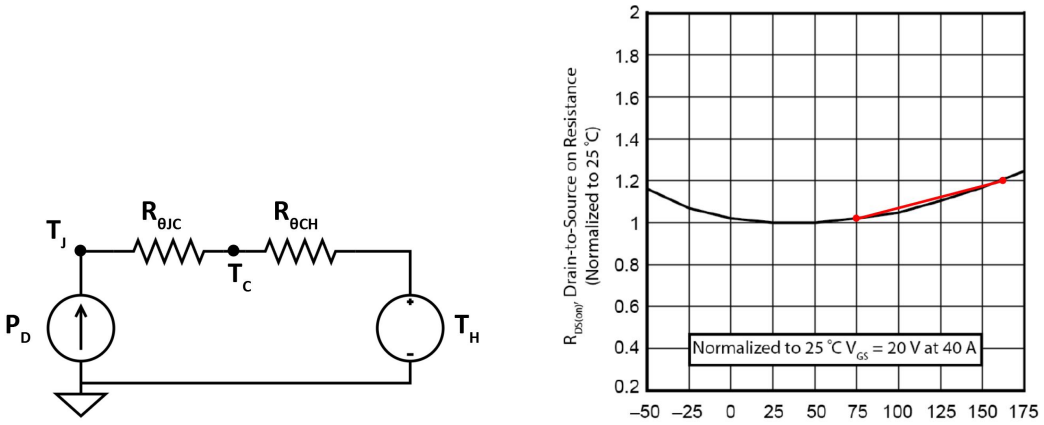
of margin over the absolute maximum junction temperature $T_{j,max} = 150°C$. The MOSFET selected in previous section exhibits a absolute maximum junction temperature of $175°C$, by the way, this value for other part numbers in the selection list drops to $150°C$. In order to face the market availability, the project rely on an absolute maximum junction temperature of $T_{j,max} = 150°C$ so that there are some margin even to use devices with maximum junction temperature of $150°c$.
The selection of the number of phases bases on thermal aspects, then the average thermal model of the stage is developed. For a single phase the equivalent electric representation of the thermal model is presented in Figure 25a.

The analysis is based on a constant baseplate temperature $T_h = 80°C$, according to the baseplate thermal simulation of section 2.3. Then, the junction temperature T_j of the MOSFET follows from the baseplate temperature, the thermal resistance $R_{th,tot}$ and the dissipated power P_D, as in equation (14):

$$T_j = T_h + P_D \cdot R_{th,tot} \tag{14}$$

The total thermal resistance results in $R_{th,tot} = 1.21\,K/W$, it is the sum of the thermal resistance junction-case $R_{th,jc} = 0.21\,K/W$ and the thermal resistance case-baseplate $R_{th,ch}$. The last parameter, for a *TO-247* package, is investigated in the Infineon application note *AN2017-01* [10] and results in $R_{th,ch} = 1\,K/W$.

The drain-source on-resistance $R_{DS,on}$ of the MOSFET is affected by the junction temperature T_j of the MOSFET itself. At room temperature, the nominal



(a) (b)

Figure 25: Average thermal model for a MOSFET (a) and $R_{DS,on}$ variation over temperature(b)

value for the selected component is $R^{25}_{DS,on} = 19\,m\Omega$, maximum. From the component datasheet, the behavior of the channel resistance in respect of the junction temperature is shown in figure 25b. As expected the channel resistance exhibits rising value in response to a temperature increase. The curve is well approximated in the temperature range $75 - 160\,°C$ by the red line of figure 25b. Under this linear approximation, the on-state channel resistance results in equation (15).

$$\begin{aligned} R_{DS,on} &= R^{25}_{DS,on} \cdot (q + m \cdot T_j) \quad , \quad T_j \in (75 - 160)°C \\ m &= 2\,10^{-3} \quad T^{-1} \\ q &= 8.8\,10^{-1} \end{aligned} \tag{15}$$

The power P_D dissipated by the MOSFET is the sum of the conduction and commutation losses. The conduction losses relate to the resistive losses during conduction, they can be evaluated as

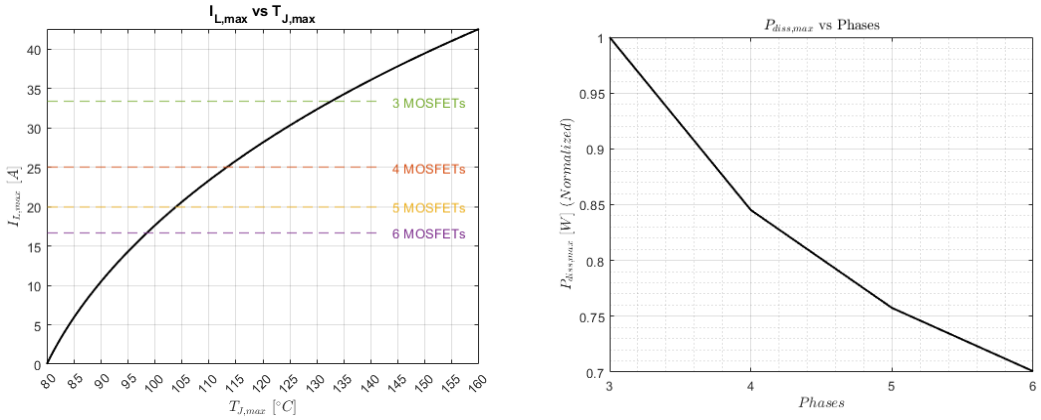
$$P_{cond} = R_{DS,on} \cdot I_L^2 \cdot D \tag{16}$$

The commutation losses relate to the commutation of the MOSFET under inductive load, they can be computed as:

$$P_{comm} = V_{bus}\, f_s\, \frac{tri + tfv + trv + tfi}{2}\, I_L \tag{17}$$

Small ripple approximation is done on the inductor current. The rising time for the drain-source voltage and the drain current t_{rv} and t_{ri} are assumed to be $12\,ns$, the falling time of voltage is $t_{rv} = 7\,nS$ while the falling time of the current t_{fi} is neglected. Then

$$K = 1/2(t_{ri} + t_{fi} + t_{rv} + t_{fv}) = 15,5\,ns \tag{18}$$



(a) (b)

Figure 26: Phase current over maximum junction temperature (a) and normalized dissipated power over phases number (b)

Please note that this is just a rough approximation of the losses in the bottom MOSFET, that is enough for the selection of the number of phases but it is not intended to be an accurate estimation.
The following equations can be grouped into the system of equations (19), the solution leads to the graph presented in Figure 26a.

$$\begin{cases} T_j & = T_h + P_d \cdot R_{th,tot} \\ R_{DS,on} & = R^{25}_{DS,on} \cdot (q + m \cdot T_j) \\ P_d & = R_{DS,on}\, I_L^2 + V_{bus} I_L f_s K \end{cases} \tag{19}$$

The result of Figure 26a states that four phases is the minimum number of phases to keep the junction temperature below the critical value $T_{j,crit} = 125°C$. Further increasing in the number of phases leads to restricted benefits in terms of power dissipation, as presented in Figure 26b. For both reasons the number of phases has set to four.

3.1.3 Inductor design

Every one out of the four interleaved phases presents the same value of inductance $L_1 - L_4 = L_{nom}$. In the following design it is assumed that the total average current is equally split between the four phases, so that holds equation (20).

$$I_{L,nom} = \frac{I_{in,nom}}{N} = 25\,A \tag{20}$$

The inductor design relates to this two quantities:

1. The inductor maximum peak current $I_{L,pk}$
2. The nominal inductance value L_{nom}
3. The inductor maximum *rms* current I_L^{rms}

First derive the inductor maximum peak current $I_{L,pk}$, that it is necessary to avoid the core saturation issue. The maximum peak value composes of the maximum average current $I_{L,nom}$ and half the maximum peak-peak current ripple (21).

$$I_{L,pk} = I_{L,nom} + \frac{\Delta I_{L,max}}{2} \tag{21}$$

The maximum inductor current ripple $\Delta I_{L,max}$ is a design choice: the higher the parameter the smaller the AC component of the inductor current, but the higher the inductance value L. By choice, this parameter has set to the 40% of the maximum average current.

$$\Delta I_{L,max} = 0.4 \cdot I_{L,nom} \tag{22}$$

Follows the maximum peak value of the inductor current, equation (23), that will be considered in the core selection process.

$$I_{L,pk} = I_{L,nom} + 0.4 \cdot I_{L,nom}/2 = 30\,A. \tag{23}$$

The relation of the current ripple $\Delta I_{L,max}$ in a boost stage is

$$\begin{aligned} \Delta I_{L,max} &= \frac{V_{in}}{f_s \cdot L_{nom}} \cdot D \\ &= \frac{V_{bus}}{f_s \cdot L_{nom}} \cdot \underbrace{\frac{1}{M}(1 - \frac{1}{M})}_{A}. \end{aligned} \tag{24}$$

The "A" term maximizes for M = 2, therefore $\Delta I_{L,max}$ is maximum for$M = 2$ and $V_{bus,nom} = V_{bus,max} = 250\,V$. This condition occurs for $V_i = 125\,V$, that is an effective valid input voltage to get $I_L = I_{L,max}$.

$$\begin{aligned} L_{nom} &= \frac{V_{bus,nom}}{4 \cdot f_s \cdot \Delta I_{L,nom}} \\ &= 62,5\,\mu H \end{aligned} \tag{25}$$

with the target switching frequency of $f_s = 100\,kHz$. At this point, both L_{nom} and $I_{L,pk}$ are known and the core size can be properly selected. The maximum *rms* inductor current will be computed later, once the saturation of the core can be evaluated.

Magnetic core selection. The selection of the core needs to consider: the core type, the core material and the physical size. First the core type is selected, over

gapped or distributed-airgap cores. The Distributed-airgap toroid cores are cheaper, compared to the gapped cores, because less constructive tasks are required. In addition, the toroid-based inductor can be better cooled once drowned into thermal-conductive resin: the wire can be wound in such a way to allow the resin to reach both the core and all the windings. This ensure a more uniform temperature of the inductor, in respect to the gapped inductors where inner windings are hotter then the external ones. Because the inductor electrical performance remains almost the same with the two types o cores, then the distributed-airgap toroid core has selected. In power inductor applications, such as switched-mode power supply (SMPS) in CCM operation, the filter inductances experience a larger DC current component compared to the high frequency AC one. They are typically realized with powder cores, different materials are available:

- Molypermalloy Powder (MPP)
- High Flux
- Kool Mμ ®

For the lowest loss inductor, MPP material should be used since it has the lowest core loss. For the smallest core size in a dc bias dominated design, High Flux material should be used since it has the highest flux capacity. For reasonably low losses and reasonably high saturation at a low cost, Kool Mμ ® should be used since it has the lowest material costs. The company experience has fount through the years the Kool Mμ ® cores to be the optimum trade-off between space consuming,core losses and price.
The *Magnetics* manufacturer provides the selection graph of Figure 27, that suggest a sizing of the core based on the parameter "LI^2".

$$LI^2 = L_{nom} \cdot I_{L,pk} = 56 \quad mH \cdot A^2 \tag{26}$$

The cores "77439-A7" has been selected, it is a little smaller than the one suggested by the graph due to the space constraint. The core parameters are shown in figure 28a, from the value of the nominal inductance-per-turn "A_L" comes the number of turns:

$$\begin{aligned} T &= \sqrt{\frac{L_{nom}\,[nH]}{A_L}} \\ &\simeq 22\,turns \end{aligned} \tag{27}$$

T is the number of turns necessary to obtain an inductance value of L_{nom} at zero $Ampere{\cdot}Turn$ operating point. For operating point with current different from zero, then the magnetic flux imposed by the DC operating point causes the magnetic permeability of the core to decrease, with a consequent decrease in the nominal inductance-per-turn parameter "A_L". Considering the nominal input current $I_{in,nom}$

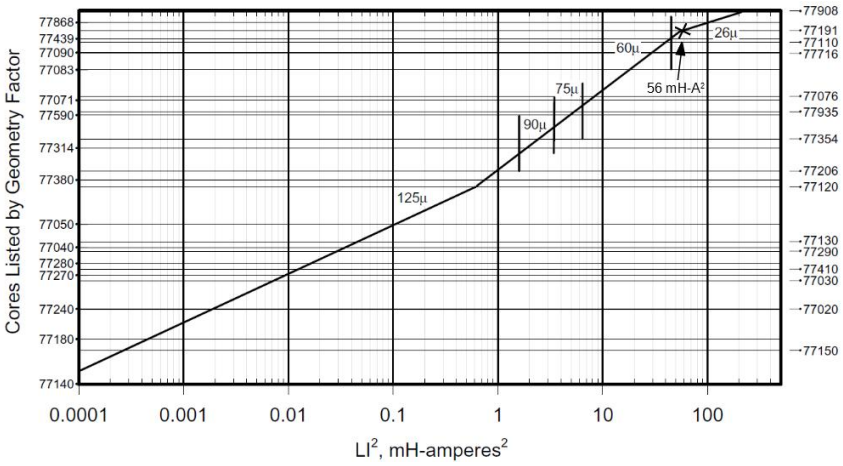


Figure 27: Input inductor core selection graph

holds equation (28) and the decrease in the inductance-per-turn value is presented in the graph of Figure 28b, it decreases down to $A_L^{load} \simeq= 79\,nH/turn^2$.

$$AT = T \cdot i_{L,nom} = 660\ [AT] \tag{28}$$

Then, the effective inductance value at the nominal current condition results in (29) and the consequent increase in the inductor current ripple is computed in (30).

$$\begin{aligned} L^{load} &= A_L^{load} \cdot T^2 \\ &\simeq 38.2\,\mu H \end{aligned} \tag{29}$$

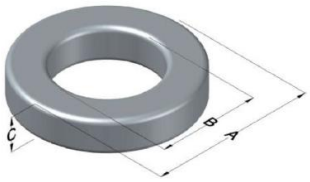
$$\begin{aligned} \Delta I_L^{load} &= \frac{A_L}{A_L^{load}} \cdot \Delta I_{L,max} \\ &= 16.3\,A \end{aligned} \tag{30}$$

A posteriori is checked that the maximum magnetic flux density B^{load} doesn't exceed the maximum core value $B_{max} \simeq 0.6\,T$, otherwise the core will saturate.

$$B^{load} = \frac{L^{load} \cdot I_{L,max}}{T \cdot Ae} = 0.289\,T \tag{31}$$

$A_e = 199\,mm^2$ is the core cross section. The magnetic flux B^{load} is well beyond the limit B_{max} so the inductor is not expected to saturate.

Copper wire sizing. The cross section of the copper wire is sized on the maximum inductor *rms* current $I_{L,nom}^{rms}$. The typical shape of the induction current ripple, under



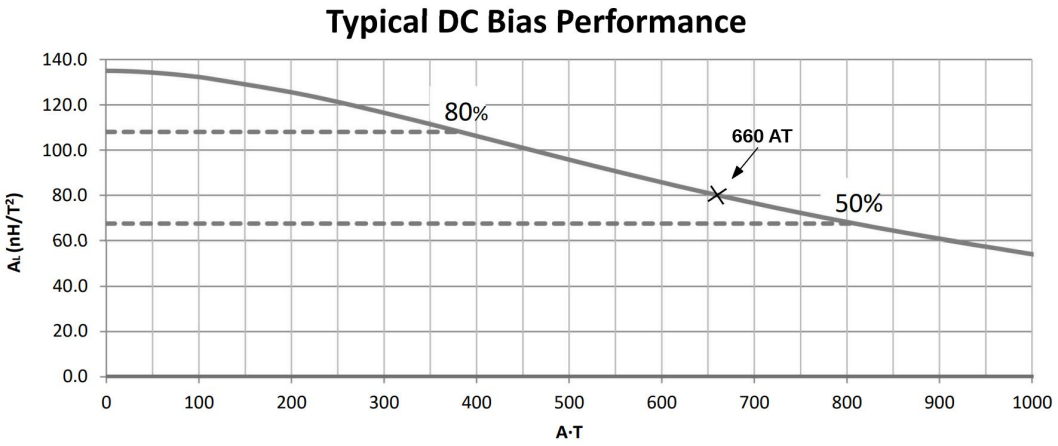
Kool Mμ Permeability (μ)	A_L (nH/T²)	Core Marking			Coating Color
		Lot Number	Part Number	Inductance Grade	
60	135 ± 8%	XXXXXX	77439A7	N/A	Black

Dimensions	Uncoated		Coated Limits			Packaging
	(mm)	(in)	(mm)	(in)		
OD (A)	46.74	1.840	47.63	1.875	max	Cardboard cut-outs Box Qty= 105 pcs
ID (B)	24.13	0.950	23.32	0.918	min	
HT (C)	18.03	0.710	18.92	0.745	max	

Electrical Characteristics			Physical Characteristics						
Watt Loss @ 100 kHz, 100mT max (mW/cm³)	DC Bias min (oersteds)		Voltage Breakdown wire to wire min (V_{AC})	Break Strength min (kg)	Window Area W_A(mm²)	Cross Section A_e (mm²)	Path Length L_e (mm)	Volume V_e (mm³)	Weight (g)
	80%	50%							
750	39	87	3000	233	427	199	107	21,300	120

Winding Information						Temperature Rating
Winding Length Per Turn				Wound Coil Dimensions (mm)		Curie Temp: 500°C
Winding Factor	(mm)	Winding Factor	(mm)	40% Winding Factor	OD 51.2	Coating Temp (Continuous up to): 200°C
					HT 26.0	
0%	62.1	40%	74.1	Completely Full Window	Max OD 63.8	Notes:
20%	68.2	45%	76.0		Max HT 38.7	
25%	69.7	50%	77.6	Surface Area (mm²)		
30%	70.9	60%	81.2	Unwound Core	6,900	
35%	72.7	70%	85.4	40% Winding Factor	9,600	

(a)



(b)

Figure 28: Core "77439-A7" parameters (a) and saturation of nominal inductance A_L (b)

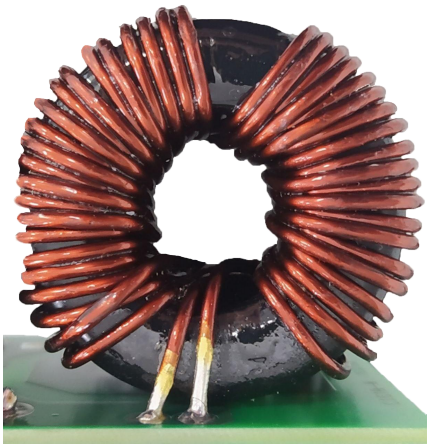


Figure 29: Input boost inductor realization

CCM operation, is a triangular waveform with a DC offset and its *rms* value may be computes as in equation (32).

$$I_{L,nom}^{rms} = I_{L,nom} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L^{load}}{I_{L,nom}}\right)^2} \\ = 25.4\, A_{rms} \tag{32}$$

The "skin effect" due to the ac component of the inductor current is neglected, the following calculations remains valid till the current is uniformly distributed into the conductor section. It is also neglected the increase in the copper resistivity due to the temperature rise.
Imposing a current density of $J = 5\, A/mm^2$, the required copper section is

$$A_w = \frac{i_{L,nom}^{RMS}}{J} \simeq 5\, mm^2 \tag{33}$$

A single wire with section $A_W = 5\, mm^2$ would be really difficult to handle, two wires of section $A_W/2$ are chosen instead. The core inner area has an occupation factor that is about $25 - 30\%$, that is quite low, this means that the wire section can be increased if needed. The Inductor realization is depicted in the Figure 29.
The power-loss in the inductor consist basically of two components: the losses in the copper wires, due to the inductor I_L^{rms} current, and the losses in the core, due to the AC component of the inductor current.

Inductor copper-loss. To compute the losses in the inductor wires the inductor parasitic series resistance r_L need to be estimated. From the core parameters of Figure 28a the mean length-per-turn $l_t = 63.7\, mm$, then the total length of the

winding wire is:

$$l_W = T \cdot l_t = 1.4\,m. \tag{34}$$

Then, the inductor DC resistance r_L leads from the second Ohm-law

$$r_L = \rho_{cu}\frac{l_W}{A_W} = 4.9\,m\Omega \tag{35}$$

The maximum power-loss in the winding wires is computed in equation (36)

$$P_{cu,max} = r_L \cdot \left(I_{L,max}^{RMS}\right)^2 = 3.16\,W \tag{36}$$

Inductor core-loss. Core loss is generated by the changing magnetic flux field within the core material, since no magnetic materials exhibit perfectly efficient magnetic response. Core loss is a function of half of the AC flux swing B_{pk} and switching frequency f_S. The parameter B_{pk} is defined as half of the AC flux swing:

$$B_{pk} = \frac{\Delta B}{2} = \frac{B_{AC,max} - B_{AC,min}}{2} \tag{37}$$

In the worst case, i.e. higher losses, the peak magnetic flux B_{pk} results

$$B_{pk,max} = \frac{L^{load} \cdot \Delta I_L^{load}}{2 \cdot T \cdot Ae} = 71\,mT \tag{38}$$

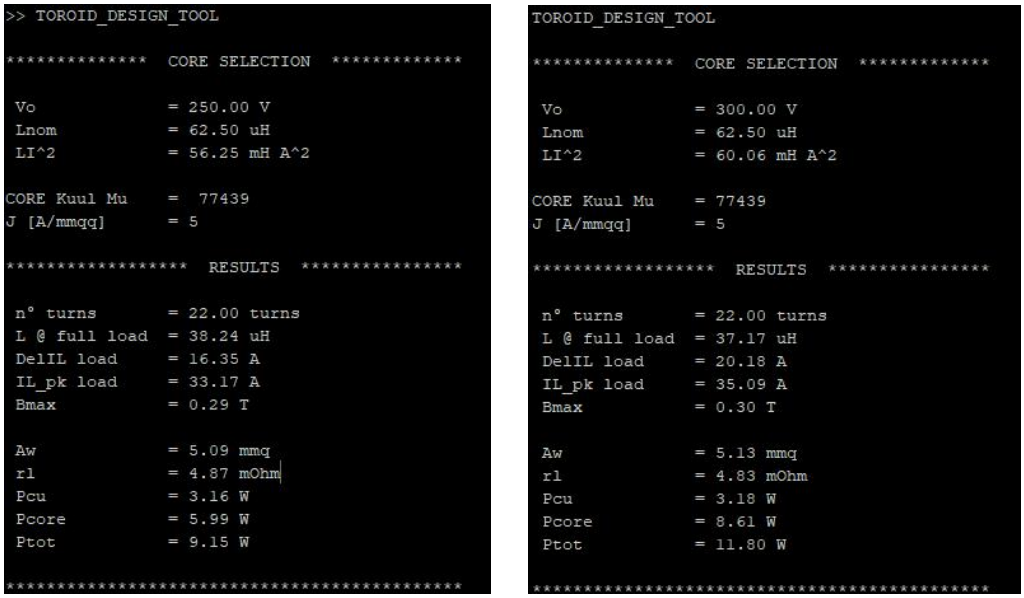
Then, the core losses results from equation (39) with $a = 44.3\,mW/mm^3, b = 1.988, c = 1.541, V_e = 21,3\,mm^3$ for the Kool Mμ ® 77439-A7 selected core.

$$\begin{aligned} P_{c,max} &= a \cdot B_{pk,max}^b \cdot f^c \cdot V_e \\ &\simeq 6\,W \end{aligned} \tag{39}$$

Inductor total loss. The maximum total losses in the inductor occurs when the average inductor current is maximum, the bus voltage is maximum and the input voltage is half the bus voltage. With the bus voltage set to $V_{bus} = 250\,V$, the total loss results in equation (40).

$$\begin{aligned} P_{L,max} &= P_{c,max} + P_{cu,max} \\ &= 9,16\,W \end{aligned} \tag{40}$$

The analysis of this section is based on the assumption of a bus voltage equal to $V_{bus} = 250\,V$. By the way, during the efficiency optimization process carried out in the experimental section 5.2, the bus voltage could be increased up to $V_{bus,max} = 300V$. Make sense to evaluate the power-loss of the inductor even for that bus voltage. The inductor design and inductor power-loss calculation implemented in a Matlab script: Figure 30a agree with previous calculation for $B_{bus} = 250V$, while Figure 30b shows the results for a bus voltage of $V_bus, max = 300V$.



(a) (b)

Figure 30: Inductor design parameters and inductor power-loss for $V_{bus} = 250V$ (a) and $V_{bus} = 250V$

3.1.4 Input capacitor design

The ripple of input current may induce a ripple on the input voltage due to the fuel-cell and connection impedances, as well as degrades the fuel cell efficiency. For this reason it is desirable to provide a low impedance path for the current AC component to close back, as close as possible to the input side of the boost inductors. This path is provided by the input capacitor. A correct selection of the capacitor requires to determine the frequency f_{in} and the rms value $I^{rms}_{in,max}$ of the input current.
The total input current has a frequency that four times higher than the switching frequency f_s, because of the ripple frequency multiplication effect of the interleaved configuration. This effect is clearly visible in the Figure 31 that shows the current of the four phases and the total input current as sum of the single currents. The input current ripple has frequency equal to :

$$f_{in} = 4 \cdot f_s = 400\,kHz \tag{41}$$

The ripple amplitude of the total input current for an interleaved structure is highly dependent on the duty cycle of the converter, and the behavior is associate to the number of phases. In the Figure 32 is computed the profile of the peak-peak ripple of the total input current for different number of phases. The plot is valid for every operating point of the boost stage, in particular make sense to study the condition

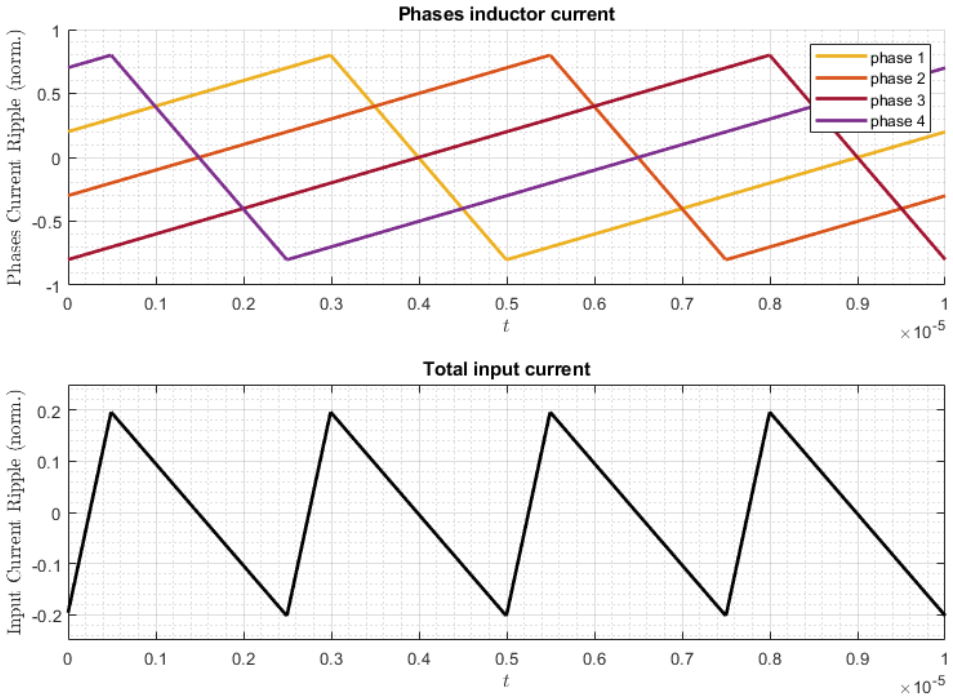


Figure 31: Simulation results of the input current ripple of a four leg interleaved boost and a single leg boost

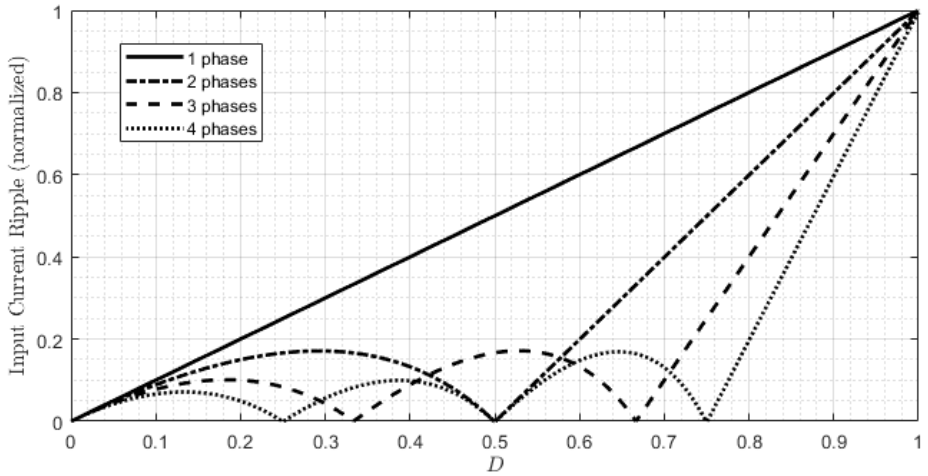


Figure 32: Peak-peak ripple of the total input current, for an interleaved boost structure with different number of phases

Table 11: Input current ripple for different values of duty cycle, four phases are considered.

D_{max}	$I_{in,pk-pk}$	$I_{in,rms}$
0.8	$3.26\,A$	$0.94\,A_{rms}$
0.9	$9.78\,A$	$2.82\,A_{rms}$
0.95	$13.04\,A$	$3.76\,A_{rms}$

of maximum input average current: the inductance value is minimum and the ripple current amplitude is maximum. This is, of course, the worst scenario for the input capacitor in terms of ripple current. Considering the normalization factor equal to ΔI_L^{load}, from the graph of Figure 32 are derived the input current ripple values listed in Table 11. The table provides the minimum *current ripple RMS* rating of the input capacitor, over the maximum duty cycle expected for the stage. To handle the input current ripple, the capacitor experiences frequencies from $f_{in} = 400kHz$ to higher order harmonics. For this frequencies, to use one or more MCC capacitors is a common choice, its capacitance value is computed in equation (42) for a maximum input voltage ripple is fixed to $\Delta V_{in} = 2\,V$ and a maximum input current ripple is $\Delta I_{in,pk-pk} = 13.04\,A$.

$$C_{IN} = \frac{\Delta I_{in,pk-pk}}{8 \cdot f_{in} \cdot \Delta V_{in}} = 8.15\,\mu F \tag{42}$$

Two $4.7\mu F$ MCC capacitors are placed in parallel, each must be capable of sustain an *rms* current of about $1A$.
The MLC input capacitors need to sustain voltage up to $275V$, then $450\,V$ rated capacitor have been selected. In fact the ceramic capacitor has strong dependence of capacitance value over operating-voltage, as a rule of thumb the component should be rated for twice the maximum operating voltage.
In addition to the ceramic capacitors, also electrolytic capacitors are placed at the input of the converter: they play the role of energy tank smoothing the input voltage. The larger the input capacitance, the better the benefits on the converter: $3x150\,\mu F$ electrolytic capacitors complete the input capacitors set. Their rated voltage is $400V$, the choose of the number and dimension of the capacitors relies on cost and occupied space in the board.

3.1.5 Bus capacitor design

The output capacitor plays a crucial role in smoothing the output voltage in a boost converter stage and ensuring stability of the circuit. To meet these requirements, the capacitance value of the output capacitor must be chosen based on the desired output voltage ripple. Increasing the capacitance value can reduce the output voltage ripple, but may also slow down the response time of the circuit. For this converter, it is not

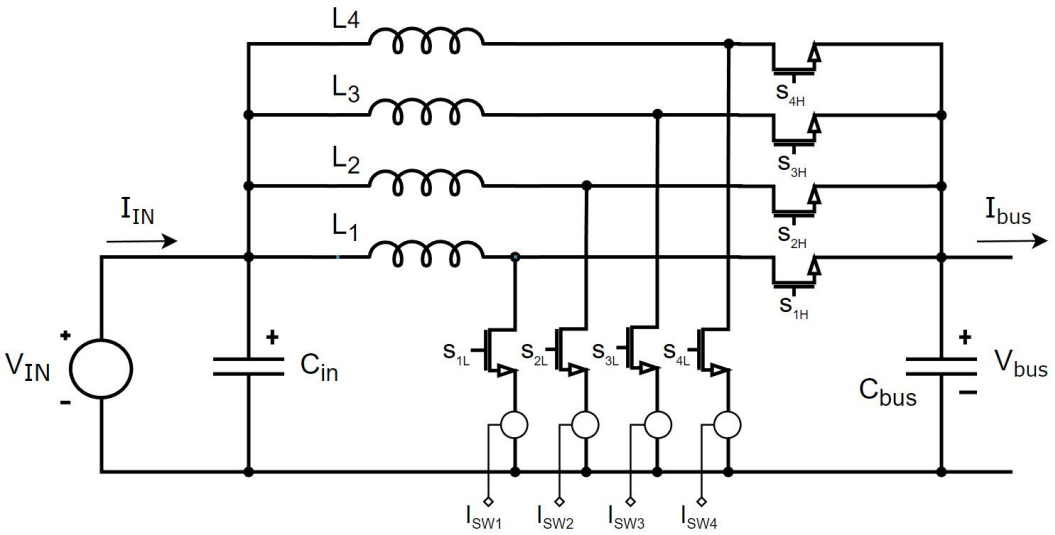


Figure 33: Basic electrical schematic of the input boost stage

required an high bandwidth of the control loop, so the bus capacitance will oversized to reduce the voltage ripple. The capacitor is therefore designed as the input boost would have no interleaving structure, but a single phase carrying all the current. The bus capacitance is computed in equation (43), it is considered the worst case condition consisting in $V_{in} = 150V$, $V_{bus} = 250V$ and $I_{bus} = 60A$ (maximum voltage gain of the input boost stage during full power operation).

$$C_{bus} = \frac{I_{bus} \cdot D}{f_s \cdot \Delta V_{bus}} = 245\,\mu F \tag{43}$$

The ripple on the bus voltage is assumed to be ΔV_{bus}. Also the *ESR* of the output capacitor adds some more ripple that is set to $\Delta V_{bus,ESR} = 0.5V$, then the *ESR* value results

$$ESR = \frac{\Delta V_{bus,ESR}}{\frac{I_{bus}}{1-D} + \frac{\Delta I_L}{2}} = 4.6\,m\Omega \tag{44}$$

To meet requirements of equation (43) and (44), across the bus voltage are placed three $100\mu F$ electrolytic and two $4,7\mu F$ *MLC* capacitors. The voltage ratings are $400V$ and $600V$, respectively. The essential schematic of the input boost stage is depicted in Figure 33.

3.1.6 Driving circuit

The MOSFET driver plays a critical role in ensuring fast and efficient turn-on and turn-off of the MOSFET in power electronic systems. Rapid switching is important

Table 12: Auxiliary converter voltage specifications

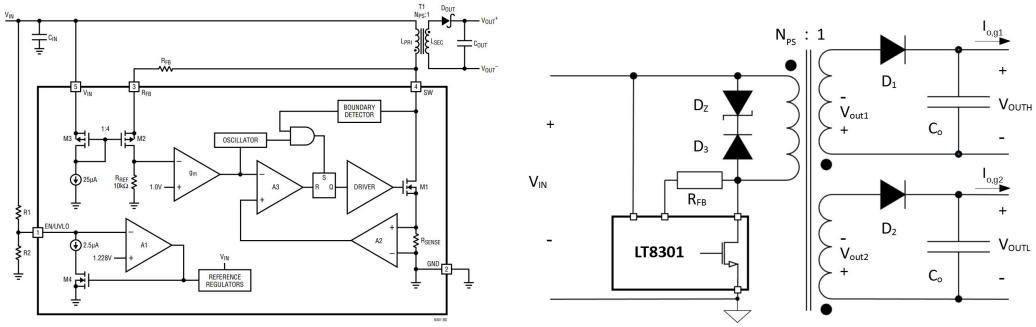
Parameter	**Symbol**	**Value**
Input voltage	V_{in}	$24\,V$
Output voltage 1	V_{OUTH}	$22\,V$
Output voltage 2	V_{OUTL}	$22\,V$

for reducing switching losses and improving power conversion efficiency.
With reference to the schematic of Figure 33, the driving of the top MOSFETs $S_{h1} - S_{h4}$ are not straightforward, since their sources are connected to the switching nodes, who's potential is time varying by definition. For every top MOSFET, the gate driver is connected between the MOSFET gate and source, then an isolated power supply is necessary to power the driving circuit. In addition to this, every bottom-MOSFET source is connected to the ground through a current transformer, to sense the switch current. This means that neither the bottom MOSFET source is connected to ground, and even to drive the bottom MOSFETs isolated power supplies and drivers are required. The input boost stage then requires a total of eight isolated power supplies, two for every phase of the interleaved topology.
This result could be achieved by a single auxiliary converter, with eight isolated outputs. By the way, this solution is not very robust: if the auxiliary converter fails, the total input stage is out of use and the entire converter operability is compromised. From this point of view, it is convenient to separate the auxiliary power supplies, introducing one dedicated auxiliary converter for every one of the four phases. Every converter, then, provides the two isolated power supplies necessary to drive the high and low MOSFET of that phase.

The main key-points for the auxiliary converter are the following:

- Effectiveness: the converter topology should be minimal, to reduce occupied space in the PCB.
- Relaxed output specifications: output voltage ripple and output voltage line regulation are not a first order aspect as they lightly impact the MOSFET driving capability.
- Isolation: the transformer must include isolation tape layers between the primary and secondaries side, as well as between the two secondary windings themselves.

Controller IC. A relevant aspect in every isolated topologies is how to transmit back the output voltage information, from the isolated secondary side of the transformer to the primary side for regulation. Historically, opto-isolators or extra transformer windings communicate this information across the isolation boundary.



(a) (b)

Figure 34: LT8301 controller internal diagram (a) and converter implementation (b)

Both solutions increase the cost and add extra components. Using the LT8301 controller [11] from "Analog Devices", it is possible to realize a flyback converter with no extra feedback-couplers. In fact, the *LT8301* controller senses the output voltage directly at the primary-side, through the flyback pulse waveform, when the main switch is off. In Figure 34a is shown the internal structure of the *LT8301* controller, while in figure 34b is shown how it is implemented this project. The feedback resistor R_{FB} is the only feedback component, and it is used to set the output voltage. The difference between the SW pin voltage and V_{IN} supply, is given as:

$$V_F = (V_{OUT} + V_D + i_{SEC} \cdot ESR) \cdot N_{PS} \tag{45}$$

where i_{SEC} is the secondary winding current, ESR is the total impedance of the secondary circuit, V_D the diode foreword voltage and N_{PS} is the secondary-to-primary turns ratio. Since the LT8301 operates in either boundary conduction mode or discontinuous conduction mode, the output voltage is always sampled on the SW pin when the secondary current is zero. The term depending on the secondary current is than ineffective, and the flyback pulse amplitude reduces to:

$$V_F = (V_{OUT} + V_D) \cdot N_{PS} \tag{46}$$

The flyback voltage is then converted to a current I_{RFB} by the flyback pulse sense circuit (M2 and M3). This current I_{RFB} also flows through the internal 10k R_{REF} resistor to generate a ground-referred voltage. The resulting voltage feeds to the inverting input of the sample-and-hold error amplifier. The relatively high gain in the overall loop causes the voltage across R_{REF} resistor to be nearly equal to V_{IREF}, internally set to $1\,V$. Than, the design equation for R_{FB} results in (47).

$$R_{FB} = (V_{OUT} + V_D) \cdot \frac{N_{PS}}{I_{REF}}. \tag{47}$$

The average output current $I_{o,gate}$ corresponds, in first approximation, to the average current injected into the gate terminal of the MOSFET. In particular, the total gate

charge $Q_{G(tot)} = 10nC$ needs to be provided by the converter output f_S times per second, during turn-on transient, leading in first approximation to an average current of

$$I_{o,g} = Q_{G(tot)} \cdot f_s \simeq 30\,mA \tag{48}$$

Furthermore, the LT8301 IC has a maximum voltage rating at the "SW" pin of $65V$, by the way the manufacturer suggest not to overcame $V_{sw,max} = 50V$ on that pin during normal operation. This constrain reflects on the maximum flyback pulse voltage $V_F^{max} = V_{sw,max} - V_{IN} = 26\,V$.

Transformer turns ratio. The transformer turns ratio is calculated on the maximum voltage stress of the switch pin "SW" $V_{sw,max}$, occurring during the off phase. The equation (49) holds for the switch voltage stress

$$V_{sw,max} = V_{IN} + (V_{OUT} + V_D) \cdot N_{PS} \tag{49}$$

The transformer turns ration results in (50), assuming the diode forward voltage $V_D = 0.7\,V$. The closest value for the transformer turns ratio would be the unit, but it is preferable to keep extra margin on the switch voltage stress, lowering the turns ratio.

$$N_{PS} = \frac{V_F^{max}}{V_{OUT} + V_D} = 1.14 \quad \longrightarrow \quad N_{PS} = 0.5 \tag{50}$$

Back-calculating the nominal switch voltage stress from equation 49 leads to $V_{sw} \simeq 35\,V$ that fully matches the desired value.
Once the transformer turns ratio has defined, the feedback resistor can be calculated from (47):

$$R_{FB} = 110\,k\Omega \tag{51}$$

Transformer primary inductance. The control IC imposes some requirements on its minimum value:

- The secondary winding needs to conduct current for a minimum of $450\,ns$, that is the minimum settle and sample time of the internal ADC of the *LT8301*.

$$\begin{aligned} L_{PRI} &\geq \frac{t_{off,min} \cdot N_{PS} \cdot (V_{OUT} + V_D)}{I_{SW,min}} \\ &\geq 17\,\mu H \end{aligned} \tag{52}$$

  The minimum switch current limit is $I_{SW,min} = 290\,mA$.

- The controller IC has a minimum switch-on time of $170\,ns$, relate to the leading-edge blanking of the initial switch turn-on current spike. If the inductor current exceeds the desired current limit during that time, oscillation

Table 13: Parameters for the transformer design

Parameter	Symbol	Value
Frequency	f_s	$275\,kHz$
Turns ratio	N_{PS}	0.5
Primary voltage	V_{IN}	$24\,V$
Secondary 1 voltage	V_{out1}	$22\,V$
Secondary 2 voltage	V_{out2}	$22\,V^{(1)}$
Secondary 1 current	$I_{o,g1}$	$30\,mA$
Secondary 2 current	$I_{o,g2}$	$30\,mA^{(2)}$
Primary current	I_p	$120\,mA^{(3)}$
Primary inductance	L_{PRI}	$24\,\mu H$

(1) $V_{out1} = V_{out1} = V_{out}$.
(2) $I_{o,g1} = I_{o,g2} = I_{o,g}$.
(3) $I_p = 2 \cdot I_o / N_{PS}$.

may occur at the output as the current control loop will lose its ability to regulate.

$$\begin{aligned} L_{PRI} &\geq \frac{t_{on,min} \cdot V_{IN}}{I_{SW,min}} \\ &\geq 14\,\mu H \end{aligned} \tag{53}$$

The higher constraint is the one of equation (52) that defines the minimum inductance value. Then the primary inductance is set 40% higher than the minimum value and results in equation (54).

$$L_{PRI} = 1.4 \cdot L_{PRI,min} = 23.8\,\mu H \quad \longrightarrow \quad L_{PRI} = 24\,\mu H \tag{54}$$

Table 13 groups the specifications for the flyback transformer design.

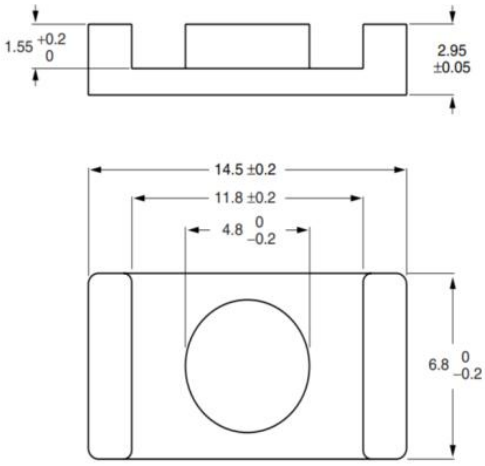
Transformer core selection. The core selection takes into account the core material, the core form and the core dimension. Typically ferrite cores are used for transformer in the range of few hundred kHz, since the transformer needs to be as small as possible the planar ER14 core is selected. Even if it is called a "transformer", the flyback magnetic is rather a mutual inductor that needs to store energy: an airgap is then expected in the core. The magnetic material 3F3 has selected, then Figure 35 shows the physical dimension of the core and the behavior of the magnetic material. The airgap has set to $150\,\mu m$, leading to an inductance factor of

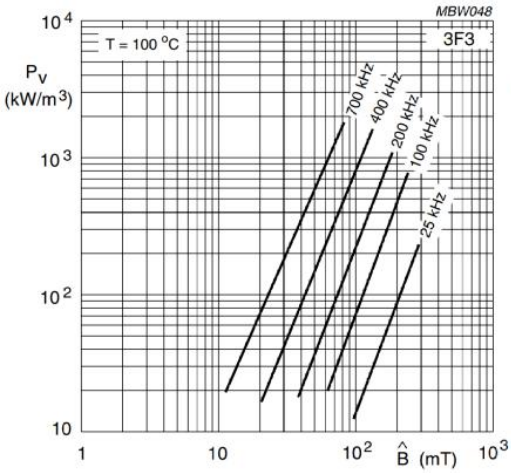
$$A_L = 160\,nH/turns^2. \tag{55}$$

CORE SETS

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
$\Sigma(l/A)$	core factor (C1)	1.08	mm^{-1}
V_e	effective volume	333	mm^3
l_e	effective length	19.0	mm
A_e	effective area	17.6	mm^2
A_{min}	minimum area	17.3	mm^2
m	mass of core half	≈ 0.9	g





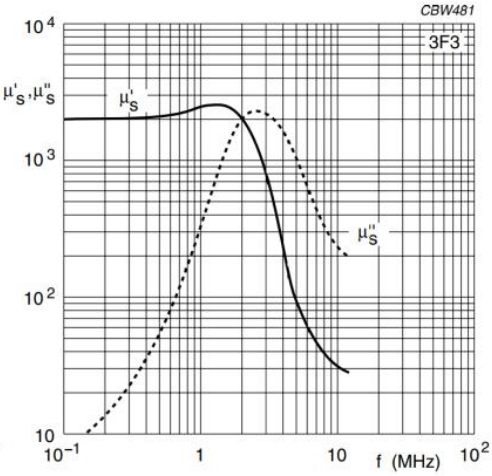


Figure 35: Core ER14 dimensions and magnetic material 3F3 characteristic

Primary and secondary windings design. The number of turns of the primary winding, T_p, results in equation (56). The number of turns of each secondary winding then results from the transformer turns ratio.

$$T_p = \sqrt{\frac{L_{PRI}}{A_L}} = 12 \tag{56}$$

$$T_s = \frac{T}{N_{PS}} = 24. \tag{57}$$

In the following, the wires sections are calculated over the average currents of the windings, rather than on the *rms* value. Moreover, the skin effect has neglected. To account for these simplifications, the wire is sized over a rather small current density $J_{trg} \simeq 2\,A/mm^2$. So that, for the secondary windings results:

$$Aw, s = \frac{I_{o,g}}{J_{trg}} = 0.015\,mm^2 \quad \longrightarrow \quad \phi_s = 0.15\,mm \tag{58}$$

and for the primary winding

$$Aw, p = \frac{I_p}{J_{trg}} = 0.06\,mm^2 \quad \longrightarrow \quad \phi_p = 0.25\,mm \tag{59}$$

A posteriori is checked that the ER14 core can host the windings. The core window area A_C results from the core parameters of Figure 35:

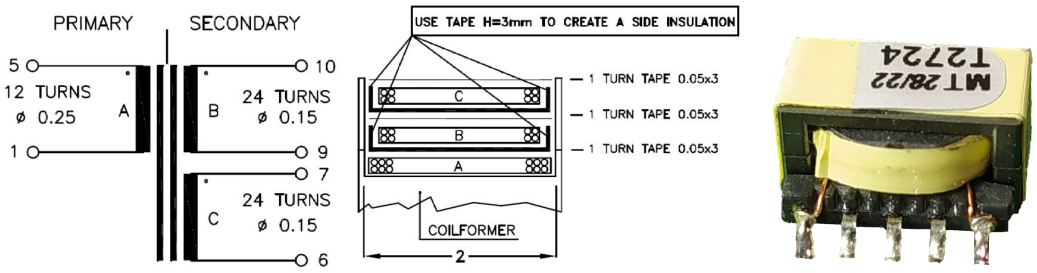
$$A_{c,min} = \frac{C - D3}{2} \cdot 2\,F = 10.85\,mm^2 \tag{60}$$

while the area occupied by the windings A_{cu} is

$$A_{cu} = 2 \cdot 0.15^2 \cdot T_s + 0.25^2 \cdot T_p = 1.83\,mm^2 \tag{61}$$

The core window area is larger than the copper area, them the ER14 core is validated. The difference between the two leaves enough space for the insulating tape between the 3 windings, and between the windings and the core. Figure 36 shows the final draw of the transformer, and the physical realization.

Clamping diode selection. The flyback topology exhibits high voltage spikes at the switching node, when the switch turns off. Then, the switching node must be clamped, to avoid dangerous voltage spikes to overcome the maximum voltage rating of the "SW" pin. The simplest clamp is the zener clamp, consisting in dissipating in a zener diode the energy associated to the voltage overshoot. The zener voltage is computed in order to make the clamping effective only for switching node voltage higher than $V_{sw,max} = 50\,V$. This is the maximum node voltage suggested by the LT8301 datasheet, lowering the clamp voltage causes more power to be dissipated



(a) (b)

Figure 36: Transformer mechanical drawing (a) and physical realization (b)

in the zener and less to be transferred to the output. The voltage of the clamping zener is calculated as follows

$$\begin{aligned} V_{zc} &= V_{sw,max} - V_{IN} - V_D \\ &\simeq 26\,V \end{aligned} \tag{62}$$

The fast TVS diode "SMAJ27A" has selected, it corresponds to the D_z component of Figure 34.

Rectifying diode selection. The rectifying diode on the secondary side are expected to exhibits fast recovery time and soft recovery behavior, not to stress the primary switch. The diode must sustain, at least, a voltage equal to:

$$V_R = \frac{V_{IN}}{N_{SP}} + V_{OUTH} = 70V \tag{63}$$

In terms of current, $1A$ rated diodes are extremely widespread, leading to an easy replacement if the diode part number would run out of stock. Diode "VS-1EFH02-M3" has finally selected, it has extremely optimized stored charge and low recovery current.

Voltage level translation. SiC MOSFETs typically have a low turn-on threshold voltage, between 3 volts to 5 volts. In case of a switching event, when the gate voltage is pulled down, the rising drain voltage transient could couple into the gate enough charge to increase the gate-source voltage beyond the turn-on threshold. To avoid such a scenario, SiC MOSFETs are driven with a negative gate-source voltage, in this way more charge should be injected into the gate-source capacitance to accidentally turn on the MOSFET.
The supply voltage V_{OUTH} of the voltage driver is then shifted down in respect to the source potential, by means of a zener diode. The zener voltage is $V_Z = 3.9V$ and the driving voltages of the mos become:

$$V_{GS,on} = V_{OUTH} - V_Z = 18.1V \quad \longrightarrow \quad V_{GS,off} = -V_Z = -3.9V \tag{64}$$

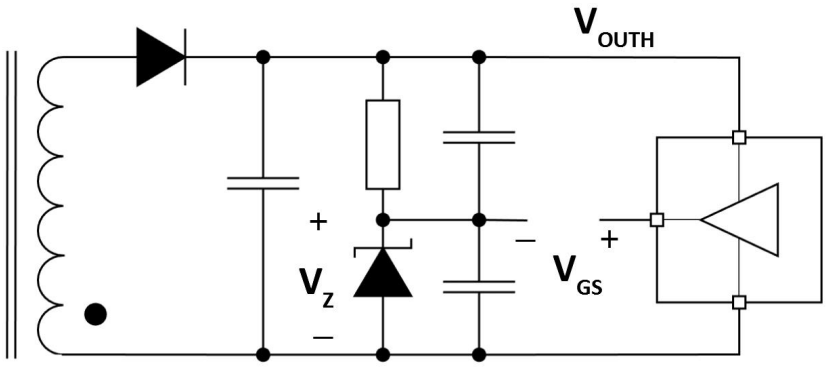


Figure 37: Voltage level shifting of the driving power supply

The connection is visible in figure 37, the same situations exactly repeats for the V_{OUTL} power rail. The zener polarization resistor R_{pol} is computed in (65) for a polarization current of $I_{pol} = 10\,mA$

$$R_{pol} = \frac{V_{OUTH} - V_Z}{I_{pol}} \simeq 1.8\,k\Omega \tag{65}$$

The polarization current I_{pol} overcomes the minimum output current $I_{O,min}$, required by the LT8301 controller (66). Then, no additional bleeder resistor is necessary.

$$I_{O,min} = \frac{L_{PRI} \cdot I_{SW,min}^2 \cdot f_{s,min}}{2 \cdot V_{OUTH}} \simeq 2\,mA \tag{66}$$

Gate driver. The logic signals for the gates driving are generated by the controller IC that manage the input boost stage, this will be discussed in the next section 3.4. From this signals, the gate driver chips need to properly drive the gate-source voltage of the MOSFETs that, indeed, has floating level if referred to ground. For this reason an electric isolation is necessary between the logic gate signals and the effective gate driving voltage.To this purpose, the isolated gate driver *UCC21520* is selected. This component is specifically designed to drive synchronous converters and provides two separated drivers, isolated from the input and isolated each other. The internal structure is visible in Figure 38. A total of four of this drivers are needed to control the eight switch of the input boost stage. Each output of the driver is connected to an isolated power supply, V_{OUTH} or V_{OUTL}, referred to the source of the device to be driven.

The total driving circuitry for the input boost is grouped in a board that connects the power board and logic board, the realization is presented in the Figure 39.

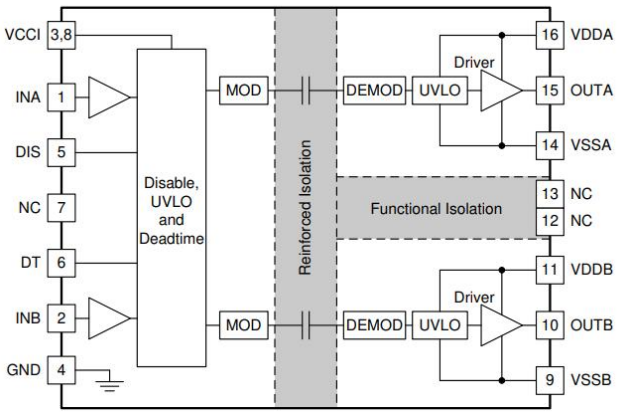
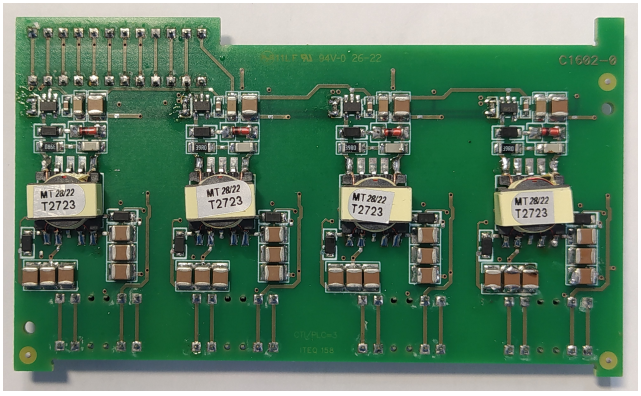
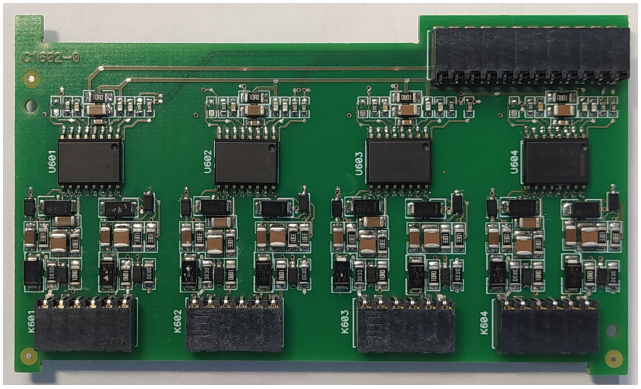


Figure 38: Internal configuration of the UCC21520 gate driver chip



(a)



(b)

Figure 39: Driving board for the input stage

3.2 Output stage

The output stage of the converter is an interleaved boost stage, the structure is similar to the boost of the input stage. Unlike the input boost, the output stage is characterized by a reduced input current but an increased output voltage. The input current of the output stage reaches up to 60 A and the output voltages reaches up to 800 V. In this context of high voltage and relatively reduced currents, an asynchronous boost configuration don't loose too much efficiency in respect to a synchronous one. On the other side, the high-voltage diodes are significantly cheaper than high-voltage MOSFETs, and the elimination of the isolated-driving of the top MOSFETs causes further decrease in the total cost of the stage.
Since the lost of efficiency with an asynchronous configuration is expected to be reduced in this context, but the cost saving is significant, the output stage has chosen with an asynchronous structure, as depicted in the following Figure 44. Interleaved operation is chosen also for this stage, since the advantages over paralleling are relevant.

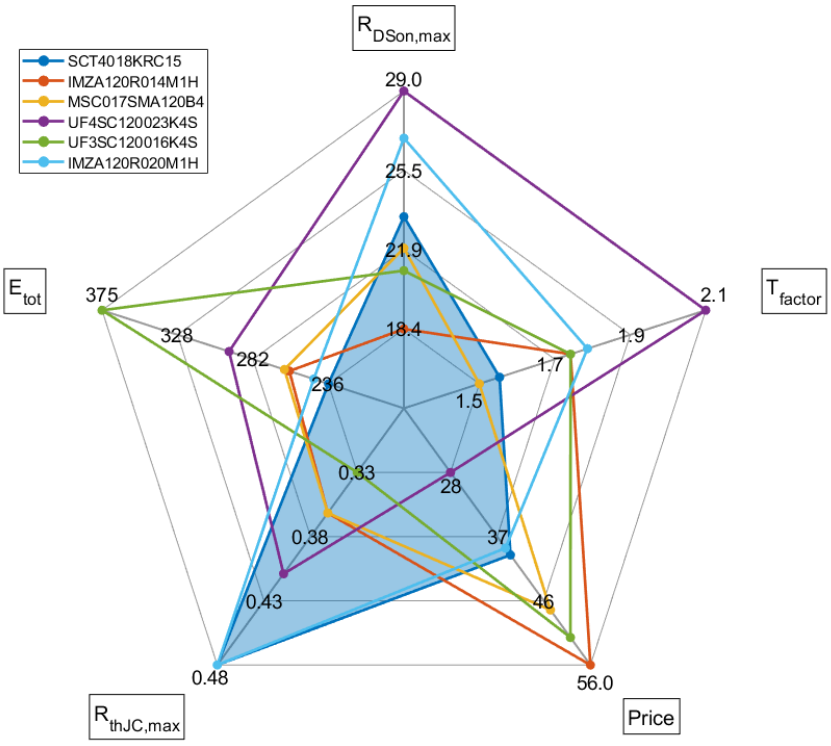


Figure 40: Selection diagram for the MOSFET part-number of the output boost stage

3.2.1 MOSFET selection

The output voltage of the stage reaches up to $800\,V$, this voltage corresponds to the V_{ds} voltage of the MOSFETs during the off-state. Then, the MOSFET must be selected in the $1200\,V$ range. For this voltage and current SiC MOSFETs are the preferred constructive technology. The parameters evaluated for the selection of the part number are the same considered in the input stage, listed in Table 10. The comparison between different candidates are made visible in the spider plot of the Figure 40. In this plot the component exhibiting the lower inner area is the most suitable. Two part-numbers are of interest, the SCT4018KRC15 (blue trace) has , and the MSC017SMA120B4 (Yellow trace). The SCT4018KRC15 MOSFET is finally preferred as a trade-off between cost and performances.

3.2.2 Diode selection

The freewilling diodes of the output stage must sustain a reverse voltage equal to the maximum output voltage $V_o = 800\,V$. As the MOSFET, also the diode is chosen in the $1200\,V$ range. The SiC power diodes are the most suited technology for this application, in terms of reverse voltage, forward voltage and switching frequency[12]. The selection plot of Figure 41 is build up on the parameters evaluated in the selection of the diode. The parameters are listed in the Table 14, then the selected part-number for the freewilling diode results in IDWD40G120C5.

Table 14: Description of the parameters considered for the selection of the MOSFET part-number of the output stage

Parameter	$[unit]$	**Description**
Price	€	It is the average commercial price for one piece.
R_{thJC}	K/W	Thermal resistance from junction to case. The maximum value (worst case) is considered.
V_F	V	The forward voltage with a current of $15\,A$ and a junction temperature of $25°C$.
Q_C	nC	Total charge of the junction capacitance.

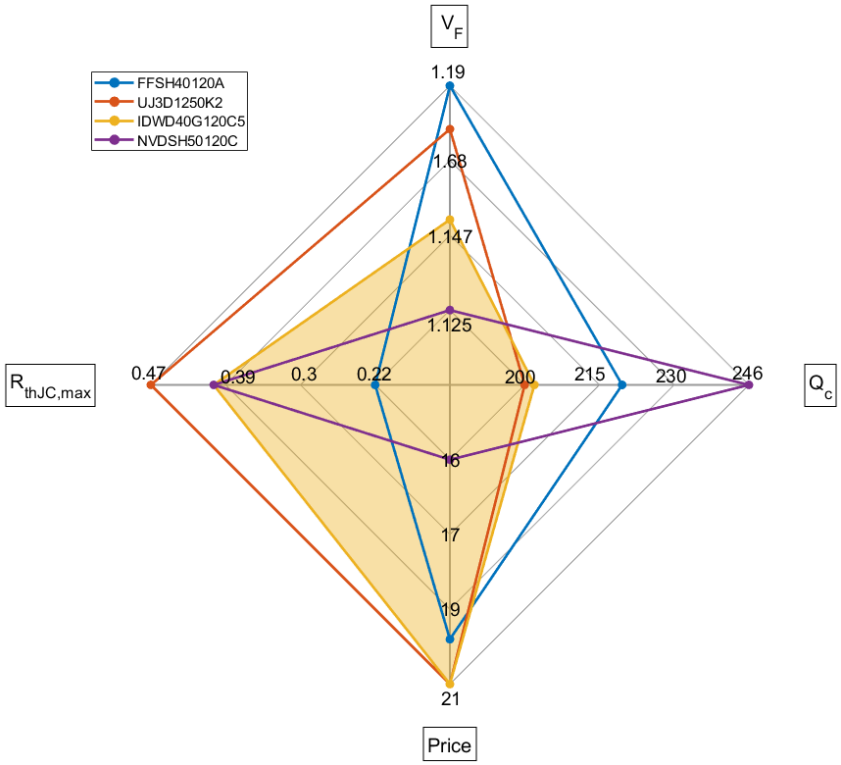


Figure 41: Selection diagram for the diode part-number of the output boost stage

3.2.3 Number of phases

The selection of the number of phases follows the procedure described in the previous section 3.1.2 for the input boost. The higher the number of phases, the lower the losses in each MOSFET, but the higher the price and the complexity. The number of phases is chosen as the minimum value that makes the MOSFET working under a junction critical temperature $T_{j,crit} = 125°C$. The average thermal model of the MOSFET is developed, the thermal dependence of the drain resistance with the junction temperature is taken into account. The plot of figure 42 relates the junction temperature and the drain current: the minimum number of phases is four, then this is set as the number of phases of the output stage.

3.2.4 Inductor design

The total current entering the output stage split between the four inductors of its phases. The nominal average current in every inductor results:

$$I_{L2,nom} = \frac{P_{nom}}{4 \cdot V_{bus,nom}} = 15\,A \tag{67}$$

The inductance value is computed to obtain a worst-case inductor ripple of 40% the nominal inductor current.

$$\Delta I_{L2} = 40\% \cdot I_{L2,nom} = 6\,A \tag{68}$$

From equation 24 can be derived the design equation for the inductor value. In this case, can't be satisfied the condition $M = 2$ that maximize the ripple, since the bus voltage can't rise above 300 $,V$. In this scenario the current ripple is maximum for the maximum output voltage $V_{o,max} = 800\,V$ and the maximum bus voltage $V_{bus,max} = 300\,V$. The inductance value results

$$L_2 = \frac{V_{bus,max}}{f_s\,\Delta I_{L2}}\left(1 - \frac{V_{bus,max}}{V_{o,max}}\right) = 311\,\mu H \tag{69}$$

The core selection relies on the parameter $LI^2 = 100\,mHA^2$, from the selection graph of Figure 27 can be found that the suggested core to be the 77868 core. By the way, this core has a diameter too large to fit into the converter physical dimension, so the 77439 core is selected instead. With a smaller core, higher decrease in the inductance value at nominal load is expected.
The compute of the number of turns, the evaluation of the inductance decrease at nominal load and the loss compute resemble exactly the process carried out in section 3.1.3 for the input boost stage. For this reason, the procedure is omitted and the results are presented out of the Matlab script outputs of figure 43.

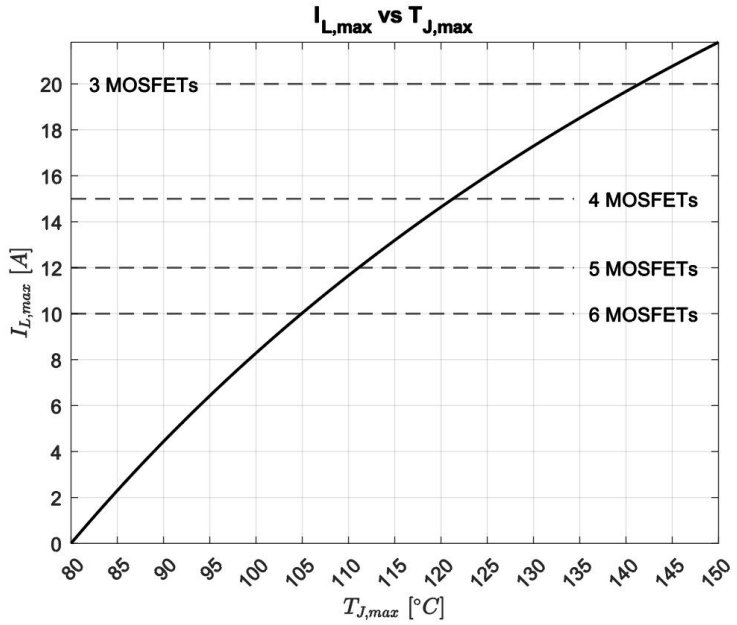


Figure 42: Phase current over maximum junction temperature, for one phase MOSFET of the output stage

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**************  CORE SELECTION  **************

 Vo              = 400.00 V
 Vi              = 250.00 V
 Lnom            = 310.95 uH
 LI^2            = 84.73 mH A^2

CORE Kuul Mu     = 77439
J [A/mmqq]       = 5

******************  RESULTS  ****************

 n° turns        = 48.00 turns
 L @ full load   = 151.52 uH
 DelIL load      = 6.60 A
 IL_pk load      = 18.30 A
 Bmax            = 0.29 T

 Aw              = 3.02 mmq
 rl              = 17.90 mOhm
 Pcu             = 4.09 W
 Pcore           = 3.24 W
 Ptot            = 7.33 W

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```

(a)

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>> TOROID_DESIGN_TOOL

**************  CORE SELECTION  **************

 Vo              = 800.00 V
 Vi              = 300.00 V
 Lnom            = 310.95 uH
 LI^2            = 100.91 mH A^2

CORE Kuul Mu     = 77439
J [A/mmqq]       = 5

******************  RESULTS  ****************

 n° turns        = 48.00 turns
 L @ full load   = 134.85 uH
 DelIL load      = 14.83 A
 IL_pk load      = 22.42 A
 Bmax            = 0.32 T

 Aw              = 3.12 mmq
 rl              = 17.35 mOhm
 Pcu             = 4.22 W
 Pcore           = 12.83 W
 Ptot            = 17.05 W

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(b)

Figure 43: Inductor design script for the output boost with $V_o = 800\,V$ and $V_{bus} = 300\,V$ (a). The design is then evaluated for $V_o = 400\,V$ and $V_{bus} = 250\,V$ (b)

3.2.5 Output capacitor design

The output capacitance is designed to obtain a residual ripple on the output voltage of $\Delta V_o = 3\,V$ under the condition of nominal power. No interleaving effect is considered, as the worst case scenario. From the ripple voltage equation (43) of the boost converter , the following equation can be derived for the output capacitance:

$$C_o = \frac{1 - \frac{V_{bus,min}}{V_o^*}}{V_o^*} \frac{P_{nom}}{f_s \Delta V_o} = 50\,\mu F \tag{70}$$

The required capacitance is maximum for the minimum bus voltage $V_{bus,min}$ and an output voltage of $V_o^* = 500\,V$. The nominal capacitance is set to $C_o = 47\mu H$, and it is obtained through two couples of electrolytic capacitors ($47\mu F$,$500\,V$) connected in parallel two by two, and then placed in series to sustain the maximum output voltage of $800\,V$. The total schematic of the output stage is finally depicted in the Figure 44.

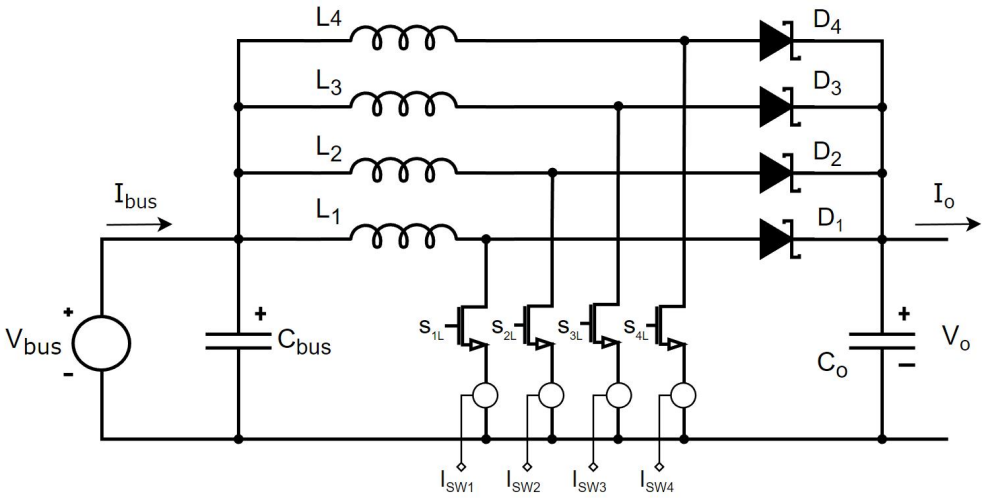


Figure 44: Schematic of the output boost stage

3.3 Buck stage

The buck-stage have been introduced to manage the condition of short circuit at the output. Therefore, during the normal operation, its behavior resembles a closed switch. Of course, since the component are not ideal, some loss occurs in the stage due to the series resistance of the MOSFET channel. To reduce the power dissipation, more than one MOSFET can be placed in parallel. The maximum loss in efficiency at nominal power, due to the series MOSFET insertion, has set to $\eta_{loss} = 0.25\%$ at full load $P_{in,max} = 15\,kW$. This corresponds to a dissipated power of

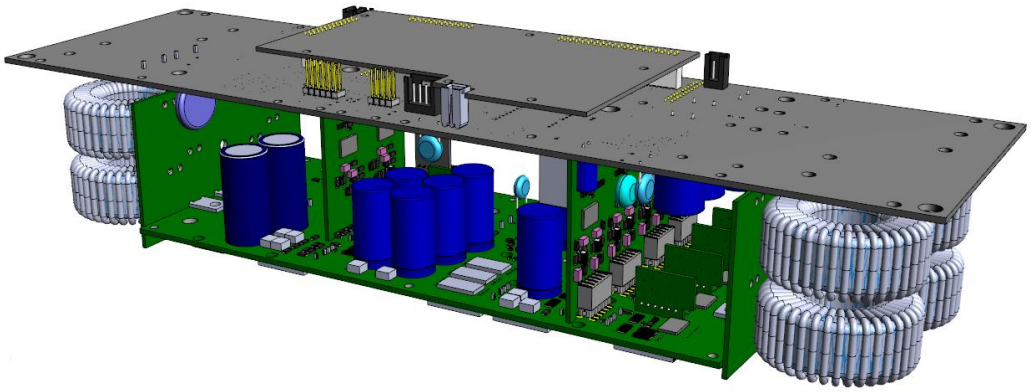
$$P_{series} = P_{in} \cdot \eta_{loss} = 37.5\,W. \tag{71}$$

The worst case condition for the power losses on the series MOSFET is when its current is maximum, i.e. when the bus voltage is minimum, $V_{bu} = 250\,V$. The required series resistance RSD^{eq}_{ON} results

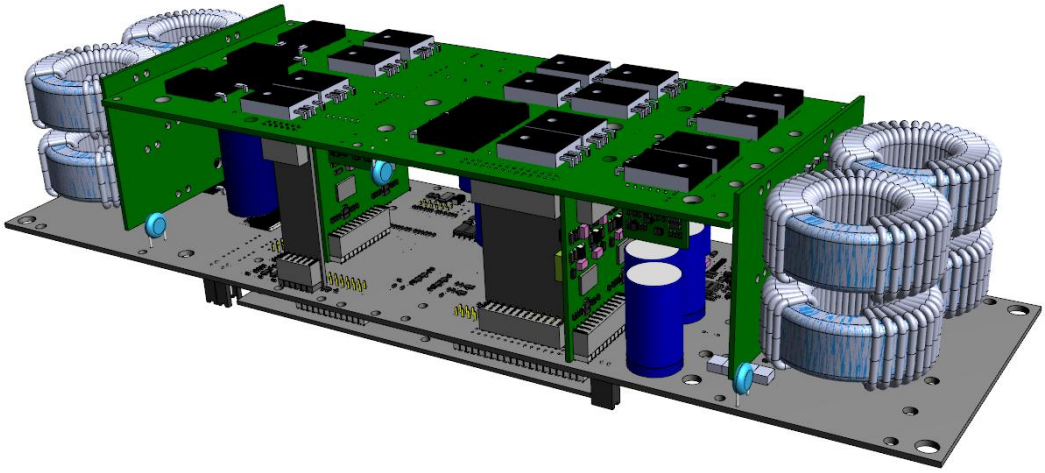
$$\begin{aligned} R^{eq}_{ds,on} &= P_{series} \cdot \left(\frac{V_{bus,min}}{P_{in,max}} \right)^2 \\ &= 10.4\,m\Omega \end{aligned} \tag{72}$$

The same part-number of the input boost is used for the MOSFET, so that two of them are placed in parallel to obtain an equivalent on-state resistance of $R^{eq}_{ds,on} = 9.5\,m\Omega$. The loss in efficiency due to the buck stage ranges from $\eta = 0.23\%$ to $\eta = 0.16\%$ at nominal power, depending on the bus voltage.
Even if this is a protecting stage, and not a proper buck stage, the diode of the stage need to satisfy the requests of the diode of a buck stage in case it must intervene. A fast response is necessary. Of course, the diode must sustain the reverse voltage V_{bus}, so it is chosen in the $400V$ range. The part-number VS-60EPU04-N3 has selected, it is an ultra-fast soft-recovery diode with a nominal current rating of $60\,A$ and an impulsive current rating of $600\,A$ for $10\,ms$.

The buck stage design completes the hardware design of the converter. The design of the PCBs have been carried out by the designer of the company and it is not part of this thesis. The resulting prototype is shown in the 3D rendering of figure 45. The converter consists of the power board, hosting the power devices, and the logic board, implementing the communication and control section as well as hosting the microcontroller board. The logic and power boards are connected by two PCBs implementing the driving section for the first and the second stage. The inductors are placed in two separated PCBs since they will be resin-embedded in a metal housing, thermally connected to the dissipating plate.



(a)



(b)

Figure 45: Rendering 3D of the prototype, the logic and power board are visible, as well as the microcontroller PCB.

3.4 Compensation and control

This converter find application in the fuel cell vehicles as interface between the FC and the vehicle battery. As described in section 1, the converter is informed by the FCC regarding the actual operating point: how much current can be extracted from the FC $I_{in,max}$ and the maximum power that can be injected into the battery $P_{o,max}$.

Control strategy. From the parameters listed in Table 15 the microcontroller set the reference values for the feedback loops. Note that the external parameters $I_{in,max}$ and $P_{o,max}$ relates to the input and output port of the converter, respectively.

External set parameters	
$I_{in,max}$	The maximum average input current of the converter
$P_{o,max}$	The maximum charging power of the battery
Measured parameters	
V_{in}	Actual input voltage of the converter
V_o	Actual output (battery) voltage

Table 15: Decision parameters used by the converter microcontroller to set the output current reference.

Based on the measured parameters V_{in} and V_o, the microcontroller detects if the limit to the output power is dictated by the FC generation ($I_{in,max}V_{in} < P_{o,max}$) or by the battery charging limitation ($I_{in,max}V_{in} \geq P_{o,max}$). In the first case, the input current should be controlled, in the second case the output current should be controlled instead. This requires two control loops, one intended to regulate the input current and a second loop to regulate the output current.
To keep the sense and control simpler, only the output current is directly regulated in this design. The input current regulation is accomplished by regulating the output current and considering an estimated efficiency η, based on the actual operating point. The efficiency is experimentally measured in the following section 5.2, then it is used in the computation for the output current reference, as depicted in the flow chart of figure 46.

Controller IC. The converter is composed of eight distinct boost phases, four for the first stage and four for the second. Every phase employs an analog controller IC to manage the operation of that phase: the controller "LM5026" has selected. It is a peak-current-mode (PCM) controller intended for active clamp converters, but it is well known to achieve high efficiency if used in synchronous converters as the boost phases of the input stage. In every phase of the input stage, the inductor current loop of the PCM structure regulates the peak current of the phase inductor

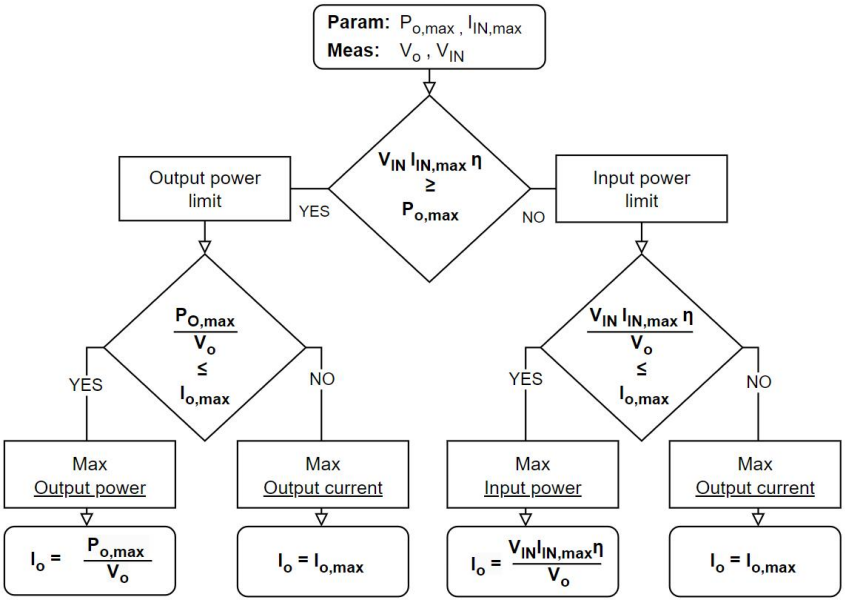


Figure 46: Flow chart for the control of the output current, the efficiency η is estimated according to the operating point

to the reference value set by the external feedback loop (for example the output voltage feedback loop). If this reference is made common to the four phases of the input boost, then the input current is equally split between the four phases. The same "LM5026" controller is used also in the output stage, for simplicity.
It is well known necessity of a compensation ramp in the PCM structure, for duty cycles greater than half. The higher is the slope of the compensation ramp, the higher is the value of the maximum duty cycle that can be reached without the presence of sub-harmonic oscillation. On the contrary, the higher the compensation slope the lower the bandwidth of the inner current loop.

The internal structure of the controller IC integrates the selection of the compensation slope by means of one resistor in series to the current sense path. The structure of the current sense and the compensation slope setting is depicted in figure 47. It is simple and cheaper to sense the switch current instead of the inductor current, they coincide during the t_{on} time. The switch current is sensed through a *CST2010-200* current transformer, with ratio $N = 200$.

The sense resistor R_s is selected to reach the threshold voltage $V_{C,th} = 0.5V$ for a switching current of $I_{sw,th1} = 30A$ for the first stage, and $I_{sw,th2} = 25A$ for the second stage, the contribution of the compensation slope is considered. The system

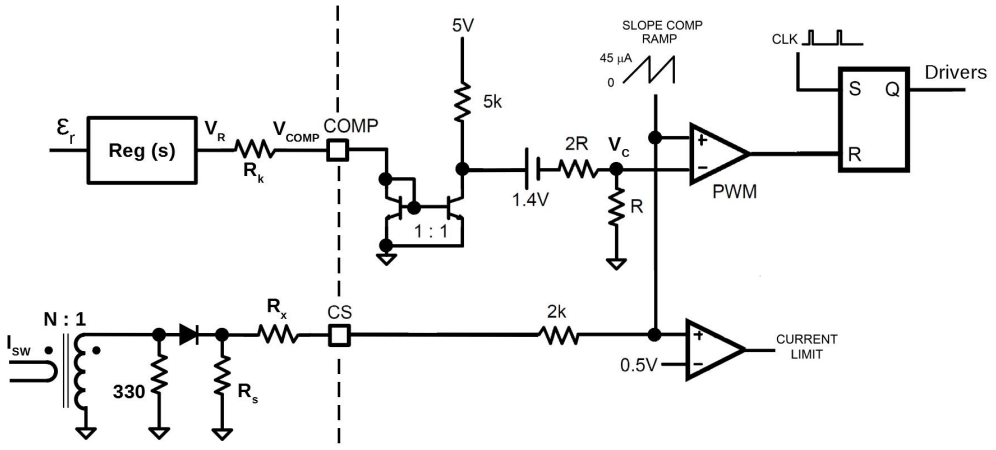


Figure 47: Switch current sense circuit (lower part) and internal circuit of *LM5026* for the feedback loop (upper part)

of equation is presented in equation (73):

$$\begin{cases} S_a = \dfrac{R_i V_{o,max}}{2\,L}\left(2 - \dfrac{1}{d_{maax}}\right) = R_i \cdot A \\ R_s = \left(V_{C,th} - (R_x - 2k)45\mu\right)\dfrac{N}{I_{sw,th}} \\ R_x \simeq \dfrac{S_a}{I_{sw,th} f_s} - sk. \end{cases} \tag{73}$$

The sense resistors R_s and the compensation resistor R_x result as follows

$$R_s = \begin{cases} R_{s1} = 2.05\,\Omega & 1^{st} stage \\ R_{s2} = 2.74\,\Omega & 2^{nd} stage \end{cases} \tag{74}$$

$$R_x = \begin{cases} R_{x1} = 2.74\,k\Omega & 1^{st} stage \\ R_{x2} = 1.47\,k\Omega & 2^{nd} stage \end{cases} \tag{75}$$

For the following evaluation, it is useful to compute the equivalent sensing resistor $R_i = (R_s)/N$. This completes the design of the current loop.

$$R_i = \begin{cases} R_{i1} = 10.25\,m\Omega & 1^{st} stage \\ R_{i2} = 13.7\,m\Omega & 2^{nd} stage \end{cases} \tag{76}$$

From the point of view of the external loop, the modulating signal V_c sets the reference value for the inner current-loop. The modulating voltage V_c comes from the output of the regulator, after some conversion internally performed by the LM5026.

The path of the modulating signal is shown in the upper part of the Figure 47, it leads to the voltage gain G_{ctrl}:

$$G_{ctrl} \triangleq \frac{\hat{v}_C}{\hat{v}_R} = -5k\Omega \cdot \frac{R}{R+2R} \cdot \frac{1}{R_K} = -139\ mV/V \tag{77}$$

The resistor R_K is selected to bias the output of the regulator at a voltage of $V_R = 5.7\,V$ when the control voltage V_C is set to the threshold value of $0.5\,V$:

$$R_k = 5k \cdot \frac{V_R - 0.7V}{5V - V_{c,th} \cdot \frac{3R}{R} - 1.4V} \simeq 12\,k\Omega \tag{78}$$

For a peak-current-mode boost converter, the duty cycle-to-output voltage transfer function $G_{vd}(s)$ is:

$$G_{vd}(s) = V_{in}M^2 \cdot \frac{1 - \dfrac{s}{\omega_{zv}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \quad , \quad \omega_{zv} = \frac{R_{load}}{M^2 L} \tag{79}$$

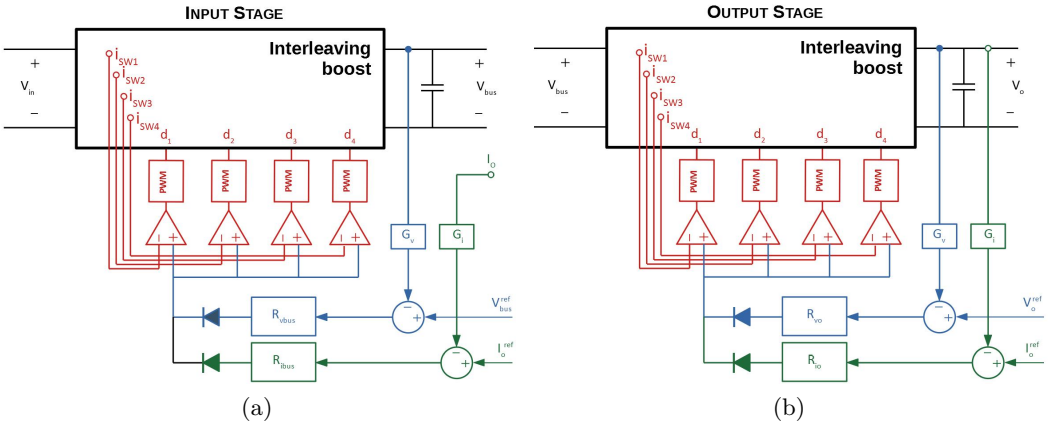
while the duty-cycle to inductor-current is expressed by the transfer function $G_{id}(s)$.

$$G_{id}(s) = \frac{2V_o M^2}{R_{load}} \cdot \frac{1 + \dfrac{s}{\omega_{zi}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \quad , \quad \omega_{zi} = \frac{2}{R_{load}C} \tag{80}$$

$$\omega_o = \frac{1}{M}\sqrt{\frac{1}{LC}} \quad , \quad Q = \frac{R_{load}}{M}\sqrt{\frac{C}{L}}$$

External control loops. The converter is a cascade of two stages, they can work simultaneously or, to optimize the efficiency, just the first boost or just the second boost can operate. Than, every stage must be able to regulate its output voltage and the total output current: (V_{bus}, I_o) for the first stage, and (V_o, I_o) for the second. The control loops of the two stages are presented in the Figure 48. Can be noticed that two external loops (voltage loop in blue and current loop in green) act on the same reference voltage for the inner current regulation loop. By the way, the diode decoupled connection ensures that only the dominant loop (e.g. higher control voltage V_R) sets the current reference. Which loop is dominant is imposed by the microcontroller by means of properly setting the reference values for the loops.

Control scenarios. Three different control scenarios may occur, depending on the operation mode, as shown in the Figure 49. The purpose of the loops may vary based on the operating mode:



(a) (b)

Figure 48: Control loops for the input stage (a) and for the output stage (b)

- $\boldsymbol{V_{bus}}$**-loop**: the firs purpose is to regulate the bus voltage when both stages are operating, Figure 49a. The second purpose is to set the output voltage when only the first stage is operation, and no battery is connected (i.e. the battery is not imposing the output voltage).
- $\boldsymbol{V_o}$**-loop**: sets the output voltage when only the first stage is operation, and no battery is connected (i.e. the battery is not imposing the output voltage).
- $\boldsymbol{I_o}$**-loop 1**$^{\boldsymbol{st}}$ **stage**: sets the output current when only the first stage is operating and the battery is connected to the output, Figure 49b.
- $\boldsymbol{I_o}$**-loop 2**$^{\boldsymbol{nd}}$ **stage**: sets the output current when only the second stage is operating and the battery is connected to the output, Figure 49c.

$\boldsymbol{V_{bus}}$**-loop**. The regulation loop of the bus voltage relies on the block diagram of Figure 50a. The bandwidth of the inner current loop is much higher than the bandwidth of the bus voltage loop, than the current loop is assumed ideal ($\hat{i}_L \simeq \hat{i}_c$) during the voltage loop design. The uncompensated loop gain results in equation (81).

$$G_u \triangleq \frac{\hat{v}_{bus}}{\hat{v}_R} = K_{DC} \cdot \frac{\left(1+\frac{s}{w_z}\right)\left(1-\frac{s}{w_{rhp}}\right)}{\left(1+\frac{s}{w_p}\right)} \cdot f_h(s) \tag{81}$$

the term $f_h(s)$ accounts for the high frequency behavior of the converter, and it is neglected in this analysis. The dc gain of the converter is given by:

$$K_{DC} = \frac{G_{ctrl} V_o V_i}{2 R_{i1} P_i} \tag{82}$$

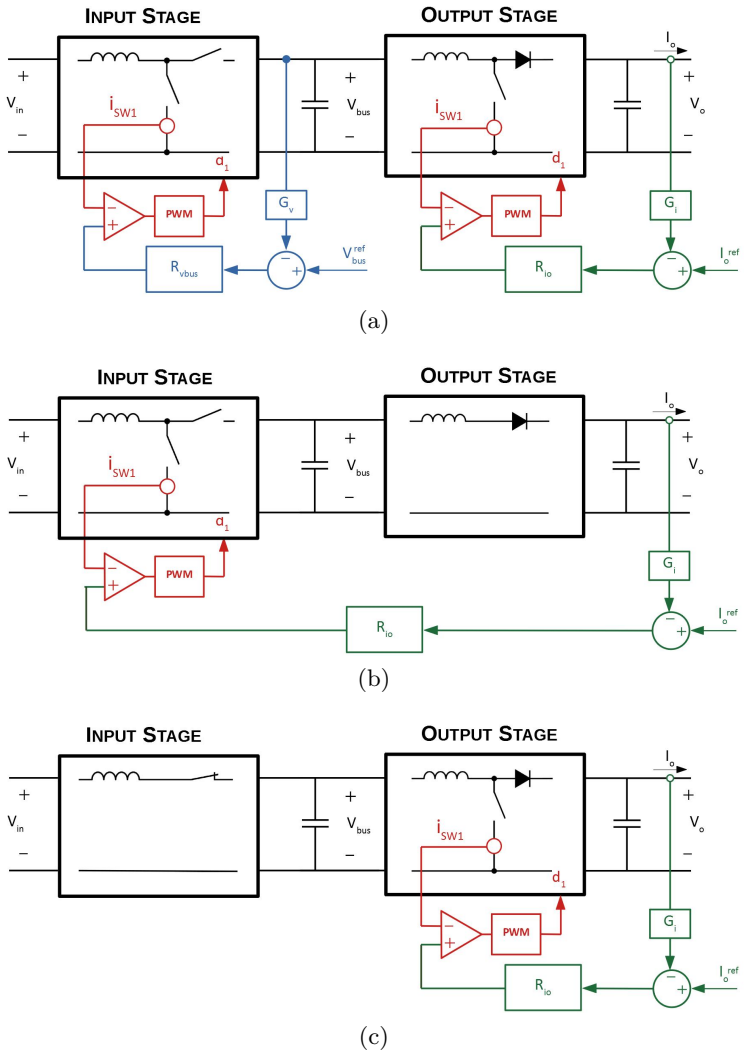
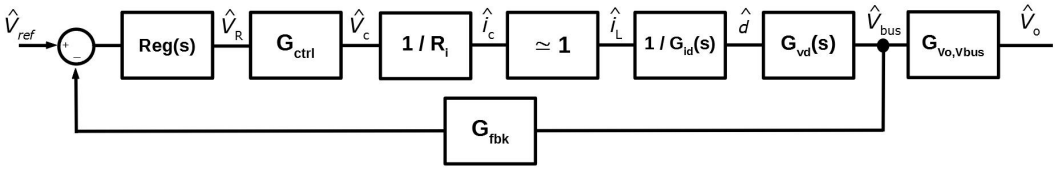
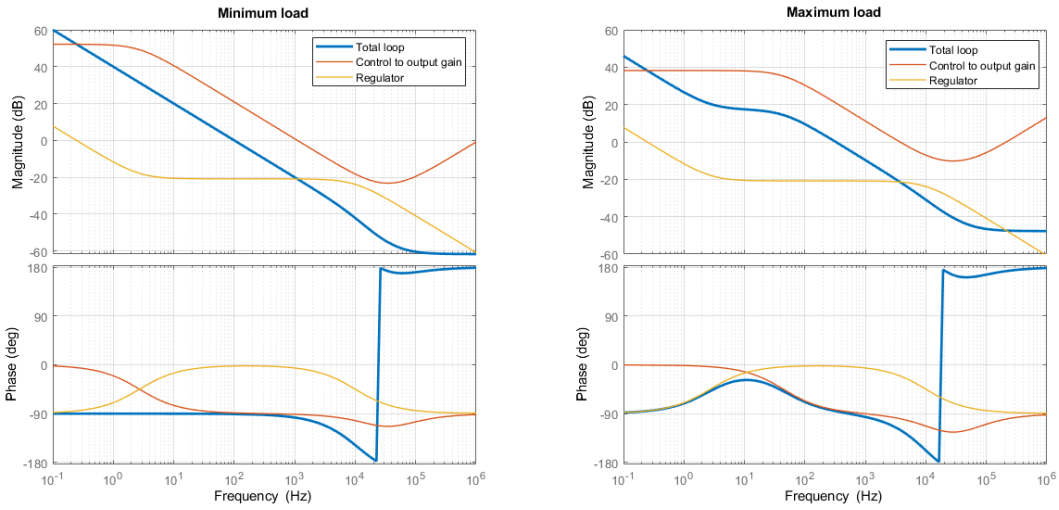


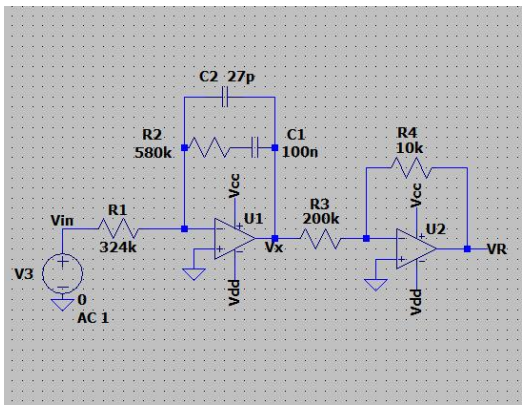
Figure 49: Control loops for different modes of operation, with battery connected to the output: both stages are operating (a), only the fists stage is operating (b) and only the second stage is operating (c).



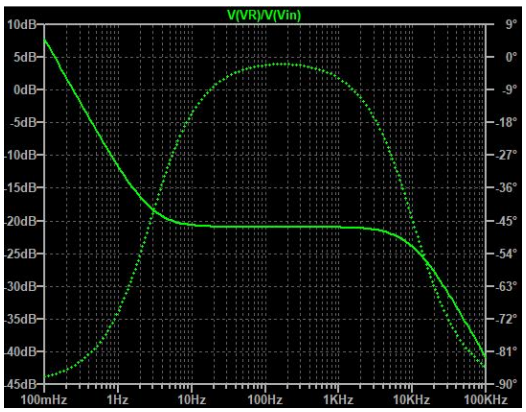
(a)



(b)



(c)



(d)

Figure 50: Block diagram of the V_{bus}-loop (a), bode plots of the uncompensated-loop-gain, regulator and compensated-loop-gain (b), regulator circuit and response (c)

The dominant pole is located at

$$w_p = \frac{2}{C \cdot R_{load}} = \frac{2P_i}{C_o V_o^2} \tag{83}$$

and the RHP zero is located at

$$w_{rhp} = \frac{R_{load} D'^2}{L_1} = \frac{V_i^2}{P_i L_1} \tag{84}$$

In addition, the ESR capacitor zero[13] can be considered. Can be noticed that its frequency is much higher than the regulator bandwidth, so its effect on the loop is strongly reduced.

$$w_z = \frac{1}{C_{bus} \cdot ESR} = 333k\, rad/s \tag{85}$$

The DC gain, as well as the pole and RHP zero positions depend on the operation point of the converter: the worst case is found for the maximum bus voltage $V_{bus} = 300V$ and the minimum input voltage $Vin = 46V$.

$$\begin{aligned} K_{DC} &= 52.2\, dB \\ \omega_p &= 17\, rad/s \\ \omega_{rhp} &= 144k\, rad/s \end{aligned} \tag{86}$$

In the left part of the Figure 50b is shown the bode plot of the uncompensated-loop-gain for an output power of $230\, W$, that corresponds to the CCM power threshold if the converter would be asynchronous.
The regulator of Figure 50c is designed to hit a crossover frequency $w_c = 2\pi\, 100\, rad/s$, the regulator zero ω_{zr} and pole ω_{pr} are placed at:

- The zero of the regulator is place coincident with the dominant pole of the uncompensated-loop-gain , so that $\omega_{zr} = w_p$
- The pole of the regulator is placed at $\omega_{pr} = \omega \cdot 100$

The regulator capacitor C_1 is set to $100\, nF$, than the other components of the regulator are calculated in equations (87) and the values are presented in the regulator schematic of Figure 50c.

$$\begin{aligned} R_2 &= \frac{1}{C_1 \omega_{zr}} \\ R_1 &= R_2 K_{DC} \frac{\omega_p}{\omega_c} \\ C_3 &= \frac{1}{R_1 \omega_{pr}} \end{aligned} \tag{87}$$

The closed-loop-gain results in the blue trace of Figure 50b. The phase margin is $pm = 89°$ at the crossing frequency $\omega_C = 2\pi 100\, rad/s$. The closed loop gain is then

evaluated for the full-power condition, and it is presented in blue trace of the right plot. Can be seen that the crossover frequency of the closed loop is increased up to $323\,Hz$, the phase margin in this case results in $pm = 94°$. The regulator design is confirmed.

V_o-loop The uncompensated-loop-gain for the output voltage regulation has the same form of the uncompensated-loop-gain of the bus voltage regulation, equation (81). Of course, different operating conditions and different passive components values occurs for the V_o loop gain, than the DC gain, the pole and the RHP zero result in equation (88) for $V_{bus} = 250V$ and $V_o = 800V$.

$$\begin{aligned} K_{DC} &= 62.6\,dB \\ \omega_p &= 51.6\,rad/s \end{aligned} \tag{88}$$

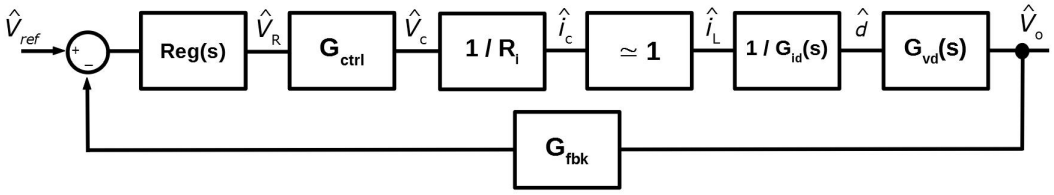
The closed-loop-gain is presented in the blue trace of Figure 51b. The phase margin is $pm = 89°$ at the crossing frequency $\omega_C = 2\pi 100\,rad/s$. The closed loop gain is then evaluated for the full-power condition, and it is presented in blue trace of the right plot. Can be seen that the crossover frequency of the closed loop is increased up to $92.5\,Hz$, the phase margin in this case results in $pm = 107°$. The regulator design is confirmed.

I_o-loop 1^{st} stage This control loop comes into play if the battery is connected to the output of the converter, and just the first stage is operating, the condition is depicted in Figure 49b. The output current is sensed through the hall-sensor ACS772LCB-100U, that exhibits a sensitivity of $R_{io} = 40\,m\Omega$. The equivalent series resistance of the battery is assumed $R_{bat} = 100\,m\Omega$, then the control of the output current $\hat{i}_o$ is obtained by controlling the output voltage $\hat{v}_o$ across the battery resistance. The block diagram of the output-current feedback loop is presented in the Figure 52a, the inner current loop is assumed to be ideal.
The uncompensated-loop-gain composes of the voltage-over-control transfer function, equation (81), with three additional terms:

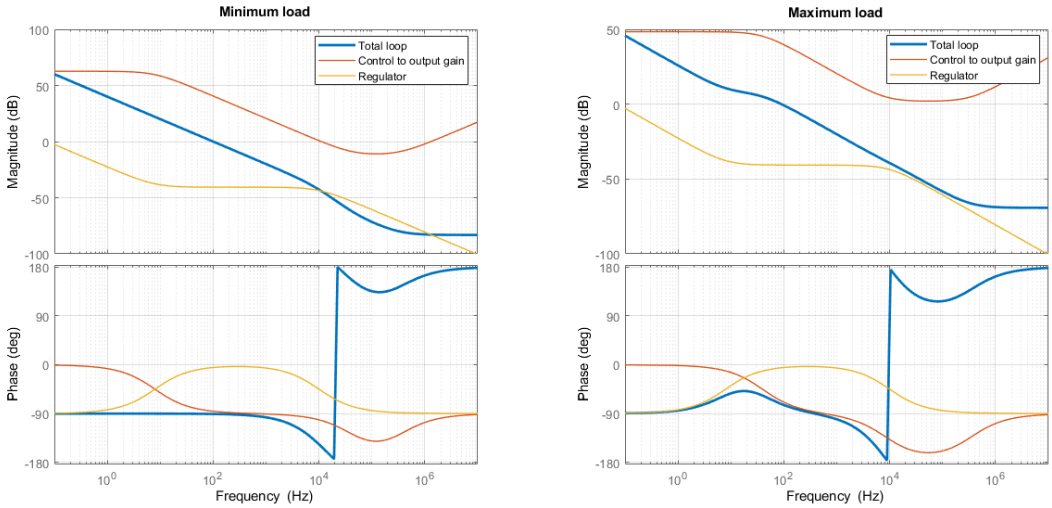
- The low-pass filter cell, introduced by the second stage $G_{Vo,Vbus}$
- The relation between output voltage and output current $1/R_{bat}$
- The sensitivity of the output current sensor R_{io}

The uncompensated-loop-gain results in equation (89):

$$G_u \triangleq \frac{\hat{i}_o}{\hat{v}_R} = K_{DC} \cdot \frac{\left(1 + \frac{s}{w_z}\right)\left(1 - \frac{s}{w_{rhp}}\right)}{\left(1 + \frac{s}{w_p}\right)} \cdot \frac{1}{1 + \frac{s^2}{\omega_{lp}^2}} \tag{89}$$



(a)



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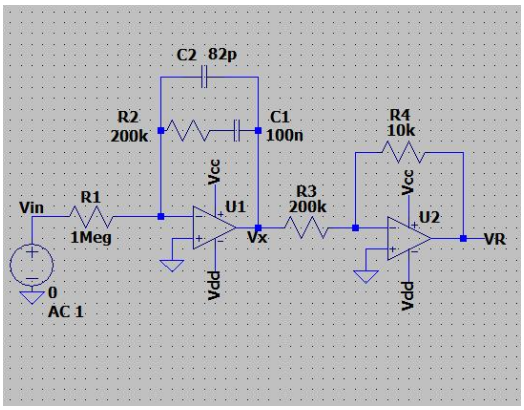

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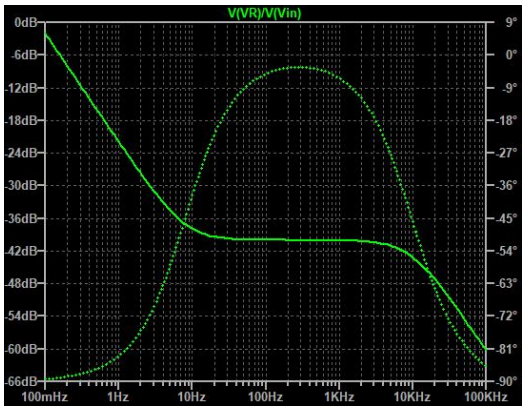


(d)

Figure 51: Block diagram of the V_o-loop (a), bode plots of the uncompensated-loop-gain, regulator and compensated-loop-gain (b), regulator circuit and response (c)

the dominant pole and the RHP zero are unchanged in respect to the V_bus control loop, but an additional second order pole appears at ω_{lp}. The closed-loop bandwidth ω_C must be much lower than ω_{lp}, to keep margin from the phase decrease caused by the complex poles.

$$\begin{aligned} \omega_p &= 17\,rad/s \\ \omega_{rhp} &= 144k\,rad/s \end{aligned} \tag{90}$$

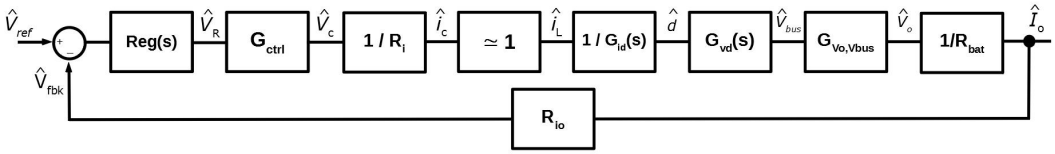
$$\omega_{lp} = \sqrt{\frac{1}{L_2 C_o}} = 1.3\,kHz \tag{91}$$

The DC gain K_{DC} has an additional term, resulting in:

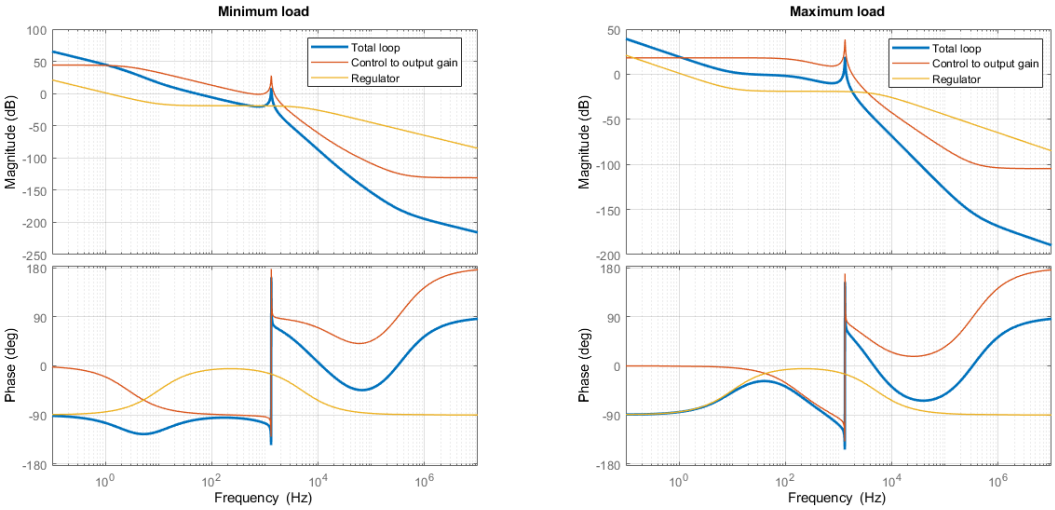
$$K_{DC} = \frac{G_{ctrl} V_o V_i}{2 R_{i1} P_i} \cdot \frac{R_{io}}{R_{bat}} = 44.2\,dB \tag{92}$$

The uncompensated-loop-gain is plot in the orange trace of Figure 52b, some parasitic resistance is considered in the low-pass filter. A regulator has design to meet a bandwidth of $\omega_c = 2\pi\,50\,rad/s$, the regulator response is plot in yellow trace. The closed-loop-gain results in the blue trace of Figure 51b. The phase margin at the crossing frequency $\omega_C = 2\pi 50\,rad/s$ is $pm = 80°$. The closed loop gain is then evaluated for the full-power condition, and it is presented in blue trace of the right plot. Can be seen that the crossover frequency, in this condition, shows large variation in value even with little change in the DC-gain of the loop. This is not a relevant issue, because the phase margin is sufficient in the entire range of variation of the crossover frequency. The zero location of the regulator is placed at $\omega_{zr} = \omega_c/5$ as a trade-off between the phase margin at the minimum load condition and the spread of the crossing frequency under the condition of full load.

***I_o*-loop 2^{nd} stage** This control loop comes into play if the battery is connected to the output of the converter, and at least the second stage is operating. When just the second stage is operating the situation corresponds to the one of Figure 49c, while, when both the first and the second stage are operating, the control scenario is depicted in the Figure 49a. The same considerations made for the output-current control of the first stage hold: the output current is sense through the hall-sensor ACS772LCB-100U, that exhibits a sensitivity of $R_{io} = 40\,m\Omega$. The equivalent series resistance of the battery is assumed $R_{bat} = 100\,m\Omega$, then the control of the output current $\hat{i}_o$ is obtained by controlling the output voltage $\hat{v}_o$ across the battery resistance. In the control of the output current by the first stage there is presence of the low-pass filter at the output, caused by the inductance and the capacitor of the second stage. Of course, for the output current control by the second stage the additional low-pass filter is no more present, and the closed-loop transfer function is easier.



(a)



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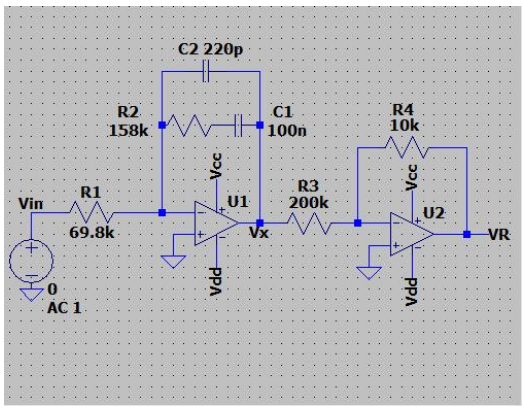
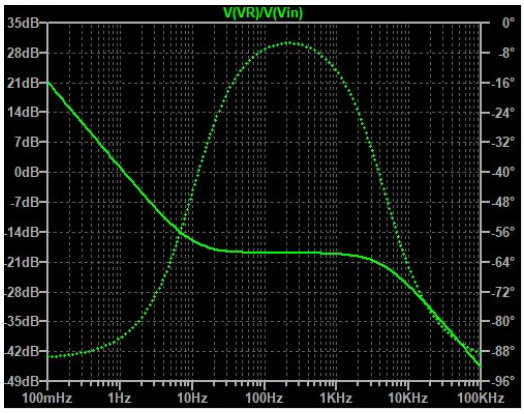


(c)



(d)

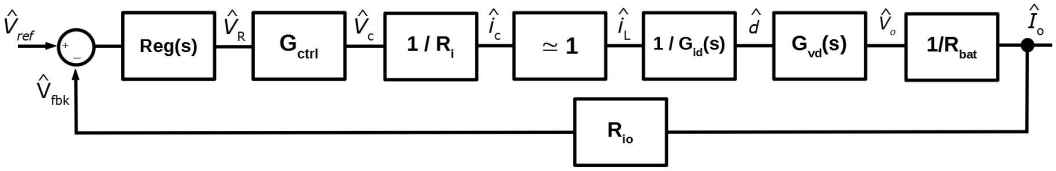
Figure 52: Block diagram of the I_o-loop for the first stage (a), bode plots of the uncompensated-loop-gain, regulator and compensated-loop-gain (b), regulator circuit and response (c)

The uncompensated-loop-gain follows from equation (89) and (92), once the term related to ω_{lp} is removed.

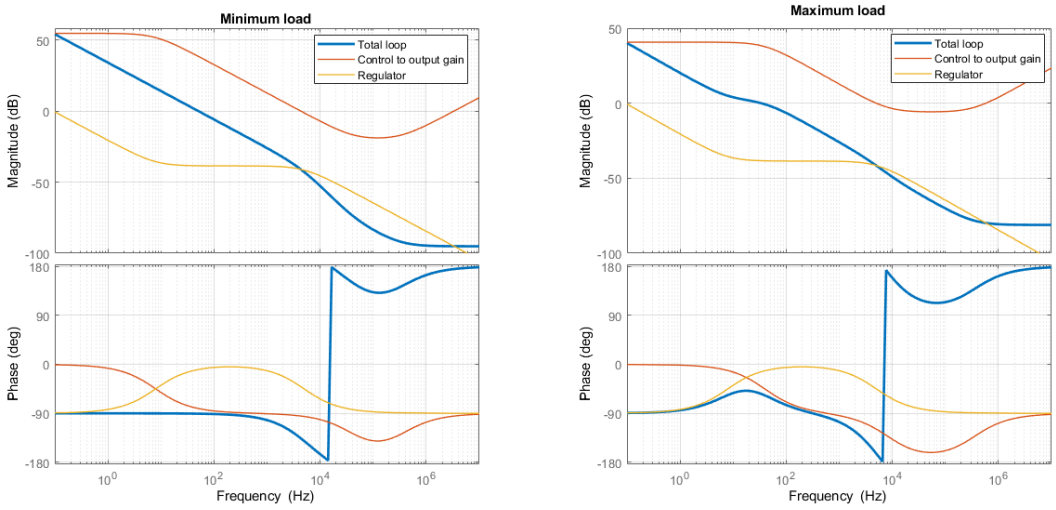
$$G_u \triangleq \frac{\hat{i}_o}{\hat{v}_R} = K_{DC} \cdot \frac{\left(1 + \frac{s}{w_z}\right)\left(1 - \frac{s}{w_{rhp}}\right)}{\left(1 + \frac{s}{w_p}\right)} \tag{93}$$

$$\begin{aligned} K_{DC} &= 54.7\, dB \\ \omega_p &= 50\, rad/s \\ \omega_{rhp} &= 268k\, rad/s \\ \omega_z &= 2M\, rad/s \end{aligned} \tag{94}$$

The closed-loop-gain results in the blue trace of Figure 51b. After the regulator design, the phase margin results $pm = 89°$ at the target crossing frequency of $\omega_c = 2\pi 50\, rad/s$. The closed loop gain is then evaluated for the full-power condition, and it is presented in blue trace of the right plot. The crossing frequency decreases to $33\, Hz$ and the phase margin is more than 90°, the regulator design is then accepted.



(a)



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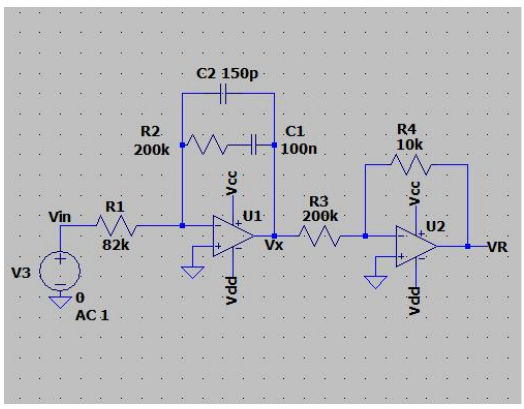

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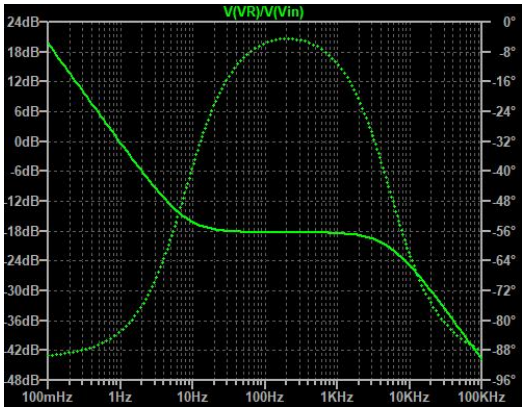


(d)

Figure 53: Block diagram of the I_o-loop for the second stage(a), bode plots of the uncompensated-loop-gain, regulator and compensated-loop-gain (b), regulator circuit and response (c)

4 Simulation

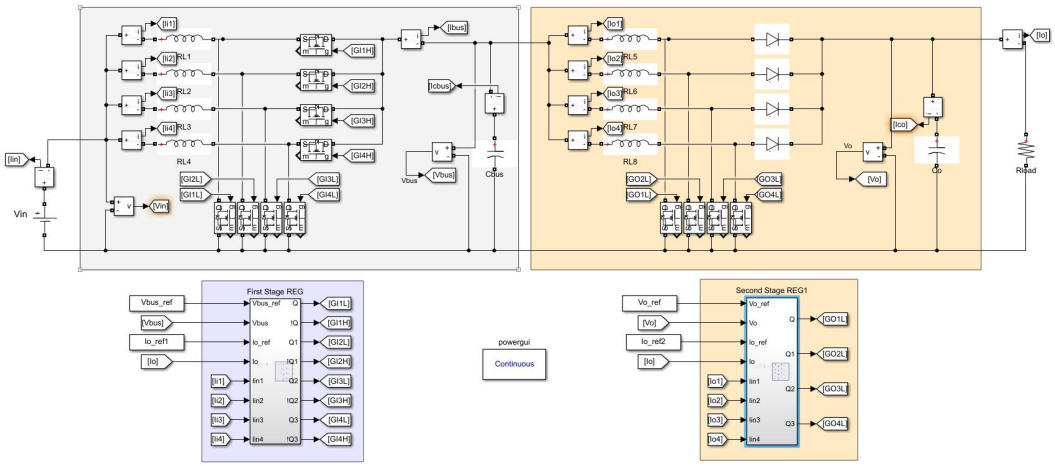
After the design phase of section 3, and before the prototype building, has carried out a simulation phase. The main purpose of the simulations are to validate the design, checking the steady state operation and the control of the stages. The simulation are carried out using Matlab and Simulink software.

4.1 Steady-state operation

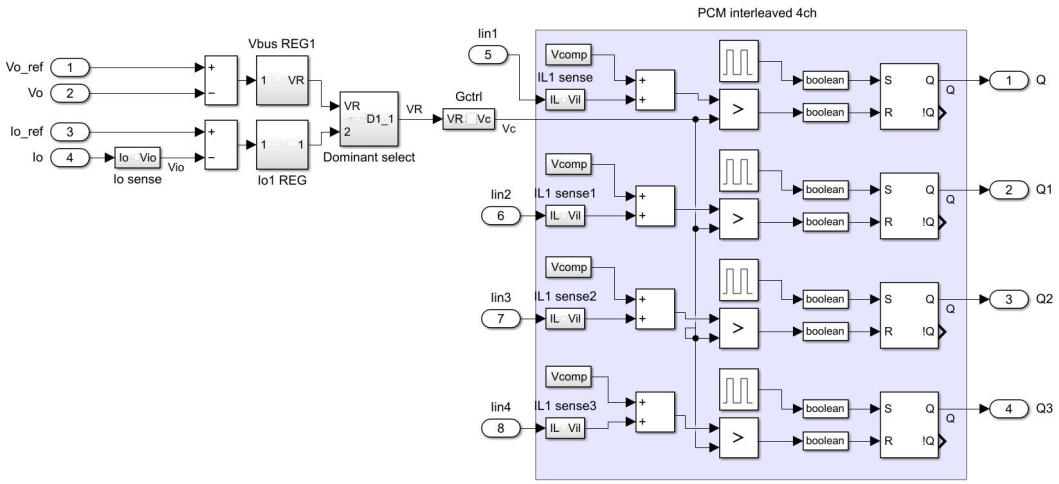
In the steady state analysis the main waveforms are checked, such as currents and voltages ripples. The tracking of the set-points are also investigated, further verification on the control are treated in the next section 4.3.

First has created the full model of the converter, shown in the figure 54a. The model has created out of the fundamental Simulink block such as MOSFETs, diodes and passives. The full PCM structure has been implemented, including the compensation ramp and the flip-flop that generates the driving signal for the MOSFETs. Also the automatic selection between the dominant feedback loop has been included, the control structure is visible in the Figure 54b.

A simulation was made in the operating point characterized by: $v_{in} = 46\,V$, $V_{bus,ref} = 300\,V$, $V_{o,ref} = 800\,V$ and $Pin = 4600\,W$. The results are presented in the Figure 55: first of all is verified the interleaving operation of the two stages. This operation point corresponds to the maximum duty cycles for the stages, since no sub-harmonic oscillations are presents in the inductors currents then the design of the compensation slopes are verified for both stages. The average value of the bus and the output voltage follow the reference values with sufficient accuracy, the voltage ripple waveforms are different to the classic boost waveforms because of the interleaving effect. The ripple amplitude was designed considering no interleaving effect, then from simulation makes clear that the interleaving effect strongly reduces both the bus and output voltage ripple amplitudes.

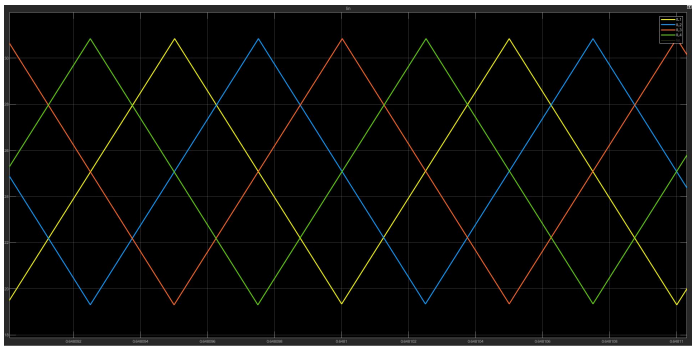


(a)

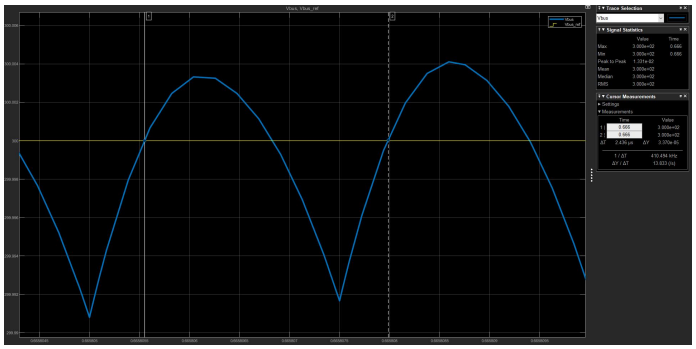


(b)

Figure 54: Simulink model of the converter (a) and the control subsystem (b)



(a)



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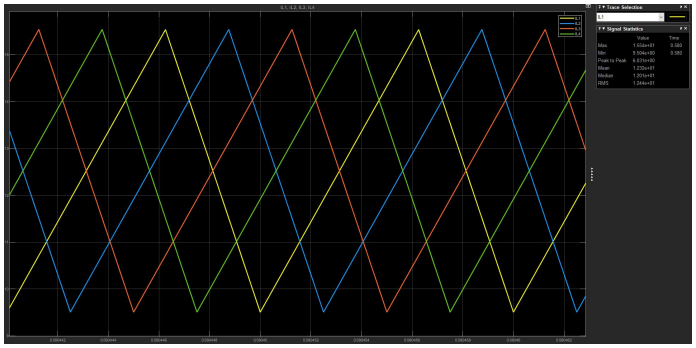

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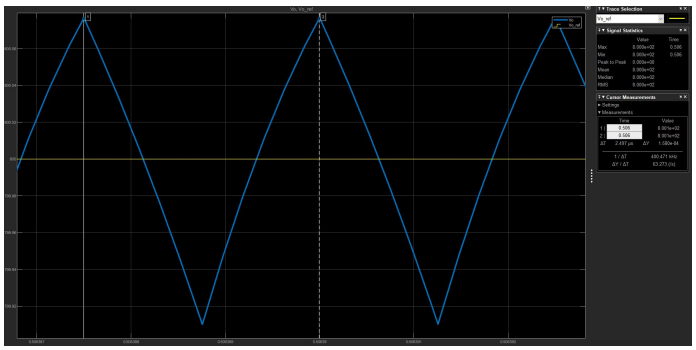


(d)

Figure 55: Simulated steady state waveforms: currents ripple of the input stage (a), bus voltage ripple (b), currents ripple of the output stage (c) and output voltage ripple on resistive load(d)

4.2 Stability analysis

The firs purpose of this analysis is to validate the theoretical loop gain, used to design the regulators in the previous section 3.4. The Linearization app of Simulink is used to linearize the model of the converter, and to measure the simulated frequency response. The second stage has been simulated, it has been put in open-loop operation and than a test signal was injected into the V_R point. The resulting perturbation on the output voltage is measured for different frequencies. First a single leg of the output stage was simulated, the frequency response of the uncompensated loop gain is presented in the figure 56. The operative conditions of the simulation are $V_{bus} = 300\,V$, $V_o = 800\,V$ and $P_o = P_{nom}/4$. The predictions from theory for this operating point are:

$$K_{DC} = 50\,dB \tag{95}$$

$$\omega_p = 250\,rad/s \tag{96}$$

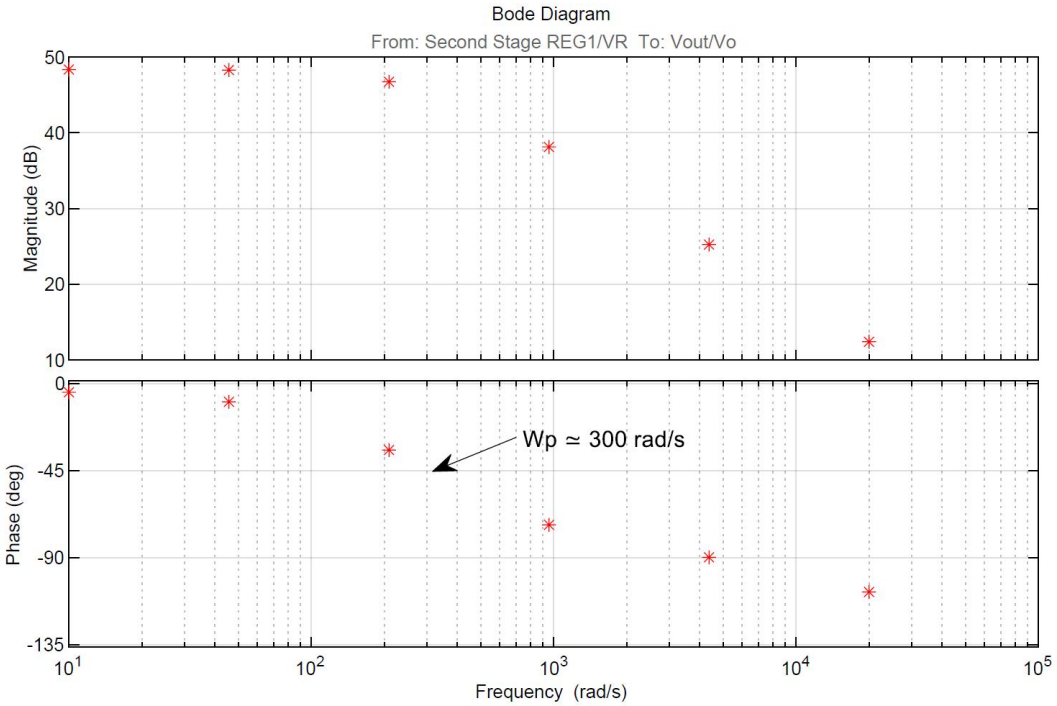


Figure 56: Simulated uncompensated-loop-gain of a single phase of the output stage

Can be seen that the simulated DC gain is closed to the one predicted by equation (82). The dominant pole locates at about $300\,rad/s$ that is reasonably close to the predicted angular frequency of $250\,rad/s$. Can be concluded that the model used to design the regulators is validated by simulation.

To investigate the effect of the interleaving, the previous simulation is repeated with all the four legs operating. The result of the simulation is presented in the figure 57. The DC-gain is not modified by interleaving, on the other side the dominant pole is pushed up to $1\,kHz$. This coincides with the theoretical prediction, in fact the dominant pole relies on the output capacitor ant the equivalent output resistance. In this simulation, with all the four phases active, the output capacitor is unchanged but the output resistance is four times smaller. The consequent increase by a factor four of the dominant pole is coherent with the expectations.

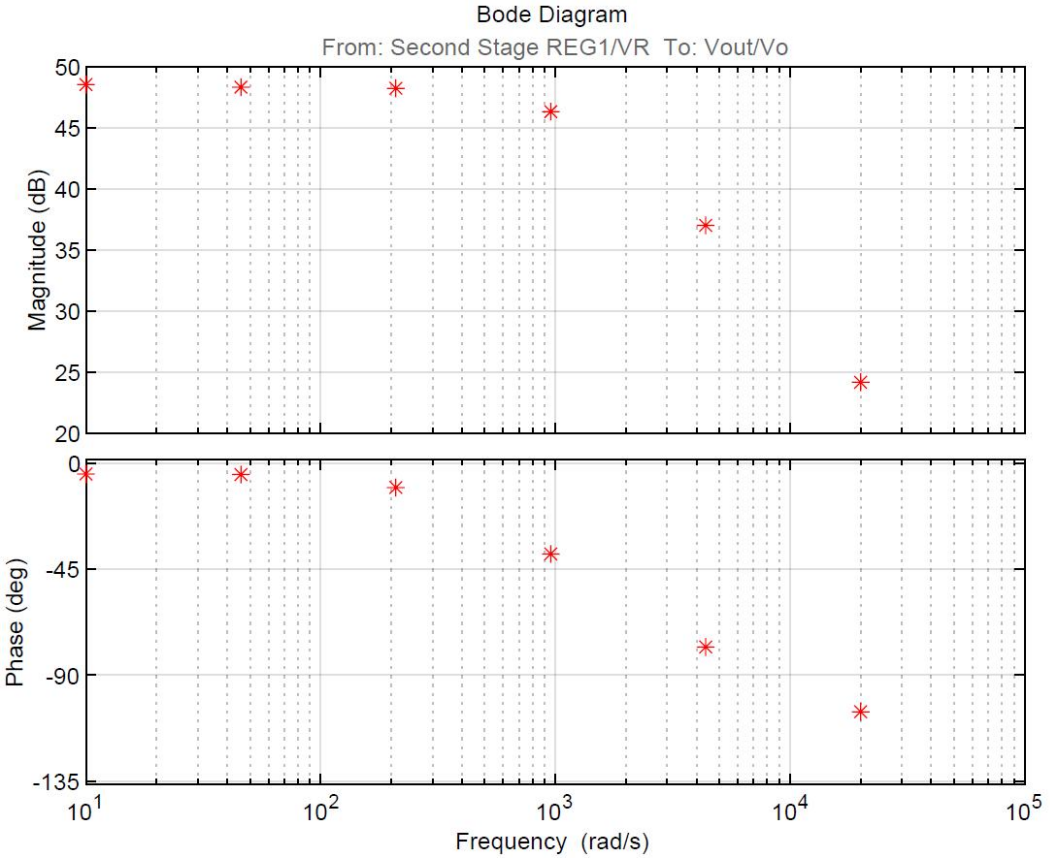
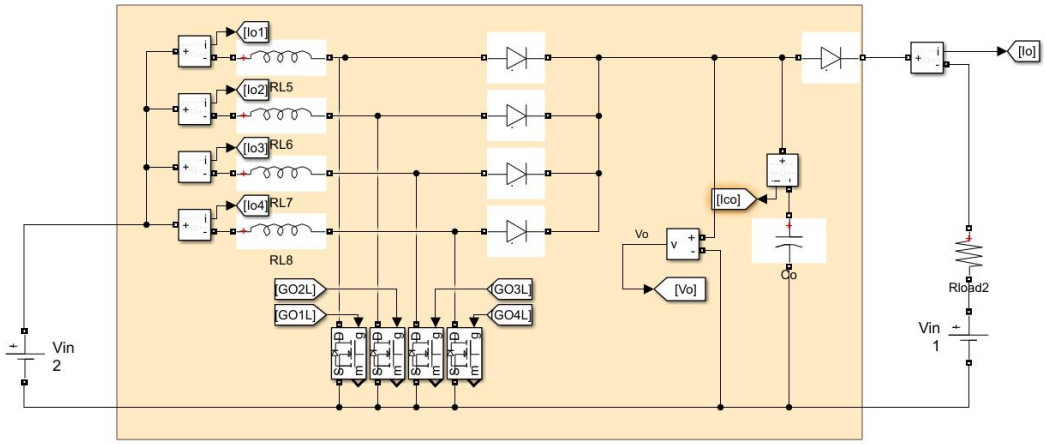


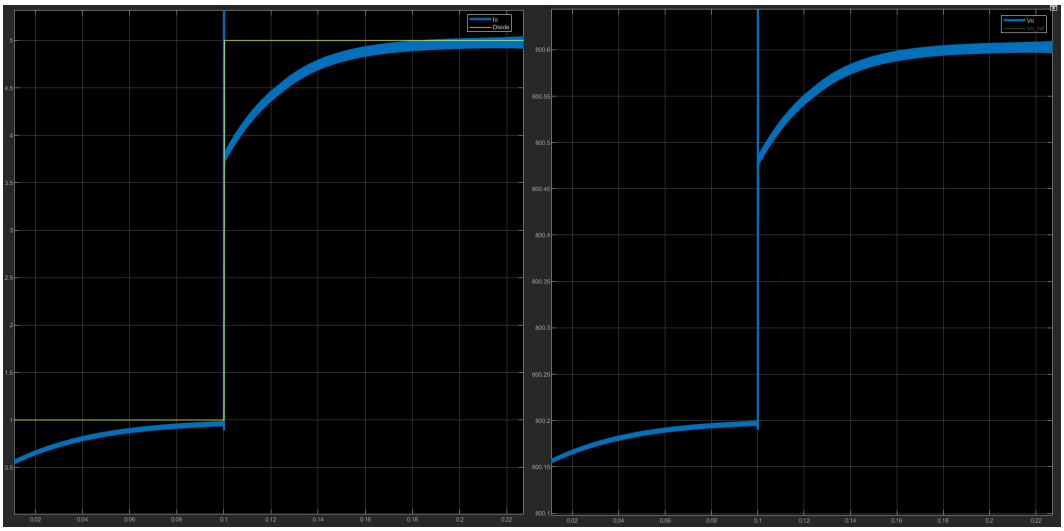
Figure 57: Simulated Uncompensated-loop-gain with four phases, output stage

4.3 Output current control

For this simulation the second stage is used and the second stage output-current control loop is tested. The model used in simulation is the one of figure 58a, in which is visible the modeling of the battery as a voltage generator and a series resistance. The series resistance is $R_{bat} = 100\,m\Omega$ and the equivalent generator is set to $V_{bat} = 800\,V$.
The simulation is intended to verify the response of the control loop to a step change of the reference value for the output current. In particular the reference output current is stepped from one to five amperes, the response of the output current and the output voltage is observed.
The simulation results are presented in the figure 58b: as the current reference is increased, the output voltage increases till the output current reaches its new reference value. The behavior resembles a first pole system response and the designed is confirmed. The output current is well regulated to its reference value.



(a)



(b)

Figure 58: Simulation of the control of the input current

5 Experimental validation

During the very first tests on the prototype, the functionality of the converter have analyzed and no evident issues has found. Control loops work as expected from the design, the control is manteined through the entire range of variation of the input and output voltage, as well as the output power. The switching frequency have been lowered from the target $100kHz$ to $70\,kHz$. The switching frequency have lowered mainly because of the switching losses, with a lower frequency the efficiency of the prototype results higher. The inductor ripple increase by the same factor the switching frequency is decreased, by the way this has found to be a good trade-off. The most important measure to perform on the prototype are the verification of the equal split of the current between the phases of the input boost stage, and the evaluation of the efficiency of the converter. The current split is investigated in the following section 5.1, while the efficiency is investigated and optimized in the section 5.2.

5.1 Current sharing between phases

The current split between the phases are a relevant aspects to evaluate in the input boost stage, since the input current magnitude is relevant. An unequal distribution of the current between the phase would causes a not uniform distribution of the heat between the components, increasing the stress and then the failure rate. From the point of view of the control, PCM controller have been used with the current reference common to all the phases of the stage. This should ensure that the inductors currents have the same peak value, then the average value of the inductors currents can be unbalanced only because of mismatching in the inductors current ripple amplitude or, in other words, because of the mismatch in the inductance value between the phases. The inductors are realized by the supplier with 10% maximum tolerance, so difference in the average currents of the phases is expected to be less than 20%.

Phase current	**Average value**	**Ripple pk-pk**
I_{L1}	$3.293\,A$	$7.876\,A$
I_{L2}	$3.305\,A$	$7.829\,A$
I_{L3}	$3.221\,A$	$7.891\,A$
I_{L4}	$3.224\,A$	$7.829\,A$

Table 16: Current sharing between the phases of the input boost.

Figure 59 shows the acquisitions for the current of the four phases of the input boost stage. The traces data are elaborated with MATLAB to extract the

parameters of the waveforms, listed in Table 16: the average current splitting is well realized, the higher average phase current is just 2.6% higher than the lower one. The output boost stage has asynchronous structure, so the current sharing is straightforward. The sharing has verified with measurements but the results are not reported.

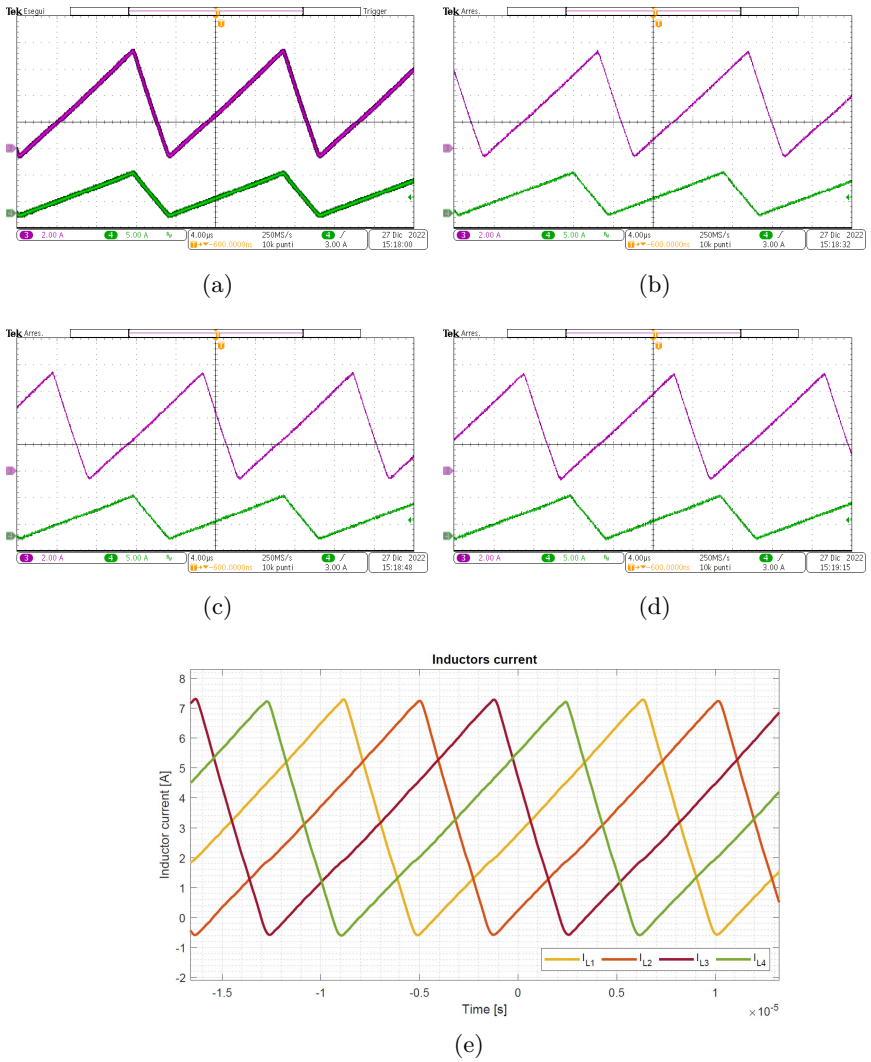


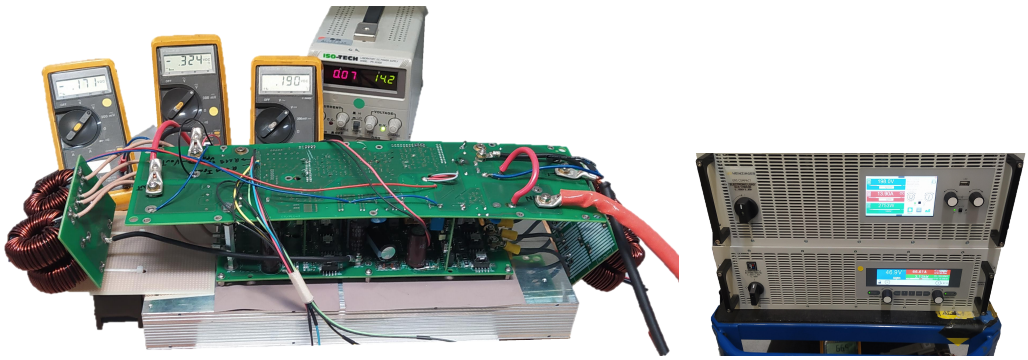
Figure 59: Inductors current of the input stage, the phase shift of the interleaved structure is visible

5.2 Efficiency optimization

The converter is design to cover a wide range of input and output voltages. According to the operating conditions, only one stage or both stages can operate, to keep the efficiency as high as possible. The verification steps on the prototype are the following:

- Investigate in which conditions the input stage can operate on its own.
- Investigate in which conditions the output stage can operate on its own.
- Investigate when it is convenient (or necessary) to operate both stages, for this conditions found the V_{bus} voltage that maximize the total efficiency.

The measurements setup is composed by a "EA-PSB 9500-90" power-supply and a "EA-ELR 11000-80" electronic load, set in constant current mode. The input, the bus and the output voltage are measured directly on the PCB board, to avoid the voltage loss along the power cables and connectors. Three multimeters "FLUKE 75" are used to this purpose. During initial tests, the input and the output current were measured through two external shunt devices. This readings matched with the indications of the displays of the instruments so good that the display readings was used as current measurements in the efficiency measurements. The test bench for the efficiency measurement is shown in the Figure 60. Some constraints are imposed by this setup: the electronic load can absorb a maximum power of $11\,kW$, while the generator can supply a maximum current of $90\,A$. More powerful equipment are of course present in the company, but at the moment of the test they were used in long-lasting tests of another product, taking some weeks. The converter is then tested according to the power limitations aforementioned.



(a) (b)

Figure 60: Setup for the measurement of the efficiency of the converter

The converter efficiency have been measured for different input voltages: 46, 115, 180 and 250 V. For every input voltage, the output voltage have been set to 200, 400, 600 and 800 V. For every set of voltages ($V_{in} - V_o$), all the possible configuration was tested: only the first stage working, only the second stage working or both stages working. This allows to determine the most efficiency setup for every ($V_{in} - V_o$) set. Please note that the first stage can't generate output voltage greater than 300 V, therefore the output voltages in the range $300V - 800V$ always requires the operation of the second stage, on its own or combined with the first. For the configuration in which both stage were operating, the bus voltage V_{bus} was adjusted till the maximum efficiency was reached, than the efficiency value was recorded. The determination of the most efficient stage-configuration and the determination of the most efficient bus voltage corresponds to the efficiency-optimization process.

In the Table 17 are listed the measurements collected to optimize the efficiency. The right column reports the output power of the converter during the tests, due to the limitation of the instruments the test-power P_{test} is about 75% of the nominal power of the converter. The conditions marked as "NP" are the condition in which the converter results not capable to operate: the losses prevents the stage to reach the output voltage set-point. This conditions are of interest because highlight the limitation in the voltage gain of the stages.

The outcome of the results collected in table 17 allows to operate the converter in its maximum efficiency configurations depending on the input and output voltage:

- When the input voltage is in the low range $46 - 180$, and consequently the current is high, than the operation of the input stage is mandatory. The second stage can't handle such an high current and its voltage gain results extremely reduced. This is confirmed by the "NP" labels when the second stage is tested in standalone mode. The first stage standalone is preferred whenever the output voltage is set to 200 V
- When the output voltage increases above $300V$ the first stage can no longer operate standalone. The second stage is preferred only when the input is 250 V and the output is 400 V.
- In all the other conditions, the most efficient operation includes both stages operating in cascade.

Table 17: Measurements for the efficiency optimization

Vin Ref [V]	Vo Ref [V]	1st	2nd	Vbus [V]	Eff [%]	Po [kW]
46	200	☑	☐	185	95,59%	3,8
		☐	☑	NP		
		☑	☑	96	95,87%	
	400	☑	☑	185	95,02%	
	600	☑	☑	185	94,05%	
	800	☑	☑	185	93,01%	
115	200	☑	☐	-	97,34%	9
		☐	☑	NP		
		☑	☑	165	96,52%	
	400	☑	☑	245	96,75%	
	600	☑	☑	212	95,67%	
	800	☑	☑	245	95,19%	
180	200	☑	☐	-	97,60%	11
	400	☐	☑	NP		
		☑	☑	245	97,18%	
	600	☑	☑	245	96,49%	
	800	☑	☑	265	95,68%	
250	400	☐	☑	-	97,60%	11
		☑	☑	275	97,53%	
	600	☐	☑	-	96,97%	
		☑	☑	300	97,17%	
	800	☐	☑	NP		
		☑	☑	265	96,08%	

NP = not possible

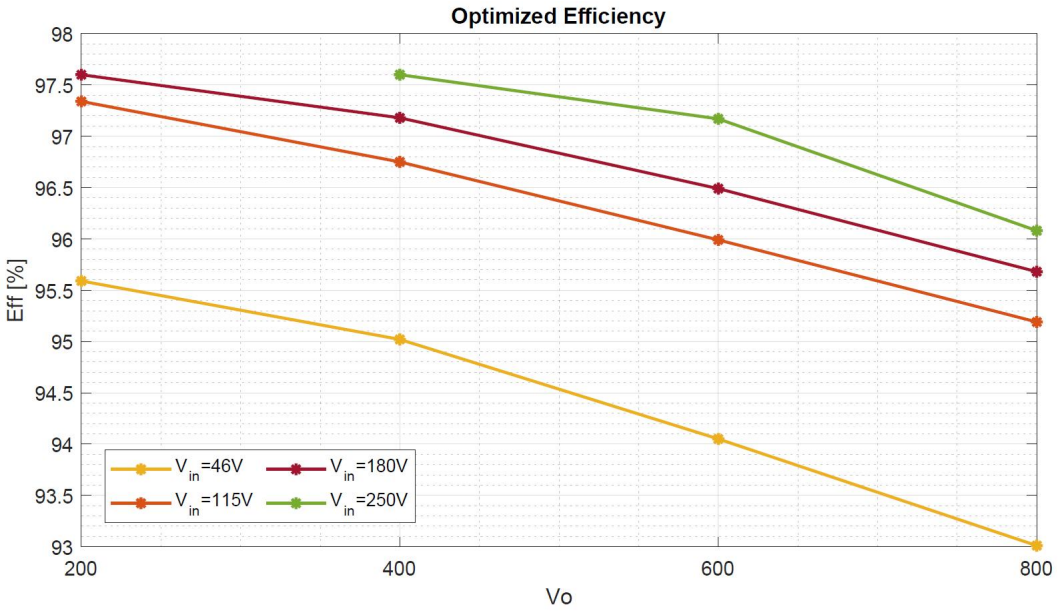


Figure 61: Optimized efficiency over output voltage

The optimized efficiency profiles are presented in the Figure 61: once set the input and the output voltage of the converter, the plot provide the converter optimized efficiency at P_{test}.

The efficiency of the converter have been further investigated, by analyzing the dependence of the efficiency over the output power. For six operating points (V_{in},V_o), the output power is stepped from $0.2P_{test}$ to P_{test} and the optimized efficiency have been recorded. The results are visible in the plot of Figure 62, the output power is normalized to the nominal test power P_{test}.

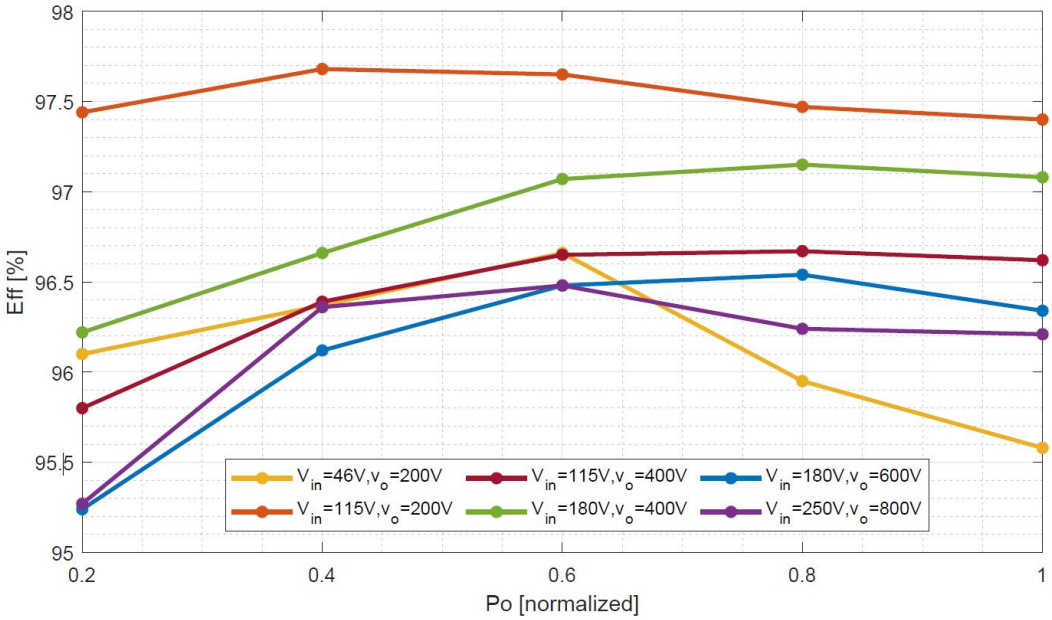


Figure 62: Relation between efficiency and output power

6 Conclusions

The project of this document has been developed during the thesis activity at the Power Control System company. The project was committed by a fuel cell manufacturer, and it is intended to interface a wide range of fuel cell stacks and vehicle batteries. Therefore, this converter experiences wide range of input and output voltages, depending on the combination of the stack voltage and the battery voltage. The project is not oriented towards obtaining the maximum efficiency at a specified operating point, but it is rather optimized to provide good efficiency within the entire operating range.

The design phase started by evaluating different topologies for the converter structure, highlighting their strength and weakness. The selected topology is a trade off between complexity and performances, and it composes of two separated stages placed in cascade. Depending on the operating point of the converter, only the first, only the second or both the stages can be active. This strategy achieves good efficiency in the entire working range by an active-setting of the operation of the stages.

The industrialization of the device played a crucial role. This converter is a commercial product and the company experience as power converter manufacturer helps to identify and optimize first order aspects such as components price, mounting cost and components availability. The selection of the power MOSFETs and the power diodes represent the most challenging aspects in keeping the price low. The magnetic components design, instead, were the most challenging aspect from the industrialization point of view. Particular effort has been placed in the cooling of the magnetic power components.

The PCB designers of the company play active role in the design process, highlighting physical constraints and realizing the first series of prototypes. With experimental measurements, the maximum efficiency configuration is investigated for every operating condition. The result is a maximum efficiency profile, that defines the optimal operation of the the two stages according to the input and the output voltages. The optimized efficiency profile will be implemented in the future control strategy of the microcontroller that manage the converter.

The result of this thesis activity is the realization of a non-isolated DC-DC converter that fully satisfy the initial requirements. The converter is optimized for the production, it also allows the realization of modular structures since it exhibits the intrinsic ability to work in parallel with other identical converters.

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